MAY 1980 Volume 5, Number 5 $2.50 in USA/$2.95 in Canada

BYTE®

the small systems journal

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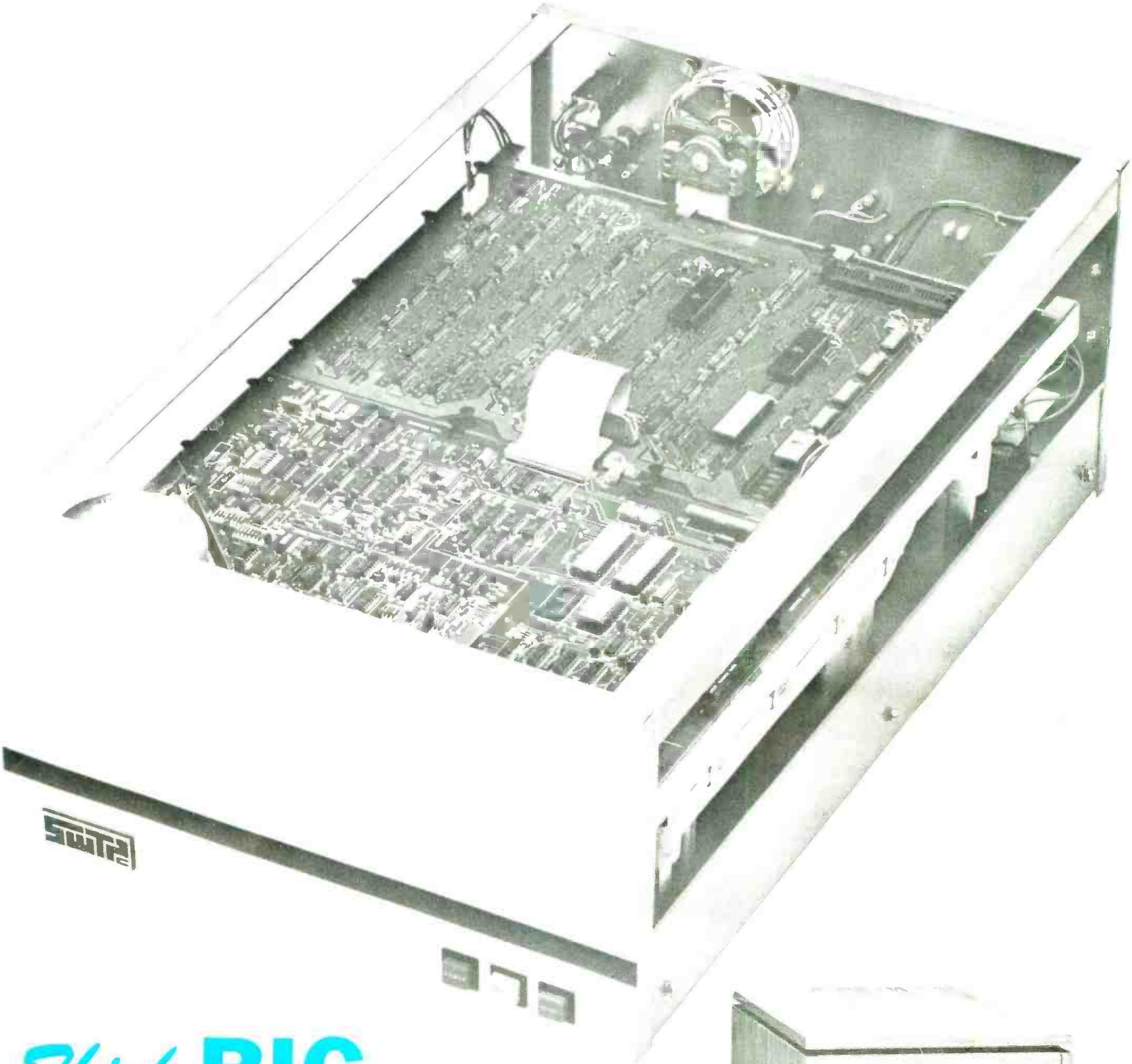
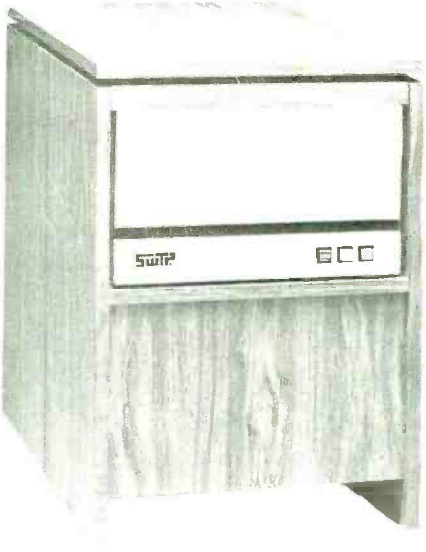
FLOPPY DISKS





Low-cost hard disk computers are here and field proven

11 megabytes of hard disk and 64 kilobytes of fast RAM in a Z80A computer for under $10K. Two floppy drives, too. Naturally, it's from Cromemco.

It's a reality. In Cromemco's new Model Z-2H you get all of the above and even more. With Cromemco you get it all.

In this new Model Z-2H you get not only a large-storage Winchester hard disk drive but also two floppy disk drives. In the hard disk drive you get unprecedented storage capacity at this price—11 megabytes unformatted.

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You get expandability, too. The high-speed RAM can be expanded to 512 kilobytes if you wish.

And the computer has a full 12-slot card cage you can use for additional RAM and interface cards.

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With the Z-2H you also get the broadest software support in the microcomputer field. Software Cromemco is known for. Software like this:

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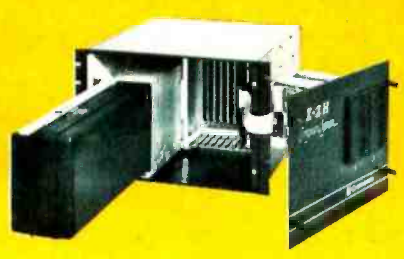
- **FORTRAN IV**
- **RATFOR (RATional FORtran)**
- **COBOL**
- **Z80 Macro Assembler**
- **Word Processing System**
- **Data Base Management**

with more coming all the time.

SMALL, RUGGED, RELIABLE

With all its features the new Z-2H, including its hard disk drive, is still housed in just one compact cabinet.



Hard disk drive at lower left can be interchanged just by sliding out and disconnecting plug. Seven free card slots are available. Z-2H includes printer interface card.

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In The Queue

BYTE May 1980
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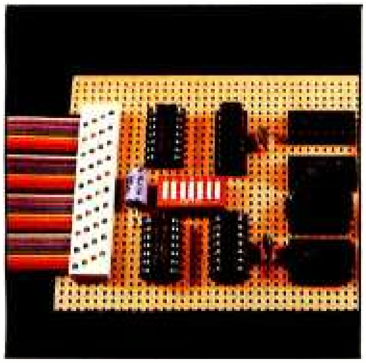
page 6



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ON LAST MONTH'S COVER

The April cover, which has received so many compliments, was a creation of the photographic artistry of Ed Crabtree. Ed is a professional commercial photographer in Peterborough, N H and has been BYTE's photographer from day one. This was Ed's first BYTE cover. We're sure it won't be his last.

Foreground

Background

Nucleus

ON THE COVER

On May's cover, Robert Tinney has formed an abstraction of the most important medium of mass storage in today's era of small computers, the floppy disk. Heightening its shimmering mystery, we find a disk wavering in the heat above some desert landscape. To enlighten you, this issue features several articles that present valuable information about floppy-disk technology. This technology is no mirage — it will even work well in a similar, hot environment of East Africa, as the editorial on page 6 describes.

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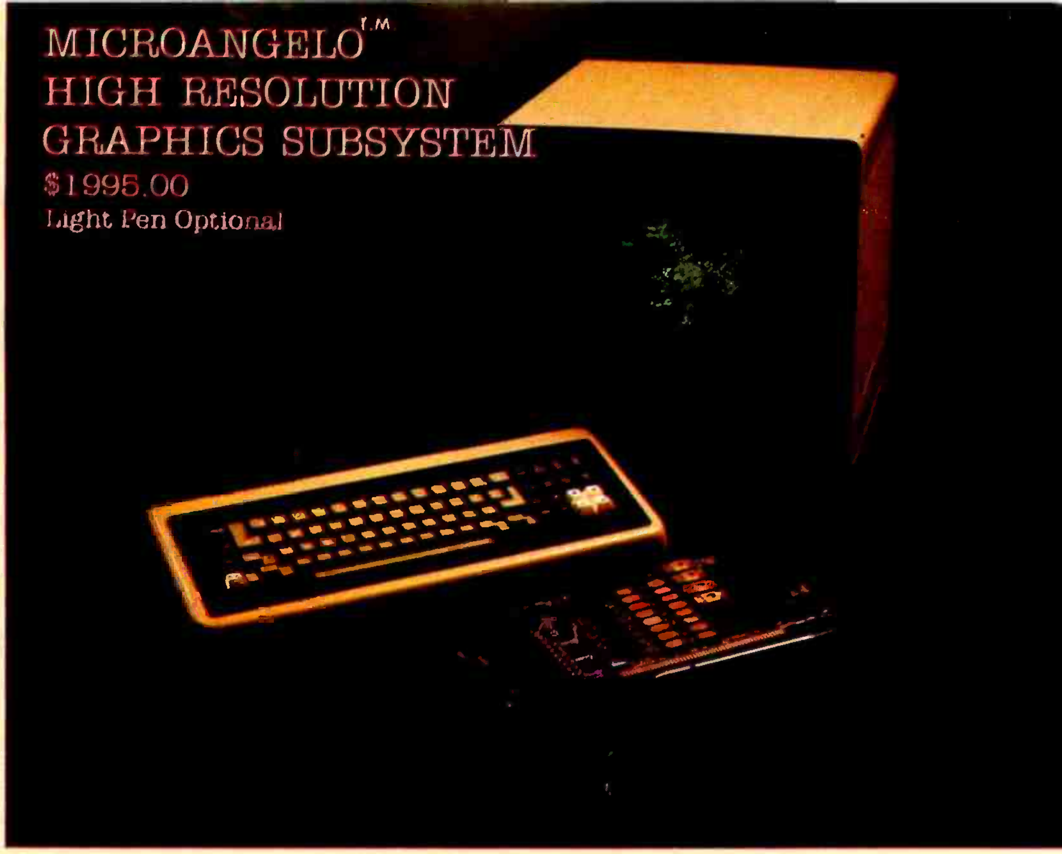

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Computer-Controlled Viewing of the 1980 Eclipse

by Carl Helmers

As noted in the March 1980 editorial, I traveled to Kenya in East Africa to observe the 1980 total solar eclipse with an Apple II Pascal system controlling the photographing of the event. This month's editorial is a commentary about the experience. This commentary was written upon my return to New Hampshire a week after the eclipse.

The final preprations for the Kenya eclipse of 1980 were made in an intensive session of 24-hour workdays, February 2, 3, 4, and 5. One physiological consequence of no sleep for 3 or 4 days is that when traveling through 8 time zones there is no possibility for jet lag! One's body is so tired that all memory of the previous time zone is erased completely. Norm Whyte and Laurel Allen, who coordinated many of the details of the trip to Kenya, arrived in Boston from California on the second of February and spent the weekend at my home. During this final weekend's activity, we each had several chores to finish. One detail, for example, was making sure that both computers would operate simultaneously off Norm's portable Honda AC generator. Another was adding a hardwood extension to Norm's telescope mount so that my camera could be attached along with his.

In connection with the program design of my experiment, a number of crucial points had to be verified. With the time allocation procedures completed as described in the March 1980 editorial, writing the real-time procedures to execute the time line proved trivial. These were the procedures left in dummy form in the listing 1 published with the March 1980 editorial. In listing 1 accompanying this editorial, readers will find the final form of the program I used. In approaching this final form I implemented the execution routines using a module named "milli" to carry out time delays of an integer number of milliseconds. The program itself was verified by driving the camera interface using a first approximation to "milli" in the form of Pascal dummy loops used to count time.

Originally I hoped that (by fortuitous circumstance) I could use some combination of Pascal statements in a loop to provide time delays in units of milliseconds. But, after perhaps an hour of fooling with various combinations, I came to the conclusion that this would not be possible. I was either 6% too slow or 6% too fast depending on whether or not I put a unary negation in a timing loop's dummy assignment statement.

Since program development time was limited by a departure schedule, it soon became apparent that the lesser of two evils (imprecision or assembly language) was to write an assembly-language routine called "milli" that links to Pascal with a single integer parameter specifying a loop delay time in milliseconds. I finished this necessary step sometime in the wee hours of February 4. I checked the accuracy with various simple test programs written in Pascal. Of course, my timing assumption was that zero time would be spent outside of "milli" executing the Pascal code of the actual program. This assumption was verified with test runs of the whole eclipse photography sequence, which showed about 1% error. By adjusting the constants in the delay routine slightly, this error was compensated at the gross level of the entire eclipse sequence's 241-second execution time.

Text continued on page 52

"After working all day with the computer at work, it's a kick to get down to Basic at home. And one thing that makes it more fun is my Shugart minifloppy™. We use Shugart drives at work, so when I bought my own system I made sure it had a minifloppy drive.

"Why? Shugart invented the minifloppy. The guys who designed our system at work tell me that Shugart is the leader in floppy design and has more drives in use than any other manufacturer. If Shugart drives are reliable enough for hard-working business computers, they've got to be a good value for my home system.

"When I'm working on my programs late at night, I can't wait for cassette storage. My minifloppy gives me fast random access and data transfer. The little minidiskettes™ store plenty of data and file easily too.

"I made the right decision when I bought a system with the minifloppy. When you lay out your own hard-earned cash, you want reliability and performance. Do what I did. Get a system with the minifloppy."

If it isn't Shugart, it isn't minifloppy.

Shugart

435 Oakmead Parkway, Sunnyvale, California 94086

See opposite page for list of manufacturers featuring Shugart's minifloppy in their systems.

Information on Potter Printer Needed

Can a reader of BYTE help me? I recently purchased a printer from salvage, and I hoped to obtain documentation and a schematic diagram from the manufacturer.

The printer is a Potter Model LP-3000, manufactured by the Potter Instrument Company, formerly of Plainville, New York. I called the firm, and I was told:

1) The company is in the process of moving to New Hampshire.
2) This particular model of printer is obsolete.
3) They have no documentation or schematic for this model.

From my examination of the circuits and machinery, I believe the Potter LP-3000 is a daisy-wheel type with a serial data input. However, whether it uses ASCII or not, I can't tell.

Can someone tell me how I can interface this printer to my Radio Shack TRS-80 Model I Level II computer with expansion interface?

Nick Tountas
838 Juniper Rd
Glenview IL 60025

Questioning "Affordable"!

When you are on Social Security, an affordable computer system that costs $6000 is like "# @ * "! When your monthly income is $360, to have an editor smugly talk of plunking down $6000 cash as if it were a minor outlay tends to be *very* irritating.

On top of that, the system Mr Helmers described is just the sort (with minor modifications) I have wanted for ages. Another thing that hurts is the industry-wide disinclination to even consider time payments or credit. I know that I'll have to wait, and probably wait over 5 years, but maybe not. If I were just disgusted with your editorial, I wouldn't have bothered to write. What I would like to know is if any BYTE reader knows of a way I can obtain such a system as Mr Helmers described — perhaps secondhand — without paying thousands of dollars cash? By squeezing, I can afford $100 a month now, and by July I should be able to afford $150 a month, perhaps more.

In a way, I have to thank Mr Helmers for that editorial. It made me mad enough to write, and perhaps there is a solution to my problem.

Fred J Remus Jr
POB 2453
San Diego CA 92112

Carl Helmers Replies

*Give the industry time. Five years ago, the same system might have been well in excess of $30,000, with inferior programming languages and comparable on-line storage capacity. Tremendous strides have been made in the past 5 years, and we can expect a certain leveling-off of prices in the future as mass production at 100,000 unit levels per year starts becoming reality. And then, of course, one looks at it from the point of view of increasing demand for these products. If we do not write about the conception of a good machine, we have no interest on the part of users....*CH

Gomoku

I was interested in the "Programming Quickie" by John Allwork ("BASIC Game: GOBANG," November 1979 BYTE, page 56) for Gobang is also called "Gomoku." There has been a competition running for Gomoku programs since 1975; I am the current champion. People interested in the contest should contact:

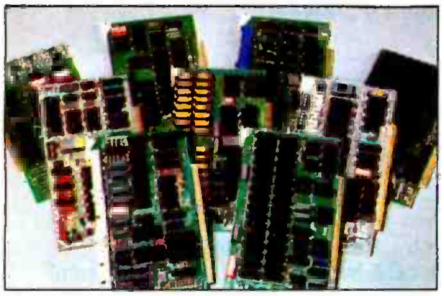
Shem Wang
Dept of Computer and Information Science
University of Guelph
Guelph, Ontario, CANADA

So far my different programs have run on large mainframe computers, but I hope to have one working on my North Star microcomputer for the next round of competition.

Mike Compton
196 Metcalfe St, Apt 810
Ottawa, Ontario
K2P 1P8 CANADA

At Intersystems, "dump" is an instruction. Not a way of life.

(Or, when you're ready for IEEE S-100, will your computer be ready for you?)



We're about to be gadflies again.

While everyone's been busy trying to convince you that large buses housed in strong metal boxes will guarantee versatility and ward off obsolescence, we've been busy with something better. Solving the *real* problem with the first line of computer products *built from the ground up to conform to the new IEEE S-100 Bus Standard*. Offering you extra versatility in 8-bit applications today. And a full 16 bits tomorrow.

We call our new line Series II.™ And even if you don't need the full 24-bit address for up to 16 megabytes (!) of memory right now, they're something to think about. Because of all the performance, flexibility and economy they offer. Whether you're looking at a new mainframe, expanding your present one or upgrading your system with an eye to the future. (Series II boards are compatible with most existing S-100 systems and *all* IEEE S-100 Standard cards as other manufacturers get around to building them.)

Consider some of the features: Reliable operation to 4MHz and beyond. Full compatibility with 8- and 16-bit CPUs, peripherals and other devices. *Eight* levels of prioritized interrupts. Up to 16 individually-addressable DMA devices, with IEEE Standard overlapped operation. User-selectable functions addressed by DIP-switch or jumpers, eliminating soldering. And that's just for openers.

The best part is that all this heady stuff is available *now*! In our advanced processor—a full IEEE Bus Master featuring Memory Map™ addressing to a full megabyte. Our fast, flexible 16K Static RAM and 64K Dynamic RAM boards. An incredibly versatile and economical 2-serial, 4-parallel Multiple I/O board. 8-bit A/D-D/A converter. Our Double-Density High-Speed Disk Controller. And what is undoubtedly the most flexible front panel in the business. Everything you need for a complete IEEE S-100 system. Available separately, or all together in our new DPS-1 Mainframe!

Whatever your needs, why dump your money into obsolete products labelled "IEEE timing compatible" or other words people use to make up for a lack of product. See the future now, at your Intersystems dealer or call/write for our new catalog. We'll tell you all about Series II and the new IEEE S-100 Bus we helped pioneer. Because it doesn't make sense to buy yesterday's products when tomorrow's are already here.

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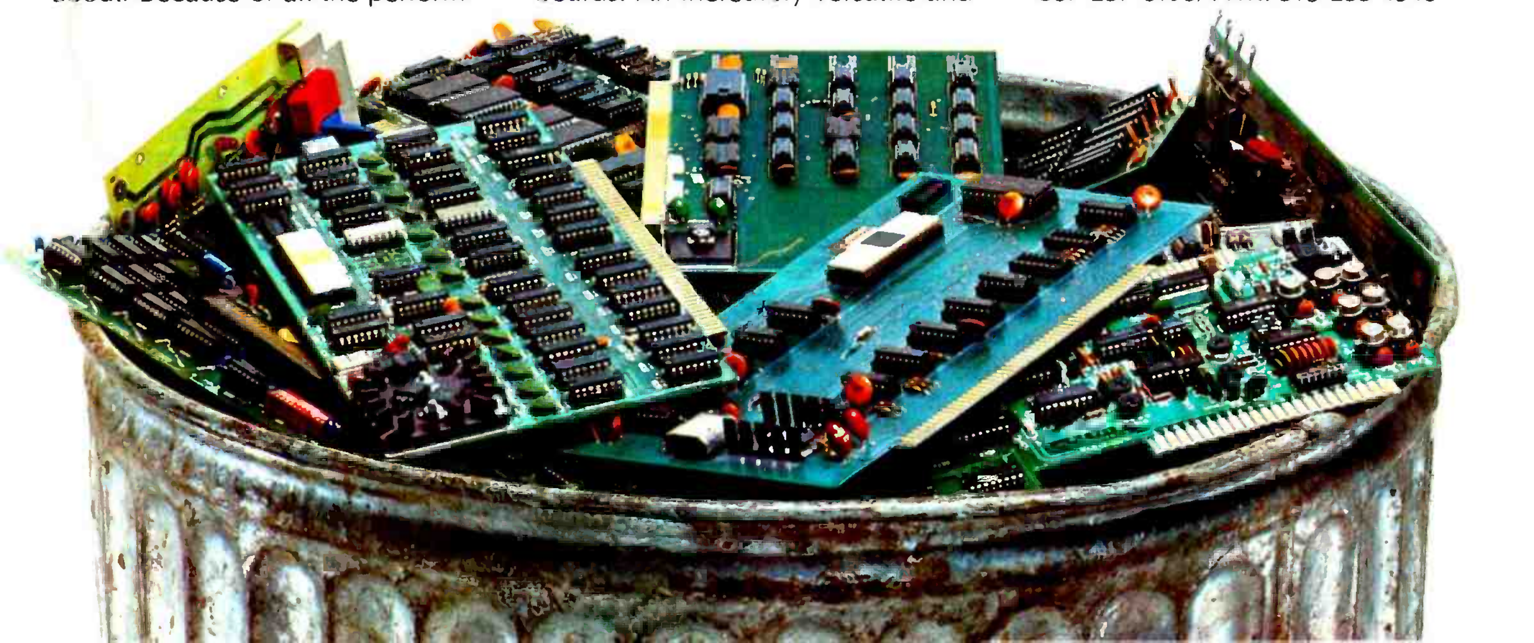

Searching for FORTRAN Compiler

I am an avid reader of BYTE and I believe that one of my fellow readers may be able to help me with a problem.

My school is thinking about expanding the courses that are offered in the area of computer science. It is hoped that an extensive course in FORTRAN programming may be offered.

Our computer is a CIP/2200 manufactured by the Cincinnati Milacron Corporation. It has a small disk-operating system and a card reader. The word size is 32 bits, and, at this point in time, the memory size is 32 K bytes. There are plans, however, to expand the memory to 64 K bytes by the time the FORTRAN course is offered.

My problem is that the Cincinnati Milacron Corporation does not make a FORTRAN compiler for our machine. I would like to know if any reader of BYTE could suggest any companies that might sell a compiler that is compatible with our machine.

Daniell B McCormick
Box 675
Presbyterian College
Clinton SC 29325

Seeking Computers for the Blind

Does any reader of BYTE know of a source for a computer system that uses audible output instead of characters displayed on a terminal for its customary interaction with the user, such as that produced by the Votrax speech interface? Such a computer system would be used by blind people. It would be desirable if a BASIC interpreter that used audible output were included.

If anyone has or knows of such a system, please contact me.

Walter F Keleher
56 Robin St
Rochester NY 14613

Altair BASIC Patch Needed

I wonder if any BYTE readers could assist me in locating the patch to Altair 8 K 4.0 Version and Altair Extended 4.0 Version BASICs which will allow these BASICs to run on a Z80.

I recently purchased a TDL ZPU which uses the Z80. The manual notes this incompatibility stating that Altair BASIC "has as part of its routines several occasions where the parity flag is checked as part of the function. In the Z80 the parity flag indicates OVERFLOW during math routines, not parity." The manual states that it contains a patch in Appendix C, but no Appendix C is included.

If any reader of BYTE knows where this patch may be obtained, please let me know.

Hugh Morgan
7725 Berkshire Blvd
Powell TN 37849

Pascal Examples Needed

Just a short note to tell you how very much I appreciated Carl Helmers' "Pascal Checkbook Balancing Program" which appeared in the January 1980 BYTE.

As a beginner, I don't think he "*profaned* Pascal by writing a simple little ..." etc. The program was *most informative*, and I studied it in detail. I have adapted it to the formulation of a metrics conversion program. It was certainly clearer than most of the program examples in the few, but confusing, texts on Pascal.

I realize that in general BYTE magazine caters to the experienced programmer, but what we need are more examples like yours—the we being those of us relatively new to the art.

So thank you once again—and *please* some more tutorials and programs!

Max Nareff
5235 Diamond Heights Blvd
San Francisco CA 94131

A Satisfied Reader Comments

I couldn't believe it! Ted Carter's article "Implementing Dynamic Data Structures with BASIC Files" (February 1980 BYTE, page 92) was exactly what I needed for a program I am writing to computerize billing on a newspaper route.

I had tentatively planned my file routines, but I scrapped my ideas after reading the article.

James E Nichol
1416 Oak Knoll Dr
Cincinnati OH 45224 ■

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80 Character Video

With 80 characters per line our VB3 is the perfect video interface for word processing. It produces a standard 80x24 display of upper and lower case characters or as much as 80x51 for a full page of text. The matrix for graphic display goes up to 160x204. And with optional EPROM, as many as 256 user programmed characters or symbols can be produced.

VB3 is memory mapped for rapid screen updating. But it occupies memory only when activated. So one or more VB3s can be located at the same address with a full 65K of memory still available to the user.

It generates both U.S. and European TV rates and meets the new IEEE S-100 standard. Other features include keyboard input, black on white or white on black, one level of grey, underline, strike thru, blinking char., blank-out char., and programmable cursor. Software includes a CP/M compatible driver and a powerful terminal simulator.

VB3 is available in several configurations. Retail prices start at $375 kit, $440 assembled.

Z-80 CPU

We spent over a year designing the CB2 to assure that it will be the most fully S-100 compatible Z-80 CPU on the market.

It operates at 2MHZ or 4MHZ by DIP switch selection and includes two sockets for 2716/2732 EPROMs or TMS 4016 2K RAMs. Memory sockets can be disabled. Separate run/stop and single step switches allow system evaluation without the benefit of a front panel.

CB2 also features an MWRITE signal, firmware vector jump, and an output port to control 8 extended address lines (allowing use of more than 65K of memory). Jumper options generate the new IEEE S-100 signals to insure future S-100 compatibility.

Retail price—$210 kit, $275, assembled.

8080 CPU

Our new CB1A is identical to our popular CB1 with the exception that the on-board RAM has been increased from 256 bytes to a full 1K.

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The Cassette Lives On

An Alternative to Floppy-Disk Mass Storage

Emory Cook
Cook Laboratories Inc
375 Ely Ave
Norwalk CT 06854

In a world where floppy and hard disks are becoming more affordable for the average small-business user and hobbyist, sequential mass storage in the form of cassette tape is gaining disfavor. Still, many disk users get into trouble when something happens to a floppy disk and they have *not* made backup copies. Although any backup system requires the time and inconvenience of regularly carrying out the file-copying procedure, one problem with using floppy disks for file backup is the cumulative cost of the number of disks needed to maintain backup copies of all records.

The Cassette Solution

What is needed is a low-cost filing medium. Cassette storage is the answer, provided we take the necessary precautions to make it reliable. Old files, such as files of records for last quarter, last year, and the years before, *belong* on cassette. The disk-to-cassette transfer for backup purposes becomes sensible in terms of both expense and security. With adequate tape recorders and high-quality cassette tapes (which use both quality tape material and quality mechanical housings) cassette storage can and does become highly dependable.

Let's go a step further. Anyone who is using a microcomputer and needs its daily functioning will be acquiring a spare microprocessor. With a three-head, audio-cassette machine,which has a separate playback head following the record head (a common piece of high-fidelity equipment), the spare microprocessor can readily be set up with a machine-language program. This program verifies a backup tape by reading the information immediately as the tape is written. [*The same result can be accomplished (a bit slower, however) for those of us who cannot afford a spare microprocessor board or an expensive cassette recorder. This can be attained by using a verification program running on the same microprocessor to reread the newly created tape and compare its information with the contents of computer memory*....GW]

Floppy disks may be a glamorous way to store programs and data, but the cassette is far from dead.

When records are backed up at the end of some reasonable period (ie: day, week, month, etc), the extra time needed to dump the records to cassette at a low transfer rate is not an overwhelming disadvantage. A second backup tape simultaneously made with a second recorder is always a good idea. In other cases, one cassette copy can simply serve as a backup for printed records, thus saving time, printer wear, ribbons, and paper.

For even the most inexpensive cassette deck, a small amount of money and attention can result in the following:

- excellent performance and reliability (no more trial-and-error adjustment of the volume control)
- a very low error rate (statistically as good as that of a 5-inch floppy disk)
- the lowest possible cost per bit stored

Problems with Cassette Storage

The main problems with currently used cassette-storage methods are dirt, variation in tape speed, problems with azimuth alignment, and inferior tape quality.

Dirt collects on the tape recorder head from several sources, from the room, from dust left on poorly manufactured tapes, and sometimes from sweaty fingers attempting to wipe the head clean. The tape head and the pressure roller can be cleaned using pure alcohol and a cotton-tipped swab.

Periodic cleaning is imperative when using poorly manufactured tapes. Cassette tapes are manufactured by slitting a 30.5 cm(12-inch) wide sheet of magnetic material called a *web*. Slitting is accomplished with knives, which often get dull from cut-

Circle 4 on inquiry card. →

ting the inherently abrasive magnetic coating. If the knives are not periodically sharpened (which is the case in making some inexpensive cassettes), the dull knives cause a fine powder of magnetic coating to collect on the edges of the tape. As a result, abrasive magnetic powders come in contact with the tape head when the cassette is later played. The poorer the quality of the tape, the greater the chance that this is occurring.

Variation in tape speed can be caused by belts slipping within the cassette recorder, but it is more often caused by flaws in the pressure roller, which with the capstan is meant to push the tape through the machine at a constant speed. Leaving the tape recorder set in play mode with the motor disengaged (as is done in several current personal computer systems that let the computer control the tape motor) may eventually cause indentations on the pressure roller, with some inevitable variation in tape speed. This variation impairs the reliability and the data-transfer rate of the cassette interface, so it is important to keep the pressure roller clean at all times and disengaged when not in use.

Azimuth of the tape head refers to the angle between an imaginary line drawn in the direction of tape movement and the vertical, magnetic gap on the record/playback head of the cassette recorder. This angle should be 90°–that is, the tape should run straight across the tape head, perpendicular to the magnetic gap. If the tape head is somehow knocked out of alignment (which happens frequently, although nobody knows how), it must be restored if the tape recorder is to faithfully play back a recorded tape.

There is an adjustment mechanism, usually a small Phillips screw, on the left-hand side of most tape heads. However, some tape recorders do not allow you to reach the mechanism when the recorder is in the play mode. Because of this, it is important to do one of two things: either buy a cassette recorder that has an azimuth access hole, or have a good craftsman carefully drill a hole over the screw so that it can be reached with a tiny screwdriver when the recorder is in the play mode.

Recording with a Peak-Signal-Strength Meter

It is the peak output, *not* the average or the root-mean-square value of the cassette signal, that most tape interfaces are sensitive to. In order to repeatedly load cassette tapes on the first try, you must be able to send a signal of known strength to the cassette interface. However, most computer systems give us no feedback on cassette signal strength—in other words, we are operating "blindly." Let us use the TRS-80 Level II tape format as an example. The cassette input port terminates within the TRS-80 with a resistance of 100 ohms. A signal from the cassette with a peak level of about 2 V is needed to insure a correct load. If the cassette record/playback head is correctly aligned with the tape, and the signal is adjusted (via the volume control and our peak-signal-strength meter) to a peak level of 2 V, then the TRS-80 (or whatever computer you have) should load correctly every time.

Figure 1 presents the circuit for a peak-signal-strength meter. The signal from the cassette recorder comes in jack 1 and goes out jack 2 to the computer. Two halves of an LM358N dual operational-amplifier device are used to create a circuit that is highly sensitive to voltage changes in the 2 V region.

Although component layout is not critical, a full-size, printed-circuit-board pattern for this circuit is given in figure 2. A 9 V transistor radio battery will have a life of around 2000 hours of continuous use. The unit can be calibrated by marking the milliammeter dial while applying a known voltage from a DC 1.5 V flashlight battery cell; the reading should not change significantly when the polarity of the input voltage is reversed. The circuit is reasonably accurate in measuring peak voltages of signals with a frequency of up to 20 kHz, and it will then give good accurate readings as long as the 9 V battery supplies 5 V or greater.

Number	Type	+9 V	GND
IC1	LM358N	8	4

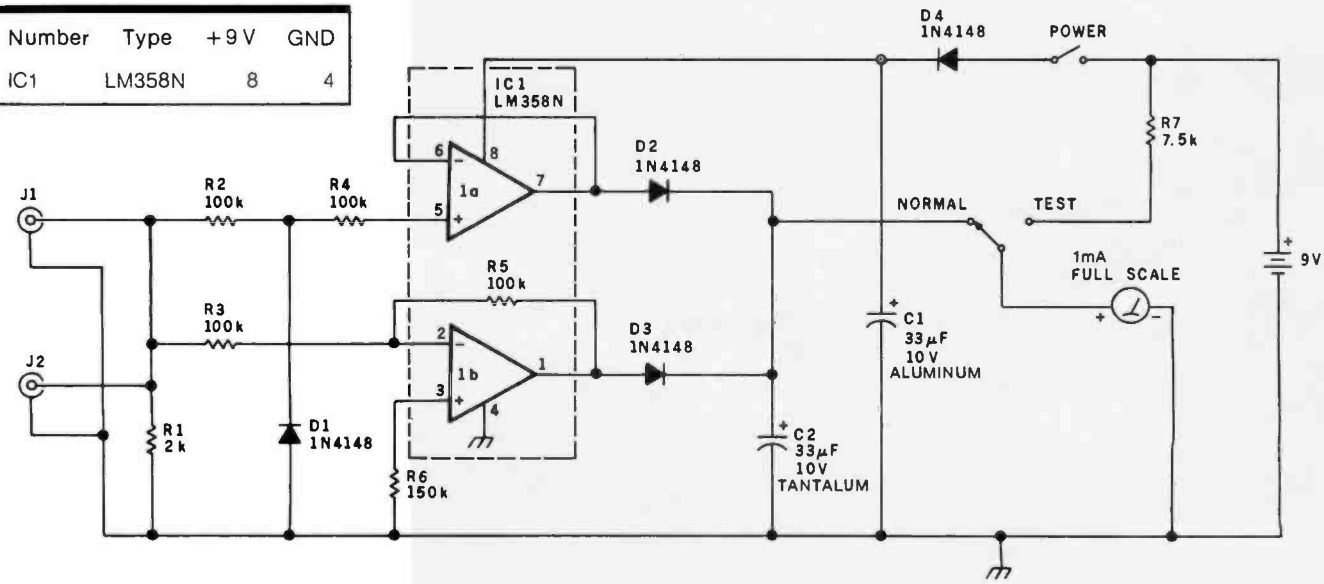
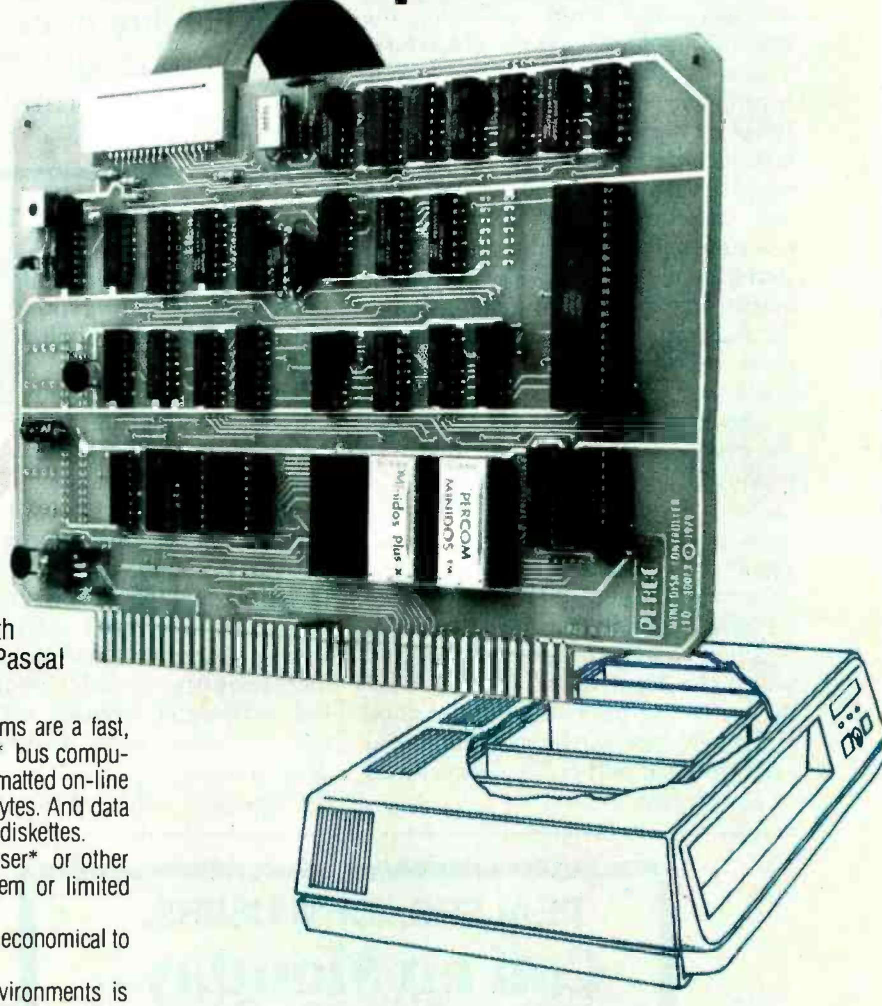


Figure 1: *Schematic diagram of peak-signal-strength meter. This meter enables the user to present the cassette interface with a signal of known peak intensity—usually, about 2 V. The circuit is designed to be sensitive to voltage changes around the 2 V area.*

From Percom . . .

Low Cost Mini-Disk Data Storage for EXORciser* Bus Computers



- Compatible with EXORciser* and other 6800/6809 computers based on EXORciser* bus concept.
- 40- or 77-track drives in one-, two- and three-drive configurations add 102K bytes to 591K bytes of random access data on-line.
- 40-track LFD-400EX® drives store data on both surfaces of mini-diskettes — almost 205K bytes per disk.
- EXORciser* bus compatible controller includes 1K of RAM, provision for 3K of PROM. Mature design features explicit clock-data separator, drive motor inactivity time-out function, and more.
- Support software includes disk operating systems, a file manager, text editor, assembly language program development/debugging aids, an extended BASIC interpreter, an SPL/M compiler and business programs. Numerous programs available from other suppliers may be used with LFD-400/800EX mini-disk systems with little or no modification. Watch for FORTRAN & Pascal announcements.

Low cost Percom LFD-400/800EX mini-disk data storage systems are a fast, dependable alternative to tape storage for 6800/6809 EXORciser* bus computers. A single 40-track LFD-400EX® drive adds 102K bytes of formatted on-line storage; a single 77-track LFD-800EX® drive adds almost 200K bytes. And data may be stored and read from either surface of LFD-400EX® minidiskettes.

Fast mini-disk data storage makes your Motorola EXORciser* or other EXORciser* bus computer more than just a development system or limited evaluation system.

For example, at the low LFD-400/800EX prices it becomes economical to use your development system as the final working system.

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The system prices are single-quantity prices. A system includes (1) the drives, power supplies and enclosure, (2) the EXORciser* bus compatible controller PC card with 1K RAM and provision for three 2708 EPROMs, (3) an interconnecting cable, (4) an 80-page users instruction manual, and (5) a system minidiskette. The Percom Software Services Group will customize the MPX DOS for a nominal charge if one of the standard versions is not suitable for your monitor. LFD-400EX® systems use 40-track drives; store 102K bytes of formatted data per minidiskette side. LFD-800EX® systems use 77-track drives; store almost 200K bytes on one side of minidiskette.

Orders may be placed by dialing 1-800-527-1592 (outside of Texas) or (214) 272-3421 (in Texas). For additional technical information dial (214) 272-3421.

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Checking the Recorder Azimuth

If your tape recorder has an azimuth-adjust screw, adjusting the azimuth angle is a simple procedure. You must first place in the cassette recorder an azimuth-calibration tape (see text box) or a similar cassette tape recorded on a machine *known* to be properly aligned. Then, playing the cassette and monitoring the recorder output with the peak-signal-strength meter, turn the azimuth-adjust screw until the meter reaches its maximum reading. The reading drops off on both sides of the optimal position.

The meter can also be used to get the best reading from a tape that was produced on a tape recorder with faulty head alignment. Simply monitor that tape with the peak-signal-strength meter, adjusting the azimuth-adjust screw until the recorder gives the strongest reading, and use the recorder to load and verify the tape. Once this has been done, the recorder can be realigned and a new tape can be made that you can later load without the same kinds of adjustment.

> One method of improving the reliability of cassette tapes is to modify the signal coming from the cassette recorder.

Problems with Reading Tapes

With most computers, you will need to load a tape using an input peak-signal level of about 2 V (which will appear as about half-scale on the milliammeter of the peak-signal-strength meter). With only slight variations due to a particular computer/recorder combination, the same reading from the peak-signal-strength meter will result in effective loads. A cassette tape coming from a recorder with a misaligned head will give a lower reading than a correctly recorded tape for the same volume setting.First try to load the tape after increasing the recorder volume until the peak-signal-strength meter gives the customary peak reading. If this does not work, you will have to load the tape after adjusting the azimuth in the manner previously described.

Whenever the tape head is misaligned with respect to the tape path, the peak-signal intensity will flutter, even if the tape being played was recorded correctly. This effect is called *skew*. If the signal variation is severe enough, you will be unable to load the tape properly due to data dropout. Signal flutter due to skew is a subtle problem; it will not show on a meter because no meter needle can move fast enough to follow the flutter.

Flutter can also be caused by *tape weave*, which has a variety of causes. If the pressure pad opposite the record/playback head is not positioned properly, it will tend to push the tape away from the center of the head. This is aggravated by the fact that most cassette recorders do not maintain tension on the supply reel, allowing the pressure pad to pull out tape freely and push the tape away from the center line of the head. Also, a tape with a thin backing is more susceptible to tape weave.

Altering Tape Waveforms

Another method of improving the reliability of cassette tapes is to modify (and sometimes rerecord) the signal coming from the cassette recorder. For example, several waveform-changing interfaces that improve the loading reliability of the cassette are available for the Radio

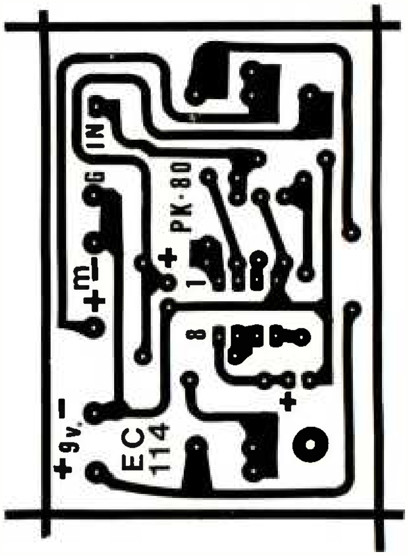

Figure 2: *Full-sized, printed-circuit-board pattern for the peak-signal-strength meter circuit of figure 1.*

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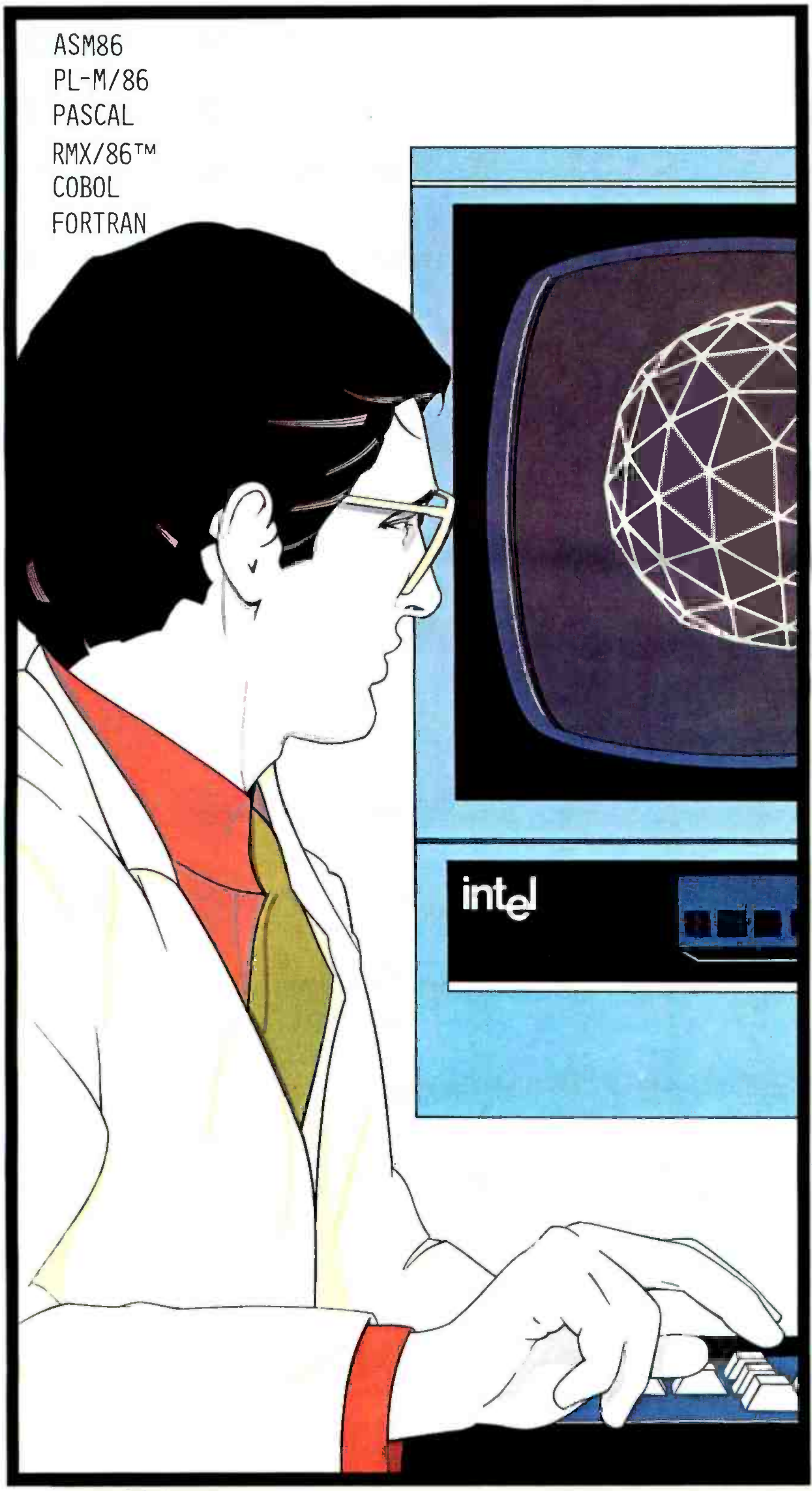
Tools to solve the



How Intel delivers the key to productivity in the '80s.

As we move into the '80s, the increasing demand for complex computer programs, the critical shortage of programmers, and the seemingly unstoppable rise in software development costs will reach crisis proportions. To understand how to bring this situation under control, we have to understand its cause.

In the 1970s, the microcomputer was used successfully to lower the cost of hardware engineering. Each new microcomputer generation integrated more and more of the system, lowering the cost of design and making it easier to put electronic intelligence anywhere and everywhere. As hardware cost dropped, rising software costs became increasingly visible.

So, today, as costs climb, management puts everyone under increasing pressure to deliver projects on time and on budget. Yet, the cost of programming is still outpacing productivity. Software development and integration still lag the system hardware. The software crisis of the '80s rages on.

Tools for structured solutions

Once a problem grows beyond a certain point, the most efficient way to solve it is with a top down approach. You break the problem into units, program and debug each one, and combine the units into a unified solution.

That's the concept. But you can't stop there. In the '80s, bridging the gap between a conceptual solution and a working one will require tools as efficient as the top down method. New tools, like a CPU with a dramatically different architecture. An architecture uniquely suited to a world of higher level languages and structured programming. Tools like a modular operating system, of a kind never before available on a 16-bit microprocessor. Tools like the

software crisis.

only complete family of programming languages, because no one language is right all the time.

Different languages have different strengths and weaknesses, and using the right language for the right job can make your programming easier. So, Intel delivers ASM86 Macro Assembly Language for space and speed sensitive modules. Our PL-M/86 systems programming language and PASCAL support structured programming at the systems and applications levels. FORTRAN and COBOL will also be available.

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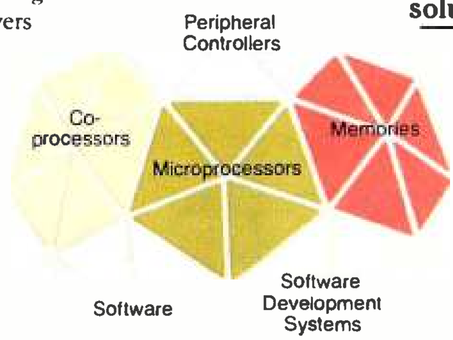

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The critical module

Since complex software requires sophisticated operating systems support, the operating system is the most critical module in your solution. It is the foundation upon which your application is built. It is also available, off the shelf, from Intel.

Today, Intel delivers the RMX/86™ operating system. RMX/86 is new, and it's the first modular, real-time, multitasking operating system for 16-bit microcomputers. File manipulation, task scheduling, and interrupt control are configured by you, according to the needs of your application. There's no unnecessary burden.

Intel's investment in the development of RMX/86 is substantial. Depending upon the features you select, you save from two to forty man years of programming effort. That's an additional two to forty man years you can devote to your application.

Tools for realizing your solution

Of course, having the foundation and the concept of your solution doesn't help if you can't write the programs to implement it. So, Intel delivers development tools to support you through the entire development cycle. Support from source entry, with CREDIT, a CRT based text editor, through compiling and debugging, with an Intellec® development system and ICE™ hardware/software debugging system. Intel's tools work with you. They shorten development time and support the structured approach you've taken.

But debugging software on a development system is not the same as testing it on the actual hardware. The ICE modules help here, too. During development, these tools let you trace through your software and debug it, symbolically, at the source language level. Now, these In-Circuit Emulators replace your prototype hardware's CPU to speed hardware/software integration.

If your hardware is built from components, ICE Modules will help you separate the hardware and software bugs, so you don't spend your time fixing engineering problems. If your hardware is built around an Intel iSBC 86/12A™ Single Board Computer, you'll already have a known, working hardware environment for program testing. You can use ICE Modules to concentrate your efforts on debugging your software.

Either way, the same software, operating system support and debugging tools are available to help you bring your application to life.

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In the '60s and '70s, programs were used to instruct computers. Applications of the '80s require programs to be the solutions to problems. High performance solutions will be the result of synergy between the hardware and the software.

To create this synergy today, Intel delivers the 8086 processor. The 8086 processor is unique. Instead of a linear, or flat architecture, the 8086 is the only microprocessor optimized to work with high level languages and the structured solutions they implement.

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To find out more about our solutions, fill out the information requested below and send it to Intel Corporation, Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051. Indicate what your particular interests are, including workshops, and we'll make sure you get the appropriate material. If you don't have a pair of scissors handy, give us a call at 408/734-8102 (Literature Department) and we'll rush the material out to you. Or call your local Intel distributor.

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Circle No. 426 for information.

Shack TRS-80. About two winters ago here at Cook Laboratories, we developed a modified tape format that records more reliably on the TRS-80. Without going into the details of the TRS-80 tape format, I can say that the unaltered tape signal crowds too much information into a given space and thus opens itself to reliability as well as saturation problems. The latter problem is what makes the TRS-80 normally so volume sensitive. The waveform we use at Cook Laboratories, when recording tapes for the TRS-80, reorders the waveform shape and narrows the pulse width so that the cassette interface does not get confused.

The various waveform modifications could certainly be used to improve the reliability of the cassette storage on other microcomputers. For example, on the old-model PETs, there is no way to alter the volume level of the built-in cassette recorder. However, Commodore can provide a documented program called S-21. This program, when running, monitors tape being played in the PET cassette deck and displays certain information about the quality of the tape signal on the PET screen. This is a very effective program to have if you know how to use it; Commodore is the only manufacturer I know that supplies a program like it.

Tape Is Also a Factor

Several factors having to do with the cassette tape itself can also affect the reliability of tape loading. As I mentioned before, a tape that is too thin will likely give in to tape weave. Tape stiffness is a property of the thickness of the backing and is proportional to the third power of the gauge thickness of the backing. This indicates that you should not use long-playing cassettes for program and data storage.

The thickness of the magnetic coating affects the reliability of cassette storage, but in a different way. Standard audio tapes, chromium dioxide or otherwise, are not optimal for digital recording because they are designed to give good frequency response in the low frequencies. But low frequencies are not needed here; rather, well-defined and sharp waveform transitions are what count. A thinner magnetic coating than what is used in standard audio cassettes results in nice improvements both in waveform resolution and sharpness of transition. Not incidentally, Cook Laboratories markets a custom line of digital cassettes under the trademark MICROFUSION. This tape has a thinner chromium dioxide coating and a heavier and, therefore, stiffer backing, both of which make it well suited for digital storage.

Cassette tapes can be used for reliable mass storage if the tape recorder is kept clean and properly aligned, if quality tape (especially tape made for digital storage) is used, and if the signal going from the cassette to the computer is monitored and kept constant (from tape to tape) with a peak-signal-strength meter. Although disks are readily available and bubble memories are not far away, no medium will ever become obsolete as long as it provides a needed function. Cassettes, too, are here to stay. ■

The following items are available from Cook Laboratories, 375 Ely Ave, Norwalk CT 06854:

AZ-80 Precision azimuth cassette, chromium dioxide. $14.95

PK-80 Kit for peak-signal-strength meter, including board, litho panel, screwdriver, meter, case, and instructions, less battery $25.90

AZ-B1 Printed-circuit board for peak-signal-strength meter, etched and drilled $2.50

MICROFUSION digital cassette,	*C-10*	*$3.26*
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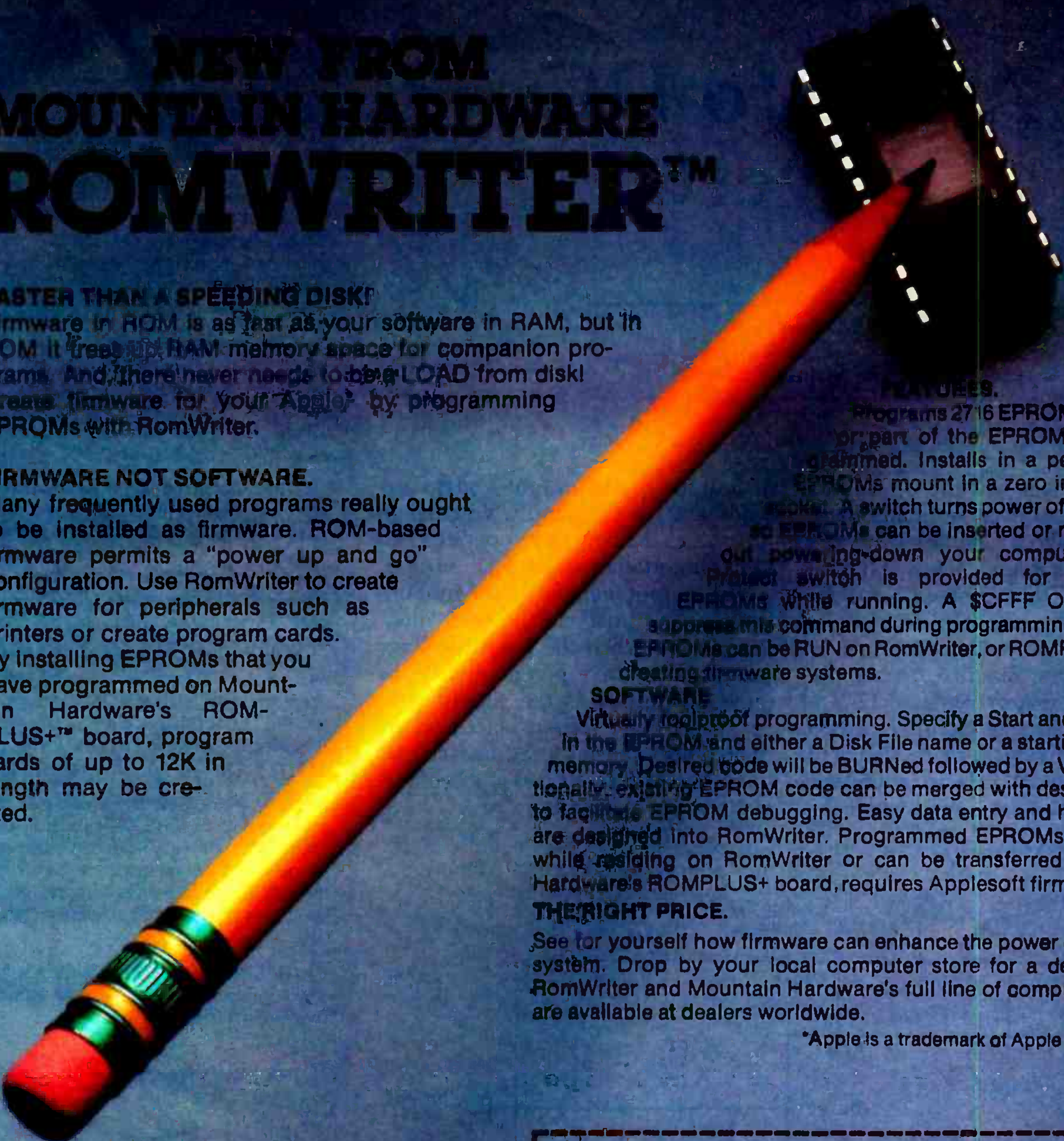

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SOFTWARE
Virtually foolproof programming. Specify a Start and End address in the EPROM and either a Disk File name or a starting address in memory. Desired code will be BURNed followed by a VERIFY. Additionally, existing EPROM code can be merged with desired changes to facilitate EPROM debugging. Easy data entry and high reliability are designed into RomWriter. Programmed EPROMs can be RUN while residing on RomWriter or can be transferred to Mountain Hardware's ROMPLUS+ board, requires Applesoft firmware.

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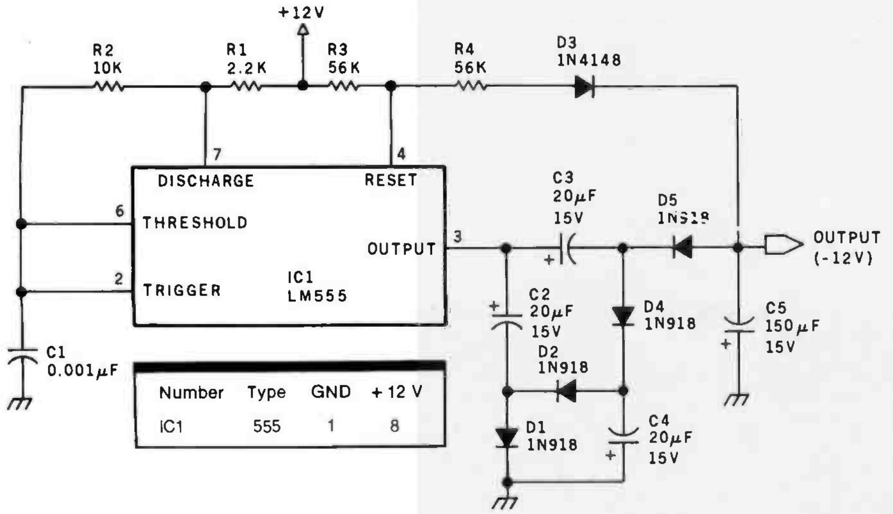
A DC-to-DC Converter

Michael Picco
POB 516
Corte Madera CA 94925

Have you ever had the need for a bipolar power source, but had only a positive voltage available? With the help of a timer and a few external components, this problem can be overcome. The circuit in figure 1 is sufficient for powering op amps or similar devices requiring a supply current of 25 mA or less at −12 V.

The heart of this circuit is a 555 timer that provides a drive signal of approximately 20 kHz to a voltage doubler. This signal is removed if the magnitude of the output voltage exceeds that of the supply voltage. In this sense, the converter operates as a switching-mode regulator.

The output voltage is set by controlling the timer via the reset input (ie: pin 4). When the output voltage reaches a negative potential with the same magnitude as the supply voltage, a low logic state is placed on the reset input, causing the timer output to go low and the increase in voltage magnitude to cease. ■



Number	Type	GND	+12 V
IC1	555	1	8

Figure 1: *Schematic for the DC-to-DC converter. The 555 timer produces a rectangular wave at about 20 kHz, which is inverted by the diode-capacitor voltage-doubler arrangement. A feedback signal reaching the reset pin of the 555 regulates the magnitude of the output, which is −12 V at 25 mA.*

I/O Expansion for the Radio Shack TRS-80

Part 1: Principles of Parallel Ports

Steve Ciarcia
POB 582
Glastonbury CT 06033

I receive a lot of mail: enough that I'm beginning to feel like the "Dear Abby" of the personal computer ranks. The sources of the letters range from high school students asking for advice on science fair projects to major corporations seeking consultant services. Even though it takes considerable time to answer this mail, I regard it as a significant opportunity to gauge reader interest. Every letter in some way contributes to my choice of article topics, either through suggestions or by continued occurrence of similar questions.

Recently, my mail has been dominated by owners of the Radio Shack TRS-80 Model I thirsting for hardware expansion by means other than Tandy Corporation equipment. The majority of questions concern connection of my interfaces to the TRS-80 expansion connector.

In general, I have tried to present projects that are computer independent. That is, the interfaces described are driven through parallel input/output (I/O) ports rather than directly from a computer bus. This had not been a problem in the past, because virtually all of the early personal computers incorporated some parallel I/O capability. For those experimenters interested in enhanced I/O capabilities, I presented the article "Memory-Mapped I/O" in the November 1977 BYTE on page 10 (reprinted in *Ciarcia's Circuit Cellar* Volume I, BYTE Books), which detailed parallel-port construction.

In the 2½ years since that article was first published, a number of significant changes have occurred in personal computing. Most importantly, the Radio Shack TRS-80, the Apple II and the Commodore PET were introduced. The difficulty in maintaining and operating a computer is no longer a serious consideration for most computer enthusiasts. Much of my mail indicates that a new explanation of parallel and serial I/O is in order, and that it is time for hardware-expansion circuits to be detailed.

> A *port* is a hardware channel for the computer to transmit and to receive *data* via an *external* peripheral device.

This month's Ciarcia's Circuit Cellar is the first of a two-part article on serial and parallel I/O port expansion of the TRS-80. The first part emphasizes parallel I/O, and the second part is concerned with serial interfacing. The result will be a complete Radio Shack software-compatible communications interface capable of supporting a variety of serial- and parallel-interfaced peripheral devices. The hardware was designed and the components were selected to be economical to build and easy to check out. First, here is a brief review of the basics.

What Is an I/O Port?

Just as some people are initially confused with the terms *hardware* and *software*, some find the concept of input and output ports difficult to understand without substantial explanation. The classical definition: a *port* is a hardware channel for the computer to transmit and receive *data* via an *external* peripheral device. The key words in this definition are *external* and *data* which imply externally collected information; the channel through which this data is obtained is called a *port*. A printer is a typical external peripheral device. The characters to be printed are sent from the computer to the printer. In some of the more sophisticated units, status signals such as *busy* and *out of paper* are returned to the computer from the printer.

Ports can be either parallel or serial. In *parallel* mode, data is transferred in increments equivalent to the word size of the computer. On the Z80, for instance, an 8-bit microprocessor, an output instruction through a parallel port transfers 8 bits at a time. A 16-bit processor such as the Intel 8086 transfers data in 16-bit increments. The number of bits transmitted simultaneously by a parallel port is dependent upon the size of the microprocessor data bus and how many bits the processor can transfer simultaneously.

However, serial data is always transmitted a single bit at a time, according to a fixed schedule defined by the data rate (usually expressed in bits per second, or *bps*) and a few specific options. The microprocessor has no single instruction that transmits serial data. It must rely on another device called a universal asynchronous receiver/transmitter (UART) to put the data word into serial form and transmit it. Any communication between the processor and the UART is in parallel form and is done through the processor's memory reference or I/O data-transfer instructions. A more in-depth discussion of serial ports will be presented next month in Part 2.

Address, Data, and Control Buses

Consider a computer system that includes a printer, video terminal with keyboard, and an audio cassette recorder as peripherals. Data would have to be relayed to the printer, to and from the video terminal, and to and from the cassette recorder. How can the computer tell the difference between data destined for the terminal and the data destined for the printer?

Most microprocessors incorporate a bidirectional *data bus* and an *address bus*: this is shown in figure 1. To keep track of the data transfer between the processor and its peripherals, the system uses a quantity of control signals which together can be called the *control bus*. The usual 8-bit processor has an 8-bit data bus, a 16-bit address bus, and a dozen or so control signals.

When the microprocessor is reading a data byte from memory, the address of the memory location being referenced is placed on the address bus. Memory information stored at that location goes on the data bus and flows from memory to the processor. When data is being written into memory, the operation is reversed. A 16-bit address bus allows the processor to directly address 65,532 (ie: 64 K) memory locations.

In an 8080 or Z80 processor there is a specific set of instructions that perform input/output functions. The operation of these I/O instructions is similar to that of memory-reference instructions, except that only 8 bits of the address bus are used. These 8 bits

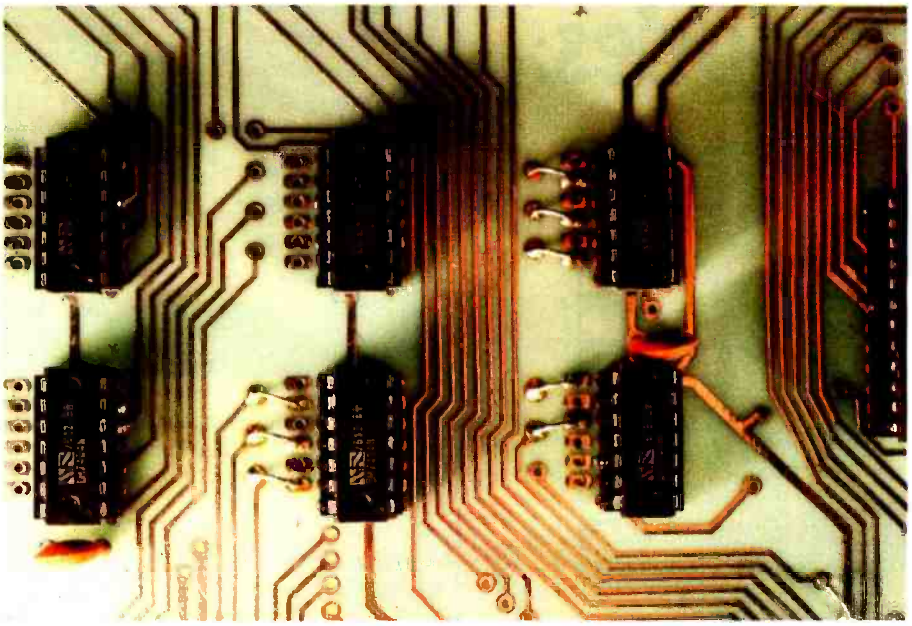


Photo 1: *There are a variety of ways to decode the address for a particular input/output (I/O) port from the signals present on the address bus. The least expensive method uses inverters and printed-circuit-board jumpers to select the correct logic polarities. Three address lines are connected through each 7404 hex inverter with two possible connections for each address line. A connection to the upper trace on the circuit board decodes a logic 1; a connection to the lower trace decodes a logic 0.*

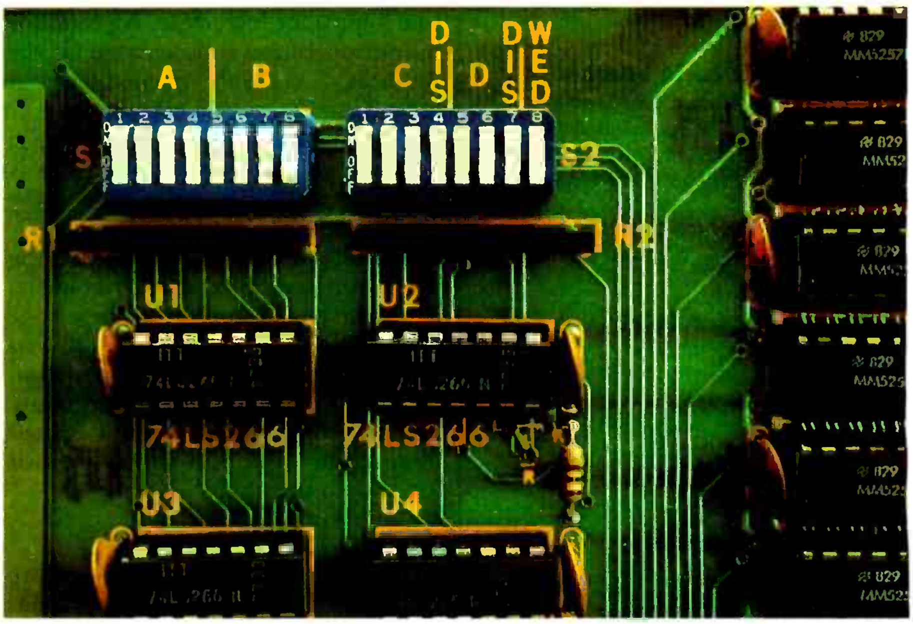


Photo 2: *A more expensive and more easily changed addressing scheme employs dual-in-line-pin (DIP) switches and exclusive-NOR gates. The schematic diagram for this is shown in figure 3b.*

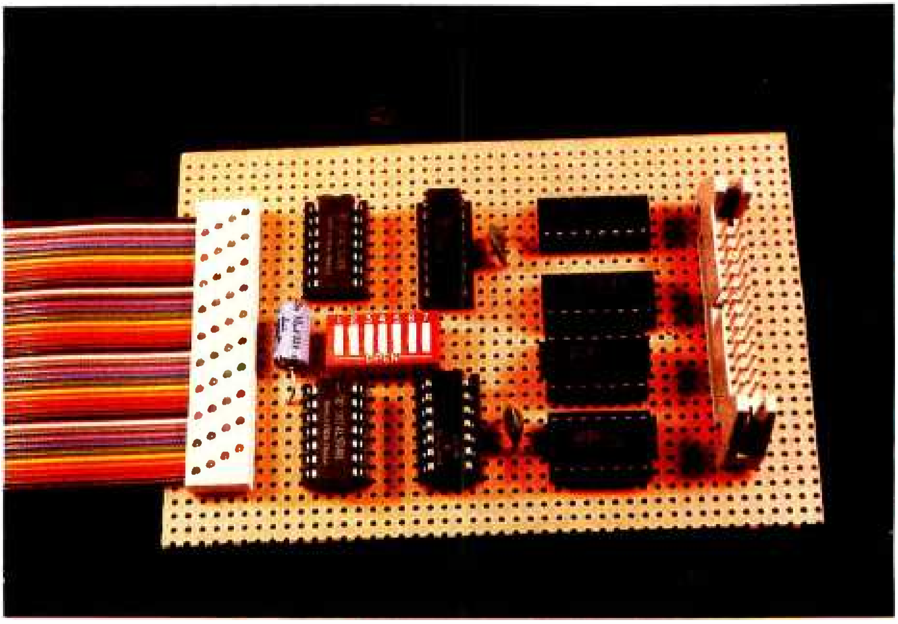


Photo 3: *Prototype of an 8-bit I/O port for the Radio Shack TRS-80. The ribbon cable at left connects to the expansion port on the keyboard/processor unit. The two I/O ports are brought out to the ribbon-cable connector on the right edge of the board.*

designate one of 256 possible I/O ports. In the case of the example system, a separate port address would be used for each peripheral.

Keeping track of bus direction and information flow is a matter of properly decoding the control signals during program execution. In a Z80 for instance, any memory-reference operation is signified by the control signal MREQ in the processor going to a logic 0, or low, state. An input or output operation is designated by the I/OREQ control signal being at logic 0.

The direction of the data bus depends on whether the processor is trying to read or to write data. If the processor is in a read mode, the RD control signal becomes a logic 0; if the processor is writing, the WR line is in the 0 state. Monitoring these four lines, MREQ, I/OREQ, RD, and WR, gives us all the information necessary to support I/O decoding functions. Figure 2 demonstrates how these control outputs are combined for system use.

Address Decoding

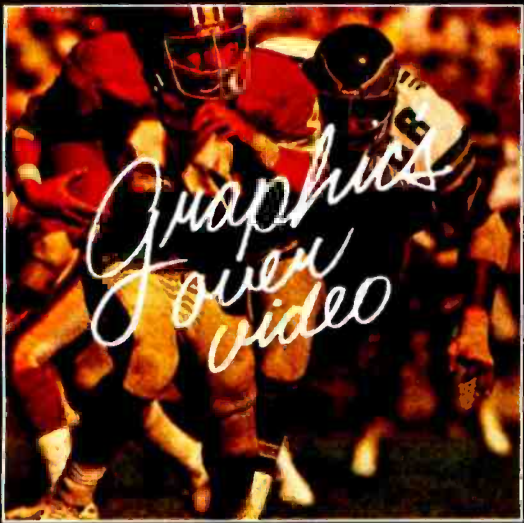
So far we have discussed how to determine when the processor wants to send a character to an output device. In such an operation the I/OREQ and WR lines are both low. To tell the difference between data for the printer and data for the terminal, we must decode the 8-bit port address.

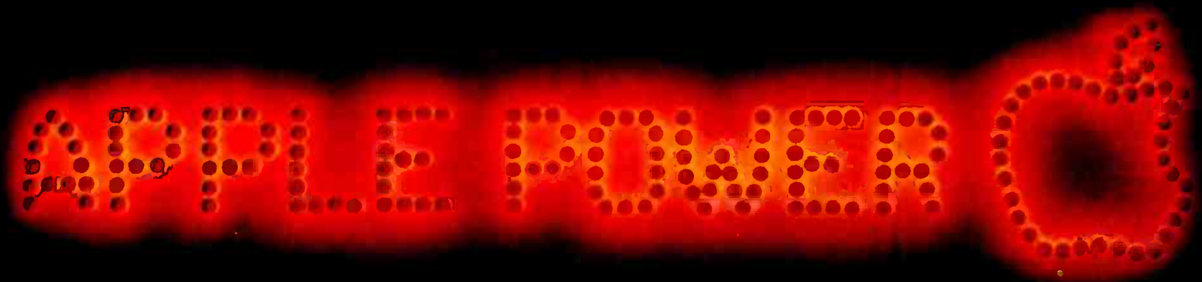
The port address is determined by the logic voltages present on the low-order eight lines (that is, the 8 least significant bits) of the address bus during I/O operations. Various techniques can be employed to decode these lines. Figure 3 outlines a few simple methods. The objective, whatever the logic employed, is to produce a single pulse (ie: a strobe) whenever the logic states representing a particular address appear on the address bus. To eliminate false outputs when the processor is executing instructions not dealing with I/O, it is best to combine control and address signals as demonstrated in figure 4.

If you own a 6800- or 6502-based system, you have probably noticed that the processor has no special I/O instructions. This does not mean that these processors have no external communications capability, only that these processors communicate with peripheral devices differently. How can we discover this different method? Let us begin by looking closely at the I/O functions of the 8080 and Z80 that we have just discussed.

A close inspection of the I/O functions of an 8080 or Z80 should point

Text continued on page 30





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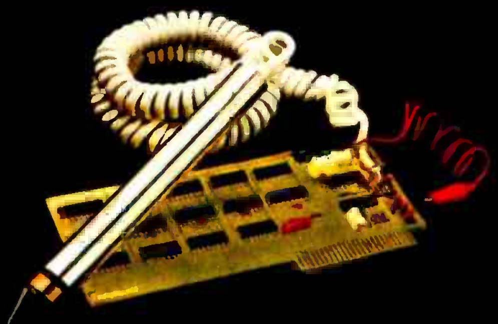

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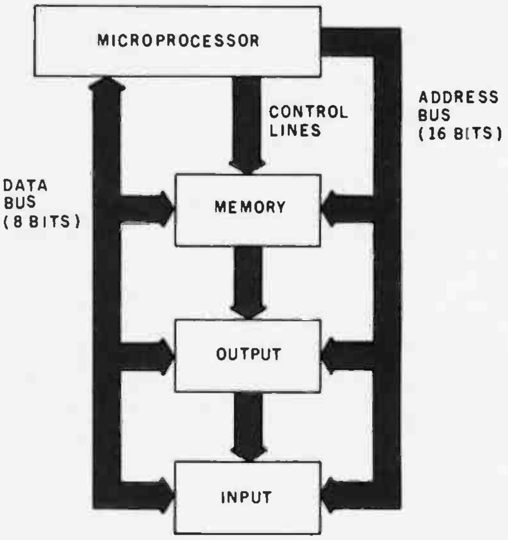

Figure 1: *Block diagram of a microcomputer system that uses an 8-bit microprocessor such as the Z80. This system uses bussing techniques that are both multiplexed and bidirectional.*

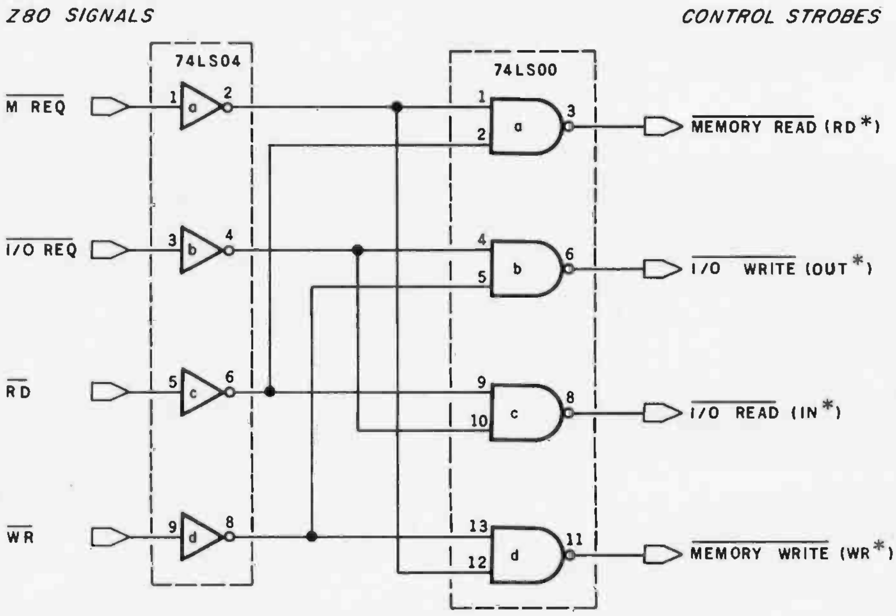

Figure 2: *Control signals on the Z80 microprocessor. The Z80 uses a variety of control signals to keep data flowing at the right time and in the right direction. Four control signals are as follows: the $\overline{MREQ}$ line goes to a low state (ie: a logic 0) when a memory- reference operation is in progress; the $\overline{I/OREQ}$ line goes to a low state when an input/output (I/O) operation is in progress; the $\overline{RD}$ line goes low when the processor is reading data from memory or from a peripheral device; the $\overline{WR}$ line goes low when the processor is writing data to memory or to a peripheral device. The $\overline{RD}$ and $\overline{WR}$ signals control the direction that data flows along the bidirectional data bus. Monitoring these four lines gives us all the information necessary to support I/O decoding functions.*

Signals from the four processor control lines are logically combined to form control-strobe signals that perform specific functions. The characters in parentheses give the names by which the control-strobe signals are known in the documentation for the Radio Shack TRS-80.

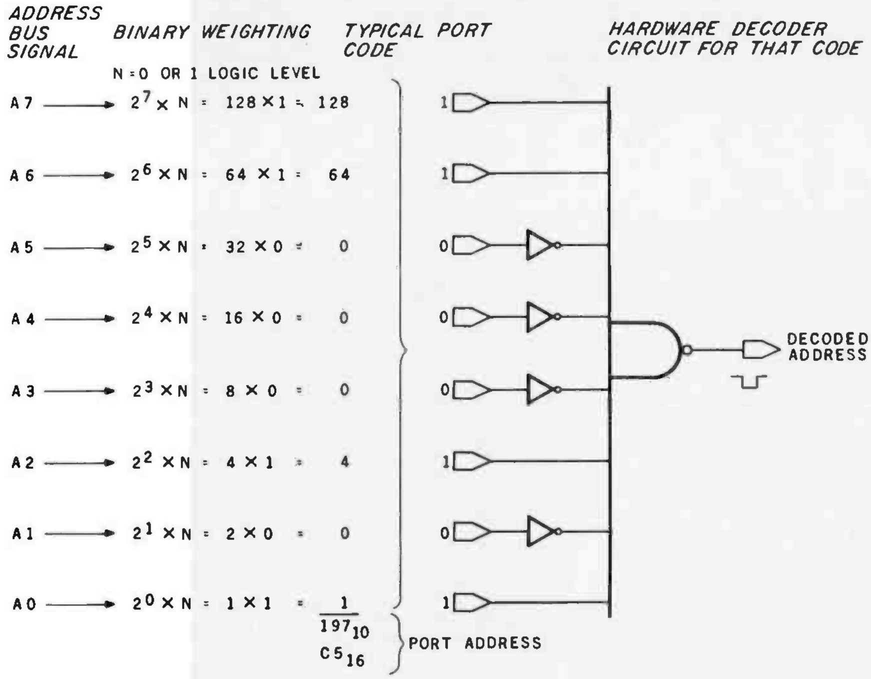

Figure 3a: *Various methods can be employed to decode the address signals that appear on the address bus during I/O operations. Here, various inverters and an eight-input NAND gate are hardwired in a configuration that will produce a logic 0 output for one of 256 possible I/O port addresses. The logic 0 output can be used to activate the interface for the peripheral device. Here the circuit decodes the address hexadecimal C5, or decimal 197.*

Number	Type	+5 V	GND
IC1	74LS85	16	8
IC2	74LS85	16	8
IC3	74LS04	14	7

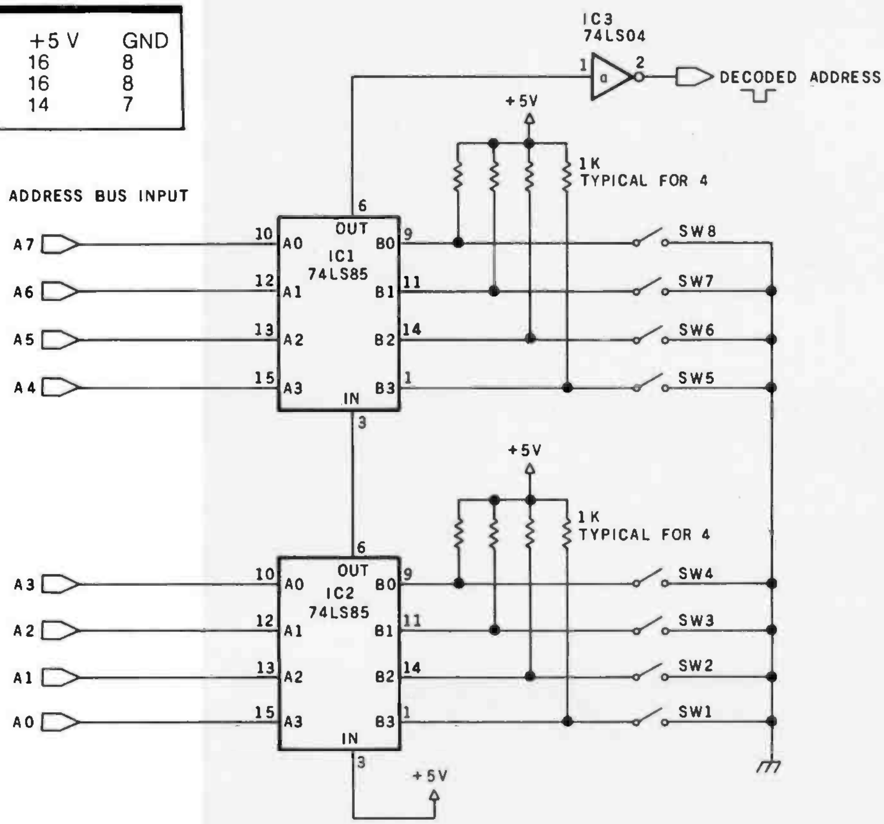

Figure 3b: *Another method of decoding an address signal. Two 4-bit comparators can be cascaded together to decode an 8-bit address. The desired 8-bit port address is set up on switches SW8 thru SW1. When the combination of high and low logic states that corresponds to the desired address appears on the address bus, the output signal produced at pin 2 of IC3 (the 74LS04 inverter) will go low to a logic 0 state. This decoding method allows the port addresses to be easily changed, but the method here is considerably more expensive than the decoding method shown in figure 3a. The switches are single-pole, single-throw (SPST) types; an open switch shows logic 1, and a closed switch shows logic 0.*

Text continued from page 24:
out that the I/O instructions bear a surprising resemblance to memory-reference instructions. The 6800 and 6502 microprocessors actually allocate a certain portion of their memory address space to be decoded and to function as I/O ports.

This technique, which can be used on the Z80 and 8080 just as easily, has certain advantages in speed and ease of use over direct I/O instructions. This technique is referred to as *memory-mapped I/O*. An illustration of the logic associated with this method is in figure 5. For a more rigorous analysis of memory-mapped I/O, I refer you to the November 1977 "Ciarcia's Circuit Cellar" article previously mentioned.

The final area for consideration is the actual transfer of data to and from the bidirectional data bus. The circuits of figure 4 and figure 5 tell only *when* the I/O operation occurs. Additional logic has to be provided to place data on the bus during an input instruction or to latch and hold the contents of the data bus during output instructions.

When the 8080 or Z80 assembly language instruction OUT (*N*),D is executed, the contents of the accumulator, D, are placed on the data bus and written into device *N*. The same is true for the BASIC-language instruction OUT *N*,D. The data is actually valid during only a few clock cycles, perhaps 500 ns. Making this data available for longer periods of time requires the addition of an 8-bit *latch*: the latch is made from a set of clocked flip-flops.

The output lines are attached to the data bus. When the proper output instruction is executed, signified by a strobe signal from our address and I/O WRITE decoder circuit as shown in figure 6, the contents of the data bus are transferred into the 8-bit register in synchronization with the processor clock signal. This combination of circuitry is commonly called an *8-bit latched parallel output port.*

External devices cannot be directly connected to the data bus for input, because of the possibility that interference and bus-loading problems will result. A three-state buffer is used as a *gate* to allow signals from the peripheral device to be placed onto the bus at the appropriate time.

During an input operation the process used for output is reversed. When the proper input sequence is executed, signified by the appropriate output from the address decoder and I/O READ decoder, the 8-bit three-state buffer is strobed into operation during the few clock cycles it takes for the processor to execute the input instruction. Logic levels present on the buffer input lines during that instant become impressed onto the data bus and are transferred into the accumulator. Figure 6 shows the logic elements that perform these functions.

Number	Type	+5 V	GND
IC1	74LS266	14	7
IC2	74LS266	14	7
IC3	74LS30	14	7

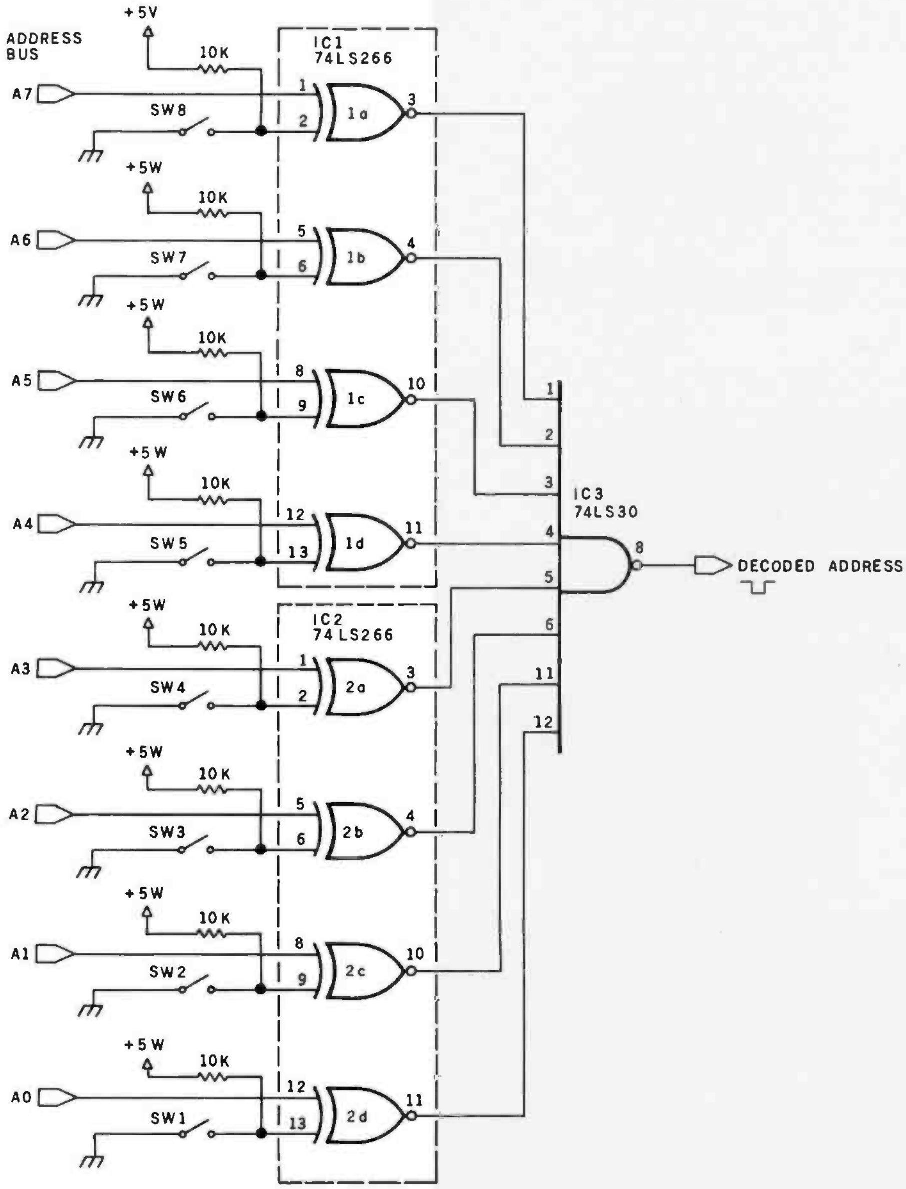

Figure 3c: *Another method of decoding an 8-bit address, using exclusive-NOR gates and an eight-input NAND gate. As in figure 3b, the desired port address is set up on switches SW8 thru SW1.*

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Text continued on page 38

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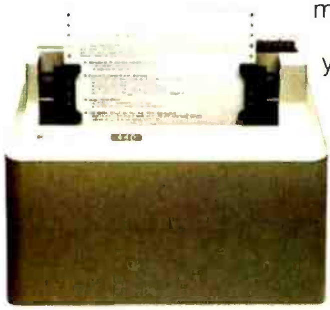

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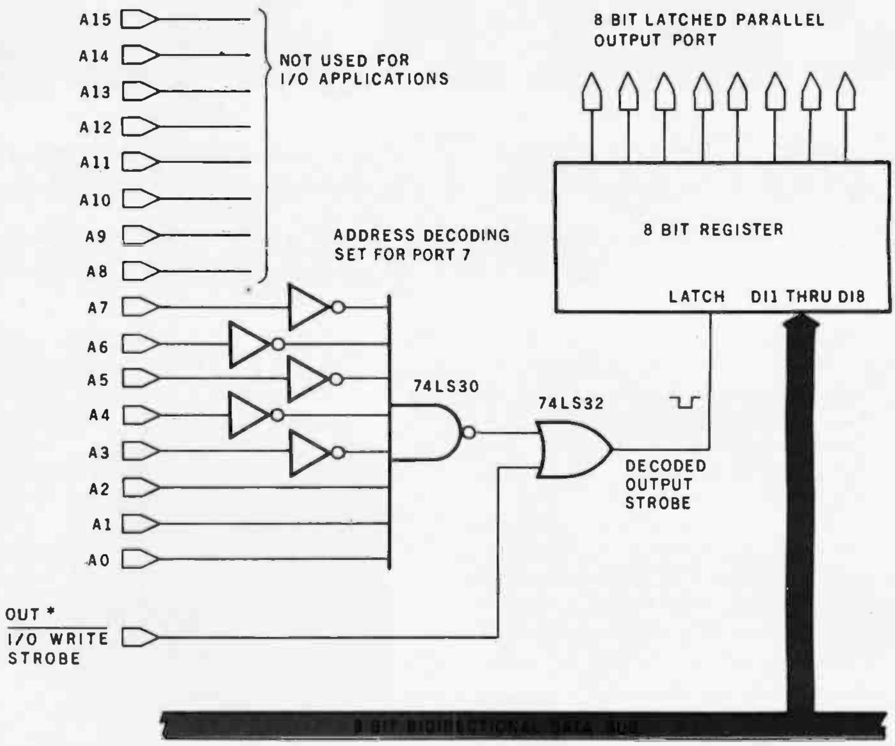


Figure 4a: *Block diagram of a typical parallel output port. The logic that decodes the 8-bit port address was shown in three forms in figure 3. The signal from the address-decoding circuit is logically combined with one of the control signals from figure 2 (I/O WRITE) to produce an output strobe signal that activates the 8-bit output latch register.*

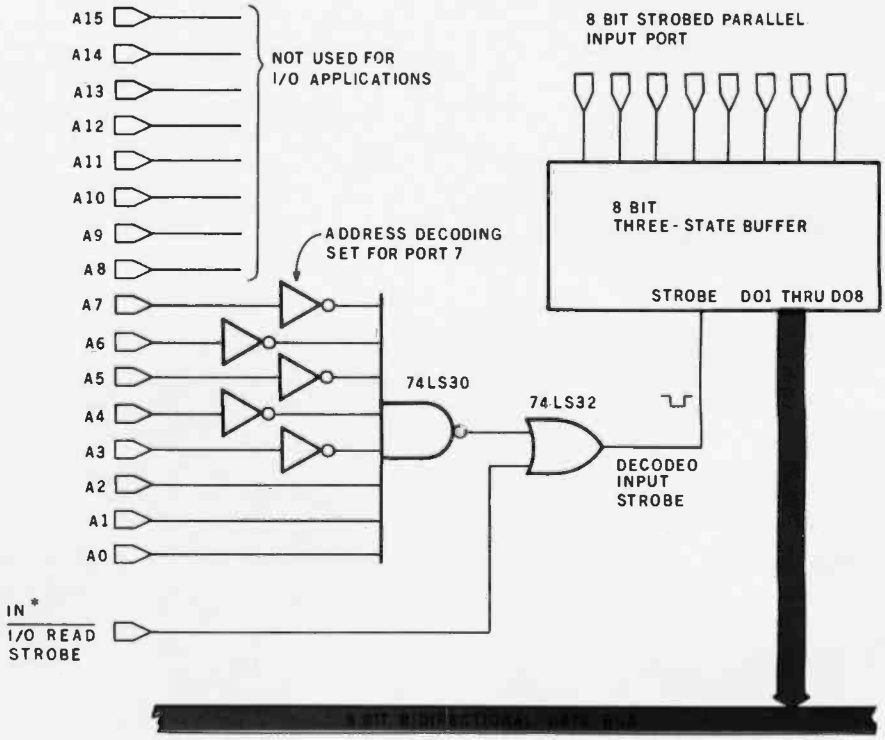
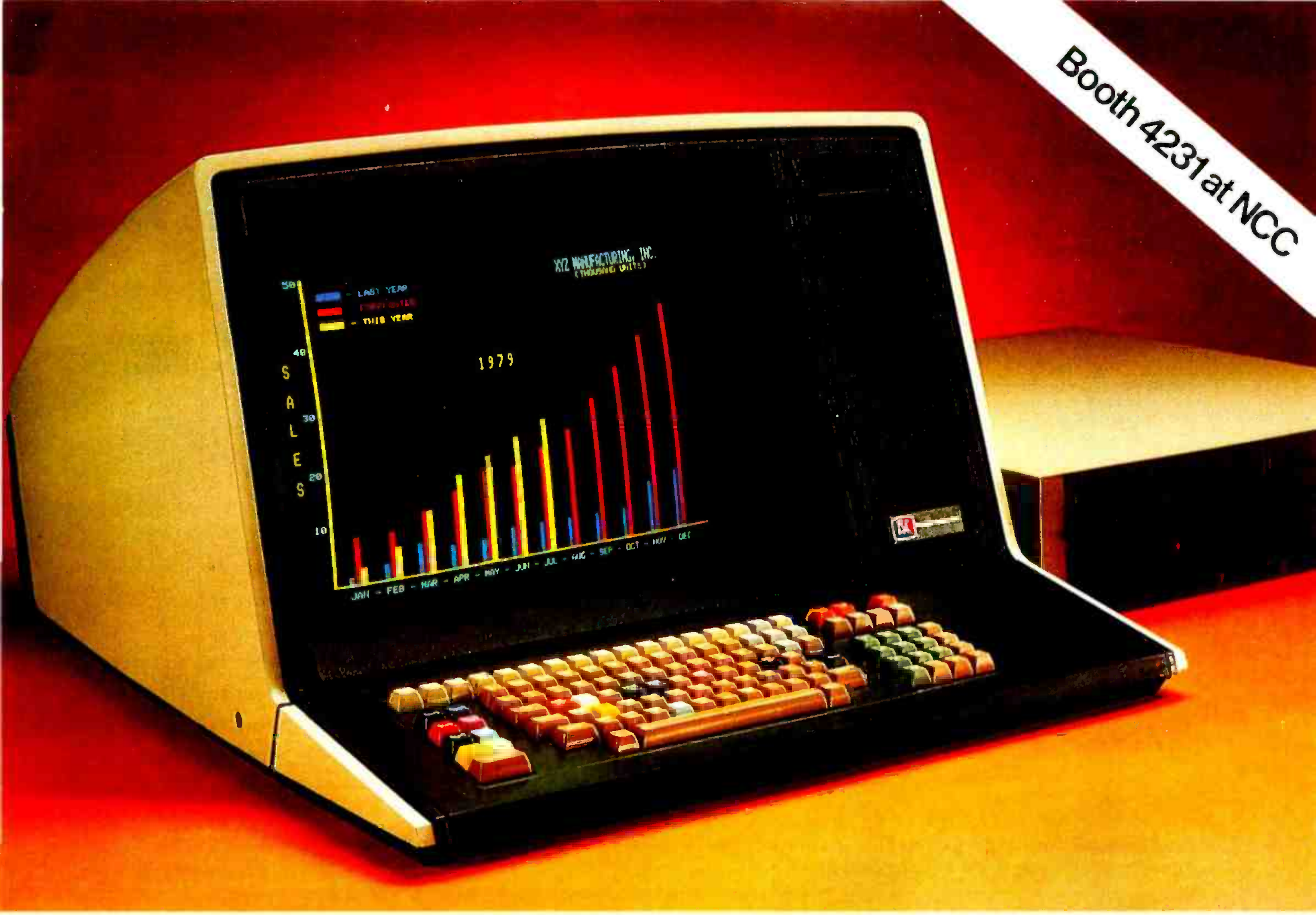


Figure 4b: *Block diagram of a typical parallel input port. Note the resemblance to the output port of figure 4a.*



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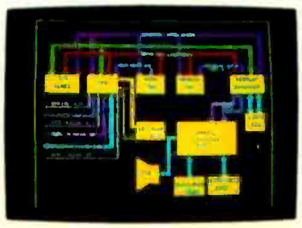

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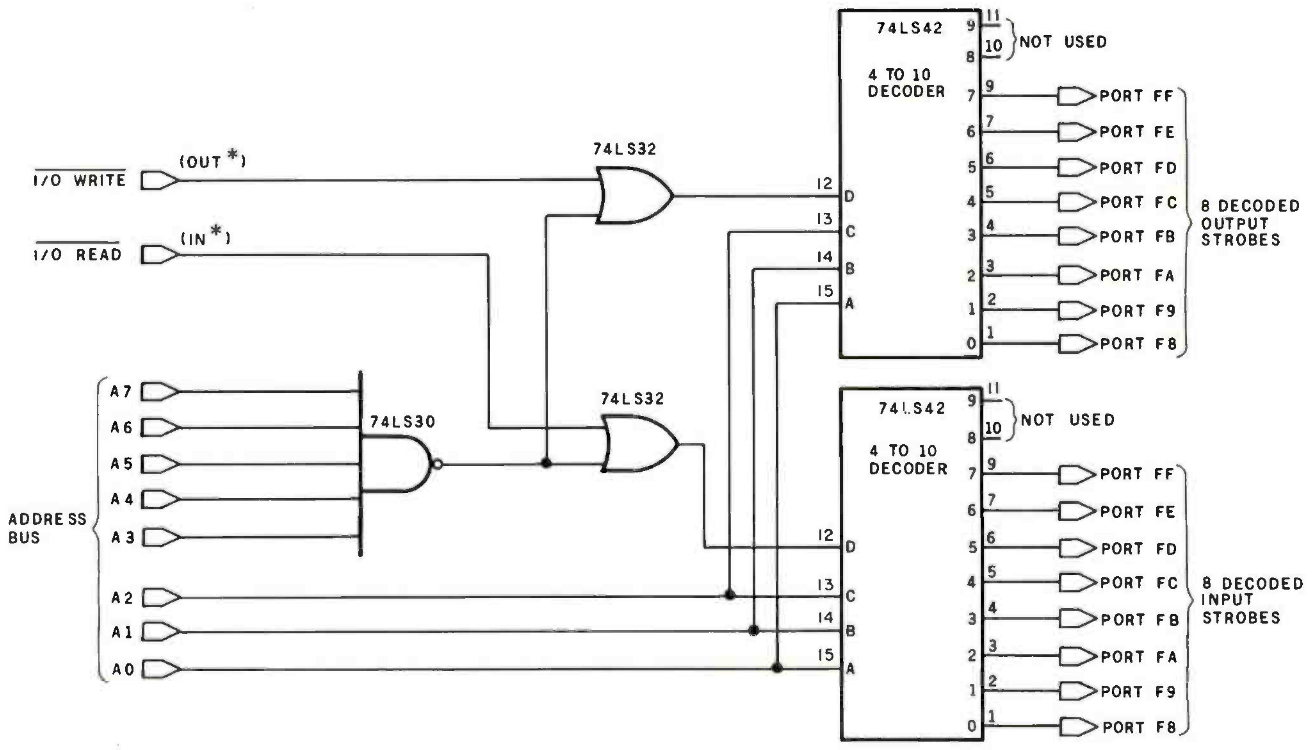

Figure 4c: *Schematic diagram of a circuit that produces eight decoded input-strobe signals and eight decoded output-strobe signals. The port addresses produced are hexadecimal F8 thru FF.*

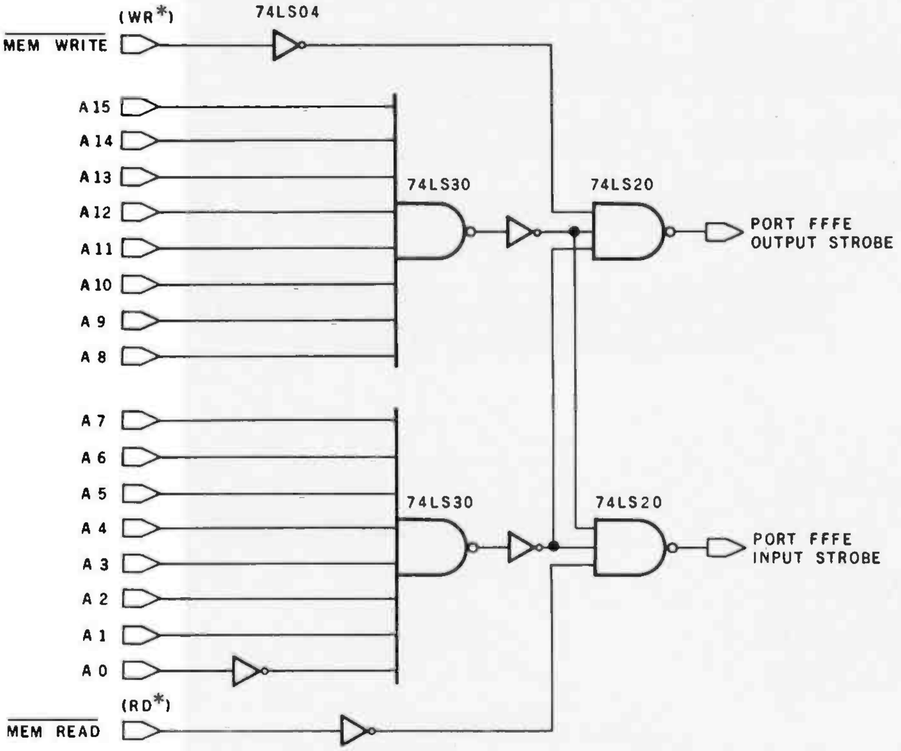

Figure 5: *Memory-mapped input and output. Some microprocessors do not have specific input and output instructions. In systems that use such microprocessors, the I/O port hardware is wired as a memory location; I/O operations take place using the memory-reference instructions (eg: load-into-accumulator and store-in-memory instructions) of the microprocessor. This type of addressing is called memory-mapped I/O, and all sixteen lines on the address bus must be decoded to perform an I/O operation.*

Number	Type	+5 V	GND
IC1	74LS377	20	10
IC2	74LS244	20	10
IC3	7404	14	7

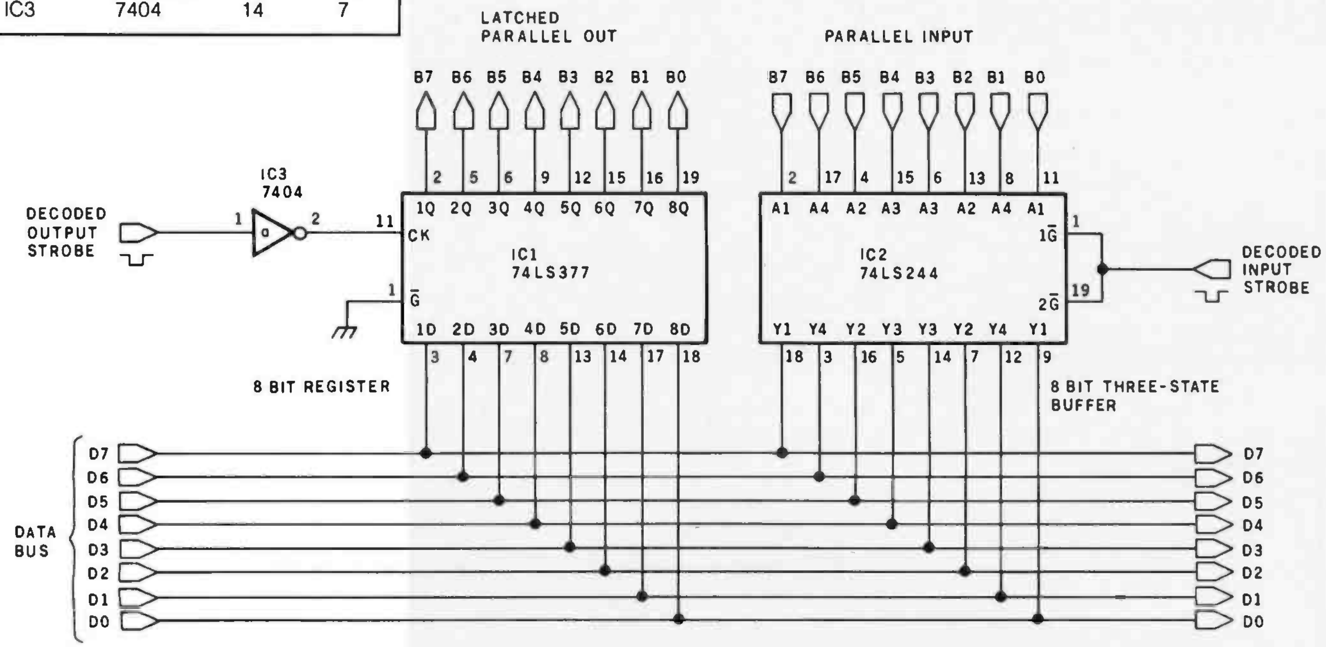

Figure 6: *Data connections in input and output ports. Once the proper port address has been decoded and combined with the read- or write-control signal to form an I/O strobe signal, the actual process of accessing the data bus for data transfer is relatively easy.*

For input to the accumulator (the most common pathway for I/O), a three-state buffer is used in conjunction with the decoded input-strobe signal that controls the enable line of the buffer.

For output from the accumulator, an 8-bit latch is connected to the data bus. During the execution of the output instruction, the contents of the data bus are clocked into the latch register and are latched there by the output-strobe signal.

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Number	Type	+5 V	GND
IC1	74LS125	14	7
IC2	74LS125	14	7
IC3	74LS75	5	12
IC4	74LS75	5	12
IC5	74LS155	16	8
IC6	74LS04	14	7
IC7	74LS04	14	7
IC8	74LS30	14	7

Text continued from page 30:
is not configured to be easily interfaced to the projects I present each month. The widely sold Level II BASIC, 16 K-byte memory version has no parallel I/O capability, aside from the single-bit cassette-motor control. With the addition of the expansion interface, the user gets one parallel output port and one half (ie: 4 bits) of an input port. If these ports are used, as Radio Shack intends, to drive a printer, then the only way to provide usable parallel I/O capability is to add a separate I/O interface.

Considering the pertinent elements of the previous discussions, it is easy to construct both parallel input and

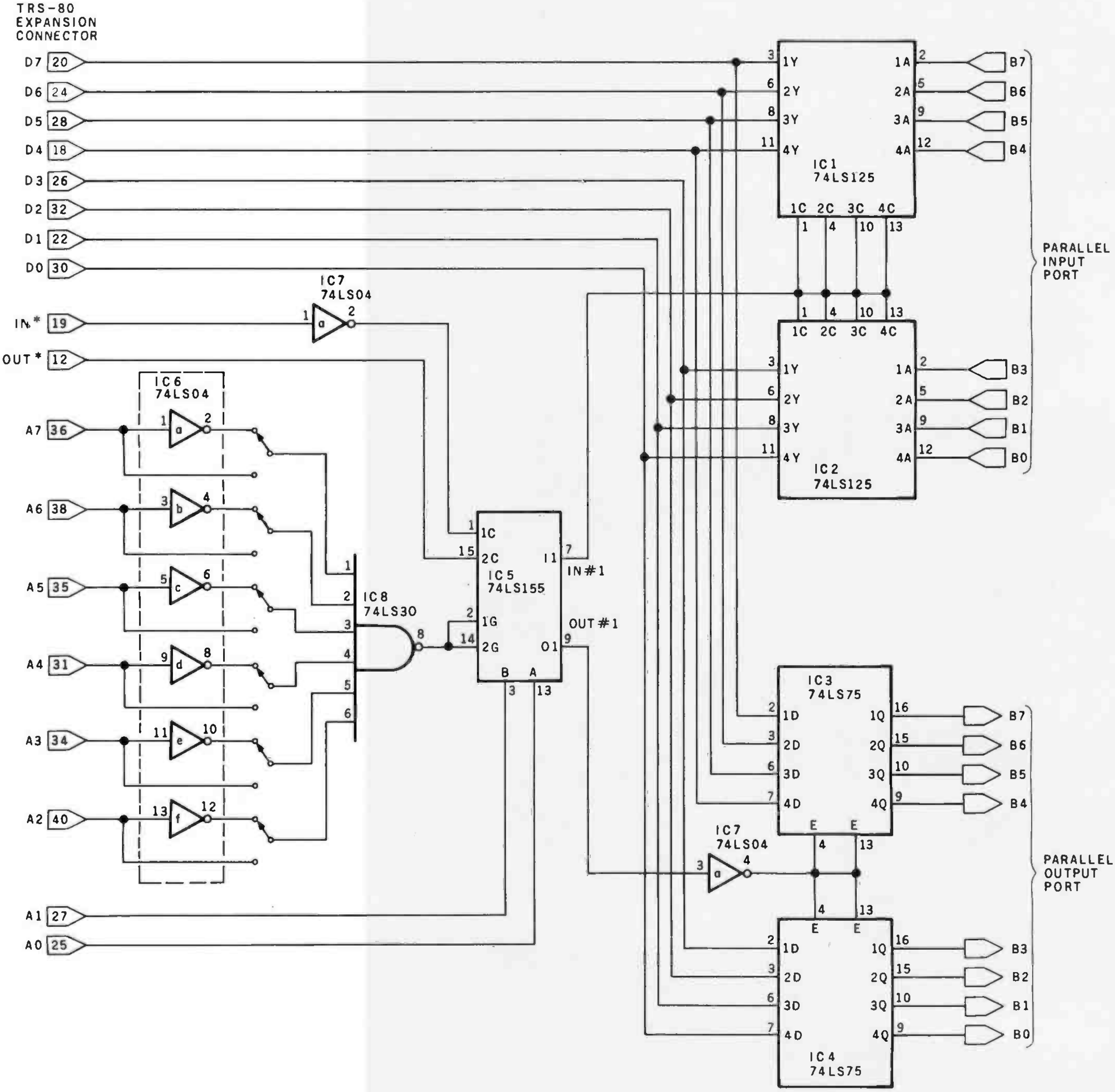

Figure 7: *A complete, economical, parallel I/O interface circuit for use with the Radio Shack TRS-80 computer, or with other computers that use a similar bidirectional data bus. This interface can be connected directly to the expansion connector at the rear of the TRS-80 keyboard/processor unit, or it can be connected through the expansion-interface unit. As the circuit is shown here, there are six presently undefined additional strobes available on IC5. These six strobes can be used to support three additional ports. Refer to figure 3 and figure 4 to determine the proper selection of the I/O port address for this interface.*

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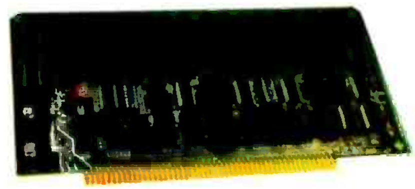

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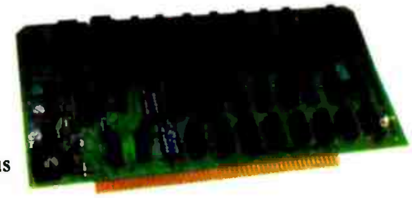

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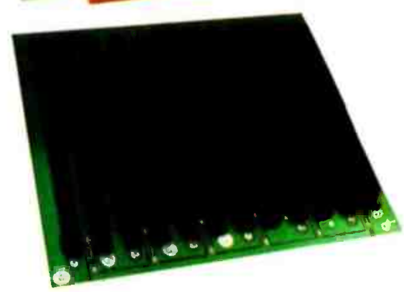

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parallel output ports for the TRS-80. The interface shown in figure 7 provides one input and one output port. The signals necessary to drive this interface are available on the forty-pin expansion connector of the keyboard/processor unit or on connector J2 on the expansion interface. In either case, a separate +5 V supply is necessary to power the circuit. The signals on the expansion connector are listed in table 1, and the pinouts are shown in figure 8.

The schematic diagram of figure 7 shows a port address FF. To set another port address simply refer to figure 3 and 4 and place the switches for the proper code.

There are many other methods for implementing I/O capability. An 8255 programmable peripheral interface, a parallel I/O device, could have been used. The circuit I have chosen to present is intended to be inexpensive and easy to operate. By minimizing potential parts-acquisition problems and keeping down the software handshaking necessary when using large-scale circuits like the 8255, I hope to enable many TRS-80 owners to build the circuit and use it to attach other "Circuit Cellar" projects to their computer system.

I hope to enable many TRS-80 owners to build this I/O circuit and to use it to attach other "Circuit Cellar" projects to their computer systems.

Those experimenters who hesitate to build hardware might want to purchase the entire communications interface. An assembled and tested unit, with power supply and containing a parallel port (for the Centronics printer) and a serial RS-232C-compatible interface, is available. The complete communications unit, called the COMM-80, will be presented in part 2 of this article and is available for $179.95 from:

MicroMint Inc
917 Midway
Woodmere NY 11598
Telephone (513) 374-6793

(New York residents please add applicable sales tax.)

Pin Number	Signal Name	Description
1	RAS*	row-address strobe output for 16-pin dynamic memories
2	SYSRES*	system-reset output, low during power-up initialization or when the reset switch is depresssed
3	CAS*	column-address strobe output for 16-pin dynamic memories
4	A10	address output
5	A12	address output
6	A13	address output
7	A15	address output
8	GND	signal ground
9	A11	address output
10	A14	address output
11	A8	address output
12	OUT*	peripheral-write strobe output
13	WR*	memory-write strobe output
14	INTAK*	interrupt-acknowledge output
15	RD*	memory-read strobe output
16	MUX	multiplexer control output for 16-pin dynamic memories
17	A9	address output
18	D4	bidirectional data bus
19	IN*	peripheral-read strobe output
20	D7	bidirectional data bus
21	INT*	interrupt input (maskable)
22	D1	bidirectional data bus
23	TEST*	placing a logic 0 on this line causes a high-impedance condition on address lines A0 thru A15, data lines D0 thru D7, WR*, RD*, IN*, OUT*, RAS*, CAS*, and MUX
24	D6	bidirectional data bus
25	A0	address output
26	D3	bidirectional data bus
27	A1	address output
28	D5	bidirectional data bus
29	GND	signal ground
30	D0	bidirectional data bus
31	A4	address bus
32	D2	bidirectional data bus
33	WAIT*	processor-wait input, to allow for slow memory
34	A3	address output
35	A5	address output
36	A7	address output
37	GND	signal ground
38	A6	address output
39	—	on Level I machines: low-current +5 V output on Level II machines: no connection
40	A2	address output

Table 1: *Description of function for the pins on the expansion port at the rear of the TRS-80 keyboard/processor unit. This pin assignment is also used in expansion slots in the expansion-interface unit. This information is provided through the courtesy of Radio Shack, a division of Tandy Corporation.*

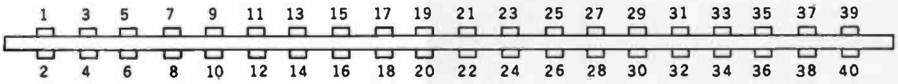

Figure 8: *The configuration of output pins on the expansion port on the rear of the TRS-80 keyboard/processor unit. See table 1 for an explanation of the function of each pin.*

Next Month

I shall complete the COMM-80 presentation by discussing the construction of a software-compatible RS-232C interface for the TRS-80 that has selectable data rates from 50 to 19200 bps. ■

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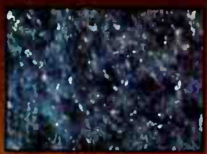 

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KIMDOS

Using Your KIM-1 with a Percom Floppy-Disk Drive

Joel Swank
4655 SW 142nd Apt 186
Beaverton OR 97005

Any owner of the MOS Technology KIM-1 knows the utility of the KIM's built-in audio-cassette interface. But, any KIM-1 owner who has expanded his system knows just as well how inappropriate the cassette is for storing long files. The standard KIM cassette format is intolerably slow, and even using the Hypertape method (a faster cassette-storage format for the KIM), a 4 K-byte file takes a minute and a half to load, not counting the time needed to position the tape.

The natural storage alternative is, of course, the floppy disk. However, there are some difficulties. A floppy-disk system requires a considerable amount of software to make it useful. In addition, many floppy-disk systems available today come with proprietary software for the 8080/Z80 or 6800 processors. Interfacing such systems to a KIM-1 requires the hobbyist to write his or her own 6502 software, working from the machine code for the other processor. While it is possible to do this, few hobbyists are willing to translate machine code to get their disk system up and running.

I decided to interface a Percom LFD-400 disk system to my KIM-1. The LFD-400 system contains a disk controller capable of controlling up to three 5-inch floppy-disk drives. It comes with complete, annotated source code for the 1 K-byte MINIDOS disk-operating system, written for the 6800 processor. MINIDOS allows the reading and writing of contiguous memory files, and is the nucleus of MINIDOS-PLUSX, a 6800-based disk-operating system sold by Percom.

KIMDOS is a KIM-1-compatible version of the Percom MINIDOS. It allows a KIM-1 to read and write files that are compatible with the Percom format. This article will concentrate on explaining the workings of the KIMDOS software. The LFD-400 system easily interfaces to the bus lines of any KIM-1 system (see table 1); because of this, hardware interfacing will not be discussed here.

The LFD-400 uses hard-sectored disks with ten 256-byte sectors per track and thirty-five tracks per disk. This gives 87.5 K bytes of usable data per disk. The controller board has sockets for up to 3 K bytes of 2708-type erasable programmable read-only memory (EPROM). KIMDOS has been written to fit in one 2708 device.

The controller board requires unregulated power supplies of +14 V, −14 V, and +8 V; or regulated power supplies of +12 V, −5 V, and +5 V. The controller is

Photo 1: *The author's personal computer system. It contains the following commercially built equipment: a MOS Technology KIM-1 microcomputer, three 8 K-byte Digital Group static memory boards, a Percom LFD-400 floppy-disk controller and two Shugart 5-inch floppy-disk drives, a Southwest Technical Products Corporation GT-6144 graphics board, an ACT-IA terminal with Leedex monitor, an Olivetti TE-300 hard-copy terminal, and several Lambda power supplies. Homebrew equipment in the system includes a programmer for erasable programmable read-only memories (EPROMs), a programmable integrated-circuit tester, a calculator interface, the motherboard, and the input/output (I/O) interface board.*
Photograph taken by John M Hannam.

composed of twenty-seven transistor-transistor logic (TTL) integrated circuits and the Z5023 universal synchronous receiver/transmitter (USRT) on a 15.24 by 25.4 cm (6 by 10 inch) two-sided printed-circuit board. Low-power Schottky (LS) components are used to reduce power consumption and minimize bus loading.

Floppy-Disk Drive

The Shugart 5-inch floppy-disk drive comes assembled and tested from Percom. A copy of the Shugart instruction manual is included in the system documentation; it is thirty-three pages long, and contains schematic diagrams and complete specifications for the drive and its operating principles. Trouble-shooting procedures are also detailed.

Each disk drive must be set up to respond to a specific drive number. This programming is accomplished by plugging a shunt block into a fourteen-pin dual-in-line pin (DIP) socket. A seven-pole DIP switch can replace the shunt block; the drive numbers may be easily changed using the switch.

Because the Shugart floppy-disk drive allows only three drive-select lines, the controller board in the Percom LFD-400 system uses only the drive-select lines that are numbered 01 thru 03. A drive-select line for device 00 exists, and can be selected by the KIMDOS software; however, this line is not usually connected to anything. With the addition of the proper jumpers to the controller and disk-drive boards, a four-drive disk system can be configured using device numbers 00 thru 03. The Micropolis disk drive could be used for this purpose, since it has a fourth drive-select line on pin 34 of the thirty-four-pin ribbon cable.

LFD-400	KIM Connector	Function	Comments
9	E-7	RST	
10	E-V	$R/\overline{W}$	
11	E-22	$\overline{VMA}$	VMA always true on KIM-1
12	E-U	ϕ_2	
19		+14 V	or use regulated +12 V
20		−14 V	or use regulated −5 V
21		+8 V	or use regulated +5 V
22		+8 V	
23		+8 V	
24	E-22	ground	
25		ground	
26		ground	
27	E-A	A0	
28	E-B	A1	
29	E-C	A2	
30	E-D	A3	
31	E-E	A4	
32	E-F	A5	
33	E-H	A6	
34	E-J	A7	
35	E-K	A8	
36	E-L	A9	
37	E-M	A10	
38	E-N	A11	
39	E-P	A12	
40	E-R	A13	
41	E-S	A14	
42	E-T	A15	
43	E-8	D7	
44	E-9	D6	
45	E-10	D5	
46	E-11	D4	
47	E-12	D3	
48	E-13	D2	
49	E-14	D1	
50	E-15	D0	

Table 1: *Hardware connections from the KIM-1 single-board computer to the Percom LFD-400 disk-drive controller. Also given is the function of each line used.*

Functions of the Controller

The LFD-400 uses a crystal oscillator to time the data and clock bits from the drive. The data is separated from the clock bits and is shifted into the universal synchronous receiver/transmitter. The USRT latches each 8-bit byte and sets a flag to notify the processor to read the byte. For a write operation, the USRT sets a flag when it is ready to receive data from the processor. After the processor has stored the data in the USRT, the data is shifted out, merged with the clock bits, and is sent to the drive.

The controller also takes care of maintaining the current sector count. The motor-control circuit contains a monostable multivibrator (commonly called a one-shot) that turns the motor off after about 3 seconds of nonuse. The drive select is a 2-bit number that is latched and decoded to select one of three drive-select lines, as discussed previously. The drive-select line for device 00 is not used. The step and direction bits are also latched. The track-0 and the write-protect lines are buffered for the microprocessor. Address decoding is provided for all controller addresses and for the 2708s. The data bus is buffered with 8835 three-state buffer devices.

Hardware Modifications

The only incompatibility between the KIM-1 and the LFD-400 lies with the use of a "low-true" logic convention on the SS-50 data bus. In the low-true convention, a voltage potential of 0.4 V or less is regarded as a true or binary 1 logic signal. This convention is used because the 8835 devices are *inverting* buffers.

The KIM-1 uses a high-true convention on its data bus; potentials of 3.5 V or greater are regarded as a true or binary 1 logic condition. To remedy this problem, I replaced the 8835 buffers with their noninverting counterparts, 8833 buffers. Since the disk-controller board does not have sockets, the 8835s had to be unsoldered. An alternative method would have been to write software that accepts and translates the inverted data coming from the controller, but the software method seemed more difficult and error-prone than the hardware method of replacing the three-state buffers.

My KIM-1 system has regulated voltage sources of +5 V, −12 V, and +12 V. I chose to bypass the

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LFD-400 regulators for +5 V and +12 V and drive the circuits that require these voltages directly from the system power supply. I fed the −12 V source into the −5 V regulator on the LFD-400 to obtain that regulated voltage.

The only other modification required was due to a problem with the oscillator circuit, which did not always start when the system was powered up. To correct this, I short-circuited the 0.001 μF capacitor near the crystal, effectively removing it from the circuit. According to the engineers at Percom Data Corporation, no one else has reported this problem.

There are five ten-pin Molex connectors on the controller board. Mates for these are available from Percom; however, it may be more convenient to simply remove the Molex connectors and replace them with another type. The pin numbers on the controller board and the KIM-1 equivalents are given in table 1.

Software and Hardware Interaction

All communication between the microprocessor and the disk controller takes place through hexadecimal memory addresses CC00 thru CC06. Because address lines A4 thru A9 are not decoded, addresses as low as hexadecimal CC10 to CC16 and as high as hexadecimal CFF0 to CFF6 also respond identically; but these addresses are not used. A complete list of controller addresses and functions is found in table 2.

The data on each floppy disk is arranged in thirty-five *tracks* or concentric circles. The motor rotates the disk at 300 rpm — one rotation takes 200 ms. Each track is divided into ten sectors in this hard-sectoring scheme.

In *hard sectoring,* the sector boundaries are detected by means of physical holes punched through the recording surface of the disk. As the disk rotates, these holes pass between a light-emitting diode (LED) and a photoelectric detector. Percom floppy disks have ten sector holes evenly spaced around the hub hole of the disk, with a single additional *index hole* placed halfway between two of the sector holes. This index hole is used to identify one sector on the disk as sector 0. Timing circuits in the controller detect the shorter distance between holes when the index hole passes the photodetector. When the index hole is detected by this method, the sector counter is reset.

Each sector occupies one tenth of the circumference of a track on the disk and passes across the disk data-transfer head in 20 ms. Data is written to the disk at a rate of 1 byte every 64 μs, theoretically giving room for up to 312 bytes per sector. It is not possible to fully use these 312 bytes. The Percom format uses a maximum of 287 bytes for leader, header, useful data, and trailer, with the data length variable from 1 to 256 bytes. Table 3 details the format of data stored in each sector.

Each track on the disk has ten sectors. The sectors are numbered in decimal from 000 to 349. In this three-digit numeral, the two high-order digits denote the track number in

2a

Hexadecimal Address	Function When Used as Input
CC00	Read USRT status: bit 0 = 1 means disk unit ready to send byte to computer at address CC01 during read operation bit 7 = 1 means disk unit ready to receive byte from computer at address CC01 during write operation
CC01	Address used to transmit data from disk drive to computer during read operation
CC02	During read operation, bits 0 thru 3 contain current sector number in binary
CC03	Drive status byte : see table 2b.
CC04	Accessing this location with a load instruction (LDA) causes a read operation to take place

2b

Bit	Value	Meaning
0	1	Write-protect notch in disk covered; disk is protected
1	1	Head is at track 0
2	0	Drive motor is on
3	0	Drive circuit is ready to write to disk
4	1	Sector pulse; drive detects sector hole
5	1	Index pulse; drive detects special index hole
6,7		Binary number of drive selected (01 thru 03)

Table 2: *Memory addresses used by the LFD-400 disk-controller board. Communication takes place between the disk and the computer via memory-mapped bytes as listed. Table 2a gives the function of 5 bytes used for input from disk to computer. Table 2b defines the permissible values of bits in the drive-status byte (hexadecimal location CC03). Table 2c gives the function of 7 bytes used to control output from the computer to the disk.*

2c

Hexadecimal Address	Function When Used as Output
CC00	Defines value that controller will recognize as the SYNC byte at the beginning of a read operation; hexadecimal FB used in Percom format
CC01	Address used to transmit data from computer to disk unit during write operation
CC02	Defines value that controller will recognize as the filler byte (written after trailer until disk motor turns off); hexadecimal FF used in this software
CC03	Data to select drive and head-movement direction: bit 4 = direction of head movement: 1 = in, 0 = out bit 5 = step pulse bit; causes data-transfer head to jump to next track in direction given by bit 4 bits 6, 7 = binary number of drive to be selected
CC04	Accessing this location with a store instruction (STA) causes a write operation to take place
CC05	Accessing this location with either a load (LDA) or store instruction causes a motor-on pulse to be sent to the disk drive
CC06	Accessing this location with either a load or store instruction causes a motor-off pulse to be sent to the disk drive

which the sector is located. The low-order digit specifies the sector within the track. When we prefix this three-digit numeral with the number of the disk drive, we obtain the *external* drive/track/sector (DTS) number, a four-digit quantity which is stored in binary-coded-decimal (BCD) form in 2 bytes.

For use in actual disk-addressing operations, the external DTS number is reformatted into a binary, *internal* drive/track/sector number. The internal DTS number has the following properties. The number of the disk drive (1 thru 3) is stored in binary form in the 2 high-order bits of the first byte of the internal DTS number. The track number (1 thru 34) is stored in the 6 low-order bits of the first byte. The individual sector number (1 thru 9) is stored in binary form in the second byte.

While the reformatting of the drive and track numbers from external to internal format involves only a simple decimal-to-binary conversion, the reformatting of the sector number employs a technique called *alternating-sector addressing*.

Why is alternating-sector addressing necessary? The sectors of the spinning disk pass under the read/write head consecutively, and there is no time between sectors during which the disk-operating system can perform housekeeping functions. While KIMDOS is performing the housekeeping routines for one sector, the next sector is already passing the head. Since housekeeping and sector reading cannot take place simultaneously, reading the sectors in sequential order would require the computer to wait for a full rotation of the disk to occur to read the sector that passed the head during housekeeping. Since every sector must be treated this way, only one sector could be read during each rotation of the disk if sectors were to be read sequentially. To remedy this problem, the sequential sector numbers are converted into alternating sector numbers.

KIMDOS reads or writes alternate sectors on the disk; the disk must rotate twice for all sectors on the track to be read or written. The order of physical sectors is therefore not the order of logical sectors. In the two complete rotations of the disk, the physical sectors are read in the following order: 0, 2, 4, 6, 8 (first rotation); 1, 3, 5, 7, 9 (second rotation). Sectors are accessed alternately to allow time in between data-transfer operations for executing housekeeping routines.

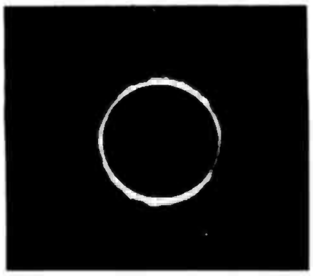
Each sector contains a *sector header* that holds information about the sector and the file of which it is a part. The first two bytes of the sector header contain the DTS number of the current sector; this is used to assure proper head position when reading. Each sector is linked via a forward pointer to the next sector and via a backward pointer to the previous sector. A forward pointer equal to 0 indicates the last sector in a file; a backward pointer equal to 0 indicates the first sector in a file.

The header also contains a data-length byte, a file-type byte, and the

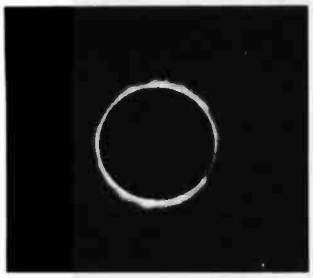
Text continued on page 158

Field Name	Length in Bytes	Contents
Leader	16	Binary zeros
Sync	1	Hexadecimal FB to indicate start of data
Current DTS number	2	Drive/Track/Sector numbers of this sector
Backward link	2	DTS number of previous sector in file
Forward link	2	DTS number of next sector in file
Byte count	1	Length of data in this sector, in hexadecimal (00 means hexadecimal 100)
Target address	2	Address of memory from which data was written
File type	1	Indicator of the nature of the data
Data	1 to 256	Data being stored
Check sum	2	2-byte cyclic redundancy check sum of all bytes after sync byte
Trailer	2	DTS number of first sector of this file, or execution address if this is last sector in this file

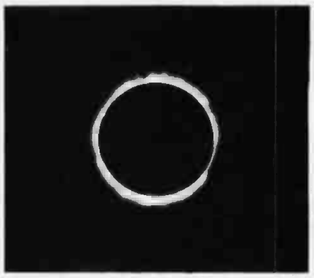
Table 3: *Table of sector fields and format. The drive/track/sector (DTS) number, stored here in internal binary format, points to a given sector.*



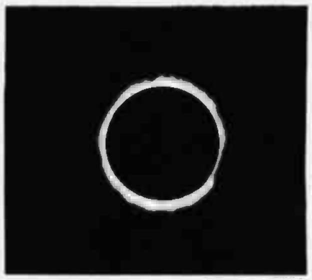
(3a) 1 millisecond



(3b) 2 milliseconds



(3c) 5 milliseconds



(3d) 10 milliseconds

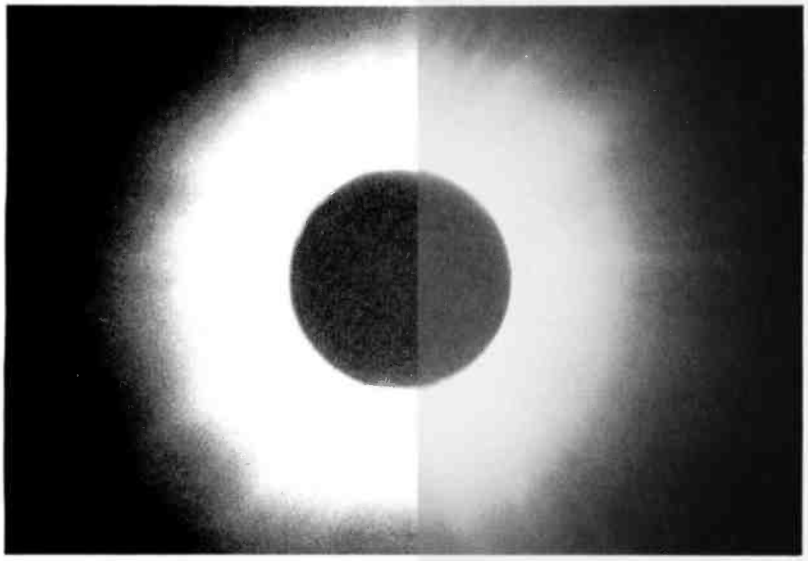


Photo 1: *A 5-second exposure with ASA 64 Ektachrome brings out significant coronal detail twice per 25-exposure cycle.*

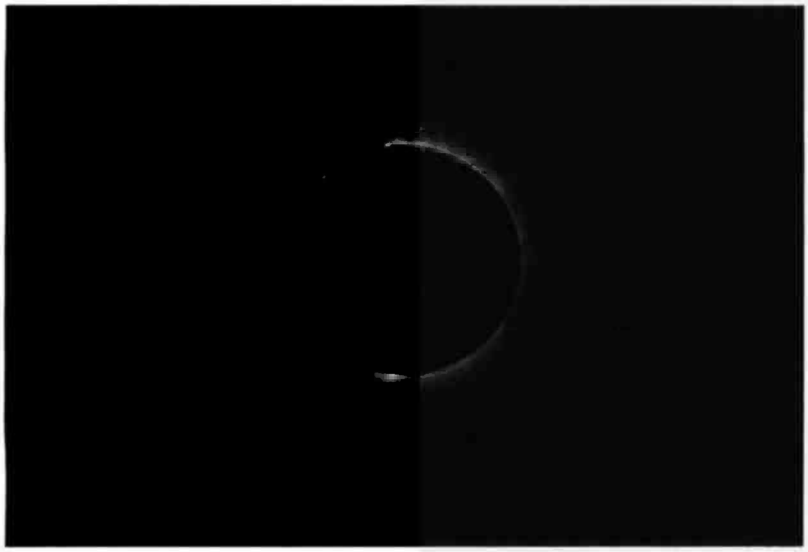


Photo 2: *A minimal length exposure shows the beginnings of some prominence detail and the inner corona. This exposure corresponds to the shortest nominal exposure time, 1 ms plus the minimum trigger-pulse width of 20 ms. The electromechanical system which is the Nikon MD-2 Motor Drive unfortunately has a minimum shutter-open time on the order of 20 ms. Thus the exposures nominally programmed at 1, 2, 5, and 10 ms were actually on the order of 21, 22, 25, and 30 ms.*

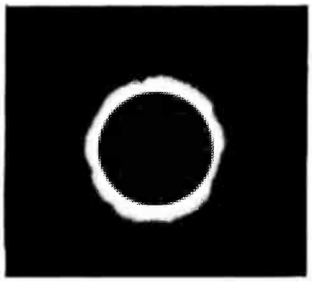
Text continued from page 6:

With this crucial timing step completed, I turned my attention to refining the Pascal program shown as listing 1 in the March 1980 BYTE editorial. These refinements included one conceptual change and some trivial changes in the experiment's design.

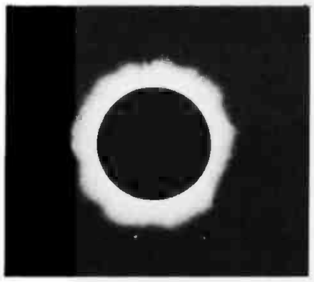
The conceptual change was that of adding a single long exposure made during the "slack time" interval at the end of the eclipse sequence during totality. As noted earlier, the model for the eclipse photography sequence used two manual inputs: one to start a sequence of diamond-ring exposures followed by automatic totality photography, and a second manual input to start the final diamond-ring sequence after a "slack time" for synchronization. My conceptual change was to open the shutter of the camera during this slack time, thus allowing one extremely long exposure to take place while waiting for the second manual input. Thus by specifying a smaller number of exposures during totality and a longer slack time, I would obtain this one long exposure.

The relatively trivial changes began with the alteration of the table of exposure times to provide a total of twenty-five different times instead of ten. In making this change I used the UCSD text editor to change the name of the table in every occurrence throughout the program. I also changed the initialization to provide a 1, 2, 5 sequence of exposure times in each decimal order of magnitude. (See photo 3's captions for the values resulting.)

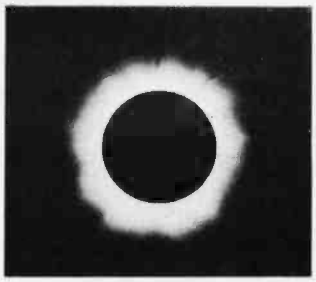
Another relatively minor change was to allow multiple tries at allocation of the exposures, rather than falling inexorably into a run of the photography sequence. This change proved quite useful in the field where it provided a means of verifying that



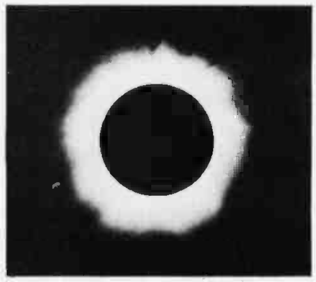
(3e) 20 milliseconds



(3f) 50 milliseconds



(3g) 0.1 second



(3h) 0.2 second

the computer had not died in the last minutes prior to totality. The program also had to be modified to talk to a 40-character-wide field on the Apple II video display instead of the 80-character width available on the terminal I normally use. This change amounted to condensation of the texts displayed during the allocation procedures. The final form of the program as used by the shores of Lake Jipe on February 16, 1980 is shown in listing 1.

The final equipment check prior to leaving was the verification that the display on a 2-inch diagonal Sanyo television screen was adequate. A jumper cord once used to interface between a tape recorder and my old homebrew computer provided the means for routing the output of the Apple's auxiliary RF modulator to the Sanyo television. The display wavered a bit when running on the portable generator. It was a tiny display but adequately readable for my purposes.

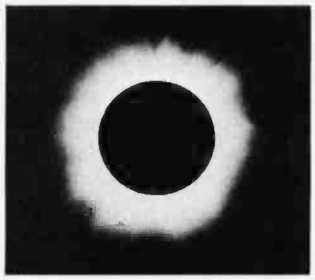
After this crucial experiment, the final detail was to make redundant copies of my eclipse application program's disk, as well as the UCSD Apple Pascal system's disks Apple1, Apple2, and Apple3. Redundancy was important. If I were to have a directory crash due to dust or dirt while on the other side of the equator 11,000 miles from home, a second chance would have been well worth it.

On Tuesday morning February 5, we hastened to Boston where the air travel to Kenya began with a trip to New York's Kennedy Airport. The party at this time consisted of myself, Tully Londoner, Norm Whyte, and Laurel Allen. Rick Lutman, the fifth member of our party, would join us in Nairobi. In due course we boarded Pan American's flight 190, an 18-hour international puddle jumper with stops at Roberts Field, Liberia, and Lagos, Nigeria. The computer equipment and telescope mount in addition to trunks and pack frames full of clothes, sleeping bags, and tools constituted our luggage.

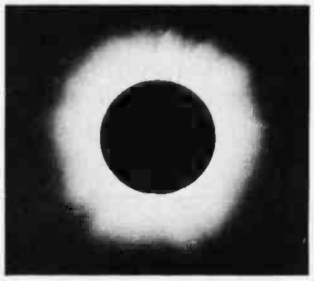
On reaching Nairobi at about 8 PM that Wednesday, we met our guide, Iain Allan, and his associate Vince Fayad. Iain does business as Tropical Ice (Mountain Guides) Ltd, Post Office Box 57341, Nairobi, Kenya. Making the connection with Iain was the only redeeming virtue of an otherwise hopelessly botched set of travel arrangements made by our US travel agents (who shall remain anonymous). Iain was our guide to the wilds of Kenyan culture for the next two weeks. His good humor and knowledge of local flora, fauna, and climate are highly recommended to anyone traveling in East Africa for purposes of game trekking or technical mountain climbing. Iain wrote the guidebook on Mt Kenya and other climbs in Kenya. He also frequently guides technical climbing trips on Tanzania's Kilimanjaro, when not tackling various other challenging rock climbs in places as diverse as Nepal and Yosemite.

As in any trip of this kind, there were some difficulties. The most significant (and in retrospect, completely avoidable) difficulty was the need to post a 30,000 shilling bond on our equipment with Kenyan customs on entry. We later had to recover our customs bond on departure (minus an exorbitant 10% fee exacted by the local branch of a major US multinational bank). The fact that we had to post a bond at all was due to an un-

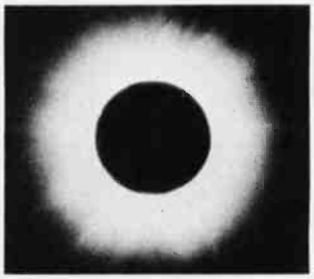
Photo 3: *Black and white reproductions of the entire series of different exposures taken with the aid of the final version of the Pascal control program for the camera. Times are nominal shutter-open intervals stored in a table in the program. Actual times reflect a fixed lower-limit overhead of approximately 20 ms.*



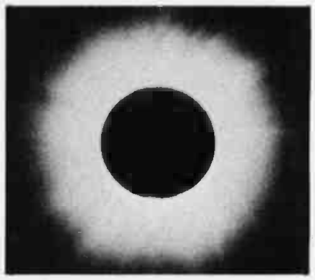
(3i) 0.5 second



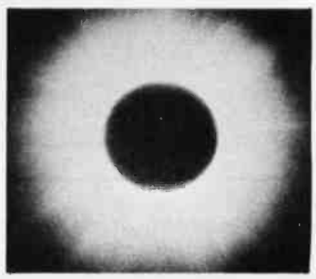
(3j) 1.0 second



(3k) 2.0 seconds



(3l) 5.0 seconds



(3m) 10.0 seconds

fortunate mistake by one of our party, a slipup which can possibly be avoided by readers in similar circumstances.

When listing personal computer equipment being carried for such an expedition, never ever list its monetary value or speak of its value. To satisfy US customs, all you need is a list of serial numbers of your personal equipment carried abroad. This list can be used to advantage when entering another country. But if you give the customs officer at another country the list of items and values you prepared for your insurance agent, it is like waving a red flag in front of a bull.

We had to post a customs bond on Norm's equipment using credit cards to obtain nearly $4000 in cash, then retrieve the cash bond at the end of the trip by pleading lack of time to Kenyan customs officials in order to get all the paperwork completed by our departure. We wasted two out of sixteen days figuring out all the "catch-22"-style sophistries of this problem.

Kenya is a very British relic of a former era, where dual languages of Swahili and English dominate. Iain pointed out that it would have been much more complicated in several countries in which he has traveled for purposes of mountain climbing. In one Asian country he has visited for climbing, Iain points out, there is not even a recognizable set of paperwork to be filled out. It was quite a relief to get back to a (relatively) sane United States at the end of the trip.

So much for the bureaucratic problems of taking computers abroad to equatorial Africa. What about the engineering problems? We did as thorough a job of preparation as we could, yet would the computers and generator still play together when we reached our final encampment on the shores of Lake Jipe in Kenya's Tsavo West National Park?

We answered this question by an ancient technique: crossing fingers and applying power. We arrived at Lake Jipe 2 days before the eclipse, after a 6-hour trek over some incredible roads in Iain's Volkswagen bus with trailer in tow. The computers were inside the bus with seven human bodies and food packed with solid CO_2 in the famous Tropical Ice Box. All the rest of our gear was carried in the trailer. The roads we traveled from Amboseli to Lake Jipe included one 5-mile stretch of a semi-improved lava flow, an unmarked dead end which looked like the main road of two alternatives, and other miscellaneous "hazards" like herds of elephants and troops of baboons.

The day before the eclipse, Norm

Photo 4: *A view of the equipment set up at the Tsavo West National Park campsite on the shores of Lake Jipe. Norm was using a 500 mm reflex lens with his camera; I was using my 1000 mm reflex lens. The two Nikon cameras were mounted on the equatorial telescope mount carted to Africa along with the 110 VAC generator in Norm's homebrew plywood shipping trunk. The Apple Pascal system is shown sitting in the bottom of its carrying case on top of a trunk.*

Listing 1: *This is the final version of my Pascal Eclipse Control Program as used in Kenya, February 16, 1980. Major changes from the previously published version include filling in the details of real-time execution and modifying the exposure table to provide twenty-five shots instead of ten. Also added was an interactive option to reenter the the exposures allocation phase so that different combinations of diamond ring and totality exposures could be tried. Initialization now puts in a symmetrical rising and falling sequence of exposure times from 1 ms to 10,000 ms. All interactive texts have been adjusted so that they will fit the 40-character width of the Apple's built-in video display.*

```
{     N O T E S   A B O U T   T H E   D E S I G N   P R O C E S S   }
{}
{    Step 1: High Level Description  - begun November 22, 1979          }
{         This is a first cut at a program to simulate the eclipse      }
{      photography process, and define some of the necessary global     }
{      data of the problem.                                             }
{                       COMPLETED 11/24/79                              }
{}
{    Step 2: Fill in allocation details -                               }
{         Achieve a complete allocation of the eclipse camera con-      }
{      trol function as evidenced by calculation of a detailed time     }
{      line for the eclipse event given various conditions:             }
{              Given:                                                   }
{                 n   = number of totality exposures                    }
{                 m   = number of diamond ring exposures                }
{                 t   = totality time                                   }
{                 s   = slack in allocated totality time                }
{              Then let us seek the following...                        }
{               * d2  = diamond ring time at 2nd contact                }
{               * d3  = diamond ring time at 3rd contact                }
{               * z   = extra slack (one half of diamond ring total)}
{               * p   = anticipation time (half first diamond ring)     }
{               * A   = required time for exposures during totality     }
{               * a   = allocated totality time for exposures           }
{               * x   = margin per frame in totality                    }
{              Theorems:                                                }
{                 d2,d3 derived from table of diamond ring frames       }
{                 A   derived from table of totality frames             }
{                 z = (d2 + d3)/2                                       }
{                 p = d2 / 2                                            }
{                 a = t - s - z                                         }
{                 x = (a - A) / n                                       }
{                                                                       }
{            PROCEDURES Detailed Here Are...                            }
{               initialize                                              }
{               normalize                                               }
{                       COMPLETED 12/16/79                              }
{}
{    Step 3: Fill in the simulated details...                           }
{         Create a program which uses the results of step 3 to          }
{      go through a detailed time line of the experiment on paper       }
{      (or terminal screen).  Each event (shutter transition            }
{      open-->close or close-->open will be marked by a report of       }
{      its nature and time of execution relative to <start> signal      }
{                                                                       }
{            PROCEDURES Detailed Here Are...                            }
{               await_cue                                               }
{               diamond_ring_burst                                      }
{               totality                                                }
{}
{    Step 4: Adapt to real time control -                               }
{         Put in augmentations of the software to actually demon-      }
{      strate operation with the Nikon F2A camera via a relay           }
{      plugged into the Apple II Game Paddle Socket                     }
{      THIS IS THE FINAL FORM OF THE PROGRAM TO BE USED IN THE          }
{      FIELD CONTROLLING THE EXPERIMENT...                              }
{         Necessary step: determining a method of measuring time        }
{      intervals from the CPU clock which is consistent with UCSD       }
{      Pascal.  Possibly use assembly language subroutine.              }
{}


PROGRAM eclipse_monitor_simulation;


   CONST
      minimum_pulse_width = 20 {milliseconds};
      overhead_duration = 210 {milliseconds};
      open_shutter_address  = -16295 {sets AN0 output to "1"};
      close_shutter_address = -16296 {resets AN0 output to "0"};
      post_ring_delay = 500 {milliseconds};

   TYPE
      seconds      = INTEGER;
      milliseconds = INTEGER;
      absolute_time =
         RECORD
```

Listing 1 continued on page 58

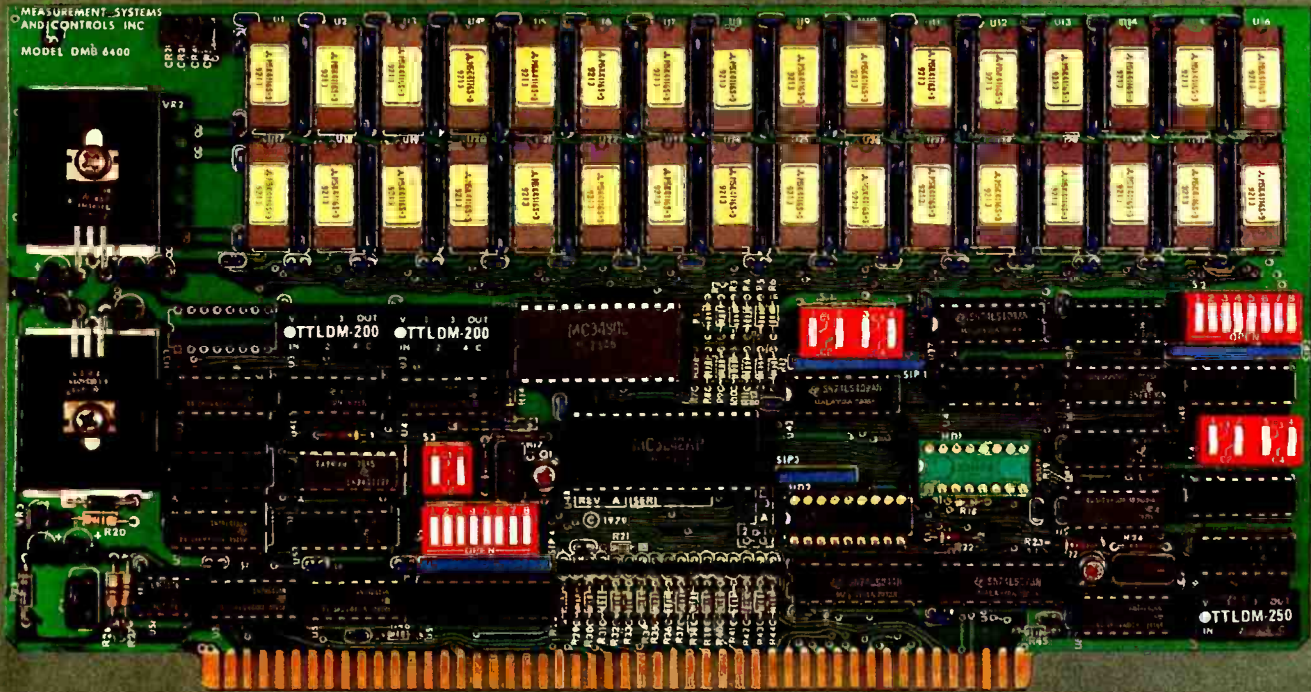
fired up the generator to supply power. We then set up our respective Apples. We naively thought that final programming details could be accomplished that day sitting in the tropical sun. But our preparations had neglected to include a canopy or sun shade. Norm's Apple worked quite well in the heat, perhaps because he had rigged up a sort of sun shade using his towel, two camera tripods, and a large piece of gaily colored cloth.

My Apple, however, had been baking in its carrying case all morning before I set it up. Its integrated circuits were hot to touch even before I turned it on. I turned it on and Pascal booted as usual. I entered my eclipse program and proceded to check it out. But after one or two allocation runs, the operation of the program was rather unusual and erratic. As often happens in such situations, I cycled the power switch in order to reboot the system's software. With this, the system simply refused to operate in a normal fashion! After leaving the system off for about 2 minutes, I was again able to get it started. But it crashed again more quickly.

My conclusion was that the direct sunlight was baking my computer, giving it the electronic equivalent of the sunburn I was so carefully avoiding for myself. It seems that Apples do not work too well when temperatures are elevated to the point where components are too hot to touch. I estimate that the surface temperature of the main board at this time was in the range of 150° to 180°Fahrenheit (66° to 82° Celsius). Noting the excessive heat, I just turned off the system and thought about strategies for keeping it cool and out of sunlight until the eclipse happened. That evening after sunset and before the nightly parade of hippos began, I verified that the computer was still functional.

As it turns out, heat was not a problem the next day, February 16, 1980. The day of the eclipse broke with a solid overcast, not an auspicious beginning. If first contact were to have occurred at 8:30 in the

Text continued on page 66



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Listing 1 continued:

```
            units        : seconds;
            thousandths  : milliseconds
         END;
      exposures     = INTEGER;
      an_exposure_detail =
         RECORD
            duration     : milliseconds;
            wait_after   : milliseconds
         END;
      string_pointer = ↑STRING;


   VAR
      s                    : STRING[128];
      crash_ahead          : BOOLEAN;

      an_integer         : INTEGER;

      x,n                  : INTEGER;
      sigma                : INTEGER;
      which_ring           : (second,third);

      a,b,c                 : absolute_time;
      ring_time             : absolute_time;
      second_contact_ring   : absolute_time;
      third_contact_ring    : absolute_time;
      tot_time              : absolute_time;
      time_totality         : absolute_time;
      margin_time           : absolute_time;
      current_time          : absolute_time;
      half_time             : absolute_time;
      quarter_time          : absolute_time;
      slack_in_totality     : absolute_time;
      dummy                 : absolute_time;
      total_elapsed_time    : absolute_time;
      total_duration        : absolute_time;

      maximum              : exposures;
      total_eclipse         : exposures;
      ring_frames           : exposures;
      current_shot          : exposures;

      twenty_five_shots : PACKED ARRAY[0..24] OF an_exposure_detail;
      transient_shots   : PACKED ARRAY[0..1] OF an_exposure_detail;

<<<< opening "EUTILS.TEXT">>>>

(    Miscellaneous routines used throughout the program )
(       ---> new_page               )
(       ---> set_parameter          )
(       ---> error_abort            )
(       ---> subtract_time          )
(       ---> divide_time            )
(       ---> add_time               )
(       ---> print_time             )
(       --->                        )
(       --->                        )
(       --->                        )
(       --->                        )
(       --->                        )



   PROCEDURE new_page;
      VAR
         stuff : STRING[24];
         clear_screen : CHAR;
      BEGIN
         stuff := '                        ';
         clear_screen := CHR( 24 );
         WRITELN( clear_screen,stuff );
         WRITELN( ' ' );
         WRITELN( ' ' );
         WRITELN( s )
      END (new_page);

   PROCEDURE set_parameter( VAR time : absolute_time );
      VAR
         a_string : STRING[128];
         i : INTEGER;
         period : BOOLEAN;
         decimal_count : INTEGER;
         factor, result : INTEGER;

         PROCEDURE add_a_digit( position : INTEGER );
            VAR
               digit : INTEGER;
            BEGIN
               digit := ( ORD( a_string[position] )-ORD( '0' ));
               IF period THEN
                  BEGIN
```

Listing 1 continued on page 60

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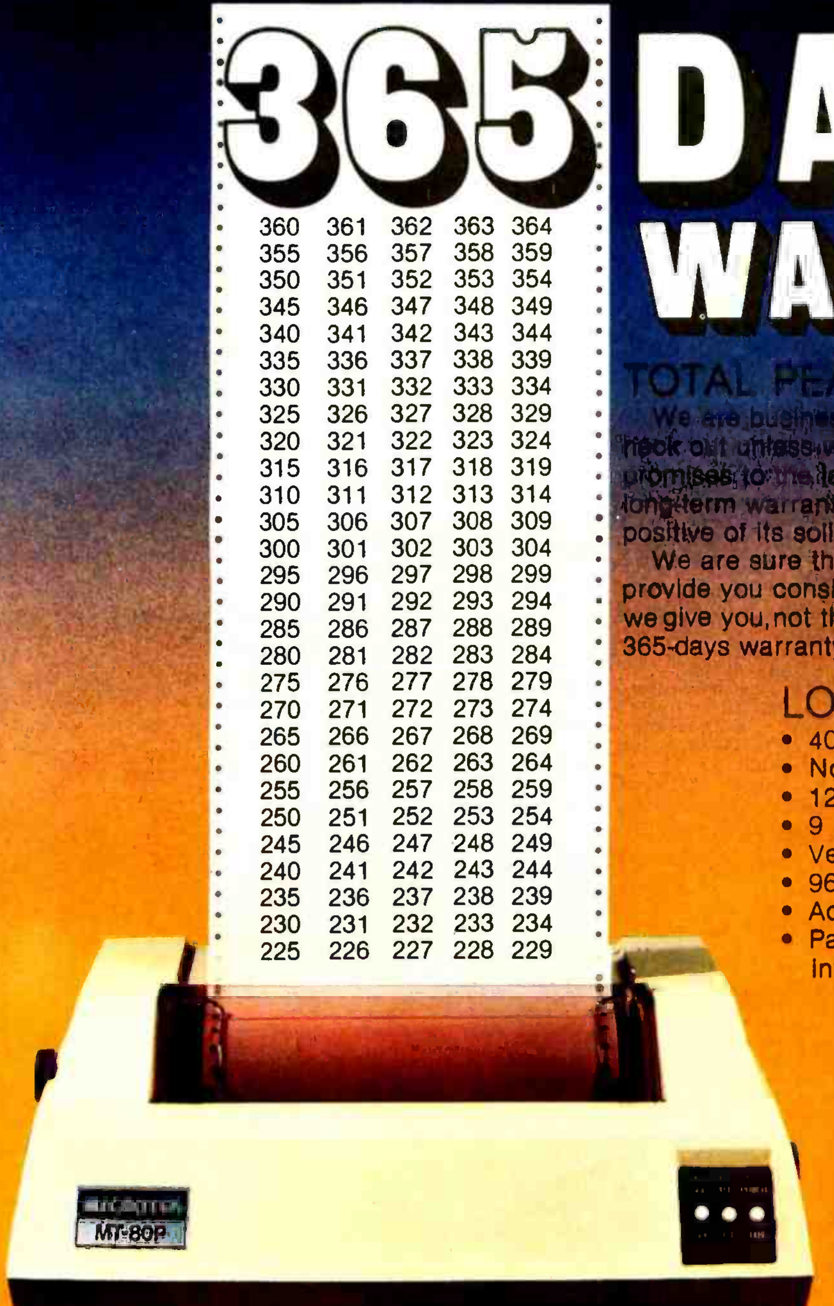

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Listing 1 continued:

```
                        decimal_count := decimal_count + 1;
                        IF decimal_count < 4 THEN
                           BEGIN
                              time.thousandths := time.thousandths
                                    + ((1000 * digit) DIV factor);
                              factor := 10 * factor
                           END
                     END
                  ELSE (before period)
                     time.units := (time.units * factor) + digit
               END;

         BEGIN (set_parameter)

         PAGE(OUTPUT);
         time.units := 0;
         time.thousandths := 0;
         WHILE ((time.units=0) AND (time.thousandths=0)) DO
            BEGIN
               factor := 10;
               decimal_count := 0;
               period := FALSE;
               WRITELN(s);
               READLN(a_string);
               FOR i := 1 TO LENGTH(a_string) DO
                  BEGIN
                     CASE a_string[i] OF
                        '0','1','2','3','4','5','6','7','8','9':
                           add_a_digit(i);
                        '.':
                           period := TRUE
                     END
                  END
            END (WHILE)
      END (set_parameter);

PROCEDURE error_abort;
   BEGIN
      maximum := 250;
      total_eclipse := 200;
      ring_frames := 25;
      WRITELN('Unrecoverable error in data');
      crash_ahead := FALSE
   END;

PROCEDURE subtract_time(a,b : absolute_time; VAR c : absolute_time);
   BEGIN
      c.thousandths := a.thousandths - b.thousandths;
      sigma := 0;
      IF c.thousandths < 0 THEN
         BEGIN
            c.thousandths := c.thousandths + 1000;
            sigma := -1
         END;
      c.units     := a.units     - b.units     + sigma
   END;

PROCEDURE divide_time(
                          VAR a : absolute_time;
                          b : absolute_time;
                          n : INTEGER
                          );
   ( a <-- b DIV n )
   VAR
      p,q : INTEGER[16];
   BEGIN
      a.thousandths := 0;
      a.units := 0;
      q := b.units;
      q := q * 1000;
      q := q + b.thousandths;
      q := q DIV n;
      p := q DIV 1000;
      IF p < 32768 THEN
         a.units := TRUNC(p);
      p := q - (1000 * p);
      IF p < 32768 THEN
         a.thousandths := TRUNC(p)
   END;

PROCEDURE add_time(a,b : absolute_time; VAR c : absolute_time);
   BEGIN
      sigma := a.thousandths + b.thousandths;
      c.thousandths := sigma MOD 1000;
      c.units     := a.units     + b.units     + (sigma DIV 1000)
   END;

PROCEDURE print_time(a : absolute_time);
   VAR
      z1000,z100 : STRING[1];
   BEGIN
      IF a.thousandths < 100 THEN z1000 := '0' ELSE z1000 := '';
      IF a.thousandths < 10 THEN z100 := '0' ELSE z100 := '';
      IF LENGTH(s) > 25 THEN s := COPY(s,1,25);
      WRITELN(s,a.units,'.',z1000,z100,a.thousandths)
```

Listing 1 continued on page 62

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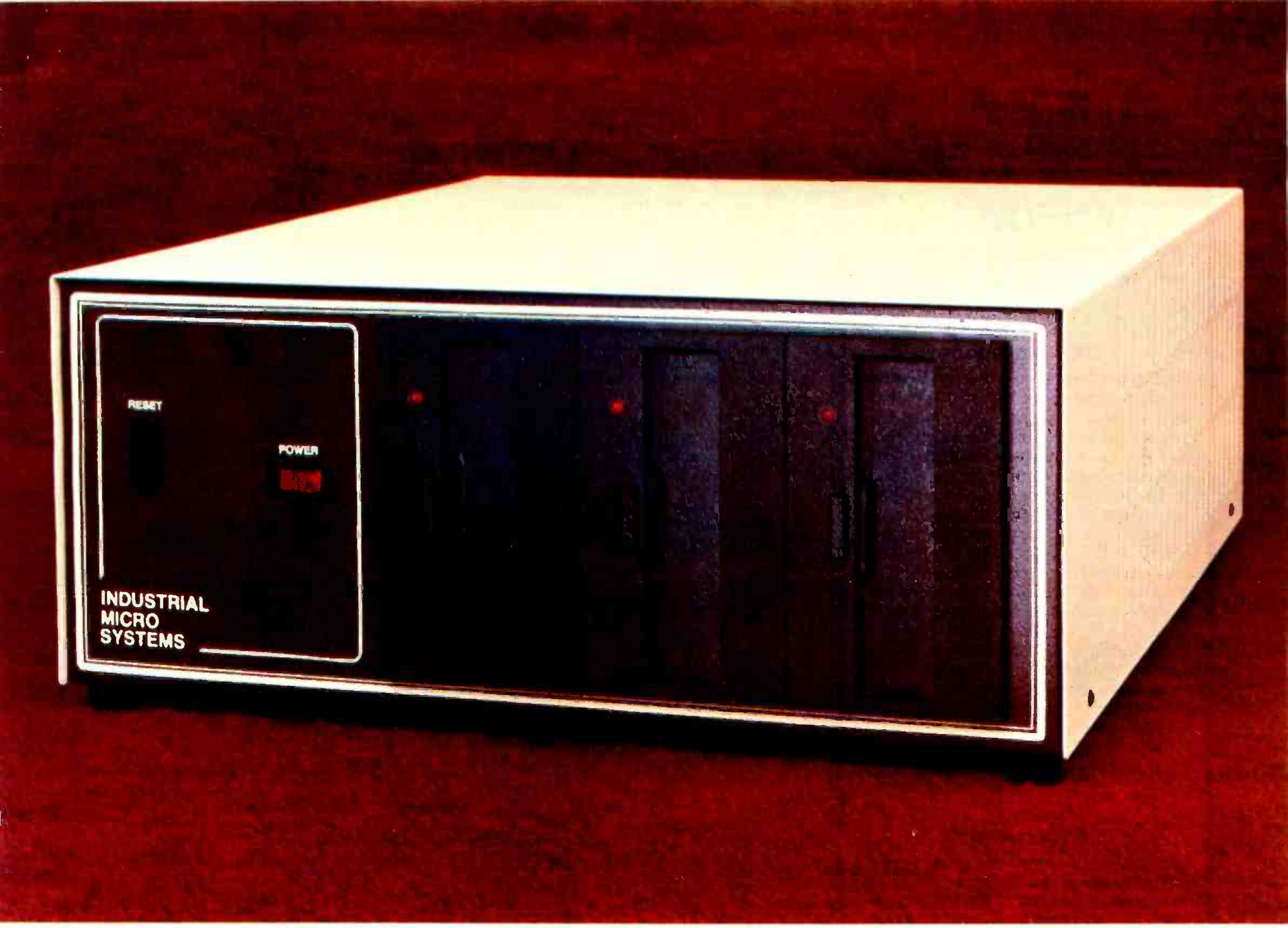
Listing 1 continued:

```
        END;
<<<< opening "ENORMAL.TEXT>>>>

PROCEDURE normalize_timing;
   VAR
      i                   : INTEGER;

   PROCEDURE sum_up_ring(ring: INTEGER; VAR ring_total : absolute_time);
      VAR
         index,i : INTEGER;
         this_ring : absolute_time;

      BEGIN
         ring_total.units         := 0;
         ring_total.thousandths   := post_ring_delay;
         FOR i := 1 TO ring_frames  DO
            BEGIN
               this_ring.units := 0;
               this_ring.thousandths := transient_shots[ring].wait_after;
               add_time( this_ring,ring_total,ring_total );
               this_ring.thousandths := transient_shots[ring].duration;
               add_time( this_ring,ring_total,ring_total )
            END
      END;

   PROCEDURE sum_up_eclipse( VAR eclipse_total : absolute_time );
      VAR
         this_shot : absolute_time;
         index,i,j : INTEGER;
      BEGIN
         eclipse_total.units := 0;
         eclipse_total.thousandths := overhead_duration;
         ( this compensates for the minimum wait after one      )
         ( frame started and ended during the slack time period)
         FOR i := 1 TO total_eclipse DO
            BEGIN
               this_shot.units := 0;
               index := (i-1) MOD 25;
               this_shot.thousandths := twenty_five_shots[index].wait_after;
               add_time( this_shot,eclipse_total,eclipse_total );
               this_shot.thousandths := twenty_five_shots[index].duration;
               add_time( this_shot,eclipse_total,eclipse_total )
            END
      END;

PROCEDURE preliminary_allocation;
    BEGIN
       s := 'Allocation of Eclipse Times...';
       new_page;
       s := 'Total time of eclipse   = ';
       print_time( time_totality );

       WRITELN( '----------------------------------------' );
       which_ring := second;
       sum_up_ring( ORD( which_ring ),second_contact_ring );

       s := 'Second contact time     = ';
       print_time( second_contact_ring );

       which_ring := third;
       sum_up_ring( ORD( which_ring ),third_contact_ring );

       s := 'Third contact time      = ';
       print_time( third_contact_ring );

       add_time( second_contact_ring,third_contact_ring,ring_time );
       s := 'Tot. diamond ring time = ';
       print_time( ring_time );
       divide_time( quarter_time,second_contact_ring,2 );
       s := 'Anticipation time       = ';
       print_time( quarter_time );


       WRITELN( '----------------------------------------' );
       sum_up_eclipse( tot_time );
       s := 'Totality time           = ';
       print_time( tot_time );
       s := 'Margin at end totality = ';
       print_time( slack_in_totality );

       divide_time( half_time,ring_time,2 );
       s := 'Diamond ring slack      = ';
       print_time( half_time );

       add_time( tot_time,slack_in_totality,total_duration );
       add_time( total_duration,half_time,total_duration );
       s := 'Total time initially    = ';
       print_time( total_duration );

       WRITELN( '-----------------------------------------------------' );
       subtract_time( time_totality,total_duration,margin_time );
       s := 'Margin for allocation   = ';
       print_time( margin_time )
    END (preliminary_allocation);
```

Listing 1 continued on page 64



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Listing 1 continued:

```
PROCEDURE margin_dispersal;
   VAR
      margin_per_frame : absolute_time;
      i : INTEGER;
   BEGIN
      divide_time( margin_per_frame,margin_time,total_eclipse );
      FOR i := 0 TO 24 DO
         twenty_five_shots[i].wait_after :=
            twenty_five_shots[i].wait_after +
            (1000 * margin_per_frame.units) +
            margin_per_frame.thousandths;
      s := 'Margin per tot. frame  = ';
      print_time( margin_per_frame )
   END {margin_dispersal};

PROCEDURE final_allocation;
   BEGIN
      sum_up_eclipse( tot_time );
      s := 'Adjusted total phase   = ';
      print_time( tot_time );

      add_time( tot_time,slack_in_totality,total_duration );
      add_time( total_duration,half_time,total_duration );
      s := 'Adjusted commitments   = ';
      print_time( total_duration );

      add_time( tot_time,slack_in_totality,total_elapsed_time );
      add_time( total_elapsed_time,ring_time,total_elapsed_time );
      s := 'Total elapsed time     = ';
      print_time( total_elapsed_time );

      WRITELN( '-------------------------------------------------------' );
      subtract_time( time_totality,total_duration,margin_time );
      s := 'Margin after allocation= ';
      print_time( margin_time )
   END {final_allocation};

PROCEDURE alloc_exposures;
   BEGIN
      ring_frames :=
         (maximum - total_eclipse) DIV 2;
      IF ring_frames < 2 THEN error_abort;
      sigma := maximum - (total_eclipse + (2 * ring_frames));
      total_eclipse := total_eclipse + sigma;
      WRITELN( '' );
      WRITELN( '        Exposures map:' );
      WRITELN( 'First diamond ring  = ',ring_frames );
      WRITELN( 'Totality            = ',total_eclipse );
      WRITELN( 'Second diamond ring = ',ring_frames );
      WRITELN( '                      --------' );
      WRITELN( '        TOTAL       = ',maximum );
      WRITELN( '' );
      WRITELN( '' );
      WRITELN( 'Press return to continue' );
      READLN( s )
   END {alloc_exposures};

   BEGIN {normalize_timing}

      alloc_exposures;

      preliminary_allocation;

      margin_dispersal;

      final_allocation

   END {normalize_timing};

PROCEDURE milli( time : INTEGER );
   EXTERNAL;

PROCEDURE ref_memory( address : INTEGER );
   { This procedure uses the variant record technique to
      reference an address passed to it as a 16 bit signed
      INTEGER.  The Apple-II hardware will set or reset the
      annunciator outputs of the Game I/O connector if the
      appropriate addresses are simply referenced by a program.
   }

   TYPE
      ptr = ↑CHAR;

      memory_access = (pointer,number)
      {this is a dummy statement required by the syntax of
         Pascal variant records such as "memory" below. The
         variant record "trick" is not the most elegant way
         to reference an absolute hardware address, since it
         requires an implementation-dependent assumption about
         variant records, ie: that a 16 bit signed two's complement
         INTEGER type maps bit for bit into the 16 bit positive
         integer value of an address stored in a Pascal pointer
         data type.
      };
```

Listing 1 continued on page 66

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Text continued from page 56:

morning as was the case in Montana last year, we would have missed the eclipse. But by the time of first contact, about 10 AM, the clouds had dissipated somewhat in the hot sun, to the point where maybe 50% of the time the sun was obscured. What this early cloudiness did, however, was keep my Apple from getting too hot too soon.

As the eclipse progressed, the air cooled off. Whether this lack of insolation due to the early phases of the eclipse affected the weather or not, it certainly helped guarantee the performance of my Apple during the total phase of the eclipse. At 11 AM when I turned on the power to my computer, it was delightfully cool in comparison with the previous afternoon. The weather had also improved considerably. We seemed by this time to be in a beautiful bowl of clear blue sky with the nearest clouds perhaps 5 to 10 miles away. This perfect eclipse-viewing weather lasted until well after the end of the event.

The Pascal system booted properly, and I proceeded to set up the final allocation I would use. Because I wanted to take a few partial phase shots manually, I had decided earlier that morning to limit the shots of totality to 200 exposures, with 120 taken during actual totality and the balance of 80 split equally between the two diamond-ring events. A slack time of 40 seconds was chosen to allow for the extra long exposure toward the end of the eclipse. Just to keep verifying the operation of the computer, I kept reentering the allocation phase of the program every few minutes.

Finally, at 11:21 AM, totality was heralded by a beautiful set of "shadow bands." After watching these last glimmers of direct sun, I removed the filter from my camera and gave the first manual cue to my eclipse program. I then had four enjoyable minutes of direct viewing of the eclipse, its effects on the local animal life, a glimpse of sunlight still illuminating the upper part of Kilimanjaro, and the incredible colorations of the distant clouds on the

Listing 1 continued:

```
      memory =
         RECORD
            CASE memory_access OF
               pointer : (a_pointer : ptr);
               number  : (a_number : INTEGER)
         END;

   VAR
      anybyte : memory;
      anychar : CHAR;

   BEGIN
      anybyte.a_number := address;
      anychar := anybyte.a_pointer↑
   END (ref_memory);

PROCEDURE take_picture(photograph : an_exposure_detail);
   BEGIN
      ref_memory(open_shutter_address);
      milli(photograph.duration);
      ref_memory(close_shutter_address);
      milli(photograph.wait_after)
   END (take_picture);



PROCEDURE initialize;
   VAR
      running_index : INTEGER;
   BEGIN (initialize)
      s := '';
      ref_memory(close_shutter_address);
      current_time.units       := 0;
      current_time.thousandths := 0;
      current_shot := 0;
      twenty_five_shots[0].duration    := 1     + minimum_pulse_width;
      twenty_five_shots[1].duration    := 2     + minimum_pulse_width;
      twenty_five_shots[2].duration    := 5     + minimum_pulse_width;
      twenty_five_shots[3].duration    := 10    + minimum_pulse_width;
      twenty_five_shots[4].duration    := 20    + minimum_pulse_width;
      twenty_five_shots[5].duration    := 50    + minimum_pulse_width;
      twenty_five_shots[6].duration    := 100   + minimum_pulse_width;
      twenty_five_shots[7].duration    := 200   + minimum_pulse_width;
      twenty_five_shots[8].duration    := 500   + minimum_pulse_width;
      twenty_five_shots[9].duration    := 1000  + minimum_pulse_width;
      twenty_five_shots[10].duration   := 2000  + minimum_pulse_width;
      twenty_five_shots[11].duration   := 5000  + minimum_pulse_width;
      twenty_five_shots[12].duration   := 10000 + minimum_pulse_width;
      twenty_five_shots[13].duration   := 5000  + minimum_pulse_width;
      twenty_five_shots[14].duration   := 2000  + minimum_pulse_width;
      twenty_five_shots[15].duration   := 1000  + minimum_pulse_width;
      twenty_five_shots[16].duration   := 500   + minimum_pulse_width;
      twenty_five_shots[17].duration   := 200   + minimum_pulse_width;
      twenty_five_shots[18].duration   := 100   + minimum_pulse_width;
      twenty_five_shots[19].duration   := 50    + minimum_pulse_width;
      twenty_five_shots[20].duration   := 20    + minimum_pulse_width;
      twenty_five_shots[21].duration   := 10    + minimum_pulse_width;
      twenty_five_shots[22].duration   := 5     + minimum_pulse_width;
      twenty_five_shots[23].duration   := 2     + minimum_pulse_width;
      twenty_five_shots[24].duration   := 1     + minimum_pulse_width;
      FOR running_index := 0 TO 24 DO
         twenty_five_shots[running_index].wait_after  := overhead_duration;

      transient_shots[0].duration    := 5      + minimum_pulse_width;
      transient_shots[1].duration    := 50     + minimum_pulse_width;
      FOR running_index := 0 TO 1 DO
         transient_shots[running_index].wait_after  := overhead_duration;

      s := 'Restarting the program';
      new_page;
      WRITELN('Enter 0 to end, 1 to continue');
      WRITELN('    then <return>        ');
      READLN(an_integer);


      IF an_integer > 0 THEN
         BEGIN
            s := 'Preliminary data initialization';
            new_page;
            s := '   Enter number of exposures';
            get_parameter(dummy);
            maximum := dummy.units;
            s := 'Enter exposures in totality';
            REPEAT
               BEGIN
                  get_parameter(dummy);
                  total_eclipse := dummy.units
               END
```

Listing 1 continued on page 68

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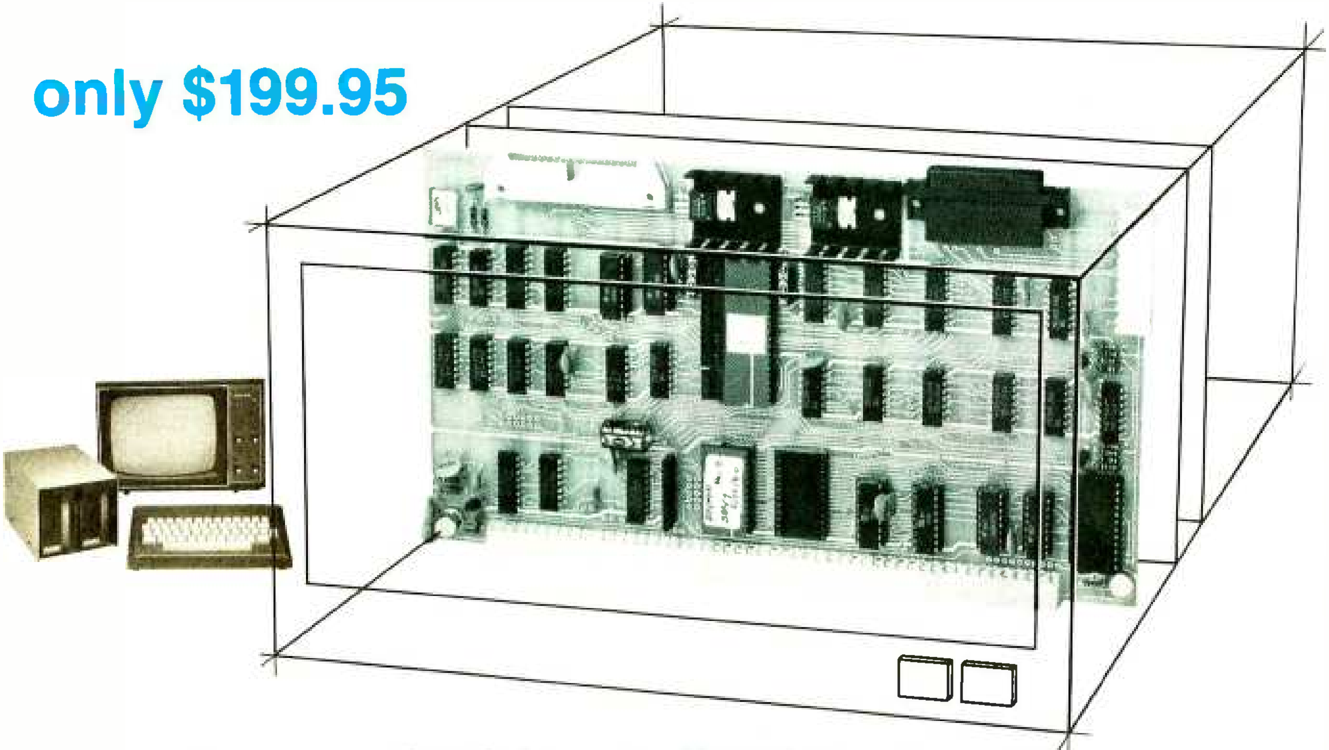

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horizon. I used a second camera with a wide-angle lens to take several hand-held pictures. Eventually the moment passed as Norm announced the coming of third contact as predicted by his computer program running in conjunction with a Mountain Hardware real-time clock. Perhaps a bit too late, I gave my second manual cue to my program, and I prepared to apply the lens cap to protect the camera and optics.

The rest of the trip was, of course, anticlimactic. I had the satisfaction of having had my program work as planned, the good fortune of avoiding a repeat of the thermal problems of the day before the eclipse, and the knowledge that a significant improvement in eclipse viewing can be achieved using a computer system. We returned home the next Thursday, and by Friday noon I was able to view the images photographed by my system during those 4 minutes in Tsavo the Saturday before. I don't know when I will next see a solar eclipse, but I am sure that whatever the state of the art of microcomputers at the time, I will be using one to improve my automation of photography of the 1980 eclipse.

Listing 1 continued:

```
            UNTIL
               (total_eclipse > 0)
                                 AND
               (total_eclipse < maximum);
            s := 'Enter totality duration (sec)';
            set_parameter(time_totality);
            s := 'Enter slack time (sec)';
            set_parameter(slack_in_totality)
         END;
      crash_ahead := TRUE
   END {initialize};

PROCEDURE await_cue;
   VAR
      anychar : PACKED ARRAY[0..0] OF CHAR;
   BEGIN {await_cue}
      WRITELN('');
      WRITELN('');
      WRITELN('');
      WRITELN('*********************');
      WRITELN('Awaiting manual cue');
      WRITELN('*********************');
      UNITREAD(2,anychar,1,0,0)
   END {await_cue};

PROCEDURE diamond_ring_burst;
   VAR
      i : INTEGER;
   BEGIN {diamond_ring_burst}
      FOR i := 1 TO ring_frames DO
         BEGIN
            IF which_ring = second THEN
               take_picture(transient_shots[0])
            ELSE
               take_picture(transient_shots[1])
         END;
      milli(post_ring_delay)
   END {diamond_ring_burst};

PROCEDURE totality;
   VAR
      exposure_count : INTEGER;
      cyclic_choice  : INTEGER;
   BEGIN {totality}
      WRITELN('Begin totality sequence');
      cyclic_choice := 0;
      FOR exposure_count := 1 TO total_eclipse DO
         BEGIN
            take_picture(twenty_five_shots[cyclic_choice]);
            cyclic_choice := (cyclic_choice + 1) MOD 25
         END;
      WRITELN('End totality sequence')
   END {totality};

PROCEDURE summarize;
   BEGIN {summarize}
      WRITELN('Press return to end program');
      READLN(s)
   END {summarize};


PROCEDURE perform_eclipse_dance;
   BEGIN
      await_cue;
      diamond_ring_burst;
      totality;
      ref_memory(open_shutter_address); {sneak in one more exposure}
      await_cue;
      ref_memory(close_shutter_address);
      milli(overhead_duration);
      diamond_ring_burst
   END;


BEGIN {eclipse_monitor_simulation}
   an_integer := 100;
   WHILE an_integer > 0 DO
      BEGIN
         initialize;
         IF an_integer > 0 THEN
            BEGIN
               normalize_timing;
               WRITELN('Is this an eclipse run? (Y = yes)');
               READLN(s);
               IF LENGTH(s) < 1 THEN s := ' ';
               IF ((s[1] = 'y') OR (s[1] = 'Y')) THEN
                  perform_eclipse_dance
            END
      END;
   summarize
END. {eclipse_monitor_simulation}
```

Articles Policy

BYTE is continually seeking quality manuscripts written by individuals who are applying personal computer systems, designing such systems, or who have knowledge which will prove useful to our readers. For a more formal description of procedures and requirements, potential authors should send a large (9 by 12 inch, 30.5 by 22.8 cm), self-addressed envelope, with 28 cents US postage affixed, to BYTE Author's Guide, 70 Main St, Peterborough NH 03458.

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Critique of Technique

This use of computer automation in photographing a solar eclipse provided a valuable improvement over manual methods. Computer automation allowed me to plan an exposure sequence which would be executed without relatively error-prone manual operations. This goal was achieved in the experiment described here. But by building on experience, one can always improve the techniques.

A relatively simple improvement would be to devote some automation to the partial phases of the eclipse. This would be accomplished by adding a loop to take photographs, for example, every five minutes, listening for the manual cue of imminent totality between partial phase shots. This would also assume cool enough temperatures for reliable operation over a 90-minute time span. I left this feature out because I had no idea of the proper exposure time to use and was too busy getting the main goal accomplished.

The problem of determining the mechanical overhead of the Nikon Motor Drive in the "bulb" position needs further attention. The shortest exposures in the 1980 eclipse were dictated by a fixed overhead time needed to ensure reliable triggering of the motor drive. If this time is too long, given the film used, then two options remain: using a slower film, or applying a filter to the lens during totality. The diamond-ring exposure times were much too long for a good photographic result. This problem would go away if a slower film or filters were applied. Since an equatorial telescope mount was tracking the sun during the eclipse, use of slower film would give a shorter effective minimum exposure time without sacrificing resolution with the long shots.

Two problems with my procedures during the 1980 eclipse will not go away given improvements in computer systems techniques. The first problem is that of inadequate timing cues. While it would be possible to use a real-time clock to coordinate with universal time, such an open-loop operation would not necessarily guarantee better timing of the start of the sequences of totality photographs due to imprecision in our knowledge of latitude and longitude at a remote site.

The second difficult problem is forgetting to verify focusing of the camera during the automatic sequence. In this eclipse, I was lucky, because I did not jar the camera while removing the filter. But, quite frankly, I forgot to even look through the viewfinder while the automatic programming sequence was in operation. Had I twisted the barrel of the lens while removing the filter I could have had a real disaster of unfocused results.

And of course, the next time I go to the tropics with a computer, a sun shade of some sort will accompany me.

High-Level Conference

A key part of the success of this application of a personal computer to eclipse photography was the use of a high-level language system for nearly all of the programming. Listing 1 shows the final version of the eclipse camera-control program with an additional month's development from the state shown in listing 1 of the March 1980 editorial. This very successful use of Pascal in a relatively sophisticated engineering application helps emphasize the importance of the high-level-language design approach.

The importance of high-level languages in design extends far beyond any particular application. To help provide our professionally oriented readers with an intensive exposure to the design philosophy of modern software tools for small computers, we have created a seminar on the subject. The seminar is organized in conjunction with the McGraw-Hill Conferences and Seminars group. It will be held at the McGraw-Hill building in New York City, June 16 and 17, 1980. The sessions of "The BYTE Conference on Languages and Tools for Microcomputing" will include six important talks on several essential high-level-language systems concepts for small computers.

Dr Fred Martin of Intermetrics Incorporated will talk about the high-level language-oriented software tools developed for the real-time systems programming of the NASA Space Shuttle flight computers. Dr Peter Grogono, author of Programming in Pascal, *will present the philosophy of Pascal, the predominant block-structured, strongly typed language of contemporary microcomputer usage. Dr Ken Bowles, the driving force behind UCSD Pascal, will provide a fascinating talk entitled "After Pascal, What?" which concerns proposed microcomputer implementations of the US Defense Department's Ada language. John Morse of Digital Equipment Corporation will set Bell Laboratories' C language into a microcomputer context, describing its value as a systems and applications program implementation language. Dr Charles Moore of Forth Incorporated will describe the characteristics of Forth as a programming tool appropriate for small computers. Dr Henry Baker of the University of Rochester will complete this suite of language-oriented tools for microcomputers by presenting information on LISP and its applications. This 2-day intensive conference will end with a panel session in which all the speakers will participate.*

For further information, contact The McGraw-Hill Conference and Exposition Center, 1221 Avenue of the Americas, Rm 3677, New York NY 10020, or see the advertisement in this issue. ■

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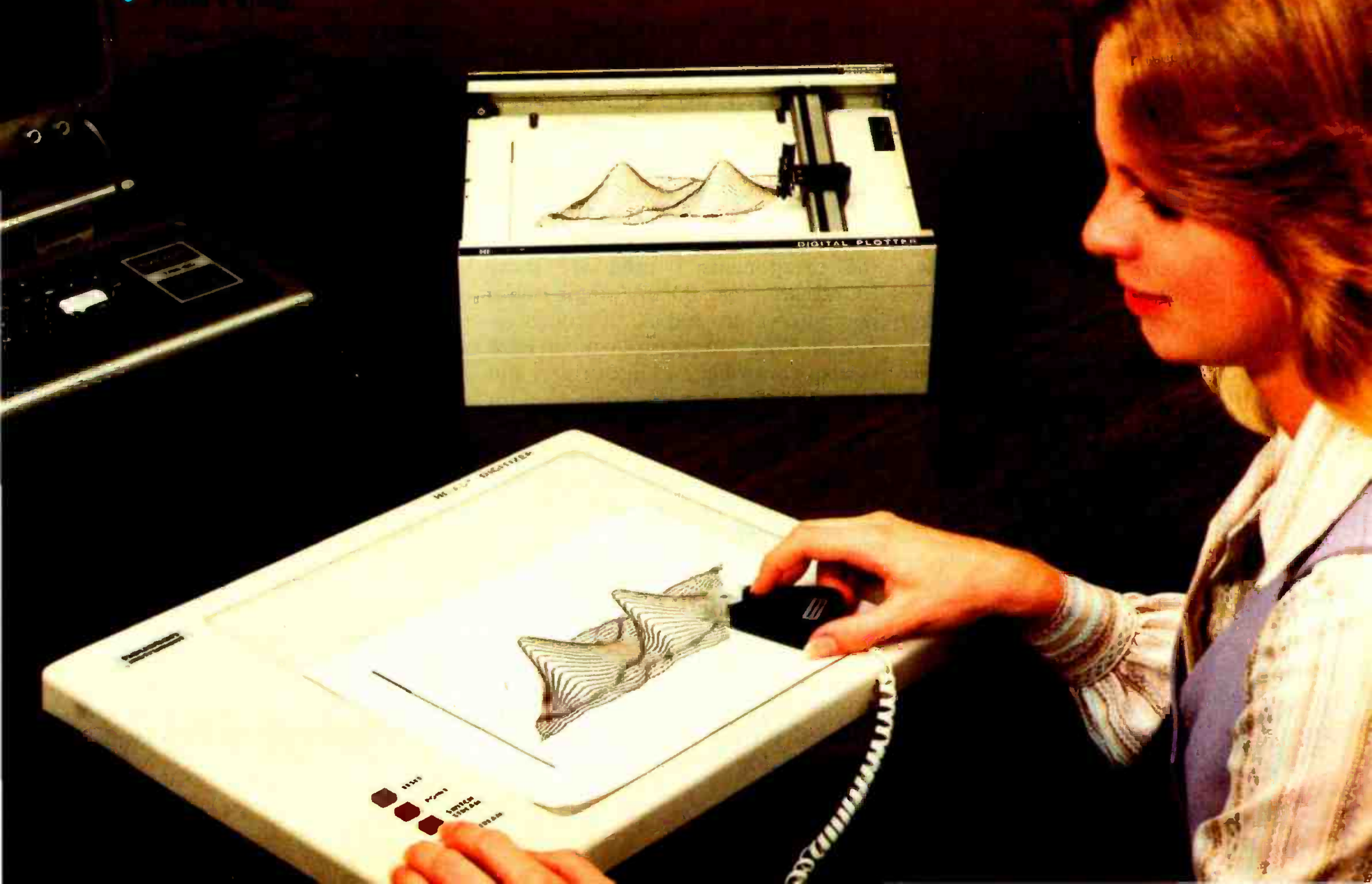

Interface a Floppy-Disk Drive to an 8080A-Based Computer

John Hoeppner
Shugart Associates
415 Oakmead Pky
Sunnyvale CA 94086

The audio cassette has been used by most of us for off-line storage of programs and data. It has two advantages: it is inexpensive, and it is easy to implement because of the wide variety of cassette interfaces available.

However, I grew tired of waiting for the BASIC interpreter and all my data to be loaded every time I powered up my system. Even then, I sometimes had to load and reload the data until the interpreter and my programs were transferred correctly. I decided to try an alternative.

On one hand, the Shugart minifloppy 5-inch disk drive, which costs about $350, was a little more expensive than my cassette recorder; but, on the other hand, the 5-inch floppy disk it uses costs about the same as a quality cassette tape — around $4. And, despite a higher initial investment, the floppy disk is more reliable, and it can transfer programs and data as much as thirty times faster than the audio cassette. It seemed the more programs that were developed, the more worthwhile the additional investment would be. Also, with a recently introduced integrated circuit from Western Digital, the FD1771 floppy-disk formatter/controller, I could design a controller myself that could be interfaced to my 8080A-based microcomputer system.

Minifloppy is a registered trademark of Shugart Associates used to describe their 5-inch floppy-disk drives.

This article describes the hardware developed to connect a Shugart floppy-disk drive to an 8080A-based system using the Western Digital FD1771 chip, as well as the software routine necessary to drive the FD1771.

The FD1771 disk formatter/controller device is compatible with the IBM 3740 format.

Hardware Characteristics

The 8080A-based microcomputer was one that I designed. However, the components I used are those found on most 8080A single-board computers: an 8080A microprocessor, an 8224 two-phase clock, an 8228 system controller and bus driver, and an 8255 programmable peripheral interface. (See figure 1.) For temporary data storage, I used 2 K bytes of programmable memory, and for my bootstrap loader, I used a 256-byte programmable read-only memory. The microcomputer interfaces to the FD1771 through the programmable peripheral interface (PPI), which can be programmed as three input/output (I/O) ports of eight lines each.

The FD1771 disk controller is compatible with the IBM 3740-type, soft-sectored format, but it can be programmed for other formats. It contains five registers: data, command, sector, track, and status. These registers hold the data and commands transferred from the 8080A processor. The FD1771 has a cyclic redundancy check (CRC) generator for performing a validity check on data transfers. It is also equipped with an internal data separator for separating clock and data bits from the disk into two separate streams. I chose not to use the internal data separator for the following reason.

Each bit of data on the disk is stored during a time interval called a *bit cell*. The bit cell is the space between two of the clock pulses that are recorded on the disk; the beginning of the bit cell is defined by the clock pulse. If the bit is to be recorded as a 1, a pulse is written in the center of the bit cell. If the bit is to be recorded as a 0, no pulse is written in the cell.

The bit pulse must be written on the disk inside certain boundaries. When the pulse is read by the disk drive, the pulse is presented to the controller within a certain time frame called the *data window*. The length of the bit cell is 8 μs. When the clock pulse is detected by the controller, a timer is activated. This timer counts 2 μs; after 2 μs have elapsed, the data window is deemed to be "open." The data window is open during 4 μs, and the bit pulse is expected to be found during the data-window interval. After the interval of the data window in over, the controller looks for another clock pulse to begin the next bit cell.

The Honor Graduate

There's been a lot of talk lately about intelligent terminals with small systems capability. And, it's always the same. The systems which make the grade in performance usually flunk the test in price. At least that was the case until the SuperBrain graduated with the highest PPR (Price/Performance Ratio) in the history of the industry.

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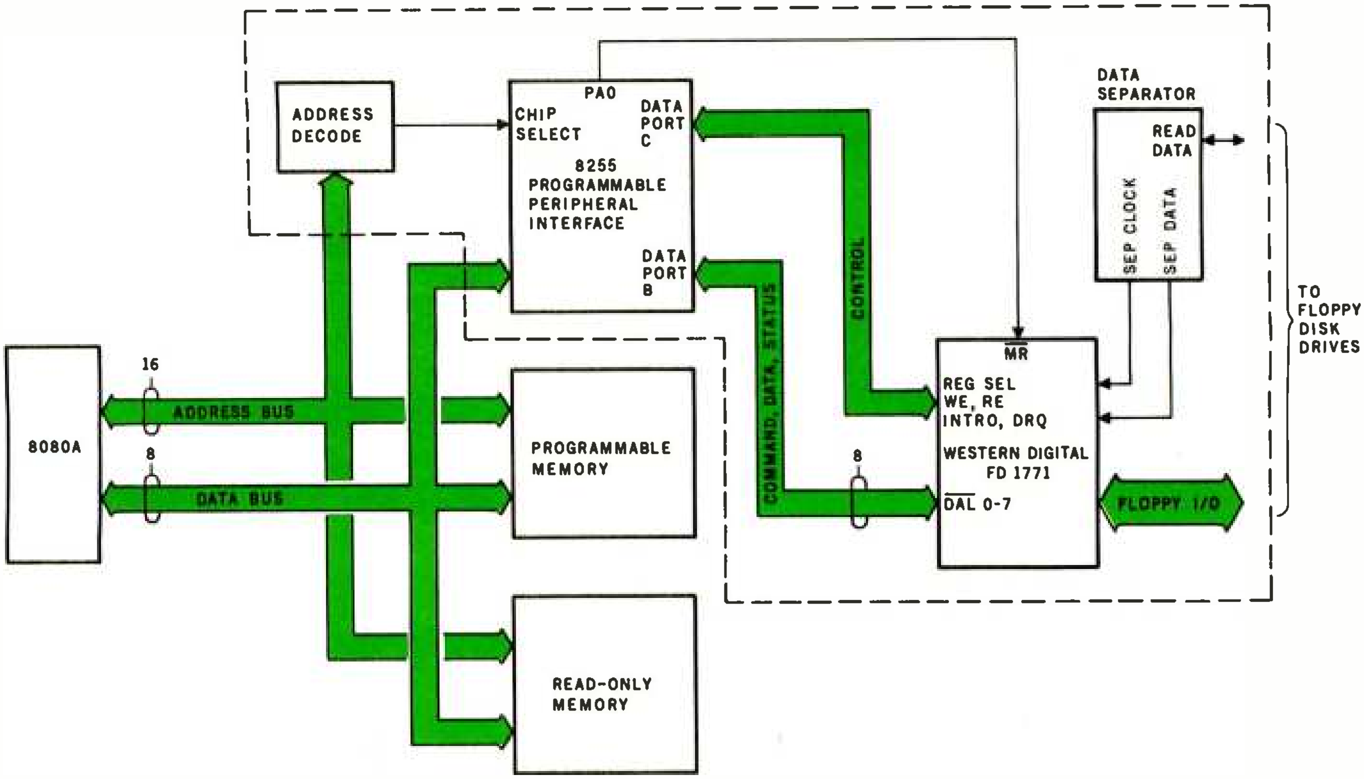

Figure 1: *Block diagram of 8080A-based computer and interface to Shugart SA400 floppy-disk drive. The Western Digital FD1771 disk-controller circuit is illustrated here as the area within the dotted lines.*

The problem with the FD1771 internal data separator arises from the counting after the clock pulse to find the beginning of the data window. The counter in the FD1771 is synchronous with the system clock pulses (at 1 MHz) that are fed into the FD1771. However, the pulses from the disk arrive at the controller *asynchronously*; the variation in the arrival intervals of the pulses is caused by a host of factors. Therefore, the data window as determined by the FD1771 can occupy varying positions within the bit cell. The position may vary by as much as 1 μs (ie: 1 clock cycle) within the 8 μs bit-cell interval.

In worst-case data patterns, this problem may lead to errors and loss of data. Therefore, I provided a data separator of my own design to replace the internal data separator of the FD1771. My data separator was built using a number of discrete logic gates of the 7400 family, as presented in figure 2.

The 5-inch floppy-disk drive I used was a Shugart SA400 minifloppy drive. It is organized to store data in thirty-five independent tracks. Each track contains 3125 unformatted bytes for a total unformatted capacity of 109.4 K bytes per disk. The formatting method I used results in an actual capacity of 71.68 K bytes per disk. The track-to-track access time of the data-transfer (ie: read/write) head is 40 ms. Once the read/write head is positioned above the correct track, another 10 ms of settling time must be allowed before a read or write operation can be performed. The basic data-transfer rate of the drive is 125 K bits per second, which translates to 15.6 K bytes per second. This compares to the audio cassette recorder's transfer rate of about 500 bytes per second.

Connecting the 8255 PPI

The 8255 programmable peripheral interface provides a universal means of interfacing peripheral devices to the 8080 microprocessor. It interfaces to the data bus through the 8228 system controller and bus driver. Three address lines (A0, A1, and A15) of the 8080A are connected to the 8255. Line A15 is connected to the chip select ($\overline{CS}$) line of the 8255, giving the PPI a memory address of hexadecimal 8000. Lines A0 and A1 directly access registers in the 8255. This method of I/O addressing is called memory mapping, because it makes certain memory addresses act as registers for communication between the computer and the peripheral device: it was necessary because the conventional I/O instructions were too slow.

The FD1771 interfaces to the processor through eight data lines (PB0 thru PB7) and seven control lines (PA1, PC0, PC1, PC2, PC3, PC6, and PC7), as shown in figure 2 (page 78). Ports A and B of the PPI, each providing eight lines for transfer of data, interface with the data lines of the FD1771. Three lines of port A also connect directly to the disk drive. Port C of the PPI handles the FD1771 control lines. The eighth control line of the FD1771 is not used, so it is tied to ground.

Six of the outputs of the PPI (PA0 thru PA3, PC2, and PC3) are logically inverted. Because the outputs of *all* ports on the 8255 go low when *any* port is commanded to change direction (from input to output, or vice versa), this inversion is necessary to prevent false signals from going to the FD1771, deselecting the drive and turning off the motor.

Due to total system-timing constraints, disk read and write routines must be performed within 56 μs.

Text continued on page 80

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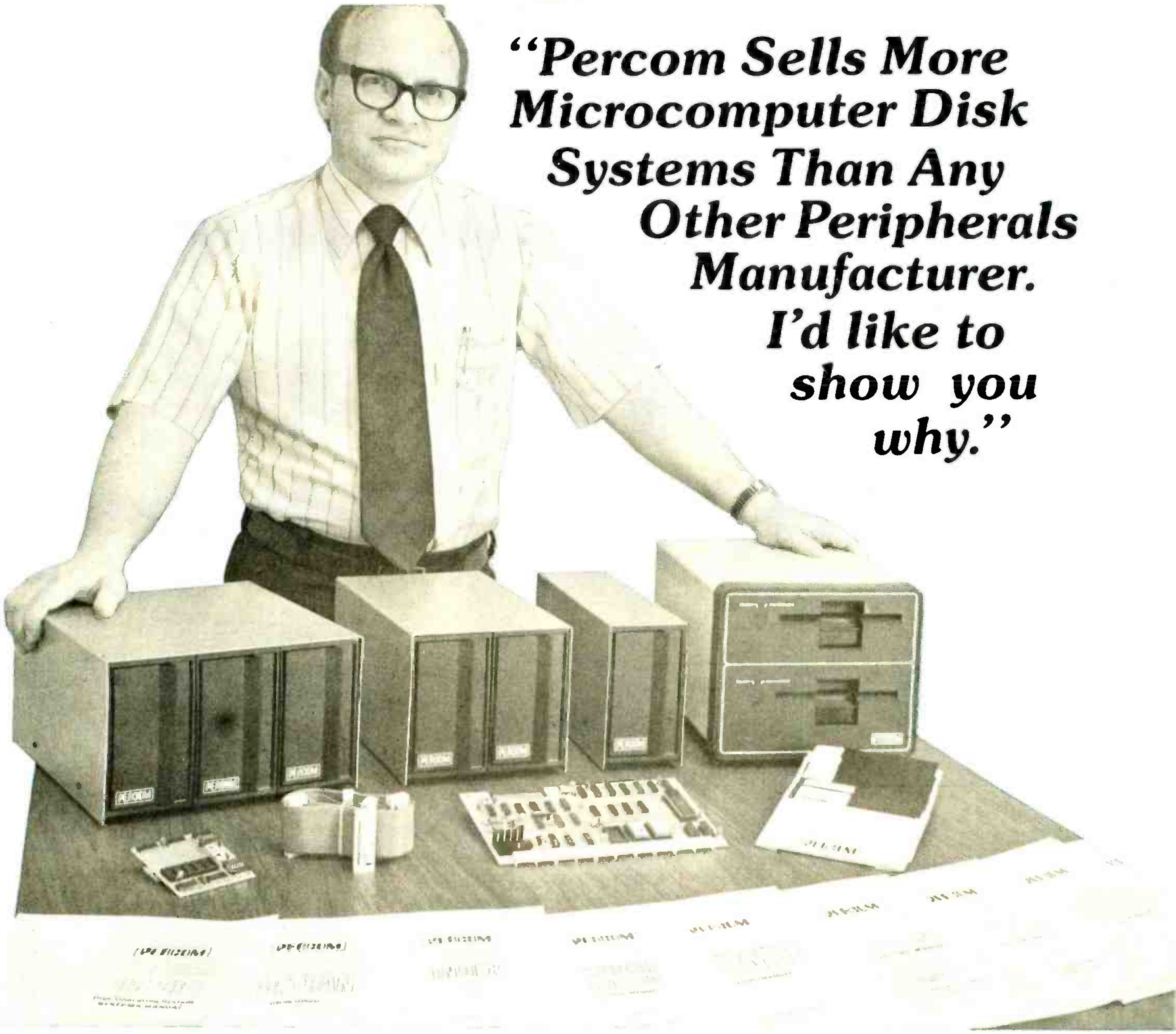

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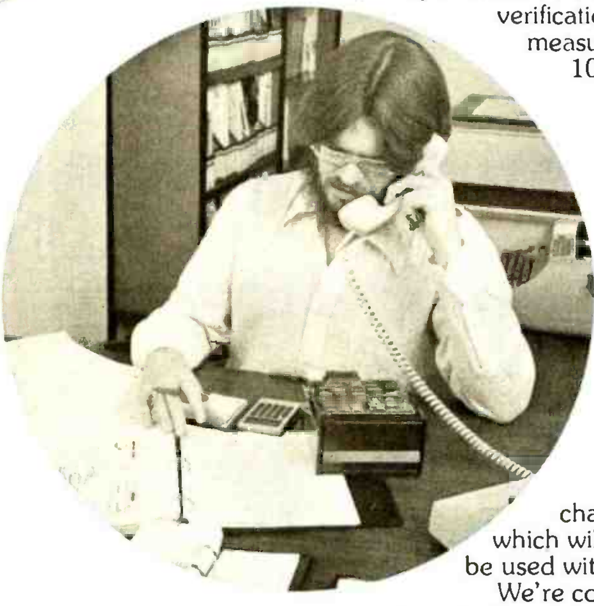

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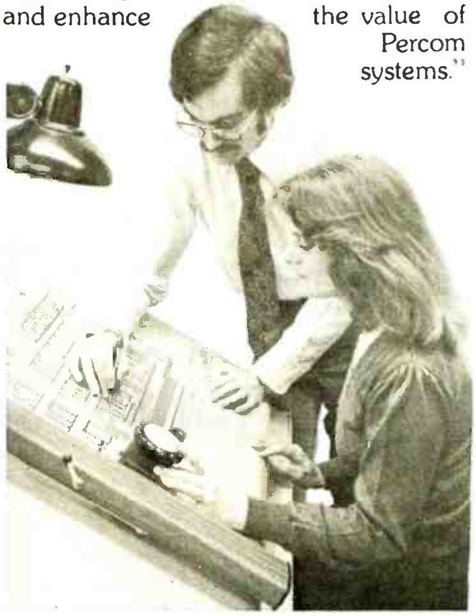

"Slipping a circuit board through the eye of a needle would be easier than slipping a cold solder joint past Beverly. These are four-drive LFD-400/800 disk system controllers she's inspecting."

Number	Type	+5 V	GND	−5 V	+12 V
IC1	8080A	20	2	11	28
IC2	8228	28	14		
IC3	8255	26	7		
IC4	FD1771	21	20	1	40
IC5	8224	16	8		9
IC6	7404	14	7		
IC7	7404	14	7		
IC8	9602	16	8		
IC9	9602	16	8		
IC10	7414	14	7		
IC11	7414	14	7		
IC12	7438	14	7		
IC13	7438	14	7		
IC14	7474	14	7		
IC15	7474	14	7		
IC16	9602	16	8		
IC17	7400	14	7		
IC18	7400	14	7		
IC19	7404	14	7		

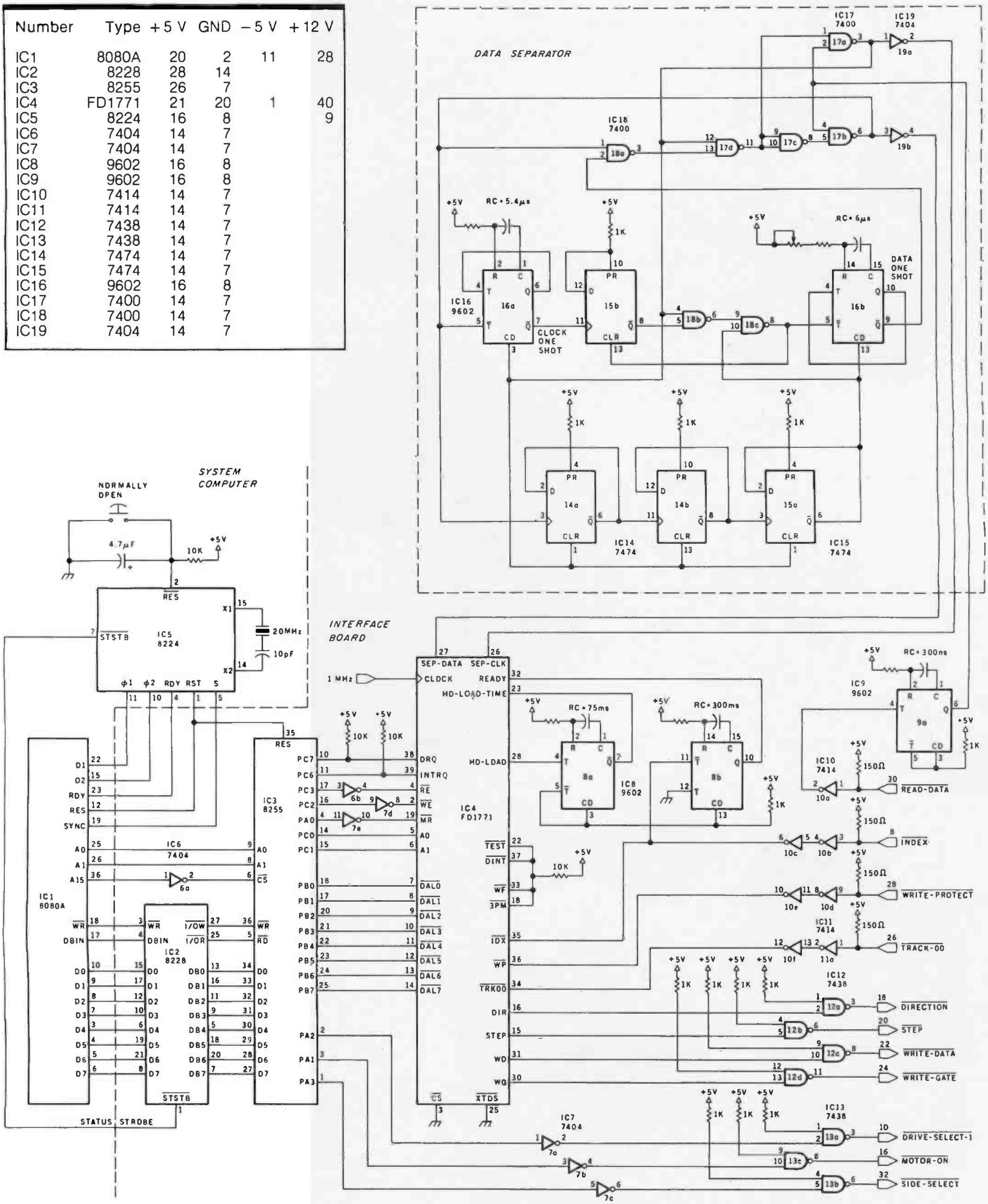

Figure 2: *Disk-controller board. The circuit to the left of the dotted line is part of the computer being interfaced; the part to the right is the interface to the floppy-disk drive. The area in the dotted box is a data separator made from 7400-series TTL devices. It separates the clock bits from the data bits as they come from the disk drive.*

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Text continued from page 74:
Therefore, it was necessary during the design process to shorten the time for checking the status of the drive. To allow fast status checking, bit 7, the most significant bit, of port C is tied to the FD1771's data-request line (DRQ). The value of the DRQ is brought into the accumulator by performing a memory-access instruction. It is then possible to perform an inclusive-OR of the accumulator with itself (ORA A), which results in the sign bit being set to 1 if there is a data request (ie: if DRQ is high). Based on the status of the sign bit, control can branch to the appropriate routine. This arrangement eliminates the need to perform a separate check on the status bits using one of the logical instructions, thereby saving a significant amount of time.

Interfacing to the SA400

The SA400 drive has connections for twelve transistor-transistor logic (TTL) compatible signal lines. Seven of them connect directly to the FD1771 lines through type-7414 Schmitt-trigger inverters used as line drivers and 7438 open-collector NAND buffers used as line receivers.

The WRITE-DATA line transmits digitized serial data to be written on the floppy disk. The WRITE-GATE signal, when activated, causes the data to be written on the disk. The WRITE-PROTECT line, when active in a low state, indicates that a write-protected disk has been inserted in the drive. The STEP line, when pulsed, causes the read/write head to move radially a distance of one track. The DIRECTION-SELECT line defines the direction that the read/write head moves when the STEP line is pulsed. The TRACK-00 line, when low, indicates when the read/write head is positioned over the outermost track, track 0. The INDEX line transmits the pulse that occurs once for every revolution of the floppy disk to indicate the beginning of a track. (The pulse comes when the index hole passes the photodetector.)

Three drive-select lines, which assign the logical drive address, are connected to port A of the 8255 through 7414 and 7438 circuits used as line drivers and receivers. A MOTOR-ON line, also tied to the 8255, controls the spindle-drive motor. The READ-DATA line is tied to the monostable multivibrator (commonly known as a one-shot) that shortens the pulse width from the drive to 300 ns before sending it to the data separator.

The FD1771 has nine other control lines, which control head positioning and data transfers, but which do not interface directly to the disk drive. Four of the lines to the FD1771 are not used. Lines TEST, DINT, WF and 3PM are therefore tied to +5 V through a 10 k-ohm resistor.

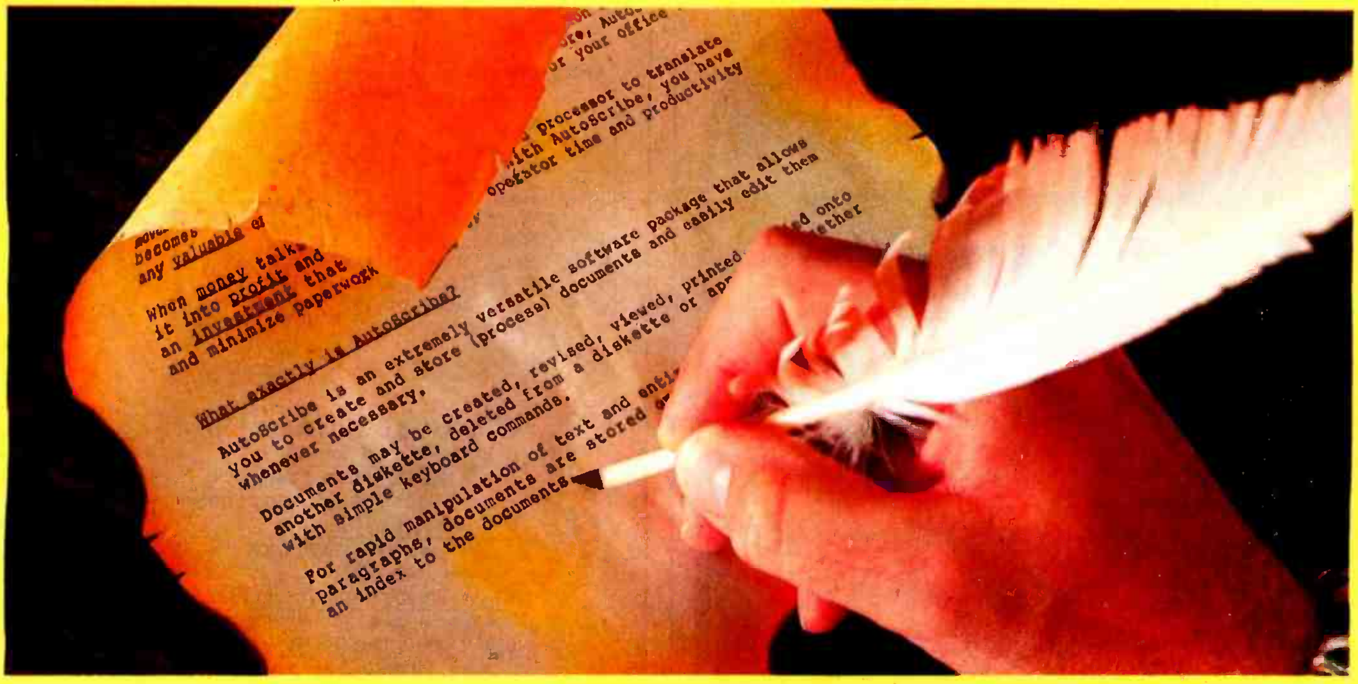
Of the remaining five control lines for the FD1771, the SEPARATED-CLOCK and SEPARATED-DATA lines transmit the clock and data bits from the data separator. (Clock pulses are used in frequency modulated (FM) encoding to signal the beginning of a bit cell.)

The READY line, which signals that the drive is ready for a read or write operation, must be active for the FD1771 to perform any function.

Text continued on page 84

A1	A0	Register Affected During Read ($\overline{RE}$ = 0, $\overline{WE}$ = 1)	Register Affected During Write ($\overline{RE}$ = 1, $\overline{WE}$ = 0)
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

Table 1: *Access to registers within the Western Digital FD1771 disk formatter/controller device. The FD1771 has five internal registers: command, data, sector, status, and track. A given register is read or written by placing the appropriate values on lines A1 and A0 and pulling down either the READ-ENABLE ($\overline{RE}$) line for a read operation, or the WRITE-ENABLE ($\overline{WE}$) line for a write operation. The sector and track registers specify the sector and track when these parameters are needed by a given command byte. The command register, when filled, causes one of eleven high-level instructions to be executed (see table 2). Data passes between the computer and the disk drive through the data register. After a command has been executed by the FD1771, the status register must be read before another command can be executed.*



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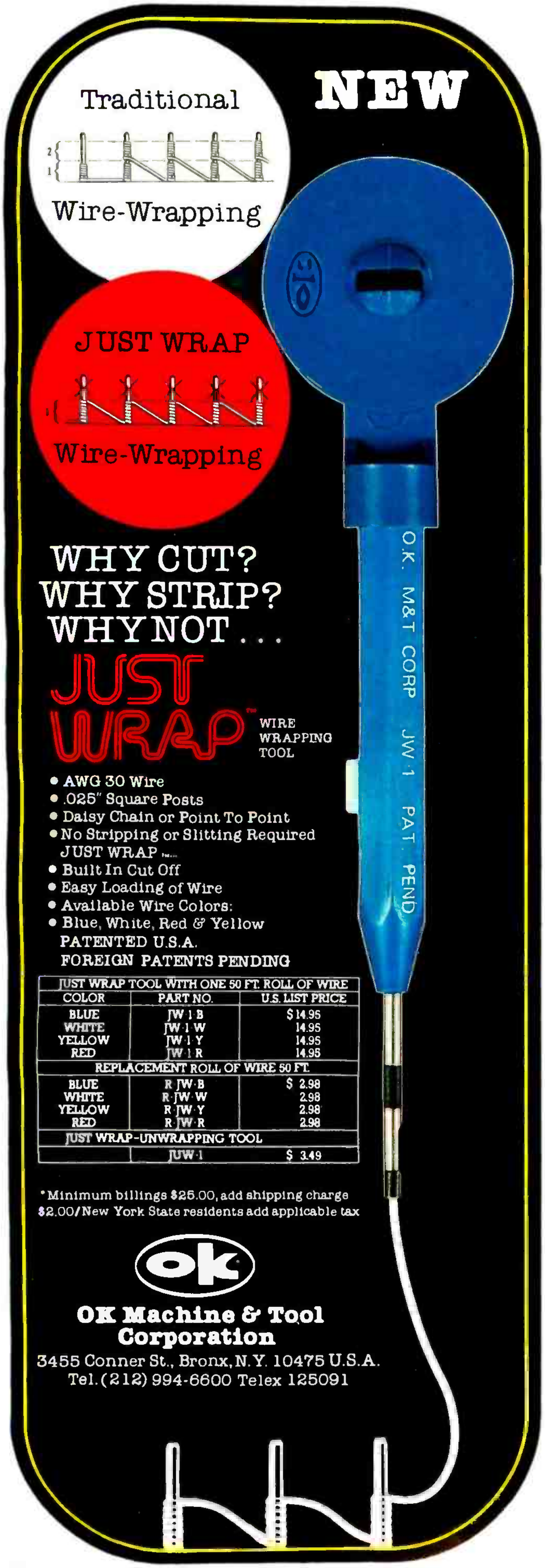

TYPE	COMMAND	BITS 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Command	1	0	0	m	b	E	0	0
II	Write Command	1	0	1	m	b	E	a_1	a_0
III	Read Address	1	1	0	0	0	1	0	0
III	Read Track	1	1	1	0	0	1	0	$\bar{s}$
III	Write Track	1	1	1	1	0	1	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

(a)

BIT VALUES FOR TYPE I

h = Head Load flag (Bit 3)
- h = 1, Load head at beginning
- h = 0, Do not load head at beginning

V = Verify flag (Bit 2)
- V = 1, Verify on last track
- V = 0, No verify

r_1r_0 = Stepping motor rate (Bits 1 thru 0)
- r_1r_0 = 11 gives 40 ms step time

u = Update flag (Bit 4)
- u = 1, Update Track register
- u = 0, No update

(b)

BIT VALUES FOR TYPE II

m = Multiple Record flag (Bit 4)
- m = 0, Single record
- m = 1, Multiple records

b = Block length flag (Bit 3)
- b = 1, IBM format (128 to 1024 bytes)
- b = 0, Non-IBM format (16 to 4096 bytes)

a_1a_0 = Data Address Mark (Bits 1 thru 0)
- a_1a_0 = 00, FB (Data Mark)
- a_1a_0 = 01, FA (User defined)
- a_1a_0 = 10, F9 (User defined)
- a_1a_0 = 11, F8 (Deleted Data Mark)

(c)

BIT VALUES FOR TYPE III

$\bar{s}$ = Synchronize flag (Bit 0)
- $\bar{s}$ = 0, Synchronize to Address Mark
- $\bar{s}$ = 1, Do not synchronize to Address Mark

(d)

BIT VALUES FOR TYPE IV

I_0 thru I_3 = Interrupt Condition flags (Bits 3 thru 0)
- I_0 = 1, Not Ready to Ready transition
- I_1 = 1, Ready to Not Ready transition
- I_2 = 1, Index pulse
- I_3 = 1, Immediate interrupt

E = Enable HLD and 10 ms Delay
- E = 1, Enable HLD, HLT and 10 ms delay
- E = 0, Head is assumed engaged and there is no 10 ms delay.

(e)

Table 2: *The high-level instructions of the FD 1771 disk formatter/controller device. When one of the instructions as defined by table 2a is loaded into the command register of the FD1771, the FD1771 executes one or a series of actions. Bits represented by a letter within a command are defined in the bit value tables for that type instruction, tables 2b thru 2e.*

Text continued from page 80:

Since the Shugart SA400 floppy-disk drive has no "ready" signal, the drive's index signal is used to determine a ready condition.

The disk drive transmits the index pulse only when the drive door is closed, the disk is inserted, and the spindle motor is turning. Because the index pulse is transmitted once for each rotation of the disk, the speed of rotation may be determined by measuring the interval between pulses. When the drive spindle has reached final speed, the index pulse is transmitted at intervals of 200 ms.

I used the index pulse to trigger a monostable multivibrator, which generates a one-shot pulse with a length slightly greater than 200 ms. When the drive is up to speed, the one-shot is continuously activated, since the index pulse retriggers it at 200 ms intervals. This one-shot pulse is connected to the ready line on the FD1771, and the derived "ready" signal remains true as long as the drive is ready.

The HEAD-LOAD and HEAD-LOAD-TIME lines are related in function. When the FD1771 issues a command to the drive, the drive may have to first load the head. The head-load time for a Shugart SA400 drive is 75 ms. Since the FD1771 is designed for use with drives having a shorter head-load time, a time-out signal to indicate that the head is loaded must be generated externally. To insure that the head is loaded, the HEAD-LOAD signal from the FD1771 is tied to a monostable multivibrator having a pulse duration of 75 ms. The output is fed back to the FD1771 as its HEAD-LOAD-TIME input to force the FD1771 to wait for 75 ms before sending a read or write command to the drive.

The FD1771 controls the floppy-disk drive with one of several 8-bit command words; these command words are high-level in the sense that each initiates a series of operations that define the function requested. Generally, each command requires some type of parameter. So, before the 8080A microprocessor sends a command, it must first load the necessary parameter in the form of an 8-bit byte into the appropriate register of the FD1771, whether the destination is the data, sector, or track register.

To place the necessary data in a register, address lines A0 and A1 are set according to the data in table 1, the READ-ENABLE (RE) line is held high and the WRITE-ENABLE (WE) line is pulled low. To implement a command, lines A0 and A1 must address the command register. An 8-bit byte representing the appropriate command is placed on the data lines of the FD1771 (via the B port of the 8255) and is sent to the command register as the WRITE-ENABLE line is toggled from high to low.

FD1771 Commands

The FD1771 recognizes eleven high-level commands; these are illustrated in table 2 with their binary representations. They can be divided into four types. Type I commands are used to move the drive's read/write head. Type II commands are read- and write-sector commands. Type III commands are read-address, read-track and write-track or formatting free freight!

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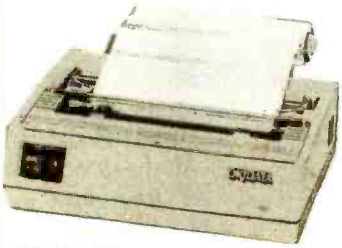

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The *restore* command causes the addressed drive to move the head to (or *seek*) track 0. When the *seek* command is executed, the addressed disk drive positions the read/write head over the track specified by the 8080A. The *step* command causes the drive to step the head one track in the direction previously selected. The *step-in* command causes the head to step one track toward track 35, the innermost track. With the *step-out* command, the head steps one track toward track 0.

A *read* command transfers a full sector of data, 1 byte at a time, from the disk to the 8080A. A *write* command transfers data for one sector from the microprocessor to the drive. A *read-track* command transfers all bytes of data on a track to the microprocessor. A *read-address* command transfers the next-encountered identification (ID) field to the microprocessor, places the sector address into the sector register, and checks the 2-byte cyclic-redundancy-check (CRC) field. During a *write-track* (format) command, the microprocessor must supply all gap, ID-field, and data bytes except for address marks and CRC bytes.

Data transfers between the 8080A and the floppy-disk drive can be performed using either direct memory access (DMA) or programmed I/O, both of which are supported by the FD1771. I chose programmed I/O, because it is the simpler method of the two, and because it is fast enough for single-density disk drives. With single-density recording, 1 byte is transferred every 64 μs. An average 8080A instruction takes 5 to 6 μs to execute, so that about ten instructions can be executed during the transfer time. This is enough time to gather the data and perform the required housekeeping functions.

Initializing the FD1771

Before the FD1771 can execute commands, it must be initialized. The program shown in listing 1 sets up the control ports of the 8255 PPI so that port A controls certain aspects of disk selection (as well as the MASTER-RESET (MR) pin of the FD1771); port B transmits the command, data, and status words for communication between the 8255 and the FD1771; and port C controls data exchanges between the two devices. All commands and parameters come from the computer to the FD1771 through port B of the 8255. All data and status information from the disk to the computer uses the same path.

Data transfers can be performed with either direct memory access (DMA) or programmed input/output.

The initialization routine of listing 1 also checks the status of the FD1771 and initializes all the registers. The stack pointer is set to memory location hexadecimal 0BEF. For large applications, code for a disk-file library could be established in this routine as well.

Formatting the Disk

Formatting the disk is a matter of loading the track-address register with the point at which formatting is to begin, issuing the seek command which moves the head to that location, loading the data register with the format values, and issuing the write-track command to place that format on the disk.

Assuming that the formatting is to begin at track 0 on the disk, for example, a seek routine (such as the one given in listing 2) is executed. First, the seek routine places the track address (which is 0) on port B of the 8255. Then, holding line A0 high and A1 low (see table 1), the routine causes a write operation to the FD1771 to take place by holding the READ-ENABLE line (RE) high and pulling the WRITE-ENABLE line (WE) low. (See line 2 of table 1.) Similarly, the command code for a seek operation (hexadecimal 10) is placed on port B of the 8255 and is deposited into the command register of the FD1771 by holding both A0 and A1 low and causing a write operation to take place. When the FD1771 receives the command byte, it executes the seek command, ending with the read/write head in position over the appropriate track (here, track 0).

At the end of the operation, the FD1771 automatically raises the logic state on the interrupt line. At the same time, a byte of status information that indicates whether the command operation was successful is made available to the 8080A. Although the byte of status information does not *have* to be interpreted, the status register *must* be read before another operation can be performed. This is the purpose of the code marked "status handshake" in listing 2.

To format each track, the write-track command must be issued. This is done by placing the command byte for the write-track command (hexadecimal F4) on port B of the 8255, setting lines A0 and A1 low, and strobing the write-enable line with a high-to-low transition. Once this command is received, the FD1771 waits for an index pulse from the disk. The data register must then be filled with the contents of the entire track, 1 byte at a time. At the end of the track the disk drive sends the next index pulse, which causes an interrupt. To write the next track, a seek-to-track-1 operation is performed and another write-track command is issued.

Floppy Disk Format

Although the FD1771 permits non-IBM data-storage formats, I chose to use a modified version of the standard IBM format illustrated in figure 3. This is a 16-sector-per-track, 128-byte-per-sector format. In other words, each of the thirty-five tracks of the floppy disk contains sixteen records (see figure 3).

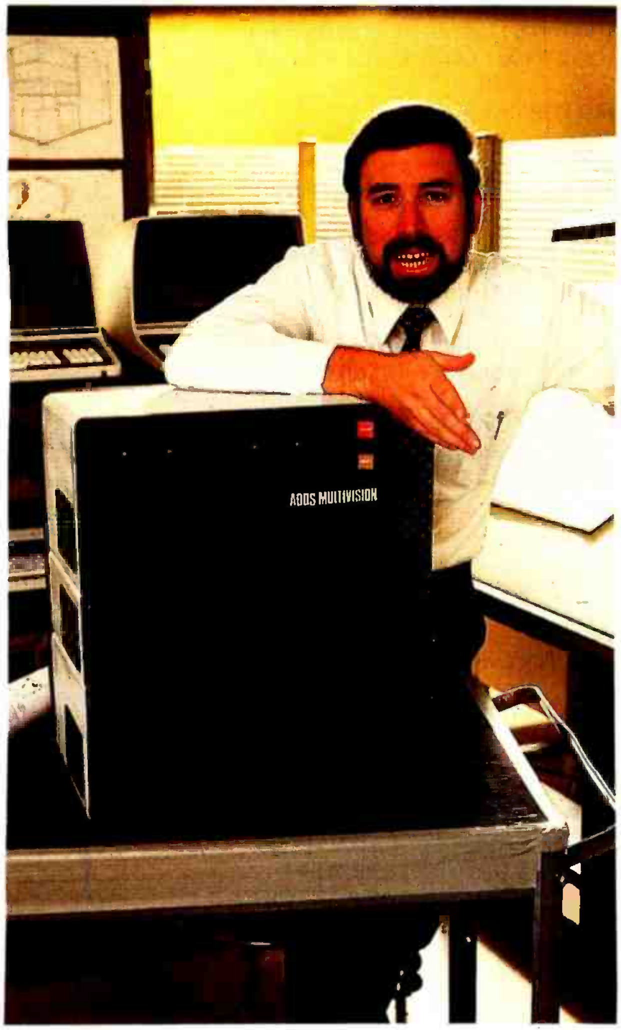
Each track starts with a gap, called G1, of 16 bytes, each containing the value hexadecimal FF. Next come sixteen records, each of which contains an identification (ID) field, a second gap (G2), a data field of 128 bytes, and an inter-record gap, G3, of 26 bytes. The track is finished with approximately 101 bytes of a final G4A gap field.

A 6-byte synchronization, or sync, section begins the identification field and is included to insure that the data separator is in phase with the data. The single-byte address mark (abbreviated as AM) field contains a unique character that defines the beginning of the ID2 section; here, it has a value of hexadecimal FE. The ID2 section

Text continued on page 100

"INTRODUCING THE HOTTEST THING OFF THE DRAWING BOARDS: A COMPUTER TRIO THAT TAKES YOU FROM SMALL TO BIG."

Geof Karlin
Director of Systems Development



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Listing 1: *Program header and initialization routines. This routine initializes the 8255 programmable peripheral interface and sets the read/write head in the floppy-disk drive to track 0.*

```
Hexadecimal   Hexadecimal   Label      Instruction      Commentary
Address       Code                     Mnemonic
                                       and Operand
                            ; INIT
                            ;
                            ;THIS PROGRAM IS DESIGNED TO PERFORM SEEKS.
                            ;READS. WRITES AND FORMATS USING THE
                            ;WESTERN DIGITAL FD1771 FLOPPY CONTROLLER
                            ;CHIP INTERFACED TO AN SA400 AND A 8080 MPU
                            CTRL     EQU      91H
0091                        ;CONTROL WORD FORMAT:
                            ;MODE=0
                            ;PORTA=DATA PORT (INPUTS)
                            ;PORTB=STATUS AND COMMAND LINES (OUTPUTS)
                            ;PORTC=INPUTS. 0-3
                            ;PORTC=OUTPUTS. 4-7
                            PORTA    EQU      8000H
8000                        PORTB    EQU      8001H        ;PORT A ADDRESS
8001                        PORTC    EQU      8002H        ;PORT B ADDRESS
8002                        CWR      EQU      8003H        ;PORT C ADDRESS
8003                        CHARS    EQU      520H         ;CONTROL WORD ADDRESS
0520                                                       ;COMMAND CHARACTERS
                            SEEK     EQU      7D0H          ENTERED VIA CONSOLE
07D0                        READ     EQU      0B10H        ;SEEK TRACK ROUTINE
0B10                        WRITE    EQU      0B80H        ;READ SECTOR ROUTINE
0B80                        PIN      EQU 798H              ;WRITE SECTOR ROUTINE
0798                                                       ;PORT B SET AS INPUTS
                                 ORG 600H                   ROUTINE
              0600          ;
                            ;INITIALIZE THE PPI (POWER UP)
                            ;
                            ;MR ALWAYS=1 AFTER INITIALIZATION
                            ;
                            INIT          LXI SP.0BFFH     ;SET THE STACK
0600          31FF0B                      CALL PIN         ;PORTB INPUTS
0603          CD9807                      LXI H.PORTA      ;PORTA ADRS
0606          210080                      MVI A.01H        ;MR=0,DR SEL,MOT ON       PPI
0609          3E01                        MOV M,A          ;WRITE PORTA              INITIALIZE
060B          77                          LXI D.PORTC      ;LOAD PORTC ADRS
060C          110280                      MVI A,O          ;RE,WE=1
060F          3E00                        STAX D           ;WRITE PORTC
0611          12            ;
                            ;PPI INITIALIZATION DONE
                            ;RESTORE TO TRACK 0 IS AUTOMATIC
                            ;
                            TRK0
0612          3E00                        MVI A,00H        ;MR=1
0614          77                          MOV M.A          ;WRITE PORTA
0615          3E08                        MVI A,08H        ;READ ENAB-STAT REG
0617          12                          STAX D           ;(RE=0) WRITE PORTC
0618          3A0180                      LDA PORTB        ;READ PORTB—GET
                                                            STATUS
061B          4F                          MOV C.A          ;SAVE STAT REG
061C          3E00                        MVI A,00H        ;RE=1 (MR,WE=1)
061E          12                          STAX D           ;WRITE PORTC
061F          79                          MOV A,C          ;MOV STATUS TO A
0620          E604                        ANI 4H           ;GET TRAK 0 STATUS
0622          FE04                        CPI 4H           ;TRAK 0?
0624          CA1206                      JZ TRKO          ;NO
                            ;
                            ;DRIVE NOW AT TRACK 0 — TEST READY
                            ;
0627          79                          MOV A,C          ;RESTOR STATUS IN A
0628          E680                        ANI 80H          ;GET READY STATUS
062A          FE80                        CPI 80H          ;READY?
062C          CA3506                      JZ INTERP        ;YES GO TO IDLE LOOP
062F          010000                      LXI B.OH         ;ERROR CODE
0632          CD0007                      CALL ERROR
```

Listing 2: *Seek routine. This routine causes the read/write head to go to (or seek) the track specified by a 2-digit number entered from the system console.*

```
Hexadecimal  Hexadecimal  Label    Instruction      Commentary
Address      Code                  Mnemonic
                                   and Operand

                          ;THIS ROUTINE IS DESIGNED TO SEEK THE
                          ;DRIVE TO A TRACK SPECIFIED BY THE 3RD & 4TH
                          ;CHARACTERS ENTERED BY AN OPERATOR.
             8000         PORTA    EQU 8000H        ;PORT A ADDRESS
             8001         PORTB    EQU 8001H        ;PORT B ADDRESS
             8002         PORTC    EQU 8002H        ;PORT C ADDRESS
             0793         POUT     EQU 793H         ;PORT B SET AS OUTPUTS ROUTINE
             0798         PIN      EQU 798H         ;PORT B SET AS INPUTS ROUTINE
             0769         STATUS   EQU 769H         ;ROUTINE, CONVERTS STATUS TO
                                                     ASCII PRINTABLE DATA
             0520         CHARS    EQU 0520H        ;COMMAND CHARACTERS ENTERED
                                                     VIA CONSOLE.
                          ;
             07D0                  ORG 7D0H         ;
                          ;
                          ;
                          ;FORM THE TRACK ADDRESS FROM THE 3RD & 4TH
                          ;CHARACTERS. 4TH CHARACTER MIGHT BE NEGATIVE
                          ;IF ONLY ONE CHAR WAS ENTERED.
                          ;
07D0         2A2205       SEEK     LHLD CHARS+2     ;GET BOTH CHARS
07D3         7C                    MOV A,H          ;XFR LS CHAR
07D4         B7                    ORA A            ;TERM ?
07D5         F2DC07                JP TWO           ;NO
07D8         7D                    MOV A,L          ;LOAD SINGLE CHAR
07D9         C3E207                JMP NEWTRK       ;YES
07DC         7D           TWO      MOV A,L          ;XFR MS CHAR
07DD         07                    RLC              ;SHIFT TO MS POSITION
07DE         07                    RLC
07DF         07                    RLC
07E0         07                    RLC
07E1         84                    ADD H            ;MERGE CHARS

                          ;NOW PUT NEW TRACK ADDRESS IN
                           FDC DATA REGISTER
                          ;
07E2         322008       NEWTRK   STA TRACK        ;SAVE TRACK ADDRESS  }
07E5         CD9307                CALL POUT        ;PORTB=OUTPUTS       }
07E8         210280                LXI H,PORTC      ;GET PORT C ADRS     }
07EB         0603                  MVI B,03H        ;A0,A1=1             }
07ED         70                    MOV M,B          ;WRITE PORTC         }
07EE         3A2008                LDA TRACK        ;TRAK ADRS           }
07F1         2F                    CMA              ;INVERT FOR WD BUS   }
07F2         320180                STA PORTB        ;WRITE PORTB         }
07F5         0607                  MVI B,07H        ;WRITE TO DATA REG   }  COMMAND
07F7         70                    MOV M,B          ;WRITE PORTC         }  HANDSHAKE
07F8         0600                  B,00H                                 }
07FA         70                    MOV M,B          ;WRITE PORTC         }
                          ;                                              }
                          ;INITIATE SEEK COMMAND                         }
                          ;                                              }
07FB         3E1F                  MVI A,1FH        ;SEEK 40 MS STEP     }
07FD         2F                    CMA                                   }
07FE         320180                STA PORTB        ;WRITE PORTB         }
0801         0604                  MVI B,04H        ;WRITE TO CMD REG    }
0803         70                    MOV M,B          ;WRITE PORTC         }
0804         0600                  MVI B,00H        ;RE,WE = 1           }
0806         70                    MOV M,B          ;WRITE PORTC         }
                          ;
                          ;WAIT FOR END OF SEEK —
                           THEN REPORT STATUS
                          ;
```

Listing 2 continued on page 92

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NEW! muLISP-79 LISP—the lingua franca of the artificial intelligence world—is now available in this efficient, low-cost version for microcomputers. Features include dynamic allocation of storage resources; program control structures such as an extended COND and a multiple exit LOOP; user functions defined as CALL by Value or CALL by Name; and 83 LISP functions. muLISP-79, CP/M version: $200.

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BASIC COMPILER	●	●	□	●	
FORTRAN-80 COMPILER	●	●	□	■	●
COBOL-80 COMPILER	●	●		●	
muMATH/muSIMP muLISP	●		□		
MICROSEED DBMS	●				
EDIT-80 TEXT EDITOR	●		□	■	
MACRO-80 ASSEMBLER	●	●	□	■	●

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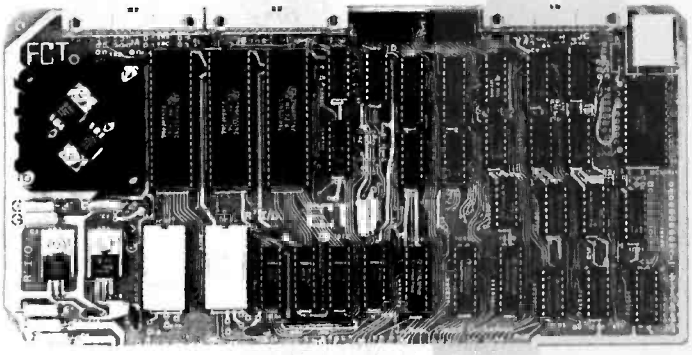
206-455-8080 Telex 328945

We set the standard.

Listing 2 continued:

```
0807    CD9807              CALL PIN
080A    7E         WAIT     MOV A,M       ;WAIT FOR END OF SEEK   }
080B    E640                ANI 40H                               }
080D    CA0A08              JZ WAIT                               }
0810    3E08                MVI A,08H     ;STAT REG READ          } STATUS
0812    77                  MOV M,A       ;WRITE PORTC            } HANDSHAKE
0813    3A0180              LDA PORTB     ;BRING STATUS           }
0816    0600                MVI B,00H     ;RE,WE=1                }
0818    70                  MOV M,B       ;WRITE PORT B
0819    2F                  CMA           ;INVERT
081A    E618                ANI 18H       ;SEEK AND CRC BITS
                   ;
081C    CD6907              CALL          ;REPORT TO CONSOLE
                            STATUS
081F    C9                  RET
                   ;
0820    00         TRACK    BYTE 0
        07D0                END SEEK
```

ECT R²I/O... The S-100 ROM, RAM & I/O Board



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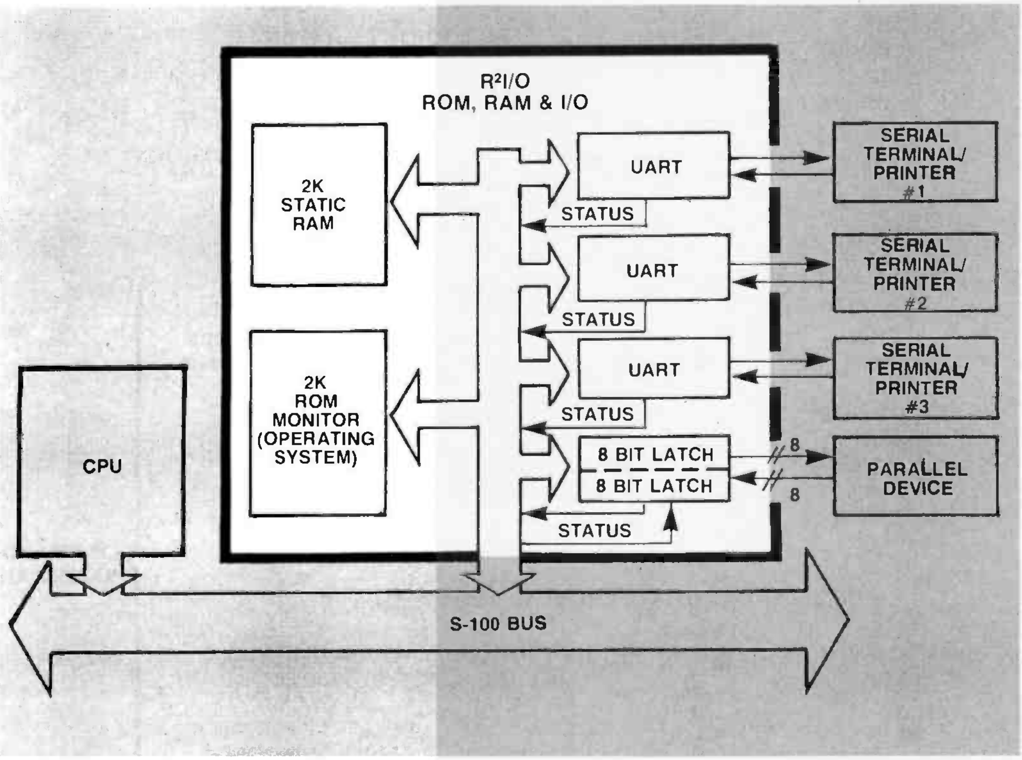

8080 APPLE MONITOR COMMANDS

A – Assign I/O
B – Branch to user routine A-Z
C – Undefined
D – Display memory on console in Hex
E – End of file tag for Hex dumps
F – Fill memory with a constant
G – GOTO an address with breakpoints
H – Hex math sum & difference
I – User defined
J – Non-destructive memory test
K – User defined
L – Load a binary format file
M – Move memory block to another address
N – Nulls leader/trailer
O – User defined
P – Put ASCII into memory
Q – Query I/O ports: QI (N)-read I/O; QO(N,V)-send I/O
R – Read a Hex file with checksum
S – Substitute/examine memory in Hex
T – Types the contents of memory in ASCII equivalent
U – Unload memory in Binary format
V – Verify memory block against another memory block
W – Write a checksummed Hex file
X – Examine/modify CPU registers
Y – 'Yes there' search for 'N' Bytes in memory
Z – 'Z END' address of last R/W memory location

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Listing 3: *Read-sector routine. This routine causes the contents of a given sector of the current track (specified by a 2-digit number entered from the system console) to be transferred from the disk drive to an area of memory starting at the location given by the value of DATBUF, using decreasing memory addresses.*

```
Hexadecimal  Hexadecimal  Label    Instruction     Commentary
Address      Code                  Mnemonic
                                   and Operand

                          ;READ READ SECTOR ROUTINE
                          ;
                          ;READ SECTOR ROUTINE INITIATES THE READ
                          ;COMMAND AND TRANSFERS ALL THE DATA FOR A
                          ;SELECTED SECTOR TO THE BOTTOM OF MEMORY
                          ;BEGINNING AT LOCATION 5FF
                          ;R,XX READ SECTOR, SECTOR ADRS
             8000         PORTA    EQU 8000H       ;PORT A ADDRESS
             8001         PORTB    EQU 8001H       ;PORT B ADDRESS
             8002         PORTC    EQU 8002H       ;PORT C ADDRESS
             0793         POUT     EQU 793H        ;PORT B SET AS OUTPUTS ROUTINE
             0798         PIN      EQU 798H        ;PORT B SET AS INPUTS ROUTINE
             0769         STATUS   EQU 769H        ;ROUTINE CONVERTS STATUS TO
                                                    ASCII PRINTABLE DATA
             05FF         DATBUF   EQU 5FFH        ;BEGINNING ADRS OF "READ"
                                                    DATA BUFFER
             0520         CHARS    EQU 520H        ;COMMAND CHARACTERS ENTERED
                                                    VIA CONSOLE
                          ;
             0B10                  ORG 0B10H
                          ;
0B10         2A2205       READ     LHLD CHARS+2    ;GET BOTH CHARS
0B13         7C                    MOV A,H         ;XFER LS CHAR
0B14         B7                    ORA A           ;TERM?
0B15         F21C0B                JP TWO          ;NO
0B18         7D                    MOV A,L         ;LOAD SINGLE CHAR
0B19         C3220B                JMP SECTOR
0B1C         7D           TWO      MOV A,L         ;XFER MS CHAR
0B1D         07                    RLC             ;SHIFT TO MS POSITION
0B1E         07                    RLC
0B1F         07                    RLC
0B20         07                    RLC
0B21         84                    ADD H           ;MERGE CHARS
0B22         327C0B       SECTOR   STA SECSTR      ;STOR SECTOR          }
0B25         CD9307                CALL POUT       ;PORTB OUTPUTS        }
0B28         210280                LXI H,PORTC     ;GET PORTC ADRS       }
0B2B         0602                  MVI B,02H       ;SECTOR REGISTER      }
0B2D         70                    MOV M,B         ;WRITE PORTC          }
0B2E         3A7C0B                LDA SECSTR      ;SECTOR ADRS          }
0B31         2F                    CMA             ;INVERT FOR WD BUS    }
0B32         320180                STA PORT B      ;WRITE PORTB          }
0B35         0606                  MVI B,06H       ;WRITE TO SECTOR      }
                                                    REG                  }
0B37         70                    MOV M,B         ;WRITE PORTC          } COMMAND
                          ;                                              } HANDSHAKE
                          ;INITIATE THE READ COMMAND                     }
                          ;                                              }
0B38         0600                  MV B,0          ;SEL CMD REG          }
0B3A         70                    MOV M,B         ;WRITE PORTC          }
0B3B         3E88                  MVI A,88H       ;READ CMD             }
0B3D         2F                    CMA             ;INVRT FOR WD BUS     }
0B3E         320180                STA PORTB       ;WRITE PORTB          }
0B41         0604                  MVI B,04H       ;ISSUE READ TO        }
                                                    CMD REG              }
0B43         70                    MOV M,B         ;WRITE PORTC          }

                          ;
                          ;WAIT FOR END OF READ — THEN REPORT
                          ;
```

Listing 3 continued on page 96

Listing 3 continued:

```
0B44    0603                 MVI B,03H      ;SEL DATA REG          }
0B46    70                   MOV M,B        ;WRITE PORTC           }
0B47    CD9807               CALL PIN       ;PORTB = INPUTS        }
0B4A    11FF05               LXI D,DATBUF   ;FWA OF DATA           }
0B4D    0603                 MVI B,03H      ;RE,WE=1               }
0B4F    C35C0B               JMP DLOOP                             }
0B52    3E0B        GD       MVI A,0BH      ;RE=0                  } DATA
0B54    77                   MOV M,A        ;WRITE PORTC           } TRANSFER
0B55    3A0180               LDA PORTB      ;GET DATA              } SEQUENCE
0B58    2F                   CMA            ;INVERT DATA           }
0B59    12                   STAX D         ;SAVE IT               }
0B5A    1B                   DCX D          ;BUMP INDEX            }
0B5B    70                   MOV M,B        ;RE=1,PORTC            }
0B5C    7E          DLOOP    MOV A,M        ;GET STATUS            }
                                             PORTC                 }
0B5D    B7                   ORA A          ;DRQ=1?                }
0B5E    FA520B               JM GD          ;YES                   }
0B61    E640                 ANI 40H        ;INTRQ SET?            }
0B63    CA5C0B               JX DLOOP       ;NO                    }
                    ;
                    ;READ DONE — GET STATUS
                    ;
0B66    3E00                 MVI A,O        ;ADRS STAT REG         }
0B68    77                   MOV M,A        ;WRITE PORTC           }
0B69    3E08                 MVI A,08H      ;STROBE RE=0           }
0B6B    77                   MOV M,A        ;WRITE PORTC           }
0B6C    EB                   XCHG                                  } STATUS
0B6D    227E0B               SHLD ISAVE     ;SAVE INDEX TO         } HANDSHAKE
                                             DATA                  }
0B70    EB                   XCHG           ;RESTOR PORTC          }
                                             ADRS                  }
0B71    3A0180               LDA PORTB      ;GET STAT BYTE         }
0B74    0600                 MVI B,0        ;STAT HANDSHAKE        }
0B76    70                   MOV M,B        ;WRITE PORTC
0B77    2F                   CMA            ;INVERT STAT
                                             BYTE
0B78    CD6907               CALL STATUS    ;REPORT STATUS
0B7B    C9                   RET
                    ;
0B7C    0000        SECSTR   WORD 0         ;SECTOR ADRS
0B7E    0000        ISAVE    WORD 0         ;DATA INDEX
                                             STORAGE AREA
        0B10                 END READ
```

Listing 4: *Write-sector routine. This routine causes a section of memory to be written to a given sector on the disk. The sector number is specified by a 2-digit number entered from the system console.*

```
Hexadecimal  Hexadecimal  Label   Instruction    Commentary
Address      Code                 Mnemonic
                                  and Operand

                          ;WRITE WRITE SECTOR ROUTINE
                          ;
                          ;WRITE SECTOR ROUTINE INITIATES THE WRITE
                          ;COMMAND AND TRANSFERS ALL THE DATA FOR A
                          ;SELECTED SECTOR
                          ;
                          ;W,XX = WRITE SECTOR,SECTOR ADRS
8000         PORTA                EQU 8000H      ;PORT A ADRS
8001         PORTB                EQU 8001H      ;PORT B ADRS
8002         PORTC                EQU 8002H      ;PORT C ADRS
0793         POUT                 EQU 793H       ;PORT B SET AS
                                                  OUTPUTS
                                                  ROUTINE
0798         PIN                  EQU 798H       ;PORT B SET AS
                                                  INPUTS ROUTINE
0769         STATUS               EQU 769H       ;ROUTINE
                                                  CONVERTS
                                                  STATUS TO ASCII
                                                  PRINTABLE DATA
0520         CHARS                EQU 520H       ;COMMAND CHAR-
```

Listing 4 continued on page 98

Listing 4 continued:

```
                                                    ACTERS ENTERED
                                                    VIA CONSOLE
                          ;
        0B80                      ORG 0B80H
                          ;
0B80    2A2205            READ    LHLD CHARS       ;GET BOTH CHARS
                                  +2
0B83    7C                        MOV A,H          ;XFER LS CHAR
0B84    B7                        ORA A            ;TERM?
0B85    F28C0B                    JP TWO           ;NO
0B88    7D                        MOV A,L          ;LOAD SINGLE
                                                    CHAR
0B89    C3920B                    JMP SECTOR
0B8C    7D                TWO     MOV A,L          ;XFER MS CHAR
0B8D    07                        RLC              ;SHIFT TO MS
                                                    POSITION
0B8E    07                        RLC
0B8F    07                        RLC
0B90    07                        RLC
0B91    84                        ADD H            ;MERGE CHARS
0B92    32E50B            SECTOR  STA SECSTR       ;STOR SECTOR        }
0B95    CD9307                    CALL POUT        ;PORTB OUTPUTS      }
0B98    210280                    LXI H,PORTC      ;GET PORTC ADRS     }
0B9B    0602                      MVI B,02H        ;SECTOR             }
                                                    REGISTER           }
0B9D    70                        MOV M,B          ;WRITE PORTC        }
0B9E    3AE50B                    LDA SECSTR       ;SECTOR ADRS        }
0BA1    2F                        CMA              ;INVERT FOR WD      }
                                                    BUS                }
0BA2    320180                    STA PORTB        ;WRITE PORTB        } COMMAND
0BA5    0606                      MVI B,06H        :WRITE TO           } HANDSHAKE
                                                    SECTOR REG         }
0BA7    70                        MOV M,B          ;WRITE PORTC        }
                          ;                                            }
                          ;INITIATE THE READ COMMAND                   }
                          ;                                            }
0BA8    0600                      MVI B,O          ;SEL CMD REG        }
0BAA    70                        MOV M,B          ;WRITE PORTC        }
0BAB    3EA8                      MVI A,0A8H       ;WRITE CMD          }
0BAD    2F                        CMA              ;INVRT FOR WD       }
                                                    BUS                }
0BAE    320180                    STA PORTB        ;WRITE PORTB        }
0BB1    0604                      MVI B,04H        ;ISSUE READ TO      }
                                                    CMD REG            }
0BB3    70                        MOV M,B          ;WRITE PORTC        }
```

Listing 4 continued on page 100

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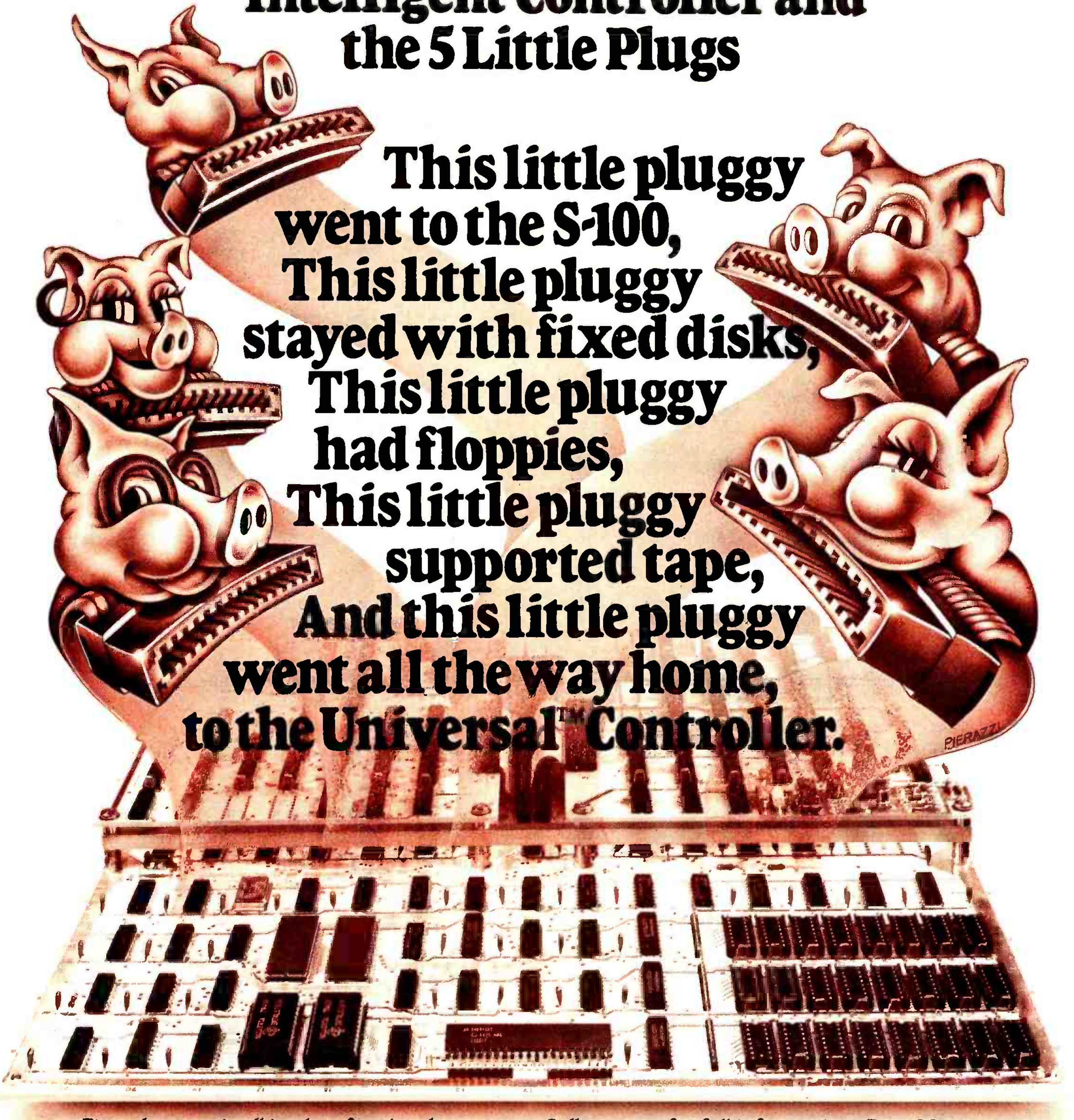

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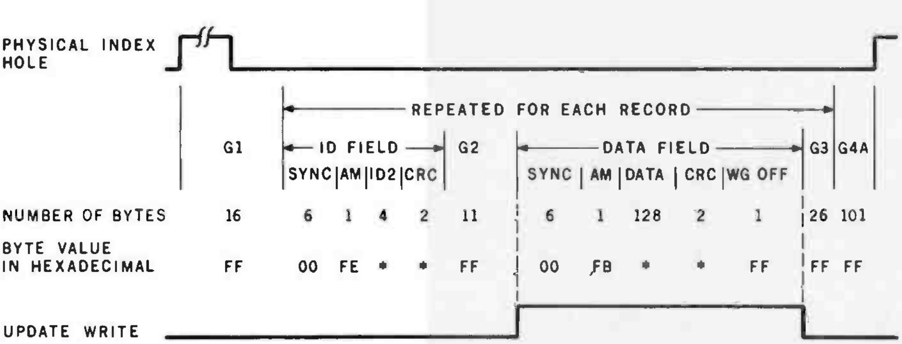
Listing 4 continued:

```
                                  WAIT FOR END OF READ — THEN REPORT

0BB4      0603                        MVI B,03H      ;SEL DATA REG        \
0BB6      70                          MOV M,B        ;WRITE PORTC         |
0BB7      110180                      LXI D,PORTB    ;PORTB ADRS          |
0BBA      0603                        MVI B,03H      ;RE,WE=1             |
0BBC      C3C70B                      JMP DLOOP                           |
0BBF      3E8D            GD          MVI A,8DH      ;LOAD DATA           |
0BC1      2F                          CMA            ;INVRT DATA          |  DATA
0BC2      12                          STAX D         ;WRITE PORT B        |  TRANSFER
0BC3      3E07                        MVI A,07H      ;WE=0                |  HANDSHAKE
0BC5      77                          MOV M,A        ;WRITE PORTC         |
0BC6      70                          MOV M,B        ;RE=1,PORTC          |
0BC7      7E              DLOOP       MOV A,M        ;GET STATUS          |
                                                      PORTC               |
0BC8      B7                          ORA A          ;DRQ=1               |
0BC9      FABF0B                      JM GD          ;YES                 |
0BCC      E640                        ANI 40H        ;INTERQ SET          |
0BCE      CAC70B                      JZ DLOOP       ;NO                  /
                                  READ DONE — GET STATUS

0BD1      CD9807                      CALL PIN       ;PORTB INPUTS        \
0BD4      3E00                        MVI A,0        ;ADRS STAT REG       |
0BD6      77                          MOV M,A        ;WRITE PORTC         |
0BD7      3E08                        MVI A,08H      ;STROBE RE=0         |  STATUS
0BD9      77                          MOV M,A        ;WRITE PORTC         |  HANDSHAKE
0BDA      3A0180                      LDA PORTB      ;GET STAT BYTE       |
0BDD      0600                        MVI B,0        ;STAT HANDSHAKE      |
0BDF      70                          MOV M,B        ;WRITE PORTC         /
0BE0      2F                          CMA            ;INVERT STAT
                                                      BYTE
0BE1      CD6907                      CALL STATUS    ;REPORT STATUS
0BE4      C9                          RET

0BE5      0000            SECSTR      WORD 0         ;SECTOR ADRS
          0B80                        END READ
```



LEGEND:

ID	IDENTIFICATION
AM	ADDRESS MARK
CRC	CYCLIC REDUNDANCY CHECK FIELD
WG OFF	WRITE-GATE-OFF BYTE

Figure 3: *Format of data as recorded on one track of the disk drive. Each track contains sixteen records, each of which contains 128 bytes. Each record consists of an identification (ID) field followed by a data field. The columns marked with an asterisk represent fields with contents that vary from record to record.*

Text continued from page 86:

contains the following: track address, side-select byte (set to 00 here), sector address, and sector length (set to 00 here because the sector length is constant); each field is 1 byte long. The cyclic-redundancy-check (CRC) section contains a 2-byte value that serves to check the accuracy of the previous bytes as written onto the disk. A command byte of hexadecimal F7 sent to the FD1771 controller causes it to generate and write the CRC bytes.

The data field also begins with a sync section. The address mark for this section, hexadecimal FD, is a different value than for the sync section in the identification field. A data section of 128 bytes follows and can be filled with any desired data. The last section within the data field is the write-gate-off (WG-off) byte, which allows the head an area in which to be

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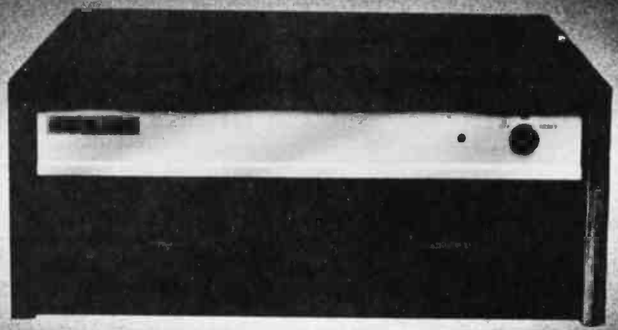

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turned off from the write mode without destroying any valid data. Although a hexadecimal FF is written to this field, we do not care what value resides in the WG-off field on the floppy disk.

Once the disk is formatted, reading or writing can begin. The read and write commands are similar in several respects to other commands such as the seek command. Each must be part of a software routine in which a command parameter is loaded into the data, sector, or track register, and the command itself is loaded into the command register. All commands also generate an interrupt signal at their completion. This interrupt must be reset through a status handshake routine that reads the status register.

However, the read and write commands differ from commands like the seek command in the following one respect: data must be transferred. For example, a write command, in a data-transfer routine like that presented in hexadecimal locations 0BB4 thru 0BCE of listing 4, places a byte of data in port B and points the address pointers (lines A0 and A1) to the data register. When the FD1771 raises the DRQ line, the $\overline{\text{WRITE-ENABLE}}$ line is brought low. The byte of data, which is placed in the FD1771 data register, is transferred from the FD1771 to the disk. The 8080A places another byte in the port and pulls the $\overline{\text{WRITE-ENABLE}}$ line low again when the FD1771 signals that it is ready to accept another byte of data. A similar procedure is followed for a read command (see listing 3), except that this command uses the $\overline{\text{READ-ENABLE}}$ line.

This concludes our discussion of the hardware and software necessary to interface a Shugart SA400 disk drive to an 8080A-based microcomputer system. Additional application information is given in the application notes available from the companies listed in the references. ■

References

1. *SA400/450 Minifloppy Diskette Storage Drives with an 8080A/FD1771 Single Density System Application Bulletin*, Shugart Associates, 415 Oakmead Parkway, Sunnyvale CA 94086
2. *FD1771 Floppy Disk Formatter/Controller Data Sheet*, Western Digital Corporation, 3128 Red Hill Ave, POB 2180, Newport Beach CA 92663
3. *Intel 8080 Microcomputer Systems User's Manual*, Intel Corporation, 3065 Bowers Ave, Santa Clara CA 95051

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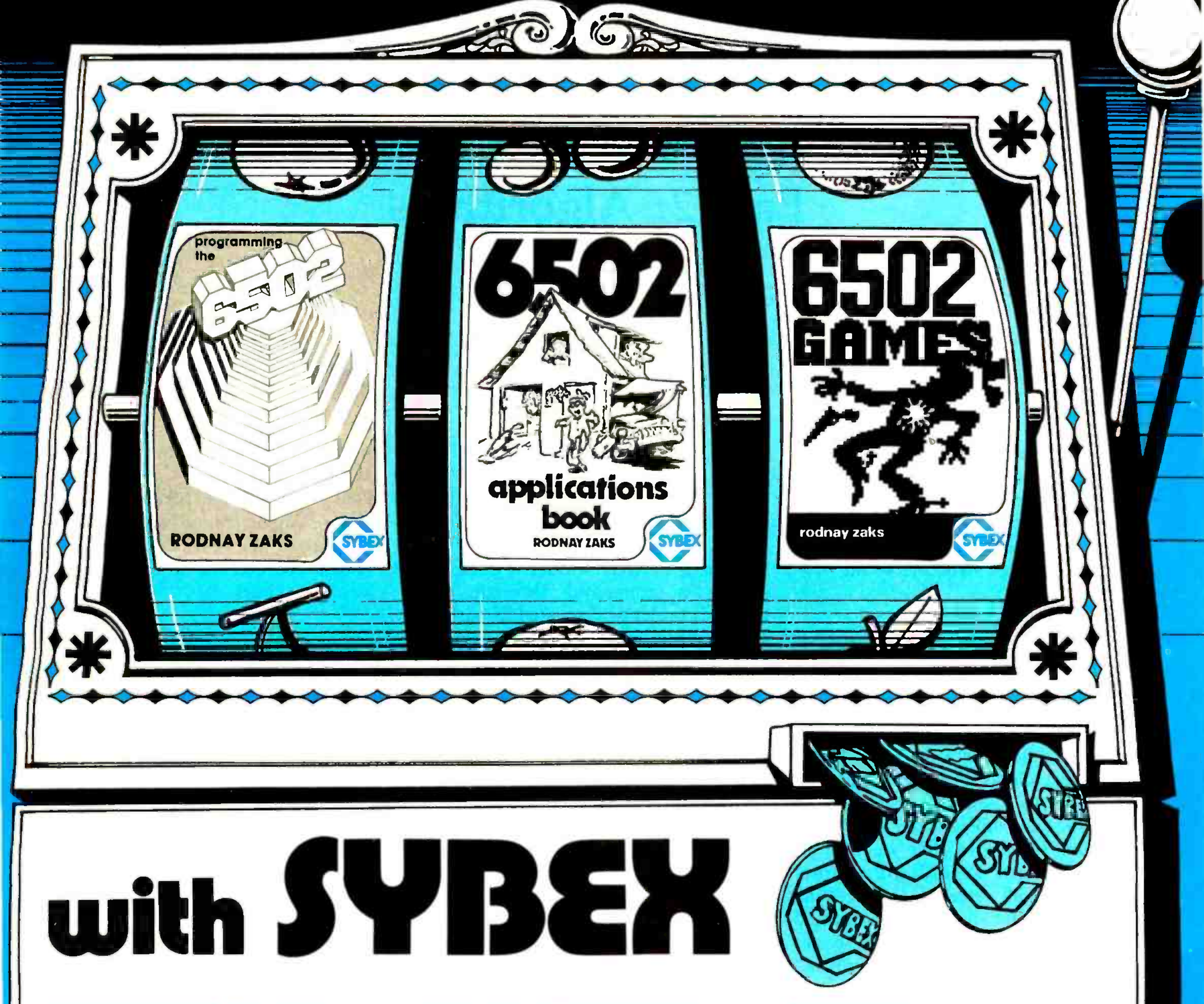

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The Commands

With what commands should the editor provide the user in order to make the program easy to use, and how does the nature of these commands affect the structure of the program?

Mode Commands

We begin to answer this question by distinguishing three major ways in which the user will use the program. The first is when the user creates a score of music. Here the editor must establish a file for the score and allow the user to overwrite the default values for the music, such as the key and time signatures. The second major use consists of editing the score. The program needs to provide facilities for locating the measure to be edited, reformatting the pages after editing, and writing the finished version out to a file. The third and hardest facility the editor must provide is the ability to display the score on the screen.

A multitude of problems must be handled automatically by the editor in adjusting the format of the score as it will appear on the screen. The above discussion leads to a definition of three separate modes of operation for the editor called the CREATE, EDIT, and DISPLAY modes. Switching between modes is done by issuing a command through the graphics tablet as discussed in part 1. The editor also switches modes automatically to display the contents of a measure while the user creates or edits the score.

Location Commands

Commands must be provided to allow sequential passage through the score. In order to do this, the user must first set a symbolic-operation mode which determines the units to be used as increments in moving through the score. These units are pages, lines, measures, or characters, and are set via commands on the template. For example, suppose you are located on page two, line one, measure three, and character twenty-one of the score, and you wish to edit page five, line four, measure one, and character three. The following sequence of commands will accomplish this:

1. Touch page. This sets the increments to pages, and sets the line, measure, and character values to one.
2. Touch forward three times. This positions you on the first line, measure, and character of page five.
3. Touch line. Touch forward three times. You are now at the first measure of line four.
4. Touch character and touch forward two times.

If you are editing the end of a unit, it is often faster to back up. If you were editing the last character, number thirty-seven, of measure one above, you could go to measure two and then back up one character rather than going forward from measure one, thirty-seven times. If the program is to provide this flexible location scheme to the user, it should be easy to determine the location of the page, line, measure, and character at any place in the score. A look back at the data structures indicates that this was accomplished using doubly-linked pointers between the score area arrays.

Edit Commands

The program must support all editing features that allow easy text manipulation. Commands to insert, delete, replace, or move pages, measures, lines, or characters must be provided, as well as methods of searching the text for patterns of music. These facilities require a set of routines that will automatically adjust the paging of the music after editing.

Note
The figure numbering sequence is continued from part 1 which appeared in the April 1980 BYTE.

Circle 61 on inquiry card.

Exit Commands

After editing a measure, the user either wants the version to become a permanent part of the score, or wishes to inform the program to ignore any changes made. This is the function of the EXIT and NULL-EXIT commands on the template. Note that the exit command must transfer the contents of the work area to the score area and make the necessary format changes while the NULL-EXIT simply does nothing.

Symbols

Music abounds with symbols. The template shown in part 1 indicates only a few. The actual design allows for one hundred different symbols. In order to avoid cluttering the template you would have to cull the necessary symbols for the type of music that is being scored. To transfer from one notational style to another is not a difficult task, since only the template and interface program would have to be changed. The main portion of the editor is protected from such alterations.

Output

The hardest problems of the editor are related to displaying the musical score on the screen in a pleasing and useful format. I will touch on three classes of problems, and outline their solutions in this section.

Dimension Problems

This set of problems is caused by the physical dimensions of the screen output. The actual physical dimensions of the height and length of the screen are fixed, and you must work around their limitations. Since most graphics screens represent points in a coordinate system, the maximum and minimum absolute coordinates for the X and Y axis are set.

In order to achieve a flexible design, no commitment should be made to any of these machine-dependent characteristics. Instead, you should work in a virtual coordinate space controlled by the editor, and write another interface program to handle the conversion of coordinates in the virtual space to the actual screen coordinates. Every dimension that is given will then represent a dimension of the virtual space in the editor. Since the option of determining the size of a score of music should be left to the user, you must understand that all dimensions are subject to scaling factors that will be set by the user on entrance to the program. With these considerations in mind, I will now discuss three problems and their solutions.

1. The Spacing Problem for the Staff

How are the dimensions for the staff, notes, and symbols determined? The solution was found by taking measurements from scores of music and determining the standard sizes. Figure 5 shows the dimensions of the staff and lists the dimensions for other symbols. Note that all dimensions are given in terms of LSPACE, which is the distance between the lines of the staff.

2. The Length of the Measure Problem

How do you assign a virtual length to a measure? Although each measure has the same number of beats, their lengths can differ radically. Observe in figure 7 that the length between notes of the same value is not always equal. This eliminates a simple method in which you would assign virtual lengths to specific note values

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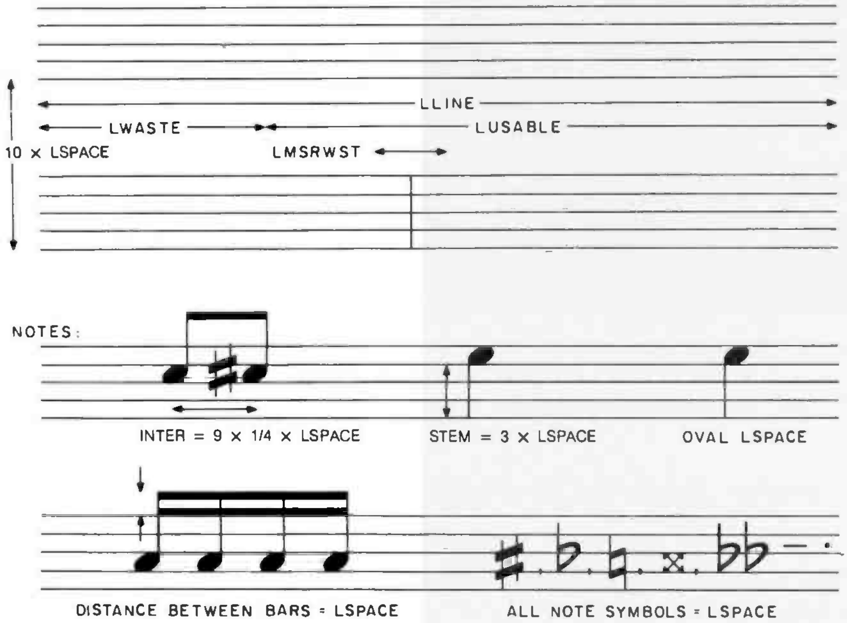


Figure 5: *Dimensions of the musical staff, notes, and symbols. All dimensions are given in terms of LSPACE, the distance between the lines of the staff.*

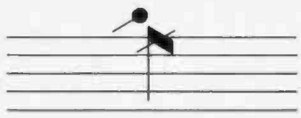
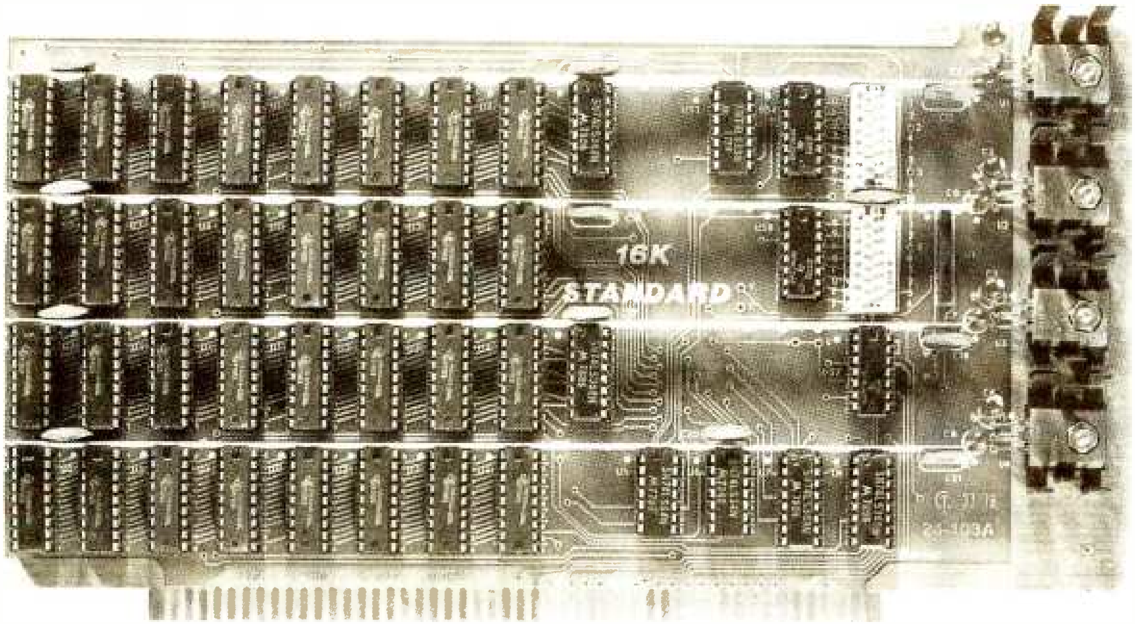


Figure 6: *An example of a rarely occurring musical symbol. Of the many thousands of symbols which are used to communicate different forms of expression, some are used only infrequently. This particular symbol is found in piano music. It directs the performer to reach inside the instrument and strike the string corresponding to the indicated note with a mallet.*

and determine the total length of the measure by summing their values. A modified approach to this simple scheme can be adopted, however. You must first determine the minimum distance between notes that allows sharps and flats to be inserted, while still preserving readability. This distance can be fine-tuned to the eye of the user, but it is approximately nine-fourths the distance between the lines of the staff, or $(9/4) \times$ LSPACE. This dimension will be called the *internote distance*, denoted by INTER. Second, a *beaming group* is defined as a set of notes that are connected by beams. Later I will discuss a routine that determines beaming groups in the measure. Assume here that the job has been done. Next, a code for each possible note value is determined (this code was actually developed much earlier and is used throughout the program in most of the data structures). This information is shown in table 5. Notice that all the values are integer quotients of 20160. There are several reasons for this particular encoding scheme. First, the editor allows for twenty-six different note values. In order that the subgroupings of these notes add up to correct total values, each note must have the same common denominator. The value 20160 fulfills the requirement. The code for one beat is 5040. Other reasons for this encoding concern the eventual placement of the notes in their proper screen locations. The total length of the measure is now the sum of the lengths of all of the beaming groups of that measure plus the lengths of the rests. The algorithm for determining the length for the beaming groups can now be stated:

1. Determine the total number of beats for the beaming group. This can be done by summing the codes for all the notes in the group and dividing by 5040, the value for one beat. Let this value be NUM.
2. Find the minimum value for the beaming group. Call this MIN.
3. Determine the number of notes required if the total number of beats were to be taken up by the minimum note. This is simply NUM / MIN.
4. Multiply this number by the internote distance. Thus you finally get the length, which is equal to (NUM / MIN × INTER.

You can now perform the above routine for all of the beaming groups of the measure and sum up the lengths, with rests included. The total value represents the virtual length of



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Others: Fifth 1008, Seventh 720, Ninth 560, Tenth 504, Eleventh 458, Twelfth 420, Thirteenth 387, Fourteenth 360, Fifteenth 336.

Table 5: *Additional musical symbols.*

the measure. This is stored in the character array of the score area.

3. The Line Length Problem

With different sized measures, how do you determine the number of measures that will fit on each line, thus assuring that the bar lines at the end of each line are aligned? The difficulty of this problem is increased by the fact that not all of the space in a line is used. Each line of music starts with a clef, key signature, and time signature. Every bar line of every measure is bounded by empty space. (Refer to figure 5.) All of these spaces must be accounted for in determining the number of measures that can fit on each line.

Assume that the total length of the line in virtual space is LLINE. The first part of that space must be allocated to the clef and signatures; this will be called LWASTE. The total usable virtual space, LUSABLE, is then equal to LLINE−LWASTE. The wasted space around each measure will be called LMSRWST. If N measures are on the line, then N×LMSRWST space has been wasted in these measures. Now suppose that you are positioned at the first measure that will go on the line. You know the virtual lengths of this measure and all that follow. Denote the sum of the lengths of these first N measures as SUMN. The problem is then to find the largest N such that:

$$\text{LUSABLE} \geq \text{SUMN} + \text{N} \times \text{LMSRWST}$$

This says that you want to find the greatest number of measures that can be put on the line before going past the end of the line. In general, the measures will not fit perfectly on the line; therefore there will be excess space at the end. This excess must be distributed equally among the measures, and to do this you must find a scaling factor to transform each X coordinate of the measure into a new coordinate. This scaling factor can be easily determined. Let EXCESS be the excess space at the end of the line. It is equal to LUSABLE − SUMN − N × LMSRWST. The scaling factor then is simply LUSABLE/(LUSABLE − EXCESS). The solution to the line length problem is shown in algorithmic form in listing 1.

Beaming

Before this problem can be formulated I will review some of the questions that must be answered when writing music on the page. These are various conventions used for writing music. The following lists a few of these problems.

Stems Up or Down?

You must first decide if a group of eighth or sixteenth notes will be underbeamed or overbeamed (ie: whether the ligature is placed at the top or bottom of the note stems which point up or down, respectively). The easiest solution to this problem consists in finding the maximum note displacement from the center line of the staff and then drawing the note stems in that direction. There are several exceptional cases for this simple algorithm. For example, if the previous group of notes was underbeamed and the maximum displacement of the next group is above the middle line of the staff (but not by much), the score will read easier if the group is underbeamed rather than overbeamed.

Determining Beam Inclination

Note in figure 7 that the ligature inclination of beaming groups is not always the same. To determine the angle of the beam, you must find the height difference between the stems of the maximum note and the minimum note. For each octave of this difference, increase the height of the tilt by one unit. Notice that the tilt can be either up or down. In the following discussion I will talk about one of the four cases: underbeamed and tilting upward. The other three cases are easy modifications to the algorithms.

Determining the Stem Lengths

The length of the stems from the notes depends on several factors. Suppose you have an underbeamed, upward-inclined beaming group. The shortest note stem must be at least a certain minimum length for readability. Once this distance is set, determine the lengths of the stems for the other notes of the beaming group. These distances depend on the location of the note and the angle of the beam. Although the algorithms are quite involved, they basically consist of solving equations to find the intersection point for the lines of the stems and the beam. A complete description of an example with all the equations is given in figure 8.

The algorithms for each of these problems are not difficult, and for the most part they consist of only a few instructions. However, the exceptional cases which make the music more readable are complex and tedious. Given the ad hoc nature of musical notation there seems to be no mechanical way to eliminate these exceptional cases. Let me briefly outline the basic algorithms. Once again, you assume that you have a routine that provides the beaming groups and that you are dealing only with an underbeamed upward-inclined group.

The beam-characteristic algorithm is shown in listing 2.

Next I will discuss how to determine the beaming groups. The basic strategy is to collect notes with flags until one either goes past a beat or encounters a rest. Then output a beaming group, and if a rest is encountered, continue within the beat to collect the remaining notes of the beat. Only in cases of syncopated rhythms will beaming groups cross over a beat. I might add that this is the reason for the strange initialization:

BEATCOUNT = BEATCOUNT + 5040

in step 2 of the algorithm, for if BEATCOUNT comes back negative from step 4, a beat has been crossed over. The algorithm is shown in listing 3.

Symbol Problems

Several ways are presented for routines that draw the notes and symbols on the screen. You must keep in mind that the eventual size of the symbols is left to the discretion of the user, and the program must therefore allow for scaling. Scaling sometimes distorts characters, so the editor must have procedures to keep this distortion within a readable limit. I found that for symbols consisting mostly of straight lines, simply storing a set of relative points and drawing lines between them is sufficient. For symbols that are curves, such as the G clef, a better approach is to use a spline-fitting routine to draw the symbol.

Listing 1: *Solution to the line-length problem in algorithmic form.*

```
1. LUSABLE = LLINE - LWASTE
2. N=1      SUMN=Virtual length of first measure
3. VALUE=SUMN+N×LMSRWST
   IF LUSABLE<VALUE THEN GO TO 4
   N = N +1
   SUMN = SUMN + VALUE of virtual length of Nth measure
   GO TO 3
4. EXCESS = LUSABLE - VALUE
   LSCALE = LUSABLE / (LUSABLE - EXCESS)
5. Store scale into the scale portion of the line array for future use when displaying the
   measure.
```

Listing 2: *Algorithm used to determine whether a group of notes should be under or overbeamed.*

```
1. Find the minimum note in the beaming group. MINX, MINY
   Find the maximum note in the beaming group. MAXX, MAXY
   Let OCTAVE be the height of an octave.
   Let MID be the height of the middle note of the staff.
   Let STEM be the minimum length of a stem.
   Let LENGTH be the virtual length of the beaming group.
2. IF (MAX - MID) ≥ (MID - MIN) then overbeam, ELSE underbeam.
   Assume underbeam.
3. TILT = (MAX - MIN) / OCTAVE (integer division)
4. For each note in beaming group:
   Get coordinates into NOTEX, NOTEY
   M = TILT / LENGTH
   B = (MINY - STEM) - MINX × M
   The height of the stem for this note is then equal to NOTEY - M × NOTEX - B.
```

Listing 3: *Algorithm to determine the beaming groups.*

```
1. BEATCOUNT = 0
   MEASURECOUNT = Number of beats to a measure times 5040.
2. BEATCOUNT = BEATCOUNT + 5040
   IF MEASURE ≤ 0      GO TO 5
3. Get value of next note into NOTEVAL
   BEATCOUNT = BEATCOUNT - NOTEVAL
   MEASURECOUNT = MEASURECOUNT - NOTEVAL
4. IF BEATCOUNT ≤ 0 THEN output group and GO TO 2.
   IF encountered a rest THEN output group and go to 3
5. Finished with measure, either continue or stop.
```
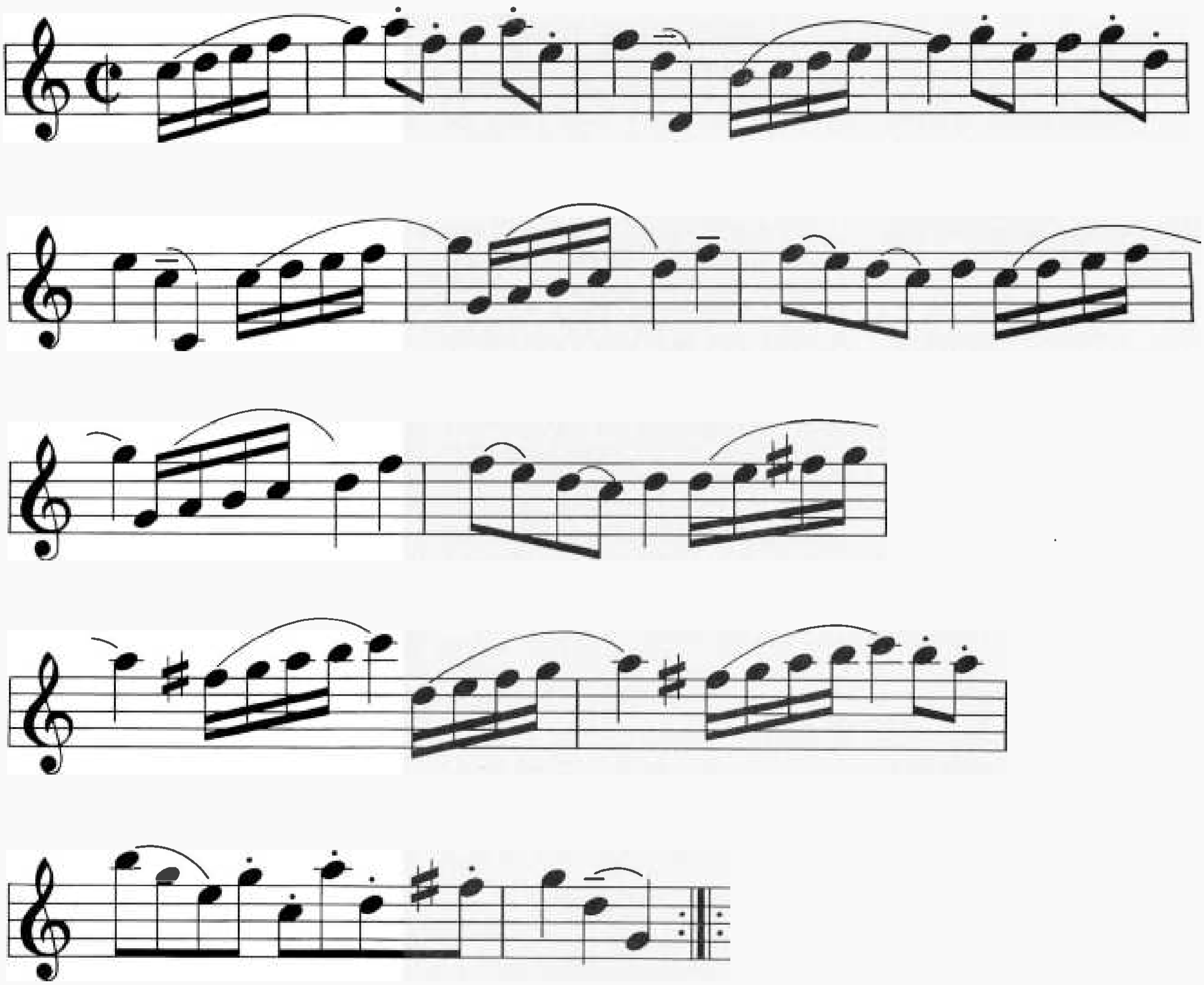
Figure 7: *Sample of a musical score, in this case part of a bourrée by J S Bach. Note the difference in note spacing and in angles of beams.*

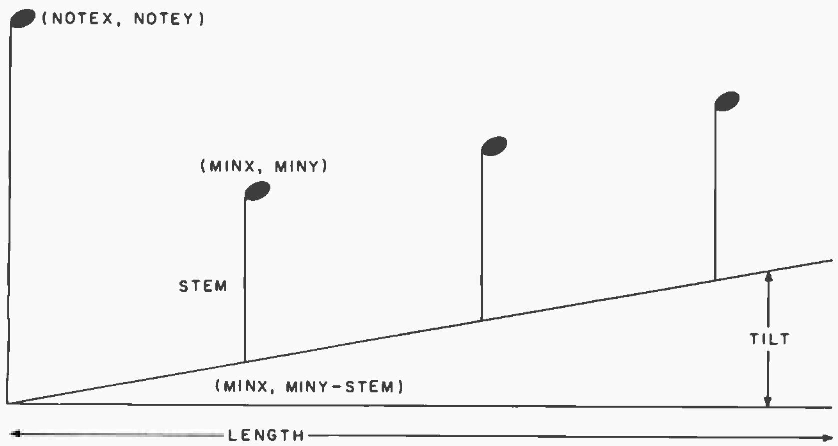

Figure 8: *Calculating the equation of the line segment forming a beam. The standard slope intercept equation $Y = mX + b$ is used. We know that the slope is $M = TILT/LENGTH$, and that the value of one point on the line is (MINX, MINY−STEM). Fitting this to the equation of the line, we can find $b = (MINY-STEM) - M \times MINX$. The heights for all the other stems can then be calculated. For each note, put the X and Y coordinates in NOTEX and NOTEY. The height for this stem is then $HEIGHT = NOTEY - M \times NOTEX - b$.*

Although this requires much more computation time on the computer, it does produce an aesthetically pleasing symbol and allows the user to fine-tune the form of the symbol by simply moving a few of the interpolation points.

Other Points

Now that the basic design of the editor has been presented, I will discuss some of the finer points of the design.

Patterns and Sequences

Although the input format is satisfactory for most music, the use of the current template becomes taxing, if not impossible, when creating a score of complex music. There is no facility that allows the user to input complex rhythms. In order to provide this ability, the concept of a pattern

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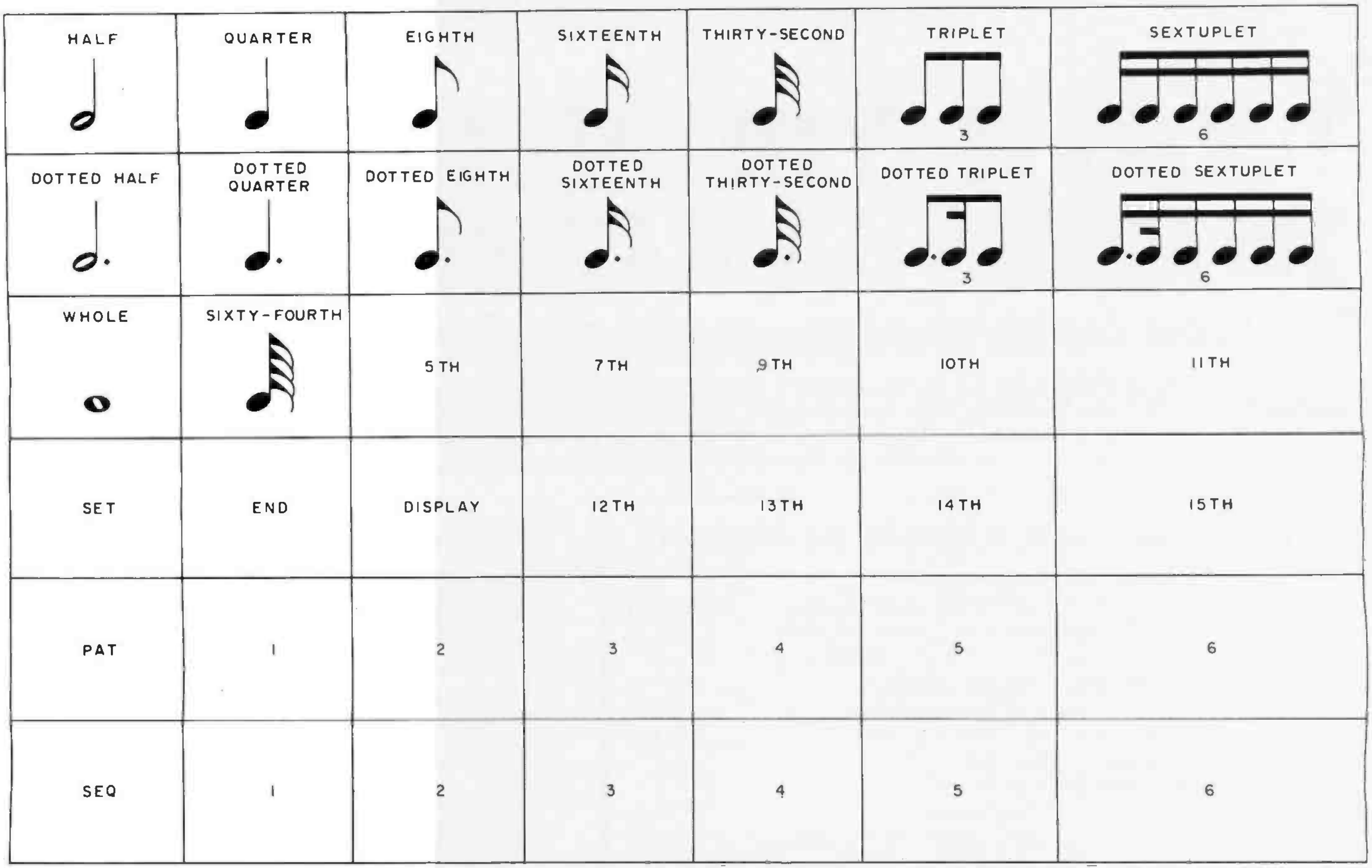

Figure 9: *Extensions to the musical template for more advanced editing.*

of rhythm is created. Here the user can establish any rhythmic pattern with a code number. When this code number is touched on the template, the interface program organizes the notes which are entered after it according to that rhythm. The template must now have more fields on it to accommodate this ability, and the interface program must be expanded to perform these computations. The extensions to the template are shown in figure 9. In order to create a rhythmic pattern the user must issue the following commands:

1. Push SET and PAT. This informs the interface program that a pattern is to be created.
2. Push a number on the PAT row. This will be the number of the pattern, and any existing pattern with this number is overwritten.
3. Push the series of note values which determines the pattern.
4. Push END. This signifies the end of the pattern.

To use the pattern the user issues the following commands:

1. Push the number of the pattern.
2. Push the pen onto the correct pitch positions on the staff, preceding them with any attached symbols such as sharps, dots, slurs, etc. Note that the order of the notes and symbols is now important, but the X locations on the staff are immaterial.

The end of the pattern occurs when the number of notes of the pattern is pushed onto the screen. If more notes are entered before another pattern number is pushed, the interface program issues a warning to the user signifying that the pattern is ended. If an insufficient number of notes is entered before another command is issued, the user is warned and the incomplete input is discarded.

A sequence, as used here, is simply a series of patterns. Suppose that sequence 1 consists of the patterns 2, 5, 1. The use of sequence 1 will cause the notes pressed to follow the rhythm of pattern 2. When all of its notes are used up, it will follow the rhythm of pattern 5, and when that is finished, it will follow pattern 1. Setting a sequence is similar to the setting of a pattern. The steps are:

1. Push SET and SEQ.
2. Push a number in the SEQ row. This is the sequence number.
3. Push a series of numbers in the PAT or SEQ row.
4. Push END.

Sequences can cross over measures and can consist of other sequences. To clarify these concepts, input the music in figure 7, using patterns and sequences. There are many ways to input that section of score. Break up the rhythms into their smallest components and then form sequences from them. Thus, three patterns are defined first: one consisting of a quarter note only, the other of two eighth notes, and the last of four sixteenth notes. The following commands do this:

1. Push SET, PAT, and 1.
2. Push QUARTER.
3. Push END.

4. Push SET, PAT, and 2.
5. Push EIGHTH twice.
6. Push END.

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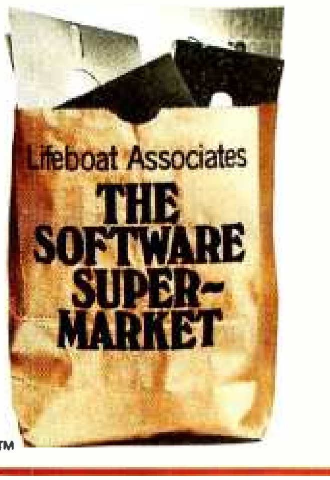

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7. Push SET, PAT, and 3.
8. Push SIXTEENTH four times.
9. Push END.

Note that there are now four sequences that can be defined. They are labelled on the score. I will create the commands for the first one only, since the others are similar:

1. Push SET, SEQ, and 1.
2. Push 3,1,2,1,2,1,1,1 on the PAT row.
3. Push END.

The other sequences consist of:

#2 - 3,1,3,1,1,2,2,1
#3 - 3,1,3,1
#4 - 2,2,2,2,2,1,1,1

The different ways of ordering sequences and patterns are numerous. The above score in particular could have been entered in several ways.

Using a scheme like this, any score of music can be entered into the editor. Other schemes could be devised to tailor the input form to the type of music being edited. The only changes to the program, however, would occur in the input-interface program; the main part of the editor would remain unchanged.

Symbols That Cross Over Measures

I have not yet approached the problem of symbols that cross over measures and, thus, over lines and pages. Nor have I discussed the placement of nested slurs or ties and how to draw them on the screen. These problems are complex; their solutions lie in keeping pointers in the character array to the locations where the symbol begins and ends. Any changes to these measures, such as deletion, must also change these pointers — for example, we do not have a beginning of a crescendo with no end. Thus these pointers must again be doubly-linked. Drawing the correct arcs for slurs and ties presents a problem because they can be separated by long distances. A routine must be called when the screen locations are known to fit a curve through these points.

Reformatting

After editing a page, the format of the pages from then on is usually different. If you simply added a character in a measure, the paging will probably remain the same; however, if you add thirty notes to the measure, it is much longer, and might change the number of measures on the line and hence the format of the page. How far this change will carry depends upon the size of the change and the scaling factors of the measures. (If the scaling factors were all 1.0, then any change to a measure would cause a complete repaging of the score.)

Whenever the user wants to display or edit the score, a formatting program must be called to repage the score. This routine must execute the algorithms given previously, which determine the beaming groups of the measures and the measure lengths of all changed measures. It must then determine which measures will go on the lines. It needs to alter the existing paging only as far as the change propagates, but there is no way to predict this in advance. Thus a simple change could cause considerable computation.

Conclusion

I hope that the reader has begun to appreciate the problems involved in creating a text editor for music. What is the utility of such a program? To anyone who has ever tried printing a score of music with india ink, the virtues of an editor with hard-copy facilities are obvious. A number of uses for the program present themselves. For example, very often music written in one key needs to be changed into one of the other keys. This is called *transposition*. A program can easily be written which takes the contents of the character array and performs the transformation.

You might wish to create computer music and display it on the screen. You could write a music-generation program and feed its output to a conversion routine that would convert its output into the format of the editor. If actual sounds were converted into pitches and durations with an electronic device, this could be placed in the editor, and you could see the music that was being played. If several scores by a composer are entered into the program and statistical analysis is performed on them to determine the probabilities of certain patterns of music, the results could, in theory, be used to drive a music-generation program that would simulate the composer's style. This same approach could be applied to music from different historical periods, thus enabling the computer to create a classical symphony or a twelve-tone quartet.■

Editor's note: The data-entry system for musical scores described in this article has a bias toward transcription of scores containing a single melodic line. Other types of musical scores contain elements which are not dealt with here. For instance, music for keyboard instruments, such as the piano, usually contain chords consisting of several notes to be sounded simultaneously. These chords are often written as several note heads sharing a single stem. It would be difficult at best to work with such music using this system. Enhancing the system to handle these elements would be a good project for the ambitious reader. . . . RSS

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Using the Computer as a Musician's Amanuensis

Part 2: Going from Keyboard to Printed Score

Jef Raskin
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More Problems with Rhythm and Tempo

The would-be Composer's Aid designer plummets into another pile of programming problems when tempi change. The beat, *sometimes* constant within a piece, may abruptly slow down, as may happen in a reflective refrain in a blues number, or gradually accelerate, as in a Greek folk dance. Changes of tempo present problems that are worse than the problems in transcribing rhythms that we have already seen.

It is not difficult to see that an abrupt change in tempo cannot be detected the instant that it happens, but only after a few notes have been played at the new speed, establishing, as musicians say, the new tempo. This brings up the concept that rhythm does not exist only in relation to the length of individual notes, but exists also in a much larger musical context.

About the Author
Jef Raskin's credentials in music include his years as a professional musician and a music teacher. He is presently the manager of Advanced Systems at Apple Computer Co. His personal music and computer equipment includes a piano, a harpsichord, an organ, a PDP-11, and three Apple II computers.

Therefore, a computer (or a human being) cannot notate rhythm in real time (ie: as it happens). The notator must wait and accumulate a significant sample (ie: listen for a while) before making any decision how to write down what has been heard. A computer program that must determine rhythms will most probably have to backtrack through the data, perhaps a number of times, before deciding how to notate the music.

> A computer (or a human being) cannot notate rhythm in real time.

Much of the fun in listening to music comes from anticipation of the rhythm; the composer or performer can use rhythmic expectations as a background against which to introduce rhythmic novelties. This is similar to the use of harmonic and melodic "surprises" that cannot be assessed until some time after they have been heard. The fact that we hear music in a context of expectations built on previous experience stands as a sentinel, guarding against the possibility that there is an easy algorithm that might "understand" music on a note-by-note basis.

Further Consequences of Changes of Tempo

A gradual change of tempo is either *accelerando* (getting faster) or *ritardando* (getting slower). In ritardando (very common at the ends of pieces or sections of pieces), how is the computer to tell the difference between a gradual lengthening of the written note values on one hand, and the use of the word "ritardando" along with an actual constant note length, on the other? This is very easy for a human to do, but it is very difficult to tell a computer how we do it.

In many pieces that require this slowing down, there is no notation for a ritardando at all. In these cases, the ritardando is inherent in the nature of the music. The conventional notation is to write the score as if nothing at all happens to the tempo.

This last problem afflicts score-to-performance transforming programs more than it afflicts programs that transform performances to scores. It is one of the symptoms of "soulless" computer performances. The computer too often is programmed with only the notes, but not with the *style*—that part of the music which is indigenous to a culture or time. Without the proper style, music tends to sound "wooden" or "dead."

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Someone Tries to Sell the Author a "Notating Machine"

An entrepreneur tried to interest me in funding a device he was in the process of patenting. According to him, it would do the "simple" task of transcribing any rhythm tapped out on its surface into standard musical notation. It was to be the size of a hand-held calculator.

I asked him the questions that I have brought up in this discussion, and it soon became clear that he had not given the matter even as much thought as I have been giving the problem in this article. As an answer to the question of accelerando and ritardando, he suggested that the instructions would specify that the user must not slow down or speed up.

As happens too often in the world of computing, he was forced to lean toward a device that would—perhaps—write down the easy rhythms, leaving the difficult ones for the user to figure out. Most users, I suspect, would rather have a device to write down the difficult rhythms. The users can figure out the easy ones without mechanical aid.

Incidentally, one of the most difficult problems for a beginner to solve is determining on which beat of a measure a piece begins. Pieces very often begin in the middle of a measure. This is also a vexing problem for anyone who would program a computer to notate rhythms.

Placing any restrictions not found in the music itself on the user seems inherently wrong to me. The system must accommodate the person, not the other way around.

There are many other problems with rhythm—for example, *rubato*, where one part momentarily goes faster or slower than accompanying parts. Another class of problems are rhythmic complexities such as triplets, grace notes (so short that their time value is not notated), and other groups of notes that break the simpler rhythmic patterns.

A *triplet* is a melodic phrase consisting of three notes of equal length, three quarter notes, for instance. These three quarter notes are played in the same time interval that two quarter notes occupy in the normal rhythm of the piece. It is difficult to tell what has happened when a few triplets are introduced in a piece. When they first occur in a piece, you may ask yourself (if you are a trained musician), "Has the tempo suddenly changed, or have triplets been introduced?" The program will be hard put to guess at the difference.

Another problem occurs when very long notes occur in a piece which previously consisted only of relatively short notes. You must decide, for instance, whether to write them as tied shorter notes or as longer note forms. Of course, they might be written as the *same* note-length notations as the earlier, shorter notes, but with a tempo change!

All of this judgment of tempo must be done in the face of the first problem, that the note lengths and inception times are not coming in precisely, but with considerable variation. Often, the amount of this variation may mask tempo or rhythmic changes. Consider, too, that the people who need the Composer's Aid most are those who may be least proficient at performing upon conventional instruments. The designer probably has a more difficult task to make the Composer's Aid accurately portray the muddled attempts at rhythmic regularity of a beginner, than to make it follow the (probably) more precise playing of a master.

Before leaving the subject of rhythm, I shall take the liberty to give the following advice to all would-be designers of automatic music-transcribing systems. First, build one that has but one key or button, and get it to determine rhythms correctly. By "correctly" I mean without unreasonable limitations. It should be able to handle any rhythm found in a Mozart or a Beatles' melodic line. If you cannot master that, then you certainly cannot transcribe more complex music, which might have a solo melody as a part of a piece.

The problems of rhythm are not

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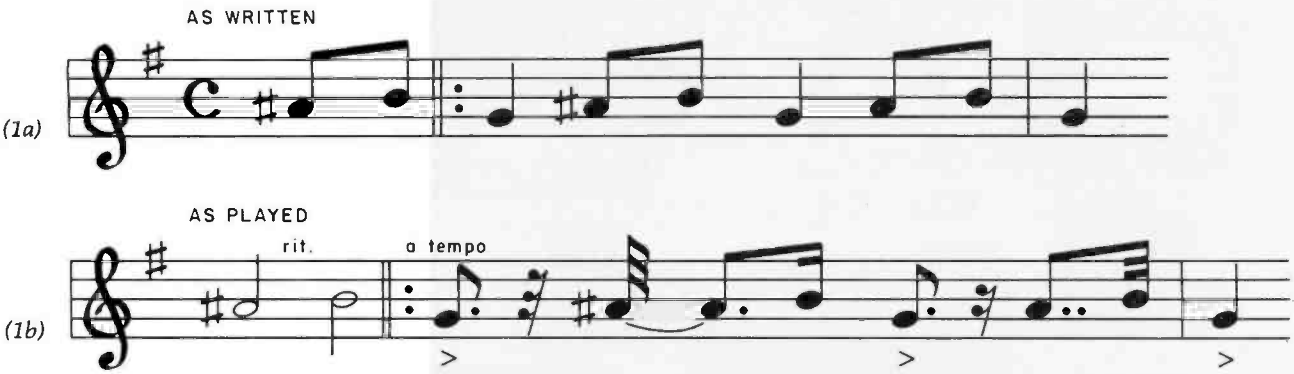
Figure 1: *The same passage as written (1a) and as performed (1b). Both examples here are from the "St Louis Blues."*

unexplored. Some of the algorithms that adaptively follow varying-rate Morse code may be useful. A number of moderately successful programs, all quite large and complex (using many techniques from artificial intelligence work, and *not* operating in real time), have been created. [*The October 1976 issue of BYTE contained several discussions of Morse-code decoding problems. . . .*RSS]

If you first succeed with rhythm, *then* you might have a chance at the rest of the problem. At least a good portion of the problem of transcribing a musical performance into a standard score will have been solved.

More and Less

It is clear that a performance of a piece often contains *more* information than is given in the score: things happen in the performance that are not specified in the written music. Jazz, usually played from sketchy "charts," is an especially good example. The lilting "dotted" rhythms of jazz are notated as equal notes on the page. But everyone "knows" how it should sound. Look at the example from W C Handy's "St Louis Blues" in figure 1.

It is clear that the performance in figure 1b is quite different from the written notation in figure 1a, as it must be in order to sound right. The figure shows just one possible way of singing the opening measure of the chorus to the "St Louis Blues" (and it is not an especially extreme example).

It is rare, if not unheard of, that two live performances are the same. Some of the changes are minor, such as changing two eighths to a dotted eighth and a sixteenth. More surprising is the modification of the opening two eighth notes into half notes (with a ritard, no less). But that is the way it is done.

Strangely enough, the same convention about playing eighth notes with a certain uneven lilt occurs in much baroque music, in spite of the fact that the notes were written down as being of equal length. Many performances of Bach's music, for example, are marred by a "wooden" playing of such passages.

Many conductors and performers play baroque music exactly as it is notated. It sounds as if you tried playing jazz or rock exactly as written in songbooks and sheet music: the result is dull music. This may help to account for some of the comments about baroque music sounding like a melodic sewing machine—some performers play it as though their in-

	INPUTS: Musical Idea	Score	Keypresses	Sound
OUTPUTS: Musical Idea	Inspiration	Plagiarization	Stimulation	Synthesized Music
Score	Composition	Arranging, Copying	Transcription	Taking Dictation
Keypresses	Improvisation	Performance	Coupling	Playing By Ear
Perceived Sound	"Science Fiction"	Automation	"Sonification"	Transmission

Table 1: *Musical transformations, representing the various ways of obtaining musical results. The table is read by starting at the top at a given input and proceeding downward and to the right to read the output. The shaded example illustrates that the term* performance *describes the connection between a printed score and the production of keypresses. (For simplicity's sake, the table deals only with keyboard instruments.) Similarly, to go from a musical idea (ie: input) to a score (ie: output) requires "composition." The term* coupling *refers to the mechanical addition of extra voices to an organ keyboard so that the organist can play more than one pipe with a single keystroke.* Automation *refers to the procedure by which mechanical musical instruments (such as music boxes and player pianos) take a score in machine-readable form and generate perceived sound. For want of a better word,* sonification *is used to describe the production of perceived sound from pressing a key on a keyboard. The terms in the row called "musical idea" are meant to be taken tongue-in-cheek.*

struments *were* sewing machines, without any regard for the original stylistic intent.

Problems Caused by Repeats and Larger Musical Structures

Here is another dilemma: how can a computer (or a human) tell if a section of a piece being performed has been repeated (perhaps with embellishments), or if it is a new section merely similar to the old one?

For example, in a Mozart rondo for the piano, almost all of the embellishments will be written out in full. In a Mozart sonata for the piano, there will usually be repeats marked and any variety will be at the performer's option. Does this mean that the computer must first be told the form of the piece before it can transcribe it? Knowing the form of a piece beforehand certainly aids a human transcriber.

Again, there is vague and general information that must somehow find its way into the program. As in having the computer play chess, methods have been found for translating an imprecise notion (eg: control the center of the board) into algorithms. Chess is a rich field, rife with human invention and complexity. Music is a more complex environment.

Problems With Notating Pitch

Having shown that there is information in a performance that is not to be found in the score (this is always the case), I would like to show that often there is information in the score that cannot be gleaned from the performance. The "spelling" of chords is one example. The two chords in figure 2 sound exactly the same on our equal-tempered organ. Nevertheless, they would be thought of differently by a musician playing them.

The notes of the two chords actually represent different pitches if sung or played on violins (or any instrument which allows the performer to vary pitch continuously rather than in discrete steps, as with an organ or piano).

The three sets of melodic notes in figures 3a thru 3c sound the same, and are all correctly but differently notated. Again, a human might guess which is the correct notation by means of global information, the musical context in which the passage occurs. In this example, the global information is the key of the piece and the customary clef of the instrument that is to play the tune. Is it reasonable to have the user predetermine the key for the computer? Or should the computer wait, as a human often must do, until the very end of the piece has been played before beginning to write it down?

Problems Transcribing Notes Sounded Simultaneously

On keyboard instruments such as the organ or piano, the performer can easily sound more than one note at any given instant. These notes may form a chord, or can be thought of as two or more melodies that are being played at the same time. In this latter case, each melody is called a *voice*. (This use of the word "voice" in music does not imply singing.) Multiple,

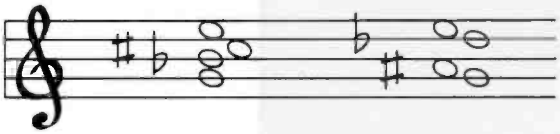

Figure 2: *Example of the equivalence of two musical notations. The chords notated here are played the same way on a keyboard instrument and sound the same, but they are written in different ways. This difference, however small, subtly influences the way many musicians interpret the chord.*

(3a)
(3b)
(3c)
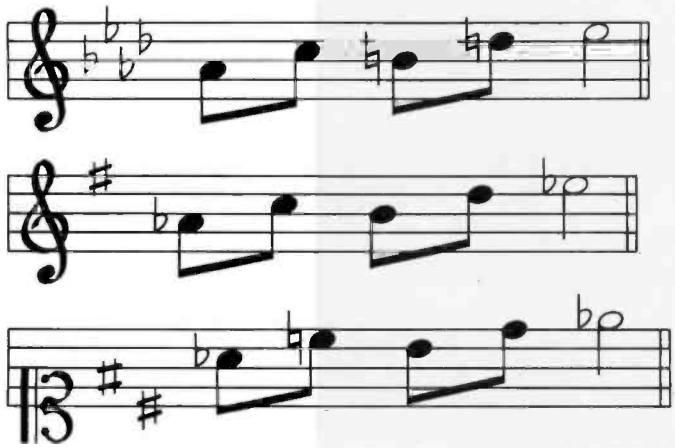
Figure 3: *Different notations for the same sounds. The three melodies here, when played, will sound exactly the same; the only difference is the choice of clef and accidentals. The first two melodies are written in the keys of A-flat Major and G Major in treble clef; the third melody is in the key of D Major in soprano clef.*

(4a)
(4b)

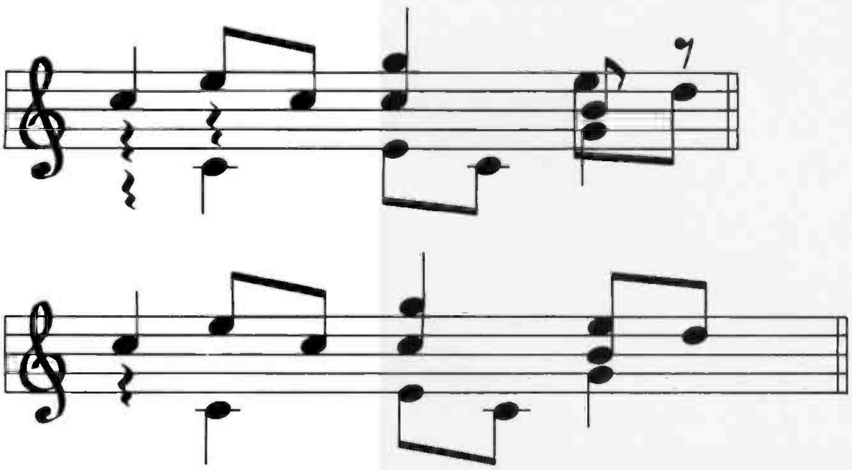

Figure 4: *A musical phrase played with two different voicings. These two phrases may sound the same, but the two correct, differing notations convey different meanings to a musician.*

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It is nearly impossible for even an expert musician to determine unambiguously, from listening alone, which note should be allocated to which voice. I realize that this portion of the discussion is delving heavily into the terminology of music, but the intricate details of music are what make this problem so fascinating. The two segments of music in figures 4a and 4b sound the same, and are both notated correctly. Nevertheless, the differences are significant and useful to the musician performing the music.

This is not the place to go further into the musical significance of these notational differences. Enough examples of problems have been amassed to give you a starting place at which to begin to think about having a computer "listen" to and "understand" music.

Problems in Determining Pitch With a Computer

If things were not difficult enough given direct input from a keyboard, many people (eg: ethnomusicologists) would love to be able to play a recording into a computer and produce a written score. So would I. However, two new problems are introduced. Finding what pitch is being played is not easy. To be sure, a simple sine wave could be digitized by a frequency counter. Unfortunately, real musical sounds are far more complex, often having harmonics and overtones that make almost any frequency-determining method unsure. And what do you do when a note slides from one frequency to another (*portamento* in musical jargon)? Or when a chorus finishes singing a chorale a semitone lower then when they started—will the computer notate it as a sudden modulation in the middle?

Even determining how long a note lasts is difficult. Try playing a piano note; strike a key and hold it down. How long does it last? Just when does its gradual dying away cease? In a quiet room, with a good piano, it may take several minutes. You might as well ask where the rainbow changes colors. Musical sounds often do not have well-defined edges with respect to time or pitch.

Summary

The point has been made, and it is possible to show many more examples than have been shown here that you cannot go from a performance to a score, or vice versa, in any easy fashion while preserving the qualities that make the notation of music readable to most musicians and the properties of a performance that make it worthwhile listening material.

A score is a highly idiomatic rendering of a piece of music, and a piece of music is a unique instance of the composition that the composer had in mind when the score was written.

These facts assure that the building of a perfect music transcriber is literally impossible. Whether it is possible to make the Composer's Aid good enough for most practical purposes remains to be seen. If we put low enough limits on the idea of "good enough," I am sure that it can be done quite easily. If it is to satisfy me (and musicians of like mind), it will probably not be easy at all.

A final suggestion: if you want to tackle any project of this sort, make sure that you know music well. Also make sure that you know your computing well or forge a partnership that can provide the needed experience. I have met many people who do not know the first thing about music trying to achieve difficult goals combining computers and music. I have also met musicians who imagined that they could get the computer to do some task that they found very easy—only to discover that they did not understand the difficulty of what they themselves could easily do.

The greatest benefit the computer confers upon mankind is that it forces us to truly understand what we are doing, for it is only through such understanding that we can instruct a computer. ■

Acknowledgments

I would like to thank the many people who have made useful suggestions about this article, and I would like to specially mention Doug Wyatt of the Xerox Palo Alto Research Center for many useful discussions about the nature of music, Brian Howard of Apple Computer Co for his excellent editing and criticisms, and both of them for the many hours of rehearsal, performance, and programming that they have shared with me.

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Comparing Floppy-Disk Drives by Software Simulation

Dennis Nendza
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Large companies learned long ago that preliminary performance specifications of systems can be predicted reasonably well by computer simulation. The National Aeronautics and Space Administration (NASA) saved much money and effort by simulating numerous systems that have been developed for the space program. In a somewhat smaller way, microcomputers can be used to simulate a variety of operational systems. Complex equations and analysis are not always required.

Here I shall present a practical simulation. I have chosen a topic of interest to myself and many small-computer enthusiasts: a comparison of the operating speeds of floppy-disk drives. This article will explain basic mechanical drive movements and illustrate the transformation of these physical events into the algorithmic steps of a computer program. Estimating one drive's performance in relation to others is the goal.

To do such a comparison, we need some knowledge of the operational parameters of floppy-disk drives. These parameters are the lengths of time required for a drive to perform a given function. All drives have at least these four parameters:

- head load
- seek
- rotational latency
- data-transfer rate

I shall look at each function in detail.

Head-Loading Motion

Before any data can be located or transferred on some drives, the data-transfer head must be *loaded*; firm contact between the head and the disk surface must be assured. To accomplish this, a pressure pad is placed against the disk on the side opposite the head. This pressure pad movement is referred to as *loading the head*. The length of time required to move the pad into place and insure that all mechanical bouncing has stopped is termed *head-load time*. Look at figure 1 to see a diagram of the head-load mechanism.

Track-Seeking Motion

Once the head is loaded, it may be necessary to move the head to a position over another data track on the disk. In most drives, the track-to-track movement, or *seeking*, is accomplished by a *stepper motor*. This motor rotates in steps of fixed, discrete increments; a specific interval of time is required for each incremental movement. Thus, to move the head across X tracks takes an amount of time equal to X intervals. Once we know the time interval required to perform a movement and the number of tracks to move across, we can predict how much time it will take the head to reach the desired track.

All stepper motors exhibit some vibration at the end of the last step in a given movement. There may be a settling time required before a read or write operation can begin.

Another type of motor is used in floppy-disk drives such as the PerSci Model 277. It is called a *linear motor* since it produces linear motion directly. The method is also called "voice-coil" positioning, due to the similarity to the action of a loudspeaker mechanism. Figure 2 depicts the stepper- and linear-motor positioning systems in simplified form.

The amount of time required per track for the linear motor to perform a seek operation varies according to the total number of tracks to be skipped. Unless the manufacturer supplies data describing the seek-time

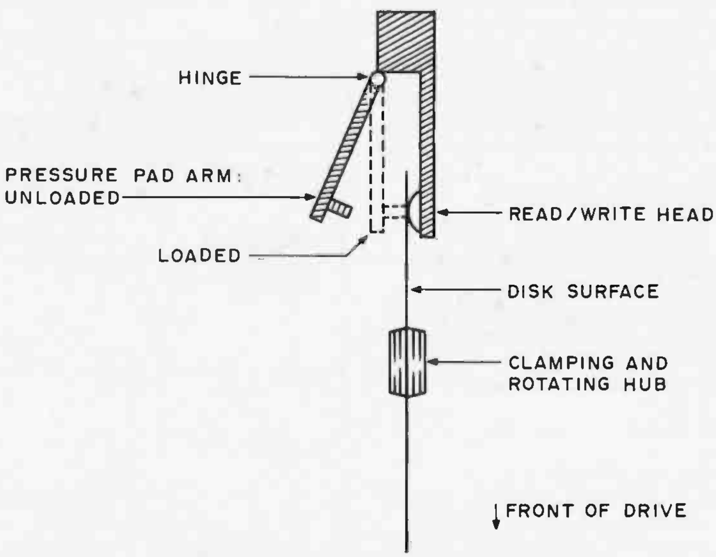

Figure 1: *Diagram showing a side view of the floppy disk loaded in the drive. When loaded, the read/write head is pressed against the surface of the disk by the pressure pad.*

About the Author

Dennis Nendza is 32 years old and is currently working as a computer systems consultant, after previous experience as a systems programmer, analyst, and data processing manager. He wrote his first computer program while in high school, using the ALGOL language.

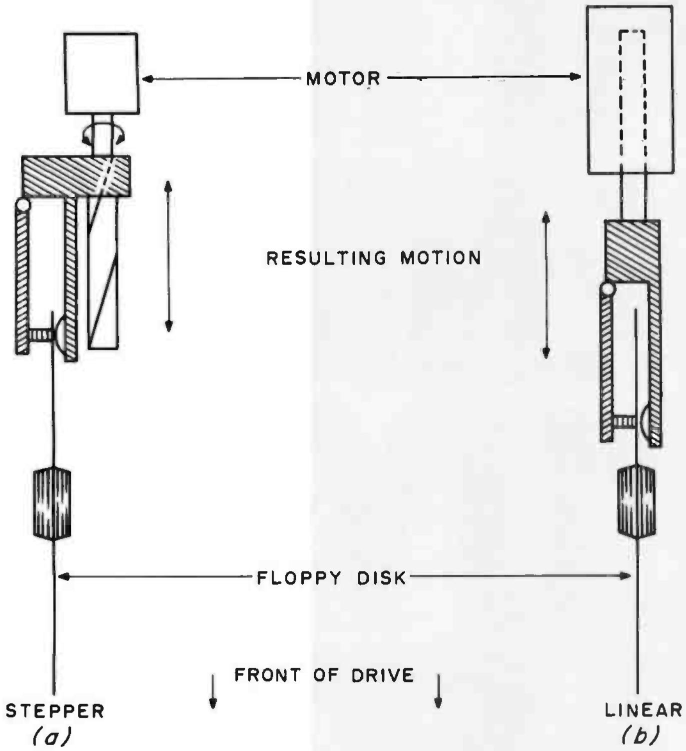

Figure 2: *Two methods of moving the read/write head from track to track across the disk. A stepper motor is shown as (a); a linear or "voice-coil" motor is shown as (b). The rotary motion of the stepper motor must be converted into linear motion by a gear arrangement.*

function, it must be derived from empirical measurements. This derivation, however, is not within the scope of this article.

Rotational Latency

Reading and writing operations are equivalent functions with respect to the actual time required for completion. With that in mind, the discussion will proceed as if a read operation is being executed. Assuming that the head is now loaded and positioned over the proper track, it remains for us to examine how long a delay may be expected in waiting for the desired record to spin past the head.

A look at figure 3 shows how most soft-sectored disk formats appear. Actually, the soft-sectored format contains 128 bytes of user data; the other data locations are used as address marks and gaps between certain fields. To determine the extent of the delay that must be endured before the desired sector is available, I will consider two cases.

The first case occurs when we begin a read operation and find the correct sector just about to pass by the head. In this event, there is no wait or *latency*, as it is called, before starting the transfer of data. The second case shows that the beginning of the desired sector just went by an instant before the read operation was started. We must now wait for one full rotation of the disk, or the *maximum rotational latency*, for the record to appear at the head again. These two extreme cases show that there are well-defined minimum and maximum rotational latencies. Of course, most delays will be at some random point within this range for actual read operations. The absolute delay for a single read operation is not predictable, but the average for a group of read operations is predictable within limits.

Data-Transfer Time

Finally, there is the most obvious function of the disk drive, data transfer. Data-transfer time is dependent on three basic parameters: disk rotational speed, data density, and format. The faster the disk surface spins past the head, the faster the

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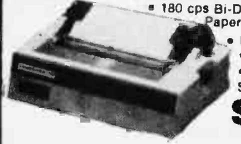

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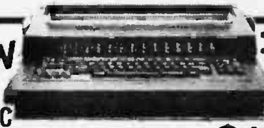

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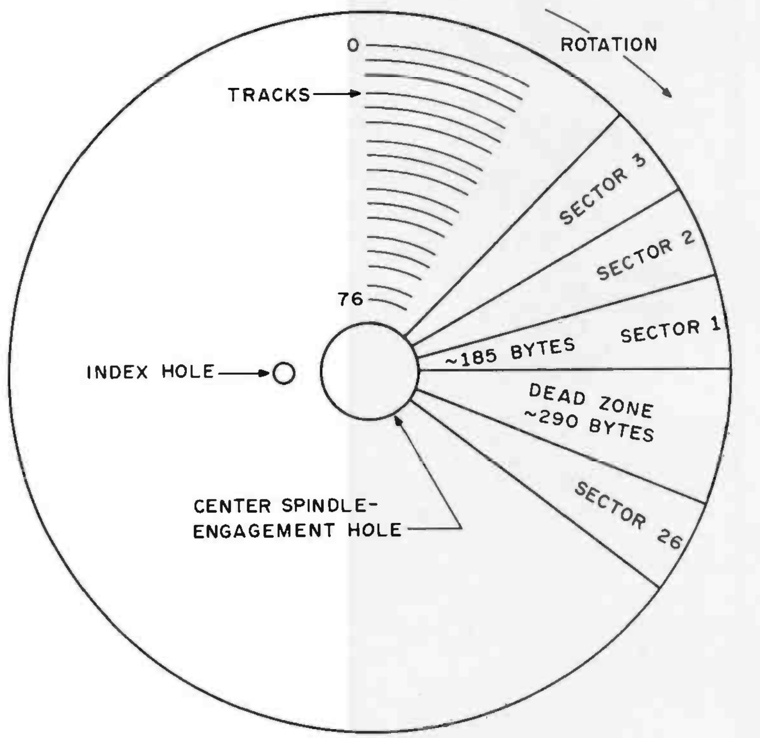

Figure 3: *Format of data storage on a soft-sectored, 8-inch floppy disk, viewed from the side that faces the pressure pad.*

head can read the data. (Large 8-inch disks spin faster than the smaller 5-inch disks.) The higher the density, the more data can be transferred in a given interval of time. Format differences can account for different effective transfer rates on large records, but will not be dealt with in this simulation. I will deal primarily with the standard IBM 3740 soft-sectored, 8-inch floppy-disk format.

Building the Simulation

We now have an understanding of what happens when a function of the floppy-disk drive is requested. We can now construct a program framework that will use this information. To read or write a record, we must pass through four distinct states: head-loading, track-seeking, rotational-latency waiting, and data-transferring. To compute the actual time required to pass through these states, we must get some information from the manufacturer's specifications for a given drive. Typically, the manufacturer will list the time for head load, track step, average latency, and sector transfer in milliseconds.

Head-load time calculation is easy. Each time that the head is loaded, a value corresponding to the head-load time is added to a total-time accumulator. As a matter of practice, most drives and control software leave the head loaded for a fixed-time interval following a disk operation. This reduces head-loading delays and acoustic noise, but it also increases disk surface wear slightly. For most programs (such as assemblers) that engage in almost continuous disk activity, the head will probably go through the load cycle only once during an execution of the program.

Computation of track-step time is not difficult in most cases. We merely figure the number of steps we must make from the current track to the desired track, and multiply that value by the specified track-step time. Do not forget to add the *settling* time, if the manufacturer gives it. (Remember that the settling time indicates the time taken by the head to stop vibrating from its track seeking and to start reading.)

Thus, for disk drives using stepper

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motors, the seek time is the absolute value of the distance from the current track to the desired track multiplied by the track-step time, all added to the settling time, or:

$$T_{seek} = ABS(P_{current} - P_{desired}) \times T_{step} + T_{settling}$$

where T is used for values of time, and P shows the position of the head in relation to data tracks on the disk.

But what should be done when the disk drive uses the linear-type motors to move the head from track to track? The specification sheets for the PerSci unit give only a single-track seek time of 10 ms. Is that the same as the stepper-motor drive timing? No—this timing is for a single-track step, and there is no settling time to be added. In fact, if the two-track seek time is measured, it is one and one-half times the single-track seek time. If a ten-track seek is measured, we find that it takes only three times as long as moving the head a distance of one track.

Well then, what can be done about this device? For this simulation, my plan of attack was direct. I merely measured the time that it took for all possible seek distances (seventy-six values) and then computed an approximating function by using a least-squares polynomial curve-fit calculation. The concepts behind this computation are not simple. Fortunately, the routine is adaptable from a book that addresses such problems, *Data Reduction and Error Analysis for the Physical Sciences* by Philip R Bevington (McGraw-Hill Book Company Inc, 1969).

When the seek time for the PerSci drive is needed in my simulation, the number of tracks the head crosses is evaluated and is given as an argument to the empirically derived seek-time function. The result of the function evaluation is the number of milliseconds required to complete the seek. Thus, the PerSci drive becomes a special case in the simulation, but handling it is not so awkward.

To compute the rotational latency, one of two possible techniques is employed. For any large number of discrete read operations, the actual, average rotational latency experienced will approach one-half of the maximum latency. This value can be used for each read operation as a typical latency. I prefer to calculate a random latency for each read operation. Approximately the same results will appear as in the first method for a large sampling of read operations. You will notice that the results from using random latency values are not likely to be the same each time the program is executed. This is due to the accumulation of random variability, which is an effect you would see if the simulation were carried out on real hardware as well as in a program. The function for randomly determining a latency time is simply: the value of the maximum latency multiplied by a random number between 0 and 1.

The final item which must be dealt with is the actual time it takes the drive to transfer the data to (or from) the disk. The time to transfer 128 bytes of data has been chosen for this simulation. The time values for each drive in this simulation were calculated based on the rotational speed and data density. Record overhead bytes and interrecord gaps were not considered. In the simulation program, the computed values are reflected in the appropriate field in DATA statements that describe the characteristics of each drive. Transfer time for *n* bytes is calculated by multiplying *n* by 8, and then dividing by the *transfer rate*, in bits per second.

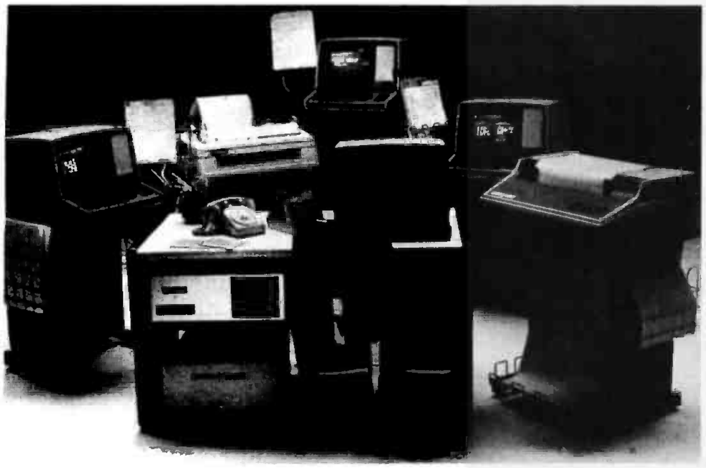
About the Simulation Program

Now that we understand the basic drive mechanics, there should be no difficulty in comprehending how the simulation works. The program performs two simulations for each disk drive under consideration.

The first simulation is a set of 500 sequential-read operations, as you would find in a sequential file-copy operation. The second simulation involves a random reading of 500 records, as you might encounter in a program that reorganizes an indexed file according to an unordered secondary key field.

These two modes of access will exhibit the characteristics of general interest concerning floppy-disk drive performance. Briefly, the program steps through the DATA statements that supply the drive name and parameters for that drive. Both simulations are run for a given drive,

Large System *Performance* / Small System *Price*



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†††Using 56K RAM per user may involve "wasting" or turning off as much as 8K RAM per user. The present maximum number of 56K RAM users is four. As many as seven 48K users can presently be supported.

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and the results are printed. Look at the program shown in listing 1 to see the simple logic and computations.

Results and Notes

If this simulation were run using a true random-number generator, you would find that the resulting timings will vary on each run. As noted earlier, this is random variation that is to be expected. Do not expect to see exactly the same results as printed here; the values *will* be within a few percent on all runs.

Referring to the simulation output shown in listing 2, observe that, on sequential-read operations, the transfer times for the 5-inch floppy-disk drives are about 25% slower than the times for the standard size (ie: 8-inch) drives. Allowing for random variation, this is very close to the 20% speed difference that might be predicted based on the different rotational rates of the two sizes of floppy disks. The 8-inch disk drives also outperform the 5-inch drives during random-access operations. Most, but not all, of the smaller drives are slower in seeking from track to track, and this really shows during random access.

The fastest-seeking drive of the group, the PerSci Model 277, does not get a chance to show off while reading sequentially, but its capability becomes apparent during random-access operation. This device really moves the head fast! The second and third places go to the Memorex Models 552 and 550 respectively; these use fast stepper-motor drives.

Now that you have read this far, I can reveal some bad news concerning this simulation. The timings obtained are not likely to be a true indication of how long it would take to actually perform these operations on a running computer system. Accomplishing so realistic a simulation involves additional simulation of the interface

Listing 1: *Program to simulate mechanical characteristics of various 8-inch and 5-inch floppy-disk drives, written in BASIC-E and running under the CP/M operating system. One step is the simulation of 500 sequential-read operations; the other is the simulation of 500 random-access read operations. Due to the use of random numbers, some variation of results is expected between different executions of this program.*

```
REM   PROGRAM TO COMPARE ACCESS TIMES OF VARIOUS FLOPPY-DISK DRIVES FOR
REM   SIMULATED SEQUENTIAL AND RANDOM READING.
REM
REM   THE FIRST TEST IS FOR 500 SEQUENTIAL READS, 128 BYTES PER READ.
REM   STARTING TRACK IS 0. THE HEAD IS LOADED AND REMAINS LOADED.
REM   WHERE A DRIVE HAS SECTORS GREATER THAN 128 BYTES, THE SECTOR TRANSFER
REM   RATE HAS BEEN ADJUSTED IN THE DATA FOR THAT DRIVE.
REM
REM   ALL TIMES ARE IN MILLISECONDS.
REM
READ DRIVES                           REM GET NUMBER OF DRIVES TO SIMULATE
INPUT "ENTER ANYTHING TO SEED THE RANDOM-NUMBER GENERATOR";A$
PRINT : PRINT : PRINT                 REM UPSPACE A FEW LINES
PRINT TAB(30); "FOR 500 READ OPERATIONS"
PRINT TAB(25); "DRIVE SPEED COMPARISON SIMULATION"
PRINT TAB(30); "ALL TIMES IN MILLISECONDS"
PRINT
PRINT "DRIVE NAME"; TAB(25);"SEQUENTIAL";TAB(40);"RANDOM"
PRINT TAB(25);"------------- + -------"
PRINT
RANDOMIZE                             REM SHAKE UP RANDOM-NUMBER GENERATOR
FOR D=1 TO DRIVES
    READ DNAME$,TTRK,TSETL,HLOAD,LATENCY,SECREAD,NSECS,NTRKS
    CURTRACK=0                        REM STARTING TRACK
    TOTALTIME=0                       REM SET TIME ACCUMULATOR TO 0
    REM LOAD THE HEAD ONCE FOR THIS SEQUENTIAL TEST
    GOSUB 1000                        REM GO ACCUMULATE HEAD-LOAD TIME
  FOR I=1 TO 500                      REM 500 SEQUENTIAL READS LOOP
    GOSUB 2000                        REM STEP TO NEXT TRACK IF NEEDED. ACCUMULATE TIME
    GOSUB 3000                        REM READ NEXT RECORD. ACCUMULATE TIME
  NEXT I
  REM   PRINT RESULTS FOR TEST 1
  PRINT DNAME$;TAB(28);INT(TOTALTIME*10)/10;TAB(40);
  REM   NOW FOR 500 RANDOM READS IN A FILE 35 TRACKS LONG
  TOTALTIME=0                         REM SET TIME ACCUMULATOR TO 0
  LOWTRACK=0                          REM LOWER FILE TRACK LIMIT
  HIGHTRACK=34                        REM UPPER FILE TRACK LIMIT
  CURTRK=0                            REM START AT TRACK 0
  FOR I=1 TO 500                      REM 500 RANDOM READS LOOP
    NEXTRK=LOWTRACK+INT(RND*35)                REM NEXT RANDOM TRACK
    TRACKSTOMOVE=ABS(CURTRK-NEXTRK)            REM NUMBER OF TRACKS TO TRAVERSE
    GOSUB 2500                        REM COMPUTE TIME TO DO SEEK. ACCUMULATE IT
    GOSUB 3000                        REM COMPUTE RECORD READ TIME. ACCUMULATE IT
    CURTRK=NEXTRK                     REM NEXT TRACK HAS BECOME THE CURRENT TRACK
  NEXT I
  PRINT INT(TOTALTIME*10)/10          REM PRINT RANDOM READ RESULTS
NEXT D
STOP
REM   SUBROUTINES FOLLOW
1000 REM ACCUMULATE HEAD-LOAD TIME
```

Listing 1 continued on page 140

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These programs, unless otherwise indicated, are for the 16k, Level II TRS-80.

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SYSTEM SAVERS

by Tom Stibolt from Acorn

If you ever use the SYSTEM command, you should buy this two program package. These programs allow you to save any system format tape on tape or disk, plus offer several features for machine language programmers. Many two part, protected system tapes like Sargon II are not system format.

With FLEXL, which is one of the two programs, you can make back-up copies of any system format tape. Most often a cassette that you make will load easier than an original. Plus you can find the filename on any system tape because it is displayed on the screen. And at any time you can stop the reading of the tape by pressing <BREAK>.

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And as a FREE BONUS, Acorn provides instructions on how to load MicroChess 1.5 onto disk.

Complete your system with the routines not found in either Level II or DOS for only $14.95. Order your System Savers, today!

TRS-80 DISK & OTHER MYSTERIES

by H.C. Pennington

We don't usually list books, but this one is so unique that we thought you would want to know about it. There are over 100 pages about how DOS works, how a disk is organized, and how to recover from errors. This is THE technical backup for NEWDOS+ with great illustrations. $22.50.

DISK*MOD

by Roy Soltoff from Misosys

This machine language program modifies your copy of the Radio Shack Editor/Assembler for use with your minidisk and any disk operating system. You can save and load both text source and assembled object files. Unlike the NEWDOS+ version you can read the directory and the allocation of granules while in the EDTASM. You can also kill files. It is a complete disk modification for one or more drives.

Other capabilities are also added which are not found on NEWDOS+. The block move command relocates a section of text to any other area. The global change command permits, for example, changing a label throughout the text. The pagination feature provides hardcopy on 8 1/2 by 11 pages on either single sheets or continous paper. In addition, high memory can be reserved, like in BASIC, for machine language routines like printer drivers. You can also display the amount of memory remaining.

The <CLEAR> key is functional, the symbol table is sorted alphanumerically and output 5-across, the scroll up/down allows 15 lines on the screen, and the 'DEFM' assembly is improved. Lower case input is now permitted and you can branch to any address. Plus, it also corrects the errors in the Radio Shack tape version. $19.95

Also available for $239.95 for the TRS-80 Model II is a similar Editor Assembler from Galactic Software. Write for a complete list of Model II software.

DISASSEMBLER

by Roy Soltoff from Misosys & Acorn

This two-pass Z-80 disassembler produces symbolic labels with output to either the video monitor, printer or tape. Radio Shack's Editor / Assembler can load the tapes. If you own the Editor/Assembler, complete the package with this program. Program on tape for two different memory locations.

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Listing 1 continued:

```
  TOTALTIME = TOTALTIME + HLOAD
  RETURN
2000 REM COMPUTE SEQUENTIAL TRACK READ-SEEK TIME
  IF I/NSECS NE INT(I/NSECS) THEN RETURN      REM NO TRACK ADVANCE
2500 IF TTRK = 0 THEN 2800                     REM USE SPECIAL PERSCI FUNCTION
  SEEKTIME = TRACKSTOMOVE*TTRK + TSETL         REM COMPUTED SEEK TIME
2600 TOTALTIME = TOTALTIME + SEEKTIME
  RETURN
2800 REM PERSCI-277 DERIVED SEEK TIME FUNCTION
  IF TRACKSTOMOVE = 0 THEN :                   REM NO MOVEMENT REQUIRED
    SEEKTIME = 0:                              REM THEREFORE SEEKTIME IS ZERO
    RETURN
  X = TRACKSTOMOVE
  SEEKTIME = 10.89605 + 2.178647*X - 4.846975E - 2*X*X + 7.936448E - 4*X*X*X - 4.406022E - 6*X*X*X*X
  GOTO 2600
3000 REM COMPUTE RECORD READTIME INCLUDING ROTATIONAL LATENCY
  RNDLATENCY = INT(RND*LATENCY)                REM RANDOM ROTATIONAL LATENCY
  TOTALTIME = TOTALTIME + RNDLATENCY + SECREAD  REM ACCUMULATE READ TIME
  RETURN
REM   FIELD ORDER IN DATA STATEMENTS
REM   DRIVE NAME, TRACK-TO-TRACK TIME, SETTLING TIME, HEAD-LOAD TIME,
REM   MAX LATENCY, TRANSFER TIME, SECTORS PER TRACK, TRACKS PER DISK
DATA 12                                        REM NUMBER OF DRIVES TO SIMULATE
DATA "PERSCI 277",0,0,40,166.7,4.096,26,77
DATA "REMEX RFD 1000A/B",6,24,50,166.7,4.096,26,77
DATA "SHUGART SA800",8,8,35,166.7,4.096,26,77
DATA "SHUGART SA400 MINI",40,10,75,200,8.192,18,35
DATA "SHUGART SA450 MINI",25,15,50,200,4.096,18,35
DATA "PERTEC FD200 MINI",25,10,35,200,8.192,16,35
DATA "ICOM FD3800 DUAL-DENSITY",10,0,40,166.7,2.048,26,77
DATA "ICOM MICROFLOPPY",40,10,75,200,8.192,16,35
DATA "MEMOREX 550",6,10,35,166.7,26,77
DATA "MEMOREX 552",3,15,35,166.7,26,77
DATA "MICRO PERIPHERALS B51 MICROFLOPPY",5,15,35,200,8.192,16,40
DATA "ALTAIR 88-DCDD",10,10,45,166.7,4.096,32,77
END
```

and software delay characteristics. However, the relative standing of the drives is unlikely to change if these factors are included.

The important elements to consider for additional simulation are: the record formats on the disk, the interface and controller characteristics, processor speed, and the algorithm of the program performing the access.

As an example of the discrepancy between the simulation and the speed of the total system, I offer the following. My system uses a Z80 microprocessor running at a 2 MHz clock rate, and contains 24 K bytes of zero-wait-state memory. The drive controller, designed by George Morrow, connects to a PerSci Model 277 with the fast-seek option. The operating system is CP/M. The time to read 500 records sequentially using BASIC-E is 109 seconds; to read 500 records randomly takes 525 seconds. Compare these times with those in the results of the simulation for the PerSci drive. Beware of making system estimates based only on a part of the total operation. Does anyone want to write an article that describes operating-system timing simulation?

Listing 2: *Output of simulation results produced by the program of listing 1.*

FOR 500 READ OPERATIONS
DRIVE SPEED COMPARISON SIMULATION
ALL TIMES IN MILLISECONDS

DRIVE NAME	SEQUENTIAL	RANDOM
PERSCI 277	43107.6	57912.2
REMEX RFD1000A/B	43650.1	92281.9
SHUGART SA800	44163.1	94881.9
SHUGART SA400 MINI	53547.8	288397.1
SHUGART SA450 MINI	55153.2	198631.3
PERTEC FD200 MINI	52804.8	201703.6
ICOM FD3800 DUAL-DENSITY	43110.0	101456.6
ICOM MICROFLOPPY	55698.8	293376.0
MEMOREX 550	44821.1	77892.1
MEMOREX 552	44000.1	66670.3
MICRO PERIPHERALS B51 MICROFLOPPY	55287.8	89390.2
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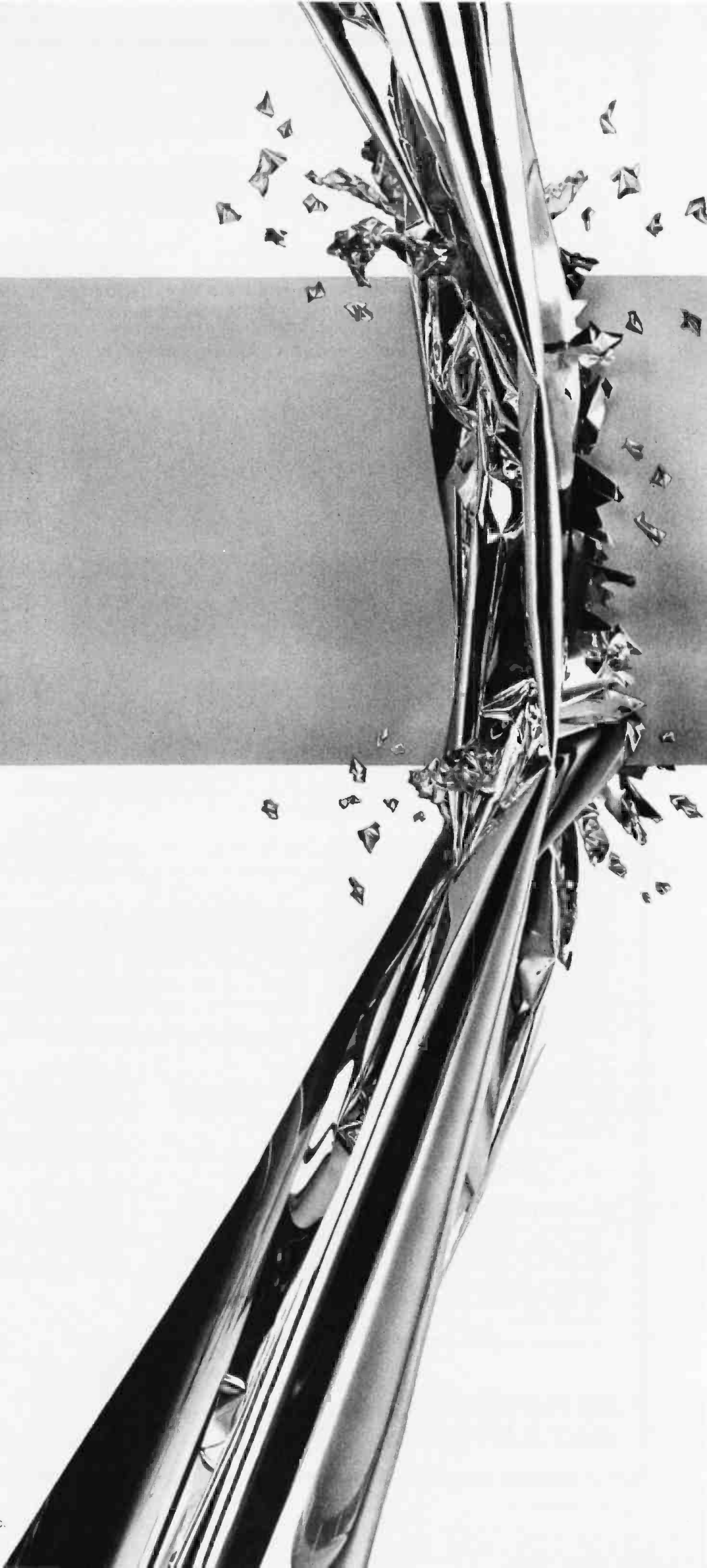
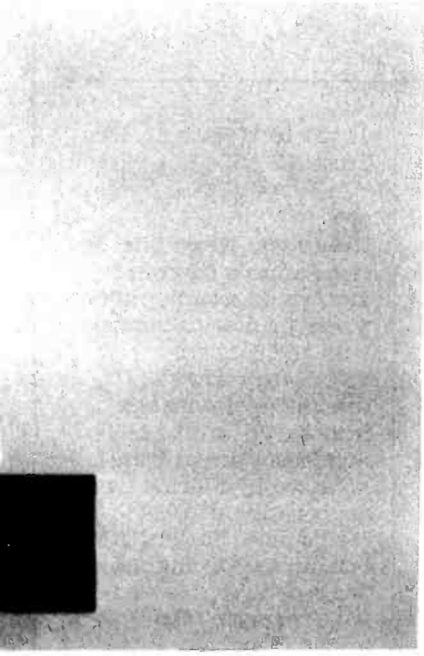
Two for One

There are two basic lessons to be learned from this exercise. The first one concerns an elementary introduction to the motions that occur in floppy-disk drives and affect their speed of operation. The second lesson concerns derivation of mathematical functions that describe these mechanical motions; it also concerns putting the functions into a program for the purpose of obtaining an estimate of performance. Performance, for the purpose of this article, considers only the relative speed of operation of the various drives. In making a decision to select a particular floppy-disk drive, you must understand that overall performance, not just speed of operation, should be examined. ■





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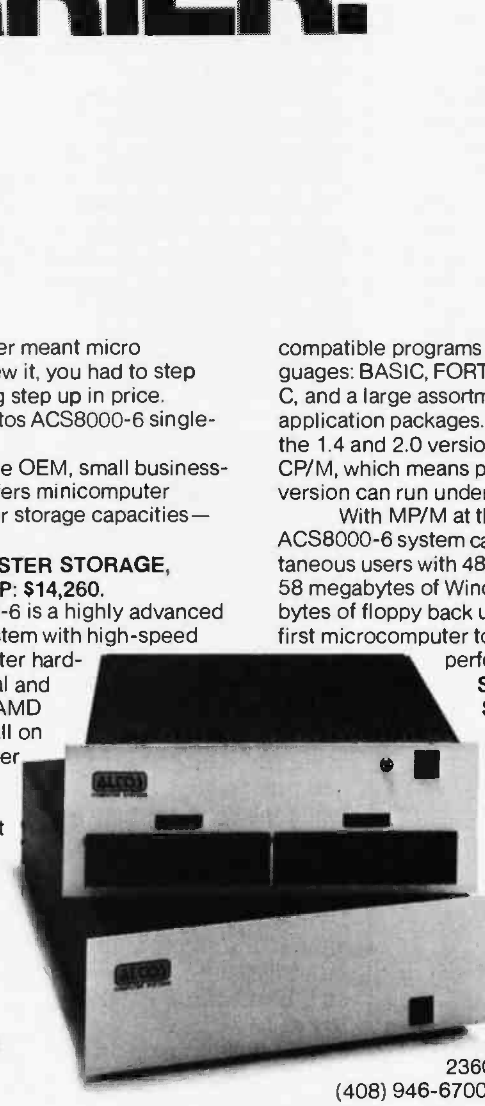

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BYTELINES

NEWS AND SPECULATION ABOUT PERSONAL COMPUTING

Conducted by Sol Libes

What To Look For At NCC: The computer show of the year is the National Computer Conference (NCC), which will be held this month (May 19 thru 22) at the Anaheim Convention Center in Anaheim, California. In 1979, 60,000 people attended the NCC. Many new products are introduced each year at NCC. The 1980 show will see many more Japanese manufacturers displaying, among other things, 8-inch Winchester disk drives and microcomputer systems. Furthermore, look for several manufacturers from the United States to show complete microcomputer systems that use the Zilog Z8000 and Motorola 68000 16-bit microprocessors. Last year's show saw the introduction of 8086-based microcomputers. Also, look for disk-operating-system-based languages and applications packages for these new 16-bit microcomputer systems. Several multiprocessing and multiuser microcomputer systems will also be shown.

John Mauchly, Computer Pioneer, Dies: Dr John W Mauchly, coinventor of the digital computer, died on January 8, 1980 at the age of 72. Together with his colleague Dr J Presper Eckert, Dr Mauchly conceived, designed, and built ENIAC, the first electronic digital computer. It was built at the University of Pennsylvania and became operational in 1944. ENIAC contained thousands of vacuum tubes, filled 150,000 square feet of space, and weighed 30 tons. It was used for ten years.

Mauchly and Eckert later formed the Electronic Control Company (later called the Eckert-Mauchly Computer Corporation) to manufacture BINAC (Binary Automatic Computer), which became the prototype for the UNIVAC I (Universal Automatic Computer). The UNIVAC I was the first commercial computer; it was installed at the United States Census Bureau in 1951.

When the company was purchased by Remington-Rand in 1950, Dr Mauchly continued with the Univac Division as Director of Applications and worked on weather-forecasting projects. In 1959 he left to form Mauchly Associates, a consulting firm that developed the critical-path method for construction.

In 1967 he founded Dynatrend, a computer consulting firm, and since 1973 he had served as a consultant to Sperry Univac.

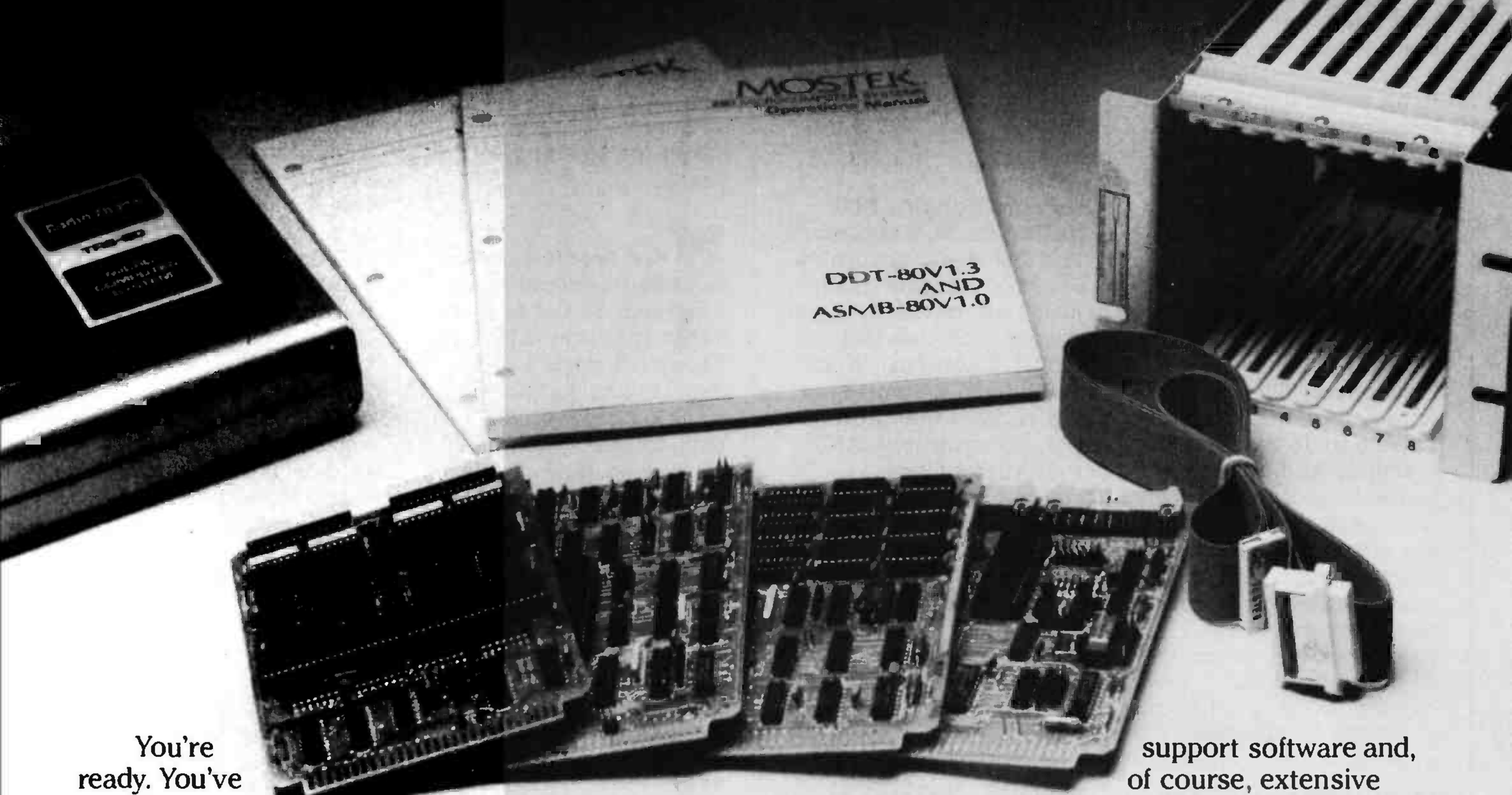
Mauchly and Eckert met in 1941 at the University of Pennsylvania's Moore School of Electrical Engineering, where both were instructors. They first proposed the building of the digital computer to the US Army in 1942 for calculating trajectory tables. ENIAC contained ten accumulators, had internal memory, used subroutines, and was all-electronic, while prior machines were electromechanical and very limited in power. Some parts of ENIAC can be seen at the Smithsonian Institution in Washington, DC.

At the time of his death Dr Mauchly was believed to be working on a word-processor project using a Radio Shack computer. He was an active proponent of personal computing, and he will be missed by many.

News Bits: Friends Amis has developed an interface for the Craig M-100 hand-held language translator that allows the user to add read-only memories containing data bases such as wine lists, Olympic scores, history, or metric conversion.... Panasonic will introduce a hand-held computer to sell for about $180 in late 1980. The RLT500 Electronic Data Center can be connected to a television set for display, to an acoustic modem for communication, to a printer for hard copy, or to a speech synthesizer for audible output. Quasar will bring out the HC2000RA Information Processor for $150, which should work with the accessories for the Panasonic machine.... Amateur robot builders have a new source for parts: Vedos Ltd, Suite 1113, 19 W 34th St, New York NY 10001.

Random News Bits: In last month's column I mentioned a rumor about a new printer to compete with the Sanders Technology word-processing dot-matrix printer. The unit has now been formally announced by Florida Data Corporation of West Melbourne, Florida. It offers up to 900 characters per second (cps) speed with correspondence-quality type and high-resolution graphics (at a slower speed). It is said to use a magnetic stored-energy print head, and to offer an almost unlimited choice of type fonts, full graphics, and extended-character format. The machine will be available in the fourth quarter of 1980, and it should be priced under $2000.... Micro Peripherals Incorporated of Salt Lake City, Utah, plans an under-$1000 word-processing printer using a seventeen-wire matrix head and printing at 60 to 75 cps.... In the meantime Diablo, Qume, and Nippon Electric Company (NEC) are rumored to be developing under-$1000 daisy-wheel printers.... Dataproducts will soon introduce a daisy-wheel printer; some observers speculate that it will sell for 20 to 30% less than current daisy-wheel units.... Next year, General Motors (GM) will make much use of on-board microcomputer systems in its vehicles to

Put your applications to work on the Mostek STD-Z80 BUS.



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meet the stringent requirements for emissions control and fuel economy. GM's need for electronic parts will be so great that the company will use 56% of the world's supply of 8 K-byte read-only memories and 40% of the analog-to-digital converters, according to a GM estimate. In all, GM will buy 13 to 15 million electronic parts each day, more than 3 billion parts per year.... Chase Manhattan Bank is developing the Personal Computer Bank Communications System. Any bank customer who has a home terminal or computer system will be able to access (via telephone) his or her account, get an up-to-the-second status report, and cause funds to be transferred. The user with a computer will also be able to do batch-mode transfers and off-line processing of bank account data.... The precursor of flat solid-state data displays may have appeared. Crokroft International of Sunnyvale, California, has introduced a liquid-crystal display (LCD) panel with 32-by-32-dot display. It operates about four times faster than current LCD displays. The company also expects to have a variable-color display in the near future.... For the first time, a microcomputer-software package has been placed on the prestigious Datamation magazine Honor Roll of Software Packages. Naturally, the software package was the CP/M operating system, a product of Digital Research. Microsoft BASIC and UCSD Pascal received honorable mention.... A report from International Resource Development, a management consulting firm, predicts that four billion dollars will have been spent on electronic-mail services and equipment by 1990. The field will be dominated by IBM, AT&T, and GT&E, with the US Postal Service getting about one quarter of the business.... A new supercomputer project has been started. Denelcor of Denver, Colorado, is planning to manufacture a computer that uses 50 processors, capable of performing 500 million instructions per second in parallel.... Texas Instruments and Hitachi are developing 64 K-bit programmable memories, which should become available next year....

Court Upholds FCC Ruling On TI Modulator: The District of Columbia Court of Appeals has rejected an appeal by Atari Corporation (see last month's column). Atari challenged the ruling of the Federal Communication Commission (FCC) that allows Texas Instruments (TI) to sell its stand-alone radio-frequency (RF) modulator while the FCC reexamines its own guidelines for electronic television accessories. Atari argued that the FCC should have forced Texas Instruments to abide by the present rules until changes became final. The present regulations prohibit the marketing of stand-alone modulators. Texas Instruments uses these modulators with its Model 99/4 personal computer system.

Radio Shack And Apple Ask FCC For Deadline Extensions: Tandy Corporation (parent company of Radio Shack) and Apple Computer Company have filed separate petitions with the FCC, asking that the FCC's July 1, 1980 deadline for compliance with new radiation standards be extended. They feel that there could be an adverse effect on products still in dealer stocks, which could take 6 to 9 months to sell. All units manufactured after July 1 will have to comply with the standards. General Electric, General Telephone and Electronic (GT&E) Services Corporation, Honeywell, Control Data Corporation, Atari, American Telephone and Telegraph (AT&T), the Computer and Business Equipment Manufacturers Association (CBEMA), and Electronic Industries Association (EIA) have also filed petitions. Most of these petitioners asked for a 2-year extension, while some asked for as many as 7 years.

Word-Processing Standard In Development: An American National Standards Institute (ANSI) Group (number 4 of X4A12) has completed a working draft of the page-image format of a word-processor standard. The purpose is to facilitate communications between word processors from different vendors in a common language. The present draft is considered only a first step; the first part of the standard is expected to be adopted by midyear.

Microprocessor Technology Seen Affecting Employment: A report presented at a recent conference of the Organization for Economic Cooperation and Development (OECD) in Paris, France, cited an impact on employment in Japan by microcomputers. The report was prepared by a special committee organized by the Japan Information Processing Development Center and sponsored by the Ministry of International Trade and Industry.

The report forecasts substantial job layoffs due to labor-saving microcomputer-controlled equipment. The biggest effect will be felt in assembly manufacturing where automation will substantially reduce the number of unskilled workers on the assembly line. On the other hand, the report predicted an increased need for systems and software personnel.

Microcomputer Lip-Reader For Deaf: The Research Triangle Institute in North Carolina, working with funds from the National Aeronautics and Space Administration (NASA) and the Veterans Administration, is developing a microprocessor-based system to help the deaf read lips. The device, called Autocuer, can increase a trained lip-reader's comprehension from the typical 25% to about 90%. A light-emitting diode (LED) display projects representations of sounds as nine simple patterns corresponding to the sound.

Commodore Introduces New 4-bit Microprocessor: While other semiconductor makers are going to larger microprocessors (typically 16-bit or enhanced 8-bit devices) Commodore has decided to go in the other direction. Chuck Peddle, the wizard who created the 6502 microprocessor (used in the PET, Apple, Ohio Scientific, Atari, and other computers) and who also created the KIM-1 and PET computers, has now turned his efforts to designing a "super" 4-bit microprocessor called the MCS4500. Using complementary metal-oxide semiconductor (CMOS) technology, it has thirty-four instructions, onboard memory (including 2 K bytes of read-only memory and 176 nybbles of scratch-pad memory), and can directly drive up to four multiplexed liquid-crystal displays (LCDs). Memory can be expanded, and many of

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the features found on 8-bit processors are included. Commodore will offer an assembler and emulator for the device that runs on a PET microcomputer.

IEEE Developing Assembly-Language Standard For Microcomputers: The Institute of Electrical and Electronics Engineers (IEEE) is developing a standard for assembly language on microprocessors (IEEE Task P694/D11). It is long overdue and will be of enormous value to all assembly-language programmers who are struggling to write code for different microprocessors. The group working on the standard has done some genuinely worthwhile things, such as demonstrating that all the current major microprocessors can be handled by a single standard.

The problems of present inconsistency are incredible. For example, in assembly code for some processors, MOV A,B means "move the contents of register B to A," while for others it means just the opposite.

The new IEEE standard should cure problems such as those that occurred when Zilog did not use the Intel mnemonics for the Z80's instructions, which are a superset of the 8080's instructions (probably because Intel copyrighted the mnemonics).

The standard also covers instruction names, address modes, operand sequences, expression evaluation, constants, labels, comments,and assembler directives. The standard does not specify the syntax necessary to support macroinstructions or conditional assembly.

The IEEE Computer Society is to be congratulated for its activities in developing computer standards, which are overcoming problems created by companies that all too often intentionally create incompatibilities to protect their competitive position.

I predict that this assembly-language standard will meet with the wide adoption that the other IEEE standards (such as the IEEE-488 interface and IEEE S-100 bus standards) have met. You can obtain a copy of the Assembly Language Standard draft by sending a self-addressed 10 by 13 inch (25.4 by 33 cm) envelope with $0.54 US postage affixed to Dr Robert G Stewart, Chairman of Computer Standards Committee, IEEE Computer Society, 1658 Belvoir Dr, Los Altos CA 94022.

Incidentally, the IEEE is also working on several other standards relevant to the microcomputer area. These projects are: Multibus, Microbus, Futurebus, Floating Point, High-Level Languages, Pascal and Relocatable Object Format. I will try to report on IEEE's progress in a future BYTELINES column.

Telecomputing Companies Off To A Good Start: The Source, a telecomputing service provided by Telecomputing Corporation of America (or TCA, headquartered in McLean, Virginia), is just six months old. The Source has 3000 subscribers and is adding 500 more per week. The company, which provides information retrieval and software services via a telephone network, has grown to thirty-five employees and a monthly revenue of $100,000. TCA is aiming to have 100,000 customers by the end of 1980.

A competing service called MicroNet, provided by CompuServe Incorporated of Columbus, Ohio, is aimed more at the hobbyist. They claim to have 1200 customers already. However, there is a dark cloud on the horizon, in the form of the Teletext and Viewdata systems now being tested by GT&E, Texas Instruments, and others. This may provide much lower cost but less flexible data access to the home television screen.

Flat CRT Unveiled At CES: Sinclair Radionics demonstrated a prototype of their flat-screen cathode-ray tube (CRT) at the Consumer Electronics Show (CES) held in January. Sinclair hopes to use it in a $125 television receiver to be available in late 1981. The electron gun is mounted sideways, with the beam deflected to strike the phosphor-coated screen. The image is brighter than images on conventional CRTs. The entire receiver will measure 2.5 by 10.2 by 12.7 cm (1 by 4 by 5 inches). The company is doing additional research to develop large-screen and color flat CRTs.

Random Rumors: Centronics, the largest supplier of printers today, will soon cut prices 20 to 30% on existing low-cost printers and will unveil new products directed specifically at the personal computer market, including both impact and nonimpact serial matrix units.... Dataproducts, Okidata, and a number of Japanese manufacturers including NEC are rumored working on multipass, high-density, dot-matrix printers to compete with the RC Sanders Technology Systems Media 12/7 printer. However, at present Sanders Technology has about a 2-year lead time on this technology.... Radio Shack might introduce more than one new personal computer system in the late fall (see the February 1980 column for previous rumors).... Reports have been circulating that Data General is developing a desk-top computer, code-named Wing. It will use a microprocessor, have two floppy-disk drives, and will be made in Taiwan.... It is rumored that Toshiba Electric Company is working on an experimental voice-input typewriter. The unit will be able to type 100,000 to 200,000 different words in Japanese and will recognize words with 90% accuracy. Toshiba recently demonstrated prototype voice-activated television and high-fidelity equipment.... More rumors are surfacing regarding the future plans of Apple Computer Company. Reportedly the new model Apple computer will be a Pascal machine for educational users. Also, Apple will place increased emphasis on the business market....

Congress Considering Two Personal Computer Bills: Did you know that two bills about personal computers have been introduced in Congress? One is H.R.3822, which would set up a national endowment for personal computers. The other is H.R.4326, which would create a presidential commission to make recommendations about the personal computer field.

MAIL: I receive a large number of letters each month as a result of this column. If you wish a response, please include a stamped, self-addressed envelope.

Sol Libes
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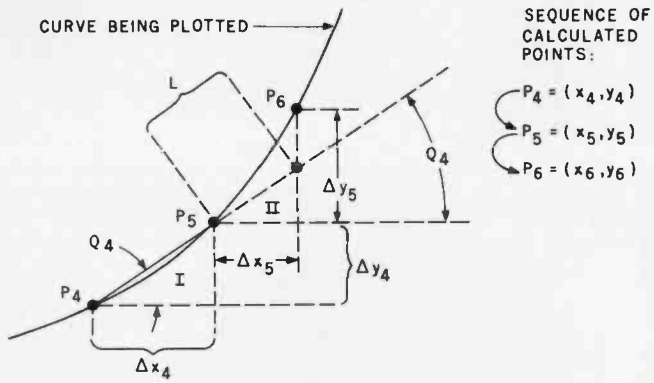
Simplifying the Curve-Plotting Calculation by Geometric Means

A David Nawrocki, 1101 Wiltshire, San Antonio TX 78209

I enjoyed reading Timothy G Bowker's interesting article "Minimizing Curve-Plotting Calculation" (December 1979 BYTE, page 134). Perhaps it is worth pointing out that his equation (1) on page 138, which involves arctangent and cosine functions, can be reduced to a more efficient form for computational purposes. Although the improvement is slight, the use of a single square-root term will allow more rapid calculation than the trigonometric functions originally used. If a very large number of points must be plotted, the accumulated savings in time can be significant.

First, let us note from the illustration in figure 1 that his Δx_5 (the quantity to be found) is related by similar triangles (I and II) to Δx_4, Δy_4, and L (quantities known from previous steps) as follows:



$$\Delta x_5 = \frac{L\,\Delta x_4}{\sqrt{\Delta x_4^2 + \Delta y_4^2}}$$

The possible scale factors M and N cancel out, and it is not necessary to compute Q_4 to obtain Δx_5.■

Alpha Locking in Software

W S Lewis, POB 1555, East Canton OH 44730

Those readers of BYTE who are not hardware fanatics can accomplish the same results in software as was obtained by use of hardware in Terry Conboy's article "Alpha Lock for Your ASCII Keyboard" (January 1980 BYTE, page 156). You can let your computer do the work!

In particular, users of the Z80 microprocessor can add 8 bytes of code to the keyboard-input subroutine. The code shown here as listing 1 should appear in the input

Listing 1: *Portion of Z80 code for uppercase to lowercase conversion, input section.*

```
Hexadecimal      Instruction       Comments
Object Code      Mnemonics

DB 30            XIN IN A,(30H)    ;STATUS PORT
CB 4F                BIT 1,A
28 FA                JR Z,XIN
DB 31                IN A,(31H)    ;KEYBOARD
CB BF                RES 7,A       ;MASK PARITY
```

Listing 2: *Final portion of Z80 code for uppercase to lowercase conversion.*

```
Hexadecimal      Instruction
Object Code      Mnemonics

FE 61            CP 61H
F8               RET M
FE 7B            CP 7BH
F0               RET P
D6 20            SUB 20H
C9               RET
```

subroutine. The code in listing 2 goes at the end of the input subroutine, just before it returns to its calling routine.

Note that the uppercase option is completely under software control. The first compare-immediate (the CP 61H) instruction in listing 2 can be changed to a return (RET) instruction when lowercase is desired, and restored to CP when uppercase is desired. ■

Maintaining a Single Exit Point

Armond Inselberg, 234 Central Ave, Mountain View CA 94040

I agree with James Lewis, author of "Some Notes on Modular Assembly Programming" (December 1979 BYTE, page 222), in his emphasis on modular programming. However, another important tenet of structured programming is the use of a single entry point and a single exit point for a given program module.

The ABORT routine in the modular 8080 code example of listing 2 (on page 224) violates this principle of having only one exit point. In this case we find that the ABORT routine can be exited by either the JNZ (ie: jump if accumulator is not equal to 0) instruction or by the RET (return from subroutine) instruction.

To apply the single-exit principle to the ABORT routine, we must arrange things such that the RET instruction causes a return either to the monitor or to the main level of the application code. To return to the monitor using RET, we must replace the current return address on the stack with the entry-point address for the monitor.

The top of the stack can be changed with the XTHL instruction, which exchanges the contents of the H and L registers with the top of the stack. The ABORT routine would then be coded:

```
ABORT     LDA SHKEY
          ORA A
          JZ RETURN          ;no shift key request
          LXI H,MONITOR      ;shift key hit
          XTHL               ;exchange stack and HL
RETURN    RET
```

However, my preference is that the return to the monitor never be made at all from the ABORT routine, since ABORT is nested below the main level of code. I would rather proceed as follows.

First, in ABORT, test for the conditions requiring a monitor return, and set up the stack (if necessary) for the return to the monitor. Then, ABORT should set a signal requesting a return to the monitor, and then just return to the main level of the application code. At the main level, either a return to the monitor or a jump to the starting point of the application would be made.

The main level would then be coded:

```
START     CALL RANDOM
          CALL NOTE
          CALL ABORT
          JZ   START         ; no monitor request
          RET                ; monitor return requested.
```
■

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Text continued from page 50:
address in the computer's memory from which the data was written onto the disk. All DTS numbers written on the disk have the bits that indicate the disk-drive number masked to 0 so that the file can be read from any disk drive, regardless of the drive in which it was loaded when it was written.

The *sector trailer* is 4 bytes long. The first 2 bytes contain the check sum. The last 2 bytes, except in the last sector in a file, contain the DTS number of the first sector of the file. In the last sector of the file, the last 2 bytes of the sector trailer contain the address at which execution of the contents of the file begins.

Software: The Basic Disk Routines

The basic disk routines handle head positioning, drive selection, sector selection, motor control, and computation of the check sum. Head positioning is performed by the use of the step and direction bits of the drive-select/status word (hexadecimal location CC03). Since the only indication of the position of the head is the track-0 bit in the drive-select/status word, the position of the head must be kept by software as a value in memory.

KIMDOS is a KIM-1 compatible version of the Percom MINIDOS disk operating system.

In a multiple-drive disk system, it is desirable to keep track of the head positions of all drives in the system. The drive-selection routine (subroutine DRIV in listing 1) takes care of this. It saves the current track number of the current drive, restores the current track of the desired drive, and latches the desired drive into the controller. KIMDOS reinitializes the track registers (hexadecimal locations 000F thru 0013) with each operation so that preservation of these bytes is not necessary. However, if the system should be expanded with additional software, the track registers become very important. Inadvertant alteration of these locations would cause reading or writing of the wrong track.

In a multiple-drive system, drive motors are either all running or all stopped. The motors cannot be controlled individually since the drive-selection circuitry does not affect the motor-on signal. This necessitates some special handling of drive selection.

The drive-selection routine must insure that the write head is disabled before switching drives, or the area currently under the head of the newly selected drive will be overwritten. The drive-selection routine must also insure that the sector counter on the controller board is synchronized with the newly selected drive. This can be done only after at least one index pulse has been received from the new drive to reset the sector counter.

The sector-selection routine reads the sector number from the controller. It must catch the leading edge of the desired sector so that the read or write operation does not begin in the middle of the sector; it does this by looking for the change from the previous sector to the desired sector. The sector-selection routine detects the disk-missing condition by setting a KIM hardware timer located on one of the 6530 devices for a quarter of a second. If the timer times out before the desired sector is found, the routine assumes that the disk is not properly inserted in the drive.

Read and Write Routines

The read and write routines are a fundamental part of KIMDOS, which is given in listing 1. Listing 2 is a cross-reference table for the symbols used in listing 1.

The read routines are designed to automatically try again to read incorrectly read sectors. They will try to read a sector up to six times before reporting a read error. Intermittent errors (such as those caused by random electrical noise, airborne contaminants, slight fluctuations in motor speed, small defects in the written data or track surface, or any combination of the above) can be recovered by rereading the sector.

After a read error, the read routine acts as follows: first, the routine rereads twice. If that fails, the routine moves the head to track 0 and back in an attempt to clear any interfering

Text continued on page 178

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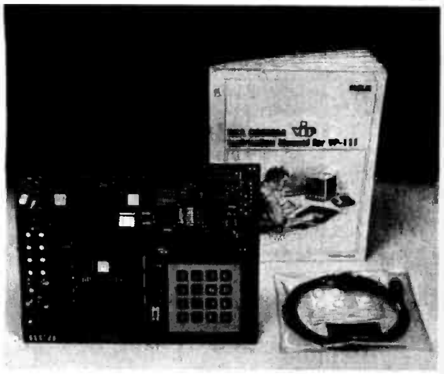

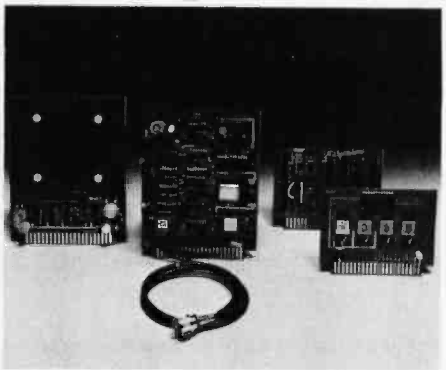

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Listing 1: *KIMDOS, a small disk-operating system for the KIM-1 microcomputer. KIMDOS is a set of disk read and write routines used with a KIM-1 connected to a Percom LFD-400 floppy-disk system. KIMDOS occupies under 1 K bytes of memory (from hexadecimal addresses C000 thru C3FE) and can be stored in one 2708 erasable programmable read-only memory (EPROM). Observe that this listing does not use standard 6502 mnemonics.*

```
Hexadecimal  Object  Label  Instruction  Operand  Commentary
Address      Code           Mnemonic

                    KIMDOS  -  MINI DOS FOR KIM

                    VERSION 3  SEPTEMBER 1979

                    ZERO PAGE STORAGE

                    01 - 0A IS THE SECTOR HEADER

C000              KIMDOS ORG   $C000

C000              DSDR   *     $0000     DESIRED DRIVE
C000              DSTK   *     $0001     AND DESIRED TRACK
C000              DSEC   *     $0002     DESIRED SECTOR
C000              BLTK   *     $0003     BACK LINK TRACK #
C000              BLSC   *     $0004     BACK LINK SECTOR #
C000              FLTK   *     $0005     FORWARD LINK TRACK #
C000              FLSC   *     $0006     FORWARD LINK SECTOR #
C000              LEN    *     $0007     BYTE COUNT (RECORD LENGTH)
C000              TCTP   *     $0008     TARGET ADDRESS
C000              TCTL   *     $0008
C000              TCTH   *     $0009
C000              FTYP   *     $000A     FILE TYPE

                    0B - 0E IS THE SECTOR TRAILER

C000              CKSL   *     $000B     THE CHECKSUM
C000              CKSH   *     $000C
C000              PSTL   *     $000D     POSTAMBLE/EXECUTION ADDRESS
C000              PSTH   *     $000E
C000              CRTK   *     $000F     CURRENT TRACK
                   CURRENT TRACK SAVEAREA
C000              CTKP   *     $0010     DRIVE 0
C000              CTKQ   *     $0011     DRIVE 1
C000              CTKR   *     $0012     DRIVE 2
C000              CTKS   *     $0013     DRIVE 3

C000              DPTR   *     $0014     DATA POINTER
C000              DPTL   *     $0014
C000              DPTH   *     $0015
C000              ALTP   *     $0016     ALTERNATE LOAD POINTER
C000              ALTL   *     $0016
C000              ALTH   *     $0017
C000              TPXH   *     $0018     CKSUM TEMP STORAGE
C000              EXCL   *     $0019     PROGRAM EXECUTION ADDRESS
C000              EXCH   *     $001A
C000              SAVEP  *     $001B
C000              CRDR   *     $001D     CURRENT DRIVE TEMPORARY
C000              HIDR   *     $001B     TEMPORARY STORAGE FOR CDTS
C000              RCNT   *     $001B     READ COUNT TEMPORARY
C000              CKPT   *     $001C     CKSUM POINTER
C000              CKPL   *     $001C
C000              CKPH   *     $001D
C000              DTSA   *     $001C     DRIVE TRACK SAVE
C000              TSSA   *     $001D     TRACK SECTOR SAVE
C000              ENDL   *     $001E     END OF DATA
C000              ENDH   *     $001F

C000              PCL    *     $00EF     PROGRAM COUNTER SAVE
C000              PCH    *     $00F0
C000              PNTL   *     $00FA     DISPLAY WINDOW
C000              PNTH   *     $00FB

                    CONTROLLER COMMUNICATION ADDRESSES

                    INPUT
C000              RDST   *     $CC00     USRT STATUS
C000              RDTA   *     $CC01     RECEIVE DATA
C000              SECT   *     $CC02     SECTOR COUNTER
C000              DVST   *     $CC03     DRIVE STATUS
C000              RRST   *     $CC04     RECEIVER RESTART PULSE
C000              MON    *     $CC05     MOTOR ON PULSE (SEND)
C000              MOFF   *     $CC06     MOTOR OFF PULSE (SEND)

                    OUTPUT
C000              SYNC   *     $CC00     SYNC WORD
C000              WDTA   *     $CC01     SEND DATA
C000              FILL   *     $CC02     FILL WORD
C000              DTSL   *     $CC03     DRIVE SELECT
C000              WPLS   *     $CC04     WRITE PULSE

                    OTHER LABELS

C000              TJX    *     $1705     TIMER START
C000              TOUT   *     $1707     TIME OUT CHECK
C000              STRT   *     $1C4F


                    EQUATES

C000              WRTBIT *     $0008
C000              MTRBIT *     $0004
C000              MILSEC *     $007D
C000              ZERO   *     $0000
C000              DRVMSK *     $00CF
C000              STEPIN *     $0010
C000              SCTMSK *     $000F
C000              HEDLEN *     $000A
C000              TRKMSK *     $003F
C000              TRKLMT *     $0023
C000              SCTBIT *     $0010
C000              STPBIT *     $0020


                    ERROR CODES

C000              DISKMS *     $0000     DISK MISSING
C000              WPROT  *     $0001     WRITE PROTECT
C000              INVSEC *     $0002     INVALID SECTOR #
```

Listing 1 continued on page 162

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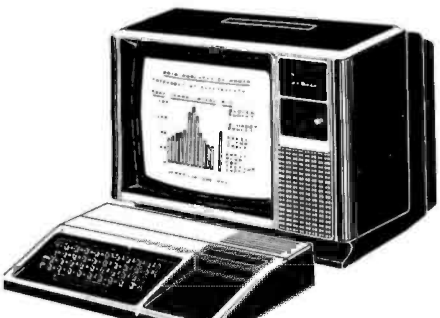

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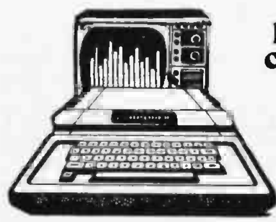

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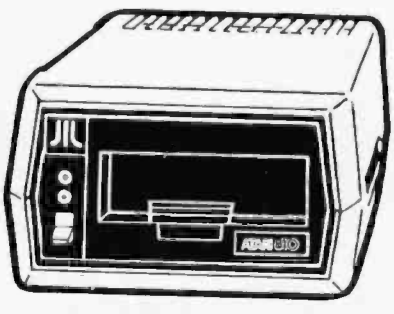

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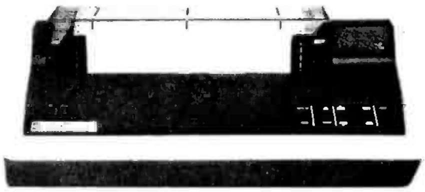
Listing 1 continued:

```
C000                BLNKSC *    $0003     BLANK SECTOR
C000                OVRUN  *    $0004     DISK OVERRUN
C000                READER *    $C005     PERMINENT READ ERROR

                     SECTION 1 THE BASIC ROUTINES


                     JUMP TABLE

C000 4C AA C1               JMP    RSEX   READ SECTOR
C003 4C CF C2               JMP    WSEX   WRITE SECTOR
C006 4C 7E C2               JMP    SAVX
C009 4C 89 C1               JMP    LODX
C00C 4C DA C0               JMP    PREP
C00F 4C B8 C3               JMP    CVTBIN
C012 4C 90 C3               JMP    CVTDEC
C015 4C 4C C3               JMP    FWDC

                     INITOV : INITIALIZE THE TRACK REGISTERS

C018 A9 FF          INITOV LOAIM $FF     OFFLINE CODE
C01A A2 04                 LOXIM $04     5 TRACK REGISTERS
C01C 95 0F          INTLUP STAZX CRTK    INIT  A REGISTER
C01E CA                    DEX           COUNT
C01F 10 FB                 BPL    INTLUP NEXT
C021 60                    RTS

                     GTKX : MOVE HEAD TO TRACK 0

C022 20 40 C0       GTKX   JSR    TKIN   MOVE IN
C025 20 40 C0              JSR    TKIN
C028 20 38 C0       GETP   JSR    TKOT   MOVE OUT
C02B AD 03 CC              LDA    DVST   TRACK 0?
C02E 4A                    LSRA
C02F 4A                    LSRA
C030 B0 F6                 BCS    GETP   NO
C032 A9 00                 LOAIM  $00    ZERO CURENT TRACK
C034 85 0F                 STAZ   CRTK
C036 F0 47                 BEQ    SETL   UNCONDITIONAL BRANCH

                     TKIN , TKOT : MOVE HEAD IN OR OUT 1 TRACK

C038 AD 03 CC       TKOT   LDA    DVST   GET DRIVE# IN 2 MSB
C03B 29 CF                 ANDIM  DRVMSK
C03D 4C 47 C0              JMP    MTVR
C040 AD 03 CC       TKIN   LDA    DVST
C043 29 CF                 ANDIM  DRVMSK
C045 09 10                 ORAIM  STEPIN STEP IN BIT
C047 8D 03 CC       MTVR   STA    DTSL   SET DIRECTION
C04A 20 83 C0              JSR    DEL
C04D 09 20                 ORAIM  STPBIT SET STEP BIT
C04F 8D 03 CC              STA    DTSL
C052 EA                    NOP
C053 EA                    NOP              STRETCH PULSE WIDTH
C054 EA                    NOP
C055 29 DF                 ANDIM  $DF    RESET STEP BIT
C057 8D 03 CC              STA    DTSL
C05A AD 05 CC              LDA    MON    RETRIGGER MOTOR
C05D 4C 83 C0              JMP    DEL

                     SEEX : MOVE HEAD TO DESIRED TRACK

C060 A5 01          SEEX   LDAZ   DSTK   GET DESIRED TRACK#
C062 29 3F                 ANDIM  TRKMSK IGNORE DRIVE#
C064 A8                    TAY
C065 C4 0F                 CPYZ   CRTK   THERE ALREADY?
C067 F0 2B                 BEQ    SOUT   YES
C069 90 0B                 BCC    STPO   LESS THAN CURRENT
C06B 20 40 C0       STPI   JSR    TKIN   STEP IN
C06E E6 0F                 INCZ   CRTK
C070 C4 0F                 CPYZ   CRTK   THERE YET?
C072 D0 F7                 BNE    STPI   NO
C074 F0 09                 BEQ    SETL
C076 20 38 C0       STPO   JSR    TKOT   STEP OUT
C079 C6 0F                 DECZ   CRTK
C07B C4 0F                 CPYZ   CRTK   THERE YET?
C07D D0 F7                 BNE    STPO   NO
C07F A2 1E          SETL   LDXIM  $1E    30 MS HEAD SETTLING
C081 D0 02                 BNE    DELA

                     DELAY 20 MS
C083 A2 14          DEL    LDXIM  $14

                     DELA : DELAY 1 MILISEC FOR EACH INC OF X

C085 48             DELA   PHA
C086 A9 7D          LUUP   LOAIM  MILSEC
C088 8D 05 17              STA    TJX    START TIMER
C08B AD 07 17       LOOP   LDA    TOUT   TIME UP?
C08E F0 FB                 BEQ    LOOP   NO
C090 CA                    DEX
C091 D0 F3                 BNE    LUUP   1 MS PER LOOP
C093 68                    PLA
C094 60             SOUT   RTS

                     DRVTST : SYNC SECTOR COUNTER TO CURRENT DRIVE

C095 20 31 C1       DRVTST JSR    START  MOTOR
C098 A0 19                 LDYIM  $19    25 CHANGES
C09A 20 80 C1              JSR    FFTIME SET TIMER
C09D A9 10          DVLUP  LOAIM  SCTBIT
C09F 2D 03 CC              AND    DVST   GET SECTOR BIT
C0A2 AE 07 17              LDX    TOUT   TIME UP?
C0A5 D0 0F                 BNE    ERRJ   YEP
C0A7 AA                    TAX
C0A8 45 1B                 EORZ   SAVEP  CHANGE IN SECTOR BIT?
C0AA F0 F1                 BEQ    DVLUP  NO, WAIT
C0AC 86 1B                 STX    SAVEP  YES SAVE AND COUNT
C0AE 88                    DEY
C0AF D0 EC                 BNE    DVLUP
C0B1 AD 05 CC       RETRIG LDA    MON    RETRIGGER MOTOR
C0B4 18                    CLC
C0B5 60                    RTS
C0B6 A9 00          ERRJ   LOAIM  DISKMS DISK MISSING
C0B8 38                    SEC
C0B9 60                    RTS


                     PREP : SELECT AND PREPARE DRIVE FOR OPERATION

C0DA A5 02          PREP   LDA    DSEC   GET SECTOR
```

```
C0BC CD 0A 0A            CMP    $0A    LESS THAN 10?
C0BF B0 0C               BCS    BADPRM NO , ERROR
C0C1 A5 01               LDA    PSTK   GET TRACK
C0C3 29 3F               ANDIM  TRKMSK CLEAR DRIVE
C0C5 C9 23               CMPIM  TRKLMT OVERFLOW?
C0C7 90 07               BCC    DRIV   NO, GO CHECK DRIVE
C0C9 A9 04       OVFL    LDAIM  OVRUN  YES, ERROR 4
C0CB 38                  SEC
C0CC 60                  RTS
C0CD A9 02       BADPRM  LDAIM  INVSEC  INVALID SECTOR
C0CF 60                  RTS

C0D0 AD 03 CC    DRIV    LDA    DVST   GET CURRENT DRIVE
C0D3 29 C0               ANDIM  $C0
C0D5 85 1D               STAZ   CRDR   SAVE
C0D7 A5 00               LDAZ   DSDR   GET DESIRED DRIVE
C0D9 29 C0               ANDIM  $C0
C0DB C5 1D               CMPZ   CRDR   SAME?
C0DD D0 08               BNE    SWIT   NO , SWITCH DRIVES
C0DF A5 0F               LDA    CRTK   GET CURRENT TRK
C0E1 C9 FF               CMPIM  $FF    DRIVE INITIALIZED?
C0E3 F0 24               BEQ    DI     NO
C0E5 D0 30               BNE    DS     YES

C0E7 48          SWIT    PHA
C0E8 A5 1D               LDAZ   CRDR
C0EA 18                  CLC
C0EB 2A                  ROLA
C0EC 2A                  ROLA           ROL DRIVE# TO 2 LSB
C0ED 2A                  ROLA
C0EE AA                  TAX
C0EF A5 0F               LDAZ   CRTK   SAVE CURRENT TRACK
C0F1 95 10               STAZX  CTKP   IN SAVEAREA
C0F3 68                  PLA
C0F4 48                  PHA
C0F5 18                  CLC
C0F6 2A                  ROLA
C0F7 2A                  ROLA
C0F8 2A                  ROLA
C0F9 AA                  TAX
C0FA B5 10               LDAZX  CTKP   GET CURRENT TRACK
C0FC 85 0F               STAZ   CRTK   FROM SAVEAREA
C0FE A9 08       DA      LDAIM  WRTBIT
C100 2C 03 CC    DB      BIT    DVST   IS WRITE GATE OFF?
C103 F0 FB               BEQ    DB     NO , THEN WAIT
C105 68                  PLA

C106 8D 03 CC            STA    DTSL   NOW SELECT DRIVE
C109 20 95 C0    DI      JSR    DRVTST SYNC TO DRIVE
C10C B0 10               BCS    DP     ERROR EXIT
C10E A5 0F               LDA    CRTK
C110 C9 FF               CMPIM  $FF    DRIVE ONLINE?
C112 D0 03               BNE    DS     YES
C114 20 22 C0            JSR    CTKX   NO , ZERO TRACK
C117 20 31 C1    DS      JSR    START  CHECK MOTOR
C11A 20 60 C0            JSR    SEEX   FIND DESIRED TRACK
C11D 18                  CLC
C11E 60          DP      RTS

                  CKSEC : PART OF CTSC

C11F AD 07 17    CKSEC   LDA    TOUT   TIME UP?
C122 D0 08               BNE    MISS   YEP
C124 AD 02 CC            LDA    SECT   GET CURRENT SECTOR
C127 29 0F               ANDIM  SCTMSK
C129 C5 02               CMP    PSEC   = DESIRED?
C12B 60                  RTS
C12C 68          MISS    PLA           RESTORE STACK
C12D 68                  PLA
C12E 4C B6 C0            JMP    ERRJ

                  START : START MOTOR

C131 A9 04       START   LDAIM  MTRBIT
C133 2C 03 CC            BIT    DVST   IS MOTOR ON?
C136 F0 0C               BEQ    STARTR YES
C138 A8                  TAY
C139 AD 05 CC            LDA    MON    START IT
C13C A2 00               LDXIM  ZERO
C13E 20 85 C0    DELSS   JSR    DELA   THEN WAIT ASEC
C141 88                  DEY
C142 D0 FA               BNE    DELSS
C144 4C B1 C0    STARTR  JMP    RETRIG

                  CTSC : WAIT FOR DESIRED SECTOR TO COME AROUND

C147 78          CTSC    SEI           DISABLE INTERRUPTS
C148 20 80 C1            JSR    FFTIME START TIMER
C14B 20 1F C1    CTLUPA  JSR    CKSEC  IF DESIRED IS CURRENT
C14E F0 FB               BEQ    CTLUPA THEN WAIT TILL NXT REV
C150 20 1F C1    CTLUPB  JSR    CKSEC  THEN WAIT FOR
C153 D0 FB               BNE    CTLUPB DESIRED
C155 18                  CLC
C156 60                  RTS


                  CRC : COMPUTE CHECKSUM FROM DATA & HEADER

C157 A5 14       CRC     LDA    DPTL   MOVE DATA PTR
C159 85 1C               STA    CKPL   TO CKSUM PTR
C15B A5 15               LDA    DPTH
C15D 85 1D               STA    CKPH
C15F A6 07               LDXZ   LEN    GET LENGTH
C161 A9 00               LDAIM  ZERO   CLEAR SUM
C163 A8                  TAY
C164 85 1B               STAZ   TPXH   CLEAR TEMP STORAGE
C166 20 72 C1            JSR    CX     COMPUTE DATA SUM
C169 86 1D               STXZ   CKPH   POINT TO HEADER
C16B E8                  INX
C16C 86 1C               STXZ   CKPL
C16E A2 0A               LDXIM  HEDLEN HEADER LENGTH
C170 A0 00               LDYIM  ZERO
C172 51 1C       CX      EORIY  CKPT   COMPUTE CKSUM
C174 0A                  ASLA
C175 26 1B               ROLZ   TPXH
C177 90 02               BCC    CQ
C179 69 00               ADCIM  ZERO
C17B C8          CQ      INY
C17C CA                  DEX
C17D D0 F3               BNE    CX
C17F 60                  RTS
```

Listing 1 continued on page 166

T.I. 810 Printer



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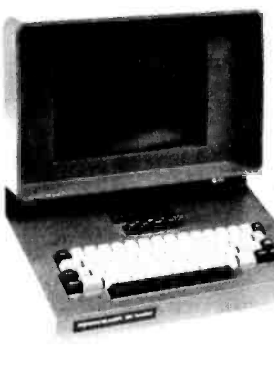

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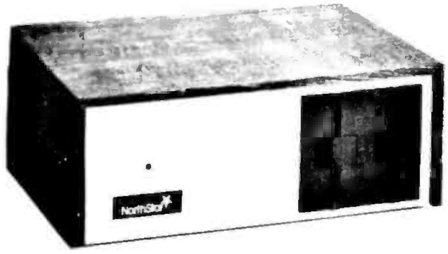

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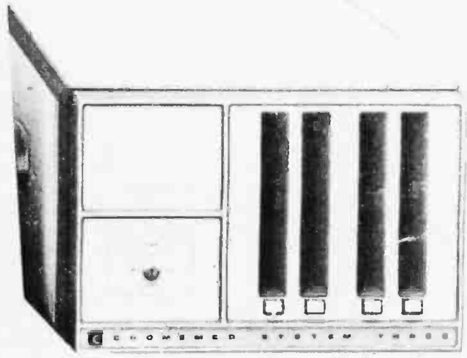

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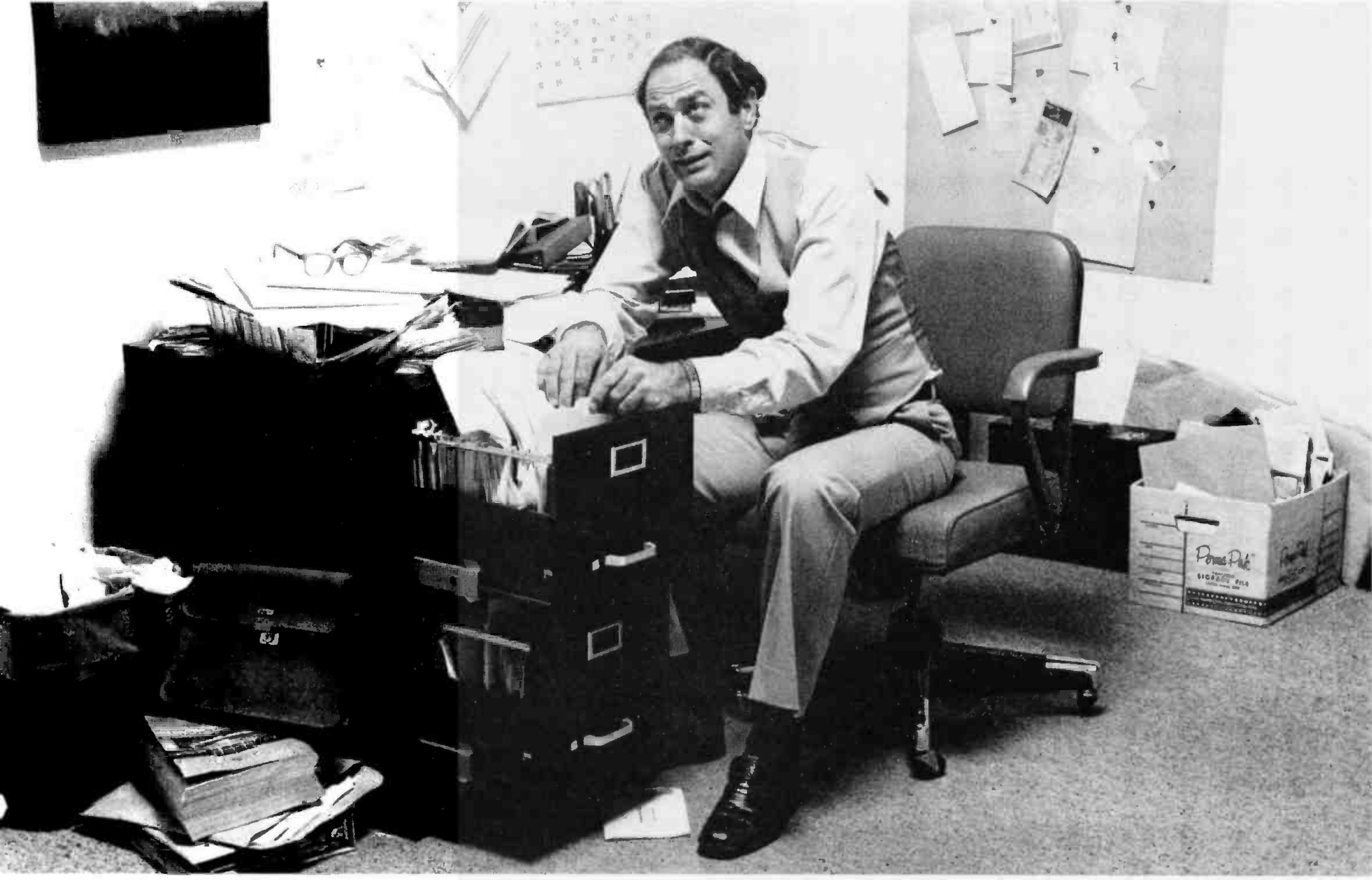
— THIS OFFER EXPIRES JULY 10, 1980 —

Listing 1 continued:

```
                          FFTIME : START TIMER FOR 1/4 SECOND.
                                   STORE TWICE FOR 6530 BUG.

C180 A9 FF       FFTIME LDAIM $FF
C182 8D 07 17    STIMER STA   TOUT
C185 8D 07 17           STA   TOUT
C188 60                 RTS



                          SECTION 2 READ ROUTINES



                          LODX : READ A MEMORY FILE FROM DISK

C189 20 AA C1    LODX   JSR   RSEX    READ A SECTOR
C18C B0 38              BCS   RDRT    PERMINENT ERROR
C18E A5 06              LDAZ  FLSC
C190 D0 06              BNE   NEND    CHECK FOR LAST SECTOR
C192 A5 05              LDAZ  FLTK    (FORWARD LINK ZERO)
C194 F0 0B              BEQ   COPPL   END
C196 A5 06              LDAZ  FLSC
C198 85 02       NEND   STAZ  DSEC    COPY FORWARD LINK TO
C19A A5 05              LDAZ  FLTK    DESIRED TRACK/SECTOR
C19C 85 01              STAZ  DSTK
C19E 4C 89 C1           JMP   LODX    READ NEXT SECTOR
C1A1 A5 0D       COPPL  LDA   PSTL    COPY EXEC ADDRESS
C1A3 85 EF              STA   PCL     TO KIM'S PC
C1A5 A5 0E              LDA   PSTH
C1A7 85 F0              STA   PCH
C1A9 60                 RTS

                          RSEX : READ A SECTOR WITH ERROR RETRY

C1AA 20 BA C0    RSEX   JSR   PREP    PEPARE DRIV
C1AD B0 17              BCS   RDRT    ERROR EXIT
C1AF 20 C7 C1           JSR   RDS     TRY UP TO 3 TIMES
C1B2 B0 12              BCS   RDRT    ERROR CODE IN A
C1B4 D0 10              BNE   RDRT    SUCCESS
C1B6 20 22 C0           JSR   GTKX
C1B9 20 60 C0           JSR   SEEX    RE-SEEK TRACK
C1BC 20 C7 C1           JSR   RDS     TRY AGAIN
C1BF B0 05              BCS   RDRT
C1C1 D0 03              BNE   RDRT
C1C3 A9 05              LDAIM HEADER READ ERROR
C1C5 38                 SEC
C1C6 60          RDRT   RTS

                          RDS : READ A SECTOR WITH 2 RETRYS

C1C7 A9 03       RDS    LDAIM $03     3 TRYS
C1C9 85 1D              STAZ  RCNT
C1CB A9 FB       READ   LDAIM $FB     SYNC CHAR
C1CD 8D 00 CC           STA   SYNC
C1D0 08                 PHP            SAVE INTERRUPT
C1D1 20 47 C1           JSR   GTSC    FIND SECTOR
C1D4 B0 0D              BCS   NDSEC
C1D6 A2 1E              LDXIM $1E     SHORT DELAY TO
C1D8 CA          RG     DEX            PASS OVER SECTOR BOUNDARY
C1D9 D0 FD              BNE   RG
C1DB AD 04 CC           LDA   RRST    START RECIEVER
C1DE 20 66 C2           JSR   IN      SKIP SYNC
C1E1 90 03              BCC   ROK     SYNC FOUND
C1E3 28          NDSEC  PLP            RESTORE INTERRUPTS
C1E4 38                 SEC
C1E5 60                 RTS
C1E6 20 66 C2    ROK    JSR   IN      GET TRACK
C1E9 A8                 TAY
C1EA 45 01              EORZ  DSTK    CHECK FOR PROPER TRACK
C1EC 29 3F              ANDIM TRKMSK  IGNORE DRIVE
C1EE D0 56              BNE   SKER    SEEK ERR
C1F0 98                 TYA
C1F1 85 01              STAZ  DSTK
C1F3 20 66 C2           JSR   IN      GET SECTOR
C1F6 C5 02              CMPZ  DSEC    PROPER SECTOR?
C1F8 D0 4C              BNE   SKER    NO
C1FA A2 00              LDXIM ZERO
C1FC 20 66 C2    HLUP   JSR   IN      GET REST OF HEADER
C1FF 95 03              STAZX BLTK
C201 E8                 INX
C202 E0 08              CPXIM $08
C204 D0 F6              BNE   HLUP
                   PREPARE FOR READING DATA
                   DETERMINE WHICH ADDRESS TO USE
C206 A5 17              LDAZ  ALTH
C208 F0 09              BEQ   NDAL
C20A 85 15              STAZ  DPTH    USE ALT IF NON-ZERO
C20C A5 16              LDAZ  ALTL
C20E 85 14              STAZ  DPTL
C210 4C 1D C2           JMP   GDAT
C213 A5 08       NDAL   LDAZ  TGTL    ELSE USE ADDRESS IN HEADER
C215 85 14              STAZ  DPTL
C217 A5 09              LDAZ  TGTH
C219 85 15              STAZ  DPTH
C21B A0 00       GDAT   LDYIM ZERO
C21D AD 00 CC    DALP   LDA   RDST    DATA READY?
C220 4A                 LSRA
C221 90 FA              BCC   DALP    NO
C223 AD 01 CC           LDA   RDTA
C226 91 14              STAIY DPTH    SAVE A BYTE
C228 C8                 INY
C229 C4 07              CPYZ  LEN
C22B D0 F0              BNE   DALP    READ UNTIL COUNT EXPIRES
C22D A2 00              LDXIM $00
C22F 20 66 C2    CLUP   JSR   IN      GET CHECKSUM
C232 95 0B              STAZX CKSL    AND POSTAMBLE
C234 E8                 INX
C235 E0 04              CPXIM $04
C237 D0 F6              BNE   CLUP
C239 20 57 C1           JSR   CRC     COMPUTE CHECKSUM
C23C C5 0B              CMPZ  CKSL    COMPARE WITH ONE READ
C23E D0 06              BNE   SKER
C240 A5 18              LDAZ  TPXH
C242 C5 0C              CMPZ  CKSH
C244 F0 0A              BEQ   SUCC
C246 28          SKER   PLP
C247 C6 1D              DECZ  RCNT    COUNT TRYS
C249 F0 03              BEQ   SERR
C24B 4C CB C1           JMP   READ
```

Listing 1 continued on page 168



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Circle 99 on inquiry card.

Listing 1 continued:

```
C24E 18          SERR    CLC              Z FLAG=1 MEANS ERROR
C24F 60                  RTS
C250 28          SUCC    PLP                RESTORE INTERRUPT
C251 A5 17               LDAZ  ALTH      ALTERNATE IN USE?
C253 F0 0D               BEQ   NOCQ      NO
C255 A5 07               LDAZ  LEN       YES , UPDATE ALTERNATE
C257 18                  CLC
C258 F0 06               BEQ   INCA      00 MEANS 100
C25A 65 16               ADCZ  ALTL
C25C 85 16               STAZ  ALTL
C25E 90 02               BCC   NOCQ
C260 E6 17       INCA    INCZ  ALTH
C262 18          NOCQ    CLC
C263 A9 FF               LDAIM $FF       Z FLAG=0 MEANS COOD READ
C265 60                  RTS

                  IN : READ A BYTE AND CHECK FOR OUT OF SECTOR

C266 AD 00 CC    IN      LDA   RDST      DATA READY?
C269 4A                  LSRA
C26A B0 0D               BCS   INQ       YES READ IT
C26C AD 02 CC            LDA   SECT      GET SECTOR FROM CONTROLLER
C26F 29 0F               ANDIM $0F
C271 C5 02               CMPZ  DSEC      STILL RIGHT ONE?
C273 F0 F1               BEQ   IN        YES
C275 A9 03               LDAIM BLNKSC EMPTY SECTOR
C277 38                  SEC                ERROR FLAG
C278 60                  RTS
C279 AD 01 CC    INQ     LDA   RDTA      GET A CYTE
C27C 18                  CLC
C27D 60                  RTS



                  SECTION 3 WRITE ROUTINES



                  SAVX : SAVE A FILE ON DISK

C27E A9 00       SAVX    LDAIM ZERO
C280 85 03               STAZ  BLTK      CLEAR BACK LINK
C282 85 04               STAZ  BLSC
C284 A2 01               LDXIM $01
C286 B5 01       KLUP    LDAZX DSTK      COPY TRACK/SECTOR
C288 95 0D               STAZX PSTL      TO POSTAMBLE &
C28A 95 05               STAZX FLTK      FORWARD LINK
C28C CA                  DEX
C28D 10 F7               BPL   KLUP
C28F 20 4C C3    SXS     JSR   FWDC      CALC FORWARD LINK
C292 20 2B C3            JSR   LNTH      CALC LENGTH
C295 A5 14               LDA   DPTL      MOVE DATA PTR
C297 85 08               STA   TGTL      TO TARGET
C299 A5 15               LDA   DPTH
C29B 85 09               STA   TGTH
C29D 20 CF C2    SXT     JSR   WSEX      WRITE A SECTOR
C2A0 B0 39               BCS   ERRD
C2A2 A5 07               LDAZ  LEN       GET LENGTH
C2A4 F0 07               BEQ   INCT      00=100
C2A6 18                  CLC
C2A7 65 14               ADCZ  DPTL      UPDATE DATA ADDRESS
C2A9 85 14               STAZ  DPTL
C2AB 90 02               BCC   NOCW
C2AD E6 15       INCT    INCZ  DPTH
C2AF A5 1F       NOCW    LDAZ  ENDH      IF TARGET GREATER
C2B1 C5 15               CMPZ  DPTH      THAN END
C2B3 F0 03               BEQ   CONT
C2B5 B0 09               BCS   SETU
C2B7 60          SRET    RTS                THEN RETURN
C2B8 A5 1E       CONT    LDAZ  ENDL
C2BA C5 14               CMPZ  DPTL
C2BC F0 02               BEQ   SETU
C2BE 90 F7               BCC   SRET
C2C0 A2 01       SETU    LDXIM $01       ELSE PREPARE FOR NEXT SECTOR
C2C2 B5 01       SLUP    LDAZX DSTK      MOVE TRACK/SECTOR TO
C2C4 95 03               STAZX BLTK      BACKWARD LINK
C2C6 B5 05               LDAZX FLTK      MOVE FORWARD LINK
C2C8 95 01               STAZX DSTK      TO TRACK/SECTOR
C2CA CA                  DEX
C2CB 10 F5               BPL   SLUP
C2CD 30 C0               BMI   SXS       UNCONDITIONAL

                  WSEX : WRITE A SECTOR

C2CF 20 DA C0    WSEX    JSR   PREP      PREPARE DRIVE
C2D2 B0 08               BCS   WSQ       ERROR EXIT
C2D4 A9 01               LDAIM $01
C2D6 2C 03 CC            BIT   DVST      WRITE PROTECT ON?
C2D9 D0 02               BNE   WSR       NO
C2DB 38          ERRD    SEC
C2DC 60          WSQ     RTS
C2DD 20 57 C1    WSR     JSR   CRC       COMPUTE CHECKSUM
C2E0 85 0B               STAZ  CKSL      SAVE IT
C2E2 A5 18               LDAZ  TPXH
C2E4 85 0C               STAZ  CKSH
C2E6 A9 FF               LDAIM $FF       FILL CHAR FOR USRT
C2E8 8D 02 CC            STA   FILL

C2EB 08                  PHP             SAVE INTERRUPT STATUS
C2EC 20 47 C1            JSR   GTSC      FIND SECTOR
C2EF B0 37               BCS   WERR
C2F1 8D 04 CC            STA   WPLS      START TRANSMITTER
C2F4 A2 10               LDXIM $10
C2F6 A9 00               LDAIM $00
C2F8 20 63 C3    WSS     JSR   OUT       WRITE LEADER 16 X 00
C2FB CA                  DEX
C2FC D0 FA               BNE   WSS
C2FE A9 FB               LDAIM $FB
C300 20 63 C3            JSR   OUT       SEND SYNC
C303 B5 01       WST     LDAZX DSTK      WRITE 10 BYTE HEADER
C305 20 63 C3            JSR   OUT
C308 E8                  INX
C309 E0 0A               CPXIM $0A
C30B D0 F6               BNE   WST
C30D A6 07               LDXZ  LEN       GET LENGTH
C30F A0 00               LDYIM $00
C311 B1 14       WSU     LDAIY DPTR      WRITE DATA
C313 20 63 C3            JSR   OUT
C316 C8                  INY
C317 CA                  DEX
```

Listing 1 continued on page 170

Listing 1 continued:

```
C318 D0 F7             BNE    WSU
C31A A0 04             LDYIM  $04
C31C B5 0D        WSV  LDAZX  CKSL    WRITE CHECKSUM & POSTAMBLE
C31E 20 63 C3          JSR    OUT
C321 E8                INX
C322 88                DEY
C323 D0 F7             BNE    WSV
C325 28                PLP            RESTORE INTERRUPT

C326 18                CLC
C327 60                RTS
C328 28           WERR PLP            RESTORE INTERRUPTS
C329 38                SEC
C32A 60                RTS

                  LNTH : COMPUTE LENGTH AND FIND LAST BLOCK

C32B A5 1E        LNTH LDAZ   ENDL    SUBTRACT TARGET
C32D 38                SEC
C32E E5 14             SBCZ   DPTL    FROM END
C330 85 07             STAZ   LEN     TO GET LENGTH
C332 A5 1F             LDAZ   ENDH
C334 E5 15             SBCZ   DPTH    LAST BLOCK?
C336 F0 05             BEQ    LQ      YES
C338 A9 00             LDAIM  $00     NO THEN LENGTH=100
C33A 85 07             STAZ   LEN
C33C 60                RTS
C33D E6 07        LQ   INCZ   LEN
C33F 85 05             STAZ   FLTK    LAST BLOCK
C341 85 06             STAZ   FLSC    CLEAR FORWARD LINK
C343 A5 19             LDAZ   EXCL
C345 85 0D             STAZ   PSTL    MOVE EXECUTION ADDRESS
C347 A5 1A             LDAZ   EXCH
C349 85 0E             STAZ   PSTH
C34B 60                RTS

                  FWDC : CALCULATE FORWARD LINK. ASSUMES
                         FLTK =CURRENT TRACK

C34C A5 06        FWDC LDAZ   FLSC    GET CURRENT SECTOR
C34E C9 08             CMPIM  $08     FIND NEXT ALTERNATE
C350 F0 0C             BEQ    FR      IF NOT 8
C352 B0 04             BCS    FQ      OR 9
C354 69 02             ADCIM  $02     THEN ADD 2
C356 D0 08             BNE    FS      UNCONDITIONAL
C358 E6 05        FQ   INCZ   FLTK    NEXT TRACK
C35A A9 00             LDAIM  $00     FIRST SECTOR
C35C F0 02             BEQ    FS      UNCONDITIONAL
C35E A9 01        FR   LDAIM  $01
C360 85 06        FS   STAZ   FLSC    NEXT SECTOR
C362 60                RTS

                  OUT : SEND A BYTE WHEN USRT IS READY

C363 48           OUT  PHA
C364 AD 00 CC     OUTQ LDA    RDST    USRT READY?
C367 10 FB             BPL    OUTQ    NO, WAIT
C369 68                PLA
C36A 8D 01 CC          STA    WDTA    SEND A BYTE
C36D 60                RTS

```

```


                       SECTION 4 KEYBOARD CONTROL ROUTINES



                       SAVK : ENTRY TO WRITE FILE
                           ENTER THE FOLLOWING VIA KIM:
                           BEGINNING ADDRESS      14,15
                           ENDING ADDRESS         1E,1F
                           EXECUTION ADDRESS      19,1A
                           DRIVE/TRACK/SECTOR     1C,1D
                           FILE TYPE              0A

C36E 20 85 C3     SAVK JSR    INTCVT INIT AND CONVERT
C371 B0 15             BCS    KERR   ERROR
C373 20 7E C2          JSR    SAVX   WRITE FILE
C376 B0 10             BCS    KERR
C378 20 90 C3     LAST JSR    CVTDEC CONVERT D/T/S
C37B 4C 4F 1C     KIMQ JMP    STRT   RETURN TO KIM

                       LOOK : READ A MEMORY FILE
                           ENTER THE FOLLOWING
                           DRIVE/TRACK/SECTOR     1C,1D
                           ALTERNATE TARGET OR 0  16,17

C37E 20 85 C3     LOOK JSR    INTCVT INIT AND CONVERT
C381 B0 05             BCS    KERR
C383 20 89 C1          JSR    LOOX   READ FILE
C386 90 F0             BCC    LAST   SHOW LAST TRK/SECTOR

C388 85 FA        KERR STAZ   PNTL   ERROR CODE TO DISPLAY
C38A A9 FF             LDAIM  $FF    ERROR FLAG
C38C 85 FB             STAZ   PNTH
C38E D0 EB             BNE    KIMQ

                  CVTDEC : CONVERT TRACK/SECTOR FOR DISPLAY

C390 A9 FF      CVTDEC LDAIM  $FF    ZERO COUNTER?
C392 85 FB             STAZ   PNTH
C394 A5 01             LDAZ   DSTK   GET TRACK #
C396 29 3F             ANDIM  TRKMSK IGNORE DRIVE#
C398 38                SEC
C399 E6 FB        LSQ  INCZ   PNTH
C39B E9 0A             SBCIM  $0A    DIVIDE BY 10 LOOP
C39D B0 FA             BCS    LSQ    BRANCH NO BORROW
C39F 69 0A             ADCIM  $0A    REMAINDER IN A
C3A1 48                PHA
C3A2 A5 02             LDAZ   DSEC   CONVERT ALTERNATE TO
C3A4 4A                LSRA
C3A5 90 02             BCC    KSS    TO SEQUENTIAL SECTOR
C3A7 69 04             ADCIM  $04    ADD 4 + CARRY
C3A9 85 FA        KSS  STAZ   PNTL   SAVE
C3AB 68                PLA
C3AC 0A                ASLA
C3AD 0A                ASLA
C3AE 0A                ASLA
C3AF 0A                ASLA
C3B0 05 FA             ORAZ   PNTL   MERGE TRACK LSB
C3B2 85 FA             STAZ   PNTL   WITH SECTOR
C3B4 60                RTS
```

Listing 1 continued on page 172

NEECO PROUDLY INTRODUCES

COMMODORE'S NEW 8000 SERIES (80 column) COMPUTERS

$1695 (available May/June '80)

CBM™ 8050 DUAL DRIVE FLOPPY DISK

The CBM 8050 Dual Drive Floppy Disk in an enhanced version of the intelligent CBM 2040 Disk Drive. The CBM 8050 has all of the features of the CBM 2040, and provides more powerful software capabilities, as well as nearly one megabyte of online storage capacity. The CBM 8050 supplies relative record files and automatic diskette initialization. It can copy all the files from one diskette to another without copying unused space. The CBM 8050 also offers improved error recovery and the ability to append to sequential files.

HARDWARE SPECIFICATIONS
Dual Drives
Two microprocessors
974K Bytes storage on two 5.25" diskettes (ss)
Tracks 70
Sectors 17-21
Soft sector format
IEEE-488 interface
Combination power (green) and error (red) indicator lights
Drive Activity indicator lights
Disk Operating System Firmware (12K ROM)
Disk Buffer (4K RAM)

FIRMWARE
DOS version 2.0
Sequential file manipulation
Sequential user files
Relative record files
Append to sequential files
Improved error recovery
Automatic diskette initialization
Automatic directory search
Command parser for syntax validation
Program load and save

CBM™ 8000 SERIES BUSINESS COMPUTERS

The new Commodore 8000 series computers offer a wide screen display to show you up to 80-character lines of information. Text editing and report formatting are faster and easier with the new wide-screen display. The 8000 series also provides a resident Operating System with expanded functional capabilities. You can use BASIC on the 8000 computers in both interactive and program modes, with expanded commands and functions for arithmetic, editing, and disk file management. The CBM 8000 series computers are ideally suited for the computing needs of the business marketplace.

SCREEN
2000 character display, organized into twenty-five 80-column lines
64 ASCII, 64 graphic characters
3 x 8 dot matrix characters
Green phosphor screen
Brightness control
Line spacing: 1½ in Text Mode
1 in Graphics Mode

KEYBOARD
73-key typewriter style keyboard with graphic capabilities
Repeat key functional with all keys

MEMORY
CBM 8016: 16K (15359 net) random access memory (RAM)
CBM 8032: 32K (31743 net) random access memory (RAM)

POWER REQUIREMENTS
Volts: 110V
Cycles: 60 Hz
Watts: 100

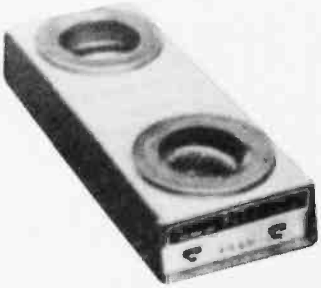
SCREEN EDITING CAPABILITIES
Full cursor control (up, down, right, left)
Character insert and delete
Reverse character fields
Overstriking
Return key sends entire line to CPU regardless of cursor position

INPUT/OUTPUT
Parallel port
IEEE-488 bus
2 cassette ports
Memory and I/O expansion connectors

FIRMWARE
24K or ROM contains:
BASIC (version 4.0) with direct (interactive) and indirect (program) modes
9-digit floating binary arithmetic
Tape and disk file handling software

The 8000 Series will be available May/June '80

Model 8016	Model 8032	2040 Dual Floppy
$1495	**$1795**	**$1295**



Available June/July

$395

CBM™ IEEE MODEM

SPECIFICATIONS
*Full or half duplex operation
*300 bits per second
*Standard IEEE 488 interface
*Switch selectable originate, off, answer-full duplex, test, half duplex
*Visible indicators are transmit data, receive data, carrier ready, test
*Frequency shifted modulation
*Bell 103/113 compatible

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Listing 1 continued:

```
                             CVTBIN : CONVERT DECIMAL DRIVE/TRACK/SECTOR
                                      TO INTERNAL FORMAT

C3B5 20 18 CØ   INTCVT JSR    INITDV INIT AND CONVERT

C3B8 A5 1D      CVTBIN LDA    TSSA
C3BA 29 ØF             ANDIM SCTMSK EXTRACT SECTOR
C3BC C9 ØA             CMPIM $ØA    VALID?
C3BE BØ 3C             BCS   INVS   NO
                CONVERT IT TO ALTERNATING SECTOR
C3CØ C9 Ø5             CMPIM $Ø5    LESS THAN 5?
C3C2 9Ø Ø8             BCC   CDQ    YES
C3C4 38                SEC
C3C5 E9 Ø5             SBCIM $Ø5    MINUS 5
C3C7 ØA                ASLA          MULTIPLY BY 2
C3C8 69 Ø1             ADCIM $Ø1    ADD 1
C3CA DØ Ø1             BNE   CDR    UNCONDITONAL
C3CC ØA         CDQ    ASLA          MULTIPLY BY 2
C3CD 85 Ø2      CDR    STAZ  DSEC   SAVE SECTOR
C3CF A5 1D             LDAZ  TSSA   GET HIGH NYBBLE
C3D1 4A                LSRA
C3D2 4A                LSRA
C3D3 4A                LSRA
C3D4 4A                LSRA
C3D5 C9 ØA             CMPIM $ØA    VALID?
C3D7 BØ 23             BCS   INVS   NO
C3D9 85 Ø1             STAZ  DSTK   SAVE LOW ORDER TRACK #
                MULTIPLY HI ORDER TRACK BY 1Ø
C3DB A5 1C             LDAZ  DTSA
C3DD 29 ØF             ANDIM $ØF    CLEAR DRIVE #
C3DF 85 1D             STAZ  HIOR   SAVE
C3E1 ØA                ASLA          MULTIPLY BY 4
C3E2 ØA                ASLA
C3E3 18                CLC
C3E4 65 1D             ADCZ  HIOR   ADD ONCE (5X)
C3E6 ØA                ASLA          MULTIPLY BY 2 (1ØX)
C3E7 65 Ø1             ADCZ  DSTK   ADD LOW ORDER
C3E9 C9 23             CMPIM TRKLMT
C3EB BØ ØF             BCS   INVS
C3ED 85 Ø1             STAZ  DSTK
C3EF A5 1C             LDAZ  DTSA
C3F1 29 FØ             ANDIM $FØ    GET DRIVE #
C3F3 C9 4Ø             CMPIM $4Ø
C3F5 BØ Ø5             BCS   INVS
C3F7 ØA                ASLA
C3F8 ØA                ASLA
C3F9 85 ØØ             STAZ  DSDR
C3FB 6Ø                RTS

C3FC A9 Ø2      INVS   LDAIM $Ø2    INVALID SECTOR
C3FE 6Ø         THEEND RTS

   ALTH   ØØ17    ALTL   ØØ16    ALTP   ØØ16    BADPRM CØCD
   BLNKSC ØØØ3    BLSC   ØØØ4    BLTK   ØØØ3    CDQ    C3CC
   CDR    C3CD    CKPH   ØØ1D    CKPL   ØØ1C    CKPT   ØØ1C
   CKSEC  C11F    CKSH   ØØØC    CKSL   ØØØB    CLUP   C22F
   CONT   C2D8    COPPL  C1A1    CQ     C17B    CRC    C157
```

```
CRDR   ØØ1C    CRTK   ØØØF    CTKP   ØØ1Ø    CTKQ   ØØ11
CTKR   ØØ12    CTKS   ØØ13    CVTBIN C3B8    CVTDEC C39Ø
CX     C172    DA     CØFE    DALP   C21D    DB     C19Ø
DELA   CØ85    DELSS  C13E    DEL    CØ83    DI     C1Ø9
DISKMS ØØØØ    DP     C11E    DPTH   ØØ15    DPTL   ØØ14
DPTR   ØØ14    DRIV   CØDØ    DRVMSK ØØCF    DRVTST CØ95
DS     C117    DSDR   ØØØØ    DSEC   ØØØ2    DSTK   ØØØ1
DTSA   ØØ1C    DTSL   CCØ3    DVLUP  CØ9D    DVST   CCØ3
ENDH   ØØ1F    ENDL   ØØ1E    ERRJ   CØE6    ERRO   C2DB
EXCH   ØØ1A    EXCL   ØØ19    FFTIME C18Ø    FILL   CCØ2
FLSC   ØØØ6    FLTK   ØØØ5    FQ     C358    FR     C35E
FS     C36Ø    FTYP   ØØØA    FWDC   C34C    GDAT   C21B
GETP   CØ28    GTKX   CØ22    GTLUPA C14C    GTLUPB C15Ø
GTSC   C147    HEDLEN ØØØA    HIOR   ØØ1D    HLUP   C1FC
IN     C266    INCA   C26Ø    INCT   C2AD    INITDV CØ18
INQ    C279    INTCVT C3B5    INTLUP CØ1C    INVS   C3FC
INVSEC ØØØ2    KERR   C388    KIMDOS CØØØ    KIMQ   C37B
KLUP   C286    KSS    C3A9    LAST   C378    LEN    ØØØ7
LNTH   C32B    LOOK   C37E    LOOX   C1Ø9    LOOP   C688
LQ     C33D    LSQ    C399    LUUP   CØ86    MILSEC ØØ7D
MISS   C12C    MOFF   CCØ6    MON    CCØ5    MTRBIT ØØØ4
MTVR   CØ47    NENO   C198    NOAL   C213    NOCQ   C262
NOCW   C2AF    NOSEC  C1E3    OUTQ   C364    OUT    C363
OVFL   CØC9    OVRUN  ØØØ4    PCH    ØØ Ø    PCL    ØØEF
PNTH   ØØFB    PNTL   ØØFA    PREP   CØBA    PSTH   ØØØE
PSTL   ØØØD    RCNT   ØØ1D    RDHT   C1C6    RDST   CCØØ
RDS    C1C7    RDTA   CCØ1    READ   C1CB    READER ØØØ5
RETRIC CØD1    ROK    C1E6    RQ     C1D8    RRST   CCØ4
RSEX   C1AA    SAVEP  ØØ1D    SAVK   C36E    SAVX   C27E
SCTBIT ØØ1Ø    SCTMSK ØØØF    SECT   CCØ2    SEEX   CØ6Ø
SERR   C24E    SETL   CØ7F    SETU   C2CØ    SKER   C246
SLUP   C2C2    SOUT   CØ94    SRET   C2D7    START  C131
STARTR C144    STEPIN ØØ1Ø    STIMER C182    STPBIT ØØ2Ø
STPI   CØ6D    STPO   CØ76    STRT   1C4F    SUCC   C25Ø
SWIT   CØE7    SXS    C28F    SXT    C29D    SYNC   CCØØ
TGTH   ØØØ9    TGTL   ØØØ8    TGTP   ØØØ8    THEEND C3FE
TJX    17Ø5    TKIN   CØ4Ø    TKOT   CØ38    TOUT   17Ø7
TPXH   ØØ18    TRKLMT ØØ23    TRKMSK ØØ3F    TSSA   ØØ1D
WDTA   CCØ1    WERR   C328    WPLS   CCØ4    WPROT  ØØØ1
WRTBIT ØØØ8    WSEX   C2CF    WSQ    C2DC    WSR    C2DD
WSS    C2F8    WST    C3Ø3    WSU    C311    WSV    C31C
ZERO   ØØØØ
```

Listing 2: *Cross-reference table for the symbols in listing 1.*

```
SYMBOL          DEFINED         REFERENCES
ALTH            43              438  476  484
ALTL            42              441  481  482
ALTP            41
BADPRM          240             232
BLNKSC          110             498
BLSC            16              515
BLTK            15              432  514  548
CDQ             733             727
COR             734             732
CKPH            53              332  338
CKPL            52              330  340
CKPT            51              343
CKSEC           292
CKSH            28              467  567
CKSL            27              459  464  565  595
CLUP            458             462
CONT            542             539
COPPL           380             374
CQ              348             346
CRC             329             463  564
CROR            48              245  248  256
CRTK            31              147  175  179  180  184  185  250
                                262  272  281
CTKP            33              263  271
CTKQ            34
CTKR            35
CTKS            36
CVTBIN          721             124
CVTDEC          692             125  672
CX              343             337  350
DA              273
DALP            449             451  456
DB              274             275
DEL             191             159  168
DELA            195             188  310
DELSS           310             312
DI              279             252
DISKMS          107             223
DP              288             280
DPTH            40              331  440  447  526  536  538  615
DPTL            39              329  442  445  524  533  534  543
                                612
DPTR            38              453  589
DRIV            243             236
DRVMSK          95              153  156
DRVTST          207             279
DS              285             253  283
DSDR            12              246  762
DSEC            14              230  296  376  428  496  702  734
DSTK            13              172  233  378  422  426  517  547
                                550  582  694  742  752  755
DTSA            54              744  756
DTSL            79              158  161  166  278
DVLUP           210             216  219
DVST            70              142  152  155  211  243  274  305
                                560
ENDH            57              537  614
ENDL            56              542  610
ERRJ            223             213  300
ERRO            562             529
EXCH            46              625
EXCL            45              623
FFTIME          356             209  318
FILL            78              569
FLSC            18              371  375  622  632  642
FLTK            17              373  377  519  549  621  638
FQ              638             635
FR              641             634
FS              642             637  640
FTYP            23
FWDC            632             126  522
GDAT            448             443
GETP            141             145
GTKX            139             284  393
GTLUPA          319             320
GTLUPB          321             322
GTSC            317             409  572
HEDLEN          98              341
HIDR            49              746  750
HLUP            431             435
IN              491             415  420  427  431  458  497
INCA            484             480
INCT            536             531
INITDV          130
INQ             501             493
INTCVT          719             668  680
INTLUP          132             134
INVS            765             724  741  754  759
INVSEC          109
KERR            685             669  671  681
KIMDOS          10
KIMQ            673             688
KLUP            517             521
KSS             706             704
LAST            672             683
LEN             19              333  455  478  530  587  613  618
                                620
LNTH            610             523
LOOK            680
LOOX            369             122  379  682
LOOP            198             199
LQ              620             616
LSQ             697             699
LUUP            196             201
MILSEC          93              196
MISS            298             293
MOFF            73
MON             72              167  308
MTRBIT          92              304
```

Listing 2 continued on page 176

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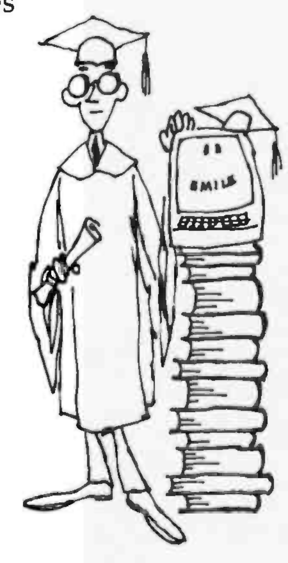

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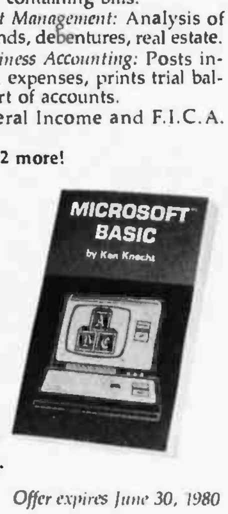

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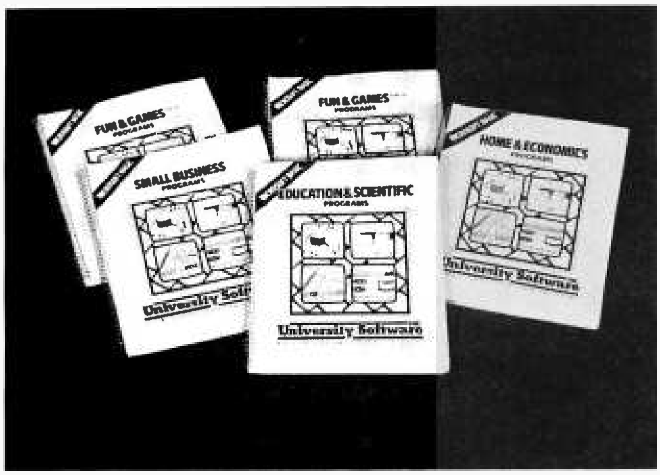

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```
MTVH        158      154
NEND        376      372
NOAL        444      439
NOCQ        485      477  483
NOCW        537      535
NOSEC       417      410
OUT         647      577  581  583  590  596
OUTQ        648      649
OVFL        237
OVRUN       111      237
PCH         60       383
PCL         59       381
PNTH        62       687  693  697
PNTL        61       685  706  712  713
PHEP        230      123  380  557
PSTH        30       382  626
PSTL        29       380  510  624
HCNT        50       405  470
HORT        400      370  389  391  392  396  397
HOS         404      390  395
ROST        67       449  491  648
RDTA        68       452  501
HEAD        406      472
READER      112      398
RETRIG      220
ROK         420      416
RQ          412      413
RRST        71       414
RSEX        388      119  369
SAVEP       47       215  217
SAVK        668
SAVX        513      121  670
SCTBIT      101      210
SCTMSK      97       295  722
SECT        69       294  494
SEEX        172      286  394
SERR        473      471
SETL        187      148  182
SETU        546      540  544
SKER        469      424  429  465
SLUP        547      552
SOUT        203      176
SRET        541      545
STAHT       304      285
STAHTR      313      306
STEPIN      96       157
STIMER      357
STPBIT      102      160
STPI        178      181
STPO        183      177  186
STRT        86       673
SUCC        475      468
SWIT        255      249
SXS         522      553
SXT         528
SYNC        76       407
TCTH        22       446  527
TCTL        21       444  525
TCTP        20
THEEND      766
TJX         84       197
TKIN        155      139  140  178
TKOT        152      141  183
TOUT        85       198  212  292  358
TPXH        44       336  345  466  566
TRKLMT      100      235  753
TRKMSK      99       173  234  423  695
TSSA        55       735
WDTA        77       651
WERR        604      573
WPLS        80       574
WPROT       108
WRTBIT      91       273
WSEX        557      120  528
WSQ         563      558
WSR         564      561
WSS         577      579
WST         582      586
WSU         589      593
WSV         595      599
ZERO        94       309  334  342  347  430  448  513

OPCODE USAGE TABLE
    *   63      ADC  9      AND  15     ASL  12
    BCC  11     BCS  22     BEQ  22     BIT  3
    BMI  1      BNE  31     BPL  4      CLC  12
    CMP  18     CPX  3      CPY  4      DEC  2
    DEX  8      DEY  3      EOR  3      INC  6
    INX  5      INY  3      JMP  15     JSR  43
    LDA  85     LDX  14     LDY  5      LSR  9
    NOP  3      ORA  3      PHA  5      PHP  2
    PLA  7      PLP  5      ROL  7      RTS  28
    SBC  4      SEC  10     SEI  1      STA  59
    STX  3      TAX  3      TAY  4      TYA  1


ADDRESS MODE OCCURENCES
    AY  0       AX  0       ZX  13
    ZY  0       IM  74      IX  0
    IY  3       Z   97      A   27
    NONE 362
```

Text continued from page 158:
particles from the head surface. In addition, this operation insures that the head is on the proper track. Another three reads are attempted; if this fails, the data is assumed to be unrecoverable.

The memory locations that must be initialized before a read operation are given in table 4.

The write routines write a contiguous block of memory to the disk on the required number of sequential sectors. They are also responsible for calculating the forward and backward links and the check sum for each sector. Each sector except the last contains 256 bytes of data; if the number of bytes to be saved is not an integer multiple of 256, the last sector may be shorter. Each sector is preceded by 16 bytes of 0s before the sync character. This is followed by the sector header, the data, and the trailer. No read operation is done after writing to verify the data, because the infrequency of write errors does not warrant the extra overhead.

The memory locations that must be initialized before an area of memory can be saved on disk are given in table 5.

Control Routines

The routines SAVK and LODK provide the interface between the user and the disk routines. These routines expect the appropriate information to be preset in memory by use of the KIM keyboard. The only incompatibility with the Percom MINIDOS routines here is in the indication of an omitted value. The Percom routines use the value hexadecimal FFFF to indicate a field not in use, and KIMDOS uses a high-order byte of 0. This is not important since the 6800 and 6502 microprocessors store their high- and low-order address bytes in the opposite order and are not compatible anyway.

The control routines SAVK and LODK convert their parameters into the proper format where necessary and call the disk subroutines. Upon return, these two routines display the results of the requested operation on the KIM display and return control to the KIM monitor. The information displayed is either the DTS number of the last sector read or written in decimal, or FF*nn*, where *nn* is an error code. The error codes are given in table 6.

Interrupts

In any system, it is often desirable to use interrupts for various processes. Because KIMDOS is involved in time-critical functions when doing disk input/output (I/O), an interrupt at the wrong time could cause catastrophic errors. Therefore, the nonmaskable interrupt (NMI) line cannot be used during disk I/O.

However, KIMDOS does allow for the use of the maskable interrupt request (IRQ) line. This is done by saving the status register and disabling the IRQ line before starting any time-critical functions. The status register is then restored after the critical function is completed. This causes the servicing of the IRQ interrupt to be delayed for as much as 20 ms at a time. Any interrupt-driven system that can tolerate this limitation can function properly with KIMDOS.

Testing

Since the drive and controller both come assembled and tested, the checkout procedure is relatively simple. The only equipment I used was a logic probe and a multimeter.

The first step is to connect the drive and controller to the KIM bus and verify all power-supply voltages. When they are correct, basic communication with the controller can be verified by entering the hexadecimal address CC05 via the KIM-1 keypad. This should start the motor and keep it on until the address is changed. If the motor does not start, then there is probably a bad connection to KIM.

Next, the motor-off pulse can be checked by pressing the + key on the KIM keypad to increment the address on the display to hexadecimal CC06. This should turn off the motor immediately. The motor time-out circuit can be checked by entering hexadecimal CC05 on the KIM display,

Hexadecimal Address	Contents
0016, 0017	Beginning memory address (optional; substitute 0 to use address stored in the disk file)
001C, 001D	Drive/Track/Sector (DTS) number of first sector in the file being read

Table 4: *Information required to read a file into memory from disk. The file being read into memory will begin at the address pointed to by hexadecimal memory locations 0016 and 0017. However, if the contents of these two bytes are 0, the file will be loaded into memory beginning at the address stored with the file. The DTS number is stored here in binary-coded decimal format, with the high-order byte stored first.*

Hexadecimal Address	Contents
0008, 0009	Beginning address of memory to be saved
000A	File type
0019, 001A	Execution address (optional ; use 0 to omit)
001C, 001D	Drive/Track/Sector number of first sector to be written
001E, 001F	Ending address of memory to be saved

Table 5: *Information required to save a file. These are the hexadecimal memory locations that must be set before the SAVK (save a file) routine from listing 1 is called. The DTS number is stored here in binary-coded decimal format, with the high-order byte stored first.*

Error Code	Message
0	Disk missing (given after read or write operation)
1	Disk protected (given after write operation only)
2	Invalid sector number (given after read or write operation)
3	Blank sector (given after read operation only)
4	Disk overrun; attempted to write more than 349 sectors
5	Permanent read error

Table 6: *List of disk-related error codes. If a read or write operation ends in failure, the left four digits of the KIM display will read FF*nn*, where* nn *is one of the error codes listed in this table.*

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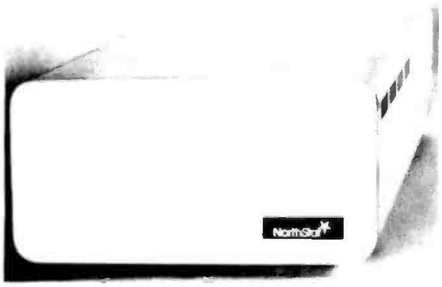

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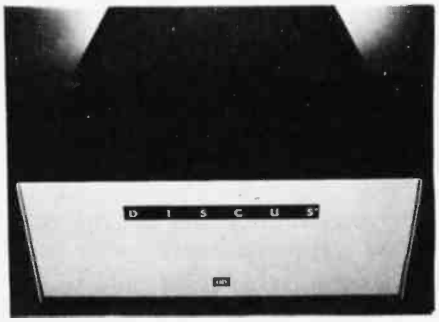

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Hard sectoring means that sector boundaries are detected by means of holes punched in the floppy disk.

followed by another address. The motor should run about 3 seconds and stop.

Now the sector-counting circuitry can be checked. With a disk inserted in the drive, enter hexadecimal CC05 and then hexadecimal CC02. The rightmost digit of the KIM display (which shows the low nybble of the contents of hexadecimal location CC02) should be rapidly changing as long as the motor is running. When the motor stops, this digit should contain a decimal digit (0 thru 9) indicating the last sector passed.

After all of the previously mentioned tests have been completed, the software can be used to do further testing. The TEST routine, given in listing 3, is included for this purpose. TEST does a static test of most of the controller functions and their interaction with various subroutines within KIMDOS. It uses the number of the key pressed on the keypad as an index into a table of subroutine addresses. From there, it does a subroutine jump to the routine thus addressed.

Upon return, the TEST routine displays the value of the accumulator in the rightmost two digits of the KIM display. It also displays the value of the carry flag in the left four digits — FFFF for carry set and 0000 for carry clear. (This is done for those routines that return the carry flag set as an error indicator and use the value in the accumulator as an error code.)

Execution of the TEST routine begins at hexadecimal 0200. The appropriate data must be set in the 0 page for the subroutines to be tested. Some subroutines must be used together. For example, the motor must be started and the drive must be selected before the head-movement routines will work. To add more subroutines, increase the value in the compare instruction at hexadecimal location 020C and add the appropriate addresses to the end of the table.

The final test that I had to do was

Listing 3: *Listing for program TEST. This program executes a given KIMDOS routine (see documentation at the beginning of the listing) depending on which key on the KIM keypad is pressed.*

```
Hexadecimal  Object  Label  Instruction  Operand    Commentary
Address      Code           Mnemonic

                            TEST : ROUTINE TO TEST THE BASIC DISK
                                   DRIVER SUBROUTINES

                            SUBROUTINES UNDER TEST

                     SUB              ADDRESS   KEY#
2000                 GTKX     *       $C022      0    GO TO TRACK 0
2000                 PREP     *       $C00C      1    PREPARE DRIVE FOR I/O
2000                 START    *       $C131      2    START MOTOR
2000                 TKOT     *       $C038      3    MOVE HEAD OUT 1
2000                 TKIN     *       $C040      4    MOVE HEAD IN 1
2000                 SEEX     *       $C060      5    FIND TRACK IN 01
2000                 GTSC     *       $C147      6    FIND SECTOR IN 02
                                                 7    RETURN TO KIM

                            KIM ADDRESSES

2000                 SCND     *       $1F1F
2000                 GETK     *       $1F6A
2000                 KIM      *       $1C4F

                            ZERO PAGE STORAGE

2000                 TOAD     *       $0020
2000                 TODQ     *       $0021
2000                 SAKE     *       $0022
2000                 PNTH     *       $00FB
2000                 PNTL     *       $00FA
2000                 INH      *       $00F9

2000                          ORG     $2000

2000 20 1F 1F        STAR     JSR     SCND      LITE DISPLAY
2003 20 6A 1F                 JSR     GETK      GET KEY
2006 C5 22                    CMPZ    SAKE      DEBOUNCE
2008 F0 F6                    BEQ     STAR
200A 85 22                    STAZ    SAKE
200C C9 08                    CMPIM   $08       VALID?
200E B0 F0                    BCS     STAR      NO
2010 0A                       ASLA              YES, MULTIPLY BY 2
2011 AA                       TAX               TO GET INDEX
2012 BD 32 20                 LDAAX   TABL      MOVE OBJECT ADDRESS
2015 85 20                    STAZ    TOAD      TO JUMP VECTOR
2017 E8                       INX
2018 BD 32 20                 LDAAX   TABL
201B 85 21                    STAZ    TODQ
201D 20 2F 20                 JSR     JMPP      CALL SUBROUTINE
2020 85 F9                    STAZ    INH
2022 A9 FF                    LDAIM   $FF       ERROR FLAG
2024 B0 02                    BCS     STOR      BRANCH ON ERROR
2026 A9 00                    LDAIM   $00       GOOD FLAG
2028 85 FA           STOR     STAZ    PNTL
202A 85 FB                    STAZ    PNTH
202C 4C 00 20                 JMP     STAR
202F 6C 20 00        JMPP     JMI     TOAD

2032 22              TABL     =       GTKX
2033 C0                       =       GTKX      /
2034 0C                       =       PREP
2035 C0                       =       PREP      /
2036 31                       =       START
2037 C1                       =       START     /
2038 38                       =       TKOT
2039 C0                       =       TKOT      /
203A 40                       =       TKIN
203B C0                       =       TKIN      /
203C 60                       =       SEEX
203D C0                       =       SEEX      /
203E 47                       =       GTSC
203F C1                       =       GTSC      /
2040 4F                       =       KIM
2041 1C                       =       KIM       /
```

GETK	1F6A	GTKX	C022	GTSC	C147	INH	00F9
JMPP	202F	KIM	1C4F	PNTH	00FB	PNTL	00FA
PREP	C00C	SAKE	0022	SCND	1F1F	SEEX	C060
STAR	2000	START	C131	STOR	2028	TABL	2032
TKIN	C040	TKOT	C038	TOAD	0020	TODQ	0021

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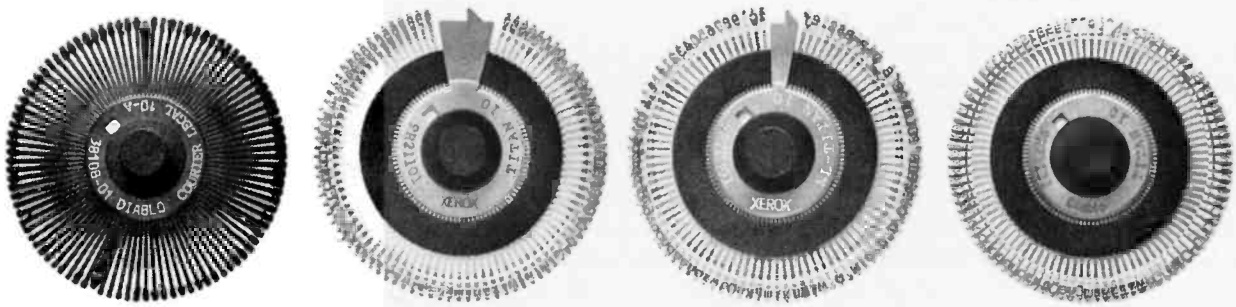

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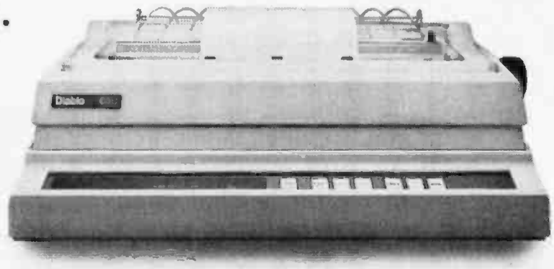

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to read and write data using a floppy disk previously recorded in the Percom format. I did this to confirm that the KIMDOS software produces results using the controller board and disk that are identical to the results produced by the Percom 6800 code. Since I found this to be the case, no one using KIMDOS needs to repeat that test.

Error Recovery

As in all systems, there will occasionally be unrecoverable errors. The Percom format allows for recovery of broken files. Since each sector contains the DTS number of the first sector of the file, each sector can be associated with its file. Reading does not have to start with the first sector; it can start on any sector and will continue to the end of the file.

When a read error occurs, try rereading the sector several times. Also try to read a sector on another track of the disk (to move the head around some) before rereading the original sector in error. Reinserting the disk may also help. If all of the above measures fail, then execute the routine LAST at hexadecimal address C378. This will display the number of the sector containing the error. To try a partial recovery, start the read operation at one sector past the displayed address. If that fails, try the next sector, and so on. Any valid sector can be read in this way. A file may have only one bad sector, with the rest readable.

> Alternating-sector addressing allows time for the housekeeping routines that must be executed between reading and writing sectors.

Expansion

To fully utilize the features of the LFD-400 disk system, a more extensive disk-operating system is necessary. This software is designed to be the basis of such a system. These subroutines can be used to perform the basic functions needed by a larger disk-operating system that provides for named files, automatic space management, and buffered I/O.

To facilitate expansion, KIMDOS has a jump table located at the beginning of the executable code that contains JMP instructions to all subroutines in KIMDOS needed by external software. This allows KIMDOS to be updated (in case of bugs or enhancements) without reassembling the calling routines. With the nine routines in the jump table, any disk I/O can be performed under external program control.

RSEX and WSEX are used to read and write individual sectors. To use them, the data at hexadecimal locations 0000 thru 000A must be supplied. (See the beginning of listing 1.) To read an individual sector, the alternate address pointer, hexadecimal locations 0016 and 0017, must point to the starting location of the file when it is loaded into memory. If the value of the alternate address pointer is 0, the sector will load beginning at an address stored in the sector header. Similarly, to write an individual sector, the data pointer, hexadecimal locations 0014 and 0015, must point to the beginning byte of

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Since the drive and controller both come assembled and tested, the checkout procedure is relatively simple.

the area to be stored on the disk file. All head positioning and drive preparation is taken care of.

LODX and SAVX are the subroutine versions of LODK and SAVK. They require the same data as LODK and SAVK, except that the DTS number must be converted to three single-byte quantities and stored in hexadecimal locations 0000 thru 0002. The subroutine PREP can be used to select the desired drive and seek the desired track. The CVTBIN and CVTDEC subroutines convert the DTS number to binary and decimal, respectively. Subroutine FWDC calculates the next sector in a file. The INITDV subroutine sets the track registers to hexadecimal FF. If any errors are encountered, control is returned to the calling routine with the carry bit set and the error code in the accumulator. This allows complete external control of the disk system.

Since developing KIMDOS, I have developed ZAPDOS. ZAPDOS is modeled after Percom's MINIDOS-PLUSX disk-operating system. It allows loading and saving of up to thirty-one named files per disk. It occupies the upper two read-only-memory sockets in the LFD-400 board. ZAPDOS contains thirteen read-only-memory resident commands to manipulate and display disk space and memory. When used with its ten disk-resident utility programs, ZAPDOS transforms KIM into a powerful microcomputer system.

Conclusion

I have been independent of cassette tape for over two years now. It has been a great pleasure to be able to load even the largest file in 1 or 2 seconds. I no longer leave my KIM system on for days to keep from spending the time necessary to write all of memory to tape and verify that the tape is good. The Percom LFD-400 is a viable and cost-effective answer to the mass-storage problem.

KIMDOS should be easily converted for use on other 6502 systems. An interface for the Apple II should be straightforward. KIMDOS is available in a 2708 read-only memory from Percom. (See below.) I would like to express thanks to Bob Haas for his valuable consultation on this project.■

Percom Data Company (211 North Kirby, Garland TX 75042) is making available the current version of KIMDOS on a 2708 erasable programmable read-only memory (EPROM) part to be used on the disk-controller board of the Percom LFD-400 5-inch floppy-disk drive. This can be obtained along with a Percom LFD-400 disk drive for $15 above the current price of the disk-drive unit. A floppy disk containing KIMDOS-related software (including the ZAPDOS disk-operating system mentioned at the end of this article) is also available from Percom.

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Over the past 25 years there has been a tremendous evolution in the functional capabilities of language systems. These systems need no longer be confined to "big" machines. Much of the improvement in function is becoming available in language systems for microcomputers.

Yet, major manufacturers are still promoting their "super" micro assemblers/debuggers as the best software tool for applications software of computer systems. Consequently, many programmers and designers continue to work with primitive language tools.

This first BYTE-sponsored conference on languages and tools for microcomputing will introduce designers, systems analysts, implementers, and managers to various high level languages and associated systems tools that are becoming commercially available. Knowledge of these recent developments is absolutely essential to productive use of microcomputer techology when that scarce resource, programmer/designer time, is being spread more and more thinly among a myriad of potential applications.

The conference will zero in on five specific high level languages because they are—or shortly will become—readily available for implementations with small computers. Speakers will explore these languages and tools for programming in terms of their usefulness for practical microcomputer applications.

Three of the featured languages are members of a family of languages evolved from FORTRAN by way of Algol: Pascal, C, and Ada. These are most appropriate for uses in which documentation is as much a part of the design philosophy as the achievement of a functional design itself. HAL/S, also in this family, will be discussed at the conference in terms of the history of software tools used in the NASA space-shuttle project's flight-control system design.These languages share purposes with some of the more common commercial languages available on large computers, such as PL/I and COBOL.

Differing in philosophy and point of view—but also commercially available—are two other languages and corresponding language concepts: LISP and FORTH. Each is characterized by a concept of language extensibility, which is implemented in a highly interactive approach. The central and dominant theme of LISP is one of list structures, which may be either data or program material. The concept of tree structures and relationships underlies LISP's usefulness in the artificial-intelligence milieu. FORTH has a central theme of a stack-oriented processor, emulated as a threaded code interpreter, and an extensible library of operations that may be defined beyond a basis set of standard primitives.

THE PROGRAM

Introduction

Carl T. Helmers, Jr.
Editor-in-Chief
BYTE Magazine

Writing in high level languages has numerous well-publicized advantages: programs are more portable; they have superior structures; they are easier to write and debug. At this first session of the conference, Carl Helmers will survey and define language systems, analyze language systems as complete tools, discuss the evolution of all high level languages, and establish reasons why specific high level languages are appropriate for microcomputers.

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Executive Officer
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The use of software tools in the development of systems involving computers is crucially important. Fred Martin, one of the designers of the HAL/S language, will review the advantages of high level language techniques and automated aids to programming from the point of view of his NASA experience with HAL/S, developed specifically to replace the machine-dependent, low-level programming that plagued the Apollo project. The crucial importance of high level languages in reliable software design will be reviewed in the context of this system—in which a software crash can literally lead to a pile of broken parts on the ground.

The Pascal Perspective

Peter Grogono
Analyst/Programmer
Concordia University

The Pascal language is one of the most attractive alternatives in the small computer field. It has steadily gained popularity in use on machines as small as the Apple-II. Peter Grogono, the author of Programming in Pascal, will provide an introduction to the language and discuss its use as a more powerful, more modular, more elegant solution to business data problems.

After Pascal, What?

Dr. Kenneth L. Bowles
Director, Institute for Information Systems
University of California, San Diego

While Pascal is an immensely useful language, it is not necessarily a panacea. Limitations of the language in areas of real time control and handling of multiple concurrent processes, in particular, argue for a new look at the design of the language. Ken Bowles will introduce one evolutionary variant that will become very important over the next decade—the Ada language, originally designed for the Department of Defense. Microcomputer implementations of this language, using machine-independent techniques, will make it a strong alternative for programming microcomputer applications systems.

Trees And Lists as Tools

Dr. Henry G. Baker, Jr.
Assistant Professor
University of Rochester

Not all programming problems are amenable to convenient solutions using conventional block-structured, sequential languages. Many require representing complex heterogeneous objects and relationships among those objects. This approach is attractive for selected applications: symbolic mathematical computation, computer-aided design, commercial integrated databases, English front-end processors, computer-aided manufacturing, robotics control, interactive graphic systems, and interactive integrated circuit-design systems.

The LISP language offers the block-structured control of Pascal, together with the friendly interactive nature of BASIC. In addition, it offers lists and trees as data structuring primitives and a tireless "garbage collector" to keep memory neat and clean.

Henry Baker will discuss the LISP language and the kinds of automated tools required to use it.

What is C?

John A. Morse
Principal Engineer, Corporate Research
Digital Equipment Corporation

The language C was originally developed at Western Electric for use as a tool for development of the UNIX operating system at Bell Laboratories. Now that C compilers are starting to become available for microcomputer systems, this language becomes a viable alternative for both operating system and application developers. John Morse will give an overview of the language C and will detail the types of applications for which it is most appropriate.

The Forth Alternatives

Charles H. Moore
Chairman of the Board
Forth, Inc.

One viable and unconventional approach to programming is the highly interactive language FORTH, a language in which the feature of extensibility is emphasized. The typical implementation of FORTH is a highly integrated combination of software development tools and programming aids oriented toward a conceptual stack machine with integers as the primitive data type. In any given application, unique extensions that fit into the matrix basic core of the language are created by the designer. Charles Moore, the inventor of FORTH, will demonstrate some of the more dynamic uses of the language in real-time applications.

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Designers, systems analysts, implementers, and managers with an interest in holding down costs on their software projects. Fields with special applicability include electronics and electronics design, automated manufacturing, scientific instrumentation design, and aerospace control systems.

Tentative Schedule

June 16, 1980

8:00- 9:00 A.M.	**REGISTRATION**
9:00-10:00 A.M.	**INTRODUCTION:** Carl Helmers
10:00-10:30 A.M.	**COFFEE INTERMISSION**
10:30-12:00 P.M.	**THE IMPORTANCE OF TOOLS:** Fred Martin
12:00- 1:30 P.M.	**LUNCHEON**
1:30- 3:00 P.M.	**THE PASCAL PERSPECTIVE:** Peter Grogono
3:00- 3:15 P.M.	**COFFEE INTERMISSION**
3:15- 4:45 P.M.	**AFTER PASCAL, WHAT?:** Ken Bowles
4:45- 5:15 P.M.	**OPEN DISCUSSION**

June 17, 1980

8:30-10:00 A.M.	**TREES AND LISTS AS TOOLS:** Henry Baker
10:00-10:30 A.M.	**COFFEE INTERMISSION**
10:30-12:00 P.M.	**THE FORTH ALTERNATIVE:** Charles Moore
12:00- 1:30 P.M.	**LUNCHEON**
1:30- 3:00 P.M.	**WHAT IS C?:** John Morse
3:00- 4:00 P.M.	**PANEL DISCUSSION:** All speakers

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DIGITAL RESEARCH

Programming Quickies

Decisions, Decisions

Geoffrey Gass, 5240 SW Dosch Rd, Portland OR 97201

Frequently, a program has to select one of two positive actions as the result of a test (eg: print a "+" or a "−" after checking the sign of a number).

Conventionally, it might be done in a skip chain like this 6800 code:

```
SGN     TST NUMB      Make the test.
        BMI NEG       One course if negative.
        LDA A #'+     The other course if positive.
        BRA PRINT     Watch out — don't run into NEG.
NEG     LDA A#'−      Minus sign for negative number.
PRINT   JSR OUTPUT    Back together again; print the
                      sign.
```

It's awkward, running into yourself like that. Here is how to avoid the awkwardness and save a couple of bytes:

```
SGN     LDA A #'+     Set up for one course in advance.
        TST NUMB      Then make the test.
        BPL PRINT     Confirming advance choice.
        LDA A #'−     Change course if advance choice
                      wrong.
PRINT   JSR OUTPUT    Print the proper sign.
```

The bytes saved (if not otherwise needed) can be used after the TST NUMB to BEQ (branch on accumulator equal to 0) past the PRINT routine if the number is zero, so 0 will be output without a sign, assuming we are dealing with a 1-byte number. ■

Formatted Program Output for the KIM-1

Lawrence A Ezard, PhD, Associate Professor of Engineering, Pennsylvania State University, Capitol Campus, Middletown PA 17057

Here is a short program that might be useful for owners of the MOS Technology KIM-1 system. It can be used to find bugs, and to print out and document programs.

The flowchart in figure 1 illustrates the algorithm utilized. This program will examine the contents of programmable memory and print the program instructions found there. The output is in a format of address, operation code, and operand. The user specifies the starting and stopping addresses to be examined by storing values in the appropriate locations. At the end of its execution, the program returns control to the KIM monitor.

In writing the program, I made use of the fact that, with three exceptions, the least significant digit (in hexa-

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decimal) of 1-byte op codes is always 8 or A. Also, with nine exceptions, the least significant digit of 3-byte op codes is always C, D, or E.

Listing 1 was produced by the program. The labels, source code mnemonics, and comments were added later. The program uses several subroutines from the KIM-1 monitor: CRLF, PRTPNT, OUTSP, PRTBYT, and INCPT.■

Listing 1: *Program in 6502 code to print out hexadecimal instruction codes from KIM-1 memory. Before running the program, do the following. Load the starting address for examination in locations 17F5 (SAL, low-order) and 17F6 (SAH, high-order). Load the ending address plus 1 in locations 17F7 (EAL, low-order) and 17F8 (EAH, high-order). Clear the decimal mode by entering 00 in location 00F1. The starting address for execution is hexadecimal 0301. The memory used is 0300 to 03D0.*

Hexadecimal Address	Hexadecimal Code			Label	Op Code	Operand	Comments
0300				TEMP1			
0301	AD	F5	17		LDA	SAL	Load starting address in POINTL
0304	85	FA			STA	FA	and POINTH
0306	AD	F6	17		LDA	SAH	
0309	85	FB			STA	FB	
030B	20	2F	1E	START1	JSR	CRLF	Do carriage return and line feed
030E	20	1E	1E		JSR	PRTPNT	Print starting address
0311	20	9E	1E		JSR	OUTSP	Print 2 spaces
0314	20	9E	1E		JSR	OUTSP	
0317	A2	00			LDX	#$00	
0319	A1	FA			LDA	(FA,X)	Load Contents of address at FB, FA
031B	8D	00	03		STA	TEMP1	
031E	C9	00			CMP	#$00	Decide if Op Code is 1 byte
0320	F0	15			BEQ	PRNT1	
0322	C9	40			CMP	#$40	
0324	F0	11			BEQ	PRNT1	
0326	C9	60			CMP	#$60	
0328	F0	0D			BEQ	PRNT1	
032A	29	0F			AND	#$0F	
032C	C9	08			CMP	#$08	
032E	F0	07			BEQ	PRNT1	
0330	C9	0A			CMP	0A	
0332	F0	03			BEQ	PRNT1	If not 1 byte
0334	4C	40	03		JMP	B3	Jump to test for 3-byte Op Code
0337	AD	00	03	PRNT1	LDA	TEMP1	Print 1-byte Op Code
033A	20	3B	1E		JSR	PRTBYT	
033D	4C	B7	03		JMP	INCAD	Jump to increment address
0340	AD	00	03	B3	LDA	TEMP1	Test for a 3-byte Op Code
0343	C9	19			CMP	#$19	
0345	F0	31			BEQ	PRNT3	
0347	C9	39			CMP	#$39	
0349	F0	2D			BEQ	PRNT3	
034B	C9	59			CMP	#$59	
034D	F0	29			BEQ	PRNT3	
034F	C9	79			CMP	#$79	
0351	F0	25			BEQ	PRNT3	
0353	C9	99			CMP	#$99	
0355	F0	21			BEQ	PRNT3	
0357	C9	B9			CMP	#$B9	
0359	F0	1D			BEQ	PRNT3	
035B	C9	D9			CMP	#$D9	
035D	F0	19			BEQ	PRNT3	
035F	C9	F9			CMP	#$F9	
0361	F0	15			BEQ	PRNT3	
0363	C9	20			CMP	#$20	
0365	F0	11			BEQ	PRNT3	
0367	29	0F			AND	#$0F	
0369	C9	0C			CMP	OC	
036B	F0	0B			BEQ	PRNT3	
036D	C9	0D			CMP	#$0D	
036F	F0	07			BEQ	PRNT3	
0371	C9	0E			CMP	#$0E	
0373	F0	03			BEQ	PRNT3	
0375	4C	A1	03		JMP	PRNT2	GOTO print 2 bytes
0378	AD	00	03	PRNT3	LDA	TEMP1	Print 3 bytes
037B	20	3B	1E		JSR	PRTBYT	Print Op Code
037E	20	9E	1E		JSR	OUTSP	Space
0381	20	9E	1E		JSR	OUTSP	
0384	20	63	1F		JSR	INCPT	Increment address
0387	A2	00			LDX	#$00	Load contents of address
0389	A1	FA			LDA	(FA,X)	at FBFA
038B	20	3B	1E		JSR	PRTBYT	Print Operand
038E	20	9E	1E		JSR	OUTSP	
0391	20	9E	1E		JSR	OUTSP	
0394	20	63	1F		JSR	INCPT	Increment address
0397	A2	00			LDX	#$00	Load contents of address
0399	A1	FA			LDA	(FA,X)	at FBFA
039B	20	3B	1E		JSR	PRTBYT	Print Operand
039E	4C	B7	03		JMP	INCAD	
03A1	AD	00	03	PRNT2	LDA	TEMP1	Print 2 bytes

Listing 1 continued on page 194

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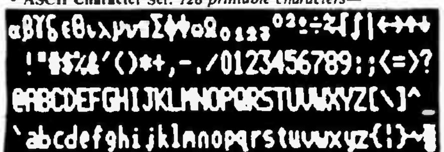

BAUDOT Character Set: *A B C D E F G H I J K L M N O P Q R S T U V W X Y Z - ? : • 3 $ # ( ) . , 9 0 1 4 ! 5 7 ; 2 / 6 8 •* **Cursor Modes:** *Home, Backspace, Horizontal Tab, Line Feed, Vertical Tab, Carriage Return. Two special cursor sequences are provided for absolute and relative X-Y cursor addressing* • **Cursor Control:** *Erase, End of Line, Erase of Screen, Form Feed, Delete* • **Monitor Operation:** *50 or 60Hz (jumper selectable.*

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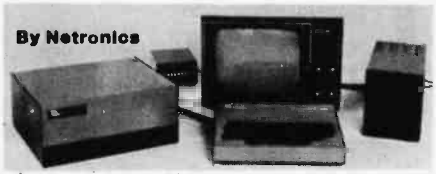

Hex Keypad/Display.

Hex Keypad/Display Specifications

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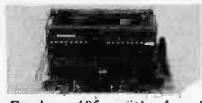

Explorer/85 with Level "C" card cage.

Level "C" Specifications

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Circle 116 on inquiry card.

Listing 1 continued:

```
03A4   20   3B   1E          JSR   PRTBYT   Print Op Code
03A7   20   9E   1E          JSR   OUTSP    Space
03AA   20   9E   1E          JSR   OUTSP
03AD   20   63   1F          JSR   INCPT    Increment address
03B0   A2   00               LDX   #$00     Load contents of
03B2   A1   FA               LDA   (FA,X)   address at FBFA
03B4   20   3B   1E          JSR   PRTBYT   Print Operand
03B7   20   63   1F   INCAD  JSR   INCPT    Increment to next Op Code
03BA   A5   FB               LDA   FB       Address
03BC   CD   F8   17          CMP   EAH
03BF   F0   03               BEQ   NEXT
03C1   4C   0B   03          JMP   START1   If this address is
03C4   A5   FA        NEXT   LDA   FA       equal to the ending
03C6   CD   F7   17          CMP   EAL      address then stop
03C9   F0   03               BEQ   STOP     Otherwise go to START1
03CB   4C   0B   03          JMP   START1   and print the Op Code
03CE   4C   4F   1C   STOP   JMP   START
```

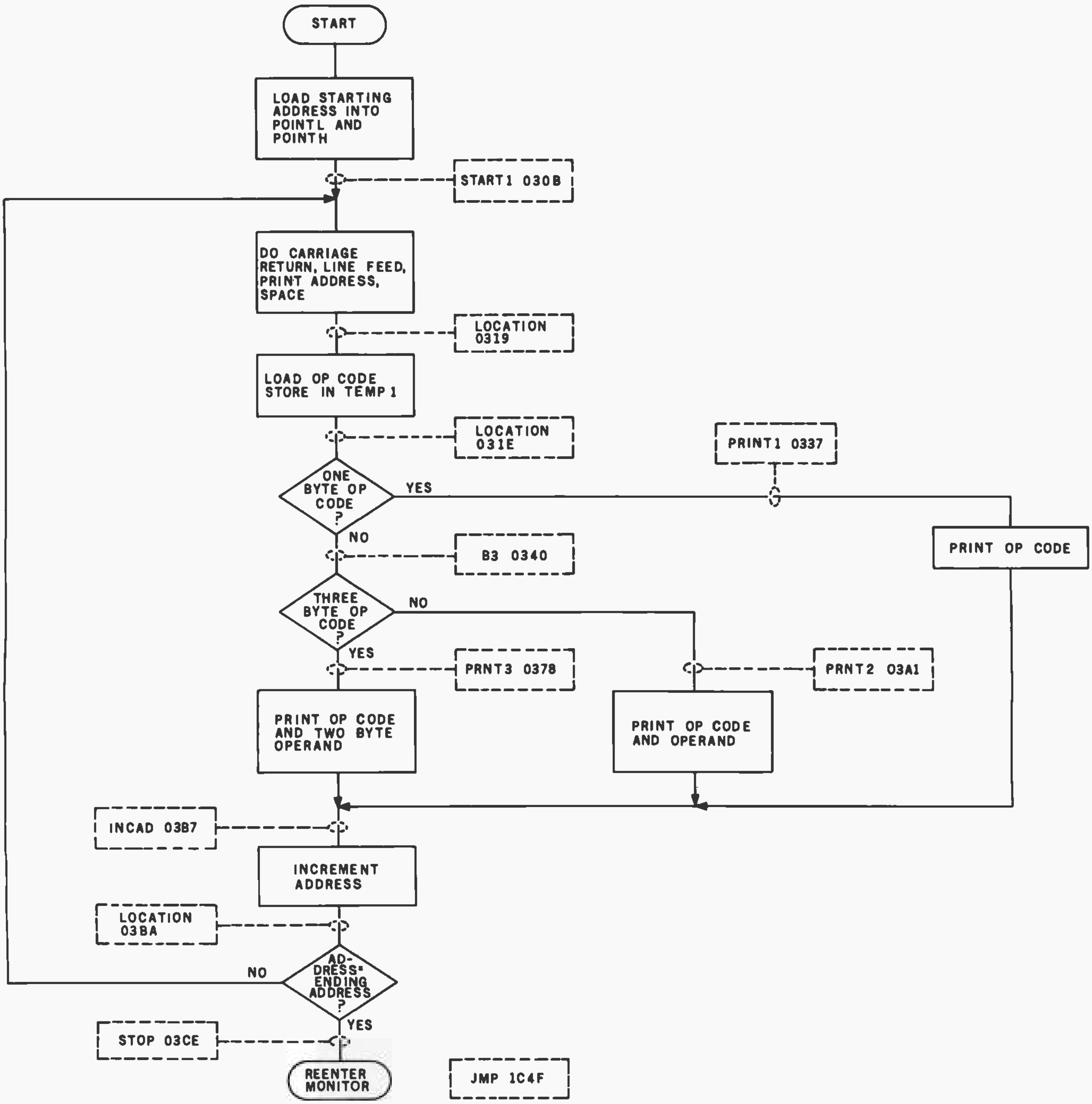

Figure 1: *Flowchart of procedure used to print hexadecimal instruction codes from KIM-1 memory.*

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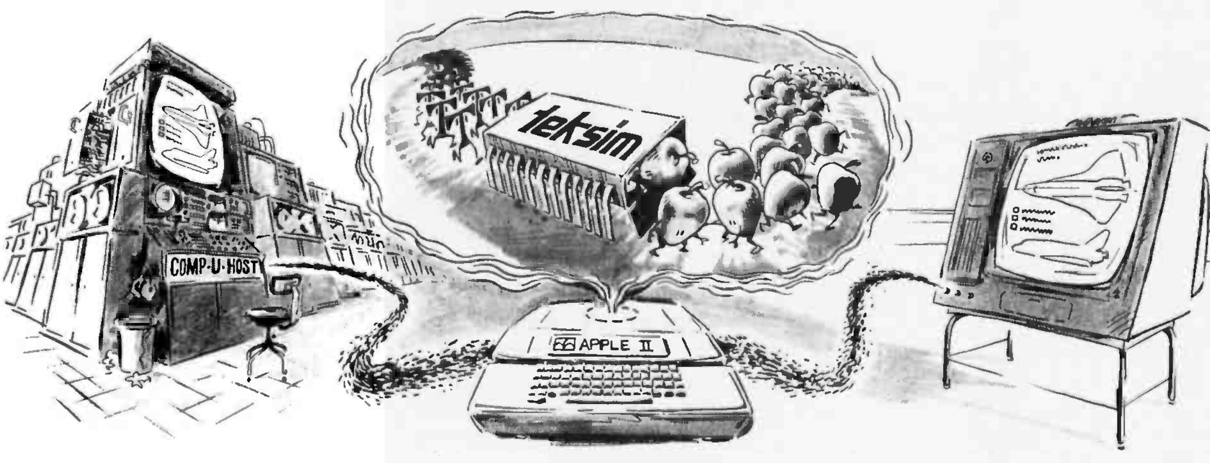

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Give Your Computer an Ear for Names

Tom Munnecke
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One of the major criticisms of the computer is that it is too literal (ie: unable to accept minor errors from fallible human operators). When the computer asks a question, if an answer is not *exactly* right the computer rejects it, even if the answer was *nearly* correct. The computer does not apply a human's reasoning ability to determine the intent of the operator. Instead, it works only with the exact response.

There is a technique which has been used since the turn of the twentieth century to retrieve names based on pronunciation, rather than their spelling. It is called the Soundex code, and was originally developed to search for names in the 1890 census files. The technique is to give each name a four-character code, consisting of the first letter of the last name followed by three digits representing the sounds found in the rest of the name. This code is then used to group together all names which "sound like" each other.

The Soundex code allows the user to enter a name in a form believed to be the proper spelling. The computer responds with a menu listing all sound-alike names, allowing the user to make a selection. If only one name is found, the computer could confirm the name identity and proceed. For example the user could misspell "Gonzales" as "Gonzalez"; "Smythe" as "Smith"; or "Andersen" as "Anderson." I amparticularly sensitive to this problem because my name (loosely pronounced "money-key") is regularly misspelled. Table 1 shows a sample of the misspellings, as collected from actual mail I have received during the last two years.

Name	Code
Munnecke	M520
Minnecke	M520
Munnuke	M520
Munneake	M520
Munneeke	M520
Municky	M520
Muneeck	M520
Monkey	M520
Muneick	M520
Munnick	M520
Monnecks	M521
Muuncake	M522
Munnedie	M530
Lunnecke	L520
Munnecle	M524
Euler	E460
Gauss	G200
Hilbert	H416
Knuth	K530
Lloyd	L300
Lukasiewicz	L222
Smith	S530
Smyth	S530
Smythe	S530
Smitty	S530
Gonzales	G524
Gonzalez	G524

Table 1: *Sample Soundex code for several names. The first fourteen names following the author's are misspellings of his name, actually found on mail, along with their respective Soundex codes. Notice that most of the misspellings reduce to the same Soundex code and could identify the correct name.*

Letters	Code Digit
b,f,p,v	1
c,g,j,k,s,x,z	2
d,t	3
l	4
m,n	5
r	6

Table 2: *Numeric single-digit codes that are assigned to letters from the corresponding groups as they occur in a name being encoded in the Soundex system.*

The exact use of the Soundex code varies greatly with the computer's file-management system. Some database management systems support Soundex codes directly; others require the programmer to structure the search logic. The program is easily modified to arrange sounds in groups other than as shown. Therefore, there are many modified versions of this technique in use around the country to account for local variations in names and programmer's whims.

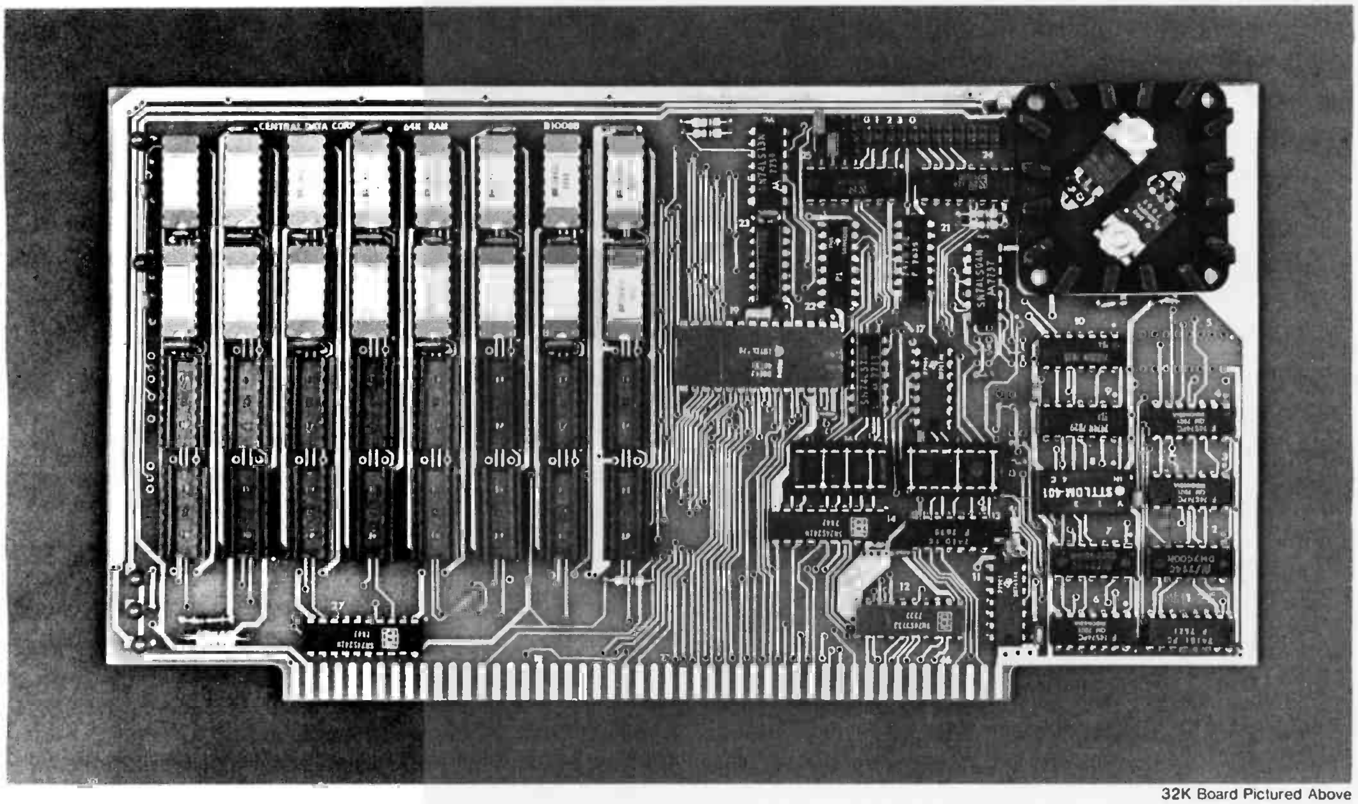
The user might see the Soundex routine working as follows (user input is italicized):

WHAT NAME: *SMITH*
SELECT ONE:
1. Smith, Jack 123 Main St
2. Smith, John 456 Central St
3. Smythe, Zachary 789 First Ave
Enter Choice:__________

If there is only one name with the sound, the computer might respond:

WHAT NAME: *SMITH*
John Smith, 123 Main St

This approach is only the most simple technique. It can be enhanced by adding the first initial of the first name, sex, birthdate, or other characteristic



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Listing 1: *Soundex program written in Microsoft BASIC for the Commodore PET. Table 3 describes variables used in the program.*

```
100     REM TEST DRIVER FOR SOUNDEX
110     INPUT "LAST NAME":N$
120     GOSUB 2000:REM EXECUTE SUBROUTINE
130     PRINT "SOUNDEX CODE =";S$
140     GOTO 100
2000    REM SOUNDEX ROUTINE TOM MUNNECKE 2/22/79
2010    REM RETURNS SOUNDEX CODE S$ FROM LAST NAME N$
2020    REM SEE KNUTH, "ART OF COMPUTER PROGRAMMING", VOL #3, P 391
2030    REM L$="  ": REM LAST SOUND
2040    S$=MID$(N$,1,1):REM START WITH FIRST LETTER OF NAME
2050    IF LEN(N$) < 2 THEN 2200:REM SKIP SHORT NAMES
2060    FOR I = 2 TO LEN (N$):REM FOR EACH REMAINING LETTER
2070    E$=MID$(N$,I,1):REM SELECT I-TH LETTER
2080    E=ASC(E$)-64:REM CONVERT A THRU Z TO NUMBER 1 THRU 26
2090    IF E > 26 OR E < 1 THEN 2160:REM USE ONLY LETTERS
2095    REM SELECT SOUNDEX CODE
2100    K$=MID$("0 1 2 3 0 1 2 0 0 2 2 4 5 5 0 1 2 6 2 3 0 1 0 2 0 2",E,1)
2110    REM        A B C D E F G H I J K L M N O P Q R S T U V W X Y Z
2120    IF K$=L$ OR K$="0" THEN 2160:REM SKIP TWO CONTIGUOUS SOUND-ALIKES
2140    S$=S$+K$:REM BUILD UP SOUNDEX RESULT
2150    IF LEN(S$)> 3 THEN 2200:REM ONLY FIRST 4 SOUNDS
2160    L$=K$:REM SAVE LAST SOUND
2170    NEXT:REM DO NEXT CHARACTER IN NAME
2200    S$=LEFT$(S$+"000",4):REM PAD TO RIGHT WITH ZEROS AND SHORTEN TO 4 CHARS
2210    RETURN
2999    END
```

to identify the person with greater accuracy.

Constructing the Soundex Code

The technique for constructing the Soundex code is found on page 391 of *The Art of Computer Programming, Volume 3: Sorting and Searching* by Donald Knuth (published by Addison-Wesley, Reading MA). The four steps in generating a Soundex code are:

1. Retain the first letter of the name, and drop all occurrences of a,e,i,o,u,w,y,h and q in other positions.
2. Assign *group numbers* to the remaining letters after the first according to the scheme given in table 2.
3. If two or more letters with the same code are adjacent in the original form of the name

Basic In A Nutshell

Name: Step-By-Step
Vendor: Program Design, Inc., 11 Idar Court, Greenwich CT 06830
Price: $49.95
Purpose: Teaches how to program a TRS-80 using BASIC
Documentation: Outstanding
Loading: OK—Level 6, not critical
Implementation: This is a case of a BASIC program that teaches BASIC programming. It starts out with the assumption that the student only knows how to turn the TRS-80 on. Three cassette tapes are mounted in the cover of a loose-leaf notebook that also contains supplementary information frames. The course is divided into ten two-part lessons. From a simple PRINT "HI" through arrays and graphics to complex programs, all of the Level II commands and statements are exercised.

The instruction method consists of explanation, example, trial and testing. Commands and statements are presented and explained, examples are shown both on the screen and in the notebook, and then the student is presented with some problems to solve using the BASIC elements under discussion. If an incorrect answer is given, two more tries are allowed, and then the correct answer is displayed. Each lesson ends with a test that is administered and scored by the computer. The results are then entered into the student's progress chart. More comprehensive examinations are given at the end of Lesson 5 and at the end of the course.

Suitability: This is the kind of educational programming that personal computing needs more of. The student (my teenage son) learned much more quickly than I could have taught him, and at his own pace. However, this course isn't just for youngsters but for anyone who wants to be able to program effectively using the BASIC language. In a household where there isn't anyone to do the teaching, this course would be especially useful. I'd like to see a similar course for assembly-language programming.

Other software available from the same vendor: IQ Builders (four different kinds), Memory Builder and Story Builder.

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80 Microcomputing, February 1980

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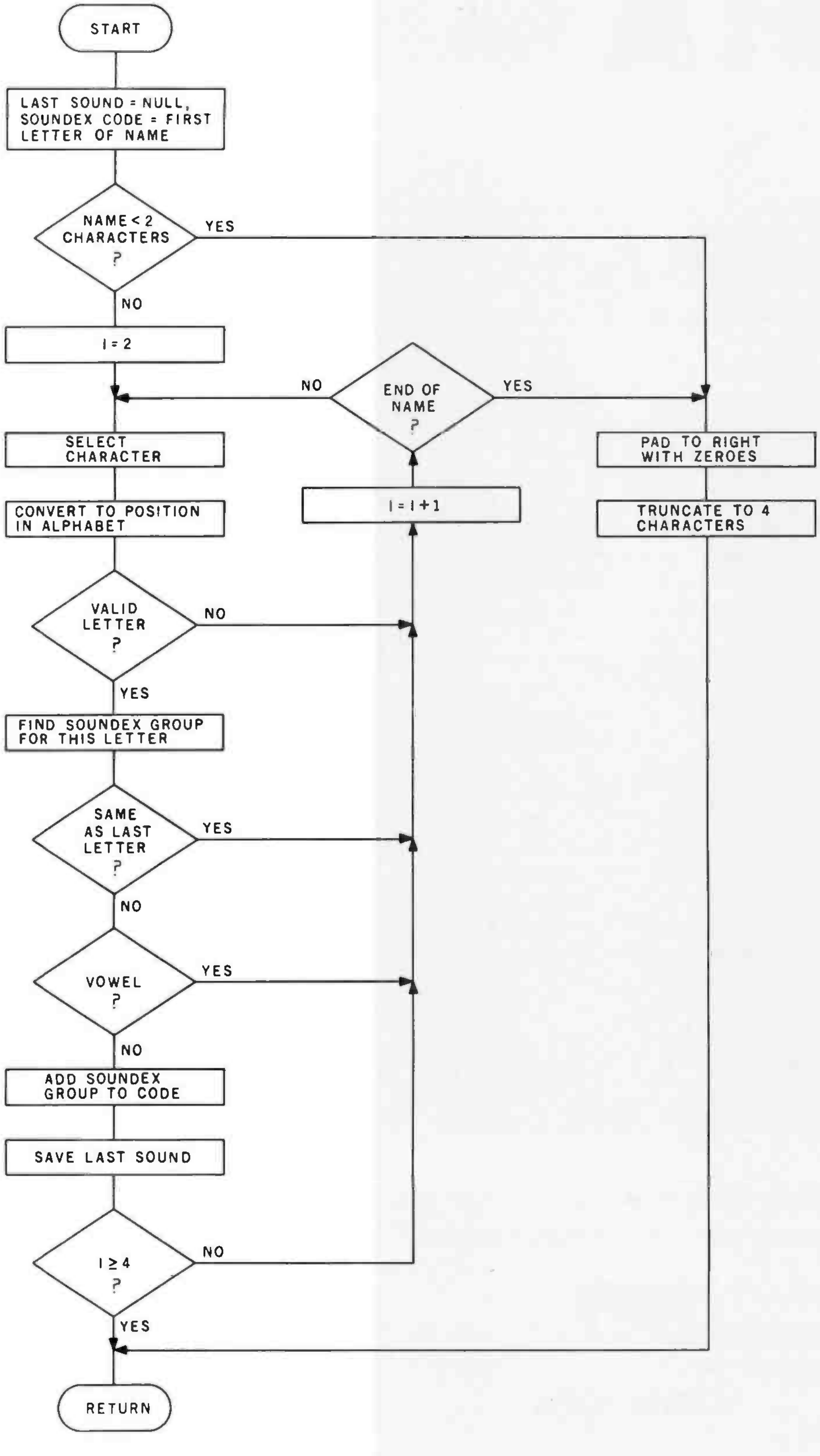


Figure 1: *Flowchart of the Soundex algorithm subroutine.*

(before step 1), omit all but the first.

4. Convert the name to the form *letter, digit, digit, digit* by adding trailing zeroes (if there are less than three digits), or by dropping rightmost digits, if there are more than three.

BASIC Program

Listing 1 shows the Soundex code generating subprogram that constructs the encoded form from a last name. It was written and tested on a Commodore PET 2001 computer, but it should work on any computer using Microsoft BASIC. It should work on other BASICs which have LEFT$, RIGHT$, and MID$ functions, and use "+" for string concatenation.

Figure 1 shows the flowchart describing the program's operation. Line numbers on the flowchart correspond to the BASIC line numbers in listing 1. The program is separated into two parts: the Soundex routine, starting at line 2000, and a test driver starting at line 100. The driver is used to ask for a name, invoke the Soundex generator, then print the results. It will be replaced by your program logic for filing and retrieving. The Soundex generator in line 2000 accepts as input the variable N$, representing the last name to be converted. It returns S$, the Soundex code for N$.

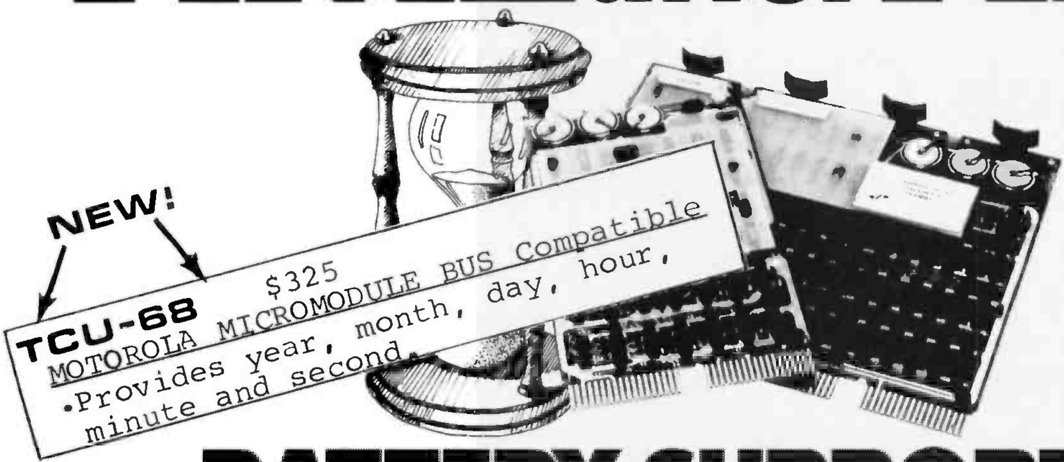
The only tricky part of the program is contained between lines 2080 and 2110. Instead of testing each letter individually, as shown in the original technique above, the program converts the letter to a number from 1 to 26, representing its position in the alphabet. It then uses this number to index a character string, containing the group codes for each letter. The comment below the index line at line 2110 documents this technique, and provides a reference in case the codes need to be changed.

The Soundex subroutine may be incorporated into programs that require the computer to understand user input. The addition of a Soundex routine can increase the usefulness of a computer. ■

Input		
N$	—	Name to be coded
Output		
S$	—	Soundex code of N$ (form: letter,digit,digit,digit)
Temporary		
I	—	Character position in N$ under consideration
E$	—	Ith Character in N$
E	—	Alphabetic sequence of E$
L$	—	Last sound during evaluation

Table 3: *Variables used in the Soundex program.*

TIME after TIME



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DIGITAL PATHWAYS

Circle 120 on inquiry card.

The Club Computer Network

Joe Kasser
11532 Stewart Ln
Silver Spring MD 20904

Does a club need a computer network? What are its uses? What are the advantages of having such a network?

This article attempts to answer these questions and provide ideas on the techniques used in implementing the network.

Basic Communications Needs

An important aspect of any hobby is communication. The sharing of information and experiences can add a great deal of enjoyment and save much time. If the techniques used to solve some problem are made available by the solvers to others, the recipients of the solution can advance the state of the art. This is done by building upon the foundations developed by the original solvers, rather than by rebuilding the same foundations.

In the computer field, communications fall into two similar but distinct categories: the exchange of personal messages and the exchange of computer data (programs or data bases).

Personal messages may contain any plain language text. Computer data may contain programs, data bases, and instructions for processing files.

About the Author

Joe Kasser is vice-president of the Chesapeake Microcomputer Club, director of information and publicity of the Radio Amateur Satellite Corp (AMSAT), and editor of ORBIT. He has worked with microcomputers professionally since 1975, and has built an 8080-based, S-100 computer system which served as the prototype for the club's construction project. He has contributed other articles to BYTE, including "AMSAT 8080 Standard Debug Monitor" (September 1976, page 108, with Richard C Allen), "The Sky's the Limit" (November 1978, page 48) and "The AMSAT-GOLEM-80" (September 1979, page 182).

Computer data comes in many forms. In the personal computer area, data may be on paper tape, cassette tape, or floppy disk. If it is on cassette, it may be in a digital saturation format or some modulated audio format. It may also be recorded at one of several data rates.

If data is on a floppy disk, the disk may be soft-sectored or hard-sectored. Data may be on 5- or 8-inch disks, which may be single or double density, single or double sided. The disk format may be compatible to a disk operating system such as CP/M or North Star, or it may not.

Most computer users do not have the means for reading or writing all of the different types of off-line storage media. Thus, two users who wish to share software may have what is known as a "media incompatibility problem."

A typical example occurs in the Chesapeake Microcomputer Club (CMC). Two members own 8080 or Z80-based systems, each running the Digital Research CP/M disk operating system. One member, however, uses 8-inch soft-sectored disks, while the other uses a North Star system (5-inch hard-sectored disks). They have no compatible medium such as tape. How then are they to share computer files?

The club is spread out over a wide geographic area. Several of the officers require access to the club roster or membership list. Currently the list is kept by one officer who has to update it, see that labels are printed for mailings, and send physical copies of the list to the other officers. Since officers may live 30 to 50 miles apart, the telephone and postal services are the only practical method for information exchange. There must be a better way.

The club has a need for disseminating information. Reports concerning main meetings, chapter meetings, group purchases, surplus information, and special interest groups have to be made available to the membership. Currently the information is passed out at meetings and through the mails by a monthly newsletter. Is there a better way?

Many of the members possess their own computer systems. The degree of sophistication ranges from a simple KIM-1 to a system with dual disk drive, large amounts of memory, and line printers. A number of members have become involved with the club computer project and the group-purchase plan for equipment. Each one of these systems is in a different stage of development. Many people are finding that their system cannot perform the tasks that they wish it to perform, because several system components (such as extra memory or disk storage capability) are lacking for one reason or another. Perhaps the capital outlay involved is not available, or they are waiting for deliveries to take place.

When contemplating the purchase of additional hardware and software, decisions involving hundreds of dollars must be made, sometimes with little factual information. At club meetings members can discuss their requirements and experiences, but that just results in acquisition of information about how a particular item of computerware works in someone else's environment and how it meets *his* requirements.

It would be nice to be able to get together with a friend and gain hands-on experience of the way that a computer system component performs in one's own environment before purchasing it. Visiting friends

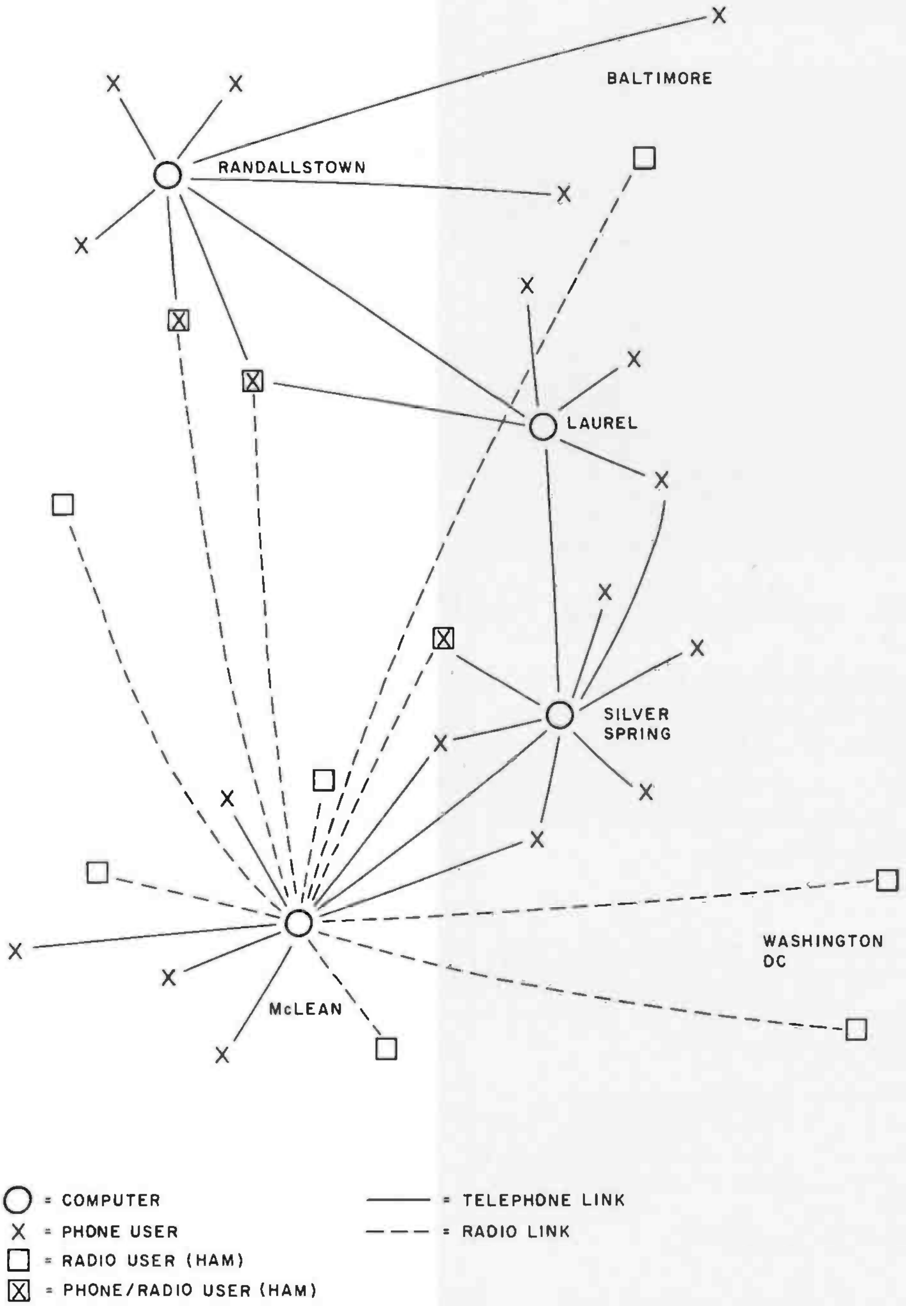

Figure 1: *Diagram of sample telephone and radio-data transmission links in a typical club computer network. Several computers form nodes in the network. Solid lines indicate telephone links; dotted lines indicate links through a 2-meter band amateur radio repeater system (at the same location as one of the computers). Communities identified are located in northern Virginia and in Maryland (except for Washington DC).*

and using their systems can provide this facility, but it is inconvenient, especially when a long session is planned or the traveling distance is great. There must be a better way.

Basic Network

There *is* a better way. It is called *a club computer network*. All club members can have access to it. It may be centralized or distributed, but it will provide a service to the club members. Access may be via the telephone line or via amateur radio-teletypewriter (RTTY) circuits. Each access method has its own advantages and disadvantages.

An example of such a network is shown in figure 1. It incorporates both radio and telephone links. It also allows for a number of computers in the system. It is spread out over a relatively wide geographic area. One computer may be accessed either via a 2-meter FM radio-teletypewriter repeater (operated by the Amateur Radio Development Association, AMRAD, using the frequencies 147.81 and 147.21 MHz), or via the telephone line. The other computers are operated on behalf of the Chesapeake Microcomputer Club Inc by various members. Note that this area-wide operation is necessitated by the geographic dispersal of the membership of the two clubs.

The central computers are located so that at least one computer is within local telephone-dialing range of each club member. Several members may be within local dialing range of more than one. If one machine in the network is down, or in use at any particular time, these members can try to access another computer.

The radio link can be used by virtually any amateur radio teleprinter station in the area that is equipped for 2-meter FM operation. Of course, *any* member of the club can access any computer by making a long-distance telephone call.

Data is collected in each computer for remote retrieval at a later time. If the data in one machine is addressed to a user outside the local telephone area, the data is automatically sent to the computer in the distant area in the late evening, when long-distance telephone rates are lowest. This inter-computer transfer takes place once per night per machine in a predetermined sequence to transfer the maximum number of messages with the minimum number of calls.

Link Types

Consider first the characteristics of the radio links. Many amateur radio operators already use noncomputerized automatic-starting radio-teletypewriter equipment for receiving message traffic. A computer network for message handling is a logical successor to these existing autostart networks.

The existing noncomputerized network works as follows. All stations monitor the same frequency. Messages are sent blind; when a message is originated into the network, the sender does not know for certain if the destination station is

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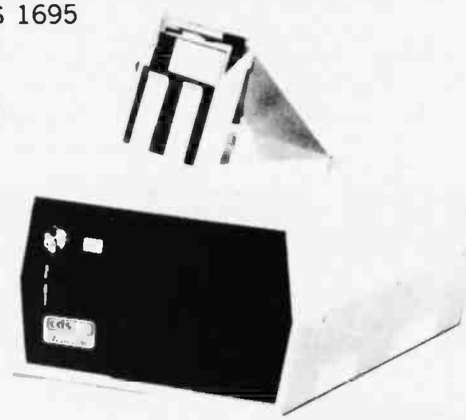

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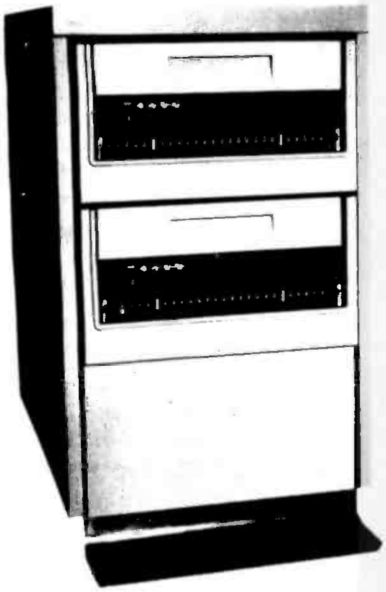

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monitoring the frequency, unless 2-way contact is first established. In the evening, or during weekends, this may not pose much of a problem, because the probability of someone being at home is great. However, during the working day, that probability decreases. Thus, if contact cannot be established directly, the message can still be *sent*, but there is a probability that the destination receiver will not be on line, and the message will be lost.

If, however, the message can be stored in a central computer by the sender, and retrieved later by the receiver, the probability of successful transmission of the message from sender to receiver is almost certain. The addition of a computer therefore becomes an asset to the network.

If several stations in the network have computers capable of answering back to the sender, the utilization of the computer may be reduced. A sender can put out a direct call. If an answer is not received (indicating that the destination is not on line or monitoring at the time), the message can either be transmitted to the computer for storage, or held and transmission attempted again at a later time. It is also possible for the assignment of which network computer will perform the store and forward operation to be rotated among the various member-station computers on basis of availability, as long as the network computer has a distinctive identification.

With a radio network set up in this way, anyone equipped either with simple radio-teleprinter equipment or with sophisticated computer equipment may make use of the full network message storage and forwarding capabilities. This concept of allowing minimally equipped stations to access the network requires that simple techniques be used for data transfer. These include 5-level ("Baudot") or ASCII plain language text, a control language that is readable by both man and machine, with minimal error checking. The advantages of more sophisticated techniques mean that many people will want to use them. That leads to a hierarchical concept of the network utilization. This will be discussed later.

The disadvantage of the radio network is that since everyone is on line, the privacy level is zero. Therefore, data that is not intended for public knowledge cannot be passed over the network. For this reason, mailing lists and other confidential club data should not be passed over the radio link. *[Also, FCC regulations require that* no *message traffic pertaining to any business or commercial activity may be transmitted by an amateur radio station...*RSS*]*

Use of the telephone line for gaining access to the computer limits the number of users that can be on line at the same time. One great advantage of the telephone line is security. The connection between the user and the computer is private. Mailing lists can be accessed and changed remotely without compromising the security of the data, provided that only authorized users are allowed access to these data files.

System Implementation

Bringing up the network for the first time can be simple or complex. One method is to install a computer equipped with dual floppy-disk drives, 32 K bytes of memory, and the phone line, and make it available 24 hours per day. It is an expensive method, especially when the demand

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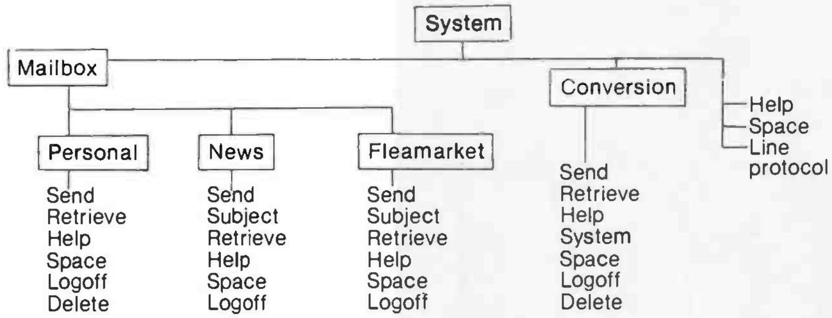

Figure 2: *Hierarchy of software modes in the club computer network software. Names of program routines are enclosed in boxes. Commands available with each program are listed below.*

for such a service has not yet been demonstrated in the club.

A second method is to bring the service on line gradually, using equipment belonging to club members, and then put together a club system as club finances allow. This method has the advantage that the cost can be spread out over a period of time, but does have a disadvantage because there will be many intervals during the early stages of the network implementation when the system is not available.

The network can be started by one or more club members making their personal systems available. On the radio link, there will be no noticeable difference with the different computers, since they should all answer to the same call sign, and the user need not know which machine is storing his traffic. In practice each computer will also transmit its own station call sign as required by law.

Telephone access is a little more difficult, because a list of numbers must be made available to the network members, and a rule must be established for dialing the computer. An example of such a rule is that if the computer does not answer by the second ring, dial another number.

When the system is first put into use, it will be lightly loaded. It can thus be used for secondary purposes apart from the message storage or media transfer applications. Club members will have a chance to use the sophisticated system and to play with it. The availability of any single computer during the early stages may be intermittent: since it is the personal system of a club member, it will be available for club use only when the owner is not using it. This unreliable accessibility will encourage members to upgrade their systems as fast as possible for their noncommunication uses. However, the system as a whole will have a greater reliability, since there is a good probability that at least one computer will be available when one is required.

Using the Telephone Link

The typical telephone communication system operates at a data rate of either 110 or 300 bits per second (bps), allowing the use of simple Bell 103-compatible modems. In order to set the data rate for a transmission, each user must transmit a carriage

```
CMC NETWORK. ENTER LOGON: - G3ZCZ
G3ZCZ LOGON IN PROGRESS AT 1115 ON 6 NOV 1978
4 MESSAGES
READY MAILBOX
MAILBOX READY HELP
CHOOSE BETWEEN 'SEND, RETRIEVE, HELP, SPACE, LOGOFF'
MAILBOX READY SPACE
DISC SPACE = 25K
MAILBOX READY SEND
DESTINATION? WB4APR
INPUT: —        BOB, WE HAVE TO DISCUSS THE RADIO PROTOCOL. CALL ME WHEN YOU HAVE A MOMENT, BETWEEN 9 AND 11
                PM ANY NIGHT EXCEPT FRIDAY. [control-Z]
MESSAGE ACCEPTED
MAILBOX READY RETREIVE
RETREIVE IS NOT VALID
MAILBOX READY RETRIEVE

 MESSAGE        SOURCE          DATED
    1           WB4APR          1 NOV 1978
    2           CMC 105         3 NOV 1978
    3           TERRY FOX       5 NOV 1978
    4           G8BTB           5 NOV 1978

MAILBOX READY RETRIEVE 2
MESSAGE READS:      BRING THE DOCUMENTATION ON THE GLOOP BOX TO THE MEETING. FRED.
MAILBOX READY
```

Figure 3: *Sample interaction between the author (G3ZCZ) and the Chesapeake Microcomputer Club-Amateur Radio Development Association (CMC-AMRAD) computer system. Characters sent by the system are shown in regular type; those typed by the user are shown in boldface type. Note that when the "RETREIVE" command (a misspelling) is entered, an error message is generated by the system.*

return character so that the computer can set up the correct data rate. Once the data rate is established, the computer sends out a sign-on message and asks the user to log in with an identification code. This identification can be a membership number, an amateur radio call sign, or some arbitrary name. It is limited to a length of eight characters. The computer will then indicate the presence or absence of any personal messages addressed to the user that has just logged in.

The software in each computer is identical in behavior and is organized in a structured top-down approach as shown in figure 2. The user has a choice of programs as shown that perform the various functions. Various commands are associated with each program as listed. Consider each program and mode in turn.

The *mailbox* program is designed to enable club members to send short messages (up to 256 characters) to each other. The messages are in plain language. The response to a SEND command is to prompt the user with DESTINATION? Upon entering the identification code of the destination, the user is prompted to send the message and terminate it with a control-Z character. Should more than 256 characters be entered, the entire message will be rejected. This discourages long messages.

The response to the RETRIEVE command is to list the sender identification of each message in the system awaiting the user.

A sample user session is shown in figure 3. The computer output is shown in regular type, the user input in boldface type.

The other messages may be retrieved in turn. The RETRIEVE command has the following characteristics: If followed by a carriage return, it lists all messages. If followed by a 0, it lists all messages. If followed by a number, it lists the corresponding message.

Identification numbers are assigned to the messages only to allow the user to retrieve them. The numbers are reassigned as messages are deleted.

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Deletion of messages is allowed by the system under restricted conditions. Only the system manager, the sender, or the retriever can delete messages. Each user is assigned a password that must be entered prior to a DELETE command. This allows some degree of security. Messages will be deleted by the system manager periodically, depending on the storage requirements of the system.

In the *news* and *fleamarket* modes, updates are handled by a single club member designated for that duty. All messages for input to the system are routed to this person for scanning before being placed on the system. This is to keep the system from being cluttered up with undesirable messages. Updates of these messages take place as time permits, with a maximum delay time of one week.

The *conversion* program is designed for exchange of data between different media. One club member desiring to receive a data file from another will arrange for the second member to put the file into the system for retrieval within hours. The expected life of a file in the conversion mode is about 24 hours. Conversion uses a different protocol than the mailbox mode. Since long files are being exchanged, the data flow has to be stopped from time to time to allow disk read and write operations. A full-duplex mode is used.

The maximum message length of 256 characters applies in all modes except conversion. Messages with more than 256 characters are rejected in their entirety. This encourages brevity. A rejection message is printed by the computer to the sender in the case of a message rejection. A user who has to retype messages will soon get the idea.

Several existing network systems carry a large number of undesirable messages. We hope to minimize them in the CMC-AMRAD network. Any user trying to enter unwanted messages may have them rejected by the system manager.

Data Complexity Levels

Data may be transmitted over a link at one of several levels of complexity of internal organization. The basic level (level 0) is plain ASCII-encoded text in half-duplex mode. Level 1 is a simple ASCII-based, full-duplex mode developed by Tim Pugh. Level 2 is an emulation of the PCNET (personal computer network) protocol. Level 0 is used by anyone in talking to the computer during execution of any user program. Level 1 may be used in the conversion mode, while Level 2 is used for intercomputer data exchange. Any properly equipped user can request any level when he logs onto the system.

Any club member having an *answer-mode modem* can run the basic network system software on his or her machine. An extension can be made to the system to allow access to the disk operating system so that other club members can play with the other software available on the machine.

Radio Restrictions

Mailbox and news are the only categories of data exchange available via radio links. Conversion-mode data may contain binary or other unusually coded files, and fleamarket may contain advertisements; radio transmission of both of these classes of messages is forbidden by law.

The procedure for logging onto the system is different from the one used over the telephone. Half-duplex mode is employed when using a single-band repeater, such as the 147.81/147.21 MHz AMRAD machine. If the inputs and outputs were on different amateur frequency bands, full-duplex operation would be easily achievable. In order to avoid the requirements for duplex exchanges and to reduce the amount of information exchanged, the modified Q *code* is employed. See my article "The Sky's the Limit: Use Ham Radio Bands for Intercomputer Communication" (November 1978 BYTE, page 48), for a more complete discussion of the use of these Q codes.

[The Q code is a system of 3-letter abbreviations that all begin with the letter Q. Various Q codes are used during Morse-code radio transmissions to speed up message exchange. An adapted set of Q codes is used for computer network communication... **RSS**]

Any amateur can log into the network and receive a reply from any on-line computer that has a message for him or her. Thus, users without computers can store their messages in the network computer; those with computers can leave messages on their own machine for later remote retrieval. Possible contention interference (from more than one machine simultaneously trying to communicate over the network) can be overcome initially by employing a different time-delay response characteristic for each computer in the network (both user and system computers).

The radio link can also be used for long-distance links between the club network and other club networks. Again, see "The Sky's the Limit" for a more complete discussion. ■

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As far as I know, the ELF is the only microcomputer that has often been built from scratch by hobbyists without using a predesigned printed-circuit board. There is *no* better way to learn microprocessor hardware than to buy a handful of parts and wire-wrap all of the connections. In ironing out your mistakes, you will become familiar with every processor timing signal, every kink in every system timing diagram, and every little architectural quirk that can grow up to be a big bug in later programs. It is a rigorous education, I promise you, but an excellent one.

Then RCA released the CDP1861 video-display-controller integrated circuit for sale, and suddenly the ELF could do something no comparable computer could do for triple the price. With the CDP1861, the ELF displays a bit-map of 1024 bytes of memory on a video screen (in black and white), with no hardware needed except the CDP1861 and several resistors, and with software consisting of a 30-byte interrupt routine.

This development was not purely a gift to hobbyists, of course. The CDP1861 formed the heart of RCA's Studio One home video game. In such games cost is probably the most important factor. Video-game-type graphic displays are now easily done on the ELF. The fourth article in the ELF series ("Build the PIXIE Graphics Display," Joseph A Weisbecker, *Popular Electronics*, July 1977, page 41) outlined the hardware required and included a simple test program, but it was up to hobbyists to come up with video software to make the ELF earn its keep.

The Video Doodler program presents a winking cursor in the upper left-hand corner of the screen. By actuating toggle switches, the cursor can be made to move horizontally, vertically, or diagonally. As it moves, it either leaves behind a trail of white dots against the black background, or it "eats" previously written white dots and lines back to blackness. Once you fill the screen, one push of the INPUT switch wipes it clean again.

Memory Requirements

The only problem is the program's size. Within the limits of a typical ELF one-page memory system, there is no room left in memory after you toggle in the program to do any drawing on the screen. The only way out of this problem is to expand memory to at least two 256-byte pages. If you shop wisely, you can do this for less than $9.00. Adding another page of memory requires only two additional 2101 static memory chips and a CD4042 complementary metal-oxide semiconductor (CMOS) latch. Figure 1 details an ELF two-page memory system.

If you do not intend to add much more memory beyond two or three pages, you might consider replacing

Text continued on page 218

About the Author

Jeff Duntemann works for Xerox Corp. He has built a small robot (named Cosmo) that he controls with his computer, and enjoys amateur radio operation (as KB2JN). His writing is not confined to technical articles; he has had a science fiction story published in Isaac Asimov's Science Fiction Magazine.

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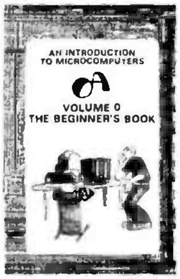

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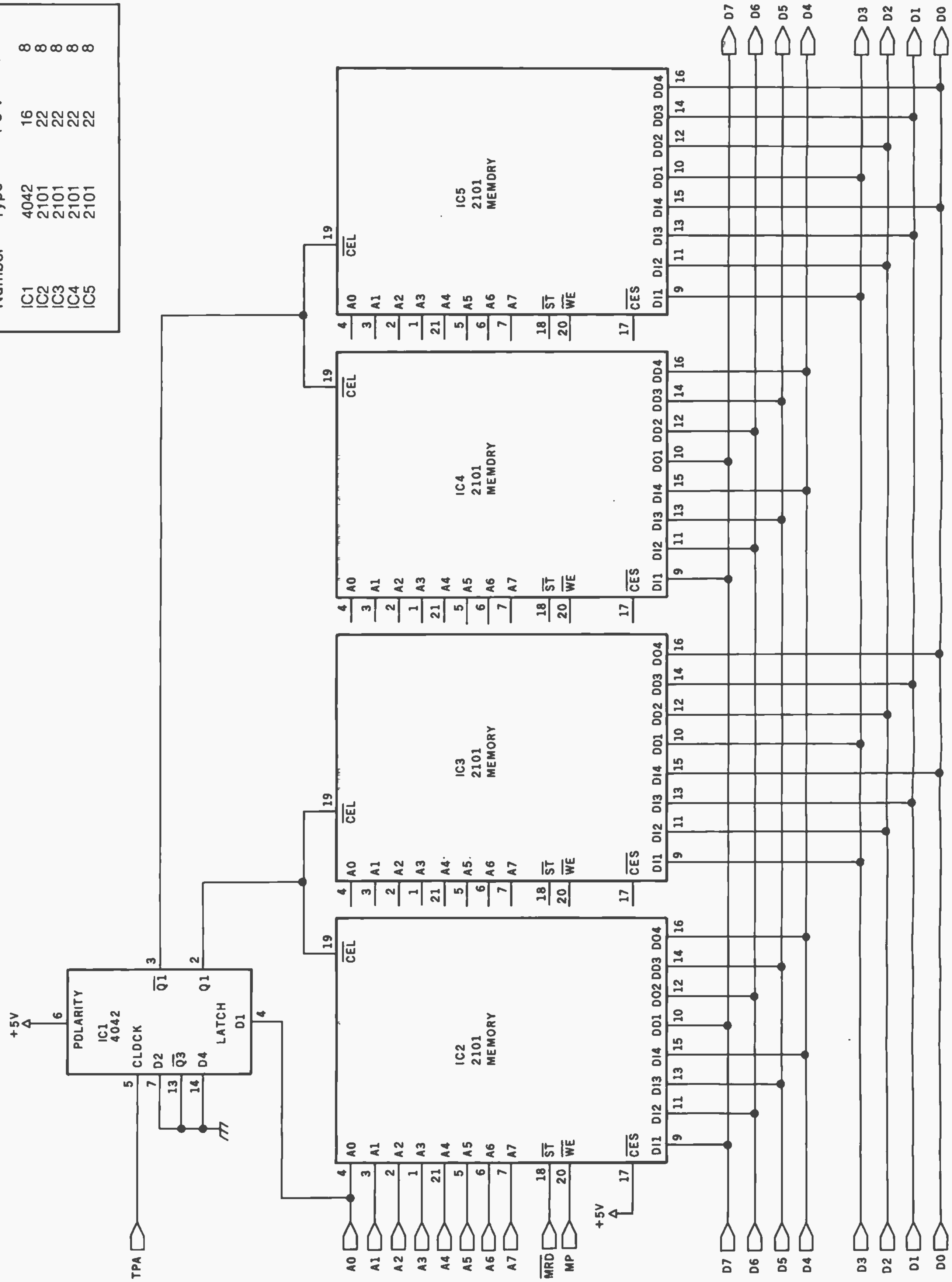

Figure 1: *Schematic diagram of a two-page programmable-memory system that can easily be added to a COSMAC ELF microcomputer. Pins 17 and 22 of the memory parts should not be connected together. Instead of 2101 memory devices, it is possible to substitute CMOS 5101, 74C920, or CDP1822CD parts. Use of complementary metal-oxide semiconductor memories enables the use of batteries to retain data in memory even when the main power supply is shut off.*

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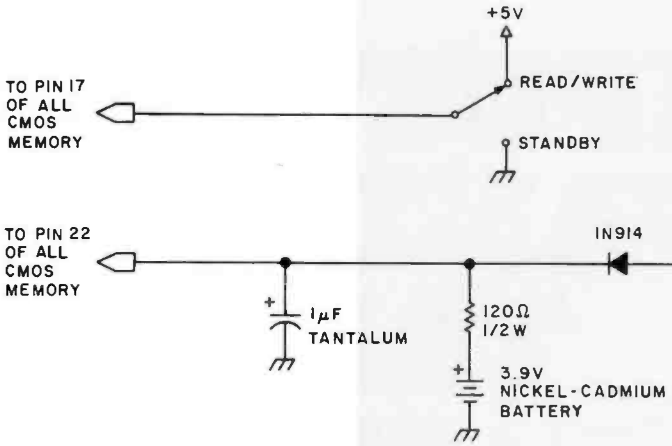


Figure 2: *Memory data-retention circuit for CMOS memories. Do not use this circuit with a 2101-type memory. The nickel-cadmium battery cells charge during normal operation, and thereafter maintain data in the memory when main power has been turned off.*

Text continued from page 214:
your 2101 devices with CMOS 5101 or CDP1822 memory. A small 3.9 V battery can allow data to be retained in CMOS memory even when the main power is off, thus keeping you from facing the exasperating job of toggle-loading 195 bytes every time you want to show off the Doodler.

If you can locate a 3.9 V nickel-cadmium battery, the circuit in figure 2 can be built and then forgotten about. The ni-cad will charge while the power is on, and keep memory alive when power is off. If you operate your ELF at least a few hours per month, the battery will never fully discharge.

Register Use

The Doodler program makes heavy use of the COSMAC general-purpose registers. A register-use summary is given in table 1 to keep everything straight while you are trying to understand the program's operation.

Where Is the Cursor?

It takes two pointers to specify a cursor position on the screen. The *byte pointer* is the memory address of a single byte somewhere among the 256 bytes displayed on the screen.

The *bit pointer* is a byte stored in half of a general-purpose register. Only one bit of this byte ever contains a binary 1. This bit represents the position of the cursor within the byte indicated by the byte pointer.

The Doodler actually has two sets of pointers for its cursor. The permanent pointers contain the actual position of the cursor at any given time. The temporary pointers are modified during each scan of the toggle switches.

The toggle switches are read and separately tested by shifting bits out of the D register (COSMAC's accumulator). Each of the first five switches controls a program function. If the first toggle switch is actuated, the temporary bit pointer is shifted one bit to the right. If during this shift the bit crosses over into the next byte, the temporary byte pointer is incremented by one.

Actuating the second toggle switch shifts the bit pointer to the left, and decrements the byte pointer if the bit crosses the border into the next byte leftward. The third toggle switch adds the hexadecimal value 08 to the byte pointer. This does not affect the

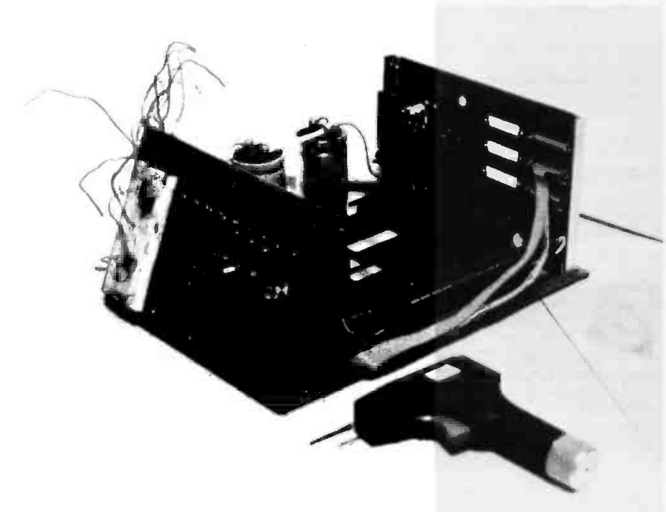


Photo 1: *The author's homebrew COSMAC computer system. It contains 2560 bytes of memory and uses a full 16-bit address display. Important processor and input/output signals are brought out through the front panel for ease in breadboarding.*

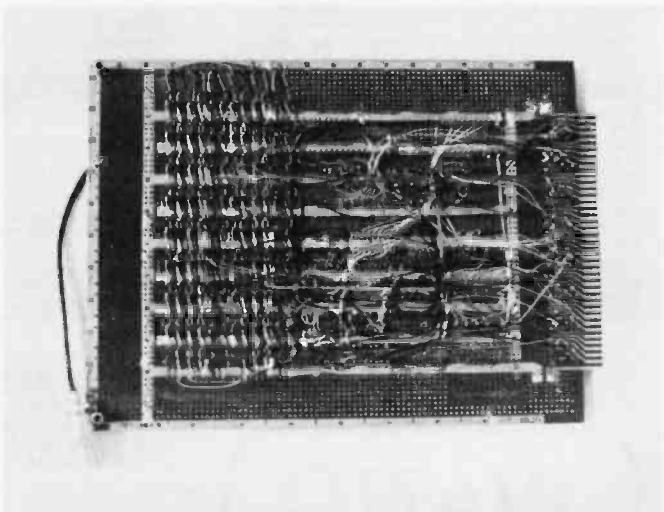
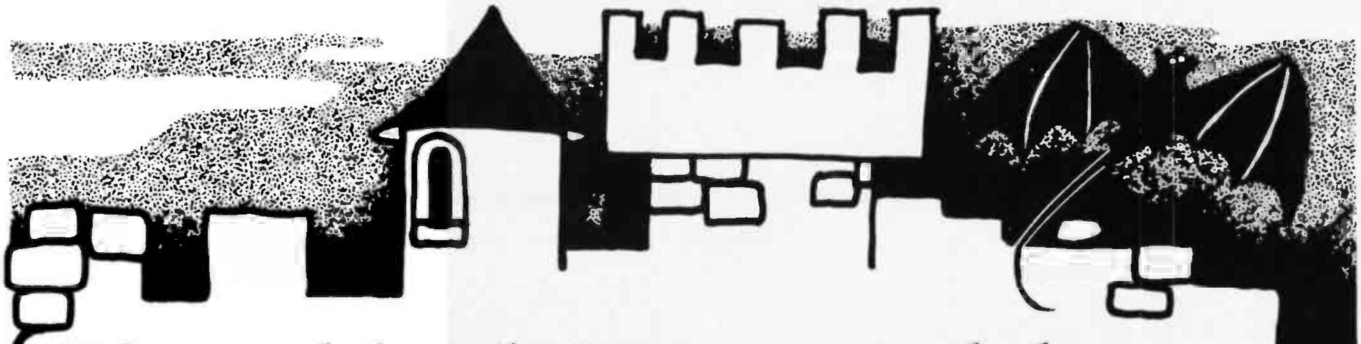


Photo 2: *Bottom side of the processor board. Six weeks of evening work with an OK Tool Hobby Wrap wire-wrap gun and 150 feet of wire were needed to complete the connections.*



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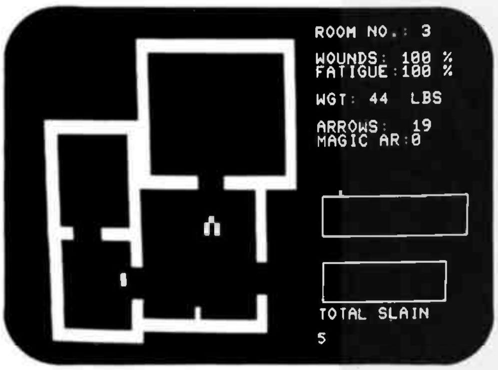

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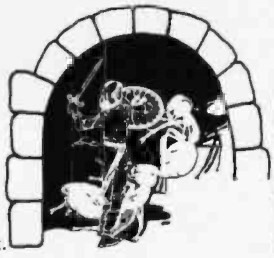

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cursor's horizontal position (the bit pointer remains the same), but the cursor is moved down one row. Similarly, the fourth toggle switch subtracts hexadecimal 08 from the byte pointer. This makes the cursor move one row upward.

Only after the toggle switches have been completely scanned are the values in the temporary pointers transferred to the permanent pointers, and the cursor moved to its new position. This makes motion on the diagonal possible without visible up-and-across motion on the way to the new position. If all four toggles are actuated, the cursor does not move. The four motions cancel one another before any information is transferred to the permanent pointers.

The fifth toggle switch determines whether the bit written into the cursor position will be a white dot or a blank space.

Register	High Byte	Low Byte
0	Direct-memory-access pointer	Direct-memory-access pointer
1	Interrupt program counter	Interrupt program counter
2	Stack pointer	Stack pointer
3	Main program counter	Main program counter
4		
5	BNKWRT program counter	BNKWRT program counter
6	DOTWRT program counter	DOTWRT program counter
7		
8	DELAY program counter	DELAY program counter
9	Temporary byte pointer	Temporary byte pointer
A	Inter-shift D storage	Temporary bit pointer
B	Permanent byte pointer	Permanent byte pointer
C		Permanent bit pointer
D	Blanking pointer	Blanking pointer
E	Delay-timing constant	Delay-timing constant
F		

Table 1: *Use of COSMAC 1802 16-bit registers by Video Doodler program.*

Operation of Subroutines

Two subroutines accomplish the transfer of information from temporary to permanent pointers and the final writing of the cursor bit onto the screen. If the fifth toggle is actuated, subroutine BNKWRT does the job and writes a 0 (blank) into memory at the cursor position. If the fifth toggle is not actuated, the job is done by DOTWRT, and the cursor leaves a white dot behind in memory and on the screen.

A third subroutine, DELAY, slows the process down so that you can direct the cursor intelligently on the screen. The execution time for DELAY (and thus the speed at which things happen) is determined completely by the constant that begins at memory location 0046. You increase or decrease this constant to slow the program or speed it up.

Text continued on page 224

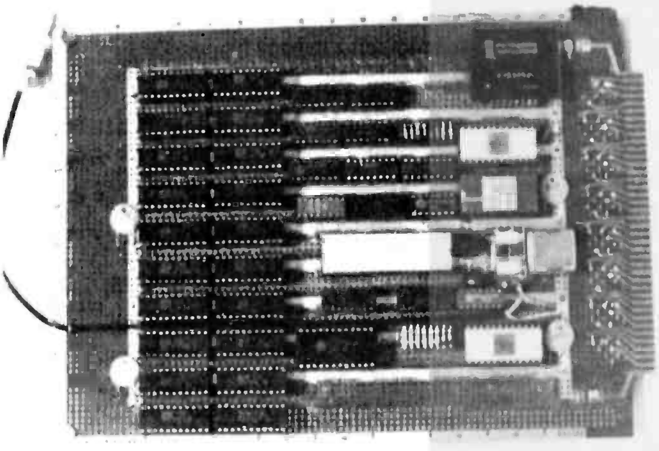

Photo 3: *Component side of the processor board. The video signal is brought off the board by the miniature 75-ohm coaxial cable.*

Photo 4: *Display produced using the Video Doodler. The isolated dot at the center right is the winking cursor.*

Listing 1: *Video Doodler program in machine code for the COSMAC ELF.*

Address	Hexadecimal Code	Comments
00	F8 00 B1 B2 B3 B5	Initialize high-order registers
06	B6 B8 A9 AB	and byte pointers
0A	F8 01 B9 BB BD	
0F	F8 80 AC AA	Initialize bit pointers
13	F8 28 A1	Initialize interrupt PC
16	F8 FF A2	Initialize stack pointer
19	F8 66 A3	Initialize MAIN PC
1C	F8 5A A5	Initialize BNKWRT PC
1F	F8 4F A6	Initialize DOTWRT PC
22	F8 45 A8	Initialize DELAY PC
25	D3	Begin executing MAIN PC
	INTERRUPT	
26	72 70	Restore D, X, & P
28	22 78 22 52	Push P, X, & D onto stack
2C	C4 C4 C4	NOP s for sync delay
2F	F8 01 B0 F8 00 A0	Re-point R0 to display page
35	80 E2	Prepare for first DMA cycle
37	E2 20 A0	DMA reset
3A	E2 20 A0	DMA reset
3D	E2 20 A0	DMA reset
40	3C 35	Test for refresh done
42	30 26	Go to return
	DELAY	
44	D3	Return to MAIN
45	F8 07 BE	Load timing constant into RE
48	2E	Decrement RE
49	9E	Load RE.1 into accumulator
4A	3A 48	Loop again if not done
4C	30 44	Go to return
	DOTWRT	
4E	D3	Return to MAIN
4F	89 AB	Update byte pointer
51	8A AC	Update bit pointer
53	EB	X=B
54	F1	Combine bit pointer & screen via OR
55	5B E2	Write dot to screen
57	30 4E	Go to return
	BNKWRT	
59	D3	Return to MAIN
5A	89 AB	Update byte pointer
5C	8A AC	Update bit pointer
5E	FB FF	Inverts D via XOR IMMEDIATE
60	EB	X=B
61	F2	Combine bit pointer & screen via AND
62	5B E2	Write blank to screen
64	30 59	Go to return
	MAIN	
66	E2 69	Turn CDP1861 on
68	3F 75	Skip clearing routine unless INPUT pressed
6A	F8 FF AD	Point RD to top of display page
6D	ED	X=D
6E	F8 00 73	Store 00 on screen & decrement pointer
71	8D	Load pointer into D
72	3A 6E	Loop again if not done
74	5D	Store 00 in last byte of display page
75	E2 6C	Input toggles
77	F6 33 89	Tests "move right" bit & branches
7A	F6 33 98	Tests "move left" bit & branches
7D	F6 33 A7	Tests "move down" bit & branches
80	F6 33 AF	Tests "move up" bit & branches
83	F6 3B B7	Tests dot/blank bit
86	7B	Turn Q on
87	30 B7	Go to EXECUTE
89	BA	Store D in RA.1
8A	8A	Fetch temporary bit pointer
8B	F6 33 92	Shift right and test for border cross

Listing 1 continued on page 224

Listing 1 continued:

```
8E   AA             Update bit pointer
8F   9A 30 7A       Put old D back in D & return to shift & test
92   19             Increment temporary byte pointer
93   76             Shift bit back into other end of bit pointer
94   AA             Update bit pointer
95   9A 30 7A       Put old D back in D & return to shift & test
98   BA             Store D in RA.1
99   8A             Fetch temporary bit pointer
9A   FE 33 A1       Shift left and test for border cross
9D   AA             Update bit pointer
9E   9A 30 7D       Put old D back in D & return to shift & test
A1   29             Decrement temporary byte pointer
A2   7E             Shift bit back into other end of bit pointer
A3   AA             Update bit pointer
A4   9A 30 7D       Put old D back in D & return to shift & test
A7   BA             Store D in RA.1
A8   89             Fetch temporary byte pointer
A9   FC 08          Add 08 to D & put sum in D
AB   A9             Update byte pointer
AC   9A 30 80       Put old D back in D & return to shift & test
AF   BA             Store D in RA.1
B0   89             Fetch temporary byte pointer
B1   FF 08          Subtract 08 from D & put difference in D
B3   A9             Update byte pointer
B4   9A 30 83       Put old D back in D & return to shift & test
                EXECUTE
B7   D5 D8 D6 D8    Generate one "wink" of cursor
BB   31 C0          Go to M(C0) if Q is on
BD   D6             Call DOTWRT & write on screen
BE   30 68          Go to test for clear
C0   D5             Call BNKWRT & write on screen
C1   7A             Turn Q off
C2   30 68          Go to test for clear
```

Text continued from page 220:

One novel effect may be produced by changing the sequence of bytes beginning at location 0046 to 01, AE, 2E, 8E. This permits the program to run at maximum speed. The cursor will streak across the screen almost too quickly for the eye to follow. As you flip the toggle switches up and down, it will paint a crazy-quilt pattern across the screen.

To clear the screen, simply hold INPUT depressed while flipping RUN up. This branches to a simple routine that writes zeroes consecutively in memory from the top of the displayed page on down.

Design Storage

Saving a design produced with the Doodler for later display involves dumping the contents of the display page of memory into some mass-storage medium. Lacking a cassette tape interface or some other storage, you will have to step through memory and write the hexadecimal contents of each byte in the page.

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Sacramento, CA 95821

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Circle 138 on inquiry card.

Book Reviews

TRS-80 Assembly Language Programming

William Barden Jr
Radio Shack, 1979
224 pages, softcover
$3.95

"The goal of this book is to take a TRS-80 user familiar with some of the concepts of programming in BASIC and introduce him to TRS-80 assembly language." With that statement in the preface, Mr Barden proceeds to do exactly that. He introduces the user of the Radio Shack TRS-80 computer to that mysterious element of programming called assembly language.

For you old-timers, *TRS-80 Assembly Language Programming* is a refreshing review of how we used to program way back in the good old days. For you novices, perhaps discouraged after trying to debug a BASIC program, this book is the change of pace you need. Throw away, or at least put aside, that BASIC user's manual, type in "SYSTEM" when the prompt character appears, and load that Editor/Assembler or TBUG tape you just bought. Now you are going to see what computer programming is all about!

Although the author states that the Radio Shack Editor/Assembler package or its equivalent is not a requirement, you will miss half the fun of reading this book if you do not have it. Also, TBUG is recommended by the author in order to fully appreciate some material.

Barden has developed a unique presentation to introduce and explain the general concepts of the TRS-80 assembly language, the mnemonic system for the Z80 microprocessor. I say a unique presentation because this is the first assembly-language book which I have enjoyed reading. Barden is not averse to injecting a little humor into his writing. After all, who says that programming books should be all bits, bytes, and syntax restrictions?

Barden begins with the architecture of the Z80, its instruction set, and its addressing modes. He then proceeds through the Editor/Assembler and the TBUG commands and formats in the first section of the book.

There is quite a bit of information packed within these first eighty-four pages, and it pays to read through Section 1 with a highlighting marker in hand. In fact, I skimmed through these pages for my first reading and then reread them more carefully the second time. This method tends to fix certain important details in your mind and will act as a referencing tool.

After you feel confident with the introductory material, move on to Sec-

tion 2. Barden not only explains the how and the why of assembly language, but does so with useful examples of assembly-language coding. When he explains how to move data, he does it by coding the instructions and discussing the pertinent background. Arithmetic and comparison operations, logical and bit operations, shifting, strings, and tables are explained and presented with appropriate coding. If you have TBUG or Editor/Assembler, you can code along with the text and actually see the operations being executed. This interactive approach works well.

In *TRS-80 Assembly Language Programming*, Barden handles the discussion of input/output (I/O) operations in an easily readable, yet informative fashion. After you complete this phase of your education, the mystery of assembly language magically evaporates, and you are ready to tackle some sophisticated assembly-language programming.

But that's not all. Barden ties together most of the loose threads by including some interesting and useful subroutines. If you want a quick routine to fill a block of memory with any given 8-bit value or move the contents of a block of memory from one area to another, you need only assemble the subroutines already coded for you and presented in the book.

Some arithmetic subroutines are also given: adding or subtracting operands containing up to 256 bytes, and multiplying or dividing 16-bit numbers. The compare subroutine is useful since it compares two 8-bit operands in true algebraic fashion. A routine for converting an 8-bit value into two American Standard Code for Information Interchange (ASCII) characters is included, as is a search subroutine. Finally, three subroutines that operate in a manner similar to the SET, RESET, and POINT statements in BASIC are given in the book.

Barden offers four complete assembly-language programs to start your program library off on the right foot. These perform the functions of writing data to the screen (good for looking at the contents of memory locations), moving patterns at high speed (great for animated graphics), a graphic bubble sort (good for demonstrations), and a program to play music via the cassette output port.

The appendices include a listing of the Z80 instruction set and a listing of the Z80 op codes. (For quick reference to Z80 mnemonics, Zilog offers the *Z80-CPU Programming Reference Card*, which I have found more convenient to use than flipping through the pages of a book.)

One further note: William Barden is also the author of *The Z80 Microcomputer Handbook* (Howard W Sams Co Inc, 1978), which takes the Z80 software a few steps deeper into the assembly-language forest.

So, what can you get for $3.95 in addition to Barden's excellent introductory text dealing with Z80 assembly-language programming? Quite possibly you will get a hard-to-shake bite from the assembly-language bug. ■

Len Gorney
Box 91 RR 5
Salisbury Rd
Clarks Summit PA 18411

Clubs and Newsletters

Newsletter for Ohio Scientific Users

The OSI Users' Independent Newsletter is edited, published, and written by Charles Curley, 6061 Lime Ave, Number 2, Long Beach CA 90805. A year's subscription is $10 for six issues. The newsletter includes articles on software, hardware, bugs and fixes, and reviews of items of interest to OSI users. Articles are welcome from enthusiastic owners and users.

Salem, Oregon Area Computer Club

Club membership is open to all those that are interested in using microcomputers for fun and business. Membership dues are $5 per year. The club meets the first Monday of each odd-numbered month at McKinley Community School, 461 McGilchrist St, Salem, Oregon. On even-numbered months, they meet at Computer Pathways Unltd Retail Store, 831 Lancaster Dr, Salem, Oregon. A monthly newsletter is published. Each meeting features a presentation by a club member or invited guest. For information, contact Salem Area Computer Club, c/o Doug Walker, 4554 Jan Ree Dr NE, Salem OR 97303.

North London Hobby Computer Club (NLHCC)

The NLHCC has scheduled their meetings for the next 3 months. The theme for the May meeting is "Computer-Aided Instruction." The meeting will be held May 7 at 7 PM in the Students Common Room in the Polytechnic of North London. On June 4, the meeting is entitled "The House Computer." July third's meeting is on "The Personal Computer and Restel/Teletext." Contact NLHCC, Holloway, London N7 8DB, ENGLAND.

TRS-80 Users Group of Sacramento

The TRS-80 users group of Sacramento meets at the Sacramento Country Branch Library, 2443 Marconi Blvd (Marconi and Fulton), Sacramento, California, from 7 to 10 PM as called. For more information, contact the TRS-80 Users Group of Sacramento, POB 255704, Sacramento CA 95825.

University of New Hampshire Computer Services Newsletter

On Line is a well-produced newsletter covering software programs, schedules of events and other activities of interest to students in the computer programs. For more information, contact Computer Services, University of New Hampshire, Kingsbury Hall, Durham NH 03824.

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787/026 Pub. Pr., $21.95 Club Pr., $16.50

MICROCOMPUTERS/MICROPROCESSORS: Hardware, Software & Applications By J. L. Hilburn & P. N. Julich
771/499 Pub. Pr., $22.50 Club Pr., $16.50

MICROPROCESSOR APPLICATIONS MANUAL By Motorola, Inc.
435/278 Pub. Pr., $38.00 Club Pr., $26.50

THE 8080A BUGBOOK: MICROCOMPUTER INTERFACING AND PROGRAMMING By P. R. Rony, D. G. Larsen & J. A. Titus
783/845 Pub. Pr., $9.95 Club Pr., $8.45

MICROCOMPUTER-BASED DESIGN By J. Peatman
491/380 Pub. Pr., $26.50 Club Pr., $18.95

DATA BASE DESIGN By G. Wiederhold
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MEMORY DESIGN: Microcomputers and Mainframes By Electronics Magazine
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783/659 Pub. Pr., $24.50 Club Pr., $19.50

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Central Oklahoma Amateur Computing Association (CENOACA)

CENOACA meets the second Saturday of each month at the OSU Technical Institute, 900 N Portland, Oklahoma City, Oklahoma, at 10 AM. Their purpose is to acquaint beginners with personal computing and increase their knowledge of special interest areas, including SwTPC and 6800 systems. Their newsletter, *CENOACA Newsbits*, is published on an irregular basis. Contact CENOACA, POB 2213, Norman OK 73070.

Another Group in Florida

The Space Coast Microcomputer Club meets on the fourth Thursday of each month at 7:30 PM in the Merritt Island Public Library Auditorium. They are affiliated with the JF Kennedy Space Center at Cape Canaveral. The group publishes *Enterprise*, a monthly newsletter. The primary interests are Z80, 8080, and S-100 systems. Dues are $5 per year, and inquiries should be sent to Ray O Lockwood, 315 Inlet Ave, Merritt Island FL 32952.

APL Newsletter

A quarterly newsletter describing tools, techniques, services, and containing general news of interest to APL users, is being published by Southwater Corp, 2348 Whitney Ave, Mt Carmel CT 06518. Subscriptions are $6 annually and requests should be sent to *APL Market Newsletter*, at the above address.

Newsletters on the UCSD Pascal System

The Institute for Information Systems is publishing newsletters describing the UCSD Pascal System developed by the University of California, San Diego. For more information, contact the Institute for Information Systems, mail code C-021, University of California, San Diego, La Jolla CA 92093.

Apple Users Group

The Goldcoast Computer Apple II Users Club desires additional members. The group publishes a monthly newsletter with programming tips, and they have a library selection of over 1000 programs. Send for details: Florida's Goldcoast Computer Apple II Users Club, 133 Brenda St, Milton FL 32570.

Feedback From Fujitsu

Feedback From Fujitsu is a newsletter from Fujitsu Limited, Japan's largest computer manufacturer. It contains items concerning discoveries and general business news of Japan's strides in the computer industry. For more information, contact *Feedback From Fujitsu*, Ruder and Finn Inc, 110 E 59th St, New York NY 10022.

Association for Computers and the Humanities

This international organization is devoted to the study of computer applications in language and literary studies, history, musicology, the visual arts, cultural anthropology, and other related social sciences. Members of the association are entitled to discount at the International Conference on Computers and the Humanities and the meetings of the Association for Literary and Linguistic Computing. The annual dues are $15, and a quarterly newsletter is available for $15 per year. For details, write Association for Computers and the Humanities, Queens College, Flushing NY 11367.

Computers and Gambling Magazine

This quarterly magazine is oriented toward computer hobbyists interested in using computers for all types of handicapping systems, card counting systems, and techniques for stock and future markets investments. Articles describe products and techniques for the computerized gambler, and advertising of products and personal computers is included. Sample issues are available for $1. Subscriptions are $5 per year and may be obtained by writing to Joe Computer, 22713 Ventura Blvd, Suite F, Woodland Hills CA 91364. ■

Observations from BYTE's Ongoing Monitor Box, The BOMB

As the card says, BYTE's BOMB is your direct line to the editor's desk. Ever since the third issue of BYTE (November 1975), BYTE's editors have used the BOMB as an important source of information on how readers react to our magazine. Therefore we thank the readers who have mailed the BOMB card to us and included their comments.

Occasionally we like to share with you some of the more interesting responses received on these cards. The most pictorial BOMB card in recent memory came from a reader in Hackensack, New Jersey, shown front and back in photos 1 and 2. It seems our friend in New Jersey was generally pleased with our January 1980 issue.

Regretfully not all of our readers have been as well pleased. On one February 1980 BYTE BOMB card most of the articles were rated as being of poor quality, and a single word appeared in the "Comments" section: "PHOOEY." Yet another BOMB card for February said: "Your best issue in my 3 years!!" Clearly, a split decision.

If you have wondered when we stop accepting BOMB cards for a given issue, we cut off tabulation during the second week of the month after the cover date of an issue.

If you have never sent in a BOMB card, but intend to do so, please observe the following points. The card should be sent to our offices in Peterborough, New Hampshire. The card is presently not postpaid, but $0.10 US postage will suffice for most readers. The card is intended to record your subjective opinion, so just write your reaction, and put any specific comments on the bottom of the card. You are free to remain anonymous, but you may put your name and address on the card if you wish. In any case, letting us know your responses to our work helps us to work better. . . .RSS

The Largest Computer Store in America?

What is the largest personal computer store in America? The answer to that question is debatable, but on the East Coast, it's probably NEECO's (New England Electronics Company Incorporated) new facility in Needham, Massachusetts. The 9000-square-foot showroom was filled with a variety of hardware and software on our recent visit. President Robert Crowell told us about their new nationwide distribution subsidiary, called Microamerica, which was announced last fall and carries most of the major computer product lines.

We have noticed a marked increase in the number of large computer stores like Bob Crowell's with diverse product lines. This supermarket-like approach can be beneficial to the industry when combined with personal service to customers—a vital ingredient to any store's success.

In the West, things are also humming in the personal computer store field. Micro-Age in Tempe, Arizona, is a good example. Run by Jeff McKeever and Alan Hald, Micro-Age has been expanding. We were favorably impressed by their facility and by their approach to the market during a recent visit. . . .CM

Texas Instruments Has an Award Winning Bubble Memory

Texas Instruments has been awarded the 1979 Information Product of the Year Award for its Model 763 Bubble-Memory Data Terminal and Model 765 Portable Bubble-Memory Data Terminal. Both terminals have a full, 128-character, alphanumeric keyboard. Up to 80,000 characters can be collected and stored in the nonvolatile bubble memory, then transmitted at rates from 110 to 9600 bits per second (bps) to a host computer system. Both units have a quiet 30-character-per-second (cps) print speed and built-in acoustic coupler modem.

A bubble memory is a small electromagnetic circuit that stores digital information by changing the magnetic polarity of a thin, crystalline film. The bubbles are cylindrical magnetic islands polarized in a direction opposite from that of the film. Bubble memory has no moving parts, and, because it works magnetically, retains information when the power is turned off. It offers higher access

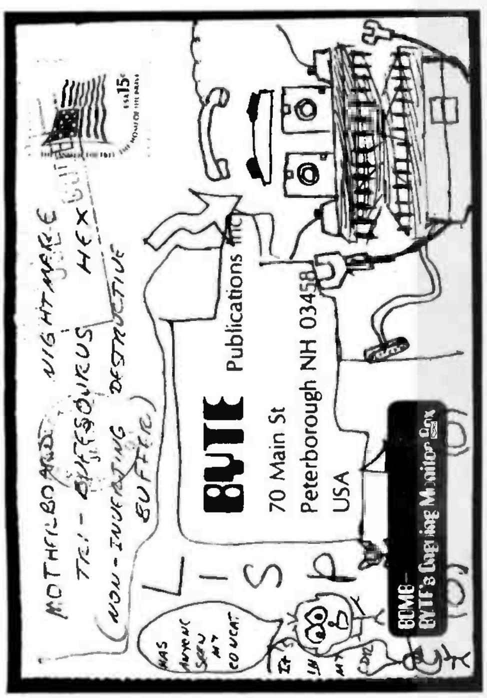

Photo 1

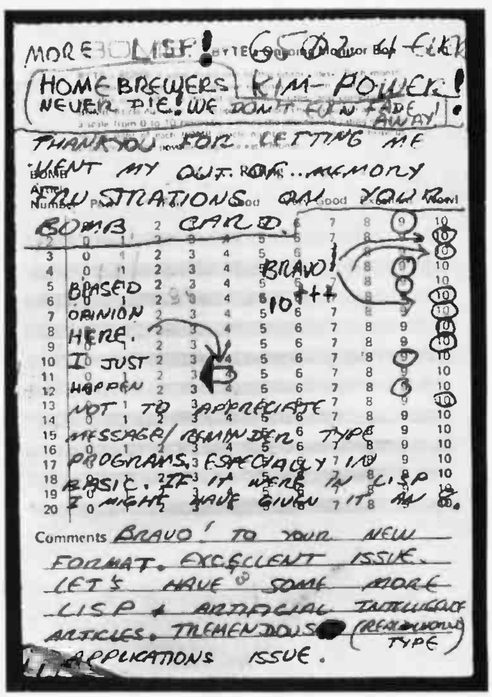

Photo 2

speeds, smaller size, and less weight and power consumption over paper-tape, cassette and floppy-disk systems. Bubble memory terminals can access any indexed record in memory in less than 15 ms (ie: 10 times faster than a floppy disk). If the data location is unknown, the character-string-search speed is 1000 cps, about 4 times the speed of a cassette search.

For more information, contact Texas Instruments, POB 1444, M/S 7784, Houston TX 77001.

The Fifth Annual California Computer Swap Meet

The Fifth Annual California Computer Swap Meet will be held on June 1, 1980, from 10 to 6 PM at the Santa Clara County Fairgrounds (344 Tully Rd, San Jose CA). Last year's event, held in September at the San Mateo County Fairgrounds, was attended by over 3000 buyers.

Personal computing hardware and software will be sold by individuals, computer manufacturers, and computer stores. New software and hardware, as well as used, will be offered by vendors and individuals who have cleaned out their back rooms and garages for the event. Admission is free to buyers. Contact the Fifth California Computer Swap Meet, POB 52, Palo Alto CA 94302, or call 415-324-2404.

Inexpensive Communications Via Meteor Trails

The hundreds of millions of meteors that enter the earth's atmosphere every day leave in their wake a very inexpensive communications medium—the meteor trail. This band of ionized particles is an effective alternative to satellites for communication. Meteor trails can be used to relay data concerning icebergs, pollution, earthquakes, and oil reserves, and can link remote villages with distant sources of supplies and emergency assistance.

Meteor burst transmission has proven reliable and cost-effective for the snow telemetry program operated by the US Department of Agriculture's Soil Conservation Service. By transmitting snowfall data from remote locations, the program has eliminated costly manual measurements.

Meteor burst transmission systems work in several stages. Remote sensors gather data while a microprocessor-controlled station emits a continuous radio signal, which bounces off a meteor trail whenever one occurs within range. When this signal reaches a transceiver at a remote site, data is transmitted via the meteor trail to the central station.

For more information, contact SRI International, 333 Ravenswood Ave, Menlo Park CA 94025.■

BYTE's Bugs

Escher's Nationality

I was interested in the February 1980 BYTE cover and in Carl Helmers' editorial concerning the Euler Problem of Königsberg. I immediately noticed when I received the issue the similarity of the cover painting to Escher's work. However, I must take argument concerning the statement that Escher was a Swiss artist.

Maurits C Escher was born on June 17, 1898 in Leeuwarden, *Netherlands*, and died March 27, 1972 in Laren, also in the Netherlands. He was in fact a *Dutchman* whose works are almost revered today in the Netherlands. I certainly commend artist Robert Tinney for combining two of Escher's more famous prints *Drawing Hands*, from January 1948, and *Reptiles*, from March 1943. However, the sequence of reptiles in Escher's original work came around and completed the cycle, by returning to the flat paper, whereas these "dragons" seem to disappear around the corner.

Naturally, the Towers of Hanoi did not go unnoticed either.

My commendation to Mr Tinney, but I think that the history of Escher, who may have been the world's greatest graphic artist, should be given correctly.

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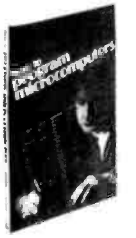

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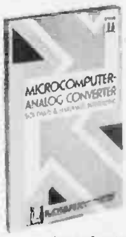

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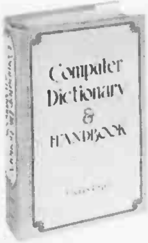

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Event Queue

MAY 1980

May and June

Microprocessor Training Courses, Cudham Hall, Cudham, Sevenoaks, Kent, ENGLAND. Microprocessor familiarization, microprocessor applications for the equipment user and for the manufacturer, and microprocessor-based equipment design and development are the courses being offered by the Sira Institute Limited. Write to Conference and Courses Unit, Sira Institute Ltd, South Hill, Chislehurst, Kent BR7 5EH ENGLAND.

May 1-2

Programming Language Technology and Ada, San Francisco CA. Conducted by Anthony Wasserman, the conference will discuss concepts of programming languages including those which support Ada language definition and development activity. The course costs $450. Registration information is available from Software Research Associates, POB 2432, San Francisco CA 94126.

May 5-7

Software Principles for Management, San Francisco CA. The course is intended for managers who need to understand what software is and how to utilize it properly. Registration is $675, and additional information is available from Technology Transfer Institute, POB 49765, Los Angeles CA 90049.

May 5-7

Data Communications, George Washington University Library, 2130 H St. NW, Washington DC. This course is intended to highlight major data communication services available, the basic choices in designing a data communications network, and essential engineering aspects of data communications. It is intended for systems analysts, engineers and managers. Contact the Director, Continuing Engineering Education, George Washington University, Washington DC 20052. The course fee is $510.

May 6-10

The Eighth Annual Canadian Association for Information Science, Toronto, CANADA. Technology, commodity, and rights are the themes of this conference. Topics will cover information in the marketplace, information transfer and policy issues, right to access, new information technologies and applications, and other subjects. For more information, contact the Program Chairman, Eighth Annual CAIS Conference, Technical Information Centre, Bell Northern Software Research, 12th Floor, 522 University Ave, Toronto, Ontario M5G 1W7 CANADA.

In order to gain optimal coverage of your organization's computer conferences, seminars, workshops, courses, etc, notice should reach our office at least three months in advance of the date of the event. Entries should be sent to: Event Queue, BYTE Publications, 70 Main St, Peterborough NH 03458. Each month we publish the current contents of the queue for the month of the cover date and the two following calendar months. Thus a given event may appear as many as three times in this section if it is sent to us far enough in advance.

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May 12-13
Data Communications, Worcester Polytechnic Institute, Worcester MA. This seminar is designed to help professionals develop an effective data communications system. Network design, requirements, software, diagnostics, and controls are some of the issues to be covered. The fee is $375 which covers everything except hotels. For information, contact Office of Continuing Education, Worcester Polytechnic Institute, Worcester MA 01609.

May 13-15
Microprocessors: New Directions for Mankind, Albuquerque NM. This symposium will deal with a variety of microprocessor applications. It is part of the Ideas in Science and Electronics Show. Contact J Arlin Cooper, Div 2331, Sandia Laboratories, Albuquerque NM 87185.

May 13-15
Electro/80 Show and Convention, Hynes Auditorium and Boston Sheraton, Boston MA. This show consists of presentations and exhibitions by computer industry manufacturers. Contact Electronic Conventions Inc, 99 N Sepulveda Blvd, El Segundo CA 90245.

May 13-16
The Ninth Annual Conference of MUMPS Users Group, Islandia Hyatt House, San Diego CA. This meeting will bring together scientific, medical, and business professionals to discuss current research and application development. Areas of participation are paper presentations, workshops and tutorials, and vendor exhibits. Contact Dr Jack Bowie, MUG 80 Program Chairman, The Mitre Corp, Mail Stop 641, 1820 Dolley Madison Blvd, McLean VA 22102.

May 21-22
The Second Clemson Small Computer Conference, Clemson University, Clemson SC. This program will consist of presentations, discussions and an exhibition. Emphasis will be placed on business, industry, engineering, science, and education. For registration information, contact J K Johnson, Continuing Engineering Education, Clemson University, Clemson SC 29631. For general information, contact W J Barnett, Electrical and Computer Engineering Dept, Clemson University, Clemson SC 29631.

May 21-23
Business and Personal Computer Sales-Expo 80, Philadelphia Civic Center, Philadelphia PA. This show is aimed at a wide range of interests in business and any other area that has a need for computers and computer-related products. Exhibitors will be giving demonstrations of equipment. Contact Produx 2000 Inc, Roosevelt Blvd and Mascher St, Philadelphia PA 19120.

May 23
The Digital Computer Association, Annual Meeting, Pacifica Hotel, 6161 Centinela Blvd, Culver City CA. A slide show, followed by dinner and an evening program, are the main events of the meeting. The price is $15 prepaid. Send reservations to Mary Rich, 731 Bayonne St, El Segundo CA 90245.

May 24-25
Amateur Radio and Computer Hobbyists Second Annual Convention, Cervantes Convention Center, St Louis MO. Speakers, presentations, equipment displays, and a flea market will be featured. For more information, contact the Gateway Amateur Radio Assocation Inc, POB 68, Marissa IL 62257.

May 31

Amateur Radio Fair, Minnesota State Fairgrounds, St Paul MN. The North Area Repeater Association is sponsoring this swapfest and exposition for personal computer enthusiasts and radio amateurs. There will be free overnight parking for self-contained campers on May 30. The admission is $3. For information, write Amateur Fair, POB 30054, St Paul MN 55175.

May 31-June 1

Microcomputers and the Physician's Office, Hyatt Regency Hotel, San Francisco CA. This seminar will provide a realistic look at microcomputer applications in the private practice. Contact Medical Data Systems, POB 193, Ojai CA 93023.

JUNE 1980

June 2-4

Improving Productivity and Distributed Data Entry, Sheraton Center, New York NY. The conference and seminar schedule includes discussions on word processing, data processing, future directions of data entry, improving data entry productivity, automated offices, installing a data-entry incentive system, and more. Contact Data Entry Management Association, POB 3231, Stamford CT 06905.

June 4-5

Microprocessors: Hardware, Software, and Application, Holiday Inn, Boston MA. This course is recommended for technical professionals who need an understanding of microprocessors in relation to their corporate and business careers. Contact Office of Continuing Education, Worcester Polytechnic Institute, Worcester MA 01609.

June 4-6

Salon de l'Ordinateur Computer Show, Place Bonaventure, Montreal, CANADA. This exhibition will feature over eighty manufacturers' hardware and software.

For more information, contact Industrial Trade Shows of Canada, 36 Butterick St, Toronto, Ontario M8W 3Z8 CANADA.

June 9-13

Microcomputer Workshop, Carnegie-Mellon University, Pittsburgh PA. Engineers, research scientists, educators, and managers will benefit from this course. It covers all aspects of microcomputers and software. Hands-on-training will be provided. The tuition is $585 and housing can be arranged. Contact the Post College Professional Education, Carnegie-Mellon University, Pittsburgh PA 15213.

June 14

Microcomputers in Business and The Professions: Systems Selection, Butler University, 4600 N Sunset Ave, Indianapolis IN. This seminar will cover various types of hardware and software, how to evaluate the kinds and performances of computers, and their applications in business and home use. The registration fee is $75. For information, contact College of Business Administration, Butler University, 4600 N Sunset Ave, Indianapolis IN 46208.

June 15-18

International Summer Consumer Electronics Show, McCormick Place, McCormick Inn, Pick-Congress Hotel, Chicago IL. The Consumer Electronics Show (CES) will feature exhibits from many companies; seminars and discussions; and items ranging from televisions, tape recorders, telephones, and translators, to computers, component systems, auto sound systems, and electronic games will be displayed. Attendance is limited to dealers and the press. Contact Consumer Electronics Shows, Two Illinois Center, Suite 1607, 233 N Michigan Ave, Chicago Il 60601.

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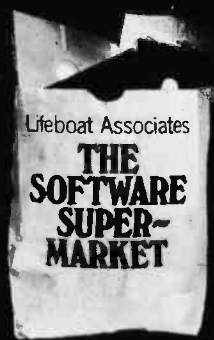

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June 16-20
Data Flow Concepts in Computer Language and Architecture, Massachusetts Institute of Technology (MIT), Cambridge MA. MIT's program will cover principles of data flow computer organization and programming language design and applications. Certain architectures will be covered and techniques will be discussed. Familiarity with languages and architecture is a prerequisite. The tuition is $750. Living arrangements can be made through the school. Contact the Office of the Summer Session, Room E19-356, MIT, Cambridge MA 02139.

June 17-19
Data Comm, Palais des Expositions, Geneva, SWITZERLAND. Data communications and distributed-data processing are the main themes of this conference and exhibition. Software development and tools, computer languages, managing data-communications systems, and definitions, concepts, and applications of data communications and distributed-data processing are some of the topics that will be covered in the conference.

For more information, contact Industrial and Scientific Conference Management Inc, 222 W Adams St, Suite 999, Chicago IL 60606.

June 18-21
Association for Computational Linguistics, University of Pennsylvania, Philadelphia PA. The meeting will cover theoretical and methodological problems of computational linguistics, speech acts, analysis of multisentence texts, dialogue, machine translation, and computational semantics. For further information contact Don Walker, Artificial Intelligence Center, SRI International, 333 Ravenswood Ave, Menlo Park CA 94025.

June 20-22
The Fifth Annual Computerfest, Franklin University, Columbus OH. Sponsored by the Midwest Affiliation of Computer Clubs, this is a gathering of interested hobbyists, professionals, and business-oriented computer users. Workshops and discussions are the main features of the conference. Contact James Crowley, 4008 Rickenbacker Ave, Columbus OH 43213.

JULY 1980

July 7-11
Computers and Related Products, Hyatt Regency Hotel, Seoul, KOREA. This show is limited to approximately forty firms for exhibition. For details, contact Robert Wallace, Rm 6015A, US Dept of Commerce, Industry and Trade Commission, Washington DC 20230.

July 14-16
Diagnostic Software: Planning and Design, Sheraton-Lexington Motor Inn, Lexington MA. The seminar is for design, test, and diagnostic engineers. Design examples, lectures, informal sessions, and programming are part of the course. The fee is $450. Contact Professor Donald French, Institute for Advanced Professional Studies, One Gateway Center, Newton MA 02158.

July 14-18
SIGGRAPH '80, Seattle Center, Seattle WA. Panel discussions and readings will be included in this conference. The topics will include graphic displays, animation/dynamics, cartography, input techniques, video and color hardware, and more. For general information, write to SIGGRAPH '80, POB 88203, Seattle WA 98188.

July 22-24
Microcomputer Show, Wembley Center, London, ENGLAND. New products will be exhibited, along with presentations of papers. For information contact TMAC, 680 Beach St, Suite 428, San Francisco CA 94109. ■

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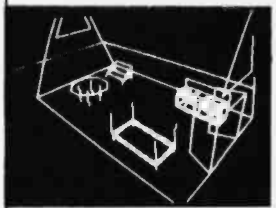

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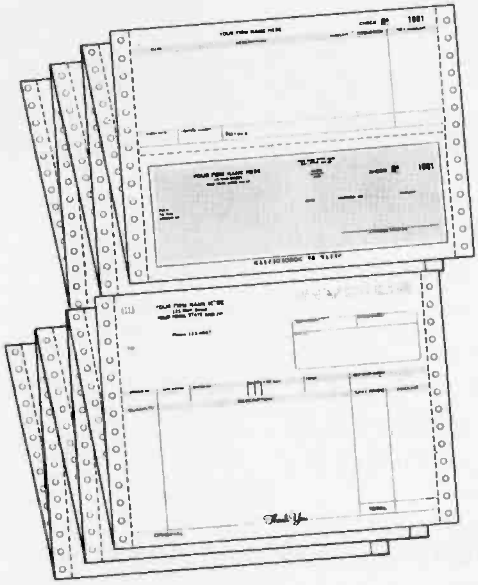

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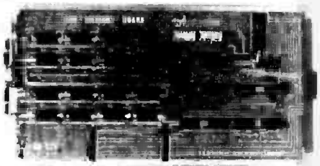

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Figure 1 shows the connection of the active error-checking and correcting apparatus between the computer and the peripheral data-storage device.

The theoretical development of error-trapping and correcting codes is largely due to the efforts of Richard W Hamming, a mathematician who first published on the subject in the *Bell System Technical Journal* early in 1950. (See reference 1.) Now, thirty years later, *Hamming codes* still represent one of the more practical approaches to the error-correcting problem.

A particularly important aspect of Hamming's work focused on his formulation of the concept of *code distance* (indicated by the letter D). This relates the uniqueness of (or "distance between") meaningful codes to the number of *simultaneous* errors (indicated by the Greek theta, θ) that can be detected and corrected.

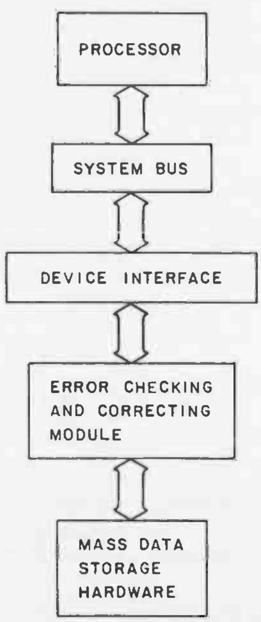

Figure 1: *Block diagram showing interconnection of error-checking and correcting system with the computer.*

Definition of Hamming Distance

The Hamming distance between any two words is defined as the number of bit positions in which they differ. In terms of logical processes this is merely the total number of bits set to logic 1 following an exclusive-OR operation between the two words, as shown in figure 2. Simple binary coding has a Hamming distance of 1. This unitary distance is precisely the source of the problem, because any given code value appears to be as valid as any other.

Normally, as a processor receives binary data from a peripheral device, no mechanism is present which can correct a bit inversion. If a bit is read erroneously, it will either invalidate the check sum and cause an error trap, or it will be loaded into main memory without detection, thus propagating the error. It may or may not be a critical fault.

Consider the following 4-bit code:

Symbol	Encoded Form bit 3210
0	0001
1	0010
2	0100
3	1000

This limited shifting pattern generates a code format with a Ham-

01001111 11101001	}	10100110
00000000 00000001	}	00000001
00000000 11111110	}	11111110
01010101 10101010	}	11111111

Figure 2: *The logical exclusive-OR function produces the output bytes shown in the right column from the input bytes shown in the left column. For each bit, the output bit is a 1 if and only if one of the input bits is a 1.*

Hamming Distance (Minimum)	
1	code uniqueness
2	single-error detection
3	single-error correction
4	single-error correction/double-error detection
5	double-error correction

Table 1: *Minimum Hamming code distances necessary to obtain the listed properties in a particular coding scheme. Capabilities increase directly as Hamming distance increases (for small distances). Correction of an arbitrary number of errors requires a Hamming distance of at least twice the number of errors plus 1.*

ming distance of 2. It is impossible to invert a single bit position and create any one of the other three valid words.

Symbol	Encoded Form
3	1000
	↓
INVALID	1100

However, if a dual error occurred, the code's error-detection capability would fail:

Symbol	Encoded Form
3	1000
	⇊
2	0100

As indicated above, when the Hamming distance increases, the allowable number of simultaneous errors, θ, also rises. Errors can be trapped effectively as long as θ does not equal or exceed the Hamming distance minus 1 $(D - 1)$. This should be clear, any sequence of $(D - 1)$ errors will result in the generation of a meaningless code word if the distance between code words is given by D. No series of $(D - 1)$ errors will produce a meaningful code.

Correcting Errors

Error-*correction* capability necessitates a larger Hamming distance, as shown in table 1. Any pattern of θ errors can be corrected if, and only if the Hamming distance D is greater than or equal to $(2\theta + 1)$. In this case, any received data word with θ errors differs from the transmitted, correct word in θ positions, but it also differs from all *other* meaningful words in at least $(2\theta + 1 - \theta)$, that is, $(\theta + 1)$ positions.

The erroneously received word therefore lies closer to the correct transmitted word than to any other possible word. Thus, it is possible to reconstruct the proper coding and recover the correct data word. To illustrate this point, the 4-bit code from the previous example does not meet the criterion of D greater than or equal to $(2\theta + 1)$, and is therefore uncorrectable. A single bit error in either of the two positions can lead to the same erroneous code:

Symbol	Encoded Form
3	1000
	↓
INVALID	1010
	↑
1	0010

Examination of the invalid code (1010) yields no information concerning what the correct pattern was initially. This meaningless value (1010)

could have been generated from an originally encoded 3 (pattern 1000), with an error in bit 1, or from an encoded 1 (pattern 0010) with an error in bit 3. Without any additional information, it is impossible to distinguish between these cases. Once an error occurs, although it can be trapped by searching for invalid codes, it cannot be corrected.

Now consider the correctable code:

Symbol	Encoded Form
0	00000
1	11101
2	11010
3	00111

Examination of this new code reveals a minimum Hamming distance (D) of 3 between the various states, permitting single error correction. (See table 1.) The inefficiency of this code is obvious; however it should be clear that any single error can be detected and *located* using this scheme.

Symbol	Encoded Form
0	00000
	↓
INVALID	00001

The erroneous pattern could only be the result of encoding a 0 with an inversion in the least significant bit. Given the word 00001, the original, correct coding could be restored. This can be attributed to the fact that even the invalid, meaningless patterns display a limited uniqueness, and are directly traceable to specific *valid* codes subject to a small number of errors.

Symbol	Binary Form	7-bit Encoded Form
00	0000	1110000
01	0001	1000001
02	0010	0100010
03	0011	0010011
04	0100	0000100
05	0101	0110101
06	0110	1010110
07	0111	1100111
08	1000	0011000
09	1001	0101001
10	1010	1001010
11	1011	1111011
12	1100	1101100
13	1101	1011101
14	1110	0111110
15	1111	0001111

Table 2: *Sixteen different logical entities or symbols can normally be represented by a 4-bit code. Use of a unique 7-bit encoding increases the Hamming distance to 3 and allows a single-bit error correction.*

Uses of Parity

Clearly, coding efficiency is hampered as the Hamming distance is increased and as the requirements for trapping and correcting power are made more stringent. It becomes a matter of systematically generating a code that displays enough "correcting power" to handle data words of a useful length, without creating an excessive code-redundancy overhead. Here, the concept of *parity* plays an important role. Parity is established in a data word through the setting of an *additional* bit, such that the total number of bits set to logic 1 is either always odd or always even.

The operation of simple parity encoding and decoding is easy to understand. Assume, for example, that a data word 4 bits wide undergoes an odd-parity test across the entire word:

```
┌ 1010
↓
1 1010
```

During encoding in this example, the fifth bit (the parity bit) is set to establish *odd* parity. Upon decoding, if the parity bit is included in an identical parity check, namely odd parity across the entire word (now 5 bits wide), the output of the parity test will be a logic 0.

If at some point between encoding and decoding, an error forces an inversion in a single bit (eg: with an error in bit 3, input to the decoder will be 10010), the odd-parity test will

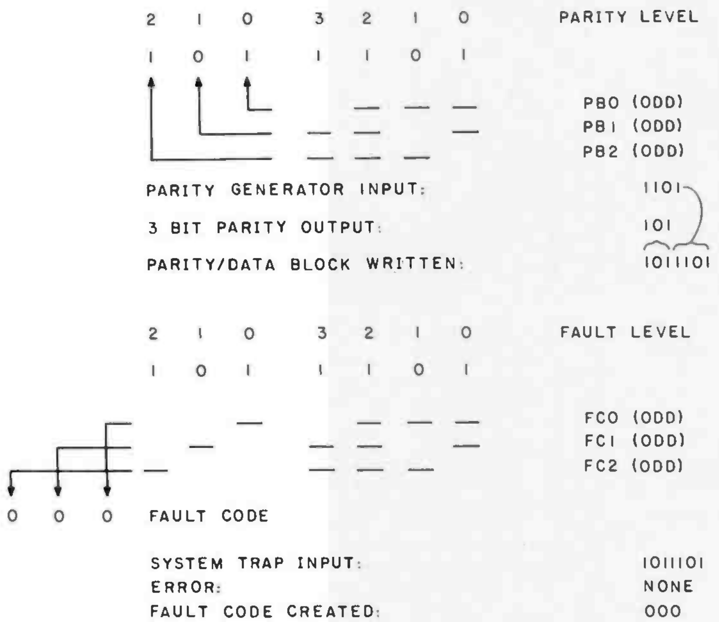

Figure 3: *Sixteen different logical states may be represented in a 7-bit code with a Hamming distance of 3. Single-bit errors may be detected and corrected. Encoding in 7 bits is accomplished by performing three distinct parity checks on 4 data bits. Table 4 shows the possible fault codes. The fault code of 000 indicates that no error was detected in decoding.*

fail and produce a logic 1 signifying an error.

Operation of Hamming Codes

Certainly this mechanism can be fooled by multiple errors, but it is possible to construct *multiple-level* parity checks which will trap a surprising number of errors. This is precisely how the Hamming codes operate. Fundamentally, Hamming's algorithm performs multiple-level parity generation on a data word at the data source. This parity code is then transmitted along with the data, and the entire code block (data plus parity code) is subsequently decoded under an analogous process. Any bit errors occurring during transmission will be detected.

Clearly, the efficiency of this error trap will approach 100% only in very simple cases. Several parameters have direct bearing on the trapping success: total word length N, number of data bits K, number of parity bits M ($M = N - K$). The ultimate goal, of course, is to realize the ideal where the quantity N/K approaches 1, and M is minimized without sacrificing trapping and correcting capability.

A 4-bit binary code is normally capable of representing sixteen different states with a Hamming distance equal to 1. Momentarily setting aside questions of efficiency, the same sixteen states can also be represented in a 7-bit code at triple the Hamming distance, as shown in table 2. Again, referring to table 1, a Hamming distance of 3 facilitates single-error correction. Encoding in 7 bits is accomplished by performing three distinct parity checks on the 4 data bits. Details of the three parity checks are summarized in table 3 and diagrammed in figure 3.

It should be understood that the actual encoded form of each symbol is irrelevant and need not be known. When no error is present, decoding of the 7-bit word will reset all three parity checks to logic 0, and will restore the data to its original form. The error-handling process is demonstrated in figure 4. With an error in the third data bit, the parity-decoding procedure flags a fault code of 110, which in table 4 is seen to correspond uniquely to an error in data position 3.

Admittedly, this does not constitute a true Hamming code, in the sense that the fault code does not display the binary form of the error-bit position within the word. This feature is convenient to implement for the shorter codes, but need not be attempted in the more comprehensive correction schemes where fault-code interpretation can be readily handled in a read-only memory.

Practicality of Use

An overhead of three parity flags for every 4 data bits is undesirable. These techniques become useful only for larger word lengths. Initially, performance increases as the data word length becomes longer, up to N = 31. It is possible to correct single-bit errors in words with 8 data bits and four additional parity flags, an overhead of 50%. Single-error correction of 16 bits requires five flags, an overhead of 32%.

In the case of an 8-bit system, an overhead of 50% may seem exorbitant, but it can pay off rapidly. Assuming that with correcting logic in operation, single errors are virtually nonexistent, it may well be possible to realize a decrease in loading time by a factor of 2, 5 or even 10. It is true that 1.5 times as many bits are being moved into and out of the storage medium, but if the data rate merely doubles, loading times will fall to

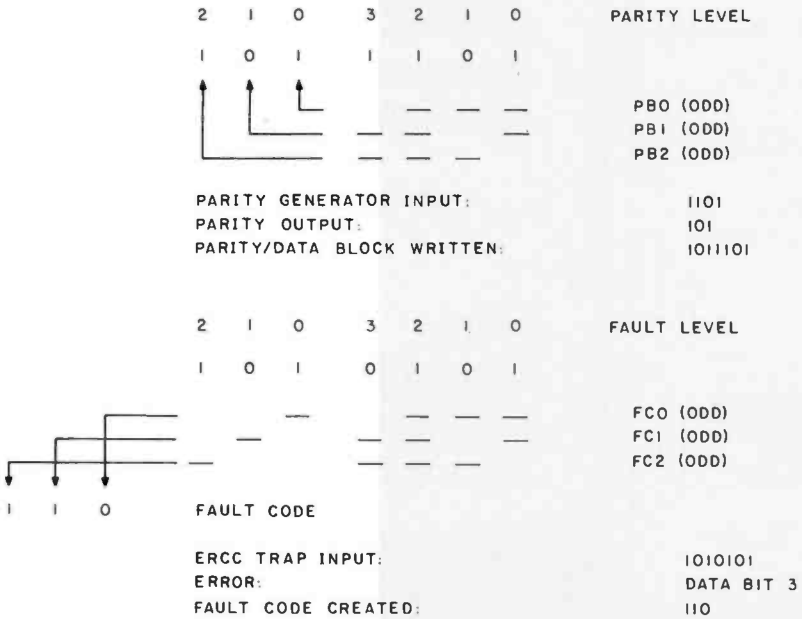

Figure 4: *Another example of encoding and decoding data composed of 4 bits in a 7-bit word. In this case an error has been detected; the fault code of 110 indicates an error in data bit 3.*

Check Bit	Data Positions	
0	0,1,2	(odd)
1	0,2,3	(odd)
2	1,2,3	(odd)

Table 3: *Encoding 4-bit data into 7 bits is done by performing 3 distinct parity checks on the 4 data bits. Each of the 3 check bits corresponds to the parity value of the data positions shown here.*

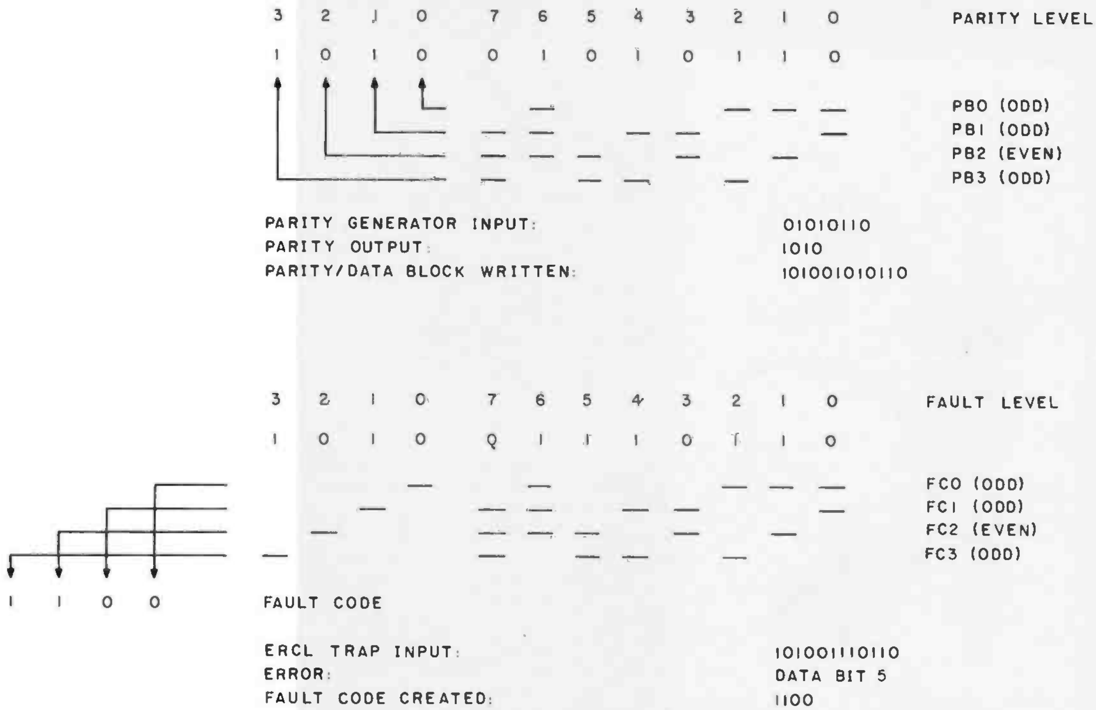

Figure 5: *Encoding and decoding for data consisting of an 8-bit byte. Four bits are used for error checking; the possible fault codes are given in table 6.*

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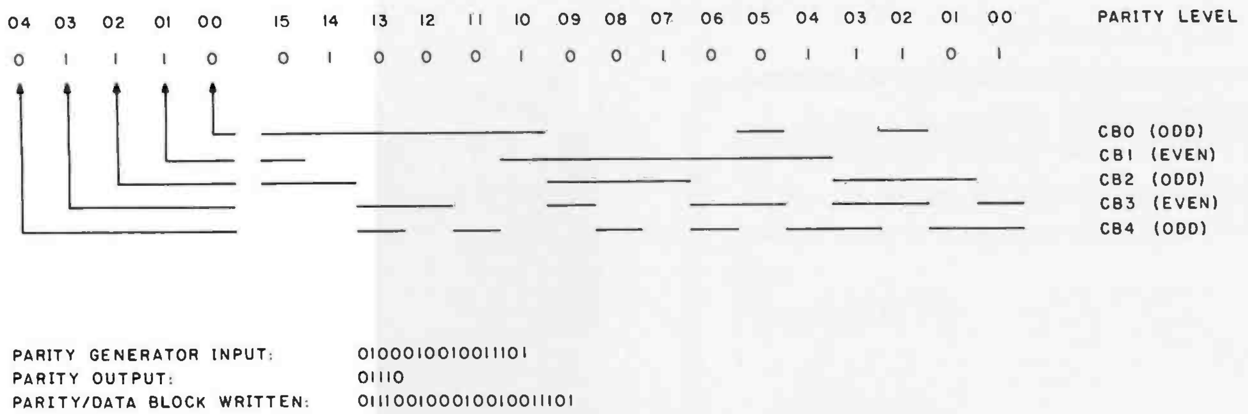

Figure 6a: *Encoding of 16-bit data using five bits for error checking; this results in a 21-bit data word being written to the peripheral device. Check bits based on even parity are set to 1 if there are an even number of 1s in the corresponding data-bit group; an odd-parity check bit is set to 1 if the number of 1s in its data-bit group is odd. This figure, figure 6b, and table 8 originally appeared in slightly different form in* Electronics *magazine, November 13, 1975, page 135. Copyright © McGraw-Hill Inc, 1975.*

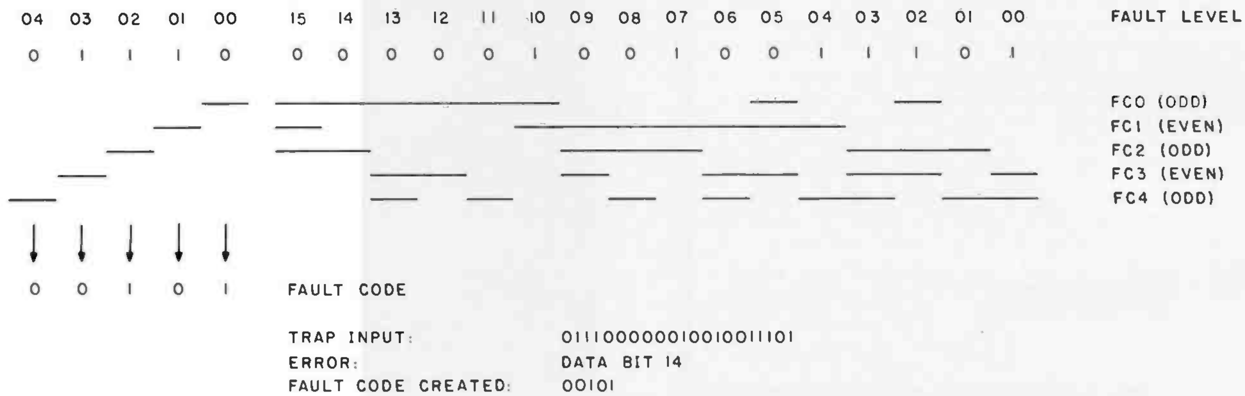

Figure 6b: *Decoding and checking the 16-bit data, 5-bit parity-check word from figure 6a. Bit 14 has been transmitted erroneously; therefore a fault code of 00101 (reading from check bit 04 to bit 00) is generated. A complete list of possible fault codes is given in table 8 (in reverse order, reading from check bit 00 to bit 04).*

Fault Code	Error
000	no error detected
001	check bit 0
010	check bit 1
011	data bit 0
100	check bit 2
101	data bit 1
110	data bit 3
111	data bit 2

Table 4: *Look-up table of fault codes used by the 4-bit into 7-bit encoding scheme. The fault code tells the error-correcting logic where the error has occurred.*

Encoding for 8 and 16 bits is shown in figures 5 and 6. The detailed parity tests for these appear in tables 5 and 7 respectively. The fault-code look-up tables are shown as tables 6 and 8. This 16-bit system was developed by the Data General Corporation. It will correct single-bit errors throughout the entire word, and will reportedly trap an average of 97% of the multiple faults that occur. Eight-bit coding logic has been verified in macroassembler routines on a DECsystem 10 by my associate Stephen J Gross, who is now at Stanford University.

Check Bit	Data Positions	
0	0,1,2,6	(odd)
1	0,3,4,6,7	(odd)
2	1,3,5,6,7	(even)
3	2,4,5,7	(odd)

Table 5: *Encoding of 8-bit data requires the use of four parity bits to allow single-bit error correction. The correspondence of each check bit to specific bits within the 8-bit data byte is shown here.*

75% of the initial value. A ten-fold increase in data rate decreases loading time by 85%. Sixteen-bit systems are even better suited to the use of error checking and correcting systems (ERCC), though the majority of microprocessors in use today operate with an 8-bit data word.

Error-Reducing Hardware

Hardware implementation utilizes standard 7400 series transistor-transistor logic (TTL). Schematic diagrams are shown in figures 7 and 8. Parity encoding and decoding is accomplished with 9-bit parity trees (using a 74180 parity generator/tester). Worst-case data path for both 8-bit and 16-bit error checking and correcting amounts to about 120 ns delay. Certainly, this interval is short enough to prevent it from imposing any constraint at even unusually high data-transfer rates. It should be clear that when handling errors, operation

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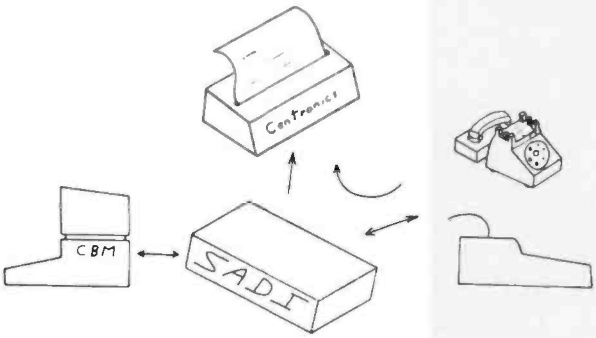

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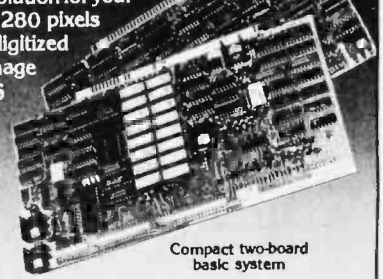

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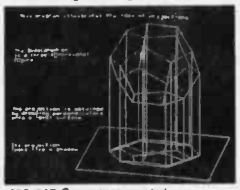

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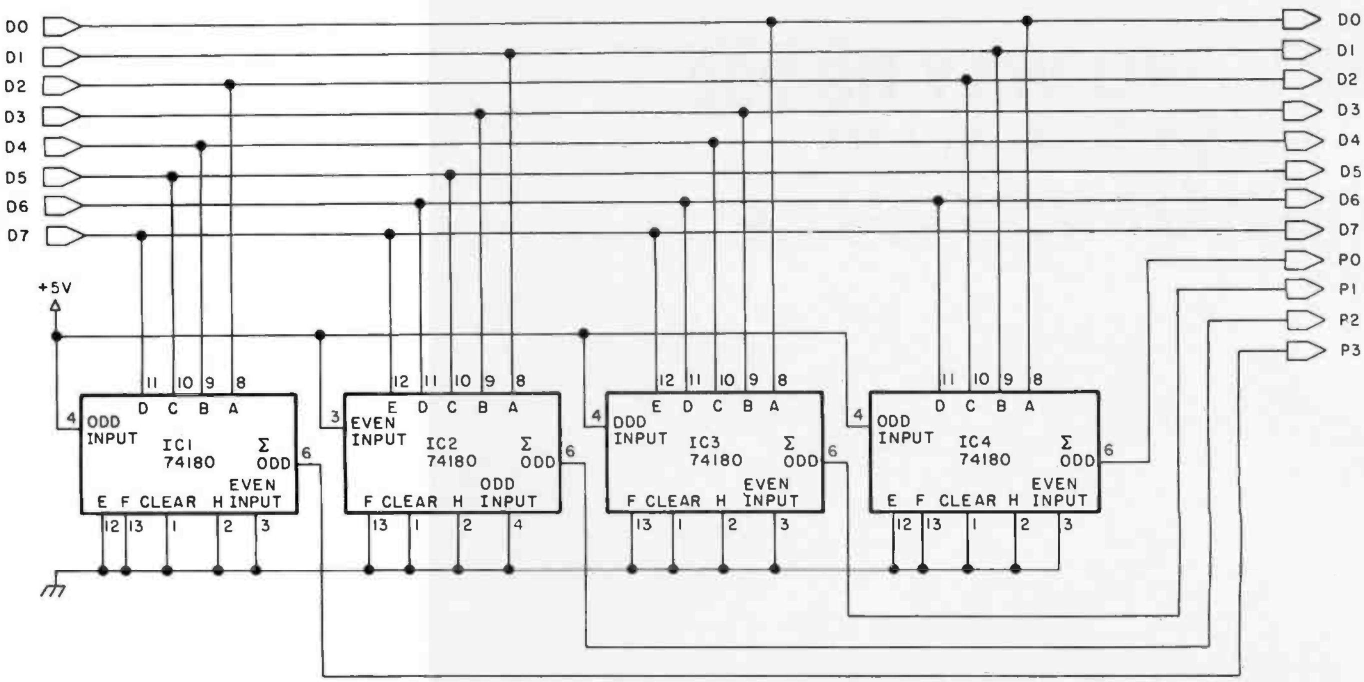

Figure 7a: *Schematic diagram of electronic logic that encodes 8-bit data. Unused input pins on the 74180 parity-generator and tester devices are connected to ground.*

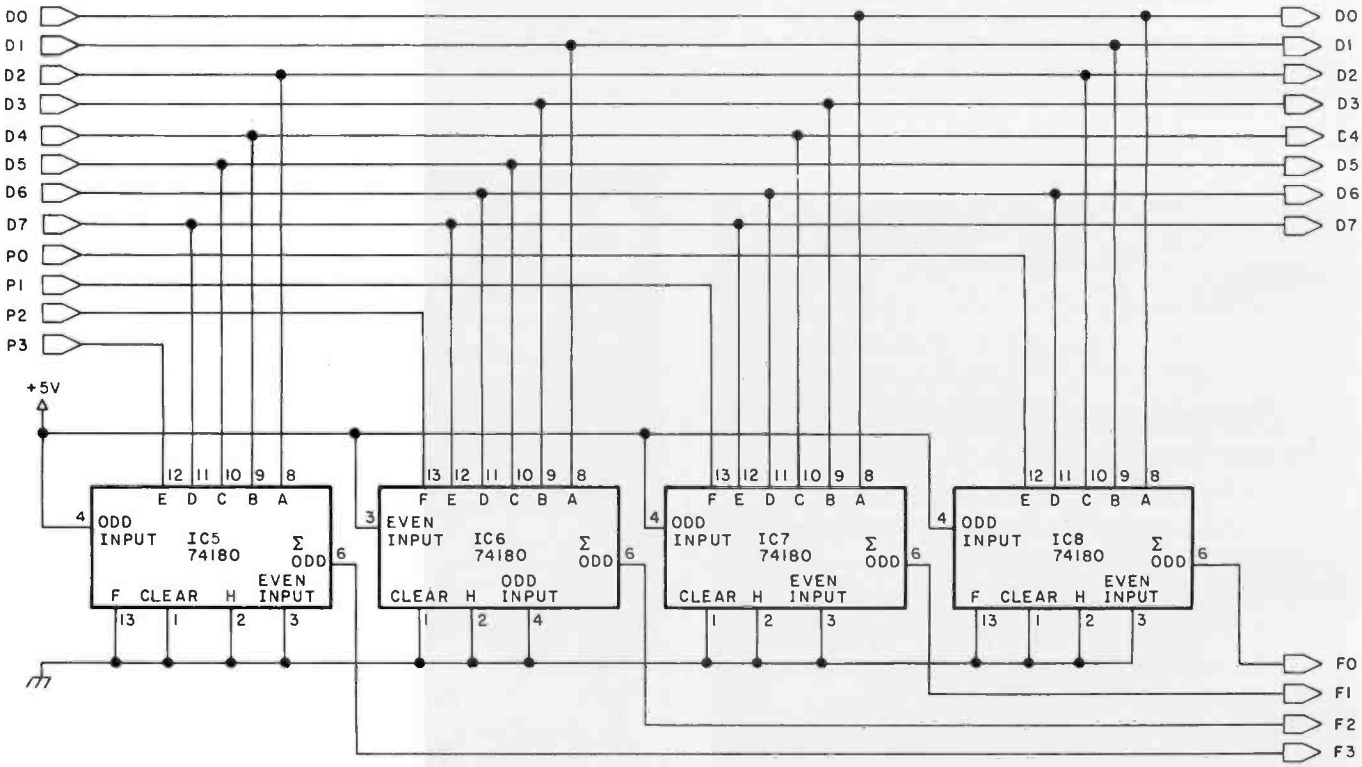

Figure 7b: *Schematic diagram of circuit for trapping errors in the 8-bit data encoded by the circuit in figure 7a. The 12-bit word received from the peripheral device is separated into 8 bits of meaningful data and 4 bits of parity-checking data. Unused inputs on the 74180s are grounded.*

of the error checking and correcting apparatus is rapid enough to make it entirely transparent to the processor and the system bus.

Though the underlying theory requires the writing of additional parity bits, the generation and interpretation of these flags are contained entirely within the error-processing system. (See figure 9.) The parity bits do not appear on the bus and are not seen by the processor; therefore no interface modification is necessary. Additional data-transfer logic is required to deal with the parity bits. The circuits in figures 7 and 8 create parallel data which must undergo a

Text continued on page 274

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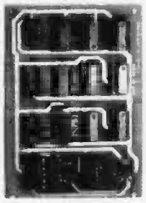

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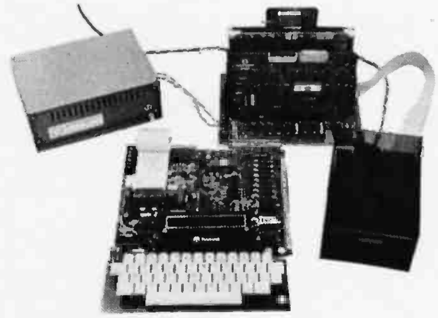

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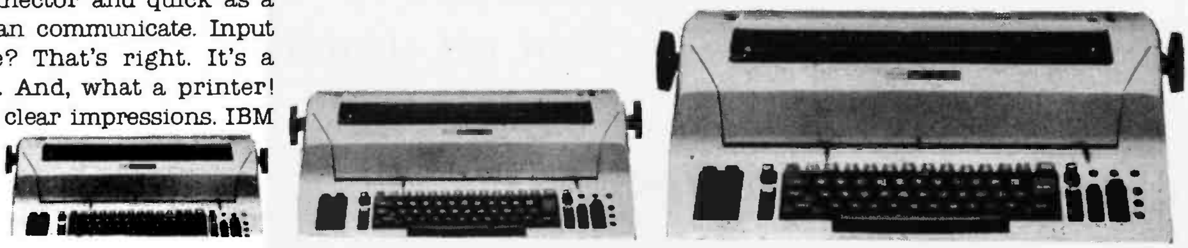

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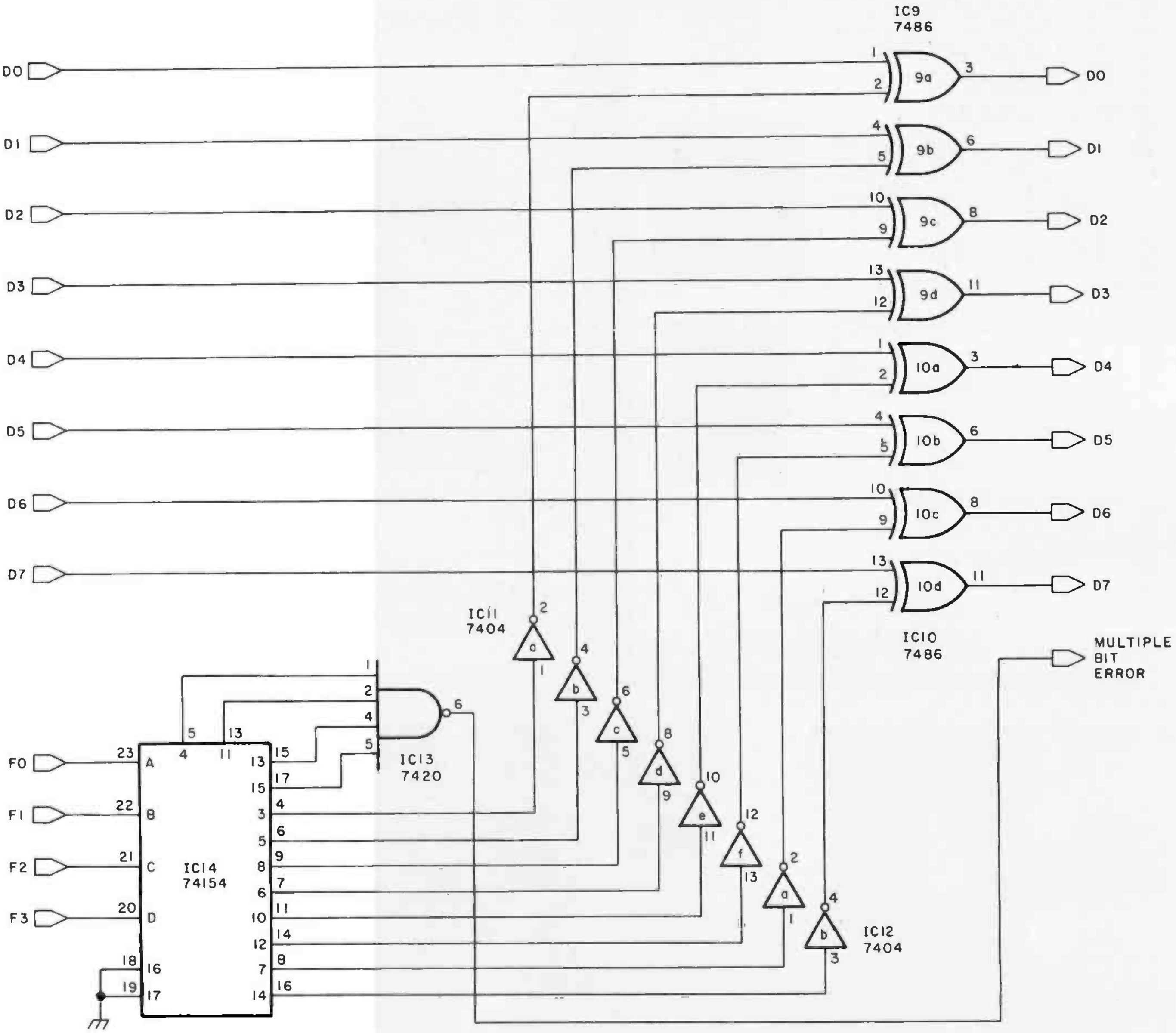

Figure 7c: *Schematic diagram of the circuit which corrects single-bit errors trapped by the circuit of figure 7b. Multiple-bit errors are made known to the processor, but cannot be corrected using this scheme.*

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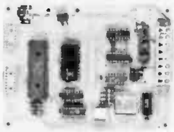

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0001	check bit 0
0010	check bit 1
0011	data bit 0
0100	check bit 2 *
0101	data bit 1
0110	data bit 3
0111	data bit 6
1000	check bit 3
1001	data bit 2
1010	data bit 4
1011	all data and parity set to logic 0
1100	data bit 5
1101	multi bit error
1110	data bit 7
1111	multi bit error

Table 6: *Look-up table of fault codes used by the 8-bit to 12-bit encoding scheme. Setting of the check-bit-2 fault code (indicated by an asterisk) shows that all data and parity bits are set to logic 1.*

Check Bit	Data Positions	
0	2,5,10,11,12,13,14,15	(odd)
1	4,5,6,7,8,9,10,15	(even)
2	1,2,3,7,8,9,14,15	(odd)
3	0,2,3,5,6,9,12,13	(even)
4	0,1,3,4,6,8,11,13	(odd)

Table 7: *The 16-bit encoding scheme uses 5 parity bits that enable single-bit error correction. Each parity-check bit performs its check operation upon the data-bit positions shown here.*

Fault Code	Error
00000	no error detected
00001	error in check bit 4
00010	error in check bit 3
00011	error in data bit 0
00100	error in check bit 2
00101	error in data bit 1
00110	multiple-bit error
00111	error in data bit 3
01000	error in check bit 1
01001	error in data bit 4
01010	all data and parity set to logic 1
01011	error in data bit 6
01100	error in data bit 7
01101	error in data bit 8
01110	error in data bit 9
01111	multiple-bit error
10000	error in check bit 0
10001	error in data bit 11
10010	error in data bit 12
10011	error in data bit 13
10100	error in data bit 14
10101	all data and parity set to logic 0
10110	error in data bit 2
10111	multiple-bit error
11000	error in data bit 10
11001	multiple-bit error
11010	error in data bit 5
11011	multiple-bit error
11100	error in data bit 15
11101	multiple-bit error
11110	multiple-bit error
11111	multiple-bit error

Table 8: *Look-up table of fault codes used by the 16-bit to 21-bit encoding scheme. The codes are shown here in order from check bit 00 to bit 04, reversed from the representation in figure 6.*

Address Input	Data Output							
	7	6	5	4	3	2	1	0
00000	0	0	0	1	0	0	0	0
00001	0	1	0	1	0	0	0	0
00010	0	1	0	1	0	0	0	0
00011	0	0	0	0	0	0	0	0
00100	0	1	0	1	0	0	0	0
00101	0	0	0	0	0	0	0	1
00110	0	0	1	1	0	0	0	0
00111	0	0	0	0	0	0	1	1
01000	0	1	0	1	0	0	0	0
01001	0	0	0	0	0	1	0	0
01010	1	1	0	1	0	0	0	0
01011	0	0	0	0	0	1	1	0
01100	0	0	0	0	0	1	1	1
01101	0	0	0	0	1	0	0	0
01110	0	0	0	0	1	0	0	1
01111	0	0	1	1	0	0	0	0
10000	0	1	0	1	0	0	0	0
10001	0	0	0	0	1	0	1	1
10010	0	0	0	0	1	1	0	0
10011	0	0	0	0	1	1	0	1
10100	0	0	0	0	1	1	1	0
10101	1	0	1	1	0	0	0	0
10110	0	0	0	0	0	0	1	0
10111	0	0	1	1	0	0	0	0
11000	0	0	0	0	1	0	1	0
11001	0	0	1	1	0	0	0	0
11010	0	0	0	0	0	1	0	1
11011	0	0	1	1	0	0	0	0
11100	0	0	0	0	1	1	1	1
11101	0	0	1	1	0	0	0	0
11110	0	0	1	1	0	0	0	0
11111	0	0	1	1	0	0	0	0

Table 9: *Truth table which is programmed into a programmable read-only memory for use in the electronic circuit of the 16-bit error-checking and correcting system.*

Number	Type	+5 V	GND
IC1	74180	14	7
IC2	74180	14	7
IC3	74180	14	7
IC4	74180	14	7
IC5	74180	14	7
IC6	74180	14	7
IC7	74180	14	7
IC8	74180	14	7
IC9	7486	14	7
IC10	7486	14	7
IC11	7404	14	7
IC12	7404	14	7
IC13	7420	14	7
IC14	74154	24	12
IC15	74180	14	7
IC16	74180	14	7
IC17	74180	14	7
IC18	74180	14	7
IC19	74180	14	7
IC20	7404	14	7
IC21	74180	14	7
IC22	74180	14	7
IC23	74180	14	7
IC24	74180	14	7
IC25	74180	14	7
IC26	7488	16	8
IC27	74154	24	12
IC28	7404	14	7
IC29	7404	14	7
IC30	7404	14	7
IC31	7486	14	7
IC32	7486	14	7
IC33	7486	14	7
IC34	7486	14	7

Table 10: *Power supply connections for integrated circuits used in electronic logic described in this article.*

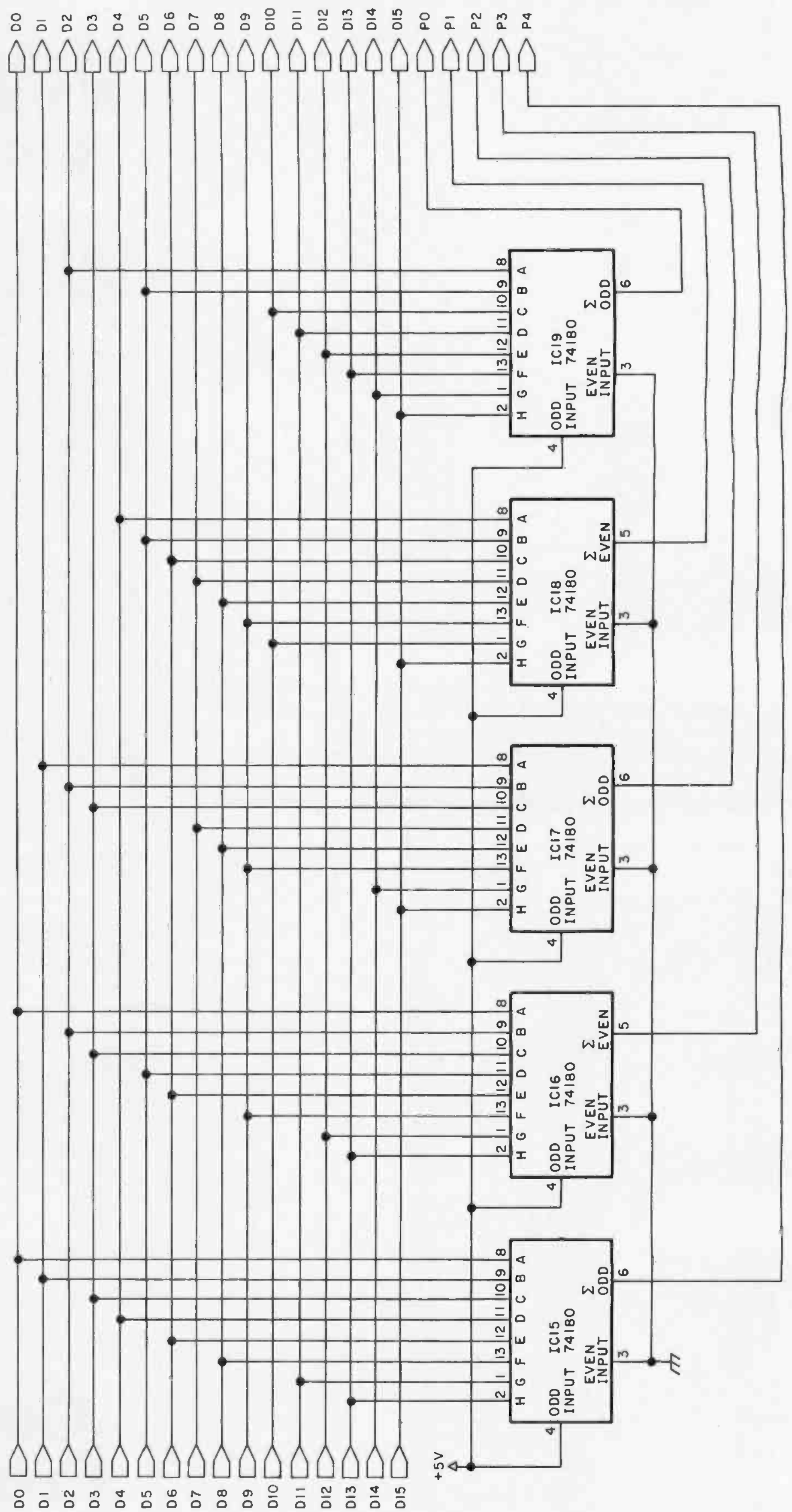

Figure 8a: *Schematic diagram of the circuit to encode 16-bit data into 21-bit words containing 5 parity bits.*

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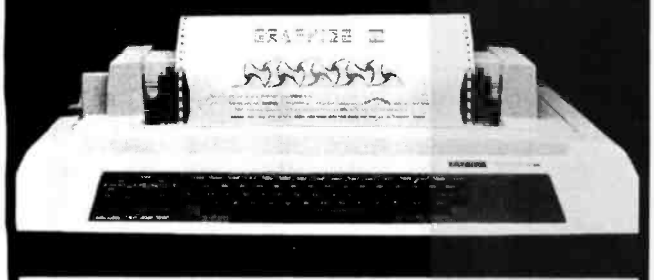

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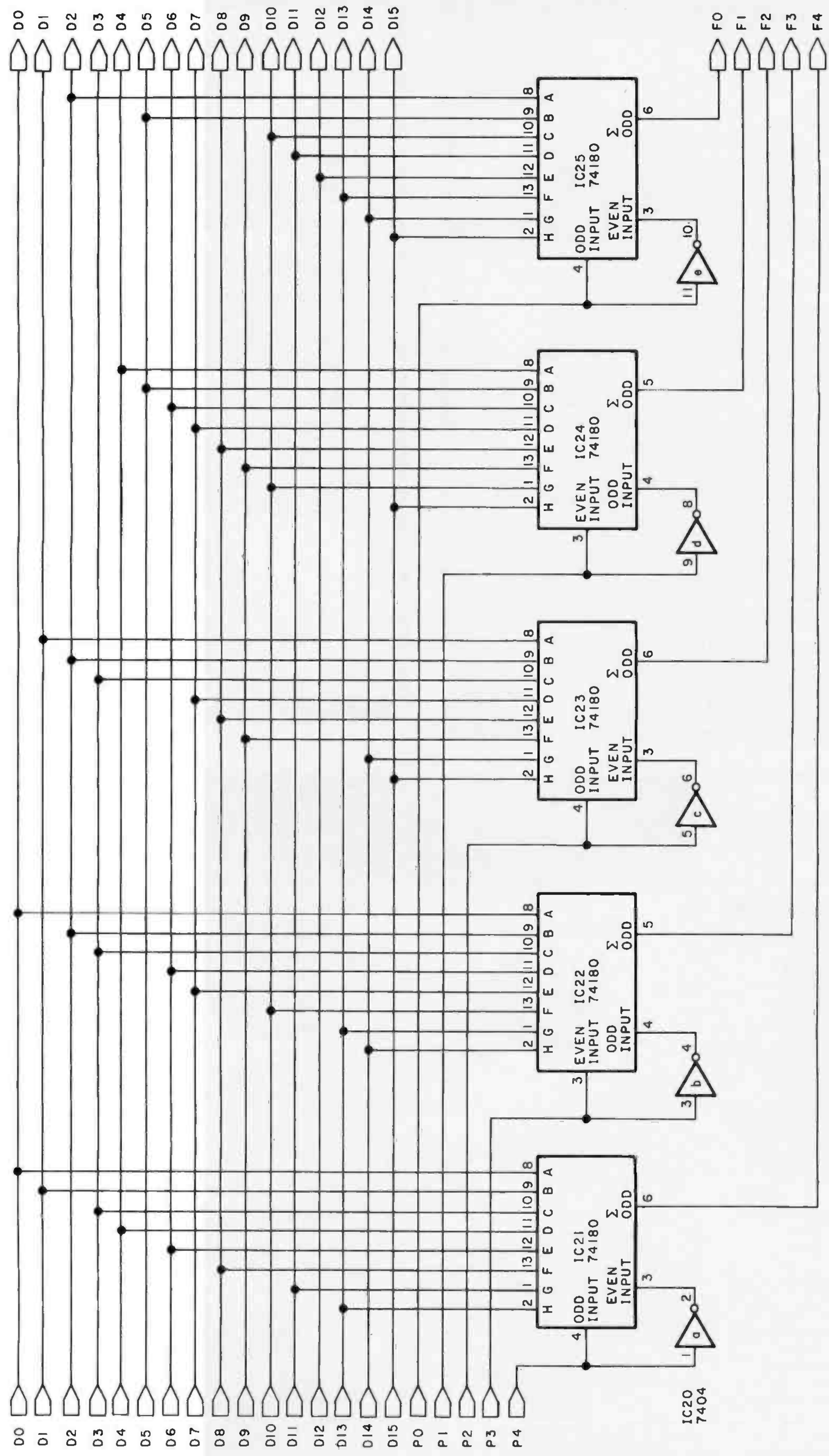

Figure 8b: *Schematic diagram of the circuit which traps errors from the encoded 16-bit data. Five error-detecting bits are sent to the error-correcting circuit of figure 8c.*

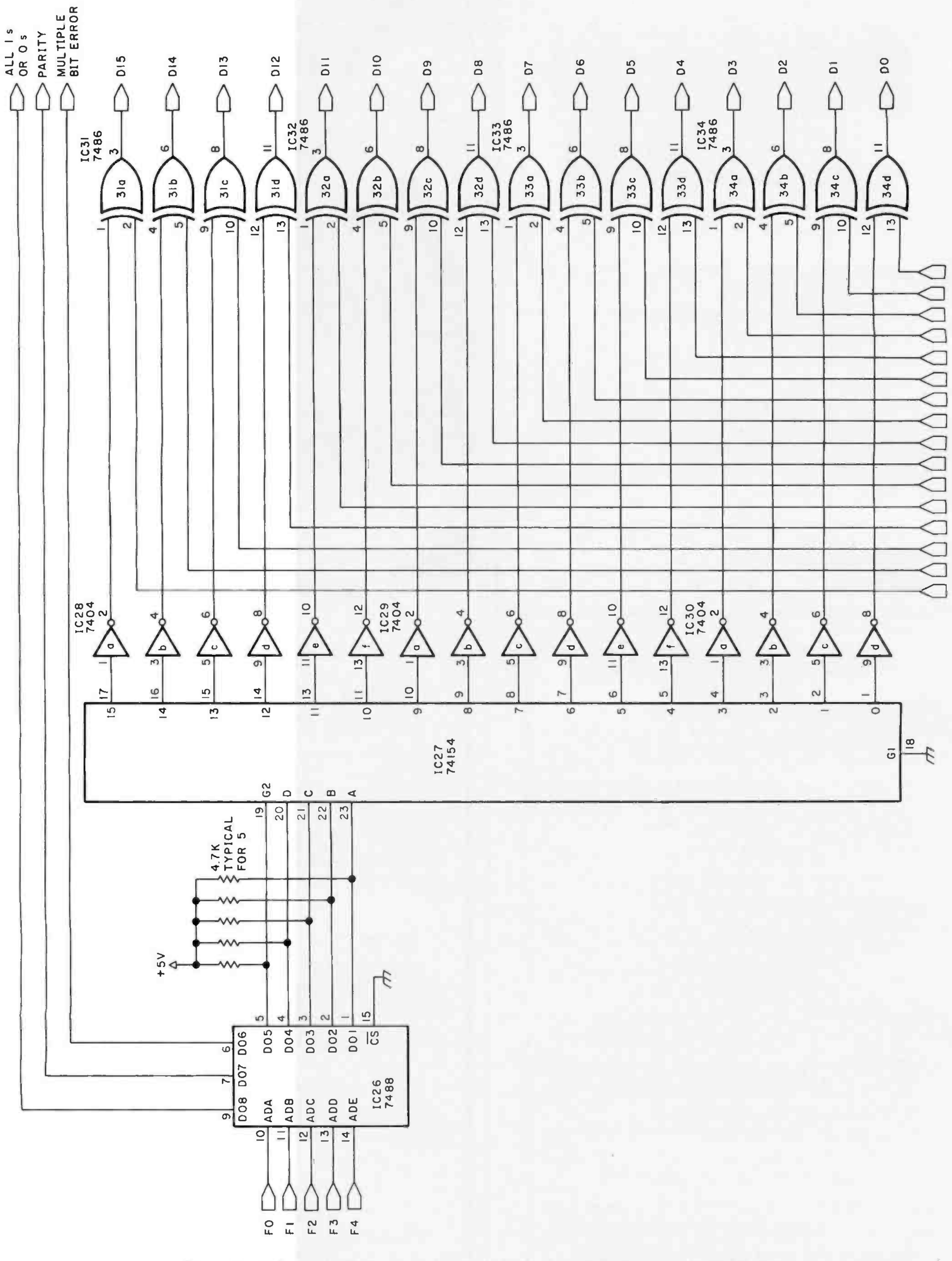

Figure 8c: *Schematic diagram of electronic logic that corrects errors in 16-bit data.*

Text continued from page 262:
parallel-to-serial conversion during a write operation, and a serial-to-parallel conversion during a read process. Details of this hardware will depend upon the actual data-transfer logic present in existing systems.

Locating single errors is accomplished by interpreting the fault code generated by the error-detection logic. This interpretation is done by use of an 8-bit by 32-word programmable read-only memory (8223/7488) which produces a binary output corresponding to the error-bit position in the data word. Error correction is achieved by loading the binary pointer into a 4-to-16 line demultiplexer that flags the proper bit line and corrects the fault with an exclusive-OR inversion. (See figure 10.) With an 8-bit system, the inconvenience of programming the read-only memory may be avoided by loading the fault code directly into the demultiplexer and then "picking off" the corresponding output.

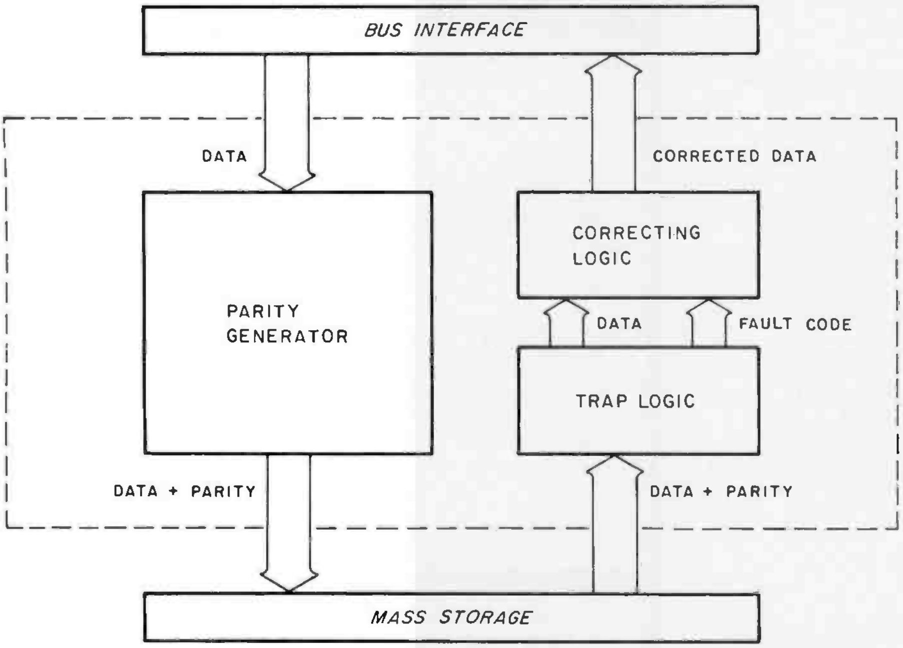

Figure 9: *Block diagram of data flow through the error-checking and correcting system. The extra parity bits are never seen by the processor, and make the system transparent from the point of view of the system bus.*

Treatment of Multiple Errors

Although single-bit errors are far more common, multiple failures within one data word can and do appear. For all intents and purposes, these are uncorrectable— particularly in longer data words. Prohibitively extensive logic would be required to locate multiple-fault bits; therefore, these errors are simply trapped to cause a processor interrupt. The

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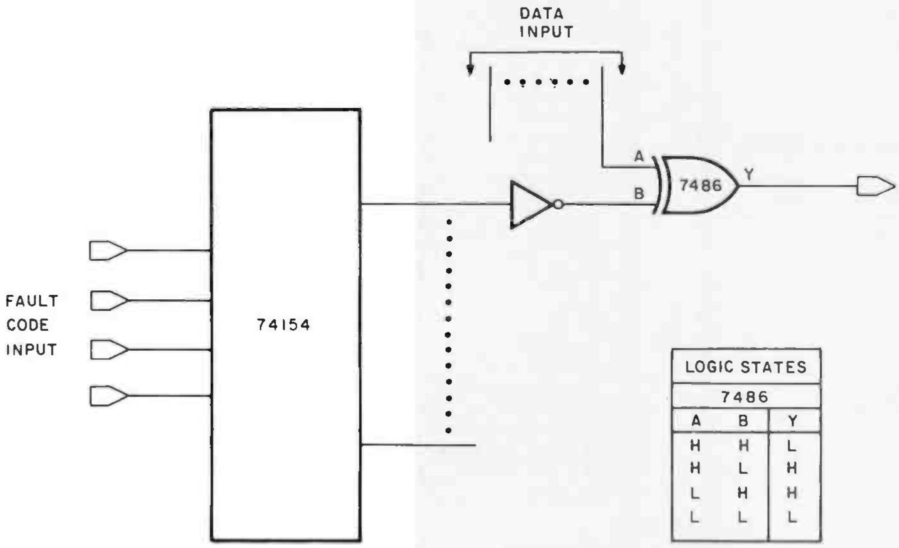
loader program can either abort the data transfer immediately, initiate a second read attempt from the last record, or display an error message on the computer terminal prompting direct operator intervention.

Theoretical Advances

As reviewed by Peterson and Weldon, the Hamming algorithm falls in the category of *cyclic codes*. (See reference 3.) In cyclic codes, executing a one-unit right-shift operation on any symbol in the complete code set will produce a binary bit pattern identical to that of one of the *other* members of the code set. Since Hamming's initial publication, an extensive array of cyclic codes has been derived. Perhaps the best known are the Bose-Chaudhuri-Hocquenghem (BCH) codes, which are related to the Hamming algorithm.

The BCH codes actually represent a generalized expansion that is particularly suited to coping with multiple-bit errors. None of these newer solutions offer major advantage over the basic Hamming check when correcting an 8-bit data word. Several mathematical difficulties are encountered when attempting to derive more effective encoding procedures. Not only is word length relatively short in these systems, but it can be shown that code redundancy overhead can be minimized to a tolerable level in only a small number of cases.

The alternative method, which is not unreasonable, would be to encode and decode entire data blocks, as opposed to individual data words. This would take advantage of the increased coding efficiency found for the longer codes, but would probably require a software implementation to minimize hardware design and expense. Such an approach would certainly increase system reliability, but it would defeat the purpose of increasing the speed and efficiency of data transfer to and from mass storage, since the processor would spend considerable time encoding and decoding the parity and data blocks before and after each data transfer. ■



LOGIC STATES		
7486		
A	B	Y
H	H	L
H	L	H
L	H	H
L	L	L

Figure 10: *Detail of the error-correcting logic. Error correction is achieved by loading a binary pointer into a 4-to-16 line demultiplexer that flags the proper bit line and corrects the fault with an exclusive-OR inversion. Eight-bit systems may load the fault code directly into the demultiplexer and avoid the use of a read-only memory.*

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1. Hamming, R W, "Error Detecting and Error Correcting Codes," *Bell System Technical Journal*, Volume 26 Number 2 pages 147 thru 160, American Telephone and Telegraph Company, 1950.
2. West, J T, "Product Development Profile: Data General Corporation," *Electronics* Volume 48 Number 23 pages 130 thru 136, November 13, 1975.
3. Peterson, W Wesley and E J Weldon Jr, *Error-Correcting Codes*, Second Edition, MIT Press, Cambridge 1972.
4. Sellers, F, Hsiao, M Bearnson, L, *Error Detecting Logic for Digital Computers*, IBM Corporation Systems Development Division, McGraw-Hill.

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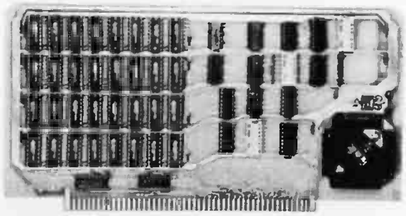

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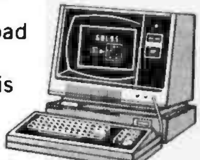

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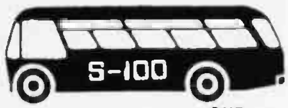

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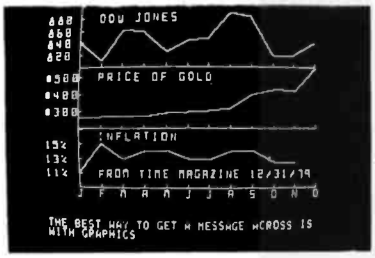

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SID — Symbolic Instruction Debugger for the 8080. Allows multiple break points with user set pass counter. Displays user labels during debugging when used with MAC. Greatly reduces hard-copy listing requirements. Includes back-trace and histogram utilities. A must for serious software development. .... **$85/$15**

ZSID — Same as SID except incorporates complete Z80 instruction set and uses Z-80 mnemonics. .... **$95/$15**

DESPOOL — Allows simultaneous printing of disk files and user access to other programs. No need to stop production while lengthy printouts are in progress. .... **$45/$5**

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ACCOUNTS RECEIVABLE — A complete open item or balance forward system. Operates alone, or interfaces with General Ledger. Produces customer statements, aged trial balance, on-line inquiry, sales reports, reminder notices and more. ...... **$695/$25**

ACCOUNTS PAYABLE — A powerful cash management system. Aged account statements, writes checks, cash requirements projection, General Ledger update and more included. Stand alone operation or interfaces with General Ledger and QSORT.............................. **$695/$25**

NAD — Name and Address System - Stores mailing lists on disk. Prints mailing labels or lists additional references information. Selective data extraction. .... **$75/$10**

QSORT — A generalized, full disk sort/merge package. Fast and flexible. Multiple key sorting. .... **$95/$15**

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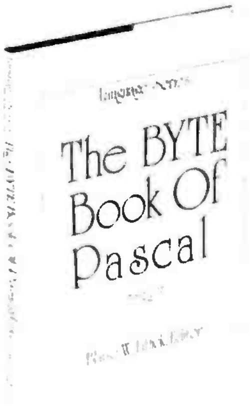
The BYTE Book of Pascal

Edited by Blaise W. Liffick

Based on the growing popularity of Pascal as a programming language, numerous articles, language forums and letters from past issues of BYTE magazine have been compiled to provide this general introduction to Pascal. In addition, this book contains several important pieces of software including two versions of a Pascal compiler - one written in BASIC and the other in 8080 assembly language; a p-code interpreter written in both Pascal and 8080 assembly languages; a chess playing program; and an APL interpreter written in Pascal.



$25.00 Hardcover pp. 342
ISBN 0-07-037823-1

YOU JUST BOUGHT A PERSONAL WHAT?

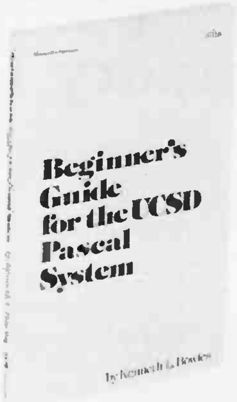
by Thomas Dwyer and Margot Critchfield

Whether you are a novice programmer or an experienced computer user, this book is filled with practical ideas for using a personal computer at home or work. It will take you through the steps necessary to write your own computer programs, and then show you how to use structured design techniques to tackle a variety of larger projects. The book contains over 60 ready-to-use programs written in Microsoft and Level II BASIC in the areas of educational games, financial record keeping, business transactions, disk-based data file and word processing. **$11.95 pp. 256 ISBN 0-07-018492-5**

Beginners Guide for the UCSD Pascal System

by Kenneth Bowles

Written by the originator of the UCSD Pascal System, this highly informative book is designed as an orientation guide for learning to use the UCSD Pascal System. For the novice, this book steps through the System bringing the user to a sophisticated level of expertise. Once familiar with the System, you will find the guide an invaluable reference tool for creating advanced applications. This book features tutorial examples of programming tasks in the form of self-study quiz programs. The UCSD Pascal Software Systems, available from SofTech Microsystems Inc, 9494 Black Mountain Road, San Diego CA 92126, is a complete general purpose software package for users of microcomputers and minicomputers. The package offers several interesting features including:



- Programs which may be run without alteration on the General Automation or DEC PDP-11 minicomputers, or an an 8080, 8085, Z80, 6502, 6800, or 9900 based microcomputers.
- Ease of use on a small, single-user computer with display screen and one or more floppy disk drives.

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The NCC:
New Emphasis on Personal Computing

What's happening in personal computing? The American Federation of Information Processing Societies, Inc (AFIPS) is banking that you'll find out at the National Computer Conference's Personal Computing Festival, to be held on May 20-22 in Anaheim, California at the Anaheim Convention Center. In the 3 years that personal computing has had a separate exhibit area at the NCC, the number of exhibitors has increased from 76 to 154. Over 20% of those who came to the NCC last year registered specifically for the Personal Computing Festival, and over half of the 60,000 plus attendees visited the Festival.

The booming show-attendance figures reflect the fast growth of the personal-computing industry as a whole. Highlights include the Apple Computer Company's expectations to triple its sales by the end of 1980. Commodore International computer sales may increase by a factor of 2 during the first quarter of 1980, and Radio Shack expects similar increases. According to industry estimates, the market value of personal-computer software sold in 1980 could surpass $150 million.

Judging from the attendance at last March's West Coast Computer Faire in San Francisco (approximately 20,000), there is an ever-increasing interest in personal computing among a wide variety of people. We expect to see a trend toward more sophisticated software at the 1980 NCC Personal Computing Festival. There will be a flood of new Pascal packages, new simulation programs, the appearance of new Forth software (look for the special section on the Forth language in the August 1980 BYTE), as well as intriguing new hardware like Microsoft's new Z80 processor circuit card for the Apple computer that allows Apple owners to use programs written to run under Digital Research Corporation's CP/M operating system. Word-processing and small-business software are two other rapidly growing areas that will be well represented at the conference.

Will some major consumer electronics companies enter the personal computer market? Is there a move toward some standardization in the microcomputer industry? Will Japanese companies make any major moves into personal computing? [Nippon Electric Company (NEC) is rumored to be unveiling a new computer at the show]. We'll keep our eyes open at the show to find out! ■

Personal Computing Festival
Preliminary List of Exhibitors

ABC Computer Inc
American Word Processing Co
Apple Computer Co
Applied Digital Data Systems Inc
Artec Electronics Inc
Atari

BASF Systems
Benwill Publishing Corp
BYTE Publications Inc

California Computer Systems
Cardamation Co
Centronics
Comprint
Compucolor Corp
Compucorp
Computer City
Computer Textile
Computerworld
Computhink
Control Data Corp
Corvus Systems Inc
Creative Computing
Cromemco Inc

Diablo Systems Inc
Dilithium Press

Electronic Data Systems-Evolution I
Executive Information Systems Inc
Exidy Inc

Findex Inc

Harris Technology
Hayden Book Co Inc
H & E Computronics
Heath/Zenith
Hewlett-Packard Co

Industrial Micro Systems
International Memories Inc (IMI)

Jade Computer Products

Leedex Corp
Lobo Drives International
LRC/An Eaton Co

3M-Data Recording Products Div
MAS (Micro Application Systems Inc)
Memory Media Products
MicroAge
Microamerica Distributing Co Inc
Microcomputer Technology Inc
Micromail
MicroPro International Corp
Microsette Co
Microsoft

NEC America Inc
North Star Computers Inc

Omni Magazine
Osborne/McGraw-Hill

Personal Software
Priam
Prodigy Systems Inc

RCA MicroComputer Products
Radio Shack
Realizations Etudes Electroniques (R2E)
Rockwell Microelectronic Devices

SD Systems Inc
Sharp Electronics Corp
Smoke Signal Broadcasting
Spectra Logic Corp
Sybex Inc

TEI Inc
TSA Software

Xymec

Back, and Bigger than Ever.

NCC Personal Computing Festival

May 20-22, Disneyland Hotel

So great is the interest in personal computing, so dynamic is the personal computer industry, that this year's Personal Computing Festival is again being held separate from the rest of NCC, at the Disneyland Hotel.

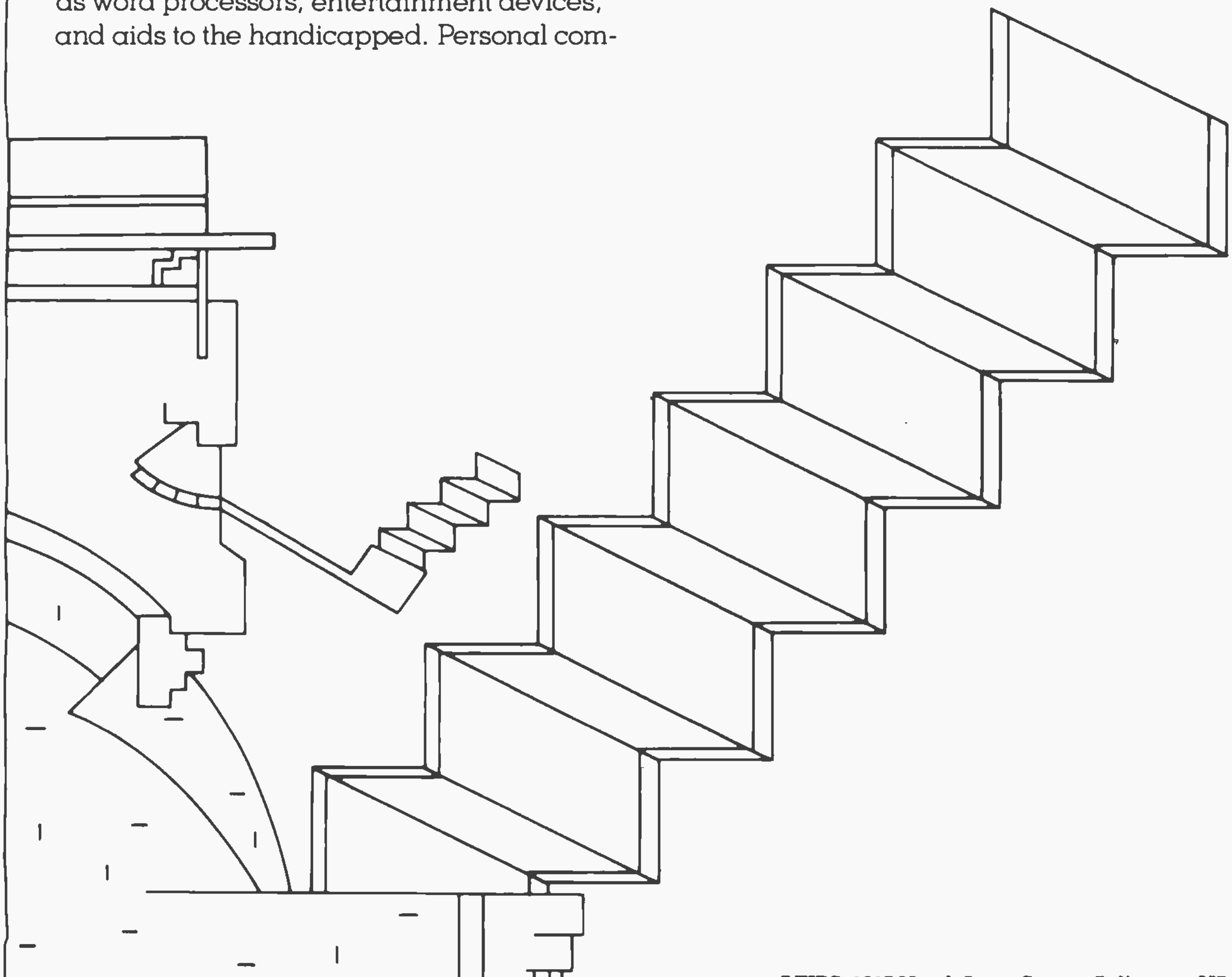
The 3-day festival features its own impressive roster of exhibitors plus over 50 learning sessions on every aspect of personal computers and their use.

Personal computers at home, at school, and in the executive suite. Personal computers as word processors, entertainment devices, and aids to the handicapped. Personal computer operating systems, programming languages, and software evaluation.

In addition, we've set aside a special area where demonstrations of personal computers will be conducted throughout the show. And we're awarding prizes for the most interesting use of personal computers.

If you're coming to NCC '80, be sure to make The Personal Computing Festival part of your visit.

Who knows—you may even win a prize.



AFIPS, 1815 North Lynn Street, Arlington, VA 22209

Circle 231 on inquiry card.

Personal Computing Festival Program Schedule

May 20 — Tuesday — 10:00 AM
High-Level Languages
Pascal Part I
Jim Gagne

Word Processing
Shopping by Objectives
Bill Radding

Portable Personal Computing
Jim Flournoy

1:00 PM
Higher-Level Languages
Pascal Part II
Jim Gagne

Computer Hardware Considerations & Applications
L Silvern

Forth Business Applications
Jim Flournoy

2:30 PM
Networks You Can Access With Your Personal Computer
Cliff Barney

May 21 — Wednesday — 10:00 AM
Using Computers to Overcome Disability Handicaps
Part I
Jeff Moyer
Mary Anne Glicksman

The Future of Personal Computing
Panel
Verne Kallejian

Operating Systems
Roger Vass

1:00 PM
Using Computers to Overcome Disability Handicaps
Part II

Computer Networks-Technical
Craig Vaughn

Software Evaluation
Tom Williams

2:30 PM
Computer Music
Carl Helmers

May 22 — Thursday — 10:00 AM
Medical Computing for Microprocessors
Jim Gagne

Data Base Management
Doug Seeley

Computers In Education
Chris Morgan

1:00 PM
Use of Computers in Kindergarden thru Ninth Grade
Flora Russ

Business Applications
Nancy Leeper

Computers In Education Panel
Chris Morgan

2:30 PM
Programming Potpourri

1980 NCC List of Exhibitors

Able Computer
Addison-Wesley Pub Co Inc
Advanced Systems Inc
AFIPS Press
Aham Inc/Rubber Urethane
Alanthus Data Communications Corp
Alpha Data Inc
Alpha Micro
AM International
Amco Engineering Co
American Magnetics Corp
American Terminal Leasing
Ampex Corp
Anadex Inc
Anderson Jacobson Inc
Ann Arbor Terminals Inc
Applied Digital Data Systems Inc
Applied Magnetics Corp
Aspen Ribbons
Association for Computing Machinery
Atlas Energy Systems
Audiotronics Video Display Div
Auerbach Publishers Inc
Aydin Controls

Ball Corp
BASF Systems
Basic Four Corp

Battelle Memorial Institute
BDT Buro-und Datenztchnik Gabil
Beehive International
Bell & Howell Display Devices
Bell System
Benson-Varian Int
Benwill Publishing Corp
Berger-Lahr Corp
Boschert Inc
British Trade Development Office
BTI Computer Systems
Burroughs Corp

CalComp
Caracters USA Inc
Centigram Corp
Centronics
Century Data Systems—A Xerox Co
Chromatics Inc
Cii Honeywell Bull
Cipher Data Products Inc
Circuit Assembly Corp
Clinton Electronics Corp
CMP Publications
Codex Corp
Compugraphic
Computer Automation
Computer Decisions
Div of Hayden Pub Co Inc
Computer Design
Computer Devices
Computer-Link Corp
Computer Power Systems
Computer Products Magazine
Computer Roomers Inc
Computer Science Press Inc
Computer Transceiver Systems Inc
Computerworld Computer Business News (CW Communications)
Computron Technologies Corp
Contal Corp
Conrac
Continental Resources
Control Data Corp
Cortron & Licon Div IIW
Cullinane Corp
Curtis 1000 Inc
Custom Systems Inc
Cyberex Inc

Daily Business Products
Data Access Systems Inc
Data Communications/McGraw-Hill Publications
Data Dimensions Inc
Data Electronics Inc
Data General Corp
Datagraphic
Data-Mate/Maine Manufacturing Co
Datamation
Datamedia Corp
Data Motion
Data Printer Corp
Datapro Research Corp
Data Processing Management Assoc
Data Processing Power
Dataran Corp
Data Specialities Inc
Dataware Inc
Datum Inc

Deciteck
Delta Data Systems Corp
Deltec Corp
Diablo Systems Inc
Digi-Data Cor.
Digi-Log Systems
Digital Associates Corp
Digital Computer Controls
Digital Equipment Corp
Digitech Data Industries Inc
Digitronics Div Contec Information Systems
Distributed Logic Corp
Diva Inc
Documation Inc
DOSC Inc (Digitron)
Dranetz Engineering Labs Inc

Eastman Kodak Inc
Edge Technology Inc
Educational Data Systems
Eichner Systems Inc
Electronic Component News
Electronic News
Elgar Corp
Emergency Power Engineering Inc
Emerson Electric Co
Emulex Corp
Epic Data
Epicon Inc
Epson America Inc
Exide Power Conversion ESE Inc

Facit Inc
Fairchild Camera & Instrument
Floating Point Systems Inc
Florida Data Corp
Four-Phase Systems
Fujitsu Ltd

General Automation Inc
General DataCom Industries Inc
General Electric Co
General Robotics Corp
General Terminal Corp
GMT Automatic Inc
Graphic Controls
GTE Sylvania

Hamilton Avnet
Harris
Haveg Industries Inc
Hazeltine Corp
HEI Inc
Hitachi America Ltd
Honeywell Information Systems Inc
Houston Instruments
Hutchinson Industrial Corp

IBM Corp
ICI American Inc
IEEE Computer Society (Computer Magazine)
Incoters Corp
Industrial Engraving Co Inc
Information Processing Inc
Informer Inc
Infosystems Magazine/Hitchcock Pub Co
INMAC

Innovative Electronics Inc
Input
Integral Data Systems
Integrated Software Systems Corp (ISSCO)
Intelligent Systems Corp
Interdyne Co
Interface Mechanisms Inc (Intermec)
International Data Corp
International Mathematical & Statistical Libraries Inc (IMSL)
International Power Machines Corp
Interstate Electronics Corp
Intertec Data Systems Corp
C Itoh Electronics Inc

Japan Market Consultants Div Engineers International Inc

Kennedy Co
Key Tronic Corp
Knickerbocker Case
Kybe Corp

Liebert Corp
LogAbax SA—US Div

3M
Magnavox Display Systems
Mag-Tek Inc
Management Science America
Mathematics Products Group Inc
Maxell
McCormack & Dodge Corp
McGraw-Hill Book Co
MDB Systems Inc
Megatek Corp
Melco Sales Inc
Memorex Corp
MFE Corp
Micon Systems Inc
Micon Industries
Microcomputer Systems Corp
Microdata Corp
Micro Peripherals Inc
Micropolis Corp
Micro-Term Inc
MiniComputer Systems Inc
Mini-Micro Systems Cahmers Pub
Monolithic Systems Corp
Mostek Corp
Motorola Inc
MBI Systems Corp

Nanodata Corp
National Computer Communications Corp
National CSS
National Electric Cable
National Technical Information Service
NCR Corp
NEC Information Systems Inc
Network Systems Corp
Newman Computer Exchange Inc
Nicolet Zeta Corp
Nippon Peripherals Ltd
Nixdorf Computer Corp
Northern Zelecon Systems Corp
Nortronics Co Inc
Nova Electric Manufacturing Co

Ohio Scientific Inc
Okidata Corp
Ontel Corp

Panasonic Co
Paradyne Corp
Peripheral Dynamics Inc
Perkin-Elmer
PerSci Inc
Pertec Computer Corp
Philips Test & Measuring Instruments Inc
Plessey Peripheral Systems
PolyMorphic Systems
Practical Automation
Precision Handling Devices
Prentice Corp
Prentice-Hall Inc
Prime Computer Inc
Princeton Electronic Products
Printronix Inc
Pro-Log Corp

Qantel Corp
Qantex
Quantor
Qume

Rascal-Milgo Inc
Racal-Vadic
Radio Shack
Ramtel Corp
Randomex Inc
Raymond Engineering Inc
Remex Div/Ex-Cell-O
Resource Management—Div of Cutler Williams
Ranco Electronic Systems

SAS Institute Inc
Scientific Measurement Systems Inc
SCI Systems Inc
Sheldon Industries Inc
Shugart Associates
Society for Computer Simulation
Software AC
Sola—A Unit of General Signal
Spatial Data Systems Inc
Specialized Products Co
Sperry Univac
Storage Technology
Structured Methods Inc
Summagraphics Corp
Systems Furniture Co

TAS Products Co
Tally Corp
Tandberg Data Inc
Tandem Computers Inc
T-Bar Inc
TEAC Corporation of America
Technology Transfer Institute
Techtran Industries Inc
Tektronix Inc
Teledyne Instruments
Telefile Computer Products Inc
Telenet Communications Corp
Teletype Corp
Televideo Inc
Telex Computer Products
Terak Corp
Termiflex Corp
Tesdata Systems Corp
Texas Instruments
Timeplex Inc
Tokyo Juki Industrial Co Ltd
Topax Electronics
Toshiba International Corp
Trilog Inc
Triple I Inc
Tymnet Inc

Universal Data Systems

Van Nostrand Reinhold
Van San Corp
Vector Graphic Inc
Verbatim Corp
Versatec
Victor Data Products
Vistron Corp
Vu-Data Corp

Wabash Tape Corp
Wall Street Journal
Wang Labs Inc
Warrex Computer Corp
Wavetek Data Communications
Wescorp
Western Peripherals
Westrex OEM Products
John Wiley & Sons Inc
Wintek Corp

Xerox Business Systems

Yourdon Inc

Zenith Radio Corp
Zilog Inc

NCC Main Conference Proceedings

During each of the 4 days of the NCC, there will be discussions and papers related to the following major topics. A detailed schedule of events will be available at the conference.

Computer Architecture
Covers design of equipment and supporting technologies, and distribution through networking. Includes decisions relating to supersystems, survivability systems and data-base installation.

Applications of Computer Technologies
Explores the use of computers in entertainment, microcomputers and their impact, management of the computing tool and staff, and the role of inhouse and academic education and training.

Data Base Management & Communications
State-of-the-art, user-oriented sessions on the storage, retrieval, and transfer of data. From hardware considerations to natural-language access to a data base.

Office Automation
Every computer-related aspect of this explosive growth area, including electronic mail. How computers are used, managed, and integrated in an overall automated office.

Simulation Technologies
Where we've been, where we are, and where we're going with computer modeling. Its value to small and large businesses and its role in decision support will be discussed. Special sessions on solar energy-simulation modeling will be included.

Software Engineering Technologies
Sessions on programming standards, software quality assurance, languages, and requirements engineering. Emphasis upon the needs and responsibilities of the user.

Social Dynamics and Special Topics
A broad spectrum of critical subjects: data security, legal issues, transborder data flow, societal impact, voice communications, venture capital and its effect upon technology.

Image Processing and Computers in Medicine
How image processing is used and will be used in industry and medicine. Trends in facsimile data coding, compression, and standards. How doctors use image-analysis display.

Professional Development Seminars
Full and half-day seminars for the professional who wants to come away with solutions and ideas he can implement now. Half-day seminars tie in with regular program sessions.

What's New?

MISCELLANEOUS

RS-232C-Compatible Paper-Tape Reader

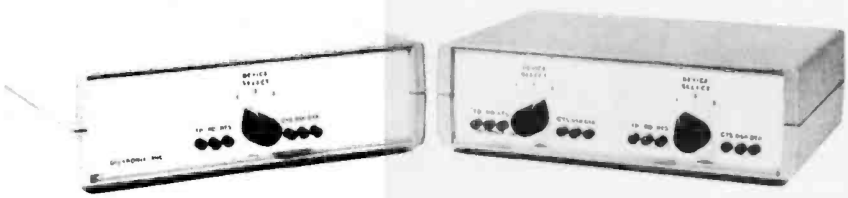
The Model 612 stand-alone paper-tape reader has the ability to read five- to eight-level tape and to transmit seven to eleven frames per character at 50 to 9600 bits per second (bps). It also features starting and stopping on character at all speeds, manual control or automatic on and off, 90 to 260 VAC, 50 to 60 Hz, and even, odd, or no parity. RS-232C, current loop, or parallel outputs are available. The price of the 612 is $656 to $854. Contact Addmaster Corp, 416 Junipero Serra Dr, San Gabriel CA 91776.

Circle 562 on inquiry card.

Bidirectional Interface for the PET

This interface package is a combination of hardware and software that enables any model of the Commodore PET to send and receive data on printers, terminals, and other peripherals. ASCII/ISO-7 characters are sent from the PET in serial or parallel mode but are received in serial mode only. Serial speeds are selectable at rates up to 240 characters per second (cps). The interface is available for either 20 mA current loop or transistor-transistor logic (TTL) serial or parallel. The machine-language program may be stored anywhere in programmable memory; the code used to terminate a message is selectable. The price for the package is £70 (approximately $160). Further details from Allen Computers, 16 Hainton Ave, Grimsby, South Humberside, ENGLAND.

Circle 563 on inquiry card.



Centronics-Compatible Switching and Monitoring Units

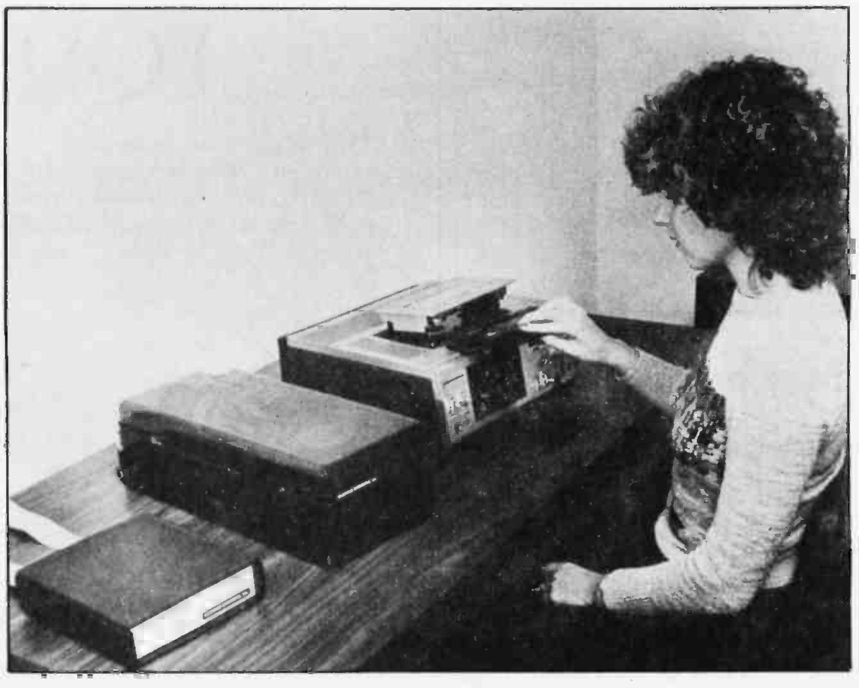
Giltonix Inc, 450 San Antonio Ave, Suite 44, Palo Alto CA 94306, has introduced a family of switching and monitoring units. The GRS 232 units are used for interfacing, configuring, and monitoring computer terminals, printers, and other peripherals that comply with the RS-232 and the IEEE-488 specifications. The new family consists of four models: the GRS 232-P24, -S24, -2P24, and -2S24. Each unit consists of a standard three-way switching system and an optional interface monitor. All the units can be cascaded and thereby allow interfacing of more than five devices. The systems can be ordered with signal monitoring capability. The units are priced at approximately $130.

Circle 564 on inquiry card.

Large Capacity Winchester Backup from Corvus

This backup system, the Mirror, employs a standard video cassette with a total capacity of 100 megabytes. In less than ten minutes, the 10 megabytes of data on the Corvus 8-inch hard disk can be transferred to a Mirror cassette. The video cassette should be of the VHS, Beta, or U-Matic format. If a larger data capacity is required, a reel-to-reel videotape recorder can be used. This approach to storage embodies standard television technology and proven cassette reliability. The Mirror uses the same Z80 and Corvus interface bus as the Corvus disk. The Mirror will interface to the Apple II, TRS-80, S-100, and LSI-11 computers. Data format in the Mirror is fully compatible with the standard NTSC signal. For error detection, the Mirror contains cyclic redundancy check (CRC) detection hardware. If unattended or remote operation is desired, a low-cost option is available to interface the Mirror to the Panasonic Omnivision NV-8200 cassette recorder allowing archival storage files to be created without operator interaction. The price of the Mirror is $790. Write Corvus Systems, 900 S Winchester Blvd, San Jose CA 95128.

Circle 565 on inquiry card.



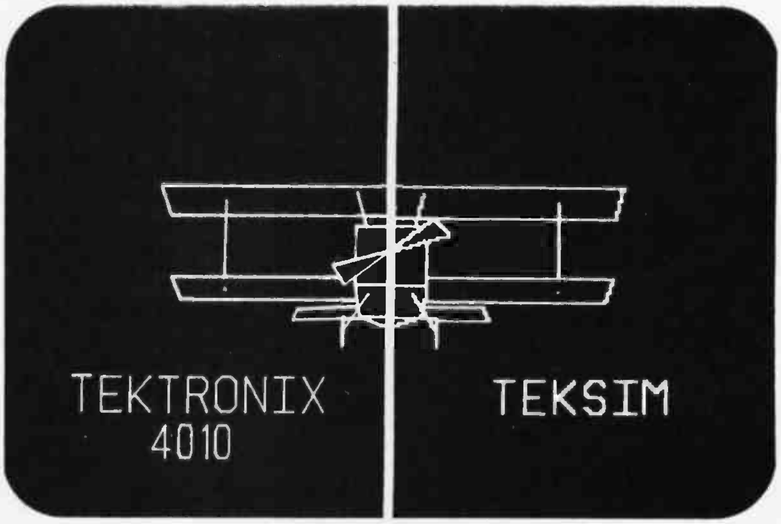
What's New?

MISCELLANEOUS

Speechlink Voice Recognition for S-100 Computers

Heuristics has announced its Model 20S-64 Speechlink 64-word voice input unit for S-100 bus computers. The 20S-64 is a speaker-programmed, isolated word-recognition device that recognizes up to 64 words at each instant. Vocabulary sets may be stored away and recalled when needed. This system will produce a usable vocabulary of several hundred words for data entry and system control applications. Word recognition is completed in 200 ms. Successive words must be separated by at least 100 ms of silence. Preprogramming of the Speechlink is necessary. The unit requires 2 K bytes of programmable memory for programs, and 64 bytes for each word in the vocabulary, up to a maximum of 4 K bytes. The price is $299 including board, microphone, and manual. Contact Heuristics Inc, 1285 Hammerwood Ave, Sunnyvale CA 94086.

Circle 441 on inquiry card.



Graphics Terminal Emulator for Apple IIs

TEKSIM, the Tektronix Simulator, employs distributed processing in its programming approach and uses the Apple's high-resolution plotting capabilities to emulate Tektronix 4010-series graphics terminals. No modification to the program in the remote computer is required to display or input graphic data. The TEKSIM-Apple combination features multicolored displays, selective erase, and a standard video output that lets any television set used with an RF converter function as a monitor. The suggested price for the plug-in device is $795, and it is available from ABW Corp, POB M 1047, Ann Arbor MI 48106.

Circle 442 on inquiry card.

Hardware and Software for Homebrewers

Snow Micro Systems Inc, POB 1704, Silver Spring MD 20902, provides low-cost hardware and software to personal computer users and clubs. Their bare boards are sold with schematics, layout drawings, and component lists. They are unassembled and come without parts. The company offers a troubleshooting service, if necessary. Some of their products include a front panel interface card, the Golem-80 S-100 Troubleshooter, a Station Controller Card, and more. Snow Micro software includes AMS-80 Version 5.8 debug packages, object code and source code, and other AMS-80 software related items. For prices and information, contact Snow Micro Systems at the above address.

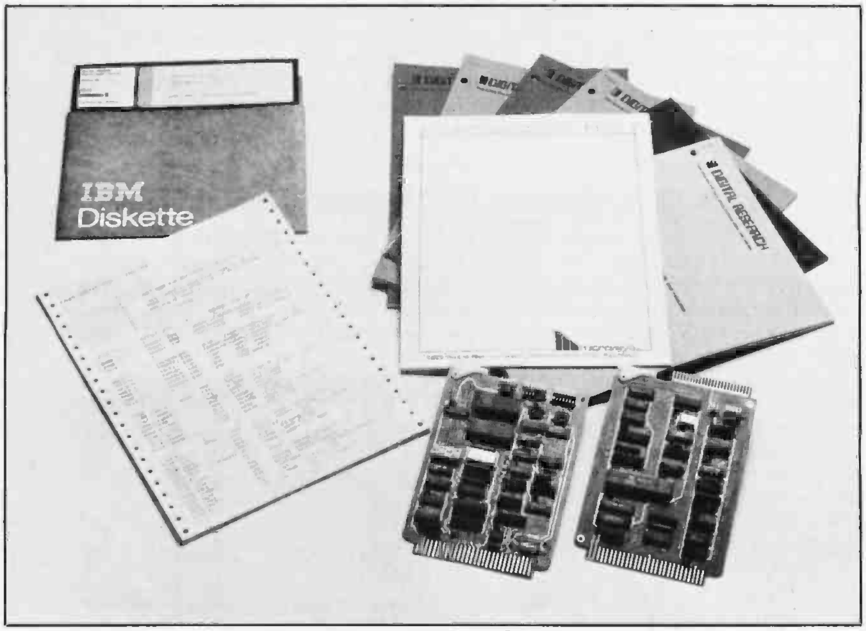
Circle 443 on inquiry card.

CP/M Package for the STD Bus

Micro/sys has developed a CP/M system for the STD Bus microcomputer card system. The Micro/sys package consists of two STD Bus-compatible cards, the SB8500 Floppy Disk Controller, the SB8420 Dual Serial Interface, and an eight-inch floppy disk containing the CP/M system. The SB8500 can control up to four floppy disk drives from a single STD Bus slot. The SB8420 provides communication with a console device, and a second serial port that can be used for printers and other devices. The cards are compatible with 8085 and Z80 microprocessors.

CP/M provides a disk file management, a text editor, and an 8080 assembler, a dynamic debugger, and various utilities. Price of the Micro/sys CP/M package is $695. For more information, contact Micro/sys Inc, 1353 Foothill Blvd, La Canada CA 91011.

Circle 444 on inquiry card.

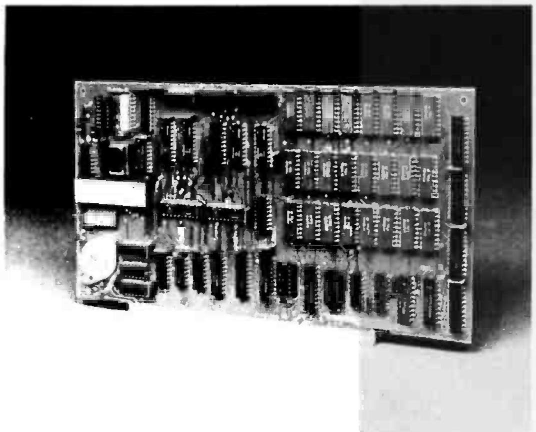


What's New?

MISCELLANEOUS

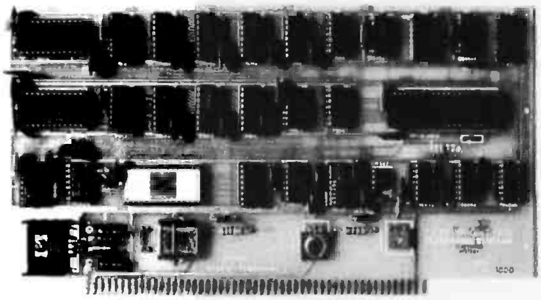
Video Graphics for S-100 Bus Systems

A single-card, high-density, computer-display system is being offered for the S-100 bus by International Product Development Incorporated (IPDI). The VG100 is designed for text-oriented applications. It has programmable fonts allowing any set of up to 256 characters to be defined in programmable memory with available software. The system can generate a combination of 16 gray levels or 16 colors, or combinations of both. The character field is 9 by 16 (or 144) pixels with a raster scan of 621 pixels. The entire character field can be changed at one time for fast animation. Adjoining character fields of any shape can be combined to create large continuous characters. The VG100 is configured in 12 K bytes of programmable memory and is selectable in three 4 K-byte blocks. The price is $645. For details, contact IPDI, 1708 Stierlin Rd, Mountain View CA 94043.



Circle 589 on inquiry card.

Video Terminal Board

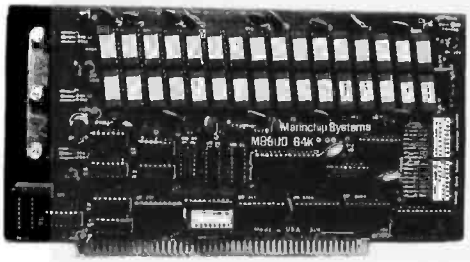


This board features full uppercase and lowercase, 5 by 7 dot matrix, 16 lines with 64 columns, and serial RS-232 input and output with parallel keyboard input. The data rate generator has a range from 75 to 1200 bits per second (bps) and is jumper-selectable. The board has 1 K byte of memory and an SFF96364 processor integrated circuit. The device is S-100 compatible. It requires ± 16 VDC at 100 mA and 8 VDC at 1A. The price is $199.95 in kit form. Contact Electronic Systems, POB 21638, San Jose CA 95151.

Circle 590 on inquiry card.

64 K Byte Memory for Heathkit/Digital H11

The CI-1103 memory module is designed for the Heathkit/Digital H11, LSI 11/2, and PDP 11/03 computers. The product uses 200 ns cycle time, type-4027, 4 K by 1-bit dynamic memory parts or 200 ns, type-4116, 16 K dynamic memory devices. The CI-1103 is available with either on-board distributed refresh or external refresh control logic. Data access time is 300 ns and cycle time is 525 ns. On-board memory-select is available in 2 K increments up to 128 K words of memory. Power consumption is under seven watts. The 8 K by 16 board is $390 and the 32 K by 16 board is $750. For information, contact Chrislin Industries Inc, 31352 Via Colinas #102, Westlake Village CA 91361.



Circle 591 on inquiry card.

Serial Interface Card for Apple II Computers

California Computer Systems' 7710A Asynchronous Serial Interface card enables the Apple II to communicate with all RS-232C serial devices. It is fully compatible with Apple Pascal. The card features selectable data rates from 50 to 19,200 bits per second (bps), 8- or 9-bit character transmission, and optional odd, even, or no parity. Software programmable interrupts, double buffered data input/output (I/O), and full handshaking are included. It is available in kit form or fully assembled and tested. The price for the card is $159.95. For more information, contact California Computer Systems, 250 Caribbean, Sunnyvale CA 94086.

Circle 592 on inquiry card.

Percom Board Interfaces Speak & Spell to Computer

Percom Data Co, 211 N Kirby, Garland TX 75042, has announced production of a printed circuit board which will interface the Texas Instruments Speak & Spell learning aid to a computer. The "Speak 2 Me 2" allows communication with a Speak & Spell in BASIC, so a computer can talk using the words and phrases of a Speak & Spell unit. The board is installed in the battery compartment. Installation involves disassembly and some modification of the Speak & Spell unit. The board with instructions, TRS-80 driver software, and a TRS-80 cable sells for $69.95. The cable connects to the printer port and may be adapted for other computers.

Circle 593 on inquiry card.

Head-Cleaning Floppy Disks from Lifeboat

Lifeboat Associates, 2248 Broadway, New York NY 10024, has an important product for floppy-disk systems: head cleaning disks. The head-cleaning floppy disks are manufactured by attaching a lint-free nylon mat to a mylar substrate. The design avoids damaging abrasion, which keeps head wear to within industry standards for normal magnetic media. The disk is used by inserting it into the drive in the same manner as a floppy disk, and loading the head for 30 seconds. It is recommended that this procedure be used once per day as prevention against oxide build-up. The disks are available in 5¼- and 8-inch sizes for $20 each, or $45 for three. Each disk is suitable for three months of daily use.

Circle 594 on inquiry card.

What's New?

PUBLICATIONS

Hardside Announces Expanded New Catalog

Hardside, a mail-order hardware company in Milford, New Hampshire, has announced the release of an expanded version of the Hardside catalog. Hardside features Radio Shack computer products at a discount price and also peripherals from other manufacturers which are suited to work with the TRS-80. The company specializes in computers and related hardware. The Hardside catalog is free from Hardside, 6 South St, Milford NH 03055.

Circle 572 on inquiry card.

Monthly Newsletter Covers the Office Computing Industry

Entitled the *Office Computing Industry Report* (OCIR), this monthly newsletter focuses on small-scale data processing, word processing, and data communications systems. OCIR also covers the merging of EDP and Business Machine distribution systems and support activities and the relationship of these new office computing systems to network-based information systems and distributed data processing. News analysis, market forecasts, new product reviews, vendor profiles, and technology forecasts are included. The *Office Computing Industry Report* is available from Vantage Research Inc, 2680 E Bayshore Rd, Mountain View CA 94043, for $195 per year in North America and $225 in Europe and Asia.

Circle 566 on inquiry card.

Supplies Catalog from Diablo

A 25-page brochure from Diablo Systems Inc, 24500 Industrial Blvd, Hayward CA 94545, illustrates and describes the variety of print wheels and ribbon cartridges designed for use on the company's Series 1640 and 1650, HyType, HyTerm, and matrix printers and terminals. The brochure contains a sample type line from all of the plastic and metallized daisy-wheel print elements. For copies of the brochure and the name of the nearest Diablo dealer, call (800) 227-2076, except in California where the number is (415) 443-2273.

Circle 567 on inquiry card.

S-100 Magazine Being Published

S-100 Microsystems is a new publication directed towards users of S-100 microcomputer systems. It is a forum on such S-100 topics as interfacing, CP/M, Pascal, Assembler, FORTRAN, and BASIC software. The magazine will also cover 16-bit microprocessors, multiprocessors, multitasking, timesharing, word processing, system development, data base management, scientific, and other applications and issues. It will be concerned with S-100 systems such as Cromemco, North Star, Intersystems, IMSAI, Poly Morphics, Processor Technology (Sol), Xitan, and others.

S-100 Microsystems is edited by Sol Libes. Sol has written 13 books, many magazine articles, and has edited several newsletters. He is the founder and past president of the Amateur Computer Group of New Jersey, the largest personal computer organization in the world. The first issue of *S-100 Microsystems* includes the complete proposed Institute of Electrical and Electronics Engineers (IEEE) S-100 Standard, the first part of a tutorial on CP/M, an article on modifying the SDS Video Board for Pascal editor functions, the source code for an 8080 disassembler, a directory of Computerized Bulletin Board Systems (CBBS), and more. *S-100 Microsystems* will be published six times a year. A sample copy is $2. For subscriptions and additional information, contact *S-100 Microsystems*, POB 1192, Mountainside NJ 07092.

Circle 568 on inquiry card.

Short Form Catalog and Price List

Sara-Tech Electronics Inc, POB 692, Venice FL 33595, has published a catalog which includes systems and peripherals from Cromemco, North Star, Centronics, Heath, and many more companies. They also have a listing for computer-paper forms for all systems. Sara-Tech sells systems, peripherals, and software of most major companies.

Circle 569 on inquiry card.

A Book on Computerized Typesetting

Donald Knuth, author of *The Art of Computer Programming*, has written *TEX and METAFONT, New Directions in Typesetting*, which describes new techniques in typesetting. Dr Knuth explains how TEX, originally designed for use in setting technical and mathematical text, can be applied to all computerized typesetting. METAFONT is a system for the design of alphabets. It is suited for implementation on raster-based devices that print or display text. With it, computers can draw new fonts of characters in seconds. TEX and METAFONT represent improvements in typesetting that will benefit the scientific and technical community. The book consists of three parts. The first is a lecture on mathematical typography; the two other parts describe TEX and METAFONT. The book costs $12 and is available from Dept TM:X, Digital Press, Educational Services, Digital Equipment Corp, 12-A Esquire Rd, N Billerica MA 01862.

Circle 570 on inquiry card.

Software Catalog for Heath Users

The Heath Users' Group has published a catalog of programs written by Heath users for all Heath computers. The programs described include games, financial applications, utilities, computer-assisted education, and amateur radio. The catalog lists the language and designated computer next to the program. Prices are given, along with services of the Users' Group. For more information, contact Heath Users' Group, Hilltop Rd, St Joseph MI 49085.

Circle 571 on inquiry card.

Intellivision from Mattel

Mattel Electronics is introducing six cartridges for its home computer system, Intellivision Intelligent Television. Soccer, Golf, Skiing, Boxing, Tennis, and Sea Battle join the existing fourteen cartridges, which range from sports and games to children's learning. Intellivision's Master Component contains a 16-bit microprocessor that delivers simulated sound effects, three-part harmony, and color reproduction. Two 12-button, hand-held controllers, each with four play-action keys, and a 16-directional control knob for movement of screen objects are included. The unit attaches to any television set.

The Keyboard Component uses programmed cassettes and features a keyboard and a digital cassette system with fast-forward and tape search. Its programs include Physical Fitness, Speed Reading, Stock Analysis, and Guitar Lessons. The Master Component will retail for approximately $300 or less. The Keyboard Component will cost around $550 and the cartridges will cost approximately $30, with the cassettes priced slightly under $30. For information, contact Mattel Electronics, 5150 Rosecrans Ave, Hawthorne CA 90250. Circle 586 on inquiry card.

Computer System from NNC

NNC Electronics, 15631 Computer Ln, Huntington Beach CA 92649, has released the System 80 computer. The System 80 uses a 4 MHz Z80 microprocessor and features a floppy-disk controller and two dual-density, 8-inch disk drives, 32 K bytes of programmable memory, two serial ports, and the CP/M operating system. The eight-slot S-100 card cage has five slots available for expansion. The desktop unit weighs less than 29 kg (65 pounds) and retails for $3995. Circle 587 on inquiry card.

Altos Announces a Hard-Disk System

The Altos Systems ACS8000-6 can take advantage of as much as 58 megabytes of hard disk storage. The system can control up to four 14.5-megabyte Shugart disks using Winchester-type technology. Altos designed the ACS8000-6 series so that it handles up to four floppy-disk drives. The floppy units could accommodate another 4.0 megabytes of on-line storage. The ACS8000-6 family comes with input/output (I/O) control to support two serial and two parallel ports in addition to the four serial ports to which the users are connected. The hard-disk controller features direct memory access (DMA) operation; firmware address checking; a high-speed first-in, first-out (FIFO) buffer; and intelligent sequencing. The controller firmware contains a routine that automatically double-checks all addresses before performing any disk writes. The FIFO enables the system to transfer data at a 7 million bits per second (bps). The system will support asynchronous, bisynchronous, and networking communications protocols and configurations. Prices range from $9450 for a single-user system with two floppy-disk drives and one 14.5-megabyte hard disk, to $14,260 for the four-user, 29-megabyte system with two dual-sided floppy-disk units. For details, contact Altos, 2338A Walsh Ave, Santa Clara CA 95050.

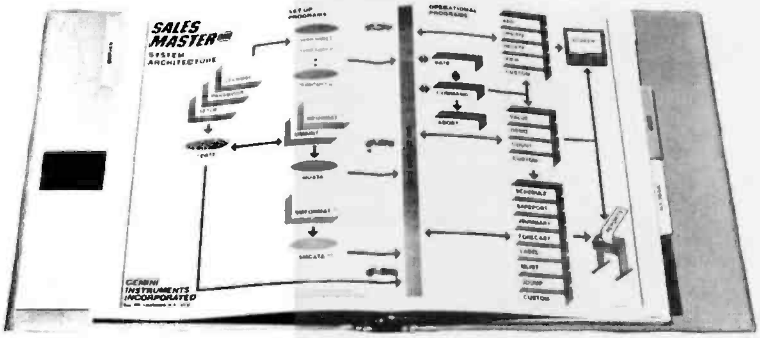
Circle 588 on inquiry card.

What's New?

SOFTWARE

A North Star Program for Salesmen

The Sales Master One is a collection of 22 programs designed by salespeople for salespeople. The Sales Master One is territory-oriented, allowing users to pinpoint selling activities to a particular location. The system generates reports on sales activities, forecasts, and schedules. Various other reports assist in daily selling efforts. The system has room for 400 jobs on one 5¼-inch floppy disk. The package contains a program that allows modifications to be made without the need to refer to the operations manual. A customized disk-operating system allows the package to be run on Cromemco, Dynabyte, and Processor Technology computers. Sales Master One comes on a 5¼-inch floppy disk with a manual for $375. Contact Gemini Instruments Inc, POB 205, Larchmont NY 10538.



Circle 573 on inquiry card.

Software from Compucolor

Compucolor Corp, POB 569, Norcross GA 30091, has released several software programs for the Compucolor II system.

The BASIC Editing package features six programs including FRED (Friendly Editor), RENUM (Renumber), MERGE, COMPAC, REMPAC (Deletes Remarks), and BASSRC (BASIC-to-Source Conversion). FRED, the most useful of the programs, allows the user to edit any line, move existing lines, delete a range of lines, and to search for the occurrence of any string, variable, or command within a program. The package comes on a floppy disk and costs $29.95.

Statistics is a series of three disks that is useful for engineering applications. The floppy disks are entitled *Statistics I, II,* and *III*. Each disk contains five programs including plot, stat, polreg (polynomial regression), index, and more. Common to all three packages is a file manager program that generates, maintains, and displays files for use by other programs. *Statistics I* sells for $24.95. *Statistics II* and *III* sell for $29.95 each.

Compucolor has also released Soundware. This program includes the software and hardware necessary to create sounds on the Compucolor II. It is written in BASIC, with a range of two to three octaves. The price is $49.95.

Circle 574 on inquiry card.

TLC-LISP for Z80 Systems

The LISP Company has announced its version of the LISP language for the Z80. TLC-LISP allows manipulation of functions as data objects; promotes object-oriented programming style; defines functions with a variable number of parameters; includes structured iteration and nonstructured escape mechanisms; contains complete string and character processing capabilities; and includes fixed- and floating-point arithmetic. The language system also contains a table-driven scanner; comprehensive error control, an autoload feature that "virtualizes" infrequently used functions and constants to disk files, freeing programmable memory; and execution speeds comparable to a KA-10 running MACLISP. Over 150 utility functions are provided. TLC-LISP is available for Z80 CP/M systems and other versions will be available soon. A detailed manual is $15, and the system on 5- or 8-inch floppy disks is $150. Write The LISP Co, POB 487, Redwood Estates CA 95044.

Circle 575 on inquiry card.

Software Catalog for TRS-80 Level II

National Software Marketing Inc, POB 6195, Hollywood FL 33021, has announced a free catalog of software for the TRS-80 Model II. The software described includes accounts receivable and payable, general ledger, payroll, inventory, rental mangagement, and a variety of financial and mathematical programs. These systems will operate on the 64 K-byte model with the built-in disk. The programs have list prices of $15 to $100.

Circle 576 on inquiry card.

A Gomoku Program

Five Stones Software, POB 1369, Station B, Ottawa, Ontario, K1P 5R4, CANADA, has released a Gomoku program for North Star Horizon disk-operating systems and CP/M-based systems. The program features a book of openings with 200 entries, the ability to take back moves, a 19 by 19 board, recent moves displayed along with the board, and the ability to customize to different screen sizes. The program requires a minimum of 32 K bytes of programmable memory and is available on 5-inch floppy disks for $29.95.

Circle 577 on inquiry card.

PLMX — A Language That Communicates with All 8- or 16-bit Microprocessors

PLMX is a universal high-level language for microprocessors. It can be used with all 8- or 16-bit microprocessors and was designed primarily for use in microcomputer product development systems and in real-time process-control applications. PLMX syntax is identical to PL/M, so the entire library of existing PL/M programs can be compiled under PLMX. PL/M programs may be used on microprocessors other than the 8080 through the PLMX compiler. PLMX is a true compiler, allowing fast compiling times —useful for real-time applications. It has been developed as a user-oriented language. There are no arbitrary formatting rules or line numbers. Comments may occur anywhere in the source text, except within reserved words, identifier names, and numbers. PLMX is priced at $1000, which includes an 8-inch compiler floppy disk and instruction manuals. To obtain additional information, write Systems Consultants Inc, Product Development Group, 4015 Hancock St, San Diego CA 92110.

Circle 578 on inquiry card.

What's New?

SOFTWARE

High-Speed Sort Utility for Ohio Scientific

BPSort is a high-speed, assembly language, sort/merge utility program for Ohio Scientific floppy and hard disk systems. It is capable of sorting 20 K bytes in ten seconds. Files can be an entire hard or floppy disk in length. BPSort handles fixed length records. Five keys can be specified for ascending and/or descending sequence. Sort parameters are established using a BASIC program. BPSort is OS-DMS compatible and is supplied as part of the BPS, an interactive data management system. It is sold in single-user licensed copies for $124. Earlier versions can be updated for $25. Order from BPS, 322 W 57th St, New York NY 10019.

Circle 579 on inquiry card.

Microsoft to Market muLISP and muMATH

Microsoft has become the distributor for muLISP-79 and muMATH-79, which were written by the Soft Warehouse of Honolulu, Hawaii. muLISP offers all of LISP's programming features, including 83 LISP functions, flexible program-control structures, and infinite precision integer arithmetic in any desired radix (2 to 36). The modular muMATH symbolic mathematics package is useful for scientific and engineering applications. The muMATH routines are written in muSIMP, which is included in the package. Both programs run with CP/M systems. The muLISP program costs $200 and the muMATH/muSIMP-79 program is priced at $250. Contact Microsoft, 10800 NE Eighth, Suite 819, Bellevue WA 98004.

Circle 581 on inquiry card.

Microsoft Announces TRS-80 Model II Software

Microsoft is selling TRSDOS-compatible versions of its COBOL and BASIC compilers for the TRS-80 Model II. Both compilers provide complete facilities for commercial or in-house software development, including Microsoft's macroassembler and linking loader. The COBOL-80 compiler is an ANSI-74 implementation of COBOL. The BASIC compiler produces object code that runs faster than interpreted BASIC programs. All Microsoft BASIC language features are supported. The BASIC compiler is also available in a version for the TRS-80 Model I. Microsoft is the author of Radio Shack's BASICs. The BASIC compiler is $395,and the COBOL-80 compiler is $750. Contact Microsoft, 10800 NE Eighth, Suite 819, Bellevue WA 98004.

Circle 580 on inquiry card.

Six Programs for TRS-80 Level II and Disk-Operating System

International Data Services has developed Microsketch III, a graphics program for the Level II with 16 K bytes of programmable memory for $7.95. Freakout is a keyboard-generated graphics and sound program for the Level II with 4 K bytes of programmable memory for $3.95. The number-base conversion program converts any base to any other base between 2 and 16. It is priced at $3.95. Three other programs are available for disk BASIC with 16 K bytes of programmable memory. BASIC to Electric Pencil file conversion, machine language to BASIC data statement conversion, and mail-list file uppercase to uppercase-and-lowercase conversion programs all cost $3.95. Contact IDS, 340 W 55th St, New York NY 10019.

Circle 582 on inquiry card.

RCA's BASIC I Compiler/Interpreter for COSMAC Development System

RCA's BASIC I Compiler/Interpreter CDP18S834 is a software package that can accelerate program development on the COSMAC DOS Development System CDP18S007. The package gives the user the option of developing and running programs in BASIC I or converting the programs to object code. The output of the compiler is assembled by the COSMAC macroassembler to produce the executable object code. Some of the features of the compiler/interpreter include: 70 characters per line, variable designation by a single capital letter, and fixed-point arithmetic. BASIC I functions include MOD, AND, OR, XOR, and USR. The USR function extends BASIC I by means of machine-language subroutines. Some of the statements available to the programmer are REM, LET, GOTO, IF, INPUT, WFLN, and NEW. With a manual, the package is priced at $300. Contact RCA Solid State Div, POB 3200, Somerville NJ 08876.

Circle 583 on inquiry card.

A Data Base System for the TRS-80

V R Data Corp, 777 Henderson Blvd, Folcroft PA 19032, has announced a Data Base system for the TRS-80 Models I and II. The Data Base system provides the capability to define and create customized records for various applications. Records may contain up to 25 user-defined variable-length fields and up to 250 characters per record. A dictionary of the fields and their characteristics is maintained by the system. Records may be added, deleted, and extended; field contents may be changed, and fields may be removed or added to the record or renamed at any time. Records may also be linked logically. The records may be sorted by any combination of fields in ascending or descending order. Reports are fully user-definable and may be routed to a printer or the video display. This four-program BASIC system requires 48 K bytes of programmable memory, a minimum of two disk drives and a line printer for the TRS-80 Model I, with 300 records per disk. Programs are available for the Model II with 950 records per disk.

Circle 584 on inquiry card.

Machine-Language Program for TRS-80 Disk Systems

The ST80-111 machine-language program is written for the TRS-80 Level II system. This package includes programs that allow users to talk to a time-sharing computer, transfer files to and from the central computer, and customize the ST80-111 system. Some of the programs included in the system are a BASIC program that creates translation tables, one that tells if a file is American Standard Code for Information Interchange (ASCII) or binary, a binary-to-ASCII conversion program, and one that changes machine-language programs to binary. The ST80-111 has been run on HP2000, IBM 370 and 360, PDP-11, Burroughs, Apple, and North Star systems. The minimum requirements for the system are the TRS-80 Level II with one disk drive and 16 K bytes of memory, an RS-232C board, and a modem. The package is produced by Small Business Systems Group, Main St and Lowell Rd, Dunstable MA 01827, and is priced at $150.

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***S100 CORE SALE:** Brand new, tested Ampex core. See article "IT'S TIME FOR CORE" (9/79 Kilobaud p. 34) which describes an easily built interface between this core and an S-100 machine. But ignore the prices in the article! Sale priced, including large documentation pkg. 8K boards $99 16K boards $230. Add $4 for schematics of core.

***OTHER SURPLUS BARGAINS:** HARD DISKS, new w/manual $895. SHUGART SA800-1/801 floppies w/manual, new $425. Full ASCII KEYBOARDS $44. TOUCHTONE DECODERS $68.

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AS SPECIALISTS IN VIDEO IMAGING ...we think we have the right monitor or modulator for your system. Our product line includes the popular "Micro-Verter" (OSI and Apple Inc. approved UHF color modulator), a variety of color and B-W monitors, color cameras, B-W cameras, Audio subcarrier kits and parts. FREE CATALOG UPON REQUEST. Dealers welcomed. Well established program with over 400 dealers.

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Apple II Or APPLE II PLUS

16K $975.95, Extra 16K E.S. RAM installed $74.95, extra 32K E.S. RAM installed $148.95.

APPLE II HOBBY/ PROTOTYPING CARD

Part No. 7907 $14.95

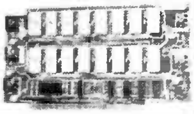
REAL TIME 100,000 DAY CLOCK

MT. HARDWARE Double the utility of your S-100 bus computer with a real-time clock that keeps time in 100μS increments for over 273 years. Program events for the entire period with real time interrupts...without derailing the system. Maintain a log of computer usage, time and date transaction printouts, call up lists...virtually any activity where time is a factor. On-board battery backup. MHPX004—$249.95

SUPER MODEM

Orignate, RS-232 and 20 mA compatable, Full duplex, and half duplex, direct connect or acoustic coupled, on board power supply, carrier detect light, DB25 plug. 300 BAUD, Type 103 compatable frequencies. Bare board Part No. 2000, $19.95, Kit Part No. 2000A, $99.95.

16K EPROM

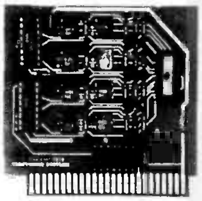


Uses 2708 EPROMS, memory speed selection provided, addressable anywhere in 65K of memory, can be shadowed in 4K increments. Board only $24.95 part no. 7902, with parts less EPROMs $49.95 part no. 7902A.

PET COMPUTER

With 16K & monitor - $795. Dual Disk Drive - $10 95

OPTO-ISOLATED PARALLEL INPUT BOARD FOR APPLE II

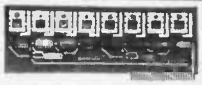


There are 8 inputs that can be driven from TTL logic or any 5 volt source. The circuit board can be plugged into any of the 8 sockets of your Apple II. It has a 16 pin socket for standard dip ribbon cable connection. Board only $15.00. Part No. 120, with parts $69.95. Part No. 120A.

VIDEO TERMINAL

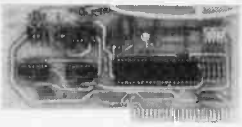
16 lines, 64 columns • Upper and lower case • 5x7 dot matrix • Serial RS-232 in and out with TTL parallel keyboard input • On board baud rate generator 75, 110, 150, 300, 600, & 1200 jumper selectable • Memory 1024 characters (7-21L02) • Video processor chip SFF96364 by Neculonic • Control characters (CR, LF, →, ←, ↑, ↓, non destructive cursor, CS, home, CL • White characters on black background or vice-versa • With the addition of a keyboard, video monitor or TV set with TV interface (part no. 107A) and power supply this is a complete stand alone terminal • also S-100 compatible • requires +16, & −16 VDC at 100mA, and 8VDC at 1A. Part No. 1000A $199.95 kit.

PARALLEL TRIAC OUTPUT BOARD FOR APPLE II



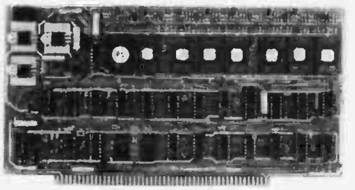
This board has 8 triacs capable of switching 110 volt 6 amp loads (660 watts per channel) or a total of 5280 watts. Board only $15.00 Part No. 210, with parts $119.95 Part No. 210A.

APPLE II SERIAL I/O INTERFACE



Baud rate is continuously adjustable from 0 to 30,000 • Plugs into any peripheral connector • Low current drain. RS-232 input and output • On board switch selectable 5 to 8 data bits, 1 or 2 stop bits, and parity or no parity either odd or even • Jumper selectable address • SOFTWARE • Input and Output routine from monitor or BASIC to teletype or other serial printer • Program for using an Apple II for a video or an intelligent terminal. Also can output in correspondence code to interface with some selectrics. • Also watches DTR • Board only $15.00 Part No. 2, with parts $42.00 Part No. 2A, assembled $62.00 Part No. 2C

8K EPROM PICEON



• Programs 2708's address relocation of each 4K of memory to any 4K boundary • Power on jump and reset jump option for "turnkey" systems and computers without a front panel • Program saver software in 1 2708 EPROM $25. Bare board $35 including custom coil, board with parts but no EPROMS $139, with 4 EPROMS $179, with 8 EPROMS $219.

WAMECO PRODUCTS

With ELECTRONIC SYSTEMS parts

FDC-1 FLOPPY CONTROLLER BOARD will drive shugart, pertek, remex 5" & 8" drives up to 8 drives, on board PROM with power boot up, will operate with CPM (not included). PCBD $42.95

FPB-1 Front Panel. (Finally) IMSAI size hex displays. Byte or instruction single step. PCBD $42.95

MEM-1A 8Kx8 fully buffered, S-100, uses 2102 type RAMS. PCBD .... $24.95, $168 Kit

QMB-12 MOTHER BOARD, 13 slot, terminated, S-100 board only .... $34.95 $89.95 Kit

CPU-1 8080A Processor board S-100 with 8 level vector interrupt PCBD .. $25.95 $69.95 Kit

RTC-1 Realtime clock board. Two independent interrupts. Software programmable. PCBD .... $25.95, $60.95 Kit

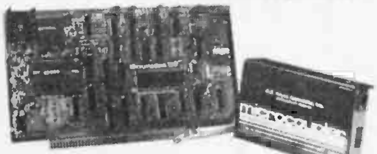
EPM-1 1702A 4K EPROM card PCBD .... $25.95 $49.95 with parts less EPROMS

EPM-2 2708/2716 16K/32K EPROM card PCBD .... $24.95 $49.95 with parts less EPROMS

QMB-9 MOTHER BOARD. Short Version of QMB-12. 9 Slots PCBD .... $30.95 $67.95 Kit

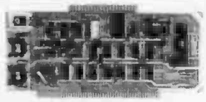
MEM-2 16Kx8 Fully Buffered 2114 Board PCBD .... $25.95, $269.95 Kit

D.C. HAYES MICROMODEM



Fully S-100 bus compatible including 16-bit machines and 4 MHz processors. • Two software selectable Baud rates—300 Baud and a jumper selectable speed from 45 to 300 Baud. (110 standard). Supports originate and answer modes. • Direct-connect Microcoupler. This FCC-registered device provides direct access into your local telephone system, with none of the losses or distortions associated with acoustic couplers and without a telephone company supplied data access arrangement. • Auto-Answer/Auto-Call. The MICROMODEM 100 can automatically answer the phone and receive input; it can also dial a number automatically. • Automatic Reset and Disconnect. • Software compatible with the D.C. Hayes Associates 80-103A Data Communications Adapter. Micromodem-DCHA32625—$379.95

TIDMA

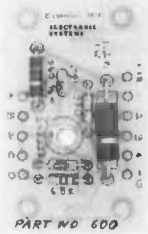


Tape Interface Direct Memory Access • Record and play programs without bootstrap loader (no prom) has FSK encoder/decoder for direct connections to low cost recorder at 1200 baud rate, and direct connections for inputs and outputs to a digital recorder at any baud rate • S-100 bus compatible • Board only $35.00 Part No. 112, with parts $110.00 Part No. 112A.

SYSTEM MONITOR

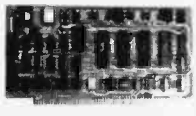
8080, 8085, or Z-80 System monitor for use with the TIDMA board. There is no need for the front panel. Complete with documentation $12.95.

RS-232/TTY INTERFACE



This board has two active circuits, one converts RS-232 to 20 mA, the other converts 20 mA to RS-232. Requires +12 and -12 volts. $9.95 Part No. 600A Kit.

SERIAL I/O



Four Serial I/O RS-232 ports. S-100 Bus. Software or jumper selectable baud rate (110, 300, 600, 1200, 2400, 4800, 9600, 19.2K), on board Xtal baud rate generator, Addressing, switch selectable. Parity or no parity (odd or even) switch selectable, 1 or 2 stop bits, 5 to 8 bits/character. Board only $29.95. Part No. 7908. With parts (kit) $199.95. Part No. 7908A.

S-100 BUS ACTIVE TERMINATOR

Board only $14.95 Part No. 900, with parts $24.95 Part No. 900A

To Order: Mention part no. description, and price. In USA shipping paid by us for orders accompanied by check or money order. We accept C.O.D. orders in the U.S. only, or a VISA or Master Charge no., expiration date, signature, phone no., shipping charges will be added. CA residents add 6.5% for tax. Outside USA add 10% for air mail postage and handling. Payment must be in U.S. dollars. Dealer inquiries invited. 24 hour order line (408) 448-0800

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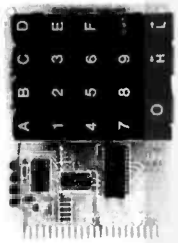
Circle 245 on inquiry card.

HEX ENCODED KEYBOARD



Four onboard LEDs indicate the HEX code generated for each key depression. The board requires a single +5 volt supply. Board only $15.00 Part No. HEX-3, with parts $49.95 Part No. HEX- 3A. 44 pin edge connector $4.00 Part No. 44P.

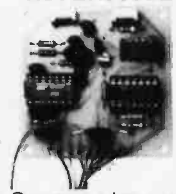
ASCII TO CORRESPONDENCE CODE CONVERTER

This bidirectional board is a direct replacement for the board inside the Trendata 1000 terminal. The on board connector provides RS-232 serial in and out. Sold only as an assembled and tested unit for $249.95. Part No. TA 1000C

T.V. INTERFACE

• Converts video to AM modulated RF, Channels 2 or 3. So powerful almost no tuning is required. On board regulated power supply makes this extremely stable. Rated very highly in Doctor Dobbs' Journal. Recommended by Apple • Power required is 12 volts AC C.T., or +5 volts DC • Board only $7.60 part No. 107, with parts $13.50 Part No. 107A

TAPE INTERFACE

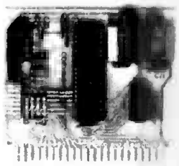


• Converts a low cost tape recorder to a digital recorder • Works up to 1200 baud • Digital in and out are TTL-serial • Output of board connects to mic. in of recorder • Earphone of recorder connects to input on board • No coils • Requires +5 volts, low power drain • Board only $7.60 Part No. 111, with parts $29.95 Part No. 111A

T.V. TYPEWRITER

• Stand alone TVT • 32 char/line, 16 lines, modifications for 64 char/line included • Parallel ASCII (TTL) input • Video output • 1K on board memory • Output for computer controlled curser • Auto scroll • Non-destructive curser • Curser inputs: up, down, left, right, home, EOL, EOS • Scroll up, down • Requires +5 volts at 1.5 amps, and -12 volts at 30 mA • All 7400, TTL chips • Char. gen. 2513 • Upper case only • Board only $39.00 Part No. 106, with parts $145.00 Part No. 106A

UART & BAUD RATE GENERATOR



• Converts serial to parallel and parallel to serial • Low cost on board baud rate generator • Baud rates: 110, 150, 300, 600, 1200, and 2400 • Low power drain +5 volts and -12 volts required • TTL compatible • All characters contain a start bit, 5 to 8 data bits, 1 or 2 stop bits, and either odd or even parity. • All connections go to a 44 pin gold plated edge connector • Board only $12.00 Part No. 101, with parts $35.00 Part No. 101A, 44 pin edge connector $4.00 Part No. 44P

ASCII KEYBOARD

53 Keys popular ASR-33 format • Rugged G-10 P. C. Board • Tri-mode MOS encoding • Two-Key Rollover • MOS/DTL/TTL Compatible • Upper Case lockout • Data and Strobe inversion option • Three User Definable Keys • Low contact bounce • Selectable Parity • Custom Keycaps • George Risk Model 753. Requires +5, -12 volts. $59.95 Kit.

ASCII KEYBOARD

TTL & DTL compatible • Full 67 key array • Full 128 character ASCII output • Positive logic with outputs resting low • Data Strobe • Five user-definable spare keys • Standard 22 pin dual card edge connector • Requires +5VDC, 325 mA. Assembled & Tested. Cherry Pro Part No. P70-05AB. $119.95.

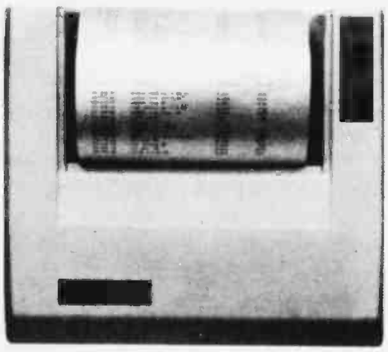
SOROC IQ 120

Upper/lower case display • Numeric keypad & cursor keys • Protected fields, ½ intensity display • RS 232 interface & aux. port. IQ120—$799.95 • IQ140 Detachable keyboard—$1199.95

MODEM

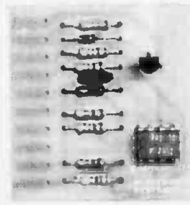
• Type 103 • Full or half duplex • Works up to 300 baud • Originate or Answer • Serial TTL input and output • connect 8 Ω speaker and crystal mic. directly to board • Requires +5 volts • Board only $7.60 Part No. 109, with parts $29.95 Part No. 109A.

COMPRINT PRINTER



Printing Characteristics: 225 characters/second (170 lines/minute) throughput • 9 horizontal x 12 vertical matrix • 96 ASCII character set with upper and true lower case • 80 characters/line • 5.8 lines/inch
Buffer Memory: standard 256 bytes; • optional; 2,048 bytes (buffer memory option designated as Model 912-2K), add $149.95.
Paper Requirements: electrosensitive type (aluminum coated) • 8-1/2 inch width • 3.7 inch max. (300 ft.) roll diameter.
Model 912-S Interfacing: serial interface RS232 and 20 mA current loop • BAUD rates 110, 150, 300, 600, 1200, 2400 and 4800 are strap selectable.
Model 912-P Interfacing: parallel interface, IEEE-488 and 8 bit parallel (strobe/ acknowledge). Model 912-S, Part No. CPIA, 32118, $579.95. Model 912-P, Part No. CPIA, 32117, $559.95.

RS-32/TTL INTERFACE



• Converts TTL to RS-232, and converts RS-232 to TTL • Two separate circuits • Requires -12 and +12 volts • All connections go to a 10 pin edge connector, kit $9.95 Part No. 232A 10 Pin edge connector $3.00 part No. 10P.

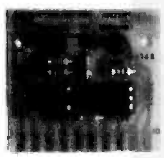
COMPUCOLOR II

With reg. keyboard
MOD3 8K $1595.95
MOD4 16K $1695.95
MOD5 32K $1995.95
Now includes $250 more, worth of software and accessories with 101 key option add $134.95 with 117 key option add $179.95

44 BUS MOTHER BOARD

Has provisions for ten 44 pin (.156) connectors, spaced 3/4 of an inch apart. Pin 20 is connected to X, and 22 is connected to Z for power and ground. All the other pins are connected in parallel. This board also has provisions for bypass capacitors. Board cost $15.00 Part No. 102. Connectors $3.00 each Part No. 44WP.

RS-232/20mA INTERFACE



This board has two passive, opto-isolated circuits. One converts RS-232 to 20mA, the other converts 20mA to RS-232. All connections go to a 10 pin edge connector. Requires +12 and -12 volts. Board only $9.95, part no. 7901, with parts $14.95 Part No. 7901A.

DC POWER SUPPLY

• Board supplies a regulated +5 volts at 3 amps., +12, -12, and -5 volts at 1 amp. • Power required is 8 volts AC at 3 amps., and 24 volts AC C.T. at 1.5 amps. • Board only $12.50 Part No. 6085, with parts excluding transformers $42.50 Part No. 6085A

To Order: Mention part no. description, and price. In USA shipping paid by us for orders accompanied by check or money order. We accept C.O.D. orders in the U. S. only, or a VISA or Master Charge no., expiration date, signature, phone no., shipping charges will be added. CA residents add 6.5% for tax. Outside USA add 10% for air mail postage and handling. Payment must be in U. S. dollars. Dealer inquiries invited. 24 hour order line (408) 448-0800

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Circle 246 on inquiry card.

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Will calls: 2322 Walsh Ave.
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Quest ELECTRONICS

NEW PRODUCTS!

Super Color S-100 Video Kit $99.95
Expandable to 256 x 192 high resolution color graphics. 6847 with all display modes computer controlled. Memory mapped. 1K RAM expandable to 6K. S-100 bus 1802, 8080, 8085, Z80 etc.

Gremlin Color Video Kit $59.95
32 x 16 alpha/numerics and graphics; up to 8 colors with 6847 chip; 1K RAM at E000. Plugs into Super Elf 44 pin bus. Not expandable to high resolution Graphics.

Elf II Adapter Kit $24.50
Plugs into Elf II providing Super Elf 44 and 50 pin bus plus S-100 bus expansion (With Super Expansion). High and low address displays, state and mode LED's optional $18.00.

1802 16K Dynamic RAM Kit $149.00
1802/S-100 expandable to 32K, Hidden refresh w/clocks up to 4 MHz w/no wait states Addl. 16K RAM **$79.00**.

Quest Super Basic
Quest, the leader in inexpensive 1802 systems announces another first. Quest is the first company worldwide to ship a full size Basic for 1802 systems. A complete function **Super Basic** by **Ron Cenker** including floating point capability with scientific notation (number range ± .17E38). 32 bit Integer ± 2 billion; Multi dim arrays; String arrays; String manipulation; Cassette I/O, Save and load, Basic, Data and machine language programs; and over 75 Statements, Functions and Operators.

Easily adaptable on most 1802 systems. Requires 12K RAM minimum for Basic and user programs. Cassette version in stock now. ROM versions coming soon with exchange privilege allowing some credit for cassette version.

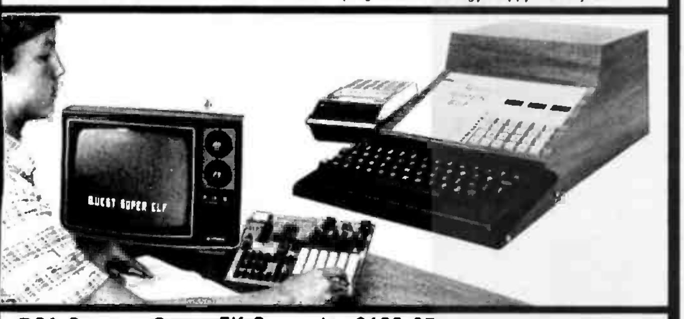
Super Basic on Cassette $40.00

Tom Pittman's 1802 Tiny Basic Source listing now available. Find out how Tom Pittman wrote Tiny Basic and how to get the most out of it. Never offered before. $19.00

S-100 4-Slot Expansion $ 9.95

Super Monitor VI.I Source Listing $15.00

Coming Soon: Assembler, Editor, Disassembler, DA/AD, Super Sound/Music, EPROM programmer, Stringy Floppy Disc System.



RCA Cosmac Super Elf Computer $106.95
Compare features before you decide to buy any other computer. There is no other computer on the market today that has all the desirable benefits of the Super Elf for so little money. The Super Elf is a small single board computer that does many **big** things. It is an excellent computer for training and for learning programming with its machine language and yet it is easily **expanded** with **additional memory, Full Basic, ASCII Keyboards, video character generation, etc.**

Before you buy another small computer, see if it includes the following features: ROM monitor; State and Mode displays; Single step; Optional address displays; Power Supply; Audio Amplifier and Speaker; Fully socketed for all IC's; Real cost of in warranty repairs; Full documentation.

The **Super Elf** includes a **ROM** monitor for program loading, editing and execution with **SINGLE STEP for program debugging** which is not included in others at the same price. With **SINGLE STEP** you can see the microprocessor chip operating with the **unique Quest** address and data bus displays **before, during and after** executing instructions. Also, CPU mode and instruction cycle are decoded and displayed on 8 LED indicators.

An RCA 1861 **video graphics** chip allows you to connect to your own TV with an inexpensive video modulator to do graphics and games. There is a **speaker system** included for writing your own music or using many music programs already written. The speaker amplifier may also be used to drive relays for control purposes.

A 24 key **HEX keyboard** includes 16 HEX keys plus **load, reset, run, wait, input, memory protect, monitor select and single step**. Large, on board displays provide output and optional **high and low address**. There is a 44 pin standard connector slot for PC cards and a 50 pin connector slot for the Quest Super Expansion Board. Power supply and sockets for **all** IC's are included in the price plus a detailed 127 pg. instruction manual which now includes over 40 pgs. of software info. including a series of lessons to help get you started and a music program and graphics target game. Many schools and universities are using the Super Elf as a course of study. OEM's use it for training and R&D.

Remember, other computers only offer Super Elf features at additional cost or not at all. **Compare before you buy. Super Elf Kit $106.95, High address option $8.95, Low address option $9.95. Custom Cabinet** with drilled and labelled plexiglass front panel **$24.95**. Expansion Cabinet with room for 4 S-100 boards **$41.00. NiCad Battery Memory Saver Kit $6.95.** All kits and options also completely assembled and tested.

Questdata, a 12 page monthly software publication for 1802 computer users is available by subscription for $12.00 per year. Issues 1-12 bound $16.50.

Tiny Basic Cassette **$10.00, on ROM $38.00,** original Elf kit board **$14.95. 1802 software;** Moews Video Graphics **$3.50.** Games and Music **$3.00,** Chip 8 Interpreter **$5.50.**

Super Expansion Board with Cassette Interface $89.95
This is truly an astounding value! This board has been designed to allow **you** to decide how you want it optioned. **The Super Expansion Board comes with 4K of low power RAM** fully addressable anywhere in 64K with built-in memory protect and a **cassette interface**. Provisions have been made for all other options on the same board and it fits neatly into the hardwood cabinet alongside the **Super Elf**. The board includes slots for up to 6K of **EPROM** (2708, 2758, 2716 or TI 2716) and is **fully socketed**. EPROM can be used for the monitor and Tiny Basic or other purposes.

A 1K Super ROM Monitor $19.95 is available as an on board option in 2708 EPROM which has been preprogrammed with a program loader/editor and error checking multi file cassette read/write software, (relocatible cassette file) another exclusive from Quest. It includes register save and readout, block move capability and video graphics driver with blinking cursor. Break points can be used with the register save feature to isolate program bugs quickly, then follow with single step. The Super Monitor is written with subroutines allowing users to take advantage of monitor functions simply by calling them up. Improvements and revisions are easily done with the monitor. If you have the **Super Expansion Board** and **Super Monitor** the monitor is up and running at the push of a button.

Other on board options include **Parallel Input and Output Ports with full handshake**. They allow easy connection of an ASCII keyboard to the input port. **RS 232 and 20 ma Current Loop** for teletype or other device are on board and if you need more memory there are two **S-100** slots for static RAM or video boards. Also a 1K Super Monitor version 2 with video driver for full capability display with Tiny Basic and a video interface board. **Parallel I/O Ports $9.85, RS 232 $4.50, TTY 20 ma I/F $1.95, S-100 $4.50. A 50 pin connector set** with ribbon cable is available at $15.25 for easy connection between the **Super Elf and the Super Expansion Board.**

Power Supply Kit for the complete system (see Multi-volt Power Supply below).

Same day shipment. First line parts only. Factory tested. Guaranteed money back. Quality IC's and other components at factory prices.

INTEGRATED CIRCUITS

7400TTL

7400N	.17
7402N	.18
7404N	19
7409N	23
7410N	18
7414N	70
7420N	18
7422N	39
7430N	.20
7442N	.50
7445N	69
7447N	.60
7448N	.69
7450N	.18
7474N	.35
7475N	.49
7485N	.88
7489N	1.85
7490N	.43
7492N	.43
7493N	.43
7495N	69
74100N	90
74107N	.35
74121N	34
74123N	59
74125N	.45
74145N	.69
74150N	.95
74151N	69
74154N	1 00
74157N	.69
74161N	.87
74162N	87
74163N	87
74174N	96
74175N	90
74190N	1 15
74192N	87
74193N	85
74221N	2 00
74298N	1 65
74365N	66
74366N	66
74367N	66

74LS00 TTL

74LS00N	35
74LS02N	35
74LS04N	35
74LS05N	35
74LS08N	35
74LS10N	.35
74LS13N	55
74LS14N	1 10
74LS20N	35
74LS22N	35
74LS28N	41
74LS30N	35
74LS33N	75
74LS38N	.55
74LS74N	1.25
74LS75N	1 00
74LS90N	85
74LS93N	70
74LS95N	1 10
74LS107N	.45
74LS112N	.45
74LS113N	35
74LS132N	89
74LS136N	45
74LS151N	85
74LS155N	.85
74LS157N	85
74LS162N	1.15
74LS163N	1 15
74LS174N	2 00
74LS190N	1 06
74LS221N	1 95
74LS258N	67
74LS367N	1.35

LINEAR

CA3045	90
CA3046	1 10
CA3081	1 80
CA3082	1 90
CA3089	2 95
LM301AN AH	35
LM305H	87
LM307N	35
LM308N	89
LM309K	1 50
LM311H/N	90
LM317T/K	3 75
LM318	1 35
LM320K-5	1 50
LM323K-5	5 95
LM320K-12	1 50
LM320K-15	1 50
LM320T-5	1 60
LM320T-8	1 60
LM320T-12	1 50
LM320T-15	1 60
LM324N	1 15
LM339N	1 55
LM340K-5	1 35
LM340K-8	1 35
LM340K-12	1 35
LM340K-15	1 35
LM340K-24	1 35
LM340T-5	1 25
LM340T-8	1 25
LM340T-12	1 25
LM340T-15	1 25
LM340T-18	1.25
LM340T-24	1.25
LM343H	4 50
LM350	7.50
LM370	1.15
LM377	3 00
LM379	5 00
LM380N	1.00
LM381	1 60
LM382	1.60
LM703H	40
LM709H	28
LM723H/N	.50
LM733N	67
LM741CH	35
LM741N	32
LM747H/N	75
LM748N	35
LM1303N	1 75
LM1304	1 10
LM1305	1 27
LM1307	2 00
LM1310	2 75
LM1458	47
LM1800	1.75
LM1812	7 50
LM1889	3.00
LM2111	1 75
LM2902	1 50
LM3900N	60
LM3905	1 75
LM3909N	89
MC1458V	.50
NE540H	3 75
NE550N	1 00
NE555V	39
NE556A	.85
NE565A	1.00
NE566V	1 50
NE567V	1.00
NE5708	5 00
78L05	60
78L08	60
78M05	85
75108	1 75
75491CN	50
75492CN	55
75494CN	.89

A to D CONVERTER

8038B	4.50
8700CJ	13.95
8701CN	22 00
8750CJ	13 95
LD130	9.95
9400CJV/F	7.40
ICL7103	9 50
ICL7107	14.25

CMOS

CD34001 Fair.	50
CD4000	.16
CD4001	.28
CD4002	.28
CD4006	1.10
CD4007	.28
CD4008	28
CD4009	45
CD4010	45
CD4011	28
CD4012	28
CD4013	39
CD4014	1 00
CD4015	1,00
CD4016	45
CD4017	1 05
CD4018	94
CD4019	.45
CD4020	1.02
CD4021	1 25
CD4022	1.10
CD4023	28
CD4024	75
CD4025	.28
CD4026	2.00
CD4027	66
CD4028	.85
CD4029	1.02
CD4030	45
CD4035	1.02
CD4040	1.02
CD4042	.85
CD4043	85
CD4044	.85
CD4046	1.67
CD4049	45
CD4050	49
CD4051	1 13
CD4060	1.42
CD4066	71
CD4068	.40
CD4069	.40
CD4070	50
CD4071	28
CD4072	28
CD4073	.28
CD4075	.28
CD4076	1 45
CD4078	.40
CD4081	.28
CD4082	.28
CD4116	.47
CD4490	5.50
CD4507	1 00
CD4508	4 25
CD4510	1 02
CD4511	94
CD4515	2 52
CD4516	1 10
CD4518	1 02
CD4520	1 02
CD4527	1.51
CD4528	79
CD4553	3 50
CD4566	2.25
CD4583	4 50
CD4585	1 10
CD40192	3.00
74C00	.28
74C04	40
74C10	28
74C14	2.10
74C20	.28
74C30	28
74C48	1 95
74C74	75
74C76	1 40
74C90	1 15
74C93	1 40
74C154	3.00
74C160	1 44
74C175	1 35
74C192	1 65
74C221	2 00
74C905	6 00
74C906	75
74C914	1 95
74C922	5.50
74C923	5.50
74C925	6 95
74C926	6 96
74C927	6 95

INTERFACE

8095	.65
8096	.65
8097	65
8098	65
8T09	1 25
8T10	4 50
8T13	3.00
8T20	5.50
8T23	3 10
8T24	3 50
8T25	3 20
8T26	1.69
8T28	2.75
8T97	1.69
8T98	1 69

MOS MEMORY

RAM

2101-1	3 95
2102-1	95
2102AL-4	1 25
2102AN-2L	1 60
21L02-1	1 18
2104A-4	4 95
2107B-6	3.75
2111-1	3 75
2112-2	3 95
2114L 300ns	7 40
4116 200ns	9 50
8/4116 200ns	64 00
2513B	6 30
MM5262	40
MM5280	3 00
MM5320	9 95
MM5330	5.94
PD411D-3	4 00
PD411D-4	5 00
P5101L	8 95
4200A	9 95
82S25	2 90
91L02A	1 50
HD0165-5	6 95
MM57100	4 50
GIAY38500 1	9.95
MCM6675IA	9 95
9368	3 50
4100	10 00
416	16 00

CLOCKS

MM5311	5 50
MM5312	3 90
MM5314	3 90
MM5369	2.10
MM5841	14 45
MM5865	7.95
CT7001	5.80
CT7010	8 95
CT7015	8 95
MM5375AA N	3 90
MM5375AG N	4 90
7205	16 50
7207	7 50
7208	15 95
7209	4 95
DS0026CN	3.75
DS0056CN	3 75
MM53104	2 50

MICROPROCESSOR

6502	12 50
6504	16 50
6522	13 60
6800	17 50
6802	18 75
6820	9 95
6850	12 95
8080A	8 95
8085	27 00
8086	75 00
Z80	14 75
Z80A	19 75
8212	2 90
8214	8 00
8216	2 90
8224	2.90
8228	5 35
8251	8 50
8253	15 00
8255	9 25
8257	19 50
8259	19 50
1802CP plas	13 95
1802DP plas	17 95
1861P	11 50
CDP1802CD	19 95
CDP1802D	25 00
CDP1861	12.95

UART/FIFO

AY5 1013	5 50
AY5-1014	7 50
3341	6 95

PROM

1702A	3.95
2513B upper case	6 95
2708	7 75
2716T1	24 50
2716 Intel	34 95
8/2716 Intel	240 00
2732	85 00
2758	22 50
8741A	85 00
8748	75 00
8748-8	70 00
8755A	65 00
N82S23	2 95
N82S123	3 50
N82S126	3 75
N82S129	3 75
N82S131	3.75
N82S136	8 75
N82S137	8 75
DM8577	2 90
8223	2.90
8/2716 Intel	240 00

CONNECTORS

30 pin edge	2 50
44 pin edge	2.75
100 pin edge	4.50
100 pin edge WW	5 25

IC SOCKETS

Solder Tin Low Profile

PIN	1 UP	PIN	1UP
8	15	22	.30
14	14	24	.35
16	16	28	.42
18	27	36	.58
20	29	40	.57

2 level 14 pin ww 20

WIRE WRAP LEVEL 3

PIN		PIN	
14	32	24	86
16	33	28	1 00
18	57	40	1 23

CRYSTALS

1 MHz	4 50
2 MHz	4 50
4 MHz	4 25
5 MHz	4 25
10 MHz	4 25
18 MHz	3 90
20 MHz	3 90
32 MHz	3 90
32768 Hz	4 00
1 8432 MHz	4 50
3 5795 MHz	1 20
2 0100 MHz	1 95
2 097152 MHz	4 50
2 4576 MHz	4 50
3 2768 MHz	4 50
5 0688 MHz	4 50
5 185 MHz	4 50
5 7143 MHz	4.50
6 5536 MHz	4 50
14 31818 MHz	4 25
18 432 MHz	4 50
22 1184 MHz	4 50

KEYBOARD ENCODERS

AY5-2376	$12.50
AY5-3600	17 95
AY5-9100	10 50
AY5-9200	16 50
74C922	5.50
74C923	5 50
HD0165-5	6 95

D Connectors RS232

DB25P	2 95
DB25S	3.95
Cover	1.50
RS232 Complete Set	6 50
DE9S	1.95
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Includes everything except case 2-PC boards 6-.50" LED Displays 5314 clock chip, transformer, all components and full instructions. Orange displays also avail. **Same kit w/.80" displays Red only $21.95 Case $11.75**

8K/16K Eprom Kit (less PROMS)	$89 00
Motherboard	$39 00
Extender Board	$8 99

RESISTORS ¼ watt 5%
10 per type .03 1000 per type .012
25 per type .025 350 piece pack
100 per type .015 5 per type 6.75
½ watt 5% per type .05

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56 key ASCII keyboard kit	$67 50
Fully assembled	77 50
53 key ASCII keyboard kit	60 00
Fully assembled	70 00
Enclosure	14 95
Metal Enclosure	29 95

LEDS

Red TO18	.15
Green, Yellow TO18	.20
Jumbo Red	20
Green, Orange, Yellow Jumbo	25
Cliplite LED Mounting Clips	8/$1 25

(specify red, amber, green, yellow, clear)

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Complete line of breadboard test equip.
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3 pos. slide	25
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Model 10 Trigger Expander Kit	$229 00
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Sinclair 3½ Digit Multimeter	$59.95
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TRANSFORMERS

6V 300 ma	3.25
12 Volt 300 ma transformer	1 25
12 6V CT 600 ma	3 75
12V 250 ma wall plug	2 95
12V CT 250 ma wall plug	3 50
24V CT 400 ma	3 95
10V 1 2 amp wall plug	4.85
17V 6 amp	12 95
12V 500 ma wall plug	4.75
12V 1 amp wall plug	6.50
12V 3 amp	8 50
10/15 VAC 8/16 VA wall plug	9.75

DISPLAY LEDS

MAN1	CA	270	2 90
MAN3	CC	125	39
MAN72/74	CA/CA	300	1.00
DL704	CC	300	1 25
DL707/DL707R	CA	300	1.00
DL727/728	CA/CC	500	1 90
DL747/750	CA/CC	600	1 95
DL750	CC	600	1 95
FND359	CC	357	.70
FND500/507	CC/CA	500	1 35
FND503/510	CC/CA	500	90
FND800/807	CC/CA	.800	2 20
3 digit Bubble			60
4 digit Bubble			80
DG8 Fluorescent			1 75
DG10 Fluorescent			1 75
5 digit 14 pin display			1 00
10 digit display			1 25
7520 Clairex photocells			39
TIL311 Hex			9 50
MAN3640	CC	.30	1 10
MAN4610	CA	40	1 20
MAN4640	CC	40	1 20
MAN4710	CA	40	95
MAN4740	CC	40	1 20
MAN6640	CC	56	2 95
MAN6710	CA	60	1.35
MAN6740	CC	60	1 35
MA1002A			8.95
MA1002E			8.95
MA1012A			8.95
102P3 transformer			2.25

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6502 based single board with full ASCII keyboard and 20 column thermal printer. 20 char. alphanumeric display. ROM monitor, fully expandable. $375.00. 4K version $450.00. 4K Assembler $85.00, 8K Basic Interpreter $100.00.

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8v 5 amp, ±18v .5 amp, 5v 1.5 amp, −5v .5 amp, 12v .5 amp, −12 option. ±5v, ±12v are regulated. Kit $29.95. Kit with punched frame $37.45. $4.00 shipping. Kit of hardware $14.00. Woodgrain case $10.00. $1.50 shipping.

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102 key, upper, lowercase, 10 Baud rates 24 x 80 char. microprocessor cont. edit. cap.

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Complete IC data selector, 2500 pg. master reference guide. Over 50,000 cross references. Free update service through 1979. Domestic postage $3.50. No foreign orders.

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8K Static RAM Kit	$135.00
16K Static RAM Kit	265.00
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16K Dynamic RAM Kit	199.00
32K Dynamic RAM Kit	310.00
64K Dynamic RAM Kit	470.00
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Indoor and outdoor. Switches back and forth. Beautiful. 50" LED readouts. Nothing like it available. Needs no additional parts for complete, full operation. Will measure −100° to +200°F, tenths of a degree, air or liquid. Beautiful woodgrain case w/bezel **$11.75**

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U-ART
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320T-12	.80
340T-5	.75
340T-12	.65
78405	5.00

MICROBYTE 16K STATIC RAM BOARD
- S-100 COMPATIBLE
- 4K BANK ADDRESSABLE
- EXTENDED MEMORY MANAGEMENT
- NO DMA RESTRICTIONS
- ASSEMBLED & TESTED
- 4MHZ OPERATION

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MICROBYTE 32K STATIC RAM BOARD
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- 4K bank addressable to any 4K slot within a 64K boundary
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14 PIN	.11	.10
16 PIN	.12	.11
18 PIN	.16	.14
20 PIN	.24	.22
24 PIN	.31	.29
28 PIN	.35	.31
40 PIN	.42	.39

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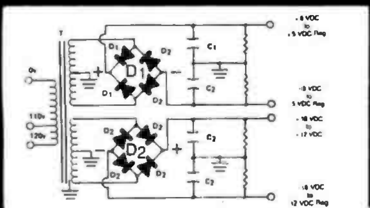

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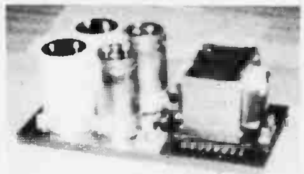

POWER TRANSFORMERS (WITH MOUNTING BRACKETS)

ITEM NO.	USED IN KIT NO.	PRI. WINDING TAPS	SECONDARY WINDING OUTPUTS 2×8 Vac	2×14 Vac	2×24 Vac	SIZE W×D×H	UNIT PRICE
T_1	1	0V, 110V, 120V	2×7.5A	2×2.5A	—	3¾"×3⅝"×3⅛"	21.95
T_2	2	0V, 110V, 120V	2×12.5A	2×3.5A	—	3¾"×4⅜"×3⅛"	27.95
T_3	3	0V, 110V, 120V	2×9A	2×2.5A	2×2.5A	3¾"×4⅜"×3⅛"	29.95
T_4	4	0V, 110V, 120V	2×4A	—	2×3A	3¾"×3⅝"×3⅛"	21.95

POWER SUPPLY KITS (OPEN FRAME WITH BASE PLATE, 3 HRS. ASSY. TIME)

ITEM	USED FOR	@+8 Vdc	@−8 Vdc	@+16 Vdc	@−16 Vdc	@+28 Vdc	SIZE W×D×H	UNIT PRICE
KIT 1	15 CARDS SOURCE	15A	—	2.5A	2.5A	—	12"×6"×4⅞"	51.95
KIT 2	SYSTEM SOURCE	25A	—	3A	3A	—	12"×6"×4⅞"	58.95
KIT 3	DISC SYSTEM	15A	1A	2A	2A	4A	14"×6"×4⅞"	66.95
KIT 4	DISC SOURCE	8A	1A	—	—	5A	10"×6"×4⅞"	49.95

EACH KIT INCLUDES: TRANSFORMER, CAPACITORS, RESIS., BRIDGE RECTIFIERS, FUSE & HOLDER, TERMINAL BLOCK, BASE PLATE, MOUNTING PARTS AND INSTRUCTIONS.

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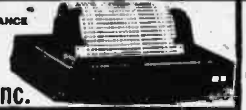

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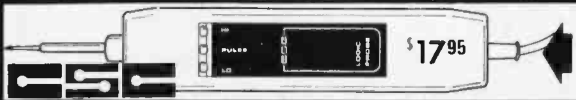

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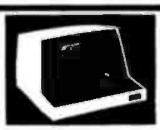

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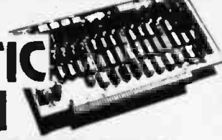

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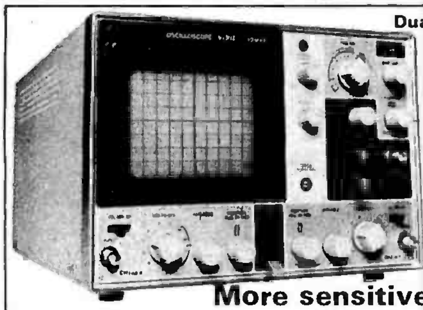

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ED209Y	yellow	4 for $1

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SD Systems KITS

27001	ExpandoRAM Kit - Expandable RAM Board Kit (No RAMs)	$220
27002	Versafloppy Flexible Disk Drive Controller Kit	250
27003	SBC-100 Single Board Computer Kit	295
27004	Z80 Starter Kit	340
27007	ExpandoPROM Kit	175
27010	Add-on RAM (16K Devices) 4116 (250nsec)(package of eight devices	165
27011	VDB-8024 Video Display Board Kit	370
27012	ExpandoRAM II Expandable RAM Board Kit (16K RAM)	460
27013	Versafloppy II Flexible Disk Drive Controller Kit	350
27014	PROM-100 PROM Programmer Board Kit	200
27015	MPB-100 Z80 Central Processing Unit Board Kit	250
27017	Add-on RAM (16K devices) 4116 (200nsec)	250
27018	SBC-200 Single Board Computer Kit	320
27024	ExpandoRAM II Expandable RAM Board Kit (No RAMs)	230

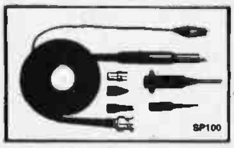
SD Systems ASSEMBLED

38001	ExpandoRAM (16K of on-board RAM)	$ 480
38002	ExpandoRAM (32K of on-board RAM)	620
38003	ExpandoRAM (48K of on-board RAM)	760
38004	ExpandoRAM (64K of on-board RAM)	900
38005	Versafloppy Flexible Disk Drive Controller	335
38006	SBC-100 Single Board Computer	350
38007	Z80 Starter System	450
38010	ExpandoPROM	245
38011	Cable for 8" Disk Drives	80
38013	VDB-8024 Video Display Board	470
38016	Cable, 8ft., 26 Pin Edge Connector (one end)	50
38017	Cable for SD-100/SD-200 Interface to Texas Instruments 810 Printer	80
38018	Cable, same as above (Internal)	120
38019	Cable, same as above (External)	80
38020	ExpandoRAM II (16K Population)	610
38021	ExpandoRAM II (32K Population)	840
38022	ExpandoRAM II (48K Population)	1070
38023	ExpandoRAM II (64K Population)	1300
38024	Versafloppy II Double Density Flexible Disk Drive Controller	430
38025	PROM-100 PROM Programmer	265
38026	MPB-100 Z80 Microprocessor Board	325
38028	SBC-200 Single Board Computer	400

NEW HICKOK LX 304 DIGITAL MULTIMETER

Compact Accurate Dependable $89.95

Universal Oscilloscope Probe



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SWITCHABLE X1 and X10 ATTENUATION FACTOR

KEY ADDITIONAL FEATURES: ● 100 MHz bandwidth ● Heavy duty tip ● Break resistant center conductor ● Slender, flexible cable ● 6 ft. length ● Wide compensation range ● Fits all scopes ● Ground reference can be activated at tip ● Includes SPRUNG HOOK, I.C. TIP, BNC ADAPTOR, INSULATING TIP and TRIMMER TOOL accessories

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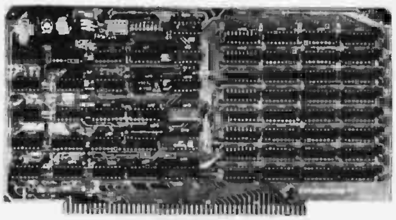
SD EXPANDORAM

The EXPANDORAM is available in versions from 16K up to 64K, so for a minimum investment you can have a memory system that will grow with your needs. This is a dynamic memory with the invisible on-board refresh, and IT WORKS!

- Bank Selectable
- Phantom
- Power 8VDC, +16VDC, 5 Watts
- Lowest Cost Per Bit
- Uses Major Brand 16K RAMS
- PC Board is doubled solder masked and has silk-screened parts layout
- Extensive documentation clearly written



- Complete kit includes all Sockets for 64K
- Memory access time: 375ns, Cycle time: 500ns.
- No wait states required
- 16K boundaries and Protection, via Dip Switches
- Designed to work with Z-80, 8080, 8085 CPU's

EXPANDORAM 64K Kit (16K Ram)

16K	$239.95
32K	309.95
48K	379.95
64K	449.95

SD'S PROM 100 PROM Programmer Board

The PROM-100 Programmer is a development tool for S-100 Bus computer systems. The Zero Insertion Force Programming Socket extends above the card cage height for easy access to PROM devices. Software verifies PROM erasure, verifies program loading and provides for reading of object file from Disk or PROM and programming into PROM/EPROM. Features include: On-board generated 25vdc Programming pulse, TTL compatible, maximum programming time for 16,389 bits is 100 seconds. Programs: 2708, Intel 2758, 2716, 2732 and TI 2516. DIP Selectable EPROM type.

PROM-100 Board Kit $149.95

SD'S SBC-200 SINGLE BOARD COMPUTER Kit $289.95

S-100 Bus compatible and based on the powerful Z80 microprocessor, the SBC-200 meets the needs of a Z-80 CPU board with many additional features. Ideal for Industrial and control applications. All of the same features that have made the SBC-100 famous, PLUS 4MHz OPERATION. • S-100 Bus Compatible • Z80 Central Processing Unit • 1024 Bytes of Random Access Memory • 8K Bytes of PROM using 2716 • Serial Input/Output Port (with Asynchronous and Synchronous Operation) • Parallel Input and Output Ports • Four Channel Counter/Timer (Z80-CTC) • Software Programmable Baud Rate Generator • No-Front Panel Required for Operation • 4 MHz Operation.

SD'S VERSAFLOPPY II

• IBM 3740 Compatible Soft Sectored Format for Single Density Drives • Operates with Single and Dual Sided Drives. Single or Double Density Drives and 5" & 8" Drives — in any combination of four simultaneously • Drive Select and Side Select Circuitry • S-100 Bus Compatible • Vectored Interrupt Operation Optional • Phase Locked Loop Data Recovery Circuit • Operates with Z80 CPU's • Uses FD1791-1 Controller Chip • Ther Versafloppy II incorporates all the possible features of a flexible disk drive controller into one board. Capable of handling four drives simultaneously, combinations of any variety are possible. such as 5" single sided, 8" dual density dual sided, 5" dual density single sided. Most popular drives are controlled directly with the Versafloppy II. The operating system for the Versafloppy II is the extremely powerful SDOS available for SD Systems. Diagnostic and control software available to complete your disk system.

KIT $335.95

SD'S VDB-8024 VIDEO DISPLAY BOARD

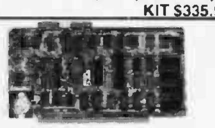
The VDB-8024 features its own on-board Z80 microprocessor. This gives the capability of using software (included in ROM) to control functions and enhancements without interference with the computer's CPU. Included in the special features: 80 characters by 24 lines display, keyboard power and interface, composite and separate video output, 2K on-board RAM, a total of 256 available characters, full cursor control, forward and reverse scrolling, underlining, field reverse, field protect enhancements, programmable characters.

KIT $329.95 A&T $389.95

SD'S "VERSAFLOPPY I" KIT

FEATURES: IBM 3740 soft sectored compatible, S-100 BNS Compatible for Z-80 or 8080. Controls up to 4 drives (single or double sided). Directly controls the following drives: Sugart SA400/450 Mini Floppy • Shugart SA800/850 Standard Floppy • PERSCI 70 and 277 • MFE 700/750 • CDC.9404/9406

$189.95



SD'S SBC-100 SINGLE BOARD COMPUTER

The SBC-100 provides a complete micro-computer on a single board! The Z80 microprocessor is used as the heart of the SBC-100. The SBC-100 meets all the requirements of a Z80 CPU board with the added features of I/O ports, counter/timer channels, on board RAM, provisions for PROM/ROM and a software programmable baud rate generator. S-100 Bus compatible, the SBC-100 features are: 8K bytes of available PROM, 1024 bytes on-board RAM, Serial I/O with both synchronous and asynchronous operation, Parallel I/O ports, Operational Vectored Interrupts, and Four Counter/Timer Channels. SD Monitor available for RS-232 and Video Terminals. Disk based system software also available.

SBC-100 KIT $249.95

TARBELL FLOPPY DISK INTERFACE

Compatible with Z80 & 8080. S-100 Bus. Uses CPM operating system. Plugs directly into your IMSAI or ALTAIR • Fastest transfer rate

KIT $190.00 Assembled & Tested $260.00

TARBELL CASSETTE INTERFACE

Plugs directly into your IMSAI or ALTAIR • Fastest transfer rate • Extremely reliable • Phase encoded • 4 extra status & control lines

KIT $99.95

SSM CB2 Z-80 CPU Board Kit $186.00

Operates at 2 MHZ or 4 MHZ by DIP switch selection and includes two sockets for 2716 or 2732 EPROMs or TMS 4016 2K RAMs. Jumper options generate the new IEEE S-100 signals.

SSM VB3 80 Character Video Board Kit $299.95

• 80 char. per line, up to 51 lines • Graphics up to 160 × 204 matrix • Up to 256 user defined symbols (optional EPROM) • Composite video

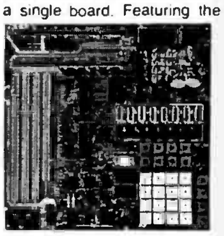
PB1 2708/2716 Programmer & 4K/8K EPROMBoard Kit SSM $124.00

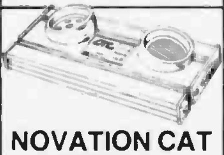
• S-100 bus • 2 separate programming sockets for 2708 or 2716 (5V) EPROMs • Programming voltage generated on board — no need for an external power supply • Software control of 2708/2716 programming selection • LEO indicator for programming mode and an on-off switch for programming voltage • 4 sockets for 4K of 2708 or 8K of 2716 EPROMs • Unused EPROM sockets do not enable data bus drive so the board is never committed to the full 4K or 8K of memory • Jumper selectable wait states (0-4) for fast or slow EPROMS

Z80 STARTER KIT

Kit: $279.95 Assembled & Tested $349.95

SD System's Z80 Starter Kit enables the novice to build a complete microcomputer on a single board. Featuring the powerful Z80 microprocessor, the Z80 Starter Kit features • Keyboard and Display • Audio Interface • PROM Programmer • Expansion and Wire Wrap Area • On Board RAM • 4 Channel Counter/Timer • Z-BUG Monitor in PROM • I/O Ports.





NOVATION CAT ACOUSTIC COUPLER/MODEM

$189.00

Let your computer communicate with other computers. Bell Systems 103 compatible 300 baud, answer or originate.

SYM-1

Reg. $269.00
NOW $219.00

- KIM-1 Compatible
- 4K ROM Monitor
- 1K Bytes 2114 RAM
- 65K Memory Expansion
- User EPROM 2716

IO4 2 Parallel/2 Serial I/O Board Kit $126.00

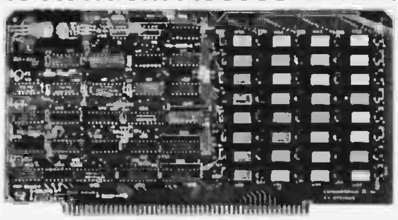
• S-100 bus • 2 serial I/O ports (2 in & 2 out) • Independent baud-rate selection from 55 to 9600 baud • Regulated +5V, +12V & −12V outputs provided on both serial headers • 2 latched parallel I/O ports (2 In & 2 out) • Independent DIP switches for setting address • Interrupt capability provided for on serial and parallel I/O ports • +8V @ 0.95A, +16V @ 0.6A, & −16V @ 80mA typical SSM

VB1B VIDEO BOARD KIT $124.00

• S-100 bus • 64 or 32 characters per line (DIP switch selectable), 16 lines • Graphics 128×48 matrix • Upper case, lower case, Greek characters, symbols and numbers • 7×9 dot character matrix • Black-on-white or white-on-black • Timing 60Hz vertical rate, 16.2KHz horizontal rate, Crystal 12.44MHz • Parallel and composite video output (US TV signals), separate video, horizontal and vertical sync SSM

SD'S EXPANDORAM II
The Randem Access Memory

- S-100 Bus Compatible
- Up to 4Mhz Operation
- Expandable Memory from 16K to 256K
- DIP Switch Selectable Boundaries
- Uses 16K (4116) or 64K (4164) Memory Devices
- Page Mode Operation Allows up to 8 Memory Boards on Bus
- Operates with Z80 CPU's
- Phantom Output Disable
- Invisible Refresh (Synchronized with Wait States)



SD Systems' ExpandoRAM II is a dynamic RAM board with capacities from 16K bytes (4116) to 256K bytes (4164). It operates on the industry S-100 Bus. The design allows 8 boards to operate from the same S-100 Bus. The ExpandoRAM II is compatible with most S-100 CPU's based on the Z80 microprocessor.

EXPANDORAM II KIT

16K	$295.95
32K	369.95
48K	444.95
64K	519.95

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FOR THE 80's.

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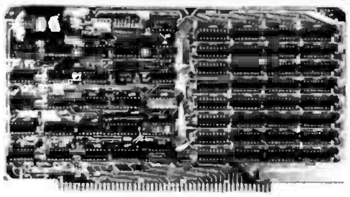

EXPANDORAM
Expandable to 64K Using 4116 RAMS

Interfaces with most popular S-100 boards
Bank selectable; PHANTOM provision
Draws only 5 watts fully populated
Designed to work with Z-80, 8080, and 8085 systems
No wait states required
16K boundaries & protect via dip switches
Kits come with sockets for full 64K
Invisible refresh

MEM-64133K 64 K KIT	$399.95
MEM-64133A A&T	$449.95
MEM-48132K 48K KIT	$334.95
MEM-48132A A&T	$384.95
MEM-32131K 32K KIT	$269.95
MEM-32131A 32K A&T	$319.95
MEM-16130K 16K KIT	$204.95
MEM-16130A 16K A&T	$259.95

Sale Price $475.00

32K STATIC RAM
Expandable 8K/32K, 2/4MHz, KIT/A&T

Switchable 2 or 4 MHz

THE JADE BIG Z
Z-80A CPU with Serial I/O Port

This CPU can accomodate a 2708, 2716, or 2732 EPROM in SHADOW mode, allowing you to use a full 64K of RAM. The MWRITE signal is generated automatically if you use the board without a front panel. There's also an independent on-board USART to control the RS232 serial port at baud rates from 75 to 19,200.

We've sold thousands of these high quality S-100 CPU boards at $159.95; but now, in a brief fit of financial insanity, we're offering them to you for only $135.00! **Don't pass this one up!**

CPU-30201K (KIT)	$135.00
CPU-30201A (A&T)	$199.00
CPU-30200B (BARE BOARD)	$35.00

S D Systems

EXPANDORAM II
4 MHz RAM Board Expandable to 256K

S-100 bus compatible, up to 4 MHz operation
Expandable memory from 16K to 256K
Dip switch selectable boundaries
Page-mode allows up to 8 boards on the same bus
Invisible refresh; PHANTOM output disable
Designed to operate in Z-80 based systems

MEM-64633K 64K KIT	$509.95
MEM-64633A 64K A&T	$559.95
MEM-48632K 48K KIT	$439.95
MEM-48632A 48K A&T	$489.95
MEM-32630K 32K KIT	$359.95
MEM-32630A 32K A&T	$409.95
MEM-16630K 16K KIT	$279.95
MEM-16630A 16K A&T	$329.95

Solid State Music

PB-1
EPROM Programmer for 2708 or 2716

MEM-99510K (KIT)	$125.00
MEM-99510A (A&T)	$175.00

JADE DOUBLE-D
Double Density Disk Controller

Read/write single or double density, 8" or 5¼" drives
On board Z-80 insures reliable operation
CP/M compatible in either single or double density
Density is software selectable
Up to 4 single or double sided, single or double density drives may be mixed on the same system
EIA level serial printer interface on board-up to 9600 baud (perfect for despooling operations)
All the hard work of disk access is done by the on board Z-80A and 2K memory, leaving your host CPU free for its normal duties
Uses IBM standard formats for proven reliability
THIS BOARD REALLY WORKS!!!!!!

IOD-1200K (DOUBLE-D KIT)	$285.00
IOD-1200A (DOUBLE-D A&T)	$349.00
IOD-1200D (MANUAL ONLY)	$15.00

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ADDS REGENT
Our Finest Line of Terminals

REGENT 20 $795.00
24 lines X 80 characters, EIA and 20ma current loop interfaces, 110 to 9600 baud, 96 ASCII codes plus 32 control codes, both upper and lower case, 8 X 8 dot matrix, reverse video, auxiliary EIA serial interface, and addressable cursor.

REGENT 25 $850.00
All the features of the Regent 20 plus an 18 key numeric and cursor control pad.

REGENT 40 $1195.00
All the features of the Regent 20 plus a 14 key numeric pad, 8 function keys, 5 cursor control keys, auxiliary port control key, reverse video, underline, blinking, plus full, half, and zero intensities, 8 X 8 dot matrix, 11 special line drawing symbols, reverse scrolling, and send/receive capability using the Regent 40's bi-directional interface.

REGENT 60 $1495.00
All the features of the Regent 40 plus Print Local, Editing, and Transmission Mode keys, business graphics, bar charts, histograms, and graphics, ability to insert or delete characters or lines, buffered mode reduces software needs, and can transmit data at baud rates other than rate received.

Special Package Price

RS-232 SET-$6.50
1 Male DB-25, 1 Female DB-25, 1 Cover

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Magnificent Magnetic Media™

5¼" single sided, single density, box of 10

MMD-5110103 (SOFT SECTOR)	$29.95
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MMD-5111603 (16 SECTOR)	$29.95

5¼" double sided, double density, box of 10

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MMD-8120103 (SOFT SECTOR)	$55.95

8" double sided, double density, box of 10

MMD-8220103 (SOFT SECTOR)	$57.95

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VERSAFLOPPY
Versatile Floppy Disk Controller

IBM 3740 soft sectored format
S-100 Z-80 or 8080 compatible
Controls up to 4 single or double sided drives
Compatible with all popular disk drives
CP/M compatible
Listings for control software included

IOD-1150K (KIT)	$239.00
IOD-1150A (A&T)	$289.00

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Z-80 STARTER
Complete Z-80 Microcomputer

On-board keyboard, display, EPROM programmer, cassette interface and S-100 interface
Wire-wrap area and room for 2 S-100 connectors
Two 8-bit parallel I/O ports, 4 channel CTC,
5 programmable breakpoints
Examine & change memory, I/O ports, or register

CPS-30010K (KIT)	$239.95
CPS-30010A (A&T)	$299.95

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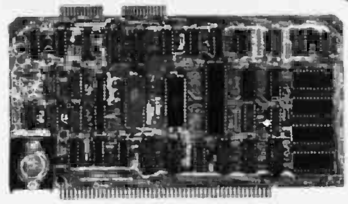

S D Systems

SBC-100/200
2 or 4 MHz Single Board Computer

S-100 bus compatible Z-80 CPU
1K of on-board RAM
4 EPROM sockets accomodate 2708, 2716, or 2732
One parallel and one serial I/O port
4-channel counter timer chip (Z-80 CTC)
Software programmable serial baud rates

CPC-30100K (2 MHz KIT)	$239.95
CPC-30100A (2 MHz A&T)	$289.95
CPC-30200K (4 MHz KIT)	$259.95
CPC-30200A (4 MHz A&T)	$309.95

Coming Soon

NEW JADE P/S I/O
Parallel Serial Interrupt Board

Z-80 SIO, PIO, 2 CTCs, expands to 2 SIOs, 4 CTCs
4 serial ports (async, sync, bisync, SDLC/HDLC)
2 parallel ports with full handshake
Software baud rate generators, interval timers, counters, and generates 32 vectored interrupts
Designed especially for MP/M multi-user multi-tasking operating systems. For use with Z-80 only

IOI-1045B (BARE BOARD)	$55.00
IOI-1045K (KIT)	$169.95
IOI-1045A (A&T)	$224.95

Solid State Music

I/O-4
2 Serial & 2 Parallel I/O Ports

IOI-1010K (KIT)	$149.95
IOI-1010A (A&T)	$199.95

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VERSAFLOPPY II

Double Density Disk Controller

Single or double density floppy disk controller
985600 bytes on 8" double sided diskettes
259840 bytes on double sided 5¼" diskettes
S-100 bus (IEEE) standard compatible
IBM 3740 format in single density
8" and 5¼" drives controlled simultaneously
Operates with Z-80, 8080, and 8085 CPU's
Controls up to 4 drives
Vectored interrupt operation optional

100-1160K KIT	**$299.95**
100-1160A A&T	**$349.95**

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ATARI 800

Don't Miss Out on Our Special Sale Price

At last there is a machine designed to give serious competition to Apple and Radio Shack. This computer contains many advanced technical features such as: built in RF modulator for use with a standard TV; 8K of internal RAM (expandable to 48K), 8K BASIC language included; extremely sharp high-resolution color graphics; and built-in peripheral I/O ports. Software is available in plug-in paks and cassette tapes, with many programs available in the areas of entertainment, education, and business/home management.

Available accessories include a printer, disk drives, game controller paddles, and memory expansion cartridges.

And JADE has the Atari 800 in stock at a special introductory price.

ATARI 800	**$825.00**
810 DISK DRIVE	**$575.00**
820 PRINTER	**$550.00**
16K RAM EXPANSION KIT	**$169.95**
CX30-04 PADDLE CONTROLLER	**$19.95**
CX40-04 JOYSTICK CONTROLLER	**$19.95**
ATARI 400	**$599.95**

We Think It's Superior

SDOS

A New Disk Operating System

SDOS is a disk operating system which will run any program that runs under CP/M*. It is designed specifically for use with the SBC-100/Versafloppy (I or II) board set by S.D. Systems. SDOS actually has more functions than CP/M, including file attributes, disk label, and read/write logical blocks. It provides additional protection features and is expandable to a multi-user realtime system. And if all that doesn't impress you, SDOS also contains S.D.'s ASSEMBLER/EDITOR/LINKER package and CBASIC 2!

SFX-55001002M (5¼" W/MAN)	**$150.00**
SFX-55001006F (8" W/MAN)	**$150.00**
SFX-55001000D (MANUAL ONLY)	**$ 15.00**

*CP/M is a trademark of Digital Research

Textool

ZIP* DIP II SOCKETS

16 PIN ZIP* DIP II	**$5.50**
24 PIN ZIP* DIP II	**$7.50**
40 PIN ZIP* DIP II	**10.25**

*** ZERO INSERTION PRESSURE**

COST FIGHTERS

RAMS	
21L02 (2 MHz)	$1.25
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4116 (250ns)	$8.95
4116 (200ns)	$9.50
4127 (70ns)	$39.95
4164 (64K x 1)	$175.00
5257 (2 MHz)	$6.75
5257 (4 MHz)	$7.25
BAUD RATE GENERATORS	
MC14411	$10.00
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8214	$4.65
8216	$2.95
8224	$3.25
8226	$3.85
8228	$4.95
8238	$4.95
8243	$8.00
8250	$14.95
8251	$6.50
8253	$13.95
8255	$6.50
8257	$19.95
8259	$17.95
8275	$49.95
8279	$8.95
3881	$12.95
3882	$12.95
3883	$45.00

6800 SUPPORT	
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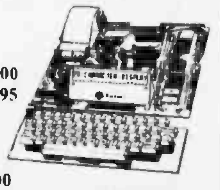
6828P	$11.95
6834P	$12.95
6840P	$18.75
6850P	$4.80
6852P	$5.79
6875L	$7.40
68488P	$25.00
PROMS	
2708 (450ns)	$8.95
2716 (450ns)	$34.95
2716 (5v)	$34.95
2732 (5v)	$95.00
2758 (5v)	$34.95
MICROPROCESSORS	
Z-80	$10.95
Z-80A	$12.50
6502	$11.50
6800	$11.95
6802	$17.95
6809	$39.95
8035	$24.00
8035-8	$24.00
8080A	$6.59
8085	$15.95
TMS9900JL	$39.95
UARTS	
AY5-1013A	$5.25
AY3-1014A	$8.25
TR1602B	$5.25
TMS6011	$5.95
IM6403	$9.00

Special Package Price

ROCKWELL AIM-65

The Head-Start in Microcomputers



KIM-1 compatible
On-board printer
Full ACSII keyboard

AIM-65 w/1K RAM	**$395.00**
AIM-65 w/4K RAM	**$439.95**
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POWER SUPPLY	**$59.95**
CASE for AIM-65	**$49.95**
4K Assembler/Editor	**$85.00**

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TRS-80 APPLE EXIDY

Everything you need to add 16K of memory to your computer. Your kit comes neatly packaged with easy to follow instructions. In just minutes your computer is ready to tackle more advanced software.

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CP/M 2.0

Digital Research has done it again! This new release of their industry standard disk operating system is bound to be an even bigger hit than the original version. All of the fundamental file-size restrictions of release 1 have been eliminated, while maintaining full compatability with the earlier versions. This new release can be field-configured by the user for a single mini-disk up through a multiple drive hard-disk system with 128 megabyte capacity. Field configuration can be accomplished easily through use of the Macro Library (DISKDEF) provided with CP/M 2.0.

A powerful operating system for only $150.00

Jade's New Motherboards

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BARE BOARD	**$24.95**
KIT	**$49.95**
ASSEMBLED & TESTED	**$59.95**

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KIT	**$89.95**
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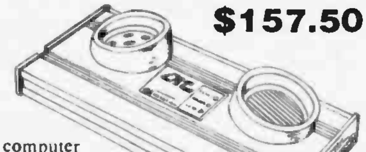

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Circle 297 on inquiry card.

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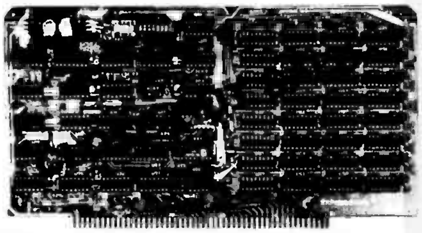
Look to QT for the BIG +

S D SYSTEMS

EXPANDORAM ST

EXPANDABLE TO 64K USING 4116 RAMS



Interfaces with most popular S-100 boards
Bank selectable; PHANTOM provision
Draws only 5 watts fully populated
Designed to work with Z-80, 8080, and 8085 systems
No wait states required
16K boundaries & protect via dip switches
Kits come with sockets for full 64K
Invisible refresh

MEM-16K (16K KIT)	$239.95
MEM-16AT (16K A&T)	$289.95
MEM-32K (32K KIT)	$309.95
MEM-32AT (32K A&T)	$359.95
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MEM-64K (64K KIT)	$449.95
MEM-64AT (64K A&T)	$499.95

SPECIAL

NOVATION CAT

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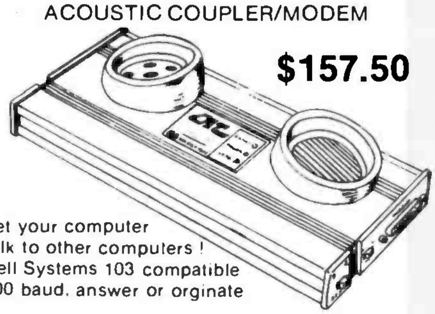

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EPROMS

1702A	$ 4.95
2708	$ 6.75
2516	$24.00
2716 (TI)	$24.00
2716 (5 VOLT)	$24.00
2758	$27.00
2532	$70.00
2732	$70.00

NEW DISK OPERATING SYSTEM

SDOS

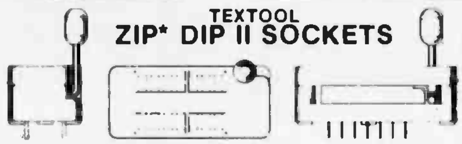
SDOS is a CP/M compatible operating system designed for the S D Sales Versafloppy I or II. It requires the SBC-100/Versafloppy board set and functions as a superset of CP/M giving 19 additional functions including the attributes, disk label and read/write logical blocks. It provides additional protection features and is expandable to a multi-user real time system. **$200.00**

TI PRINTERS

TI810 PARALLEL	$1895.00
TI810 SERIAL	$1695.00

TEXTOOL

ZIP* DIP II SOCKETS



16 PIN ZIP* DIP II	$5.50
24 PIN ZIP* DIP II	$7.50
40 PIN ZIP* DIP II	10.25

* ZERO INSERTION PRESSURE

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A powerful operating system for only ... $150.00

5¼" DISK DRIVES

MPI B-51	$295.00
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QT DISKETTES

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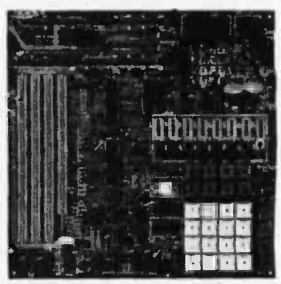
S D SYSTEMS

Z-80 STARTER KIT

COMPLETE Z-80 MICROCOMPUTER



On-board keyboard, display, EPROM programmer, and cassette interface
On-board S-100 interface
Wire-wrap area and room for 2 S-100 connectors
Two 8-bit parallel I/O ports, 4-channel CTC, 5 programmable breakpoints
Examine and change memory, I/O ports, or register

Z-80K (KIT)	$279.95
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S D SYSTEMS

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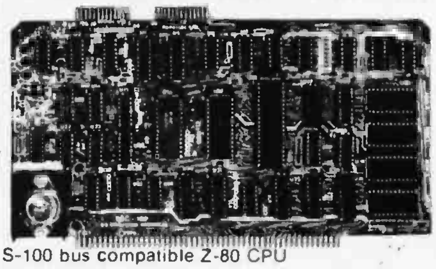
OR 4 MHz SINGLE BOARD COMPUTER



S-100 bus compatible Z-80 CPU
1K of on-board RAM
4 EPROM sockets accomodates 2708, 2716, or 2732
One parallel and one serial I/O port
4-channel counter timer chip (Z-80 CTC)
Software programmable serial baud rates

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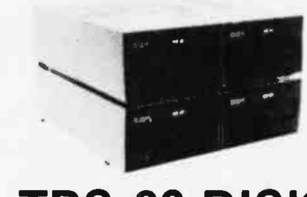
SBC-100AT (2 MHz A&T)	$299.95
SBC-200K (4 MHz KIT)	$289.95
SBC-200AT (4 MHz A&T)	$339.95



TRS-80 DISK DRIVE (CABLES INCLUDED)

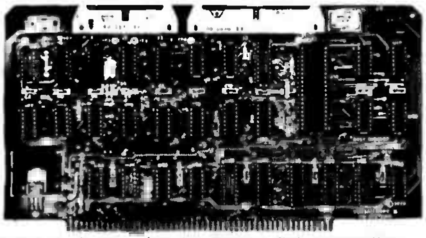
TRS-80 I (5¼")	$395.00
TRS-80 II (8")	$1095.00
APPLE II	$1550.00

DISK DRIVE SYSTEMS

S-100

MS-800-1 (Drive with cables & power supply)	$1095.00
MS-800-2 (2 Drives with cables & power supply)	$1595.00

S D SYSTEMS
VERSAFLOPPY II
DOUBLE DENSITY DISK CONTROLLER



Single or double density floppy disk controller
985600 bytes on 8" double sided diskettes
259840 bytes on double sided 5¼" diskettes
S-100 bus (IEEE) standard compatible
IBM 3740 format in single density
8" and 5¼" drives controlled simultaneously
Operates with Z-80, 8080, and 8085 CPU's
Controls up to 4 drives
Vectored interrupt operation optional

VF-2K (KIT)	**$335.95**
VF-2AT (A&T)	**$385.95**

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Assembled and Tested	$155.00
MICRO-MODEM II	$350.00
WIZARD CONTROLLER for 8" Disk Drive	$360.00
SORRENTO CONTROLLER for 8" Apple Disk Drive	$360.00
INTROL X-10 SYSTEM (turns appliances on/off)	$275.00
MICRO-MUSIC (Software)	$180.00
AIO/Serial-Parallel Board Kit	$115.00
AIO/Serial-Parallel Board A&T	$155.00
INTEGER Firmware Card	$179.00
PARALLEL INTERFACE CARD	$90.00
VISICALC(Business Software Package)	$124.95
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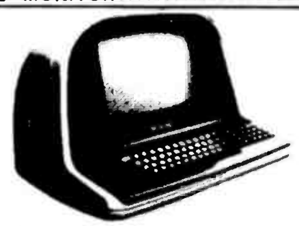
ROM WRITER (Epromburner) Mountain Hardware (order)	$175.00
PROGRAMMER AID #1	$50.00
APPLE CLOCK	$280.00
SANYO 15" MONITOR	$295.00



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- Protected fields
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- 12x10 character res.
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- Numeric pad
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- Self-test
- Auxiliary port

SALE PRICE $895.00
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4116-200 ns

Expansion Kit	$60.00 ea.
100 pcs	$5.95 ea.
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Z80A (4 MHz)	$12.95
6502	$11.25
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6802	$19.50
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8216	$ 2.95
8224	$ 4.00
8238	$ 6.00
8243	$ 5.00
8251	$ 7.00
8253	$19.00
8255	$ 6.25
8257	$17.95
8259	$19.95
8275	$69.95
8279	$17.50
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64 ea.	$1.20 ea.
100 ea.	$1.10 ea.
1,000 ea.	$.95 ea.
2102-1	$1.35
2114L (450 ns)	$5.25 ea.
100 ea.	$4.75 ea.
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100 ea.	$4.50 ea.

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2513 Lower (5 v)	$10.95
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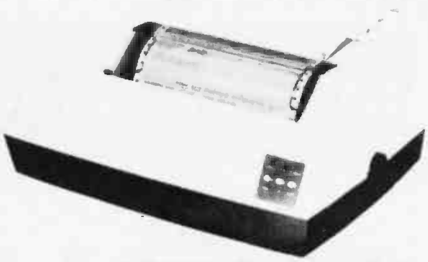

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VB1B Memory Mapped Video Interface	$26.95
VB2 I/O Mapped Video Interface	$29.95
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OB1 Vector Jump & Prototyping Board	$29.95
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SB1 Music Synthesizer Manual	$10.00
All Other Manuals	$ 5.00
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100 Pin edge connector (standard ww)	$ 4.00
Card Guides	$ .15

S-100 KITS & ASSEMBLED BOARDS

CB1A 8080 CPU	
Kit	$129.95
Assembled & Tested	$189.95
CB2 Z-80 CPU	
Kit	$185.95
Assembled & Tested	$250.00
VB1B Memory Mapped Video Interface	
Kit	$125.00
Assembled & Tested	$180.00
VB2 I/O Mapped Video Interface	
Kit	$150.00
Assembled & Tested	$195.00
VB3 80 Character Video Interface	
80x24 Display, 2 MHz	
Kit	$299.95
Assembled & Tested	$389.95
80x24 Display, 4 MHz	
Kit	$324.95
Assembled & Tested	$410.00
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4 MHz	$ 89.00
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Kit	$ 59.00
Assembled & Tested	$ 89.00
IO4 2P + 2S I/O Interface	
Kit	$126.00
Assembled & Tested	$199.95
SB1 Music Synthesizer (4)	
Kit	$199.00
Assembled & Tested	$279.00
OB1 Vector Jump & Prototyping Board	
Kit	$ 55.00
Assembled & Tested	$ 85.00
MB6B 8K Static RAM	
450 ns RAM	
Kit	$129.95
Assembled & Tested	$149.95
250 ns RAM	
Kit	$159.95
Assembled & Tested	$224.95
MB7 Low Power 16K Static RAM	
Kit	$269.96
Assembled & Tested	$375.00
PB1 2708/2716 EPROM Programmer	
Kit with Textool sockets	$129.95
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MB3 4K 1702 EPROM Board	
Kit - without EPROMs	$ 65.00
Assembled & Tested	$125.00
MB8A 16K 2708 EPROM Board	
Kit - without EPROMs	
Assembled & Tested	
T1 Active Terminator	
Kit	$ 34.00
Assembled & Tested	$ 64.00
MT1 15 Slot Motherboard	
Kit (with Connectors)	$129.95
Assembled & Tested	$149.95
XB1 Extender Board	
Kit (with Connector)	$ 19.95
Assembled & Tested	$ 29.95

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SUPER SAVER. Thanks to Commodore their printer prices have been drastically reduced:
Commodore Printer (tractor feed) ....
was $995 **NOW $795**
Commodore Printer (friction feed) ....
was $849 **NOW $695**

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TNW Bi-Dir.RS-232 printer S-face $229.00
KIM 1 (A Single Board Computer from Commodore) $179.00
PET TO IEEE Cable $39.95
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KIM1 & Power Supply Package Special .. $200.00

We have a complete inventory of Apple computers, peripherals, & software In-Stock for immediate delivery —

$200 in FREE accessories with the purchase of a 48K Apple II reg. or Apple II plus.
16K Apple reg. or plus — $1,195 ($100 in *free* acces.)
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48K Apple reg. or plus — $1,495 ($200 in *free* acces.)

Apple Accessories
PASCAL $495
Micromodem $379
VisiCalc $150
The Controller (Business Package) .... SALE! $550
The Cashier (POS System) .... SALE! $200
Integer BASIC ROM Card $200
Centronics Printer Interface $225
Disk and Controller $595
Parallel Printer Card $180
Communications Card $225
Hi-Speed Serial Card $195
Firmware Card $200
NEW! AppleWriter Text Editor $75

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- Answer Originate • Bell 108
- 300 Baud • Low Profile Design

Looks good, works great! **$179.00**

NEW FROM EXIDY THE SORCERER II 48K COMPUTER

Z-80 Microprocessor. Full-sized keyboard • ROM PAC Programs • Microsoft BASIC • Powerful Graphics • Serial and Parallel I/O • Dual Cassette I/O Memory Internally Expandable • S-100 Expansion Options.
48K Sorcerer II **$1,395**

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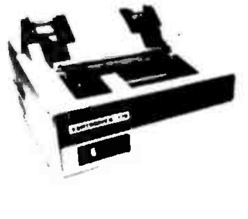

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The Paper Tiger Printer From Integral Data

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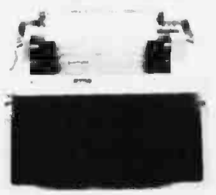

Standard features include: 4 character 8.3 to 16.5 cpi • 56 cps at 10 char. per in. • Selectable line spacing • 8 switch-selectable form sizes.

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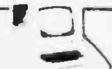

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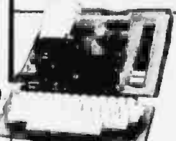

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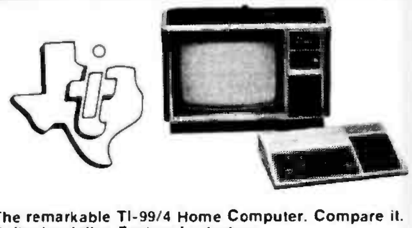

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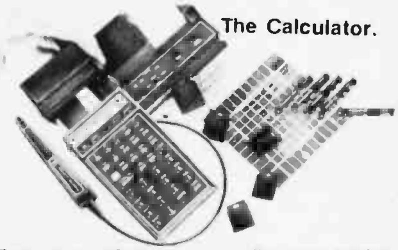

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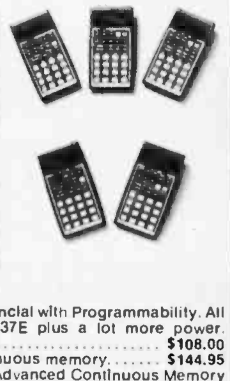

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74LS09	.42
74LS10	.35
74LS11	.75
74LS13	.59
74LS14	1.25
74LS15	.35
74LS20	.35
74LS21	.35
74LS22	.35
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74LS40	.35
74LS42	1.05
74LS47	1.05

74LS51	.29
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74LS73	.54
74LS74	.54
74LS75	.71
74LS76	.54
74LS78	.49
74LS83	1.05
74LS85	1.50
74LS86	.54
74LS90	.71
74LS92	.90
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74LS95	.99
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74LS107	.54
74LS109	.54
74LS112	.54
74LS123	1.50
74LS125	1.05
74LS132	.99
74LS136	.59
74LS138	1.05

74LS139	1.05
74LS151	1.05
74LS155	1.05
74LS157	1.05
74LS160	1.15
74LS161	1.39
74LS162	1.25
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74LS190	1.39
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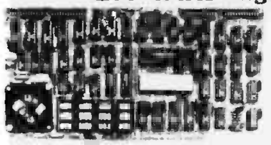
incorporated

Z80-4MHz Single Card Computer



Cromemco's Single Card Computer is a complete computer which brings the power of the Z-80 and the flexibility of the S-100 bus to the dedicated computer environment.

The card offers 4 MHz operation, 8K bytes of on-board 2716 PROM, and 1K byte of static RAM memory. This stand-alone card also provides an RS-232 (or 20mA current loop) serial interface with programmable baud rates to 76,800, vectored interrupts, 24 bits of bidirectional parallel I/O, and 5 programmable timers. Only a power supply and PROM software are required for operation. The Single Card Computer is assembled and tested (Model SCC-W) for $450. The Monitor and Control BASIC are available in two ROM's (Model MCB-216) for $90.

SCC-W (Assembled) **$450.00**

Processor: 4MHz Z-80
Instruction Set: 158 instructions incl. the 78 instructions of the 8080
ROM Capacity: 8K Bytes located from address 0000 to 1FFF
ROM Type: Intel 2716 PROM or equivalent
RAM Capacity: 1K Bytes located from address 2000 to 23FF
RAM Type: 4045, Static

Serial I/O Ports:
I/O Levels: RS-232 or 20mA current loop
Baud Rates: 110 to 76,800 (software selectable)
Parallel Ports:
Input Port: 24 bits bidirectional
Output Port: 24 bits bidirectional
Input Load: One TTL equivalent
Output Drive: 20 TTL loads
Interval Timers:
Number of timers: 5

Timer range: 0-16.32 milliseconds (software set.)
Timer resolution: 64 microseconds
Vectored Interrupts:
No. of restart locations (Z-80 mode): 65,536
General Information:
UART type: 5501 Bus: S-100
Power requirements: +8V at 1.4A; +18V at 70mA; −18V at 25mA
Operating environment: 0-55°C

DISCRETE LEDS

XC556R	.200"	red	5/$1
XC556G	.200"	green	4/$1
XC556Y	.200"	yellow	4/$1
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XC22Y	.200"	yellow	4/$1
MV10B	.170"	red	4/$1
MV50	.085"	red	6/$1
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XC209G	.125"	green	4/$1
XC209Y	.125"	yellow	4/$1
XC526R	.185"	red	5/$1
XC526G	.185"	green	4/$1
XC526Y	.185"	yellow	4/$1
XC526C	.185"	clear	4/$1
XC111R	.190"	red	5/$1
XC111G	.190"	green	4/$1
XC111Y	.190"	yellow	4/$1
XC111C	.190"	clear	4/$1

INFRA-RED LED ¼"x¼"x1/16" flat 5/$1

DISPLAY LEDS

TYPE	POLARITY	HT	PRICE
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MAN 2	5 x 7 Dot Matrix-red	.300	4.95
MAN 3	Common Cathode-red	.125	.25
MAN 4	Common Cathode-red	.187	1.95
MAN 7G	Common Anode-green	.300	1.25
MAN 7Y	Common Anode-yellow	.300	.99
MAN 72	Common Anode-red	.300	.75
MAN 74	Common Cathode-red	.300	1.25
MAN 82	Common Anode-yellow	.300	.49
MAN 84	Common Cathode-yellow	.300	.99
MAN 3620	Common Anode-orange	.300	.49
MAN 3630	Common Anode-orange ± 1	.300	.99
MAN 3640	Common Cathode-orange	.300	.99
MAN 4610	Common Anode-orange	.400	.99
MAN 4640	Common Cathode-orange	.400	.99
MAN 4710	Common Anode-red	.400	.99
MAN 4730	Common Anode-red ± 1	.400	.99
MAN 4740	Common Cathode-red	.400	.99
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MAN 4840	Common Cathode-yellow	.400	.99
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MAN 6630	Common Anode-orange ± 1	.560	.99
MAN 6640	Common Cathode-orange-D.D.	.560	.99
MAN 6650	Common Cathode-orange ± 1	.560	.99
MAN 6660	Common Anode-orange	.560	.99
MAN 6680	Common Cathode-orange	.560	.99
MAN 6710	Common Anode-red-D.D.	.560	.99
MAN 6730	Common Anode-red ± 1	.560	.99
MAN 6740	Common Cathode-red-D.D.	.560	.99
MAN 6750	Common Cathode-red ± 1	.560	.99
MAN 6760	Common Anode-red	.560	.99
MAN 6780	Common Cathode-red	.560	.99
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DL707	Common Anode-red	.300	.99
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DL746	Common Anode-red ± 1	.630	1.49
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DL749	Common Cathode-red ± 1	.630	1.49
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FND70	Common Cathode	.250	.69
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FND359	Common Cathode	.357	.75
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CA3059N	3.25
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CA3081N	2.00
CA3082N	2.00
CA3083N	1.60
CA3086N	.85
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14 pin LP	.20	.19	.18
16 pin LP	.22	.21	.20
18 pin LP	.29	.28	.27
20 pin LP	.34	.32	.30
22 pin LP	.37	.36	.35
24 pin LP	.38	.37	.36
28 pin LP	.45	.44	.43
36 pin LP	.60	.59	.58
40 pin LP	.63	.62	.61

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	1-24	25-49	50-100
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14 pin SG	.49	.45	.41
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18 pin WW	.99	.90	.81
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1N754	6.8	400m	4/1.00
1N757	9.0	400m	4/1.00
1N759	12.0	400m	4/1.00
1N959	8.2	400m	4/1.00
1N965	15	400m	4/1.00
1N5232	5.6	500m	28
1N5234	6.2	500m	28
1N5235	6.8	500m	28
1N5236	7.5	500m	28
1N5242	12	500m	28
1N5245	15	500m	28
1N456	25	40m	6/1.00
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1N3600	50	200m	6/1.00
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47 pf	.05	.04	.03	.01µF	.05	.04	.035
100 pf	.05	.04	.03	.022µF	.06	.05	.04
220 pf	.05	.04	.03	.047µF	.06	.05	.04
470 pf	.05	.04	.035	.1µF	.12	.09	.075

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.33/35V	.39	.31	.25	4.7/25V	.63	.51	.41
.47/35V	.39	.31	.25	6.8/25V	.79	.63	.50
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3.3/50V	.14	.12	.09	1.0/16V	.15	.13	.10
4.7/25V	.15	.13	.10	1.0/25V	.16	.14	.11
10/25V	.15	.13	.10	1.0/50V	.16	.14	.11
10/50V	.16	.14	.12	4.7/16V	.15	.13	.10
22/25V	.17	.15	.12	4.7/25V	.15	.13	.10
22/50V	.24	.20	.18	4.7/50V	.16	.14	.11
47/25V	.19	.17	.15	10/16V	.14	.12	.09
47/50V	.25	.21	.19	10/25V	.15	.13	.10
100/25V	.24	.20	.18	10/50V	.16	.14	.12
100/50V	.35	.30	.28	47/50V	.24	.21	.19
220/25V	.32	.28	.25	100/16V	.19	.15	.14
220/50V	.45	.41	.38	100/25V	.24	.20	.18
470/25V	.33	.29	.27	100/50V	.35	.30	.28
1000/16V	.55	.50	.45	220/16V	.23	.17	.16
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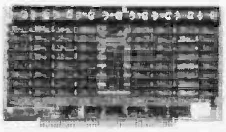

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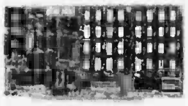

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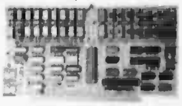

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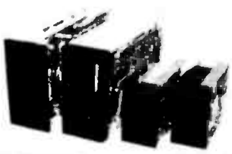

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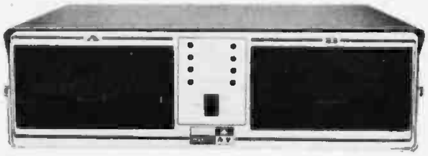

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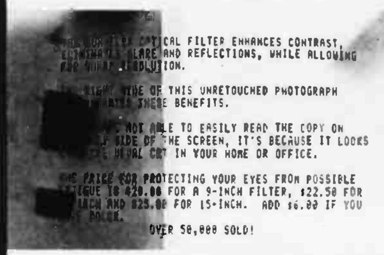

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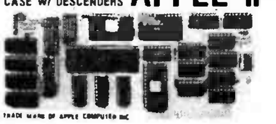

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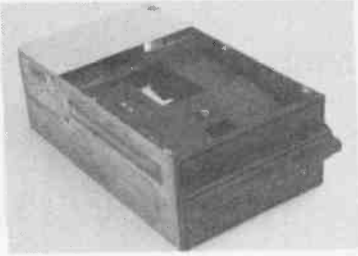

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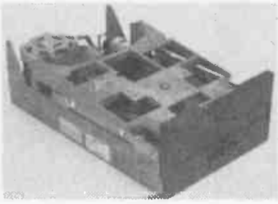

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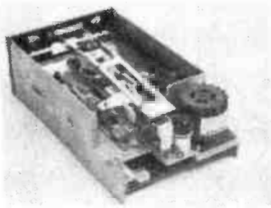

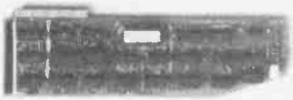

The following 5¼" mini-floppies share most features with their 8" cousins, so without further ado. . .

Siemens FDD 100-5D	$279
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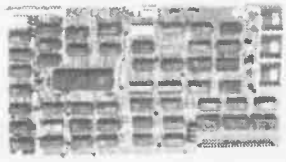
Qume Datatrak 5 (double sided)	$399
BASF Mini mini	$279
SA 400	$299



All the above mini-floppies are fully SA400 compatible.

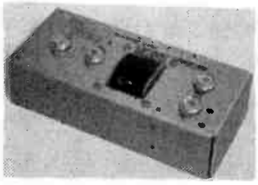
Manuals for all drives are $10, refundable against future purchase of drives.
Also, all 8" drives can be ordered with 220 v/50 hz for worldwide use.
Moving on to the realm of floppy disk controllers . . . although we still feel that single density is more reliable, there are many excellent double density disk controllers available, so choose your weapons carefully,

Tarbell floppy disk controller, A & T	$325
Tarbell floppy disk controller, A & T	$225
Tarbell double density, DMA A & T	$425
Tarbell double density, DMA, kit	$325
Delta Products double density disk controller Operate at 2 or 4MHZ, with 8 or 5" drives	$399
Micromation doubler w/programmable UART RS-232 port	$495
Sorrento Valley single density for Apple	$399

Again, purchase price of manuals ($5) is applicable towards future purchase price.

Subtract 15% OFF any Controller with Purchase of 2 Drives.

Disk Accessories

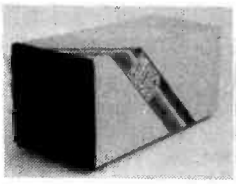


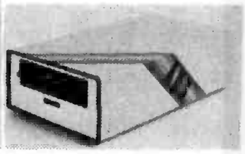
Cable kits for 8" drives with 10'50 cond. flat cable, power cable, & all connectors. Assembled if desired. ONe drive 27.50, two 33.95, three 38.95 for mini floppies (34 cond): one 24.95, two, 29.95

CP-206 Power-one power supply. Powers two drives more than adequately, top quality. 2.8A/24V, 2.5A/5V, .5A/-5V. $99.

Electrolabs
POB 6721, Stanford, CA 94305
415-321-5601 800-227-8266
Telex: 345567 (Electrolab Pla)
Visa MC Am. Exp.

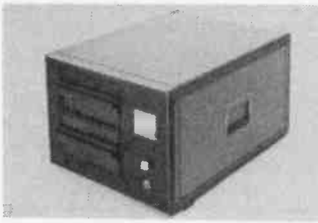
ENCLOSURES, SLEEVES





Double disk drive enclosure.
Enclosure alone $139.
Including power supply & fan $199.

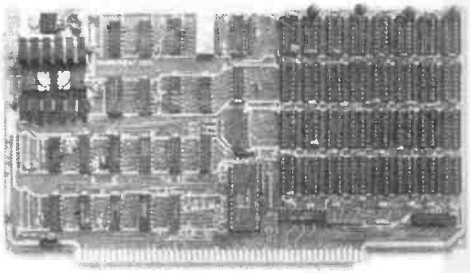
Single disk drive enclosure. Fits all 8" disk drives, please specify make & model No. of drive to assure proper mounting hole positions. Nonmar paint available in blue, beige, silver, & off-while.
Enclosure alone $60
Including power supply & fan $109.



Rackmount Mainframe MT-200. This gorgeous beast is so appealing that it can easily function also as stand-alone mainframe. Very modern styling with fully actively terminated S-100 bus.
Enclosure alone $399.
With power supply & fan $499.
With 15 slot S-100 bus $699.
With two 8" single-sided disk drives $1,699.
With two 8" double sided disk drives in place of single-sided variety $2,299.

Media

8". . $39.95/10 single-sided/single density
8"... $55.00 single sided/double density
8". . $55.00 double sided/single density
8". . $60.00 double sided
8". . specify hard or soft
5 ¼". . $34.95 single sided
5 ¼". . $60.00 double sided
Verbatism, Memorex, Scotch,or equivalent name brand
Diskette head cleaning kid for 5¼" or 8" – $28.75 includes everything for 1 drive for 1 year
Alignment Diskette $39
For Floppy Drives



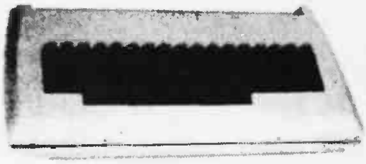
EXTRA SPECIAL !!

Imsai 65K dynamic RAM III

We made a special purchase of this now unavailable board, which were always noted for their fine performance & quality. We have a limited quanity on hand, get your orders in rapidly. These come assembled and tested, with burned-in 200 Ns RAM. Kit 299

A & T **$399.**

Keyboard Special

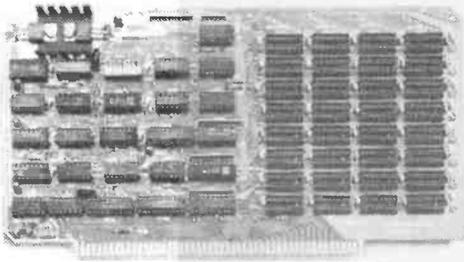


CHERRY "PRO" Keyboard $119.00
Streamlined Custom Enclosure $34.95
BOTH ONLY $134.95!!!

SD Systems Expandoram II Dynamic RAM

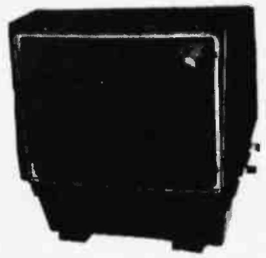
Operates at 4 Mhz, expandable memory from 16K to 256 K, allows up to 8 boards on the same bus, Z-80 based, and invisble refresh, among other things.

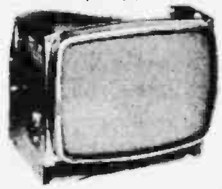
16K kit	$295.
16K A & T	$349.
32 K kit	$369.
32 K A & T	$419.
48K Kit	$440.
48K A & T	$490.
64K kit	$510.
64K A & T	$560.



Data Display Monitors

Used 12" Sylvania monitors. Composite Video, 15 MHz, 120VAC. Rebuilt with NEW P39 anti-glare tube $89.00
New P4, $89.00, used P4 $69.00
U-fix model, 10/$300.00





"OEM STYLE" as above, will fit any case, (Both versions serviced by qualified tech). Identical to above but subtract $12.00

Televideo 912c $760.

Upper/lower case
Adjustable baud rate — 80 X 24
Editing capabilities — Printer port
Second page memory option

This is a VERY limited extravaganza, so please act quickly

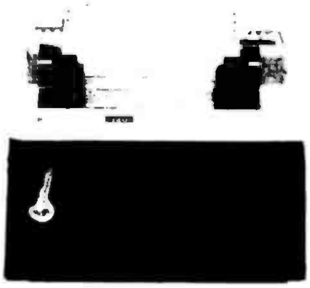
New!

Televideo 920c $860.

Same specs as above, save for special function keys, ideal for text editing and word processing

ELECTROLABS

POB 6721 Stanford CA 94305
(415) 321-5601 (800) 227-8266
Telex: 345567 (Electrolab Pla)



Paper Tiger

IDS MODEL 440

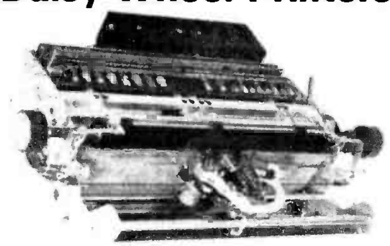
- 8 Software Selectable Character Sizes
- Parallel & Serial Interface
- 98 ASCII Character set, upper & Lower case
- Forms length control
- Tractor Feed $899.

Graphics option with 2K CRT screen buffer add $199.00

Dynamic Devices Modem

- Acoustically coupled modem assembly set
- Asynchrous 0-300 Baud
- Switchable originate or answer modes
- Operates full or half duplex mode
- 15 minute assembly $129.
- Novation Cat $179.
- Digicomm Coupler $189.

Daisy Wheel Printers



Qume Sprint 3\45

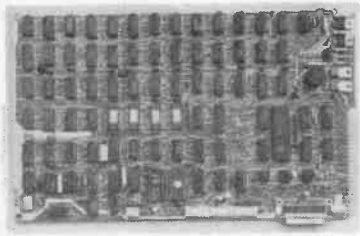
PRINTER (factory warr.)	$1499.
POWER SUPPLY (Borschert) (Shown mounted on rear of printer)	349.
COMBINATION SPECIAL	1699.
Cases available	200.
S-100 interface card	149.
SPRINT 5/45 RO, RS-232 Complete, assembled, in case, plug-in & print, hence, no muss & no fuss	$2699.

EASTER IC EGG HUNT
(while supply lasts)

2708	$ 8.50	2114	$ 5.99
2716	25.00	2114-2	6.99
2732	95.00	pd411	2.50
2147	12.95	21L02 450 Ns	1.05
6502	$ 6.25		
6809	49.00		
6845	39.00		
8085	13.00		
1771	26.95		
1791	37.95		
AY5-1013A	3.95		

UNPRECEDENTED!!!
* 16K Dynamic RAM Set of 8 For: TRS-80, Apple, Exidy, Heath, etc.
* Includes all parts & instructions
* 200 NS $59.

Please call for dealer or quantity pricing. Minimum order $20.00
We do custom prom programming.



ESAT 200B

BI-LINGUAL 80x24 COMMUNICATING TERMINAL

Scrolling, full cursor, bell, 8x8 matrix, 110- 19,200 baud, Dual Front Applications. Arabic & Hebrew, Multilingual Data Entry Forms Drawing, Music, & Switchyards. $279.

Circle 306 on inquiry card.

DIGITAL MULTIMETERS

Sinclair PDM35 Reg. $69.95 **$49.95**

Hickok LX303 **$69.50**

B&K PRECISION 3½-Digit Portable DMM Model 2800

Beckman TECH310 **$130.**

MURAPHONE Cordless Telephone System
Reg. $89.95 **$74.95**

GTE Flip-Phone™
$37.95

Portable VOM Multitester
Model VM520 **$19.95**
▪ 20 KΩ VDC ▪ 10 KΩ VAC

HICKOK Digital CB In-Line Tester
$169.95 Reg. $399.00
Model 388

100 MHz 8-Digit Counter (CSC)
▪ 20 Hz to 100 MHz range ▪ LED display ▪ Fully automatic
Model MAX100 Reg. $150.00 **$127.50**

6"x9" 3-Way Speaker
▪ 20 oz. ceramic magnet
Model BP2000-69TR **$14.95 ea.**

CSC Logic Monitor
• Automatically displays static and dynamic logic • Works with DTL, HTL, TTL, and CMOS • 16 LED display
Model LM-1 **$59.95**

Telephone Answering — CODE-A-PHONE
Model 1500 Call Control Reg. $349.95 **$249.95**
Model 1400 **$199.95**

FREE
8 pc. Tool Set (value $14.95) with $200.00 purchase from this ad.

Portable Oscilloscopes (NLS)
15 MHz Dual Trace Triggered Miniscope Reg. $435.00 **$369.95** Model MS-215

15 MHz Triggered Miniscope Model MS-15 Reg. $319.00 **$269.95**

30 MHz Dual Trace Triggered Miniscope Model MS-230 Reg. $559.00 **$479.95**

CSC Function Generator
Model 2001 Reg. $185.95 **$157.95**
▪ Sine-, square-, triangle- and separate TTL square wave output ▪ Frequency range: 1Hz-100KHz

Weller® Xcelite® Attache Style Tool Case
Model TC100/ST Reg. $471 **$279.95**

Service Master Tool Kit
Model 99-SM Reg. $69.95 **$47.50**

B&K PRECISION Portable Digital Capacitance Meter
Model 820
▪ Measures capacitance from 0.1pF to 1 Farad ▪ Resolves to 0.1pF ▪ 10 ranges for accuracy and resolution ▪ 4 digit easy-to-read LED display ▪ 0.5% accuracy

WAHL ISO-TIP 60 Cordless Soldering Iron
$29.95 Model 7800

Thermal-Spot Model 5800 **Circuit Tester $29.95**

Miniature High Fidelity 3-Way Stereo Speakers
Reg. $149.95 **$69.50 PR**
Model HF-9

CSC 3½-Digit 0.1% Digital Capacitance Meter
Model 3001
▪ 9 ranges from 1999 pF to 199.9 μF
▪ 0.1% of reading accuracy
Reg. $190.00 **$170**

In-Dash Car Stereos
8-Track Tape Player with AM/FM/MPX Radio Model C-777 **$52.50**

Cassette Tape Player with AM/FM/MPX Radio Model CAS-888 **$57.50**

DIGITAL MULTIMETER Simpson 461
Complete with nickel-cadmium batteries, AC charger/adapter, test leads
$149.95

CSC Logic Probe
▪ Compact circuit powered ▪ Detects pulses as short as 50 μsec ▪ DTL/TTL/HTL/CMOS compatibility
$44.95 Model LP-1

CSC Proto Preassembled Boards
Model PB-104 **$49.95**
Fully assembled breadboard contains four QT-59S sockets, seven QT-59B bus strips and four 5-way binding posts

Proto Board with Built-in Power Supplies
▪ Regulated ▪ Short-proof
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BSR X-10 Remote Control for Lights & Appliances
4 Pc Standard Starter Kit ▪ One (1) Standard Command Console • Two (2) Lamp Modules • One (1) Appliance Module Reg. $87.95 **$79.50**

5 Pc Ultrasonic Starter Kit ▪ One (1) Deluxe Ultrasonic Command Console • One (1) Hand Held Remote Unit ▪ Two (2) Lamp Modules ▪ One (1) Appliance Unit Reg. $112.95 **$99.95**

Lamp Modules $14.50 · Appliance Modules $14.50 · Wall Switch Modules $14.50
Standard Command Console $36.00
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Stereo Power Booster
Model POW-40 ▪ 40W stereo **$24.95**

RC Circuit Box
▪ 36 resistors (15 Ω to 10 MΩ) ▪ 18 capacitors (100 pf to 0.22 μf)
Reg. $49.95 **$42.** includes test leads
VIZ Model WC 412A

Magnifier Lamp
Precision ground and polished magnification lens. Model MG10A **$49.95**

30 MHz LEADER Dual Trace with Delay Line
$899.95 Model LBO-520

Chess Challenger 7
Reg $110.00 **$79.95** Model BBC

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B&K PRECISION 30 MHz Portable Frequency Counter
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501.00 to 750.00	7.50
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4001	.22	4023	.22	4066	.70	74C83	1.30
4002	.22	4024	.75	4069	.45	74C86	.50
4006	1.10	4025	.22	4071	.20	74C93	.95
4007	.27	4027	.45	4072	.35	74C151	1.75
4009	.45	4028	.80	4081	.22	74C157	1.75
4010	.45	4029	.95	4093	.95	74C160	1.20
4011	.22	4030	.45	4516	1.00	74C161	1.15
4012	.22	4034	2.25	4518	1.00	74C163	1.00
4013	.40	4035	.97	4520	1.00	74C165	1.25
4014	1.20	4040	1.00	74C00	.27	74C173	1.20
4015	1.00	4042	.85	74C07	.27	74C174	1.20
4016	.45	4045	.45	74C08	.30	74C175	1.20
4017	1.05	4046	1.95	74C10	.27	74C192	1.30
4018	.90	4049	.75	74C14	1.20	74C193	1.40
4019	.45	4050	.45	74C20	.27	74C901	.50
4020	1.10	4051	1.10	74C42	.90	74C902	.50
4021	1.10	4052	1.10	74C73	.75	74C914	1.90
4022	1.00	4053	1.10	74C74	.50		

1488 RS232 INTERFACE	1.40	5280/2107B 4K DYN RAM	3.60
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2708 8K EPROM (450 ns)	9.95	82S126	2.95
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UPD410 1-4K STAT. RAM	9.95	8225S	5.95
4116 2 16K RAM 150 NS	9.95	8251	6.95
4116 3 16K STATIC RAM 300 NS	5.50	8834	2.25

8130	2.95	8T380	2.25	8837	2.25
8131	2.95	8830	2.95	8838	2.25
8833	2.50				

DATEL'S DAC-08BC — 8 bit DAC — $9.95

8" DISKETTES — HARD SECTOR
$1.75, 10/$16.00

CRYSTALS $3.45 ea.
2.000 MHz · 4.000 MHz · 3.57 MHz · 5.000 MHz · 6.000 MHz · 6.144 MHz · 8.000 MHz · 10.000 MHz · 20.000 MHz

RIBBON CABLE FLAT (COLOR CODED) #30 WIRE
26 cond. - .50/per foot
40 cond. - .75/per foot
50 cond. - .90/per foot

UNIVERSAL 4Kx8 MEMORY BOARD KIT
$69.95
32-2102-1 fully buffered, 16 address lines, on board decoding for any 4 of 64 pages, standard 44 pin buss, may be used with F 8 + KIM

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FCS 8024 - 4 digit C.C. 8" display	$5.95	DL-707 C.A. .3"	$ .75
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FND 510 C.A. .5"	$ .85	HP3400 .8" CA	$1.95
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PRINTED CIRCUIT BOARD
4" x 6" DOUBLE SIDED EPOXY BOARD 1/16" thick $.60 ea. .... 5/$2.60

EPOXY glass vector board 1/16" thick with 1/10" spacing $1.95

74S00	.30	74S16	.40	74S151	1.25
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74S08	.40	74S86	.65	74S158	1.25
74S11	.35	74S112	.85	74S174	1.40

7 WATT LD-65 LASER DIODE IR $8.95
25 watt Infra Red Pulse (SG 2006 equiv.) Laser Diode (Spec sheet included) $24.95

MINIATURE MULTI-TURN TRIM POTS
100K, 5K, 10K, 20K, 250K, 1 Meg. $.75 each 3/2.00

2N3820 P FET	$ .45
2N 5457 N FET	$ .45
2N2646 UJT	$ .45
ER 900 TRIGGER DIODES	4/$1.00
2N 6028 PROG. UJT	$ .65

FP 100 PHOTO TRANS.	$ .50
RED, YELLOW, GREEN LARGE LED's. 2"	6/$1.00
RED/GREEN BIPOLAR LED's. 2"	$ .95
TIL-118 OPTO-ISOLATOR	$ .75
MCT-6 OPTO ISOLATOR	$ .80
1 WATT ZENERS: 3.3, 4.7, 5.1, 5.6, 9.1, 10, 12, 15, 18, or 22V	6/$1.00

TTL REED RELAY — SPST 5V 20ma $1.00

Silicon Power Rectifiers

PRV	1A	3A	12A	50A	125A	240A
100	.06	.14	.35	.90	3.70	5.00
200	.07	.20	.40	1.30	4.25	6.50
400	.09	.25	.65	1.50	6.50	9.60
600	.11	.30	.80	2.00	8.50	12.50
800	.15	.35	1.00	2.50	10.50	16.50
1000	.20	.45	1.25	3.00	12.50	20.00

SILICON SOLAR CELLS
4" diameter .4V at 1 AMP. $10.00

IN 4148 (IN914) .... 15/$1.00
.1 or .01 uf 25V ceramic disc. caps. 16/$1.00, 100/$50.00

RS232 CONNECTORS
DB 25P male $2.95
DB 25S female $3.50
HOODS $1.50

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323K - 5V 3A	$5.75	340K - 12, 15 or 24 V	$1.50
309K	$1.60	340T - 5, 6, 8, 12, 15, 18 or 24 V	$1.30
723	$ .50	79MG	$1.35
320T - 5, 12, or 15V	$1.30	320M5	$ .75
LM305H	.75		

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2N6233 NPN SWITCHING POWER	$1.95
MRF 8004 a CB RF Transistor NPN	$ .75
2N3772 NPN Si TO-3	$1.00
2N4908 PNP Si TO-3	$1.00
2N5086 PNP Si TO-92	4/$1.00
2N3137 NPN Si RF	$ .55
2N3919 NPN Si TO-3 RF	$1.50
2N1420 NPN Si TO-5	3/$1.00
2N3767 NPN Si TO-66	$ .70
2N2222 NPN Si TO-18	5/$1.00
2N3055 NPN Si To-3	$ .60
2N3094 NPN Si TO-92	6/$1.00
2N3906 PNP Si TO-92	6/$1.00
2N5296 NPN Si TO-220	$ .55
2N1546 PNP GERM TO-3	$ .95
2N1309 PNP GE TO-5	$ .40

TTL IC SERIES

7400	.17	7448	.75	74155	.75
74101	.17	7450	.17	74157	.65
7402	.17	7472	.35	74160	.85
7403	.17	7473	.35	74161	.80
7404	.24	7474	.42	74162	1.20
7405	.24	7475	.49	74163	.82
7406	.33	7476	.45	74164	.85
7407	.35	7480	.45	74165	.85
7408	.27	7483	.60	74166	1.05
7409	.24	7485	.75	74167	1.35
7410	.17	7486	.42	74170	1.60
7411	.22	7489	1.60	74173	1.30
7412	.22	7490	.50	74174	.85
7413	.42	7491	.55	74175	.75
7414	.90	7492	.50	74176	.75
7416	.33	7493	.50	74177	.75
7417	.37	7494	.60	74180	.75
7420	.17	7495	.80	74181	1.90
7425	.35	7496	.80	74190	1.20
7426	.33	74107	.35	74191	1.20
7427	.35	74121	.35	74192	.79
7430	.17	74122	.39	74193	.79
7432	.27	74123	.42	74194	.85
7437	.27	74125	.45	74195	.65
7438	.27	74126	.45	74196	.85
7440	.17	74145	.75	74197	.85
7441	.85	74148	1.10	74276	1.95
7442	.50	74150	1.10	74279	.75
7445	.70	74151	.65	74368	.65
7446	.75	74153	.55	74325	2.25
7447	.75	75154	1.10	75491	1.05
				75492	1.05
				8197	1.25
				8798	1.10

14 pin headers .... 3/$1.00
16 pin headers .... $.40 ea.

MM5387AA .... CLOCK CHIPS $5.95
MM5314 .... $4.75

NO. 30 WIRE WRAP WIRE SINGLE STRAND
100' $1.40

ALCO MINIATURE TOGGLE SWITCHES
MTA 106 SPDT $1.05
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74LS05	.35	74LS162	1.10
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74LS09	.35	74LS164	1.10
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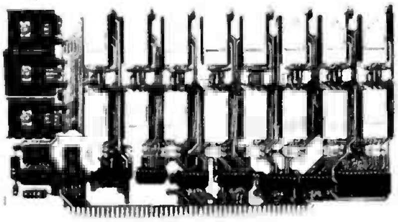

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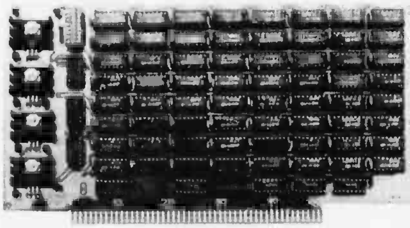

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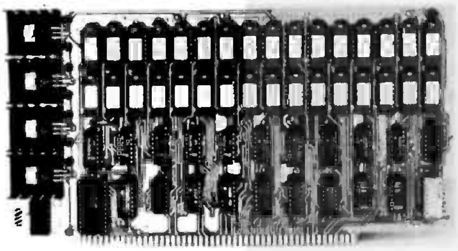

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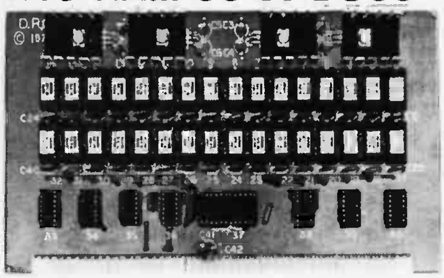

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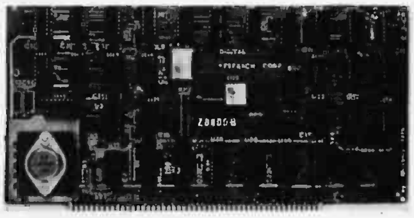

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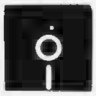

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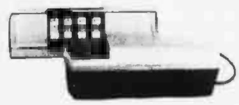

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CD4069	.35	74C161	2.39
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CD4071	.35	74C164	2.39
CD4072	.35	74C173	2.59
CD4073	.35	74C174	2.75
CD4075	.35	74C175	2.75
CD4076	1.29	74C192	2.39
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74LS00N	.35	74LS164N	1.19
74LS01N	.28	74LS165N	.89
74LS02N	.28	74LS166N	2.48
74LS03N	.28	74LS168N	1.89
74LS04N	.39	74LS169N	1.89
74LS05N	.28	74LS170N	1.99
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74LS10N	.28	74LS175N	.99
74LS11N	.39	74LS181N	2.20
74LS12N	.39	74LS190N	1.15
74LS13N	.47	74LS191N	1.15
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74LS15N	.39	74LS193N	.98
74LS20N	.26	74LS194N	1.15
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74LS76N	.45	74LS261N	2.49
74LS78N	.65	74LS266N	.59
74LS83AN	.99	74LS273N	1.75
74LS85N	1.19	74LS275N	4.40
74LS86N	.45	74LS279N	.59
74LS90N	.75	74LS283N	1.10
74LS92N	.75	74LS290N	1.29
74LS93N	.75	74LS293N	1.95
74LS95N	.88	74LS295N	1.10
74LS96N	.98	74LS298N	1.29
74LS107N	.45	74LS324N	1.75
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74LS113N	.49	74LS352N	1.65
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74LS124N	1.35	74LS366N	.99
74LS125N	.89	74LS367N	.99
74LS126N	.89	74LS368N	.99
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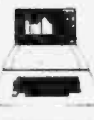

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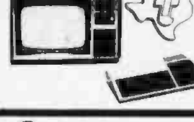

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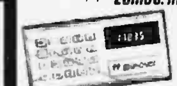

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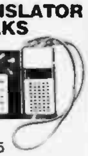

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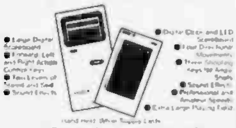

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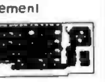

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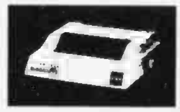

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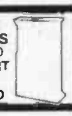

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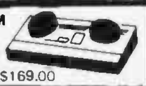

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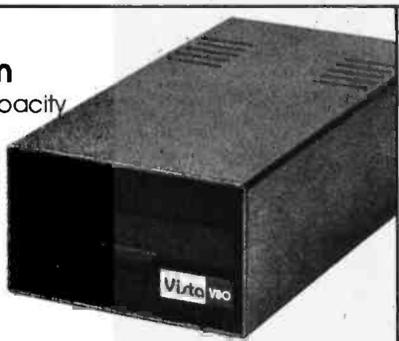
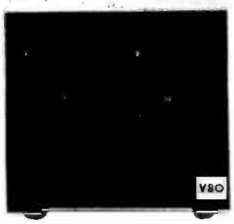

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WANTED: Printer for use with Apple II. Will trade (or sell) Nikon FTN camera with f1.4 lens, Speedlight and Ringlight units, filters, closeup rings, and many other attachments. Write for complete list and send description of printer. Also, will sell Applesoft II read-only memory card for $100 or highest bid. Gene Boggess, Star Route POB 220-6, Columbus MS 39701, (601) 327-6555.

FOR SALE: BYTE, *Kilobaud, Interface Age;* 1977 and 1978 plus some odd issues. Best offer. Les Palenik, 25 Allview Cres, Toronto Ontario, CANADA M2J 2R4.

FOR SALE: 16 DIP (4 K by 1-bit) dynamic programmable memories (a set of eight). Motorola 7839; 250 ns chips. Interchangeable with TMS 4027, Intel 2104A-3, MK 4096-6, and many other brands. In excellent condition, used approximately twenty hours. I upgraded my TRS-80 with 16 K chips. Will sell for $35. Daryl Holder, Rt #2 POB 260-C, Loretto TN 38469, (615) 853-6740 after 4 PM.

FOR SALE: Complete ready-to-go SwTPC system. 6800/1 upgraded to a 6800/2, 28 K, MP-T board, CT-64 in customized cabinet, Hitachi 12-inch with direct video interface, PR-40 with parallel interface, AC-30, JPC TC-3 4800 bps tape interface with CFM/3 operating system. All documentation, assembly instructions, user guides, and source listings included. Software: three BASICs, three Assemblers, two Editors, Disassembler, Tracer, Relocator, games, and more. $1950. Allen Porter, 493 Selfridge Dr, Colorado Springs CO 80916, (303) 574-4146.

FOR SALE: I have four Shugart SA400 disk drives for $285 each and two Shugart SA801 disk drives for $420 each. Need money fast; will take good offer. They work great and were bought in 1979. Four drive cables for $20. David Sparks, 5232 Cornell Ave, Westminster CA 92683, (714) 997-7640.

FOR SALE: 6800 Microprocessor Trainer by Heathkit, Model ET-3400. Includes all manuals, built and tested trainer, programmed learning course (ET-3401), specially built peripheral interface adapter experiment board, and all parts for experiments. $365 value, sell for $315. Excellent condition. James Temple, 24 Spruce Ave, Bethpage NY 11714, (516) 822-6083.

FOR SALE: ESAT 200B 80/24 terminal, $220; GRI 756 keyboard with case, $60; Leedex Video 100 monitor, $100; SD Z80 starter system with 4 K programmable memory, added operating system for video display on 2 K erasable-programmable read-only memory, $260. All assembled, little used, perfect working condition. G Kish, 1621 Payne, Wichita KS 67203, (316) 262-7315.

FOR SALE: Heathkit (Motorola 6800 processor) computer and the Heath H9 video terminal. Computer has 4 K memory expandable to 64 K. Includes BASIC in read-only memory, double-function keypad on computer console, 1 K monitor also with access to memory and processor registers, 8-bit parallel and serial input/output (I/O) with EIA or 20 mA current loop. Cassette interface and cables. Complete documentation and operation manuals. Burned in for one hundred hours. Asking $480. Osi McReynolds, Rt #1 POB 71-B, Coeburn VA 24230, (703) 395-3797.

FOR SALE: PerSci Model 277 dual-diskette drive with a Model 1070 intelligent diskette controller. Capacity ½ megabytes. All books and line diagrams included. Part of a purchased system that was used for six months. James Holle, 9613 W Lincoln Ave, West Allis WI 53214, (414) 541-9808.

FOR SALE: S-100: Vector Graphic 8 K static programmable memory (250 ns), $120. Ithaca Audio Z80A processor (4 MHz), $120. SSM IO-4 (four parallel and two serial ports), $100. SSM PB-1 2708/2716 programmable read-only memory programmer, $110. SSM VB-1B video interface, $100. ECT rack-mount card cage with Thinker Toys Wunderbuss 20-slot mother board and all connectors, $175. All boards assembled and tested, used less than twenty-five hours. Will consider best offer. Send money order to Richard Haendel, 2500 Nonesuch Rd Apt 16-G, Abilene TX 79605, (915) 692-5405.

FOR SALE: PolyMorphic video terminal interface (VTI) board for S-100 systems. Video is spotty, but also can be used as parallel input port (8212 on board) and 1 K programmable memory. Fully socketed, never used, video should be easily fixable. $75 or best offer. Roger Buldain, 601 N Francis, Lansing MI 48912, (517) 337-2278.

FOR SALE: Heathkit ET-3400 Microprocessor Trainer with EE-3401 self-instruction program. Extra memory chips and components. Assembled and in excellent condition. Asking $150. William Portl, Second St, Evans City PA 16033, (412) 538-5454.

WANTED: Program libraries (manuals) for obsolete but working HP-9100A and/or HP-9100B desktop calculators. Thomas H Richardson, Kansas Wesleyan, Dept of Chemistry, Salina KS 67401.

FOR SALE: E-HUH 8100 S-100 bus expansion interface for TRS-80. On-board programmable UART, serial and parallel input/output (I/O), 16 K, 250 ns programmable memory, six card slots. All enclosed in custom metal cabinet with power supply. Full hardware and software documentation. Ready to plug in and turn 16 K system into 32 K. Cables included. Must sell, $700 value only $500. Michael Lesser, 14623 Pine Glen Cir, Lutz FL 33549, (813) 971-8492 nights.

FOR SALE: S-100 system; IMSAI front panel with vector 18-slot mother board, in case with power supply, $200; IMSAI MIO, $100; 8 K WMC Static Mem-1, $100; two 4 K static, $50 each; Ithaca Audio Z80 processor, $125; Cromemco Bytesaver, $125. Above boards operating in system. Tarbell Floppy-Disk Controller, partially assembled, $125; three IBM 8-inch FD33 floppy disks, one complete, one less interface card, and one less motor and interface card, all three for $225. Digitronics high-speed paper tape, with 8-inch autospooler, $100; TDL S-100 case, $20. John Potter, 5439 Eadie Pl, West Palm Beach FL 33407, (305) 686-4666.

FOR SALE: Two Viatron 21s, one robot printer. $500 for three units. Also, SwTPC 6800 and CT-1024, $250. G Ludwig, POB 408, Rice Lake WI 54868, (715) 234-2680.

FOR SALE: Crossassembler for M6800 microprocessor. 4-kilo word program written in BASIC for HP-2000A. Directly usable in other HPs. With simple changes, it assembles languages of other 8-bit microprocessors. Program supports same properties as Motorola's own crossassembler. Program on paper tape, full documentation, user manual, and two-year full support; $163 (includes postage). For manual and documentation, send $3. If required: program in other languages or on other media. Panu Pietikainen, Rauduntie 11 H, SF-02130 Espoo 13, FINLAND.

WANTED: Copy of Z80 Assembler listing from BYTE Nybbles library. Harlan Michael, 315 Valley Vista Dr, Jackson MS 39211, (601) 982-6533 days or (601) 956-5268 evenings.

FOR SALE: Three Heath 4 K by 16 memory boards. All in excellent condition with documentation. $100 each, or all three for $270. Dan Buckler, 6115 A 42nd Pl, Hyattsville MD 20781, (301) 927-0765.

FOR TRADE: Compucolor game programs for other homemade game programs written for the Compucolor II. Programs must be 8 K or less. Paul Weisberg, POB 2453, Melfort Saskatchewan, CANADA S0E 1A0, (306) 752-3566.

FOR SALE: Five new single-board 8080A microprocessors, completely assembled and tested. Each includes 1 K by 8 erasable-programmable read-only memory and 256 by 8 programmable memory. Complete documentation, featured in *CQ* magazine April, May, June 1979. $50 each. Platteter, 1315 Q St, Bedford IN 47421, (812) 279-6265.

WANTED: Ohio Scientific Superboard IIs with all manuals and documentation, up to $150 paid depending on year and condition. Send year and condition for my offer. For Sale: TI 99/4 microcomputer. Paid $1150, first certified check for $1075 gets it. Brand new and still in original carton. Or will trade TI 99/4 for $950 plus Ohio Scientific Superboard II in good condition. Gregg Beasey, 15 Cardinal Ln, East Islip NY 11730.

FOR SALE: Control Data Corp 10 megabytes disk drive for AlphaMicro AM-500 system. Elmer G Mitchell, 1520 18th St, Huntsville TX, (713) 291-3447.

WANTED: I have a small amount of 8080 equipment (processor, a few support chips) and a large supply of other stuff (74xx, MM3501, etc) and would like to buy or trade for anything 6800ish (processor, bareboard, support, etc). Give a hand to an uprooted American. R M Bownes, 146 Warren Rd, Donaghdee County Down, NORTHERN IRELAND BT21 OPQ. PS: Please use airmail, it's a lot faster.

WANTED: Drawings and schematics for making an electrical sleep device, and other schematics for experimental hypnosis. K de Groot, P-Lastmanstr. 7, Helmond, HOLLAND.

WANTED: Heathkit Microprocessor Trainer ET-3400 and Memory I/O Accessory ETA-3400 for use with Heathkit Microprocessor Course. Will trade for Teletype printer parts, and/or cash. Please write and give details (ie: assembled/unassembled and if the unit(s) are operational). George Keim, POB 160, Yap Island GU 96943. First class mail for fastest reply, US Domestic Post Office rates.

February BOMB Results Graph Theory

Readers of BYTE expressed a burning interest in "A Computer-Controlled Wood Stove" by Steve Ciarcia (page 32). Steve won first place in the voting, his fourth first-place finish in as many months. Second place in the tally went to John A Lehman for "A Financial Analysis Program" (page 192). Judging from comments written on the BOMB cards, many readers were fascinated by an example of the balance sheet for MITS, Inc. Third place was taken by Ted Carter for "Implementing Dynamic Data Structures with BASIC Files" (page 92). Fourth place was taken by Robert A Morris for "Comparison of Some High-Level Languages" (page 128).

Reader Service

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BOMB

BYTE's Ongoing Monitor Box

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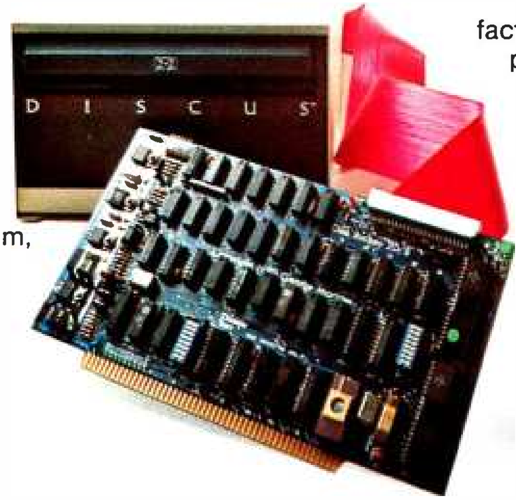

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