

BYTE

THE SMALL SYSTEMS JOURNAL[®]

APRIL 1987 VOL. 12, NO. 4

\$3.50 IN UNITED STATES
\$4.50 IN CANADA / £1.75 IN U.K.
A MCGRAW-HILL PUBLICATION
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Instruction Set Strategies

The Rising Mac



MACINTOSH SE

MACINTOSH II



Eureka: The Solver™

Anyone and everyone who routinely works with equations needs Eureka: The Solver

It solves the most complex equations in seconds. Whether you're a scientist, engineer, financial analyst, student, teacher, or some other professional, you need Eureka: The Solver!

Any problem that can be expressed as a linear or non-linear equation can be solved with Eureka. Algebra, Trigonometry and Calculus problems are a snap.

Eureka: The Solver also handles maximization and minimization problems, does plot functions, generates reports, and saves you an incredible amount of time.

$X + \exp(X) = 10$ solved instantly instead of eventually!

Imagine you have to "solve for X," where $X + \exp(X) = 10$, and you don't have Eureka: The Solver. What you do have is a problem, because it's going to take a lot of time guessing at "X." Maybe your guesses get closer and closer to the right answer, but it's also getting closer and closer to midnight and you're doing it the hard way.

With Eureka: The Solver, there's no guessing, no dancing in the dark—you get the right answer, right now. (PS: $X = 2.0705799$, and Eureka solved that one in .4 of a second!)

How to use Eureka: The Solver

It's easy.

1. Enter your equation into the full-screen editor
2. Select the "Solve" command
3. Look at the answer
4. You're done

You can then tell Eureka to

- Evaluate your solution
- Plot a graph
- Generate a report, then send the output to your printer, disk file or screen
- Or all of the above

Eureka: The Solver includes

- ☑ A full-screen editor
- ☑ Pull-down menus
- ☑ Context-sensitive Help
- ☑ On-screen calculator
- ☑ Automatic 8087 math co-processor chip support
- ☑ Powerful financial functions
- ☑ Built-in and user-defined math and financial functions
- ☑ Ability to generate reports complete with plots and lists
- ☑ Polynomial finder
- ☑ Inequality solutions

*Introductory price—good through July 1, 1987

Some of Eureka's key features

You can key in:

- ☑ A formula or formulas
- ☑ A series of equations—and solve for all variables
- ☑ Constraints (like X has to be < or = 2)
- ☑ A function to plot
- ☑ Unit conversions
- ☑ Maximization and minimization problems
- ☑ Interest Rate/Present Value calculations
- ☑ Variables we call "What happens?," like "What happens if I change this variable to 21 and that variable to 27?"

All this power for only \$99.95!

Equation-solving used to be a mainframe problem, but we've solved that problem.

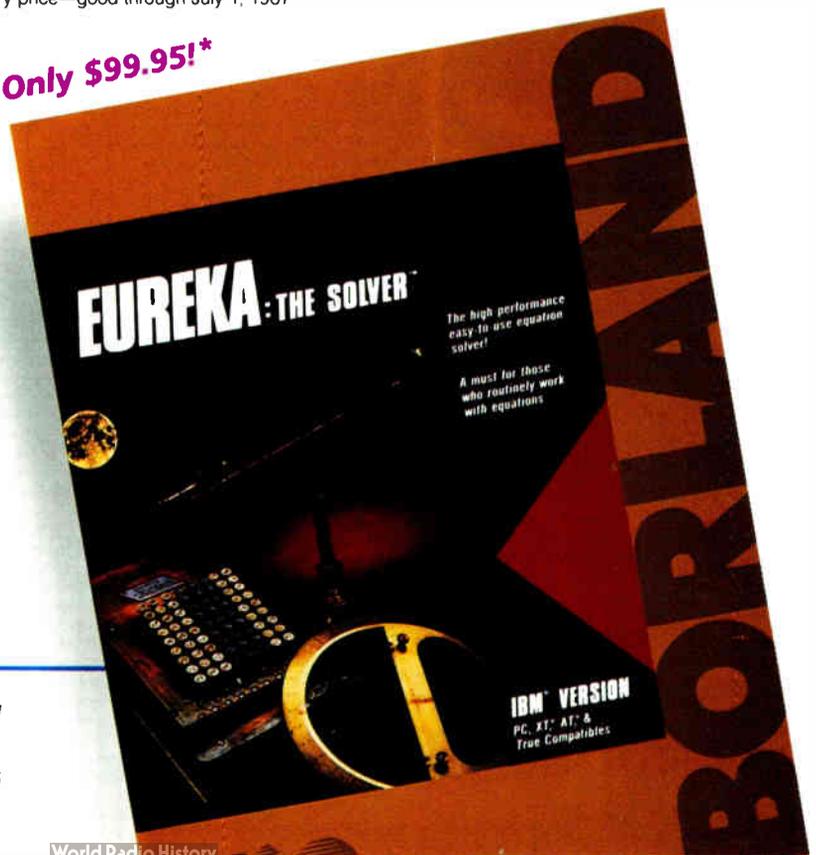
Eureka: The Solver is all you need—and it's yours for only \$99.95!

That kind of savings you can calculate with your fingers!

System requirements

IBM PC, AT, XT, Portable, 3270 or true compatibles.
PC-DOS (MS-DOS) 2.0 and later. 384K

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Turbo Basic[®]

Introducing Turbo Basic, the high-speed BASIC you'd expect from Borland!

It's the BASIC compiler you've been waiting for. And it's so fast that you'll never have to wait again.

Turbo Basic is a complete development environment; it includes a lightning-fast compiler, an interactive editor, and a trace debugging system.

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With Turbo Basic your only speed is "Full Speed Ahead"!

You probably already know us for both Turbo Pascal[®] and Turbo Prolog.[™] Well, we've done it again!

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In fact, building fast compilers is a Borland specialty; both our Turbo Pascal and our Turbo Prolog outperform all their rivals by factors, and with Turbo Basic, we're proud to introduce the first high-speed BASIC compiler for the IBM[®] PC. If BASIC taught you how to walk, Turbo Basic will teach you how to run!

The Critics' Choice

“Borland has succeeded in stretching the language without weighing us down with unnecessary details . . . Turbo Basic is the answer to my wish for a simple yet blindingly fast recreational utility language . . . The one language you can't forget how to use, Turbo Basic is a computer language for the missus, the masters, the masses, and me.

Steve Gibson, InfoWorld

Borland's Turbo Basic has advantages over the Microsoft product, including support of the high-speed 8087 math chip.

John C. Dvorak ♪ ♪

Turbo Basic ends the basic confusion

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It's fast, BASICA-compatible, and because Turbo Basic is a Borland product, the price is right, the quality is there, and the power is at your fingertips. You see, Turbo Basic's part of the fast-growing Borland family of programming languages—we call it the "Turbo Family." Hundreds of thousands of users are already using Borland's languages, so you can't go wrong. So join a whole new generation of smart IBM PC users—get your copy of Turbo Basic today. You get an easy-to-read 300+ page manual, two disks, and a free MicroCalc spreadsheet—and an instant start in the fast new world of Turbo Basic. All of this for only \$99.95—Order your copy of Turbo Basic today!

Free spreadsheet included, complete with source code!

Yes, we've included MicroCalc, our sample spreadsheet, complete with source code, so that you can get started right away with a "real program." You can compile and run it "as is," or modify it.

A technical look at Turbo Basic

- ☑ Full recursion supported
- ☑ Standard IEEE floating-point format
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- ☑ New long integer (32-bit) data type
- ☑ Full 80-bit precision
- ☑ Pull-down menus
- ☑ Full window management

System requirements

IBM PC, XT, AT and true compatibles, PC-DOS (MS-DOS) 2.0 or later. One floppy drive, 256K

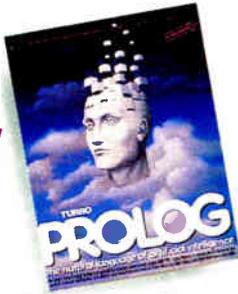
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Turbo Prolog™

“ If you're at all interested in artificial intelligence, databases, expert systems, or new ways of thinking about programming, by all means plunk down your \$100 and buy a copy of Turbo Prolog. **Bruce Webster, BYTE 9/86** ”

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\$99.95!



Turbo Prolog, the natural language of Artificial Intelligence, is the most popular AI package in the world with more than 100,000 users. It's the 5th-generation computer programming language that brings supercomputer power to your IBM PC and compatibles. You can join the AI revolution with Turbo Prolog for only \$99.95. Step-by-step tutorials, demo programs and source code included.

New! Turbo Prolog Toolbox

Our new Turbo Prolog Toolbox™ enhances Turbo Prolog—with more than 80 tools and over 8,000 lines of source code that can easily be incorporated into your programs. It includes about 40 example programs that show you how to use and incorporate your new tools.

New Turbo Prolog Toolbox features include:

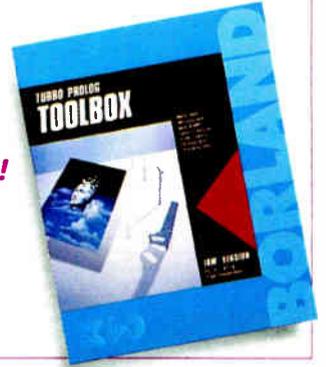
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System requirements

Turbo Prolog: IBM PC, XT, AT or true compatibles. PC-DOS (MS-DOS) 2.0 or later. 384K. Turbo Prolog Toolbox requires Turbo Prolog 1.10 or higher. Dual-floppy disk drive or hard disk. 512K.

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- Turbo Database Toolbox®
- Turbo Editor Toolbox®
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- Turbo GameWorks®
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- ☑ Matrix operations: inversions, determinants and eigenvalues
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3. Logarithm
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5. 5-term Polynomial

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System requirements

IBM PC, XT, AT or true compatibles. PC-DOS (MS-DOS) 2.0 or later. Turbo Pascal 2.0 or later. Graphics module requires graphics monitor with IBM CGA, IBM EGA, or Hercules compatible adapter card, and requires Turbo Graphix Toolbox. 8087 or 80287 numeric co-processor not required, but recommended for optimal performance. 256K.

Turbo Pascal 3.0

Includes 8087 & BCD features for 16-bit MS-DOS and CP/M-86 systems. CP/M-80 version minimum memory: 48K; 8087 and BCD features not available. 128K.



Turbo C[®]

Turbo C: The fastest, most efficient and easy-to-use C compiler at any price

Compilation speed is more than 7000 lines a minute, which makes anything less than Turbo C an exercise in slow motion. Expect what only Borland delivers: Quality, Speed, Power and Price.

Turbo C: The C compiler for amateurs and professionals

If you're just beginning and you've "kinda wanted to learn C," now's your chance to do it the easy way. Like Turbo Pascal, Turbo C's got everything to get you going.

If you're already programming in C, switching to Turbo C will considerably increase your productivity and help make your programs both smaller and faster. Actually, writing in Turbo C is a highly productive and effective method—and we speak from experience. Eureka: The Solver and our new generation of software have been developed using Turbo C.

Turbo C: a complete interactive development environment

Free MicroCalc spreadsheet with source code

Like Turbo Pascal and Turbo Prolog, Turbo C comes

with an interactive editor that will show you syntax errors right in your source code. Developing, debugging, and running a Turbo C program is a snap.

Turbo C: The C compiler everybody's been waiting for. Everybody but the competition

Borland's "Quality, Speed, Power and Price" commitment isn't idle corporate chatter. The \$99.95 price tag on Turbo C isn't a "typo," it's real. So if you'd like to learn C in a hurry, pick up the phone. If you're already using C, switch to Turbo C and see the difference for yourself.

System requirements

IBM PC, XT, AT and true compatibles. PC-DOS (MS-DOS) 2.0 or later. One floppy drive. 320K.

Technical Specifications

- Compiler:** One-pass compiler generating linkable object modules and inline assembler. Included is Borland's high performance "Turbo Linker." The object module is compatible with the PC-DOS linker. Supports tiny, small, compact, medium, large, and huge memory model libraries. Can mix models with near and far pointers. Includes floating point emulator (utilizes 8087/80287 if installed).
- Interactive Editor:** The system includes a powerful, interactive full-screen text editor. If the compiler detects an error, the editor automatically positions the cursor appropriately in the source code.
- Development Environment:** A powerful "Make" is included so that managing Turbo C program development is highly efficient. Also includes pull-down menus and windows.
- Links with relocatable object modules** created using Borland's Turbo Prolog into a single program.
- ANSI C compatible.**
- Start-up routine source code included.**
- Both command line and integrated environment versions included.**

*Introductory price—good through July 1, 1987

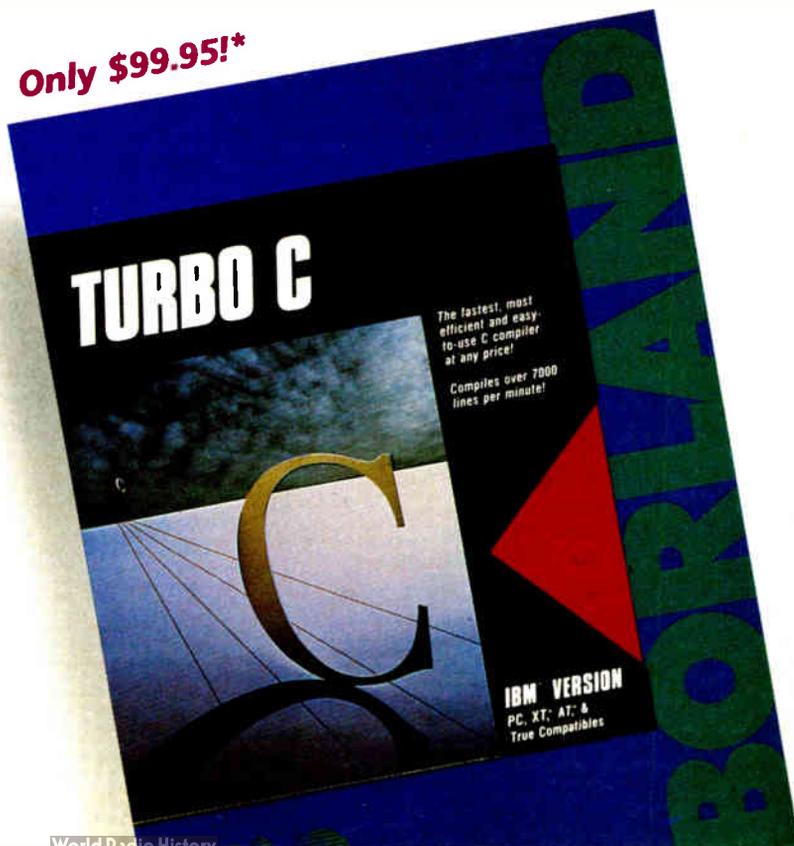
Sieve benchmark (25 iterations)

	Turbo C	Microsoft [®] C	Lattice C
Compile time	3.89	16.37	13.90
Compile and link time	9.94	29.06	27.79
Execution time	5.77	9.51	13.79
Object code size	274	297	301
Price	\$99.95	\$450.00	\$500.00

Benchmark run on a 6 Mhz IBM AT using Turbo C version 1.0 and the Turbo Linker version 1.0; Microsoft C version 4.0 and the MS overlay linker version 3.51; Lattice C version 3.1 and the MS object linker version 3.05.

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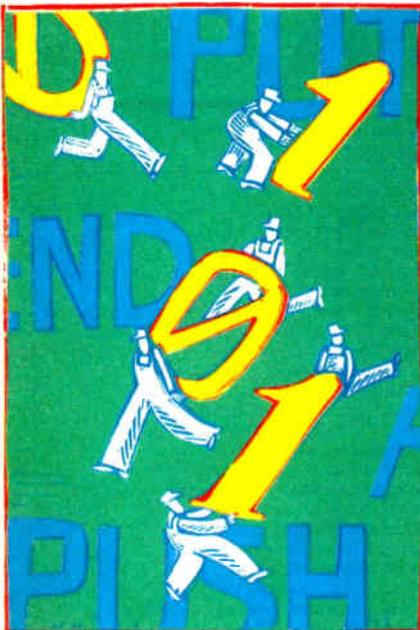
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BYTE (ISSN 0360-5280) is published monthly with one extra issue per year by McGraw-Hill Inc. Founder: James H. McGraw (1860-1948). Executive, editorial, circulation, and advertising offices: One Phoenix Mill Lane, Peterborough, NH 03458. phone (603) 924-9281. Office hours: Monday through Thursday 8:30 AM — 4:30 PM, Friday 8:30 AM — 1:00 PM, Eastern Time. Address subscriptions to BYTE Subscriptions, P.O. Box 590, Martinsville, NJ 08836. Postmaster: send address changes, USPS Form 3579, undeliverable copies, and fulfillment questions to BYTE Subscriptions, P.O. Box 596, Martinsville, NJ 08836. Second-class postage paid at Peterborough, NH 03458 and additional mailing offices. Postage paid at Winnipeg, Manitoba. Registration number 9321. Subscriptions are \$22 for one year, \$40 for two years, and \$58 for three years in the U.S. and its possessions. In Canada and Mexico, \$25 for one year, \$45 for two years, \$65 for three years. \$69 for one year air delivery to Europe. 31,000 yen for one year air delivery to Japan, 15,600 yen for one year surface delivery to Japan, \$37 surface delivery elsewhere. Air delivery to selected areas at additional rates upon request. Single copy price is \$3.50 in the U.S. and its possessions, \$4.25 in Canada and Mexico, \$4.50 in Europe, and \$5 elsewhere. Foreign subscriptions and sales should be remitted in U.S. funds drawn on a U.S. bank. Please allow six to eight weeks for delivery of first issue. Printed in the United States of America.

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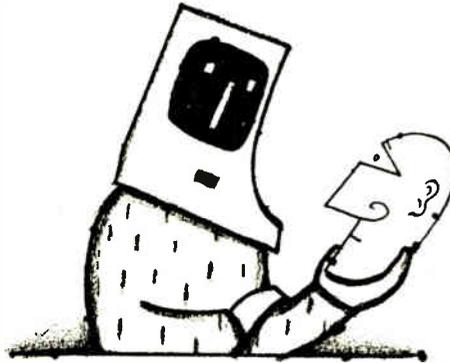
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EDITORIAL

Open Systems

With the March introduction of the Macintosh II—the open Mac—and the February introduction of the Commodore A2000—the open Amiga—the trend toward open, flexible personal computers has become dominant once again. Atari has announced that it will be opening its ST systems as well. Since the Apple II world and the IBM PC world have long had open architectures, the entire industry seems to recognize once again the need to let users upgrade their systems and adapt them for different applications. It is much easier to build in flexibility than to have 20/20 foresight about every owner's future needs.

The Macintosh II deserves praise for more than its openness. The CPU is a 68020, and every machine contains a 68881 floating-point processor as well. A memory management unit is optional. The NuBus is a full 32-bit bus designed to facilitate use of additional processor



cards. The graphics controller has unsurpassed flexibility. The standard I/O connectors will meet most people's needs. Backward compatibility with the Macintosh and the Macintosh Plus is high. As Gregg Williams and Tom Thompson point out in their in-depth Product Preview in this issue, the only apparent flaw is the absence of multitasking in the Macintosh systems software. Apple is hard at work on that, and context-switching programs can help in the meanwhile.

The Macintosh II has the most powerful standard equipment of any personal computer. It has no 640K-byte barrier to worry about and no shortage of sockets for memory. The Macintosh SE, with its one expansion slot, room for multiple internal disk drives, and other changes for somewhat faster operation, is a nice enhancement of the Macintosh Plus. Both machines have the superb Macintosh user interface.

All things considered—the open Apple IIGS, the new Macs, the responsiveness to criticism from users—Apple seems to be in a very strong position. No longer does product architecture box in the whole company. Indeed, the Macintosh II is a splendid foundation for the next decade of Apple hardware. John Scully, Jean-Louis Gassée, and the entire Apple development team deserve credit for thinking things through, establishing a sound strategy, and executing it flawlessly. We applaud them.

We also wish to note that Apple has left ample room on the low end for 68020 systems from Atari and Commodore. A Commodore A2000 with a 68020/68881 card from Computer System Associates in San Diego is the current price/performance leader among 68020-based

personal computers, but Atari and Commodore machines with 68020s as standard equipment should bring costs down further.

Extra 80386 Coverage

The first 1987 issue of the BYTE Listings Supplement is now available. Besides including source code to accompany selected articles that ran in the first quarter, the Listings Supplement contains 29 pages of excerpts from BIX conferences related to the Intel 80386. These excerpts contain a great deal of valuable technical information, especially relating to systems software. An order card for the Listings Supplement is found following page 208. The full text of all the conferences is, of course, available on BIX.

Bonus Electronic Articles— On-line Supplements to BYTE

This issue of BYTE introduces a new service to extend and complement our coverage. In addition to the articles published in the magazine, we will regularly publish related articles on BIX. Such articles will not appear in the table of contents at the beginning of BYTE, but they will be listed in the table of contents for the section to which they are related. (It will also be noted that they are available through BIX rather than in print.) Our first such bonus electronic article supplements this month's Theme section on instruction set strategies. The related article available on BIX covers the Acorn RISC Machine and was written by James J. Farrell III and John F. Stockton. (On BIX, join the apr87.sup conference and read the acorn.risc topic.)

Dick Pountain on Algorithms

Starting in June, Dick Pountain will write a column for BYTE on algorithms that will appear in the Kernel section. The first column is a dandy that covers RLL encoding. From now on, when Dick writes articles on major European products, they will appear in the Features section. Dick's news coverage will continue to appear in the international section of BYTE, distributed outside North America. Dick will be writing more for BYTE than ever. His new efforts will replace his popular BYTE U.K. column.

—Phil Lemmons
Editor in Chief

BIX Specials

BIX users have the advantage this month of being able to join a new conference called *bix.specials*. This conference contains never-before-published BYTE-quality articles that extend the magazine by providing BIX users the same high-quality information that has made BYTE famous.

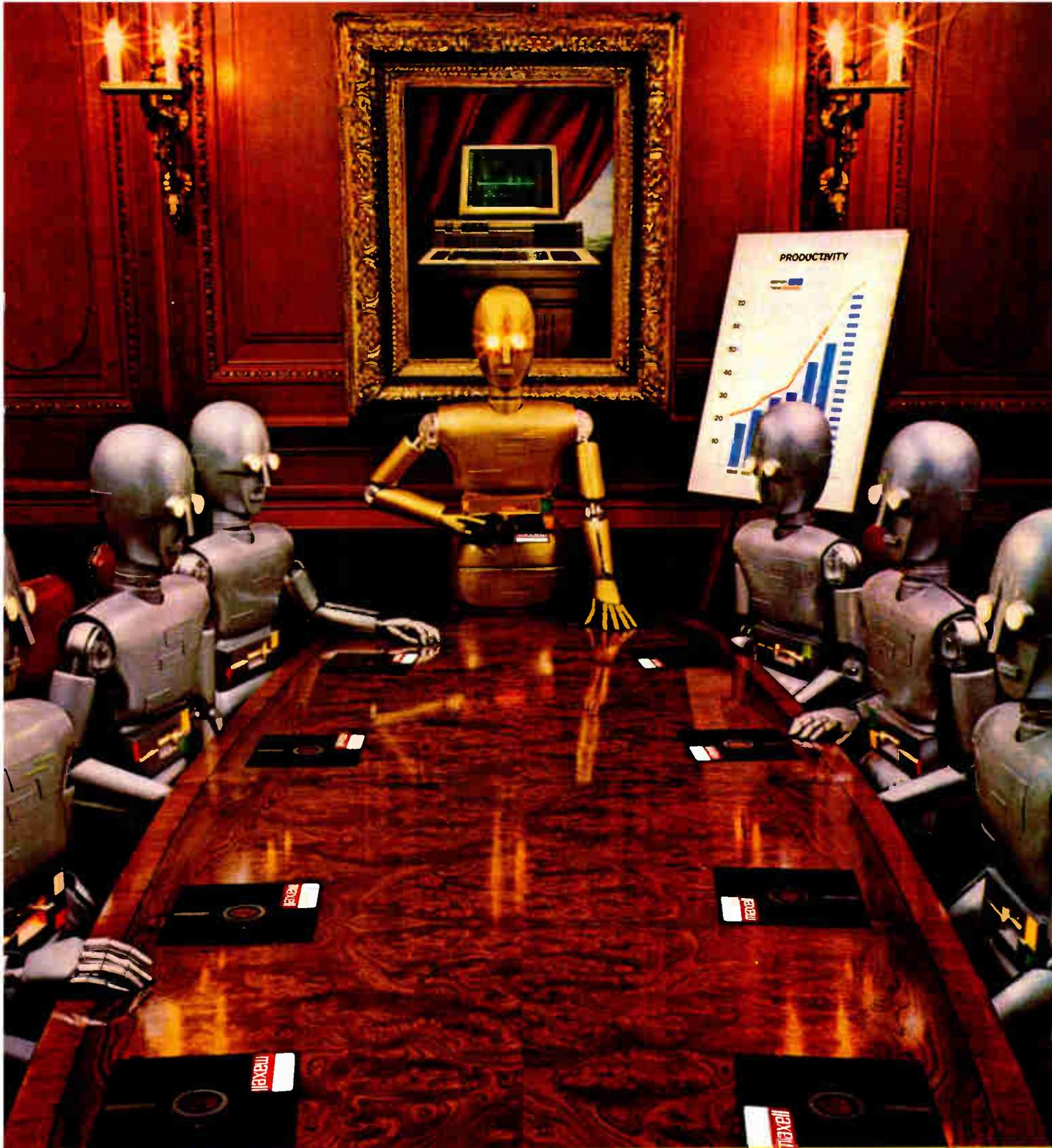
The *bix.specials* conference started off with the following:

Jim Mooney, a member of the working group creating IEEE standard 855-1985, gives BIX users a thorough overview of the MOSI standard for operating system interfaces.

Michael Keryan tells how to build a real-time clock for the Commodore Amiga for less than \$25. BIX's listings area contains a file with the schematics, timing diagrams, program listing, and a parts list for the unit.

Randy Finch describes an AmigaDOS batch program that prints a set of text files from a directory to an output device.

Best of all, the article authors are on hand to discuss their work directly with BIX users, doubly enhancing the worth of the articles.



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MICROBYTES

Staff-written highlights of developments in technology and the microcomputer industry.

Lipid Membranes as Electronic Components: Ultra-Small Memory with Low Power Requirements

Two physiologists have come up with a way to use lipid membranes as electronic components. Olaf Andersen of Cornell Medical Center and Robert Muller of the State University of New York Health Sciences Center (both in New York City) claim that memory elements based on this technology can be extremely small and function under very low power requirements.

Lipid membranes, which consist of a layer of lipid molecules only two molecules thick, are normally nonconductive. But with addition of an antibiotic substance called monazomycin, ion channels can be formed in the layer. The conductive capability of these channels varies with the applied voltage, allowing the membrane to act as a switch. The voltage involved, however, is only half a volt, much less than that required for traditional semiconductors.

One problem with the new technol-

ogy is that it is much slower than traditional semiconductor elements. But this slowness has an advantage for memory applications in that the memory would have to be refreshed less often (approximately once per second).

Although a patent has been issued for the technology, no lipid-membrane-based memory elements have been built yet, and both Andersen and Muller cannot predict when this technology might be used in working components. However, Muller, who has been working on this research since 1969, suggests that lipids may be used for other electronic tasks. According to Muller, by mixing the right proportion of lipids with water, one can create tiny tubes of conductive water surrounded by nonconductive lipids. Theoretically, you could use this technique to create wires measuring only 70 to 80 angstroms in diameter.

New Modulation Method Could Pack More Data onto Disks; Company Says It Plans Drive

A new modulation method promises more information on computer disks, better audio recording, and more efficient communications, according to its inventors. Called harmonic modulation, the method is being developed by Audel Inc. (Tucson, AZ), which hopes to license the technology to disk drive makers and others. Modulation, imparting information by varying a signal with time, is fundamental to transmitting and recording data electronically. In theory, information can be impressed on a signal by modulating any characteristic of the signal. Most common are amplitude modulation (AM), where the information varies the strength of the signal, and frequency modulation (FM), where the information varies the frequency of the signal. A third common method is phase modulation (PM), where the information varies the phase angle of the signal.

According to Richard C. Gerdes, co-inventor of the technique, harmonic

modulation varies another characteristic of the signal: the relationship between the basic frequency (the fundamental) and a frequency three times as high (the third harmonic.) "When viewed on a scope it could be called waveform modulation, but it is truly harmonic modulation," Gerdes said. The important thing is not the fundamental frequency or the third harmonic but the relationship between them. Since both the fundamental and the third harmonic are transmitted, the signal is inherently self-clocking and self-calibrating, the company claims.

Harmonic modulation offers a very high data-transmission rate, according to Audel. Gerdes said the process can encode 6 bits of information for every cycle of the fundamental frequency. Thus a 1-kHz signal can transmit 6000 bits of information per second. Most modulation systems can transmit much less information on a 1-kHz channel.

continued

Nanobytes

A report from **Dataquest** (San Jose, CA) on the international semiconductor market in 1986 showed three Japanese firms at the top of the list, based on revenues: **NEC**, **Hitachi**, and **Toshiba**. The research firm said this is the first time a U.S. company hasn't been among the reigning trio. The remaining top suppliers were, in order, **Motorola**, **Texas Instruments**, **Philips-Signetics**, **Fujitsu**, **Matsushita**, **Mitsubishi**, and **Intel**. Fluctuations in exchange rates had a "significant impact" on the chip industry and, hence, the rankings, **Dataquest** said. . . . **International Battery Corp.** (Reseda, CA) is marketing lithium replacement batteries for IBM PC ATs and work-alikes. The company says the batteries, made by **Tadiran**, are approved by **Underwriters Labs**. Each one costs \$27.50. . . .

Tallgrass Technologies (Overland Park, KS) has started shipping its **LightFile WORM** optical storage systems. Capacities range from 200 to 800 megabytes, and prices from \$5495 to \$12,495. The firm says its **LightTrack** software makes the WORM system "look and act like a normal DOS drive." **Tallgrass** is looking for VARs to handle the **LightFile** line. . . .

New England Software (Greenwich, CT) is selling an OEM version of **Graph-in-the-Box**—its memory-resident (128K) graph-generator software that works with IBM PCs and compatibles—to programmers and applications developers who want to incorporate it in their packages. The "starter" **Application Development Kit**, selling for \$187.60, contains the regular program, documentation, and a technical manual. Meanwhile in Sweden, **Ide Data AB**, the

continued

Swedish firm that developed Graph-in-the-Box, was given the Golden Cog Award, an annual prize for innovation in industry. Previous winners have been Saab, Philips, and Ericsson. This is the first time the prize has gone to a software house. . . .

Bedford Research Associates (Bedford, MA) has retooled the Interactive Signal Processing package to run on IBM's PC XT and AT. The system, previously available only for DEC's PDP and VAX machines, provides signal processing, graphics display, simulation, and database management capabilities. A license costs \$1300; maintenance and updates, \$300 a year. . . .

Thomson Consumer Products (Culver City, CA) is packing its 14-inch 450A monitor with the Chauffeur HT monochrome graphics adapter board from **STB Systems** (Richardson, TX) to let spreadsheet users fit 12 month columns and a totals column on the screen. The Spreadsheet Monitor supports a display width of 132 characters; the Chauffeur HT is compatible with the Hercules Graphics Card but offers resolution of 1056 by 352. The monitor/board combo costs \$545. . . .

The Farmer's Software Exchange (Fort Collins, CO) is a user's association organized to help farmers and ranchers. The group offers, at a discount, programs geared toward agricultural operations as well as word processing and database packages. For more information, phone (800) 237-4182, or write to the Exchange at P.O. Box 660, Fort Collins, CO 80522. . . .

Condor Computer (Ann Arbor, MI) has put its Condor 3 on a 3½-inch disk. The program occupies only 128K bytes, leaving about 600K for data. . . . **Centram** (Berkeley, CA), developer of the TOPS network, and **Blyth Software** (San Mateo, CA) are working on a TOPS version of Blyth's relational database package for the Macintosh, Omnis 3. As many as 32 users will be able to simultaneously share files. . . . In a film made by **Ray Kurzweil**, musician **Stevie Wonder** says technology has been for him "a brother, a mother, and a friend."

Gerdes said harmonic modulation should be able to put at least 10 megabytes of data onto a conventional 5¼-inch floppy without special head-positioning mechanisms in the drive. Other systems promise 10 megabytes on a 5¼-inch floppy (notably the one Konica showed at COMDEX last November), but they do it by using a more precise head-positioning mechanism (which increases the cost of the drive) to cram more tracks per inch onto the disk. Harmonic modulation works by getting more bits onto each track.

Since harmonic modulation can be combined with AM and FM in the same disk drive, Gerdes said, it should be possible to increase the capacity of a drive considerably by using AM to lay down servo tracks (guide paths for the head) to put even more tracks per inch onto the disk.

Gerdes told *Microbytes Daily* that Audel is planning to build a disk drive using harmonic modulation by the second quarter of this year. He said that the company is negotiating with several firms about licensing the technology.

Warp Speed, Mr. Sulu: Experimental Computer Calculates 100 MIPS; Drives a Car, Too

An experimental parallel-processing computer developed at Carnegie Mellon University (Pittsburgh) has proved capable of, among other things, "intelligently" driving a car. By calculating distances and directions based on video input from cameras attached to the front of the vehicle, the computer can make decisions about whether to increase or decrease speed and which way to turn to avoid obstacles. The computer, called Warp (short for "warp speed" from *Star Trek*), gets its nickname not from the speed at which it travels, about 1 mph, but from the speed at which it calculates. According to professor H. T. Kung, the computer makes more than 100 million calculations per second. Within the next two weeks, a specially designed van under Warp control will be tested at

speeds of up to 35 mph.

The Warp computer uses 10 Weitek floating-point processors working in parallel to achieve such amazingly high performance, which Kung said is about 100 times faster than a "normal" computer. Even though the initial testing has been in the area of vehicular control (the Department of Defense is funding the \$10 million project), the computer has shown surprising test results in the areas of signal processing and magnetic retina imaging.

In addition to DOD projects, Kung said he hopes to develop vehicular assistance applications for handicapped drivers. There are currently only two prototypes of the Warp in existence, but General Electric has signed a contract to manufacture nine more.

Philips Shows CD-I Images; Some Oppose Closed Architecture, Others Plan Products

At a recent conference sponsored by the Institute for Graphic Communication (Boston), Philips International showed for the first time to the public a videotape of CD-I (compact disc-interactive) images generated by prototype hardware. The tape demonstrated the technology's ability to handle several different types of video—including animation and limited motion—and three levels of audio quality. The demo was designed to interest possible software developers in creating products for the new format.

Although first announced in March 1985, CD-I is still a long way from the consumer marketplace. Richard Bruno, manager of the CD-I technical staff at Philips's laboratories in Eindhoven, The Netherlands, and editor of the CD-I specs document called the

"Green Book," said that prototypes of the drive will be available in January 1988; at a conference in October, Bruno had said shipments to consumers would begin by the end of 1987. Philips executives now see 1990 as the breakthrough year for CD-I technology.

CD-I builds on already-developed compact audio disk and CD-ROM products. It's an interactive entertainment and education tool that combines a CD-ROM drive with audio and video processors, a 68000-series microprocessor, and a real-time operating system.

At the conference, representatives of Apple Computer (Cupertino, CA) said Apple is withholding support for the CD-I format. The company said its newest Apple, the IIGS, would be a better choice for audio and video pro-

continued

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grams for the consumer market. Apple officials had serious questions about the proprietary chip set selected by Philips for its CD-I products.

CP/M developer Gary Kildall, president of KnowledgeSet (Monterey, CA), has been critical of the closed architecture employed by Philips. He

said he'd like to be able to buy the chip set and use it in a hybrid system. Kildall's company develops software for CD-ROM applications.

Several companies have announced intentions to develop CD-I products, but they're at least a year from market. Spinnaker (Cambridge, MA), Broder-

bund (San Rafael, CA), and Aegis Development (Santa Monica, CA) are among the firms to make public commitments. Aegis said it has begun work on its first CD-I title, *20,000 Leagues Under the Sea*, but that release will depend on arrival of hardware and development tools from Philips.

Seagate to Start Building 3½-inch Hard Disk Drives

Seagate Technology (Scotts Valley, CA) said it will start producing high-capacity 3½-inch disk drives later this year. The hard disk drives will have an average access time of less than 30 milliseconds, the company said, and will incorporate sputtered thin-film media and open-loop rotary stepper actuators.

The new drives will come with embedded controllers and SCSI interface or with the ST412 interface using MFM (modified frequency modulation) or RLL (run-length limited) recording.

SCSI-equipped models will be available with formatted capacities of 30 and 45 megabytes, as will two models

using RLL recording. Two units that use the ST412/MFM interface will have formatted capacities of 20 and 30 megabytes. Evaluation drives will be available during the second quarter, the company said. Prices, in OEM quantities of 500, will run from \$495 to \$695, Seagate said.

Company Proposes Format Standard for Optical Disks

Guidelines defining the format standard for 5¼-inch optical disks have been proposed to the American National Standards Institute by Optotech Inc. (Colorado Springs, CO), a manufacturer of optical drives. Optotech claims that, unlike other recent format proposals submitted to ANSI, its proposal is the only one that fully specifies how to encode and decode information on disk, as well as the only one to couple track format with an error-

correction code. According to Optotech representatives, both data encoding and decoding must be specified to ensure that disks are completely interchangeable.

The disk format standards proposed by Optotech include a 512-byte sector size, continuous/composite grooves for tracking, and a two-of-seven encoding scheme with resynch fields. Additionally, the proposal provides for a data banding technique in which the

disk is banded into regions of identical angular velocities so that disk capacity approaches that of constant linear density without the seek-time penalties usually associated with constant linear velocity.

A previous proposal presented to ANSI recommended a sampled-servo format based around a disk pitted in a specific pattern to guide the head, as opposed to the continuous groove suggested by Optotech.

Researchers Use ICs to Repair Severed Nerves

Advances in microelectronics and microsurgery may make it possible for accident victims to regain almost complete functionality of reattached limbs, according to medical researchers at the Stanford University Medical Center. Currently, most reattached appendages provide about 5 percent to 20 percent functionality, say Drs. Morton Grosser and Joseph Rosen.

Because there are more than 2000 individual axons (the nerve fibers that make up the nerve), it is virtually impossible to reconnect them using microsurgery. Consequently, signals to and from the brain cannot correctly get past the reattached nerve union once a severed nerve is sewn back together.

However, Rosen and Grosser have

found that by drilling holes into the silicon of a tiny integrated circuit and implanting that unpowered switchboard between the two ends of the severed nerve, axons will grow, over a period of three to nine months, into the holes. The chip is then connected to an external computer that scans nerve signals above and below the integrated circuit, thereby enabling the surgeons to correctly identify the two halves of the individual axons on a computer screen. The computer is then used to program the chip to make the appropriate "connections." Exact connection of every axon isn't necessary because the nervous system simultaneously transmits some information.

After two years of experimentation, Rosen and Grosser have grown

axons of small mammals into the chips, but they stress that implanting the chips in humans is several years away. "What we eventually hope to do," says Grosser, "is hard-wire a person permanently."

Theoretically, the doctors will be able to, for example, connect a nonambulatory rat to a computer, punch a few keys on the keyboard, and the rat will be able to run around.

The most difficult part of the process has been precisely laser-drilling the 8-micron diameter holes into the 1-millimeter by 1.5-millimeter silicon chips.

Grosser says that once they "get a genuine direct access to the peripheral nervous system, there is no end to what can be accomplished."

TECHNOLOGY NEWS WANTED. *The news staff at BYTE is always interested in hearing about new technological and scientific developments that might have an impact on microcomputers and the people who use them. We also want to keep track of innovative uses of that technology. If you know of advances or projects that involve research relevant to microcomputing and want to share that information, please contact us. Call the Microbytes staff at (603) 924-9281, send mail on BIX to Microbytes, or write to us at One Phoenix Mill Lane, Peterborough, NH 03458.*

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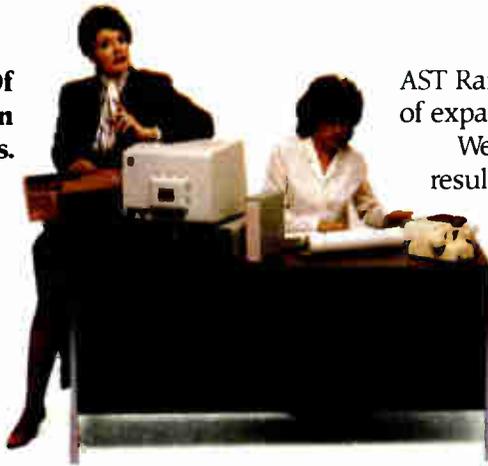
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LETTERS

Spatial Case

The Great Language Debate, which seems to be raging on BIX and in your magazine, has prompted me to write. J. David Reynolds Jr. ("The Ideal Programming Language," January Letters) comments for the promotion of an advanced programming environment. However, as sophisticated as it sounds, it is not more than a new combination of old ideas. While it will make programming easier, it is not a major step forward.

Mr. Reynolds's proposal, like many others, is based on the idea that people think best in languages. This is not true. To begin with, languages are one-dimensional; they consist of one symbol followed by another. The real world consists of four dimensions: three of space and one of time. Mankind has evolved a remarkable visual-manipulative system to cope with it. An advanced method of programming a computer would exploit this natural system. With this system, you would not tell the computer what to do, you would show it.

Everything in the computer is an object (and I do mean everything—from bits to the operating system itself). Moreover, a compound object may be taken apart and its components viewed. Associated with each object is a control panel that may be invoked at any time by the user. But the thing that will make this system work is the splicing editor.

The splicing editor is a program that allows you to change any sequence of actions. You can view the action at full speed, slow motion, or by single-stepping, forward or backward. Like a film editor, you could splice out any sequence you do not want and replace it with one of your own. It will have the functionality of any programming language with features that include loops, conditions, and sub-sequences. The editor and the control panels will give users two of the things they want most from a computer: control and confidence.

Confidence in the programs is increased with this system because the user can see the actions as they take place (when running in slow motion, of course). If the program takes the same actions the user would do the task, his confidence is increased.

This proposal is different from any other in that it intends to use a different

part of the brain. Previous systems use the language centers while this would use the visual-manipulative centers. Nor is the above complete. Space and time have limited my discussion to only the major points.

Shawn Corey
Winchester, Ontario, Canada

Relax, Redux

Having used relaxation methods almost three decades ago for heat-conduction calculations, I read Gregg Williams's article, "An Introduction to Relaxation Methods" (January), with enjoyment and a feeling of nostalgia. However, to promote the classical relaxation algorithm as a useful numerical technique in this day of high-speed computers is misleading.

Relaxation was used because it is efficient for hand calculation. It has two advantages: First, it reduces the computation effort, especially with block-relaxation and over-relaxation techniques. Second, it is very forgiving if mistakes are made. The residuals can always be recalculated at any step. This feature also allowed the "computer" to make quick approximate calculations knowing that once the residuals were approximately correct, they could be recalculated and the process continued with appropriate accuracy and precision.

One aspect that makes the classical relaxation method inappropriate for machine calculation is the step requiring that the largest residual be found. The human eye and brain can easily find the largest residual by quickly scanning the network of nodes. The time needed by a machine to search for the largest residual is much better spent on performing "relaxation" computations on all nodes in succession and repeating the calculations in an iterative manner, such as with the Jacobi or Gauss-Seidel methods. In fact, these iterative methods are sometimes called "relaxation" methods. The convergence criteria are known and there are techniques that can be used to speed up convergence. The iterative methods are easily programmed.

Another problem with adapting the classical relaxation method to machine computation is just keeping track of which relaxation block applied to which nodes. It's an accounting problem that carries a large computational overhead.

With advances in direct (i.e., noniterative) methods for solving large systems of equations, the generally preferred methods in heat transfer and other field-type problems are the finite-element method and boundary-element method.

I believe your readers would have benefited more from the article if Mr. Williams had discussed some of the programming problems that are encountered with the classical relaxation method even if it is no longer used in any serious way. Also, there are some interesting and useful principles that can be learned by playing with the relaxation method. It is very instructive to watch a mesh "relax" as the computations proceed. In this respect, we "old-timers" have an advantage in that we were forced to do such extensive computations by hand.

George E. Zinsmeister
Amherst, MA

Your recent article on relaxation methods, aka finite difference, underscores the use of an alternative solution technique available to the technical professional. Our company has taken the method one step further by integrating finite differences with Lotus 1-2-3. By assigning nodes or elements as spreadsheet cells, models can be built and analyses conducted quickly using the "what if" capability of the spreadsheet.

Binary Engineering has been applying these techniques to a wide variety of problems, including most of those mentioned in your article. Our clients include Ford, Boeing, AT&T, GE, Grumman, Norton, and various DOD/military organizations. We submit that the method is excellent for use in parametric studies where engineers need to bound a problem and test various options. Accuracies are dependent on the size of the model built

continued

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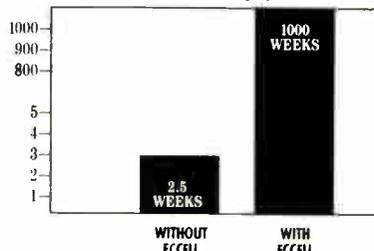
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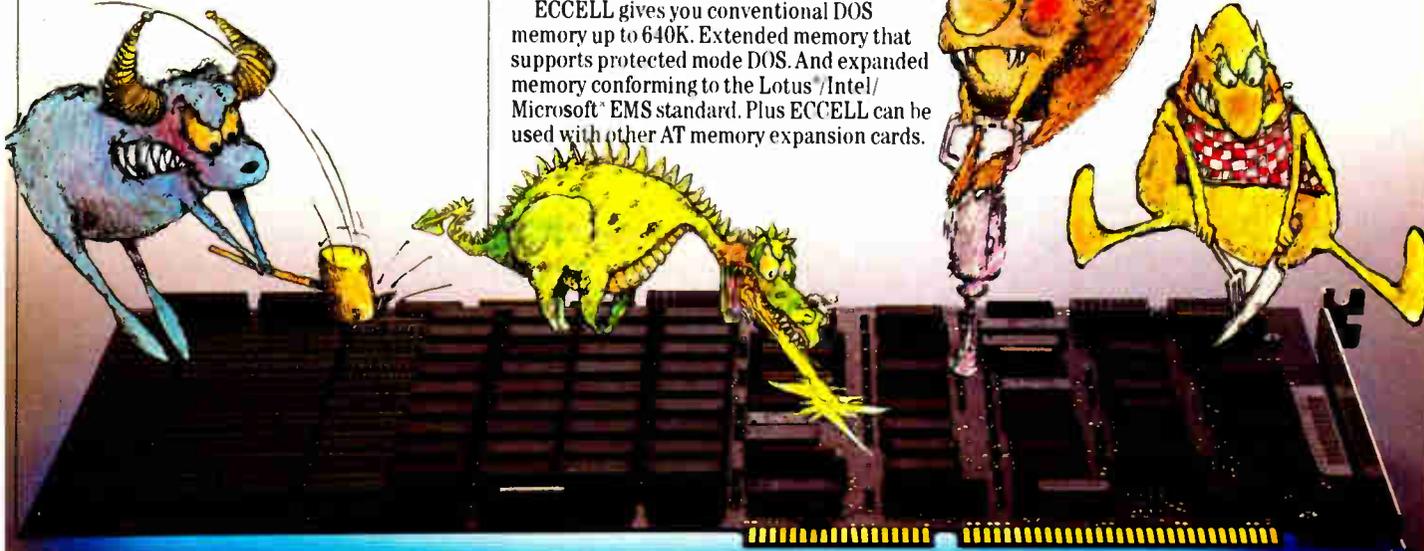
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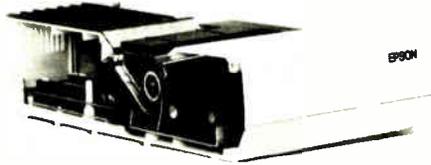


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but are generally well within acceptable tolerances.

Furthermore, spreadsheet-based finite-difference methods offer a logical option to finite-element methods. In general, with both methods available, engineers can now choose a solution method most appropriate to the size and complexity of the problem as well as to their own computer expertise.

Please continue to offer general articles of interest to engineers and scientists.

Kevin Shea
President

Binary Engineering
Holden, MA

Simple PAL Patch

Thank you for a fascinating series of articles on programmable hardware in your January issue. It is good to see its virtues more widely known.

One of the patches that Trevor G. Marshall describes in his article, "PALs Simplify Complex Circuits," seems unnecessarily complicated, however. He wants to generate the signal T1 that is asserted "when ADS pulses and CTTL is low . . . until CTTL goes high" and uses a solution that involves tristating the T1 pin when CTTL is high and using a pull-up resistor. The whole thing can be done more elegantly with the equation

$$IF (VCC) T1 = ADS \cdot /CTTL + T1 \cdot /CTTL$$

Although this equation turns T1 off as soon as CTTL goes high, the specified hold time for inputs to the clocked latches (such as RFIOI and HOLD86I, where T1 is used) is zero nanoseconds after the rising edge of the clock (CTTL); and T1 will take *at least* zero nanoseconds to change state after the clock rises. This modification makes for a more elegant design and, more importantly, saves a discrete resistor, thus reducing board costs.

Martin Kochanski
Speldhurst, Kent, U.K.

3-D Graphics

Much of my recent programming has been with real-time graphics applications and I was elated when I found a fast square-root routine in a BYTE article, "Real-Time 3-D Graphics for Microcomputers," by Marcus Newton (September 1984). Although I had a problem with divide overflow when the argument in DX:AX exceeded 4600:0000h, this was solved by modifying the algorithm to compute a better initial guess.

Then I found another algorithm in an assembly language textbook for the IBM

continued

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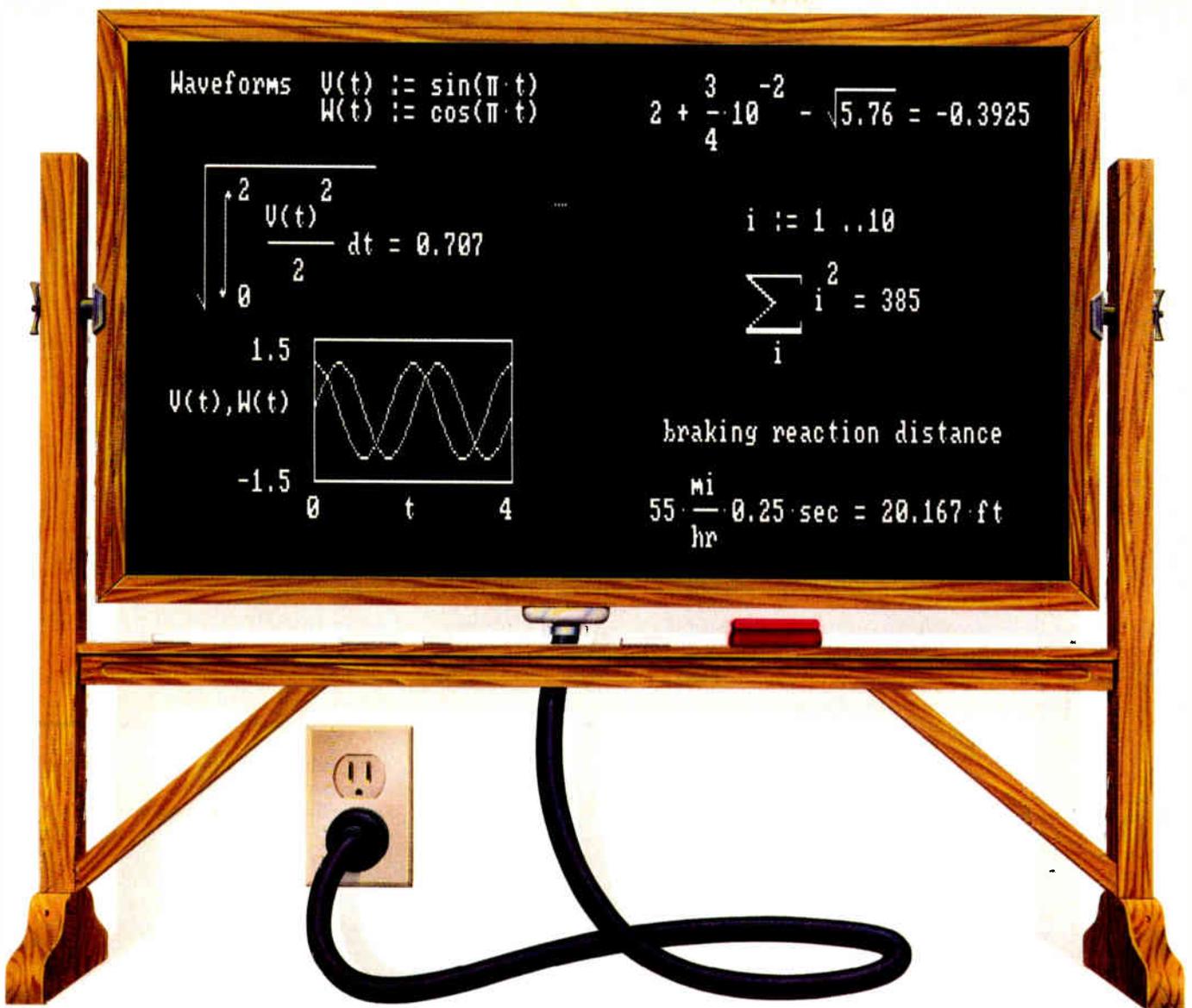
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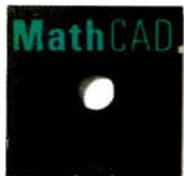
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LETTERS

Listing 1

```
;The argument is placed in DX:AX.
;The square root is returned in SI
```

ISQRT PROC NEAR

```

PUSH    AX
PUSH    BP
PUSH    CX
PUSH    DI
PUSH    DX      ;Note 1
PUSH    SI
XOR     DI,DI
XOR     SI,SI
XOR     BP,BP
MOV     CX,16
GET_DIGIT:
SHL     SI,1
MOV     DI,SI
SHL     DI,1
INC     DI
SHL     BX,1    ;consider
SHL     DX,1    ;BX:DX:AX
ADC     BX,BP   ;as one 48-
SHL     AX,1    ;bit register
```

```

ADC     BX,BP   ;and shift it
SHL     BX,1    ;left 2 bits
SHL     DX,1
ADC     BX,BP
SHL     AX,1
ADC     DX,BP
CMP     DI,BX
JA      NO__DIGIT:
SUB     BX,DI
INC     SI
NO__DIGIT:
LOOP   GET__DIGIT
POP     SI
POP     DX      ;Note 1
POP     DI
POP     CX
POP     BP
POP     AX      ;Note 1
RET
```

ISQRT ENDP

;Note 1 - Optional if argument needs to be saved.

370. This algorithm was easily converted to 8088 code and, at first glance, promised to be twice as fast as Mr. Newton's, since it consisted of short, fast instructions and with no multiply or divide instructions. But, before I could write the code and compare benchmarks, I came across "C Versus Assembly — C Plus Assembly" by Tom Hogan (BYTE's *Inside the IBM PCs*, Fall 1986). He reminded me that fast instructions are not fast if they are not in the instruction queue. This is amply demonstrated in the integer square-root routine in listing 1, which was run for 60,000 iterations and compared with Mr. Newton's algorithm.

Newton's algorithm	25.5 seconds
Listing 1 (calculated)	10.6 seconds
Listing 1 (actual)	39.1 seconds

The calculated value was based on the execution times given for each instruction and a CPU clock of 4.77 megahertz. It did not take into account the time required to fetch instructions into a queue that was quickly emptied by fast instructions. Not only was this algorithm slower than Mr. Newton's, it took four times as long to execute as the preliminary calculations indicated.

It is these little gems of wisdom provided by BYTE and its writers that I find so useful and interesting.

Douglas R. Simpson
Virginia Beach, VA

PAL Project

I wish to compliment you on the January issue. The emphasis on hardware was

quite welcome. I especially appreciated the construction article by Robert A. Freedman, "A PAL Programmer." This excellent construction project fills a gap not served by any commercial product to my knowledge. Though I have actively searched, I have yet to find a vendor offering a truly low-cost general-purpose PAL programmer such as this.

As a design consultant, I have frequently used PALs and know from my professional associations that these parts have revolutionized logic design. PALs are excellent garbage collectors, reducing several square inches of random logic to a single chip. In addition, a designer achieves flexibility for design revision with these parts. However, PALs and programmable logic in general are little used by hobbyists because no low-cost programmer was previously available. Your readers have been well served by Mr. Freedman's article. Thanks.

Steven H. Leibson
Denver, CO

Should We Hide...?

I have seldom been moved to write to a magazine in response to an article and, most often, it has been in praise. Sadly, my letter to you must be an expression of outrage at your publication of the article "Local Effects of Nuclear Weapons," by John R. Fanchi (December 1986).

Although we have been living under the threat of nuclear holocaust for a generation and more, it is a mistake to think that this is a normal state, that one can

continued

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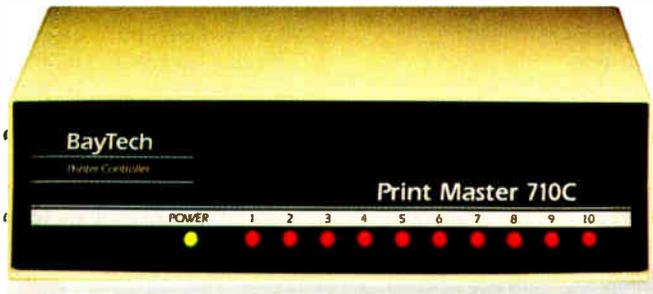
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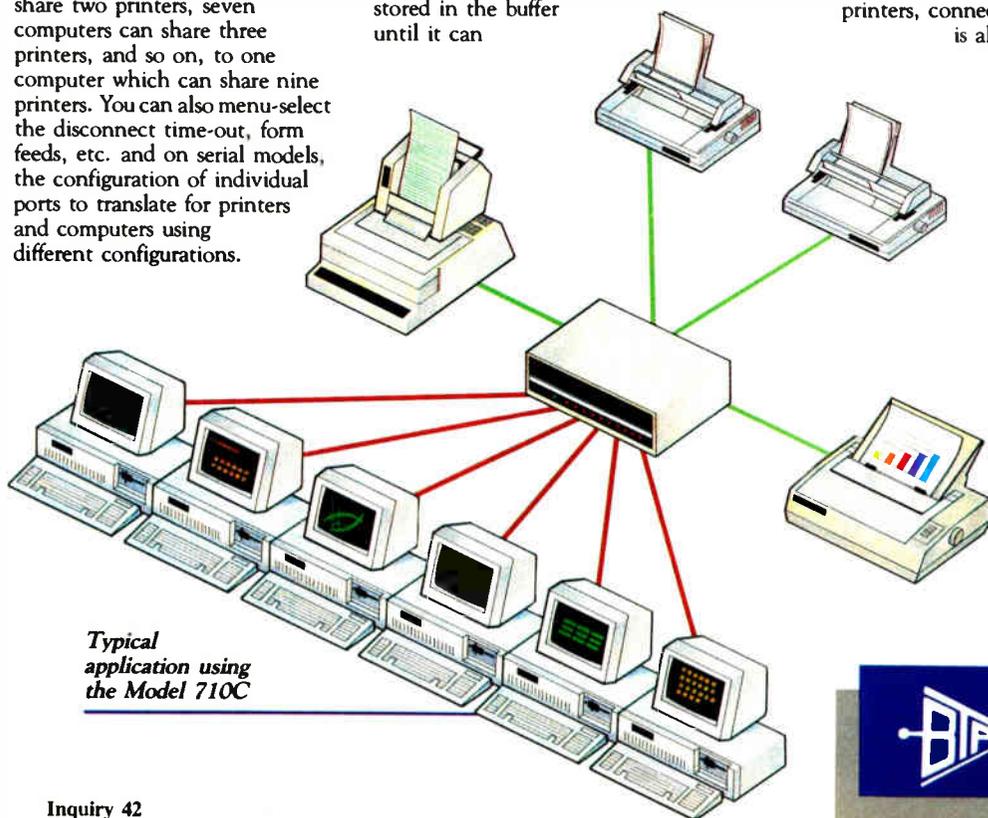
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make contingencies against it as against a fire or flood. It is especially mistaken to espouse this view in a respected, widely read publication.

The present leaders of our country believe that we can survive a "limited nuclear war" and seem perfectly willing to test this supposition should the opportunity arise. If we demonstrate an acceptance of this situation through our popular media, we might well find ourselves engaged in the Big Nightmare one of these days.

Please, think about the import of Mr.

Fanchi's article. It is fine to use one's expertise in programming to spin fanciful structures of logic based on the wildest premises, to simulate reality without fear of the consequences. It is quite another to publish them willy-nilly. Conjecture has a nasty way of becoming reality. Don't toy with the bomb, gentlemen.

Mark W. Pemburn
No address given

...Or Should We Seek?

John R. Fanchi, in his presentation of nuclear effects models, echoes a proposal

made at a recent European Physical Society meeting on nuclear winter. It was suggested there that a package of such models be developed for educational purposes in order to raise general awareness of the true nature of nuclear war and its aftermath.

May I correct one point concerning nuclear winter? Although there are a handful of vociferous critics, the atmospheric community is united in its conclusion that the threat of nuclear winter is genuine. Climate prediction on the nuclear aftermath is not like forecasting tomorrow's weather. There are many, many uncertainties. Nevertheless, as the Steering Committee of the authoritative SCOPE ENUWAR review has stated, "Because of the possibility of a tragedy of unprecedented dimension, any disposition to minimize or ignore the widespread environmental effects of nuclear war would be a fundamental disservice to the future of global civilization."

If anyone is interested in helping to compile and distribute a set of nuclear programs, I can be contacted by snail mail here at the University, through Sciencenet (identifier M.KELLY/OMNET), via ARPANET or similar on the U.K. academic network JANET (identifier F030@UEA.CPC865), or on GREENNET (identifier CRU-NORWICH).

P.M. Kelly
Climatic Research Unit
University of East Anglia
Norwich NR4 7TJ, U.K.

Dumb Disk Drives

A couple of points:

First, why should your main processor have to operate the disk drive? Why aren't disk drives built smart? I should be able to plug any disk drive into any computer, secure in the knowledge that a standard set of instructions sent to the disk drive port will enable me to receive data from and send data to the drive.

In fact, from the main processor's point of view, a drive is merely a chunk of intelligent "external memory." Let's call the commands that communicate with such memories "External Memory Management," or EMM. Then, all operating systems would have the same EMM commands: READ/WRITE/ERASE file.type, LOCK/UNLOCK file, MAKE/CHANGE directory, CATALOG/\$name/\$name.... SHOW space on disk, and so on. The drive would have a standard set of messages, such as one warning of insufficient space to store a file, or one indicating that the requested file is in a directory other than the current one, and so on. The operating system could automatically

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append system-specific file-type extensions to certain filenames; but apart from that, no system-specific considerations apply.

Drives could have buffers built in for high-speed data transfer to relieve the CPU of waiting time. A sophisticated drive might respond to an enhanced EMM and READ/WRITE data into this buffer and automatically rewrite files as time permits, thus reducing the chance of data loss.

Drives could be built to conform to the minimum EMM command set, or provide (standard) enhancements to the set. Users could add any drives to their system or replace any drive with any other drive. Drives could be built to read any existing disk format so that the actual format of your disk would no longer matter. (Commodore's 1571 reads three disk formats: Commodore's single-sided and double-sided formats, and CP/M. It is a smart drive.)

Finally, since the system only knows how to communicate via EMM; it doesn't matter what form external memory takes physically. This would simplify the installation of RAM disks and would provide automatic compatibility with any future mass-memory technologies.

Am I just dreaming, or is this a feasible (and useful) idea?

Second, regarding Fred Gruenberger's surprise that the lowly 6502 may run some programs *faster* than the 8088 ("Comparing Clock Rates," November 1986 Letters): He seems to suffer from at least one of two pervasive fallacies: that older/smaller/slower means worse; and that "professional" means superior.

"Better" and "worse" are not absolute categories but depend on your requirements. I use a Commodore 64 at home and an IBM PC XT at work. In practical terms (how much work you can get done in a given time), I find no difference whatever. The PC has faster hardware but the programs written for it are clumsier and more complicated in actual use (I use Lotus 1-2-3 and WordPerfect). So it comes to the same thing. Granted, my friend, who has access to hundreds of kilobytes at once from his program, needs the extra memory of the PC. But most people don't. Like my employer, they bought the PC not because it was better, but because it was "professional."

"Professional" just means that you get paid for it. In a mature industry, that usually implies that you are worth what you are paid. This is emphatically *not*

true in the computer industry. My "professional" programs cost 5 to 10 times as much as my home-computer programs. They do not do 5 to 10 times as much work or function 5 to 10 times faster. In fact, while overall they show some superiority over the cheaper (or free) programs, they also display some odd deficiencies. My \$70 word processor for the C-64 comes with over forty printer drivers. WordPerfect comes with four, which I'm supposed to adapt to my particular printer. For \$300, I think I should get more printer drivers, not fewer.

Wolf Kirchmeir
Blind River, Ontario, Canada

FIX

Acta Price

I appreciate Ezra Shapiro's review of my program, Acta, in his February Applications Only column. However, I'd like to point out to readers that the retail price is \$59.95, not \$79.95.

David Dunham
Maitreya Design
Goleta, CA

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BOB STANTON HAD A GREAT IDEA. AN HOUR LATER HE WAS TESTING IT.

Appointments. Everybody takes them — dentists, auto-body shops, dance instructors. And lots of computer applications need appointment screens.

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Bob set up dimensioned screen variables for the days of the month and a screen pointer for selecting a date, and he was done. Then Screener generated the code.

Then Bob drew the appointments window, built an appointment file, filled in the connecting code and tested it — ONE HOUR AFTER HE STARTED!

Testing was a breeze. Screener doesn't just write code, it compiles your source, displays a screen, gets the changes, then replaces the old code in your program.

So here are Bob's appointment screens. You can see the source listing to the right. We marked all the code Screener wrote for him.



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WHAT'S NEW

Microsoft Releases CD-ROM Reference

Microsoft has announced Bookshelf, a CD-ROM reference library that contains 10 common reference tools including *The American Heritage Dictionary*, *Roget's Thesaurus*, *The Chicago Manual of Style*, and a U.S. zip code directory. The memory-resident program can be implemented while you are using your word processor or other software.

Bookshelf runs on IBM PCs or compatibles with at least 640K bytes of RAM or 512K with a hard disk drive. You also need a CD-ROM drive and MS-DOS CD-ROM extensions.

Price: \$295.

Contact: Microsoft Corp., P.O. Box 97017, Redmond, WA 98073-9717, (206) 882-8080.

Inquiry 576.

Tektronix's PC Graphics Products

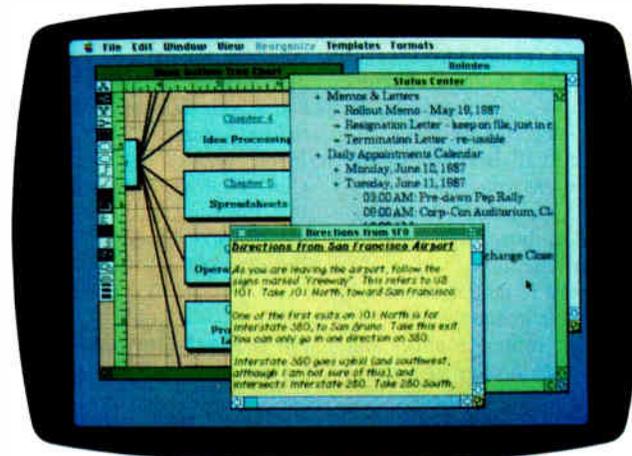
Tektronix has entered the advanced PC graphics market with a graphics coprocessor card, a high-resolution monitor, and two terminal-emulation software packages.

The Plot 10 PC4100 graphics coprocessor board uses the TI TMS34010 Graphics System Processor chip. Memory built into the board includes a frame buffer and 1 megabyte of general-purpose RAM. The PC4100 provides resolution of 640 by 480 pixels and can emulate both the IBM EGA and CGA for compatibility with existing software.

The 13-inch Tektronix Multiple-Line-Rate color graphics monitor has a nearly flat cylindrical surface with a



Bookshelf, a CD-ROM reference library.



More 1.1c takes advantage of the Mac II's color capabilities.

silica glass coating to reduce glare. The raster display monitor has a 60-Hz noninterlaced refresh rate and a viewing area of 240 by 180 mm.

The Plot 10 PC-07 terminal-emulation package emulates selected capabilities of the Tektronix 4107 color graphics terminal. It also provides Tektronix features such as segments, true zoom and pan, viewports, and DEC VT-100 compatibility.

The Plot 10 PC-05 terminal-emulation package adds selected 4105 terminal capabilities to the IBM PC and compatibles. Included are points, vectors, filled panels, and graph text. In text mode, it will also emulate the DEC VT-100.

Price: \$1800 (PC4100 board); \$950 (graphics monitor); \$495 (Plot 10 PC-05 software); \$995 (Plot 10 PC-07 software).

Contact: Tektronix Inc., P.O. Box 500, Beaverton, OR 97077, (503) 644-0161.

Inquiry 577.

Macintosh II Color Supported by More 1.1c

Living Videotext has announced that version 1.1c of More, an integrated idea processor/presenter, takes advantage of the spectrum of colors available on Apple's Macintosh II.

With More 1.1c you can create and manipulate text in standard outline form, as tree charts, or as bullet charts.

In outline form the program can color screen elements such as the background, title bars, scroll bars, and scroll boxes. With tree charts, you can color all the lines surrounding and joining the boxes of the chart or add three-dimensional shading on the boxes, the area inside the boxes, and the text within.

More offers commands, such as undo, that simplify the text-creation process. You can choose from a variety of text styles including italic, boldface, and shadow. An outline database disk, based on General Information's address and telephone number directory, is also included.

Price: \$295.

Contact: Living Videotext Inc., 2432 Charleston Rd., Mountain View, CA 94043, (415) 964-6300.

Inquiry 578.

Compaq Introduces Smaller "Transportable"

Compaq's Portable III isn't a laptop, but with a weight of 20 pounds and a size approximating that of a large shoebox, it's the company's smallest computer yet. The PC AT-compatible Portable III is based on an 80286

continued

running at 12 MHz (switchable to 6 MHz). It comes standard with 640K bytes of RAM (expandable to 6.6 megabytes) and a single 1.2-megabyte 5¼-inch floppy disk drive. Either a 20- or 40-megabyte hard disk drive is optional with a claimed access time of less than 30 ms.

The Portable III has a red-orange gas-plasma display with a resolution of 640 by 400 pixels. It includes a dual-mode display adapter that will display both high-resolution text and CGA-style graphics. On the rear panel are serial and parallel ports and a connector for an external RGB monitor. The 84-key keyboard is detachable and has function keys arranged along the top.

Two IBM-style expansion slots located inside the unit are taken up by the modem and memory expansion, if any. A thin expansion unit attached to the back enables you to add two more expansion slots to the system. The Portable III has a 145-watt power supply and must be plugged into a standard AC outlet. Options include memory expansion, an internal Hayes-compatible modem, a desktop pedestal, and a carrying case.

Price: \$3999 with a floppy disk drive; \$4999 with a 20-megabyte hard disk; \$5799 with a 40-megabyte hard disk.

Contact: Compaq Computer Corp., 20555 FM 149, Houston, TX 77070, (800) 231-0900; in Texas, (713) 370-0670.

Inquiry 579.

Designing Printed Circuit Boards

A CAD program for designing printed circuit boards has been announced by CAD Software. PADS-PCB runs on the IBM PC AT and XT and enables you to design boards of up to 32 by 32 inches and up to 30 layers. The program supports surface-mounted devices, including the ability to design type 1, 2, and 3 boards with components on the top and bot-



The HP LaserJet II: more features, lower price.

tom layers. A fine-line design capability lets you place up to three tracks between integrated-circuit component pads. Using the Expanded Memory option (\$250), you can design boards with more than 200 integrated circuits.

PADS-PCB uses the Expanded Memory capability provided by the Lotus-Intel-Microsoft specification, enabling you to design boards with up to 400 equivalent 14-pin integrated circuits.

The ASCII editor within the program lets you enter manually prepared schematics as well as those from logic capture systems.

You can route connections with either interactive or automatic routing routines and place tracks on any grid from 1 to 250 mils. You can display tracks or pads at a center line width or filled. Sixteen colors are available for distinguishing between items and layers.

A Design Rule Check checks the entire board or a window on the board for air-gap spacing violations. A two-dimensional drafting capability enables you to generate engineering and manufacturing documentation. An engineering change order routine is included for you to use in incorporating changes such as deleting components or connections, adding components or connections, disconnecting pins, changing parts or part names, and so

on. A parts library, also included, consists of about 1000 TTL and CMOS parts and their descriptions. You can also enter your own parts into the library.

The program runs on IBM PC XTs and ATs with at least 512K or 640K bytes of RAM. You also need an EGA, a color monitor, and a mouse. The company recommends using a 20-megabyte hard disk drive and a wide-carriage dot-matrix printer.

Price: \$975.

Contact: CAD Software Inc., P.O. Box 1142, Littleton, MA 01460, (617) 486-9521.

Inquiry 580.

HP's Next-Generation LaserJet

Hewlett-Packard has introduced the HP LaserJet Series II printer, a new model with a number of enhanced performance features over the original LaserJet, but with a price less than that of the original.

The Series II comes with 512K bytes of RAM, and a variety of memory upgrades are available including a one-megabyte board for full-page 300-dpi graphics. Also available are 2-megabyte and 4-megabyte boards. The unit comes standard with both an RS-232C serial port and a Centronics-compatible parallel port.

Weighing in at about 50 pounds, the Series II is 30 percent lighter than previous

models and has a new paper path that delivers documents face down in the correct order. The input bin can hold 200 sheets, and the output bin holds 100 sheets. The printer also has two font-cartridge slots, and all existing font cartridges are compatible with the Series II. The printer comes with six different fonts.

Price: \$2495. Memory expansion: \$495 (1 megabyte); \$995 (2 megabytes); \$1995 (4 megabytes).

Contact: Hewlett-Packard Company, 1820 Embarcadero Rd., Palo Alto, CA 94303, (800) 367-4472.

Inquiry 581.

Amiga Communications

Aegis Development has announced Diga!, a telecommunications program for the Amiga. Diga!, which uses the standard Amiga window/menu environment, supports batch-file XMODEM and Kermit file protocols as well as CompuServe Protocol B and MIDI (all with several file-transfer options).

Two Amigas running Diga! can send text messages to each other while doing file transfers using the program's Doubletalk option. Diga! can do DEC VT52 and VT100 emulations, and other terminal emulations are possible through a custom mode. The program also includes a sophisticated scripting language, a menu of options available from the Amiga Help key, multiple books of telephone and address information, 10 macro keys, and the ability to allow users with the correct passwords to control the Amiga from a remote terminal.

Price: \$79.95.

Contact: Aegis Development Inc., 2210 Wilshire Blvd., Suite 277, Santa Monica, CA 90403, (213) 306-0735.

Inquiry 582.

continued

80386

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Inquiry 270 for End-Users. Inquiry 271 for DEALERS ONLY.

World Radio History

Mapping on the PC

Atlas*Graphics is a menu-driven graphics tool capable of geographic data and decision analysis. It enables you to combine data and boundary files into a geographic file for producing maps for analysis and presentation.

Design capabilities let you choose from 16 colors and 8 fonts for the text and icons you can enter into your maps. You can draw points, lines, and polygons on the maps, draw circles around any point, zoom in on any area, and label areas. In addition, you can import data from ASCII and DIF files or enter data directly.

When you want to display data on a map, you can select from 26 predefined hatch patterns. Output devices supported include plotters, printers, and slide makers.

Also included in the program are boundary and data files, which include census, demographic, and statistical information.

Atlas*Graphics runs on IBM PCs, XT's, AT's, and compatibles with at least 512K bytes of RAM, a color or monochrome graphics board and monitor, and two floppy disk drives.

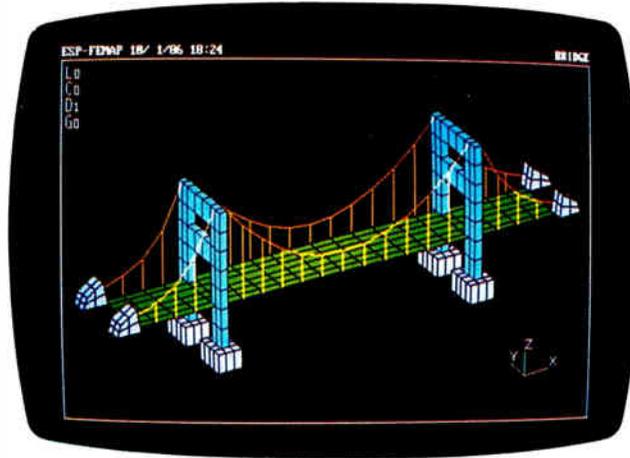
Price: \$450.

Contact: STSC Inc., 2115 East Jefferson St., Rockville, MD 20852, (301) 984-5000.
Inquiry 583.

Apple Upgrades IIe

Apple has rolled out an upgraded version of its IIe. The major difference from the original IIe is that the keyboard has been redesigned to be functionally equivalent to the keyboard of an Apple IIGS. The new keyboard incorporates an 18-key numeric keypad and has its two programmable function keys, cursor-control keys, and alphanumeric keys in a QWERTY layout.

The new IIe has also gone through a color change. It's



Develop 2-D and 3-D finite-element models with FEMAP.

being shipped in Apple's platinum (light gray) color. Also included is a newly revised owner's manual, a guide to AppleSoft BASIC, and two double-sided training disks.

Finally, the new IIe is shipped with the Apple 80-column upgrade card already installed.

Price: \$829.

Contact: Apple Computer Inc., 20525 Mariani Ave., Cupertino, CA 95014, (408) 996-1010.

Inquiry 584.

Finite-Element Modeling with FEMAP

FEMAP lets you develop and verify two- and three-dimensional finite-element models. The program includes read and write interfaces to MSC/PAL and MSC/NASTRAN.

An element library includes line, plane, and solid elements. Applied loads consist of nodal forces and moments, gravity, element pressures, line loads, centripetal accelerations, and enforced displacements and accelerations. Constraints consist of applied boundary conditions and permanent constraints at the node level.

FEMAP enables you to per-

form three-dimensional color-shaded hidden-line and wireframe plotting. You can align the view with any coordinate system, zoom, magnify, autoscale, pan, and center. You can also rotate the three-dimensional viewing angle, and you have the choice of plotting elements as lines or filled objects.

Also included is a multi-level coordinate system for creating geometry. An on-line calculator and file interface enable you to customize the program and create your own modeling routines.

The program runs on IBM PCs, XT's, AT's, and compatibles with 512K RAM, MS-DOS or PC-DOS 2.0 or higher, a 10-megabyte hard disk drive, and a monitor with a CGA or EGA.

Price: \$995.

Contact: Enterprise Software Products Inc., P.O. Box 264, Harleysville, PA 19438, (215) 256-1829.

Inquiry 585.

AppleShare File Server

Apple Computer's AppleShare file server enables groups to share information over the AppleTalk network. It's the first product to incorporate Apple's published standard for the AppleTalk Filing Protocol (AFP), Apple reports.

The server offers access to up to 25 users from anywhere on the AppleTalk network. You can run additional network services, such as electronic mail. By adding disks you can increase the storage capacity to hundreds of megabytes of on-line storage. You can add additional AppleShare file servers to a network, as well as connect to AppleTalk networks through bridges, and user access remains transparent.

To run the file server you need a dedicated Macintosh Plus and a hard disk as the Server. AppleTalk Personal Network cables and connectors for each workstation and the server are also necessary. Macs with at least 512K bytes of RAM can function as workstations on the network.

Price: \$799.

Contact: Apple Computer Inc., 20525 Mariani Ave., Cupertino, CA 95014, (408) 996-1010.

Inquiry 586.

IBM Upgrades Convertible

IBM announced enhancements to the PC Convertible, including a "supertwist" LCD screen, a 256K-byte static CMOS memory board, and a Hayes-compatible internal 300/1200-bps modem.

The screen is the same size as that of the original PC Convertible, and it displays dark blue characters against a reflective silver background. The surface of the screen is etched and, because it isn't backlit, the battery life of the PC convertible is between six and ten hours.

A new 256K-byte memory board, when combined with the system's standard 256K and a 128K-byte memory-expansion board, enables you to expand the total memory to 640K bytes. The previous limit was 512K bytes.

continued

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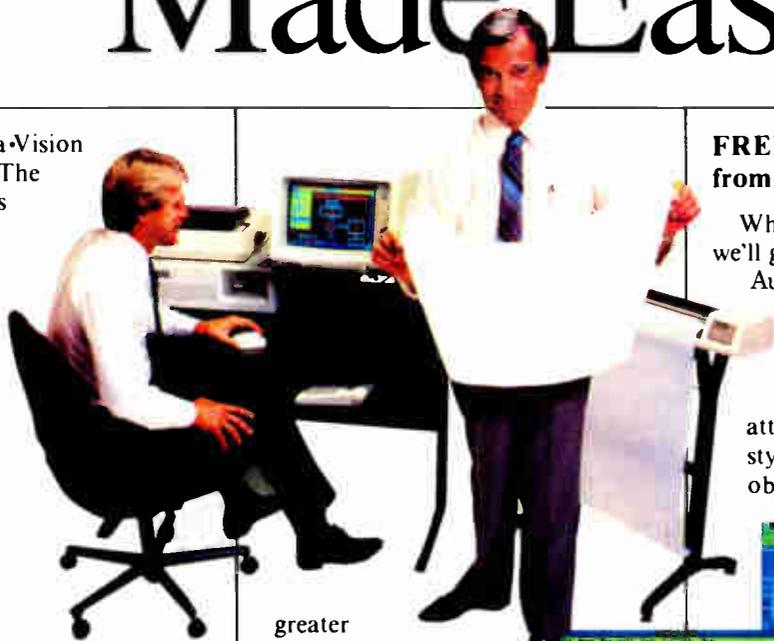
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Demo disk** or brochure available to qualified customers. In Texas or for customer support, call (214) 234-1769.

MICROGRAFX, Inc., 1820 North Greenville Avenue, Richardson, Texas 75081.

Inquiry 178

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Price: \$1995 for PC Convertible with new screen.

Upgrades for current owners: \$250 (screen); \$390 (memory expansion); \$450 (modem).

Contact: IBM Corp., 900 King St., Rye Brook, NY 10573, (201) 358-5677. **Inquiry 587.**

Processing Text and Graphics on the Apple II

Charts Unlimited from Graphware is a graphics and text-processing program that runs on 64K RAM Apple IIs and enables you to create, edit, and print full-page flowcharts and organizational charts.

The worksheet is 123 columns by 90 rows. Although the entire worksheet is not visible at one time, a feature called View lets you shrink it to one-eighth its normal size and display it on the right side of your screen.

Flowchart objects, boxes, and geometric shapes are included. And you can make use of the program's text-editing capabilities to enter, insert, and delete characters on the worksheet. You can print full-page charts vertically or horizontally in enhanced or normal print on most dot-matrix printers, according to Graphware.

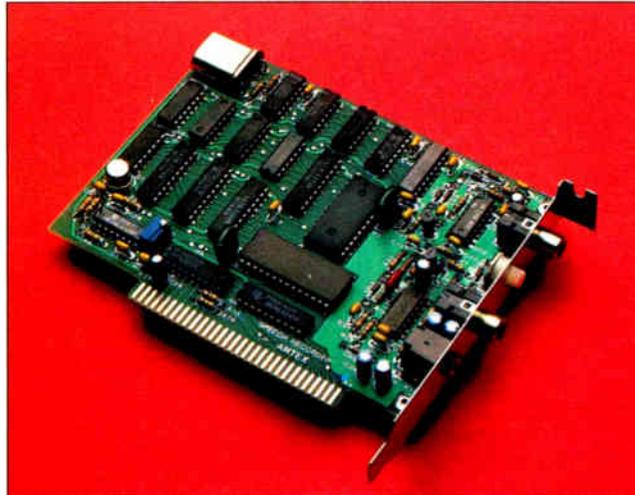
Price: \$49.95.

Contact: Graphware Inc., P.O. Box 373, Middletown, OH 45042, (513) 424-6733.

Inquiry 588.

Digital Audio on a Floppy Disk

The Antex Model VP 600 is a half-length card for the IBM PC and compatibles that converts voice-frequency audio into digitally encoded waveforms for storage on a floppy disk. The board comes with ports for both microphone and cassette input, and menu-driven software for board control is included.



Antex Model VP 600 converts audio to digital waveforms.

The Model VP 600 uses adaptive differential pulse-code-modulation encoding and handles frequencies from 20 Hz to 3500 Hz with a 48-dB dynamic range. Sampling rates of 4 kHz or 8 kHz are selectable. At the 4 kHz sampling rate, an hour of voice recording requires 7.2 megabytes of disk storage.

Price: \$345.

Contact: Antex Electronics Corp., 16100 South Figueroa St., Gardena, CA 90248, (213) 532-3092.

Inquiry 589.

An 80386 Motherboard for the PC

The ZEOS 386/M is an IBM PC AT-compatible motherboard that upgrades IBM PCs, XTs, and ATs to 80386-based systems. The unit has a 16-bit PC AT-compatible bus for peripherals and a 32-bit, 16-MHz zero-wait-state bus for memory.

The 386/M comes with the Phoenix 80386 IBM PC AT-compatible ROM BIOS, and hardware support for the 80386 is provided by Chips and Technologies' seven-chip AT/386 chip set combined with the company's 82C206 integrated peripheral controller.

Sockets are provided on the motherboard for Chips and Technologies' two-chip EGA

and Western Digital's single-chip floppy disk controller. The board has provisions for up to 16 megabytes of fast zero-wait-state RAM. A minimum of 1 megabyte of memory is required.

To ensure compatibility with standard PC/AT/XT expansion boards, the 16-bit PC AT I/O-expansion bus runs at 8 MHz while the system runs at 16 MHz. You can also slow the system down via keyboard commands for software that's dependent on clock speed. A socket for the 80387 math coprocessor chip is also included.

Price: \$1995 (without RAM). **Contact:** ZEOS International, 530 5th Ave. NW, Suite 1000, St. Paul, MN 55112, (800) 423-5891; in Minnesota, (612) 633-4591.

Inquiry 590.

Mega ST has Megabyte Memories

Atari has released new versions of its ST series of personal computers. The Mega ST 1, ST 2, and ST 4 are shipped with 1, 2, and 4 megabytes of RAM, respectively. All have a newly designed 22-inch-square by 2-inch-high system unit that results in a smaller footprint than either the 520ST or

1040ST. They also have detachable keyboards and built-in 800K-byte 3½-inch disk drives.

Additional enhancements to the Mega ST include a battery-backed real-time clock, internal mounting space for an additional circuit board, and full access to the 68000 system bus via an external connector. Atari says it will soon be offering RAM expansion upgrades of up to 16 megabytes.

Atari has also announced that prices will be reduced on existing ST models. The 520ST will retail for "under \$300." A 1040ST with a monochrome monitor will sell for \$899, and a 1040ST with a color monitor for \$1099. **Price:** Starting at "about" \$1000 (final pricing not available at press time). **Contact:** Atari Corp., 1196 Borregas, Sunnyvale, CA 94088, (408) 745-2000. **Inquiry 591.**

Clip-on 68020 Mac Upgrade

The Prodigy Prime Macintosh enhancement board adds considerable power to an existing Macintosh. Included is a 16-MHz 68020 microprocessor, 1 megabyte of RAM, an internal fan, a non-volatile RAM disk, and an additional power supply. The unit is user-installable and clips onto a 128K or 512K Macintosh or a Macintosh Plus motherboard.

Available options include up to 4 megabytes of RAM, a 16-MHz 68881 math coprocessor, a 68851 paged-memory-management unit for expanded memory use, an enhanced SCSI controller that can handle up to 24 peripherals, and an expansion connector for large screen monitors and other devices.

Price: \$1995. **Contact:** Levco, 6160 Lusk Blvd., Suite C-203, San Diego, CA 92121, (619) 457-2011.

Inquiry 592.

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Admit it. You're intrigued with the idea of C programming. You may be working in BASIC, Pascal or Assembler now. But you're drawn to the power, portability and flexibility of C. And if money is what motivates you, imagine having it all for just \$75 with Mark Williams Let's C.*

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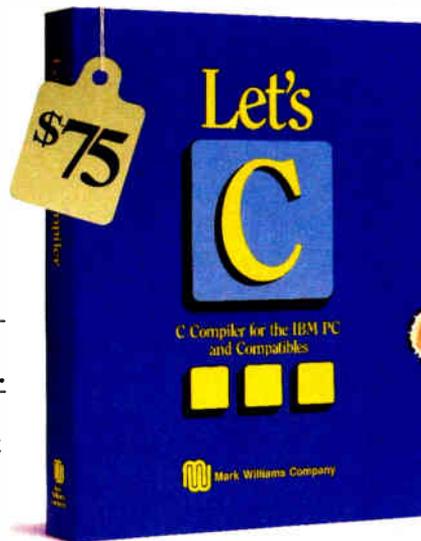
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—William G. Wong, *BYTE*, August 1986.

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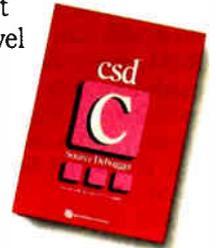
—Christopher Skelly, *COMPUTER LANGUAGE*, February 1986

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—Marty Franz, *PC TECH JOURNAL*, August 1986

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Inquiry 167

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SYSTEMS

Commodore Joins the Clone Wars

Commodore International has started selling its two IBM PC XT clones in the U.S. Introduced in Europe last year, the PC10-1 and PC10-2 are shipped with standard equipment that includes an RS-232C serial port, a parallel printer port, and a multifunction color/monochrome graphics card that's compatible with IBM monochrome and CGA modes, as well as with Hercules and Planatronics modes.

Both units use the 8088 microprocessor running at 4.77 MHz. Each machine has five full-length expansion slots and space for two half-height floppy disk drives and a hard disk drive, with a power supply large enough to handle the complete system.

The PC10-1 includes a single 5¼-inch floppy disk drive and 512K bytes of RAM, which can be expanded to 640K bytes on the motherboard. The PC10-2 includes two 5¼-inch floppy disk drives and 640K bytes of RAM.

Both units come with MS-DOS 3.2 and GW-BASIC 3.2. **Price:** \$999 (PC10-1); \$1199 (PC10-2).

Contact: Commodore Business Machines, 1200 Wilson Dr., West Chester, PA 19380, (215) 431-9100. **Inquiry 593.**

Computer in a Cube

The CUBIX² and CUBIX³ are the two members of L/F Technologies' CUBIX System V. They are both multiuser UNIX systems built around an 80286 microprocessor, and both run at 8 MHz with no wait states.

The CUBIX² is an 11-inch cube. It supports up to eight users and is shipped with one megabyte of RAM (expandable to four megabytes), eight serial I/O ports, one 80186-based Ethernet port, a single 1.2-megabyte floppy



Commodore enters the PC clone sweepstakes with the PC10.

disk drive, and a 20-megabyte hard disk drive.

The CUBIX³ is for larger processing applications. It sits on the floor and supports up to 16 users. You can expand its RAM to eight megabytes.

System options for both include a 60-megabyte streaming tape drive for backing up the hard disks, an 80287 math coprocessor chip, and a proprietary-design uninterruptible power supply.

Both CUBIX systems are compatible with UNIX software written for the AT&T 6300 Plus. The CUBIX operating system mirrors the UNIX system V.2 release, so it is able to perform operations previously restricted to large machines, such as compiling FORTRAN.

Price: \$4795 (CUBIX²); \$5995 (CUBIX³).

Contact: L/F Technologies, 2800 Lockheed Way, Carson City, NV 89701, (702) 883-7611.

Inquiry 594.

TeleVideo's Three Workstations

TeleVideo has rolled out its first multiuser workstations designed for use with both UNIX System V and MS-DOS.

Designed for between two and eight users, the 80286-based TELENIX-286 has a 40-megabyte hard disk, a single 1.2-megabyte floppy disk drive, a 60-megabyte streaming tape drive, 1 megabyte of RAM, five expansion slots, and a 14-inch monochrome monitor.

The 80386-based TELENIX-386 is designed for between eight and 16 users. It comes with either a 40-megabyte or 71-megabyte hard disk drive, two megabytes of RAM (expandable to 16 megabytes), a 60-megabyte streaming tape drive, and eight expansion slots, including two 32-bit slots.

Both systems come with Microport Systems' V/AT UNIX, a version of AT&T's System V operating system. Both also feature TeleVideo's

proprietary high-performance disk controller. The company claims disk I/O performance is increased by a factor of three over competing 80286-based machines because an entire track of data can be transferred in one disk revolution instead of three.

Options include Microport's Merge-286 and Merge-386 software, which allow both UNIX and MS-DOS applications to run concurrently.

Price: \$5995 (TELENIX-286); \$9000 (TELENIX-386).

Contact: TeleVideo Systems Inc., 1170 Morse Ave., P.O. Box 3568, Sunnyvale, CA 94088-3568. **Inquiry 595.**

Victor Rolls Out Champion

Victor Technologies has unveiled Champion, the company's entry into the low-cost IBM PC-compatible market. Champion comes standard with an 8086 microprocessor, 640K bytes of RAM, a monochrome graphics card, and a single 5¼-inch floppy disk drive. A 12-inch monochrome monitor is optional.

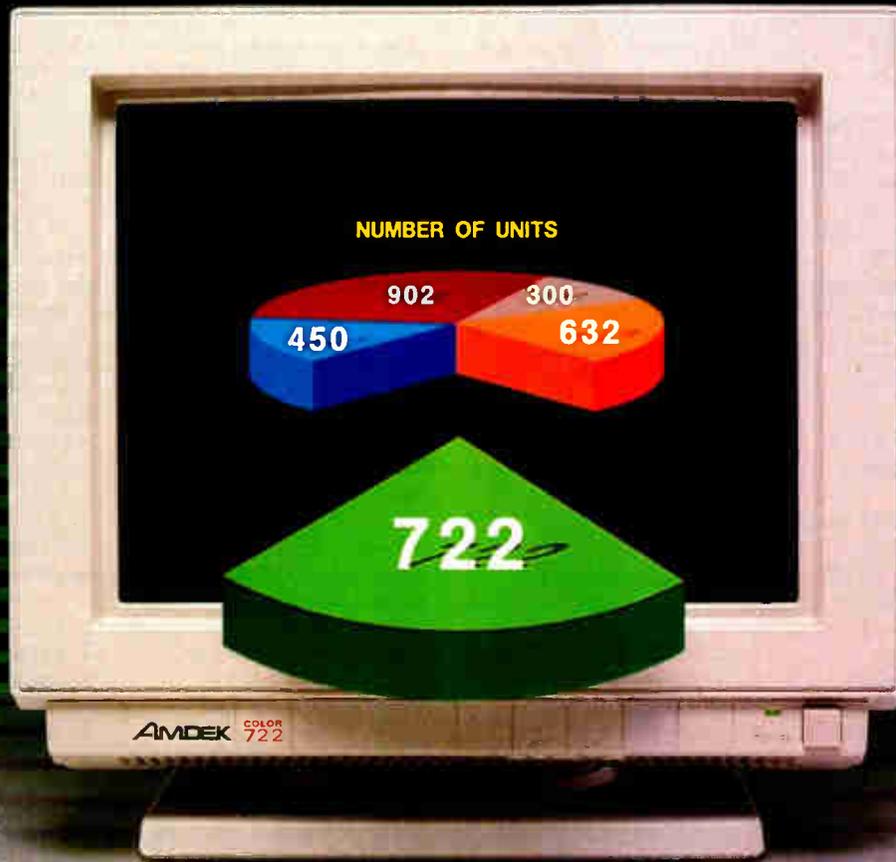
The system has five expansion slots, serial and parallel ports, and a 67.5-watt power supply. Standard software includes MS-DOS 3.1, GW-BASIC, the Word Result word processing package, and the Calc Result spreadsheet.

Price: \$799 (Champion); \$119 (12-inch monochrome monitor).

Contact: Victor Technologies Inc., 380 El Pueblo Rd., Scotts Valley, CA 95066-4269, (408) 438-6680.

Inquiry 596.

continued



Enhanced graphics without an enhanced price. The Amdek 722 EGA monitor.

The Amdek 722 high performance color monitor is ideal for all enhanced graphics applications. Amdek engineered the 722 monitor to fully support *both* the IBM Enhanced Graphics Adapter (EGA: 640 x 350 lines resolution), and the IBM Color Graphics Adapter (CGA: 640 X 200). In the EGA mode, you can use any combination of 16 colors from a 64-color palette.

The result is an EGA monitor specifically designed to give you the ultimate in high resolution performance for a wide range of business graphics, engineering, educational purposes, and similar applications.

Other advanced design features include a high quality

etched glass, non-glare screen, and a 3-position switch that allows you to choose green, amber or full-color text.

Ask your computer dealer to show you some of the enhanced features of the Amdek 722 EGA monitor. And then ask to see the *best* feature of all—the price! The Amdek 722 EGA is more monitor for the money. And it's backed by more warranty for your peace of mind—*three years* on the CRT, and *two years* on all other parts and labor.

Once you compare the quality and price, you'll focus your attention on the best monitor for enhanced graphics—the Amdek 722 EGA monitor.

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PERIPHERALS

5¼-inch Floppies on the Macintosh

Abaton's Drive 5.25 for the Macintosh lets you import and export data files directly to and from your Mac using disks created by IBM, CP/M, or UNIX systems. The unit reads and writes over 50 5¼-inch formats and allows the daisy-chaining of additional 8-, 5¼-, 3½-, or 3-inch disk or tape drives.

The Drive 5.25 is also a complete CP/M computer with a built-in Z80 microprocessor and 64K bytes of RAM. It comes with a licensed copy of CP/M 2.2, allowing you to run CP/M programs using your Macintosh as a terminal.

Both an RS-232C serial port and a standard Centronics-compatible parallel printer port are included, as is disk-format translation software.

Price: \$695.

Contact: Abaton Technology Corp., 7901 Stoneridge Dr., Suite 500, Pleasanton, CA 94566, (415) 463-8822.
Inquiry 597.

Monitor the Power Line

The Monitron 2000 is a low-cost power-line monitor that detects and classifies power-line irregularities. It has individual LEDs that show voltage spikes, high voltage, low voltage, dropout, and power failure. A dual-mode on/off LED indicates the operational status: green for normal continuous operation or flashing red to indicate that power's been restored after a blackout.

The unit's fault-detection trigger points are set in accordance with ANSI standard C84.1. The Monitron 2000 responds to voltage disturbances or power interruptions in .5 microseconds and locks

the appropriate LED on until you press the reset button.

Using an included desktop stand or Velcro mounts, the Monitron 2000 easily attaches to a computer terminal, power filter, or uninterruptible power supply.

Price: \$299.

Contact: Mendon Electronics Corp., 3800 Monroe Ave., Pittsford, NY 14534, (716) 248-8480.

Inquiry 598.

Low Cost 300/1200-bps Modem

The Sportster 1200 is USRobotics' low-cost 300/1200-bps modem, a stand-alone auto-dial, auto-answer unit. The Sportster 1200 is fully compatible with the AT modem command and S-Register set, and it comes complete with two RJ11C telephone jacks.

The unit has two LED status lights: data/test mode and carrier-detect/received-data mode. Other status messages are displayed on-screen from the modem's ROM. The Sportster 1200 can also automatically redial a busy number up to 10 times. The built-in speaker's volume has a thumbwheel control.

Price: \$149.

Contact: USRobotics Inc., 8100 North McCormick Blvd., Skokie, IL 60076, (312) 982-5010.

Inquiry 599.

New Commodore 64/128 Accessories

Commodore has introduced three new peripherals that extend the capabilities of the Commodore 64 and 128 personal computers.

The 1581 disk drive uses 3½-inch disks and stores

808K bytes per disk. It's compatible with the C-128, C-64, Plus 4, and C-16 computers and has a data-transfer rate three times the speed of the Commodore 5¼-inch drive.

The 1764 RAM expansion adds 256K bytes of memory to the Commodore 64. It plugs into the 64's expansion port and comes with software that enables you to use it as a standard RAM disk. It also comes with special RAM disk software for the GEOS (Graphic Environment Operating System) that's supplied with the 64C.

Finally, the company introduced the 1351 two-button Mouse, which you can use in both joystick and proportional modes. It works with the C-64.

Price: \$399 (1581 disk drive); \$129 (1764 RAM-expansion module); \$49 (1351 Mouse).

Contact: Commodore Business Machines Inc., 1200 Wilson Dr., West Chester, PA 19380, (215) 431-9100.
Inquiry 600.

Ricoh's Low-cost Laser Printer

The PC Laser 6000 is Ricoh's new compact six-page-per-minute laser printer with 300-dpi resolution. It comes standard with 1 megabyte of memory and is expandable to 2 megabytes.

The unit's controller has its own graphics command set, which includes Diablo 630 emulation. Optional emulation cards are available for the HP LaserJet Plus, IBM Pro-Printer, and the Epson FX-80.

The 6000 has eight resident fonts, and optional font cartridges are also available. There's also a special line-printer Compressed mode. All features and fonts are accessed through a program-

mable front panel, eliminating any DIP switches.

Based on Ricoh's newest second-generation print engine, the 6000 can print a fully bit-mapped 8½- by 14-inch legal-size pad. Paper can be delivered either face down in collated order, or face up in reverse order.

The PC Laser 6000 weighs 34 pounds and measures 8 inches high by 16 inches wide by 16½ inches deep.

Price: \$2395; \$249 (512K RAM expansion).
Contact: Ricoh Corp., 5 Dedrick Place, West Caldwell, NJ 07006, (201) 882-2000.
Inquiry 601.

3.5-inch External Floppy for PCs

Manzana's MDQ is an external 3½-inch host-powered disk drive for the IBM PC and compatibles. Besides upgrading PCs to 720K bytes of storage, the MDQ can transfer data between different brands of laptop and desktop computers.

For computers without an external drive port, Manzana provides a mux adapter card that intercepts the signal and power from the controller drive and sends it to the MDQ drive.

The MDQ comes with Manzana's 3FIVE software, which includes a device driver and format program that allows the 3½-inch drive to work with versions of PC-DOS or MS-DOS 2.0 or higher.

Price: \$395; \$355 (without mux adapter card).
Contact: Manzana Microsystems Inc., 7334 Hollister Ave., Suite B, Goleta, CA 93117, (805) 968-1387.
Inquiry 602.

Here's a plug for dBASE.™

Clipper™ NEWS RELEASE

FOR IMMEDIATE RELEASE

For information contact:

■ Nantucket
Nantucket Corporation®
12555 Jefferson Blvd.
Los Angeles, CA 90066
(213) 390-7923

CLIPPER™ NETWORKS DBASE APPLICATIONS

LOS ANGELES, California... Nantucket's Clipper now lets developers and business persons plug an unlimited number of workstations together to run their dBASE III and dBASE III PLUS applications, using Clipper's new networking capabilities.

This new release compiles programs to run on networks that support DOS 3.1 calls for networking functions, plus single-user programs for DOS 2.0 or greater.

Compiled Applications can be distributed freely, need no runtime module, no licensing fee or royalty. And there is no extra cost per user, regardless of how many users are connected to a Clipper network. Plus the new release now packs even more of Clipper's famous speed, on both single-user and networking applications.

The new Clipper also sports Expanded Memory support, additional functions and improved memo fields. The new release, dubbed Autumn '86, is not copy protected.

Clipper Autumn '86 is available for a suggested retail price of \$695. Registered users of Clipper may upgrade to the new version for \$139.

Clipper and Nantucket are trademarks of Nantucket Corporation. Other products trademarked by others. Copyright 1986, Nantucket Corporation.

Inquiry 189 for End-Users. Inquiry 190 for DEALERS ONLY.

That W And Thi



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Catch your breath. We're not done. There's also 14 function math, subdirectory support, go to page, and improved spelling correction and Mail-Merge. There's even an optional 40 function key interface. Like we were saying, this one's loaded.

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Word Finder is a trademark of MicroVox, Inc.

Inquiry 181

World Radio History

APRIL 1987 • B Y T E 41

ADD-INS

Another Hi-Res PC Graphics Controller

Metheus Corp. has introduced the 1004 high-resolution graphics controller designed for CAD and CAE applications. The 1004 has a screen resolution of 1024 by 768 pixels and displays 16 colors from a palette of 4096. It occupies a single 8-bit slot in an IBM PC XT- or PC AT-compatible computer.

In addition to high-resolution graphics, the 1004 fully emulates an IBM CGA and can display text in 960-by-600-pixel resolution for superior legibility.

Using proprietary bit-slice technology, the 1004 uses drawing rates varying from 5 million pixels per second for random vectors all the way to 42 million pixels per second for area fills.

The 1004 also features security-verification hardware that allows programmers to build in a security key to prevent unauthorized use of software.

Price: \$2995.

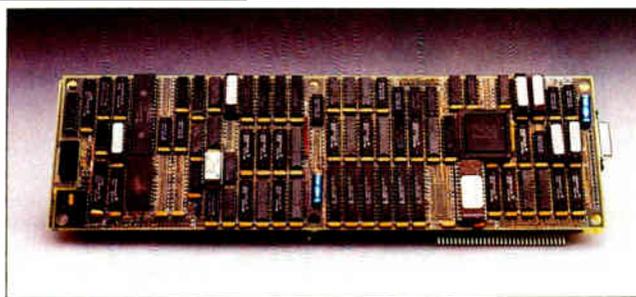
Contact: Metheus Corp., 5510 Northeast Elam Young Pkwy., Hillsboro, OR 97214, (503) 640-8000.

Inquiry 603.

Memory/Modem Card for the Toshiba Laptop

Megahertz Corp. is shipping a combination EMS memory and modem card for the Toshiba T3100 laptop computer. The Helix EMS/T1200 has one megabyte of expanded memory and a Hayes-compatible 300/1200-bps modem.

You can configure the card's memory as either regular extended memory or with the Lotus/Intel/Microsoft Expanded Memory Specification. Software drivers allow programs such as Lotus 1-2-3, Symphony, Framework, and others to access the expanded memory.



The Metheus 1004 displays 16 colors at 1024 by 768 pixels.

The modem is fully Hayes-compatible and includes auto-answering, auto-dialing, automatic adjustment to incoming data speed, and full- or half-duplex operation.

The EMS/T1200 comes bundled with Crosstalk communications software.

Price: \$795.

Contact: Megahertz Corp., 2681 Parleys Way, Suite 2-102, Salt Lake City, UT 84109, (801) 485-8857.

Inquiry 604.

Two Add-ins for Amiga Fans

Progressive Peripherals & Software has rolled out the MegaBoard, a compact two-megabyte RAM expansion for the Amiga. The MegaBoard uses programmable-array logic and zip-packaged 256K-byte RAMs for small package size and high reliability. It's designed to fit snugly next to the Amiga without intruding on your workspace.

Price: \$599.95.

Contact: Progressive Peripherals & Software Inc., 464 Kalamath St., Denver, CO 80204, (303) 825-4144.

Inquiry 606.

Meanwhile, Commodore has expanded the capabilities of the Amiga with the introduction of the Genlock 1300 video synchronizer, which can synchronize an external video signal from a VCR, camera, or videodisc player with the text, sound, and graphics generated by the Amiga. This

allows you to superimpose the Amiga's graphics, stereo sound, and titles over videotaped images. You can display the resulting synchronized graphics on a monitor or TV set or record them on videotape for later use.

The Genlock 1300 weighs 2½ pounds and fits into the Amiga chassis. It then connects to the RGB port of the computer's main console. The Genlock 1300's input ports accept an RS-170 composite signal, stereo audio lines, and an Amiga computer signal. Output ports include both composite and RGB video, as well as a stereo audio signal.

Price: \$195.

Contact: Commodore Business Machines Inc., 1200 Wilson Dr., West Chester, PA 19380, (215) 431-9100.

Inquiry 607.

1000-word Speech Recognition System

VoiceScribe-1000 is a word-pattern-matching system that Cherry Electrical Products claims is capable of recognizing 1000 words or phrases with an accuracy of 99.3 percent.

Software packaged with the board includes overlays for popular applications including spreadsheets, word processors, databases, and more.

The VoiceScribe-1000 requires a hard disk drive and at least 512K bytes of RAM. The system comes with software, an expansion card, a

microphone, and a tutorial manual.

Price: \$1195.

Contact: Cherry Electrical Products Corp., 3600 Sunset Ave., Waukegan, IL 60087, (312) 360-3500.

Inquiry 608.

Controlling the Real World

Cortec's D64180 coprocessor card is designed as a dedicated intermediate processor between an IBM PC or compatible and real-world devices that require rapid response. The card easily controls several simultaneous real-time processes through its powerful computing capabilities including two direct-memory access channels, two built-in RS-232C ports, two programmable counter/timers, 256K bytes of RAM (expandable to 512K), and two Intel standard iSBX bus connectors.

The board's D64180 processor has several advantages for real-time control over the 8088 family, included advanced interrupt capability, improved interrupt capability, improved interrupt latency, bit-manipulation instructions, a simpler instruction set, programmable wait states, and clock speeds of 6 and 9 MHz.

The iSBX bus connectors allow for the addition of a wide variety of iSBX Multimodule boards such as RS-422/423 synchronous and asynchronous dual-channel serial communications ports, A/D-to-D/A converters, and I/O control modules. The iSBX boards interface directly to the coprocessor's I/O bus and can decode up to 16 registers out of the 256 available in the I/O space of the HD64180.

Price: \$445.

Contact: Cortec Associates Inc., 4353 Shadow Wood Dr., Eugene, OR 97405, (503) 343-0006.

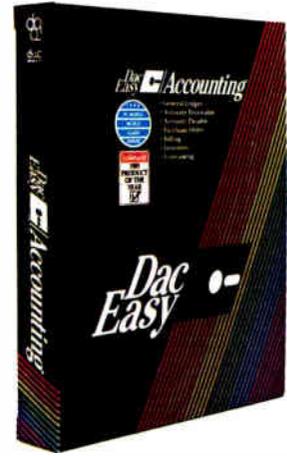
Inquiry 605.

continued

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PC WORLD
October 1986

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Two C Compilers

Borland has announced Turbo C, a C language development system. The program implements ANSI C and supports Kernighan & Ritchie C. Borland reports that the system compiles at a rate of 7000 lines per minute on a 6-MHz IBM PC AT.

With Turbo C you can choose to use an integrated environment or a command-line interface.

The integrated environment comes with an editor, compiler, and linker. Its Run operation recompiles all necessary files, generates executable code, runs the program, then returns to the user interface.

In command-line mode you can select compiler options from the command line, the integrated environment, or from a configuration file—without having to set environment variables, according to Borland.

The built-in editor enables you to call and toggle between the editor and the message window. The editor window provides insert/overwrite, auto-indent, and block capabilities. The message window displays error messages. According to Borland, Turbo C steps through multiple errors, and the interactive editor positions the cursor in the source code at the point of error.

Compiler options include an in-line assembler, multiple levels of optimization, generation of 80186/80286/8087 instructions, warning suppression, and multiple memory models. A LINT facility that supports ANSI prototypes is also provided. Other features include a library that supports the IEEE floating-point standard, support for UNIX-compatible routines, supplemental functions for BIOS and DOS calls, and optional Pascal calling conventions. **Price:** \$99.95.

Contact: Borland Interna-

tional, 4585 Scotts Valley Dr., Scotts Valley, CA 95066, (408) 438-8400. **Inquiry 609.**

Mark Williams Company has announced version 4.0 of the Let's C compiler, which, like Borland's Turbo C, runs on IBM PCs and supports Kernighan & Ritchie C. The new version features in-memory compilation and development features such as 80286 code generation, ROMable code, 8087 math coprocessor support, large and small memory models, and an option for a large and small model source-level debugger.

The company reports that the speed of the compile-edit cycle has been increased by more than a factor of two because the compilation is handled within RAM, and an editor is integrated into the compiler. The editor locates source-code errors by flagging the program and pulling the source code into the editor at that location. When you exit the editor, the program recompiles the code. **Price:** \$75.

Contact: Mark Williams Co., 1430 West Wrightwood, Chicago, IL 60614, (312) 472-6659.

Inquiry 610.

BASIC Programming Language for the Atari ST

MichTron has introduced GFA BASIC, a high-level language for the Atari ST. Some of the commands in the program let you incorporate routines from other languages. GFA BASIC has a command that lets you load and execute a non-BASIC Atari ST application from within a BASIC program. Another command calls a routine written and compiled in C. Both commands allow full parameter passing, according to MichTron. Other commands include graphics, UNIX-style DOS functions,

and new keywords.

With GFA BASIC, you can incorporate the features found in GEM, including windows, drop-down menus, and alert boxes. The program also enables you to accept parameters from the main program and use local variables. Line numbers are eliminated with labels in their place, and subroutines have taken the form of procedures. **Price:** \$79.95.

Contact: MichTron, 576 South Telegraph, Pontiac, MI 48053, (313) 334-5700.

Inquiry 611.

Programming Know-How in English

The expert-system shell Xi Plus from Expertech enables you to use plain English to create knowledge bases and applications that check and share expert decision know-how. The program is rule based and has extended inferencing, which includes forward, backward, and demon priority rules. Also included are interfaces for external files, graphics, and telecommunications.

The program runs on IBM PCs and compatibles with at least 512K bytes of RAM. **Price:** \$1250.

Contact: Expertech, 650 Bair Island Rd., Suite 204, Redwood City, CA 94063, (415) 367-6293.

Inquiry 612.

Virtual Memory Manager

Sapiens V8 is a virtual memory manager for C programmers designed around a least-recently-used 1K paging system. The program emulates an 80386 memory-management system and offers an 8-megabyte workspace.

The program runs on IBM PCs with at least 256K bytes of RAM and MS-DOS or PC-DOS 2.0 or higher.

Price: \$300.

Contact: Sapiens Software Corp., P.O. Box 7720, Santa Cruz, CA 95061-7720, (408) 458-1990.

Inquiry 613.

Debugging with VIM

VIM is an interpreter for 8088 machine code that executes in virtual memory on IBM PCs, XTs, ATs, and compatibles with at least 320K bytes of RAM. The VIM virtual debugging environment includes the addressing space of the processor, so the program under test can work with its own copy of DOS, interrupt vectors, RAM disks, device drivers, and resident utilities. **Price:** \$69.

Contact: Digital Dispatch Inc., 1580 Rice Creek Rd., Minneapolis, MN 55432, (612) 571-7400.

Inquiry 614.

Locate Compiler Syntax Errors in QuickBASIC

Bascheck is a compiled artificial intelligence program designed to find compiler syntax problems in files written to run with BASIC interpreters. Written in Prolog, the program writes a printable .ERR file to your hard or floppy disk when it locates illegal compiler syntax and compiler switch requirements. The program supplies line numbers, commands, a statement of the problem, and suggested corrections. The Sieve of Eratosthenes compiled with QuickBASIC and Turbo Pascal are included.

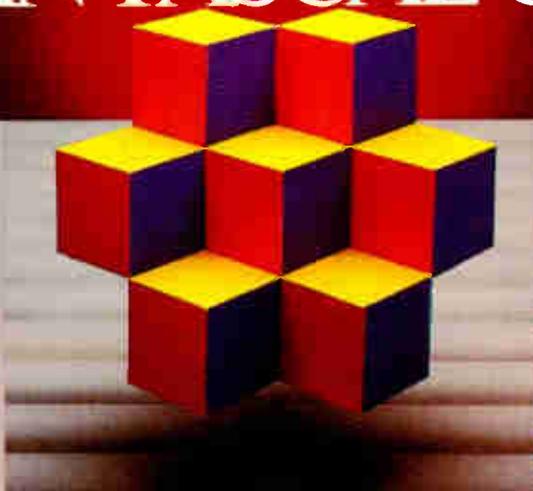
Bascheck runs on IBM PCs and compatibles with PC-DOS or MS-DOS 2.0 or higher.

Price: \$59.95.

Contact: Haines & Associates Inc., 12000 Westheimer, Suite 214, Houston, TX 77077, (713) 493-3149.

Inquiry 615.

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Finite-Element Modeling

PCTRAN Plus is a modular finite-element analysis program that has menus to assist you in creating finite-element models. You can call the menus with the press of one key, according to Brooks Scientific, or you can type commands if you prefer.

PCTRAN Plus runs on IBM PC XTs, ATs, and compatibles with at least 640K RAM, a floating-point chip, and a high-resolution graphics display card.

Price: \$1295.

Contact: Brooks Scientific Inc., 55 Wheeler St., Cambridge, MA 02138, (617) 491-9220.

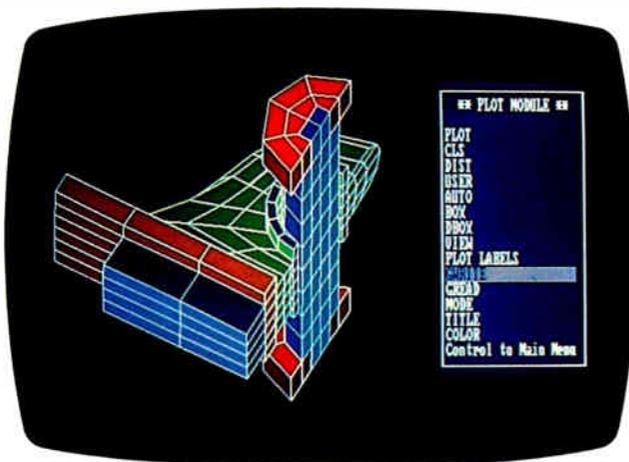
Inquiry 616.

CCICAP Analyzes Linear Electronic Circuits

With CCICAP you can analyze circuits with up to 100 nodes and 300 circuit elements. The available circuit elements include passive elements of resistors, capacitors, and inductors as well as the four types of controlled sources. Built-in models are included for operational amplifiers, bipolar junction transistors, and field-effect transistors. Desired outputs are indicated using voltmeter and ammeter elements.

You can also use CCICAP to analyze noise at any node in the circuit. White noise sources are included for all circuit resistances, and white and flicker voltage and current noise sources are included for active elements. The noise calculations are performed as part of the frequency analysis. You can also calculate circuit time-domain responses to impulse and step inputs.

The program produces two types of output: an ASCII file



PCTRAN Plus helps create finite-element models.

with the data in tabular format, or a binary data file for use by a postprocessor.

CCICAP is not copy-protected and runs on IBM PCs and compatibles with at least 440K bytes of RAM and MS-DOS 2.0 or higher. It will operate with or without an 8087 coprocessor.

Price: \$50.

Contact: Circuit Concepts Inc., 6955 Santa Fe, Houston, TX 77061, (713) 643-5451.

Inquiry 617.

Converting Units

Unit*Assistant, a memory-resident unit-conversion program from Thermal Systems Analysis Inc., breaks down units into their base units and then converts each of them. It then determines the appropriate factor for converting the input units to the output units. You can enter the complete unit groups in single lines using base unit names, common abbreviations, prefix names and symbols, and unit exponents. You can also combine several unit groups into one request.

The program runs on the IBM PC, XT, AT, and compatibles with at least 256K RAM and MS-DOS or PC-DOS 2.0 or higher.

Price: \$75.

Contact: Thermal Systems Analysis Inc., P.O. Box 193,

Broomfield, CO 80030, (303) 469-8507.

Inquiry 618.

Peregrine Falcon Announces EGG

The technical word processing program EGG offers WYSIWYG editing, enabling you to watch your changes being made as you edit complex math and chemical symbols.

EGG offers 17 levels of superscripting and subscripting on each line. You can transfer multilevel formulas and chemical structures as complete units in horizontal or vertical column block moves throughout the document. You can also incorporate word processing text files into the program.

Peregrine also offers the ChemLibrary (\$125), which includes 500 preformed chemical structures and a design kit of 100 characters with which you can modify and combine existing structures or create new ones.

EGG runs on IBM PCs, ATs, XTs, and compatibles with at least 256K bytes of RAM and a graphics board. The company recommends 24-pin printers for optimal output.

Price: \$495.

Contact: Peregrine Falcon Co., 2330 Marinship Way, Suite 307, Sausalito, CA 94965, (415) 331-8131.
Inquiry 619.

Fast Fourier Transform Spectrum Analyzer

Sofcad Electronics has announced a spectrum signal analyzer program that you can use to analyze digital and analog signals on an IBM PC, Commodore 64, or Commodore 128. With FFTSA, spectrum plots of amplitude versus frequency will be in discrete form, and if enough points are taken in the discrete plots, a Fourier transform of the signal will be produced by an accurate joining of the ends of the discrete lines. If the waveform you're analyzing is a true repetitive wave, the spectrum plot is a Fourier series amplitude representation.

The program includes amplitude spectrum, phase spectrum, and time plots. Also featured are Hamming and Hanning window functions, disk save and load functions, and functions of AM, FM, triangular, sine, and pulse waveforms.

According to Sofcad, plots can be from 16 to 1024 points. The Commodore version plots in the text mode, and the spectrum is limited to 512 points.

The IBM PC version of FFTSA requires 256K bytes of RAM and a CGA for high-resolution graphics printing. The Commodore version requires that you use a Simon's BASIC cartridge for plotting on a monitor or television screen.

Price: \$99 for the IBM version; \$49 for the Commodore 64/128 version.

Contact: Sofcad Electronics Inc., P.O. Box 21845, Columbus, OH 43221, (614) 488-3400.

Inquiry 620.

continued

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BEST MOUSE FOR DESKTOP PUBLISHING

Ergonomic styling is a must for all mouse-intensive desktop publishing applications. High resolution is essential for high-resolution screens.

BEST MOUSE FOR SPREADSHEETS & WORD PROCESSING

The smooth-tracking LOGITECH mouse is a productivity tool for all types of data entry and editing. We've even created a special mouse interface for 1-2-3 which makes 1-2-3 users up to 30% more productive!

BEST MOUSE SOFTWARE

"Logitech's Plus Package adds an excellent menu builder (with useful examples), a fast windowing text editor, and an outstanding Lotus 1-2-3 interface." Ezra Shapiro Byte, Dec. '86, pg. 324

Our Plus Software also includes our Microsoft-compatible drivers, and CLICK which sets the mouse automatically for any application.

BEST DEALS

We offer either our C7 or Bus mouse, with Plus software, packaged with some of the most exciting applications on the market, at very exciting prices.

LOGIPAINT Special Offer! \$149

The LOGITECH Mouse with PC Paintbrush is the most advanced paint set available for the PC. It offers 11 type fonts, a pallet of 16 colors, and the ability to import and embellish files from other applications.

LOGICADD \$189

The LOGITECH Mouse packaged with Generic CADD and Dot Plot turns your PC into a complete CADD workstation. Generic CADD offers the features and performance of high priced CADD at an unbelievably low price. DotPlot is the add on utility that enables you to produce crisp, high resolution drawings from your dot matrix printer.

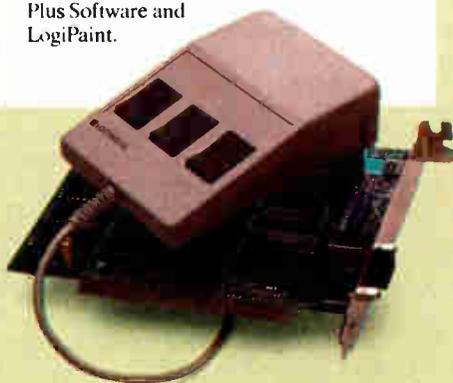
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The LOGITECH Mouse packaged with LOGIPAINT and LOGICADD. Together they are the complete graphics toolkit for combining freehand and technical drawings.

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LOGITECH BUS MOUSE \$149 with LogiPaint

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Money Matters teaches financial concepts in a three-module set. Module 1 contains two disks and teaches the structure of financial statements. Module 2 contains three disks and helps you interpret financial statements. Module 3 contains two disks and offers lessons on financial forecasting and budget control. The program, which includes color graphics, operates on IBM PCs, XTs, ATs, and compatibles.

Price: \$300 for the three-module set.
Contact: CBT Systems Inc., 111 Speen St., Suite 510, Framingham, MA 01701, (617) 879-7174.
Inquiry 621.

Training Program for MAP

Scientific Systems has introduced MAP-Facts Advanced Concepts, a computer-based training program for Manufacturing Automation Protocol, the standard developed by General Motors. The program presents an overview of factory communications, from the International Standards Organization's seven-layer model for Open Systems Interconnection to implementation and performance information.

As a reference aid, MAP-Facts supplies up-to-date information on MAP specifications and descriptions of terminology. As a training tool, the program helps you work on reaching measurable goals by practicing on the information covered in each topic. Feedback helps you identify areas that require further study. Text and graphic screen displays, on-line help windows, and a glossary of technical terms and abbreviations enable you to progress at your own pace.

To run the program you need an IBM PC or compatible with at least 256K bytes of RAM, a CGA, and two floppy disk drives or one floppy and one or more hard disk drives.

Price: \$595.
Contact: Scientific Systems Inc., One Alewife Place, 35 CambridgePark Dr., Cambridge, MA 02140, (617) 661-6364.
Inquiry 622.

Bank Street Writer Plus for Apple IIs

Broderbund has announced the Apple IIe, IIc, and IIGS version of Bank Street Writer. Bank Street Writer Plus includes a spelling corrector with a 60,000-word dictionary, an on-line thesaurus, an editor, and pull-down menus.

Price: \$79.95.
Contact: Broderbund Software Inc., 17 Paul Dr., San Rafael, CA 94903-2101, (415) 479-1170.
Inquiry 623.

Macintosh Desktop Publishing

FullWrite Professional offers word processing and desktop publishing capabilities with WYSIWYG editing.

Some of the word processing features include footnotes and end notes, tables of contents, indexing, spell checking, hyphenating, outlining,

accessing style sheets, and folding. You can also search text attributes in any portion of the document.

Desktop publishing features include wrapping text around nonrectangular sidebars, guttering, kerning, and flexible leading. You can also place independently formatted documents within the main document, allowing for multiple column styles on a single page.

The program runs on 512K-byte Macs.

Price: \$215.
Contact: Ann Arbor Softworks, 2393 Teller Rd., Suite 106, Newbury Park, CA 91320, (805) 375-1467.
Inquiry 624.

Low-cost Graphics Program

The Draftsman from Hire Education lets you produce pie charts, exploded pies, stacked and cluster bar charts, scatter plots, and line graphs. You can size and move each graph and place several on the screen at the same time. In edit mode you can draw on the screen, embellish graphs, and create organizational charts and flowcharts.

You can import data from dBASE II or Lotus 1-2-3. Input formats include DIF, comma-delimited files, data storage files, and keyboard input. You can also use a mouse for input.

The program also features a slide-show mode that lets you

present slides in any sequence and at any interval.

The Draftsman runs on IBM PCs and compatibles with at least 128K bytes of RAM and a color monitor. The company recommends 192K bytes of RAM and two floppy disk drives or a hard disk.

Price: \$25.
Contact: Hire Education Inc., 3631 Jenifer St. NW, Washington, DC 20015, (202) 966-1635.
Inquiry 625.

Automate for Small Businesses

RHM & Associates has unveiled a small business order entry and billing program. Automate includes invoicing, billing, inventory, and record-keeping capabilities.

To keep track of your inventory, at the time of sale you enter quantity sold and stock number. The program checks your inventory and enters an item description, the price, tax, and totals. You can also enter merchandise, labor, services, payments on account, or payments to vendors. When the sale is complete, your inventory is updated. You can print individual customer statements as well. Also reported are sales, costs, margins, markups, and low stocks.

Automate handles 32,000 stock numbers, 999 customer accounts, and 10 line items per invoice. You can have up to six windows with look-up files on the screen at one time for reference information.

The program runs on IBM PCs with 256K bytes of RAM and a CGA.
Price: \$149.95.
Contact: RHM & Associates, 913 Helen St., Midland, MI 48640, (517) 631-9334.
Inquiry 626.

WHERE DO NEW PRODUCT ITEMS COME FROM?

The new products listed in this section of BYTE are chosen from the thousands of press releases, letters, and telephone calls we receive each month from manufacturers, distributors, designers, and readers. The basic criteria for selection for publication are: (a) does a product match our readers' interests? and (b) is it new or is it simply a reintroduction of an old item? Because of the volume of submissions we must sort through every month, the items we publish are based on vendors' statements and are not individually verified. If you want your product to be considered for publication (at no charge), send full information about it, including its price and an address and telephone number where a reader can get further information, to New Products Editor, BYTE, One Phoenix Mill Lane, Peterborough, NH 03458.

dBase, dPen.*

When the ball point pen was introduced, it immediately became indispensable. Never again would you have to struggle with leaky, messy fountain pens. The same is true for database management software. From its inception, it has become a necessary part of the business mainstream. At least that's what anyone who's ever used one will say.

But, the most indispensable database of all is dBase,® outselling all other databases combined. And with good reason. dBase is more powerful, more flexible, has more features and is easier to use. And now it's easier to learn and more powerful than ever thanks to its newest version, dBase III PLUS. But that's not all.

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IBM XT 286-20 Mb

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- Purchase Price \$2,799

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AT&T 6300

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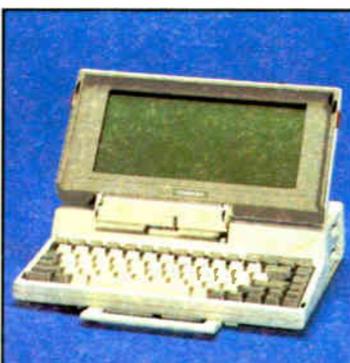


Compaq Deskpro 86-40 Mb
 16, 8 & 4 MHz Clock Speeds • 1 Mb RAM Memory • 80386 Based CPU • One 1 Mb Hard Drive (w/controller) • One 1/2 Mb Half/Height Floppy Drive • 6 Expansion Slots • Compaq 101 Keyboard • One Serial One Parallel • Color or Monochrome Available as Option.
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Compaq Deskpro 286-40 Mb
 • 640K RAM Memory • 80286 Based CPU • One 40 Mb Hard Drive (w/controller) • One 1.2 Mb Half/Height Floppy Drive • Seven Expansion Slots • Compaq Keyboard • Graphics Card • One Parallel Port • Free 90-Day, On-Site Service Contract • Color or Monochrome Available as Option.
Purchase Price: \$3,895
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ITT XTRA XP W/20 Mb
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Enhanced Leading Edge Model D
 • 512K RAM Memory • 1200B Internal Modem • Two 360K Half/Height Floppy Drives • Four Expansion Slots • Keyboard • Text Display Card • Monochrome Monitor • One Serial Port and Parallel Port • Software Bundle • Color Monitor Option Available.
Purchase Price: \$1,375
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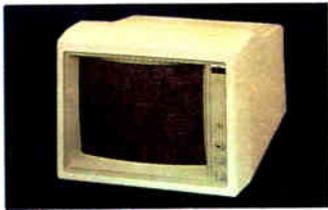
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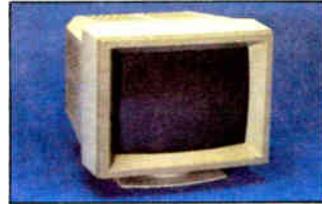
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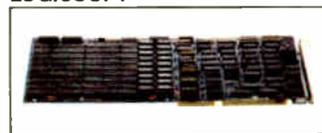
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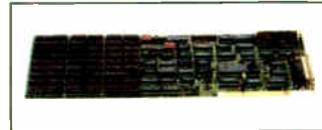
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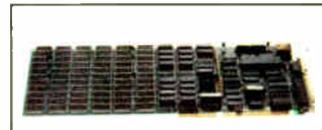
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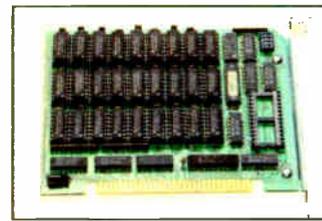


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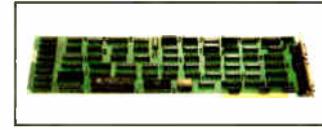
GRAPHICS BOARDS

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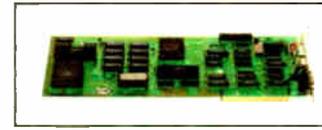
ORCHID Turbo EGA \$569
Evergraphics \$106

HERCULES Monochrome Graphics Card \$199
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TECMAR Graphics Master \$475
EGA Master \$275

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5251-11 \$609

DCA IRMA Board \$779

MODEMS

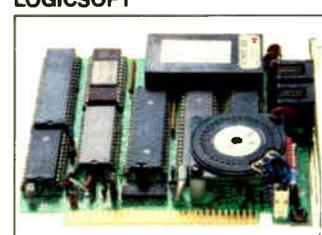
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EVEREX Evercom II \$149

HAYES Smartmodem 1200 \$389
Smartmodem 1200B w/Smartcom II \$359



Smartmodem 2400 \$559
Smartmodem 2400B w/Smartcom II \$559

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Logic (Hayes Comp.) 1200 Baud External Modem \$169
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Logic 2400B Internal Modem 2400B w/Software \$299

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Bernoulli Box (20 Mb) \$1799
Bernoulli Box (20 + 20) \$2499
Bernoulli Box Plus \$4199

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Tandon TM-100 360 K 1/2 Ht \$95
Toshiba 360 K 1/2 Ht \$109

BACK UP POWER SUPPLIES

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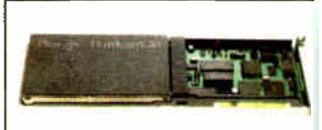
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EVENTS AND CLUBS

April 1987

EVENTS

1987 East Coast Logo Conference, Arlington, VA. Jean-Paul Emard, Meckler Publishing, 11 Ferry Lane West, Westport, CT 06880, (203) 226-6967. *April 2-4*

CHI and GI '87: Special Combined Conference on Human Factors in Computing Systems and Graphics Interface, Toronto, Ontario, Canada. Wendy Walker, Conference Coordinator, CHI & GI '87 Conference Office, Computer Systems Research Institute, University of Toronto, 10 Kings College Rd., Room 2002, Toronto, Ontario, Canada M5S 1A4, (416) 978-5184. *April 5-9*

Fourth Annual International Conference on Technology and Education, Fort Worth, TX. Fran McGehee, Marketing Information, Tandy Corp./Radio Shack, 1800 One Tandy Center, Fort Worth, TX 76102, (817) 390-3487. *April 7-9*

Satellite Communications Status '87: Technology, Applications, and Markets, New York, NY. Susan Smith, Industry Representative, Frost & Sullivan Inc., 106 Fulton St., New York, NY 10038, (212) 233-1080. *April 9-10*

Type-X '87, New York, NY. TypeWorld Exhibits, P.O. Box 170, Salem, NH 03079, (603) 898-2822. *April 9-11*

Twentieth Small College Computing Symposium, St. Paul, MN. Dr. G. Michael Schneider, Department of Computer Science, Macalester College, 1600 Grand Ave., St. Paul, MN 55105, (612) 696-6287. *April 10-11*

RAINBOWfest, Schaumburg, IL. Rainbow Magazine, The Falsoft Building, 9509 U.S. Highway 42, P.O. Box 385, Prospect, KY 40059, (502) 228-4492. *April 10-12*

Trenton Computer Festival '87, Ewing Township, NJ. Department of Electronics Engineering Technology, Trenton State College, Hillwood Lakes, CN4700, Trenton, NJ 08650-4700, (609) 771-2487. *April 11-12*

Alaska Association for Computers in Education (AACED '87), Anchorage, AK. Dennis Dempsey, AACED Conference Chairman, Homer High School, 600

East Fairview Ave., Homer, AK 99603, (907) 235-8186. *April 16-18*

Perscomp '87, International Conference on Personal Computers, Sofia, Bulgaria. Dr. Marcel Israel, ITKR/BAN, Acad. G. Bonchev Str., bl.2, 1113 Sofia, Bulgaria. *April 21-24*

CADDM '87: First International Conference on Computer Aided Drafting, Design and Manufacturing Technology, Beijing, China. Automation Technology Institute, P.O. Box 242, Pebble Beach, CA 93953, (408) 624-5892. *April 21-25*

Artificial Intelligence and Advanced Computer Technology Conference and Exhibition, Long Beach, CA. Tower Conference Management Co., 331 West Wesley St., Wheaton, IL 60187, (312) 668-8100. *April 22-24*

Integrating On-Line Communication Technologies: Bringing the World to Your School, Stillwater, OK. Connie Lawry, Assistant Director, Education Extension, Oklahoma State University, 108 Gundersen, Stillwater, OK 74078, (405) 624-6254. *April 23*

1987 Annual Systems Conference, Louisville, KY. Richard B. McCaffrey, Association for Systems Management, 24587 Bagley Rd., Cleveland, OH 44138, (216) 243-6900. *April 26-29*

Seventeenth International Symposium on Industrial Robots, Chicago, IL. Paula Harrington, Society of Manufacturing Engineers, One SME Dr., P.O. Box 930, Dearborn, MI 48121, (313) 271-1500, extension 297. *April 26-30*

DEXPO South 87: Twelfth National DEC-Compatible Exposition, Nashville, TN. Expoconsul International Inc., 3 Independence Way, Princeton, NJ 08540, (609) 987-9400. *April 28-30*

If you send notice of your organization's public activities at least four months in advance, we will publish them as space permits. Please send them to BYTE (Events and Clubs), One Phoenix Mill Lane, Peterborough, NH03458.

CLUBS

European PROFS (Professional Office System—IBM) User Group, PROFS Secretary, Rutherford Appleton Laboratory, Chilton, Didcot, Oxfordshire OX11 0QX, United Kingdom, 0235-21900, extension 6456.

System Operators Quarterly (SOQ) club, send SASE to Brett W. Wagner, 1375 South Lyn Circle, South Euclid, OH 44121.

Hi Society, newsletter of Houston's Epson Users Society; QX-10 Users, Epson Users Society, P.O. Box 37049, Houston, TX 77237.

Apple Fontrix Club, for users of Fontrix from Data Transforms of Denver; P.O. Box 29857, Thornton, CO 80229-0857.

Sacramento Amiga Computer Club (SACC), P.O. Box 19784, Sacramento, CA 95819-0784, (916) 944-7400.

NEC PC-8000 Users Group of QLD, David Clark, P.O. Box 281, Upper Mt. Gravatt, 4122, Queensland, Australia.

The Catalyst BBS, 4 Teddington Rd., Rondebosch 7700, South Africa, (012) 69 2792.

Charleston Amiga Users Group, 1030 Ft. Sumter Dr., Charleston, SC 29412, BBS: (803) 571-6030.

Color Computer-Milwaukee Users Group (CoCo-Mug), John Dais, 3784 North 73rd St., Milwaukee, WI 53216.

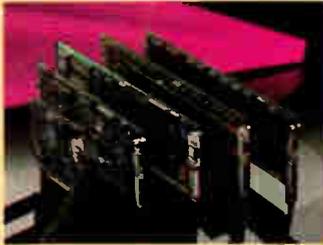
SPE Microcomp News, the newsletter of the Society of Petroleum Engineers (SPE) Microcomputer User Group; P.O. Box 833836, Richardson, TX 75083-3836.

Micropsy, users group for use of computers in psychology, counseling, therapy, and research; Martin Schaaf, 32 Crest Rd., San Anselmo, CA 94960.

Investors' User Group, 2252 Main St., Suite 15, Chula Vista, CA 92011, (619) 423-0538.

Between Bytes, journal of the Jersey Atari Computer Society (JACS); P.O. Box 710, Clementon, NJ 08021. ■

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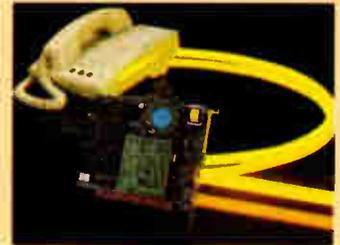
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- Runs with multi-line phones

Evercom 12 Modem

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- Hayes and Bell 212A compatible
- Supports tone and pulse dialing
- Automatic answer and voice/data switching
- Bitcom software included



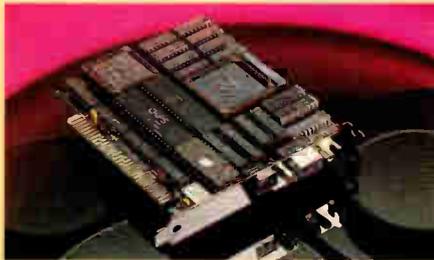
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Excel Stream-20



Evercom 24



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Excel Stream-60



Evercom 12



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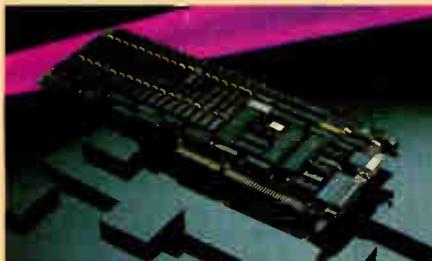
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ASK BYTE

Conducted by Steve Ciarcia

Modems Can't Wait

Dear Steve,

A few nights ago, a friend and I were discussing an annoying problem: the interaction between call waiting and modems. Call waiting is very nice to have, but if I am accessing another computer through my modem when a call waiting signal comes through, I usually end up getting disconnected.

Is there a way to filter out the call waiting signal before it reaches the modem? Also, I would like to find out more about the telephone system; can you recommend any sources?

Robert Wayment
Fairfax, VA

I have received a number of letters from modem users with the same complaint. At present, there is nothing you can do to eliminate the problem short of dropping the call waiting feature or having a second phone line installed without call waiting.

A device to filter out the call waiting signal during a data communication session would require some complex filter design and intelligence—some of the tones used during data communications can approximate those used by call waiting. The device would have to know if a tone belonged to the data stream or to the call waiting signal.

The easiest publication on telephone electronics to obtain (and the most affordable) can be purchased at your local Radio Shack for \$3.49: Understanding Telephone Electronics (item number 62-1388). The book was originally developed and published by the Texas Instruments Learning Center.—Steve

Above Board Incompatibility

Dear Steve,

I bought an Intel Above Board PS a few months ago to use in my Zenith 158 computer. It works perfectly at 5 MHz, but at 8 MHz it decides that there is no expanded memory present and refuses to load the device driver.

Zenith was unable to help, since they were unfamiliar with the board, and it obviously wasn't a problem with the computer. Intel simply said the board isn't designed to work at 8 MHz and that I should just use it at 5 MHz.

This is obviously a poor solution, since

it forces me to use the computer at less than its full capability, not to mention the additional expense I incurred buying the 8-MHz 8087.

Even though the computer uses 150-nanosecond chips, I tried 120-nanosecond chips in the Above Board to see if they would work, but with no success. Can you suggest what else to look for on this board that might be causing the problem? Obviously, something on it will not work at 8 MHz.

George W. Snavely Jr.
Ponca City, OK

I've heard several reports of problems with expanded storage boards failing at higher clock speeds. Now that IBM has come out with an official 8-MHz AT board, manufacturers are scrambling to make the changes necessary for proper operation with the faster clock, but that doesn't help you any.

It is not a simple matter to tweak a board to run 33 percent faster than the original design. Changing the RAMs was a good first shot at the problem, but nothing else is that easy, particularly because the logic chips are soldered in place. You could very well wind up with a mutilated board that works neither fast nor slow.

In short, I think that the only practical thing you can do is sell the board and buy one that's rated for 8 MHz. The June 10, 1986, issue of PC Magazine reviewed 11 expanded memory boards but didn't mention which would work at 8 MHz. I'd hope that a phone call to the vendors would sort things out, but the key is to make the call before plunking down the money.—Steve

Quad-Density PC Floppy

Dear Steve,

How difficult is it to add a quad-density floppy drive to an IBM PC running PC-DOS version 3.0? What additional hardware or software would be required?

Jack Locascio
SHAPE, Belgium

Adding a quad-density drive to a PC isn't difficult at all. You need only replace the disk controller card with one that can handle the drives, install a device driver to control the controller, connect the drives, and you're on the air. Such con-

trollers usually come with software for the driver on a floppy disk so you won't have to write any code.

Two words of caution are in order: First, you'll need to buy quad-density (IBM calls them "high-capacity") floppy disks to use the new drive at 1.2 megabytes. Second, you won't be able to write disks for use in 360K-byte drives even if you format them for 360K. The problems come from the size of the read/write head (it's much narrower) and the strength of the magnetic field (it's a lot weaker) of the quad-density drives as compared to standard drives.

Tall Tree Systems markets a package called JDiskette for PCs that will probably do the trick. You can connect your old 360K drives to the new controller as well as a new 1.2-megabyte drive, but you may have trouble with space for three drives in your PC's enclosure (the 1.2-megabyte byte drives are half-height). You could shoehorn up to four half-height drives into a stock IBM PC, but you'll have to upgrade the power supply to handle the extra load.

There are some complexities in the software that make using the quad-density drives something more of a hassle than you might expect, but these may have been worked out since the review I read last year. It's probably worthwhile to buy a manual first to make certain that you'll like what you're getting into.

continued

IN ASK BYTE, Steve Ciarcia answers questions on any area of microcomputing. The most representative questions received each month will be answered and published. Do you have a nagging problem? Send your inquiry to

*Ask BYTE
c/o Steve Ciarcia
P. O. Box 582
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News about the Microsoft Language Family

New FORTRAN Compiler Uses Microsoft® C Code Emitter and Optimizer

Microsoft FORTRAN Optimizing Compiler Version 4.0 was redesigned to take advantage of the innovative optimizer and code generator technology of Microsoft C Compiler Version 4.0. We have taken the C optimizer and added loop optimizations. These enhancements result in the fastest execution and smallest, most efficient code size for MS-DOS® FORTRAN programs. The compiled code generated by Version 4.0 is 17% faster on the Sieve benchmark and 220% faster on the Lookup benchmark than our nearest competitor.

Compile-time switches let you choose the level of optimization. The compiler can optimize for execution speed or for code size. Optimization can be turned off altogether in the early development stages to speed up compilation.

The new compiler supports a wide range of math libraries. You can produce in-line 8087/80287 instructions for fast execution or emulate the math co-processor if it is not present. On non-8087/80287 systems, the alternate math package is provided for more speed but less accuracy (64 bit) than the IEEE math standard (80 bit).

By default, the FORTRAN compiler uses the instruction set for the 8086/8088 processor. Programs can take advantage of the more powerful instruction sets of 80186/80188/80286 processors by turning on a switch option when compiling.

New Microsoft FORTRAN Optimizing Compiler Gains GSA Certification at Highest Level

Now, Microsoft FORTRAN Optimizing Compiler Version 4.0 is Full ANSI FORTRAN 77. The General Services Administration (GSA) has certified it at the highest level without any errors. We have gone beyond ANSI FORTRAN 77 by adding IBM® VS and DEC® VAX® FORTRAN extensions to simplify porting to and from these environments.

Medium and huge memory models have been added to the existing large memory model support. The medium memory model allows programs with up to 1 megabyte code to access 64K of data. The huge model lets you write programs with up to 1 megabyte each for code and data and arrays larger than 64K. You may mix memory models in your programs by the use of NEAR, FAR and HUGE keywords to make the most efficient use of memory. For example, you could create a medium model program and declare a huge array.

Microsoft CodeView™ Debugger Included Free with the New Microsoft FORTRAN Optimizing Compiler

The innovative windowing debugger that was included in Microsoft C Compiler has been added to our new FORTRAN package. Now, Microsoft CodeView lets you debug using your FORTRAN source or disassembled code or both intermingled. You can watch and change the values of your local and COMMON variables as you debug. You may set the conditional breakpoints on variables, expressions, or memory. Trace and single step through the execution of your FORTRAN application. Watch and change registers and flags as you execute. Program and CodeView screen I/O are kept separate so you can easily debug graphics programs. You may view the program output on two separate monitors or through screen swapping on a single monitor.

In addition to CodeView, Microsoft FORTRAN Optimizing Compiler Version 4.0 includes a number of other utilities, such as the new program maintenance utility (MAKE) that rebuilds your applications after your source files have changed, a faster overlay linker, a library manager, an EXE file compression utility, an EXE file header utility, and an MS-DOS environment setting utility.

Version 4.0 has the most complete set of diagnostic error messages available on a FORTRAN compiler for the MS-DOS operating system (almost twice as many as our competitors). The comprehensive documentation, separated into three manuals, is brand new with non-ANSI extensions highlighted in blue to stand out from the rest of the text.

For more information on the products and features discussed in the Newsletter,
write to: Microsoft Languages Newsletter
16011 NE 36th Way, Box 97017, Redmond, WA 98073-9717.
Or phone:
(800) 426-9400. In Washington State and Alaska,
call (206) 882-8088. In Canada, call (416) 673-7638.

Latest DOS Versions:

Microsoft C Compiler	4.00
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Microsoft Pascal	3.32
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Microsoft®

Look for the Microsoft Languages Newsletter every month in this publication.

For more information, contact

Tall Tree Systems
P. O. Box 50690
Palo Alto, CA 94303
(415) 493-1980

Back in 1985, the controller card, a drive cable, and software cost \$250. The 1.2-megabyte drive is not included, so you'll have to do some shopping in the back pages of BYTE. If Tall Tree also supplies the drives, I'd suggest you buy a complete package from them to avoid problems.—Steve

Right to Left

Dear Steve,

I am an archaeologist connected with a foundation that is currently doing most of its fieldwork in the Middle East. As part of the research and publication requirements connected with our work, we are required to produce Arabic translations of the reports on our research. Up until now we have had this publication done in Cairo. This has created problems for us regarding control of the publication schedule and quality control, not to mention communication problems over such a long distance.

With the increasing popularity of laser printers, we have considered obtaining an Arabic font and producing our publications in the United States, saving us much time and cost in the publication process. We have access to an excellent Arabic font, but the Arabic language is read from right to left and we have been unable to locate a word processing system that would allow us to produce the text in right-to-left format.

I have an IBM PC with 256K bytes of memory and would be willing to purchase a laser printer that would be capable of this task if I could find a right-to-left word processing system. I would appreciate any information you could give me.

Jeffrey A. Blakely
Nashville, AR

These people may be able to help:

Gamma Productions Inc.
710 Wilshire Blvd., Suite 609
Santa Monica, CA 90401
(212) 394-8622

I saw their advertisement for Multi-Lingual Scribe recently. It is supposed to handle right-to-left and left-to-right text

in Arabic (among other languages) with vowel points and whatnot. I'll admit to being a little out of my depth on this one. While the advertisement did not mention laser-printer support, it's probably on their list of things to do.—Steve

Apples and Pertecs

Dear Steve,

There is not much literature on personal computers here in Chile, so I have several questions that I hope you can answer.

What is the best way to expand the memory of an Apple II+ from 64K bytes to 128K bytes? How can I do this and also upgrade to a 65816 microprocessor?

Also, what disk operating system is used by the Pertec 2000 model 4202 computer (manufactured by Pertec Computer Corp.)? Is it compatible (or can it be made compatible) with a more standard computer system?

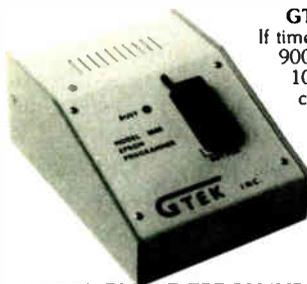
Finally, is it possible to replace the 8085A processor in the Pertec computer with an 8088 processor?

Juan Luis Espinoza Valledor
Arica, Chile

Several companies currently manufacture add-in memory cards for the Apple

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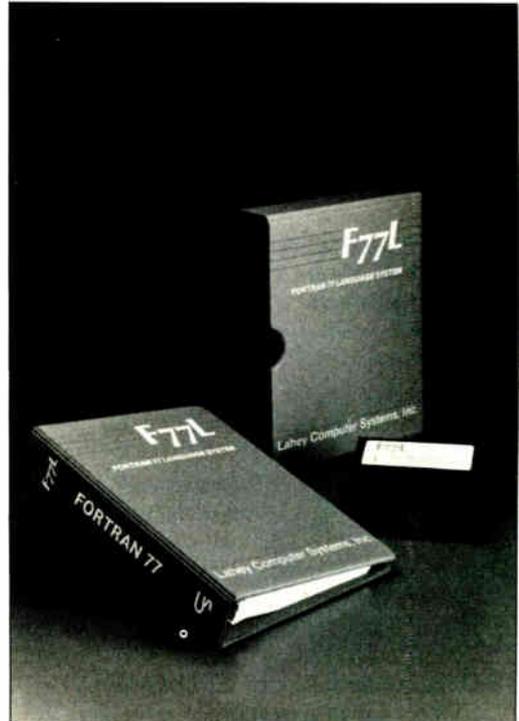
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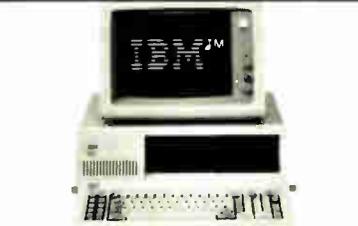
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11+. These cards range in capacity from about 64K bytes up to several megabytes, although 256K or 512K is a common size. Because of the 64K address space of the 6502 microprocessor, these cards must be either bank-switched in segments or utilized as RAM disks.

Some of the manufacturers that make add-in RAM cards also produce add-in cards that contain a 65816 microprocessor. Most of these combinations are designed only for use in the Apple IIe. Applied Engineering (P.O. Box 798, Carrollton, TX 75006, (214) 241-6060) makes a card called the RamFactor for the II+, which is available with a piggy-back card containing a 65816 processor. The combination of these two cards would give you extended memory and a 65816 processor in one package.

The Pertec 2000 model 4202 uses a proprietary operating system. As far as I can determine, it is not directly compatible with any other system, and conversion is likely to be impractical. Likewise, changing to an 8088 microprocessor might be possible, but not practical. You would have to make significant hardware modifications and you would have to adapt another operating system to work on the machine or, worse, write one from scratch. —Steve

CIRCUIT CELLAR FEEDBACK

Lis'ner 1000

Dear Steve,

I am a biomedical engineering student at the Western Australian Institute of Technology. I am working on a speech-recognition and text-to-speech synthesizer system to enable speech- and hearing-impaired people to use a telephone.

I found your article "The Lis'ner 1000" in the November 1984 BYTE to be most useful and interesting because you have demonstrated for the first time the construction of a speech-recognition system based on a general voice-recognition IC. Since you have special knowledge in this field, I was wondering if you could give me some advice and information on the latest developments in speech-recognition chips. I would also like to know of any further developments to the Lis'ner 1000.

I am involved with a firm in Western Australia that is very interested in low-cost speech-recognition systems for their products and I know some students working on speech-recognition systems for their projects in robotics. Your advice would be most appreciated.

K. S. Strasser
Perth, Western Australia

First of all, I have no further plans to enhance or modify the Lis'ner 1000 project for now.

To keep up to date on chips and components, there are a number of good references that will assist you. First, IC Master, published by Hearst Business Communications Inc., contains, in a two-volume set, specifications for virtually every IC currently available. While this contains a lot of information you might not need, it does contain references and sources for speech chips in current production with manufacturer's data and contact information. The books are updated yearly and cost about \$125. The Application Note Directory is particularly valuable, as it lists hundreds of available design papers from IC manufacturers, each one a complete project in itself.

Also, many of the component-related electronics magazines, such as EDN, Electronic Products, and Electronics, carry announcements and articles on new chips. —Steve

Career Planning

Dear Steve,

Upon reading your article about data encryption in the September 1986 BYTE, I noticed the section in which you gave your qualifications. I am a junior at Vanderbilt University studying electrical engineering and I am very interested in going into digital design and applications. I am particularly interested in computer and microprocessor control. Since these areas seem to be a major part of your experience, I wonder if you could offer any advice? Is there any special education or experience that I should pursue to make myself more marketable?

Richard Stahl
Nashville, TN

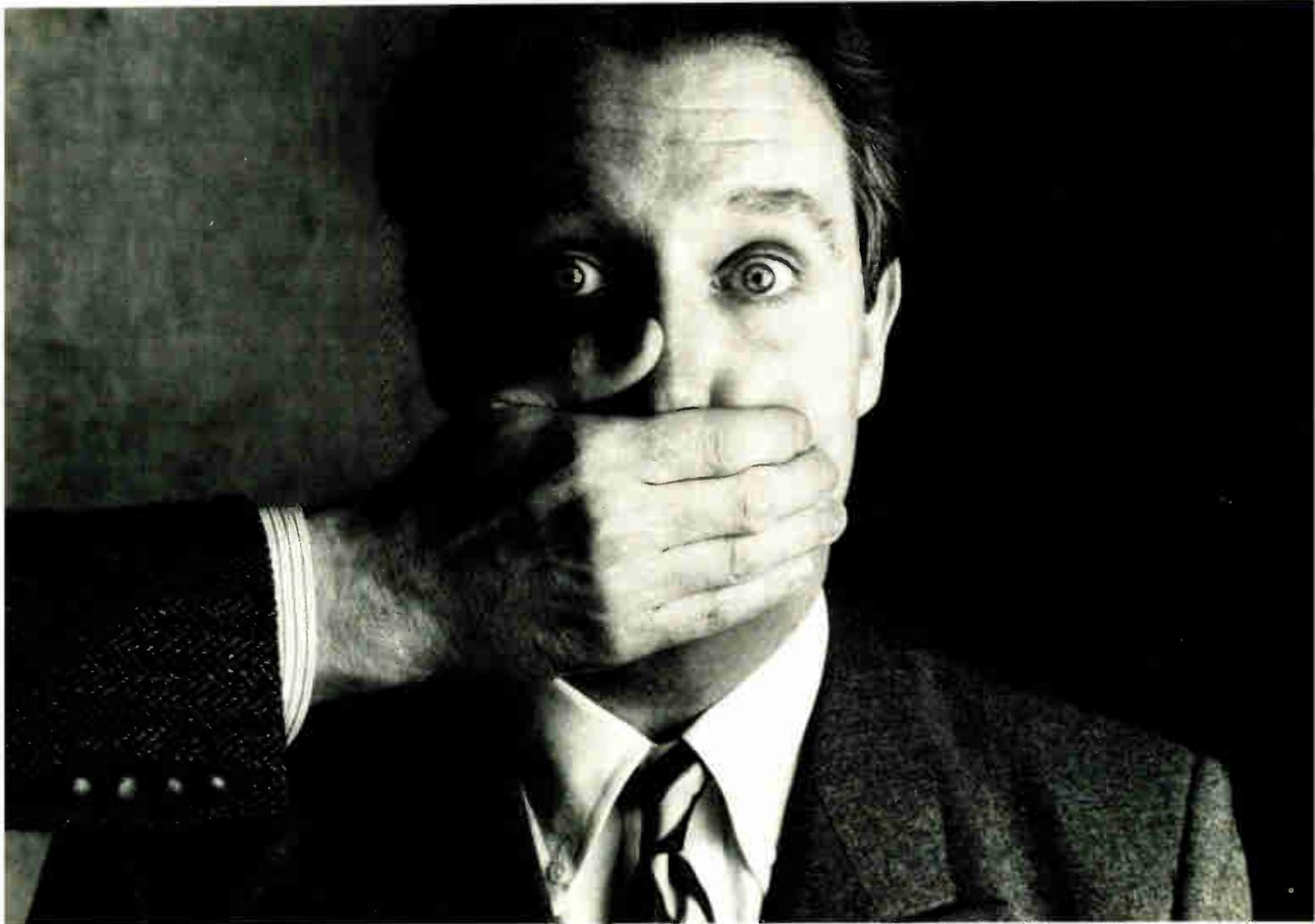
The harsh fact is that most of the detailed subjects you study will be out of date in about five years. Any marketable skills you learn will age much faster than you do.

You should concentrate on engineering fundamentals but not specialize in any particular area. Learn a little about control systems, something about microwaves, and perhaps a bit more about computer program design. The advantage you'll have over a narrow specialist is that you'll be able to tackle nearly any job; perhaps not as well initially, but you won't be lost at sea.

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find that a lot of people can't do it very well.

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You might want to sign up with the IEEE as a student member. They publish a lot of useful journals that cover state-of-the-art developments, and the prices are reasonable enough that you can subscribe to some that will keep you in touch with other fields. I'm sure there's a chapter at Vanderbilt, so you won't have any trouble finding them.—Steve

BBSs and the Law

Dear Steve,

I am currently a student at UCLA Law School and am writing an article concerning computer bulletin boards and the First Amendment. I recently read your article "Turnkey Bulletin-Board System" in the December 1985 BYTE. In it you stated: "These activities [the misuse of public bulletin-board systems by phreaks, pirates, etc.] have spurred many state legislatures and the U.S. Congress to pass a variety of laws aimed at restricting the activities of bulletin boards (an extensive discussion on this topic, complete with voluminous source data, is available on BIX under 'BBS/other' and 'tele.policy' conferences)."

I am unfamiliar with the various databases and bulletin boards, and I don't have a modem. Therefore, I am writing to ask if you have a copy of these sources or know of a way I could obtain them. Is BIX a widely accessible bulletin board? I would appreciate any help you could give me concerning legislation or court cases on bulletin boards.

Eric Jensen
Los Angeles, CA

BIX is the BYTE Information Exchange and is a large teleconferencing system operated by BYTE magazine. The system is available to anyone by subscription and features over 140 computer-related topics and special conferences on a variety of current events and new technologies.

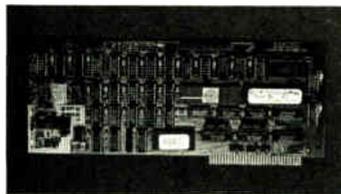
By the way, the conferences that are mentioned in the quote are now a bit dated. Places you'd look for discussions on this subject, in addition to the BBS conference, are teleco.digest, networks, and packet.net.

Further BIX information is available in any recent issue of BYTE or from

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You'll need your own modem and a terminal or microcomputer to access the materials on BIX. The articles are protected by copyright, but you can download them for personal use. —Steve

Sound-Activated Switches

Dear Steve,

Do you have any information on com-

mercially available sound-activated switches? I am particularly interested in switches that provide contact closure and those with a sensitivity threshold that can be programmed.

Steve Newman
Santa Clara, CA

A commercially available sound-activated switch with adjustable sensitivity is available from Radio Shack (part number 277-1011) for \$4.95.

However, if by "programmed" you mean through software, then this inex-

pensive circuit won't do unless you are willing to modify it.

If your needs are not too complex, then you could replace the sensitivity adjustment control with a network of resistors and low-voltage reed relays. Assuming that your computer can control external switches or relays (with some sort of external I/O controller board), then this would be easy. A 4066 CMOS switch and resistor network would do nicely. A good reference for this type of circuit is The CMOS Cookbook by Don Lancaster (Howard W. Sams, 1977).

Since you haven't specified just how sensitive you need this switch to be and over what frequency range it will operate, it's hard to suggest anything more specific. For commercial sources of this type of circuit, check companies that supply burglar alarm equipment. Mountain West (4215 North 16th Street, P.O. Box 10780, Phoenix, AZ 85064-0780) is one such mail-order firm. You might check the listings in your phone directory for other sources. —Steve

Talk to Me, Computer

Dear Steve:

I've just built a speech synthesizer that I've interfaced to my IBM PC. The heart of this synthesizer is the ever-popular General Instrument SP0256A-AL2. This chip produces words by concatenating allophones. The circuit is simple and the synthesizer produces sound that is good enough for my needs. What I would really like now is a piece of software that translates text files to phonemes. And if the source code was available, I'd sell my soul to get my hands on it!

Patrick Beauchemi
Westmount, Quebec, Canada

I'm not aware of any code readily available to perform the conversion you're interested in, but I can recommend one book that will put you on the right course: Principles of Computer Speech by Ian H. Witten (Academic Press Inc., 1983).

Mr. Witten is from the University of Calgary in your native Canada. The book gets rather involved with various forms of speech-synthesis theories and analyses needed for a good understanding of the subject.

Many of the past Circuit Cellar articles that deal with speech-synthesis projects are available in book form from BYTE Books. Volume 4 of Ciarcia's Circuit Cellar contains an excellent description of the text-to-speech algorithm in the article "Build the Microvox Text-to-Speech Synthesizer, Part 2: Software." Contact: BYTE Books, McGraw-Hill Book Company, P.O. Box 400, Hightstown, NJ 08250. —Steve ■

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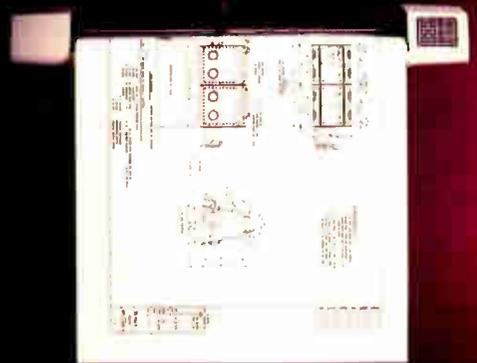
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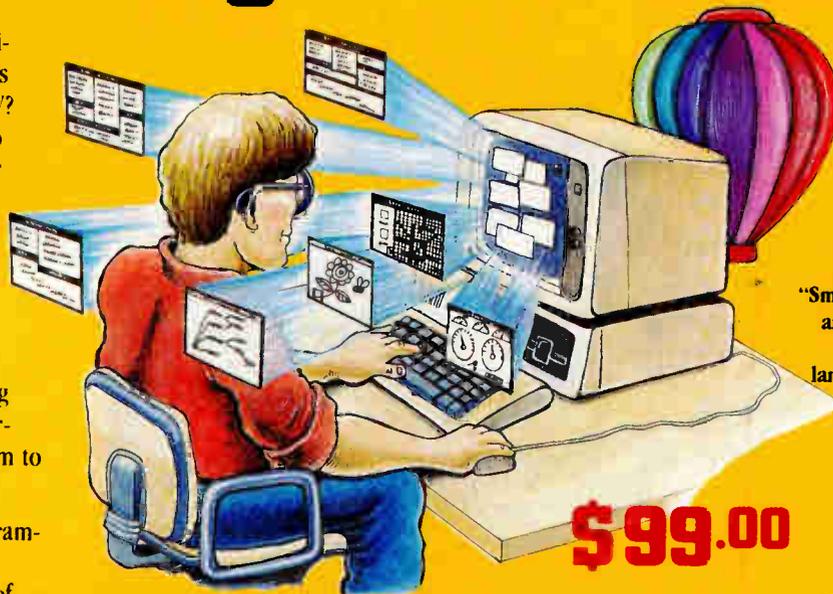
*John C. Dvorak,
Contributing Editor, PC Magazine*

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*Dr. Paul Soper, Senior Specialist
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*Dr. Barry Fishman, Sr. Project Engineer
Hughes Aircraft Company*

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BOOK REVIEWS

REDUCED INSTRUCTION SET COMPUTERS

William Stallings, ed.
IEEE Computer Society Press
Washington, DC: 1986
ISBN 0-8186-0713-0
471 pages, \$44

THE DESIGN OF THE UNIX OPERATING SYSTEM

Maurice J. Bach
Prentice-Hall Inc.
Englewood Cliffs, NJ: 1986
ISBN 0-13-201799-7
471 pages, \$37.33

THE ART OF PROLOG: ADVANCED PROGRAMMING TECHNIQUES

Leon Sterling and
Ehud Shapiro
MIT Press
Cambridge, MA: 1986
ISBN 0-262-19250-0
427 pages, \$29.95

REDUCED INSTRUCTION SET COMPUTERS

Reviewed by
Phillip Robinson

The designers of today's central processors have tried to increase system performance by implementing more and more processing elements in hardware, leading to CISC (complex instruction set computers). Proponents of RISC (reduced instruction set computers) claim that smaller processors with many general-purpose, on-chip registers and small, hard-wired instruction sets will be able to run rings around complex processors. What's more, the design of such chips will be less difficult, time-consuming, and expensive than the design of CISC chips. Wringing the speed out of smaller instruction sets requires more advanced compilers to optimize instruction and register usage.

RISC originated in a project at IBM (which resulted in the IBM 801, a machine that was not sold commercially) but was reborn at the University of California at Berkeley and at Stanford University. David A. Patterson and John L. Hennessy showed that small groups of graduate students and professors could design extremely fast, easily manufactured, 32-bit processors in a relatively short time. Their studies caught the attention of computer firms, and soon start-up companies and old-timers (including IBM and Hewlett-Packard) were building



RISC machines. During 1986, a number of these machines were announced and were actually shipped. At the same time, CISC-oriented designs still dominated the market. Lively debates sprang up between those who saw RISC as the wave of the future and those who just thought it taught a few lessons that could be incorporated into the mainstream of system design. Who is right? Until recently, the only way to hear the sides in the RISC debate was to read business magazines or to plow through the high-end technical literature at conferences and in journals. *Reduced Instruction Set Computers*, edited by William Stallings, is one of the first books to strike some sort of middle ground.

Nature of the Book

A banner across the front of this book proclaims *Tutorial Tutorial Tutorial*. . . Unfortunately, that isn't an accurate description of the text. Instead, this is a collection of important papers about RISC with some introductory essays, a glossary, and a bibliography. The 32

papers were originally published between March 1977 and June 1986. Some come from journals ranging from *Communications of the ACM* to *Datamation*. Almost a third come from conference proceedings (including four from the famous COMPCON Spring '86 RISC-CISC shootout) and IBM publications, and one comes from a book on RISC for VLSI.

The book includes articles by some of the big names in RISC: John Cocke, John L. Hennessy, David A. Patterson, Carlo H. Séquin, and Joel S. Birnbaum. C. Gordon Bell is here siding with the RISC philosophy because of the current speed of logic relative to memory, and Manolis Katevenis is represented by a chapter from his ACM award-winning dissertation on RISC.

Many important RISC machines are also represented, including the IBM 801 and RT, Stanford MIPS chip, Berkeley RISC chips, HP Spectrum series, MIPS 32-bit CMOS chip, and the Intel 80386. (Whoops: the 386? I thought that was a mistake at first, too. Turns out it was added as an example of the state of the art in CISC processors.)

The papers are organized by topic into six sections titled "In-

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struction Execution Characteristics," "RISC Overview," "Optimized Register Usage," "RISC Compilers," "Example Systems," and "An Assessment of RISC." Each section has an introductory essay written by the editor. Some of these essays are lucid, illustrated introductions to the particular topic at hand. Others are single-page summaries of the articles within the section.

At the end of the book is a glossary, a list of acronyms, and an annotated bibliography. These sections are generally helpful, and the bibliography is definitely thorough.

Legibility and Selection

The text is always legible, though the print quality varies quite a bit. Each article has been lifted directly from its original source, and some of the reproductions are rougher than others. The technical level of the articles covers quite a range, too. "Strategies for Managing the Register File in RISC" by Yuval Tamir and Carlo H. Sequin is chock-full of mathematical analyses and ends with a mathematical proof that occupies three full pages. Another type of article is represented by "RISC: Back to the Future?" by C. Gordon Bell, a straightforward, historical account of RISC-like principles throughout the last 30 years of computer design. Bell's article requires little technical knowledge of the reader but offers a total historical perspective.

As I mentioned before, many of the important names in RISC research and development are represented in this book. Also, the section on example systems does a creditable job of covering the spectrum of RISC machines. The organization of articles couldn't be improved, and the introductory essays help to set the context for each section. The bibliography will be a boon to anyone researching the technical aspects of RISC.

The most fun section of the book is the final "An Assessment of RISC." Within this hundred pages is a taste of the debate about RISC's impact now and its probable future. The articles come from both the skeptical side and the advocacy side, and they include some of the direct back-and-forth that appeared in the "Open Channel" column in *IEEE Computer* magazine. These articles and columns argue about RISC instead of just describing it in technical, measured tones. They criticize and analyze such famous processors as the doomed iAPX432 from Intel and the MicroVAX.

Drawbacks

The biggest problem with this collection is what was left out. Most important is the lack of reference to the convergence of gallium arsenide (GaAs) technology and RISC designs. As I discuss in my article on RISC (see page 143), GaAs RISC processors can reach speeds of 100 MIPS, an order of magnitude greater than the current silicon RISC chips.

I was also disappointed by the limited space allotted to articles on register usage and RISC compilers. Proper compiler design is really a crux in many RISC designs, and the three articles in that section leave me still hungry for more. I'd also like to see some discussion and analysis of so-called hybrid processors. These new, important chips—such as the Fairchild Clipper and the Inmos Transputer—claim to combine the best of RISC with the best of CISC.

A Solid Collection

Although the fundamental element of RISC processors seems simple—a smaller, more efficient instruction set will yield faster computers—the practicalities of implementing an improved computer system using a RISC CPU are not simple. They involve complex questions of compiler design and register usage. This book does not pretend to teach state-of-the-art RISC system design. Instead, it is a well-rounded collection of articles

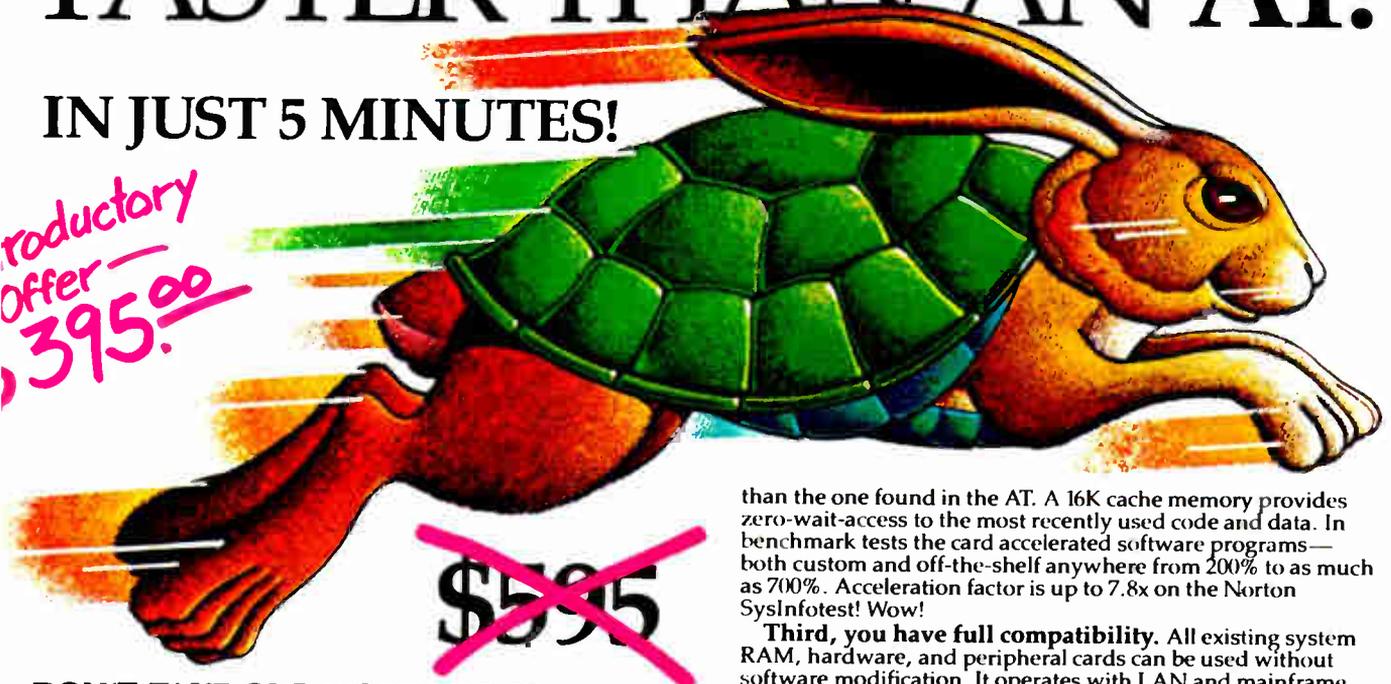
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Second, it is advanced. The *BREAKTHRU 286* replaces the CPU of the PC or XT with an 80286 microprocessor that is faster

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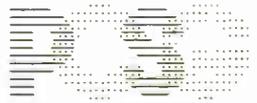
Third, you have full compatibility. All existing system RAM, hardware, and peripheral cards can be used without software modification. It operates with LAN and mainframe communication products and conforms to the Lotus/Intel/Microsoft Expanded Memory Specification (EMS). Software compatibility is virtually universal.

Fourth, it is the best there is. There are several other boards on the market. Some are priced about the same as the *BREAKTHRU 286* and some are cheaper. We at PCSG have compared them all, but there simply was no comparison. What we discovered is that many cards being sold offer only a marginal speed up in spite of their claims. We found some to be merely versions of the obsolete 8088 or 8086, and others to be just poorly engineered. The 8MHz *BREAKTHRU 286* is unequivocally the best executed and most completely reliable speedup board manufactured today.

PCSG has since early 1983 dominated the lap portable market with ROM software such as Lucid spreadsheet and Write ROM that reviewers rated as excellent. We were proud to successfully enter the IBM PC market last year with disk access speedup software. Now we are so pleased with the *BREAKTHRU* speedup card. We use them on our own PC's to make them faster than AT's. We are really excited about this product.

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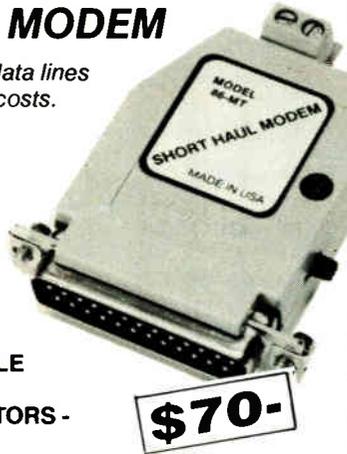


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BOOK REVIEWS

from other sources. The articles begin by describing the goals behind RISC and continue through RISC's advantages, the challenges of designing a RISC system, descriptions of current RISC machines, and prognostications of RISC implementation. It is the best collection of RISC articles I have seen, but it does have several surprising holes, especially in its disregard of the convergence of RISC and GaAs technologies. Still, I recommend it for anyone who wants to go beyond the RISC-is-coming articles in the business press and for those involved in RISC who want a good reference collection.

Phillip Robinson is a contributing editor for BYTE and editor of the Desktop Engineering newsletter. He can be reached at P. O. Box 40180, Berkeley, CA 94704.

THE DESIGN OF THE UNIX OPERATING SYSTEM

Reviewed by Thomas M. Houser

Many UNIX users will welcome the arrival of Maurice J. Bach's authoritative book on the UNIX kernel. Bach, an employee at Bell Laboratories, taught a course on the subject there in 1983 and 1984. While *The Design of the UNIX Operating System* is the only book available on the subject, it is extremely well written and as elegant as the system it describes. For those UNIX users who want more than a user's view of the system, this book is priceless.

Although many books on UNIX exist, Bach's deals specifically with the UNIX kernel. The kernel is the memory-resident portion of UNIX and was originally about 10,000 lines of C code. The kernel consists of only those functions that are required to serve critical user needs while maintaining the integrity of the system. Although both the UNIX kernel code and line-by-line commentaries are available, this book abstracts the principles and philosophy behind the system, which can be obscured by pages of linear listings. At the same time, the book is practical and includes short listings of code and/or pseudocode and major data structures to illustrate the points.

Who Should Read This Book?

Let me be slightly provocative and say anyone who programs a computer should read this book. The study of operating systems may seem a bit recondite. After all, not many of us live in the rarefied atmosphere of operating system design. However, getting a glimpse of a good software design is rewarding no matter what the application. Choices for data structures, how to decompose the problem, and awareness of trade-offs are all design problems that are difficult to teach other than by example. This exposition of UNIX is a good example that is nontrivial but comprehensible.

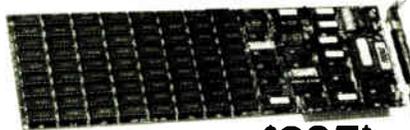
More specifically, this book could profitably be used as part of an operating systems course. It is pedagogical without being pedantic. That is, Bach is very careful to explain his terminology (e.g., when he uses the term "core" his footnote explains he means main memory, not the hardware technology). However, he does not indulge in formalisms or unnecessary abstractions. He introduces problems that appear at the end of each chapter and encourages the reader to think about the material he has presented from different angles.

Finally, any programmer who uses UNIX regularly will embrace this book and take the most from it. Bach makes many less-apparent aspects of the system clear. The book should also help readers obtain an understanding of the gestalt of the UNIX system and enable them to use it in a way that will amplify its potential.

The two major functions of the UNIX kernel are maintaining

continued

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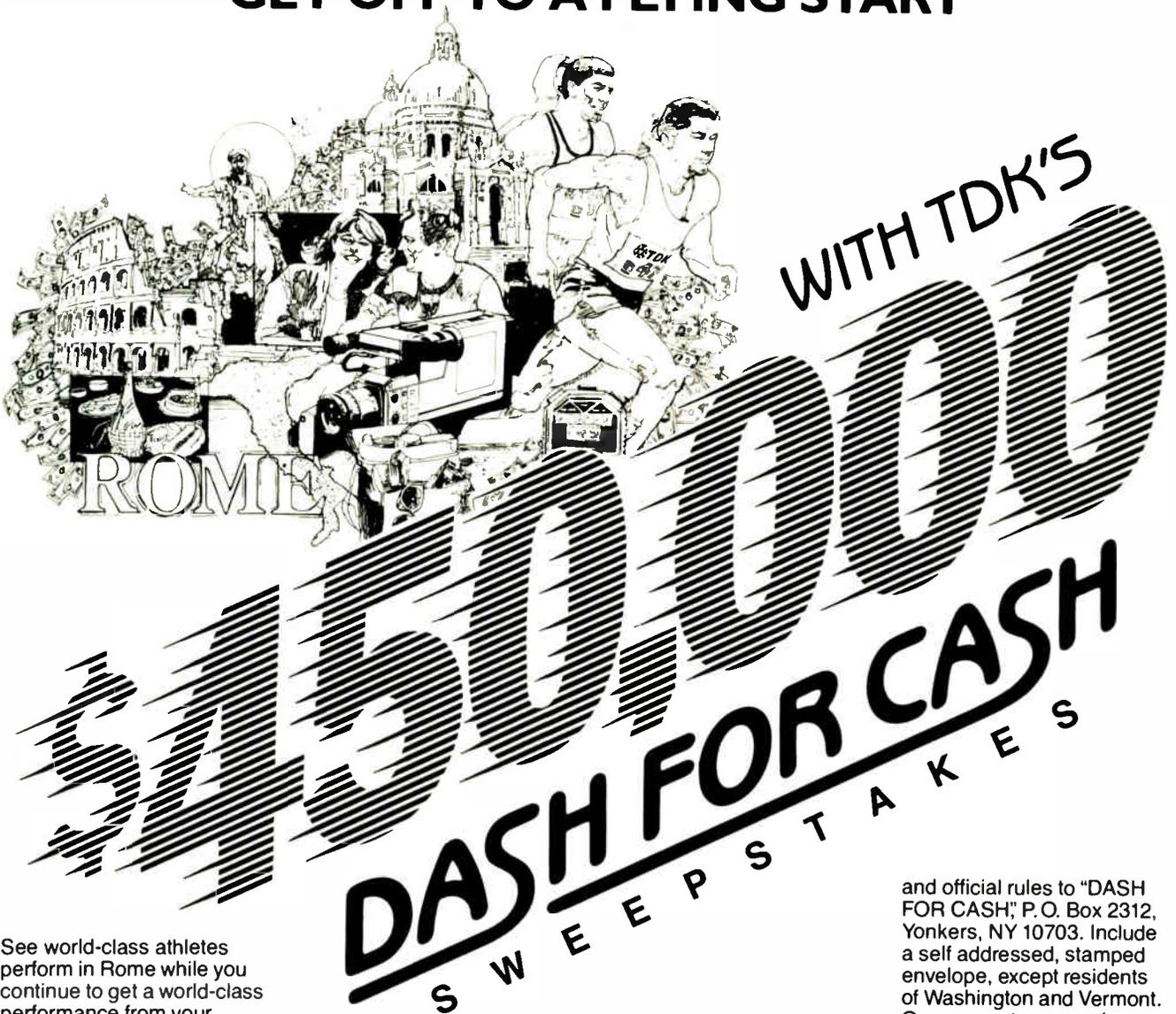
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the file system and managing processes, and these constitute the book's two main areas of exposition. In addition, a chapter on memory management covers both segmentation and paging. These are the two classic schemes and both have been used in various versions of UNIX. Another chapter also covers the new interprocess communications (IPC) facilities in Bell Laboratories' System V version—shared memory, semaphores, and messages. The two last chapters of the book are devoted to the more exotic topics of multiple processor machines and distributed UNIX.

Before jumping into the myriad details, Bach gives a lucid overview of the file and process subsystems. A discussion of files includes the organization of files in memory and the logical layout of the disk as well as the normal functions of a UNIX device driver. If you've ever pondered the meaning of "inode" or "superblock," an explanation awaits in these pages. Notice that while devices are clearly not files, UNIX abstracts the concept and attempts to treat them the same when possible. This is the kind of abstraction that leads to simpler and more reliable systems. The overview of the process subsystem describes process states, kernel and user stack, and the major data structures for managing processes (e.g., `u_area`, process table, etc.).

Bach introduces the classic "critical section" problem here. The problem, simply stated, is how to synchronize the use of one resource (e.g., a data structure) by multiple processes that may try to use it asynchronously. He presents the UNIX solution, which is simply to prevent all interruptions of critical sections of code by raising the priority level. Bach lets us in on a very interesting design choice in this chapter—all tables in the operating system have fixed sizes. This makes the algorithms simpler, faster, and more reliable. Sometimes the system administrator can tune the system accordingly so users don't run out of resources and yet table sizes are still "reasonable."

The File System

Bach uses a bottom-up treatment of the file system. He covers the file buffer cache, the internal representations of files, and level 1 input/output routines like read, write, open, close, and link.

He describes all the major data structures relevant to these topics and their interrelationships. He shows how both files and directories are represented in memory and on the disk. Algorithms to manipulate these data structures are covered both in the text and by a short (one page or less) C code segment. Where C would make the algorithm verbose, Bach resorts to pseudocode. Besides these two characterizations of the algorithms, there is almost always an example as well. This may seem like overkill, but some operating system features can be very subtle, and multiple explanations accelerate comprehension by offering the reader a choice. One thing that struck me about the file system is that two of the major data structures, the buffer pool and the in-core inode list, are very similar in structure. Bach uses clear diagrams throughout the book to describe the data structures.

Bach covers the device drivers in a later chapter. He defers this I/O topic due to the necessity of understanding process control when discussing terminal drivers. In addition, he discusses the somewhat new stream concept that implements a character driver as a stream of message-passing modules. This allows better modularization and reusability of code that implements I/O protocols that, for example, are needed in networking.

Process management is less visible to the user than file manipulation. Several classic and subtle problems arise in the implementation of multiprocess architectures such as UNIX. Bach covers all facets of process control with the same care that went into describing the I/O system: Context switch, signals, process

continued

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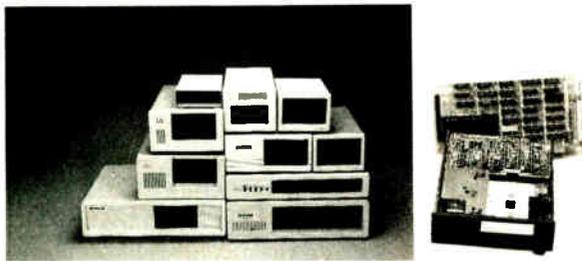
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priority, process state, child processes, process scheduling, interrupts, and system booting are all described.

UNIX's Shortcomings

Bach points out UNIX's shortcomings as well as its strengths. There are several anomalies with signals that he describes. The most severe, which I can attest to, is that signals cannot be reliably caught by the user and, in fact, can easily result in the process dying. This is simply because the default semantics of a signal are to cause a core dump (the process dies). When a user wants to catch a signal, he or she must issue a library call to do so. When the signal is issued, it gets automatically reset to its default value. A race condition is then set up. Can the user reset the signal handler before another signal comes in? If so, everything's great; if not, the process dies. Through a private conversation with Dennis Ritchie, UNIX's designer, Bach determined that in the beginning signals were only to be fatal or ignored and users were not normally expected to handle signals. Bach discusses the issue in some detail and is not too parochial to give solutions present in the Berkeley BSD UNIX, which is the other prominent UNIX.

One of the problems of UNIX has been the limited bandwidth between processes. That is, processes that need to communicate must do so through narrow channels like byte-wide pipes. Therefore, performance can be a problem. Three new features address this limitation: shared memory, messages, and semaphores. Here again, these three features are implemented using common structures internally, which facilitates their description and comprehension. Bach also discusses network communications and gives a brief but revealing discussion of the Berkeley BSD sockets concept.

What Else?

Now that UNIX is running on many manufacturers' machines, there is great interest in using it in ways for which it was not originally intended. The last two chapters in the book discuss how to expand the horizons of UNIX. They consist of multiprocessor UNIX systems and distributed UNIX systems. The former is a tightly coupled set of processors running UNIX, while the latter is UNIX running across a network of machines. Bach warns us in the preface that this discussion does not imply a commitment by AT&T.

Running UNIX on a multiprocessor architecture poses a problem due to the means of handling critical sections described earlier. Sections of code in the kernel are currently executed without interruption. This is harder to enforce with more than one processor. Bach describes two solutions in some detail. The chapter on distributed UNIX presents the idea of a cluster of machines working on one problem and, less complex, a virtual disk. All these features have been worked on by computer manufacturers, and some are current offerings. However, it was interesting to hear the thoughts of a Bell Labs representative.

A Success

As Ritchie himself admits, UNIX offered no really new concepts when it was introduced. However, the inclusion (and maybe more important, the omission) of features and the way in which these features were integrated created a system with great appeal and synergy. A happy consequence of UNIX's portability is that most of this book is machine-independent. Probably one of the hardest subjects to describe in a linear text is an asynchronously driven operating system, but Bach succeeds.

Thomas M. Houser (2625 NE Seavy Place, Corvallis, OR 97330) is on the technical staff at Hewlett-Packard. He has 15 years' experience in technical applications and systems software.

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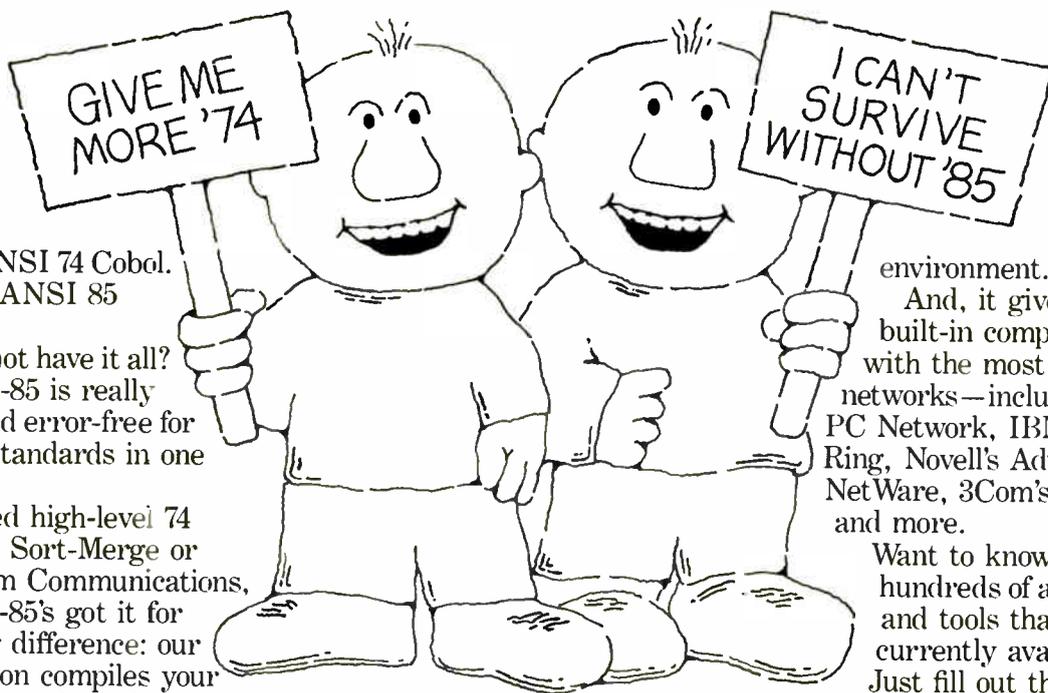


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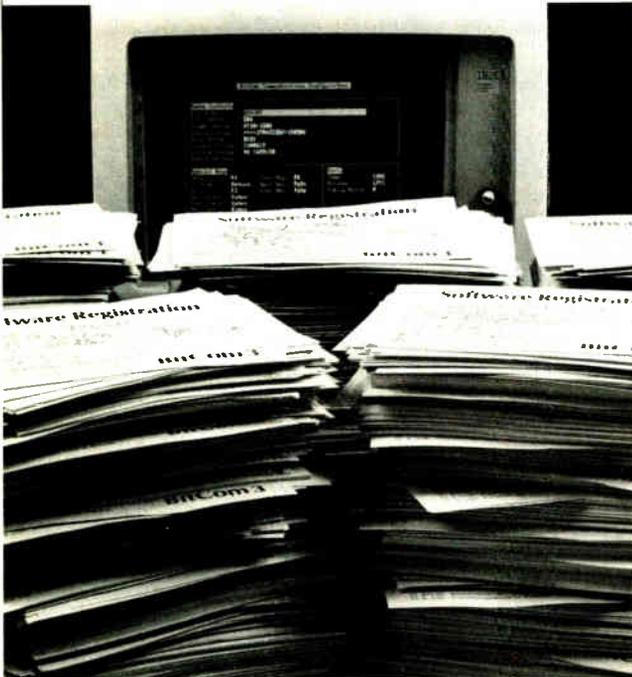
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THE ART OF PROLOG: ADVANCED PROGRAMMING TECHNIQUES

Reviewed by Steven H. Rogers

Only a few years ago logic programming and Prolog were esoteric topics largely confined to the academic world. Then came the announcement by representatives of the Japanese Fifth Generation Computer Systems project that the software for this ambitious undertaking would be based on Prolog. After an impressive string of successes in shipbuilding, automaking, consumer electronics, and semiconductors, a major Japanese initiative such as this attracted international attention; interest in Prolog soared.

Several introductory books about Prolog have appeared during the past five years or so. *Programming in Prolog* by W. F. Clocksin and C. S. Mellish (Springer-Verlag, 1982) is notable among these, providing the closest thing to a standard definition of core Prolog that we now have. BYTE has also responded with tutorials (see "Prolog Goes to Work" and "Logic Programming" in the August 1985 issue). The book in review here, *The Art of Prolog: Advanced Programming Techniques* by Leon Sterling and Ehud Shapiro, focuses on the needs of those who want to dig deeper into Prolog and logic programming.

The book, intended as a text for graduate students, is divided into four parts: Logic Programs, The Prolog Language, Advanced Prolog Programming Techniques, and Applications. An appendix gives a brief description of working with a typical Prolog implementation.

Logic Programs

Throughout the book, the authors emphasize the distinction between logic programming and Prolog. Logic programming consists of the definition of rules describing the relationships between objects. Computation, in this context, is the inference of the logical consequences of these rules. Prolog implementations diverge from this purely declarative framework to make efficient use of the underlying hardware.

The first four chapters devoted to logic programs provide a sound foundation for understanding Prolog. Rules, facts, and queries that form the basis for logic programming are illustrated with a biblical database. This database is extended to demonstrate the basics of data structures and recursive programming. The fifth chapter, which delves more deeply into the theory of logic programming, can be safely skipped by some readers.

The Prolog Language

While no true Prolog standard exists, the Edinburgh syntax described by Clocksin and Mellish is now generally accepted as the de facto standard. *The Art of Prolog* follows this syntax with the exception of the authors' preference for a \leftarrow instead of a $:-$ to connect the head of a clause to its body. I experimented with several of the examples and exercises using Prolog 86 from Solution Systems (Norwell, MA). I experienced no difficulties, so any Prolog interpreter or compiler that stays close to the Edinburgh syntax should serve as a study aid for this text.

The authors start with "pure" Prolog or Prolog programs that conform to a strict logic programming model. They then cover arithmetic, metalogical predicates, cuts and negation, and extralogical predicates. This solid review of Prolog basics is a good introduction to Prolog programming. This section concludes with a chapter covering such practical issues as style and efficiency.

Advanced Programming Techniques

This section is the heart of the book. It shows how Prolog can be used to write programs that are difficult to express in other pro-

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gramming languages. The authors provide a look at some more advanced techniques that have been developed over the years by members of the Prolog community. These techniques help programmers make the most of Prolog's unique features.

Chapter 14 covers nondeterministic programming, the most obvious feature of Prolog that is lacking in a procedural language like Pascal or C. Nondeterministic programs choose their next operation from multiple alternatives. While such behavior can be implemented in procedural languages, it is built in to Prolog. The generate-and-test method of problem solving is introduced, with the *N* queens problem as one example. No-frills versions of classic artificial intelligence programs such as Eliza are presented in Prolog, and extensions are suggested as exercises for the reader.

Two chapters cover incomplete data structures such as difference lists that are useful for such things as first-in/first-out queues. Separate chapters also cover definite clause grammars, making parsing easier for applications like writing interpreters and pattern recognizers. A chapter on second-order programming discusses the use of Prolog to find sets of solutions to problems. An interesting example of this is a program to efficiently route wiring on a circuit board or integrated circuit.

Sterling and Shapiro devote a chapter to the use of some classic AI search techniques in Prolog. They show how problems can be represented as state-space graphs and present Prolog programs that search state spaces using depth-first, hill climbing, and best-first search strategies. They also show how these techniques can be applied to planning and game-playing programs.

One aspect of Prolog programming is the equivalence of programs and data. This makes it easy to write programs that analyze, manipulate, or simulate other programs. Such programs are called metaprograms, and *The Art of Prolog* illustrates them by showing how to write and use metainterpreters (a metainterpreter is an interpreter for a language written in the language itself). Sterling and Shapiro demonstrate how Prolog metainterpreters can be applied to the building of expert system shells and program debugging aids.

Applications of Prolog

In addition to the many smaller examples illustrating the previous sections, the authors devote the last part of the book to examples of some larger-scale applications. I, for one, really appreciated the quantity and variety of examples.

One chapter demonstrates some nontrivial game-playing programs. Another describes a prototype credit evaluation expert system for commercial loans. Another shows how to write Prolog programs for performing symbolic mathematics. The vehicle used is a simplified version of PRESS (Prolog equation solving system), which solves symbolic equations. The final application is a compiler for a simplified version of Pascal called PL.

A Good and Readable Text

Although it's not what I would call light reading, *The Art of Prolog* is a rewarding book for serious students of artificial intelligence and programmers interested in exploring the advantages of logic programming. It is more readable than most graduate-level texts and detailed enough for a working programmer to use for self-study. Anyone considering a serious programming project in Prolog would benefit from this book, particularly the concluding portions on advanced techniques and applications. ■

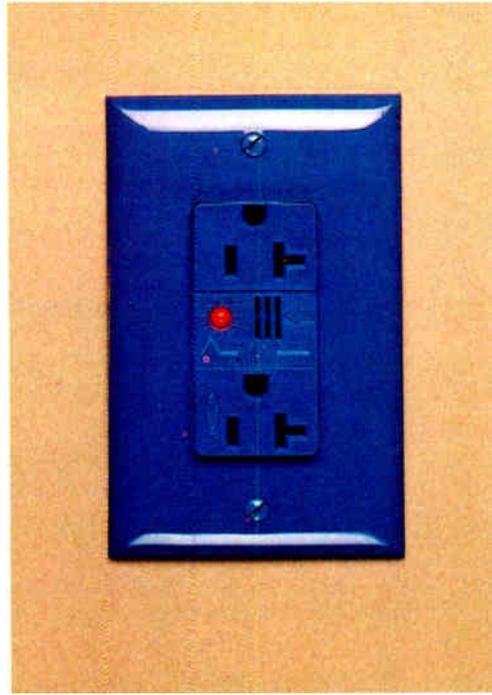
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Gregg Williams and Tom Thompson

The Apple Macintosh II

The Mac II's improvements include hardware slots, color, speed, and a compatible, open-ended system design

Editor's note: *The following is a BYTE product preview. It is not a review. We provide an advance look at this new product because we feel it is significant. A complete review will follow in a subsequent issue.*

Innovation and compatibility don't always go together easily. Some companies, when asked to improve their computer, go for a bigger-is-better approach, like the man who tried to breed his horses larger so they could pull a carriage faster—the strategy works, but only so far. Other companies, like Apple, take a think-then-act approach that looks beneath the surface of a problem to deliver a broader, more fundamental answer—in contrast to the horse breeder above, they retain the carriage but power it with an automobile engine.

Apple has combined innovation and compatibility in the Macintosh II, the Mac with color and peripheral-card slots, and it has been worth the wait. Apple has added the roman numeral "II" in homage to the Apple II, a product that has had a supernaturally long life span so far, and Apple's action in doing this is one that, for once, contains more substance than hyperbole. The original Mac's lack of slots stunted its growth and forced Apple to expand the machine by offering new

continued

Gregg Williams is a senior technical editor at BYTE; he wrote the original Macintosh product preview in the February 1984 issue. Tom Thompson is a BYTE technical editor whose past work includes contract programming for NASA. Both have been using Macintoshes for several years. They can be reached at One Phoenix Mill Lane, Peterborough, NH 03458.



The Apple Macintosh II.

models. With the Mac II, Apple—and, more important, third-party developers—can expand the machine radically without forcing you to buy a new computer. One thing is obvious: This is the design on which Apple plans to build its Macintosh empire.

About the only valid complaint that comes to mind—its lack of multitasking—will probably be remedied once Motorola's 68851 memory management chip becomes available. Even its under-\$5000 price is defensible. As is the case with many other new computers, you are buying it partially for its *potential*—but never before have we seen a computer in which that surcharge is so reasonable.

System Description

Here are the most important features of the Macintosh II (see also the system block diagram in figure 1 and the circuit boards in photo 1):

- **68020 and 68881 processing power:** The Mac II comes with a Motorola 68020 processor running at 15.6672 megahertz and a 68881 floating-point coprocessor. The inclusion of the latter chip as standard gives system software and any application access to hardware-assisted number crunching and the speed boost that comes with it. Existing applications that use SANE (standard Apple numerics environment) run 3 to 30 times faster auto-

matically, but applications that directly access the 68881 will be 30 to 200 times faster.

- **Six NuBus slots:** These six slots will let you extend the Mac II's hardware with coprocessors, LAN cards, and other add-ins. NuBus is a 96-pin card used until now in minicomputers and adapted for microcomputer use by Apple. Any card can become the "master," and the machine can be configured to start from any card. Because the 68020 motherboard acts like a NuBus card, it is possible for an add-in NuBus card to "take over" the system.

- **Growth within the same footprint:** The Mac II box, about the size of an IBM PC AT, has room inside it for the options most people want. The Mac II comes with 1 megabyte of memory (expandable to 8 megabytes on-board and up to 2 gigabytes using NuBus slots), one 800K-byte 3½-inch floppy disk drive, two Mini-8 serial (RS-232/RS-422) ports, a DB-25 SCSI hard disk interface, and two Apple Desktop Bus (ADB) connectors (for mouse and keyboard). The box also contains room for a second floppy disk drive; a 20-, 40-, or 80-megabyte internal hard disk; and six NuBus expansion cards. All this can be added without increasing the amount of space the Mac II takes on your desk.

- **Backward compatibility:** The Mac II supports most existing monochrome Mac programs (more than 95 percent of them) and the few programs that use QuickDraw's fixed-color capability. It does this because of the similarity of the 68000 processor (in the old Mac) and the 68020 (in the Mac II) and the heavy use in both machines' software of high-level libraries that let the same software run on vastly different machines.

- **Color support:** The Mac II supports color through Color QuickDraw and various other extensions to the Mac II Toolbox. Application programs manipulate 48-bit "absolute" colors, then translate them to the nearest approximations available through the attached video or printer cards.

- **No standard video output:** Though this sounds strange at first, it's really an advantage. All Mac II hardware and both old and new Mac software are designed to work with any Mac II video card, *present or future*. (Your video card will take up one NuBus slot.) Because you will be able to add any card and use it with all your software, hardware designers are

continued

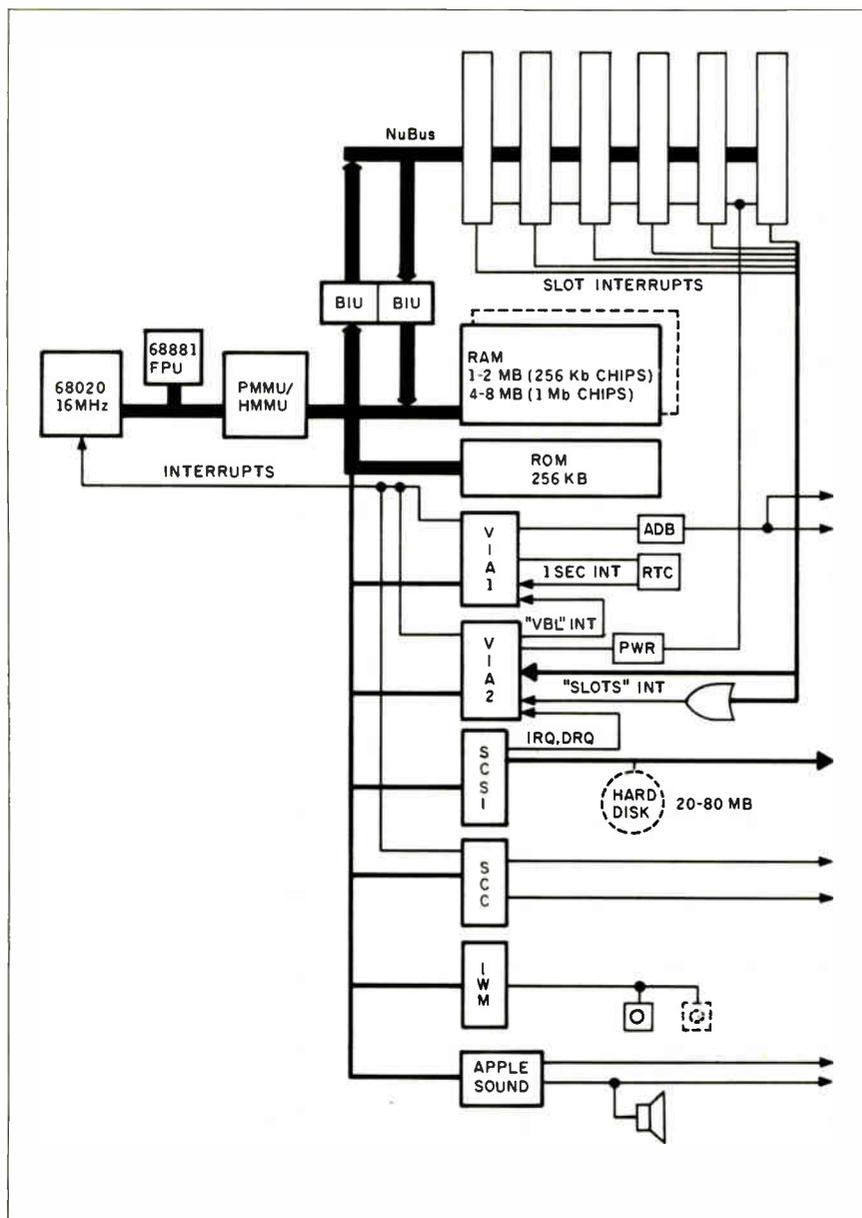


Figure 1: A block diagram of the Macintosh II. The dashed components are optional.

MACINTOSH II

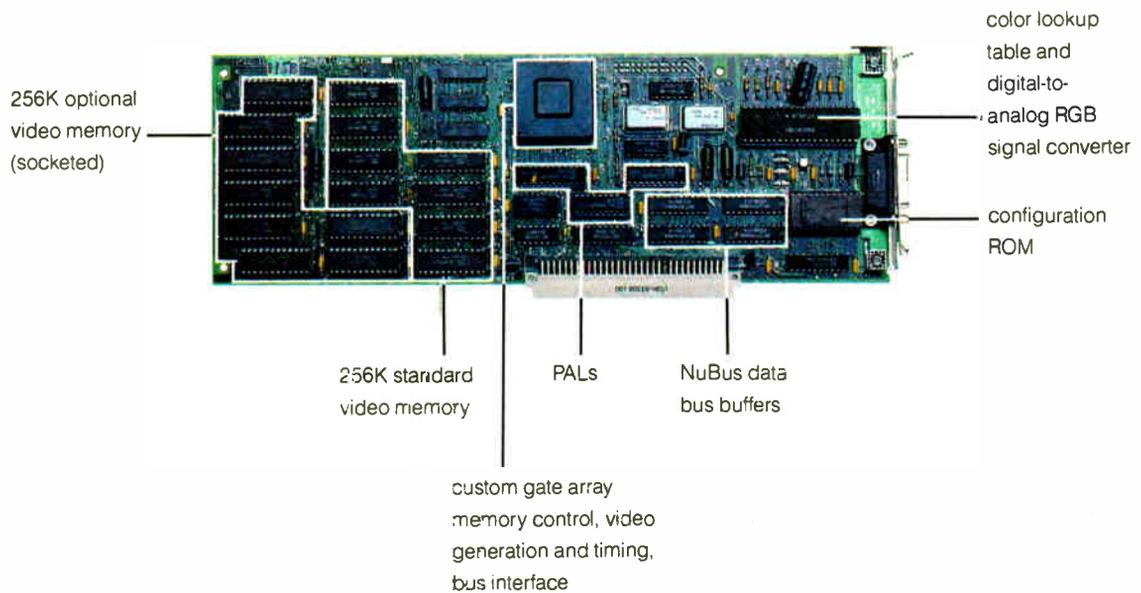
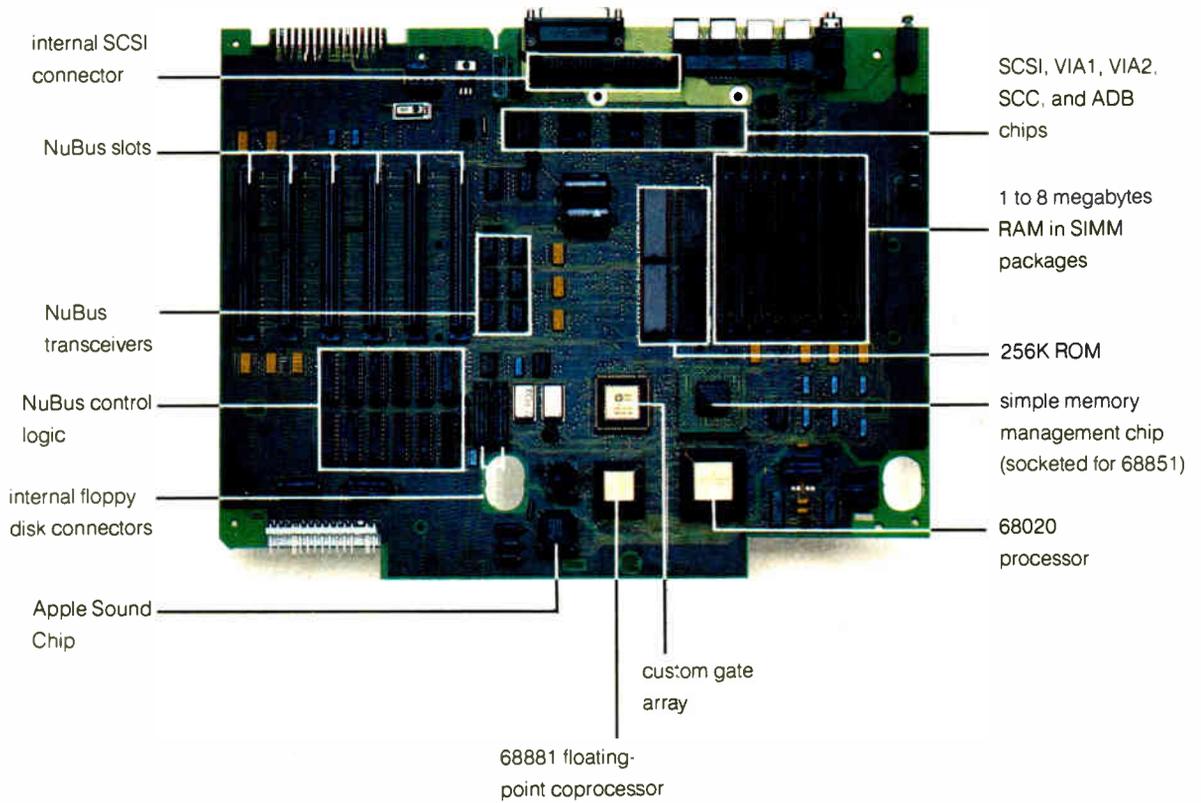


Photo 1: *The motherboard (top) and the NuBus Graphics Card (bottom).*

more likely to build custom video cards—which means you will eventually have numerous video output options from which to choose.

- **640-by-480-pixel video:** Apple has currently announced only one video board that will drive either a color or monochrome board at the 640 by 480 resolution. The standard board has 256K bytes of memory and displays up to 16 colors (or shades of gray) on the screen at one time, from a palette of more than 16 million colors. By adding an extra 256K bytes of memory to the board, you can increase this to 256 on-screen colors (or shades) at one time.

- **Multiple-screen desktop:** One consequence of the video design is that multiple video displays can be combined to create a “desktop” that spans two or more monitors. Even combined color and monochrome displays draw their contents correctly, and a window can span multiple displays.

- **MS-DOS and UNIX capability:** Apple says that a third-party company will offer an 80286 coprocessor card. Apple is also working on a version of UNIX, but that will have to wait for the availability of the Motorola 68851 memory management chip.

- **Sound support in hardware:** The Mac II contains a custom Apple Sound Chip (ASC) that replaces the old Macintosh sound-generating software with hardware and adds stereo capability, four-voice synthesized sound, and arbitrary sound sampled at up to 44.1 kilohertz. (Sound output is limited to 7.5 kHz, up from 5 kHz on old Macs.) Because these functions are now in hardware, sound can be used freely in applications without noticeable system degradation.

- **Other enhancements:** The Toolbox ROM, containing Color QuickDraw and other libraries of system software, is now 256K bytes long. An improved TextEdit allows the retention of text attributes like color, style, font, vertical spacing, and size during cut-and-paste operations. Use of the ADB frees the processor from much of the routine servicing of the keyboard and mouse and makes the Mac II more accessible to future input peripherals. SCSI data transfers are now faster because of hardware handshaking. Apple also offers detachable 81- and 105-key keyboards.

NuBus

NuBus is a 32-bit high-performance bus that emphasizes independence of any particular system architecture and a simple

yet sophisticated transaction protocol. A card's address space is determined by the slot it occupies on the bus, and a “strictly fair” arbitration protocol allows every card a chance at bus access. Multiprocessing is possible by allowing multiple bus-master cards and restricting access to shared resources through bus locking. We'll take a closer look at each of these characteristics in turn to see how the NuBus design accomplishes this.

NuBus is a multiplexed bus (i.e., address information and data share the same lines at different intervals) operating synchronously at 10 MHz. The bus reads and writes data to a 32-bit address space of 4 gigabytes. Bus addressing is accomplished by driving all 32 bits of the address onto the multiplexed lines. Data transfers can be 8-, 16-, or 32-bit quantities, a facility that complements the dynamic bus-sizing capabilities of the 68020 processor. NuBus explicitly defines data sizes of a byte (8 bits), halfword (16 bits), and word (32 bits) and their addressing relationship. (When a halfword is broken into 2 bytes, the most significant byte is in the lower memory address. Words are broken into halfwords similarly.) These sizes will be referred to as NuBus byte, NuBus halfword, and NuBus word when it is necessary to distinguish between a NuBus quantity and a 68020 quantity. NuBus also defines block transfers of 2, 4, 8, or 16 NuBus words. However, we won't cover this capability since it's not used by the Mac II.

Two important points must be made about the NuBus address space. First, all addressable resources occupy a single address space whether it's a memory chip or a control register. There isn't an “I/O space” or “CPU space” or other entity requiring additional control signals and logic. Second, since the addressing relationship of data sizes has been defined from the bus's point of view, you know precisely where byte x lies on NuBus. This provides a common ground where processors that address bytes differently can share information. If a processor's bus-interface circuitry is wired so that reading or writing a byte corresponds to reading or writing a NuBus byte, dissimilar processors can share data through NuBus byte transfers.

Each slot on the bus is hard-wired with a unique 4-bit ID number that identifies it to a peripheral card inserted into the slot and limits NuBus to a maximum of 16 slots. This ID serves to set the address range that the card will respond to and also figures in the arbitration scheme, which will be described later.

The upper sixteenth of the 4-gigabyte address space (256 megabytes) is termed *slot space*. This slot space is partitioned

into 16 regions of 16 megabytes each. Slot addresses are of the form FSxxxxxx, where S (bits 27 through 24) is assigned by the slot ID. This assignment of a fixed address space based on a card's position on the bus is called *geographic addressing*. No jumpers or DIP switches are required to configure a card into the system since a card's address range is determined by the ID of the slot it occupies. The remaining portion of the NuBus address space is unreserved and can be allocated to devices as needed.

The NuBus specification makes two requirements of a card on the bus. First, the card must respond with the appropriate control signals to reads of the NuBus word located at the top of its allocated slot space (address FSFFFFFC). This is required to indicate that the bus slot is occupied. Accesses to an unoccupied slot will be handled by a bus time-out mechanism. Second, a card must have a configuration ROM located at the top of its slot space. The purpose of this ROM is not defined by the NuBus specification. The presence of a configuration ROM does happen to satisfy the first NuBus card requirement: indicating slot occupancy.

NuBus also specifies the physical dimensions, or form-factor, of a card. Two types of cards are defined: a triple-height form-factor and a PC-style form-factor. The PC form-factor is defined for micro-computer use and describes a 4- by 13-inch card that uses a 96-pin Eurocard type C connector.

NuBus Lines

NuBus is composed of 96 lines: 51 signal lines and 45 power and ground lines. All signals are active low except for the address/data lines that use tristate drivers. The signal lines can be divided into three types: Utility, Bus Data Transaction, and Arbitration System Signals. All signal names ending in an asterisk are active low.

The power lines supply voltages of +5 V, -5.2 V, +12 V, and -12 V for every card on the bus. The Utility lines carry signals that are supplied to the backplane by the computer system. Some of these signals are the Clock (CLK*), Power Fail Warning (PFW*), Card Slot Identification (ID3*-ID0*), and Reset (RESET*). The Bus Data Transaction lines handle addressing and data (AD31*-AD0*), parity signals (SPV* and SP*), and two lines that manage the start and end of a data transfer (START* and ACK*). The Arbitration System Signals handle the arbitration of several cards contending for ownership of the bus. The Arbitration Signals (ARB3*-ARB0*) are used to determine the next bus master, and Bus Re-

continued

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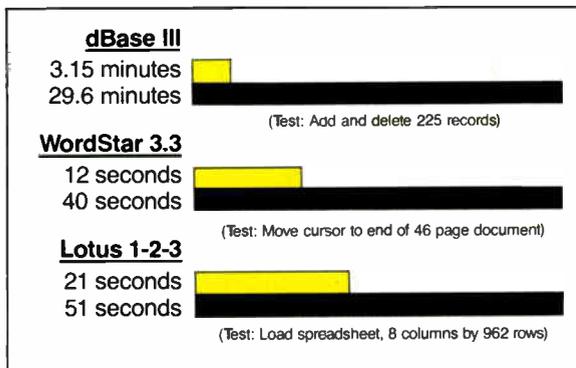
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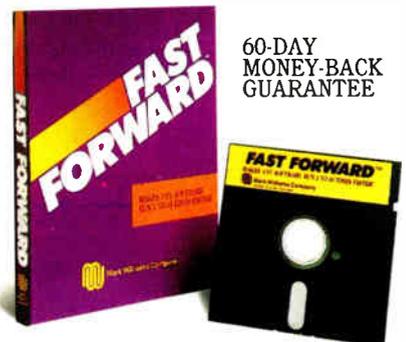
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quest (RQST*) is used to indicate that a card wants bus ownership.

To use NuBus, a card normally obtains ownership of the bus. It accomplishes this by requesting the bus and waits until this request is granted. A card that owns the bus can initiate a data transfer and is called a *master*. A card becomes a *slave* when it is addressed by a master and responds to the data transfer. A read or

write between a master and a slave card begins with a START* cycle, followed by multiple bus cycles to address and transfer the data, and ends with an ACK* cycle. Such a data transfer is called a *transaction*. *Tenure* is the period of time a card continuously owns the bus. The NuBus specification does not require a card to become a master. A special line, the Non-Master Request (NMRQ*), allows

this type of card to signal a need for service.

Two of the Bus Data Transaction lines, termed Transfer Mode, serve double duty during a NuBus transaction. At the start of a transaction, these two lines (TM1* and TM0*) carry a transaction code that indicates the type of transfer (read or write and data size) taking place. At the end of a transaction, they carry a response status code that indicates whether the data transfer was successful. See tables 1 and 2 for more information on the transaction codes and their response codes. See figures 2 and 3 for a detailed look at complete NuBus read and write transactions.

NuBus also defines an Event Transaction, which is a special form of a write transaction. Its purpose is to post interrupts to a slave card. The Mac II does not use Event Transactions, so they will not be discussed further.

NuBus Arbitration

When many cards are on the bus, it's possible that two or more of them may request bus ownership on the same clock cycle. NuBus provides distributed arbitration logic (so called because the components implementing the arbitration mechanism are present on every card) to handle this situation. The arbitration protocol is called "fair" because cards attempting to own the bus at the same moment will eventually obtain access to the bus and obtain access before any of the competing cards get access a second time. Because there isn't a special priority scheme embedded in the NuBus arbitration logic, it is said to be "strictly fair." The NuBus design avoids a preemptive or priority arbitration protocol that can produce conditions where higher-priority cards continue to own the bus and "starve" a lower-priority card's access to the bus.

A card requests use of the bus by asserting the Bus Request line (RQST*). It will not assert RQST*, however, if this line was asserted on the last clock cycle. If the card is able to assert RQST*, it will continue to do so until it gains ownership of the bus and begins a transaction by asserting START*. Once it has asserted RQST*, a card drives its slot ID onto the arbitration lines ARB3*-ARB0*. The card will unassert these lines if it finds higher IDs present. This results in the arbitration lines holding the ID of the highest-numbered card competing for the bus. The ID present on these lines indicates the next bus master. As you can see, when several cards request the bus on the same clock cycle, the arbitration contest will be won by the card with the highest slot ID.

Table 1: NuBus Transfer Mode signals.

TM1*	TM0*	AD1*	AD0*	Type of Cycle
0	0	0	0	Write byte 3
0	0	0	1	Write byte 2
0	0	1	0	Write byte 1
0	0	1	1	Write byte 0
0	1	0	0	Write halfword 1
0	1	0	1	Block write
0	1	1	0	Write halfword 0
0	1	1	1	Write word
1	0	0	0	Read byte 3
1	0	0	1	Read byte 2
1	0	1	0	Read byte 1
1	0	1	1	Read byte 0
1	1	0	0	Read halfword 1
1	1	0	1	Block read
1	1	1	0	Read halfword 0
1	1	1	1	Read word

Table 2: NuBus Transaction Response signals.

TM1*	TM0*	Type of Acknowledge	Comment
0	0	Bus Transfer Complete	The transaction was successful.
0	1	Error	During a read, the data may be corrupted. During a write, the transaction may not have completed successfully.
1	0	Bus Timeout Error	Slave failed to respond in 256 cycles. The bus time-out logic has generated an ACK* to terminate the transaction.
1	1	Try Again Later	Slave cannot complete transaction at this time. The slave may be able to complete the transaction at a future request.

Table 3: NuBus Attention Cycle signals.

TM1*	TM0*	Type of Attention Cycle	Comment
0	0	Attention-Null	Used to reinitiate arbitration or end a locked-resource transaction.
0	1	reserved	
1	0	Attention-Resource-Lock	Start of a locked-resource transaction.
1	1	reserved	

The winning card has access to the bus immediately if the bus is not busy, or at the completion of a transaction if the bus is busy. Once this card owns the bus, the remaining cards again contend for the bus and undergo the arbitration contest to select the next bus master. This process repeats until all the cards that requested the bus have been granted bus access. Fairness is implemented by the requirement that a card can request the bus only if RQST* is not already asserted. Other cards will be blocked from competing for the bus until all the cards that requested the bus simultaneously on a previous clock cycle have owned the bus.

A bus master may continue to own the bus as long as RQST* is unasserted (that is, no other card is requesting use of the bus). The master is said to be *parked* on the bus and can continue to use the bus without undergoing an arbitration contest. Bus parking reduces the time normally required to gain access to the bus in a computer system with few active cards. However, once RQST* is asserted, the bus master won't start another transaction, and a new arbitration contest begins.

Multiprocessing on NuBus

The NuBus specification also lets a master lock the bus. This is necessary for certain operations that must be allowed to complete in a multiprocessor environment (e.g., a test-and-set operation on a semaphore).

The NuBus specification defines two types of locking: bus and resource. Bus locking is used by a master to ensure an unbroken bus tenure. A master can also lock the bus to gain performance for a large data transfer involving many bus transactions, although this is not recommended. Resource locking is used to inform a slave card to lock out all local access routes on the card to a resource being addressed by NuBus. For example, a multiprocessor card might have dual-ported RAM that the processor could access during a NuBus transaction on the same RAM. Resource locking informs the card to lock out the local CPU port while a locked NuBus transaction is in progress. More than one card can be locked during a resource lock. Note that resource locking accompanies bus locking; that is, a continuous bus tenure occurs during a resource lock.

Bus locking occurs when the master continues to assert RQST*. The master, having won the arbitration contest previously, is still the highest ID card in the competition and thus continues to own the bus.

Resource locking requires the master
continued

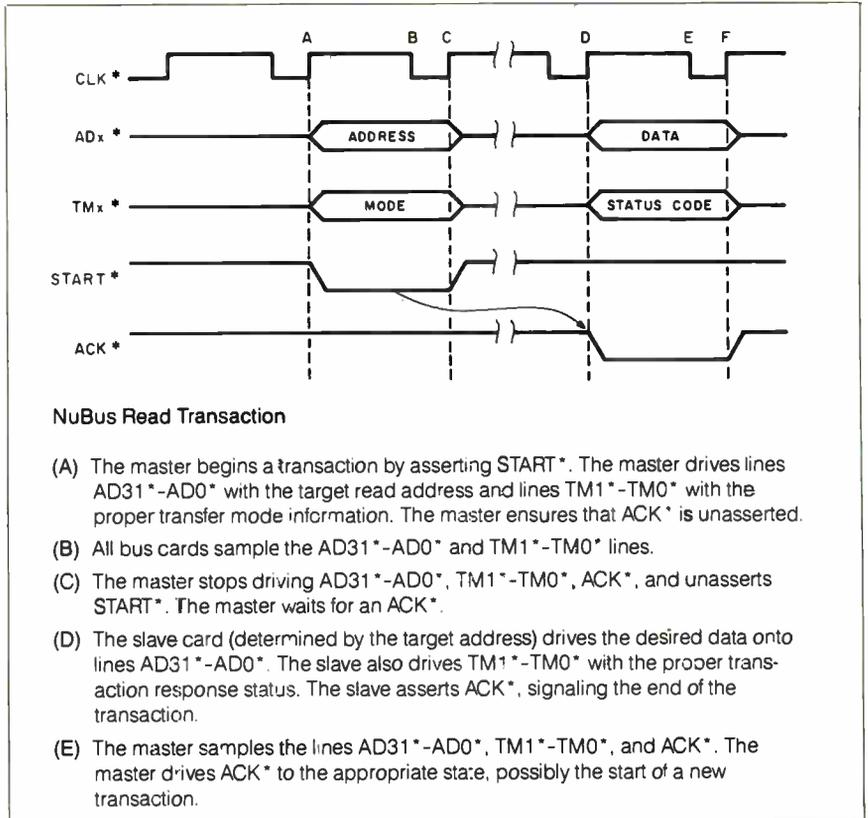


Figure 2: Timing diagram for a NuBus read transaction.

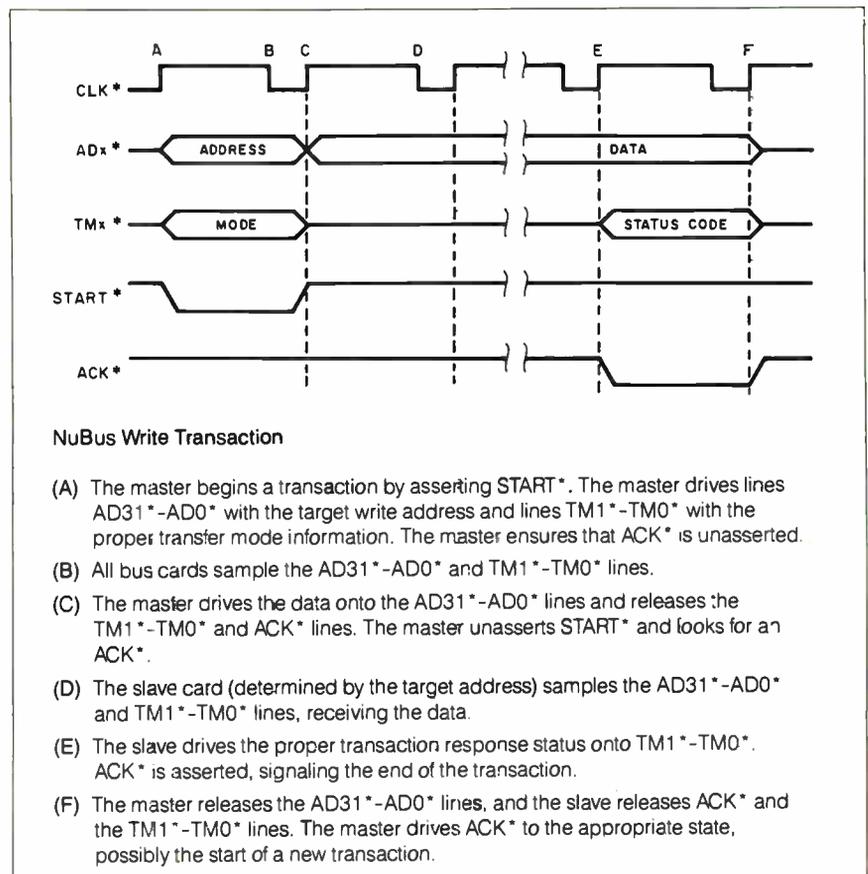


Figure 3: Timing diagram for a NuBus write transaction.

to issue certain signals to inform cards on the bus that a locked transaction is occurring. The master begins the lock by issuing an Attention-Bus-Lock cycle. An Attention cycle is generated by asserting both START* and ACK* at the beginning of a bus transaction. The master also drives an Attention-Resource-Lock code onto the Transfer Mode lines (see table 3). At the end of the locked transaction, the master issues an Attention-Null cycle (START* and ACK* asserted with the corresponding code on the Transfer Mode lines) to signal the end of the bus lock. All cards with lockable resources sample the bus for an Attention-Bus-Lock cycle and note it. If a card happens to be addressed by the master during this interval and before an Attention-Null cycle is issued, it will lock its resources. NuBus does not require a card to lock its local resources, but its use in a multiprocessor environment won't be reliable if it doesn't.

Apple NuBus

The Macintosh II comes equipped with six NuBus slots. These slots are hardwired with IDs from 9 to 14 (9 to E hexadecimal), and each follows the PC form-factor as described in the NuBus specification. The motherboard is treated as slot 0, and ID 15 (which has no corresponding physical slot) is reserved. One of the slots will be occupied with a video card.

Apple has worked with the IEEE NuBus proposal group and has followed the specification closely. Not all of the NuBus features are supported, however. Apple calls this subset of the NuBus specification Apple NuBus, which dif-

fers from the specification in one area: Apple NuBus does not supply -5.2-V power to the NuBus backplane.

Some parts of the NuBus specification are "open"; that is, certain parts are undefined or optional and can be implemented as the designer sees fit. One of these is the use of the NMRQ* line: It can be bused, or each slot can have its own dedicated interrupt line. Apple has chosen the latter method, feeding each line to the VIA2 (versatile interface adapter) chip. Although bus parity is described in the NuBus specification, its use is not required. Bus parity is not generated by Apple NuBus, and the NuBus lines SP* and SPV* are not used.

The processor on a card is not required to communicate to the bus by NuBus byte addressing, but it is convenient if several processors are sharing the bus. The Macintosh II is designed to support NuBus byte addressing. The bus transceivers are wired to place 68020 data bytes onto the bus in NuBus byte order. This wiring does not affect addressing. Finally, NuBus doesn't specify the contents of the NuBus configuration ROM. Apple describes specific information for the configuration ROM that enables the Macintosh II to install a driver for the card, run machine or card initialization code, and load bootstrap code if the card can be booted. All these code blocks in the configuration ROM are loaded into main memory on the Mac II's motherboard before being executed.

Apple NuBus has some limitations brought about by the Macintosh system architecture. For some time-critical operations (for example, a data transfer to the IWM), the 68020 must prevent NuBus

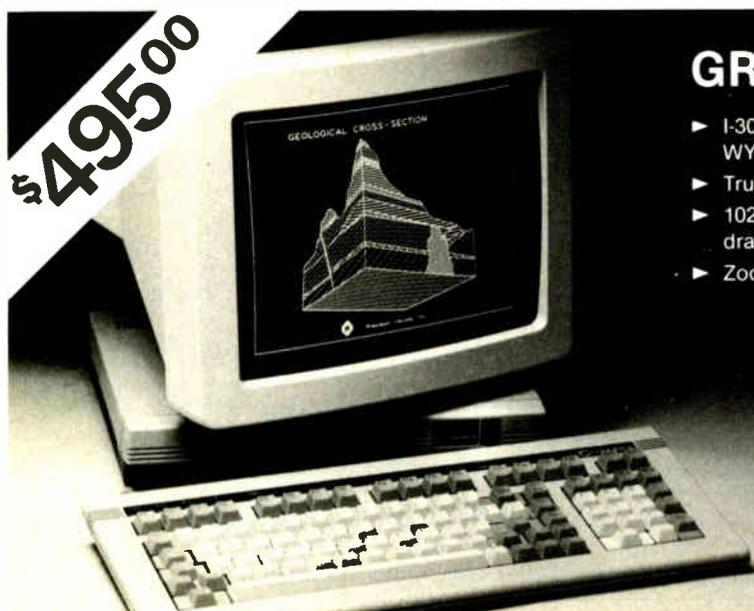
from interfering with its local bus. It does this by performing a *local bus lock*. This is accomplished by asserting a line (BUS-LOCK*) to the VIA2. This informs the NuBus interface to lock the motherboard RAM from NuBus access. The NuBus interface will respond with a Try-Again-Later transaction response code to any access attempt.

Current Macintosh software uses an address space of 4 megabytes, compared to the Macintosh II's 4 gigabytes. This came about because the 68000 processor is limited to 24-bit addresses and the location of the Mac ROMs in this address space. This poses a problem for the Macintosh II, since it must support the existing base of Mac software. The Macintosh II uses a mode bit on the VIA1 to indicate if it is running in a 32-bit mode or a 24-bit "compatibility" mode. In the 24-bit mode, logical addresses of the form Sxxxx hexadecimal are mapped to physical addresses of the form FS0xxxx hexadecimal. The 24-bit mode restricts the Mac II to six NuBus slots, and each slot is limited to 1 megabyte.

A vendor wishing to support either addressing mode should design a card's NuBus address decode to ignore AD23*-AD20* and use AD19*-AD0*. The card must be able to produce a 32-bit address to access resources on the motherboard.

From Bits to Pixels

The old Macintoshes use a bit map to represent the screen; one bit represents one pixel, and only two colors are possible: black and white. The Mac II generalizes this to 1, 2, 4, 8, 16, or 32 bits per pixel. Apple's first video board will use either



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4- or 8-bit pixels, thereby allowing 16 or 256 different colors, respectively. On the high end, a 32-bit pixel gives a theoretical limit of 4,294,867,296 different colors on-screen at one time—from a 48-bit-wide palette representing more than 280 trillion colors. (These numbers far exceed other system constraints.)

The design of Color QuickDraw allows the support of three different layouts of video memory. In *planar* layout, the video display comprises one or more *bit planes*, where the number of colors or shades of gray possible equals 2^n , where n is the number of bit planes. Here, adjacent bits in a bit plane contribute to the definition of different pixels, but the n bits that define a given pixel are scattered throughout memory. Color QuickDraw supports the monochrome one-plane graphics and the eight-fixed-color graphics supported by previous Macintoshes.

The second layout is the one Apple supports completely: *chunky* pixels. In this layout, all the bits for one pixel are adjacent and are followed by all the bits for the next pixel. Each pixel is defined by 1, 2, 4, 8, 16, or 32 adjacent bits in memory. This layout works well with Apple's preferred design of graphics output devices, which use *color lookup tables*. These cards use the numeric value stored in the pixel's memory to index into a known table of colors from a much larger color spectrum. In the case of Apple's first video card, the actual (Apple calls it *concrete*) color is 24 bits wide, giving 16,777,216 colors from which to choose.

The last layout is a hybrid of the first two, *chunky-planar*. It has separate memory areas for the red, green, and blue components of its pixels, with the components being chunky, that is, 1, 2, 4, or 8 adjacent bits describing a given component. This layout might be used someday to drive a very high-resolution color device that would use three slots for its three bit planes. The current implementation of Color QuickDraw does not support this, but the overall design permits it.

Color on the Mac II

One of the most impressive additions to the Macintosh II is its use of color. But how did the Apple designers do this, while still allowing the machine to run most existing Macintosh applications? The answer lies in the parts of the Mac II's Toolbox ROM code called Color QuickDraw; its supporting package, the Color Manager; and several other sections of the Toolbox. Here are the most important aspects of Color QuickDraw:

Backward compatible: According to Apple, "All changes are designed to be fully backward-compatible with the older

Macintosh ROM." The designers of the new code do this in several ways. First, some QuickDraw routines have the same name but have been extended to take care of color and other enhancements (e.g., CopyBits). Some routines and data structures are new but are color equivalents of their monochrome counterparts (e.g., NewCWindow, bkPixPat). Some data structures replace the data in a given field with a handle to a larger pixel-oriented data structure. Of these, some flag the color orientation of the data structure by setting the top 1 or 2 bits of a given field to 1s. Overall, the designers said that about 80 percent of the Color QuickDraw code—mostly high-level routines—is the same as it was in the older QuickDraw; the rest is low-level routines that have been enhanced or changed to deal with colored pixel structures.

Generalized: Many data structures have been made more versatile. For example, the mouse cursor is still 16 by 16 pixels, but it can now be in color. Similarly, the patterns that QuickDraw uses to "paint" areas are no longer limited to being an 8 by 8 monochrome image. Color QuickDraw supports colored rectangular patterns with each side being a power of 2.

Adaptive: Color QuickDraw adapts to the display hardware that it is currently using. For example, Color QuickDraw drawing routines look at the current configuration of the graphics output device (video screen, printer, etc.) and adapt accordingly. Also, both the color cursor and color icons have two images: a color image for normal use and a monochrome one for use when the screen is either monochrome or 4-colored (i.e., 1- or 2-bit pixels). Color QuickDraw uses the appropriate image automatically.

Room to grow: The designers have created data structures with future expansion in mind. Several data structures have a field or fields reserved for future Apple use and a single field available for the application's use. In addition, Apple's first video display card can grow from 4 to 8 bits per pixel (increasing the possible number of colors from 16 to 256). Color QuickDraw is designed to use pixels up to 32 bits wide from a color palette with 48-bit-wide entries.

Color QuickDraw does not do all this work by itself. The Color Manager routines and data structures manage the use and mapping of color through a data structure called a *gDevice* (graphics output device) that describes the display (or printer) device being used.

Absolute and Concrete Colors

One of the most unusual features of the Mac II is that it was not designed with a

standard video output. Although only one video card is available now, Apple expects that several video cards of differing color capabilities and resolutions will be available eventually. With such diversity possible, how can a software developer know what to put on the Mac II's video display?

Just as Apple hardware engineers designed the Mac II to one of several video output cards, the system software engineers envisioned a way of representing video images that any video output card can use. They decided that all applications should work with colors in an *absolute* form, represented internally as three 16-bit values, one each for the red, green, and blue components of the color. As we will see below, the Color QuickDraw software and the Mac II video hardware will work together to translate an absolute color to the closest concrete color the video card can supply.

The Color Lookup Table

As we mentioned before, the Mac II is most comfortable with printer interface and video output cards that use a color lookup table. In this way, even the standard video card, which can display only 16 colors, can offer that many colors from a much larger palette. When you start up the Mac II, system software initializes each graphics output device with its closest approximation to the values for a standard color table. When an application requests an absolute color, certain routines (described below) use the current device's color table to supply the best approximation that device can supply.

The Color Manager provides several routines that allow running programs to interact with the current graphics output device. Among them are

Color2Index and Index2Color: These translate between the absolute color and the index number of the closest concrete color the device can supply.

InvertColor: This routine translates an absolute color to the closest concrete representation of its inverse.

GetSubTable: This routine is given a table of absolute colors and calculates their nearest concrete equivalents in the color table of the current device.

Since both desk accessories and multiple application programs (through Apple's Switcher program now and, perhaps someday, multitasking programs on a future Apple machine) must share the same color table, the Color Manager includes routines to change and protect the current device's color table:

continued

Color QuickDraw adds six modes that are equivalent to the modes of TI's TMS34010 chips.

SetEntries: This routine lets the application change an entry in the current device's color lookup table.

ProtectEntry: This "locks" a table entry so other applications (running under Switcher) or desk accessories cannot change it (or it can also unlock an entry).

ReserveEntry: This reserves or unreserves a given entry for exclusive use by the current application; other programs will not be able to "see" or use it.

Color Drawing Modes

Color QuickDraw supports the source/destination drawing modes of old QuickDraw (copy, OR, XOR, BIC [black-is-changed], and their negative counterparts), but all but the copy modes don't make sense when they are used with colored pixels. Color QuickDraw adds six modes that are equivalent to the modes of the Texas Instruments TMS34010 chip. The modes are replace-with-transparency (allows one image to overlay another), additive (which is like combining colored lights), subtractive (like mixing paints), maximum and minimum (for overlapping aliased objects), and blend (combines source and destination pixels in a fixed ratio).

Inside gDevice

So far, we've talked only about the interaction between Mac II software and the current graphics output device hardware. (This device is usually a video display but can also be a printer or an off-screen pixel map.) The data structure that bridges the software and the hardware is called the *gDevice*, or graphics device; this data structure is created when the system software opens the device driver for a given device.

In general, the *gDevice* record gives the system software access to certain necessary information about the current device. Here are some of the most important fields:

gdType is an integer that tells the software the type of the current device, for example, fixed-color, color lookup table, or direct RGB.

gdSearchProc points to a linked list of one or more routines that translate an absolute color to a concrete color. This routine can be called by higher-level routines

like *Color2Index*, and different applications can install their own search routines for use by them alone.

gdCompProc is similar to *gdSearchProc* except that it points to a linked list of routines that map an absolute color to its concrete complement. This routine is called by *InvertColor*.

gdPMap is a handle to the device's pixel map.

Other Color-related Changes

The Apple software engineers have added several new window-related data structures and Toolbox routines that include color support. The *GrafPort* structure of the old Macintosh has *CGrafPort* as its counterpart. Similarly, the color equivalent of the old *WindowRecord* is *CWindowRecord*. Also, *NewCWindow* and *GetNewCWindow* create a new window. The Mac II's *Window Manager* routines have been expanded to work correctly with both *WindowRecords* and *CWindowRecords*.

The *CWindowRecord* is identical in size and most of its fields to the old *WindowRecord* (at least in the first implementation of the Mac II Toolbox ROM). Color-related information is stored in that window's *auxiliary window record*. This record points to a color window table, which determines the colors used for the window background, border, text, close and zoom box highlighting, and title bar background.

When the Apple engineers decided to preserve the congruence between the monochrome and color window records, this meant there was no space for the *CWindowRecord* to point to its auxiliary window record. Instead, the global variable *AuxWindowList* points to a linked list of auxiliary window records, each of which points to the color window record that owns it. Also, a window can do without one if it uses the system software's default window colors.

Controls (buttons, check boxes, etc.) have *auxiliary control records* that are analogous to auxiliary window records. The routines *SetDeskColor* and *SetDeskPixPat* allow software to add color and patterns to the desktop itself.

The following menu components can also contain their own independent colors: the menu title and the menu item background, text, check mark, and command key. The Mac II has systemwide default menu colors if the *System* file contains a *menu color information table* (an 'mctb' resource). An application can override these values if it contains its own 'mctb' resource.

(The engineers also described two other changes to menus that are not related to color. First, menu bars now have

their own *definition procedure*, which controls how they are drawn. Although the Apple-supplied procedure will restrict menu bars to the top of the main screen, it will be possible to write a different definition procedure that can allow, for example, a menu title and its body to be "torn off" and moved around the desktop or attached to a window's drag bar. Second, Mac II menu items can have secondary menus that pop up to the right side of the item [as in the Commodore Amiga]. These let you make several related choices with one mouse movement.)

Macintosh II Video Card

The Macintosh II does not come with a built-in monitor. Video is "broken out" into a graphics card that plugs into a NuBus slot. This eliminates some processing constraints coupled to the video display that are a fact of life with the old Macintosh.

Apple will offer a Macintosh II Video Card that can provide up to 256 colors or shades of gray on a 640-by-480-pixel display. This card has a user-selectable color depth of 1, 2, 4, or 8 bits. It features a color lookup table that can be adjusted to display any 256 colors selected from a palette of 16.8 million. The video card will come equipped with 256K bytes of RAM, providing video memory that supports a display of up to 4 bits per pixel, or 16 colors. As an option, the video memory can be expanded to 512K bytes, allowing a display of 8 bits per pixel, for the maximum of 256 colors.

The heart of the Macintosh II Video Card is a custom chip called the TFB, named after its designer. This chip handles video timing and generation and on-card memory control. The TFB uses two clocks on the card for generating video signals. The first is a 30.24-MHz clock used with color monitors. The second is a 12.27-MHz clock used to generate RS170 video (RS170 video is an RGB signal with NTSC timing that is used with projection TVs or film recorders). A software-controlled interlace bit is used to select which clock signal the TFB uses to generate the display.

The video card features an adjustable color lookup table (CLUT). This is a chip with a memory array and three 8-bit D/A converters that generate the red, green, and blue analog signals. A color pixel that is to be displayed is first presented to the CLUT. This byte (we're assuming 8-bit color depth) is used as an offset into the memory array that is composed of 256 values that are 24 bits wide. This 24-bit value drives the three 8-bit D/A converters. A copy of the CLUT values is

continued

The Tale of the Emperor's Database

How long will it take to sort it out?

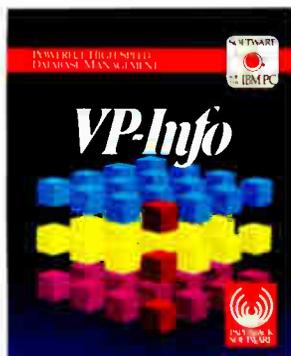
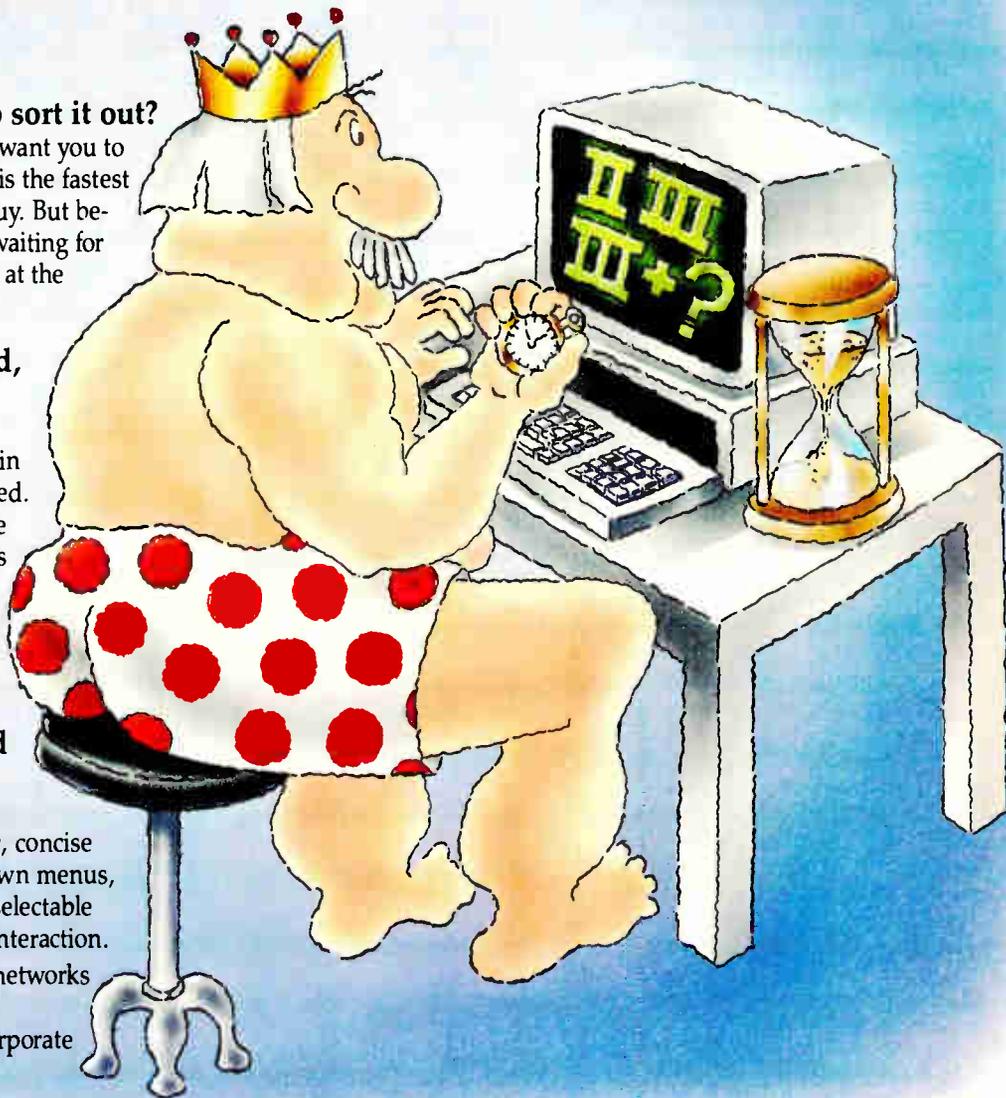
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***VP-Info* features a versatile and extended command language.**

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maintained in Macintosh II memory. If you happen to alter a color, this table in RAM is updated. The RAM table is then loaded into the CLUT, preserving your new selection. The CLUT mechanism offers ample flexibility in color selection without complex color-generation hardware. Applications or desk accessories that used the VBL interrupt will still function—a “fake” VBL interrupt is provided by the Mac II.

Enhancements to TextEdit

One of the shortcomings of the original Macintosh is that the standard text-editing package, TextEdit, cannot handle tabs or any change in font, size, or styling. (Obviously, it can't handle color information, either.) In addition, TextEdit has its own scrap, distinct from the Scrap Editor's desk scrap (used to implement the Macintosh's cut-and-paste Clipboard).

The TextEdit code in the Macintosh II uses the same edit record as the old Macintosh ROM to store a unit of text but interprets some of the fields differently to deliver new features. The most important of these are

txSize: If $txSize \geq 0$, the edit record is of the old type and nothing changes. If $txSize < 0$, this is a new edit record, and the following fields are interpreted as described below.

txFont and *txFace*: If this is a new edit record, combine these two fields to make a handle; its value will point to this edit record's style record (discussed below).

lineHeight: If $lineHeight \geq 0$, use it and the *fontAscent* field as normal. If $lineHeight < 0$, use the style record's pointer to the line-height table (LH-Table), which contains information on the spacing between any given line and the one that follows it.

Using Styled Text

The old edit record has room for the text of the record and nothing more. The style table and style run data structures contain the additional information that the old edit record lacks.

Apple defines a substring of text with the same font/size/styling/color/vertical spacing attributes as a *run*. The *style table* contains one record for each distinct font/size/styling/color combination; the *stCount* field within a record contains the number of runs in the edit record text that use this combination.

The edit record points through the *style record* to a table called the *style run table*. The first record points to the first character of text and to the style table entry that describes its font/size/styling/color/vertical spacing attributes. The second

record points to the first character of the second run and its attributes, and so on sequentially through the runs of the edit record's text.

The enhanced TextEdit routines cut and paste directly to the desk scrap (instead of the internal scrap the old TextEdit routines used). In addition, the Mac II designers have defined a new scrap type, *styl*, to go with the *TEXT* scrap type used by old Macintosh applications. The *styl* scrap type, *StScrpRec*, contains a table that is almost identical to the style table in that it describes the spacing, font, size, style, and color of a certain run of text. However, it is like the style run table in that it describes the text linearly, with one record for each of the runs as they appear. The *stCount* field has a new meaning: It gives the starting character position for the run.

Though the enhanced TextEdit is still not versatile enough to meet the needs of all applications (word processors, for example), it will be useful in many others. Also, applications' use of the *styl* record will make the cutting and pasting of styled text more commonplace among programs.

The result of all this is a set of routines and data structures that is backward-compatible with existing Macintosh software but has the ability to save a string of text with its spacing, font, size, style, and color attributes and pass it (via the standard Macintosh Clipboard) to another program that can use it. For compatibility with existing Macintosh applications, Apple recommends that a software developer save text directly to the desk scrap (both *TEXT* and *styl* records) and the old TextEdit private scrap that older programs expect to see.

Sound

The Macintosh II has decoupled sound generation from the hardware that limited the sound capabilities on the Macintosh. Some of the sound generation has been implemented in a custom chip, reducing the CPU overhead required to make complex stereophonic sounds. Also, the sound drivers have been expanded and are now incorporated into a Sound Manager.

The old Macintosh tied sound generation to the video display's Vertical Blanking interrupt and a buffer of 370 bytes interleaved with the buffer for disk speed control. The restriction imposed by this time interval (the blanking interrupt) limits digital sound reproduction on a Mac to a maximum frequency of 11 kHz. This is an ideal condition at best: Actually, the Mac has a practical frequency range of 5 kHz, due to the sound hardware and filtering. The Mac's hardware

limits digital sound sampling rates to 22 kHz.

The Mac II has independent sound-generation circuitry. It can sample at 44.1 kHz, the same as a compact disk player's sample rate. However, a CD uses 16 bits of information to encode sounds, while the Mac II uses 8 bits. Finally, the Mac II's sound-reproduction circuitry, although improved, yields a practical frequency range of only 7.5 kHz.

The sound hardware consists of an Apple Sound Chip (ASC) and two Sony power-amplifier chips. The ASC has two pulse-width-modulated outputs, each routed to its own Sony chip to produce stereophonic sound. Only one of the Sony chips drives the Mac II's internal speaker, producing monophonic sound. The Sony chips drive an external stereo jack with the appropriate voltage levels for Walkman-style headphones and booster amplifiers, which simplifies interfacing the Mac II to stereo sound equipment (the Mac overdrives this type of equipment). The Mac II senses whether something is plugged into the external stereo jack and generates stereophonic or monophonic sound as appropriate.

A four-voice Wave Table Synthesizer is built into the ASC. Repetitive waveforms can be loaded and played continuously without CPU intervention. The ASC reduces CPU overhead in waveform synthesis from 50 percent to less than 10 percent. Sound generation now requires so little processor overhead that complex sound generation can be performed concurrently. For example, you could have a favorite waltz sound file read off a hard disk and play while you worked with a spreadsheet or word processor. You can't play a sound file from a floppy disk concurrently because the IWM disk-controller chip requires too much processor intervention.

As stated earlier, the sound software has been improved. All old Sound Driver and Synthesizer calls are supported. The programmer also has four new synthesizers available for use.

The first is the Note Synthesizer. This software plays a simple melody of notes, one at a time. The software is equivalent to the Mac Square Wave Synthesizer if the Note Synthesizer is programmed to play square waves.

The second is the Wave Table Synthesizer. It plays sounds using wave table lookup synthesis. A *wave table* is one complete oscillation of a waveform stored in a table of 512 or 256 8-bit samples encoded in an offset binary format. A wave table can be loaded or modified at any time during play. The Synthesizer can

continued

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play a single tone or several. A one-shot mode plays a wave table upon command, rather than continuously. This software corresponds to the old Four Voice Synthesizer if four waveforms are played.

The third is the Musical Instrument Digital Interface Synthesizer. It provides a convenient software interface to play an

external synthesizer attached to the Mac II using the MIDI music standard. You'll need a vendor's MIDI interface unit to complete the connection between the Mac II's serial port and the music equipment. The MIDI Synthesizer conforms to the current MIDI specification. The Sound Manager has 16 channels that cor-

respond to MIDI channels.

Finally, there is the Sampled Sound Synthesizer, which plays prerecorded or sampled sounds. As with the Wave Table Synthesizer, the sounds are encoded in offset binary. The sounds can be played at the original or different sampling rates. Different sampling rates change the pitch

The Mac SE is one of the two new members of the Macintosh line. It will be priced from \$2600 to \$3600, depending on the system configuration, and should be available by the time you read this.

At first glance, the outside of the Mac SE resembles a Mac Plus: It has a built-in 9-inch monochrome monitor with a 512- by 342-pixel display, a single 3½-inch 800K-byte floppy disk drive, two serial ports, a connector for an external drive, and an SCSI port as standard. The housing looks almost the same, but then you note small differences. The cooling vents on the top of the Mac Plus are moved to the front of the machine. The compartment for the clock/calendar battery is missing—so is the mouse port. A new access panel for reaching a single peripheral card has appeared. The plug-in jack for the keyboard is gone because the Mac SE keyboard uses the Apple Desktop Bus, whose connector (one of two) is located on the back of the machine. Finally, when you turn the Mac SE on, you hear the purr of a cooling fan.

Internally, the Mac SE basically resembles the Mac Plus. The Mac SE uses the same 68000 microprocessor running at 7.83 MHz. It has the same SIMM (single in-line memory modules) holding a megabyte of RAM, expandable to 4 megabytes. It uses the same sound-generation circuitry as the Mac Plus. However, the similarities to the Mac Plus end here. The Mac SE has 256K-byte system ROMs. The power supply has been beefed up: It has a maximum output of 100 watts, and we've already mentioned the cooling fan. Many of the discrete components that populated the Mac Plus motherboard have been combined into a large gate-array chip on the SE's motherboard. The clock/calendar chip is powered by a seven-year lithium battery, also mounted on the motherboard, and a 50-pin SCSI connector is mounted next to the NCR 5380 SCSI controller chip.

There's enough room in the upper housing and adequate power to mount an internal SCSI 20-megabyte hard disk or

an extra 3½-inch floppy disk drive. Both hardware options are available from Apple for the Mac SE. Last but not least, a single 96-pin slot using a Euro-card type C connector is mounted on the side of the Mac SE's motherboard (see photo A). This connector makes unbuffered processor signals and power available to vendor cards that can be plugged into the slot. The card must lie parallel to the motherboard in the cramped space at the bottom of the Mac SE.

The most interesting thing about the Mac SE, of course, is its expandability. Apple has announced that it will supply a 5¼-inch 360K-byte floppy disk controller card, with software to translate Macintosh text files to an MS-DOS file format and back. An Apple spokesperson indicated that a third-party company will announce a 8086-based expansion card that will give the Mac SE IBM PC compatibility. The card will emulate both the IBM monochrome and CGA cards in software and will give approximately the same performance as an IBM PC. It will contain an Intel 8086 proces-

sor but has no provision for the use of an 8087 numeric coprocessor. The board will do no multiprocessing: At all times, either the 8086 or the 68000 will be in control of the machine. The board will use Mac SE memory for its computation. Other possible uses for the slot are a coprocessor card (68020 or 68881, for example), a local area network card, and an interface board to an external expansion box.

The amount of code and data in ROM has doubled, from 128K bytes for the Macintosh Plus to 256K bytes for the Mac SE. About 160K bytes of this is actual code and resources, comprising the code from the Mac Plus ROM, considerable enhancements to that code, and all the code libraries that were formerly stored in RAM except the International Utilities Package (which handles time, date, currency, and other country-specific items). The rest of the space is taken up by the Macintosh system fonts (Chicago 12, Monaco and Geneva 9 and 12 for roman-language-based systems, and kanji for Japanese systems). The

The Mac SE



of the sounds and can be used for special effects. This synthesizer corresponds to the old Free-Form Synthesizer.

SCSI

The Macintosh II uses the same NCR 5380 SCSI controller chip as does the Mac Plus. However, a number of changes

to the Mac II hardware have improved performance and reliability of the SCSI interface.

The first of these changes is that the Mac II SCSI interface now supports an SCSI interrupt. This interrupt signal (IRQ) is connected to the VIA2 chip. The 5380 DMA (direct memory access) Re-

quest signal, which indicates that the data register is ready to be read or written, is also brought out to the VIA2 as an interrupt. This setup prevents the SCSI bus RESET* signal from causing a permanent interrupt to the 68020, since RESET* is not maskable through the 5380.

continued

Mac SE and Mac II ROMs share some of the same code. Some of the routines that use identical code are Appletalk drivers, TextEdit routines, SCSI Manager, ADB drivers, and the Script Manager.

The video circuits in the earlier Macintoshes spend 50 percent of the RAM access time available during display of a horizontal line, leaving the other 50 percent of that time for doing everything else (they spend all of the time for normal computation during the vertical and horizontal retrace intervals, when the video screen is not drawing anything). As mentioned earlier, the Mac SE integrates 19 discrete chips into one custom gate array and a PAL. Because this gate array can transfer twice as much data (collects two words instead of one word) at a time into the video circuitry, the Mac SE now spends only one quarter of the RAM access time servicing the

video display. This provides a theoretical performance boost of approximately 25 percent for applications running in RAM. (The actual increase varies from 10 percent to 20 percent.)

The SCSI hardware in the Mac SE now does its signal handshaking in hardware; this allows it to run faster than it would under software that polls the SCSI port periodically and more accurately than it would under software that does "blind" (i.e., no handshaking) reads and writes. Like the Mac II, the SCSI hardware also provides an SCSI interrupt to the Mac SE. This, combined with the rewritten SCSI Manager, should provide a performance boost for SCSI hard disk operations.

The Mac SE, like the Apple IIGS, uses the new Apple Desktop Bus to connect the keyboard, mouse, and other human-input devices to the computer. (See "The Apple IIGS" by Gregg Wil-

liams and Richard Grehan in the October 1986 BYTE for more details.) This scheme decreases the amount of time the 68000 must take to service these devices and makes the design of new input devices much easier (and these devices can be used on both Macintoshes and Apple IIGSs).

Finally, the Mac SE has increased the amount of parameter RAM (used to maintain user preferences, time, and other data even when the machine is turned off) from 20 bytes to 256 bytes. Apple has not decided what to use this extra memory for, but we're sure it will eventually be put to good use.

There will be no upgrade path from the Mac Plus to the Mac SE. There are so many changes to the Mac SE's housing, motherboard, and analog board that it would be more economical to purchase a new computer rather than attempt an upgrade.

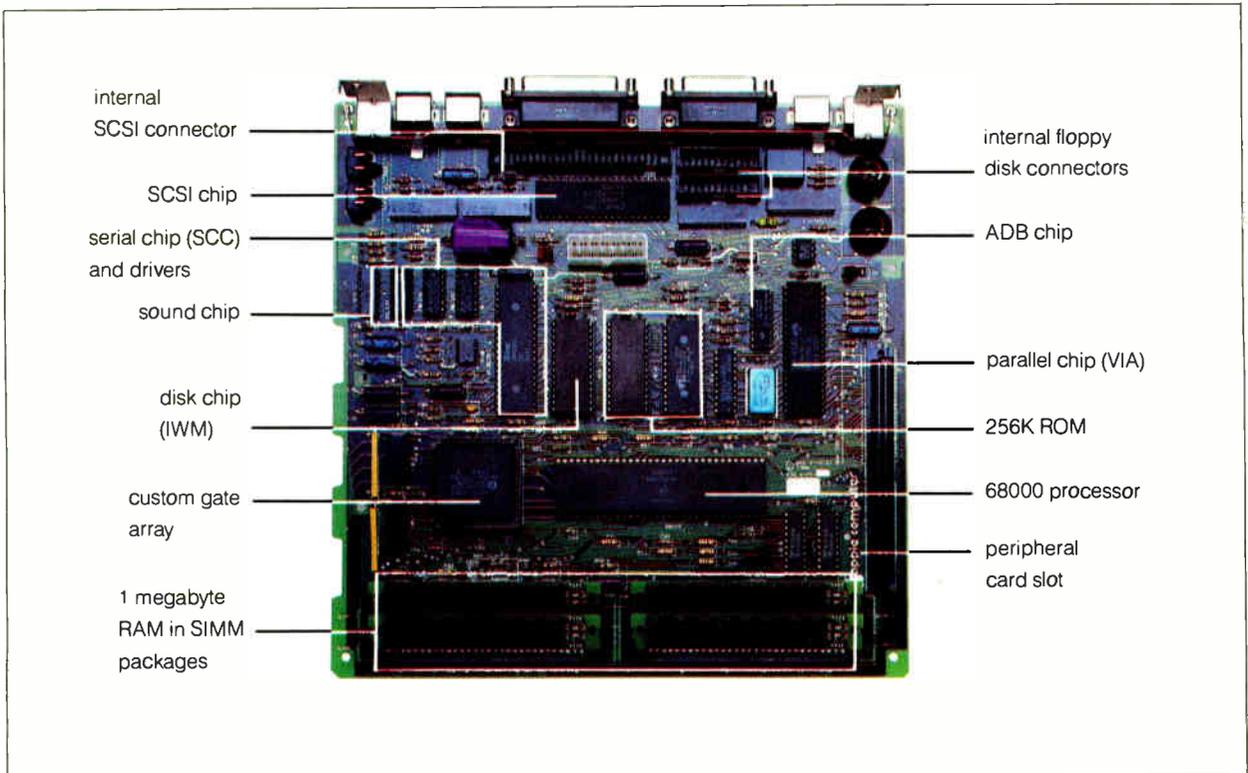


Photo A: *The Mac SE motherboard.*

This means that a slow device on the SCSI bus can now interrupt the processor when it has completed an operation. For example, suppose you have a hard disk and a tape backup unit attached to the Mac II SCSI bus. You order the tape unit to find the logical end of the tape and copy a file to it. The tape unit disconnects from the SCSI bus while executing the seek to end of tape. You can continue to manipulate files on the hard disk, since the SCSI bus is free for use while the tape unit is disconnected. When the tape unit reaches the tape end, it attempts to reconnect to the SCSI bus and generates an interrupt. Software then starts the process of copying the file from the disk drive to the tape unit. The important thing to note is that the interrupt mechanism prevents slow devices from tying up the Mac II processor or SCSI bus.

The second change is that the SCSI interface supports hardware handshaking during an SCSI bus transfer. The Mac Plus SCSI interface has two modes of data transfer: pseudo-DMA and blind reads or writes. The pseudo-DMA mode allows the 5380 to perform the SCSI bus handshake, but the 68000 polls the chip to check on the status of the transfer. The processor fetches or writes a byte when the 5380 indicates that the transfer operation is complete. Each byte moved through the SCSI interface has to be checked in this manner. It's obvious that SCSI transfers consume some CPU overhead and lower the effective transfer rate.

The alternative for Mac Plus SCSI transfers is to utilize blind reads or writes. These operations simply pass data bytes through the SCSI bus with no handshaking, nearly tripling the data-transfer rate. If the SCSI device is fast enough to handle this data flow, this isn't a problem. If the device isn't fast enough, however, the processor can write invalid data by overrunning the chip during a write operation, or it can read invalid data during a read operation by accessing the chip before it has received a valid byte. The Mac II's hardware handshake eliminates polling by allowing the 68020 to access the 5380 only when valid data is available. This is accomplished by suppressing the DSACK0* line, which holds the processor off the chip. The Mac II's handshake DMA eliminates the CPU overhead required to perform reliable high-speed SCSI transfers. It must be noted that these hardware handshakes must occur within 16 microseconds or a bus error will be issued in an attempt to end a presumed deadlock. Therefore, handshake DMA should be used only with high-speed devices.

A 50-pin SCSI connector is located internally in the Mac II. On the outside, a

DB-25 SCSI connector—identical to the Mac Plus's—lets you connect other SCSI peripherals. The SCSI Manager now has the capability to partition hard disks and boot from a particular partition.

Slot Manager

The NuBus specification spares you from knowing intimate hardware details to configure a new card into the Mac II: The address space is set when the card is plugged into a slot. In a similar manner, something should spare you from knowing intimate software details to install a device driver for a new card or set an interrupt vector for the driver. This is the Slot Manager's job.

At start-up, the Slot Manager detects the presence of a configuration ROM on a NuBus card. If the card is defined as a boot device, the Slot Manager will read the boot code in the configuration ROM into memory and transfer control to it. If the card is not bootable, information is read in the ROM that describes the device driver or drivers for the card. The start-up code next attempts to read a driver with the same resource name in the System File and install it in the Mac II's main memory. If a resource with this name can't be found in the System File, the named driver is read from the configuration ROM and installed into memory.

This method of driver installation provides two benefits. First, the device driver embedded in the card's ROM is installed automatically into the system without user intervention. Second, should the device driver code need fixing, the vendor can provide the new code on a disk that can be inserted into the System File using a simple install program. Since the System File is searched first for the card's device driver, this replaces the old driver in the configuration ROM.

Interrupts using NMRQ* are posted to the VIA2 chip. The Slot Manager determines which slot requested service by reading a register in the VIA2 and dispatches the appropriate interrupt routine. Interrupt routines are also in the configuration ROM as part of the device driver.

Script Manager

One of the most significant concepts of the original Macintosh was its division of a file into *resources*, where each resource is a certain type of data used by the file. In the case of program files, the code resource (which contains the executable code of the program) is separate from, say, the information relating to dialog boxes in the DITL resource. This makes it possible, for example, for a developer to change the text contained in dialog boxes without having to change the code of the program itself. Thus, a developer

can easily change a program to French, Spanish, or another Romance language (i.e., one that uses the Roman alphabet).

But what about other languages, like Arabic, which reads right to left and alters the shape of its letters based on its surrounding letters? What about Japanese, which has far more than the 256 characters allowed in a normal Macintosh font? To meet these needs, Apple has added another library of code, the Script Manager, to isolate language differences from the rest of an application program, thereby making it far more portable among different human languages.

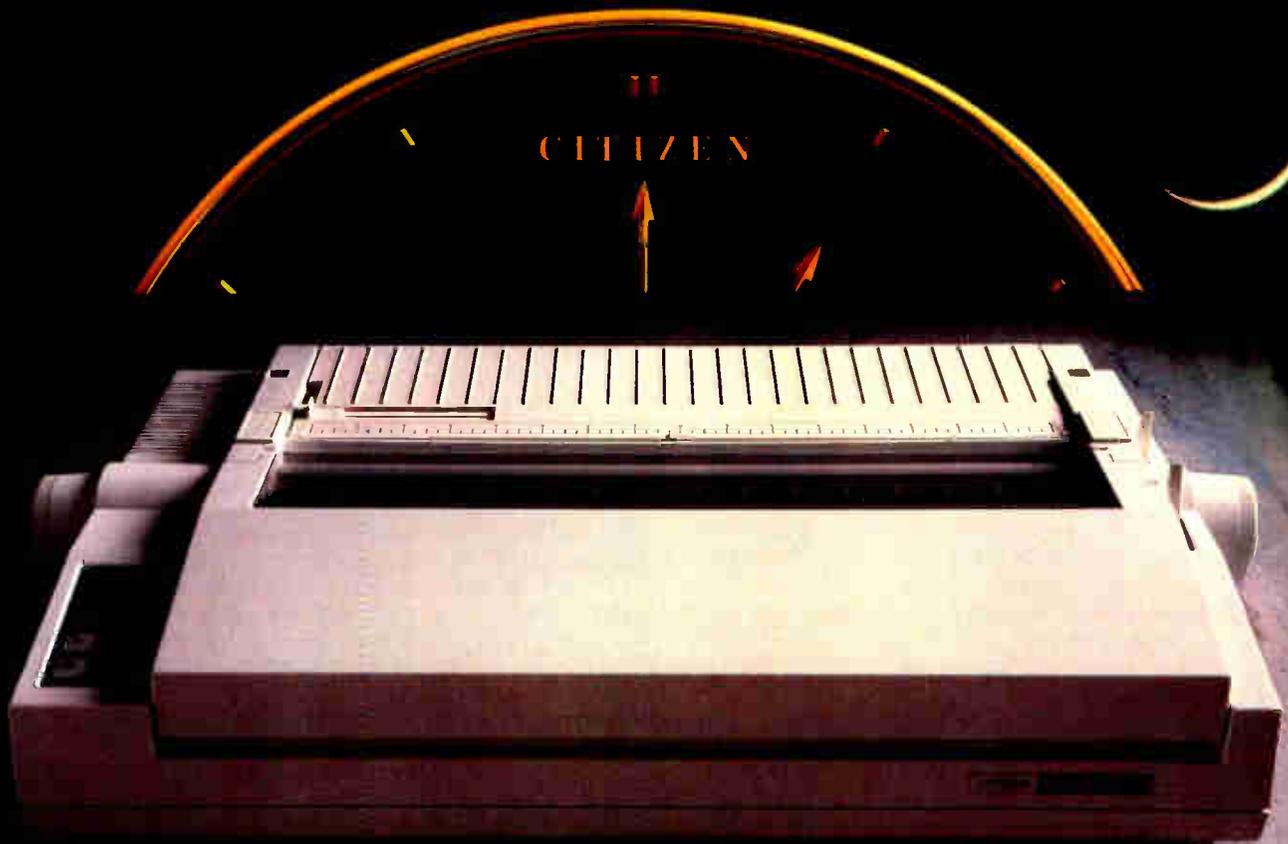
(In addition to the features of the Script Manager, the TextEdit editing package and the International Utilities Package have been extended to work correctly with the Script Manager. Also, the system software described here will work with any Macintosh with enough memory to hold the needed programs and data. Because of this, references will be made to routines and data structures from the old Toolbox ROM, not the newer Mac II Toolbox ROM.)

According to Apple, a *script* is a "writing system" that includes a character set; a writing direction (left to right or vice versa); keyboard mapping(s) and text input method(s) (e.g., multiple keystrokes per character); text drawing, measuring, and editing methods; sorting methods; and time, date, and number formats. To use a given script, the Script Manager must have an associated *script interface file* for that script. Apple now has RIS (roman interface system), KIS (kanji interface system, also called KanjiTalk) for Japanese, and AIS (Arabic interface system) for the major Arabic languages. (AIS has been available since October 1986.)

Not all applications will need to use the Script Manager. (But those applications that do use it have access to routines they would normally have to provide themselves.) The enhanced TextEdit can handle text selection, highlighting, word selection, dragging, and word-wrapping of a given script automatically; only applications that do extensive text manipulation or that don't follow the *Inside Macintosh* guidelines will need to use Script Manager routines. But for those applications that do need to use them, the following paragraphs describe some of the major routines, what they do, and why they are needed.

The Macintosh finds which script to use by looking at the font associated with the current GrafPort. The routine FontScript returns the value of the current script. Applications can cause the keyboard to change in accordance with the

continued



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user's font by using the KeyScript routine.

Each font has a direction associated with the drawing of its words; for example, the Arabic font places its characters on the screen right to left. The low-memory global variable `teSysJust` determines the direction of text justification (e.g., right-justified for Arabic) and the direction of successive words in whatever font. For example, a mixed sequence of Arabic and English words is placed right to left if `teSysJust` is on and left to right if it is off. In both cases, though, individual English words are written left to right and Arabic words are written right to left.

In languages with more than 256 characters (Japanese, for example), individual characters are represented by 16-bit words, but some roman characters are still represented by 8-bit bytes. This presents problems when searching a text string for a character that is represented in one byte—it may mistakenly match the second byte of a 16-bit character. To prevent this, the application should call the routine `CharByte`, which determines whether a given byte in a string is a 1-byte character or the first or second byte of a 16-bit character.

Similarly, the complexities of certain languages (including Japanese and Arabic) make it difficult to associate a certain pixel location on-screen (where the mouse button was clicked, for example) with the character it corresponds to in the associated text string. To help solve this, the routines `Pixel2Char` and `Char2Pixel` associate a given character in the text

string with the number of pixels the drawn character is from the beginning edge of its representation on-screen.

Some languages do not use spaces to separate words. Because of this, the Script Manager uses a *break table* to define where text can be correctly broken. The break table is actually a collection of rules or templates, called *continuation sequences*, that define what character sequences shouldn't be broken. The routine `FindWord` uses the break table to determine where word breaks occur.

Finally, languages differ in the way they add "blank" space to make a certain text string justified. The routine `DrawJust` draws text fully justified, using a method particular to the given script to fill the line of text out so that it fills the entire space between both margins.

Multiple-Screen Desktop

One of the most amazing things the Mac II can do is to treat the images from two separate monitors as if they were both part of one large desktop area. As you can see from photo 2, the devices don't even have to be of the same type. The paragraphs that follow give a brief explanation of how this is accomplished.

Each graphic output device (gDevice) connected to the Mac II defines a rectangular area, the `gdRect`, it is responsible for. When the gDevices are connected properly, the Mac II system software considers the desktop (the region called `GrayRgn`) to be the union of all the devices' `gdRects`. By referencing `GrayRgn`, system software can move objects among

all the display areas of the different output devices without any limitations; also, "well-behaved" Macintosh applications can use the larger desktop without having to do anything special to use it.

All the gDevices are connected together in a linked list of handles; a program gets the first device by calling the `GetDeviceList` routine, or it can get the primary device (the one that contains the menu bar) by calling `GetMainDevice`. The `ColorQuickDraw` routines have been extended to draw to multiple gDevices. When a `ColorQuickDraw` routine receives a drawing command, it checks to see if the drawing is intended for the screen (as opposed to an off-screen bit map). If it is, the routine compares the rectangle in which the drawing is to take place with the `gdRects` of all the screen devices and issues a drawing command to each device where there is some intersection between the two.

A window can even span multiple screens because the Mac II Window Manager has been modified to the dragging boundaries enforced by the older Macintosh ROM (thus enabling the mouse pointer and the objects it is dragging to move among screens). Also, since the various screens may be of different resolutions and color depths, the cursor-drawing routines must keep track of which screen contains the cursor.

MS-DOS Compatibility

Apple sees several ways in which to give its users the levels of MS-DOS (and IBM PC) compatibility. Depending on the user's needs, it may be enough to provide file transfer capability through a network of Macs and IBM PCs or through a file conversion utility called `Passport` that Apple plans to announce later this year. (Apple offers a 5¼-inch disk drive that, when connected to a Macintosh, allows the appropriate software to read and write IBM PC-compatible files.)

Apple told us that an unnamed third-party company will provide an 80286 multiprocessor NuBus card and software for the Mac II that will give approximately the performance of a 6-MHz IBM PC AT. This combination will let you work on MS-DOS applications in a Macintosh window, with full access to the desktop and desk accessories and some cut-and-paste capability between applications on the different machines. They will also be able to use a Macintosh hard disk in such a way that both IBM and Macintosh programs will be able to read and write each others' files directly.

The 80286 card will be capable of true multiprocessing with the Mac's 68000. It also will have a socket for the addition of

continued

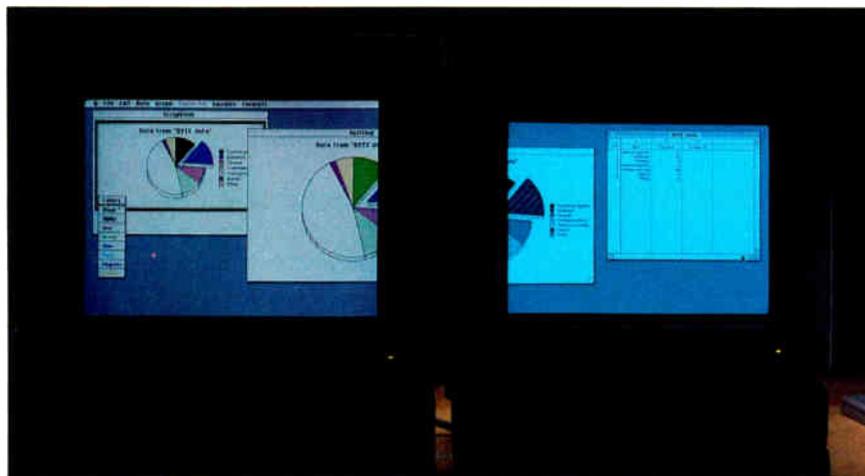
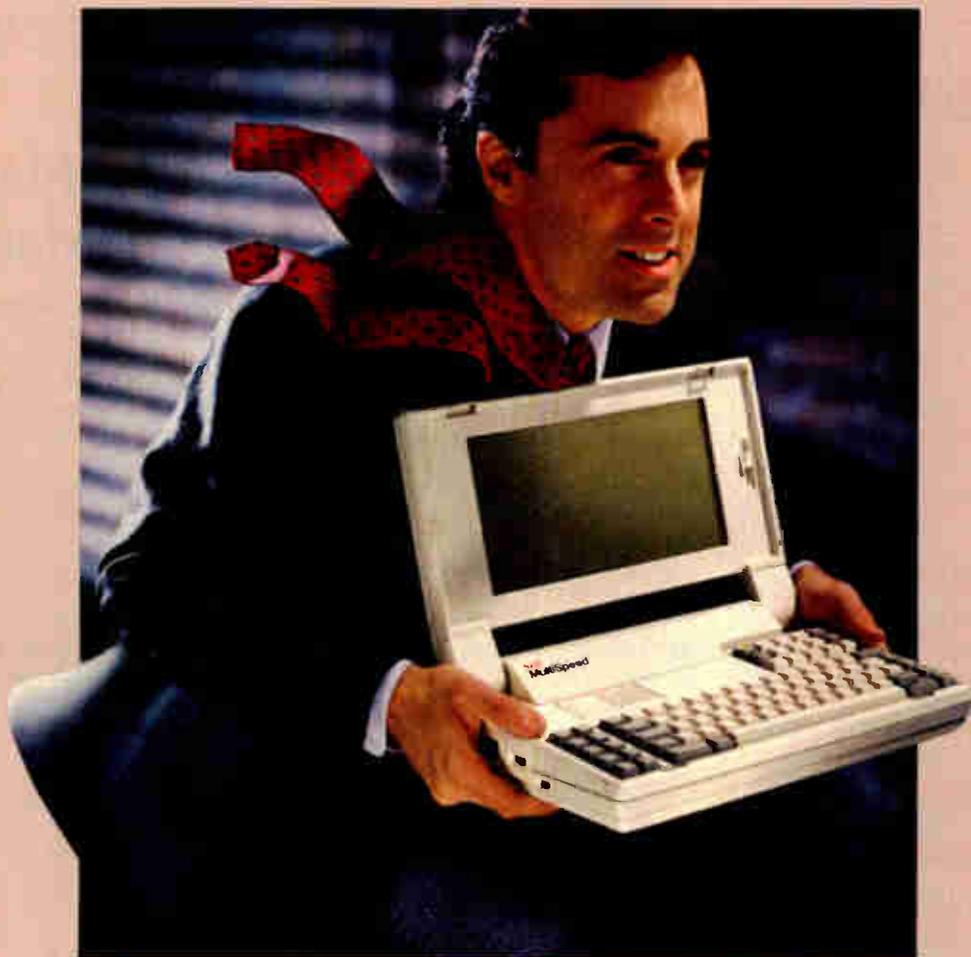


Photo 2: The Macintosh II's multiple-screen desktop. The Mac II automatically configures the desktop to be the union of all active video devices. Windows and icons can be dragged between screens and still display properly. "Well-behaved" application programs will be able to use the extra desktop area. The program in use is an unmodified version of *Cricket Graph 1.0*, and as you can see on the color monitor, the Mac II supports the old `QuickDraw` fixed-color scheme. The *ScrapBook* shows an earlier version of the chart and demonstrates the new color `PICT` format.

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an 80287 math coprocessor chip, and it will include 1 megabyte of memory for the 80286's exclusive use (with the possibility of expanding that to 4 megabytes).

This card will emulate both the IBM monochrome and CGA (color) boards and the Hercules monochrome text/graphics board in software. It will also be able to use the Macintosh SE mouse to control mouse-based IBM PC applications.

UNIX on the Macintosh II

Since UNIX is multitasking, the Mac II will need the Motorola 68851 memory management chip (which Apple will make available to Mac II owners). Apple made no announcement regarding a UNIX product, but Jean-Louis Gasse, vice president of product development at Apple, spoke of a version of UNIX that would contain 4.2 BSD (Berkeley Standard Distribution) features. Such a version, he said, would have to boot up the machine and would take over the system, turning the Macintosh into a "vanilla" UNIX machine; a future version might give programs access to the Macintosh ROM as a library.

Pricing and Availability

Although Apple disclosed no prices, one spokesperson quoted a price of between \$4200 and \$4300 for the basic Macintosh II (one floppy disk, 1 megabyte of memory) with the video card and a monochrome display and a price of less than \$6000 for the basic Mac II and the color display. Apple gave us no indication of how much an internal hard disk or a video board upgrade would cost. (A list of the official prices will be on BIX by the time you read this.)

Apple plans to ship the Mac II sometime in the second quarter of this year. Because of the dissimilarity between the Mac II and earlier Macintoshes, no upgrades are possible. Also, Apple does not plan to reduce the price of either the Macintosh 512KE or the Macintosh Plus because of the Mac II's introduction.

Caveats

We wrote this article after two visits to Apple in December 1986 and January 1987 (this included discussions with the hardware and software design team), about a day's worth of hands-on experience with the Mac II, study of three binders full of technical documents, and several follow-up calls to the Apple staff.

The design team described both the hardware and software as "late alpha." This means that the final hardware (and especially the software) may differ somewhat from the details of what we've described here, but the overall design will

be the same. In particular, any performance times measured in seconds should be taken as "ballpark" estimates.

Observations

Overall, we were very impressed with the machine. The Macintosh II is generally 3 to 4 times faster than a Mac Plus, except when it is dealing with a lot of transcendental math, in which case it is between 30 and 40 times faster (see the text box

"Comparing the Mac Plus, the Mac SE, and the Mac II"). The normal actions of a Macintosh user—opening, moving, resizing, and scrolling—were effortless because they were very quick. One of the slowest operations, scrolling a window of color information, was noticeable but not objectionable—somewhere around one second to scroll the contents of a full-screen color window about an inch.

Both the monitors have an area of 640

Comparing the Mac Plus, the Mac SE, and the Mac II

Although these timings shouldn't be considered as gospel (after all, we worked on machines that weren't finished yet), we think we can draw some conclusions about how fast the three machines are relative to each other.

Here are the overall conclusions: The Mac SE is about 10 percent to 20 percent faster than the Mac Plus, and the Mac II is roughly 3 to 4 times faster than the Mac Plus (except in applications where heavy number crunching is done, in which case the Mac II can be 30 to 40 times faster). The paragraphs that follow

will explain these conclusions.

Figure A shows the results of running some standardized tests on the three machines. A bar's height shows how much faster a machine is than a Mac Plus, and the number on top of the bar is the number of seconds it took to run the test.

The first three programs are standalone programs compiled by Lightspeed C, version 2.01. "Quicksort" is the standard BYTE sort benchmark. "Dhrystone" is the Dhrystone benchmark, version 1.1; this test simulates an average program by executing a known mix of control, assignment, and proce-

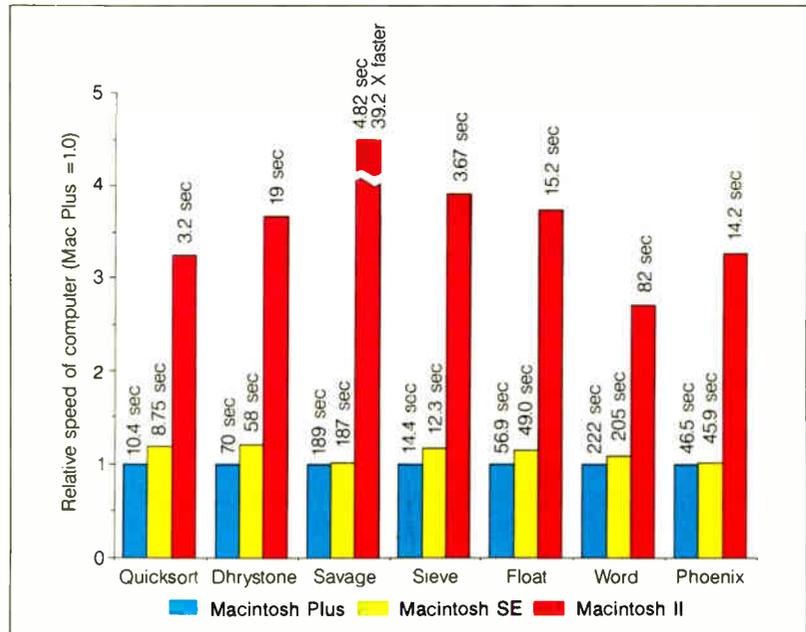


Figure A: Relative performance of Macintosh family computers. The length of a bar tells how much faster a given computer is than a Macintosh Plus when running a given program. The number over each bar tells how long a program took to run on a given computer.

by 480 pixels, which is 1.75 times the size of the Macintosh screen. Since most Macintosh applications will let you use this extra area, some of them were easier to use just because of the larger screen. The monochrome screen measures 12 inches diagonally, and the color RGB screen measures 13 inches. "Wonderful," you may say, "finally, a larger screen for my Macintosh!" Well, yes and no—it is larger, but it's also showing

more pixels in each direction. Actually, both Mac II monitors have about the same pixel per inch density as the old Macintosh.

The precision of the color monitor is remarkable. When it was displaying a monochrome image, we found ourselves thinking we were looking at the monochrome monitor—which means that the monitor can display true black-and-white dots, even at the edge of the screen, with-

out color fringes. This is an important factor when you remember you may be reading text, often as small as 9 or 10 points, on this screen for long periods of time.

Another remarkable quality of the Mac IIs we tested was their stability. Even though these were late-alpha prototypes, most of the software we tried out—software designed for the older Macin-

continued

ture statements. Its result is usually expressed in dhrystones per second, but here we used the number of seconds needed to execute the test. "Savage" does a large number of transcendental functions (e.g., sine and exponentiation). The Mac II's relative performance of 39.2 times faster is due to its use of its 68881 floating-point coprocessor.

The next two tests are stand-alone programs compiled using Microsoft Compiled BASIC, version 1.0. "Sieve" is one iteration of the Sieve of Eratosthenes. "Float" is a test of multiplication and division.

"Word" gives an indication of a machine's video display performance by smooth scrolling through a 63K-byte Microsoft Word document (we used Word 1.0). The time given in figure A is for the Mac II using a monochrome display (1 bit per pixel).

Finally, "Phoenix" exercises the graphics and the SANE numerics package heavily by measuring the time that a machine takes to transform a wire-image approximation of a sphere to a drawing smoothed with unframed faces; we used Dreams of the Phoenix's Phoenix 3D, version 1.2, three-dimensional program.

Remember, one key concept of the Mac II is that it lets the user decide how many colors to use on the screen at a time, with fewer colors giving better performance. Figure B bears this out. For the Mac II, it plots the number of bits per pixel versus the time required to smooth-scroll through a 63K-byte Microsoft Word document. As you can see, the relationship is almost linear. Though the Mac II using 1 bit/pixel performs 2.71 times faster than the Mac Plus, that performance degrades to 1.79 when using 4 bits/pixel (16 colors) and

1.28 when using 8 bits/pixel (256 colors).

One final set of figures comes from looking at the role the 68881 floating-point coprocessor plays in the performance of the Mac II. Normally, this can't be estimated because the 68881 is used automatically by system software. However, Apple had a demonstration program that did three-dimensional plots using no 68881 support, using the 68881 driven by the SANE numerics package (most applications will use it this way) and using the 68881 directly. The figure we used, Sombrero, is a

common one that uses the sine function a great deal to create a figure of concentric ripples.

The times (and their respective ratios) are no support, 1165 seconds (1.0); SANE support, 261 seconds (4.46 times faster); and direct support, 37 seconds (31.5 times faster). The most important figure is the middle one because many existing applications use the SANE package; so when they run on the Mac II, they will get this level (up to 5 times faster) of improvement—and the more time the application spends using SANE, the greater the improvement.

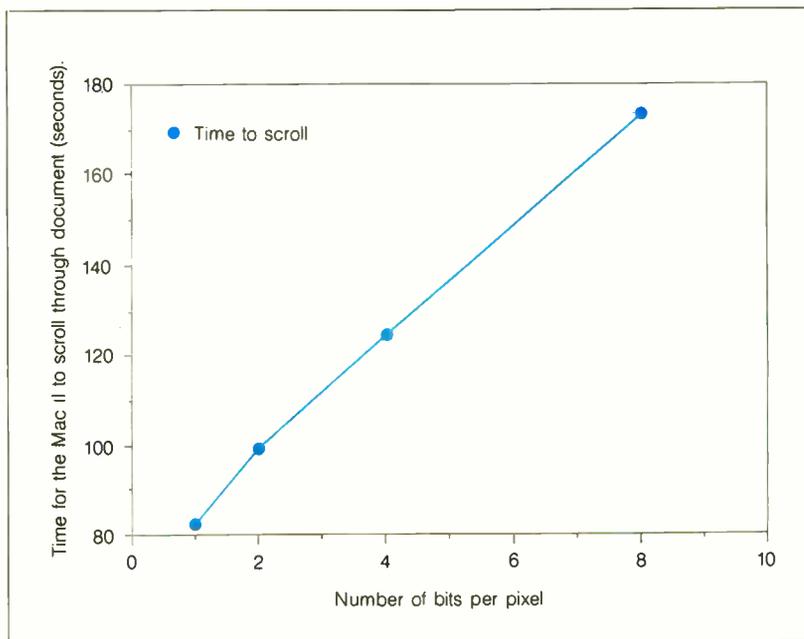


Figure B: Macintosh II video display times as a function of the number of bits per pixel on the video display. As this figure shows, the more bits per pixel (or, equivalently, the more colors that can be displayed on-screen at one time), the longer the Macintosh II takes to scroll through a document of a given size.

toshes—worked fine. The prototypes crashed only once or twice in several hours' usage (which is far more stable than most prerelease machines we see). We feel this is a testament to the stability of the machine's hardware and software architectures and is indicative of the quality of the hardware and software to come.

The bottom line on software compatibility is this: Mac software developers have had for quite some time now a list of guidelines to follow to ensure that their software would be compatible with future machines. Most companies have fol-

lowed those guidelines, and their software will run on the Mac II (Apple claims "greater than 95 percent" compatibility). So the more recent your software and the more conscientious the software company, the more likely your old software will run correctly on the Mac II.

One concern we have involves the price and usefulness of any kind of MS-DOS compatibility card. In our experience, such cards always sacrifice some performance in the emulation of MS-DOS and cost as much as or more than an equivalent IBM PC clone. Another concern is

that Apple told us that the third-party Mac SE and Mac II cards would use software to simulate and display the PC color and monochrome screens. The Commodore Amiga 2000's MS-DOS card uses hardware to maintain the screen's contents and software to display them and still cannot completely update the display. We feel that the all-software approach (for both the contents and the display of the MS-DOS cards) will either be too slow or will eat up too much of the processor's time. However, we will all have to wait for the products to come out before we can make any final judgments.

Though NuBus peripheral cards will be slow in coming, they will nevertheless be extremely important to the future of the Mac II. Many of the add-ins to the old Mac that required "major surgery"—memory upgrades, internal hard disks, and 68020 processors—are either included in the Mac II or are already planned for. Still other enhancements, like a full-page video display and other ideas we haven't thought of yet, will be much easier (and therefore much more likely) to be developed.

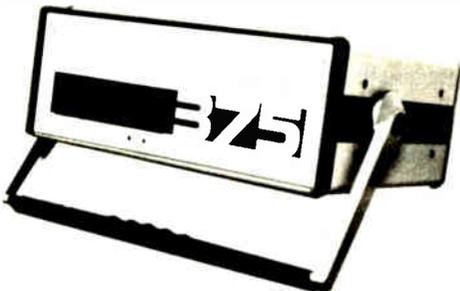
Conclusions

Apple has come a long way since the first 128K-byte Macintosh (with 64K ROMs) was introduced about three years ago. Now Apple has a true product line with the Macintosh 512KE, the Macintosh Plus, the Macintosh SE, and the Macintosh II, with prices from less than \$2000 to more than \$6000. The Macintosh is even affordable, with the bottom-of-the-line Mac 512KE having four times as much memory and twice as much ROM and disk storage, all for a street price slightly more than half the original Mac's \$2500 price tag.

Often, a new machine with new features has an uncertain future. Will enough people buy new machines to prompt software developers to create new software that brings out its potential? Will enough programs come out to prompt the public to buy new machines? The Mac II will have some of this inevitable chicken-and-egg problem, but not as much as other machines. Mac II applications are not so much built-from-scratch implementations as they are bells and whistles added to a product that already has a large, established market. Also, both developers and buyers have been—no other word will do—*lusting* so much after these added capabilities that the only limitation, we think, will be the time it takes developers to learn how to use them. Just as the Macintosh has literally changed the way we compute, we're looking forward to the innovations the Macintosh II will make possible. ■

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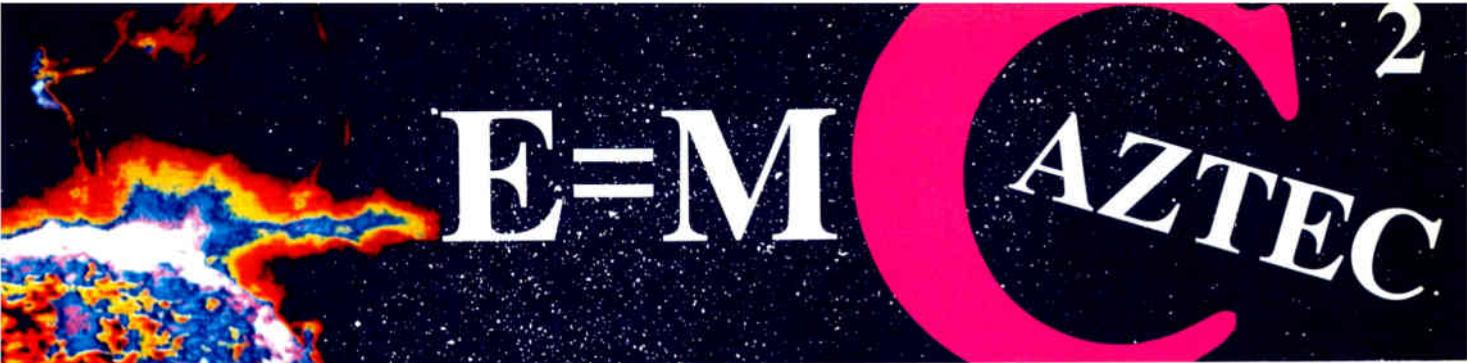
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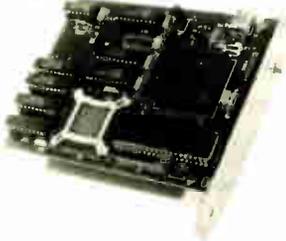
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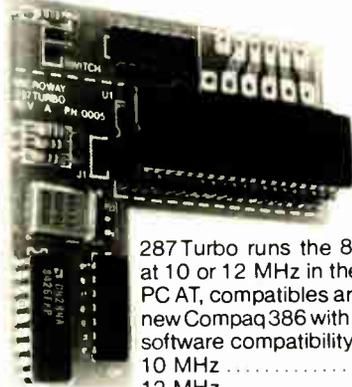
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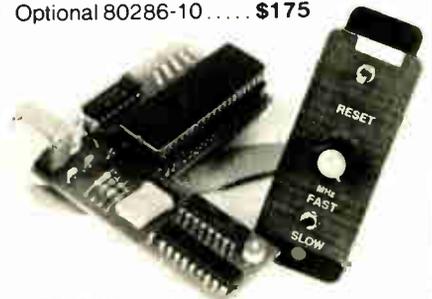
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Steve Ciarcia

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It was awful! The smell down here was something. We all have glorious thoughts when we see pictures of forests with the sun gleaming through the tree boughs illuminating little patches of the underbrush. Well, there I was lying in one of these patches with my nose nestled into the leaves, and I assure you that the wondrousness of the scene lost something between the picture and here. Two-dimensional photographic representations of forests always seem to leave out little things like the odorous admixture of animal droppings, wet decaying vegetation, and the cast-offs from a variety of six- and eight-legged members of the animal kingdom.

Don't get me wrong. I love forests. I even live in one (it's a forest by Connecticut standards, anyway). But crawling on my stomach through a swamp in November is not the same as having a picnic in the state park under the pines. This surely was different. A matter of life and death of sorts. Well, not really death, more like losing the *big* game.

I could hear some rustling off in the distance. Since it was November, practically all the leaves were off the trees and there wasn't much to hide behind. Fortunately, the leaves had not yet lost their fluffy and crunchy consistency. They provided me with cover and concealment as well as alerting me to any approaching foe. Well, not a foe exactly; more like an

Steve Ciarcia (pronounced "see-ARE-see-ah") is an electronics engineer and computer consultant with experience in process control, digital design, nuclear instrumentation, and product development. The author of several books on electronics, he can be reached at P.O. Box 582, Glastonbury, CT 06033.

overzealous friend, out for blood.

I had been running, walking, and now crawling through these woods for a good four hours. There was no time limit. It would just get darker, colder, and damper. I shivered a little to think that I had to stay in this hole in the underbrush much longer, but I had heard a noise in the distance. There was no way to know that I wasn't in the cross hairs of someone's gun sight already and they were waiting for me to make the first move.

Making the Move

My head pounded with anxiety. This was supposed to be a game, but it seemed more than real. I was both the hunter and

the hunted. I could play the defensive role and stay forever buried in the leaves, or I could be a man, jump out from cover, and get blown away!

The darkness would only compound my situation. I had to either make my way back to the house and concede defeat or shoot it out here in the woods and—I hoped—be the victor. Either option was not going to be easy. If I could hear my opponent, he would most assuredly hear me when I moved.

He didn't even have to be that close to score a hit, a couple of hundred yards and I was still dead meat. My only hope was that if I moved quickly enough, I could get off the first shot. In any case, once I

continued

Illustrations by Elliott Banfield



There was no way to know that I wasn't in the cross hairs of someone's gun sight.



"Zeeeeooooooooohh!"
it blasted forth
and echoed loudly
through the
forest.

fired, my position would be known.

So move it is. Back toward the house, wherever that is (after wandering around in two square miles of woods for four hours, I wasn't exactly sure where home was). First, I had to be ready for action. I moved my hand down to the laser gun: It was time to reenergize it for possible action. I carefully wrapped my fingers around the pistol grip, ready to click the firing switch to the first position. But at that moment, the strangely attractive blue, silver, and black laser gun seemed less a weapon than merely the article of engineering curiosity it started out to be. It would become a weapon only when I acted to defend my engineering ego by proving that it worked.

For months it seemed, every time I watched TV or opened a mail order catalog I saw ads for laser tag games. The TV commercials had all these svelte young people somersaulting all over the place shooting infrared pistols at each other. Without considering the morality of the game itself, it bothered me that someone would spend \$100 for such a game when it had a range of only 50 feet. In fact, one user told me that one of the games couldn't be used indoors. All a player had to do was aim at the ceiling and the reflection triggered everyone's hit indicator.

It seemed to me that the real violence was having to be close enough to "see the whites of their eyes" to score points in that game (you might as well go back to using rocks and clubs). The skill of the hunt and the escape was lost because of the limited range of the infrared pistols. Having to be in such close proximity seemed more like hand-to-hand combat

to me and hardly qualified as a gentlemanly sport. It was just a bang-you're-dead game, played the same as it was when you were a kid.

Here was a challenge: I could take a stone age game and add an element of modern skill and cunning to it. I could build a pair of laser guns that would let us play a superior version of the game. In pursuit of such a challenge, cost was no object.

I don't remember exactly how it went from concept to reality, but it might have had something to do with mentioning possible technological improvements on the game at a computer club meeting. With an audience yelling, "Yeah, great!" and "Ya gotta do it, Steve," it became a case of putting the project where the mouth is. In any case here I am, lying in a damp hole sniffing decaying vegetation, trying not to be the target of my own invention.

Two of these laser guns existed, and one was in my hand. The other was possessed by my friend Jeff (former friend if he got the drop on me). They were in fact real laser guns I had designed using readily available components and a little mad-scientist genius. The pistol housing started life as a heat gun. To that I added a 2-milliwatt helium-neon 12-volt laser, a 4 by 32 telescopic sight, xenon flash lamps, a phaser sound synthesizer, and assorted electronics. The finished product was truly an imposing sight.

The first click of the trigger switched on the power from the battery pack attached to my belt. To indicate that it was energized, an LED on the pistol butt below the scope glowed red. I pushed my

safety glasses up a little so that I could see the LED just to make sure. Since the glasses were tinted blue and intended for protection against He-Ne laser radiation, the light from red LEDs was also filtered. Fortunately, only red light was affected, and I could see everything else very well.

The laser gun was energized and ready. One more squeeze on the trigger to the next position and it would fire a timed one-second laser burst as well as emit a loud phaser sound. The red He-Ne light would come out the front end and be mostly invisible in daylight. Since it was dusk, with a damp mist hanging about six feet above the forest floor, a shot would look like a light saber in *Star Wars*.

The mist unfortunately also affected the pistol's range. While the laser gun had been successfully test-fired at 250 yards, I estimated its potential range at a quarter of a mile. Tonight, however, trying for much more than 100 yards could prove futile, or should I say fatal.

There was more than the phaser sound to give me away when I fired. Simultaneously with the laser and phaser, bright lights on either side of the gun would flash. In the dim light, it would most assuredly give my position away.

I fingered the trigger but was careful not to accidentally press it to the fire position. That would have to wait till later. Now I either had to escape back to civilization or go on the attack and seek out my opponent. As I slowly rose from my covered position I decided to choose the more realistic avenue, try to sneak out and if cornered, then fight back.

I stood up. The electronic target on my chest (another technological innovation) felt awkward and heavy, but I felt some consolation in the fact that it was the ultimate target rather than me specifically. Of course, like the laser gun it had to have more spice than the off-the-shelf game. It was about the size of a cake pan cover with four rectangular pods around the perimeter. Rather than just flash a little LED (which you couldn't see through the safety glasses anyway) to indicate a hit, this target sets off a loud noise and four xenon strobe lights (the pods) when the laser hits it. If you can shoot at something from 100 yards away, it makes sense that you and the opponent should know when you hit the right thing. If not, the noise and light emitted from your gun will alert an opponent to your presence and the hunter becomes the hunted.

With full knowledge of the weapon and considerably less about the terrain, I decided to make my way out and back to civilization.

"So I get caught. So I get zapped. The humiliation is only temporary. Just because I designed this super tag game

doesn't make me an expert at it. Damp woods, yechy swamps, cold mists, I've had enough! Take me, I'm yours. But wait, perhaps I can sneak out first."

I listened but heard nothing. "No hunter within earshot? Which way should I go? North, toward the highway, or south, toward the center of town? By the way, which way is north? There's no sun, I'm out here in the dark woods, and there's no compass on this stupid gun!"

Feverishly glancing around for some indication of a suitable direction, I was startled by a rustling in the leaves. As I quickly swung in that direction with the laser gun held at my waist like an Uzi, I clicked the trigger to the firing position and fired a burst of laser light in the direction of the noise.

"Zeeooooooooohh!" it blasted forth and echoed loudly through the forest.

Because of the low hanging mist and darkening light, it was like setting off a flashbulb. I could see the beam pierce the darkness and impact 20 feet up the side of a tree about 50 yards away. "Nice shot, Ciarcia," I thought sarcastically, as I was blinded by the flash.

It was only a one-second burst, but it seemed an eternity. I knew instantly that I hadn't hit the target since there was no corresponding flash of light from my opponent's hit detector, and I doubted he'd be sitting in a tree waiting for me. My vision slowly returned.

Again there was a rustling of the leaves. This time it was louder. A sudden jab of fear and vulnerability struck me. I dove forward under a small pine tree with the laser gun held in both hands out in front of me. I nervously waited for the laser to recharge.

Just as I was about to consider another alternative, something jumped about 10 feet in front of me.

"Yieeee," I yelled as we both saw and startled each other.

Two eyes stared back, conveying a look of curiosity rather than anger. I must have looked very strange to the brown floppy-eared rabbit who sat there looking at me. He must surely have been laughing to himself. I breathed a sigh of relief and felt a little foolish. If I felt unnerved after a run-in with a fuzzy little rabbit, I surely would not be successful in this "game." Perhaps I wasn't cut out to be a Green Beret after all.

"I give up, Jeff. I'm going home," I said to myself. "Home?" I wasn't exactly sure where home was. "Oh what the hell," I thought. I switched the laser gun back to the off position to conserve batteries and struck off in the same direction as the rabbit.

The rabbit was pretty smart after all, and I soon came upon a path. While I

really wasn't playing the game anymore, just to be on the safe side I stopped every hundred feet or so and listened. After coming this far and surviving so long, it hardly seemed appealing to get ambushed. Who knew at this point whether I was still the hunted or not. For all I knew, Jeff went back to the house hours ago and was now sipping a warm cognac.

I had walked a good third of a mile along the path. It was very overgrown where I first encountered it, but now the path looked well traveled. "I must be approaching civilization again, but I haven't seen or heard . . . But wait, is there a clearing ahead? I can see lights and hear voices."

The clearing wasn't a meadow or anything. Instead, it was a traffic circle at the end of a housing development that bordered the woods.

I had come out barely a quarter of a mile from my house. I approached the lights and voices cautiously and listened. "Officer, please. You've got to understand that this is not what it looks like. No! . . . I mean yes, it's a real gun, but it's not a *real* real gun!"

Through the bushes I could see Jeff trying to explain to two police officers why he was sneaking around the woods looking like a cat burglar from the 25th century and carrying a ray gun. Jeff's appearance certainly didn't help things. He had a laser gun and the futuristic-looking metallic target on his chest and helmet, revolutionary sixties long hair, wrap-around blue safety glasses, black clothing, and camouflage-greased face. No

wonder someone called the police.

While not close enough for the two officers or Jeff to see me, I could hear the nervous tone in his voice as he continued his explanation. "You see, officer, it's a *laser gun!*" He raised the blue, silver, and black weapon so they could see it better.

These guys were no babes in the woods. They had been to the police academy and had apprehended their share of perpetrators, but they had also seen science fiction movies. Fantasy and reality can be hard to differentiate on a dark street corner. I could sense their anxiety at such a statement and saw them suddenly jerk back defensively as he motioned with the laser gun.

I fully expected the two officers to pounce on Jeff, thinking he was making an offensive move. They would be heroes in the eyes of the community, with tomorrow's headlines reading "Cops Foil High-Tech Hit Man" or "Cops One, Phasers Zero."

Jeff still didn't see me as I walked toward him. Like him, I had a black jacket, blue jeans, and the same strange-looking electronics. This terrorist attire combined with the laser guns certainly wasn't going to make the explanation any easier.

I removed my safety glasses as I approached the two policemen. Jeff continued trying to explain. His voice sounded stressed, and the pitch became higher. "But it's just a game! I'm not threatening anyone. Yes, it's a real laser . . . but it's not a *real* real laser!"

continued



Two eyes stared back, conveying a look of curiosity rather than anger.

"Officer, perhaps I can help." I could see the immediate relief on Jeff's face as I approached. He didn't have to say he was glad to see me. That much I expected. What interested me more, however, was the sudden metamorphosis from frightened animal to logical human being again. The wild-eyed expression I previously observed was instantly replaced with a look of astonishment at seeing me. I suppose I should have expected that. After all, we had been tracking each other for five hours.

I continued instructively, "My friend and I are working on a technological experiment for a national magazine article. The laser guns you see with us are merely a highly improved and significantly more powerful version of the guns often seen in arcade games. While theoretically capable of burning holes through the steel of a police car, this particular gun uses—" A screech of tires interrupted my explanation as another police car rounded the corner and approached our position.

I was about to continue explaining the design attributes of my laser gun in contrast to the death ray they anticipated it to be, when I looked at Jeff. His expression had changed from confidence to wild hysteria. It was almost telepathic. I could hear his mind screaming, "What are you doing? What are you saying? They're going to put us in jail and throw away the key! Tell them it's a game! Tell them it's a game!"

In the split second that I watched him and sensed his hysteria, I saw him move his finger to the trigger button on the gun. When I saw the LED light up on the back of his gun, I knew it was now armed. Almost instinctively, perhaps the result of

anticipating this moment during the past five hours of the hunt, I too clicked on the power to my gun and charged the laser. Was he still playing the game? Perhaps he was going over the edge? In either case, I wasn't going to be a sitting duck.

Completely oblivious to the question being asked of me by one of the officers, I stared at Jeff and watched for his next move.

My entire consciousness seemed focused on this one activity. Perhaps if it had been high noon in Dodge City, Kansas, rather than a residential street in Connecticut, the standoff would have been less surprising. At the instant I saw Jeff swing his gun up to bear on me, I did the same. We both fired at the same time! We both hit the targets!

The two lasers fired, hit their targets, and harmlessly reflected off the shiny surface into a hundred dazzlingly brilliant rays. Without a doubt, the phaser sounds and lights on the laser guns startled the two policemen (who instinctively assumed defensive postures), but the coup de grace was the eight xenon flash lamps going off at the same time on the hit detectors. I was even a bit surprised. I had designed them to be seen at 100 yards. At 10 feet they were quite a bit brighter.

The world of fantasy immediately dissolved into cold, hard reality as I again became aware of our surroundings. I knew our goose was cooked when the second police car came to a screeching stop, both doors flew open, and the next word was, "Freeze!"

A Serious Game of Tag

Before everyone sends me letters suggesting that I am advocating war toys, let me reiterate that I approached this as an engineering project. The choice of subject material was primarily determined on the basis of how much fun I'd have relating

the story about it. April articles have become a fun break in the otherwise grueling schedule.

While I could have added voice synthesis and recognition to a Betsy-Wetsy doll instead, it surely would not have been as much fun to tell as what I've just described or the night of the computer club meeting at a crowded Denny's restaurant when I walked in with the laser gun. But that's a story for another time . . .

The idea for this story came about because of all the pre-Christmas fervor over laser tag. In all honesty, I must say that I never bought or used the laser tag game, and my comments on it are based on what other people have told me. When I first saw it, I felt it was too expensive for such a short-range device, and close-range combat didn't appeal to me. After I had made the decision to use it as the subject and tried to acquire a laser tag unit for comparison, none were to be found anywhere. The apparent popularity of a souped-up TV remote control finally convinced me that I should build the real thing.

I'll leave it to you to decide whether you think this story was fantasy or reality and whether the laser gun was just a paper project. By the way, you might want to check out the photo below.

Circuit Cellar Feedback

This month's feedback begins on page 58.

Next Month

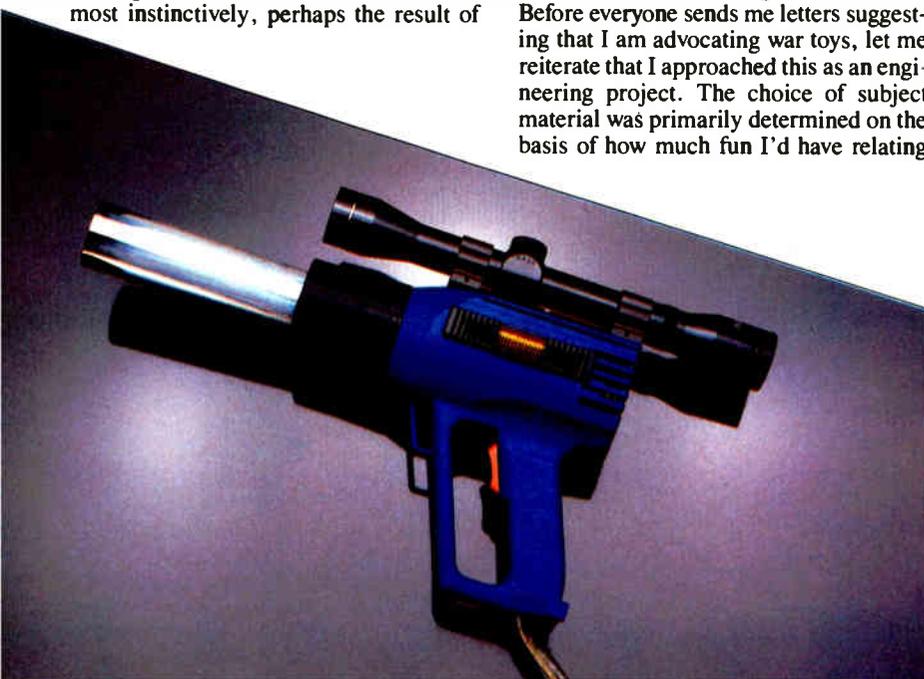
Steve will show how to build the Circuit Cellar video digitizer. ■

Editor's Note: Steve often refers to previous Circuit Cellar articles. Most of these past articles are available in book form from BYTE Books, McGraw-Hill Book Company, P.O. Box 400, Hightstown, NJ 08250.

Ciarcia's Circuit Cellar, Volume I covers articles in BYTE from September 1977 through November 1978. *Volume II* covers December 1978 through June 1980. *Volume III* covers July 1980 through December 1981. *Volume IV* covers January 1982 through June 1983. *Volume V* covers July 1983 through December 1984.

There is an on-line Circuit Cellar bulletin board system that supports past and present projects. You are invited to call and exchange ideas and comments with other Circuit Cellar supporters. The 300/1200/2400-bps BBS is on-line 24 hours a day at (203) 871-1988.

To be included on the Circuit Cellar mailing list and receive periodic project updates and support materials, please circle 100 on the Reader Service inquiry card at the back of the magazine.



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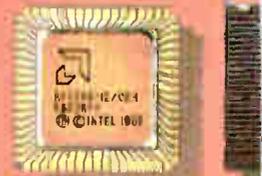
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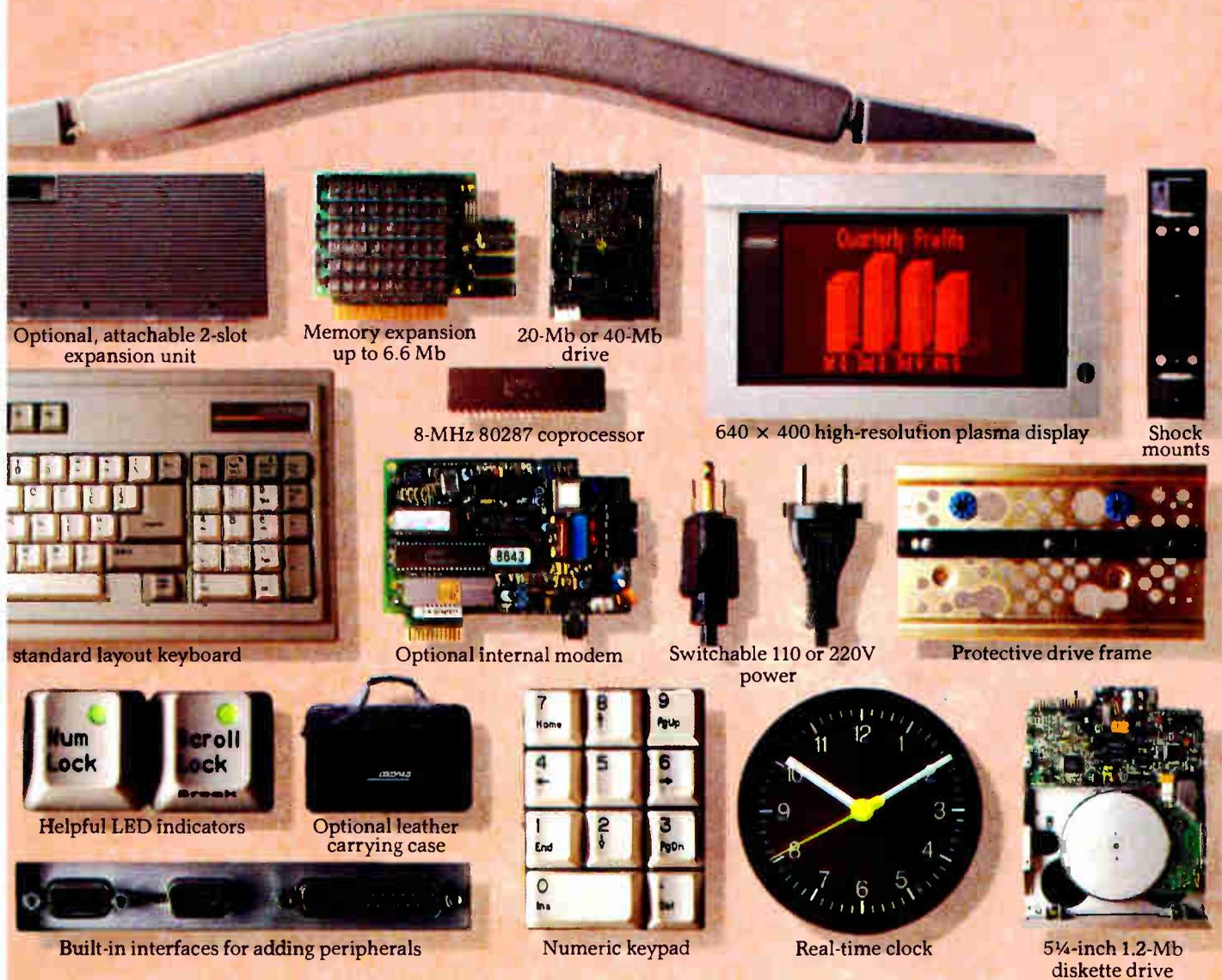
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This COMPAQ PORTABLE III
is so busy in the office,
it doesn't get out much.



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Build BERT, the Basic Educational Robot Trainer, Part 1

*Even a child can program this talking robot,
built from off-the-shelf components*

Why is it, I asked myself, that very simple robots, even commercially available ones, require so much training to operate? This, I decided, was a problem, and I wanted to do something about it. What I eventually did was write a menu-driven, interactive control language intended to be simple enough for a ten-year-old to use. As it turned out, during field tests with children, I found that any child who could read could program a robot within one minute of hitting the keyboard.

This, I felt, was progress. The next step was to design a robot that my fellow computer club members could build and program. That was how BERT was born.

Simplifying the Project

My goal was to reduce the complexity of the project for those building a robot for the first time. Accordingly, all the hardware, the software, and the little bits in between have been designed and tested already. All the circuits have been designed around off-the-shelf components rather than expensive, hard-to-get technology. Most of the mechanical parts (switches, speakers) are inexpensive enough to purchase new (as opposed to scrounging through the junk box). Parts such as the printed circuit boards, gearbox, and ROM are available from Amarobot in Richmond, California. (A complete kit is available as well. See address at the end of this article.)

To build BERT (see photo 1), you will

Karl Brown teaches electronics at Vancouver Community College. His hobbies include computer hardware design and juggling. He can be reached at Vancouver Community College, Electronics Department, 250 West Pender St., Vancouver, B.C., Canada V6B 1S9.

need only commonly used electronics tools: a fine-tip soldering iron, wire cutters, pliers, and so on. Photo 2 shows BERT's circuit boards assembled and cabled together. Figures 1 through 4 are complete schematics of BERT's circuitry, and figures 5 through 7 are assembly and parts location drawings. These drawings should provide all the information you need to assemble BERT's circuit boards. To program him, you will need a device capable of transmitting ASCII code at 300 baud, with 7 data bits, no parity, and 1 stop bit. In other words, almost any computer with a serial port, or a serial terminal itself, can be used.

While developing BERT and BERTL, his programming language, I was able to

research and examine quite a few of the personal robots presently on the market. There was a wide range of on-board electronics, from a minimum of two driver chips to a maximum of a complete 68000-based system with a megabyte of RAM and two 500K-byte disk drives. The mechanics of all these robots were quite similar. The method of locomotion, almost without exception, was wheels powered by electric motors. Flashing LEDs for eyes, speech synthesizers, and obstacle sensors were found on nearly every "untethered" robot.

I determined that innovation was not really needed in the hardware. Rather, I felt that simplification was required in the

continued



Photo 1: BERT in the Amarobot kit configuration.

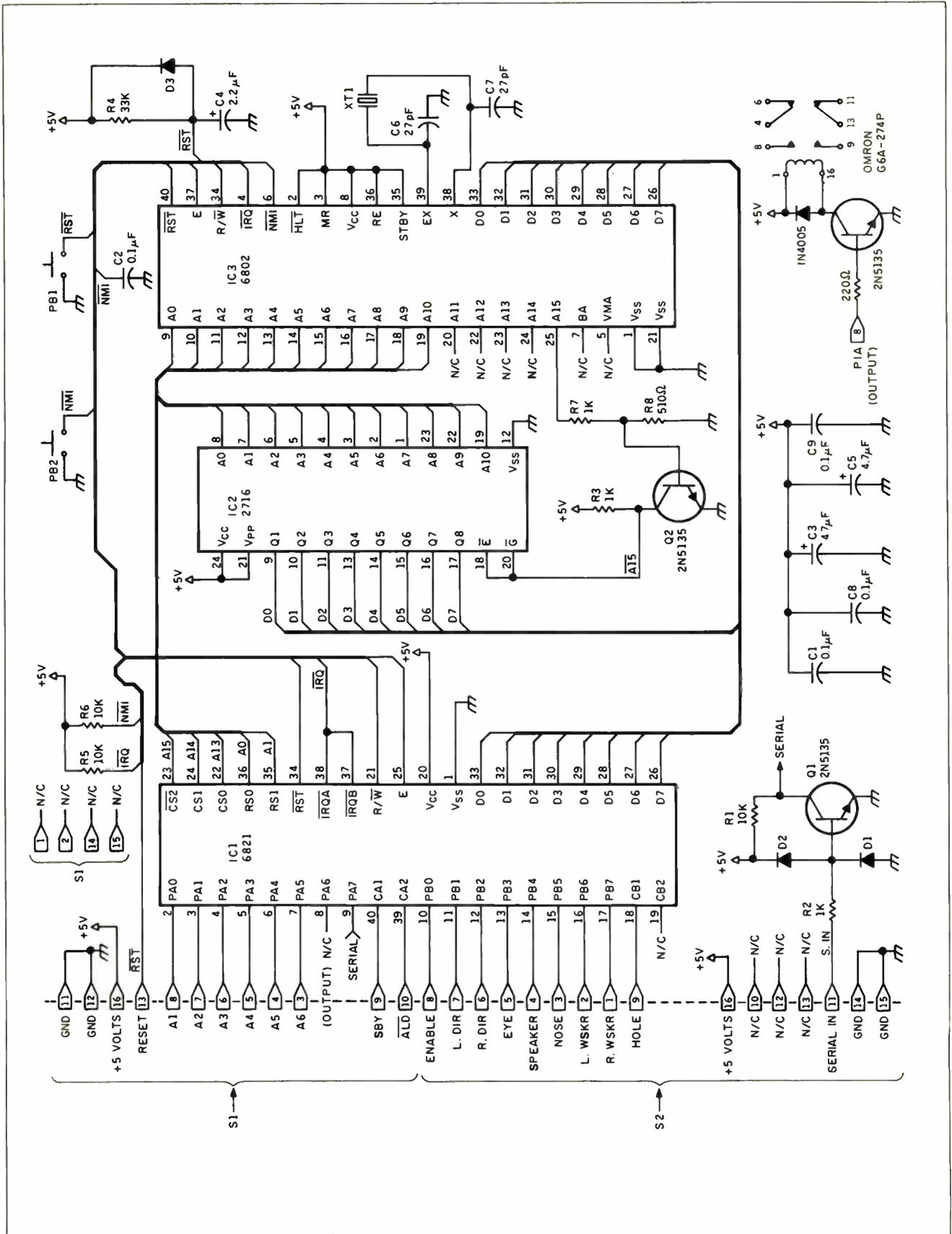


Figure 1: Schematic diagram of BERT's on-board computer.

software. It seemed to me that a different approach to robotics was needed. Instead of considering a robot as a robot per se, I started thinking of it as merely another peripheral for a computer. I felt that making a robot roam around should be no more difficult than making a printer print. In fact, I thought, I could actually treat the robot just like a printer.

Robot Printers

That is how I propose we control our robot—simply by sending it a string of ASCII text, which it will remember and then execute. The simplest command format I could think of looks like *Command, Parameter*, where *Command* is a single letter (say F for “forward”) and *Parameter* is a hexadecimal number (00 to FF).

As an example, let’s say we wanted our robot to traverse an area on the floor in the shape of a square. To accomplish this, he would have to execute the following maneuvers: move forward 30 centimeters, turn left 90 degrees, move forward 30 cm, turn left 90 degrees, move forward 30 cm, turn left 90 degrees, move forward 30 cm, and stop. Using the BERTL robot control language that I developed, that program would be F30, L15, F30, L15, F30, E.

The program could be written with any text editing program, EDLIN or WordStar (in nondocument mode) for example, and then sent to the robot via its serial port. After the last character (the E for “end”) in the program has been transmitted, the robot will beep, then wait for his forward sensor (the “nose” sensor) to be activated. Upon activation of the nose sensor, he will do the little “square

dance.” After the entire program has been executed and the robot is right back where he started, he will sit there and wait for the nose sensor to be activated again. Should the sensor be activated, the square dance will be repeated. The above sequence will continue until either the test button is depressed (executing the self-test procedure) or the on-board computer is reset via the reset button or by cycling the power.

Gears and Microprocessors

The first question apt to spring up about a robot is “What can it do?” Well, quite independently, BERT can beep, blink, talk, move forward and backward, turn left and right, and avoid obstacles. Let’s examine the hardware requirements necessary to enable our robot to perform these tasks.

Beep and blink: Beeping for attention can be handled by a speaker tied to a single bit of a parallel port. Simply toggle the bit every millisecond and the speaker beeps at 1 kilohertz. Blinking, another method of communication, is nothing more than an LED connected to another bit of our port. Toggling that particular bit will cause the LED to blink.

Speech: All we require for this task is two chips. A 28-pin speech synthesizer chip, an 8-pin amplifier chip, and a couple of capacitors and resistors compose the entire circuit.

Forward, backward, left, and right: For these movements, the minimum requirement would be two motors attached to wheels, with some sort of feedback to tell the on-board computer how far the wheels have turned. The next require-

continued

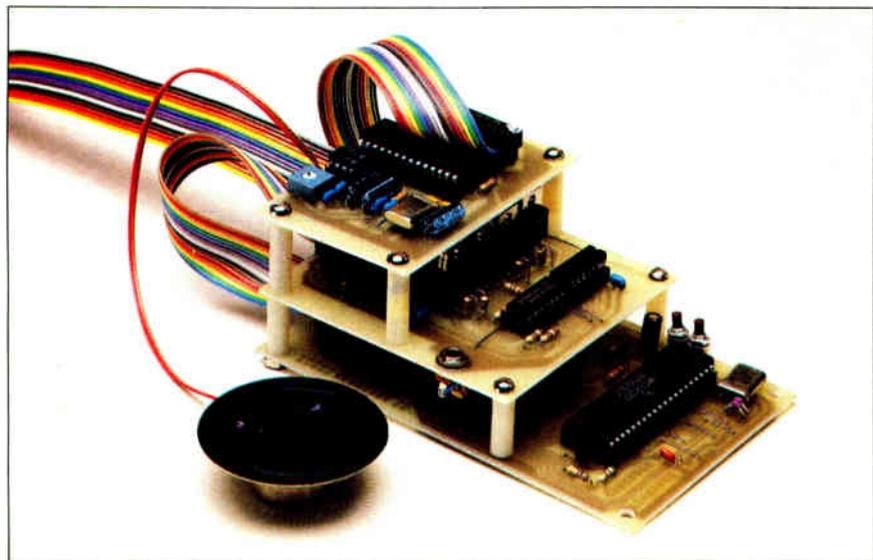


Photo 2: BERT’s circuit boards, from top to bottom: speech board, motor driver board, and the on-board computer, assembled and cabled together.

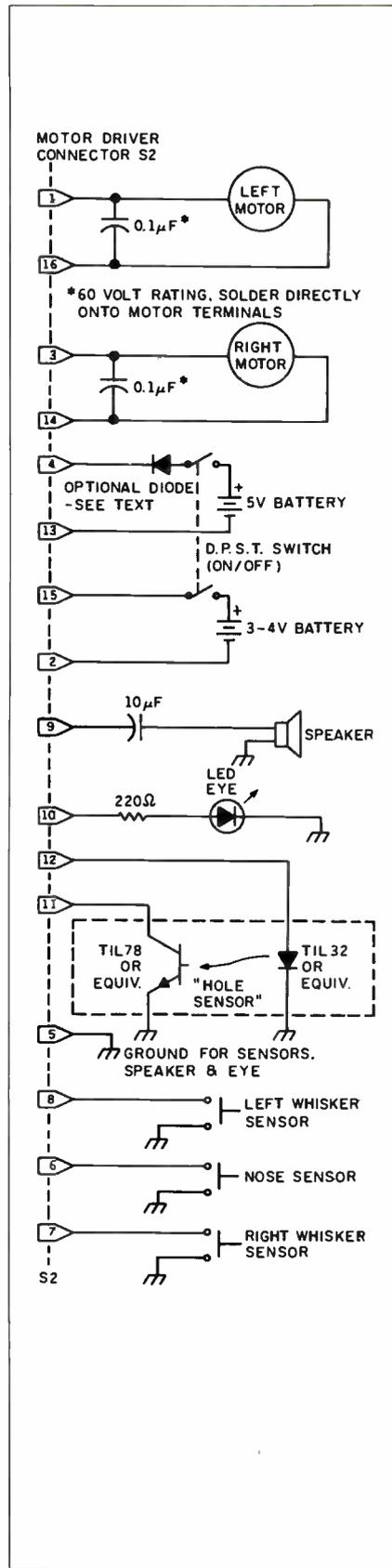


Figure 2: Schematic diagram of the robot base.

ment is some kind of motor control. I chose DC motors instead of the more common (in robotic circles) stepper type. Stepper motors rotate precisely the amount you tell them to. This ability allows designers to assume that they need not bother with positional feedback circuitry and software. This assumption is generally sound for disk drives and printers, where loads and environments can be maintained within design specifications. Hobby robots, however, are rarely allowed the luxury of a closely controlled environment. Hills, low batteries, rugs, and changing payloads cause a robot to stall or put widely varying strains on the drive train. If no feedback is obtained from the wheels, the controlling com-

puter is completely oblivious to any positional inaccuracies that may be the result of the above load problems.

Using a DC motor, however, demands that some sort of feedback from the drivetrain be used to control the motor's rotation. Thus, we have the benefits of feedback as well as the ultimate benefit for hobbyists: DC motors are cheaper.

Obstacle sensing: This can be tough or easy, depending upon how sophisticated we wish to be. The simplest (and least expensive) method would be to use a piece of wire and a switch. Not very glamorous, I admit, but certainly effective. A more elegant method would be to use an infrared proximity detector, a device that sends out a beam of infrared light and

then looks for the reflection. When the reflection passes a certain threshold of brightness, the detector circuit outputs a signal, indicating an object nearby.

Both of these methods can be thought of as accomplishing the same task as a cat's whiskers (apparently, felines use their whiskers as feelers to determine clearances). That is to say, their output is a binary "go/no-go" signal. Therefore, I shall refer to them hereafter as the robots "whiskers."

Obstacle avoidance: Here we are asking our robot to demonstrate some form of intelligence. Data can be gained about the presence of an obstacle using the whiskers. To actually do something about the obstacle requires some form of deci-

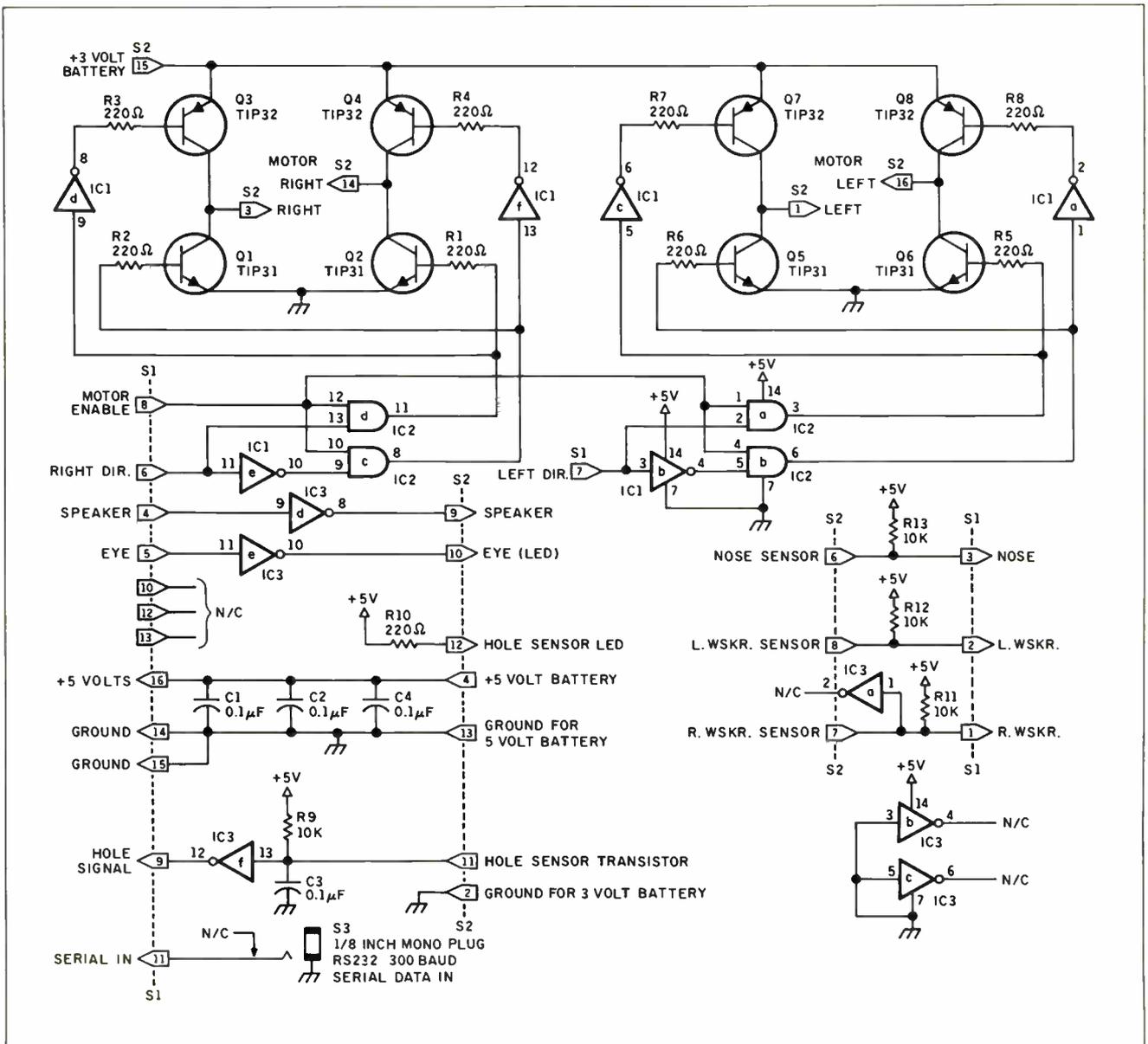


Figure 3: Schematic diagram of BERT's motor control board.

sion-making capability. An on-board computer (OBC) gives our robot this ability to make decisions based upon information gained by the robot's whiskers. BERT's OBC is a three-chip printed circuit board. The circuit design and microprocessor choice was influenced by two parameters: price and simplicity—in that order.

Power Supplies

How do we power our robot? If we were to use an AC power supply, the attendant power cord would severely restrict the mobility of the little beast. Batteries are the answer, but do we use rechargeable or disposable batteries? If rechargeable, shall we choose Gel-Cell or nickel-cadmium? How many hours of operation will we get before recharging is necessary? What type of battery charger should be used?

For the sake of simplicity and cost, I recommend that commonly available nickel-cadmium batteries and charger be used. BERT requires two power supplies (battery packs). This is necessary for two reasons. First, the OBC requires +5 volts (plus or minus 0.4 V). Most small DC motors require between 1.5 and 4 V. Second, small DC motors are electrically noisy. Connect a motor to a battery, then look across the battery's terminals with an oscilloscope. You will find spikes with an amplitude in the hundreds of volts. Obviously, a separate battery will be needed to power the on-board computer.

BERT's Specifications

BERT's brain consists of a 1-MHz Motorola 6802 microprocessor with 128 bytes of on-chip RAM, a 2K-byte 2716 ROM, and a 6821 PIA (peripheral interface adapter) used as two 10-bit parallel I/O ports.

BERT consumes 1 watt of DC power, and his motors consume up to 500 milliamperes. We download programs to BERT via an RS-232C, 300-baud serial interface. BERT uses LEDs for his eyes, and three switches for his nose and left and right sensors. He beeps from one small 8-ohm speaker and speaks from another, under control of an SP0256-AL2 speech synthesizer with a 64-word vocabulary.

BERT can test himself with a built-in self-test subroutine and can execute 15 different subroutine branch conditions. You can interface external devices to BERT through a 1-bit I/O port in the PIA. This can be used to initiate switch closure for activating external devices.

If you have ever tried to write machine language, feedback-driven motor control routines, you will be glad to know that our OBC's software is already written in

6800 machine code. It is supplied in the kit as a preprogrammed EPROM.

Putting the Pieces Together

In the following discussion, the schematic diagrams of the OBC (figure 1), robot base (figure 2), motor control board (figure 3), and speech board (figure 4) should be consulted for reference. (See also photo 2.)

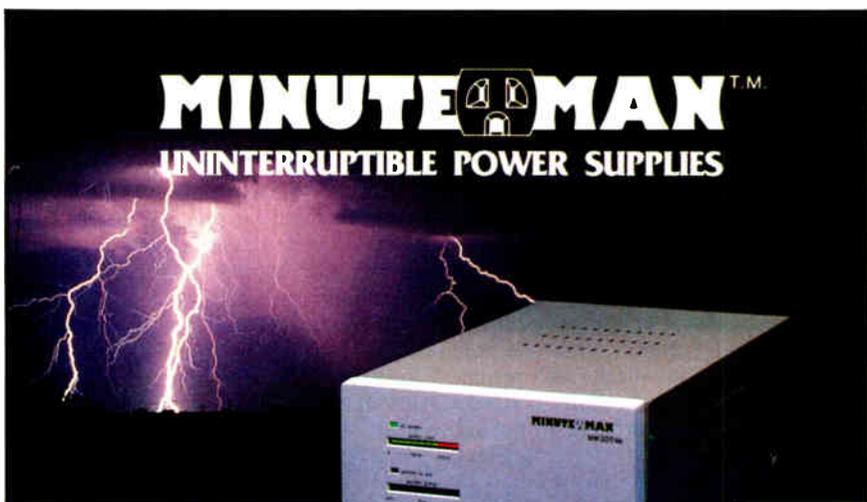
Assembly/parts location drawings of these boards (figures 5, 6, 7, and 8) show the location of all components, and the parts lists give a complete description of

part identification and values. These should be followed closely when you assemble and solder the printed circuit boards. In part 2 of this article, we'll interconnect the printed circuit boards and test them.

The Robot Base

The design of BERT's base is fairly straightforward. The main requirements are that the driving wheels be somewhere near the base's center of gravity, and each driving wheel must be powered by

continued



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its own DC motor. You can build your own base from scratch, buying some type of motorized toy and modifying it, or purchase the preassembled base from AmaroBot. I strongly suggest the latter.

BERT uses an optical "switch" to sense how many rotations the wheels have made. Looking at the schematic diagram of the robot base (see figure 2), you can see an infrared LED and its companion phototransistor labeled "hole sensor." These constitute the optical switch. If we were to place the LED on one side of a solid wheel and the transistor on the other, then drill a hole through the wheel, when the hole came around to the LED's position, light from the LED would fall upon the transistor. Since light from the LED causes the transistor to turn on, it would output a logic-low signal.

In the above scenario, with one hole drilled through the wheel, each revolution would equal one "unit." If you choose to build your own base or modify an existing vehicle, you must arrange the infrared LED and phototransistor in such

a position as to give the OBC some indication of how many units it has gone.

It is not absolutely necessary to drill the holes in the wheel itself. Since we are using small DC motors (which are typically high-speed, low-torque devices), there will probably be some sort of gear train involved. You could drill the holes in any convenient gear of the train. But I suggest that the gear you choose be near the end of the train (i.e., nearer to the wheel than the motor); otherwise the gear backlash could affect the accuracy of positional feedback.

The number of holes used will depend on the circumference of the driving wheels. A good point to aim for would be about one hole per centimeter of wheel circumference. For example, if your wheel were 9.6 cm in diameter, giving a circumference of 30 cm, then you would need 30 holes in the wheel. If, for the same size wheels, you were to choose to drill the holes in a gear instead, you would have to base the number of holes on the gear ratio relative to the wheels' circumference.

If you feel that building gearboxes, calculating gear ratios, drilling holes, and fabricating a bracket for the hole sensor is too much like work, you can purchase a gearbox with two motors, gears, and sensors completely assembled from AmaroBot. Due to the limited drive current of

the motor driver board, I recommend that the weight of the bare motorized base (less batteries, speakers, sensors, and electronics) be less than 4 kilograms. This will allow for approximately 2 kilograms of batteries and still leave us some payload capability (enough, say, for a small cat).

Base Population

The permanent inhabitants of the platform are shown in the robot base schematic (figure 2). These devices mount directly onto the base and connect to the electronics via one DIP connector (motor driver connector S2).

The sensors (nose, left, and right) can be microswitches attached to a bumper of sorts. My favorite "sensor" is an old keyboard switch with a springy loop of wire glued onto it as a bumper. This combination is inexpensive and serviceable.

As for the batteries, I recommend nickel-cadmium because of their cell voltage. A fully charged cell is approximately 1.25 V. If you use four of them in series, you have $4 \times 1.25 = 5$ V—just perfect for the OBC.

(If, however, you decide to use disposable batteries with a voltage of approximately 1.5 V per cell, you would have to deal with 6 V. To get this down to a manageable voltage, a diode of .7 V in series with the batteries would lower the voltage to approximately 5.3, within the OBC's range. The placement of this diode is shown in figure 2 and labeled "optional diode.")

The OBC uses up about 200 milliamperes. The motors use a widely varying amount of current depending upon many conditions. I recommend using four "D" cells (4 amperes per hour per cell) for the OBC and three "C" cells (1.8 amperes per hour per cell) for the motors. This combination gives a fair power per weight ratio with approximately 4 to 6 hours of operation per charge.

One last thing about batteries. They can be dangerous. For safety's sake, install the on/off switch in an accessible area. Unfortunately, small batteries, unlike small power supplies, are capable of lots of current for a short period. I have helped many people build their own robot and have seen more than one small wiring accident turn into a full-blown fire. Even though none are shown in the diagram, you might actually consider using a fuse or two in the higher-current areas.

The Motor Control Board

When the OBC wishes to turn a motor on, it makes a pin on the PIA go high. When high, this pin is at approximately +4 V. This signal is used to drive two

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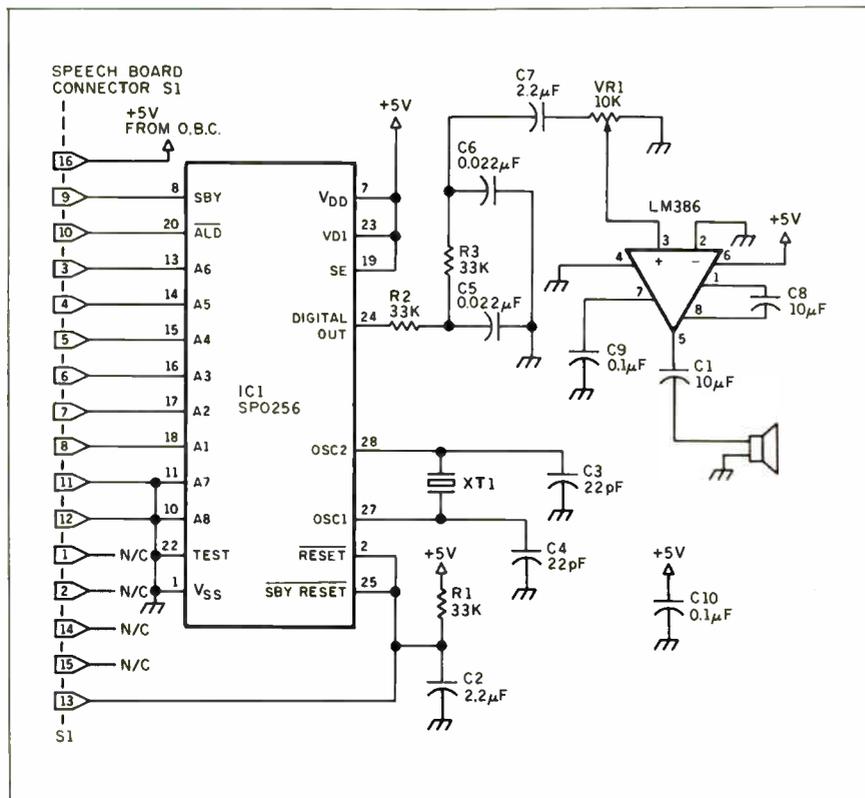


Figure 4: Schematic diagram of BERT's speech board.

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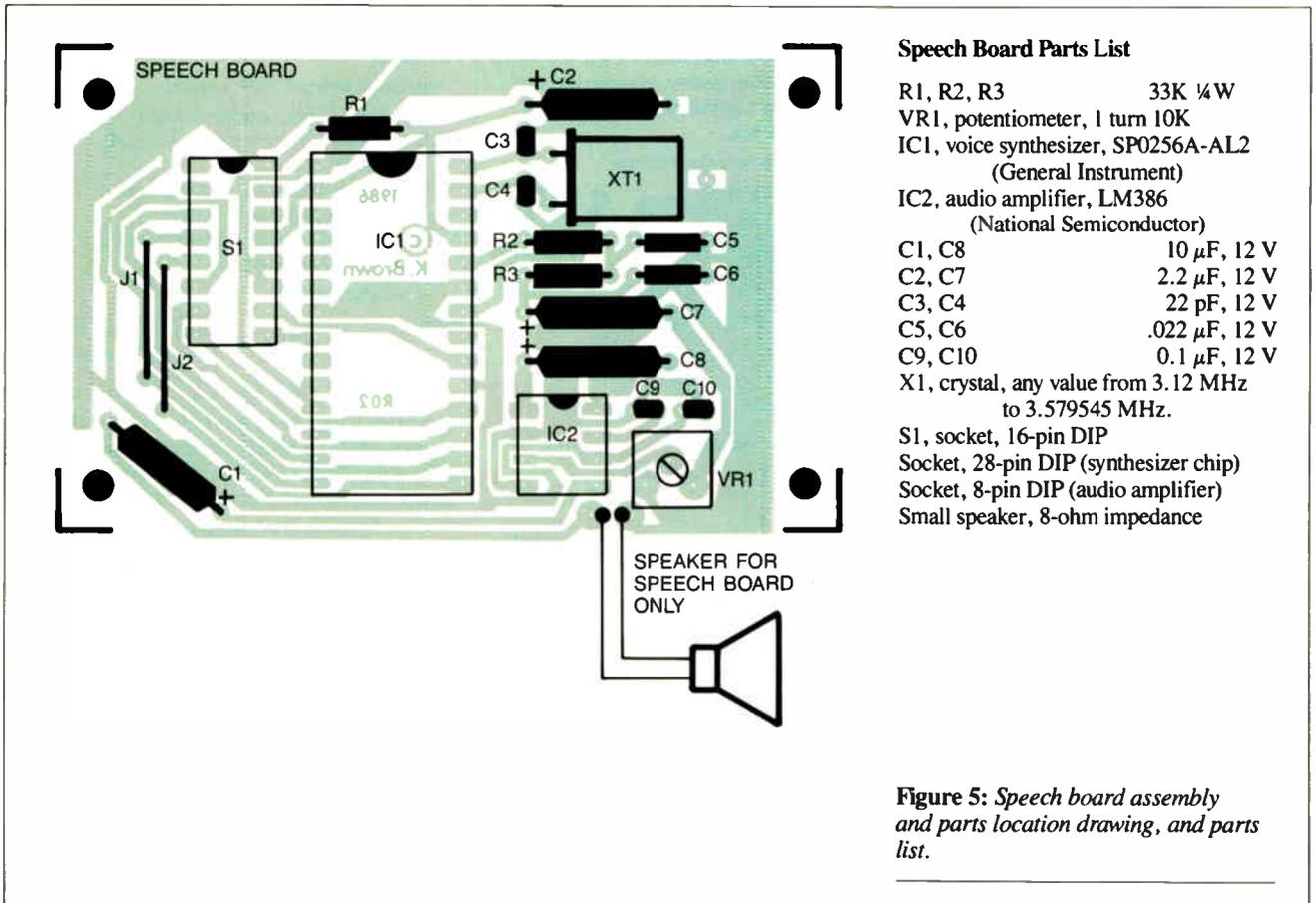
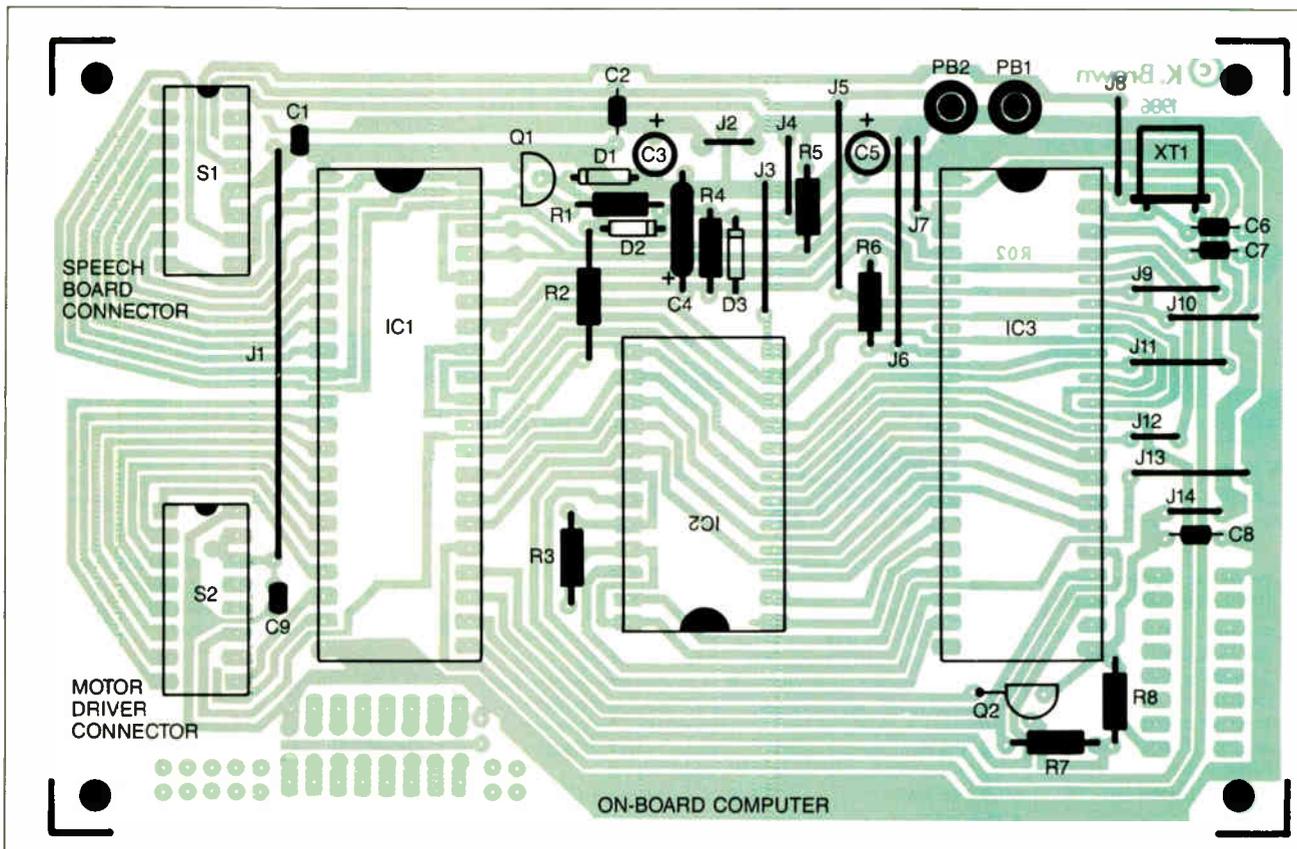
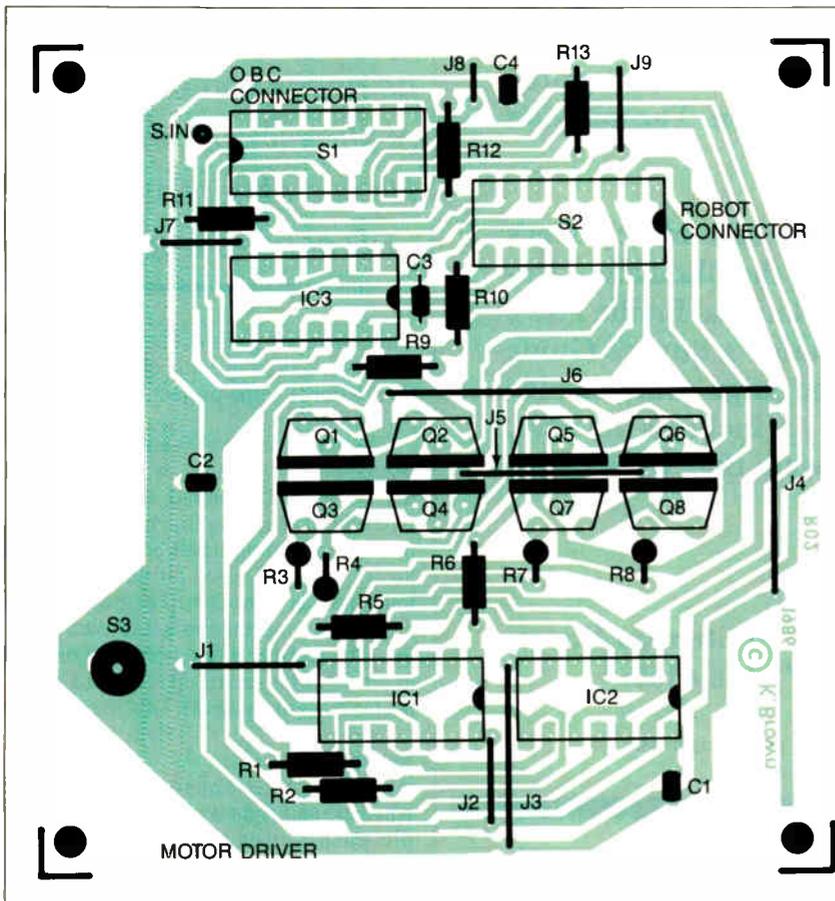


Figure 5: Speech board assembly and parts location drawing, and parts list.





Motor Driver Board Parts List

- R1 through R8, R10 220 ohm ¼W
- R9, R11, R12, R13 10K ¼W
- IC1 74LS04
- IC2 74LS08
- IC3 74LS14
- C1 through C4 0.1 µF, 12 V
- Q1, Q2, Q5, Q6, transistor, TIP31
- Q3, Q4, Q7, Q8, transistor, TIP32
- S1, S2 16-pin DIP socket
- S3 ¼-inch phone jack
- Cable, ribbon 16-pin DIP
- Socket, 14-pin DIP (for IC1, IC2, and IC3)

Figure 7: Motor driver board assembly and parts location drawing, and parts list.

On-board Computer Parts List

- R1, R5, R6 10K ¼W
- R2, R3, R7 1K ¼W
- R4 33K ¼W
- R8 510 ohm ¼W
- IC1 6821 PIA
- IC2 2716 EPROM
- IC3 6802 microprocessor
- C1, C2, C8, C9 0.1 µF, 12 V
- C3, C5 (radial leads) 4.7 µF, 12 V
- C4 (axial leads) 2.2 µF, 12 V
- C6, C7 27 pF, 12 V
- Q1, Q2 transistor, 2N5135
- D1, D2, D3 diode, 1N4148
- XT1 crystal, 4 MHz
- S1, S2 socket, 16-pin DIP
- PB1, PB2 switch, SPST, momentary, push-button
- Socket 40-pin DIP (microprocessor)
- Socket 40-pin DIP (PIA)
- Socket 24-pin DIP (EPROM)

Figure 6: On-board computer assembly and parts location drawing, and parts list.

Circuit Board Assembly Instructions

1. Solder in all capacitors.
2. Solder in all jumpers.
3. Solder in all sockets. The OBC connector socket is installed backward (pin 1 facing backward relative to the other sockets).
4. The ¼-inch phone jack, which is the robot's serial data connector, is connected to ground via its screw collar. Connect its TIP connector to the solder pad labeled "S.IN" near connector S1.
5. Solder in all resistors.
6. Solder in all transistors.

Caution! The metal heat-sink tabs on the transistors are connected to the collector lead. Do not let the transistors touch each other or any other circuit component.

7. Install all integrated circuits, observing precautions to protect chips from static electricity.

pairs of current amplifier transistors. The DC motor may require 50 milliamperes to start turning with no load. If the motor is loaded down, we might be talking about currents of half an amp or so.

Four transistors are used to control each motor. These are arranged in a common "H" or "bridge" configuration. The transistors used in this circuit are rated far in excess of the current loads we will be putting on them. This allows us to simplify the circuit, cut down on weight, and save money by doing away with a heat-sink.

Referring to the motor control board schematic (figure 3), you can see that we are using TTL logic to provide base current for the transistors. This really cuts down on the parts count, which makes the circuit very easy to build and troubleshoot. Admittedly, this design does push the drive capability of the gates a bit. However, hundreds of people have used this circuit and I've yet to hear of a failed gate.

Since BERT is such a small robot, he really needs some method of attracting attention. He can either flash an LED or beep a speaker. While the PIA has enough current capability to do both, it would be unwise to risk using its outputs

continued

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*Since BERT is so small,
he needs some method
of attracting attention.*

*He can either flash an
LED or beep a speaker.*

while there are gates to spare on IC3 (the 74LS14). Utilizing some of these unused gates affords some protection for our expensive PIA.

The base-mounted speaker must have one end tied to ground, with its free end tied to a 10-microfarad capacitor. The free end of the capacitor must be tied to pin 9 of the motor driver board's connector S2. The LED used for the robot's eye must have its cathode tied to ground, with the anode connected to a 220-ohm resistor. The resistor's free end must then go to pin 10 of the motor driver board's connector S2 (see figure 3).

Sensors

BERT's three sensors—nose, left whisker, and right whisker—can be simple push-button switches. When the switch is depressed by striking an object, it should make a pin on the PIA go low. In other words, under normal conditions, the PIA's sensor-connected pins should be high. This is accomplished by tying one end of three 10K resistors (one for each of the sensors) to +5 V, and the other end to its sensor's output. When the switch is closed, it will pull one end of its 10K resistor to ground. These three resistors (R11, R12, and R13) are located on the motor control board.

Next month, in part 2, we'll test each of BERT's circuit boards and base wiring and get down to programming his on-board computer. ■

The following parts are available from Amrobot, 2913 Ohio St., Richmond, CA 94804, (415) 451-6780.

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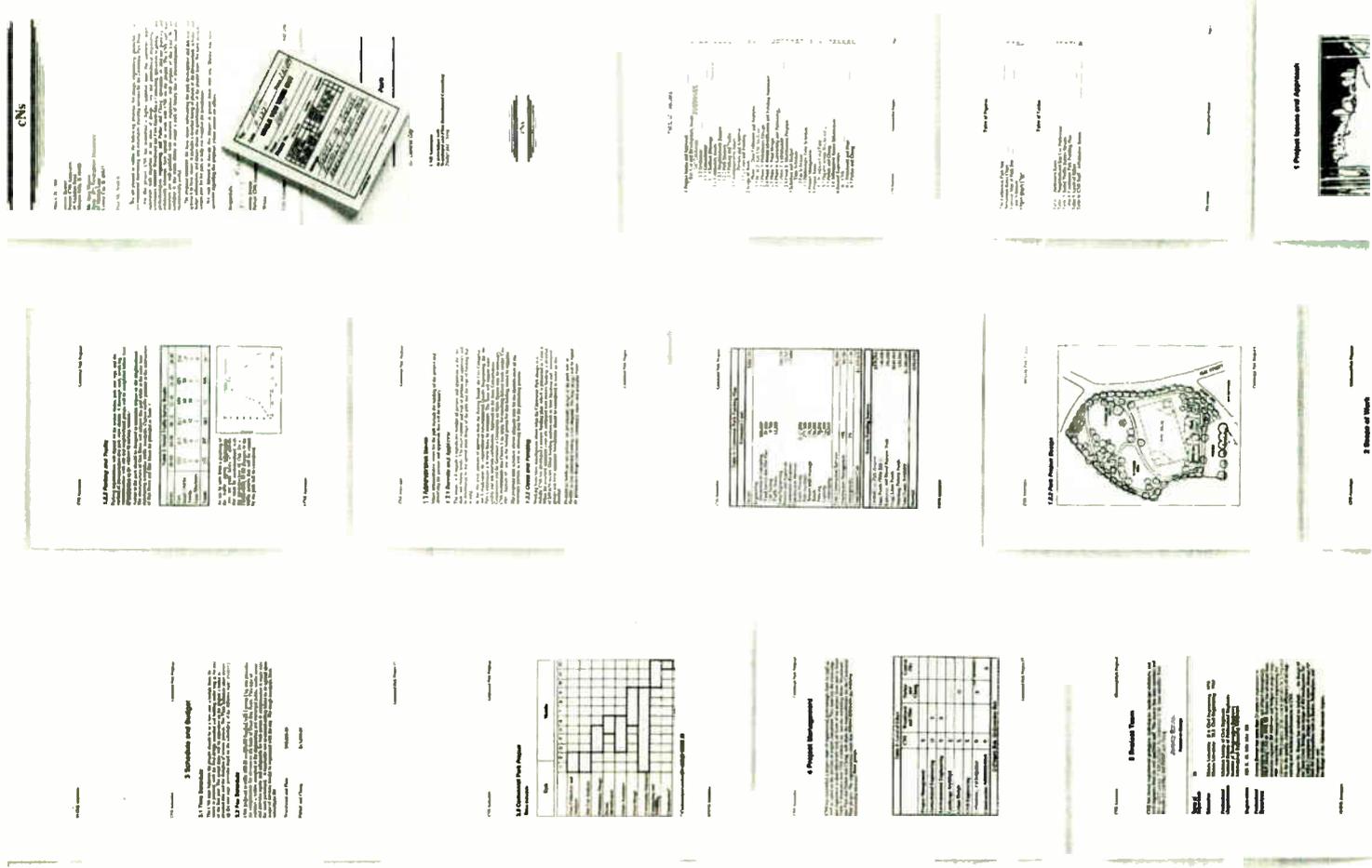
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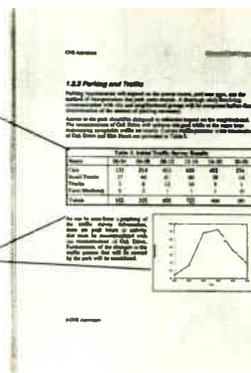
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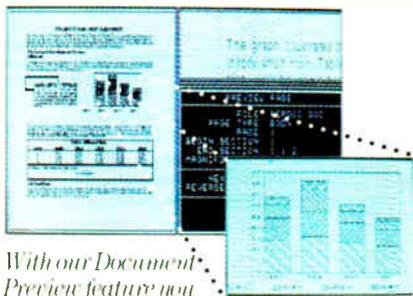
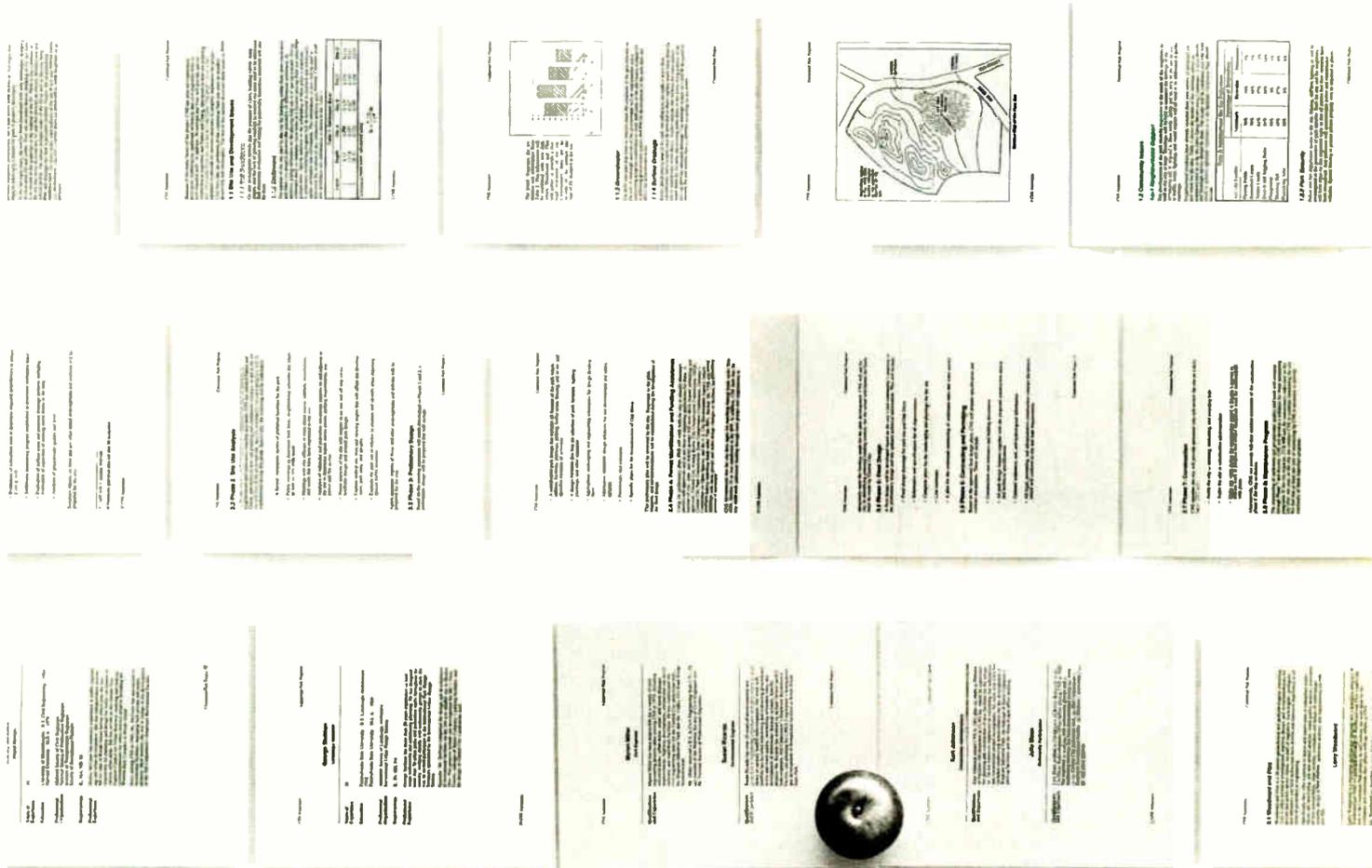
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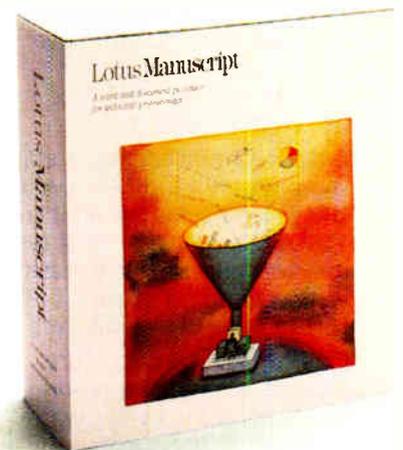
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Mukkai S. Krishnamoorthy and Snorri Agnarsson

Concurrent Programming in Turbo Pascal

Adding these two new data types gives you parallel programming ability



One of the most important programming paradigms is the concept of parallel or concurrent programming. We have implemented concurrent programming features in Turbo Pascal 3.0 (for the IBM PC or compatibles running under PC-/MS-DOS 2.0 or greater), that are similar to the constructs used in Modula-2. The implementation includes the two data types `Process` and `IoProcess`.

Two primitive operations can be performed on the `Process` data type: Create a new `Process` with the function `NewProcess`, and transfer control from one `Process` to another `Process` with the procedure `transfer`.

Two primitive operations can be performed on the `IoProcess` data type: Create a new `IoProcess` with the function `NewIoProcess`, and attach an `IoProcess` to an interrupt with the procedure `IoAttach`.

`Processes` and `IoProcesses` are different and incompatible data types in our implementation. `IoProcesses` are interrupt-driven, but control is transferred between `Processes` in a synchronous fashion, using the `transfer` procedure. The term `IoProcess` is used in a loose sense; it could be any interrupt-driven process, including a clock process. The next two sections discuss the implementation of these constructs. A section with examples follows.

The Process Data Type

The following Turbo Pascal constructs were especially useful to us in implementing our `Process` types (see reference 1). `GetMem` is a routine that allocates a memory area of a given size and returns a pointer to the starting address. The `MemW` array allows access to absolute

memory locations. The `Addr` function gives the address of a memory location (variable). The `Seg` function gives the segment part of the address of a location (variable). The `Ofs` function gives the offset part of the address of a location (variable). The `Ptr` function is used to assign specific values to a pointer variable. Turbo Pascal allows the insertion of machine language code via the inline statement.

Each process has its own separate run-time stack. All the information needed to restart a suspended process is stored in fixed locations on its stack. Therefore, all you need to know about a process is the location of its stack. The `Process` data type can then be implemented as a pointer to the stack location. `Process` is implemented as type `Process = ^integer`.

The `NewProcess` function, shown in listing 1, uses `GetMem` to allocate a memory area for the stack of the new process. The `MemW` array and the `Seg` and `Ofs` functions are then used to modify the new stack. The stack is set up in such a way that if `transfer(p1,p2)` is issued, where `p2` is the new process, then control is passed to the beginning of the procedure whose offset is `prog`. The stack is empty at this point. The assembly language for the procedure transfer is given in listing 2a so you can follow what transfer does. To actually use this procedure from Turbo Pascal, you should enter the machine code for the procedure transfer with an inline statement as shown in listing 2b.

Executing a transfer results in replacing the run-time stack with the stack pointed to by one of transfer's parameters and saving the current stack position in the other parameter variable. As a result, on exit from transfer, control is held by a new process. The old process can be restarted from its point of suspension by issuing

another transfer.

To understand the two routines `NewProcess` and `transfer`, you need to study them together. `NewProcess` sets up the stack with the address of the process routine in the place where transfer expects a return address. The slack that `NewProcess` puts on the stack is to account for transfer's parameters `p1` and `p2`. The function of the routines can be described as follows: The statement `p1:=NewProcess(Ofs(prog),size)` initializes the process `p1` in such a way that a subsequent `transfer(p2,p1)` transfers control to the beginning of the routine `prog`.

The statement `transfer(p1,p2)` should be executed only when `p2` is an initialized `Process`. It has the effect of initializing `p1` to continue executing from the statement following the transfer call. Also, control is transferred to the location specified by `p2`. There are thus two ways of initializing a `Process` `p1`: `transfer(p1,p2)` or `p1:=NewProcess(Ofs(prog),size)`.

The IoProcess Data Type

Similar to the `Process` data type, the `IoProcess` data type is implemented as type `IoProcess = ^integer`. A properly constructed `IoProcess` is the address of an interrupt handler, ready for use as an interrupt vector in the 8088 processor. Associated with the handler is the Turbo

continued

Mukkai S. Krishnamoorthy, an associate professor at Rensselaer Polytechnic Institute, has published several articles in Theoretical and Practical Computer Science. Snorri Agnarsson obtained his Ph.D in computer science working on research relating to modularity in software design. They can be reached at the Department of Computer Science, Rensselaer Polytechnic Institute, Troy, NY 12181.

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Pascal procedure that you want to execute when the interrupt is invoked.

Since the interrupt handler can be invoked at any time and the Turbo Pascal environment may not be active at the time, the interrupt handler must construct the proper environment before executing the Turbo Pascal procedure. The assembly language routine inthandler in listing 3 constructs this environment. For each loProcess, a new copy of the routine is needed, since each copy may need to refer to a different Turbo Pascal procedure. Each copy also contains the proper values

needed to initialize the machine registers to construct a Turbo Pascal environment.

Since all Turbo Pascal procedures are invoked with short calls, you need to initialize the CS register to the proper value before calling the Turbo Pascal procedure. This is done by performing a long call to the procedure shortcaller (listing 4), which resides in the Turbo Pascal code segment. The shortcaller procedure then performs a short call to the desired Turbo Pascal procedure, followed by a long return to inthandler.

continued

Listing 1: The function NewProcess takes as parameters the offset of a parameterless procedure and the size of the stack used, in bytes.

```
{ NAME: newprocess
  EXAMPLE CALL:
    p:=NewProcess(Ofs(prog),1000);
    prog is the parameterless procedure, from which
    the new process is created. The stack of the
    new process p is 1000 bytes.
}
function NewProcess(prog: integer; size: integer): Process;
var stack: ^Integer;
begin
  GetMem(stack,size);
  MemW[Seg(stack^):Ofs(stack^)+size-10]:=prog;
  MemW[Seg(stack^):Ofs(stack^)+size-12]:=Ofs(stack^)+size-12;
  NewProcess:=Ptr(Seg(stack^),Ofs(stack^)+size-12);
end;
```

Listing 2a: The assembly language code for the procedure transfer is given so you can see how transfer works.

```
; procedure transfer(var p1,p2: Process);
;
cseg          segment 'cgroup'
              assume cs:cseg
transfer      proc      near
;
  push      bp          ; Turbo Pascal generated prolog
  mov      bp,sp       ; - - - -
;
  pop      bp          ; Align with 'newprocess' setup
  les     bp,dword ptr [bp]+4 ; get address of p2
  mov     ax,es:[bp]+2   ; get segment part of p2
  mov     bx,es:[bp]    ; get offset part of p2
  mov     bp,sp        ; bp - point to parameter
  les     bp,dword ptr [bp]+8 ; get address of p1
  mov     es:[bp],sp    ; store sp in offset part
  mov     es:[bp]+2,ss  ; store ss in segment part
  mov     ss,ax        ; new stack segment from p2
  mov     sp,bx        ; new stack pointer from p2
  mov     bp,sp        ; re-establish bp for epilog
;
  mov     sp,bp        ; Turbo Pascal generated epilog
  pop     bp           ; - - - -
  ret     8             ; - - - -
;
transfer      endp
cseg          ends
```

Listing 2b: To use the procedure transfer, you need to enter the machine code for transfer with an in-line statement as shown below.

```
procedure transfer(var p1,p2: process);
begin
  inline(
    $5D/ $C4/ $6E/ $04/ $26/ $8B/ $46/ $02/ $26/ $8B/ $5E/ $00/
    $8B/ $EC/ $C4/ $6E/ $08/ $26/ $89/ $66/ $00/ $26/ $8C/ $56/
    $02/ $8E/ $D0/ $8B/ $E3/ $8B/ $EC);
end;
```

Listing 3: Shown here is the assembly language routine for the code that constructs the proper environment for invoking the Turbo Pascal procedure that you have associated with an interrupt. To use this, you must enter the machine code with an in-line statement as shown in listing 5.

```
cseg          segment 'cgroup'
      assume  cs:cseg
inhandler    proc  near
      jmp    start ;jump over data area
getbase:
      call   base ;subroutine to get base of data area.
base:
      pop    di   ;pop address of base into di.
      ret    2    ;return with offset of base in di.
; data area:
newsword     dw    ? ;data segment register for Pascal
stkoffset    dw    ? ;offset of stack
stksegment   dw    ? ;segment of stack for Pascal
procoffset   dw    ? ;offset of interrupt handler
              ;handler segment must be callsegment
calloffset   dw    ? ;offset of short call routine
callsegment  dw    ? ;segment of short call routine
savessword   dw    ? ;word to save ss into
savespword   dw    ? ;word to save sp into
newsd        equ  newsword-base ;offset base to newsword
newsp        equ  stkoffset-base ;offset base to stkoffset
newss        equ  stksegment-base ;offset base to stksegment
handler      equ  procoffset-base ;offset base to procoffset
caller       equ  calloffset-base ;offset base to calloffset
sovess       equ  savessword-base ;offset base to savessword
sovesp       equ  savespword-base ;offset base to savespword
start:
      push   di           ;save di
      call   getbase      ;get base of data area in di
      mov   word ptr cs:[di]+savess,ss ; save ss
      mov   word ptr cs:[di]+savesp,sp ; save sp
      mov   ss,word ptr cs:[di]+newss ; get new ss
      mov   sp,word ptr cs:[di]+newsp ; get new sp
      push  ax           ; save the rest of the registers
      push  bx
      push  cx
      push  dx
      push  bp
      push  si
      push  es
      push  ds
      mov   ds,word ptr cs:[di]+newsd ;get ds for Pascal
      mov   bx,word ptr cs:[di]+handler ;get handler offset
      call  dword ptr cs:[di]+caller ;long call
      pop   ds           ;restore registers and
      pop   es           ;return from interrupt
      pop   si
      pop   bp
```

continued

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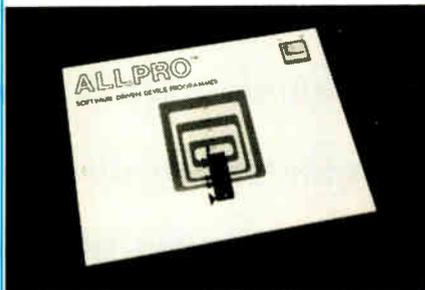
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```

pop      dx
pop      cx
pop      bx
pop      ax
call     getbase
mov      ss,word ptr cs:[di]+savess
mov      sp,word ptr cs:[di]+savesp
pop      di
iret
inhandler  endp
cseg      ends
  
```

Listing 4: This small section of code (only 3 bytes in an in-line statement) is used at the beginning of NewIoProcess to initialize the CS register to the proper value before calling the Turbo Pascal procedure that you have associated with an interrupt.

```

cseg      segment 'cgroup'
          assume  cs:cseg
shortcaller  proc  far
              call  bx
              ret
shortcaller  endp
cseg      ends
  
```

Listing 5: NewIoProcess creates a process that can handle an asynchronous interrupt. It returns a pointer to an area of memory that has been set up as an IoProcess. This pointer can be passed as a parameter to the procedure IoAttach.

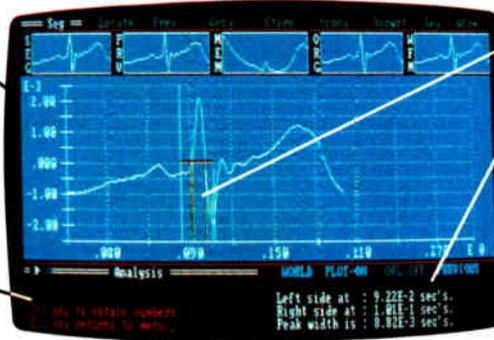
```

{ NAME: newioprocess
  EXAMPLE CALL:
  p:=NewIoProcess(Ofs(prog),1000);
  prog is the parameterless procedure, from which
  the new ioprocess is created. The stack of the
  new ioprocess p is 1000 bytes.
}
function newioprocess(prog: integer; size: integer):
    ioprocess;
procedure shortcaller;
begin
  inline($FF/$D3/$CB);
end;
const inhandler: array[1..85] of byte=
(
  $EB, $16, $90, $E8, $00, $00, $00, $5F, $C3, $00, $00, $00, $00,
  $00, $00, $00, $00, $00, $00, $00, $00, $00, $00, $00, $00,
  $57, $E8, $E7, $FF, $2E, $8C, $55, $0E, $2E, $89, $65, $10,
  $2E, $8E, $55, $06, $2E, $8B, $65, $04, $50, $53, $51, $52,
  $55, $56, $06, $1E, $2E, $8E, $5D, $02, $2E, $8B, $5D, $08,
  $2E, $FF, $5D, $0A, $1F, $07, $5E, $5D, $5A, $59, $5B, $58,
  $E8, $8B, $FF, $2E, $8E, $55, $0E, $2E, $8B, $65, $10, $5F,
  $CF);
var area: ^integer;
begin
  GetMem(area,size+85);
  Move(inhandler,area^,85);
  memw[Seg(area^):Ofs(area^)+ 8]:=Dseg;
  memw[Seg(area^):Ofs(area^)+10]:=Ofs(area^)+size+85;
  memw[Seg(area^):Ofs(area^)+12]:=Seg(area^);
  memw[Seg(area^):Ofs(area^)+14]:=prog;
  memw[Seg(area^):Ofs(area^)+16]:=Ofs(shortcaller)+12;
  memw[Seg(area^):Ofs(area^)+18]:=Cseg;
  newioprocess:=area;
end;
  
```

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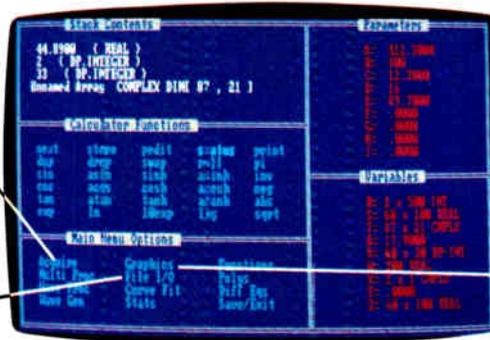


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Listing 6: IoAttach attaches an asynchronous process to an interrupt. Each time the interrupt is invoked, the procedure associated with the IoProcess is called.

```
{ NAME: IoAttach
PARAMETERS:
  'intnum' is an interrupt number
  'proc' is an ioprocess created by newioprocess
}
procedure IoAttach(intnum: byte; proc: ioprocess);
var regs: record
    ax,bx,cx,dx,bp,si,di,ds,es,flags: integer
end;
begin
with regs do
begin
ax:=$2500 + intnum; { DOS function 25H sets an }
ds:=Seg(proc^);    { interrupt vector.      }
dx:=Ofs(proc^);
end;
MsDos(regs);      { request DOS function }
end;
```

Listing 7a: Shown below is a simple example of how to use the Process data type. Note that control is passed synchronously between prog1 and prog2 with the procedure transfer.

```
{ $K- } { turn off checking for stack overflow }
program multitest;
type Process=^integer;
... { definitions of NewProcess & transfer }
var p1,p2: process;
procedure prog1;
begin
while true do
begin
writeln('Hi');
transfer(p1,p2);
writeln('He');
transfer(p1,p2);
end;
end;
procedure prog2;
begin
while true do
begin
writeln('Ho');
transfer(p2,p1);
end;
end;
var p0: process;
procedure main;
begin
p1:=newprocess(ofs(prog1),1000);
p2:=newprocess(ofs(prog2),1000);
transfer(p0,p1);
end;
begin main end.
```

The Turbo Pascal function `NewIoProcess` (see listing 5) constructs an `IoProcess`, given the offset of a parameterless Turbo Pascal procedure, and the desired stack size of resulting `IoProcess`. The new `IoProcess` is constructed by allocating a memory area, part of which serves as the stack of the `IoProcess` and part of which contains the inhandler routine, which constructs the Turbo Pascal environment and calls the desired Turbo Pascal procedure.

With the `NewIoProcess` function, we can construct interrupt handlers. To use a handler, we need to be able to attach it to an interrupt—in other words, to store its address in the appropriate interrupt vector. This function is performed by the

procedure `IoAttach`, shown in listing 5. `IoAttach` takes two arguments: an interrupt number and an `IoProcess`. It has the effect of storing the address of the interrupt handler in the vector associated with the specified interrupt. It uses a call to the operating system to perform this.

Examples

Listing 7a shows a simple program illustrating the use of the `Process` data type. Two processes, `p1` and `p2`, are created. Both processes loop indefinitely, printing on the screen. The processes transfer control between each other in an alternate fashion. As a result, their output is interspersed, as shown in listing 7b.

Listing 8a shows a program using an `IoProcess` to count timer interrupts. The procedure `incrementer`, which is executed for each interrupt, simply increments a global variable count for each timer interrupt. The main program then prints out the increasing value of count in an infinite loop, as shown in listing 8b.

Conclusion

The constructs described in this article are similar to the ones used in `Modula-2`, as described by Niklaus Wirth (see reference 2). The main difference is that in this case, the types `IoProcess` and `Process` are incompatible, and the procedures associated with the `IoProcesses` are fully executed at each interrupt, while the ones in `Modula-2` can suspend execution and resume

New IoProcess constructs an IoProcess; IoAttach stores the address of the IoProcess in an interrupt handler.

again at the next interrupt.

Wirth describes how to construct higher-level process control constructs, using round-robin scheduling, signaling of events, and so forth. Similar features can be constructed easily for our Turbo Pascal processes. Interrupt processing by use of the `IoProcess` data type turned out to be fast enough to handle interrupt-driven communication at 9600 bits per second. ■
Editor's note: *Snorri Agnarsson has written an interrupt-driven asynchronous communications program for the IBM PC using the process implementation described here. The source code for this communications program is written in Turbo Pascal and can be downloaded from BYTenet Listings. See page 4.*

REFERENCES

1. *Turbo Pascal Reference Manual*. Borland International Inc.
2. Wirth, Niklaus. *Programming in Modula-2*. New York: Springer-Verlag, 1983.

Listing 7b: The output of the program in listing 7a.

Resulting output:

```
Hi
Ho
He
Ho
Hi
Ho
.
.
.
```

Listing 8a: A simple example of how to use the data type `IoProcess`. A routine to increment the variable count is attached to the timer tick interrupt.

```
{ $K- } { turn of checking for stack overflow }

program interrupttest;

type IoProcess = ^integer;

var count: integer;
var timerhandler: IoProcess;

... { definitions of NewIoProcess and IoAttach }

procedure incrementer;
begin
  count:=succ(count);
end;

begin
  timerhandler:=NewIoProcess(Ofs(incrementer),1000);
  count:=0;
  IoAttach($1C,timerhandler); { attach timerhandler to user }
  while true do { timer interrupt ( 1Ch ) }
  begin
    writeln(count);
    Delay(100); { delay 100 milliseconds }
  end;
end.
```

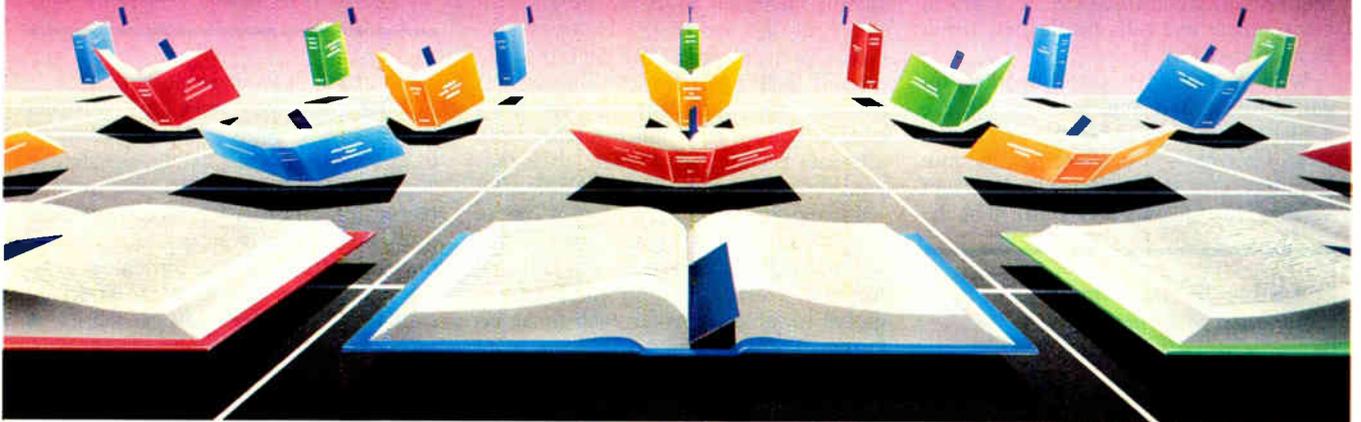
Listing 8b: Shown is the output of listing 8a. The variable count is written out after a delay of approximately 100 milliseconds.

Resulting output:

```
0
1
3
5
7
8
10
12
.
.
.
```

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The Adapter/386 does not provide all the speed of a turbo card or a "real" 386 machine. In fact, the translator card slows down the AT by about 10 percent for existing code. But it is also priced at only one-third the cost of a drop-in 386-based turbo card, and less than one-tenth the cost of a separate desktop 386 machine. For software developers and AT owners who want to experiment with 386 software, the Adapter/386 is an inexpensive alternative to buying a stand-alone 386-based PC or a full-blown 386 turbo board.

To install the Adapter/386, you remove the AT's 80286 processor chip from its socket in the motherboard and insert the Adapter/386 in its place. The Adapter/386's components mount on the underside of the board so that it fits under the PC AT's disk drives (see photo 1). If a math coprocessor is present in the AT, it must be removed and installed in the Cheetah math coprocessor adapter board (supplied with the Adapter/386). The

Adapter board, in turn, must be plugged back into the coprocessor's socket.

A 32-bit Interface to a 16-bit Bus

The 80386 is a 32-bit microprocessor with a 32-bit external data bus. This creates a problem because the 80286 has only a 16-bit data bus. However, there is a solution. When the BS16 (bus size 16) pin of the 80386 is tied to ground, the 16-bit mode of operation is activated, and the

80386 configures itself for double 16-bit word fetches. In this mode, the processor provides the extra bus cycle required for the extra word fetch; the Adapter/386 is designed to run in this mode.

The 80386 is designed to use 32-bit physical addresses. In the Adapter/386 the high-order 8 address bits are ignored to provide the 24-bit addresses (16 megabytes of memory) used by the 80286. In

continued

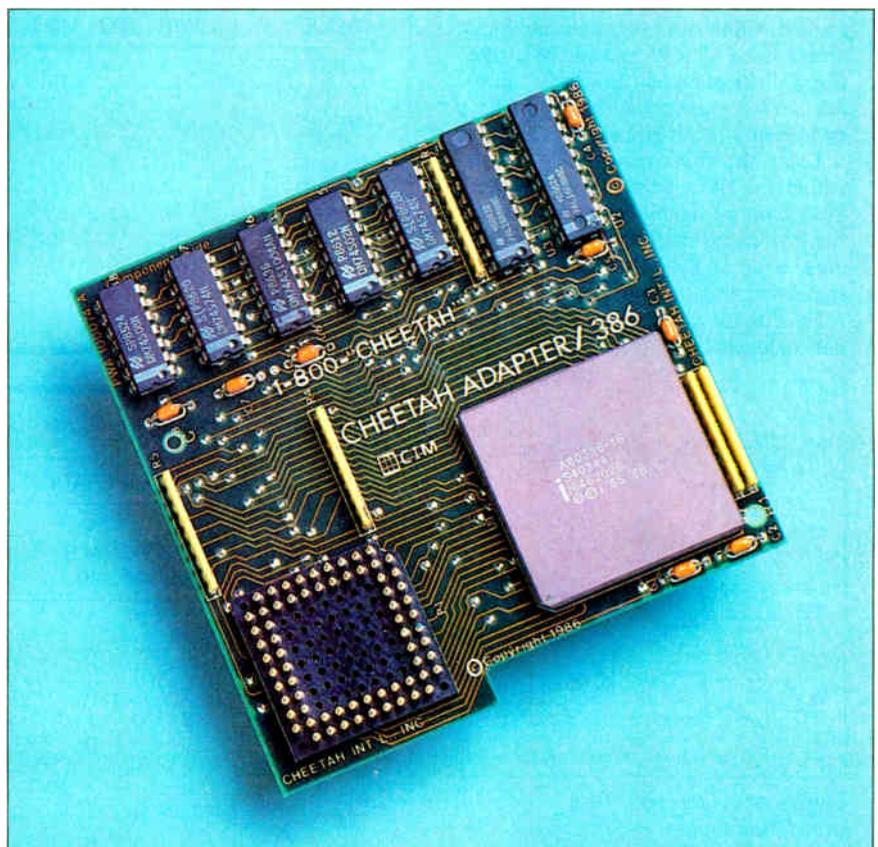


Photo 1: The Cheetah Adapter/386 board with pin grid array plug (lower left).

Jon Shiell, a BYTE contributing editor, is a system architect and microprogrammer. He can be contacted on BIX as jshiell, or c/o BYTE, One Phoenix Mill Lane, Peterborough, NH 03458.

the case of some status signals, the Adapter/386 provides the emulation of the required 80286 signals based on their 80386 functional equivalents. (See the text box below.)

Due to delays in the initiation of memory and I/O cycles of the emulated 80286 signals, circuitry on the Adapter/386 board momentarily negates the READY signal to the 80386 at the beginning of each bus operation to allow the 80286 system to catch up. After this short period, required to permit the 80386 to synchronize with the 80286 system's READY signal, the 80386 continues as if it were an 80286.

The negating of the READY signal constitutes a wait state, which is added to every data-transfer cycle. This allows the 80386 to properly respond to devices of various speeds within the 80286 system. Unfortunately, what was a zero-wait-state (0WS) access becomes a one-wait-state (1WS) access, for a 20 percent processor slowdown. In turn, 1WS access becomes a 2WS access, for a 15 percent slowdown.

The additional wait state that the 80386 incurs does not provide more access time for the memory system; rather, it allows the logic on the adapter to properly initiate the access for the system. The overall

system slowdown will normally be less than the slowdown at the CPU, so the user of a 1WS AT would see, perhaps, a 10 percent slowdown instead of the expected 15 percent. In addition, the use of 32-bit operations and the virtual machine function of the chip will also increase the effective speed.

The best fix for this slowdown is to replace the AT's clock crystal with a faster one. For example, replace the 12-megahertz crystal in a 6-MHz AT with, say, a 14.3-MHz crystal. (See "Speeding Up the PC AT" by Brian K. Roemmele in BYTE's Fall 1986 special issue *Inside the IBM PCs*.)

Converting Unique 80386 Signals to 80286 Signals

Bus cycles on an 80286 system are identified by the state of four signals during a bus status cycle. These four signals are S0, S1, COD/INTA, and M/IO. The Adapter/386 emulates the generation of these signals by using four of its own signals: W/R, D/C, M/IO, and ADS. The conversion between 80386 bus status cycles and 80286 bus status cycles is performed within two programmable logic arrays: one PAL16R8 and one PAL16R6 (for a description of PALs, see "Introduction to Programmable Array Logic" by Vincent J. Coli, January BYTE).

Using the clock-registered elements within the PALs permits the emulated 80286 control signals to be asserted and removed at the clock edges corresponding to an actual 80286. Table A maps the signals between the two systems:

In addition to the status/control signals, address lines A0 and A1 must be

generated by the Cheetah Adapter/386, since they are not produced directly by the 80386. Rather, the 80386 produces four byte-enable signals: BE0, BE1,

BE2, and BE3. The relationship between the byte-enable signals (BEn) and the two address lines (A0 and A1) is defined in table B and figure A below. ■

Table A: 80386 to 80286 signal map.

BUS CYCLE	80386 SIGNALS				80286 SIGNALS			
	W/R	D/C	M/IO	ADS	S1	S0	COD/INTA	M/IO
INTERRUPT								
ACKNOWLEDG	0	0	0	0	0	0	0	0
MEMORY DATA READ	0	1	1	0	0	1	0	1
MEMORY DATA WRITE	1	1	1	0	1	0	0	1
I/O READ	0	1	0	0	0	1	1	0
I/O WRITE	1	1	0	0	1	0	1	0
MEMORY INSTR READ	0	0	1	0	0	1	1	1
HALT/SHTDWN	1	0	1	0	0	0	0	1

Table B: Byte-enable-to-address-signal conversion.

2ND CYCLE REQ'D	16-BIT BUS OPERATION			32-BIT BUS SINGLE CYCLE				XFER SIZE
	80286 SIGNALS BHE	A1	A0	80386 SIGNALS BE3	BE2	BE1	BE0	
No	1	0	0	1	1	1	0	1 byte
No	0	0	1	1	1	0	1	1 byte
No	0	0	0	1	1	0	0	2 bytes
No	1	1	0	1	0	1	1	1 byte
Yes	0	0	1	1	0	0	1	2 bytes
Yes	0	0	0	1	0	0	0	3 bytes
No	0	1	1	0	1	1	1	1 byte
No	0	1	0	0	0	1	1	2 bytes
Yes	0	0	1	0	0	0	1	3 bytes
Yes	0	0	0	0	0	0	0	4 bytes

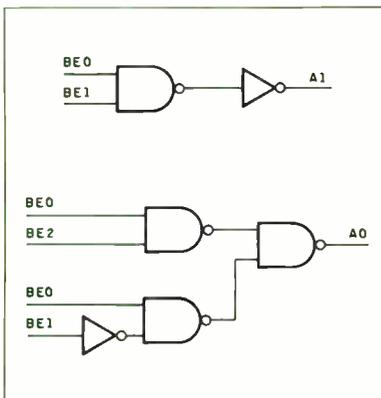


Figure A: Address bits 0, 1 translation logic.

Compatibility

The limitations of the 16-bit data bus/24-bit address bus used on the Adapter/386 do not affect the functionality of the 80386 processor, other than to require two memory accesses per double word (instead of one) and to restrict the amount of overall available memory. (Note that the current generation of "real" 386 machines keep the 24-bit address limit.) The 80386 is still capable of using virtual memory and operating in all of its available modes, including protected mode.

Mathematics coprocessor compatibility is handled by an adapter board included with the Cheetah Adapter/386. This small board is necessary because the signals CMD0 and CMD1, inputs of the 80287 coprocessor, must be connected differently when a 386 processor is present. A PC AT connects the latched version of the 286 address bit 1 to the coprocessor's CMD0 input and address bit 2 to the coprocessor's CMD1 input. Use of an 80287 with an 80386 requires that address bit 2 be connected to CMD0 and a ground level be connected to CMD1.

IBM's PC AT math coprocessor diagnostics will not run with the Adapter/386. But this does not mean that the two processors are incompatible. The IBM diagnostics were written early in the PC AT design phase and use math coprocessor instructions that have been subsequently disallowed by Intel. One test of coprocessor compatibility used by Cheetah is AutoCAD, which, according to the company, performs flawlessly.

Speed is the only disadvantage of the Adapter/386. Because it does not use caching and is data-bus-limited, the overall system throughput suffers somewhat compared to a "pure" 80386 implementation. In addition, the extra wait state required to synchronize the 80386 to the 80286 system lengthens each bus cycle.

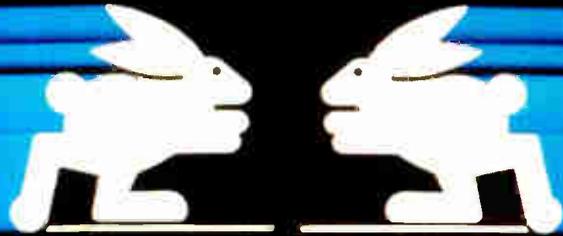
Product Support

With the Adapter/386, you get the math coprocessor adapter, a copy of the Intel 80386 Programmer's Reference Manual, a \$25 rebate for a BIX membership (or additional connect time if you are already a member), a list of the 80386 software that Cheetah International knows works with its adapter, coupons for discounts on various 80386 software products, and, of course, installation instructions.

The BIX time is included in the package because Cheetah intends to support the product interactively through a BIX vendor support conference.

For more information contact Cheetah International Inc., 107 Community Blvd., Suite 5, Longview, TX 75606, 800-CHEETAH; (214) 757-3001 in Texas. Indicate your type of AT. ■

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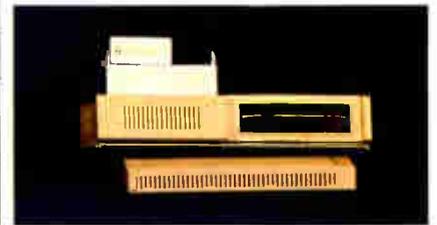
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Instruction Set Strategies

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For additional information on instruction set design, join BIX's on-line supplement to this issue in the conference apr87.sup. In the conference topic acorn.risc, James J. Farrell III and John F. Stockton explore the design characteristics of the Acorn RISC processor, a chip created especially for microcontroller applications. (For information on joining BIX, see page 340.)



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Introduction

Instruction Set Strategies

“TO MICROCODE OR NOT TO MICROCODE” merely begins the list of design questions that engineers ponder when they create new microprocessors. From there, engineers delve into the complexities of instruction pipelining, the frustrating von Neumann bottleneck, and the intricacies of efficient compiler construction. These myriad choices focus on the instruction set strategy envisioned for a new chip.

To date, two prominent approaches to designing CPUs and their instruction sets have emerged—reduced instruction set computer (RISC) and complex instruction set computer (CISC) designs. The primary difference between these strategies is whether to use a small number of fast-executing instructions or to use more complicated instructions that make writing programs easier. But there are other strategies as well, including one that author Phil Koopman Jr. calls a writable instruction set computer (WISC). The articles on the following pages throw some light into the dark corners of microprocessor design to help you understand the role of the instruction set.

As we put together this group of articles, a common thread began to emerge—RISC and CISC designs are beginning to converge. Many of the best design ideas from each approach are being combined to create hybrid CPUs that have both RISC and CISC components. Both the Fairchild Clipper CPU chip set and the Motorola 68030, for example, exhibit this convergence of methodologies.

To set the stage for this exploration of instruction set strategies, Phillip Robinson surveys the RISC landscape to establish where the tenets of this design approach have brought us to date. Next, Thomas L. Johnson of Motorola explains how the new MC68030 microprocessor incorporates many RISC-like features in what at first seems to be a classic CISC machine. Mike Ackerman and Gary Baum’s article on the Fairchild Clipper goes a step further in demonstrating the convergence of RISC and CISC in that processor.

RISC designs with their abbreviated instruction sets place a substantial burden on compilers. The new Novix NC4016 CPU uses FORTH as its instruction set, and Dan Miller shows how this stack-oriented RISC machine and FORTH contribute to the creation of an efficient C compiler.

To close out our tour of instruction set strategies, Phil Koopman discusses the advantages of a writable instruction store on a stack-based microprocessor.

For additional information on instruction set design, see the BIX conference apr87.sup, topic acorn.risc, for an article on the Acorn RISC processor. James J. Farrell III and John F. Stockton explore the design characteristics of this chip.

All this RISC-versus-CISC debate may ultimately prove only one thing: that one person’s acronym is another person’s anachronism.

—G. Michael Vose, Senior Technical Editor

How Much of a RISC?

*The past, present, and future
of reduced instruction set computers*

Phillip Robinson

JUST A FEW YEARS AGO, the idea of a new computer architecture based on simplified, streamlined central processors was mainly an academic curiosity. Invented at IBM and shaped at Berkeley and Stanford, the RISC principle embodied a heresy: that most commercial microprocessor architecture had bloated far beyond the optimum level.

Later, the heresy became a debate. In fact, a panel discussion entitled "The Great RISC versus CISC Debate" at the 1986 COMPCON show in San Francisco turned into the conference's centerpiece. Laboratory experiments have proved that lean chips with reduced instruction sets can run benchmark tests at fantastic speeds, but some system designers remain unconvinced that RISC will be as useful in the real world of complex systems and applications.

To learn the state of RISC, I talked to some of its original proponents and surveyed the state of commercial RISC machines. My conclusion is that RISC principles have greatly influenced computer design, even when they aren't adhered to directly. Furthermore, enough RISC machines, ranging from the microcomputer level to the superminicomputer level, are now on the market that the commercial potential of RISC will soon be evident, instead of just the subject of conference debate.

But don't expect RISC to change the world right away. As one of the early RISC researchers, Professor John Hennessy of Stanford, puts it, "Market directions always move more slowly than [the introduction of] technical products."

Several marketing departments have leapt on the RISC bandwagon with statements that claim a processor takes advantage of both RISC and complex instruction set computer ideas. And if you read the comments in the BIX conferences "cpus/risc" and "rwars/computers," you'll find a lot of argument over what is RISC and what isn't. For example, some people refer to the Novix chip (see the article entitled "Stack Machines and Compiler Design," by Daniel L. Miller on page 177) as RISC, and others do not. In the end, most people agree that RISC isn't just a smaller instruction set. It is a simplified microprocessor that jettisons all baggage that slows the raw processing speed.

Tracing Its Roots

Both RISC and its predecessor, CISC, are commonly credited to IBM. The first CISC machine was probably the IBM 360 mainframe, which was created in 1964. The 360 made extensive use of microprogramming, building instructions out of series of microinstructions that were in turn stored in ROM within the CPU. Decoding an instruction into a sequence of microinstructions requires several look-up operations and, therefore, multiple clock cycles.

Engineers understood the additional clock cycles to be a natural consequence of putting more hardware functions into software. They tried to beat the rapidly growing expense of software by implementing more and more software functions in hardware.

RISC began in 1975 at IBM. John

Cocke, an IBM Fellow, was working with a team to make a very large telephone switching system. Such a large system needed a fast controller. The team experimented along many lines, including slashing the instruction set. Later, after abandoning the switching system project, the team considered using the controller itself as a computer. The outgrowth of their efforts was the 801 minicomputer built in 1979. (The team named it after the number of the IBM building in which it was made.)

According to Cocke, reducing the number of instructions was more a result than a cause. His team had trace statistics listings of how often each instruction was used that convinced it not to add complicated instructions to a machine when those same instructions could be built up from simpler ones without hurting performance.

The team designed the 801 with very fast memory and fixed format instructions that could execute in a single clock cycle. That allowed a lot of pipelining and overlapping of instruction execution.

Although the 801 never became a commercial product, the IBM RT PC workstation announced early in 1986 took up the RISC baton: It is a direct offshoot of the 801. Another IBM Fellow, G. Glenn Henry, who had previously worked on the System/38, was a guiding force be-

continued

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hind the RT. The RT's foundation is a microprocessor called the research/office products division microprocessor and a companion memory management chip. The ROMP works with standard memory, 150-nanosecond 256K-byte DRAMs. It has a very fast memory bus and can transfer one word of data and one address every machine cycle (170 ns). The bus has 32 lines that function as address lines during half of the cycle and as data during the other half. Figure 1 shows the RT's processor-board block diagram.

The ROMP has 118 instructions, less than half the number of the DEC VAX-11/780, the computer most often used today as a standard for speed and an example of CISC architecture. That, however, is nearly three times as many instructions found in other RISC designs. That midpoint status, along with the fact that instead of a single instruction format the ROMP has seven different formats, leads some RISC proponents to say that the RT isn't a true RISC machine. Still, it has many of the elements of a RISC machine, and until other RISC micros appear, the RT's commercial success or failure might represent the success or failure of the RISC concept to the buying public.

RISC Defined

RISC is more than just a small instruction set. David Patterson, a professor at the University of California at Berkeley whose group first coined the term, says that the definition of RISC is a matter of constant debate in the computer architecture community. However, there are a

few points that are commonly accepted.

First, a RISC machine must execute one instruction each clock cycle. Traces of computer programs consistently show that the most heavily used instructions are the primitives. With proper design, engineers can write these to run in a single clock cycle. That simplifies pipelining, interrupts, and a host of other microprocessor design attributes. Sticking to primitives, however, requires compilers to use more software subroutines for complex procedures.

A major argument against RISC has been that the processors will need to use so many more of the simple instructions in the place of powerful, complex instructions that the increase in path length (number of instructions to get the job done) will negate the advantage of running each instruction faster. According to Professor Hennessy of the Stanford MIPS (microprocessor without interlocked pipe stages) project, RISC machines pay around a 30 percent penalty in added instructions over microcoded machines. However, he says, "We are willing to take a 30 percent hit in return for a fivefold improvement in cycles per instruction."

Second, a RISC machine must use a fixed format for the instructions. Doing so makes decoding simple. Assigning each field to a particular function allows hardwiring of the instructions, and avoiding microcode adds more speed. Only 6 percent to 10 percent of the chip area of the Berkeley RISC I and II chips was devoted to control functions, while 50 percent to 60 percent of the total chip area in a 68000 or Z8000 is the control section.

Third, RISC machines stick to a load/store architecture. That means the only instructions that deal with memory are simple load or store instructions. All other manipulations take place inside the microprocessor registers. This arrangement simplifies addressing and makes it easier to restart instructions for exception conditions. It also requires a large number of on-chip registers, a common feature of RISC chips and one that some detractors claim is the main reason for improved performance.

Finally, RISC machines require more compile-time effort than CISC machines. Because of RISC's relatively few instructions and addressing modes, more effort should go into compilers that can order the primitive instructions in the most efficient manner, tailoring the instruction sequences to the exact requirements of the high-level language chosen.

The Berkeley Camp

A team including Dr. David Patterson developed the RISC I and II chips (see "RISC Chips," November 1984 BYTE). While these chips were based on the previous IBM work, they also established some standards for RISC. After the successful design and fabrication of simple 32-bit microprocessors that ran from 2 to 10 million instructions per second peak, the Berkeley team tackled a project called SOAR (Smalltalk on a RISC). This project resulted in another RISC chip that was dedicated to running Smalltalk, and it proved, according to Patterson, "that you don't really need anything beyond a RISC machine to run Smalltalk."

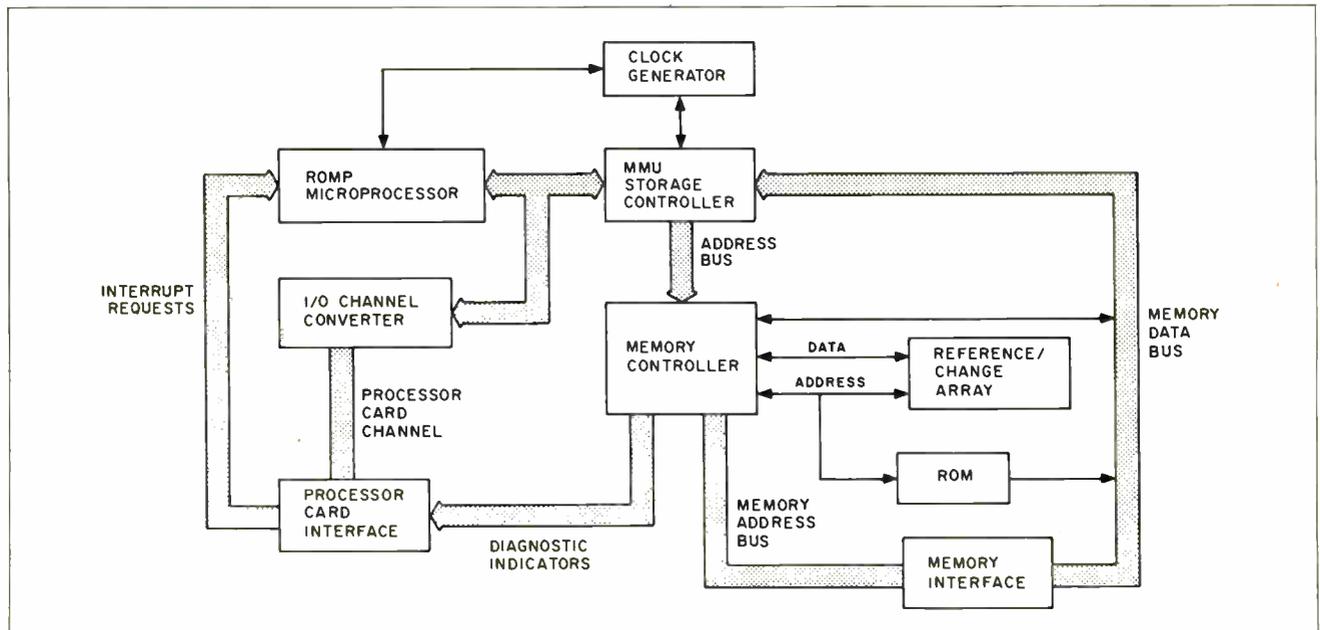


Figure 1: The IBM RT PC processor-board block diagram.

The University of California at Berkeley team turned further to symbolic processing with the SPUR (symbolic processing using RISCs) project. Its goal was to design a multiprocessor workstation for conducting parallel-processing research. The research focused on using LISP. The SPUR project is complex, including workstation development and research efforts in integrated circuits, computer architecture, operating systems, and programming languages. The SPUR system is built around 6 to 12 high-performance, CMOS, homogeneous RISC processors. The team chose the number of processors to permit parallel-processing experiments within a package small enough to be a personal workstation.

The SPUR processor supports Common LISP and IEEE floating-point processing. It uses three custom 2-micron CMOS chips: a cache controller, CPU, and floating-point coprocessor unit. Figure 2 shows the arrangement of these on a processor board. The CPU is based on the Berkeley RISC architecture and uses a simple, uniform pipeline with hard-wired instructions and a large register file. It tries to stick to an instruction per clock cycle. SPUR goes beyond RISC II in that it adds a 512-byte instruction buffer, a fourth execution pipeline stage, a coprocessor interface, and support for LISP tagged data. Figure 4 compares the SPUR and RISC II pipelines.

AMD Building Blocks

Another processor based on the Berkeley RISC design is one that Advanced Micro Devices cooked up from two families of its VLSI chips: the bipolar Am29300 and the CMOS Am39300. AMD can use the chips in these families to make 32-bit, fixed-word-length RISC chip sets. The 29300 can support cycle times of 80 ns. The pipeline in the AMD RISC chips is a two-level instruction-fetch-and-execute scheme. Both chips have a 4-gigabyte addressing capability for virtual memory structures.

The Am29334 four-port, dual-access register file; the Am29332 ALU (which includes a barrel shifter and a 64-bit-in, 32-bit-out funnel shifter); and the Am29337 bounds checker are the basis of the AMD design. Several 29334 register file chips can be teamed to make larger register blocks. AMD has published a RISC processor design based on these components that closely resembles the Berkeley RISC I chip. Figure 3 shows a block diagram of that processor.

AMD uses the 29334 register file chip in the AMD RISC design to duplicate the overlapping register windows of the Berkeley RISC design (see "RISC Chips" by John Markoff, November

1984 BYTE). The overlapping improves context-switching speed. The Berkeley research showed that one of the largest shares of CPU time was spent changing processor status for moves between different program procedures or routines. With the register windows, the chip does not have to copy all register values to

memory when going to a routine and then read them back when returning from a routine. Instead, each procedure is assigned one register window, and the program can change procedures just by switching the active register window within the register file in the CPU.

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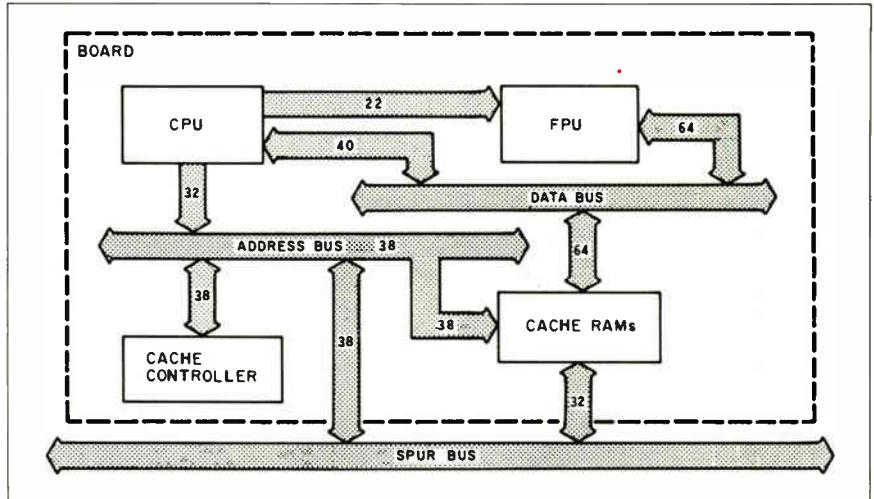


Figure 2: The SPUR processor-board block diagram.

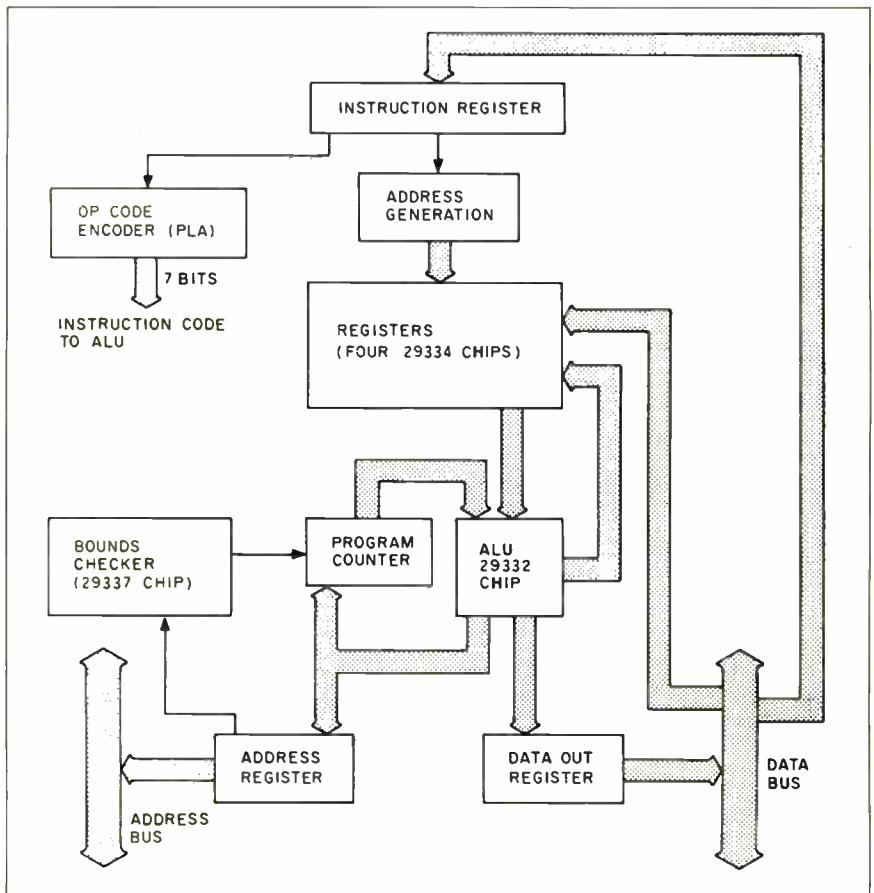


Figure 3: The AMD RISC-system block diagram.

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Four 29334 chips can form the basis of a register block with seven register windows and 10 global registers. Each window has 32 registers split into 10 global registers, 10 local registers, 6 incoming-parameter registers, and 6 outgoing-parameter registers. The Berkeley RISC design had 138 registers in eight windows. The global registers are available to all procedures.

Each one of the 33 instructions is 32 bits long with a fixed format. The op code occupies a 7-bit field. The design has 23 more bits organized into three fields that specify the two source operands and the one destination. All instructions are decoded by running the 7-bit op code through an on-chip programmable-logic-array section containing the control logic.

While the chip executes one instruction, it fetches the succeeding instruction from memory. To handle conditional branch instructions, AMD uses a delayed branch. The compiler used with the processor contains a code reorganizer that rearranges the sequence of instructions so that the one following the branch instruction is always executed no matter what the branch condition. AMD claims that in nine out of ten cases the succeeding operation can be useful. In the tenth case, it is a time-wasting NOP instruction.

The Stanford Camp

Professor John Hennessy of Stanford University was one of the other early academic stalwarts of RISC. He helped put together the Stanford MIPS chip project. After MIPS succeeded in making a fast simple chip, the Stanford group turned to symbolic processing, much as the Berkeley group did. But their paths diverged. While Patterson's team customized its chip to symbolic-processing languages such as Smalltalk and LISP, the Stanford team, according to Hennessy, went for raw speed.

This project, termed MIPS-XMP, produced a 100 percent fully functional 32-bit microprocessor chip on the first fabrication round. The chip was designed to run at 20 MIPS peak, and the Stanford team currently has parts that work at 17 MIPS peak. Of the 125,000 transistors on the chip, only 25,000 to 30,000 are nonmemory functions. The rest include a big on-chip cache and 32 general-purpose registers.

After the original MIPS project, Hennessy temporarily left Stanford to help form MIPS Computer Systems of Sunnyvale, CA. He still works for the firm as chief scientist, while keeping his position at Stanford. MIPS has introduced a series of RISC boards and systems rooted in the Stanford MIPS experience, but it uses wholly new designs. The company has

announced parts with speeds up to 16 megahertz. Both Patterson and Hennessy see MIPS computers as the most pure commercial versions of RISC ideals.

The MIPS boards and chip sets are meant to be the building blocks for superminicomputers. The CPU cards include 3-, 5-, 8-, and 10-MIPS machines based on a custom 32-bit processor with 10-MIPS performance. This chip has 32 general-purpose registers, instruction support for three external coprocessors, and hard-wired machine code. It doesn't have hidden registers, condition codes, variable-length instructions, or multiple-address modes.

The HP Spectrum

MIPS and Hewlett-Packard made parallel efforts in studying instruction use in programming. HP has chosen an architecture that it calls "beyond RISC" to be the foundation for all its new-generation computers. The Spectrum systems are overdue, with a reported software problem holding them up long enough to embarrass HP, but they promise great speed and compatibility with their popular predecessor, the HP 3000 minicomputer.

That compatibility might have been a primary reason that HP chose to deviate from a strict RISC processor strategy. According to William Worley, the principal architect of the HP Spectrum line, "We have to distinguish between architecture and implementation. Some implementations will realize all of the theoretical efficiencies of RISC. Not all will. Each implementation needs to make sense as a business proposition."

HP made extensive studies of instruction use and tried to keep the CPU to a minimum configuration that would also provide compatibility with the previous generation. Joel Birnbaum, the man HP recruited to start its RISC effort, says that, "Whenever someone suggested we really ought to have a wonderful instruction, like 'test left, shift mask, dim the lights,' we had to ask: 'How often will we execute it, and what is the performance degradation?'" HP wanted op code compatibility along with peripheral subsystem, interrupt response, and I/O compatibility. In fact, the company claims that the next step in the Spectrum line is RISC I/O, that is, direct attachment to the bus from any peripheral.

Although the Spectrum chips will appear in workstations, HP has given most of the attention to their use in minicomputers.

An ARM for AI

ARM (Acorn RISC machine) is the name for a RISC chip developed by one of Brit-

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ain's leading personal computer makers. (Acorn is presently a subsidiary of Olivetti.) The company wanted a new processor for AI applications involved with Britain's fifth-generation computing project, Alvey.

What Roger Wilson, Acorn's senior software designer, wanted was a 32-bit microprocessor with some of the advantages of the 6502 from MOS Technology. Specifically, that meant good interrupt-handling capability. Wilson felt that many 16- and 32-bit chips lagged behind the 6502 in interrupt handling. In 1983 he began looking for new designs.

The work on RISC caught his attention, and over the next 18 months, a four-man design team from Acorn used software tools from VLSI Technology Inc., of San Jose, California, to structure a single 25,000-transistor chip that comprised a full 32-bit microprocessor: the ARM. (VLSI has nonexclusive marketing rights to the chip.) This chip is already available on evaluation boards and will eventually form the basis of a new family of Acorn products.

The first samples of the ARM were

complete in April 1985. They were fabricated in 3-micron double-metal CMOS and occupied 50 square millimeters of silicon real estate. This is significantly smaller than most microprocessors. For instance, the 68020 puts 192,000 transistors onto a chip of 80-mm². That difference in size means better yields for ARM production and therefore much lower prices for the chips.

Acorn claims that the ARM has a factor-of-4 advantage in that respect already with the 3-micron chip. According to Simon Woodward, the ARM systems product manager, Acorn plans to scale the design for fabrication in 2-micron double-metal CMOS, a process that should generate a 30-mm² chip.

At that size, the ARM might have as much as a factor-of-10 advantage in price over commercial 32-bit microprocessors. "We get better performance than a Motorola or Zilog with about one-tenth the number of components and a much smaller chip," says Steve Furber, senior designer at Acorn's business division.

According to Acorn, the 2-micron version should be able to produce 3 MIPS.

That's about twice the CPU performance of a VAX-11/780. Even at that pace, it can work with comparatively cheap, slow (4-MHz) RAM chips. Some other fast microprocessors require expensive, high-speed RAM to make a fast system.

The present ARM chips run at around 4 MIPS, peaking at something over 6.6 MIPS. They are primarily intended for use within microcomputers, but because of their extremely good interrupt responses, Woodward suggests they would do well in real-time systems and industrial controllers. The fast processing is not limited to LISP, as some press reports have claimed. ARM chips can support a wide range of high-level languages. However, running LISP, they can outperform a Symbolics 3670 workstation, according to Acorn.

Since the chips began to appear in 1985, Acorn has been working on support chips and evaluation systems based on the ARM. Acorn has designed a set of ARM-related controller chips that handle memory, I/O, and video. The video chip also has a full sound system on it. The

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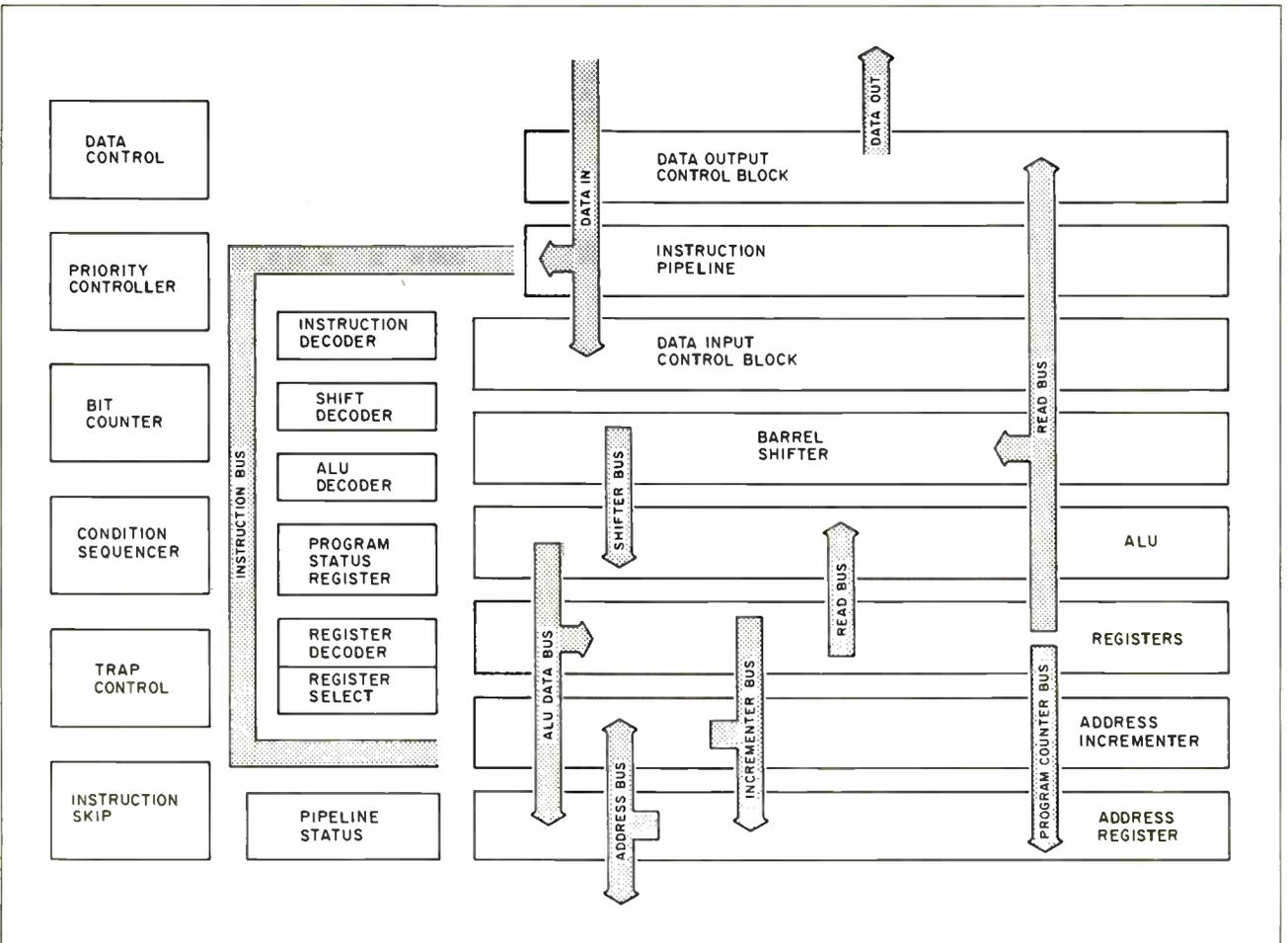
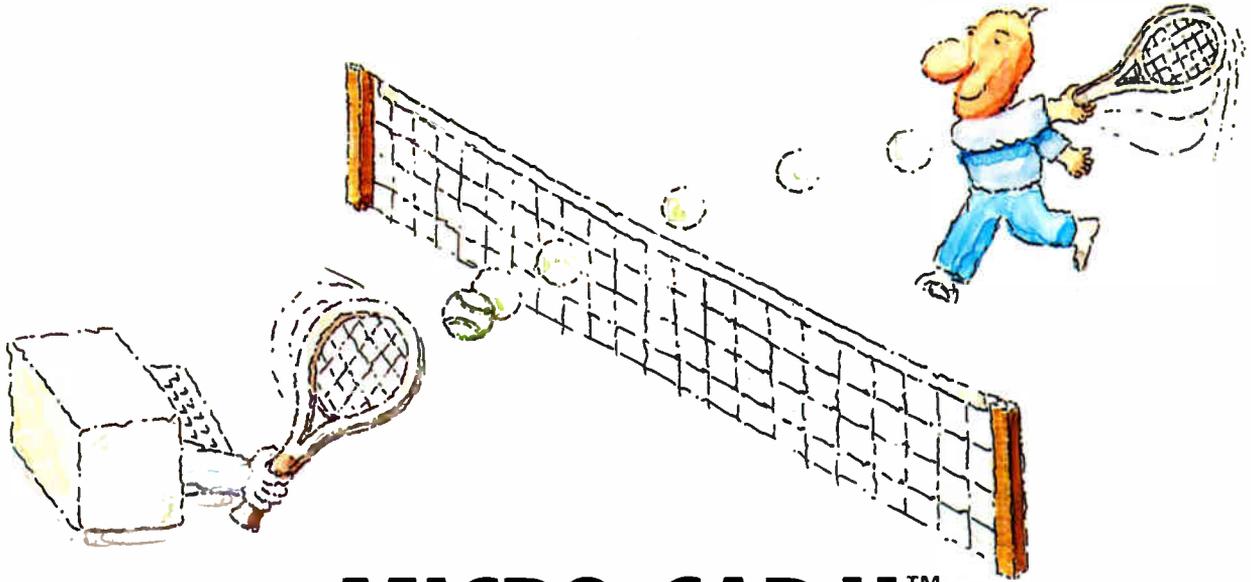


Figure 4: The ARM block-and-position diagram.

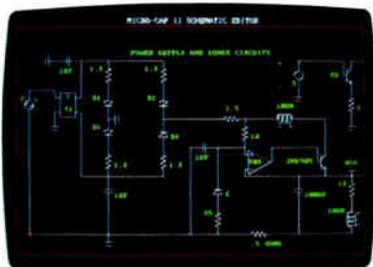


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Universities continue to explore RISC, with processors aimed at symbolic processing.

ARM can work without these chips, but they make a more powerful system if combined with it. One of the evaluation systems was on the market at press time, and the other was scheduled for early this year. Woodward says Acorn is "looking at a number of possibilities of distribution in the states," but the firm "can handle direct contact with U.S. companies and is doing so now."

Gallium Arsenide and RISC

Gallium arsenide (GaAs) can be used in place of silicon for many integrated-circuit purposes. It has several key advantages, including radiation hardness and less temperature sensitivity, but its key advantage to most computer makers is its speed. Because electrons travel faster in GaAs, circuits built on GaAs wafers can be faster than the same circuits on silicon.

The main disadvantages of GaAs are that it is harder to work with than silicon and the chip makers have less experience with it. However, the state of the art in GaAs-chip technology has produced parts that have several thousand gates or memory cells. Although GaAs technology hasn't yet reached far enough to produce CISC processors, it can be used to implement a simple processor such as a RISC CPU, especially if that CPU is partitioned into a chip set.

However, the Department of Defense needs high-speed, radiation-hard processors, so it decided in the spring of 1984 that DARPA (Defense Advanced Research Projects Agency) would award contracts to several firms to design and make GaAs RISC processors. For high performance, DARPA wanted a single-chip microprocessor, and the only single-chip design that met all its needs was the MIPS chip developed under a DARPA grant at Stanford. Texas Instruments, RCA, and McDonnell-Douglas were chosen as the first-round contractors to make a single-chip, all-GaAs, MIPS microprocessor that could run at 200 MHz. Because of the RISC emphasis on an instruction every cycle, that would mean peak performance approaching 200 MIPS. On the way to that goal, DARPA expected the contractors to make various GaAs chips that embodied part of the final design.

Philip Congdon, manager of gallium arsenide systems and components at TI, says that a team from Control Data Corp. and TI has designed the CPU and is nearly done designing the floating-point processor to accompany it. The chips have about 10,000 transistors in a bipolar technology that uses only one transistor per gate.

Although the 200-MIPS figure is the peak performance, because of the 5-ns clock cycle, a more realistic figure would first subtract approximately 32 percent for NOPs in the pipeline and then decrease what's left by 32 percent for inadequate bandwidth to memory. Even using GaAs memory chips, the system is hampered by radio-frequency effects in the interconnects between chips and is even restrained by the speed of light: Electrons

can travel only about five feet in a single clock cycle. The sustainable performance rate of the TI chips will be about 92 MIPS, about 10 times the capability of other fast RISC processors such as the MIPS or RISC II chips. Congdon expects to see the first chips no later than mid-1987. Figure 5 is a block diagram of the TI/CDC GaAs RISC system. The next chip in the series would be a memory management unit.

While CDC might employ these chips in a supercomputer, TI will be selling them on boards as computer-system demonstration units to the government. When such chips might hit the commercial market is an open question.

Another computer that reportedly includes GaAs parts is the upcoming Cray-3 supercomputer. Seymour Cray's designs are often referred to as RISC-like because of his drive for simplicity and speed.

High Native Instruction Rates Win

The RISC idea has had a huge impact on computer architecture. Even designers who aren't embracing it are borrowing from it. With a raft of new commercial pure and not-so-pure RISC products appearing from the micro to the supermini level, there is no doubt that RISC has outgrown the stage of academic exercise. At the same time, universities continue to explore the RISC idea, particularly with processors aimed at symbolic processing.

How well the eyebrow-raising instruction rates of these new, simplified chips will translate into practical processing power and commercial success is not certain. The next two or three years should provide some answers. Stanford's Hennessy believes that "the state of the art in compiler technology has just started to improve dramatically in the last year." He adds, "One of the real breakthroughs is progress in the register allocation area." Interestingly, the original work was done at IBM on the 801 project. Stanford carried on the research and then a RISC team at DEC's Western Research Lab did more, including work with new algorithms that reinforces the value of general-purpose registers. This should lead to even greater advantages for RISC processors.

Referring to the flagship of Digital Equipment's minicomputer line as a well-known standard, Patterson bluntly states, "I think in the next few years a lot of companies will come out with inexpensive RISC machines that will be faster than DEC's 8600." He continues, "I'd say, if you were going to design a brand new instruction set today, you'd have to be real stubborn not to employ some of the RISC ideas." ■

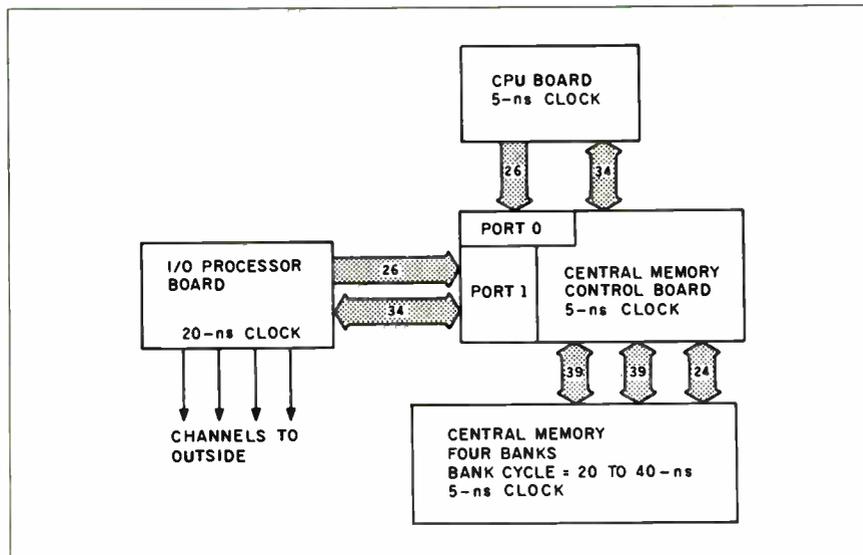


Figure 5: The TI/CDC GaAs RISC-system block diagram.

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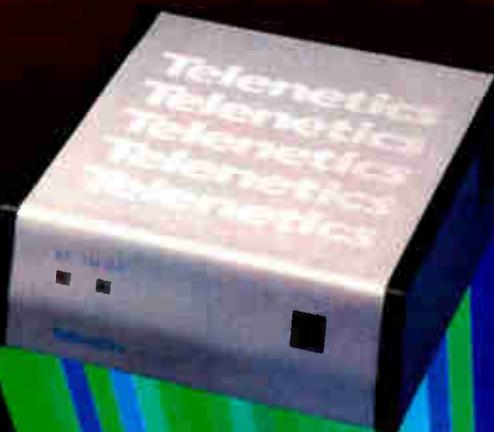
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The RISC/CISC Melting Pot

*Classic design methods converge
in the MC68030 microprocessor*

Thomas L. Johnson

COMPARISONS OF THE relative architectural merits of the reduced instruction set computer and complex instruction set computer methods might prove to be one of the more interesting computer science debates of the late 1980s. However, these two seemingly disparate views of the correct way to build microprocessors might not be as far apart as they seem. This article examines the Motorola 68030 microprocessor with respect to the RISC-like features in this classic CISC machine.

Before delving into the MC68030's innards, I will encapsulate the RISC and CISC strategies. The term RISC is somewhat of a misnomer. The acronym RISC has two commonly accepted meanings. The older meaning is reduced instruction set computer, and the newer is reusable instruction set computer. Both names imply that RISC has something to do with optimizing the microprocessor's instruction set. While this is true, it is also misleading, since RISC is much more than simply an architecture that necessitates a smaller or more efficient instruction set. Likewise, CISC is more than just an architecture that embodies complex or high-semantic-content instructions. It is much more reasonable to label RISC and CISC as implementation methodologies than as architectural constraints.

The Tenets of RISC

The major tenet of RISC is the investigation of the assignment of system functionality within an architecture. RISC strategies normally lead to the offloading of the more complex or infrequently used instructions onto the compiler. The in-

structions and addressing modes that are left on the RISC processor are those frequently used by code generators embedded in compilers, those most advantageous to a language, and those that are vastly more efficient if implemented in hardware. Overall, the following RISC implementation features lead to improved performance:

Single-cycle operation for every instruction—In order to operate in a single cycle, an instruction must be either relatively simple or backed up by additional hardware logic. Whether simple or not, single-cycle instructions yield rates of many millions of instructions per second. High MIPS rates by themselves do not directly indicate the amount of work accomplished but only how fast the engine is running to accomplish the work. A good analogy is a car engine's revolutions per minute versus the same car's miles per hour. The lower the gear, the higher the rpm for a given mph. The rpm by itself will not let you determine how long it will take to travel a distance, only how hard the engine will work during that time.

Load/store design—This point dictates that only load and store operations should reference external memory. This tenet lets all other implemented instructions follow the criterion of single-cycle operation since they will then have to operate only on on-chip registers (memory references can be indeterminate in length of time due to normal memory-access delays such as refresh and direct-memory-access controllers).

Hard-wired control—Microcoded architectures have variable-length instruction size and execution time. In a CISC machine, microcode is a highly desirable trait because it lets the designer implement many flexible, complex (high semantic content) instructions and addressing modes in minimal silicon real estate. In a RISC machine, however, microcode is less desirable. Microcode doesn't lend itself to single-cycle operations as directly as dedicated hardware logic, since the microprocessor's hardware has to dynamically interpret microcode.

Relatively few instructions and addressing modes—Adherence to this point facilitates the implementation of both single-cycle operation and hard-wired control with a relatively small investment in design time and silicon real estate. More easily decoded instructions plus simpler addressing modes can yield faster execution.

Fixed instruction format—This tenet, once again, simplifies the design of the control circuitry. Less complex circuitry can normally run faster overall.

More compile-time efforts—This criterion states that much of the static runtime complexity can and should be handled prior to run time by an optimizing compiler. An example of this would be the generation of an intermediate language by all language compilers, which

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in turn is compiled by an intermediate optimizing compiler into object code (i.e., common pseudocode rear-ends on all compilers). This software technology can also be used to great advantage on CISC machines, and this capability is just now coming into vogue.

Minimal pipelining—Pipelining in a CISC machine allows more efficient use of the available bus bandwidth and lets it produce performance equivalent to a RISC architecture.

The combination of these tenets allows the design of a processor using minimal design time and silicon area but requires a very complex compiler. The designer can then put these silicon savings to advantage by implementing a number of helpful features, such as overlapping register sets (called multiple register sets—greater than 100 registers is not unusual for RISC machines), special hardware (barrel shifters, floating hardware, cache memories, hardware multipliers), or special functionality (interprocess communications hardware).

A machine with a reduced or simplified instruction set does not necessarily have a crippled instruction set. Due to the massive numbers of on-chip registers, most program variables needed by a given procedure will be kept in the machine. Therefore, each reference to a variable need not be surrounded by load and store instructions. The RISC 1 implemented at the University of California at Berkeley in the late 1970s, for instance, has 138 thirty-two-bit registers arranged as 8 overlapping windows of 24 registers each. You can use 6 registers for parameter passing into and out of called routines. Thus, a procedure call/ return is a simple matter of updating a "window pointer" and changing the program counter. This simple procedure means that no data transfers to the external world actually take place.

CISC Performance

CISC computers attempt to squeeze the most performance out of any given architecture. Since designers can make internal microcode execute much faster than external instructions, the overriding concern of a CISC implementation is to build into the processor high-semantic-content instructions (where such instructions are useful) that reduce the number of external instructions that the microprocessor must fetch.

Additionally, microcode allows the inclusion of many varied addressing modes and several control points in the microprocessor's internal hardware. Microprocessors like the MC68030 normally

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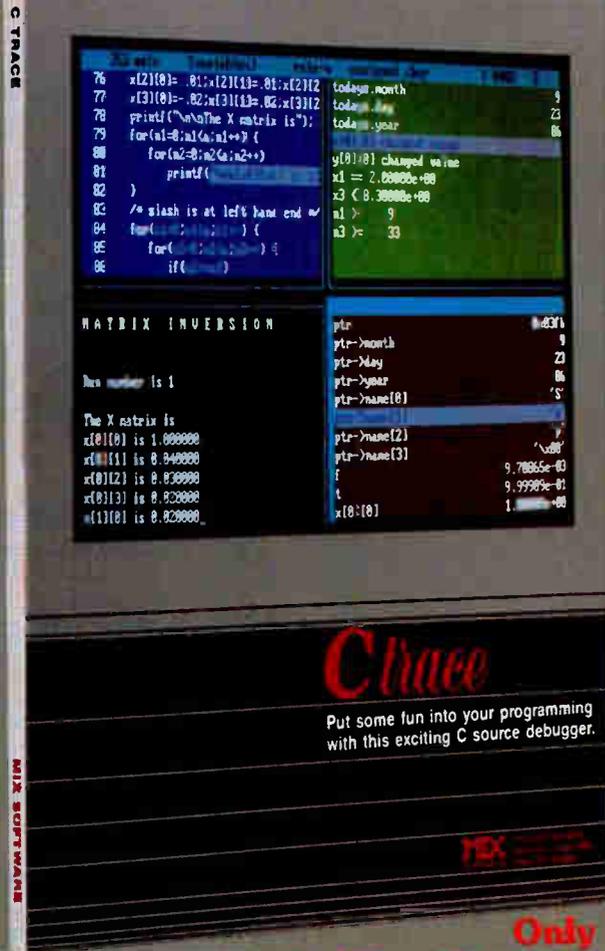
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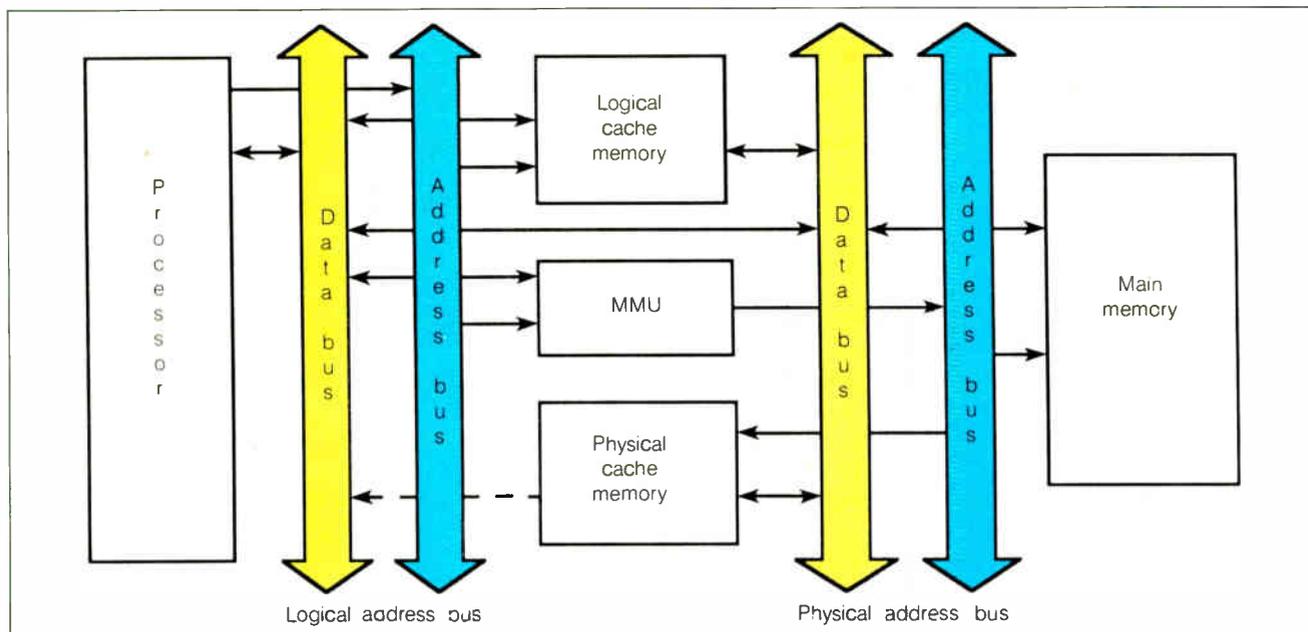


Figure 1: The traditional approach to interfacing a microprocessor to memory.

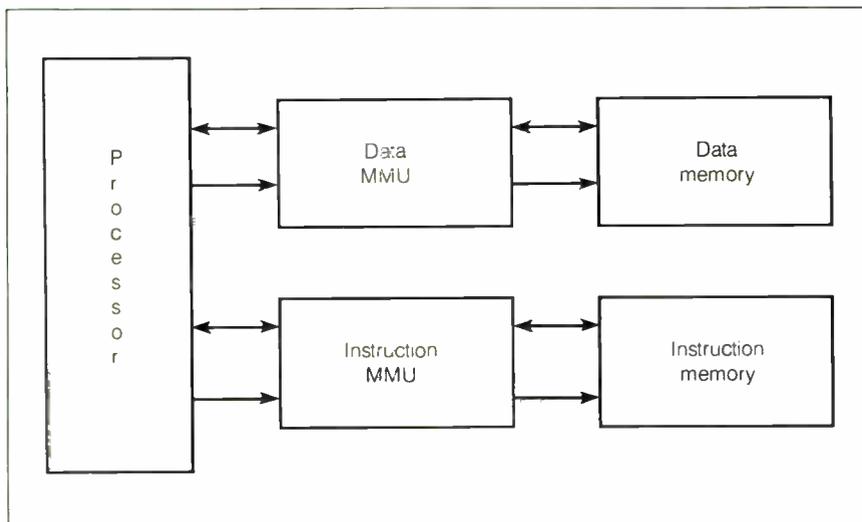


Figure 2: The Harvard-architecture method of linking a processor to memory.

do not attempt to limit the programmer/compiler to load/store architectures. However, they do incorporate many high-level constructs to assist high-level language-compiler writers (features such as simple stacking primitives for procedure calls/returns). Due to the circuit complexity that results from CISC implementations, much more time is normally involved in the design/debugging of the processor and much more care must be taken to ensure proper operation at high clock rates.

Overall, the trade-offs between the traditional CISC and RISC implementation philosophies are normally ones of circuit complexity and assignment of system fea-

tures between the software and hardware elements.

The von Neumann Bottleneck

A common problem incurred in both RISC and CISC microprocessor design is the von Neumann bottleneck, where microprocessors process information faster than the memory system can supply it. This problem has several solutions. The most traditional approach is for the system designer to implement some sort of cache to act as a buffer between the main memory and the microprocessor. This cache can take several forms, and I will not attempt to discuss the relative merits of the various cache designs here.

Suffice it to say that a cache memory is a fast-access (relative to the main-memory system) local memory where copies are kept of the most recently accessed main-memory locations, along with some bookkeeping data.

Another recent approach to limiting the effects of the von Neumann bottleneck is *alternate architectures*. The most widely known of these, the *Harvard architecture*, presents separate paths to the memory system for instructions and data. This technique almost doubles the available bus bandwidth, allowing the processor to wait on the memory subsystem less often and allowing other attached processors (i.e., DMA processors) to affect the main processor less. Figures 1 and 2 show these two techniques. Designers can use cache memories, Harvard architectures, and other bandwidth-saving techniques to great advantage on both CISC and RISC processor implementations.

The MC68030

The Motorola 68030 builds upon the architecture born in 1979 with the release of the MC68000. For a complete discussion of the M68000 series of processors, see my article "A Comparison of MC68000 Family Processors" in the September 1986 BYTE.

While each of the M68000 microprocessors is based on the same CISC architecture, each has one very RISC-like feature: a large, undedicated, full-width register complement. The supervisory- and user-level programming models for these processors are shown in figures 3 and 4.

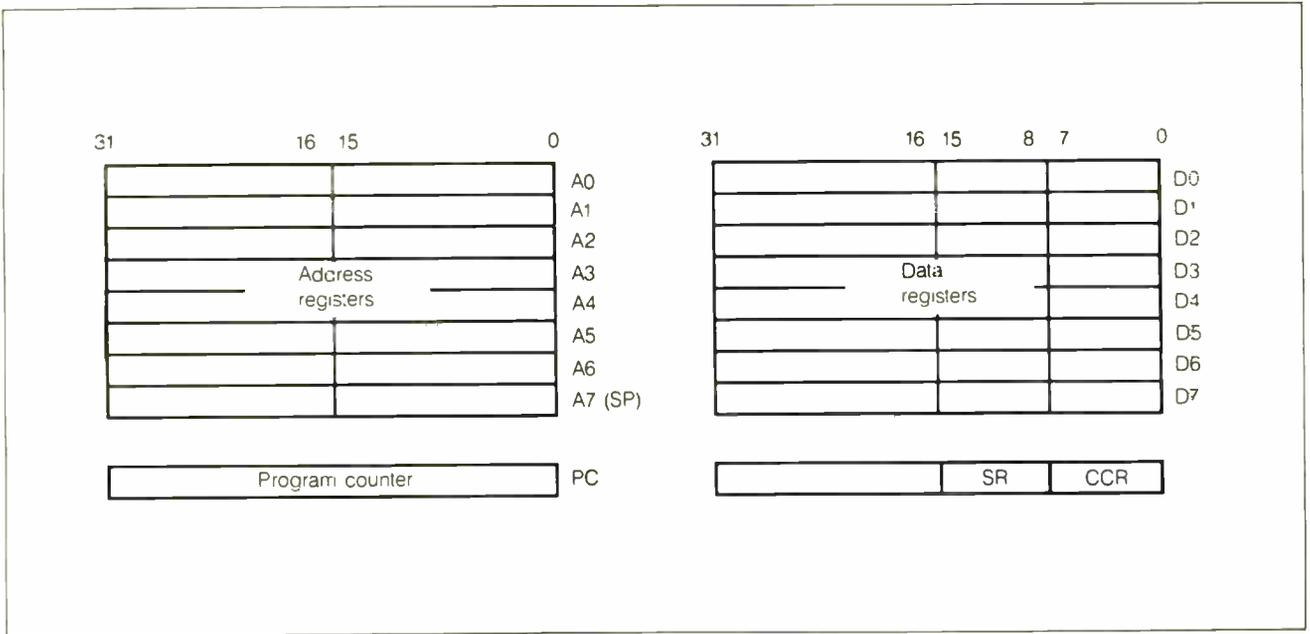


Figure 3: The user programming model's registers in the M68000 series.

In addition to the register set, the M68000 series has specific hardware designed to make the processor execute instructions as efficiently as possible. This hardware includes full-width internal 32-bit data and address buses regardless of the size of the external paths, separate ALUs for addresses or data that allow simultaneous address and data calculations, 3-byte instruction pipelines for the MC68000/008/010, and a 3-word instruction pipe for the MC68020. The MC68020 also includes full on-chip support for the coprocessor interface to allow the attachment of closely coupled coprocessors (such as the MC68881 or MC68882 floating-point coprocessors or the MC68851 paged memory management unit), a 256-byte on-chip instruction cache memory, and a 32-bit bus data buffer that acts as a prestaging area for the instruction pipeline and a holding area for data transfers.

RISC-like Features in the MC68030

The MC68030 maintains full upward object-code compatibility for user-level programs and is still a full virtual processor, capable of both virtual memory and virtual machine operation. Note that the MC68030 maintains the same programming models as the MC68020 and adds functionality to the supervisory-level registers (see figure 5). The MC68030 has all the features and functionality of the MC68020.

Many of the MC68030's features are those you might expect to find only in RISC machines. This reinforces the con-

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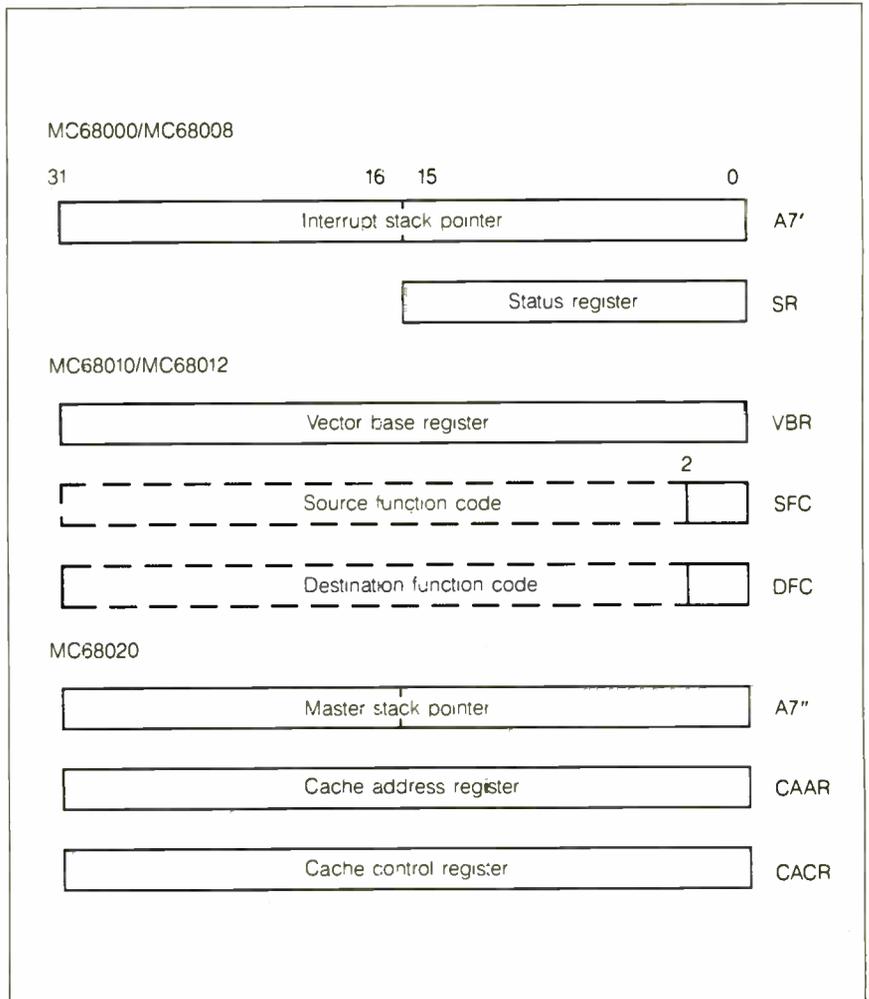


Figure 4: The additional registers in the supervisory programming model.

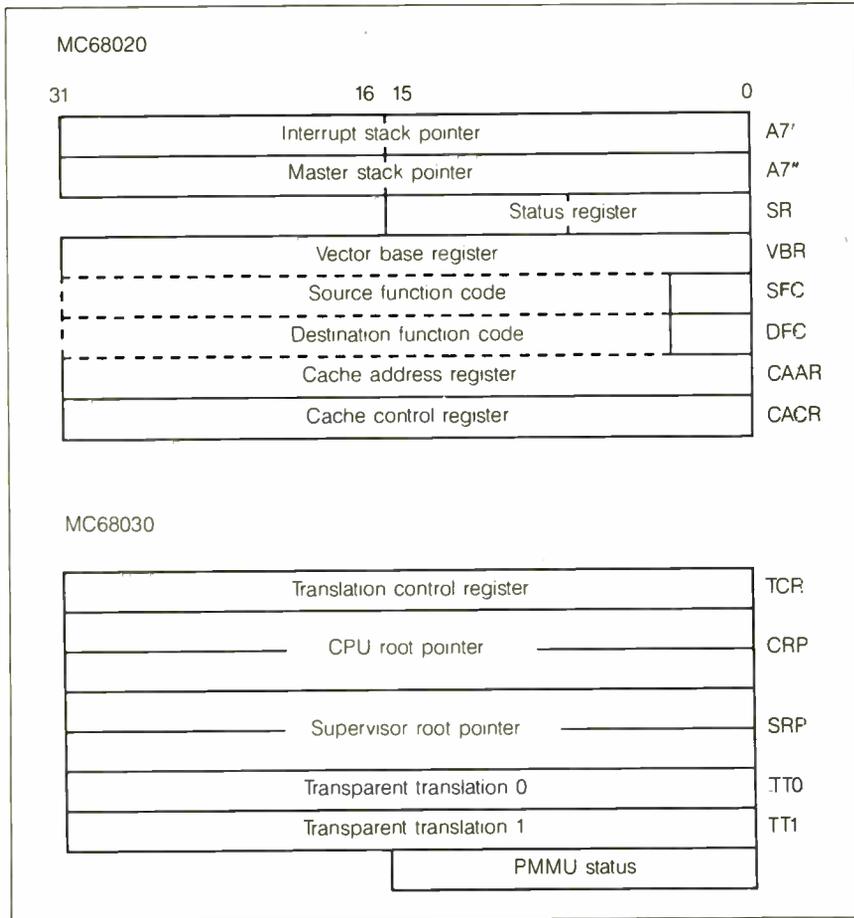


Figure 5: Additional MC68020/MC68030 supervisory model registers.

cept that RISC is not an architecture but rather an implementation method that can be applied equally well to CISC processors. As I look at some of the MC68030 features in detail, refer to figure 6.

First, although the MC68030 incorporates a two-cycle execution unit rather than the single-cycle EU found in some RISC processors, the time required for an instruction to execute can be as little as zero clock cycles. This is due to the overlapping nature of internal/external bus activity and the autonomy of internal processor resources.

Working in conjunction with the two-cycle EU is the unique two-level microcode structure, which is perhaps the MC68030's single most non-RISC feature. The initial instruction decode generates a call into the first level of microcode. Here, specific *nanocode words* are called to generate the proper control signals for instruction execution.

Due to the methods employed, adding new instructions—or modifying the way in which current instructions execute—is simply a matter of modifying the microcode; you don't need to modify the execution hardware. Once you have verified execution hardware, you can verify all instructions by verifying the contents of the microstores. Simply put, if you were to slice the MC68030 horizontally across the die, you could consider the upper half (the microstores) a software interpreter and the lower half (the EU, caches, etc.) a RISC engine (see figure 7).

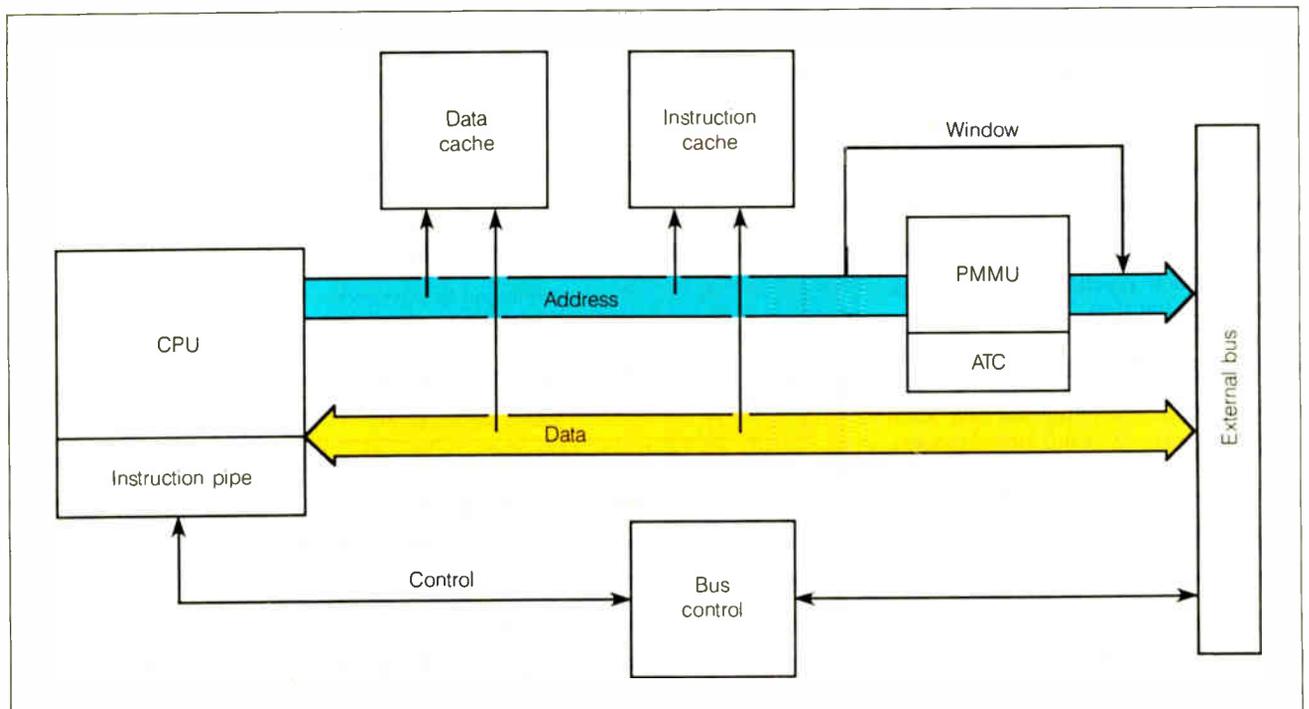


Figure 6: A functional block diagram of the MC68030 microprocessor.

The MC68030 also features a 256-byte data cache to complement the 256-byte instruction cache. The caches are arranged as 16 lines of four longwords (32-bit values) each, with each longword separately accessible. Whereas the instruction cache is read-only, the data cache has a user-selectable write-allocate policy to help prevent the stale-data phenomenon that occurs when data is written to the cache and not to main memory. Due to a combination of the write-allocate policy and a cache-content-freezing mechanism, you treat this cache like a 64-entry by 32-bit extension to the normal eight data registers. This means that the on-chip complement of registers can appear to be a total of 80 registers in either the user or supervisory programming model. This is more than many current RISC microprocessors.

The two design goals for the MC68030's caches were to reduce the processor's external bus activity over that of the MC68020 and to increase effective CPU throughput, even though larger memory sizes or slower memories increased average access times. The throughput increase directly attributable to the MC68030's instruction and data caches is derived by three basic means. On-chip caches can be accessed in less time than external memories, providing improved access times for data residing in the caches.

The burst-fill capability of the caches lets data be found in the caches even though they have never been accessed before, lowering the average access times for data in the cache even further. In burst-fill operation, the MC68030 will always attempt to completely fill a cache line. To accomplish this, it might request a burst fill from external hardware during a data/instruction read. If the external hardware can operate in a burst mode for this access, it will respond to the MC68030 to indicate this fact. The MC68030 will then simply latch data on the trailing edge of each successive clock until the cache line is filled.

Harvard Architecture

The structure of the instruction and data cache memories and the way in which they are incorporated into the overall microprocessor architecture make the MC68030 the first CPU to use a modified Harvard architecture internally on a single chip. The autonomous nature of the caches lets accesses to both caches and external accesses occur simultaneously with instruction execution. This parallelism of instruction execution, along with instruction and data accesses to both caches and the external world, is enhanced to allow multiple instructions to

execute concurrently internally along with a single data access to the external world.

The microprocessor has three separate internal 32-bit buses for data and instruction movement. Consequently, there are separate paths to memory for both instructions and data within the chip. Because of these multiple buses, the execution unit can access data from the data cache and instructions from the instruction cache while simultaneously fetching an operand from the external world. Until now, this modified Harvard capability has been almost entirely a feature of RISC machines.

Three-Stage Pipeline

The MC68030 uses a three-stage instruction pipeline much like that of the MC68020. The size of the pipeline is a trade-off between increasing the performance of the on-chip EU on interpreted microcode and the frequency of branches in normal code. A pipe that is too long must be repeatedly cleared and refilled as program branches take place. However, a microcoded processor without any type of instruction pipeline uses too much time in the sequential execution of in-line instructions. It is, therefore, helpful in microprogrammed architectures to let the processor work on the various phases of instruction execution simultaneously whenever possible without unduly wasting time on decoding instructions that will never be used due to branching. Sim-

The on-chip complement of registers can appear to be a total of 80 registers in either model.

ulation studies show that a three-stage pipeline is optimal for the M68000 architecture.

To further reduce the effects of the von Neumann bottleneck, the MC68030 can run three different types of external bus cycles on a bus cycle by bus cycle basis. These three types are asynchronous bus cycles (the same type of bus cycle run on the original MC68000), synchronous two-cycle bus cycles, and the burst bus cycles—the previously discussed bus cycle that works well with newer RAM technologies such as static-page and nibble-and-column-mode dynamic RAMs and allows the transfer of up to four 32-bit values in as little as five clock cycles. The burst-fill type of bus cycle is requested by the MC68030 whenever possible. However, external logic is free to choose the type of bus cycle needed.

On-Chip Hardware for Instruction Support

One of the most basic concepts of RISC architectures is that of hardware support *continued*

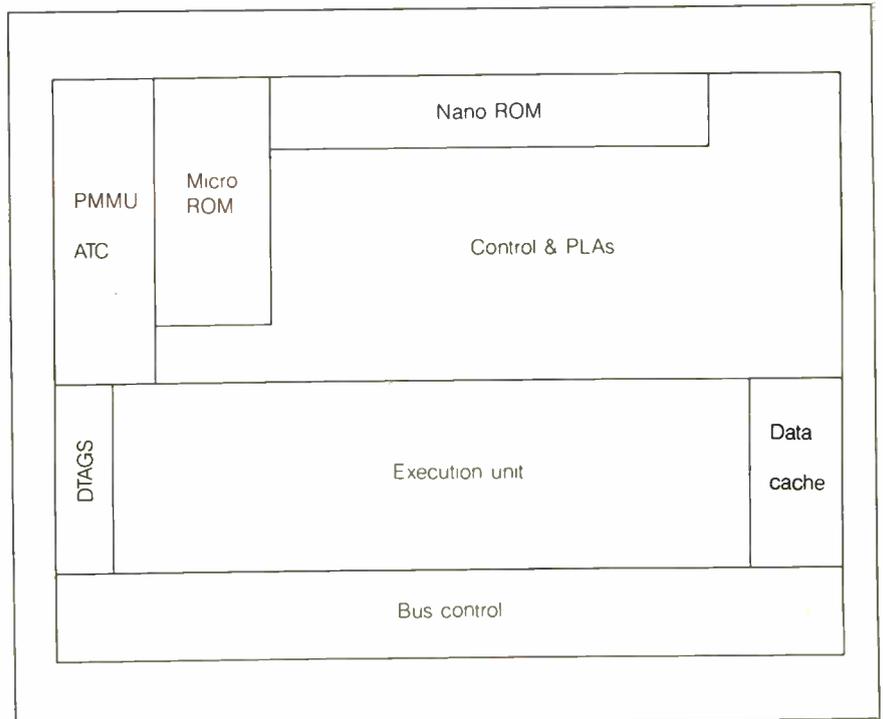


Figure 7: The location on the chip of the various MC68030 circuits.

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for instructions. The MC68020/MC68030, although not RISC processors, have an impressive amount of on-chip hardware for special instructions. This support includes a 32-bit barrel shifter that lets the processor shift or rotate a 32-bit value up to 32 bits in a single clock cycle. Additionally, all ALUs on the devices are a full 32 bits wide. Also assisting in overall execution is the MC68851 paging MMU, brought on-chip in the MC68030. This paging MMU, with on-chip translation descriptor cache, lets the MC68030 generate physical addresses for the external memory subsystem with no additional delay (address translation occurs in parallel with other processor activities).

Finally, one of the bastions of RISC is that due to the simpler nature of the hardware, it can obtain substantially higher clock rates. This is not without its problems. To use these higher clock rates, external memory must be made to respond without imposing so many wait states that the faster clock becomes meaningless. The MC68030 has a design frequency of 20 megahertz. The original design frequency of the MC68000 was 8 MHz, and it is currently offered by Motorola in 12.5-MHz frequencies. The design frequency of the MC68020 was 16.67 MHz and is currently offered in speeds to 25 MHz. If past performance is any indicator, it is safe to assume that the MC68030 will be offered in speeds substantially higher than 25 MHz and average performance of much greater than 5 MIPS.

Conclusion

It is a serious mistake to assume that the acronym RISC stands for higher performance than the acronym CISC. Instead, it is more accurate to say that RISC represents a step forward in defining a set of methods that can be used to advantage in the implementation of any microprocessor architecture. The RISC feature that I believe holds the most promise for the future is in the area of division of overall system responsibility between the microprocessor's hardware and intelligently written high-level language compilers. It is important to remember that, although a genre of applications exists for which assembly language coding is essential due strictly to performance—especially *real-time performance*—the number of applications that fall within this genre is diminishing. In the end, regardless of whether an architecture is labeled RISC or CISC, it is up to the system implementors to choose the architecture that most directly addresses their concerns for the highest, most cost-effective performance and reusability of their current systems and applications software. ■

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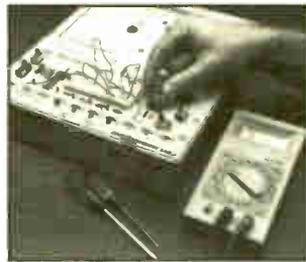
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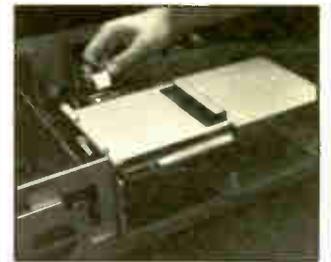
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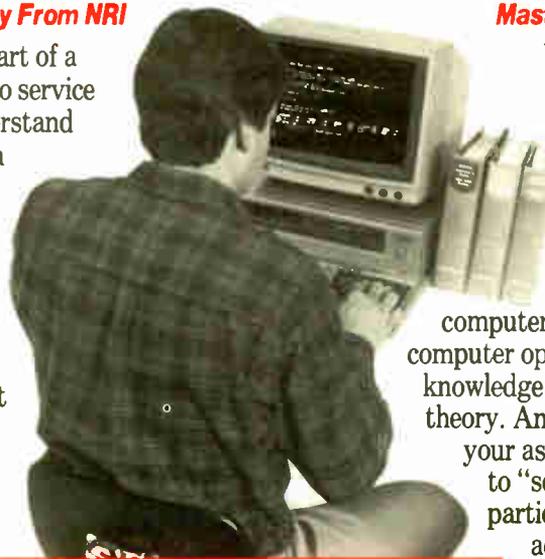


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The Fairchild Clipper

*A microprocessor that attempts to balance
the best of CISC and RISC*

Mike Ackerman and Gary Baum

THE FAIRCHILD CLIPPER processor differs from other commercial 32-bit microprocessors architecturally as well as mechanically. Its features include a balanced instruction set, high-bandwidth dual buses, caching, hardware-managed pipelining and resource allocation, concurrent processing units, and hardware-based operating system support. Moreover, it can process up to 33 million instructions per second.

The processor comes as a preassembled module. Physically, it comprises a set of three CMOS VLSI chips and a smaller CMOS clock generator, which partition processing and memory features to minimize interchip traffic. These chips include the combined CPU/floating-point unit; the two identical cache/memory management units (CAMMUs), one for data and the other for instructions; and the clock generator chip, which distributes the required clock signal.

Balancing CISC and RISC

Clipper's instruction set fosters fast-executing compiled code from compilers that optimize register use. Unnecessary operations have been eliminated. The remaining operations are relatively simple for globally optimizing compilers to work with. These RISC-like instructions are implemented in fast-acting hardwired logic; most frequently used instructions execute in one 30-nanosecond clock cycle.

In accord with RISC philosophy, Clipper is essentially a load/store machine in which all arithmetic and logical instruc-

tions operate only on data in registers; only loads, stores, branches, calls, and stack manipulations access memory. The hardware architecture provides the needed registers: thirty-two 32-bit registers, sixteen for the operating system and sixteen for user programs. To simplify and speed up decoding, all instructions are formatted as multiples of 16-bit parcels. The most frequently used instructions are the shortest.

The instruction set includes 101 hardwired and 67 high-level macroinstructions that operate on the basic data types. Each instruction specifies the operation to be performed, plus the type and location of its operands. These operands can reside in memory, in a register, or within the instruction itself. To speed decoding, all instructions contain from one to four 16-bit parcels. Figure 1 details Clipper's instruction formats.

These instruction formats fall into two groups, those with addresses and those without. Instructions with addresses are those that must access memory, such as loads, stores, and branches. Instructions without addresses are the arithmetical and logical types and generally can execute in one clock cycle. Although instructions can have zero, one, or two operands, only one operand can access a memory address.

Clipper's instruction set consists of 10 functional categories. Load/store instructions transfer addresses, bytes, halfwords, words (32 bits), longwords, and floating-point quantities (single and double) between memory and registers. Move instructions transfer 32- and 64-bit

quantities between registers (integer and floating point).

Arithmetic instructions operate on register contents or intermediate values of variable length. These include add, subtract, multiply, divide, negate, modulus, and scale operations. Logical instructions operate on register contents. These include AND, OR, exclusive-AND, and NOT operations.

Shift/rotate instructions operate on words and longwords. Conversion instructions can change single- or double-precision floating-point numbers into integers rounded to IEEE specifications. Compare instructions test the value of words or floating-point numbers of either precision; an atomic test-and-set instruction is also included.

String instructions (compare, initialize, and move) manipulate character strings. Stack instructions manage program and system stack. These include push, pop, save multiple registers, and restore multiple registers. Control instructions include branch, call, call supervisor, return, and NOP.

Scattered throughout these 10 categories are the 67 CISC-like macroinstructions. For example, all conversion and string instructions are macros; except for push and pop, some stack operations are

continued

Mike Ackerman is a design engineer and Gary Baum is strategic marketing manager at Fairchild Semiconductor Corporation, Advanced Processor Division, 4001 Miranda Ave., Palo Alto, CA 94304.

macros; and some move, arithmetic, and control instructions are also macros. Except for format, however, programmers should see no difference between macros and faster-acting hard-wired elemental instructions. In fact, each macroinstruction is implemented in the CPU's macroinstruction unit as a sequence of the hard-wired instructions.

Additional CISC-related features include a complete set of nine addressing modes for load/store instructions to facilitate access to the complex data structure elements (e.g., arrays, records, and arrays of records) of typical high-level languages. Clipper provides separate modes, with dedicated resources and unique privileges, for users and the oper-

ating system. Moreover, hardware support exists for key OS functions such as system calls, exception handling, and virtual memory.

Clipper provides nine memory-addressing modes (see figure 2) to specify a unique virtual address as the sum of several factors. With the relative mode and

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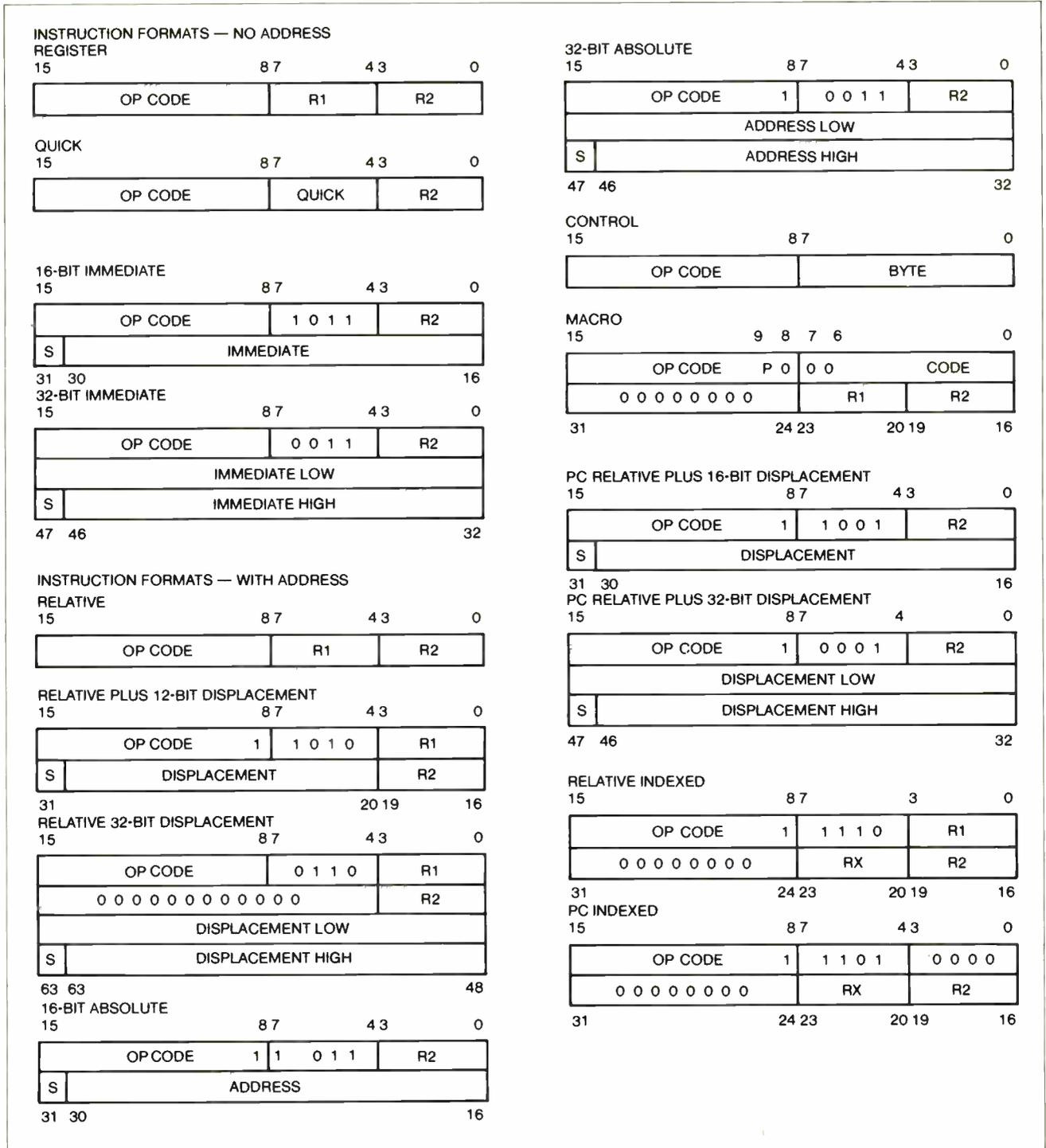


Figure 1: Clipper's balanced instruction set blends 101 RISC-like hard-wired streamlined instructions with 67 CISC-like macros.

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the two relative-with-displacement modes, the virtual address in question either is in a register or is to be computed as the sum of the values in a specified register and the displacement carried with the instruction itself. The two absolute modes carry within the instruction the virtual address as a pure displacement value. The two program-counter relative modes facilitate branching relative to the program counter's current value. The two indexed modes sum the two specified register values to arrive at the virtual address.

These addressing modes facilitate access to data structures, such as arrays and records, commonly used in high-level languages. Figure 3a maps how the relative-plus-displacement mode accesses an array entry. Items in a two-dimensional array are accessed via relative indexing in figure 3b.

In the one-dimensional array, the dis-

placement value points to the array's base, while the register value defines the offset of the item at hand. Simply incrementing the register by a fixed amount causes the same addressing mode to point to the next item in the array. Thus, a sequence of items from an array can be quickly accessed using a loop with only one basic instruction and a fixed addressing mode.

In the two-dimensional array, one register value points to the first item in the selected row, while the second register defines the item's offset within the row. Incrementing the first register yields the same offset in a new row, while incrementing the second register points to the next item in the same row. Thus, the instruction stays the same while entries in a whole set of two-dimensional arrays are accessed by simply incrementing registers. Except for the initial instruction fetch, all operations can proceed on-chip.

Clipper supports 10 distinct basic data types. These comprise both signed and unsigned versions of bytes, 16-bit half-words, 32-bit words, and 64-bit long-words; 32-bit single-precision and 64-bit double-precision floating-point numbers that conform to the IEEE standard are also included primarily for technical or workstation applications. These primitive data types can serve as building blocks for the more complex structured data types, such as arrays and records.

Exception Handling

Exceptions are those internal hardware conditions, external events, or even particular instructions whose detection causes the system to suspend normal processor operation and in its place perform some special predetermined sequence of operations.

Essentially, exceptions fall into three categories: traps, interrupts, and super-

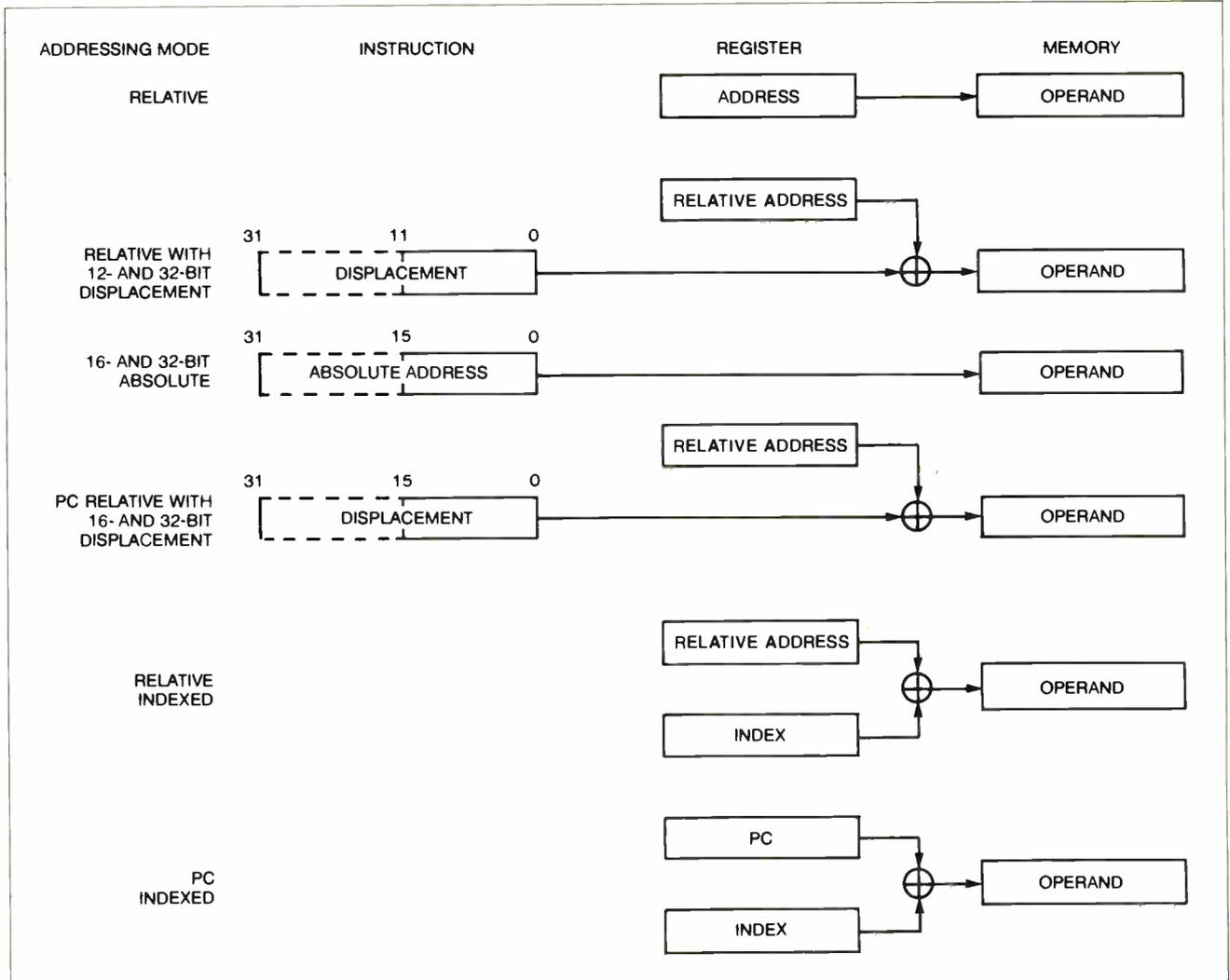


Figure 2: Nine modes for addressing the virtual address space help systems and programmers deal efficiently with data structures.

visor calls. Traps are anomalous internal events that can occur while an instruction is being processed. Classic examples range from simple attempts to divide by zero to complexities such as a virtual memory system page fault. Interrupts are a means for external devices to signal to a CPU that they need servicing. An example here could be a DMA controller signaling that it has finished transferring a block of data into memory. Supervisor calls are program-generated requests for services that the operating system provides.

When one of these exceptions occurs, the appropriate software handler must be invoked—usually as soon as possible. This need for immediate action means that exceptions must suspend normal processing. When the handler finishes its task, control returns to the point at which the program halted.

Unfortunately, the same pipelining that boosts system throughput complicates exception handling. When an exception occurs, the pipeline must clear to allow for processing the exception handler as soon as the currently executing instruction is finished. When the exception handler is completed, normal processing resumes. Then the pipeline must refill and the instruction pointer back up to refetch the next program instruction. Because Clipper executes multiple instructions concurrently, simultaneous multiple exceptions, such as a divide by zero that occurs in the same clock cycle as a page fault or floating-point fault, present added complications.

The architecture supports 18 traps, 256 vectored interrupts, and 128 programmable supervisor calls. The traps handle page faults, attempts at violating memory protection, floating-point errors such as an overflow, arithmetic errors such as trying to divide by zero, and violation of a privileged instruction by a user-mode program. Any of these conditions causes the hardware to generate the appropriate trap.

Clipper also handles priority-encoded interrupts. It encodes the interrupt type as one of the possible 256 on the byte-wide interrupt bus and invokes supervisor calls by executing a calls instruction. Within the instruction, a parameter specifies the call type.

Clipper handles all exceptions in much the same way. Initially, the current contents of the program counter (PC), the supervisor-status-word (SSW) register, and the program-status-word (PSW) register are saved on the supervisor stack.

Next, a new SSW and PC are copied from the vector table. This is a data structure that occupies the first real page of memory. The vector table contains the

address and SSW value for every exception-handler routine. Address/SSW pairs are stored in vector table locations corresponding to their particular type of trap, interrupt, or call. The exception-handling software executes using the new SSW and PC values. After processing the exception, the handler routine executes a return-from-interrupt instruction. This restores the old PC, SSW, and PSW values from the supervisor stack. Finally, the program picks up from where it had halted.

Clipper's load/store-type operation requires extensive hardware register support. If most of the instructions are to operate on information in registers, the registers must be available. The register complement includes a 32-bit PC and thirty-two 32-bit general-purpose storage registers that can accommodate addresses or data words. General-purpose registers save program steps when compared to address- and data-dedicated registers by

eliminating unnecessary register-to-register transfers when performing arithmetic operations on addresses. Clipper also contains eight 64-bit registers for floating-point arithmetic.

In support of multiuser operating systems, Clipper has two operating modes: user and supervisor. These modes are distinguished by the registers they have access to and by the instructions each can use. Programs executing in supervisor mode (usually the operating system) have access to the data in all thirty-two general-purpose and eight floating-point registers. Access for user-mode programs is restricted to only sixteen of the general-purpose registers, called the user registers, and to all the floating-point registers. The sixteen registers inaccessible to user programs are supervisor registers. An additional sixteen 32-bit registers and four 64-bit floating-point registers are available to the macroinstruction unit and

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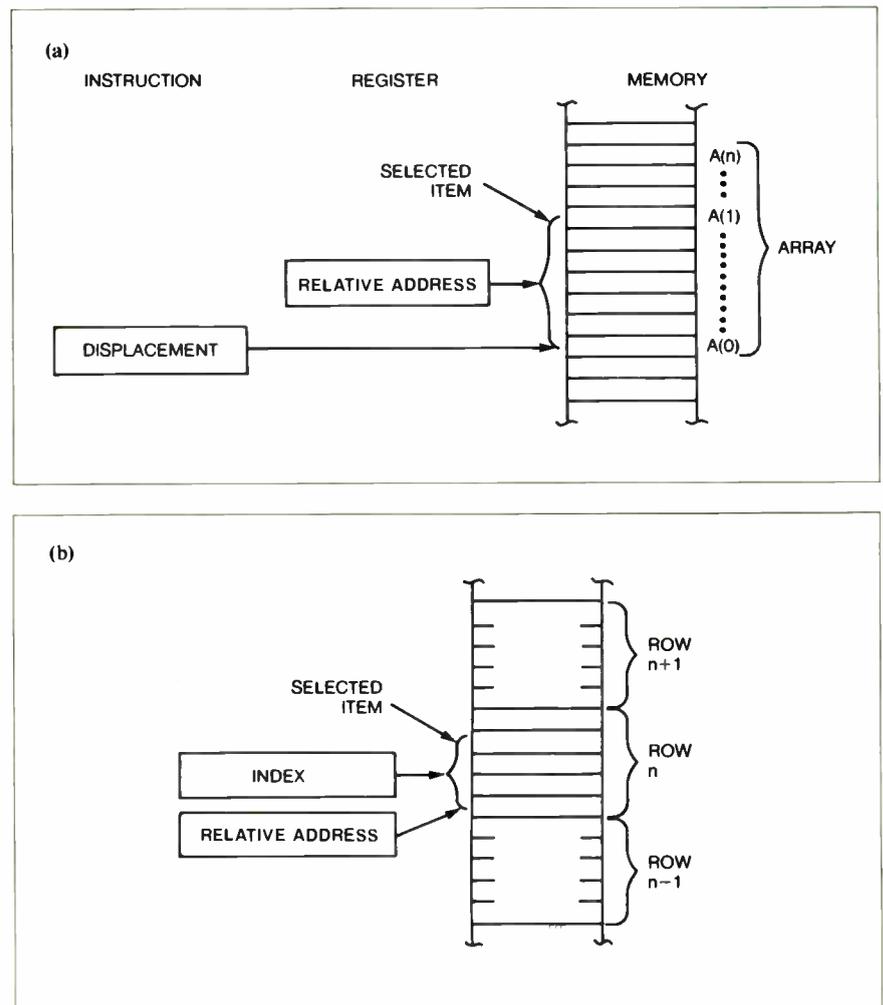


Figure 3: (a) Relative addressing provides a simple means for accessing any array item. (b) Relative indexing facilitates the more complex task of accessing items in two-dimensional arrays.

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FAIRCHILD CLIPPER

are hidden from the user.

The CPU/FPU chip accommodates two 32-bit status words, the PSW and SSW. Both status words contain flag bits that identify and control the CPU. The PSW, which is accessible to both modes, contains the exception flags. The SSW, which is accessible only to supervisor-mode programs, contains the flags for in-

terrupts, address translation and protection, and modes of operation.

Each of the two CAMMUs in the processor module contains five software-accessible registers for initialization and control. Two of these registers (page directory origin registers, or PDOs) contain the base addresses of the supervisor and user page-table directories that are

used for memory-page translation. Another register (fault) contains a virtual address pertaining to a particular fault condition, so that the operating system can use its contents in support of virtual memory processes. The two remaining registers (control and reset) help control the CAMMUs. Figure 4 shows all the

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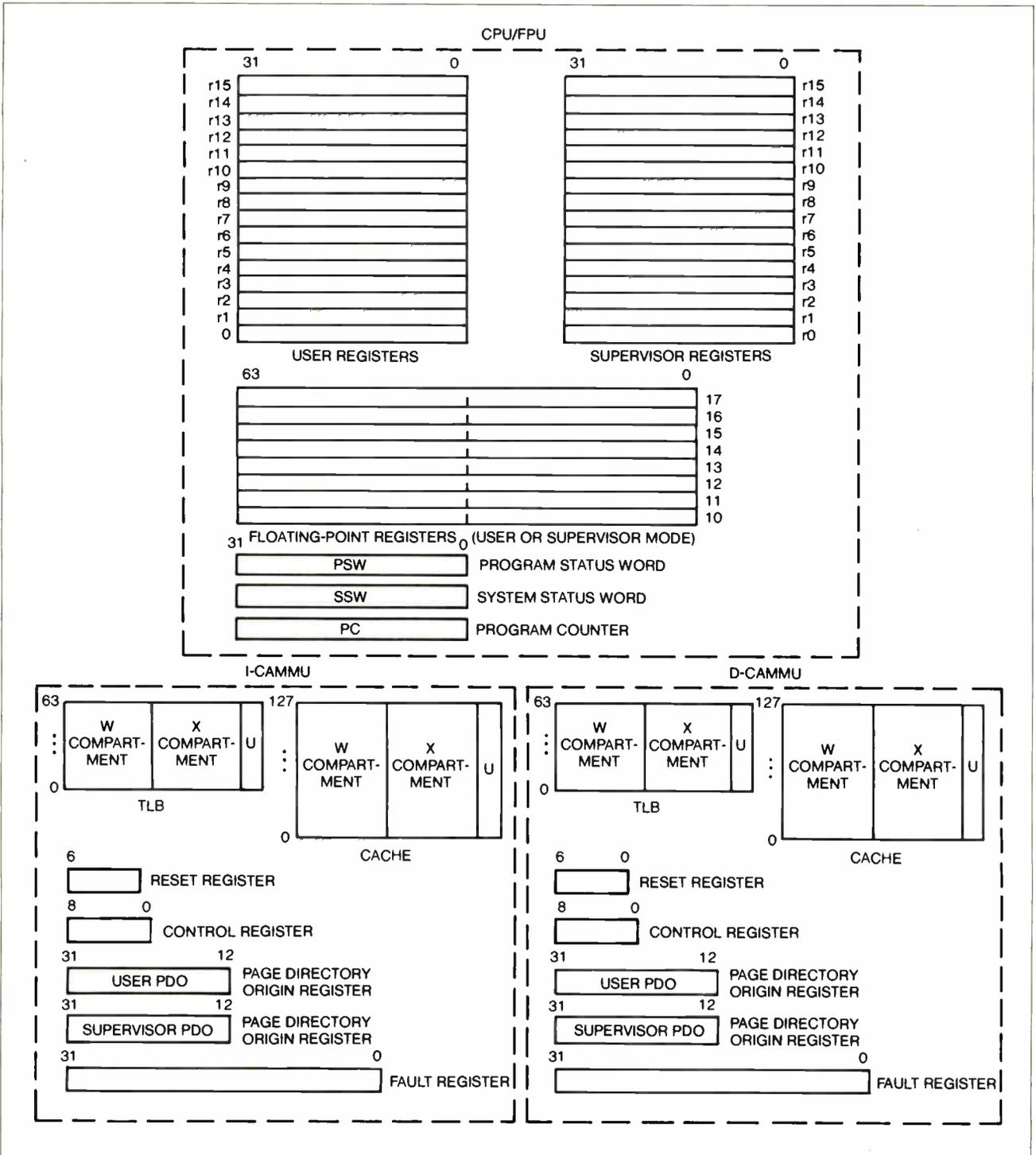


Figure 4: The CPU/FPU chip and CAMMU register sets for user and supervisor modes.

register sets for user and supervisor modes on a module.

Dual-Bus Bandwidth

Clipper uses two buses between its CPU/FPU and the CAMMUs. Each bus is dedicated—one to data and the other to instruction traffic. The two-bus system effectively more than doubles the single-bus bandwidth by eliminating bus arbitration. In addition to raising the bandwidth, the two buses and two CAMMUs increase the caching operation's efficiency.

Burst-mode transfers also enhance the bandwidth over the Clipper bus for information exchanges between the processor module and main memory. Through these, the module can send 16 data bytes (four 32-bit words) for each address word. Figure 5 shows the relationship of the module's VLSI chips to the dual internal and system buses.

Figure 5 also shows the unique partitioning method for the chip set. Instead of an integer ALU alone, the CPU/FPU also contains a floating-point arithmetic processor that can perform more than 2 million floating-point operations per second (MFLOPS). The result is faster floating-point operation than if the data and control signals had to pass off-chip to a floating-point coprocessor. Moreover,

the architecture allows floating-point and integer operations to proceed simultaneously.

Functional partitioning of the cache and memory management functions is evident in figure 5. Dual CAMMU chips integrate all memory access functions onto dedicated chips for data and instructions. Each CAMMU contains a 4K-byte cache plus its control logic and the management logic to support demand-paged virtual memory with ample 4K-byte pages.

Memory Caches

Clipper's closely integrated caches bridge the gap between its 30-ns CPU/FPU and the 500-ns main-memory systems that are practical using 150-ns DRAMs. The full hierarchy extends from 30 ns for CPU registers to over 30 milliseconds for data on disks. Bridging this million-times gap in access times are the main memory and two separate caches, one within each CAMMU. One caches data, while the other caches instructions. Each cache is in reality a two-level mechanism: The 4K-byte main caches each contain a quadword buffer that is, in effect, a smaller high-speed virtual cache.

Information within the main caches is organized into two sets of 128 lines each,

with a line holding a 16-byte quadword. A cache access causes the entire line containing the accessed item to be loaded into the quadword buffer. Subsequent sequential accesses to information in the same line do not require cache access. Instead, the faster quadword buffer satisfies the request.

A quadword buffer can be accessed in one 30-ns clock cycle. Upon a miss (the sought-for information not present in the quadword buffer), two additional 30-ns clock cycles are consumed to access the main cache and perform virtual address translation, making a total of 90 ns. Transferring information over the tightly coupled data or address buses in either direction between CPU and CAMMUs takes 15 ns. Thus, the total access time, including bus time for information in a quadword buffer, is 60 ns, and 120 ns from either of the main caches.

Obviously, a cache improves the CPU/memory access time only when the sought-after information is in the cache. And, of course, sometimes it is not there and a cache miss occurs. Then the miss-replacement time comes into play. Clipper uses a burst-mode technique to transfer a 16-bit line from main memory over the system bus to the cache, typically in

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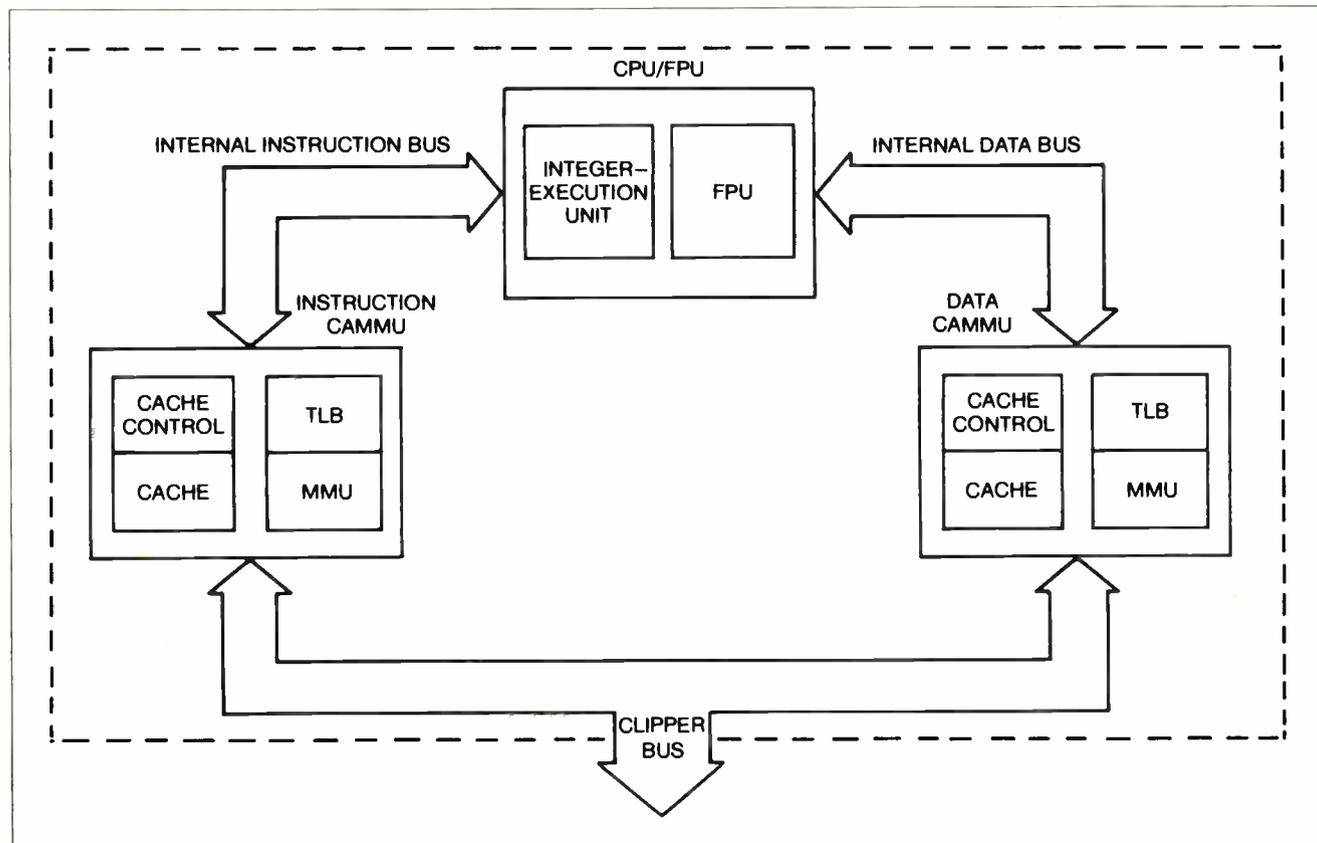
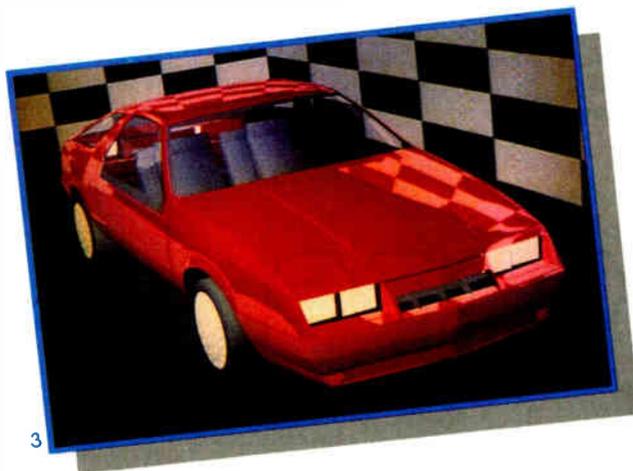


Figure 5: Twin high-bandwidth buses connect data and instruction CAMMUs to the CPU.

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Clipper's caches are closely tied to their on-chip MMUs and their translation lookaside buffers.

half as many clock cycles as conventional microprocessors (figure 6).

If the cache is full when a miss occurs, the newly fetched line must overwrite one of the lines already in the cache. Set associativity of the cache organization determines the cache's flexibility in deciding which line to overwrite. Clipper's two-way set-associative caches divide each 4K-byte total storage into two compartments of 2K bytes each. Thus, information from any main-memory location can be written to one of two locations in the appropriate cache. This flexibility makes it less likely that potentially useful information will be overwritten in response to a cache miss.

The effectiveness of caches, in terms of hit rates, depends on the line size and degree of set associativity as well as the cache size. The curves in figure 7 indicate that Clipper's 8K-byte total cache size along with its 16-byte lines and two-way set associativity deliver the same 90 percent hit rate as a 128K-byte, direct-mapped cache with 4-byte lines, but with less than 10 percent of the hardware.

With prefetching, the instruction cache's hit rate can exceed 96 percent.

Prefetching brings the next 16 bytes of memory into the instruction cache, in anticipation of a CPU request. Because prefetching happens concurrently with other CPU and CAMMU operations, this mechanism can deliver a 100 percent hit rate for bursts of in-line code sequences.

Hit-rate and miss-replacement concepts are relatively straightforward for read accesses. The need to update main memory makes write accesses somewhat more complex. Clipper supports the two prevalent mainframe-type caching strategies—write through and copy back.

Under a write-through strategy, main memory is updated each time the cache is altered. Hence, main memory and the caches always contain the same data, ensuring consistency. Unfortunately, write through doubles the cache access time and consumes main-memory bus bandwidth.

Clipper also supports a copy-back strategy. Here, memory is updated only when a line that has been modified in the cache must be overwritten. Only then is the line copied back to main memory before being overwritten. Data consistency during copy-back caching is assured by a CAMMU's bus-watch hardware. This guards against stale data by fulfilling bus master-read requests from the cache instead of from main memory. CAMMU control-register bits and bus-cycle type manage the bus-watch operation.

Clipper's caches are closely tied to their on-chip MMUs and their translation

lookaside buffers (TLBs). In brief, the CPU generates 32-bit virtual addresses that the MMU/TLB translates into real addresses. The caching mechanism compares these real addresses with addresses stored in the cache. Upon a match, the word associated with the internal address is returned to the CPU.

Pipelining

Pipelining in the CPU has three phases. Parallel and concurrent operations take place in each phase. In order of occurrence, the three phases are fetch, decode, and execute (see figure 8). The execute phase supports more concurrent operations than either of the others, in essence another level of pipelining.

In the first phase, instructions from the cache or from the macroinstruction unit are brought into the CPU's instruction buffer. This buffer holds two words, or up to four instructions.

Next, instructions are decoded into resource requests. In response to these requests, resource management logic makes allocations using its table of busy resources. This resource scoreboard keeps tabs on the status of currently executing instructions and on which of these are using particular resources. This detailed tracking lets the CPU restart instructions that have caused page faults and continue executing instructions after interrupts and traps. Therefore (unlike software-managed pipelines), programmed instructions, interrupts, and traps do not crash the pipeline.

The pipeline's final phase issues in-

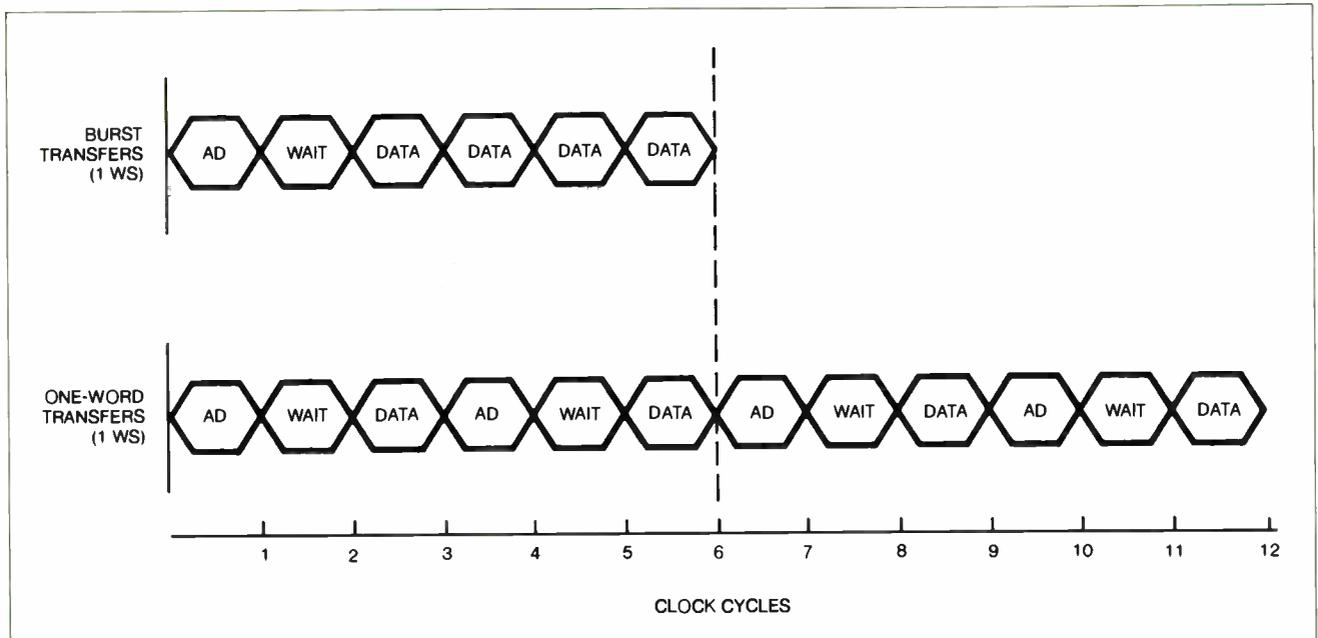


Figure 6: Burst transfers typically halve cache-replacement time over that consumed with conventional microprocessor memory-to-cache coupling.

structions for execution in either the CPU's three-stage integer-execution unit or its FPU. In this phase, up to four successive instructions (three integer and one floating point) can execute simultaneously and are often overlapped.

The first (L) integer-execution stage reads into the L register's operands from the general register file. Immediate operands move directly from the instruction buffer to the L registers via the J register.

The second (A) stage performs arithmetic, logical, and shift operations on L register operands or on the previous operation's intermediate results. Results are stored in the A register.

The third and final (O) stage sends the A register contents to the FPU, to the general register file for storage via the bypass loop as feedback to the A stage, or to the data CAMMU. The bypass loop immediately feeds back to the next instruction intermediate results of multi-instruction calculations. The bypass loop's feedback action renders pipeline flushing, and its consequent program complications and performance degradation, unnecessary. Figure 9 diagrams the interaction among the major functional blocks in the CPU/FPU.

The load/store architecture lets only arithmetic and logical instructions operate on registers. This eliminates the need for an address pipeline or even separate calculation phases for effective addresses. Instructions requiring an effective-address calculation simply make one pass through the integer-execution unit's

continued

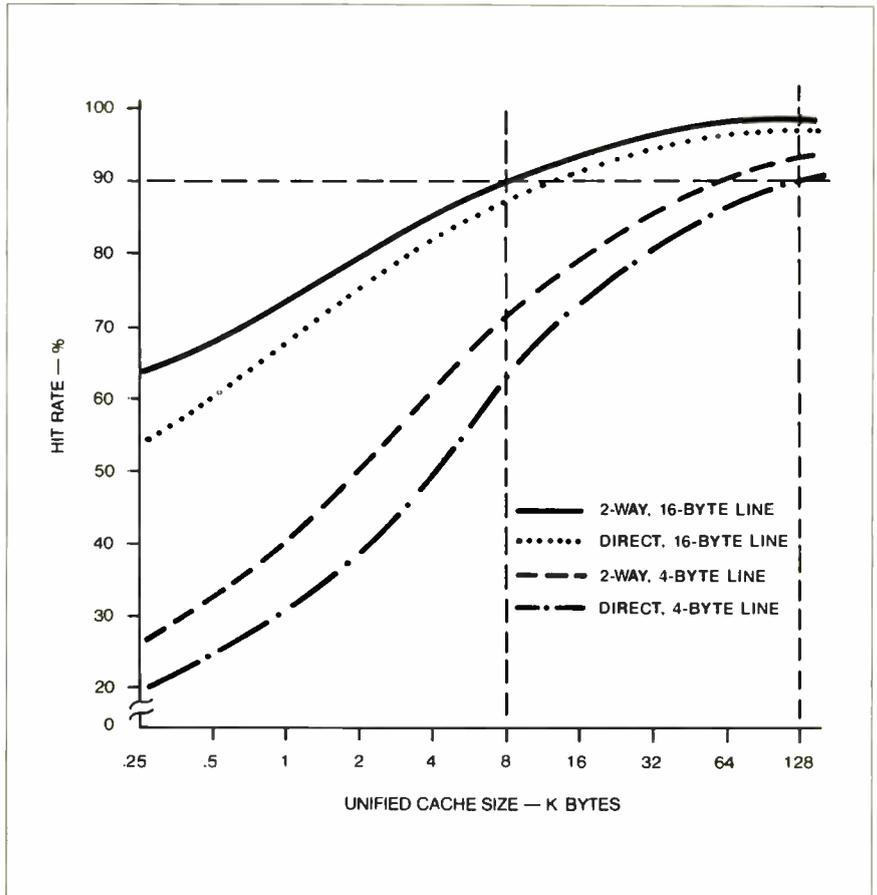


Figure 7: Cache hit rates increase with the line size, associativity, and cache size in rather complex relationships. Two-way set-associative units with a 16-byte line average 90 percent hit rates at only 8K bytes; direct-mapped caches with 4-byte lines require 128K bytes to approach the same 90 percent.

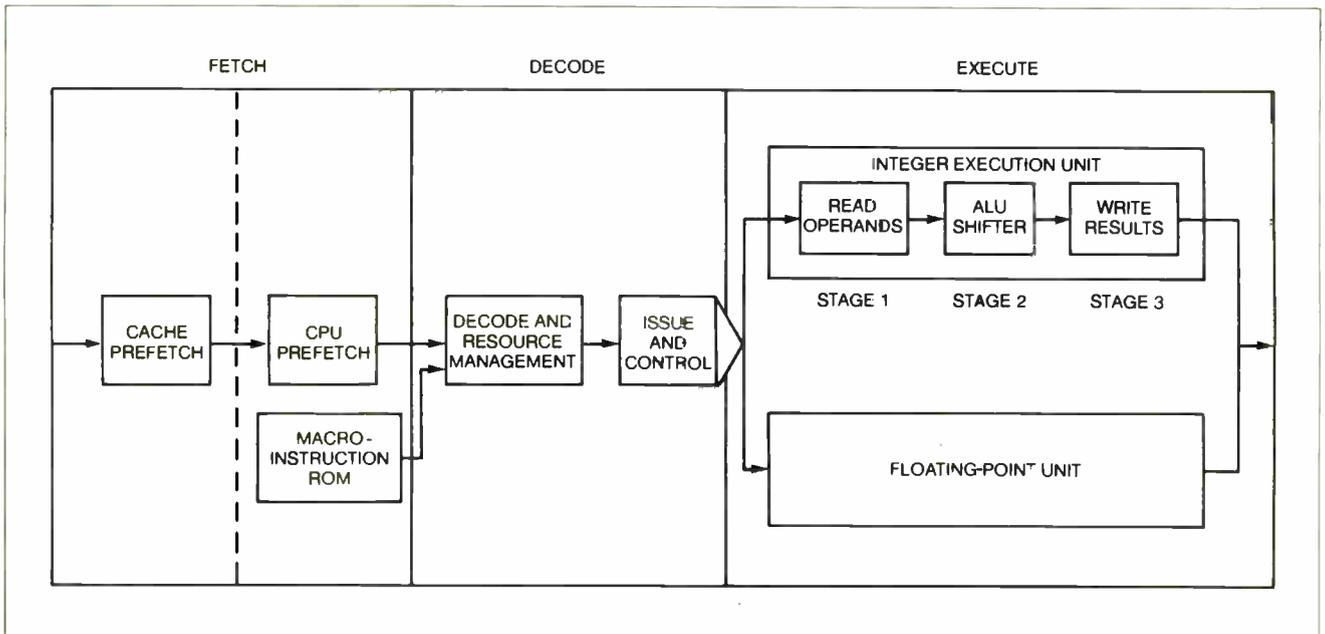


Figure 8: Pipelining relies on hardware-resource and feedback management to oversee operations in its three phases. The throughput is enhanced by overlapping the phases and by simultaneous operations within each phase.

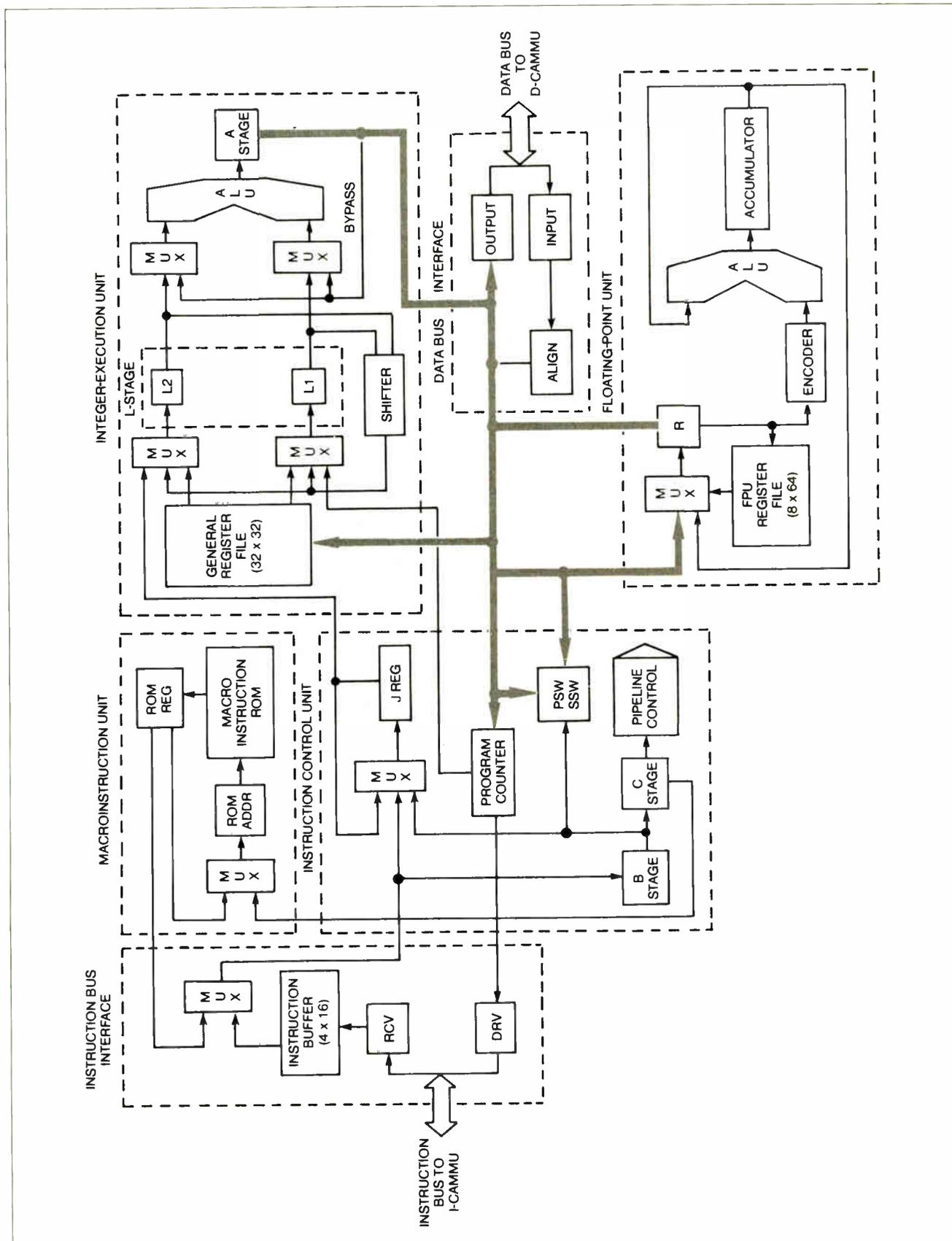


Figure 9: The CPU is essentially a three-stage machine, with three phases of integer execution and a separate but concurrent floating-point unit.



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ALU, which in these cases has no arithmetic or logical function to perform and hence is free for computing the address.

Memory Management

Clipper's virtual address space is a straightforward, nonsegmented linear 4-gigabyte (2^{32} -byte) space. Clipper creates three separate real address spaces via a 3-bit system tag. These spaces contain main memory, boot ROM, and I/O, which is memory-mapped. Also, internal operating modes create up to four instantaneous virtual address spaces.

For multiprogramming (multitasking or multiuser operation), Clipper provides 1 million 4K-byte pages of virtual address space—corresponding to its 32-bit addressing hardware. Similarly, the real address space (defined by the amount of physical DRAM-based memory actually in place) is divided into 4K-byte page frames.

The 4K-byte size has distinct advantages over smaller pages: higher TLB hit rate; faster I/O transfers, because 4K bytes is an efficient unit for disk transfers; and access of larger physical-address cache concurrently with address translation. Most important, it allows translating virtual to real memory addresses (mapping) with only two-level page tables (see figure 10).

Here, each process owns a unique collection of page tables that contains its map and thereby defines its address space. The base level is a one-page table directory containing 1024 entries. Each entry pinpoints a unique page table. In turn, page tables are also one page long and contain page pointers.

Finally, each CAMMU contains two page directory origin registers. One points to the PDO base for the supervisor-mode program (operating system); the other is for the currently executing

process. For context switching, upon a process swap, the operating system simply changes the user PDO, and the new user has a unique address space. The data and instruction CAMMUs, each with two PDOs, generate four memory maps, which in turn create four possible simultaneously active address spaces: supervisor and user spaces for instructions and data alike.

To save overhead on page-table lookups, the CAMMUs cache address translations of 128 frequently used pages in TLBs. Concurrently with cache access in its CAMMU, the TLB is searched. Hence, accesses to a directory in memory or a page table are made only upon TLB misses.

Processes can share pages by simply putting entries for the same real-page frame in each process-page table. The supervisor can access user pages similarly. Also, the supervisor can use a user PDO for its operand's addresses and thereby gain fast access to the entire user address space.

Demand Paging

Clipper's architecture includes four key features in support of demand-paged virtual memory. A fault bit in each page-table entry monitors for the CAMMU the page's presence in main memory. Also, CAMMUs can activate a dedicated-page fault trap upon attempting to access an absent page. And, in the face of a page fault, the instruction being attempted can be aborted and reexecuted or resumed after the OS has loaded the missing page.

Finally, referenced and dirty bits in the page-table entries help choose the best candidate for a newly swapped-in page to replace. The R bit indicates to the OS how recently its page has been used. Thereby, the OS has grist for a page-replacement algorithm based on usage. The D bit indicates whether or not a main-memory page has been modified. If it has, upon replacement it must be written back onto the disk. If it has not, the OS can discard it.

Notwithstanding the new features Clipper brings to microprocessors, software compatibility is proving to be little problem. In our view, the preponderance of software for 32-bit microprocessors is being written in high-level languages. The CLIX operating system, derived from the UNIX System V Release 3.0 operating system, and optimizing compilers for popular programming languages promise a relatively simple port of most existing and future programs. For developing proprietary applications, Clipper comes with a complete set of software-development utilities, including interactive debuggers and simulators. ■

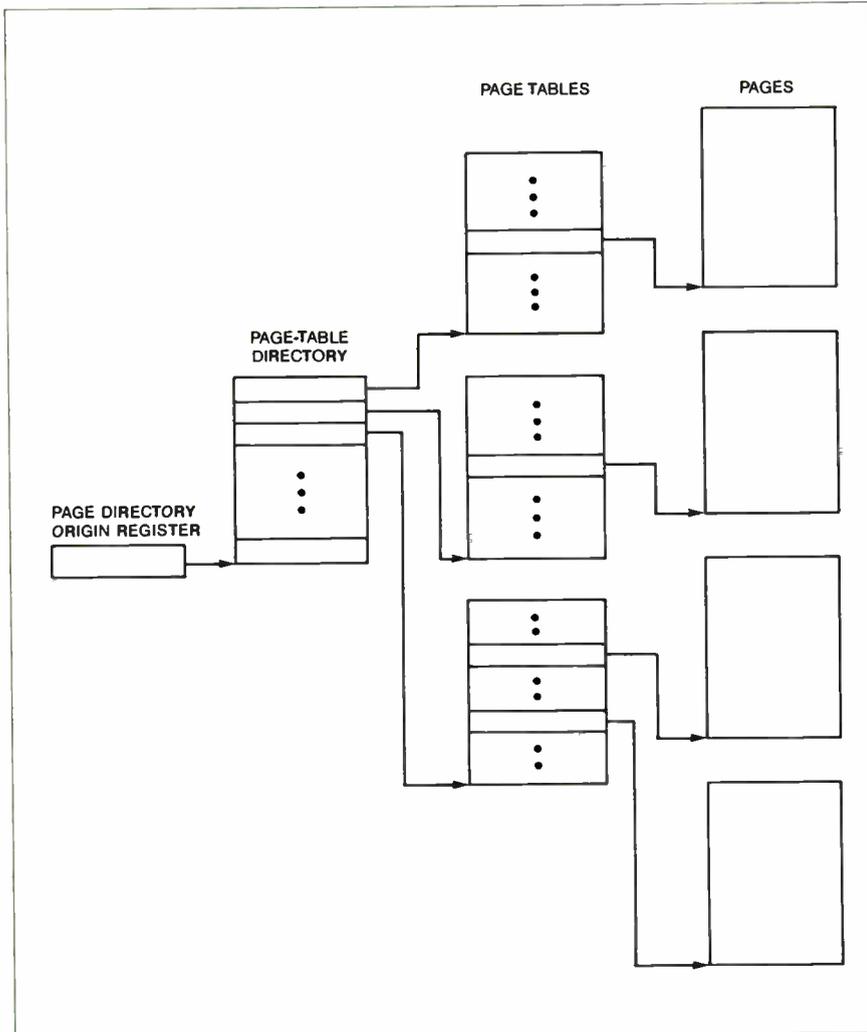


Figure 10: Virtual-to-real address translation proceeds quickly under the two-level system that moves from a 1024-entry page-table directory to one-page tables to the pages themselves.

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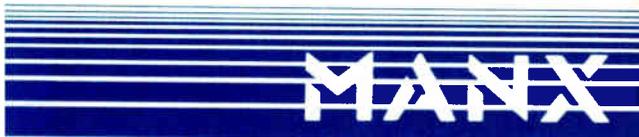
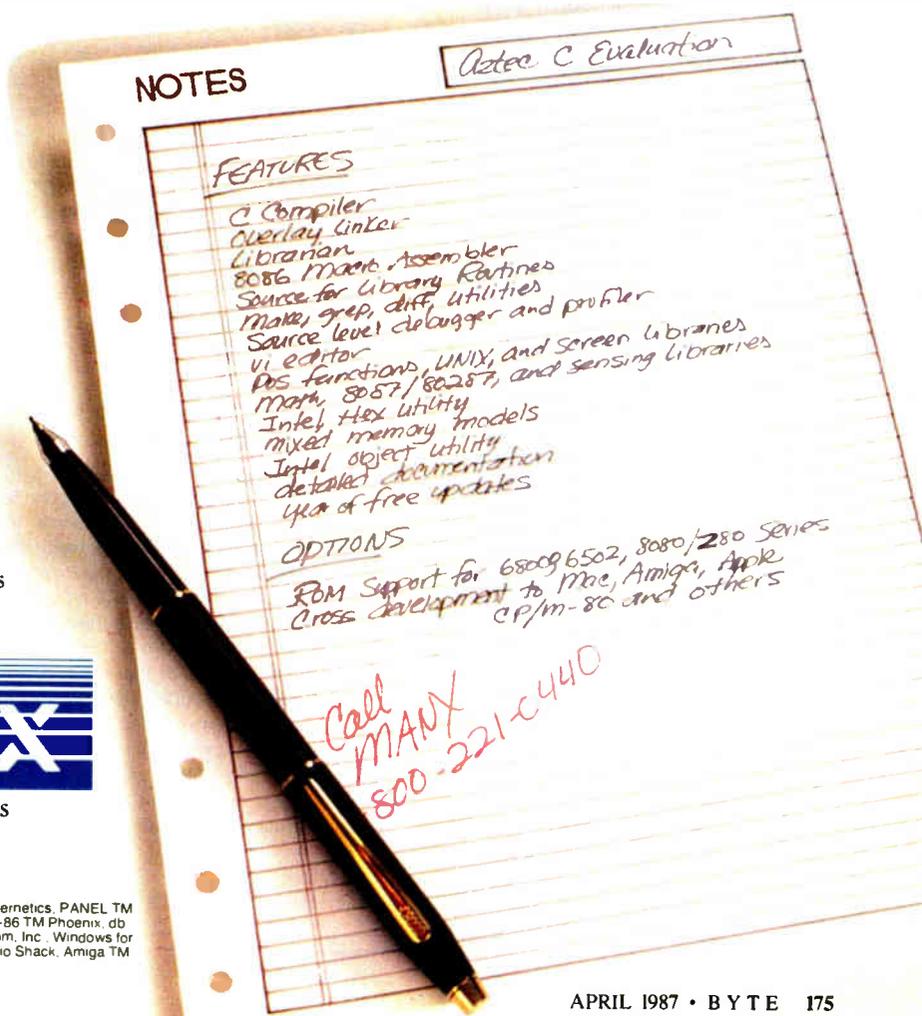
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Stack Machines and Compiler Design

*The Novix CPU's FORTH instruction set
and the design of a C compiler*

Daniel L. Miller

ONE OF THE MOST UNUSUAL instruction set strategies extant today finds a derivative of the FORTH language functioning as the instruction set of the Novix NC4016/6016 series microprocessors. The Novix processor, called a stack machine, uses a stack extensively for temporary data storage and execution of all operations on the data stored there. This extensive use of stacks has potential in the creation of efficient high-level language compilers.

The RISC-like architecture of the Novix CPUs provides internal parallel instruction execution over multiple data paths. Parallel execution results from compacting instructions, a technique that further enhances the potential for building more efficient compilers.

This article examines the Novix instruction set and its use in producing an efficient C compiler based on the time-tested Small-C compiler originally written by Ron Cain. In addition to bringing C to the Novix CPUs, creating this compiler—which outputs FORTH as intermediate code—gives programmers a way to build FORTH-executable files from C source code and interactively debug C programs using FORTH.

The Novix NC4016/6016

The new microprocessor from Novix Inc. (Cupertino, CA) directly executes a stack machine code similar to the intermediate stack code produced by recursive descent compilers. The 3-micron CMOS fabricated NC4016 single-chip computer has a companion extended version called the NC6016. NC4016 development kits with

RAM, ROM, and application notes are available and include an RS-232C interface and a FORTH native-code optimizing compiler. Assembled and tested boards for stand-alone computers and drop-in cards for the IBM PC and dedicated development workstations are available.

Theory of Operation

Most of the NC4016's execution speed comes from hardwiring its instruction set in silicon. The chip is designed for simplicity. It has no pipeline, no microcode sequencer, and no microcode. All instructions except memory accesses execute in one cycle. Novix has minimized address-calculation delays by fixing the address size at 16 bits and simplifying multiple modes of address calculation.

The NC4016 is a stack machine. Stacks facilitate the evaluation of expressions and minimize the control overhead needed to organize data. The stack uses only a few pointer registers to keep track of and access its data.

A stack machine not only uses a stack for temporary data storage but executes all operations on data in the stack. The ALU thus finds all its data in a predefined location and can get that data without an address specification. For example, to add two numbers in memory, the chip first passes the numbers to the stack and then adds them. It places the result on the stack. To pass the result to memory, the chip places the address on the stack, and a store instruction removes both the address and the result from the stack and places the result in memory.

A stack on a fixed-data-type machine is very efficient. A pointer to the end of the stack organizes the access to many data elements on the stack. In addition, no address need be compiled for stack access. For ordinary memory accesses, a source and destination address must be compiled. To access a stack, only one address pointer stored in register 0 is needed.

The Novix chips are modified stack machines. They have an additional hardware return stack to hold subroutine return addresses.

Toward an Efficient C Compiler

C compilers also use stacks to create local variables and to pass run-time parameters among tasks. C breaks tasks up into functions. C permits information hiding within functions to aid transparency, facilitate error checking, and reduce side effects. A C program consists essentially of a series of functions with one beginning function specified as `main()`.

You can easily implement a C-language run-time allocation stack using the NC4016's fast-access memory locations called *pseudoregisters*. You can access data by allocating one of the pseudoregisters to create a pointer into the stack. You can use the stack to file clusters of infor-

continued

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A stack on a fixed-data-type machine is very efficient.

mation called frames. Offsets into the stack are addressed or fetched as a two-part address. A routine to find data first asks which frame and then which element in the frame to fetch. A stack frame is a miniature segmented memory with a two-part address.

Stack frames store information on entry to functions. They permit temporary storage of variables and parameters so that subsequent routines can run and use the stack without interfering with another function's variables, operations, or parameters.

If more than one function is called in turn, each places its set of parameters and

local variables in a separate frame on the stack. The last executed function's parameters and variables will be on the top of the stack and will be removed when the function finishes. A run-time stack thus allows reentrant code for subroutine calls. This is an especially important feature of C programs running in multitasking environments.

Here's how the run-time stack for a compiled C program is organized. The C compiler translates a program's expressions. A C program at run time evaluates its expressions, which are placed on the run-time stack, and also puts local variables on the stack. Because the NC4016's hardware data-stack size is 256 elements (you can extend this with simple support circuitry), the elements are streamed at high speed to a software-controlled C stack in memory. Fast memory-access pseudoregisters store the stack-frame pointers. The NC4016 instruction set pseudoregister operations

support this, allowing high-speed software stack implementation. Since instructions execute at the clock speed, use of the pseudoregister instructions enables microcode-like performance of custom C run-time stack instruction sequences.

Parallel Instruction Execution

The NC4016 instruction set is subdivided into six instruction classes with each bit of chip real estate devoted to controlling a hardware operation. Like horizontally microcoded bit-slice architecture instructions, multiple operations can be compacted and coded within a single op code to execute in parallel. A separate bus exists for the data stack, return stack, and memory and address lines. This introduces a local parallelism into the program flow, increases execution efficiency, and is often called concurrent instruction field execution. For example, the op code 147348 (8 I@ ;) simultaneously references all four address spaces. It fetches a value from the input register, pushes it onto the data stack, and forces a subroutine return, which pops the return address from the return stack and fetches the next instruction.

The NC4016 has 17 user-accessible word-wide registers. These include the first and second elements of the data stack, the return stack pointer, the return and data stack registers, the program counter, a multiplier and divisor temporary-storage register, a square-root temporary-storage register, and port-control registers.

The NC4016's six classes of instructions include Call, Branch, Math (ALU), Internal Reference, Local Reference, and Literal Reference (see figure 1). The upper 4 bits of an instruction's field determine its class. Because subroutines are so important, 2 bits in each instruction are reserved to flag the hardware. When reset, bit 15 forces a hardware subroutine call. The remainder of the field contains the call-instruction address. The memory range of called subroutines is 32K words (64K bytes).

When set, bit 5 in the instruction field forces a hardware subroutine return. The return address is popped from a dedicated hardware stack and placed in the program-counter register. Thus, subroutine calls and returns take very little time—two cycles total or, if the return bit can be piggybacked on the preceding instruction, one clock cycle total.

You can directly address the low 32 words of memory using address bits in the instruction field. These 32 memory locations can be treated as off-chip registers and accessed in two machine cycles. A compiler can allocate storage in these

continued

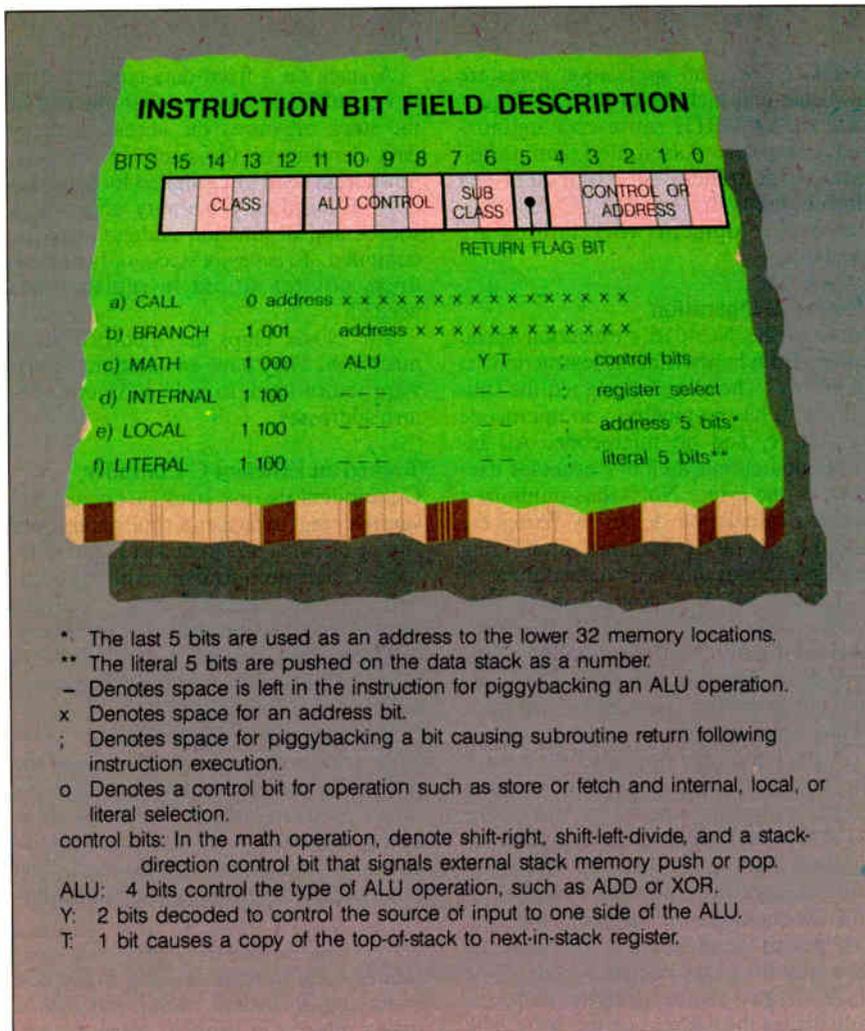


Figure 1: Each 16-bit Novix instruction has a class and an instruction field. This bit-field description shows all the critical fields.



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Table 1: The 40 one-word FORTH primitives in the Novix NC4016 instruction set.

Instructions Corresponding to Single FORTH Words:

Abbreviation	Operation
Memory Access	
Fetch	Fetch value at memory address pointed to by top of stack. The common FORTH abbreviation for this is @.
Store	Store the value of the second stack element in the address pointed to by the top stack element. The common FORTH abbreviation for this is '!', which should not be misread as factorial.
nn@	Fetch from pseudoregister
nn!	Store to pseudoregister
l@	Fetch from internal register
l!	Store to internal register
n!	Store to the 16-bit address given in the next in-line RAM location
n@	Fetch from the 16-bit address given in the next in-line RAM location
nn@	5-bit literal fetch (5-bit address embedded in the op code)
nn!	5-bit literal store
Arithmetic/Logic	
+	Add top two stack elements as 16-bit two's-complement integers
+c	Add with carry; used to chain addition operations to add 32-, 48-, 64-bit, or larger numbers
-	Subtract top of stack from the second stack element as 16-bit two's-complement
-c	Subtract with carry
OR	Bit-by-bit logical OR
AND	Bit-by-bit logical AND
XOR	Bit-by-bit logical XOR
2/	Arithmetic shift of top of stack right 1 bit
2*	Arithmetic left-shift
0<	Replace top of stack number with a true flag if the number is negative or a false flag if the number is positive.
D2/	32-bit-number arithmetic shift-right
D2*	32-bit-number arithmetic shift-left
*	Multiply step
*_	Signed multiply step
*F	Fractional multiply step
/	Divide step
/'	Last divide step
S'	Square-root step
Structure Control	
If	Jump if top of stack is 0
Else	Unconditional jump
#Loop	Jump and decrement loop counter if it is not 0
Times	Sets repeat-instruction counter; executes the following instruction multiple times; the number of times is set by the number on top of the stack
Call	Jump to subroutine (optimized to take only one cycle)
Exit	Return from subroutine (no overhead if piggybacked on preceding instruction, one cycle otherwise)
Stack Manipulation	
Copy	Copy top of stack. The common FORTH abbreviation is DUP (for duplicate)
Drop	Pop the top of stack and discard
Over	Switch the order of the top two stack elements
R>	Pop the top of the return stack to the data stack
R@	Copy the top of the return stack to the data stack
#I	Copy the loop index to the data stack
>R	Pop the top of the data stack to the return stack

pseudoregisters to optimize program execution speed.

The NC4016's Instruction Set

The NC4016 instruction set directly executes 40 one-word FORTH primitives and 123 combinations of FORTH words as single instructions (see tables 1 and 2). You create the code that you need to build an application either from these primitives, such as Store, Fetch, Call, or Return, or build it up from various combinations of these primitive words.

Some common FORTH words are not included in the instruction set but are synthesized from several instructions. Microcode-like performance is still attained. For example, cmFORTH defines a common FORTH word

0=

to test the top of the stack for 0. The 0= instruction is implemented in cmFORTH by using primitives as follows:

: 0= IF 0 EXIT THEN - 1 ;

This assigns 0= as a call to three Novix instructions ((octal) 110021, 157540, 147343). The code for 0= executes in three (IF branches either to 0 or to -1) cycles because of the low overhead for call and return. Now, whenever the source code invokes 0=, a jump to these three instructions is compiled. On other CPUs, a jump to a short subroutine is to be avoided because of the overhead (see table 3). On the NC4016, this is the preferred programming style. Redundant code storage is minimized. Short phrases like 0= are repeatedly referenced, not repeated in-line. This results in tremendous code density.

For example, 20 executions of 0= require memory storage for 20 instructions calling 0= and 3 words for storing 0=s code—23 words total. The clock-cycle overhead is (1 × 20) for the calls and (3 × 20) for 20 executions totaling 60 cycles.

On the 68000 using in-line assembly code, a similar operation to test a flag and branch if it is false or fall through to the code immediately below if it is true is:

TST.W FLAG
BEQ.S False.

The test instruction TST.W is roughly equivalent to 0= in function. It requires 6 bytes of storage if FLAG is a global variable. Twenty repetitions of the code phrase would require 60 words. Therefore, the NC4016 attains a threefold compaction in this simple example. Clock cycle times are 60 clock cycles total for

the NC4016 versus 240 clock cycles total for the 68000.

Code Density and Simplified Compilation

The NC4016 compiler permits stripping small redundant code phrases from memory because of the low cost of subroutine invocation and return. The savings increases with the redundancy in the program flow. The more times a code fragment is reused, the greater the code density compared to in-line code. Any high-level-language overlay like a C compiler can take advantage of the NC4016's underlying "assembly" FORTH code density.

The low overhead for passing parameters via the stack permits extreme code modularity. Instructions for all operations (including operating-system and application code) are stored in respective chunks in memory and jumped to in the appropriate order to create an application. A one- or two-cycle subroutine jump and return permits high code density. Because the 24- to 36-cycle jump-and-return overhead imposed by a normal architecture is avoided, the code is 22 to 34 cycles faster for each subroutine call. For each call to the same subroutine, the overall code storage becomes denser by the length of code in the subroutine. Since the chunks of code are jumped to rather than placed in-line, FORTH systems require less memory space than in-line assembly language code. (For this reason, video-game manufacturers have used FORTH extensively to decrease memory cost.) The NC4016 speeds up subroutine accesses leading to dense code, measured either by the number of bytes accessed or by the time required for code interpretation.

Implicit reference of most of the arithmetic operators that operate on data in the stack achieves some additional increase in code density because these instructions do not need to store addresses for the operands. Other instructions encode short addresses within the instruction (see figure 1) to decrease storage. Finally, some increase in density is achieved by encoding simultaneous control of multiple data paths in one instruction. A single instruction may simultaneously operate the ALU, perform a store or fetch, and cause a subroutine return (see figure 1 and table 2).

Another advantage to compiling to FORTH on the NC4016 is simplicity of compilation. A complicated machine requires a complicated compiler to handle the multiple options and addressing modes. A complex compiler can tame a complicated architecture at the expense

continued

Table 2: The 123 Novix instructions created by combining FORTH primitives.

Instruction Corresponding to Multiple FORTH Words

Data Fetch (16-bit-word data)

@+ @-
 @+c @-c
 @SWAP - @swap -c
 @OR @XOR
 @AND
 DUP @ SWAP nn + (incrementing fetch)
 DUP @ SWAP nn - (decrementing fetch)
 l@! (swap the top of stack and any internal register)

Data Store (16-bit-word data)

COPY STORE
 SWAP OVER STORE nn+ (incrementing store)

Short Literal Fetch (address embedded in the last 5 op code bits)

nn + nn+c
 nn - nn-c
 nn SWAP - nn SWAP -c
 nn OR nn XOR
 nn AND

Full Literal Fetch

n+ n+c
 n- n-c
 n SWAP - n SWAP -c
 n OR n XOR
 n AND

Return Stack

R>Swap R> R>DROP

Stack Manipulation

SWAP DROP DROP COPY
 SWAP - SWAP -c
 OVER + OVER +c
 OVER - OVER -c
 OVER SWAP - OVER SWAP -c
 OVER OR OVER XOR
 OVER AND MODULUS -

All stack-manipulation operations above may be followed by the shift operators *, 2/, or <0 in a single combined op code.

Local Data Fetch

nn @ + nn @ +c
 nn @ - nn @ -c
 nn @ SWAP - nn @ SWAP -c
 nn @ OR nn @ XOR
 nn @ AND

Local Data Store

COPY nn ! COPY nn ! +
 COPY nn ! - COPY nn ! SWAP -
 COPY nn ! OR COPY nn ! XOR
 COPY nn ! AND

Internal Data Fetch

nn i @ + nn l@ -
 nn l@ SWAP - nn l@ SWAP OR
 nn l@ XOR nn l@ AND
 COPY nn l@ + COPY nn l@ -
 COPY nn l@ SWAP - COPY nn l@ OR
 COPY nn l@ XOR COPY nn l@ AND

Internal Data Store

COPY nn !! COPY nn !! +
 COPY nn !! - COPY nn !! SWAP -
 COPY nn !! OR COPY nn !! XOR
 COPY nn !! AND nn l@!

The NC4016 encourages simple modular code by using a simple data type.

of execution speed and code size. But pushing complexity into the compiler doesn't necessarily make it reliable. It makes the compiler/CPU combination obscure to the programmer who must know its conditions, exceptions, bugs, and failures. The programmer has the ultimate responsibility for his or her application's reliability. The best solution from a compiler writer's perspective is a machine with a regular instruction set, a limited number of addressing modes, and few complicated instructions.

The NC4016 chip uses only 4000 gates built from just 16,000 CMOS transistors, a comparatively simple gate array chip that simplifies code compilation. Each field in every instruction specifies a defined data path or controls a simple operation (see figure 1). The FORTH compiler can therefore be simple and short. The public domain cmFORTH compiler written by Chuck Moore is typical. Because it is simple, it has room to include

the cmFORTH language kernel, one-instruction look-back optimization, a meta-compiler for generating custom application ROMs, an in-line assembler, a serial-port manager, and a mechanism to access a host computer's disk drives—all in only 2K words of memory.

The NC4016 also encourages simple modular code by using a simple data type (16-bit integers). Address modes are limited. Instruction length is fixed to eliminate packing and unpacking. The modularity of code encourages breaking up any routine or complex formula into small, understandable chunks. The inputs to each chunk can be tested and an application assembled from small, easily understood, and interactively developed FORTH subroutines (words).

Hardware protection prevents uncontrolled recursion or uncontrolled multiple-subroutine reentry that would use up all available stack space. For example, in a conventional multiuser system, if multiple tasks called multiple nested procedures—each task not knowing what other tasks had piled on the stack—the total available stack could be consumed. FORTH multitasking systems have set aside a separate set of stacks, and a small amount of memory for system variables, for each user or task. A task manager

controls switching the multiple stacks, which may be physically separated by bank switching so a user can access only his or her stack. In the NC4016, the stacks are circular. The stack-pointer register rolls over (like the mileage odometer in a car), and an uncontrolled stack access wipes out only the individual user's stacks and does no damage to any other running task. This eliminates system crashes due to stack underflow and overflow.

Small-C for the NC4016

The limited data-type C-language compiler front end, hosted on an IBM PC development station, outputs FORTH for the NC4016 as its intermediate stack language. This FORTH intermediate code is fed to an optimizing FORTH compiler that functions as the NC4016's native-code assembler. The C-language compiler is based on the Small-C compiler originally written by Ron Cain, with enhancements provided by J. E. Hendrix. Small-C is a C-language subset that includes integer, character, external-integer, and character data types, pointers, and simple arrays. It does not include two-dimensional arrays, arrays of pointers, and structures. [Editor's note: *Small-C for the NC4016 is available as Delta-C from Silicon Composers, 210 California Ave., Suite 1, Palo Alto, CA 94306, (415) 322-8763; \$195. Novix Small-C NS4100 is available from Novix Inc., 19925 Stevens Creek Blvd., Suite 280, Cupertino, CA 95014; \$149. The public-domain cmFORTH compiler is available on BIX and BYTEnet Listings.*]

According to the newsletter *Novix Register* (February 7, 1987), the NC4016 runs the compiled C code Sieve benchmark approximately six times the speed of an IBM PC AT. (Using cmFORTH instead of C, the time is 0.45 second per 10 iterations at 6 MHz. This is three times the speed of the Sieve in C on a VAX 780). When coupled with fast static memory, the Novix chips can run at 8 MHz to further increase performance.

The NC4016 runs at an 8-MHz clock speed with a consistent 8-million-instructions-per-second operation. Because of the compacted parallel field instruction set (see table 2), the effective number of operations per second may be 1.6 times greater for a typical instruction mix.

The translation to FORTH greatly simplifies the code-generating portion of the C compiler, since it does not have to deal with the assembly of the instruction fields or with multiple addressing modes. The FORTH source code is address independent and can be loaded anywhere in memory since it does not use absolute

continued

Table 3: A subroutine call and return operation for three microprocessors and the associated number of clock cycles needed to perform the operation.

Cost of Operation (16-bit operations, in clock cycles)

Sample 16-bit Operations	NC4016 (16-bit)	68010 (a)	8088 (b)
CALL SUBROUTINE and RETURN	1 0 or 1	BSR 18 RTS 16	CALL NEAR 23 20
REGISTER-REGISTER MOVE	1 (c)	8 - > 16(d)	2
REGISTER-MEMORY MOVE	2 to 4	8 - > 16	17 - > 24
DIVIDE unsigned integer	31	108	159 - > 184
MOVE pseudoregister to stack	2	8(e)	15(f)
SUB 16-BIT INTEGER DATA	1	4 - > 16(g)	18 - > 25
ADD 16-BIT INTEGER DATA	1	4 - > 16	18 - > 25
BRANCH CONDITIONAL	1	6 - > 10(h)	4 or 16(h)
BRANCH ALWAYS	1	10	15

(a) *M68000 Programmer's Reference Manual*, 4th ed, Motorola. The range of time is because time varies with address mode.

(b) *iAPX 86/88 User's Manual Programmer's Reference*, Intel, May 1983.

** Move one-word-size register. Decreases to four for each subsequent register transfer.

(c) Used to access the external control ports.

(d) The range includes the variation in effective address source and/or destination calculation due to the various addressing modes.

(e) Move.W Dn, - (A7) pushes a register to top of stack.

(f) Push register to staD].

(g) SUB.W <EA>, Dn Destination register subtract.

(h) The smaller time is if the branch is not taken.



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Listing 1: A Small-C source-code fragment.

```
sflags(i,v) int i,v; {
    int j,x;
    j = flgs[i>>4];
    j = i&15;
    x = 1<<j;
    if (v) flgs[i>>4] := x;
    else flgs[i>>4] &= (x);
}
```

references, only named variables. The FORTH compiler, not the C compiler, assigns the absolute addresses required.

Listings 1 and 2 show examples of Small-C source code and the FORTH intermediate code generated by the Small-C compiler that in turn can be compiled by cmFORTH. In listing 1, the procedure sflags(i,v) has two arguments and declares two local variables. The C stack frame viewed while sflags is running would look like figure 2. A separate stack (the FORTH return stack) holds the pointer to the calling routine's C stack

Listing 2: The FORTH intermediate code corresponding to the C source code in listing 1.

```
: sflags RECURSIVE
  *csp @ >R
  2 #params      2 #locals
  4 ]local @ 15 AND
  2 ]local !
  1 2 ]local @ <<
  1 ]local !
  3 ]local @
  IF   flgs      4 ]local @      4 >> + DUP @      1 ]local @ AND SWAP !
  THEN
  R> *csp ! ;
```

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pointer. In listing 2, RECURSIVE marks the function as being able to call itself, and *csp @ >R pushes the calling function's C stack-frame pointer onto the return stack. 2 #params and 2 #locals push the parameters onto the C stack and allocate local variables. At the end of the function, R > *csp ! restores the C stack frame of the caller.

These code sequences constitute the function-calling overhead. Within the listing 1 code fragment is the C assignment statement $x = 1 < j$. Its FORTH translation is

```

1      (load the constant 1 onto
      the stack)
2 ]local @ (load the value of j onto the
      stack)
<<      (shift each bit in j one
      place to the left)
1 ]local ! (store the result into x)
    
```

Similarly, the C code while ($x=z$) { doIt(); } translates to FORTH as

```

BEGIN JSR UNTIL :SUBR X
@ Z @ = IF DOIT DROP 0 EXIT THEN
1 EXIT
:SUBR
    
```

This basic structure in pseudocode is
indefinite loop:
BEGIN jump-to-subroutine UNTIL
subroutine: TEST DOIT EXIT?

The subroutine is inside an indefinite loop. It contains the test condition and the code to be executed while the condition is true. Failing the test exits the subroutine and sets a flag that halts the loop. The definition of the subroutine pair is interesting, since it creates a labeled goto statement with automatic return not provided for in the usual structured FORTH environment. The subroutines :subr and ;subr are defined and the source code is included in the small run-time macro-instruction FORTH library that heads each compiled file. This library of several commonly used routines is compiled into low memory when the translated C code is loaded. These macroinstructions save space, since you can call the frequently needed macros repeatedly without speed penalty, and they need not be repeated inline in the code.

Conclusion

Implementing a C compiler on the Novix chip had the positive side effects of code relocatability, interactive debugging, and portability. The FORTH intermediate code does not have to be loaded at a certain location. Memory locations are referred to by named variables and constants. The FORTH source is a unique

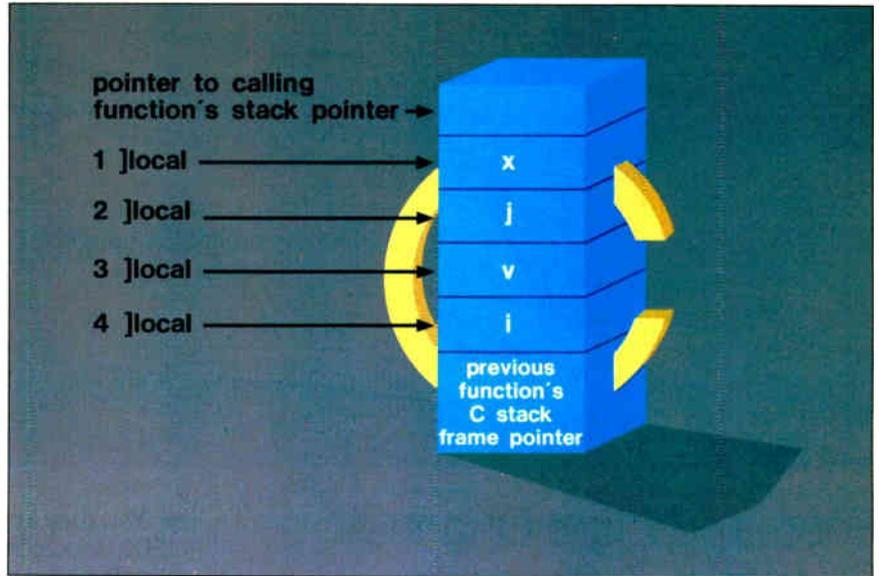


Figure 2: The C stack frame for the code fragment shown in listing 1.

nonbound assembly code for the Novix processor. Library modules, in high-level FORTH code, can be called and compiled almost instantaneously due to the chip's speed. Libraries of C-translated-to-FORTH code can be brought in by passing the code through the FORTH compiler/optimizing assembler, which then assumes the functions of a traditional loader and linker. The FORTH compiler/optimizing assembler is also interactive. Input from the keyboard or files is immediately executed and can be immediately debugged. A C function can be compiled independently to the FORTH stack language. You can test the translated code by using the interactive FORTH system to inspect or set the variables and the parameters.

The Kernighan and Ritchie C standard is widely ported. Translation to FORTH intermediate code adds an additional layer of portability at the FORTH level. The translated code can be run on any machine hosting a compatible FORTH compiler. A FORTH language can be implemented on a new machine, providing an additional pathway of C-language portability at the FORTH intermediary level.

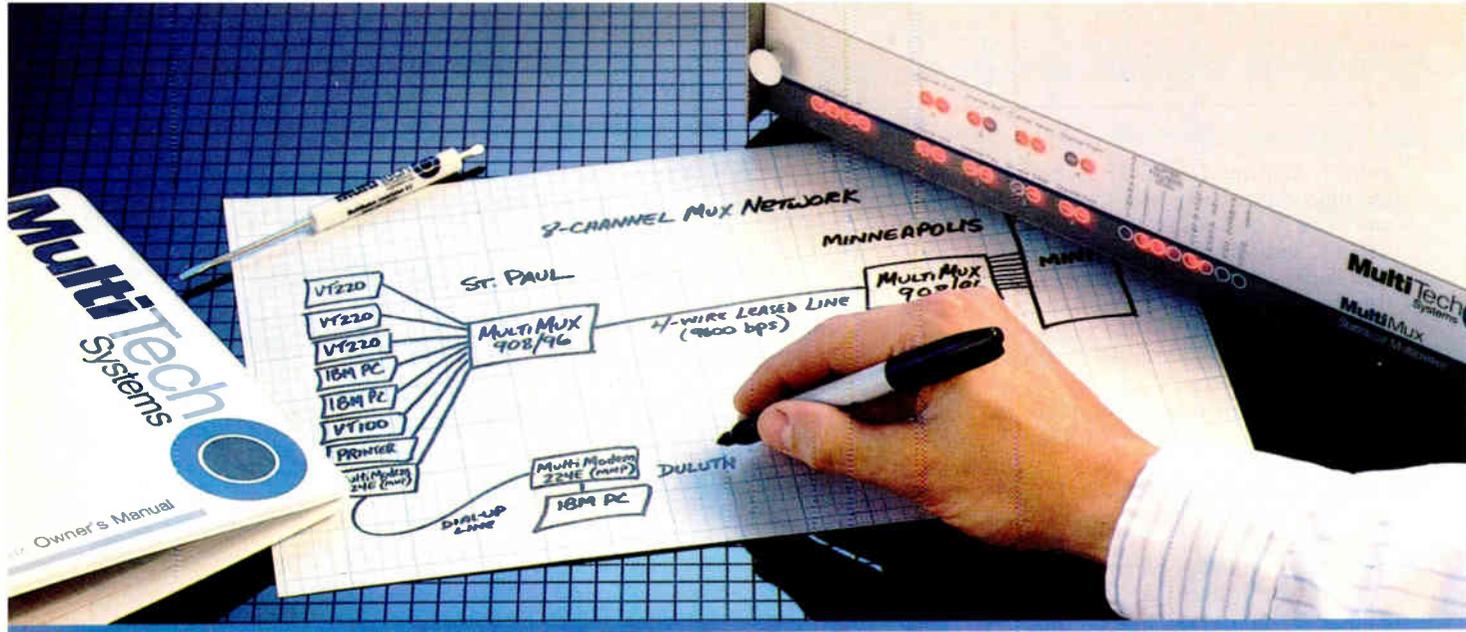
An extension of the NC4016 series, the NC6016, is in the final design stage and is of interest to future compiler writers because it includes supervisor and user-space protection; 16-megabyte segmented address range and segments for program, data, and local memory space; and byte-addressing operators. The instruction set is more regular than the NC4016, allowing easier code generation. A window of 32 memory locations with two-clock access can be slid anywhere in memory and used to speed pa-

rameter passing between functions and facilitate stack frames.

The Novix chips offer flexibility and, with the Small-C language translator, familiarity to C programmers. There is a synergy in the combination of the Novix hardware, optimizing FORTH assembler/compiler, and C-language compiler. The applications will be interesting. ■

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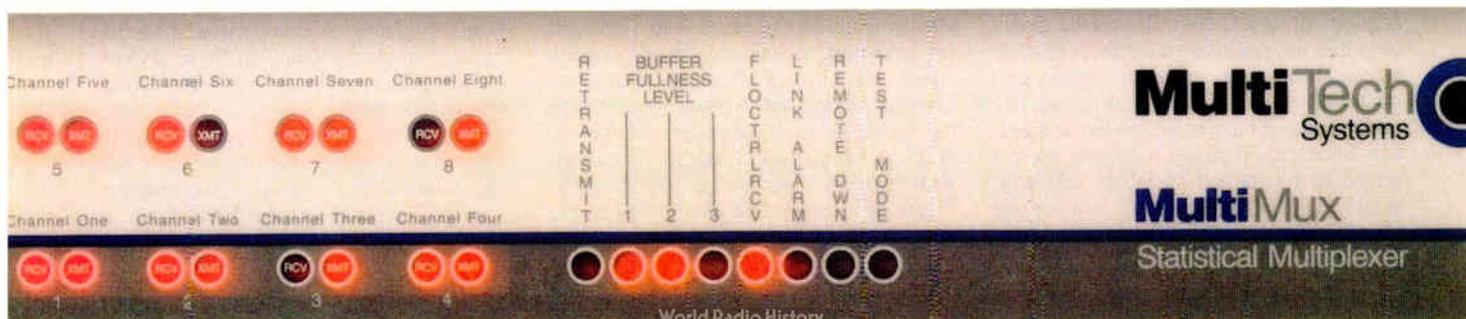
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The WISC Concept

A proposal for a writable instruction set computer

Phil Koopman

THE TRADITIONAL COMPLEX instruction set computer architecture with its large, complicated instruction set has become the mainstay of the microprocessor industry. Recently, however, proponents of the reduced instruction set computer architecture have made the controversial claim that RISC architectures can execute programs more quickly than CISC machines. Before you decide which side of the line you're on, I'd like to present an alternative computer architecture that combines elements of both RISC and CISC philosophies to produce an interesting, streamlined, flexible, and potentially fast machine.

My proposed architecture is called WISC, for writable instruction set computer. My purpose is not to show that either the RISC or CISC approach is somehow wrong, but rather to introduce an alternative that blends RISC and CISC concepts into a simple but powerful architecture.

First, I want to look at the key ideas from the RISC and CISC concepts. Then I can select the best ideas for the proposed WISC architecture. Finally, I will combine these ideas to define the WISC architecture and consider an overview design for a generic WISC machine.

Key RISC Concepts

RISC systems are based on the concept of optimizing the few instructions that are used the most and eliminating infrequently used instructions to reduce hardware complexity and increase hardware speed. I will look at the key RISC concepts, examine their strong or weak

points, and pick the ones that are most desirable for an alternative architecture.

First, RISC machines must execute all instructions in a single memory cycle. Some authors have referred to this as single-clock-cycle operation, but the real resource limitation is the amount of time required to reference program memory. The idea here is that if a CPU can execute instructions as quickly as they are fetched from memory, maximum system throughput speed will result. Clearly, using as much of the memory bandwidth as is available is a desirable goal for WISC.

RISC machines must use hard-wired control. The intent of using hard-wired control is to allow for fast single-memory-cycle operation of op codes and (when combined with a very small instruction set) reduce the amount of silicon area required for implementation on a single chip.

But it is not clear whether hard-wired control is an absolute requirement. Since a designer can make a small amount of microcode memory extremely fast in relation to large amounts of program memory (while achieving a reasonable cost/performance trade-off), there is no reason why a microcoded processor cannot achieve single-memory-reference-cycle operation for most operations.

As for the chip-area argument, microcoded designs can have fewer gates than hard-wired designs (exclusive of the actual microcode memory). If I wish, I can use the extra silicon area available in a streamlined WISC single-chip implementation for microcode memory.

Next, RISC machines use relatively

few instructions and addressing modes. This concept is a side effect of the need to keep things simple in a hard-wired, single-cycle processor. If a chip can support additional instructions without reducing the clock-cycle speed for basic instructions—as is often the case with microcoded CPUs but usually not with hard-wired CPUs—no real incentive exists to limit the number or types of instructions. Instructions with fancy indirect-address modes or multiple-memory-cycle operation should be supported if the net result is a speed-up of the entire system for an important application program or language run-time environment. So a WISC design should not unnecessarily restrict the number and variety of possible instructions.

RISC processors use a load/store design, which allows "load from memory" and "store to memory" as the only memory-reference instructions. This tends to reduce clock-cycle times by shortening delays in the memory-to-CPU data path and simplifying control logic. It also simplifies restarting after a virtual memory page fault. However, if virtual memory is not being used (as is the case in the vast majority of personal computers today) or if a memory reference can be combined with another operation for a net savings

continued

By day Phil Koopman is a U.S. Navy submariner and engineering duty officer; by night he designs computer hardware, software, and microcode. He can be reached at 20 Cattail Lane, North Kingstown, RI 02852.

*No evidence exists
that a fast computer
requires an architecture
with a difficult
assembly language.*

in time, then no reason exists for restricting the system to a load/store design. Thus, WISC computers should not be limited to a load/store design.

RISC machines use a fixed instruction format. Fixed instruction formats allow simpler decoding of instructions and reduced hard-wired logic. They also minimize the number of microcoded instructions that are wasted on shifting and interpreting op codes and operands.

Making all instructions the same size (e.g., a 16-bit format aligned on even-byte boundaries on a 16-bit machine) makes a lot of sense for simple, fast hardware design. You can argue that compressing variable-length instructions into the smallest space possible speeds program execution by reducing the number of memory accesses. But the trade-offs in unpacking these compressed instructions and formatting them properly for execution might eat up much of the savings with more complex hardware and extra instruction fetching when refilling a pre-fetch pipeline after a branch. Most people seem willing to increase memory space somewhat for faster program execution speeds. So WISC should use a fixed instruction format.

Finally, RISC machines trade off more sophisticated compiler technology for less complex hardware. This argument is based on the assumption that all programming is done in high-level languages that shield the user from the machine. No doubt sophisticated compiler technology can improve the speed of a high-level language program. It remains to be seen whether this speed increase can surpass the capability of an experienced assembly language programmer to handcraft the few lines of code that might break the speed bottleneck for a complex application program. Inasmuch as no evidence exists that a fast computer requires an architecture with a difficult assembly language, WISC should not have features that demand the use of a sophisticated compiler, although it could benefit from such a compiler.

A Major RISC Problem

For all its good, the RISC design has an Achilles' heel. The low semantic content

of each instruction requires a high memory bandwidth, resulting in a sharp memory price/performance trade-off.

Consider the common operation of decrementing the value at a memory location. In a RISC machine this would be accomplished by a load, decrement register, and store using five memory cycles: three for instructions and two for memory data references. An efficient CISC or WISC architecture might support a single decrement instruction that uses only three memory cycles: one for the instruction and two for memory data references. If many commonly required high-level language functions are not supported in a RISC machine, memory access for instructions can create a bottleneck.

Another example is the absolute value operation applied to a value already resident in a CPU register or hardware data stack. In any processor without this function as a built-in primitive, absolute value determination consists of a sign comparison, a conditional branch, and a subtraction (or two's complement). This is a total of three instructions and a possible conditional branch that upsets any instruction pipelining that might exist. If the absolute value function is included in the instruction set, execution requires only one memory reference.

Now you might be thinking, "What about a memory cache? Doesn't that solve the memory bottleneck problem?" But a cache is only a partial solution. First a cache speeds up memory references only on the second and subsequent accesses to a memory location. Thus, the effectiveness of a cache is reduced by compiler optimizations such as unrolling loops. Second, a cache introduces additional system cost and complexity and results in extra delay when encountering a cache "miss" that requires fetching an instruction from memory. Finally, a cache design is often based on the concept of "locality" of programs. This contradicts the current software doctrine of breaking up programs into smaller and smaller procedures and functions for modularity and reusability—or forces greater memory usage by compiling functions and subroutines as in-line code, which further reduces cache effectiveness.

Simply put, it is better to have no memory bottleneck problem than to have a limited memory bandwidth with a cache. Therefore, WISC should be designed to minimize the number of memory references needed to accomplish each function in a high-level program.

To avoid the RISC memory bottleneck problem and achieve high performance, I can borrow some concepts from CISC machines. A CISC machine's CPU has

an extensive and complex instruction set that attempts to support high-level language control and data structures directly. All of today's widely used 16-bit microprocessors are CISC designs.

Borrowing from CISC

Two common CISC traits that might be useful in a WISC design are a minimal semantic gap and the inclusion of as many high-level language-oriented instructions as possible.

The driving force behind the complexity of a CISC machine is the desire to speed up common high-level language operations such as character-string manipulation, pointer maintenance, looping, and array handling. By reducing the so-called semantic gap between the high-level language statements used in a program and the machine-code instructions available on the CISC machine, programs should require fewer memory references, take up less space, and run faster. To handle the very complex instructions that can be used, designers of CISC machines often use microcoded implementations. Likewise, to provide complex instructions while minimizing hardware complexity, WISC should employ a microcoded design.

An unfortunate side effect of complex and comprehensive instruction formats can be an excessive amount of decoding logic or multiple microcycles just to decode an instruction before any real work is done. But this side effect can be reduced by the adoption of a simple fixed instruction format for WISC instructions. Using a fixed instruction format eliminates complex manipulation of instructions to extract the meaning of an op code and its operands, thus reducing hardware requirements and speeding up the processor.

Powerful high-level language-oriented instructions, such as decrementing a memory-location value or string manipulations, can speed up programs significantly by reducing the number of instruction fetches from program memory. The only pitfall is that such instructions must be well suited to high-level languages, or compilers ignore them in favor of synthesizing primitive instruction sequences that do the job exactly. Examples of problem areas include zero-based versus one-based arrays and loop counters, subroutine calling, parameter passing, and list/record data-structure manipulation.

The answer to the semantic mismatch caused by high-level language instructions that don't quite meet high-level language requirements is to customize the processor's instruction set for each language environment. This customization

continued

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64180	199.50	199.50	995.00			500.00	2000.00
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6801,3	199.50	199.50	995.00	149.50	499.50		
6804	199.50	199.50	995.00				
6805	199.50	199.50	995.00				
6809	199.50	199.50	995.00	149.50	499.50		
68c11	199.50	199.50	995.00				
68000,8,10	299.50	299.50	1250.00				
68020		399.50	1500.00			700.00	2500.00
8400/c00	199.50	199.50	995.00				
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8044/51	199.50	199.50	995.00	149.50	499.50		
80515		199.50	995.00				
8080	199.50	199.50	995.00	149.50	499.50		
8085	199.50	199.50	995.00	149.50	499.50		
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would be accomplished in WISC with a writable microprogram memory, sometimes called a writable control store, that employs high-speed RAM to store microcode. Such an arrangement would let the processor's microcoded instruction set be changed as the operating system requires.

Therefore, a WISC goal should be to execute all instructions in a single memory-reference cycle and use 100 percent of available memory bandwidth, except where a microcoded complex instruction clearly results in performance superior to

multiple simple instructions for a particular application or high-level language run-time environment. Of course, instructions involving memory operand access will be longer than a single memory cycle, but they will nonetheless tend to keep the memory productively engaged at all times.

Using Stacks

The WISC architecture should use one final feature to synergistically work with other design aspects to increase speed and decrease complexity of the system:

hardware-implemented push-down last-in/first-out stacks.

The stack concept has proved its value in computers and modern-language implementations that use stacks for implementing subroutine return-address storage or parameter passing. However, these stacks are generally realized as an address register that points to main memory, with perhaps the top few elements of the stack located in special registers. I propose using completely independent high-speed memories to implement two stacks for the WISC architecture. One stack would be primarily for subroutine return-address storage and the other for data storage.

The advantage of a hardware return-address stack is that subroutine calls and returns can be processed at a high speed, with the return address transferred to or from the return stack in parallel with decoding the next instruction. A hardware data stack lets subroutine parameters be passed to subroutines without main-memory accesses in addition to providing for a large amount of scratch work space for storing temporary results. In fact, the underlying structure of modern languages such as Modula-2 seems to presume the existence of a stack of some sort.

In addition to reducing subroutine-call overhead, use of a data stack simplifies (and quickens) the machine's operation by eliminating the need for operand decoding. Since a stack machine implicitly addresses certain elements on the stack relative to the current stack pointer position, the CPU does not suffer any delays while source and destination registers are selected from a large register bank. Furthermore, the instruction bits freed by not needing fields for selecting registers allows the use of a narrow word size (16 bits or less), packing multiple op codes into each program word, or using constants or other values in the same word as an op code, all while maintaining a simple instruction format.

In-line literal values are required in a stack machine only for providing values for variable initialization, arithmetic constants, or branching addresses. These values can either be incorporated into unused instruction bits or placed into a memory cell after the instruction requiring the value. One interesting approach that some stack-oriented processors use is to have two instruction types: one for operations (consisting of an op code with no parameters) and one for subroutine branches (consisting of only an address with a flag indicating an implied op code of a call).

So the WISC design should include

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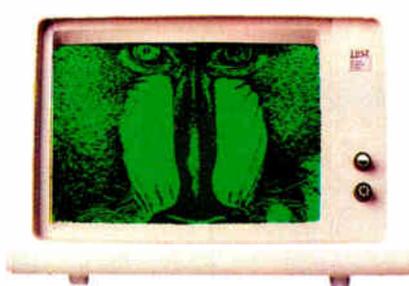
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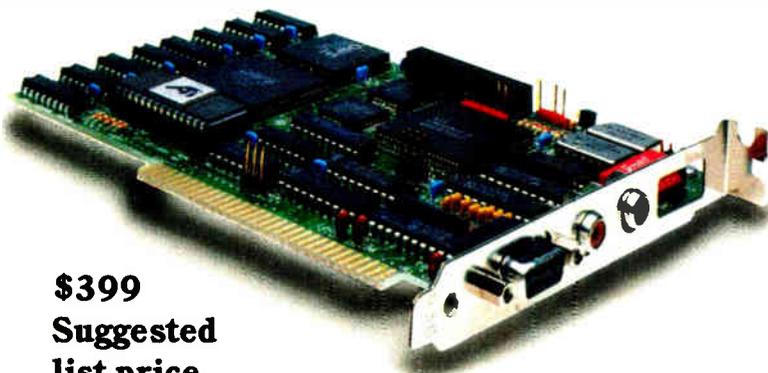
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hardware stacks. The use of hardware stacks will reduce subroutine-call overhead and the complexity and delay associated with operand decoding, since all operands are implicit.

A Generic WISC Computer

Having described the attributes of a WISC computer, I would like to present a generic architecture for WISC implementation. Figure 1 shows a block diagram of one possible format for a WISC computer.

The resources of this generic WISC computer are a data stack, an ALU with a small number of registers (perhaps only

one), a return stack with a bidirectional data path to the program counter for subroutine-call address manipulation, a program memory, and a microcoded controller. All the resources are connected to a central data bus, with access to I/O services through an appropriate interface.

The WISC machine in figure 1 has several interesting aspects. One feature not always found on hardware-based stack designs is that the registers above the ALU can hold the top one or two data-stack elements. These registers allow the use of a single-ported data-stack RAM.

The entire instruction decoding path, from the return-address stack all the way

through to the microinstruction register, is completely independent of the data bus. This independence allows for ALU and data-stack operations on data while instructions are fetched and decoded simultaneously. This structure allows use of nearly 100 percent of the memory bandwidth. An added benefit is that there is no need to implement an instruction prefetch unit; no time is lost flushing an instruction queue when a branch is encountered. In fact, implementing a delayed branch similar to the ones used by some RISC machines can eliminate almost all idle or wasted memory cycles.

The microinstruction register forms a one-stage microinstruction pipeline and eliminates wasted time that would otherwise result from waiting for microprogram memory access in a nonpipelined design. The only drawbacks to this design are that a two-microcycle minimum is imposed on all op codes and that delayed microinstruction branches must be used for condition code testing. However, the small high-speed memory used to implement the microprogram memory and data-stack memory should allow for multiple microcode cycles within each memory-cycle time, essentially eliminating the impact of these drawbacks on system performance.

A design approach for instruction decoding that could greatly simplify the CPU hardware would be to use, for example, an 8-bit op code that directly addresses a word in the microcode memory. This would directly address the first microprogram instruction of a page of microprogram memory; one page of microprogram memory would be allocated to each op code. This would allow complete flexibility in instruction set assignment while using very little instruction decoding logic.

The Past, Present, and Future of WISC

Constructing a hodgepodge of previously successful computer design techniques does not guarantee success. The WISC design criteria presented here represent a careful balance of often conflicting design requirements. That said, I will look at some past and current computers that inspired some of the WISC machine's unusual design features.

The Burroughs B1700, a microcoded machine, had a different instruction set for each language it supported: BASIC, FORTRAN, and COBOL/RPG-II. The tailored instruction set for each language resulted in smaller programs and much faster execution speed than that found on comparable machines of the time. But the complexity of the architecture for vari-

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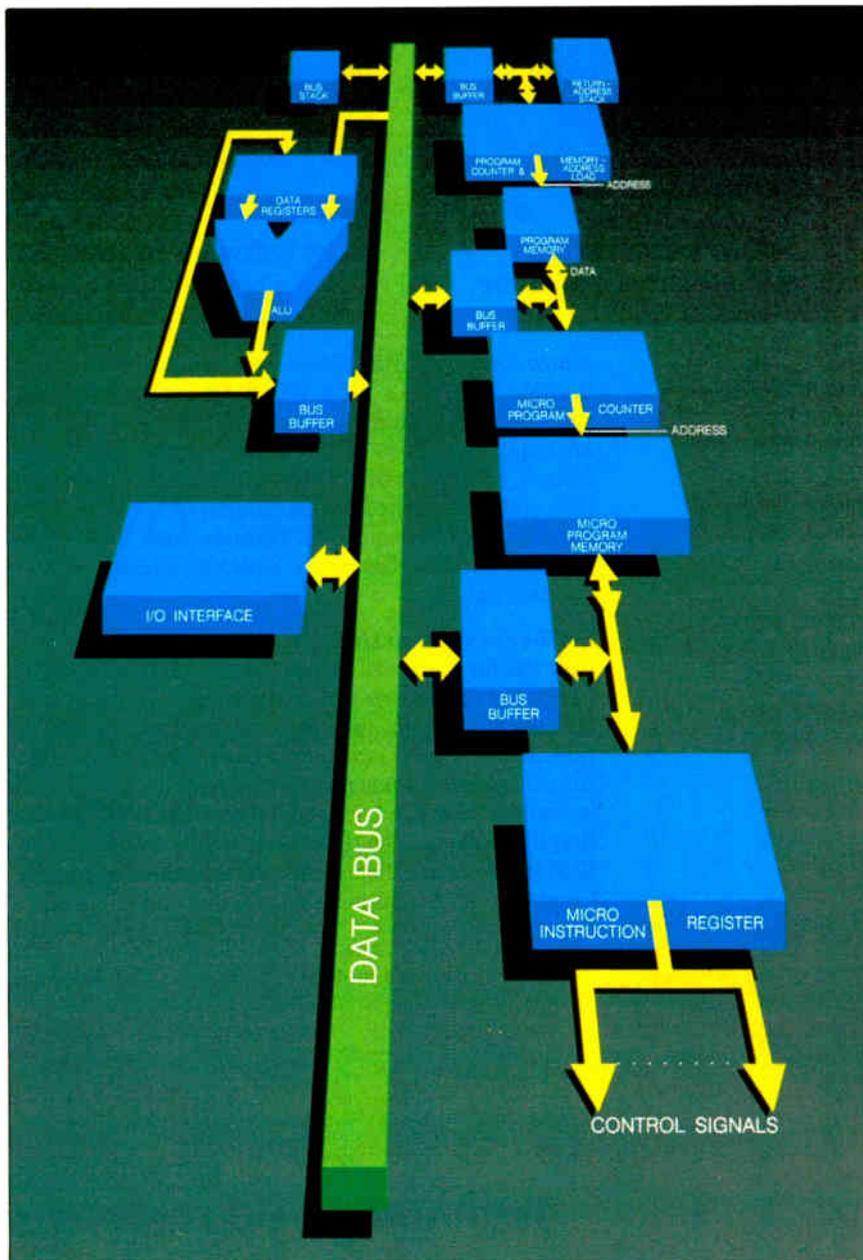


Figure 1: A block diagram of a possible WISC machine implementation.

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As you can see, industry experts project that the gap between dry and canned soups will begin to close by 1990. They also believe mergers will follow.

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Bad news this month comes from TNG (The Noodle Group). By year's end, they project the price of noodles to double—up to eighteen cents a barrel. How will this price hike affect you? A two-cent per can increase on all noodle soups you sell.

Recommended Reading: "Cup or Bowl?"
This in-depth study discusses the habits of the American soup eater. Call and I'll send you a copy.

Sincerely,

Robert Welke

Mr. R. Welke
Director, Canned Soup Council

NUTS

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Spring 1987



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Pecan

Another great favorite in the bakery. And our own superb pecans will satisfy even the most discriminating Southern tastes.

Walnut

Blond English Walnuts are just one of the many varieties available, in the best nutcracking tradition.



Chestnut

Superior varieties from our own plantations in Italy and France. All the best for more than seasonal consumption.



Pistachio

With an unusually subtle and delicate flavor, these perennial favorites will be perfect for either sweet or savory dishes.



able-width operand support made the machine expensive.

The current RISC II and MIPS processors (see "How Much of a RISC?" by Phillip Robinson on page 143) strive to achieve single-memory-cycle execution with the use of fixed instruction formats. Interestingly, the IBM RT PC and the Pyramid 90x computers use hybrid hard-wired/microcoded designs to allow for some complex instructions within a RISC framework.

One early reference to a stack machine was a design for a 1950s ALGOL language-specific processor known as ALCOR. While it was never built, it called for a two-stack machine that would have used one stack for operand storage and another stack for instruction storage.

More recently, the Novix NC4016 chip (see "Stack Machines and Compiler Design" by Daniel L. Miller on page 177) efficiently executes the dual-stack-based FORTH language with a hard-wired RISC architecture. The NC4016 is designed with single-cycle operation in mind and has low procedure-calling overhead due to the use of stacks, but it has a hard-wired instruction set like other RISC processors. Another stack-oriented processor, the MVP Microcoded CPU/

16, combines hardware stacks with writable microprogram memory to allow redefinable instruction sets but is not optimized for single-memory-cycle instruction execution.

While none of the individual design features of WISC are new, I believe that implementing a true WISC machine will lead to discoveries about the nature of modern computer architectures and how to make them better. In the end, designing a more efficient computer architecture will lead to less expensive, more capable computers. ■

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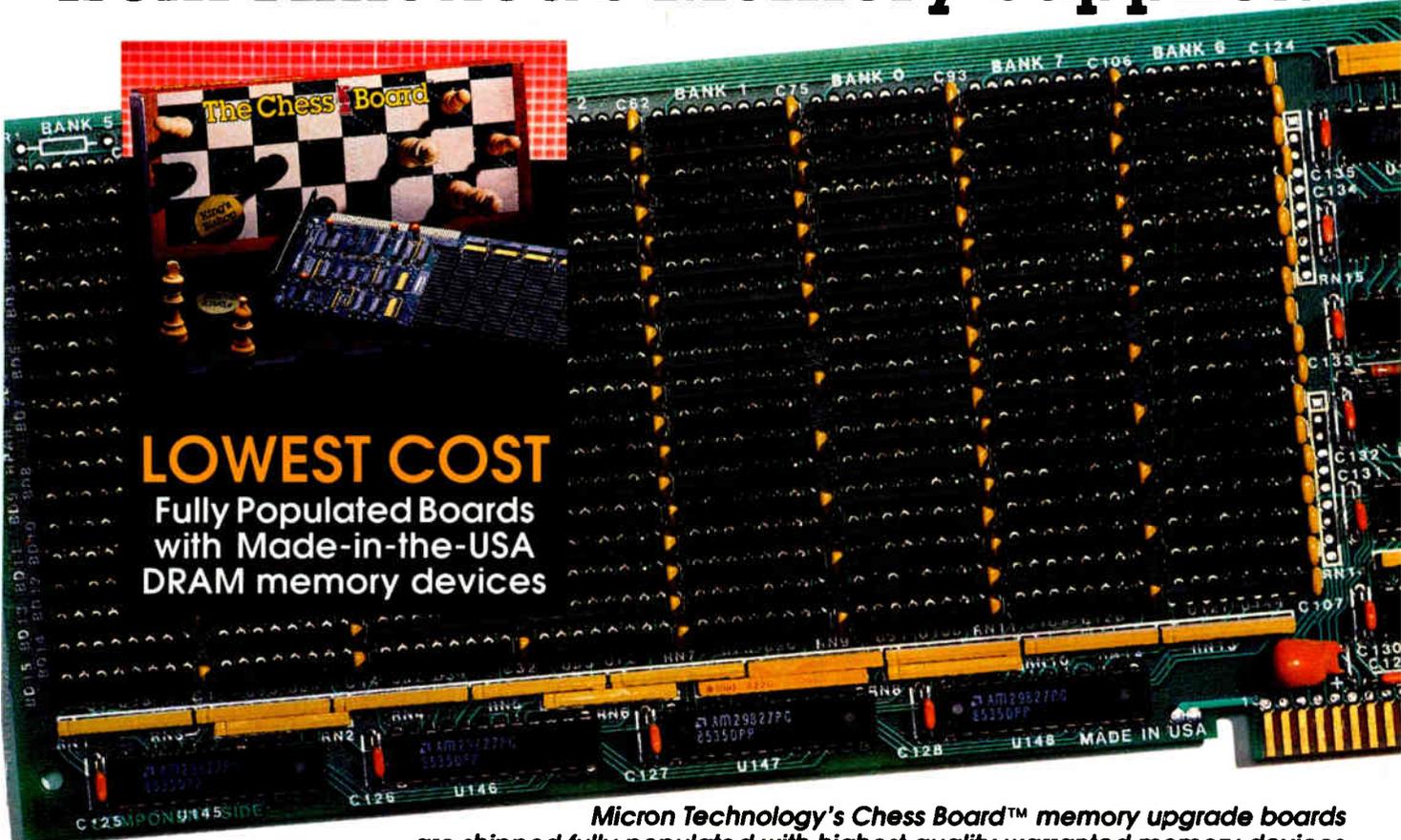
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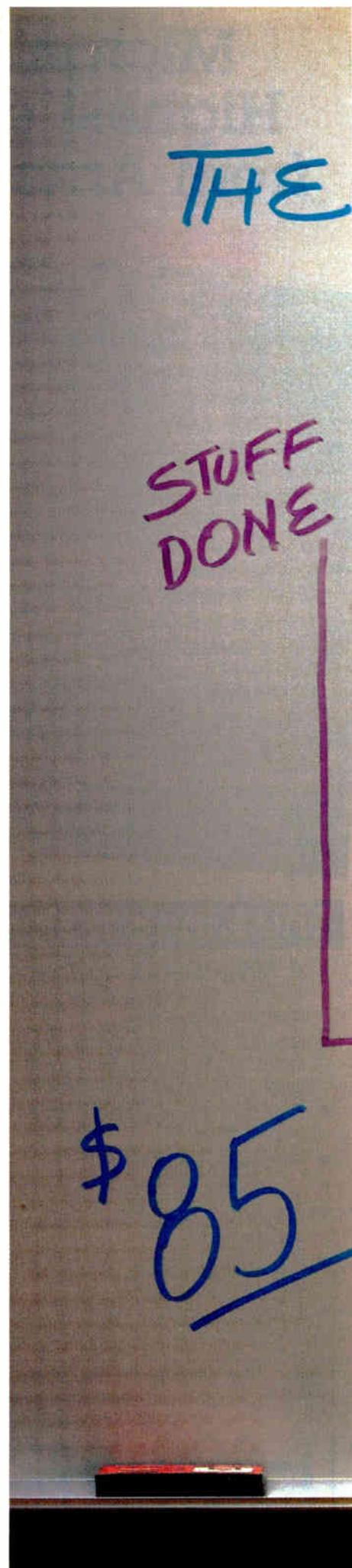
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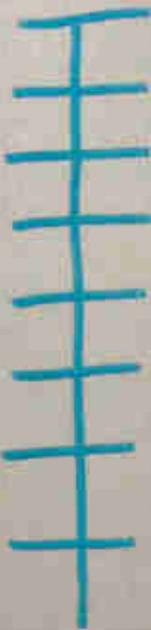
IBM® PC, XT, Portable, AT, COMPAQ® Portable, PLUS, DESKPRO. Two 5.25" double-sided disk drives (hard disk recommended for optimal performance). Minimum of 80K required for RAM-resident portion of Metro. DOS 2.0 or higher. Metro is unprotected and can be removed from memory.

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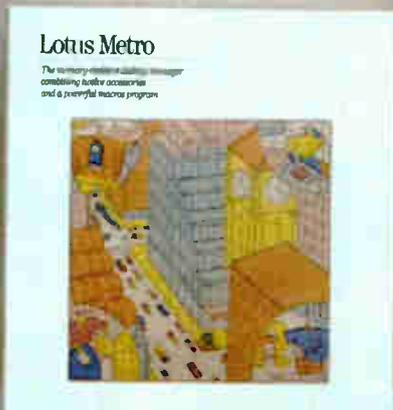
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State of the Art in Dot-Matrix Impact Printers

George A. Stewart and Jane Morrill Tazelaar

BYTE tests 53 *current models ranging in price* *from \$329 to \$2645*

Dot-matrix impact printers have always been economical compared to printers based on daisy-wheel, ink-jet, plotter, laser, and similar technologies. Over the years, they have improved substantially in terms of graphics capabilities, speed, and output quality.

For an up-to-date look at the dot-matrix printer market, we asked 28 companies to send representative models from their printer lines. Our only prerequisites were that the printers be compatible with the IBM PC through a parallel interface and that they be equipped with a tractor-feed mechanism.

We tested the printers' throughput in draft and high-quality modes, sound level, and print quality in text and graphics modes (see figure 1). We also performed benchmark tests and compiled additional information supplied by the companies: general specifications, general features, and convenience features. This information is presented in tables 1 through 4. The text box on page 213 lists the addresses of all the companies whose printers we tested. Figure 2 presents our rankings of the top 10 printers in three application areas: correspondence, high-volume printing, and general personal computer use. (Note: Our tests focused on word processing and graphics. We did not test performance for other uses, such as printing extra-wide spreadsheets.)

Printer Tests

•*Price.* Although price is not a benchmark item, we included it in table 1 to help you judge each printer's price/performance ratio. The price quoted applies to the printers as equipped for our tests—with a parallel interface and a tractor-feed mechanism.

•*Throughput.* Most printer companies rate speed in terms of the maximum characters per second (cps). This figure is useful for comparisons with other similarly ranked units, but it does not give you an accurate figure of a printer's speed on typical text including carriage returns,

blank lines, columns, and form feeds.

To get a more realistic measurement of throughput, we put together a five-page, 300-line, 16,000-character test document based on a BYTE review manuscript. It's typical of routine professional correspondence: single-spaced copy with indented paragraphs, top and bottom margins of approximately 1½ inches, a ragged-right margin, and a left margin of approximately 1¼ inches. The last page contains three simple tables (i.e., text arranged in columns and rows). We ran the test in draft and high-quality modes for all the printers. Output was on standard 8½-by-11-inch office-grade computer paper.

The throughput test results reveal that comparing nominal cps figures is not always a good way to determine the fastest printer. Other factors affecting throughput include the speed of carriage returns, the speed of the paper-advancing mechanism, and the printer's intelligence (its ability to optimize performance by compressing horizontal and vertical spacing into a single continuous motion). Our throughput tests factor in all these elements (see photo 1).

The graphics throughput test was performed on printers with IBM or Epson emulation. First, we printed a series of gray-scale patterns in each of four modes (single density, double density at half speed, double density at full speed, and quad density); next, we ran a graphics stress test consisting of 25 solid black bars at quad density. The graphics test file contained about 72K bytes.

•*Sound level.* During the three throughput tests, we measured the noise produced by the printers using a Radio Shack sound-level meter (model number 33-2050). The meter was set for "A" weighting (corresponding to the sensitiv-

ity of the human hearing system) and slow meter response (to average the noise peaks). For each test the meter was set at ear level in front of and slightly above the printer; the actual printer-to-meter distance was 2 feet. Sound-level ratings are in decibels (dB) above 0 dB, which is defined as a sound-pressure level of .0002 microbars.

For comparison purposes, a sound level of 60 to 70 dB is considered "very noisy" for a private office, rendering telephone conversation difficult, and "noisy" in a general office, according to L. L. Beranek's book *Acoustics* (McGraw-Hill, 1954).

•*Print quality.* The outputs of the three throughput tests were used to evaluate the print quality of each printer. A group of 23 BYTE staff members ranked each print sample for sharpness and uniformity of characters and graphic patterns. No judgment was made on the aesthetic merits of one type font versus another. The results were compiled and each printer was rated according to its average score from the individual scoresheets (see figure 1). [Editor's note: *Four printers could not be tested in time for this review (Genicom 3410.02, Mannesmann Tally MT-490, NEC P5XL, and Newbury Data OSP-3). Those results will appear in a future issue.*]

Specifications

Many of the specifications found in table 2 are self-explanatory. Some of the less obvious include the following:

•*Maximum CPS/Draft and NLQ* give the printer's rated maximum-output rate on a single line in the 10-pitch setting with draft and highest-quality characters, respectively. Compare these numbers

continued

George A. Stewart and Jane Morrill Tazelaar are BYTE technical editors. They can be reached at BYTE, One Phoenix Mill Lane, Peterborough, NH 03458.

with the throughput figures obtained in our tests. Note that not all companies refer to their highest quality as near-letter quality; some call it high quality, and others call it correspondence quality. In this article, the term "NLQ" refers to a printer's highest-quality output, regardless of what the company calls it.

•**Character matrix** is the size of the grid used to define each character in the 10 characters-per-inch NLQ font; the higher the numbers, the more detailed the

character forms can be.

•**Graphic density** shows how many dots a printer can place in one inch, both horizontally and vertically. For comparison purposes, laser-printer density is 300 by 300 dpi; typeset resolution is 1200 by 1200 dpi or higher.

•**Buffer.** Computers are capable of sending data to the printer much faster than it can be printed. To free up the computer during printing, most printers include a memory buffer, which accepts

data from the computer at high speed and then distributes it to the printing mechanism at what is typically a much slower speed. This allows the computer to "think" it has completed its printing task sooner than it actually has. The larger the buffer, the greater the savings of computer time.

Note, however, that the operating system or application running on the computer must be designed to take advantage of buffered printing. In addition, the only time that buffered printing makes a guaranteed difference is when the amount of text to be printed is no larger than the buffer size. For reference in evaluating buffer sizes, one single-spaced page of text will fill approximately 2K bytes of buffer memory.

Specifications related to paper handling will help you decide if a given printer can handle the forms or mailing labels that you intend to use. The chart indicates whether various capabilities are available in either standard or optional form.

•**Maximum characters per line** may be an important specification if you plan to print multicolumn spreadsheets or reports. The maximum number is ordinarily obtained using condensed-pitch characters.

•**Maximum copies** is the company's rating based on no-carbon-required paper; the number indicated includes the original and all copies.

•**Bottom feed** indicates whether the printer has a slot in its underside to allow fanfold paper to feed directly up from the

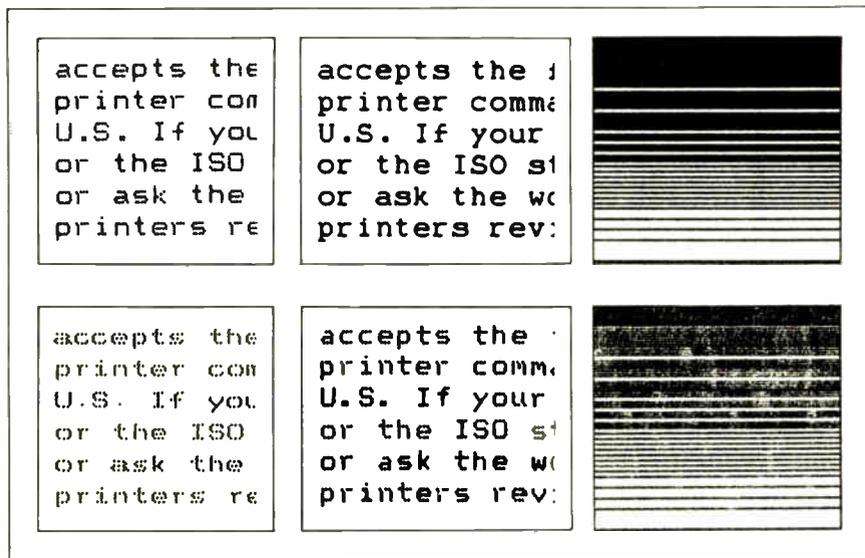


Figure 1: Representative samples of draft, NLQ, and graphics printing. On a scale of 1 to 5 the samples on the top row received a rating of 5 (excellent); those on the bottom received a rating of 1 (unacceptable).

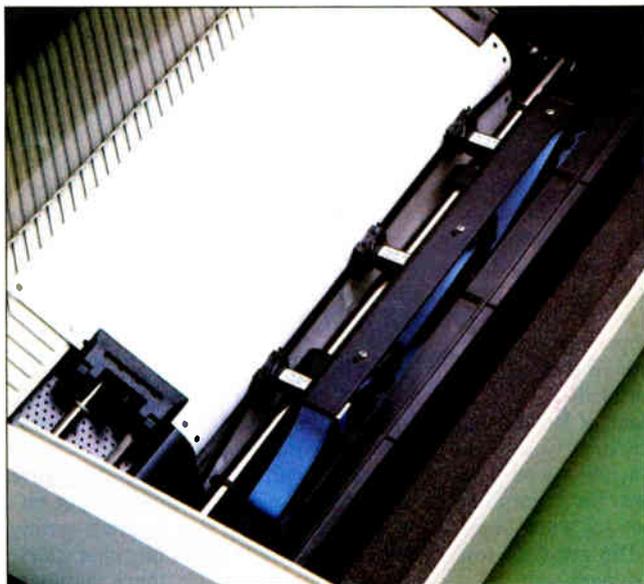


Photo 1: Output Technology's OT-700e uses a three-head design to achieve a maximum speed of 700 cps. The three heads give the greatest advantage for printing on wide forms because all three heads are used. On 8-inch forms, only two of the print heads are used.

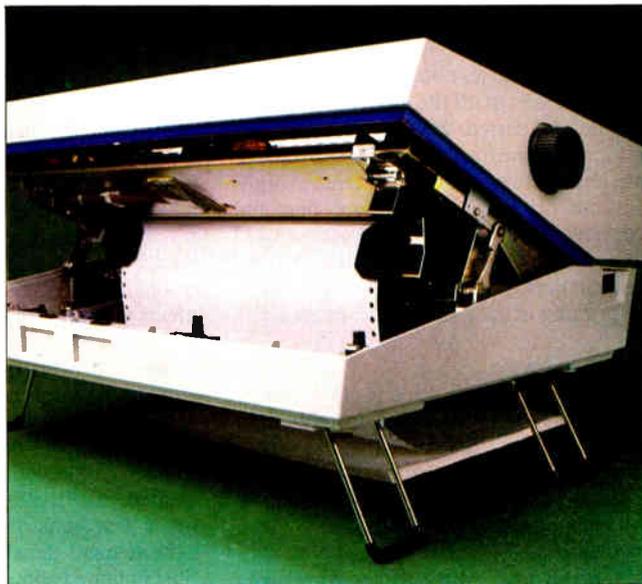


Photo 2: The Genicom 1020 has a novel method of accessing the tractor-feed mechanism: "lifting the hood." This printer is one of the most versatile in terms of form handling. It even lets you rip off a form and begin printing at the top line of the next form.

REVIEW: DOT-MATRIX PRINTERS

Table 1: Benchmark results. Prices include a parallel interface and tractor feed. Throughput is in cps. Sound level is in dB (0 dB = .0002 μ bar). Print quality: 5 = excellent; 4 = good; 3 = average; 2 = poor; 1 = unacceptable; * = not available.

Company	Model	Price	Throughput			Sound level			Print quality		
			Draft	NLQ	Graphics	Draft	NLQ	Graphics	Draft	NLQ	Graphics
Advanced Matrix Technology	AMT 2002	\$1995	137	33	*	73	82	*	2	4	*
Alps America	ALQ218	\$660	121	74	449	70	70	156	3	3	3
	ALQ324	\$1080	106	50	337	70	71	208	3	4	3
	P2000	\$995	145	39	737	70	67	95	3	3	3
	P2100	\$1595	187	56	833	65	63	84	3	3	3
Brother International Corp.	2024L	\$1295	93	63	461	70	73	152	4	3	2
	M-1709	\$699	113	32	412	71	68	170	2	3	4
C. Itoh Digital Products Inc.	C-3*0XP	\$699	161	29	467	70	69	150	4	4	4
	C-8*5 Supra	\$1995	187	94	458	76	72	153	4	4	2
Canon USA Inc.	A-50	\$499	92	26	427	70	71	164	2	2	3
	A-60/G	\$679	116	71	385	71	70	182	4	4	3
Citizen America Corp.	120D	\$269	90	21	461	71	70	152	3	2	3
	Tribute 224	\$949	119	57	*	73	74	*	4	4	*
Dataproducts Corp.	8012	\$535	94	18	178	69	67	393	2	3	4
	8070 Plus	\$1999	226	56	476	73	71	147	2	3	3
Datasouth Computer Corp.	DS 180 Plus	\$1395	130	*	*	75	*	*	2	1	*
Epson America Inc.	EX-1000	\$899	136	44	1458	71	70	48	3	3	2
	LQ-2500	\$1595	93	34	400	72	72	175	3	3	3
Fujitsu America Inc.	DL 2600	\$1495	145	72	933	70	68	75	3	2	2
	DX 2200	\$695	119	30	496	72	71	141	3	3	3
Genicom Corp.	1020	\$999	125	76	519	72	71	135	3	3	3
	3210	\$1495	176	38	*	78	76	*	3	2	2
	3410.02	\$2645	*	*	*	*	*	*	*	*	*
IBM Corp.	Proprinter XL	\$799	123	30	254	75	73	276	3	3	2
Infoscrite Inc.	1100P	\$1490	125	35	*	77	75	*	3	3	*
	1400	\$1845	183	56	*	74	72	*	2	2	*
JDL Inc.	JDL-850 EWS	\$2495	110	96	504	67	65	139	4	4	4
Mannesmann Tally	MT-290	\$1099	143	38	414	74	72	169	4	3	4
	MT-490	\$2549	*	*	*	*	*	*	*	*	*
NEC Information Systems	P5XL	\$1674	*	*	*	*	*	*	*	*	*
Newbury Data Inc.	OSP-3	\$1560	*	*	*	*	*	*	*	*	*
Nissho Information Systems	NP-2410	\$2040	175	104	833	72	71	84	4	4	2
	NP-910	\$1445	191	36	631	72	71	111	4	3	3
Okidata	ML193 Plus	\$749	115	36	435	73	71	161	3	3	3
	ML294	\$1499	201	77	625	72	70	112	3	3	2
Olympia USA Inc.	NP 136	\$649	133	38	574	70	69	122	4	3	3
Output Technology Corp.	OT-700e	\$1995	198	75	642	79	79	109	3	2	3
Panasonic Industrial Co.	KXP-1092i	\$549	111	34	515	72	73	136	3	4	3
	KXP-1080i	\$329	87	22	361	72	73	194	3	2	2
	KXP-1091i	\$429	102	27	*	71	69	*	2	3	*
Printronix Inc.	P1013	\$795	109	43	464	79	78	151	2	4	3
Seikosha America Inc.	BP-5420 AI	\$1849	247	84	1458	70	70	48	2	2	2
	MP-1300 AI	\$699	159	43	579	71	68	121	2	3	3
	SL-80 AI	\$549	57	30	251	67	69	279	2	3	2
Star Micronics America Inc.	NB24-15	\$1099	112	50	507	74	75	138	4	4	2
	NR-15	\$799	138	37	673	74	71	104	4	3	2
	NX-15	\$499	78	19	348	72	70	201	3	2	3
Tandy Corp./Radio Shack	DMP 130	\$350	60	14	120	63	62	583	2	2	2
	DMP 2110	\$1295	138	65	470	70	74	149	4	4	2
	DMP 430	\$699	119	67	380	72	74	184	3	3	2
Texas Instruments Inc.	Omni 880	\$2195	183	56	*	70	69	*	2	3	*
Toshiba America Inc.	P341e	\$999	96	45	*	75	74	*	4	4	*
	P351-2	\$1599†	142	65	625	71	72	112	4	4	3

† At press time, Toshiba lowered the price of the P351-2 to \$1399.

floor (while the printer is on a stand or a table with a slot). This is the preferred paper path when dealing with heavy multipart forms, since it minimizes jams and drag on the tractor (see photo 2).

Word Processing Features

Table 3 lists many key word processing features. *Emulation* indicates the software compatibility of a printer as stated in the documentation. Emulation primarily

concerns a printer's response to escape codes for font changes, graphics, paper control, and so forth.

A font is a set of letterforms for a given

continued

REVIEW: DOT-MATRIX PRINTERS

Table 2: General specifications. Max. CPS is the company's specification. Density = dots per inch. Buffer measurements are in K bytes. Pull=pull tractor; push=push tractor; tractor=type not specified. Paper handling: S = standard; O = optional; * = feature is available. Linear measurements are in inches; * = not available or not applicable. H x V = horizontal by vertical.

Company	Model	Max. CPS				Paper handling											Size HxWxD	Wt. lbs.
		Draft	NLQ	Print wires	Char. matrix	Graphic density H x V	Buffer size (Std-Opt.)	Max. char./line	Max. form width	Accept.	Max. copies	Friction	Pull	Push	Tractor	1-Bin		
AMT	AMT 2002	250	45	16	32x72	480x240	6.5 - 40	264	3-15	6	S		O	O	O	*	7x25x18	45
Alps	ALQ218	200	100	18	18x24	240x216	7-64	160	4-10	3	S		O	O	O	*	6x18x16	31
	ALQ324	240	80	24	24x36	240x216	7-64	272	4-16	3	S		O	O	O	*	6x24x16	38
	P2000	250	55	9	18x23	240x216	4-256	272	4-16	*	S	S	S			*	6x24x16	37
	P2100	400	80	18	18x23	240x216	4-256	272	4-16	*	S	S	S			*	6x24x16	42
Brother	2024L	160	80	24	16x30	* x 180	1 - *	272	5-15	5	S	S	S	O			6x22x15	29
	M-1709	200	50	9	9x7	240x216	24-40	272	4-16	3	S	S	S	O			4x19x12	16
C. Itoh	C-310XP	300	50	9	17x17	240x72	2-10	137	4-11	4	S	S	S	O	O	*	5x17x14	21
	C-815 Supra	333	135	24	24x36	360x180	42 - *	232	4-16	5	S	S		O	O	*	6x23x16	33
Canon	A-50	180	34	9	23x18	240x72	2 - *	132	4-10	3	S		S				4x16x13	18
	A-60/G	200	100	18	23x18	240x*	8.5 - *	137	4-10	3	S		S	O			4x15x12	14
Citizen	120D	120	25	9	17x17	240x216	4 - *	160	4-10	3	S		S	O		*	4x15x9	8
	Tribute 224	200	66	24	36x24	360x180	24 - *	244	4.5-16	3	S		S	O			5x23x14	16
Dataproducts	8012	180	30	9	36x18	165x83	2 - *	136	3-10	3	S		S				5x17x14	*
	8070 Plus	400	100	18	36x18	165x83	4-6	226	4-15	6	S		S	O		*	10x23x13	40
Datasouth	DS 180 Plus	180	*	9	*	75x72	4 - *	272	4-16	6			S			*	7x24x16	35
Epson	EX-1000	250	50	9	*	240x216	8-128	272	4-16	3	S	S	S	O			5x24x15	25
	LQ-2500	270	90	24	*	360x180	8 - *	272	4-16	4	S	S		O			6x23x15	26
Fujitsu	DL 2600	288	96	24	36x24	360x180	8 - *	272	4-16.5	5	S		S	O	O		6x22x15	40
	DX 2200	220	44	9	19x16	240x60	8-16	272	4-16.5	3	S		S	O			5x23x14	26
Genicom	1020	200	100	18	36x18	240x144	2-64	232	4-16	4	S		S	O	O	*	10x24x15	39
	3210	240	60	8	9x18	240x144	2-8	217	* - 15.5	4	O		S	O			6x25x16	37
	3410.02	400	120	18	18x15	240x144	*	228	* - 15.5	6	O		S	O	O	*	*	*
IBM	Proprinter XL	200	40	9	*	120x144	4-8	232	3-15	4	S		S				5x16x14	*
Infoscrite	1100P	200	100	9	19x18	144x144	3 - *	224	1.5-16	6	S		S	O	O	*	7x26x15	32
	1400	400	80	18	24x18	144x144	8-32	224	1.5-16	6	S		S	O	O	*	7x26x15	32
JDL	JDL-850 EWS	300	120	24	36x24	180x180	128 - *	272	3-18	4	S	S	S	O	O		8x26x17	42
Mannesmann Tally	MT-290	200	50	9	18x48	288x144	8 - *	264	3-16	5	S	S	O	O	O	*	5x20x10	25
	MT-490	400	150	18	18x48	240x72	8 - *	225	3-16	4	O	O	O	O	O	*	9x26x18	79
NEC	P5XL	290	100	24	17x32	360x180	8-40	272	5-16.5	4	S			O	O	O	6x23x15	37
Newbury	OSP-3	200	50	18	40x16	240x216	3 - *	*	6-13	3	S			O	O	O	9x21x19	44
Nissho	NP-2410	300	150	24	24x36	360x180	6-54	238	4-16	5	S			O	O	O	6x24x17	41
	NP-910	350	58	9	17x24	240x72	4-52	237	4.5-16	5	S			O	O	*	5x24x16	33
Okidata	ML193 Plus	200	40	9	17x17	240x72	8 - *	233	3-16	4	S		S	O		*	5x21x15	13
	ML294	400	100	18	17x17	288x72	8-32	233	3-16	4			S			*	6x21x13	16
Olympia	NP 136	200	40	9	18x24	240x144	7-8	233	4-16	3	S		S	O	O		4x24x14	22
OTC	OT-700e	700	66	9	*	100x69	8 - *	226	4-16	6			S			*	6x27x17	34
Panasonic	KXP-1092i	240	48	9	18x18	240x72	6-32	137	4-10	3	S	S	S	O			5x17x14	22
	KXP-1080i	120	24	9	18x18	240x72	1-4	137	3-10	3	S		S				5x16x11	13
	KXP-1091i	160	32	9	18x18	240x72	1-4	137	3-10	3	S		S				5x16x11	15
Printronic	P1013	178	63	24	24x36	360x180	2 - *	137	2-10	3	S		S				5x16x12	22
Seikosha	BP-5420 AI	420	104	8	24x16	240x120	18 - *	217	5-15.5	5	S		S	O		*	8x23x16	60
	MP-1300 AI	300	50	9	24x18	240x72	10-16	160	4-10	5	S		S	O		*	6x18x18	19
	SL-80 AI	135	45	24	36x17	360x180	16 - *	160	4-10	3	S		S	O			10x22x17	15
Star Micronics	NB24-15	180	60	24	24x31	360x360	5-21	272	4-15.5	3	S		S	O			5x23x15	33
	NR-15	240	60	9	18x23	240x216	12-28	272	4-15.5	3	S		S	O			4x21x14	26
	NX-15	120	30	9	18x23	240x216	4-20	272	4-15.5	3	S		S	O			4x21x14	24
Tandy	DMP 130	100	*	9	19x19	240x144	*	*	4-10	3	S		S	O			5x15x10	11
	DMP 2110	240	83	24	30x24	240x120	*	226	4-15	4	S		S	O			6x22x15	34
	DMP 430	184	108	9	18x18	240x144	*	220	4-15	3	S		S			*	6x22x14	28
TI	Omni 880	300	75	9	15x18	240 x *	2-16	220	3-15	4			S		*	8x26x20	55	
Toshiba	P341e	180	60	24	*	360x180	2 - *	226	4-15	3	S			O	O		6x22x15	31
	P351-2	250	83	24	*	360x180	4 - *	266	4-15	6	S			O	O	*	6x22x15	33

character set. Typical fonts are Courier and Elite, which resemble the 10-pitch and 12-pitch settings on IBM Selectric typewriters; other typical fonts are roman and sans serif.

•*Pitch* lists the different character densities in cpi, including proportionally spaced density. Some printers can output each font in draft and NLQ; other units include draft as one of their fonts. The *Number of fonts* and *Draft & NLQ* columns in table 3 clarify this point.

The two primary ways of expanding a printer's text capabilities are through *font cartridges*, which increase the number of entire character fonts available, and *downloadable characters*, which you can create on your PC (with appropriate software) and append to the printer's provided character set.

•*Character sets* indicates whether a printer can reproduce the full IBM extended character set, referenced by ASCII codes 128 through 255; the Epson character set, referenced by the same range of characters; the international character set; or some other special character set such as APL.

•*Styles* tells whether a printer is able to apply the following attributes to each character in a font: superscript, subscript, bold, underlined, and italic.

•*Color*. We noted whether a printer could accept and use multicolor ribbons, but we did not test this feature.

Convenience Features

Other important printer features relate to ease of use, versatility, and potential long-term satisfaction with a product. This information appears in table 4.

•*Ribbon*. Printers were ranked according to the ease of changing their ribbons. A rating of 1 means the ribbon cartridge dropped right in with no need to handle the ribbon itself; a 2 rating means the ribbon required some additional handling

to be positioned properly. Estimated ribbon life and cost are also listed.

Today's dot-matrix printers are intended to operate in a number of different hardware and software environments: with a parallel or serial interface, with IBM, Epson, or other emulation, with paper-empty detection or override, with a default text-quality setting, and so forth. In addition to software controls (commands sent from the host computer), the printers offer a hardware means of setting the configuration.

•*DIP switches (DIP)*. Most printers allow you to define the power-up conditions of the unit by setting DIP switches. Conditions you can set may include the type of interface, the default character set, and software-emulation modes.

•*Front panel (FP)*. In addition to DIP switch settings, most printers let you modify the print characteristics (e.g., draft or high-quality, font, and character pitch) by using a set of buttons and indicators (see photo 3). This is handy when you don't want to go to the trouble of including the needed escape codes in your word processing text.

•*Menu*. A few printers let you make a much larger set of changes by using the front-panel buttons in conjunction with a menu that is output on the printer or on a built-in display.

Printer Evaluation

Before trying to judge printers based on the benchmark results and feature lists, it's important to have a clear idea of what general printer application you have: business-letter printing, high-volume business printing, or general applications, including word processing and graphics generation.

For printing letters, output quality is of first importance. Here, dot-matrix printers generally attempt to emulate the qual-

continued

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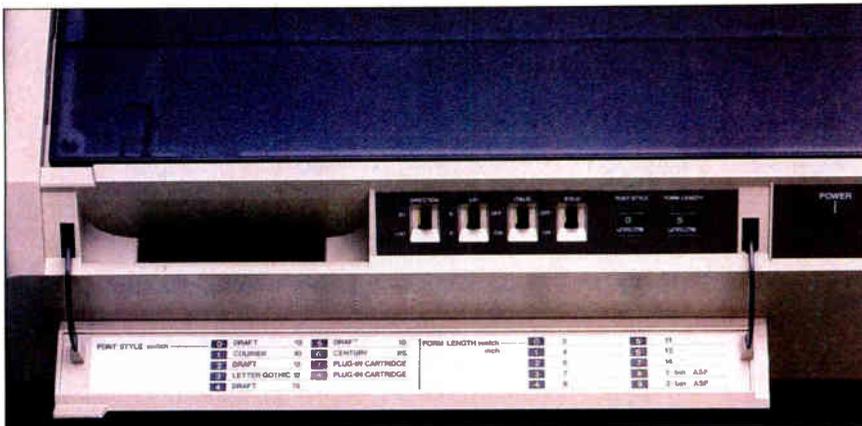


Photo 3: The Nissho NP-2410 has two control panels, exemplifying this method of selecting printer features.

REVIEW: DOT-MATRIX PRINTERS

Table 3: Printer features. Pitch measurements are in cpi. Draft & NLQ tells if separate modes are available for every font. Styles: _s = superscripts and subscripts; **b** = bold; *i* = italic; u = underlined; • = feature is available.

Company	Model	Emulation	Pitch	# of fonts Draft & NLQ Cartridges Download	Char. sets	Styles	Color
AMT	AMT 2002	Diablo 630 & Ink Jet, Qume Sprint 11, NEC Spinwriter, IBM Color, Epson JX-80	10, 12, 13.3, 15, 17.1, 20	4 • • •	Epson, IBM	_s b <u>u</u>	•
Alps	ALQ218	Epson FX-80, Epson JX-80, IBM Graphics Printer	10, 12, 17, 20	1 • • •	Epson, IBM, International	_s b <u>u</u>	•
	ALQ324	Epson LO-2500	10, 12, 17, 20	1 • • •	Epson, IBM, International	_s b <u>u</u>	•
	P2000	Epson FX-100, Diablo 630S	5, 6, 8.5, 10, 12, 17	1 • • •	Epson, IBM, International	_s b <u>u</u>	•
	P2100	Epson FX-100	5, 6, 8.5, 10, 12, 17	1 • • •	Epson, IBM, International	_s b <u>u</u>	•
Brother	2024L	Epson FX-80, Diablo 630	10, 12, 16.7, 20	3	International	_s b <u>u</u>	•
	M-1709	Epson FX-286, IBM Proprinter XL	5, 6, 8.5, 10, 12, 17, 20	2 • •	Epson, IBM, International	_s b <u>u</u>	•
C. Itoh	C-310XP	Epson FX-80+, IBM Proprinter	10, 12, 17.1	2 • • •	Epson, IBM, International	_s b <u>u</u>	•
	C-815 Supra	IBM Proprinter XL, Toshiba P351, Qume Sprint 11	10, 12, 17	2 • • •	IBM, International	_s b <u>u</u>	•
Canon	A-50	Epson FX, IBM Graphics Printer	5, 8.57, 10, 12, 17.14	1 • • •	Epson, IBM, International	_s b <u>u</u>	•
	A-60/G	Epson FX, IBM Graphics Printer	5, 6, 8.5, 10, 12, 17	1 • •	Epson, IBM, International	_s b <u>u</u>	•
Citizen	120D	Epson FX, IBM Graphics Printer	5, 6, 8.5, 10, 12, 17, 20	1 • •	Epson, IBM, International	_s b <u>u</u>	•
	Tribute 224	Diablo 630, Epson LO-800/1000, Qume Sprint 11, Toshiba 1340	10, 12, 16.7, 18	2 • • •	Epson, IBM, International	_s b <u>u</u>	•
Data-products	8012	IBM Color Printer, IBM Graphics Printer	10, 12, 13.3, 17.1	1 • •	IBM	_s b <u>u</u>	•
	8070 Plus	Dataproducts P80/8070/8072, IBM Color Printer, IBM Graphics Printer, IDS Prism	10, 12, 17.1	1 • •	IBM, International	_s b <u>u</u>	•
Datasouth	DS 180 Plus	None	5, 6, 8.25, 10, 12, 16.5	1 •	APL, IBM, International	<u>u</u>	•
Epson	EX-1000	Epson FX, IBM Graphics Printer, IBM Proprinter	10, 12, 17, 20	3 •	Epson, IBM, International	_s b <u>u</u>	•
	LQ-2500	Epson ESC/P, Epson EX	10, 12, 15	6 • •	Epson, International	_s b <u>u</u>	•
Fujitsu	DL 2600	Diablo 630, Epson JX-80, Fujitsu, IBM Graphics Printer	10, 12, 15, 17, 18, 20	2 • •	IBM, International	_s b <u>u</u>	•
	DX 2200	Epson FX-80/JX-80, IBM Graphics Printer, IBM Proprinter	10, 12, 15, 17.1, 20	2 •	Epson, International	_s b <u>u</u>	•
Genicom	1020	Diablo 630, Epson FX-80/100, IBM Color Graphics, IBM Graphics Printer, ANSI X364-1979	10, 12, 17.1	1 • •	IBM, International	_s b <u>u</u>	•
	3210	IBM Graphics Printer, Okidata ML 84 Step 2	5, 6, 6.55, 7.5, 8.25, 10, 12, 13.1, 15, 16.5/17	2 • •	IBM, International	_s b <u>u</u>	•
	3410.02	ANSI X364-1979, IBM Graphics Printer	5, 6, 8.35, 10, 12, 13.1, 15, 16.7	2 •	IBM, International	_s b <u>u</u>	•
IBM	Proprinter XL	IBM Proprinter, IBM Graphics Printer	5, 6, 8.55, 10, 12, 17.1	1 • •	IBM, International	_s b <u>u</u>	•
Infoscribe	1100P	Diablo 630, Epson MX-80, IBM Graphics Printer, IDS Prism	10, 12, 16.5	1 • •	International	_s b <u>u</u>	•
	1400	Diablo 630, Epson MX-80, IBM Graphics Printer, IDS Prism	10, 12, 16.5	2 • •	Epson, IBM, International	_s b <u>u</u>	•

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Company	Model	Emulation	Pitch	# of fonts Draft & NLQ Cartridges Download	Char. sets	Styles	Color
JDL	JDL-850 EWS	Epson FX, MX, RX, LX, and JX series, IBM Color Graphics Printer	10, 12, 15, 17.1, 20	2 • • •	APL, Epson, IBM, International	$\begin{smallmatrix} s \\ s \end{smallmatrix} \underline{b} / \underline{u}$	•
Mannesmann Tally	MT-290	MT-140, Epson FX, IBM Proprinter	5, 6, 7.5, 8.6, 10, 12, 17.1, 20	1 • •	APL, Epson, IBM, International	$\begin{smallmatrix} s \\ s \end{smallmatrix} \underline{b} / \underline{u}$	•
	MT-490	ANSI, Epson FX-100, IBM Proprinter	5, 6, 7.5, 8.6, 10, 12, 15, 17.1	1 • •	Epson, IBM, International	$\begin{smallmatrix} s \\ s \end{smallmatrix} \underline{b} / \underline{u}$	•
NEC	P5XL	Epson FX/MX, JX-80, LQ-1500	10, 12, 15, 17, 20	3 • •	Epson, IBM, International	$\begin{smallmatrix} s \\ s \end{smallmatrix} \underline{b} / \underline{u}$	•
Newbury	OSP-3	IBM Proprinter	10, 12, 15, 17	2 • •	IBM, International	$\begin{smallmatrix} s \\ s \end{smallmatrix} \underline{b} / \underline{u}$	•
Nissho	NP-2410	Epson LQ-1500	10, 12, 15, 18	4 • •	Epson, IBM, International	$\begin{smallmatrix} s \\ s \end{smallmatrix} \underline{b} / \underline{u}$	•
	NP-910	Epson FX-100+, IBM Graphics Printer	10, 12, 15, 18	2 • •	Epson, IBM, International	$\begin{smallmatrix} s \\ s \end{smallmatrix} \underline{b} / \underline{u}$	•
Okidata	ML193 Plus	IBM Graphics Printer, IBM Proprinter	5, 6, 8.5, 10, 12, 17.1	1 • •	IBM, International	$\begin{smallmatrix} s \\ s \end{smallmatrix} \underline{b} / \underline{u}$	•
	ML294	Epson JX-80, MX-80/100, IBM Color Printer, IBM Graphics Printer	5, 6, 8.5, 10, 12, 17	1 • •	IBM, International	$\begin{smallmatrix} s \\ s \end{smallmatrix} \underline{b} / \underline{u}$	•
Olympia	NP 136	Epson FX-80, IBM Proprinter	10, 12, 17	1 • • •	Epson, IBM, International	$\begin{smallmatrix} s \\ s \end{smallmatrix} \underline{b} / \underline{u}$	•
OTC	OT-700e	DEC LA 120 (DEC ANSI), Epson FX/MS-100	5, 6, 8.3, 10, 12, 16.6	1 •	Epson, IBM, International	$\begin{smallmatrix} s \\ s \end{smallmatrix} \underline{b} / \underline{u}$	•
Panasonic	KXP-1092i	Epson FX-80, IBM Proprinter	5, 6, 7.5, 8.5, 10, 12, 15, 17	3 • •	Epson, IBM, International	$\begin{smallmatrix} s \\ s \end{smallmatrix} \underline{b} / \underline{u}$	•
	KXP-1080i	IBM Graphics Printer, Epson RX-80	5, 6, 7.5, 8.5, 10, 12, 15, 17	2 • •	IBM, International	$\begin{smallmatrix} s \\ s \end{smallmatrix} \underline{b} / \underline{u}$	•
	KXP-1091i	Epson RX-80, IBM Proprinter	5, 6, 7.5, 8.5, 10, 12, 15, 17	2 • •	IBM, International	$\begin{smallmatrix} s \\ s \end{smallmatrix} \underline{b} / \underline{u}$	•
Printronix	P1013	Diablo 630, Epson LQ-1500, IBM Proprinter	10, 12, 17.1	1 • • •	Epson, IBM, International	$\begin{smallmatrix} s \\ s \end{smallmatrix} \underline{b} / \underline{u}$	•
Seikosha	BP-5420 AI	Epson FX-80, IBM Color Printer	10, 12, 16, 20	1 •	IBM, International	$\begin{smallmatrix} s \\ s \end{smallmatrix} \underline{b} / \underline{u}$	•
	MP-1300 AI	Epson FX-80, IBM Graphics Printer	10, 12, 17, 20	1 • •	IBM, International	$\begin{smallmatrix} s \\ s \end{smallmatrix} \underline{b} / \underline{u}$	•
	SL-80 AI	Epson LQ-1500, IBM Graphics Printer	10, 12, 17, 20	1 • •	IBM, International	$\begin{smallmatrix} s \\ s \end{smallmatrix} \underline{b} / \underline{u}$	•
Star Micronics	NB24-15	Epson LQ-1000, IBM Graphics Printer, IBM Proprinter	10, 12, 15, 17, 20	1 • • •	Epson, IBM, International	$\begin{smallmatrix} s \\ s \end{smallmatrix} \underline{b} / \underline{u}$	•
	NR-15	Epson FX-85, IBM Graphics Printer, IBM Proprinter	10, 12, 15, 17	1 • •	Epson, IBM, International	$\begin{smallmatrix} s \\ s \end{smallmatrix} \underline{b} / \underline{u}$	•
	NX-15	Epson FX-85, IBM Graphics Printer	10, 12, 15, 17	1 • •	Epson, IBM, International	$\begin{smallmatrix} s \\ s \end{smallmatrix} \underline{b} / \underline{u}$	•
Tandy	DMP 130	IBM Graphics Printer	5, 6, 8.5, 10, 12, 17	1 •	IBM, International, Tandy	$\begin{smallmatrix} s \\ s \end{smallmatrix} \underline{b} / \underline{u}$	•
	DMP 2110	IBM Graphics Printer	5, 6, 8.3, 10, 12, 16.7	2 •	IBM, International, Tandy	$\begin{smallmatrix} s \\ s \end{smallmatrix} \underline{b} / \underline{u}$	•
	DMP 430	IBM Graphics Printer	5, 6, 8.3, 10, 12, 16.7	1 •	IBM, International, Tandy	$\begin{smallmatrix} s \\ s \end{smallmatrix} \underline{b} / \underline{u}$	•
TI	Omni 880	IBM Proprinter, TI Model 850/860 XL	5, 6, 8.3, 10, 12, 16.7	1 • •	IBM, International	$\begin{smallmatrix} s \\ s \end{smallmatrix} \underline{b} / \underline{u}$	•
Toshiba	P341e	IBM Graphics Printer, Qume Sprint 5 & 11	5, 6, 6.7, 8.3, 10, 12, 13.4, 16.7	3 • •	IBM, International	$\begin{smallmatrix} s \\ s \end{smallmatrix} \underline{b} / \underline{u}$	•
	P351-2	IBM Graphics Printer, Qume Sprint 5 & 11	5, 6, 6.7, 8.3, 10, 12, 13.4, 16.7	3 • •	IBM, International	$\begin{smallmatrix} s \\ s \end{smallmatrix} \underline{b} / \underline{u}$	•

REVIEW: DOT-MATRIX PRINTERS

Table 4: Convenience features. Ribbon ease: 1 = easiest; 2 = average. Ribbon-life measurements are in millions of characters. Documentation ease and technical quality: 3 = best; 2 = average; 1 = inadequate.

Company	Model	Ribbon					Interfaces		Documentation	Comments		
		Ease	Life	Cost	DIP	FP	Menu	Std.		Opt.	Manuals: pages	Ease
AMT	AMT 2002	1	10	\$35	•	•	parallel, serial		Programmer's Reference Manual:184, Operator's Manual:83	2	2	Print-head life given as one year. Has draft, memo, and letter-quality print styles.
Alps	ALQ218	1	2	\$15	•		parallel, serial		User's Manual:240	1	1	24-wire head also available. Interface cartridges available for various compatibilities.
	ALQ324	1	2	\$15	•		parallel	serial	User's Manual:240	1	1	18-wire head also available. Interface cartridges available for various compatibilities.
	P2000	2	3	\$12	•	•	parallel, serial		User's Manual:130	1	1	Interface cartridges available for various compatibilities.
	P2100	2	3	\$12	•	•	parallel, serial		User's Manual:130(QRC*)	1	1	Interface cartridges available for various compatibilities.
Brother	2024L	1	2	\$10	•	•	parallel, serial		Owner's Manual:84	3	2	Forms "parking" allows single-sheet printing without unloading forms.
	M-1709	2	2	\$12	•	•	parallel, serial		Owner's Manual:126	2	2	
C. Itoh	C-310XP	1	2	\$9	•	•	parallel	serial	User's Manual:215(QRC)	1	1	Has draft, near-letter-quality, and letter-quality print styles.
	C-815 Supra	2	6	\$35	•		parallel, serial		User's Manual:150	2	2	
Canon	A-50	2	3	\$10	•		parallel	serial, loop	Operation Manual:171	2	2	Ribbon cartridges sold in 6-packs for \$60.
	A-60/G	1	2	\$13	•	•	parallel or serial		Operation Manual:116	2	2	Ribbon cartridges sold in 6-packs for \$78. Has draft, near-letter-quality, and near-letter-quality "plus."
Citizen	120D	2	2	\$6	•		parallel	serial	User's Manual:184(QRC)	2	2	Font cartridges are credit-card-like cards. Emulator modes are enabled with similar cards.
	Tribute 224	2	4	\$22	•	•	parallel, serial		Reference Manual:108(QRC), User's Manual:82(QRC)	1	1	
Data-products	8012	2	4	\$10		•	parallel		Owner's Guide:80	2	3	Ribbon cartridges sold in 6-packs for \$61. Has draft, text, and letter quality.
	8070 Plus	2	7	\$10		•	parallel, serial		Operating Guide:75(QRC)	2	2	Ribbon cartridges sold in 6-packs for \$60. Has draft, correspondence, and letter quality.
Datasouth	DS 180 Plus	1	4	\$10	•		parallel or serial	loop	Operator's Manual:85(QRC)	2	2	
Epson	EX-1000	1	3	\$15	•	•	parallel, serial	loop	User's Manual:225(QRC)	1	2	Control panel includes SelectedType with an LCD.
	LQ-2500	1	2	\$18	•	•	parallel, serial		User's Manual:225(QRC)	2	1	
Fujitsu	DL 2600	2	15	\$30	•		parallel, serial		User's Manual:191	2	2	
	DX 2200	1	3	\$13	•	•	parallel or serial	dual, parallel, & serial	User's Manual:168	2	2	
Genicom	1020	2	4	\$12	•	•	parallel or serial		Operator's Manual:100, Personality Reference Manual:80(QRC)	2	2	Has personality cartridges containing emulation and interface information. Zero-inch tear-off saves forms.
	3210	2	4	\$12	•	•	parallel, serial		User's Manual:150	3	2	Also prints bar codes.
	3410.02	2	15	\$24	•	•	parallel, serial		User's Manual:150	3	3	
IBM	Proprinter XL	2	3	\$13	•	•	parallel	serial	Guide to Operations:175(QRC), Guide to Programming:100	1	2	"Quiet" printing mode.
Infoscribe	1100P	2	5	\$11	•		parallel, serial, dual (switchable), or loop		Operator's Manual:100	2	2	Bar code printer option. Draft, near-letter, and correspondence quality.
	1400	2	5	\$11	•		parallel	dual, parallel, & serial	Operator's Manual:100	3	3	Bar code option. Draft, correspondence, and near-letter quality.
JDL	JDL-850 EWS	2	*	\$60	•	•	parallel or serial		Operator's Manual:90	2	1	Optional emulation ROM cards. Control panel includes an LCD. This is also a color plotter.

* QRC = quick-reference card

REVIEW: DOT-MATRIX PRINTERS

Company	Model	Ribbon			Interfaces			Documentation		Comments	
		Ease Life	Cost	Dip FP Menu	Std.	Opt.	Manuals: pages	Ease Quality			
Mannes- mann Tally	MT-290	1 3	\$14	• • •	parallel	serial, loop	Operator's Manual:80, Ap- plications Manual:114	2 2	Ribbon cartridges sold in 5-packs for \$69.75.		
	MT-490	2 5	\$7	•	parallel, serial		Operator's Manual:50, Ap- plications Manual:140	2 1	Ribbon cartridges sold in 10-packs for \$69.50.		
NEC	P5XL	1 3	\$14	• •	parallel, serial		Technical Reference Guide:173, User's Guide:42	2 1			
Newbury	OSP-3	2 *	\$8	•	parallel, serial	parallel, serial	User Handbook:240	2 2	Has draft, near-letter-quality, and letter-quality print styles.		
Nissho	NP-2410	1 6	\$15	• • •		parallel, serial	User's Manual:118, Pro- gramming Manual:106, IBM coax and twinax	2 2	Optional zero-inch tear-off saves forms.		
	NP-910	1 6	\$15	• •		parallel, serial	User's Manual:87, Pro- grammer's Manual:93, In- terface Manual:11, IBM coax and twinax	2 2	Has plug-in font chips, not car- tridges. Optional zero-inch tear-off tractor system.		
Okidata	ML193 Plus	1 3	\$9		•	parallel, serial	Getting Started:22, IBM Compatible Reference Guide:46	1 2	Personality modules. Okifont soft- ware included.		
	ML294	2 5	\$19	• •	parallel, serial		Printer Handbook:25, IBM Compatible Reference Guide:107	1 2	Plug-in personality cartridges, Oki- font software, and color print software.		
Olympia	NP 136	2 3	\$10	• •	parallel	serial	Operation Manual:157	1 2	Font cartridges are credit-card-like cards that slide into a slot.		
OTC	OT-700e	2 6	\$20	• •	parallel, serial		Operator's Guide:115	2 2	Three-head design achieves max- imum throughput when printing on wide (136-column) forms. Also prints bar codes.		
Panasonic	KXP-1092i	1 3	\$12	•	parallel	serial	Operating Instructions:150	1 1	Exceptional manual. Lots of informa- tion packed into first three pages.		
	KXP-1080i	1 3	\$10	•	parallel	serial	Operating Instructions:107	2 2			
	KXP-1091i	1 3	\$10	•	parallel	serial	Operating Instructions:120	1 1			
Printronix	P1013	1 3	\$10	•	parallel		User's Reference Manual:225(QRC)	2 2	Identity cartridge includes character- set, font, and emulation mode. Has a serial 24-wire hammer-and-shuttle assembly.		
Seikosha	BP-5420 AI	2 8	\$15	• •	parallel, serial		Operation Manual:90	2 2			
	MP-1300 AI	1 8	\$19	• •	parallel, serial		Owner's Manual:161	1 1			
	SL-80 AI	1 2	\$9	• •	parallel		Preliminary Technical Document:54	3 2	128 downloadable characters.		
Star Micronics	NB24-15	2 5	\$11	• •	parallel	serial, loop	User's Manual:240, User's Guide:2	2 2			
	NR-15	2 3	\$12	• •	parallel	serial, loop	User's Manual:214, User's Guide:2	2 2			
	NX-15	2 3	\$12	• •	parallel	serial, loop	User's Manual:195, User's Guide:2	2 2			
Tandy	DMP 130	2 2	\$11	•	parallel, serial		Operation Manual:118	2 3	Ribbon refills sold in 3-packs for \$12.95. Has Microfont, which lets you print everything in subscript-size type.		
	DMP 2110	1 2	\$14	•	parallel		Operation Manual:180	2 2	Microfont lets you print everything in subscript-size type.		
	DMP 430	1 4	\$16	•	parallel, serial		Operation Manual:132	2 2	Microfont lets you print everything in subscript-size type.		
TI	Omni 880	2 *	\$5	• •	parallel, serial		Quick Reference Guide:20, User's Manual:100, Worldwide Service and Support:12	2 2	Ribbon spools sold in 6-packs for \$27. Has interfaces for IBM, TI PC, and Macintosh.		
Toshiba	P341e	1 2	\$12	•	parallel, serial		User's Manual:154, Annex II to User's Manual:13	1 1			
	P351-2	1 2	\$12	• •	parallel, serial		User's Manual:224	1 2	Quiet-printing mode. Bidirectional tractor available. Electronic in- tegrated sheet feeder optional.		

Printer Companies

Advanced Matrix Technology Inc.

Model tested: AMT 2002 Office Printer
1157 Tourmaline Dr.
Newbury Park, CA 91320
(805) 499-8741

Alps America

Models tested: P2100, P2000, ALQ324, ALQ218
3553 North First St.
San Jose, CA 95134
(800) 828-2577

Brother International Corp.

Models tested: 2024L, M-1709
8 Corporate Place
Piscataway, NJ 08854-0159
(201) 981-0300

C. Itoh Digital Products Inc.

Models tested: C-310XP, C-815
Supra
19750 South Vermont St., Suite 220
Torrance, CA 90502
(213) 327-2110

Canon U.S.A. Inc.

Models tested: A-50, A-60/G
One Canon Plaza
Lake Success, NY 11042-9979
(516) 488-6700

Citizen America Corp.

Models tested: Tribute 224, 120D
2425 Colorado Ave.
Santa Monica, CA 90404
(213) 453-0614

Dataproducts Corp.

Models tested: 8070 Plus, 8012
Route 13 S
Milford, NH 03055
(603) 673-9100

Datasouth Computer Corp.

Model tested: DS 180 Plus
4216 Stuart Andrew Blvd.
Charlotte, NC 28210
(800) 222-4528

Epson America Inc.

Models tested: EX-1000, LQ-2500
2780 Lomita Blvd.
Torrance, CA 90505
(213) 539-9140

Fujitsu America Inc.

Models tested: DX 2200, DL 2600
3055 Orchard Dr.
San Jose, CA 95134-2017
(408) 946-8777

Genicom Corp.

Models tested: 1020, 3410.02, 3210
One Genicom Dr.
Waynesboro, VA 22980
(703) 949-1000

IBM Corp.

Model tested: Proprinter XL
Old Orchard Rd.
Armonk, NY 10504
(800) 426-2468

Infoscrite Inc.

Models tested: 1100P, 1400
1808 Michael Faraday Ct.
Reston, VA 22090
(800) 233-4442

JDL Inc.

Model tested: JDL-850 EWS
2801 Townsgate Rd., Suite 104
Westlake Village, CA 91361
(805) 495-3451

Mannesmann Tally

Models tested: MT-490, MT-290
8301 South 180th St.
Kent, WA 98032
(206) 251-5500

NEC Information Systems Inc.

Model tested: Pinwriter P5XL
155 Swanson Rd.
Boxborough, MA 01719
(800) 343-4418

Newbury Data Inc.

Model tested: OSP-3
2200 Pacific Coast Hwy., Suite 208
Hermosa Beach, CA 90254
(213) 372-3775

Nissho Information Systems

Models tested: NP-2410, NP-910
10855 Business Center Dr., Suite 100
Cypress, CA 90630
(714) 952-8700

Okidata

Models tested: ML294, ML193
Plus
532 Fellowship Rd.
Mt. Laurel, NJ 08054
(800) 654-3282

Olympia USA Inc.

Model tested: NP 136
Box 22, Route 22
Somerville, NJ 08876
(201) 722-7000

Output Technology Corp.

Model tested: OT-700e
East 9922 Montgomery, Suite 6
Spokane, WA 99206
(800) 468-8788

Panasonic Industrial Co.

Models tested:
KXP-1080i, KXP-109ii,
KXP-1092i
2 Panasonic Way
Secaucus, NJ 07094
(201) 348-7000

Printronix Inc.

Model tested: P1013
17500 Cartwright Rd.
Irvine, CA 92713
(714) 863-1900

Seikosha America Inc.

Models tested: SL-80 AI,
MP-1300 AI, BP-5420 AI
1111 Macarthur Blvd.
Mahwah, NJ 07430
(201) 529-4655

Star Micronics America Inc.

Models tested: NX-15, NR-15,
NB24-15
200 Park Ave., Suite 3510
New York, NY 10166
(212) 986-6770

Tandy Corp./Radio Shack

Models tested: DMP 130,
DMP 2110, DMP 430
1800 One Tandy Center
Fort Worth, TX 76102
(817) 390-3011

Texas Instruments Inc.

Data Systems Group
Model tested: Ormi Model 880
P.O. Box 809063
Dallas, TX 75380-9063
(800) 527-3500

Toshiba America Inc.

Models tested: P351 Model 2,
P341e
2441 Michelle Dr.
Tustin, CA 92680
(714) 730-5000

ity of a daisy-wheel printer output by placing the dots so close together that they approximate solid lines. This can be done with multiple passes of the print head or by increasing the number and density of the wires on the print head. The printers we tested had print-head densities ranging from 8 to 24 wires.

For correspondence, the availability of single-sheet paper-handling systems such as friction-feed and cut-sheet feeders will probably be an important factor, in addition to print quality.

High-volume applications include printing regular reports, mailing lists, and forms. Here the key feature is speed. Special form-handling capabilities such as bottom feed, the ability to tear off a form and continue printing on the top line of the next form, and the ability to print multipart forms may also be important.

Included in general applications are

full-featured word processing and bit-map graphics printing. Font availability, print quality, and available attributes are all important for word processing. For bit-map graphics, resolution and software emulation determine how useful a given model will be. Since graphics printing usually involves a high volume of data, the presence and size of an input buffer may assume extra importance as well.

To assist you in sorting out all the information contained in the charts, we've ranked the top 10 printers in the three general application areas of high-quality correspondence, high-volume printing, and general use (see figure 2). Printers in the top row achieved the highest scores on the NLQ print-quality test. Printers in the second row had the highest throughput in draft mode; to be considered for this category, a maximum form width of at least

13.5 inches was required. The bottom row features the 10 least-expensive qualifying printers. To qualify, printers had to offer superscripts, subscripts, underlining, boldface, and italic, and had to have an overall print-quality score (draft + NLQ + graphics)/3 of at least 3.

A Safe Buy

No printing technology on the horizon can compete with dot-matrix impact technology as a low-cost yet versatile system of printing. Dot-matrix printers have put daisy-wheel quality under siege, and they can even make a respectable attempt at laser printer productions.

In summary, you can purchase a printer without fear that tomorrow's printer will render yours obsolete. The real challenge is in finding the printer with the features you need, and that's where our tables will help. ■

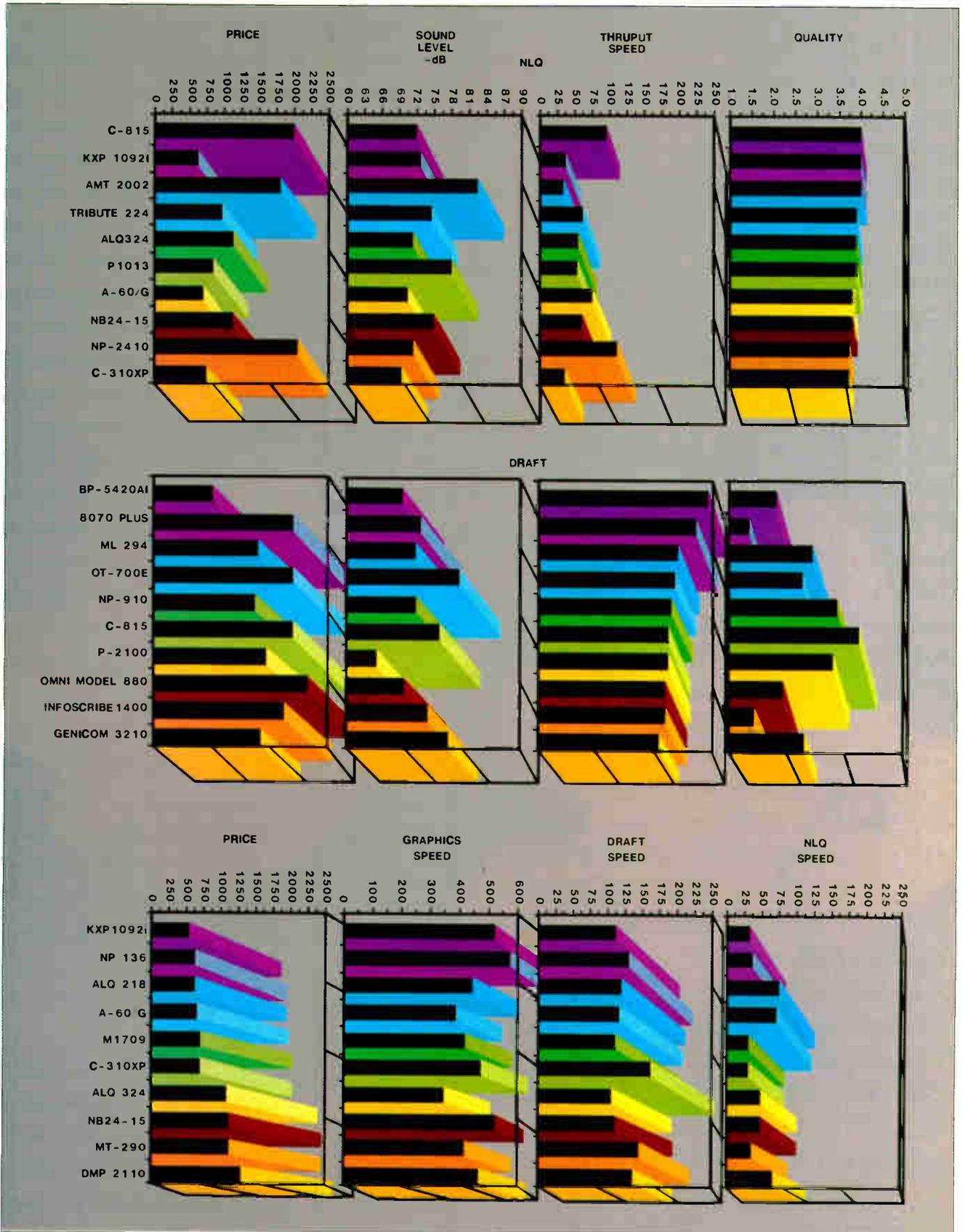
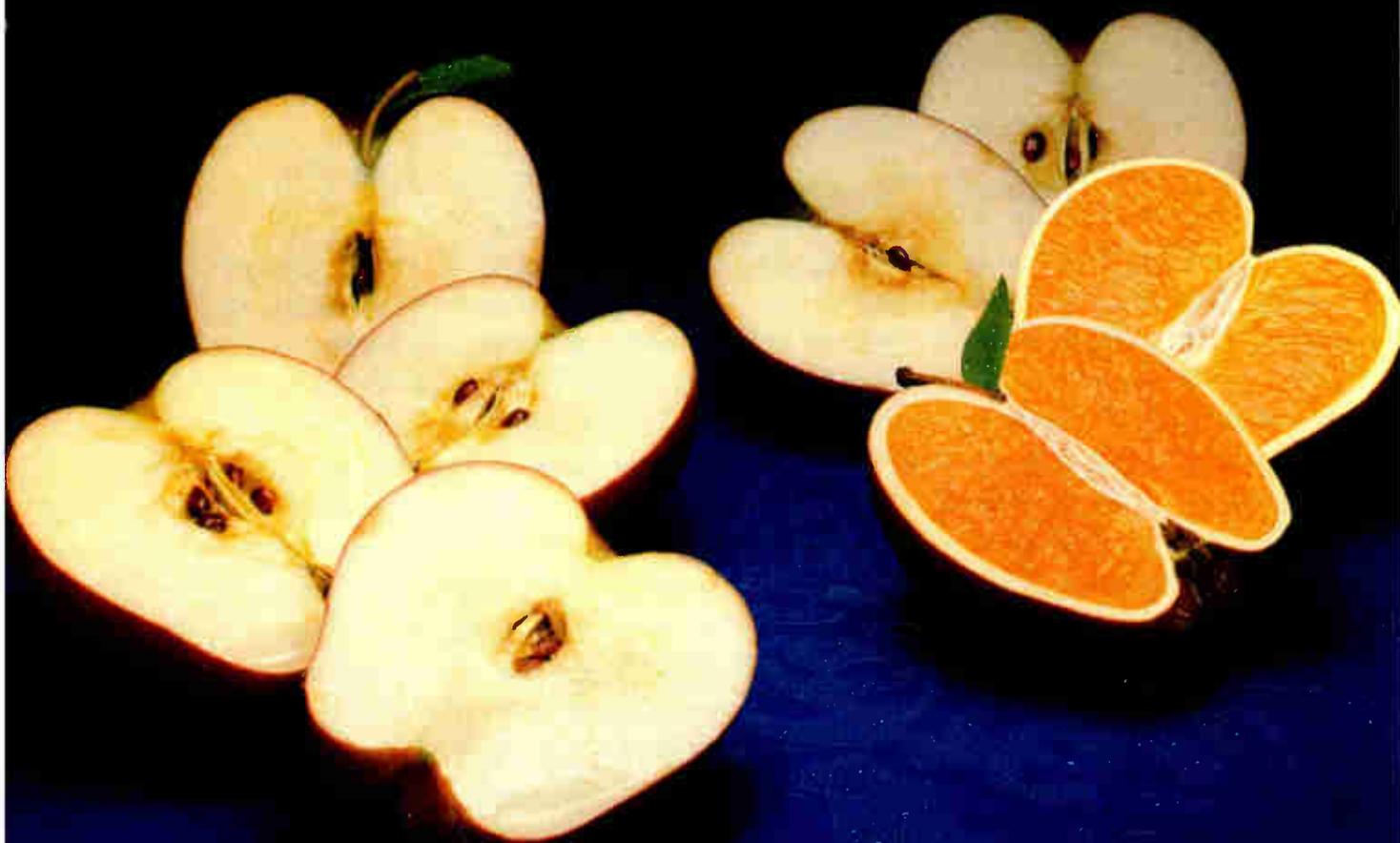


Figure 2: The top-ranked printers in three categories: NLQ printing (top row), high-volume printing (middle row), and general personal computer applications (bottom row). See text for further information.



MOTOROLA



MC68020 vs. 80386.

How to run apples-to-apples vs. apples-to-oranges benchmarks on these archrival 32-bit MPUs.

Choosing the world's highest-performance 32-bit microprocessor should be as easy as making an apples-to-apples comparison with such industry-standard benchmarks as Whetstone and Dhrystone performance.

How to tell apples from oranges.

When pulling an apples-to-apples comparison, anyone, anywhere, should be able to easily duplicate the comparison factors and results. Repeatably.

Attempt no. 1.

So, when comparing the MC68020 and 80386, the first task is to find one of each.

Motorola shipped over a quarter of a million MC68020s last year, so finding one is easy. Get the fastest available—a 25 MHz—and a 20 MHz Motorola floating-point coprocessor, the MC68881.

Next (things get harder), try to get your hands on a fully functional, bug free 80386 MPU and 80387 floating point.

And now you know why it's so hard to make an apples-to-apples comparison: you can get the Motorola devices, but "comparable" '386 and '387s? No way. You have to settle for the slower '386 and the promise of silicon yet to come on the '387.

Attempt no. 2.

All right, if you can't find the chips, go for readily-available 32-bit systems and compare real, live, '020- and '386-based systems from the commercial market.

Exasperating, isn't it? There are hundreds of choices of commercially-available, '020-based systems. But, finding comparable '386-based systems...?

Attempt no. 3.

Running real benchmarks on real products is the best comparison. We've looked at two questionable comparison attempts. Now it's time to try some industry-standard approaches, such as Whetstone and Dhrystone benchmarking. That should allow an apples-to-apples comparison, shouldn't it? If not, at least it should be apples-to-apples on paper.

Here are currently-available Whetstone and Dhrystone procedures for the MC68020 and the 80386 32-bit processors. To use industry-standard methods of comparison, you'll have to—must—rerun the Whetstones and Dhrystones for the '386 along the same universally-accepted lines as for the '020.

And discover which has the greater potential for being a keystone and which for being a millstone in your new design. The MC68020 is *still* the highest-performance microprocessor no matter how you slice it!

WHETSTONE PERFORMANCE

The Whetstone is a standard double-precision, floating-point benchmark written in FORTRAN.

MC68020/68881

- Execution of standard Whetstone benchmark written in FORTRAN: recognized and run by all leading systems manufacturers (Cray, DEC, IBM, etc.).
- Double-precision floating point: specified by standard Whetstone for high accuracy.
- Complete, 10-loop-count execution: 1 million Whetstone instructions.
- Unary instructions executed: specified by standard Whetstone; single-operand operations.



- Entire Whetstone benchmark procedure was not modified from the original standard: no tricks or tweaks to hype performance.
- Result: 1.24 million Whetstones/second with commercially-available silicon (68020, 68881).

80386/80387

- Execution of vendor-modified Whetstone benchmark written in C: nobody else in the industry uses this particular procedure.
- Single-precision floating point: non-standard Whetstone sacrifices accuracy for "performance."
- Incomplete, 2-loop-count execution: only 200,000 Whetstone instructions.
- No unary instructions executed: intentional '386-vendor modifications to Whetstone spec avoids single-operand operations.
- Altered Whetstone benchmark procedure allowed '386 vendor more favorable results: avoided branch control overhead.
- Result: Claims that provide no ability for apples-to-apples comparison.



DHRYSTONE PERFORMANCE

The Dhrystone Benchmark measures CPU performance on a typical mix of high-level language statements.

MC68020

- Dhrystone results measured on commercially-available system: Sun Microsystems 3/200 workstation.
- Commercially-available operating system (UNIX®).
- Commercially-available UNIX® C compiler (cc).



- Real-world memory architecture: Dhrystone WRITE operations must pass through to main-memory DRAM.
- Result: 6362 Dhrystones with commercially-available, real-world systems.

80386

- Dhrystone results measured on specially-modified "hot box" built by '386 vendor: '386 "starter kit" version not commercially available.
- No operating system used: '386 vendor used own modified debug monitor.
- '386 Vendor used own internal "beta" version of C compiler: not commercially available.
- Utopian memory architecture: zero-wait-state WRITE operations to unlimited cache SRAM—no write through to main memory.
- Result: Claims that provide no ability for apples-to-apples comparison.



UNIX is a registered trademark of AT&T.

For an engineer-to-engineer or senior-manager-to-senior-manager update on the real 32-bit system products, call toll-

1-800-521-6274

free any weekday. If the call can't cover your needs, we'll have the appropriate person get in touch.

For more information on the MC68020,

and an apples-to-apples comparison, send the coupon to Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, AZ 85036.

We're
on your
design-in
team.



MOTOROLA

To: Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, AZ 85036

Please send me more information on the MC68020 32-bit system solution and apples-to-apples comparisons.

289BYTE040087

Name _____

Title _____

Company _____

Address _____

City _____ State _____ Zip _____

Call me (_____) _____



We designed our V.32 modem on the premise that speed is useless without reliability.

At Codex, we understand that all the speed in the world won't get you anywhere if you can't depend on it. And that's why we developed our V.32 modem to give you 9600 bps full-duplex dial transmission, rivalling the reliability of a dedicated leased line.

Admittedly a pretty big claim.

But then, it's really what you'd expect from the recognized leader in high speed modems. In fact, more data communications professionals prefer Codex than any other brand.* And it's our high speed modem expertise that has allowed us to make a modem that not only meets, but exceeds the V.32 standard.

Our V.32 modem uses the same VLSI technology and forward error correction scheme (Trellis Coded Modulation) as our high speed leased line modems that reliably transmit data up to 19,200 bps.

So, you can be sure of continuous high quality transmission over a wide

range of line conditions. This now allows you to cut connect time and save money by sending data at up to 9600 bps full duplex over ordinary dial lines.

We've even added a proprietary long haul echo cancellation feature, eliminating both local and distant echoes that can plague dial networks. So even if the phone company sends your data over satellite links, it arrives intact.

Plus our V.32 modem includes a soft strap front panel, multiple ACUs, a nest card option for maximum space savings, and operates in synchronous or asynchronous applications.

To find out more about the Codex V.32 modem, call 1-800-426-1212, Ext. 235. Or write Codex Corporation,

Dept. 707-35, 7 Blue Hill River Road, Canton, MA 02021-1097. You'll discover

that when we tell you about a V.32 with high speed performance and

reliability, we're not blowing smoke.

codex

 **MOTOROLA**



*McGraw-Hill's Data Communications Brand Preference study cites Codex as offering the best technology, best price performance ratio, best service organization, and most informative literature for various modem, multiplexer and network control product categories. © 1986 Codex Corporation. Motorola and  are trademarks of Motorola, Inc. Codex is a registered trademark of Codex Corporation.



An Evolutionary Quartet of AT Clones

Wayne Rash Jr.

These clones are
more remarkable for similarities
than for differences

The original IBM PC AT was introduced in 1984. Three years later IBM, NEC, Tandy, and Hewlett-Packard have each taken that original design and speeded it up, created new keyboards, and added enhanced graphics adapters and monitors. In using the original PC AT design, each company sought to improve it and to make its computer distinctive from the rest. All these evolutionary changes are a mixed blessing since some of the features of the original PC AT, such as a satisfactory keyboard layout, have been changed.

These four new computers, the 8-MHz IBM PC AT (upper left), the NEC APC IV (upper right), the Tandy 3000 HD (lower left), and the HP Vectra (lower right), differ in size, compatibility, and ease of use. However, they are as alike in performance as any group I've ever tested.

Similarities

The 8-MHz IBM PC AT and the three clones are more remarkable for their similarities than for their differences. All of them have the same capabilities, run at the same 8-MHz speed (except for the NEC APC IV, which is switchable between 6 and 8 MHz), and have the same basic internal and external design. Each has a 20-, 30-, or 40-megabyte hard disk drive, a 1.2-megabyte high-capacity floppy disk drive, and an 8-MHz version of the Intel 80286 processor. Each also has 640K bytes of RAM except for the new PC AT, which has 512K. The new PC AT that I reviewed came with an optional 360K-byte floppy disk drive, although this does not come standard with the computer. Also, each machine was delivered with an optional enhanced graphics adapter and an enhanced graphics color monitor. The principal differences

among the units are in external size, internal space, and ease of use. There are also differences in standard accessories and bundled software.

IBM PC AT

The new IBM PC AT (\$5295) can't technically be described as a clone, but it is a derivative of the original design. Its large size allows you to mount two floppy disk drives and two hard disks internally. However, the unit takes up a lot of space on a desktop—so much that you may want to consider mounting it sideways next to your desk. The larger size might be inconvenient, but it is an advantage if you need that many disk drives. The motherboard has eight slots; five are left open for future expansion. This is one area where I would consider the larger size to be a worthwhile trade-off.

The PC AT is equipped with a front-panel key lock. This device locks the case shut and disables the keyboard. While it won't prevent criminal activities, it will prevent casual snooping and carelessness. This is an item that should be on all PCs.

The PC AT keyboard has always had excellent tactile feedback, and the enhanced keyboard carries on that tradition. Regrettably, the layout takes the IBM PC's history of unfortunate design and expands on it. The sad part about this is that the original keyboard layout for the PC AT was significantly better.

Specifically, in the new layout IBM has moved some of the keys around and has added two small keypads for editing commands and cursor control. The Ctrl and Alt keys are now on the same row as the space bar, which is now shorter. The 12 function keys form a row along the top of the keyboard. The SysRq key has been made a secondary function.

The result of all these changes is that some programs have become much harder to use. WordStar's control codes, for example, are now difficult to enter because you have to stretch one finger down to the lower left corner in order to press the Ctrl key. Your only other option is to use two hands where one was once sufficient. To make matters worse, the Caps Lock key has been moved next to the A key, where the Ctrl key is located on most

continued

Wayne Rash Jr. is a member of the professional staff of American Management Systems Inc. (1777 North Kent St., Arlington, VA 22209), where he consults with the federal government on microcomputers.



IBM PC AT

Company

IBM Corp.
113 Westchester Ave.
White Plains, NY 10604
(800) 447-4700

Size

21 ¼ by 16½ by 6¼ inches
51 pounds

Components

Processor: 80286 running at 8 MHz with one wait state

Memory: 512K bytes, expandable to 16 megabytes

Mass storage: One half-height 1.2-megabyte 5¼-inch floppy disk drive or one 360K-byte floppy disk drive and a 30-megabyte hard disk

Display: Optional 12-inch green monochrome, EGA, or RGB; 80 characters by 25 lines

Keyboard: 101 keys; 12 function keys; indicator lights for Caps Lock, Scroll Lock, and Num Lock keys

I/O interfaces: Eight slots—two IBM PC compatible; six PC AT compatible; one serial and one parallel port

Software

BASIC in ROM

Documentation

Guide to Operations, 192 pages

Price

\$5295

NEC APC IV

Company

NEC Information Systems Inc.
1414 Massachusetts Ave.
Boxborough, MA 01719
(617) 264-8000

Size

21 ½ by 16½ by 6½ inches
40 pounds

Components

Processor: 80286 running at 6 or 8 MHz with one wait state

Memory: 640K bytes, expandable to 10 megabytes

Mass storage: One half-height 1.2-megabyte 5¼-inch floppy disk drive or one 360K-byte floppy disk drive and a 20- or 40-megabyte hard disk

Display: Optional 12-inch monochrome, EGA, or RGB. 80 characters by 25 lines

Keyboard: 84 keys; 10 function keys; indicator lights for Caps Lock, Scroll Lock, and Num Lock keys

I/O interfaces: Eight slots—two IBM PC compatible; six PC AT compatible; two serial ports and one parallel port

Software

MS-DOS 3.11; GW-BASIC

Documentation

MS-DOS User's Guide, 346 pages

GW-BASIC User's Guide, 326 pages

Price

\$5420

Tandy 3000 HD

Company

Tandy Corp.
1800 One Tandy Center
Fort Worth, TX 76102
(817) 390-3700

Size

19 by 18 by 6½ inches
26 pounds

Components

Processor: 80286 running at 8 MHz with one wait state

Memory: 640K bytes, expandable to 1 megabyte on motherboard (12 megabytes under XENIX)

Mass storage: One half-height 1.2-megabyte 5¼-inch floppy disk drive or one 360K-byte floppy disk drive and a 40-megabyte hard disk

Display: Optional 12-inch monochrome, EGA, or RGB; 80 characters by 25 lines

Keyboard: 101 keys; 12 function keys; indicator lights for Caps Lock, Scroll Lock, and Num Lock keys

I/O interfaces: Ten slots—three IBM PC compatible; seven PC AT compatible; one serial and one parallel port

Software

None

Options

MS-DOS 3.2; GW-BASIC; DeskMate II

Documentation

Installation and Operation Manual, 123 pages

MS-DOS Handbook, 73 pages

Price

\$4299

keyboards. A number of programs that depend on standard PC AT key positions are going to be difficult to use with this keyboard unless the program can re-assign keys.

The initial computer that I received for this review was so unreliable that I had to swap it for a new one to complete the re-

view. The first unit suffered a series of hard disk crashes, even after I replaced the hard disk. I was not able to determine a specific cause for the hard disk failures. The original IBM PC AT has also had a history of hard disk problems. The problem did not occur with the replacement unit.

NEC APC IV

Of the four computers in this review, the NEC APC IV (\$5420) is the one I preferred in terms of overall quality. Unlike the new PC AT, the APC IV has a keyboard based on the older PC AT standard, and the hard disk drive caused no problems. The chassis is approximately the

HP Vectra

Company

Hewlett-Packard Co.
974 East Arques Ave.
Sunnyvale, CA 94086
(800) 367-4772

Size

16¾ by 15½ by 6¾ inches
26 pounds (with one floppy disk drive)

Components

Processor: 80286 running at 8 MHz with one wait state
Memory: 640K bytes, expandable to 3.64 megabytes
Mass storage: One half-height 1.2-megabyte 5¼-inch floppy disk drive and a full-height 40-megabyte hard disk
Display: Optional 12-inch monochrome, EGA, or RGB; 80 characters by 25 lines
Keyboard: 103 keys; 18 function keys; indicator lights on bezel for Caps Lock, Scroll Lock, and Num Lock keys
I/O interfaces: Seven slots—two IBM PC compatible; five PC AT compatible; one serial and one parallel port.

Software

None

Options

MS-DOS 3.1; Personal Application Manager; Executive MemoMaker; Executive Card Manager; Charting Gallery; Drawing Gallery; HP Mouse

Documentation

Using Vectra, approximately 300 pages; *Vectra MS-DOS User's Reference*, approximately 375 pages

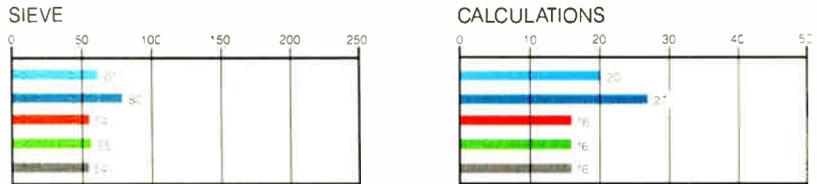
Price

\$5495

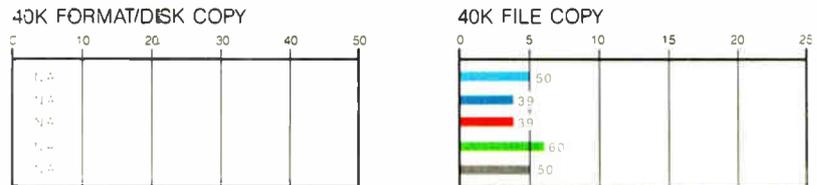
DISK ACCESS IN BASIC (IN SECONDS)



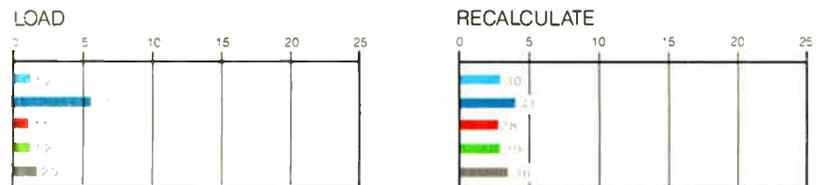
BASIC PERFORMANCE (IN SECONDS)



SYSTEM UTILITIES (IN SECONDS)



SPREADSHEET (IN SECONDS)



Legend:
■ IBM PC AT (8 MHz) ■ IBM PC AT (6 MHz)
■ NEC APC IV ■ TANDY 3000 HD ■ HP VECTRA

The graphs for Disk Access in BASIC show how long it takes to write and then read a 64K-byte sequential text file to a hard disk. (For the program listings, see BYTE's *Inside the IBM PCs*, Fall 1985, page 195.) The Sieve graph shows how long it takes to run one iteration of the Sieve of Eratosthenes prime-number benchmark. The Calculations graph shows how long it takes to do 10,000 multiplication and 10,000 division operations using single-precision numbers. The 40K Format/Disk Copy benchmark was not performed because all the computers had only one 1.2-megabyte floppy disk drive. The

40K File Copy graph shows how long it takes to copy a 40K-byte file using the DOS COPY command. The Spreadsheet graphs show how long it takes to load and recalculate a 25- by 25-cell spreadsheet in which each cell equals 1.001 times the cell to its left. The spreadsheet used was Microsoft Multiplan. Tests on the two IBM PC AT computers were done using PC-DOS 3.2 and BASIC; the NEC APC IV used MS-DOS 3.11 and GW-BASIC; the Tandy 3000 HD used MS-DOS 3.11 and GW-BASIC; and the HP Vectra used MS-DOS 3.1 and GW-BASIC.

same size as that of the PC AT. The motherboard has eight slots, with five available for expansion. The APC IV is a dual-speed machine; you must move a slide switch to change speeds from 6 to 8 MHz. It is also the quietest of the group.

The touch of the APC IV keyboard is crisp with an excellent tactile feedback,

and the layout of the original PC AT keyboard has been retained. At about ¾ inch in thickness, the keyboard is slimmer than the others. In addition, because the bezel extends only slightly beyond the keys, it takes up less space on your desk.

The NEC Enhanced Graphics Monitor that accompanied the APC IV that I re-

viewed was the best in this group of excellent monitors. The characters on the screen were crisp and fully formed, and they seemed slightly easier to read than those on the other monitors. The NEC monitor is mounted on a stand that allows tilting and swiveling.

continued

These machines are fast, relatively quiet, and easy to use.

Like the PC AT, the APC IV has a key lock to protect your machine. However, unlike the PC AT, the key lock on this unit has a reset position. This allows you to invoke a hardware reset without having to turn the machine off. The lock assures that resets won't be accidental.

Tandy 3000 HD

The Tandy 3000 HD system unit (\$4299) is slightly smaller than the PC AT and the APC IV. This conserves desk space, but the computer can hold only three disk drives. Tandy makes good use of the available internal space, however, by providing ten expansion slots, seven of which are available for use. This is the largest number of available slots in any of the four machines. To cool this large unit, the computer has two fans, making the 3000 HD the noisiest of the quartet.

The 3000 HD's front panel does not have a key lock, but it does have a reset switch. All four machines should have both, but of the two, the reset switch is more useful.

Tandy followed IBM exactly when it came to laying out the 3000 HD keyboard, but not when it came to providing tactile feedback. The keys feel like they are mounted on foam rubber and give poor tactile response.

The enhanced graphics monitor supplied with the 3000 HD also has its flaws. Unlike the monitors supplied by other companies, which have a matte screen finish, the 3000 HD monitor has a very shiny finish. This caused viewing problems due to reflections on the screen.

HP Vectra

The HP Vectra (\$5495) is the smallest of the four computers. Accordingly, it also has the least interior space for drives and boards. The keyboard is Hewlett-Packard's own design and does not resemble either the original or the enhanced PC AT keyboard. It features ten function keys down the left side, eight function keys across the top, and separate cursor and numeric keypads on the right side.

The HP Vectra's small size will save you some desk space, but in this case you've got to compromise quite a bit. There is room for only two disk drives and seven expansion slots, with four available for expansion. If you get the hard disk version of the HP Vectra, all the disk drive space is taken, and you will

need an expansion chassis to add more.

Another area of compromise is compatibility. While most software for the IBM PC AT will run properly on the HP Vectra, there may be some isolated problems. For example, I could not get Fox Research's 10-Net, a local area network package, to run. I suspect that some of the incompatibility is due to the section of ROM BIOS provided by Hewlett-Packard. The remainder of the ROM BIOS is provided by Phoenix, and normally it does not cause compatibility problems.

Hewlett-Packard also has areas of incompatibility with itself. You need to run a program called Patch to support the operation of the HP EGA card. Worse yet, Hewlett-Packard's own graphics program, Drawing Gallery, would not work with the HP EGA or the HP Mouse at first. The mouse itself is Hewlett-Packard's own design and is not completely compatible with other mouse-oriented software.

Hewlett-Packard has provided the HP Vectra with a DOS shell program called the Personal Application Manager. This is a menu-driven system that allows you to move a highlighted cursor around with the arrow keys or a mouse and then press Return to invoke a function. The program's documentation mentions support only for the HP Mouse. I tried using the Microsoft Mouse with the HP Vectra, but the cursor became very touchy to even the slightest movement, and this made it very hard to control. The HP Mouse was much easier to control.

You can move around the menus with the mouse, but you can't run all the applications that you can call. The setup program, for example, will not work with the mouse.

Setting Up

The setup procedures for getting these four machines running differed, but with the exception of the 3000 HD, the process was quick and relatively easy. Each of the systems provides a menu for you to choose the setup alternatives, and you simply make the appropriate choices. All the machines also require you to partition the hard disk and determine the boot partition.

Because PC AT clones have such a wide variety of equipment that can be installed in them, you need to have more information about the individual components than you do to set up a PC or PC clone. The setup programs require that you know the type of drive that is installed or the number of heads and cylinders that the drive has. Normally, the drive type is posted on the outside of the drive.

Tandy makes the setup process much

harder by requiring you to run a low-level format program as the first step in preparing the hard disk. This program requires that you enter the list of bad tracks on the disk by typing in the number of the head and the track that's defective. The list is attached to the floppy disk drive cover inside the computer. In my review unit, several entries listed on the error map as being bad produced an error message, indicating that there was no such cylinder. The formatting program refused to accept these entries, and I had to skip them entirely.

According to the bad-track list that accompanied the 3000 HD, the computer's hard disk had 23 bad tracks. This is a relatively high number; most hard disks have only two or three. The format program handled all 23 bad tracks when it prepared the disk for MS-DOS. However, I encountered problems when I tried to format the disk for use with Concurrent PC DOS; the format program simply would not accept a hard disk with that many bad tracks. [Editor's note: *Tandy will repair or replace a hard disk found to have an excessive number of bad tracks.*]

Tandy compounds the setup process by requiring you to move a jumper inside the machine if you plan to use an enhanced graphics adapter. Hewlett-Packard, on the other hand, doesn't mention the EGA in its standard documentation; it instead tells you how to hook up separate cables to drive an RGB monitor. Instructions for using the Hewlett-Packard EGA are covered only in a separate manual.

Using the ATs

These machines are fast, relatively quiet, and easy to use. They all have sufficient hard disk space, run the same software, and are even the same shade of beige. The primary difference is the keyboards. Because keyboard selection is very subjective, you should try each keyboard yourself.

Once you have loaded whatever software you plan to use, running these machines is very simple. Since they all have hard disks, you need only turn them on. The HP Vectra starts more quickly than the others because it dispenses with the display of the memory test. The other computers display each 64K bytes of RAM as it is tested. The more memory you have installed in your computer, the longer this process takes.

I tried a variety of business software packages on these machines, including WordStar, dBASE II and III, Lotus 1-2-3, and Framework. They all performed properly. The Hewlett-Packard graphics software had problems running on the HP Vectra, but this was due to an installation

problem. A few packages, including poly-COM/240, a communications package, had trouble with the enhanced keyboard on the PC AT and the 3000 HD because the software designers had set things up for the original PC AT keyboard.

The only other operational consideration of any significance is the speed of the microprocessors. All four computers run at 8 MHz. Unfortunately, a few programs have copy-protection schemes that work only on a PC AT with a 6-MHz clock rate. The switchable speed on the APC IV avoids that compatibility problem. Presumably, newer software will have this problem fixed.

There are few differences in compatibility beyond those I've noted. I was able to use 360K-byte double-density disks formatted in the high-capacity 1.2-megabyte drives of all the review machines in any of the other MS-DOS computers I have access to. The PC AT that I reviewed was delivered with both a 1.2-megabyte high-capacity drive and a 360K-byte double-density drive, which eliminated any problems with disk compatibility. All the review units were delivered with a version of MS-DOS 3.1 or PC-DOS 3.2.

Documentation

Like the machines themselves, the documentation for these computers is fairly uniform. All the machines include a booklet that tells you how to connect the keyboard and monitor, how to run the setup program, and where to find out about disk formatting and loading MS-DOS. In addition, all the review machines came with an MS-DOS manual and a manual for BASIC, if the language is included. The PC AT and the HP Vectra units I reviewed both included a separate optional hardware operations manual.

All the manuals are clearly written, and they all matched the machines that they were shipped with, except for the HP Vectra, which had a supplementary manual for the EGA card and monitor. The start-up guide for the APC IV is particularly well done with excellent color photos detailing every step of the installation process. The other manuals use drawings and sketches that serve their purposes well.

Benchmarks

In keeping with their other similarities, these machines all performed at much the same speed in the benchmarks. The HP Vectra was somewhat faster than the others in the Disk Access in BASIC Write benchmark on the hard disk, but it ran at about the same speed in the corresponding Disk Access in BASIC Read test. The PC AT was slightly slower in the BASIC

Performance Calculations and Sieve benchmarks. This difference in speed seems to be related to the PC AT's ROM BASIC, since the difference did not show up in the Spreadsheet Recalculate benchmark. The HP Vectra, however, was slightly slower than the others in the Spreadsheet Load test. See page 219 for the complete benchmark results.

The Final Verdict

You can safely select from any machine in this group on the basis of personal preference, keyboard feel, or price. There are

very few operational differences among them, and those that exist are minor. The only serious hardware problem I had was with the PC AT, although Tandy's long hard disk bad-track list could have caused a problem.

In short, these are fast, capable machines that will meet most business needs. The differences in their performance are so slight that you might as well choose on the basis of the dealer or the way you feel about the individual brand. Any of them should provide satisfactory service. ■

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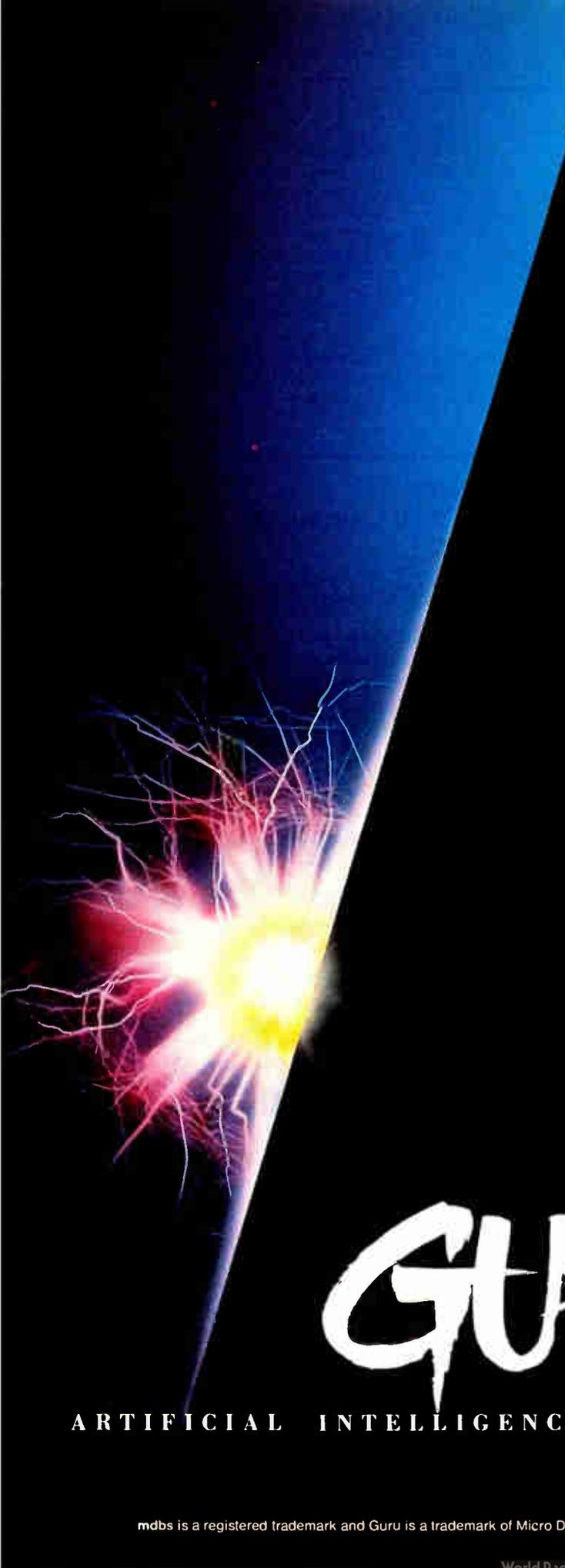
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The Apple IIGS

Philip Chien

Graphics and sound capabilities, expanded memory capacity, and more

When you purchase an Apple IIGS you get the system unit, a detachable keyboard, a mouse, the ProDOS 8/16 utilities, and documentation for \$999. The IIGS comes with 256K bytes of memory on the motherboard, two serial ports, a mouse port, 40-/80-column RGB and composite video output, a real-time clock, and a smart disk controller that supports both 800K-byte 3½-inch and 143K-byte 5¼-inch floppy disk drives. You will need to purchase at least one 3½-inch disk drive (\$399) because the system software comes on 3½-inch disks. You will also need to purchase a monitor: RGB, composite, or monochrome. See page 226 for a list of options and their prices.

Detachable Keyboard

I found the keyboard to be one of the nicest features of the IIGS; it is easy to use, reliable, and comfortable. Unlike the Apple II keyboards, the Apple IIGS's keyboard is detachable and includes a built-in numeric keypad. Most users will enjoy the convenience of a standard keypad but, as a left-handed person, I miss a detachable keypad that can be placed where it's convenient. The layout of the keyboard is similar to that of the Apple IIe, although some changes have been made: A couple of minor keys have been rearranged, and the closed Apple key has been renamed the Option key for compatibility with the Macintosh. The Reset key has been placed at the top of the keyboard in a position where it is almost impossible to hit by accident, but easy to reach if necessary.

The Apple IIGS includes built-in keyboard maps and character sets for seven foreign languages and the Dvorak keyboard arrangement. Because the keys are all made from the same mold, it is practical to remove the key caps and move them

to the correct positions for the layout you choose. On a sculpted keyboard like that of the Apple IIe, the key caps are not designed to be moved, and a keyboard will feel "lumpy" if you swap the keys.

System Design

The IIGS's microprocessor is Western Design Center's 65C816, which is capable of operating in 16-bit native mode or in 6502-emulation mode. The 65C816 can address up to 16 megabytes of memory—256 banks of 64K bytes each—and it can operate at either 1 or 2.8 megahertz. The slower speed may be required for Apple II games and hardware that rely on a system speed of 1 MHz for proper operation. [Editor's note: *In this article, "Apple II" refers to the entire Apple II series, which consists of the Apple II, II+, IIe, and IIc.*] The IIGS cannot take

advantage of the full address space of the 65C816; it is expandable up to 8 megabytes only. The 65C816 is software-compatible with the 6502, and anyone who can program the 6502 should have no problem programming the 65C816.

On the Apple IIGS, most of the circuitry that needed 70 TTL chips on the original Apple and 20 chips on the Apple IIe has been shrunk into one surface-mount-device (SMD) chip named the Mega II [Editor's note: See "*The Apple IIGS*" by Gregg Williams and Richard Grehan in the October 1986 *BYTE* for more information on the Mega II]. The SMD design means the IIGS will be much more reliable than earlier Apple machines since there are fewer components to fail. Unfortunately, because the SMD chips are soldered to the motherboard, the entire motherboard must be replaced if repairs become necessary.

The IIGS has seven IIe-compatible multipurpose expansion slots and a dedicated memory-expansion slot that supports up to 8 megabytes of RAM. Each of the IIe-compatible expansion slots has a default assignment to one of the built-in I/O functions: Slot 1 is set to the printer port, slot 2 is set to the serial modem port, slot 3 is for the 80-column display, slot 4 is for the mouse, slot 5 is set to the 3½-inch disk drives, slot 6 is set to the 5¼-inch disk drives, and slot 7 is set to AppleTalk. If you want to place an expansion board into one of the slots, you have to give up the built-in function as-

continued

Philip Chien (Earth News, 3094 Coney Island Ave., Brooklyn, NY 11235) is a freelance author who has written over 150 articles about the space, video, and computer industries.



signed to whatever slot you choose.

In addition, the IIGS has a game I/O port, a sound-interface port, and the desktop bus. The game port is available as a 16-pin socket inside the machine and a DB-9 connector at the rear of the unit. The sound-interface port is a 7-pin connector on the IIGS motherboard that can be attached to an audio processor; the desktop bus is a mini-DIN 4-pin serial connector that attaches the keyboard, mouse, and other input devices to the IIGS.

Externally, the IIGS's connectors look more like a Macintosh Plus's than an Apple II's (see photo 1). Both serial ports use the Mac Plus's sub-8 connector, a miniserial connector that eliminates handshaking and DCE-to-DTE problems. Apple's sub-8 cables have a built-in crossover circuit, and the same cable that attaches an Apple to a printer can attach an Apple to a modem, one Apple to another, or even a printer directly to a modem for remote applications. For compatibility with other equipment, adapter cables are available for other products that use standard DB-25 connectors. The SmartPort is a set of routines for controlling block I/O devices such as 3 1/2-inch and 5 1/4-inch floppy disk drives, but you can also use it for a variety of block applications including working with hard drives and file transfer.

Hard drives are not considered an integral part of the IIGS's structure, but they are available as options. A hard drive can operate off the built-in SmartPort, the AppleTalk serial port, an SCSI interface, or a custom interface card. Hard drives are available in internal, external, and multiuser network models. Apple sells a 20-megabyte external SCSI drive, the Apple Hard Disk Drive 20SC (\$1299),

and the Apple II SCSI Controller Card (\$129).

For the first time, Apple is offering a system fan as an option (\$49), and it is recommended if you have more than three interface cards or more than a megabyte of RAM.

Firmware and Memory

The Apple IIGS has more built-in ROM than any other Apple II—128K bytes. This 128K contains Applesoft BASIC, a resident toolbox, resident desk accessories, I/O interface routines, the SmartPort protocol converter, the AppleTalk driver, the monitor, and a general set of I/O driver routines.

The toolbox routines are similar to those found in the Macintosh and include graphics, sound, calculations, and other utilities. The desk accessories include a Mac-like Control Panel that lets you set up the various defaults in the IIGS. The Control Panel also lets you choose the color of the text and display; set the time; configure the slots, serial ports, and the RAM disk; choose the keyboard layout and language; set the system speed (either 1 or 2.8 MHz); and even adjust the volume and pitch of the speaker's beep. A battery-protected portion of memory stores the Control Panel data and powers the IIGS's clock.

The IIGS employs an expanded version of the Monitor, which is the set of bottom-level programming and access utilities built into the Apple. The mini-assembler and the disassembler are both improved and use all the 65C816 op codes. Figure 1 compares an improved IIGS disassembly listing with the same code disassembled on an earlier Apple. It's quite easy to use the monitor to examine memory, change memory, or write a

quick program. The new monitor functions include pattern search, ASCII input, toolbox calls, store and restore registers, a hex/dec converter, a hex/ASCII dump, and direct access to the clock. The step and trace functions, which have been missing in every Apple since 1980, have returned in the IIGS.

Depending on which video modes and operating systems you use, anywhere from 64K to over 200K bytes of RAM is available for your programs. Under the 6502 8-bit mode, extra memory beyond 64K is accessed as a RAM disk. Under the 65C816 16-bit mode, all the expansion memory is configured as one continuous bank of memory. Booting Applesoft on a standard unexpanded IIGS gets you 56K bytes free—the same amount of free space you would get with a 128K-byte IIe. When you enter Applesoft BASIC, you still have only 47K of free space and 36K free with ProDOS installed, which is the same amount of space you would have with the IIe.

The IIGS includes a special slot just for memory expansion. Apple sells a 256K-byte memory-expansion card (\$129) that can be upgraded to 1 megabyte of RAM (\$336), but third-party manufacturers have more powerful and less expensive memory boards. For example, Applied Engineering sells two different expansion boards: The GS RAM board, with a megabyte of RAM, costs \$299 and can hold up to 1.5 megabytes of RAM using 256K-bit RAM chips. The GS RAM Plus board costs \$599 with a megabyte of RAM and can be expanded to 8 megabytes using 1-megabit RAM chips. At the time of this writing, one megabyte of RAM retails for about \$300 (the same price as 16K bytes back in 1978), but prices are expected to come down.

Graphics and Sound

The IIGS supports all the current Apple text and graphics modes including 40- and 80-column text, lo-res graphics, hi-res graphics, double hi-res graphics, and combinations of mixed graphics and text. In addition, two new super hi-res modes have been added: either 320 by 200 pixels with 16 colors per line, or 640 by 200 pixels with 4 colors per line. You can select from a palette of 4096 colors. As with earlier Apple graphics modes, the horizontal resolution is limited to specific color choices, so the actual true horizontal resolution is half of what Apple claims [Editor's note: See "The Apple IIGS" in the October 1986 BYTE for more details.]

The IIGS's graphics modes may be typical of most good computers, but its sound capabilities are unmatched. An Ensoniq sound processor, which is also

continued

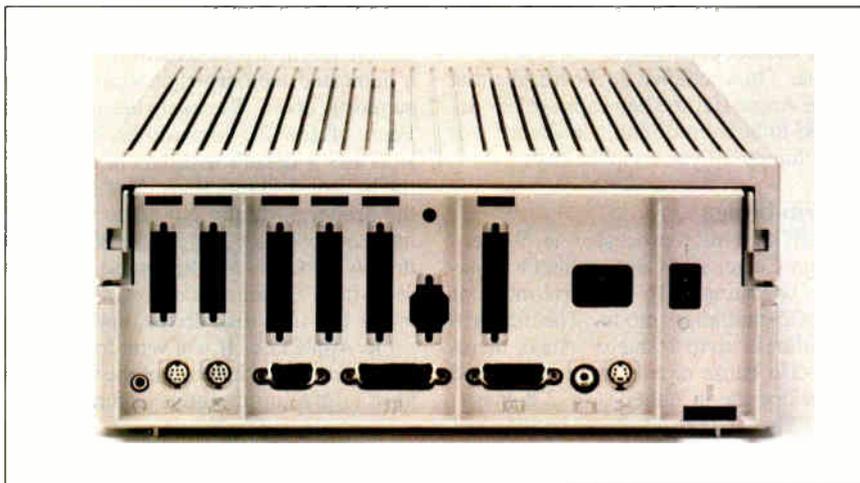


Photo 1: The back of the computer shows the wealth of built-in I/O. From left to right are the headphone jack, two serial ports, a joystick port, a disk drive port, the RGB and monochrome/composite video connectors, and the keyboard connector.

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Toshiba America, Inc., Information Systems Division

Apple IIGS

Company

Apple Computer Inc.
20525 Mariani Ave.
Cupertino, CA 95014
(408) 996-1010

Size

11 by 13¼ by 4½ inches; weight: 8¾ pounds

Components

Processor: 65C816, switchable between 1 and 2.8 MHz

Memory: 256K bytes of RAM, expandable to 8 megabytes

Mass storage: Purchased separately (see options)

Display: 40- or 80-column by 24-line text; 40- by 48-pixel or 80- by 48-pixel, 16-color lo-res graphics; 280- by 192-pixel or 560- by 192-pixel, 6-color hi-res graphics; 320- by 200-pixel, 16-color or 640- by 200-pixel, 4-color super hi-res graphics

Keyboard: Detached with 80 keys; built-in numeric keypad and cursor keys; one-button mouse that plugs into keyboard

I/O interfaces: Seven IiE-compatible slots; one dedicated memory-expansion slot; two serial ports; mouse port; RGB and composite video ports; smart disk controller; game I/O port; sound-interface port

Software

ProDOS 8/16 utilities; Applesoft II BASIC; tutorial

Options

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- 5¼-inch, 143K floppy disk drive: \$299
- 256K-byte memory-expansion card: \$129
- Apple Hard Disk Drive 20SC: \$1299
- Apple II SCSI controller card: \$129
- System fan: \$49

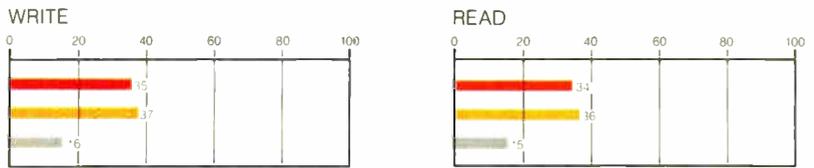
Documentation

200-page owner's guide; *Setting Up Your Apple IIGS*; *Apple IIGS System Disk User's Guide: A Touch of Applesoft BASIC*

Price

\$999

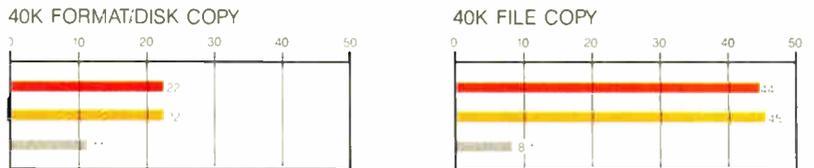
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■ APPLE IIGS ■ APPLE IIE ■ MACINTOSH PLUS

The graphs for Disk Access in BASIC show how long it takes to write and then read a 64K-byte sequential text file to a blank floppy disk. (For the program listings, see *BYTE's Inside the IBM PCs*, Fall 1985, page 195.) The Sieve graph shows how long it takes to run one iteration of the Sieve of Eratosthenes prime-number benchmark. The Calculations graph shows how long it takes to do 10,000 multiplication and 10,000 division operations using single-precision numbers. The System Utilities graphs show how long it takes to format

and copy a 40K-byte file using the system utilities. The Spreadsheet graphs show how long it takes to load and recalculate a 25- by 25-cell spreadsheet in which each cell equals 1.001 times the cell to its left. The BASIC tests for the IIGS and the Apple IIe were performed under Applesoft II BASIC; the spreadsheet tests for these machines were performed under Appleworks version 2.0. The spreadsheet used with the Macintosh was Microsoft Multiplan version 1.02, and the BASIC benchmarks were performed with Microsoft BASIC 2.0.

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The primary hardware change from earlier Apples on the IIGS is the serial ports: The IIGS uses the Zilog 8530 AICA.

used in the Ensoniq Mirage music synthesizer, forms the heart of the IIGS's sound circuitry. It has 64K bytes of dedicated RAM and generates music based on digital waveforms stored in memory, which can produce up to 32 separate voices simultaneously. Besides music, the sound circuitry can be used to record and produce excellent-quality speech and singing.

The music processor is actually a digital tape recorder: Input sound, with all its harmonics, is stored as a digital waveform. You can produce a waveform by calculating the wave with a mathematical formula, by loading a presaved waveform from a disk, by plotting, or by inputting from a musical instrument. For example, if you have a sound digitizer board and microphone, you can play a note on a French horn into the Ensoniq circuit and

save the waveform in RAM. You can then modify the waveform, producing notes higher or lower than possible with an actual French horn, or combine it with other notes or waveforms. Apple has licensed out all the waveforms available from Ensoniq and has made them available to developers.

I have seen a couple of demonstration programs that use the Ensoniq chip on the Apple IIGS—the dealer demo and a demonstration program for the Deluxe Music Construction Set by Electronic Arts. However, the only full-fledged music program that I have used is the Music Studio by Activision. Although this program is very impressive, it does not utilize the full capabilities of the Ensoniq chip. For example, it doesn't provide the ability to digitally record either sounds or speech.

Ironically, although the IIGS produces true stereo sound, the only audio output in the standard IIGS is a small mono speaker and a stereo plug with both connectors wired together. To get true stereo output, you can purchase a third-party board such as the Supersonic board (\$59.95) produced by MIDIdeas. It attaches to the IIGS's 7-pin sound-interface port, multiplexes the Ensoniq output into true stereo music, and amplifies it. All you need to add is a pair of speakers. MIDIdeas also sells a Digitizer board (\$39.95) that permits you to input music

to the IIGS through the Supersonic board.

Hardware Changes

The primary hardware change from earlier Apples on the Apple IIGS is the serial ports. Very early Apples used the Motorola 6850 asynchronous communications interface adapter (ACIA), which controls serial-to-parallel conversions. In 1980, the more powerful Synertek 6551 ACIA was used in the Apple III, the Super Serial Card, and the IIc's built-in serial ports. The Apple IIGS uses the Zilog 8530 ACIA, the same serial chip used in the Macintosh. Besides Macintosh and AppleTalk compatibility, the Zilog chip has more sophisticated interrupt-driven buffered firmware, making it easier to program. The extra registers on the 8530 make it possible to use MIDI, RS-422, and other high-speed serial protocols.

The disadvantage of the 8530 is that it is not directly compatible with programs that work directly with the 6551. Programs in this category are ASCII Express, Access II, and most other communications programs that work directly with the 6551. Printing programs in this category include Print Shop, Dazzle Draw, and Power Print. Most of these programs will work with no problems on the IIGS if you plug an old Apple Super Serial Card into the IIGS and toggle it on through the Control Panel.

The clock on the IIGS is not compatible with many programs designed to work with the clocks on earlier Apples. Earlier Apple clocks were peripheral cards that plugged into a slot, and they had specific locations where a program could call for the time. On the IIGS, the clock is an integral part of the system and does not have a slot allocated to it. The simplest way to access the clock is through the ProDOS time call, but you can also access the clock through the Toolbox, through the monitor, or directly.

There is no auxiliary slot in the IIGS since the 80-column display and extra memory are already built-in. Cards designed for the auxiliary slot will not work in the IIGS.

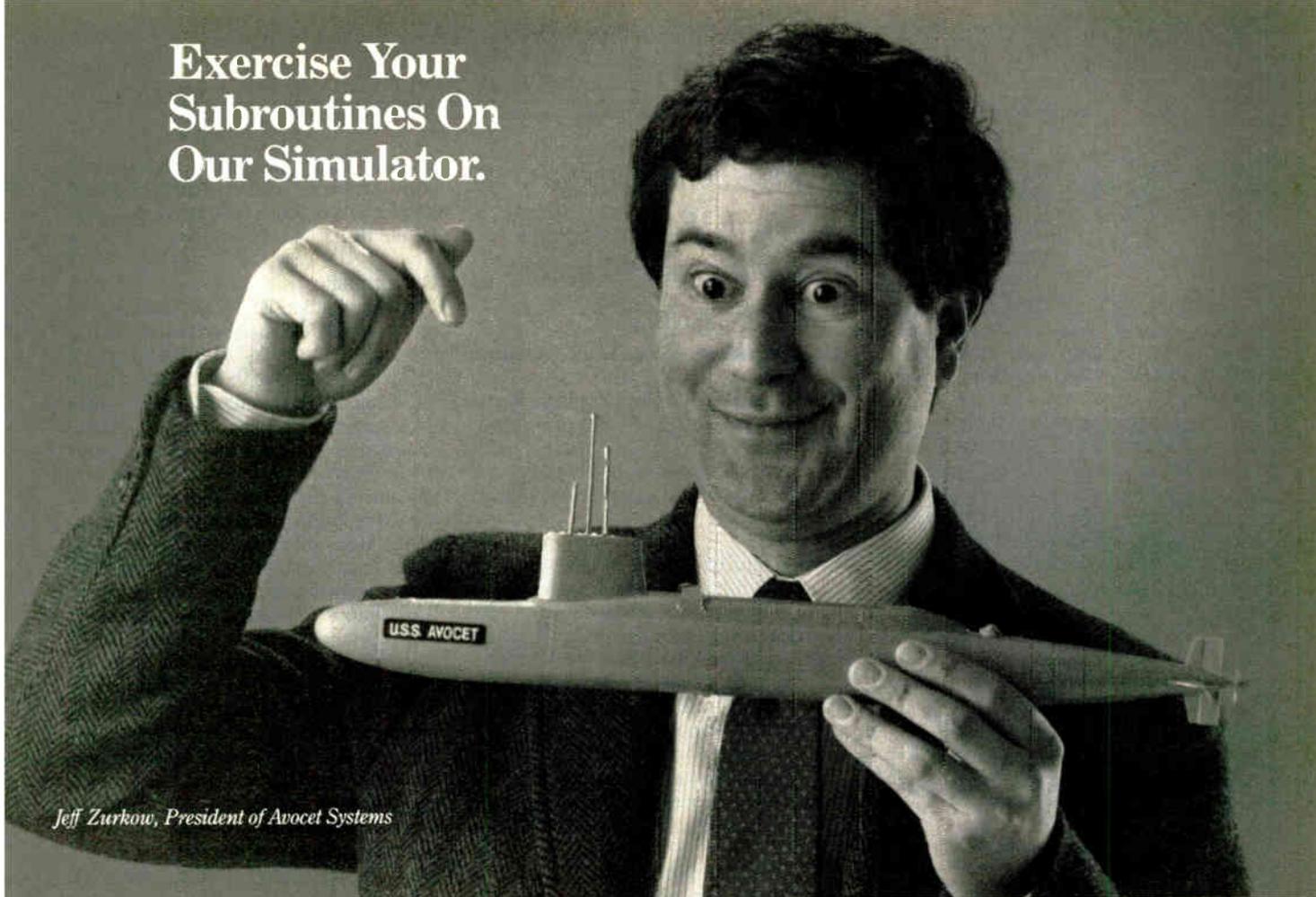
Most peripheral cards are not needed on the IIGS simply because the capabilities are already built-in (e.g., the mouse and the RGB video). Interface cards that use the direct-memory access line or phantom slot techniques (i.e., cards that pretend to be in more than one slot, like the Videx PSIO card and the Prometheus VERSAcad) will not work due to the larger memory map of the IIGS. Almost all other peripheral cards, including exotic I/O cards, digitizers, and co-processors, should work in the IIGS. I

continued

1a	1b
20001	*20001
1 = m 1 = x 1 = LCbank (0/1)	
00/2000: 85 01 STA 01	2000 - 85 01 STA \$01
00/2002: 20 D5 9E JSR 9ED5	2002 - 20 D5 9E JSR \$9ED5
00/2005: 20 00 BF JSR BF00	2005 - 20 00 BF JSR \$BF00
00/2008: E6 E6	2008 - E6 01 INC \$01
00/2009: 01 A5 A501	200A - A5 D0 LDA \$D0
00/200B: D0 EF BNE 1FFC {-11}	200C - EF ???
00/200D: 44 20 E1 MVP E120	200D - 44 ???
00/2010: 22 ED FE FF JSL FFFEEED	200E - 20 E1 22 JSR \$22E1
00/2014: 07 EA ORA [EA]	2011 - ED FE FF SB \$FFFE
00/2016: FC BE F2 JSR (F2BE,X)	2014 - 07 ???
00/2019: 73 40 ADC (40,S),Y	2015 - EA NOP
00/201B: 82 18 DF BRL FF36 {-20E8}	2016 - FC ???
00/201E: 12 62 ORA (62)	2017 - BE F2 73 LDX \$73F2,Y
00/2020: 71 30 ADC (30),Y	201A - 40 RTI
00/2022: 61 F0 ADC (F0,X)	201B - 82 ???
00/2024: 73 87 ADC (87,S),Y	201C - 18 CLC
00/2026: F7 38 SBC [38],Y	201D - DF ???
00/2028: 0C 90 6B TSB 6B90	201E - 12 ???
00/202B: 42 00 WDM 00	201F - 62 ???
00/202D: 00 D0 BRK D0	2020 - 71 30 ADC (\$30),Y

Figure 1: Identical code disassembled on the IIGS and the IIe. 1a shows the IIGS's new monitor features that support the 65C816, direct and relative branch addresses, and a status line at the top of the screen with the m, x, and LC registers. Note that the IIGS disassembly specifically supports the ProDOS MLI call (JSR \$BF00).

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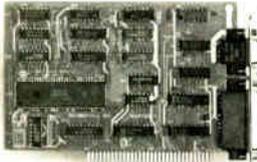
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REVIEW: APPLE IIGS

Compatibility on the Apple IIGS with earlier machines is excellent, but not perfect.

used the Computereyes Digitizer, Apple Cat Modem, PCPI CP/M Applicard, Microbuffer II+ parallel/serial card, Phasor Music and Sound Interface, and A/D converters with the IIGS without any problems.

Compatibility

The IIGS fully supports all the capabilities of a IIe and also provides access to the advanced features of the IIGS. Compatibility on the Apple IIGS with earlier Apples is excellent, but not perfect. If a program violates Apple's developer guidelines and uses illegal memory locations, it may fail on the IIGS. Examples of such programs are those that use unimplemented op codes of the 6502 or those that have jumps into the middle of ROM routines.

Apple claims that 95 percent of the currently available programs are compatible with the Apple IIGS. I converted the Brickout, hi-res demo, Applesoft I, and lo-res demo programs that came with my nine-year-old Apple from cassettes to disk, and they ran successfully without modification on the IIGS.

Other more recent programs also worked without any problems, such as Webster's New World Spelling Checker, BPI accounting, Mousepaint, various ProDOS utilities, assorted programming languages including UCSD Pascal, Manx C, and Sig Forth, and dozens of computer games, including Microsoft Flight Simulator.

Apple has given dealers a compatibility list that indicates which programs work directly with the IIGS, which ones have upgrades available, and which ones will not work.

Although 3½-inch floppy disk drives are considered the standard drives for the IIGS, 5¼-inch floppy disk drives are still available for users with large libraries of older floppy disks. All the IIGS drives support ProDOS 16, which is an enhanced version of the ProDOS 8 operating system, and the 65C816 processor, but programs originally designed for the IIe can also use the same enhanced capabilities.

Programs running on the IIGS operate about twice as fast as they would on a standard IIe, and 80-column displays are faster and scroll more smoothly. The

clock, sound chip, graphics, toolbox, and other enhanced features can all be supported by programs originally designed for the IIe.

Benchmarks

I ran the standard BYTE benchmark tests on an Apple IIGS using Applesoft BASIC version 2.0 at the fast (2.8-MHz) speed. The configuration of the IIGS I tested had an Apple RGB monitor, two 3½-inch drives, and a 256K-byte memory-expansion board. For comparison, the results of the tests are shown for the Apple IIe and the Macintosh Plus. The results of the Disk Access in BASIC benchmarks on the IIGS are close to the standard IIe times, but the microprocessor-intensive benchmarks on the IIGS, the Sieve and Calculations tests, are appreciably faster than those on a IIe. Applesoft BASIC does not take advantage of the faster instructions of the 65C816. Higher performance is possible using a programming language specifically designed for the IIGS such as the C language available with the Cortland Programmer Workshop package.

As another comparison, I ran the benchmarks on an Apple IIe with an Applied Engineering TransWarp card. This card has a 65C02C processor running at 3.5 MHz. The results for the Disk Access in BASIC tests were essentially the same as those for the standard Apple IIe, but the result of running the Sieve and Calculations tests were 81 and 31 seconds, respectively; the Spreadsheet Recalculate time was 7 seconds.

The Apple IIGS has the potential to be a powerful computer, but it needs a faster microprocessor and the ability to address more memory. If you are considering whether to buy a IIGS or a IIe, the IIe appears to be less expensive; the system unit with 128K bytes of memory and an 80-column card lists for \$829, versus the \$999 list price of the IIGS.

However, you have to then consider all the built-in devices of the IIGS. With a IIe you would have to purchase a floppy disk controller, I/O cards, a mouse and mouse controller, and a numeric keypad to get the same features that are built-in on the IIGS.

If you are making a choice between the IIGS and other computers such as the Macintosh, Amiga, and Atari ST, the IIGS does not have the programming power of the 68000 microprocessor. However, it can access more memory and is much more expandable. In addition, the IIGS has a database of over 25,000 Apple II-compatible programs ready to run and use as well as many new programs that are designed to use the new capabilities of the IIGS. ■

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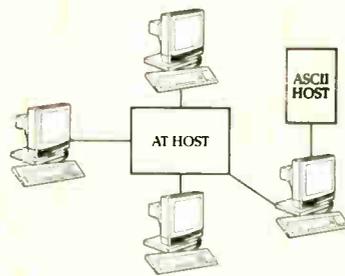


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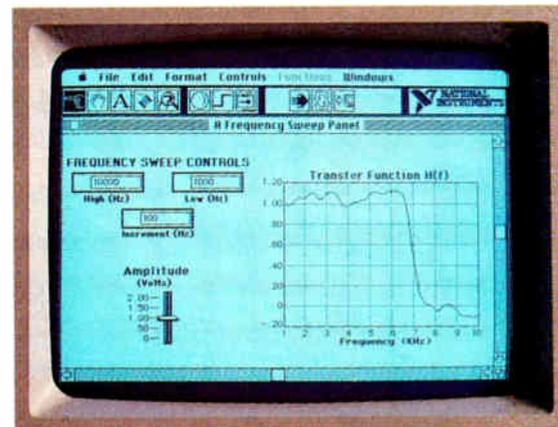
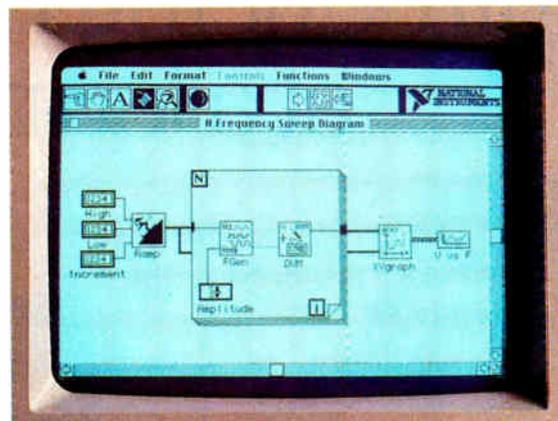
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Five OCR machines from CompuScan, Dest, Canon, IOC, and EIT

For years, optical character recognition (OCR) technology has struggled with the problem of reading the printed word. In the earliest days of the technology, the problem was so great that special fonts, called OCR-a and OCR-b, were created just for OCR machine reading. Although these special fonts worked, they represented the failure of the machines to read text produced by ordinary typewriters and printers.

The technology has improved, but in starting this review of five OCR machines, I still had some doubts about their ability. However, those doubts were cast aside when I tried the first machine. I was amazed to find that the CompuScan PCS 230 read, with only a 5 percent error rate, an old wrinkled letter that was typed in a font not even supported by the machine.

CompuScan PCS 230

The CompuScan PCS 230 (\$5695) is a large unit, about the size of an office typewriter. It has a rather flimsy front cover that you remove, flip over, and hook under a lip at the lower front of the machine to create a catch tray for the documents. The tray extends about 6 inches. You place the documents to be read in a metal holder on top of the machine.

The on/off rocker switch is located on the rear panel, which is difficult to reach. The other controls, scan/eject and stop, and the indicator lights for Ready and Run status are located on the front of the system under a plastic membrane.

The PCS 230 simply plugs into the wall and connects to the serial port of your IBM PC or compatible with a supplied cable. Software installation is simple. Unlike that of some other systems, the software is not memory-resident and does not run from within a word processor; it is a stand-alone program that creates files that are either compatible with most popular word processors or plain ASCII.

Unlike the other systems, the PCS 230 contains its own Motorola 68000 microprocessor. The 68000 removes the OCR's

dependence on the host computer's speed, allowing it to scan documents just as quickly for an IBM PC as it does for an IBM PC AT. The PCS 230 has a resolution of 200 dots per inch.

Clearing a paper jam from the PCS 230 is simple. A full-width cover simply lifts off, allowing access to the removable main roller. Reinstalling the roller is a bit more difficult; you have to make certain that the roller's gears are properly engaging the drive gears, but the entire operation requires no tools.

I did encounter one jam with the system, but I was pushing it to the limit trying to get it to read very wrinkled pages. The PCS 230 was the only unit that jammed, but it was also the only one that read really poor-quality test sheets, which tempted me to try scanning the badly worn pages in the first place. However, in scanning a stack of 40 pages, some worn and others new, I didn't encounter another jam.

Dest PC Scan

The Dest PC Scan (\$2885) is a very compact, solidly built unit that is meant to be placed on top of an IBM PC-style system unit and support a monitor. Paper feeds into a slot in the front of the unit one sheet at a time, and each sheet is returned through another slot just beneath the feed slot. The entire mechanism is enclosed, which might make removing a paper jam difficult, but I experienced no jams while operating the unit.

The on/off rocker switch is located on the rear of the unit, and the front has a display that indicates the condition of the machine.

The PC Scan has a resolution of 300 dpi, and it comes with software that requires 256K bytes of RAM. The unit con-

nects to a special board, which is small enough to go into a short slot of an IBM PC or compatible. Installation is straightforward except for the cable connector, which is surprisingly delicate and requires careful

handling.

The unit I reviewed did not work at first. After reinstalling the software several times, I called Dest's technical-support line. The technician spent nearly an hour working with me while I reinstalled the hardware and software several times. Finally, he suggested I inspect the connectors again, explaining that even a very slight bend on one of the pins could cause strange reactions in the software. I had already checked them once but, using a magnifying glass, I found that one of the pins on the board's connector had apparently been slightly bent during the previous installation. After several adjustments and switching the cable end-to-end, the unit operated perfectly. The real problem was that the connectors were poorly designed.

On power-up, the PC Scan performs diagnostics separately from the software, displaying the results by lighting a series of symbols and showing a number code on a large display.

Canon IX-12

The Canon IX-12 (\$1190) is a freestanding unit about the size of a small dot-matrix printer. Paper feeds through a slot on top of the unit and comes out through another slot just behind the input slot. A jam on this unit should be simple to clear because the top hinges up, exposing all the drive wheels. However, I experienced no paper jams.

Fortunately, I had little trouble installing the IX-12's IBM PC-compatible board into my computer and connecting the

continued

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scanner to the board. That was in spite of the fact that the 14-page documentation lacked information about the I/O address that the board required. The IX-12 has a resolution of 300 dpi.

The IX-12 uses a software package, OCR ReadRight, that's sold separately for \$595 and requires 384K bytes of RAM. OCR ReadRight is menu-driven and offers you the option of reading a number of documents into one file or renaming each document. Using this software is simple; different fonts can be mixed on one page, and you don't need to specify the fonts being used. As the hardware scans, the software displays a continuous readout of the text. If you wonder whether a certain font will be recognized, you can just look at the first few lines. If the font is not recognized, you can then press Escape to immediately cancel the scan, returning the software to its main menu and ejecting the page.

IOC Reader

Like the Canon IX-12, the IOC Reader (\$4295) from Intelligent Optics is, though somewhat larger, a freestanding unit with a paper feed and paper return on the top. The IOC Reader has a plastic tray for catching the output paper; I spent some time trying to discover how to install this tray (the documentation doesn't mention this) and finally gave up. According to Intelligent Optics, the same tray is used for several different scanner models. The one supplied with my review unit doesn't fit anywhere on the machine; you just shove it under the front of the unit.

The IX-12 connects to an RS-232C port on any computer. Unfortunately, I had some problems at first. My review unit did not work right away, and the documentation was not sufficiently detailed for me to determine whether the problems were with the scanner itself, the interface protocols, or the cables.

Eventually I got the unit operating, but only at the cost of partially disassembling the scanner and moving all the internal connectors. According to a technician at Intelligent Optics, this is a common problem. After the unit read only one page, I replaced its cover and found it was out of commission again. Twice more I was able to get the unit operating, but only for a minute or two at a time. I then asked the company for another unit.

The new machine appeared to be identical to the first, but everything worked on the first try with absolutely no problems. Admittedly, it's difficult to judge whether a company quality-control problem exists by examining only two units, but if you consider buying one, you might want to test it out first.

Otherwise, the IOC Reader proved to

PCS 230

Type

Text-only scanner

Company

CompuScan Inc.
81 Two Bridges Rd.
Building 2
Fairfield, NJ 07006
(201) 575-0500

Size

Height: 8 inches; width: 17 inches;
depth: 19 inches; 25 pounds

Features

Accepts up to 50 sheets for automatic feed; 200-dpi resolution

Necessary Hardware

IBM PC, XT, AT, or compatible with serial port, one floppy disk drive, and 256K bytes of RAM

Necessary Software

DOS 2.0 or later

Documentation

40-page user's manual

Price

\$5695

PC Scan

Type

Text-only scanner

Company

Dest Corp.
1201 Cadillac C.
Milpitas, CA 95035-9974
(408) 946-7100

Size

Height: 4 inches; width: 16 inches;
depth: 11½ inches; 13 pounds

Features

Extensive diagnostics; made to fit under monitor; 300-dpi resolution

Necessary Hardware

IBM PC, XT, AT, or compatible with 256K bytes of RAM and two floppy disk drives or one floppy disk drive and one hard disk drive

Necessary Software

DOS 2.0 or later

Documentation

180-page user's manual

Price

\$2885

be a very fast and accurate unit with a resolution of 100 to 400 dpi. I found, however, that test speeds for this unit can vary greatly, depending on whether you load the optional character fonts that come on the disk. Six of the character fonts are contained in easily replaceable ROM chips. Three more fonts are on a disk, and you can load them, if you choose, each time the program is initiated. At press time, Intelligent Optics had just announced an enhancement to the program disk that, according to the company, allows the IOC Reader to recognize multiple fonts on a page.

You can also use the IOC Reader with an EGA board as a graphics scanner. It even allows you to work with graphics using just a floppy disk-based computer because the IOC Reader software, which requires 512K bytes of RAM for graphics and text (256K for text only), compresses a full page of graphics data (about 470K bytes) into only 50K bytes.

EIT Personal Scanner 2000

The EIT Personal Scanner 2000 (\$2495) from Electronic Information Technology is a "flatbed" unit. The glass scanner plate

is highly curved, however, and cannot easily accept hardbound material.

Although the Personal Scanner 2000 is about the size of a monitor, it has very little on the inside since there is no need for paper-transport mechanisms. The paper remains stationary, and only the small scanner lens moves. This approach avoids the possibility of a paper jam entirely.

The unit also requires a 10-megabyte hard disk and is connected by a special cable to an IBM PC-compatible card. The documentation mentions some problems with external hard disk drives and recommends that the unit be used only with an IBM PC XT, AT, or compatible with an internal hard disk. I used it with my Tandy 1200, which has an internal 10-megabyte hard disk. EIT recommends that you use DOS 2.0 or later, but not DOS 3.0 or later with a PC XT. Like the other machines, the Personal Scanner 2000 comes with software. It requires 512K bytes of RAM.

Of the units reviewed, the Personal Scanner 2000 is the most sensitive to skewed lines. It sometimes rejected pages as unreadable that were scanned successfully by all the other units. Also, it is the only unit that required calibration. How-

IX-12

Type

Text and image scanner

Company

Canon U.S.A. Inc.
One Canon Plaza
Lake Success, NY 11042
(516) 488-6700

Size

Height: 3¾ inches; width: 13½ inches;
depth: 11½ inches; 13 pounds

Features

Five-page auto-feed; font-trainable;
300-dpi resolution

Necessary Hardware

IBM PC, XT, AT, or compatible with 384K
bytes of RAM (640K bytes
recommended), and IBM-compatible
monochrome or color graphics display

Necessary Software

DOS 3.0 or later

Documentation

14-page booklet; 18-page ReadRight
manual for OCR software

Price

IX-12: \$1190
OCR ReadRight software: \$595

IOC Reader

Type

Text and image scanner

Company

Intelligent Optics Corp.
4 Heritage Park Rd.
P.O. Box 712
Clinton, CT 06413
(203) 669-3650

Size

Height: 6 inches; width: 14 inches;
depth: 14 inches; 18 pounds

Features

Auto-feed for up to 30 pages; additional
fonts can easily be added to disk when
made available, with up to ten in active
memory; works with a wide variety
of word processors and computers;
100- to 400-dpi resolution

Necessary Hardware

RS-232C asynchronous or bisynchronous
interface; computer or word processor
capable of supporting a program loaded
from disk

Documentation

User's manual; service manual;
IOC dealer manual

Price

\$4295

Personal Scanner 2000

Type

Text and image scanner

Company

Electronic Information Technology Inc.
373 Route 46 W
Fairfield, NJ 07006
(201) 227-1447

Size

Height: 11 inches; width: 13 inches;
depth: 13½ inches; 11 pounds

Features

Font-trainable with included software;
240-dpi horizontal and 300-dpi vertical
resolution

Necessary Hardware

IBM PC XT, AT, or compatible with internal
10-megabyte hard disk drive, 512K bytes
of RAM, and IBM Color Graphics Adapter
(or equivalent) or Tecmar, MDS Quantel,
or Hercules graphics or EGA boards

Necessary Software

MS-DOS 2.0 or later; 3.0 or later
should not be used with a PC XT

Documentation

Three manuals; 280 pages total

Price

\$2495

ever, the process is automatic except for the insertion of the test sheet, and you need to do it only once, which takes less than a minute. The scanner has a resolution of 240 horizontal by 300 vertical dpi.

Benchmark Considerations

To test the scanners, I used six pages of sample text. I initiated each scan program, entered all the required information, and then began timing when I entered the final command. I stopped timing when the computer was done with the task. Thus, my results reflect the actual time required to scan one complete document and return to the scan program. As a result, my test times are far longer than the advertised times. The scan times often mentioned in advertisements seem to be only the time required to run the document through the scanner without processing the information. In actual use, the scanner will start and stop repeatedly, sometimes at every line, while the text is processed.

Also, some of the scanners permit adjustment of the scanned area of the page. Making the measurements and required settings takes time but speeds up the scan times. Since not all the scanners allow or

need these adjustments, all timings were done using the default settings.

In addition, reading the same page of text two different times can sometimes result in different test times and, in some cases, the file generated by the scan varied in size. Second, all but the CompuScan PCS 230 are dependent on the host computer for character recognition; therefore, a faster computer will significantly decrease the recognition times I had with my Tandy 1200, which uses a 4.77-MHz 8088.

Test Documents

I conducted six different tests; each consisted of a unique page of text that was read by each of the scanners. Some people may be critical of using such a wide range of text and images, but I was trying to simulate the mix that you might encounter in a typical office. The times and numbers of errors that occurred while reading each of the pages are listed in table 1.

The first page was a high-quality offset reproduction of Courier 10 text and numbers in both single and double spacing with some deep indentations. The top

two inches of the page contained a large letterhead with an outlined border, and the bottom line was typeset in an unrecognizable font. This test page was the only one with a font that was supported by all the scanners. Here, the CompuScan PCS 230 was the clear winner.

The second page contained wide margins and had six different fonts that had been reproduced by a good copier. The fonts included Courier 10, Madeleine-Proportional Space, Prestige Pica, Letter Gothic, Courier 12, and Prestige Elite. Once again, the PCS 230 was the clear winner.

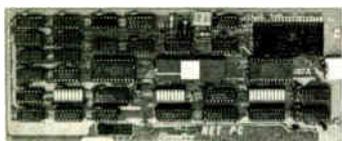
The third page was a contract with some deep indentations, some underlining, and both single and double spacing. The font used was Prestige Elite. The IOC Reader won this test in speed, but it had four times as many errors as the PCS 230, which came in second. The only scanner to read the page with no errors was the Dest PC Scan.

The fourth page was a double-spaced manuscript with wide margins printed in Courier 10 on my Tandy DWP-510 daisy-wheel printer. Any editor would be like-

continued

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REVIEW: TEXT SCANNERS

Table 1: OCR benchmarks. Document sizes are in characters; times are in minutes:seconds. Errors, shown in parentheses, indicate the number of mistakes of any nature made during the test. All timings were performed on a Tandy 1200, an IBM PC XT-compatible equipped with a 10-megabyte internal hard disk, one floppy disk drive, 640K bytes of RAM, a serial port, and a color graphics board with an RGB monitor.

Document	Size	CompuScan PCS 230	PC Scan	IX-12	IOC Reader	Personal Scanner 2000
1	1559	0:39 (0)	3:05 (0)	1:37 (3)	1:33 (0)	2:28/8:44 ^a (0)
2	1648	0:55 (2)	1:44 (10)	1:45 (10)	0:59 (>1000)	— ^b
3	2234	0:58 (2)	1:35 (0)	2:04 (4)	0:40 (8)	4:55 (7)
4	1181	0:40 (1)	1:23 (22)	1:40 (32)	0:42 (30)	10:37 (67)
5	2430	1:16 (6)	1:46 (0)	2:30 (114) ^c	0:40 (20) ^d	5:25 (27) ^e
6	2007	2:28 (7)	— ^f	1:56 (24)	1:30 (about 1000) ^g	— ^b

^a This scanner hung up on the last line, which was typeset and couldn't be read anyway; the other scanners skipped it. After 2:28, the entire page had been read with no errors, but the software didn't give up on the last line until 8:44. The scan can be stopped manually.

^b The machine rejected the page because of a skew error. However, the lines of text on the page appeared perfectly perpendicular to the vertical edges of the paper when checked with a T-square.

^c Most of the errors were case and special-character errors.

^d All errors were either opening or closing parentheses.

^e All errors were either closing parentheses or extra spaces.

^f The machine did not scan because of the graphic logo at the start of the page. When set to retry, it hung up, and when set to eject if unreadable, the entire page was ejected, even if only the first few inches were unreadable.

^g The machine could not read the underlined portions, which were about one-half of the text.

ly to encounter many similar pages every day, and the ability to read this sort of document would be helpful for many publishers. In this test, the PCS 230 read the page just two seconds faster than the IOC Reader. However, the IOC Reader had 30 errors, compared to just one for the CompuScan PCS 230.

The fifth page consisted of lower- and uppercase letters in five-letter groups, along with the common English symbols (. , ; : () ? ! @ # \$ % & — + =), several English sentences, the alphabet (again, upper- and lowercase) written in sequence, and the numbers 0 through 9 printed in groups of five as a string.

For this test I created five identical pages to provide new test sheets for each

scanner. I prepared them on the Tandy DWP-510 using a new Courier 10 print wheel and a carbon film ribbon to produce dark and consistent characters.

In this test, the IOC Reader was the fastest, but it produced 20 errors. The PC Scan was the only scanner to read the page with no errors. The Canon IX-12 had a whopping 114 errors on this page, but almost all of them were case and special-character errors.

The sixth page was a short letter that used extensive underlining and was centered with a small letterhead, including a graphic logo, at the top. The text was a high-quality offset of Prestige Pica. Again, I had a number of identical copies.

continued

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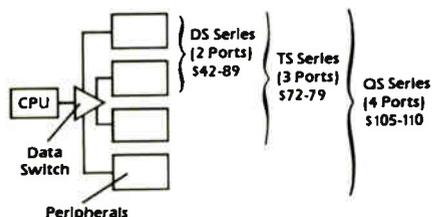
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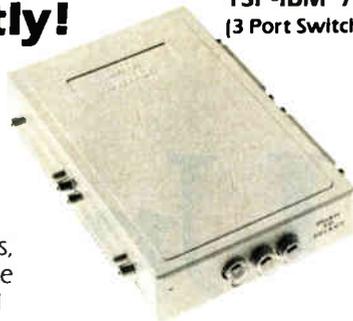
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The Personal Scanner 2000 and the PC Scan could not read this page because of the graphic logo. All the other scanners quickly skipped the signature and letterhead or assigned them garbage symbols. The IX-12 was fast but had 24 errors, while the PCS 230 was slower but had the fewest (7) errors.

Reading Between the Lines

Until recently, the most amazing thing about desktop OCR machines wasn't how well they could read text, but that they could read any text at all. Each of the scanners I tested, however, read the text and created clean ASCII files quickly and accurately, at least when presented with text that matched its requirements. I omitted, however, the number of typefaces supported by the machines for two reasons. First, claims vary greatly, and while some companies claim their machines support only a few typefaces, these machines actually recognized just as many or more than the machines that are claimed to support a lot of typefaces. Second, the number of typefaces recognized can be updated and added to by the company, often just by releasing a new version of the software.

Most of the recognition problems occurred with pages that mixed characters and graphics. This is a common problem with letterheads and lined paper. The unreadable or high-error pages used fonts that were not recommended by the companies. This, of course, is not necessarily a fault of the scanners; rather, it is an indication of their lack of versatility.

Capitalization errors were a big problem. Some of the scanners had great difficulty telling the difference between upper- and lowercase V's and W's. However, if you are building database files where capitalization is not critical, then these are not fatal errors.

The most expensive units had the best performance in reading a wide variety of fonts with few errors and ignoring nontext material, such as fancy letterheads. If you need to read the widest variety of text, possibly using unknown fonts, then the CompuScan PCS 230 is the winner, with the IOC Reader a close runner-up. Only these two units permit you to stack a large number of pages in the tray, reading them either as one large file or assigning sequential names to each set of documents separated by a blank sheet. The less expensive scanners did very well when working within their more narrow capabilities. The question you face is whether the text you need to scan falls within the scope of the less expensive units. [Editor's note: *At press time, CompuScan had just announced the PCS 235, a lower-priced version of the PCS 230, for \$3150.*] ■



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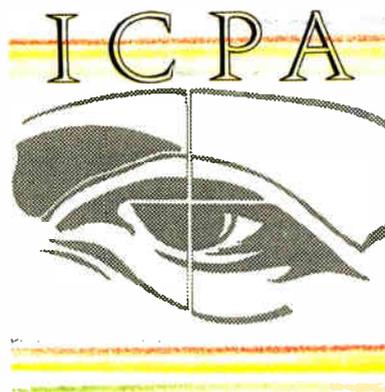
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The GCLISP 286 Developer

Ernest R. Tello

A Golden Common LISP interpreter and compiler for the IBM PC AT

Gold Hill Computers' GCLISP 286 Developer (\$1195) is a LISP development system for the IBM PC AT and 100 percent compatibles that is implemented as a subset of the Common LISP specification and incorporates various ZetaLISP concepts. It contains version 2.0 of the interpreter and version 1.0 of the compiler, requires PC-DOS or MS-DOS version 3.0 or higher, and can use up to 15 megabytes of extended memory. The system supports packages, transcendental functions, lexically scoped variables, and bignum data types. Golden Common LISP currently has no object-oriented extension.

Like GCLISP version 1 for the IBM PC and compatibles [Editor's note: See the review by Bruce D'Ambrosio in the December 1985 BYTE], the GCLISP 286 Developer comes with the GMACS screen editor, a debugging utility, an interactive tutorial, on-line help, a GCLISP reference manual, and two books: *The Common LISP Reference Manual* by Guy L. Steele Jr. (Digital Press, 1984) and *LISP* (second edition) by Patrick H. Winston and Berthold K. Horn (Addison-Wesley, 1984). The interpreter has been enhanced to take advantage of the large address space of the 80286 and is called the Large Model (LM) interpreter version 2.0 to distinguish it from version 1. The interpreter needs a minimum of 1.5 megabytes of memory. You also have the option of installing the LM compiler that comes with the system. The compiler requires at least 3 megabytes of memory and 700K bytes of space on your hard disk. It can be invoked from either the interpreter or the editor.

Lexical vs. Dynamic Scoping

The addition of lexically scoped variables brings the GCLISP 286 Developer closer to the Common LISP standard. GCLISP version 1 has dynamically scoped variable bindings. In Common LISP, a distinction is made between *scoping* and *exten-*

tent. *Scoping* refers to the range of a variable over a body of code, whereas *extent* refers to the length of time for which the name of the variable is bound. With lexical scoping, references to a variable can occur only in those program portions where the variable is defined. With indefinite scoping, references to a variable can occur anywhere in the program. To say that a variable has dynamic extent means the name of the variable remains bound only as long as the function that calls it continues to be invoked. If a variable binding has indefinite extent, this means that it continues to exist as long as there is a possibility of a reference to it occurring. *Dynamic scoping* is simply a convenient term for indefinite scoping and dynamic extent.

In GCLISP version 2, variables are normally bound with lexical scoping and indefinite extent. You can give variables dynamic scoping by declaring them as special. The *catcher* specified by the *catch* or *unwind-protect* special forms is dynamically scoped. The exit point specified by the *block* construct has lexical scoping and dynamic extent. Any *GO* targets named by the tags in a *tagbody* and referred to by *GO* have lexical scoping and dynamic extent. All named constants such as *nil* and *pi* have dynamic scoping and indefinite extent.

Stack Groups

Stack groups are not part of the Common LISP standard, but instead are a feature that was first introduced in ZetaLISP for LISP machines. With the large memory space available with the GCLISP 286 Developer, you can use stack groups to create alternate transient processes, or coroutines, each with its own environment. You can halt or resume these pro-

cesses at any point, and their halted state is kept in suspension until the stack group is resumed. At all times there is a current stack group containing two stacks; one keeps track of the current state of the computation, and the other saves all the current variable bindings. Also, each stack group has a state that is always either active, resumable, exhausted, or broken. It is exhausted when the function called by the stack group has been completely evaluated. A stack group is in a broken state if it is in an error condition when it is halted.

When any stack group resumes, it can transmit a LISP object from the old stack group to the new stack group to evaluate it. What stack groups do, then, is allow the creation of distinct processes, each with its own separate stack and binding environment, that can call upon one another to return values needed for their computations. Although using stack groups adds some overhead, it minimizes the difficulty of creating sophisticated operations.

Running in Protected Mode

The GCLISP 286 Developer runs in the protected mode of the 80286, but it uses the DOS and BIOS file system and external device driver interface from the nonprotected mode. This takes some doing, since the 80286 processor does not provide a means of switching to the nonprotected mode from the protected mode without reinitializing the chip. Gold Hill gets around this by treating the PC AT as a two-processor virtual machine. The first 1 megabyte of the PC AT's memory is reserved for unprotected-mode activities running under

continued

Ernest R. Tello (1518 West Cliff Dr., Santa Cruz, CA 95060) is a consultant interested in artificial intelligence applications for business, engineering design, and space technology.

GCLISP 286 Developer

(with LM interpreter version 2.0 and LM compiler version 1.0)

Type

LISP development environment

Company

Gold Hill Computers
163 Harvard St.
Cambridge, MA 02139
(617) 492-2071

Format

Seven 5¼-inch 360K-byte floppy disks; not copy-protected

Computer

IBM PC AT or 100 percent compatible with extended-memory card; interpreter requires 1.5 megabytes of memory; compiler requires 3 megabytes and a hard disk

Necessary Software

PC-DOS or MS-DOS version 3.0 or 3.1

Language

LISP

Documentation

447 pages in a three-ring binder including user's guide, GCLISP reference manual, LM interpreter guide, and LM compiler guide; *The Common LISP Reference Manual*; *LISP*

Price

\$1195

PC-DOS. However, this memory is suspended as if it were another processor when the 80286 enters the protected mode and runs GCLISP in the 15 megabytes located above the 1-megabyte DOS workspace.

According to Gold Hill, these two virtual processors run synchronously and communicate with one another by a shared-memory message-passing scheme. Control is transferred between the two modes of the 80286 through PC AT BIOS processor mode-switching services.

Considering the elaborate mechanism needed to emulate DOS and BIOS from GCLISP running in the protected mode, it is impressive that so much of this interface is available. GCLISP functions are provided for DOS file operations such as working with path names and opening, closing, renaming, and deleting files.

Functions are also provided for invoking the DOS command processor, executing external DOS programs, and invoking some DOS and BIOS interrupts directly. Specifically, only those interrupts that pass parameters in registers are fully implemented. This is because of the difficulty of emulating real-mode interrupts from protected mode. The documentation recommends that if users need an interrupt with in-memory parameter passing, they should implement their own emulation using services provided in the LM kernel.

Running the Compiler

The LM compiler cannot run from the floppy drive; you must install it on the hard disk. A batch file automates the loading of customization files that modify the system to run the compiler. A couple of initialization files ensure that the compiler is automatically loaded when it is first invoked from within the interpreter or editor. Some files containing compiler deconstruct enhancements are copied. The CPATCH.LSP file actually modifies the interpreter itself, and it even changes the version number from 2.0 to 2.1.

You can run the GCLISP compiler in three ways. You can issue the compile or compile-file functions from the interpreter, or you can use the appropriate key commands to compile a program from within the GMACS editor. The compile-file function takes the name of a disk file of LISP source code and compiles it. The compile function, on the other hand, takes a LISP function name as an argument.

Both compile and compile-file can produce fast-load files or assembly language listings in a DOS-compatible format. The documentation says you can use the assembly language files for debugging, the implication being that if you were to assemble them with the MASM macro assembler, you would have the assembly language equivalent of the LISP function only. Currently the package has no provision for adding user-defined built-in functions to GCLISP; the most you can do is add user-defined functions as compiled fast-load files.

A number of variables determine the way the compiler environment behaves. For example, setting the compiler: *optimize-space* variable to true optimizes the size of the resulting code rather than its speed. The value of the gcomp: *286-p* variable determines what machines the compiled code will run on. If this variable is set to nil, then the code will run on both 8088/8086- and 80186/80286-type processors. If the variable is set to true, then only the 80186/80286 processors will run the

code. Obviously, the additional instructions on these chips will be used in this mode. The compiled code, however, will run only on version 2.0 or higher of the interpreter. The 8088/8086-compatible code is intended for the subsequent release of version 2.0 and 2.1 for the IBM PC and compatibles.

The LM compiler supports the complete language as used with the LM interpreter, with the following exceptions: the #, load-time evaluation macro; the progV form, which allows the binding of dynamic variables whose names can be determined at run time; throw and catch with multiple-value functions; and go and return-from between functions in the same lexical environment. In addition, closures in argument lists cannot use &aux, &optional, or supplied-p variables in optional arguments. Some of these limitations are due to the nature of the compiled environment. Functions that are evaluated at run time cannot be implemented in a compiler. According to Gold Hill, the other functions will be implemented in a later version of the compiler.

Memory space in GCLISP, as in any LISP system, is divided between cons space and atom space. The cons space is where the pointers for linked lists are stored. The atom space is the memory space used for data values that can be organized into lists. Interpreted LISP functions tend to use mainly cons space, whereas compiled functions use more atom space.

In using the GCLISP compiler, the order of compilation is important. With the interpreter, as with any LISP, forward references are commonplace. As a rule, program development in the interpretive environment proceeds in a flexible top-down fashion where functions can be entered into the interpreter that call other functions and as-yet-unwritten macros. With the compiler, though, macros have to be defined prior to compiling the functions that define them. In the same vein, all declarations must be made with the expressions defvar, defconstant, defparameter, or defstruct before you can use declared names in a compiled function. For large programs, it is possible to make all such declarations in a single file that you can compile prior to any of the other source files. Another difficulty of using compiled GCLISP rather than interpreted code is that since it consists of machine code, you lose the ability to manipulate the code as data.

Hardware Support

The GCLISP 286 Developer provides support for many of the PC AT's hardware enhancements and extensions such

SOFTWARE REVIEWS

as the 80287 math coprocessor, the Enhanced Graphics Adapter, the Professional Graphics Adapter, most of the popular mouse drivers, and, ideally, as much as 15 megabytes of extended memory. I tested the system with the AST Advantage and Everex RAM 3000 extended-memory AT boards. According to Gold Hill, other extended-memory boards supported are Tall Tree Systems' JRAM-AT, M.A. Systems' AT Optimizer, and Magnum Memory. The Lotus/Intel/Microsoft "above-board" standard is not supported.

The Gabriel Benchmarks

The set of benchmarks that follow are based on those published by Richard P. Gabriel in his *Performance and Evaluation of LISP Systems* (MIT Press, 1985). To my knowledge, they are the most complete and elaborate set of benchmarks for the LISP language ever compiled. The results of the benchmark tests are shown in table 1. I ran the benchmarks for interpreted and compiled GCLISP on an 8-MHz IBM PC AT with 512K bytes of base memory and 3 megabytes of extended memory. For comparison, I used the values for Common LISP

on the VAX-11/750, the Xerox Dandelion, and the Symbolics 3600, as published in Gabriel's book.

A number of these benchmarks show different ways of doing the same thing. For example, tak was designed to test the speed of making numerous function calls. A variation is stak, which uses special binding to pass arguments instead of using normal argument passing. The takr benchmark is a version of tak that neutralizes the effect of cache memory by jumping around in memory. The ctak benchmark returns values with the catch and throw mechanism rather than with function returns. The takl benchmark is like tak but does not have any explicit arithmetic.

Other benchmarks test a variety of operations that programmers might do in LISP. These range from numeric and algebraic calculations to knowledge representation and search problems used in artificial intelligence. The numeric and algebraic tests are the symbolic derivative program deriv and its data-driven variant dderiv; an iterative test dividing nils by 2, called div2-iter; and its recursive counterpart, div2-recur. The polynomial

continued

Table 1: Gabriel benchmarks run on an 8-MHz IBM PC AT with 3.5 megabytes of memory using the Everex RAM 3000 extended-memory card. Comparisons, which are as published in Richard P. Gabriel's Performance and Evaluation of LISP Systems, are shown for Common LISP running on a VAX-11/750 and two LISP machines, the Xerox Dandelion and the Symbolics 3600. Data for the polynomial benchmarks was not available for the Dandelion because its implementation of Common LISP does not support the bignum data type. All times are in seconds.

	Interpreted GCLISP	Compiled GCLISP	VAX 750	Xerox Dandelion	Symbolics 3600
tak	106.70	4.90	2.69	1.67	0.60
stak	94.87	16.87	6.21	4.66	2.58
takr	110.94	5.05	4.39	1.75	0.60
ctak	130.63	11.26	13.86	63.20	7.65
takl	789.66	46.41	12.35	14.00	6.44
deriv	161.04	19.00	24.50	23.90	5.12
dderiv	178.24	20.81	32.90	33.30	5.24
div2-iter	210.22	13.72	14.32	23.80	1.85
div2-recur	184.85	16.27	9.07	24.80	2.89
frpoly5rxyz1	4.92	0.38	0.37	N/A	0.05
frpoly15rxyz1	502.80	117.20	21.51	N/A	3.45
frpoly5r3	5.20	0.71	0.48	N/A	0.05
frpoly15r3	432.40	64.20	31.05	N/A	3.84
destruc	266.19	14.50	11.30	17.58	3.03
trav-init	1819.24	68.08	35.44	48.00	8.62
boyer	1212.46	77.23	69.38	74.60	11.99
browse	1490.34	285.02	195.11	174.00	30.80
fread	6.45	6.40	11.21	8.00	4.60
fprint	6.76	6.68	6.08	13.70	2.60
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arithmetic-manipulation programs frpoly5rxyz1 and frpoly15rxyz1 take the fifth and fifteenth power, respectively, of the polynomials $r = x+y+z+1$, $r = 100,000(x+y+z+1)$, and $r = 1.0(x+y+z+1)$. The frpoly5r3 and frpoly15r3 benchmarks take the fifth and fifteenth power of the cube of the three equations given above.

Various destructive list-processing functions are tested with destruc, and trav-init initializes and traverses a tree. The boyer benchmark tests the performance of functions used in theorem proving, and browse creates a hierarchical artificial intelligence database and browses it. Some I/O tests read from a file with fread, write to a file with fprint, and read and print to the console with tprint. [Editor's note: *The GCLISP versions of these benchmarks are available on disk, in print, and on BIX. See the insert card following page 208 for details. Listings are also available on BYTEnet. See page 4.*]

One thing that stands out clearly in the benchmarks is the speed of GCLISP compiled code in comparison to interpreted code. The average speedup for the 20 benchmarks run with both compiler and interpreter is 11.1 seconds. The compiler does not significantly speed up I/O operations, but programs rich in deep data representations, like those used in artificial intelligence, often improve dramatically with the compiler. In some cases, the tests for GCLISP compare surprisingly well with those recorded for the more expensive machines. In others, they lag behind considerably.

New Releases

At the time of this writing, Gold Hill was about to release version 2.2 of the GCLISP 286 Developer. According to Gold Hill, this version will have a foreign language interface to C, a 25 percent faster fload, and a compiled GMACS and LISPLIB. The GMACS editor will have many enhancements such as incremental search, standard EMACS and user-defined key-chord bindings, and multibuffer operations using tag tables. The GMACS and LISPLIB sources will be available on request, free of charge. Upgrades from the GCLISP 286 Developer 2.0 are \$90, and upgrades from GCLISP version 1 are \$895.

Also, the GCLISP 386 Developer for the IBM PC XT and PC AT is now available. It comes bundled with a plug-in board, called the Hummingboard. The Hummingboard features the Intel 80386 operating at a clock speed of 16 MHz. It plugs into any IBM PC or compatible and is claimed to run GCLISP five times faster than the GCLISP 286 Developer. It

comes with 6 megabytes of high-speed dynamic RAM and is expandable to 24 megabytes. The GCLISP 386 Developer plus the Hummingboard is priced at \$7000.

An Enormous Improvement

The GCLISP 286 Developer is an enormous improvement over version 1 of GCLISP. Not only does it satisfy one of the main distinguishing features of Common LISP—lexical scoping—but it is a system that allows you to build large applications. The earlier product had a number of impressive features such as the editor and on-line documentation, but because it used up so much memory, there was little room for applications. This is no longer a problem with a memory-space limit of 16 megabytes. The compiler, which improves the speed of code

approximately 10 to 15 times over that of the interpreter, is also a necessary part of a serious LISP development environment.

I recommend this version of LISP for people interested in doing serious artificial intelligence projects where mathematical problem solving is not one of the foremost issues. (GCLISP 2.0 still does not support multidimensional arrays, or even a random function.) GCLISP is currently the MS-DOS LISP system that allows you to develop the largest LISP programs. Although many programs developed in full versions of Common LISP on larger machines will not yet run in GCLISP, the opposite is not true. Programs written with this system that do not use stack groups or machine-dependent features should run in complete Common LISP systems. ■

Turbo Pascal Toolboxes

Namir Clement Shammam

Blaise Computing's Power Tools Plus version 2.00 (\$99.95) and Turbopower Software's Turbo Extender version 1.04 (\$85) are Turbo Pascal software add-ons that extend programming productivity for the IBM PC, XT, AT, and compatibles running PC-DOS 2.0 or higher by providing libraries of routines. I tested these packages on an IBM PC XT with 512K bytes of memory, an 8087 coprocessor, a 20-megabyte hard disk, and two 360K-byte floppy disk drives running PC-DOS 3.1. The number of system buffers you use in your configuration file influences both software performance and I/O operations; I used 16. [Editor's note: *Both these packages have had new versions since this review was written, but the changes are minor and involve no new functionality. The current versions are Power Tools Plus version 2.02 and Turbo Extender version 1.07.*]

Power Tools Plus

While Power Tools Plus version 2.00 runs under either Turbo Pascal 2.0 or 3.0, the latter is recommended. The minimum memory needed is the same as for Turbo Pascal—64K bytes. A hard disk is also recommended but not required. This library provides string functions and routines for screen support,

window management, menu management, keyboard control, DOS utilities, file handling, directory maintenance, memory management, program control, and interrupt service support.

The string functions FillStr, LeftStr, RightStr, MidStr, and SubStr, among others, are notable for their execution speed and provide approximate Pascal equivalents of BASIC's STRING\$, TIME\$, DATE\$, LEFT\$, RIGHT\$, and MID\$ string functions, as well as string justification, numeric conversion, and upper- and lowercase conversion. Timings carried out for varied substring lengths show the effect of manipulating different numbers of characters. The RightStr function executes more slowly as the number of characters decreases, while the other functions increase in speed when handling fewer characters, as you would expect.

The screen-support routines in Power Tools Plus extend the screen, cursor-control, graphics, and color capabilities to cover the monochrome, Color Graphics Adapter, PCjr, and Enhanced Graphics Adapter display modes. Some of the routines duplicate Turbo Pascal screen intrinsics to accommodate the different display adapters. You can also access

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multiple text screens depending on the type of video monitor you use. A library procedure obtains the monitor type and the exact number of displayable text pages from memory. You can write to one screen while you display another because the routines support both a current screen page and an active, or displayed, page. You can also access the screen's direct memory to send or fetch data to or from the screen quickly.

The window management routines extend Turbo Pascal's support for text-mode windows to include the EGA video

board; to support the creation, removal, and management of many bordered windows; and to let you manipulate cursor position, text I/O, and display attributes.

The menu management routines provide a special type of window for menu selection. Three stages are involved in displaying a desired menu: constructing the menu descriptor, specifying the physical display and its appearance, and calling a routine that shows the menu and returns the selection made.

The keyboard-control routines in Power Tools Plus perform keyboard scan-

ning and special errorproof input operations. Keyboard scanning returns an extended code (generated by pressing either the function or cursor-control keys) and then queries or assigns the status of such keys as Caps Lock, Num Lock, Scroll Lock, or the Alt-Shift key combination. The routines also support keyboard buffer flushing and a two-way character transfer between the buffer and the application program. The errorproof functions enable a program to prompt for the correct entry of integers and reals; if the input does not conform to the definition of an integer or a real, an error message is displayed. These functions prevent execution halts if you enter invalid numeric data, but they can be frustrating if you have just entered a large numeric matrix.

The DOS utility routines allow Turbo Pascal applications to inquire about DOS and control its environment. You can set the system time and date, access the DOS version number, verify whether DOS is in a critical uninteruptible state or not, and query and assign DOS-environment parameters and their current status. You are actually only affecting the application's copy of the DOS environment and any "child" programs (those executed from within others) that the application initiates; you are not affecting the original DOS environment that is associated with COMMAND.COM. You can install the PRINT spooler running under DOS 3.0 or higher, and you can insert or remove text files from the print queue.

The file-handling routines in Power Tools Plus provide DOS-based file manipulation for nontext file structures including file creation, opening, closing, and I/O. Random access is available and relocates the file pointer by using absolute and relative displacements. You can set or read the date and time stamp, the file attributes, and the disk-transfer area. These routines differ from those in Turbo Pascal by using a file-handler number to reference a file. In addition, they perform I/O by using memory pointers and counters to keep tabs on the source and destination of the data. The file-handling routines also support networks and the types of file-access rights supported by DOS, and they provide for the locking and unlocking of either a partial file or a whole one.

The directory-maintenance routines manipulate and manage directories. Some routines duplicate DOS commands that create, delete, and change directories; others perform more esoteric tasks such as changing the directory name, returning or setting the volume name, and scanning through the files of a directory. Together, these routines provide a much-

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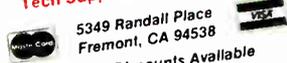
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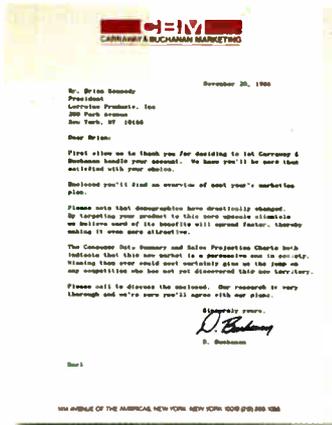
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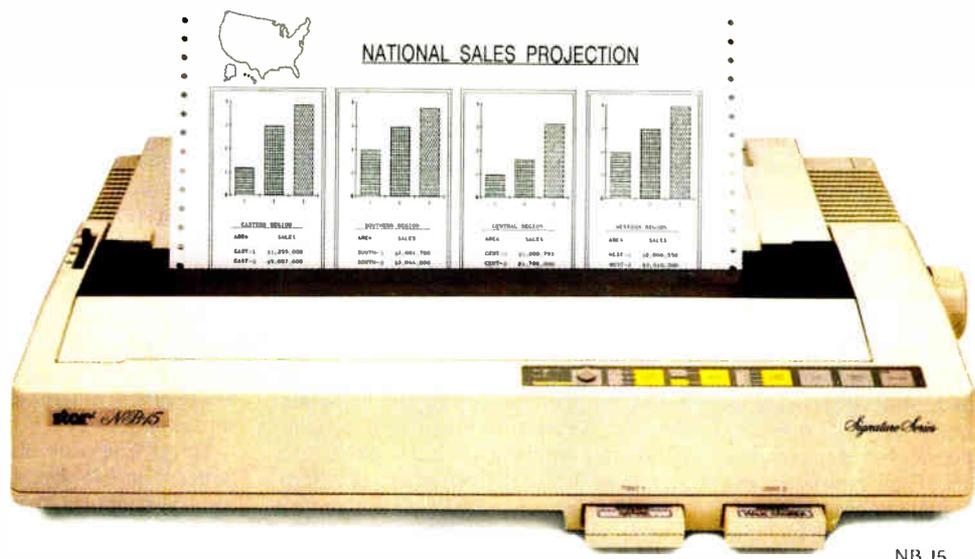
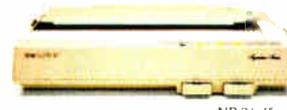
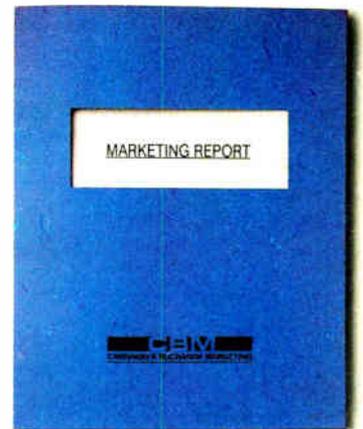
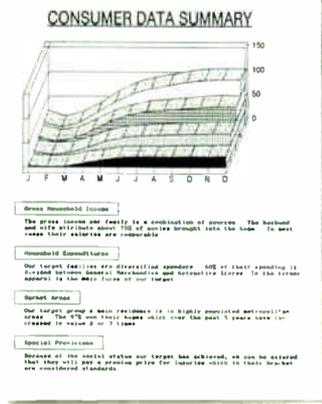
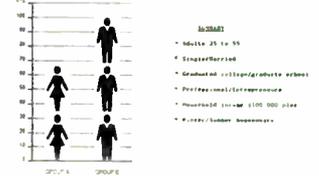
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Power Tools Plus version 2.00**Type**

Turbo Pascal routines library providing string functions and routines for screen support, window management, menu management, keyboard control, DOS utilities, file handling, directory maintenance, memory management, program control, and interrupt service support

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Blaise Computing Inc.
2560 Ninth St.
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Berkeley, CA 94710
(415) 540-5441

Format

Three 5¼-inch disks

Computer

IBM PC, XT, AT, or PCjr with PC-DOS 2.0 or higher and at least 64K bytes of RAM; hard disk recommended; some routines use extended memory, if available

Necessary Software

Turbo Pascal 2.0 or 3.0; 3.0 recommended

Language

Turbo Pascal; source code modules included

Documentation

310-page user's manual

Price

\$99.95

Turbo Extender version 1.04**Type**

Turbo Pascal routines library that lets you break Turbo Pascal 3.0's 64K-byte limit and use up to 640K bytes for programs; also lets you manipulate large arrays; contains utilities to create a source module from your source code, find altered modules and recompile them, verify cross-module calls and maintain support-structure integrity, and create a single .EXE file from source code

Company

Turbopower Software
3109 Scotts Valley Dr.
Suite 122
Scotts Valley, CA 95066
(408) 438-8608

Format

Two 5¼-inch disks

Computer

IBM PC, XT, or AT with PC-DOS 2.0 or higher; no minimum or recommended amount of RAM mentioned

Necessary Software

Turbo Pascal 3.0

Language

Turbo Pascal; source code included in compressed archive form, as is a utility that translates it back into source code

Documentation

146-page manual

Price

\$85

is a source code printer with page-size and margin-control options. Another utility, INCLUDE, generates a list of include directives and inserts it into your source code. It checks your program for all the correct hierarchical interrelated routine calls and maps these dependencies. PROCPAK, another utility, removes comments, tabs, blank lines, and trailing lines, thus compressing your source code so it occupies less disk space. Blaise Computing also includes CLOCK, a memory-resident clock that you can install in color with an alarm message and interval.

The 310-page user's manual, which comes in a three-ring binder, contains a number of appendixes including a quick-reference guide for the routines, important data types and variables, routine dependencies, and even troubleshooting questions and answers. The manual also provides additional insight on the workings of MS-DOS. I would like to see more program examples included, however.

Turbo Extender

Version 1.04 of Turbo Extender lets you break the 64K-byte limit of Turbo Pascal version 3.0 and use up to 640K bytes for programs. Since it is targeted toward large systems, no minimum or recommended amount of RAM is mentioned; however, I ran it with 512K. Instead of using chained and overlaid programs, Turbo Extender uses a faster technique that creates separately compiled modular programs. Thus, when you alter programs, you need only recompile the modules in which you made changes.

Turbo Extender contains the BIGTURBO library of included files. You use these files to create Pascal modules that support calling routines across module boundaries. The BIGTURBO library includes the following support utilities: SHELLGEN, which creates a Turbo Pascal source module by adding directives to your source code to define the module boundaries; BIGMAKE, which finds any altered modules and recompiles them (similar to the make utility in UNIX); EXPORTER, which verifies the cross-module calls and maintains the integrity of BIGTURBO support structures; and BUILDDEXE, which gives you the option of creating a single .EXE file from your source code.

Turbo Extender also supports arrays larger than 64K bytes. The BIGARRAY library supports five memory models using a virtual system with a paging operation. These memory models include RAM-based arrays, which use RAM space outside Turbo Pascal's workspace to store large arrays; RAM-based large

continued

desired feature: directory access for advanced Pascal programs.

The memory management routines provide access to DOS memory management services. The routines can determine the total amount of memory installed on your machine as well as the total amount of memory available. They can also determine the memory sizes of the Turbo Pascal environment, which include program size, static data size, minimum stack space, and maximum stack and heap size. The routines support allocation and alteration of DOS memory blocks and use pointers to perform the necessary accesses. They can detect extended memory installed on an IBM PC AT, and they provide a procedure for two-way data movement between main and extended memory.

The Power Tools Plus program-control routines work with the memory management routines to invoke child processes.

You can make these routines RAM-resident after they terminate execution, which yields memory-resident applications like SideKick, SuperKey, and ProKey. You can even execute a DOS command from within an application: A library procedure loads a copy of COMMAND.COM as a child process and then executes the specified DOS command.

The interrupt service routine support is a set of low-level routines that manipulate hardware and software. You can invoke RAM-resident routines and set up SuperKey-like keyboard macro applications. Blaise Computing includes MKEY, a simple keyboard macro utility, as a practical example of using interrupt service routine support along with program-control routines. You can also enable or disable interrupts, set or return interrupt vectors, and more.

The Power Tools Plus package also comes with a set of program utilities. One

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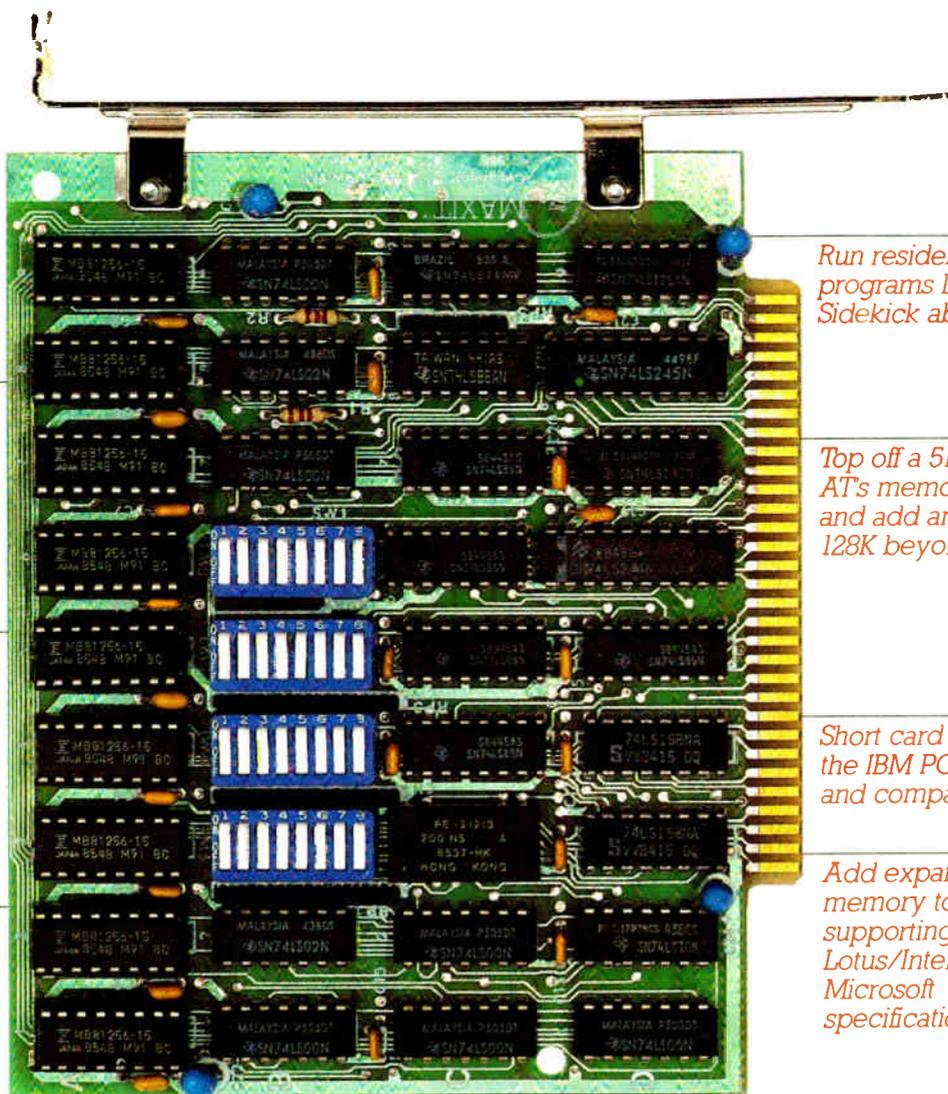
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arrays for sparse matrixes and arrays, which use RAM to store sparse arrays and pointers to skip over empty array members; disk-based arrays, which use disk space to store large arrays; disk-based virtual arrays, which are similar to disk-based arrays but let you specify array size during compile or run time; and expanded memory resident arrays, which use the Lotus/Intel/Microsoft Expanded Memory Specification to store large arrays. BIGARRAY contains routines to create, initialize, remove, and manipulate the contents of the arrays. These routines are similar for each memory model type, allowing you to switch from one model to another with a minimum of editing. The price of using the BIGARRAY library is that you can expect a decrease in the speed of array and matrix manipulations; however, being able to tackle such large arrays is a definite advantage. If you wish, you can run such time-consuming operations overnight.

I tested the speed of manipulating large matrixes in memory; that is, outside Turbo Pascal 3.0's data segment. For equal 50- by 50-pixel matrixes, the Turbo Pascal data-segment multiplication for a real array was 2.22 times faster than the Turbo Extender matrix multiplication in RAM; for a 75- by 75-pixel integer array, it was 4.61 times faster. However, Turbo Pascal data-segment multiplication cannot handle the larger arrays. I tested the Turbo Extender for up to a 120- by 120-pixel array for both real and integer multiplication in RAM. The real array took more than 36 minutes, while the integer array completed the operation in just over 22 minutes. The Turbo Pascal multiplication could not even attempt to process this size array.

Turbo Extender also includes other utilities for the analysis of overlay programs, the use of disk caching, and source code encryption. The code encryptor, PCRYPT.COM, has an interesting feature: It transforms your original source code into a form that is extremely difficult to read. This encrypted form compiles slightly faster with Turbo Pascal because it conforms to the manner in which Turbo Pascal stores its data tables. My tests on three approximately 30K-byte programs showed significant reductions in file size with PCRYPT.COM (the programs were reduced between 25 percent and 40 percent); however, compile-time reductions were minimal (about 1 second per program). The ASCII source code actually compiles faster than the encrypted code but there are fewer lines in the encrypted program, so it compiles slightly faster. The reduction in file size itself is worthwhile, however; even if the compile-time change is insignificant,

smaller, scrambled source-code files are reason enough to make PCRYPT.COM valuable.

Complementary Products

Power Tools Plus is a well-crafted product supported by excellent documentation. This new version is an improvement over the original Power Tools package, and its library is even better. I recommend Power Tools Plus to the Turbo Pascal programmer who is looking for a well-conceived, robust library of time-saving routines.

I recommend Turbo Extender for the Turbo Pascal programmer who wants to overcome the 64K-byte limitations to write bigger programs or manipulate larger arrays.

These packages are complementary to each other. I strongly recommend them to the Turbo Pascal programmer of average or advanced skill. ■

Namir Clement Shammas (4814 Mill Park Ct., Glen Allen, VA 23060) is a freelance writer and columnist for several microcomputing magazines.

Lattice® Works

LATTICE ANNOUNCES MICROSOFT WINDOWS SUPPORT IN VERSION 3.2

Version 3.2 of the Lattice MS-DOS C Compiler features full support for Microsoft Windows—including the "far," "near," and "pascal" keywords.

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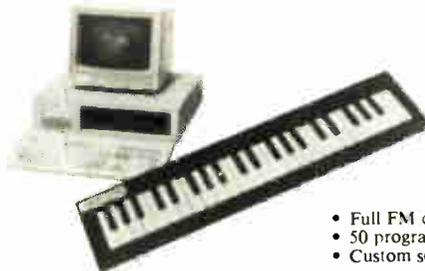
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R:base System V

Stephen Cobb

A relational database management system for single and multiple users

R:base System V is a "son" of R:base Series 5000, which is descended from the mainframe system called Relational Information Management that is used by NASA. Microrim introduced its R:base Series 4000 database program in 1983 as a direct challenge to Ashton-Tate's best-seller, dBASE II. Now R:base System V version 1.0 claims to go beyond dBASE III Plus.

Hardware Requirements

When you begin the relatively simple and clearly described process of putting R:base System V on your computer, you realize this program is a landmark in the area of hardware requirements. To run R:base System V you need at least 512K bytes of RAM (640K if you plan to share the program over a network), and a hard disk is required. One reason for this is that there are eleven 5¼-inch disks in the R:base System V package. When installed (a surprisingly speedy process that takes less than 20 minutes from start to finish) the full system eats up 3.6 megabytes. About half a megabyte consists of files for the tutorial, which can later be removed.

Once installed, it takes just 7 seconds for an IBM PC XT to load the system, and about 1 second for a Compaq 386. In practice, you may not need to install the full system. R:base System V consists of several separate but related programs, each of which has a specific role in the overall system. You can access the programs from the main menu that is presented when you type RBSYSTEM from the DOS prompt. This enables you to move easily from one element to the other, although you can enter them independently, directly from DOS. When you determine which elements of the system you need, you can erase the others if you are short on disk space.

Setup with Express

To begin managing information with R:base System V, you need to define the

structure of the information. Veteran programmers will be pleased to know that you can still go directly from DOS to the R> prompt of the programming language, which includes a built-in editor.

However, for ease and, in some cases, speed (as compared to the direct programming approach), R:base System V provides four Express programs that use simple point-and-pick-type menus to do the grunt work involved in defining not only the database structure but also the data-entry forms, the printed reports, and even the menus that pull together a whole application.

For example, to have R:base System V prompt you through the process of defining the structure of your database, you use Definition Express, which lays out the tables in which your information will be stored. The idea of a data table is an easy one to grasp. It corresponds to typical everyday databases like the phone book, where the name, address, and phone number are in separate columns, and each entry is in a separate row.

In R:base System V, a single database can consist of up to 80 different tables and 800 columns—about twice the capacity of R:base Series 5000. The 1530-characters-per-record limit of R:base Series 5000 is upped to 4096 in R:base System V. In addition, new data types have been added to the Text, Real, Integer, Date, Time, and Currency data types that are available in R:base Series 5000. The new Double data type offers 15-digit accuracy for numbers in the range of 10^{307} to 10^{-307} , while the Note data type provides a variable-length text field of some 4000 characters stored directly in the record and occupying only as much space as the entry uses. This is suitable for such things as extended comments.

In the data tables, the columns, or fields, of data are assigned a name, a type, a length, and attributes such as Key, which tells the program that the column is to be indexed. A personnel database might have "lastname" as a Key column to speed up the process of locating records by employees' last names. This is a different approach from some other databases, which have to be indexed retroactively. However, you can do this with R:base System V as well.

The entire definition process is a straightforward matter of deciding on names for the fields of data and picking a type from the menus. Context-sensitive help is available at all times. Once you have created the structure of a database in the Definition Express, you can proceed to the Application Express, which is probably the most impressive part of the entire system. This program literally writes new programs for you.

Let's say you want to manage personnel records. You can create a completely menu-driven application, including help screens for the clerk who will enter and update the data, by responding to the questions that the Application Express asks. You pick functions such as "edit records," "delete records," and "print records" from a list of options and assign them to your application menu, which can be vertical or horizontal.

A menu entry such as "print reports" can lead to another menu showing the various reports available. Picking the fields to report on and the selection criteria for the records is again a simple set of menu choices.

What developers will like about the Application Express is the ability to call up routines that have been written in R:base

continued

Stephen Cobb (TME Associates, 1615 Polk St., Suite One, San Francisco, CA 94109) is a personal computer consultant and teacher of microcomputer students.

R:base System V version 1.0**Type**

Single- and multiple-user relational database management system

Company

Microrim
3925 159th Ave. NE
Redmond, WA 98052
(206) 885-2000

Format

Eleven 5¼-inch disks

Computer

Single user: IBM PC, XT, AT, or compatible with 512K bytes of RAM and a hard disk drive; multiple user: same as above, but 640K bytes of RAM is required; supports a variety of networks including 3Com, Novell, and Ungermann-Bass

Language

FORTRAN

Documentation

Single-user guide; multiuser guide; learning guide, user's manual; building applications/command dictionary; conversion guide; command summary; keyboard template

Price

\$700

System V from within an Express-generated application, thus pulling together work from the programming level.

When you have completed building an application with the Express, R:base System V writes the actual code needed to do the tasks you have defined. You can then run your application or have it run automatically the next time you use the system. The Application Express uses some default arrangements of data entry and reporting screens, which I found to be generally acceptable. If they are not to your liking, you can use the Form Express to draw out your forms the way you like them. Using a similar process, Report Express takes care of the format and design of your printouts.

The entering and editing of the actual data is also a smooth process with the timesaving ability to carry a duplicate of the data from the previous record over to a new record for situations where there's a lot of similarity between entries. In the definition of your data-entry forms, you can select (without programming) such checks as doubled keystrokes, value ranges, and math calculations.

Perhaps the most remarkable data-entry feature available is "regions," which

permit you to update more than one table at a time from the same form. This gives you tremendous savings in data-entry time and makes your entry form almost unlimited in scope, since R:base System V lets you scroll the regions in a defined area of the data-entry screen. Such sophistication is rare in a microcomputer product.

The menus are easy to use in all parts of the program, and I enjoyed the flexibility of the user interface. You can usually pick from an R:base System V menu by highlighting an option and pressing Enter. The movement of the highlighting is accomplished by using the arrow keys, numbers (if the options have them), or the first letter of the option. Indeed, flexibility seems to be the forte of this system. You can easily change the screen colors for the program and for your application, and the parameters for starting R:base System V allow such explicit commands as going directly from DOS to the Definition Express without displaying the logo that normally precedes the program, using blue foreground and white background. An area that lacks flexibility is printer control; you cannot readily access the command of fonts on the printer and other special functions. You would have to program around these limits or use a separate printer-control utility. However, R:base System V accommodates wide reports better than R:base Series 5000.

If you want to perform complex operations not included in the Express modules, you can go to the R:base environment to define them. Here you have a handy alternative to looking up commands in the manual until you remember them. The program has a Prompt-by-Example mode that groups the available commands into database manipulation, operations, and utilities. This is a great way to learn the language.

Suppose you want the minimum, maximum, sum, average, and standard deviation for the salaries of all accounting department personnel hired since last July. This falls under the category labeled "look at data," so you select it. You then select the table where that data resides from the on-screen list. You enter conditions such as "dept=accounting" by pointing at a list of choices. As you do this, R:base System V writes the command line across the top of the screen. This way you can see what the command language looks like as it goes together. You can then choose to execute, edit, or abandon the string of instructions you have created. When you're ready to work without Prompt-by-Example, you can press Escape to leave this mode. You receive great assistance if you mess up the syntax of a command; in some cases, a

help screen with a correct diagramming of commands is displayed. Many of the help screens are pop-up rather than full-screen, which is often preferable since you can compare the suggestions with your work that is still displayed.

Other Features

With all this power, R:base System V is likely to be given some large databases to handle. There is no program limit to an R:base database, just the limits of DOS. With large databases in use, users will appreciate the availability of archive commands that you can incorporate into applications. These commands let you perform backup and restore procedures without returning to DOS.

When more than one person needs to get into the database, R:base System V is ready to run in multiuser mode on a local area network. The commands to move into multiuser mode are straightforward. The multiuser installation is clearly explained in the documentation, and I found that it worked as described (not something I can say for all such installations I have done). For the control of shared information, basic security functions allow you to restrict access to defined areas of the application. The file-and-record locking allows everyone to look at the same record, but only one person can edit it. If someone makes changes to a record you are viewing, you see them right away.

When you look at your data from different angles, you will find the powerful Crosstab feature sometimes gives you the perspective you need. To find out, for example, how many units of your different products the sales staff has sold, cross-tabbing could list products vertically and sales people horizontally with a count of products by salesperson as well as totals for each product, all products, and all salespersons.

If it's number power over your data that you want, R:base System V's improved SuperMath feature will seldom let you down. Its 70 financial, trigonometric, statistical, and mathematic functions should be able to do the calculations you need. This includes reporting where 10 breakpoints per report are allowed for subtotals and field totals.

However, if you just can't get the kind of analysis you'd like from a database arrangement of your data, R:base System V lets you export files to the standard spreadsheet formats with a program called FileGateway, which is extremely easy to use. I was able to make a Lotus 1-2-3 spreadsheet out of my database with no trouble, and you are allowed to set specific parameters for the selection of data to be exported. To go the other way and bring data from spreadsheets or

APPLICATION REVIEWS

other databases is also very smooth. File-Gateway can read the file structure of the source data, replicate it in R:base, and provide you with a chance to modify it before completing the conversion. It also does a good job of reading data from dBASE III, whose users Microrim is clearly out to convert. However, Microrim assumes, with some justification, that if you make the move you'll decide to stay, since it doesn't provide a direct export to dBASE programs. [Editor's note: Since this review was written, Microrim released R:base System V version 1.1.

The new version includes a direct interface to Lotus' The Application Connection, the ability to transfer data files between mainframe and microcomputer databases, and the capacity to export as well as import data in a dBASE III and dBASE III Plus file format.]

With R:base System V, Microrim has met the formidable challenge of providing a friendly and encouraging environment that serves both the neophyte and the power user and that permits and facilitates the growth of applications beyond single-user limits. ■

Word Handler

Mick O'Neil

Word Handler from Advanced Logic Systems was one of the first Macintosh word processors released after Apple made the decision to unbundle MacWrite. Upon receiving a review copy of an early version of Word Handler, my initial excitement quickly turned to disappointment. Version 1.1 did some interesting things with words but included a nonstandard clipboard that was incompatible with the regular Macintosh clipboard. Thus, it prevented the importation of graphics into a Word Handler document. I attempted to get around this lapse by using the Import MacWrite Document option, but, alas, Word Handler replaced MacWrite document graphics with empty space.

Fortunately for all those original purchasers of Word Handler, the company has released version 1.6, which sells for \$79.95 and runs on the 512K Macintosh and Macintosh Plus. Upgrades are available for a \$2 shipping fee. Version 1.6 now incorporates a standard clipboard that makes the package a serious challenger in the Macintosh word processing market.

Handling Documents

Word Handler's Utilities menu offers some refreshing alternatives that should become standard in Macintosh word processors. For example, you can copy, rename, and delete a document from within the program. These file utilities are a marked improvement on MacWrite's required procedure of quitting the program, using the Finder for a file alteration, and then rebooting the program. Another useful option included in the utilities is Append Document, which allows you to combine several documents into one.

Document size is limited only by disk space. The on-line help feature under this menu is slow, but adequate. A word of caution about the Delete Document option: Deletion of a document will delete it from disk and will also remove the document from the active window.

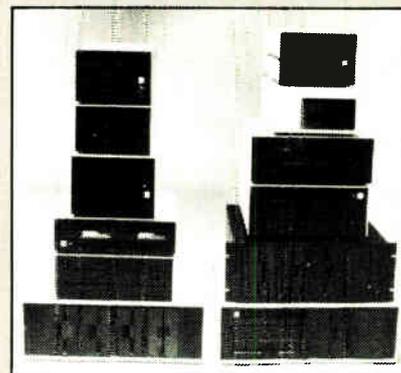
Like Microsoft Word, Word Handler allows you to work with up to four open documents. This feature makes it a simple matter to cut and paste between documents and is handy for reviewing outlines or notes while preparing correspondence. Unfortunately, the program doesn't have any convenient mechanism for organizing windows and lacks Word's window-expansion and window-contraction facilities.

Abbreviations and Forms

Another useful feature for serious writers is Word Handler's Abbreviation system. You can store abbreviations for often-used words or phrases and then recall them by simply typing the abbreviation and pressing a command-key combination. There is no limit on the number of abbreviations that you can store. The Abbreviation options are similar to Microsoft Word's Glossary feature, but much more intuitive. Still, Word's glossary is superior in its ability to store and recall multiple-line phrases, like addresses or headings, while Word Handler is limited to one line of 44 characters.

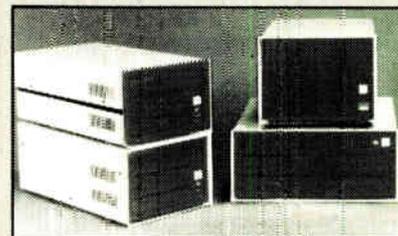
Word Handler includes an easy-to-use Form Fill feature that is handy for simple tasks like periodic bank correspondence where only a few fields change in value or for limited mail drops where the names and addresses vary. This should not be confused with Microsoft Word's full-*continued*

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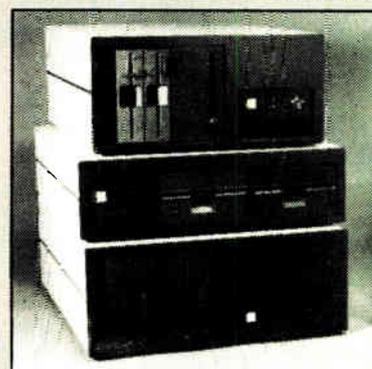
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Table 1: The results of performing various functions with Word Handler using a 4000-word text file converted to proper format. Note: All tests were done on a Macintosh Plus with the System file loaded on a RAM disk with the program disk in the internal drive and the data disk in the external drive. Run program shows the time required to run the program directly from the Finder. Load document refers to the time required to load a document while the program is running, while Load from Finder results from double-clicking the document icon while in Finder mode. Save document refers to the first save of a formatted text file, and Save revision shows the time required to resave the same document after it has been revised. Search document indicates the time required for the program to find a unique word inserted at the end of the file, and Scroll document refers to a manual scroll from the beginning of the document to the end. All times are in seconds.

	Word Handler	MacWrite	Microsoft Word 1.0
Run program	12.3	15.7	12.4
Load document	8.1	14.4	5.6
Load from Finder	22.2	26.6	15.7
Save document	.	12.4	23.3
Save revision	8.9	7.4	20.0
Search document	12.3	7.2	17.9
Scroll document	293.3	64.5	73.5

*The program has an automatic Save feature when you quit the program or close a document.

Word Handler version 1.6

Type

Word processor

Company

Advanced Logic Systems
1283 Rearwood Ave.
Sunnyvale, CA 94089
(408) 747-1988

Format

One 3½-inch, 400K-byte disk; not copy-protected

Computer

512K-byte Macintosh or Mac Plus

Language

C

Documentation

120-page user's manual

Price

\$79.95

tured Mail Merge capability. Word allows merging text from a text file, while with Word Handler you must enter data individually to fill in each form.

Other Features

A major improvement over MacWrite is Word Handler's flexibility in handling

margins. When you select Show Margin from the Format menu, the program displays a horizontal scroll bar that allows you to move the margin controls beyond the six-inch mark. A Mirror-Image Margins option is included in the print process, which adjusts margins on facing pages for binding purposes.

Other useful features include an accurate word count; a unique text-formatting function that inverts case, capitalizes words, capitalizes all letters, or converts them all to lowercase; and the standard MacWrite-type headers and footers that allow you to insert automatic pagination markers. The documentation is thorough and well-presented in a 120-page user's manual, and the software is provided on a single 3½-inch, 400K-byte disk that is not copy-protected.

Reservations

Word Handler departs from the normal Macintosh conventions by eliminating the Save As command from the File menu. In fact, documents are automatically saved upon quitting, and revisions replace originals as a matter of course. The program attempts to minimize problems in file-handling by including a Make Backup option when you open a document and by offering you a chance to make a second copy of a document from the Utilities menu. Still, I found myself getting lost in all this cautious logic.

continued

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May 86

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Jan 86

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Business Computer Digest
Aug 86

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Jerry Pournelle,
Byte Magazine Sept. 86

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Teleconnect Magazine
May 86

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World Record History

An irritating quirk in the program is the necessity of choosing the Format Section option to activate the ruler for setting or changing tabs or moving margins. One might assume that pointing at and dragging a tab icon would be enough of an indication that you want to reformat the section, and requiring you to first choose Format Section seems unnecessary.

Finally, Word Handler is sluggish at times. The program is particularly slow

when scrolling line by line (see table 1). Though Word Handler goes some way toward resolving this problem by including Next Paragraph and Next Page options, a smooth, quick line scroll is an important convenience to writers working on the Macintosh's small screen.

If Advanced Logic Systems can sort out the logic and speed of the program's formatting options, its program is poised to make a serious challenge to the low end

of the Macintosh word processing market. Nonetheless, the current version of Word Handler is a vast improvement on MacWrite and it provides some of the features of much more expensive programs. ■

Mick O'Neil (Box 544, APO, NY 09378) is a computer coordinator for the U.S. Department of Defense dependent schools in the U.K.

Lightning and Flash

Whitney Bolton

Lightning and Flash are disk-cache programs for the IBM PC and compatibles. They help application programs run faster by making disk access more efficient. Lightning is also available bundled with the Breakthru 286 board, which makes memory access faster by replacing the 8088 microprocessor chip with a cached 80286. Since the two packages carry different price tags, cater to different phases of computer activity, and offer different results, I'll concentrate on the software alone in this review.

Cache Benefits

Every time your system accesses the disk to read or write data, the platter spins, the

heads swing, and time passes while information is loaded or unloaded. Some software gets as much of its program and data files into RAM as possible, accessing the disk only for the first load and the final save. But most users can't choose their programs for this feature alone: Your favorite program may need frequent reads from overlay files.

You can prod a slow program in two ways. One method is to use a software utility to set up a RAM disk that masquerades as a drive but is really just part of RAM. However, RAM is volatile, so when the machine goes off, so does the information in the RAM drive. If your RAM drive is holding a program, no

problem: The original is still on your floppy disk. But if it is holding data, only the most recent version you saved to a disk will survive a blackout.

The second solution to slow programs is a disk cache. Like a RAM drive, a disk cache takes up a share of memory, so caching wasn't practical for microcomputers until the price of memory chips came down. Much of this extra memory can now be installed inexpensively with add-on boards that come complete with cache software. For example, Quad Master III, the software packaged with the Quadram Quadboard, includes a disk-cache program among its capabilities. But such a cache program isn't very flexible—you can decide on the size of the cache when you boot the system, but that's about all.

Working Cache

So what's a cache? It's a program that sets aside part of RAM to intercept all your application program's requests to the disk drive (by ambushing them in vector 13H). It honors read requests only for data or program files that haven't already been encached. It honors write requests only for data that's been changed. Sectors move in and out of the cache at about 50 times the speed of sectors moving to and from floppy disks.

Of course, the real increase in speed isn't anywhere near 50 times; internal processor speed, bus connections, and program design all take their toll. But a disk cache does get faster as your work session gets longer. The first read from disk takes as long with a cache as without. The next time, however, the cache program spots the familiar request and fills it from electronic memory. The more reads that are stashed in the cache, the more it remembers and the faster the application program runs. Although saving to disk is also speeded up, an application program that writes more than it reads won't benefit as much as one that reads more than it writes. In addition, application programs that already make the most of your available memory, such as

continued

Lightning version 4.40B

Type

Disk-cache program

Company

Personal Computer Support Group Inc.
11035 Harry Hines Blvd.
Suite 207
Dallas, TX 75229
(214) 351-0564

Format

One 5¼-inch disk

Computer

IBM PC, XT, AT, or compatible with a minimum of 128K bytes of RAM

Language

Assembly language

Documentation

81-page user's manual

Price

Copy-protected: \$49.95
Unprotected: \$89.95

Flash version 5.0

Type

Disk-cache program

Company

Software Masters
6223 Carrollton Ave.
Indianapolis, IN 46220
(317) 253-8088

Format

One 5¼-inch disk

Computer

IBM PC, XT, AT, or compatible with a minimum of 256K bytes of RAM

Language

Assembly language

Documentation

105-page user's manual

Price

\$69.95

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- * AC voltage: 200mv — 750v, 5 ranges
- * Resistance: 200 ohms — 20M ohms, 6 ranges
- * AC/DC current: 200uA — 10A, 6 ranges
- * Capacitance: 2000pf — 20uf, 3 ranges
- * Transistor tester: hFE test, NPN, PNP
- * Temperature tester: 0° — 2000° F
- * Conductance: 200ns
- * Fully over-load protected
- * Input impedance: 10M ohm



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- * Resistance: 200 ohms — 20M ohms, 6 ranges
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- * Input impedance: 10M ohm
- * 180 x 86 x 37mm, weighs 320 grams



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3.5 DIGIT AUTORANGING DMM

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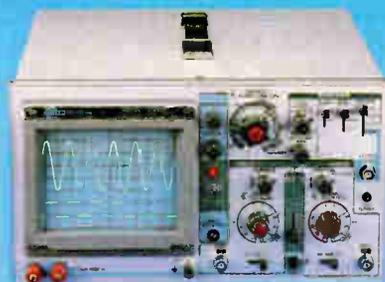
- * Basic DC accuracy: plus or minus 0.5%
- * DC voltage: 200mv — 1000v, autoranging or 5 manual ranges
- * AC voltage: 2v — 750v, autoranging or 4 manual ranges
- * Resistance: 200 ohms — 20M ohms, autoranging
- * AC/DC current: 20mA — 10A, 2 ranges
- * Fully over-load protected
- * Audible continuity tester
- * Input impedance: 10M ohm
- * 160 x 75 x 34mm, weighs 230 grams



DMM-100 \$29.95
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- * DC voltage: 2v — 1000v, 4 ranges
- * AC voltage: 200v — 750v, 2 ranges
- * Resistance: 2k ohms — 2M ohms, 4 ranges
- * DC current: 2mA — 2A, 4 ranges
- * Fully over-load protected
- * Input impedance: 10M ohm
- * 130 x 75 x 28mm, weighs 195 grams



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- * AC voltage: 2v — 500v, autoranging
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XyWrite, won't be the best candidates for caching, either.

Lightning

Lightning version 4.40B comes in a copy-protected version for \$49.95, or an unprotected version for \$89.95. The copy-protected version is a key disk that doesn't boot with DOS. You have to insert the copy-protected Lightning disk as a separate step at the start of every session.

Lightning's options allow you to choose the cache size at installation. As you work, you can check the performance of Lightning, turn the interception of requests to specific disk drives off and on, write-protect data on a specified drive, and unload the program if you want to use the RAM it occupies for something else. You can also call up a Lightning help screen that summarizes the syntax for these options. The user's manual is generally well written, but it is short. The order of the chapters—with installation instructions in Chapter XI—isn't logical.

Flash

Flash version 5.0 offers all the options of Lightning and more. [Editor's note: *The company has released version 5.3 of Flash since this review was written.*] Like Lightning, Flash supports expanded-memory formats such as the Lotus/Intel/Microsoft Expanded Memory Specification used with Intel's Above Board. But it also lets you perform many other functions, such as activating and deactivating a high-priority flag that prevents files from being swapped out of memory when the cache begins to get crowded; giving the program a list of files to direct straight

into high priority when you access them; teaching Flash where to read by both sector and track; flattening the program's learning curve by inserting data pointers; deactivating and reactivating the cache program without unloading it; and emptying the cache or emptying it only for a specific drive.

You can use the program without ever invoking any of these options or the others in the Flash bag of tricks. However, the Flash user's manual takes a purposeful 81 pages to demonstrate how you can use the options to make your cache more efficient. After all, a disk cache is in many ways like an intelligent RAM drive; the more intelligent it is, the better. Flash stands at the top of the class.

Cache Savings

I tried both programs on an IBM PC with two floppy disk drives and 640K bytes of RAM, first with Microsoft Word 3.0 and then with a disk-intensive file handler, PFS:File 2.0. With Word, I loaded a 20K-byte document, changed one character, and then saved it. Word takes 13 seconds to do this task; it spins off a .BAK file at the same time. Lightning cut the process down to 10.6 seconds the first time and did not speed up on the second and third tries. On its first attempt, Flash cut the process down to 9.9 seconds and, on its third attempt, to 6.8 seconds, little more than half the Word total.

With PFS:File, I sorted a simple 60-record file first alphabetically and then numerically. The unaided program took 10.3 seconds with both tasks. Lightning took 4.1 seconds with the first sort and 2.7 with the second; Flash made it in 6.6 seconds the first time and then in 2.9 on

its second try. Sorting a really large file with either Lightning or Flash would provide a very handsome cache discount. For example, if you save 1 second in every 6, the time savings is more significant for long files.

Hard Cache

Lightning's helpmate, the Breakthru 286 board, supplants the 8-bit, 4-MHz 8088 with an 80286 chip that has 16-bit-wide doors and an 8-MHz clock. The Breakthru board, a half-slot card that sells for \$395 with Lightning, buffers memory-writes and stores memory-reads in a fast 16K-byte on-board cache, so it isn't hobbled by the relatively slow main memory. It accepts an 80287 math coprocessor chip, so it offers a speed-up option over the 8087 chip for number-juggling operations like computer-assisted design.

The Breakthru 286 won't greatly speed up saving and sorting, which chiefly involve disk access. For these activities, there's the disk-cache program. But for activities that demand memory access, such as searching and scrolling, the quicker chip is much faster than the 8088.

Hardware options like the Breakthru 286 board span the generation gap between your aging 8088 model and the peppy 286 youngsters, enhancing memory access but at a higher price. Well-written, well-documented software like Lightning and Flash can make the disk-intensive action quicker for only \$49.95 and up. ■

Whitney Bolton (96 Moore St., Princeton, NJ 08540) is a professor of English and the author of many books and articles.

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REVIEW FEEDBACK

Scribble!

I'm writing in response to the Scribble! review by Warren Block (January) and want to emphasize several statements in the review and correct some additional points.

As Mr. Block states, some features in Scribble! work flawlessly with Kickstart 1.2 but work inconsistently with Kickstart 1.1. This is due to Kickstart problems, not problems with Scribble!. The scroll-bar flicker is also caused by Kickstart 1.1 and will not occur with 1.2. Similarly, requesters are activated with 1.2 and you can access gadgets through the keyboard by pressing the first letter of the gadget.

Mr. Block also mentions a problem with closing windows. Project Quit and Project Close are two very different functions. Project Close will close the current window; Project Quit will quit the current project. By pressing the F4 key, you can save a project throughout its creation. If necessary, you can press F4 after every single word, number, or any stroke pressed.

Help is accessed by pressing the F1 key. Micro-Systems Software also sells FunKey Strips!, a function-key-definition template that fits into the slot of the Amiga keyboard directly above the function keys.

Finally, all commands are segregated logically; the keys on the right side of the keyboard respond to menu items, while the Alt keys are for all other nonmenu commands. The Ctrl keys are WordStar-compatible keyboard commands for those who are familiar with the IBM product.

Esther L. Appleman
Micro-Systems Software Inc.
Boca Raton, FL

MTBASIC

Frederick D. Davis's review of MTBASIC (January) may be misleading, since the version he examined is at least a year old. The current version, 3.0, has a built-in editor and allows you to examine the values of variables after a run. Full graphics and color support are now included, as well as other features.

Mr. Davis complains that the allocation of time among tasks is "erratic." "Not immediately obvious" would be a better choice of words. MTBASIC provides a true multitasking environment within the confines of MS-DOS. MS-DOS's lack of re-entry makes it impossible for MTBASIC to allow more than one task at a time to do system calls. Therefore, MTBASIC blocks a

task's execution until the system call is complete, and it then resumes. As a result, tasks execute asynchronously with respect to each other.

Jack Ganssle
President, Sofaid Inc.
Columbia, MD

Thank you for taking an interest in multitasking BASIC with Frederick D. Davis's review of MTBASIC. He did a good overall job of reviewing, but one fact should be corrected. The MTBASIC language is not the first multitasking BASIC. Analog Devices' MACBASIC language, originally written for the Analog Devices' model 150 computer, was ported to the IBM industrial XT about two years ago.

MACBASIC, which runs under Concurrent CP/M, is a fully interactive compiler complete with syntax checking and line editing. Like most interpreters, you can check values of variables after running the program. There is no problem with stopping a program. Ctrl-B works, although the language lets you disable it during disk operations. Variables need not be declared. Time allocation for periodic tasks is handled in a logical manner, and an overrun counter is available. Overtime tasks will start again at their next regular time. Another advantage is being able to drive a plotter from BASIC commands. MACBASIC is available from Analog Devices Inc., 2 Technology Way, P.O. Box 9106, Norwood, MA 02062, (617) 329-4700.

Tom Roskelley
Kalkaska, MI

Evaluation Team Report

I read the product evaluation of IBM PC AT compatibles by the Arizona State University team (January) with great interest and some misgivings. It is always interesting to see what opposition is being offered to IBM and what is available in the market.

My misgivings arise from the reviewers' use of The Norton Utilities' Sysinfo. I have found this utility to be grossly misleading as an indicator of calculation speed. For example, my Eagle 1630 with an 8-MHz 8086 and an 8087 coprocessor has a speed of 1.1 seconds using Sysinfo. A colleague has an IBM PC AT with a 6-MHz 80286 and a coprocessor installed that has a speed of 5.8 seconds using Sysinfo. Yet a computationally intensive program of mine takes 20 minutes on my Eagle and 40 min-

utes on his IBM. These times are exclusive of data-in/data-out times.

Sysinfo is not a good indicator of anything and should certainly not be used in comparative ratings of hardware.

W. R. Hunter
Springfield, VA

In the Evaluation Team Report of the IBM PC AT compatibles, the authors claim to have tested PC-DOS 3.0 on the computers. I don't know what the effect of 3.0 is, but I can tell you that PC-DOS 3.1 will not completely work on a Sperry PC/IT. Try to format a few floppy disks with PC-DOS 3.1 on this machine and see what happens! I also found that PC-DOS 3.1 will not work at all on a Sperry 8088 clone.

Doug McGarrett
Jamaica, NY

Stride 440

I noticed as I read Paul A. Sand's review of the Stride 400 (January) that he didn't like the Wyse keyboard's audible feedback. To turn the key clicks off, simply type Shift-Enter (not Return). See page 32 of the Quick Reference Guide that is packaged with every Wyse WY-50 terminal.

Andrew Zimmerman
Ephrata, PA

A letter from Stride Micro informed us that the company's correct address is 680 South Rock Blvd., P.O. Box 30016, Reno, NV 89520-0016. Also, Stride Micro now offers revised manuals, p-System 4.22, and a 68020 upgrade option for the Stride 440.

Cathryn Baskin
Senior Technical Editor, Reviews

Correction

In the 23 *Modems* review (December 1986), the three signal levels used in the series of impairment tests were -8 dBm (decibels referenced to 1 milliwatt, measured at the modem), -16 dBm, and -26 dBm. The levels were incorrectly reported as -5 dBm, -15 dBm, and -25 dBm in the review and in the Review Feedback in the March issue. ■

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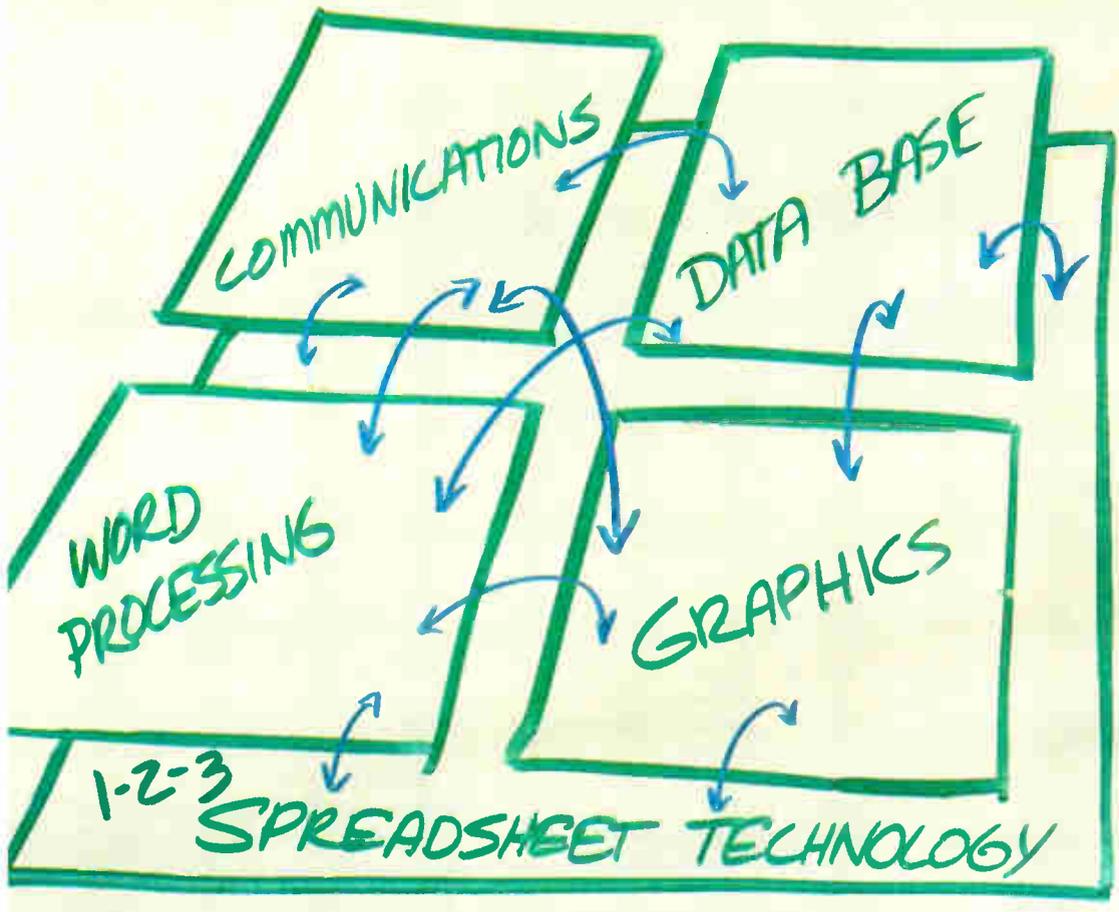
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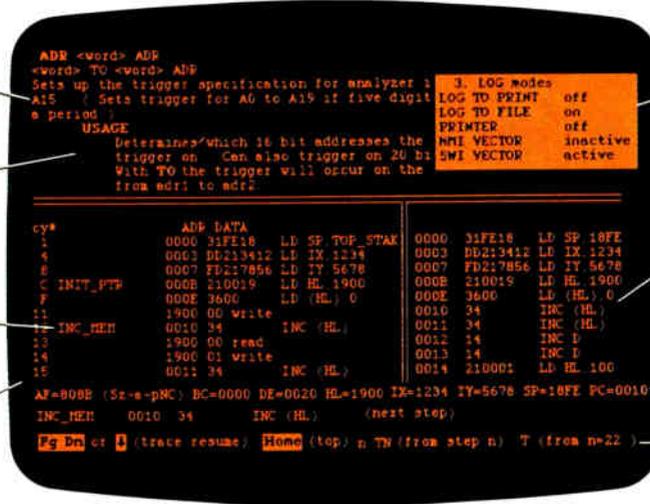
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Back to Work!

Jerry Pournelle

The curse is lifted, and Jerry chooses the best and worst of 1986

I started this two days before Christmas. It's much later than that now. In fact, we're well into January, and the column is overdue. Sigh.

Since this is the year's-end column, it will have my annual Best of the Year Awards, and since it comes out in the April *BYTE*, it's also the appropriate place to mention the year's greatest follies.

First though, an update.

All Systems Go

Last month, my most important systems were acting funny. I'm pleased to report that's a thing of the past. This month we're in great shape, barring a minor glitch or two.

First, the Golem, my big CompuPro 286/Z80 system. The Golem came back from his refurbishing with a new 80-megabyte hard disk. When he first came back, I had some problems because they'd set a jumper wrong on the PC Video Board (which is an S-100 board that emulates an IBM PC screen so well that it will run Flight Simulator and other stuff like that, as long as it's reasonably well behaved, which, alas, most PC software isn't). I fooled around with the system for a while without much luck. Then Tony Pietsch came over, and in an hour or so the Golem wasn't just running: it was *zinging*.

The Golem has two 8-inch disk drives, an 80-megabyte hard disk, a 5¼-inch 96-tpi drive, 2 megabytes of M-Drive/H (RAM disk), and a tape drive for backup. The tape system is about 25 percent slower than 8-inch disk drives, but whereas the disks will hold a megabyte each, the tapes hold 10. It takes about half an hour to servo-write and format one of the tapes, but it's a job that can run unattended, and once done needn't ever be done again. After that, backing up an entire disk directory is a matter of following menu prompts. You can also do it with a batch file.

The CompuPro under Concurrent

DOS is *fast*. At the moment, it's controlled by the PC Video Board driven by a Data Desk keyboard and our ancient but absolutely reliable TeleVideo 950. It's also linked, using CompuPro's networking systems, to a CompuPro 10 "Shirley" that's about to become the major system for everyone else in the house; Big Kat, the Kaypro 286i PC AT clone; and Lucy Van Pelt, the genuine IBM PC we keep downstairs. There's also a way to connect to Zeke, the ancient CompuPro Z80 I'm writing this on, but in fact it's easier to "link" those two simply by moving 8-inch disks. In some cases, parallel is faster than serial . . .

Networks

The net works fine. I can move files off Big Kat over to the Golem, where I can work on them with a good macro editor (I still use Word Master). I can also use Crosstalk to capture BIX files and send them over to the Golem's 80-megabyte hard disk. That disk has one logical drive formatted as PC-DOS media; the rest are formatted as Concurrent CP/M. For text and data files it makes no difference which way things are stored, but, of course, PC command files have to be executed off the PC format.

The CompuPro system uses Arcnet, which they license from Datapoint. Viasyn makes networking boards for their S-100 and modified S-100 CompuPro systems and PCompatible boards that drop into any slot on your PC or AT. Arcnet connects with coaxial cable. Coax isn't terribly expensive, and it's not too hard to make up cables to length provided you have the right tools: a coax stripper is essential. When Viasyn's Kevin Fischer came down to set up my net, he brought a special crimping tool that makes the job

even simpler, but I'm told that particular model costs more than a hundred dollars.

Setting up the net was simple enough for Kevin, who's in charge of training for Viasyn. I expect it would have taken me a

bit longer. The manuals aren't really bad—Viasyn has apparently abandoned the notion that manuals are a mere afterthought—but they're pretty terse.

We had one difficulty, a conflict between the Orchid ECCELL expanded memory board and the CompuPro net board—just when I'd got the ECCELL working in Big Kat. Sigh. The CompuPro board has a couple of kilobytes of on-board RAM, and while it's not critical where that's addressed, it has to be addressed *somewhere* that doesn't overlap with memory already installed. The net also needs some unused I/O ports (the 8086/8088 has 256 of them, so you needn't worry: some will be available) and unused vectored interrupts. All that's resettable on the CompuPro NET-PC board. Kevin Fischer was able to take care of the problem easily, but as I look at the manuals I think it might have taken me all day and a couple of phone calls. They certainly assume you're familiar with hexadecimal math.

On the other hand, the board dropped into the IBM PC and ran first time at the default settings. If I were setting up a net I might be tempted to try it first by myself, but for anyone with a critical need, I'd strongly recommend dealing with a CompuPro Systems Center. As usual, Pournelle's law applies: If you don't know what you're doing, deal with someone who does.

I've had the network up and running for only a day, and I'm already wondering how I lived without it. Since Shirley

continued

Jerry Pournelle holds a doctorate in psychology and is a science fiction writer who also earns a comfortable living writing about computers present and future.

the CompuPro 10 has four Z80s, each with its own block of user memory, it runs WRITE fine; meaning that Mrs. Pournelle can use her Ampex terminal to write her books and stash the work on the Shirley's hard disk, while I can periodically use the net to back up her files on the Golem's hard disk, 8-inch drives, or tape backup system.

Meanwhile, we can send text files to and from Lucy Van Pelt and Big Kat and move stuff in and out of BIX to and from any of the computers on the net. We can even use the Golem to do spelling checking of files stored on the Shirley without moving the files at all.

It isn't perfect. For one thing, DOS isn't smart enough to participate directly in the net: to get something to or from one of the IBM PC-DOS machines, we have to give the commands at *that* machine. Concurrent DOS is smart enough to let you do it remotely: Roberta can run the spelling check program located on the Golem's hard disk against a file on the Shirley without transferring anything to or from either machine.

At the moment, we don't have any provision for networking Atari, Amiga, or Macintosh machines into the system. I understand Corvus can probably do it, but Corvus uses a different networking system entirely, with twisted pairs rather than coax cable.

Networking raises some interesting ethical and legal problems. Consider the spelling checking example I gave above. If I transfer the spelling program directly to Shirley without erasing it from the Golem, I'm clearly in violation of the licensing agreement. Suppose, though, I run it in Shirley but access it from the Golem through the net. We now have the program in two different computers—on disk in one and in the other's main memory—but it's being run by only one person.

Suppose, though, that while Roberta is running that spelling program, I also invoke it on the Golem. We now have the program in use by two people at once, and that's surely unethical as well as illegal.

I expect I'll have a lot more to say about networks in the next few months.

Big Kat

When I left off last month, Big Kat was working off his hard disks but couldn't find his floppies. I'd diagnosed that as a problem with the disk controller, and the technicians at Kaypro agreed. They sent out a new controller board. Since Big Kat's clock had been acting funny whenever he was turned off, they sent a new battery as well; and while they were at it, they sent the latest revisions of the Kay-

pro ROMs. Now it was up to me.

Disassembling Big Kat is easy enough. There are several cables running to the disk controller board, and none are marked; so with the new board set parallel to the old, I took a marking pen and proceeded to mark both cables and the places they plugged in. I don't know if you can get the cables in backward on a Kaypro, but you sure can on a lot of computers, so why take chances?

I also installed the new battery. Once you've done that, you have erased the small RAM the 286i uses to store your setup options in.

Now it was time to change ROMs. Again I'm a worrier: there are four sockets but only two ROM chips, and once you have pulled out a chip, you'd be amazed at how quickly you can be confused about where it used to be. Or at least *I* can be confused, and I'd rather not be. One possibility would be a Polaroid snapshot, but this is simple enough for a pencil-and-paper diagram.

I used a chip puller; getting down inside the machine with a small flathead screwdriver to pry out the chip isn't easy. Pulling the chips was no problem. Putting them in nearly drove me crazy.

I did everything right. Examine the chip. Make sure all the pins are straight. Put it carefully in place and look again to be sure the pins all fit in the socket, then get out a powerful flashlight and look again. Then push in carefully—and watch several pins buckle and bend.

Don't panic. Out comes the flathead alligator pliers. Ground myself carefully. Straighten the pins carefully. Now it has to go back in—

Which was where I got smart.

Two years ago I gave a product of the year award to Tweek, a contact enhancer fluid that solves all kinds of problems with PCs. It came to me as in a vision that this was exactly what I needed here. I still have a nearly infinite supply—a little of that stuff goes a *long* way—so I fished it out of the tool cabinet and ran a bit of it along the newly straightened pins.

Presto!, the chip went in with no effort at all. In future I'll *never* insert chips without first lubricating with that stuff.

After that it was all simple. Of course Big Kat came up nearly blind, booting off a floppy and unable to find his hard disk. I had to scramble around until I found the Kaypro utility disk with the Setup program on it; there's a new version that seems to know about Orchid extended memory boards. I'm still having some problems with EMS (expanded memory specification) standards, but the RAM disk works fine, and I have a new program that seems to be able to use the RAM disk for swapping in EMS. More

on that next month.

The Kaypro Setup program is self-prompting, and once it was all done I did Ctrl-Alt-Del. Presto! Big Kat was as good as new. The whole thing hadn't taken more than an hour.

One thing bothers me a bit. The Kaypro invoice for a new disk controller board is \$450; I have seen whole drive systems advertised for less than that.

Back to Normal

Anyway, all the machines are working again, and I'm writing this on Zeke II, the world's least portable microcomputer. Not that this keeps him from being carried about. Just after Thanksgiving, in what is turning out to be a ritual, I took old Zeke off to a motel about 50 miles from here, and from Tuesday noon until Sunday evening I didn't talk on the phone or do much of anything but work. The result was that *Storms of Victory*, volume III of the *Janissaries* series, is finished and ought to be out in hardbound from Ace Books before May; and I got home and put out volume II of the *Imperial Stars* series, *Republic and Empire*.

If that weren't enough, I answered a couple of hundred letters, stuffed a lot of software into the machines, and managed to get up to Alamo, California, for the wedding of Pam Clark, onetime managing editor of BYTE; and the day after Christmas, Barbara Clifford, Jim Ransom, Mike Hyson, and Larry Niven will be over here for the whole weekend to work on *America: A Spacefaring Nation Again* (Baen Books); we ought to have that in print by next fall.

Keyboards

If you have a lot of computers, going from one to another will drive you nuts: every time you change, the keyboard is different.

The original IBM PC keyboard was wretched, although it did have what I thought was a pretty good feel. Some people didn't like the clicky noises it made, but I rather did. What was awful was the layout.

The AT keyboard was better, but it had problems, too. The Escape key is in the wrong place. Backspace is *way* too far away from the home keys—who needs to have the \ | key up there, anyway? And if you type much text, you'll greatly appreciate having the uppercase of comma and period be comma and period; the > and < symbols can be off somewhere on the side. The AT keyboard also makes you share the arrow and numeric pad keys, which is a pain.

Still, I'd rather have the AT keyboard than the PC one, and when Data Desk In-

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World Radio History

ternational came out with an AT-style keyboard for the PC, I was eager to get one. They also did a version for the AT—the AT and the PC translate the keyboard codes differently, so it takes a different ROM.

The keyboard that came with Big Kat is all right, but it was never one of my favorites for touch and feel. I first substituted the Enigma keyboard. That worked pretty well, but it's large and heavy, and again the touch isn't the positive action that a genuine PC keyboard had; and for most of last year, I used a Data Desk keyboard on both Big Kat and the Golem.

In December, Data Desk brought out the Turbo-101 Enhanced Keyboard. This one has a number of nifty features, including two Ctrl and Alt keys on different sides of the board so you can make nearly any control keystroke one-handed. The Escape key isn't exactly where I want it, but at least it's in the upper left corner. There's a separate cursor pad, again not quite as I'd have laid it out, but better than acceptable.

It also has some switches underneath: the Turbo-101 will work with PC, PCjr, and PC AT computers, so you can carry it from one machine to the other.

Finally, the Turbo-101 has the "new

IBM style" function key system: 12 function keys across the top of the keyboard. Eventually, one supposes, most keyboards will be laid out this way, but for just now that causes some problems. For example, WordPerfect is a pretty good text editor, but it has a zillion commands for all 10 function keys: function key, Shift function key, Ctrl function key, and Alt function key all do something different. It's impossible to remember all those commands. WordPerfect comes with a little template to fit around the function key groups as they are on the standard PC and AT (and the original Data Desk) keyboards. They also make another one in a strip model, and it sort of fits above the Turbo-101's function keys, but you'll need some tape to hold it there.

If you're particular about keyboards, you'll probably like the Turbo-101. I sure like mine.

Flash: Data Desk now has a Turbo-101 that works with the Macintosh. It's about time the Mac had a decent keyboard.

The Incredible PC Type Right

Mike Weiner, who brought you the incomparable Word Finder, has done it again.

PC Type Right is another product de-

veloped by Mike Weiner of Microlytics for Xerox. This time Xerox is going to do its own marketing, through Softsel. Type Right is an on-the-fly spelling checker; but it's like no other.

It doesn't look like much: a box about the size of two packages of cigarettes laid end to end and cables. Mine came with two cables, one for a PC AT, the other for an XT. Installing PC Type Right consists of plugging it into your keyboard and computer. Turning it on takes about two minutes of reading; the manual is exceptionally clear, but then this thing is exceptionally simple to use. It toggles on and off from the keyboard by doing Alt*.

After that, when you type a word not in its vocabulary, the box beeps twice. Not loudly; and indeed you can, from the keyboard, change the pitch and duration of the beeps.

The dictionary is awfully good: there are 100,000 words in it, including, I'm told, most of my own personal computer dictionary; that is, I sent Mike Weiner a copy of the Word Plus special dictionary I've built over the years writing this column and my computer books, and they incorporated it into their already excellent word list. I've tested PC Type Right,

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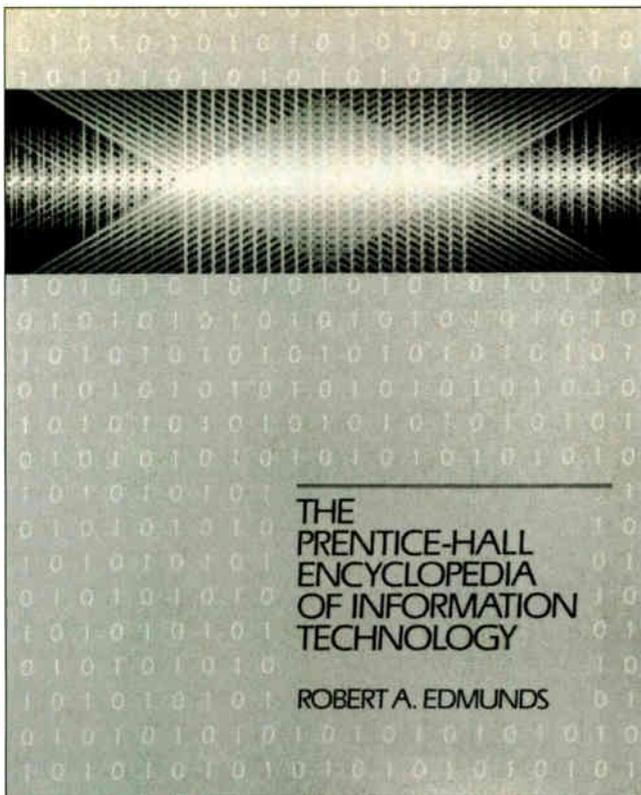
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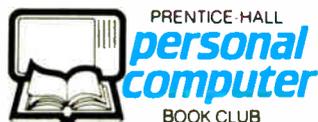


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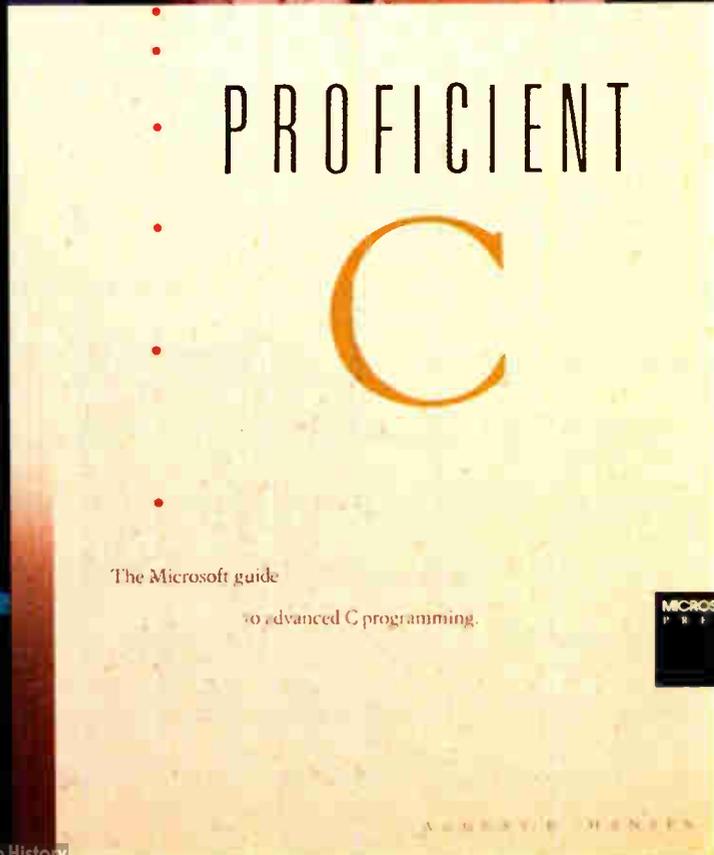
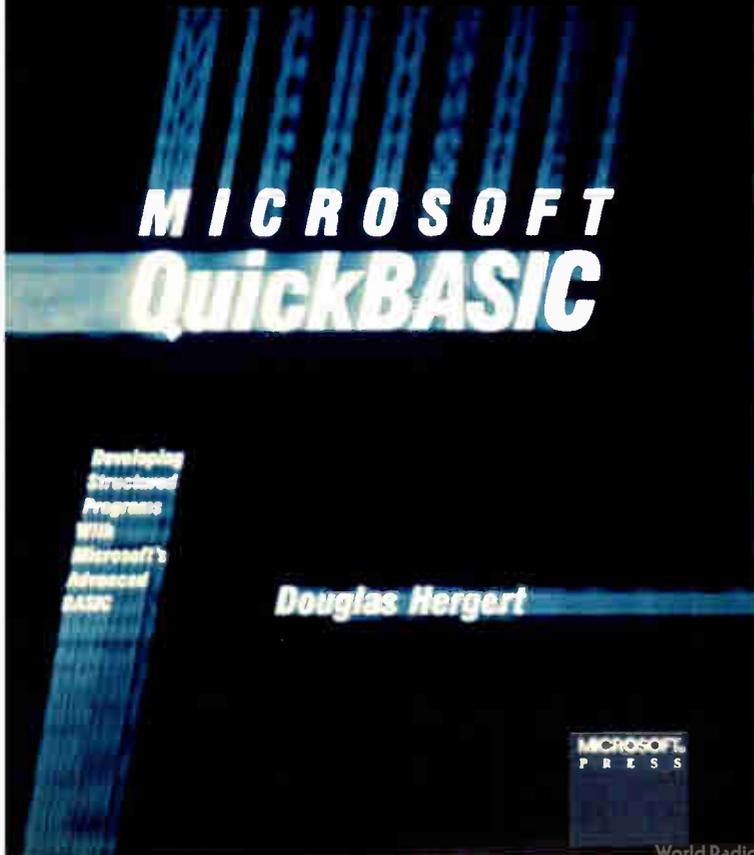
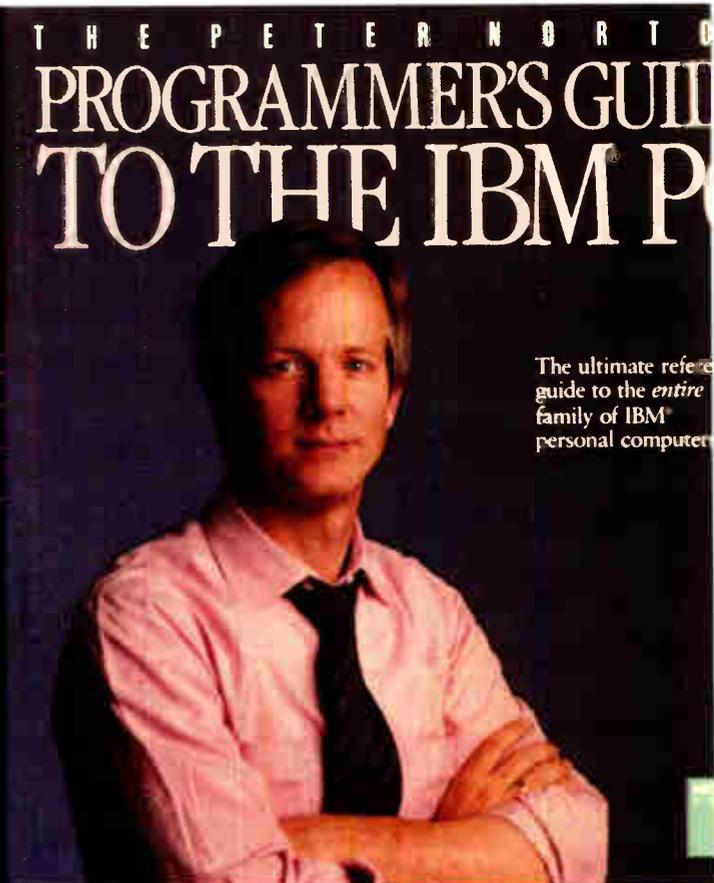
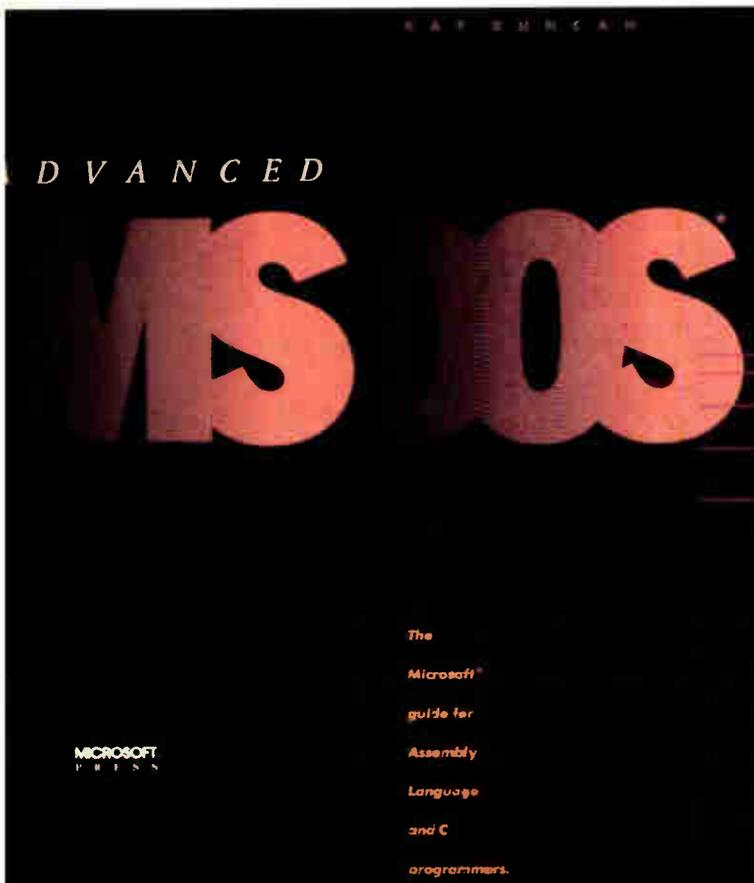
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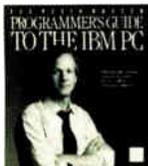
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and it knows most of the words I want it to; it glitches on "pournelle" but not "Pournelle." It knows "gizmo" and "glitch." And so forth.

Better still, you can add words. Not a lot; the literature says 1200. But since PC Type Right's dictionary knows thousands of words that other spelling check programs do not know, 1200 may well be enough.

I find on-line spelling checkers annoying when I'm trying to do creative writing and generally prefer to run the finished product through Word Plus (or WordPerfect's very nice spelling checker if I'm writing with that); but for letters, and memos composed on-line for MCI or BIX, and other things that are never going to be put through a spelling checker, this thing is pretty valuable. It's incredibly fast, it takes up no memory, and you can turn it on and off with a single command. The vocabulary is huge. If you want a thesaurus, there's always Word Finder.

If you need an on-line spelling checker, this is the one to get.

Faster than Light

Fair warning: Barry Workman is an old friend, and my son Alex is VP of R&D there, so I suppose you could say I've some bias toward Workman and Associates. On the other hand, I've good reason to believe they're good guys.

Anyway, Workman has come out with a new version of FTL Modula-2 for PCs and compatibles. If you get the FTL compiler, math library, and the editor toolkit, you'll have one of the best deals of the year.

FTL now has longcard and longint data types. There's also an 8087 math library. The neat part about that is that the math library senses the presence of the 8087 and uses that if available; otherwise, it does the calculations in software. All the data types are compatible between 8087 and non-8087 versions.

Like CP/M FTL Modula-2, the PC version was written by Dave Moore, an Australian programmer who writes some of the neatest code I've ever seen. Everything he does runs *fast*, and PC FTL Modula-2 is no exception. The FTL package comes with built-in editor, linker, and assembler. The documents were either written by my son Alex or edited by him. I think he's done a good job; certainly he shares my prejudices for examples.

The best deal, though, is the optional editor toolkit; this is the Modula-2 source code for the editor, and it really is: if you compile the sources with the FTL compiler, you get the identical editor Workman ships. I know of at least two people

PC Type Right is incredibly fast, takes up no memory, and you can turn it on and off with a single command.

who are using this editor to write a PC version of WRITE in Modula-2. After they get that going, I'll suggest some additional features.

I haven't done enough tests to make a fair comparison between Logitech Modula-2 and FTL. FTL is definitely faster, but Logitech sells more debugging tools; their dynamic debugger is a bit of a wonder. On the other hand, professional programmers might want to look at FTL's libraries, and even if they do the development in Logitech Modula-2, they might consider recompiling programs with FTL to see if they'll run faster.

Beginners and students need FTL Modula-2; it's fast, and if you get the editor toolkit you'll not only have examples of well-tested code, but a bunch of modules you can incorporate into other programs.

Highly recommended.

Logicadd and Other Good Stuff

One of the best things to come out this year was Generic CADD for the PC. This is a low-cost CAD program that does an awful lot of what the big expensive ones do and comes with a well-written manual that makes it fairly easy to learn.

Logicadd is Generic CADD and the Logitech Logimouse in a combination package; if you want a CAD program and don't have a mouse, this is the combination to buy. I always did like the Generic CADD documents. The Logicadd documents are the same as Generic CADD, but perfect-bound rather than wire-bound; the book won't lie flat without a ruler to hold it open.

Logitech has also brought out the Turbo Pascal to Logitech Modula-2/86 Translator. The name tells what it does, but in fact the program is valuable even if you don't have any Turbo Pascal programs to translate. By discussing the differences between Turbo Pascal and Modula-2, the manual manages to give a great number of examples of Modula-2 code.

Indeed, the chapter "Advanced Software Engineering Using Modula-2" is worth the price of the package by itself; careful study of how the translator works, with attention to why it does that, plus ex-

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amination of the examples will tell you a lot about the Modula-2 philosophy.

Any Turbo Pascal user who's curious about Modula-2 will find this package invaluable.

Finally, there's Logipaint Set, which you can also buy with the Logimouse. I confess I've done so little with this that I can't compare it with anything; I'm quite pleased with RIX SoftWork's EGA Paint, and so far I've had no real reason to do more with Logipaint Set than scribble around. More on this one another time.

WordStar 4

The main complaint people have about WordStar is that MicroPro never updated it after version 3.3; but that, I'm glad to say, is over.

I got a test copy of version 4 about a week ago, and I haven't had a chance to really wring this out for bugs. Maybe there won't be any. It's pretty clear that 4 is strongly based on NewWord, and that was pretty thoroughly tested. On the other hand, this isn't *just* NewWord. There are some additional features.

From everything I've seen, if you liked WordStar—and an awful lot of people did—you'll love this. I can't imagine anyone will prefer WordStar 2000. WordStar 4 puts MicroPro back in the game as a serious contender again.

WordPerfect Once More

Regular readers will recall that due to machine failures a couple of months ago, I decided I'd better get used to writing with a PC-DOS text editor. After considerable trial and error, I started using WordPerfect. Eventually, I developed a love/hate relationship with the program, much like the one I had with WordStar; but I kept using it.

Meanwhile, WordPerfect has once again been improved; at least I have a new version that promises a whole bunch of features, including column math, a certain degree of automatic indexing and concordance generation, and improved footnote handling. I also see that some of the document deficiencies have been fixed.

Along with the new version of WordPerfect, they sent, just for me, a disk with a complex macro that will go through a WordPerfect file and convert the WP italic codes to underbars. It does this by finding the "underline on" code, backspacing, inserting an underbar, etc.; when it's finished, it recursively calls itself. Since going to the beginning of the document is part of the macro, this thing takes a bit of time if the document is very long; but it does work and illustrates just what you can do with WordPerfect's

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macro capability. Indeed, it's intriguing enough that I expect I'll spend some time studying just what else WP macros can accomplish. I don't think it has the flexibility that old Word Master had under CP/M, but then not very much does.

Anyway, I've got WordPerfect installed on the Z-181 as well as on the Kaypro 286i, and I find I'm getting used to it. I haven't found out whether it will work under Concurrent DOS or not; if it will, I expect my search is over. There are still things I wish it did differently, but you can't have everything.

Jot!

I once collaborated on a book with my friend G. C. Edmundson. That was back in the early days, just about the time I was getting Ezekial, my friend who happened to be a Z80 computer. When Gary sent me the manuscript of his first draft, I discovered it was *crammed* with shorthand abbreviations.

It made sense, of course. After all, the manuscript was going to be retyped, so why bother to spell out all the words? I later learned that a number of writers employ that trick. I never did, but anyone who does may be interested in Jot!, a PC-DOS RAM-resident utility that expands

abbreviations as you type them. Thus, if you like typing "w/o" as short for "without," you can teach that to Jot!, whereupon the program will dutifully expand your abbreviation as soon as you finish typing it.

It's a little weird watching it do that; weird enough that I don't use Jot! very much. On the other hand, I can see that if I got used to it, this program could increase my productivity. I'm pretty sure Gary will use it, once he gets a PC-DOS machine. What he bought after he saw Ezekial was, of all things, one of the very first Altos machines, handmade in a garage when Altos was a start-up company. It now serves as a dedicated word processor and still works quite well.

Jot! won't work with EGA, but like Ready! it does know how to make use of Lotus/Intel/Microsoft expanded memory. That's fairly important if you, like me, have a full-up machine and are still running out of memory because of all the RAM-resident software.

RS-232C Blues

The next time someone talks about the "RS-232C standard" I'm going to throw something heavy at them.

PCXFER is a program that transfers

files from PC machines to the Z-181 portable. The instructions say, "Use a null-modem cable."

That turns out to be a silly instruction. If you go to a computer store and ask for a "null-modem cable," they may or may not have anything to sell you; but if they do, it probably won't be the right one for the PCXFER program. There are, it seems, a wide variety of cables, none alike, that answer to the name "null modem."

I found that out the hard way. Eventually, I got the actual cable connections required for the Zenith transfer, and they're complicated: Pin 1 goes straight through. Cross-connect (i.e., swap over) pins 2 and 3. Cross-connect pins 4 and 5. Cross-connect pins 6 and 20. Pins 7 and 8 go straight through.

If you don't have a special cable made, or make your own, that turns out not to be an easy task. When PCXFER didn't work, I couldn't tell if I had problems with the Kaypro 286i, the Zenith Z-181, the cable, or the PCXFER program. I was about to go nuts, when I remembered WireTap.

WireTap is one of the most useful little gadgets I ever saw. It substitutes for a full

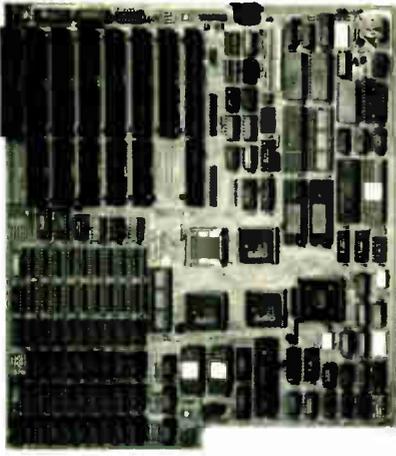
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breakout box or SmartCable. WireTap has both switches and sockets for pins 2, 3, 4, 5, 6, 8, and 20; the switches disconnect, and you can then use little patch wires to cross-connect. In addition, there are red and green LEDs; red shows that pin has plus (high) state, and green shows negative or low.

WireTap let me make up the goofy cross-connections Zenith means by "null modem"; and when I plugged it into Big Kat's com port, I found a pattern of lights nothing like what I got out of either the Z-181 or the IBM PC. That was enough warning. I tested PCXFER on the regular PC, and it works like a charm. I'll figure out what's wrong with Big Kat's serial port next week. Probably a jumper.

Folly of the Year

It's time for my annual Folly of the Year Award. As usual, I invite readers to make nominations; this year I had an "onions" topic in my BIX conference, so I got a lot of nominations.

The nominees were IBM, for the PC XT Model 286; IBM again, for the software test attempting to enforce the 6-megahertz clock speed on the AT; Apple Computer, for their "look and feel" lawsuit; and Haba, for Hippo-C.

After considerable thought, the Pournelle Onion goes to IBM for the Model 286, which tried to set the industry back two years so that IBM could sell some old 286 chips.

Best of the Year

This shouldn't be thought of as any big deal. I get tons of stuff every year, and I

can't possibly evaluate it all. I'm sure to overlook a lot of important products.

The ground rules for this are a bit different from most annual awards. In my case, these are products I got this year, regardless of when they were first produced; and it's all completely subjective, based largely on how useful they've been to me. As it happens, I'm still using most of the equipment and software I was using last year. My main PC clone is Big Kat; the most useful "big" system is the Golem, a CompuPro System C; and I carry the NEC PC-8201, with Purple Computing's wonderful Sidecar memory box, nearly everywhere I go. I write with WRITE, communicate over an OmniTel modem with Crosstalk, and do what spreadsheets I do (mostly expense accounts) with SuperCalc. The printer is controlled with Applied Creative Technology's Printer Optimizer. I've had and used all of those for more than a year, and I don't see any reason to change to anything else.

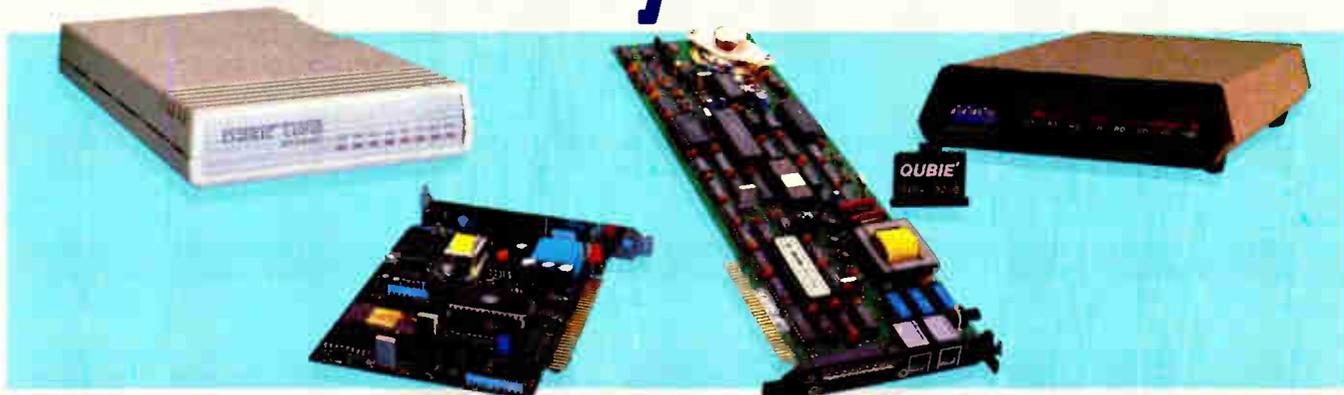
However, of the things that have come in this year, some have been more useful than others. Herewith, the lowest-key awards in the industry.

Utility software: XenoCopy-PC. This PC-DOS program reads any of about 200 different disk formats—examples include HP-125, TRSDOS Color Computer, Epson Valdocs, and a whole bunch of stuff—and copies files from the foreign format to PC-DOS format. It's simple to use, reasonably priced, and works like a charm. Given all the weird stuff I get, I don't see how I could live without it.

Language: Workman's FTL Modula-2

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Game of the year: the most spectacular was StarGlider for the Atari ST; but the one that impresses me most is Starflight for the PC. StarGlider is an arcade-like game. Starflight is a game of strategy and

exploration. One tip on Starflight: have your printer on, and use Print Screen often; otherwise, you'll never remember all the things the aliens tell you.

In the hardware category, the Atari ST wins hands down as the most useful and exciting machine I acquired in 1986, with honorable mention to the Amiga. The most improved machine of 1986 was the upgrade from Macintosh to Mac Plus.

The most useful gadget this year was WireTap. I suppose a full breakout box might be preferable, but this is more portable and seems to be as useful.

Portable of the year is the Zenith Z-181. If you intend to carry a full-service computer from place to place, this is the right machine. The screen is easy to read, and even using the disk drives fairly often it runs several hours on a battery charge. At 11 pounds it's not light, but neither is it impossibly heavy to carry around.

Printer of the year was the HP LaserJet Plus. The LaserJet has done me yeoman service; it has printed thousands and thousands of pages quickly and efficiently and has never failed me; and the upgrade to the Plus was a significant improvement.

Last year I invited my readers to nominate products for best of the year. Significant nominees were Cheetah's Expanded/Extended Memory Board for the AT, Microsoft Windows, Borland's Turbo Prolog, and all the companies who dropped copy protection. On sheer volume, Turbo Prolog wins hands down; I don't think I ever got as many rave letters for anything else. People who like that one like it a lot.

On the other hand, the trend to abandon copy protection is very significant. You may recall that last year the Folly award went to Microsoft because of a glitch on a copy-protection scheme; this year they abandoned copy protection forever and ought to be congratulated for it. So should Ashton-Tate.

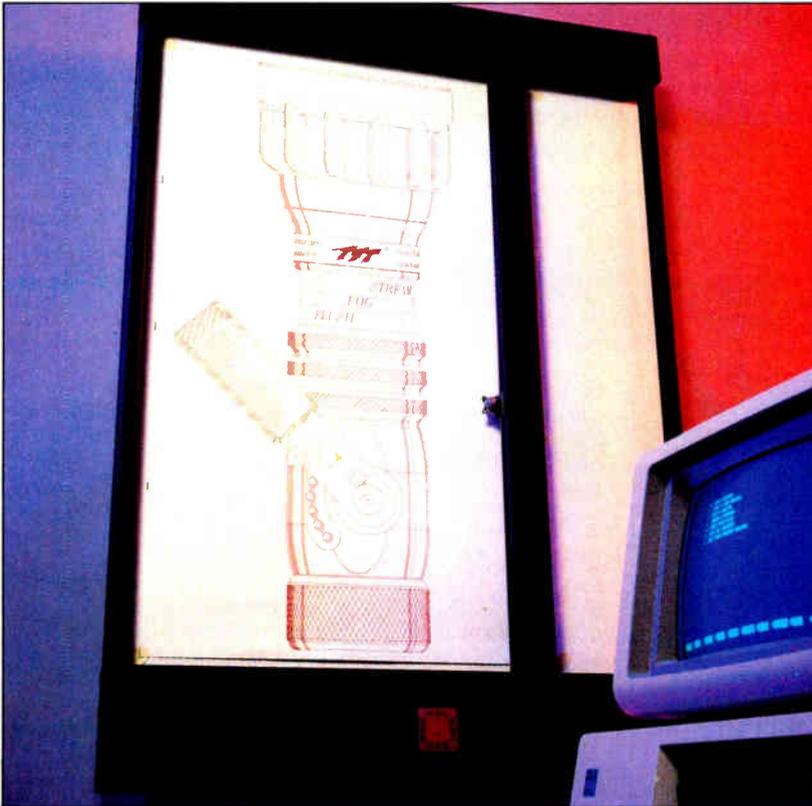
Winding Down

It is now nearly dawn. This column is due, and in about two hours I am supposed to catch an airplane to Las Vegas for the Consumer Electronics Show. I've never been to a CES before, but I've had a preview of some spectacular announcements by Atari and have heard rumors about improvements to the Amiga. There are also supposed to be developments in the CD-ROM field. Since I've always been gadget-happy, this seems like a good year to go see what's happening.

Meanwhile, AT&T keeps talking about sending me color and a larger hard disk for the 6300 Plus, which I still suspect is one of the best machines to come out last year.

Last year wasn't terribly exciting, but it did see a new surge in the microcomputer industry. Let's hope 1987 is even better. ■

Jerry Pournelle welcomes readers' comments and opinions. Send a self-addressed, stamped envelope to Jerry Pournelle, c/o BYTE, One Phoenix Mill Lane, Peterborough, NH 03458. Please put your address on the letter as well as on the envelope. Due to the high volume of letters, Jerry cannot guarantee a personal reply.



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A Head Full of Cotton

Bruce Webster

*Bruce battles
the flu while looking at a surprise
Christmas present*

A new year has started, ushered in by a recurring bout with the latest strain of flu going around. It has left me feeling as though I'm trying to think with a head full of cotton—a condition some friends would argue was normal. The new year has also come accompanied by about 6 inches of snow, a relief to the desperate ski resorts and skiers around the state, but a bit of a disappointment to us regular denizens who were enjoying the clear, dry winter we'd been having so far.

Magic Sac

A package came via Federal Express a few days back. When my son Aaron brought it downstairs to my office, the airbill was missing, so I don't know where it came from. Inside was a set of Mac ROMs (labeled originals, not copies), a Magic Sac package, and a typewritten letter that read:

From: Santa

Ho! Ho! Ho! Your Christmas wish has reached me, and since you've been good this year, the elves and I decided to send you a Magic Sac. Next year, we'll go for a Compaq 386.

Ho! Ho!
Santa.

This is not a cutesy introduction; that letter was actually inside the package, and the airbill was really missing. Anyway, having written about the Magic Sac since I first saw it at the West Coast Computer Faire early in 1986, I was excited to have one of my own to play with.

The package I got contained the new version of Magic Sac, which includes a battery-backed clock/calendar that supports both Magic Sac and TOS (regular Atari) operations. It came with the cartridge itself (2 inches wide by 1 inch high, sticks out about 3½ inches when connected to the ST), an ST-formatted disk with various programs, a Mac-formatted disk with a transfer program, and a cable with a DB-25 connector for the ST modem port and a DB-9 connector for the Mac modem port. As mentioned, you have to supply your own Mac ROMs; only the 64K-byte ones will work, and they must be originals. According to the documentation, the Magic Sac can detect copied ROMs and won't function with them.

Installation was quick, easy, and relatively idiotproof. The manual had extremely detailed instructions on installing the ROMs, inserting the cartridge (which goes into the largely unused cartridge port on the left side of the ST), and booting up the software. I used the MFORMAT program to format some blank 3½-inch disks into what the manual calls "MAGIC format" (400K bytes only).

Since the Atari drives can't currently read Mac-formatted

disks, I had to drag the Mac Plus over by the Atari and use the transfer cable (provided with the Magic Sac). I then ran MRECEIVE on the ST and TRANSFER on the Mac to copy software over. This copies

the disk in the internal drive of the Mac to the MAGIC format disk in drive A of the ST. We're talking slow here, folks: about 12 minutes to do one disk.

Using Magic Sac is almost like using a Mac. The left button on the ST mouse functions as the Mac's mouse button; the other is ignored. The screen is larger, both in real terms and in pixels (640 wide by 400 high, as compared to 512 by 342 on the Mac), and properly written Mac applications can use the extra screen space. The Ctrl key on the ST keyboard is used in place of the Mac's Command key.

There are some work-arounds and rough spots. Since the Mac uses automatic disk eject and the ST uses manual, you must use the Mac method first (click on disk, then select the Eject command or type Ctrl-E), then wait for the letter of the drive (A or B) to flash on the menu bar before manually ejecting the disk. Also, some of the small system fonts (like that used to label icons) aren't as readable on the ST as they are on the Mac.

After I was done, I ran a benchmark program—the same object code I used on the Mac Plus—to see what the results would be. Table 1 tells the story. The Atari ST had a definite edge on performance benchmarks, but the ROM differences between the original 64K-byte ROMs and the current 128K-byte ROMs showed up in just about everything else. The disk I/O benchmarks were drastically different, I suspect because the Magic Sac is working with the worst of both worlds: the old 64K-byte ROMs and System and Finder, and the Atari ST disk drives. (Looking back through my files, I notice that the times are slower than similar benchmarks run on a 512K-byte Mac with the old ROMs.)

You may think this is an unfair comparison, but Apple has been shipping only 128K-byte ROM machines (the Mac Plus and the Mac 512K-E) for quite a few months now; between those and the upgrades, 64K-byte ROM machines are a dying breed. The upshot is that processor-bound applications will run faster on the Magic Sac, whereas, I/O-bound applications—those doing a lot of graphics and/or disk access—will run faster on the Mac Plus and the Mac 512K-E.

By the way, a minor bug surfaced during the benchmarks. The benchmark program I used is self-timing via calls to the

continued

Bruce Webster, a consulting editor for BYTE, can be reached c/o BYTE, P.O. Box 1910, Orem, UT 84057, or on BIX as bwester.

function TickCount, which returns the number of ticks (sixtieths of a second) that have elapsed since the system was last booted. *Inside Macintosh* warns that this function may be off by a few ticks, but since I time only to 1/10 second, that gives me a slop of ± 3 ticks. However, on the Atari ST, I found that the times reported by the program were significantly longer than the actual time elapsed, by a consistent factor of roughly 1.2. This forced me to go back and retime everything with a stopwatch. Be aware of this if you're writing your own programs for the Magic Sac that use TickCount.

Just after I had everything up and running, my wife Sandra walked into the office. After she had talked to me for a minute or so, I pointed to the ST's screen (which, of course, had the Mac desktop on it) and asked her if she noticed anything interesting. She shook her head and said no. I asked her to look again, and she said it looked just like the other Macintosh. I then pointed out which computer I was using. She did a classic double take and said, "How'd you do that?" (In her defense, I must point out that she also is suffering from the flu.) I explained what the product was, and she replied, "I bet the people at Apple aren't very happy about this."

Ah, there's the rub. While I doubt that John Sculley is losing any sleep over the Magic Sac, Data Pacific has still had to tread carefully to avoid legal action by Apple. The name was changed from MacCartridge to Magic Sac (the software and hardware come inside a stapled brown-paper lunch sack; Dave Small says it's in memory of the surprise packages you once could get at toy stores and carnivals). The manual describes in great detail and with many warnings how to remove the ROMs from your Macintosh, giving no indication of the possibility of getting ROMs any other way. The license agreement states that "... the use of the Magic Sac currently requires the use of software which is the property of others, including Apple Computer, Inc." and that use of it "... will require you to procure the right to use such software from Apple and/or other authorized parties." Betcha the lawyers had fun coming up with the wording on that one. I can just see some end user calling up Apple's legal department and asking for permission to use the Finder and System files on an Atari ST.

This raises an interesting issue: Am I legally limited to using the Finder and System files on a Macintosh? Almost every major Macintosh software package available bundles it with the

Finder and System files, yet a check of several licensing agreements mentioned no limitations as to being able to use that software only on the Macintosh. The same licensing agreements let me make working copies of the master disks (and the manuals usually encourage it). If I have an ST with a Magic Sac and I borrow a friend's Macintosh to transfer over Mac software that I have purchased, all I've done is made working copies, right? I've paid for the software, and I haven't violated any licensing agreements or copyright laws, so is there a problem?

Given the current limitations of the Magic Sac, I don't see it as a major threat to Apple. Software transfer is clumsy, time-consuming, and requires a Macintosh. Data interchange with Macintoshes (except via bulletin boards) is likewise awkward. The current version supports only 400K-byte disks, even if you have double-sided drives. Sound is not supported; but then again, the same is true for owners of Lisas (er, Mac XLs). Hard disk drives are likewise not supported, nor is version 5.0 (or later) of the Finder. Because of the disk transfer process, you can't run copy-protected software. The current version supports only the Atari hi-res monochrome monitor, though late word from Data Pacific indicates that color support has been implemented in-house.

However, many of those limitations may change. The manual hints at future support of the 128K-byte ROM, which would boost performance. This would also lead to support of later versions of the Finder. Likewise, the manual predicts support of 800K-byte floppy disks as well as ST-compatible hard disks. Most important, they mention a forthcoming hardware product that will allow Atari ST disk drives to directly read disks in Macintosh format. That will eliminate the major bottleneck and let users run Mac software without access to a Mac.

In my January column, I gave the Magic Sac an award as the Best Hack of 1986. My opinion hasn't changed at all. And given the large amount of public domain Mac software, you could get by with few purchases of Mac software (you'd need at least one, to get the System and Finder files). At \$149 for the Magic Sac, you can have your ST and Mac it, too.

PAL Expansion Chassis

The Amiga—unlike the original Mac or Atari ST—was designed and built with an open architecture in the form of an expansion bus coming out one side of the computer. Commodore was counting on third-party developers to produce the hardware that would make use of that bus. Unfortunately for Commodore, that hardware was slow in coming, and many of the early products were unreliable or emitted RF signals at levels the FCC found unacceptable. Furthermore, the developers had problems dealing with the bus signals, problems passing them through, problems with power, and problems keeping the cost down (because of all the other problems). All this has served to underscore the lesson that everyone should have learned from the Apple II and the IBM PC: The best open architecture is based on internal slots. Apple, Atari, and Commodore all seem to have now learned that lesson, since official statements and unofficial rumors indicate that the next generation of Macs, STs, and Amigas will have internal slots. So where does that leave those of us with the earlier machines?

Well, those of us with Amigas can look at the PAL expansion chassis, available from Byte-by-Byte at a base price of \$1795. The PAL is about 6 inches high and sits on top of the Amiga, having exactly the same footprint. It connects with the expansion bus through a hardware device called the "staple," a small, thin box (about the size of the Alegria memory box) that plugs into both the Amiga's expansion bus and the PAL's connecting bus. Your monitor then sits on top of the PAL, some 6 inches higher than it was before. I didn't find this bothersome at all—in

continued

Table 1: Benchmarks from the same program run on the Macintosh Plus and on the Atari 1040ST with a Magic Sac. All times are in seconds.

	Mac Plus	Atari ST
Performance:		
sieve	5.9	4.2
matrix mult	6.6	5.6
sort	10.5	7.9
Graphics:		
vertical lines		
offset = 0	12.9	13.1
offset = 1	87.1	174.0
offset = 20	87.1	174.1
offset = 100	86.7	174.4
circles	9.4	17.2
rectangles	17.8	21.8
Input/Output:		
disk write	14.1	56.3
disk read	9.5	12.6
random read	35.7	92.6

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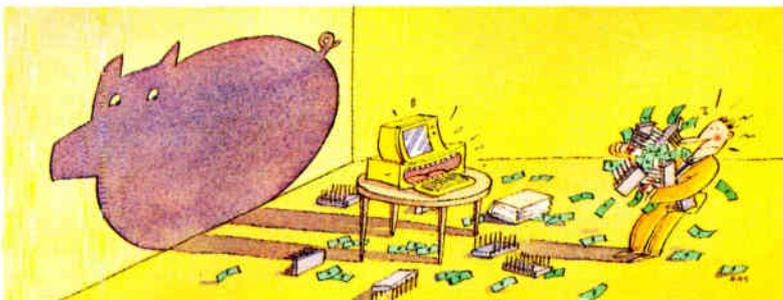
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fact, it cured my tendency to hunch over the computer—but it might be troublesome to hunt-and-peck typists who have to continually look back and forth between monitor and keyboard.

Inside, the PAL has a heavy-duty power supply, a cooling fan, a battery-backed clock/calendar, and 1 megabyte of RAM. The RAM is located in a section of the Amiga memory map that was originally reserved by Commodore for future use, then was “unreserved.” This means that you can still add another 8 megabytes of RAM with expansion cards. Also, the PAL boot disk loads into that memory portions of the operating system that would normally be in “chip RAM,” the lower 512K-byte area where all graphics images must reside. This, of course, frees up that memory for graphics data.

For those expansion cards, the PAL has five “Zorro-standard” 100-pin expansion slots. Byte-by-Byte sells a RAM card capable of holding 2 megabytes for \$1195. Other manufacturers are also producing Zorro-compatible cards, though many have complained that Commodore may be changing the standard for future Amiga machines. One nice touch is that the cards can be added or removed without opening up the PAL itself. Instead, the back of the PAL has five small, removable covers—one for each slot. You remove the cover, insert or extract the card, then replace the cover.

The PAL also has room for three half-height mass storage devices, like hard disks. You do, of course, have to open up the PAL to install the device and connect it with its controller card. Byte-by-Byte offers the PAL with either a 20-megabyte hard disk (\$3195) or a 40-megabyte hard disk (\$3995). Byte-by-Byte is also looking at a future potential for CD-ROM devices in those locations.

The PAL I received—for just two weeks (sigh)—came with a 40-megabyte hard disk and a 2-megabyte memory card; list price would have been \$5190. Setup took only a few minutes: Move the monitor off the top of the Amiga; remove the StarBoard II and Alegria memory cards from the expansion bus; put the PAL on top of the Amiga; connect it to the expansion bus with the staple; put the monitor on the PAL; plug the PAL into an outlet; power it up; boot up the Amiga. The PAL came with its own Kickstart and Workbench disks (both version 1.2); the start-up sequence created a Workbench RAM disk.

The PAL’s hard disk, like any other, works faster than floppy disks but slower than a RAM disk, as the benchmarks in table 2 illustrate. As you can see, for most operations the hard disk is only two to three times faster than the floppies. This is due more to performance problems with AmigaDOS than anything else and is not an accurate reflection of the speed of the hardware itself.

Some notes on the benchmarks themselves are in order. The first disk benchmark was a Lattice C routine that repeated the following steps five times: Open a file for output; write out 256 512-byte buffers; close the file; open the same file for input; read in 256 512-byte buffers; close the file. The second routine wrote out 1024 512-byte buffers; the timing did not include either opening or closing the file. The third routine was similar. (Source to all three routines can be found in the ask.webster/benchmarks topic on BIX.)

The application benchmarks were done under the CLI, using Superbase, a new database program for the Amiga. The picture file was loaded from within Superbase. The first copy benchmark was done from df0: to the indicated device (RAM disk, hard disk, floppy disk); the second was done from the device itself to a subdirectory on that same device.

A note on the Lattice C compilation benchmarks: The Lattice C manual recommends that you not assign the logical device QUAD: to the same physical device where your source files are located. However, since I did exactly that for the initial RAM disk and hard disk benchmarks, I also did it for the floppy disk benchmarks. I then ran a second set (for just hard and floppy disk) with QUAD: assigned to RAM:. You can see the difference in performance, especially for the floppy-based compilation. Moral: Listen to what the manual tells you.

The only real disadvantage with the PAL is that it prevents you from using any other hardware that plugs into the expansion bus, since the PAL grabs the bus for itself and does not pass it out anywhere. However, if you don’t have an investment in expansion hardware, that’s not a problem at all.

Because of costs, the PAL is obviously not for the weak of pocketbook. It’s designed and priced for power users, and Byte-by-Byte has had success selling it into engineering and scientific environments. Also, Byte-by-Byte offers a discount to developers; contact them for more details. While I haven’t had it long enough to really wring it out, I have had absolutely no problems with it during the period it has been here, and it appears to be a solid, well-built piece of hardware. If you’re looking at significantly expanding your Amiga 1000, consider the PAL—especially if you can get someone else to foot the bill.

Product of the Month: Guide

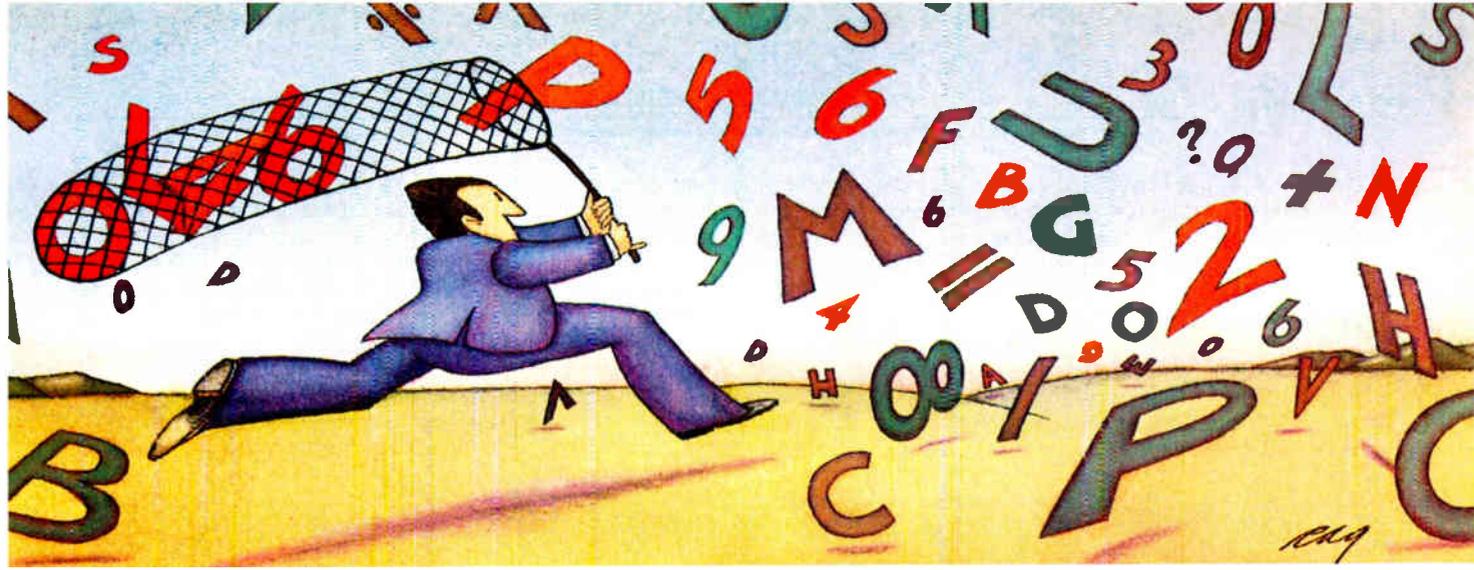
Some years back, Ted Nelson (of *Computer Lib/Dream Machine* fame) pushed the term “hypertext.” Regular text proceeds in a start-to-finish flow—essentially one-dimensional. Nelson was referring to multidimensional text, where a given chunk—a word, phrase, sentence, paragraph, page, or document—could be associated with any number of other chunks, each of which could in turn be connected with other chunks, and so on. The associations would extend between documents; browsing through this vast network of items would uncover new relationships and information. Nelson, by the way, has been working ever since then to bring a full-blown hypertext system—Project Xanadu—on-line; for more information, contact XOC Inc., P.O. Box 7213, Menlo Park, CA 94026.

Others have been intrigued by the concept of hypertext, and one company—Owl International—has brought the first hypertext processor to market in Guide. The documents produced by Guide are called Guidelines. A Guideline appears at first glance to be just a regular text file, until you find that with a push of the

continued

Table 2: Benchmarks run on an Amiga 1000 with a PAL expansion chassis connected. All times are in seconds.

	RAM disk	PAL hard disk	floppy disk
Disk benchmark (dbench)			
128K file read/write (5x)	53	110	216
512K file write (1x)	22	55	111
512K file read (1x)	21	31	63
Compile and link (Lattice C 3.10)			
dbench (90 lines)	27	47	181
with QUAD:=RAM:	—	40	104
speechtoy (1380 lines)	105	149	535
with QUAD:=RAM:	—	127	256
Compile and link (Aztec C 3.20a)			
dbench	14	23	93
speechtoy	87	108	272
Application work (all from CLI)			
load application (189K)	6	10	32
load picture (39K)	1.3	2.2	4.8
copy app from floppy	18	33	63
copy app to subdirectory	1.5	19	61



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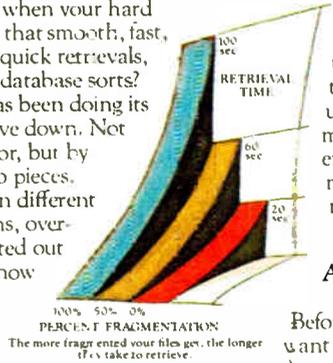
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mouse button you can expand and shrink text (and/or graphics), jump to related portions of text in that or other documents, and cause pop-up notes and pictures to appear.

The underlying concept of Guide is that of "buttons." A button is a section of text (or graphics) that is connected to some other text (or graphics). A button could be a single character, a word, a sentence, a picture—in short, any part of your document that you can select by dragging your mouse. The three types of buttons are replacements (including inquiries), references, and notes. Buttons are not visible within the text; your document looks normal. However, the aspect of the button text is changed, and when you move the cursor over a button, it (the cursor) changes shape, the new shape reflecting what type of button is beneath. If you then click the cursor, you trigger that button.

A replacement button is indicated by boldface text; when you move the cursor over it, the cursor changes to a circle with cross hairs. When you click the mouse, you replace the buttoned text (graphics, etc.) with different text, graphics, and/or buttons. A typical use is to replace a brief comment or description with longer, more detailed text. Note that you can continue to browse in the text before and after the expanded section, just as you can activate buttons elsewhere and then scroll back to this section and still see the replacement text. If you move the cursor within the replacement text and click the mouse, it (the replacement text) disappears and the original text is back in place.

An inquiry is actually a collection of replacement buttons that are mutually exclusive. In other words, an inquiry might have

four replacement buttons; if you choose any one of them, it and the other three are all replaced by that one button's replacement text.

A reference button is indicated by italicized text; the cursor changes to a fat arrow pointing to the right. When you click the mouse, the button doesn't replace or expand text. Instead, it moves you to another portion of your document or even to another document entirely. As with the replacement button, you can get back to where you came from by clicking on the reference text. Or you can click on the special backtrack icon at the top of the vertical scroll bar. Note, however, that you can back up only through 32 references, so if you've wandered too far afield, you may have to go directly back by closing and opening files.

A note button is flagged by underlined text; the cursor changes to a fat asterisk. It pops up a small chunk of text and/or graphics while you hold the button down, analogous to the ubiquitous yellow Post-it notes. Unlike the previous two buttons, the text (which is in its own window) goes away as soon as you release the mouse button.

What if you've selected a number of replacement and reference buttons, and you want to quickly back up to your original document? One command, Top Level, will take you all the way back. And while buttons are not normally visible throughout the text, you can select the Show Symbols command, which will bracket each button in the text with symbols indicating which type of button it is.

Creating a Guideline is straightforward. You enter text just as you would with a word processor. When you want to create a button, you select the text for that button with the mouse, just as you would select text to be cut or copied. You then go to the Make menu and select the appropriate command. You can open other files to grab text (or graphics) to paste in or to create reference links. You can create any number of buttons within a button, and you can nest buttons to an unlimited depth. The actual details are specific to each button but are easily learned, thanks to the manual and example files.

Speaking of which, the manual is very well done, even by Macintosh standards. The first 70 pages or so form a tutorial that does an excellent job of teaching you how to use Guide. The next 60 pages are a user's guide, and the last 60 explain each of the commands in detail. Guide comes on two disks with lots of example files and is not copy-protected.

The Guide disks include MiniGuide, a desk accessory version that lets you open and read Guidelines while within other applications. One possible use of MiniGuide is to create custom help files for certain applications to allow on-line help for those less familiar with how to use those programs. Also included is a Calendar Kit. This contains a template of a single month, where each date is a reference button. By clicking on a given date, you go to an appointment calendar for that specific day. By copying this file and then changing it to a specific month, you can create your own appointment book.

How useful do I think Guide is? It's hard to say because I am so used to thinking in a linear paper-and-pencil format, and I'm not yet skilled at creating and using Guidelines. The feeling, though, reminds me of when I first learned Pascal, some seven years ago. Prior to that time, I had done most of my high-level coding in FORTRAN, which has just one real data structure: the array. In FORTRAN, you build everything out of arrays, and I had gotten very good at doing just that. Now I was confronted with the freedom to define my own data structures: arrays, records, sets, enumerated data types, subranges, strings, and so on. I felt unsure of myself, and it took me some months to become confident of my own ability to create the right data structures. Now—some 100,000 lines of Pascal later—I take that as a

continued

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Guide \$134.95
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 Glen Ellyn, IL 60138
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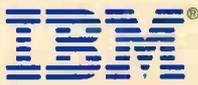
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ACCORDING TO WEBSTER

Guide proves the contention that the best software being developed is on the Macintosh.

matter of course; were I to go back to FORTRAN, I'd probably feel terribly constrained. I suspect that if I use Guide long enough, the same thing may happen: Word and outline processors will feel limited.

Guide easily earns its award as product of the month on three different counts: innovative application, excellent software (I have yet to run across a single bug), and high-quality documentation. It is proof of the contention made by my friend Frank Boosman that the best, most innovative software being developed today is being done on the Macintosh.

Notes and Updates

Batteries Included has released a new version of Tom Hudson's excellent paint program DEGAS, called DEGAS Elite. Like its predecessor, DEGAS Elite runs on the Atari ST with either a color or monochrome monitor. Unlike its predecessor, it allows you to have multiple pictures open simultaneously; lets you draw basic shapes (circle, line, etc.) by setting two points; does scaling, flipping, rotating, and 10 levels of magnification; and has lots of other nifty new things. Best of all, it's only \$79.95. If that's too rich for your pocketbook, you can buy the original DEGAS for \$39.95. And, of course, neither is copy-protected. If you own an Atari ST, you should own either DEGAS or DEGAS Elite—it's that simple.

Lattice has also released version 3.10 of their C compiler for the Amiga. Improvements include rewritten documentation, elimination of numerous bugs, support for version 1.2 of the Amiga system software, and substitution of BLINK for ALINK. ALINK is the original Amiga linker and is notorious for being both big and slow. BLINK, developed by the folks at The Software Distillery, is a great improvement. Also, the Lattice Text Management Utilities are now bundled in. The result of all these improvements is that I have now switched back to Lattice C for my Amiga development, mostly because I find it easier to get my applications up and running using it. Off the shelf, it costs \$225. There is also a Professional Package that includes all of the above plus the Lattice Screen Editor, Make Utilities, and (best of all) the Metascope Debugger for \$375—a good deal.

The Hackers Corner

BLINK, mentioned previously, is a public domain linker for the Amiga developed by a group of Amiga hackers known collectively as The Software Distillery (235 Trillingham Lane, Cary, NC 27511, (919) 469-4210). Said programmers have developed several other programs for the Amiga, including POPCLI, a utility that lets you bring up a new CLI window from within any application and blanks your screen after a certain amount of time elapses with no user input. They have also produced HACK, a graphics version of the old UN*X dungeon game. All of these are public domain and can be downloaded from The Software Distillery BBS, which is at (919) 471-6436. If you don't have a modem, they can send you the software on a disk; write or call to find out what the current costs are.

In the Queue

Next month will include a report on the MacWorld Exposition, a look at the Radius FPD (Full Page Display) for the Mac, and the usual odds and ends. Until then, I'll see you on the bit stream. ■

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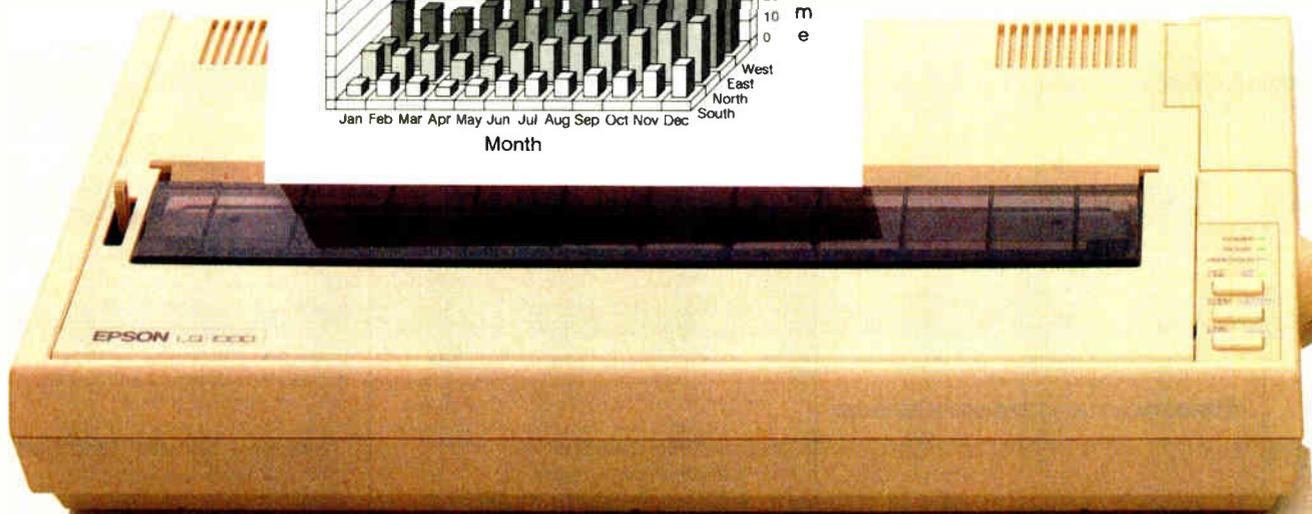
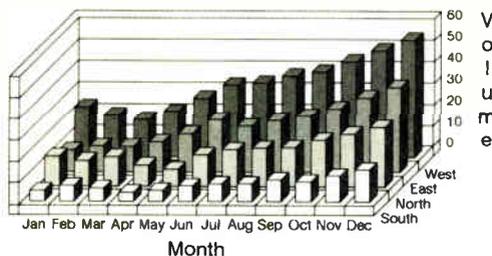
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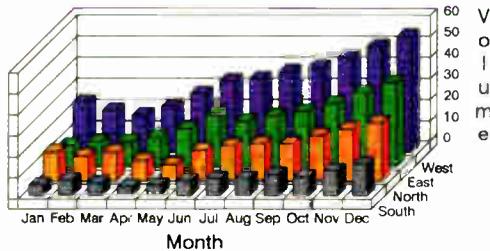
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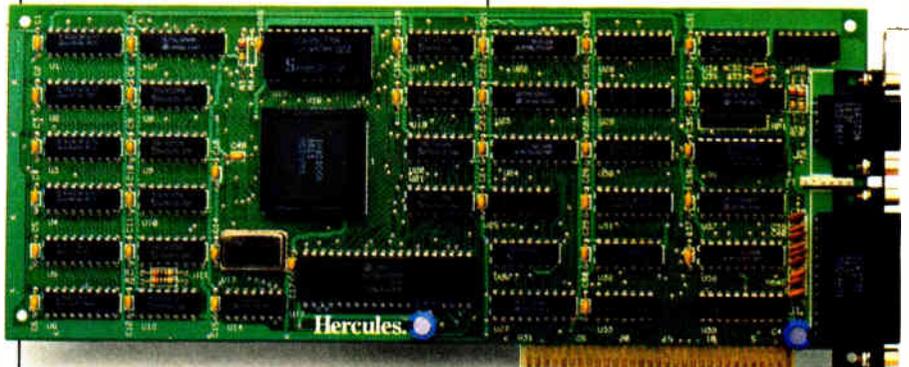
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Another Odd Lot

Ezra Shapiro

Try as I might, I can come up with no unifying theme for this month's selection of products; there's just no category that covers them other than "miscellaneous software." There's an innovative text system for the Macintosh, two unusual integrated packages for MS-DOS, and a free-form database program (also for MS-DOS). These programs are not traditional, however; there's something unique about each of them—perhaps that's the theme.

Beyond Word Processing

It's tougher to describe **Guide** (Owl International, \$134.95) than it is to use it. The program is a text-creation tool, but that doesn't mean it's a word processor. Billed as the first "hypertext" system for the Macintosh, **Guide** is intended to free the writer from the mental restrictions imposed by working on paper or with software that merely duplicates paper. The theory is to tap the power of the computer screen as a primary output device. **Guide** lets you develop complex, layered documents that display information as a series of visual explosions. My gut reaction is that this is an important program, one that will influence software design for years to come.

The heart of **Guide** is a simple text editor. You start by entering data as you would with any ordinary word processor. However, **Guide** is relatively limited if all you want to do is generate flat text files; its real strength lies in the way it allows you to build layers upon layers. You can define any area in a document as a **Guide** "button." Clicking the mouse on a button opens a hidden layer of text or graphics.

Guide has several types of buttons. The first replaces a section of a screen with something else. You can use this feature to substitute common language for a technical expression, expand an acronym to a full-length phrase, or even replace a single word with an entire screen full of data. The cursor normally appears as an I beam. When you slide it over a replace-

Consisting of the following items: *Guide, IS-2000, A-Plus, and askSam*

ment button, it changes shape to a cross-hair target. Clicking the mouse makes the substitution. When you're over the replacement, the cursor turns into a hollow box; clicking reverts to the original. Replacement buttons can be grouped into an "inquiry"—a series of buttons arranged into a menu.

The second type of button jumps you to a reference point somewhere else in your document or to an entirely different document. As an example, you could create a file that is nothing but an index; clicking the mouse on any line would send you off to the appropriate material, wherever it might be. To get back to your starting point, you'd click a special box at the top of the right-hand scroll bar.

The third type is called a "reference" button. When it's over the button region, the cursor changes into an asterisk. Holding down the mouse button opens a window containing additional data; the window vanishes when you release the mouse button (perfect for footnotes).

Creating a file is a piece of cake. When you want to include a button, you merely make a selection from a pull-down menu. The operation is roughly equivalent to switching from plain text to boldface and back. Editing an existing file is slightly trickier, but it is not difficult; you have to deactivate the buttons with a "freeze" command before you can rework your document.

That's all there is to it, really, with two minor notes. Buttons can be regions of text or imported graphics (either MacPaint or MacDraw), and buttons can be nested for as much depth as you want. Imagine, if you will, a sales report that jumps to a bar graph of sales by region, then each bar of the graph jumps to a pie chart of sales by state, and so on.

On the practical side, I found the program confusing at first, though I admit I tried to run it without reading the documentation beforehand. All of Owl's literature brags about how easy it is to use **Guide**, so I thought I'd take a stab at it. Mistake. I simply couldn't figure out what the menu items were supposed to accomplish. However, after loading the tutorial files—still without cracking the manual—it took me only about five minutes to grasp the operation of the program. So yes, it's easy after you get the point, but those opening moments of panic could have been avoided with more obvious menu entries or a built-in help command. The on-line help system is a collection of **Guide** documents that must be opened and read; there's no sensitivity to context. It works (in fact, all the help and tutorial documents are excellent), but the software could be improved with something as simple as a help command that merely gives you a message that says, "Load the help file, you dummy."

Once I got rolling with **Guide**, I had no problems that I could identify as resulting from glitches in the program, but it did seem rather too easy to get lost. Clicking in the scroll bar, or in an empty spot on the screen, would occasionally drop me into uncharted regions of a document. It was never difficult to get back to where I was supposed to be, but I was never sure whether I was dealing with bugs or features. The bottom line on this part of my experience is that **Guide** documents have to be designed very carefully to avoid dismaying the casual reader.

Guide is put together well. Documentation is clear and precise, and the disk tutorials are thorough to the point of ex-

continued

Ezra Shapiro is a consulting editor for BYTE. Contact him at P.O. Box 170040, San Francisco, CA 94117. Because of the volume of mail he receives, Ezra, regretfully, cannot respond to each inquiry.

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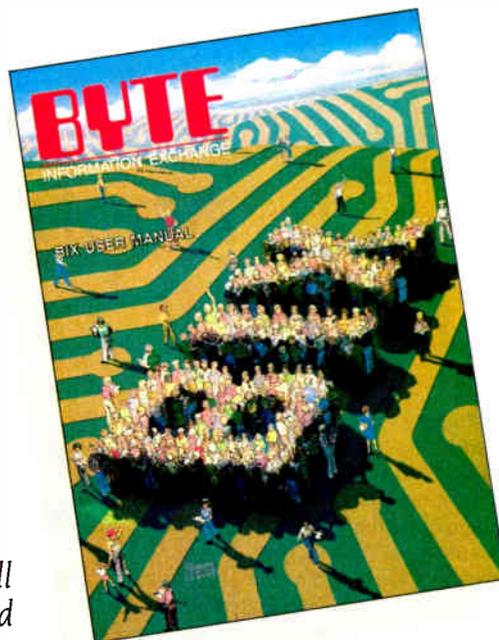
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cess; if you cruise through a few files, you'll be up and running in no time.

Guide has limited hard-copy output capabilities, but it does export files in a couple of formats so you can massage them with your favorite word processor or page layout program. Even so, I wouldn't recommend the program to anyone who has to print on paper. Guide is much stronger for on-screen presentations; the manufacturer suggests electronic mail, training materials, and software tutorials.

Two ancillary products are important to note. When you purchase Guide, you also receive a MiniGuide desk accessory that lets you read Guide files from within other applications. This strengthens the case for using Guide as a reference engine or as a tool for building help files or tutorials for other programs.

You can also buy a separate package, the Guide Envelope, for \$199.95. The Envelope creates read-only Guide documents so you can send your output to readers who don't own the Guide software itself. Owl International distributes many of its press releases this way.

On the whole, I'm enthusiastic about Guide, but I'm not sure I'd want to use it on a regular basis. It's great for communicating with others, but I doubt it's an effective product for an isolated individual. While I often scrawl little notes to myself, I don't build elaborate tutorial systems for my own use. I'm better off with an outliner or with notepad-style desk accessories.

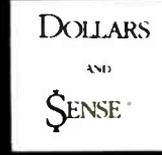
Speculating wildly for a moment, my analysis of Guide as an application software package may be missing the point of this exercise. The marketing crew is a savvy bunch, and the program itself hails originally from the University of Edinburgh, that hotbed of artificial intelligence research. These are smart people who look to the future. I could easily see Guide as the precursor of a CD-ROM operating system; the unobtrusive layering of Guide's structural hierarchy would be an ideal mechanism for plowing through a massive text database. We'll just have to wait and see, won't we?

Old Friend

I first met a unique software package called Intuit more than three years ago. At that time, it was the slickest and most fluid example of integration I had seen, but it was application and operating system rolled into one. You plugged in your Intuit disk and waved good-bye to MS-DOS. When the program came to market shortly thereafter, the author had included a separate utility to read and write DOS disks, but it wasn't enough to satisfy

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users who didn't want to have to switch operating systems. On a floppy-disk-only machine, Intuit was okay, but it was a real pain on a hard disk system.

Well, I'm pleased to report that Intuit is back as IS-2000 (Noumenon, \$39.95), only this version will run—meekly—as a DOS program if you want. You don't have to kiss off your favorite memory-resident goodies, and hard disk use is no problem. I have no idea why the name was changed from a good moniker to something that sounds like a piece of construction machinery, but whatever it's called, this program is worth the investment of 40 bucks, even if you use it only to squander a pleasant rainy afternoon.

It's a tidy little business-oriented package. The main elements are word processor, spreadsheet, and database. The word processor is old-fashioned by today's standards (largely because it's not pure "what you see is what you get"), but it's certainly adequate. The spreadsheet is excellent, and it was the first I'd seen to allow computations based on English-language row and column names. The database is ideal for mailing-list management and features a straightforward query system.

Two tricks are worth mentioning. First, it's possible to "tilt" the spreadsheet 90 degrees (swapping rows with columns); this makes writing labels for columns much easier. Second, once you've created a database and a matrix document for mail merge, you can view individual records in position in the matrix and edit them there, rather than having to switch back to the database view.

All the documents you create are stored in one huge IS-2000 file (though you can import and export ASCII). This frees you from the limitations of 11-character filenames (IS-2000 allows 67 characters), and because all data is stored as variable-length records, you'll chew up less disk space than with other programs.

It's only fair to point out that IS-2000 is a world unto itself. It might take some time adjusting to IS-2000's nomenclature and command structure. The documentation is a real help, as are the on-line explanations, but there's something about the unusual directory format and operating style of the program that's a little brain-bending.

However, this is the only \$39.95 product out there that's complete enough to run a small business, and for that reason alone I recommend it. IS-2000 is one of the best bargains in the industry.

Good Grades

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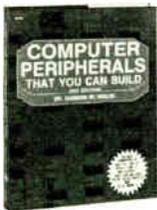
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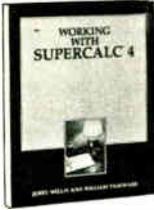
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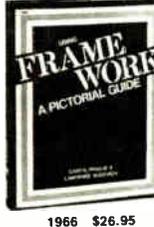
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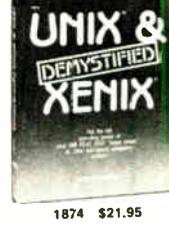
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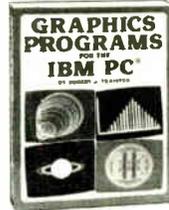
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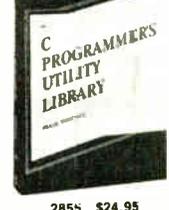
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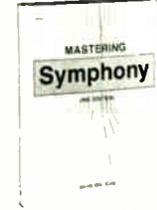
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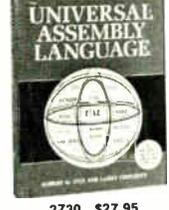
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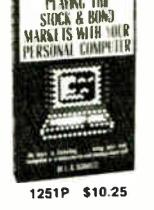
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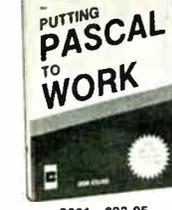
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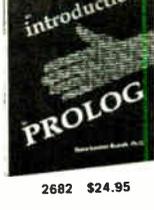
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rectory structures. Next you had to cope with the desktop metaphor for windowing interfaces. Now it's time to brace yourself for the newest development in this evolution: the loose-leaf binder metaphor. And no, I'm not joking.

A-Plus (Savant, \$89.95) is an integrated windowing product that includes a word processor, a paint program, and a nifty little calculator. Because it was targeted initially at high school students, it uses the metaphor of a loose-leaf notebook for directory and file organization. And even though I can't resist taking potshots at it, both the metaphor and **A-Plus** itself work exceptionally well.

For basic writing and drawing tasks, **A-Plus** is more than sufficient. It's smaller, faster, and more fun to use than Microsoft Windows, and it doesn't demand a mouse. The comparison to Windows is a fair one; though **A-Plus** isn't an operating system shell, it uses icons and positionable windows in a similar fashion. Speed on an 8088-based MS-DOS system is excellent, CGA graphics are quite palatable, and cut-and-paste integration is smooth and trouble-free.

Although this is not a product for sophisticated business uses, it's fine for casual writing and painting, simple reports, and even high school homework. If you have to correspond in a foreign language, **A-Plus** lets you select the appropriate character set for French, Spanish, German, Italian, Greek, and mathematics (Isn't math a foreign language?). **A-Plus** remaps the characters from the extended IBM set to simple Alt-key sequences.

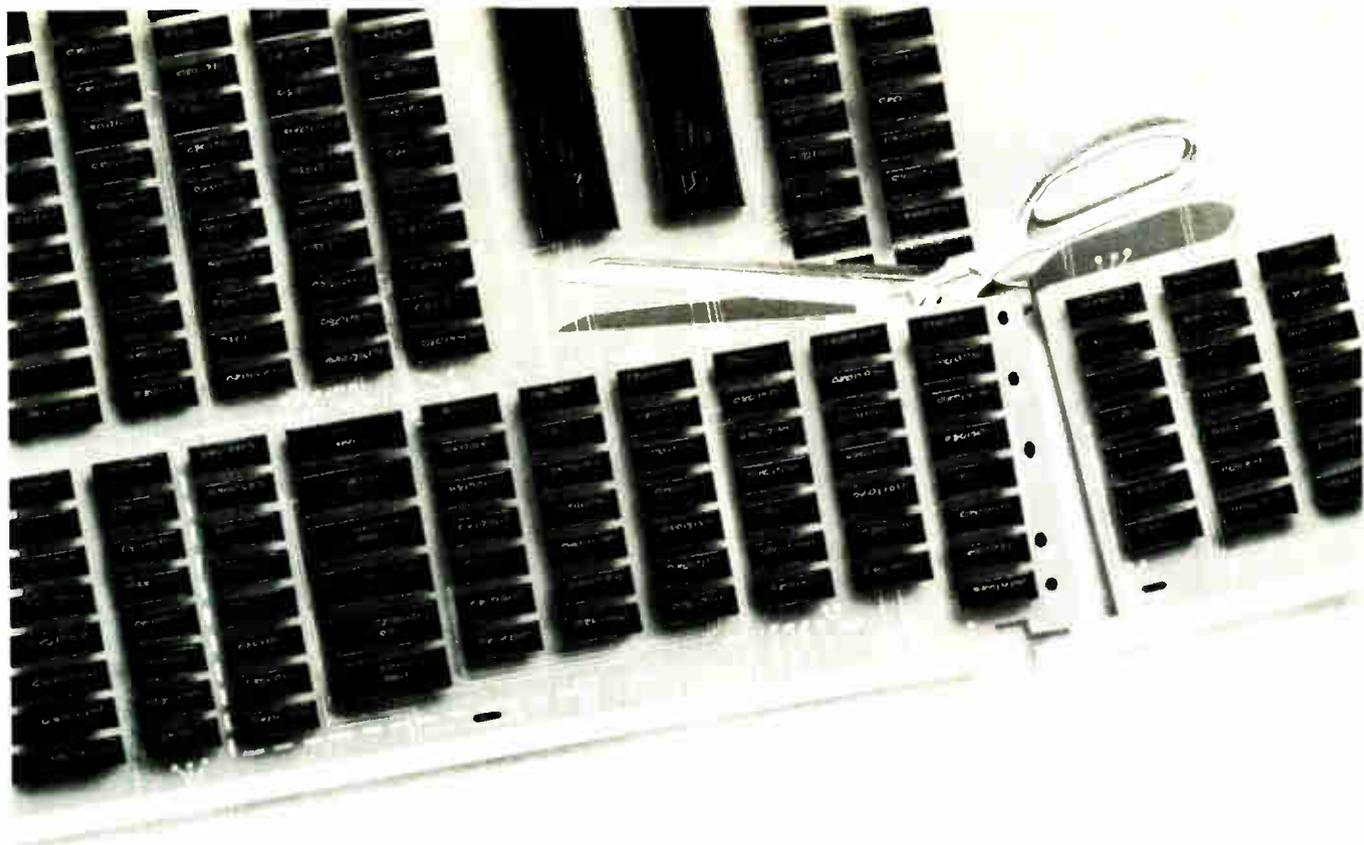
The documentation is among the best I've seen in the past year. It was written by a teacher, who has learned that students need clear writing—and that they hate a condescending tone. The manual is thorough, enjoyable to read, and doesn't make me feel like I'm either a professor of computer science or a fumble-fingered jerk. Any author of software documentation should study it closely.

If you've got a PC and a kid in the house, get the kid a copy of **A-Plus**. If you've got a PC but lack the child, buy a copy anyway and treat yourself.

Text Database

And finally, **askSam** (Seaside, \$200) is one of those obscure products that comes out of nowhere and attracts a loyal cult following of users who can make the program do incredible things. It's a free-form text-oriented database for MS-DOS that features flexible formatting, powerful query options, huge file capacity, and variable-length records for dense data packing. You can enter records as raw text, or you can define explicit field names merely through the judicious use of square brackets. It will perform calculations on numeric fields—it has a large selection of built-in functions—and on the whole, it's one of the most impressive examples of programming I've seen, combining good database management, word processing for document creation, and excellent analytical tools. If you work with large amounts of text that don't fit neatly into an orthodox database structure, or if you want to store records that bear no resemblance to each other, **askSam** is a good choice.

But like **IS-2000**, **askSam** is idiosyncratic and frequently cryptic. You can search for something like a right-justified numeric field anywhere in the database, for example, but to do so you have to master an arcane parameter syntax. I found **askSam** intriguing, but I was often flustered by it. Perhaps it tries too hard to do too many things, to be a program for every possibility you can imagine. So I give it a qualified recommendation; if you're willing to give the program enough time to get into it deeply, it's top-notch. On the other hand, if you're not willing to devote yourself to your computer with religious zeal, you might be better off looking for a program that's less flexible—but more traditional. ■



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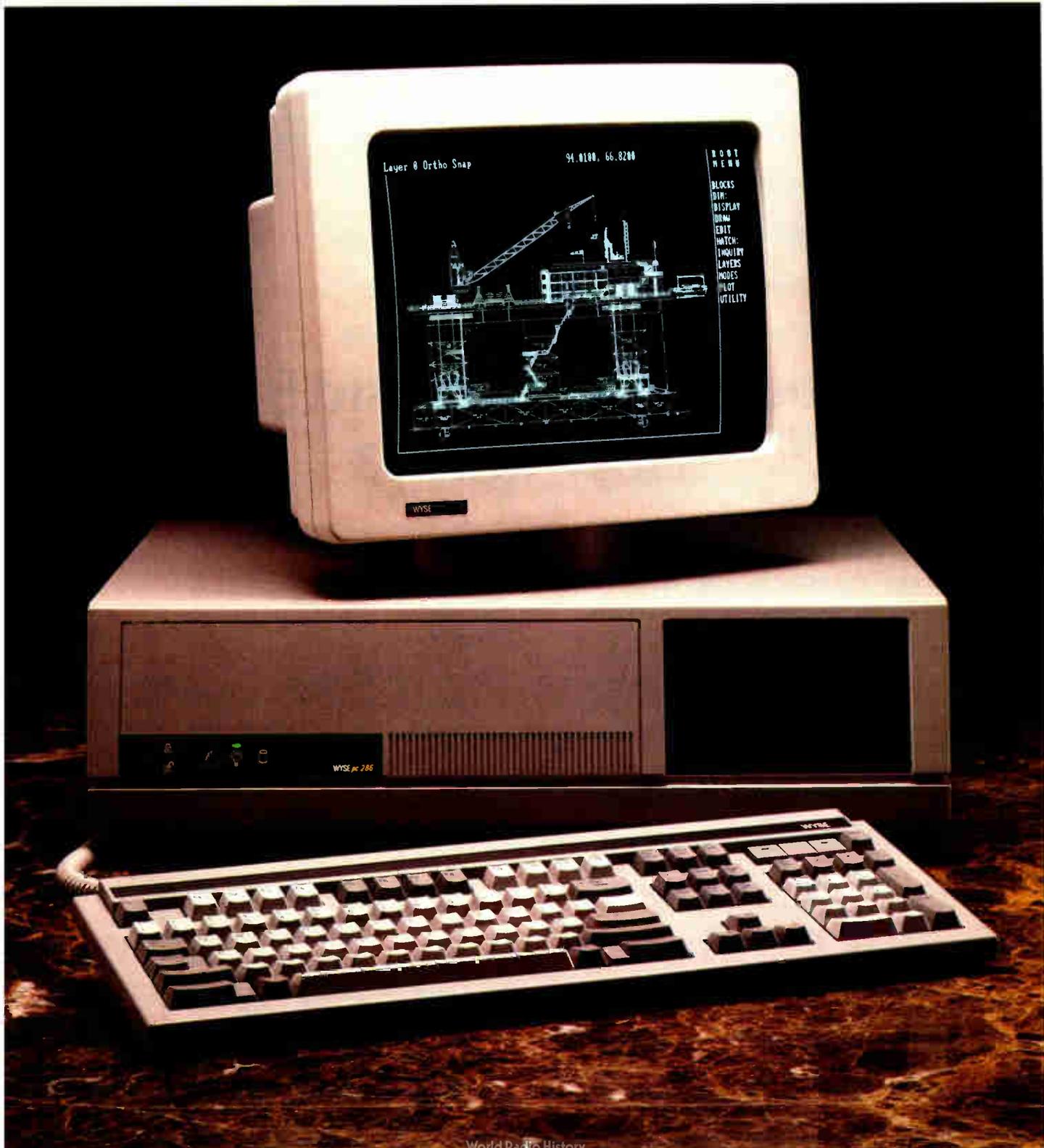
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Distinctive Coloring

Dick Pountain

Some consistency is recommended, but the choice is—or should be—yours

Color computing is definitely here to stay. A few years ago, I couldn't have made this broad statement with such certainty. The general feeling was that, while it was fun for game playing, color served no purpose for serious business users commensurate with its higher price. It increases hardware costs above those for monochrome and involves a trade-off in the quality of text reproduction: The color monitors affordable at present have a restricted bandwidth that generates characters that are not as sharp as those on a good monochrome system. The only way to sidestep this trade-off is to spend a lot of money on a fine-pitch, high-bandwidth monitor like those that are used in professional CAD/CAM systems, and they currently cost far more than the typical personal computer itself.

Nevertheless, color has caught on for the simple reason that it provides more information. When business applications were restricted to word processing and accounting, and user interfaces were text-only "glass teletypewriters," color offered little advantage. The advent of business graphics saw the first real use for color; a complex pie chart or stacked bar chart is immediately more comprehensible due to the additional dimension color supplies. The advent of windowing and resident utilities also made color desirable. Once the monitor screen ceases to be a single work area and becomes a "desktop" on which many different activities can simultaneously take place, the extra discrimination provided by properly used color is welcome indeed.

I have no hard information on what percentage of serious IBM PC users purchase color monitors, but the explosive sales growth of EGA cards for the PC suggests it is substantial; Apple IIx, Amiga, and Atari ST users have the color option, too.

To add significantly to visual information, color needs to be used intelligently; much current software doesn't do this.

Still, you can do a lot to arrive at an ergonomically sound and effective use of color. This is the subject to which I am devoting this month's column.

The Ergonomics of Color

When I purchased my IBM PC two years ago, I had a difficult time deciding whether or not to buy a color monitor. I had been using a monochrome monitor at work and wasn't sure if I could live with the fuzzy characters produced by a CGA monitor, as most of my work is writing. When the time came, however, the fact that I review software more or less forced me to purchase color.

Having thus decided, I had to optimize the display as much as possible. My first shock came when I discovered how little control PC-DOS gives you over the display colors; manipulating ANSI escape sequences is a total pain, and even then you can't change the border color. The *scrattr* program in Norton Utilities solved that problem. Then I experimented for several months with different color schemes, trying each one for at least a week to see if I could live with it. When I found the scheme that worked for me, I began the task of making my most-used application programs fit into the scheme. More on that later.

Color is, of course, partly a subjective matter; people have their own preferences, and it would be foolish to attempt to dictate. Nevertheless, I found that some factors have an objective basis. In particular, questions of perceived sharpness, contrast, and saturation profoundly affect the usability of the computer for long periods. These are largely physical factors that are tied to the actual hardware you are using; they vary from one computer and monitor to another and must be

determined by experiment. Other factors belong to the realm of cognitive psychology; for instance, how you can best use colors to discriminate and inform. These factors are largely independent of the hardware, and you can analyze them in a semiscientific way and prescribe rules that will work for all systems.

The physical factors arise from the actual phosphors employed, the scanning rate of the CRT tube, and so on. On an IBM PC with a CGA card and an IBM color monitor, I found that certain combinations of colors are unusably fuzzy because "fringing" occurs around the edges of the characters. Green or cyan on brown and brown on green are particularly bad. In general, the best sharpness occurred with black characters on light-colored backgrounds.

Other combinations offer so little contrast as to be illegible, for example, dark red or white on brown and black on blue. The best contrast occurred, as you might expect, with black on light colors or bright white or cyan on dark colors. I was already convinced of the desirability of dark text on a light background because the CP/M machine I used for several years was one of the rare few that allowed you to reverse the screen; bright text on a black background reminds me of reading neon signs through a car window on a dark night.

The final physical factor is saturation of hue. Some combinations offer adequate sharpness and contrast but are extremely fatiguing to the eyes over a long period. On the sharpness and contrast criteria, I decided that black on white, black on cyan, black on brown (i.e., dark yellow), and black on green were my favored com-

continued

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You can categorize software displays in two ways that seem relevant to the color question: by the screen area and by cognitive functions.

binations. Many people like white or cyan on dark blue. However, black on cyan and black on green proved to be tiring after a short time; the green background is particularly lurid on the IBM PC. I eventually found that black on brown was the least fatiguing for me in the long term; this neatly confirms the findings of those Swedish ergonomists who proposed black-and-amber monitors some years ago. The other combinations I ranked are as follows: Black on white is better than black on cyan, which in turn is better than black on green.

I must stress that these judgments apply only to my hardware and my preferences; I suggest that you perform the same exercise on your equipment. The results may vary. For example, when I repeated the exercise on the Apricot Xen-i with an EGA monitor, the results were different; black on white was the clear winner, followed by black on cyan.

Having selected this ranked set of preferred combinations on purely physical grounds, I began to consider the cognitive factors, trying to devise a systematic approach to software coloring.

Three Simple Rules

You can categorize software displays in two ways that seem relevant to the color question: by the screen area itself and by cognitive functions.

First, consider the actual screen area. When you are using multiwindow displays, either from resident programs like SideKick or as an intrinsic part of the operating system as on the Amiga, the screen is naturally divided into different functional areas. With ordinary full-screen software, you can also have status

lines and other special parts of the screen. I propose to distinguish two categories: *area*, a part of the screen that forms a unit like a pop-up window or a status line, and *line*, an individual line of text within an area. For both areas and lines, you want to use color as effectively as possible to improve your ability to distinguish different objects one from another. For an area, you can express its cohesion as a unit by making it a different color than the rest of the screen, for example, a cyan window on a white screen. But you also need to use color to discriminate within lines. For example, in a word processor, you may need to mark text for cutting and pasting or to draw attention to a menu choice.

I propose the following commonsense rule about areas and lines:

Rule 1: Use the background color to distinguish areas and the foreground color to distinguish within lines inside areas.

So you might make a window black on cyan to distinguish it from a black-on-white screen. If you need to emphasize words within the window, you might use bright white or yellow on a cyan background (the background color expresses the fact of belonging to the area).

The second method of categorization applies to actual cognitive functions. You can analyze three different functions for color in a display, namely, emphasis, de-emphasis, and normal reading. The requirements for these three sorts of colors are very different. The emphasis color needs to catch your attention. It can be as brash and eye-hurting as you like; this is the color you use for warnings, error messages, and clear marking or selecting. The de-emphasis color is used to tone down nonvital information. For example, in a word processor, you might have a permanent status line containing information that you refer to only occasionally. This should not stand out more than the normal text. Far from catching your eye, it should be there only if you actually look for it. The color for normal reading should be as easy to read and as nonfatiguing as possible.

These three color categories visually form a third spatial dimension of sorts on the screen: Normal is the ground plane, emphasis jumps out of the screen at you, and de-emphasis recedes into the back-

ground. These three categories are independent of the area and line categories, so you can employ them all as "axes" to create two-dimensional tables containing six color combinations (see table 1).

Using this technique, you can devise consistent color schemes that apply across all your application programs. You may feel that this is a lot of fuss about nothing and that playing around by trial and error is as good, but my experience has been that even with only 16 screen colors and five or six application programs to play with, consistency soon becomes impossible without some formal structure.

A few extra categories are also needed. You could make a series of such tables: one for the primary or "best" color combination, one for the second best, and so on, so that you can use these successively to color new windows on the screen.

Then you need to apply some restrictions. On an IBM PC, for example, the usable color combinations are quite limited. Of the possible combinations of the 16 available colors, many provoke instant nausea—try bright yellow on magenta. On machines that use analog monitors, like the Amiga and Apple IIGS, more palatable combinations and more subtle shadings are possible. Even so, I propose these conservation principles:

Rule 2: Try to minimize the number of colors on the screen at once.

Rule 3: An area should be based on a single color combination (foreground and background) with one emphasis color and one de-emphasis color that are sparingly used.

Rule 3 suggests that I not use an extra color for the border or title of a window; in fact, I prefer a thin black rule as the border for windows. Black, as well as providing the best contrast for reading text, has a structural quality that makes it the best color for defining frames, borders, boxes, and diagrams of all sorts. This is probably due to the fact that we all grow up reading black text on white paper.

Using these principles, I have arrived at my optimum set of colors. My first choice is black on brown (dark yellow), which is used everywhere from the DOS prompt to the various editors and programming environments. My second choice is black on white, which I use to discriminate pop-up windows, like the SideKick Notepad, SuperKey, and the various ProComm menus. My third choice is black on cyan, which I use as a second level of discrimination; for example, the Files menu of the SideKick Notepad is black on cyan on my system. With-

Table 1: My choices for emphasis, de-emphasis, and normal printing within areas and lines.

	Emphasis	Normal	De-emphasis
Area	white on red	black on brown	black on green
Line	white on brown	black on brown	blue on brown

in these sets of colors, I use bright white as the emphasis color and dark blue as the de-emphasis color.

I also find it useful to distinguish some actual software functions that are represented by a consistent color combination throughout my system. For example, I choose to make all help screens black on green—green seems to express the notion of assistance—and all error messages or warnings are bright white on red.

I don't claim scientific status for these rules, but I still have 20/20 vision and can sit up all night programming without headaches. I view the idea of returning to a monochrome system with horror; when using SideKick on a friend's green-on-black monochrome monitor, I found the screen totally confusing.

Implementing Your Scheme

It's all very well deriving theoretical principles for color selection, but how do you actually implement the resulting scheme? Software writers often take a pretty cavalier approach to color selection in their programs. I have software ranging from the good—you can change the colors of every part of the system—to the bad—you can change only the background, or various unrelated bits of the program share the same color—to the ugly—you're stuck with what some color-blind programmer chose.

If the program permits color selection at all, you still may face potential pitfalls. I seem to have dozens of programs that set the background or border color back to black when I exit from them.

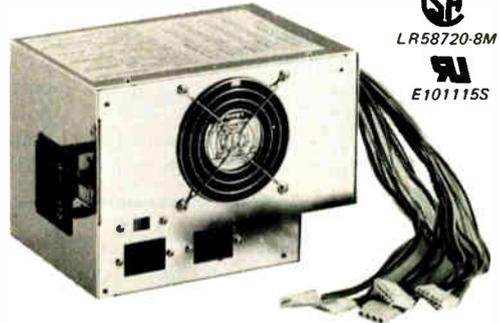
I think you should be able to expect modern software to come with a comprehensive color installation routine. Ideally, this routine would let you alter the colors interactively on a facsimile of the actual application screen. Alternatively, software that uses a simple teletypewriter-style user interface, like most compilers and interpreters, would be transparent to the colors you have already set; it wouldn't alter those colors, either during use or upon exit.

Some software does deliver the goods. For example, Gazelle Systems' Q-DOS shell program lets you select the colors on the actual application screen, while Executive Systems' X-Tree is nearly as good. My favorite editor, PC-Write, doesn't have an interactive color routine but does allow you to put color attributes into a setup file; it also lets you control everything down to the color of the cursor when it goes past the end of a line. The shareware communications program ProComm has adequate color installation as do most of Borland's products, with an occasional exception. SideKick and Su-

continued

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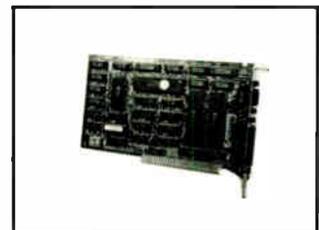
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perKey are fine, but Turbo Pascal's TINST installation program lets you change everything *but* the editor's screen colors—a particularly virulent bright yellow on black. Turbo Prolog lets you set every color except for the thick black window frames, which make for a very unsightly multiwindow screen.

Drastic Action

As a rule, I will no longer use software that doesn't permit color installation, but

some programs are so essential that drastic action is justified. I couldn't live without Turbo Pascal, but I also couldn't live with its retina-aping editor, so I patched it. Probing around with DEBUG I got lucky quite quickly, as the color data is kept in one place in low memory: CS:177—attribute for highlighted, or emphasized, text; CS:178—attribute for normal text; and CS:179—attribute for marked, or de-emphasized, text.

Since then I've become the Sherlock

Holmes of color software, sniffing out color data wherever it may be hidden. The general trick is to search for INT 10s (video interrupts) in the code, using DEBUG's search feature. Then by browsing around them, look for the ones that are calls to video function 9 (write attribute/character) and occasionally functions 6 or 7 (scroll active page) and patch the correct attribute value into the BH or BL register. Practice on a copy. It's sort of fun for a while, but I can't help feeling that it shouldn't be necessary.

It's easy to write programs with flexible color installation, especially if you're working in C or Pascal; if you use variables instead of literals for the color attributes, writing a program to install the colors is easy. But if you don't include this capability from the start, it's a real pain to do later. Many programmers must work exclusively on monochrome screens or simply don't think of it, because there is far too little color flexibility across the industry. If you are writing applications that are portable across different computer families, the problem is more difficult; but for IBM-only programs, there is no excuse. Portable programs could at least be transparent as, for example, XLISP is.

Under PC-DOS 2.0 or higher, you can deal with those programs that disrupt your colors when they exit by putting a color-setting ANSI escape sequence into the DOS prompt string. For example, I use prompt \$e[30;47m[\$p]:, which resets the screen to black on brown (you must have ANSI.SYS loaded for this to work).

Those irritating programs that blitz just the border color require you to do a manual repair job using, for example, Norton's scratr utility. I eventually got fed up with scratr clearing my whole screen, so I wrote a little utility in Turbo Pascal 3.0 that sets the border color. If you share my little color obsession, BDR.PAS is found in listing 1.

It's nice to dream that soon we will all be using workstations with 256-color screens and graphics coprocessors and that all software will come with a built-in interactive palette editor, but I shan't hold my breath waiting. ■

Editor's note: This is Dick Pountain's last BYTE U.K. column. Dick is off covering the Hannover Faire for BYTE. When he returns, he'll begin work on a new series of columns dealing with software algorithms. Dick will continue to report on new and interesting European hardware and software in the What's New sections of BYTE and BIX. His first Algorithms column, on run-length decoding, will appear in the June issue.

Listing 1: BDR.PAS, a Turbo Pascal 3.0 program to change the color of the border on the screen of an IBM PC or compatible. When compiled into its .COM form, BDR expects one numerical parameter between 1 and 16 to tell it what color you wish your border to be.

```
program bdr;
var color,error: integer;
begin
  if ParamCount <> 0
  then begin
    val(ParamStr(1),color,error);
    if error = 0 then Port[$3D9] := color
  end
end.
```

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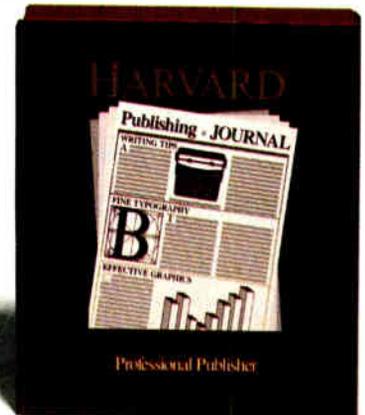
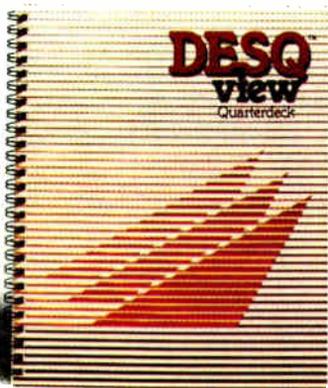
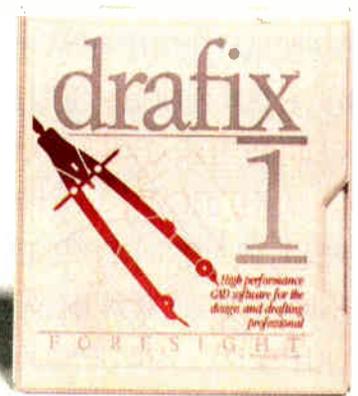
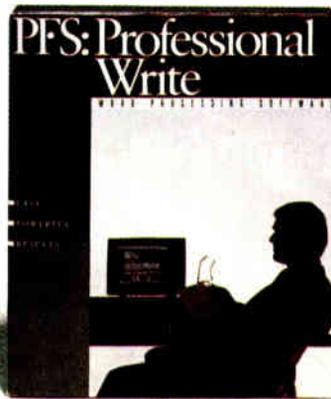
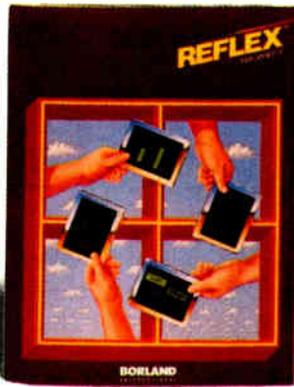
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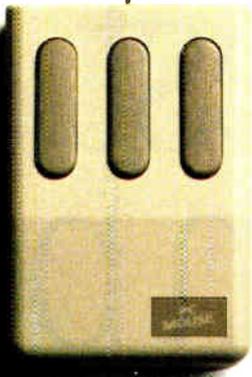
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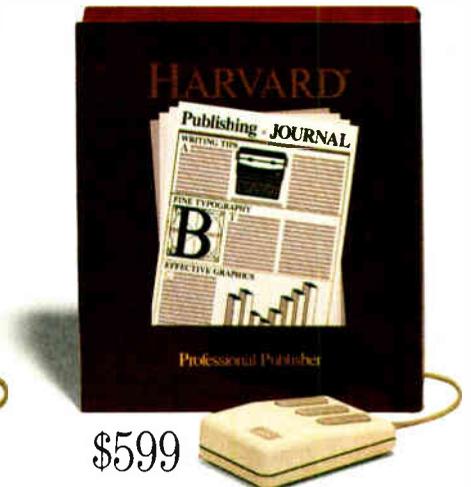
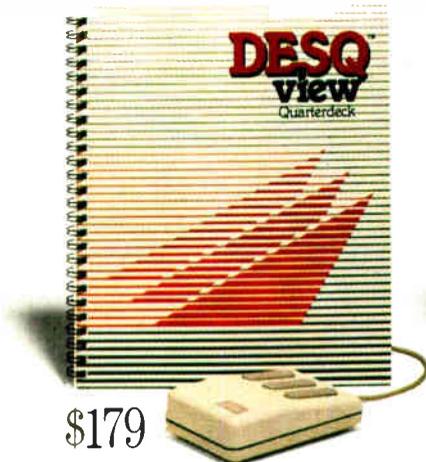
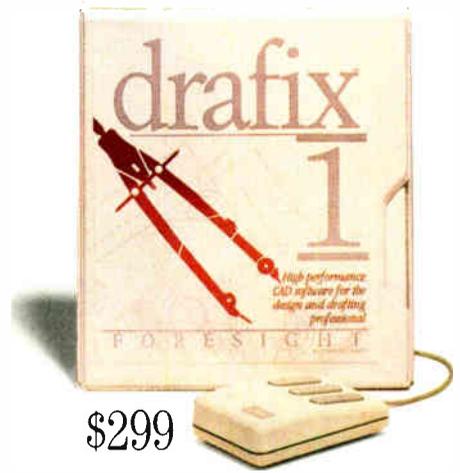
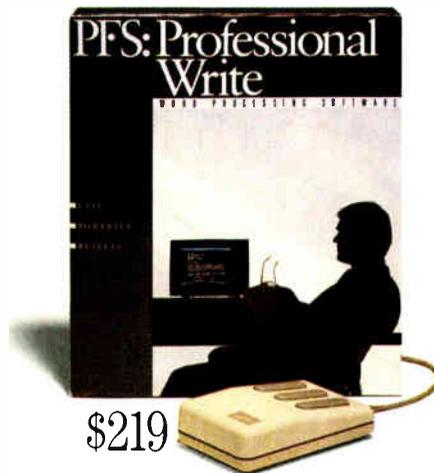
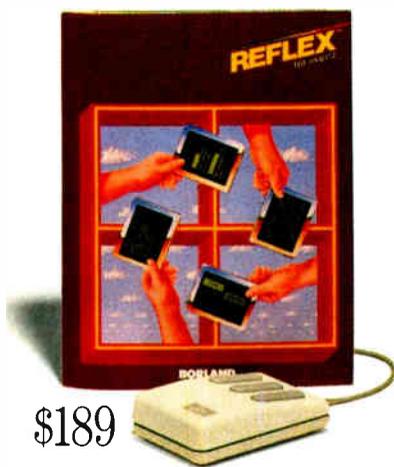
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CHAOS MANOR MAIL

Conducted by Jerry Pournelle

Dahdahdah Didididit?

Dear Jerry,

Computer types interested in using their computers for packet radio communication via amateur radio shouldn't be deterred by the five-word-a-minute Morse code and simple electronic theory tests required by the FCC for the Technician license (see "New Communications Not So New," December 1986 Chaos Manor Mail). Five words a minute is 25 characters a minute—or around one character every two seconds. If you fill in seven out of ten blanks correctly on the content of a plain text message sent at five words a minute, you've passed.

You can learn to decode five words a minute in a short time by practicing changing into dits and dahs the signs and advertisements you see while waiting in lines. BYTE is just another way of saying "dahdididit dahdidahdah dah dit."

Morse code practice programs are available as shareware on ham radio disks for the IBM PC and compatibles from many sources.

David Cowhig
Arlington, VA

I agree that it isn't hard to learn Morse code. On the other hand, I still don't see why it's needed; there are fewer and fewer ham operators all the time. I would think that some infusion of new blood would be welcome. And hackers still consider Morse code cruel and unusual punishment.—Jerry

Dear Jerry,

The reason you gave for the FCC's requirement of the Morse code test on the amateur license is largely correct; for reasons many people have difficulty understanding, most of organized American amateur radio, specifically the Amateur Radio Relay League, has done everything it can to keep that requirement on the books. My college roommate (also a ham) and I used to laugh that someday prospective hams are going to wonder why they are required to interpret this not-very-good teletype code manually. I enjoy using Morse code and in fact am fairly good at it, but requiring it for VHF licenses does nothing but exclude digital experimenters. Contrary to your reply to David Knisely's letter the Technician license *does* require a code exam. Many

other countries' versions of that license do not.

David Kazdan
Cleveland, OH

Latin Lives

Dear Jerry,

Regarding Charles H. Porter's letter (December 1986) divining the death of CP/M: I have never used CP/M, but I do have a recent reissue of the third edition of Newton's *Principia Mathematica*, originally published in 1726, which is an example of original thought written in Latin halfway between the time of Columbus and now, not twice as long ago, as Mr. Porter would suggest.

Furthermore, the availability of mass-produced books due to the introduction of printing in Europe in the 15th and 16th centuries had the exact effect he denies, namely, resurrecting long-forgotten Greek texts, to the great benefit of Western science.

Hugh David
London, U.K.

V20 Quirks

Dear Jerry,

I recently read that you are tinkering with the NEC V20 chip. I have a sad tale of incompatibility for you.

I own a Sanyo MBC-755 PCCompatible with an Intel Above Board installed. The computer has few or no compatibility problems. However, I read and heard all sorts of good things about the V20, so I went out and got one.

At first, it seemed as if the chip was working rather well. But after about 15 minutes, it locked up tighter than Tokyo traffic. I rebooted and reloaded everything onto RAM disk. Five minutes passed and it locked up again. Needless to say, this continued until I excised the V20.

I think I know why this happened: The Sanyo is an 8-MHz machine. I was careful to buy the V20-8, but it seems that the little bugger is too fast for the 150-nanosecond memory and support stuff on the Above Board. Know anybody who wants a V20?

I spoke to several other PC users here, and one guy said his ITT XTRA also didn't like the V20. Seems that whoever wrote the ITT's BIOS did a cheap, sleazy thing. The BIOS is full of timing loops

and one of the things that it does as part of its power-up test is to test the clock frequency against some DMA timers. Naturally, it decides that something has gone terribly awry and indicates a catastrophic failure code.

Oh well, I guess these are some of the drawbacks of an open architecture. Good luck with your V20 experiments.

Spence R. Spencer
APO San Francisco, CA

There are a lot of quirks about the V20. Some use them with no trouble at all and get wonderful results. Others have problems. I guess you just have to experiment. Thanks for the information.—Jerry

Word Processor Search

Dear Jerry,

I just wanted to comment on your remark in the November 1986 BYTE that you still had not decided which word processor you preferred. I remembered that you had made some favorable remarks about Q&A when it first came out.

I am now using version 2 of Q&A and like it very much. It seems to have good capabilities but pretty much keeps out of the way. I think the updated version has some changes that make it more suitable as a day-to-day word processor. These include the ability to make automatic backups of files and to turn off the tab line indicator "golf ball." The macro key capability is also very handy.

The major liability I can see is that some functions, like block moves, boldfacing, or underlining, take a fair amount of time and number of keystrokes. In its favor is the very fast screen updating and the very wide range of printers supported. I also like the integrated spelling checker and have ordered the thesaurus module that Symantec has announced.

Now, if only there was a way to make the cursor stop blinking at me, other than cutting a trace on the video board. I know it can be replaced within a program by a software-controlled nonblinking cursor, because I have seen a memory-resident utility that does it. Unfortunately, it is not compatible with some other memory-resident items that I value more, and it uses techniques that some programs overcome or ignore or fail to reset when terminating. Nonetheless, it shows that it is possible.

continued

ble and I think all programs, particularly word processors, should allow the choice of a blinking hardware cursor or a non-blinking software-generated and -controlled one.

Rich Wood
Orinda, CA

I agree completely that the Q&A editor is one of the nicest in the business, and their spelling checker and other auxiliary software is good, too. Plus you get the database and financial software.

My only problem is that the program is

a real memory hog that demands more than I want to give it. I use a lot of memory-resident programs, and while Q&A can take the place of most of them, it doesn't do it all.

Still, I strongly recommend that anyone starting in the PC game look at Q&A; it has features that nothing else can have. Alas, one of them is not a nonblinking cursor. —Jerry

Dear Jerry,

While reading your column in the September 1986 BYTE, I noticed that two

applications you mentioned having problems with were spelling checking and indexing. WordPerfect 4.1 does a great job at both.

You can spell-check a single word, a page, or an entire document with a simple keystroke (actually, a "chord"). As the program breezes through your file, it uses a main dictionary file plus a supplemental one compiled by the user. (These are best installed on a hard or virtual disk.) When it comes to an unrecognized word, it displays a list of possible correct spellings in order of resemblance to the word in question. As the program hunts for alternatives, the user may either (1) select a replacement from the list of alternatives, (2) skip the misspelled word once, (3) skip the word throughout the rest of the search, (4) add the word to the supplemental dictionary, (5) edit the word, (6) look up another word, or (7) search for other spellings that are phonetically similar to the word in question. The process is very fast and "learns" easily.

Indexing is not so automatic, as the user must select words for inclusion, but it does allow sublevels in the index and finds page numbers of all occurrences.

The program is a very good all-around heavy-duty word processor (although it does have some minor flaws). It even includes, among other unique features, a thesaurus.

Scott Englander
Ringoes, NJ

As I've said in the column, WordPerfect has become my default PC text editor. It's not that I'm so happy with it as that all the others have more or less fatal (for me) defects or lack features that are vital to me. —Jerry

Model 100 Book

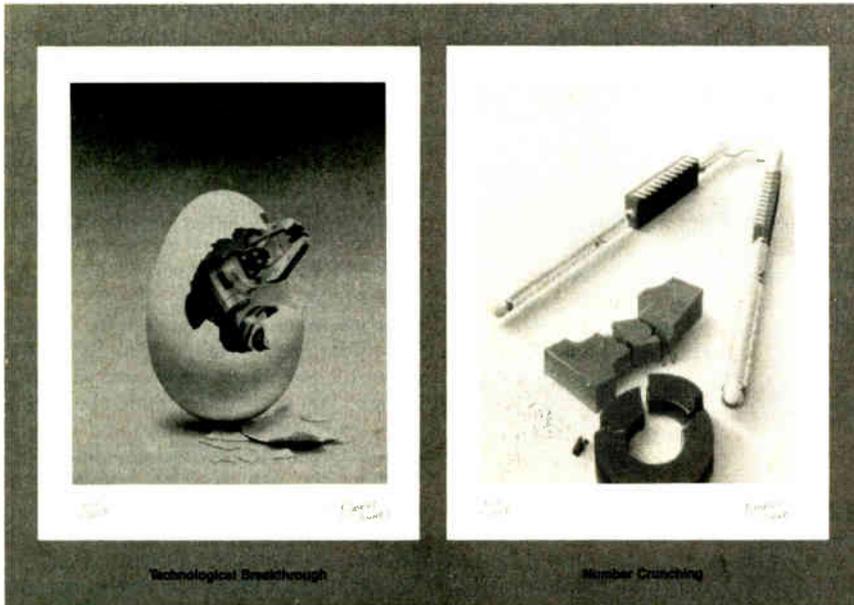
Dear Jerry,

In your July 1986 column, you made a reference to the book *Exploring the Radio Shack Model 100*. You suggested ordering this book directly from the author (Marvin C. Mellon, 6914 Berquist Ave., Canoga Park, CA 91307). However, a call to that area code through directory assistance yielded no such name. How can I contact him quickly for ordering and pricing details?

William R. Holden
Baton Rouge, LA

Apologies. That should have been Marvin C. Mallon, who definitely is listed in the Canoga Park phone book and directory.

And his twin books on the NEC PC 8201 and Tandy Model 100 are still the best introductions to those machines that I know of. —Jerry ■



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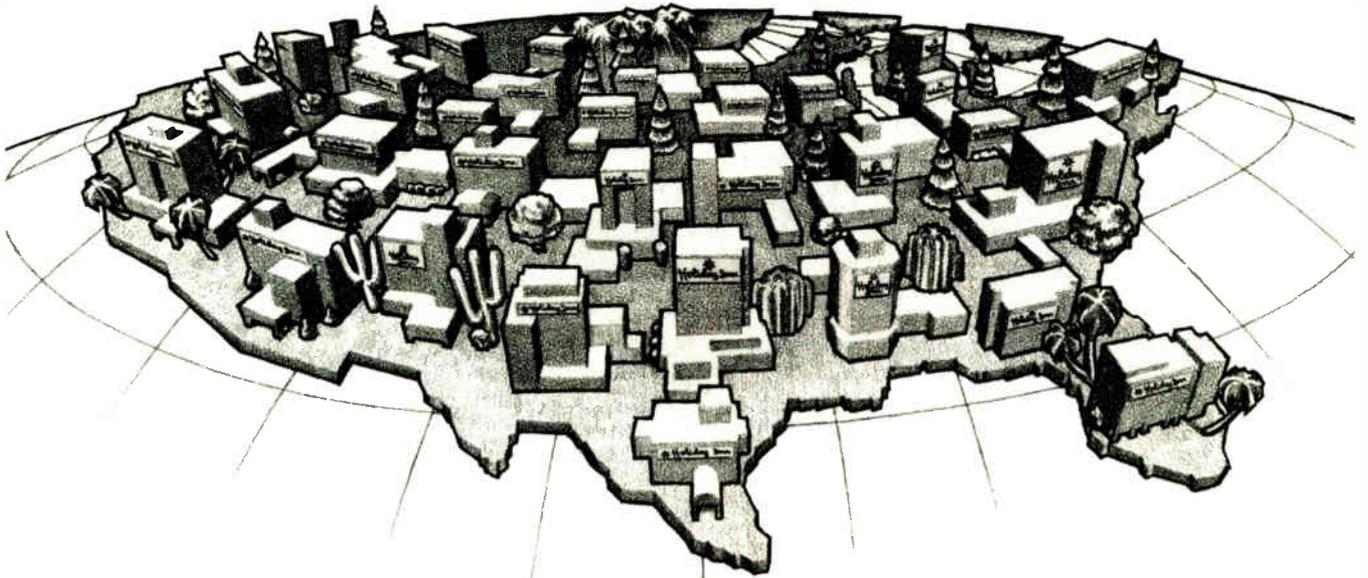
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The Best of BIX is a look at just a few of the thousands of messages that are posted each month on the BYTE Information Exchange. This month's choice of offerings come from the Amiga, Atari ST, IBM PC, Pascal, and BASIC conferences. If you'd like information on how to join the BIX community, see the advertisement on page 340.

AMIGA

This month's Amiga section starts off with a thread on possible problems with keyboard extension cables and goes on to a longish thread on WAITing for multiple ports.

KEYBOARD EXTENSION CABLES

amiga/softw.development #3639, from dmilligan (David Milligan), Sat Jan 17 23:54:49 1987.

TITLE: Beware of keyboard extension cables!! PHOOF!

Hey, people, I'm in a real tight bind right now. I'm using my Atari 1040 ST to type this 'cause I fried my Amiga's keyboard by plugging in an extension cable that had a screwed-up plug contact on one end. When I plugged it into the Amiga's keyboard, it shorted two contacts together. Now, when I turn on the Amiga, the LED on Caps Lock always stays on and no response at all from the keyboard. The Amiga still boots just fine and the mouse and trackball still work, but have you ever tried to operate a C compiler without a keyboard on the Amiga?

I've disassembled the keyboard physically and there are only two ICs visible. I can replace the chip(s) if that'll fix it, but I don't know how to diagnose the electronics used in the Amiga keyboard. I'm an ohm meter-and-soldering-iron type of guy, but that's as far as it goes.

amiga/softw.development #3640, from aalexis (Andrew Alexis), Sun Jan 18 10:25:46 1987. A comment to message 3639.

The same thing happened to me, but I'm afraid it resulted in a new system board, too. It actually happened twice and was not properly fixed the first time. It turned out to be the keyboard itself, or rather, a short in it.

amiga/softw.development #3644, from dmilligan, Sun Jan 18 19:43:57 1987. A comment to message 3640.

I'm keeping my fingers crossed on the motherboard - it appears to be okay and the system still boots fine.

amiga/softw.development #3646, from aalexis, Sun Jan 18 20:33:36 1987. A comment to message 3644.

The second time my system booted fine too, except for the keyboard. The first time, there was smoke and molten plastic, so be careful. As far as I can tell, replacing the motherboard is kind of a cure-all for whatever ails the machine. But my Amy has worked just fine since the second time (fingers crossed).

amiga/softw.development #3649, from dmilligan, Mon Jan 19 00:37:27 1987. A comment to message 3646.

I had a friend bring his keyboard over and everything worked perfectly, so I can safely say that it's the keyboard that fried. Now, if I only knew for certain which chip was cooked. Actually, the only one I can get locally is the 556 timer, so if that doesn't fix it, it's new keyboard time.

amiga/softw.development #3688, from dmilligan, Fri Jan 23 02:24:06 1987. A comment to message 3649.

If anyone cares to know, the fix for my fried keyboard WAS the 556 timer chip. After unsoldering it, I was able to see the black burnt area beneath the chip. I replaced it and now it works again. Whew!

amiga/softw.development #3689, from langeveld (Willy Langeveld, moderator), Fri Jan 23 03:09:14 1987. A comment to message 3688.

So what was it that blew it in the first place? Might be nice to know in case it happens to one of us sometime. . . .

amiga/softw.development #3782, from dmilligan, Sun Feb 1 05:20:42 1987. A comment to message 3689.

What caused the failure was a defective set of handset crimpers that I bought locally - when the handset plug was crimped to the cord, the metal tabs in it set at an angle, and when it was plugged into the keyboard, it shorted the +5V line with the lines next to it. PHOOF! After I repaired the keyboard and got a decent set of crimping pliers, I tried it again and it works just fine. I'm using a regular modular wall jack cord and not the wimpy handset stuff. Handset cords just won't work (at least none that I've tried).

amiga/softw.development #3692, from grr, George Robbins, Commodore-Amiga), Fri Jan 23 11:06:58 1987. A comment to message 3688.

The cable you used must have reversed +5 and ground. This is not a healthy mode of operation for TTL (transistor-transistor logic) or near-TTL chips like the 555 timer. Some phone cords swap the conductors, some don't - the phones don't much care.

amiga/softw.development #3783, from dmilligan, Sun Feb 1 05:24:29 1987. A comment to message 3692.

Well, the cable conductors weren't reversed, as I've been through that before because SOME phones care, unfortunately. What happened was a badly crimped connector wadded the sockets' contacts together.

WAITING ON MULTIPLE PORTS

amiga/softw.development #3650, from dquick (Dave Quick), Mon Jan 19 01:38:58 1987.

I've run into a small problem and wondered if anyone else had any suggestions. I'm working on a program that needs to do two things within a repeating loop: Check a IDCMP port for messages, and check for a regular timed event. I'm using the IDCMP for RAW key events and for Mouse events using Wait(). This is no problem. The problem is that while I'm waiting for a message, I'd also like to wait for a timer event so I can change color registers to cycle colors. RKM 1 recommends using Wait() to do this, but the details for setting this up properly are very sketchy. If anyone could provide some help on this, I'd be internally grateful. (Helps with indigestion.)

amiga/softw.development #3656, from cschepner (Carolyn Schepner, Commodore-Amiga), Mon Jan 19 13:23:02 1987. A comment to message 3650.

All you have to do is Wait() on a combined mask. To create the mask, OR together the masks you want to Wait() on. For example:

continued

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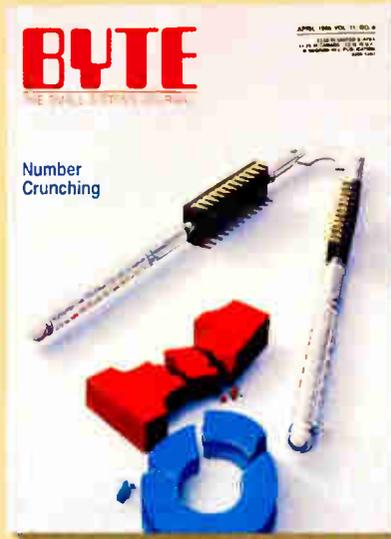
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ULONG myMask;

```
myMask = (1 << timerport->mp_SigBit) | (1 << window->UserPort->mp_SigBit); signals = Wait(myMask);
/*signals
also a ULONG */
```

Then check signals and handle messages for the port(s) whose sigbit is set. Note that if you used CreatePort() to create your timerport, there has been a signal bit allocated for the port. If you're doing it by hand, YOU must allocate the signal bit and properly initialize the MsgPort.

amiga/softw.development #3669, from dquick, Mon Jan 19 22:45:35 1987. A comment to message 3656.

Thanks for the quick response, Carolyn. I follow you so far, but how do I tell the timerport that I want a signal every 50,000 micros or so? That seems to be the only remaining part of the puzzle.

amiga/softw.development #3723, from cschepner, Mon Jan 26 19:17:00 1987. A comment to message 3669.

You use SendIO to send a timer request message with the command TR__ADDRREQUEST. Use 50,000 for tr__time.tv__micros.

amiga/softw.development #3753, from dquick, Sat Jan 31 02:19:50 1987. A comment to message 3723.

Thanks, Carolyn. I now have timer messages every 50,000 micros, and my colors are cycling just fine until I press a key or move the mouse. At that point, everything hangs. The routine I had for reading RAWKEY and MOUSE events worked great until I tried to marry it to the timer routine. The mask I have set up to use with Wait() looks like: (1 << Timer__Port->mp_SigBit | 1 << window->UserPort->mp_SigBit)

After the wait I do a: while(message = GetMsg(window->UserPort))

Within the loop I check for various key or mouse events by assigning message structure member's values to variables, then ReplyMsg(message).

```
After that loop I: (void) GetMsg(Timer__Port);
do_my_cycling( ); Time__Req.tr__time.tv__micros=50000;
Time__Req.tr__time.tv__secs=0; SendIO((char *)
&Time__Req.tr__node.
```

Then I start the whole Wait() loop over at the top. I'm probably doing something very obviously wrong to someone with more C experience. Am I backing up the timer port when I read the UserPort? I hate to be such a pest, but I'm going crazy very quickly on this one.

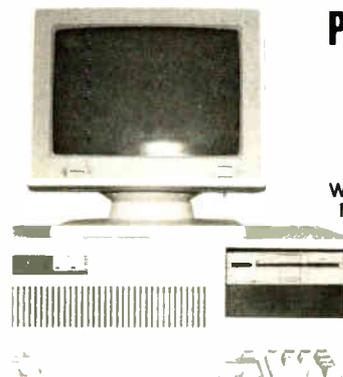
amiga/softw.development #3754, from cheath (Charlie Heath, Microsmiths Inc.), Sat Jan 31 03:44:21 1987. A comment to message 3753.

Looks to me like you're reusing the timer message before the previous one got finished. What you probably need to do is something like:

```
(flags = Wait(both_sig_bits) )
if ( flags & 1 << TimerPortSigbit ) {
    send_another_timer_request( );
}
if ( flags & 1 << window->etc_sigbit )
{
    Process_GetMsg( );
}
```

continued

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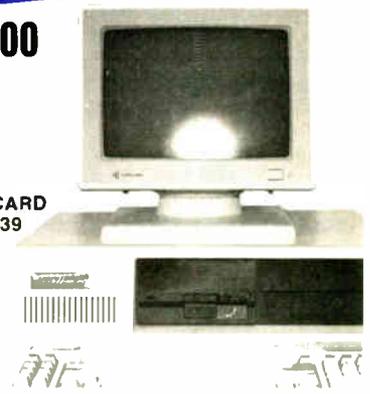
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That is, test the returned signal bits from the Wait() to see if the timer has expired, 'cause if it hasn't and you reuse the message, it's GURU time!

amiga/softw.development #3755, from jsan (Jez San), Sat Jan 31 07:39:31 1987. A comment to message 3753.

I'm bewildered why you are using timer requests ANYWAY!!! Shirley, if you wanna do color cycling, the best thing is to use a VBlank routine that switches the colors EVERY frame (i.e., 20 milliseconds for me and 16.6 milliseconds for you)! Or, if you don't want the smoothness of transition that an every-frame routine will give you, do a two-VBlanks-per-cycle routine instead! This can be done using the 68000 exception vector 3 in hardware or I'm sure there's an equivalent OS routine that lets you link into the system VBlank queue. Not only is this far less hassle than talking to the CIA chip (8520), but it's also a more direct way of accomplishing it!

amiga/softw.development #3781, from dquick, Sun Feb 1 03:25:30 1987. A comment to message 3755.

Basically, I'm using timer requests because they were the first thing I found in the RKMs that looked like they'd do what I wanted (and that I thought I might be able to figure out). I'm sure that the VBlank routine would be much smoother. If you can point me in the right direction as to where to look in the docs for the information I need, I'd love to try it. Please try to keep it to C stuff, though. I'm just starting to feel like I'm getting my C legs straight, without getting into 68000 assembly just yet. (Give me time.) My usual approach to a software project is to design it first and then try to figure out how the heck to do what I just designed. It doesn't always work, but when it does, I learn a lot very quickly.

amiga/softw.development #3784, from jsan, Sun Feb 1 07:57:39 1987. A comment to message 3781.

Suggest reading ROM Kernel Manual (volume 1) page 1-51 and 1-56 for Vertical Blank interrupts. Also, I suspect you will need a BIT of assembler code to vector off the Vertical Blank. . . . but I may be wrong, since I don't know C. . . . !

amiga/softw.development #3785, from dquick, Sun Feb 1 16:50:32 1987. A comment to message 3784.

Thanks, I'll check that out. From my initial scan of that info, it looks like it might be a good alternative. Mostly it will depend on how correct their C example is. Often, it takes me longer to figure out where the problems in the examples are than it does to figure out the actual procedure itself. I still have the original manuals, so this might not be as big a problem for someone with the Addison-Wesley books.

If anyone has purchased both, I'd be interested in finding out if the Addison-Wesley versions are more correct, or about the same as the originals. I've done some assembler on 6502 machines and even a little on Intel chips, so I'm not afraid of learning it on the Amiga. The real concern is development time.

Since most of my work right now is not real-time graphic-intensive, I really don't require the extra speed and control I know I'd get in assembly. Actually, the timer-request code seems to work pretty well for what is basically a very leisurely color-cycling application. You do have to play with the actual timing interval quite a bit in order to avoid little glitches in the cycling.

Speaking of VBlank, there is also a VBlank option in the timer-request system. I didn't start out using that because the RKM Volume 1 seemed to imply from the examples that this was really more useful for time delays of a second or more.

amiga/softw.development #3789, from afinkel (Andy Finkel, Commodore-Amiga), Sun Feb 1 21:35:25 1987. A comment to message 3785.

VBlank operations are good for applications where you don't need a finer time resolution than 1/60th of a second. Color cycling fits into that (usually). You might also be able to use Intuiticks, which are really easy to add once you have a working IDCMP main loop waiting on multiple events.

(There is a gotcha with those. V1.1 Intuiticks come twice as fast as they were supposed to. V1.2 corrects this, but if you want to have the same speeds on both, you'll have to check for version number. This isn't a problem if it's for your own use, of

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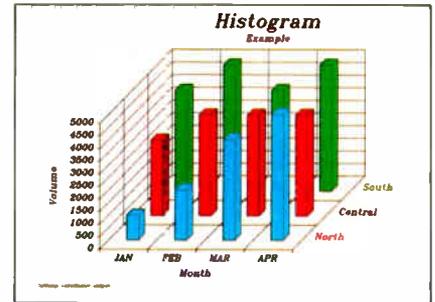
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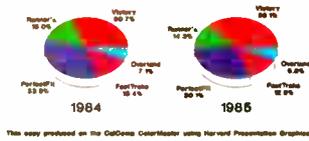
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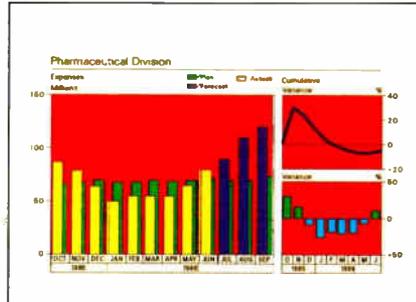


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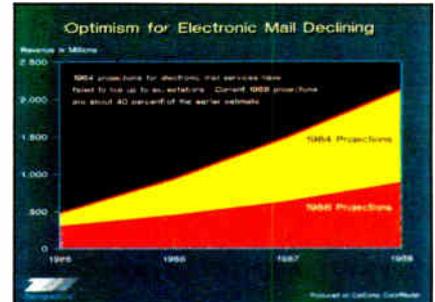
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course, and probably will stop being a problem very soon as more and more people pick up V1.2)

ATARI ST

This month's Atari sections starts off with a thread on the strange case of "re-booting," which finishes with some thoughts on the length of time required between power-off and power-on. Next is a thread on C-Shell command-line problems, and we finish up with two short (though related) threads on trackballs, mice, and joysticks.

RE-REBOOTING PROBLEMS

atari.st/main #1601, from tjefries (Tom Jeffries), Fri Jan 23 01:52:42 1987.

There has been some discussion on BIX of the ST's restarting the boot procedure after getting nearly finished. I discovered something that may be coincidental and is silly enough that I hesitate to bring it up, but I would be curious to see if this is the answer, and the only way to find out is to have several people try this "fix."

Recently, my screen display started flickering. This has happened before and I have been told that sooner or later I would need some new chips. I remembered, though, that I had been switching monitors a lot recently, so I tried pushing the monitor plug in a little harder. The flicker was gone.

Another thing that was gone, though, was the re-rebooting problem, which had been getting fairly bad (once out of every two or three times). I have not had the problem reoccur in the last 8 or 10 hours of work.

Is the solution really this simple? It certainly could be that if the OS doesn't see a monitor, it will reboot. I'm not sure why the reboot occurs when it does. Is the interrupt that checks the monitor shut off during disk I/O?

If you have been plagued with this problem, try pushing the monitor connector in as hard as you can without breaking anything. Post a note here with the results.

atari.st/main #1602, from dsmall (David Small), Fri Jan 23 01:54:20 1987. A comment to message 1601.

Sure, the monitor connector will generate a high-priority MFP interrupt if it gets loose. Having that jiggle is singularly bad karma - in fact, last time I trashed my hard disk, that was why.

atari.st/main #1605, from alex (Alexander Pournelle, Workman & Associates), Fri Jan 23 02:04:42 1987. A comment to message 1602.

Hmm, I thought that was the PLI: Product Liability Interrupt. It shut down the ST before it croaked a monitor, so. . .

atari.st/main #1609, from blevine (Robert Levine), Fri Jan 23 21:26:50 1987. A comment to message 1601.

Glad to know I'm not the only one with the re-rebooting problem. I don't have any flicker on the monitor so I can't confirm your observation. However, my monitor connector has a loose fit and I keep moving the ST around the desk to get a more comfortable position for the keyboard. So I wouldn't be surprised if that contributed to the problem.

I'm pretty sure that mouse movements during the boot phase will sometimes cause the re-reboot, but not always. I did some

experiments where I booted repeatedly off a disk with no AUTO folder and no accessories (in order to keep things as simple as possible) and mousing around appears to be a no-no.

I'm also thinking that you need to give the ST a good rest when you turn the power-off and on for a cold boot.

atari.st/main #1612, from tjefries, Fri Jan 23 23:29:11 1987. A comment to message 1609.

As far as I can tell, waiting less than 10 seconds on a power-off is asking for trouble; knowledgeable people have recommended 15.

atari.st/main #1613, from jtittsler (Jim Tittsler, Atari Corp.), Sat Jan 24 01:41:00 1987. A comment to message 1612.

The necessary off-time varies between the 520 (where you are switching the +5V supply) and the 1040 (where you are switching the AC line). A second or two will work with the 520 . . . but 10 seconds or so is probably more appropriate for the 1040.

atari.st/main #1615, from tjefries, Sat Jan 24 02:06:26 1987. A comment to message 1613.

Actually, I have an upgraded 520. I bought it before the 1040s were out. Seems to take more than a second or two, but maybe mine just has especially retentive memory chips (small chuckle).

atari.st/main #1624, from dsmall, Mon Jan 26 22:06:33 1987. A comment to message 1613.

A better way is to put a short assembler routine into your AUTO folder that zaps the memory-valid flags. Then, anytime you RESET, you force a system coldstart.

Just check out the BIOS variable list for the two .longs to zap.

C-SHELL CAUTIONS

atari.st/main #1630, from sprung (Ron Sprung), Thu Jan 29 00:46:27 1987.

This just cost me two hours of real sweat, folks. I have a copy program that I use from my shell. I'd finished a day's work, and went to back up the files I'd worked on during the day. I happened to be in C-Shell, so typed

```
copy prtsedit.* \ a:
```

then, to my horror, saw:

```
prtsedit.prg -> prtsedit.mod
```

I'd forgotten that C-Shell expands the command line before giving it to the called program. (Sigh.) On the plus side, I did the work better the second time.

The point is, when using a shell that expands the command line, use considerable caution with utilities not supplied with the shell. I think this convinces me to be against command-line expansion by shells.

atari.st/main #1631, from jim__kent (Jim Kent), Thu Jan 29 01:09:59 1987. A comment to message 1630.

Also, it shows the value of a text editor that saves your last version in, say, prtsedit.bak. . . . Many a slip 'tween the fingers and the chip. . . .

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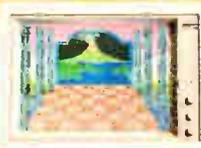
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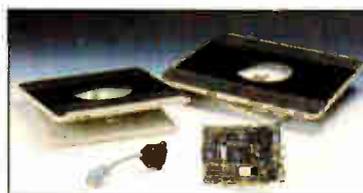
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atari.st/main #1632, from sprung, Thu Jan 29 15:32:36 1987. A comment to message 1631.

Agreed - I have always preferred for editors to rename the read version to .bak when saving the edited version. ConTEXT does that; EMACS does not. Maybe the next version of ConTEXT will be neat enough to make me switch for good.

atari.st/main #1637, from alexl. (Alex Leavens), Fri Jan 30 05:39:36 1987. A comment to message 1632.

Ron, here's a cute little shell script that will back up your source file, and then run EMACS on it. . . (Assumes the source file is a .C file. . .):

```
#
# MEDIT.SH Back up source file, then edit it using MicroEMACS
#

cp $1.c $1.bak
edit $1.c
```

atari.st/main #1639, from sprung, Fri Jan 30 12:07:43 1987. A comment to message 1637.

If I worked from the C-Shell, I'd probably do just that. Guess I need to add some capabilities to my menu shell. It is cute though.

atari.st/main #1640, from tjeffries, Fri Jan 30 13:01:59 1987. A comment to message 1637.

Alex, how would you feel about sharing your technique for enlarging the image on the monochrome monitor?

atari.st/main #1636, from alexl., Fri Jan 30 05:38:00 1987. A comment to message 1630.

I wrote my own command script, called COPY.SH, which explicitly searches through the command line and sucks out the CORRECT directory/pathname, and then passes the copy commands as appropriate to the copy utility, just to avoid such a problem. If you're interested, here it is. . .

```
#
# COPY.SH
#
# copies things from current directory to \ newdirectory
#
#

foreach i ($*)
  set directory = $i
end

foreach i ($*)
  if ($i == $0) then
    continue

  else if ($i == to) then
    continue

  else if ($i == $directory) then
    continue

  else if (-e $directory \ $i) then
    echo "File $i already exists in $directory \ , overwrite it
    (y or n)?"
    set a = $<
    if ($a == y) then
      cp $i $directory \ $i
      echo "---file $i overwritten in $directory \ "
    endif
  else
```

```
cp $i $directory \ $i
echo "---file $i copied to $directory \ "
endif
```

end

#Note: This only works with Dave Beckemeyer's C-Shell. . .

USING A TRACKBALL. . .

atari.st/tech #1509, from jimomura (Jim Omura), Wed Jan 7 00:11:18 1987.

I tried hooking up my Atari trackball to the 1040ST. It won't work in the Mouse port, regardless of the setting (Trackball or Joystick). It works in the Joystick port in the Joystick setting. Funny thing is that although Joust is very nice with the trackball, Time Bandit suffers terribly. Not what I would have expected at all.

atari.st/tech #1550, from jtittsler, Fri Jan 16 03:18:19 1987. A comment to message 1509.

As you mentioned in your message, (one of the two versions of) the Atari trackball can be switched between Trackball and Joystick modes. When in Joystick mode, it detects motion of the ball and generates the corresponding joystick "switch closure."

In Trackball mode, rather than providing the quadrature-phase signals that the IKBD is expecting, the unit provides a "direction" and a "velocity" signal for each axis. The velocity signal is a pulse train that corresponds to the ball rotation. I can think of two ways of using the trackball: 1) Write some software. Put the IKBD in joystick mode and in a custom ISR (interrupt service routine) fake mouse input. This is probably not a good idea because of the number of interrupts you will get in this manner. 2) Modify your trackball. Ignore all of the clever circuitry inside the trackball, and go back to the quadrature signals produced by the optical interrupters on the bearings that the ball rides on.

. . . AND A JOYSTICK

atari.st/tech #1578, from ddenhart (David Denhart), Thu Jan 22 11:49:41 1987.

I need help using the joystick on the ST. The problem is that the operating system is interpreting the joystick button as the right mouse button and calling my mouse server (which I set up using INITMOUSE). I have no problems with the mouse or joystick movement, just the button. Any suggestions?

atari.st/tech #1580, from jtittsler, Fri Jan 23 02:23:21 1987. A comment to message 1578.

The button on joystick1 and the right mouse button are the same (in hardware) as far as the IKBD controller knows. The interpretation of the button is based upon the mode you put the IKBD in. Requesting any of the mouse modes (relative, absolute, or cursor) will make the two buttons logically part of the mouse. A joystick-mode command will make both ports look like joystick ports and logically separates the two buttons.

If you want to use both the mouse and a joystick, you will have to avoid using the right mouse button, and use the software of your mouse ISR to pick off the right button state.

atari.st/tech #1581, from dsmall, Mon Jan 26 22:13:15 1987. A comment to message 1580.

Alexl. tells me that trying to boot the system with a joystick

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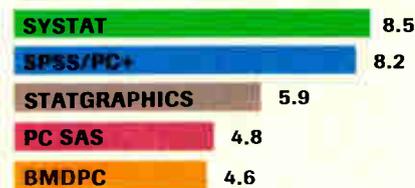
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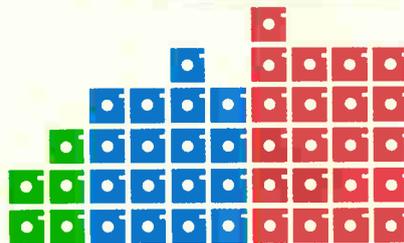
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connected makes it fizzle. I can't remember the exact details, but it was definitely voodoo time.

atari.st/tech #1583, from jtittler, Mon Jan 26 22:54:45 1987. A comment to message 1581.

That sure sounds like voodoo, since an at-rest joystick is all open switches, so if the system can tell it is there, it is doing okay!

atari.st/tech #1585, from alexl., Tue Jan 27 06:04:02 1987. A comment to message 1581.

Early versions of the keyboard had a problem with simultaneous joystick/keyboard entries. If the joystick was on, the keyboard would get lunched. This isn't normally a problem, but see, my joystick had fallen behind my desk, and was on, and I had forgotten it was connected, and. . . <grin>

atari.st/tech #1584, from mmanlove (Mike Manlove), Mon Jan 26 23:18:29 1987. A comment to message 1583.

I tried booting with a joystick in mouse port 0 once. Didn't work worth beans, but it didn't crash, either.

atari.st/tech #1586, from alexl., Tue Jan 27 06:04:45 1987. A comment to message 1583.

This joystick wasn't at rest. (It had fallen behind the desk on its side. . . .)

IBM PC and Compatibles

When is an error not an error? That's the discussion of the first thread of this month's IBM section. It's followed by two long threads that show how discussions progress (and digress) on BIX. The first is everything you ever wanted to know about reset switches. The final thread starts out with a discussion of PATHs but quickly goes into "Trojan horse" programs before returning to the business at hand.

AN ERROR THAT'S NOT

ibm.pc/hardware #2018, from bernie.g (Bernie Gallagher), Sat Jan 3 14:07:47 1987.

The other day, out of curiosity, I ran the diagnostics diskette that came with my PC XT. About halfway through, it came up with the following error message:

```
SYSTEM UNIT 600
0:04:19
ERROR - SYSTEM UNIT 1302
```

I have had my computer for nearly a year now and have had no problems with it. I can't find in the "Guide to Operations" what this error message means, either. Is this a mere "routine" error message, or should I bring in my PC for service? By the way, the diagnostics are version 2.07.

ibm.pc/hardware #2020, from pletcher (Peter Fletcher), Sat Jan 3 16:04:35 1987. A comment to message 2018.

I bet you had a modem connected to your serial port and powered up. The diagnostics are telling you (in their own inimitable way) that one of the handshaking lines on the serial port is pulled high (or low). Try again after physically disconnecting your modem.

ibm.pc/hardware #2024, from bernie.g, Sat Jan 3 19:21:15 1987. A comment to message 2020.

You mean that I got that diagnostic error message just because I have a modem (namely, IBM's own internal 1200-baud PC modem) inside my PC?! Well, I'll try removing the modem and rerunning the diagnostics, but if the message goes away, does that mean there's something wrong with the modem (which is about 6 months old and has had plenty of use since I started running my own BBS without any problems)?

ibm.pc/hardware #2023, from rfm (Rich McAllister), Sat Jan 3 19:05:10 1987. A comment to message 2018.

My "Guide to Operations" and "Hardware Maintenance and Service" books show 13xx as Game Control (joystick) Adapter problems. Do you have a game control adapter (say, on a multifunction card)? Have you ever used it?

ibm.pc/hardware #2025, from bernie.g, Sat Jan 3 19:33:17 1987. A comment to message 2023.

Your explanation sounds more logical than the modem. I have the IBM game control adapter, which the store threw in as a freebie when I bought my PC and I have used it on rare occasions to play Flight Simulator. Aside from crashing into Lake Michigan every time I've tried playing it, it seems to be working correctly, although it has, otherwise, had very little use.

ibm.pc/hardware #2027, from pletcher, Sat Jan 3 19:43:10 1987. A comment to message 2024.

Ignore my previous comment. Serial-port errors are 11xx, not 13xx. It shows how long it has been since I ran my diagnostics. However, if you do get an 11xx error when a modem is connected, it does not mean that ANYTHING is defective - simply that the modem is holding one of the handshaking control lines in a state other than its default (open-circuit) state. You will also usually not see them from INTERNAL modems - only external ones attached to a "real" serial port. As someone else has noted, 13xx errors come from the game port - perhaps you have such a port but your joystick was not connected or your multifunction card hasn't got one but is jumpered as if it had. Sorry for the confusion.

ibm.pc/hardware #2131, from bernie.g, Sat Jan 10 14:14:06 1987. A comment to message 2023.

Yup, that was the problem. I removed the joystick adapter and the diagnostics gave my machine a clean bill of health! Thanks.

THE WORD ON RESET SWITCHES

ibm.pc/hardware #2048, from Ikolakowski (Lee Kolakowski), Sun Jan 4 13:00:10 1987.

In a publication awhile ago they gave instructions on how to add a reset button to your PC. The one thing that was not clear was whether this fix allowed you to bypass the POST routines when a hard boot is required. Any experiences?

ibm.pc/hardware #2049, from jfleming (Jon Fleming), Sun Jan 4 14:00:08 1987. A comment to message 2048.

It pulls one line low for a moment and forces a reset. It is not supposed to bypass the POST, but rather be just like the big red switch without any power spikes. My experience is that the POST will be skipped maybe 20% of the time, especially if you blip the switch real quick.

continued

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ibm.pc/hardware #2055, from geary (Michael Geary), Sun Jan 4 17:10:27 1987. A comment to message 2049.

No, whether the reset button runs the POST is not a random occurrence. It is determined by the last reboot you did before that - cold or warm. It does the same kind again when you press the reset switch. The reason is that there is a warm-boot flag in memory, which is set by the Ctrl-Alt-Del code only. It is not set after a cold boot. You can easily make your reset button always give you a warm boot, simply by setting that flag yourself in your AUTOEXEC.

To do that, type in the following to create a program called SET1234.COM:

```
debug
a
xor ax,ax
mov ds,ax
mov word ptr [472],1234
int 20

r cx
c
n set1234.com
w
q
```

Then, just put "set1234" in your AUTOEXEC.BAT, and your reset button will always skip the POST. The word at 0:472h is the warm-boot flag. The value of 1234h tells the BIOS to do a warm boot. Of course, if some program changes this value to something else, you would get a cold boot again.

One warning. Do not use this program if you have a Paradise Autoswitch EGA card and you use the autoswitching feature. This program disables the autoswitching on that card.

ibm.pc/hardware #2062, from killer1 (Carrell Killebrew, Texas Instruments), Sun Jan 4 21:24:43 1987. A comment to message 2055.

The type of the last boot is what your PC will do when you hit the reset button ONLY IF the memory containing the boot flag does not lose the info. When the reset line is activated, the 8253 timer is halted (so it cannot send refresh requests to the 8237), and the 8237 DMA controller is disabled (so it cannot do a refresh using DMA ch. 1, even if one is requested by the 8253). Many memories will hold good information well past the 4-millisecond refresh interval (would you believe over a second?); thus, a fast button push will USUALLY allow the 8088 to read good info from the boot flag.

It would be nice to disable the POST memory test. < sigh >

ibm.pc/hardware #2067, from rmorse (Ron Morse), Mon Jan 5 00:15:48 1987. A comment to message 2062.

Is this not the same flag that some EGA clones clobber? I know that with both the Video 7 (love that name) VEGA and the ORCHID TurboEGA, I get a full POST with both the hot and cold reboot sequences. The VEGA has a new ROM set that is supposed to correct this problem (version 1.06?), but I replaced it with the Orchid board before I received the new chips, so I cannot testify as to the implementation of the fix.

ibm.pc/hardware #2068, from drifkind (David Drifkind), Mon Jan 5 01:54:59 1987. A comment to message 2062.

Sounds like you need a leetle bitty cap in the RESET line to hold the low time down. The 808x doesn't need RESET low for any particular length of time, just long enough to synchronize the edge. A couple-hundred picofarad cap between chip and switch might take care of it.

ibm.pc/hardware #2089, from geary, Tue Jan 6 16:43:24 1987. A comment to message 2062.

Oops - right you are. My reset button must have a one-shot or something to avoid holding down the RESET line for very long, because it works just fine every time. (It's on an Atron card.)

ibm.pc/hardware #2088, from geary, Tue Jan 6 16:41:04 1987. A comment to message 2067.

No, it's a different problem that causes IBM PCs (not XT's or AT's) to run the full POST when there is an EGA present. The PC's BIOS picks up the value from the low-memory reset flag and holds it in the BP register during POST. It checks the value in BP several times, and the memory test is run after the EGA card's initialization routine is called. The initialization code in most EGA cards (including IBM's) clobbers BP, and when the system BIOS checks BP after that, it no longer thinks it is doing a warm boot and runs the full memory test. It's the PC's BIOS that is at fault here - the documentation for initialization code in adapter cards doesn't say they should preserve BP or any registers. In fact, the IBM EGA BIOS returns an initialization status code in BP! The XT and AT BIOSs don't have this problem. In any case, the fix for an EGA vendor is simple: preserve BP during initialization.

ibm.pc/hardware #2069, from drifkind, Mon Jan 5 02:16:26 1987. A comment to message 2068.

(I mean the HIGH time. Who ever heard of an active-high RESET line?)

ibm.pc/hardware #2091, from drifkind, Tue Jan 6 21:01:02 1987. A comment to message 2089.

If anyone's interested, I just built myself a reset button using a .01 microfarad cap (with a 10K discharge resistor), which does the job nicely.

ibm.pc/hardware #2092, from barryn (Barry Nance), Tue Jan 6 21:19:43 1987. A comment to message 2091.

Would you post the details, please? I built the "NMI Pushbutton" (see 'nmixit.lqr' in the ibm.lbr area of listings, as I recall) for an IBM PC. I'd be interested in doing something similar for my AT clone.

ibm.pc/hardware #2094, from petewhite (Peter White), Tue Jan 6 22:53:41 1987. A comment to message 2092.

Barry, I thought all clones had a "soft" reset built in. I've seen several that had the connections on the motherboard, even when they didn't have a switch. Or are we talking something different?

ibm.pc/hardware #2097, from drifkind, Wed Jan 7 00:37:48 1987. A comment to message 2092.

I would, except that I just looked at a schematic and discovered that what I did doesn't work. I mean, it works, but it doesn't work. I mean . . . oh, well. I'll get it right tomorrow, THEN I'll post it.

ibm.pc/hardware #2103, from drifkind, Wed Jan 7 19:14:04 1987. A comment to message 2092.

Okay, here goes. This worked on a true-blue PC, should work on many clone clones, but otherwise I wouldn't care to guarantee it. Hint: If there is an electrolytic capacitor near the 8284 IC on your motherboard, it probably WON'T work.

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But I'm getting ahead of myself. First, find the 8284 IC on the motherboard. It should be very near the 8088, and should be socketed. Connect a .1 microfarad capacitor in parallel with a 10K ohm resistor, and connect one lead of this assembly to pin 9 of the 8284. One wire to your normally-open pushbutton switch goes to the other lead of the cap/resistor combination, and the other wire goes to pin 11 of the 8284. The best way to do this is to buy an 18-pin socket, connect the components and wires to it, insert it in the 8284's socket and insert the 8284 into it. Voila! Instant reset.

The cap prevents the RES/ input from staying low long enough to "de-refresh" the memory. This circuit relies on the IBM's power supply providing a "power good" signal with minimal source capacity, which can be "glitched" low. If your clone has an RC circuit to delay reset after power-up, the modification gets a bit more complicated.

ibm.pc/hardware #2105, from barryn, Wed Jan 7 19:47:15 1987. A comment to message 2103.

I *knew* I should have majored in Electrical Engineering instead of Philosophy when I was in college! < grin >

Okay, I think I get the idea. One question, though (to keep me out of trouble. . .): by connecting the capacitor and resistor in parallel, you *do* mean that they should both be connected to the same pins (9 <- -> 11 on the 8284)? Right?

ibm.pc/hardware #2106, from ronlepine (Ronald Lepine), Wed Jan 7 20:35:11 1987. A comment to message 2105.

```
_____cap_____
9-----<____resistor____>-----switch-----11
```

is the way I read it. With 9 and 11 being the pins.

ibm.pc/hardware #2107, from barryn, Wed Jan 7 20:50:04 1987. A comment to message 2106.

Thanks. Since I can use a separate socket sandwiched in between the chip and the present socket, this looks like an even "safer" modification to do than the NMI pushbutton I did about a year ago.

Okay, here's another question: What happens when the reset button is pushed? Is there any kind of debugging aid/tool (software-wise) that I can "attach" to it?

ibm.pc/hardware #2113, from drifkind, Wed Jan 7 22:48:40 1987. A comment to message 2107.

What happens when the reset button is pressed is exactly what happens when the power is turned on, and you can't change that without changing the ROMs. But, you say, how can I (this is you talking, remember) skip the POST if it's the same as power-on? It's that "1234" flag at 40:72 (or 0:472) - 1234h is an unlikely value to find in uninitialized memory after power-up, so the ROM uses that to tell the difference between power-on reset and a three-key reset.

ibm.pc/hardware #2114, from barryn, Wed Jan 7 23:00:21 1987. A comment to message 2113.

Skipping the POST is no big deal. My AT clone goes through it pretty quickly. No, what I meant was that I want the ability to hit the switch and go into a DEBUG.COM-type environment so I can find out why I had to hit the switch.

I think what I'll do (when I get a little time. . .) is to write a small shell that loads DEBUG.COM and makes it resident (I'll record the address/entry point for when I need it). I'll put this in my AUTOEXEC.BAT and, if I ever have to hit the switch,

I'll use the resident Debug program to examine the "corpse" of the program that caused the lock-up.

ibm.pc/hardware #2115, from drifkind, Wed Jan 7 23:29:26 1987. A comment to message 2114.

Did you say. . . AT? The AT uses an 82284 clock generator instead of the 8284 in the PC. Its pinout is different, but the two important pins, 9 and 11 (ground and RES/), are still the same. I would GUESS you could do the same thing, but I can't prove it. Let me know if you try. Yes, you do want to skip the POST; otherwise the memory test will wipe out that corpse you were trying to autopsy.

ibm.pc/hardware #2119, from barryn, Thu Jan 8 05:32:32 1987. A comment to message 2115.

Yes, I realized I had an 82284, but that pins 9 and 11 were still the ones I wanted (I looked it up). Thanks!

ibm.pc/hardware #2117, from geary, Thu Jan 8 03:29:41 1987. A comment to message 2107.

The reset switch pulls down the "power good" line from the power supply. This does a hard reset; it would be pretty difficult to attach any kind of software debugging tool to that.

ibm.pc/hardware #2111, from drifkind, Wed Jan 7 22:33:23 1987. A comment to message 2106.

You got it. Sorry, I wasn't explaining things too well when I wrote that. It would be, like, a rully good idea to mount that switch where you won't hit it accidentally.

ibm.pc/hardware #2122, from a.lane (Alex Lane), Thu Jan 8 20:47:25 1987. A comment to message 2106.

What reason for a single-pole single-throw momentary switch (particularly the momentary part)? I found out the hard way that it's important after wiring a C-64 in similar fashion to add reset capability; I used a regular switch, thinking it shouldn't matter how long the line is grounded, as long as it's not forever. I burned the CPU out in short order, according to the repair shop. I'm not much of a hardware guru, so I ask: Why?

ibm.pc/hardware #2123, from petewhite, Thu Jan 8 21:39:20 1987. A comment to message 2122.

Depending on the circuit, any time you short a signal to ground, you create a current draw. Holding that connection for any length of time can create heat. NOTHING likes a lot of heat in a computer. It's like the idiots who insist on putting a fuse in to protect a transistor. Almost always the transistor protects the fuse quite nicely.

ibm.pc/hardware #2124, from drifkind, Thu Jan 8 22:27:00 1987. A comment to message 2122.

A momentary switch is not "momentary" in any real sense; it just means the switch is closed as long as you hold the button down. The capacitor is in that reset circuit to make the connection really momentary; it effectively acts as a short circuit for a few milliseconds or so, then turns into an open circuit until the switch is released. Can't say why you would have a problem with a C-64, except that I've heard stories that it doesn't respond to a reset in any ordinary fashion. But that's another tale. . .

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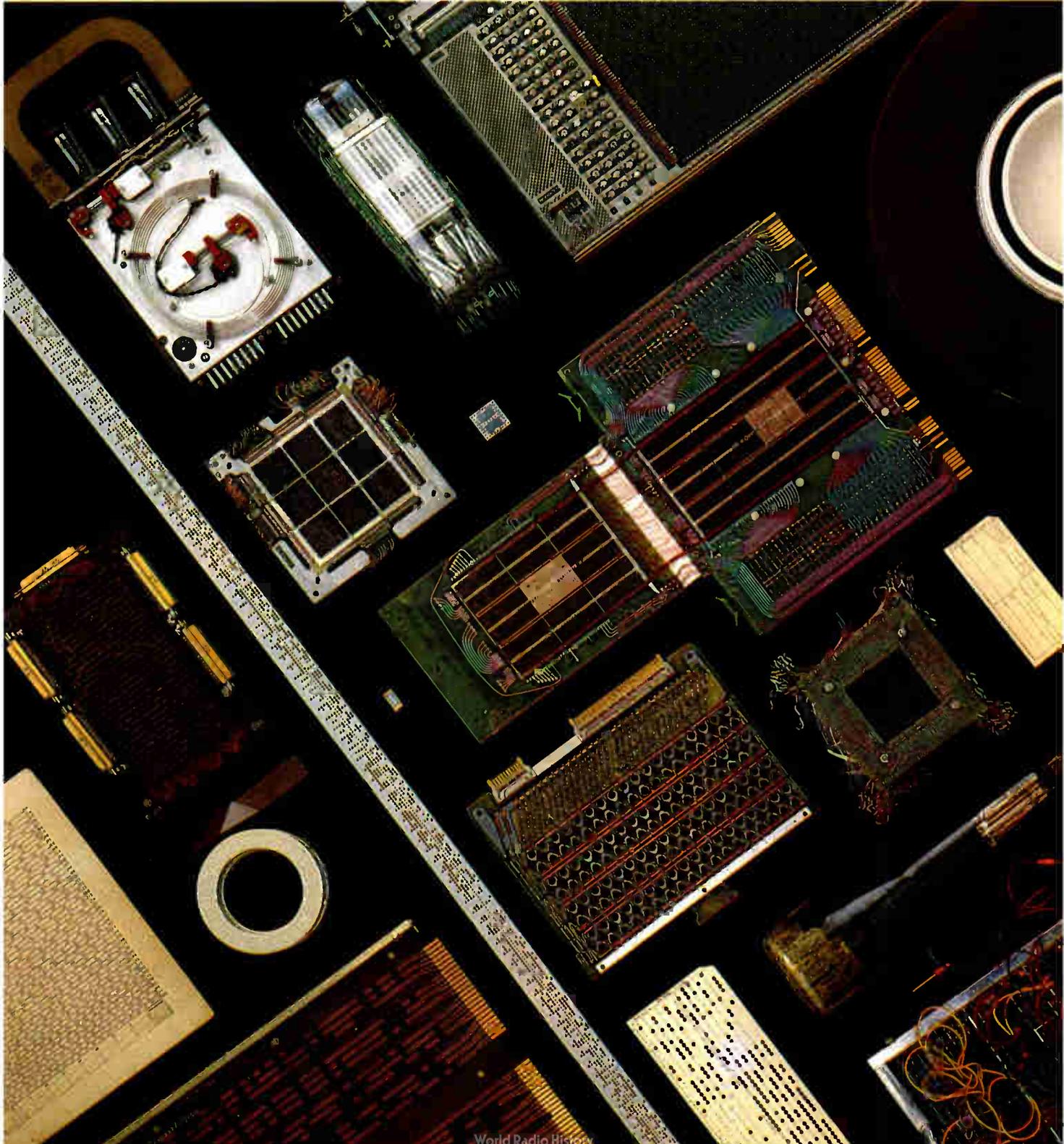
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PATHS AND TROJAN HORSES

ibm.pc/software #2019, from mhagberg (Michael Hagberg), Sun Jan 11 19:52:44 1987.

Does anyone know of a program to add or remove directories from the PATH command? If not, it might be a good program for some guru to write. Commands like "Path +c: \ dir" would add to the existing path and "Path -c: \ dir" would remove from the existing path.

I have a turbo XT and would like a program to tell it to enter the turbo mode or return to the normal mode. The keyboard command is (Alt)(Ctrl)'-' to change modes. I tried the Key-fake command but don't know the ASCII code for the '-' on the cursor pad, when (Alt)(Ctrl) is pressed. Can anyone help?

ibm.pc/software #2021, from Ikolakowski, Sun Jan 11 20:33:09 1987. A comment to message 2019.

You can make a simple batch file to add directories to a path. . . it looks like this

```
path = %PATH%%1
```

Now for some removing of directories. . . .

ibm.pc/software #2023, from bbrown (Bob Brown), Sun Jan 11 22:13:32 1987. A comment to message 2021.

> batch file to add to PATH. . .

Ahhh. . . but on a *real* operating system, you'd have an AFTER= operand to put the added directory in the right place, like Datapoint's RMS does. (RMS is the best small-computer operating system going. Too bad so few people can use it.)

Lessee now . . . on MS-DOS you'd want it to be BEFORE=, and put it at the end, if not specified. In RMS, the user's working directory is always first so ya can set up defaults, which makes AFTER make sense.

ibm.pc/software #2025, from mmallett (Mark Mallett), Mon Jan 12 00:28:00 1987. A comment to message 2023.

Having the current working directory first in the path (or anywhere in the path, for that matter) is an excellent invitation for Trojan horse programs especially in multi-user environments, as UNIX folks all know.

ibm.pc/software #2030, from bbrown, Mon Jan 12 21:25:53 1987. A comment to message 2025.

> having the current working directory first in the path
> is an invitation for Trojan horse programs. . .

MS-DOS does that by default, doesn't it? First search the current directory, then start on the "explicit" path, I think. RMS, of which I spoke highly, has each user's *private* working directory first. I'm interested in the "Trojan horse" aspect of this discussion. For the reason given above, I think it's probably okay to discuss it here. I s'pose a program could "deposit" a load module with the same name as a system command in the current directory, and that load module would be executed the next time a user tried to invoke the system command. Since the MS-DOS path is accessible to any program, a Trojan horse could deposit its fake command in the directory at the head of the path. In a *good* operating system, the privileges a program has depend, in some measure, upon the directory from which it is run, so only the contents of the user's directory and any with lower privileges (which should be none) are in danger. Have I guessed right, or are there other ways to use PATH to open doors for Trojan horses?

ibm.pc/software #2032, from mmallett, Mon Jan 12 22:33:42 1987. A comment to message 2030.

Yes, the "with the same name as a system command in the current directory" is the sort of thing I was referring to. I suppose it doesn't matter too much in single-user systems, but it is something to keep in mind anyway, just to condition yourself. A typical scenario might be something like: User writes a program called "ls" (or "dir") and puts it in his home directory. He invites another user on the system to connect to his directory and try to do a directory (via "ls" on UNIX, or "dir", say). If the other user has the current working directory in his path, and especially if it is FIRST in the path so that it prevents the normal system utilities from being found before that one, the program is run from the offender's area and may access private files in the second person's area. If that second person has some sort of privileges that can be invoked (if there are process-oriented privs as in VMS and other systems), the Trojan program may be able to access otherwise protected system areas.

It may not be something that you have to worry about. Or is it? I probably shouldn't have brought it up, but I always react negatively to a suggestion of having the working directory first in a path. Personally, I leave the working directory out of the path entirely, and if I want to run some program in nonstandard ("system," or "bin," or what have you) areas, I reference them explicitly (either by alias or full specification). It's something to worry about if you are in multi-user environments, or if any hands other than your own are ever on your computer, literally or figuratively.

ibm.pc/software #2033, from skluger (Sigi Kluger), Mon Jan 12 22:45:01 1987. A comment to message 2032.

It would also cut down on disk search time if one could disable local search under MS-DOS.

ibm.pc/software #2034, from bbrown, Mon Jan 12 22:52:04 1987. A comment to message 2032.

> Trojan horse programs. . .

Ummm. . . I see. Under MS-DOS you simply have to trust those who give you software to try out. Or set up *very* controlled conditions for testing it. The Trojan-horse-in-the-path problem is not serious under RMS, but that's so far off the topic I'll leave it. Send mail if you want info.

ibm.pc/software #2027, from sjg (Steve Glynn), Mon Jan 12 12:08:46 1987. A comment to message 2019.

Alt-Ctrl -

The problem is that there is no ASCII code for the combination you need. There is only one program I know of that could hit that combination for you, but it's too big and expensive for that task alone. (See Jan 87 BYTE UK.)

I suggest you trace through your BIOS to find what Alt-Ctrl does. It will probably just OUT to a port; you can then do that from Turbo or BASIC or whatever.

ibm.pc/software #2028, from dmick (Dan Mick), Mon Jan 12 12:33:50 1987. A comment to message 2019.

I've seen (and have) a shareware program called "EE," for Environment Editor. It would sometimes allow such changes to the environment, but you had to be careful not to . . . something. I suspect it crashed when you went beyond

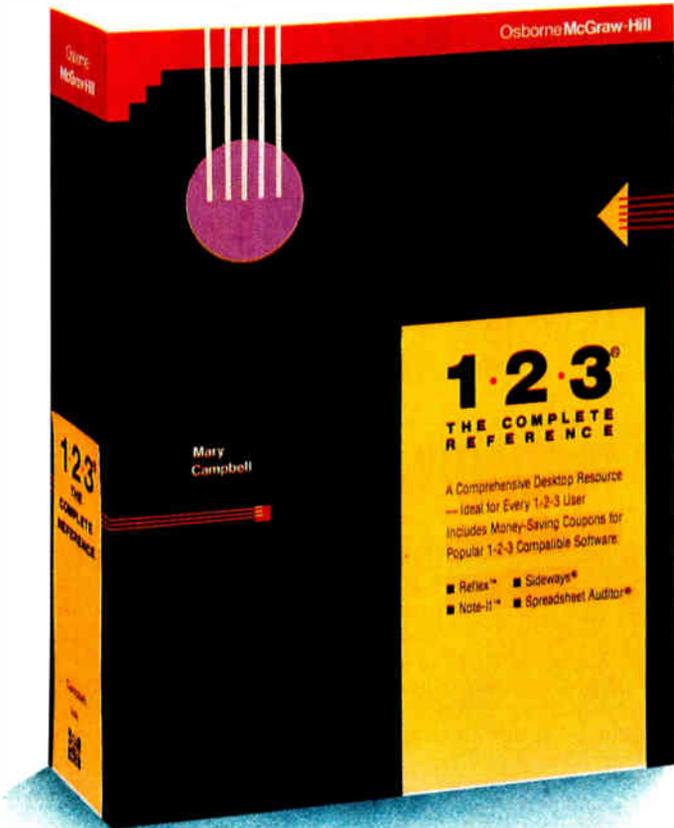
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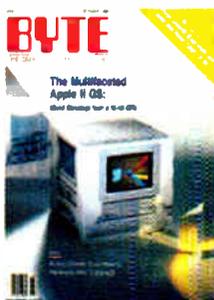
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the allocated space, for lack of being able to find out how much environment space was available, and lack (under DOS 2.x) of a way to expand it nicely. But I've used it, like you say, on occasion.

ibm.pc/software #2031, from jfleming, Mon Jan 12 21:29:28 1987. A comment to message 2019.

Here is a Debug script to create programs called SLOW.COM and FAST.COM. To use them, either:

1. Use your word processor or other program to make a file containing ONLY the stuff between the dashed lines, but not including the dashed lines. Call it (say) FASTSLOW.SCR. Then, at the DOS prompt with DEBUG.EXE accessible in the default directory or on the path,

```
DEBUG < FASTSLOW.SCR
```

will create the appropriate programs.

2. At the DOS prompt, type DEBUG and enter the lines below by hand.

NOTE that the blank lines (only a RETURN) are important!

```
nfast.com
acs:0100
IN AL,61
OR AL,04
OUT 61,AL
INT 20
```

```
r cx
0008
```

```
w
nslow.com
acs:0100
IN AL,61
AND AL,FB
OUT 61,AL
INT 20
```

```
r cx
0008
w
q
```

This works on all clones that I have seen/heard of that use <Ctrl> <Alt> <grey minus> to switch speeds. Some have pins on the motherboard to enable/disable turbo; I have found that these can be used to install a hardware fast/slow switch (which works only in fast mode), at least on mine.

PASCAL

Pascal coverage this month includes discussion of Digital Research's Pascal dialect and techniques for transferring files.

A PASCAL-DIALECT DIALOGUE

pascal/other #154, from pschauble (Paul Schauble), Thu Jan 1 22:44:33 1987.

I've recently been handed a set of programs written in MT Pascal that run on MS-DOS. I need to keep these running until they can be rewritten in another language. The problem is that the manuals are useless; Digital Research no longer supports the package, and the only thing I could get from the people who

continued

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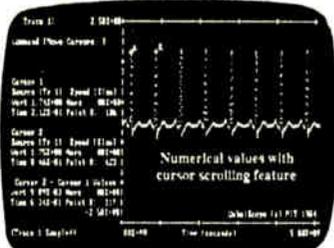
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supposedly do is a list of bug fixes in the last five revisions. Is there anyone here who is knowledgeable about this package who might offer a bit of assistance?

pascal/other #155, from jcourtney (John Courtney), Sat Jan 3 13:30:38 1987. A comment to message 154.

Pascal MT+/86 assistance? I might be able to help a little. At work we are using MT+ in an embedded real-time system on both 8086 and Z80 hardware (obviously different compilers). I just put a note in the microsoft/languages topic about using MS-Pascal in a ROM-based system, but got no for an answer. The bottom line for you is probably to run, do not walk, to the store and buy any Pascal system except MT+. Unfortunately, it looks like we are stuck with it until we can junk the current hardware and start from scratch. (Anyone know of a Pascal-to-Modula translator out there? I guess I should ask that elsewhere. . . .)

pascal/other #156, from pschauble, Sat Jan 3 18:41:45 1987. A comment to message 155.

I sympathize. I seem to be in the same situation. The program I am contending with is scheduled to be rewritten, but I have to get one more revision out of the MT version.

My immediate question is this: This program is overlaid using the MT overlay system. Am I correct in assuming that the base of the overlay area /O1:xxxx plus the code size of the largest overlay cannot exceed the maximum code segment size of the root /R:xxxx? Actually, the manual notes that overlays are handled in 128-byte units, so that the overlay area /O1 must be 128 bytes above the end of root code and the /R address must be 128 bytes above the end of the overlay. Correct?

pascal/other #157, from mpack (Micropack Ltd.), Sat Jan 3 20:33:09 1987. A comment to message 155.

I have a Pascal-to-Modula translator, which I am in the process of getting someone to market for me. It handles Turbo or UCSD Pascal (via a command-line option). I would be quite interested if you want to give it a thorough testing for me. Logitech sells a Modula-2 compiler that can produce ROM-able code (last I heard). Let me know if you are interested. Don Milne.

pascal/other #158, from rbrukardt (Randall Brukardt), Sat Jan 3 20:43:15 1987. A comment to message 155.

I don't know of a good Pascal-to-Modula translator, but I do know of a good Pascal-to-Ada translator. Of course, since we sell it. . . . You should pay a visit to the PasTran topic of the "Janus.ada" conference. You can talk to one of the authors of it, dstock (Daniel Stock).

PASCAL FILE TRANSFER

pascal/feedback #186, from plennon (Paul Lennon), Mon Nov 17 23:09:34 1986.

I have a rather awkward problem to solve that involves the passage of an unknown file variable type from one program/procedure to another. You see, the company I work for uses several different types of computers for program development. Each of these computers uses its own "enhanced" form of standard Pascal. What I would like to do is develop a set of standard libraries that would perform some of these enhancements on a less endowed system. For example, in my department, we do extensive database-development work on an Apollo Token Ring network using Domain Pascal. We also use several IBM PC XT's running Turbo.

I am currently developing a collection of routines that will perform operations that are common to Turbo on the Apollo. Presently I have completed a set of string-handling routines

that work satisfactorily; the next problem is file I/O. The Apollo opens/assigns a file with an OPEN command like so:

```
OPEN(filevar, pathname, history, error__status);
history = "NEW", "OLD", "UNKNOWN"
```

Turbo uses the ASSIGN statement:

```
ASSIGN(filevar, pathname);
```

The problem is that in a truly functional procedure I will not know what file type "filevar" is. In most programs the programmer has a good idea what type of files he is working with; in this case I won't.

My question is this: Is there a generic way of transferring an unknown file type from one procedure to another or is it a function of the operating system/compiler? I am particularly interested in porting some Turbo-developed software over to the Apollo. Sure, I could use a word processor and manually rewrite the I/O calls, but the source code is about 2 inches thick!

I'd really appreciate any insight that any of you can provide. I'll be happy to provide more specific details.

pascal/feedback #187, from dmick (Dan Mick), Mon Nov 17 23:14:33 1986. A comment to message 186.

Well, you can always open it as a "file of byte" and read enough to determine the real structure, then close it and reopen with the correct structure. There's also the "file" type in Turbo, which opens for block I/O (i.e., no implicit structure). Both, I am led to believe, have similar performance, since either Turbo or DOS does blocking on the "file of byte" to avoid one-byte reads, anyway. But either of these allow you to open the file regardless of its type.

pascal/feedback #188, from avincent (Andrew Vincent), Tue Nov 18 05:47:38 1986. A comment to message 187.

Look into using the UNIV prefix to parameters, if you are using Apollo Pascal. Non-standard, but it may do what you want.

pascal/feedback #189, from mpack, Tue Nov 18 14:38:14 1986. A comment to message 186.

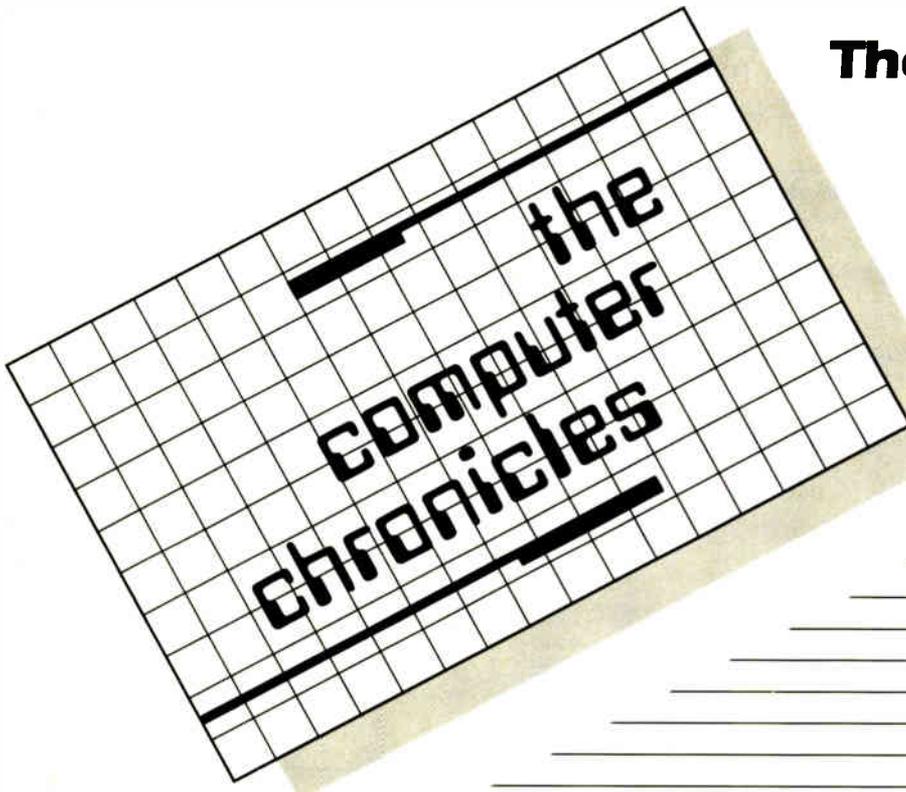
As I understand your problem, you have run into the differences between file-handling routines in different implementations of Pascal. You want to develop a set of portable routines of your own, but don't know how to write a set of generic routines that will handle all file types (including structured files).

This requires that you be able to pass an untyped parameter to a Pascal procedure. Unfortunately this is not possible in ISO standard or J&W standard Pascal. It is possible in UCSD Pascal (prior to version IV.2) only for machine-code (external) procedures. In fact, the only Pascals that make it easy (that I know of) are Turbo Pascal (easiest) and UCSD Pascal IV.2 (messy, but it can be done).

You should check and see if such a thing is possible in Domain Pascal. If it is, you should check out atari.st/listings, where I posted a module called FileIO, which is a file-handling module such as you would need. It is written in Modula-2, but should be easily converted to Pascal, providing that the Pascal implementations are good enough (Turbo is).

If you find that you cannot have untyped parameters, it may still be possible using various standard tricks. So if you have no joy, let me know and I will expand on these. ■

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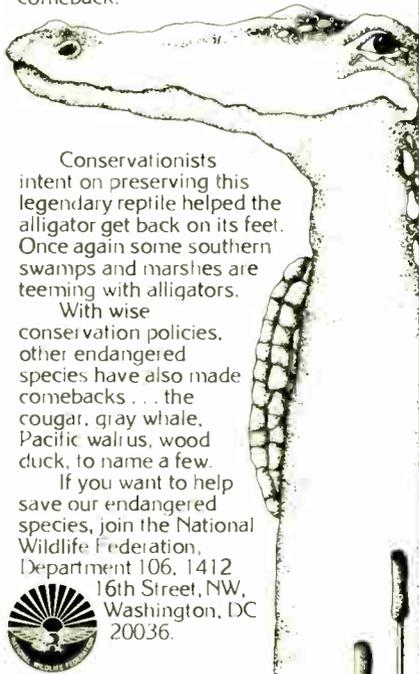
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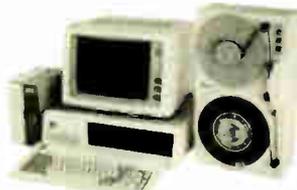
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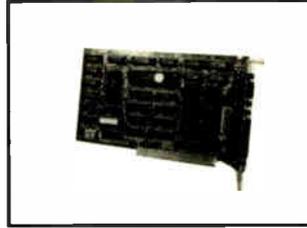
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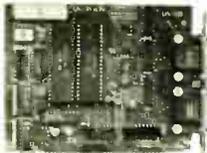
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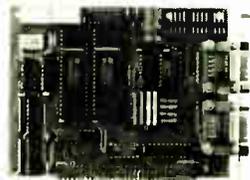
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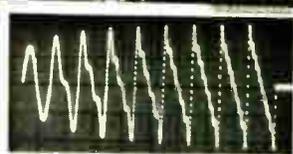
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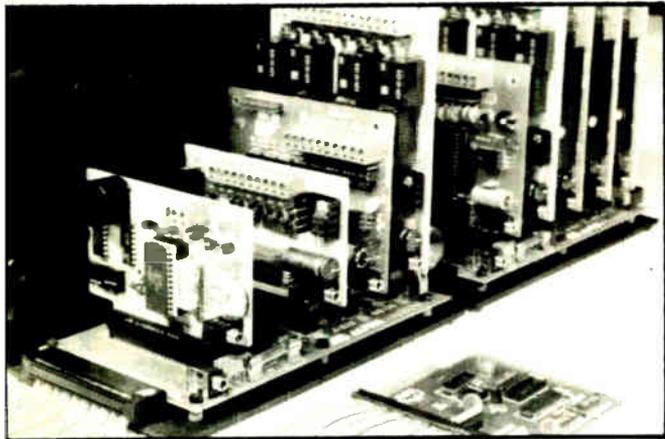
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Inquiry 142

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NEW



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The A-BUS is backed by Alpha's continuing support (our 11th year, 50000 customers in over 60 countries).

The complete set of A-BUS User's Manuals is available for \$10.

About the A-BUS:

- All the A-BUS cards are very easy to use with any language that can read or write to a Port or Memory. In BASIC, use INP and OUT (or PEEK and POKE with Apples and Tandy Color Computers)
- They are all compatible with each other. You can mix and match up to 25 cards to fit your application. Card addresses are easily set with jumpers.
- A-BUS cards are shipped with power supplies (except PD-123) and detailed manuals (including schematics and programming examples).

Relay Card

RE-140: \$129

Includes eight industrial relays (3 amp contacts, SPST) individually controlled and latched. 8 LED's show status. Easy to use (OUT or POKE in BASIC). Card address is jumper selectable.

Reed Relay Card

RE-156: \$99

Same features as above, but uses 8 Reed Relays to switch low level signals (20mA max). Use as a channel selector, solid state relay driver, etc.

Analog Input Card

AD-142: \$129

Eight analog inputs. 0 to +5V range can be expanded to 100V by adding a resistor. 8 bit resolution (20mV). Conversion time 120us. Perfect to measure voltage, temperature, light levels, pressure, etc. Very easy to use.

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Digital Input Card

IN-141: \$59

The eight inputs are optically isolated, so it's safe and easy to connect any "on/off" devices, such as switches, thermostats, alarm loops, etc. to your computer. To read the eight inputs, simply use BASIC INP (or PEEK)

24 Line TTL I/O

DG-148: \$65

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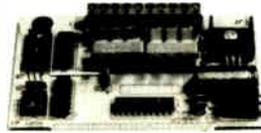
PH-145: \$79

Each tone is converted into a number which is stored on the board. Simply read the number with INP or POKE. Use for remote control projects, etc.

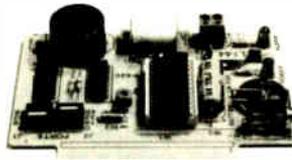
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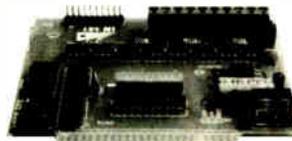
ST-143



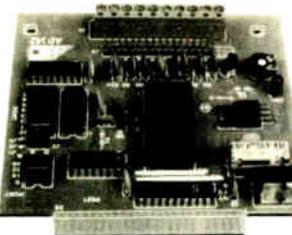
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RE-140



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AO-142

Smart Stepper Controller SC-149: \$299

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Remote Control Keypad Option RC-121: \$49

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TRS-80 Model 102. 200 Plugs into 40 pin "system bus"	AR-136 \$69
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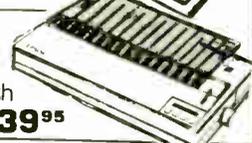
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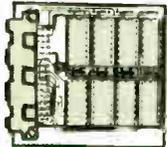
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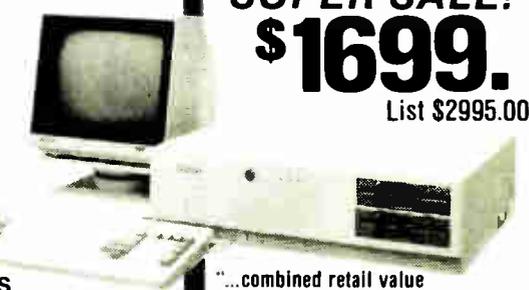
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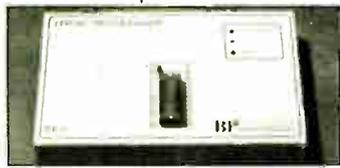
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Coffle BBS (338)
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Lotus ASCII utilities (813): Allows all codes and embedded printer controls, etc. Requires Lotus 1-2-3
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Lotus Financial Utilities #2 (822): Calculate proforma income statements, track your income and more. Requires Lotus 1-2-3
1-2-3 (824) Cash flow ledger
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Mapmaker (727): Helps you draw maps. It requires monochrome and color monitors and cards
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Kraft Paint (731): This graphics program requires a joystick
Pictures (733): These can be displayed on your screen or your printer, includes Snoopy calendar, pinups, more
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dBASE III routines (1614): Over 60 dBASE III routines (Requires dBASE III)
Global Concordance (1615): Lists all global symbols in your applications
dBASE II programs (1616): For accounting, mail labels, form letters, and more (Requires dBASE II)
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MUMPS (1617): Data manager runs under MUMPS (see disk 1609 for MUMPS)
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More DOS utilities (1912): Includes Other, Mjog, Grep, and many more
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FontGen (2917): Create fonts for Epson FX, IBM, Proprietary, or compatible printers
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Z80MU 3.1 (3438): Run Z80 programs under PC DOS
EGAUtilities (3439): Palette-setting, 43 line mode patches, NANSI.SYS Commando (3440): DOS file handler. Can manipulate squeezed files and files in .LBR format
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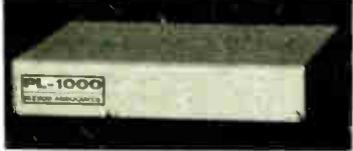
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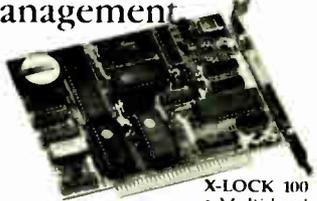
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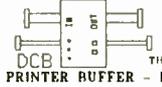
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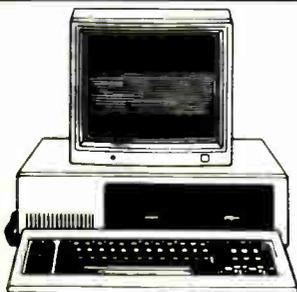
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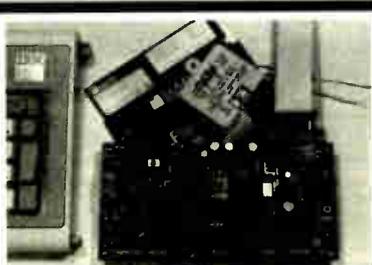
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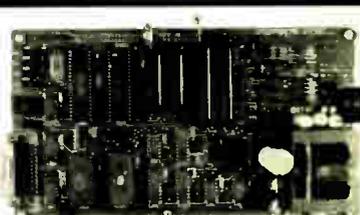
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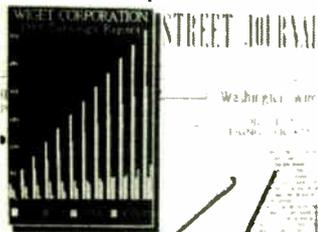
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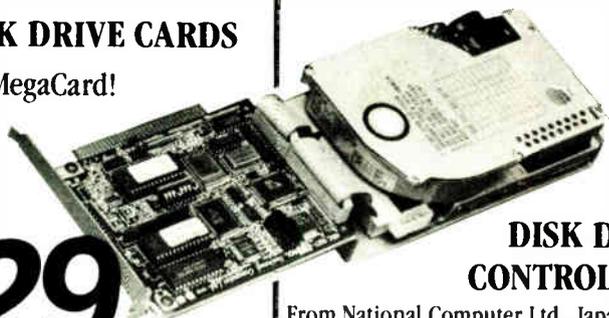
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#A



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#B

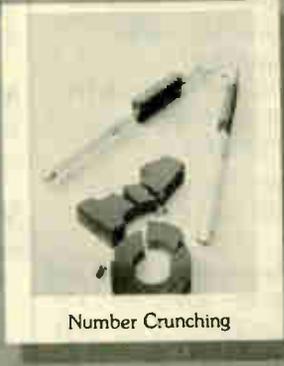


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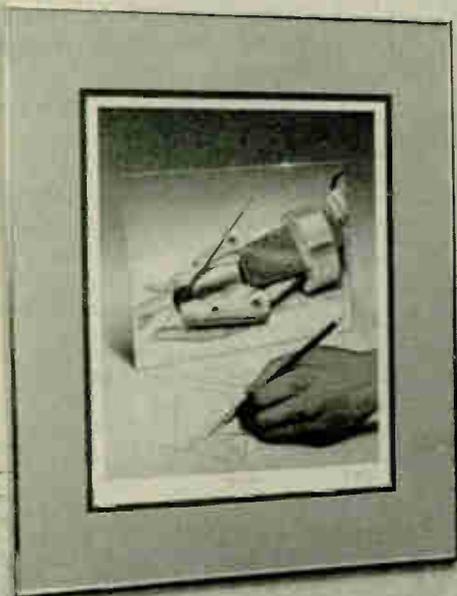
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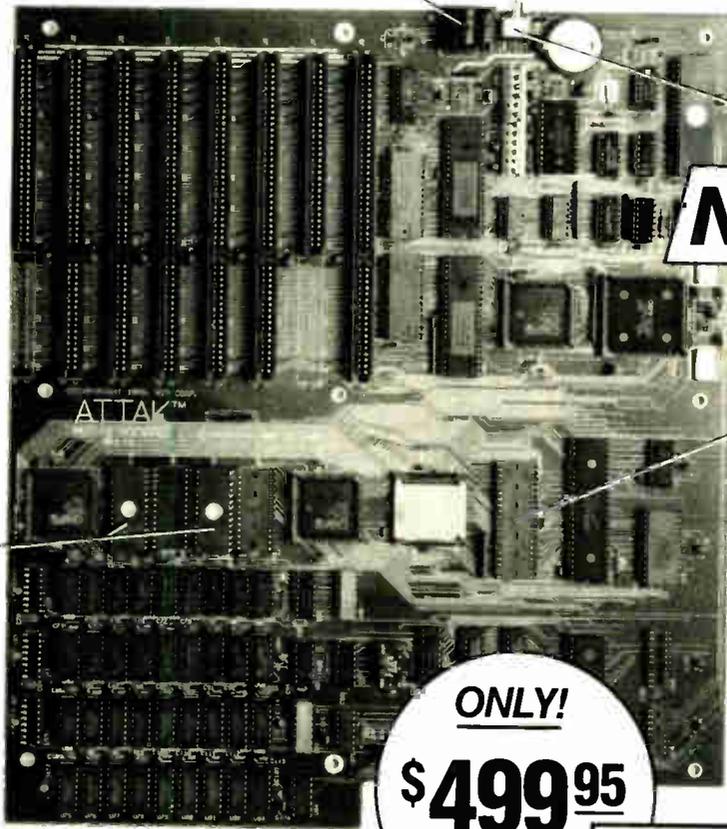
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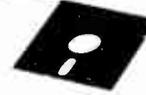
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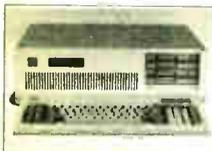
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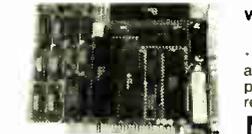
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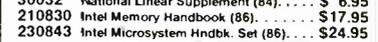
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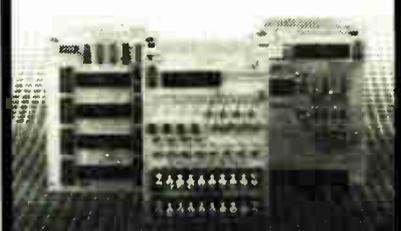
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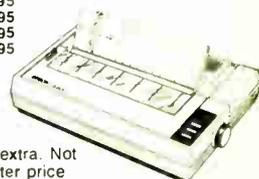
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The 410 color plotter will connect to the serial port of virtually any micro-computer. Simple ASCII commands direct one of the four color pens to draw circles, arcs or ellipses on paper or transparency material up to 11 by 17 inches. The plotter is capable of producing the full upper and lower case alphabet along with seven international character sets. Text can be printed horizontal, vertical or diagonal in sizes from 1/16 to 6 inches, slanted forward or backward to 85 degrees.

Enlargements or reductions are achieved through elaborate firmware. Pen travel is four inches per second with .004" pen resolution. Standard pens are available in an assortment of 32 different colors and widths.

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OTHER PLOTTERS AVAILABLE:

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Qume 142 PC Compatible
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Quantity Two

These Qume double sided PC compatible drives bear the IBM logo. The drive was manufactured for IBM for use in the recently discontinued PC Junior computer. We have purchased a large quantity of these drives and are currently offering them in sets of two for only \$65 each.



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\$115

The Panasonic 475 is jumper selectable between 96 TPI format and 1.2 Megabyte as used in the IBM/AT computer.

Suggested price of this drive is \$189 but because of unusual buying opportunity, California Digital is able to offer these drives at only \$115 each, quantity two.

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These Fujitsu Daisy Max 830 were manufactured for Motorola's Computer Division. The purchase order was canceled and Fujitsu was forced to liquidate these 80 character per second daisy wheel printers at "fire sale" prices.

Features: bullet proof construction, serial RS-232 interface, Diablo 630 wheels and commands, programmable line spacing in increments of 1/96" and column spacing of 1/120". The printer is also capable of underscoring, bold overprint, shadow print, centers and justifies along with vector plotting. Factory suggested price of the Daisy Max 830 was \$2495, while supplies last California Digital is offering this liquidated special at only \$759. Also available: tractor and sheet feeders.



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was \$3540 now only
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The Bernoulli Box by Iomega, features 10 and 20 megabyte removable cartridges, and delivers reliability, expandability, transportability, security and speed in one versatile subsystem. It lets you transfer megabytes of information safely and swiftly for primary or backup storage. Or combine several software programs onto a single cartridge for easy switching from one to another.

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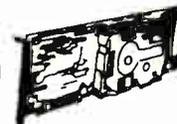


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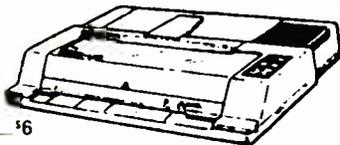
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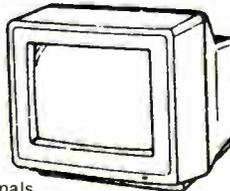
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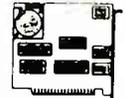
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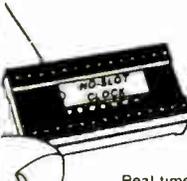
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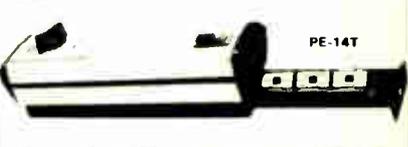
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74LS10	.16
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74LS12	.22
74LS13	.26
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74LS15	.26
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74LS21	.22
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74LS33	.28
74LS37	.26
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74LS47	.75
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74LS75	.29
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74LS107	.34
74LS109	.36
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74LS153	.39
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7430	.19	74166 1.00
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ADC0804	3.49	8T27 1.29
ADC0809	4.49	8T95 .89
ADC0816	14.95	8T96 .89
ADC0817	9.95	8T97 .59
ADC0831	8.95	8T98 .89
DAC0800	4.49	DM8131 2.95
DAC0806	1.95	DP8304 2.29
DAC0808	2.95	D8833 2.25
DAC1020	8.25	D8835 1.99
DAC1022	5.95	D8836 .99
MC1408L8	2.95	D8837 1.65

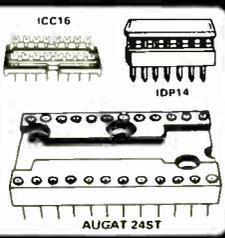
IC SOCKETS		
8 PIN ST	.11	100-
14 PIN ST	.11	.09
16 PIN ST	.12	.10
18 PIN ST	.15	.13
20 PIN ST	.18	.15
22 PIN ST	.15	.12
24 PIN ST	.20	.15
28 PIN ST	.22	.16
40 PIN ST	.30	.22
64 PIN ST	1.95	1.49
ST SOLDER TAIL		
8 PIN WW	.59	.69
14 PIN WW	.69	.52
16 PIN WW	.65	.58
18 PIN WW	.99	.90
20 PIN WW	1.09	.98
22 PIN WW	1.39	1.28
24 PIN WW	1.49	1.35
28 PIN WW	1.69	1.49
40 PIN WW	1.99	1.80
WW-WIREWRAP		
16 PIN ZIF	4.95	CALL
24 PIN ZIF	5.95	CALL
28 PIN ZIF	6.95	CALL
40 PIN ZIF	9.95	CALL
ZIF-TEXT TOOL (ZERO INSERTION FORCE)		

EDGECARD CONNECTORS		
100 PIN ST	S-100	1.25 3.95
100 PIN WW	S-100	1.25 4.95
62 PIN ST	IBM PC	1.00 1.95
50 PIN ST	APPLE	1.00 2.95
44 PIN ST	STD	1.56 1.95
44 PIN WW	STD	1.56 4.95

36 PIN CENTRONICS		
MALE		
IDCEN36	RIBBON CABLE	6.95
CEN36	SOLDER CUP	4.95
FEMALE		
IDCEN36/F	RIBBON CABLE	7.95
CEN36C	RT ANGLE PC MOUNT	4.95

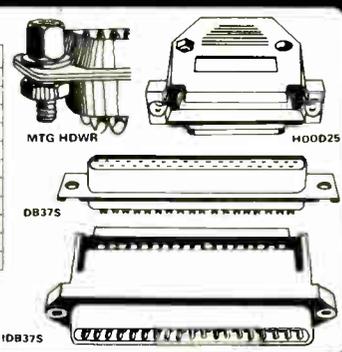
INTERSIL		
ICL7106	9.95	
ICL7107	12.95	
ICL7660	2.95	
ICL8038	4.95	
ICM7207A	5.95	
ICM7208	15.95	

DIP CONNECTORS										
DESCRIPTION	ORDER BY	CONTACTS								
		8	14	16	18	20	22	24	28	40
HIGH RELIABILITY TOOLED ST IC SOCKETS	AUGATxxST	.62	.79	.89	1.09	1.29	1.39	1.49	1.69	2.49
HIGH RELIABILITY TOOLED WW IC SOCKETS	AUGATxxWW	1.30	1.80	2.10	2.40	2.50	2.90	3.15	3.70	5.40
COMPONENT CARRIES (DIP HEADERS)	ICCxx	.49	.59	.69	.99	.99	.99	.99	1.09	1.49
RIBBON CABLE DIP PLUGS (IDC)	IDPxx95	.95	1.75	...	2.95



DIODES/OPTO/TRANSISTORS		
1N751	.25	4N26 .69
1N759	.25	4N27 .69
1N4148	25 1.00	4N28 .69
1N4004	10 1.00	4N30 .69
1N5402	.25	4N37 1.19
KBPO2	.55	MCT-2 .59
KB08A	.95	MCT-6 1.29
MDA990-2	.35	TIL-111 .99
N2222	.25	2N3906 .10
PN2222	.10	2N4401 .25
2N2905	.50	2N4402 .25
2N2907	.25	2N4403 .25
2N3055	.79	2N6405 1.75
2N3904	.10	TIP31 .49

D-SUBMINIATURE									
DESCRIPTION	ORDER BY	CONTACTS							
		9	15	19	25	37	50		
SOLDER CUP	MALE DBxxP	.82	.90	1.25	1.25	1.80	3.48		
	FEMALE DBxxS	.95	1.15	1.50	1.50	2.35	4.32		
RIGHT ANGLE PC SOLDER	MALE DBxxPR	1.20	1.49	...	1.95	2.65	...		
	FEMALE DBxxSR	1.25	1.55	...	2.00	2.79	...		
WIRE WRAP	MALE DBxxPWW	1.69	2.56	...	3.89	5.60	...		
	FEMALE DBxxSWW	2.76	4.27	...	6.84	9.95	...		
IDC RIBBON CABLE	MALE IDBxxP	2.70	2.95	...	3.98	5.70	...		
	FEMALE IDBxxS	2.92	3.20	...	4.33	6.76	...		
HOODS	METAL MHOODxx	1.25	1.25	1.30	1.30		
	GREY HOODxx	.65	.6565	.75	.95		

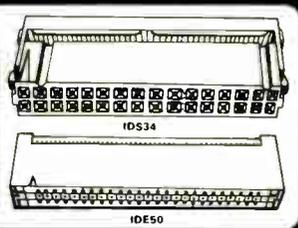


LED DISPLAYS		
FND-357(359)	COM CATHODE .362"	1.25
FND-500(503)	COM CATHODE .5"	1.49
FND-507(510)	COM ANODE .5"	1.49
MAN-72	COM ANODE .3"	.99
MAN-74	COM CATHODE .3"	.99
MAN-8940	COM CATHODE .8"	1.99
TIL-313	COM CATHODE .3"	.45
TIL-311	4x7 HEX W/ LOGIC .270"	9.95

DIFFUSED LEDS		
JUMBO RED	T1 1/4	.10 .09
JUMBO GREEN	T1 1/4	.14 .12
JUMBO YELLOW	T1 1/4	.14 .12
MOUNTING HDW	T1 1/4	.10 .09
MINI RED	T1	.10 .09

ORDERING INSTRUCTIONS: INSERT THE NUMBER OF CONTACTS IN THE POSITION MARKED 'x' OF THE ORDER BY PART NUMBER LISTED
EXAMPLE: A 15 PIN RIGHT ANGLE MALE PC SOLDER WOULD BE DB15PR
MOUNTING HARDWARE \$1.00

IDC CONNECTORS							
DESCRIPTION	ORDER BY	CONTACTS					
		10	20	26	34	40	50
SOLDER HEADER	IDHxxS	.82	1.29	1.68	2.20	2.58	3.24
RIGHT ANGLE SOLDER HEADER	IDHxxSR	.85	1.35	1.76	2.31	2.72	3.39
WW HEADER	IDHxxW	1.86	2.98	3.84	4.50	5.28	6.63
RIGHT ANGLE WW HEADER	IDHxxWR	2.05	3.28	4.22	4.45	4.80	7.30
RIBBON HEADER SOCKET	IDSxx	.79	.99	1.39	1.59	1.99	2.25
RIBBON HEADER	IDMxx	...	5.50	6.25	7.00	7.50	8.50
RIBBON EDGE CARD	IDExx	1.75	2.25	2.65	2.75	3.80	3.95



SWITCHES		
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DPDT	MINI-TOGGLE ON ON	1.50

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IBM

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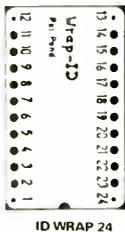
P500-1 BARE - NO FOIL PADS \$15.15
 P500-3 HORIZONTAL BUS \$21.80
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18	IDWRAP 18	5	1.95
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22	IDWRAP 22	5	1.95
24	IDWRAP 24	5	1.95
28	IDWRAP 28	5	1.95
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22	35V .40	10	35V 1.00

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10µf	50V .05	680	50V .05
22	50V .05	.001µf	50V .05
27	50V .05	.0022	50V .05
33	50V .05	.005	50V .05
47	50V .05	.01	50V .07
68	50V .05	.02	50V .07
100	50V .05	.05	50V .07
220	50V .05	.1	12V .10
560	50V .05	1	50V .12

MONOLITHIC

.01µf	50V .14	.1µf	50V .18
.047µf	50V .15	.47µf	50V .25

ELECTROLYTIC

	RADIAL		AXIAL	
1µf	25V .14	1µf	50V .14	
2.2	35V .15	10	50V .16	
4.7	50V .15	22	16V .14	
10	50V .15	47	50V .20	
47	35V .18	100	35V .25	
100	16V .18	220	25V .30	
220	35V .20	470	50V .50	
470	25V .30	1000	16V .60	
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DIP 16 PIN 15 RESISTOR	1.09
DIP 14 PIN 7 RESISTOR	.99
DIP 14 PIN 13 RESISTOR	.99

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WBU-T	1 38 x 6.50"	---	---	1	630	---	6.95
WBU 204 3	3.94 x 8.45"	1	100	2	1260	2	17.95
WBU 204	5.13 x 8.45"	4	400	2	1260	3	24.95
WBU 206	6.88 x 9.06"	5	500	3	1890	4	29.95
WBU-208	8.25 x 9.45"	7	700	4	2520	4	39.95



WBU-208

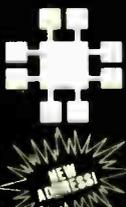
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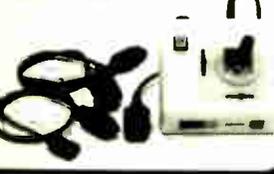


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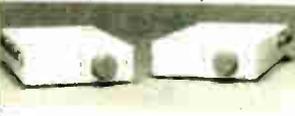
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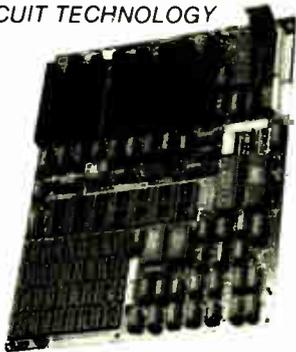
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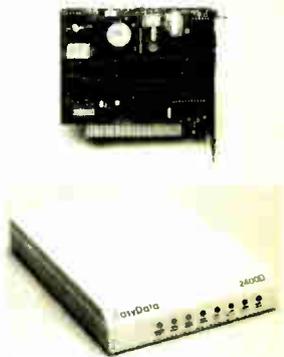
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- CAN RUN WITH COLOR GRAPHICS CARD IN THE SAME SYSTEM



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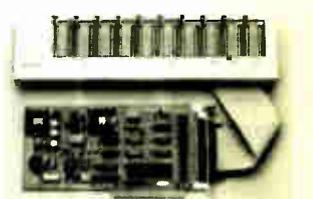
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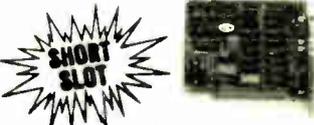
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BOMB

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BYTE's ongoing monitor box (BOMB) lets you rate each article you've read in BYTE as excellent, good, fair, or poor. Each month, you can mail in the BOMB card found at the back of the issue. We tally your votes, total the points, tell you who won, and award the two top-rated nonstaff authors

\$100 and \$50, respectively. An additional \$50 award for quality goes to the nonstaff author with the best average score (total points divided by the number of voters). If you prefer, you can use BIX as your method of voting. We welcome your participation.

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BOMB RESULTS

Winner of January's reader poll is Jerry Pournelle's "A Tale of Two Clones," and in second is the BYTE staff's What's New. Winner of \$100 for being the first nonstaff author to place is Jon C. Snader for his Programming Project, "Look It Up Faster with Hashing."

Next is Microbytes, followed by Vincent J. Coli, who wins \$50 for placing second with his "Introduction to Programmable Array Logic." The \$50 award for quality also goes to Mr. Coli. Congratulations to all.

COMING UP IN BYTE

Theme:

Desktop publishing, whether or not it turns into the next "trend," is technically grounded in the ability of microcomputers to produce finely tuned graphics and text in a variety of configurations and styles. In terms of both hardware and software design, the approaches taken to produce high-quality printed materials are fascinating and fully detailed.

Features:

Ready to go are articles on the Turing machine, the C++ programming language, part 2 of how to build a basic educational robot trainer (BERT), and storing complex, dense designs—like city maps—on CD-ROMs.

Circuit Cellar:

Steve Ciarcia will show how to build a video digitizer.

Programming Project:

Pull-down menus you can write in C.

Programming Insight:

Complex math in Pascal.

Special 68000 Series:

Do-it-yourself construction projects for the Atari 520ST.

Reviews:

A group review of 15 internal modems for the IBM PC and compatibles leads off the section, followed by reviews of the new Compaq Portable and Commodore's updated 64, removable cartridge drives, eight SCSI drives for the Macintosh, three BASICs for the Macintosh, Turbo and Chalcedony Prolog, and OPSS for the PC. Applications package reviews available for publication include Q&A, Lyrix, and Zoomracks.

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Index of companies covered in articles, columns, or news stories in this issue.
Each reference is to the first page of the article or section in which the company name appears.

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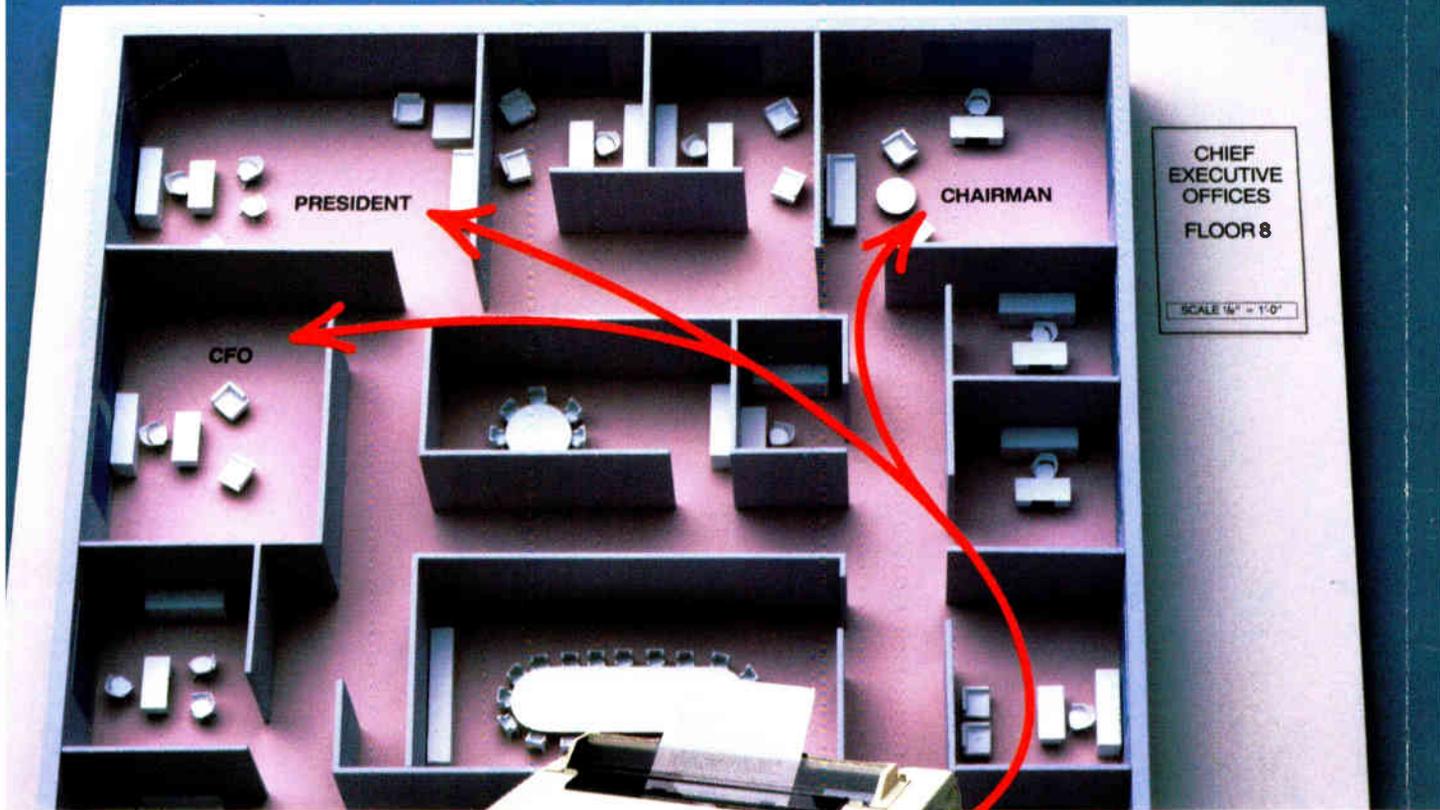
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