

T．M．No．888－2328－001

## Returns And Exchanges

Damaged or undamaged equipment should not be returned unless written approval and a Return Authorization is received from HARRIS CORPORATION, Broadcast Systems Division. Special shipping instructions and coding will be provided to assure proper handling. Complete details regarding circumstances and reasons for return are to be included in the request for return. Custom equipment or special order equipment is not returnable. In those instances where return or exchange of equipment is at the request of the customer, or convenience of the customer, a restocking fee will be charged. All returns will be sent freight prepaid and properly insured by the customer. When communicating with HARRIS CORPORATION, Broadcast Systems Division, specify the HARRIS Order Number or Invoice Number.

## Unpacking

Carefully unpack the equipment and preform a visual inspection to determine that no apparent damage was incurred during shipment. Retain the shipping materials until it has been determined that all received equipment is not damaged. Locate and retain all PACKING CHECK LISTs. Use the PACKING CHECK LIST to help locate and identify any components or assemblies which are removed for shipping and must be reinstalled. Also remove any shipping supports, straps, and packing materials prior to initial turn on.

## Technical Assistance

HARRIS Technical and Troubleshooting assistance is available from HARRIS Field Service during normal business hours (8:00 AM - 5:00 PM Central Time). Emergency service is available 24 hours a day. Telephone 217/222-8200 to contact the Field Service Department or address correspondence to Field Service Department, HARRIS CORPORATION, Broadcast Systems Division, P.O. Box 4290, Quincy, Illinois 62305-4290, USA. The HARRIS factory may also be contacted through a FAX facility (217/221-7096).

## Replaceable Parts Service

Replacement parts are available 24 hours a day, seven days a week from the HARRIS Service Parts Department. Telephone 217/222-8200 to contact the service parts department or address correspondence to Service Parts Department, HARRIS CORPORATION, Broadcast Systems Division, P.O. Box 4290, Quincy, Illinois 62305-4290, USA. The HARRIS factory may also be contacted through a FAX facility (217/221-7096).

NOTE
The \# symbol used in the parts list means used with (e.g. \#C001 = used with C001).

| MANUAL REVISION HISTORY HX 1V EXCITER 988-2328-001 |  |  |  |
| :---: | :---: | :---: | :---: |
| Rev. \# | Date | ECN | Pages Affected: |
| 001-A | May 1992 | 37936 | Replaced Title Page, 5-4 and 5-5 Added MRH-1/MRH-2 |
| 001-B | June 1992 | 37946 | Replaced Title Page, MRH-1/MRH-2 and pages 7-13 to 7-16 |
| 001-C | Apil 1993 | 38515 | Replaced Title Page, MRH-1/MRH-2 and all of Section VII |
| 001-D | Feb. 1994 | 38751 | Replaced Title Page, MRH-1/MRH-2 and all of Section VII |
| 001-E | July 1994 | 39201 | Replaced Title Page, MRH-1/MRH-2 and all of Section VII |
| 001-F | Aug. 1994 | 39224 | Replaced Title Page, MRH-1/MRH-2, and pages iv, v, 4-2, 5-14, 5-16, 5-17, 7-17, 7-18, \& 7-19 |
| 001-G | Oct. 1994 | 39513 | Replaced Title Page, MRH-1/MRH-2, and pages 7-7 \& 7-8 |
| 001-H | April 1995 | 39915 | Replaced Title Page, MRH-1/MRH-2, and page 1-3 |
| 001-J | May 1995 | 39754 | Replaced Title Page, MRH-1/MRH-2, and page 5-7 |
| 001-K | 05-09-95 | 39893 | Replaced Title Page, MRH-1/MRH-2, and pages 7-17 to 7-19 |
| 001-L | 01-09-96 | 39936R | Replaced Title Page, MRH-1/MRH-2, and pages 7-12 to 7-14 |
| 001-M | 02-28-96 | TBD | Replaced Title Page, MRH-1/MRH-2, and page 4-8 |
| $001-\mathrm{N}$ | 10-28-96 | 41553 | Replaced Title Page, MRH-1/MRH-2, and pages iv, v, and 4-7 to 4-10 |
| 001-N1 | 10-30-96 | 41456 | Replaced Title Page, MRH-1/MRH-2, and pages 7-1 and 7-28. Added 7-29 \& 7-30 |
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| 001-P | 09-09-97 | 41796 | Replaced Title Page, MRH-1/MRH-2, iv, v, and all of Sections IV, V, \& VII |
| 001-P1 | 02-08-99 | 42225 | Replaced Title Page, MRH-1/MRH-2, and all of Section VII |
| 001-P2 | 05-31-00 | 45921 | Replaced Title Page, MRH-1/MRH-2, and all of Section VII |

## Guide to Using Harris Parts List Information

The Harris Replaceable Parts List Index portrays a tree structure with the major items being leftmost in the index. The example below shows the Transmitter as the highest item in the tree structure. If you were to look at the bill of materials table for the Transmitter you would find the Control Cabinet, the PA Cabinet, and the Ouqut Cabinet. In the Replaceable Parts List Index the Control Cabinet, PA Cabinet, and Output Cabinet show up one indentation level below the Transmitter and implies that they are used in the Transmitter. The Controller Board is indented one level below the Control Cabinet so it will show up in the bill of material for the Control Cabinet. The tree structure of this same index is shown to the right of the table and shows indentation level versus tree structure level.

Example of Replaceable Parts List Index and equivalent tree structure:


The part number of the item is shown to the right of the description as is the page in the manual where the bill for that part number starts.
Inside the actual tables, four main headings are used:
Table \#-\#. ITEM NAME - HARRIS PART NUMBER - this line gives the information that corresponds to the Replaceable Parts List Index entry;
HARRIS P/N column gives the ten digit Harris part number (usually in ascending order);
DESCRIPTION column gives a 25 character or less description of the part number;
REF. SYMBOLS/EXPLANATIONS column 1) gives the reference designators for the item (i.e., C001, R102, etc.) that corresponds to the number found in the schematics ( $\mathrm{COO1}$ in a bill of material is equivalent to Cl on the schematic) or 2) gives added information or further explanation (i.e., "Used for 208 V operation only," or "Used for HT 10LS only," etc.).
Inside the individual tables some standard conventions are used:
A \# symbol in front of a component such as \#COO1 under the REF. SYMBOLS/EXPLANATIONS column means that this item is used on or with $\mathrm{COO1}$ and is not the actual part number for C 001 .
In the ten digit part numbers, if the last three numbers are 000, the item is a part that Harris has purchased and has not manufactured or modified. If the last three numbers are other than 000, the item is either manufactured by Harris or is purchased from a vendor and modified for use in the Harris product.
The first three digits of the ten digit part number tell which family the part number belongs to - for example, all electrolytic (can) capacitors will be in the same family ( 524 xxxx 000 ). If an electrolytic (can) capacitor is found to have a $9 x x \operatorname{xxx} x x x$ part number (a number outside of the normal family of numbers), it has probably been modified in some manner at the Harris factory and will therefore show up farther down into the individual parts list (because each table is normally sorted in ascending order). Most Harris made or modified assemblies will have $9 \mathrm{xx} \operatorname{xxxx} \mathrm{xxx}$ numbers associated with them.
The term "SEE HIGHER LEVEL BILL" in the description column implies that the reference designated part number will show up in a bill that is higher in the tree structure. This is often the case for components that may be frequency determinant or voltage determinant and are called out in a higher level bill structure that is more customer dependent than the bill at a lower level.
S.O. Box 4290, QUINCY, IL

CUSTOMER NAME: $\qquad$ (if different from billing informotion)
ADDRESS:
$\qquad$
ADDRESS: $\qquad$
$\qquad$

TELEPHONE NUMBER: $\qquad$
FAX NUMBER: PREFERRED
PAYMENT METHOD: $\qquad$

FREQUENCY (If required): $\qquad$
EQUIPMENT NAME: $\qquad$
EQUIPMENT PART NUMBER: $\qquad$
EQUIPMENT SERIAL NUMBER: $\qquad$

| ITEM \# | QTY | HARRIS PART NUMBER | DESCRIPTION OF PART <br> (PART'S NAME, DESCRIPTION, SPECIFICATION FROM PARTS LIST IF AVAILABLE) | SCHEMATIC REFERENCE REFERENCE NAME (e.g. COO1, R100, etc) | ITEM USED ON (NEXT HIGHER ASSEMBLY IF KNOWN) (e.g. COO USEd on 9928025 OO1, SCHEMATIC 8398099 991) | COMMENTS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
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## WARNING


#### Abstract

THE CURRENTS AND VOLTAGES IN THIS EQUIPMENT ARE DANGEROUS. PERSONNEL MUST AT ALL TIMES OBSERVE SAFETY WARNINGS, INSTRUCTIONS AND REGULATIONS.


This manual is intended as a general guide for trained and qualified personnel who are aware of the dangers inherent in handling potentially hazardous electrical/electronic circuits. It is not intended to contain a complete statement of all safety precautions which should be observed by personnel in using this or other electronic equipment.

The installation, operation, maintenance and service of this equipment involves risks both to personnel and equipment, and must be performed only by qualified personnel exercising due care. HARRIS CORPORATION shall not be responsible for injury or damage resulting from improper procedures or from the use of improperly trained or inexperienced personnel performing such tasks.

During installation and operation of this equipment, local building codes and fire protection standards must be observed. The following National Fire Protection Association (NFPA) standards are recommended as reference:

- Automatic Fire Detectors, No. 72E
- Installation, Maintenance, and Use of Portable Fire Extinguishers, No. 10
- Halogenated Fire Extinguishing Agent Systems, No. 12A


#### Abstract

WARNING ALWAYS DISCONNECT POWER BEFORE OPENING COVERS, DOORS, ENCLOSURES, GATES, PANELS OR SHIELDS. ALWAYS USE GROUNDING STICKS AND SHORT OUT HIGH VOLTAGE POINTS BEFORE SERVICING. NEVER MAKE INTERNAL ADJUSTMENTS, PERFORM MAINTENANCE OR SERVICE WHEN ALONE OR WHEN FATIGUED.


Do not remove, short-circuit or tamper with interlock switches on access covers, doors, enclosures, gates, panels or shields. Keep away from live circuits, know your equipment and don't take chances.

## WARNING

IN CASE OF EMERGENCY ENSURE THAT POWER HAS BEEN DISCONNECTED.

## WARNING

IF OIL FILLED OR ELECTROLYTIC CAPACITORS ARE UTILIZED IN YOUR EQUIPMENT, AND IF A LEAK OR BULGE IS APPARENT ON THE CAPACITOR CASE WHEN THE UNIT IS OPENED FOR SERVICE OR MAINTENANCE, ALLOW THE UNIT TO COOL DOWN BEFORE ATTEMPTING TO REMOVE THE DEFECTIVE CAPACITOR. DO NOT ATTEMPT TO SERVICE A DEFECTIVE CAPACITOR WHILE IT IS HOT DUE TO THE POSSIBILITY OF A CASE RUPTURE AND SUBSEQUENT INJURY.

## TREATMENT OF ELECTRICAL SHOCK

1. IF VICTIM IS NOT RESPONSIVE FOLLOW THE A-B-CS OF BASIC LIFE SUPPORT.

PLACE VICTIM FLAT ON HIS BACK ON A HARD SURFACE
(A) AIRWAY

IF UNCONSCIOUS,
OPEN AIRWAY


LIFT UP NECK
PUSH FOREHEAD BACK
CLEAR OUT MOUTH IF NECESSARY OBSERVE FOR BREATHING

CHECK CAROTID PULSE
(B) BREATHING

IF NOT BREATHING.
BEGIN ARTIFICIAL BREATHING


TILT HEAD
PINCH NOSTRILS
MAKE AIRTIGHT SEAL
4 QUICK FULL BREATHS
REMEMBER MOUTH TO MOUTH
RESUSCITATION MUST BE
COMMENCED AS SOON AS POSSIBLE


IF PULSE ABSENT. BEGIN ARTIFICIAL CIRCULATION

## (C) CIRCULATION

DEPRESS STERNUM $11 / 2$ TO 2 INCHES
 APPROX. RATE
OF COMPRESSIONS
--80 PER MINUTE $\left\{\begin{array}{l}\text { ONE RESCUER } \\ 15 \text { COMPRESSIONS } \\ 2 \text { QUICK BREATHS }\end{array}\right] \begin{aligned} & \text { APPROX. RATE } \\ & \text { OF COMPRESSIONS } \\ & --60 \text { PER MINUTE }\left\{\begin{array}{l}\text { TWO RESCUERS } \\ 5 \text { COMPRESSIONS } \\ 1 \text { BREATH }\end{array}\right.\end{aligned}$


NOTE: DO NOT INTERRUPT RHYTHM OF COMPRESSIONS WHEN SECOND PERSON IS GIVING BREATH

CALL FOR MEDICAL ASSISTANCE AS SOON AS POSSIBLE.
2. IF VICTIM IS RESPONSIVE.
A. KEEP THEM WARM
B. KEEP THEM AS QUIET AS POSSIBLE
C. LOOSEN THEIR CLOTHING
D. A RECLINING POSITION IS RECOMMENDED

## FIRST-AID

Personnel engaged in the installation, operation, maintenance or servicing of this equipment are urged to become familiar with first-aid theory and practices. The following information is not intended to be complete first-aid procedures, it is a brief and is only to be used as a reference. It is the duty of all personnel using the equipment to be prepared to give adequate Emergency First Aid and thereby prevent avoidable loss of life.

## Treatment of Electrical Burns

1. Extensive burned and broken skin
a. Cover area with clean sheet or cloth. (Cleanest available cloth article.)
b. Do not break blisters, remove tissue, remove adhered particles of clothing, or apply any salve or ointment.
c. Treat victim for shock as required.
d. Arrange transportation to a hospital as quickly as possible.
e. If arms or legs are affected keep them elevated.

NOTE
If medical help will not be available within an hour and the victim is conscious and not vomiting, give him a weak solution of salt and soda: 1 level teaspoonful of salt and $1 / 2$ level teaspoonful of baking soda to each quart of water (neither hot or cold). Allow victim to sip slowly about 4 ounces (a half of glass) over a period of 15 minutes. Discontinue fluid if vomiting occurs. (Do not give alcohol.)
2. Less severe burns - (1st \& 2nd degree)
a. Apply cool (not ice cold) compresses using the cleanest available cloth article.
b. Do not break blisters, remove tissue, remove adhered particles of clothing, or apply salve or ointment.
c. Apply clean dry dressing if necessary.
d. Treat victim for shock as required.
e. Arrange transportation to a hospital as quickly as possible.
f. If arms or legs are affected keep them elevated.

## REFERENCE:

ILLINOIS HEART ASSOCIATION

AMERICAN RED CROSS STANDARD FIRST AID AND PERSONAL SAFETY MANUAL (SECOND EDITION)

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## SECTION I GENERAL INFORMATION

### 1.1. Introduction

This section contains a general description, overall block diagram, and specifications of the Harris VHF TV exciter.

### 1.2. Equipment Description

The Harris VHF TV exciter is a CCIR system $M$ television exciter. Both the aural and visual exciters are included in a single package. All operator indicators are front-panel mounted for ease of operation. An analog and an LED digital display provides indications of exciter parameters (see Figure 1-1). All internal circuitry is mounted on plug-in circuit boards with the exception of the two modular final amplifiers, and the power supply. A motherboard provides power and control connections, all If and if connections are coaxial. The mother board will accommodate 13 plug-in circuit boards. The meter and control circuit board mounts behind the front panel. The aural and visual final amplifiers are mounted in the rear along with the power supply section.
Phase-locked loops in the visual as well as the aural circuits are stabilized from a single reference. Digital control circuits provide simple and precise user interface. Separate wide-band

RF final amplifiers are provided for both aural and visual outputs.
A flushing fan assures cool and reliable operation. The flow of the fan forces air between final visual and aural amplifiers and along side of the main power supply where the regulators are mounted. Cooling air exits on each side of the chassis and from the top cover after passing through the card cage where the plug-in circuit boards are housed.
The internal power supply allows operation from potentials in the 120 -volt range as well as the 240 -volt range, 50 or 60 Hz .

The unit mounts on slide rails in a standard 19 -inch rack for ease of maintenance. The majority of controls mounted on circuit boards are accessible from the top.

### 1.3. Equipment Specifications

Refer to Table 1-1 for electrical and physical specifications of the VHF TV exciter.

NOTE
Specifications subject to change without notice.


Figure 1-1. HX 1V Exciter

## HARRIS HXIV VHF EXCITER SPECIFICATIONS



[^0]Relative to visual poak eync.
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## SECTION II INSTALLATION

### 2.1. Introduction

This section contains information required for installation and preliminary checkout of the VHF TV exciter.

### 2.2. Unpacking

The equipment becomes the property of the customer when the unit is delivered to the carrier. Carefully unpack the unit and perform a visual inspection to determine that no apparent damage has been incurred during shipment. All shipping materials should be retained until it has been determined that the unit was not damaged in shipment. Claims for damaged equipment must be filed promptly or the carrier may not accept the claim.
Each VHF TV exciter shipment consists of the following items in addition to the exciter:
Manual
Power cord
Exciter mounting hardware (only with units sold separately)
The contents of the shipment should be as indicated on the packing lists. If the contents are incomplete, or if the unit is damaged electrically or mechanically, notify the Harris Customer Service Department (217-222-8200) at the following address:

Harris Corporation, Broadcast Division
P. O. Box 4290

Quincy, IL 62305
ATTEN: Customer Service Department

### 2.3. Installation

The VHF TV exciter may be mounted in any convenient location in a 19 inch ( 48.3 cm ) rack within reach of signal and power cables. The Exciter should not be mounted directly above heat generating equipment such as power amplifier stage, otherwise no special requirements need be observed.

## WARNING

ASSURE POWER IS DISCONNECTED BEFORE PROCEEDING.
a. Assure power is disconnected before proceeding.
b. Set the unit on a work surface and remove any packing from the outside of the unit.
c. If the exciter purchased was part of a transmitter, proceed directly to paragraph 2-3.2. If the exciter was purchased for other replacement configurations proceed with paragraph 2.3.1.
2.3.1. Exciter Mounting
a. Remove the sliding portion of each slide rail from the sides of the exciter.
b. Mount the front edge of each slide rail to its respective side of the cabinet with the hardware supplied.

## CAUTION

## ASSURE THE SLIDE RAILS ARE PARALLEL AND LEVEL BEFORE

 DRILLING MOUNTING HOLES IN THE RACK CABINET.c. Assure the slide rails are parallel and level. Mark and drill holes for mounting the rear of each rail. Hardware is supplied for this purpose.
d. After the slide rails are mounted, extend both rails fully and lift the exciter onto the rails over the stops. Push the exciter fully into the rack.

### 2.3.2. Input Power Selection

Pull the exciter forward out of the rack until the slide-rail stops are encountered.

## WARNING

## ASSURE POWER IS DISCONNECTED BEFORE PROCEEDING.

a. Assure power is disconnected before proceeding.
b. Remove the top cover of the exciter and the cover of the power supply. Refer to paragraph 5.3.1. Check the wiring to the ac terminal strip on the right hand side of the power supply. Refer to Exciter Power Supply schematic 839 -7900-504 and assure that the exciter is wired for operation with the primary voltage with which the unit will be used ( 105 to 125 volt range or 210 to 250 volt range). A tag on the exciter indicates the voltage the exciter was set to when leaving the factory.

### 2.3.3. Exciter Inputs And Outputs

Prepare cabling for the exciter inputs and outputs. The rearpanel connections available for use on the exciter are identified by Figure 2-1 and described by Table 2-1.

### 2.3.4. Exciter Remote Control Connections

Prepare cabling for the exciter remote controller. The functions available are described by Table 2-2.

### 2.3.5. Circuit Boards

There are 13 slots in the motherboard for exciter circuit boards. J 1 is the slot on the right side when the exciter is viewed from the front. The circuit boards install in the sequence given in Table 2-3 with the component side to the left when viewed from the front.


Figure 2-1. Exciter Inputs and Outputs

Table 2-1. Exciter Inputs and Outputs

| CONNECTOR | DESCRIPTION |
| :--- | :--- |
| $\mathrm{J}-1$ | AC POWER |
| $\mathrm{J}-2$ | VISUAL RF OUT |
| $\mathrm{J}-3$ | AURAL RF OUT |
| $\mathrm{J}-4$ | VIDEO INPUT |
| $\mathrm{J}-5$ | COMPOSITE AUDIO IN |
| $\mathrm{J}-6$ | Sub-Carrier 1 IN |
| $\mathrm{J}-7$ | Sub-Carrier 2 IN |
| $\mathrm{J}-8$ | MONO AUDIO IN |
| $\mathrm{J}-9$ | CONTROL/REMOTE INTERFACE |
| $\mathrm{J}-10$ | EXTERNAL PFC (option) |
| CB1 | BREAKER/ON/OFF SWITCH |


| J9 |  |  |
| :--- | :--- | :--- |
| PIN \# | EUNCTION | SIGNAL |
| 1 | VISUAL RAISE COMMAND | ACTIVE LOW |
| 2 | VISUAL LOWER COMMAND | ACTIVE LOW |
| 3 | AURAL RAISE COMMAND | ACTIVE LOW |
| 4 | AURAL LOWER COMMAND | ACTIVE LOW |
| 5 | AURAL MUTE COMMAND | ACTIVE LOW |
| 6 | VISUAL MUTE COMMAND | ACTIVE LOW |
| 7 | VISUAL POWER SENSE OUT | DC VOLTAGE PROPORTIONAL TO DAC SETTING |
| 8 | AURAL POWER SENSE OUT | DC VOLTAGE PROPORTIONAL TO DAC SETTING |
| 9 | VISUAL MUTED STATUS, OPEN COLLECTOR | LOW=MUTED |
| 10 | AURAL MUTED STATUS, OPEN COLLECTOR | LOW=MUTED |
| 11 | VISUAL UNLOCKED STATUS, OPEN COLLECTOR | LOW=UNLOCKED |
| 12 | AURAL UNLOCKED STATUS, OPEN COLLECTOR | LOW=UNLOCKED |
| 13 | DUAL CORRECTION STATUS, OPEN COLLECTOR |  |
| 14 | VOLTAGE OUTPUT | +15V DC @ 10 MA |
| 15 | VISUAL VSWR INPUT, DC VOLTAGE | FOLDBACK PROPORTIONAL TO VSWR |
| 16 | AURAL VSWR INPUT, DC VOLTAGE | FOLDBACK PROPORTIONAL TO VSWR |
| $17-20$ | UNUSED |  |
| 21 | NOTCH DIPLEXER REMOTE (LOW = BYPASS) |  |
| 22 | AURAL GROUP DELAY REMOTE (LOW = BYPASS) |  |
| $23-26$ | GROUND |  |
| 27 | UNUSED |  |
| $28-37$ | USED FOR EXCITER SWITCHER |  |

Table 2-3. Circuit Board Placement

| SLOT |  |
| :--- | :--- |
| J1 | CIRCUIT BOARD |
| J2 | Video input/Diff Gain Corrector |
| J3 | Notch Diplexer Equalizer (Optional) |
| J4 | Open for option |
| J5 | Differential Phase Corrector |
| J6 | Modulator/Delay Compensator |
| J7 | VSB/AGC |
| J8 | Linearity/Quadrature Corrector |
| J9 | Open for options |
| J10 | Offset Option |
| J11 | Visual Converter |
| J12 | Open for options |
| J13 | Aural Group Delay Corrector (Optional) |

## SECTION III OPERATION

### 3.1. Introduction

This section identifies all controls and indicators associated with the VHF TV exciter.

### 3.2. Controls And Indicators

Refer to Figure 3-1 for the location of all controls and indicators associated with day-to-day standard operation of the VHF TV exciter. The function of each control and indicator is listed in Table 3-1.


Figure 3-1. Exciter Controls and Indicators

Table 3-1. Exciter Controls and Indicators

| REF | IIEM | YUNCJION |
| :---: | :---: | :---: |
| 1 | DRIVE POWER MW | Displays numeric drive power in milliwatts. |
| 2 | POWER BAR GRAPH | Displays power 0-1 watt. Visual power ref. peak sync. Aural power C.W. |
| 3 | METER SELECT DRIVE POWER | Selects Visual or Aural output for display on digital readout and power bar graph. |
| 4 | VISUAL/AURAL RAISE LOWER | Momentary switch to raise or lower exciter output power. This is a two speed control. When first depressed the power will change slowly, but if it is then held down for aproximately 10 seconds the power will change at a faster rate until released. It will return to the slower rate upon release. The power adjustment commands are independent of the meter select. Be sure to check metering before making exciter power adjustments to see if VIS or AUR PWR is being monitored. |
|  |  | The controller power fail circuits maintain control after an ac power outage. During this time the power controls are still active and will raise or lower the power if depressed even though ac is not present. |
| 5 | STATUS LEDS |  |
|  | SECOND CORRECTOR | Indicates optional corrector for dual power level is in use. |
|  | AURAL MUTE | Indicates aural exciter is muted either internally (PLL failure) or externally (MAIN CONTROLLER on/off or overload.) |
|  | VISUAL MUTE | Indicates VISUAL exciter is muted either internally (PLL failure) or externally (MAIN CONTROLLER on/off or overload.) |
|  | BOARD BYPASS | Indicates one of the correction modules has been left in bypass position.(i.e. VSB, DELAY COMP) Jumpers are provided on the individual boards to disable its bypass status if a particular board is not needed for normal operation. |
|  | AURAL IF LOCK | IllumInated when AURAL PLL is unlocked. |
|  | VISUAL IF LOCK | Illuminated when VISUAL IF PLL is unlocked. |
|  | MASTER LOCK | Illuminated when the MASTER PLL is unlocked. |
|  | POWER | Illuminated when ac power is on. (AC POWER SWITCH/BREAKER IS LOCATED ON BACK PANEL OF UNIT.) |

### 4.1. Introduction to Theory of Operation

This section provides theory of operation for the VHF TV exciter. For purposes of discussion, the circuitry is divided into functional subassemblies by the following text. Refer to the separately packaged block diagram and schematic diagram as required for the following description. All circuit boards plug into a mother board that provides interconnections between circuits.

### 4.2. Video Differential Gain/Low Frequency Linearity Correction Board

Refer to 843-5285-411

### 4.2.1. Functional Description

This video input card contains circuitry to allow the independent linearity adjustment of the luminance and the chrominance signal components. Circuitry can also clip the peak white luminance signal peaks that exceeds a set level.
This video card performs sync regeneration, low frequency linearity (LFL) correction, differential gain correction and white signal clipping. The interaction between differential gain and LFL corrections is minimized. The video signal is clamped with adjustable clipping levels. Output signal level can be easily adjusted. When the card is used in an HTEL 5/10 exciter, the input video and sync voltage levels can be monitored through exciter metering. The board is designed to work with NTSC and PAL signals.

### 4.2.2. Detailed Theory of Operation

### 4.2.2.1. Input Stage

Input video signal is fed to the video board from the I/O panel through an SMB connector. The shield is not grounded at any point in the cabling of the transmitter to allow common mode signal rejection in the first stage. Provisions for a selection of AC or DC coupling by changing the selector jumper JP5. The input circuit, opamp U3, is designed for approximately 40 dB of input common mode rejection. It can be floated or grounded by jumper JP3. In this circuitry capacitor C31 is left as an option for cable compensating purpose. U3 is a unity gain amplifier, the output voltage is measured by two peak reading detector circuits, one measures the voltage above zero volts DC as a video component measurement, The other detector measures the amplitude of the negative sync voltage.
Adjustable voltage divider R1 sets the signal level for further processing and ultimately the card output level. U1 is a non-inverting amplifier with a gain of two when R46 is present. If R46 is replaced with a jumper, the gain is 1 . U11 performs as a sync separator which outputs sync pulses at pin 1 and burst pulses at pin 5 .
Burst pulses drive Q15 and Q14 which clamps the signal coming into U11. A notch filter at input pin 2 of U11 blocks burst frequency so that the sync level can go down as much as -6 dB without affecting the performance of the clamping circuit.
4.2.2.2. Sync removal and Reinsertion Stage

The output signal from U6 is frequency response corrected (U14) before the delay line DL1 and Sync stripper U16. Since there is a timing difference between the sync pulses from U11 and the sync pulses of the main signal, DL1 is used for time compensation. Sync pulses from U11 are processed through U7 which creates stripping pulses and new sync pulses. Timing is correctly adjusted by pots R105, R110 at U7 so that the output from U16 is sync-stripped. U16 is a gain controllable opamp whose gain is controlled by pulses coming into pin 2 . Blanking level is adjusted by R124 and R131. At the same time, new sync pulses from pin 8 of U7 are processed by Q13, Bessel lowpass filters and U2. The lowpass filters are to shape up the sync so that sync specs are met and 6 MHz signal bandwidth is preserved. Jumpers JP1 and JP2 select between NTSC and PAL sync pulses. The newly created syncpulses are adjusted by R2 and fed to U2. U2 is an isolation stage between the filters and the input of signal-sync combiner U8. DL1 provides enough delay so that the new sync pulses and the video signal time up correctly. Timing for sync reinsertion is adjusted by R106 and R111 (in both circuits, sync stripping and sync creating, the first pots are to adjust trailing end of the pulse and the second pots adjust the leading end).
When video input is missing, PLL chip U17 fails to lock incoming sync with its internally generated 15 kHz square wave. The output at pin 8 of U17 goes high, that turns on Q16. In order to isolate the digital chips from the rest of the circuit, isolated power supplies including L8 and L3, are used for U3, U4 and U17.

### 4.2.3. Differential Gain

Video from U5 is differential gain adjusted by U5, Q1, Q2, Q3 and Q4. The gain is decreased by shunting the video signal to AC ground through R28 and R29 and increased by the increase in feedback gain of U5. The gain corresponding to a certain video signal level is adjusted when either of Schottky switching diodes CR1, CR2, CR3, CR4 is turned on. In this case, the signal will see a small impedance, approx. 10 ohms max., at the emitter of the transistor. R11, R12, R13 and R14 adjust the magnitude of the change or the slope of the differential gain curve. R3, R4, R5, R6 set the switching levels or the thresholds. The reference threshold levels are provided by the voltage dividers at the base of the transistors. These dividers are carefully and accurately designed so that the blanking level will not change. The differential gain stage is deactivated when all the threshold levels are switched to 4.3 V by switch S 1 . S1 also provides the necessary voltage to activate Q9 and Q10 when the correction is off.

### 4.2.3.1. Low Frequency Linearity

To correct low frequency linearity (LFL), the burst frequency component of the video signal must be completely filtered out. DL2 is a high quality delay line that shifts the chroma frequency ( 3.58 MHz for NTSC or 4.43 MHz for PAL) 180 degrees. That is equivalent to a delay of 140 ns for NTSC signal or 110 ns for

PAL signal. The delayed signal and the original one are combined at the output of U10 and the resulted signal has no chroma component. Pot R96 adjusts the magnitude of the delayed signal until a perfect luminance is obtained. At the same time, signal subtraction is performed by U12 to restore the chrominance of the signal. The luminance is corrected by LFL correction circuit which is similar to the differential gain circuit above. AD8037, U4, is used as a opamp to allow control of the clipping levels of the signal. R71 sets the white clipping level and the sync clipping level is set by R96 and R104.
The chrominance and luminance are recombined at U15 to restore the video signal. Pot R115 adjusts the mixing ratio. This adjustment affects the response of the circuit. The response has a pole close to 4 MHz . This response problem is corrected by C 70 in the input of U 15.

### 4.2.3.2. Output stage

Output stage consists of U15 which is designed as a first order allpass group delay equalizer. The circuit will provide enough group delay to compensate for the group delay of the frequency response correction network (U14).
The output level is controlled by U1 and R1
The board is set up so that when used with Harris HTEL and PLATINUM exciters with an input level of 0.75 to 2.0 volts. It will produce a maximum 1.5 Vpp video signal on 75 ohm output load. For input levels below 0.75 vpp , change R46 to 750 ohm .

### 4.3. Notch Diplexer Equalizer

Refer to 839-7900-493

### 4.3.1. General Description \& Theory of Operation

Four active allpass networks are used to equalize the delay and amplitude response distortion caused by the Notch Diplexer. Each of the four sections are very similar in design but have considerable flexibility in adjustment.
The term allpass defines a network which has a changing phase characteristic, with a flat amplitude response. The action of an active allpass can best be explained using a simplified schematic, Figure 4-1.
If the voltage E1 was plotted as a function of frequency, it would have the familiar bandpass filter characteristic due to the tuned elements C 1 and L1. E1 would have a related phase shift at various frequencies. E2 would have a flat amplitude response and no phase shift. When E1 and E2 are subtracted in A1, the
output E3 has the unique property of having E1's phase and E2's amplitude. Thus the allpass network. In a practical circuit it is possible to have four significant controls.
a. Frequency - C46, C4, C36, and C24 of actual circuit adjust the frequency of resonance or delay.
b. Q-R42, R30, R85, and R92 of actual circuit adjust the $Q$ of the resonant circuit or magnitude of delay.
c. Balance-R40, R10, R80, and R52 of actual circuit adjust amplitude response - causes a peak or valley.
d. Phase - C20, C3, C32, and C22 of actual circuit adjust amplitude response - causes a sinewave shape.

### 4.4. Differential Phase Corrector

Refer to 839-7900-490
The purpose of the differential phase corrector is to correct transmitter distortions of the color sub-carrier phase with luminance level. It operates at video and predistorts the color phase.
The differential phase corrector consist of a first order all pass network which provides a phase characteristic without disturbing the amplitude response. A clamp pulse generator and clamping circuits are provided to maintain blanking level.
The all pass network consists of two video paths 180 degrees out of phase. The out of phase signals are summed together in a RL network. The ratio of $L$ to $R$ determines the resultant phase. By changing the value of $R$ with video luminance the corresponding phase is changed.
The input video is applied to a back porch clamp consisting of C45 and Q13. Clamping is done during back porch. L3 presents a high impedance to sub- carrier to prevent distortion due to the clamp pulse. A dual JFET Q14 provides a high impedance to the clamp and a low impedance output.
Ul form a differential amplifier and generates the two video paths which are 180 degrees out of phase. Q6 is a current source for the differential amp and also provides bias stabilization. R4 and C 1 set the amplifiers frequency response and are set for a flat response. C48 equalizes the two 180 degree outputs for symmetrical response and is set for minimum interaction between differential phase and gain. Q1 and Q2 buffer the two video paths and provide a low impedance drive for the all pass network.
L2 and R17 form the basic all pass network. The two video paths are summed together and buffered by Q3. R17's value is modified as a function of luminance level and creates the desired correction shape.
A Schotky diode network is used to change R17's value with luminance level. An adjustable reverse bias (Threshold) is applied to the diode. As the video level increase it will eventually exceed the diode's bias and the diode will become forward biased. When this happens the diode acts as a switch and places an adjustable resistor (Slope) in parallel with R17. There is a total of five diode networks to allow precise correction of differential phase.
The output of the allpass network is passed through a second clamp consisting
of C14 and Q4 and buffer amp Q4, it is then applied to the output amplifier.
The output amplifier consists of Q7, Q8 and Q15 provides a 75 ohm drive impedance for the output of the card and for the monitor output connector.
Clamp pulses are generated by a sync separator and are timed to coincide with back porch and level shifted to provide back porch clamping to 0 Vdc . U 1 provides a inverted video output to drive the clamp pulse generator. Q9 and U 4 amplify the inverted video signal to approximately 10 V peak to peak. U4 is also band limited by C 27 such that sub-carrier is suppressed and only luminance passes. CR11 provides rough peak sync clamping to 0 Vdc . U5 is a high speed comparator and separates sync from the band limited video. U6 provides a time delay to correctly position the clamp pulses during back porch. Q10 and Q11 offset the clamp pulse to correctly bias the clamping FETs Q5 and Q13.

### 4.5. Modulator/Delay Compensator Board <br> Refer to 839-7900-443 (sheet 3)

### 4.5.1. Modulator Circuit

### 4.5.1.1. Functional Description

The Modulator printed circuit uses a double balanced mixer to perform modulation of the IF carrier by the video signal from the Amplifier board. In addition to the mixer, the board contains amplification circuits and a frequency response equalization network.

### 4.5.1.2. Detailed Description

The output signal from the IF Oscillator is applied to the Modulator input jack J1. Since the signal level from the oscillator ranges from 150 to 300 mV rms , the IF Drive potentiometer R1 is used to adjust the level supplied to amplifier Q1. The voltage gain of approximately 4 is determined by the ratio between R5 and the effective impedance at the collector of Q1. This impedance is the parallel combination of R4 and the impedance reflected back to the primary of $T 1$, which is a $4: 1$ stepdown rf transformer. The output from Q1 and T1 provides the drive signal for the $\mathrm{L}(\operatorname{pin} 3)$ and $L^{\prime}($ pin 1$)$ ports of the mixer U1. See Figure 4-2 .
Assuming perfect balance of the mixer diodes and transformers, there will not be an IF output when there is no current input
to the X port (pin 5). The Modulator Balance potentiometer R37 is adjusted to cancel any output caused by slight inherent mixer imbalance. The IF output from mixer port $R$ (pin 6) is proportional to the current flowing into the X port (pin 5). Consequently, the video signal amplitude modulates the IF signal. To provide the correct modulation depth, some current must be added to the video signal. The Modulator Bias potentiometer R12 adjusts this current offset to provide the proper modulation depth. The Video Drive potentiometer R10 adjusts the amount of video signal current to the modulator.
The modulated output from the mixer U 1 and the Modulator Balance potentiometer R37 are summed in the emitter of the grounded base amplifier Q2. The gain of approximately two is determined by the ratio of the emitter input resistor R16 and the collector impedance. The signal from R37 is added at the low impedance point at the emitter.
A frequency response equalization network is inserted between Q2 and Q3. Capacitors C10 and C11 control the frequency of this series resonant circuit and R20 controls the Q. R40 serves as a slope or tilt control. This permits correction for slight frequency response deviations elsewhere in the exciter circuits. A second harmonic trap, L3 and C12 or C13, is inserted at the input to the common base amplifier Q3. The signal is amplified six times and applied to emitter follower Q4 The output is routed through jumpers at P1 to test jack J2 or to the delay compensator circuit.

### 4.5.2. Delay Compensator Circuit

Refer to 839-7900-443 sheets 1 and 2

### 4.5.2.1. Functional Description

The Delay Compensator board contains two identical active allpass networks in cascade. An allpass network has the characteristic of flat amplitude response and nonlinear phase response. Since group delay is a result of nonlinear phase shift, an allpass network corrects group delay in the transmitter by providing compensation at certain frequencies. Delay errors caused by the notch diplexer (if used) are corrected by the notch diplexer equalizer.
In an active allpass network the signal is split into two paths: a narrow band path and wideband path. The narrow band path is a series tuned circuit with variable Q and frequency controls for adjustment of the amount of group delay correction and the


Figure 4-2. Modulator
frequency at which it is applied. The wideband path has only an attenuator and fixed phase shift network. For proper allpass operation, the signals must be combined at the output such that the narrow band signal is 6 dB greater and 180 degrees out-ofphase at the resonant frequency of the tuned circuit.

### 4.5.2.2. Detailed Description

The signal is applied to the allpass network through P1-1 and is split into two paths. In the narrow bandpath, emitter follower Q101 provides isolation and power amplification to drive the series resonant circuit of C109, C111 and L105. The Q is determined by the parallel combinations of R145, R147, R149, and R151 selected by the 16 position switch S103. L109, L115, C 139 and C122 is a variable phase shift network providing the proper phase relationship between the two signal paths. BALANCE potentiometer R105 is used to obtain the proper amplitude relationship between the two paths. In the wideband path, the signal passes through a fixed phase shift network C103, L101 and C107, and a fixed attenuator R117, R119 and R121. The two signals are combined in T 101 . The secondary of T 101 is the vector difference of the two signals applied to the primary.
When the BYPASS toggle switch S101 is set to the IN position, Q101 receives collector voltage, and PIN diode switches CR101 and CR103 are supplied current to turn them on. When S101 is set to the OUT position, Q101 and CR103 turn off blocking the narrow band path signal. CR101 is also turned off to compensate for a small gain change in the BYPASS mode. The signal still passes through the wideband path, but no group delay compensation is provided by the narrow band path. Q103 is a common base amplifier with a voltage gain of approximately nine to compensate for the loss in the allpass section. The output of the first allpass network is applied to the second network through emitter follower Q105.
Q102, Q104 and Q106 make up the second allpass network. The output of this section and the output of the Modulator/Delay Compensator board are applied to output jack J3.

### 4.6. VSB/AGC Board

Refer to 839-7900-491

### 4.6.1. Vestigial Sideband Filter Circuit

The purpose of the vestigial sideband filter circuit board is to provide frequency response shaping that is required in television. This is accomplished in filter FLl which is a surface acoustic wave device.
In CCIR-M systems the filter also provides the receiver delay equalization.
The video IF signal is input through capacitors C 1 and C 2 . The VSB IN/VSB OUT switch allows switching the VSB filter in or out of the circuit. When the switch is set to VSB IN, the signal path will be through CR1. When the switch is set to VSB OUT, the signal path will bypass the VSB filter.

### 4.6.1.1. VSB Signal Path

The signal through C1 and CR1 is applied to gain stage Q5 which provides approximately 15 dB of gain to overcome half the 30 dB loss in filter FL1. The signal is inductively coupled from Q5 to emitter-follower Q6. Resistor R23 establishes a

51 -Ohm input impedance for filter FL1. The signal is coupled into FLl by capacitor C16.
The output of the filter is coupled through C10 and applied to gain stage Q 3 which provides approximately 15 dB of gain to overcome half the 30 dB loss in filter FL1.

### 4.6.1.2. Bypass Path

When the VSB OUT/VSB IN switch is set to VSB OUT, transistors Q1 and Q2 will bias diode CR2 on and bias diode CR1 off. The signal path will bypass the VSB filter. The arrangement of $\mathrm{R} 6 / \mathrm{R} 7 / \mathrm{R} 8$ in the bypass path is a variable attenuator which allows adjustment of the signal level from the bypass path to the same level as the output from the VSB filter path so that a level shift does not occur when the filter is switched in or out.

### 4.6.1.3. AGC Circuit (Visual)

Refer to drawing 839-7900-491
The visual exciter power is controlled by the IF AGC circuit.
Control voltage from the metering and control board is applied to the + input of comparator U101A. Detector input from the visual amplifier provides the - comparator input through buffer U101B.
In AUTO mode the output of U101A controls the attenuation through a voltage divider formed by PIN diode CR101 and R107. Attenuation is variable from 1 to approximately 40 dB . R116 provides adjustment of the AGC range by limiting the maximum current applied to CR101.
In MAN (manual) mode the control voltage is routed directly to the gain control circuit, and is used for trouble shooting purposes only.
Emitter follower Q101 provides isolation and low impedance drive. Q102 provides $10-11 \mathrm{~dB}$ of gain. The net gain of the AGC section is $9-10 \mathrm{~dB}$ with CR101 fully turned on.

### 4.7. Linearity/Quadrature Corrector Board

Refer to 839-7900-444
The purpose of this circuit board is to adjust the carrier phase and gain as a function of the video level. As the transmitter power output level increases, the amplitude of the signal will compress and the phase of the signal will shift. This circuit board will pre-distort the IF signal to compensate for the shift in phase and amplitude caused by the power amplifiers.

### 4.7.1. IF Linearity Corrector Circuit

### 4.7.1.1. Functional Description

Refer to sheet 1 of 839-7900-444
It is advantageous from the viewpoint of performance to perform differential gain correction on the IF signal instead of the video signal. The correction circuit uses diodes which are biased to turn on at a variable dc voltage level.
The signal is normally attenuated a fixed amount by using a resistive L-pad. The diodes are normally reverse biased by equal, but opposite polarity, dc voltages. Reducing the dc voltage amplitude permits the diodes to conduct on the signal peaks. This inserts additional resistance in parallel with the series arm of the L pad thereby decreasing the attenuation. Varying the resistance in series with the diodes provides for a variable gain expansion.
4.7.1.2. Detailed Description

The input signal is applied through input jack Jl to the 90 degree splitter. One output will be routed by jumpers at E1-4 to the Quadrature Corrector the other output to the Linearity Corrector circuit. Transistor amplifier pair Q1-Q2 amplifies the signal 10 times ( 20 dB ). Q2 is a low impedance emitter follower which drives the initial gain network, CR1 through CR4. Threshold controls (TH1 and TH2) potentiometers R37 and R38 determine the turn on points of the diodes while slope controls (SL1 and SL2) potentiometers R10 and R11 vary the amount of gain expansion or compression achieved during the on period of the diodes. U1A and U1B are unity gain inverting amplifiers, with buffer amplifiers, to provide the opposite polarity dc voltage for biasing of the diodes. The 10 uH inductors, shunted by 2 k ohm resistors, isolate the IF signal from the dc circuits. Diode CR9 compensates for temperature drift in CR1-CR8. Jumpers P3 and P2 are provided in both gain networks to allow either expansion or compression functions.
Transistors Q3 and Q4 amplify the signal approximately 8 dB before it is applied to the second expansion network. Threshold controls TH1, 2, and 3 are used to adjust the differential gain in the white to black region, while TH 4 adjusts the sync amplitude.
The signal is applied to output through emitter follower Q5, matching resistor R28, and lowpass filter consisting of capacitors C22 and C23 and inductor L9. Jumpers at P6 route the output to the Quadrature Corrector or the test output J4. The linearity correction circuit may be bypassed by setting the toggle switch S1 to the Bypass position.

### 4.7.2. ICPM Corrector

Refer to sheet 2 of 839-7900-444
The gain expansion circuits of the Quadrature Corrector are identical to the Linearity circuit. Signals from the linearity and quadrature circuits are summed together by R162 and R159.
The two signals are 90 degrees apart in phase and the signal from the linearity circuit is much larger due to the low resistance of R162 ( 16 ohms ) compared to R159 ( 100 ohms ).
The resulting output is the vector sum of these two signals. A change of gain on the linearity side produces gain correction with only small change in phase of the sum vector. A change in gain on the Quadrature side produces change in phase of the carrier with little change in the magnitude of the vector sum.
Q106 has approximately 6 dB of gain. The output at J3 feeds the visual mixer.
The Quadrature Correction may be bypassed by setting switch S101 to bypass (out).

### 4.8. 1 Watt Final Amplifier

Final Amplifier - 992-8328-001
Circuit Board - 992-7093-001
Refer to schematic 839-7900-023

### 4.8.1. Functional Description

The exciter houses two identical class A final amplifiers. One amplifier is used for the sound output and one amplifier is used for the vision output. The jumper plug P1 is placed between 1 and 2 for sound service and between 1 and 3 for vision service
or dual carrier sound. This plug routes the control voltage to the input attenuator for single carrier sound AGC.

### 4.8.2. Theory Of Operation

### 4.8.2.1. RF Path

RF is input to J 1 and applied to gain stage U3 through a capacitor C31. The gain of this stage is 18 dB . The output of this stage is attenuated by a pad consisting of pin diodes CR2, CR3, and CR4. These diodes function as current-controlled resistors. Regulator U5, R1 and CR1 form a bias network for the diodes. When the jumper plug is in the 1-3 position, the fixed diode current reduces the attenuation to the 3 dB minimum value. If the jumper plug is in the 1-2 position, the AGC amplifier controls the attenuation.
After signal attenuation by the pad, the signal is then divided into two equal paths by HY1 and each path is amplified again by a 35 dB amplifier ( U 1 and U 2 ). The signal is then re-combined by HY2 to the 1-Watt power level. The signal output is through a directional coupler with a -10 dB sample port.

### 4.8.2.2. RF Sample Detection

The sample from the directional coupler located in Final Amp is applied to peak detector CR5. The DC output of CR5 will be proportional to the RF output through the directional coupler. This DC potential is applied to buffer U4C.
As diode CR5 becomes warmer with operation, it will increase conduction. This temperature effect is overcome by use of a second diode, CR6, which is of the same type as CR5 and is mounted adjacent to CR5. The potential from CR6 is applied to buffer U4D.
The voltage from U4D is subtracted from the voltage from U4C at the input to summing amplifier U4A. The output is a voltage which remains proportional to the RF output through the directional coupler, but is now compensated for temperature variations.

### 4.8.2.3. AGC Loop (Vision)

The voltage at U4 pin 1 is now routed to the VSB/IF AGC as DETECTOR INPUT where it is the sample input to the AGC differential amplifier U101. Final amplifier attenuation is fixed at minimum.

### 4.8.2.4. AGC Loop (Single Carrier Sound)

Comparator U4B compares the potential from U4A pin 1 on the non-inverting input to a power control input potential on the inverting input which is generated on the metering and control circuit board. This potential is used as a reference to adjust the output level from U4B. This potential adjusts automatic gain control loop of the sound 1 watt amplifier circuit by varying the resistance of the RF interstage pad.

### 4.8.2.5. AGC Loop (Dual Carrier Sound)

The RF power sample DC voltage is routed to the Aural Linearization card as the sample for the AGC differential amplifier U1. Final amplifier attenuation is fixed at minimum.

### 4.8.3. Alignment

There are no adjustments except the change in jumper position that determines the AGC operation. Replacement of the
unit may also require realignment of the AGC or the set-up of exciter power limits.

### 4.9. B'TSC Single Carrier Sound Circuit Board

## Refer to schematic 839-7900-479

### 4.9.1. Functional Description

A voltage controlled oscillator is modulated by the combined audio signals, and up converted to the sound channel frequency. Integrated circuit U8 is the main phase lock loop for frequency control.

### 4.9.2. Detailed Circuit Theory

### 4.9.2.1. Voltage Controlled Oscillator (VCO)

The voltage controlled oscillator consists of Q1. The tuned circuit consists of CR1 through CR6, L1, C2 and C3, C5 and C6 establish the feedback ratio across Q1 to sustain oscillation. Varactor diodes in the oscillator circuit allow the frequency of oscillation to be changed simply by changing the bias on the varactors. The VCO output is applied to buffer Q2 which provides a gain of 15 dB . The output of Q2 is routed through a resistive pad and monolithic amplifier U3 to provide high isolation for the VCO. The signal is attenuated and a sample is made before another amplification stage U4. The NE5205 amplifiers have a gain of about 18 dB . J4 is the IF output, it may be optionally group delay corrected before up conversion to the sound channel frequency.
L2, L3, C21, C22 and C23 form a low pass filter to attenuate any harmonics.

### 4.9.2.2. Phase Lock Loop

The aural IF phase lock loop (PLL) is U8. With the exception of the prescaler U 2 , it contains the programmable divide by N counter, divide by R counter, the phase detector and the lock detection circuits.
The VCO frequency is sampled by U 2 a divide by 10 or 11 dual modulus prescaler. The output of the prescaler is applied to U8 a multipurpose frequency synthesizer IC. U8 further divides the VCO frequency down to 12.5 kHz .

U18 prescales the 16 MHz input to 800 kHz and applies it to U8. U8 then further divides the 800 kHz to 12.5 kHz . The phase detector within U8 compares the two signals, the phase detector outputs are filtered and the difference is integrated by U9. The output voltage of U9 varies the bias on the varactor cathodes. This controls the average frequency of the VCO. A large change in the phase detector output will cause the diodes in parallel with R25 or R26 to conduct, this will shorten the lock time if the phase/frequency error is large due to a power. failure.
Q3, Q4 and Q5 process U8 lock detector output to drive the on board lock LED and the remote output.

### 4.9.2.3. Audio Inputs

Monaural audio is applied to buffers U19 followed by U10 which is configured as a differential amplifier to remove any common mode noise on the audio inputs. U11 is used to form the preemphasis network. The exact preemphasis curve used is determined by the selection of resistors R43, R44, R45 and R46.
Composite BTSC signal is applied to amplifiers U21 and U12 in a common mode rejecting circuit.
Subcarriers 1 and 2 are buffered, followed by a level control. Both are combined and can be summed with the monaural or composite input, depending on the position of J 7 .
The monaural or composite signals may be switched to the modulated oscillator by the CMOS switch U14. The switching is controlled by either the local switch, S 3 or by remote control contact closure.

### 4.9.2.4. Up conversion

The IF output, J4, is either routed through the aural group delay corrector or jumpered to J 3 . The following pad is 10 dB without the delay equalizer or 6 dB when the optional equalizer is used.
The local oscillator input is $\mathbf{J} 2$, the attenuated signal is amplified by U15 and drives the mixer LO input. L8 and C76 are a local oscillator trap.


Figure 4-3. Aural Converter Block Diagram

### 4.10. Aural Delay Corrector Circuit Board (Optional)

 Refer to Drawing 839-7900-492
### 4.10.1. Functional Description

The Aural Delay Corrector is provided as an option to equalize the aural rf circuits when operating through a notch diplexer. It is intended as a means of improving TV stereo operation when non-stereo type notch diplexers are used, namely, single cavity diplexers.
The Aural Delay Corrector is a passive, adjustable allpass circuit operating at the aural IF frequency of 32.5 MHz . The corrector is basically a single section allpass with two tuned resonators for equalizing the group delay error existing in the aural notch diplexer.
A bypass system is provided to allow switching the allpass section out and for switching in an adjustable pad to make up for the insertion loss of the allpass resonators. The bypass mode can be operated manually with a switch located on the board or remotely through external wiring that provides an isolated switch contact closure.

### 4.10.2. Detailed Description

The input signal path is through J1 and relay contacts 2,4 of K 1 to pin 1 the input to HY 1 , a $90^{\circ} \mathrm{PC}$ mounted hybrid. The signal is divided equally between the output pins 2 and 5 with a $90^{\circ}$ phase shift and is applied to resonators F1 and F2. The signal is reflected off the resonators and is recombined in HY1 at output pin 6. The delay equalized signal is connected to output jack J2 through bypass relay K1 contacts 6 and 8 .
The 90 degree phase shift plus the resonator phase shift, when recombined in the hybrid, provides an inverse group delay curve to that existing in the rf output notch diplexer. Slight adjustment of resonators F1 and F2 provides an adjustable level of equalization to correct the rf output group delay. Typically,
resonators F1 and F2 are tuned to have the same delay curve and then both F1 and F2 are positioned on 32.5 MHz . A slight adjustment of either F1 or F2 will then flatten out or peak up the overall delay response curve as required for equalization.
An adjustable rf pad consisting of R1, R2 and R3 is used to match the insertion loss of the allpass circuit when the aural delay corrector is switched in and out of the aural IF path. Adjusting R3 provides about 6 dB of level adjustment between -2 and -6 dB insertion loss points to maintain nearly equal operating levels in either normal or bypass modes.
In the operating mode, bypass relay K 1 is de-energized (drawing 837-7900-026 shows the de-energized mode).
To bypass the corrector, switch S1 grounds the bottom of K1 coil through CR2 to activate K1, bypassing the resonators and switching in the rf pad. +15 VDC is applied to the coil of K 1 through R4. CR1 bypasses coil transients and CR3 absorbs power supply transients.
Bypass switch S1 also activates the bypass board LED indicator on the front panel of the exciter through CR4. The bypass indicator line can be disabled for prolonged operation in the bypass mode without illuminating the front panel LED, if desired, by moving patch pin Pl from 2,3 contacts to 2,1 . Normal operation requires P1 to be in 2,3 position for proper front panel LED indication of the aural corrector bypass mode. CR5 isolates the switch contacts for remote control operation. The bypass mode can be activated remotely through an isolated contact closure wired to pins E1 and E2. A holding contact between E1 and E2 holds bypass relay K1 energized, bypassing the aural delay corrector. An open contact releases K1 for normal operation. Note, when S1 is in the bypass mode, remote operation is deactivated. Remote operation requires local switch S1 to be in the normal operating position.

### 4.11. VHF Synthesizer Card 1

Refer to schematic 839-7900-528

### 4.11.1. Circuit description

The VHF synthesizer card 1 performs two basic tasks:
a. Creates all the reference frequencies used by the phase locked loops from on board 10 MHz standard or an externally applied 5 or 10 MHz PFC input.
b. Creates IF frequency for the modulator of 37 MHz for system M or 38.9 MHz for system B.

### 4.11.2. Detailed Circuit Description

### 4.11.2.1. 10 MHz Generation

10 MHz is the main reference frequency used by the synthesizer. Used to create all other reference frequencies. The 10 MHz has two primary sources, the on board OCXO or the PFC input. On board detection circuits sense the presence of a PFC input and automatic switching is used to select the appropriate 10 MHz signal.
PFC input of either 5 or 10 MHz applied to J 5 is buffered by Q4 and amplified in a class $C$ amplifier Q5. The output of this class C amp is rich in harmonics. A tuned circuit consisting of C 20 and L 1 and a series tuned 10 MHz crystal Y1 selects the 10 MHz harmonic. The level of 10 MHz is detected by CR 5 and compared by U3. If there is sufficient 10 MHz level U3's output goes low and drives a PFC indicator DS1. U3 also drives a switchable 15 V voltage regulator. When PFC is present the regulator is shut down and consequently shuts down on board

10 MHz OCXO Y4. If there is an insufficient level of the PFC input, then U3 will select on board 10 MHz OCXO Y4 by powering up the switchable voltage regulator U 1 , which in turn powers up the OCXO. The actual selection of the 10 MHz signal, be it either the PFC input or on board standard, is performed by U4 configured as a SPDT switch. The output of this switch is the primary 10 MHz signal and used to create all other reference frequencies.

### 4.11.2.2. 5 MHz Generation

The primary 10 MHz signal from U4 is distributed by a buffer U5 to other parts of the card. One output is applied to J 3 for future use. A second output is divided by 2 in U6 to create a 5 MHz reference frequency and is applied to Jl . The third output creates the 800 kHz reference frequency.

### 4.11.2.3. 16 MHz Generation

10 MHz from U5 is divided by 5 in U7. The output of U7 is a $20 \%$ duty cycle pulse train at 2 MHz . This pulse train has high harmonic content. A tuned circuit consisting of L4 and C26 and a series 8 MHz crystal Y 2 selects the fourth harmonic or 8 MHz . The 8 MHz signal is full wave rectified or doubled by U 8 to create the 16 MHz reference frequency. Tuned circuit L5 and C 28 and a series tuned 16 MHz crystal Y3 performs further filtering of the 16 MHz . The 16 MHz signal is buffered by U 9 and applied to J4.


Figure 4-4. VHF Synthesizer Card I Block Diagram

### 4.11.2.4. 800 kHz Generation

A second output of the 8 MHz signal is buffered by U9 and then divided by 5 in U10 to create 1.6 MHz . This 1.6 MHz is divided by 2 in U6 to obtain 800 kHz and is then applied to J 2 .

### 4.11.2.5. IF Generation

A PLL generates the IF carrier for the modulator. This PLL uses a mixing technique where the VCO frequency is mixed with a harmonic of the 10 MHz reference and then locked to the 800 kHz reference. Using the mixing technique reduces the total divider ratios and improves the phase noise performance.
U 14 contains both the VCO and mixer. The tank for the VCO is formed with L15, C38 and the varactor diodes CR4, CR14 and CR15. The VCO frequency is mixed with the 3rd harmonic of 10 MHz . The 10 MHz applied to U14 via a square wave with good 3rd harmonic content. Tank circuit L7 and C107 peak the 30 MHz level.
The output of U14 is the difference between the 30 MHz and the VCO frequency, typical 7 MHz for a 37 MHz IF or 8.9 MHz for a 38.9 MHz IF. A band pass filter follows U14 to remove. any unwanted mixer products. This filter consists of L6, L8, L20, C110, C111 and C112.
The filtered 7 to 9 MHz signal is amplified by U 13 and applied to a programmable divider chip U 2 .
The programmable divider chip U2 also receives the 800 kHz reference frequency. Both the 800 kHz reference and the mixed VCO frequency are divided down to 100 kHz . A phase/frequency comparitor within U 2 compares the phase of the two 100 kHz signals. Any difference in the frequency or phase is
detected and output as a pulse whose duty cycle is equal to the phase difference. U11 integrates these pulses to create a DC control voltage proportional to the phase difference. This DC control voltage is used to lock the VCO to the desired frequency.
A passive low pass filter is used on this control voltage to remove any 100 kHz that might be present after the integrator. This filter consists of C121, C123, C125, C126, C122, C124, L9, L10 and L11.
The VCO frequency is sampled and buffered by Q1 and amplified by U15, Q2 and Q3. A low pass filter centered about the desired IF frequency removes any harmonics and unwanted spurs. This band pass filter consists of $\mathrm{C} 138, \mathrm{C} 137, \mathrm{C} 134$, C139, C140, C135, C136, L17, L18 and L19.
Lock detection is accomplished by U3 and its output mutes the exciter in the event of loss of lock.

### 4.12. VHF Synthesizer Card \#2

Refer to schematic 839-7900-529

### 4.12.1. Circuit Description

The VHF synthesizer card 2 performs the task of generating the LO used to convert the visual and aural IFs to carrier. It contains a main PLL loop that runs from 150 to 300 MHz in 5 MHz increments and a rachet PLL loop that runs from 10 to 15 MHz in 10 kHz increments. The main loop's VCO is offset by the rachet loop in a SSB mixer prior to phase detection. This allows the final frequency to cover the 150 to 300 MHz range in 10 kHz increments. For low band channels the main loop's


Figure 4-5. VHF Synthesizer Card 2 Block Diagram
output is divided by two yielding a frequency range of 75 to 150 MHz in 5 kHz increments.

### 4.12.1.1. Detailed Circuit Description.

### 4.12.1.1.1. 10 to 15 MHz Rachet Loop

The frequency of the rachet loop is such that the difference of the desired LO minus the rachet frequency yields a frequency divisible by 5 MHz .
The primary rf source is a 95 to 150 MHz VCO U5. U5's output is buffered by a 6 dB pad U12 and split into two paths by hybrid HY1. One path is amplified 18 dB by U 9 and applied to a divide by $10 / 11$ dual modulus prescaler U7. The output of the prescaler is applied to a programmable divider U6 where the VCO frequency is divided down to 100 kHz .
An 800 kHz reference signal from card 1 is applied to J 2 and then to the programmable divider U6 where it is also divided down to 100 kHz . A phase frequency detector within U6 compares the phase of the two 100 kHz signals. Any difference in the frequency or phase is detected and output as a pulse whose duty cycle is equal to the phase difference. U2 integrates these pulses to create a $D C$ control voltage proportional to the phase difference. The VCO is locked to the desired frequency by this DC control voltage.
A passive low pass filter is used on this control voltage to remove any 100 kHz that might be present after the integrator. This filter consists of C33, C34, C35, C36, C37, L2 and L3.
Potentiometer R13 sets the gain of the loop for best stability and rejection to microphonics.
The other output of hybrid HY1 is amplified 18 dB by U10, divided by 5 by U8, and then divided by 2 by U4. This total division of 10 yields a frequency range of 9.5 to 15 MHz in 10 kHz increments. The divided output of U 4 is filtered by a 21.4 MHz low pass and then buffered by a 6 dB pad U13 and 12 dB amplifier U22.
Lock detection is accomplished with U1 and its output is used to mute the exciter in the event of a loss of lock.

### 4.12.1.1.2.SSB Mixer

A single side band mixer is used to offset the main loop VCO's frequency by the rachet loops frequency. This SSB mixer consists of mixers U 16 and $\mathrm{U} 17,90$ degree hybrids U 2 and U 3 , a 0 degree power combiner U18, and attenuators U23 and U19.
The main loop's VCO signal is applied to one 90 degree hybrid and the rachet loop's signal to the other 90 degree hybrid. The hybrid outputs are then mixed in the two mixers, which produce two primary outputs at the sum and the difference frequencies. When the mixers create these sums and differences, the sum signals are in phase but the difference frequencies have a 90 degree relationship with each other. This 90 degrees from the mixers plus the 90 degrees from the hybrids add and create a 180 degree difference. By phasing the hybrids correctly the output of the two mixers will have both lower side bands in phase but the upper side bands will be 180 degrees out of phase. When combined in the 0 degree combiner U18 the lower side bands will add and the upper side bands will cancel. The lower side band or difference frequency is then buffered and amplified 18 dB by U 20 .
4.12.1.1.3. Main 150 to 300 MHz PLL

A 150 to $300 \mathrm{MHz} \mathrm{VCO} \mathrm{U30} \mathrm{is} \mathrm{the} \mathrm{primary} \mathrm{signal} \mathrm{source} \mathrm{for}$ the main PLL. U30's output is buffered by a 6 dB attenuator U32 and then split into two paths by hybrid U32. One path is divided by 1 or 2 by U35, depending on the required frequency, then amplified 12 dB by U36 and routed to the LO output J3. The other VCO output from splitter U32 is amplified 12 dB by U33 and routed to the SSB mixer.
The output of the SSB mixer is applied to a programmable divider U 27 which divides the main VCO frequency to 5 MHz . The output of this divider is one pulse for ever N input pulses. This small pulse is to narrow for good phase detection and must be stretched. The output of the counter is divided by 2 in U28 which yields a $50 \%$ duty cycle square wave. The square wave is then applied to a one shot monostable multivibrator U29 that triggers on both positive and negative edges. The multivibrator's output is twice the frequency of the input and cancels the divide by 2 of U 28 , the pulse width is 20 nsec . This 5 MHz pulse train is applied to the phase frequency comparitor U24.
The 5 MHz reference from card 1 is applied to Jl and then to phase frequency comparitor U 24 where the phase of the two 5 MHz signals is compared. Any difference in the frequency or phase is detected and output as a pulse whose duty cycle is equal to the phase difference. U25 integrates these pulses to create a DC control voltage proportional to the phase difference. It is this DC control voltage that is used to lock the VCO to the desired frequency.
A passive low pass filter is used on this control voltage to remove any 5 MHz that might be present after the integrator. This filter consists of C58, C57, C56, C53, C54, C55, L5, L6 and L7.
Potentiometer R44 is used to set the loop gain for best stability and rejection to microphonics.
Lock detection is accomplished with Ul and its output is used to mute the exciter in the event of a loss of lock.

### 4.13. Metering and Control Circuit Board

Refer to 839-7900-027
The purpose of the metering and control circuit board is to provide status outputs to the user interface, drive the LED's on the front panel of the exciter, it interfaces the switches with the control logic, and provides the exciter power output control. Sheet 1 of the schematic diagram is divided into the visual portion on top and the aural portion on bottom.

### 4.13.1. Visual Power Control Circuit

The control circuit consists of a 12-bit digital-to-analog converter U15 and a 12-bit up-down counter consisting of U9, U10, and U11. The up-down counter is clocked up and down via U7. U7 is a low-frequency oscillator which can oscillate at two frequencies. U7 begins operation at a low frequency and after a period of time, it changes to a higher frequency.
If one of the VISUAL POWER switches is depressed, the logic gates consisting of U1 and U2 allow the oscillator output to clock the up-down counter. When a RAISE or LOWER switch is not pressed, the logic inhibits the clock. A series of Schmitt triggers (U6) detects when a RAISE or LOWER switch has been pressed and forms a time delay circuit with R4 and C 1 . Before the time delay expires, the clock is allowed to
run at low frequency. After the time delay has expired, the clock frequency is increased. This dual frequency circuit allows small increments of power to be accomplished easily and also allows large power changes without delay.
Diode CR1 discharges capacitor Cl when the switch is released and returns the clock to slow operation. The timing sequence will start over again when a switch is again pressed.
The output of the up-down counter drives U15 which converts the digital input to an analog voltage output. The analog voltage output of U15 is applied to buffer amplifier U17 and CMOS muting switch U19. During normal operation, the power control potential is routed to the visual power amplifier through the closed contacts of U19. If the switch is open, the power amplifier will be muted.

### 4.13.2. Aural Power Control Circuit

The control circuit consists of a 12-bit digital-to-analog converter U16 and a 12 -bit up-down counter consisting of U12, U13, and U14. The up-down counter is clocked up and down via U8. U8 is a low-frequency oscillator which can oscillate at two frequencies. U8 begins operation at a low frequency and after a period of time, it changes to a higher frequency.
If one of the AURALPOWER switches is depressed, the logic gates consisting of U4 and U5 allow the oscillator output to clock the up-down counter. When a RAISE or LOWER switch is not pressed, the logic inhibits the clock. A series of Schmitt triggers (U20) detects when a RAISE or LOWER switch has been pressed and forms a time delay circuit with R15 and C5. Before the time delay expires, the clock is allowed to run at low frequency. After the time delay has expired, the clock frequency is increased. This dual frequency circuit allows small increments of power to be accomplished easily and also allows large power changes without delay.
Diode CR2 discharges capacitor C5 when the switch is released and returns the clock to slow operation. The timing sequence will start over again when a switch is again pressed.
The output of the up-down counter drives U16 which converts the digital input to an analog voltage output. The analog voltage output of U16 is applied to buffer amplifier U18 and CMOS muting switch U19. During normal operation, the power control potential is routed to the aural power amplifier through the closed contacts of U19. If the switch is open, the power amplifier is muted.

### 4.13.3. Metering Circuit

The metering portion of the exciter is detailed on page 2 of the schematic diagram.
The VISUAL POWER and AURAL POWER switches (S5 and S6) operate a bi-stable flip-flop consisting of U21. The flip-flop selects through CMOS switch U22 whether visual power or aural power will be monitored. LED DS13 or DS14 will illuminate to indicate which switch has been selected.
DC potentials representative of aural or visual power (as selected) are routed through U22 to analog display U23/U24 and U25. Analog-to-digital converter U25 converts the analog voltage input to a digital level and drives the $31 / 2$ digit main display (DS1 and DS2).
-3The lower portion of page 2 of the schematic diagram interfaces the IF lock, interfaces the master lock, details the logic that drives the front-panel LED's, and provides the outputs for remote control.

### 4.14. Main Power Supply

Refer to 839-7900-504
The power supply is located in right rear area of the main chassis. AC power is input to the exciter through an ac line filter and circuit breaker/switch. A fan, connected to the ac input potential, operates whenever power is switched on. Terminal board TB1 and a power transformer with five primary windings allows a wide selection of operational voltages in the 120 and 240 volt range.
All dc supplies in the exciter are full-wave rectified, filtered, and regulated for stable operation. The dc potentials are distributed throughout the exciter for operation of the internal circuitry. Certain potentials are re-regulated on some circuit boards to assure stable operation of certain critical circuits.

### 4.14.1. Positive 24 Volt Supply

A 24 -volt winding of transformer T1 is full-wave rectified by bridge rectifier CR1 into a +29.2 volt dc source. This potential is regulated into a stable positive 24 -volt supply at 2 amperes by U1. Diode CR9 protects the regulator from a reverse polarity potential applied to the output and diode CR4 protects the regulator from a short circuit on the regulator input. R16 provides a means to adjust the output of the regulator. Capacitor C6 prevents oscillation of the regulator and the capacitors on the output filter high frequency ac components.

### 4.14.2. Positive and Negative 15 Volt Supplies

A 32-volt winding of transformer T1 is full-wave rectified by bridge rectifier CR2 into a +20.2 and a -20.2 volt dc source. These potentials are regulated into stable positive and negative 15 -volt supplies at 2 amperes by U2 and U3. Diodes CR 10 and CR11 protect the regulators from a reverse polarity potential applied to the output and diodes CR5 and CR6 protect the regulators from a short circuit on the regulator inputs. R17 provides a means to adjust the output of the positive regulator and R18 provides a means to adjust the output of the negative regulator. Capacitors C7 and C8 prevent oscillation of the regulators and the capacitors on the output filter high frequency ac components.

### 4.14.3. Positive and Negative 5 Volt Supplies

A 17-volt winding of transformer T 1 is full-wave rectified by bridge rectifier CR3 into a +10.4 and a -10.4 volt dc source. These potentials are regulated into stable positive and negative 5 -volt supplies at 2 amperes by U4 and U5. Diodes CR12 and CR13 protect the regulators from a reverse polarity potential applied to the output and diodes CR7 and CR8 protect the regulators from a short circuit on the regulator inputs. R19 provides a means to adjust the output of the positive regulator and R20 provides a means to adjust the output of the negative regulator. Capacitors C9 and C10 prevent oscillation of the regulators and the capacitors on the output filter high frequency ac components.

## SECTION V MAINTENANCE

### 5.1. Introduction

This section provides general maintenance information, electrical adjustment procedures, and troubleshooting information for the VHF TV exciter. It is strongly suggested that each procedure be read through completely before attempting any adjustments.

### 5.1.1. Safety Considerations

Only low potentials are present on the circuit boards within the VHF TV exciter $(+24,+/-15,+/-5)$, however primary power is present in the shielded cage in the right rear of the unit. This area should be covered during troubleshooting to prevent accidental contact with the primary line potential. The information contained in this section should be performed by trained and experienced personnel. Good judgment, care, and common sense are the best accident preventives.

### 5.1.2. Routine Mechanical Maintenance

All electronic equipment is more stable if it is kept cool. Routinely verify the exciter cooling fan is operating. There is a fine mesh RF filter located between the fan and the exciter chassis. It is important that this filter be kept clean. It can be removed for cleaning by removing the four fan mounting screws. New exciters have captive nuts for the screws. Wash filter with soap and water and reassemble.
Other accumulations of dirt may be removed with a vacuum cleaner. Do not use high pressure compressed air.

### 5.2. Vision Path Adjustments

The transmitter is very stable, investigate the possibility that another problem exists before major adjustments are made. Problems might include:
a. Exciter fan failure or a dirty fan filter causing the exciter to overheat due to reduced air flow.
b. A change in exciter power supply voltage. Refer to power supply alignment procedure near the end this section.
c. Any change in RF amplifier gain due to a soft failure could change the needed drive level or require a different amount of correction.
Investigate these possibilities before changing the correction.

### 5.3. Vision Adjustment Sequence

The exciter is factory tuned and tested and is ready for operation in the transmitter. Normal VISUAL adjustment consists of a brief check of the basic performance (items 1-3 in Table 5-1).
Then pre-correction and level matching for the transmitter (items 4-12 in Table 5-1) should be carried out in the order shown.

### 5.3.1. Optional Notch Diplexer Unity Gain

The purpose of this procedure is to set the Video gain of the Notch Diplexer EQ module to unity. If you do not have the Notch Diplexer EQ module, skip the following steps and move on to the Video Input/Diff Gain board adjustments.
The Notch Diplexer EQ was factory set for proper compensation of the diplexer if equipped - no adjustment should be necessary.
a. Place Notch Diplexer Module on extender.
b. Apply modulated staircase test signal to exciter.
c. Set S1 to bypass.
d. Measure video input level at TP2 with a high frequency scope and note the voltage.

Table 5-1. Visual Adjustment Sequence

| Procedure | See | Section |
| :--- | :--- | :--- |
| 1) Check video level | Video Input Set Up | 5.3 .2 .1 |
| 2) Check depth of modulation | Depth Of Modulation | 5.3 .3 |
| 3) Check exciter swept response | Response Equalizer | 5.3 .6 |
| 45) Adjust ICPM | Quadrature Corrector | 5.3 .11 |
| 5) Differential gain coarse adjustment | IF Linearity Correction | 5.3 .11 |
| 6) Differential gain fine adjustment | Video Differential Gain | 5.3 .2 .2 |
| 7) Luminance linearity correction | Luminance Linearity | 5.3 .3 .3 |
| 8) Adjust differential phase | Differential Phase Corrector | 5.3 .13 |
| 9) Adjust group delay | IF Delay Compensation | 5.3 .14 |
| 10) Recheck sync level | Video Input Set Up | 5.3 .2 .1 |
| 11) Recheck depth of modulation | Depth of Modulation | 5.3 .3 |
| 12) Adjust power limits | Power Limit Control | 5.3 .17 |

e. Observe video output at TP6 and set R65 for unity gain across module.
f. Set S1 to normal (correction in).
g. Set R3 for unity gain at TP6 compared to TP2.
h. Observe video at TP6 on a vectorscope or waveform monitor and set R43 for best differential gain.
i. Proceed to video input board gain adjustments

### 5.3.2. Video Differential Gain/Low Frequency Linearity Board Adjustments

### 5.3.2.1. Video Level Adjustment

a. Apply a IVp-p staircase luminance only video signal to the exciter video input.
b. Set the following bypass switches to OUT: differential gain corrector, low frequency (LFL), notch diplexer equalizer, receiver equalizer and differential phase corrector.
c. Connect a scope to the video monitor output on the Diff Phase board. J2 must be terminated with 75 ohms.
d. Adjust R1 for the correct level of the video component and R2 for the correct sync amplitude. Sync plus video should equal one volt peak to peak.
e. Check to verify that the IF Linearity, Quad corrector, and Differential Phase switches are in the IN position and that the initial adjustments have been completed.

### 5.3.2.2. Correction For Differential Gain.

## Refer to Figure 5-1 below

a. Select the differential gain display on the vectorscope. A waveform monitor with a subcarrier bandpass display may be used. It will be more difficult to view the small changes in differential gain.
b. Apply a lVp-p staircase or ramp video signal with chroma to the exciter video input.
c. Set the BYPASS (DIFF GAIN) switch to the IN position.
d. Start with all differential gain controls maximum CCW.
e. Adjust the sections of white compression or white expansion as needed. The goal is to straighten the vector-
scope display of differential gain. The threshold controls determine the starting point of the correction and the slope controls the amplitude of the correction.

### 5.3.2.3. Correction For Luminance Linearity Error

Set the BYPASS (LFL) switch to the IN position.
a. Monitor the transmitter output with the demodulator connected to a waveform monitor and vectorscope.
b. Place the waveform monitor in the differentiated step mode.
c. Start with all LF linearity controls maximum CCW.
d. Adjust the sections of white compression or white expansion as needed. The goal is equal amplitude of all the differentiated steps. The threshold controls determine the starting point of the correction and the slope controls the amplitude of the correction.
e. Adjust CW the threshold control to set the point at which correction begins, if this point is not visible increase the slope.
f. Adjust the slope control to change the amplitude of the correction.
g. Adjust R2 for the correct sync level.

### 5.3.3. Depth of Modulation

## Refer to Figure 5-2

Check the depth of modulation and adjust if needed. Depth of modulation is adjusted by R12, the MOD BIAS control on the MOD/DELAY board. Use MOD BIAS and SYNC LEVEL R2 to attain proper video levels at the transmitter output. Any further video level adjustments for program levels shall be done with R1, video gain on the video card.
Differential gain and low frequency linearity adjustments may have an affect on frequency response and group delay, check these parameters after the transmitter gain and linearity corrections have been made and trim the adjustments as needed.


Figure 5-1. Diff. Gain, Effect of TH and SL Controls


Figure 5-2. Depth of Modulation

### 5.3.4. Video input board alignment procedure

NOTE: For transmitter correction adjustment refer to the previous section. The alignment procedure is for boards that require a total alignment due to repair etc.

### 5.3.4.1. Initial System Setup

## Refer to Table 5-2

Set JP1, JP2 and JP4 for NTSC or PAL.
Set JP5 for AC or DC coupling to ground or float the video input cable shield. Floating the shield may help with common mode signals caused by ground loops for example.

### 5.3.4.2. Control Presetting

a. Turn off Differential Gain and Low Frequency Correctors to correctly align the board, by setting S1 and S2 to OUT. Temporarily install video card in exciter using extender card.
b. Turn off white clipping by turning R71 fully counterclockwise (CCW).
c. Apply 1.0 volt p -p video to the input at J 1 from a video test signal generator.
d. Using an oscilloscope monitor the voltage at TP4 and adjust R1 for a 1.1 volt p-p level.
e. Check TP8, the generated burst pulses should be 1.7 volts p-p.
f. Check TP6, the regenerated sync pulse amplitude should be 5 volt p-p.

### 5.3.4.3. Loss of Video Adjustment

The following potentiometers are 4 turn.
a. Turn R106 and R111 fully CCW.
b. Adjust R141 until U17 locks and the loss of video indicator DS1 is off. Adjust R141 to be half way between the two points where DS1 illuminates, indicating loss of video.
c. Temporarily remove video to check loss of video operation, DS1 should illuminate.
5.3.4.4. Sync Removal Adjustment
a. Preset R110 full clockwise (CW) and R105 full CCW.
b. Monitor TP7, sync-clipped video, with an DC coupled oscilloscope.

| SYSTEM | NTSC | PAL |
| :---: | :---: | :---: |
| JP1 | $3-2$ | $1-2$ |
| JP2 | $1-2$ | $3-2$ |
| JP4 | $1-2$ | $3-2$ |
| COUPLING | AC | DC |
| JP5 | $3-2$ | $1-2$ |
| GROUNDING | GROUND | FLOAT |
| JP3 | $1-2$ | $3-2$ |

c. Adjust R131 until the waveform in Figure 5.3 is obtained. This adjustment will move most of the sync pulse to the blanking level.
d. Adjust R110 and R105 until a sync-free waveform as shown in Figure 5-4 is obtained.
e. R105 will remove any glitch if present just before burst. Be careful to only remove the glitch, not the burst.
f. R110 will remove the sync.
g. Readjust R131 until the blanking level is flat.
h. Adjust R124 to set the blanking level to 0.0 volts DC.
i. Recheck for flatness in the blanking level, readjust R131 if needed.
5.3.4.5. Sync Level Adjustment

Adjust R2 for approximately 700 mV p-p of sync at TP5.

### 5.3.4.6. Frequency Response and Group Delay

Use one of the following procedures.


Figure 5-3. Sync Removal


Figure 5-4. Blanking Level Flatness

### 5.3.4.6.1. VM700 alignment procedure.

If a VM700 is available, connect the video card output test jack J2 to the VM700, terminate the input with 75 ohms.
a. Select a $\sin X / X$ generator signal.
b. Select Group Delay and $\operatorname{Sin} \mathrm{X} / \mathrm{X}$ from the measurement menu of the VM700.
c. The response and group delay of the board are being adjusted. Use the VM700 Relative-Reference mode for best accuracy.
d. First adjust R115 for best compromise between group delay and response.
e. Adjust R120 for best frequency response.
f. Adjust R157 for best group delay.
g. Repeat steps e and funtil the required response and group delay is achieved.

### 5.3.4.6.2. Waveform monitor procedure

a. Select a multiburst test pattern signal.
b. Adjust R115 for the flattest response as observed on the waveform monitor.
c. Select a Multipulse or other group delay measuring signal from the generator.
d. Adjust R115 for a best compromise for group delay and response, repeating steps $a$ and $b$ as needed.
e. Adjust R120 for best frequency response.
f. Adjust R157 for best group delay.
5.3.4.7. Sync Parameter Adjustment
a. Observe video and reinserted sync at TP5.
b. Adjust front porch duration with R111.
c. If a glitch appears at the leading edge of sync, readjust R111 until it just disappears and the timing is still in within specification.
d. Adjust sync duration with R106.

### 5.3.4.8. White Clip Adjustment

a. Select a staircase or ramp signal from the generator that has $100 \%$ luminance.
b. Increase video level with R1 until luminance level is higher than the desired clip level.
c. Adjust R71 clockwise to set the luminance white clip to the desired level, such as $110 \%$.
d. Reset R1 for $100 \%$ luminance level.


Figure 5-5. Modulator Output Waveform
e. Differential gain and low frequency linearity adjustments may have an affect on frequency response and group delay, check these parameters after the transmitter gain and linearity corrections have been made and trim the adjustments as needed. Video and sync level final adjustments may be set with R1 and R2.

### 5.3.5. Visual Modulator Alignment Procedure

a. This procedure adjusts the modulator output level and modulation depth. It is assumed that the modulator has not previously been set-up, is badly out of adjustment, or components have been replaced.

1. Set IF drive control fully CW.
2. Set modulator FREQ and $Q$ controls fully CCW.
3. Set VIDEO DR (DRIVE) control and MOD BIAS control to mid-range.
4. Proper adjustment of the MOD BAL (BALANCE) control requires a demodulator with a display of ICPM. If this control has previously been adjusted, do not disturb its setting. Otherwise, set this control for mid-range, then refer to MOD BAL adjustment after completing this level and ratio adjustment.
5. Apply a IV p-p luminance only ramp/staircase to the exciter video input. Set VIDEO GAIN, R18, on the Video Input/Diff Gain board for 1 V p-p at J 2 on the Diff Phase board ( J 2 must be terminated in 75 ohms).
6. Set jumper P1 to the MOD TEST POSITION (P1 2-3) on the MOD/DELAY COMP board. Connect the modulator PC board test output, J 2 , to the input of a high frequency oscilloscope (BW 50 MHz ). Terminate in 50 ohms.
7. Adjust the modulator video level control for 700 mV at peak of sync and mod bias control for 88 mV p-p at white for CCIR - M ( $12.5 \%$ ratio) or $70 \mathrm{mVp}-\mathrm{p}$ at white for CCIR - B ( $10 \%$ ratio). See Figure 5-5. The two controls interact so it will be necessary to go back and forth until both conditions are achieved at the same time.
8. Restore jumpers and cables to normal.
b. Although the setting of the IF DRIVE control is not critical, some adjustment may be desirable to improve linearity. This procedure assumes the modulator ratio is set up properly.
9. Apply a modulated staircase/ramp to exciter input.
10. Observe demodulated exciter output on a vectorscope (or band-limited sub-carrier on a waveform monitor).
11. Adjust IF DRIVE, R1, for best differential gain.
c. Modulator Balance

This adjustment should not normally be required unless a modulator component is replaced or a new unadjusted PC board is installed. Before attempting this adjustment, insure that the modulator set-up adjustments have been accomplished.

1. Apply a five step staircase to the exciter video input.
2. Switch out all exciter correction by setting to bypass.
3. Demodulate the exciter output and observe incidental phase on a WFM.
4. Adjust mod balance control for a minimum incidental phase at white.
. Readjust MOD BIAS for correct modulation depth at white. See Figure 5-2.
5. If the diffferential phase was PREVIOUSLY adjusted, the transmitter differential phase and ICPM may need to be adjusted when the exciter is returned to operation.
d. Check swept response at the output of the exciter and
5.3.6. Response Equalizer Adjustments Wuteh ady ustmo Three controls make up the Response equalizer on the Modulator. See Figure 5-6.
a. Slope control - used to tilt the entire sweep waveform from -0.75 to 4.18 MHZ
b. Q and FREQUENCY (the other two controls) work together and are usually used to correct for response problems around the carrier (if needed at all).
These controls should be used only to flatten the exciter frequency response and not to correct tuning errors elsewhere.
If no equalization is required, the $Q$ and FREQUENCY controls should be set fully CCW. This effectively removes them from the circuit. This adjustment procedure assumes that the modulator has been previously adjusted for the proper output level and modulation depth. If this has not been done, perform modulator set-up before proceeding.
Large amounts of equalization ( 1 dB ) are not normally required. However, large amounts of correction (if used) will attenuate the modulator board output level and may require readjusting the video level control to restore the correct modulator output level.

### 5.3.6.1. Adjustment Procedure

a. Apply sync pulse video sweep $(0-5 \mathrm{MHz})$ to the exciter video input.
b. Observe swept response of exciter output. The VSB IN/OUT switch should be set to OUT. Set DELAY COMP IN/OUT switches to out.
c. Set modulator Q and FREQ controls fully CCW. Swept response should be only slightly tilted at this time.
d. Use the Slope control to take out as much tilt as possible (level up the -0.75 and 4.18 markers).
e. If response is flat, leave Q and FREQ fully CCW (this effectively takes them out of circuit).
f. If the -0.75 and 4.18 MHZ markers are even but there is a response problem in between them, adjustment of $Q$ and FREQ will be necessary.
g. Adjust modulator Q control partially CW and then adjust the FREQ control until changes in the passband response are evident. Watch the area below carrier it may take several turns.
h. Using the least possible clockwise rotation of the Q control, alternately adjust Q, FREQ and Slope of the
Lur modulator section for the flattest response from -0.75 MHz to +4.18 MHz . Switch in VSB and touch up response if necessary

### 5.3.7. VSB Filter Gain Adjustment

a. The PAD control, R7, adjusts the VSB filter circuit for unity gain as the filter is switched in and out.
b. Set the exciter for minimum power out.
c. Set jumper J101 to MANUAL position. Raise exciter power to a nominal power. Note the exciter power reading with the VSB filter in.
d. Switch VSB out and set the PAD control, R7, on the VSB/AGC board, for the same power level observed when the filter was in.
e. Switch VSB to IN, and set jumper, J101, back to AUTO.

### 5.3.8. IF AGC Adjustment

This adjustment sets the amount of headroom in the IF AGC circuit, and prevents overshoots in drive level after a loss of drive.
If readjustment is necessary perform the following steps after the Power Limit Adjustment.
a. Connect a DC VOM to TPl on the VSB/AGC board.
b. Bring the transmitter up to normal operating power.
c. Turn the IF AGC control (on the VSB/AGC board) fully CW for maximum voltage at TP1, and note the voltage.
d. Now turn the IF AGC control CCW until the voltage at TP 1 is $20 \%$ less than the maximum voltage noted in the previous step.

### 5.3.9. Depth Of Modulation

This procedure assumes video input set up has been performed and modulator alignment is intact. This check of the exciter for luminance modulation may be performed to establish a starting point in total transmitter set up. This procedure may also be used looking at total visual transmitter output to correct shift in modulation level due to linearity correction.


Figure 5-6. Modulator Q \& Frequency Adjustment Effects
a. If checking exciter only, connect exciters VIS RF output through attenuators to a demodulator, then set linearity and quad correction to bypass (out).
If checking transmitter output all linearity adjustment should have been previously done and correction left in the state normally used for transmission.
b. Apply $1 \mathrm{v} p-\mathrm{p}$ video with luminance ramp to exciter video input.(or use program V.I.T.S. containing a $12.5 \%$ luminance reference.)
c. Observing demodulated video with zero-carrier reference set luminance level to $12.5 \%$ using the MOD BIAS control R12. BE SURE TO ADJUST ONLY THE BIAS. A complete modulator alignment will be required if any other controls are disturbed.

5.3.10. IF Linearity and Quadrature Correction (Coarse Differential Gain and ICPM)

2 switches
The following adjustments should be used to correct for differential gain and ICPM that is normally introduced in a transmitter. Keep in mind that the IF linearity adjustment is a coarse adjust. The fine adjust will come from the Video differential gain adjustments on the Video input board to be adjusted later. These adjustments should be made after the transmitter is at operating power, and any AGC or drive attenuator adjustments which might effect drive required have already been accomplished. IF Linearity and ICPM adjustments do interact.

### 5.3.10.1. Control Presets

a. Apply modulated stairstep signal to the video input.
b. On linearity corrector, set TH-1 through TH-4 (threshold) fully CCW. Set SL-1 through SL-4 (slope) to midrange. Set NORMAL/BYPASS switch to NORMAL (IN).
c. On Quadrature Corrector, set TH-1, through TH-4 (threshold) fully CCW. Set SL-1 through SL-4 (slope) to midrange. Set NORMAL/BYPASS switch to NORMAL (IN).
d. Adjust VISUAL POWER control for $100 \%$ power out- $h$ put.
e. The thresholds will become active first in the sync or black region and will appear to walk across the vector scope display as you turn the control clockwise. The objective in this correction sequence is to place the breakpoints at the required level between sync and white then adjust the amount of gain or phase change using the slope control for each section of the corrector.

### 5.3.10.2. ICPM Correction

Using a synchronous demodulator with a quadrature video output, monitor ICPM and perform the following steps on the Quadrature Corrector:
When a section of correction doesn't seem to work well, set its controls to maximum CCW and continue with other sections of the corrector. Many times the two sections that work the best will be all that is needed. The ICPM correction and IF Linearity correction do interact and adjustment may require more than one interation of each corrector adjustment.
a. Adjust TH-1 and SL-1 for optimum incidental phase in the white to gray region.
b. Adjust TH-2 and SL-2 for optimum incidental phase in the gray to black region.
c. Adjust TH-3 and SL-3 for optimum incidental phase in the black region.
d. Adjust TH-4 and SL-4 for optimum incidental phase in the sync region.
If the direction of phase correction is not in the direction needed to counteract the transmitter shift you may reverse the jumpers at P1 on the IF linearity section of the corrector to reverse the direction of phase shift of all TH and SLOPE CONTROLS. Connecting P1 1-2 and 3-4 generally provides the direction of shift needed to compensate the Harris solid state HT series units.
Jumpers P101 and P102 on the quad section reverse the phase of ONLY TH-2 and TH-4, and may help in case of S shaped phase distortion curves.

### 5.3.10.3. IF Linearity Adjustments

Make final adjustments to the IF Linearity Corrector such that Differential gain is within 2 to 4 percent or as close as possible.
a. Observe differential gain and perform the following IF Linearity Corrector adjustments (see Figure 5-1).
b. Adjust TH-1 and SL-1 for optimum differential gain in the white to gray region.
c. Adjust TH-2 and SL-2 for optimum differential gain in the gray to black region.
d. Adjust TH-3 and SL-3 for optimum differential gain in the black region.
e. Adjust TH-4 and SL-4 for optimum sync to video ratio at $100 \%$ power. Make minor adjustments to visual power as necessary.

## NOTE

Plugs P2 and P3 on the Linearity Board are normally set for gain expansion (Pins 1-3). Compression can be accomplished in sections two and four by connecting plugs P3 and P2 to ground (pins 1-2). This may be needed to correct for $U$ shaped gain curves.
5.3.11. Differential Gain Correction at Video

Refer to 5.3.2.

## r 5.3.12. Differential Phase Correction

) Using envelope detection on the demodulator observe the transmitter's differential phase distortion and adjust as follows (see Figure 5-8).
a. Set Phase corrector NORMAL/BYPASS (in/out) switch to NORMAL(in) position.
b. Set all slope controls mid range.
c. Set all threshold controls fully CCW.
d. Starting with threshold 1 advance the threshold control to set the first break-in point in the phase corrector, then adjust the slope to increase or decrease the desired amount of correction. If the correction is in the wrong direction adjust threshold 1 and 2 fully CCW and skip to threshold 3.
e. Adjust the slope control CW to increase correction. Adjust the slope control CCW to decrease correction.
f. Use remaining threshold and slope pairs as required to optimize the transmitter differential phase.


Figure 5-7. ICPM Display

### 5.3.12.1. Clamp Pulse



With a DC coupled scope on TP8, adjust R84 to put the clamp pulse peak at 0 V .

### 5.3.12.2. Frequency response

Using a multiburst signal or video sideband adapter as a video source, adjust C 1 for a flat response as monitored on J 2 on the differential phase corrector card.
Adjust C48 for minimum interaction between differential gain and differential phase while switching the NORMAL/BYPASS switch in and out.
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### 5.3.13. Visual IF Delay Compensator Adjustments

The delay compensator board is used only to correct for delay introduced by tuned amplifiers following the exciter. Group delay adjustments should normally be performed after all other tuning and linearity adjustments have been completed. If the exciter is used by itself, both delay compensator sections should be bypassed. Shoill bees minor back to Coingelat
goold

### 5.3.13.1. Delay Compensator Preliminary Set Up

The delay compensator is divided into two identical sections each having a wide band path and a narrow band path. The frequency of the narrow band sections may be preset to approximate the anticipated correction. This will make final adjustment through the transmitter less difficult.
buared below
P. Connect the exciters VIS RF OUT to the spectrum analyzer using attenuators.
c. Set both delay compensator bypass switches to out.
d. Switch off the VSB Filter.
e. Set $Q$ of both delay compensators to 14. - sets hax $Q$ fox
f. Set BALANCE of both fully CCW. Sedor
g. Switch on the front delay compensator.
h. Set the frequency of the null. 75 MHz above carrier using FREQ control. See Figure 5-9.
i. Set front Q control to 8 .
j. Alternately use BALANCE and PHASE controls to restore flat response.
k. Switch in the rear delay comp section.

1. Set the frequency of the null 3 MHz above carrier using FREQ control. See Figure 5-10.
m . Set rear Q to 8 .
n. Alternately use BALANCE and PHASE of the rear section to restore flat response.
o. Switch VSB FILTER back in and reconnect exciter to transmitter.

### 5.3.13.2. Delay Compensator Adjustment Through Transmitter

Generally, the BALANCE and PHASE controls of each section can be used to correct minor frequency response deficiencies without interacting with the group delay adjustments. Refer to Figures 5-11 \& 5-12. Correspondingly, moderate
a. Apply video sweep with sync to exciter video input.


Figure 5-8. Diff. Phase, Effects of TH and SL Controls
adjustments of the group delay $Q$ and FREQ controls will not affect the frequency response adjustment.
a. Set up test equipment per Figure 5-13.
b. Apply video sweep and sync to the exciter input and observe the transmitter output on a sideband analyzer.
c. Sample the transmitter before the notch diplexer (if used) and set Notch Diplexer Equalizer to BYPASS.

## NOTE

Since the equalized VSB filter provides receiver equalization, the demodulator sound trap should be on during the following adjustments for CCIR-M units.
d. Set DELAY COMP switches to OUT position.
e. Set VSB IN/OUT switch to OUT position.


Figure 5-9
Preliminary Adjustment of the Left Section of the Delay Equal-


Figure 5-11. Effect of "BAL" Control on Amplitude Response
f. Ensure that transmitter frequency response is correct with both VSB and delay compensator bypassed.
g. If group delay adjustments not have been previously performed, or the condition of alignment is unknown, perform preset adjustments.
h. Switch the VSB and DELAY COMPS back in.
i. Using the Balance and Phase controls, adjust for the best flat frequency response through the transmitter. The front corrector should control the low end of the band and the rear the high end. The Q and FREQUENCY controls primarily effect the group delay which is observed to be correct when minimum ringing occurs on 2 T pulse and so done with mu/ti-pulor $t$ nece.


Figure 5-10
Preliminary Adjustment of the Right Section of the Delay


Figure 5-12. Effect of 'PHASE" Control on Amplitude Response


Figure 5-13. Test Equipment for Group Delay and
Notch Diplexer Equalizer Adjustments


2OT PULSE EXHIBITING
AMPLITUDE DEFICIENCY
AT SUBCARRIER. ADJUST
PHASE AND BALANCE FOR
FLAT SWEEP RESPONSE
Figure 5-14. Typical Waveforms, Envelope Delay Adjustments
minimum baseline distortion is seen on the 12.5 or 20 T modulated pulse. See Figure 5-14.

## CAUTION

DO NOT TURN THE FREQUENCY CONTROLS MORE THAN ONE OR TWO TURNS FROM THE PRESET OR THEY MAY BE MOVED OUT OF THE PASSBAND AND THE EFFECT WILL NOT BE VISIBLE MAKING IT IMPOSSIBLE TO RECOVER THE DESIRED ALIGNMENT WITHOUT STARTING OVER.
j. Apply composite video test signal to the exciter. Observing 2 T adjust the front section FREQ for symmetrical overshoots, and the front $Q$ for minimum ringing and overshoot.
k. Observing 12.5 or 20 T adjust rear FREQ for a symmetrical baseline, and the rear $Q$ for best compromise of minimum ringing of window leading edge, 2 T symmetry \& close in ring, and baseline symmetry of the 12.5 or 20 T pulse.

1. Repeat several cycles of amplitude response and pulse adjustments until both conditions are satisfactory.
m. Small changes in differential gain, ICPM, or differential phase may occur as a result of the delay adjustments a quick check of those parameters should be made when completing delay adjustments.
n. Sample transmitter after the notch diplexer and proceed to notch diplexer equalizer adjustments if used.

### 5.3.14. Notch Diplexer Equalizer Adjustments

This optional module is used to compensate the visual group delay error caused by the aural cavities of a notch diplexer.
Four stagger-tuned all pass networks delay the lower video frequencies by an amount corresponding to the delay of the upper video frequency sidebands in the diplexer.
See drawing 839-7900-169
Controls are:
Section 1 controls the lowest frequency range

- Bal R-40
- Phase C-20
- Freq C-46
- Q R-42

Section 2 controls

- Bal R-10
- Phase C-3
- Freq C-4
- Q R-30

Section 3

- Bal R-80
- Phase C-32
- Freq C-36
- QR-85

Section 4 controls the highest frequency range

- Bal R-52
- Phase C-22
- Freq C-24
- Q R-92

Gain and bias controls:

- In Circuit Gain R-3
- Bias R-43
- Master Gain R-65


### 5.3.15. Group delay adjustments

a. The all pass networks have been preset to the approximate diplexer correction at the factory. Usually only slight adjustment to section 4 is needed in the field to optimize system performance.
b. Observing 12.5T pulses adjust $Q$ control R-92 to remove baseline disturbance. See Figure 5-14.
c. Observing sweep adjust balance and phase controls for flattest response. The effect of these controls is shown in Figures 5-11 and 5-12.
d. The phase of the last section can be used to peak up 4.18 MHz at video approximately 1 dB to compensate the high frequency roll off of the notch diplexer.

### 5.3.16. Power Limit Adjustments

1. Visual Power Limit

The Visual Power Limit control limits the maximum power available from the visual amplifier of the exciter. The Power Limit control is set such that the maximum power out of the transmitter is 110 percent.
a. Using the VIS LIMIT control, reduce transmitter power output to 50 percent or less.
b. Raise Visual transmitter power until it reaches a maximum or $100 \%$ using the Visual Raise button on the front of the Exciter.
c. Repeat steps $a$ and $b$ until the Raise control will no longer increase the transmitter power output.
d. Adjust the VIS LIMIT control until the transmitter power output is $110 \%$.
e. Lower Visual transmitter power output with the VISUAL lower control on the front of the Exciter to $100 \%$ (or your normal operating power).

1. Aural Power Limit
f. The Aural Power Limit control limits the maximum power available from the aural amplifier of the exciter.
g. Using the AUR LIMIT control, reduce transmitter power output to 50 percent or less.
h. Raise Aural transmitter power until it reaches a maximum or $100 \%$ using the AURAL Raise button on the front of the Exciter.
i. Repeat steps $a$ and $b$ until the Raise control will no longer increase the Aural transmitter power output.
j. Adjust the AUR LIMIT control until the transmitter power output is $110 \%$.
k. Lower Transmitter power output with the Aural lower control on the front of the Exciter to $100 \%$ (or your normal operating power).

### 5.3.17. Final Amp

### 5.3.17.1. VisuaVAural Selection

There are no adjustments in the final amp, only selection of aural or visual service if it is necessary to replace the unit. Remove its cover and place J1 in the appropriate position.

### 5.4. Exciter Synthesizer Adjustments

### 5.4.1. VHF Synthesizer Card 1

### 5.4.1.1. 10 MHz Frequency Standard Adjustment

a. Remove power to the exciter.
b. Remove the cover to the synthesizer slot and place card 1 on the extender card. Disconnect the PFC input, J5, from card 1. (If you do not have the PFC option, there won't be a cable connected to J5).
c. Connect a frequency counter to the 10 MHz connector J3.
d. Apply power to the exciter and allow 15 minutes warm up minimum.
e. Measure the frequency on the counter. It should be 10.000000 MHz exactly. If not adjustment of R1 may be required.
f. Reconnect the PFC input, J5, to card 1 and replace synthesizer card into the RFI enclosure and refit the cover.
5.4.1.2. Internal PFC Adjustment
a. Remove power to the exciter.
b. Verify that the PFC option has been installed in the exciter.
c. Remove the cover to the synthesizer slot and place card 1 on the extender card.
d. Connect a frequency counter to the 10 MHz connector J3.
e. Apply power to the exciter and allow 15 minutes warm up minimum.
f. The PFC ON indicator DS1 should be illuminated. If not check that there is a minimum of 1 Vpp at the PFC input, J5.
g. Measure the frequency on the counter. It should be 10 MHz exactly. If not adjustment of the internal PFC vernier may be required.
h. Replace synthesizer card 1 into the RFI enclosure and refit the cover.

### 5.4.1.3. External PFC Adjustment

a. Remove power to the exciter.
b. Verify that the PFC option has been installed in the exciter and that the external 5 or 10 MHz standard has been applied to the exciter at J10.
c. Remove the cover to the synthesizer slot and place card 1 on the extender card.
d. Connect a frequency counter to the 10 MHz connector J3.
e. Apply power to the exciter and allow 15 minutes warm up minimum.
f. The PFC ON indicator DS1 should be illuminated. If not check that there is a minimum of 1 Vpp at the PFC input, J5.
g. Measure the frequency on the counter. It should be 10 MHz exactly. If not adjustment of the external PFC frequency may be required.
h. Replace synthesizer card 1 into the RFI enclosure and refit the cover.
5.4.1.4. Testing An Untuned Card 1 Synthesizer

In the event that an untuned synthesizer card must be replaced in the field the following test equipment is required for satisfactory alignment:
a. Oscilloscope Tektronic 475 or equivalent.
b. Frequency counter HP5315A or equivalent.
c. Spectrum analyzer HP3585 or equivalent.
d. Modulation monitor HP8901 or equivalent.

### 5.4.1.4.1. Visual inspection

Visually inspect the PWB for shorts and opens. Visually inspect the PWB for the correct installation of all integrated circuits and semiconductors.

### 5.4.1.4.2. Programming

a. Refer to the channel assignment and determine what frequency the synthesizer is to be set for.
b. Refer to the programming chart, Table 5-3, and remove the jumpers for the correct IF frequency of operation.

NOTE: $\mathrm{IN}=$ LOW $=0$

$$
\mathrm{OUT}=\mathrm{HIGH}=1
$$

5.4.1.4.3. Test Connections
a. Remove power from the exciter.
b. Remove the cover from the synthesizer slot and place card 1 on the extender card.
c. Turn on the exciter power supply.

### 5.4.1.4.4. Reference frequency chain setup

a. Disconnect the PFC input to card 1 at J5. If applicable.
b. Connect the frequency counter to the boards 10 MHz connector J3. Allow 15 minute warm up.
c. Adjust R1 (frequency Adjust) for 10.000000 MHz as read on frequency counter.
d. Connect the frequency counter to the boards 5 MHz connector. The frequency should be 5.000000 MHz .
e. Connect the oscilloscope to TP4. Adjust L4 for maximum peak to peak signal.
f. Connect the frequency counter to the boards 16 MHz connector, J4. The frequency should be 16.000000 MHz .
g. Connect the frequency counter to the boards 800 kHz connector. The frequency should be 800.000 kHz .

### 5.4.1.4.5.PFC Setup

a. Temporarily connect the spectrum analyzers rear panel 10 MHz output to card l's 10 MHz PFC input J 5 .
b. Connect the oscilloscope to TP1. Adjust L1 for maximum dc voltage on scope (Approximately 6VDC).
c. DS1 (PFC ON IND.) should be on.
d. Reconnect the exciter PFC input to card 1, J5 (if applicable).

### 5.4.1.4.6. 30 MHz Peaking Adjustment

a. Connect the spectrum analyzer through a scope probe to TP 6. Set the analyzer for a span of $0-40 \mathrm{MHz}$.

Table 5-3

| SYNTHESIZER CARD 1 |  |  |
| :---: | :---: | :---: |
| PROGRAMING CHART |  |  |
| IF |  |  |
| FREQUENCY | JUMPER <br> SELECTION |  |
| MHz | 7654321 | PLL BW |
| 37.0 | 1000110 | 001 |
| 37.1 | 1000111 | 001 |
| 37.2 | 1001000 | 001 |
| 37.3 | 1001001 | 001 |
| 37.4 | 1001010 | 001 |
| 37.5 | 1001011 | 001 |
| 37.6 | 1001100 | 001 |
| 37.7 | 1001101 | 001 |
| 37.8 | 1001110 | 001 |
| 37.9 | 1001111 | 001 |
| 38.0 | 1010000 | 001 |
| 38.1 | 1010001 | 001 |
| 38.2 | 1010010 | 001 |
| 38.3 | 1010011 | 001 |
| 38.4 | 1010100 | 001 |
| 38.5 | 1010101 | 001 |
| 38.6 | 1010110 | 001 |
| 38.7 | 1010111 | 001 |
| 38.8 | 1011000 | 001 |
| 38.9 | 1011001 | 001 |
| 39.0 | 1011010 | 001 |
| 40.0 | 1011011 | 001 |

b. Adjust L 7 for maximum 30 MHz signal as seen on the analyzer.

### 5.4.1.4.7. PLL Lock Adjustment

a. Connect the modulation monitor RF input to the boards 37 MHz connector J6. Select frequency on the modulation monitor.
b. Connect the oscilloscope to U11 pin 7.
c. Adjust C38 for +7 Vdc on U11 pin 7. The loop should be locked. Lock is indicated by a stable dc voltage on the scope. The modulation monitor should read the desired IF frequency.

### 5.4.1.4.8. Output Filter Adjustment

a. Connect the boards IF output J6 to the spectrum analyzers 50 ohm input. Set the analyzer for:

| CENTER: | 20 MHz |
| :--- | :---: |
| SPAN: | 40 MHz |
| RBW: | 1 kHz |
| REF: | +10 dBm |
| RANGE: | +10 dBm |
| INPUT: | 50 OHMS |

b. Alternately adjust L17, L18, L19 for maximum IF frequency level. The level should be +7 dBm minimum. Spurs should be less than -80 dBc .

### 5.4.1.4.9.FM Noise Measurement

a. Connect the IF output J6 to the modulation monitor RF input.
b. Measure the FM noise relative to 75 kHz deviation with 75 usec de-emphasis. The noise measured should be less than -80 dB .

### 5.4.2. VHF Synthesizer Card 2

There are no user adjustments required on card 2.

### 5.4.2.1. Testing A Synthesizer Card 2

In the event that a synthesizer card must be replaced in the field the following test equipment is required for satisfactory alignment:
a. Oscilloscope Tektronic 475 or equivalent.
b. Frequency counter HP 5315A or equivalent.
c. Spectrum analyzer HP3585 or equivalent.
d. Modulation monitor HP8901 or equivalent.

### 5.4.2.2. Visual Inspection

a. Visually inspect the PWB for shorts and opens.
b. Visually inspect the PWB for the correct installation of all integrated circuits and semiconductors.

### 5.4.2.3. Programming

a. Refer to the channel assignment and determine what frequency the synthesizer is to be set for.
b. Refer to the programming chart (Table 5-4, 5-5 and 5-6)and remove the jumpers for the correct RACHET (Frach) and LO (Flo) frequency of operation.

NOTE: All columns except NO-6

$$
\text { Jumper in }=\text { low }=0
$$

Jumper out $=$ high $=1$
Column NO-6
Jumper in $=$ high $=1$
Jumper out $=$ low $=0$

### 5.4.2.4. Test Connections

a. Remove the cover from the synthesizer slot and place card 2 on the extender card.
b. Connect the 5 MHz and 800 kHz from card 1 card 2 Jl and J2.
c. Turn on the power supply.

### 5.4.2.5. Ratchet PLL Setup

a. Set R13 for mid range.
b. Connect the frequency counter through a scope probe to the junction of L4 and C39. The frequency measured should agree with the programming chart. This is the ratchet loop frequency (Frach on programming chart).
c. Connect the spectrum analyzer's tracking generator output through a 100 k resistor to U 2 pin 3 . Connect the
spectrum analyzers RF input through a scope probe to the junction of R15 and R13.
d. Set the analyzer for:

| START: | 0 Hz |
| :--- | :--- |
| STOP: | 500 kHz |
| RBW: | 1 kHz |
| REF: | -25 dBm |
| RANGE: | -25 dBm |
| INPUT: | 1 M ohm |

e. Adjust L 3 for a notch centered at 100 kHz .
f. Adjust L2 for a notch centered at 200 kHz .
g. Remove the tracking generator and 100 k resistor.

### 5.4.2.6. Main PLL Setup

a. Set R44 to mid range. (This is a 5 turn pot).
b. Connect the frequency counter to the LO output connector J3. The frequency measured should be the desired LO frequency (Flo on programming chart).
c. Connect the spectrum analyzer's tracking generator output through a 100 k resistor to U25 pin 3. Connect the spectrum analyzers RF input through a scope probe to the junction of R43 and R44.
d. Set the analyzer for:

| START: | 0 Hz |
| :--- | :--- |
| STOP: | 500 kHz |
| RBW: | 1 kHz |
| REF: | -25 dBm |
| RANGE: | -25 dBm |
| INPUT: | 1 M ohm |

e. Adjust L 5 for a notch centered at 100 kHz .
f. Adjust L7 for a notch centered at 200 kHz .
g. Remove the tracking generator and 100 k resistor.

### 5.4.2.7. FM Noise Measurement

a. Connect the LO output J3 to the modulation monitor RF input.
b. Measure the FM noise relative to 75 kHz deviation using 75usec de-emphasis. The noise should be less than 80 dB .

### 5.4.2.8. ICPM Measurement

At the exciter output, J2
a. Adjust R13 for best ICPM and microphonics.
b. Adjust R14 for best ICPM and Microphonics.
c. ICPM should measure less than $+/-.5$ degree peak to peak.

### 5.4.2.9. Final Installation

a. Remove card 2 from the extender and place it into the RFI enclosure.
b. Refit the RFI enclosure cover to the synthesizer slot.
c. Refit the exciter lid.

Table 5-4

| SYNTHESIZER CARD 2 |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| PROGRAMMING CHART USA CHANNEL PROGRAMMING |  |  |  |  |  |  |  |  |  |
| CHAN | $\mathrm{F}_{\text {LO }}$ | $\mathrm{N}_{\mathrm{U} 35}$ | FVCO | $\mathrm{F}_{\text {RACH }}$ | 1N0-7 | 1A0-5 | $F_{\text {SSB }}$ | $\mathrm{N}_{\mathrm{U} 27}$ | N0-6 |
|  |  |  |  |  | 76543210 | 543210 |  |  | 6543210 |
| 2 - | 92.24 | 2 | 184.48 | 14.48 | 10010000 | 001000 | 170 | 34 | 1011110 |
| 2F | 92.25 | 2 | 184.50 | 14.50 | 10010001 | 000000 | 170 | 34 | 1011110 |
| 2+ | 92.26 | 2 | 184.52 | 14.52 | 10010001 | 000010 | 170 | 34 | 1011110 |
| 3- | 98.24 | 2 | 196.48 | 11.48 | 01110010 | 001000 | 185 | 37 | 1011011 |
| 3F | 98.25 | 2 | 196.50 | 11.50 | 01110011 | 000000 | 185 | 37 | 1011011 |
| 3+ | 98.26 | 2 | 196.52 | 11.52 | 01110011 | 000010 | 185 | 37 | 1011011 |
| 4. | 104.24 | 2 | 208.48 | 13.48 | 10000110 | 001000 | 195 | 39 | 1011001 |
| 4 F | 104.25 | 2 | 208.50 | 13.50 | 10000111 | 000000 | 195 | 39 | 1011001 |
| 4+ | 104.26 | 2 | 208.52 | 13.52 | 10000111 | 000010 | 195 | 39 | 1011001 |
| 5- | 114.24 | 2 | 228.48 | 13.48 | 10000110 | 001000 | 215 | 43 | 1010101 |
| 5 F | 114.25 | 2 | 228.50 | 13.50 | 10000111 | 000000 | 215 | 43 | 1010101 |
| 5+ | 114.26 | 2 | 228.52 | 13.52 | 10000111 | 000010 | 215 | 43 | 1010101 |
| 6- | 120.24 | 2 | 240.48 | 10.48 | 01101000 | 001000 | 230 | 46 | 1010010 |
| 6 F | 120.25 | 2 | 240.50 | 10.50 | 01101001 | 000000 | 230 | 46 | 1010010 |
| $6+$ | 120.26 | 2 | 240.52 | 10.52 | 01101001 | 000010 | 230 | 46 | 1010010 |
| $7-$ | 212.24 | 1 | 212.24 | 12.24 | 01111010 | 000100 | 200 | 40 | 1011000 |
| 7F | 212.25 | 1 | 212.25 | 12.25 | 01111010 | 000101 | 200 | 40 | 1011000 |
| 7+ | 212.26 | 1 | 212.26 | 12.26 | 01111010 | 000110 | 200 | 40 | 1011000 |
| 8 - | 218.24 | 1 | 218.24 | 13.24 | 10000100 | 000100 | 205 | 41 | 1010111 |
| 8 F | 218.25 | 1 | 218.25 | 13.25 | 10000100 | 000101 | 205 | 41 | 1010111 |
| $8+$ | 218.26 | 1 | 218.26 | 13.26 | 10000100 | 000110 | 205 | 41 | 1010111 |
| 9- | 224.24 | 1 | 224.24 | 14.24 | 10001110 | 000100 | 210 | 42 | 1010110 |
| 9F | 224.25 | 1 | 224.25 | 14.25 | 10001110 | 000101 | 210 | 42 | 1010110 |
| $9+$ | 224.26 | 1 | 224.26 | 14.26 | 10001110 | 000110 | 210 | 42 | 1010110 |
| 10- | 230.24 | 1 | 230.24 | 10.24 | 01100110 | 000100 | 220 | 44 | 1010100 |
| 10F | 230.25 | 1 | 230.25 | 10.25 | 01100110 | 000101 | 220 | 44 | 1010100 |
| 10+ | 230.26 | 1 | 230.26 | 10.26 | 01100110 | 000110 | 220 | 44 | 1010100 |
| 11- | 236.24 | 1 | 236.24 | 11.24 | 01110000 | 000100 | 225 | 45 | 1010011 |
| 11F | 236.25 | 1 | 236.25 | 11.25 | 01110000 | 000101 | 225 | 45 | 1010011 |
| 11+ | 236.26 | 1 | 236.26 | 11.26 | 01110000 | 000110 | 225 | 45 | 1010011 |
| 12- | 242.24 | 1 | 242.24 | 12.24 | 01111010 | 000100 | 230 | 46 | 1010010 |
| 12F | 242.25 | 1 | 242.25 | 12.25 | 01111010 | 000101 | 230 | 46 | 1010010 |
| 12+ | 242.26 | 1 | 242.26 | 12.26 | 01111010 | 000110 | 230 | 46 | 1010010 |
| $13-$ | 248.24 | 1 | 248.24 | 13.24 | 10000100 | 000100 | 235 | 47 | 1010001 |
| 13F | 248.25 | 1 | 248.25 | 13.25 | 10000100 | 000101 | 235 | 47 | 1010001 |
| 13+ | 248.26 | 1 | 248.26 | 13.26 | 10000100 | 000110 | 235 | 47 | 1010001 |

Table 5-5

| $\begin{gathered} \text { SYNTHESIZER CARD } 2 \\ \text { PROGRAMMING CHART } \\ \text { AUSTRALIAN CHANNEL PROGRAMMING } \end{gathered}$ |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CHAN | FLO | $\mathrm{N}_{\mathrm{U} 35}$ | FVCO | $\mathrm{F}_{\mathrm{RACH}}$ | 1N0-7 | 1A0-5 | $\mathrm{F}_{\text {SSB }}$ | $\mathrm{N}_{\mathrm{U} 27}$ | N0-6 |
|  |  |  |  |  | 76543210 | 543210 |  |  | 6543210 |
| 0 | 85.15 | 2 | 170.30 | 10.30 | 01100111 | 000000 | 160 | 32 | 0100000 |
| 1 | 96.15 | 2 | 192.30 | 12.30 | 01111011 | 000000 | 180 | 36 | 1011100 |
| 2 | 103.15 | 2 | 206.30 | 11.30 | 01110001 | 000000 | 195 | 39 | 1011001 |
| 3 | 125.15 | 2 | 250.30 | 10.30 | 01100111 | 000000 | 240 | 48 | 1010000 |
| 4 | 134.15 | 2 | 268.30 | 13.30 | 10000101 | 000000 | 255 | 51 | 1001101 |
| 5 | 141.15 | 2 | 282.30 | 12.30 | 01111011 | 000000 | 270 | 54 | 1001010 |
| 5A | 177.15 | 1 | 177.15 | 12.15 | 01111001 | 000101 | 165 | 33 | 1011111 |
| 6 | 214.14 | 1 | 214.15 | 14.15 | 10001101 | 000101 | 200 | 40 | 1011000 |
| 7 | 221.15 | 1 | 212.15 | 12.15 | 01111001 | 000101 | 200 | 40 | 1011000 |
| 8 | 228.15 | 1 | 228.15 | 13.15 | 10000011 | 000101 | 210 | 42 | 1010110 |
| 9 | 235.15 | 1 | 235.15 | 10.15 | 01100101 | 000101 | 225 | 45 | 1010011 |
| 10 | 248.15 | 1 | 248.15 | 13.15 | 10000011 | 000101 | 235 | 47 | 1010001 |
| 11 | 255.15 | 1 | 255.15 | 10.15 | 01100101 | 000101 | 245 | 49 | 1001111 |

Table 5-6

| SYNTHESIZER CARD 2 PROGRAMMING CHART <br> EUROPEAN CHANNEL PROGRAMMING |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CHAN | $\mathrm{F}_{\text {LO }}$ | $\mathrm{N}_{\mathrm{U} 35}$ | Fvco | $\mathrm{F}_{\text {RACH }}$ | 1N0-7 | 1A0-5 | FSSB | $\mathrm{N}_{\mathrm{U} 27}$ | N0-6 |
|  |  |  |  |  | 76543210 | 543210 |  |  | 6543210 |
| E2 | 87.15 | 2 | 174.30 | 14.30 | 10001111 | 000000 | 160 | 32 | 1100000 |
| E2A | 88.65 | 2 | 176.30 | 11.30 | 01110001 | 000000 | 165 | 33 | 1011111 |
| E3 | 94.15 | 2 | 188.30 | 13.30 | 10000101 | 000000 | 175 | 35 | 1011101 |
| E4 | 101.15 | 2 | 202.30 | 12.30 | 01111011 | 000000 | 190 | 38 | 1011010 |
| E5 | 214.15 | 1 | 214.15 | 14.15 | 10001101 | 000101 | 200 | 40 | 1011000 |
| E6 | 221.15 | 1 | 221.15 | 11.15 | 01101111 | 000101 | 210 | 42 | 1010110 |
| E7 | 228.15 | 1 | 228.15 | 13.15 | 10000011 | 000101 | 215 | 43 | 1010101 |
| E8 | 235.15 | 1 | 235.15 | 10.15 | 01100101 | 000101 | 225 | 45 | 1010011 |
| E9 | 242.15 | 1 | 242.15 | 12.15 | 01111001 | 000101 | 230 | 46 | 1010010 |
| E10 | 249.15 | 1 | 249.15 | 14.15 | 10001101 | 000101 | 235 | 47 | 1010001 |
| E11 | 256.15 | 1 | 256.15 | 11.15 | 01101111 | 000101 | 245 | 49 | 1001111 |
| E12 | 263.15 | 1 | 263.15 | 13.15 | 10000011 | 000101 | 250 | 50 | 1001110 |

### 5.5. Aural Adjustments

### 5.5.1. Aural PLL/VCO

The PLLVCO on the Aural Converter board is factory set and adjustment should be made only if necessary.
a. Set jumpers for desired frequency (see Table 5-7).
b. Connect a dc coupled scope to TP1 (Directly below DS1).
c. Adjust L 1 for 8 Vdc at TPl .
d. The loop should be locked and DS1 should be off.

### 5.5.2. Frequency Adjustment

The operating frequencies are all determined by the reference oscillator on the Synthesizer Card 1. (Refer to 10 MHZ Frequency Standard adjustment or PFC frequency adjustments on the VHF synthesizer Card 1 discussed earlier in this section).

### 5.5.3. Aural Deviation Adjustment Sequence

The following adjustments match the incoming signals to the exciter to provide proper on air deviation at transmitter output.

## a. Mono Deviation

1. Apply +10 dBm balanced mono signal to J 8 , the mono input of the exciter
2. Remove any signals from SC 1 and SC 2 (J6 and J7 on the back of the exciter)
3. Set J 5 on the Aural converter board to local (Pins 2-3, the two pins closest to the top of the board).
4. Set S2 to mono/SC
5. Adjust R49 for desired deviation as observed using aural mod monitor
b. SC 1 Deviation
6. Apply 1V RMS unbalanced SC signal to SC 1 input
7. Remove any signal from mono input
8. Set J5 to local
9. Set S2 to Mono/SC
10. Adjust R58 for desired deviation of SC 1
c. SC 2 Deviation
11. Apply $1 V$ RMS unbalanced SC signal to SC 2 input
12. Remove any signal from mono input
13. Set J5 to local
14. Set S2 to Mono/SC
15. Adjust R67 for desired deviation of SC 2
d. Comp Deviation
16. Apply 1V RMS unbalanced composite signal to the composite input, J5
17. Set J 5 to local
18. Set S2 to Composite
19. Adjust R61 for desired deviation

### 5.6. Aural Group Delay Corrector Adjustments (option)

The intent of adjusting the aural group delay corrector is to make the overall aural IF to RF output path as transparent as possible to the aural stereo signal when operating through a notch diplexer.
It is good practice to begin the aural equalization process by noting the amount of stereo separation error, L into R or R into L , when the aural transmitter system is operated with and without the notch diplexer. This can be done by noting the separation values before and after the diplexer with an RF probe at these points connected to the aural demodulation test equipment.
For example, if -38 dB of separation is measured at the input to the diplexer and -32 dB after the diplexer (aural corrector out), then 6 dB is the maximum amount of correction possible to make the system transparent. The effect of adjusting the corrector is to make the output separation equal to -38 dB when the corrector is switched in. A 6 dB improvement, of course, requires perfect equalization of the system which is not practical, but a close approximation can be readily achieved. In practice, acceptable levels of equalization occur when the corrector is adjusted for about 2 to 4 dB stereo separation improvement instead of the ideal 6 dB as in the above example. If overall separation values better than -38 dB (the input signal separation) are desired, then the baseband input system (stereo generator, etc.) must be adjusted.

## NOTE

The aural group delay corrector has the characteristic that over compensation is possible by introducing additional L-R sideband phase shift. In some stereo systems this may appear to be beneficial by improving stereo separation at the output better than the input, however, there is a performance trade-off point where synchronous AM noise and SUB to SAP crosstalk begin to increase. This occurs when the output stereo separation begins to exceed the input separation value while adjusting the group delay corrector. It is recommended that only enough group delay correction be introduced into the system to correct for the notch diplexer.
The aural delay corrector can be adjusted without the need for group delay measuring equipment by simply adjusting it for best stereo separation. This is true for delay curves that are reasonably symmetrical.
Typically, a single cavity notch diplexer, properly tuned, will exhibit a symmetrical response curve for which the aural group delay corrector is intended to equalize. A properly tuned, single cavity notch diplexer implies that both cavities (a single cavity on each hybrid arm) are simultaneously tuned to the aural carrier frequency for minimum reject load power, a good indicator of symmetrical tuning. This is mentioned here because if the diplexer is not properly tuned, and a condition of

Table 5-7. PLL Switch Settings

| IF | PROGRAM DATA FOR U8 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | A5 | A4 | A3 | A2 | A1 | A0 | RA2 | RAI | RA0 | N9 | N8 | N7 | N6 | N5 | N4 | N3 | N2 | N1 | N0 |  |
| 32.5 MHz | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | $0=$ Jumper IN |
| 33.4 MHz | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1=Jumper OUT |

stagger tuning exists, then group delay equalization will be difficult. Correct delay equalization is still possible in this case, however, accurate group delay measuring equipment will be required.
The procedure described below is intended to be a simple routine adjustment that does not require expensive group delay measuring equipment.

### 5.6.1. Initial Procedure

## NOTE

The aural group delay corrector has been factory set to equalize a typical single cavity notch diplexer. It may be close enough for satisfactory operation, try it first before making adjustments.
a. Set the stereo input signal for BTSC equivalent mode operation (companding off) and briefly check the system for good overall wideband performance, i.e., satisfactory frequency response, low noise and distortion levels that might otherwise interfere with stereo separation measurements. Make this check before the diplexer and with the corrector switched out.
b. Set the demodulated test output equipment for stereo separation tests, either $L$ into $R$ or $R$ into $L$ under maximum modulation levels ( 37.5 kHz for L or R only and an additional 5 kHz for the pilot).

## NOTE

37.5 kHz deviation occurs due to 12.5 kHz modulation existing in the $L+R$ channel and 25 kHz in the $L-R$ channel for an $L$ or $R$ only input signal when the pilot PRO and SAP are switched off (BTSC linear mode).
c. Note the amount of stereo separation existing in the system at two modulating frequencies $(400 \mathrm{~Hz}$ and 4 kHz ) before and after the diplexer with the delay corrector switched out. Be sure the diplexer cavities are at normal operating temperature.
d. Switch the aural delay corrector in and determine if it is providing a satisfactory level of equalization at both modulating frequencies ( 400 Hz and 4 kHz ). The corrector should equalize about $1 / 2$ to $3 / 4$ of the error introduced by the diplexer. Also, the separation values should be reasonably well balanced within 2 to 3 dB between 400 Hz and 4 kHz . If this level of performance is not achieved then adjustment is required.

### 5.6.2. Adjustments

a. Set the modulating tone to 400 Hz and temporarily switch off the pilot, Pro and SAP carriers. Adjust the main channel for 37.5 kHz deviation with a L or R only input signal ( BTSC equivalent mode) and switch the pilot back on. Be sure the RF sample is after the diplexer.
b. Adjust F1 or F2 trimmer capacitors (see Figure 5-15) one at a time very slowly for best separation. It is good practice to note the starting position of each trimmer by noting the position of the adjustment slot. Typically, only a $1 / 4$ turn on either side of the starting position is all that is necessary to notice a change in separation. Alternately adjust F1 and F2 for best separation.
c. Set the modulating tone for 4 kHz and repeat the above, if necessary, to obtain about the same value of separation


Figure 5-15. Top View of Aural Delay Corrector
as at 400 Hz . Only a very slight adjustment is needed to bring about a reasonable compromise between the two frequencies, typically within 2 to 3 dB .

## NOTE

The RF sample after the diplexer will now show improved stereo separation while the input side of the diplexer will show decreased separation which is really the test equipment interpreting the precorrection as distortion. The same characteristic is also true of AM synchronous noise and crosstalk.

### 5.6.3. Retuning Procedure

a. Should it be noticed that during tuning adjustment of Fl or F2 little or no reaction is observed and it is felt that the corrector has been tuned too far, then realignment of the corrector is necessary to get F1 and F2 resonators back on the aural IF carrier.
b. A simple RF sweep test of the aural delay corrector will suffice in re-establishing performance. The objective is to locate the amplitude dips in the sweep response and retune them back on the aural IF frequency ( 32.50 MHz ). Tuning of F1 and F2 is done by adjusting the trimmer capacitors. Refer to Figure 5-16 for typical test equipment setup. Attempt to get the sweep response curves shown in Figure 5-18 with the same amplitude levels as shown.

## NOTE

This is a frequency response test. Measuring the group delay curve is not necessary at this time for a simple alignment of the resonators. From previous measurements on this circuit, each 1 $d B$ of amplitude dip introduces approximately 100 ns of delay with the same general curve shape. The amplitude and frequency position of the response dip can then be used as a guide for proper operation of the delay corrector. Refer to Figure 5-18 for typical response curves showing this relationship.
c. If an RF sweeper with an accurate 32.50 MHz marker is not available, then an alternate method of sweep alignment is shown in Figure 5-17. This method uses a visual sideband analyzer setup in the normal manner except the exciter visual IF output is fed to the aural delay corrector for sweep response alignment. The 4.5 MHz marker will
provide the accuracy for positioning the resonators on the aural IF frequency.
d. The amplitude dip in the frequency response curve caused by F1 and F2 should be about equal in amplitude. If not, then adjust the link coupling as shown in Figure $5-20$ for equal amplitudes and with the typical levels shown in Figure 5-19.
e. When F1 and F2 amplitude dips are both positioned on the aural IF carrier, as shown in Figure 5-18, then the delay corrector is ready again for stereo separation adjustments as described above.

### 5.7. Meter Calibration

Meter calibrate controls are located along the top-front edge of the exciter on the Meter/Control board.
a. Visual Power Calibrate (RF Wattmeter Method)

1. Connect the visual RF output to a RF wattmeter and disconnect the I/O cable from the exciter.
2. Apply a black picture (no set up) to the video input Proper sync ratio must be maintained for meter cali-


Figure 5-16. Typical Sweep Setup Aural Delay Corrector


Figure 5-17. Alternate Sweep Method Aural Delay Corrector
bration by observing demodulated exciter output on a waveform monitor or scope.
3. Increase visual power such that a 0.6 W is read on a RF wattmeter. (Adjust VIS LIMIT if required, to obtain 1 watt out of the Exciter).
4. Now adjust the VIS PWR CAL CCW until all bars on the bar graph are lit. Then adjust CW until 3 of the bars go out. The Bar graph is now calibrated.
5. The CAL control sets the reference for the digital meter. It should be set so that both digital and analog bargraph meters agree. Adjust CAL such that \% POWER METER reads 1000 mW .
6. Lower the Exciter output to zero, and reconnect the RF output and the I/O cable to the Exciter.
7. Turn the transmitter on and raise the power to your normal operating power.
8. If the VIS LIMIT control was moved, it will be necessary to do POWER LIMIT ADJUSTMENTS later in this section.
b. Alternate Visual Power Calibrate (Spectrum Analyzer Method)

1. Apply video to the input of the Exciter.
2. Connect a spectrum analyzer to the output of the exciter with a 10 dB pad and disconnect the I/O cable from the back of the Exciter. The 10 dB pad will keep you from overloading the input to the analyzer, which is usually rated at 1 watt input.
3. Increase visual power until you have +20 dBm on the spectrum analyzer at the peak of sync. ( +20 dBm with a 10 dB pad is +30 dBm which is equal to 1 watt. Adjustment of the "VIS LIMIT" control may be required, to obtain 1 watt out of the Exciter).


Figure 5-18. Aural Delay Corrector Amplitude Response Curves. NOTE: Amplitude Response is Broadband with a Small Response Dip as Shown Above.
4. Now adjust the VIS PWR CAL CCW until all bars on the bar graph are lit. Then adjust CW until 3 of the bars go out. The Bar graph is now calibrated.
5. The CAL control sets the reference for the digital meter. It should be set so that both digital and analog bargraph meters agree. Adjust CAL such that \% POWER METER reads 1000 mW .
6. Lower the Exciter output to zero, and reconnect the RF output and the I/O cable to the Exciter.
7. Turn the transmitter on and raise the power to your normal operating power.
8. If the VIS LIMIT control was moved, it will be necessary to do POWER LIMIT ADJUSTMENTS later in this section.
c. Aural Power Calibrate

1. Connect AURAL RF OUT to a RF wattmeter.
2. Adjust AURAL RAISE/LOWER for 1 watt output.
3. Set AURAL calibrate pot R61 for full-scale 1 watt on the bar graph. The \% POWER METER should read 1000.
d. Refer to power limit adjustments if limit controls were adjusted during this procedure.

### 5.7.1. VSWR Foldback

A voltage applied to the VSWR inputs on the remote control connector will reduce power by a proportional amount. When used with the Harris transmitter these controls should be fully CW.

### 5.8. Power Supply Adjustment Procedure

Supply;Adjustment Procedure
The power supply has been set at the factory and adjustment should be made only if necessary.

A quick check of the 5 power supply voltages ( $+24,+15$,$15,+5$ and -5 volts) can be made by placing the Extender card into an empty slot and see if all 5 Green LED's come on. For a more accurate check, use a VOM to measure the supply voltages by looking at the rear lead of the 2W LED series dropping resistors on the Extender card. The voltages on each resistor should be from top to bottom, $+24,+15,-15,+5$ and -5 volts.
If the voltages need adjustment, it will be necessary to gain access to the power supply itself. The procedure is as follows;
a. Remove power to the exciter.
b. Remove rear top cover.
c. Remove the rear aluminum cross-member to which the top rear cover was fastened. There are 2 screws in each end of the cross-member and 8 screws along the back that will need to be loosened. The cross-member may now be removed.
d. Remove the 7 screws holding the top cover on the power supply. WARNING - Primary power is present inside the power supply cage if power is returned to the exciter. This area should be covered during troubleshooting to prevent accidental contact with the primary line potential.
e. Using a DC VOM or scope, clip a test lead on one of the test points inside the power supply cage, route the test lead outside the cage, and refasten the power supply cover. Refer to Table 5-8 for test points and adjustments.
f. Apply power to the exciter, and note the voltage.
g. If adjustment is necessary, remove power from the exciter, remove the power supply cover, and make a slight adjustment on the appropriate potentiometer. Now refasten the power supply cover, return power to the exciter, and recheck the voltage. If it is still incorrect, repeat the procedure.


Figure 5-19. Typical Amplitude \& Delay Aural Delay Corrector


Figure 5-20. Link Coupling Adjustment Aural Delay Corrector
h. If it is correct, remove power and reassemble the exciter.

### 5.9. Component Replacement On Circuit Boards

The circuit boards used in the VHF TV exciter are doublesided circuit boards with plated through-holes. Soldering on this circuit board is possible with conventional tools if care is observed.
For repair, a de-soldering station is suggested such as an Air-Vac PVSG-60E De-Soldering System made by Air-Vac Engineering Co., Inc., 100 Gulf St., Milford, CT 06460 (203-874-2541). This de-soldering system utilizes a venturi to develop the suction and therefore requires an air pressure source of approximately 35 PSI. It is relatively inexpensive for such a system and works well.
Techniques must be developed using the de-soldering station. Sometimes, it may be necessary to add solder to the connection to assist heat flow to the connection several times until the solder can be removed in steps. Possibly, removing solder from both sides of the circuit board will assist in clearing the throughholes.
The circuit board used in the VHF TV exciter utilizes plated through-holes. Because of these through-holes, solder fills the holes by capillary action. This condition requires that defective components be removed carefully to avoid damage to the circuit board.
On all circuit boards, the adhesive securing the copper track to the circuit board melts at almost the same temperature at which solder melts. A circuit-board track can be destroyed by excessive heat or lateral movement during soldering. Use of a
heat source no larger than necessary with steady pressure is required for circuit board repair.
To remove a component from a circuit board such as the type used in the VHF TV exciter, cut the leads from the body of the defective component while the device is still soldered to the circuit board.
Carefully grasp each component lead, one at a time with miniature long-nose pliers. Heat each lead independently. When the solder begins to melt, carefully pull the lead from each hole. The holes may then be cleared of solder with vacuum.
Install the new component and solder the component in place.

## WARNING

MOST SOLVENTS WHICH WILL REMOVE ROSIN FLUX ARE VOLATILE AND TOXIC BY THEIR NATURE AND SHOULD BE USED ONLY IN SMALL AMOUNTS IN A WELL-VENTILATED AREA, AWAY FROM FLAME (INCLUDING CIGARETTES) AND A HOT SOLDERING IRON. OBSERVE THE MANUFACTURER'S CAUTIONARY INSTRUCTIONS.

After soldering, remove flux with a cotton swab moistened with a suitable solvent. Rubbing alcohol is highly diluted with water and is not effective. Solvents are available at electronic supply houses which are useful.
The circuit board should be checked to ensure that the flux has been removed from the circuit board and not just smeared about. Rosin flux is not normally corrosive, but rosin can absorb enough moisture in time to become conductive and cause problems.

Table 5-8
Power Supply Adjustments

| Voltage | Test Point | Adjust |
| :---: | :---: | :---: |
| +24 | E1 | R-16 |
| +15 | E3 | R-17 |
| -15 | E5 | R-18 |
| +5 | E7 | R-19 |
| -5 | E9 | R-20 |
| GND | E10 |  |

## SECTION VI

## TROUBLESHOOTING

### 6.1. Introduction

Most troubleshooting consists of visual checks. All the various indicators (meters, led's, and fuse) should be used to isolate the problem to a specific area of the VHF TV exciter, the input, or the load.
Once the trouble is isolated, refer to Section IV for detailed explanations of the circuit theory and diagrams in section VIII to aid in problem resolution.

### 6.2. Troubleshooting Assistance

Assistance with troubleshooting is available from the Harris Customer Service Department either by letter to the following address or by telephone (217-222-8200) 24 hours a day.

Harris Corporation, Broadcast Division
P. O. Box 4290

Quincy, IL 62305
ATTEN: Customer Service Department
It is necessary to have the model number and serial number of the unit to retrieve certain information. Organize material before calling or writing, listing all observable symptoms and characteristics, sequence of events, meter readings, revision level of circuit boards.

### 6.3. Returns

To return material to Harris under warranty, a return authorization number must be obtained from the Harris Customer Service Department prior to returning any unit for any reason. A return authorization will assure speedy and accurate handling of your return. A written description including the following information must accompany all returns unit in addition to the return authorization number:
a. The customer name, address, and telephone number.
b. The return authorization number.
c. A description of the problem or why the unit was returned.
Ship or otherwise return the product, transportation and insurance prepaid to:

Harris Corporation, Broadcast Division
P. O. Box 4290

Quincy, IL 62305
Units not under warranty may be returned for repair without return authorization. Contact our Repair Dept. for information on our current rates, estimates, and scheduling. If a quick turn around is needed for emergencies consult the Repair Dept. Supervisor by phone at 217-222-8200.

# SECTION VII PARTS LIST 

## Introduction

This section provides descriptions and part numbers of electrical components, assemblies, and selected mechanical parts required for maintenance of the VHF TV exciter.

Replacement parts may be obtained from the Harris Customer Service Department at the following address or by calling 217/222-8200 24 hours a day.

Harris Corporation, Broadcast SystemsDivision
P. O. Box 4290

Quincy, IL 62305

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PWB, EXCITER MOTHERBOARD . . . . . . . . . . . 9928288001 7-11
AURAL CONVERTER PWB . . . . . . . . . . . . . . 9928299001 7-11
VSB/IF AGC BD . . . . . . . . . . . . . . . . . . . . 9928324001 7-13
PWB, DIFF PHASE CORR. . . . . . . . . . . . . . . 9928325001 7-14
CMR FILTER MODULE . . . . . . . . . . . . . . . . . 9928326002 7-16
PC ASSY FIL BOX . . . . . . . . . . . . . . . . . . . 9172100510 7-16
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POWER SUPPLY EXT . . . . . . . . . . . . . . . . . 9928327001 7-17
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MODULE FINAL AMPL . . . . . . . . . . . . . . . . . 9928328001 7-18
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PWB, EXTENDER CARD . . . . . . . . . . . . . . . 9928329001 7-19
PWB, SYNTHESIZER BD \#1 . . . . . . . . . . . . . . 9928347001 7-19
PWB, SYNTHESIZER BD \#2 . . . . . . . . . . . . . . 9928348001 7-21
*PWA, VIDEO BOARD W/VIDEO . . . . . . . . . . . 9929564001 7-23
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TUNED EXCITER CH-13 . . . . . . . . . . . . . . . . . . . 9949253013 7-27

Table 7-1. FORMAT-TUNED EXCITER - 9949253000

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS ( $f$ ) |
| :--- | :--- | :--- | :--- |
| 9928323002 | TUNED RFI AURAL GROUP | 0.0 EA | OPTION QTY 1 REQ |
| 9928527001 | NOTCH DIP/REC EQ BD | 0.0 EA | OPTION QTY 1 REQ |
| 9949155002 | INTERNAL PFC KIT | 0.0 EA | OPTION QTY 1 REQ |
| 9949175002 | EXTERNAL STD PFC KIT | 0.0 EA | OPTION QTY 1 REQ |
| 9949253002 | TUNED EXCITER CH-2 | 0.0 EA | QTY 1 REQ |
| 9949253003 | TUNED EXCITER CH-3 | 0.0 EA | QTY 1 REQ |
| 9949253004 | TUNED EXCITER CH-4 | 0.0 EA | QTY 1 REQ |
| 9949253005 | TUNED EXCITER CH-5 | 0.0 EA | QTY 1 REQ |
| 9949253006 | TUNED EXCITER CH-6 | 0.0 EA | QTY |
|  |  |  | 1 REQ |
| 9949253007 | TUNED EXCITER CH-7 | 0.0 EA | QTY 1 REQ |
| 9949253008 | TUNED EXCITER CH-8 | 0.0 EA | QTY 1 REQ |
| 9949253009 | TUNED EXCITER CH-9 | 0.0 EA | QTY 1 REQ |
| 9949253010 | TUNED EXCITER CH-10 | 0.0 EA | QTY 1 REQ |
| 9949253011 | TUNED EXCITER CH-11 | 0.0 EA | QTY 1 REQ |
| 9949253012 | TUNED EXCITER CH-12 | 0.0 EA | QTY 1 REQ |
| 9949253013 | TUNED EXCITER CH-13 | 0.0 EA | QTY 1 REQ |

Table 7-2. TUNED RFI AURAL GROUP - 9928323002

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS (b) |
| :--- | :--- | :--- | :--- |
| 5450121000 | RES 1M OHM 1/4W 5\% 1206 | 0.0 EA | R005 RO06 ADD FOR SINGLE CAVITY HIGH |
|  |  |  | BAND DIPLEXER QTY 2 |
| 9928323001 | PWB AURAL GROUP DELAY | 1.0 EA |  |

Table 7-3. PWB AURAL GROUP DELAY - 9928323001

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS ( $h$ ) |
| :--- | :--- | :--- | :--- |
| 3581881000 | EJECTOR KIT CARD | 1.0 EA |  |
| 3821140000 | PWR DIVIDER, 2 WAY 90 DEG ESD | 1.0 EA | HY001 |
| 3840431000 | RECT. 1N4001 ESD | 4.0 EA | CR001 CR002 CR004 CR005 |
| 3840720000 | TRANSZORB 1N6377 15V 5W ESD | 1.0 EA | CR003 |
| 4940483000 | INDUCTOR 1880NH 2\% | 2.0 EA | L002 L004 |
| 5170052000 | CAP TRIMMER 0.8-11.0PF | 2.0 EA | C001 C002 |
| 5190014000 | CAP RF CHIP 3.3PF 500V | 2.0 EA | C003 C004 |
| 5450121000 | RES 1M OHM 1/4W 5\% 1206 | 0.0 EA | R005 R006 ADD FOR HIGH BAND SINGLE |
|  |  |  | CAVITY DIPLEXER QTY 2 |
| 5482400201 | RES 100 OHM 1/2W 1\% | 1.0 EA | R004 |
| 5482400273 | RES 562 OHM 1/2W 1\% | 1.0 EA | R001 R002 |
| 5500882000 | POT 100 OHM 1/2W 10\% | 1.0 EA | R003 |
| 5780021000 | RELAY DPDT 12V | 1.0 EA | K001 |
| 6040859000 | SW, TGL DPDT | 1.0 EA | S001 |
| 6100900000 | HEADER 3 CKT STRAIGHT | 1.0 EA | P001 |
| 6121184000 | SHUNT JUMPER 0.1" CENTERS | 1.0 EA | P001 |
| 6200700000 | *RECPT, MALE SMB,PC MOUNT | 2.0 EA | J001 J002 |
| 8220900023 | BRKT, CAP MOUNTING | 2.0 EA | C001 C002 |
| 8220900183 | COIL, L1-L3 | 2.0 EA | L001 L003 |
| 8397900028 | COVER | 2.0 EA |  |
| 8397900492 | SCHEM, AUR GROUP DELAY | 0.0 EA |  |
| 8434999361 | PWB, GROUP DELAY CORR. | 1.0 EA |  |
| 9172100497 | CABLE, EXC 3-1/2" W1 | 1.0 EA | W001 |
| 9172100502 | CABLE EXC 9" W6 | 1.0 EA | W006 |
| 9172100503 | CABLE EXC 10" W7 | 1.0 EA | W007 |

## Table 7-4. NOTCH DIP/REC EQ BD - 9928527001

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS (k) |
| :---: | :---: | :---: | :---: |
| 0000000010 | B/M NOTE: | 0.0 EA | SELECT ON TEST C021 C022 C023 |
| 3581881000 | EJECTOR KIT CARD | 1.0 EA |  |
| 3800125000 | XSTR, NPN 2N4401 ESD | 3.0 EA | Q001 Q003 Q004 |
| 3800126000 | XSTR, PNP 2N4403 ESD | 1.0 EA | Q002 |
| 3821304000 | IC, HA5020 ESD | 13.0 EA | U001 U002 U003 U004 U005 U006 U007 U008 U009 U010 U011 U012 U013 |
| 3840431000 | RECT. 1N4001 ESD | 1.0 EA | CR004 |
| 3840719000 | TRANSZORB 1N6373 5V 5W ESD | 2.0 EA | CR002 CR003 |
| 3840720000 | TRANSZORB 1N6377 15V 5W ESD | 1.0 EA | CR001 |
| 4940239000 | CHOKE WIDE BAND | 2.0 EA | RFOC1 RFOC2 |
| 4940372000 | CHOKE RF 0.10UH | 15.0 EA | L002 L003 L004 L005 L007 L009 L010 L013 L014 L015 L016 L018 L021 L023 L024 |
| 4940404000 | CHOKE RF 33.0UH | 4.0 EA | L017 L019 L020 L022 |
| 5000787000 | CAP, MICA, 200PF 500V 5\% | 1.0 EA | C016 |
| 5000801000 | CAP, MICA, 2PF 500V +/- .5PF | 1.0 EA | C079 |
| 5000809000 | CAP, MICA, 22PF 500V 5\% | 1.0 EA | C014 |
| 5000817000 | CAP, MICA, 47PF 500V 5\% | 2.0 EA | C003 C013 |
| 5000821000 | CAP, MICA, 68PF 500V 5\% | 2.0 EA | C024 C074 |
| 5000826000 | CAP, MICA, 120PF 500V 5\% | 1.0 EA | C001 |
| 5000835000 | CAP, MICA, 470PF 500V 5\% | 1.0 EA | C010 |
| 5000957000 | CAP, MICA, 7PF 500V +/- .5PF | 1.0 EA | C080 |
| 5160453000 | CAP . 1 UF 100V $20 \%$ X7R | 3.0 EA | C004 C006 C008 |
| 5160530000 | CAP .01UF 10\% 100V X7R | 26.0 EA | C026 C028 C030 C032 C034 C036 C038 C040 |
|  |  |  | C042 C044 C046 C048 C050 C052 C054 C056 |
|  |  |  | C058 C060 C062 C064 C066 C068 C070 C072 |
|  |  |  | C075 C076 |
| 5180108000 | CAP, VAR 9-120 PF 100 V | 10.0 EA | C002 C009 C011 C012 C015 C017 C018 C019 |
|  |  |  | C020 |
|  |  |  | C 025 |
| 5220548000 | CAP 10UF 50V 20\% | 26.0 EA | C027 C029 C031 C033 C035 C037 C039 C041 |
|  |  |  | C043 C045 C047 C049 C051 C053 C055 C057 |
|  |  |  | C059 C061 C063 C065 C067 C069 C071 C073 |
|  |  |  | C077 C078 |
| 5220550000 | CAP 100UF 25V 20\% | 2.0 EA | C005 C007 |
| 5482400001 | RES 1 OHM 1/2W 1\% | 4.0 EA | R011 R020 R029 R031 |
| 5482400185 | RES 75 OHM 1/2W 1\% | 19.0 EA | R001 R005 R006 R007 R023 |
|  |  |  | R026 R038 R041 R052 R054 R055 R068 R069 |
|  |  |  | R074 R075 R083 R084 R093 R101 |
| 5482400201 | RES $100 \mathrm{OHM} 1 / 2 \mathrm{~W} 1 \%$ | 7.0 EA | R034 R045 R048 R060 R063 R080 R089 |
| 5482400218 | RES 150 OHM 1/2W 1\% | 8.0 EA | R002 R024 R025 R039 R040 R053 R094 R099 |
| 5482400242 | RES 267 OHM 1/2W 1\% | 1.0 EA | R096 |
| 5482400266 | RES 475 OHM 1/2W 1\% | 4.0 EA | R056 R067 R076 R085 |
| 5482400301 | RES 1 K OHM 1/2W 1\% | 23.0 EA | R010 R017 |
|  |  |  | R022 R032 R033 R046 R047 R058 R059 R065 |
|  |  |  | R066 R077 R078 R086 R087 R090 R091 R092 |
|  |  |  | R095 R098 R100 R102 R013 |
| 5482400305 | RES 1.1K OHM 1/2W $1 \%$ | 1.0 EA | R004 |
| 5482400330 | RES 2K OHM 1/2W 1\% | 3.0 EA | R003 R062 R104 |
| 5482400342 | RES 2.67K OHM 1/2W 1\% | 7.0 EA | R012 R027 R037 R042 R044 R049 R051 |
| 5482400366 | RES 4.75K OHM 1/2W 1\% | 4.0 EA | R019 R071 R072 R081 |
| 5482400385 | RES 7.5K OHM 1/2W 1\% | 3.0 EA | R013 R030 R035 |

5482400434 5482400466 5500628000 5500842000 5500865000 5500901000 6040469000 6100900000 6100933000

6121184000 6200700000 8397994080 8434999463 9172272001

9172272002

9172272003

RES 22.1K OHM 1/2W 1\% 4.0 EA RES 47.5 K OHM 1/2W 1\% 2.0 EA POT 10K OHM .5W 10\% POT 200 OHM 1/2W 10\% POT 1 K OHM 1/2W 10\% POT 500 OHM 1/2W 10\% SW TGL SPDT HEADER 3 CKT STRAIGHT JUMPER, PWB TEST POINT

SHUNT JUMPER 0.1" CENTERS *RECPT, MALE SMB,PC MOUNT SCHEM, NOTCH DIP/REC EQ PWB, NOTCH DIP/REC EQ BD INDUCTOR, 20 UHY CT

INDUCTOR, 38.5 UHY CT

INDUCTOR, 13 UHY CT
1.0 EA
7.0 EA
1.0 EA
6.0 EA
1.0 EA
5.0 EA
7.0 EA
5.0 EA
2.0 EA 0.0 EA 1.0 EA 2.0 EA
3.0 EA
0.0 EA

R009 R015 R016 R018
R008 R014
R105
R021 R028 R036 R043 R064 R079 R088
R061
R050 R057 R070 R073 R082 R097
S001
JP001 JP002 JP003 JP004 JP005
TP001 TP002 TP003 TP004 TP005 TP006 TP007

J002 J003

L011 L012 SELECT QTY 2 FOR SYS M,B, QTY 2 FOR SYS D,I,K1,L
L001 L006 L008 SELECT QTY 3 FOR SYS M,B SELECT QTY
1 FOR SYS D,I,K1,L

Table 7-5. INTERNAL PFC KIT - 9949155002

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS $(d)$ |
| :--- | :--- | :--- | :--- |
| 3060016000 | NUT, HEX KEP 6-32 | 2.0 EA |  |
| 3581073000 | BRAKE FOR KNOBPOT | 1.0 EA | \#R001 |
| 5520781000 | POT 2OK OHM 1.5W | 1.0 EA | R001 |
| 7001251000 | CRYSTAL OSCILLATOR | 1.0 EA |  |
| 8397900503 | SCHEM, INT PFC FREQ STD | 0.0 EA |  |
| 9172100500 | CABLE EXC 8" W4 | 1.0 EA |  |
| 9172100502 | CABLE EXC 9" W6 | 1.0 EA |  |
| 9397900230 | BRKT, POT MTG PFC OPTION | 1.0 EA |  |
| 9992812001 | WIRE/TUBING LIST, INT PFC | 1.0 EA |  |

Table 7-6. EXTERNAL STD PFC KIT - 9949175002

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS (c) |
| :--- | :--- | :--- | :--- |
| 9172100503 | CABLE EXC 10" W7 | 1.0 EA | W007 |
| 9172100508 | CABLE, PFC 15" W16 | 1.0 EA | W016 |

## Table 7-7. BASIC HX1V EXC VIS/AUR - 9928372001

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS (al) |
| :--- | :--- | :--- | :--- |
| 0000000010 | B/M NOTE: | 0.0 EA | FOR SCHEMATIC LIST SEE 939-7911-051 |
| 0074060029 | BRZ, FINGERS TWIST 97-560 | 59.50 IN |  |
| 0074060077 | BRZ,PH FGR STK 97-0621-02 | 12.0 EA | \#NOTES: 24 PIECES 7.7" LG |
| 2500086000 | PLUG/CORD MOLDED BLACK | 1.0 EA |  |
| 3540624000 | TERMINAL, MALE | 2.0 EA |  |
| 3560208000 | CLAMP, FLAT CABLE 2" | 1.0 EA |  |
| 3580165000 | STUD 82 OVAL HEAD | 8.0 EA |  |
| 3580184000 | RETAINER 82 ALL HDS | 16.0 EA | \#USE WITH 1/4 TURN FASTENERS |
| 3581214000 | SCREWLOCK, FEMALE | 1.0 EA | \#JO09 |
| 3581965000 | STUD 82-11-320-16 | 8.0 EA |  |
| 3582104000 | CARD GUIDE | 26.0 EA |  |
| 3582613000 | RECEPTACLE, 82 LEAFSPRING | 16.0 EA |  |

3583283000 3583561000 3583562000 3821636000 4020020000 4140240000 4240001000 4300030001 4300192000 4480512000 4480933000 5560049000 6100738000 6101113000 6201563000 6202109000 8150365001 8152324001

8220900106
8220900371
8397900050
8397900463
8397900464
8397900465
8397900466
8397900467
8397900541
8434999143
8434999144
8434999350
9148789002
9172100208
9172100210
9172100497
9172100498 9172100499 9172100500 9172100501 9172100502 9172100503 9172100504 9172100505 9172100506 9172100507 9172100508

9172100558 9172100559 9172100560 9172315251 9172456072 9397900051 9397900235 9397900486 9397900488

| SLIDE, FULL EXT DRAWER | 1.0 EA |  |
| :---: | :---: | :---: |
| SPRING CLIP 0.50 DIA | 0.0 EA | FD PART HB (4 REQ) |
| SPRING CLIP 0.75 DIA | 0.0 EA | FD PART LB (4 REQ) |
| MIXER W/BNC CONNECTOR ESD | 1.0 EA | MX001 |
| CLIP, FUSE | 2.0 EA | \#USE ON 943-4999-346 |
| CORE BALUN | 1.0 EA |  |
| GROMMET 3/8 MTG DIA | 1.0 EA |  |
| FAN 115VAC 106CFM 4.69"SQ | 1.0 EA |  |
| FINGER GUARD, 119MM FAN | 1.0 EA |  |
| FILTER SLIMLINE | 1.0 EA |  |
| HINGE DOOR POSITIONING | 2.0 EA |  |
| ATTEN, COAX, BNC, 6DB, 2W | 1.0 EA |  |
| PLUG HOUSING | 1.0 EA |  |
| PLUG/RECP, D, 37PIN | 1.0 EA |  |
| POWER SPLITTER | 1.0 EA | HY1 |
| JACK, BNC 75 OHM BULKHEAD | 1.0 EA |  |
| BANDPASS FILTER | 0.0 EA | FD PART HB |
| BANDPASS FILTER | 0.0 EA | FD PART |
|  |  | LB |
| LARGE WINDOW EXCITER | 1.0 EA |  |
| SHIPPING LABEL | 0.0 EA |  |
| BRKT, PLUNGER | 1.0 EA |  |
| COVER DUAL PC BD | 1.0 EA |  |
| COVER END PC BD | 2.0 EA |  |
| COVER SINGLE PC BD | 9.0 EA |  |
| BAR FRONT | 1.0 EA |  |
| BAR TOP COVER | 1.0 EA |  |
| WIRING DIAG, HXIV EXC. | 0.0 EA |  |
| PANEL EXCIT MTG-UPPER | 1.0 EA |  |
| PANEL EXCIT MTG-LOWER | 1.0 EA |  |
| SUPPORT MTHBOARD | 1.0 EA |  |
| MIXER PLATE | 1.0 EA |  |
| CABLE EXC AMP | 2.0 EA | W012 RIBBON |
| CABLE EXC METER M/B | 1.0 EA | W013 |
| CABLE, EXC 3-1/2" W 1 | 3.0 EA | W001 |
| CABLE EXC 5" W2 | 1.0 EA | W002 |
| CABLE EXC $7^{\prime \prime}$ W3 | 1.0 EA | W003 |
| CABLE EXC 8" W4 | 2.0 EA | W004 |
| CABLE EXC 7" W5 | 2.0 EA | W005 |
| CABLE EXC 9" W6 | 7.0 EA | W006 |
| CABLE EXC 10" W7 | 4.0 EA | W007 |
| CABLE EXC 12" W8 | 1.0 EA | W008 |
| CABLE EXC 13" W9 | 4.0 EA | W009 |
| CABLE EXC 9" W10 | 2.0 EA | W010 |
| RIBBON CABLE EXC 43" W14 | 1.0 EA | W014 |
| CABLE, PFC $15{ }^{\prime \prime}$ W16 | 0.0 EA | W016 \#PFC CABLE IS AN OPTION QTY 1 REQ'D |
| CABLE COAX 50 OHM 14" | 2.0 EA | W011 |
| CABLE COAX 50 OHM 9" | 2.0 EA | W022 |
| CABLE COAX 50 OHM 12" | 1.0 EA | W023 |
| CABLE EXCITER 14" W251 | 1.0 EA | W251 |
| CABLE, VIDEO IN $11^{\prime \prime}$ W12 | 1.0 EA | W012 COAX |
| BRKT, PLUNGER ASSY | 1.0 EA |  |
| TOOL, EXCITER ALIGNMENT | 1.0 EA |  |
| BAR, TOP FRONT | 1.0 EA |  |
| BAR BOTTOM FRONT | 2.0 EA |  |

9434999087
9434999332
9434999337
9434999338
9434999339
9434999346
9434999356
9434999383
9434999402
9434999861
9928001002
9928260001
9928262001
9928288001
9928299001
9928323001

9928324001
9928325001
9928326002
9928327001
9928328001
9928329001
9928347001
9928348001
9928527001
9929564001 .

| BLANK 19.0" EXTRUSION | 2.0 EA |
| :--- | :--- |
| FRT PANEL EXCITER | 1.0 EA |
| CAGE FRT ASSY | 1.0 EA |
| CAGE REAR ASSY | 1.0 EA |
| DIVIDER CARD CAGE | 11.0 EA |
| COVER TOP REAR | 1.0 EA |
| PLATE PWR AMP ASSY | 1.0 EA |
| COVER TOP EXCITER HXIV | 1.0 EA |
| PANEL REAR EXCITER | 1.0 EA |
| CHASSIS EXCITER | 1.0 EA |
| PWB, METERING \& CONTROL | 1.0 EA |
| PWB, MOD/DELAY COMP. | 1.0 EA |
| PWB, LIN/QUAD CORR. | 1.0 EA |
| PWB, EXCITER MOTHERBOARD | 1.0 EA |
| AURAL CONVERTER PWB | 1.0 EA |
| PWB AURAL GROUP DELAY | 0.0 EA |
|  |  |
| VSB/IF AGC BD | 1.0 EA |
| PWB, DIFF PHASE CORR. | 1.0 EA |
| CMR FILTER MODULE | 1.0 EA |
| POWER SUPPLY EXT | 1.0 EA |
| MODULE FINAL AMPL | 2.0 EA |
| PWB, EXTENDER CARD | 1.0 EA |
| PWB, SYNTHESIZER BD \#1 | 1.0 EA |
| PWB, SYNTHESIZER BD \#2 | 1.0 EA |
| NOTCH DIP/REC EQ BD | 0.0 EA |
| *PWA, VIDEO BOARD W/VIDEO | 1.0 EA |

\#GROUP DELAY PWB IS AN OPTION QTY 1 REQUIRED
\#OPTION QTY 1 REQD WHENUSED.

Table 7-8. PWB, METERING \& CONTROL - 9928001002

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS (h) |
| :---: | :---: | :---: | :---: |
| 3582827000 | SPACER, LED MOUNT . 25 LG | 8.0 EA | \#DS005 \#DS006 \#DS007 \#DS008 \#DS009 |
|  |  |  | \#DS010 \#DS011 \#DS012 |
| 3800319000 | XSTR, MPS-A14 ESD | 2.0 EA | Q001 Q002 |
| 3800713000 | DARLINGTON TRANSISTOR PNP ESD | 7.0 EA | Q003 Q004 Q005 Q006 Q007 Q008 Q009 |
| 3820285000 | IC CD4029BE ESD | 6.0 EA | U009 U010 U011 U012 U013 U014 |
| 3820523000 | IC, 4066/14066 ESD | 2.0 EA | U019 U022 |
| 3820587000 | IC, CD4011/MC14011 ESD | 5.0 EA | U001 U002 U004 U005 U021 |
| 3820593000 | IC TL072ACP ESD | 4.0 EA | U017 U018 U027 |
|  |  |  | U028 |
| 3820618000 | IC, 4081/14081 ESD | 2.0 EA | U003 U026 |
| 3820626000 | IC, 4093B/14093B ESD | 2.0 EA | U006 U020 |
| 3820711000 | PRECISION IC MULTIPLIER ESD | 1.0 EA | U029 |
| 3820718000 | IC, AD7525KN ESD | 2.0 EA | U015 U016 |
| 3821008000 | IC, LM3914N ESD | 2.0 EA | U023 U024 |
| 3821026000 | IC, 4046B/14046 ESD | 2.0 EA | U007 U008 |
| 3821147000 | CONVERTER A/D 3-1/2 DIGIT ESD | 1.0 EA | U025 |
| 3840205000 | DIODE SILICON 1N914/4148 ESD | 5.0 EA | CR001 CR002 CR014 CR015 CR016 |
| 3840431000 | RECT. 1N4001 ESD | 1.0 EA | CR003 |
| 3840610000 | LED, GREEN ESD | 1.0 EA | DS005 |
| 3840611000 | LED, RED ESD | 7.0 EA | DS006 DS007 DS008 DS009 |
|  |  |  | DS010 DS011 DS012 |
| 3840719000 | TRANSZORB 1N6373 5V 5W ESD | 2.0 EA | CR010 CR013 |
| 3840720000 | TRANSZORB 1N6377 15V 5W ESD | 2.0 EA | CR011 CR012 |
| 3840823000 | LED 10 SEG BARGRAPH, RED ESD | 2.0 EA | DS003 DS004 |
| 3840824000 | LED DISPLAY . 560 INCH ESD | 2.0 EA | DS001 DS002 |

3860085000 5060244000 5060246000 5160453000

5160530000

5160725000 5160765000 5220548000 5260374000 5482400130 5482400269 5482400301

5482400305
5482400337
5482400366
5482400401

5482400418
5482400430
5482400459
5482400469
5482400477
5482400489
5482400501
5482400566 5482400601 5500950000 5500953000 5500960000 6041111000 6041112000 6100828000 6100900000 6100933000 6121184000 6121295000 8397900027 8434999038

ZENER, 1N4740A 10V ESD
CAP .22UF $63 \mathrm{~V} 5 \%$
CAP 0.47UF $63 \mathrm{~V} 5 \%$
CAP. 1 UF $100 \mathrm{~V} 20 \%$ X7R
CAP . 01 UF $10 \% 100 \mathrm{~V} \times 7 \mathrm{R}$

CAP 1.OUF 50V 20\%
CAP 10PF 5\% 100V C0G
CAP 10UF 50V 20\%
CAP 1.0F 5.5 V
RES 20 OHM 1/2W 1\%
RES 511 OHM 1/2W 1\%
RES 1K OHM 1/2W 1\%
RES 1.1 K OHM $1 / 2 \mathrm{~W} 1 \%$
RES 2.37 K OHM $1 / 2 \mathrm{~W} 1 \%$
RES 4.75K OHM 1/2W $1 \%$
RES 10K OHM 1/2W 1\%

RES 15 K OHM $1 / 2 \mathrm{~W} 1 \%$
RES 20 K OHM $1 / 2 \mathrm{~W} 1 \%$
RES 40.2 K OHM $1 / 2 \mathrm{~W} 1 \%$
RES 51.1 K OHM $1 / 2 \mathrm{~W} 1 \%$
RES 61.9 K OHM $1 / 2 \mathrm{~W} 1 \%$
RES 82.5 K OHM $1 / 2 W 1 \%$
RES 100 K OHM $1 / 2 W 1 \%$

RES 475 K OHM $1 / 2 W 1 \%$
RES 1 MEG OHM $1 / 2 W 1 \%$
POT 2000 OHM $1 / 2 W 10 \%$
POT 20K .5W MULTITURN
POT 1 K OHM
SW PB GRAY MOM W/O LED
SW PB GRAY MOM W/GRN LED
HEADER, 26 PIN PC RIBBON
HEADER 3 CKT STRAIGHT
JUMPER, PWB TEST POINT
SHUNT JUMPER 0.1" CENTERS
CONN, 37 PIN, STRAIGHT, D RECP
SCHEM, METER \& CONTROL
PWB, METER BOARD

| 1.0 EA | CR004 |
| :---: | :---: |
| 1.0 EA | C011 |
| 1.0 EA | C010 |
| 10.0 EA | C001 C005 C009 C017 C018 C033 C034 C035 |
|  | C036 C043 |
| 20.0 EA | C003 C007 C012 C019 |
|  | C020 C021 C025 C026 C027 C028 C029 C030 |
|  | C031 C032 C037 C038 C039 C040 C041 C042 |
| 2.0 EA | C002 C006 |
| 1.0 EA | C008 |
| 4.0 EA | C013 C014 C015 C016 |
| 1.0 EA | C004 |
| 1.0 EA | R011 |
| 1.0 EA | R080 |
| 8.0 EA | R007 R009 R010 R018 R020 R021 |
|  | R076 R077 |
| 1.0 EA | R029 |
| 1.0 EA | R030 |
| 2.0 EA | R003 R014 |
| 32.0 EA | R001 R002 R012 R013 R022 R023 R024 R025 |
|  | R026 R027 R038 R039 R040 R041 R042 R043 |
|  | R044 R045 R046 R047 R048 R049 R050 R051 |
|  | R052 R053 R054 R055 R056 R057 R071 R081 |
| 1.0 EA | R033 |
| 1.0 EA | R028 |
| 1.0 EA | R037 |
| 2.0 EA | R063 R067 |
| 1.0 EA | R036 |
| 4.0 EA | R004 R005 R015 R016 |
| 11.0 EA | R006 R017 R031 R062 R065 R066 R068 R069 |
|  | R070 R078 R079 |
| 1.0 EA | R034 |
| 1.0 EA | R035 |
| 2.0 EA | R008 R019 |
| 1.0 EA | R032 |
| 4.0 EA | R058 R060 R061 R064 |
| 4.0 EA | SW001 SW002 SW003 SW004 |
| 2.0 EA | SW5/DS013 SW6/DS014 |
| 1.0 EA | J001 |
| 2.0 EA | \#JP001 \#JP002 |
| 1.0 EA | TP001 |
| 2.0 EA | JP001 JP002 |
| 1.0 EA | J002 |
| 0.0 EA |  |
| 1.0 EA |  |

Table 7-9. PWB, MOD/DELAY COMP. - 9928260001

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS $(g)$ |
| :--- | :--- | :--- | :--- |
| 3581881000 | EJECTOR KIT CARD | 1.0 EA |  |
| 3800114000 | *XSTR, NPN, 2N5109 ESD | 7.0 EA | Q001 Q003 Q004 Q101 Q102 Q105 Q106 |
| 3800536000 | XSTR, NPN, 2N5179 ESD | 3.0 EA | Q002 Q103 Q104 |
| 3821225000 | IC, ASK-1 ESD | 1.0 EA | MX001 |
| 3840361000 | DIODE HP5082-3077/A5S377 ESD | 4.0 EA | CR101 CR102 CR103 CR104 |
| 3840431000 | RECT. 1N4001 ESD | 2.0 EA | CR105 CR106 |
| 3840720000 | TRANSZORB 1N6377 15V 5W ESD | 2.0 EA | CR007 CR008 |

3840838000 4040198000

4040264000 4780392000 4940239000 4940375000 4940376000 4940378000 4940383000 4940384000 4940388000 4940398000 4940446000

5000804000 5000807000 5000808000 5000809000 5000840000 5000957000 5160530000 5160736000

| TRANSZORB 1 N6380 36V 5W ESD SPACER TO-5, TO-9, TO-11 |
| :---: |
| HEAT SINK FOR TO-5 CASE |
| XFMR, RF MODEL T4-1 |
| CHOKE WIDE BAND |
| CHOKE RF 0.18UH |
| CHOKE RF 0.22UH |
| CHOKE 0.33UH 10\% 780MA |
| CHOKE RF 0.82UH |
| CHOKE RF 1.00 UH |
| CHOKE RF 2.20 UH |
| CHOKE RF 10.0UH +/-10\% |
| CHOKE POWER LINE 100UH |
| CAP, MICA, $10 \mathrm{PF} 500 \mathrm{~V}+/-.5 \mathrm{PF}$ |
| CAP, MICA, 18PF 500V $5 \%$ |
| CAP, MICA, 20PF 500V $5 \%$ |
| CAP, MICA, 22PF 500V 5\% |
| CAP, MICA, 680PF 300V 5\% |
| CAP, MICA, 7PF 500V +/- .5PF |
| CAP .01UF 10\% 100V X7R |
| CAP .001UF 10\% 100V X7R |

5160891000 5180045000 5200446000 5200448000 5220548000 5220561000 5482400101 5482400105 5482400118 5482400134 5482400147 5482400158 5482400166 5482400169 5482400181

5482400185 5482400201 5482400205 5482400209 5482400218 5482400226 5482400230 5482400234 5482400247 5482400251 5482400258 5482400262

CAP 0.100 UF $10 \% 50 \mathrm{~V}$ CAP VAR 9-35PF 200 V CAP, VAR .8-10PF CAP, VAR .8-14PF CAP 10UF $50 \mathrm{~V} 20 \%$ CAP 100UF $63 \mathrm{~V} 20 \%$ RES 10 OHM $1 / 2 \mathrm{~W} 1 \%$ RES 11 OHM $1 / 2 \mathrm{~W} 1 \%$ RES 15 OHM $1 / 2 \mathrm{~W} 1 \%$
RES 22.1 OHM 1/2W 1\%
RES 30.1 OHM 1/2W 1\%
RES 39.2 OHM 1/2W 1\%
RES 47.5 OHM $1 / 2 W 1 \%$
RES 51.1 OHM 1/2W 1\%
RES 68.1 OHM 1/2W 1\%
RES 75 OHM $1 / 2 \mathrm{~W} 1 \%$
RES 100 OHM $1 / 2 W 1 \%$
RES 110 OHM $1 / 2 W 1 \%$
RES 121 OHM $1 / 2 W 1 \%$
RES 150 OHM $1 / 2 \mathrm{~W} 1 \%$
RES 182 OHM $1 / 2 W 1 \%$
RES 200 OHM $1 / 2 W 1 \%$
RES 221 OHM 1/2W 1\%
RES 301 OHM 1/2W 1\%
RES 332 OHM 1/2W 1\%
RES 392 OHM $1 / 2 W 1 \%$
RES 432 OHM $1 / 2 W 1 \%$

| 1.0 EA | CR009 |
| :---: | :---: |
| 7.0 EA | XQ001 XQ003 XQ004 XQ101 XQ102 XQ105 |
|  | XQ106 |
| 1.0 EA | XQ001 |
| 4.0 EA | T001 T002 T101 T102 |
| 4.0 EA | L103 L104 L113 L114 |
| 1.0 EA | L003 |
| 4.0 EA | L109 L110 L115 L116 |
| 2.0 EA | L101 L102 |
| 1.0 EA | L004 |
| 4.0 EA | L105 L106 L111 L112 |
| 1.0 EA | L002 |
| 3.0 EA | L006 L107 L108 |
| 2.0 EA | L001 |
|  | L005 |
| 2.0 EA | C138 C139 |
| 1.0 EA | C013 |
| 1.0 EA | C012 |
| 4.0 EA | C103 C104 C107 C108 |
| 1.0 EA | C020 |
| 2.0 EA | C111 C112 |
| 1.0 EA | C019 |
| 41.0 EA | C001 C002 C003 C005 C007 C008 C009 C014 |
|  | C016 C018 C021 C023 C025 C027 C029 C101 |
|  | C102 |
|  | C105 C106 C113 C114 C115 C116 C117 C118 |
|  | C119 C120 C123 C124 C125 C126 C127 C128 |
|  | C129 C130 C131 C132 C133 C134 C136 C137 |
| 5.0 EA | C015 C022 C024 C026 C028 |
| 2.0 EA | C121 C122 |
| 1.0 EA | C011 |
| 2.0 EA | C109 C110 |
| 1.0 EA | C135 |
| 3.0 EA | C004 C006 C017 |
| 5.0 EA | R005 R135 R136 R139 R140 |
| 1.0 EA | R022 |
| 1.0 EA | R019 |
| 6.0 EA | R033 R034 R145 R146 R153 R154 |
| 1.0 EA | R110 |
| 2.0 EA | R021 R029 |
| 3.0 EA | R109 R125 R126 |
| 3.0 EA | R016 R123 R124 |
| 3.0 EA | R006 R119 |
|  | R120 |
| 2.0 EA | R121 R122 |
| 5.0 EA | R009 R018 R025 R101 R102 |
| 1.0 EA | R007 |
| 2.0 EA | R133 R134 |
| 2.0 EA | R103 R104 |
| 2.0 EA | R117 R118 |
| 2.0 EA | R035 R036 |
| 4.0 EA | R141 R142 R143 R144 |
| 2.0 EA | R004 R011 |
| 2.0 EA | R027 R032 |
| 4.0 EA | R113 R114 R115 R116 |
| 2.0 EA | R137 R138 |

5482400266
5482400277
5482400293
5482400301
5482400321
5482400326
5482400330
5482400334
5482400366

5482400381
5500841000
5500842000
5500865000
5500901000
6040469000
6100679000
6100933000
6120775000
6200700000
8397900443
8434999324

RES 475 OHM 1/2W $1 \%$
RES 619 OHM 1/2W 1\% RES 909 OHM 1/2W 1\% RES 1K OHM 1/2W 1\% RES 1.62 K OHM $1 / 2 \mathrm{~W} 1 \%$ RES 1.82K OHM 1/2W 1\% RES 2K OHM 1/2W 1\% RES 2.21K OHM 1/2W 1\% RES 4.75K OHM 1/2W 1\%

RES 6.81K OHM 1/2W 1\%
POT 50 OHM 1/2W 10\% POT 200 OHM 1/2W 10\% POT 1 K OHM $1 / 2 W 10 \%$ POT 500 OHM 1/2W 10\% SW TGL SPDT PLUG, SHORTING, . $25^{\prime \prime}$ CTRS JUMPER, PWB TEST POINT JACK, PC MT, . 040 PINS *RECPT, MALE SMB,PC MOUNT SCHEM, MOD. DELAY PWB, MOD DELAY

| 2.0 EA | R008 R013 |
| :--- | :--- |
| 2.0 EA | R107 R108 |
| 1.0 EA | R030 |
| 1.0 EA | R017 |
| 4.0 EA | R111 R112 R129 R130 |
| 2.0 EA | R003 R038 |
| 1.0 EA | R031 |
| 3.0 EA | R002 R127 R128 |
| 6.0 EA | R014 R015 R023 |
|  | R024 R026 R028 |
| 2.0 EA | R131 R132 |
| 3.0 EA | R001 R105 R106 |
| 2.0 EA | R020 R037 |
| 3.0 EA | R010 R012 R040 |
| 2.0 EA | R147 R148 |
| 2.0 EA | S101 S102 |
| 2.0 EA | P001 P002 |
| 1.0 EA | TP001 |
| 6.0 EA | P1-1 P1-2 P1-3 P2-1 P2-2 P2-3 |
| 3.0 EA | J001 J002 J003 |
| 0.0 EA |  |
| 1.0 EA |  |

Table 7-10. PWB, LIN/QUAD CORR. - 9928262001

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS (I) |
| :---: | :---: | :---: | :---: |
| 3581881000 | EJECTOR KIT CARD | 1.0 EA |  |
| 3800114000 | *XSTR, NPN, 2N5109 ESD | 6.0 EA | Q002 Q004 Q005 Q102 Q104 Q105 |
| 3800536000 | XSTR, NPN, 2N5179 ESD\| | 4.0 EA | Q001 Q003 Q101 Q103 |
| 3800622000 | XSTR, N -JFET U310 ESD | 1.0 EA | Q106 |
| 3820415000 | IC, 324 ESD | 4.0 EA | U001 U002 U101 U102 |
| 3840252000 | DIODE HP5082-2900/AHR2900 ESD | 18.0 EA | CR001 CR002 CR003 CR004 CR005 CR006 |
|  |  |  | CR007 CR008 CR009 CR101 CR102 CR103 |
|  |  |  | CR104 CR105 CR106 CR107 CR108 CR109 |
| 3840431000 | RECT. 1N4001 ESD | 2.0 EA | CR010 CR011 |
| 3840720000 | TRANSZORB 1N6377 15V 5W ESD | 2.0 EA | CR013 CR014 |
| 3840838000 | TRANSZORB 1N6380 36V 5W ESD | 1.0 EA | CR012 |
| 4040198000 | SPACER TO-5, TO-9, TO-11 | 6.0 EA | XQ002 XQ004 XQ005 XQ102 XQ104 XQ105 |
| 4040660000 | HEAT SINK | 1.0 EA | XQ106 |
| 4040725000 | HEAT SINK TO-5 CASE | 6.0 EA | XQ002 XQ004 XQ005 XQ102 XQ104 XQ105 |
| 4780412000 | XFMR RF T9-1 | 1.0 EA | T101 |
| 4940239000 | CHOKE WIDE BAND | 2.0 EA | L010 L110 |
| 4940262000 | CHOKE RF 10UH 10\% | 16.0 EA | L001 L002 L003 L004 L005 L006 L007 L008 |
|  |  |  | L101 |
|  |  |  | L102 L103 L104 L105 L106 L107 L108 |
| 4940376000 | CHOKE RF 0.22UH | 2.0 EA | L009 L109 |
| 4940446000 | CHOKE POWER LINE 100UH | 2.0 EA | L011 L012 |
| 5000753000 | CAP, MICA, 56PF 500V 5\% | 3.0 EA | C022 C023 C122 |
| 5000759000 | CAP, MICA, 100PF 500V 5\% | 2.0 EA | C123 C124 |
| 5000761000 | CAP, MICA, 150PF 500V 5\% | 1.0 EA | C024 |
| 5000811000 | CAP, MICA, 27PF 500V 5\% | 2.0 EA | C012 C112 |
| 5000822000 | CAP, MICA, 75PF 500V 5\% | 2.0 EA | C011 C111 |
| 5160453000 | CAP .1UF 100V 20\% X7R | 16.0 EA | C006 $\mathrm{C007} \mathrm{C} 008 \mathrm{C009} \mathrm{C} 015 \mathrm{C016} \mathrm{C017} \mathrm{C018}$ |
|  |  |  | C106 |
|  |  |  | C107 C108 C109 C115 C116 C117 C118 |
| 5160530000 | CAP .01UF 10\% 100V X7R | 28.0 EA |  |


| 5160736000 | CAP .001UF 10\% 100V X7R | 16.0 EA | C002 C013 $\mathrm{C} 019 \mathrm{C021} \mathrm{C} 056 \mathrm{C} 057 \mathrm{C} 058$ |
| :---: | :---: | :---: | :---: |
|  |  |  | C059 C060 C113 C119 C121 C132 C133 C159 |
|  |  |  | C160 |
| 5160891000 | CAP 0.100UF 10\% 50V | 7.0 EA | C004 C044 C045 C102 C104 C144 C145 |
| 5220561000 | CAP 100UF 63V 20\% | 5.0 EA | C029 C030 C129 C130 C161 |
| 5260049000 | CAP 6.8UF 35V 20\% | 16.0 EA | C025 C026 C027 C028 C034 C035 C036 C037 |
|  |  |  | C125 C126 C127 C128 C134 C135 C136 C137 |
| 5260311000 | CAP 2.2UF 35V 10\% | 4.0 EA | C038 |
|  |  |  | C039 C138 C139 |
| 5401334000 | RES NETWORK 15K OHM | 2.0 EA | R057 R157 |
| 5401600213 | RES 330 OHM 3W 5\% | 2.0 EA | R017 R117 |
| 5401600216 | RES 430 OHM 3W 5\% | 2.0 EA | R007 R107 |
| 5482400101 | RES 10 OHM 1/2W 1\% | 6.0 EA | R063 R064 R065 R163 R164 R165 |
| 5482400121 | RES 16.2 OHM 1/2W 1\% | 1.0 EA | R162 |
| 5482400147 | RES 30.1 OHM 1/2W 1\% | 1.0 EA | R154 |
| 5482400166 | RES 47.5 OHM 1/2W 1\% | 2.0 EA | R028 R128 |
| 5482400169 | RES 51.1 OHM 1/2W 1\% | 4.0 EA | R001 R066 R070 R101 |
| 5482400177 | RES 61.9 OHM 1/2W 1\% | 2.0 EA | R005 R105 |
| 5482400185 | RES 75 OHM 1/2W 1\% | 1.0 EA | R158 |
| 5482400201 | RES 100 OHM 1/2W 1\% | 2.0 EA | R159 R160 |
| 5482400205 | RES $110 \mathrm{OHM} 1 / 2 \mathrm{~W} 1 \%$ | 1.0 EA | R120 |
| 5482400218 | RES 150 OHM 1/2W 1\% | 2.0 EA | R054 R161 |
| 5482400226 | RES 182 OHM 1/2W 1\% | 1.0 EA | R008 |
| 5482400234 | RES 221 OHM 1/2W 1\% | 2.0 EA | R026 R126 |
| 5482400237 | RES 237 OHM 1/2W 1\% | 4.0 EA | R009 R023 R109 R123 |
| 5482400247 | RES 301 OHM 1/2W 1\% | 5.0 EA | R006 R015 R106 R108 R115 |
| 5482400258 | RES 392 OHM 1/2W 1\% | 2.0 EA | R027 R127 |
| 5482400262 | RES 432 OHM 1/2W 1\% | 2.0 EA | R019 R020 |
| 5482400285 | RES 750 OHM 1/2W 1\% | 5.0 EA | R004 R014 R104 R114 R119 |
| 5482400318 | RES 1.5K OHM 1/2W $1 \%$ | 6.0 EA | R041 R068 R069 R141 R168 R169 |
| 5482400330 | RES 2K OHM 1/2W 1\% | 16.0 EA | R029 R030 R031 R032 R033 R034 R035 R036 |
|  |  |  | R129 R130 R131 R132 R133 R134 R135 R136 |
| 5482400334 | RES 2.21 K OHM 1/2W 1\% | 4.0 EA | R055 R056 R155 R156 |
| 5482400342 | RES 2.67 K OHM 1/2W 1\% | 2.0 EA | R003 R103 |
| 5482400358 | RES 3.92K OHM 1/2W 1\% | 2.0 EA | R013 R113 |
| 5482400385 | RES 7.5K OHM 1/2W 1\% | 8.0 EA | R044 R047 R050 R053 R144 |
|  |  |  | R147 R150 R153 |
| 5482400393 | RES 9.09 K OHM 1/2W 1\% | 2.0 EA | R002 R102 |
| 5482400401 | RES 10K OHM 1/2W 1\% | 4.0 EA | R024 R025 R124 R125 |
| 5482400426 | RES 18.2K OHM 1/2W 1\% | 2.0 EA | R012 R112 |
| 5500842000 | POT 200 OHM 1/2W 10\% | 2.0 EA | R011 R111 |
| 5500865000 | POT 1 K OHM 1/2W 10\% | 14.0 EA | R010 R021 R022 R037 R038 R039 R040 R110 |
|  |  |  | R121 R122 R137 R138 R139 R140 |
| 6040859000 | SW, TGL DPDT | 2.0 EA | S001 S101 |
| 6100679000 | PLUG, SHORTING, .25" CTRS | 9.0 EA | P001 P001A P002 |
|  |  |  | P003 P004 P005 P006 P101 P102 |
| 6120775000 | JACK, PC MT, . 040 PINS | 26.0 EA | P1-2 P1-4 P1-3 P1-1 P3-3 P3-1 P3-2 P2-3 P2- |
|  |  |  | 1 P2-2 P4-3 P4-1 P4-4 P4-2 P6-3 P6-1 P6-2 |
|  |  |  | P101-1 P101-2 P101-3 P102-3 P102-1 P102-2 |
|  |  |  | P5-1 P5-2 P5-3 |
| 6200700000 | *RECPT, MALE SMB,PC MOUNT | 4.0 EA | J001 J002 J003 J004 |
| 6201955000 | HYBRID, QUADRATURE | 1.0 EA | HY001 |


| 8397900444 | SCHEM, LIN/QUAD CORR. | 0.0 EA |
| :--- | :--- | :--- |
| 8434999325 | PWB, LIN/QUAD CORR. | 1.0 EA |

Table 7-11. PWB, EXCITER MOTHERBOARD - 9928288001

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS (c) |
| :---: | :---: | :---: | :---: |
| 5160736000 | CAP .001UF 10\% 100V X7R | 31.0 EA | C003 C006 C009 C012 C015 C016 C017 C018 |
|  |  |  | C019 C020 C021 C022 C023 C024 C025 C026 |
|  |  |  | C027 C028 C029 C030 C031 C032 C033 C034 |
|  |  |  | C035 C036 C037 C038 C039 C040 C048 |
| 5160777000 | CAP 100PF 5\% 100V C0G | 5.0 EA | C041 C042 C043 C044 C045 |
| 5160891000 | CAP 0.100UF 10\% 50V | 5.0 EA | C002 C005 C008 C011-014 |
| 5220548000 | CAP 10UF 50V 20\% | 5.0 EA | C001 C004 C007 C010 C013 |
| 6100679000 | PLUG, SHORTING, . $25{ }^{\prime \prime}$ CTRS | 3.0 EA | P001 P002 P003 |
| 6100828000 | HEADER, 26 PIN PC RIBBON | 1.0 EA | J019 |
| 6100848000 | HEADER, STRAIGHT 2 POS | 4.0 EA |  |
| 6101027000 | HEADER, MALE 12 PIN | 2.0 EA | J018 J020 |
| 6101064000 | HDR, 10 PIN PC RBN | 2.0 EA | J016 J017 |
| 6120904000 | JACK, PC MT GOLD PLATED | 9.0 EA | \#3 USED WITH P001 \#3 USED WITH P002 \#3 USED WITH P003 |
| 6121184000 | SHUNT JUMPER 0.1" CENTERS | 4.0 EA |  |
| 6121309000 | CONN, PC EDGE 56 CONT | 13.0 EA | J001 J002 J003 J004 |
|  |  |  | J005 J006 J007 J008 J009 J010 J011 J012 J013 |
| 8397900475 | SCHEM, MOTHERBOARD | 0.0 EA |  |
| 8434999352 | PWB, MOTHERBOARD EXC | 1.0 EA |  |

Table 7-12. AURAL CONVERTER PWB - 9928299001

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS ( $w$ ) |
| :--- | :--- | :--- | :--- |
| 3581881000 | EJECTOR KIT CARD | 1.0 EA |  |
| 3581928000 | JUMPER 1/4 LG 1/8H | 19.0 EA |  |
| 3800189000 | XSTR, NPN 2N3904 ESD | 3.0 EA | Q003 Q004 Q005 |
| 3800707000 | XSTR, NPN BFR96 ESD | 2.0 EA | Q001 Q002 |
| 3820361000 | IC, IFC SRA-1 ESD | 1.0 EA | MX001 |
| 3820443000 | IC, CD4053BE ESD | 1.0 EA | U014 |
| 3820749000 | IC NE5532A ESD | 7.0 EA | U009 U010 U011 U012 U019 U020 U021 |
| 3820905000 | IC, 78L08/78L82 ESD | 6.0 EA | U002 U005 U007 U013 U017 U023 |
| 3820907000 | IC MC145152P2 ESD | 1.0 EA | U008 |
| 3821126000 | IC 78L12A ESD | 2.0 EA | ESD U001 U016 |
| 3830189000 | IC, SA5205A ESD | 4.0 EA | U003 |
|  |  |  | U004 U015 U022 |
| 3830346000 | *IC, MC12019 ESD | 2.0 EA | U006 U018 |
| 3840205000 | DIODE SILICON 1N914/4148 ESD | 12.0 EA | CR012 CR013 CR014 CR015 CR016 CR017 |
|  |  |  | CR018 CR019 CR020 CR021 CR022 CR023 |
| 3840611000 | LED, RED ESD | 1.0 EA | DS001 |
| 3840720000 | TRANSZORB 1N6377 15V 5W ESD | 2.0 EA | CR010 CR011 |
| 4040509000 | SOCKET IC 28 PIN | 1.0 EA | XU008 |
| 4040673000 | SOCKET 8 PIN DIP (DL) | 12.0 EA | XU003 XU004 XU009 XU010 XU0111 XU012 |
|  |  |  | XU015 XU018 XU019 XU020 XU021 XU022 |
| 4040675000 | SOCKET IC 16 CONT | 1.0 EA | XU014 |
| 4040873000 | SOCKET ADAPTER SOIC8-DIP8 | 5.0 EA | \#U003 \#U004 \#U015 \#U018 \#U022 |
| 4920636000 | COIL, VAR .366-.627UH | 1.0 EA | L001 |
| 4920765000 | FIXED RF INDUCTOR 345NH | 4.0 EA | L002 L003 L009 L010 |
| 4920769000 | FIXED RF INDUCTOR 600NH | 1.0 EA | L008 |


| 4940394000 | CHOKE 6.80UH | 2.0 EA | L004 L005 |
| :---: | :---: | :---: | :---: |
| 4940446000 | CHOKE POWER LINE 100UH | 2.0 EA | L006 L007 |
| 5001296000 | CAP 430PF 100V 5\% | 1.0 EA | C054 |
| 5060232000 | CAP .01UF 100V 5\% | 6.0 EA | C081 C082 C083 C087 C088 C089 |
| 5080529000 | CAP . 01 UF 63VDCW | 1.0 EA | C045 |
| 5080559000 | CAP TRIMMER 3.5-38 PF | 1.0 EA | C114 |
| 5160453000 | CAP .1UF 100V 20\% X7R | 23.0 EA | C014 C019 C025 C028 C041 C042 C046 C047 |
|  |  |  | C048 C051 C052 C060 C061 C069 C073 C079 |
|  |  |  | C080 C084 C085 C090 C091 C092 C093 |
| 5160530000 | CAP .01UF 10\% 100V X7R | 29.0 EA | C008 C009 C010 C011 C012 C013 C015 C016 |
|  |  |  | C017 C018 C020 C024 C026 C027 C029 C058 |
|  |  |  | C059 C064 C065 C067 |
|  |  |  | C068 C070 C071 C072 C074 C107 C108 C109 |
|  |  |  | C110 |
| 5160725000 | CAP 1.OUF 50V 20\% | 1.0 EA | C075 |
| 5160736000 | CAP .001UF 10\% 100V X7R | 10.0 EA | C007 C094 C095 C096 C097 C098 C099 C100 |
|  |  |  | C105 C106 |
| 5160765000 | CAP 10PF 5\% 100V C0G | 4.0 EA | C043 C044 C057 C086 |
| 5160773000 | CAP 47PF 5\% 100V COG | 1.0 EA | C002 |
| 5160777000 | CAP 100PF 5\% 100V C0G | 3.0 EA | C021 C023 C053 |
| 5160778000 | CAP 120PF 5\% 100V C0G | 3.0 EA | C022 C111 C112 |
| 5160780000 | CAP 180PF 5\% 100V C0G | 2.0 EA | C005 |
|  |  |  | C113 |
| 5160782000 | CAP 270PF 5\% 100V C0G | 1.0 EA | C006 |
| 5160783000 | CAP 330PF 5\% 100V C0G | 1.0 EA | C003 |
| 5160786000 | CAP 560PF 5\% 100V C0G | 2.0 EA | C031 C034 |
| 5160862000 | CAP 680PF 5\% 100V C0G | 1.0 EA | C001 |
| 5200448000 | CAP, VAR .8-14PF | 1.0 EA | C076 |
| 5220548000 | CAP 10UF 50V 20\% | 5.0 EA | C030 C055 C056 C062 C063 |
| 5220549000 | CAP 22UF 35 V NON-POL | 2.0 EA | C032 C033 |
| 5220577000 | CAP 100UF 16V 20\% | 4.0 EA | C049 C050 C077 C078 |
| 5260358000 | CAP 22UF 35V 10\% | 1.0 EA | C004 |
| 5280036000 | DIODE VARACTOR KV3901 | 6.0 EA | CR001 CR002 CR003 CR004 CR005 CR006 |
| 5482400001 | RES 1 OHM 1/2W 1\% | 1.0 EA | R064 |
| 5482400101 | RES 10 OHM 1/2W 1\% | 1.0 EA | R005 |
| 5482400121 | RES 16.2 OHM 1/2W 1\% | 1.0 EA | R013 |
| 5482400139 | RES 24.9 OHM 1/2W 1\% | 3.0 EA | R122 R123 R124 |
| 5482400147 | RES 30.1 OHM 1/2W 1\% | 1.0 EA | R084 |
| 5482400158 | RES 39.2 OHM 1/2W 1\% | 1.0 EA | R109 |
| 5482400162 | RES 43.2 OHM 1/2W $1 \%$ | 1.0 EA | R081 |
| 5482400169 | RES 51.1 OHM 1/2W 1\% | 2.0 EA | R009 R121 |
| 5482400181 | RES 68.1 OHM 1/2W 1\% | 1.0 EA | R071 |
| 5482400185 | RES 75 OHM 1/2W 1\% | 4.0 EA | R016 R056 R059 R065 |
| 5482400193 | RES 90.9 OHM 1/2W 1\% | 4.0 EA | R015 R017 R070 R072 |
| 5482400201 | RES 100 OHM 1/2W 1\% | 3.0 EA | R007 R008 R088 |
| 5482400212 | RES 130 OHM 1/2W 1\% | 2.0 EA | R080 R082 |
| 5482400218 | RES 150 OHM 1/2W 1\% | 4.0 EA | R040 R041 R108 R120 |
| 5482400226 | RES 182 OHM 1/2W 1\% | 2.0 EA | R083 R085 |
| 5482400242 | RES 267 OHM 1/2W 1\% | 1.0 EA | R086 |
| 5482400247 | RES 301 OHM 1/2W 1\% | 3.0 EA | R012 R014 R042 |
| 5482400266 | RES 475 OHM 1/2W 1\% | 1.0 EA | R006 |
| 5482400301 | RES 1K OHM 1/2W 1\% | 12.0 EA | R001 R020 R021 R024 R057 R066 R069 R075 |
|  |  |  | R076 R078 R079 R095 |
| 5482400318 | RES 1.5K OHM 1/2W 1\% | 3.0 EA | R011 R093 R107 |
| 5482400321 | RES 1.62K OHM 1/2W 1\% | 1.0 EA | R003 |
| 5482400334 | RES 2.21 K OHM 1/2W 1\% | 1.0 EA | R002 |

5482400351 5482400358 5482400366 5482400369 5482400373 5482400386 5482400401

5482400442 5482400451 5482400469 5482400501 5482400547 5500970000 6040469000 6100900000 6100933000 6121184000 6200700000 8397900479 8434999355 9397900545 9434999176 9992559002

RES 3.32K OHM 1/2W 1\%
RES 3.92K OHM 1/2W $1 \%$
RES 4.75K OHM 1/2W 1\% RES 5.11 K OHM 1/2W 1\% RES 5.62K OHM $1 / 2 \mathrm{~W} 1 \%$ RES 7.68K OHM 1/2W $1 \%$ RES 10K OHM 1/2W 1\%

RES 26.7K OHM 1/2W 1\% RES 33.2K OHM 1/2W 1\% RES 51.1K OHM 1/2W 1\% RES 100K OHM 1/2W 1\% RES 301K OHM 1/2W 1\% POT 1K OHM 1/2W 10\% SW TGL SPDT HEADER 3 CKT STRAIGHT JUMPER, PWB TEST POINT SHUNT JUMPER 0.1" CENTERS *RECPT, MALE SMB,PC MOUNT SCH, AURAL CONVERTER PWB, AURAL CNVTR SHIELD PC BOARD COVER, PC BD HARDWARE LIST
2.0 EA
2.0 EA
3.0 EA
2.0 EA
3.0 EA
2.0 EA
21.0 EA
2.0 EA
4.0 EA R090 R091 R096 R097
1.0 EA R089
1.0 EA R077
2.0 EA R025 R026
4.0 EA R049 R058 R061 R067
1.0 EA S002
6.0 EA J005 J007 J008 J009 J010 J011
1.0 EA TP001
6.0 EA P005 P007 P008 P009 P010 P011
5.0 EA J001 J002 J003 J004 J006

Table 7-13. VSB/IF AGC BD - 9928324001

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS (d) |
| :---: | :---: | :---: | :---: |
| 3581881000 | EJECTOR KIT CARD | 1.0 EA |  |
| 3800114000 | *XSTR, NPN, 2N5109 ESD | 5.0 EA | Q003 Q005 Q006 Q101 Q102 |
| 3800152000 | XSTR, D40C5 ESD | 1.0 EA | Q004 |
| 3800189000 | XSTR, NPN 2N3904 ESD | 2.0 EA | Q001 Q002 |
| 3820428000 | IC, LM358 ESD | 1.0 EA | U101 |
| 3840321000 | *DIODE 5082-2800 ESD | 1.0 EA | CR011 |
| 3840355000 | DIODE HP5082-3081/A5S139 ESD | 1.0 EA | CR101 |
| 3840361000 | DIODE HP5082-3077/A5S377 ESD | 6.0 EA | CR001 CR002 CR003 CR004 CR005 CR006 |
| 3840431000 | RECT. 1N4001 ESD | 1.0 EA | CR007 |
| 3840720000 | TRANSZORB 1N6377 15V 5W ESD | 2.0 EA | CR009 CR010 |
| 3840838000 | TRANSZORB 1N6380 36V 5W ESD | 1.0 EA | CR008 |
| 4040198000 | SPACER TO-5, TO-9, TO-11 | 5.0 EA | XQ003 XQ005 |
|  |  |  | XQ006 XQ101 XQ102 |
| 4040513000 | HEAT SINK PA1-1CB | 1.0 EA | Q004 |
| 4040673000 | SOCKET 8 PIN DIP (DL) | 1.0 EA | XU101 |
| 4040725000 | HEAT SINK TO-5 CASE | 3.0 EA | Q003 Q005 Q006 |
| 4780392000 | XFMR, RF MODEL T4-1 | 3.0 EA | T001 T002 T101 |
| 4840336000 | SAW FILTER ESD | 1.0 EA | FL001 |
| 4940239000 | CHOKE WIDE BAND | 1.0 EA | L102 |
| 4940398000 | CHOKE RF 10.0UH +/-10\% | 2.0 EA | L001 L003 |
| 5000801000 | CAP, MICA, 2PF $500 \mathrm{~V}+/-.5 \mathrm{PF}$ | 1.0 EA | C026 |
| 5000826000 | CAP, MICA, 120PF 500V 5\% | 1.0 EA | C107 |
| 5000844000 | CAP, MICA, 1000PF 100V 5\% | 1.0 EA | C008 |
| 5160059000 | CAP, DISC .0015UF 1KV 10\% | 18.0 EA | C001 C002 C006 C007 C011-017 |
|  |  |  | C021 C022 C027 C028 C029 C030 C031 C101 C103 C106 C108 C114 |
| 5160067000 | CAP DISC .003UF 1KV 20\% | 4.0 EA | C005 C010 C012 C018 |
| Rev. P2: 05-31-00 | $8$ | 3-001 | $7-13$ |

5160074000 5160375000 5160453000 5160556000 5220548000 5260342000 5482400042 5482400085 5482400109 5482400118 5482400126 5482400169 5482400181 5482400185 5482400201 5482400234 5482400247 5482400258

5482400266 5482400269 5482400273 5482400285 5482400301 5482400318 5482400330 5482400401 5482400434 5482400466 5482400601 5500901000 5500942000 5580045000 5590047000 6040469000 6100679000 6100900000 6100933000 6120775000 6121184000 6200700000 8172100362

8397900491 8434999362 9992573002

CAP, DISC .005UF 1KV 20\%
CAP .01UF 50V -20/+80\% Z5U
CAP . 1 UF $100 \mathrm{~V} 20 \%$ X7R CAP .33UF 100 V 20\% CAP 10UF 50V 20\% CAP 2.7UF 35V 10\% RES 2.67 OHM 1/2W 1\% RES 7.5 OHM 1/2W 1\% RES 12.1 OHM 1/2W 1\% RES 15 OHM 1/2W 1\% RES 18.2 OHM 1/2W 1\% RES 51.1 OHM 1/2W 1\% RES 68.1 OHM 1/2W 1\% RES 75 OHM 1/2W 1\% RES 100 OHM 1/2W $1 \%$ RES 221 OHM 1/2W 1\% RES 301 OHM 1/2W 1\% RES 392 OHM 1/2W 1\%

RES 475 OHM 1/2W 1\% RES 511 OHM 1/2W 1\% RES 562 OHM 1/2W 1\% RES 750 OHM 1/2W 1\% RES 1K OHM 1/2W 1\% RES 1.5K OHM 1/2W 1\% RES 2K OHM 1/2W 1\% RES 10K OHM 1/2W 1\% RES 22.1K OHM 1/2W 1\% RES 47.5 K OHM 1/2W 1\% RES 1MEG OHM 1/2W $1 \%$ POT 500 OHM 1/2W 10\% POT 100K OHM 1/2 W 10\% HTR, SAW FILTER 5W 24VDC THERMISTOR 10K OHM SW TGL SPDT PLUG, SHORTING, .25" CTRS HEADER 3 CKT STRAIGHT JUMPER, PWB TEST POINT JACK, PC MT, . 040 PINS SHUNT JUMPER 0.1" CENTERS *RECPT, MALE SMB,PC MOUNT HEATER BLANKET

SCHEM, VSB/IF AGC
PWB, VSB/IF AGC
HARDWARE LIST, VSB IF AGC
1.0 EA C016
6.0 EA C019 C023 C024 C025 C102 C104
5.0 EA C003 C004 C013 C014 C112
1.0 EA C115
3.0 EA C040 C041 C042
3.0 EA C015 C105 C111
1.0EA R114
2.0 EA R006 R008
1.0 EA R013
1.0 EA R112
1.0 EA R031
3.0 EA R001 R021 R023
1.0 EA R032
1.0 EA R025
3.0 EA R026 R101 R107
3.0 EA R022 R024 R110
1.0 EA R109
2.0EA R104

R106
1.0 EA R105
2.0 EA R113R118
1.0 EA R017
2.0 EA R002 R018
3.0 EA R012R128 R132
7.0 EA R005 R009 R010 R011 R027 R028 R029
2.0 EA R020 R030
8.0 EA R003 R004 R015 R016 R102 R103 R108 R115
1.0 EA R019
1.0EA R120
1.0 EA R127
1.0 EA R007
1.0 EA R116
1.0EA HR001
1.0 EA RT001
1.0 EA S001
1.0 EA P002
1.0 EA J101
1.0 EA TP001
3.0 EA E001 E002 E003
1.0EA P101
3.0 EA J001 J002 J003
2.0 EA \#HR001 ONE

ON TOP ONE ON BOTTOM COVER WITH 055-0190-009 TO A MIN OF . 12 DEEP

Table 7-14. PWB, DIFF PHASE CORR. - 9928325001

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS $(m)$ |
| :--- | :--- | :--- | :--- |
| 3581881000 | EJECTOR KIT CARD | 1.0 EA |  |
| 3800086000 | XSTR, 2N4391 ESD | 2.0 EA | Q005 Q013 |
| 3800189000 | XSTR, NPN 2N3904 ESD | 1.0 EA | Q006 |
| 3800190000 | XSTR, PNP 2N3906 ESD | 5.0 EA | Q008 Q009 Q010 Q011 Q012 |
| 3800246000 | XSTR, 2N2219A ESD | 5.0 EA | Q001 Q002 Q003 Q007 Q015 |

3800558000 3820366000 3820371000 3820406000 3820440000 3820452000 3820947000 3840205000 3840321000 3840431000 3840659000 3840720000 4040198000 4040660000 4040673000 4040675000

4940398000 4940413000 5000817000 5000842000 5080412000 5080558000 5080559000 5160453000

5160736000 5220548000 5220550000

5400326000 5482400047 5482400166

5482400185
5482400201
5482400209
5482400230
5482400247
5482400266
5482400269
5482400273
5482400285
5482400301
5482400309
5482400318
5482400330
5482400342
5482400347
5482400354
5482400358
5482400366

| XSTR, 2N5566 ESD | 2.0 EA | Q004 Q014 |
| :---: | :---: | :---: |
| IC, MC14528BCP ESD | 1.0 EA | U006 |
| IC, MC7912CT ESD | 1.0 EA | U003 |
| IC, MC7812CT ESD | 1.0 EA | U002 |
| IC, 3083 ESD | 1.0 EA | U001 |
| IC, LM311/CA311 ESD | 1.0 EA | U005 |
| IC, SE5534 ESD | 1.0 EA | U004 |
| DIODE SILICON 1N914/4148 ESD | 6.0 EA | CR011 CR012 CR013 CR014 CR015 CR016 |
| *DIODE 5082-2800 ESD | 4.0 EA | CR017 CR018 CR019 CR020 |
| RECT. 1 N4001 ESD | 3.0 EA | CR006 CR009 CR010 |
| DIODE HP5082-2811/A2S811 ESD | 5.0 EA | CR001 CR002 CR003 CR004 CR005 |
| TRANSZORB 1N6377 15V 5W ESD | 2.0 EA | CR007 CR008 |
| SPACER TO-5, TO-9, TO-11 | 5.0 EA | \#Q001 \#Q002 \#Q003 \#Q007 \#Q015 |
| HEAT SINK | 2.0 EA | XQ004 XQ014 |
| SOCKET 8 PIN DIP (DL) | 2.0 EA | \#U004 \#U005 |
| SOCKET IC 16 CONT | 2.0 EA | \#U001 |
|  |  | \#U006 |
| CHOKE RF 10.0UH +/-10\% | 1.0 EA | L002 |
| CHOKE RF 330.0UH | 2.0 EA | L001 L003 |
| CAP, MICA, 47PF 500V 5\% | 2.0 EA | C027 C036 |
| CAP, MICA, 820PF 300V 5\% | 1.0 EA | C033 |
| CAP .047UF 200V 5\% | 2.0 EA | C014 C045 |
| CAP TRIMMER 5-60 PF | 1.0 EA | C001 |
| CAP TRIMMER 3.5-38 PF | 1.0 EA | C048 |
| CAP .1UF 100V 20\% X7R | 15.0 EA | C021 C022 C023 C024 C026 C028 C029 C031 |
|  |  | C032 C034 C035 C037 C040 C041 C042 |
| CAP .001UF 10\% 100V X7R | 2.0 EA | C015 C016 |
| CAP 10UF 50V 20\% | 4.0 EA | C025 C030 C038 C039 |
| CAP 100UF 25V 20\% | 19.0 EA | C002 C003 C004 C005 C006 C007 C008 C009 |
|  |  | C010 C011 C012 C013 C017 C018 C019 C043 |
|  |  | C044 C046 C047 |
| * RES 560 OHM 1W 5\% | 2.0 EA | R066 R110 |
| RES 3.01 OHM 1/2W 1\% | 2.0 EA | R053 R054 |
| RES 47.5 OHM 1/2W 1\% | 9.0 EA | R002 R011 R012 R034 R061 R064 R068 R087 R107 |
| RES 75 OHM 1/2W 1\% | 7.0 EA | R039 R040 R067 R073 R105 R106 R109 |
| RES 100 OHM 1/2W 1\% | 8.0 EA | R008 R009 R037 R041 R043 R099 R101 R103 |
| RES 121 OHM 1/2W 1\% | 2.0 EA | R065 R108 |
| RES 200 OHM 1/2W 1\% | 1.0 EA | R035 |
| RES 301 OHM 1/2W 1\% | 2.0 EA | R006 R007 |
| RES 475 OHM 1/2W 1\% | 2.0 EA | R038 R104 |
| RES 511 OHM 1/2W 1\% | 1.0 EA | R017 |
| RES 562 OHM 1/2W 1\% | 1.0 EA | R005 |
| RES 750 OHM 1/2W 1\% | 6.0 EA | R018 R019 R020 R052 R059 |
|  |  | R063 |
| RES 1K OHM 1/2W 1\% | 16.0 EA | R013 R014 R015 R016 R026 R027 R028 R029 |
|  |  | R031 R032 R036 R047 R049 R056 R058 R102 |
| RES 1.21K OHM 1/2W 1\% | 2.0 EA | R004 R033 |
| RES 1.5K OHM 1/2W $1 \%$ | 1.0 EA | R071 |
| RES 2K OHM 1/2W 1\% | 3.0 EA | R062 R069 R088 |
| RES 2.67K OHM 1/2W $1 \%$ | 1.0 EA | R077 |
| RES 3.01K OHM 1/2W 1\% | 1.0 EA | R072 |
| RES 3.57K OHM 1/2W 1\% | 1.0 EA | R083 |
| RES 3.92K OHM 1/2W 1\% | 1.0 EA | R080 |
| RES 4.75K OHM 1/2W 1\% | 8.0 EA | R024 |
|  |  | R025 R030 R050 R055 R079 R081 R086 |

5482400401

5482400418 5482400466 5482400530 5500628000 5500865000 5500899000 6040859000 6100900000 6100933000

6121184000 6200700000 8397900490 8434999363 9992562001

| RES 10K OHM 1/2W 1\% | 9.0 EA | R001 R003 R010 R042 R070 R074 R075 R076 |
| :---: | :---: | :---: |
|  |  | R100 |
| RES 15K OHM 1/2W $1 \%$ | 1.0 EA | R082 |
| RES 47.5K OHM 1/2W 1\% | 1.0 EA | R085 |
| RES 200K OHM 1/2W 1\% | 1.0 EA | R078 |
| POT 10K OHM .5W 10\% | 5.0 EA | R021 R022 R023 R051 R060 |
| POT 1K OHM 1/2W 10\% | 1.0 EA | R084 |
| POT 2 K OHM 1/2W | 5.0 EA | R044 R045 R046 R048 R057 |
| SW, TGL DPDT | 1.0 EA | S001 |
| HEADER 3 CKT STRAIGHT | 1.0 EA | J001 |
| JUMPER, PWB TEST POINT | 8.0 EA | TP001 TP002 TP003 TP004 TP005 TP006 TP007 TP008 |
| SHUNT JUMPER 0.1" CENTERS | 1.0 EA | P001 |
| *RECPT, MALE SMB,PC MOUNT | 1.0 EA | J002 |
| SCHEM DIFF PHASE CORR | 0.0 EA |  |
| PWB, DIFF PHASE | 1.0 EA |  |
| HARDWARE LIST | 1.0 EA |  |

Table 7-15. CMR FILTER MODULE - 9928326002

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS (a) |
| :--- | :--- | :--- | :--- |
| 6120200000 | RECEPTACLE 3 CONTACT | 1.0 EA | J008 |
| 8397900502 | SCHEMATIC, CMR FILTER | 0.0 EA |  |
| 8434999327 | COVER TOP FILTER ASSY | 1.0 EA |  |
| 8434999328 | COVER TOP DUAL SOUND ASSY | 1.0 EA |  |
| 9172100510 | PC ASSY FIL BOX | 1.0 EA |  |
| 9172100511 | PC ASSY FIL BOX W/TOROID | 1.0 EA |  |
| 9397900842 | CABLE, FILTER BOX | 1.0 EA |  |
| 9434999326 | COVER, BOTTOM FILTER ASSY | 1.0 EA |  |
| 9434999329 | COVER BOT DUAL SD ASSY | 1.0 EA |  |
| 9992648001 | HARDWARE LIST | 1.0 EA |  |

Table 7-16. PC ASSY FIL BOX - 9172100510

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS (e) |
| :--- | :--- | :--- | :--- |
| 3540309000 | TERM SOLDER | 3.0 EA |  |
| 3840799000 | DIODE, BIPOLAR ESD | 2.0 EA | CR002 CR005 |
| 5160736000 | CAP .O01UF 10\% 100V X7R | 4.0 EA | C002 C004 C006 C008 |
| 5160891000 | CAP 0.100UF 10\% 50V | 4.0 EA | C001 C003 C005 C007 |
| 6121268000 | RECEPTACLE RT ANG BNC | 4.0 EA | J004 J004A J005 J005A |
| 8434999354 | PWB, FILTER BD. | 1.0 EA |  |
| 9220900368 | DIVIDER SHLD FILTER | 2.0 EA |  |
| 9220900369 | TOROID ASSY DIV SHLD | 2.0 EA |  |

Table 7-17. PC ASSY FIL BOX W/TOROID - 9172100511

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS (e) |
| :--- | :--- | :--- | :--- |
| 3540309000 | TERM SOLDER | 3.0 EA |  |
| 3840799000 | DIODE, BIPOLAR ESD | 3.0 EA | CR003 CR008 CR011 |
| 5160736000 | CAP .O01UF 10\% 100V X7R | 5.0 EA | C002 C004 C006 C008 C010 |
| 5160891000 | CAP 0.100UF 10\% 50V | 5.0 EA | C001 C003 C005 C007 C009 |
| 6121268000 | RECEPTACLE RT ANG BNC | 4.0 EA | J004 J004A J005 J005A |
| 8434999354 | PWB, FILTER BD. | 1.0 EA |  |
| 9220900368 | DIVIDER SHLD FILTER | 2.0 EA |  |
| 9220900369 | TOROID ASSY DIV SHLD | 2.0 EA |  |

Table 7-18. POWER SUPPL.Y EXT - 9928327001

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS $(h)$ |
| :--- | :--- | :--- | :--- |
| 3540624000 | TERMINAL, MALE | 10.0 EA |  |
| 3582995000 | END PLATE, 261 TERM BD | 1.0 EA |  |
| 3583226000 | INSULATING COVER, PLASTIC | 5.0 EA |  |
| 3821031000 | IC, LM338K ESD | 3.0 EA | U001 U002 U004 |
| 3821049000 | IC, LT1033/LM333 ESD | 2.0 EA | U003 U005 |
| 4100391000 | INSULATOR TRANSISTOR T03 | 5.0 EA |  |
| 4140240000 | CORE BALUN | 10.0 EA | L001 L002 L003 L004 L005 L006 L007 L008 |
|  |  |  | L009 L010 |
| 4721665000 | TRANSFORMER, POWER TOROID | 1.0 EA |  |
| 4840379000 | RFI POWER LINE FILTER | 1.0 EA | FL001 |
| 5080561000 | EMI FILTER FEEDTHRU | 5.0 EA | FL002 FL003 FLO04 FL005 FL006 |
| 5600036000 | MOV 6500A 80J 150 VAC | 2.0 EA | RV001 RV002 |
| 6060834000 | CIRCUIT BREAKER 4A 250V | 1.0 EA | CB001 |
| 6120885000 | RECEPTACLE HOUSING | 1.0 EA | J011 |
| 6120978000 | HOUSING, RECPT 12 CKT | 1.0 EA |  |
| 6140786000 | TERM BD, 2C MODULAR 261 | 5.0 EA | \#TB001 |
| 6140787000 | TERM BD, 4C MODULAR 261 | 5.0 EA | \#TB001 |
| 8397900504 | SCHEM, POWER SUPPLY | 0.0 EA |  |
| 9220900181 | CABLE, EXC P.S. | 1.0 EA | W019 |
| 9397900487 | COVER PWR SUPPLY - TOP | 1.0 EA |  |
| 9434999335 | COVER PWR SUPPLY | 1.0 EA |  |
| 9435285200 | PWR SUPPLY EXCITER | 1.0 EA |  |
| 9435285201 | ANGLE, FILTER MTG | 1.0 EA |  |
| 9928021001 | PWB, POWER SUPPLY | 1.0 EA |  |
| 9992651001 | HARDWARE LIST | 1.0 EA |  |
| 9992652001 | WIRE/TUBING LIST | 1.0 EA |  |

## Table 7-19. PWB, POWER SUPPLY - 9928021001

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS ( $k$ ) |
| :---: | :---: | :---: | :---: |
| 3540336000 | TERMINAL, SOLDER | 10.0 EA | E001 E002 E003 E004 E005 E006 E007 E008 |
|  |  |  | E009 E010 |
| 3540688000 | TERM, SOCKET, 0.093" DIA | 12.0 EA |  |
| 3840597000 | RECT 1N4002 ESD | 10.0 EA | CR004 CR005 CR006 CR007 CR008 CR009 |
|  |  |  | CR010 CR011 CR012 CR013 |
| 3840702000 | RECT FW BRIDGE 600V 35A ESD | 3.0 EA | CR001 CR002 CR003 |
| 4040803000 | HEATSINK FOR BRIDGE | 3.0 EA | \#CR001 \#CR002 \#CR003 |
| 4040804000 | TRANSISTOR SOCKET | 5.0 EA | XU001 XU002 XU003 XU004 XU005 |
| 5160453000 | CAP .IUF 100V 20\% X7R | 5.0 EA | C021 C022 |
|  |  |  | C023 C024 C025 |
| 5220548000 | CAP 10UF 50V 20\% | 5.0 EA | C006 C007 C008 C009 C010 |
| 5220567000 | CAPACITOR 8200 MFD 16V | 2.0 EA | C004 C005 |
| 5220568000 | CAPACITOR 6800UF 50V 20\% | 3.0 EA | C001 C002 C003 |
| 5220569000 | CAP 100UF 50V 20\% | 5.0 EA | C016 C017 C018 C019 C020 |
| 5260318000 | CAP 10UF 35V 20\% | 5.0 EA | C011 C012 C013 C014 C015 |
| 5400336000 | *RES 1.5K OHM 1W 5\% | 2.0 EA | R025 R026 |
| 5400338000 | * RES 1.8K OHM 1W 5\% | 2.0 EA | R023 R024 |
| 5400345000 | * RES 3.6K OHM 1W 5\% | 2.0 EA | R021 R022 |
| 5482400219 | RES 154 OHM 1/2W 1\% | 5.0 EA | R001 R002 R003 R004 R005 |
| 5482400258 | RES 392 OHM 1/2W 1\% | 2.0 EA | R009 R010 |

5482400319 5482400339 5500625000 5500812000 6100833000 8434999069

RES 1.54 K OHM 1/2W 1\% RES 2.49K OHM 1/2W 1\% POT, 500 OHM .5W 10\% POT 100 OHM 1/2W 10\% HOUSING, PLUG 12 POS PWB, POWER SUPPLY
2.0 EA R007 R008
1.0 EA R006
3.0 EA R016 R017 R018
2.0 EA R019 R020
1.0 EA J001

Table 7-20. MODULE FINAL AMPL - 9928328001

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS (c) |
| :--- | :--- | :--- | :--- |
| 3040089000 | NUT, HEX 6-32 | 6.0 EA | \#USED AS SPACERS FOR PC BOARD TO |
|  |  |  | KEEP OFF OF HEATSINK |
| 3820734000 | *IC, CA2830C/MHW592 ESD | 2.0 EA | U001 U002 |
| 6200571000 | RECEP. BNC UG535-U | 2.0 EA | J001 J002 |
| 9397900499 | BRKT GND FINAL AMP | 2.0 EA |  |
| 9397900500 | SPACER CONN/GND BRKT | 2.0 EA |  |
| 9434999033 | HEATSINK, RF AMP | 1.0 EA |  |
| 9434999357 | COVER FINAL AMP | 1.0 EA |  |
| 9927093001 | PWB, FINAL AMP | 1.0 EA |  |
| 9992567001 | HARDWARE LIST | 1.0 EA |  |

Table 7-21. PWB, FINAL AMP - 9927093001

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS (p) |
| :---: | :---: | :---: | :---: |
| 3820411000 | 1C, PSC-2-1 ESD | 2.0 EA | HY001 HY002 |
| 3820594000 | *IC TL074ACN ESD | 1.0 EA | U004 |
| 3820746000 | IC, 79L05AC ESD | 1.0 EA | U006 |
| 3821126000 | IC 78L12A ESD | 1.0 EA | U005 |
| 3830189000 | IC, SA5205A ESD | 1.0 EA | U003 |
| 3840321000 | *DIODE 5082-2800 ESD | 2.0 EA | CR005 CR006 |
| 3840355000 | DIODE HP5082-3081/A5S139 ESD | 3.0 EA | CR002 CR003 CR004 |
| 3840720000 | TRANSZORB 1N6377 15V 5W ESD | 2.0 EA | CR007 CR008 |
| 3840838000 | TRANSZORB 1N6380 36V 5W ESD | 1.0 EA | CR009 |
| 3860081000 | ZENER 1N4729A ESD | 1.0 EA | CR001 |
| 4040673000 | SOCKET 8 PIN DIP (DL) | 1.0 EA | XU003 |
| 4040674000 | SOCKET 14 PIN DIP (D-L) | 1.0 EA | XU004 |
| 4040873000 | SOCKET ADAPTER SOIC8-DIP8 | 1.0 EA | \#U003 |
| 4940262000 | CHOKE RF 10UH 10\% | 1.0 EA | L003 |
| 4940390000 | CHOKE RF 3.30UH | 2.0 EA | L001 L002 |
| 4940398000 | CHOKE RF 10.0UH +/-10\% | 1.0 EA | L004 |
| 5160453000 | CAP .1UF 100V 20\% X7R | 15.0 EA | $\mathrm{C} 007 \mathrm{C008} \mathrm{C} 009 \mathrm{C012} \mathrm{C} 014 \mathrm{C} 015 \mathrm{C016} \mathrm{C} 017$ |
|  |  |  | C018 C019 C023 C026 C028 C029 C030 |
| 5160516000 | CAP 1UF 100V 20\% | 2.0 EA | C020 C021 |
| 5160530000 | CAP .01UF 10\% 100V X7R | 11.0 EA | C001 C002 C003 C004 C005 C006 C022 C024 |
|  |  |  | C025 C027 C031 |
| 5260097000 | CAP 47UF 35V 20\% | 2.0 EA | C011 C013 |
| 5260358000 | CAP 22UF 35V 10\% | 1.0 EA | C010 |
| 5482400169 | RES 51.1 OHM 1/2W 1\% | 2.0 EA | R014 R015 |
| 5482400201 | RES 100 OHM 1/2W 1\% | 1.0 EA | R017 |
| 5482400230 | RES 200 OHM 1/2W 1\% | 1.0 EA | R016 |
| 5482400301 | RES 1K OHM 1/2W 1\% | 3.0 EA | R004 R006 R007 |
| 5482400330 | RES 2K OHM 1/2W 1\% | 1.0 EA | R002 |
| 5482400385 | RES 7.5K OHM 1/2W 1\% | 1.0 EA | R001 |
| 5482400401 | RES 10K OHM 1/2W 1\% | 1.0 EA | R005 |
| 5482400442 | RES 26.7K OHM 1/2W 1\% | 1.0 EA | R003 |

5482400469 5482400701 6100679000 6100978000 6120904000 6202518000 8397900023 8434999031

RES 51.1K OHM 1/2W 1\% 4.0 EA
RES 10MEG OHM 1/2W $1 \%$ PLUG, SHORTING, .25" CTRS HDR 10C 2ROW RT ANG JACK, PC MT GOLD PLATED DIR COUPLER, .5-500 MHZ SCHEM, FINAL AMP PWB, FINAL AMP
2.0 EA
1.0 EA
1.0 EA
3.0 EA
1.0 EA
0.0 EA
1.0 EA

R008 R009 R010 R011
R012 R013
P001
J003
\#3 PINS USED WITH P001
DC001

Table 7-22. PWB, EXTENDER CARD - 9928329001

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS (c) |
| :--- | :--- | :--- | :--- |
| 3581881000 | EJECTOR KIT CARD | 1.0 EA |  |
| 3582612000 | BLOCK, MOUNTING | 1.0 EA |  |
| 3840661000 | LED, GRN, T 1-3/4, RT ANG ESD | 5.0 EA | DS001 DS002 DSO03 DSO004 DS005 |
| 5401600210 | RES 240 OHM 3W 5\% | 2.0 EA | R004 R005 |
| 5401600222 | RES 750 OHM 3W 5\% | 2.0 EA | R002 R003 |
| 5401600303 | RES 1.2K OHM 3W 5\% | 1.0 EA | R001 |
| 6100933000 | JUMPER, PWB TEST POINT | 1.0 EA | TP001 |
| 6121225000 | CONN, PC EDGE 28 POS DUAL | 1.0 EA | J001 |
| 8397900172 | SCHEM, EXCITER EXTENDER | 0.0 EA |  |
| 8434999364 | PWB, EXTENDER CARD | 1.0 EA |  |

## Table 7-23. PWB, SYNTHESIZER BD \#1-992 8347001

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS (p) |
| :--- | :--- | :--- | :--- |
| 3581881000 | EJECTOR KIT CARD | 1.0 EA |  |
| 3581928000 | JUMPER 1/4 LG 1/8H | 11.0 EA | JP001 JP002 JP003 JP004 JP005 JP006 |
|  |  |  | JP007 JP008 JP009 JP010 JP012 |
| 3800116000 | XSTR, 2N3866 ESD | 3.0 EA | Q001 Q002 Q003 |
| 3800189000 | XSTR, NPN 2N3904 ESD | 3.0 EA | Q004 Q005 Q007 |
| 3800190000 | XSTR, PNP 2N3906 ESD | 1.0 EA | Q006 |
| 3820184000 | IC, 340T-5/7805 +5V REG ESD | 1.0 EA | U016 |
| 3820521000 | IC, 339 ESD | 1.0 EA | U003 |
| 3820605000 | IC 7905C ESD | 1.0 EA | U012 |
| 3820690000 | IC 10131 ESD | 1.0 EA | U006 |
| 3820692000 | IC 10136 ESD | 2.0 EA | U007 U010 |
| 3820749000 | IC NE5532A ESD | 1.0 EA | U011 |
| 3820868000 | IC MC145151P2 ESD | 1.0 EA | U002 |
| 3821217000 | IC 1036 ESD | 1.0 EA | U001 |
| 3821221000 | IC 10216 ESD | 4.0 EA | U004 U005 U008 U009 |
| 3821228000 | IC NE 602 ESD | 1.0 EA | U014 |
| 3821230000 | IC NE 592 ESD | 2.0 EA | U013 U015 |
| 3840205000 | DIODE SILICON 1N914/4148 ESD | 9.0 EA | CR003 CR005 CR006 CR007 CR008 CR010 |
|  |  |  | CR011 CR012 CR015 |
| 3840661000 | LED, GRN, T 1-3/4, RT ANG ESD | 1.0 EA | DS001 |
| 4040198000 | SPACER TO-5, TO-9, TO-11 | 3.0 EA | Q001 Q002 Q003 |
| 4442958000 | XTAL 8 MHZ | 1.0 EA | Y002 |
| 4442959000 | XTAL 10 MHZ | 1.0 EA | Y001 |
| 4442960000 | XTAL 16 MHZ | 1.0 EA | Y003 |
| 4780392000 | XFMR, RF MODEL T4-1 | 1.0 EA | T001 |
| 4920777000 | IND, VAR 2.2UH NOM | 1.0 EA | L004 |
| 4920778000 | IND VAR .288UH NOM | 1.0 EA | L007 |
| 4920779000 | IND VAR .33UH NOM | 3.0 EA | L017 L018 L019 |
| 4920780000 | IND VAR 1.23UH NOM | 1.0 EA | L001 |

4940379000 4940392000 4940398000 4940399000 4940402000 4940403000 4940465000 4940468000 4940469000 4940470000 5001253000 5001268000 5001271000 5001281000 5001285000 5001287000 5001289000 5001292000 5060230000 5060234000 5060236000 5060239000 5060254000 5060263000 5160417000 5160530000 5160767000 5160768000 5160769000 5160770000 5160773000 5160782000 5160831000

5160891000

5160906000 5160907000 5160910000 5180057000 5260050000 5260311000 5260358000 5280037000 5482400142 5482400151 5482400166 5482400169 5482400173 5482400189 5482400201 5482400209 5482400230

CHOKE RF 0.39 UH CHOKE RF 4.70 UH CHOKE RF $10.0 \mathrm{UH}+/-10 \%$ CHOKE RF 12.0 UH CHOKE RF 22.0UH CHOKE RF 27.0UH IND, 2.7UH 5\% IND 1,200 UH 10\% IND 1,500 UH 10\% IND 8,200 UH 10\% CAP 5PF $100 \mathrm{~V}+/-.5 \mathrm{PF}$ CAP 33PF 500V 5\% CAP 43PF $100 \mathrm{~V} 5 \%$ CAP 100PF 300V 5\% CAP 150PF 500V 5\% CAP 180PF 500V 5\% CAP 220PF 300V 5\% CAP 300PF 300V 5\% CAP .001UF 100VAC 5\% CAP .0022UF 100V 5\% CAP .0047UF 100/63V 5\% CAP .022UF $100 \mathrm{~V} 5 \%$ CAP .0082UF 100V 5\% CAP .0039UF 100V 5\% CAP 1000PF 10\% 200V CAP .01UF 10\% 100V X7R CAP 15PF 5\% 100V C0G CAP 18PF 5\% 100V C0G CAP 22PF 5\% 100V C0G CAP 27PF 5\% 100V C0G CAP 47PF 5\% 100V C0G CAP 270PF 5\% 100V C0G CAP 0.010UF 10\% 100V

CAP 0.100UF 10\% 50V

CAP 33PF 10\% 200V CAP 0.330UF $10 \% 50 \mathrm{~V}$ CAP 820PF 10\% 200V CAP, VAR 9-35PF CAP 1UF 35V 20\% CAP 2.2UF 35V 10\% CAP 22UF 35V 10\% DIODE, VARACTOR BB505 RES 26.7 OHM 1/2W 1\% RES 33.2 OHM 1/2W 1\% RES 47.5 OHM 1/2W 1\% RES 51.1 OHM 1/2W 1\% RES 56.2 OHM 1/2W 1\% RES 82.5 OHM 1/2W 1\% RES 100 OHM 1/2W 1\% RES 121 OHM 1/2W 1\%

RES 200 OHM 1/2W 1\%

| 1.0 EA | L015 |
| :--- | :--- |
| 1.0 EA | L016 |
| 2.0 EA | L012 L013 |
| 2.0 EA | L006 L008 |
| 3.0 EA | L002 L003 L014 |
| 1.0 EA | L020 |
| 1.0 EA | L005 |
| 1.0 EA | L010 |
| 1.0 EA | L009 |
| 1.0 EA | L011 |
| 2.0 EA | C134 C140 |
| 1.0 EA | C028 |
| 2.0 EA | C110 C112 |
| 2.0 EA | C019 C107 |
| 1.0 EA | C020 |
| 1.0 EA | C026 |
| 1.0 EA | C014 |
| 1.0 EA | C126 |
| 3.0 EA | C113 C114 C122 |
| 1.0 EA | C124 |
| 1.0 EA | C121 |
| 2.0 EA | C116 C117 |
| 1.0 EA | C123 |
| 1.0 EA | C125 |
| 3.0 EA | C013 C103 C132 |
| 3.0 EA | C034 C039 C040 |
| 1.0 EA | C033 |
| 2.0 EA | C133 C136 |
| 1.0 EA | C137 |
| 2.0 EA | C135 C138 |
| 1.0 EA | C139 |
| 1.0 EA | C035 |
| 17.0 EA | C003 C005 C007 C012 C015 C016 C036 C052 |
| C053 |  |
| C0 |  |

5482400234
5482400247
5482400251
5482400266
5482400268
5482400273
5482400281

5482400289
5482400301
5482400309
5482400318
5482400326
5482400330
5482400334
5482400342
5482400351
5482400366
5482400381
5482400401
5482400418
5482400426
5482400430 5482400466 5482400468 5482400481 5482400501 5501074000 6200700000 7001271000 8172199001 8397900528 8434999375 9397900540 9992664001

RES 221 OHM 1/2W 1\% RES 301 OHM 1/2W $1 \%$ RES 332 OHM 1/2W 1\% RES 475 OHM 1/2W 1\% RES 499 OHM 1/2W $1 \%$ RES 562 OHM 1/2W 1\% RES 681 OHM 1/2W 1\%

RES 825 OHM 1/2W 1\% RES 1 K OHM $1 / 2 W 1 \%$ RES 1.21 K OHM $1 / 2 \mathrm{~W} 1 \%$ RES 1.5 K OHM $1 / 2 \mathrm{~W} 1 \%$ RES 1.82K OHM 1/2W $1 \%$ RES 2K OHM 1/2W $1 \%$ RES $2.21 \mathrm{~K} \mathrm{OHM} 1 / 2 \mathrm{~W} 1 \%$ RES 2.67K OHM 1/2W 1\% RES 3.32K OHM $1 / 2 \mathrm{~W} 1 \%$ RES 4.75K OHM 1/2W $1 \%$ RES 6.81 K OHM $1 / 2 \mathrm{~W} 1 \%$ RES 10K OHM 1/2W 1\% RES 15K OHM 1/2W 1\% RES 18.2K OHM 1/2W 1\% RES 20K OHM 1/2W 1\% RES 47.5K OHM 1/2W 1\% RES 49.9 K OHM $1 / 2 \mathrm{~W} 1 \%$ RES 68.1K OHM $1 / 2 W 1 \%$ RES 100K OHM 1/2W 1\% POT 20K OHM .75W 10\% *RECPT, MALE SMB,PC MOUNT OCXO 10 MHZ
SPEC, TEST PROCEDURE
SCHEM, FREQ SYNTH CARD \#1
PWB, SYNTHESIZER BD \#1 SHIELD PC BOARD
HARDWARE LIST

| 4.0 EA | R131 R132 R136 R137 |
| :--- | :--- |
| 1.0 EA | R126 |
| 1.0 EA | R054 |
| 8.0 EA | R019 R036 R105 R106 R109 R120 R121 R129 |
| 2.0 EA | R115 R116 |
| 2.0 EA | R032 R033 |
| 15.0 EA | R015 R037 R038 R042 R044 R048 R049 R052 |
|  | R056 R058 R059 R060 R064 R065 R066 |
| 1.0 EA | R055 |
| 5.0 EA | R018 R045 R046 R057 R130 |
| 1.0 EA | R128 |
| 1.0 EA | R027 |
| 1.0 EA | R107 |
| 5.0 EA | R003 R004 R112 R113 R119 |
| 1.0 EA | R022 |
| 1.0 EA | R118 |
| 2.0 EA | R021 R026 |
| 3.0 EA | R029 R111 R114 |
| 1.0 EA | R020 |
| 7.0 EA | R008 R009 R010 R014 R028 R123 R124 |
| 2.0 EA | R005 R127 |
| 4.0 EA | R053 R067 R102 R125 |
| 1.0 EA | R122 |
| 1.0 EA | R117 |
| 1.0 EA | R006 |
| 1.0 EA | R016 |
| 1.0 EA | R013 |
| 1.0 EA | R001 |
| 6.0 EA | J001 J002 J003 J004 J005 J006 |
| 1.0 EA | Y004 |
| 1.0 EA |  |
| 1.0 EA |  |
| 1.0 EA |  |
| 1.0 EA |  |
| 1.0 EA |  |

Table 7-24. PWB, SYNTHESIZER BD \#2-992 8348001

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS (I) |
| :--- | :--- | :--- | :--- |
| 3581881000 | EJECTOR KIT CARD | 1.0 EA |  |
| 3581928000 | JUMPER 1/4 LG 1/8H | 26.0 EA |  |
| 3820411000 | IC, PSC-2-1 ESD | 1.0 EA | HY001 |
| 3820648000 | IC, LM339A ESD | 1.0 EA | U001 |
| 3820690000 | IC 10131 ESD | 1.0 EA | U004 |
| 3820907000 | IC MC145152P2 ESD | 1.0 EA | U006 |
| 3821126000 | IC 78L12A ESD | 1.0 EA | U003 |
| 3821218000 | IC 1007 ESD | 1.0 EA | U002 |
| 3821219000 | IC 1028 ESD | 1.0 EA | U025 |
| 3821220000 | IC 10E016 ESD | 1.0 EA | U027 |
| 3821221000 | IC 10216 ESD | 1.0 EA | U026 |
| 3821222000 | IC 12090 ESD | 2.0 EA | U028 U035 |
| 3821223000 | IC 12013 ESD | 1.0 EA | U007 |
| 3821224000 | IC 12040 ESD | 1.0 EA | U024 |
| 3821225000 | IC, ASK-1 ESD | 2.0 EA | U016 U017 |
| 3821226000 | IC MSC-2-1W ESD | 2.0 EA | U018 U032 |
| 3821227000 | IC 12009 ESD | 1.0 EA | U008 |

3821229000 3821231000 3821232000 3821233000 3821234000 3821235000 3821237000 3830189000 3840205000 3840659000 3840725000 3860078000 3860163000 4040198000 4040873000 4780392000 4840392000 4920781000 4920782000 4920783000 4920784000 4940238000 4940390000 4940398000 4940418000 4940446000 4940467000 5001293000 5001295000 5001300000 5060231000 5060234000 5060235000 5060237000 5060253000 5060263000 5160417000

5160827000 5160831000

5160833000 5160834000 5160891000

5160905000 5160906000 5160909000 5220548000 5220550000 5260308000 5260311000 5260316000 5260358000

IC 10198 ESD
IC MWA-130 ESD
IC MWA-230 ESD
IC JH-139 ESD
IC V105L001 ESD
IC M2009706 ESD
IC JH-113 ESD
IC, SA5205A ESD
DIODE SILICON 1N914/4148 ESD
DIODE HP5082-2811/A2S811 ESD
RECT 1N5818 ESD
ZENER, 1N4734A 5.6V ESD
ZENER, 1N4735A 6.2V ESD
SPACER TO-5, TO-9, TO-11
SOCKET ADAPTER SOIC8-DIP8
XFMR, RF MODEL T4-1
FILTER, LOW PASS 21.4MHZ
IND VAR 1000UH NOM
IND VAR 3900UH NOM
IND VAR 2.2MH NOM
IND VAR 1.5MH NOM
CHOKE RF 39UH
CHOKE RF 3.30UH
CHOKE RF $10.0 \mathrm{UH}+/-10 \%$
CHOKE RF 820.0UH
CHOKE POWER LINE 100UH
ND 8.2UH 10\%
CAP 330PF 100V 5\%
CAP 390PF 100V 5\%
CAP 620PF 100V 5\%
CAP .0015UF 63V 5\%
CAP .0022UF 100V 5\%
CAP .0033UF $100 \mathrm{~V} 5 \%$
CAP .0068UF $100 \mathrm{~V} 5 \%$
CAP .0056UF $100 \mathrm{~V} 5 \%$
CAP .0039UF $100 \mathrm{~V} 5 \%$
CAP 1000PF 10\% 200V

CAP 4700PF 10\% 100V CAP 0.010UF 10\% 100V

CAP .022UF 10\% 50V CAP 0.047UF 10\% 50V CAP 0.100UF 10\% 50V

CAP 22PF 10\% 200V
CAP 33PF $10 \% 200 \mathrm{~V}$
CAP 100PF $10 \% 200 \mathrm{~V}$
CAP 10UF $50 \mathrm{~V} 20 \%$
CAP 100UF 25V 20\%
CAP 22UF 10 V 20\%
CAP 2.2UF 35V 10\%
CAP .47UF 35V 20\%
CAP 22UF 35V 10\%

| 1.0 EA | U029 |
| :---: | :---: |
| 1.0 EA | U022 |
| 2.0 EA | U033 U036 |
| 1.0 EA | HY003 |
| 1.0 EA | U005 |
| 1.0 EA | U030 |
| 1.0 EA | HY002 |
| 3.0 EA | U009 U010 U020 |
| 3.0 EA | CR003 CR005 CR006 |
| 2.0 EA | CR001 CR002 |
| 1.0 EA | CR009 |
| 1.0 EA | CR007 |
| 1.0 EA | CR004 |
| 3.0 EA | XU022 XU033 XU036 |
| 3.0 EA | \#U009 \#U010 \#U020 |
| 1.0 EA | T001 |
| 1.0 EA | U014 |
| 1.0 EA | L007 |
| 2.0 EA | L005 L012 |
| 1.0 EA | L003 |
| 1.0 EA | L002 |
| 1.0 EA | L004 |
| 2.0 EA | L008 L009 |
| 1.0 EA | L010 |
| 1.0 EA | L006 |
| 1.0 EA | L011 |
| 1.0 EA | L001 |
| 1.0 EA | C056 |
| 1.0 EA | C089 |
| 3.0 EA | C034 C054 C057 |
| 2.0 EA | C036 C058 |
| 1.0 EA | C033 |
| 2.0 EA | C053 C055 |
| 2.0 EA | C035 C037 |
| 2.0 EA | C010 C011 |
| 1.0 EA | C090 |
| 10.0 EA | C007 C008 C045 C048 C066 C072 |
|  | C074 C075 C077 C078 |
| 1.0 EA | C040 |
| 12.0 EA | C001 C006 C017 C018 C020 C025 C026 C032 |
|  | C039 C047 C065 C079 |
| 2.0 EA | C044 C046 |
| 2.0 EA | C043 C051 |
| 29.0 EA | C002 C003 C004 C005 C009 C012 C013 C019 |
|  | C021 C022 C023 C024 C038 C041 C049 |
|  | C052 C061 C062 C063 C064 C067 C073 C076 |
|  | C080 C081 C082 C085 C086 C087 |
| 1.0 EA | C068 |
| 1.0 EA | C030 |
| 1.0 EA | C059 |
| 3.0 EA | C014 C042 C050 |
| 4.0 EA | C016 C027 C070 C088 |
| 2.0 EA | C083 C084 |
| 1.0 EA | C015 |
| 1.0 EA | C060 |
| 1.0 EA | C071 |

5482400001
5482400101
5482400168
5482400173
5482400185
5482400201
5482400230
5482400242
5482400251
5482400258
5482400268
5482400281
5482400301
5482400347
5482400351
5482400368
5482400373
5482400389 5482400418 5482400426 5482400434 5482400451 5482400501 5500935000 5560111000 5560112000 6200700000 8172200001 8397900529 8434999376 9392859024 9397900540 9992663001

RES 1 OHM 1/2W 1\%
RES 10 OHM 1/2W 1\%
RES 49.9 OHM $1 / 2 \mathrm{~W} 1 \%$
RES 56.2 OHM 1/2W 1\%
RES 75 OHM 1/2W 1\%
RES 100 OHM 1/2W 1\%
RES 200 OHM 1/2W 1\%
RES 267 OHM 1/2W 1\%
RES 332 OHM 1/2W 1\%
RES 392 OHM 1/2W 1\%
RES 499 OHM 1/2W 1\%
RES 681 OHM 1/2W 1\%
RES 1 K OHM $1 / 2 \mathrm{~W} 1 \%$
RES 3.01K OHM 1/2W 1\%
RES 3.32K OHM 1/2W 1\%
RES 4.99K OHM $1 / 2 \mathrm{~W} 1 \%$
RES 5.62K OHM 1/2W $1 \%$
RES 8.25K OHM 1/2W $1 \%$
RES 15K OHM 1/2W 1\%
RES 18.2K OHM 1/2W 1\%
RES 22.1K OHM 1/2W 1\%
RES 33.2K OHM 1/2W 1\%
RES 100K OHM 1/2W 1\%
POT 2 K OHM 1/2W 10\%
ATTEN 6DB 50 OHM ATTEN 10DB 50 OHM
*RECPT, MALE SMB,PC MOUNT SPEC, TEST PROCEDURE
SCHEM, SYNTHESIZER BD \#2
PWB, SYNTHESIZER BD \#2
COAX CABLE, 50 OHM
SHIELD PC BOARD
HARDWARE LIST, PWB,SYNTHESIZER

| 4.0 EA | R024 R025 R026 R057 |
| :--- | :--- |
| 1.0 EA | R056 |
| 7.0 EA | R022 R023 R048 R051 R055 R058 R059 |
| 2.0 EA | R005 R016 |
| 4.0 EA | R034 R035 R036 R037 |
| 5.0 EA | R014 R020 R021 R045 R046 |
| 1.0 EA | R030 |
| 2.0 EA | R018 R019 |
| 2.0 EA | R054 |
|  | R065 |
| 8.0 EA | R028 R029 R052 R053 R060 R061 R062 R063 |
| 2.0 EA | R027 R042 |
| 2.0 EA | R006 R047 |
| 7.0 EA | R007 R008 R009 R010 R017 R033 R040 |
| 1.0 EA | R043 |
| 2.0 EA | R001 R049 |
| 1.0 EA | R015 |
| 1.0 EA | R067 |
| 1.0 EA | R041 |
| 2.0 EA | R011 R012 |
| 1.0 EA | R068 |
| 2.0 EA | R031 R032 |
| 1.0 EA | R004 |
| 2.0 EA | R002 R003 |
| 2.0 EA | R013 R044 |
| 4.0 EA | U012 U013 U023 U031 |
| 1.0 EA | U019 |
| 5.0 EA | J001 J002 J003 J004 J005 |
| 0.0 EA |  |
| 0.0 EA |  |
| 1.0 EA |  |
| 1.0 EA |  |
| 1.0 EA |  |
| 1.0 EA |  |

Table 7-25. *PWA, VIDEO BOARD W/VIDEO - 9929564001

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS (m) |
| :--- | :--- | :--- | :--- |
| 3581881000 | EJECTOR KIT CARD | 1.0 EA |  |
| 3800189000 | XSTR, NPN 2N3904 ESD | 11.0 EA | Q001 Q002 Q003 Q004 Q005 Q006 Q007 |
|  |  |  | Q008 Q009 Q010 Q016 |
| 3800190000 | XSTR, PNP 2N3906 ESD | 2.0 EA | Q011 Q012 |
| 3800573000 | XSTR, J309 ESD | 1.0 EA | Q014 |
| 3800578000 | XSTR, PN4258 ESD | 2.0 EA | Q013 Q015 |
| 3821379000 | IC CLC522 VGA ESD | 1.0 EA | U016 |
| 3821568000 | IC LM1881N ESD | 1.0 EA | U011 |
| 3821580000 | IC LT1252 VIDEO OPAMP ESD | 9.0 EA | U001 U002 U003 U006 U008 U010 U012 U014 |
|  |  |  | U015 |
| 3821584000 | IC AD8037AN ESD | 1.0 EA | U004 |
| 3821598000 | IC 74AC00 ESD | 1.0 EA | U007 |
| 3821620000 | IC 9631 OPAMP ESD | 1.0 EA | U005 |
| 3821664000 | IC, OP AMP, TL054 ESD | 1.0 EA | U013 |
| 3830384000 | IC, 567D ESD | 1.0 EA | U017 |
| 3840205000 | DIODE SILICON 1N914/4148 ESD | 8.0 EA | CR011 CR012 CR013 CR014 CR015 CR016 |
|  |  |  | CR017 CR018 |
| 3840431000 | RECT. 1N4001 ESD | 2.0 EA | CR009 CR010 |

3840659000

3840719000 3840780000 4040768000 4040873000 4840439000 4840445000 4920857000 4940394000 4940397000 4940398000 4940419000 5060232000 5060239000 5160453000

5160530000 5160765000 5160766000 5160769000 5160773000 5160777000 5160881000 5160971000 5160974000 5220548000

5220550000 5220570000 5220578000 5220588000 5260096000 5260108000

5482400130 5482400168 5482400185 5482400187 5482400201 5482400209 5482400213 5482400215
5482400218
5482400222
5482400226
5482400228
5482400230
5482400231
5482400234
5482400242
5482400247

DIODE HP5082-2811/A2S811 ESD
TRANSZORB 1N6373 5 V 5 W ESD
LED, RED ESD
SOCKET 24 PIN DIP (DL)
SOCKET ADAPTER SOIC8-DIP8
LINE, DELAY 200NS
LINE, DELAY 400 NS
INDUCTOR, FIXED RF 197NH
CHOKE 6.80UH
CHOKE RF 8.20 UH
CHOKE RF $10.0 \mathrm{UH}+/-10 \%$
IND $1000 \mathrm{HH} 10 \%$
CAP .01UF $100 \mathrm{~V} 5 \%$
CAP .022UF $100 \mathrm{~V} 5 \%$
CAP .1UF $100 \mathrm{~V} 20 \%$ X7R

CAP .01UF 10\% 100V X7R
CAP 10PF 5\% 100 V C0G
CAP 12PF 5\% 100V C0G CAP 22PF 5\% 100V C0G CAP 47PF 5\% 100V C0G CAP 100PF 5\% 100V C0G CAP 820PF 5\% 100V C0G CAP 470PF 5\% 100V C0G CAP 1000PF 5\% 100V C0G CAP 10UF 50V 20\%

CAP 100UF 25 V 20\%
CAP 2.2UF 50V 20\%
CAP 1.OUF 50V 20\%
CAP 100UF 25 V 20\% NP
CAP 100UF 10V 20\% CAP 4.7UF 35V 20\%

RES 20 OHM 1/2W 1\%
RES 49.9 OHM 1/2W $1 \%$
RES 75 OHM 1/2W $1 \%$
RES 78.7 OHM 1/2W $1 \%$
RES 100 OHM 1/2W 1\%
RES 121 OHM 1/2W 1\%
RES 133 OHM 1/2W 1\%
RES 140 OHM 1/2W 1\%
RES 150 OHM 1/2W 1\%
RES 165 OHM 1/2W 1\%
RES 182 OHM 1/2W 1\%
RES 191 OHM 1/2W 1\%
RES 200 OHM 1/2W 1\%
RES 205 OHM 1/2W 1\%
RES 221 OHM 1/2W 1\%
RES 267 OHM 1/2W 1\%
RES 301 OHM 1/2W 1\%

| 8.0 EA | CR001 CR002 CR003 CR004 CR005 CR006 |
| :---: | :---: |
|  | CR007 CR008 |
| 2.0 EA | CR019 CR020 |
| 1.0 EA | DS001 |
| 1.0 EA | XDL001 |
| 1.0 EA | \#U017 |
| 1.0 EA | DL002 |
| 1.0 EA | DL001 |
| 1.0 EA | L009 |
| 2.0 EA | L006 L007 |
| 1.0 EA | L001 |
| 1.0 EA | L002 |
| 2.0 EA | L003 L008 |
| 1.0 EA | C074 |
| 2.0 EA | C052 C060 |
| 21.0 EA | C001 C003 C004 C005 C008 C011 C012 C033 |
|  | C043 C048 C054 C056 |
|  | C061 C068 C069 C071 C072 C076 C077 C080 |
|  | C081 |
| 3.0 EA | C028 C036 C073 |
| 1.0 EA | C070 |
| 2.0 EA | C020 C035 |
| 1.0 EA | C042 |
| 1.0 EA | C051 |
| 4.0 EA | C038 C039 C045 C046 |
| 1.0 EA | C015 |
| 1.0 EA | C079 |
| 2.0 EA | C016 C029 |
| 2.0 EA | C055 |
|  | C075 |
| 1.0 EA | C 027 |
| 1.0 EA | C067 |
| 2.0 EA | C050 C053 |
| 1.0 EA | C037 |
| 5.0 EA | C002 C006 C017 C018 C078 |
| 24.0 EA | C007 C009 C010 C013 C014 C019 C022 C023 |
|  | C024 C030 C032 C034 C040 C041 C047 C049 |
|  | C057 C058 C059 C062 C063 C064 C065 |
|  | C066 |
| 1.0 EA | R150 |
| 3.0 EA | R069 R093 R112 |
| 3.0 EA | R065 R086 R151 |
| 1.0 EA | R080 |
| 8.0 EA | R038 R039 R040 R041 R042 R043 R044 R045 |
| 1.0 EA | R142 |
| 2.0 EA | R052 R053 |
| 1.0 EA | R084 |
| 4.0 EA | R054 R055 R098 R155 |
| 1.0 EA | R087 |
| 1.0 EA | R135 |
| 3.0 EA | R050 R051 R091 |
| 4.0 EA | R048 R049 R108 R156 |
| 1.0 EA | R119 |
| 3.0 EA | R027 R090 R097 |
| 1.0 EA | R072 |
| 1.0 EA | R109 |

5482400251
5482400262
5482400266
5482400268

5482400273
5482400285
5482400290
5482400301

5482400313
5482400323
5482400330
5482400334
5482400343
5482400351
5482400366
5482400373
5482400401

5482400451
5482400573
5482400581
5482400601 5500398000
5500901000
5500913000
5500921000
5500922000
5500923000
5500928000
5501101000
5501102000
6041192000 6100679000 6100900000 6100933000

6120775000 6121184000 6200700000 8435285411 8435285413

RES 332 OHM 1/2W 1\% RES 432 OHM 1/2W $1 \%$ RES 475 OHM 1/2W $1 \%$ RES 499 OHM $1 / 2 W 1 \%$

RES 562 OHM 1/2W 1\% RES 750 OHM 1/2W 1\% RES 845 OHM 1/2W 1\%

RES $1 \mathrm{~K} \mathrm{OHM} 1 / 2 \mathrm{~W} 1 \%$

RES 1.33K OHM 1/2W 1\% RES 1.69 K OHM $1 / 2 \mathrm{~W} 1 \%$ RES 2K OHM 1/2W 1\% RES 2.21 K OHM $1 / 2 \mathrm{~W} 1 \%$ RES 2.74 K OHM 1/2W 1\% RES 3.32K OHM 1/2W 1\% RES 4.75K OHM 1/2W 1\% RES 5.62K OHM 1/2W 1\% RES 10K OHM 1/2W 1\%

RES 33.2K OHM 1/2W 1\%
RES 562K OHM 1/2W 1\% RES 681K OHM 1/2W 1\% RES 1MEG OHM 1/2W $1 \%$ POT 1 K OHM 1/2W 10\% POT 500 OHM 1/2W 10\% POT, 5 K OHM, $1 / 2 \mathrm{~W}$ POT 100 K OHM $1 / 2 W$ POT 10K OHM 1/2W POT 1K OHM 1/2W POT 20K OHM 1/2W POT 20KOHM 1/2W POT 200 OHM 1/2W SWITCH TGL SPDT PLUG, SHORTING, . $25^{\prime \prime}$ CTRS HEADER 3 CKT STRAIGHT JUMPER, PWB TEST POINT

JACK, PC MT, . 040 PINS SHUNT JUMPER 0.1" CENTERS *RECPT, MALE SMB,PC MOUNT SCH, VIDEO DIFF GAIN, LFL PWB, VIDEO DIFF GAIN, LFL

| 1.0 EA | R073 |
| :---: | :---: |
| 1.0 EA | R136 |
| 4.0 EA | R077 R082 R085 R130 |
| 15.0 EA | R019 R020 R021 R022 R023 |
|  | R024 R025 R026 R064 R067 R107 R114 R117 |
|  | R118 R121 |
| 4.0 EA | R070 R100 R103 R129 |
| 7.0 EA | R036 R037 R047 R083 R089 R101 R147 |
| 9.0 EA | R056 R057 R058 R059 R060 R061 R062 R063 |
|  | R102 |
| 22.0 EA | R028 R029 R032 R033 R034 R035 R074 R075 |
|  | R076 R081 R092 R113 R116 R122 R133 R134 |
|  | R138 R139 R140 R143 R152 R153 |
| 1.0 EA | R128 |
| 2.0 EA | R030 R031 |
| 2.0 EA | R127 R154 |
| 2.0 EA | R088 R125 |
| 1.0 EA | R099 |
| 1.0 EA | R137 |
| 2.0 EA | R094 R146 |
| 1.0 EA | R132 |
| 7.0 EA | R066 R068 |
|  | R078 R079 R095 R148 R149 |
| 1.0 EA | R158 |
| 1.0 EA | R123 |
| 1.0 EA | R126 |
| 2.0 EA | R159 R160 |
| 3.0 EA | R071 R115 R157 |
| 8.0 EA | R003 R004 R005 R006 R007 R008 R009 R010 |
| 1.0 EA | R120 |
| 2.0 EA | R144 R145 |
| 3.0 EA | R124 R131 R141 |
| 1.0 EA | R001 |
| 4.0 EA | R105 R106 R110 R111 |
| 8.0 EA | R011 R012 R013 R014 R015 R016 R017 R018 |
| 1.0 EA | R002 |
| 2.0 EA | S001 S002 |
| 1.0 EA | JP006 |
| 5.0 EA | JP001 JP002 JP003 JP004 JP005 |
| 9.0 EA | TP001 TP002 TP003 TP004 TP005 TP006 |
|  | TP007 TP008 TP009 |
| 3.0 EA | JP6-1 JP6-2 JP6-3 |
| 5.0 EA |  |
| 2.0 EA | J001 J002 |
| 0.0 EA |  |
| 1.0 EA |  |

Table 7-26. TUNED EXCITER CH-2-9949253 002

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS (d) |
| :--- | :--- | :---: | :--- |
| 3583562000 | SPRING CLIP 0.75 DIA | 8.0 EA | \#BAND PASS FILTER |
| 4840098000 | FLTR BANDPASS CH-2,E3,A1 | 4.0 EA |  |
| 9434999087 | BLANK 19.0" EXTRUSION | 2.0 EA |  |
| 9434999156 | PLATE,MTG,SPARE EXTRUSION | 2.0 EA |  |
| 9882328001 | DP, HX1V | 1.0 EA |  |
| 9928372001 | BASIC HX1V EXC VIS/AUR | 1.0 EA |  |

Table 7-27. TUNED EXCITER CH-3-994 9253003

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS (d) |
| :--- | :--- | :--- | :--- |
| 3583562000 | SPRING CLIP 0.75 DIA | 8.0 EA | \#BAND PASS FILTER |
| 4840099000 | FLTR BANDPASS CH-3, R2 | 4.0 EA |  |
| 9434999087 | BLANK 19.0" EXTRUSION | 2.0 EA |  |
| 9434999156 | PLATE,MTG,SPARE EXTRUSION | 2.0 EA |  |
| 9882328001 | DP,HX1V | 1.0 EA |  |
| 9928372001 | BASIC HX1V EXC VIS/AUR | 1.0 EA |  |

Table 7-28. TUNED EXCITER CH-4-994 9253004

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS (d) |
| :--- | :--- | :--- | :--- |
| 3583562000 | SPRING CLIP 0.75 DIA | 8.0 EA | \#BAND PASS FILTER |
| 4840100000 | FILTER BANDPASS CH-4 | 4.0 EA |  |
| 9434999087 | BLANK 19.0" EXTRUSION | 2.0 EA |  |
| 9434999156 | PLATE,MTG,SPARE EXTRUSION | 2.0 EA |  |
| 9882328001 | DP, HXIV | 1.0 EA |  |
| 9928372001 | BASIC HXIV EXC VIS/AUR | 1.0 EA |  |

Table 7-29. TUNED EXCITER CH-5-994 9253005

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS (d) |
| :--- | :--- | :--- | :--- |
| 3583562000 | SPRING CLIP 0.75 DIA | 8.0 EA | \#BAND PASS FILTER |
| 4840101000 | FLTR BANDPASS CH-5, R3 | 4.0 EA |  |
| 9434999087 | BLANK 19.0" EXTRUSION | 2.0 EA |  |
| 9434999156 | PLATE,MTG,SPARE EXTRUSION | 2.0 EA |  |
| 9882328001 | DP, HX1V | 1.0 EA |  |
| 9928372001 | BASIC HXIV EXC VIS/AUR | 1.0 EA |  |

Table 7-30. TUNED EXCITER CH-6-994 9253006

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS (d) |
| :--- | :--- | :--- | :--- |
| 3583562000 | SPRING CLIP 0.75 DIA | 8.0 EA | \#BAND PASS FILTER |
| 4840102000 | FLTR BANDPASS CH-6, R4 | 4.0 EA |  |
| 9434999087 | BLANK 19.0" EXTRUSION | 2.0 EA |  |
| 9434999156 | PLATE,MTG,SPARE EXTRUSION | 2.0 EA |  |
| 9882328001 | DP, HXIV | 1.0 EA |  |
| 9928372001 | BASIC HXIV EXC VIS/AUR | 1.0 EA |  |

Table 7-31. TUNED EXCITER CH-7-994 9253007

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS (d) |
| :--- | :--- | :--- | :--- |
| 3583561000 | SPRING CLIP 0.50 DIA | 8.0 EA | \#BAND PASS FILTER |
| 4840072000 | FLTR BANDPASS CH-7,E5,A6,R6 | 4.0 EA |  |
| 9434999087 | BLANK 19.0" EXTRUSION | 2.0 EA |  |
| 9434999156 | PLATE,MTG,SPARE EXTRUSION | 2.0 EA |  |
| 9882328001 | DP, HX1V | 1.0 EA |  |
| 9928372001 | BASIC HX1V EXC VIS/AUR | 1.0 EA |  |

Table 7-32. TUNED EXCITER CH-8-994 9253008

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS (d) |
| :--- | :--- | :--- | :--- |
| 3583561000 | SPRING CLIP 0.50 DIA | 8.0 EA | \#BAND PASS FILTER |
| 4840073000 | FLTR BANDPASS CH-8,E6, A7,R7 | 4.0 EA |  |
| 9434999087 | BLANK 19.0" EXTRUSION | 2.0 EA |  |
| 9434999156 | PLATE,MTG,SPARE EXTRUSION | 2.0 EA |  |
| 9882328001 | DP, HX1V | 1.0 EA |  |
| 9928372001 | BASIC HX1V EXC VIS/AUR | 1.0 EA |  |

Table 7-33. TUNED EXCITER CH-9-994 9253009

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS (d) |
| :--- | :--- | :--- | :--- |
| 3583561000 | SPRING CLIP 0.50 DIA | 8.0 EA | \#BAND PASS FILTER |
| 4840074000 | FILTER BANDPASS CH-9 | 4.0 EA |  |
| 9434999087 | BLANK 19.0" EXTRUSION | 2.0 EA |  |
| 9434999156 | PLATE,MTG,SPARE EXTRUSION | 2.0 EA |  |
| 9882328001 | DP, HX1V | 1.0 EA |  |
| 9928372001 | BASIC HXIV EXC VIS/AUR | 1.0 EA |  |

Table 7-34. TUNED EXCITER CH-10-994 9253010

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS (d) |
| :--- | :--- | :--- | :--- |
| 3583561000 | SPRING CLIP 0.50 DIA | 8.0 EA | \#BAND PASS FILTER |
| 4840075000 | FLTR BANDPASS CH-10,E7,A8,R8 | 4.0 EA |  |
| 9434999087 | BLANK 19.0" EXTRUSION | 2.0 EA |  |
| 9434999156 | PLATE,MTG,SPARE EXTRUSION | 2.0 EA |  |
| 9882328001 | DP, HX1V | 1.0 EA |  |
| 9928372001 | BASIC HX1V EXC VIS/AUR | 1.0 EA |  |


|  | TabIe 7-35. TUNED EXCITER CH-11-994 9253011 |  |  |  |
| :--- | :--- | :--- | :--- | :---: |
| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS (d) |  |
| 3583561000 | SPRING CLIP 0.50 DIA | 8.0 EA | \#BAND PASS FILTER |  |
| 4840076000 | FLTR BANDPASS CH-11,E8,A9,R9 | 4.0 EA |  |  |
| 9434999087 | BLANK 19.0" EXTRUSION | 2.0 EA |  |  |
| 9434999156 | PLATE,MTG,SPARE EXTRUSION | 2.0 EA |  |  |
| 9882328001 | DP, HX1V | 1.0 EA |  |  |
| 9928372001 | BASIC HX1V EXC VIS/AUR | 1.0 EA |  |  |

Table 7-36. TUNED EXCITER CH-12-994 9253012

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS (d) |
| :--- | :--- | :--- | :--- |
| 3583561000 | SPRING CLIP 0.50 DIA | 8.0 EA | \#BAND PASS FILTER |
| 4840077000 | FLTR BANDPASS CH-12,E9,R10 | 4.0 EA |  |
| 9434999087 | BLANK 19.0" EXTRUSION | 2.0 EA |  |
| 9434999156 | PLATE,MTG,SPARE EXTRUSION | 2.0 EA |  |
| 9882328001 | DP, HX1V | 1.0 EA |  |
| 9928372001 | BASIC HX1V EXC VIS/AUR | 1.0 EA |  |

Table 7-37. TUNED EXCITER CH-13-9949253 013

| HARRIS P/N | DESCRIPTION | QTY/UM | REF. SYMBOLS/EXPLANATIONS (d) |
| :--- | :--- | :---: | :--- |
| 3583561000 | SPRING CLIP 0.50 DIA | 8.0 EA | \#BAND PASS FILTER |
| 4840078000 | FLTR BANDPASS CH-13,E10,A10 | 4.0 EA |  |
| Rev. P2: 05-31-00 |  |  |  |
|  |  | WARNING: Disconnect primary power prior to servicing. |  |


| 9434999087 | BLANK 19.0" EXTRUSION | 2.0 EA |
| :--- | :--- | :--- |
| 9434999156 | PLATE,MTG,SPARE EXTRUSION | 2.0 EA |
| 9882328001 | DP, HX1V | 1.0 EA |
| 9928372001 | BASIC HX1V EXC VIS/AUR | 1.0 EA |

## ELECTROSTATIC DISCHARGE CONTROL A GUIDE TO HANDLING INTEGRATED CIRCUITS

This paper discusses methods and materials recommended for protection of ICs against ESD damage or degradation during manufacturing operations vulnerable to ESD exposure. Areas of concern include dice prep and handling, dice and package inspection, packing, shipping, receiving, testing, assembly and all operations where ICs are involved.
All integrated circuits are sensitive to electrostatic discharge (ESD) to some degree. Since the introduction of integrated circuits with MOS structures and high quality junctions, safe and effective means of handling these devices have been of primary importance.

If static discharge occurs at a sufficient magnitude, 2 kV or greater, some damage or degradation will usually occur. It has been found that handling equipment and personnel can generate static potentials in excess of 10 kV in a low humidity environment; thus it becomes necessary for additional measures to be implemented to eliminate or reduce static charge. Avoiding any damage or degradation by ESD when handling devices during the manufacturing flow is therefore essential.

## ESD Protection and Prevention Measures

One method employed to protect gate oxide structures is to incorporate input protection diodes directly on the monolithic chip. However, there is no completely foolproof system of chip input protection in existence in the industry.
In areas where ICs are being handled, certain equipment should be utilized to reduce the damaging effects of ESD. Typically, equipment such as grounded work stations, conductive wrist straps, conductive floor mats, ionized air blowers and conductive packaging materials are included in the IC handling environment. Any time an individual intends to handle an IC, in any way, they must insure they have been grounded to eliminate circuit damage.
Grounding personnel can, practically, be performed by two methods. First, grounded wrist straps which are usually made of a conductive material, such as Velostat or metal. A resistor value of 1 megohm ( $1 / 2$ watt) in series with the strap to ground completes a discharge path for ESD when the operator wears the strap in contact with the skin. Another method is to insure direct physical contact with a grounded, conductive work surface.

This consists of a conductive surface like Velostat, covering the work area. The surface is connected to a 1 megohm ( $1 / 2$ watt) resistor in series with ground.

In addition to personnel grounding, areas where work is being performed with ICs, should be equipped with an ionized air blower. Ionized air blowers force positive and negative ions simultaneously over the work area so that any nonconductors that are near the work surface would have their static charge neutralized before it would cause device damage or degradation.
Relative humidity in the work area should be maintained as high as practical. When the work environment is less than $40 \%$ RH, a static build-up condition can exist on nonconductors allowing stored charges to remain near the ICs causing possible static electricity discharge to ICs.
Integrated circuits that are being shipped or transported require special handling and packaging materials to eliminate ESD damage. Dice or packaged devices should be in conductive carriers during all phases of transport and handling. Leads of packaged devices can be shorted by tubular metalic carriers, conductive foam or foil.

## Do's and Don'ts for Integrated Circuit Handling

## Do's

Do keep paper, nonconductive plastic, plastic foams and films or cardboard off the static controlled conductive bench top. Placing devices, loaded sticks or loaded burn-in boards on top of any of these materials effectively insulates them from ground and defeats the purpose of the static controlled conductive surface.
Do keep hand creams and food away from static controlled conductive work surfaces. If spilled on the bench top, these materials will contaminate and increase the resistivity of the work area.
Do be especially careful when using soldering guns around conductive work surfaces. Solder spills and heat from the gun may melt and damage the conductive mat.
Do check the grounded wrist strap connections daily. Make certain they are snugly fitted before starting work with the product.
Do put on grounded wrist strap before touching any devices. This drains off any static build-up from the operator.
Do know the ESD caution symbols.
Do remove devices or loaded sticks from shielding bags only when grounded via wrist strap at grounded work station. This also applies when loading or removing devices from the antistatic sticks or the loading on or removing from the burn-in boards.

Do wear grounded wrist straps in direct contact with the bare skin never over clothing.

Do use the same ESD control with empty burn-in boards as with loaded boards if boards contain permanently mounted ICs as part of driver circuits.

Do insure electrical test equipment and solder irons at an ESD control station are grounded and only uninsulated metal hand tools be used. Ordinary plastic solder suckers and other plastic assembly aids shall not be used.

Do use ionizing air blowers in static controlled areas when the use of plastic (nonconductive) materials cannot be avoided.

## Don'ts

Don't allow anyone not grounded to touch devices, loaded sticks or loaded burn-in boards. To be grounded they must be standing on a conductive floor mat with conductive heel straps attached to footwear or must wear a grounded wrist strap.

Don't touch the devices by the pins or leads unless grounded since most ESD damage is done at these points.

Don't handle devices or loaded sticks during transport from work station to work station unless protected by shielding bags. These items must never be directly handled by anyone not grounded.

Don't use freon or chlorinated cleaners at a grounded work area.

Don't wax grounded static controlled conductive floor and bench top mats. This would allow build-up of an insulating layer and thus defeating the purpose of a conductive work surface.

Don't touch devices or loaded sticks or loaded burn-in boards with clothing or textiles even though grounded wrist strap is worn. This does not apply if conductive coats are worn.

Don't allow personnel to be attached to hard ground. There must always be 1 megohm series resistance ( $1 / 2$ watt between the person and the ground).

Don't touch edge connectors of loaded burn-in boards or empty burn-in boards containing permanently mounted
driver circuits when not grounded. This also applies to burnin programming cards containing ICs.

Don't unload stick on a metal bench top allowing rapid discharge of charged devices.
Don't touch leads. Handle devices by their package even though grounded.

Don't allow plastic "snow or peanut" polystyrene foam or other high dielectric materials to come in contact with devices or loaded sticks or loaded burn-in boards.

Don't allow rubber/plastic floor mats in front of static controlled work benches.

Don't solvent-clean devices when loaded in antistatic sticks since this will remove antistatic inner coating from sticks.

Don't use antistatic sticks for more than one throughput process. Used sticks should not be reused unless recoated.

## Recommended Maintenance Procedures

Daily:
Perform visual inspection of ground wires and terminals on floor mats, bench tops, and grounding receptacles to ensure that proper electrical connections via 1 megohm resistor (1/2 watt) exist.

Clean bench top mats with a soft cloth or paper towel dampened with a mild solution of detergent and water.

## Weekly:

Damp mop conductive floor mats to remove any accumulated dirt layer which causes high resistivity.
Annually:
Replace nuclear elements for ionized air blowers.
Review ESD protection procedures and equipment for updating and adequacy.

## Static Controlled Work Station

The figure below shows an example of a work bench properly equipped to control electro-static discharge. Note that the wrist strap is connected to a 1 megohm resistor. This resistor can be omitted in the setup if the wrist strap has a 1 megohm assembled on the cable attached.



[^0]:    ${ }^{1}$ Inquire about avallability of other CCIR aystem standerds.
    ${ }^{2}$ Al spece guaranteed at 0.5 w without cormetion; at 1.0 w with correction.
    ${ }^{3} \pm 2 \mathrm{~Hz}$ with optional Precise Frequency Control for Sytem M.
    4 Relative to Banking.

