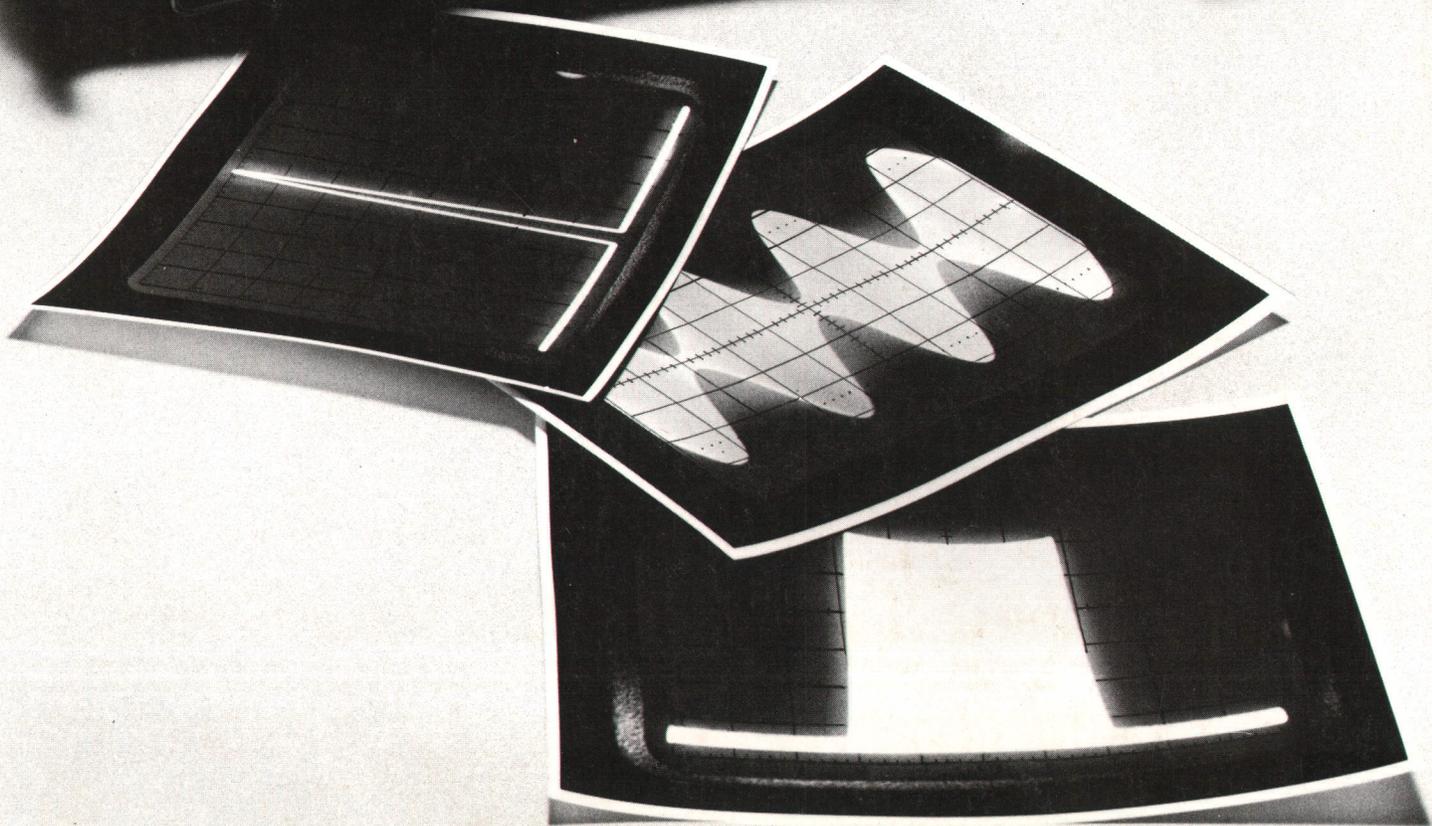


# HEWLETT-PACKARD JOURNAL



# A Solid State VHF Signal Generator for Today's Exacting Requirements

*The spectral purity of a vacuum-tube oscillator and the freedom from aging effects characteristic of solid-state oscillators are combined in a new 450 kHz–550 MHz signal generator. High-quality FM and AM capabilities are included too, in addition to CW.*

**By Raymond M. Shannon, Kenneth L. Astrof, Michael S. Marzalek, and Larry C. Sanders.**

**F**OR ABOUT 20 YEARS THE FAMILIAR HP 608 VACUUM-TUBE SIGNAL GENERATOR has been the instrument of first choice for critical RF testing. Because its performance was consistent, many users considered it a standard even where its performance characteristics, essential to the tests at hand, were incompletely specified.

HP has recognized for years how desirable it would be to bring the advantages of solid-state circuitry to signal generators of this caliber, and indeed work was begun some years ago to do so. One of the reasons why it has taken time to accomplish the task has been the difficulty of matching the vacuum-tube oscillators' extraordinary demonstrated (if not always specified) spectral purity.

## Objectives

From the start this program aimed to produce a solid-state generator which, as a minimum, would match the CW performance of the old vacuum-tube generators. In addition, it would also incorporate a high quality FM capability to meet the needs of the fast-growing communications industry, and it would cover the IF as well as the RF ranges, which formerly required two generators. Desirable options would be built-in counter capability, for precision frequency settability, and self-contained synchronization capability for long-term stability.

## Conflicting Requirements

Each aspect of the objectives calls for a different design approach. A CW source free of non-harmonic or sub-harmonic spurious generations and low in sideband noise would preferably be a fundamental oscillator, perhaps band-switched to cover the desired range of frequencies, as were the tube generators. Such an approach, it was quickly

determined, could not produce the spectral purity that was a primary instrument objective. This is because of practical limitations on tank-circuit Q and on the signal-to-noise ratio attainable with transistors and with the varactors needed for FM.

Perhaps the best approach to FM generation is to translate the output of a fixed-frequency oscillator, to which accurate and constant FM may easily be applied, down to the desired frequency range by heterodyning it with a second tunable oscillator. This technique was attractive also as a simple



**Cover:** CW, AM, and FM—the scope photos depict the output capabilities of HP's new Model 8640A/B 0.45–550 MHz Signal Generator. Not so easily depictable is the exceptional purity of the new Generator's RF output, which defines the state of the art for solid-state generators. For a verbal depiction,

see the article beginning on this page.

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## Signal Generators and Radio Receiver Measurements

Modern communications systems are placing increased demands on the instruments that test them. Traditional instruments are no longer adequate for state-of-the-art receiver measurements, so a new class of signal generators is needed to respond to these more stringent requirements.

Signal generators of today must have better frequency stability and provide more precise modulation and level control than their predecessors. Spectral purity is also taking on increasing importance, and this trend is likely to continue as receiver technology advances and spectrum crowding becomes an ever greater problem.

For any receiver test, being able to tune the generator accurately and with sufficient resolution to set the RF frequency precisely on the particular channel desired, is important. Then the generator must remain at the set frequency long enough to complete the measurements. Thus the frequency stability of the generator is a prime consideration—it should be commensurate with the bandwidth of the receiver under test.

Crystal-controlled receivers, for example those used in HFSSB and narrowband FM communication systems, present some of the most stringent requirements on a signal generator. With the tightening of carrier specifications by governmental regulatory agencies, it has become necessary for the generator itself to be crystal controlled so as to maintain the required stability. Synthesized signal generators (e.g. output always derived from a precision standard) and continuous-tuning signal generators with internal phase-lock synchronizers both serve this purpose.

One of the most demanding tests facing a modern signal

generator is the measurement of adjacent channel rejection ratios on a narrowband UHF receiver. In this test, two generators are used. One is tuned to the desired channel in the receiver and a reference signal-to-noise level is established. The second generator is then tuned to an adjacent channel and its signal level increased until the signal-to-noise ratio measured in the first channel is reduced by some specified amount (typically 6 dB). Sideband phase noise on the second signal that falls into the first channel must be below some minimum amount so as not to interfere with the measurement.

A wide range of power output is needed to check the dynamic range of AGC circuits. In particular, measurements of "least-usable" sensitivity require microvolt level output from the signal generator. Achieving these low levels is not simply a matter of adding more attenuation to the signal generator output—leakage levels from the generator itself may be at higher levels unless careful attention is paid to adequate rf shielding.

Today's testing methods place conflicting requirements on a signal generator. For thorough checkout of a multi-channel receiver, automatic test systems are largely used as a means of reducing costs. These require signal sources that can be tuned by remote control rapidly but accurately to several different frequencies. Frequency synthesizers meet this requirement admirably but the very nature of a synthesizer makes it difficult to hold spurious responses and sideband noise to very low levels. Thus, many test set-ups use a frequency synthesizer for several of the tests, and a standard signal generator, such as the Model 8640A/B for the tests where signal purity is critical.

means of achieving wide frequency range. But the scheme has drawbacks with respect to the higher priority CW objectives. The mixer produces spurious outputs, and higher sideband noise results from the translation of the carrier to a lower frequency with 1:1 translation of residual FM. The degradation in residual FM, sideband noise and stability, compared to the equivalent fundamental oscillator, is approximately proportional to the ratio of the sum of the two heterodyned frequencies to their difference (the actual output frequency).

Another attractive method of generation is multiplication or division of a signal to translate its frequency from a range where a single oscillator could be optimized for CW and FM performance. The trade-off in this approach is that maximum FM deviation varies as bands are changed, but if the required deviations can be achieved at the most often-used RF and IF frequencies, this could be acceptable. Division would seem to be preferable, since multiplication results in spurious subharmonics and increased noise.

Little has been said here about attaining the desired AM performance, because this is accom-

plished in the level control portion of the instrument which is relatively independent of the generation method.

Such was the reasoning that led to selecting the scheme shown in simplified form in the block diagram of Fig. 3. The main advantages of this scheme are: 1) elimination of tracking errors and restabilization time when switching between bands, since the tank circuit is not switched; 2) freedom to use a coaxial-cavity tuned oscillator, because the master oscillator operates in the UHF band, thereby achieving the best possible spectral purity; and 3) facility to incorporate CW, FM, and AM generation, a 550-MHz counter, and a frequency synchronizer all in one unit. This approach is not unique to this instrument, the Model 8640A/B, but the resulting performance is, and that is due to its execution. Among many reasons for this are proprietary manufacturing capability in high-frequency monolithic integrated circuits, microwave power transistors, and thin-film technology.

### System Organization

While the building blocks of the system are dealt



**Fig. 1.** New Model 8640A solid-state Signal Generator, which covers 450 kHz to 550 MHz range of frequencies, rivals special purpose vacuum-tube generators in spectral purity. Besides highly stable CW signal, new Generator produces modulated signals, both AM and FM, with calibrated modulation. Wide range of output levels, +19 to -145 dBm, meets requirements of broad variety of RF tests.

**Fig. 2.** Model 8640B Signal Generator is identical to Model 8640A in range of capabilities but also includes 550-MHz Counter for highly accurate frequency setting. In addition, Model 8640B has phase-locking to give crystal stability to output signal. Unit shown here also has optional audio oscillator.

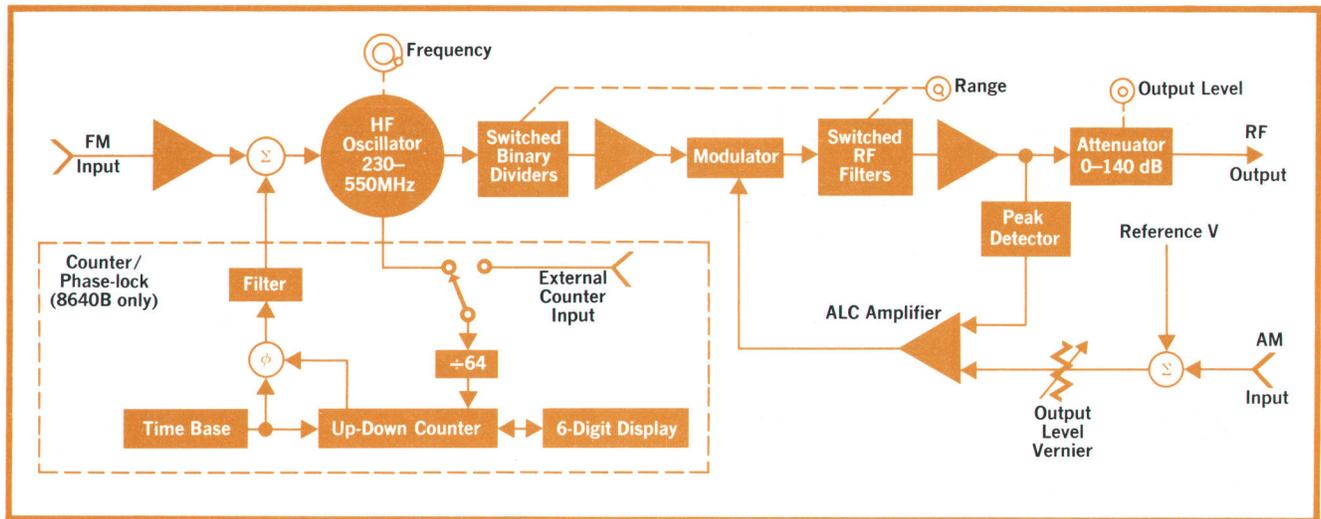
with individually in the pages which follow, their organization bears importantly on the results obtained.

Sub-harmonic generations might reasonably have been expected from the inclusion of counter circuits. This has been avoided by isolation. The counter's pickup in the cavity is separate from the range dividers' pickup; the counter is also separated from the cavity by a buffer amplifier. Then too, the cavity itself acts as a filter against any sub-harmonics generated in the counting process. Thanks to the availability of 550-MHz monolithic IC's for the counter circuits, it was practical to use an entirely separate scaler to divide down to a frequency more suitable for counting, so the divider chain in the output path need not run at a rate lower than the selected frequency. This has virtually eliminated sub-harmonics in the output. It also makes available a 550-MHz counting capability for measuring external signals.

It has become common practice in instruments to place all signal amplification in one lump at the output. This practice was considered not suitable for the new Generator because the high S/N ratio

of the oscillator would be degraded by the reduction in signal amplitude that results from the inherent insertion loss of the modulator, the 4 dB of attenuation needed for leveling, the 6 dB for AM, and up to 18 dB for output level adjustment. In quality receivers, gain is distributed in such a way that there is always a net forward gain in the signal path, thereby attaining the lowest possible noise figure. It was possible to adopt this practice in the new Generator because proprietary microwave transistor and thin-film capability made it economically feasible to use two essentially identical amplifiers, one ahead of the lossy modulator and the other as the output amplifier. The S/N improvement, over that obtained when all gain is lumped at the output, is 8 to 18 dB, depending upon output level setting. The additional buffering of the oscillator that the forward amplifier provides has the further benefit of virtually eliminating oscillator pulling by the modulator.

The same thin-film wideband feedback amplifier also contributes to achieving low harmonics and desirable output impedance characteristics. Digital dividers translate the oscillator frequency down to



**Fig. 3.** Block diagram of Model 8640A/B Signal Generator. HF oscillator always operates in 230–550 MHz range, allowing use of high-Q cavity as resonant circuit. Frequency dividers give lower ranges. Counter and phase-lock circuits are in Model 8640B only; otherwise Models 8640A and 8640B are identical.

10 octave-wide bands, and switched low-pass filters attenuate the consequent harmonics. It was first thought that these filters should be as far down the signal path as possible, so as to attenuate amplifier-caused harmonics as well. That would be between the output amplifier and the peak detector that is used to control signal level. It was found that the filters then prevented the feedback amplifier from correcting the waveform distortion caused by the peak detector loading. Better harmonic performance resulted when the filters were moved ahead of the output amplifier.

As for output impedance, the peak detector and AGC loop form an apparent constant-voltage source, and a series resistor establishes impedance. This holds true, however, only within a band above and below the carrier that is equal to the AGC bandwidth (the AM modulation bandwidth). Further away, the output impedance is more complex, but not as severe a departure as would be seen looking back into a filter instead of the low output impedance of the amplifier. Out-of-band output VSWR is typically 1.5 or better. That becomes important, for example, when driving a wideband device whose stability might be affected by source impedance, or when combining the outputs of two generators.

The output amplifier also has sufficient slew rate ( $> 15000 \text{ V}/\mu\text{s}$ ) to deliver a linear 19 dBm of power at frequencies up to and greater than 500 MHz.

### The Cavity Oscillator, Origin of Spectral Purity

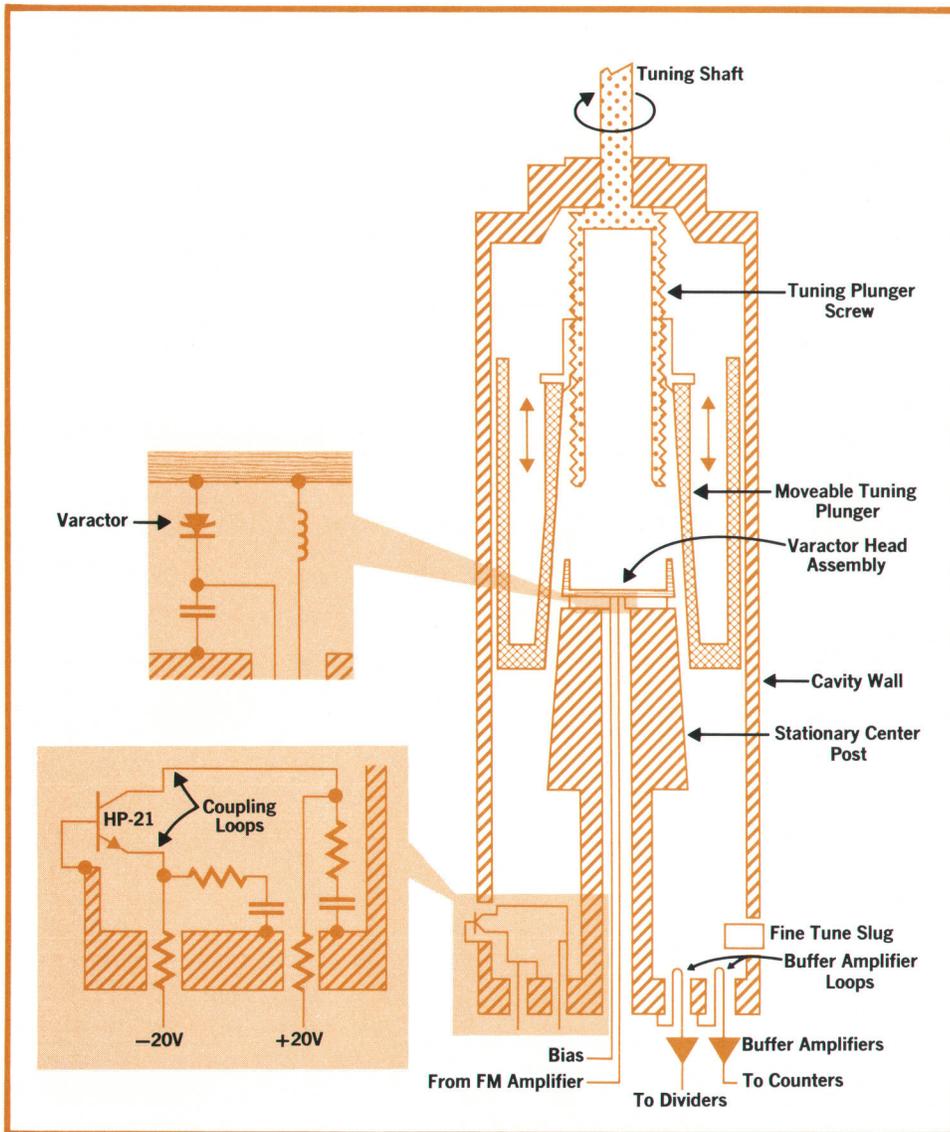
The master oscillator is of the foreshortened coaxial resonator type, tuned with a non-contacting plunger (Fig. 4). Fine tuning is by insertion of a

small slug into the cavity. Feedback for oscillation is by collector and emitter loops coupled magnetically through the cavity. AGC, necessary for stable oscillation, is accomplished by modulating the conduction angle with self bias developed by rectification in the oscillator base-emitter junction. Oscillator stability is shown in Fig. 5.

The ideal goal for a signal generator is to produce a single spectral line in the frequency domain. This ideal is never achieved because of thermal and excess noise in the transistor and other practical components. The amplitude of this noise is generally flat with respect to frequency, perhaps rising at the high end because of partition noise in the transistor above  $\sqrt{1-\alpha} f_c$ . It may increase at the lower frequencies because of  $1/f$  noise.

In analyzing this situation, the oscillator can be considered a feedback system in which the phase shift around the loop must equal zero for sustained oscillation. The one-sided bandwidth of this loop is equal to the ratio of the center frequency to twice the operating Q of the tank. Noise causes both amplitude and phase modulation of the desired oscillator frequency. The AM is removed by gain control action in the oscillator. Phase modulation outside the loop bandwidth is left unchanged, while inside that band the phase deviation is converted to an equivalent frequency deviation by the phase vs. frequency characteristic of the tank circuit.

Now, since the original noise spectrum was flat, and since the modulation index is equal to the deviation divided by the modulation rate, the modulation index (and therefore the power in the sideband) increases as the equivalent modulation rate de-



**Fig. 4.** Coaxial resonant cavity oscillator is heart of instrument. Active device is low-noise transistor (HP-21) operating in common-base configuration biased by current source. Cavity is less than  $1/4$  wavelength long so that short at bottom end causes opposite end near tuning plunger to appear inductive. Capacitance between tapered tuning plunger and center post resonates with resulting inductance at selected frequency. Moving plunger changes capacitance and thus changes resonating frequency. Varactor diodes are in series with capacitance between varactor end cap and plunger; total capacitance thus formed is in parallel with plunger capacitance.

creases at noise frequencies closer to the carrier. This noise increases towards the carrier at 6 dB/octave (from the original signal-to-phase noise) until the effect of  $1/f$  noise becomes significant ( $1/f$  noise is up-converted to RF by the nonlinearity of the oscillator transistor). Then noise rises at 9 dB/octave.

Because the output from the oscillator is taken from an independent pickup loop, the filtering effect of the cavity attenuates noise sidebands by 6 dB/octave above the loop bandwidth until reaching the thermal-plus-excess noise floor of the buffer amplifier, about 160 dB down. These characteristics are summarized in Fig. 6.

Thus it can be seen that the amplitude of oscillator noise power, at any frequency removed from the carrier, depends on the original signal-to-additive-noise ratio at the input port of the transistor, and upon operating  $Q$ . The limit on actual signal

power at the input is set by the permissible voltage swings on the transistor and on the varactor tuning element that provides FM. Every effort, therefore, was devoted to maximizing operating  $Q$ , which is more than 500.

The lump sum effect of noise over any given bandwidth can be found by integrating the noise curve over that bandwidth, and its net effect is the residual FM. That is why it is always absolutely essential, when stating the residual FM of a signal generator, to state the upper and lower limits of the measurement bandwidth.

Other possible contributors to residual FM are line-related sidebands and microphonics. Both of these make negligible contribution to the output of this instrument in any normal laboratory environment. Other than the emitter and collector loops, which are embedded in plastic blocks, the main sources of microphonic effects are the cavity center

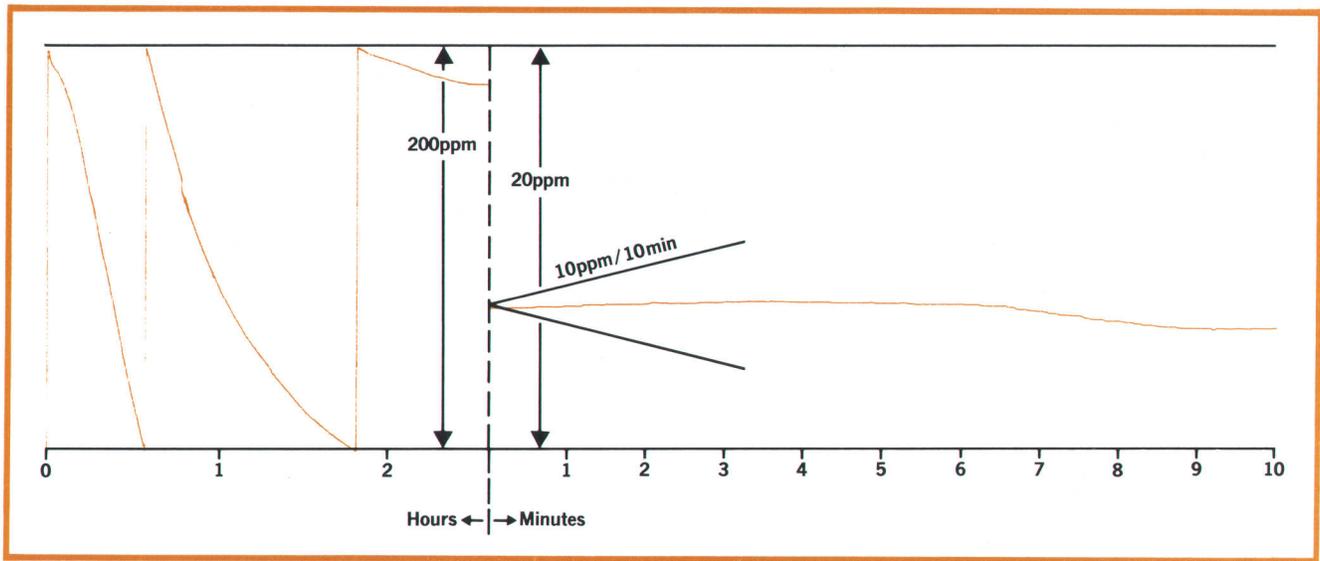


Fig. 5. Frequency stability and warm-up characteristics of Model 8640A/B Signal Generator are shown by recording of 500-MHz output frequency as function of time from cold start. Recorder sensitivity and chart speed were changed after 2 hours to show short-term stability.

conductor and tuning plunger. Both of these are supported in a heavily damped structure to minimize microphonic effects.

#### Constant Deviation FM

FM is accomplished with a varactor imbedded in the cavity center conductor (Fig. 4). It is coupled into the tank circuit with the tuning plunger, which is so tapered as to linearize the frequency-tuning curve and to cause FM sensitivity to vary in an easily-compensatable way as the oscillator is tuned across its range. A tapped pot gives a two-segment, piece-wise linear compensation for FM sensitivity vs. frequency. Across the specified octave bandwidth tuning range of the oscillator, less than 2% variation typically is encountered. In the band-

overlap region sensitivity roll-off is slightly greater.

Because the dividers which generate the lower output frequencies also divide down the oscillator deviation, the FM system gain must change appropriately with band changes to keep FM deviation constant. Otherwise the user would have to readjust the FM controls each time the band is switched if he wished to maintain a given deviation. Furthermore, the drive signal to the varactor ought to be shaped to compensate for varactor nonlinearity. This involves compression of the negative peaks of the modulating waveform and expansion of the positive peaks. The expansion is accomplished with a diode shaping network in the feedback path of an operational amplifier to vary its gain as a function of signal level. Negative compression is done with a

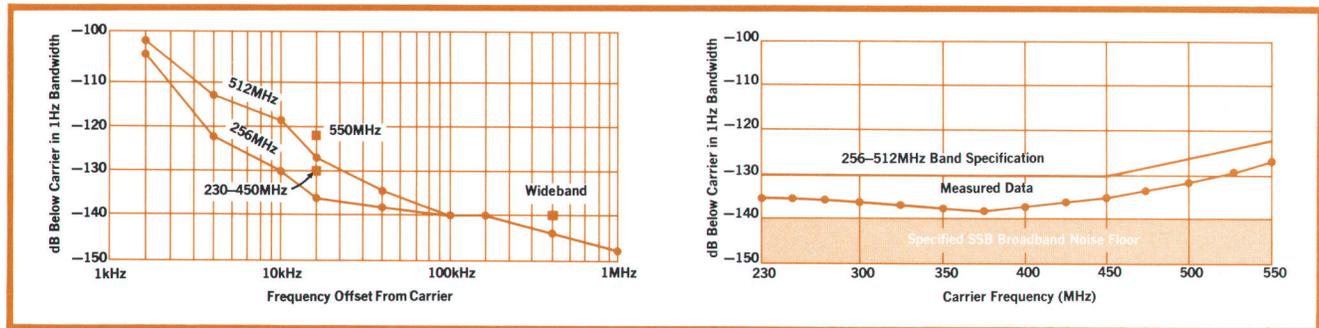
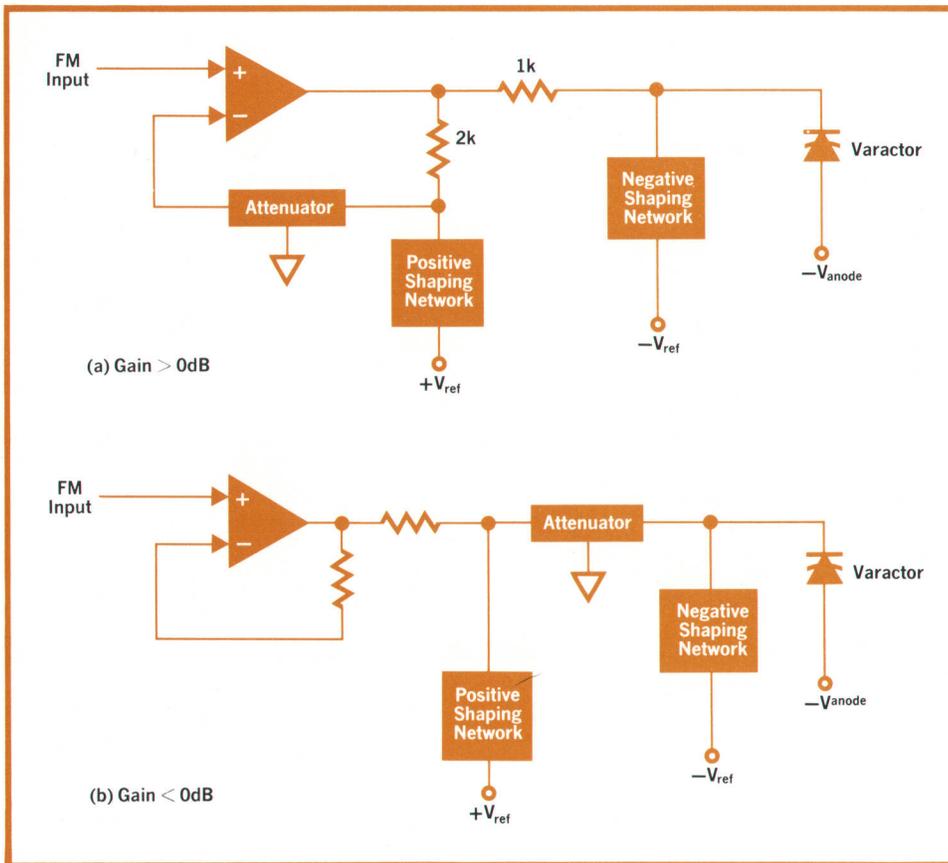


Fig. 6. Measured single-sideband noise (in 1-Hz bandwidth) versus offset from carrier (*l*). Square markers indicate specified limits. Low level of close-in noise is especially important for tests of adjacent channel interference. Signal-to-phase noise (in 1-Hz bandwidth) at 20 kHz offset from carrier is shown as a function of carrier frequency in (*r*). On lower frequency ranges, noise decreases approximately 6 dB per range down to noise floor.



**Fig. 7.** Shaping network for varactor control during frequency modulation is switched according to drive level required. When high drive levels are needed (a), attenuator and positive-shaping network are switched into amplifier feedback network. When low drive levels are needed (b), attenuator and shaping network are in output network.

similar network on the output.

The simplest way to achieve the gain change as the band is changed would be to place a programmed attenuator either before or after a fixed-gain amplifier. There are difficulties with either placement. If the attenuator follows the shaping amplifier, it would interact and disturb the shaping. In front of the amplifier, it would decrease the S/N ratio of the FM system, in turn affecting the oscillator sideband noise. The solution is to place the attenuator and positive shaping network in the feedback path when a gain greater than one is required of the amplifier (Fig. 7), and thus when shaping is important. When small signals are required and positive shaping is no longer needed, the attenuator is switched into place after the amplifier, now configured for unity gain. In this way gain is applied only in the wide-deviation modes where good S/N is achieved anyway. In low-deviation settings the amplifier noise actually is attenuated; it makes no contribution to sideband noise at peak deviation settings 1/16 of maximum or less.

To achieve wide deviation at high rates, 30-volt swings are needed. These are delivered by a discrete-device operational amplifier. The result is a 3-dB bandwidth specification of 250 kHz for the modulating signal; 300 to 500 kHz is typical, de-

pending on band and deviation settings.

The wide FM deviation possible with this Generator allows its use as a sweep-frequency generator by application of a sawtooth waveform to the FM input. The sweep waveform from an oscilloscope, for example, could be used (with suitable attenuation) for tests and alignment of IF filters and discriminators. FM distortion is plotted in Fig. 8.

#### Amplitude Control

The heart of the amplitude leveling and modulating system is a broadband, transformer-coupled, balanced, diode modulator (Fig. 9). It must operate over a range of 60 dB: 10 dB for vernier range, 46 for 99% AM, and 4 dB for leveling. To preserve S/N ratio it is driven with input power of some 17 dBm but it must have second harmonic distortion below 40 dB up to 8 MHz because of filtering arrangements. The balanced configuration accomplishes the latter requirement and has the added advantage of greatly reducing feedthrough of the modulating signal, important in the pulse mode. It is also important to keep the diodes from rectifying the drive signal when driven at this high level, which would self-bias the diodes and degrade linearity and frequency response. This problem is overcome by driving the diodes with a high-impedance modulation

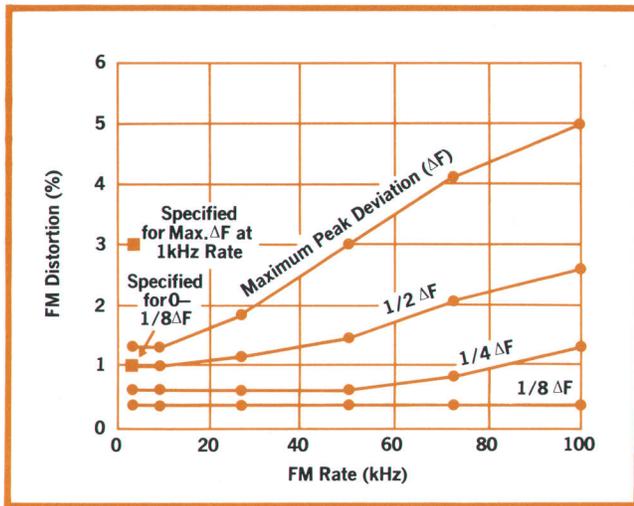


Fig. 8. FM distortion as a function of FM rate measured on 8-16 MHz band. Performance on other bands is similar.

driver that will not supply rectification current.

This modulator, with an RF peak detector and an ALC amplifier, accomplishes output leveling, output level vernier, and modulation in a conventional ALC feedback control system. Long-term amplitude stability is shown in Fig. 10. A negative peak detector is used since NPN transistors are used in the amplifier's output stage, and they have higher current sinking capability on negative peaks. This active pulldown minimizes the effect of nonlinear detector loading.

Additional level control is provided by a 140-dB attenuator with pads of 10, 20 (two of them), 30 and 60 dB, selected in combination to achieve desired attenuation. Output level has normally been specified as flatness plus some attenuator error, typically 0.1 dB/10 dB. That was reasonable when the attenuator was of the waveguide-beyond-cutoff type, with a continuous error function proportional to motion of the attenuator probe. Most new genera-

tors, however, use step attenuators. The error limits for any given total attenuation still are approximately  $\pm 0.1$  dB for each 10 dB of attenuation between 10 dB steps but, if the worst possible algebraic sum of errors should occur, the step-to-step range of error could amount to as much as 1.1 dB (when switching between 50 and 60 dB steps). To reduce this effect, an adjustable calibrating correction signal is applied to the metering circuit whenever the 30- and 60-dB pads are switched in. Thus the Model 8640A/B is specified in terms of a combined maximum error over a stated power output range. By using a power meter to calibrate the output at a particular frequency with the 20-dB pad switched in, the user can be assured that the worst case total error on lower amplitude ranges would be less than  $\pm 1$  dB, plus the error of the power measurement. Typical error is much less than this, especially at frequencies below 100 MHz.

### Amplitude Modulation

Applying an ac signal onto the reference dc that controls output level produces amplitude modulation by action of the feedback loop. Percentage modulation is made nearly independent of output level by having the output vernier control the ac signal along with dc, maintaining a constant ratio.

The leveling loop also suppresses incidental AM during FM. To maximize this capability, as well as to provide as much AM capability as possible, the AM bandwidth was made 100 kHz at 50% modulation. AM distortion levels are shown in Fig. 11.

The maximum rate of AM for any given modulation depth is set by the time constant of the RC filter at the detector output since the derivative of the modulated envelope must not exceed the derivative of the capacitor decay; this is the slew rate limitation of the ALC loop. A short time constant is required for wide AM bandwidths.

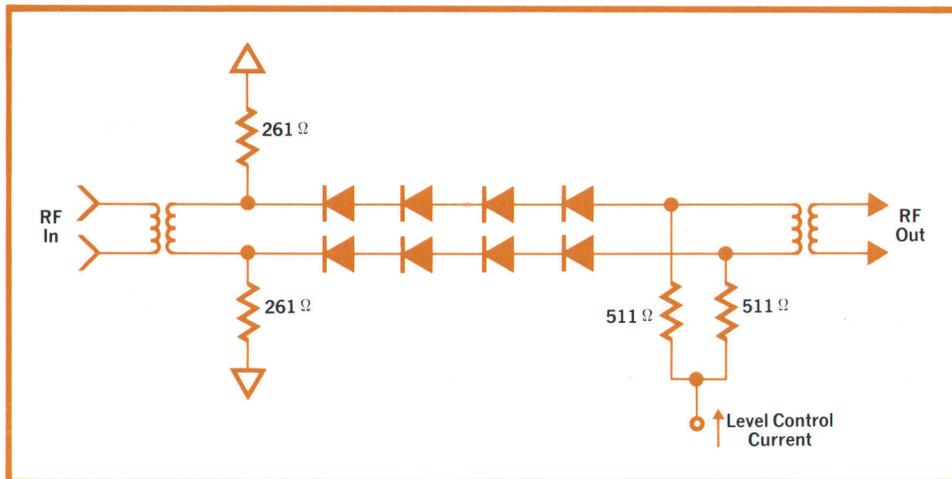
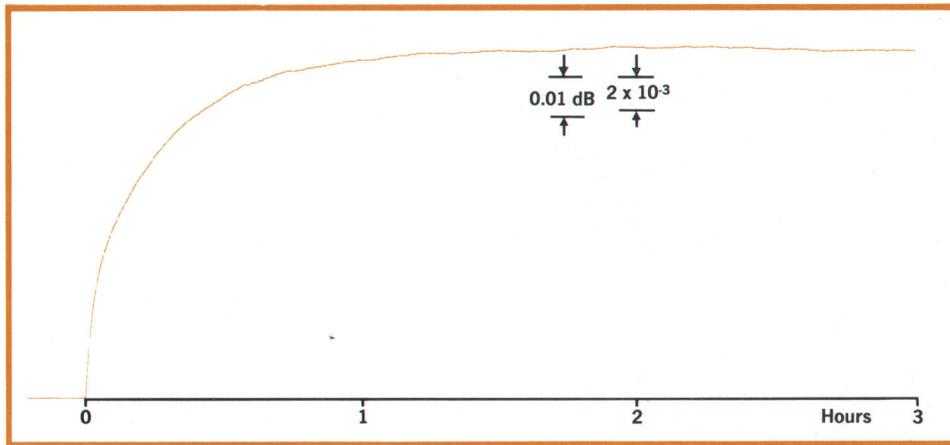


Fig. 9. Broadband modulator uses forward-biased junction diodes as electrically-controllable resistors to give 60-dB range of attenuation. Balanced configuration suppresses second harmonic generation and reduces pulse feedthrough during pulse modulation.



**Fig. 10.** Amplitude stability and warm-up characteristics are shown by this recording of output level versus time from cold start. Output level was set to 0-dBm range.

But for best leveling at lower frequencies, the capacitor must hold its charge from one RF cycle to the next. Otherwise the resulting sawtooth would distort the output. Clearly a compromise must be made between the AM and leveling capabilities. The decision was to maximize AM bandwidth in the carrier range 8 MHz to 512 MHz, then reduce it by a factor of 2 at 8 MHz and again at 2 MHz to maintain leveling.

#### Pulse Modulation

In pulse modulation the RF detector operates in a sample-and-hold mode. As the pulse is applied the RF output, normally held off, is switched on to whatever level results from the previous sample's charge on the hold capacitor. Any correction required by the dc reference signal then is imposed through the normal action of the ALC loop. Also, the meter then reads peak pulsed RF power. A certain minimum pulse width is of course necessary to achieve this action, and there are limits on how long the sample can be held without an appreciable error in peak RF level. Thus the specifications include limits on rate and width.

Because the RF detector becomes back-biased when the RF level setting is reduced quickly, one would expect the correction to desired amplitude to be slow. This effect has been prevented with circuits that detect a preset value of error between reference and feedback signals at the summing junction of the ALC amplifier. When that value is exceeded the hold function of the detector is partially disabled, until the error falls below its preset limit plus a short fixed time thereafter. Thus the hold capacitor is made to discharge rapidly, giving prompt response to reductions in the output level vernier.

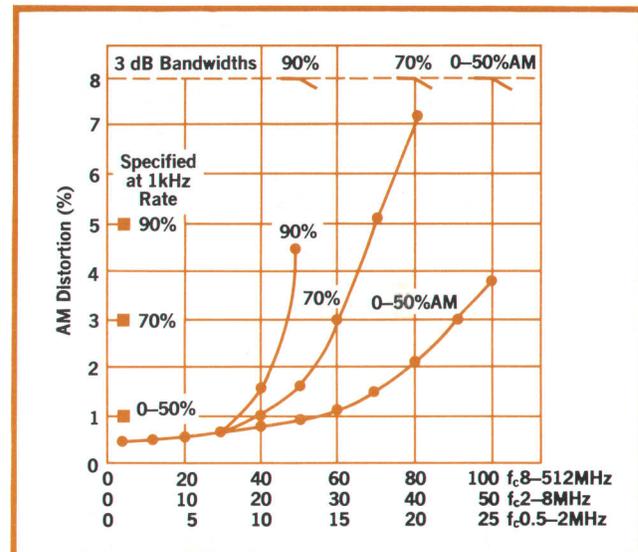
To drive the modulator, built-in circuits generate pulses of controlled rise and fall time. This minimizes the envelope distortions and ringing that

would be expected from those low-pass filters that are in the circuit to remove RF harmonics. The filters' bandwidth imposes some limits on risetime and pulse width, but circuits to be tested in the generator's frequency range would be expected to have bandwidths less than that imposed by the filters. If faster risetimes are required, an external balanced mixer can be used as a fast switch.

The pulse-forming circuits also make it possible to obtain pulsed outputs with sinewave drive.

#### Metering Modulation

Like all signal generators, the Model 8640A/B is an open-loop system designed to deliver a known amount of modulation, AM or FM, for a given modulating voltage input. It has a meter that reads the applied voltage and that thus implies the level of modulation.



**Fig. 11.** AM distortion as function of AM rate measured on 200-MHz carrier at +13 dBm level, representative of all frequency bands.

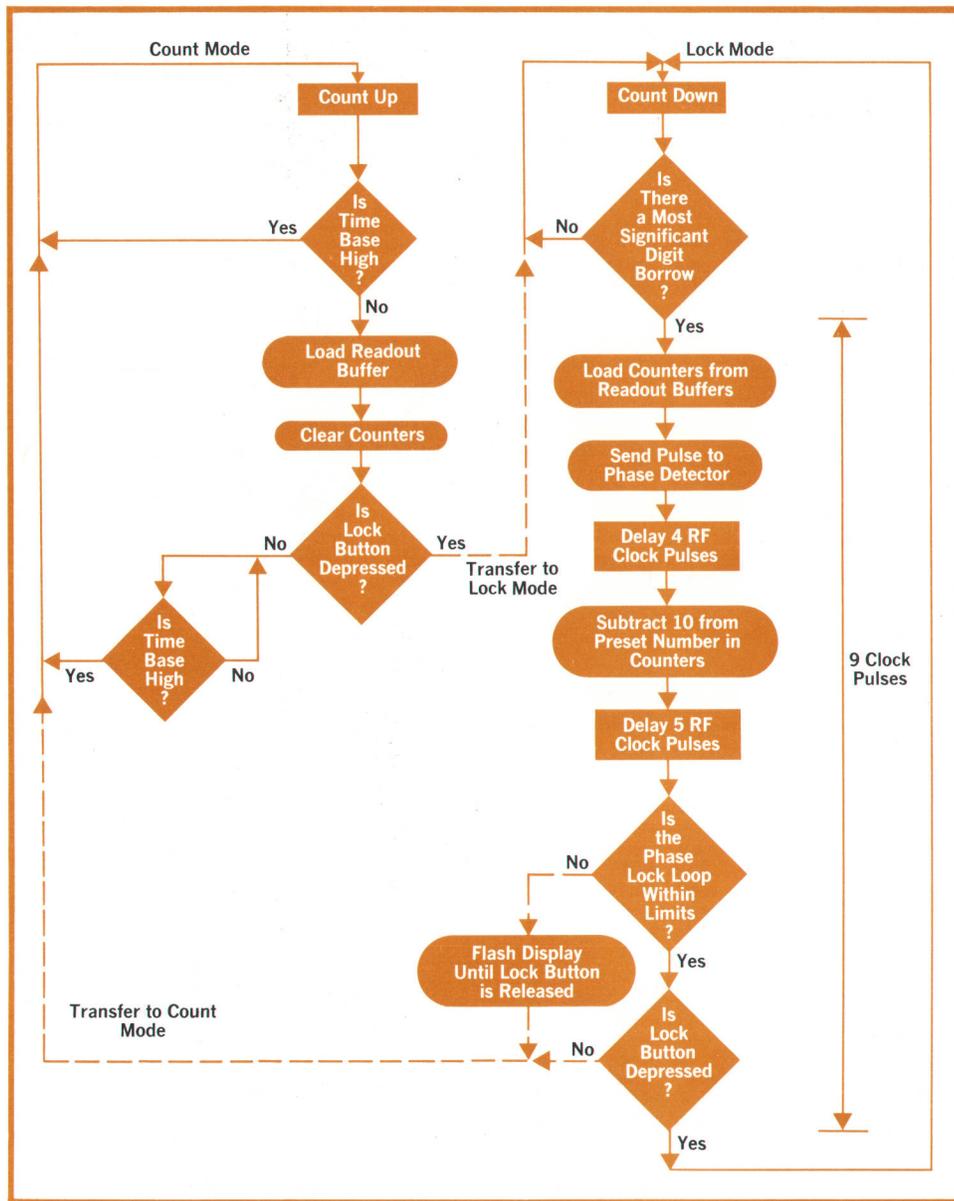


Fig. 12. Flow diagram illustrates control of counter during operation in phase-lock mode. Normally, counter operates in count mode to measure output frequency but when "Lock" button is depressed control goes into lock mode. Instrument then retains count in readout buffer, and it switches counting circuits to count down.

Even with careful meter detector design, and using meters of 1%-of-full-scale tracking error, total error can be 3 to 4% of reading. So the new generator's AM and FM systems are calibrated at the external input terminals. With either vernier at maximum, one volt peak produces 100% AM, or whatever peak FM deviation is selected. An external DVM thus may be used to indicate modulation with greater accuracy.

FM can be calibrated at any particular output frequency by switching the FM mode switch to the CAL position. This applies a very accurate internal 1-volt signal to the FM input. The operator then adjusts the FM vernier to give the exact frequency shift desired on the digital display of the Model 8640B, or on a counter connected to the Model 8640A's rear-panel auxiliary output. This combina-

tion of dc and FM vernier can also be used as an electrical fine tune.

During pulse modulation, the meter remains a valid measure of peak pulse value down to a low pulse rate; rates too low are sensed by a rate detector that automatically disables the meter to alert the user that an out-of-spec error in output level may be present. No check is provided for too-narrow pulses.

#### Signal Generator Performance—Synthesizer Stability

The B version of the Model 8640 can lock its RF output frequency to an internal or external crystal reference, to reduce drift. It also contains a built-in counter that can display output frequency (the counter can also be used to measure external signal frequencies up to 550 MHz).

RF is first pre-scaled by a factor of 64, providing a signal in the range of 4 - 8 MHz for the counter circuits. The gate signal to control counting is derived from a 5-MHz reference, which may be the built-in crystal or an external oscillator. Programmable counters in the time base chain, under the control of range and expand buttons, divide that frequency by a factor that produces a six-digit display resolution of at least 1 part in  $10^4$  in the unexpanded mode; expand buttons lengthen the gate time to increase resolution by 10 or 100 times. A front-panel annunciator indicates any overflow that may result from use of the expand modes.

To lock the signal generator to the 5-MHz reference, and thereby achieve synthesizer stability, the counter is caused to act as a self-programmed  $\div N$  frequency synthesizer (Fig. 12).

When the lock button is pressed, the contents of the readout buffer store, at the end of the count cycle, are held. This number is then preset into the counters, which have been switched into count-down configuration. The 4 - 8 MHz signal derived from the RF counts this preset number down to zero. Now the number still held in the readout buffer is again set into the counters, and the process repeats. Each time the stored number is preset into the counters, a pulse is sent to one input of the

phase-frequency detector; its other input is the time-base signal, which originally determined the counting period for the preset number. A dc voltage proportional to the phase difference between the two signals is produced, and this voltage is summed into the FM circuits of the oscillator to stabilize its frequency. The system thus formed is a programmable divide-by-M-and-N phase-lock loop, where M is the time base divide number and N is 64 (prescaler number) times the readout number, or

$$f_{osc} = \frac{N}{M} \times 5 \text{ MHz.}$$

Actually, it is the leaving of the zero state that initiates a pulse to the phase-frequency detector, and the counter input is disabled for 9 more clock pulses to allow time to preset the counters. To correct, a pulse is injected into the second-least significant counter decade, having the effect of subtracting 10 from the preset number.

Lock is possible either in normal or X10 expand mode, but not in X100.

Should the oscillator drift out of the hold-in range of the lock system, the instrument automatically returns to the count mode and signals this condition by flashing the display. The same thing happens if lock is attempted in the X100 mode. Re-locking requires only that the lock button be released, tuning

## ABBREVIATED SPECIFICATIONS

### Models 8640A and 8640B Signal Generators

(Unless otherwise noted, specifications apply within nominal frequency bands and over top 10-dB range of Output Level vernier.)

#### Frequency Characteristics

**RANGE:** 500 kHz to 512 MHz in 10 octave bands (to 1024 MHz with External Frequency Doubler).

**BAND OVERLAP:** Bands extend 10% below (e.g., down to 450 kHz) and 7% above nominal frequency bands (e.g., up to 550 MHz).

**FINE TUNING:** >200 ppm. In locked mode (8640B):  $\pm 20$  ppm by varying internal time base vernier.

#### ACCURACY:

8640A, mechanical dial: better than 0.5%. Resettability is better than 0.1%.

8640B, 6-digit numerical display with X10 and X100 expand: depends on internal or external reference used (internal crystal aging rate: <2 ppm/year).

#### STABILITY:

	Normal	Locked (8640B)
Time (after 2-hr warm-up)	<10 ppm/10 min	<0.05 ppm/hr
Temperature (15 to 35°C ambient)	<50 ppm/°C	<2 ppm total
Line voltage (+5% to -10%)	<1 ppm	<0.1 ppm
Load (open to short)	<1 ppm	None
Output level (10 dB change on output vernier)	<1 ppm	None
Mode change (CW to FM)	100 Hz or <0.5% of selected peak deviation, whichever is greater	None

#### RESTALLIZATION TIME:

	Normal	Locked (8640B)
After frequency change	<15 min	None after relocking
After band change	None	
After 1 min in RF OFF mode	<10 min	

#### Spectral Purity

RESIDUALS (average rms value):

	Post-detection bandwidth of 300 Hz to 3 kHz	Post-detection bandwidth of 20 Hz to 15 kHz
RESIDUAL AM:	>85 dB down	>78 dB down
RESIDUAL FM (230 to 550 MHz CW and up to 1/8 max allowable peak deviation)	<5 Hz	<15 Hz
Up to max allowable peak deviation	<15 Hz	<30 Hz
Residual FM decreases by 1/2 for each frequency range down from 230-to-550 MHz range until reaching noise floor.		
NOISE FLOOR	1 Hz	4 Hz

#### HARMONICS (at 1 volt output and below):

>35 dB below fundamental of 0.5 to 128 MHz.  
>30 dB below fundamental of 128 to 512 MHz.

**SUBHARMONICS and NON-HARMONIC SPUROUS** (excluding those within 15 kHz of carrier whose effects are specified under residual AM and FM):

8640A: None detectable; 8640B: >100 dB below carrier.

**NOISE** (averaged rms level stated in a 1-Hz bandwidth 20 kHz from carrier on one side).

On 256-512 MHz range, >130 dB below carrier from 230 to 450 MHz increasing linearly to >122 dB down at 550 MHz. On lower ranges, decreases 6 dB per range until reaching SSB broadband noise floor of >140 dB.

#### Output Characteristics

**RANGE:** continuous from -145 to +19 dBm (0.013  $\mu$ V to 2 V) into 50  $\Omega$ .

#### LEVEL ACCURACY

	Using top 10 dB of vernier range		Using full vernier range	
Output level (dB)	+19 to -7	-7 to -47	-47 to -137	-137 to -145
Accuracy, including meter reading (dB)	$\pm 1.5$	$\pm 2.0$	$\pm 2.5$	$\pm 3$

**LEVEL FLATNESS:**  $\pm 0.5$  dB from 0.5 to 512 MHz referred to output at 50 MHz.

**IMPEDANCE:** 50  $\Omega$ . <1.3 VSWR on 0.5 V and lower ranges; <2.0 VSWR on 1 and 2 V ranges.

**AUXILIARY OUTPUT:** Rear-panel BNC output, > -5 dBm into 50  $\Omega$  from 500  $\Omega$  source impedance.

#### Modulation Characteristics

**TYPES:** Internal AM and FM, external AM, FM, and Pulse. Capable of simultaneous AM and FM or Pulse and FM.

#### AMPLITUDE MODULATION:

DEPTH: 0 to 100% (up to +13 dBm output level).

LOWER MODULATING FREQUENCY LIMIT: DC or 20 Hz (switch-selected).

UPPER MODULATING FREQUENCY LIMIT:

Carrier Frequency	0 to 50% AM	70% AM	90% AM
0.5-2 MHz	25 kHz	20 kHz	12.5 kHz
2-8 MHz	50 kHz	40 kHz	25 kHz
8-512 MHz	100 kHz	80 kHz	50 kHz

AM DISTORTION (at 400 Hz or 1 kHz):

	0.5-512 MHz	<1%	<3%	<5%
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EXTERNAL AM SENSITIVITY: 0.1% AM per mV peak with  $\pm 5\%$  accuracy at 400 Hz and 1 kHz for 0 to 90% AM (input Z=600  $\Omega$ ).

INDICATED ACCURACY:  $\pm 8\%$  of reading on 0-100 scale of front-panel meter,  $\pm 9\%$  on 0-3 scale.

PEAK INCIDENTAL PM (at 30% AM): <0.15 radians from 0.5 to 128 MHz; <0.3 radians from 128 to 512 MHz.

PEAK INCIDENTAL FM: Equals PEAK INCIDENTAL PM  $\times$  MODULATING FREQUENCY.

#### PULSE MODULATION:

ON-OFF RATIO (at maximum vernier): >40 dB.

PEAK INPUT REQUIRED: >1 V above ground into 50  $\Omega$ , sinewave or pulse; 5 V maximum. (Input Z=50  $\Omega$ .)

#### PULSE CHARACTERISTICS

Carrier frequency (MHz)	0.5-1	1-2	2-4	4-8	8-32	32-512
Rise and fall times ( $\mu$ s)	<9	<4	<2	<1.5	<1	<1
Repetition rate	50 Hz to 50 kHz	50 Hz to 100 kHz	50 Hz to 250 kHz	50 Hz to 500 kHz	50 Hz to 500 kHz	50 Hz to 500 kHz
Minimum width*	10 $\mu$ s	5 $\mu$ s	2 $\mu$ s	1 $\mu$ s		

\*For level accuracy within 1 dB of CW.

#### FREQUENCY MODULATION:

DEVIATION: Maximum allowable equals 1% of lowest frequency of each band (e.g., 160 kHz on 16-32 MHz band).

#### MODULATING FREQUENCY LIMITS:

DC or 20 Hz (switch selected) and 250 kHz. With 8640B in locked mode, lower limit is 50 Hz.

DISTORTION: <1% for deviations up to 1/8 maximum allowable; <3% for maximum allowable deviations.

EXTERNAL FM SENSITIVITY: 1 V peak yields maximum deviation selected on Peak Deviation switch with  $\pm 5\%$  accuracy (FM vernier full clockwise).

INDICATED ACCURACY:  $\pm 10\%$  of front-panel meter reading.

INCIDENTAL AM (at 400 Hz and 1 kHz rates): <0.5% AM for FM up to 1/8 max. allowable deviation; <1% AM for FM at maximum allowable deviation.

#### INTERNAL MODULATION SOURCE:

FREQUENCY: 400 Hz and 1 kHz ( $\pm 2\%$ ) fixed.

OUTPUT LEVEL, at front panel: 10 mV to 1 V (independently adjustable with  $\pm 20\%$  accuracy).

OPTIONAL VARIABLE SOURCE: 20 Hz to 600 kHz ( $\pm 10\%$ ), continuously variable in 5 decade bands, plus fixed 400 Hz and 1 kHz. Output to front panel independently adjustable from 20 mV to 3 V.

#### Counter Characteristics

##### EXTERNAL RF INPUT:

FREQUENCY RANGE: 20 Hz to 550 MHz

SENSITIVITY:  $\geq 100$  mV rms into 50  $\Omega$

EXTERNAL REFERENCE INPUT: 5 MHz, 0.2-5 V into 1000  $\Omega$

##### INTERNAL REFERENCE

Accuracy: Better than  $\pm 1$  ppm, 15 to 35°C.

Drift rate: <0.05 ppm over any hour; >2 ppm per year.

##### General

POWER: 100, 120, 220, and 240 V, +5%, -10%, 48 to 440 Hz, 175 VA max.

WEIGHT: 45 lb (20, 4 kg).

DIMENSIONS: 16% in W x 5% in H x 18% in D (425x140x478 mm).

OPERATING TEMPERATURE RANGE: 0 to 55°C.

PRICES IN USA: 8640A: \$3100, 8640B: \$4450.

Option 001 (internal variable audio oscillator): \$150.

readjusted to the desired frequency, and the button again pressed.

### FM While Phase-Locked

FM is possible, *while phase locked*, down to a rate of 50 Hz, with no constraints on deviation. This gives crystal accuracy and stability to the carrier during FM, an especially important consideration when testing narrowband, crystal-controlled receivers. This results from the use of a phase-lock loop bandwidth of 5 Hz maximum. The loop uses the integral of the phase error to control the oscillator, so there not only is no frequency offset but also no long-term average phase offset. Thus two Model 8640B Generators locked to a common reference will be phase-coherent on a long-term average basis.

To allow for continuous locked coverage of all frequencies, including those not related to 5 MHz in an M/N ratio, pulling capability is provided for the crystal reference oscillator over a  $\pm 20$  ppm range. The reference can be switched out of calibration and subjected to voltage control with a front-panel knob. A light denotes uncalibrated operation.

Refinements in the loop circuits include an active elliptic filter to remove any sampling frequency that may result from imbalance in the nulling type phase detector. There is no degradation in specified residual FM from normal to locked mode. For quick response to large errors, resulting from such loop transients as those generated when changing voltage to the VCXO, a speedup circuit follows the phase detector.

### Acknowledgments

Many more people than can possibly be listed here have made the Model 8640A/B possible, as it was truly the result of a substantial group effort. All should feel proud of their accomplishments. The principal design engineers, other than the authors, were Jim Harmon, Howard Swain and Ed Taylor (electrical), and Bill Bull, Bob DeVries and Gary Wey (mechanical). Dan Derby was responsible for the industrial design, Bill Boller and Bob Guisto for the interface to production tooling. A special thanks to the production team, who made much contribution in the late prototype and early production stages. 🍷



**Kenneth L. Astrof** (LEFT to RIGHT)

Ken Astrof graduated in 1964 from Queens University, Kingston, Ontario, with a BSc (EE) whereupon he went to work for a Montreal communications firm designing microwave feed systems for satellite ground stations. The work/study programs available at American firms lured him south in 1966, however, where he joined HP and obtained his MSEE degree at Santa Clara University four years later under the HP Honors Co-op program.

At HP, Ken worked on S-parameter test sets, Network Analyzers, and on the leveling and amplitude modulation portions of the 8640A/B Signal Generator. A long-time camper, Ken also finds activities closer at home with his family, which includes three young kids, where he gardens and makes furniture.

### Larry C. Sanders

On earning a BS degree in physics from Utah State University in 1961, Larry Sanders went to work for the Stanford Radio Science Lab, studying "whistlers" on a research vessel in Antarctic waters. A year and a half later

he returned for graduate study, earning his MSEE degree at Brigham Young University in 1966. He then joined Bell Labs in Holmdel, N. J.

A westerner at heart, Larry came to HP in 1970 going to work on mixers and filters for spectrum analyzers and then on to the oscillator and FM portions of the 8640A/B Signal Generators. Larry's spare time activities include photography, woodworking and hi-fi construction. He and his wife have four children, ages 1 to 7.

### Michael S. Marzalek

A Phi Beta Kappa from the University of California at Berkeley (BSEE, 1969), Mike Marzalek joined HP the year of his graduation, going right to work on the digital control portion of the 8660-series Synthesized Signal Generators, and then on to the Model 8640B Signal Generator. Meanwhile, he has completed course work for an MSEE at Stanford under the HP Honors Co-op program.

Mike finds time to devote to folk guitar and to back-packing and also to working with his brother in radio-controlled model sailplane competitions.

### Raymond M. Shannon

Ray Shannon has spent most of his professional life synthesizing frequencies, starting at a midwest company designing for military communication systems and moving to HP six years later where his initial projects were special versions of the 5100-series Synthesizers. Subsequently, he contributed to the 8660-series Synthesized Signal Generators before moving on to the 8640A/B program as Project Manager. Ray, who is now Section Manager for signal generators, holds a BSEE degree from the University of Cincinnati (1959).

Ray plays the piano, does choral singing, paints and does woodcarving. Outdoors, he likes tent-camping with his family, which includes three youngsters, 6 to 13.

# Computer-Aided Design of Modular Power Supplies

*A universal circuit and a computer program—these make it possible to obtain fixed-voltage, modular power supplies in a wide range of output ratings at low cost, but with laboratory-grade performance and reliable operation assured.*

**By Willis C. Pierce, Jr., James S. Gallo,  
and William T. Walker**

**J**UST ABOUT EVERY ELECTRONICS ENGINEER, it seems, has had to put together a power supply at one time or another—usually as an afterthought.

But these afterthoughts are getting harder to do. Many of today's circuits require a high order of regulation from a power supply. Reliable operation under all conditions of temperature and line voltage is obligatory. To protect sensitive circuits, current limiting and overvoltage protection must be designed in and the power supply itself must be protected from line transients, short-circuited outputs, and other accidents of the external world.

More and more, special know-how is needed to obtain a design that meets these requirements. The designer must make sure that the regulator control loop is stable under all conditions. He must anticipate worst-case conditions and, to obtain maximum reliability without resorting to expensive overdesign, verify that all components are always operated conservatively.

So why do circuit designers continue to reinvent the wheel, so to speak? The main reason is efficiency by optimizing the design to supply a particular current level at one voltage. To meet this requirement in production units, manufacturers are offering a growing number of modular power supplies—units that have the good regulation, reliability, and other attributes of a high-quality lab supply, but that are designed for a narrow range of voltages. Where there is a match between circuit requirements and power-supply capability, these provide an economical means of powering circuits reliably.

Meeting every individual requirement with an optimized design, however, has not been easy to do at low cost. For reliable operation, each rating requires an individual design. Modifying one design to

achieve a different rating is not a satisfactory solution because it often results in some components operating at elevated temperatures with consequent loss of reliability.

## **Computer-Generated Modular Supplies**

The use of a computer in the design phase is now changing this situation. With computer-aided design it is possible to obtain any output rating within a wide range at low cost, but with high-quality performance assured.

A new series of modular power supplies has been designed with this technique. Initially, 44 different ratings are offered (see table, P. 16). These meet the most asked-for voltage-current combinations but the design approach makes it possible to react quickly and economically to requests for special voltage and/or current ratings with no sacrifice in performance or reliability.

The design approach is based on a circuit configuration that can be used for voltages as high as 150 volts or as low as 1 volt and with output power up to 200 W. The basic circuit uses a series regulator. Though not as efficient as other types of regulators, it gives better performance. Supplies in this new line have lab quality performance—0.01% regulation, 8-hour stability of 0.1%, ripple and noise less than 2 mV peak-to-peak, a temperature coefficient of less than 0.01% °C, and load transient recovery within 50 $\mu$ s (full load to half load). Furthermore, conservative operation of all components is assured.

## **Four Packages**

In working out the basic design, it was realized that more than one mechanical design would be needed to handle the wide range of power levels



**Fig. 1.** New family of fixed-voltage, modular power supplies are in packages that are  $\frac{1}{8}$ ,  $\frac{1}{4}$ , or  $\frac{1}{2}$  of standard rack width depending on output power capability needed.

expected. The new series (Fig. 1) has four different packages (two of the packages are the same size but differ in output power ratings and in details of the internal layout). Using four packages allows standard voltage ratings to be offered with four current ratings in a 1, 2, 4, 8 ratio.

### Design Considerations

One of the design goals was to use identical circuit components wherever possible so design variables could be held to a minimum and also to reduce the parts inventory. This led to a reexamination of the series regulator circuit.

Usually, a series regulator is inserted in the positive leg of the supply, as shown in Fig. 2a, with the emitter driving the output (NPN silicon power transistors have proved to be the best choice for series regulator service). This configuration requires the reference supply to provide drive current for the regulator, which would mean a unique reference circuit for each current rating.

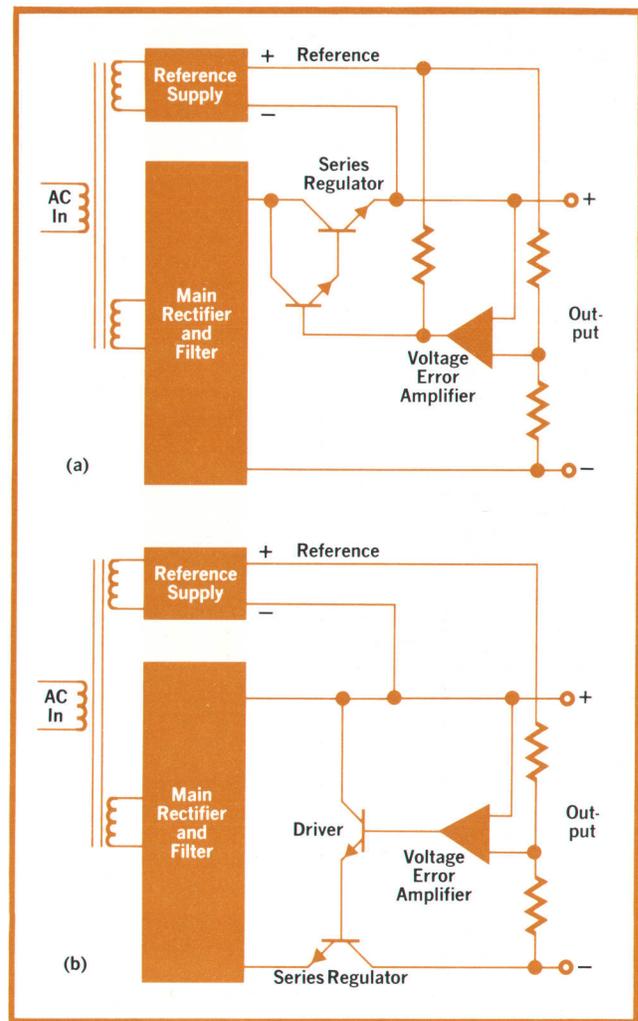
For the new design, the series regulator is in the negative leg, with the collector driving the output, as shown in Fig. 2b. Drive current can then be provided from the unregulated dc. Thus, the same reference circuits can be used for all members of this family.

This configuration has the further virtue of reducing the required rectifier voltage over that required by the Darlington configuration of Fig. 2a, thus reducing the power dissipation in the series regulator.

### The Transformer

For efficient use of space, the power transformer should not be any larger than needed to handle the selected power level. With four package sizes, four transformer sizes can be used. Since the power consumption within each package size will not differ substantially, the primary windings and the Faraday

shield for each transformer size can be the same for all ratings supplied in that package. In the interests of maximum efficiency, however, the main second-



**Fig. 2.** Conventional series regulator (a) is in positive leg of supply. New modular supplies place series regulator in negative leg (b) so reference circuit need not supply regulator drive current.

## New family of modular power supplies

Model*	Output Voltage Range (volts)	Maximum Output Current (amperes) at 50°C			
		A-suffix Models (1/8 width)	C-suffix Models (1/4 width)	E-suffix Models (1/4 width)	G-suffix Models (1/2 width)
62003-	3 ± 0.5	2	4.25	8.5	17
62004-	4 ± 0.5	2	4	8	16
62005-	5 ± 0.5	2	4	8	16
62006-	6 ± 0.5	1.75	3.75	7.5	15
62010-	10 ± 0.5	1.5	3.25	6.5	13
62012-	12 ± 0.6	1.5	3	6	12
62015-	15 ± 0.75	1.25	2.5	5	10
62018-	18 ± 0.9	1	2.25	4.5	9
62024-	24 ± 1.2	0.75	1.75	3.75	7.5
62028-	28 ± 1.4	0.7	1.5	3.25	6.5
62048-	48 ± 2.4	0.45	1	2	4

\* Complete model number includes letter suffix; e. g., Model 62003A (output: 3V @ 2A).

ary differs for each voltage rating. The secondary voltage is made as low as possible to keep power dissipation at a minimum. Towards this end, it is selected to provide just enough voltage to keep the series regulator from saturating under worst-case conditions.

Power for the reference circuit and the comparator amplifiers is provided by a separate winding on the power transformer. This provides better regulation for the reference supply than would supplying it from the main rectifiers, and it also ensures that the reference and the comparators remain energized in the event that some accident shorts the output. Furthermore, it allows a standardized 6.2V reference to be used for all supplies, even those that have outputs of less than 6 volts.

What else can be made identical for all members of this family? By designing the regulator drivers to require an input of no more than 1V @ 5 mA, a high-gain, low-drift IC can be used as the voltage comparator amplifier and the same type can be used for all units. The same can be said for the current comparator.

### Enter the Computer

Several calculations involved in the design of a power supply are the same for a wide range of voltage and current ratings—only the numbers differ. But plugging in numbers is not enough—careful attention must be paid to the thermal characteristics of the supply, not only to ensure safe semiconductor temperatures, but to make sure that capacitors, transformers, printed circuit boards, and wire insulation are not subject to excessive heating. To handle all these variables on a repetitive basis, an interactive computer program of 500 statements was written in BASIC for use on the HP Model 2000C Timeshare System.

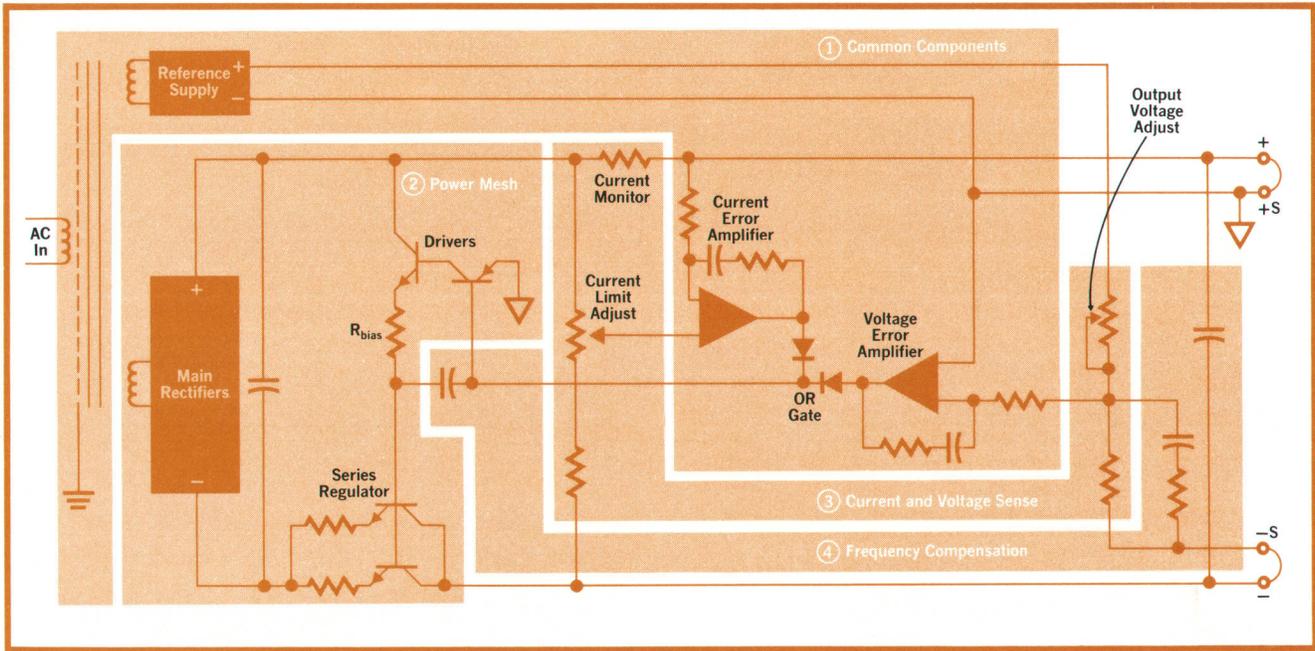
Here is how the computer is used (see box on opposite page). Equations are programmed to evaluate

worst-case tolerance, temperature, and operating conditions from which the computer program generates the optimum value for a part. Since the optimum value may not be standard, the program asks the engineer to select a value from the list of parts available, bearing in mind the mechanical requirements of the printed circuit board used in the selected package (the circuit board for each package was planned to allow for the varying sizes of parts that different ratings may call for). The computer then evaluates performance with this part. These steps may be repeated until a good match is found, but the final choice is always left to the designer.

### The Circuit

The basic circuit is shown in Fig. 3. Those parts that are common to all versions of the design are contained in the area marked ①. Not shown are the diodes that protect the regulator and other circuits from reverse currents accidentally caused by active loads or by other power supplies in a system. Also not shown is an optional crowbar circuit that shorts the output in case an accident raises the output voltage above nominal. The basic design also includes a thermostat mounted on the heat sink to open the source line in case of excessive temperatures.

At the start of a design, the designer tells the computer what the desired voltage and current ratings are. The computer checks these values against package capabilities, as shown by the chart of Fig. 4, and then recommends a package size. The computer also specifies the voltage of the transformer main secondary winding and the breakdown voltage ratings for the rectifier and filter capacitor. It determines peak and rms ripple currents and calculates the minimum filter capacitance needed to hold ripple of the unregulated dc below a specified design value under conditions of full load and low line at 50 Hz.



**Fig. 3.** Universal circuit can be used for wide range of voltage-current ratings. Circuits in area ① are standardized for all versions. Computer helps designer select parts in other areas to achieve efficient design.

The designer then selects a regulator transistor and the number of them he thinks he'll need, using past experience as a guide. He also enters in the rated minimum collector-to-emitter operating voltage, the dc current gain, and the thermal resistance (junction to heat sink) of the type selected.

Since the operating point of a regulator transistor varies with current, so does the power dissipation and the junction temperature. The computer has an

accurate thermal model of each package, so it can determine maximum junction temperature and present it to the designer to show whether or not the temperature would ever be excessive (although the regulator transistors are rated for operation up to 200°C, thermal fatigue is reduced and reliability enhanced by operating the transistors at lower temperatures).

The designer also selects the driver transistor,

Portion of program illustrates interactive nature of computer-aided power supply design. Design example involves 30V supply with maximum output of 1.5A. Section here establishes thermal environment of driver Q3. Up to this point, package size (type C), rectifiers, main filter capacitors, and series regulators have been chosen.

As in previous steps, computer asks, "which calculation?" Designer answers with #5 (step 1). Computer confirms that this calculates worst-case conditions for driver Q3 and it then instructs designer to enter temperature (TA) of air inside power supply. Based on previous experience, he enters 66°C (step 2). Computer then scans surface corresponding to junction temperature and determines that worst case occurs when load draws 0.87 A (step 3). Maximum Q3 dissipation would then be 0.65 W.

It was previously determined that Q3 would be in TO-5 package mounted on circuit board, which gives thermal resistance of 175°C/W from junction to air for this transistor. This results in junction temperature of 180.7°C (step 4). Computer then asks, "shall we go on?" Designer responds with "no," so computer asks for new value of thermal resistance (step 5). Designer decides to add top-hat radiator

to Q3, which gives thermal resistance of 115°C/W. Program then repeats steps 2, 3 and 4, determining that maximum junction temperature would be 141.3°C. This is acceptable so designer says yes when computer asks "continue?"

```

-----
1- CALCULATION #75
  CALCULATES WORST CASE PD & TJ OF DRIVER-Q3
2- ENTER TA(INSIDE)
  766
  WORST CASE CONDITIONS FOR DRIVER-Q3:
3- ILOAD= .87      AMPS      BETA OF Q4= 54
  MAX PD= .65     WATTS
  DRIVER-Q3 OFF HEAT SINK
4- TJMAX= 180.7   DEGREES C FOR OJA= 175  DEGREES C/WAIT
  CONTINUE?NO
5- ENTER Q3 PAR: OJA
  7115
  ENTER TA(INSIDE)
  766
  WORST CASE CONDITIONS FOR DRIVER-Q3:
2,3,4 Repeat ILOAD= .87      AMPS      BETA OF Q4= 54
  MAX PD= .65     WATTS
  DRIVER-Q3 OFF HEAT SINK
  TJMAX= 141.3   DEGREES C FOR OJA= 115  DEGREES C/WAIT
  CONTINUE?YES
-----
  CALCULATION #?

```

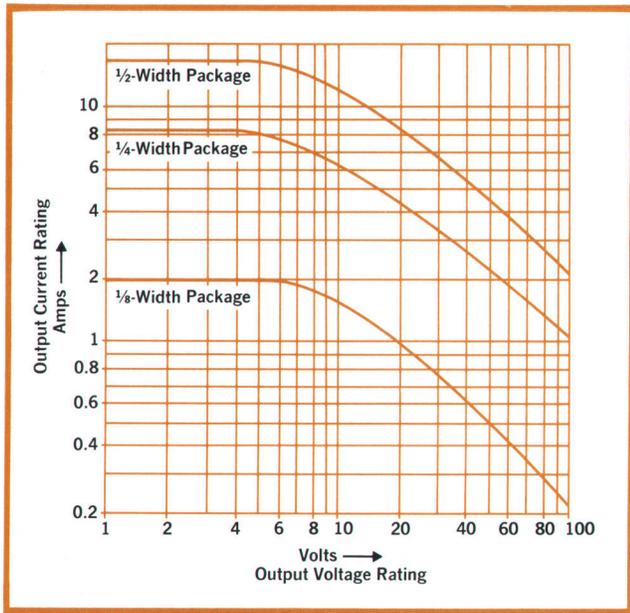


Fig. 4. Output voltage-current rating determines package size.

entering in the appropriate parameters. The computer selects a value for the driver bias resistor. Power dissipation and junction temperature in the NPN driver both can be described in terms of a surface that varies in two dimensions with power supply output load current and regulator current-gain increments. This is because the operating point of the NPN driver depends on both of these parameters. Similarly the operating point of the PNP driver

(used to provide more gain, shift the dc level of the error amplifier output, and translate the amplifier voltage output to a current) depends on the output current, the regulator gain, and the NPN driver gain. The program scans all these surfaces for the worst-case junction temperatures and presents them to the operator. If he finds that any exceed  $150^{\circ}\text{C}$ , he has the option of changing the design and re-evaluating.

When the designer is satisfied with the results, the design of the power mesh, region ② in Fig. 3, is complete.

#### Current and Voltage Levels

Next the computer selects the resistors for over-current sensing (region ③). These must ensure that the current-limit amplifier takes control of the drivers when the current goes above 103% of rated output, and that the current cuts back to 10% of rated output under short-circuit conditions. This limits the dissipation of the series regulator by reducing the current as the voltage drop across the regulator increases during overload conditions. The regulator may thus be designed for efficient operation at the nominal output voltage, rather than have the excess power capability needed to handle short-circuit conditions at maximum rated current.

Again, the computer recommends specific values, the designer selects available values and enters them into the program. The computer tests these values, taking account of the tolerances allowed for these parts so that every production unit with this design will cut back to the proper current level.

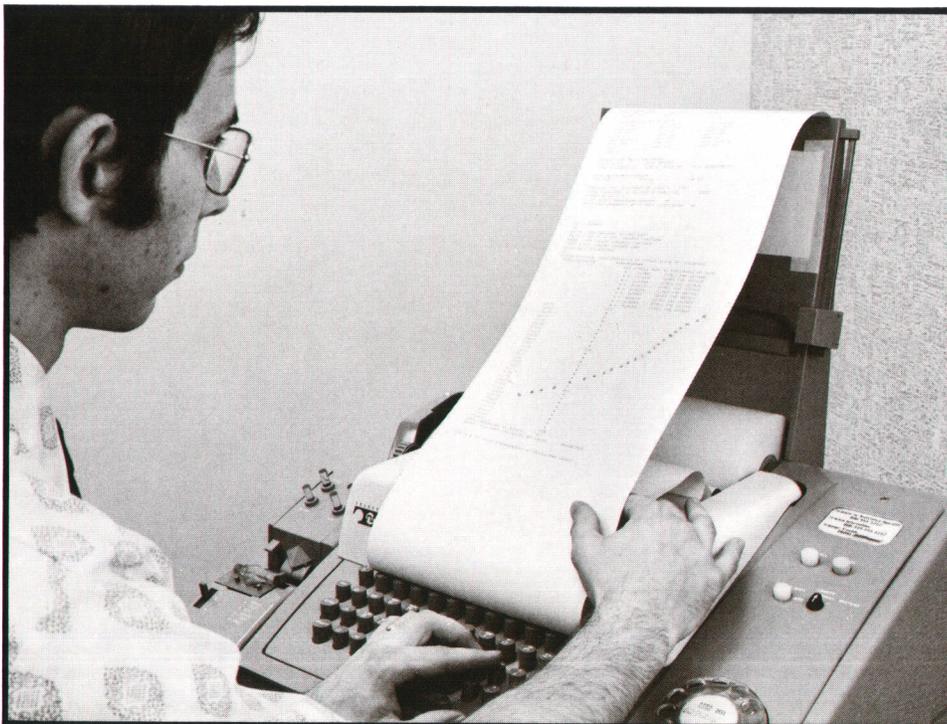


Fig. 5. Computer calculates and plots open-loop gain of voltage-control loop for designer (frequency axis is vertical with origin at top).

The computer then selects the resistors for the voltage programming string with the goal of providing a  $\pm 5\%$  range of adjustment, or at least  $\pm 0.5$  volts, while maintaining the temperature coefficient within the  $0.01\%/^{\circ}\text{C}$  specification. If the supply is to have the optional crowbar, the computer selects the resistors for the crowbar trip level, making sure that allowable tolerances on parts do not cause the minimum and maximum levels to go outside a narrow range.

### Stability

Finally, the computer asks the designer to enter the ac parameters of the transistors, and to enter values for the capacitors that affect ac performance, shown in region ④ of Fig. 3. The program then calculates and plots the magnitude of the open-loop gain of the voltage-control loop from 1 kHz to 1 MHz, and it calculates the frequency of gain crossover, as shown in Fig. 5. This allows the designer to make adjustments in the values of the capacitors to get the desired response.

### Time-saver

All of this took about one hour of the designer's time. He can then quickly assemble a prototype to verify that performance is as predicted.

Using this approach, the 44 power supplies in the standard series were designed within the engineering time required for two or three supplies by the conventional one-at-a-time approach. Supplies with special ratings can be designed and produced with the same exacting criteria as standard models but without costly engineering charges. The computer can also generate other pertinent information, such as a derating curve for ambient temperatures above

## SPECIFICATIONS

### HP Model 62000-Series Modular Power Supplies

**DC OUTPUT** (See Table, Page 16).

**DC OUTPUT ISOLATION:** Output is isolated, either output terminal may be grounded.

**LOAD REGULATION:** Change in output voltage is less than  $0.01\%$  or 1 mV, whichever is greater, for change from no load to maximum rated load.

**LINE REGULATION:** Change in output voltage is less than  $0.01\%$  or 1 mV, whichever is greater, for input line voltage change from 104 to 127 V.

**RIPPLE AND NOISE:** Residual ac voltage on dc output is less than 1 mV rms or 2 mV p-p (up to 20 MHz) for any line or load condition within ratings.

**TEMPERATURE COEFFICIENT:** Less than  $0.01\%/^{\circ}\text{C}$  change in output over temperature range of 0 to  $50^{\circ}\text{C}$  with constant load and ac line voltage after 30-minute warm-up.

**OPERATING TEMPERATURE:** 0 to  $50^{\circ}\text{C}$  ambient. Operation to  $71^{\circ}\text{C}$  possible with appropriate derating.

**COOLING:** Convection cooled.

**STABILITY:** Total drift over 8-hour period (following 30-minute warm-up) is less than 0.1% of output under conditions of constant line, load, and ambient temperature.

**LOAD TRANSIENT RECOVERY:** Recovers in less than 50  $\mu\text{s}$  to within 15 mV of nominal output following load change from full load to half load or vice versa.

**INPUT VOLTAGE:** 104–127 Vac, 48–63 Hz single phase. Other line voltages available.

**INPUT POWER** (varies within each series according to output ratings):

A-suffix models: 31 to 47 W.

E-suffix models: 143 to 198 W.

C-suffix models: 74 to 100 W.

G-suffix models: 277 to 384 W.

### MECHANICAL:

MODELS	PACKAGE	DIMENSIONS	WEIGHT
A-suffix	1/8 width	1.91 in W x 5.03 in H x 12.25 in D 48 x 128 x 311 mm.	6 lb 2,7 kg
C-suffix	1/4 width	3.94 in W x 5.03 in H x 12.25 in D 100 x 128 x 311 mm.	10 lb 4,5 kg
E-suffix	1/4 width	3.94 in W x 5.03 in H x 12.25 in D 100 x 128 x 311 mm.	13 lb 5,9 kg
G-suffix	1/2 width	8.11 in W x 5.03 in H x 11.50 in D 206 x 128 x 292 mm.	21 lb 9,5 kg

### PRICES IN U.S.A.:

A-suffix models: \$89.

E-suffix models: \$145.

C-suffix models: \$125.

G-suffix models: \$195.

Overvoltage Protection Crowbar: \$30.

Crowbar with System Trigger Input and Output: \$40.

**MANUFACTURING DIVISION:** NEW JERSEY DIVISION

Green Pond Road

Rockaway, New Jersey 07866

## CHANGE OF ADDRESS NOTICE

The address shown is NOT correct.  
It should be as I have indicated below

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$50^{\circ}\text{C}$ . Because of the standardized design, specials with outputs up to 99 volts are recognized under the Component Program of Underwriters' Laboratories, Inc, as are the standard units.

### Acknowledgments

Mechanical design was by Val Marra, John Pratt, and Jack Leber. Mauro DiFrancesco and John O'Connor contributed to the circuit design (John also designed the crowbar). Victor Tom contributed some of the initial work on the computer program and Jon Williams developed the automatic test set used in production. Transformer design was by Win Siepel. Others who contributed to the overall effort include Nick Greendyke, Bill Darcy, Tony Stanislaos, Gene Gilligan, and Ken Woolley. 🐶



**James S. Gallo (CENTER)**

Following graduation with a BSEE degree from the Newark College of Engineering (1962), Jim Gallo entered a military-sponsored program at MIT, earning an SM degree in astronautical control systems two years later. He then spent four years at the White Sands Missile Development Center in New Mexico as the officer in charge of instrumentation requirements for testing inertial guidance components. Following that, he spent one year as an instructor in control systems at the Air Force Academy.

Finishing his tour of duty in 1969, Jim joined the HP New Jersey Division, going to work on Digital Voltage Sources. Now Engineering Group Leader for Power Supplies, he nevertheless still likes to get involved in the minutiae of product design.

Jim enjoys tennis and handball for recreation but most of his spare time is taken up by his family of four girls and one boy, ages 3 to 11.

**William T. Walker (LEFT)**

From Lehigh University (BSEE, 1969), Bill Walker went to HP, an arrangement that was cut short only three months later by an obligation to join the U. S. Army. Bill spent half of his two-year military stint with the Satellite Communications Agency and then off to Vietnam as a battalion communications officer, a situation that involved herding truck convoys as much as riding the air waves.

Returning to HP, Bill picked up on the project he had left—developing a system for automatic test of components during component evaluation. Once that was completed, he joined the modular power supply project.

Bill's spare time activities include wood cuts, in linoleum blocks as well as wood. He is married but so far has not acquired additional family. Bill is a member of Tau Beta Pi and Eta Kappa Nu.

**Willis C. Pierce (RIGHT)**

Although EE subjects figured prominently in his college program, Bill Pierce took his BS in ME (California State Polytechnical College, 1959). He then used both disciplines by going to work for a welding equipment company, designing control circuits. While engaged in that activity he earned his MSEE (Stevens Institute of Technology, 1967) and three patents.

Bill joined HP in 1968, going to work on the 6177B family of Precision DC Current Sources (HP Journal, September 1969). He then moved into the modular power supply program as project leader.

Bill and his wife have 3 boys, one 12 and a pair of 10-year-olds, who all swim competitively. This has involved him as a YMCA swimming official and as a board member of a local swim club, but on his own, he likes to play tennis.

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