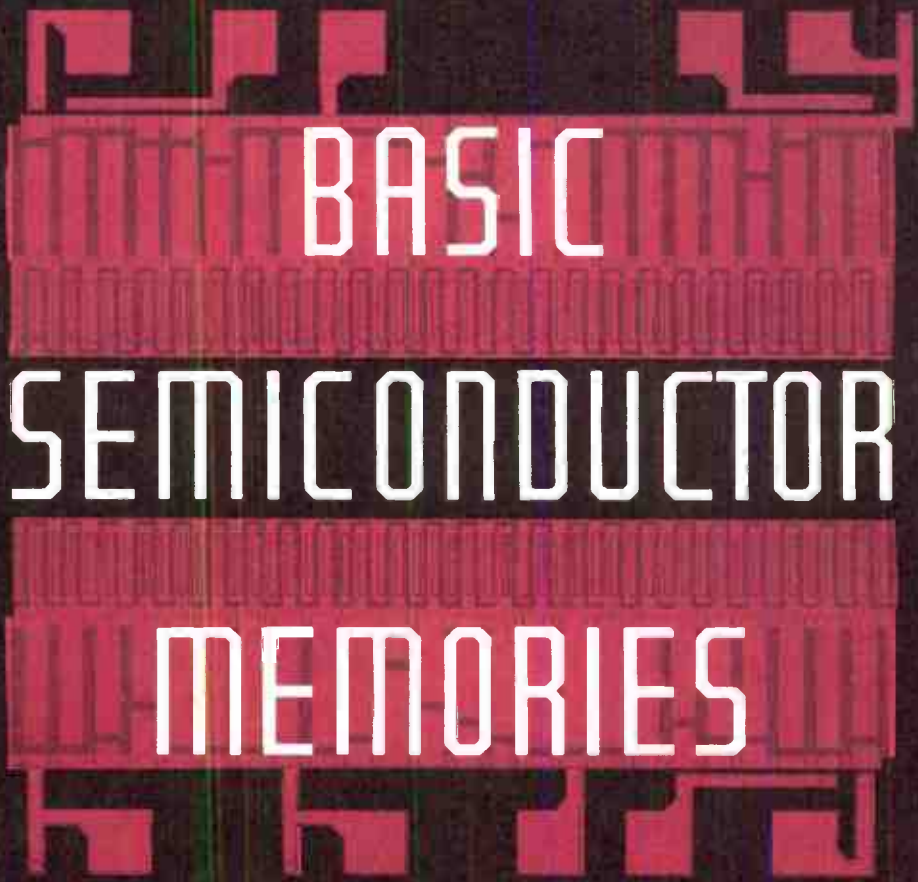
GTE LENKURT

DEMODULATOR

SEPTEMBER/OCTOBER 1975



BASIC SEMICONDUCTOR MEMORIES

PARTS 1 AND 2

BASIC SEMICONDUCTOR MEMORIES
Part 1

Virtually all data processing equipment is concerned with the storage and transfer of information in a digital form. The essential characteristic of the elements comprising such equipment is operation in at least two well-defined and distinct states.

Data processing systems have revolutionized our world, allowing vast amounts of information to be stored, exchanged, updated, and utilized in ways undreamed of a few years ago. A chain of department stores can be tied together, for example, by a data network making current inventory, personnel and credit information instantly available at widely separated locations; a railroad can control activity at its switchyard from a control center hundreds of miles distant; switching functions within a telephone company office can be accomplished rapidly and reliably in accordance with stored program instructions. The information involved in each of these examples is different, but the underlying processing principles are the same.

A digital computer or data processor of any type is basically a stored-program machine, in which a memory facility holds a set of operating instructions — the system program. Information is put into a digital format (see the August, 1974, *Demodulator* for a discussion of this conversion) and fed into the machine, which retains it in a data memory. The instructions in the program memory, which are also in digital form, tell the processor what problem is to be solved, or function performed, related to the input data. When the operations demanded by the program memory have been completed, the data is fed out to be utilized in some manner. In practice, program instructions are often stored within the same memory facility as the data; in this way, the program can also be changed if desired.

Despite surface differences, the ways in which memory facilities receive, hold, and feed out information are all based on either sequential or random access principles.

Sequential Memories

The sequential, or serial, memory method requires that the data bits comprising the information be arranged in a particular order. Data stored in this manner — including both programmed instructions and input information — is retrieved strictly in accordance with its position in a time sequence.

A simple example of sequential memory storage is paper tape, which uses the presence or absence of holes to indicate the condition of a data bit; the combined states of several bits identify a particular digit (see Figure 1). The tape is moved through a sensing device to convert the hole patterns into a series of pulses for electronic processing. Each piece of information is retrieved as it passes the

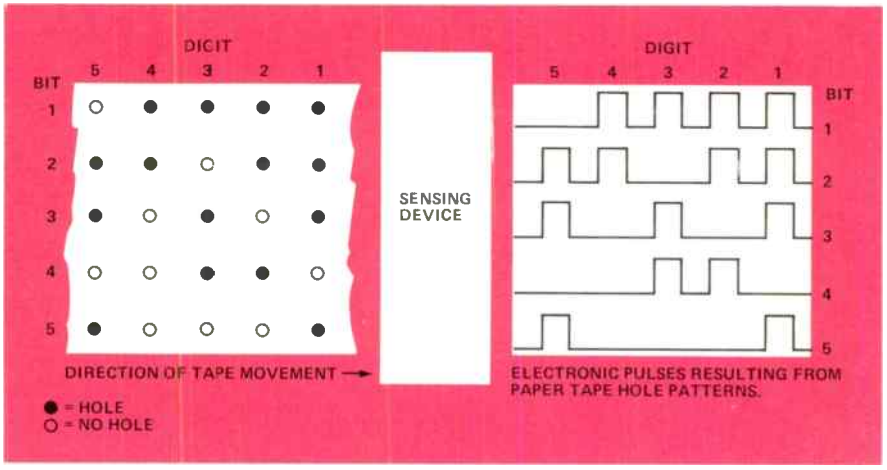


Figure 1. Paper tape is a form of sequential memory storage, in that the bits identifying a given digit can only be retrieved during their allotted sensing time, which may cause delay in finding desired data.

sensor. Another form of sequential memory storage is magnetic tape, which stores information as magnetic flux variations corresponding to the 1's and 0's of digital data.

Sequential access memory systems, including punched cards and magnetic disks as well as tapes, have been widely used in the area of mass computer memories. They typically contain program instructions and must be physically introduced into the processor system – threaded through a sensing device, for example – so that input data can be operated upon. They may also be used to retain the data for future processing. These devices provide a permanent storage capability since the cards, disks, and tapes can be removed and filed for repeated use, and they have non-destructive readouts (i.e., data does not have to be re-entered every time it is used); however, they have some shortcomings which limit their usefulness in high-speed memory applications.

For example, sequential access can be a relatively slow process because a large amount of irrelavent data may have to be scanned before the desired bits are found. This delay may be from milliseconds to minutes, which is much too great for many of the uses to which modern data processing equipment is put. Additionally, these sequential mass memory systems require a mechanism to move the data-carrying medium past the sensor; this device is of necessity completely mechanical, and is subject to the adjustment and maintenance considerations which apply to all such devices.

Temporary Memories

Cards, tapes and disks continue to play an important role as high-density, long-term mass memory storage elements in such applications as personnel record maintenance, inventory control, and retention of performance data for comparison with future achievements.

For low capacity, temporary memory storage, however, structures composed of semiconductor devices have become dominant in recent years.

Temporary data storage facilities are used in such areas as office equipment (calculators, etc.) and immediate-use or "working" memories wherein a data processing device can hold the data with which it is dealing at any given time. It is not uncommon for a data processing system to use tapes and similar elements as permanent, high-volume program storage facilities, and semiconductor structures for the "working" memories in which the stored data is operated upon.

Temporary memories are also widely used in data processing terminals, which serve as remote input/output units for a large central computer and may be in any number of forms, from a simple typewriter keyboard to a small computer. Terminals provide a means of encoding data for manipulation by a central computer, and decoding it for use by a human operator.

Interconnection of central computer and remote terminal is commonly made over telephone lines through an interface unit called a modem, or data set. The data set may also contain a temporary memory facility which allows it to hold data and either condition it for transmission over the lines or prepare received data for application to the processor.

The semiconductor devices used in temporary memory structures are typically arranged as groups of individual units called memory cells, each of which stores one bit of information as either a logic 1 or logic 0. A cell may consist of as little as one transistor-capacitor combination, or it may be a complex arrangement of several components, but, whatever its composition, it has at least two states that can represent digital data bits.

Shift Registers

A shift register is a device for the temporary storage of digital information; when a shift, or clock, pulse is applied, the register accepts new data and moves every stored bit one step toward the output.

Figure 2 shows an example of a semiconductor shift register containing five memory cells, each of which is a solid-state reset-set (R-S) flip-flop circuit. Data applied to the register input in a digital form is stored and shifted from cell to cell in accordance with the clock cycle rate. A logic 1 on the S input of cell 1, for example, will set the flip-flop to the 1, or "on," state if a clock pulse is present at input C, thus storing the digit. On the next clock pulse, the stored bit is shifted out of cell 1 to set the second cell to the 1 state, and a new digit is fixed in the first cell. This procedure continues through the register, with the output of the final cell being shifted out for data processing. The clock frequency controls the rate at which the shift register stores and feeds out data bits, with each bit being delayed between input and output by as many clock cycles as there are cells in the register. Since the storage and retrieval are done on a first-in, first-out basis, the shift register is a sequential memory storage device.

Digital data can also be handled by a random access process. This does not mean, of course, that no orderly procedure is involved; it means, rather, that information can be stored in a particular memory cell, or location, and retrieved without regard for any other location.

Random Access Memory Systems

A random access memory (RAM) can be defined as a structure in which any data bit can be stored (written) or retrieved (read out) in any order.

One of the most basic ways to create a memory cell is through the use of the bistable multivibrator, or

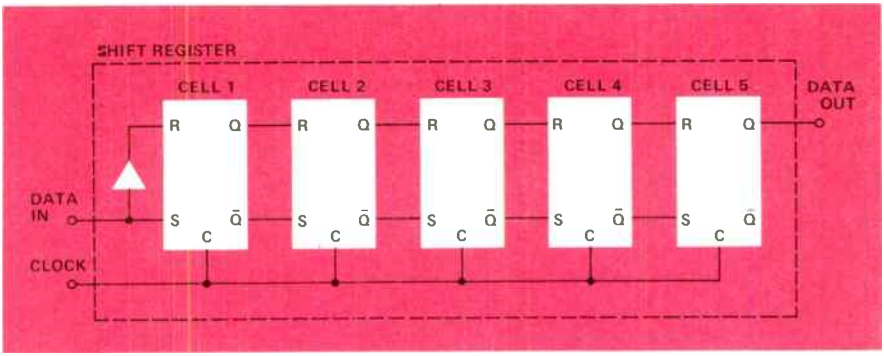


Figure 2. The shift register, which stores data for as long as it takes for the clock to move it through each cell, is typical of semiconductor sequential memory systems.

flip-flop. As shown in Figure 3, such a memory cell may consist of only two transistors, two resistors, and a power source. In this cell, one or the other of the transistors is always conducting, holding the other one off. When an external signal forces the off transistor into conduction, the initially on transistor turns off and remains in this condition until another external signal resets it. The flip-flop, therefore, has two stable states which can be used to store information in the form of logic 1's and 0's.

A RAM is essentially a matrix of such memory cells with each cell identified by a unique code, or address. The data processing equipment can retrieve a bit of information by addressing the proper location. Because of the matrix structure, the time required to locate any given bit is approximately the same as that required to locate any other bit. For example, in Figure 4 the digit stored in cell 1, at location A1, could be available at the data output in almost exactly the same time as the bit in cell 16, location D4. This rapid access to information makes the RAM ideal for application as a temporary storage facility.

Random access memory structures are of two basic types: read/write and read only. A read/write RAM is programmable; that is, data can be entered into, changed, and removed from the memory at any time. A read only memory (ROM), however, has certain data patterns fixed into it, usually during the manufacturing process. In such a structure, information can be read out – it will always perform the same function – but the stored program does not change. Because the data pattern is fixed, a ROM retains its program regardless of circuit power considerations; that is, it is a "nonvolatile" memory device. A read/write memory, however, needs a constant source of power to remain in operation; if power is removed, the semiconductors stop conducting and the stored information is lost, so the read/write RAM is considered to be a "volatile" device.

Although it is not technically accurate to do so, common usage has led read/write memories to be referred to simply as RAM's, while read only structures – which are, in reality, a type of RAM – are designated ROM's, and this discussion will follow the same nomenclature.

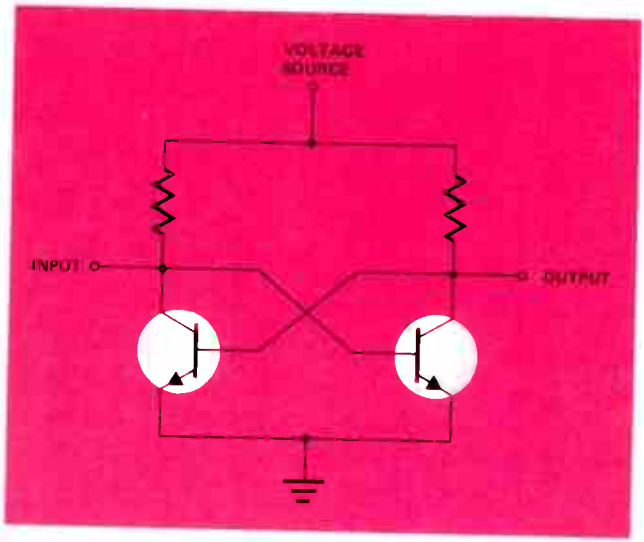


Figure 3. The bistable multivibrator, or flip-flop, has two stable states, making it an ideal digital data memory storage cell.

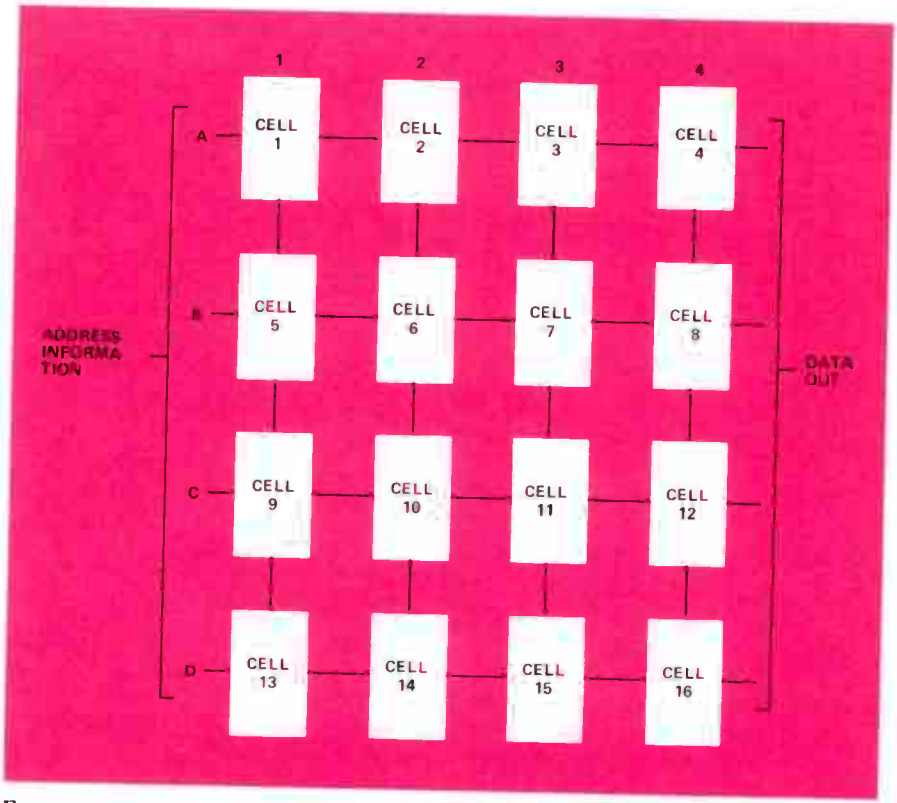


Figure 4. A random access memory (RAM) is a matrix of memory cells, any of which can be accessed without regard for any other cell.

Bipolar and Unipolar Transistors

The two most widely used devices in memory matrix design today are the bipolar and unipolar, or field effect, transistor. Each can be easily realized as an integrated circuit (IC) component, and they are readily adaptable to virtually any circuit configuration.

Essentially, a bipolar transistor is a semiconductor device whose conductive properties depend upon both majority and minority carriers; that is, current flows in a bipolar transistor because of the simultaneous movement of both positive and negative charges. Negative charges predominate in N-type semiconductor material because there is a surplus of free electrons within the material's atomic structure; P-type material, however, has a shortage of free electrons. The regions in which the electrons would normally exist act as positive, mass-bearing charges called "holes"; P-type material thus maintains an excess of positive charge carriers. The common transistor is a general type of bipolar device, since its current flows due to hole and electron movement. Figure 5A shows the normal flow pattern within an NPN structure (Figure 5B shows a bipolar NPN structure as an integrated circuit). The forward-biased emitter-base junction allows electrons to be injected by the emitter into the base region. Within the base, the greater part of the current flow is caused by holes combining with the excess electrons. The reverse bias of the collector-base junction allows electrons to pass into the collector region; because there are two N-type regions, electrons are the majority carriers, although the simultaneous action of the minority carrier holes is indispensable.

The field effect transistor (FET) is a unipolar device, in that its current flow is the result of the movement of only one type of carrier. In what is called the p-channel FET, holes are the majority carriers, while the carriers in an n-channel FET are electrons.

Figure 5C shows a p-channel FET structure operating in the enhancement mode, which is the most common operating mode for FET's. In this mode, there is no conduction within the device when the gate voltage is zero; the other mode of operation is called depletion, wherein the semiconductor device is always conducting and requires a proper gate-to-source voltage to turn off.

When the gate in Figure 5C is made negative with respect to the source, it creates an electrostatic field which attracts holes from the n-type semiconductor material toward the area directly below the gate dielectric material. Initially, this n-type area has a surplus of electrons, but as the holes are drawn into it, the electrons are neutralized. At some gate voltage, the holes become dominant and a current-carrying channel is produced between source and drain in which holes are the majority carriers. Because the gate is electrically isolated from the rest of the structure by the dielectric material, there is no current flow into it; the channel, which allows current to flow between source and drain, is created and maintained by the electrostatic field.

The need to provide more electronic function in increasingly small areas has resulted in a great variety of miniaturized circuits. Bipolar transistors, for example, can be realized as discrete items, such as those seen in various entertainment products. In data processing applications, however, the large number of components required to produce a memory matrix makes the use of such bulky devices impractical; a circuit board with several hundred discrete transistors mounted on it — which is what a memory

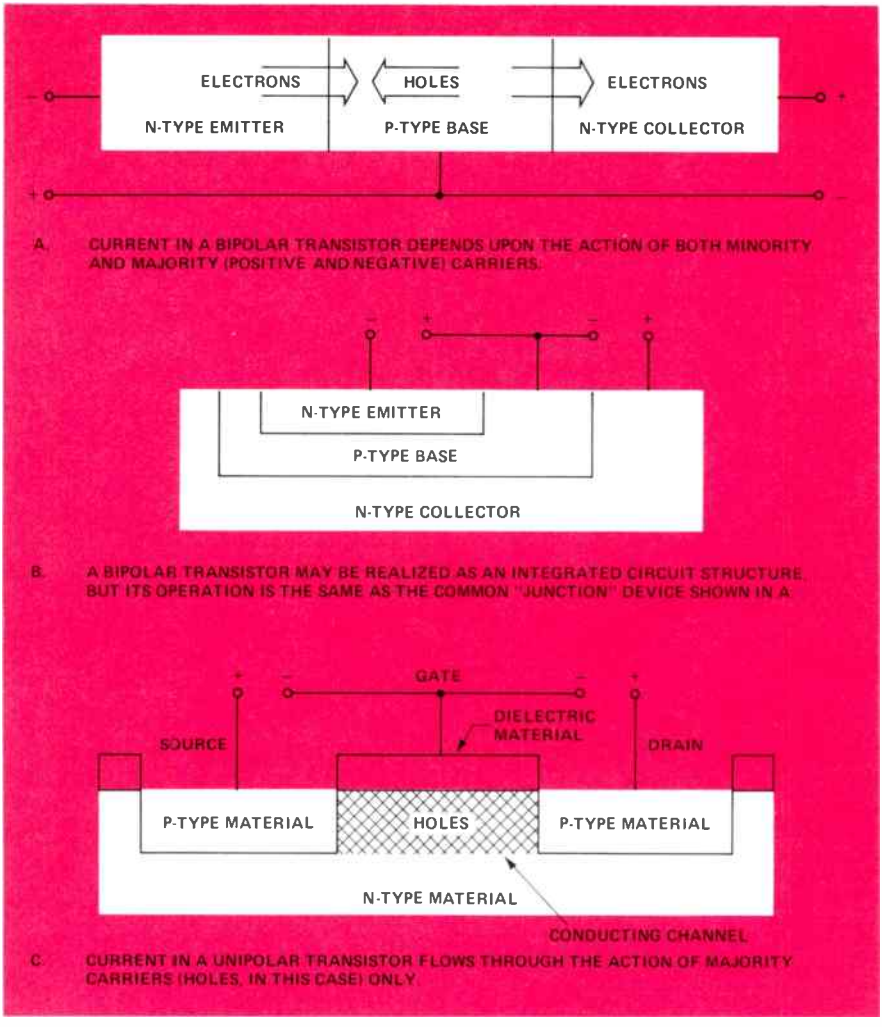


Figure 5. Bipolar and unipolar transistor structures are the most widely used semiconductor memory cell components.

matrix would require – would be too unwieldy to be of any real use.

Bipolar Transistor RAM's

Integrated circuit techniques allow quantities of circuit elements to be realized in a small space; these techniques have been used to produce bipolar transistor memories of various microminiaturized sizes and densities.

The basic storage element in these matrices is the bistable flip-flop, which appears in many circuit variations to meet different application requirements.

A bipolar RAM cell which has been widely used is the transistor-transistor-logic (TTL) type, exemplified by the multiple-emitter circuit (see Figure 6). In this case, the data processor applies

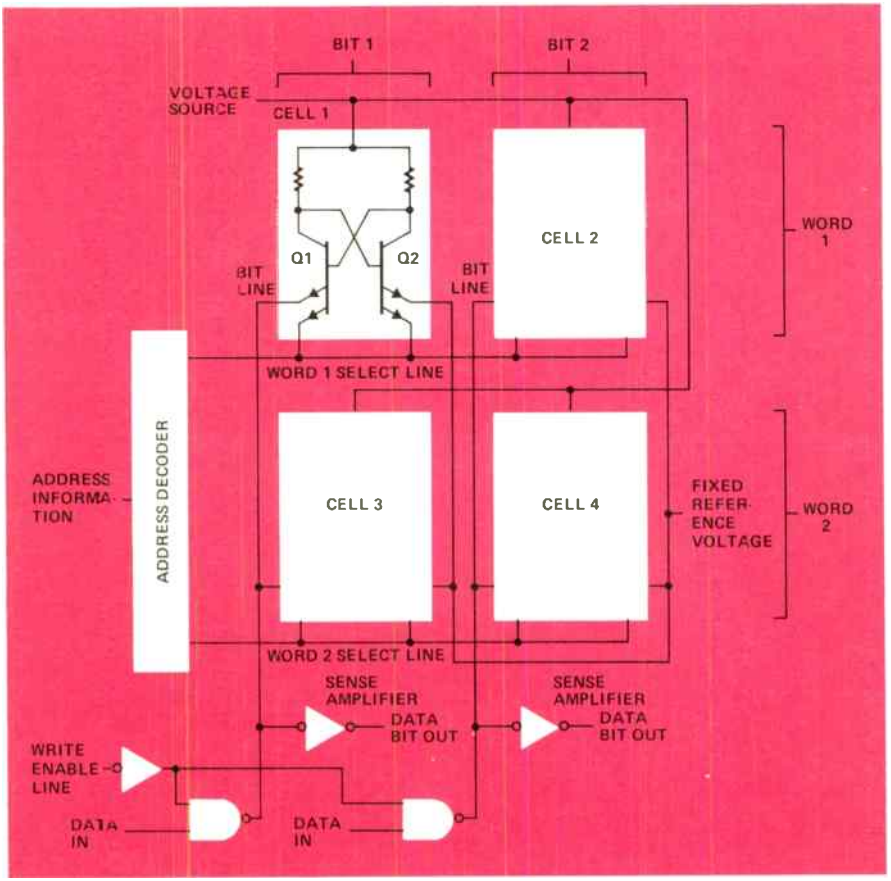


Figure 6. A 2-word, 2-bit-per-word memory array utilizing multi-emitter bipolar transistor structures.

an address code to a decoding circuit; the decoded address raises the voltage on the correct word select line (places it at a logic 1 level), preparing the cell for the read or write function. A logic 1 bit can be written into the cell, for example, by placing the write enable line at a low voltage (logic 0) level while the data bit input is logic 1. This causes the bit line to be low, turning Q1 on and Q2 off, a state which represents a logic 1 within the cell. Once the write function is complete, the address changes, the word select line returns to a logic 0 state, and Q1 remains on. To read out the stored digit, the address raises the word select line level and the write enable line is held high (logic 1), allowing read current representing the value of the cell's contents to flow into the appropriate sense amplifier for output to the data processor. Because the read process does not change the state of the flip-flop, the stored information is not lost and the cell is considered to have a "non-destructive" readout capability.

The 2-word, 2-bits-per-word memory shown in Figure 6 is, of course, limited in its application. The same

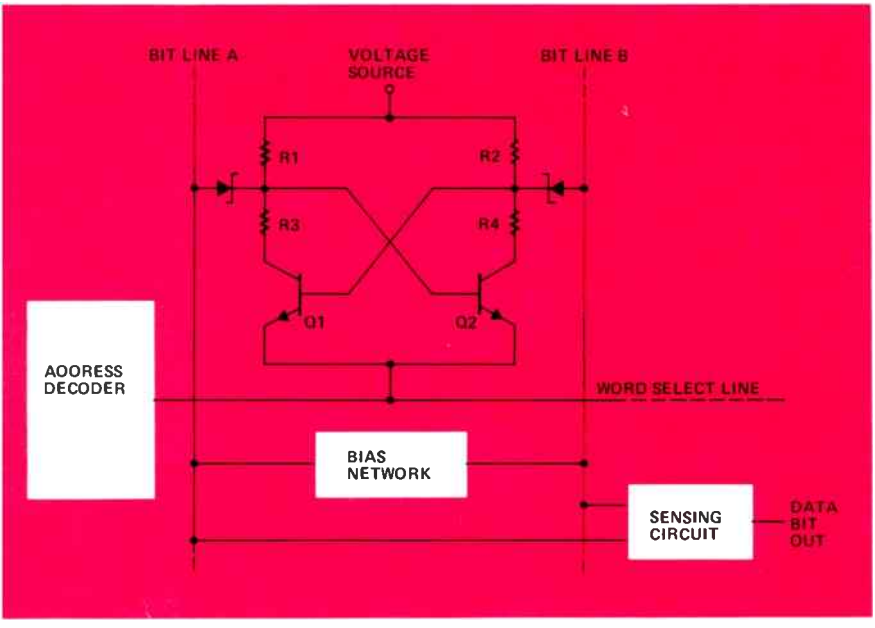


Figure 7. A diode coupled memory cell uses gating diodes to control conduction and reduce power consumption.

addressing, reading, and writing functions, however, are performed in bipolar RAM's containing several times the number of cells. A typical example of expanded capacity is a single integrated circuit capable of storing 16 words of 4 bits each, for a total of 64 bits on one tiny silicon chip. GTE Lenkurt uses nine such chips in both its 262A and 262B data sets. The bipolar RAM's comprise a data memory, in which input data is held to be operated upon. Because of the read/write capabilities of the RAM's, the data being processed can constantly be updated and changed.

Major considerations in memory design include the speed with which a cell can be made to change state (access time) and the amount of power dissipated by the cell's components.

Operating in a saturation mode – in which the "on" transistor constantly conducts the maximum possible current – the TTL-type memory cell requires some amount of time to drive the transistor out of saturation before a change of state can occur. This delay is only on the order of nanoseconds, but is enough to concern circuit designers. In addition, the saturation mode consumes relatively large amounts of power. Two of the more successful configurations developed to overcome these disadvantages are the diode coupled and emitter-coupled logic (ECL) cells.

Diode Coupled RAM's

Two gating diodes are used to control conduction in a diode coupled cell (Figure 7). In integrated circuits, these diodes are frequently "hot-electron," or "Schottky barrier," devices, which become forward-biased at lower voltages than conventional diodes.

If the state of a cell must be changed to store a bit, the address

decoder causes the voltage on the word select line to be forced low, while the voltage is raised on the bit line associated with the transistor to be turned off. Referring to Figure 7, in which Q2 is hypothetically to be turned off, raising the bit line B voltage and dropping the word select line (effectively making it more negative) draws additional current through R4, increasing the base voltage on Q1 to the point at which it begins conducting. The cross-coupling of the transistors then causes Q2 to turn off, thus effecting the cell's change of state.

Reading the stored digit out of a diode coupled cell also requires that the word select line be forced low, but in this case there is no voltage increase on either of the bit lines. The combined effects of the lowered word select line and a bias network cause the diode associated with the "on" transistor to be forward-biased, causing the diode to conduct. Since the diode associated with the "off" transistor is reverse biased, a differential voltage develops between the bit lines. A sensing circuit determines the cell's logic state from this voltage.

Read current in a diode coupled cell is greater than standby current, which flows when the cell is storing a bit without being addressed, but is substantially lower than write current. Because of this, the voltage developed across the load resistors during the read operation is not great enough to change the cell's state and the readout is a nondestructive process.

Since standby current is lower than read current and is present a greater percent of the time, overall power consumption in a diode coupled cell is lower than that of a TTL device.

ECL RAM's

The structure of emitter-coupled logic (ECL) memory cells closely resembles that of TTL cells, but biasing techniques are used to keep the transistors out of saturation. This allows the ECL storage element to change state very rapidly; the greatest advantage of ECL over other semiconductor memory configurations is that it has the shortest access time of all. Reading and writing processes are accomplished in essentially the same manner as for TTL, but at a greater speed. Because it constantly draws high current, however, an ECL memory cell has even higher power consumption than TTL, a fact which does impair its usefulness in certain applications.

Numerous other semiconductor memory cell configurations utilizing bipolar transistor integrated circuit technology have appeared. Virtually all of these are variations on the three basic types described here. The October, 1975, *Demodulator* will continue this discussion, describing some of the basic metal oxide-silicon (MOS) memory structures.

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BASIC SEMICONDUCTOR MEMORIES
Part 2

Almost every new computer utilizes semiconductor memory devices, and the use of these devices is spreading to the communications field. Semiconductor memories are beginning to replace cores and drums in telephone switching centers, and digital data carrier systems using PCM techniques, which are inherently suited to semiconductor logic and memory circuits, are being readied for introduction.

The September, 1975, *Demodulator* introduced many of the concepts basic to the understanding of semiconductor memories, and described various types of bipolar transistor read/write random access memory (RAM) cells. This issue concentrates on the discussion of metal oxide-silicon devices.

MOS Technology

One of the major objectives in semiconductor memory design has been to incorporate as much capacity as possible in the smallest area. The greatest size reductions have been achieved with metal oxide-silicon (MOS) techniques, which produce field effect transistor (FET) structures that are considerably more compact than the bipolar integrated circuits (IC's) previously discussed.

An MOS FET is formed by depositing an insulating metal oxide – most often silicon dioxide – on a chip of silicon. Etching processes then remove the oxide from selected areas of the chip, exposing the substrate at source and drain locations while leaving the gate region insulated. Further processing establishes n- and p-type areas within the substrate.

The size reduction possible with MOS techniques allows a much denser memory array to be produced within a given space than is possible with bipolar devices; there are also substantially lower power requirements and reduced packaging costs.

Storage cells composed of MOS FET's may be of either a static or dynamic nature. A static cell retains its stored data as long as power is supplied to the circuit; a dynamic cell depends upon capacitive charge storage to hold its data, and must receive a "refresh" input to counteract the effects of leakage.

Static MOS RAM's

The basic static MOS RAM cell is a bistable multivibrator (see Figure 1) closely resembling the bipolar flip-flop used in TTL memories. In an MOS flip-flop, however, transistors serve not only as cross-coupled inverters (Q3 and Q4), but also as load resistances (Q1 and Q2). Electrical isolation of the FET gate results in a very high input resistance which can be controlled by the gate voltage. A large-value resistor can thus be produced by an FET in a relatively small space compared to a conventional resistor.

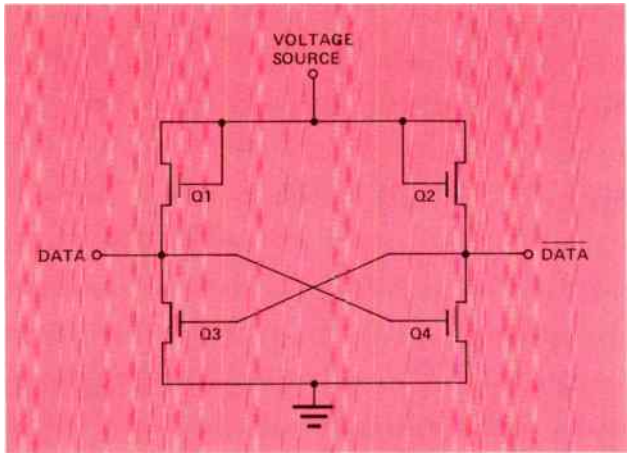

Figure 1. The heart of the static MOS RAM storage cell is the bistable flip-flop composed entirely of field effect transistors (FET's). The logic level at one terminal is always the complement of that at the other.

Since only one of the cross-coupled inverters conducts at any given time, the cell has two stable states which can be used to store information in the form of logic 1's and 0's. The state of the cell is determined by external address and data signals. The cell's state remains constant unless changed by an external signal, so no refresh action is required and the circuitry needed to support the operation of the cell is simplified.

A static MOS RAM storage unit, however, contains a minimum of four transistors, so it occupies a considerable amount of space on a silicon chip and consumes a relatively large amount of power. Because of these disadvantages, static devices have been largely replaced by dynamic MOS RAM's.

Dynamic MOS RAM's

The basic storage element in a dynamic MOS RAM cell is a capacitor, which holds and releases a stored charge in response to read and write commands. While the capacitor could be an external device, it is much more common for dynamic RAM's to utilize the capacitance existing between gate and source of the MOS FET itself. This capacitance is due to the isolation of the gate from the rest of the structure by a dielectric material. Charging the gate-source capacitance sufficiently to turn the transistor on represents a logic 1 state in most applications, while a lower charge or no charge at all serves as a logic 0.

Inevitably, as with all capacitive devices, the charge stored in the gate-source region drains off due to leakage current. If the charge is allowed to deteriorate too much, the data bit is lost, so some means must be provided to periodically restore, or refresh, the charge; a common requirement is that every cell in a memory matrix be refreshed every 2 milliseconds. Circuits to accomplish this are included in dynamic RAM designs, as are address decoding circuits.

The operation of a typical dynamic MOS RAM cell can be illustrated with the 3-transistor cell shown in Figure 2. In this case, information is stored as a charge in the gate-source capacitance (C_G) of transistor Q2. To write a data bit into this cell, an address decoder produces a write select signal, activating transistor Q1 and allowing data on the write data line to be transferred to the storage element. Depending

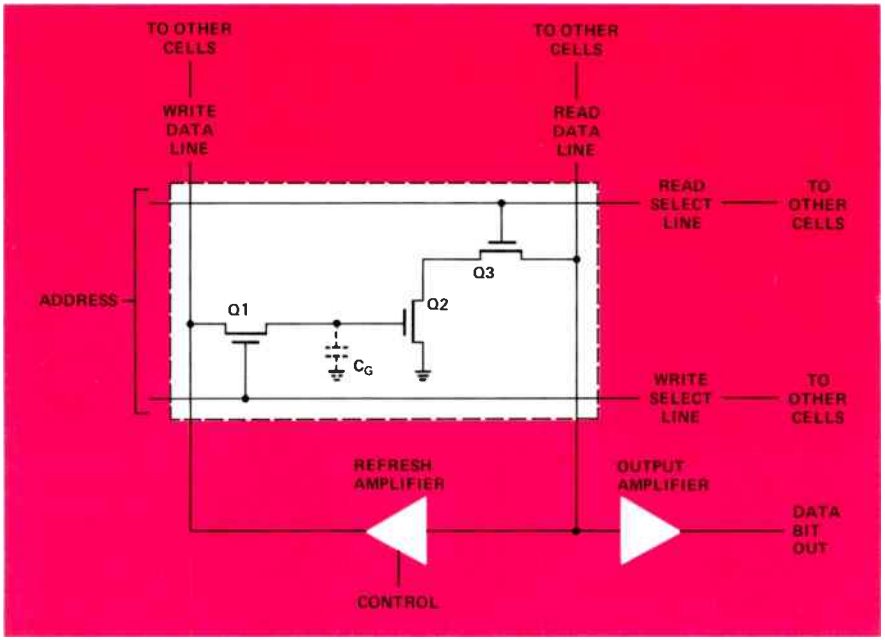

Figure 2. A dynamic MOS RAM cell stores data in the gate-source capacitance of one of its transistors.

upon the state of the data input, C_G either charges or is discharged. When the write select signal is removed at the end of the write cycle, the bit is held in the cell.

At the beginning of a read cycle, both the read and write data lines are preset to some voltage. When the address decoder produces a read select signal, Q3 is ready to begin conducting. If the charge on C_G is sufficient (logic 1), Q2 turns on and current flows through Q2 and Q3, reducing the voltage on the read data line. With no charge on the capacitance, Q2 and Q3 remain off and the read data line stays at its preset level. Because of the gate isolation, C_G is in the same condition (charged or discharged) at the end of the read cycle as at the beginning, making the read process "nondestructive." An output amplifier senses the state of the read data line and determines what cell condition would produce it (a low-level line generally indicates a stored logic 1) for application to the data processor.

Refresh

Refresh of the stored digit in Figure 2 is accomplished through a clocked amplifier connected between the read and write data lines. Control circuitry provides the timing necessary to keep the refresh cycle separate from the read and write operations.

The refresh process involves reading out the stored digit and writing it back into the cell. To do this, both data lines are preset at the beginning of the refresh cycle. A read select signal is then produced, transferring the bit to the read data line in the same manner as the normal read operation. The refresh amplifier inverts the condition of the read data line and applies it to

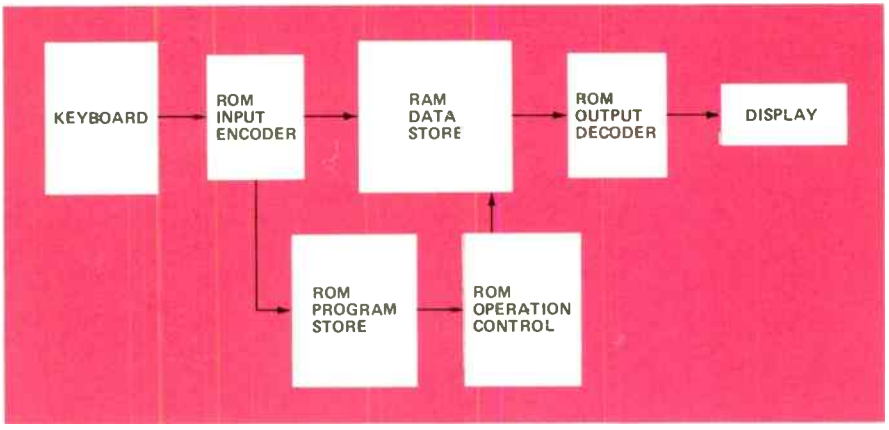

Figure 3. A pocket calculator typically utilizes both RAM and ROM facilities to process input data.

the write data line. A write select signal then replaces the read signal and the data present on the write data line is entered into the memory. If, for example, a logic 1 (maximum charge) is stored on C_G, the read data line is forced low (logic 0) when the read select signal forces Q2 and Q3 into conduction. The refresh amplifier inverts this and applies logic 1 to the write data line; the presence of the write select signal causes this data to be written into the cell as a refreshed bit. With no charge (logic 0) on C_G, this sequence is repeated, with a logic 0 appearing on the write data line to ensure that the capacitance is not charged by stray circuit currents.

In Figure 2, timing from the control circuitry allows a single amplifier to serve an entire column of cells. One alternative configuration uses a common read/write data line. This lets the cell form a loop within itself and thus eliminates refresh amplifiers.

ROM's

A read only memory (ROM) is a data storage facility into which information is normally written only once. After this entry, a ROM always produces the same output when addressed.

The difference between the read/write RAM and the ROM can perhaps be best illustrated with the example of the pocket calculator. In almost all calculator designs, a RAM matrix serves as a "working," or data, memory and ROM's are used for input/output interface, timing control and program storage (see Figure 3).

Each key on the calculator keyboard is identified by a unique binary number; all of these numbers are permanently fixed in the ROM encoder so that, when a key is pressed, the corresponding binary number appears as the encoder output. If a digit key is pressed, the bits comprising the number are written into the RAM data store. Function key (addition, subtraction, etc.) numbers are applied to the ROM program store as addresses. In the program store are contained instructions for each function; when an address is presented, the proper instructions are read out of the ROM, leading to performance of the desired operation upon the data held in the RAM. When the function has been

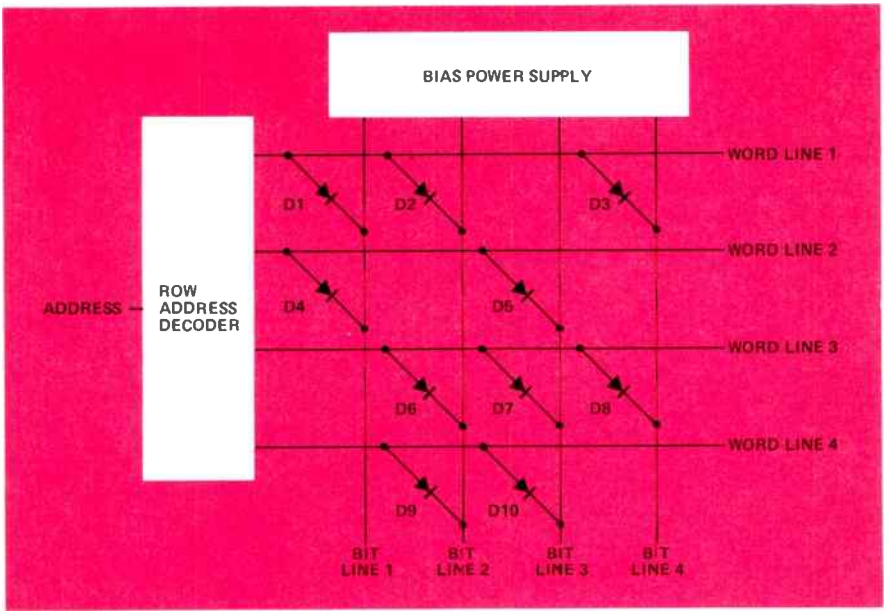

Figure 4. A diode network with random access addressing is the simplest type of semiconductor ROM.

completed, the result is read out and applied to the decoder, which puts it into a form suitable for display.

The basic ROM structure is a matrix of elements, each of which is accessed by a random address code, allowing approximately equal access time to all bits. The simplest ROM structure is a network of diodes wherein the presence or absence of a diode determines the logic state of a particular location; such a network is shown in Figure 4. The row address decoder raises the voltage on the appropriate word line to a high positive level, forward-biasing the diodes attached to that line. When the diodes begin conducting, they force their associated bit lines to a high (logic 1) level, while bit lines not connected to diodes remain low (logic 0). Output amplifiers sense the state of each line and present the bits to the data processor's other circuitry.

For example, if the row address decoder raises the word line 1 level, diodes D1, D2, and D3 conduct, raising bit lines 1, 2 and 4. In this case, the matrix output would be the binary number 1101. The next address might raise word line 4, in which case the output would be 0110. In some applications, column (bit line) addressing is added to select fewer than the maximum possible bit outputs.

ROM matrices are also formed with bipolar and MOS devices. In the most common configurations, the presence or absence of conductors establishes logic states.

Figure 5 shows a ROM matrix utilizing multiple-emitter bipolar transistors. In this case, the collectors are used as row enabling contacts, replacing the word lines, and emitter contacts are omitted from selected locations to set logic levels. When the row address decoder raises the voltage

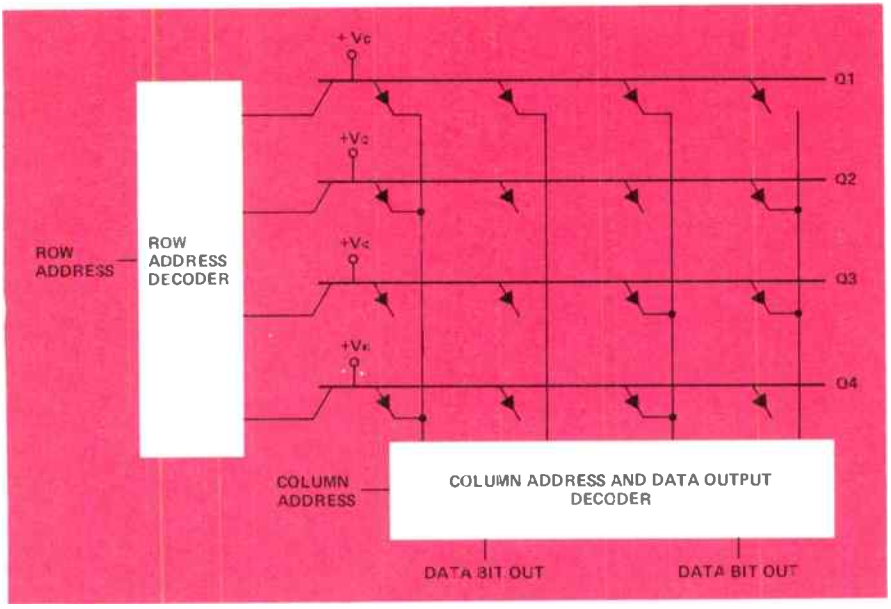

Figure 5. Bipolar read only memory matrix.

on the appropriate collector to a sufficiently high level, the transistor segments with emitter contacts begin conducting; for example, if Q2 is selected, the matrix output is 1001 (the level of columns 1 and 4 raised by conduction, 2 and 3 remaining low). In Figure 5, column address and data output decoding selects two of the four bits for application to the processor.

In Figure 6, a ROM matrix composed of static MOS FET devices is shown. Logic states are determined by the presence or absence of gates within the transistor structures. Reading this memory is accomplished in the same manner as diode and bipolar ROM's, except that the bit lines are driven low (to ground) when the FET's conduct.

Programmable ROM's

Semiconductor memories are almost universally formed on minute silicon chips capable of holding large numbers of integrated circuit devices; the chips often contain complete addressing, decoding, and output circuitry in addition to the memory cells.

In the formation of standard ROM matrices – in which the stored data is never to be changed – logic states are established during the manufacturing process by omitting the proper elements to create the desired bit pattern. This is the most prevalent type of read only memory. There are cases, however, in which standard memories are not available to meet application requirements, so programmable ROM (PROM) matrices are also produced

A PROM is essentially a semiconductor matrix which has its program written into it at some time other than the manufacturing process. The manufacturer provides a chip on which all of the rows and columns (word and bit lines) are linked by conducting devices. Before integrating the chip into a circuit, the purchaser of the PROM

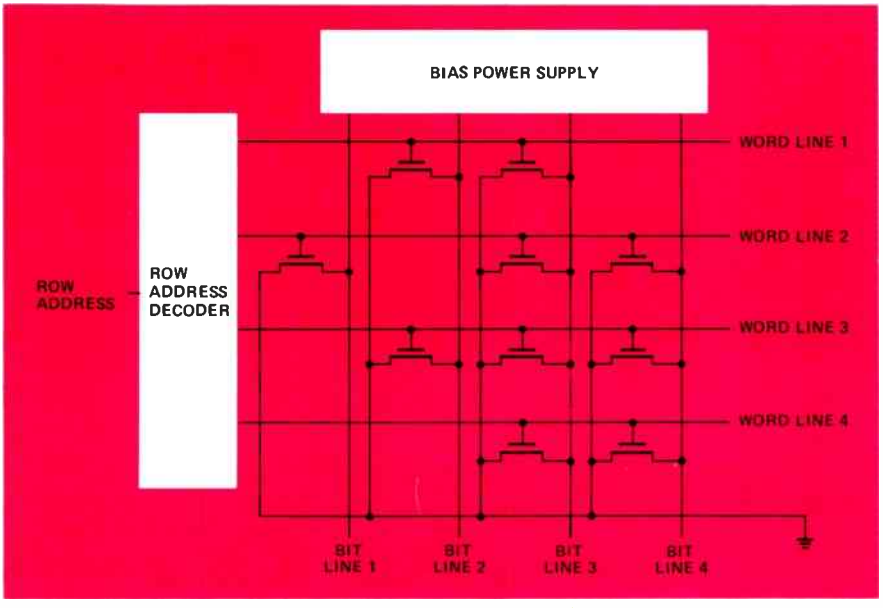

Figure 6. The logic states within a static MOS ROM are determined by the presence or absence of gate contacts.

uses various techniques – from application of a high-level write current to a laser beam – to eliminate devices from the matrix. In this way, a stored program unique to a given application can be produced.

New Developments

This discussion has covered structures that are representative of devices currently used in data processing memory facilities, and has not attempted to consider all of the variations of the basic structures. Advances are being made at a remarkable rate, and today's technology may be totally obsolete in a few years. Among the new memory devices that may bring this about are charge coupled devices (CCD's), bucket brigade devices (BBD's) and magnetic bubbles. Charge coupled and bucket brigade devices are similar in that both store digits as the presence or absence of electric charge.

A basic CCD is a semiconductor chip – either n- or p-type – over which a dielectric material is laid. A series of gate contacts are placed along the dielectric. Charge is stored as minority carriers under the gate regions. When the substrate is p-type, for example, applying a positive voltage to one gate attracts electrons out of the substrate until they dominate in the area directly beneath the gate, forming a "potential well." This storage condition is maintained for times up to several seconds after the gate voltage is reduced. Raising the potential on the next gate in the series forms a second potential well into which the stored charge is transferred; gate potentials are sequentially raised by a clocked voltage to move the stored bit through the device. The CCD is thus a sequentially accessed memory facility similar to the shift register.

The movement of charge in a buck-

et brigade device is the same as in the CCD. Potential wells, however, are replaced by "buckets" of material unlike the substrate: for example, n-type areas may be embedded beneath the gates in a p-type chip to act as MOS storage capacitors.

Fabrication techniques currently limit the production of CCD's and BBD's, but they hold the promise of extremely small, very fast, low-power memories of high density, and many manufacturers are investigating their commercial feasibility.

Magnetic bubble technology is still in the developmental stage, but it also shows great promise. The bubbles, which are tiny, mobile particles whose polarity is opposite to that of the thin film containing them, can be arranged to form coded data patterns, thus providing a storage medium.

Conventional bipolar and MOS devices are being modified to achieve an optimum combination of memory cell size, speed and power consumption. N-channel and p-channel MOS FET's are being combined on one chip as complimentary MOS (CMOS) devices for low-power applications, and Schottky diodes are being introduced into various bipolar configurations to decrease power consumption and increase speed. One such modification has resulted in the low-power Schottky TTL memory cell, which has access speed approaching that of ECL (the fastest presently available cell type) and power requirements close to those of MOS FET's; GTE Lenkurt uses this family of devices in its 262A and 262B data sets to achieve the most rapid data processing possible with the least power. In another development, metal-nitride oxide semiconductors are being looked at as possible non-volatile read/write RAM's (memory facilities which would not lose stored data when power is removed).

Whether improvements to existing structures continue at the present rate, or new technologies take over completely, there is no doubt that semiconductors will play an increasingly important role in data processing systems.

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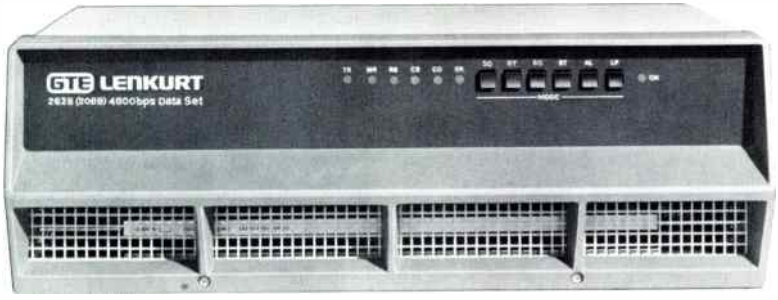

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