

# PHILIPS TECHNICAL REVIEW

The PCB 5010 digital signal processor  
Advanced telecommunications  
Ion-beam mixing



**PHILIPS**

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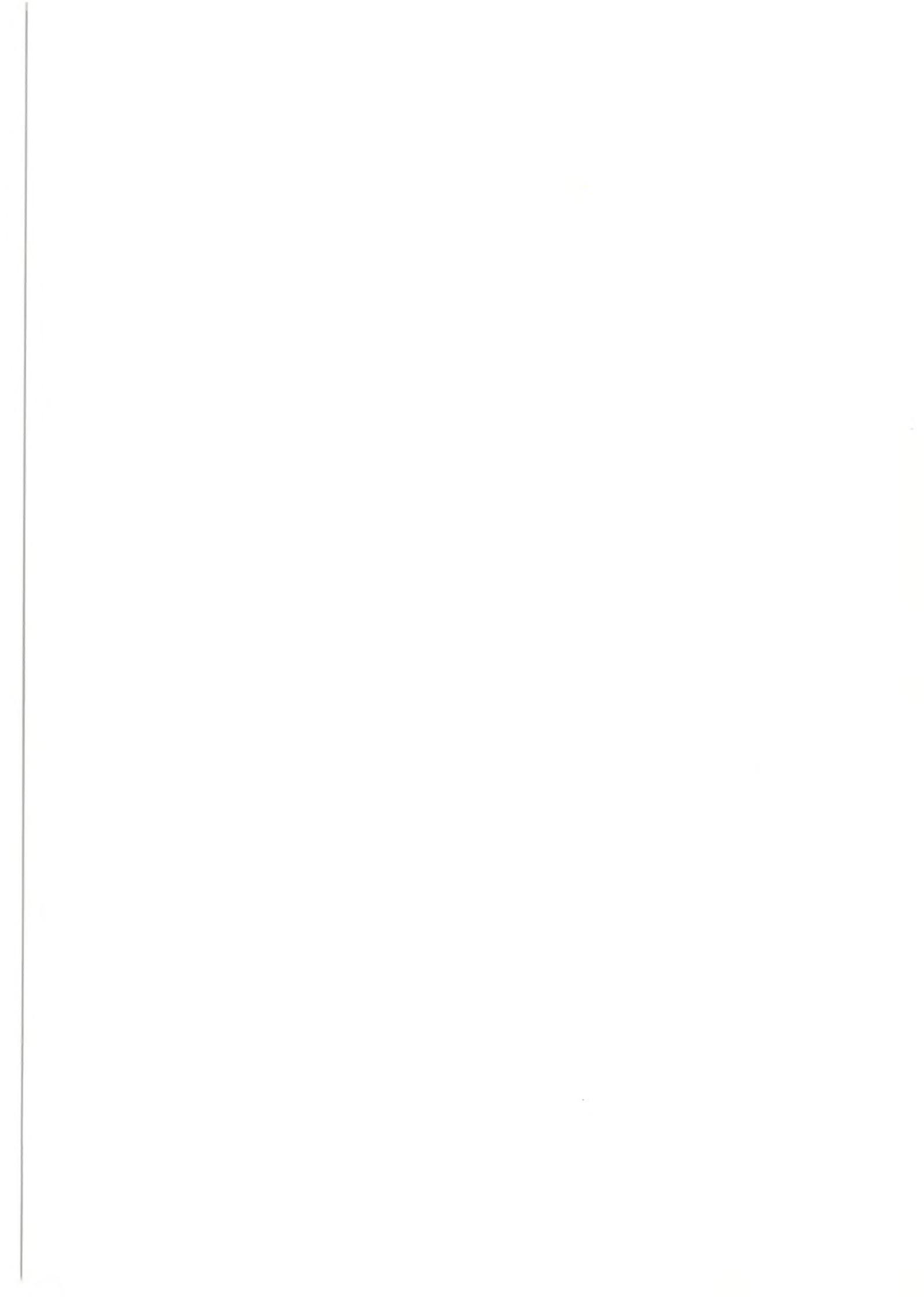
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## Developments in integrated digital signal processors, and the PCB 5010

J. L. van Meerbergen

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*Since computers first appeared on the scene, more than 40 years ago, their dimensions and energy consumption have rapidly diminished, while their performance and capabilities have steadily increased. Even the vast numbers of calculations per second required for processing digital signals can nowadays be performed on a very small number of chips, or sometimes just one. This is done with a special type of 'computer': the digital signal processor. Some time ago the author of the article below presented a paper<sup>[\*]</sup> on the developments in this field. At Philips, one recent result of these developments is the PCB 5010 integrated digital signal processor. A general picture of these developments and the PCB 5010 itself are the main topics of this article.*

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### Introduction

For many people, the word 'computer' used to conjure up the standard image of a number of metal cabinets set up in a special room and usually fitted with the well-known magnetic tape units. This picture is changing, however, now that so many of us have home computers and personal computers.

And there seems to be no end to the developments: many users of a Compact Disc player, for example, will not always realize that it contains a special kind of computer for processing the signals. In the near future rather similar devices will also be found in telephones, telephone exchanges, television receivers and all kinds of audio equipment. This will mean the large-scale use of special integrated circuits ('application-specific integrated circuits' or ASICs) designed for digital signal processing. These will include chips designed for one particular application (as in the Compact Disc player, for example) as well as more generally applicable chips, usually known as *digital signal processors* (fig. 1).

The first part of this article gives the general picture of the gradual evolution of the digital signal proces-

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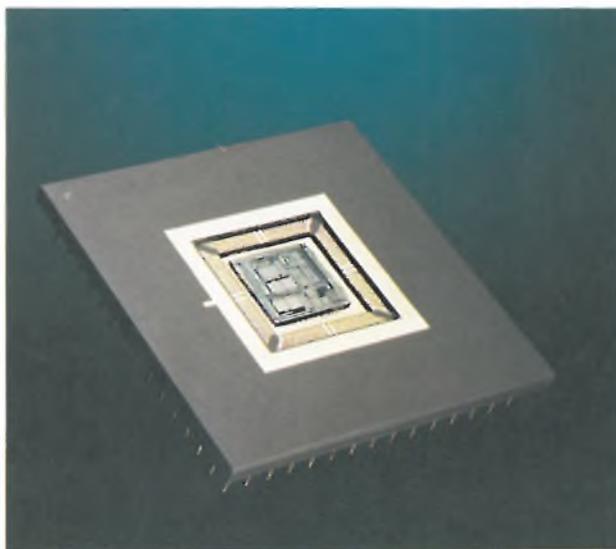


Fig. 1. A digital signal processor is a 'computer on a chip' designed for processing digital signals. These chips contain many tens of thousands of transistors and are designed so that several million typical signal-processing instructions can be executed per second.

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[\*] J. L. van Meerbergen, Architectures and characteristics of commercially available general-purpose signal processors; paper presented at 'Workshop wave digital filters' IMEC, Louvain, Belgium, 1986.

sor. This is followed by a discussion of the PCB 5010 digital signal processor now available from Philips, with attention to its architecture and also to programming facilities and supporting accessories. This signal processor is primarily intended for a wide range of applications in telecommunications, audio and speech-processing.

### The architecture of computers

Every computing process can be broken down into four elementary operations:

- the input and output of data;
- storage in a memory (of data, intermediate results, final results, and computation procedures or algorithms);
- the execution of the computations;
- the control of the entire process.

This functional division has been of great importance in the design of computers from the earliest days. The

Data, memory addresses and instructions were exchanged in turn via this 'main route'. This is generally referred to as a *von Neumann* architecture (fig. 2). It was the standard computer design for many years, first for the large 'main-frame' computers, and later for minicomputers and microcomputers too. In microcomputers the central processing unit consisted of only a few chips, and was soon to consist of only one — the microprocessor.

Signal processing was performed on main-frame computers right from the start, and efforts were soon made to use microprocessors in the same way. Hopes were expressed that it would be possible to process signals 'in real time', and ultimately on a single chip, so that all the advantages of digital signal processing<sup>[2]</sup> would become available for countless applications.

It was soon realized, however, that in some ways the ordinary microprocessor was not so suitable for this purpose and that it was necessary to adapt the de-

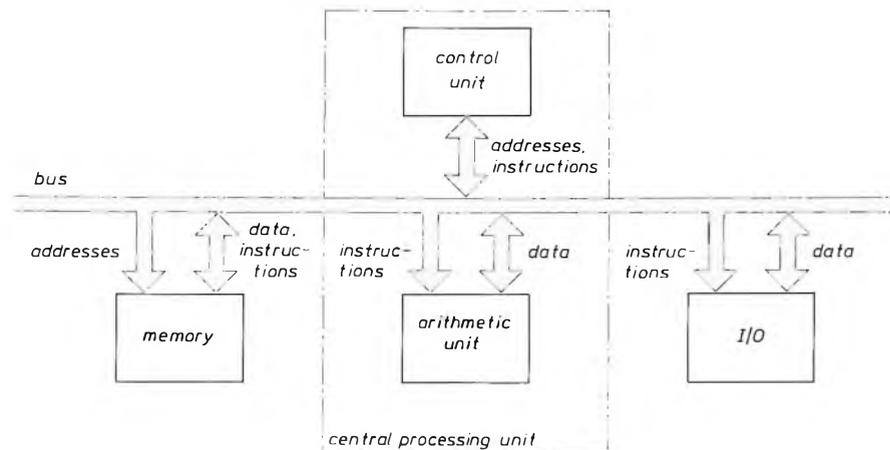


Fig. 2. One of the oldest and best-established forms of computer architecture is the von Neumann architecture shown here. All communication between the main parts of the computer (memory, arithmetic unit, input and output devices I/O, control unit) goes via a single common route: the bus.

four different functions have been performed more or less independently, by:

- input and output (I/O) devices;
- a memory;
- an arithmetic unit;
- a control unit.

The interconnection of the individual devices or units in a specific pattern determined the ultimate architecture of the computer<sup>[1]</sup>. Originally a single common provision was made for the interconnections: a *bus*. All communication between the different parts of the computer was made via the bus in successive steps.

sign more specifically to signal processing. The chips that resulted from this development are referred to as digital signal processors. Almost without exception, the first types commercially available had the original von Neumann architecture.

### Digital signal processors

So just how do digital signal processors differ from microprocessors? In the first place, a signal processor has to be capable of performing very large numbers of operations per unit time. The exact number depends

directly on the bandwidth of the signals to be processed. At present the most advanced signal processors can handle signals with a bandwidth of up to several tens of kilohertz; integrated signal processors for general applications with video signals are still a thing of the future.

One of the most common digital operations is the multiplication of pairs of numbers from two sequences and the addition of the products, such as

$$y = \sum_{i=1}^N a_i x_i.$$

(Incidentally, this is equivalent to calculating the scalar product of two  $N$ -dimensional vectors.) Operations of this type are found in algorithms for filtering, correlation, spectral analysis, etc. To perform them reasonably quickly the arithmetic unit must include a multiplier/accumulator combination or MAC (*fig. 3*). This can compute one subproduct  $a_i x_i$  in the smallest unit of time present in the signal processor (one *clock cycle* or *machine cycle*) and at the same time add the previous subproduct  $a_{i-1} x_{i-1}$  to the sum already calculated from all the earlier subproducts. The presence of a MAC is in itself a distinctive difference as compared with the original microprocessors. Much more radical changes in the architecture are required, however, if we are to obtain signal processors that are fast enough; this aspect will be dealt with at some length in the following sections.

The maximum processing rate of a signal processor is also affected by the number of chips used; as the

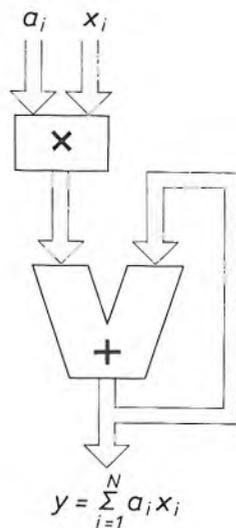


Fig. 3. In digital signal processing it is often necessary to sum  $N$  products of the type  $a_i x_i$ . This takes a disproportionate amount of time in the von Neumann architecture shown in fig. 2. The situation can be improved by providing the arithmetic unit with a multiplier/accumulator combination as shown here.

number of chips diminishes less time will be lost in transferring the signals. As well as an arithmetic unit and a control unit, signal processors must therefore also contain memory facilities. These consist of a ROM (Read-Only-Memory) for storing unchanging quantities, such as the program and constant values, and a RAM (Random-Access Memory) for storing intermediate and final results. The versatility of application is considerably increased if these on-chip memories can be supplemented by external storage as required.

Since the input signals will often be analog in origin and signal processors are digital devices, analog/digital (A/D) conversion will frequently be encountered as a preliminary operation and D/A conversion as a final operation. In one type of signal processor (the Intel 2920) the converters are present on the chip as part of the input/output devices. In general, however, it seems preferable (at least in the present state of the technology) to add the converters to the signal processor as separate components. The specific requirements of individual applications, which can vary considerably, are then more easily taken into account.

### The architecture of signal processors

The basic von Neumann architecture has one serious disadvantage: everything happens *consecutively*. Before any one operation is completed, many steps (often very many) have to be completed. For example:

- the location (the 'address') where the next instruction is stored in the memory is determined (e.g. by adding 1 to the previous address);
  - the instruction is read from the memory and transferred to the control unit;
  - the instruction is interpreted ('decoded');
  - the address of data necessary for executing the instruction is sent to the memory;
  - the data is sent from the memory to the arithmetic unit;
  - the arithmetic unit then executes the instruction;
  - the result of the instruction is stored in the memory.
- Then the complete cycle (the *instruction cycle*), which clearly requires more than one *machine cycle*, may be repeated.

The component that restricts the speed most of all is the one most characteristic of the von Neumann structure — the common signal bus, which handles every exchange of information between the various

<sup>[1]</sup> The combination of the arithmetic unit and the control unit is often called the central processing unit.

<sup>[2]</sup> J. B. H. Peek, Digital signal processing—growth of a technology, 103-109, in the special issue 'Digital signal processing I, background', Philips Tech. Rev. 42, 101-144, 1985.

parts of the processor. It acts as a bottleneck. For higher speeds it is necessary to change to a 'non-von Neumann' architecture (sometimes just called a 'non-von' architecture).

The most common alternative is the Harvard architecture, in which data and instructions are stored in separate memories and which therefore has to have separate connections for data and control information. This gives the architecture shown in *fig. 4*, where the signal processor is divided into two parts, called the controller and the data path. The exact nature of the connections *between* these two parts is mostly of less importance.

### The architecture of the PCB 5010

The design of our PCB 5010 signal processor is based on the Harvard architecture of *fig. 4*. It has been modified in some essential aspects, however, to obtain sufficient versatility and signal-processing capacity.

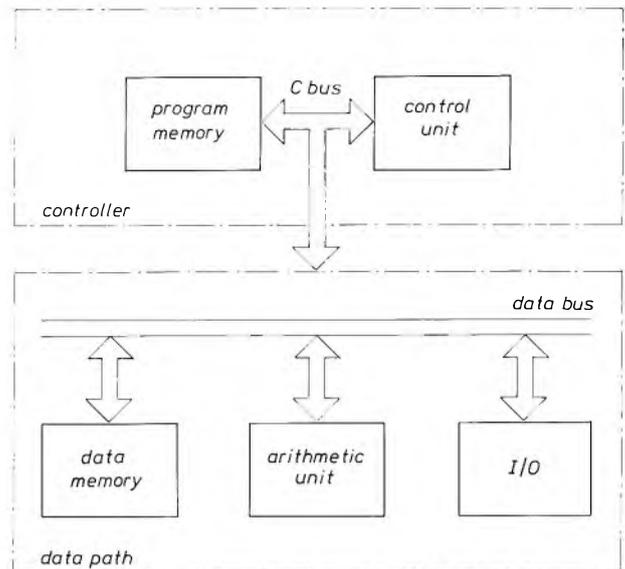
One of the main modifications is the duplication of the data bus, resulting in an X bus and a Y bus, each 16 bits wide<sup>[3]</sup>. The reason for this is that most signal-processing operations have two operands and can only be performed efficiently with a duplicated data bus. There is also the advantage that complex numbers can be more easily manipulated with a duplicated bus. As a direct consequence of this duplication, the RAM for the data is divided into two parts. A separate ROM is also available for data.

As we have seen, every signal processor has to have a multiplier/accumulator combination *MAC* to reach the speed required in the many 'vector-like' operations that arise. High-speed processing is also required for other types of operation, such as logic AND, NOT, OR etc., for operations on absolute values and for operations on individual bits ('masks'). The PCB 5010 has a separate arithmetic and logic unit *ALU* for these activities.

Finally, to facilitate data input and output our signal processor has two serial input devices and two serial output devices, as well as a combined parallel input/output device. This brings us to the block diagram<sup>[4]-[6]</sup> of the PCB 5010 in *fig. 5*.

A computer drawing of the actual plan of the PCB 5010 is shown in *fig. 6*; the numbers 1 to 5 refer to the main components in the previous figure. There are some 135 000 transistors in all in this drawing, yet this IC only occupies an area of 61 mm<sup>2</sup> when fabricated in 1.5- $\mu$ m CMOS technology.

In the following sections of this article we shall take a closer look at the structure of the controller and of the two principal components of the data path: the



*Fig. 4.* A modern alternative to the von Neumann architecture is the Harvard architecture shown here. This has separate memories for the program and the data, and separate connections for the control information and the data. These connections are called the control bus (or C bus) and the data bus. The total architecture can now be divided into two parts, called the controller and the data path.

data memory and the arithmetic unit. We shall see that in each of these components every effort is made to decentralize as many activities as possible to prevent bottlenecks, e.g. by providing a separate address-computation unit for each memory.

Besides the architecture, various other aspects are important in assessing the performance of a signal processor. They include:

- the time (in seconds and in number of machine cycles) required for executing an instruction;
- the number of (sub)operations that can be performed simultaneously;
- facilities for interaction with the outside world;
- the possible degree of overlap in time of executions of successive instructions in different parts of the signal processor ('pipelining').

These all depend greatly on the way in which the signal processor can be programmed (the 'microcode'). We shall return to this point later.

The ultimate critical factor in comparing signal processors is the time required for performing a num-

<sup>[3]</sup> F. P. J. M. Welten *et al.*, A 2- $\mu$ m CMOS 10-MHz microprogrammable signal processing core with an on-chip multiport memory bank, *IEEE J. SC-20*, 754-760, 1985.

<sup>[4]</sup> J. L. van Meerbergen *et al.*, A 2- $\mu$ m CMOS 8-MIPS digital signal processor with parallel processing capability, *Int. Solid State Circ. Conf. (ISSCC)*, Digest of technical papers, Anaheim, Cal. 1986.

<sup>[5]</sup> F. J. van Wijk *et al.*, A 2 $\mu$ m CMOS 8-MIPS digital signal processor with parallel processing capability, *IEEE J. SC-21*, 750-765, 1986.

<sup>[6]</sup> Introducing the PCB 5010/PCB 5011 programmable DSPs, Philips Electronic Components and Materials Division, Eindhoven 1986 (16 pages).

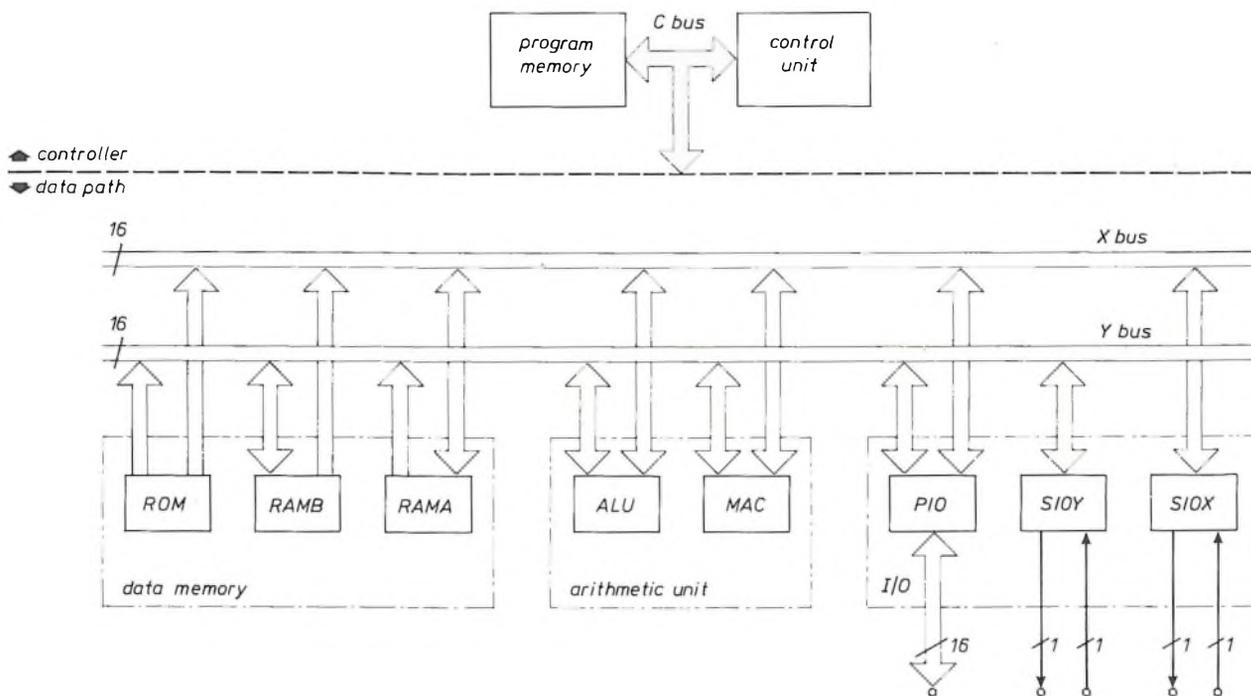


Fig. 5. The PCB 5010 digital signal processor has a Harvard architecture with two independent 16-bit data buses: the X bus and the Y bus. The data memory consists of three parts: a ROM (read-only memory) for unchanging data and two RAMs (random-access memories) RAMA and RAMB. The arithmetic unit consists of two parts: a multiplier/accumulator combination MAC and an arithmetic and logic unit ALU. The input and output devices I/O consist of a parallel unit PIO, which has a 16-bit connection to the outside world, and two serial units SIOX and SIOY, each with a 1-bit input and a 1-bit output.

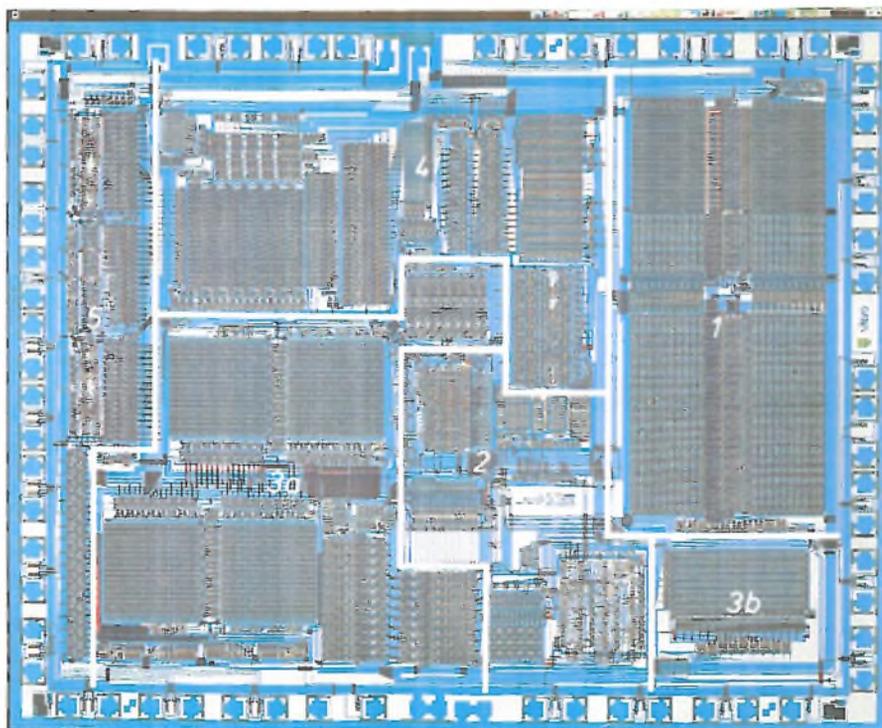


Fig. 6. Computer drawing of the integrated digital signal processor PCB 5010. The most important components are: 1 program memory; 2 control unit; 3a, 3b data memory; 4 arithmetic unit; 5 input and output devices I/O. The complete circuit contains some 135 000 transistors and is fabricated in 1.5- $\mu\text{m}$  CMOS technology. It occupies an area of 61 mm<sup>2</sup>.

ber of standard operations at a given accuracy. Typical operations might be a 128-point FFT ('Fast Fourier Transform'), a complex multiplication or a particular elementary filtering operation. These operations are often called 'benchmarks'.

### The arithmetic unit

#### The multiplier/accumulator combination MAC

Fig. 7. shows a block diagram of the multiplier/accumulator with its various supporting devices. The operation of multiplier *MPY* is based on the 'modified

Booth's algorithm'<sup>[7]</sup> and in one machine cycle it can compute the product of two 16-bit words *P* and *Q*. The product is stored temporarily as a 32-bit word in the product register *PR*. At the same time the accumulator *ACC* can add the previous contents of *PR* to the contents of the accumulator register *ACR*. The contents of *ACR* are then multiplied, under the control of the block *S/SD*, either by 1,  $-1$ ,  $-2^{-15}$ ,  $2^{-15}$  or by 0. The output of the accumulator has a width of 40 bits, so that even if large numbers of products are added together, there are no overflow errors.

The 'barrel shifter', *BS*, the corresponding barrel-shift register *BSR* and the format adjuster *FA* derive one group or two groups of 16 bits from the 40-bit contents of *ACR* to form the output signal of the *MAC* unit.

The operands *P* and *Q* presented to *MPY* may come directly from the X bus and the Y bus via the X and Y input selectors *ILX* and *ILY*. It is also possible to select the previous X and Y information, which is automatically stored in the latches *MXL* and *MYL*. In addition, *P* can take the value  $-1$ , and *Q* the logically inverted value of the current Y information.

Certain special occurrences, such as overflow in *ACC*, are reported directly to the control unit by means of a 'flag' or 'flag signal'.

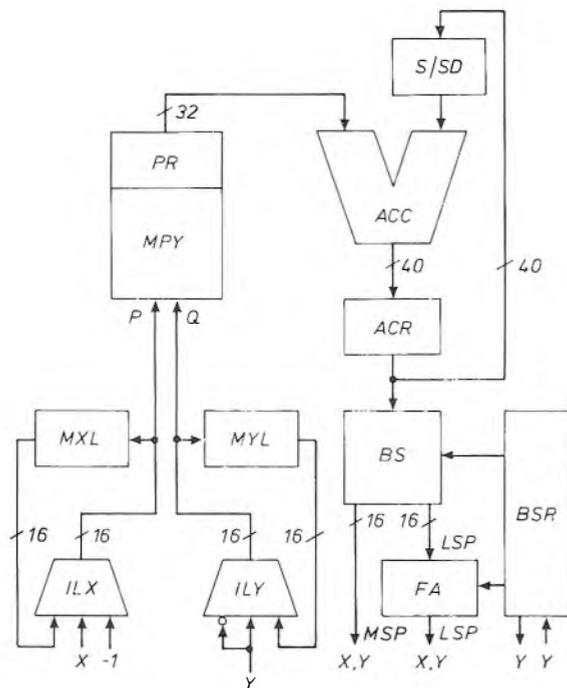


Fig. 7. Block diagram of the multiplier/accumulator combination *MAC* of the PCB 5010. The number of operations that can be performed in each machine cycle has been greatly increased by the addition of extra registers and selectors. The operations required are specified by a 7-bit code via the C bus (not shown explicitly). The numbers beside the oblique strokes in the connections indicate how many bits are transferred in parallel. The significance of the designations is:

<i>ACC</i>	accumulator
<i>ACR</i>	accumulator register
<i>BS</i>	barrel shifter
<i>BSR</i>	barrel-shift register
<i>FA</i>	format adjuster
<i>ILX</i>	X-input selector
<i>ILY</i>	Y-input selector
<i>LSP</i>	least-significant part
<i>MPY</i>	multiplier
<i>MSP</i>	most-significant part
<i>MXL</i>	X latch
<i>MYL</i>	Y latch
<i>P</i>	operand 1
<i>PR</i>	product register
<i>Q</i>	operand 2
<i>S/SD</i>	sign/scale-down block
<i>X</i>	16-bit connection to the X bus
<i>Y</i>	16-bit connection to the Y bus

#### Multiplication with greater precision

Blocks *S/SD*, *BS*, *BSR* and *FA* are also important because they permit calculations to be made at a greater precision than 16 bits, though at the expense of more processing time. For example, the product of a 46-bit operand and a 31-bit operand can be computed in 7 machine cycles at most<sup>[8]</sup>. This is done in much the same way as multiplying two large numbers together conventionally: subproducts are determined first, then shifted appropriately and added.

#### The arithmetic and logic unit ALU

A block diagram of the arithmetic and logic unit *ALU* of the PCB 5010 is shown in fig. 8. Grouped around the logic unit *LU*, which can perform operations on a single operand *A* or on two operands *A* and *B*, there are a number of registers and other supporting devices.

A total of 31 different arithmetic and logic operations can be executed, including addition, subtraction, absolute-value determination, AND, OR, NOT and shift operations. The selectors *ILA* and *ILB* permit either the current information on the X and Y buses to be used for *A* and *B*, or the previous information, which is always automatically stored in the latches *AAL* and *ABL*.

At the output of *LU* a set of 15 registers are available for temporary storage. During each machine cycle the present result of *LU* can be stored in one of these registers, and the contents of any other two registers can be read out via the X bus and the Y bus.

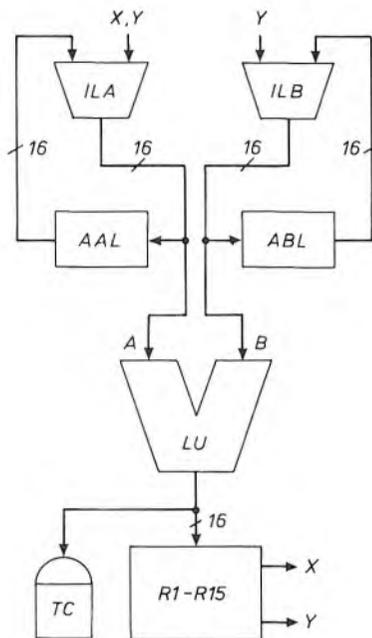


Fig. 8. Block diagram of the arithmetic and logic unit *ALU* of the PCB 5010. As well as two selectors and two latches, this unit contains a file of 15 independent 16-bit registers. The operations required from *ALU* are specified in each machine cycle by a 7-bit code via the C bus. Also, 4 bits are reserved on the C bus for selecting one of the registers from the register file. The significance of the designations is:

<i>A</i>	operand 1
<i>AAL</i>	A latch
<i>ABL</i>	B latch
<i>B</i>	operand 2
<i>ILA</i>	A-input selector
<i>ILB</i>	B-input selector
<i>LU</i>	logic unit
<i>R1-R15</i>	register file
<i>TC</i>	trash can
<i>X</i>	16-bit connection to the X bus
<i>Y</i>	16-bit connection to the Y bus

The arithmetic and logic unit *ALU* can send status information directly to the control unit of the signal processor by means of flags, (e.g. about overflow or the sign of the computed result). If just this status information is to be stored, the rest of the computed result is consigned to the 'trash can' *TC*.

If required, *ALU* can perform computations to a higher precision than 16 bits, but again it will take longer for the processing.

The units *MAC* and *ALU* are to some extent complementary. *MAC*, for instance, is designed for processing 16-bit words (and hence for vector operations), while *ALU* is particularly suited for processing individual bits. There are seven types of instructions for *MAC*, all concerned with multiplication and addition, while *ALU* has 31, some very different from the others. Finally, in *MAC* there is always room for intermediate and final results with a maximum length of 40 bits; in *ALU* the length is always 16 bits, unless special arrangements are made. These differences are summarized in *Table I*.

Table I. Comparison of some complementary features of the multiplier/accumulator combination *MAC* and the arithmetic and logic unit *ALU*.

<i>MAC</i>	<i>ALU</i>
Designed for vector operations (16-bit word level)	designed for other operations (bit level)
7 slightly different instructions (all connected with adding and multiplying)	31 sometimes very different instructions (such as AND, OR, NOT, EXOR, shifting, addition, subtraction, incrementing)
Gives 40-bit intermediate result and 40-bit final result (can be extended)	gives 16-bit result (can be extended)

### The data memory

As already mentioned, three memories are provided for storing all the various data required during the operation of the signal processor. One memory with 512 locations, each of 16 bits, stores unchanging data, such as constants and filter coefficients, and is therefore a ROM. This data is entered into the memory once only, during manufacture. The other two are RAMs; these store intermediate or final results. They each have 128 memory locations of 16 bits (*fig. 9*). Each of the three memories has its own output-data register (*DRR*, *DRB* and *DRA*).

To keep the capacity of the arithmetic unit and the X and Y buses of the signal processor free as far as possible for the actual signal-processing operations, each of the three memories has its own address-computation unit, or ACU, denoted by *ACUR*, *ACUB* and *ACUA*. During each machine cycle a new mem-

[7] A very good short description of this algorithm is given in: L. P. Rubinfeld, A proof of the modified Booth's algorithm for multiplication, IEEE Trans. C-24, 1014-1015, 1975.

[8] The length of the operands is not quite an integer multiple of 16, because one bit in each group of 16 is always reserved as a sign bit, and the length can only increase effectively by multiples of 15, thus: 16, 31, 46, ...

ory address can be computed in an ACU from the old address and some additional data. For example, a fixed number can be added to the previous address. If this is a 'modulo- $N$ ' addition, the data memory is scanned repeatedly in a fixed pattern, which is very useful for repetitive look-up of filter coefficients. Another possible operation is the reversal of the order of the address bits, which facilitates the calculation of Fast Fourier Transforms.

In both *RAMA* and *RAMB* the computed addresses are longer than is necessary for addressing 128 differ-

ent locations. As *ACUB* supplies an 8-bit address, a later version of this signal processor can thus have a larger *RAMB* with 256 locations. *ACUA* supplies a 12-bit address, which is also available at the connector pins of the signal processor for addressing an external memory. It can be extended by 4 bits from a page register *PG* to form a 16-bit address, so that an external data memory with 64k (= 65 536) locations can be used.

### The controller

The controller is the 'brain' that directs the entire operation of the signal processor. It determines what happens in the signal processor in each individual machine cycle. The program memory is of major importance here. It stores all the possible instructions for all the components of the signal processor. These instructions have a fixed length of 40 bits. The program memory of the PCB 5010 can contain 1024 such instructions (992 in a ROM and 32 in a RAM). The instructions stored in the ROM are entered permanently when the signal processor is manufactured; the instructions in the RAM can be changed at any time. During each machine cycle a 40-bit instruction is entered into the instruction register *IR* (fig. 10), and the various sub-instructions are then distributed over the entire chip. A part of some instructions goes straight to the X bus and the Y bus ('load immediate', see the section on the microcode); the rest of the information in the instructions goes to the various parts of the signal processor via connections that we shall not consider further here (the C bus). At the same time the program counter *PC* determines the next address for the program memory.

For certain frequently occurring types of program special provisions have been made. A particular instruction may have to be repeated  $N$  times, and a separate instruction-repeat register (*RPR*) is available for such operations. While this is in use, the contents of the program counter *PC* remain unchanged. Other regularly occurring events include interruptions and the execution of subroutines. The current program is then stopped for a moment, and this is noted in a 'stack register', so that the program can be resumed later. The stack register has five levels, but if required it can be extended by a part of one of the data memories described in the previous section. The stack register enables other subroutines and interruptions to be processed inside a subroutine.

Since the controller represents the 'nerve centre' of the signal processor, it has many connections to the outside world and other parts of the chip. We have already encountered several examples, such as the capa-

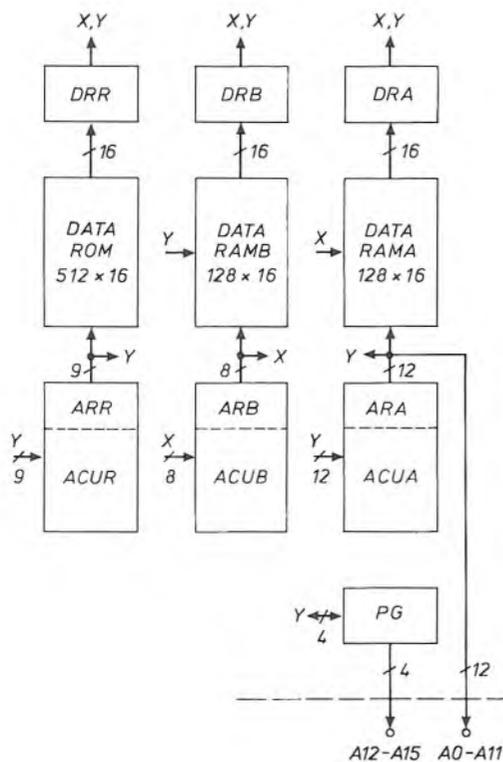


Fig. 9. Block diagram of the three data memories of the PCB 5010. Each memory has its own address-computation unit and its own output-data register. The 12-bit address of one of the two RAMs is also available externally. If this address is extended by an extra 4 bits from a page register, an external data memory with 64k (=  $2^{16}$ ) memory locations can be used. In each machine cycle for each of the address-computation units three bits of information are reserved on the C bus. The significance of the designations is:

<i>ACUA</i>	address-computation unit A
<i>ACUB</i>	address-computation unit B
<i>ACUR</i>	address-computation unit R
<i>ARA</i>	address register A
<i>ARB</i>	address register B
<i>ARR</i>	address register R
<i>A0-A15</i>	address bits 0-15
<i>DRA</i>	output-data register A
<i>DRB</i>	output-data register B
<i>DRR</i>	output-data register R
<i>PG</i>	page register
<i>RAMA</i>	random-access memory A
<i>RAMB</i>	random-access memory B
<i>ROM</i>	read-only memory
<i>X</i>	16-bit connection to the X bus
<i>Y</i>	16-bit connection to the Y bus

bility for external interruption of a current program. Clock-synchronization signals and any reset signals also reach the controller from outside. Status information about the various components of the signal

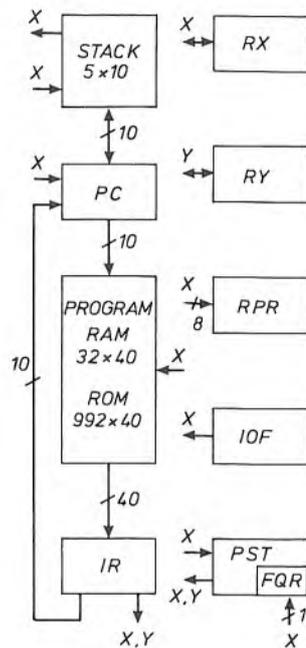
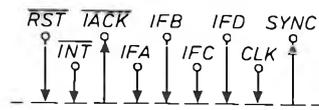


Fig. 10. Block diagram of the controller of the PCB 5010, consisting of the program memory and the control unit. The program memory is mostly read-only, with a small random-access section. The memory address is supplied by the program counter. The contents of the program memory are written to the 40-bit instruction register, and from there the information is distributed via the C bus (not shown) and some of it possibly also via the X bus and the Y bus. The control unit consists mainly of a number of registers that serve a variety of purposes. The arrows at the top indicate that the control unit can exchange certain information with the outside world. The significance of the designations is:

<i>CLK</i>	clock
<i>FQR</i>	mode bit (P mode/NP mode)
<i>TACK</i>	acknowledgment
<i>IFA</i>	user flag A
<i>IFB</i>	user flag B
<i>IFC</i>	user flag C
<i>IFD</i>	user flag D
<i>INT</i>	interrupt signal
<i>IOF</i>	input/output status and user flag register
<i>IR</i>	instruction register
<i>PC</i>	program counter
<i>PST</i>	processor-status register
<i>RAM</i>	random-access memory
<i>ROM</i>	read-only memory
<i>RPR</i>	instruction-repeat register
<i>RST</i>	reset signal
<i>RX</i>	X register
<i>RY</i>	Y register
<i>STACK</i>	stack register
<i>SYNC</i>	synchronization signal
<i>X</i>	16-bit connection to the X bus
<i>Y</i>	16-bit connection to the Y bus

processor is always stored in the 16-bit processor-status register *PST* in the form of 1-bit flag signals. Similarly the register *IOF* contains input/output flags that indicate the status of the input and output circuits of the processor, and four user flags that originate outside the chip. Finally, the controller contains two registers, *RX* and *RY*, that save the signals on the X bus and the Y bus if there is an interruption.

### General diagram

A block diagram giving a general picture of the component parts of the PCB 5010 signal processor discussed above is shown in fig. 11. The numbers beside the interconnections indicate the number of parallel bits. The symbols *X* and *Y* indicate a direct connection to the X bus and the Y bus. Some connections to the outside world are also indicated (the chip is in an encapsulation with 68 connector pins). The internal connections for control purposes (the C bus) are not shown, however.

### Programming

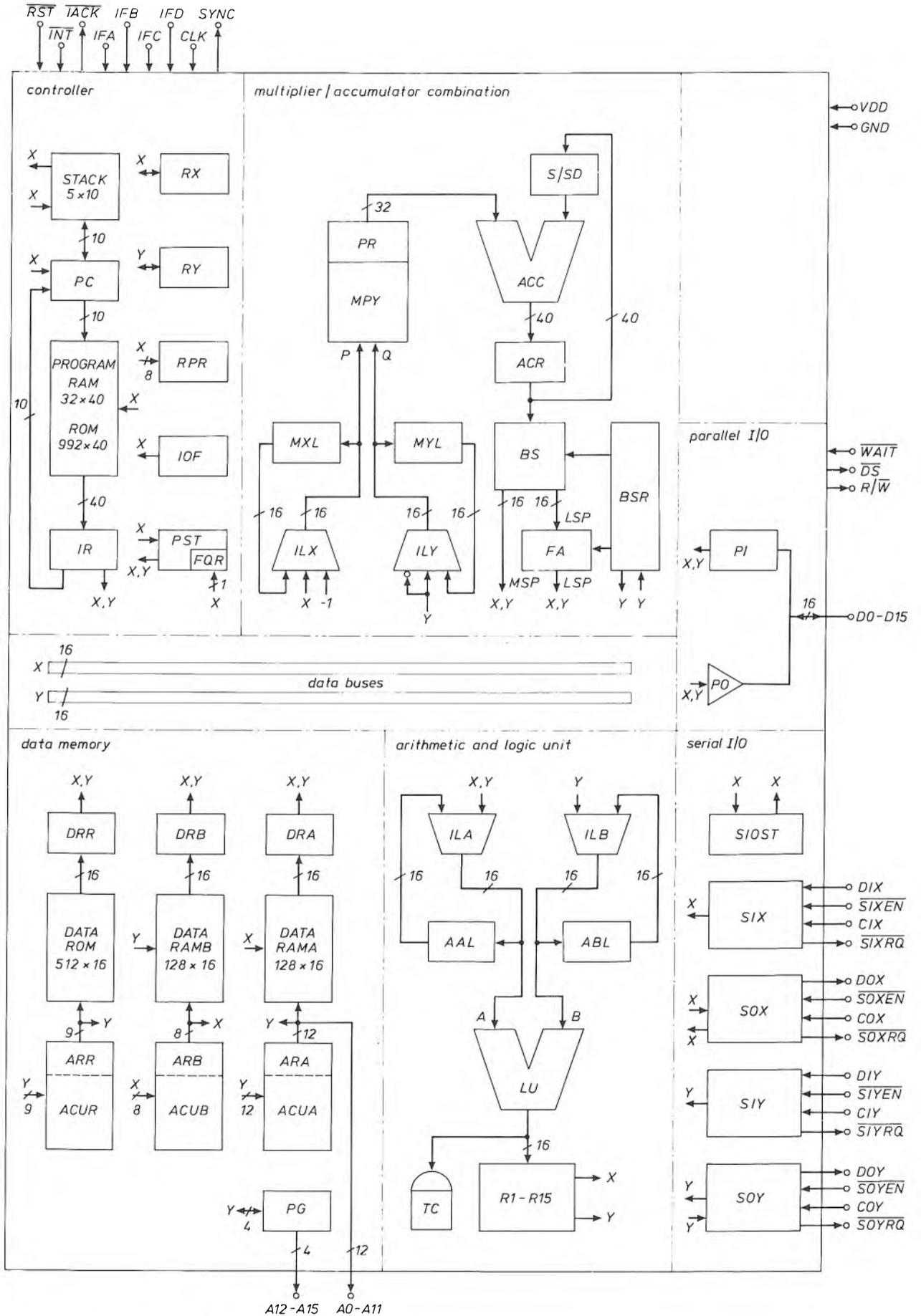
The architecture of signal processors has been discussed at some length above, because it very largely determines the *theoretical* processing capabilities of the signal processor, such as the maximum available degree of parallelism. The *actual* processing capacity is also very dependent, however, on the 'programmability' of the processor. This can be deduced from the structure and diversity of the instructions (the 'microcode') that can be used to program the chip. Another extremely important point here is the amount of effort required from the user to translate a particular required function into a processing program (an algorithm) and hence into a sequence of basic instructions. This is mainly determined by two factors:

- the 'transparency' of the microcode;
- the facilities available for creating, testing and correcting a processing program.

We shall now look first at the microcode itself, and then at the available facilities.

### The microcode

The PCB 5010 works with 40-bit instructions and a machine cycle time of 125 ns. In the *pipeline mode* (the P mode) each machine cycle corresponds to a single instruction; in the *non-pipeline mode* (the NP mode) the instructions follow one another at regular intervals of two machine cycles (we shall return to this point later). Each instruction represents one or more basic operations. In one machine cycle, for example,



◁ Fig. 11. General diagram of the PCB 5010, produced by combining the block diagrams from the four previous figures and adding the data buses and the input and output devices. The significance of the designations not given earlier is:

<i>CIX, CIY</i>	X, Y input clock
<i>COX, COY</i>	X, Y output clock
<i>DIX, DIY</i>	serial X, Y input
<i>DOX, DOY</i>	serial X, Y output
<i>DS</i>	data strobe
<i>D0-D15</i>	parallel input/output
<i>GND</i>	ground
<i>PI</i>	parallel-input latch
<i>PO</i>	parallel-output latch
<i>R/W</i>	read/write
<i>SIOST</i>	serial I/O control register
<i>SIX, SIY</i>	serial X, Y input latch
<i>SIXEN, SIYEN</i>	X, Y input enable
<i>SIXRQ, SIYRQ</i>	X, Y input request
<i>SOX, SOY</i>	serial X, Y output latch
<i>SOXEN, SOYEN</i>	X, Y output enable
<i>SOXRQ, SOYRQ</i>	X, Y output request
<i>VDD</i>	supply voltage
<i>WAIT</i>	wait signal

the following basic operations can be performed simultaneously:

- calculation of the product of two 16-bit numbers;
- addition of the previous product in the accumulator;
- data transfer via the X bus;
- data transfer via the Y bus;
- three address computations in *ACUA*, *ACUB* or *ACUR*.

The basic operations available are not always the same, however. There are four different types of instruction, as shown schematically in *fig. 12*. The two bits on the far left indicate the type of instruction. The  $3 \times 3$  bits of each instruction on the far right indicate the operations to be carried out in *ACUA*, *ACUB* and *ACUR*.

The instructions of types 0 and 1 are very similar; the difference is that one type has a 7-bit sub-instruction for the arithmetic and logic unit and the other has a 7-bit sub-instruction for the multiplier/accumulator combination. Both types of instruction also contain two groups of 5 bits (*SX* and *SY*), which indicate the source of the information on the X bus and the Y bus. Finally, there are three groups of 4 bits (*DX*, *DY* and *RFILE*), which indicate the destinations of the information on the X bus, on the Y bus and at the output of *LU*.

An instruction of type 2 in *fig. 12* is called a branch operation. The three bits of *BR* indicate the type of branch in the program; the six bits of *COND* indicate the condition for making the branch, and the sixteen bits of *NAP* determine the new address that the branch leads to in the program memory.

Instruction type 3 can be used to feed a group of 16 bits directly to the X bus and the Y bus as new data; this is called a 'load immediate' instruction.

Since the sub-instructions always have a fixed location, programming is greatly simplified. For example,

instruction type 0:

39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	ALU					AOPS					SX					SY					DX				DY				RFILE				ACUA		ACUR		ACUB	

instruction type 1:

39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	MPY					MOPS					SX					SY					DX				DY				RFILE				ACUA		ACUR		ACUB	

instruction type 2:

39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	NAP																BR			COND			—				ACUA		ACUR		ACUB							

instruction type 3:

39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	DATA																DX				DY				RFILE				ACUA		ACUR		ACUB					

Fig. 12. The PCB 5010 operates with instructions of four types. Each instruction consists of 40 bits, numbered here from 0 to 39. The bits numbered 38 and 39 indicate the type. The instructions are individually divided into segments of from 2 to 16 bits. Each segment represents a sub-instruction and is indicated by one of the letter combinations listed here:

<i>ACUA</i>	type of ACUA operation	<i>DY</i>	destination on Y bus
<i>ACUB</i>	type of ACUB operation	<i>MOPS</i>	multiply operands
<i>ACUR</i>	type of ACUR operation	<i>MPY</i>	type of multiplier/accumulator operation
<i>ALU</i>	type of ALU operation	<i>NAP</i>	address of next instruction if <i>COND</i> is true
<i>AOPS</i>	ALU operands	<i>SX</i>	source on X bus
<i>BR</i>	type of branch operation	<i>SY</i>	source on Y bus
<i>COND</i>	branch condition	<i>RFILE</i>	destination in register file
<i>DATA</i>	16-bit data word transmitted on X bus and Y bus		
<i>DX</i>	destination on X bus		

the entire data stream of a program can be selected and then the corresponding address computations can be determined.

### Accessories

Besides the PCB 5010, there is a very similar processor, the PCB 5011. This has no program memory, however, and no on-chip data ROM; the chip has connector pins for these, so that external memories can be connected to it. The PCB 5011 contains 70 000 transistors, while the PCB 5010 has about 135 000. Fig. 13 is a photograph of the PCB 5011. The left-hand two-thirds of fig. 6 can clearly be identified here. The large number of external connections is also immedi-

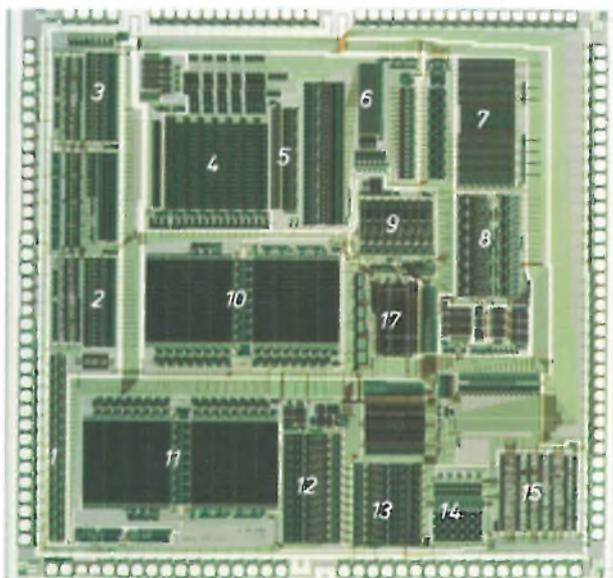


Fig. 13. Photograph of the PCB 5011 digital signal processor. This processor is identical to the PCB 5010 in fig. 6 and fig. 11, except that it does not have the program memory and the data memory ROM. The connections for these go to connector pins, so that external memories can be used instead. The following components are indicated by numbers (the abbreviations are the same as in the previous figures): 1 *PI* and *PO*; 2 *SIX* and *SOX*; 3 *SIY* and *SOY*; 4 multiplier; 5 accumulator; 6 barrel shifter; 7 register file; 8 logic unit; 9 *ACUB*; 10 *RAMB*; 11 *RAMA*; 12 *ACUA*; 13 *ACUR*; 14 *STACK* and *PC*; 15, 16 various components of the control unit; 17 *PST*.

ately obvious: the PCB 5011 has 144, the PCB 5010 'only' 68. (The integrated circuit shown in fig. 1, incidentally, is also of type PCB 5011.)

The PCB 5011 can be used in the design or development phase of a system (before any final decision has been made about the contents of the ROM in the PCB 5010), in applications where it is not worth

making a special version of the PCB 5010 with ROMs specified by the user, and in applications where a very large program memory is required.

To facilitate the use of the PCB 5010/PCB 5011 special software has been written in the programming language PASCAL. This can be used on several widely used computers (VAX, IBM-PC). In the first place there is a *simulator program*, which can simulate the entire operation of a signal processor programmed for a specific application. There is also an *assembly program* that makes it unnecessary to specify the contents of the instructions bit by bit, requiring only symbolic indications that can be handled more readily (i.e. groups of letters — 'mnemonics' — that look like abbreviations). In this program these are automatically translated into bit sequences. The program also contains a *macro library*, in which frequently occurring algorithms, such as certain kinds of filtering and FFT operations, are stored in 'macrocode' as ready-to-use subroutines for the signal processor.

To test a system in which the PCB 5010/PCB 5011 is used under realistic conditions, e.g. in real time, the 'Stand-alone Debug System' (SDS) can be used. The SDS is an *emulator*, i.e. a device that functions in exactly the same way as a later definitive version of the PCB 5010, but also has a variety of facilities for interrupting a program being run in the signal processor at any moment and for investigating the internal status of the signal processor at that moment. Program modifications are also easily made.

Finally, there is a *prototype board* containing the PCB 5011 and all the external memories and circuits required for loading these memories. This board can be used, for example, for making a prototype of a system that will later include one or more PCB 5010 chips.

### Applications

The PCB 5010 has its greatest signal-processing capacity when it is used in the pipeline mode: in pipelining a new operation starts while the last part of the previous operation is still being performed at another location on the chip during the same machine cycle. This is done in product accumulation, for example. A single product accumulation really takes two machine cycles, but by pipelining the multiplication part and the addition part the effective duration is only about one machine cycle in long sequences of product accumulations. Programming in the pipeline mode is rather more difficult than in the non-pipeline mode. It is therefore possible to select one of the two modes and even to switch from one to the other within the same signal-processing program.

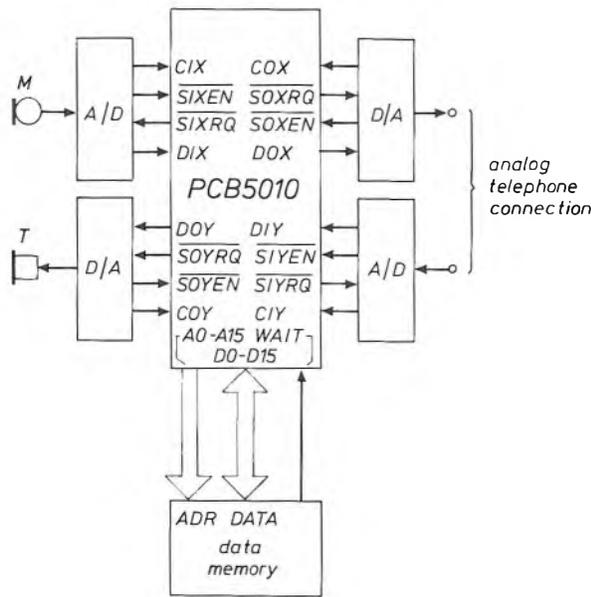


Fig. 14. Example of the application of the PCB 5010 in telecommunications. The figure shows how the signal processor can be used in an analog telephone connection: after addition of a telephone *T*, a microphone *M* and A/D and D/A converters, a single PCB 5010 can perform all the processing operations required for transmitting and receiving. It can also be seen how the internal data memory *RAMA* can be replaced by an external memory.

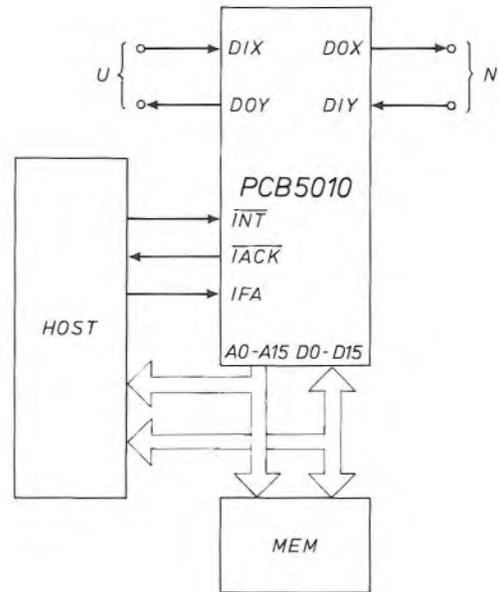


Fig. 15. A PCB 5010 can be controlled from an external microprocessor *HOST* in combination with an external data memory *MEM*. The example shown here relates to a terminal in a telecommunication system; the PCB 5010 links the user *U* to the rest of the network *N*.

The PCB 5010 can be used in a variety of system configurations; in a minimum configuration only A/D and D/A converters have to be added. In many communication applications incoming and outgoing signals can even be processed effectively simultaneously (fig. 14). It is also possible to use an external microprocessor to control the signal processor; this makes it even more versatile (fig. 15). Also, since the PCB 5010 chips have extensive input/output facilities, they can easily be combined to form a multiprocessor system suitable for more demanding applications (fig. 16).

Just how powerful the PCB 5010/PCB 5011 signal processors are can be seen most clearly from the time required to execute a number of characteristic processing operations. A summary of these is given in Table II. Unless otherwise stated, the information in this Table relates to 16-bit quantities, for both signal samples and filter coefficients. In the examples relating to the Fast Fourier Transform (FFT) 'looped code' processing programs were used. This reduces the number of steps in the program to only about 40. It is also possible to halve the time required by using 'straight-line code', which avoids program loops. However, this requires about 100 times the number of program steps, and therefore about 100 times the memory capacity<sup>[5]</sup>. With the processing times given in Table II, the processors can be used for many applications in the fields for which they were originally devel-

oped: telecommunications (especially in telephony)<sup>[9]</sup>, audio and many kinds of speech-processing (such as speech coding, voice recognition and speaker identification).

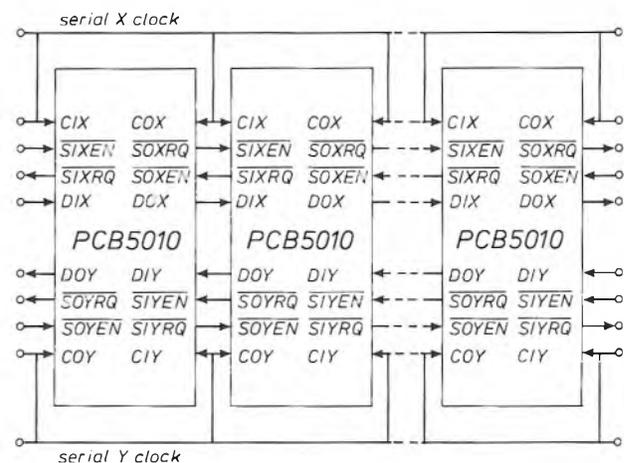


Fig. 16. Even greater versatility in processing can be obtained by combining several PCB 5010 chips. One method of combining the chips is illustrated here.

[9] K. Hellwig, K. Rinner, J. Schmid and P. Vary, Digitaler Signalprozessor für den Sprach- und Audiofrequenzbereich, PKI Tech. Mitt. No. 1, 57-64, 1986, Philips Kommunikations Industrie AG, Nuremberg, Germany.

**Table II.** Some benchmarks illustrating the signal-processing capacity of the PCB 5010/PCB 5011. The right-hand column gives the time required for performing a number of frequently occurring operations; in filtering operations this is the time required for calculating one sample of the output signal. Unless otherwise stated, all the quantities (signal samples, coefficients) have the standard word length of 16 bits.

Type of operation	Processing time ( $\mu$ s)
Non-recursive filtering (per filter coefficient)	0.125
Non-recursive filtering (64 filter coefficients; including input and output)	9.250
Recursive filtering (2nd-order section)	0.625
Recursive filtering (2nd-order section)*	1.875
Recursive filtering (2nd-order section; including input and output)*	3.375
Complex multiplication	1
128-point FFT	927
128-point FFT (including window function and input and output)	1100
256-point FFT	2112
256-point FFT (including window function and input and output)	2300

\* both signal samples and filter coefficients have double word length

### Teamwork

The PCB 5010 is one of the results of the 'SIGMAPI' project. The team included staff from Philips Research Laboratories (Eindhoven), Valvo (Hamburg)

and TeKaDe (Nuremberg). Besides the author, F. J. A. van Wijk and F. P. J. M. Welten also shared the responsibility for the development of the chip architecture. They received considerable support from the system designers R. J. Sluijter, P. Vary and K. Hellwig. Others who contributed were A. Delaruelle, J. A. Huisken, J. Stoter, W. Gubbels, J. Schmid, K. Rinner and J. Wittek (in the design), and K. J. E. van Eerdewijk (in the testing).

**Summary.** Digital signal processors have gradually evolved away from the older computer concepts to become a separate class of large to very large digital integrated circuits. Modern versions have the 'Harvard architecture', which is characterized by separate arrangements for transfer and storage of data and control information. This also applies to the PCB 5010, developed primarily for applications in telecommunications, audio and speech-processing. The PCB 5010, fabricated in 1.5- $\mu$ m CMOS technology, contains 135 000 transistors on an area of 61 mm<sup>2</sup> and can execute eight million instructions per second. Each instruction takes the form of a 40-bit 'microcode' word and specifies a maximum of six different sub-operations that can be executed simultaneously. As a general rule the data words have a length of 16 bits, but for some intermediate results 40 bits are available and if required, computations can be carried out with greater precision. The PCB 5010 has three data memories (a 512  $\times$  16-bit ROM and two 128  $\times$  16-bit RAMs) and a program memory (1024  $\times$  16 bits, mostly in a ROM). Various items of supporting software and hardware are available to facilitate the application of the PCB 5010.

1938

THEN AND NOW

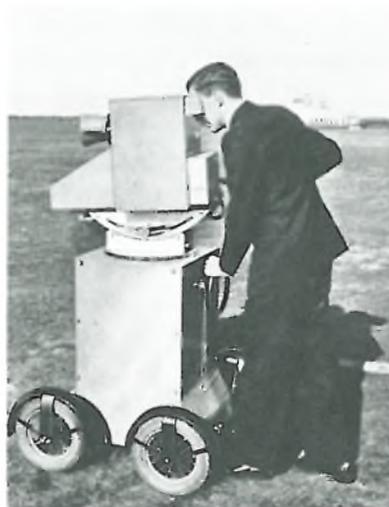
1988

## Television cameras

In 1938 a transportable television camera was definitely something you did not see every day. Nor would many users ever have thought of taking one on holiday (lower photographs [\*]). The pictures it took were only monochrome, of course. The zoom lens had not yet become a standard accessory, and there was still no simple way of recording the pictures. Since the number of picture lines had not been standardized, the camera shown offered the options of 405 or 567 picture lines rather than the 525 or 625 used today.

In 1988 many inventions in many fields have led to a very handy unit for the ordinary consumer. This is the 'camcorder', in which the camera and the recorder are combined. The very up-to-date VKR 6840 unit shown in the colour photograph only weighs 1.2 kg and measures 24 cm × 15 cm × 11 cm. The camera takes

colour pictures with sound, of course. Some of the essential functions like focusing, diaphragm control and setting the white balance have the option of manual or automatic operation. This camcorder has a zoom lens (zoom factor of 6) that can be operated by a motor or manually. The built-in video recorder (VHS-C system) gives an hour's 'filming' for each cassette. Recorded material can be inspected at any time with the built-in monochrome electronic viewfinder. The camcorder connects directly to a colour television receiver for playback in colour, or a cassette adapter can be used with any of the 130 million or more VHS recorders that have now been produced worldwide.



[\*] From Philips Technical Review, January 1938.

## Technological aspects of advanced telecommunications

G. Lorenz

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*The text below is an almost word-for-word account of the speech by Prof. G. Lorenz, member of the Group Management Committee of N.V. Philips' Gloeilampenfabrieken, at the European Conference 'Telecommunications: a European perspective', held on 18th and 19th June 1987 in the Kongresshalle in West Berlin. The speech is published by permission of the Corporate External Affairs Department of Philips International B.V. We have added the references and illustrations.*

*The speech gives an account of telecommunications today and looks ahead to future developments. We are sure it will interest our readers to learn how the management of our Company see these developments and how they think they should react to them from a European standpoint.*

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Modern telecommunications is going through a development phase that many people would describe as revolutionary. Throughout the world companies and research groups are working on these developments. Changes in communication are leading to the well-known convergence of communication and information. We can also see that the users are increasingly demanding global services and that they need low-cost, highly developed communication techniques that form the links between the terminals or between communication networks. Services intended for speech will continue to dominate for a long time to come, but even now the greatest growth area is to be found in non-speech services. The rapid increase in data communication will certainly continue. This year data communication within our company has increased by about 40%. Multimedia services intended for the combination of speech, data, text, pictures —

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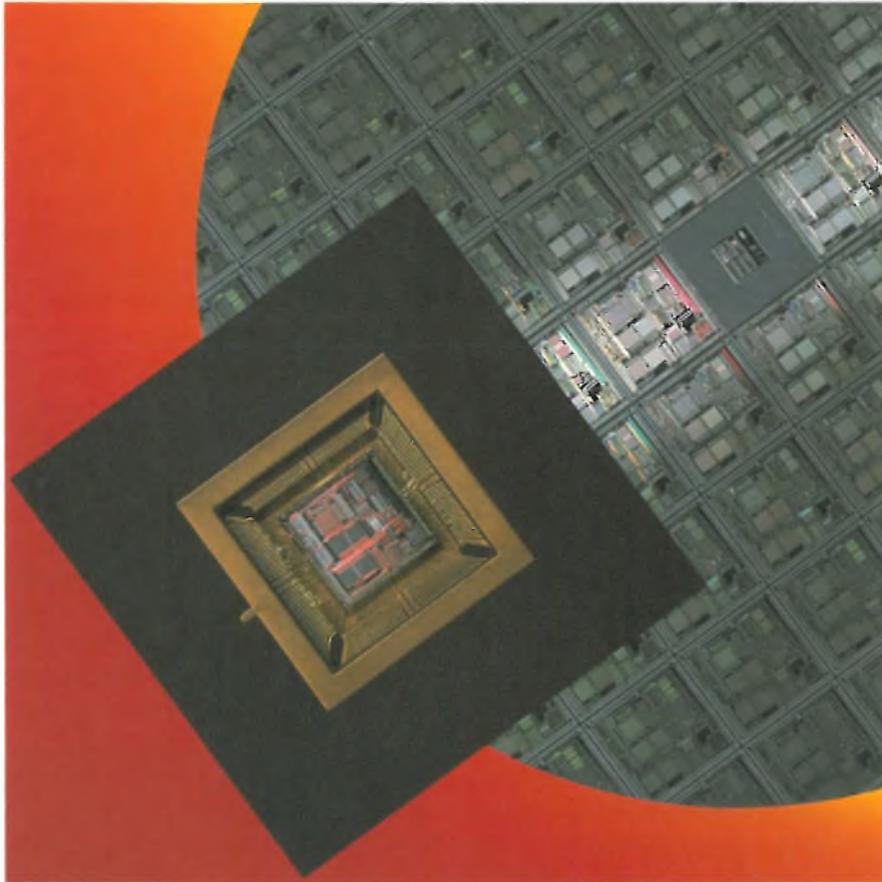
*Prof. Dr G. Lorenz is a member of the Group Management Committee of N.V. Philips' Gloeilampenfabrieken.*

either moving or stationary — are also being developed. In order that they can adapt to the needs of the market for non-speech services, the networks should have the option of flexible bandwidth, so that the services they offer can be adapted fairly easily by using different combinations. These developments in telecommunications, which will be of most interest to the business community, and will also be useful for the general public, particularly the private user, can only happen if the necessary technologies become a reality and consensus is reached on the standardized services and their coordinated introduction. We want more competition in Europe — so as to release dynamic forces. I think we would all endorse this, if the larger market, the unified European market, becomes a reality. I believe that the policy of the European Community is going in this very direction. If we only want to increase competition, without at the same time creating larger markets, we in Europe would be going in the wrong direction.

Telecommunications is based on three basic technologies: microelectronics, optical technology and software technology.

Everyone knows about the triumphal progress of microelectronics<sup>[1]</sup>. Millions of electronic functions can be combined on a silicon chip (*fig. 1*): speeds are increased, dissipation reduced and the costs significantly cut. These were the developments that made

possible to access this stored information at any place and at any time, and this is what we need for communication in dialogue form. Finally, the third option is an abundance of transmission capacity for all kinds of information. Nor is this last development at an end, and the basis of this unlimited transmission capacity is not only microelectronics, but optical-fibre technology as well.



**Fig. 1.** Philips are producing increasing quantities of 'Very-Large-Scale Integration' circuits. These large and complex microelectronic circuits are true systems on a single chip. They require considerable technological capability and a great deal of 'know-how' relating to the applications of the chips.

digitization<sup>[2]</sup>, integration and modern telecommunications into a reality. In the last 20 years the number of electronic functions on a chip has increased by a factor of 250 000 and the costs have fallen by a factor of 40 000. I believe that this is a unique occurrence in the history of industry. And these developments still continue, as we all know. Technological developments have given us another option: the amount of memory capacity. Today all kinds of information can be stored in large quantities at decentralized locations anywhere in the world. In principle, anyone can ac-

At present submicron technology is being developed throughout the world. We can assume that by the end of the eighties chips with many millions of transistor functions will be in mass production. By 1995 we — Philips, that is — expect to have structures with smallest dimensions of the order of 0.3 microns. This will be yet another step forward, which in turn

<sup>[1]</sup> J. C. van Vessel, From transistor to IC: a long road?, Philips Tech. Rev. 42, 326-334, 1986.

<sup>[2]</sup> See for example Philips Tech. Rev. 42, 101-144, 1985, Digital signal processing I, Background (special issue).

will offer a degree of integration of 100 million or more transistor functions. Finally, we can assume that the trend towards larger-scale integration will again be accompanied by a 10- to 100-fold reduction in the costs. These costs relate to the electronic functions.

The effect on the development of telecommunications is enormous: memory circuits and microprocessors are becoming more important, new processor families, in particular signal processors<sup>[3]</sup>, are being developed and produced everywhere, and parallel processing is the new buzz-word. Structures connected with Artificial Intelligence will gain in significance, as will ASICs (Application-Specific Integrated Circuits). Standard logic circuits will become less important, and so will customized circuits. We estimate that by 1995, 45% of all microelectronic circuits will be ASICs, and we expect that complete systems or subsystems will be integrated on a single chip. Systems-on-silicon is the in phrase. The condition for this development is not only that the technology should be available, but also that design and software know-how should be more effective, with the possibility of manufacturing prototypes quickly. As a result, the organizational structure of semiconductor companies will change. Until 1975 ICs were designed on the basis of geometric components, such as transistors, resistors, etc. Now design is based on structured components, such as registers or central processors. ASICs form the third stage, which is based on the concept of functional designs. Here is an example: work is in progress to enable a 'silicon compiler' for complex digital filters to produce the IC layout at the production centre from the filter equation alone. We are just starting to use this technology. It is in principle ready for use, the software is being improved and the development people are gradually learning to use it. ASICs will largely solve the problem of deciding between customized ICs — generally expensive because the quantities are small — and cheap standard circuits. As I have said, we have not yet reached the limits of silicon technology. We shall be there when we can integrate a billion ( $10^9$ ) electronic functions. Then we shall have reached the physical limits of silicon technology. And this will happen in the foreseeable future.

The current digitization of telecommunications is essentially based on the microelectronic components available to us today. However, if we consider the future requirements for telecommunications, especially for broadband communication, we can see that we do not yet have the necessary technological conditions for making the circuits at economic cost. I have the impression that the innovation process in telecommunications is changing radically. Up till now microelectronics has been the motive force behind the innova-

tion process in telecommunications. But now we know that to an increasing extent telecommunications is the driving force behind the innovation process in microelectronics, and that is a fundamental change. It signifies a considerable responsibility for both researchers and development people in telecommunications.

The telecommunications of the future will require series-to-parallel converters, A/D and D/A converters, electro-optical converters, complex digital filters, cheap encoders and decoders, SLICs (Subscriber Line Interface Circuits), switches with fast clock rates. All these are components that cannot be used in their present form in computer technology. This is why I never tire of explaining the new product requirements to our IC producers, making clear to them that we need communication circuits, not just microcontrollers for memories and microprocessors. 140 megabits/second is the requirement of the future. Everyone working in this field knows what that means — clock rates of 1.2 GHz for time-multiplex switches. And for microelectronics this means gate propagation delays of 500 picoseconds. These requirements cannot yet be met with the current technology (CMOS). Bipolar technologies are faster, but today they are suitable only for small-scale integration, and gallium arsenide, as a new material being worked upon, will certainly be the basis of an important technology in the future, but this technology has the disadvantage that it is very expensive. Gallium arsenide is a compound, not a simple element like silicon, and it also does not seem fundamentally suited to complementary logic.

You will see that I have my doubts about gallium arsenide. True, its applications are still in their infancy, but I do not believe that within the next ten years it will compete with silicon on a broad basis: the development and innovation potential of silicon technology is still much too great. Gallium arsenide will certainly be used when very high speeds are required. Another alternative on which work is being carried out is the integration of bipolar transistors and CMOS processors. This provides circuits fabricated partly in bipolar technology where high speeds are required, and partly in CMOS technology where high speeds are unnecessary. These circuits are much better in terms of power consumption and permit the possibility of much larger-scale integration.

Future requirements for telecommunications will also depend upon the system technology chosen for broadband services. In this context I should mention the asynchronous time-multiplex process, i.e. fast packet switching. This technique has the advantage that it is in principle service-independent and gives the user the bandwidth he needs at a given time depending on the nature and quality of the service required. I be-

lieve that this development must be discussed in depth with the microelectronics manufacturers. In our opinion we must devote considerable attention to fast packet switching.

Now something about the optical technologies. Gallium arsenide will continue to be very important for lasers. We are working on further integration towards monolithic optoelectronic circuits based on

Now I should like to say a few words about fibre-optic communication<sup>[4]</sup> (*fig. 2*). We have known for a long time that light is eminently suitable for the transmission of signals. The transmission of information by light was first suggested at the end of the last century. Only with the advent of the laser did it become possible to propagate light in a protected environment — the optical fibre. The optical fibre turns out



**Fig. 2.** Three optical-fibre cables. The left-hand cable contains six groups of ten optical fibres. The cable at the centre is a high-voltage cable intended for power distribution, with two optical-fibre cables at the centre for communication purposes. The right-hand cable contains six separate optical fibres. The optical fibres themselves are extremely thin, but each can carry many millions of bits per second.

substrates of new materials such as indium phosphide. At present experimental waveguide circuits — optical-waveguide circuits based on lithium niobate — are being developed. AT&T have recently presented studies of directly linked optical fibres - real 'photonics' therefore — but enormous R & D investment will be required before truly commercial 'photon' products such as switches, modulators, multiplexers and possibly even 'photon processors' and 'photon memories' come on to the market. We can already see that telecommunications will now bring forth photonics to stand beside electronics.

to be an ideal transport medium. Today fibre-optic cables can handle transmission rates of between 2 and 565 megabits/s. Distances of 35 kilometres can be bridged without repeaters. Fibre-optic cable is more economical than copper cable, with the result that the costs of information transmission fall. Because of its large bandwidth and insensitivity to external electro-

<sup>[3]</sup> See pp. 1-14 of this issue: J. L. van Meerbergen, Developments in integrated digital signal processors, and the PCB 5010.

<sup>[4]</sup> A. J. A. Nicia, An optical communication system with wavelength-division multiplexing and minimized insertion losses, I. System and coupling efficiency, Philips Tech. Rev. 42, 245-261, 1986.

magnetic fields, the optical fibre is more and more being used in local-area networks (LANs)<sup>[5]</sup>. The LANs that we make and sell tend increasingly to be fibre-optic networks. We are actively working on the development of systems for 1.2 to 2.4 gigabits/s, and these will appear on the market in about two years. And there is a vast amount of research with coherent systems as the objective. We are also working on combining other optical functions such as modulation, polarization, equalization and directional coupling in integrated optics based on lithium niobate. In the future we will probably also include indium phosphide or gallium arsenide as the substrate in these projects. The introduction of the optical fibre enabled costs to be reduced, and this will continue. We are now working on optical fibres for wavelengths of between 2 and 3 microns and the same applies to the transmitters and detectors.

The optical fibre is an innovation. The application of optical fibres however is purely a process of substitution: something is replaced, it works a little more efficiently and is slightly less expensive. The real challenge for the optical fibre is to penetrate to the lower level of the transmission hierarchy. If we have an innovation, we must not let it become purely a matter of substitution. Such a substitution generally leads to lower sales and production and therefore fewer jobs. The important thing is that the creative application of an innovation should create products and markets — new services and equipment must come into being, new products and new services must be introduced in a creative way. The challenge for the optical-fibre technology is to penetrate the lower level right through to the private subscriber. We believe that each home will have an optical-fibre connection with a high transmission capacity<sup>[6]</sup>. Today the cost factor still plays a fundamental role. But it is not only the cost factor, it is also the ideas factor, i.e. the answer to the question of what we are going to do with the optical-fibre option. Europe well understands the significance of the modern telecommunications infrastructure. The RACE programme is also aimed at the general introduction of optical-fibre networks from 1995 onwards. This programme needs the accompanying technology: the evolution of fabrication technologies, components, optical elements and finally process technologies, so that materials and equipment can become economically available. We must be ready for the transmission of moving pictures, probably of high-definition quality, via these networks.

I would like to say something here about optical memories, which are playing an ever-greater role. This is connected with the fact that the new telecommunications networks will incorporate more and more

intelligence, and new services will undoubtedly spring up. Databases and media for information storage will increase in importance and we think that the future need for broadband communication will be strongly influenced by the moving picture. If I may depart briefly from my main theme here: we talk a lot about moving pictures and other new services and we soon begin to wonder if there is a market for them, and if we need all of this. Of course we do not approach this problem with ordinary market research methods. Indeed, this applies to every basic innovation — by its very nature there never is a market for it at the start! As a rule, market research makes predictions for the future on the basis of existing markets. I can only say from experience that it is extremely difficult to predict how a basic innovation will fare in the market. I started in microelectronics in 1966. In that year we also wrote a scenario for 20 years ahead — 1986, and I was considered a hopeless optimist. But even this hopeless optimist's estimate was a factor of ten too low! This is why we must not give up just because there is no obvious market. As entrepreneurs we must not be faint-hearted. We must be bold enough to do innovative things. We must therefore tackle the new telecommunications a little more boldly and not concern ourselves too much with fundamental studies about future developments. Entrepreneurial initiative is stimulated by greater competition, of course, but it is stimulated even more by large markets. To put it another way: the unified European market is the real issue, and it is more important than greater competition. So I would like to give a higher priority to the European Community policy for the creation of a unified European market than to the call for more-competition in this market. However, I do admit that they are both related.

Let me now return to optical storage media (*fig. 3*) and mention the Compact Disc<sup>[7]</sup>, a real success story based on consumer electronics, not a professional application. We have already achieved submicron technology with our small silver disc. The little pits have structures smaller than one micron, so that millions of units of information can be stored in one square millimetre. We have also brought out CD-ROM. CD-ROM is used throughout the world for professional applications and has a memory capacity of 550 megabytes, which is equivalent to 1500 floppy disks or 200 000 standard A4 pages. And CD-ROM will be incorporated in the overall concept for office and production automation. We are bringing out a disc on which the user himself can enter data and as a next step we shall be bringing out a disc that can be rewritten many times. We have recently brought out CD-VIDEO, the integration of sound, text and vision.

An interactive Compact Disc (CD-I) is being prepared. We also have Digital Optical Recording (DOR), which enables large archiving systems<sup>[8]</sup> to store 500 000 A4 pages or 25 000 pages in facsimile quality on an LP-size disc, corresponding to a resolution of



Fig. 3. This photograph shows various types of optical discs, all products of pioneering research work at Philips. An optical video disc is shown at the bottom of the photograph, and at the top a Compact Disc, now most familiar in the version used as an audio disc. At the centre there is an Optical Digital Data Disc, used for data storage.

4 million pixels per A4 page. Users of these systems work with many millions of A4 pages. They wish to enter information, read it, transfer it, and 'browse' quickly through it, and they want decentralized operation. And they want to be able to connect to the public network, too.

Now let me make a few more remarks about software technology. On the hardware side we have a quite astonishing costs trend that we do not find on the software side. This is one of the reasons why software is the problem today. We need better tools and methods for software development. We need a significant improvement in software productivity. Software productivity is increasing each year by about 10%: this is a not unusual increase, but for the rapid development

process in telecommunications it is not enough. Everyone knows that the software costs for the development of telecommunications systems now account for much more than 50% of the total costs. Work on this is under way at the research laboratories. We are examining methods based on formal specification procedures and on new design techniques — and in the context of ESPRIT and RACE<sup>[9]</sup> programmes, too. We must intensify our efforts. In the research laboratories work is in progress on object-oriented programming and universal software, and finally application-oriented languages are being developed. Expert systems will play an important role in the highly-complicated field of test and diagnosis. It has to be said that the software technology is lagging behind. This is a very important point for the introduction of broadband communication as well as the technological aspects — the theme of this speech.

Another condition is the development of the market. We must achieve a united European market and we must also be bold enough to develop such markets, for example in the field of telecommunications. Another condition is the innovative strength of those offering services. They have a great responsibility. Innovations such as digitization, ISDN (Integrated Services Digital Network), microelectronics, optical fibres, optical technologies must not be seen as pure substitution processes. Modern telecommunications must be seen as a creative, innovative process. There must be a much closer cooperation between the user, the manufacturer and the provider of services, and in turn this must lead to new services being developed and offered. There will be the odd failure. There is no such thing as innovation without risk. We have tremendous opportunities, but there are also risks. Exploitation of the innovative potential is what counts, not merely substitution and rationalization. Compatibility is another condition, like standardization.

I would like to mention a final condition — a change in procurement policies. I think it is logical to say we want innovation, we must be bolder, but that also means we want larger markets, we want a unified

[5] J. R. Brandsma, PHILAN, a local-area network based on a fibre-optic ring, Philips Tech. Rev. 43, 10-21, 1986.

[6] J. van der Heijden, DIVAC — an experimental optical-fibre communications network, Philips Tech. Rev. 41, 253-259, 1983/84.

[7] M. G. Carasso, J. B. H. Peek and J. P. Sinjou, The Compact Disc Digital Audio system, Philips Tech. Rev. 40, 151-155, 1982.

[8] L. Vriens and B. A. J. Jacobs, Digital optical recording with tellurium alloys, Philips Tech. Rev. 41, 313-324, 1983/84; J. A. de Vos, Megadoc, a modular system for electronic document handling, Philips Tech. Rev. 39, 329-343, 1980.

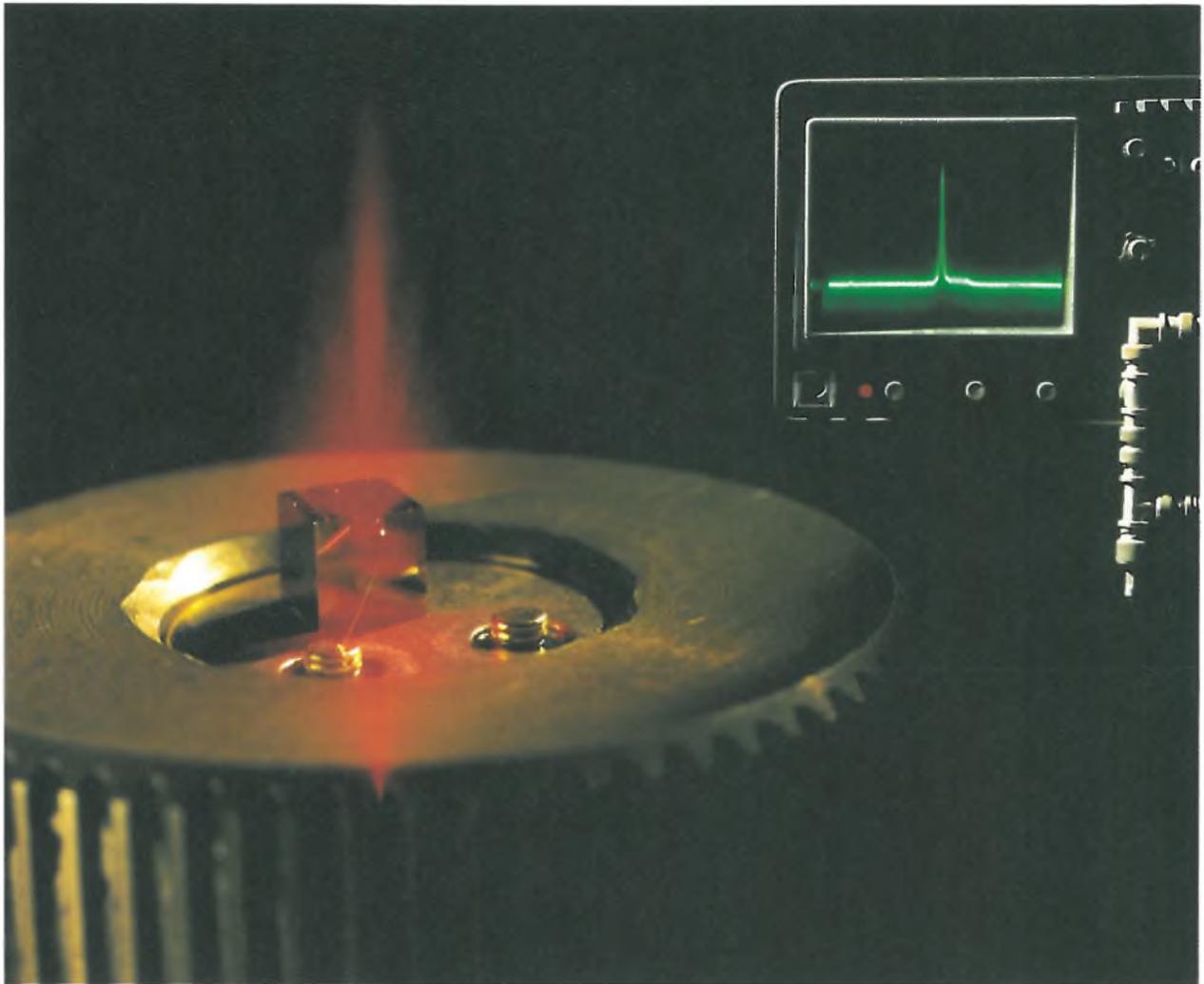
[9] ESPRIT: European Strategic Programme for Research and development in Information Technology. RACE: R&D in Advanced Communications technologies in Europe.

European market. If we want a unified European market, we must be more consistent and demand a change in the procurement policies of the large European national governmental telecommunications departments. We welcome the European Community programme and recommendations for telecommunications.

To sum up: firstly, for us the basic technologies of microelectronics and optics represent unlimited resources for the future development of telecommunications. Electronic functions, memory capacity, transmission capacity are available in almost unlim-

ited quantities and inexpensively. The further development of technology will also create the conditions for broadband communication. Secondly, new technologies are being developed for integrated optics and photon-based components. Thirdly, there is a software bottleneck. New methods, increased productivity are required. Fourthly, the prerequisites for advanced telecommunications — apart from the technology, standardization, the development of new services — are a unified European system, a unified European market and changes in the national procurement policies.

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## Semiconductor laser for visible light

Lasers made of semiconductor materials are used as light sources in fibre-optic communication systems, laser printers and many kinds of optical recording systems, such as Compact Disc. In optical recording<sup>[1]</sup> the wavelength of the laser light is of very great significance, since the maximum attainable information density on the optical disc is inversely proportional to the square of the wavelength. At present the laser wavelength usually has a value of about 800 nm, which is outside the visible-light range (400-700 nm). Recently Philips have made a semiconductor laser that operates at 650 nm. This laser was formed from a number of single-crystal layers (consisting of compounds of the chemical elements Al, Ga, In and P) with different compositions and doping. The layers were applied successively to a gallium-arsenide substrate by metal-organic vapour-phase epitaxy (MO-VPE)<sup>[2]</sup>. The photo-

graph shows an operating laser without its protective casing. The shiny copper cube (2 mm × 2 mm × 2 mm) acts as a heat sink; the actual laser (0.3 mm × 0.3 mm × 0.1 mm) is attached to the top of the front surface, and can be identified by the connecting wire. This laser can provide light pulses at a peak power of 100 mW or more, and the limits of its performance have not yet been reached. Because of its high available power it can be used for writing data to optical discs as well as read-out. The oscilloscope picture at the upper right of the photograph shows that the spectrum of the emitted radiation has only one significant line, at 650 nm.

[1] See also G. E. Thomas, Future trends in optical recording, Philips Tech. Rev. 44, No. 2, April 1988.

[2] P. M. Frijlink, J. P. André and M. Erman, Metal-organic vapour-phase epitaxy of multilayer structures with III-V semiconductors, Philips Tech. Rev. 43, 118-132, 1987.

## Improved adhesion of solid lubricating films with ion-beam mixing

K. Kobs, H. Dimigen, H. Hübsch and H. J. Tolle

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*The application of ion beams in semiconductor technology is widely known: the striking developments in the integrated-circuit industry would hardly have been possible without the progress in semiconductor doping achieved through ion implantation. In recent years there has also been increasing interest in other preparative methods, since ion bombardment is not only an excellent method of modifying the electrical properties of solids, but can also be used to modify their optical, chemical and mechanical properties. Furthermore, when thin-film deposition is combined with ion bombardment it is easy to produce novel surface alloys by ion-beam mixing, and problems due to poor adhesion between substrate and film can be avoided. At Philips GmbH Forschungslaboratorium Hamburg ion-beam mixing has been used to improve the adhesion of  $\text{MoS}_x$  lubricating films on steel to extend the useful life.*

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### Introduction

A bombardment of a solid by a beam of energetic ions results in an implantation of ions, with displacements of atoms near the implanted ions. Ion implantation has been widely used for many years in the semiconductor technology for fabricating layers of n-type and p-type material<sup>[1]</sup>. In comparison with the more conventional method of doping by thermal diffusion it permits better control of the depth profile, with reduced lateral doping, and almost any element can be used as the doping material. These advantages more than outweigh the need for annealing and for equipment that is more complicated and expensive.

In recent years ion bombardment has been increasingly used for modifying metallic surfaces<sup>[2]</sup>. With the wide variety of ion beams and experimental conditions there are many ways of improving properties such as hardness, wear resistance and corrosion resistance. Ion bombardment can be performed at well-defined low temperatures, with hardly any effect on the manufacturing tolerances or the conditions for machining the surface.

Three methods for modifying a surface with ion beams are shown in *fig. 1*. In the first method there is an implantation very like that used for semiconductors, but at a much higher dose, of the order of  $10^{17} \text{ cm}^{-2}$ . This means that the concentration of the implanted ions may reach 10 at. % or more, leading to the formation of a surface alloy with a typical thickness of 0.1 to 0.3  $\mu\text{m}$ , depending on the implantation conditions (the ion energy in particular) and the target material.

The other two methods in *fig. 1* make use of the 'mixing' capacity of an ion beam. In both, a deposition of a thin film is followed by ion bombardment to induce a kind of mixing of the atoms of the film and the substrate. This may produce some kind of surface mixture, or it may give a well-defined surface alloy (*fig. 1b*). The advantage over direct implantation (*fig. 1a*) is that the dose can be reduced by two orders of magnitude, because of secondary collisions between the atoms that have been 'knocked out' of their positions in the film or substrate. The experimental conditions can usually be adjusted, especially for somewhat thicker films, so that the mixing is restricted to the interface region of the film and the sub-

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strate (fig. 1c). The adhesion of the film can be substantially improved in this way without affecting its surface properties.

Various examples of improved adhesion of metal films on substrates due to ion-beam mixing have been reported recently [3]. We have studied this method for improving the adhesion of solid lubricating films of  $\text{MoS}_x$  ( $x = 1.6$  to  $1.9$ ) on steel [4]. In the last few years there has been increasing interest in the application of such films for reducing wear and friction. It has been shown that sputtered  $\text{MoS}_x$  films have excellent lubricating properties in inert gas or in vacuum [5]. With films obtained under optimized sputtering conditions the coefficient of friction can be as low as 0.02. Wider application is still limited, however, by the short 'sliding life', which depends on the adhesion of the film and the degree of cohesion between the crystallites of  $\text{MoS}_x$  [6].

In the ion-beam mixing of  $\text{MoS}_x$  films the effect on the film structure must also be taken into account, because of the high correlation with the friction. A film that is amorphous after bombardment no longer has lubricating characteristics, since the coefficient of friction will have increased to 0.4 [7]. It is therefore prudent just to modify the interface region. This requires careful optimization of the ion energy and dose for a given film thickness.

In this article we shall first present some of the results of our tribological investigations, which demon-

strate the beneficial effect of ion-beam mixing on the sliding life of  $\text{MoS}_x$  films. Then we shall discuss changes in the properties of the film due to the ion beams, and we shall conclude by considering the modification of the interface region.

### Improving the sliding life

The equipment and the procedure for depositing  $\text{MoS}_x$  films on steel by r.f.-diode sputtering have been described in an earlier article in this journal [8]. The sputtering was performed in the non-reactive mode with an  $\text{MoS}_2$  target and at an argon pressure of 2.6 Pa. The power density was  $5 \text{ W/cm}^2$ , the residual gas pressure in the vacuum chamber was less than  $6 \times 10^{-4}$  Pa and the temperature was less than  $60^\circ\text{C}$ . Before starting a deposition the steel substrate was cleaned by ion etching to avoid any effects from surface contamination on the adhesion of the film.

The ion bombardment was carried out in a Varian-Extrion Model 200 implanter with a mass-separated ion beam (Fraunhofer Institut für Festkörpertechnologie, Munich, and the Fraunhofer Arbeitsgruppe für integrierte Schaltungen, Erlangen). The beam-current

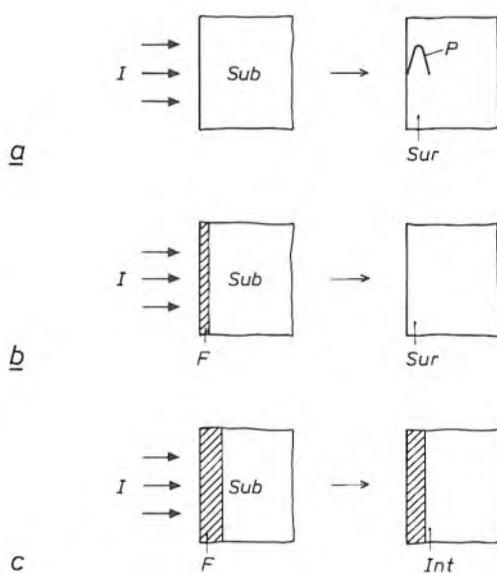


Fig. 1. Diagram showing three methods for ion-beam modification of solids [2]. a) Implantation of ions  $I$  into a substrate  $Sub$ , to produce a surface layer  $Sur$  of thickness  $0.02$  to  $1 \mu\text{m}$  with a characteristic doping profile  $P$ . b) Mixing of the atoms of a thin deposited film  $F$  ( $< 0.2 \mu\text{m}$ ) and the substrate to give a surface layer  $Sur$  of mixed composition. c) Formation of an interface layer  $Int$  of mixed composition between a film of thickness  $0.05$  to  $1 \mu\text{m}$  and the substrate — this is the subject of this article.

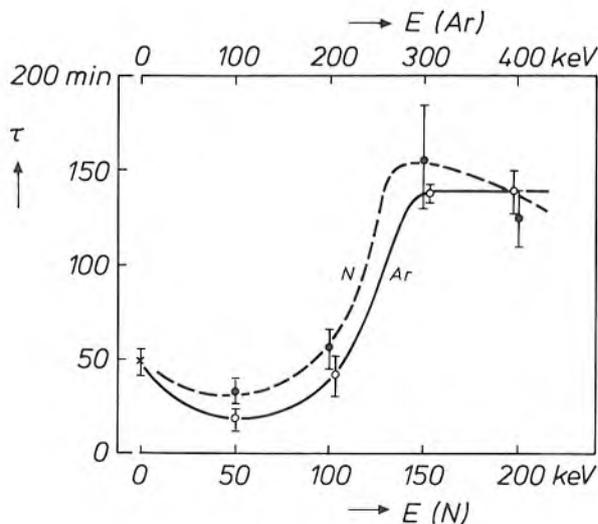
- [1] See for example W. K. Hofker and J. Politiek, Ion implantation in semiconductors, Philips Tech. Rev. 39, 1-14, 1980; H. J. Ligthart and J. Politiek, An open 800-kV ion-implantation machine, Philips Tech. Rev. 43, 169-179, 1987.
- [2] See for example G. K. Wolf, Die Anwendung von Ionenstrahlen zur Veränderung von Metalloberflächen, Metalloberfläche 40, 101-105, 1986.
- [3] A. E. Berkowitz, R. E. Benenson, R. L. Fleischer, L. Wielunski and W. A. Lanford, Ion-beam-enhanced adhesion of Au films on Si and  $\text{SiO}_2$ , Nucl. Instrum. & Methods Phys. Res. B7/8, 877-880, 1985; J. E. E. Baglin and G. J. Clark, Ion beam bonding of thin films, Nucl. Instrum. & Methods Phys. Res. B7/8, 881-885, 1985; D. K. Sood, W. M. Skinner and J. S. Williams, Helium and electron beam induced enhancement in adhesion of Al, Au and Pt films on glass, Nucl. Instrum. & Methods Phys. Res. B7/8, 893-899, 1985; R. A. Kant, B. D. Sartwell, I. L. Singer and R. G. Vardiman, Adherent TiN films produced by ion beam enhanced deposition at room temperature, Nucl. Instrum. & Methods Phys. Res. B7/8, 915-919, 1985.
- [4] K. Kobs, H. Dimigen, H. Hübsch, H. J. Tolle, R. Leutenecker and H. Rysse, Improved tribological properties of sputtered  $\text{MoS}_x$  films by ion beam mixing, Appl. Phys. Lett. 49, 496-498, 1986.
- [5] M. N. Gardos, Quality control of sputtered  $\text{MoS}_2$  films, Lub. Eng. 32, 463-475, 1976; R. I. Christy and H. R. Ludwig, R. F. sputtered  $\text{MoS}_2$  parameter effects on wear life, Thin Solid Films 64, 223-229, 1979; R. I. Christy, Sputtered  $\text{MoS}_2$  lubricant coating improvements, Thin Solid Films 73, 299-307, 1980; H. Dimigen, H. Hübsch, P. Willich and K. Reichelt, Stoichiometry and friction properties of sputtered  $\text{MoS}_x$  layers, Thin Solid Films 129, 79-91, 1985.
- [6] T. Spalvins, Frictional and morphological properties of Au- $\text{MoS}_2$  films sputtered from a compact target, Thin Solid Films 118, 375-384, 1984.
- [7] T. Spalvins, Tribological properties of sputtered  $\text{MoS}_2$  films in relation to film morphology, Thin Solid Films 73, 291-297, 1980.
- [8] H. Dimigen and H. Hübsch, Applying low-friction wear-resistant thin solid films by physical vapour deposition, Philips Tech. Rev. 41, 186-197, 1983/84.

density was  $5 \mu\text{A}/\text{cm}^2$  and the maximum temperature was  $150^\circ\text{C}$ . The mixing experiments were performed with beams of singly charged nitrogen ions ( $\text{N}^+$ ) or doubly charged argon ions ( $\text{Ar}^{2+}$ ) at various energies (50 to 400 keV) and ion doses ( $0.3$  to  $5 \times 10^{16} \text{ cm}^{-2}$ ).

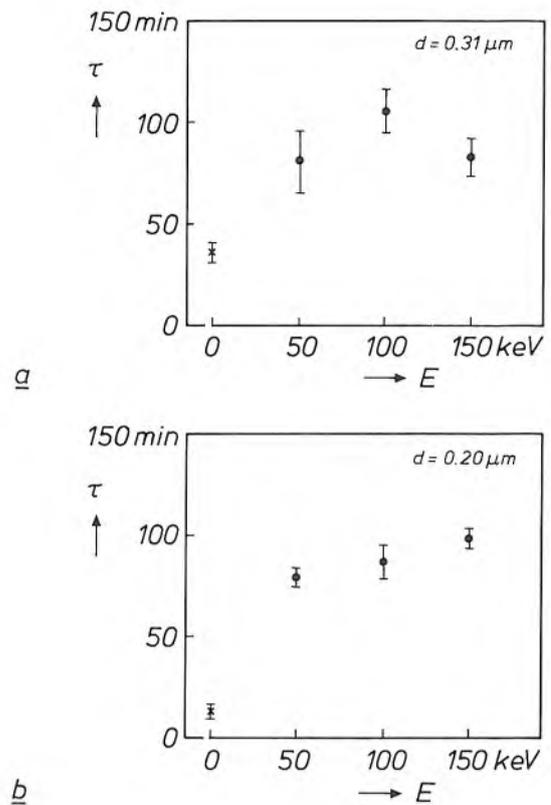
The friction and wear of the films were determined with a ball-on-disc tribometer with an oscillating steel ball<sup>[9]</sup>. The advantage of this method of testing is that it gives an unambiguous indication of the final failure of the film, which is signalled by a sudden increase of more than an order of magnitude in the coefficient of friction. The measurements were made in a dry nitrogen atmosphere with a relative humidity of less than 0.5%. Each film life was measured five times; the ball oscillated at a frequency of 7 Hz and the standard sliding load was 5.1 N.

The effect of the energy of the ion beams on the sliding life is shown in *fig. 2* for an  $\text{MoS}_x$  film  $0.47 \mu\text{m}$  thick bombarded with nitrogen or argon ions at a dose of  $1 \times 10^{16} \text{ cm}^{-2}$ . No improvement is found at the lower energies; the mixing with nitrogen ions at 50 keV or argon ions at 100 keV in fact gives a slight reduction in the life. At high energies, however, there is a considerable improvement in the sliding life. The lives of nitrogen-bombarded films and argon-bombarded films are nearly identical, if we bear in mind that the nitrogen ions only require about half the energy of the argon ions.

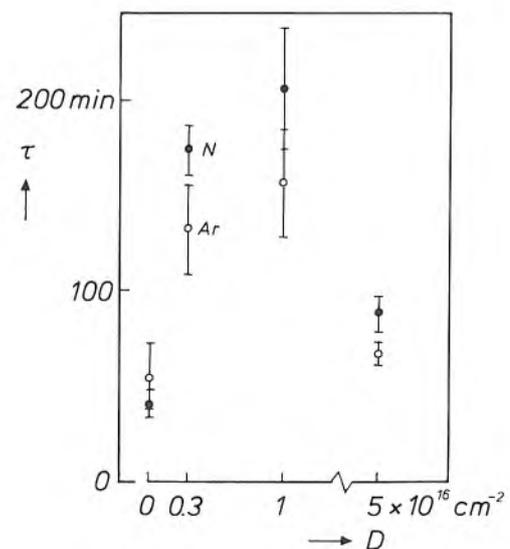
The observed dependence of the sliding life on the energy of the ion beams indicates that the implanta-



**Fig. 2.** Sliding life  $\tau$  of  $0.47\text{-}\mu\text{m}$   $\text{MoS}_x$  films sputtered on steel, before ion-beam mixing ( $\times$ ) and after mixing with nitrogen ions ( $\bullet$ ) and argon ions ( $\circ$ ), as a function of their energy  $E$ . The dose was  $1 \times 10^{16} \text{ cm}^{-2}$ , and the lives were measured at a sliding load of 5.1 N. Ion-beam mixing at high energies gives an appreciable improvement in the sliding life. The nitrogen ions require only about half the energy of the argon ions for the same sliding life.



**Fig. 3.** Life  $\tau$  at a sliding load of 5.1 N for  $\text{MoS}_x$  films of thickness  $d = 0.31 \mu\text{m}$  and  $0.20 \mu\text{m}$  sputtered on steel, before ion-beam mixing ( $\times$ ) and after mixing with nitrogen ions (dose  $1 \times 10^{16} \text{ cm}^{-2}$ ) as a function of their energy  $E$  ( $\bullet$ ). Even after ion-beam mixing at a relatively low energy (50 keV) the sliding life is considerably improved — by a factor of more than two for the  $0.31\text{-}\mu\text{m}$  film and by a factor of almost seven for the  $0.20\text{-}\mu\text{m}$  film.

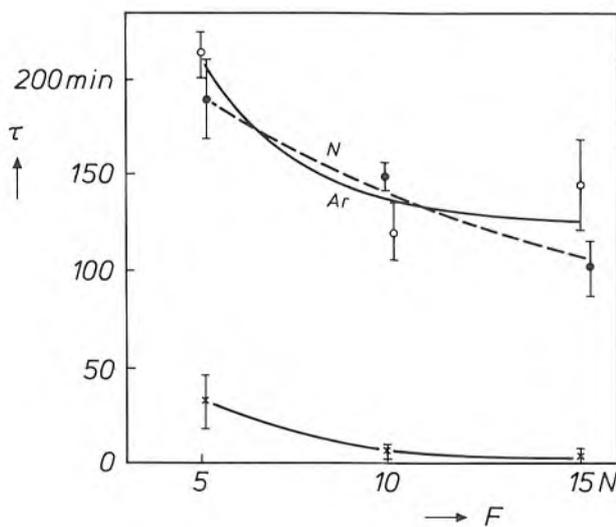


**Fig. 4.** Effect of the dose  $D$  on the life  $\tau$  at a sliding load of 5.1 N for  $\text{MoS}_x$  films of thickness  $0.43 \mu\text{m}$  sputtered on steel, after mixing with nitrogen ions at 150 keV ( $\bullet$ ) and argon ions at 300 keV ( $\circ$ ). In both cases the highest values are obtained at a dose of  $1 \times 10^{16} \text{ cm}^{-2}$ .

tion range of the ions is essential for the improvement in life due to interface mixing. This is in agreement with the results of life measurements for thinner films; see *fig. 3*. With a 0.31- $\mu\text{m}$  film the life is found to more than double after mixing with nitrogen ions of energy only 50 keV. Under the same conditions the life of a 0.20- $\mu\text{m}$  film increased by nearly seven times.

The dose dependence of the sliding life is shown in *fig. 4*. These results were obtained with 0.43- $\mu\text{m}$  films bombarded with nitrogen ions at an energy of 150 keV and argon ions at an energy of 300 keV. The maximum life was observed at a dose of  $1 \times 10^{16} \text{ cm}^{-2}$ , but a very similar improvement was obtained at  $3 \times 10^{15} \text{ cm}^{-2}$ .

For practical applications it is very important to know whether the improvement in the sliding life is also found for higher loads. *Fig. 5* shows the effect of the load on the lives of three differently treated  $\text{MoS}_x$  films of thickness 0.29  $\mu\text{m}$  deposited on steel. As the load was increased the life of the unbombarded film fell rapidly to only a few minutes. On the other hand, the sliding lives of films bombarded with nitrogen or argon ions were only reduced relatively slightly on increasing the load.



**Fig. 5.** The sliding life  $\tau$  as a function of the applied load  $F$  for  $\text{MoS}_x$  films of thickness 0.29  $\mu\text{m}$  sputtered on steel, before ion-beam mixing ( $\times$ ) and after mixing with nitrogen ions at 100 keV ( $\bullet$ ) and argon ions at 250 keV ( $\circ$ ) at a dose of  $1 \times 10^{16} \text{ cm}^{-2}$ . At high loads the sliding life of the unbombarded film is reduced to a few minutes, whereas the bombarded films still have a long sliding life.

It should be emphasized that ion-beam mixing does not give any significant change in frictional behaviour during the sliding life. In all the tribological experiments it is found that the coefficient of friction is virtually unaffected by the ion energy and the dose [4].

#### Change in film properties

In seeking to explain the improvement in sliding life due to ion-beam mixing, we have used optical microscopy and profilometer measurements to study the wear tracks made by the oscillating steel ball. These investigations showed that there were considerable differences in the appearance of the bombarded and unbombarded films, which depended on the number of cycles of the oscillating ball. Even after a single cycle some of the material has been removed from the surface of the unbombarded  $\text{MoS}_x$  film. After ten cycles most of the wear track and the surrounding region have been damaged, indicating flaking. This has been confirmed by the profile measurements, which showed that the profile was rectangular.

These effects were not observed for  $\text{MoS}_x$  films bombarded with nitrogen or argon ions at high energies. For a 0.36- $\mu\text{m}$  film bombarded with argon ions at an energy of 400 keV and a dose of  $1 \times 10^{16} \text{ cm}^{-2}$ , the first wear occurred after 1000 cycles with no flaking of the film. This indicates a considerable improvement in the adhesion of the film to the substrate. The wear track now has a typical ditch profile instead of a rectangular one. These results confirm observations of improved adhesion of sputtered  $\text{MoS}_x$  films that had been ion-bombarded at a very low film thickness before the sputtering had been completed [10].

Profilometer measurements of unbombarded and bombarded areas on the same sample reveal a significant reduction in the film thickness for the bombarded areas. This reduction increases with the energy of the incident ions; see *fig. 6*. The reduction in thickness is not due to sputtering effects, as has been demonstrated by electron-probe microanalysis. It is correlated with an increase in the film density of up to 40% and gives a greater cohesion between the  $\text{MoS}_x$  crystallites and an improvement in the effective film thickness.

A further indication of the effect of these structural changes is the increase in the reflectance of sputtered  $\text{MoS}_x$  films due to ion-beam mixing. For example, bombardment with argon ions at an energy of 400 keV gives an increase in the reflectance from 15 to 55%, probably because of the reorientation of the  $\text{MoS}_x$  platelets. It has been found that platelets with their basal planes perpendicular to the plane of the film reorient themselves parallel to the plane, giving an

[9] H. Dimigen, K. Kobs, R. Leutenecker, H. Ryssel and P. Eichinger, *Wear resistance of nitrogen-implanted steels*, *Mater. Sci. & Eng.* 69, 181-190, 1985.

[10] J. Chevallier, S. Olesen, G. Sørensen and B. Gupta, *Enhancement of sliding life of  $\text{MoS}_2$  films deposited by combining sputtering and high-energy ion implantation*, *Appl. Phys. Lett.* 48, 876-877, 1986.

increased reflection [11]. A partial recrystallization of the  $\text{MoS}_x$  film can also be induced by the ion bombardment, as has been demonstrated for sputtered  $\text{WS}_2$  films [12]. Investigations with scanning and transmission electron microscopes are in progress with the aim of clarifying the structural changes.

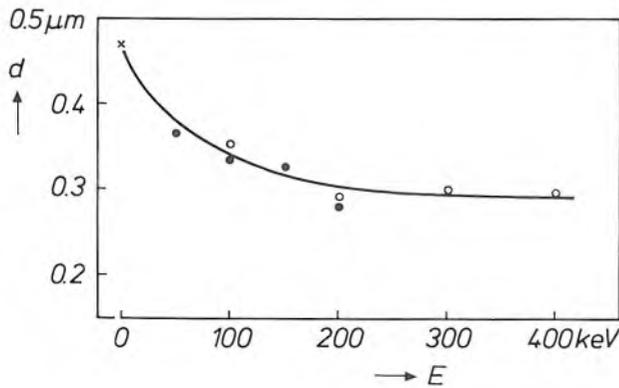


Fig. 6. Thickness  $d$  of  $\text{MoS}_x$  films sputtered on steel, before ion-beam mixing ( $\times$ ) and after mixing with nitrogen ions ( $\bullet$ ) and argon ions ( $\circ$ ) as a function of their energy  $E$  at a dose of  $1 \times 10^{16} \text{ cm}^{-2}$ . A marked reduction in film thickness is observed for increasing ion energy.

#### Modification of the interface region

A useful method for studying the modification of the interface region between a film and its substrate is secondary-ion mass spectrometry (SIMS) [13]. In this method an ion beam sputters ionized particles from the surface to be investigated. The ions sputtered successively are analysed by mass in a quadrupole field, and the variation in composition with depth can then be determined. Our SIMS experiments were performed by using a beam of oxygen or argon ions at an energy of 7 keV and a primary ion current of  $0.5 \mu\text{A}$ , using a scanned area of  $0.5 \text{ mm} \times 0.5 \text{ mm}$ . The resulting sputter rates were  $1 \mu\text{m/h}$  for the  $\text{MoS}_x$  films and  $0.3 \mu\text{m/h}$  for the steel substrates.

Fig. 7 shows the SIMS depth profiles of molybdenum, sulphur and iron for  $\text{MoS}_x$  films on steel after mixing with nitrogen ions at 50 and 200 keV. Mixing with ions at 50 keV does not give any broadening of the interface as compared with the unbombarded film. A markedly broadened interface of about 80 nm is detected after mixing at 200 keV, revealing a high correlation with the observed increase in the sliding life. The distance measured between the interface and the surface has become much smaller as a result of the reduction in the film thickness described previously.

Fig. 8 shows the SIMS profiles for the same type of film, but now after mixing with argon ions at 400 keV.

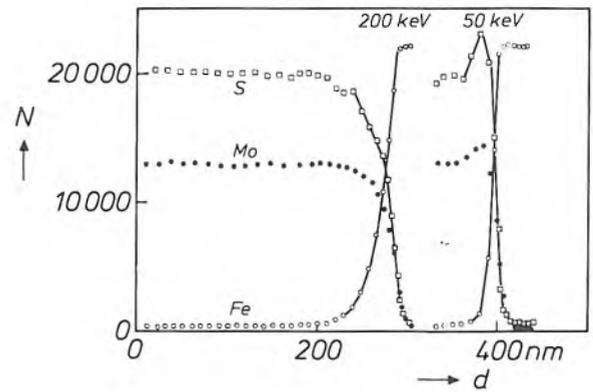


Fig. 7. SIMS depth profiles of molybdenum, sulphur and iron for  $\text{MoS}_x$  films of thickness  $0.47 \mu\text{m}$  sputtered on steel, after mixing with nitrogen ions at 50 and 200 keV, at a dose of  $1 \times 10^{16} \text{ cm}^{-2}$ . The number of secondary-ion counts per second ( $N$ ) is plotted against the depth  $d$ . After mixing at 50 keV some reduction in the thickness of the film is observed, but the intensity changes at the interface are fairly sharp. After mixing at 200 keV the reduction in thickness is much larger and the intensity changes are more gradual.

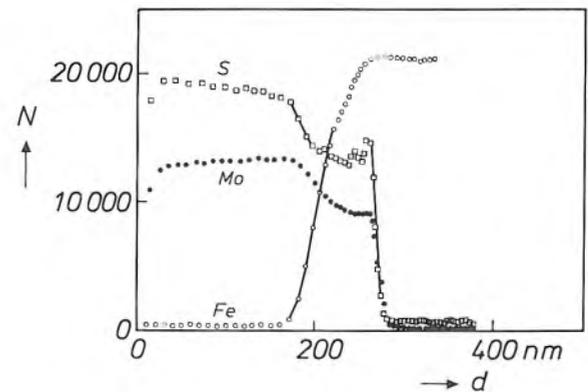


Fig. 8. SIMS depth profiles of molybdenum, sulphur and iron for an  $\text{MoS}_x$  film of thickness  $0.47 \mu\text{m}$  sputtered on steel, after mixing with argon ions at 300 keV, at a dose of  $1 \times 10^{16} \text{ cm}^{-2}$ . The broadening of the interface region is more significant than in the samples of fig. 7.

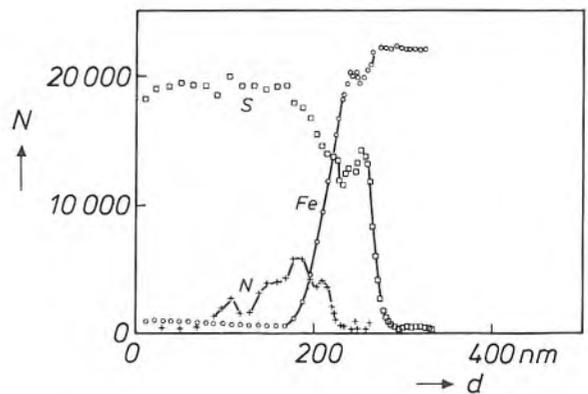


Fig. 9. SIMS depth profiles of sulphur, iron and nitrogen for an  $\text{MoS}_x$  film of thickness  $0.43 \mu\text{m}$  sputtered on steel, after mixing with nitrogen ions at 150 keV, at a dose of  $5 \times 10^{16} \text{ cm}^{-2}$ . The intensity changes for sulphur and iron are almost the same as in fig. 8. The highest nitrogen intensity is observed at the interface.

The broadening of the interface is more significant than for the nitrogen-implanted films at the same dose, because of the greater mixing effect of the argon ions.

On increasing the dose of the nitrogen ions to  $5 \times 10^{16} \text{ cm}^{-2}$  almost the same profiles are obtained as with the argon ions at a dose of  $1 \times 10^{16} \text{ cm}^{-2}$ ; see *fig. 9*. The nitrogen depth profile was also determined for this sample. The maximum nitrogen concentration was found to be located at the interface. This indicates that the ion range corresponds well with the thickness of the  $\text{MoS}_x$  film.

In the work described here we cooperated closely with R. Leutenecker of the Fraunhofer Institut für Festkörpertechnologie, Munich, and with Prof. H. Ryssel of the Fraunhofer Arbeitsgruppe für integrierte Schaltungen, Erlangen.

The tribological tests were performed by W. Mohwinkel, and the electron-probe microanalyses were made by Dr P. Willich and D. Obertop.

Some of the work was supported by the Ministry of Research and Technology of the German Federal Republic, under Grants 03 T 0002 E6, 03 T 0002 A5 and 13 N 5353/0.

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**Summary.** Ion-beam mixing of sputtered  $\text{MoS}_x$  films on steel can considerably lengthen their sliding life, especially at higher loads. The best results are obtained with films of thickness 0.3 to 0.5  $\mu\text{m}$  bombarded with nitrogen ions at 150 to 200 keV or argon ions at 300 to 400 keV, with a dose of  $1 \times 10^{16} \text{ cm}^{-2}$ . The mixing has no adverse effect on the frictional behaviour during the sliding life. The improvement in the sliding life can be attributed to improved adhesion of the  $\text{MoS}_x$  films, as demonstrated by profile measurements and secondary-ion mass spectrometry. An ion beam can also introduce significant structural changes in a film, giving a noticeable increase in the film density and the reflectance.

## Scientific publications

These publications are contributed by staff from the laboratories and other establishments that form part of or are associated with the Philips group of companies. Many of the articles originate from the research laboratories named below. The publications are listed alphabetically by journal title.

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	Philips Research Laboratories, Sunnyvale P.O. Box 9052, Sunnyvale, CA 94086, U.S.A.		<i>S</i>	
P. K. Bachmann, W. Hermann, H. Wehr & D. U. Wiechert	<i>A</i>	Stress in optical waveguides. 2: Fibres	Appl. Opt. 26	1175-1182 1987
J. M. Towner	<i>S</i>	Influence of conductor linewidth on short-circuit failure	Appl. Phys. Lett. 50	1581-1582 1987
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N. J. A. van Veen	<i>E</i>	XPS on impregnated cathodes: surface concentrations and thermal stability	Appl. Surf. Sci. 29	113-126 1987
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J. L. van Meerbergen, Developments in integrated digital signal processors, and the PCB 5010,  
Philips Tech. Rev. **44**, No. 1, 1-14, March 1988.

Digital signal processors have gradually evolved away from the older computer concepts to become a separate class of large to very large digital integrated circuits. Modern versions have the 'Harvard architecture', which is characterized by separate arrangements for transfer and storage of data and control information. This also applies to the PCB 5010, developed primarily for applications in telecommunications, audio and speech-processing. The PCB 5010, fabricated in 1.5- $\mu\text{m}$  CMOS technology, contains 135 000 transistors on an area of 61 mm<sup>2</sup> and can execute eight million instructions per second. Each instruction takes the form of a 40-bit 'microcode' word and specifies a maximum of six different sub-operations that can be executed simultaneously. As a general rule the data words have a length of 16 bits, but for some intermediate results 40 bits are available and if required, computations can be carried out with greater precision. The PCB 5010 has three data memories (a 512  $\times$  16-bit ROM and two 128  $\times$  16-bit RAMs) and a program memory (1024  $\times$  16 bits, mostly in a ROM). Various items of supporting software and hardware are available to facilitate the application of the PCB 5010.

G. Lorenz, Technological aspects of advanced telecommunications,  
Philips Tech. Rev. **44**, No. 1, 16-22, March 1988.

Word-for-word account of a speech at the European Conference 'Telecommunications: a European perspective' on 18th and 19th June 1987 in West Berlin. The speaker comes to the following conclusions. Firstly, for us the basic technologies of microelectronics and optics represent unlimited resources for the future development of telecommunications. Electronic functions, memory capacity, transmission capacity are available in almost unlimited quantities and inexpensively. The further development of technology will also create the conditions for broadband communication. Secondly, new technologies are being developed for integrated optics and photon-based components. Thirdly, there is a software bottleneck. New methods, increased productivity are required. Fourthly, the prerequisites for advanced telecommunications — apart from the technology, standardization, the development of new services — are a unified European system, a unified European market and changes in the national procurement policies.

K. Kobs, H. Dimigen, H. Hübsch and H. J. Tolle, Improved adhesion of solid lubricating films with ion-beam mixing, PhilipsTech. Rev. **44**, No. 1, 24-29, March 1988.

Ion-beam mixing of sputtered MoS<sub>x</sub> films on steel can considerably lengthen their sliding life, especially at higher loads. The best results are obtained with films of thickness 0.3 to 0.5 μm bombarded with nitrogen ions at 150 to 200 keV or argon ions at 300 to 400 keV, with a dose of  $1 \times 10^{16}$  cm<sup>-2</sup>. The mixing has no adverse effect on the frictional behaviour during the sliding life. The improvement in the sliding life can be attributed to improved adhesion of the MoS<sub>x</sub> films, as demonstrated by profile measurements and secondary-ion mass spectrometry. An ion beam can also introduce significant structural changes in a film, giving a noticeable increase in the film density and the reflectance.

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