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Contents

Motor traffic is the lifeblood of today's city. Keeping it moving, night and day, rain or shine, has become a complex art integrating various mathematical and communications disciplines and served by the versatility of modern electronic control. Essential to the execution of that control are solid-state switching devices such as thyristors and triacs. In this as in many other applications, long-term reliability under varying and adverse conditions is fundamental. The article beginning on page 53 describes recent developments which further enhance that reliability and quantifies the results of life tests.

Digital control of radio and audio equipment.

Part 4 - Displays and control of analogue functions with RTS

U. SCHILLHOF

The third part of this article in the previous issue of E.C.&A. introduced the microcomputer-controlled radio tuning system (RTS) and described how a radio is electronically tuned with a digital frequency synthesiser. This part of the article describes the display and analogue control functions of the RTS as shown in Fig.1.

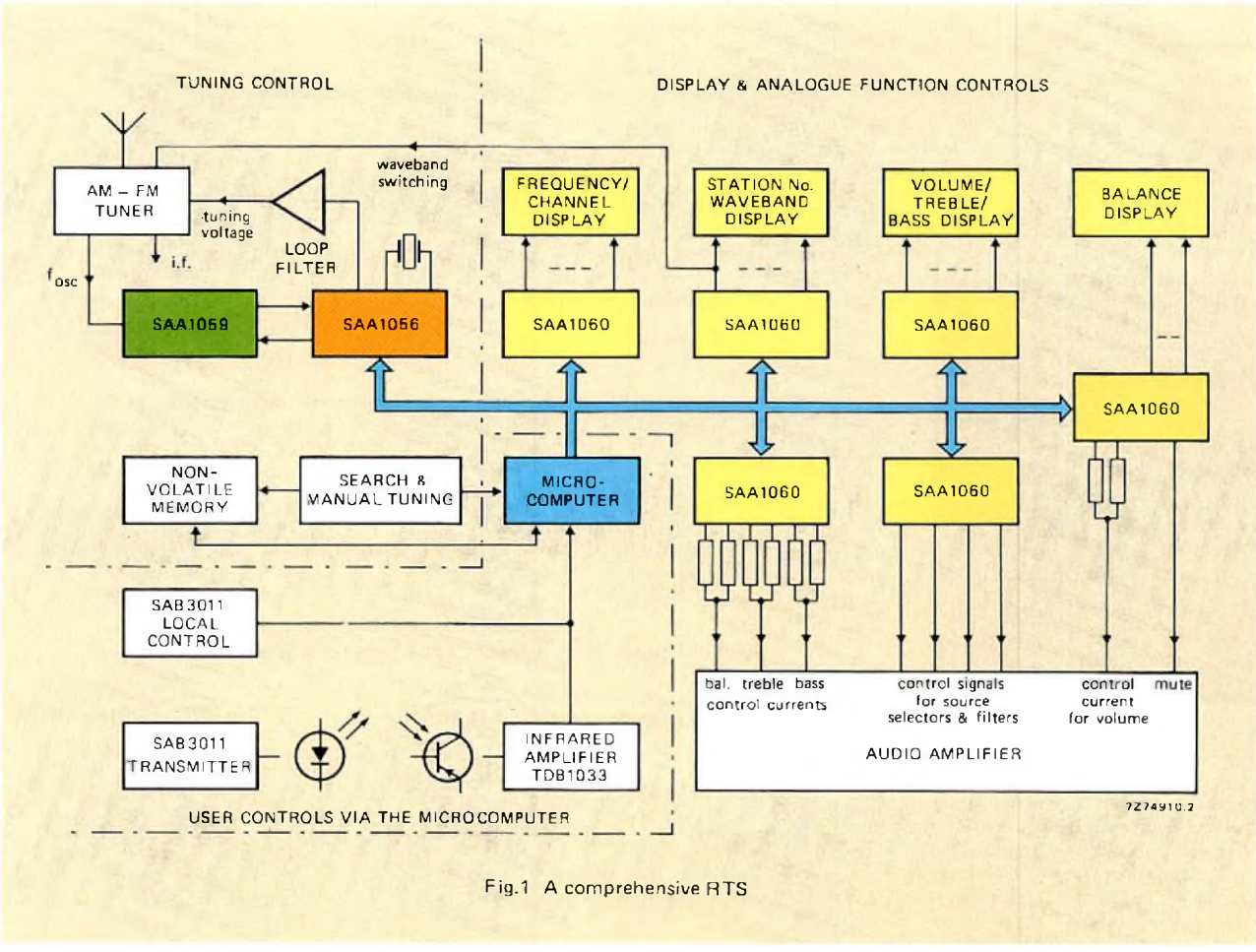


Fig.1 A comprehensive RTS

Three integrated circuits are available for performing the RTS display and analogue control functions. The LED display interface SAA1060 (DIFA-LED) is for LED display and analogue function control via external D-to-A converters. The computer-controlled analogue memory SAB3013 (CCAM) is for controlling up to six analogue functions via internal D-to-A converters. The LCD interface SAA1062 (DIFA-LCD) is for driving liquid crystal displays.

The SAA1060 and SAA1062 are software-compatible circuits that accept serial data from the microcomputer bus (CBUS) and convert it into parallel form for:

- Driving 7-segment LED numeral displays of frequency, channel number, preset station number or analogue control position.
- Driving LED bargraph displays of analogue control positions.
- Driving 7-segment liquid crystal displays of frequency, channel number, preset station number or analogue control position.
- On/off control of analogue functions with LED indication. Required functions are selected via band-switching diodes, logic-level-controlled integrated circuits, and integrated source selectors TDA1028 and TDA1029.
- Control of analogue functions via D-to-A conversion resistor ladders and integrated electronic potentiometers TDA1073 and TDA1074A. The SAB3013 incorporates internal D-to-A conversion which allows the integrated electronic potentiometers to be driven via extended filter networks.

For numeral displays, the data input to the SAA1060 or SAA1062 must be seven-segment decoded by the microcomputer. The display and control facilities can be extended by using more than one IC of the same type. It will be shown that the additional ICs can be connected to the CBUS by using extra data enable (DLEN) lines and/or more clock (CLB) lines.

LED DISPLAYS AND CONTROL OF ANALOGUE FUNCTIONS WITH SAA1060

The integrated circuit

The integrated LED display interface circuit SAA1060 converts up to 16 bits of serial data to parallel form for driving LED function indicators or segmented numeral displays. Facilities are provided for duplex operation so that up to 32 bits of data can be time-division multiplexed at the 16 outputs. Since the circuit does not incorporate a 7-segment decoder (this function is performed by the microcomputer when driving numeral displays), it can also be used to operate d.c.-controlled integrated source selectors, switches and active filters. If an external binary-weighted resistor network is used to effect the necessary D-to-A conversion, the circuit can also be used to drive LED bargraph displays and to operate d.c.-controlled electronic potentiometers. A block diagram of the SAA1060 is given in Fig.2(a).

The data format for the SAA1060 is shown in Fig.2(b). The display data is transmitted from the microcomputer via the CBUS as 18 bits of information comprising a leading zero followed by a 17-bit data word composed of 16 data bits followed by a load selection bit. The bus control stage distinguishes between noise on the CBUS and valid data by verifying the presence of the leading zero with the data line enable (DLEN) signal HIGH during the first clock (CLB) pulse. The shift register is then enabled and the 17-bit data word is written in.

If the word length is correct, the data is accepted and the bus control stage feeds a 'valid' pulse to the load control stage. This stage then activates the enable line to data latch A or B, thereby allowing the contents of the shift register to be transferred to the selected latch on the 19th clock pulse with DLEN LOW. Which data latch is selected depends on the state of the load selection bit (bit 17 of the data word). If the load bit is HIGH, the data is transferred to latch A. If the load bit is LOW, the data is transferred to latch B. The contents of the selected data latch determines the state of the open-collector outputs in such a way that they are LOW for LOW data bits. The state of the data bits is therefore a direct representation of the state of the segments of a common-anode display. Outputs Q_8 and Q_{16} are capable of sinking up to 80 mA d.c. so that they can each drive two parallel-connected display segments (e.g. the numeral 1 for the most significant digit of a display). All the other outputs can sink up to 40 mA d.c.

The logic level applied to input LOEX determines whether the data is loaded directly into the selected data latch (static drive of up to 16 display segments or LEDs) or loaded in synchronism with the falling edge of the next DUP pulse (duplex drive of 2 x 16 numeral segments). When operating in the static mode, input LOEX must be HIGH. When operating in the duplex mode, LOEX can be either HIGH or LOW.

When the circuit is operating in the duplex mode, the contents of data latch A are presented at the outputs when DUP is LOW; the contents of data latch B are presented at the outputs when DUP is HIGH. If the DUP signal is derived from a half-wave rectified a.c. voltage applied to one of the two groups of common anodes, the output switching will occur during the zero crossing of the anode supply. Since little or no current is flowing at this instant, radiated interference due to switching transients is minimised. During duplex operation, the display data must be presented as two words separated

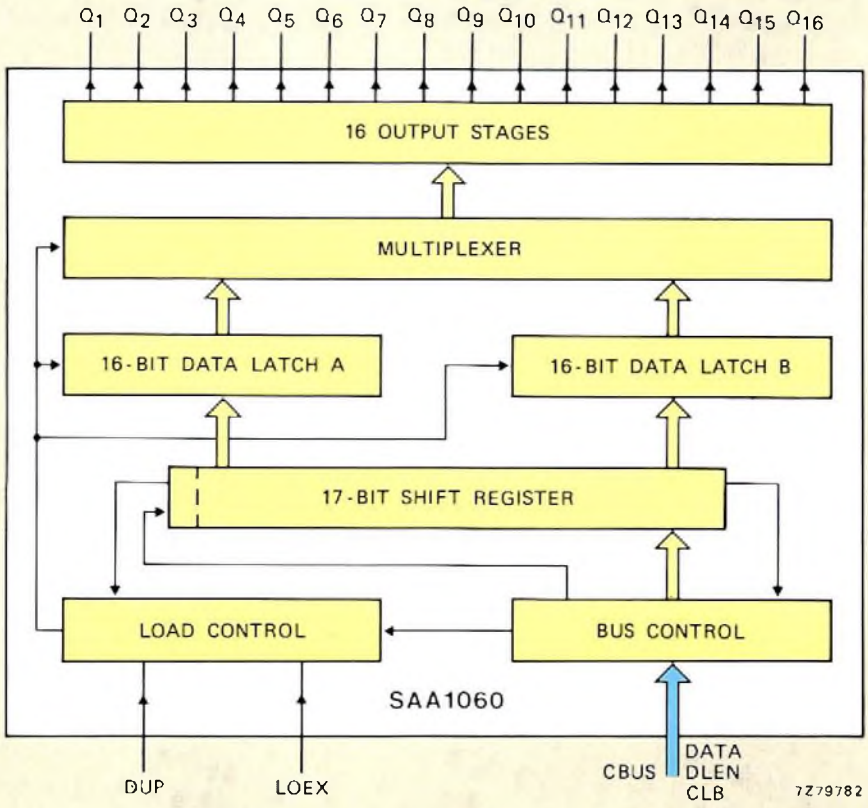


Fig.2(a) LED display/interface circuit SAA1060

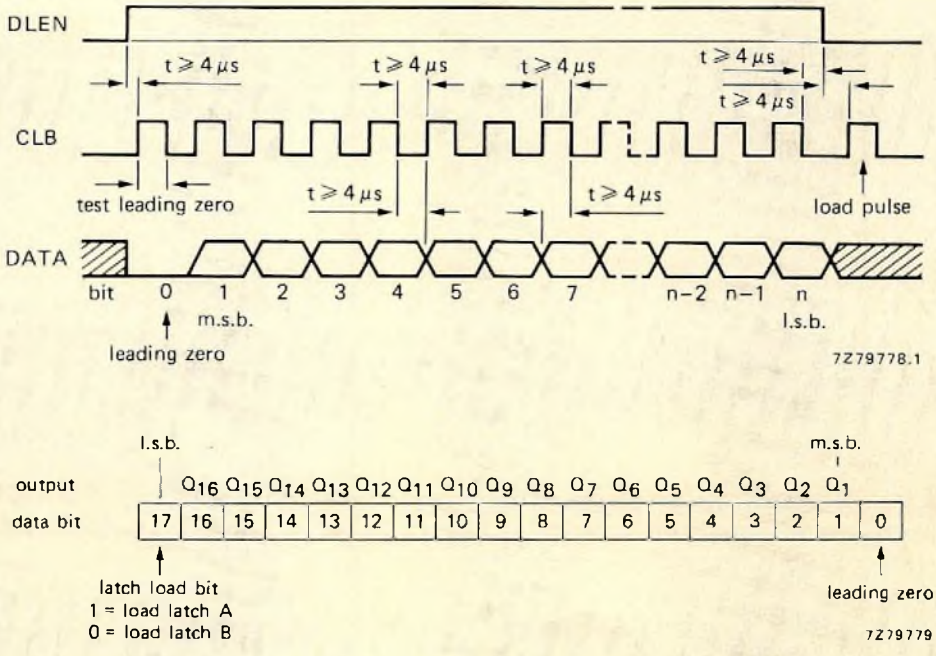


Fig.2(b) SAA1060 data format

by an interval greater than the period of the a.c. supply from which the anode drive pulses are derived (i.e. greater than 20 ms for a 50 Hz anode supply). The a.c. current sinking capability of the outputs during duplex operation is 120 mA peak for outputs Q_8 and Q_{16} and 60 mA peak for all the other outputs.

When operating the SAA1060 in the duplex mode, the segments of the display are divided into two groups. The common anodes associated with one of the groups of segments are fed with a.c. positive half-cycles (V_A). The anodes associated with the other group of segments are fed with a.c. positive half-cycles phase shifted 180° with respect to V_A. The IC requires a 5 V d.c. supply. When operating the SAA1060 in the static mode, the common anodes of the display also require a d.c. supply. A typical power supply circuit for either operating mode is given in Fig.3.

A typical frequency/channel number display

Figure 4 is the circuit diagram of a typical frequency/channel number display in which the SAA1060 drives 7-segment LED indicators in the duplex mode. In an a.m. radio, the display would require four digits capable of displaying 0 to 9999 kHz. For f.m., a 4½-digit display capable of indicating from 0 to 199.99 MHz is required. A 4½-digit display is shown in the diagram. Figure 4 is used as a basis for the following design recommendations and description of the data format.

For duplex 50 Hz operation, input LOEX of the SAA1060 may be either HIGH or LOW, the display segments must be divided into two groups (group A and B), the common anodes of each group must be fed with alternate positive-going supply pulses, and the display data must be provided by two data words (word A and word B) separated by an interval of more than 20 ms if LOEX is LOW. As previously explained, the state of the 17th bit of each data word steers the data to the correct latch in the SAA1060.

From Fig.4 it can be seen that, if there is a positive voltage on the common anode of a digit indicator when there are LOW levels on the appropriate cathodes, the digit will light up. The contents of the latch containing the associated data word must therefore be presented at the outputs of the SAA1060 coincident with the voltage pulse at the corresponding common anode. This synchronisation is achieved by deriving the DUP signal from one of the anode pulse trains (V_B) so that the contents of latch B are presented at the outputs (DUP = HIGH) when the anodes of segment group B are positive. The contents of latch A are then presented at the outputs (DUP = LOW) when the anodes of segment group A are positive.

The following basic design rules should be followed:

- Divide the segments of the required display into two groups of approximately equal number (16 max). Designate one group as group A and the other as group B.
- Connect the cathodes of the segments in pairs (one from group A, one from group B), via a current limiting resistor, to the outputs of the SAA1060. If necessary, two pairs of segments can be connected to

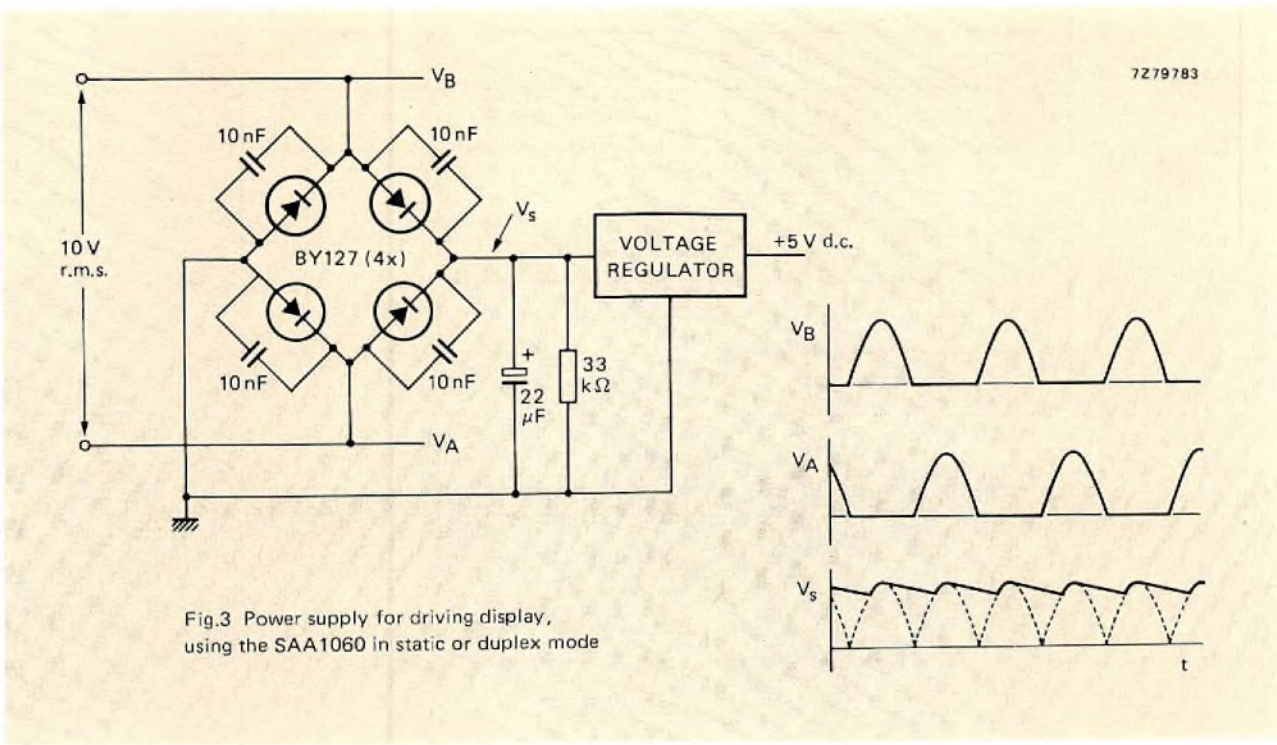


Fig.3 Power supply for driving display, using the SAA1060 in static or duplex mode

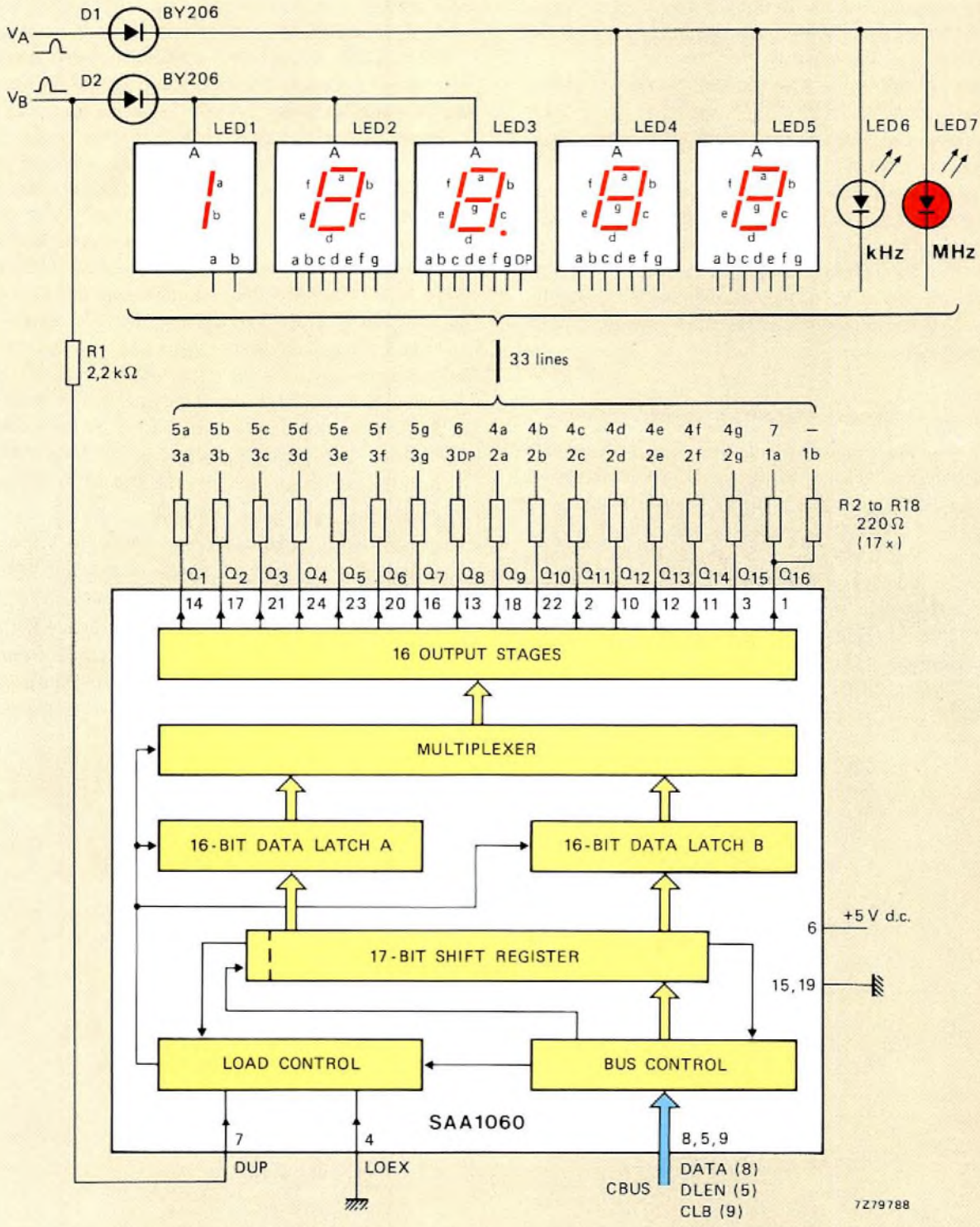


Fig.4 Typical frequency/channel number display circuit

outputs Q_8 and/or Q_{16}. The value of the current limiting resistor can be calculated from:

$$R \leqslant \frac{1.4\,V_{rms} - 2V_d - V_f - V_{QL}}{I_{peak}}$$

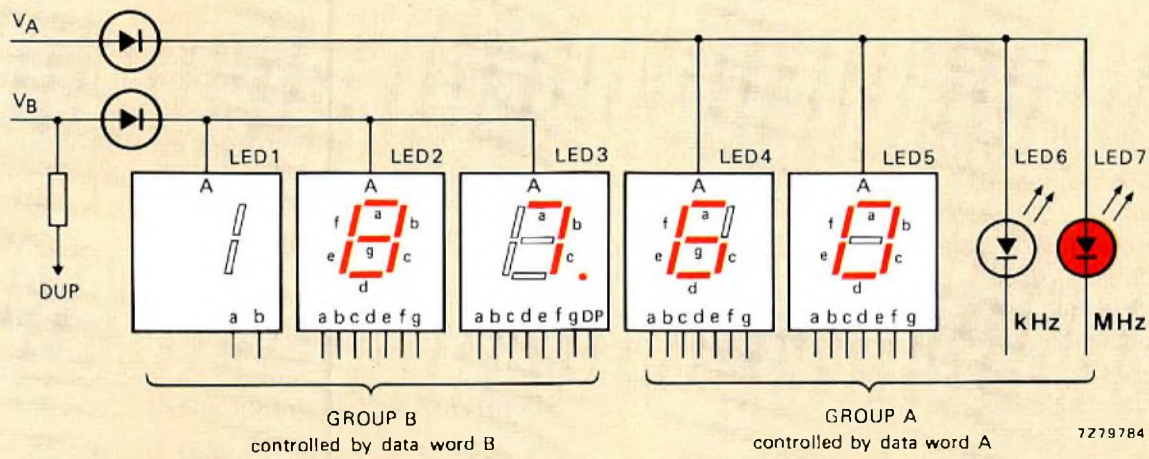
where

V_{rms} = the rms value of the anode supply voltage
V_d = the forward voltage across a BY127 diode (≈0.7 V)
V_f = the forward voltage across a LED segment (≈1.5 V)
V_{QL} = the maximum LOW state output voltage from the SAA1060 (0.5 V)
I_{peak} = the required peak segment current

– Connect the common anodes of the indicators in group A and group B, via diodes to V_A and V_B respectively.

– Derive the DUP pulses from V_B via a resistor to limit the input current to about 6 mA (12 mA max), i.e. $R = 1.4\,V_{Brms}/0.006$.

The composition of the two display data words is best illustrated by an example. Assume that it is required to display the frequency 87.60 MHz as shown in Fig.5. The relationship between the contents of the data latches, the IC outputs and the indicator segments for the circuit of Fig.4 is given in the Table. From Fig.5, it can be seen that data word A controls LED4, 5, 6 and 7 and must therefore command the display 60 MHz. The segments to be lit are thus 4a, 4d, 4e, 4f, 4g, 5a, 5b, 5c, 5d, 5e, 5f and 7. Since an active segment is defined by a LOW data bit, it can be seen from the Table that bits 1 to 6, 9 and 11 to 16 of data word A must be LOW. Data bit 17 must be HIGH to indicate that the data must be steered to latch A. The complete data word is shown in Fig.5.



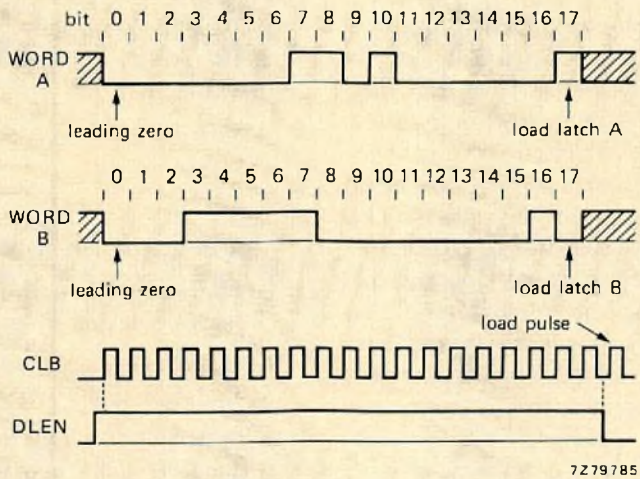


Fig.5 Data format for displaying numerals 87.60

Relationship between the contents of the data latches, the IC outputs and the indicator segments in Fig.4

bit of word in latch	SAA1060 output	latchA LED/segment	latch B LED/segment
1	Q_1	5a	3a
2	Q_2	5a	3b
3	Q_3	5c	3c
4	Q_4	5d	3d
5	Q_5	5e	3e
6	Q_6	5f	3f
7	Q_7	5g	3g
8	Q_8	6	3DP
9	Q_9	4a	2a
10	Q_{10}	4b	2b
11	Q_{11}	4c	2c
12	Q_{12}	4d	2d
13	Q_{13}	4e	2e
14	Q_{14}	4f	2f
15	Q_{15}	4g	2g
16	Q_{16}	7	1a and 1b
17	–	HIGH	LOW

Word B controls LED1, LED2 and LED3 and must command the numeral 8 for LED2 and the numeral 7 followed by a decimal point for LED3. From Fig.5, it can be seen that the segments to be lit for this display are 2a, 2b, 2c, 2d, 2e, 2f, 2g, 3a, 3b, 3c and 3DP. Table 1 shows that the LOW bits for data word B are 1 to 3 and 8 to 15. In this case, data bit 17 must be LOW to indicate that data word B must be steered to latch B. The complete data word is shown in Fig.5.

A typical control position display

With conventional analogue control of audio functions, the control positions are indicated to the user by the visible position of switch levers, knobs, dials etc. When the analogue functions are electronically controlled, as in RTS, the control positions of electronic potentiometers and switches must be indicated by electronic means such as 7-segment numeral indicators, bargraphs and LED lamps. Figure 6 shows the SAA1060 being used in duplex mode to drive 7-segment LED numeral indicators and LED lamps which indicate the control positions of electronic potentiometers for adjusting bass response, treble response and volume. The circuit is designed on the same principles as previously described for frequency and channel number displays.

Using multiple display interface circuits

Since the SAA1060 can control and drive displays for a wide variety of analogue functions, it will often be necessary to use more than one of these circuits in an RTS. One or more of the following four methods can then be used to allow the circuits to share a common DATA line:

- Use separate DLEN or CLB lines for each SAA1060.
- Use multiple DLEN and CLB lines so that each SAA1060 receives a different combination of clock and data line enable signals. For example:

IC1	DLEN1	CLB1
IC2	DLEN1	CLB2
IC3	DLEN2	CLB1
IC4	DLEN2	CLB2

- When using two SAA1060 circuits, invert the data words for one IC and connect an inverter in the DATA line to that IC. The leading zero check in the other IC will then cause the inverted data word to be rejected.
- The state of the 17th bit of the data words transmitted to the SAA1060 determines the data latch in which the word will be stored. The state of input DUP determines which data latch contents will be displayed. If more than one SAA1060 is used in the static mode (LOEX = HIGH), the DUP inputs can be programmed so that each IC will only accept data in which the state of the 17th bit is not the same as the state of the DUP input.

Control of switching functions

In addition to acting as a LED indicator driver, the SAA1060 can also be used to perform signal switching functions via d.c.-controlled static switches, band-switching diodes and logic-level controlled inputs of the stereo decoder and search tuning circuits. Typical of these functions are:

- Waveband selection via band-switching diodes in the tuner.
- Mono/stereo switching at the decoder.
- Muting interstation noise (silent tuning).
- Selection of search tuning criteria e.g. local stations (high signal strength) or stereo broadcasts.
- Audio source selection (phono, tape, radio) via 2-pole 4-position source selector TDA1029.
- Switching of rumble and scratch filters, mono/stereo, monitor, audio muting, contour, etc. via 4-pole, 2-position source selectors TDA1028.

A typical switch control and function display circuit is given in Fig.7. The TDA1028 and TDA1029 are fully described in Part 5 of this article.

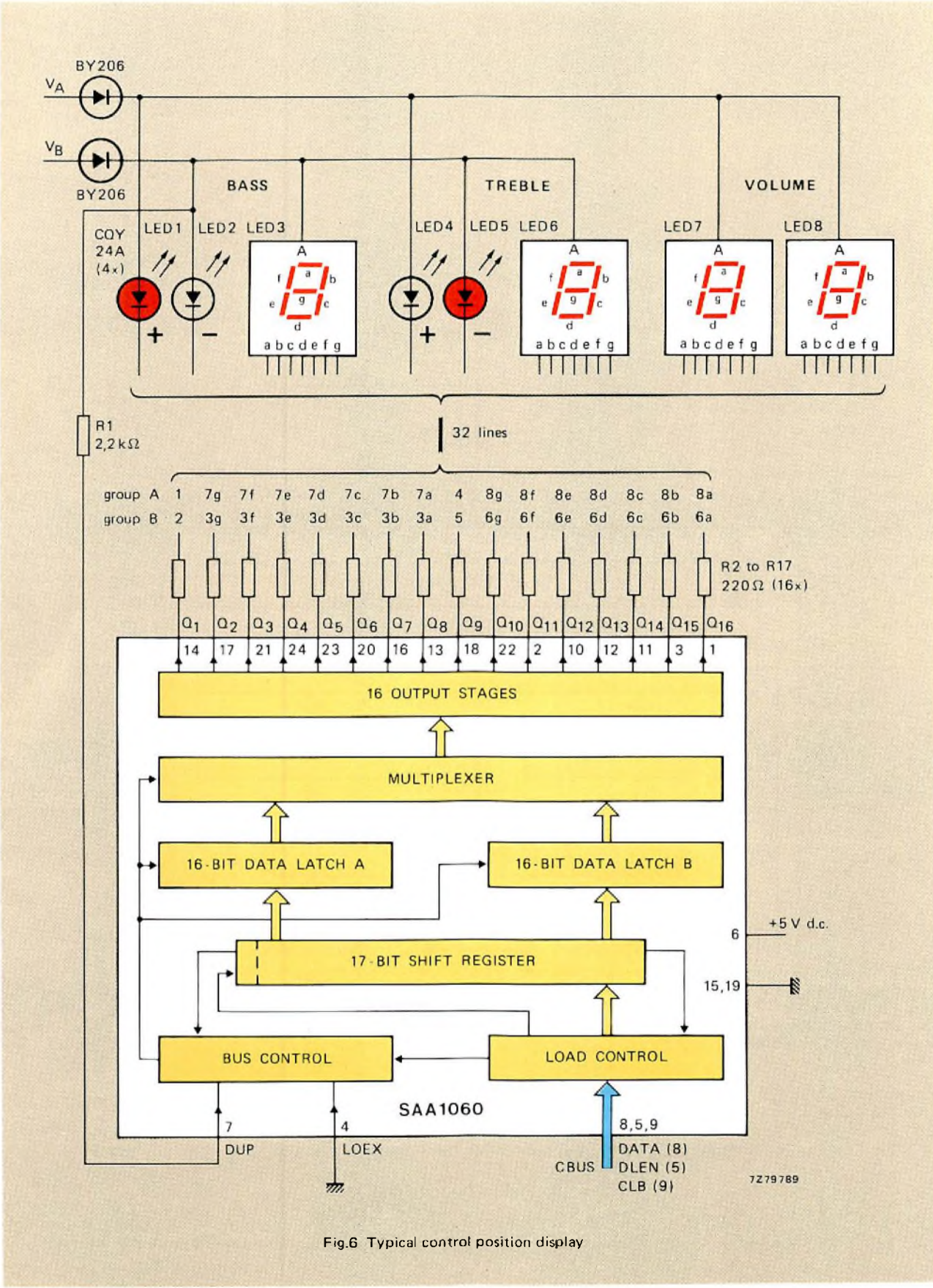


Fig.6 Typical control position display

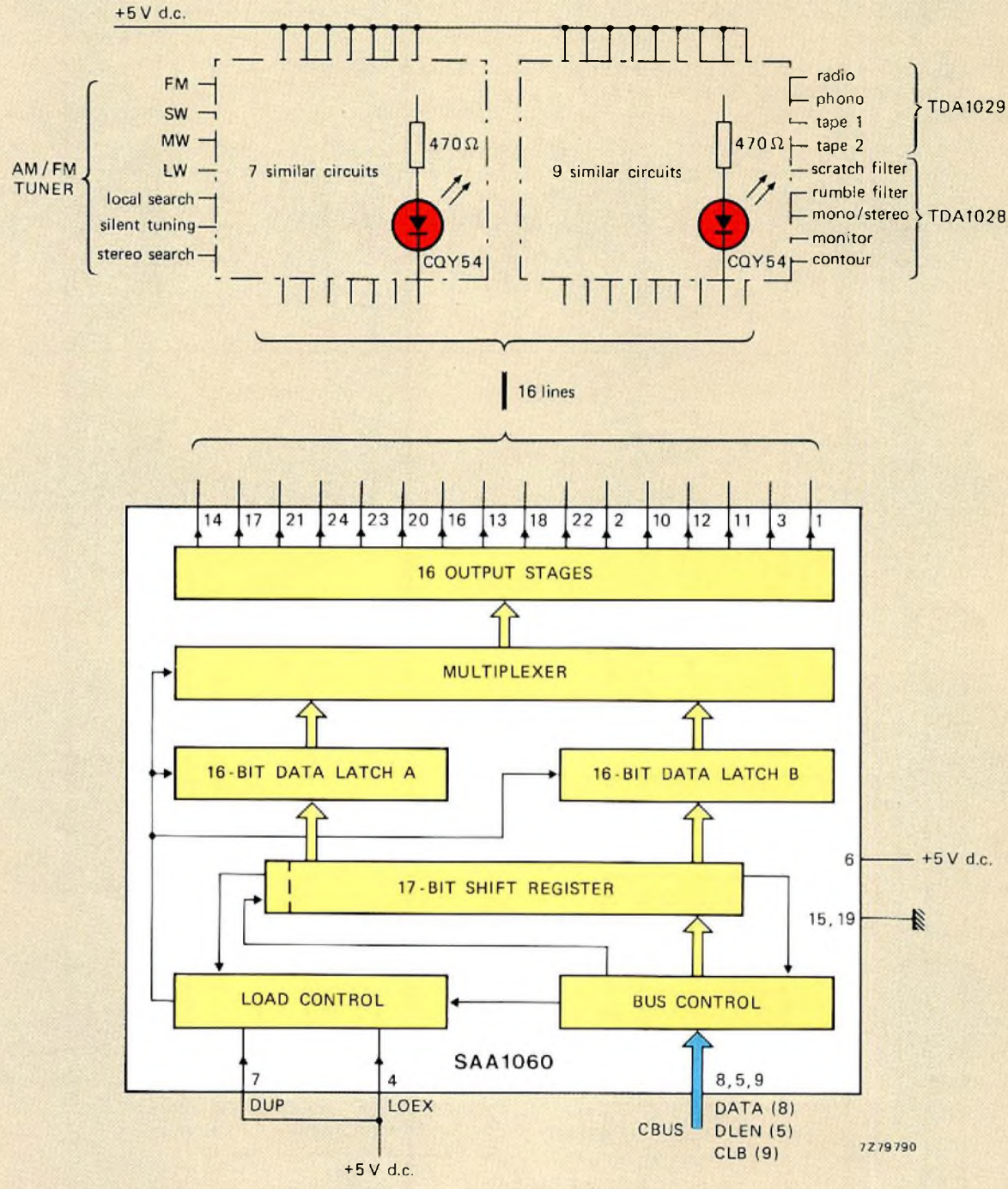


Fig.7 Typical switch control and display circuit

Control of analogue signal functions

If simple binary-weighted-resistor network D-to-A converters are connected to the outputs of the SAA1060, can be used to control analogue signal functions such as volume, bass response, treble response, stereo balance, etc. via integrated electronic potentiometer circuits TDA1074A*. A typical analogue signal control circuit is given in Fig.8. In this circuit, bass and treble response are each controlled via a 4-bit binary-weighted resistor network D-to-A converter and a TDA1074A to achieve $2^4-1=15$ control increments (e.g. flat and ±7 steps). Stereo balance control is obtained by varying the gain of the stereo channels with opposite sign via similar D-to-A converters and a second TDA1074A. 64-increment volume control can be effected by using six outputs of a second SAA1060 and a 6-bit D-to-A converter to simultaneously control the gain of both stereo channels with the second TDA1074A. The remaining ten outputs of

* A second integrated electronic potentiometer circuit, specifically designed for volume and balance control, will be available shortly.

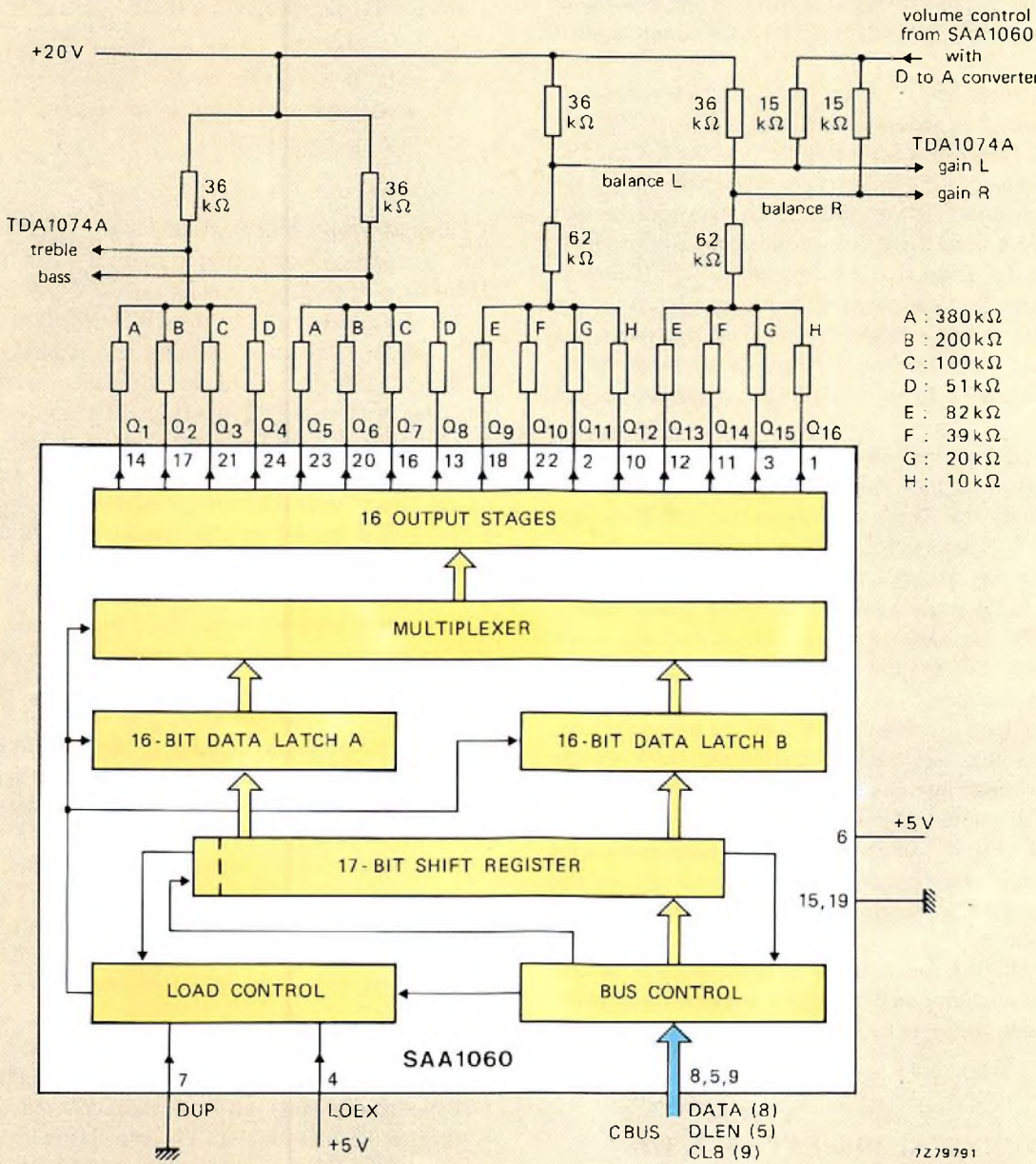


Fig.8 Typical analogue signal control circuit using SAA1060

the second SAA1060 could be used to provide LED bargraph or 7-segment numeral indication of the balance control setting. The bass, treble and volume control setting indication has already been described with the aid of Fig.6.

The integrated electronic potentiometers will be fully described in a later article.

CONTROL OF ANALOGUE SIGNAL LEVELS WITH THE SAB3013

The computer-controlled analogue memory SAB3013 provides 64-increment digital control of up to six analogue signal levels. A block diagram of the circuit is given in Fig.9.

The circuit is controlled by six 12-bit data words each incorporating a leading zero as shown in Fig.10. The data is derived from the microcomputer via the CBUS. The two bits following the leading zero of each data word are coded to correspond with the 2-bit system address code on inputs SAA and SAB. This allows up to four SAB3013 circuits to be driven from a common CBUS. The next three bits of the data word are the binary address for the appropriate analogue latch. The six most significant bits of the data word are binary coded to represent the required increment (0 to 63) for the selected analogue function.

The data received from the CBUS is temporarily stored in the data buffer. If there is a leading zero, DLEN is LOW (data complete), and twelve data bits have been received, a 'valid' signal is passed to the latch/load control on the trailing edge of the next clock pulse on input CLB. This allows the data to be synchronously loaded into the selected latch. During loading, signal $\overline{\text{BUSY}}$ goes LOW and the reception of further data from the CBUS is inhibited.

The contents of the data latches are internally converted into pulse-width modulated outputs with a cycle time of 64 clock periods and a duty factor proportional to the analogue values as shown in Fig.11. As shown in Fig.9, external RC filters smooth the pulse-width modulated outputs to obtain d.c. control voltages for the two integrated electronic potentiometer circuits TDA1074A.

The SAB3013 can be used with the internal 30 kHz to 1 MHz oscillator or with externally-generated clock pulses within the same frequency range.

LIQUID CRYSTAL DISPLAY WITH THE SAA1062

The LCD interface circuit SAA1062 is a CBUS-compatible 17 or 20-bit serial to parallel converter with an internal circuit for generating an a.c. drive signal for connection to the common electrode (backplane) of a liquid crystal display. The circuit incorporates internal data validation and is capable of operating in one of the following three modes:

- Synchronous master mode. Valid data is presented at the outputs in synchronism with the internally-generated backplane drive signal.
- Slave mode. The backplane driver is inhibited and the data, if valid, is presented at the outputs in synchronism with an externally-generated (by another SAA1062) backplane drive signal.
- Static mode. The backplane driver is inhibited and the data, if valid, appears directly at the outputs. In this mode, the circuit can be programmed to invert the data at the outputs.

A block diagram of the SAA1062 is given in Fig.12. The data from the microcomputer consists of an 18-bit or 21-bit word including a leading zero as shown in Fig.13.

The data received from the CBUS is loaded into the shift register. If there is a leading zero, DLEN has gone LOW (data complete) and the correct number of data bits have been received (18 bits for BLS = HIGH, 21 bits for BLS = LOW), the bus control stage generates a load latch pulse (LOL) which allows the data to be transferred to the latch (synchronous or slave mode) or output buffer (static mode) on the trailing edge of the next CLB pulse.

In the synchronous mode, an external 22 nF capacitor is connected between input C_{ext} and ground, and an internally-generated 60 Hz backplane drive signal is available at output/input AC/EL for connection to the common electrode of the LCD. The data word, if valid, is transferred from the register to the latch at the next CLB pulse after generation of the LOL pulse and is then transferred to the output buffer in synchronism with the backplane drive signal.

In the static mode, input C_{ext} is connected to V_{CC} and output/input AC/EL is connected to a logic LOW level so that the data will be inverted at the outputs. The internally-generated backplane signal is inhibited and the data, if valid, is transferred directly from the register to the outputs.

In the slave mode, input C_{ext} is connected to V_{EE}, the internally-generated backplane drive signal is inhibited and the data, if valid, is transferred from the register to the latch by the CLB pulse following the LOL pulse. The data is transferred from the latch to the output buffer in synchronism with an externally-generated (by another SAA1062) backplane drive signal connected to output/input AC/EL.

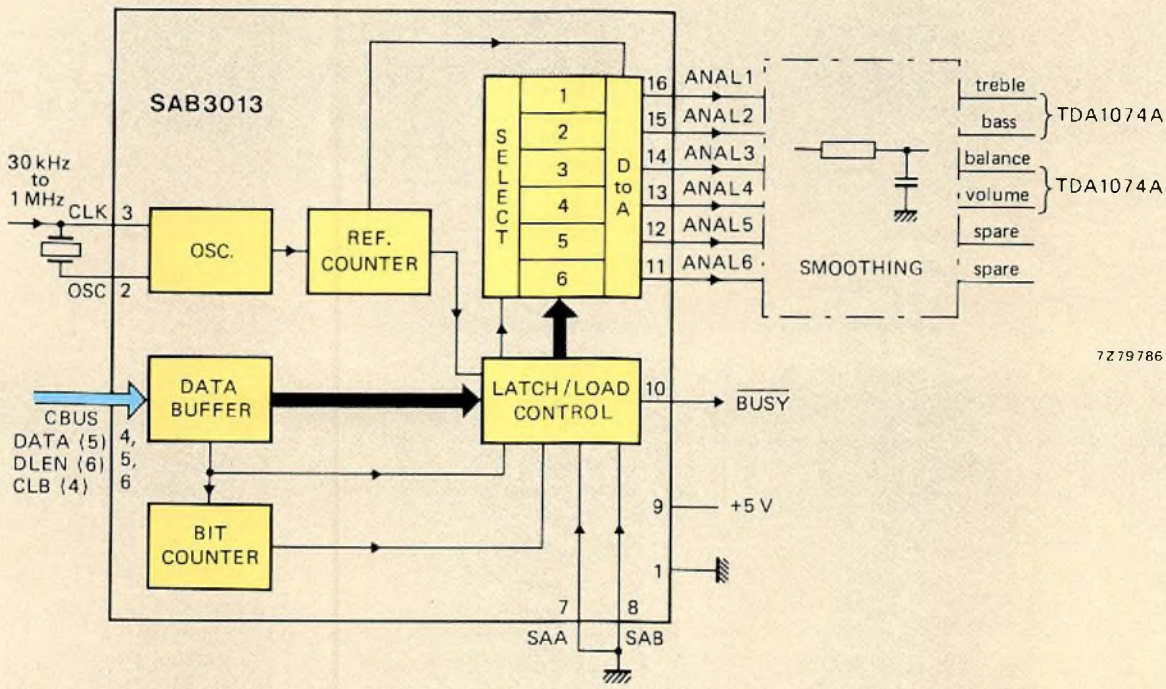
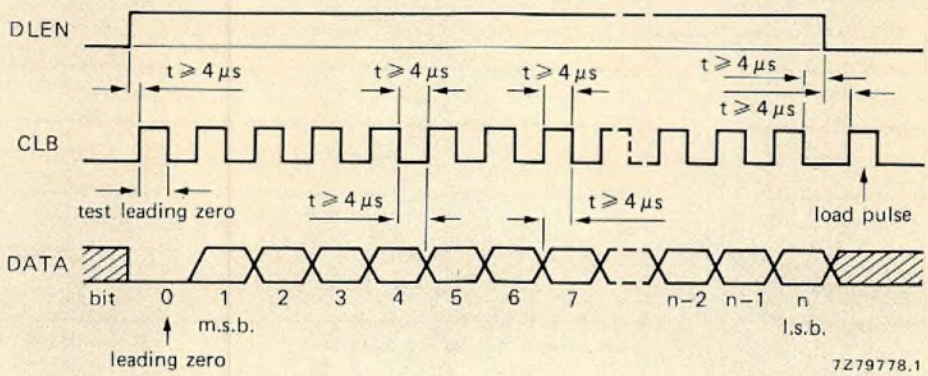


Fig.9 Typical analogue signal level control circuit using SAB3013



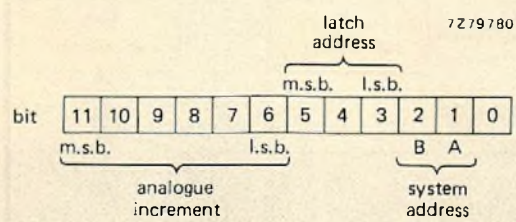


Fig.10 SAB3013 data format

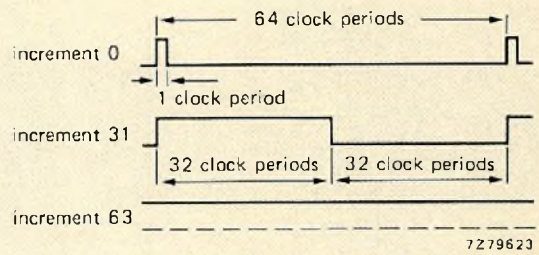


Fig.11 Pulse-width modulated analogue outputs from the SAB3013

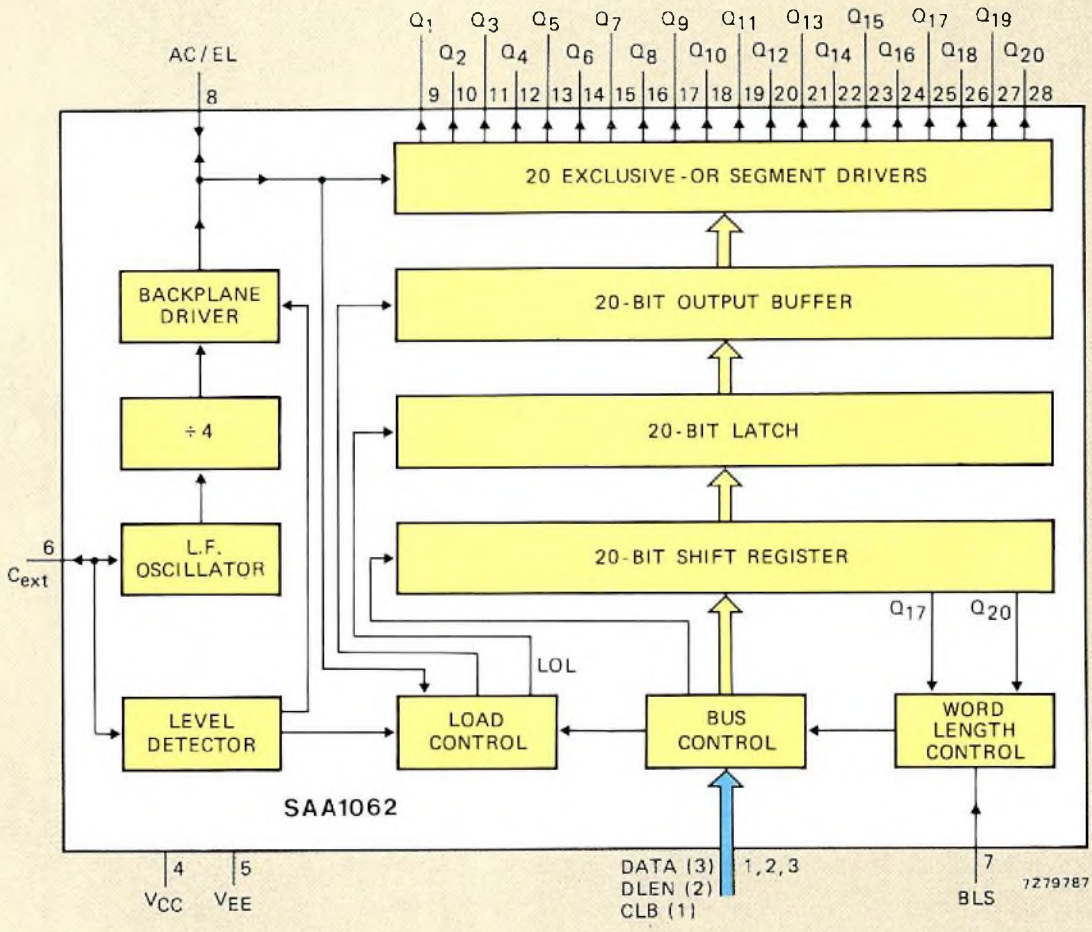
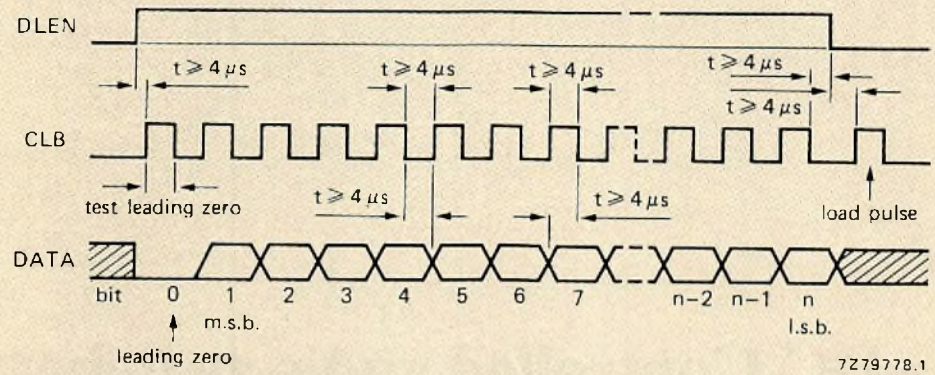


Fig.12 LCD display/interface circuit SAA1062



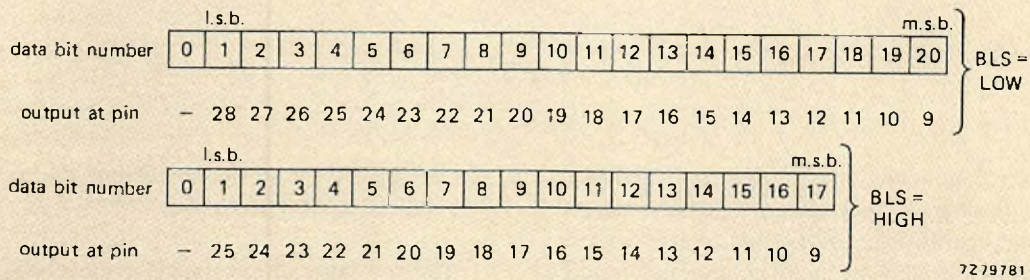


Fig.13 Data format for the SAA1062

The previous parts of this article appeared in earlier issues of Electronic Components and Applications as follows:

Part 1 — Frequency measurement and display system for a.m. and f.m. radios. Vol. 1, No. 2

Part 2 — Voltage converter and memory for preset radio tuning. Vol. 1, No. 4

Part 3 — Introduction to microcomputer-controlled radio tuning system. Vol. 1, No. 4

Part 5 - DC-Controlled audio switches and filters

E. A. KILIAN

The use of semiconductors, integrated circuits and small high-quality passive components on densely packed printed-wiring boards has contributed much towards reducing the size of radio and audio circuits and improving their performance and reliability. The front-panel layout and reliability of modern units in slim-line and mini cabinet format however, is still restricted by the necessity of using electro-mechanical components such as switches and potentiometers. These precision miniature components are costly to manufacture and install, and are subject to wear and contamination. Furthermore, to avoid crosstalk, instability due to positive feedback and spurious electrical pick-up, they must be carefully positioned, adequately screened, and connected to the controlled circuits via expensive and bulky shielded cables.

To overcome these problems, we have developed a new range of d.c.-controlled integrated circuits which can perform most of the required switching, filtering and level control functions in radio and audio equipment. In manually-controlled units, front-panel switches must still be used to control the integrated circuits. But, since they only have to switch d.c. on and off, they can be simple switches operated by low-profile pocket calculator style pushbuttons. The absence of a.c. signals on the control lines to the ICs completely eliminates the previously imposed control positioning strictures and also allows the circuits to be used in digitally-controlled systems such as our Radio Tuning System (RTS) as described in Part 4 of this article. In this case, the circuits are driven by the microcomputer data via serial to parallel decoders SAA1060.

The new range of integrated circuits comprises:

TDA1028 – Signal sources switch.

TDA1029 – Signal sources switch.

TCA730 A and TDA1073 – D.C.-controlled volume and balance control circuit.

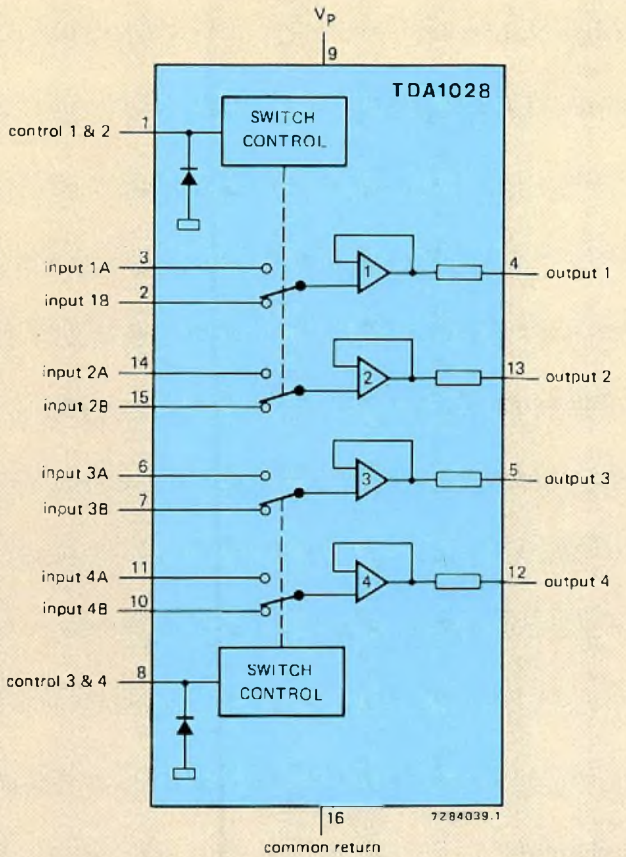
TCA740A and TDA1074A – D.C.-controlled tone control circuit.

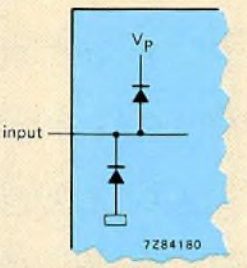
This part of the article describes the TDA1028 and the TDA1029. The other circuits will be described in future parts of the article.

The TDA1028 shown in Fig.1 contains two pairs of single-pole, two-position electronic switches. The TDA1029 shown in Fig.2 contains one pair of single-pole, four-position electronic switches. Typical stereo switching functions performed by the circuits are:

- Source selector with up to four inputs (TDA1029).
- Source selector with up to five inputs (½TDA1028 + TDA1029).
- Source selector capable of switching up to seven inputs (two TDA1029).
- Mono/stereo selector switch (½TDA1028).
- Muting on/off switch (½TDA1028).
- Monitor selector with on/off switch (½TDA1028).

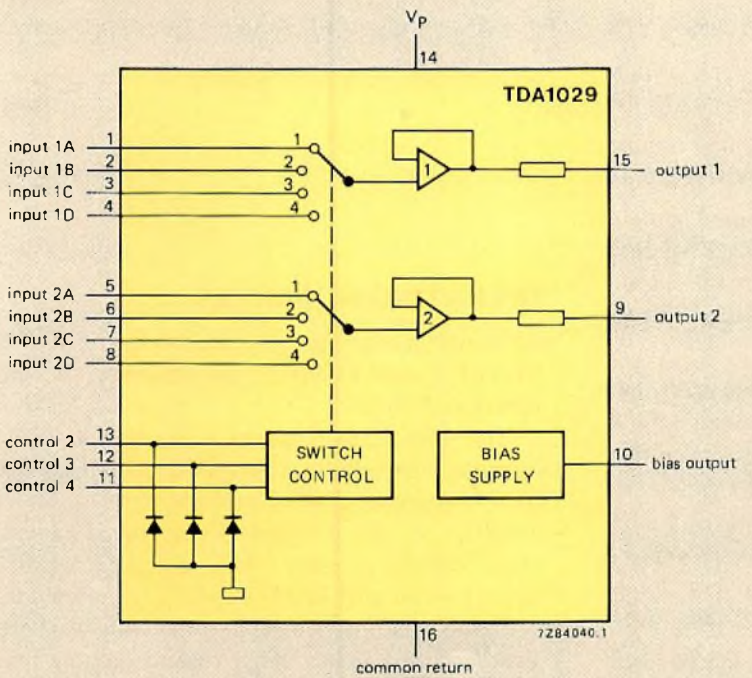
More extensive information for potential users is available in a separate publication. Requests for copies should mention this article, and the nature of the applicant's interest.

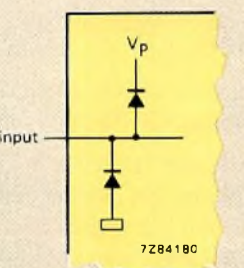




Internal diodes connected to each input

Fig.1 Block diagram of TDA1028





Internal diodes connected to each input

Fig.2 Block diagram of TDA1029

TABLE 1
Analogue switch characteristics

	Bipolar	MOS
crosstalk attenuation* (R_S = 47 kΩ, f = 20 kHz)	60 dB	58 dB to 62 dB
total harmonic distortion (R_S = 4.7 kΩ, f = 20 kHz, $V_i \leq$ 5 V r.m.s.)	0.03% ($R_L \geq$ 4.7 kΩ)	≈ 0.1% ($R_L \geq$ 470 kΩ)
total harmonic distortion (R_S = 47 kΩ, f = 20 kHz, $V_i \leq$ 5 V r.m.s.)	0.03% ($R_L \geq$ 4.7 kΩ)	0.5% to 1% ($R_L \geq$ 470 kΩ)
total harmonic distortion when driven via an emitter follower (R_S = 47 kΩ, f = 20 kHz, V_i = 5 V r.m.s.)	0.1% ($R_L \geq$ 4.7 kΩ)	0.1% ($R_L \geq$ 470 kΩ)
noise voltage with direct drive (R_S = 47 kΩ, f = 20 Hz to 20 kHz)	5 μV	6 μV to 7 μV
noise voltage with emitter follower (R_S = 47 kΩ, f = 20 Hz to 20 kHz)	12 μV	14 μV
switch actuation (each position)	1 pin to 0 V or LOW level	3 or 4 pins to HIGH and LOW levels

* non-selected input to selected input.

Since the TDA1028 and TDA1029 incorporate a unity-gain operational amplifier in each output signal path, it is also possible to introduce frequency-selective feedback between input and output and thereby construct active audio-frequency filters to perform such functions as:

- Rumble filter with in/out switch (½ TDA1028).
- Scratch filter with in/out switch (½ TDA1028).
- Loudness (contour) control with in/out switch (½ TDA1028).
- A four-function circuit which can select mute/rumble filter/subsonic filter/linear response (TDA1029).

The TDA1028 and TDA1029 are manufactured in bipolar technology. Since a number of MOS analogue switches are also available, it is interesting to compare the characteristics of switches using the two technologies. This is done in Table 1.

From the information in Table 1, it is apparent that the bipolar TDA1028 and TDA1029 possess several advantages not exhibited by other currently available integrated switch arrays. The main advantages are:

- Simple switching by connecting one wire to 0 V or logic LOW level for each switch position. This allows use of digital control or operation via very simple front panel switches.
- Low total harmonic distortion which is independent of source and load resistance. The TDA1028 and TDA1029 do not therefore need to be driven via emitter-followers.
- Low crosstalk between non-selected and selected inputs.
- Signal input up to 6 V r.m.s. and input impedance up to 470 kΩ.
- The circuits can also be connected as switched active filters. This cannot be achieved with other available switch arrays without using additional active components.

OPERATING PRINCIPLES

Although the switching functions performed by the TDA1028 and TDA1029 are different, the mode of operation is similar.

The pole of each switch is connected to the non-inverting input of an operational amplifier. Full feedback is internally applied to the inverting input of each amplifier so that the gain of each signal path is accurately defined as unity. As a safeguard against short-circuit, an internal 400 Ω resistor is connected in series with each output. An input protection network consisting of two diodes and a current limiting resistor is connected to each signal input. The transfer characteristic of each switch is essentially linear for d.c. inputs from 3 V to Vp – 1 V. With a 20 V supply, this allows

TABLE 2
Typical performance data

Supply voltage range	V_P	6 to 23	V
Operating ambient temperature	T_{amb}	−30 to +80	°C
Supply voltage	$V_{P\,typ}$	20	V
Signal input voltage (r.m.s.)	V_{i} typ	6	V
Voltage gain	G typ	1	
Distortion (V_i = 4.5 V r.m.s.)	d_{tot}	0.01	%
Crosstalk* (f = 1 kHz, R_S = 47 kΩ)	α typ	−80	dB
Signal-to-noise ratio (V_i = 500 mV, R_S = 47 kΩ)	S/N typ	100	dB
100 Hz hum rejection (R_S = 10 kΩ)	a_{100} typ	−80	dB
Current consumption (outputs unloaded)			
TDA1028	I_9 typ	2.9	mA
TDA1029	I_{14} typ	3.5	mA
Bias voltage from TDA1029	V_{10} typ	11	V

* non-selected input to selected input.

input signals up to 6 V r.m.s. Since the audio signals applied to the inputs will normally be symmetrical about 0 V, it is necessary to apply a d.c. bias voltage to each input. A suitable voltage is available from pin 10 of the TDA1029. To ensure the maximum permissible input signal excursion, the bias voltage from the TDA1029 remains at the centre of the permissible input voltage range regardless of supply voltage or temperature. Any unused inputs must be connected to the bias voltage. To minimise switching transients appearing at the outputs, the small d.c. offset currents (20 nA typ.) at the inputs are accurately matched and are independent of the switch position.

Each pair of switches is operated by applying a voltage level to the appropriate control input. With all of the control inputs disconnected (resistance to the common return at least 33 MΩ) or connected to a logic HIGH level greater than 3.3 V, the switches will be in the positions indicated in Fig.1 and Fig.2. With a control input connected to the common return or to a logic LOW level of less than 2.1 V, the switches will select the appropriate input. The maximum leakage current from a control input in the HIGH state is 1 μA. The maximum current into a control input in the LOW state is 200 μA.

An internal circuit in the TDA1029 ensures that, if more than one source is selected at the control input, only the signal associated with the control input with the lowest pin number will be passed to the output. Typical performance data for the circuits is given in Table 2.

APPLICATIONS

The possible circuit configurations for the TDA1028 and TDA1029 are far too numerous to describe in their entirety in this article. The following examples however, serve to illustrate the high performance and design flexibility which can be achieved with the integrated circuits.

The TDA1029 as a four-input stereo source selector

Figures 3a and 3b show the TDA1029 connected to select an input from one of four stereo signal sources. The RC filters connected to each of the tape and pick-up inputs prevent spurious r.f. signals from reaching the inputs of the TDA1029 where they would be demodulated. Recording inputs for the two tape recorders are derived from the outputs of the TDA1029. Bias current for each amplifier input is derived via 470 kΩ resistors connected between the internally-generated bias voltage (≈11 V) at pin 10 and each input pin of the TDA1029. The magnetic cartridge input to the TDA1029 is fed via a Signetics dual low-noise preamplifier type NE542 connected in a circuit which provides RIAA equalisation for record reproduction. The circuit is given in Fig.3b.

The crosstalk attenuation and channel separation performance of this circuit is considerably influenced by circuit layout, screening and types of input/output sockets used. The performance of a laboratory model is given at the end of this part of the article.

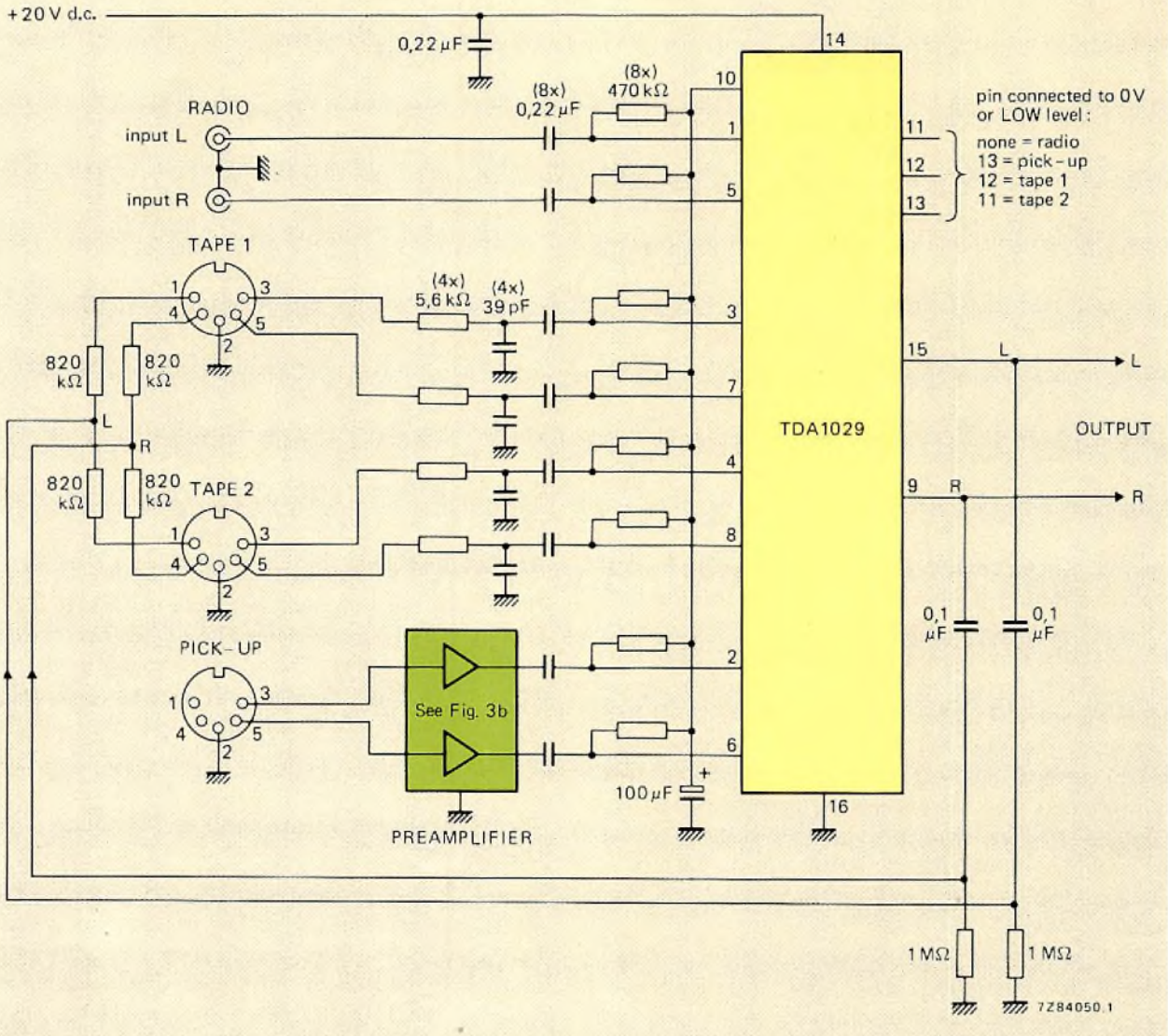


Fig.3(a) TDA1029 connected as a four-input stereo source selector

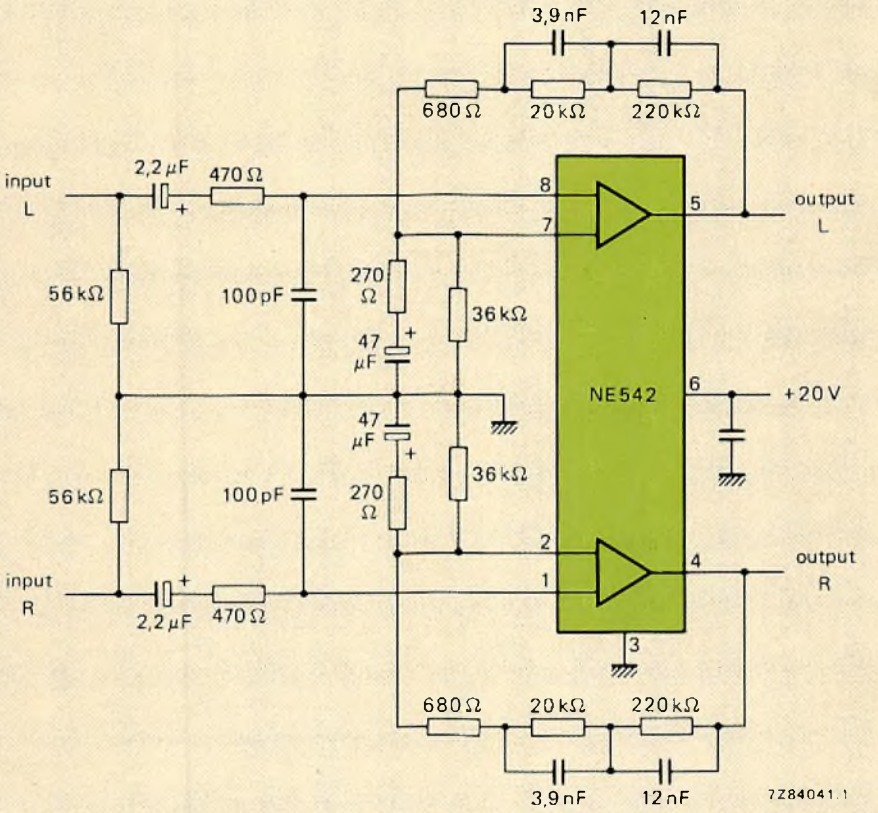


Fig.3(b) Signetics NE542 as a low-noise stereo preamplifier with RIAA equalization for magnetic cartridges

The TDA1029 and TDA1028 as a five-input stereo source selector with monitoring facility

Figure 4 shows how the TDA1028 can be used to extend the circuit of Fig.3a to incorporate an auxiliary input and an input from a tape monitor head. The latter facility permits recorded programme material to be compared with the source during recording. The monitor facility can only be used with a recorder that has a monitor head or separate record and playback heads.

The performance achieved with a laboratory model of this circuit is given at the end of this part of the article.

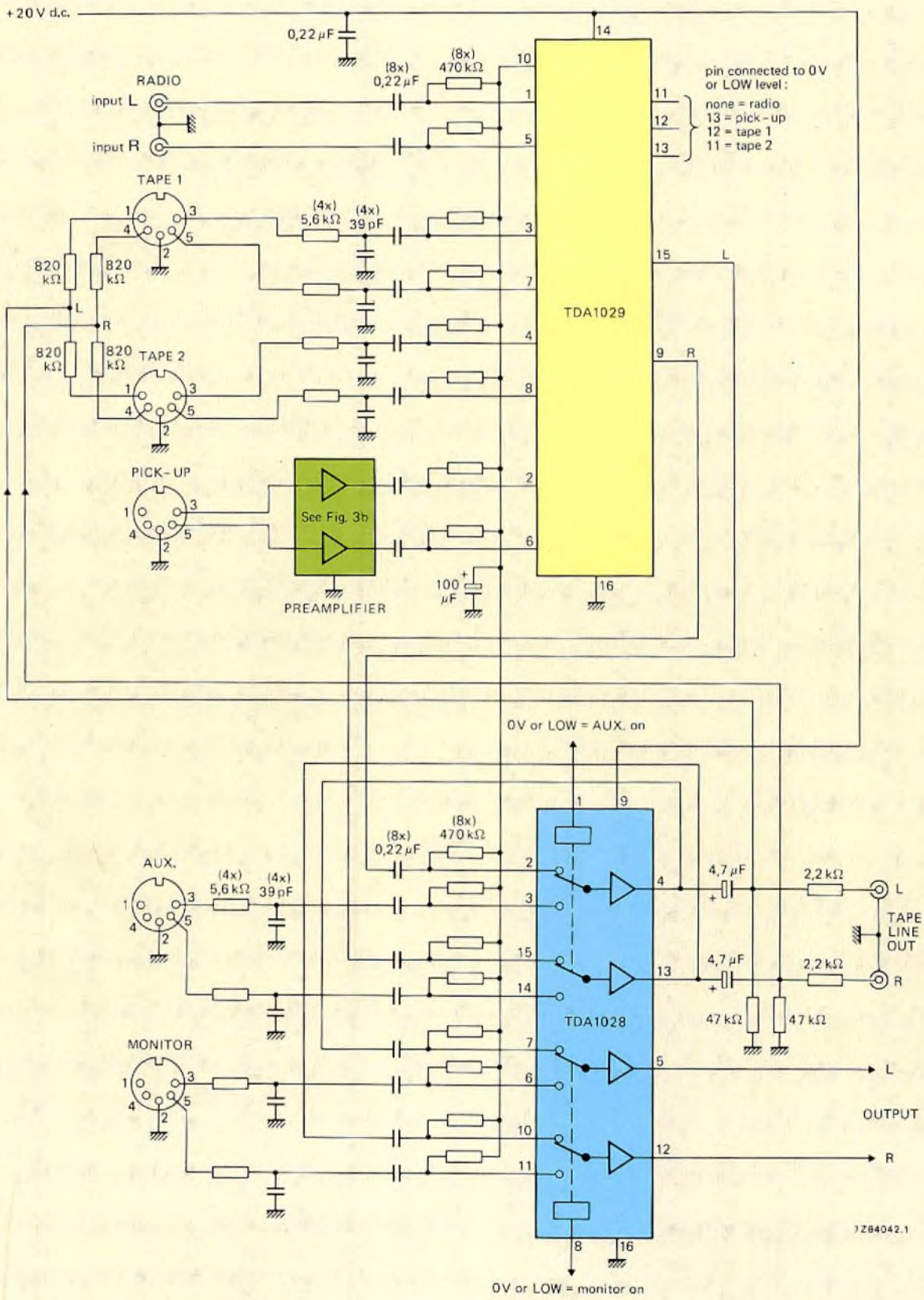


Fig.4 TDA1029 and TDA1028 connected as a five-input stereo source selector with monitoring facilities

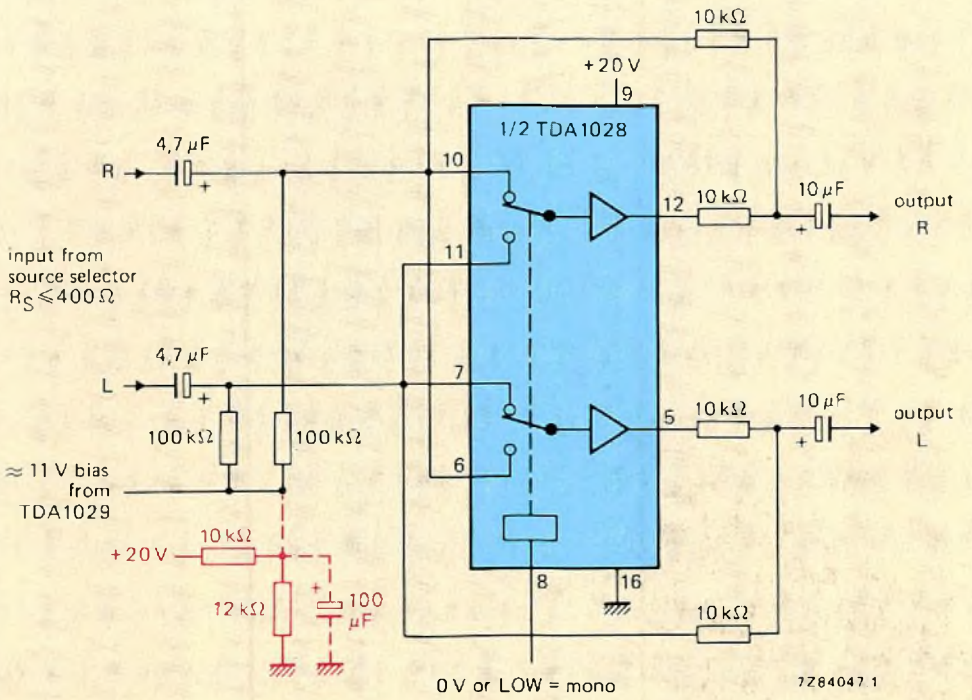
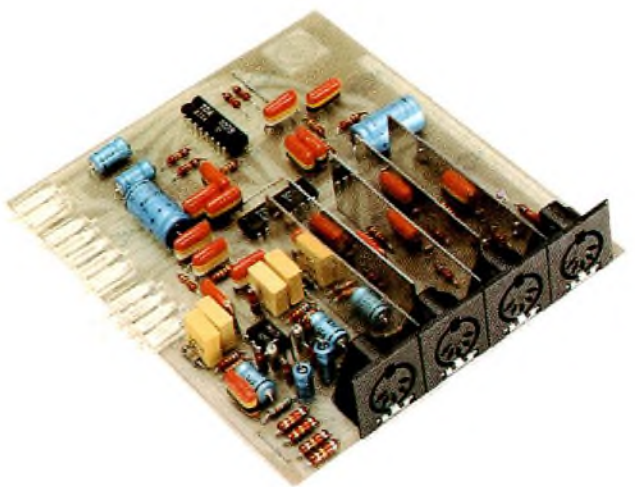


Fig.5 Half of the TDA1028 as a mono/stereo switch. The dotted circuit is an alternative method of obtaining the input bias if this circuit is not used in conjunction with the TDA1029 source selector



Laboratory model of the circuit arrangement shown in Fig 10

Half of the TDA1028 as a mono/stereo switch

Figure 5 shows one half of the TDA1028 connected as a mono/stereo switch. If the circuit is used in conjunction with the TDA1029 source selector, the input bias can be derived from pin 10 of the TDA1029. Otherwise, a separate voltage divider network (shown dotted in Fig.5) must be connected across the 20 V supply to obtain the bias of about 11 V.

With a source resistance of 400 Ω (TDA1029 output) the noise voltage over the frequency range 20 Hz to 20 kHz is 4 μV r.m.s. Under the same conditions, the stereo channel separation is 90 dB at 1 kHz, 82 dB at 10 kHz, 80 dB at 15 kHz and 77 dB at 20 kHz. The output impedance of the circuit is 5 kΩ.

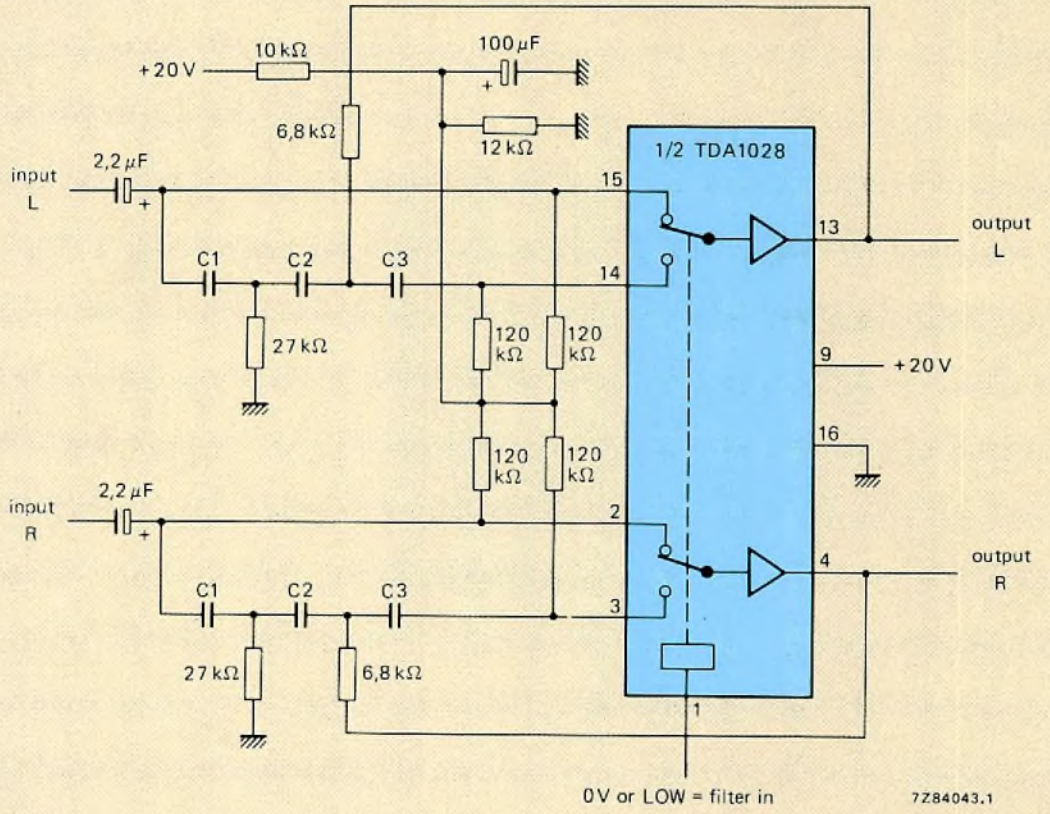


Fig.6 Half of the TDA1028 as a stereo high-pass (rumble) filter or a subsonic filter. For the rumble filter C_1 = 68 nF, C_2 = 33 nF, C_3 = 150 nF. For the subsonic filter C_1 = 0.33 μF, C_2 = 0.15 μF, C_3 = 0.68 μF

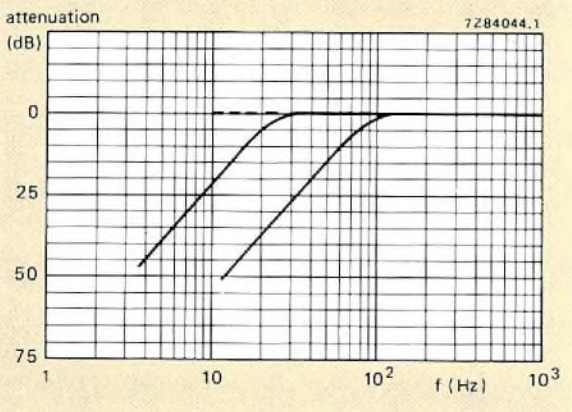


Fig.7 Response curves for the filters in Fig.8

Half of the TDA1028 as a rumble or subsonic filter

Figure 6 shows one half of the TDA1028 connected as a third-order (18 dB/octave) active high-pass filter with Butterworth response and component values chosen according to the method proposed by Fjällbrant (Ref.). The circuit can be constructed with component values chosen to achieve a cut-off frequency of 70 Hz to prevent the reproduction of turntable rumble. Alternatively, component values can be selected to achieve a cut-off frequency of 20 Hz to prevent large excursions of the low-frequency loudspeaker cone due to the reproduction of subsonic signals.

The filter response curve has a slope of nearly 18 dB/octave below 70 Hz or 20 Hz as shown in Fig.7. When the filter is fed from a 400 Ω source (TDA1029 output), the noise voltage over the frequency range 20 Hz to 20 KHz is 5.3 μV r.m.s. Under the same conditions, the stereo channel separation is 100 dB at 1 kHz, 86 dB at 10 kHz, 83 dB at 15 kHz and 80 dB at 20 kHz.

If the circuit is used in conjunction with a TDA1029 source selector the bias voltage divider can be omitted and the bias voltage obtained from pin 10 of the TDA1029.

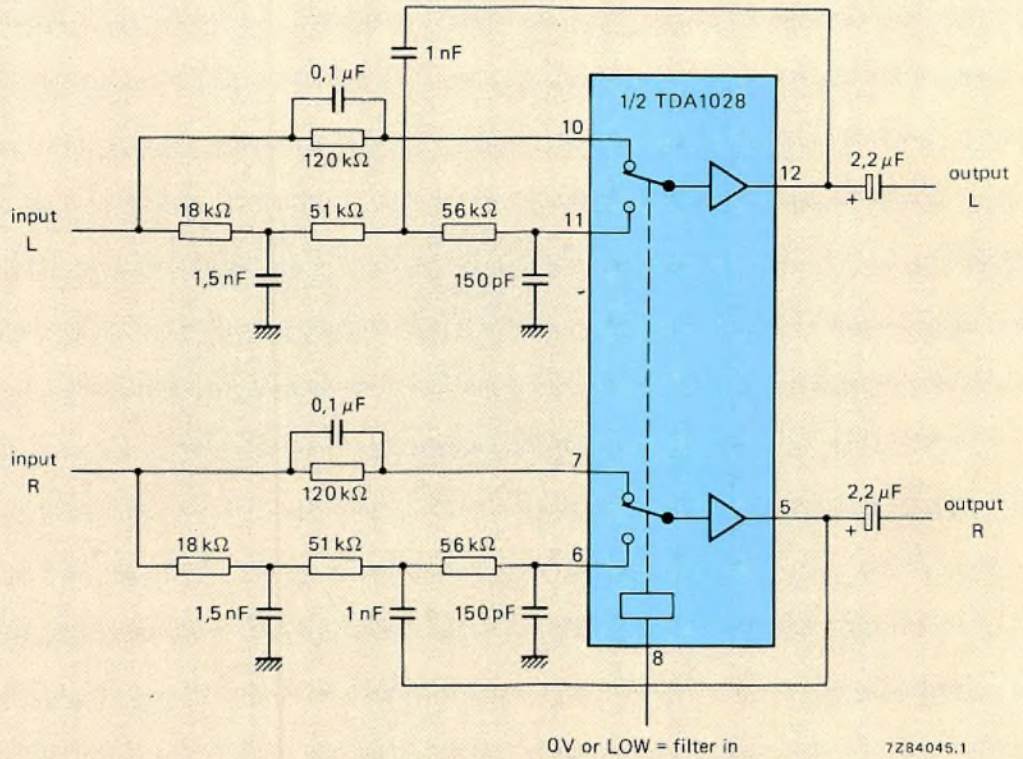


Fig.8 Half of the TDA1028 as a stereo low-pass (scratch) filter

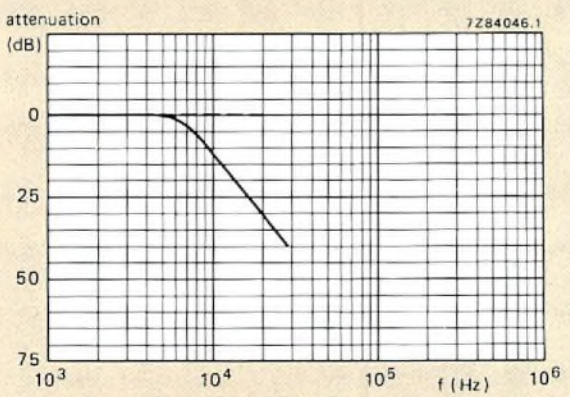


Fig.9 Scratch filter response curve

Half of the TDA1028 as a scratch filter

Figure 8 shows one half of the TDA1028 connected as a scratch filter designed on the same principles as the previous circuit. The filter has a cut-off frequency of 6.8 kHz to prevent the reproduction of spurious noise such as that caused by tape hiss or scratched records. If this circuit is direct-coupled to the output of the circuit in Fig.3a, Fig.4 or Fig.6, additional input biasing is not necessary. If the circuit is used alone however, a bias voltage of about 11 V must be derived from a potential divider network connected across the 20 V supply as shown in Fig.6. The total resistance in the input paths has been made to be about the same (≈120 kΩ) for both switch positions. This results in constant bias current and constant d.c. voltages at the inputs so that switching transients are minimised.

Figure 9 shows that the filter response curve has a slope of about 14 dB/octave from 7 kHz to the upper limit of the audible frequency range. When the filter is fed from a 400 Ω source (TDA1029 output), the noise voltage over the frequency range of 20 Hz to 20 kHz is 12 μV r.m.s. Under the same conditions, the stereo channel separation is 97 dB at 1 kHz, 86 dB at 10 kHz, 80 dB at 15 kHz and 78 dB at 20 kHz.

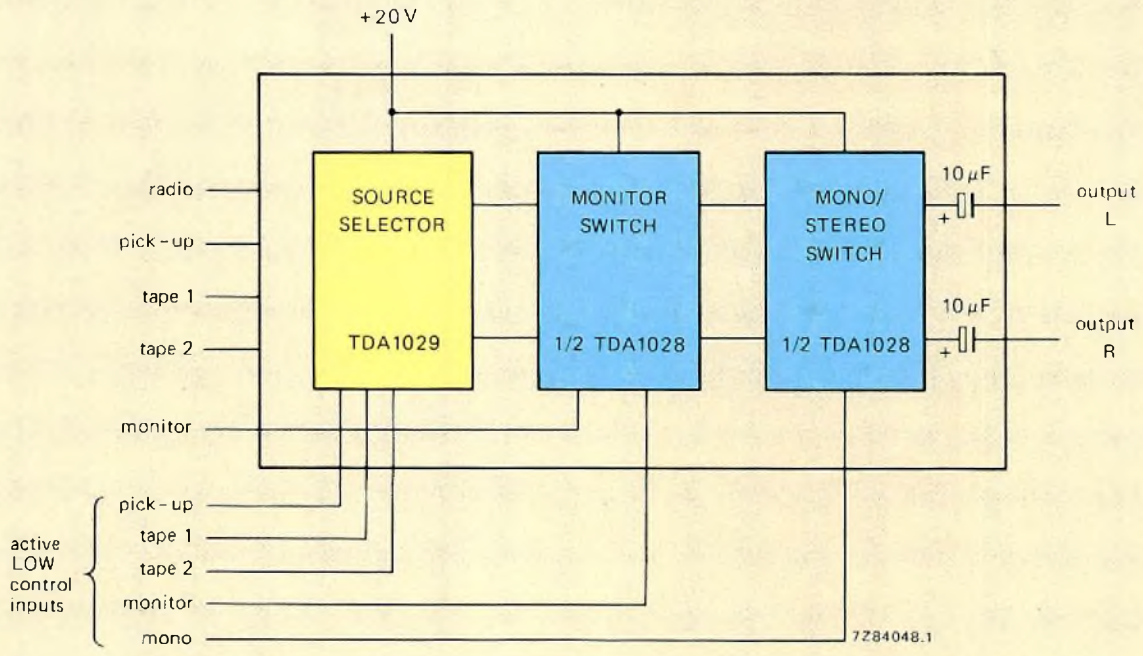


Fig.10 Interconnection of the application circuit to form the preamplifier shown on page 23

Combination of the application circuits to form a complete audio preamplifier

The source selector circuits can be interconnected with one or more of the TDA1028 application circuits to form a wide variety of audio preamplifiers. An evaluation model of such a combination has been constructed as shown on page 23. This circuit is interconnected as shown in Fig.10. It should be noted that the screening plates mounted between the input circuits to the TDA1029 and between the record/replay tape inputs are necessary to maintain the high level of stereo channel separation and crosstalk attenuation that can be achieved with the TDA1028 and TDA1029.

The crosstalk attenuation between any selected and non-selected input with source resistances from 4.7 kΩ to 47 kΩ in parallel with 250 pF is at least 80 dB at 1 kHz and at least 60 dB at 10 kHz. The stereo channel separation when using a 1 kHz radio input from a source with a resistance of 4.7 kΩ in parallel with 250 pF and a load resistance of 4.7 kΩ is 86 dB. If the source resistance is increased to 47 kΩ and the input signal is injected into the monitor input, the stereo channel separation is 65 dB at 1 kHz and 41 dB at 20 kHz. With input voltages from 1 V r.m.s. to 5 V r.m.s., the distortion is less than 0.02% at 1 kHz and less than 0.07% at 20 kHz. The unweighted noise voltage measured at the output of the circuit is 5.5 µV to 7 µV with source resistances in the range 4.7 kΩ to 47 kΩ.

REFERENCE

Fjällbrant, T., 'Canonical active RC filters with low sensitivity of the transfer function', Ericson Technics 2 (1967) page 211.

The YK1220 (15 kW) right, and YK1230 (25 kW) second from right, are the first of a new generation of compact, high-efficiency, wideband klystrons. Shown for comparison are the YK1195 (55 kW) left, a precursor of new technology, and the conventional YK1151 (20 kW).

An important feature of the new klystrons is that each can cover the full u.h.f. TV band from 470 MHz to 860 MHz; normally, three would be required, each covering only part of the band. Typical efficiency is 45%, compared with less than 35% for previous types. Because the focusing coils are mounted between the cavities instead of around them, one of the new types occupies a floor space only some 50 centimetres square instead of about one metre in diameter as before. Cooling can be by water, vapour, or vapour condensation. High-stability dispenser type cathodes are used and an integral ion-getter pump prolongs life by removing ions that penetrate the vacuum; such penetration increases with time and is the principal wear-out factor. An additional advantage of the pump is that it permits monitoring of the ratio of ion penetration so that the end of useful life can be predicted well ahead. The minimum life expectancy of the new klystrons is 30 000 hours.

On the basis of extensive technical and financial evaluation, the Independent Broadcasting Authority has specified the YK1220 and YK1230 for use in 47 new transmitters to be built for Britain's fourth TV channel. Mullard Ltd. is to supply them and Pye TVT, another U.K. Philips Company, is to build 23 of the transmitters.

Application note

A new approach to a PCM codec for telephony

Some recently developed monolithic analogue-to-digital and digital-to-analogue converters (ADCs and DACs) work with sufficient accuracy and speed for coding and decoding speech signals. It has therefore become common practice for pulse-code-modulated (PCM) telephony systems to incorporate a coder/decoder (CODEC) in each voice channel, as shown in Fig.1, instead of using a shared CODEC for multiplexed signals. It would obviously be advantageous if the analogue filters could be included in the integrated circuit. Since they require close tolerances, however, integrating their components with sufficient accuracy would complicate the IC process. We have therefore taken a different approach and developed an integrated CODEC in which the frequency response of the voice channel is limited by on-chip digital filters.

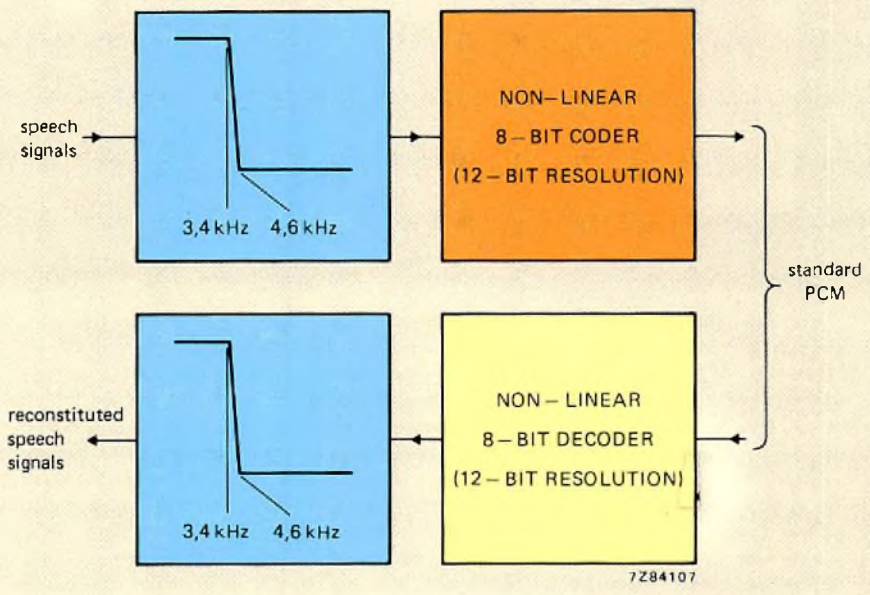


Fig.1 Conventional CODEC

This note is based on a laboratory report. Requests for additional data should mention the title of the note, the issue of E.C.&A. in which it appeared, and the nature of the applicant's interest.

THE CONVENTIONAL CODEC

Coding

An analogue signal limited to a bandwidth f can be completely defined by amplitude samples taken at intervals of not more than 1/2f seconds. In telephony PCM systems, the voice signals are sampled 8000 times per second. A vital part of a telephony CODEC is therefore an input filter which restricts the high-frequency response of the system to 4 kHz. The filter must meet the requirements of the CCITT with regard to small pass-band ripple and sharp cut-off.

After band-limiting and sampling, each sample is quantised according to an approximately logarithmic compression law and converted into an 8-bit binary code. The quantum level of each sample is usually measured by successive approximation using weighted current-sources or a ladder network of resistors. When integrating a CODEC, obtaining sufficient accuracy for the quantum steps necessitates control of additional parameters of the IC process. This also makes the coder more expensive to integrate than a purely digital circuit.

Decoding

In the receiving equipment, the 8-bit PCM words are applied to the input of a DAC which generates output pulses with amplitudes equal to the quantised values of the samples of the original voice signal. Since this is achieved in a similar manner to that used for quantising the samples in the coder, the same tight control of the IC process is required. The out-of-band components of the reconstituted analogue signal are removed by a sharp cut-off analogue filter similar to the one used in the coder.

A NEW APPROACH

The two main obstacles to integration of a PCM CODEC for telephony applications are:

- the required accuracy for the parameters of the analogue filters
- the additional process control required for integrating the current-sources or ladder network of resistors which define the quantising levels in the coder and decoder.

Figure 2 shows a new approach to CODEC design that eliminates both these obstacles.

The coder uses uniform sigma-delta modulation in which the number of quantising levels is reduced to two. A sampling rate of 256 kHz is necessary to achieve the required ratio of signal to in-band quantising distortion. A single RC filter at the analogue input is then sufficient to suppress spurious signals above 256 kHz minus the upper frequency of the speech band (256 kHz – 3.4 kHz = 252.6 kHz). The speech signal, now coded into one bit per sample, is limited to 3.4 kHz by a digital filter before it is converted into standard 8 kHz, 8-bit per sample PCM signal.

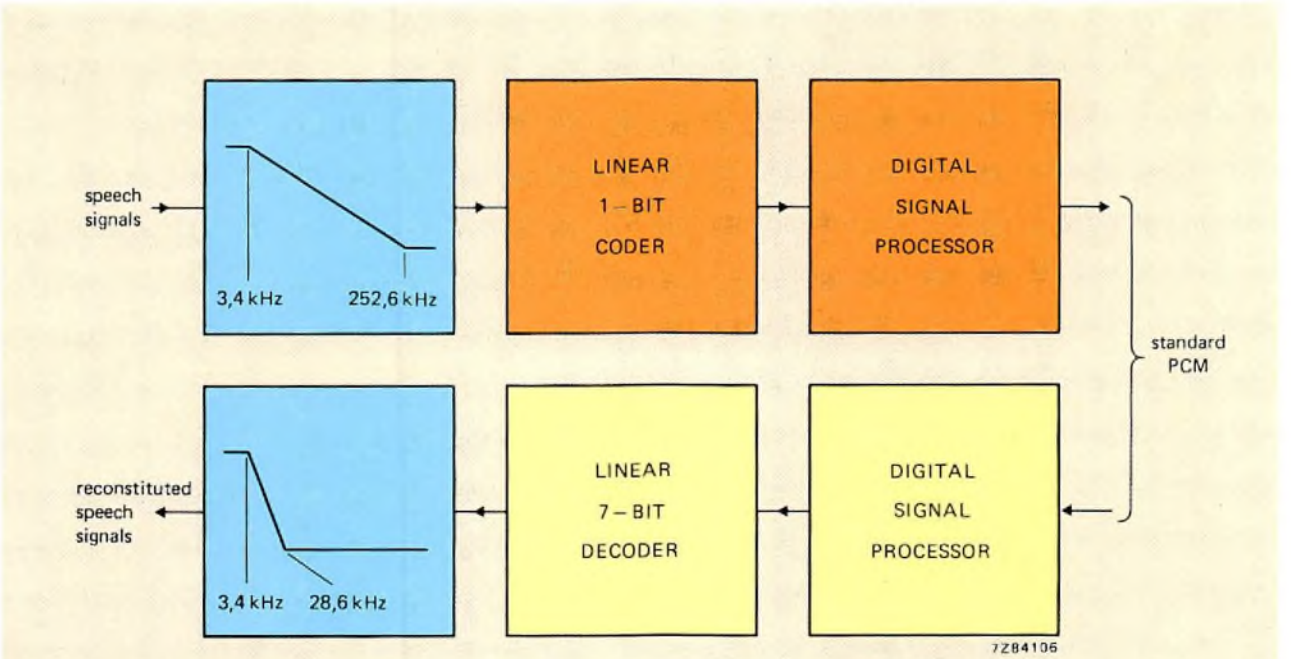


Fig.2 New approach to CODEC design. The analogue filters are much simplified by implementing A to D conversion before limiting the bandwidth of the speech signals to 4 kHz

A similar technique is used in the decoder. The 8 kHz PCM signal is passed through a sharp cut-off 3.4 kHz digital low-pass filter which converts the sampling rate to 32 kHz and suppresses all the spectrum lobes except those occurring at multiples of 32 kHz. The 32 kHz PCM signal is then passed to a digital 7-bit sigma-delta modulator which operates at a sampling rate of 512 kHz and is followed by a low-resolution (7-bit) DAC. A simple second-order analogue filter suppresses the remaining spurious signals above 32 kHz minus the upper frequency of the speech band.

The main advantages of this approach can be summarised as follows:

- Precision analogue functions have been eliminated by introducing digital signal processing.
- The digital filters are insensitive to temperature, ageing and variations of the IC process.
- The low-resolution ADCs and DACs do not impose precision requirements on the IC process.

The new CODEC is being manufactured as two ICs. A logical future step will be to integrate it, together with the present peripheral components, onto a single chip. A more detailed description will be published in a later issue of Electronic Components & Applications.

TDA1060 - a comprehensive integrated control circuit for SMPS

H. HOUKES

A switched-mode power supply (SMPS) converts an alternating voltage into a stabilised d.c. voltage. To achieve this, the input voltage is rectified and periodically connected to the load by a switching transistor, output transformer and filter acting as a d.c.-to-d.c. converter. A comparator monitors the output and increases the duty factor of the switching cycle if the load voltage is too low, and decreases the duty factor if the load voltage is too high. Unlike a conventional series regulator, the SMPS does not incorporate a power-dissipating series control element and is therefore much more efficient. Since the switching can be effected at ultrasonic frequency, the size and weight of SMPS circuit components, and the losses they introduce, can be minimised. However, although the SMPS is lightweight, compact, and efficient, it must incorporate a complex control circuit capable of performing the following functions:

- generation of drive pulses for the SMPS switching transistor,
- control of the duty factor (pulse duration) of the drive pulses to counteract load variations,
- provision of a stable temperature-compensated reference voltage for comparison with a sample of the output voltage,
- amplification of the error voltage by a circuit with adjustable gain and means of applying frequency compensation (phase shift) to ensure control loop stability.

In addition to performing these control functions, the circuit must also protect the supply from hazardous operating conditions by providing:

- presetting of the maximum attainable value for the duty factor of the SMPS switching,
- a slow-start facility to limit the amplitude of the inrush current which passes through the SMPS switching transistor when the supply is switched on,
- overload and overvoltage protection,
- protection if the supply voltage to the control circuit is too low,
- protection in the event of a fault in the feedback circuit,
- protection if the core of the output transformer becomes saturated.

It may also be desirable for the control circuit to incorporate:

- a feedforward facility to compensate for input voltage variations,
- logic-compatible remote on/off switching,
- external synchronisation of the SMPS switching.

There are many types of d.c.-to-d.c. converter suitable for SMPS circuits: flyback (ringing choke), forward (feed-through) using one or two switching transistors, and push-pull using up to four switching transistors. We have already introduced integrated control circuits for consumer SMPS applications such as television receivers. This article describes the comprehensive integrated SMPS control circuit TDA1060 for controlling industrial SMPS circuits using flyback or forward converters. The TDA1060 is second-sourced by Signetics under the type number NE/SE5560.

BASIC SMPS CONTROL LOOP

The basic control loop for a fixed-frequency pulse-duration regulated SMPS is shown in Fig.1. The output voltage V_O is sensed via a feedback network and compared with a reference voltage V_{ref}. Any difference between V_O and V_{ref} is amplified and fed to a pulse-width modulator (PWM), where it is compared with the instantaneous level of a ramp waveform (sawtooth or triangular) from oscillator. The output from the PWM is a rectangular waveform synchronised with the oscillator waveform; its duty factor δ depends on the difference between V_O and V_{ref}. This signal drives the base of the SMPS power switching transistor so that its conduction period, and hence the amount of energy transferred from the input to the output of the SMPS, is controlled to maintain a constant output voltage.

As shown in Fig.1, protection circuits can be added to influence the duty factor via an additional PWM input at P1, or at P2 via a gate at the PWM output. The SMPS output can be inhibited by a protection circuit connected directly to the base of the switching transistor at P3.

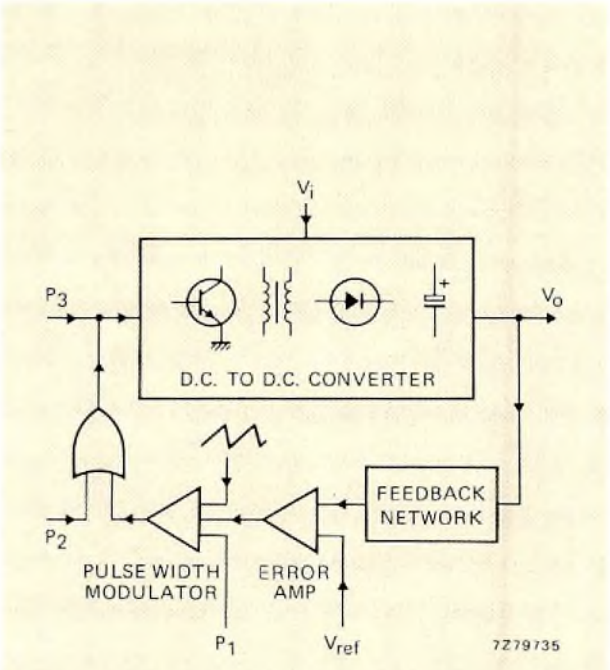


Fig.1 Basic SMPS control loop

INTEGRATED SMPS CONTROL CIRCUIT TDA1060

The circuit elements in the feedback path of the SMPS control loop are integrated in the SMPS control circuit TDA1060, a block diagram of which is given in Fig.2. In addition to providing drive pulses with a duration proportional to the output voltage from the SMPS, the TDA1060 incorporates the following features:

- Voltage/current regulator which supplies the internal circuitry and inhibits the output drive pulses in the event of the supply voltage to the IC being too low. The stabilised voltage is also available externally. (Pins 1, 2, 12)
- A temperature-compensated reference voltage source based on the band-gap energy of silicon.
- Fail-safe control loop. If the feedback path becomes open-circuit, the duty factor of the output pulses is reduced to zero. If the feedback path becomes short-circuit, the duty factor of the output pulses is reduced to an externally-set value δ_O. (Pins 3, 4)
- Externally adjustable switching frequency, up to 100 kHz. The switching can be synchronised with an external *lower* frequency applied to a TTL-compatible input. (Pins 7, 8, 9)
- Pre-regulation (feedforward) to compensate for variations of the d.c. input to the converter, thereby allowing use of a minimum size output transformer and easing the task of the main control loop. (Pin 16)
- Direct access to the input of the pulse-width modulator, allowing use of a separate control loop, for example, in constant-current operation. (Pin 5)
- Accurate setting of the maximum obtainable duty factor for the SMPS drive pulses to prevent saturation of the output transformer core in mains-isolated power supplies using a forward converter. (Pin 6)
- Initiation of the duty factor reduction/fast switch-off/slow-start sequence in the event of excess current being drawn from the SMPS. (Pin 11)
- Remote on-off switching with slow-start to reduce the inrush current that passes through the switching transistor. (Pin 10)
- Drive pulses derived from a bistable circuit to prevent double pulsing.
- Immediate inhibiting of the output drive pulses in the event of excess output voltage from the SMPS or saturation of the core of the output transformer. (Pin 13)

Each of these functions will be described in further detail in the following paragraphs.

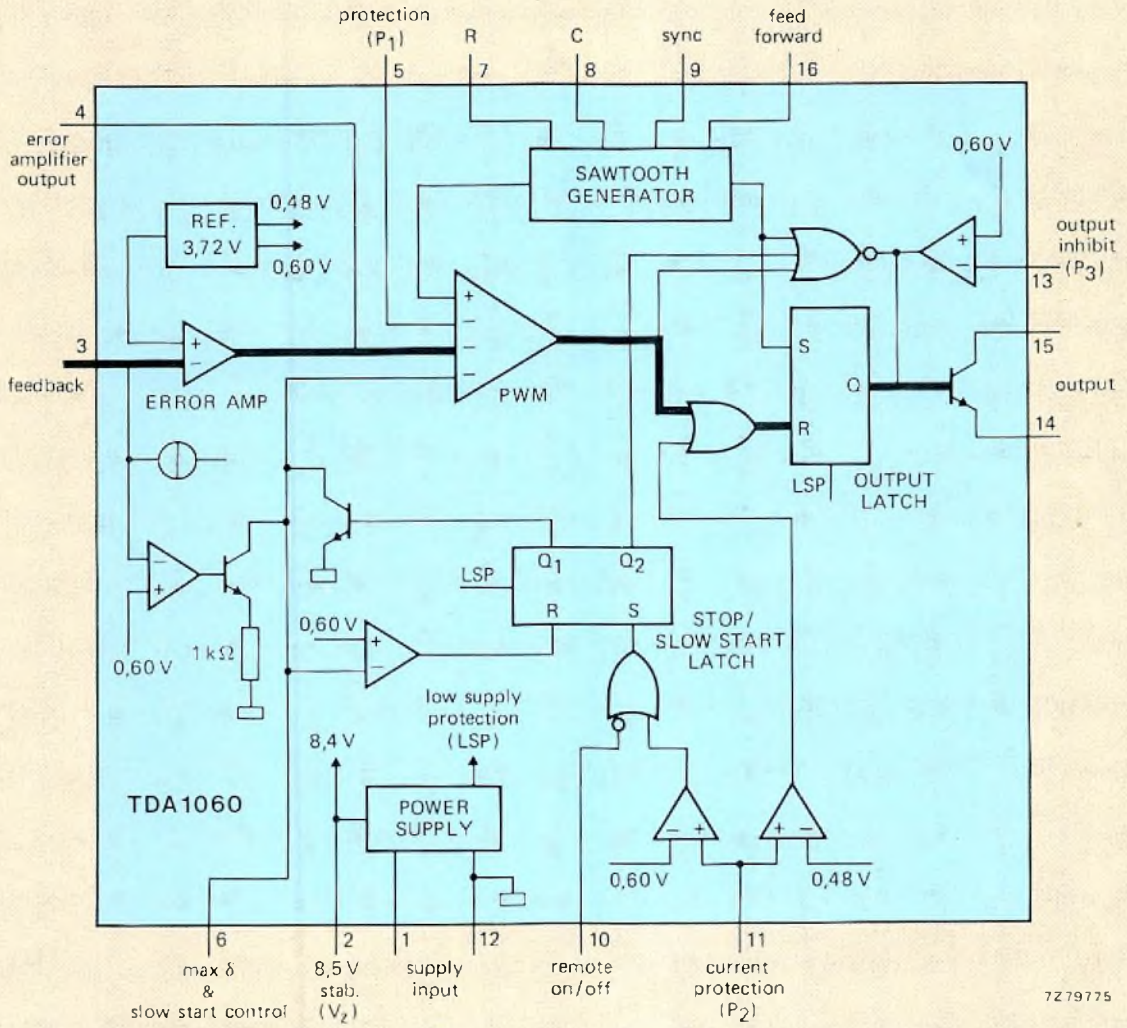
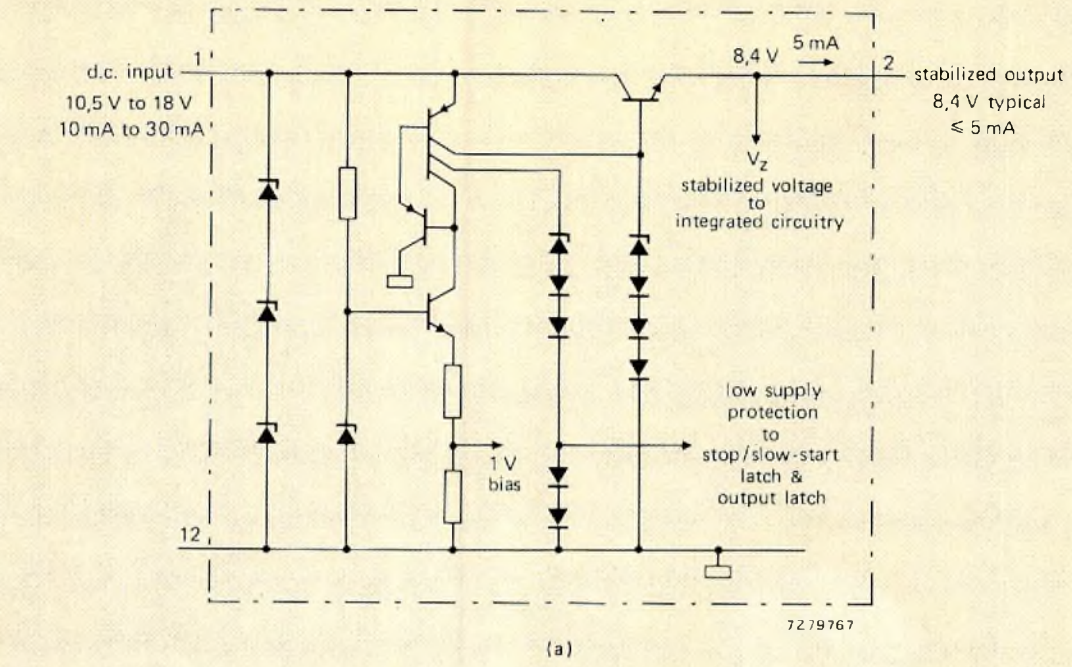


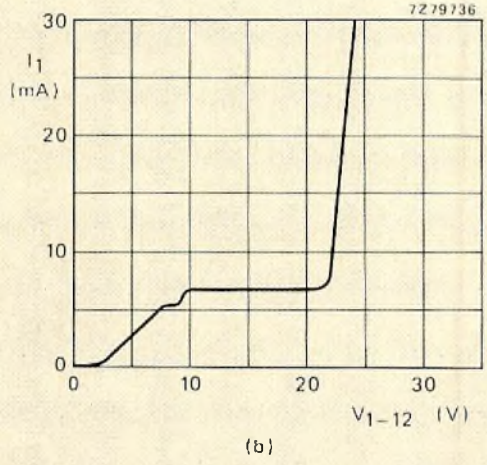
Fig.2 Block diagram of the TDA1060

Power supply

The TDA1060 incorporates a series regulator to provide a stabilised 8.4 V supply for its internal circuits. A schematic diagram of the circuit is given in Fig.3a. Pin 1 can be connected either to a current source (for example, via a series resistor to the d.c. input to the SMPS converter), or to a voltage source (for example, a battery). A current source must feed between 10 and 30 mA into pin 1; three internal zener diodes limit the voltage developed at pin 1 to between 20 and 30 V, as shown by the typical input characteristic given in Fig.3b. A voltage source must provide between 10.5 and 18 V at pin 1. The current consumption from a 12 V source is less than 10 mA as long as pin 2 is not connected and the value of



(a)



(b)

Fig.3 Power supply.
(a) Schematic diagram;
(b) Typical input characteristic showing voltage at pin 1 as a function of input current

the frequency-determining resistor connected between pins 7 and 12 (see Fig.2) is not less than 20 kΩ. If the voltage at pin 1 falls below 9.5 V, that is ($V_Z + 4\,V_{BE}$), the low-supply protection (LSP) level drops and inhibits the output latch and stop/slow-start latch, as shown in Fig.2.

The stabilised output voltage V_Z from the series regulator (typically 8.4 V) supplies the remainder of the integrated circuitry and is also available at pin 2 for external use (for example, for precise setting of the maximum duty factor of the SMPS drive pulses, as explained later). Up to 5 mA can be drawn from pin 2.

Reference voltage

To ensure that the output voltage from the SMPS is accurately controlled under all conditions, the reference voltage with which the output voltage sample is compared must remain very stable for long periods and be largely independent of temperature variations. In the TDA1060, the reference voltage has a typical value of 3.72 V, based on the band-gap energy of silicon. This results in a long-term stability of 2 mV/1000 hours and a temperature coefficient of ±0.01%/°C. The reference voltage is connected to the non-inverting input of the error amplifier, as shown in Fig.2.

Control loop error amplifier

The error amplifier shown in Fig.4 is an operational amplifier with an open-loop gain A_O of 60 dB. The reference voltage is connected to its non-inverting input. The output from the SMPS (V_O) is connected, via a potential divider and resistor R_3, to the inverting input. The closed-loop gain A_f of the amplifier is set by applying feedback to the inverting input via resistor R_f. The closed-loop gain can be expressed as:

$$A_f = \frac{A_O}{1 + \beta A_O}$$

in which β is the feedback fraction given by:

$$\beta = \frac{R_3}{R_f}$$

The effect of error amplifier gain on control loop sensitivity is shown in Fig.5.

The error amplifier must be externally frequency-compensated by limiting its high-frequency response with a capacitor connected between the output (pin 4) and the common rail. A value of 22 nF will cause the frequency response to roll-off at 20 dB/frequency decade above 600 Hz, as shown in Fig.6. Phase shift networks may be inserted into the feedback path to ensure stability of the control loop.

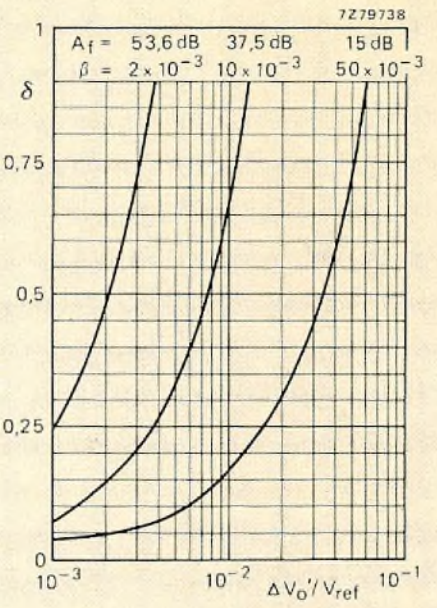


Fig.5 Output pulse duty factor as a function of feedback voltage change with error amplifier gain as a parameter. With a reference voltage of 3.72 V, the horizontal axis represents feedback voltages of 3.72 mV to 223 mV

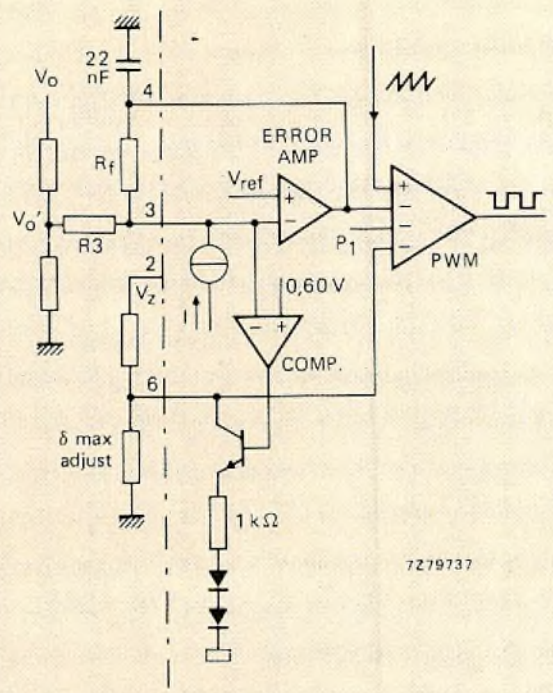


Fig.4 Error amplifier and loop fault protection

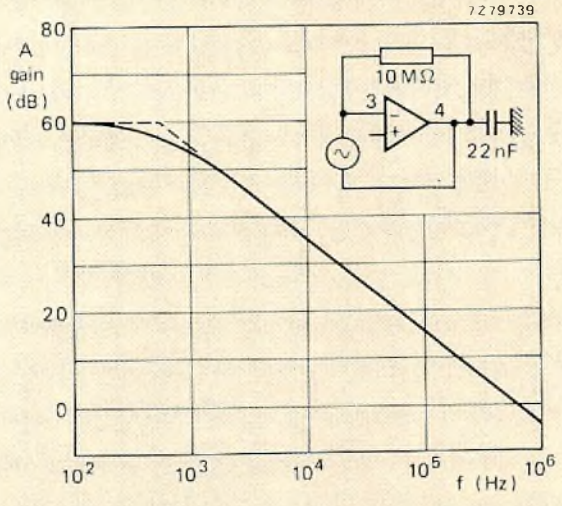


Fig.6 Frequency response of compensated error amplifier

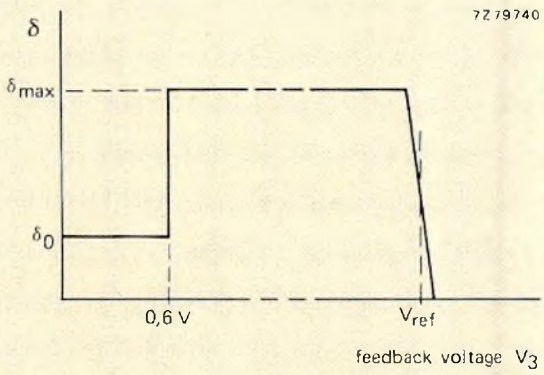


Fig.7 Limitation of maximum value of duty factor in the event of a short-circuit in the feedback path

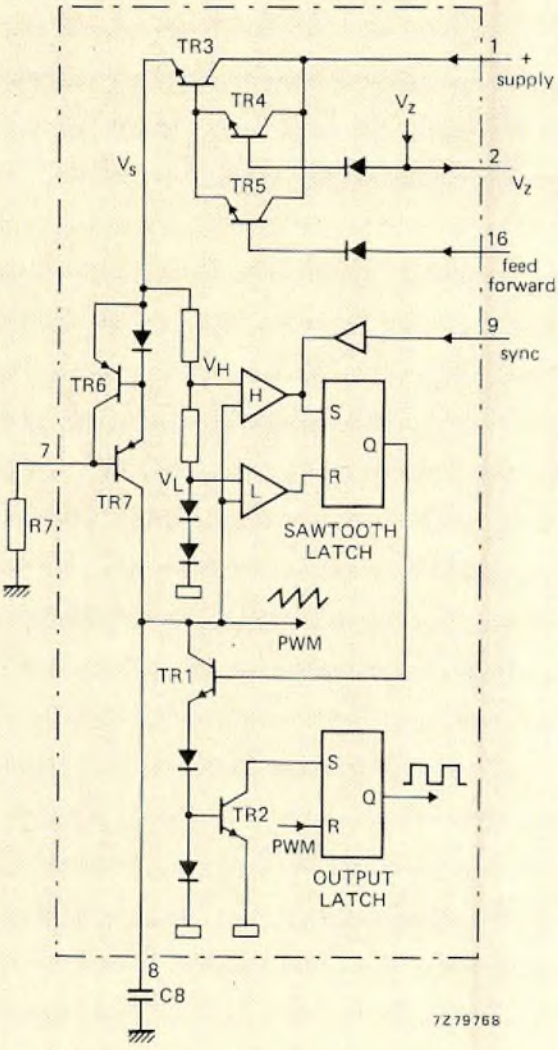


Fig.8 Sawtooth generator

Loop fault protection

The TDA1060 provides protection for the SMPS in the event of the feedback path becoming open-circuit or shorted to the common rail.

Figure 4 shows that, in the open-circuit case, pin 3 would be floating and the error amplifier output would therefore settle at the reference voltage, causing a large duty factor and a consequent high output from the SMPS. This is prevented by an internal current source which produces a large potential difference across R_3 (pin 3 positive) and thereby forces the voltage at the error amplifier output to fall. If the value of R_3 is greater than 470 kΩ, the voltage at the error amplifier output (inverting input to the PWM) falls below the level of the sawtooth waveform at the PWM input and the duty factor of the SMPS drive pulses is reduced to zero.

In the short-circuit case pin 3 is pulled down to 0 V, which would normally cause a high output from the error amplifier and consequently demand the preset maximum duty factor for the SMPS drive pulses. However, if the voltage at pin 3 falls below 0.6 V, a comparator in the IC causes an internal transistor to switch a 1 kΩ resistor in parallel with the external resistor which sets the maximum attainable duty factor. The duty factor is therefore reduced to a limited maximum (δ_0) as shown in Fig.7. The actual value of δ_0 is determined by the value of external resistors as will be described later. The two diodes in series with the internal 1 kΩ resistor simulate the lower level of the sawtooth input to the PWM.

Sawtooth generator

The sawtooth generator shown in Fig.8 provides a ramp waveform for comparison with the error amplifier output in the PWM. The frequency of the sawtooth, and therefore the switching frequency of the SMPS, is a function of the time-constant formed by the external resistor connected to pin 7 and the external capacitor connected to pin 8. The generator can be either free-running or synchronised with a signal applied to pin 9.

Timing capacitor C_8 charges from the positive supply rail via control transistors TR_3 and TR_7, the charging current being controlled by R_7 and TR_6. The ultimate amplitude, and therefore the slope of the increasing voltage across C_8, is determined by the level of V_S which, in turn, is determined by either stabilised voltage V_Z or by the feedforward voltage applied to pin 16. Voltage V_H (approximately 5.7 V without feedforward) is a function of V_S; voltage V_L is $2V_D \approx 1.3$ V. The waveforms associated with the generation of the sawtooth are given in Fig.9.

When the voltage on C_8 reaches V_H, the H-comparator sets the sawtooth latch which switches on TR_1 to discharge C_8. During the discharge (flyback) period, TR_2 conducts and sets the output latch. When the voltage

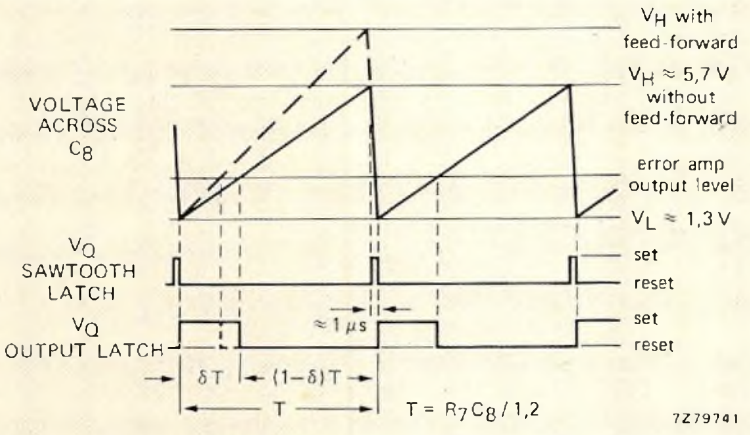


Fig.9 Sawtooth waveform generation

across C_8 has fallen to V_L, the L-comparator resets the sawtooth latch which switches off TR_1. The cycle then repeats. The operating frequency of the sawtooth generator (100 kHz max) is given by: $f \approx 1.2/R_7C_8$ Hz.

Synchronisation

The sawtooth frequency can be synchronised with an external *lower*-frequency signal applied to the TTL-compatible input at pin 9. Figure 11 illustates the synchronisation action. When the level of the synchronising signal is LOW (below 0.8 V), the sawtooth latch cannot be set when the voltage across C_8 has risen to V_H. The capacitor therefore continues to charge toward V_S until the synchronising signal goes HIGH (above 2 V). The SET input of the sawtooth latch is then no longer disabled and a transition occurs at the latch output, thereby switching on TR_1 and discharging C_8. The cycle then continues as previously described. The falling edges of the sawtooth waveform are thus delayed and synchronised with the LOW-to-HIGH transitions of the signal applied to pin 9. If pin 9 is not used, it is advisable to connect it to V_Z at pin 2.

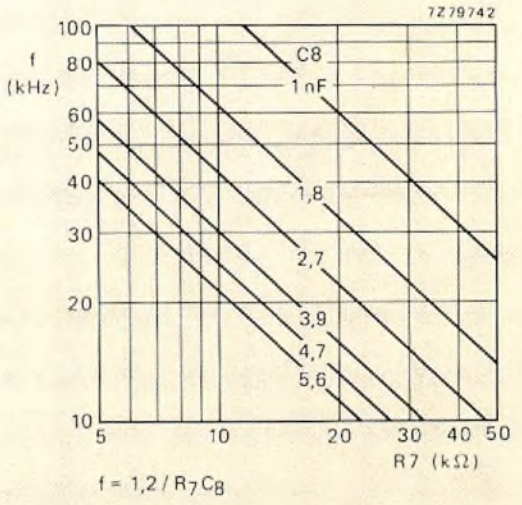


Fig.10 Sawtooth generator frequency as a function of the values of R_7 and C_8

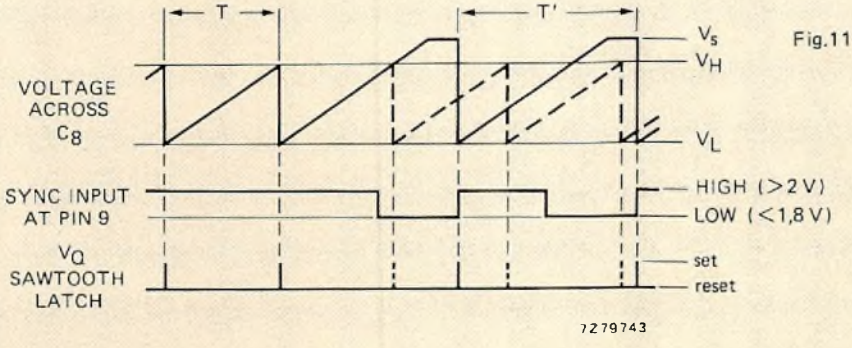


Fig.11 Synchronisation of sawtooth generator

1/T = free-running frequency
1/T' = synchronized frequency

Pre-regulation (feedforward)

In cases where the input voltage V_i to the SMPS is subject to variation, it is beneficial to use a separate control loop to adjust the duty factor (δ) of the SMPS drive pulses to compensate for the input voltage variations. This pre-regulation or feedforward control can considerably ease the requirements for the main control loop which then only has to compensate for SMPS load variations.

For a forward converter operating in the continuous current mode, the output voltage is given by:

$$V_O = \frac{\delta V_i}{n}$$

where n is the turns ratio of the output transformer.

If the duty factor is varied inversely to the change of input voltage so that $\Delta\delta \propto 1/\Delta V_i$, input voltage variations will be compensated.

To cater for a maximum load transient occurring coincident with maximum input voltage, the turns ratio for the SMPS output transformer is calculated from:

$$n = \frac{\delta_{max}\, V_{i\,max}}{V_O}$$

If the $\Delta\delta \propto 1/\Delta V_i$ compensation is also applied to the δ_{max} setting, the turns ratio, and therefore the cost and bulk of the output transformer, can be considerably decreased at the expense of slightly slower response to load transients.

In the PWM, the output level from the error amplifier is compared with the level of the ramp from the sawtooth generator. The duty factor of the output pulses from the PWM (SMPS drive pulses) is proportional to the time taken for the sawtooth voltage to reach the level of the error amplifier output. The duty factor of the PWM output pulses can therefore be reduced by increasing the slope of the sawtooth waveform. This is shown in Fig.12. The illustration also shows that the maximum obtainable duty factor is proportional to the time taken for the sawtooth voltage to reach the level of the δ_{max} control voltage at pin 6. The maximum obtainable duty factor is therefore also decreased if the slope of the sawtooth waveform is increased.

Referring again to Fig.8, it can be seen that, if a voltage proportional to the SMPS input voltage V_i and greater than V_Z is applied to pin 16, the action of supply control transistors TR_3 and TR_5 will cause V_S and V_H to vary with V_i variations. An increase of V_i will increase V_S, thereby increasing the charging current of C_8 and steepening the slope of the generated sawtooth. Figure 9 shows that, since V_H has also increased, the increased slope of the sawtooth has very little effect on the sawtooth period. In the PWM, the sawtooth waveform will now reach the level of the error amplifier output earlier than before. The duty factor of the PWM output pulses will therefore be reduced to compensate changes of SMPS input voltage. The transfer function of the feedforward circuit is given in Fig.13. This graph shows that the feedforward function overcompensates δ for changes of V_i, thereby counteracting the extra damping of the duty factor caused by the storage time of the SMPS power switching transistor. The curve can be shifted closer to the ideal characteristic by connecting the lower end (point A) of the V_i feedforward potential divider to a portion of V_Z at point B, as shown in the inset of Fig.13. If pin 16 is not used, it must be connected to pin 12 (common return) or pin 2 (V_Z).

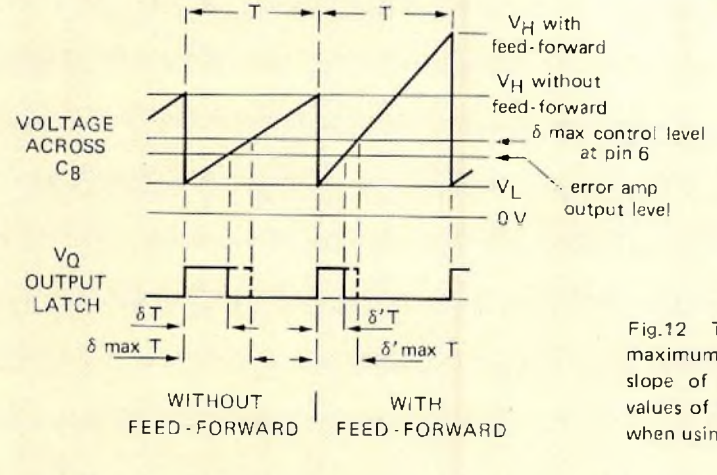


Fig.12 The duty factor for normal operation and the maximum obtainable duty factor are both reduced if the slope of sawtooth waveform is increased. The normal values of duty factor are δ and δ_{max}. The increased values when using feed-forward are δ' and δ'_{max}

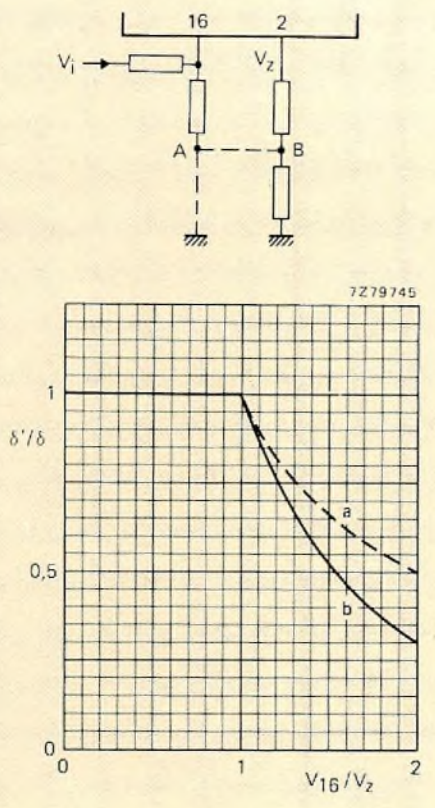


Fig.13 Transfer characteristic of the feed-forward circuit. Curve (a) is the ideal case with δ' proportional to V_i. Curve (b) is the measured result with the potential divider connected between V_i and ground

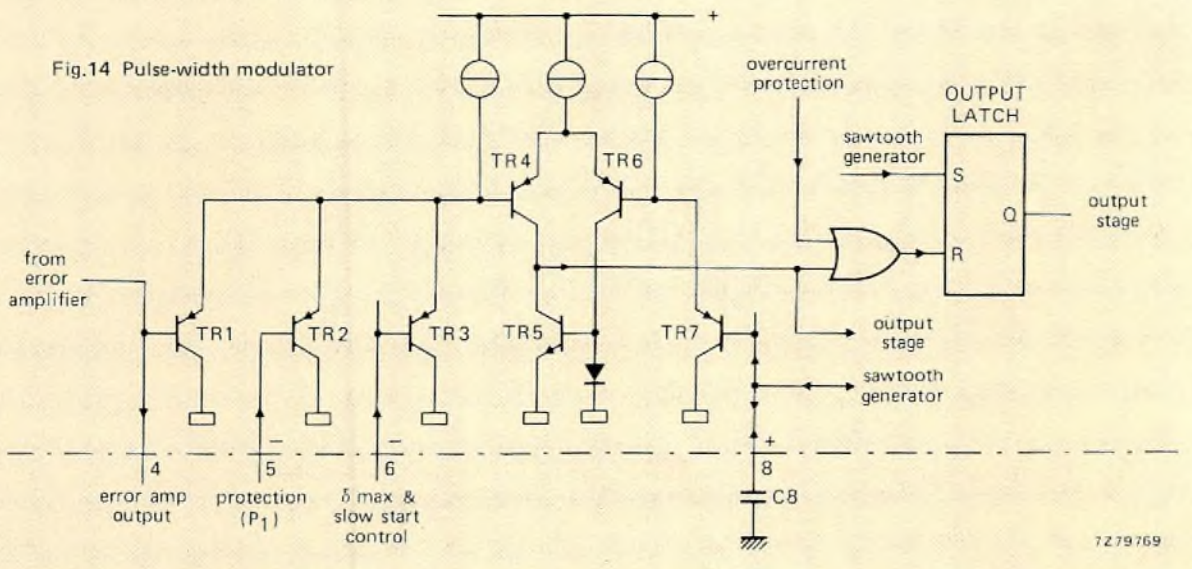
Pulse-width modulator

The pulse-width modulator (PWM) generates pulses with a duration (δT) proportional to the *lowest* of the levels at the three inverting inputs and with a frequency ($1/T$) equal to that of the sawtooth generator. The circuit of the PWM is given in Fig.14.

The sawtooth waveform across C_8 is compared with the *lowest* of the three voltages on pins 4, 5, and 6. During normal operation when the error amplifier output is lower thsn the voltages on pin 5 and pin 6, TR_5 and TR_6 conduct, the input to the OR gate is LOW, and the output latch will be set by the sawtooth generator during the flyback period of the sawtooth. When the sawtooth ramp at the base of TR_7 reaches the level of the error voltage at the base of TR_1, transistors TR_5 and TR_6 turn off and TR_4 conducts to put a HIGH level at the input of the OR gate, thereby resetting the output latch. The duration of the pulses at the Q terminal of the output latch, and therefore the duty factor of the SMPS drive pulses, is thus proportional to the error voltage. The duty factor of the pulses at the PWM output is plotted as a function of the voltage on pin 4, 5 or 6 in Fig.15.

The voltage at pin 6 of the PWM sets the maximum attainable duty factor and controls the slow-start circuit, as explained under the next two headings. An additional input is provided at pin 5. This input can be used to reduce the duty factor below the value resulting from the voltage applied to pin 4 or pin 6. This facility allows the use of a separate control loop with an external error amplifier and reference voltage (for example, constant-current control). If pin 5 is not used, it must be connected to pin 6 or to pin 2 (V_Z).

Fig.14 Pulse-width modulator



Setting maximum duty factor δ_{max} and reduced maximum duty factor δ_o

The maximum duty factor attainable with the TDA1060 operating at a frequency of 50 kHz is about 0.95. A duty factor as large as this could cause problems in many applications. For example, in an isolated forward converter, the duty factor must not exceed 0.5 so that the core of the output transformer can completely demagnetise during the off-period of the power switching transistor. The TDA1060 therefore incorporates a facility for limiting the maximum attainable duty factor to a preset value.

As previously explained with the aid of Fig.14, the PWM is controlled by the *lowest* of the voltages applied to pins 4, 5, and 6 with the transfer function shown in Fig.15. The maximum duty factor that can be demanded by the error amplifier output at pin 4 can therefore be limited by applying a voltage to the δ_{max} setting input at pin 6. To ensure an accurate and stable δ_{max} setting, the voltage at pin 6 should be derived from a potential divider connected across the stabilised voltage V_Z at pin 2. The duty factor is inversely proportional to the slope of the sawtooth waveform, which is defined by V_H. Since V_H is also derived from V_Z, the δ_{max} setting is almost independent of V_Z tolerances. The maximum attainable duty factor is plotted as a function of the values of the potential divider resistors R_2 and R_6 in Fig.16.

The maximum duty factor is reduced to a value δ_o when the voltage at pin 3 drops below 0.6 V. Since δ_o is determined by an internal 1 kΩ resistor switched between pin 6 and the common rail, δ_o is also influenced by the values of the resistors in the potential divider

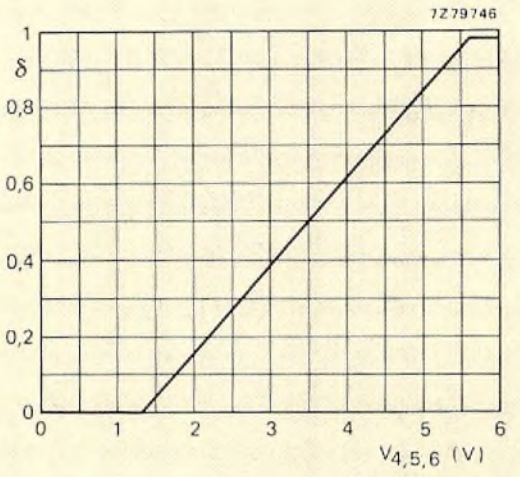
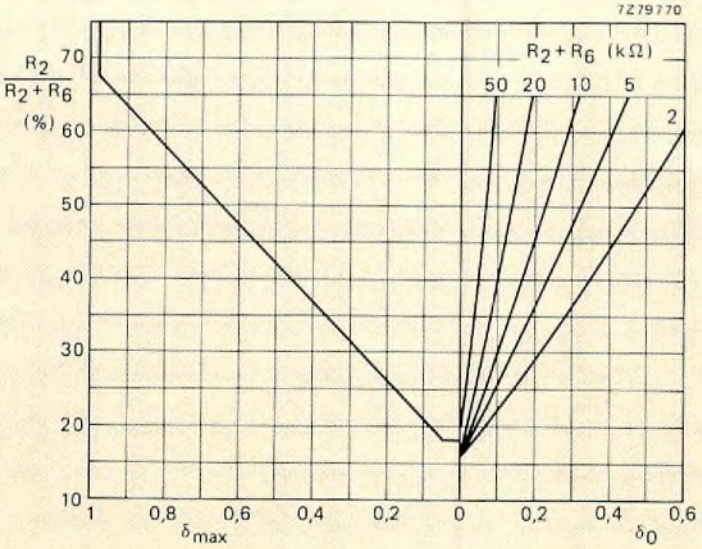


Fig.15 Transfer function of the pulse-width modulator



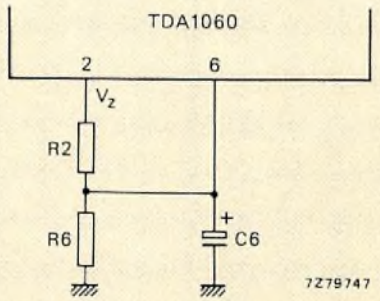


Fig.16 Maximum attainable duty factor and reduced maximum duty factor as functions of the values of the resistors in the potential divider connected between pins 2 and 6

connected to pin 6. The maximum duty factor and reduced maximum duty factor are plotted as functions of the potential divider resistor values in Fig.16. It should be noted that the spread of δ_O can be considerable because of the tolerance of the internal 1 kΩ resistor. The selected value of δ_O must be small enough to ensure that the energy in the SMPS is limited to a safe level in the event of a short-circuit in the feedback path. However, if δ_O is too small, the SMPS output voltage will be too low to allow the feedback voltage at pin 3 to rise above the short-circuit loop protection level (0.6 V) during start-up with maximum load and minimum input voltage. A practical value for δ_O is 0.1 to 0.2.

Overcurrent protection

The TDA1060 provides protection of the SMPS switching transistor if too much current is drawn from the output. The protection is progressive and is activated at two current levels. If the collector current increases to the first threshold, the duty factor is limited to provide a nearly constant peak current. If the current increases to the second threshold, the SMPS is switched off for a brief period (dead-time) and then restarted with a slowly increasing duty factor (slow-start).

The output current can be sensed directly, or a reasonable indication of it can be derived by sensing the collector or emitter current of the SMPS output transistor. The collector current can be sensed by connecting a resistor or current transformer in series with the output transistor. The voltage developed across the current sensor is connected to the TDA1060 current protection input at pin 11 as shown in Fig.17. The current turn-on spike must be damped by an RC network connected in parallel with the current sensing resistor.

If the voltage at pin 11 reaches threshold A (0.48 V), the output from comparator A overrides the PWM information and resets the output latch, thereby curtailing the on-period of the SMPS output transistor and thus limiting the duty factor. The effectiveness of this cycle-by-cycle current limiting diminishes at low duty factors because the storage time of the output transistor is then dominant in determining the duty factor. The collector current of the output transistor therefore increases again until the voltage at pin 11 reaches threshold B (0.6 V). Comparator B then activates the stop/slow-start circuit which immediately inhibits the output pulses from the TDA1060. After a brief deadtime, a slow-start is initiated by slowly increasing the duty factor.

Figure 18 shows the effect of the two-stage current limiting on the output V/I characteristic of a forward converter. In the event of a persistent short-circuit at the output of the SMPS, the duty factor limiting/switch-off/slow-start sequence will be repetitive, causing the SMPS output to 'hiccup'.

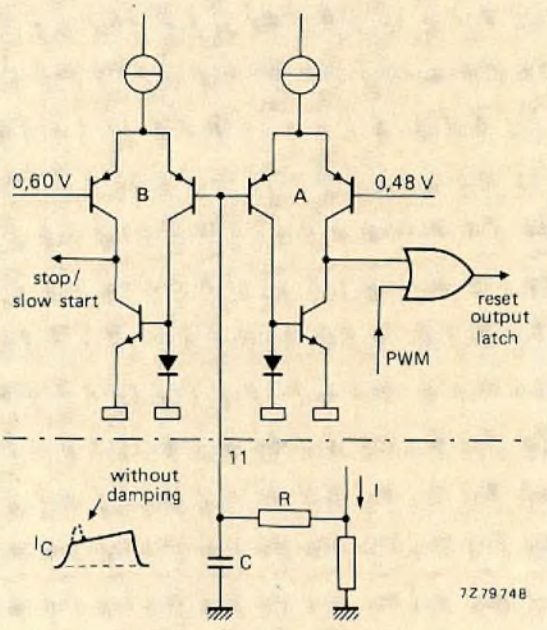


Fig.17 Over-current protection

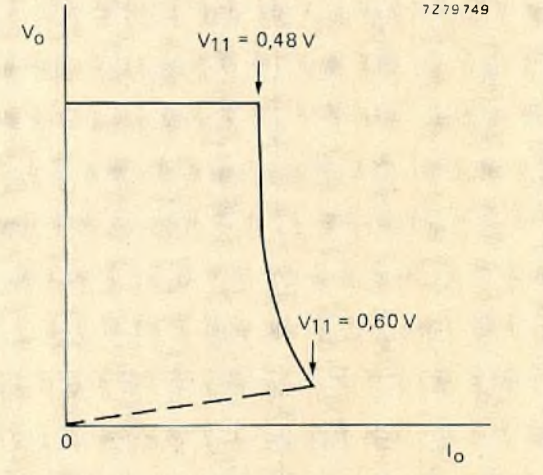


Fig.18 Output V/I characteristic during current limiting by the circuit of Fig.17

Stop/slow-start circuit

The stop/slow-start circuit provides an immediate stop followed by a dead-time and a slow-start during which the duty factor of the output pulses, and thus the output voltage of the SMPS, rises gradually to a steady-state value. This prevents inrush current which would pass through the SMPS switching transistor. The circuit is shown in Fig.19.

The circuit action is initiated by the stop/slow-start latch being set by the remote control or overcurrent input. Output Q_2 from the latch then inhibits the output pulses by enabling the OR gate and holding the output transistor base LOW. Output Q_1 causes TR_1 to conduct and thereby discharge external capacitor C_6 via an internal 50 Ω resistor. After time constant $50 \times C_6$ has allowed the voltage at pin 6 to fall to 0.6 V (the dead-time), a comparator resets the latch, removes the inhibit from the output transistor and switches off TR_1. Capacitor C_6 then starts to charge toward V_Z via R_2, and the slowly increasing potential at pin 6 causes the PWM to generate pulses with a duty factor which slowly increases to the steady-state value dictated by the *lowest* input to the PWM. The circuit action is illustrated by the waveforms in Fig.20.

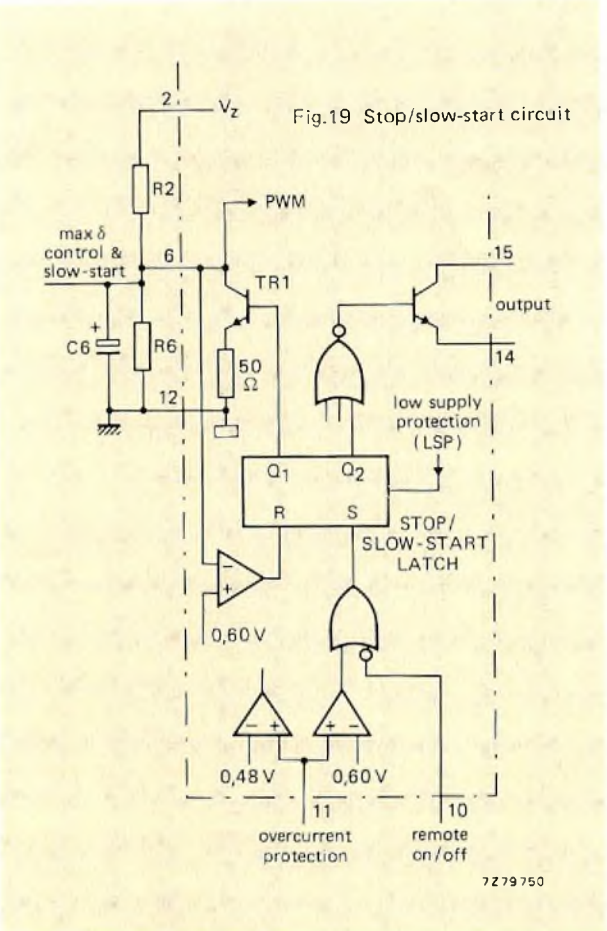


Fig.19 Stop/slow-start circuit

Normal switch-on and low-supply protection

A low-supply protection (LSP) facility provides a slow-start when the voltage at pin 1 rises above 9.5 V, as it will during normal switch-on.

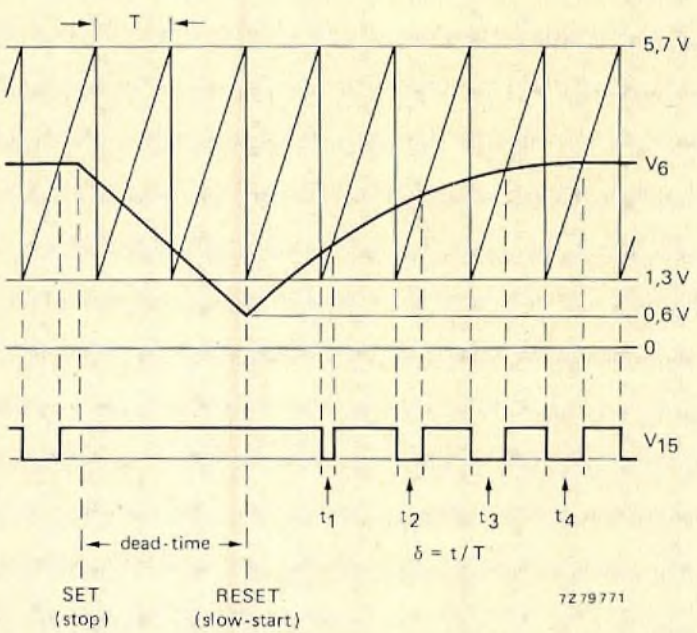


Fig.20 Waveforms associated with the stop/slow-start circuit

Remotely-controlled on/off switching

Figure 19 shows that the output pulses from the TDA1060 can be switched on and off by applying logic levels to the TTL-compatible input at pin 10. This facility allows on/off switching of the SMPS output by a remote control circuit, for example in the sequential start-up of a number of power supplies. A low level (<0.8 V) at pin 10 causes immediate inhibition of the output pulses from the TDA1060. A subsequent HIGH level (>2 V) at pin 10 switches on the circuit with a slow-start. If the remote control facility is not required, pin 10 should be connected to the stabilised voltage V_Z at pin 2.

Output stage

The output stage of the TDA1060 is shown in Fig.21. The npn output transistor is driven via a transistor switching circuit and a latch to prevent double pulsing of the output during one pulse period. As shown in Fig.8, the output latch receives a 'set' pulse via TR_1 and TR_2 when the amplitude of the sawtooth waveform reaches V_H (start of flyback). This defines the start of the SMPS output transistor conduction period δT. As shown in Fig.21, the output latch is reset by either the PWM output or by the overcurrent protection circuit. This defines the end of the SMPS output transistor conduction period. The output latch is bypassed by an OR gate which inhibits the output pulses while the latch is being set or reset.

Both the collector and the emitter of the output transistor are brought out to pins of the TDA1060, thereby permitting flexibility of design for the base drive circuit of the SMPS output transistor. This also eliminates the switching voltage spikes on the internal 0 V bonding wire which could occur if the emitter were internally grounded. The output transistor is protected against collector voltages exceeding the IC supply voltage by internal clamping diodes. The maximum permissible output current is 30 mA with a saturation voltage of not more than 400 mV. The output pulses will cease if the emitter voltage of the output transistor rises above 5 V.

Overvoltage and SMPS output transformer core saturation protection

As shown in Fig.21, a level of more than 0.6 V at pin 13 of the TDA1060 will cause the output transistor to cease conducting, thereby inhibiting the output pulses. This input can therefore be used for overvoltage protection or to prevent saturation of the core of the output transformer of a high-power forward converter during transient conditions.

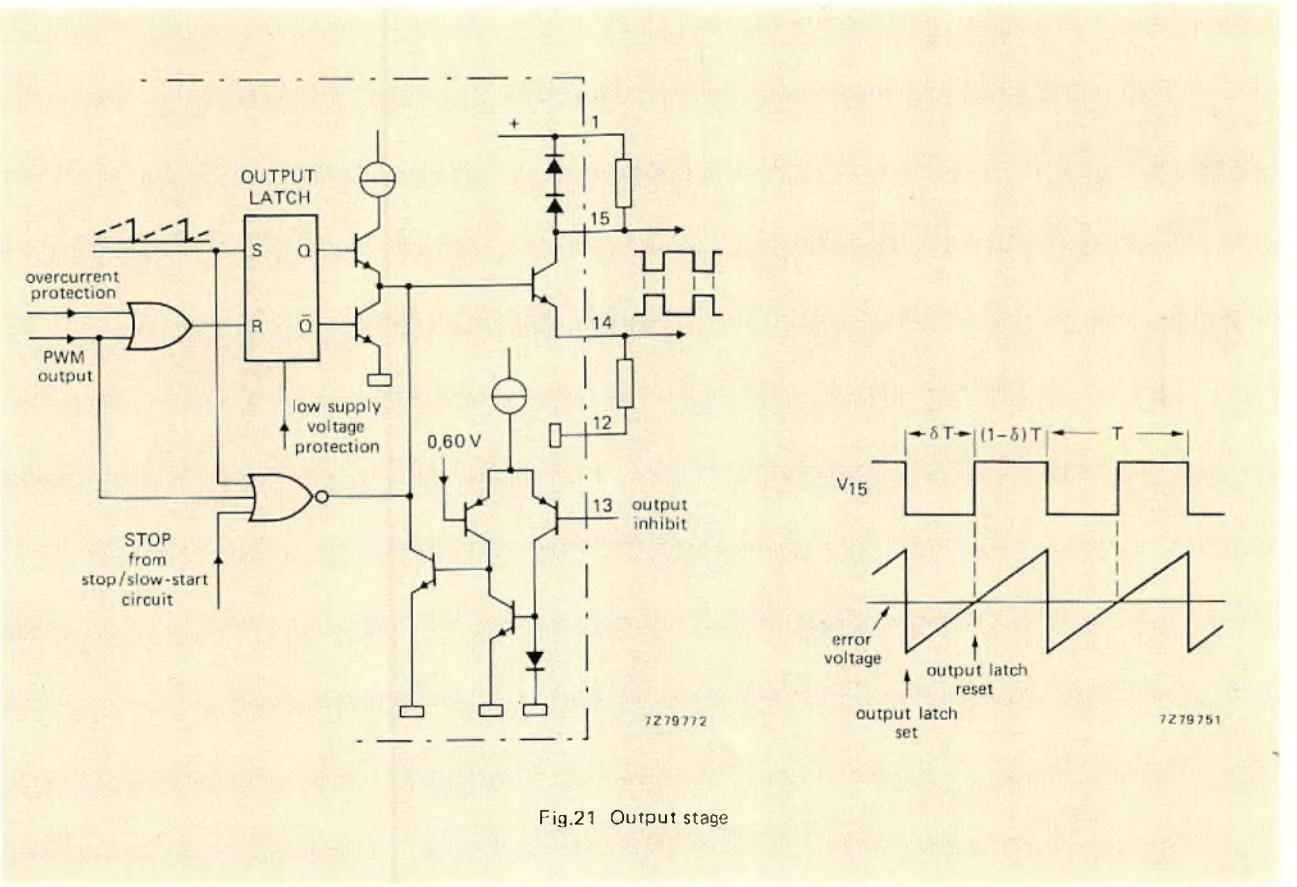


Fig.21 Output stage

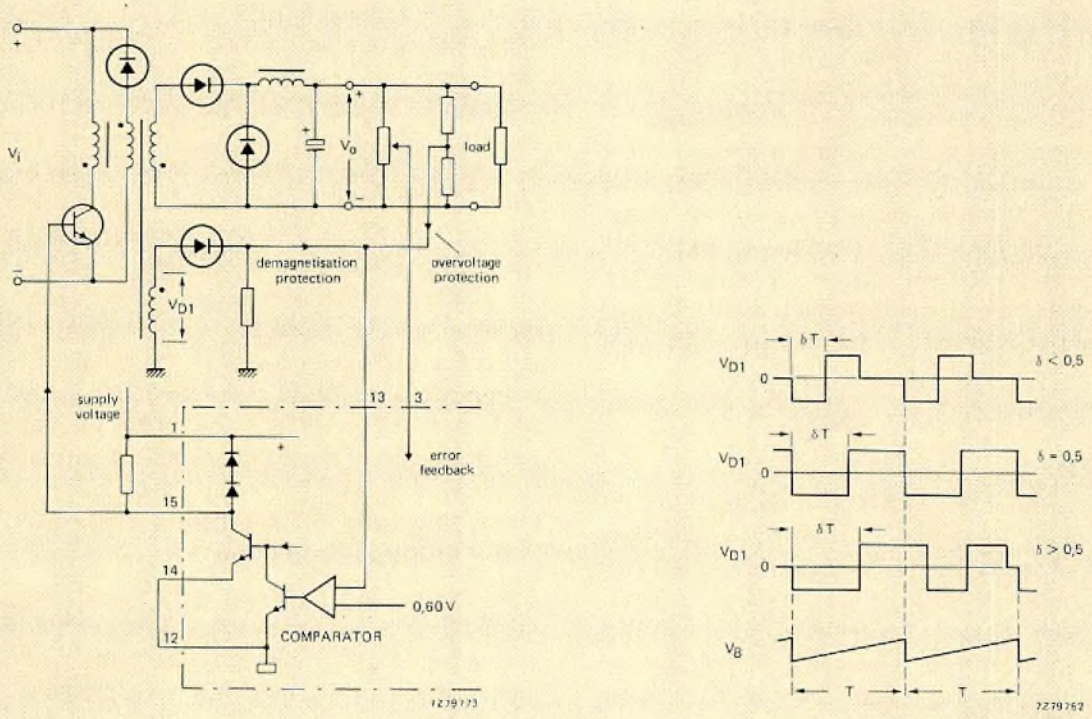


Fig.22 Output inhibiting for overvoltage protection and/or prevention of output transformer core saturation

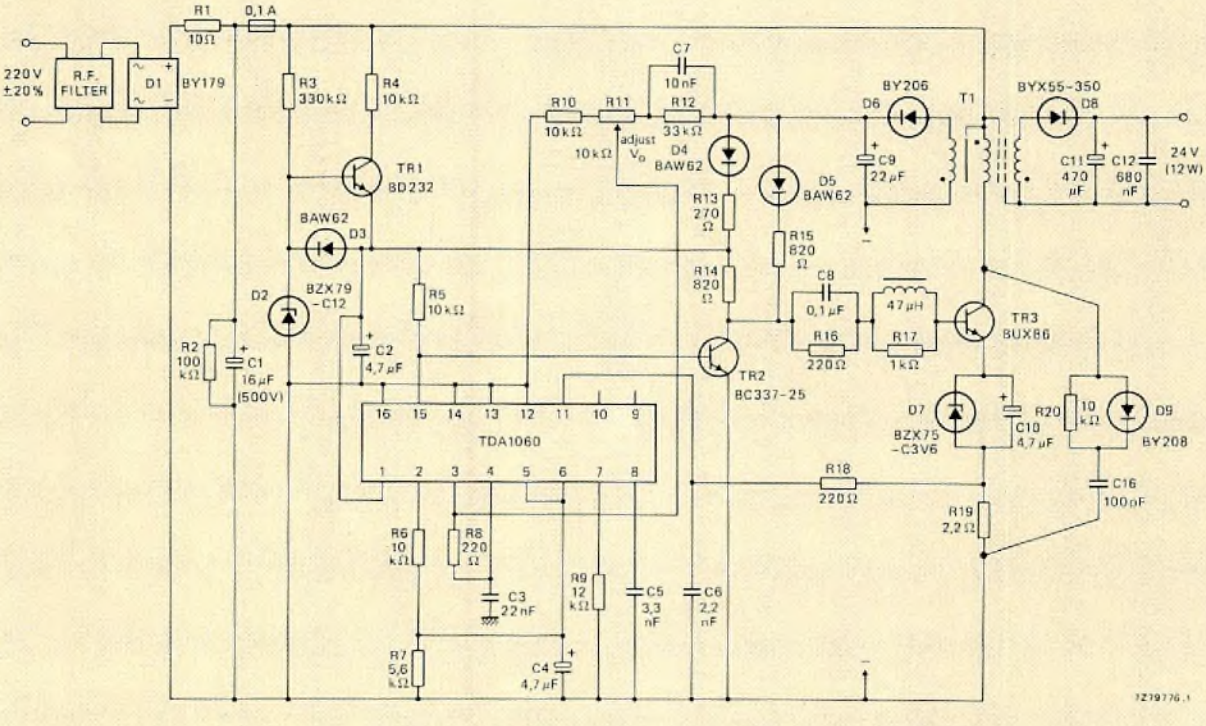


Fig.23 24 V, 12 W SMPS using a flyback converter

Figure 22 shows that, if the duty factor of the SMPS output pulses exceeds 0.5, the average value of the voltage across D_1 during switching period T will be greater than zero. This indicates that the core of the output transformer has been unable to completely demagnetise during the off-period of the SMPS output transistor. If the voltage at the cathode of D_1 is applied to pin 13 of the TDA1060, the integrated output transistor will be prevented from conducting again until the voltage at the cathode of D_1 has fallen below 0.6 V, indicating demagnetisation of the core of the SMPS output transformer. It should be noted that the sawtooth period is not affected by this action.

The overvoltage protection can be achieved by feeding a portion of the SMPS output voltage to pin 13. If this voltage exceeds 0.6 V, the previously described inhibiting action will be initiated.

It should be noted that double pulsing at the output of the TDA1060 can occur when using the inhibit function at pin 13 because the output latch is then bypassed. Pin 13 must be connected to the common return if it is not in use.

THE TDA1060 IN PRACTICAL SMPS CIRCUITS

24 V/12 W SMPS with a flyback converter

Figure 23 is the circuit of a 220 V a.c. mains-fed SMPS capable of delivering an output of 24 V at up to 0.5 A. The circuit will regulate the output voltage for load variations from 70 to 100% (I_O min = 0.35 A). The feedback information for pin 3 of the TDA1060 is derived from a supplementary winding on the SMPS output transformer. This winding also provides the supply current for the TDA1060 and for the driver stage for the BUX86 power switching transistor. At switch-on, a starting circuit comprising TR_1, D_3, and R_2 provides the initial power for the IC until the feedback voltage takes over and power becomes available from the output transformer. Design details for this SMPS are given in the reference.

The performance of the circuit is shown by Figs.24, 25, and 26. Curves a and b of Fig.24 show the load regulation for V_{in} min and V_{in} max. The maximum change of output voltage is 200 mV (<1%) for the specified load range of 0.35 to 0.5 A. If the output is unloaded, the output voltage increases to about 10% above the nominal value. If this is unacceptable, either a fixed pre-load must be applied or the output transformer must be redesigned to accommodate a greater load range. As a comparison, curve c of Fig.24 shows the load regulation if the feedback voltage is derived directly from the output of the SMPS (no mains isolation).

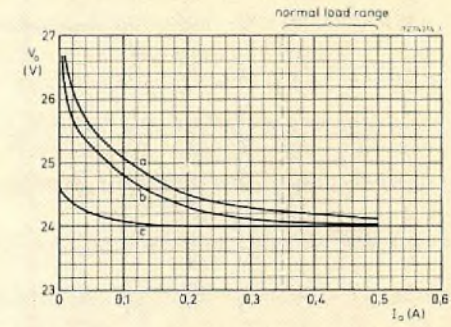


Fig.24 Load regulation for (a) V_i = 375 V d.c. (mains voltage 20% above nominal), (b) V_i = 240 V d.c. (mains voltage 10% below nominal), (c) control input taken direct from output voltage

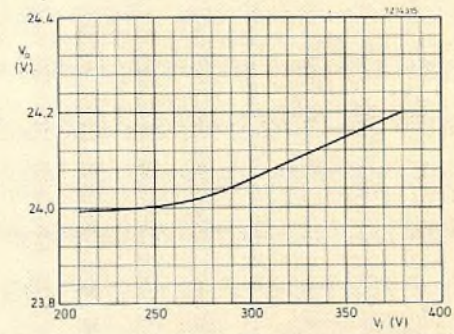


Fig.25 Line regulation (rated load). The plot covers a mains input voltage range from about −20% to +20% with respect to 220 V r.m.s.

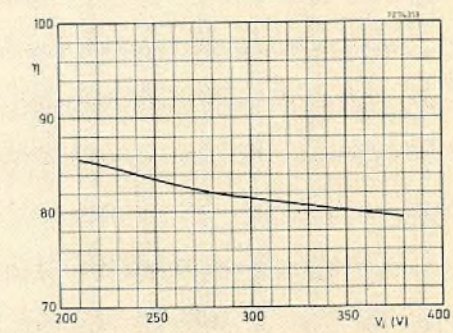


Fig.26 Efficiency at rated load as a function of converter d.c. input voltage. The plot covers a mains input voltage range from about −20% to +20% with respect to 220 V r.m.s.

Figure 25 shows the output voltage regulation at the maximum load (0.5 A). The maximum change of output voltage is 200 mV (<1%) for input voltage variations corresponding to ±20% variation of the nominal 220 V a.c. mains input.

Figure 26 shows the efficiency of the SMPS as a function of input voltage variations corresponding to ±20% variation of the nominal 220 V a.c. mains input. The efficiency varies from 79.5 to 85.5%.

24 V/240 W SMPS with a forward converter

Figure 29 is the circuit of a 220 V mains-fed SMPS capable of delivering an output of 24 V at 10 A. Since this circuit is required to regulate both the output voltage and current, the control is effected at the secondary side of the output transformer. Mains isolation is included in the output transformer, the driver transformer (standard component), and in the small auxiliary mains transformer that provides the +20 V supply for the driver and control circuits.

The voltage feedback is derived from potential divider R_{20}, R_{21}, and R_{22}, and fed to the error amplifier input at pin 3 of the TDA1060. The closed-loop gain of the error amplifier is set by feedback resistor R_{17} and the source resistance determined by R_{18} in conjunction with the parallel resistance of the potential divider at the junction R_{21}/R_{22}. As previously explained, the closed-loop gain of the error amplifier is given by:

$$A_f = \frac{A_O}{1 + \beta A_O} \approx 62.5 \approx 36\ \text{dB}$$

where A_O is the open-loop gain = 60 dB = 1000, and

$$\beta = \frac{R_{source}}{R_{17}}$$

Figure 6 shows that, with a frequency-compensation capacitor of 22 nF, this gives a low-pass corner frequency of about 10 kHz. The influence of this on the phase shift of the total loop can be ignored because the corner frequency of the total loop is determined by the inductance of the output choke L_2 and the value of the output smoothing capacitor C_{17}. With $L_2 = 320\,\mu H$ and $C_{17} = 4700\,\mu F$, the low-pass corner frequency of the total loop is:

$$f_O = \frac{1}{2\pi\sqrt{(L_2 C_{17})}} \approx 130\ \text{Hz}.$$

Figure 27 shows the regulation of the output voltage as a function of the mains input voltage with output current as a parameter. The maximum output voltage variation is 90 mV (<±0.2%) for −10% +20% mains input voltage variation with loads from zero to maximum (10 A).

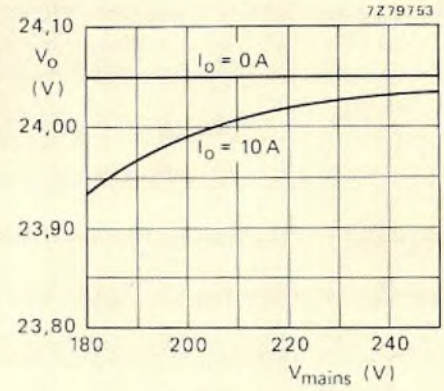


Fig.27 Output voltage regulation as a function of r.m.s. mains input voltage with load current as a parameter

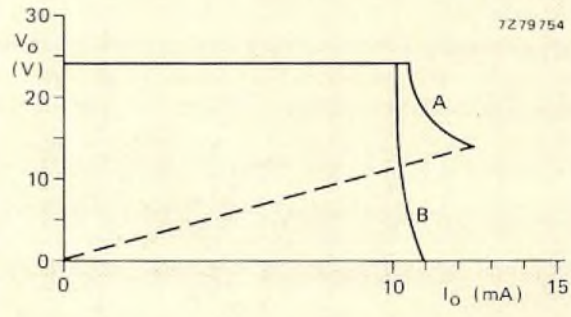


Fig.28 Output V/I characteristic. Curve A was achieved using a current sensing transformer in the collector lead of the SMPS output transistor. Curve B was achieved by sensing the output choke current

The magnitude of the output choke current is a good indication of both the output current of the SMPS and the collector current of the output transistor. The choke current can therefore be sensed and used for current regulation and overcurrent protection. The current is sensed by 10 mΩ wire bridge R_{23}. The voltage developed across this resistor (≈100 mV at full load) is compared with a reference voltage (developed across the resistors R_{24} and R_{25} and derived from V_Z at pin 2 of the TDA1060) by an operational amplifier NE535. The output from the NE535 is applied to the additional PWM input of the TDA1060 at pin 5. This results in the output V/I characteristic shown by curve B of Fig.28. Curve A was obtained when using a current-sensing transformer connected in the collector lead of the SMPS output transistor, the output from the transformer being connected to the overcurrent protection input of the TDA1060 at pin 11.

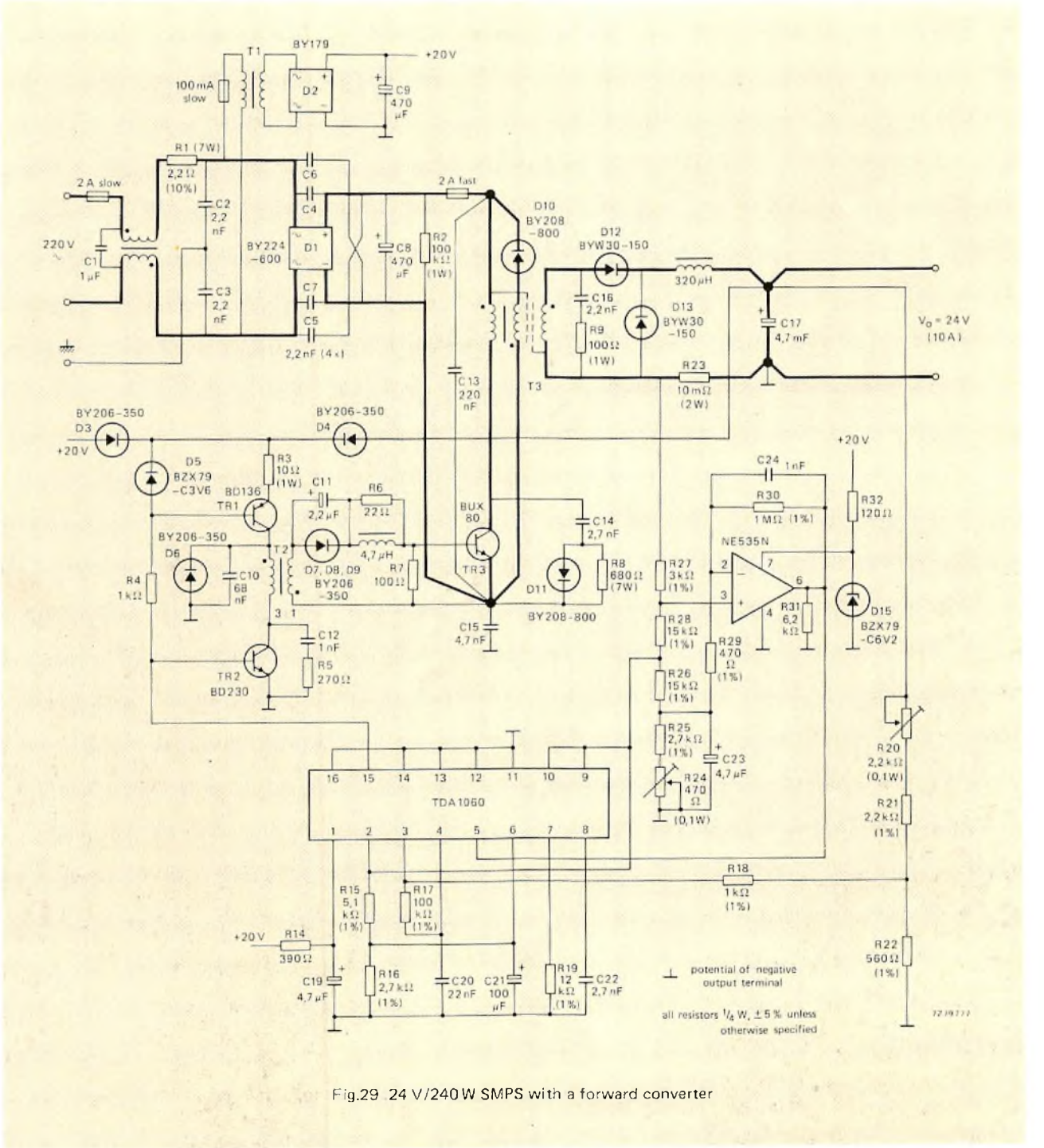


Fig.29 24 V/240 W SMPS with a forward converter

Figure 30 shows that the current regulation method used in the circuit of Fig.29 responds quickly enough to protect the SMPS output transistor if the output of the supply is short-circuited. The figure shows that the current does not overshoot when an output short-circuit occurs.

The measured overall efficiency of the SMPS is shown in Fig.31. When the output is fully loaded, the efficiency of the SMPS is greater than 90%. The efficiency remains above 70% when the output load is reduced to 20% of the maximum.

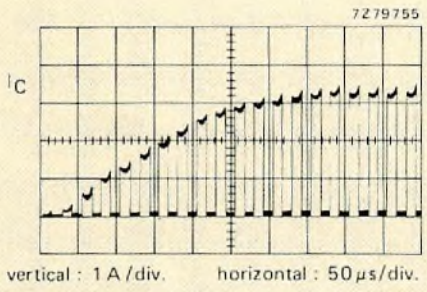


Fig.30 Response of current protection circuit. (from no load to short-circuit)

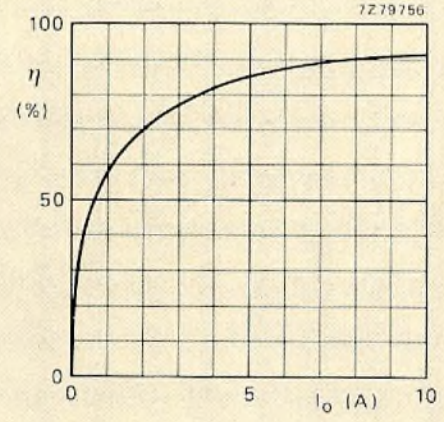


Fig.31 SMPS efficiency as a function of output current

SMPS with double-forward or push-pull converter

Double-forward and push-pull converters are basically two parallel-connected forward converters being driven alternately. Figure 32 shows how standard integrated logic circuits can be used to steer the output pulses from the TDA1060 alternately to the two drive circuits. The symmetry and protection circuits that are necessary to ensure safe operation of a push-pull converter are not shown.

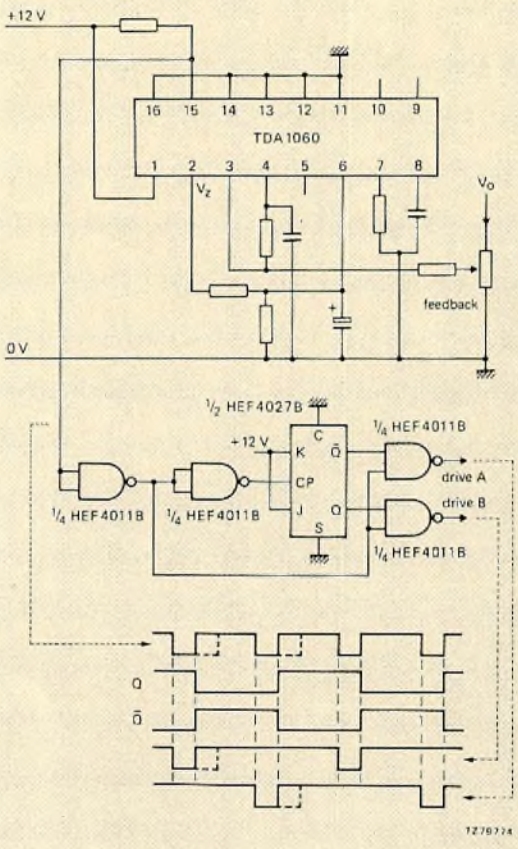


Fig.32 Pulse steering circuit for SMPS using a double-forward or push-pull converter

REFERENCE

12 W, 24 V SMPS using, BUX86, Technical Note 027. N.V. Philips' Glocilampenfabrieken, Elcoma Marketing Communications. Eindhoven, The Netherlands. 1976.

Mains pollution caused by domestic appliances

Part 1 - Definitions and Standards

W. EBBINGE

Thriving demand for electrical appliances creates problems for both appliance manufacturers and electricity suppliers. The latter are committed to providing alternating current of reliably constant voltage, frequency, and waveform. At the same time, manufacturers must satisfy consumer demand for appliances with a wider range of capabilities, increased operating convenience, and greater efficiency. To do so they must avail themselves of modern solid-state electronics, and especially of such power control devices as thyristors, triacs, and switching transistors. Improperly applied, however, these can be a source of mains pollution: that is, of amplitude and waveform disturbances that adversely affect the electricity distribution network and other electricity users.

Recognition of this problem was one of the factors that led the electrical industries and supply authorities of the E.E.C. and E.F.T.A. to create the European Committee for Electrotechnical Standardisation (CENELEC). In its Standard EN 50 006 (Ref.1), CENELEC has recommended limits for three types of mains pollution and prescribed methods for measuring them:

- harmonic distortion
- flicker
- d.c. bias.

An understanding of what these are, how to measure them, and how to keep within the recommended limits, has now become essential to designers and manufacturers of electrical appliances. Here we shall deal with the applicable definitions and standards. Subsequent articles will treat each type of pollution in more detail and point the way to preventive measures.

HARMONIC DISTORTION

The mains waveform should be a pure sinusoid. Any other waveform of the same frequency can be synthesised by the superposition of other sinusoids at integral multiples of that frequency: f, $2f$, $3f$, etc. Here, f is referred to as the *fundamental*, and $2f$, $3f$, etc. as the second, third, etc. *harmonics*. Thus, if the mains waveform assumes any shape other than a pure sinusoid, it is said to contain harmonics. The more it departs from sinusoidal the greater the harmonic content.

Quantitatively, *harmonic content* is defined as the ratio, expressed as a percentage, of the r.m.s. value of a harmonic to the r.m.s. value of the fundamental. CENELEC Standard EN 50 006 defines allowable *harmonic distortion* in terms of the content of each harmonic of the mains frequency from the second to the fortieth.

Maximum harmonic content permitted by the CENELEC recommendations

	harmonic order (n)	maximum harmonic content %
odd harmonics	3	0.85
	5	0.65
	7	0.60
	9	0.40
	11	0.40
	13	0.30
	15 . . . 39	0.25
even harmonics		
(a) symmetrical control	2 . . . 40	0.20
(b) asymmetrical control	2	0.30
	4 . . . 40	0.20

Any switching action (or in fact any load impedance variation) that does not coincide with the zero-crossing of the mains waveform can introduce harmonic distortion. Consider for example Fig.1, which shows a control circuit such as might be found in a light dimmer. On each alternation of the mains, the diac D triggers the triac TR into conduction at a mains phase angle determined by the setting of the variable resistor. The waveform of the resulting output current departs substantially from a pure sinusoid; the harmonic content is therefore high.

Operating as it does on both alternations of the mains cycle, the triac in the circuit of Fig.1 gives what is known as symmetrical control. If it were to be replaced by a thyristor, the control would be asymmetrical and the waveform would be as shown in Fig.2. In general, asymmetrical control gives higher harmonic content than symmetrical control, especially in respect of even-order harmonics.

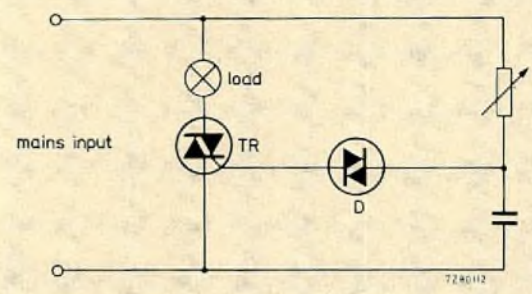
Another source of harmonic distortion is the bridge rectifier circuit often found in television receivers. When operating into a capacitive load this can be a particularly troublesome source; the current waveform seen by the mains is as shown in Fig.3. Other sources are transformers and fluorescent lights. Switched-mode power supplies may be yet another, although not enough experience has yet been gained with their use in domestic appliances to judge how serious a one.

Harmonics from any of these sources can be fed back into the mains, where they may affect other electrical equipment such as hi-fi installations or remote-control equipment as used with night-tariff or street-lighting meters.

The extent to which they are fed back depends in part on the impedance of the source. A purely resistive impedance, such as that represented by a controlled lamp or heating element, is generally worst; and the lower the impedance the worse the harmonic distortion.

It also depends on the impedance of the mains. The higher the mains impedance, the greater the harmonic distortion due to a given source. Mains in urban areas, which normally have low impedance, are less liable to pollution by harmonic distortion than those in rural areas where there are fewer consumers and the impedance is correspondingly higher. Areas with inadequate or outmoded grid systems, where electricity usage has outpaced renewal, are particularly vulnerable.

For purposes of measuring or calculating harmonic distortion, the CENELEC standard specifies a hypothetical mains impedance of $(0.40 + 0.25j)\Omega$ at 50 Hz. This value (sometimes called conventional, artificial, or reference impedance) may later be revised in the light of further information on the effective value of the mains impedance at harmonic frequencies and on the combined effect of many sources of disturbance operating simultaneously on the same mains.



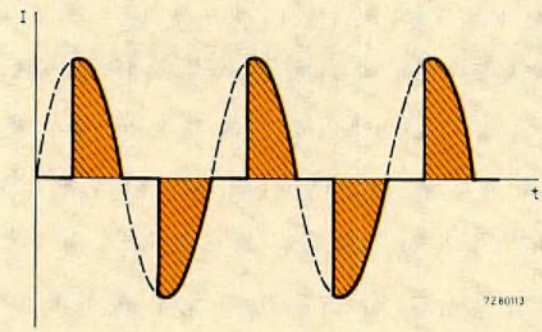


Fig.1 Symmetrical phase control.
Typical circuit and output current waveform

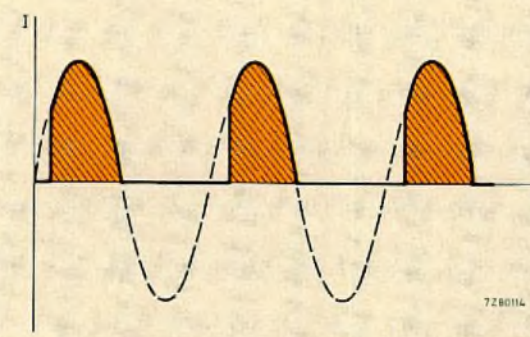


Fig.2 Typical current waveform for asymmetrical control

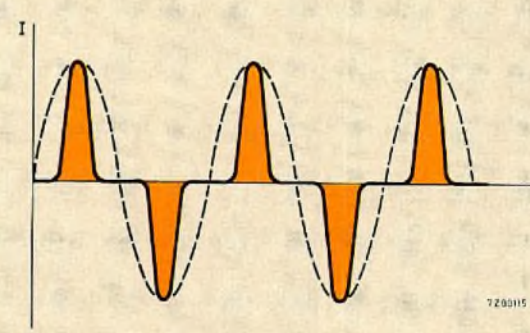


Fig.3 Current waveform of a bridge rectifier circuit

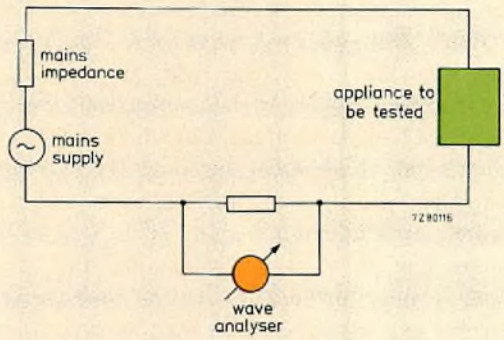


Fig.4 Recommended set-up for measuring current harmonic distortion due to an electronically controlled appliance

In simple cases the harmonic distortion fed back into the mains can be calculated analytically; an example for phase control of a resistive load is given in Ref.2. For more complicated cases it may be preferable to use a wave analyser, as shown in Fig.4, with an appropriate network to simulate the $(0.40 + 0.25j)\Omega$ mains impedance. Either way, when the appliance is driven from the nominal mains voltage at 50 Hz, the harmonic content should not exceed the values recommended by CENELEC, as given in the Table on p. 49. (If a wave analyser is used, the measurement may be affected by distortion already present on the mains; this should be checked and guarded against.)

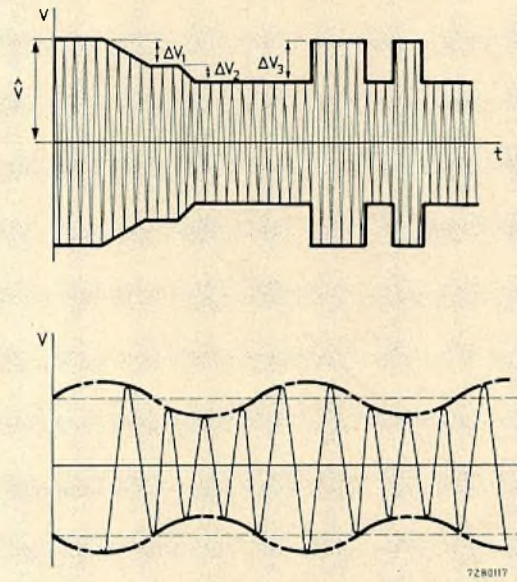


Fig.5 Voltage changes due to a controlled appliance may be gradual, abrupt, irregular, or periodic

FLICKER

The mains voltage should be constant. Load variations can cause it to fluctuate, however, either irregularly or periodically (Fig.5). High-power industrial usage is chiefly to blame, but domestic appliances play a part too. Amongst the offenders are dish-washers, washing machines, refrigeration equipment, motor speed controls, and electrical central heating installations.

Because of its effect on lighting, this type of mains pollution is called flicker. Fluctuations of light intensity can be severely irritating. Results of investigations of this effect are summarised by the curve reproduced in Fig.6, which has been adopted by CENELEC as a standard for evaluating flicker. The curve shows the maximum voltage variation, as a function of frequency, that can be generally tolerated in lighting circuits before discomfort is evident; the dip around 1000 cycles per minute marks the frequency region at which sensitivity to flicker is greatest.

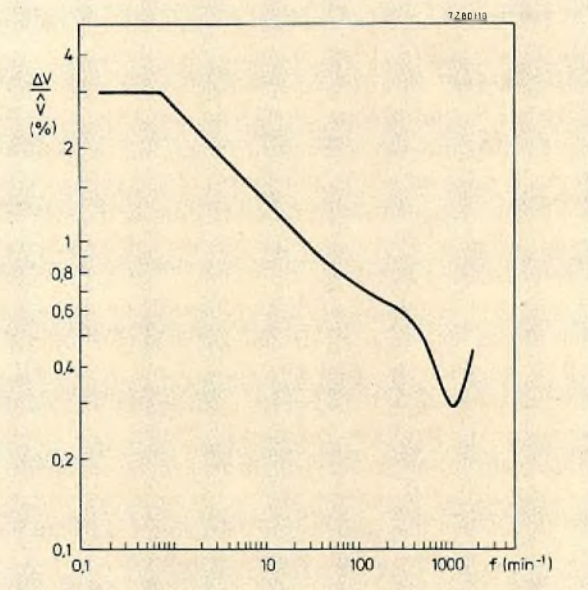


Fig.6 Flicker curve; relative voltage variation as a function of frequency, defining the threshold of unacceptable irritation embodied in the CENELEC recommendations

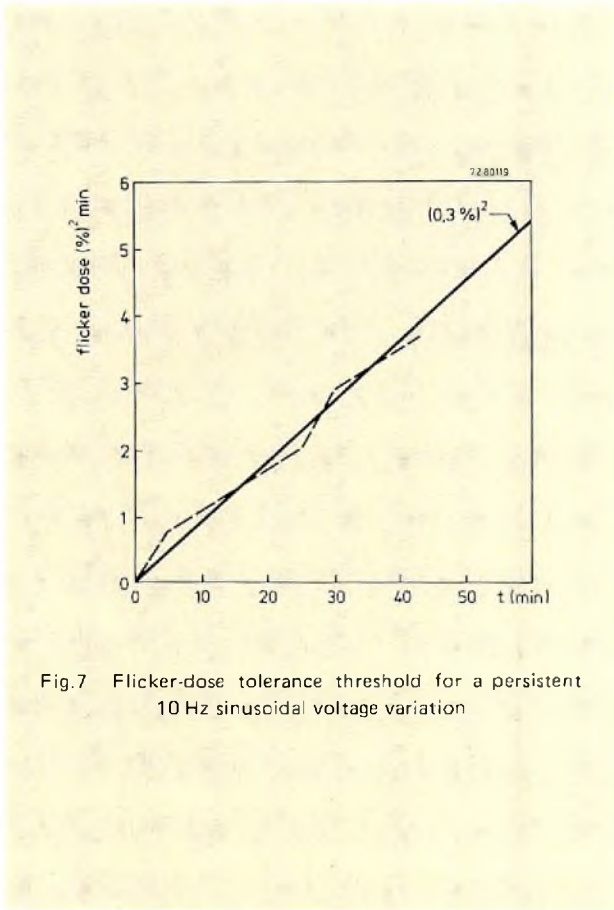


Fig.7 Flicker-dose tolerance threshold for a persistent 10 Hz sinusoidal voltage variation

The irritating effect of flicker depends not only on amplitude and frequency but also on duration of exposure. Flicker that might be tolerable over a short period may become intolerable over a long one. Experience has shown that this time-dependent effect, known as *flicker dose*, is proportional to the square of the voltage variation. The accepted unit of flicker dose is the $(\%)^2$ minute, where $(\%)^2$ refers to the relative voltage variation expressed as a percentage.

Figure 7 is a graph of flicker-dose tolerance based on the flicker due to a 10 Hz sinusoidal modulation of a 50 Hz supply. The solid line corresponds to a relative voltage variation of 0.3%, which is the limit for indefinite tolerance under these conditions. A persistent flicker dose lying above the line will, in general, be experienced as intolerable. However, if the flicker varies, as indicated by the dashed line, brief excursions above the limit line are tolerable provided the average remains below it.

At frequencies below about 120 cycles per minute the voltage fluctuations that cause flicker can fairly easily be measured directly, provided their frequency and amplitude are constant. At higher frequencies a flicker meter is preferable. Of those in use the most popular is the one developed by the French electricity authority (EDF). This measures the frequency and amplitude of the flicker and indicates by a red or green light whether or not they exceed a certain threshold of irritation. The EDF threshold correlates with the CENELEC flicker curve but does not entirely agree with it.

Flicker due to voltage fluctuations that are not constant is more difficult to assess. No satisfactory method has yet been devised, or least none that has the unqualified endorsement of CENELEC.

D.C. bias

Certain types of loads can disturb the symmetry of the a.c. waveform, imposing a d.c. bias on the mains. Examples are half-wave rectifiers and appliances using asymmetrical phase control. The consequences are potentially cumulative, increasing in severity as the number of such loads increases, and can result in saturation of supply transformers and the creation of damaging electrolytic effects. For permanently wired appliances, such as cookers, water heaters, and electrical central heating installations, it is therefore especially important to ensure that there is no possibility of imposing d.c. bias or asymmetric loading on the mains. Any d.c. leakage in the appliance can aggravate the problem and should also be guarded against.

For appliances that are not permanently wired, the randomness with which plugs are inserted tends to neutralise cumulative effects of d.c. bias, at least in countries where mains plugs are symmetrical. In countries such as England and Australia, where mains plugs are polarised, however, pluggable appliances can create as great a risk of cumulative d.c. bias as permanently wired ones.

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2. HAENEN, G. Evaluation of mains-borne harmonics due to phase-controlled switching. Electronic Applications Bulletin, Vol. 33 no. 1, July 1975, pp. 13 to 28.

Reliable thyristors and triacs in TO-220 plastic packages

P. BLUNT

No devices make more demands on power semiconductor fabrication techniques than thyristors and triacs. Their construction and packaging must withstand rapid, large fluctuations of temperature and provide effective insulation to enable high voltages to be handled by small structures. They must have stable leakage characteristics to prevent false triggering. These requirements have not been well satisfied by traditional technology. However, eutectic bonding and diffusion isolation have now overcome the conformance and reliability barriers set by the usual soft-soldered TO-220 thyristor and triac construction methods. Power-control equipment using TO-220 devices based on the new technology is setting new standards for reliability. This article gives the reasons for the design changes, and justifies them with intermediate results from continuing, long-term life testing.

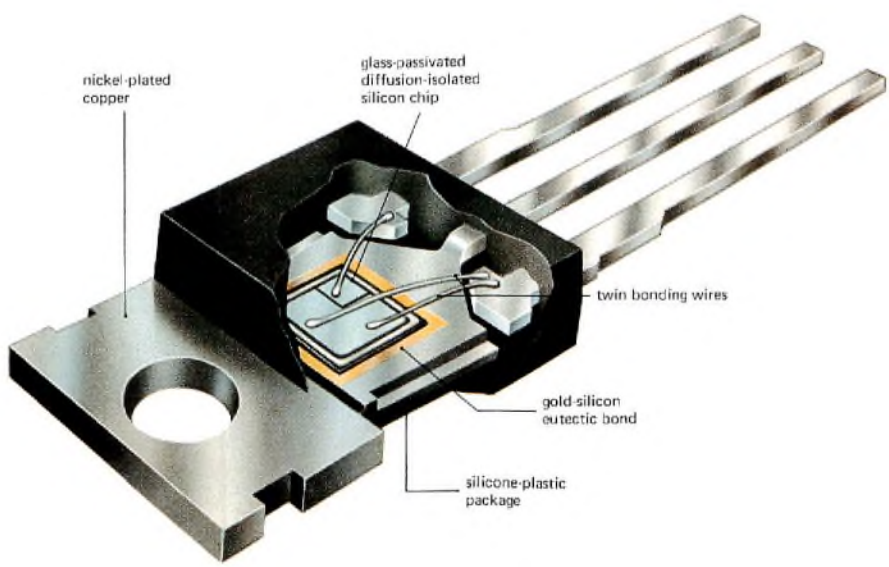

Fig.1 Cut-away view showing principal constructional features of TO-220 thyristors and triacs; diffusion isolation and glass passivation are the key to improved reliability

THYRISTOR AND TRIAC CONSTRUCTION

Traditional construction is based on a double mesa chip. Figure 2 shows the basic problems. A rim of glass around the base of the chip means that a soft-soldered bond must be used. Soft solder tends to deteriorate with time at elevated temperatures; it undergoes plastic deformation when subjected to thermally-induced mechanical stresses. Thermal conductivity is poor at the outset and gets worse, resulting in poor fatigue performance.

Device quality is limited by production problems. On-slice testing is not possible because the n-type bases are interconnected before dicing. Exposure of the base after dicing can allow complete or partial shorting during the soldering process. Complete shorts will be detected, of course, but partial shorts may not be detected by inspection and may cause trouble later. Coinciding mesa troughs weaken the chips, increasing the incidence of cracking due to thermal stresses.

How can the desired properties be achieved using available technology? Firstly, a low, stable thermal resistance is required, coupled with a chip bond that resists thermal cycling stresses. Experience with power transistors has shown that a gold-eutectic bond is unexcelled in these respects. Eutectic bonding, however, requires a flat chip base with the active regions remote from the bonding surface.

Excellent isolation is also necessary. This can be achieved using diffusion-isolation which isolates the edges completely, leaving all region interfaces on the upper surface and making it possible to deposit wide glass strips for insulation between active regions. The base of the chip is flat and suitable for eutectic bonding. On-slice testing is now possible, an additional quality safeguard. Moreover, the device cannot be damaged by dicing or the effects of bonding. This design is shown in Fig.3. It is used in all our TO-220 thyristors and triacs.

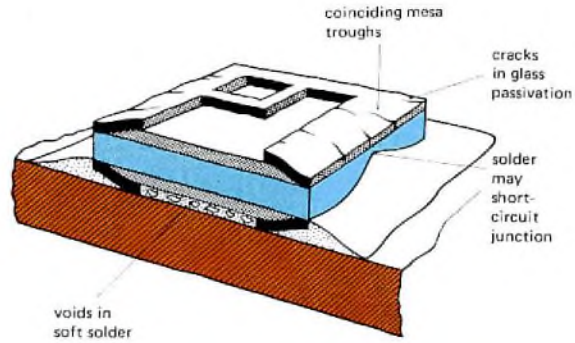

Fig.2 The disadvantages of the old form of thyristor construction are obvious in this drawing

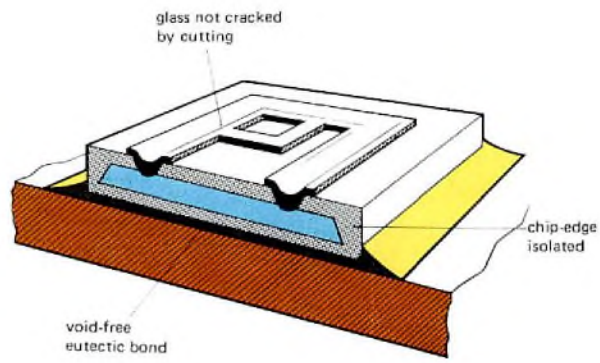

Fig.3 Diffusion isolation solves problems inherent in the old design

QUALITY

Reliable quality parameters can only be obtained by the objective reduction of valid test results. Here we present intermediate results from a continuing series of long-period life tests on samples of production TO-220 eutectic-bonded triacs and thyristors. Life testing is carried out under a variety of conditions and to a number of national and international standards. The results are presented in a form suitable for easy comparison. In addition, some notes on test methods are given.

Although quality is determined by testing, no amount of testing will improve it. Quality must be inherent in design and production, which is why so much attention has been given to the detail design of the TO-220 devices and development of the eutectic-bonded, diffusion-isolated construction.

The new design was carefully evaluated during pilot production by means of measurement and life testing. During production proper, the care with which the design is reproduced is monitored by further testing carried out by the Quality Control Laboratory on randomly-taken samples. The results of these tests are fed back to ensure that the highest standards of workmanship are maintained and any residual design faults corrected.

Figure 4 shows how the production and inspection of TO-220 thyristors and triacs are integrated to ensure a quality product. Devices are checked at each stage in their production from component parts to finished device. The finished product is 100% inspected – and then checked again.

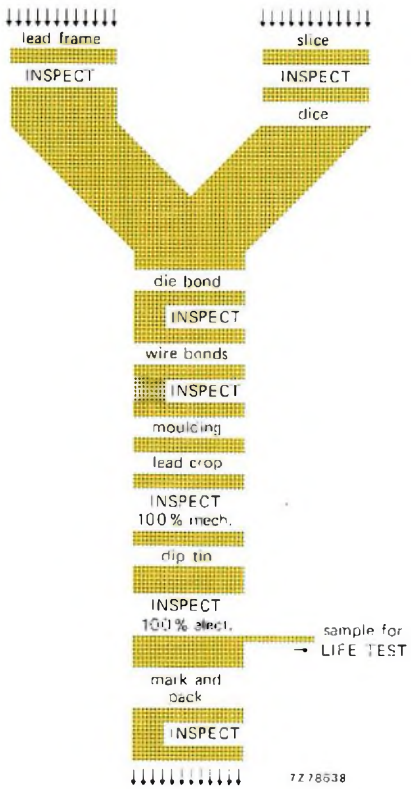

Fig.4 Careful integration of production, inspection and quality control is the key to maintaining quality

Conformance

Conformance is specified in terms of AQL, acceptable quality level; the TO-220 devices described here are always supplied to an AQL, even when none is specified. Our standard AQLs for TO-220 thyristors and triacs are given in Table 1; they are of course determined according to the methods laid down in MIL-STD-105D and IEC Publication 410 (BS6001).

Following the 100% factory inspection, a sample from each batch of TO-220 devices is routed to the Quality Control Laboratory and checked to established whether the batch satisfies the specified AQLs.

Reliability

Life tests reveal failure rate and its time dependence. These are the two fundamental measures of reliability..

TABLE 1

AQLs for TO-220 eutectic thyristors and triacs. Definitions and methods are those of MIL-STD-105D and IEC Publication 410 (BS6001)

inspection criterion	AQLs		inspection level
	individual	combined	
mechanical/visual			
major dimensions		1.5%	I
other dimensions			
visual			
electrical characteristics			
major	0.4%	0.65%	II
other		2.5%	II
inoperatives			
mechanical			
+		0.1%	II
electrical			

The point after which failure rate rises above some acceptable level is termed end of useful life.

Life testing must be carried out under conditions that can be related to operating conditions. To reduce testing time and to properly explore the reliability of the device, conditions should be at or above Absolute Maximum Ratings. All our TO-220 devices are tested in this way.

Accelerated life-test methods are currently under investigation in our Quality Laboratory.

TESTS, PURPOSES AND RESULTS

Three main aspects of reliability are explored by the tests carried out on our TO-220 thyristors and triacs. They are: leakage current stability, thermal fatigue, and the effects of hostile environments. All the results given were obtained from tests carried out on triacs and thyristors taken from normal production. Only catastrophic failures are given; these are open or short-circuit devices.

Leakage current stability

All reverse-biased semiconductor junctions exhibit leakage current which varies with the temperature of the junction and the voltage applied. Migration of ions trapped in the passivating glass tends to increase the leakage of passivated devices. In thyristors and triacs, excessive leakage current causes spurious triggering.

We test TO-220 devices at maximum rated voltage and junction temperature. The leakage current and its rate of increase with time are good indicators of the general quality of processing: chip surface stability and the effectiveness of the passivation. If leakage causes a device to turn on, that device is considered a catastrophic failure.

Conditions and results

Table 2 gives the conditions under which d.c. blocking tests are carried out, and Table 3 gives the results of nearly ten million device-hours testing of triacs and thyristors.

Figure 5 shows how leakage current varied with time during the tests.

TABLE 2
D.C. blocking test conditions

device type	voltage (d.c.)	T_{mb} (°C)	gate	notes
triac	V_{D1} = 400 V	110	open	T_1 negative
thyristors	V_D = 400 V	100	open	forward blocking

TABLE 3
D.C. blocking test results
V_D^* = 400 V, T_{mb} = 110 °C, gate open circuit

sample	duration (h)	catastrophic failures	device hours
1083	1200	0	1.3×10^6
318	2400	1	7.6×10^6

* Anode positive with respect to cathode on thyristors. MT2 positive with respect to MT1 on triacs.

Note on test validity

Our tests are carried out with the gate electrode open circuit. Tests in which the gate is connected through a resistor increase the leakage current at which turn-on occurs and are therefore optimistic with an artifically low number of failures.

A.C. operation

Whereas testing is carried out under d.c. conditions, in practice most thyristors and triacs operate under a.c. conditions. Tests indicate that a.c. operation results in about a ten-fold improvement in useful life and reliability compared to d.c. testing at the same temperature.

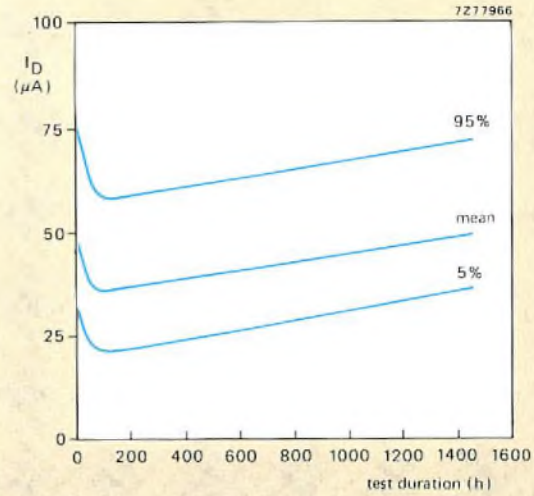

Fig.5 Leakage current variation during the d.c. blocking test. Note the small spread between the 5th and 95th percentiles

TABLE 4
Thermal fatigue test results
I = max rated r.m.s. current
T_j swing from rated T_j (max) to 25 °C

sample	duration (cycles)	catastrophic failures	device cycles
260	10 000	0	2.6×10^6
160	30 000	0	4.8×10^6
120	50 000	0	6.0×10^6
60	100 000	0	6.0×10^6

Thermal fatigue

Cyclic temperature variations induced by power switching stress all internal structures and bonds. Power cycling is thus an effective test of structural integrity. We subject TO-220 thyristors and triacs to maximum rated current until maximum rated junction temperature is reached. The current is then turned off and the devices force-cooled to reduce the junction temperature to 25 °C. This is the most severe possible power-induced temperature cycling test.

Table 4 shows that the eutectic-bonding technique gives a fatigue-free chip bond. Under the same conditions, devices with soft-soldered bonds would show failures after one tenth the number of cycles recorded in Table 4.

Environment

Moisture

Our modern, plastic-encapsulated semiconductors are largely immune to the effects of moisture. More immune, in many cases, than the equipment in which they are used. Junction passivation and pure plastic encapsulants make TO-220 thyristors and triacs exceptionally resistant to moisture, as Table 5 shows. Figure 6 shows how conditions vary through the 24-hour cycle of the test.

TABLE 5
Moisture resistance test results
Relative humidity 95%, T_{amb} = 55 °C, cycle time 24 h

sample	duration (cycles)	catastrophic failures
600	28	0

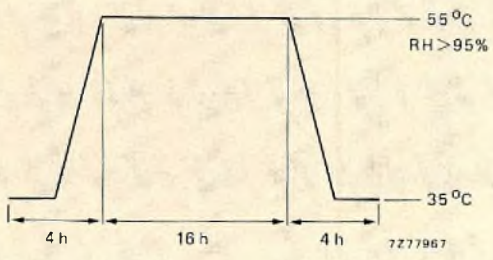

Fig.6 The variation in conditions over one 24 h cycle of the moisture resistance test

Tropical storage

This test is a highly-accelerated simulation of extreme tropical environments. Its results, Table 6, reinforce those obtained by the previous test.

TABLE 6
Tropical storage test results
Steam at 122 °C and 210 kPa absolute

duration (h)	sample	catastrophic failures	device hours
3	300	2	900

High-temperature storage

Any damaging effects of long-term storage at high temperature are revealed by this test. As Table 7 shows, no such effects are apparent.

TABLE 7
High-temperature storage test results
T_{amb} = 125 °C

duration (h)	sample	catastrophic failures	devices hours
1000	500	0	5×10^5

Rapid changes of temperature

This test examines the structural integrity of devices under more severe conditions than the thermal-cycling test. Conditions and results are given in Table 8.

Note that no transition time is specified: the devices move directly from oven to refrigerator. Since thermal capacity is small, the transition from one temperature to another will be brief and the test correspondingly severe.

TABLE 8
Rapid change of temperature test
30 minutes at −40 °C, 30 minutes at 125 °C, fast transition

device	sample	duration (cycles)	catastrophic failures
triac	500	5	5
thyristor	600	5	0

DERATING FOR INCREASED LIFE

As with most semiconductor devices, derating TO-220 thyristors and triacs so that they operate well within their ratings will greatly improve life and reduce failure rate.

Laboratory results

Operation of a device at a junction temperature below $T_{j\,max}$ reduces failure rate and increases useful life. Laboratory measurements on TO-220 thyristors and triacs indicate that the useful life increase is exponential, as shown by Fig.7. This graph may be used to scale the indicated minimum useful life from life testing.

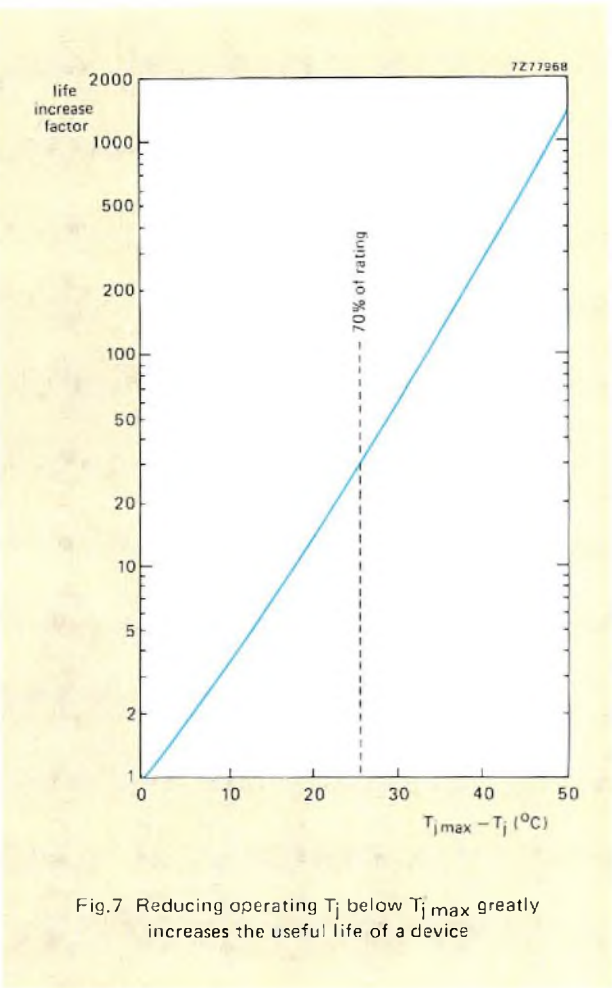

Fig.7 Reducing operating T_j below $T_{j\,max}$ greatly increases the useful life of a device

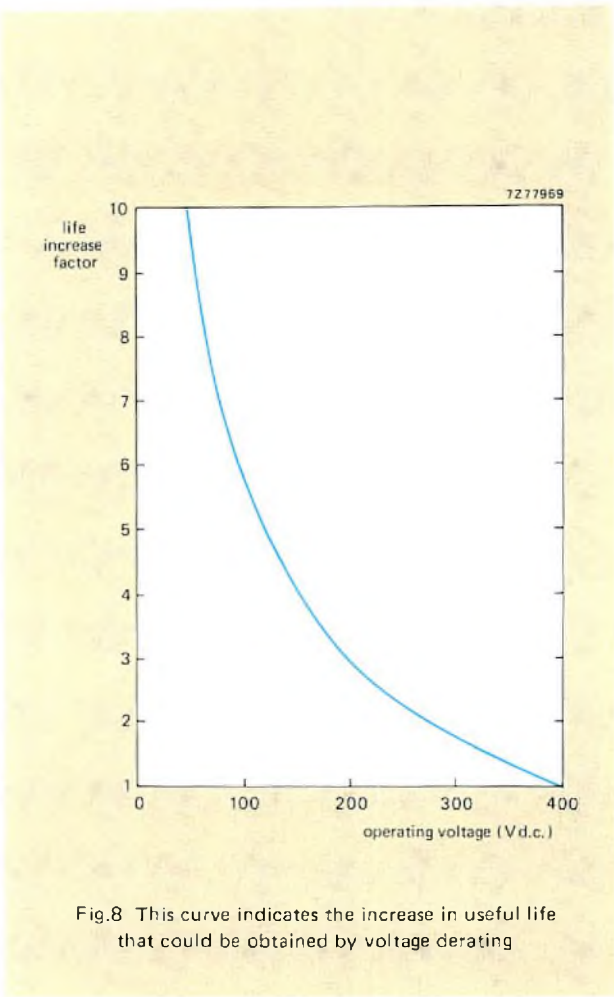

Fig.8 This curve indicates the increase in useful life that could be obtained by voltage derating

Operation at a voltage lower than the maximum rating reduces the rate of increase of leakage current. Figure 8 shows the effect of applied voltage on leakage current increase factor. The data from this graph may be used to derive the effect of derating on the useful life indicated by d.c. blocking tests.

Field results

Eutectic-bonded thyristors and triacs have been in use for about four years and, as expected, there has been no evidence of field failures. It is already apparent from experience of a large-scale application in electric heater controllers that our eutectic-bonded TO-220 devices are significantly more reliable in practice than devices using the older, soft-solder technology.

ACKNOWLEDGEMENT

The author is indebted to Mr. D. Haslem of the Semiconductor Measurement Laboratory at Stockport for his invaluable assistance in preparing the foregoing material for publication.

Segment field magnets for large electric motors

D.C. permanent-magnet motors are now often preferred to a.c. types for many industrial applications: they are cheaper, more reliable, smaller, and simpler to control. Unfortunately, suitable motors are not always available at short notice and at a price commensurate with the intended application, owing to high tooling costs and long delivery lead-in times for the ferrite field magnets required. However, that need no longer be an obstacle.

Ferroxdure segment magnets are now available in most of the sizes required for motors up to 8 kW (about 10 h.p.) with stator diameters up to 250 mm. IEC frame sizes covered by these segment dimensions are 48 to 160. Because of the production methods employed, tooling charges are lower and deliveries can be started quickly. Full magnetic material properties are achieved.

To enable designers to take full advantage of this development, computer-aided analysis and optimisation programs are also available. Amongst other things, these programs can accurately predict the performance of a motor under starting and stall conditions where armature reaction has the greatest effect.

ADVANTAGES OF PERMANENT-MAGNET MOTORS

Cost

For a given total flux, Ferroxdure is significantly cheaper than copper for field generation. Stator construction is simpler, and so manufacturing costs are reduced. Now that suitable magnets are available quickly in moderate quantities and with reduced tool charges, full use can be made of these advantages.

Reliability

Unless they are misused, Ferroxdure magnets are truly permanent. They are not affected by time, voltage transients or mechanical vibration. There are none of the risks of failure due to insulation breakdown as with a wound stator. Thus, motor reliability is nearly doubled when permanent-magnet excitation replaces a field winding.

Control

Electronic control systems for d.c. motors are simpler, and thus often cheaper, than those for a.c. motors. This is especially true where continuous, fine control is required. Moreover, a.c. control systems are a rich source of mains pollution, causing transients that can upset the operation of measuring and control instrumentation.

Size

A Ferroxdure field system is more compact than the equivalent copper winding. A reduction in size of one or two frame sizes is generally possible when a wound field d.c. motor is replaced by a permanent-magnet design.

Efficiency

Permanent-magnet motors are generally more efficient than wound-field types since no dissipation is required to maintain the field. This aspect of design is of increasing importance as energy costs increase. Moreover, the increased efficiency can greatly simplify equipment cooling problems.

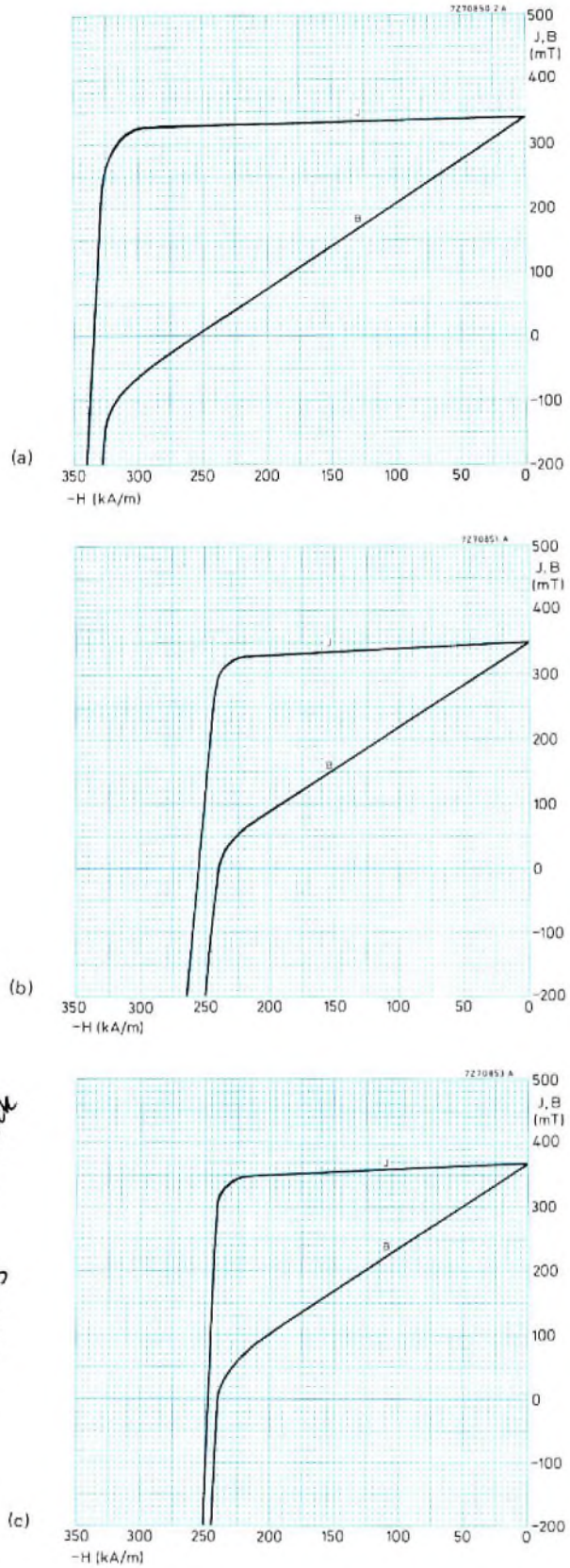

Fig.1 The three grades of Ferroxdure most suitable for large motor field magnets: (a) FXD270; (b) FXD330; (c) FXD380. Both B-H and J-H properties are shown

FERROXDURE SEGMENT MAGNETS

Material properties

Demagnetisation curves for the three grades of Ferroxdure recommended for use in large motors are given in Fig.1. All are anisotropic: their magnetic properties are optimum in the direction in which they are to be magnetised in service. For most motor segments, this preferred direction of magnetisation is radial. FXD270 is a high coercive force ferrite intended for applications where armature reaction is exceptionally high or where low temperatures are encountered. FXD330 is the standard ferrite for motor segments; its higher remanence allows greater flux densities to be achieved. FXD380 has both high remanence and high coercivity and is intended for applications where maximum efficiency or minimum size is required. The main properties of these materials are listed in the table.

Principal properties of the grades of Ferroxdure suitable for large motor magnets: typical values

	FXD270	FXD330	FXD380	units
Remanence	340	370	390	mT
Coercivity	263	239	263	kA/m
Polarization coercivity	334	247	279	kA/m
Maximum energy	21,5	25,5	27,8	kJ/m³

Segment geometries

Field systems for medium and large motors generally consist of two, four, or more segments of ferrite shaped to fit into a tubular steel housing which also acts as the magnetic return circuit. Figure 2 is a section through a two-pole field system of this type. Larger motors generally use four or more segments; this reduces the effect of armature reaction and makes it possible to use thinner segments. A four-pole system, Fig.3, requires a stator housing ring of about half the cross sectional area required for a two-pole system.

Figure 4 shows the main dimensions of a segment magnet. The outer radius of the segment, r_o, is usually made slightly larger than the inner radius of the stator housing. This causes the segment to touch at its ends only and obviates the chance of its rocking within the housing. A small additional air gap is introduced between segment and housing which must be included in the calculation of the field system performance.

Segments of subtended angle β greater than about 120° are shaped so that the housing-contact points are separated by an angle of 90° to reduce the segment-housing gap.

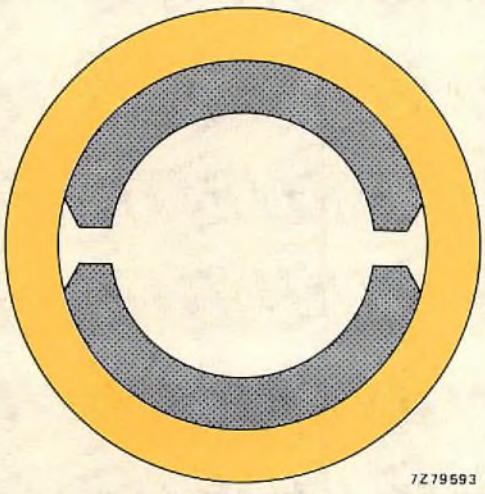

Fig.2 Section through a two-pole motor-field system using Ferroxdure permanent magnets

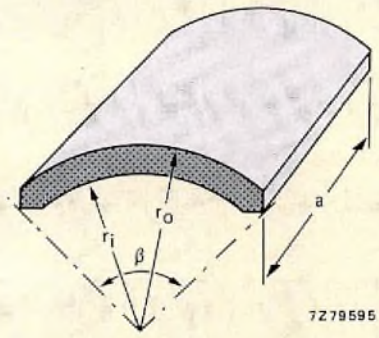

Fig.4 The principle dimensions used to specify a Ferroxdure motor segment magnet

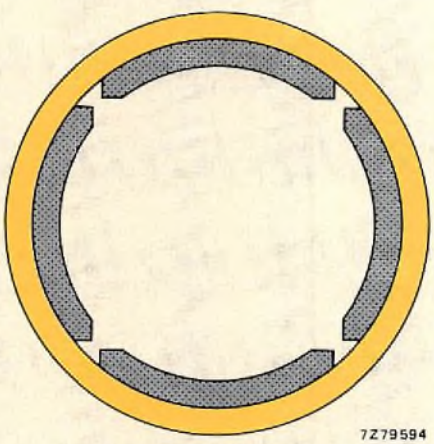

Fig.3 Section through a motor field system with four Ferroxdure segments. Note that the return-ring cross-section has about half the area of that for the two-pole system of Fig.2 and that the segments are about half as thick

LARGE MOTOR SEGMENTS

The range of standard segments contains magnets suitable for most motors of up to 100 mm diameter and 600 W (about ¾ h.p.).

Segments for larger motors are often required in quantities smaller than what has previously been the break-even level for economic tooling. Moreover, samples for development and prototype evaluation have been subject to delays associated with tooling which were often unacceptable, necessitating recourse to a less-than-optimum solution in the form of a wound field d.c. motor or a.c. motor.

Such compromise is no longer necessary. A combination of machining and pressing techniques now makes it possible to offer a range of segments for 4-pole motors in the range 100 mm to 250 mm diameter and up to 8 kW (about 10 h.p.) power. Expensive tools are generally not required and, consequently, initial delivery times are greatly reduced and development samples are available at moderate cost.

Abstracts

Digital control of radio and audio equipment

Part 4 – Displays and control of analogue functions with RTS

This is the second in a series of articles describing a versatile microcomputer-controlled Radio Tuning and control System (RTS). It explains how two new computer-bus compatible integrated circuits are used to drive LED or liquid-crystal displays of frequency, channel number or control position. The article also describes how the ICs can provide digital control of analogue functions such as volume, balance and tone control.

Part 5 – DC-controlled audio switches and filters

This article describes how two new integrated circuits are used to provide static switching of signals in audio preamplifier applications. Since the ICs incorporate a unity-gain operational amplifier in each signal path, they can also be used to construct active filters to eliminate scratch, rumble and infrasonic frequencies during record reproduction.

TDA1060 – A comprehensive control circuit for SMPS

This article describes how a single IC is used to provide the comprehensive control and protection facilities required by switched-mode power supply circuits in applications such as computer and telecommunications supplies with power ratings of between 10 W and 5 kW.

Mains pollution caused by domestic appliances

Part 1 – Definitions and standards

Power control using modern solid-state devices such as thyristors and triacs can seriously disturb the mains supply. This article considers the major types of disturbance produced by domestic appliances, i.e. harmonic distortion, flicker and d.c. effects. The CENELEC Standard EN 50 006 is introduced and its proposals on maximum harmonic content and flicker dose are discussed.

Reliable thyristors and triacs in TO-220 plastic packages

New manufacturing methods significantly improve the conformance and reliability of plastic-packaged thyristors and triacs. Gold-eutectic bonding gives low, stable thermal resistance and diffusion isolation completely isolates the edges of the die, allows on-slice testing, and protects against damage during dicing and bonding. Notable amongst the improvements revealed by life testing are low leakage-current spread and exceptionally low incidence of thermal fatigue effects.

Digitale Steuerung von Rundfunk- und NF-Geräten

Teil 4 – Steuerung und Wiedergabe von Analogfunktionen mit dem RTS-System

Im zweiten Beitrag einer Artikelserie über das vielseitige mikroprozessorgesteuerte Rundfunk-Abstimm-, Bedien- und Anzeigesystem RTS wird der Einsatz zweier neuer integrierter Schaltungen zur Steuerung von LED- bzw. Flüssigkristallanzeigen für die Wiedergabe von Frequenz, Kanalnummer und Analogwertstufen der übrigen Bedienfunktionen beschrieben. Ausserdem wird gezeigt, wie diese integrierten Schaltungen zur digitalen Steuerung von Analogfunktionen (z.B. Lautstärke, Balance, Klangfarbe) verwendet werden können.

Teil 5 – Gleichspannungsgesteuerte NF-Signal-Schalter und -Filter

In diesem Artikel werden zwei neue integrierte Analogsignalschalter vorgestellt und wird beschrieben, wie diese Schaltungen zum Umschalten von NF-Signalen in NF-Vorverstärkern eingesetzt werden können. Da die integrierten Schaltungen in jedem Signalpfad einen voll gegengekoppelten Operationsverstärker enthalten, lassen sich mit diesen Schaltungen auch durch Gleichspannungssignale umschaltbare aktive Filter zur Unterdrückung von Rausch- und Rumpelgeräuschen sowie von Subsonicsignalen aufbauen.

TDA1060 – Eine umfassende Steuer- und Regelschaltung für Schaltnetzteile

Dieser Artikel beschreibt, wie sich mit einer integrierten Schaltung alle Anforderungen bezüglich Regelung und Entstörung erfüllen lassen. Es handelt sich hierbei um Schaltnetzgeräte mit Leistungen von 10 W bis 5 kW wie sie z.B. zur Versorgung von Rechnern und Fernmeldeeinrichtungen benötigt werden.

Beeinflussungen des Versorgungsnetzes durch Haushaltsgeräte

Teil 1 – Definitionen und Normen

Eine Leistungssteuerung mit Hilfe von Halbleiter-Bauelementen wie Thyristoren und Triacs kann zu einer ernsthaften Beeinflussung des Versorgungsnetzes führen. Dieser Artikel behandelt die Hauptarten von Beeinflussungen, die durch Haushaltgeräte verursacht werden. Hierzu gehören Verzerrungen, Flackereffekte und Gleichspannungsanteile. Der CENELEC Standard EN 50006 wird vorgestellt und die darin enthaltenen Vorschläge bezüglich des maximalen Oberwellengehalts und Flackeranteils diskutiert.

Thyristoren und Triacs im TO-220-Kunststoffgehäuse

Mit neuen Fertigungsmethoden konnte die Qualität und Zuverlässigkeit von Thyristoren und Triacs im Kunststoffgehäuse wesentlich verbessert werden. Durch eutektische Bondung ergibt sich ein kleiner stabiler thermischer Widerstand. Mit Hilfe der Isolierdiffusion wird ein vollständige Isolation der Kristallkanten erreicht, die eine Vormessung auf der Kristallscheibe erlaubt und gegen eine Beschädigung der Kristallsysteme beim Trennen und Bonden schützt. Bei den Lebensdauerprüfungen konnte vor allem eine kleine Streuung des Leckstromes und ein aussergewöhnlich geringer Auftreten von thermischen Ermüdungserscheinungen festgestellt werden.

Commande digitale d'équipements radio et audio

4ème partie – Affichage et commande de fonctions analogiques dans le système d'accord radio commandé par micro-ordinateur

Cet article est le second d'une série qui décrit un système polyvalent de commande et d'accord radio commandé par micro-ordinateur. Il explique comment deux nouveaux circuits intégrés compatibles avec bus d'ordinateur sont utilisés pour commander des affichages à LED ou à cristaux liquides de la fréquence, du numéro de canal ou de la position des commandes. L'article décrit également comment les circuits intégrés peuvent assurer la commande digitale de fonctions analogiques telles que le réglage du volume, de la balance et de la tonalité.

5ème partie – Commutateurs et filtres audio à commande par courant continu

Cet article décrit l'application de deux nouveaux circuits intégrés à la commutation statique de signaux dans des préamplificateurs audio. Etant donné qu'un amplificateur opérationnel à gain unitaire est incorporé au trajet de chaque signal dans ces circuits intégrés, ils peuvent également servir à la construction de filtres actifs pour éliminer le bruit d'aiguille, le ronronnement et les fréquences infrasoniques au cours de la lecture des disques.

Control digital de equipo de radio y audio

Parte 4 – Visualización y control de funciones analógicas con 'RTS'

Este artículo es el segundo de una serie que describe un sistema de control y sintonía de radio controlado por microordenador (RTS "Radio Tuning System"). Explica como se utilizan dos nuevos circuitos integrados, compatibles con bus del ordenador para excitar visualizadores LED o cristal líquido de frecuencia, número de canal o posición de control. Este artículo también describe como los circuitos integrados pueden proporcionar control digital de funciones analógicas, tales como control de volumen, equilibrio y tono.

Parte 5 – Conmutadores y filtros de audio controlados por c.c.

Este artículo describe el empleo de dos nuevos circuitos integrados para proporcionar conmutacion estática de señales en un preamplicador de audio. Puesto que los circuitos integrados incorporan un amplificador operacional de ganancia-unidad en cada via de señal, también pueden ser empleados para construir filtros activos que eliminen los ruidos de aguja, ronquidos y frecuencias infrasónicas durante la reproducción de grabaciones.

TDA1060 – Un circuit de commande complet pour alimentations à découpage

Cet article décrit comment un seul circuit intégré peut assurer toutes les fonctions de commande et de protection que nécessitent les alimentations à découpage (switched mode power supply) dans des applications à l'informatique et aux télécommunications, de puissance comprise entre 10 W et 5 kW.

TDA1060 – Circuito de control para fuente de alimentación conmutada

Este artículo describe como se utiliza un solo circuito integrado para proporcionar el completo control y protección que requieren las fuentes de alimentación conmutadas en aplicaciones tales como alimentaciones para ordenadores y telecomunicaciones con potencias comprendidas entre 10 W y 5 kW.

Pollution du secteur causée par les appareils domestiques

1ère partie – Définitions et normes

La régulation de puissance à l'aide de dispositifs état solide modernes tels que thyristors et triacs est susceptible de causer de graves perturbations de l'alimentation secteur. Le présent article considère les principaux types de perturbations causées par les appareils domestiques, c'est à dire la distorsion harmonique, le scintillement et les effets de courant continu. L'article présente la norme CENELEC EN 50 006 et en examine les propositions sur la teneur maximale en harmoniques et la dose de scintillement.

Polución de la red causada por aplicaciones domésticas

Parte 1 – Definición y normas

El control de potencia utilizando modernos dispositivos de estado sólido, tales como tiristores y triacs, puede pertubar seriamente la alimentación de red. Este artículo considera los principales tipos de perturbaciones producidas por aplicaciones domésticas: distorsión armónica, parpadeo y efectos de c.c. Se describe la norma CENELEC EN 50 006 y se analizan sus propuestas sobre máximo contenido armónico y dosis de parpadeo.

Des thyristors et des triacs fiables sous enveloppe de plastique TO-220

De nouvelles méthodes de fabrication améliorent nettement la conformité aux spécifications et la fiabilité de thyristors et triacs sous enveloppe de matière plastique. Le collage or-eutectique donne une résistance thermique faible et stable et l'isolation par diffusion isole complètement les bords de la puce, ce qui permet le contrôle sur disque et protège contre les dégradations au cours du découpage et de la fixation. Parmi les améliorations que révèlent les essais d'endurance, un faible étalement des courants de fuite et la rareté exceptionnelle des effets de fatique thermique méritent d'être mentionnés.

Tiristores y triacs fiables en cápsula de plástico TO-220

Nuevos métodos de fabricación mejoran significativamente la conformidad y fiabilidad de tiristores y triacs encapsulados en plástico. La unión eutéctica da baja y estable resistencia térmica y el aislamiento de difusión aisla completamente los bordes de la pastilla, permite comprobación sobre placa y protege contra daños durante la separación y soldadura de las patillas. Entre las mejoras puestas de manifiesto por los ensayos de duración de vida, son notables la baja dispersión de corriente de fuga y la excepcionalmente baja incidencia de efectos de fatiga térmica.

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