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Contents

The 'office of the future' is virtually with us today — electronic mail is making its entry, word processors write our letters, and computers converse with each other; not with people yet, but as one of the articles in this issue shows — that time is not far off. Nonetheless, however much computers take over the drudgery of office tasks they are not likely to replace the essential personal contacts of daily business life. However much we trust computers, as social beings we place more trust in the people we have met and spoken to. The telephone, therefore, is here to stay. In a number of recent issues we have drawn attention to the advances made in electronic telephones and telephone exchanges. Again in this issue we deal with two-tone dialling ICs which speed up our essential telephone traffic.

Engineers who hesitate to tackle problems involving magnetics will welcome this new approach to smoothing-choke design. The magnetic properties of the core material are already taken into account in easy-to-use charts.

Improved method of power-choke design

J. JONGSMA and L. BRACKE

A power smoothing choke which is to carry a significant direct current component or to have a well-defined inductance is usually wound on a core whose magnetic circuit includes an air gap. The reluctance (magnetic resistance) of this air gap reduces the effective permeability of the core: either to increase the ampere-turns at which saturation occurs, or to reduce the effect of variations in the permeability of the core material on the inductance of the choke.

The traditional route to the design of a choke with a gapped core involves the use of Hanna curves, or some derivative of them. (Ref. 1, 2, 3). This design route has a number of disadvantages and limitations. Initial core selection is uncertain and designs may have to be made using a number of cores before the optimal solution is found. The design procedure involves considerable calculation and iteration, and the effects of changes in core operating conditions and mechanical tolerances, especially on the airgap, are not readily predicted.

To simplify the design of power chokes using Ferroxcube grade 3C8 cores, we have devised a method based on computer-generated charts. The first step in the design is the selection of a suitable core: this selection usually proves to be final. The published data (Ref. 4) for each core includes a further chart that replaces the Hanna curve and which is used for graphical design of the choke.

DESIGN METHOD

Ferroxcube 3C8 manganese-zinc ferrite is established as an excellent material for power transformer and choke cores operating at ultrasonic frequencies, especially those in switched-mode power supplies (SMPS). The new core selection and design charts greatly simplify the design of such chokes.

Starting with the peak current I_M that the choke is required to pass without saturating the core, and the minimum inductance required L_{min}, the designer obtains directly all the information necessary for the construction of the choke. Core size, spacer thickness, number of turns, and winding geometry are derived by straightforward procedures. Of especial interest to those engineers to whom the subject is a black art: the magnetic properties of the core do not enter into the process at all.

The design method allows for ratios of alternating to direct current from small (smoothing chokes) to large (push-pull converter chokes). Parameter spreads due to manufacturing and temperature variations are taken into account in the construction of the design charts. The design procedures allow for spacer tolerances.

Core operating conditions

The selection and design charts are constructed for cores of Ferroxcube 3C8 operating at a hotspot temperature of 100 °C. Operation at lower temperatures leads neither to core saturation nor to inductances lower than L_{min}. The design peak flux density B_M is 0.32 T; however, the charts can be used for a lower value by designing for a peak current $0.32 I_M/B_M$. (Symbols used in this article are listed and defined in the Table; symbols for currents are illustrated by Fig.1. Note that in the equations the unit of frequency is kHz, *not* Hz; and the unit of length, mm. Some constants in the equations are based on these units.)

Applications

For the purposes of the new design method, applications are divided into three classes:

I $I_{ac}/I_0 < 0.3$
as in smoothing chokes, and converter chokes for fly-back-type SMPS, where the core flux density remains above zero.

II $I_{ac}/I_0 \approx 1$
as in chokes where the operating flux density returns periodically to zero. This is the case with flyback converters of the ringing-choke type.

III $I_{ac}/I_0 > 2$
as in converter chokes for push-pull-type SMPS, and fluorescent-lighting ballast chokes, where excitation is symmetrical.

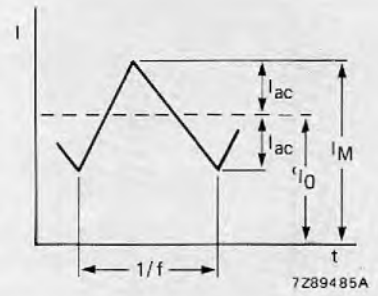

Fig.1 Symbols for choke current used in the text. (See also the Table)

Definition of symbols used

symbol	unit	definition
A_L	H	induction factor L/N^2
b_w	mm	winding (layer) breadth
B_M	T	peak flux density
d	mm	nominal wire diameter
d_o	mm	overall wire diameter
f	kHz	frequency
f_e	kHz	effective frequency (see text)
F_R	–	a.c. resistance factor R_{ac}/R_{dc}
h	mm	thickness of foil conductor
H	mm	winding height
H_a	mm	available winding height
i	mm	thickness of interleaving
I_e	A	r.m.s. current at full load
I_0	A	d.c. component of current at full load
I_{ac}	A	a.c. component of current at full load
I_M	A	peak value of current at full load
L	H	inductance
N	–	number of turns in a winding
p	–	number of layers
P_W	W	winding loss
R_{ac}	Ω	a.c. resistance
R_{dc}	Ω	d.c. resistance
s	mm	spacer thickness

Note: subscript id means 'ideal' value.

In class III applications, the limiting factor in a design is core loss rather than core saturation. Operation at a permissible level of core loss usually entails reducing the peak flux density in the core; the amount of the reduction depends on operating frequency. The treatment given to class III designs here generally yields satisfactory results.

CORE SELECTION

The design charts in Ref.4 are supplemented by three core selection charts. Each chart covers a group of core types according to shape:

- UU and UI cores (Fig.2), comprising respectively two U cores or a U and an I core, generally give designs with the lowest ferrite cost. However, they are not available complete with coil formers.
- EE cores, a pair of E cores, may be preferable where other considerations dominate, such as the availability of coil formers.
- EC cores, although designed primarily for transformers, might perhaps be chosen because their use for both transformers and chokes in the same equipment simplifies parts stocking.

Figure 2 shows the core selection chart for UU and UI cores, examples of which are shown in Fig.3.

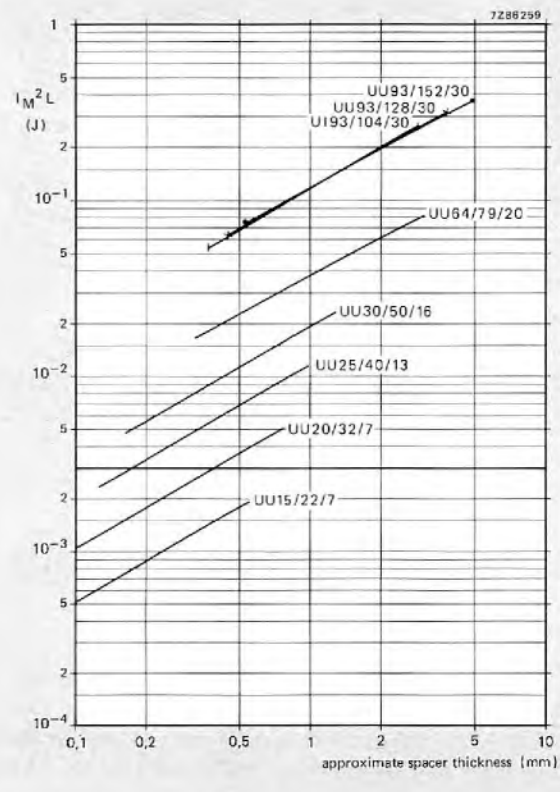

Fig.2 Selection chart for U cores as given in Ref.4

Fig.3 A selection of cores in Ferroxcube grade 3C8 ferrite

Selection procedure

The selection curves are used to select a suitable core for the intended application. A full design can then be made using the design chart in the core data sheet with confidence that the result will be useful. The selection charts are used as follows:

- Knowing the value of peak choke current I_M and the minimum inductance required L_{min}, calculate the value of $I_M^2 L_{min}$.
- Choose, at least provisionally, the shape of core (UU/UI, EE, or EC) based on the considerations in the previous paragraph. Draw on the appropriate selection chart a horizontal line $I_M^2 L_{min}$. For class III designs use a value of $0.1 f I_M^2 L_{min}$, where f is the operating frequency in kHz.
- A core whose curve intersects this horizontal line can be used for the application. The spacer thickness corresponding to the intersection is, however, only an indication of the final value.

Effect of core size

Where, as is usual, more than one core could be used, the final choice may be governed by the consideration that operation near the right-hand end of the curves carries the risk of overheating. Moreover, selection of a larger core will generally result in a more conservative, efficient design than one based on a core that is only marginally large enough.

SPACER THICKNESS AND NUMBER OF TURNS

In the data sheet for the type of core selected, refer to the chart giving $(I_M^2 L)_{max}$ and A_L as functions of spacer thickness. (Note: A_L for these power cores is the induction factor in henrys.)

The charts contain a pair of curves of $(I_M^2 L)_{max}$ and A_L for each of the three application classes. The design chart for the UU64/79/20 is given as Fig.4. In the design procedure, use the pair of curves of the appropriate class of application, as follows:

1. On the chart, draw again the horizontal line $I_M^2 L_{min}$ (or $0.1 f I_M^2 L_{min}$ for class III applications) as in the selection procedure. The working point of the core must lie above this line and below the $(I_M^2 L)_{max}$ curve for the core. In Fig.5, that is between lines SQ and SP.
2. Select a suitable spacer, of nominal thickness s. Draw vertical lines s_{min} and s_{max} on the chart, where $s_{max} - s_{min}$ is the tolerance field on the thickness of the spacer and the associated adhesive films. (Epoxy adhesive films vary in thickness from about 10 μm to about 20 μm.) Ensure that the horizontal distance between the intersection and s_{min} (a in Fig.5) is greater than the distance from s_{min} to s_{max} (b in Fig.5).

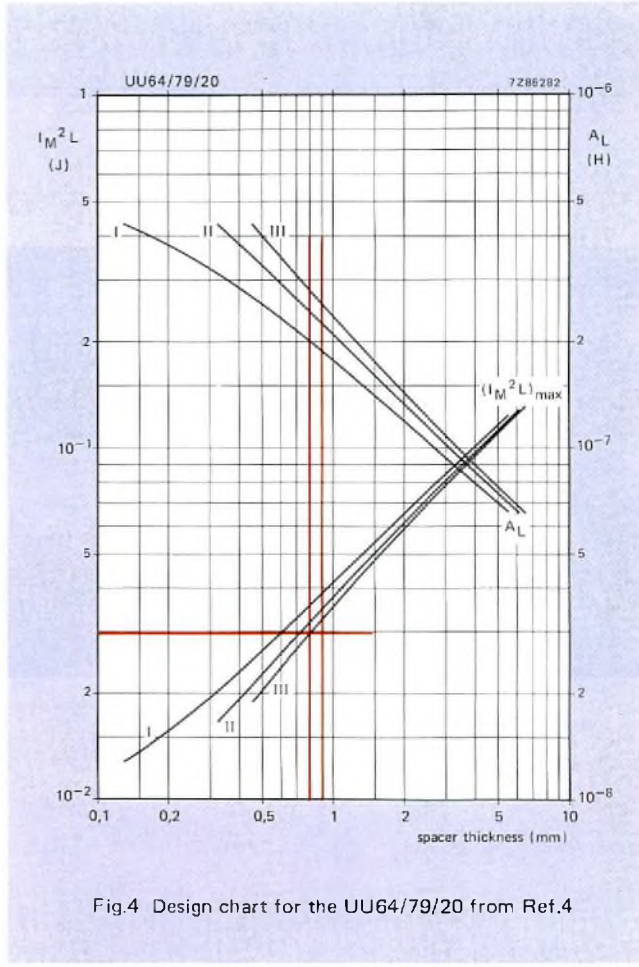

Fig.4 Design chart for the UU64/79/20 from Ref.4

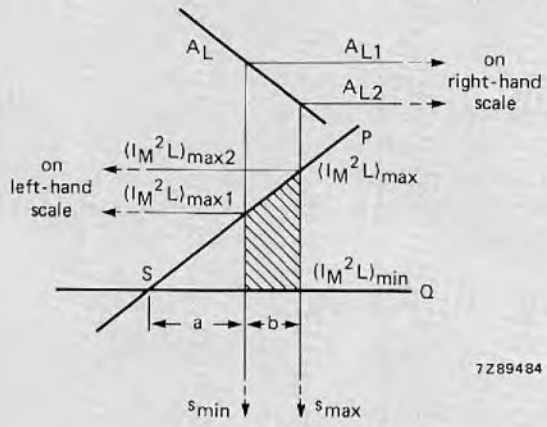

Fig.5 Construction for graphical design of chokes using the new design charts

3. For s_{min}, read values of $(I_M^2L)_{max\,1}$ and $A_{L\,1}$ from the chart. To avoid saturation the maximum number of turns allowed is

$$N_{max} = \sqrt{\frac{(I_M^2L)_{max\,1}}{I_M^2A_{L\,1}}} \qquad (1)$$

Note: the upper left-hand corner of the shaded area in Fig.5 is the most critical point regarding number of turns and core saturation.

4. For s_{max}, read the value of $A_{L\,2}$. The minimum number of turns required to achieve L_{min} is then

$$N_{min} = \sqrt{\frac{L_{min}}{A_{L\,2}}} \qquad (2)$$

Note: the lower right-hand corner of the shaded area is the most critical for number of turns and L_{min}.

5. Select an integral number of turns N between N_{min} and N_{max}.

Note: If 'a' was taken to be only marginally greater than 'b' (Fig.5), the design attempt might fail since such an integer would not exist. Making $a < b$ makes $N_{max} < N_{min}$.

6. Establish the winding geometry using the winding-design procedure in the next section.

WINDING DESIGN

The losses due to eddy-currents in a winding carrying a.c. increase rapidly with conductor size (as d^4 for wire), but resistive losses in a conductor decrease with increasing size (as d^{-2} for wire). It follows, therefore, that there must be a frequency-dependent 'ideal' conductor size at which losses are minimum. (This is discussed fully in Ref.5.) This sets the upper limit to conductor size; there is no reason to increase losses by using a thicker conductor. The use of a thinner conductor is sometimes tolerable (low current density) or necessary (inadequate space).

The procedures that follow allow the ideal number of layers and wire size, or the thickness of strip, to be determined for chokes with an operating-current waveform similar to that shown in Fig.1. They also indicate the course of action in the event of the available winding window being insufficient to accommodate the ideal winding.

Copper conductors are assumed here and the operating temperature is taken to be 100 °C, so that conductor resisitivity is 1/45 $\Omega mm^2/m$ (30% higher than that at 20 °C). Symbols used are defined in the table and Fig.1.

Effective frequency and effective current

To allow for the effect of waveform on eddy-current losses in the choke windings, it is necessary to convert actual frequencies and currents to effective values. For sinusoidal currents, the effective frequency f_e is equal to the actual frequency f. For small amounts of waveform distortion, and small d.c. components, f_e can still be taken as equal to f. For the waveform of Fig.1, and provided that the rise and fall times are between 15% and 85% of the repetition period,

$$f_e = \frac{1.3f}{\sqrt{1 + 3(I_0/I_{ac})^2}} \qquad (3)$$

In designs for class I applications f_e may be only a few kilohertz. Eddy-current effects are then negligible so that windings can be designed as if they are to carry d.c. only. Remember to use the correct value for d.c. resistivity.

For the waveform of Fig.1, the effective current I_e is given by

$$I_e^2 = I_0^2 + I_{ac}^2/3$$

For sinusoidal currents with a significant d.c. component, however,

$$f_e = \frac{f}{\sqrt{1 + 2(I_0/I_{ac})^2}}$$

and

$$I_e^2 = I_0^2 + I_{ac}^2/2$$

where I_{ac} is the amplitude of the a.c. component.

Multi-layer wire windings of solid, round wire

In the following design procedure, it is assumed that all layers have the same breadth. However, where the number

of turns in the winding cannot be divided into the ideal number of layers, a difference of one turn per layer is permissible.

1. The ideal wire diameter is

$$d_{id} = 2.6 \left(\frac{b_w}{Nf_e} \right)^{1/3}$$

2. Select the nearest standard wire size (for d and d_o) from a wire table such as that for IEC grade 1 winding wires.
3. The ideal number of layers is now

$$p_{id} = \frac{N}{b_w/d_o - 1}$$

Note: this expression is valid only for d_o from step 2.

- If $p_{id} \geqslant 1.5$ and the current density in wire d_{id} is excessive, make a new design using a larger core.
- If $p_{id} \leqslant 1.5$, also consider a foil or strip winding.
- If $p_{id} \leqslant 1$, the expression for d_{id} in step 1 is not valid: go to the single-layer winding procedure.

Find p by rounding p_{id} to the next highest integer. This rounding increases the spacing between turns.

4. The required winding height is

$$H = p(d_o + i)$$

5. If H exceeds the available height H_a, or if current density is low:
   - reduce p by one layer
   - select the thickest wire for which $d_o \leqslant pb_w/(N + p)$,
   - repeat from step 4, even if p = 1.
6. $F_R = 1 + \frac{1}{2}(d/d_{id})^6$.

   Note: $F_R = 1.5$ for $d = d_{id}$; when $d < 0.7d_{id}$, $F_R \approx 1$.
7. $P_W = I_e^2 R_{ac} = I_e^2 F_R R_{dc}$.*

Single-layer windings of solid, round wire

This design procedure is to be used only when p_{id} calculated in step 3 of the previous section comes out as equal to or less than unity.

1. Select the thickest wire for which $d_o \leqslant b_w/(N + 1)$.
2. $F_R = 0.33\, d\, f_e^{\frac{1}{2}} N/(N + 1)$, only if $p_{id} \leqslant 1$ in step 3 of the last section.
3. $P_W = I_e^2 R_{ac} = I_e^2 F_R R_{dc}$.*

* The d.c. resistance of copper wire is $0.0283/d^2$ Ω/m at 100 °C.

Bunched (Litz) wire windings

Eddy-current effects in bunched-conductor (or Litz-wire) windings are negligible and, thus, no special design procedure is required. Conductors of this type are not, however, necessarily the complete solution: their packing factor, and, consequently, winding thermal conductivity are both low. They might be an attractive alternative where the ideal solid-conductor winding fills less than half the available height. The resistance of bunched conductors, like that of solid conductors, is 30% higher at 100 °C than at 20 °C.

Foil or strip windings

Chokes for high-current, low-voltage SMPS often use windings of strip or foil conductor. The width b_w of the strip is equal to the available winding width.

1. $h_{id} = \frac{3.1}{\sqrt{(Nf_e)}}$
2. $h_{min} = 0.8 \frac{h_{id}}{\sqrt{N}}$
3. $h_{max} = \frac{H_a}{N} - i$

   Choose a value for i that suits a strip of thickness about H_a/N. If $h_{max} < h_{min}$, try a wire winding.
4. Select a strip of thickness h such that $h_{min} \leqslant h < h_{max}$. Aim for $h = h_{id}$.
5. $F_R = 1 + \frac{1}{3}\left(\frac{h}{h_{id}}\right)^4$

   When $h = h_{id}$, $F_R = 1.33$; when $h < 0.6\, h_{id}$, $F_R \simeq 1$.
6. $P_w = I_e^2 R_{ac} = I_e^2 F_R R_{dc}$.

   Note: d.c. resistance of copper strip,is $1/(45b_w h)\Omega$/m at 100 °C.

DESIGN EXAMPLE

A choke of 30 mH minimum inductance is required for a peak current of 1 A at 30 kHz with a waveform as shown in Fig.1. $I_{ac}/I_0 = 0.1$, so this is a class I design.

Core selection

Cost is important and quantities justify customised coil formers, so a UU core is selected.

The value of $I_M^2 L_{min} = 3 \times 10^{-2}$ J. A horizontal line of this value drawn on the UU core selection chart intersects the curve for the UU 64/79/20 core at a spacer thickness of about 0.7 mm.

Number of turns and spacer thickness

Another horizontal line for $I_M^2 L_{min} = 3 \times 10^{-2}$ J drawn on the design chart for the UU64/79/20 core, Fig.4, intersects the $(I_M^2 L)_{max}$ curve for class I at a spacer thickness of 0.6 mm. A resin-bonded paper sheet of 0.9 mm thickness with a tolerance of −0.1 mm is available. Adhesive thickness is between 0.01 mm and 0.02 mm, so the final spacer thickness could be 0.81 to 0.92 mm. Vertical lines of these values are drawn on the design chart. The condition given with reference fo Fig.5, that a > b, is satisfied.

From Fig.4, $(I_M^2 L)_{max\,1} = 0.036$ J and $A_{L1} = 2 \times 10^{-7}$ H. Thus, from Eq.(1),

$$N_{max} = \sqrt{\frac{0.036}{1 \times 2 \times 10^{-7}}} = 424.26 \text{ turns}$$

$A_{L2} = 1.9 \times 10^{-7}$ H, so the minimum number of turns is, from Eq.(2),

$$N_{min} = \sqrt{\frac{0.03}{1.9 \times 10^{-7}}} = 397.36$$

Since N_{max} is, as it should be, greater than N_{min}, the design is successful so far and a number of turns can be selected between these limits.

Winding design

The effective operating frequency for the core is given by Eq.(3),

$$f_e = \frac{1.3 \times 30}{\sqrt{1 + 3\,(0.1^{-2})}} \simeq 2.25 \text{ kHz}$$

At this effective frequency, eddy-current effects can be neglected, and the winding can be designed to fit the space available, allowing for the coil former wall thicknesses.

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A new integrated voice synthesiser uses formant coding to reduce the required bit rate. It incorporates an 8th-order filter with three programmable formant frequencies and four programmable bandwidths. The circuit uses dynamic NMOS technology, has a 4 kHz speech bandwidth, and can easily be interfaced with most 8-bit microcomputers.

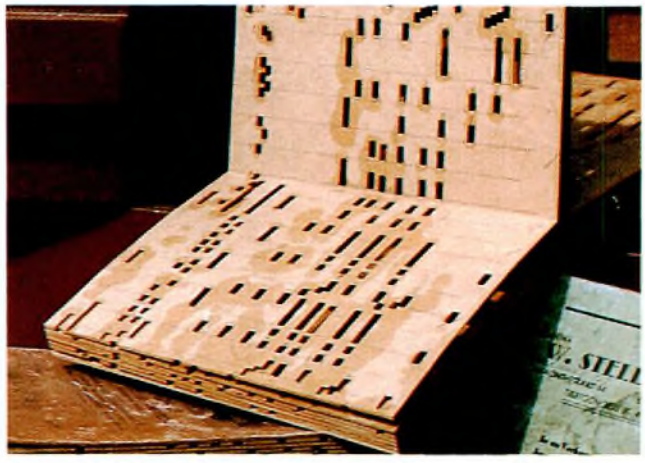
Integrated voice synthesiser

H. E. VAN BRÜCK and D. J. A. TEULING

Until now, communication between machine and man has mainly been in sign language from visual displays, audible communication being restricted to cries of alarm emitted by beepers, hooters, bells and buzzers. Voice communication has been impractical because analog storage of speech required the use of moving parts which unduly prolonged the retrieval time, and digital storage of speech required an enormous number of bits. The development of speech synthesis techniques has changed this situation by reducing the required bit-rate for digital speech synthesis by at least one order of magnitude so that it is now economically feasible to open a new wideband voice channel between machine and man. Such a channel is provided by our newly developed, totally digital integrated voice synthesiser MEA8000.

Figure 1 shows the stages of various methods of speech storage. In stages 1 and 2, (waveform coding) the actual speech waveform is stored but the digital approach (stage 2) requires a very large memory. In stages 3 and 4, a very much smaller memory is required because redundant speech information is eliminated and only the essential characteristics of the speech sounds are stored. This voice 'score' is then used to control a voice generating instrument (speech synthesiser). In stage 4, the method used in the MEA8000, formant coding allows further reduction of the required bit rate.

To clarify the fundamental principles of speech synthesis, consider the following analogy. The human voice mechanism shown in Fig.2 can be thought of as a voice sound generating instrument analogous to a music generating instrument such as a Dutch street organ. To digitally store the sound from the street organ would require a very large number of bits per second, but it is controlled at a much slower rate by a musical 'score' stored on linked punched cards. This reduced information rate is possible because the stored data does not have to include information regarding the nature (timbre) of the sound which is characteristic of the instrument.



To digitally store the sound output from this Dutch street organ would require a very high bit rate, but it is controlled, at a much slower rate, by a musical 'score' stored on linked punched cards

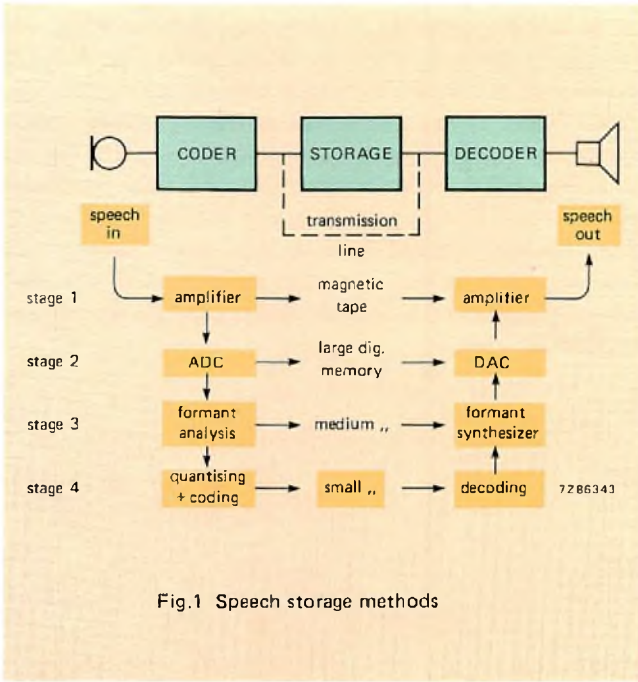


Fig.1 Speech storage methods

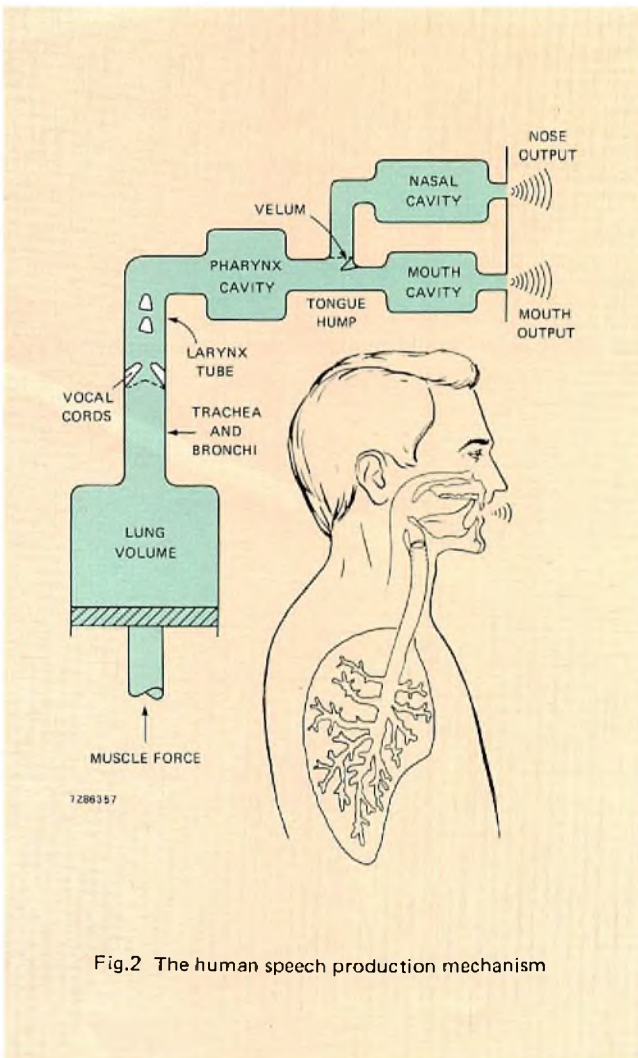


Fig.2 The human speech production mechanism

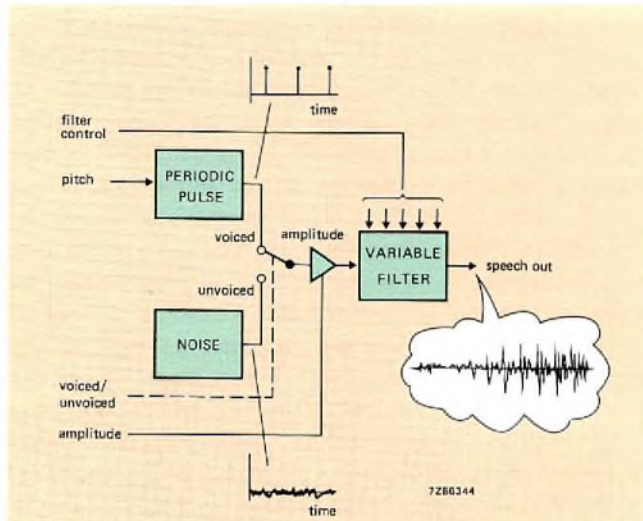


Fig.3 Simple electronic model of the human speech production mechanism

The required bit rate for a voice generating instrument (speech synthesiser) can be similarly reduced by extracting the voice 'score' which contains only the control information for the voice producing instrument which, since it is an electronic model of the human voice mechanism, will produce the required sounds. Figure 3 is a block diagram of a simplified electronic model of the human speech reproduction mechanism. A combination of a periodic signal, representing the pich of the original speech, and an aperiodic signal, representing the unvoiced sound in the speech, is fed to a variable filter comprising four resonators, via an amplifier which controls the amplitude. The resonators model the sound in accordance with the formants in the original speech. Each resonator is controlled by two parameters, one for the resonant frequency and one for the bandwidth. The information required to control the model is:

- pitch
- amplitude
- voiced/unvoiced

} excitation source (vocal cords)

- filter control — spectrum shaping (vocal tract)

A good replica of the original speech is obtained by periodic updating of this control information.

One method of obtaining the control information is to use linear predictive coding (LPC) in which the speech waveform is sampled and the weighted sum of N previous samples is made to conform to the actual sample by adjusting the weighting coefficients. These weighting coefficients can be used during synthesis to define the response of a digital filter which shapes the voice frequency spectrum. The predictor order N should be at least eight to obtain telephone quality speech. From the eight LPC weighting coefficients, it is possible to extract the central frequencies and bandwidths of the four voice spectrum formants which, for

normal speakers, represent the vocal tract resonances at frequencies up to 4 kHz. In the method used in the MEA8000, formant coding allows further reduction of the required bit rate. The information derived from the coding process then consists of four bytes of speech code which determine the speech synthesiser parameters, and therefore the speech output, during a time slot called a speech frame. The duration of the speech frame must be long enough for it to contain a sufficient number of speech samples to allow the speech parameters to be calculated, yet short enough to isolate changes of the speech parameters. In the MEA8000, the duration of the speech frame is programmable and can be set to 8, 16, 32 or 64 ms. In practice, speech coding is a fairly complex process during which digitised speech samples from a recorded voice are analysed by a computer to produce the speech code. This is applied to the synthesiser which translates it into the required pitch, amplitude, voiced/unvoiced and filter control information. At present, speech coding for the MEA8000 is a service that can only be provided by the synthesiser manufacturer.

The main features of the MEA8000 are:

- 4 kHz speech bandwidth
- can be directly interfaced with most 8-bit microcomputers
- melodies can be generated
- bit-rate from 500 to 4000 bits per second
- two operating modes
- 8th-order digital filter with three programmable formant frequencies, one fixed formant frequency and four programmable formant bandwidths
- dynamic NMOS technology
- 24-pin plastic DIL package
- typical current consumption, 30 mA from a 5 V supply
- minimal external audio filter requirement.

INTERNAL STRUCTURE OF THE MEA8000

Formant synthesiser

Investigations at the Institute for Perception Research (IPO) in Eindhoven, The Netherlands have revealed that four formant frequencies can adequately model the voice spectrum. Moreover, the highest of the four frequencies can be constant. Figure 4 is a block diagram of the MEA8000. As shown in Fig.5, the excitation source and the four formant resonators actually consist of a 16-bit multiplication and addition unit which calaculates the voice samples at a rate of 8 kHz. The synthesiser is controlled by eleven 14-bit parameters representing pitch, pitch increment (rate of pitch change) for voiced operation or noise selection for unvoiced operation, amplitude, four filter centre frequencies and four filter bandwidths.

To simplify decoding, we have used three multipliers in the digital formant filters as shown in Fig.6 so that the bandwidth and centre frequency each determine only one filter parameter and the speech codes can be decoded in accordance with simple one-dimensional tables in the parameter ROM. It is also feasible to use only two multipliers for the filters as shown in Fig.7. Parameter P would then, however, depend on both the centre frequency and the bandwidth so that the ROM would have to contain a two-dimensional table and its storage capacity would have to be quadrupled.

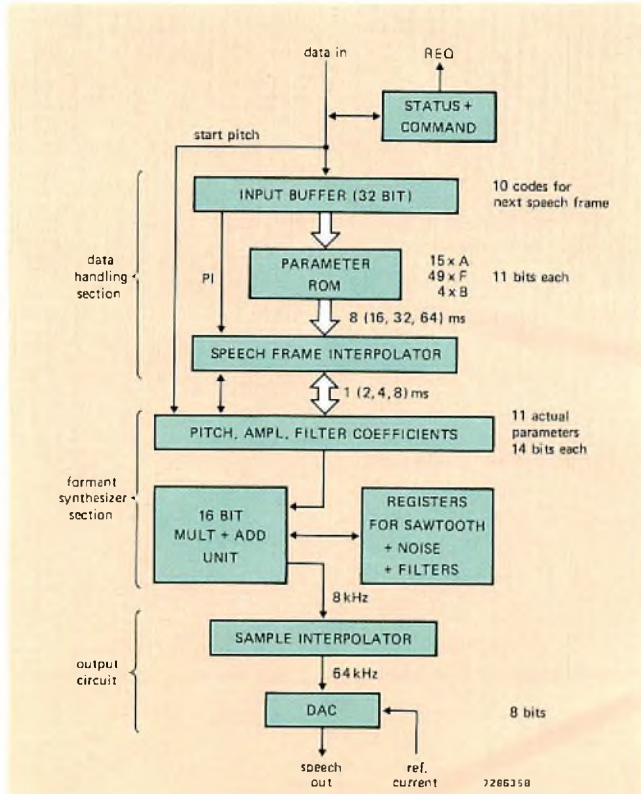


Fig.4 Block diagram of the MEA8000

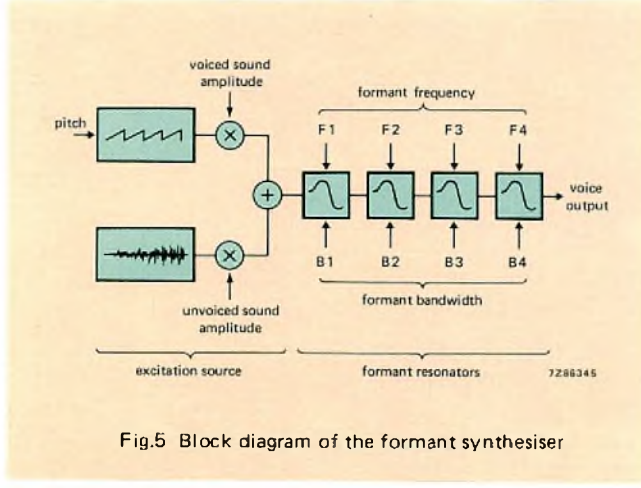


Fig.5 Block diagram of the formant synthesiser

It is useful to incorporate facilities for generating non-voice sounds such as melodies. One method of doing this is to program the pitch. The method we have used, which in our opinion gives superior results, is to excite a high-Q resonator with random noise. The high-Q resonator is simulated by allocating the same centre frequency to formant filters 1 and 2. As shown in Table 4, the range of common centre frequencies available for these two filters is almost one and a half octaves ranging from 440 Hz (note A) to 1047 Hz (note C^2).

Output circuit

The 16-bit speech samples from the formant synthesiser section are rounded to 8-bits before being converted into an analog signal by the output circuit. The output circuit shown in Fig.8 combines pulse-width and current modulation techniques to implement a single circuit which performs the dual functions of a simple 8-bit DAC and a linear interpolator which generates seven additional samples between each 8 kHz sample from the formant synthesiser section. The sample rate of the DAC is therefore 64 kHz which is far above the audible frequency range thus allowing the use of a very simple external audio filter.

Input data handling

Since the human vocal tract is a mechanical system, its characteristics change quite slowly during the formation of voice sounds. It has been found that the speech synthesiser control parameters can be adequately represented if they are updated once every few tens of milliseconds with linear interpolation during the intervals to ensure a smooth change over from one set of characteristics to the next. In the MEA8000, the updating period (speech frame) can be set to 8, 16, 32 or 64 ms.

The speech code from a microcomputer is passed along a data bus to the MEA8000 as a block of four bytes for each speech frame. Each code (excluding the start pitch) is loaded during the previous speech frame and stored in a 32-bit input buffer before being translated into control parameters by the parameter ROM and speech frame interpolator.

The output signal is derived from two parallel-connected open-drain pulse current sources. One of the current sources generates the reference current (I) and the other generates sixteen times the reference current (16I). The direct reference current I is externally applied to the integrated circuit. The four least-significant bits of the 8-bit sample from the interpolator control the duration of the pulse from the I current generator and the four most-significant bits control the duration of the pulse from the 16I current generator. In this way, 256 average output current levels can be generated.

To prevent limited rise and fall times affecting the average output current, both current sources are turned off for at least two clock periods and on for at least three clock periods during each 64 kHz sample. Figure 9 shows a large number of superimposed output pulses for a variety of amplitudes and durations. Both amplitude modulation and pulse-width modulation are evident.

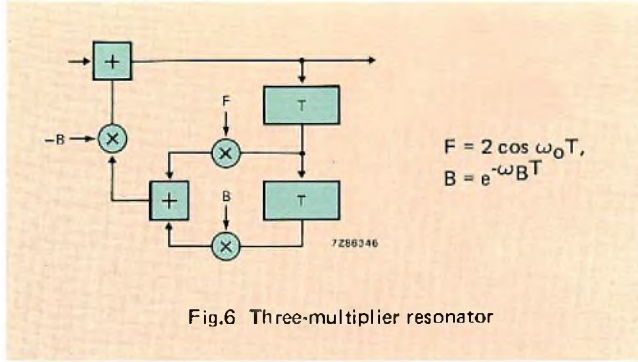


Fig.6 Three-multiplier resonator

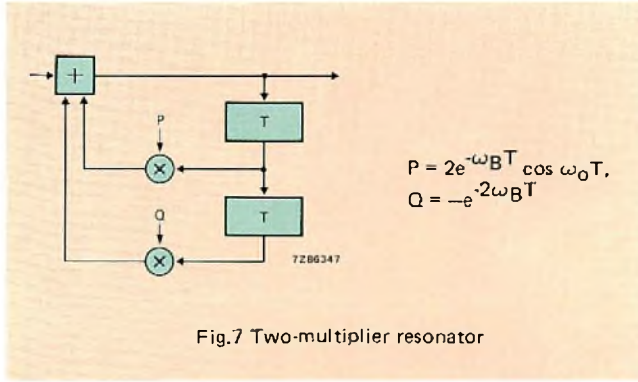


Fig.7 Two-multiplier resonator

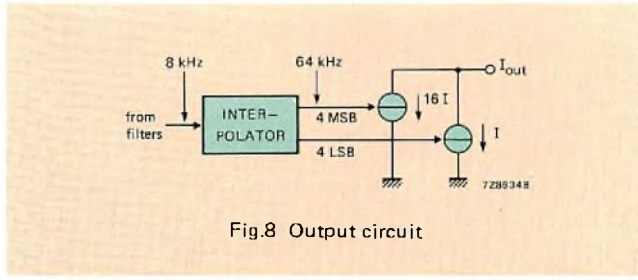


Fig.8 Output circuit

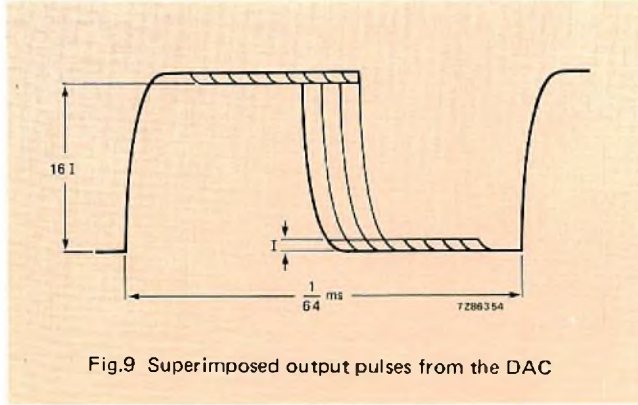


Fig.9 Superimposed output pulses from the DAC

THE MEA8000 INTERFACE

Timing

System timing is determined either by clock pulses from an internal oscillator controlled by an external 3.84 MHz to 4 MHz crystal, or by externally-applied clock pulses within the same frequency range at a TTL-compatible input. Pulses at one-third of the clock frequency are also available at an output pin.

Control interface

The fact that the MEA8000 is a microcomputer peripheral is reflected in the control connections as shown in the interface examples given in Fig.10. Typical control software requires between 50 and 100 bytes of machine code. The functions of the control and data inputs to the MEA8000 are:

- $\overline{CE}$ enables the circuit (active LOW)
- $\overline{W}$ controls the write operation (active LOW)
- $\overline{R}/W$ controls the read operation (active LOW)
- AO addresses the input buffer (AO = 0) or the command register (AO = 1) during a write operation
- D0-D7 data bus. Line D7 is bidirectional to allow the status bit to be read out.

Control inputs $\overline{CE}$, $\overline{W}$ and $\overline{R}/W$ can be used in many combinations to allow simple interfacing with a wide variety of microprocessors and microcomputers. The control input truth table is given in Table 1. Figure 11 and 12 show two ways to use the control inputs to interface the MEA8000 to most popular microcomputers.

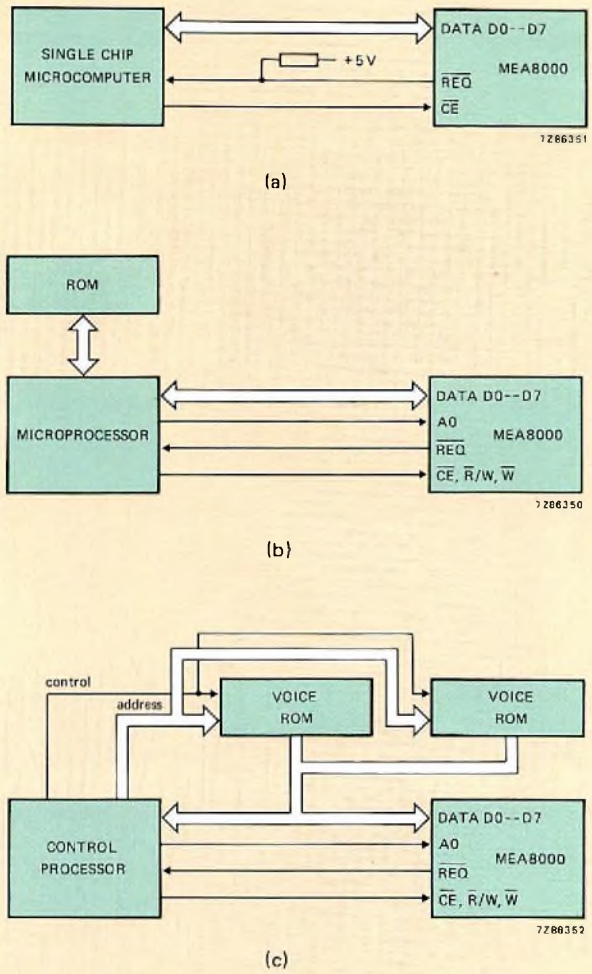


Fig.10 Typical interface between the MEA8000 and control devices
(a) very simple system using a single-chip microcomputer with an on-board voice ROM
(b) MEA8000 as a microprocessor peripheral
(c) system using more than one voice ROM

TABLE 1
Control input truth table

$\overline{CE}$	$\overline{W}$	$\overline{R}/W$	A0	operation
0	0	1	0	write data
0	0	1	1	write command
0	X	0	X	read status
0	1	1	X	three-state data bus
1	X	X	X	

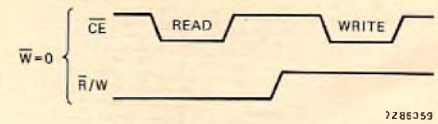


Fig.11 Chip enable (CE) used as a read or write strobe

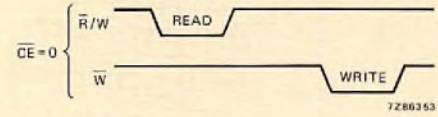


Fig.12 Separate read and write strobes

Command word

The command word is written into the MEA8000 via data bus lines D4-D0 as shown in Table 2 and Fig.13. Bits D1 and D0 of the command word enable the $\overline{REQ}$ output which carries the status bit to signal a request for the next byte of speech code. Bit D4 silences the synthesiser immediately but the mode setting is not affected. Bits D3 and D2 select one of the following modes of operation:

– SLOWSTOP. After power-on reset, the circuit is in this mode and the $\overline{REQ}$ output is disabled. The synthesiser is silent. Voice output commences upon receipt of five bytes of speech code (start pitch plus first speech frame). If the next speech frame is written-in before the current speech frame ends, the voice output continues. If the next speech frame is not received before the current speech frame ends, the synthesiser repeats the last speech frame at a decreasing amplitude and then goes silent. Voice output resumes after five bytes of speech code (start pitch plus one speech frame) have been written-in.

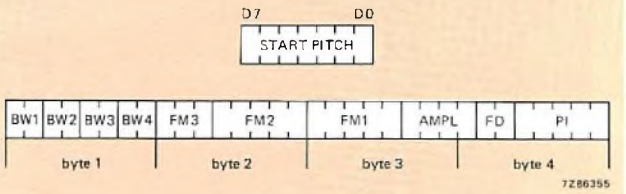


Fig.13 Data format for the MEA8000

– CONTINUOUS. Operation is similar to that in the SLOWSTOP mode but, if the supply of speech code ceases, the last speech frame is repeated until the STOP command is received or the next speech frame (4 bytes) is written-in.

TABLE 2
Command word bit allocation

D_4	D_3 D_2	D_1 D_0
0 = no action	0X = no action	0X = no action
1 = stop	10 = SLOWSTOP mode	10 = disable $\overline{REQ}$
	11 = CONTINUOUS mode	11 = enable $\overline{REQ}$

D_7, D_6 and D_5 not used.

Data format

During voice output, speech codes are transmitted to the MEA8000 as blocks of four bytes (speech frame) as shown in Fig.13, Table 3 and Table 4. When starting, five bytes are required, the first being interpreted as the starting pitch and the last four being interpreted as the speech frame. Each block of four bytes that follows is also interpreted as a speech frame. Figure 14 shows a header and a start pitch byte followed by twenty-one four-byte speech frames of hexadecimal code for synthesising the word 'stop'.

TABLE 3
Speech code bit allocation

code	bits	parameter
pitch	8	initial value for pitch
FD	2	speech frame duration
PI	5	pitch increment (rate of change) or noise selection
AMPL	4	amplitude
FM1	5	frequency of 1st formant
FM2	5	frequency of 2nd formant
FM3	3	frequency of 3rd formant
FM4	0	frequency of 4th formant (fixed)
BW1	2	bandwidth of 1st formant
BW2	2	bandwidth of 2nd formant
BW3	2	bandwidth of 3rd formant
BW4	2	bandwidth of 4th formant

												——(a)——		(b)	
												00	58	00	31
05	D2	FE	50	0A	D7	FE	70	1A	D8	F5	90	1A	D8	F0	10
44	D9	F8	70	48	DA	FF	B0	08	DB	FF	90	46	DB	FF	02
79	D1	67	0F	AA	CF	9F	7E	BB	AD	96	C1	96	CC	85	BE
46	8F	B4	99	55	D7	24	12	45	B6	13	9E	05	B5	A3	1F
05	B5	A0	00	2A	B3	B0	70	59	B3	E5	B0	2A	B2	DD	B0
19	B2	ED	90												

speech codes

(a) header containing byte count of word code file for microcomputer.
(b) start pitch

Fig.14 Speech codes for the word 'stop'

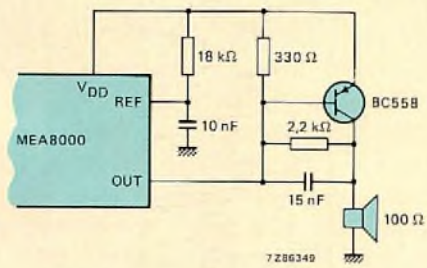
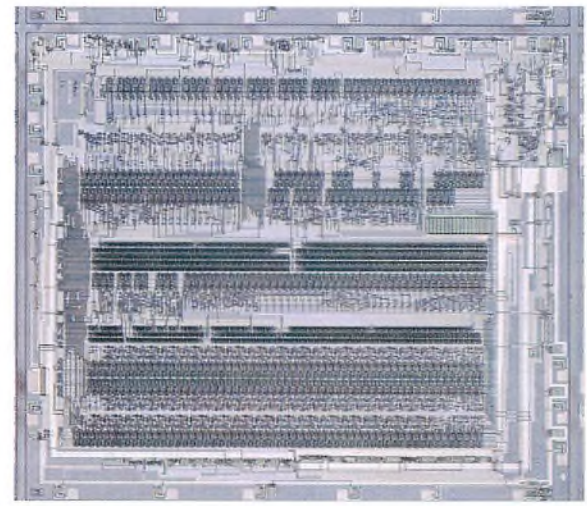


Fig.15 Simple audio output stage



The crystal of the MEA8000

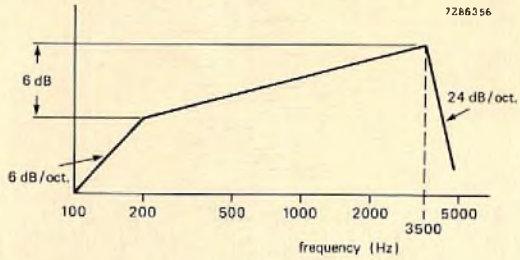
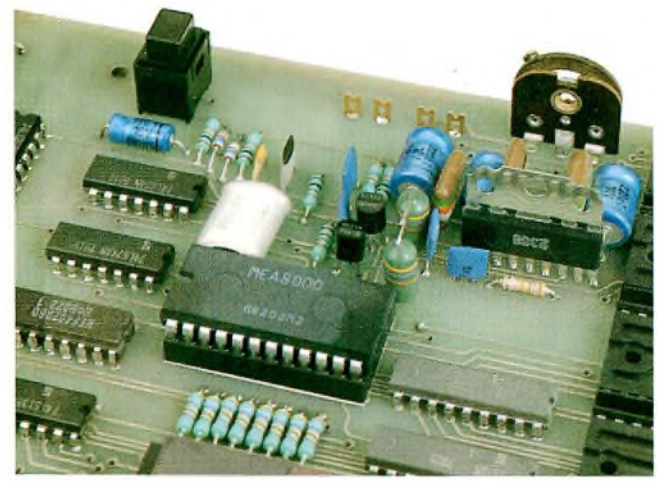


Fig.16 Output filter transfer characteristic for obtaining optimum voice quality



Part of a demonstration board incorporating the MEA8000 voice synthesiser and an integrated output stage TDA1011

Audio output circuit

Figure 15 shows a simple 25 mW audio output stage for the MEA8000. If more output power is required, it can be obtained from an integrated audio power amplifier such as the TDA1011. The best voice quality is obtained if an audio filter with the transfer characteristic shown in Fig.16 is used.

TABLE 4

Speech code parameters when using a clock frequency of 3.84 MHz

binary code	FD (ms)	pitch (Hz)	PI Hz/8 ms	ampl.	FM1 (Hz)	FM2 (Hz)	FM3 (Hz)	BW (Hz)
0	8	0	0	0	150	440	1179	726
1	16	2	1	0.008	162	466	1337	309
2	32	4	2	0.011	174	494	1528	125
3	64	6	3	0.016	188	523	1761	50
4		8	4	0.022	202	554	2047	
5		10	5	0.031	217	587	2400	
6		12	6	0.044	233	622	2842	
7		14	7	0.062	250	659	3400	
8		16	8	0.088	267	698		
9		18	9	0.125	286	740		
10		20	10	0.177	305	784		
11		22	11	0.250	325	830		
12		24	12	0.354	346	880		
13		26	13	0.500	368	932		
14		28	14	0.707	391	988		
15		30	15	1.00	415	1047		
16		32	noise		440	1110		
17		34	−15		466	1179		
18		36	−14		494	1254		
19		38	−13		523	1337		
20		40	−12		554	1428		
21		42	−11		587	1528		
22		44	−10		622	1639		
23		46	−9		659	1761		
24		48	−8		698	1897		
25		50	−7		740	2047		
26		52	−6		784	2214		
27		54	−5		830	2400		
28		56	−5		880	2609		
29		58	−3		932	2842		
30		60	−2		988	3105		
31		62	−1		1047	3400		
⋮		⋮						
255		510						

The frequency of FM4 is fixed at 3500 Hz. The BW (bandwidth) column applies to all four filters. For exact values, the figures in the pitch and pitch increment columns should be multiplied by 1.024.

ACKNOWLEDGEMENTS

The authors wish to acknowledge the contributions made by H. van Essen and H. Wulms of the Philips Research Laboratory who designed the speech processing part of the MEA8000, and by L. Willems, and L. Vogten of the Institute of Perception Research, Eindhoven, who developed the speech analysis software.

Safe, sure, solderless connections, particularly to ribbon cable, can be made quickly and economically by insulation displacement. However, the design of an effective insulation displacement connector is more subtle and complex than its simple appearance suggests.

Insulation displacement connections

J. A. M. ROELOFS and A. SVED

Insulation displacement connections are rather similar to crimped and wire-wrapped connections in the sense that they are gas-tight, high-pressure, solderless connections. The difference lies in the fact that the ID connection is made through the insulation, thus eliminating the need to strip the wire. Although the technique can be used with single wires, the greatest economic benefit of ID connections is realised with flat ribbon cable. Here, up to 64 connections can be made with a single press operation taking no more than a second or so. What is more, the process lends itself readily to automation and machines are available that allow an unskilled operator to perform some 30 jointing operations a minute (i.e., more than 1800 joints if 60 pin connectors are used).

When the ID connection is made the wire is forced between the tines of a fork that parts the insulation, thrusting the bare conductor against the tines (Fig.1). This causes them to open slightly and the combination of pressure and movement deforms the wire until a high-pressure contact has been formed. At first sight it looks simple, but as we shall show later, a sound insight into the elastic and plastic behaviour of materials is needed to design a truly reliable connector system. The core of this article is how such reliable connections can be ensured by thoroughly based investigation of the factors involved in making a high-pressure contact.

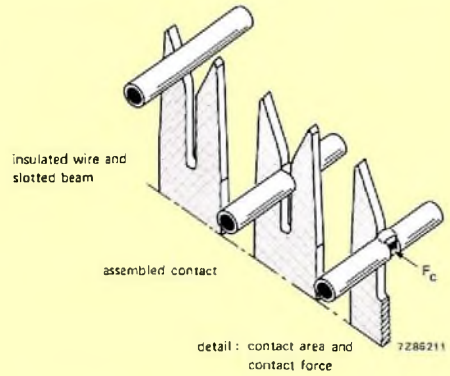


Fig.1 Principle of the ID connection. When a wire is forced between the tines of an ID fork the insulation is parted and the bare copper forces the tines apart

As part of a general study on pressure contacts we have investigated insulation displacement contacts. These studies have involved finite element analysis of the tine shaping with a view to a proper distribution of stress, and thus of stored energy. They have also included a full analysis of all the factors involved in pressure contacts.

COMPARISON WITH OTHER JOINTING TECHNIQUES

In comparing various jointing techniques a number of factors must be considered:

- costs, including speed of processing, cost of equipment and qualification (training) of staff
- number of defects
- long term reliability
- breadth of application.

Table I compares a number of detailed aspects affecting the above considerations. With the insulation displacement technique, provided the design is well founded, there is virtually no chance of operator error. The defect rate and the long term reliability are entirely dependent on how the connector is designed and made.

Comparison of jointing techniques

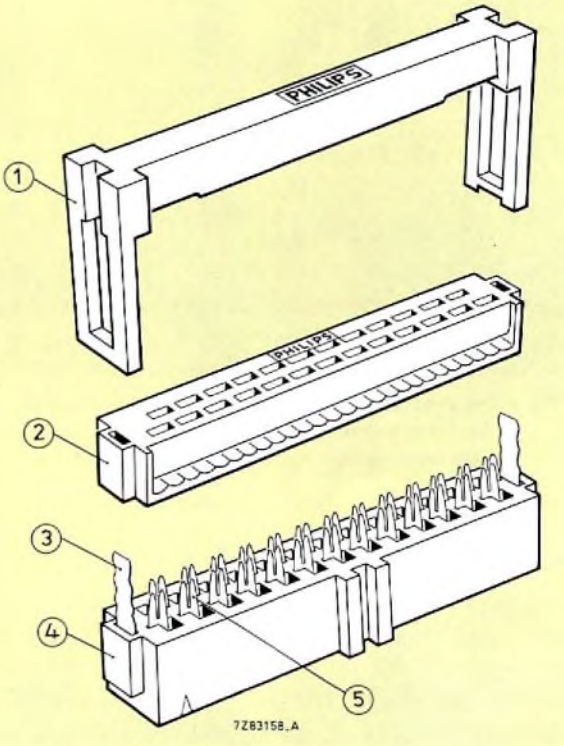
criteria	hand soldering	wire-wrap	crimp	IDC
cost per joint	high	medium to low	low	low
investment	low	low to high*	medium to high*	low to medium
automation	no	yes	yes	suitable
working speed	slow	medium to fast*	medium to fast*	fast
staff qualification	high	low	low	low
heat used	235 °C (2s)	none	none	none
used for single stranded wires	yes	only by overwinding	yes	yes
used for single solid wire	yes	yes	yes	yes
for flat ribbon cable, solid or stranded	under certain conditions	no	under certain conditions	yes
possibility of remaking joint	possible	under certian conditions	impossible	under certain conditions

* Depending on degree of automation.

TYPICAL ID CONNECTOR

Figure 2 shows the various parts comprising the female half of an F303 connector combination. The strain relief bridge is really an accessory, but the rest perform essential 'tool' functions during the actual jointing operation.

When making the connection the ribbon cable is inserted into the pressure block where ribs placed close to the contacts position and hold it. The contact block is placed above with the barbed locking tongues slightly inserted into their mating slots. With a hand or machine tool the parts are then pressed together and the jointing operation is complete. The ribbon cable can then be folded back over the pressure block and the strain relief bridge can be clipped in position. The cable is pulled taught and the contacts are thus relieved of strain, Fig.3.



1 strain relief bridge
2 pressure block
3 locking tongue
4 contact block
5 contact fork

Fig.2 Component parts of an F303 insulation displacement connector

Conductor

The conductor used in ID jointing is of electrical copper either stranded (7 strands) or solid single strand. It will be clear that these behave differently. A solid conductor will deform as soon as the stresses exceed the yield point for electrical copper, while a stranded conductor will rearrange before deforming. Careful shaping of the inlet slot can promote proper rearrangement before deformation (the actual jointing) begins, see Fig.4.

As it is forced into a slot narrower than its diameter the conductor deforms. Copper that flows along the line of the applied force increases the area of contact between the conductor and the sides of the slot. The shape of the inlet plus the combination of movement and pressure promotes flow in the direction of movement.

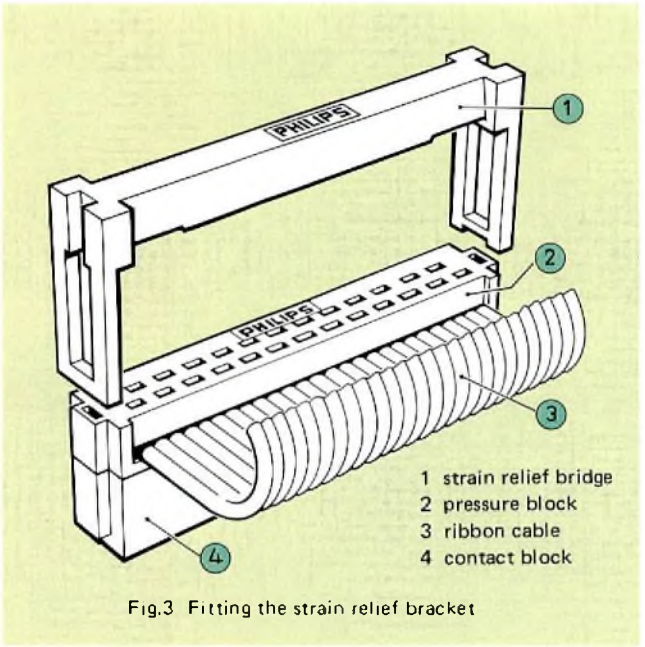


Fig.3 Fitting the strain relief bracket

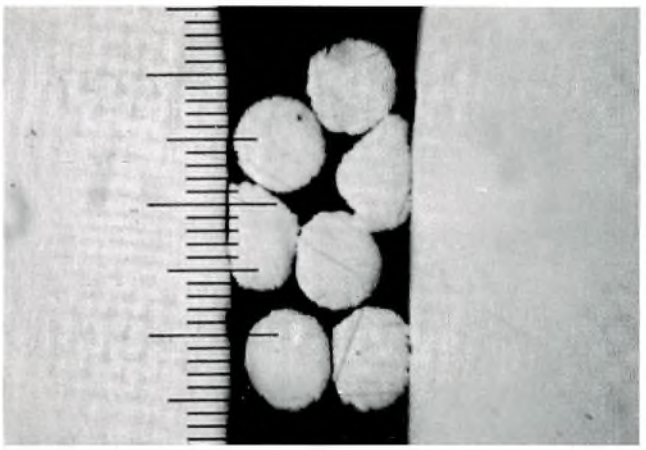


Fig.4 The strands in a stranded conductor are rearranged before deforming to form the actual joint. Microphotograph at 50 X magnification

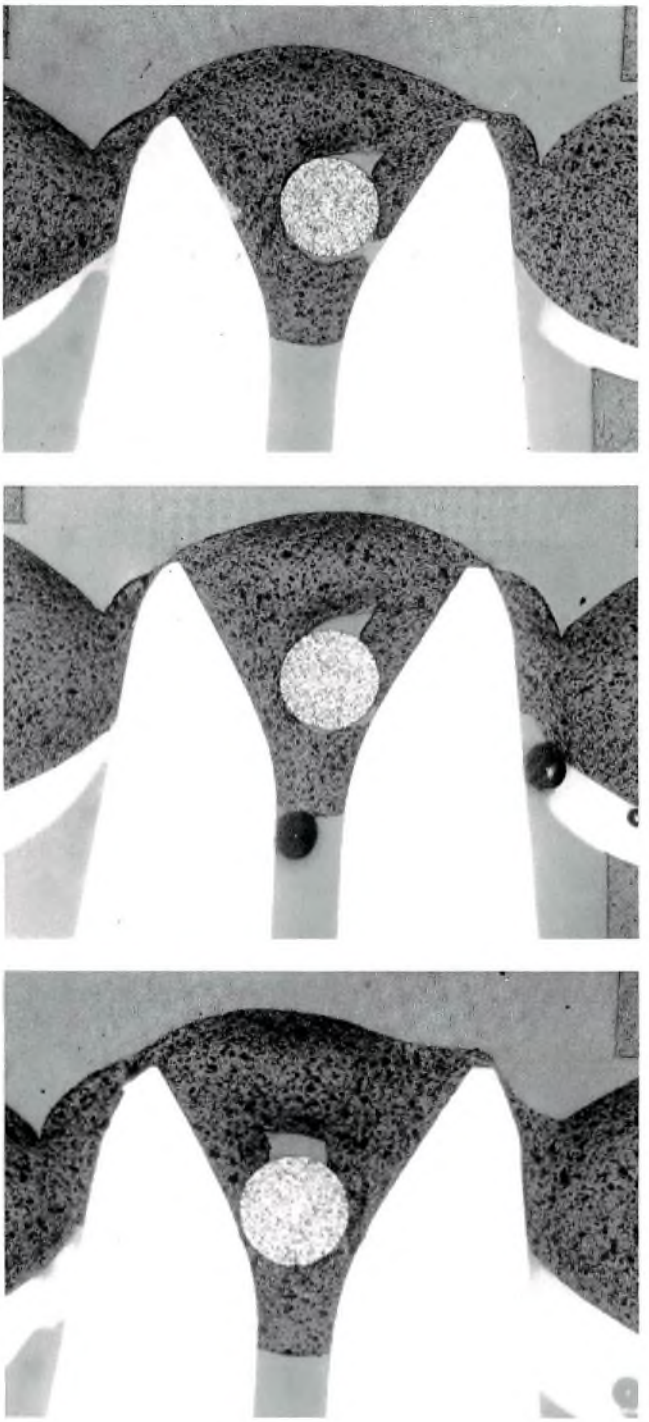


Fig.5 Micrograph showing how the inlet guides the wire into the contact fork. Magnification 50 X

Contact fork

The design of the contact fork is critical to the performance of an ID connection. The inlet area must be so shaped that the insulation is displaced and the conductor is guided into the contact slot (Fig.5). The slot and the tines must be so dimensioned that a good, gas-tight* joint is formed that, owing to the stored energy in the tines, maintains a low contact resistance indefinitely. The edges of the contact forks should be flat (i.e., not knife edges) in order to deform the copper conductor without nicking (cutting) it.

Another important aspect of the contact fork is its spring properties. It is important that once the joint is made the fork continues to exert pressure on the copper conductor. In the F303 range, beryllium copper is used because of its higher stiffness and because it relaxes very slowly, thus maintaining pressure indefinitely.

* Many authors use the term 'cold weld' in describing this type of connection. Scanning electron microscope investigations have not disclosed any evidence of cold welding, simply a high pressure, gas-tight joint. We are forced to conclude, therefore, that cold welds rarely, if ever, occur.

When a wire is forced between the tines of a fork, the insulation is first stripped from the wire and then the wire itself enters the slot. The tines are deflected and the wire is flattened. At each position along the slot an equilibrium will exist between the deflection of the tines and the flattening of the wire.

The force/deflection curves for a family of points l_1 to l_f can be plotted as in Fig.6. If the force/deformation (flattening) curve for the wire is now plotted on the same scale (Fig.7) the point of equilibrium will enable us to determine the force acting on the wire at any point. On the horizontal scale we can read off the slot width or the thickness of the deformed wire. The dashed line from l_f to the x axis represents the drop in contact force if the wire were released. The shaded area bounded by this line and by the force deflection curve represents the energy stored in one tine.

It is imperative that the joint be gas-tight. Most metals, including copper and its alloys, tarnish rapidly in contact with air. For example, a monatomic layer is formed on clean copper within 1 μs at a gas pressure of 1 Torr. Under normal atmospheric conditions a tarnish layer (consisting mostly of oxides) some 2 – 10 nm (20 – 100 Å) thick will be formed. Oil, finger marks and tool smear add their share of contamination. With the ID connection this tarnish layer is removed together with superficial copper to bring clean copper into contact with the less tarnishing surface plating of the contact fork.

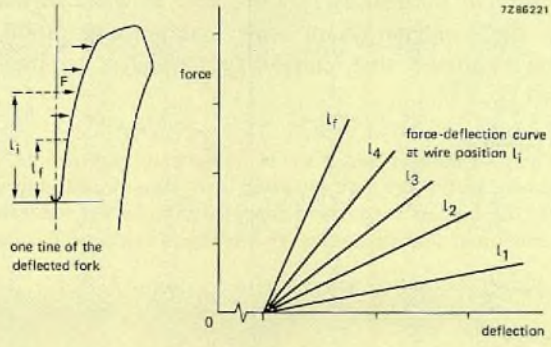


Fig.6 Family of force deflection curves for one half of a contact fork

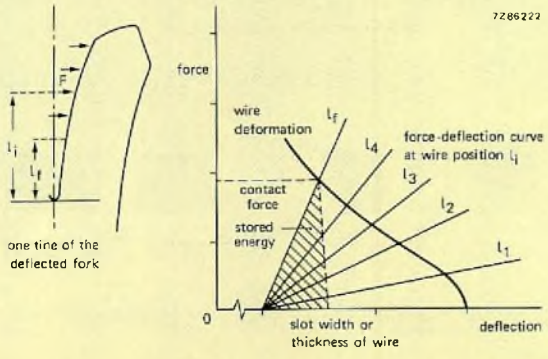


Fig.7 Force/deformation curve superimposed on the force/deflection curve of Fig.6. The shaded area is a measure of the energy stored in the spring element

COPPER

Copper is a highly ductile metal that relaxes early and work-hardens under stress. Work-hardening reduces ductility and increases brittleness. It is one of the reasons why a nicked copper wire (one with a small cut, as sometimes occurs in stripping) will fracture sooner under conditions of vibration than one that is not nicked. In ID connections work-hardening affects both the copper wire and the beryllium copper fork.

In the copper wire it increases the resistance to plastic flow, while in the tines of the fork it increases the stress needed for a given deflection, and thus increases the energy stored in the deflected tine.

In the plastically deformed copper conductor there will be relaxation and retardation. The high stress peaks in the asperities reduce relatively quickly and the material creeps until an equilibrium based on the increased area of the contact faces is reached.

As can be seen in Fig.8, the yield strength of pure copper is too low for it to be used as a spring material. However, adding small amounts of other metals (e.g., 1 – 2% beryllium) can considerably increase yield strength. Such spring materials absorb considerable amounts of energy when elastically deformed and return this energy when unloaded. Beryllium copper, furthermore, relaxes very, very slowly so that enough energy can be stored for the required life of the connector.

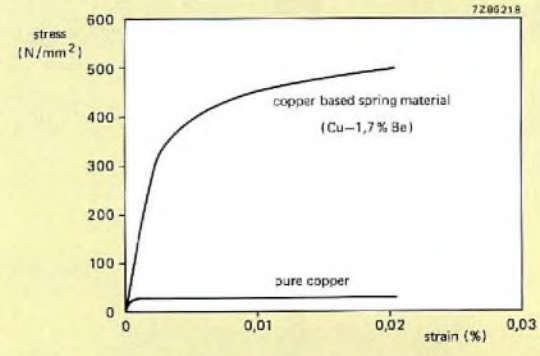


Fig.8 Stress/strain relationship for copper and beryllium copper. Just the addition of 1.7% beryllium transforms copper into an excellent spring material

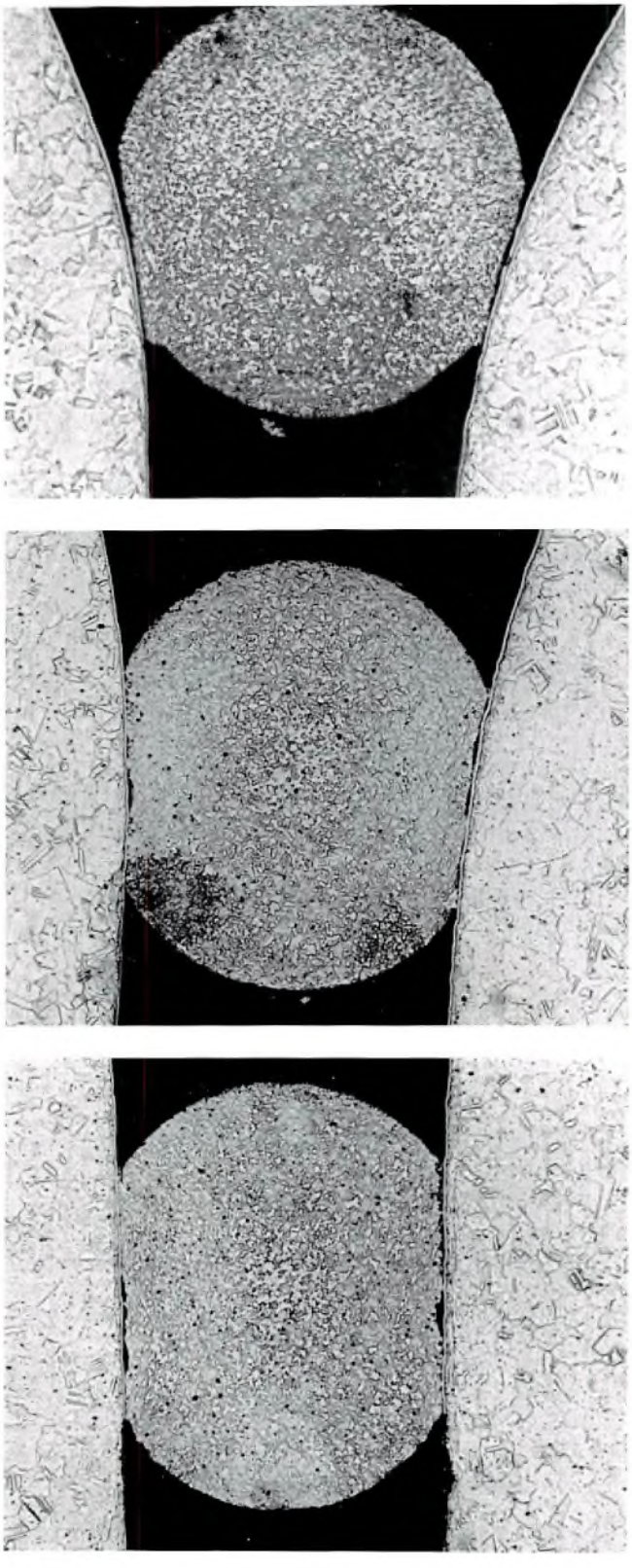


Fig.9 Three stages in forming the ID connection. At a magnification of 200 times one can see the importance of the shape of the inlet slot. In the lowest view the wire is fully deformed but has not yet reached its final position

Contact area

When the copper wire is forced between the tines of the fork its circumference is flattened. This is partly due to broadening (at right angles to the conductor axis) and partly to lengthening (along the conductor axis). Lengthening does not increase contact area, whereas broadening does. Fortunately, the sliding action as the wire is thrust between the tines of the fork promotes broadening rather then lengthening.

The force which thrusts the wire into the contact fork is transmitted by the edges of the pressure block. If these are too wide the wire will bend, see Fig.10, which means that the wire will not reach its intended position in the slot, with the result that the requisite deformation will not be obtained and that the residual contact force will be lower than required.*

When two metals are pressed together they do not contact with the intimacy that one might expect. Although apparently smooth, the mating surfaces are covered with asperities (prominences) which act as current bottlenecks and increase contact resistance. The extent to which these asperities are flattened depends on the applied force and the ductility of the metals. In a properly designed ID connection the combination of wipe and pressure produces a contact surface that closely approximates to the ideal (Fig.11).

* It may be thought that it would be better to transmit the thrust actually within the slot. However, computer models have shown that this hinders the flow of copper within the slot and leads to a reduction of contact area and an increase in contact resistance.

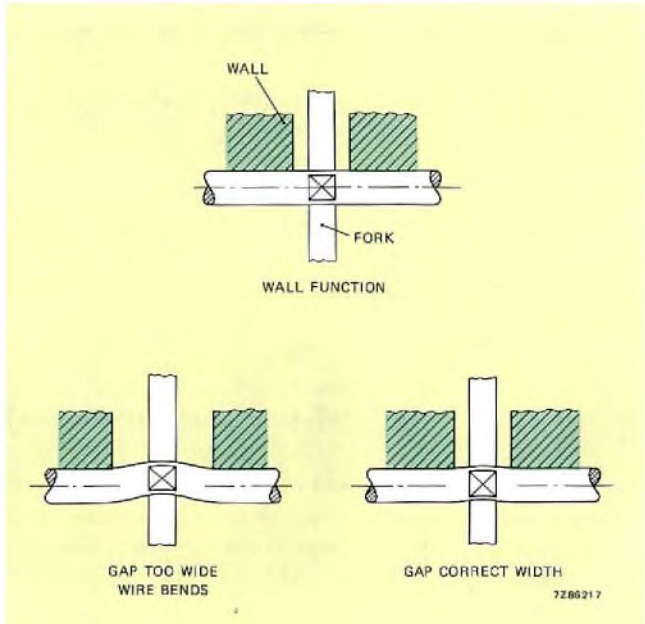
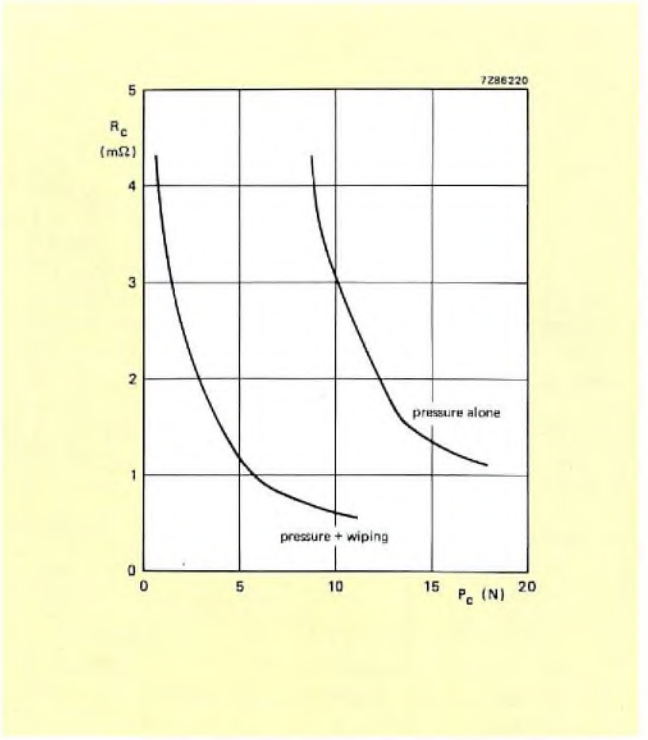


Fig.10 Because the thrust is transmitted through the edges of the slot it is important not to have the slot too wide. If it is the wire buckles and does not reach its intended place in the fork.



Contact resistance

If the conductor makes a pure metallic contact with the fork and if the pressure is such that all asperities are flattened so that they effectively overlap, the contact resistance (Ref.1, 2) is given by

$$R_c = \frac{\rho}{2}\sqrt{\frac{\pi}{nA_w}}$$

where ρ is the average resistivity of the two metals involved, A_w is the total area of each contact face, and n is the number of contacting faces.

In our case the resistivities are:

fork, ρ_f, is 83.0×10^{-3} mΩ mm²/mm,

wire, ρ_w, is 14.54×10^{-3} mΩ mm²/mm

and the number of contacting faces (n) is 2.

This leads to a contact resistance of

$$R_c = \frac{30.562 \times 10^{-3}}{\sqrt{A_w}}\ \text{m}\Omega$$

The minimum contact resistance obtainable with an ideal contact surface is given by

$$R_{c\,min} = \frac{\rho_f}{2D}$$

where D is the diameter of the conductor. With AWG 28 conductor D is 0.32 mm and with a beryllium copper contact fork the minimum resistance is 129.69 μΩ, say 0.13 mΩ.

Rewriting the first equation we get:

$$A_w = \frac{\pi}{n}\left(\frac{\rho}{2R_c}\right)^2$$

which allows us to calculate the requisite contact area for the minimum obtainable contact resistance. In the present case, with $R_c = 0.13$ mΩ, the requisite contact area is 55.27×10^{-3} mm².

A noteworthy result of the above equation is that for the contact resistance to rise to ten times its original value (a commonly applied standard in determining the limits for a faulty contact) the contacting area has to be diminished to *one hundredth* of its original value.

Ribbon cable

Most ID connector systems are designed for differing sorts of cable. There is so much interplay between cable and connector that close cooperation between cable manufacturer and connector manufacturer is needed for the successful design of a system. It is far better if the manufacture of both is in the same hands, as in our case. This allows an optimum relationship between the properties of both to be attained.

Flat ribbon cable is shown in Fig.12.

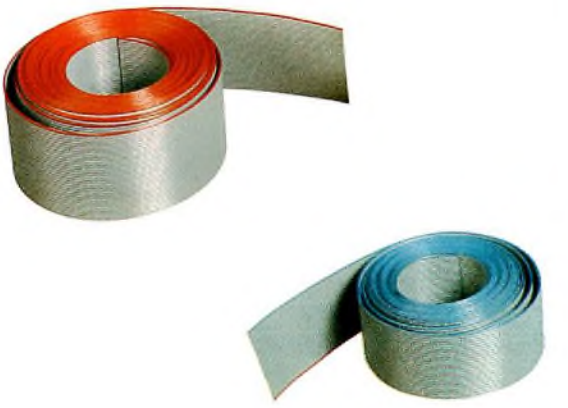
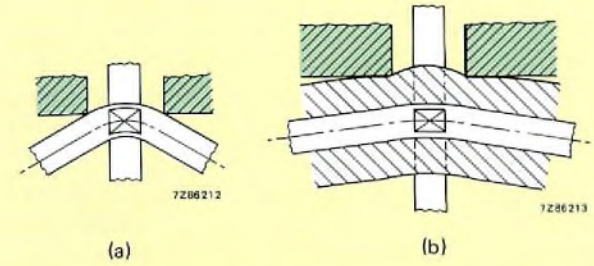


Fig.12 Standard flat ribbon cable. The first wire is marked red for identification purposes and every fifth wire black to ease counting and splitting

To ensure proper transmission of the thrust the slots are made barely wider (in the longitudinal direction of the cable) than the thickness of the contact forks. In the transverse direction they are just large enough to accommodate the slight expansion of the contact forks during pressing and any misalignment resulting from manufacturing tolerances. These latter are in any case very small because of the extensive automation used in the manufacture of F303 connectors.

Insulation

Apart from its obvious insulation function much is asked of the insulation both during and after the pressing operation. It must deform to accomodate misalignment between each conductor and its fork. It must also support the conductor so that it does not bend vertically when being forced between the tines of the fork (Fig.13). To a certain extent these are conflicting requirements. A further requirement is that stresses do not cause the slits made by the tines of the fork to spread either circumferentially or longitudinally. Here it should be remembered that the faces of the tines are not knife edges. They must be flat in order to deform the copper conductor without nicking it.



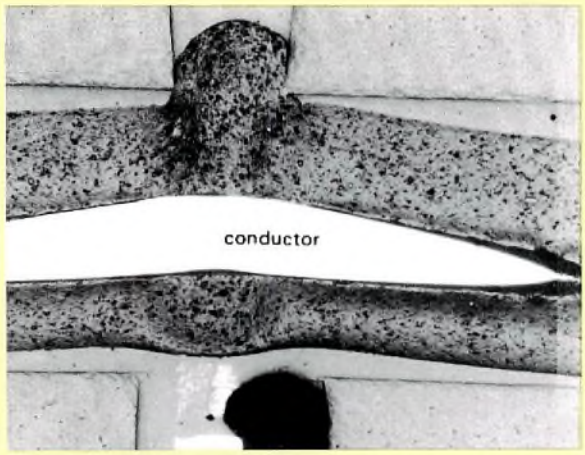


Fig.13 Insulation helps support a wire during the jointing operation: (a) an uninsulated wire after jointing and (b) an insulated wire. The photomicrograph below shows how little bending actually occurs

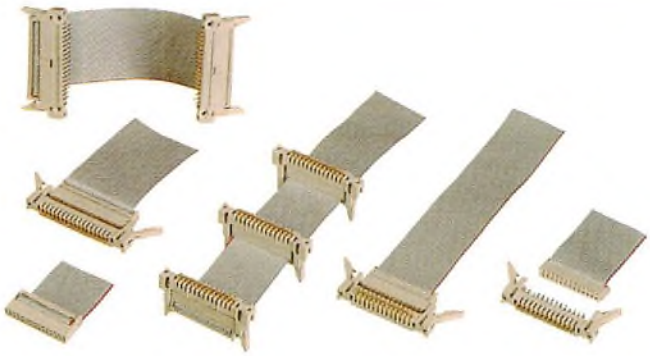


Fig.14 A selection of the F303 connector range

TYPES OF CONTACT FORK

Although there are many varieties in the detail design of contact forks, four main categories exist, as shown in Fig.15. Type (a) is a single fork that forms a double contact with the conductor. Type (b), the tube contact and the double fork contacts shown in (c) and (d) have a further slot that may also make contact with the conductor. For this reason they are sometimes known as four-point contacts. It is said, although we do not wholly agree, that the main function of the additional slot is usually to relieve the main contact of stresses transmitted through the cable. A little consideration will show that if the main contact is properly designed and dimensioned the additional contacts formed by the strain relief gap cannot contribute significantly to reducing contact resistance. If the strain relief function is performed by other means the additional fork can be dispensed with.

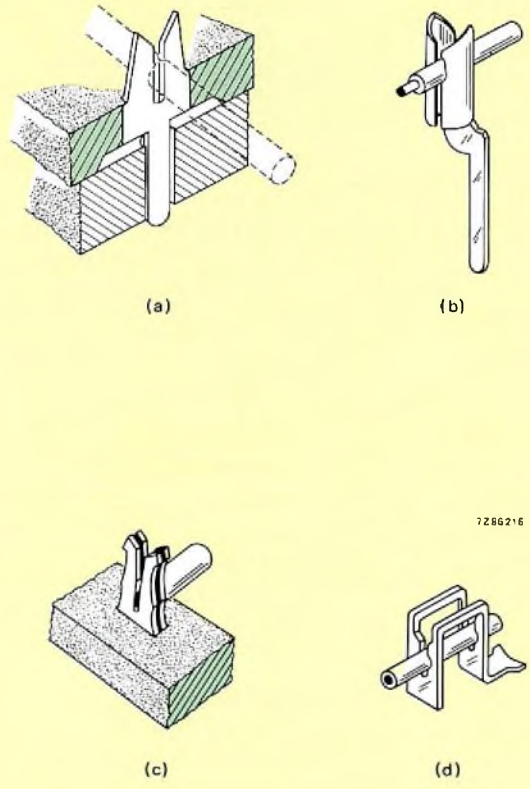


Fig.15 Four common types of contact fork. The double fork contacts shown in (b), (c) and (d) seem to offer greater security but this is far from being the case. When the mechanisms involved are fully analysed it is seen that a properly designed and manufactured single fork contact achieves minimum contact resistance, maintains it indefinitely and does not suffer the drawbacks associated with being mechanically coupled to another system

PLASTICS

Plastics differ in many respects from metals, the differences being determined by their molecular and macromolecular structure. For cable insulation two molecular types come into consideration:

- filamentary or linear molecules, possibly with some branching (e.g., polyethylene)
- filamentary molecules with strong cross-linkages (e.g., hard rubber, amino plastics and phenol plastics.

They may be unordered (amorphous) or partly ordered (partly crystalline). The molecules in each filament are bound together by primary atomic bonds. Between filaments weaker, secondary bonds (e.g., van der Waals forces) exist which increase the molecular order, i.e., create a certain amount of sub-microscopic crystallisation (Fig.15(a)). Extrusion (forcing through a nozzle) causes a certain alignment in the filaments with some crystallisation (Fig.15(b)). Undesired crystallisation can be prevented by copolymerisation or by the addition of fillers and softeners.

Plastics differ in their behaviour under stress. In its pure state PVC (polyvinyl chloride) is a very brittle material and it is the addition of fillers, stabilisers and softeners that determine its final properties. In hard PVC, plastic deformation precedes fracture. Soft PVC undergoes considerable plastic deformation before splitting or tearing takes place.

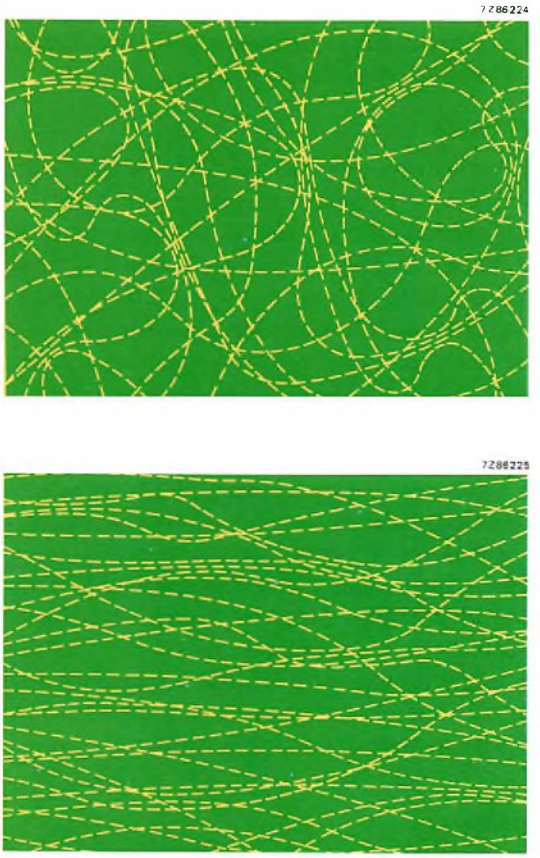


Fig.16 Arrangement of the molecular filaments in PVC, (a) unextruded; (b) extruded. Note the areas of crystallisation in both cases

Mechanical forces are insufficient to loosen primary atomic bonds, so that an extruded cable insulation is more resistant to stresses along the axis of the cable than to those across it. In an ID joint the tines of the fork apply stresses at right angles to the cable axis and cause tiny slits along the cable axis.

Another important point for cable insulations is that they should be *thermoplastic*. Thermoplastics are those that above their melting point merely soften over a wide temperature range and are not completely liquid even at their dissociation temperature. Softening means that over the entire spectrum from solid to liquid the macromolecules are thermally mobile but, because of 'matting effects', they are only free to slide against each other. The softeners mentioned earlier lower the melting point to the minimum working temperature (soft PVC $\simeq -30\,^{\circ}C$). In *thermosetting* plastics the dissociation temperature is below the melting point.

The properties of PVC also vary with temperature and time (see Fig.17). It is the visco-elastic and elasto-viscous behaviour that is particularly important for ID connections. This can be demonstrated by the model of Fig.18. Here a force is applied to the upper block loading the PVC blocks. It is assumed that the force is just sufficient to compress the PVC until the upper block just rests on the copper block. Initially high stresses build up in the PVC because its visco-elastic behaviour causes a delay between stress and strain. Once the load is taken by the copper block the elasto-viscous phase begins. The strain remains constant and the stress falls with time and is shifted to the copper block. If the load were increased further it would be borne by the copper block alone until that, too, entered its plastic phase.

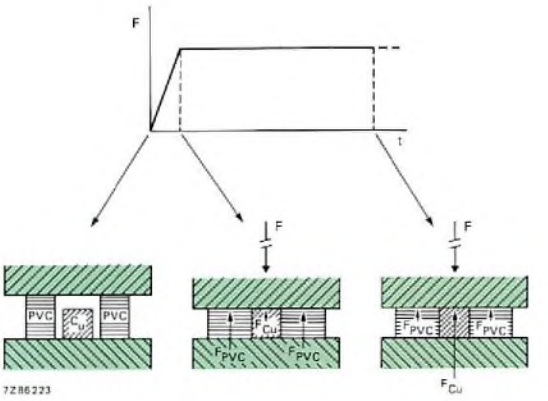


Fig.17 The stress strain relationship in PVC is dependent on temperature and time

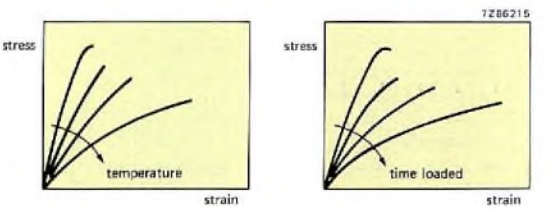
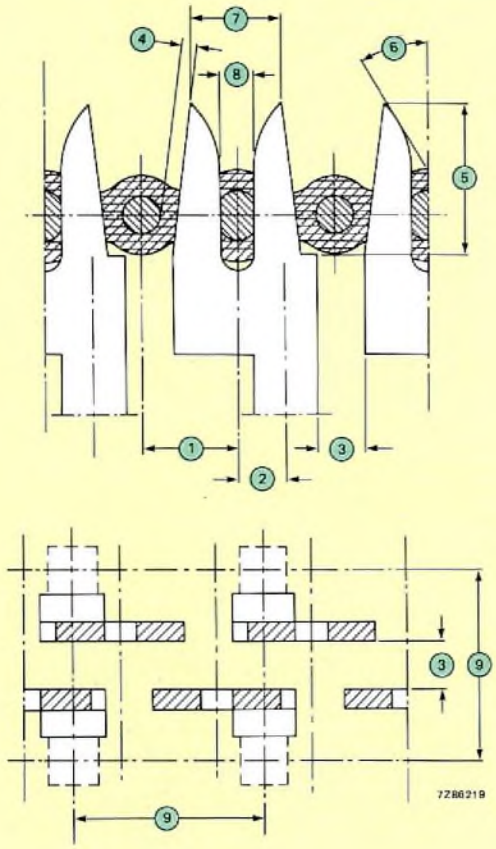


Fig.18 Model showing how PVC elastically deforms when loaded

F303 connector types

Cable connectors									
number of contacts:	10	14	16	20	26	34	40	50	60
polarising key:	with/without								
strain relief bracket:	with/without								
Male headers									
number of contacts:	10	14	16	20	26	34	40	50	60
clamp/ejectors:	with/without								
connection pins:	dip solder		straight 90°						
	wire wrap		straight 90°						

F303 connectors can be supplied with any combination of the features mentioned above. Coding pegs can also be supplied.



1 conductor spacing
2 conductor-contact spacing (½ conductor spacing)
3 creepage path = min. wall thickness
4 insulation resistance
5 max. connector height
6 optimum inlet angle
7 conductor spacing
8 contact slot (determined by conductor)
9 connector raster

Fig.19 The properties of an F303 connector are the direct result of conductor dimensions and 'e' grid spacing

Fig.20 Manual and automatic tools used for making F303 ID connections

Pressure block

During the pressing operation the pressure block has two main functions: 1, to correctly position the ribbon cable with respect to the contact forks and 2, to transmit the thrust so that the conductors are forced between the tines of the forks. In the F303 the cable is positioned by ribs in the pressure block. Being part of the same mould ensures that they are accurately positioned with respect to the slots through which the contact forks pass.

Contact block

The contact block holds two rows of contacts with ID forks, staggered with respect to each other to match the conductor spacing of the cable. The forked contacts are identical, but in the one row they are turned 180° to those in the other row. At each end of the block there are barbed tongues that locate the two blocks with respect to each other and lock them together after the pressing operation.

With ID techniques being widely used for interconnection to printed circuit boards it is not surprising that the 'e' pitch has become the standard on which the distance between conductors is based. Half 'e' (1.27 mm or 0.05 in.) is the standard distance and this allows connection to a two-row connector with the pins on the normal 'e' pitch.

Conductor dimensions and circuit board grid, of course, determine the size of the connector, see Fig.19. For compact interconnection to a pin array on the 'e' grid, the spacing between adjacent connectors leads to a connector housing width of 6.35 mm and a length of $(2.54n + 2 \times 3.81)$mm, where n is the number of contacts per row.

REFERENCES

1. HOLM, R. 1979. 'Electric contacts' 4th ed. Springer Verlag.
2. GREENWOOD, J. A. 1966. International research symposium on electrical contact phenomena.

For the dual-tone multi-frequency dialling system now being widely adopted, subscriber telephones have to incorporate means to generate the prescribed tone pairs. Although no two of the eight tones are harmonically related, they can all be derived from one crystal oscillator. This article tells how.

Bipolar ICs for DTMF telephone dialling

J. J. A. GEBOERS

THE DTMF DIALLING SYSTEM

Impulse dialling with a rotary telephone dial is a slow process which engages exchange equipment for longer than necessary and is subject to inaccuracy. Electronic pulse dialling systems are more accurate, allow a pushbutton keyboard to be used, and speed up the process from the subscribers's point of view. These systems, however, still engage the exchange equipment for a long time during dialling and require the use of a memory for the dialled information because the exchange cannot process the pulse trains as quickly as they can be generated. The solution lies in a pushbutton dialling system where each digit, or other keyboard function, is represented by a discrete tone burst within the frequency limits of the telephone speech band (300 Hz to 3400 Hz). To eliminate line whistles, each tone burst must be a combination of two fundamental frequencies. Since each dialled digit is represented by a different pair of frequencies, the system is known as dual-tone, multi-frequency (DTMF) dialling.

For a 4 x 4 matrix keyboard, as shown in Fig.1, eight tones are necessary to represent, for example, the ten numerals (0 to 9), two functions (★), and (#), and four additional keys to allow for future extension of facilities. Eight tones recommended by the CCITT have been so chosen that minimum intermodulation occurs between harmonics of each of the 16 possible pairs of fundamental frequencies. The four lower frequency tones recommended by the CCITT are 697 Hz, 770 Hz, 852 Hz and 941 Hz; they are allocated to the four 'row' lines of the keyboard matrix. The four recommended higher frequency tones are 1209 Hz, 1336 Hz, 1477 Hz and 1633 Hz; they are allocated to the four 'column' lines of the keyboard matrix.

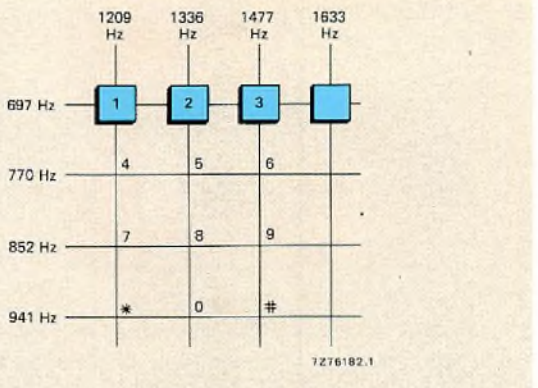


Fig.1 Allocation of dialling tones to keyboard functions

Our range of integrated circuits for DTMF telephone dialling satisfy the diverse requirements of telephone authorities throughout the world

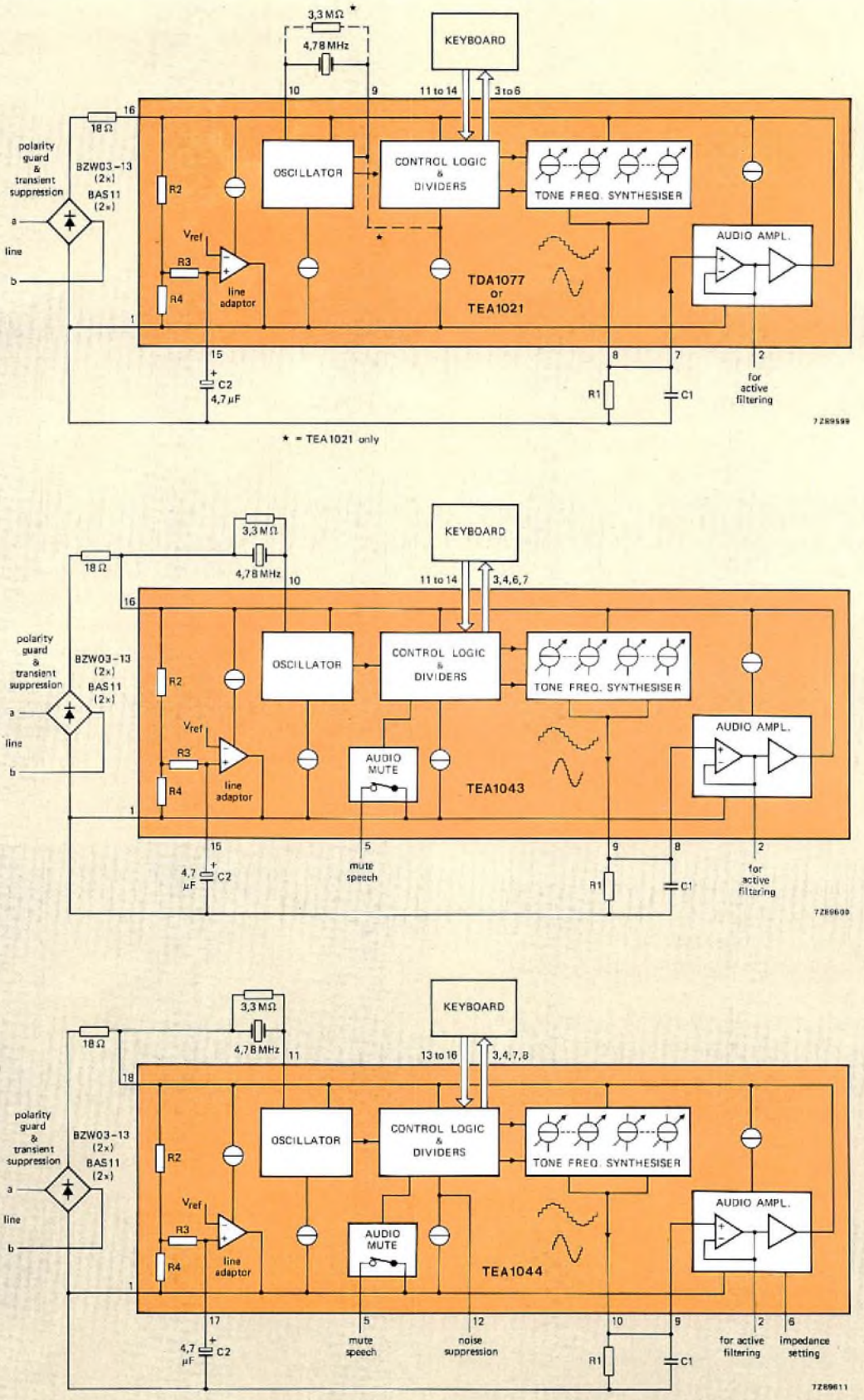


Fig.2 Block diagrams of the dialling circuits

INTEGRATED CIRCUITS FOR DTMF DIALLING

In 1978 we introduced the TDA1077, our first integrated circuit for DTMF dialling. The range has now been extended to include the TEA1021 and TEA1043 in DIL 16-pin plastic or cerdip encapsulation and the TEA1044 in DIL 18-pin plastic or cerdip encapsulation. Unlike the TDA1077 in which the impedance of the circuit (900Ω) is defined by an internal resistor network, the impedance of the new circuits is defined by a low-impedance output stage. The current consumption is therefore less than that of the TDA1077. The new circuits also have less spread of the tone output level. The TEA1043 and TEA1044 have an internal switch which allows simple muting of the speech circuits without the need for a common contact on the keyboard. One of the additional pins of the TEA1044 is used to provide adjustment of the impedance of the circuit without increasing current consumption as would be the case with a parallel resistor. The other additional pin allows connection of a capacitor for interference suppression.

The choice of technology to produce the DTMF dialling circuits was influenced by the need for both analog and digital circuit elements and the necessity for the circuits to operate under the following conditions:

- a supply current range of 10 mA to 120 mA from the telephone lines
- matching to a maximum line impedance of 900Ω
- a minimum supply voltage of 1.3 V.

The low operating current and voltage enable the circuits to operate when connected to long lines. The high operating current is necessary for operation with short lines and high line voltage. Consideration of these points has resulted in I^2L designs which also incorporate current-mode logic for the high frequency clock circuits, thereby allowing fast logic circuitry to be contained on the same chip as the analog circuitry.

INTEGRATED FUNCTIONS

Block diagrams of the four integrated DTMF dialling circuits with their basic peripheral components are given in Fig.2. The circuits generate the two-tone combinations recommended by the CCITT, from a highly stable crystal oscillator source. The crystal oscillator generates a 4.78272 MHz square-wave which is divided by 12 to obtain a 398.56 kHz clock. Two variable dividers produce square-waves at the tone frequencies demanded by the keyboard inputs. Two scalers then divide the selected tone-frequency square-wave into 18 increments for the higher-frequency tone and into 14 increments for the lower-frequency tone. Each of these increments is converted into a current by a current source, the sum of the currents being equal to the instantaneous amplitude of a sinewave. The tone-frequency square-waves are thus converted into crude sinewaves composed of 14 (lower tone) or 18 (upper tone) constant-amplitude increments. The high-order harmonics are attenuated by an RC low-pass filter before the tones are connected to the telephone line via an output amplifier with adjustable input level.

Line adaptor

To allow their use with very long lines, the dialling circuits are so designed that they are capable of operating from a minimum supply voltage of 1.3 V. Since the composite dialling tone signal modulates the line voltage, it must be superimposed on a d.c. level so that its negative-going peaks do not reduce the line voltage to less than 1.3 V. The maximum tone levels on the line are −4 dBm for the higher frequencies and −6 dBm for the lower frequencies. This corresponds to a peak level of 1.25 V (0.7 V + 0.55 V) for the composite tone signal on a 600Ω line. The output bias level must exceed this level by at least 0.75 V to allow a margin for a ±2 dB tone level tolerance and for variations over the line current and operating temperature range. The resulting 3.3 V d.c. output bias level shown in Fig.3 is maintained by a shunt regulator in the line-adaptor section of the circuit. The low-pass filter formed by integrated resistors R_2, R_3 and an external capacitor prevents a.c. line signals influencing the operation of the shunt regulator.

The action of the low-pass filter could cause a problem when power is initially applied to the circuit by pressing a keyboard pushbutton. The operation of the shunt regulator would then be delayed for a few milliseconds whilst the filter capacitor was charging. During this period, the lines would act as a current source loaded by the impedance of the circuit (900Ω) and the ensuing voltage developed across the circuit could over-drive the sensitive tone receivers in the exchange. The line adaptor therefore incorporates a circuit which causes rapid charging of the filter capacitor each time power is applied. This reduces the line voltage overshoot to only 1 V above the 3.3 V level set by the line adaptor.

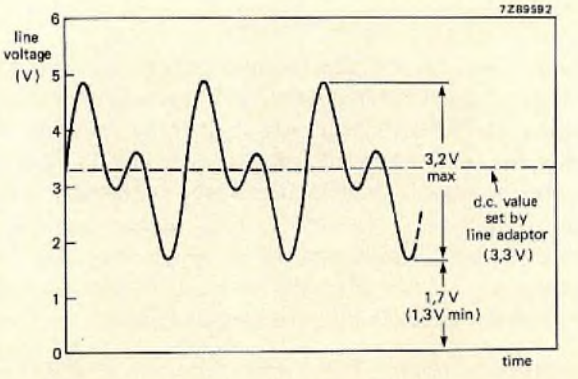


Fig.3 The output bias level is determined by the minimum voltage required by the integrated circuit and by the maximum amplitude of the dual-tone output

Dialling tone generator

Oscillator and dividers. Ideally, the system clock frequency should be the lowest common multiple of the eight required tone frequencies. This frequency (1.4×10^{14} MHz) however is impractical. Calculations have shown that all the tones can be generated to within 0.11% of the required frequency by using a clock frequency of 199.28 kHz and eight integer dividers. Since some of the divisors would then be odd numbers, however, some of the synthesised tone waveforms would be asymmetrical and would therefore have a large even harmonic content. This is overcome by doubling the clock frequency to 398.56 Hz and also doubling the divisors. The crystal oscillator frequency is twelve times the clock frequency, i.e. 4.78272 MHz. The required tone frequencies, divisors and frequency errors are shown in the Table.

The CCITT recommend that the tones should be within ±1.3% of the specified frequencies. Many telephone authorities, however, require a closer tolerance of ±1%. Factors contributing to frequency errors are:

- manufacturing tolerances for the crystal
- temperature-dependent drift of the crystal frequency
- long-term frequency drift of the crystal
- tone synthesiser errors (see Table).

Generation of tones from a 398.56 kHz clock

tone required (Hz)	divisor	tone generated (Hz)	absolute error (Hz)	relative error (%)
697	572	696.78	−0.22	−0.03
770	518	769.42	−0.58	−0.08
852	478	851.62	−0.38	−0.04
941	424	940.00	−1.00	−0.11
1209	330	1207.76	−1.24	−0.10
1336	298	1337.45	+1.45	+0.11
1477	270	1476.15	−0.85	−0.06
1633	244	1633.44	+0.44	+0.03

For a typical crystal, the manufacturing tolerance and temperature-dependent frequency drift over the temperature range −25 °C to 70 °C is less than 0.1%. Over about 15 years, the frequency drift will be less than 0.1%. The total frequency error, including that of the synthesiser is therefore $0.1 + 0.1 + 0.11 = 0.31\%$, well within both of the specified limits. Because of the extremely low error of the synthesiser, a cheaper crystal with a 0.5% tolerance could be used without exceeding the specified limits.

Sinewave synthesis. The outputs from the dividers for the higher and lower-frequency tones are symmetrical square-waves which contain considerable odd-numbered harmonics. The lower-order odd-numbered harmonics (11th and less) are eliminated by synthesising the tone frequencies as crude stepped sinewave approximations as shown in Fig.4. Each half cycle of the tone waveform comprises seven discrete amplitudes for a lower-frequency tone and nine discrete amplitudes for a higher-frequency tone. Each amplitude increment is generated by switching on an individual current source for the duration of each step of the sinewave. The sum of the increments for the higher-frequency tone is 2 dB (1.26 times) greater than that for the lower-frequency tone in accordance with existing standards. The frequency of the tones is varied by changing the duration of each step. To switch the current sources, it is necessary to generate square-waves with a period of 1/14th or 1/18th of the required tone frequency period by using scalers following the variable-length dividers as shown in Fig.5. Ideally, these scalers should have a length of 1/14th or 1/18th of the divisors shown in the Table. This, however, would require scaling by non-integer divisors, which is impractical. To obtain the correct tone frequencies, some of the steps of the synthesised waveform are therefore made a few clock periods longer than the others. For example, the 1209 Hz tone requires the clock frequency to be divided by 330 and each of the 14 steps of the synthesised sinewave should have a duration of $330/14 = 234/7$ clock periods. The problem is solved by allocating 24 clock periods to each of

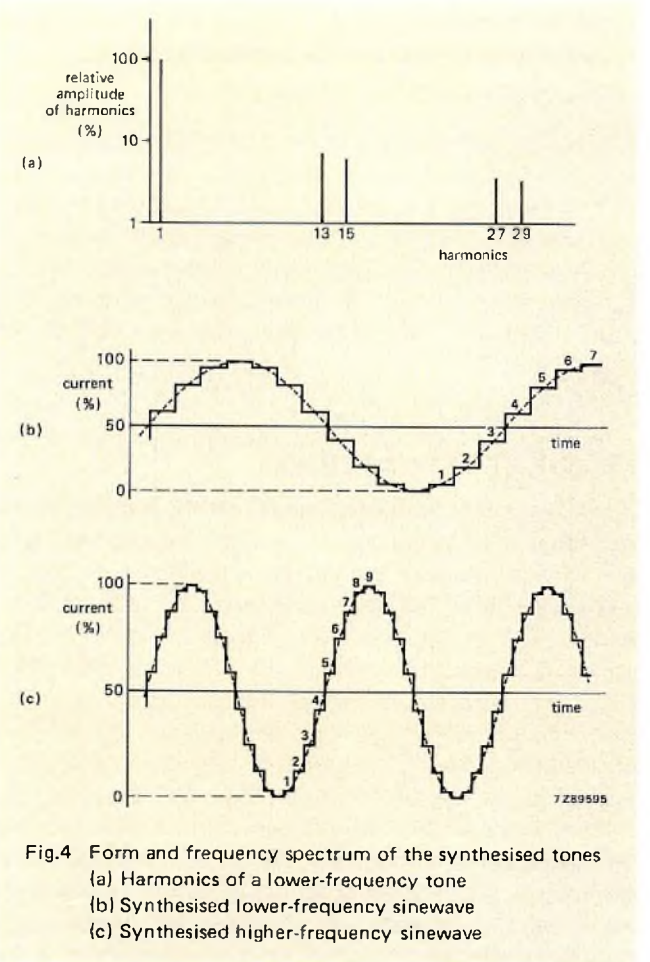


Fig.4 Form and frequency spectrum of the synthesised tones
(a) Harmonics of a lower-frequency tone
(b) Synthesised lower-frequency sinewave
(c) Synthesised higher-frequency sinewave

12 steps and 21 clock periods to each of the remaining 2 steps. A similar procedure is used to generate the 18-step lower-freqiency tones. The harmonics from the 13th upwards (lower frequency tones) or 17th upwards (higher frequency tones) can be attenuated by a low-pass filter which can comprise either a first-order passive RC network at the output of the synthesiser, or a second-order active network via the additional pin provided between the two stages of the output amplifier.

Audio amplifier and filtering

The output current from the sinewave synthesiser causes a voltage drop across resistor R_1 (Fig.2). At this point, the signal path is broken to allow the insertion of filter components in series with the input to the audio amplifier. The connection between the two stages of the audio amplifier is also brought out to a pin to allow the connection of active-filter components in the feedback path to provide additional attenuation of the higher-order odd harmonics of the tone frequencies.

The amplitude of the tone output is directly proportional to the value of R_1 and can therefore be adjusted to meet specific requirements.

Speech muting

Figure 6(a) shows the interconnection of the dialling and speech circuits of a conventional pushbutton or rotary dial telephone. A high-quality mechanical changeover contact normally short-circuits the dialling unit. Depression of any keyboard pushbutton (or rotation of the dial) actuates the contact to transfer the short-circuit to the speech circuit. In a pushbutton keyboard such a contact must be operated by every pushbutton and is consequently rather complex.

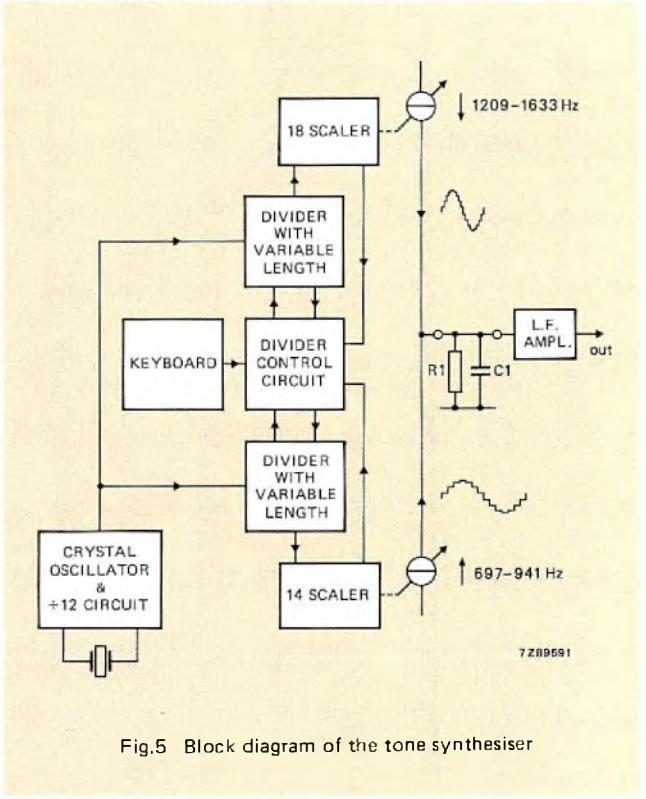


Fig.5 Block diagram of the tone synthesiser

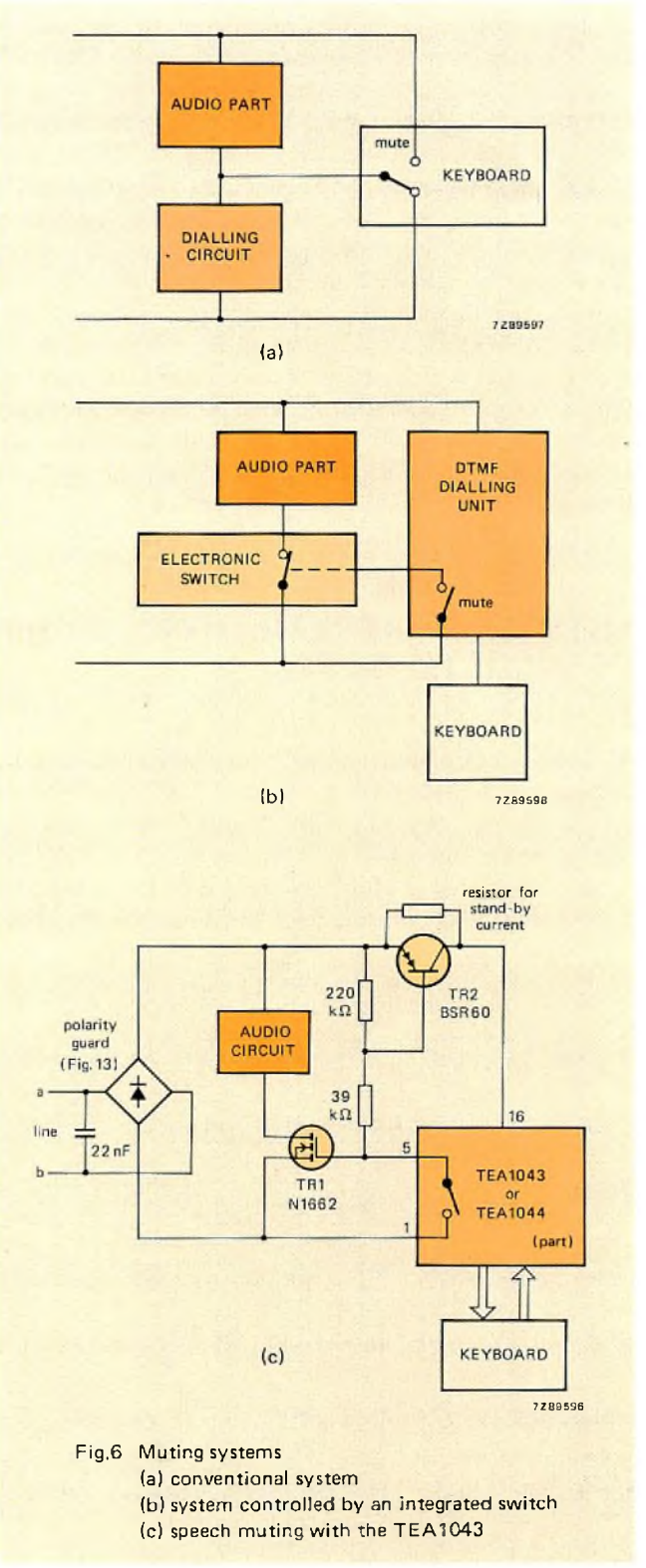


Fig.6 Muting systems
(a) conventional system
(b) system controlled by an integrated switch
(c) speech muting with the TEA1043

If the dialling circuit has a high impedance in the speech mode, it can be connected in parallel with the speech circuits as shown in Fig.6(b). The muting function can then be performed by an electronic switch in the dialling circuit. Fig.6(c) shows such an arrangement which can be used with the TEA1043 or TEA1044. Alternatively of course, the transistor switches in Fig.6(c) can be operated by using a common contact on the keyboard when using the TDA1077 or TEA1021 which do not have internal muting switches. In the circuit of Fig.6(c), pressing any keyboard pushbutton causes TR_1 to turn off and TR_2 to conduct, thereby connecting the dialling circuit to the lines and isolating the speech circuits. When dialling is not in progress, the dialling circuit is isolated but a resistor in parallel with TR_2 allows the passage of sufficient current to permit the keyboard scanning circuits to detect the pressing of a keyboard pushbutton. A 47 kΩ resistor is used if the voltage across the speech circuits is at least 3 V. If the voltage is less than 3 V, a lower value resistor must be used to provide a standby current of at least 50 μA. In the mute condition, the voltage across the dialling circuit is 0.7 V and its impedance is about 8 kΩ.

APPLICATION AND PERFORMANCE OF THE INTEGRATED CIRCUITS

Line matching

When there is an impedance match between the lines and the dialling circuit, the balance return loss is high and reflections on the line are highly damped. Figure 7 shows that the balance return loss when using any of the DTMF dialling circuits, connected to a line consisting of 600 Ω, or 900 Ω in parallel with 30 nF, is more than 14 dB over the frequency range 300 Hz to 3400 Hz as required by the CCITT. The variation of balance return loss with frequency is largely caused by an impedance variation due to the low-pass filter in the line adaptor and to the r.f.i. filter.

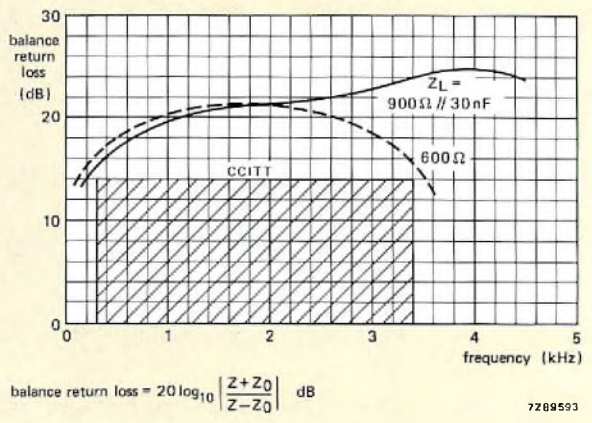


Fig.7 Balance return loss as a function of frequency

Since the highest line impedance that is likely to be encountered is 900 Ω, the internal impedance of the dialling circuits is set at this level and can be reduced to match lower impedance lines by adding an external resistor. In the TDA1077, the impedance is determined by two internal resistors in the line adaptor (R_2 and R_4 in Fig.2). The TEA1021, TEA1043 and TEA1044 have a low-impedance output stage which determines the impedance presented to the lines. In these circuits, the values of R_2 and R_4 are therefore higher than in the TDA1077 and there is a consequent reduction of current consumption. To reduce the impedance of the circuits to 600 Ω, it is necessary to connect a 2.7 kΩ resistor in parallel with the TDA1077, TEA1021 and TEA1043, or to connect a 240 Ω resistor between pin 6 of the TEA1044 and the negative supply line.

Reducing harmonic distortion

Since each cycle of the synthesised tone waveform is composed of eighteen square-wave steps for the higher frequency tone and fourteen steps for the lower frequency tone, a low-pass filter must be provided to attenuate harmonics above the 13th (lower frequency) or 17th (higher frequency).

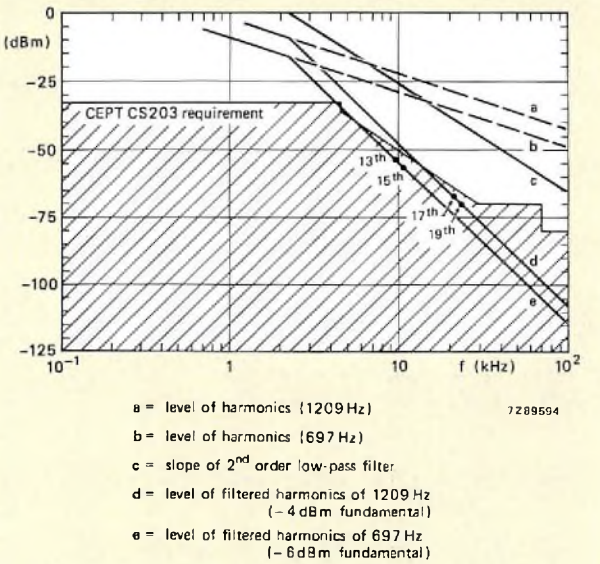


Fig.8 Harmonic content of the tones and the effect of filtering

The filter can be a simple first-order type consisting of a capacitor and resistor connected at the input to the output stage, or it can be a second-order active type using the internal output buffer as the active element. The type of filter chosen depends on the maximum acceptable level of harmonic distortion and on the cost of the required peripheral components and their assembly.

Specification CEPT CS203 requires that the level of tone harmonics in the speech band (300 Hz to 4300 Hz) does not exceed −33 dBm, and that this maximum level decreases by at least 12 dB per octave and does not exceed −70 dBm between 28 kHz and 70 kHz. At frequencies between 70 kHz and 200 kHz the level of any spurious signal should not exceed −80 dBm. This specification is shown by the shaded area of Fig.8 which also shows that a second-order low-pass filter will reduce the level of harmonics generated by any of the DTMF dialling circuits to the specified level. Figure 9 shows the dialling circuits with first-order filters for less stringent requirements, and Fig.10 shows the dialling circuits with second-order active filters. The frequency spectra are given in Fig.12(a) for circuits without a filter, in Fig.12(b) for circuits with a first-order passive filter, and in Fig.12(c) and (d) for circuits with a second-order active-filter.

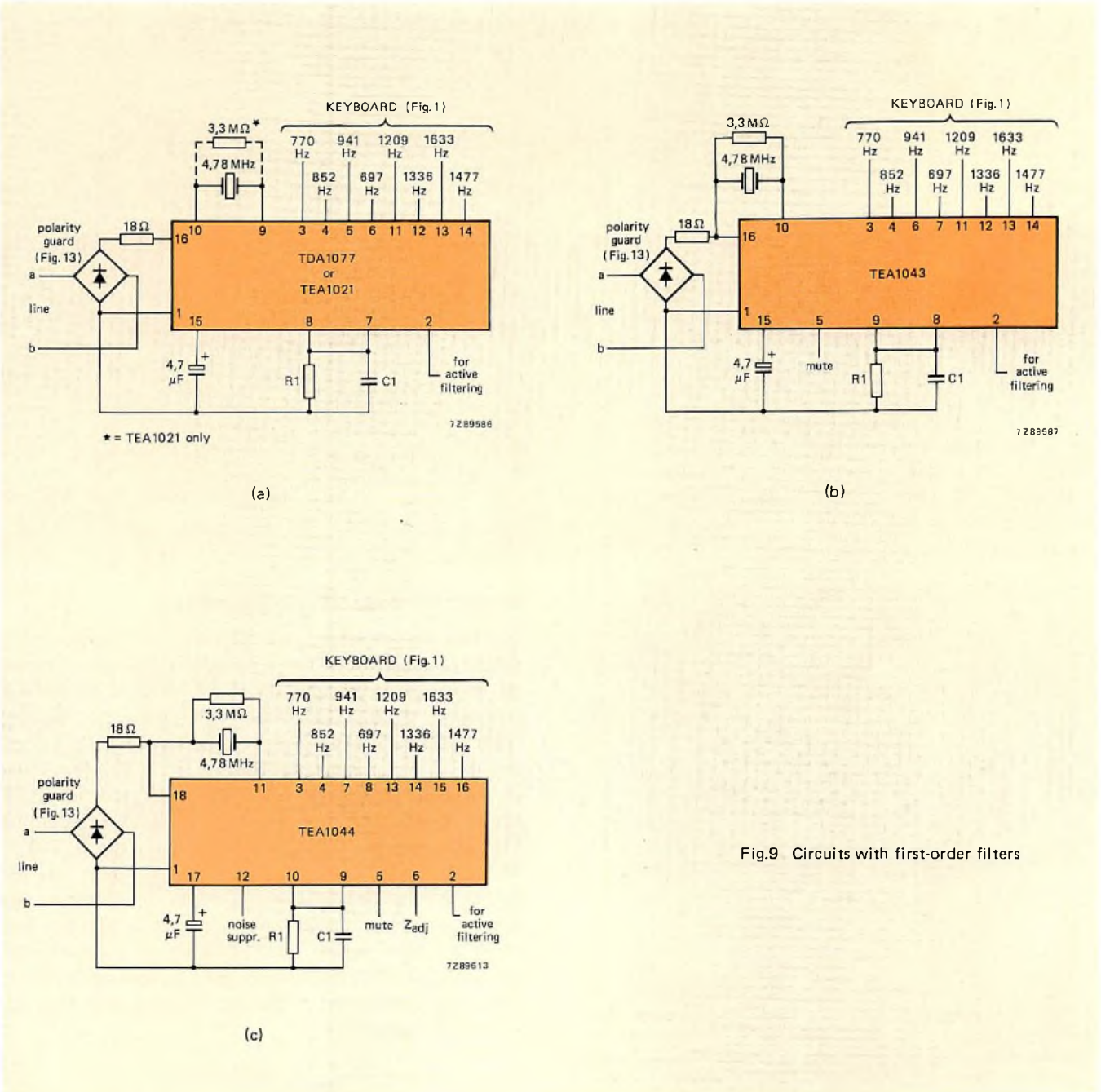


Fig.9 Circuits with first-order filters

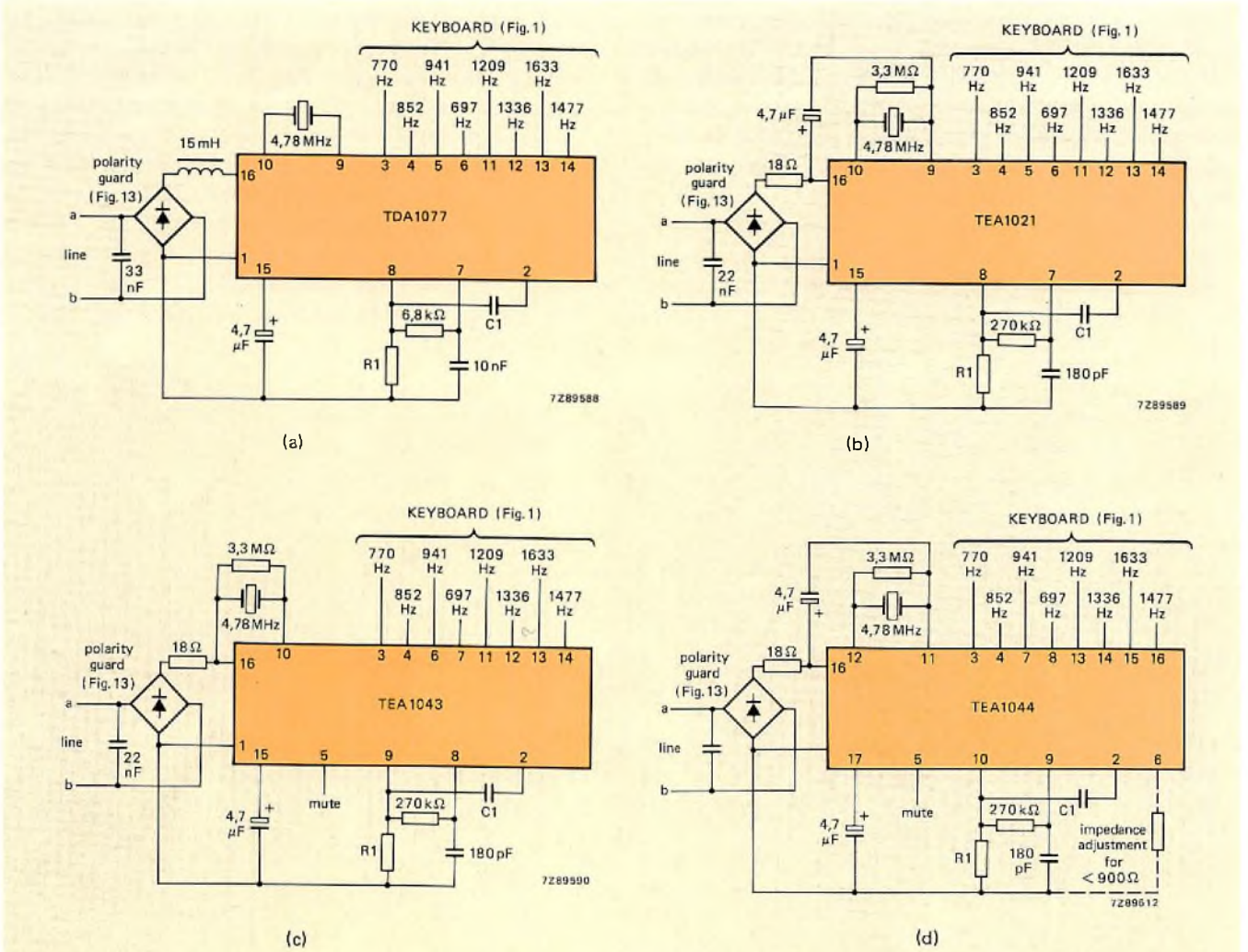


Fig.10 Circuits with second-order filters

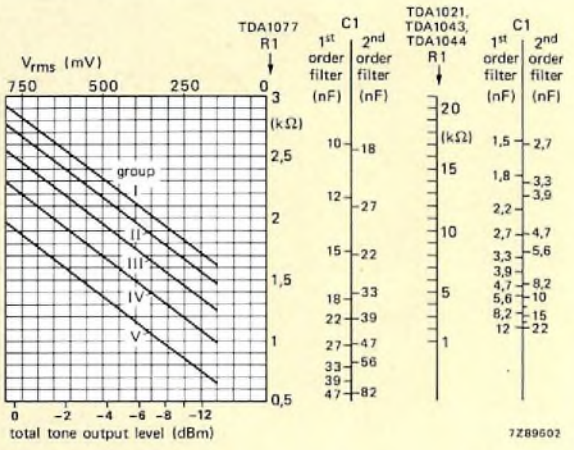


Fig.11 Tone output level adjustment for a dialling circuit with an impedance of 900Ω. If the impedance is changed to 600Ω with an external resistor, the value of R_1 read from the graph must be multiplied by 1.25 (TDA1077, TEA1021 and TEA1043) or divided by 1.54 (TEA1044)

Output level and filter adjustment

The tone output levels from all three dialling circuits are subject to some spread due to manufacturing tolerances and can be adjusted by selection of the value of the resistor connected to pin 8 (TDA1077 and TEA1021) or pin 9 (TEA1043) or pin 10 (TEA1044). The level of the higher-frequency tone, however, is always 2 dB ± 0.7 dB above that of the lower-frequency tone. The total production of circuits is therefore divided into five groups (1 to 5) for the TDA1077 and into three groups (2 to 4) for the TEA1021, TEA1043 and TEA1044. The group to which any IC belongs is identified by dots on the body of the circuit, the number of dots corresponding to the group number. The combined tone output level is shown as a function of resistor value with group number as a parameter in Fig.11. The output level shown in the graph is the amplitude of the combined tones given by

$$V_{out} = \sqrt{(V_1^2 + V_2^2)}$$

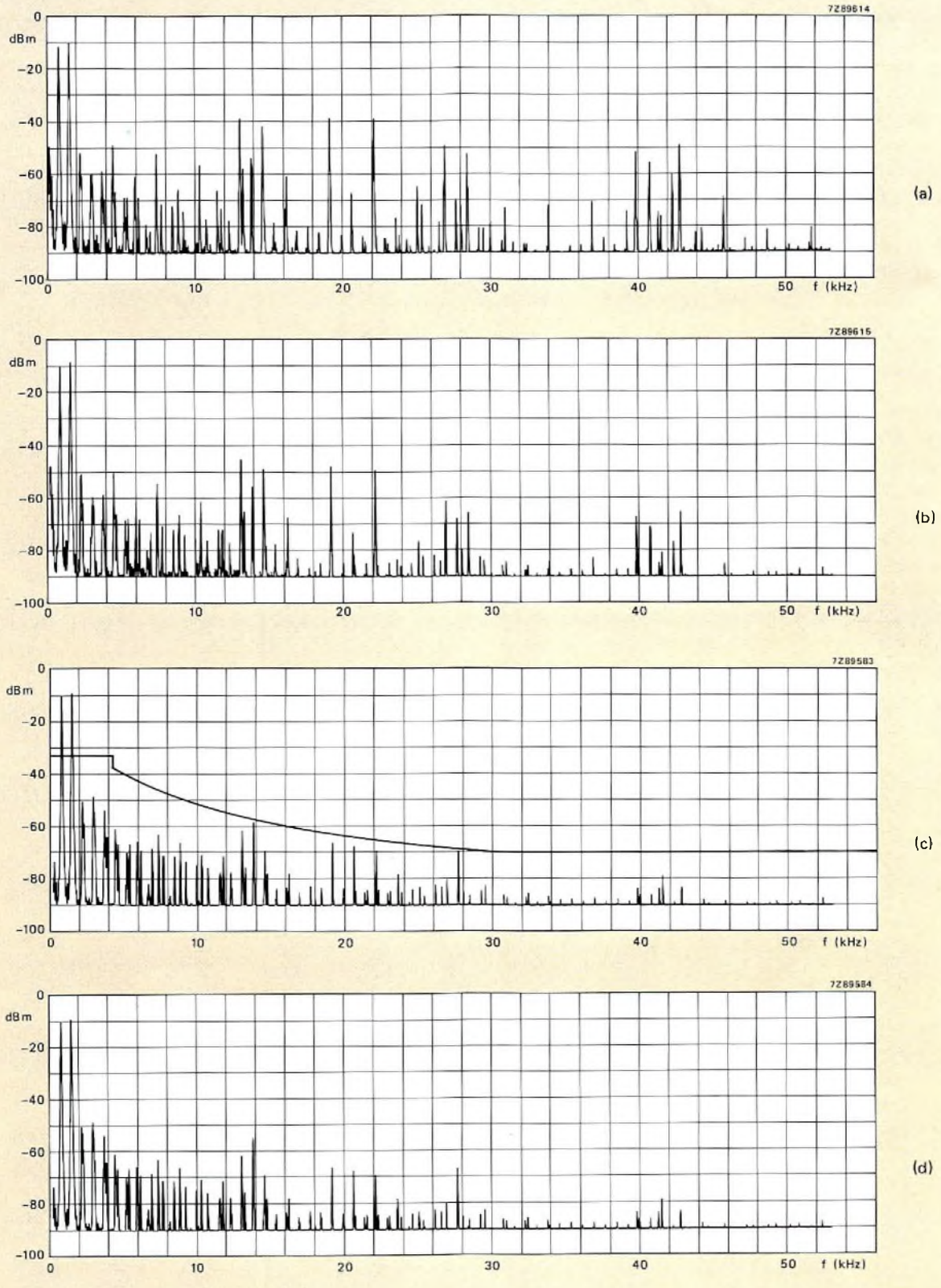


Fig.12 Frequency spectra
(a) All circuits without filter
(b) All circuits with first-order passive filter
(c) TDA1077, TEA1021 and TEA1044 with second-order active filter
(d) TEA1043 with second-order active filter

where V_1 is the amplitude of the lower-frequency tone and V_2 the amplitude of the higher-frequency tone; $V_2 = 1.26\,V_1$ i.e. $V_1 + 2$ dB. The measuring conditions for Fig.12 are line impedance 600Ω, line current 75 mA and ambient temperature 25 °C.

After the resistor value has been selected to obtain the required tone output level, the value of the filter capacitor connected to the same pin of the IC must be determined. For passive first-order filters, the time-constant (RC) must always be 26 μs. For active second-order filters, it must always be 46 μs. These values result in a maximum attenuation of ±0.3 dB in the passband of the filter due to the combined effect of ripple and component tolerances (R = ± 1%, C = ± 10%).

Polarity guard and suppression of line transients

Current surges in the telephone lines can cause voltages to be developed that are high enough to destroy the integrated dialling circuit. Figure 13 shows three methods of providing the necessary protection against these high voltage transients. Arrangement (c) is probably the most economical since the bridge rectifier is in any case essential to act as a polarity guard. In this circuit, the zener diodes function as normal diodes unless the voltage across the dialling circuit increases to the zener voltage. There are several possible configurations for arrangement (c) any of which are satisfactory as long as there is always one zener in series with each diode. An 18Ω

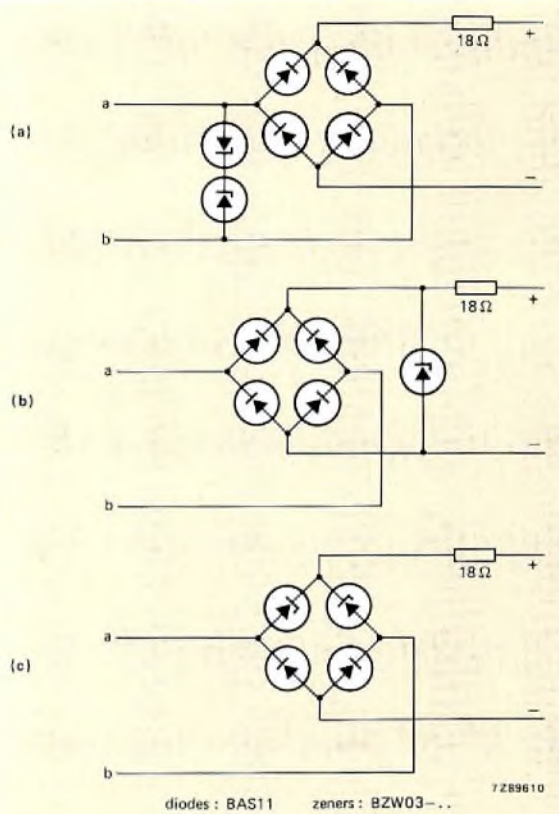


Fig.13 Polarity-guards and line-transient suppression circuits

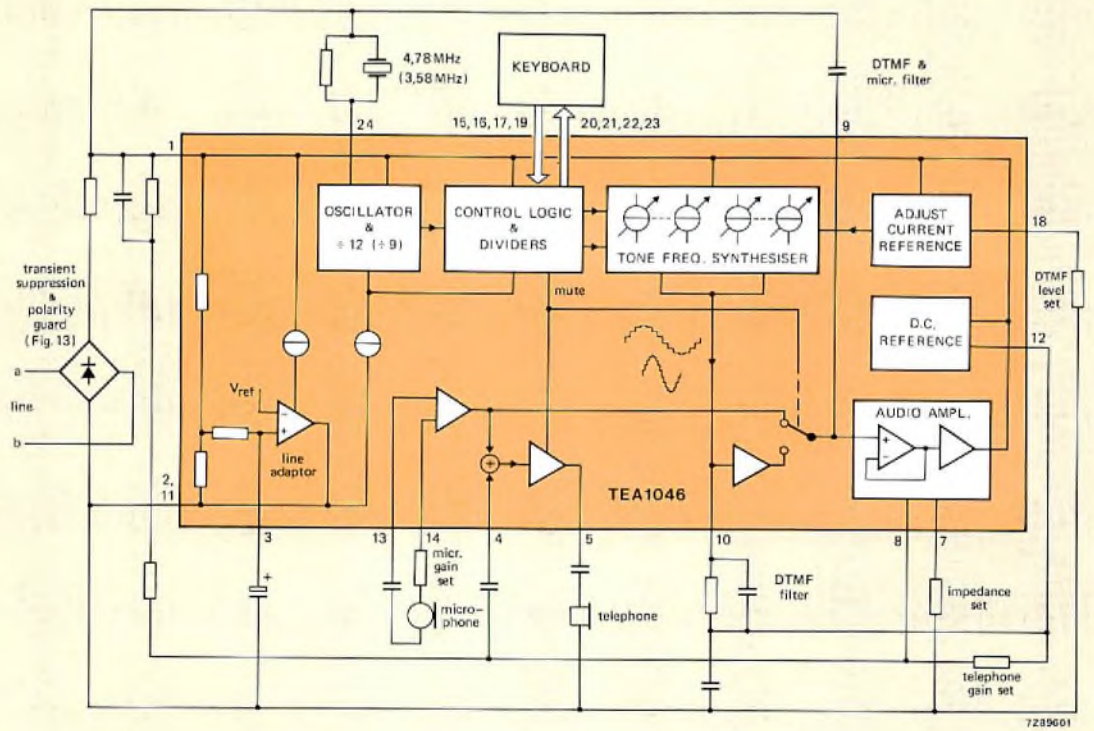


Fig.14 Block diagram of future dialling circuit TEA1046

current limiting resistor must be connected in series with the supply to the dialling circuit because the clamping voltage of the zener diodes can be as high as about 22 V in the event of high-level current surges.

RFI and noise suppression

In exceptional cases where the telephone is close to a source of r.f.i., the interference currents can cause incorrect operation. Dialling circuits without the r.f. filter at the input as shown in Fig.10 can tolerate about 2 mA (p-p) interference current within the frequency range 100 kHz to 30 MHz. With the r.f. filter circuit shown in Fig.10(a), the dialling circuit functions correctly with interference currents within the same frequency range but with a level of up to 60 mA superimposed on line currents of 15 mA to 120 mA (TDA1077) or 8 mA to 150 mA (TEA1021, TEA1043 and TEA1044). The capacitor connected between pins 9 and 16 of the TEA1021 circuit of Fig.10(b) suppresses interference from the logic circuits and from the DAC of the frequency synthesiser. The same function is performed by the capacitor connected between pins 12 and 18 of the TEA1044.

Automatic dialling

All the DTMF dialling circuits can be used for automatic dialling if the keyboard is replaced by, or paralleled with bilateral analogue switches (e.g. 2 x HEF4066B) or an analog multiplexer/demultiplexer (e.g. 2 x HEF4051B). This system can be used for repertory dialling, redial of last dialled number and rapid dialling in case of emergency.

FUTURE TRENDS

At present, DTMF dialling is only being introduced into existing telephone networks as new exchanges are required. Since the conversion/replacement of existing exchange dialling equipment and subscriber sets will take many years, it is envisaged that this will create an increasing world-wide demand for DTMF dialling circuits over the next ten years. During that period, we will be developing more comprehensive and higher performance DTMF dialling circuits. Typical of these circuits in development are the TEA1046 and the RO129.

DTMF dialling circuit TEA1046

This circuit, shown in Fig.14 contains the speech, supply and DTMF dialling functions on the same chip. For a basic subscriber set, the keyboard inputs are connected to a 4 x 4 pushbutton matrix. If extended dialling functions are required, a CMOS microcomputer can be connected directly to the same keyboard inputs. The circuit includes a microphone amplifier, the gain of which can be set by an external resistor so that it can be used with a dynamic (symmetrical) microphone or an electret (asymmetrical) microphone. A first-order low-pass filter at the output of the microphone amplifier acts as an additional filter for the dialling tones during dialling. The amplitude of the signal from the microphone amplifier to the telephone amplifier (sidetone) is reduced by a potential divider which is part of the anti-sidetone network.

Next generation DTMF dialling circuit

This is a second generation tone dialler that can be used in conjunction with either the present speech circuits or active circuits. Since all the muting functions are integrated, the circuit can be simply interfaced with the speech circuit. Additional dialling functions include register recall (flash) for use in PABX sets and redial of last number with up to 21 digits.

ACKNOWLEDGEMENT

The author wishes to acknowledge the assistance given by B. Defretin, D. J. G. Janssen and H. J. M. Otten during the preparation of this article.

Mains interruption is always inconvenient and can often be costly or dangerous. A back-up inverter fed by an accumulator can ensure continuity of supply to critical equipment. The one described here takes over instantly and matches the frequency and phase of the mains exactly.

PWM uninterruptable power supplies

L. HAMPSON

Uninterruptable power supply (UPS) systems have been developed for those electronic installations, especially computers and communication systems, which require a power supply unaffected by mains degradation or failure. This article describes a laboratory prototype UPS which has been designed to demonstrate the application of PWM techniques to UPS systems. The UPS is based on our Pulse Width Modulation (PWM) speed control system for a.c. motors (see Refs. 1 to 6), and is notable for its simple filter requirements and high efficiency. It has been designed in modular form using two modules: a PWM waveform generation module, type VM5000*, and a power supply and current sensing module, type VM5001*. The power ratings are 3 kVA (three-phase output) and 2 kVA (single-phase output), but the basic design can readily be extended to higher powers.

DESIGN OF A CONVENTIONAL UPS

A block diagram of a conventional UPS is shown in Fig.1. Power is normally taken from a three-phase mains supply, which is then rectified to provide a high-voltage d.c. link for an inverter. The switching elements of the inverter are usually thyristors switched at 50 Hz to give quasi-square waveforms. A filter removes harmonics from the inverter output, producing a sinewave input for the isolating transformer. This transformer isolates the load from the d.c. link and provides a standard mains voltage.

In the event of mains failure, power is taken from a battery supply connected across the d.c. link. Failure of the UPS itself is most unlikely, but should it occur a static switch supplies a.c. power direct from the mains to the load. The frequency and phase of the a.c. output waveforms are synchronised with the mains supply by means of a phase-locked loop system. This minimises any disturbance to the output voltage associated with the operation of the static switch. Current sensing and output voltage regulation systems are required, and the more sophisticated designs include a complex inverter triggering system which allows output voltage control from zero to full voltage.

UPS USING PWM

The laboratory prototype UPS described in this article has been constructed for demonstration purposes and comprises those sections of a conventional UPS enclosed within the broken line of Fig.1. By adding the sections lying outside the broken line, the prototype can be readily converted to a full commercial system.

As mentioned above, the prototype has been developed from our PWM a.c. motor speed control system (see Ref.1). At the heart of this system is a purpose-designed LSI circuit, type HEF4752V, which generates the PWM waveforms for a three-phase inverter. The output from the inverter consists of sinewave-weighted PWM voltage waveforms whose voltage and frequency can be controlled directly via the HEF4752V. The harmonic content of these waveforms is very low, so that the filter section of the UPS is only required to integrate the waveforms, in order to produce a sinewave output voltage to the load. A simple L-section lowpass filter can therefore be used. In contrast, the inverter output waveforms of a conventional quasi-squarewave UPS have a high harmonic content, necessitating the use of a complex filter design. Such

*For further information on these modules contact Mullard Ltd.

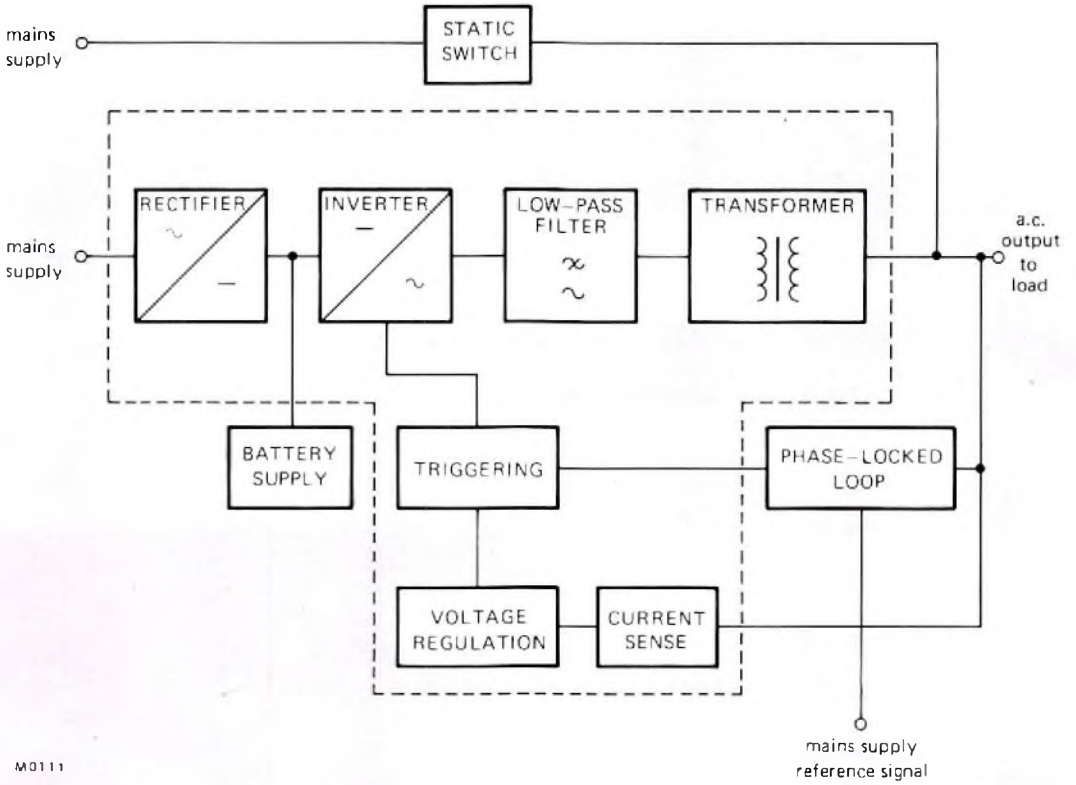


Fig.1 Block diagram of conventional UPS

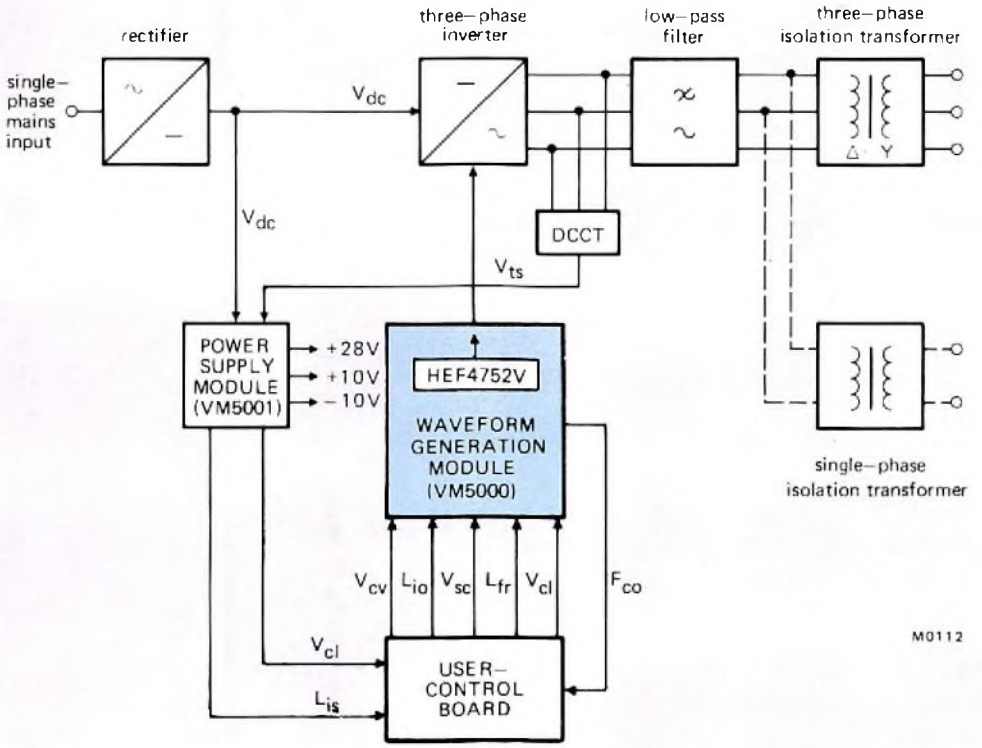


Fig.2 Block diagram of PWM UPS

filters are inevitably expensive and bulky, and although effective in removing harmonics from the output waveform, a corresponding proportion of the output power is lost as well. The essential justification for using PWM techniques in a UPS system is the consequent reduction in the requirements of the filter. With a simple filter, costs and volume are reduced, a better transient response is achieved, and the overall efficiency of the system improved. A block diagram of the PWM UPS is shown in Fig.2. It consists of the following sections.

1) Conventional rectifier/power supply for the d.c. link to the inverter
2) Three-phase inverter – the 12-thyristor auxiliary-commutated type described in Ref.2
3) Waveform generation and triggering system – the PWM waveform generation module
4) Three-phase current-sense circuit – using a DCCT transformer (Ref.3)
5) Low-voltage power supply for PWM waveform generation module and user-control circuits – located on the power supply module
6) Lowpass filter
7) User-control board
8) Isolation transformers

A general view of the UPS is shown in Fig.3a, and the lowpass filter and waveform generation and power supply modules are shown in Fig.3b.

The features of the UPS system which also appear in the PWM a.c. motor speed control system have been described extensively in earlier articles (Refs.1 to 6). This article therefore concentrates on those aspects which distinguish the UPS system from the a.c. motor speed control system, namely the filter, the user-control board, and the adjustments and modifications required by the waveform generation and power supply modules. The isolation transformers are standard types and are not described.

Power rating of UPS

Although UPS systems normally operate from a three-phase mains, such a supply is not always available. Thus for ease of demonstration, the UPS has been designed to operate from UK or European single-phase mains with nominal a.c. voltages of 240 or 220 V. Operating from the 220 V European mains, the following voltages and maximum power (kVA) ratings are available from the system.

D.C. link voltage

The d.c. link voltage V_{dc} is obtained by rectifying the a.c. mains supply. The value of V_{dc} for a choke input filter is given by:

$$V_{dc} = 220 \times \sqrt{2} \times \frac{2}{\pi} = 198 \text{ V}.$$

A standby battery of 200 V would thus be suitable for ensuring continuity of supply in the event of mains failure.

Output voltage from inverter

At full modulation and operating with a three-phase output, the line-to-line inverter output voltage V_{o3} is given by:

$$V_{o3} = \frac{V_{dc}}{2\sqrt{2}} \times \sqrt{3} = 121 \text{ V}.$$

With a single-phase output the inverter output voltage V_{o1} is given by:

$$V_{o1} = \frac{V_{dc}}{\sqrt{2}} = 140 \text{ V}.$$

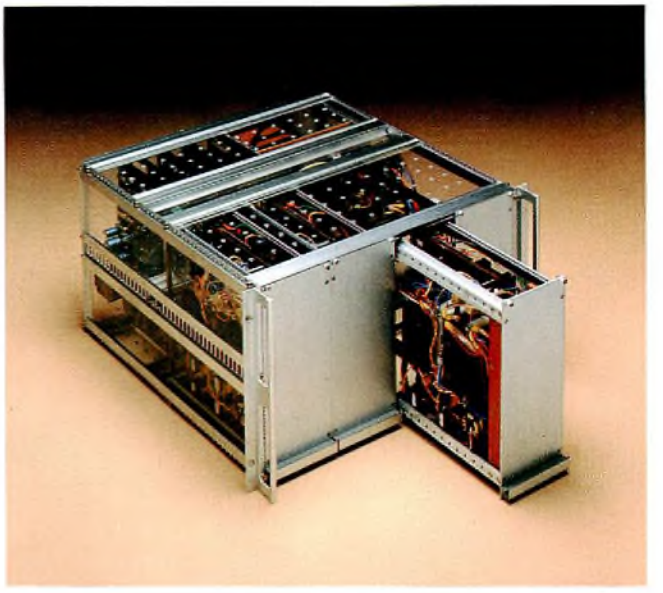


Fig.3a Laboratory prototype of PWM UPS, showing single phase of the three-phase inverter

Fig.3b UPS lowpass filter (left), power supply module (centre), waveform generation module (right)

Maximum power output from inverter

With a three-phase output the maximum output power from the inverter P_{o3} is given by:

$$P_{o3} = \sqrt{3} \times V_{o3} \times I_{T(AV)} \times \frac{\pi}{\sqrt{2}}$$

where $I_{T(AV)}$ is the average on-state current of the inverter switching elements. In the inverter circuit of the UPS laboratory prototype, the switching elements are BT155 type ASCRs, with a value of $I_{T(AV)}$ equal to 6.5 A (mounting-base temperature 85°C). The three-phase output power is thus:

$$P_{o3} = \sqrt{3} \times 121 \times 6.5 \times \frac{\pi}{\sqrt{2}} = 3.0 \text{ kVA}.$$

For a single-phase output the maximum output power of the inverter P_{o1} is given by:

$$P_{o1} = V_{o1} \times I_{T(AV)} \times \frac{\pi}{\sqrt{2}}$$

$$= 140 \times 6.5 \times \frac{\pi}{\sqrt{2}} = 2.0 \text{ kVA}.$$

If the BT155s are replaced by BTW63s, average on-state current 22 A, then P_{o3} and P_{o1} are 10.2 and 6.8 kVA respectively.

Three-phase filter

The small-signal response of an L-section lowpass filter is defined by the cut-off frequency f_{co} and the damping factor δ. If L and C are the inductance and capacitance of the filter and R_L is the load resistance per phase, then:

$$f_{co} = \frac{1}{2\pi\sqrt{(LC)}} \quad (1)$$

and:

$$\delta \simeq \frac{1}{2\sqrt{(LC)}} \left(\frac{L}{R_L}\right) \quad (2)$$

To minimise the cost of the filter components, it is desirable that the cut-off frequency should be as high as possible. For the PWM UPS system, an acceptable sinewave output voltage (high-frequency ripple <5%) is obtained with a filter having a cut-off frequency of about one-fifth of the inverter switching frequency. The number of pulses per cycle of the output waveform can be 15, 21, or 30 (see Ref.4), with corresponding inverter switching frequencies of 750, 1050, and 1500 Hz. Although a switching frequency of 1500 Hz would correspond to the highest filter cut-off frequency, it would also maximise the inverter switching losses. The UPS is thus operated at an inverter switching frequency of 1050 Hz.

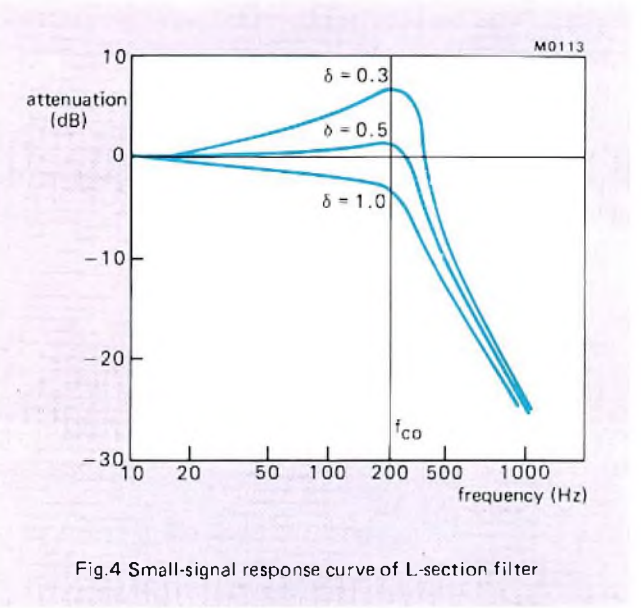


Fig.4 Small-signal response curve of L-section filter

This gives an acceptable level of inverter switching losses and a filter cut-off frequency of about 200 Hz.

The small-signal response curve of an L-section filter with a cut-off frequency of 200 Hz is shown in Fig.4. The filter has a typical attenuation of 12 dB per octave above the cut-off frequency and a lowpass characteristic below the cut-off frequency. The output frequency (50 Hz) is located on the lowpass section, and the switching frequency and sidebands are on the attenuation curve.

For given values of R_L and δ, the required inductance and capacitance of the filter can be calculated from Eqs.1 and 2. With a phase voltage of 70 V and a nominal maximum power output of 2.5 kVA, the value of R_L is approximately 6 Ω. If a value of δ equal to 0.6 is selected, then L and C can be calculated as 5.7 mH and 110 μF respectively.

A single phase of the filter is shown in Fig.5, and the input and output voltage waveforms are shown in Fig.6. The capacitor network is balanced across the inverter output so that, in principle, there is no reversal of d.c. voltage across the capacitors. This arrangement permits the use of electrolytic types, giving a compact low-cost design. A small catching diode (type BAS11) is placed across each capacitor to ensure that any reverse voltages are less than the permitted limit. Forward voltage drops across the capacitors are equalised by voltage-sharing resistors. Since the two arms of the filter are effectively in parallel, the capacitance of each arm must be approximately 50 μF.

Because of the high ripple currents associated with this application, the use of correctly rated capacitors is essential if a predictable service life is to be achieved. The 115 types used in the filter design are characterised by their high ripple current ratings, and are thus an ideal choice. Referring to Fig.7, it can be seen that the capacitor ripple current consists of two components: a low-frequency (50 Hz) ripple I_{50} corresponding to the a.c. output frequency of the UPS, and a

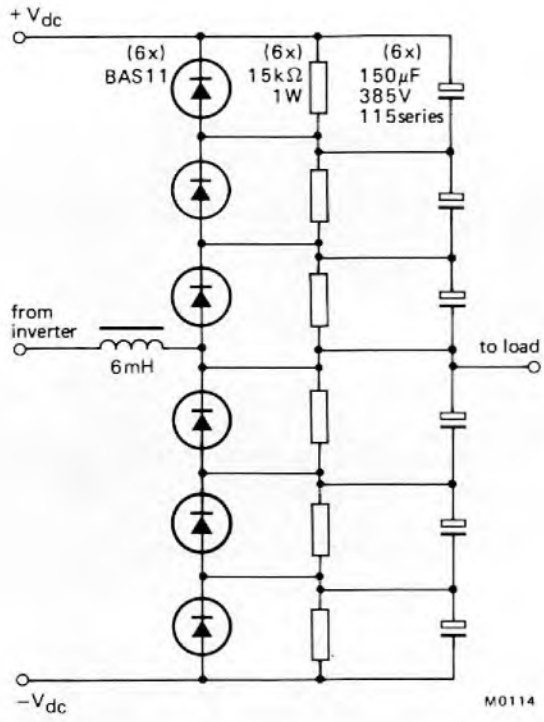


Fig.5 Single phase of L-section filter

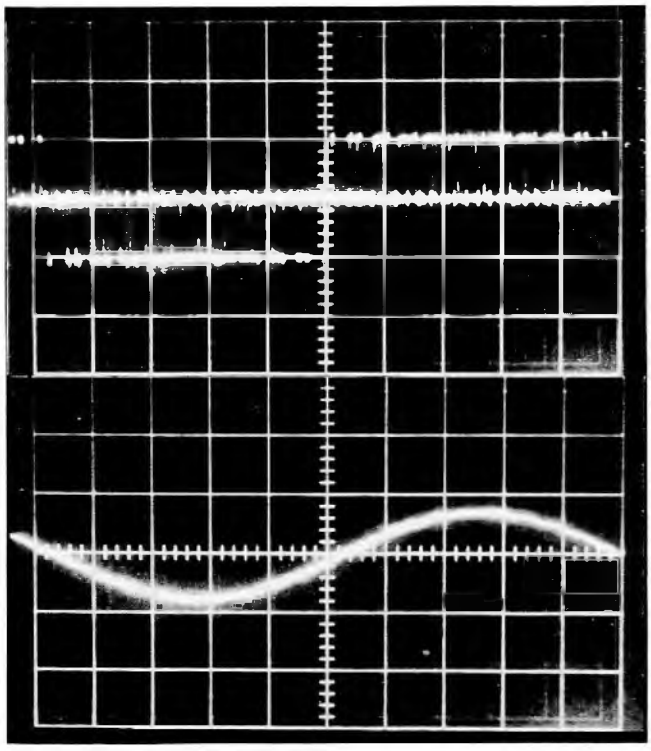


Fig.6 Lowpass filter 50 Hz line-to-line voltage waveforms
upper trace — input voltage
lower trace — output voltage
Vertical scale : 200 V / div

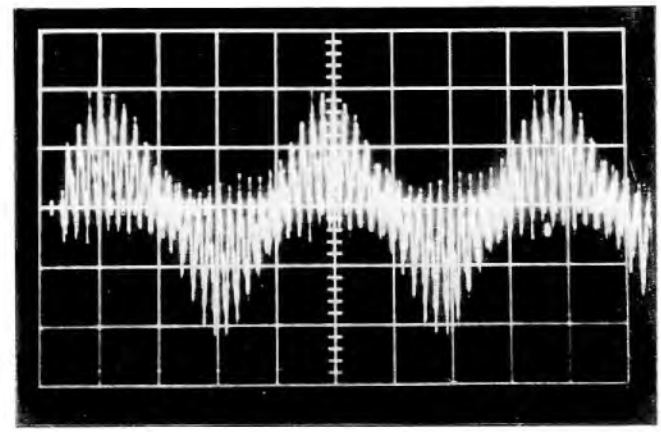


Fig.7 Lowpass filter capacitor ripple current waveform
Vertical scale : 2 A / div

high-frequency (1050 Hz) ripple I_{1050} produced by the switching frequency of the inverter. The total r.m.s. value of the capacitor ripple current I_{cap} can be expressed as the sum of these two components:

$$I_{cap} = \sqrt{\left\{\left(\frac{2\pi \times 50 \times C \times V_{dc}}{2\sqrt{2}}\right)^2 + \left(\frac{I_{pk\text{-}pk}}{2\sqrt{3}}\right)^2\right\}}, \quad (3)$$

low-frequency component (I_{50}) — high-frequency component (I_{1050})

where $I_{pk\text{-}pk}$ is the mean peak-to-peak value of the high-frequency ripple current over a 50 Hz cycle assuming a triangular waveform. To select a capacitor with a suitable ripple current rating, the values of the two components of I_{cap} must be known. The low-frequency component can be calculated directly as 1.1 A; however, before the high-frequency component can be evaluated, $I_{pk\text{-}pk}$ must be determined. The value of $I_{pk\text{-}pk}$ may be estimated from Fig.7 or alternatively, I_{cap} can be measured with a true r.m.s. meter and $I_{pk\text{-}pk}$ can then be calculated from Eq. 3. Using the latter approach the high-frequency component is found to be 1.1 A.

The rated ripple currents for the 115-series capacitors are standardised at a frequency of 100 Hz and at an ambient temperature of 85°C. The 100 Hz ripple current I_r which is equivalent to the 50 and 1050 Hz components present in the filter is given by:

$$I_r = \sqrt{\left(\frac{I_{50}^2}{r_{50}} + \frac{I_{1050}^2}{r_{1050}}\right)} \quad (4)$$

where $\sqrt{r_{50}}$ and $\sqrt{r_{1050}}$ are the appropriate frequency multiplying factors (see published data; also Ref.6). Thus:

$$I_r = \sqrt{\left(\frac{1.1^2}{0.83^2} + \frac{1.1^2}{1.19^2}\right)} = 1.62 \text{ A}.$$

From the 115-series data, the ripple current rating (100 Hz, 85°C) of a 150 μF capacitor is 1.2 A. The life expectancy of an electrolytic capacitor is determined principally by its core temperature, and the 115-series capacitors are designed to operate at a maximum core temperature of 95°C, corresponding to a life expectancy of 10 000 h. A 150 μF capacitor operated at an ambient temperature of 85°C, with a 100 Hz ripple current of 1.2 A, will have a core temperature of 95°C and thus a life expectancy of 10 000 h. By reducing the core temperature the life expectancy can be extended, an increase by a factor of 2 being achieved for each 10°C reduction in the core temperature. Thus for a core temperature θ:

$$\text{life expectancy} = 10\,000 \times 2^{n}, \qquad (5)$$

where:

$$n = \frac{95-\theta}{10}.$$

If an ambient temperature of 50°C is assumed, then a 150 μF capacitor operated with a 100 Hz ripple current of 1.62 A will have a core temperature given by:

$$\theta = 50 + 10\left(\frac{1.62}{1.2}\right)^{2} = 68^{\circ}\text{C}. \qquad (6)$$

Full details of the origin of Eq.6 are given in Ref.6. For θ = 68°C, n = 2.7, and substituting this value into Eq.5, a life expectancy of 65 000 h is obtained. The 115-series 150 μF capacitor is thus well suited to this application. If a longer life expectancy is required, then the capacitor ripple current must be reduced by using series/parallel networks.

The filter chokes are wound on 'Telcon' steel strip cores operating at a maximum flux density of 1500 mT. Each winding consists of 90 turns of bifilar wound 2 X 1.8 mm enamelled copper wire. Because of the required value of the inductance and the peak value of the line current, a ferrite core cannot be used because the filter would become unacceptably large and costly.

PWM waveform generation module

The primary function of the waveform generation module (see Fig.8) is to generate the PWM waveforms and produce isolated trigger pulses for the 12-thyristor inverter. The module is able to vary the output frequency, change the output voltage at a given frequency, and implement a range of user-control functions. A full description of the facilities of the module is given in published data. In the PWM UPS system the module is required to perform the following functions.

- Set the output frequency to 50 Hz
- Set the nominal a.c. output voltage of the UPS
- Implement current limiting through voltage control
- Implement voltage regulation with variations in load

Clock setting

The operation of the module is principally defined by four clock inputs to the PWM IC HEF4752V, and by the components and connections in a program plug. The numbers within circles on Fig.8 indicate the pin numbers of the program plug. The four clock inputs F_{cf}, F_{cv}, F_{cr}, and F_{co} have the following functions.

- F_{cf} determines the output frequency of the PWM waveforms
- F_{cv} determines the output voltage at a given output frequency
- F_{cr} sets the maximum switching frequency for the inverter
- F_{co} sets the interlock delay period required at the changeover between the upper and lower main thyristors in each phase of the inverter

The clock input F_{cf} is set by V_{sc}, the d.c. input to a voltage-controlled oscillator, in conjunction with capacitors C1 and C2 on the program plug. A second d.c. voltage V_{cv}, also the input to a voltage-controlled oscillator, sets F_{cv}. The clock inputs F_{cr} and F_{co} are fixed by the resistor values R2 and R1 on the program plug. For a given application, the required values of the four clock inputs are determined by the inverter output frequency, the nominal output voltage, the maximum switching frequency of the inverter, and the interlock delay period. For the prototype UPS system, these are respectively 50 Hz, 120 V, 1050 Hz, and 40 μs. Following the approach set out in the waveform generation module data, it can be shown that the corresponding value of V_{sc} is −8 V, with C1 + C2 = 470 pF, that V_{cv} = −3.9 V, and that R2 and R1 are 9.83 kΩ and 6.2 kΩ respectively.

Load current limiting

The load current limiting function of the waveform generation module is implemented via the V_{cl} input. This input voltage, derived from the power supply module (see below), is proportional to the sum of the moduli of the three-phase load currents. Below a preset value, V_{cl} has no effect on the system; however, once the preset value is exceeded, the frequency of F_{cv} is increased rapidly to a maximum of about 3 MHz. The output voltage is inversely proportional to F_{cv}, so that this sudden increase in F_{cv} causes a corresponding rapid fall in the output voltage, and a consequent limitation of the load current.

Voltage regulation

Regulation of the output voltage (below the trigger level for V_{cl}) is achieved via the V_{cv} input. A circuit on the user-control board (see below) causes the value of V_{cv} (nominally −3.9 V) to tend towards zero as the load current is increased, and to become more negative as the load current falls. Since the output voltage varies inversely with the

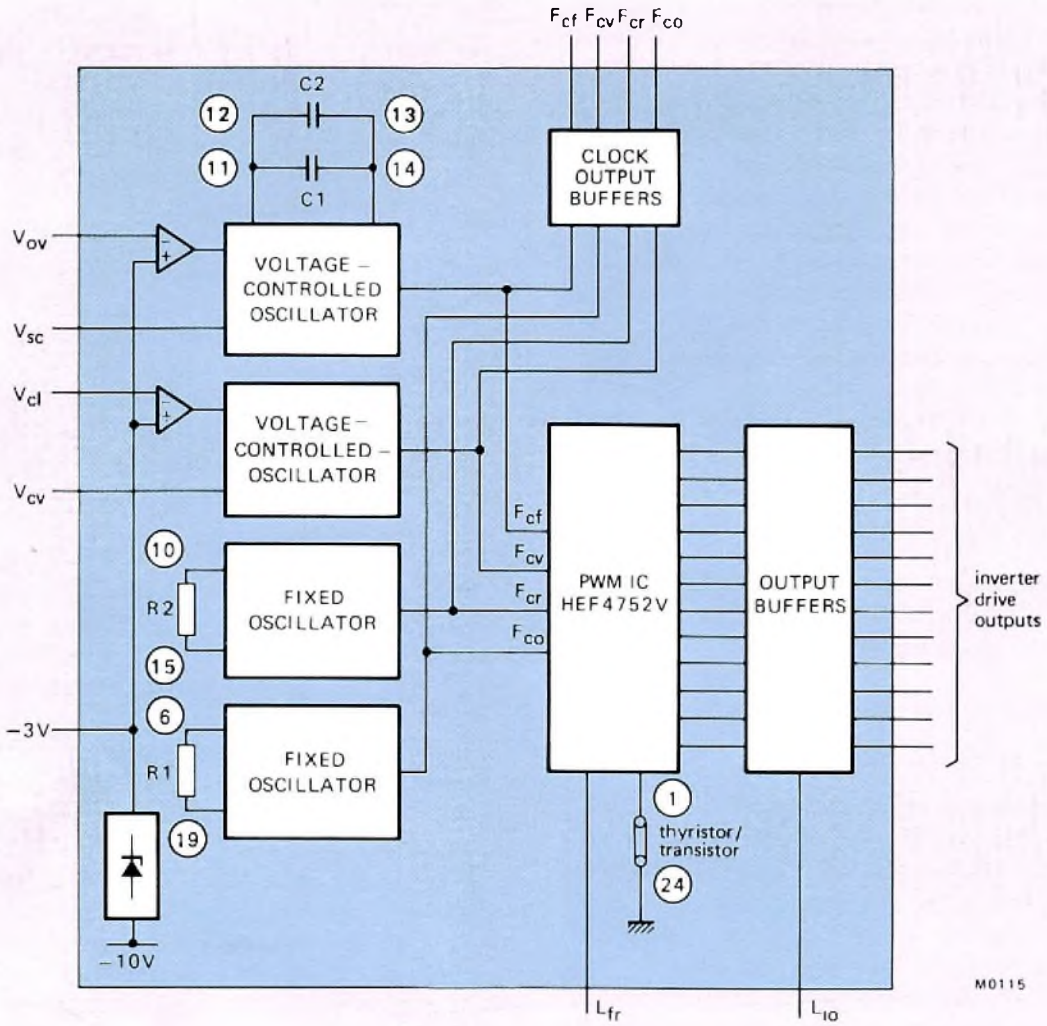


Fig.8 Block diagram of PWM waveform generation module

absolute value of V_{cv}, this will result in a regulated output voltage with variations in load current.

The voltage regulation system compensates for voltage drops in the inverter and filter section. Compensation for changes in the d.c. link voltage can be achieved via the V_{lv} connection on the power supply module.

Modification of trigger pulse frequency

The normal trigger pulse train for the main thyristors has a frequency equal to the inverse of the interlock delay period, which for an interlock delay of 40 μs corresponds to 25 kHz. While this is satisfactory for the inverter of an a.c. motor speed control system, it is too low for the UPS and, if used, would result in latching problems at the zero cross-overs of the load currents. The difficulty arises because of the inductive load of the filter and the relatively low value of the BT155 snubber capacitors. To obtain a higher trigger pulse frequency, the module is set-up for the transistor mode of operation by interconnecting pins 1 and 24 on the program plug (replacing the trigger pulse train by a block pulse), and the main drive ouput-enable signal L_{io} is chopped at a frequency of F_{co}. The L_{io} signal is chopped via a gating circuit on the user-control board.

Conversion to single-phase operation

The UPS may be readily converted from a three-phase to single-phase output. To operate the UPS in the single-phase mode, the trigger pulses for the upper thyristors in the Y-phase are replaced by the trigger pulses for the lower thyristors in the R-phase, and similarly the Y-phase lower thyristors are driven by the trigger pulses for the upper thyristors in the R-phase. The change between three- and single-phase operation is effected by a 4-pole 2-way dual-in-line switch on the waveform generation module connected

between the current sinking diodes and the output driver transistors; see Fig.9. In the single-phase mode, the B-phase should either be switched out from the d.c. link or may be left operating in a redundant mode but disconnected from the external load.

Power supply and current-sensing module

In the UPS system, the power supply and current-sensing module provides low-voltage power supplies for the waveform generation module and user-control board, a logic signal L_{is} which enables/disables the complete system at switch-on and switch-off, and an isolated signal V_{cl} proportional to the sum of the moduli of the three-phase load currents. The V_{cl} signal is derived in conjunction with an external DCCT system; see Fig.2. A full description of the module is given in published data; see also Ref.5.

User-control board

The user-control board (see Fig.10) includes the following facilities.

- Soft-start circuit
- Output voltage regulation circuit
- Gating circuit for generating the chopped L_{io} signal
- Potentiometer control for V_{sc}
- Phase reversal switch

Soft-start circuit

This circuit ensures a reduced output voltage at start-up. Under established operating conditions (soft-start switch in position 1 and transistor TR1 off), V_{cv} is set to −3.9 V by VR2, and F_{cv} will be equal to 347 kHz giving the UPS a nominal three-phase output voltage of 120 V. In position 2 of the soft-start switch (corresponding to stop), TR1 is saturated, thus clamping V_{cv} to the −10 V supply line and setting the F_{cv} clock to approximately 820 kHz. At start-up, this high value of F_{cv} gives the UPS an initial output voltage of about half the nominal operating value.

Output voltage regulation circuit

The current-sensing voltage V_{cl} is directly proportional to the load current. As the load current rises, the increasing value of V_{cl} will cause the positive voltage across VR1 to rise, thereby causing V_{cv} (nominally −3.9 V) to tend towards zero. Conversely, a falling load current will make V_{cv} more negative. Output voltage regulation with changes in load current is thus readily achieved, the degree of compensation being adjustable via VR1. Figure 11 shows the variation of output voltage with d.c. link current. In the compensated curve of Fig.11, VR1 has been set to give a degree of overcompensation, illustrating the range of control available.

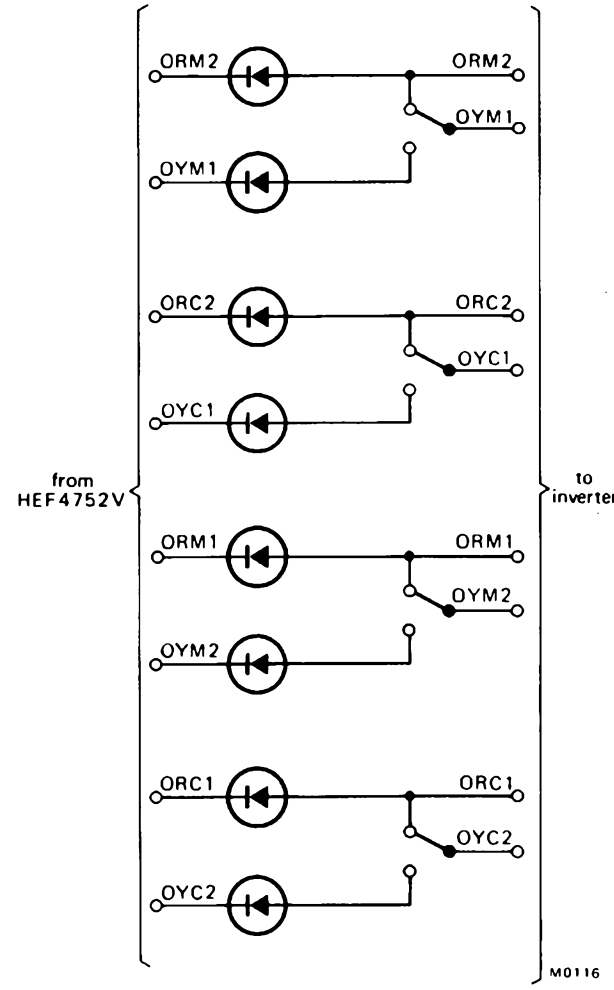


Fig.9 Three-phase to single-phase conversion; switch shown in single-phase position

Gating circuit

The F_{co} clock signal from the clock output buffers on the waveform generation module is used as a high-frequency chopping signal to generate high-frequency trigger pulses for the thyristor gates. The signal is gated with the L_{is} (start-up delay) logic signal via IC1, and the gate output signal is used as the L_{io} input for the waveform generation module.

Output frequency setting and phase reversal

The output frequency of the UPS is set by the negative d.c. control voltage on the V_{sc} input of the waveform generation module. The value of V_{sc} is set by a simple ten-turn potentiometer VR3 on the user-control board. If required, the phase sequence of the outputs in the three-phase mode can be reversed by switching the L_{fr} signal; see Fig.10.

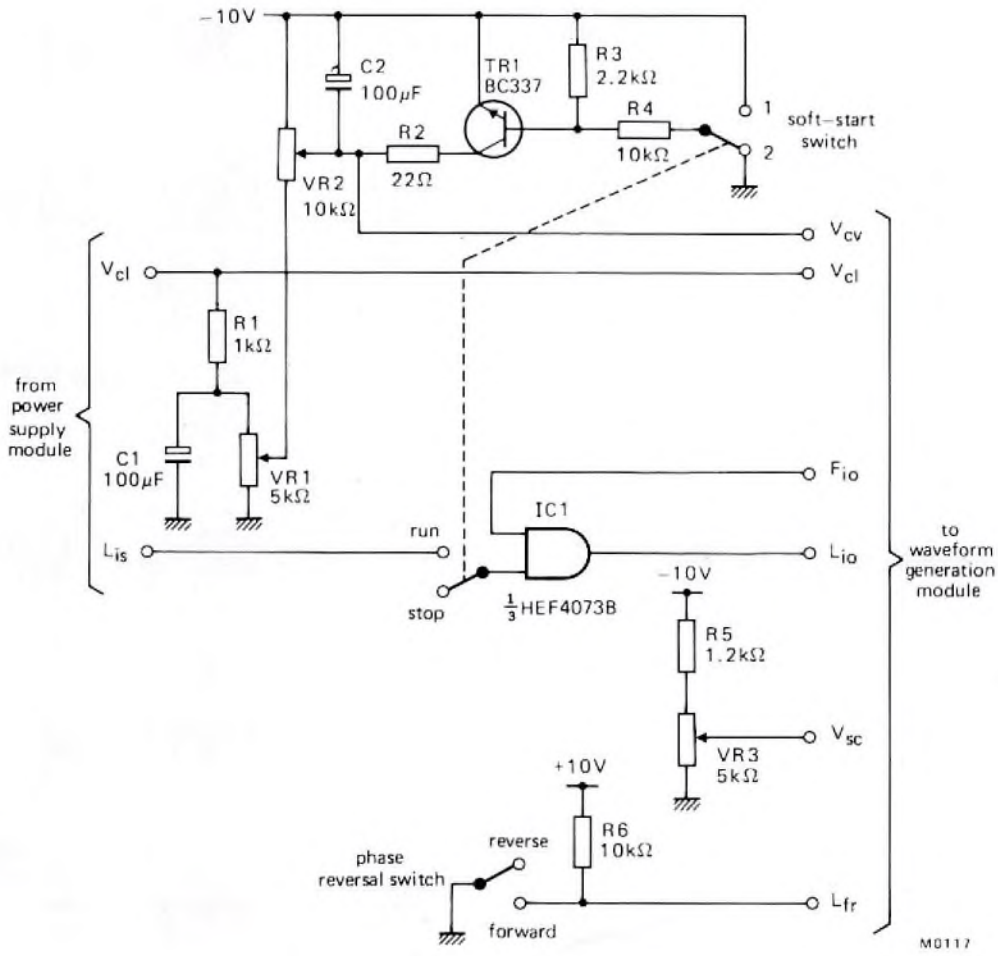


Fig.10 User-control board

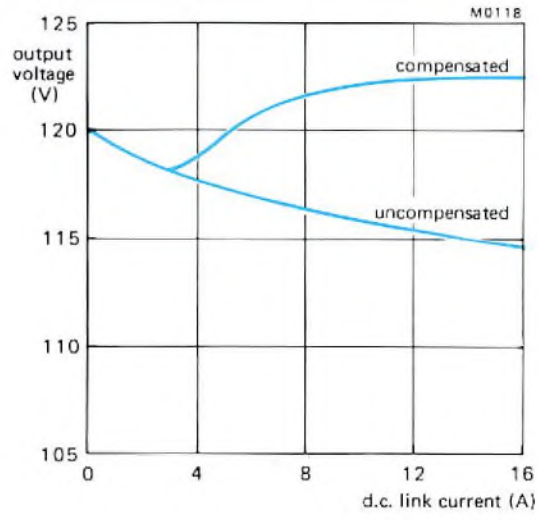


Fig.11 Output voltage versus d.c. link current

Performance of UPS

Output voltage and current

Waveforms of three-phase line-to-line output voltage and current for zero-load, half-load, and full-load current are shown in Fig.12. The full-load current condition corresponds to a load of approximately 2.5 kW. The residual ripple on the voltage waveforms, caused by the individual PWM pulses, is comparable with currently available commercial quasi-squarewave units. Similar waveforms are obtained for a single-phase output, although as previously indicated the output voltage is increased by a factor of $2/\sqrt{3}$.

Efficiency

The efficiency of the PWM UPS system can be evaluated by measuring the power in a resistive load, relative to the d.c. link input power. The results for a three-phase load are shown in Table 1, and those for a single-phase load are shown in Table 2.

TABLE 1

Efficiency of UPS system with three-phase resistive load

Load condition as a percentage of full load %	D.C. input power W	Three-phase a.c. power to load W	Efficiency %
100	2656	2550	96
50	1330	1210	91
25	738	650	88

TABLE 2

Efficiency of UPS system with single-phase resistive load

Load condition as a percentage of full load %	D.C. input power W	Single-phase a.c. power to load W	Efficiency %
100	1947	1850	95
50	950	855	90

Transient response with load switching

The transient response of the UPS has been tested under two conditions: half load to full load switching, and full load to half load switching. The resulting voltage waveforms are shown in Fig.13. In the half to full load switch, the disturbance on the voltage waveform is shown at the fifth cycle, and on the full to half load switch the disturbance occurs at the sixth cycle. In both cases the maximum disturbance is only about 30% of the peak value of the voltage waveform, well within current commercial requirements.

Total harmonic distortion

The total harmonic distortion for load conditions varying from zero load to full load is less than 3%. The harmonic content of the PWM waveform is the least significant component in this figure. The main contribution comes from the ripple on the d.c. link, with an additional but smaller contribution being made by the filter.

Load power factor

Initial testing has shown that the UPS will meet normal commercial requirements by working into loads with power factors of 0.8 to unity.

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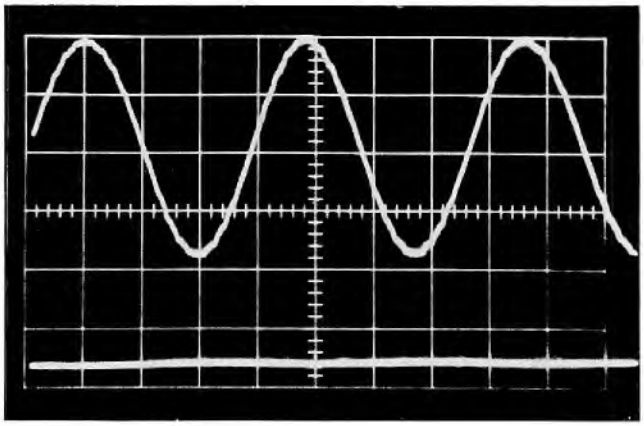
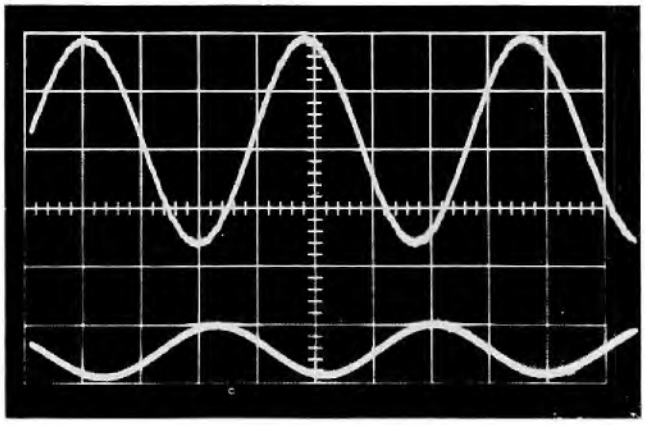
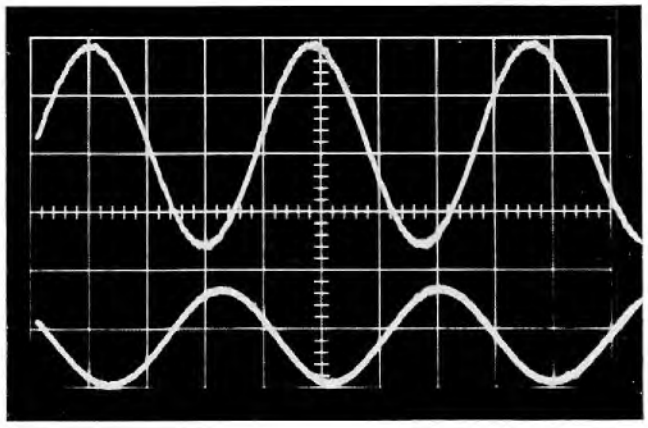


(a)

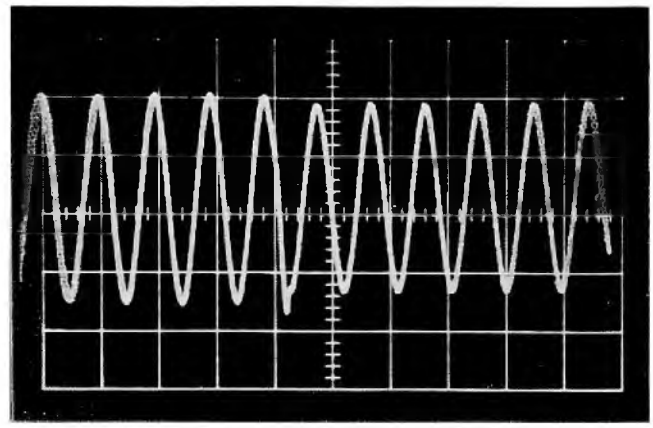


(b)

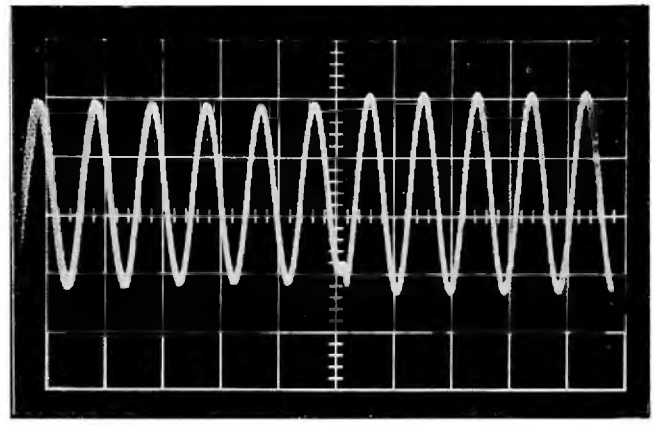


(c)

◁ Fig.12 Line-to-line voltage (upper trace) and line current (lower trace)
(a) zero load (b) half load (c) full load
Vertical scale: 100 V / div (upper trace)
20A / div (lower trace)



(a)



(b)

△ Fig.13 Transient response of UPS to 50% load change
(a) half to full load switching
(b) full to half load switching
Vertical scale : 100 V / div

If you can't justify the expense of a custom chip, and combinations of random logic make your design too cumbersome or complex, integrated fuse logic may be the answer. It enables you to configure an off-the-shelf chip to do a custom job. What's more, it doesn't penalise you for having second thoughts about design details.

New developments in integrated fuse logic

K. A. H. NOACH

Custom logic is expensive – too expensive if your production run is short. 'Random logic' is cheaper but occupies more sockets and board space. Integrated Fuse Logic bridges the gap. Using IFL, you can configure an off-the-shelf chip to perform just the logic functions you need. Design and development times are much shorter, and risk much lower, than for custom logic. Connections are fewer than for random logic and, for all but the simplest functions, propagation delay is usually shorter. Yet another advantage that IFL has over custom logic is that it allows you to redesign the functions without redesigning the chip – giving you an invaluable margin not only for cut-and-try during system development but also for later revision of system design. You're not tied down by the need to recover capital invested in a custom chip.

An IFL chip is an array of logic elements – gates, inverters, and flip-flops, for instance. In the virgin state everything is connected to everything else by nichrome fuses and, although the chip has the capacity to perform an extensive variety of logic functions, it doesn't have the ability to. What gives it that is programming: selectively blowing undesired fuses so that those that remain provide the interconnections necessary for the required functions.

Signetics Series 20 IFL, named for the number of pins, supplements the well-known Series 28. The package is smaller – little more than a third the size, in fact – but the improved architecture, with user-programmable shared I/O, compensates for the fewer pins. The series comprises the following members, in order of increasing complexity:

- 82S150/82S151 – field-programmable gate array
- 82S152/82S153 – field-programmable logic array
- 82S154/82S159 – field-programmable logic sequencer

The even-numbered types have open-collector, and the odd-numbered types three-state outputs.

Entry to all the devices is via a product matrix, an array of input and shared I/O lines fuse-connected to the multiple inputs of an array of AND gates (see Fig. 1, 2 and 6). To exploit the capacity of any device it is important to make the most economical use of the AND gates it has available. Application of the Morgan's theorem can help in this. For example, inputs for the function

$$F = A + B + C + D$$

would occupy four of the AND gates of the product matrix. However, the same function rewritten as

$$\overline{F} = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D}$$

would occupy only one. Moreover, the second function could be done on the simplest of the Series 20 devices (*and* leave eleven gates over for other functions), whereas the first could not. The fact that all inputs of the Series 20 devices, including the shared ones, incorporate double buffers that make the true and complement forms of all input variables equally accessible, greatly facilitates the use of de Morgan's theorem for logic minimisation.

To convert the minimised logic equations to the pattern of fuses to be blown you can use either a programming sheet (see e.g. Fig.5) or boolean equation program-entry software that lets you enter the equations via the keyboard of a terminal. The direct programmability of logic equations makes system design with IFL simple and sure. Functional changes can be made by replacing one IFL chip by another, differently programmed. In many cases you can even remove the original one, reprogram it on the spot, and re-insert it. Programming machines qualified for the Series 20 are at present available from DATA I/O, KONTRON, and STAG.

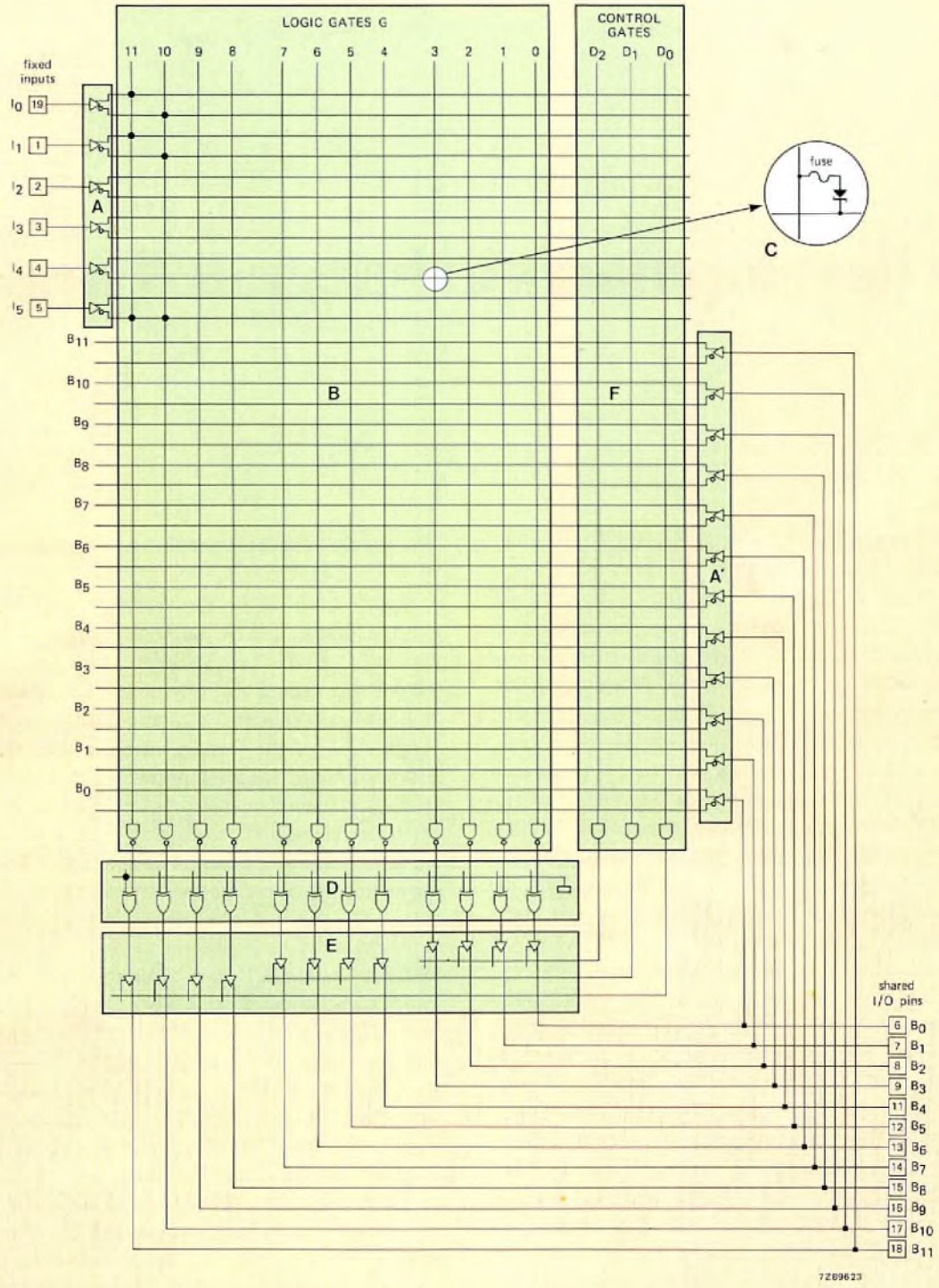


Fig.1 Field-programmable gate array 82S151. A, dedicated inputs; A', programmable I/O. B, product (NAND) matrix with fused connections C; each of the vertical lines in the matrix represents 36 inputs to the terminating NAND gate. D, exclusive-OR array with inputs grounded via fuses for polarity control. E, programmable three-state output buffers. F, fuse-programmable control matrix. Square dots (■) represent permanent connections, round dots (●) intact fuse connections. Connected as shown, the array is programmed for the functions

$$\overline{B}_{11} = I_0\, I_1\, \overline{I_5} \quad \text{and} \quad B_{10} = \overline{I_0}\, \overline{I_1}\, \overline{I_5}$$

FPGA 82S150/82S151

The field-programmable gate array is the simplest of the Series 20 IFL devices; Fig.1 shows the functional diagram. The array can accept up to 18 inputs. There are six dedicated input pins (A) and twelve (A′) that can be programmed as inputs, outputs, or bidirectional I/O. All input variables, whether on dedicated or programmed input pins, are available in both true and complement form in the product matrix (B), and both forms are buffered: either form can drive all twelve product lines if required. In the virgin state, all the input variables and their complements are connected to all the product lines via a diode and a fuse (C), and the product matrix is effectively inoperative. To enable it to generate the required functions, unrequired connections between individual input lines and product lines are severed by blowing the connecting fuses.

At the output of the product matrix are twelve NAND gates, each with 36 inputs to accommodate the 18 possible input variables and their complements. Each of the product terms is normally active-Low, but a unique feature of Signetics IFL is that any or all of them can be independently programmed active-High. This is done by means of an array of exclusive-OR gates (D) at the NAND-gate outputs; when the fuse that grounds the second input of each OR gate is blown, the output of that gate is inverted.

The product matrix and exclusive OR-gate connections shown in Fig.1 illustrate the flexibility conferred by having buffered complements of all input variables internally available, together with independently programmable output polarities. Output B_{11}, shown with its exclusive OR-gate fuse intact, is programmed

$$\overline{B_{11}} = I_0 I_1 \overline{I_5}$$

At the same time, and without using any additional inputs, output B_{10} (fuse blown) is programmed

$$B_{10} = \overline{I_0}\,\overline{I_1}\,\overline{I_5}$$

Each of the exclusive-OR gates drives a three-state output buffer. In the virgin state all the buffers (E) are disabled and therefore in the high-impedance state. The function of the programmable I/O pins (A′) is then determined by the I/O control matrix (F). The three AND gates at the control-matrix output are active-High, and when one of them is in the High state the four output buffers it controls are enabled; the corresponding I/O pins then act as outputs. Conversely, when a control-matrix AND-gate output is Low and the control fuse for the corresponding three-state buffer is intact, the pins controlled by that gate act as inputs. Thus, these pins can be programmed in groups of up to four to act as inputs or outputs according to the state of selected input variables. If required, any of the programmable I/O pins can be made a dedicated output by blowing the control fuse of the output buffer associated with it.

The speed of the FPGA compares favourably with TTL, although its propagation delay (currently specified as 30 ns) is longer than the individual gate delay of TTL. When the number of inputs required is large, however, the FPGA more than makes up for this. When more than eight inputs are required, for example, the FPGA has a distinct advantage. Then, the overall propagation delay of TTL often amounts to two or three gate delays, but that of the FPGA to only one (see Table 1).

TABLE 1
Comparison of propagation delays for FPGA and TTL

number of inputs	TTL gates in series	t_{pd} (ns)			
		FPGA	TTL		
			74	74LS	74S
≤8	1	30	20	17	7
>8	2	30	40	35	16

FPLA 82S152/82S153

Architecture

With two levels of logic, embodied in a product matrix terminating in 32 AND gates coupled to a ten-output OR matrix (Fig.2), the FPLA is a step up in complexity from the FPGA. Again, there is provision for 18 input variables, internally complemented and buffered, but here divided between eight dedicated input pins and ten individually programmable I/O pins. As before, exclusive-OR gates grounded by fuses provide output polarity control, and any of the programmable I/O pins can be made a dedicated output by blowing the control fuse of the output buffer associated with it.

Programming

The first step in programming the FPLA is to define the required functions in boolean equations. These do not necessarily have to be minimised, but a good principle is: the fewer terms you use, the more capacity you will have left for implementing other function on the same FPLA or for altering the program during prototype development. Karnaugh maps will yield sums of products suitable for the FPLA. Logic minimisation methods (Quine-McCluskey, for instance, Ref.1,2) are particularly useful for complicated functions and are often necessary for reducing them to minimum-sums-of-products (MSP). A program called LOGMIN, accessible via data link to Signetics' computer, derives MSPs for an array of up to 16 inputs and 8 outputs.

When the required functions have been defined, corresponding programming instructions are entered in a programming table the layout of which reflects the FPLA

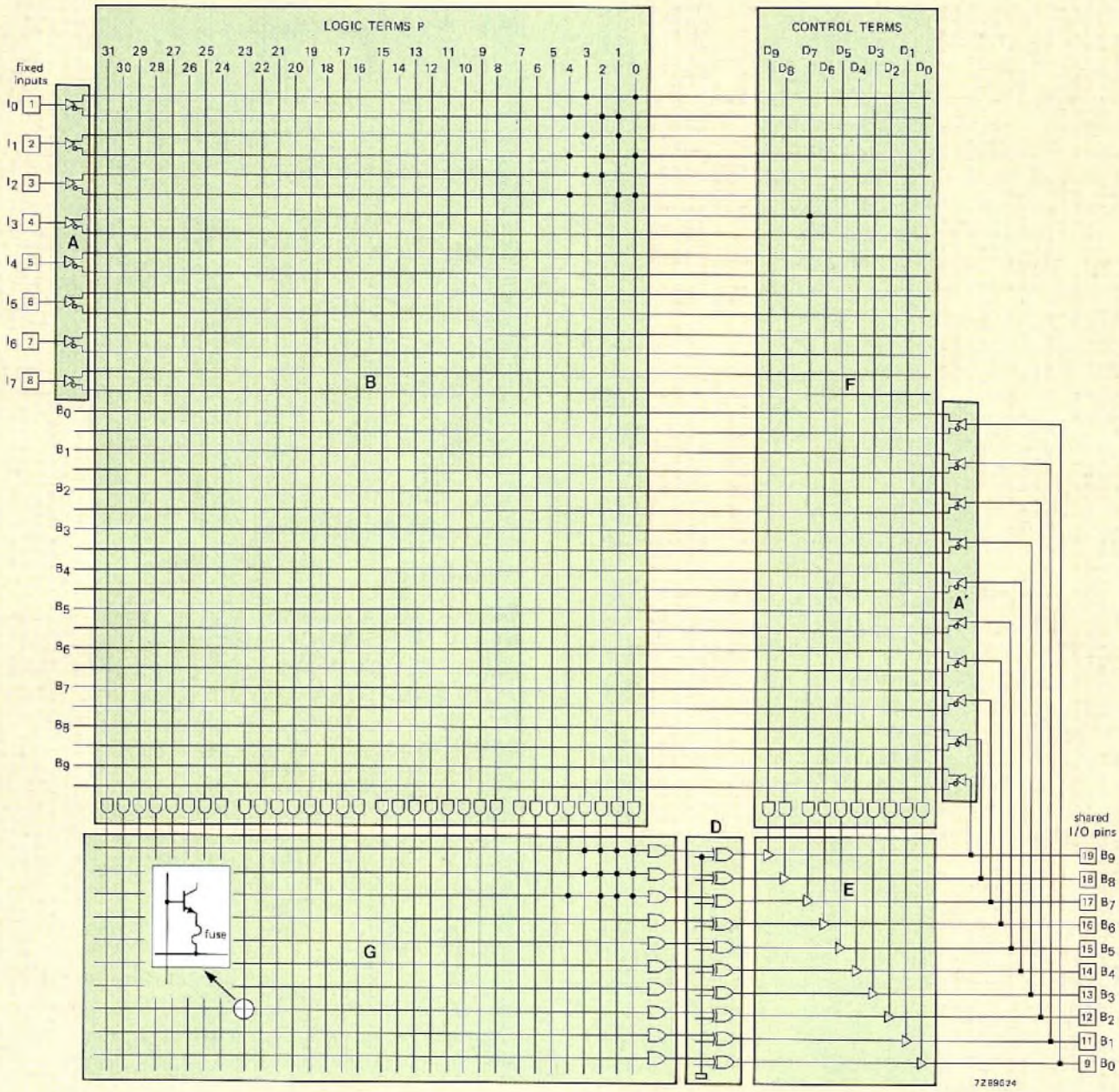


Fig.2 Field-programmable logic array 82S153. A to F, as in Fig.1. G, sum (OR) matrix. Connected as shown, the array is programmed as a single-bit full adder with Carry Enable

architecture. (A computer program that accepts boolean equations as input and generates an FPLA programming table as output is also available.) The programming machine blows the FPLA fuses in the pattern prescribed by the table.

As an illustration of FPLA programming, consider a full adder. Figure 3 shows a TTL version (74LS80) and the corresponding logic equations. Note that the feedback of $\overline{C}_{n+1}$ introduces a second propagation delay. In the FPLA this is eliminated by redefining Σ in terms of A, B and C_n, as shown in Fig.4, and using the right-hand side of the equation for $\overline{C}_{n+1}$ instead of the term itself. At first glance this would appear to require a minimum of three product terms for $\overline{C}_{n+1}$ plus four for Σ, or a total of seven. The Karnaugh maps, however, show considerable overlap between the two functions: the map for $\overline{C}_{n+1}$ differs from that for Σ only by having $A\,B\,C_n$ instead of $\overline{A}\,\overline{B}\,\overline{C}_n$. Rewriting the equation for $\overline{C}_{n+1}$ to introduce $\overline{A}\,\overline{B}\,\overline{C}_n$ and eliminate $A\,B\,C_n$,

$$\overline{C}_{n+1} = A\,\overline{B}\,\overline{C}_n + \overline{A}\,B\,\overline{C}_n + \overline{A}\,\overline{B}\,C_n + \overline{A}\,\overline{B}\,\overline{C}_n$$

increases the numner of product terms by one, but now $\overline{C}_{n+1}$ and Σ have three terms in common. Therefore, since the FPLA allows multiple use of product terms, it is sufficient to program each of the common terms only once; thus, the original seven product terms are effectively reduced to five.

To fill in the programming table (Fig.5), first allocate inputs and outputs.

Inputs		Outputs:	
A	$= I_0$	$\overline{C}_{n+1}$	$= B_7$
B	$= I_1$	$\overline{\Sigma}$	$= B_8$
C_n	$= I_2$	Σ	$= B_9$

Next, enter the product terms of Σ in the product-matrix (AND) part of the table, using H to indicate a true input and L a false one.

- Term 0 is $A\,\overline{B}\,\overline{C}_n$: mark H, L, L in columns I_0, I_1, I_2 of row 0
- Term 1 is $\overline{A}\,B\,\overline{C}_n$: mark L, H, L in columns I_0, I_1, I_2 of row 1
- Term 2 is $\overline{A}\,\overline{B}\,C_n$: mark L, L, H in columns I_0, I_1, I_2 of row 2
- Term 3 is $A\,B\,C_n$: mark H, H, H in columns I_0, I_1, I_2 of row 3.

Fill the rest of rows 0, 1, 2, and 3 with dashes to indicate that all other inputs are to be disconnected from Terms 0, 1, 2, and 3 (fuses blown).

The product terms of Σ must be added to form the sum-of-products required at output B_9. Indicate the required addition by putting an A (for Attached, i.e. fuse unblown) in the Term 0, 1, 2 and 3 spaces of column $B(O)_9$; Term 4 is not required for Σ, so put a dot in the Term 4 space to indicate that it is to be disconnected (fuse blown). To indicate that the output is to be active-High, put an H in the polarity square above the $B(O)_9$ column. Finally, fill row D_9 with

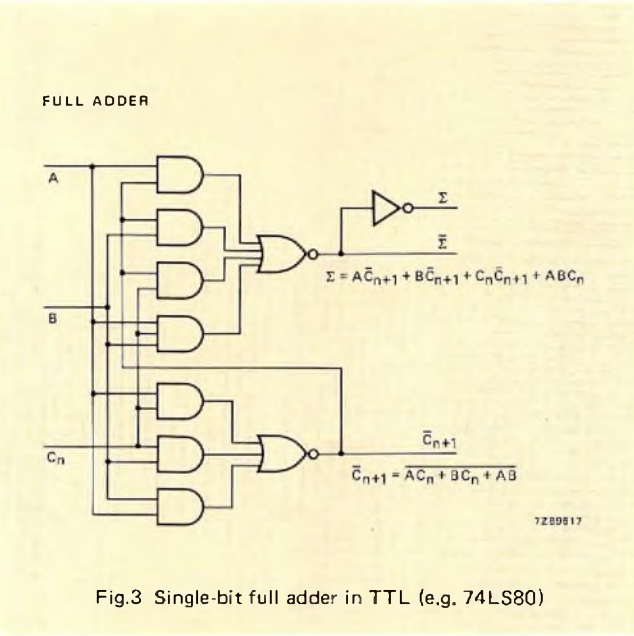


Fig.3 Single-bit full adder in TTL (e.g. 74LS80)

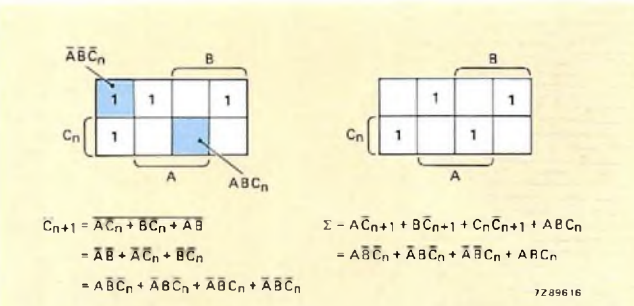


Fig.4 Karnaugh maps and logic equations for the full adder of Fig.3, illustrating how the equations are reduced for the FPLA implementation shown in Fig.2 and 5

dashes to indicate that all fuses on line D_9 of the control matrix are to be blown and B_9 is to be a dedicated output. This completes the programming of Σ.

The $\overline{\Sigma}$ output on B_8 is programmed in just the same way, except that the polarity square above the $B(O)_8$ column is marked L to indicate active-Low. (Note that in the FPLA the Σ and $\overline{\Sigma}$ outputs change simultaneously, because all output signals traverse the exclusive-OR array (D), whether they are active-Hight or active-Low. In the TTL full adder shown in Fig.3 the output inverter delays the change of Σ with respect to $\overline{\Sigma}$.)

The output C_{n+1} on B_7 contains three of the same terms as Σ, plus the term $\overline{A}\,\overline{B}\,\overline{C}_n$. Only this last term needs to be additionally programmed in the product matrix: mark L, L, L in columns I_0, I_1, I_2 of the Term 4 row. Indicate the addition

$$A\,\overline{B}\,\overline{C}_n + \overline{A}\,B\,\overline{C}_n + \overline{A}\,\overline{B}\,C_n + \overline{A}\,B\,\overline{C}_n$$

by putting an A in rows 0, 1, 2 and 4 of column $B(O)_7$, and show that Term 3 ($A\,B\,C_n$) is not required by putting a dot

FPLA PROGRAM TABLE (Logic)

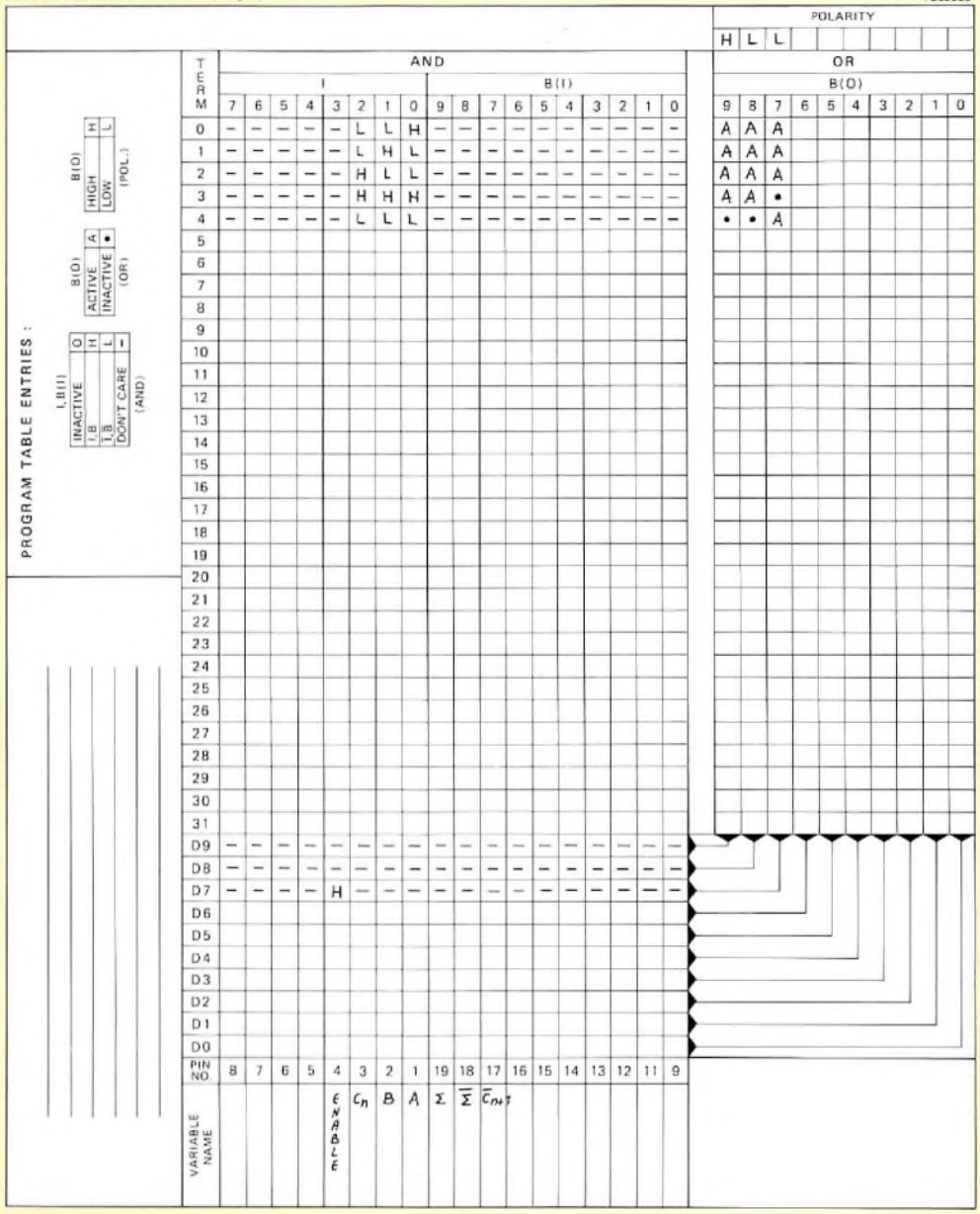


Fig.5 FPLA programming table filled in for the full adder of Fig.2

in the Term 3 row to indicate disconnection (fuse blown). Put an L in the $B(O)_7$ polarity square to indicate active-Low.

Identifying B_7 as a dedicated output by indicating that all the fuses to control term D_7 are to be blown, would now complete the programming of the full adder. However, a useful supplementary feature would be a Carry Enable function to keep the B_7 output buffer in the high-impedance state except when the enable input I_3 is true. The output buffer is enabled when both the fuses of a control term are blown, or when one is blown and the term that controls the

output buffer is true. Thus, a Carry Enable can be provided via the I_3 input by leaving the fuse for active-High operation of the enable signal to control term D_7 intact. To indicate this, put an H in the I_3 column of row D_7 and fill the rest of the row with dashes.

The full adder with output Carry Enable uses only four of the eight dedicated inputs, three of the ten programmable I/O pins, and five of the 32 AND gates. The remaining capacity can be used for programming other functions which may, if required, also make use of AND-gate outputs already programmed for the full adder.

All fuses not indicated as blown in the programming table are normally left intact to preserve capacity for later program revisions or the addition of supplementary functions. If it is essential to minimise propagation delay, however, the finalised program should include instructions for blowing all unused fuses to minimise load capacitance.

Table 2 compares the propagation delay of the FPLA and TTL; the value given for the FPLA is a worst-case value with all fuses intact.

TABLE 2
Comparison of two-level logic propagation delays for FPLA and TTL

number of of inputs	TTL gates in series	t_{pd} (ns)			
		FPLA	TTL		
			74	74LS	74S
≤4	1	40	40	33	14
5–8	2	40	43	35	16
>8	3	40	63	53	25

FPLS 82S154 – 82S159

Architecture

The FPLS (Fig.6, page 118) is the most complex of the Series 20 IFL devices. Like the FPLA, it has a 32-term product matrix followed by an OR matrix. In the FPLS, however, the OR matrix is larger and comprises three distinct parts, with architecture differing in detail from type to type. In the 82S154 and 82S155, for instance, the first part consists of eight 32-input gates coupled, like those of the FPLA, to an output-polarity-controlling exclusive-OR array. The second consists of twelve additional gates which control four flip-flops. These are what give the FPLS its sequential character, enabling it to dictate its next state as a function of its present state. The third part is the deceptively simple complement array (I in Fig.6): a single OR gate with its output inverted and fed back into the product matrix. This enables a chosen sum-of-products to become a common factor of any or all the product terms and makes it possible to work factored sum-of-products equations. It is also useful for handshaking control when interfacing with a processor and for altering the sequence of a state machine without resorting to a large number of product terms.

The 82S154 and 82S155 have four dedicated inputs and eight programmable I/O pins that can be allocated in the same way as in the FPLA. It also has four shared I/O pins (L) whereby the flip-flops can be interfaced with a bi-directional data bus. Two product terms, L_A and L_B in the control matrix F, control the loading of the flip-flops, in pairs, synchronised with the clock.

Figure 7 shows the architecture of the flip-flop circuitry in the 82S154 and 82S155. The flip-flops are positive-edge triggered and can be dynamically changed to J-K, T, or D-types according to the requirements of the function being performed; this considerably lessens the demands on the logic. The three-state inverter between the J and K inputs governs the mode of operation, under the control of the product term F:

- When the inverter is in the high-impedance state the flip-flop is a J-K type, or a T type when J = K.
- When the inverter is active, $K = \overline{J}$ and the flip-flop is a D type; the K input must then be disconnected from the OR matrix.

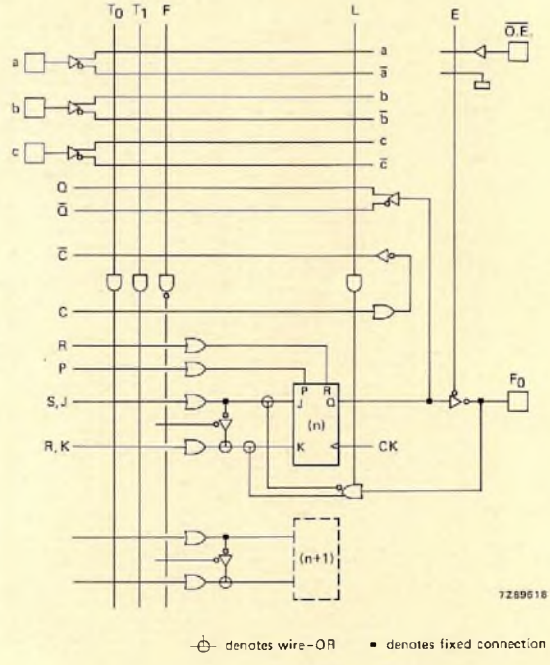


Fig.7 Architecture of the 82S155 flip-flop circuitry

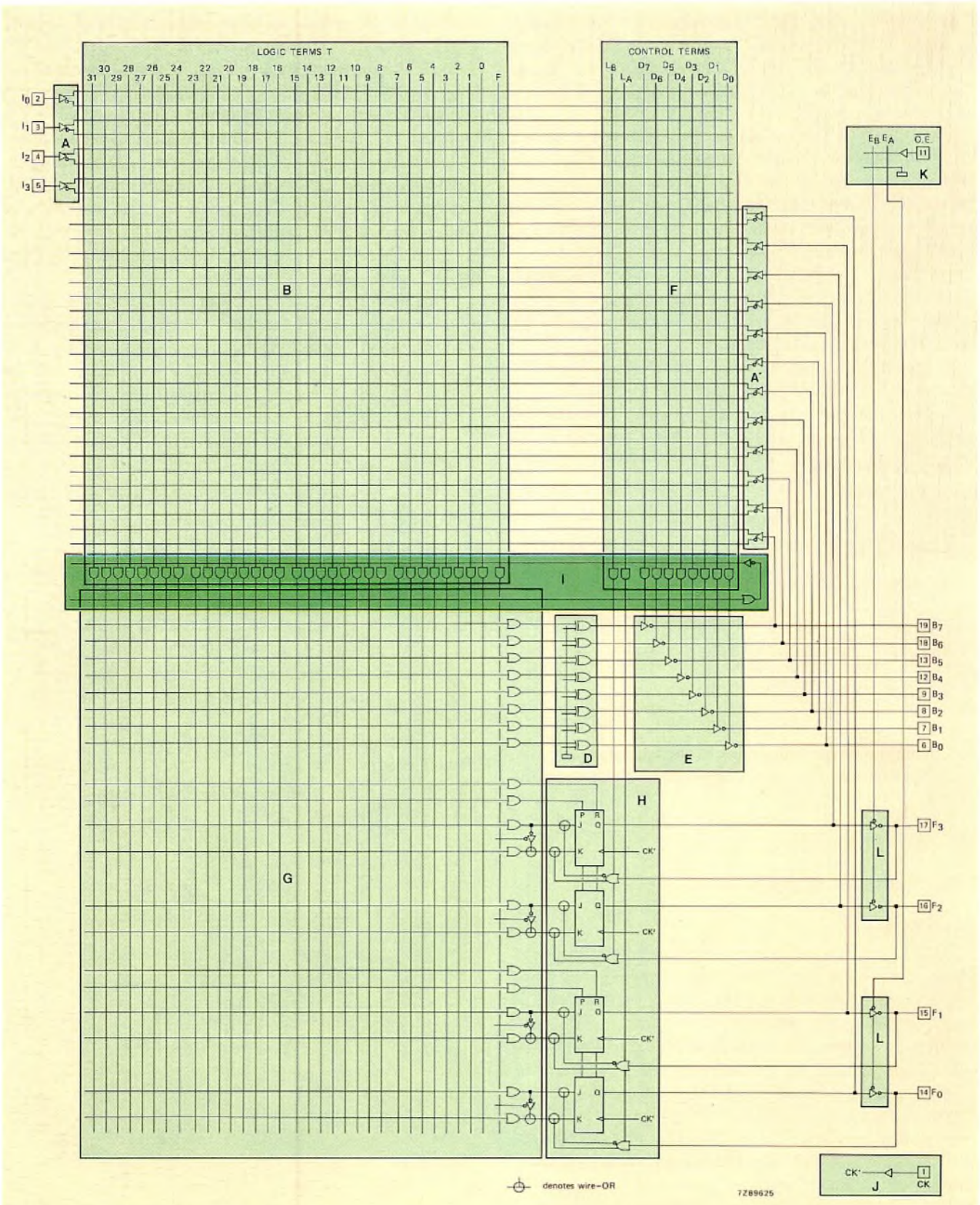


Fig.6 Field-programmable logic sequencer 82S155. A to G, as in Fig.3. H, flip-flops and bus-load buffer. J, clock input. K, output-buffer enable. L, three-state flip-flop output buffers

All the product terms from the product matrix (T_0 to T_{31} in Fig.6) are fuse-connected to the J and K input OR gates. If both fuses of any one product term are left intact, J = K and the flip-flop is a T type.

The flip-flops of the 82S154 and 82S155 have asynchronous Preset and Reset controlled by terms in the OR matrix that take priority over the clock. When power is applied all flip-flops are set to a defined state. Their three-state output buffers can be controlled from the enable pin OE or permanently enabled or disabled by blowing fuses or leaving them intact in the enable array (K in Fig.6).

The 82S156/7 and 82S158/9 sequencers have, respectively, six and eight flip-flops. The architecture differs in detail but is similar in principle to that of 82S154 and 82S155.

Programming

The FPLS is programmed in much the same way as the FPLA, using a table to instruct the machine that blows the undesired fuses. It is not necessary to work with a circuit diagram; in fact, it is even undesirable to do so, since applying the necessary logic reduction techniques would in most cases make the diagram difficult to read and more a hindrance than a help. An example of how to program the FPLS as a universal counter/shift-register is given in the Appendix.

DEVELOPMENT AND PRODUCTION ECONOMY WITH IFL

Underlying the design philosophy of the Signetics Series 20 IFL is the concept of programmable arrays whose architecture emulates logic equation formats rather than mere aggregations of gates. The unique combination of features which support this philosophy includes:

- double-buffered true and complement inputs
- programmable-polarity outputs
- programmable I/O for internal feedback and maximum freedom in allocating inputs and outputs
- truth-table programming format.

These features are common to all the IFL devices. In the field-programmable logic sequencers they are further supported by:

- flip-flops with dynamically alterable operating modes
- a complement array for simplified handshaking control.

From the development engineer's point of view an important advantage of IFL is that it eliminates breadboarding. Once he has worked out the functions required in terms of minimised logic equations, he can program an IFL device accordingly. Once programmed, it will perform those functions.

Loading the instructions into the programming machine usually takes no more than a couple of hours; after that, the machine can program the devices at a rate of 100 an hour. Moreover, since any IFL device can be programmed in many different ways, IFL has considerable potential for simplifying purchasing and stock control. One type of device can be programmed to perform a diversity of tasks for which it would otherwise be necessary to purchase and stock many different devices.

Series 20 IFL is second-sourced by Harris Semiconductor.

APPENDIX

Programming an FPLS as a counter/shift-register

Objective: to program an 82S155 FPLS as a count-up, count-down, shift-right, shift-left machine governed by three control terms – COUNT/$\overline{\text{SHIFT}}$, RIGHT/UP, LEFT/DOWN. Direct implementation would result in a machine with 64 state transitions (see Table A1), which is beyond the scope of the 82S155 or even the 28-pin 82S105. Logic reduction is therefore necessary.

As there are only four feedback variables (D, C, B, A), you can do the reduction by hand, one mode at a time; the control terms need not be included till the summary equations are written. Using the transition mapping method suggested here, you can examine the excitation equations for all types of flip-flops (R-S, J-K, D, T) and choose those types that will perform the required functions using the fewest product terms. Table A2 summarises the rules for flip-flop implementation using transition maps; the transition symbols used in the table mean:

present state	next state	transition symbol
0	0	0
0	1	α
1	0	β
1	1	1

Using these symbols, construct Table A3 from Table A1 to enable you to examine the excitation equations for all types of flip-flops. Proceeding one mode at a time, transfer the state conditions from Table A3 to Karnaugh maps, as in Fig.A1. Following the rules in Table A2, derive the excitation equations for the different types of flip-flops (the examples shown in Fig.A1 omit the T type because it is the same as the J-K type when J = K). In deciding which types of flip-flop to use, remember that logic minimisation with IFL is different from logic minimisation with 'random logic':

TABLE A1
Present-state/next-state table for counter/shift-register

state no.	present state	next state															
		count down				count up				shift left				shift right			
	D C B A	D	C	B	A	D	C	B	A	D	C	B	A	D	C	B	A
0	0 0 0 0	1	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0
1	0 0 0 1	0	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0
2	0 0 1 0	0	0	0	1	0	0	1	1	0	1	0	0	0	0	0	1
3	0 0 1 1	0	0	1	0	0	1	0	0	0	1	1	0	1	0	0	1
4	0 1 0 0	0	0	1	1	0	1	0	1	1	0	0	0	0	0	1	0
5	0 1 0 1	0	1	0	0	0	1	1	0	1	0	1	0	1	0	1	0
6	0 1 1 0	0	1	0	1	0	1	1	1	1	1	0	0	0	0	1	1
7	0 1 1 1	0	1	1	0	1	0	0	0	1	1	1	0	1	0	1	1
8	1 0 0 0	0	1	1	1	1	0	0	1	0	0	0	1	0	1	0	0
9	1 0 0 1	1	0	0	0	1	0	1	0	0	0	1	1	1	1	0	0
10	1 0 1 0	1	0	0	1	1	0	1	1	0	1	0	1	0	1	0	1
11	1 0 1 1	1	0	1	0	1	1	0	0	0	1	1	1	1	1	0	1
12	1 1 0 0	1	0	1	1	1	1	0	1	1	0	0	1	0	1	1	0
13	1 1 0 1	1	1	0	0	1	1	1	0	1	0	1	1	1	1	1	0
14	1 1 1 0	1	1	0	1	1	1	1	1	1	1	0	1	0	1	1	1
15	1 1 1 1	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1	1
control terms																	
COUNT/$\overline{\text{SHIFT}}$		1				1				0				0			
RIGHT/UP		0				1				0				1			
LEFT/DOWN		1				0				1				0			

TABLE A3
Transition table for counter/shift-register

state no.	present state	transition															
		count down				count up				shift left				shift right			
	D C B A	D	C	B	A	D	C	B	A	D	C	B	A	D	C	B	A
0	0 0 0 0	α	α	α	α	0	0	0	α	0	0	0	0	0	0	0	0
1	0 0 0 1	0	0	0	β	0	0	α	β	0	0	α	β	α	0	0	β
2	0 0 1 0	0	0	β	α	0	0	1	α	0	α	β	0	0	0	β	α
3	0 0 1 1	0	0	1	β	0	α	β	β	0	α	1	β	α	0	β	1
4	0 1 0 0	0	β	α	α	0	1	0	α	α	β	0	0	0	β	α	0
5	0 1 0 1	0	1	0	β	0	1	α	β	α	β	α	β	α	β	α	β
6	0 1 1 0	0	1	β	α	0	1	1	α	α	1	β	0	0	β	1	α
7	0 1 1 1	0	1	1	β	α	β	β	β	α	1	1	β	α	β	1	1
8	1 0 0 0	β	α	α	α	1	0	0	α	β	0	0	α	β	α	0	0
9	1 0 0 1	1	0	0	β	1	0	α	β	β	0	α	1	1	α	0	β
10	1 0 1 0	1	0	β	α	1	0	1	α	β	α	β	α	β	α	β	α
11	1 0 1 1	1	0	1	β	1	α	β	β	β	α	1	1	1	α	β	1
12	1 1 0 0	1	β	α	α	1	1	0	α	1	β	0	α	β	1	α	0
13	1 1 0 1	1	1	0	β	1	1	α	β	1	β	α	1	1	1	α	β
14	1 1 1 0	1	1	β	α	1	1	1	α	1	1	β	α	β	1	1	α
15	1 1 1 1	1	1	1	β	β	β	β	β	1	1	1	1	1	1	1	1

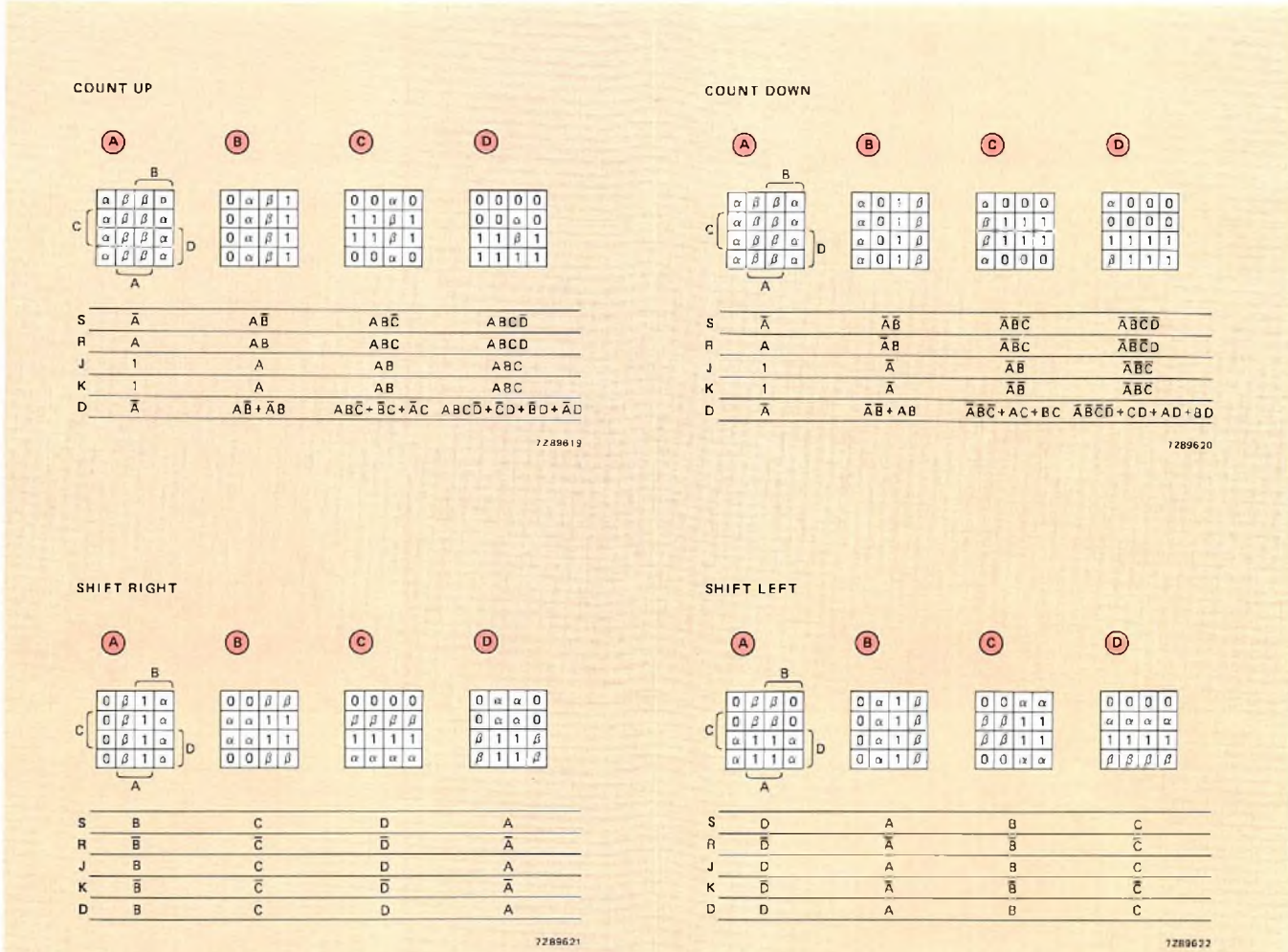


Fig.A1 Karnaugh maps and flip-flop excitation functions for the counter/shift-register

TABLE A2
Rules for flip-flop implementation using transition maps

flip-flop type	input	must include	must exclude	redundant
R-S	S	α	β,0	1,x
	R	β	α,1	0,x
D	D	α,1	β,0	x
T	T	α,β	0,1	x
J-K	J	α	0	1,β,x
	K	β	1	0,α,x

TABLE A4
Number of product terms required for counter/shift-register flip-flop excitation

flip-flop type	count up	count down	shift right	shift left	total
S R only	8	8	8	8	32
J K only	4	4	8	8	24
D only	10	10	4	4	28
FPLS	4(J-K)	4(J-K)	4(D)	4(D)	16

with random logic you seek to reduce the number of standard packages required; with IFL you seek to reduce the number of product terms.

From Fig.A1 it is evident that you should choose J-K or T flip-flops for the counter mode and D flip-flops for the shift mode, for you then require only one product term per flip-flop per mode. Table A4 summarises the number of product terms per mode the various types of flip-flops would require.

Figure A2 shows the completed programming table for

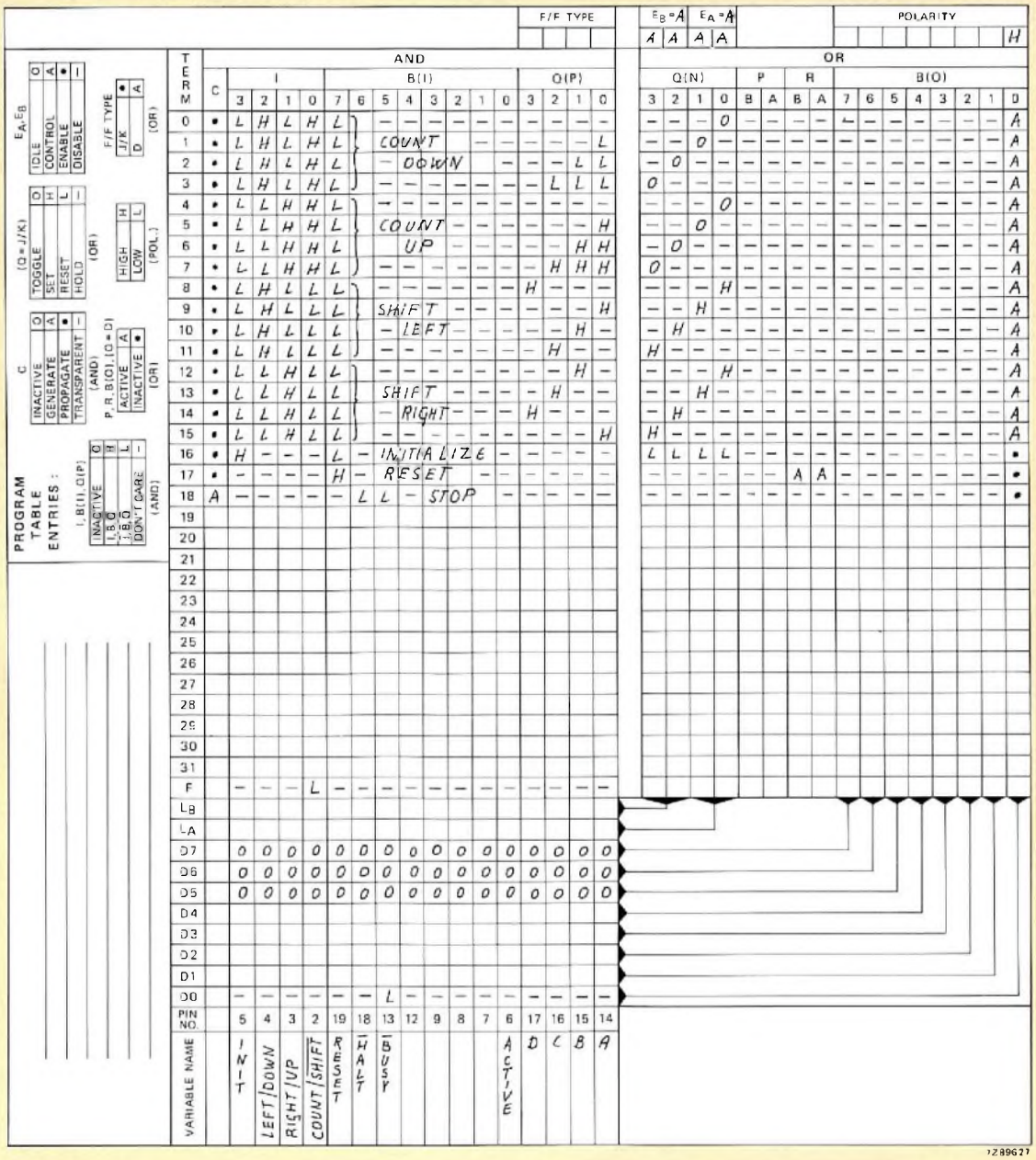


Fig.A2 82 S155 FPLS programming table for the counter/shift register

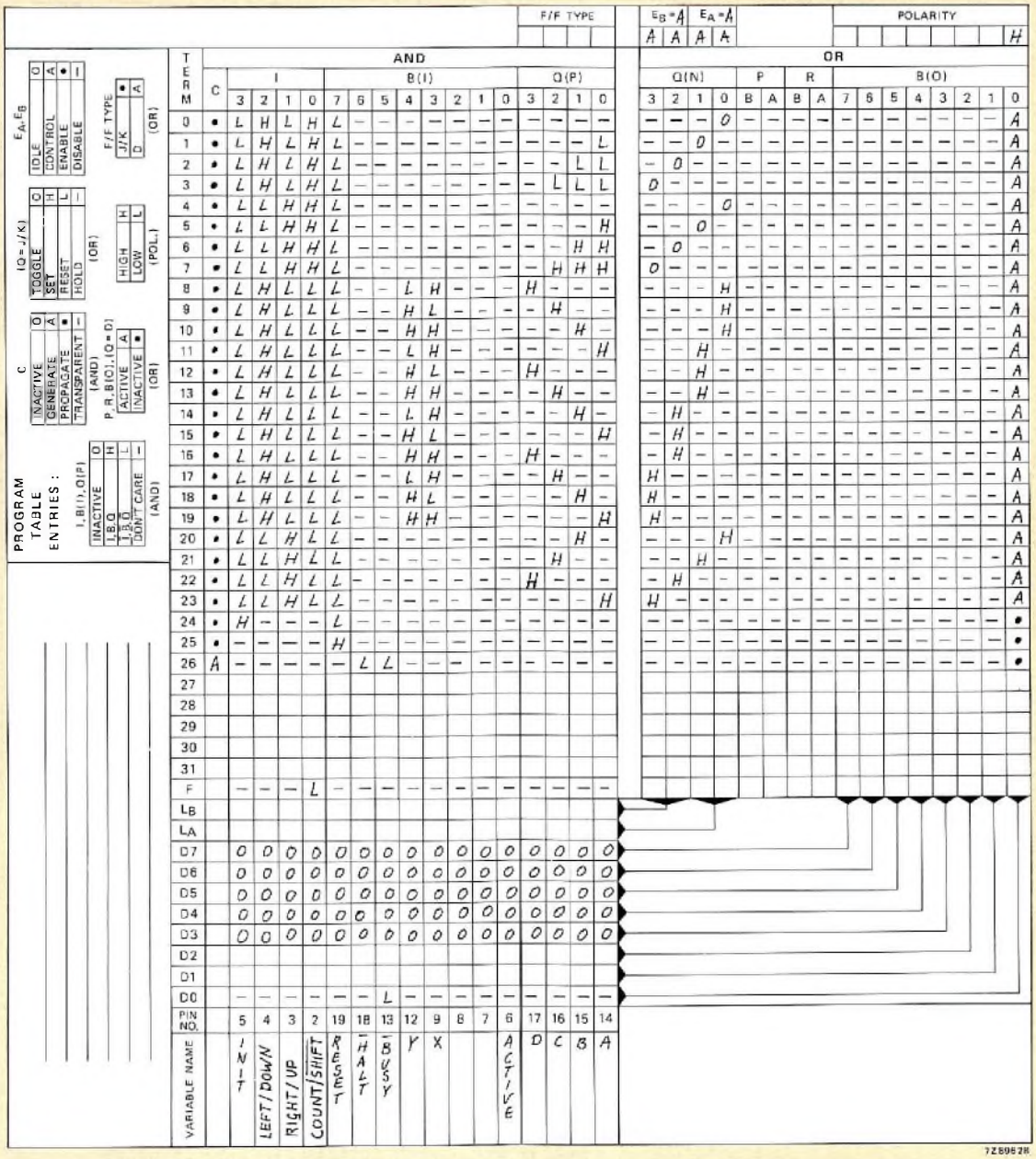


Fig.A3 Modified 82S155 FPLS programming table for the counter/shift-register with the addition of a binary multiplier

the counter/shift-register. The programming of Terms 0 to 15 reflects the flip-flop excitation equations and illustrates the value of being able to switch the flip-flops dynamically from one type of operation to another. Terms 16, 17 and 18, respectively, provide for INITIALIZE, asynchronous RESET, and STOP functions.

The programming of the two additional inputs $\overline{\text{HALT}}$ and $\overline{\text{BUSY}}$ illustrates the value of the complement array, which is made active when $\overline{\text{HALT}}$ and $\overline{\text{BUSY}}$ are Low (A in the Complement square of Term 18) and propagated into all the other terms (dot in the Complement squares of Terms 0 to 17). This means that unless the $\overline{\text{HALT}}$ and $\overline{\text{BUSY}}$ inputs are High none of the product terms will be true and the state of the machine will not change. If the complement array were not used, twice the number of product terms would be required, even if one of the additional inputs were omitted.

As it is, the design uses only 19 of the 32 product terms available, so there is ample capacity for extending its capabilities. For example, the shift-left function can be augmented by a binary multiplication capability, using a D type flip-flop to make it shift one, two, or three places according to the state of two extra inputs, X and Y. Figure A3 shows the revised programming table. The binary multiplication function occupies nine additional product terms and is an example of why initial product-term minimisation is always worthwhile: it affords design flexibility and frees capacity for additional features or refinements that might not otherwise be feasible.

The IFL counter/shift-register has a set-up time of 50 ns – just half what it would be if LS TTL were used.

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Research news

Low-noise multi-purpose AlGaAs laser

Philips Research Laboratories, Eindhoven, and Philips Elcoma Division have cooperated in making a semiconductor laser diode that is both simple to manufacture and capable of stable, low-noise operation up to high powers. The laser combines a number of features that enable it to be used in applications as diverse as optical information recording, video and audio disc read-out, and fibre-optic telecommunication.

For video and audio disc read-out a short wavelength is required, a symmetrical and not too narrow beam, and insensitivity to interference from light reflected back into the laser. For optical recording an additional requirement is that the geometry of the beam should remain stable for nanosecond pulses with a power of 50 mW. For fibre-optic communication the beam should also be easy to modulate; another requirement for this application is a high signal-to-noise ratio.

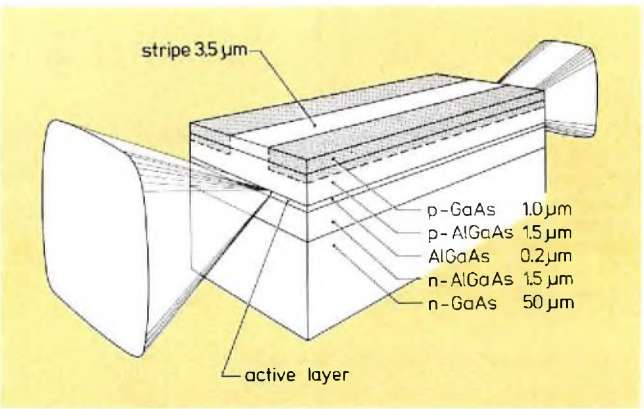
As the diagram shows, the diode laser consists of a single-crystal of gallium-arsenide with a number of layers in which some of the gallium has been replaced by aluminium (AlGaAs). In one of these layers, the active layer, light is generated by the recombination of negative and positive charge carriers (electrons and holes) that are injected into the layer from opposite sides. If some of the light is confined in the structure by mirrors, laser action can occur, giving a very intense and concentrated emission of light.

The light is confined vertically by enclosing the active layer between cladding layers with a lower refractive index. Cleavage planes at the front and back of the crystal provide end-mirrors.

A problem that had to be overcome was that of confining the optical flux laterally in the active layer. One widely used method is to confine the light excitation to a narrow strip-like region (the 'stripe') in the active layer. This can be done by giving the material outside the stripe a higher resistivity by bombarding it with high-energy protons. This method is fairly simple and gives lasers that are not very sensitive to reflected light; however, they have undesirable non-linearities and instabilities. It is possible to eliminate these by introducing a stepped variation in the optical properties in the lateral direction in the active layer. Such 'index-guided' lasers are more difficult to manufacture. They are also sensitive to interference from reflected light, and this makes noise control difficult.

In the new AlGaAs laser these problems have been solved by keeping the proton implantation shallow, leaving the active layer completely unaffected. Lasers with stripe widths of only 3.3 μm can be produced in this way. These lasers, in which the end mirrors are protected by a special coating, provide a stable beam at powers of up to 50-100 mW. The noise characteristics are good, even after prolonged operation at high temperatures. Lasers that combine these features can be successfully used in all the applications mentioned earlier.

A hermetic encapsulation has been developed in which the laser element is mounted on a copper heat sink that has a reference surface for positioning the laser beam without any need for further adjustment. A photodiode mounted beneath the laser can be used for monitoring the radiation from the rear mirror. A special encapsulation for optical-communication applications contains a collimating micro-lens and a glass-fibre connector (a 'pigtail').



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Abstracts

Improved method of power-choke design

A method of designing gapped-core power chokes based on computer-generated charts now published with the data for grade 3C8 Ferroxcube has a number of advantages over traditional methods using Hanna curves. Initial core selection is more positive, the final design takes account of tolerances and temperature effects, and the designer need not concern himself with the magnetic properties of the core.

Integrated voice synthesiser

In our newly-developed totally digital voice-output IC, the MEA8000, the bit-rate requirement has been reduced to a practical level by using the principle of formant synthesis. The article discusses the principles of voice synthesis and explains each part of the new integrated circuit. It also explains how the IC has been designed for simple interfacing with a microcomputer.

Insulation displacement connections

Increases in circuit packing density increase the demands made on interconnection techniques. Soaring labour and machinery costs increase the cost per connection. Insulation displacement (ID) connections, with their potential for making many connections in one operation, are now bringing relief to equipment manufacturers. This article describes the economic and technological foundations of ID connections and their inherent reliability.

Bipolar ICs for DTMF telephone dialling

Use of I^2L technology in the integrated circuits for Dual-Tone Multi-Frequency (DTMF) dialling allows digital and analogue circuits to be combined on one chip. The tones generated are accurate and stable, with low harmonic distortion, and the circuits can be used in conjunction with first or second-order filters and transient voltage suppression to meet the requirements of different telephone authorities.

Uninterruptable power supplies

An uninterruptable power supply uses a battery and an inverter to enable mains-powered equipment to continue operating throughout a mains failure. Switchover from mains to battery power is immediate, and the alternating current supplied is of the same voltage, frequency, and phase as the mains. Efficiency of the supply is 96% at full load and 91% at half load.

New developments in integrated fuse logic

Field programmable logic fills a gap between custom LSI and conventional logic circuits. As a replacement for conventional TTL, the integrated fuse logic described here has an important advantage in that it enables the designer to program the required functions without regard to the details of the circuits in which they are implemented.

Eine verbesserte Methode zum Entwurf von Speicherdrosseln

Eine Methode zum Entwurf von Speicherdrosseln mit Luftspalt beruht auf Computer-Diagrammen, die unter Berücksichtigung der Daten von Ferroxcube 3C8 erstellt wurden und nunmehr veröffentlicht werden. Diese Methode bietet gegenüber den herkömmlichen Methoden, die mit Hanna-Kurven arbeiten, eine Reihe von Vorteilen. Die zu Anfang erfolgende Kernauswahl ist zuverlässiger, der endgültige Entwurf berücksichtigt Toleranzen sowie Temperatureffekte, und der Konstrukteur braucht sich nicht mit den magnetischen Eigenschaften des Kerns zu beschäftigen.

Integrierter Sprachsynthesizer

Bei unserer neuentwickelten, vollständig digital arbeitenden Sprachausgabe-IS (MEA8000) wurden die Bitraten-Anforderungen unter Anwendung des Prinzips der Formantensynthese auf ein praxisgerechtes Niveau reduziert. Der Beitrag erörtert die vorherrschenden Sprachsyntheseverfahren und beschreibt die einzelnen Funtionsblöcke der neuen integrierten Schaltung. Ausserdem macht der Artikel deutlich, dass bei der MEA8000-Entwicklung auf eine einfache Schnittstelle zum steuernden Mikrocomputer besonders Wert gelegt wurde.

Schneidklemmkontakte

Bei zunehmender Packungsdichte der Schaltungen werden auch an die Technik der Anschlüsse höhere Anforderungen gestellt. Infolge des steilen Anstiegs der Lohn- und Maschinenkosten nehmen die Kosten je Anschluss zu. Schneidklemmkontakte (ID - Kontakte) gestatten es, viele Verbindungen in einem Arbeitsgang herzustellen, und führen jetzt zu einer beträchtlichen Arbeitserleichterung für den Gerätehersteller. In diesem Artikel werden die wirtschaftlichen und technologischen Grundlagen von Schneidklemmkontakten sowie ihre konstruktionsbedingte Zuverlässigkeit und zum Schluss verschiedene Ausführungen beschrieben.

Integrierte Schaltungen für DTMF-Nummernwahl in Fernsprechern

Die in den integrierten Schaltungen für Zweiton-Multifrequenz-Nummernwahl (DTMF - Dual-Tone Multi-Frequency) verwendete I^2L-Technik erlaubt es, digitale und analoge Schaltungsabschnitte auf einem Kristall zu kombinieren. Die erzeugten Töne sind frequenzgenau und -stabil mit geringem Oberwellenanteil. Die Schaltungen können in Verbindung mit Filtern 1. oder 2. Ordnung sowie mit Bauelementen zur Störspannungsunterdrückung betrieben werden, um die individuellen Anforderungen der einzelnen Postverwaltungen zu erfüllen.

System zur kontinuierlichen Stromversorgung

Das System arbeitet mit einem batteriebetriebenen Wechselrichter und gewährleistet den kontinuierlichen Betrieb eines netzgespeisten Verbrauchers bei Netzausfall. Die Umschaltung von Netz- auf Batteriebetrieb erfolgt schlagartig, wobei eine dem Versorgungsnetz gleiche Spannung, Frequenz und Phasenlage geliefert wird. Der Wirkungsgrad bei Batteriebetrieb beträgt bei voller Last 96%, bei halber Last 91%.

IFL-Schaltungen

Die IFL-Schaltungen füllen eine Lücke aus zwischen kundenspezifischen LSI- und diskreten Logik-Schaltungen. Als Ersatz für herkömmliche TTL-Schaltungen haben die hier beschriebenen IFL-Schaltungen einen grossen Vorteil. Sie ermöglichen dem Entwickler, die erforderlichen Funktionen zu programmieren, ohne auf detaillierte Anforderungen der Gesamtschaltung Rücksicht nehmen zu müssen.

Une méthode améliorée pour l'étude des bobines d'alimentation

Une méthode d'étude des bobines d'alimentation à noyau ouvert, basée sur des tableaux générés par ordinateur qui viennent d'être publiés avec les données pour le Ferroxcube 3C8, offre plusieurs avantages par rapport aux méthodes classiques utilisant les courbes de Hanna. Le choix initial du noyau est plus sûr, la conception finale tient compte des tolérances et de l'influence de la température, et le projeteur n'a pas besoin de se soucier des caractéristiques magnétiques du noyau.

Circuit intégré à sortie vocale

Dans le circuit intégré à sortie vocale, entièrement numérique, que nous venons de mettre au point, le MEA8000, le débit de bits a été réduit à un niveau raisonnable par l'emploi du principe de la synthèse formante. L'article expose les principes de la synthèse de la voix et explique chaque partie du nouveau circuit intégré. Il explique également comment il a été conçu pour être connecté de manière simple à un micro-ordinateur.

Connexions à déplacement d'isolant

L'accroissement de la densité d'intégration des circuits impose des exigences de plus grandes aux techniques d'interconnexion. La hausse du coût de la main d'oeuvre et des équipements augmente le coût par connexion. Offrant la possibilité de réaliser de nombreuses connexions en une seule opération, les connexions à déplacement d'isolant (ID) portent actuellement secours aux fabricants d'équipements. Cet article décrit les bases économiques et technologies des connexions ID ainsi que leur fiabilité.

Circuits intégrés pour la sélection des numéros de téléphone par le système DTMF

L'emploi de la technologie I^2L dans les circuits intégrés pour la sélection DTMF (Double Tonalité Multi Fréquence) permet de combiner des circuits analogiques et numériques sur une même puce. Les tonalités engendrées sont précises et stables, avec une faible distorsion harmonique et les circuits peuvent être utilisés conjointement avec des filtres du premier ou du second ordre pour la suppression des tensions transitoires afin de satisfaire les exigences des différentes administrations.

Alimentation ininterruptible

Une alimentation ininterruptible, composée d'une batterie et d'un onduleur, permet à des équipements alimentés par le secteur de continuer à fonctionner en cas de panne de ce dernier. Le passage du secteur à la batterie est immédiat et le courant alternatif fourni est de la même tension, fréquence et phase que le secteur. Le rendement de l'alimentation est de 96% en pleine charge et de 91% à demi-charge.

Logique intégrée à fusibles

La logique intégrée à fusibles comble une lacune entre les circuits LSI personnalisés et les circuits logiques conventionnels. En tant que solution de rechange pour la TTL conventionnelle, la logique intégrée à fusibles ici décrite présente un avantage important car elle permet au concepteur de programmer les fonctions requises sans s'occuper du détail des circuits dans lesquels elles sont mises en oeuvre.

Un método mejorado para el diseño de choques de potencia

Los métodos de diseño con choques de potencia con núcleos con entrehierro, basados en los datos para ferroxcube de grado 3C8 ahora publicados mediante cartas generadas por un ordenador, presentan un número de ventajas sobre los métodos tradicionales que usan las curvas de Hanna. La selección inicial es más positiva, el diseño final tiene en cuenta tolerancias y efectos de temperatura y el diseñador no necesita involucrarse con las propiedades magnéticas del núcleo.

Circuito integrado para salida de voz

La barrera de comunicación final entre el hombre y sus máquinas ha sido sobrepasada por la disponibilidad de circuitos integrados que pueden hablar. Con nuestro CI's MEA8000 para salida de voz recientemente desarrollado, totalmente digital, la tasa de bits requerida ha sido reducida a un nivel práctico por el uso del principio de síntesis formante. El artículo discute los principios de síntesis de voz y explica cada una de las partes del nuevo CI. Se explica también como se ha diseñado el circuito para una simple interfaz con un microcomputador.

Conexiones por desplazamiento del aislamiento

El aumento de la concentración de componentes en los circuitos implica un incremento de las exigencias impuestas a las técnicas de interconexión. La elevación de los gastos de mano de obra y maquinaria repercuten también en los gastos por conexión. La posibilidad de hacer muchas conexiones en una sola operación que ofrece la técnica de conexiones por ID (Insulation Displacement) supone ahora un alivio para los fabricantes de equipos electrónicos. Se describen en este artículo los principios económicos y tecnológicos de las conexiones por ID y su inherente seguridad funcional.

Circuitos Integrados para discado telefónico DTMF

El uso de la tecnología I^2L en los Circuitos Integrados para discado telefónico Dual-Tono, Multifrecuencia (DTMF), permite combinar en una sola pastilla circuitos digitales y analógicos. Los tonos generados, son estables y exactos con baja distorión armónica, los circuitos pueden usarse en conjunción con filtros de primero y segundo orden y supresión de voltajes transistorios para satisfacer los requerimientos de las diferentes Compañías telefónicas.

Sistema de suministro de potencia ininterrumpible

Un sistema de suministro de potencia ininterrumpible usa una batería y un inversor para capacitar al equipo alimentado por la red para continuar funcionando durante los fallos de suministro de energía. La conmutación de red a batería es inmediata y la corriente alterna suministrada es del mismo voltaje, frecuencia y fase que la de red. La eficiencia del sistema es del 96% a plena carga y del 91% a media carga.

Lógica integrada fusible

La lógica programable por campo llena un vacío entre el LSI, específico por encargo (custom - LSI) y los circuitos lógicos convencionales, como reemplazamiento del TTL convencional, la lógica integrada posible, descrita aquí tiene una importante ventaja por la cual se capacita al diseñador para programar las funciones requeridas sin tener en cuenta los detalles de los circuitos en los que se insertan.

Authors

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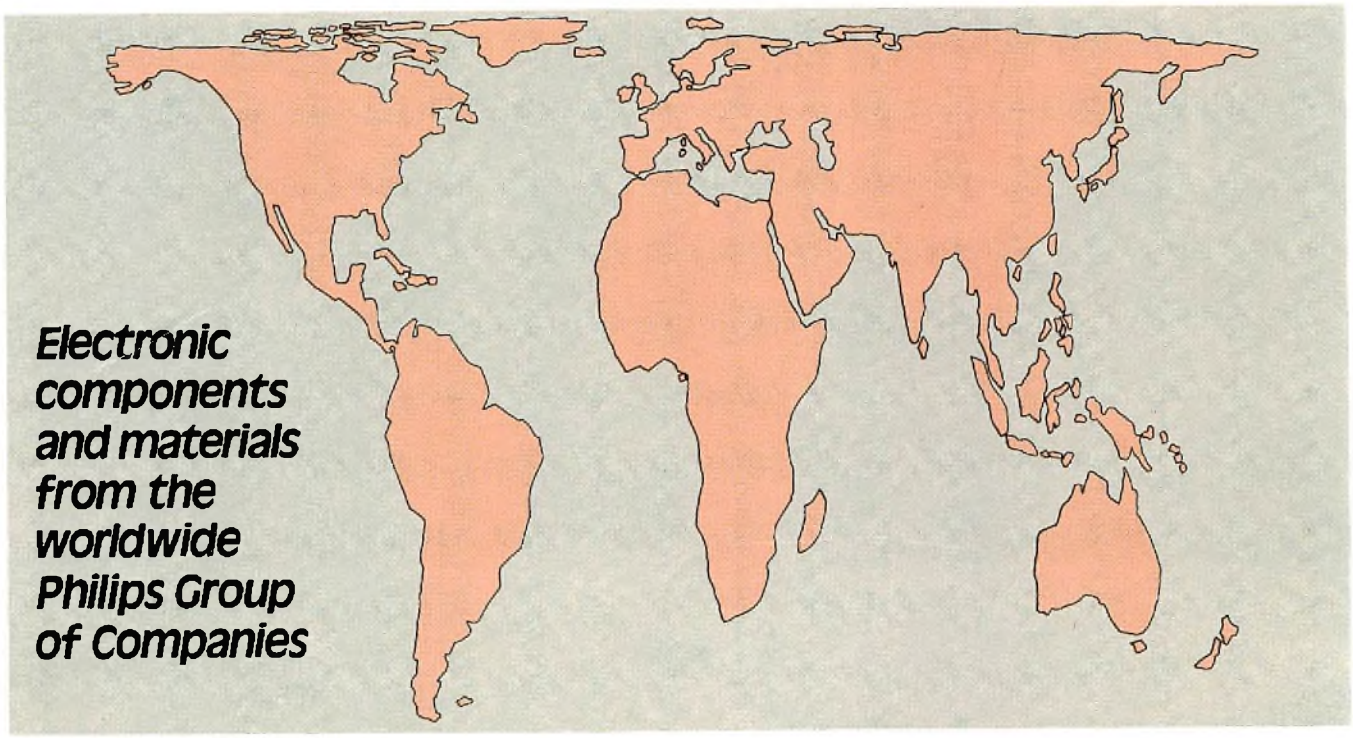

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