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Contents

Synthetic speech is hardly new, as the dolls on the cover can testify – though not in so many words, of course. The extent of their vocabulary was 'Mama!', which just about defined the state of the art till microelectronics got into the act. Now, not only toys and games, but instruments, control panels, and computers are starting to talk back to us, and in most cases what they have to say is well worth listening to. How well they say it is another question, though. But there is progress to report there too. The editing system described on page 241 enables you to improve a speech synthesiser's articulation and intonation in some cases even beyond that of the original on which its vocabulary is based. The next step – eloquence?

A microprocessor bus on Eurocard for systems with distributed intelligence expands easily from 16 to 32 bits.

Expandable microprocessor bus for distributed processing

CECIL KAPLINSKI

Although the cost of processing has declined considerably, so far no microprocessor-bus design has seriously considered distributing intelligence within the system. Now, however, a microprocessor bus has been based on the concept of distributed processing; as a result, it offers a vehicle for expanding systems from 16 to 32 bits without relying heavily on a central CPU. Moreover, the bus simplifies system construction by enabling solution-implementing functions to be placed at the site of an application problem.

The VMEbus is designed around the widely available DIN Eurocard standard, which provides users with all the facilities generally available on buses. These include a 24-bit address width and a 16-bit data bus on a primary 96-pin connector. However, both widths can be extended to 32 bits on an optional, second 96-pin connector. In addition to routing address and data lines, the primary connector accommodates all the signals necessary to operate a complex system, including interrupts, arbitration of bus usage, and provisions for distributing intelligence.

With such functions, system modules can transfer data at 24-Mbyte/s rates, and asynchronous control information can be transferred according to the priority of the information. In addition, several types of bus error can be reported, including those occurring on a single transfer, errors on a module, or even system errors.

Within the VMEbus, a so-called "interintelligence" bus, or I^2B, carries system messages and private messages between modules in serial fashion. Messages consist of either familiar interrupts – "Do something for me" – or system commands such as "Disconnect yourself from the bus". As with any bus the I^2B carries the message recipient's address. But unlike most buses, the I^2B can selectively address a single module (a consumer) or can broadcast a message to all modules belonging to a certain class. The I^2B also differs from conventional buses in that it carries the address of the message producer.

The VMEbus has the backing of three IC manufacturers, Signetics, Motorola, and Mostek, who expect it to have a long life because its initial 16-bit architecture can evolve simply and consistently into 32 bits. Built-in features that allow for this expansion include the definition of extensions for 32-bit data and address, the reservation of modifier codes that allow for functional extension, and extra address space on the serial bus to provide for future demands.

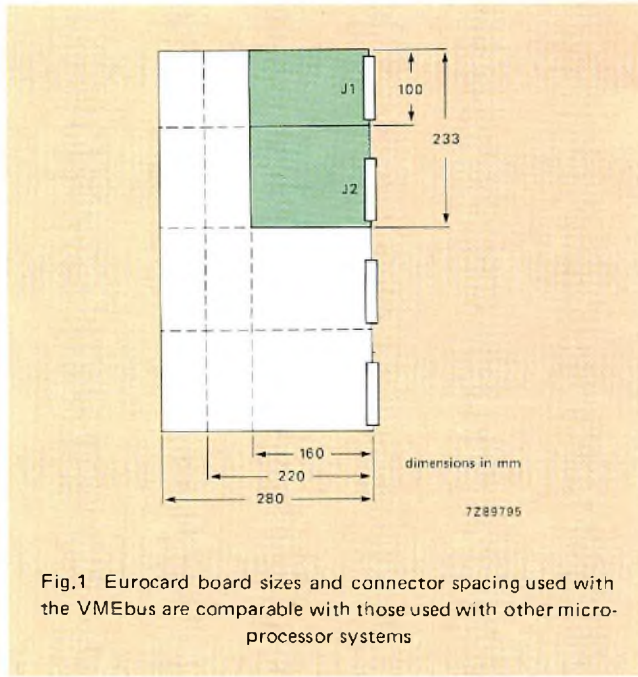

Fig.1 Eurocard board sizes and connector spacing used with the VMEbus are comparable with those used with other microprocessor systems

Card format and connectors

Choice of the Eurocard format for the VMEbus is in line with recent developments in the semiconductor industry. There is a need for internationally acceptable products that support high levels of integration. The Eurocard format, with its high pin-to-area density, accommodates these needs, especially when combined with new semiconductor packaging trends such as small-outline packages and chip carriers.

The board format of the VMEbus will be implemented on printed-circuit boards and backplanes that meet DIN 4162 and 4194 mechanical standards. The standard card sizes are shown in Fig.1. While any of the standard sizes shown will work with the VMEbus, initial units will probably be based on the two most popular sizes. The smaller of these – 160 x 100 mm^2 – is comparable with the popular STD board size. The larger format, 160 x 233.68 mm^2, is comparable with the S-100 and Multibus-style boards.

Only the upper connector, J1 (Fig.2), is necessary and supports high-performance (16-bit data, 24-bit address) microprocessors. Connector J2 is optional in 16-bit systems; it can be used with the larger of the two board formats when an application requires user-defined I/O to enter through the card cage.

The J2 connector is always needed in 32-bit systems. It extends the data and address capacity of the VMEbus to encompass support of microprocessors with up to 32 data lines and 32 address lines (4 Gbytes). Both J1 and J2 provide

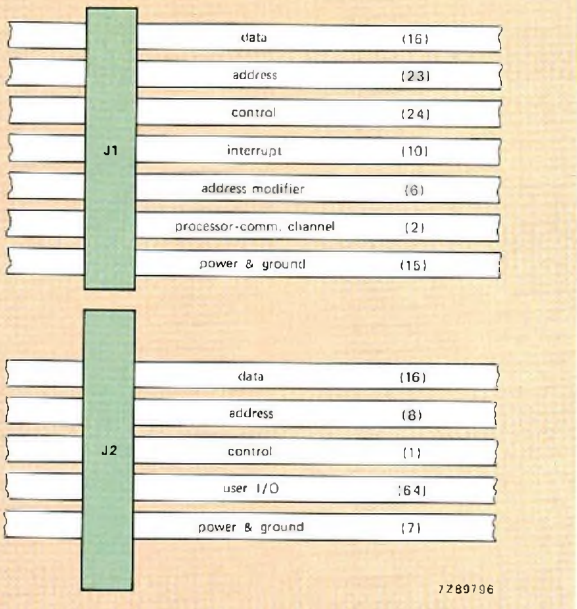

Fig.2 VMEbus connectors J1 and J2. Only J1 is required; J2 allows additional user I/O functions to be brought into the system

5 V power and ground, but only J1 provides ±12 V. Pin assignments on J1 are grouped to allow for ground isolation between critical signal groups. This type of partitioning allows unintelligent slave boards to implement only a proper subset of the pins in the connector.

The J1 pin-assignment chart is given in Table 1. The chart for J2 is not shown since the majority of the pin assignments – 64 of the 96 pins – are devoted to user I/O.

TABLE 1
J1/P1 pin assignments

pin number	signal mnemonics row A	row B	row C
1	D_0	BBSY	D_8
2	D_1	BCLR	D_9
3	D_2	ACFAIL	D_{10}
4	D_3	BG0IN	D_{11}
5	D_4	BG0OUT	D_{12}
6	D_5	BG1IN	D_{13}
7	D_6	BG1OUT	D_{14}
8	D_7	BG2IN	D_{15}
9	GND	BG2OUT	GND
10	SYSCLK	BG3IN	SYSFAIL
11	GND	BG3OUT	BERR
12	DS_1	BR_0	SYSRESET
13	DS_0	BR_1	LWORD
14	WRITE	BR_2	AM_5
15	GND	BR_3	A_{23}
16	DTACK	AM_0	A_{22}
17	GND	AM_1	A_{21}
18	AS	AM_2	A_{20}
19	GND	AM_3	A_{19}
20	IACK	GND	A_{18}
21	IACKIN	SERCLK	A_{17}
22	IACKOUT	SERDAT	A_{16}
23	AM_4	GND	A_{15}
24	A_7	IRQ_7	A_{14}
25	A_6	IRQ_6	A_{13}
26	A_5	IRQ_5	A_{12}
27	A_4	IRQ_4	A_{11}
28	A_3	IRQ_3	A_{10}
29	A_2	IRQ_2	A_9
30	A_1	IRQ_1	A_8
31	–12 V	+5 V STDBY	+12 V
32	+5 V	+5 V	+5 V

Bus protocols

As an asynchronous bus, the VMEbus allows multiple master and slave operations. To minimise bus-transmission time, the bus must be terminated as illustrated in Fig.3. The control of the exchange protocol depends on five signals: AS, DS_0, DS_1, DTACK, and BERR (see "VMEbus signals").

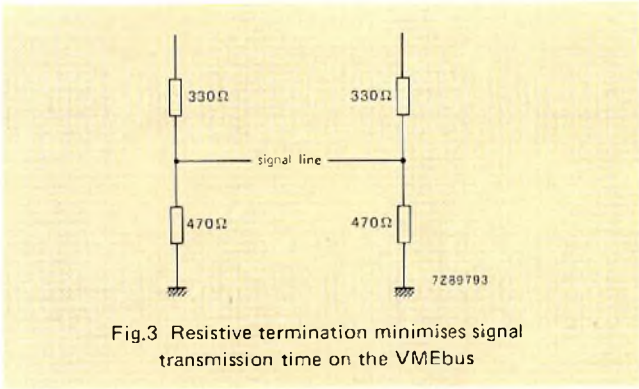

Fig.3 Resistive termination minimises signal transmission time on the VMEbus

Figure 4 shows a typical read bus cycle. Signal AS establishes that a valid address is on the bus, and DS_0 and DS_1 indicate that data transmission will occur on selected data lines. Signals DS_0 and DS_1 distinguish not only between byte data-transfers on the top or bottom eight data lines, but between byte and word transfers. Either DTACK or BERR can terminate a bus cycle. Normal termination occurs through DTACK. But should an error occur – for example, incorrect parity on a memory card – BERR will signal termination instead of DTACK. The master can then repeat or abort the operation, depending on conditions in the slave.

This protocol differs from that of other systems in that it has two strobes, AS and DS. This allows for a non-interruptible read-modify-write operation, which is necessary to ensure a safe semaphore. Semaphores are needed in virtually all modern multiprocessing systems to guarantee that system resources, including processor scheduling, are allocated safely and consistently.

Priority levels

To allow fast peripherals and additional processors to use the bus, the VME system provides for various masters to gain control. The bus recognises four priority levels. For a system having dynamic re-allocation of priorities, three dynamic levels – normal, urgent and relaxed – can be used for standard operations; the fourth level is used in emergencies. Each level has its own request line and a daisy-chain grant line. No fixed preallocation to priority levels is needed since any master can change its priority depending on the urgency of its request.

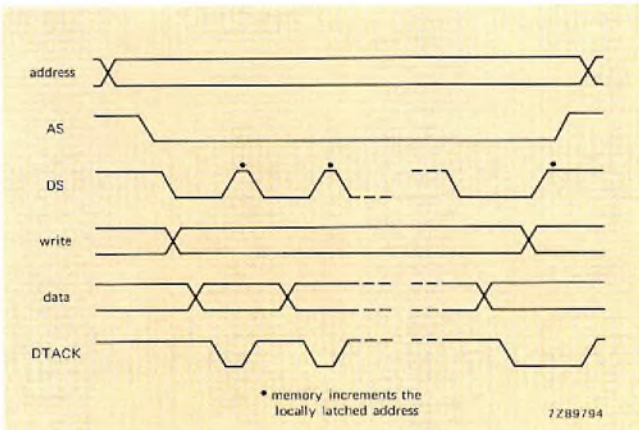

Fig.4 Signals DTACK and AS are important to read-cycle operation; AS establishes that a valid address is on the bus and DTACK ends the read-cycle

Interrupt levels

Interrupts (IACK, IRQ_1 to IRQ_7) work the same as priority levels. There are seven levels of interrupt-level requests. When the processor responds with an interrupt acknowledge, it is daisy-chained down the bus for the intended module to seize and use. This simple interrupt system is supplemented by a more sophisticated system for use in distributed-intelligence systems. (At this time, however, the advanced system is still in the development stage.)

Most conventional buses use an *ad hoc* series of lines to identify I/O, interrupt acknowledge, etc. By contrast, the VMEbus has a consistent and flexible way to describe such transfers. An address modifier is provided in addition to the address. The modifier consists of six lines that follow the timing protocols of the address lines, providing additional functional information (Table 2). These lines distinguish between normal memory transfers, extended address-memory transfers, and interrupt-acknowledge and short-address (only 16 lines) transfers. Moreover, the lines provide a distinction between 16, 24, and 32-bit address transfers, and also between user and system transfers. Some unused codes are reserved, while others are left to the requirements of the application system.

Extensive error-reporting mechanisms are also built-in. Two failure lines exist, in addition to BERR. One is ACFAIL, which warns all attached modules of power failure. The other is SYSFAIL, whereby any module can alert the system, or alert a special monitor attached to the system, of a failure.

Communication between processors

Most modern microprocessor systems contain more than one processor, with the additional processors tightly bound to an I/O controller. Such processors should be able to receive interrupts because they may be operating in time-critical modes whenever the CPU is sending commands. Unfortunately, though, most microprocessor systems have no means of passing messages from the CPU to peripheral processors. The situation becomes more complicated when the system contains many equivalent processors.

The problem is not only to provide communications between a processor and I/O, but also to provide communication between processors. In addition to semaphores, an operating system should be able to send and wait for messages between processors. The kernel of a multiproces-

TABLE 2
Address-modifier codes

hexadecimal code	address modifier 5	4	3	2	1	0	function	defined by
38-3F	H	H	H	X	X	X	undefined	reserved
37	H	H	L	H	H	H	extended supervisory ascending access	VMEbus spec
36	H	H	L	H	H	L	extended supervisory program access	VMEbus spec
35	H	H	L	H	L	H	extended supervisory data access	VMEbus spec
34	H	H	L	H	L	L	undefined	reserved
33	H	H	L	L	H	H	extended nonprivileged ascending access	VMEbus spec
32	H	H	L	L	H	L	extended nonprivileged program access	VMEbus spec
31	H	H	L	L	L	H	extended nonprivileged data access	VMEbus spec
30	H	H	L	L	L	L	undefined	reserved
20-2F	H	L	X	X	X	X	undefined	user
18-1F	L	H	H	X	X	X	undefined	reserved
17	L	H	L	H	H	H	undefined	reserved
16	L	H	L	H	H	L	undefined	reserved
15	L	H	L	H	L	H	short supervisory I/O access	VMEbus spec
14	L	H	L	H	L	L	undefined	reserved
13	L	H	L	L	H	H	undefined	reserved
12	L	H	L	L	H	L	undefined	reserved
11	L	H	L	L	L	H	short nonprivileged I/O access	VMEbus spec
10	L	H	L	L	L	L	undefined	reserved
08-0F	L	L	H	X	X	X	undefined	reserved
07	L	L	L	H	H	H	standard supervisory ascending access	VMEbus spec
06	L	L	L	H	H	L	standard supervisory program access	VMEbus spec
05	L	L	L	H	L	H	standard supervisory data access	VMEbus spec
04	L	L	L	H	L	L	undefined	reserved
03	L	L	L	L	H	H	standard nonprivileged ascending access	VMEbus spec
02	L	L	L	L	H	L	standard nonprivileged program access	VMEbus spec
01	L	L	L	L	L	H	standard nonprivileged data access	VMEbus spec
00	L	L	L	L	L	L	undefined	reserved

sor operating system must issue commands and receive acknowledgement that they have been obeyed. A communications channel must be available to a diagnostic system to control the access of possibly faulty modules onto the parallel bus.

To satisfy the need for communications between processors, the VMEbus uses the I^2B. In addition to providing the necessary communications functions, it has a large enough address and function space to allow a specific application to use portions for its own purposes. And some address and function codes have been reserved for future expansion.

Even with its apparent power, the I^2B is not meant to be totally self-sufficient. Its main function is to carry packets of information indicating which modules wish to communicate with each other. In general, the I^2B does not carry the message itself. Since messages tend to contain large amounts of data, they must reside in a memory that is accessible to

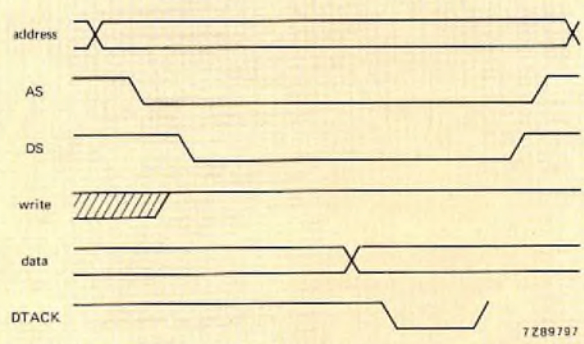

Fig.5 Signals AS, DS, and DTACK control the timing of block moves in which long messages are transferred from one module's memory to another's

VMEbus signals

Signal nomenclature on the VMEbus is similar to that of other microprocessor buses. But the functions associated with each signal are unique to the VMEbus. The following glossary defines each signal and its function:

ACFAIL (Ac Failure): An open-collector-driven signal that indicates that the input to the power supply is no longer being provided, or that the required input voltage levels are not being met.

AM_0-AM_5 (Address Modifier, bits 0-5): Three-state-driven lines that provide additional information about the address bus, such as size, cycle type, and/or DTB master identification.

AS (Address Strobe): A three-state-driven signal that indicates a valid address is on the address bus.

A_1-A_{23} (Address Bus, bits 1-23): Three-state-driven address lines that specify a memory address.

A_{24}-A_{31} (Address Bus, bits 24-31): Three-state-driven bus-expansion address lines.

BBSY (Bus Busy): An open-collector-driven signal generated by the current DTB master to indicate that it is using the bus.

BCLR (Bus Clear): A totem-pole-driven signal generated by the bus arbitrator to request release by the current DTB master in the event that a higher level is requesting the bus.

BER (Bus Error): An open-collector-driven signal generated by a slave. This signal indicates that an unrecoverable error has occurred and the bus cycle must be aborted.

BG0IN/BG3IN (Bus Grant 0-3 In): Totem-pole-driven signals, generated by the arbiter or requesters, that form a daisy-chained bus grant with Bus Grant Out signals. The Bus Grant In signal indicates to this board that it may become the next bus master.

BG0OUT/BG3OUT (Bus Grant 0-3 Out): Totem-pole-driven signals, generated by requesters, that form a daisy-chained bus grant with Bus Grant In signals. The Bus Grant Out signal indicates to the next board that it may become the next bus master.

BR_0-BR_3 (Bus Request, 0-3): Open-collector-driven signals, generated by requesters, that indicate that DTB master in the daisy chain requires access to the bus.

DS_0 (Data Strobe 0): A three-state-driven signal that indicates during byte and word transfers that a data transfer will occur on data-bus lines D_0 through D_1.

DS_1 (Data Strobe 1): A three-state-driven signal that indicates during byte and word transfers that a data transfer will occur on data-bus lines D_8 through D_{15}.

DTACK (Data Transfer Acknowledge): An open-collector-driven signal generated by a DTB slave. The falling edge of this signal indicates that valid data are available on the data bus during a read cycle, or that data have been accepted from the data bus during a write cycle.

D_0-D_{15} (Data Bus, bits 0-15): Three-state-driven bidirectional data lines that provide a data path between the DTB master and slave.

D_{18}-D_{31} (Data Bus, bits 16-31): Three state-driven bidirectional lines for data-bus expansion.

GND: Ground.

IACK (Interrupt Acknowledge): A signal from any master processing an interrupt request. Routed via the backplane to slot 1, it is looped back to become slot 1 IACKIN to start the interrupt-acknowledge daisy chain.

IACKIN (Acknowledge In): A totem-pole-driven signal that forms a daisy-chained acknowledge with IACKOUT, and indicates to the Eurocard that an acknowledge cycle is in progress.

IACKOUT (Acknowledge Out): A totem pole-driven signal that forms a daisy-chained acknowledge with IACKIN and indicates to the next board that an acknowledge cycle is in progress.

IRQ_1-IRQ_7 (Interrupt Request, 1-7): Open-collector-driven signals, generated by an interrupter, that carry prioritised interrupt requests. Level 7 is the highest priority.

LWORD (Long word): A three-state-driven signal indicating that the current transfer is a 32-bit transfer.

RESERVED (Reserved): Signal lines reserved for future VMEbus enhancements. These lines must not be used.

SYSCLK (System Clock): A constant 16 MHz clock signal that is independent of processor speed or timing and is used for general system timing.

SYSFAIL (System Fail): An open-collector-driven signal that indicates a failure in the system, and can be generated by any module on the VMEbus.

SYSRESET (System Reset): An open-collector-driven signal that, when low, causes the system to be reset.

WRITE (Write): A three-state-driven signal that specifies the data-transfer cycle in progress (either read or write). A high level indicates a read operation, a low level indicates a write operation.

both the producer and consumer of the message. In some cases, the message may have to be transferred from the memory of the producer module to that of the consumer module; this is called a block move. The VMEbus provides a facility for rapid block moves by overlapping memory accesses with the bus-transfer period.

A block move is signalled by a unique code on the address-modifier lines. The code indicates that the current address is being accessed, and that the next address will also be accessed.

After the first transfer, the address is not asserted, but is assumed to have been latched in memory. As Fig.5 shows, AS is asserted at the beginning of the block transfer, along with a valid starting address. The first transfer proceeds normally, with DS strobing the data and DTACK providing the slave handshake. When DS goes high, the memory

module must increment the address it previously latched internally. For the next transfer, and all subsequent transfers until the end of the block move, AS remains asserted, and DS and DTACK provide the handshake.

This system allows memory to pipeline its operation; that is, to read the next word during the bus propagation and handshake time. Pipelining is particularly suitable for x 1 RAMs – 16K or 64K – since they can be accessed faster when operated in a paging mode.

Message system

The I^2B operates synchronously on a serial bus line, and has a built-in arbitration protocol. Each I^2B message consists of a packet of information that carries the following data:

Priority. This is the priority of the message within the system. It also serves as the priority for using the I^2B when two producer modules attempt to use the bus simultaneously.

Producer of the information. Unlike most buses, the I^2B carries, with each packet of information, the identity of the transmitter (producer). Several address ranges are predefined (Table 3), indicating system modules or functions. Others are free for use as the application dictates.

Address of the consumer(s). This identifies the receiver. Some addresses are reserved for the system, and normally designate more than one consumer module. The other addresses are free to be allocated to the application, individually or in groups.

Message type. Two bits define the message type. Three types of messages can be sent – interrupts, system commands, and user information. Table 4 shows the bit coding.

Function code. This field allows a message to carry functional information, called parameters. Such information is 2 bytes long, and can be used as an index in a predefined table of addresses, much the same as an interrupt vector (Table 5).

Acknowledgements. Each transmitted information packet is acknowledged separately. Two acknowledge bits allow a consuming module to indicate whether it is on or off line, and whether it can accept the message (Table 6).

The I^2B requires two communication lines: One is SERCLK, a clock provided once per system bus for the

TABLE 3
Consumer-address assignments

address range	use
63	primary system monitor
56 – 62	reserved (for additional system monitor)
48 – 55	user monitors
16 – 47	available to users
8 – 15	reserved
0 – 7	available to users

TABLE 4
Message-type assignments

value of type field	message type
11	system commands
10	interrupts
01	available for user definition
00	reserved

TABLE 5
Function codes

message type	1st byte	2nd byte	use
11	255	255	power fail
		254	disconnect
		253	connect
		252	reset
		251-0	reserved
	254	255	perform diagnostics
		254-0	reserved
	253	ff	set function-table base address to data given in ff field. 253 is the most significant byte
	252		
	251		
	250		
	249	vector	flush cache of segment whose descriptor is in the function-table address with 4 x vector as offset
	248-196		reserved
	128-195	sn	set semaphore number sn
	64-127	sn	reset semaphore number sn
	63-0		reserved
10	255-1		reserved
	0	vector	interrupt vector
01	255-0	255-0	available for application use

TABLE 6
Interpretation of acknowledge bits

ACK	NACK	interpretation
True	True	This can only occur in broadcast messages. It implies that some but not all the consumers can accept the message.
True	False	Normal acknowledge. The consumer(s) has accepted the message.
False	False	The consumer is disconnected from the I^2B, i.e., it is not present, lacks power, or has been disconnected.
False	True	The consumer is present but cannot accept the message now.

timing information used by all bus units; this line operates at 4 MHz. The other communications line, SERDAT, is an open-collector line used to transmit information. Its wired-AND property is used during arbitration.

A packet of information is transmitted in the order shown below – MSB first, LSB last. Bits on SERDAT are synchronised with the positive-going edge of SERCLK, and are maintained until the next positive-going edge.

start bit	priority bits	producer address	consumer address	message type	function bits	ACK bits
1 bit	5 bits	6 bits	6 bits	2 bits	16 bits	2 bits

The start bit is a signal generated by all producers who have messages ready for transmission. This signals all potential producers that they should either take part in the pending arbitration cycle or remain inactive until the end of the transmission. After the start bit, users having messages place their priorities serially on the SERDAT line, MSB first. On the negative-going edge of SERCLK, active producers sample SERDAT. Since SERDAT is an open-collector line, any message at a ONE (ground) appears on the bus even if another message is transmitting a ZERO (high). A module that puts a ONE on the bus at the positive-going edge of SERCLK and samples a ZERO on the negative edge loses arbitration and must retire until the end of the packet. At the end of bit 6, the priority level demanded will have appeared, serially, on SERDAT.

The remaining message sender(s) must place a producer address on SERDAT in a similar manner. At the end of this phase, only one module should remain. Thus if two or more modules attempt to use the I^2B simultaneously, arbitration is performed automatically on the basis of the priority of their messages. If two or more message producers have the same priority, and both win the priority arbitration, then the producer address, which cannot be duplicated in the system, must resolve the confict. All potential consumers must sample the data on the negative-going edge of SERCLK. This way, if a message is destined for one of the consumers, they can respond appropriately.

The producer address can be used in the arbitration process, but more typically it provides the message consumer with the producer address. Consumer addresses can be duplicated if they are used in the broadcast message. More often, there will be only one module per address, and a single module might have more than one address if it embodies more than one logical module.

Message bits describe the type of message to appear on the bus: system command, interrupts, or user messages. System commands help control and synchronise the system. Interrupts include the priority (interrupt level) and an interrupt vector. User messages contain information that is transparent to the system, and thus can serve any purpose required.

Function bits contain the information passed in a message. In general, this information is the address of a function to be performed, equivalent to the interrupt vector in an interrupt type of message.

The two acknowledge bits are inverses of one another – Acknowledge (ACK) and Not Acknowledge (NACK). They can determine whether a module was on-line and whether it could accept a message. In addition, acknowledge bits allow any bus user to monitor the bus and generate a transmission error. They also allow a producer to ensure that its message has appeared on the I^2B in un-interrupted form. If it has not, acknowledge bits tell the consumer to ignore the message.

ACKNOWLEDGEMENT

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Schottky barrier diodes combine the short reverse recovery time of silicon with the low forward-biased knee voltage more commonly associated with germanium diodes.

Schottky-barrier diodes combine the best of germanium and silicon

Th. HAFEMEISTER

Two basic types of small-signal p-n junction diodes are available:

- silicon diodes with a wide range of reverse characteristics, a forward-biased knee voltage of about 700 mV and a moderate reverse recovery time
- germanium diodes which are more expensive than silicon types and have a much more limited range of reverse characteristics, a forward-biased knee voltage of about 200 mV and, in most cases, a very long reverse recovery time.

It is thus evident that there is a need for a range of small-signal diodes which combine the desirable features of both types namely, simple inexpensive construction, low forward voltage, short reverse recovery time (fast switching) and a reasonable range of reverse breakdown voltages. Schottky-barrier diodes provide a partial answer because they have a low forward voltage at low current density as shown in Fig.1 and, since they are metal-semiconductor junctions, they are easily fabricated majority carrier devices which are free from the storage delay time exhibited by p-n junction diodes which depend upon minority carrier injection. Their switching speed is therefore only limited by their reverse capacitance. Since the Schottky barrier cannot absorb reverse energy, some form of protection must be provided. In a Schottky-barrier diode with an n-type semiconductor, this can be achieved by constructing the diode so that the barrier ends upon a diffused p-type guard ring which, together with the n-type semiconductor, forms a 'protection' p-n junction diode in parallel with the Schottky-barrier diode. A diode with such a construction has a sharply defined reverse breakdown voltage similar to that of a zener diode and can be made to withstand reverse voltages up to 100 V. This type of construction is used in our range of Schottky-barrier diodes with the prefix BAT. Our present range of Schottky-barrier diodes is:

BA481. Low reverse capacitance, steep forward characteristic and low noise. Mainly for use in u.h.f. mixers. It can be used to replace germanium point-contact diodes.

BAT81/82/83. Very short reverse recovery time for fast switching in logic, clipping, clamping and transistor speed-up circuits.

BAT85. Similar electrical performance to germanium gold-bonded diodes like the AAZ18. Similar low forward voltage but better thermal characteristics.

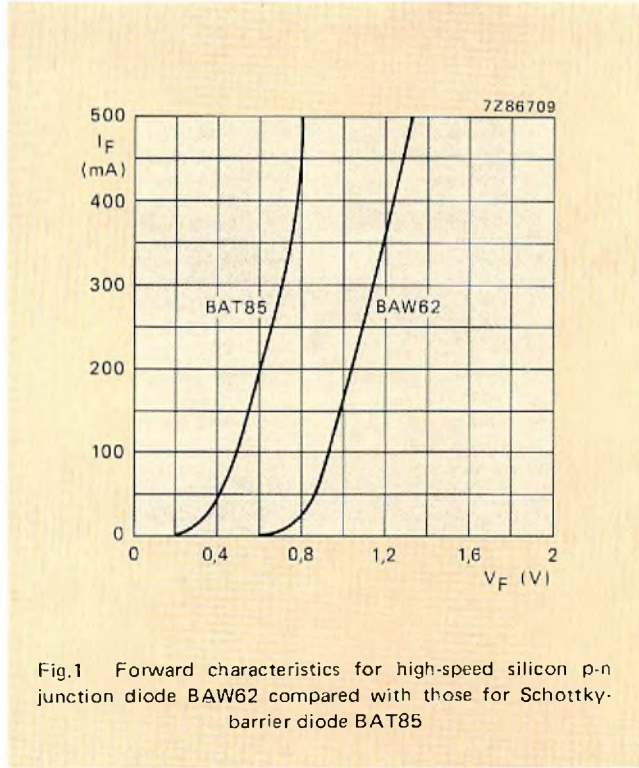
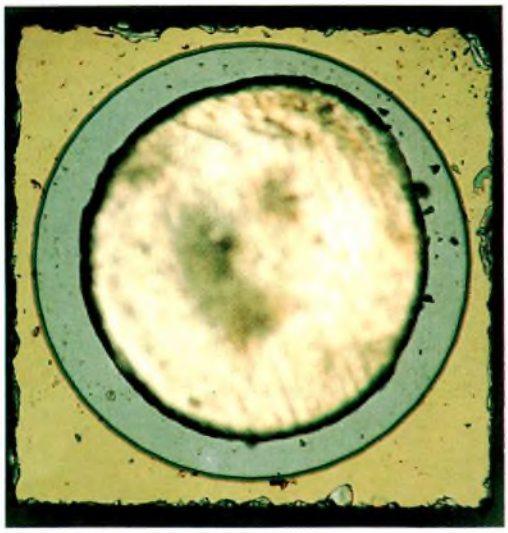
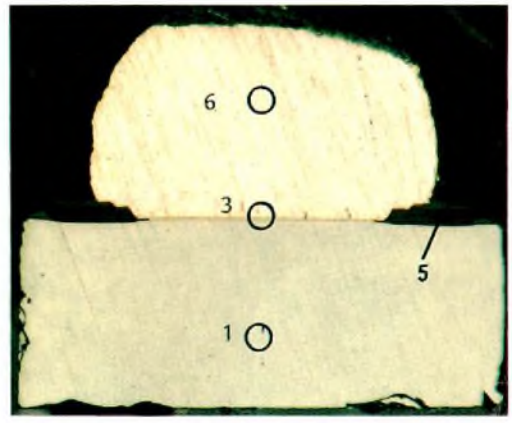


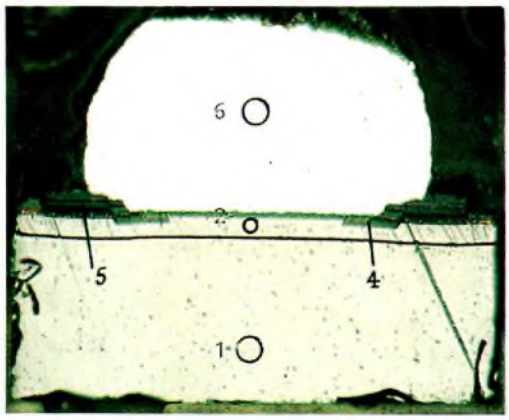
Fig.1 Forward characteristics for high-speed silicon p-n junction diode BAW62 compared with those for Schottky-barrier diode BAT85



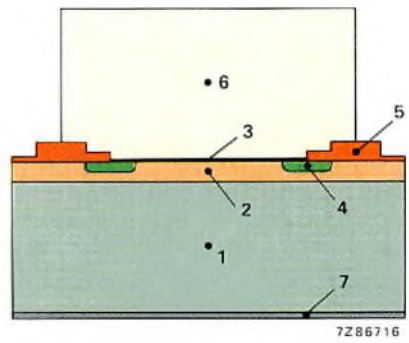
(a)



(c)



(b)



(d)

1. low resistivity doped substrate
2. n doped epitaxial layer
3. metal to silicon contact
4. p doped guard ring diffusion
5. insulation
6. silver pressure contact
7. back contact of the crystal.

Fig.2 Cross-section of BAT83 Schottky-barrier diode with guard ring 'protection' diode.
(a) plan-view
(b) cross-section before etching
(c) cross-section after etching
(d) key to indicated areas

SCHOTTKY-BARRIER DIODE TECHNOLOGY

Planar technology is used to fabricate our range of Schottky-barrier diodes as shown by the illustration of a BAT85 in Fig.2. They consist of a low-resistivity n^{++} substrate (1) onto which a higher-resistivity n-doped epitaxial layer (2) is grown. It is the doping concentration and thickness of this layer, in conjunction with the p^+ guard ring diffusion (4), that defines the reverse breakdown voltage of the diode.

The process is started by growing a layer of thermal oxide on the silicon wafer and performing additional processing steps to stabilize the oxide charges. A ring is then etched in the thermal oxide and p^+ boron is diffused into the ring (4). This completes the p-n 'protection' diode. A contact window is then etched within the inner circumference of the ring and the metal-to-silicon contact (3) is made by evaporation of the metal. This completes the metal-semiconductor Schottky-barrier diode. A thin metal contact layer (7) is added to the base of the structure and a thick silver pressure contact (6) added to the top. Finally, for high reliability and good thermal conductivity, the diode is mounted in a whiskerless glass envelope type DO-34.

OUR SCHOTTKY-BARRIER DIODE TYPE RANGE

The main characteristics of our Schottky-barrier diode type range are given in Table 1 and Fig.3.

Type BA481

Specifically for use in u.h.f. mixers, this diode has the low level of forward voltage shown in Fig.3(a). At a forward current of 40 mA, the forward voltage is about 600 mV and the dynamic resistance is less than 16Ω. Other characteristics which suit this diode for u.h.f. mixers are its low capacitance when reverse biased (Fig.3(d)) and its noise figure of less than 8 dB (Table 1).

Types BAT81/82/83

The Schottky barriers of these diodes are protected by guard-ring diodes with minimum reverse breakdown voltages of 40 V, 50 V and 60 V respectively. As shown in Fig.3 and Table 1, they are characterized by low forward voltage, low diode capacitance and a reverse recovery time of less than 1 ns with a load of 100Ω. These features make them particularly suitable for high speed operation in clipping, clamping and transistor speed-up circuits.

Type BAT85

The Schottky barrier of this diode is protected by a guard-ring diode with a minimum reverse breakdown voltage of 30 V. A special feature of the BAT85 is its low forward voltage at high forward currents. As shown in Fig.3(a), the forward voltage at forward currents above 4 mA is lower than that of the BAT81/82/83. The specified maximum average forward current is 100 mA and the maximum allowed non-repetitive peak forward current ($t < 10$ ms) is 600 mA. This diode is a more technologically advanced replacement for gold-bonded germanium diodes such as the AAZ18.

COMPARISON WITH OTHER DIODES

The main characteristics of Schottky-barrier diodes are compared with those of silicon p-n junction diodes in Table 2. Figure 4 compares the forward and reverse characteristics of Schottky-barrier diodes BA481 and BAT85 with those of germanium point-contact diode OA90 and germanium gold-bonded diode AAZ118.

Type BA481

The forward and reverse characteristics of the BA481 are compared with those of germanium point-contact diode OA90 in Fig.4. With a forward current of 0.1 mA, the forward voltage across the BA481 is about 250 mV and, since the forward characteristic is very steep, the forward voltage only increases to about 450 mV with a forward current of 10 mA. The forward resistance is therefore lower than that of the OA90 which has a forward voltage of 1 V with a forward current of 10 mA. The BA481 is therefore a replacement for the OA90 in f.m. radio ratio detectors.

Type BAT85

The forward and reverse characteristics of the BAT85 and germanium gold-bonded diode AAZ18 are compared in Fig.4. The forward characteristics of the two diodes are very similar although the forward voltage of the BAT85 is somewhat lower than that of the AAZ18 at all levels of forward current. Figure 4(b) however shows that the reverse leakage of the BAT85 is far less than to that of the AAZ18. Table 2 shows that the reverse recovery time for the BAT85 is <5 ns with a 100Ω load. Although this is longer than the recovery time specified for the BAT81/82/83 (<1 ns) due to the different chip layout, it is considerably shorter than that for the AAZ18 (<70 ns). The BAT 85 is a faster, more technologically advanced diode with better electrical and thermal characteristics than the germanium gold-bonded diode, and can therefore replace it in a wide variety of applications.

TABLE 1
Characteristics of our Schottky-barrier diodes (T_{amb} = 25 °C)

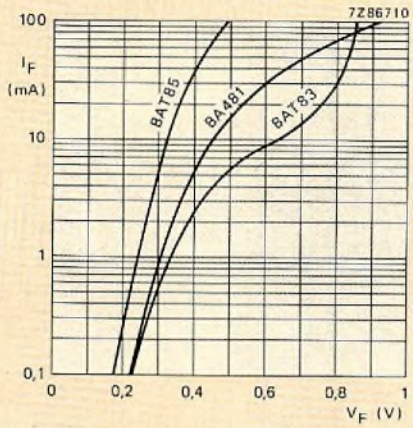
characteristic	BA481	BAT81	BAT82	BAT83	BAT85
reverse breakdown voltage, V_R (V) at I_R (μA)	>4/10	>40/10	>50/10	>60/10	>30/10
reverse current I_R (nA) at V_R (V)	<10/4	<200/30	<200/30	<200/30	<1500/25
forward voltage V_F (mV)					
at I_F = 1 mA	<400	<410	<410	<410	250 typ.
10 mA	<550	<1000	<1000	<1000	<400
100 mA	–	–	–	–	500 typ.
diode capacitance C_d (pF)					
at V_R = 0 V	<1,1	–	–	–	–
1 V	–	<1,6	<1,6	<1,6	<10
reverse recovery time t_{rr} (ns) ($I_F = I_R$ = 10 mA, R_L = 100 Ω)	–	<1	<1	<1	<5
noise figure NF_{SSB} (dB) (f_0 = 900 MHz, f_{if} = 35 MHz, F_{if} = 1,5 dB, I_0 = 2 mA	<8	–	–	–	–
envelope	DO-34				
thermal resistance from junction to ambient $R_{th\ j\text{-}a}$	<0,32 K/mW*				
storage temperature $T_{stg\ max}$	200 °C				
junction temperature $T_{j\ max}$	usually 125 °C** at $V_{R\ max}$				

* on infinite heatsink with 4 mm lead length.

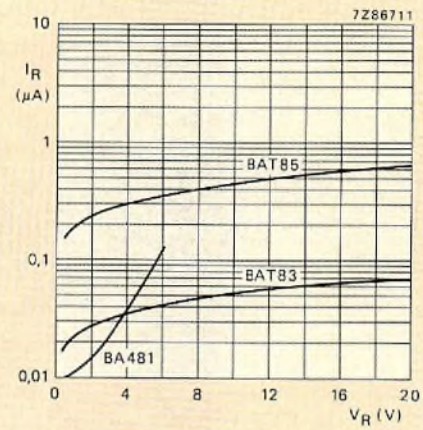
** determined by the thermal stability of the reverse characteristic.

TABLE 2
Schottky-barrier diodes compared with silicon p-n diodes

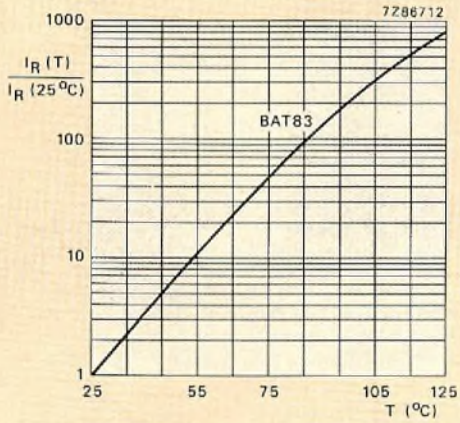
parameter	Schottky-barrier diode	p-n diode
forward knee voltage	adjustable, <500 mV typ.	700 mV typ.
differential forward resistance	depends on crystal R	independent of crystal R
switching time	short due to lack of minority carrier injection	long, depends on minority carrier injection
reverse capacitance	identical for both types	
reverse breakdown characteristic	smooth, round	sharp
reverse energy handling	critical unless a "protection' diode is integrated	not critical



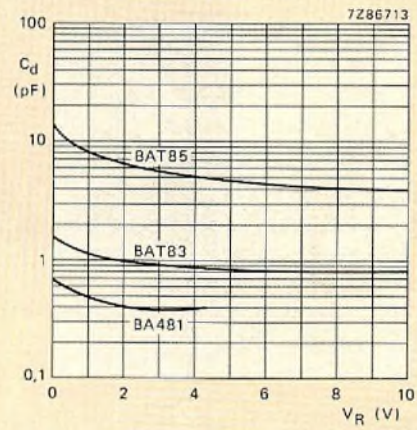
(a) Forward V/I characteristic



(b) Reverse V/I characteristic

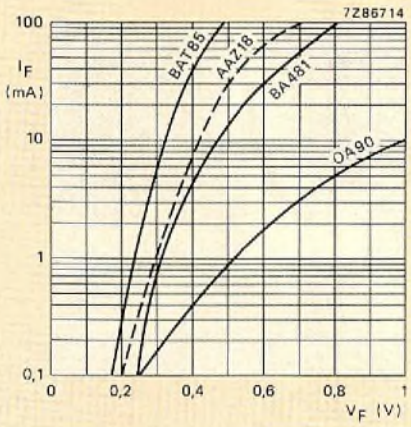


(c) Reverse current as a function of temperature

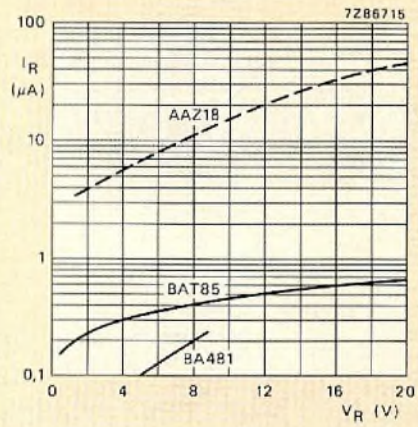


(d) Capacitance as a function of reverse voltage

Fig.3 Schottky-barrier diode characteristics



(a) Forward characteristics



(b) Reverse characteristics

Fig.4 Comparison of the V/I characteristics of Schottky-barrier diodes BAT85 and BA481 with those of germanium diodes AAZ18 and OA90

Isolated Power Modules (IPMs) are now the preferred building blocks for controllable d.c. bridges and a.c. controllers. Each module contains a pair of power devices and has an isolated mounting base. They can be connected by busbars, and several of them can share a common heatsink. Our recently introduced BGX-series of thyristor/thyristor modules are encapsulated in the industry standard TO-240AA outline, and incorporate refinements in chip design which give them outstanding performance and reliability. Polydox passivation (a layer of semi-insulator deposited under the glass) ensures high temperature stability, and a wide p-ring (resurf) introduced along the upper and lower surfaces of the n-base region of the crystal gives high voltage-blocking capability.

The BGX-series currently comprises six basic types, with r.m.s. on-state currents ranging from 50 to 140 A. Versions of each basic type are available with repetitive peak voltage ratings of 600, 800, 1200, and 1400 V. The rate of rise of off-state voltage that will not trigger any device (dV_D/dt) is 200 V/μs for the 600 and 800 V versions, and 1000 V/μs for the 1400 V version. The 1200 V version is available with a dV_D/dt of either 200 or 1000 V/μs.

The article that begins opposite describes a microprocessor-based three-phase fully-controlled a.c. controller using three BGX12-TT IPMs as the switching elements.

Ramp-and-pedestal methods of thyristor triggering in three-phase power controllers are subject to error due to drift and variations in the balance of the phases. The 'look-back' system described here eliminates those errors by predicting the times of impending zero crossovers of each phase on the basis of those just past.

Microprocessor-based phase controller – the 'look-back' system

J.E. GILLIAM

The control of power from a mains supply to a load is of fundamental importance in power engineering. The simplest approach uses a resistor in series with the load, the value of the resistor being varied with changing power requirements. However, since power is dissipated in the resistor, this arrangement is very inefficient. A further disadvantage lies in the need for some form of electromechanical control to adjust the resistor value. A variable transformer introduced between the mains supply and the load provides a more efficient means of power control. the number of secondary turns selected determining the power supplied. This is a great improvement on the simple series resistor, but an electromechanical control is still required to vary the number of secondary turns used.

Electronic control techniques (notably phase control) became possible with the development of thyristors. In phase control, the power supplied to a load is varied by triggering thyristors to conduct for a specific proportion of the mains cycle. If the power control range is to extend from zero to full power, then triggering is necessary on both the positive and negative half-cycles of the supply waveform; the circuit used to achieve this is termed a fully-controlled a.c. controller (Fig.1a). As the trigger angle (thyristor trigger point) of a single-phase fully-controlled a.c. controller varies from 0 to 180°, the power supplied to the load will change from full power to zero (Fig.1b).

Conventionally, the thyristor trigger points are determined using analogue techniques. and while these are adequate for single-phase applications, they have serious deficiencies when applied to three-phase systems. This article describes a microprocessor-based three-phase fully-controlled a.c. controller, called the 'look-back' system*,

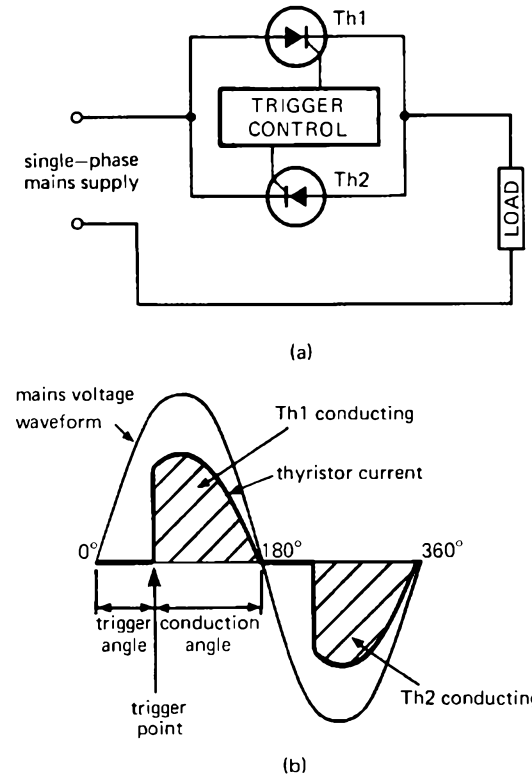


Fig.1 (a) Single-phase fully-controlled a.c. controller (b) Thyristor current waveforms in relation to supply voltage

*British patent application 8205159

which overcomes many of the disadvantages of analogue controllers. Before discussing this system in detail, it will be helpful to review analogue controllers and practical triggering requirements.

ANALOGUE PHASE CONTROLLERS

To trigger a thyristor at a particular point with respect to the mains supply, a timebase must be generated which is in phase with the mains waveform. Conventionally, this timebase takes the form of a ramp voltage synchronous with each half-cycle of the mains waveform. The trigger point is then set by a pedestal voltage whose amplitude is varied in accordance with the required trigger position; see Fig.2. The offset voltage in Fig.2 is required because the circuit which detects the equality of the ramp and pedestal voltages (and hence triggers the thyristor) cannot function at low voltages.

Although satisfactory in single-phase applications, ramp and pedestal techniques cannot fully meet the more exacting requirements of three-phase systems. A three-phase fully-controlled a.c. controller is shown in Fig.3. An important requirement of this circuit is that it should deliver equal quantities of power to each phase of the load. Adjusting the ramps and their offsets will ensure that a ramp and pedestal controller can meet this requirement initially, but drift or variations in the balance of the three-phase supply will inevitably result in subsequent misalignment. This is particularly serious with a transformer or motor load, where even a small degree of phase imbalance can result in magnetic saturation, giving rise to large unbalanced magnetising currents.

PRACTICAL TRIGGERING REQUIREMENTS

For purely resistive loads, the thyristors in a phase controller could be triggered by a single pulse at the required trigger angle (the situation shown in Figs. 1b and 2). However, many practical loads will have a significant inductive component and in such cases the power requirements cannot be controlled by single-pulse triggering. The difficulty arises from the lag between current and voltage, since for a trigger angle less than the phase angle the single trigger pulse will be issued when the load current is flowing in the direction opposite to that required to turn on the thyristor. This situation is prevented by maintaining the trigger signal for a time which is sufficient to ensure thyristor turn-on when the required state of the load current is attained. Since the control circuits must be isolated from the high-voltage thyristor stack, the trigger signal comprises a train of trigger pulses which are passed to the thyristor via a trigger transformer.

The triggering requirements of a phase control system can thus be defined by a set of block waveforms which

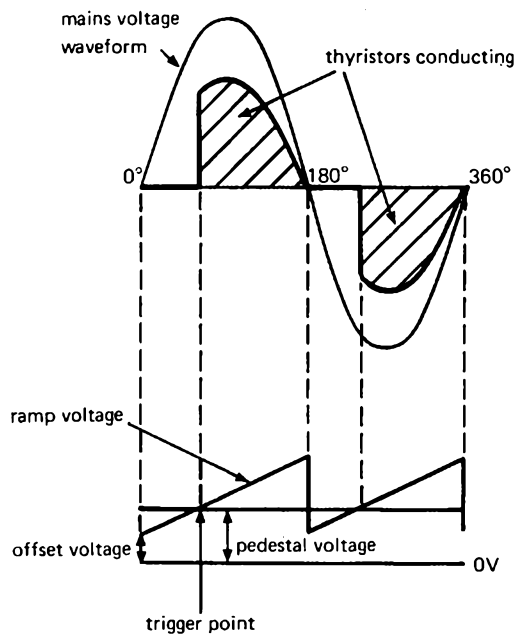


Fig.2 Ramp and pedestal voltage waveforms

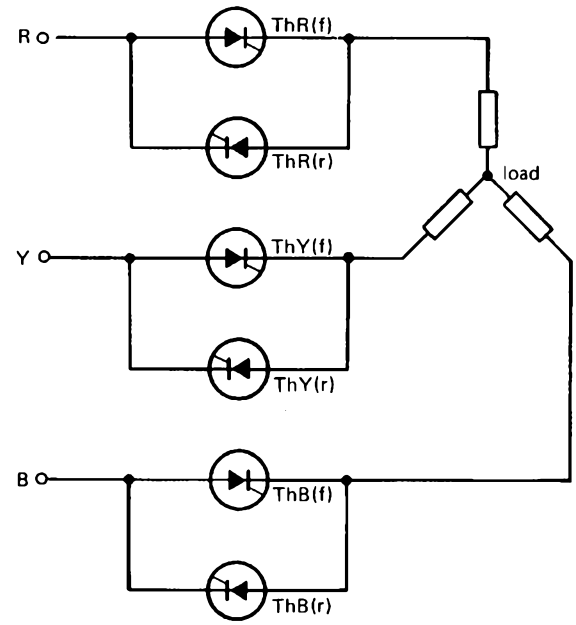


Fig.3 Three-phase fully-controlled a.c. controller. ThR(f) denotes the Red phase forward thyristor, able to conduct from source to load. ThR(r) denotes the Red phase reverse thyristor, able to conduct from load to source. ThY(f), ThY(r), ThB(f), and ThB(r) are similarly defined.

specify the range over which the trigger pulses must be sustained. The block waveforms required to trigger a three-phase fully-controlled a.c. controller over a conduction angle of 20° are shown in Fig.4. Two important features of Fig.4 should be emphasised: the block waveforms terminate at a zero crossover (ZCO) of two phases, and the thyristors are triggered in pairs (ThR(r) with ThY(f), ThR(r) with ThB(f) etc).

The changes in the pattern of the block waveforms as the conduction angle is increased are shown in Fig.5. Up to a conduction angle of 60°, the blocks increase in width. At 60° blocks from the same thyristor merge, and from 60 to 120° blocks belonging to different thyristors overlap. From 120 to 150° the block waveforms are shifted to the left with respect to the mains waveforms.

LOOK-BACK SYSTEM

By exploiting the adaptability of microprocessor-based design, the look-back system largely solves the problem of phase imbalance characteristic of analogue controllers. The system monitors the three-phase mains supply and by responding 'intelligently' to any imbalance in this supply, maintains a balanced set of outputs. In addition to overcoming the deficiencies of analogue controllers, the look-back system provides a number of other advantages.

- Fewer components are required.
- Triggering can start within four cycles of turn-on.
- Synchronisation is maintained during rapid changes in the supply frequency and temporary gross distortions of the supply waveforms.
- The system has high noise immunity.
- A precise balance is maintained between the phases. This is achieved without costly setting-up procedures, and is unaffected by variations in the balance of the three-phase mains.
- The system adjusts itself to supply frequencies in the range 45 to 65 Hz.
- By changing the software, additional functions can be added at little extra cost. For example the input control voltage could be 'sculptured' to give a linear relationship between the control voltage and the output power, or a soft-start could be provided to ensure a steady build-up of flux when driving transformer loads.

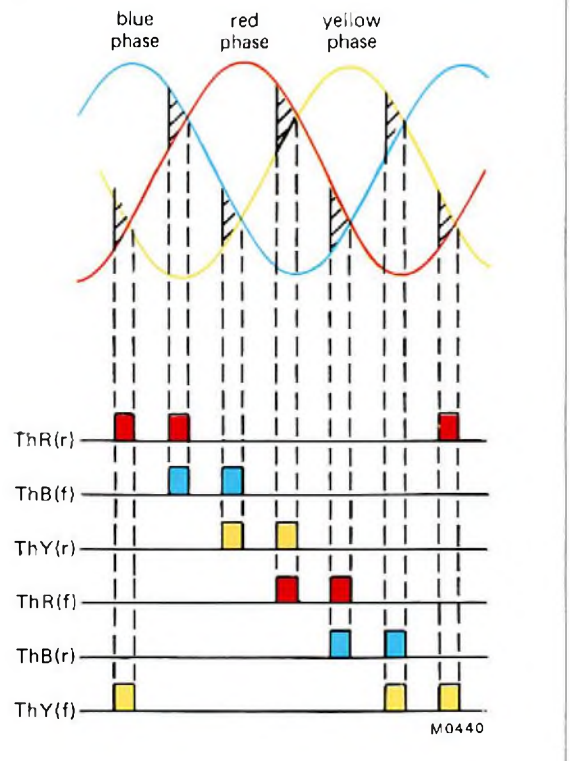


Fig.4 Thyristor block waveforms for three-phase fully-controlled a.c. controller with 20° conduction angle. The voltage waveforms for each of the three phases are shown relative to a virtual neutral.
(ThR(r), THB(f) etc correspond to the thyristors in Fig.3)

Principle of operation

In a three-phase phase control system, each pair of thyristors must be turned on at a point before the appropriate ZCO which will ensure that the prevailing power requirement of the load is met. To do this, the system must establish a timebase synchronous with the mains and estimate the arrival times of anticipated ZCOs. These requirements are interrelated, and in the look-back system the ZCOs of the mains waveforms are used as points of reference for the system timebase.

The memory of the microprocessor used in the look-back system stores continuously updated information on the frequency of the three-phase mains and the separation of the ZCO points. To do this, the microprocessor's internal counter is interrupted and reset at each ZCO point, and the number of counts is entered in RAM. The area of RAM used to store this information is organised as a rotating stack of six 8-bit words. Thus the microprocessor always holds a record of the separation of ZCO points in the previous full cycle of the mains, and is able to 'look back' to this information to estimate the position of the next ZCO. Since the separation of the ZCOs does not vary very much from cycle to cycle, errors in the estimates are small. It is this capacity for generating accurate estimates of the positions of anticipated ZCOs which determines the excellent performance of the look-back system.

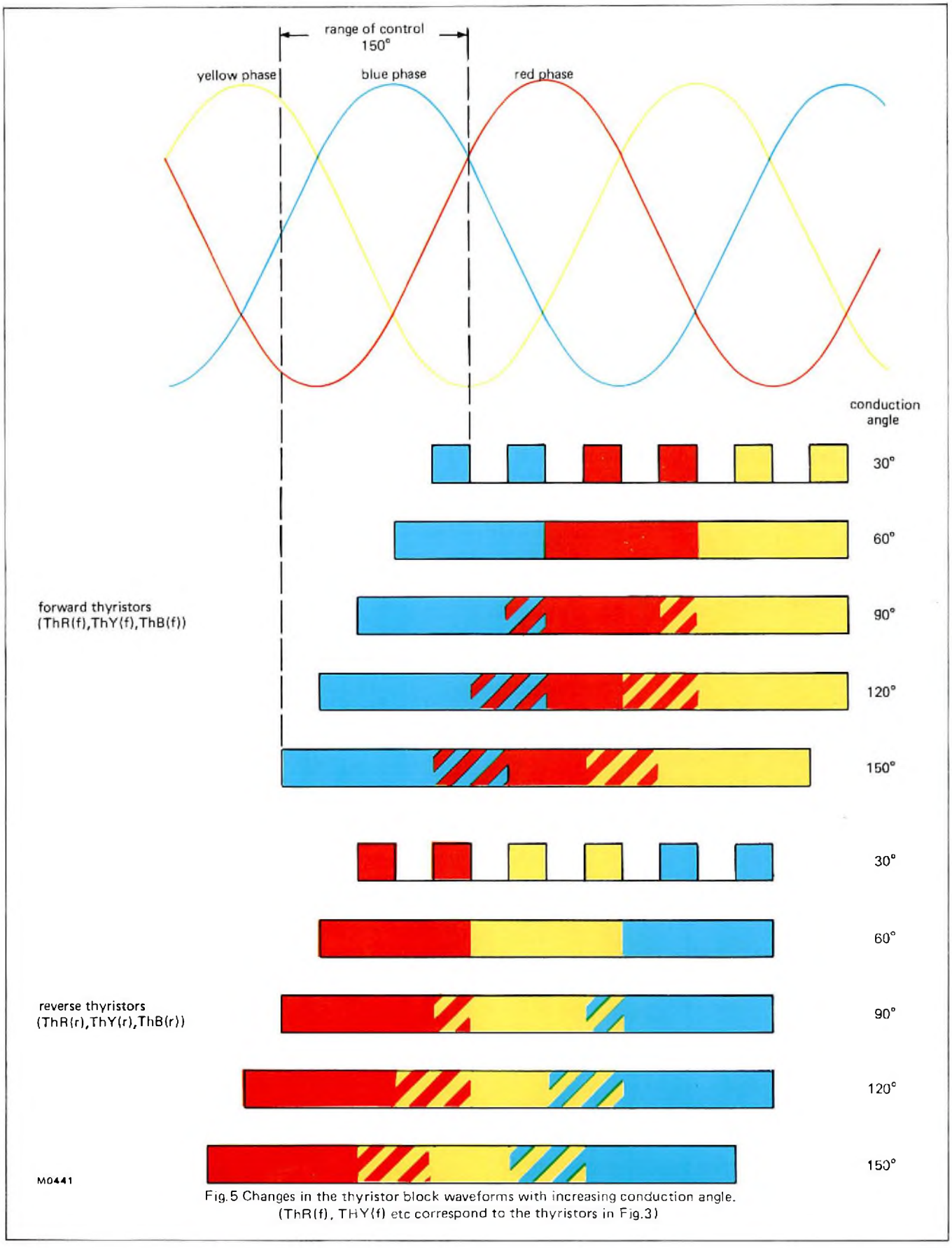


Fig.5 Changes in the thyristor block waveforms with increasing conduction angle. (ThR(f), THY(f) etc correspond to the thyristors in Fig.3)

System components

A block diagram showing the principal components of the look-back system is shown in Fig.6, and the microprocessor and its immediate peripherals are shown in Fig.7. The thyristor stack, comprising three BGX12-TT Isolated Power Modules, is shown in Fig.8. The system uses an 8035 microprocessor, a member of the 8048 family. This device incorporates an asynchronous 8-bit counter, and when operated with a 6 MHz crystal has a machine cycle time of 2.5 μs. An external divide-by-6 operation generates a clocking period for the internal counter of 15 μs. The thyristor block waveforms are generated by switching Port 1 pins LOW, and the trigger pulse trains are generated by gating the block waveforms with a high-frequency chopping signal (Fig.9). After amplification, the trigger pulse trains are passed to the thyristors via trigger transformers, thus isolating the control circuits from the high-voltage thyristor stack.

A microprocessor is a serial device and as such it cannot perform two independent tasks at the same time. In particular, it cannot simultaneously register the arrival of a ZCO and start a thyristor block waveform. To overcome what would otherwise be a limitation on the issuing of trigger pulses, the arrival of a ZCO is registered by the modulo-32 counter, clocked by the same 15 μs clock pulses as the asynchronous 8-bit counter. The modulo-32 counter is started at a set time prior to the anticipated arrival of a ZCO, and is then stopped by a HALT command from the ZCO detector circuit (Fig.7). By a subsequent interrogation of the modulo-32 counter, at a point when thyristor triggering is not required, the microprocessor is able to determine the actual ZCO arrival time.

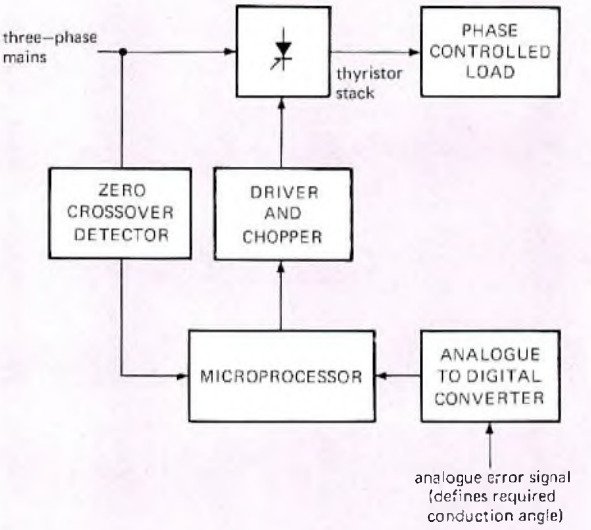


Fig.6 The look-back system — principal components

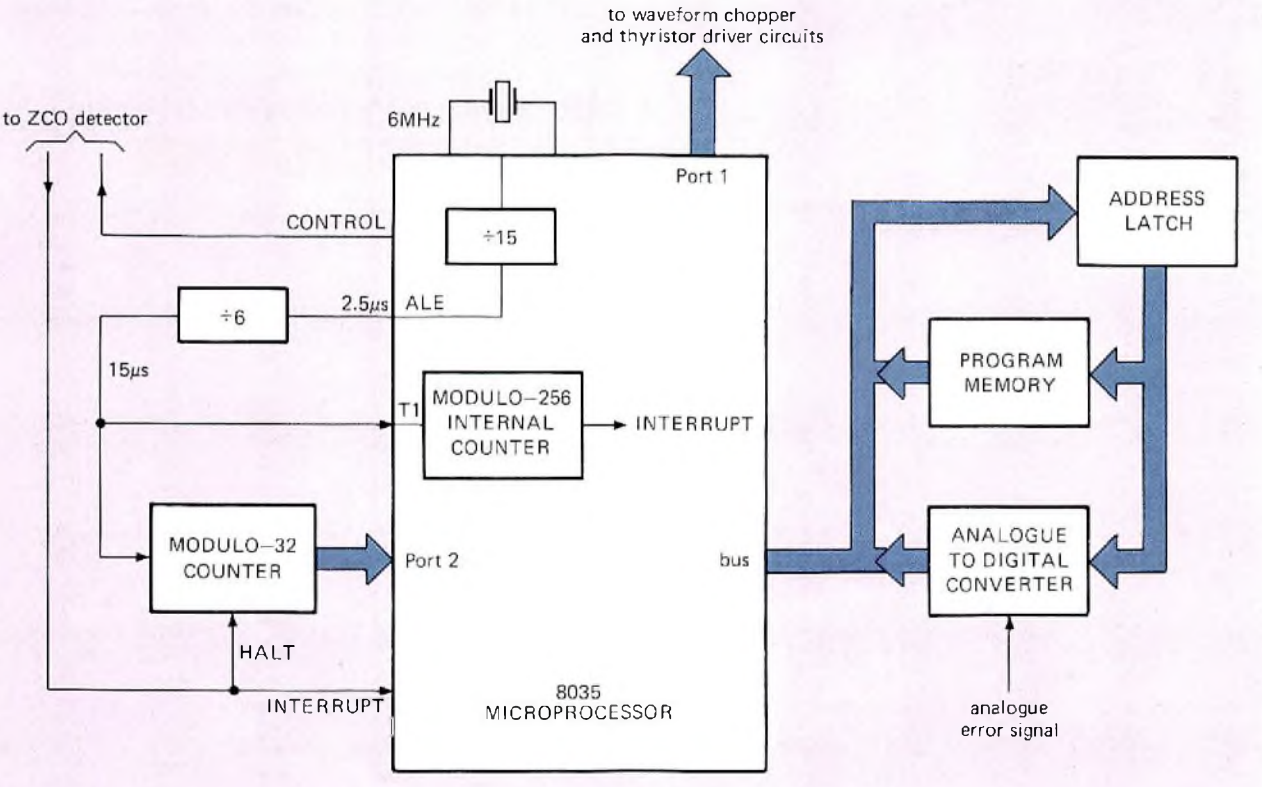


Fig.7 Microprocessor and immediate peripherals.

Performance

Immunity to waveform distortions and maintenance of synchronisation

A single-event displacement of a ZCO pulse, arising from a one-off distortion of the supply waveforms, could degrade the internal timebase. To prevent this, the look-back system rejects any ZCO signal which falls outside a short time interval or 'window' on either side of the expected position of the ZCO. By reducing the width of this window the immunity to such distortions can be increased. As the window is narrowed, however, the risk of rejecting displaced ZCOs which reflect a real change in the supply frequency will increase, and the ability of the system to maintain synchronisation with the supply will therefore be reduced. This problem is particularly acute when the supply is derived from a local generator which may not have the frequency stability of a mains supply. However, because the look-back system is able to predict the position of ZCOs with a high degree of certainty, it can perform well with respect to both immunity to single-event waveform distortions and synchronisation. In practice a ZCO window of 1.6° wide at 50 Hz is compatible with the ability to stay in synchronisation with a supply frequency changing at the rate of 0.56 Hz/s.

If a ZCO pulse is not detected within the window, then in effect the system introduces a substitute ZCO pulse at one of the window edges. This allows the system to continue operation during a temporary loss of synchronisation, especially during temporary gross distortions of the supply waveforms. The window and the substitute ZCO pulse are both generated by software.

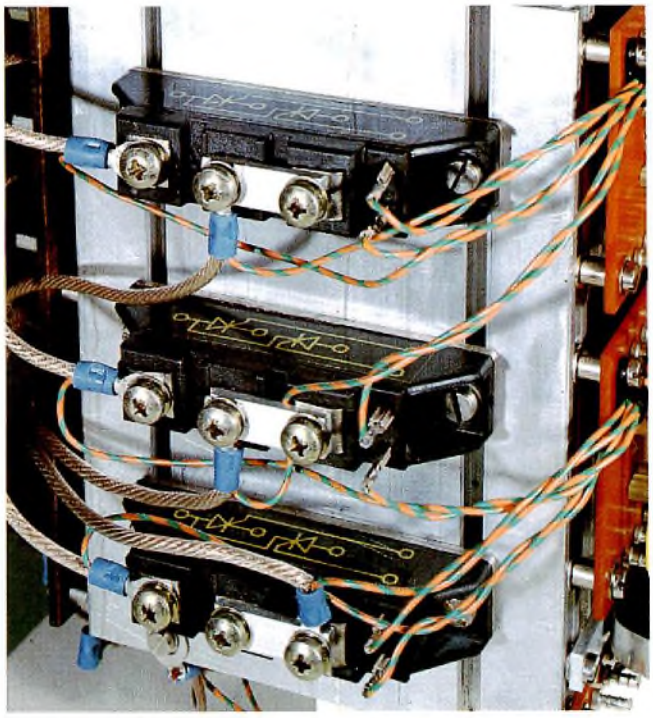


Fig.8 Thyristor stack comprising three BGX12 Isolated Power Modules. Each module contains two thyristors and has a totally isolated mounting base, thereby permitting the three modules to be mounted on a common heatsink.

Noise immunity

Mains-borne interference can result in spurious ZCO pulses. In assessing the influence of such pulses on the look-back system, three situations must be considered.

1) The modulo-32 counter is inactive. A spurious ZCO pulse will then have no effect on the counter and will not degrade the performance of the system.
2) The modulo-32 counter is being incremented prior to a HALT command (true ZCO pulse). A spurious ZCO pulse could then inhibit a single increment of the counter.

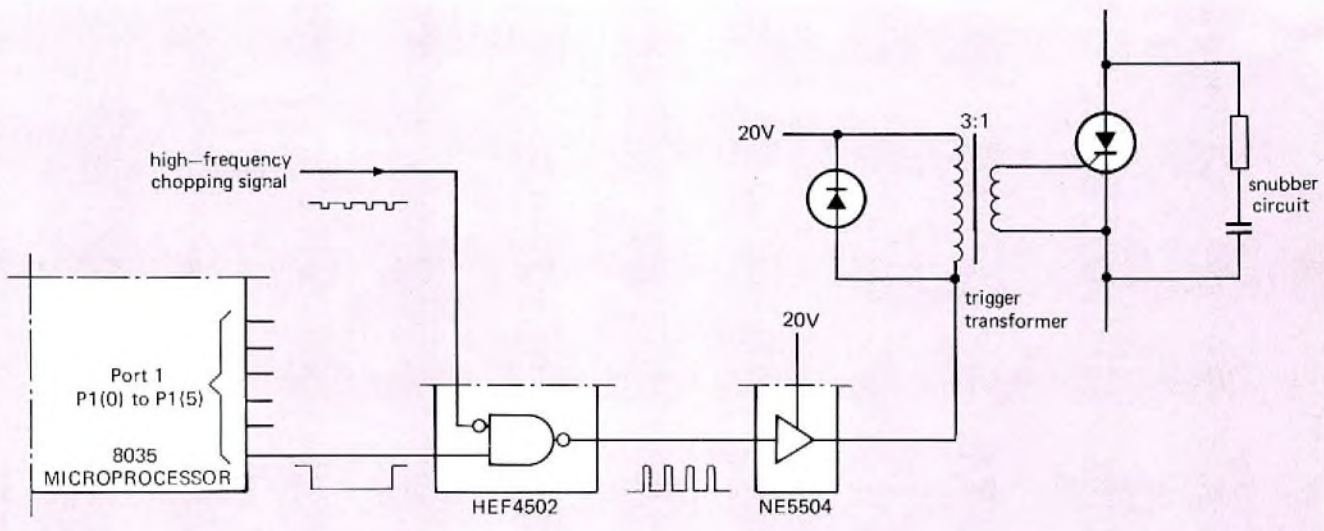


Fig.9 Waveform chopper and thyristor driver circuits

3) The HALT command is HIGH prior to the final counter value being read by the microprocessor. A spurious ZCO pulse could then momentarily disable HALT producing a single erroneous increment of the counter.

Even in the last two situations the effect on the system will be marginal, and it is clear that overall the look-back system has high noise immunity.

Time to find synchronisation

There is often a need to 'inch' machinery, and for reasons of safety this is done with the mains isolator. It is thus very important for a phase control system to synchronise promptly with the mains. The look-back system synchronises within four cycles of switching on the mains, at which point triggering can commence. This delay is not perceptible to the operator.

Resolution

The resolution of the look-back system is ultimately limited by the finite size of the microprocessor's internal counter, since this determines the maximum counter value which can be assigned to a 60° interval. With an 8-bit counter, and a 15 μs clocking period, a 60° interval at 50 Hz will generate a counter value of 222, so the best attainable resolution at this frequency is 60/222, or 0.27°. In practice, the look-back system does not attain this resolution but is constrained by the conversion of the analogue error signal into a digital input for the microprocessor. The output of the A-to-D converter is an 8-bit word, defining a conduction angle of between 0 and 150°, so the resolution is 150/256, or 0.58°. By using a 10-bit A-to-D converter, the resolution of the system could be improved, up to the limit of 0.27°, but this is not considered necessary for phase control.

STRUCTURE OF THE LOOK-BACK PROGRAM

The structure of the look-back program is shown in Fig.10. The program may be divided into two parts. Part 1 includes an initialisation procedure and the establishment of the timebase. Part 2, which is cyclic in structure, maintains synchronisation and generates the thyristor block waveforms.

Part 1

Activating the reset line of the microprocessor starts an initialisation routine which sets the flags and registers and enables the external interrupt pin. This pin is connected to the output of the zero crossover detector, which at this point is initialised to produce one pulse for each full cycle of the mains. By measuring the time between the next two pulses from the ZCO detector, the microprocessor checks that the mains frequency is within acceptable limits – greater than 45 Hz and less than 65 Hz. If the mains frequency is acceptable, it is used to prime all six of the 60° look-back memory locations. The control line to the ZCO detector (Fig.7) is then activated so that ZCO pulses are generated for every 60° of the mains waveform. Over the next two full cycles of the mains, the look-back memory locations are adjusted so that they reflect the true separation of ZCOs during this period. The microprocessor's timebase is then synchronised with the mains, and triggering is started.

Part 2

This section of the program continually processes the information required to generate the thyristor block waveforms and maintain synchronisation. A complete description of its operation would be extremely complex, but an understanding of the basic principles can be obtained by following a simplified description through a series of successive ZCOs; see Fig.11.

The situation depicted in Fig.11 covers a pair of block waveforms to be started between ZCO_n and ZCO_{n+1}, and terminated at ZCO_{n+1}. The starting position of the waveforms is calculated during the period between ZCO_{n-1} and ZCO_n (the preparation time), using the most recent error signal and the estimated separation of ZCO_n and ZCO_{n+1} as stored in the look-back memory. The speed of the microprocessor is such that it is able to calculate the starting position two or three times before the most recent estimate must be committed for use. This ensures a very short response time for the system. Following ZCO_n, the microprocessor's internal counter is loaded with a number that will generate an overflow of the counter at the calculated position of the start of the block waveforms. This overflow generates an internal interrupt, and the appropriate pins of Port 1 go LOW defining the start of the waveforms.

A further counter overflow, occuring just prior to ZCO_{n+1}, initiates the sequence which terminates the waveforms at the anticipated position of ZCO_{n+1}. The modulo-32 counter is then interrogated to determine the true time for the occurrence of ZCO_{n+1}, and the relevant look-back memory location amended as necessary. If the measured position of ZCO_{n+1} differs from the anticipated position by more than three 15 μs clock periods, or 45 μs, the look-back memory location is amended as though the measured position was 45 μs or –45 μs from the predicted position for positive and negative errors respectively. This limitation on the allowed error in the position of a ZCO is equivalent to the generation of a ZCO window 90 μs wide.

To summarise, the operation of Part 2 of the look-back program consists essentially of the repetition of the

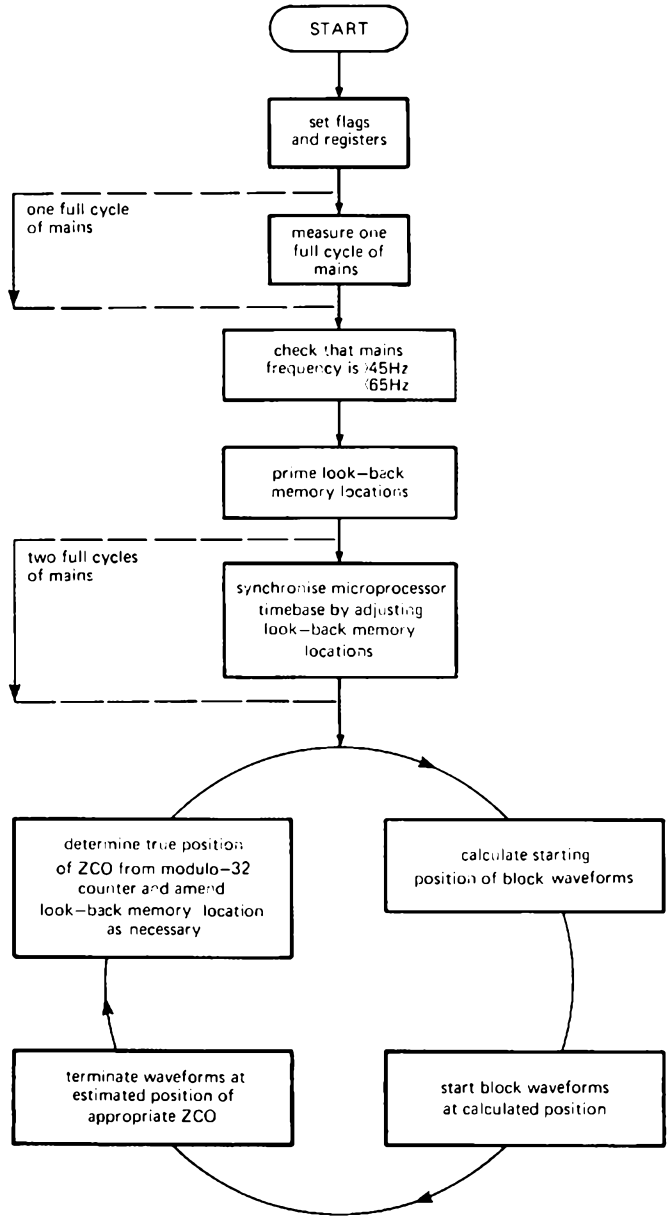


Fig.10 Structure of the look-back program

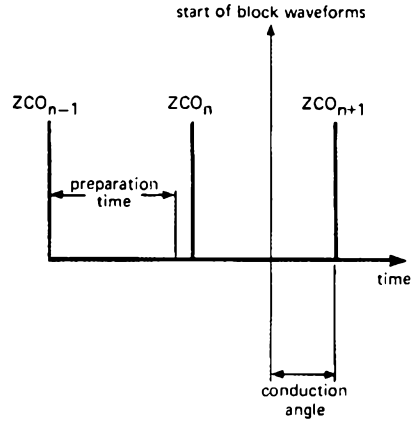


Fig.11 Timing diagram for establishment of thyristor block waveforms. The conduction angle is in the range 0 to 60°.

following sequence: calculate the starting position of the block waveforms, terminate the waveforms at the appropriate ZCO, then monitor the true position of the ZCO to maintain the integrity of the internal timebase.

FUTURE DEVELOPMENTS

While the system described in this article has been designed specifically for a fully-controlled a.c. controller, the basic operating principles of the look-back system are applicable to all types of a.c. controller or three-phase bridge. As a future development, the look-back program could be structured to provide the basis of a universal three-phase power controller.

The ppm (for 'parts per million') concept applies primarily to the prevention of component-related rejects during equipment assembly. Use of a ppm system requires not only that the IC manufacturer's quality control system is effective, but also that the IC manufacturer and equipment manufacturers to whom he supplies cooperate fully after delivery of the ICs, with the object of further improving quality.

PPM management – a tool for IC quality improvement

J. TH. VERSCHOOR

The pace of development in the field of microelectronics is possibly unique in engineering history. Continual advances in technology result in a succession of new manufacturing processes, each extending the possibilities available to the circuit designer. As a result, solutions are now available for electronic problems that were, themselves, undreamt of until recently. LSI circuits are now being delivered with many thousand transistor functions to a chip: current 4 μm device geometry is giving way to 2 μm geometry; up to 10^6 components can be produced on one chip – as in a 256 K RAM. Figure 1 shows, by way of example, a currently-produced LSI chip.

Such rapid development has, inevitably, radically altered the design of electronic equipment. These changes are characterised by:

- new and extended system functions
- increased system complexity, with rapid growth in component and function count
- more comprehensive integration of sub-systems and circuits
- greater rationalisation, coupled with the increased use of automatic assembly methods
- working of materials, discrete components and ICs closer to their maximum capacity.

These design trends have inevitably been accompanied by

- more stringent quality requirements for both component manufacturer and user
- the approach of typical operating conditions to Absolute Maximum Ratings
- a reduction in the accessibility of individual circuit functions.

There is, moreover, intense world competition in the industry, but cost structures vary widely.

In these circumstances, IC manufacturers and OEMs (Original Equipment Manufacturers) now combine to formulate the direction to be taken by new developments, in a situation of continuous innovation.

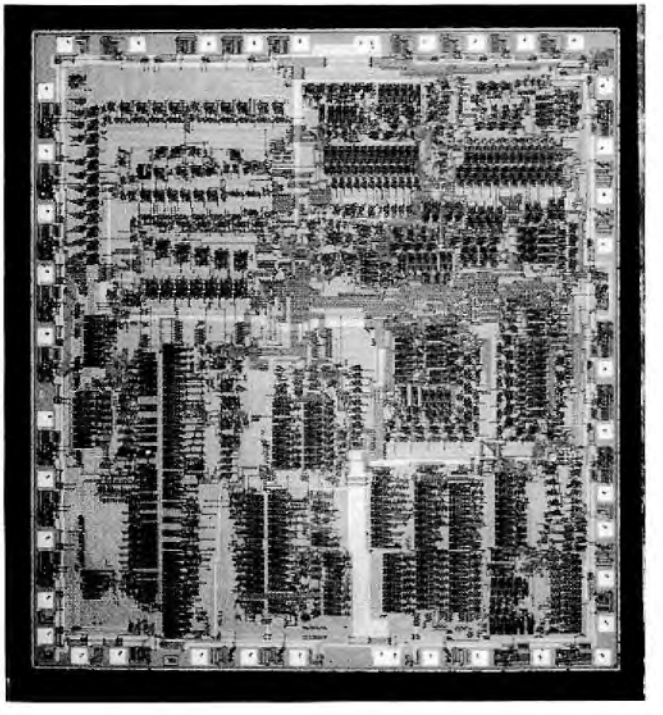


Fig.1 The SAA5070, a microprocessor peripheral circuit for viewdata. Chip area is about 29 mm^2

THE CURRENT QUALITY SITUATION

Quality in development and production

Process release

ICs are manufactured in production lines dedicated to particular process technologies. Process-control modules – test slices or circuits – processed together with production devices enable process conditions to be monitored and maintained. Before being approved for full-scale production, every new process or production line is subjected to a rigorous quality evaluation before process release is granted.

Device development

The device-development engineer must adhere strictly to the characteristics and capabilities of the process technology. These define such aspects as transistor parameters, track clearances and structural dimensions. Design data that determine the conformance and reliability achievable are also dictated by the process. These include current density, and the characteristics of bonds and insulation layers. Since these properties are already known, the combination of an approved process and adherence to design rules results in very reliable devices.

The electrical properties of individual device types are those typical of the process used in their manufacture. Thus, analogue devices, and digital devices such as NMOS dynamic memories, have their own particular characteristics. To some extent, reliability is also process determined. It is, therefore, imperative that the quality requirements of each new IC type are clearly defined before development commences, and to ascertain that this quality is realisable with the chosen process technology during preparation of the initial specification.

In production, the performance and quality of devices are assured by the manufacturer's Quality Control Department by process monitoring and product evaluation.

Pre-delivery inspection and quality control

Final electrical testing

A 100% electrical test is performed on every device, using automatic test equipment, immediately before delivery. In order to obtain a test specification that matches the performance required in the intended application, consultation between manufacturer and OEM is necessary. Such consultation can result in a final electrical test more closely suited to the application requirement.

Lot release

Before a lot of ICs is cleared for delivery, samples are taken by the Quality Control Department and checked for conformance to specification. These samples are taken after marking and packing, according to sampling plans of IEC Publication 410 (MIL-STD-105D). Release of the lot depends on the set AQL being achieved for a key device characterstic or group of characteristics.

Fig.2 Quality in diffusion: Inspection of the step-coverage of the aluminium metallisation in a LOCMOS circuit, using a scanning electron microscope

In practice, the actual level of defectives delivered is far below the AQL. Note that process and inspection activities are organised on zero-defect goals.

OEM rejects

Between being received by the OEM and completion of the equipment in which they are incorporated, ICs undergo a number of operations, from incoming inspection to final equipment tests. *Device characteristics are, of course, required to remain within set limits through all these operations*, but evaluations that take place at every stages of equipment assmebly do reveal rejects.

Incoming inspection and belt rejects are often due to inadequate correlation between the manufacturer's final electrical test specification and application-oriented tests performed by the user ('correlation defects'). With the more complex digital ICs, and linear types, it is not possible to define all the essential characteristics in the initial specification. *It is, therefore, important that manufacturer's and OEM's test methods and criteria are compare at the earliest possible stage.*

Causes of rejects* during equipment assembly as revealed by analysis fall into three broad categories. These are shown in Fig.3 which is based on experience during 1981 and shows the importance of analysing devices rejected at any stage in their life. The information so obtained can then be used to identify process or design faults, incorrect use or other problems, and to initiate corrective action.

The stress conditions imposed during endurance testing are so chosen by the device manufacturer that the results obtained can be used to forecast reliability over extended periods. Where possible, these results are combined with experience of devices in the field. Figure 4 shows the relationship between failure rate and complexity for ICs. This shows that, in addition to the advantages of miniaturisation, more extensive integration yields a significant increase in the reliability of a given number of functions. This trend can be expected to extend to VLSI devices.

Analysis reveals mainly non-systematic faults that can be correlated with process inadequacy and thus lead to corrective action. But some failures are certainly application dependent. Experience shows that corrective action can take a long time in such cases.

Quality feedback loops

ICs can be rejected at any stage of their production and use. Figure 5 shows how, by analysing these rejects, feedback can be applied to the manufacture, testing and application of devices, with a consequent increase in the understanding

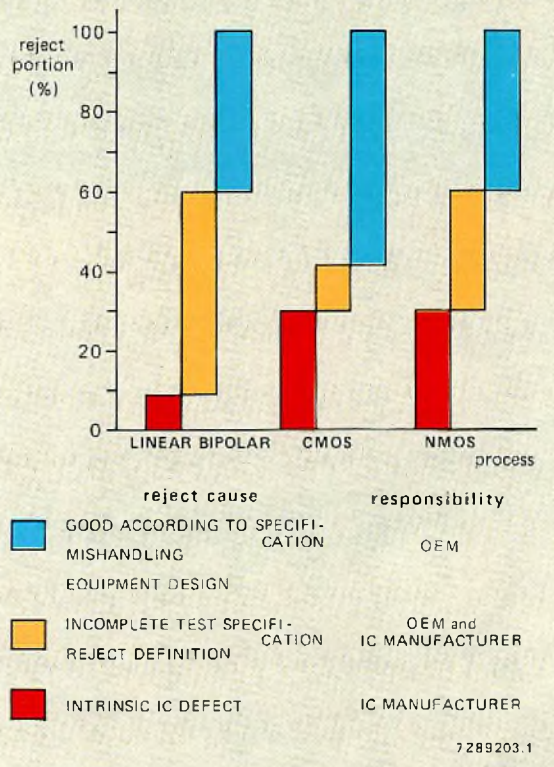


Fig.3 Distribution of causes of IC rejection during 1981 for linear-bipolar, CMOS and NMOS ICs

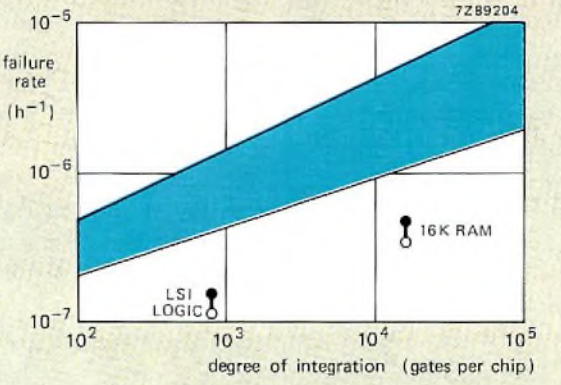


Fig.4 Predicted failure rate as a function of complexity for digital integrated circuits in various technologies and encapsulations. The shaded band is derived from MIL-HDBK-217C; points are results of accelerated life tests; circles are field failure rates for LSI logic devices and 16K RAMs. It can be seen that the reliability *per function* increases with the complexity of the IC: this trend can be expected to continue into VLSI

* The following definitions are used in this article:
Reject: a product that has been rejected for any reason.
Defect: a product whose parameters lie outside specified limits, and/or which does not function in the intended application.
Failure: a product that has ceased to perform its required function.

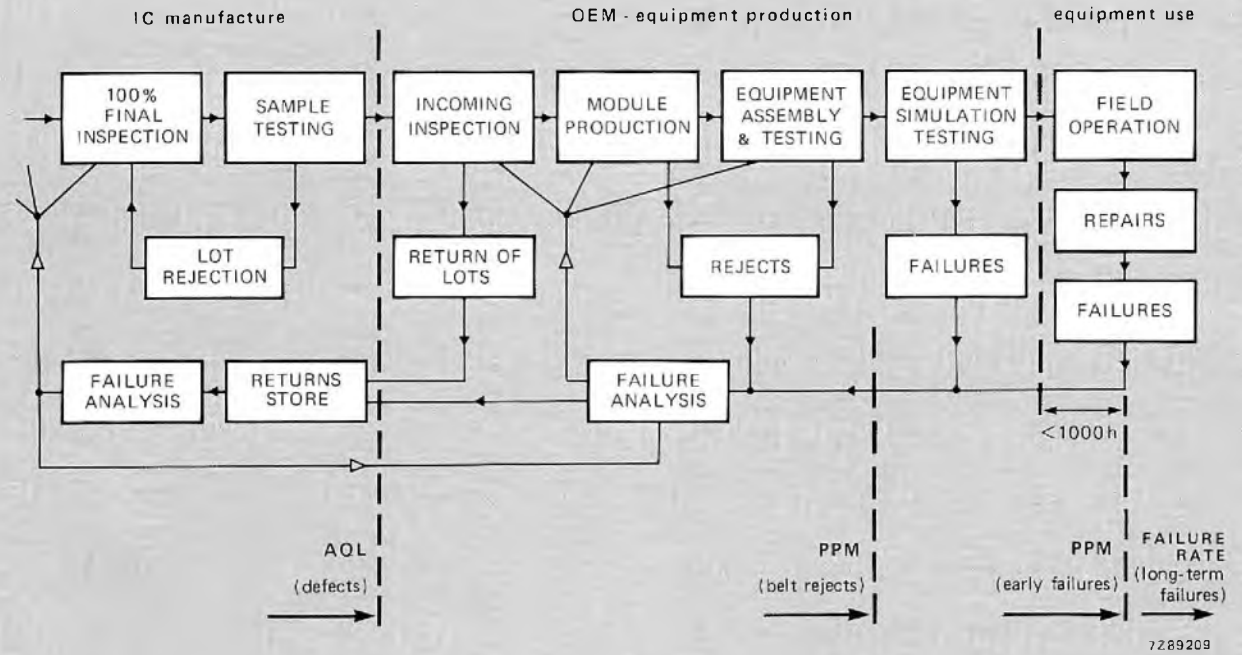


Fig.5 By analysing the rejects from all stages of the life of an IC, feedback can be applied to the manufacture and application of devices, with consequent increase in the understanding of the problems of the quests for higher quality. However, fed-back data must be both accurate and detailed

of the problems of the quest for higher quality. Corrective action, resulting in higher reliability in the field, completes the feedback system.

Such a complete feedback system requires the development by both manufacturer and OEM of a common quality-improvement strategy. Achievement of higher quality requires both more application-oriented testing, and more information feedback for corrective action by the manufacturer. Increasing the sample size for AQL determination by the manufacturer will not, alone, satisfy these requirements: primarily because the tests carried out cannot normally be dedicated towards any individual application. However, routine testing carried out by the OEM can satisfy the requirements, but only if operating and test conditions, and their spreads, are fully communicated to the IC manufacturer.

PPM MANAGEMENT

The ppm concept applies primarily to the detection of rejects during equipment assembly. The ppm level, in the context of quality control, is the number of rejects in one million devices.

The main reason for using ppm as a measure of reject level is, of course, that it results in numbers of more relevance than percentages. Furthermore, there is then no danger of reject level and AQL data being confused. A more subtle advantage of ppm is that the higher numbers (0.1% = 1000 ppm; 0.01% = 100 ppm) further stimulate the drive towards better quality. The use of the ppm system requires not only that the manufacturer's quality-control system is effective, but also that manufacturer and OEM cooperate fully after delivery of ICs with the object of further improving quality.

Note that ppm cannot replace AQL. The AQL system will remain in use as a formal basis for lot acceptance or rejection on the basis of sample testing. Moreover, AQL is an essential adjunct to contractual quality limits: for example, for processing complaints as defined in procurement contracts. However, AQL does not define actual quality levels, which is the purpose of the ppm system.

The strategy of ppm

The fundamental feature of the ppm concept, which is now accepted by electronic component manufacturers and OEMs throughout the world, is *the setting of targets for quality-improving activities*. Such targets should always be both *achievable* and *measurable*. Hence, although each successive target represents a step towards the ideal of zero defects, this is not in itself a suitable target at any stage. Not only are some defects inevitable, but the cost of preventing defects increases disproportionately as their number tends toward zero. Moreover, measurement accuracy is never 100% either, so that a zero-defect target is not measurable with certainty.

PPM system parameters

Central to a successful ppm strategy is the choice or specification of the following:

A *quality indicator* that reflects the overall quality of the product. For ICs, non-proper functioning is the usual quality indicator.

Quality-level target of the quality indicator. If this is exceeded, corrective action must be taken.

Quality-level targets:

- apply to conformance as well as reliability
- cannot be guaranteed by the manufacturer, but
- express a sincere intention of quality-improving activity, actual results being compared with the targets at regular intervals
- must be seen as goals requiring a *joint* effort by manufacturer and user.

Product range. The range of product types that may be considered technically coherent in the context of the specific application.

Time schedule for the achievement of the quality target.

PPM-policy

We have formulated the following general policy for a ppm system based on these parameters:

The management of the company will, for all IC product categories, promote and pursue task-setting in the form of quality-level targets expressed as the maximum number of defective items per million products (ppm) together with firm time schedules.

Application of ppm

The quality-level target is the combined reject level, expressed in ppm, for tests carried out during and after the assembly of equipment:

- incoming inspection
- production-line testing of modules or sub-systems
- final testing of finished equipment
- equipment burn-in or screening test.

Fall-off and call rates

The overall reject level of ICs in equipment during assembly *(belt rejects)* is directly related to the average number of repairs required per 100 sets *(the fall-off rate)*. It is often suggested that the average number of service calls per set per year in the field *(the call rate)* is directly related to the fall-off rate. It can now be shown that, for linear integrated circuits, fall-off and call rates are not directly related.

The first period of field operation can be simulated by a life test under typical operating conditions lasting 300 h to 1000 h. Defective devices during that test, or during initial field operation, are termed *early failures*. In Fig.6, normalised early failures are plotted against normalised belt rejects for tv receivers. Each point relates to a particular type of linear IC. It is clear that there is very little correlation between early failures and belt rejects: the calculated correlation coefficient is 0.11. If the circled point (1.4/4.2) is excluded, the correlation coefficient rises to only 0.17 – still very low.

The reason for this poor correlation can be found in the failure causes themselves. Belt rejects are usually due to defects like open and short circuits that are not time dependent. Early-failure mechanisms, such as degradation and leakage, are time dependent. The other major cause is the high percentage of correlation defects in the belt rejects (see section *Pre-delivery inspection and quality control*) not present in the early failures.

This indicates that *separate quality-level targets should be set for early failures and belt rejects.* These determine the component-related portion of the call rate.

Conformance and fall-off rate

The conformance (zero-hour quality) of devices delivered by the manufacturer must also be high: it directly influences the level of belt rejects and, thus, the equipment fall-off rate.

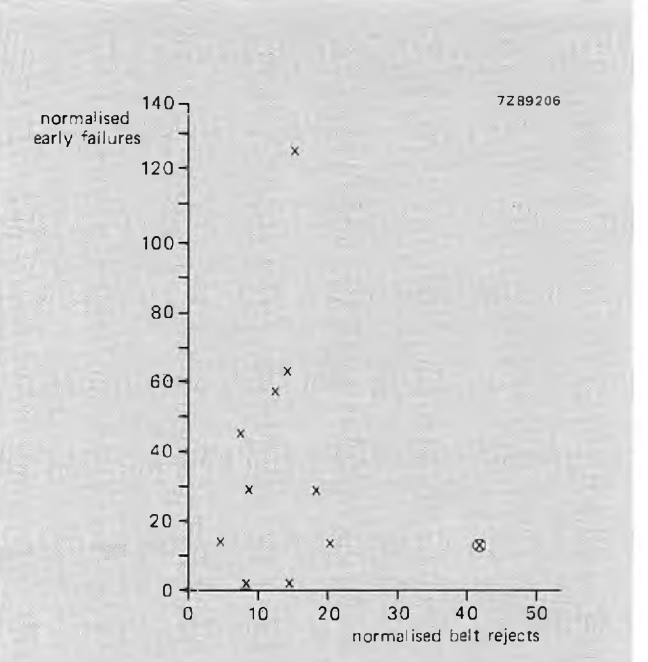


Fig.6 A plot of normalised early failures and normalised belt rejects for TV receivers showing that there is, in fact, little relationship between the two. The correlation factor is only 0.11 for all points, and rises to no more than 0.17 if point ⊗ is disregarded

Line inspection and call rate

Line inspection and quality control during IC manufacture followed by corrective action reduces the incidence of die and assembly defects. This 'in-line quality' is associated with early failures and reliability generally and, therefore, directly influences the call rate.

Manufacturer's quality-level targets

As part of the ppm strategy, the manufacturer will define internal quality-level targets. Conformance will be measured as a process average during acceptance testing. Line quality will be maintained by intermediate quality controls, such as pre-seal visual inspection.

Figure 7 summarises the relationships between the quality controlled by the IC manufacturer and the quality experienced by the OEM.

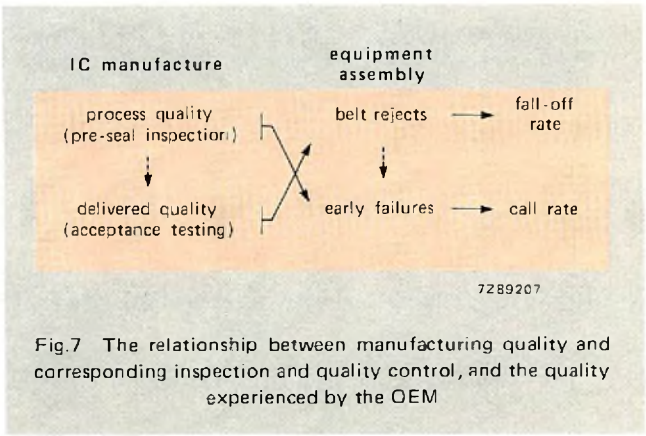


Fig.7 The relationship between manufacturing quality and corresponding inspection and quality control, and the quality experienced by the OEM

PPM verification

Fundamental to the quality-improving role of the ppm system is regular comparison of actual quality and agreed quality-level targets. This entails the collection by the OEM of accurate and detailed data on the quality experienced.

Early-failure information is readily available from simulation testing, provided the quantity involved, operating conditions, and number of rejects are known. Information collection from the equipment-assembly process itself is more complicated: additional administrative and organisational measures are necessary if useful data are to be obtained.

Finally, if the achievement of quality-level targets is to be verified, the conditions set out under the next three headings must be fulfilled.

Sufficient quantities

In order to obtain an acceptably high confidence level for the fraction defective in the original production lot of an IC type or group of types, a sufficiently large quantity of devices must be involved in the quality-level target verification. Thus:

For a Target of 100 ppm and 10^5 devices tested, the upper and lower confidence limits for a 90% confidence interval are 7 and 16 devices rejected. Thus, less than 7 rejects means that the target is met; more than 16, that it is not met. Between 7 and 16 lies a band of uncertainty.

Where possible, such large quantities should be obtained by combining technically coherent or structurally similar device types used in the same or similar applications.

Then, depending on the fall-off and call rates required, the ppm quality level for a range of ICs can be defined for

- type and position in the equipment
- type only in the equipment
- a group of structurally similar types
- a group of types that are technically coherent in application.

Sufficiently large quantities for verification purposes can also be achieved by extending the period over which quality-level verification takes place. The maximum verification period that can be used is, however, limited by innovation and alteration in both component and equipment design, and production. Similarly, the minimum verification period is determined by the time it takes to work the required verification quantity through equipment production. In practice, the optimum verification period seems to be about 3 months.

Unambiguous reject data

For reliable verification of quality level, it is vital that the number of rejects is expressed as a percentage of a defined number of devices used, and that the devices that comprise this total are clearly related to the rejects concerned. Thus, random mixing of batches with different date codes, or from different manufacturers, during equipment assembly leads to verification difficulties.

Complete failure analysis

It is essential that all devices rejected during equipment assembly and simulation testing are returned to the manufacturer *after* functional analysis by the OEM. Alternatively, some agreed, well-defined sample of the rejects may be returned.

The rejects are analysed by the manufacturer. In some cases, a sample only of the rejects is analysed. In either event, a complete review of the failure analyses must be given and must involve all devices rejected by the OEM, broken down into the following categories, in ppm.

- Manufacturer-related failures/defects
  - inherent device failures/defects
  - test or inspection escapes.

- Incomplete test specification (manufacturer and OEM related
  - mismatch between test specification and device specification or application conditions (correlation problems)
  - differences in failure/defect definitions.
- OEM-related rejects
  - unjustified replacement
  - faulty application or handling (e.g. overstress).

In order to make these distinctions, a clear agreement between manufacturer and OEM is required on failure/defect definitions.

Information feedback

In order to demonstrate the achievement of quality-level targets, it can be seen that considerable cooperation between manufacturer and OEM is required. However, the costs involved in such a cooperative programme are, for both parties, such as to be justifiable only where a fairly large volume of devices is involved. It is our intention to build up such cooperative relationships with large-volume users with the aim of achieving regular ppm verification under the conditions discussed in the previous section.

In order to help smaller-quantity users of ICs maintain and improve quality experienced, detailed information will be provided both directly and through regular publication, supplemented by contact where necessary.

In the professional areas where small quantities of devices of very high quality are required, such as aerospace and telecommunications, the quality level is not only protected by regular discussion of failure analysis results, and by the necessary corrective action, but the ppm verification system is replaced by stringent preventive measures, to avoid any reliability hazard.

Where the full ppm strategy is implemented, agreement on the form of the information to be fed back is essential.

OEM-generated information

The information fed back to the manufacturer concerning rejects must cover the following:

- Origin of rejects returned:
  - incoming inspection
  - belt tests
  - final equipment test
  - burn-in test
  - simulation test or field operation.
- Rejects to be returned:
  - all rejects
  - an initial sample
  - only when in excess of a set proportion of total devices
- Additional data:
  - test or measurement conditions
  - device operating time
  - environmental conditions
  - electrical conditions
  - failure mode
  - total quantity involved
  - persons to contact
  - frequency of failure returns (weekly, monthly, . . .).

Manufacturer's response

The manufacturer's response to the rejects and supplementary information from the OEM shall comprise:

- confirmation of receipt of rejects
- preliminary analysis results
- final analysis report
- corrective-action plan
- interim action, screening or lot release procedure
- schedule for the introduction of the required changes.

Success criteria

Figure 8 shows the essential features of the information feedback process. The success of a ppm strategy of this type depends on

- short lines of communication
- fast action and reaction
- systematic and controlled information flow.

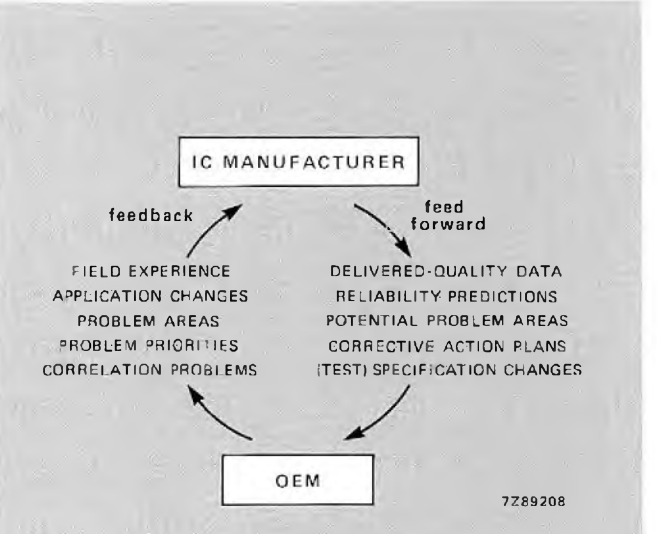


Fig.8 Basic information flow between manufacturer and OEM required for succesful implementation of a ppm system

PPM and CECC

Both ppm and CECC are systems concerned with the achievement of high quality, so it is important to understand the essential difference between them.

CECC is a system of quality *assurance:* it seeks to ensure that the quality of products delivered is equal to or better than the CECC-agreed level. For a given series of devices, this level is set by a set of test specifications that apply to, and are mandatory for, all CECC-approved suppliers. AQLs are set for conformance, and reject criteria for environmental and endurance testing. These are not targets and so the CECC system does not have a quality-improving function.

PPM is, however, a system of quality *improvement:* targets are set and the manufacturer is committed to improving actual product quality in cooperation with the OEM. PPM relates to the actual quality of the product as experienced by the OEM in his assembly line and afterwards. Both aspects of quality are monitored with a view to improvement. Although the ppm system assumes that the manufacturer operates a satisfactory quality-control system, approval of it is not required.

The circumstances of the modern electronics industry require continuous improvement in the quality of components and finished equipment of all types. Indeed, increased complexity and, thus, improved capability, is practicable only if the achievable quality of each circuit element can be improved in proportion.

AQL-based systems, such as CECC, are economic for the OEM, and CECC approval demonstrates confidence in the component-manufacturer's quality-control ability. However, such systems neither prove nor indicate the manufacturer's ability or intention to improve quality.

A sound system of Quality Assurance, as is demonstrated by CECC approval, is an essential background to good product quality. However, only a ppm system is capable of yielding the progressive improvement in quality that today's circumstances demand.

The new a.m. variable-capacitance diode BB112 is supplied in accurately matched sets of three for use in the long/medium wavebands of many types of radio. Since they are single diodes they allow the optimum circuit layout which cannot be achieved with diodes made in multiple units. Their voltage range (1 V to 9 V) makes them ideal for car radios.

Single variable-capacitance diode for a.m. car radios

Incorporation of features such as electronic station pre-selection and automatic search tuning in the a.m. section of multi-waveband car radios requires the use of low-voltage (<10 V) variable-capacitance diodes for tuning, and LW/MW band-switching diodes such as our BA423 (Ref.1). The variable-capacitance diodes must have a min/max capacitance ratio that enables them to tune the three resonant circuits normally used in the a.m. section of car radios (two r.f. circuits and the local-oscillator) to frequencies in the medium waveband (510 kHz to 1610 kHz) and long waveband (150 kHz to 300 kHz). Their voltage/capacitance characteristic curve and series resistance must be such that they don't cause undue distortion of the signal or damping of the tuned circuits. Accurate tracking of the tuned-circuits also demands that the voltage/capacitance characteristic curves of the diodes be closely matched. This can be achieved by manufacturing multiple diodes on the same crystal (e.g. the BB212 described in Ref.2), or individual diodes which are subsequently measured and supplied as matched sets. However, even when multiple diodes are on the same crystal, the voltage/capacitance characteristics of each diode must still be measured after manufacture and any crystals containing diodes which are not matched to within the required accuracy must be discarded. Obviously, this rejection of crystals incurs a cost penalty. Furthermore, variable-capacitance diodes manufactured with a common cathode connection restrict design flexibility because each diode cannot be positioned close to the tuned circuit of which it forms a part.

These considerations have led us to manufacture new single a.m. variable-capacitance diodes type BB112 using the recently developed controlled-growth profiled epitaxial process. After manufacture, these diodes are subjected to a unique computer-controlled measurement and selection procedure so that they can be supplied in sets of three with capacitance matched to within less than 3% over the tuning voltage range 1 V to 9 V. Other outstanding characteristics of the BB112, of particular importance in the a.m. section of a car radio are:

- the maximum required tuning voltage is less than 10 V
- the maximum capacitance of 440 pF to 540 pF and the max/min capacitance ratio of at least 18 allows tuning of the required frequency range
- the normally used part of the tuning voltage/capacitance characteristic shown in Fig.1 closely follows the law required to minimise non-linear distortion of signals applied to the tuned circuits. This is described in greater detail in Ref.1

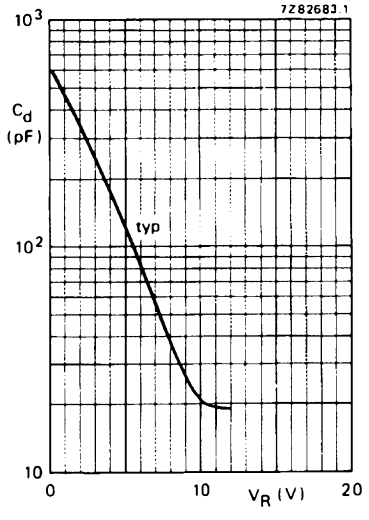


Fig.1 Typical capacitance as a function of tuning voltage for variable-capacitance diode BB112 (f = 1 MHz)

- the temperature coefficient of capacitance is only 0.05%/°C
- leakage current at the maximum tuning voltage (12 V) is less than 50 nA at 85 °C.
- series resistance of less than 1.5Ω when the tuning voltage is 1 V causes minimal damping of the tuned circuits

Even with such a high-performance variable-capacitance diode as the BB112, the following precautions, which are more fully discussed in Ref.2, must be taken when designing the a.m. section of a car radio with variable-capacitance diode tuning:

- the tuning voltage must be stabilised against temperature and supply voltage variations. A typical stability requirement is ±0.1% for a tuning stability of ±1 kHz in the medium waveband
- since non-linear distortion caused by the variable-capacitance tuning diodes increases with high signal levels and with low tuning voltage, some form of r.f. gain control must be applied to prevent strong aerial signals causing increased distortion and allowing the reception of spurious signals by shifting the tuned frequency
- to minimise non-linear distortion and radiation, the local oscillator signal should have a low level (about 150 mV) which remains constant throughout the tuning range of the radio. Such a signal is available from our integrated a.m. radio circuit TDA1072 (Ref.2, 3 and 4)
- parasitic capacitance due to other components and connections in parallel with the tuning diodes must be minimum
- the tuning voltage must be adequately decoupled at signal frequencies
- the smoothing resistors in series with the tuning voltage applied to the diodes must be correctly chosen with regard to leakage current and acceptable voltage drop.

A MW/LW SECTION FOR A VOLTAGE-TUNED CAR RADIO

Description

Figure 2 is a block diagram of a variable-capacitance diode tuned MW/LW section of a car radio. The required high sensitivity is obtained by using a preselector followed by two r.f. amplifiers, each with a variable-capacitance diode tuned bandpass filter and an asymmetric J-FET type BF410 (Ref.5). This type of transistor has been chosen because it has low feedback capacitance, low h.f. noise and its transfer characteristic approximates a square law over a much wider range of gate-source voltages than any other FET. It can therefore handle larger input signals without causing undue non-linear distortion or intermodulation.

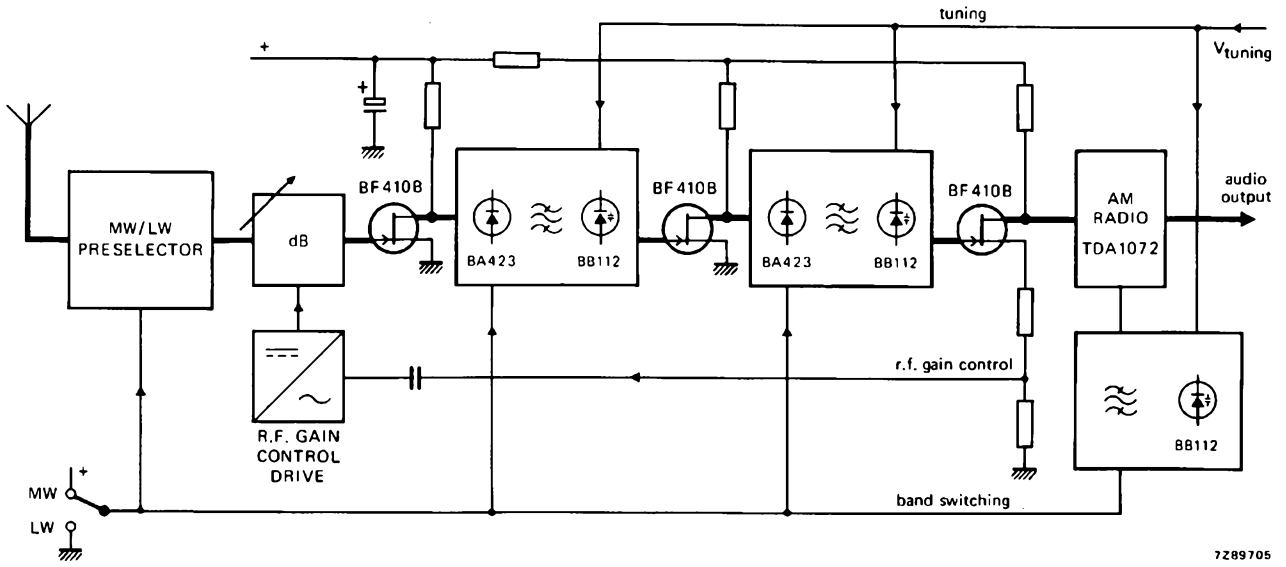


Fig.2 Block diagram of the a.m. section of a variable-capacitance diode tuned car radio

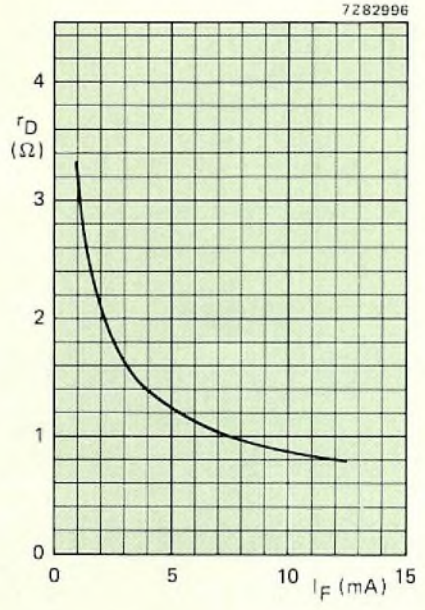


Fig.3 Typical resistance as a function of forward current for band-switching diode BA423 (f = 1 MHz, T_j = 25 °C)

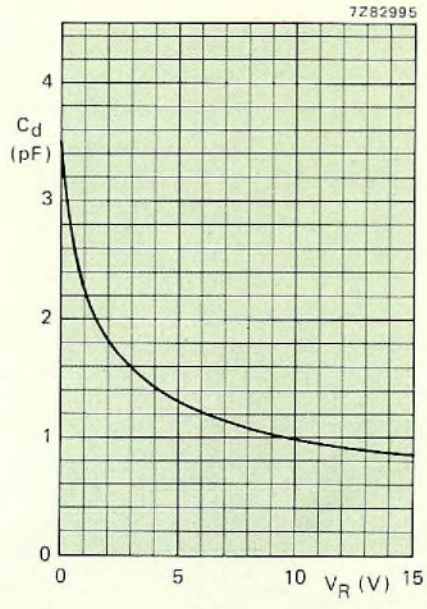


Fig.4 Typical capacitance as a function of reverse voltage for band-switching diode BA423 (f = 1 MHz, T_j = 25 °C)

Since the lowest tuning voltage is only about 1 V, the ability to handle the wide range of aerial input levels encountered in cars, without the tuning diodes causing distortion or detuning, is ensured by incorporating a d.c. controlled r.f. attenuator between the preselector and the r.f. amplifiers. The attenuator is controlled by the a.c. coupled output from a third BF410 FET which acts as a buffer between the r.f. amplifiers and an integrated a.m. radio circuit TDA1072. The a.c. output from the source of this third FET is converted into a signal level dependent d.c. control signal by the r.f. gain control drive block before it is applied, via an emitter-follower, to the r.f. attenuator. If required, the gain control threshold may be made adjustable. A third variable-capacitance diode tunes the local-oscillator resonant circuit connected to the TDA1072.

Waveband switching is achieved with simple d.c. change-over switching (mechanical or electronic) to control the d.c. bias applied to MW/LW band-switching diodes BA423 connected in the tuned circuits. This type of switching is difficult to implement with switching diodes other than the BA423 because they require a high current to reach the necessary low forward resistance (minimum damping of tuned circuits), and a high reverse voltage (compared with the car battery voltage) to achieve the low capacitance necessary to minimise detuning. Our switching diode BA423 solves the problems because, at 1 MHz, it requires a forward current of only 10 mA to reduce its forward resistance to less than 1.2Ω and, with a reverse voltage of only 3 V, its capacitance is less than 2.5 pF. The forward current/forward resistance and reverse voltage/capacitance characteristics of the BA423 are given in Fig.3 and Fig.4.

Performance

If the performance given on the next page is compared with that of the circuit on page 123 of Ref.2 which has a single-tuned r.f. stage, it is evident that, with the double tuned circuit, the signal to noise ratio is about the same, the i.f. suppression is increased by about 10 dB and the image suppression is increased by about 50 dB.

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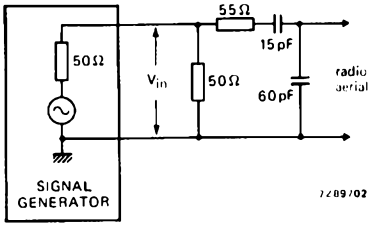
2. BAHNSEN, B. P., 'Voltage-controlled tuning of a.m. radios' Electronic Components and Applications, Vol. 2, No. 2, February 1980.
3. 'Integrated a.m. radio TDA1072' Technical note 148, March 1980, ordering code 9398 014 80011.
4. BAHNSEN, B.P. and GARSKAMP, A., 'Integrated circuits for car radios' Electronic Components and Applications, Vol. 3, No. 2, February 1981.
5. 'Asymmetric J-FET improves radio performance' Electronic Components and Applications, Vol. 2, No. 3, May 1980.

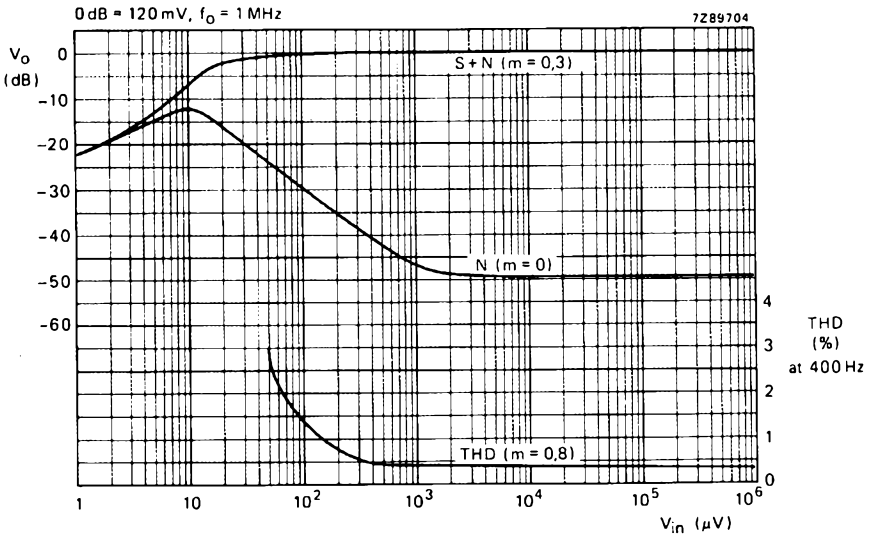
PERFORMANCE OF THE A.M. SECTION

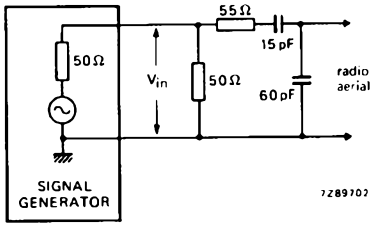
supply voltage range	10.5 to 15	V
long wave frequency range	150 to 300	kHz
medium wave frequency range	510 to 1610	kHz
a.g.c. range (V_{in}/3 V) for 10 dB variation of output	>100	dB
maximum r.f. signal handling capability (m = 0.8, THD < 1%)	>2	V
THD over most of the a.g.c. range (m = 0.8, f_{mod} = 400 Hz)	<1	%

tuned frequency f_0	160	200	250	600	1000	1500	kHz
aerial input voltage (V_{in}) for S+N/N = 26 dB (see Fig.5)	200	200	200	110	110	110	μV
i.f. suppression at f_0 (V_{in} = 100 μV)	>90	>80	>70	>60	>70	>80	dB
image rejection at f_0 (V_{in} = 100 μV)	>100	>100	>100	>100	>90	>80	dB
r.f. bandwidth (−3 dB) at f_0	10	12	15	10	15	20	kHz



(a) medium-wave operation





(b) long-wave operation

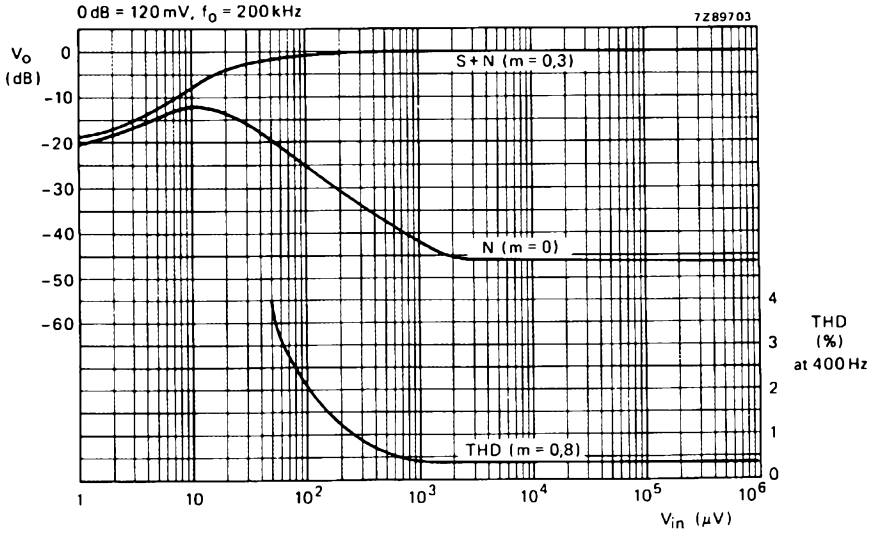


Fig.5 Performance of the a.m. section shown in Fig.2

Compactness, low cost, and compatibility with modern microwave integrated circuitry are principal features of the dielectric-resonator oscillator (DRO). In applications such as satellite tv, radar beacons, and digital communications, the DRO is a real alternative to bulkier, more expensive cavity-stabilised oscillators. This article describes the DRO and tells how to use it as a stable microwave signal source.

Dielectric-resonator oscillators – a new microwave signal source

B. J. VAN DER HEIJDEN

Dielectric-resonator oscillators (DROs) are microwave oscillators stabilised by a ceramic resonator. In many applications, DROs provide an attractive alternative to conventional crystal oscillators and cavity stabilised oscillators.

DROs are small, light and inexpensive, at least compared with cavity stabilised oscillators which are often bulky and costly to produce. And unlike crystal oscillators, they don't need wide-band frequency multipliers to operate at microwave frequencies. Moreover, they are highly compatible with modern microwave integrated circuitry.

They do have a somewhat restricted tuning range, and a higher f.m. noise than the cavity stabilised oscillator, but for a lot of applications, for example in digital telecommunications, satellite TV, radar beacons and doppler transponders, this is of minor importance.

At present, practical DROs cover the microwave region from below 4 GHz to about 16 GHz; with improvements in Q-value, even higher operating frequencies should be attainable in the future.

This article describes the DRO, and shows how this new oscillator can be used to provide a stable, low-cost microwave signal source.

DRO OPERATION

In principle, the DRO operates in a similar way to the cavity stabilised oscillator. Here a signal source, formed by an active semiconductor device such as a negative resistance Gunn diode or IMPATT diode, is coupled, via transmission line, to a high-Q cavity resonator. A major characteristic of this oscillator is its exceptional stability, due principally to the strong off-resonance decoupling between the diode circuit and the output load.

In the DRO, a ceramic disc resonator – e.g. of sintered barium titanate – replaces the cavity resonator. Figure 1 shows schematically three DRO circuit configurations suitable for operating with a Gunn or IMPATT diode, a silicon bipolar transistor or a GaAs FET.

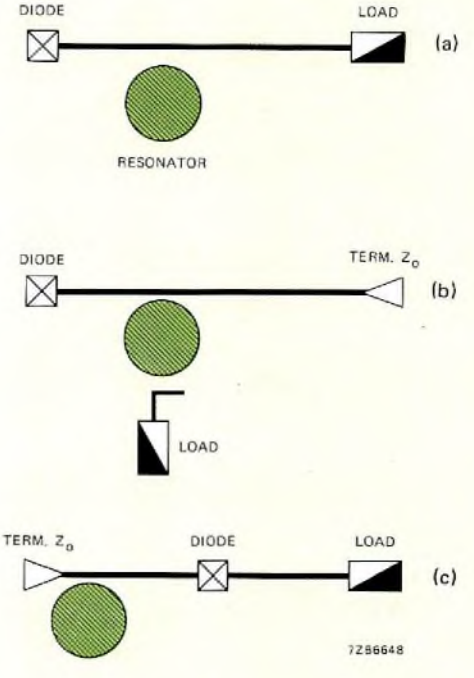
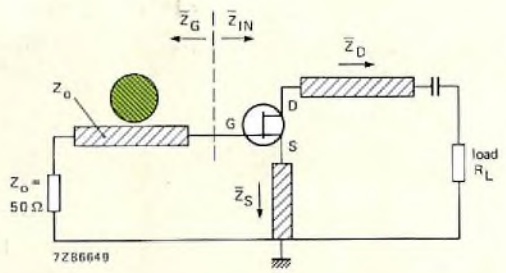


Fig.1 Circuit configurations for a negative resistance oscillator, stabilised by a dielectric resonator: (a) reaction type DRO, high loaded Q-value Q_L, suffers from parasitics and mode jumps; (b) transmission type DRO, relatively high Q_L, free of parasitics and mode jumps; (c) reflection type DRO, relatively low Q_L, free of parasitics

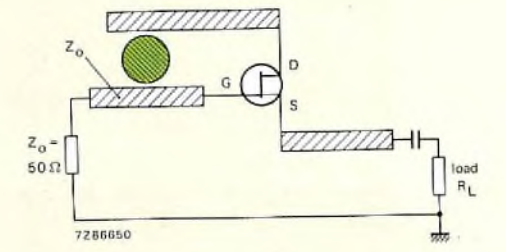
The circuit of Fig.1(a) has been favoured by some users because of its very high loaded Q-value. It does, however, suffer severely from parasitics and mode jumps, and has now been almost entirely replaced by the circuits of Fig.1(b) and 1(c). The first of these – known as the transmission type DRO – is the direct counterpart of the cavity-stabilised oscillator circuit (Kurokowa circuit). The active element, a Gunn diode for example, is mounted at the end of a transmission line terminated with its characteristic impedance, and inductively coupled to a ceramic resonator. Microwave power is extracted from the resonator field by a coupling loop or probe. The circuit exhibits high loaded Q-values and an absence of mode jumping and parasitics.

Oscillators of the type shown in Fig. 1(c) – known as reflection type DROs – are also free of mode jumping and parasitics, but their loaded Q-values are generally lower than those of the transmission type DRO. They are, however, more efficient than the transmission type DRO, and in some applications their use is preferred.

Figure 2(a) shows a reflection type FET DRO with the dielectric resonator coupled to the gate of the FET, and the microwave power tapped from the drain. The system is based on 50 Ω transmission line. With proper biasing (not shown) and suitable impedances in the drain and source circuits, the input resistance to the gate terminal will become negative, and the conditions for oscillation at the resonant frequency of the resonator can be fulfilled. At resonance, the impedance presented in the coupling plane consists of a high resistance in series with 50 Ω, and at other frequencies the gate sees a matched load, eliminating mode jumps and spurious oscillations. Another type of FET DRO is shown in Fig.2(b). Here oscillation is produced by an external feedback loop (via the dielectric resonator) between drain and gate transmission lines.



(a)



(b)

Fig.2 (a) Reflection type FET oscillator stabilised by a dielectric resonator coupled to the gate circuit; (b) FET oscillator using feedback (via the dielectric resonator) between drain and gate to produce oscillation

THE DIELECTRIC RESONATOR

With a dielectric constant of around 40, barium titanate resonators are much smaller than corresponding cavity resonators. Barium titanate has other important properties too, notably:

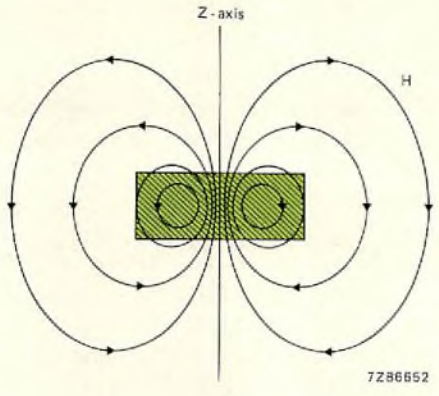
- very high temperature-stability, i.e. relatively small – *but positive* – resonant-frequency temperature-coefficient τ_{f0} (averaging around 1.5×10^{-6}/K for a 10 GHz resonator in the temperature range –20 °C to +100 °C). Note: as will become apparent later, a positive temperature-coefficient is needed to compensate thermal drift in the oscillation frequency of the circuit containing the active element.
- low dielectric loss, which means that the resonator will have a high unloaded Q-value (of around 8000 at 4 GHz, and 3500 at 10 GHz).

The high temperature stability of barium titanate is fortuitous, and is due to the effect of thermal expansion on resonant frequency being balanced by an almost equal and opposite effect produced by temperature dependent variations in the dielectric constant.

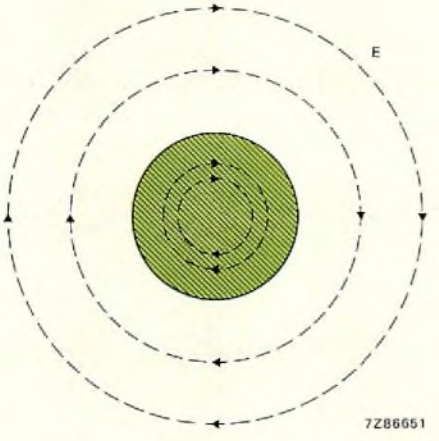
DESIGN CONSIDERATIONS

The ceramic disc should preferably operate in its lowest order cylindrical $TE_{01\delta}$ mode, the electromagnetic field pattern of which is shown in Fig.3. The high dielectric constant of barium titanate causes most of the electromagnetic field energy (about 80%) to be confined within the disc. Resonance in the disc is then produced by reflections at the dielectric/air interface.

The electromagnetic field outside the disc allows easy coupling to external circuitry (in contrast to the cavity resonator in which the field lies entirely within the cavity). Moreover, the degree of coupling can easily be varied by varying the distance between disc and circuitry. Figure 4 shows examples of this coupling, (a) to a coaxial line via an aperture in its outer conductor, and (b) to a microstrip transmission line.



(a)

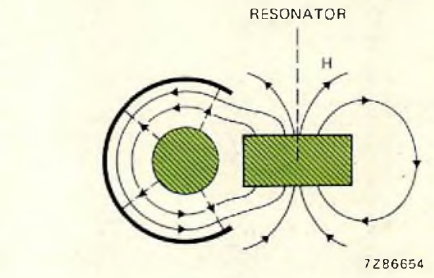


(b)

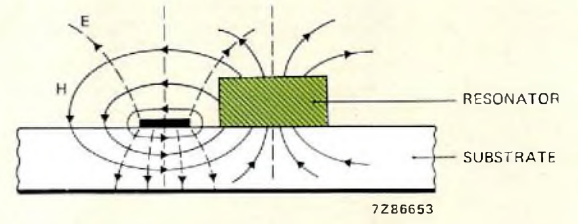
Fig.3 (a) Magnetic field pattern and (b) electric field inside and outside a cylindrical dielectric resonator operating in the $TE_{01\delta}$ mode

To minimise radiation losses, which would result in a very low effective Q-value, the ceramic disc is mounted on quartz rings inside a metal enclosure. These rings maintain the spacing between the disc and enclosure wall, essential for optimum Q-value, temperature stability and mode separation. They also secure the resonator in the optimum position for coupling to coaxial or microstrip transmission line.

With most of the field energy confined within the dielectric, the resonant frequency of the disc (and therefore the oscillator output frequency) is much less sensitive to ambient humidity variations than is that of the cavity resonator. Nevertheless, the metal enclosure is sealed to minimise external influences.



(a)



(b)

Fig.4 Inductive coupling of a $TE_{01\delta}$ mode disc resonator: (a) to coaxial line through a hole in the outer conductor, and (b) to a microstrip transmission line

FREQUENCY AND POWER LIMITATIONS

Practical frequency and power limitations of a DRO are set by the active device and the circuit used, and to a lesser extent, by the resonator. DROs can, in principle, operate at frequencies between 1 GHz and 18 GHz without frequency multiplication, and the envisaged application is usually the deciding factor in selecting the active device.

For the highest frequencies, Gunn diodes are currently the most suitable. But the efficiency of Gun-diodes rarely exceeds 4%, whereas GaAs FETs and bipolar transistors commonly have efficiencies up to 20%. Nevertheless, highly stable Gunn-diode DROs delivering several hundred milliwatts are not uncommon.

The upper frequency limit of the oscillator is set by the minimum unloaded Q-value consistent with high stability and low f.m. noise. Below about 8 GHz, dielectric resonators and cavity resonators have roughly comparable Q-values, so losses are about the same. But above 8 GHz, the Q-value of the dielectric resonator falls off more rapidly than that of the cavity resonator, resulting in higher losses and lower stability. With currently available dielectric materials, DROs are restricted to a practical upper limit of about 16 GHz.

A lower frequency limit for the DRO is set by the size of the resonator. Barium titanate DROs capable of operating effectively below 1 GHz would need resonators greater than 5 cm diameter (operating in the $TE_{01\delta}$ mode), thus forfeiting the principal advantage of the DRO (i.e. its compactness). Future development of suitable high dielectric materials, however, will doubtless extend this lower limit.

TEMPERATURE STABILITY

An unstabilised oscillator will usually suffer relatively large frequency drifts with changes in ambient temperature. A temperature coefficient of frequency τ_{fu} of around -100×10^{-6}/K is not unusual, and is due principally to capacitance drifts in the active device. With frequency stabilisation using a resonator, this will be reduced by a factor S – called the *stabilisation factor*. So the overall temperature coefficient of frequency of the stabilised oscillator is

$$\tau_f = \tau_{fu}/S + \tau_{fo}$$

where τ_{fo} is the resonant-frequency temperature coefficient of the dielectric, i.e. 1.5×10^{-6}/K for barium titanate. S is a function of circuit efficiency, and of the unloaded Q-values of the resonator and unstabilised oscillator. As a general rule, S increases with increasing resonator Q-value, and falls with increasing circuit efficiency, so the design of a DRO is inevitably a compromise between these two quantities.

In the transmission type circuit of Fig.1(b), with resonator and unstabilised oscillator Q-values of say 2500 and 50 respectively, and a circuit efficiency of about 40%, you could expect a stabilisation factor of around 25. So the average value of τ_f would be $(-100/25 + 1.5) \times 10^{-6}$/K, i.e. -2.5×10^{-6}/K.

It's clear from this that the resonator must have a positive temperature coefficient to compensate the negative coefficient of the active element. In the example given here, a somewhat larger τ_{fo} is in fact needed for complete temperature compensation.

Figures 5 and 6 show, respectively, the temperature dependent frequency/power variation of a Gunn DRO (JS1200) and a microstrip-based FET DRO (JS1300). The latter is a particularly stable device with a temperature coefficient τ_f of about -1×10^{-6}/K between –20 °C and +60 °C.

For even better temperature stability, DROs can be supplied with a temperature dependent voltage regulator. This could take the form of an NTC thermistor (mounted in the heatsink) that automatically reduces the diode voltage with increasing temperature. Figure 7 shows how the inclusion of an NTC thermistor improves the temperature stability of a high-power Gunn DRO.

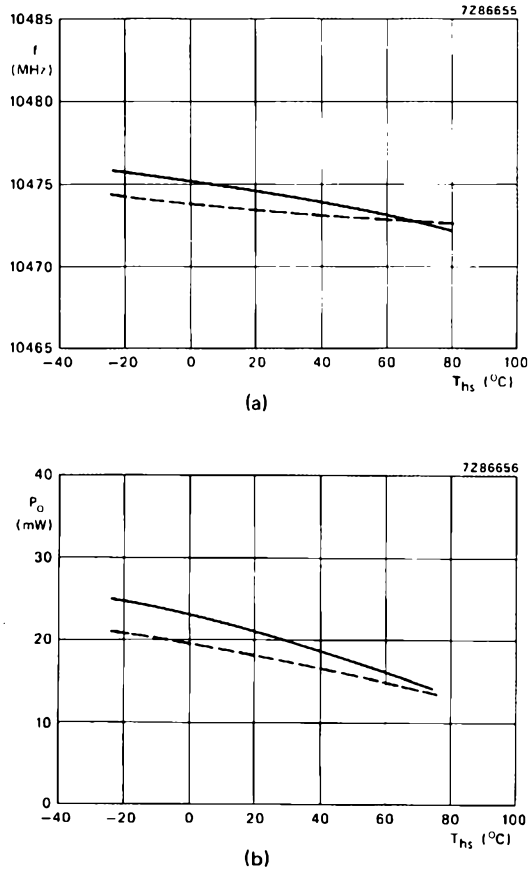


Fig.5 (a) Frequency f and (b) output power P_o of a Gunn DRO (JS1200), both as a function of heatsink temperature T_{hs}. Conditions: zero detuning, bias voltages –8 V (solid line), –7 V (broken line)

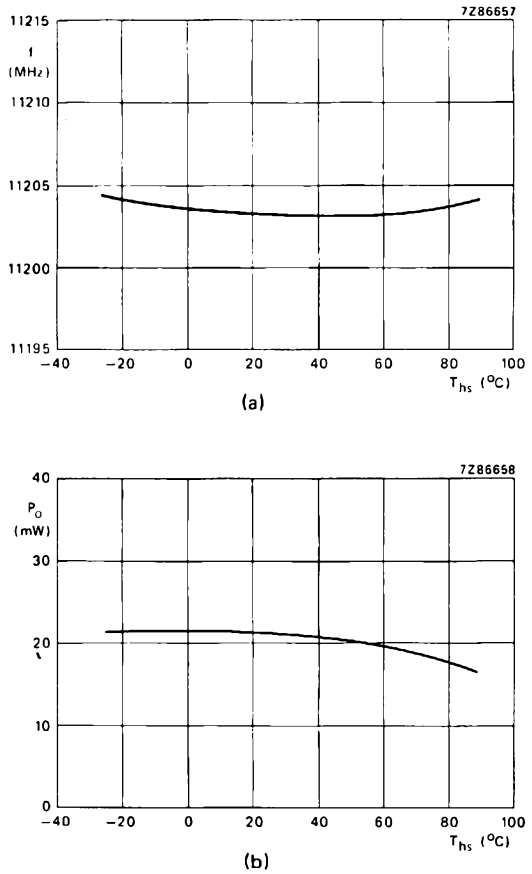
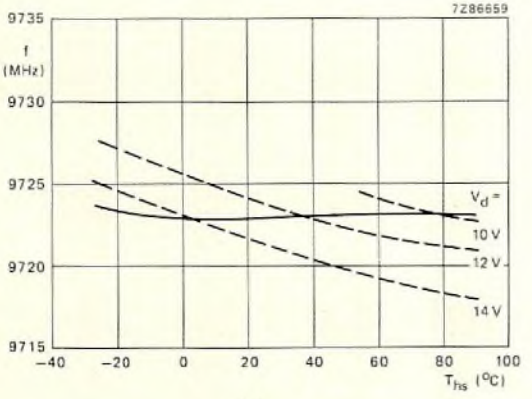
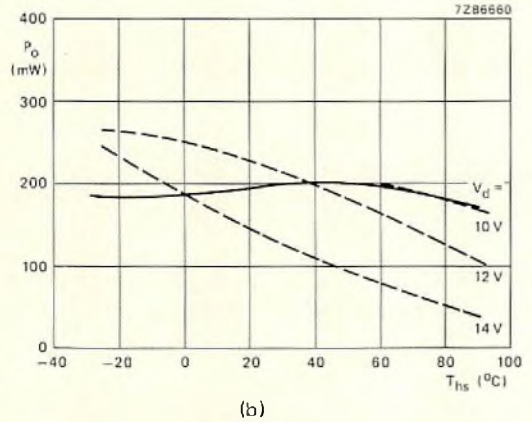


Fig.6 (a) Frequency f and (b) output power P_o of a FET DRO (JS1300), both as a function of heatsink temperature T_{hs}. Conditions: zero detuning, I_{DS} = 47 mA



(a)



(b)

Fig.7 (a) Frequency f and (b) output power P_o of a high-power Gunn DRO with a temperature dependent voltage regulator, both as a function of heatsink temperature T_{hs}. The voltage regulator dramatically improves temperature stability, at the expense of higher d.c. supply voltage (18 V compared with 12 V for the basic DRO). The broken lines give the performance at constant bias voltage

TUNING

A DRO can be tuned to a limited extent by perturbing the resonator's magnetic field. This can be done by varying the air gap between the ceramic disc and the metal enclosure, with, for example, a movable metal plate or screw coaxial with the ceramic disc.

However, DROs are designed for optimum mode separation at a specific frequency. A large degree of detuning may reduce this separation to an unacceptable degree, and may even cause modes to coincide. So to minimise the chance of mode jumping, and to maintain acceptably high Q-values, the resonant frequency should be kept to within 1% of specification. Outside this range the DRO's performance will deteriorate rapidly, with a greater chance of spurious responses within the operating band, poorer coupling with associated microwave circuitry and higher temperature coefficient of frequency τ_{fo}. This last effect is rather critical and should always be borne in mind when tuning a DRO by any substantial amount. For example, a 6% detuning may result in a tenfold increase in τ_f.

Figure 8 shows a typical tuning curve of a Gunn DRO operating at around 10 GHz, and Fig.9 shows how the external Q-value of a typical DRO is influenced by tuning.

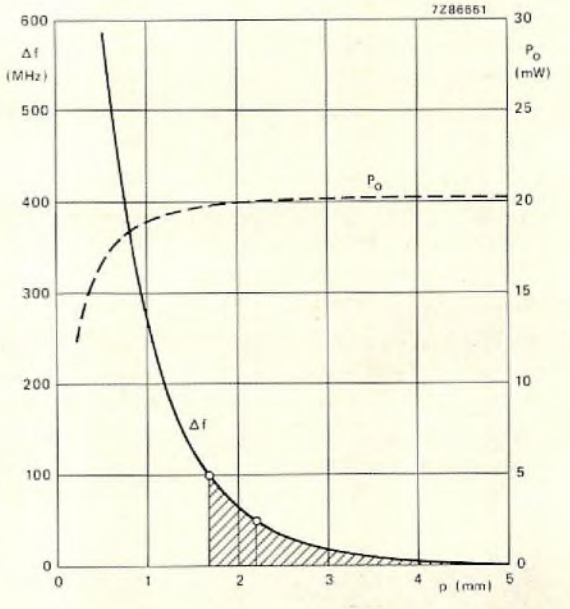


Fig.8 Tuning Δf (solid line) and output-power P_o (broken line) of a typical DRO, both as a function of the airgap P between tuning screw and resonator. Operating frequency 10.475 GHz. For very small air-gaps, thermal expansion of the housing becomes important, resulting in large variations in τ_{fo}. This, plus the degraded Q and reduced mode separation that inevitably accompanies tuning away from specification, limits the tuning range to about 1% (shaded region)

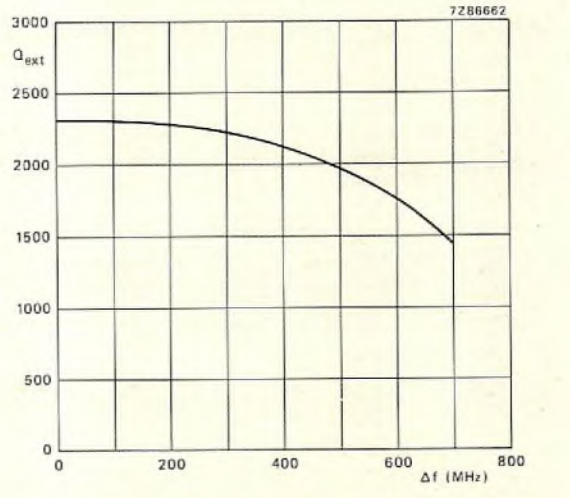


Fig.9 External Q-value Q_{ext} (determined from injection locking measurements) as a function of tuning Δf. Operating frequency 10.475 GHz, output power 20 mW at Δf = 0

NOISE

FM noise in an oscillator originates mainly from the active device, FET oscillators being generally noisier than Gunn oscillators. In a DRO, however, the f.m. noise is reduced by the factor S (stabilisation factor). Since S can be as high as 30 (at X-band frequencies), the f.m. noise of a DRO may therefore be as much as 30 dB down on that of an unstabilised oscillator.

Figure 10 shows how the SSB f.m. noise-power (in a 1 Hz bandwith) of a typical Gunn DRO varies with distance f_m from the carrier frequency (10.475 GHz). The SSB noise can also be expressed in terms of the r.m.s. frequency deviation Δf_{rms} defined in a 1 Hz band at f_m. For example, an f.m. noise power of −125 dBc/Hz at f_m = 100 kHz corresponds (from Fig.10) to a Δf_{rms} of 0.1 Hz/√Hz. The a.m. noise level measured under the same conditions is about −148 dBc/Hz at f_m = 100 Hz.

Comparable FET DROs usually exhibit f.m. noise figures between 10 and 20 dB worse than those given above, and an a.m. noise of about −144 dB/Hz at 100 kHz. These figures are, however, strongly affected by the gate bias voltage and by circuit design.

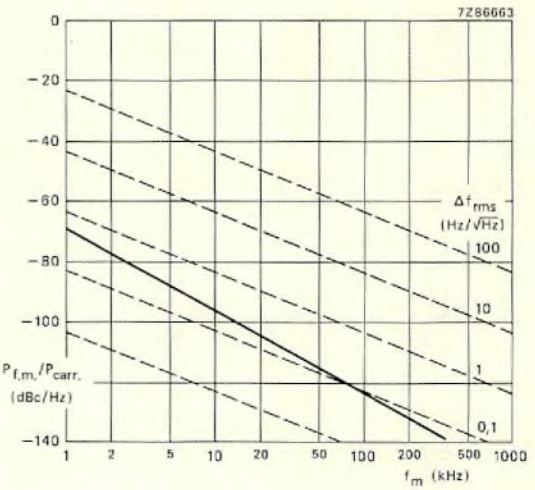


Fig.10 Relative SSB noise power $P_{f.m.}/P_{carrier}$ of a typical Gunn DRO (JS1200) measured in a 1 Hz bandwidth as a function of the distance f_m from the carrier. Bias voltage −8 V, carrier frequency 10.475 GHz, output power 20 mW. The SSB noise can also be expressed in terms of the r.m.s. frequency deviation Δf_{rms} defined in a 1 Hz band at f_m, and given by $\Delta f_{rms} = f_m\sqrt{[2\,P_{f.m.}/P_{carrier}]}$. Broken lines represent contours of constant Δf_{rms}

FREQUENCY PULLING AND OUTPUT ISOLATION

Frequency pulling of an oscillator is a measure of the influence the load has on the output frequency. It's defined as the peak-to-peak frequency shift of the output signal that occurs as the phase of the load's reflection coefficient changes through 360°.

The frequency pulling suffered by a DRO (and for that matter by a cavity stabilised oscillator) is significantly less than that suffered by an unstabilised oscillator. It's given approximately by

$$\Delta f_p = \tfrac{1}{2}(s - 1/s)\, f_0/Q_{ext}$$

in which s is the v.s.w.r. and Q_{ext} is the external Q-value of the oscillator. Very often frequency pulling is defined for a v.s.w.r. of 1.5.

For a standard DRO operating at 10.475 GHz, with 20 mW output power, a v.s.w.r. of 1.5 and a Q_{ext} of 2200, Δf_p is about 2.3 MHz – significantly less than the 100 MHz that could be expected of an unstabilised oscillator working under similar conditions.

For applications where appreciable phase or amplitude changes in load reflection-coefficient may occur, it may be necessary to insert an isolator between oscillator and load. With, say, 40 dB isolation between the oscillator and load, the frequency pulling (for a v.s.w.r. of 1.5) can fall as low as 23 kHz. This is illustrated in Fig.11, which shows how frequency pulling of a Gunn DRO (JS1200) varies with load isolation.

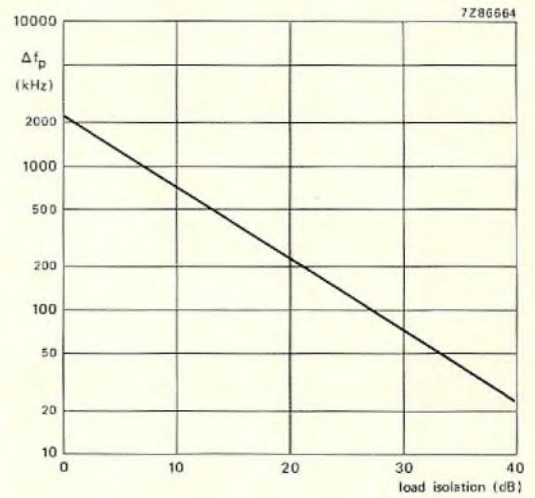


Fig.11 Frequency pulling Δf_p of a Gunn DRO (JS1200) as a function of load isolation. Constant load v.s.w.r. = 1.5, 20 mW output power, operating frequency 10.475 GHz

First-in/first-out buffers are often essential for interfacing computer peripherals and other applications. A new LSI controller chip now makes it possible to build large yet economical FIFO buffers using standard RAM chips.

Controller IC for FIFO buffers

JEFF SELTZER

More and more digital systems require large first-in/first-out (FIFO) buffer memories to interface asynchronous sub-systems. Now, with the introduction of the Signetics 8X60, large FIFO buffers can be built from high-density RAM chips to form compact and economical systems. The new LSI chip, known as a FIFO RAM Controller (FRC), can be used with RAM chips to produce FIFO registers with depths of up to 4096 words (where the words can be of any desired length).

In many applications – examples include peripheral interfacing, data communications and data acquisition – there has been an urgent need for large FIFO buffers (see "Where FIFO Buffer Storage Is Needed"). But, until the introduction of the new controller chip, all the available techniques for building large FIFOs resulted in bulky and expensive systems. For example, FIFO memory chips have been available for several years, but with very limited capacity – typically 64 x 4 bits. Most FIFO applications require a large number of IC packages to produce the required buffering capability. However, in applications where only a limited amount of buffering is required, LSI FIFO chips may yield the most compact and cost-effective design.

Fitting the FIFO to the task

Before examining the FIFO RAM controller in detail, first look at some of the alternatives. This will help you to select the best method for a specific application, and will highlight some of the advantages of the new approach. Of course, regardless of the method employed, the application determines the required buffer size. The memory itself may be built from standard RAMs or from available FIFO memory chips.

For buffer memories in general, though not necessarily for FIFO buffers, semiconductor RAMs are commonly used because they are inexpensive and readily available. The one chosen depends on the buffer size and speed requirements. In most buffer applications, high speed is required, and static RAMs are a popular choice because they tend to be faster and are more easily interfaced than dynamic RAMs. However, even with static RAMs, additional logic is required to address the buffer from both system interfaces. This logic must be capable of generating and keeping track of addresses in the RAM where data are stored. It must also control read and write cycles and provide status signals to indicate buffer availability.

An advantage of RAMs as buffers, of course, is that they allow random access. Data in the RAM can be directly accessed, and new data can be directly written into any RAM location. A disadvantage, however, is the need for a sophisticated buffer controller, or for substantial logic in the buffered sub-systems to generate addresses and interpret control signals. To avoid undue cost and complexity, RAM-based buffer designs usually must be operated under the control of the systems that are being interfaced. This, in turn, means that they often must be completely filled up by one sub-system before being completely emptied by the other sub-system. The net result of this constraint is that, if large amounts of data are flowing through the buffer, there will be inherent delays that detract from overall system performance. In fact, where real-time response is required, RAM buffering may prove impractical.

Fortunately, RAM buffering isn't essential in most applications, for direct access to the buffer is rarely needed. Most systems require sequential data transfer that can be handled by a straightforward FIFO buffer, without the need for complex address-control circuitry in either sub-system. With FIFO organisation of the buffer memory,

information can be read by the receiving sub-system immediately after it has left the transmitting sub-system. The only restrictions on the speed of data transfer are the relative speeds of the sub-systems and the capacity of the buffer.

For applications where random access to the buffer is not required, the most common technique is to use one of several FIFO memory chips that are currently available. However, these have limited capacity and are available in only a few specific depth and word-width configurations. They do have separate data and control lines for input and output operations, which facilitates their use by two independent sub-systems. Two asynchronous handshake lines allow read/write control, as shown in Fig.1 for a typical LSI FIFO chip. Usually, these circuits can sustain quite high I/O clocking rates of about 10 MHz.

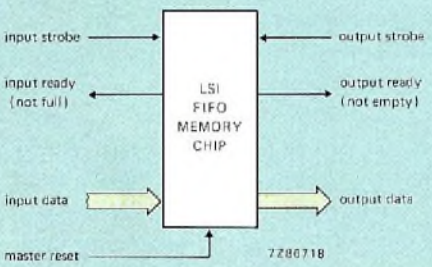


Fig.1 For a typical FIFO memory chip, an input strobe enters data into the stack, and another strobe later removes the data. Status lines can be used to prevent entry of data if the stack is full or removal if it is empty

Internally, a FIFO memory circuit consists of a series of storage registers daisy-chained to form a stack as shown in Fig.2. A flip-flop associated with each register indicates whether that register contains valid data or is empty. Data presented to the FIFO circuit enter the first register and propagate through the stack. Propagation continues until the signal either encounters a full register or reaches the end of the stack. New data can be written into the buffer as soon as the previous entry has been copied forward from the first register. When data are read from the last register, data in all the preceding registers are copied forward by one location. The read operation can be repeated as soon as data in the last register have been replaced.

Construction of a large FIFO memory from FIFO chips, using a configuration such as that shown in Fig.3, presents two significant problems. Firstly, the chips have only a small capacity. Therefore a large number of chips must be cascaded to achieve depth and/or paralleled to achieve width. Secondly, there is a 'fall-through' delay – the time required for a piece of data to propagate from the first register in the FIFO to the last. When FIFO devices are used to build a large buffer, the fall-through time increases as the stack becomes deeper. For large memories the problem becomes quite significant.

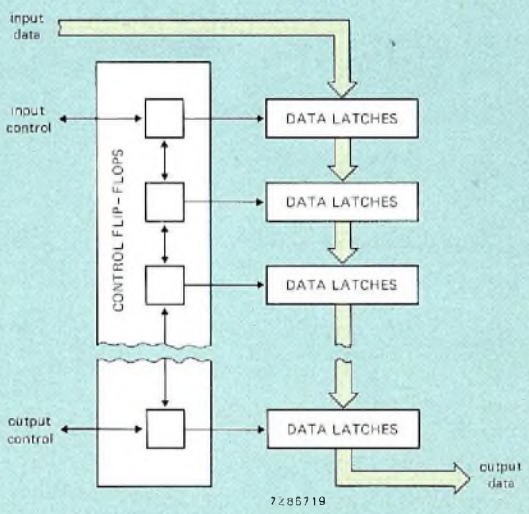


Fig.2 In a FIFO circuit, data are stored in a series of internal registers. Control flip-flops – one for each register – keep track of how many stack locations are in use. Data in a register are propagated forward whenever the next register is empty

RAMs provide an alternative

Because of the problems that occur when FIFO chips are used to build large buffer memories, alternatives must be considered. Most of the alternatives employ standard semiconductor RAMs to provide the data storage. Then, data can be stored in sequential locations in the RAM, and the address lines can be controlled to achieve the desired FIFO effect. Since the RAM controller can directly access any location, this approach eliminates the fall-through problem.

As mentioned earlier, unless the RAMs have dedicated control logic to achieve FIFO operation, the interfaced sub-systems will have to provide the control functions – with a consequent loss in overall system performance. There are several ways to implement the FIFO controller. Sometimes, the function can be conveniently implemented in software. Since digital systems often use microprocessors, the software approach can minimise the hardware overhead.

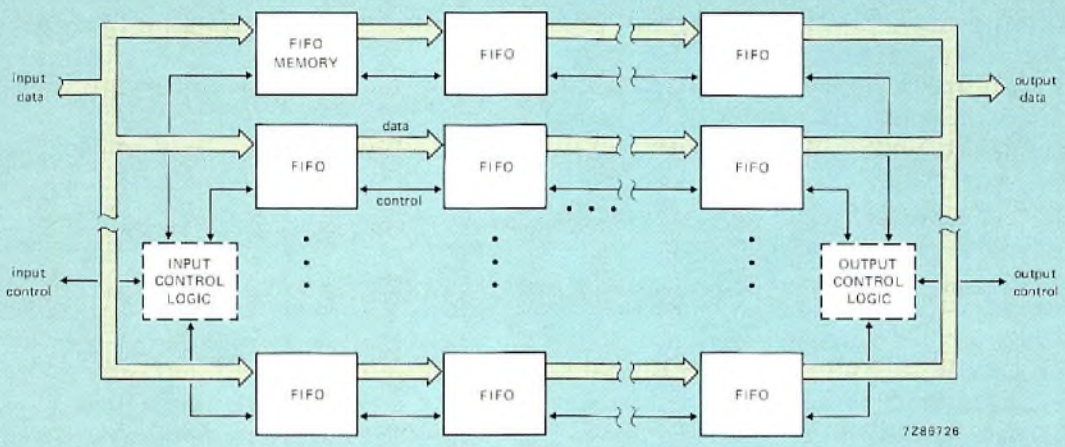


Fig.3 To build a large FIFO buffer, several FIFO memory chips can be cascaded. The depth of the buffer can be increased by connecting more chips in a chain; width can be expanded by connecting chains in parallel

WHERE FIFO BUFFER STORAGE IS NEEDED

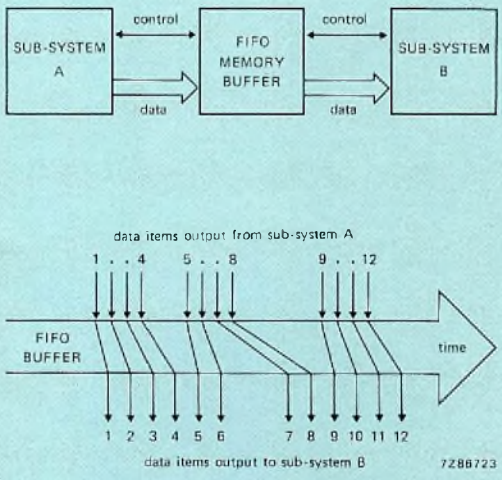
Wherever two digital sub-systems operate asynchronously, yet must communicate, a first-in/first-out buffer memory may be required. As shown in the diagram, a FIFO buffer can be used to interface two asynchronous sub-systems, A and B. Instead of being transferred directly from sub-system A to sub-system B, data are first accumulated in a FIFO buffer from which they are read into sub-system B at a different speed, but in the same sequence.

The buffer used must be sufficiently large to hold an entire block of data from the first sub-system (e.g. a complete sector from a disk). Though FIFO memory chips are available, they tend to have limited storage capability (typically 64 X 4 bits). The 8X60 controller chip meets the need for increased buffer capacity by allowing registers with depths of up to 4096 words to be built from high-density RAM chips.

There are many situations in which the speed of one or more sub-systems cannot be controlled by the system designer and where the data rate required by one of the sub-systems exceeds the capacity of the other. For example, high-speed peripherals must often be interfaced to computers that have limited channel or memory speed. The data rate of the peripheral may be fixed by mechanical characteristics (such as the rotation speed and recording density of a disk), while the I/O speed of the computer may be limited by memory speed. This type of situation could become more prevalent in the future as transfer rates of peripherals increase due to technological advances.

Another application where FIFO buffers can prove useful is in data-acquisition systems that must monitor and respond to a large number of real-time events. The events may occur at any time, including the period during which the processor is retrieving previously stored data. A FIFO buffer can store the events as they occur and present the data to the computer when it can handle the processing.

Data-communications systems often require buffering. In distributed communication networks, efficient use of the communication channel is important. Stations in the network must be capable of receiving or transmitting messages as soon as the communication channel becomes available. Use of FIFO buffers for interfacing allows efficient use of the communication channel even during periods when a station's processor is busy. In other data-communications systems, FIFO buffers can optimise use of the channel and processor by allowing messages or sets of messages to be stored and assembled for subsequent transmission.



The software solution to the FIFO-control problem is quite straightforward. As shown in Fig.4,. two address indices can act as pointers for the next read and write locations in the RAM space dedicated to FIFO buffering. The normal I/O ports of the microprocessor provide access for data to be written into and read from RAM. A software routine increments the associated pointers when a read or write operation is performed – resulting in circular addressing of the data storage in the buffer memory. Comparison of the address pointers determines the full or empty status of the buffer.

While this technique can often be used to manage a FIFO buffer when a microprocessor is present, it is unacceptable for many applications. The slow execution of programmed I/O can result in inadequate performance. Also, the additional burden on the microprocessor can detract from other processing functions, and outweigh the advantages of the FIFO. These problems can be avoided with a hardware implementation of the RAM controller.

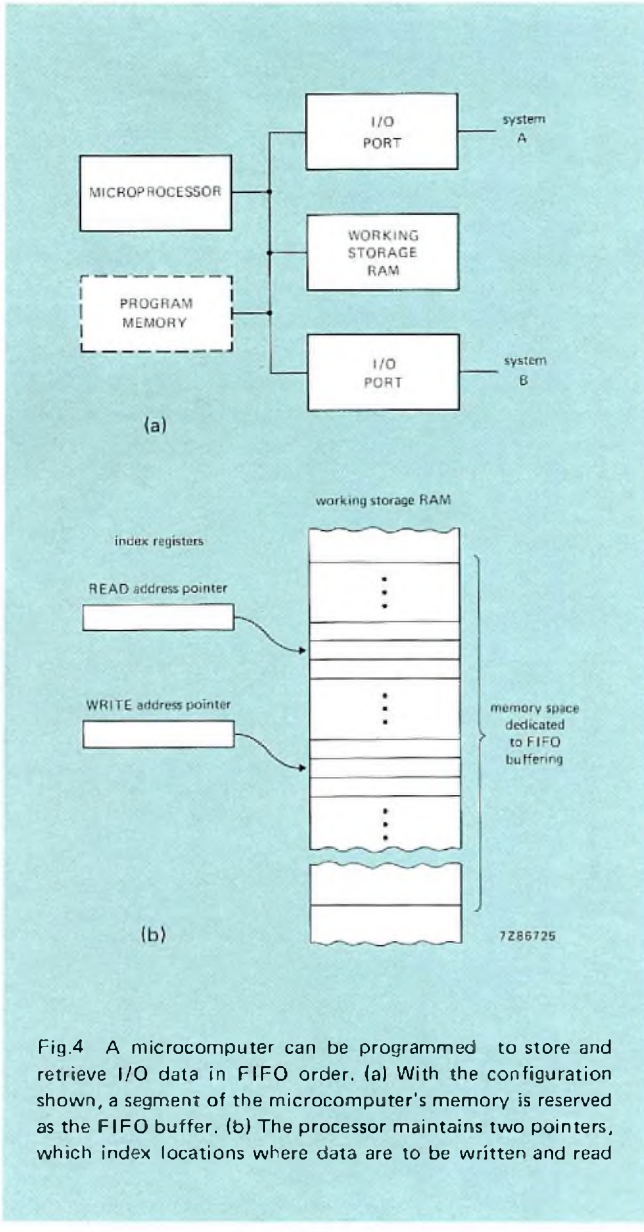


Fig.4 A microcomputer can be programmed to store and retrieve I/O data in FIFO order. (a) With the configuration shown, a segment of the microcomputer's memory is reserved as the FIFO buffer. (b) The processor maintains two pointers, which index locations where data are to be written and read

A hardware controller for RAMs

The hardware controller shown in Fig.5 can be built with about 16 logic ICs to perform a function similar to the software version. This controller generates 12-bit address pointers and therefore can address up to 4K words of RAM. The word width is determined solely by the number of RAMs connected in parallel. The control logic can be expanded to support deeper buffers by adding more counter stages.

The operation of the circuit is fairly simple. When a write cycle is requested, the multiplexer selects the current contents of the write address counter to access the RAM. Write enable to the RAM is activated once the address has stabilised. When the cycle has concluded and the request has been removed, the write address counter and the stack status counter are incremented. Similarly, a read cycle proceeds using the read address counter, except that write enable is not activated and the stack status counter is decremented on completion. When the stack status counter contains all zeros, it indicates an empty or full condition depending on the last operation performed. Since the storage devices are RAMs and can be accessed only one location at a time, an arbitration circuit is included. This arbitrates between read and write requests, should they occur concurrently. Once a read or write cycle has begun, it continues until the corresponding request signal is removed.

A design such as that of Fig.5 could easily achieve a data rate exceeding 5 MHz, depending on the RAMs employed. But, because the control logic requires about 16 chips, there is no worthwhile saving compared with an array of FIFO memory chips until the buffer size exceeds about 4K bits. However, use of an LSI circuit as the hardware controller drastically reduces the package count and the associated costs of development, manufacture, test, and support.

An LSI circuit for FIFO control

The 8X60 LSI circuit performs all of the functions of RAM control to form a FIFO buffer. The chip is fabricated in bipolar TTL and ISL (injected Schottky logic) to provide high-speed and low-power operation. A buffer memory built with the 8X60 and RAM chips competes with arrays of FIFO memory chips for buffer sizes as small as 512 bits (see Fig.6). Readily available 4K-bit static RAM chips offer high speed and economise on board space for larger capacity buffers.

The 8X60 provides a unique combination of features. It can control buffers with depths of up to 4096 words and with any width. The width is determined by the type and quantity of RAM devices used. Data rates achievable with

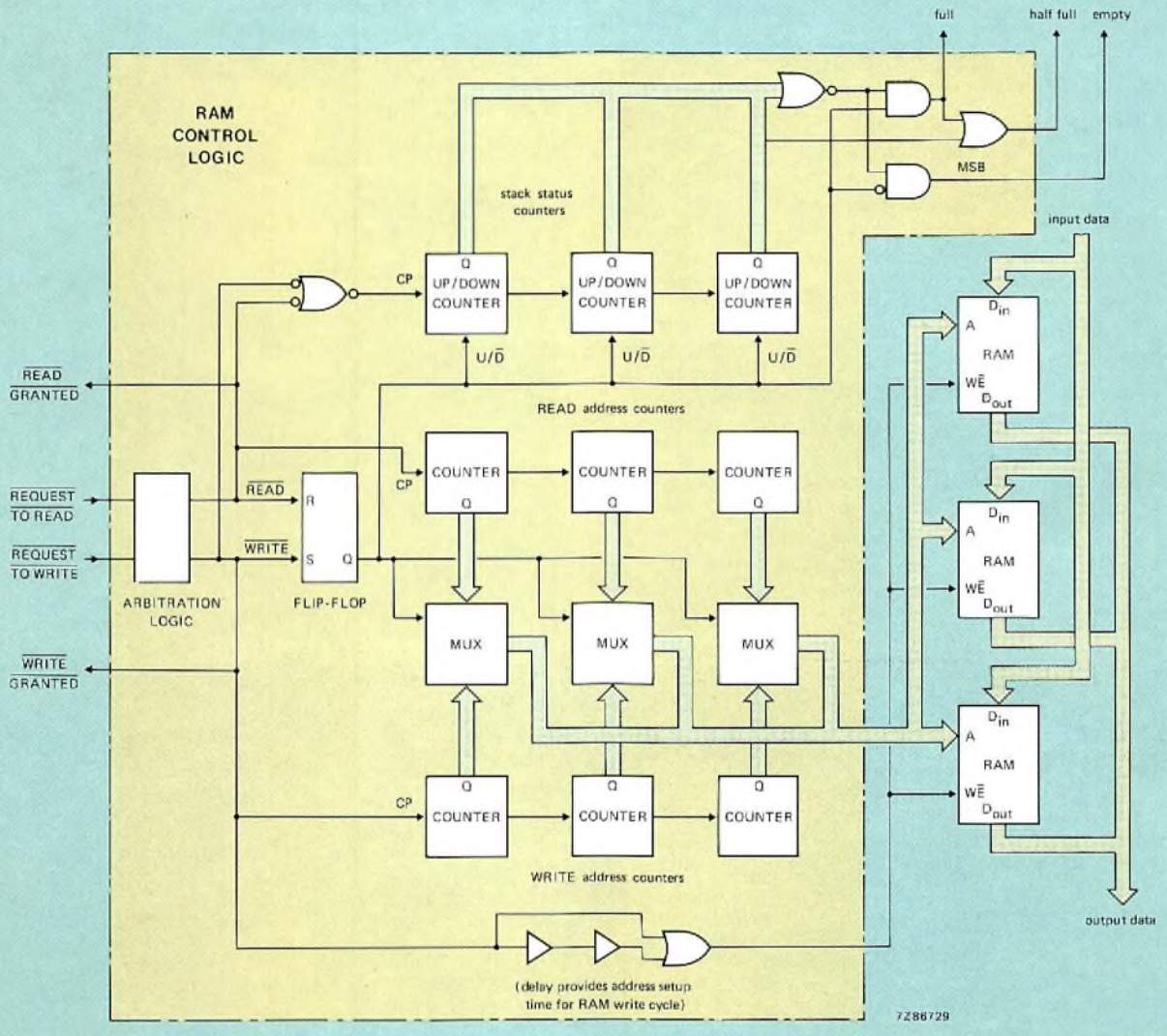


Fig.5 Conventional RAM chips can be addressed in FIFO sequence by using this hardware controller. The disadvantage of this method is that the circuit requires about 16 digital ICs plus additional RAM chips

this FIFO/RAM combination can exceed 8 MHz, which competes with current FIFO memories but does not suffer the lengthy data fall-through delays associated with them.

The signals associated with the 8X60 are identified in Fig.7; a block diagram of the chip is shown in Fig.8.

The 8X60 controls FIFO buffering by generating the addresses used to access the RAM. Also it interprets control signals from the sub-systems that are being interfaced and provides appropriate status information. Separate handshake control lines are used to request either write or read operation. A request for either operation causes the appropriate RAM location to be addressed. Once the address is stable, the corresponding control output acknowledges that the request has been granted. Upon completion of the data transfer to or from the RAM, the request input is removed. This causes the control output, and then the address output, to be terminated.

Write-cycle operation is as follows: When the $\overline{SI}$ (Shift In) request input goes low, the write operation will start – provided the read cycle is not in progress (as determined by the arbitration logic) and provided the stack is not full (as determined by the status signal). Then the write address will appear on the outputs and, after the address has stabilised, the $\overline{WRITE}$ output will go low. When the $\overline{SI}$ input is returned to the high state, the $\overline{WRITE}$ output goes high before the address outputs are disabled. The write-address counter and status counter are then both incremented.

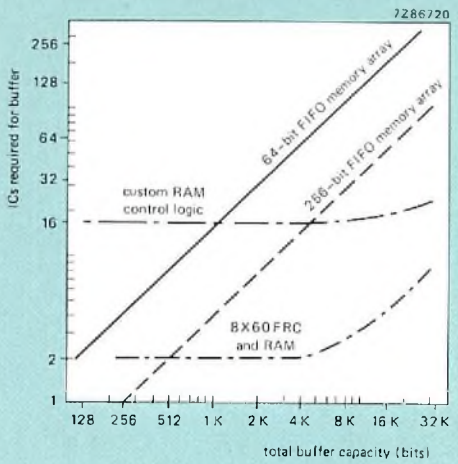


Fig.6 As the size of a FIFO buffer memory increases, the parts count increases rapidly when FIFO chips are used. When RAMs are used, the count climbs more slowly. Use of the 8X60 provides the most compact system for large FIFO buffers. The graph assumes the use of RAMs with capacities up to 4-kbits

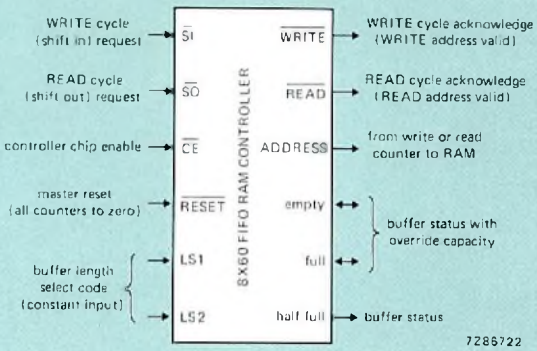


Fig.7 Signal connections to the 8X60 RAM controller are shown here grouped by function. The $\overline{SI}$ and $\overline{SO}$ lines initiate write and read cycles, respectively

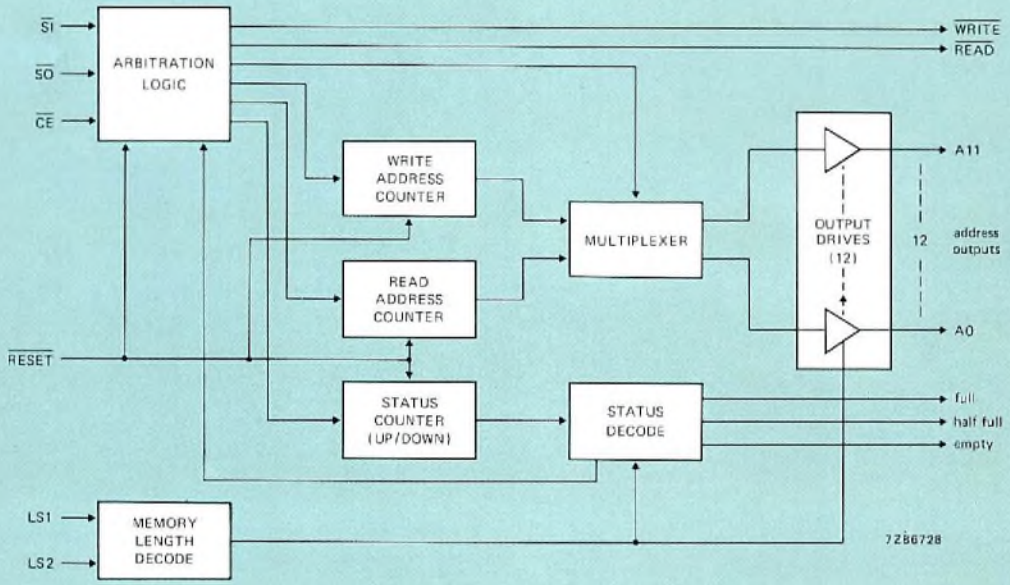


Fig.8 The 8X60 provides all the functions needed to control RAMs so that they function as FIFO buffers. As shown in this internal block diagram, the circuit generates all necessary addresses and status codes. Arbitration logic establishes priorities of concurrent read and write requests

When the $\overline{SO}$ (Shift Out) request input goes low, the read cycle will begin – provided a write cycle is not in progress and the buffer is not empty. The read address will appear on the outputs and the $\overline{READ}$ output will go low. When $\overline{SO}$ is returned high, $\overline{READ}$ goes high. The Address outputs are disabled, the read-address counter is incremented, and the status counter is decremented.

To avert the possibility of operational conflicts, arbitration logic ensures that $\overline{SI}$ and $\overline{SO}$ are treated on a first-come first-served basis. If one cycle is requested while the other is in progress, the requested cycle will begin as soon as the one in progress is completed.

The buffer length of the FIFO memory can be hardware selected via the Length-Select inputs (LS1 and LS2) as

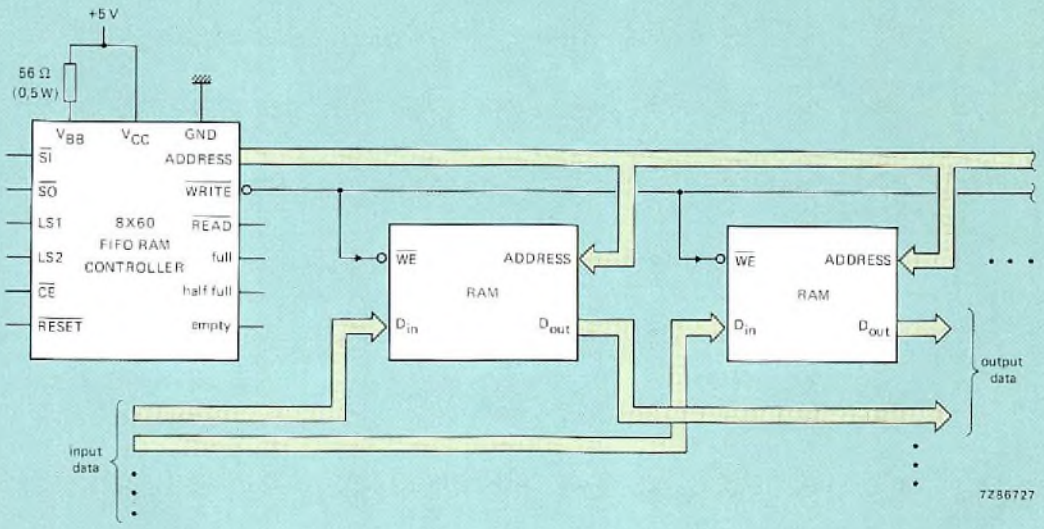


Fig.9 A FIFO buffer can be built by connecting the 8X60 controller to RAM chips as shown. Several RAMs can be connected in parallel to achieve the desired word width. For this simple configuration, the address space of each RAM equals the desired FIFO buffer length

shown in the table. When the selected length is less than the maximum available, the unused high-order address outputs are inhibited (placed in the high-impedance state).

Signal combinations for buffer-length selection

LS1	LS2	half length (words)	full length (words)
L	L	2048	4096
H	L	32	64
L	H	512	1024
H	H	128	256

The 8X60 also generates status signals indicating whether the FIFO buffer is empty, full (no more available locations), or at least half-full.

Almost any semiconductor RAM can be used with the 8X60. It provides control signals that can be used directly to control the Write-Enable ($\overline{WE}$) input to a RAM (Fig.9), provided that the address setup time required by the RAM is sufficiently short (no more than 5 ns).

The most convenient way to build a buffer memory around the 8X60 is to use RAMs that have an address space equal to the desired FIFO buffer depth. The number of devices required is then determined solely by the word width. The buffer can also use RAMs of different sizes, but some design effort will be required to address them using conventional address decoding techniques. In this case, the chip-select decoder itself must be disabled until an I/O operation commences – to provide sufficient address setup time during a write cycle.

Since the 8X60 achieves FIFO operation through simple control of address lines, a number of interesting memory designs and FIFO applications become possible. For example, consider an 8X60 connected to the low-order address lines of a large computer memory. The Chip-Enable ($\overline{CE}$) input to the 8X60 could be controlled to enable the address outputs and FIFO control operations upon request from the processor. A large, hardware FIFO memory space would then be available to the system and/or software designer (see Fig.10).

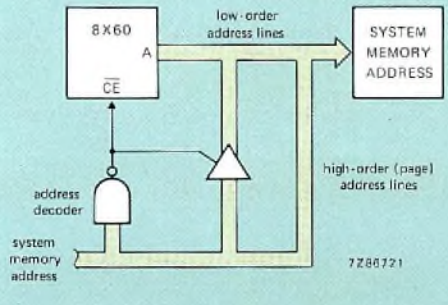


Fig.10 To use a segment of a large system memory as a FIFO buffer, you can connect the 8X60 to the low-order address lines of the memory. In this way, a page of the computer's memory is dedicated as a FIFO buffer. The SI and SO inputs to the 8X60 can be derived from the system's read/write control lines

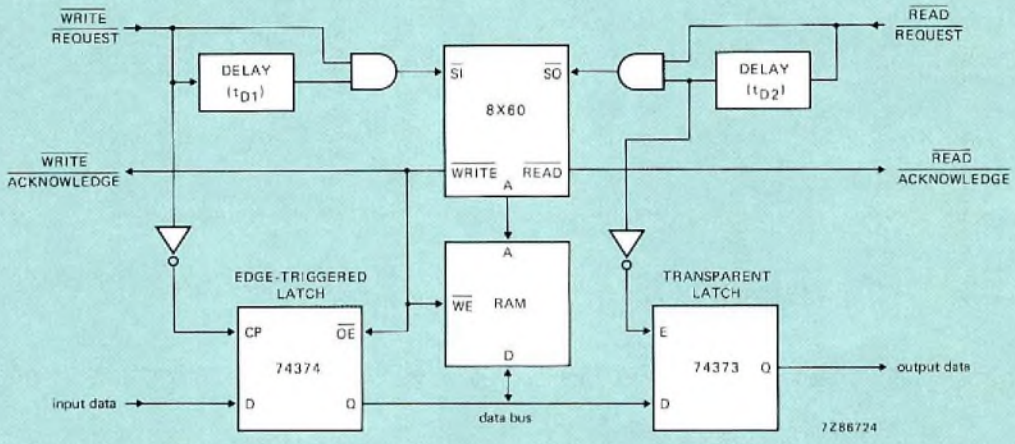


Fig.11 Data pipeline latching avoids system delays when data must be written into or read from the buffer instantaneously. The scheme requires extra logic, and time delays may have to be included to allow access time for data transfer to and from the RAM. Delay t_{D1} maintains an adequate write pulse for the RAM; delay t_{D2} provides RAM address access and latch setup times

The arbitration logic in the 8X60 allows it to interface between two asynchronous systems – much like a dual-port memory. However, an important difference is that the RAM may not be immediately available for access upon request if the opposing cycle is in progress. For applications that cannot tolerate the arbitrary delay of one cycle before a request is granted, data latches may be used to interface the RAM input and/or output data, thus forming a data pipeline.

One way of implementing a full input and output pipeline is shown in Fig.11. The block diagram also shows where delay circuitry could be included, if necessary, to provide sufficient access time for data transfer into and out of the RAM.

Since the 8X60 does not actually handle the buffered data, any interfacing to the RAM data lines should be designed to suit the particular application. With an interface as shown in Fig.11, a data word can be written or read immediately upon request, while the actual data transfer to or from the FIFO buffer may occur at any time thereafter.

Large FIFO buffers can be extremely useful in system design. The 8X60 controller coupled with standard RAMs, provides designers with a cost-effective and straightforward method for building them.

ACKNOWLEDGEMENT

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Higher quality synthesised speech through fast and easy editing

Most manufacturers have opted for either waveform analysis or straight linear predictive coding (LPC) to achieve low bit rates (1-2 kbits/s) for their voice synthesisers. However, it seems that some of them will soon abandon their initial choice in favour of formant synthesis. Formant synthesis is a variation of LPC, and was first used in our fully digital MEA8000 voice synthesiser described in the reference. The MEA8000 is steadily gaining popularity because it has all the advantages of LPC but reduces the bit rate by a further 30%.

Any voice synthesiser needs an editing system to obtain the lowest possible bit rate and the highest possible speech quality. Present editing systems for both waveform analysis and LPC synthesisers have the severe disadvantage that the speech to be edited is usually displayed on a screen in the form of complex tables of parameters. It is a specialised task to edit these parameters because the editor must know what the codes mean before he can start.

We have overcome this disadvantage with our new editing system for the MEA8000. The parameters of the synthesised voice are displayed on a screen graphically instead of as codes. Speech editing is so simplified by this method that the entire editing process can now be learnt in only half a day.

The spoken message to be encoded is recorded on an audio cassette tape and taken to one of our four editing centres in Europe. The speech is then digitised, and analysed by a host computer so that it is in a form suitable for the MEA8000. The synthesised speech parameters generated by the computer are four formants, pitch, amplitude and information as to whether the sounds are voiced or unvoiced.

As shown in the photograph, the speech to be edited is displayed on a c.r.t. screen as up to 128 frames of 8 to 64 ms each. Any parameter can be changed over the complete display, or over only part of it. Any discontinuities in the interpolated values which would cause distortion of the edited synthesised voice are clearly visible on the screen, and can easily be erased.

Another unique feature of our editing system is a facility for making an A-B comparison between successive versions of the edited speech and between the edited speech and the original recorded message. This facility allows the quality of the synthesised signal to be monitored throughout the editing process. This is an essential feature for any good editing system because speech quality is very subjective, and much of the editing process is a matter of getting the voice to sound right. For this reason, we always invite the customer to supervise the editing. By altering the amplitudes, voiced/unvoiced sections and formant frequencies/bandwidths, the speech can be made to sound as natural as possible. Several other facilities are available to make the editing process very efficient, including the possibility of listening to the message step by step. Any unnatural sounds heard in the A-B comparison can be easily located on the screen by examining the shape of the displayed parameter curves. The synthesised speech can even be made better than that on the original tape by altering the intonation and amplitude of some words to obtain a desired emphasis.

Once the quality has been perfected, the next important step is to reduce the bit rate needed by the MEA8000 to produce the sound. This is done by extending the length of any speech frames that contain only slow changes of parameters. The normal speech frame duration is 8 ms but, when the parameters change slowly (as with the longer vowels, and the letters 's' and 'f'), the frame duration can be prolonged to 16, 32 or 64 ms, with a corresponding reduction of bit rate. This operation is very simple because the graphic display shows the information very clearly.

We are currently developing a stand-alone speech editing system which will be made available to customers so that, once we have supplied the software, they can do the editing for the MEA8000 on their own premises.

REFERENCE

VAN BRÜCK, H. E. and TEULING, D. J. A. 'Integrated voice synthesiser' Electronic Components and Applications, Vol. 4, No. 2, February 1982, pp 72-79.

Using the natural infrared radiation of the environment, thermal imagers can see through fog and smoke, even in total darkness. They can also picture much that is otherwise invisible, such as heat loss and patterns of temperature distribution. Present developments in infrared detectors promise to simplify both the optics and electronics of tomorrow's thermal imagers.

Detectors for thermal imaging

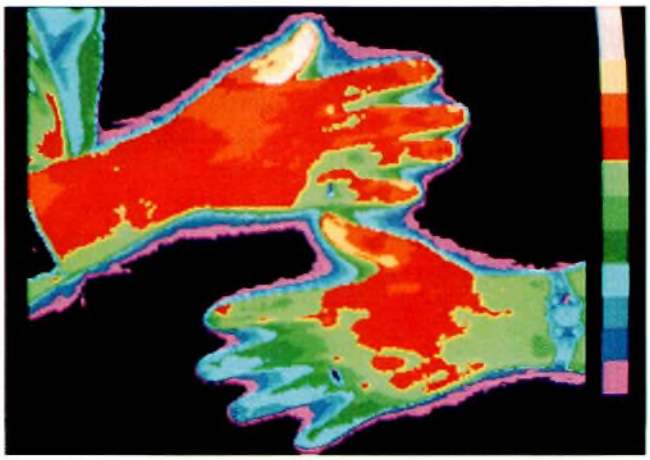
J. A. CHIARI and F. D. MORTEN

Thermal imaging converts the infrared radiation of a scene into a live picture of that scene; the thermal image is a pictorial representation of temperature differences. In so far as it is displayed on a scanned raster, the thermal image may more or less resemble a television picture of the scene.

Originally developed to extend the scope of night vision systems, thermal imagers at first provided an alternative to image intensifiers. As the technology has matured, however, its range of application has expanded and now extends into fields that have little or no relation to night vision.

Energy conservation and management. Thermal imaging can visually identify areas of heat loss from buildings and industrial installations; quite simple thermal imagers can be used to inspect pipe lagging and other forms of insulation.

Thermal image made at night with a SPRITE detector (see pp. 247-8); black is hot. (Photo courtesy of Marconi Avionics)



Being non-invasive, thermography is the method of choice in diagnosing joint diseases. Here, the ten-colour display clearly reveals deficient vascularisation of the left hand. (Photo courtesy of Philips Medical Systems)

Medical thermography. Thermal imaging can reveal diagnostically significant patterns of body temperature distribution; the procedure is simple and completely hazard-free for both patient and operator.

Security surveillance. Thermal imaging surveillance systems can work in total darkness; unlike radar or ultrasonic systems, they radiate no energy, so they are undetectable.

Aerial surveys. Thermal imaging from the air can reveal otherwise invisible geological and ecological features.

Meteorological survey by satellite. Temperature gradients and discontinuities discerned by thermal imaging significantly augment the information obtainable by observation in the visible part of the spectrum.

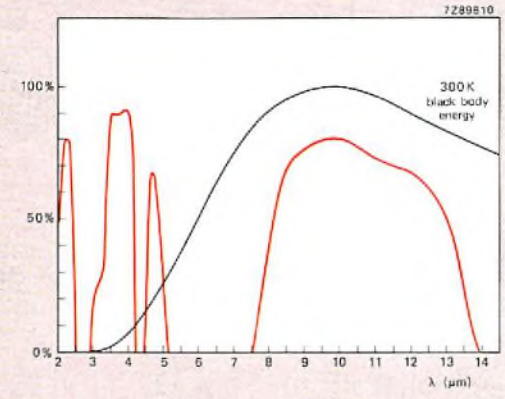


Fig.1 The atmosphere is most transparent to infrared at wavelengths between 3 μm and 5 μm and from 8 μm to 13 μm. The red curves show the transmission of infrared over a distance of a mile (1.6 km); the black curve shows the spectrum of black-body radiation at 300 K

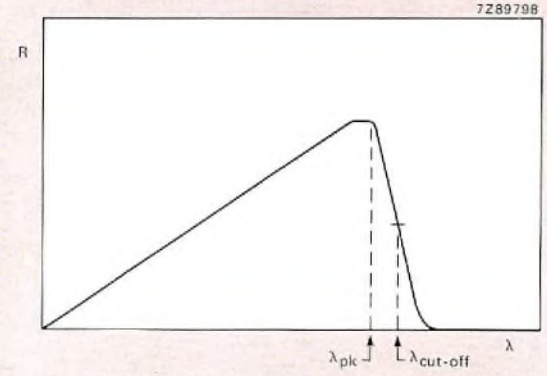


Fig.2 The responsivity R of a quantum detector falls off rapidly above the peak response wavelength λ_{pk} of the semiconductor used; at the cut-off wavelength, responsivity is down to half its peak value

Police, fire, and rescue services. Thermal imagers have the advantage over image intensifiers that they can see through fog and smoke as well as in darkness. In murky weather they can distinguish detail over far greater distances than the eye.

Thermal imagers for all these applications operate in one of two 'windows' where the atmosphere is especially transparent to infrared: one for wavelengths between 3 μm and and 5 μm and the other for wavelengths from about 8 μm to 13 μm. The infrared radiation of objects at ordinary temperatures (i.e. around 300 K) coincides well with the 8 μm to 13 μm window, which is where high-performance thermal imagers are designed to operate. At higher temperatures the peak of the radiation spectrum shifts toward the shorter wavelengths, making the 3 μm to 5 μm window more suitable for viewing objects significantly hotter than the environmental average. Imagers for operation there are generally simpler and cheaper than 8 μm to 13 μm imagers, but with inherently lower performance potential. However, where atmospheric humidity is high, this may be at least partially offset by the fact that humidity absorbs infrared much less at 3 μm to 5 μm than at 8 μm to 13 μm.

INFRARED DETECTORS

Quantum detectors

The detectors most used in thermal imagers are quantum detectors. In a quantum detector incident radiation excites excess carriers in proportion to its intensity. The response is rapid, generally of the order of a microsecond.

Quantum detectors are semiconductors in which the band-gap energy is less than the photon energy of the radiation to be detected; i.e. about 0.25 eV for detectors working at 3 μm to 5 μm, and about 0.1 eV for those working at 8 μm to 13 μm. Silicon (1.15 eV) and germanium (0.75 eV) are therefore unsuitable.

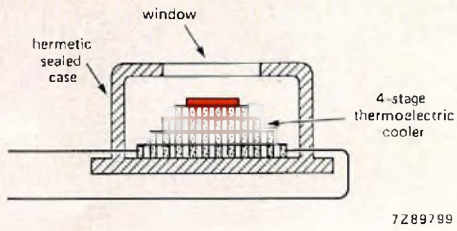
Of the materials which are suitable, two that are preferred in present-day detectors are lead tin telluride and, especially, cadmium mercury telluride. Both have the advantage that they can be adapted for use either at 8 μm to 13 μm or at 3 μm to 5 μm by varying their composition.

Operating mode

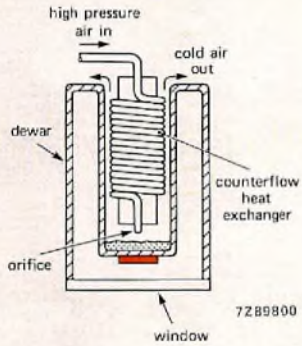
Quantum detectors are classified according to their mode of operation: photovoltaic or photoconductive.

- In a photovoltaic detector the field across a p-n junction separates carriers of opposite polarity to produce an e.m.f.
- In a photoconductive detector the conductivity of the semiconductor increases in proportion to the number of excess carriers; the detector is biased so that the conductivity change causes a corresponding voltage change.

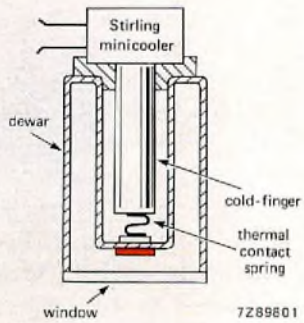
Lead tin telluride is a photovoltaic detector. Cadmium mercury telluride can also be used as a photovoltaic detector but is mainly used as a photoconductive one. Photoconductive detectors are generally preferred because they are easier to couple to the required preamplifiers. However, in high-performance systems using many detector elements close together, the heat generated by the bias current can cause cooling problems. For such systems it is likely that photovoltaic detectors, which do not require any bias current, will come into increasing use.



(a) A four-stage thermoelectric cooler (Peltier effect) built into the encapsulation of a 3 μm to 5 μm detector can cool it to 193 K in about 25 seconds using only a few watts



(b) A Joule-Thomson cooler using bottled compressed gas (e.g. air) can cool an 8 μm to 13 μm detector to 80 K and keep it there for as long as the gas supply lasts; one with its own compressor requires about 30 seconds cool-down time and consumes about 80 W per watt of cooling load



(c) A Stirling-cycle cooling engine requires about 5 to 10 minutes cool-down time to 80 K and consumes about 50 W per watt of cooling load; the working fluid is helium

Fig.3 Three ways of cooling infrared detectors

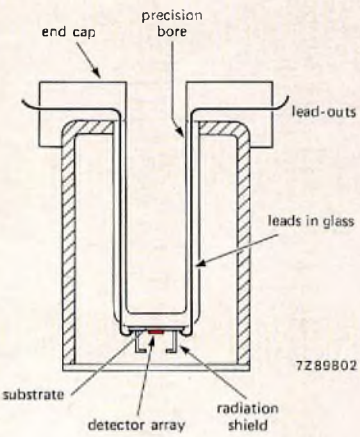


Fig.4 Simplified cross-section of dewar with infrared detector mounted

Fig.5 Precision-bore inner wall of a dewar before assembly, showing leads-in-glass construction

Cooling

At ordinary temperatures the signal output of an infrared quantum detector is very small and is swamped by thermal noise due to random generation and recombination of electron-hole pairs in the semiconductor. To make the detector sensitive enough to resolve small temperature differences in the scene being observed, and to make the response clearly distinguishable from the thermal noise, the detector must be cooled to cryogenic temperature: about 193 K (–80 °C) for detectors working at 3 μm to 5 μm, and about 80 K (–193 °C) for those working at 8 μm to 13 μm. Figure 3 shows three types of cooler used with infrared quantum detectors.

Joule-Thomson and engine-cooled detectors are mounted in precision-bore dewars into which the cooling device is inserted (Fig. 4). The detector is mounted in the vacuum space at the end of the inner wall and looks out through an infrared window of germanium, silicon, or sapphire. It is surrounded

by a cooled radiation shield that matches its acceptance angle to the convergence angle of the infrared optical system. In dewars of our manufacture the electrical connections to the detector elements are made via wires embedded in the inner wall of the dewar (Fig. 5), a construction which protects them from damage due to vibration.

Thermoelectrically cooled detectors are usually mounted in a hermetic encapsulation with a base designed for good contact with a heatsink (Fig. 6).

Fig.6 Thermoelectrically cooled vacuum encapsulation for 3 μm to 5 μm infrared detectors with up to 64 elements. The radial connectors around the window are for the detector elements, the two prongs near the base are for the cooler supply

Thermal detectors

Infrared radiation incident on a thermal detector changes an electrical property of the detector element by causing a small change in its temperature; thermal detectors do not require cooling. Their response is much slower than that of quantum detectors, and they are extensively used in non-imaging applications such as fire and intruder detection and remote sensing. The pyroelectric vidicon is an imaging device that does use a thermal detector, but it responds only to time variations in scene temperatures. This can be an advantage, however, in surveillance systems, where it can detect any change in an otherwise static scene.

IMAGING TECHNIQUES

In present-day thermal imagers the infrared image is optically focused and mechanically scanned across a detector whose output is electronically converted into a visual image. Depending upon the performance required, the detector may consist of one or many elements. The optics, the mode of scanning, the detector configuration, and the signal-processing electronics are closely interrelated.

Single-element scan

To obtain a thermal image from a single-element detector, the focused infrared image is scanned across the element line by line (Fig. 7). Variations in the electrical output of the element are amplified to drive a display which is scanned in synchronism with the detector to generate an optical counterpart of the infrared image.

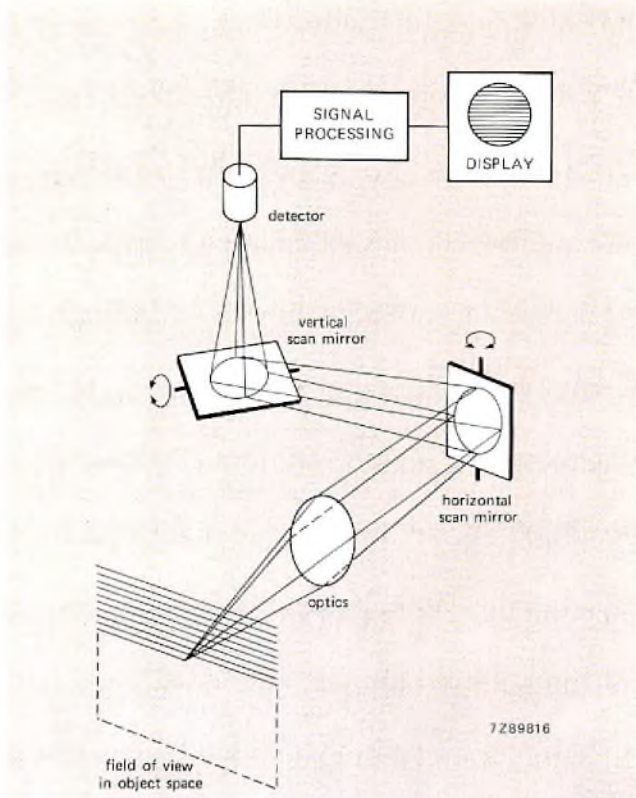


Fig.7 Principle of a simple scanning and imaging system (proportions and optical path lengths distorted for illustrative purposes). One mirror oscillates rapidly about a vertical axis to scan the field of view horizontally; another oscillates less rapidly about a horizontal axis to scan it vertically. The display is electronically scanned in synchronism to generate a visual counterpart of the infrared image

For a flicker-free display the whole image should be scanned at least twenty-five times a second. If the resolution along each line is to be comparable with tv standards, the signal processing circuits must have a large bandwidth and the output will contain a correspondingly large noise component. The performance of a single-element detector is therefore limited, and a 70-line image is about the best that can be done with reasonable sensitivity.

Multi-element scan

Multi-element detectors overcome many of the shortcomings of single-element detectors. The elements can be arranged so that a cumulative output is obtained by summing the outputs of individual elements (serial scan), or so that a simpler, slower-speed scanning system can be used (parallel scan). Combinations of the two arrangements are also practical.

If n elements are used, the signal-to-noise ratio can be improved by a factor $\sqrt{n}$; about 30 elements are required before the improvement is significant. Experimental detectors with up to 384 have been built, but the practical maximum is currently about 200.

Serial scan

Figure 8 illustrates serial scanning of a detector consisting of a row of eight elements. The scanning mechanism could be the same as that shown for a single element detector in Fig. 7. To obtain an output signal equal to eight times that of a single element, the eight outputs are added together in phase. However, as the noise contribution of the separate elements is incoherent, the noise in the cumulative output only increases by $\sqrt{8}$.

The image from a serial-scanned array can be diplayed by a light-emitting diode (LED) scanned synchronously or by a cathode ray tube (e.g. a tv picture tube). Since the same detector elements scan all lines of the infrared image, the uniformity of the displayed image is good. However, for an image consisting of many lines (e.g. 625 for tv compatibility), the required scanning speed is too high to be mechanically practical and the required bandwidth of the signal-processing electronics is inconveniently large.

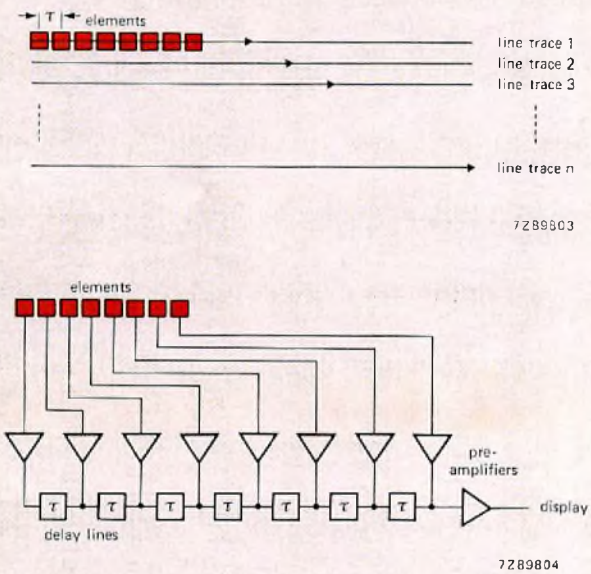


Fig.8 Serial scanning of an eight-element array. Horizontal deflection sweeps each line of the image across the whole array; vertical deflection shifts successive image lines into line with the array. Delay lines and summation circuits in the signal-processing electronics provide for the signals from the separate elements to be added together in phase

Parallel scan

If the detector contains one element for each line of the image (Fig. 9), the image need only be scanned in one direction - horizontally across the row of elements. The required scanning speed is therefore slower and the deflection simpler. Figure 10 illustrates a practical arrangement in which the display is provided by a row of LEDs corresponding to the row of detector elements.

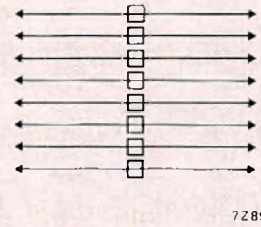


Fig.9 Parallel scan. The image is swept back and forth across the array and each detector element generates one picture line

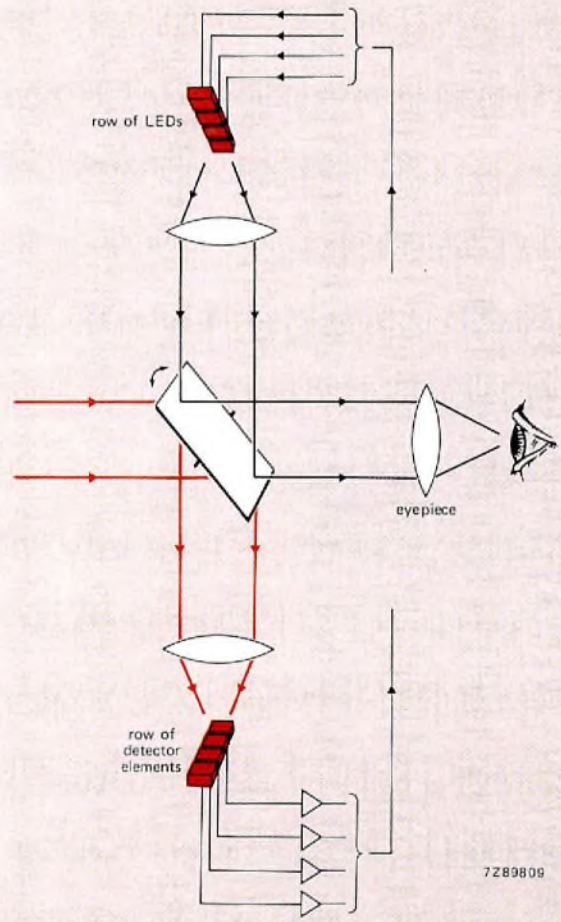
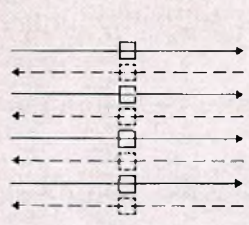
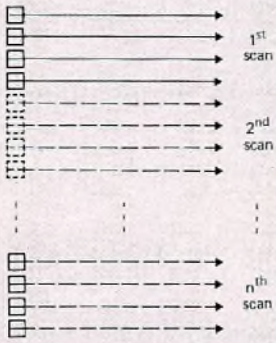


Fig.10 Parallel scan with an oscillating mirror silvered on both sides. One side of the mirror sweeps the infrared image back and forth across the row of detector elements; the amplified output of each element drives a corresponding LED. The other side of the mirror sweeps the image of the LEDs back and forth across the eyepiece to produce a visual counterpart of the infrared image

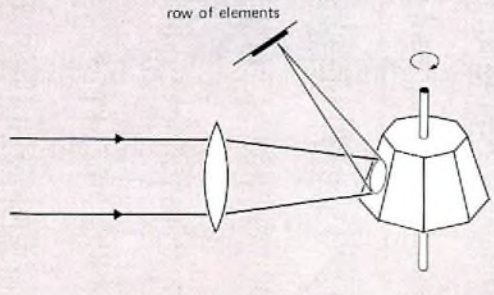


(a) Interlaced parallel scan doubles the number of lines that can be obtained from a given number of elements. The elements are spaced a line-width apart and the scanning optics are arranged to displace the infrared image by that amount on alternate scans

7Z89806



(b) Banded parallel scan more than doubles the number of lines. The detector is a close-spaced row of elements across which the horizontal deflection sweeps an image band as wide as the row is long. The vertical deflection shifts successive horizontal deflections by the width of one band



7Z89815

(c) One way of providing banded parallel scan is with a multi-faceted rotating mirror. The inclination angles of the facets are stepped so as to shift the image by the width of one band at a time. As each facet passes the lens it sweeps one band across the detector array; the next facet sweeps the next lower band, and so on. An eight-faceted mirror as shown would enable a 60-element array to generate 480 lines

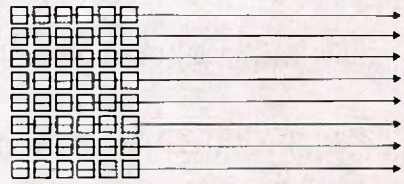
Fig.11 Interlaced and banded parallel scan

Because of the lower scanning speed, parallel scan requires less bandwidth than serial scan. However, the performance of the detector elements, amplifiers, and LEDs must be extremely uniform, otherwise the picture will be streaky.

If the picture is to be displayed by a cathode-ray tube instead of by a row of LEDs, the signal-processing electronics must include a parallel-to-serial scan converter and a frame buffer. For 625-line CCIR tv compatibility, the detector would have to consist of 625 elements, which is more than is practical. A way around that requirement is to use interlaced or banded parallel scan (Fig. 11).

Serial-parallel scan

Banded parallel scan of a matrix array as shown in Fig. 12 combines the output amplitude advantage of serial scan with some of the speed and bandwidth advantage of parallel scan. However, providing separate connections to all the detector elements in the plane of such an array is impracticable. Practical arrays for serial-parallel scan overcome that barrier by staggering the elements, as in the staircase array of Fig. 13, at the cost of some increase in the complexity of the signal-processing electronics.



7Z89807

Fig.12 Idealised detector array for serial-parallel scan of eight image lines at a time, each line being represented by the cumulative output of six detector elements. Bringing out separate leads from each element to the signal-processing circuits is a practical barrier

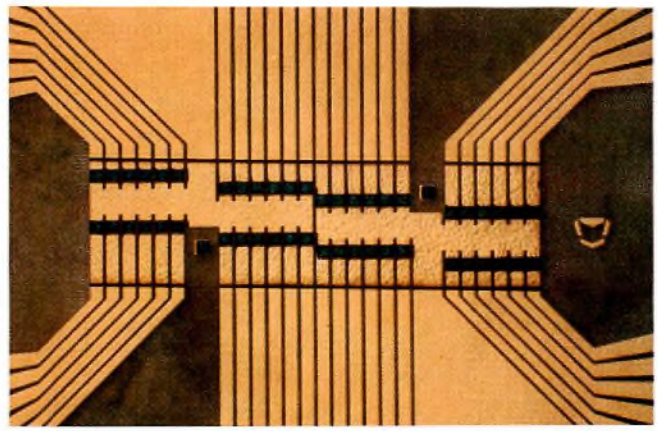


Fig.13 Practical detector array for 8 x 6 serial-parallel scan. Staggering the elements to solve the connection problem introduces delays between image lines that have to be compensated in the signal-processing electronics

Focal-plane processing arrays

Signal processing in the element

A drawback of serial scan is the need for multiple preamplifiers and delay lines in the signal processing circuitry. A recent advance that overcomes that drawback is the SPRITE (Signal PRocessing In The Element) detector invented at the Royal Signals and Radar Establishment, Great Malvern, and developed at Mullard, Southampton (Ref. 2 and 3). In a SPRITE

detector a single strip of CMT with only three connections replaces a whole row of discrete elements of a conventional serial-scanned detector. It requires only one preamplifier and no external delay lines (Fig. 14).

The sensitive element of a SPRITE detector is elongated in the direction of scan and biased in such a way that the carrier drift velocity exactly matches the scan velocity. As each image point travels the length of the element the carriers it excites travel with it and continue to accumulate. Thus, the signal integration which, for a conventional array is done by external delay lines and summation circuitry, is in the SPRITE detector done in the element itself.

The eight-element SPRITE detector shown in Fig. 15 and 16 is equivalent in performance to an array of at least 64 discrete elements, but requires only 24 connections instead of 65; the simplification of the external circuitry it allows is even more significant.

The number of SPRITE elements that can be combined in a single detector is ultimately limited, as in other photoconductive detectors, by the balance between practical cooling capacity and the heat generated by the detector bias current. Experimental 16 and 24-element SPRITE arrays have been made and tested under laboratory conditions.

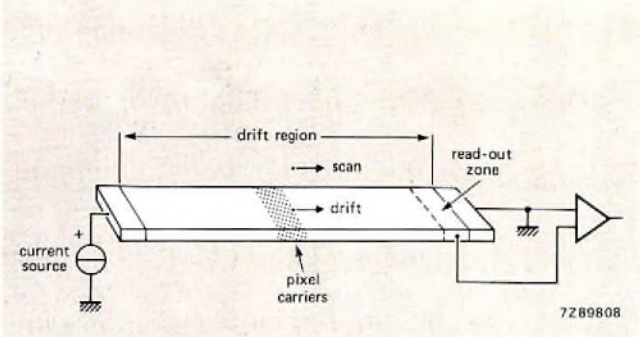


Fig.14 The SPRITE detector element: an elongate strip of CMT biased so that the carrier drift velocity equals the scan velocity of the infrared image

Staring arrays

Although the SPRITE detector eliminates many of the connections and much of the circuitry required with discrete-element arrays, it still has to be mechanically scanned. Other approaches to focal-plane processing now being pursued aim at eliminating that requirement too, at least in applications in which a limited number of picture elements (pixels) will suffice. Figure 17, for instance, shows an experimental staring array that is scanned electronically by circuits integrated with the array; the function of the associated optics is reduced merely to focusing the infrared image onto the matrix of sensitive elements. A long-term goal is to produce staring arrays with upwards of 10^5 elements (Ref. 4 and 5).

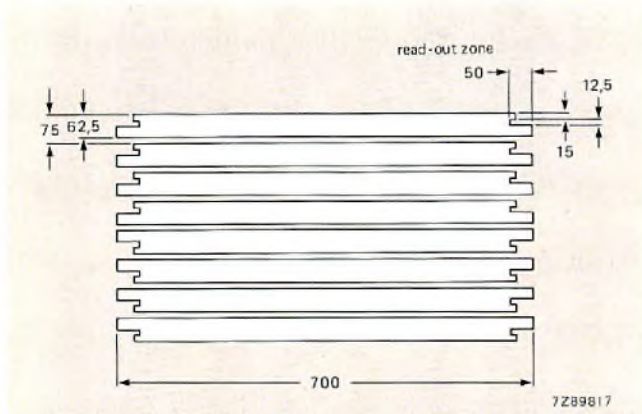


Fig.15 Eight-element SPRITE array for parallel scan; dimensions in μm

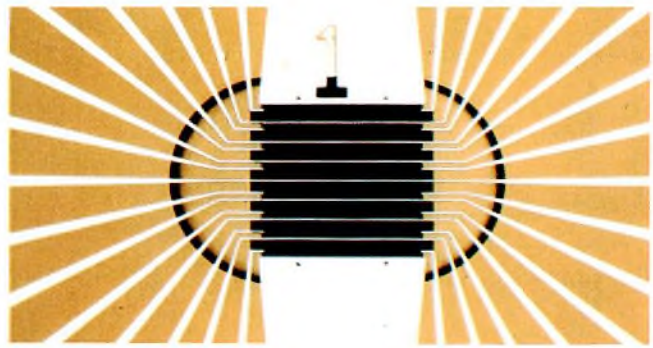


Fig.16 Eight-element SPRITE array, about 35 times actual size.

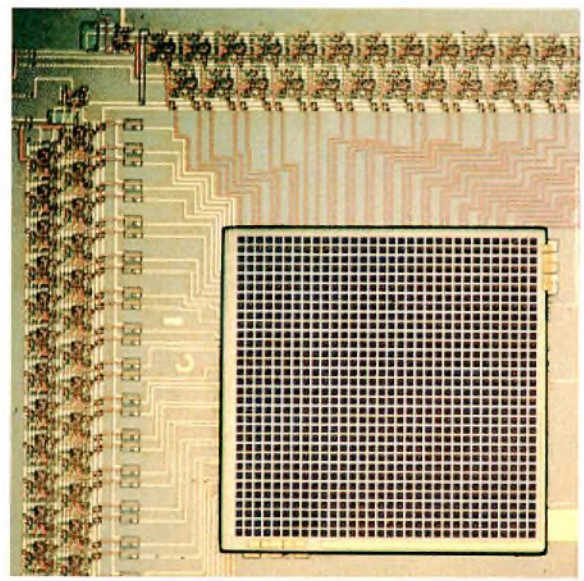


Fig.17 Photomicrograph of the sensitive area of an experimental staring array in which the detector elements are scanned electronically instead of optically; the element pitch is 40 μm

DETECTOR PARAMETERS

The parameters by which infrared detectors are usually specified are responsivity, noise, detectivity, time constant, and cut-off wavelength.

Noise, together with responsivity, determines a detector's ability to detect small input signals. It is a function of frequency; there is a low-frequency region of flicker or 1/f noise, a flat mid region, and a high-frequency roll-off determined by the detector time constant. Noise may be specified at one or a number of frequencies, or as a noise spectrum. It is expressed in $V/Hz^{1/2}$.

Responsivity, R, is the ratio of output voltage to radiant input power, expressed in volts per watt. As the output voltage due to incident radiation is a very small fraction (about 10^{-5}) of the d.c. bias voltage across the detector, the responsivity is measured by exposing the detector to chopped radiation from a calibrated source and measuring the alternating voltage component at the chopping frequency.

Detectivity, D*, is a figure of merit that takes account of resposivity, noise, and detector size; it is expressed in $cmHz^{1/2}/W$.

$$D^* = \frac{V_S}{V_n} \frac{\sqrt{(A\Delta f)}}{W}$$

where

V_S = r.m.s. signal voltage
V_n = r.m.s. noise voltage in the bandwith Δf
A = detector area
W = r.m.s. radiation power incident on the detector

As D* varies with the wavelength of the radiation and the frequency at which the noise is measured, these are stated in parentheses whenever D* is given. For example, D*(5μm, 800 Hz, 1) means that the given value was measured at 5μm wavelength, with the noise measured at 800 Hz; the 1 means that the measurement has been normalised to unit bandwidth. D* may also be measured at a specific black-body temperature, in which case that, instead of the wavelength, is stated.

For a SPRITE element D* is, by convention, based on a nominal sensitive area A equal to a square with a side equal to the element width (i.e. 62.5 μm).

An advantage of D* as a figure of merit is that it enables one to calculate a theoretical maximum detectivity that would apply when performance is limited only by noise due to fluctuation of the background radiation. That maximum depends on the cut-off wavelength of the detector and its field of view and is denoted D^*_{BLIP} (for Background Limited Infrared Photodetection).

Time constant, τ, is determined by measuring the time between incident radiation being cut off and the output of the detector falling by 63%.

Cut-off wavelength, $\lambda_{c\text{-}o}$, is the longer of the two wavelengths at which the responsivity of the detector is down to half its maximum. The wavelength at which the responsivity is maximum is denoted λ_{pk}.

Figure 18 shows the responsivity, noise, and detectivity of some typical infrared detector elements.

IMAGER PERFORMANCE

The performance of a thermal imager is usually specified in terms of temperature resolution, angular resolution, and field of view.

Temperature resolution

Temperature resolution is a measure of the smallest temperature difference in the scene that the imager can resolve; it can be expressed in two ways:

- noise equivalent temperature difference (NETD) is the temperature difference for which the signal-to-noise ratio at the input to the display is unity
- minimum resolvable temperature difference (MRTD) is the smallest temperature difference that is discernible on the display; it is typically less than 0.3 K and can be less than 0.1 K.

Temperature resolution depends on the efficiency of the optical system, the responsivity and noise of the detector, and the signal-to-noise ratio of the signal-processing circuitry.

Angular resolution

In principle, the angular resolution, in radians, is the effective width of a detector element divided by the focal length of the infrared optics. However, it may be degraded by the optical transfer function of the lens or the frequency response of the signal-processing circuitry or the display. Angular resolution is typically 1 milliradian and can be as small as 0.1 milliradian. Angular resulution is sometimes called instantaneous field of view (IFOV).

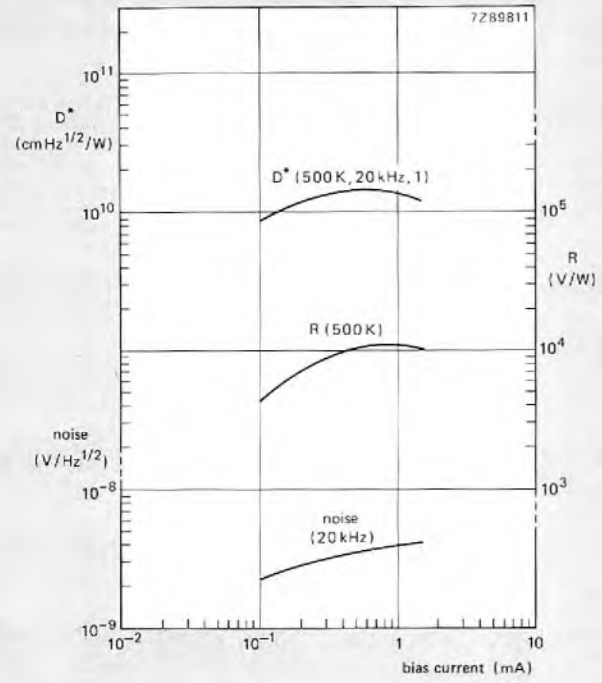
System field of view

The system field of view (sometimes called total field of view, TFOV) is the angle subtended by the scene imaged. When the angles subtended parallel to and perpendicular to the direction of scan differ, the angle subtended by the diagonal may be given. Together, the required system field of view and angular resolution determine the number of pixels required.

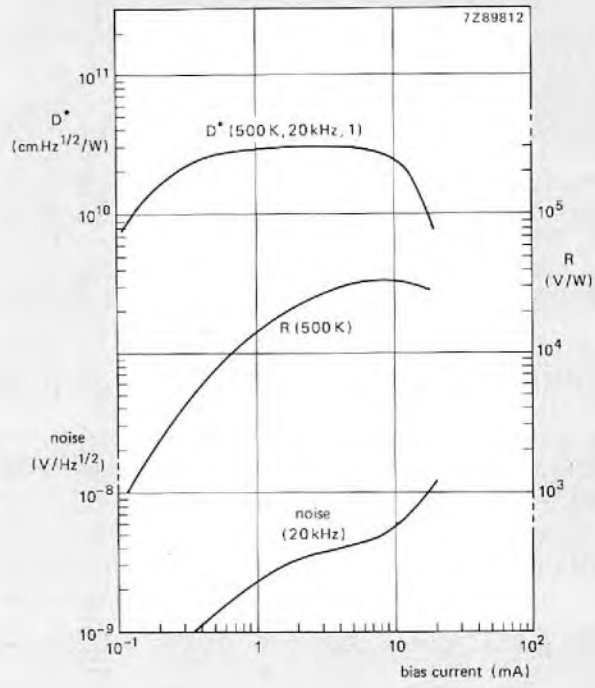
The term field of view is also used to describe the convergence angle of the infrared optics to which the detector is matched. Thus, the terms instantaneous field of view, system field of view, and detector field of view refer to three distinct quantities and must not be confused.

Performance equations

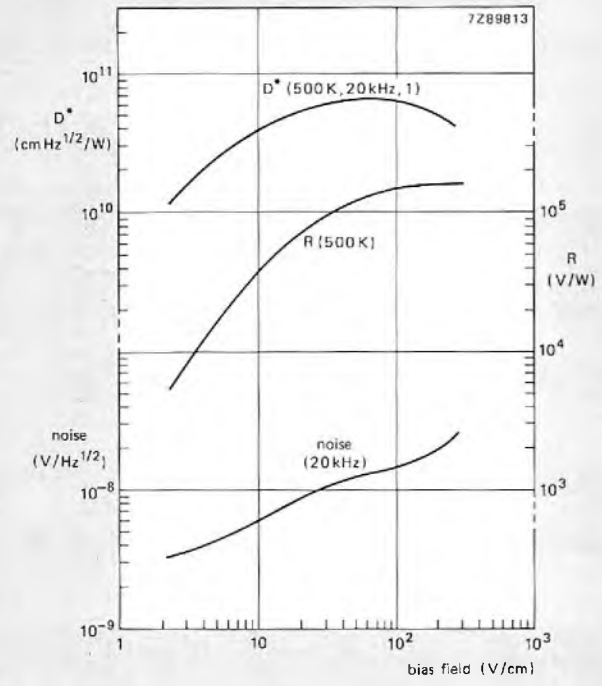
To estimate the performance of a detector in a specific imaging situation it is necessary to take account not only of its detec-



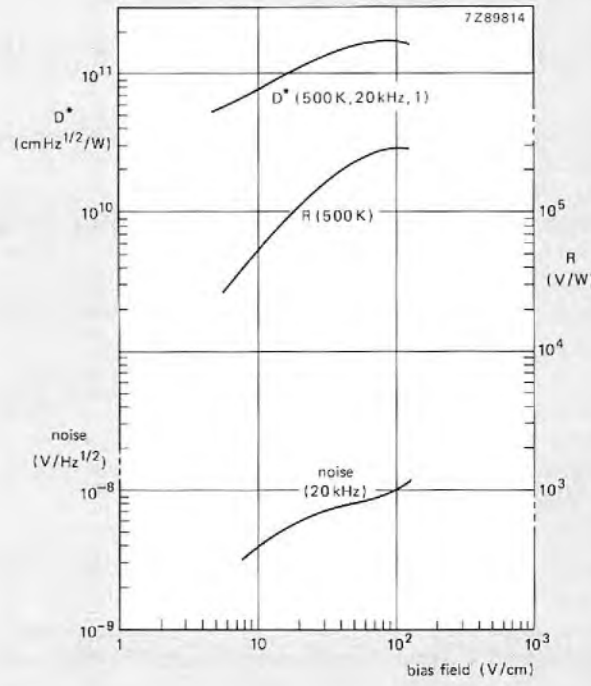
(a) 50 μm square CMT element for 3 μm to 5 μm, at 195 K



(b) 50 μm square CMT element for 8 μm to 13 μm, at 77 K



(c) SPRITE element for 3 μm to 5 μm, at 195 K



(d) SPRITE element for 8 μm to 13 μm, at 77 K

Fig.18 Responsivity, noise, and detectivity as functions of bias

tivity D* but also of the transmission characteristics of the atmosphere and the radiation characterisitics of an object to be imaged. A useful figure of merit is

$$M^*(f,T_1,L) = \int_0^\infty D^*(\lambda,f,1)t(\lambda,L)\left(\frac{dW_\lambda}{dT}\right)_{T_1} d\lambda$$

where

$t(\lambda, L)$ = the atmospheric transmission as a function of wavelength over a distance L
W_λ = the spectral exitance of the object
T_1 = the temperature of the object (considered as a black-body)

As a function of M*, the noise equivalent temperature difference is

$$NETD = \frac{1}{M^*}\frac{4F^2\sqrt{\Delta f}}{\sqrt{A}}$$

where

F = the effective f-number of the optical system (i.e. the nominal f-number multiplied by the transmission)
Δf = the electrical bandwidth
A = the sensitive area of the detector

If the NETD, the angular resolution α, and the pixel rate p are specified, and M* and the focal length F and effective diameter D of the lens are known, one can calculate the number of elements required, n, from

$$M^*\sqrt{n} = \frac{4F\sqrt{p}}{D^2\,NETD\,\alpha}$$

This equation assumes a perfect optical system, 100% scanning efficiency, and no reduction of signal-to-noise ratio in signal processing or display; it also disregards any departure from the atmospheric transmission $t(\lambda,L)$ assumed in calculating M*. Nevertheless, it does afford a useful indication of the relation between detector parameters (M*, n) and system performance (NETD, α, p).

A constraint to be observed in applying the equation is that the detector time constant τ must be shorter than the scanning time t_p per pixel: $\tau < t_p = n/p$.

DETECTOR PACKAGES

Detectors for thermal imagers are supplied only in self-contained, thermally insulated encapsulations complete with window, radiation shield, lead-outs, and provision for cooling:

- 3 μm to 5μm detectors in hermetic encapsulations with integral termoelectric cooler; Fig. 6 and 19
- 8 μm to 13 μm detectors in dewars; Fig. 20 to 23.

Within the range of standard encapsulations listed in Table 1 a variety of detector arrays is available, including SPRITE. Table 2 compares some characteristics of standard 3 μm to 5 μm and 8 μm to 13 μm multi-element arrays; Table 3, the characteristics of standard SPRITE arrays. Non-standard arrays can also be supplied to customer specifications.

Technology described in this article has been developed with support of the U.K. Ministry of Defence Procurement Executive.

Fig.19 M4RPY single-element detector for 3 μm to 5 μm; xenon-filled housing with two-stage thermo-electric cooler and sapphire window

Fig.20 M2RPY dewar for arrays of up to 50 elements; Joule-Thomson cooled, with anti-reflection coated germanium window, for 8 μm to 13 μm

Fig.21 M3RPY dewar for arrays of up to 55 elements; engine cooled, with anti-reflection coated germanium window, for 8 μm to 13 μm

Fig.22 M5RPY dewar for linear arrays of up to 120 elements; engine cooled, with anti-reflection coated window, for 3 μm to 5 μm or 8 μm to 13 μm

Fig.23 Dewar for linear arrays of up to 60 elements; engine cooled, anti-reflection coated germanium window, for 8 μm to 13 μm; a larger version accommodates up to 120 elements

TABLE 1
Detector encapsulations

	M1RPY	M2RPY	M3RPY	M4RPY
i-r wavelengths (μm)	3-5	8-13	8-13	3-5
operating temperature (K)	195	77	77	220
cooling method	thermo-electric (4-stage)	Joule-Thomson	Stirling engine	thermo-electric (2-stage)
number of elements, typ.	10-64	up to 50	up to 55	1
suitable for SPRITE array	yes	yes	yes	no

TABLE 2
Typical performance of CMT detector arrays of up to 55 elements, at 195 K and 77 K

	195 K	77 K	
cut-off wavelength	4.4	11.5	μm
element size	50 x 50	50 x 50	μm
field of view (half angle)	40	15	degrees
element bias current	0.5	2	mA
element resistance	300	50	Ω
$D^*(\lambda_{pk}, 20\,kHz, 1)$	1.5×10^{11}	5×10^{10}	$cmHz^{1/2}/W$
$D^*(500\,K, 20\,kHz, 1)$	1.5×10^{10}	2.4×10^{10}	$cmHz^{1/2}/W$
responsivity, R(500 K, 800 Hz)	1.2×10^{4}	1.5×10^{4}	V/W
time constant, τ	2	0.3	μm

TABLE 3
Typical performance of eight-element SPRITE arrays at 195 K and 77 K

	195 K	77 K	
i-r wavelengths	3-5	8-13	μm
field of view (half-angle)	14	12	degrees
element bias field	30	30	V/cm
element resistance, typ.	3000	500	Ω
power dissipation			
per element	1.5	9	mW
per array	12	80	mW
pixel rate per element	6×10^{5}	1.8×10^{6}	pixel/s
$D^*(500\,K, 20\,kHz, 1)$, mean, for 62.5 μm x 62.5 μm scan	5×10^{10}	11×10^{10}	$cmHz^{1/2}/W$
responsivity, R (500 K, 800 Hz)	1.5×10^{5}	6×10^{4}	V/W

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Abstracts

Expandable microprocessor bus for distributed processing

A microprocessor bus based on the concept of distributed processing makes it possible to expand systems from 16 to 32 bits without relying heavily on a CPU. Data can be transferred between modules connected to the bus at 24 Mbytes/s and asynchronous control information can be transferred according to priority. Address modifiers distinguish between various types of transfer, and a special facility provides for rapid transfer of messages between producer and consumer modules by overlapping memory accesses with the bus transfer period.

Schottky-barrier diodes combine the best of germanium and silicon

Silicon diodes have a wide range of reverse characteristics, a forward biased knee voltage of about 700 mV and a moderate reverse recovery time. Germanium diodes are more expensive than silicon types, the available range is not so wide and they have a long recovery time. They do however have a forward-biased knee voltage of about 200 mV. Our new range of Schottky-barrier diodes combine the desirable features of both silicon and germanium diodes because of their simple construction, low forward voltage and short reverse recovery time.

Microprocessor-based phase controller – the 'look-back' system

The performance of analogue three-phase phase controllers can be seriously impaired by phase-imbalance. By using a microprocessor to monitor the balance of the three-phase supply, the described system largely overcomes this problem and provides a number of additional benefits. Although developed specifically for a fully-controlled phase controller, the basic operating principles of the look-back system are applicable to all types of a.c. controller or three-phase bridge.

PPM management – a tool for IC quality improvement

PPM – for parts per million – is a system of quality improvement in which targets are set and the IC manufacturer is committed to improving product quality in cooperation with a manufacturer of equipment in which the products are used. PPM relates to the actual quality of the product as experienced by the equipment manufacturer in his assembly line and afterwards.

Single variable-capacitance diode for a.m. car radios

To tune the three resonant circuits often used in the a.m. section of electronically-tuned radios it is necessary to use three variable-capacitance diodes. If such diodes are manufactured in multiple units they tend to be expensive and to restrict component layout. This article describes variable capacitance diodes BB112 which operate over the tuning voltage range 1 V to 9 V (ideal for car radios) and are supplied in accurately matched sets of three.

Dielectric-resonator oscillators – a new microwave signal source

Dielectric-resonator oscillators (DROs) are microwave oscillators stabilised by a ceramic resonator. DROs are light, inexpensive and highly compatible with modern microwave integrated circuitry, and in many applications, e.g. digital telecommunications, satellite TV, radar beacons and doppler transponders, they provide an attractive alternative to conventional crystal oscillators and cavity stabilised oscillators. With a current frequency range from below 4 GHz to about 16 GHz, and with the strong chance of this being extended significantly in the future, DROs are certain to see increasing application as stable low-cost microwave signal source.

Controller IC for FIFO buffers

An LSI controller IC organises RAM chips into FIFO registers with depths up to 4K words of any desired length. Data rates can exceed 8 MHz and are not encumbered by the fall-through delays associated with FIFO chips. Internal arbitration logic resolves read-write conflicts on a first-come-first-served basis, and status signals report whether the register is full, half full, or empty.

Detectors for thermal imaging

Although the requirement for cryogenic cooling is likely to persist, recent developments in infrared detectors promise to considerably simplify the optical and signal-processing systems associated with thermal imagers. Photoconductive elements that eliminate the delay-and-integration circuitry formerly required with serial-scanned arrays are already a practical reality. Staring arrays now in advanced stages of development will also eliminate optical scanning.

Verbreiterbarer Mikroprozessorbus für verteilte Verarbeitung

Ein Mikroprozessorbus, der auf dem Prinzip der verteilten Datenverarbeitung basiert, ermöglicht es, Systeme ohne wesentliche Abhängigkeit von einer CPU von 16 Bit auf 32 Bit Breite zu erweitern. Daten lassen sich zwischen Moduln, die an den Bus angeschlossen sind, mit 24 MBytes/s übertragen; asynchrone Steuerinformationen können gemäss ihrer Priorität übertragen werden. Adressmodifizierer unterscheiden zwischen unterschiedlichen Übertragungsarten. Ein besonderes Leistungsmerkmal sind schnelle Übertragungen zwischen Sende- und Empfangsmodul durch zeitliche Überlappung von Speicherzugriffen mit der Busübertragungsphase.

Schottky-Barrier-Dioden vereinen die guten Eigenschaften von Germanium- und Silizium-Dioden.

Silizium-Dioden decken mit ihrer Sperrspannung einen grossen Bereich ab; die Schleusenspannung beträgt etwa 0,7 V; die Sperrverzögerungszeit liegt bei mittleren Werten. Germanium-Dioden sind etwas teurer als Silizium-Dioden; ihr Sperrspannungsbereich ist nicht so ausgedehnt und die Sperrverzögerungszeiten sind relativ gross. Ihre Schleusenspannung liegt jedoch bei 0,2 V. Unsere neuen Schottky-Barrier-Dioden vereinen die guten Eigenschaften von Silizium- und Germanium-Dioden. Sie zeichen sich besonders aus durch ihren einfachen Aufbau, ihre niedrige Durchlassspannung und ihre kurze Sperrverzögerungszeit.

Phasenreglung mit Mikroprozessor– das "look back"-System

Die Wirksamkeit einer analogen 3-Phasen-Regelschaltung kann durch Abweichungen in der Phasenlage stark verschlechtert werden. Benutzt man jedoch zur Überwachung der Phasenlage der 3-phasigen Versorgungsspannung einen Mikroprozessor, dann lässt sich das Problem mit dem beschriebenen "look back"-System bewältigen, welches darüber hinaus noch weitere Vorteile bietet. Obgleich für eine reine Phasenreglung entwickelt, lassen sich die Grundprinzipien dieses Systems auch für Wechselstromregelungen und für 3-Phasen-Brückenschaltungen anwenden.

Das ppm-Management, ein Werkzeug zur Verbesserung der Qualität integrierter Schaltungen

Das Kürzel ppm – als part per million – steht hier für ein Managementsystem der Qualitätsverbesserung, wobei Qualitätsziele für integrierte Schaltungen gesetzt werden und der IC-Hersteller sich verpflichtet, diese Ziele in Zusammenarbeit mit dem Gerätehersteller, der die Bauelemente einsetzt, in vorgegebener Weise zu erreichen. Qualitätsangaben in ppm beschreiben die während und nach der Gerätefertigung beobachtete Qualität der Bauelemente.

Kapazitäts-Einfachdiode für AM-Autoradios

Zur Abstimmung der im AM-Teil elektronisch abgestimmter Rundfunkempfänger häufig verwendeten drei Resonanzkreise ist der Einsatz von drei Kapazitätsdioden erforderlich. Die Fertigung derartiger Dioden als Mehrfacheinheiten ist im allgemeinen teuer und schränkt die Freiheit beim Schaltungsaufbau ein. Dieser Beitrag beschreibt die Kapazitätsdiode BB112, die sich mit einem Abstimmspannungsbereich von 1 V bis 9 V optimal für den Einsatz in Autoradios eignet. Sie wird in Dreiersätzen aus exakt übereinstimmenden Dioden geliefert.

Oszillatoren mit dielektrischem Resonator – neue Mikrowellen-Signalquellen

Oszillatoren mit dielektrischem Resonator stellen Mikrowellen-Signalquellen dar, deren Stabilität mit Hilfe eines keramischen Resonators erreicht wird. Sie sind leicht, preiswert und in hohem Masse kompatibel zu modernen integrierten Mikrowellenschaltungen. Diese Oszillatoren bilden für viele Anwendungen – z.B. digitale Nachrichtenübertragung, Satellitenfernsehen, Radarbaken, Doppler-Transponder – attraktive Alternativen zu Kristalloszillatoren und Oszillatoren mit Hohlraumresonator. Bei dem gebräuchlichen Frequenzbereich von unterhalb 4 GHz bis etwa 16 GHz (und möglicher Erweiterung in Zukunft) erscheint es sicher, für Oszillatoren mit dielektrischen Resonator wachsende Anwendungsbereiche als kostengünstige, stabile Mikrowellen-Signalquellen gewinnen zu können.

Steuer-IC für FIFO-Puffer

Ein neuer LSI-Steuer-IC organisiert RAM-Schaltungen zu FIFO-Registern (FIFO = First In First Out) mit einer Tiefe von bis zu 4 K Worten beliebiger Länge. Die Datenrate kann 8 MHz überschreiten; sie wird nicht durch die bei FIFO-Schaltungen auftretenden "Durchfall"-Verzögerungen begrenzt. Eine interne Arbitrationslogik löst Lese-/Schreib-Konflikte auf der Basis "wer zuerst kommt, wird zuerst bedient". Statussignale indizieren, ob die Register voll, halbvoll oder leer sind.

Wärmebild-Detektoren

Obgleich die Erfordernis der Kryostat-Kühlung weiterbestehen wird, versprechen jüngste Entwicklungen von Infrarot-Detektoren erhebliche Vereinfachungen hinsichtlich der optischen und der Signalverarbeitungs-Systeme, die mit Wärmebild-Detektoren verbunden sind. Fotoleitende Elemente, bei denen die früher in seriell abgetasteten Anordnungen notwendigen Verzögerungs- und Integrationsschaltungen überflüssig sind, sind bereits vorhanden. Starrende Mosaike, bei denen auch die optische Abtastung entfällt, befinden sich im fortgeschrittenen Entwicklungsstand.

Bus extensible pour le traitement réparti

Un bus de microprocesseur, basé sur le concept du traitement réparti, offre la possibilité de porter la capacité des systèmes de 16 à 32 bits, sans imposer de fortes exigences à une unité centrale de traitement. Les données peuvent être transférées entre des modules raccordés au bus, à la cadence de 24 Mbytes/s, et l'information de contrôle asynchrone peut être acheminée conformément au degré de priorité. Des modificateurs d'adresse établissent la distinction entre les divers types de transfert et, d'autre part, un dispositif spécial assure l'acheminement rapide des messages entre le module producteur et le module utilisateur par chevauchement des accès mémoire et de la période de transfert bus.

Des diodes Schottky combinant les avantages du silicium et du germanium

Parmi les caractéristiques des diodes au silicium, citons: caractéristiques en inverse très diverses, coude de chute en tension en direct voisin de 700 mV, temps de recouvrement inverse modéré. Quant aux diodes germanium, plus coûteuses, seul le coude de chute de tension 200 mV présente un interêt parmi les caractéristiques énumérées ci dessus. Nos diodes Schottky, grâce à leur construction simple, combinent faible chute de tension et temps de recouvrement inverse très court.

Système en boucle pour contrôleur de phase à base de microprocesseur

Les performances des contrôleurs de phase analogiques triphasés peuvent être dégradées considérablement par un déséquilibre de phase. En utilisant un microprocesseur pour contrôler l'équilibre de l'alimentation triphasée, le système décrit résout ce problème dans une large mesure et apporte plusieurs avantages supplémentaires. Bien qu'il ait été spécifiquement conçu pour un contrôleur de phase à contrôle total, les principes essentiels de fonctionnement du système en boucle sont applicables à tous les types de contrôleurs à courant alternatif ou de ponts triphasés.

Gestion PPM - un outil pour améliorer la qualité des circuits intégrés

Le système de gestion PPM (parties par million) est une méthode d'amélioration de la qualité dans laquelle des objectifs sont établis, après quoi le fabricant de circuits intégrés reçoit mission d'améliorer la qualité du produit en coopération avec l'équipementier qui utilisera ce produit. L'expression PPM se rapporte à la qualité réelle du produit telle que constatée par l'équipementier sur sa chaîne de montage et ultérieurement.

Diode unique à capacité variable pour autoradios a.m.

Les premières diodes à capacité variable a.m. étaient présentées sous forme de triplets contenus dans des boîtiers à 4 ou 5 connexions. Le triplet étant monolithique, les trois circuits résonants se côtoyant, cette disposition faisait obstacle à l'implantation rationnelle des composants. De plus, le rendement d'appariement des trois diodes présenté sur le cristal étant médiocre, les dispositifs restaient coûteux. Cet article décrit des diodes à capacité variable monojonction type BB112 appariées avec précision trois par trois.

Oscillateurs à résonateur diélectrique - une nouvelle source de signal pour hyperfréquences.

Les oscillateurs à résonateur diélectrique sont des oscillateurs pour hyperfréquences stabilisés par un résonateur céramique. Ce sont des composants légers, peu coûteux et très compatibles avec les circuits intégrés modernes pour hyperfréquences. En outre, dans de nombreuses applications - comme par exemple les télécommunications numériques, la télévision par satellite, les balises radar et les émetteurs-récepteurs à variation de fréquence (Doppler) - ils remplacent avantageusement les oscillateurs classiques à cristal et les oscillateurs stabilisés par cavité résonante. Avec une plage de fréquence normale s'étendant depuis moins de 4 GHz jusqu'aux environs de 16 GHz, et sachant que cette plage a toutes chances de se trouver considérablement élargie à l'avenir, les oscillateurs à résonateur électrique vont incontestablement connaître des applications plus nombreuses en tant que sources de signal pour hyperfréquences, avec des avantages en matière de stabilité et de prix.

Circuit intégré contrôleur de FIFO

Avec le 8X60 des blocs FIFO (First In First Out) peuvent être aisément conçus à partir de RAM standard de grande capacité pour la réalisation de système compacts et économiques. Ce circuit permet la réalisation et le contrôle de blocs FIFO de profondeur 64, 256, 1024 ou 4096 mots de longueur définie par l'utilisateur. Il est réalisé en technologie ISL, compatible TTL, qui permet un fonctionnement à grande vitesse et à faible consommation.

Détecteurs pour présentation visuelle thermique

Malgré les contraintes apportées par leur refroidissement cryogénique, de récents développements intervenus dans les détecteurs à infrarouges semblent devoir simplifier considérablement les systèmes optiques et de traitement des signaux des dispositifs de visualisation par voie thermique. Des éléments photoconducteurs sont déjà disponibles et permettent d'éliminer les circuits de retard et d'intégration que nécessitaient antérieurement les dispositifs à balayage série. Des dispositifs en mosaïque se trouvent maintenant à un stade de développement avancé et permettront aussi d'éliminer le balayage optique.

Bus de microprocesador extensible para procesado distribuido

Un bus de microprocesador basado en el concepto de procesado distribuido permite extender sistemas de 16 a 32 bits sin depender mucho de una CPU. Los datos pueden transferirse entre los módulos conectados al bus a 24 Mbytes/s, con posibilidad de transferir información de control asincrónica con arreglo a la prioridad. Los diferentes tipos de transferencia se distinguen por modificadores de dirección y una facilidad especial posibilita la transferencia rápida de mensajes entre los módulos productores y consumidores por solapamiento de los accesos a memoria y del periodo de transferencia del bus.

Diodos de barrera Schottky combinando lo mejor del germanio y del silicio

Los diodos de silicio poseen una simpla gama de características inversas, un voltaje de codo de polarización directa de 700 mV y un tiempo de recuperación inversa moderado. Los diodos de germanio son más costosos que los tipos de silicio, la gama disponible no es tan grande y su tiempo de recuperación es largo. Tienen en cambio un voltaje de codo de polarización directa de unos 200 mV. Nuestra nueva serie de diodos de barrera Schottky combinan las características favorables de los diodos de silicio y de germanio, por razón de su construcción sencilla, su bajo voltaje directo y su corto tiempo de recuperación inversa.

Controlador de fase a microprocesador – sistema retrovisor ("look-back")

El funcionamiento de los controladores de fase analógicos a tres fases puede verse perturbado gravemente por un desequilibrio de fase. Empleando un microprocesador para verificar la simetría de la alimentación trifásica, el sistema descrito vence dicho problema y ofrece además varias ventajas complementarias. Aunque el sistema se ha desarrollado específicamente para un controlador de fase del tipo de control completo, sus principios básicos de funcionamiento son aplicables a todos los tipos de controlador de c.a. o puente trifásico.

Control PPM – auxiliar para mejorar la calidad de los CI

El PPM – partes por millión – es un sistema de mejoramiento de calidad que fija ciertos objetivos y que obliga al fabricante de CI a perfeccionar la calidad de su producto en cooperación con el fabricante de los equipos en que se beneficia dicho producto. PPM refiere a la calidad efectiva tal como el fabricante de equipos la experimenta en su línea de montaje y con posterioridad a la producción.

Diodo de capacitancia variable discreto para autorradios de m.a.

Para sintonizar los tres circuitos resonantes usados con frecuencia en la sección de m.a. de radios de sintonía electrónica se precisan tres diodos de capacitancia variable. Si tales diodos se manufacturan como unidades multiples tienden a ser costosos y dificultan la disposición de los componentes. El artículo describe los diodos de capacitancia variable BB112 con margen de voltaja de sintonía de 1 V a 9 V (ideal para autorradios), los cuales se proveen en conjuntos exactamente seleccionados de tres ejemplares.

Osciladores a resonador dieléctrico – una nueva fuente de señales de microonda

Los osciladores a resonador dieléctrico son osciladores de microonda estabilizados por un resonador cerámico. De peso ligero y de bajo costo, son perfectamente compatibles con los modernos circuitos integrados de microonda. En muchas aplicaciones, como las telecomunicaciones digitales, la televisión por satélite, los faros de radar y los transpondores doppler, constituyen una alternativa atractiva de los osciladores a cristal o de cavidad convencionales. Con un margen de frecuencias que se extiende desde menos de 4 GHz hasta unos 16 GHz (con grandes probabilidades de ser extendida considerablemente en el futuro) los osciladores a resonador dieléctrico seguramente encontrarán cada vez más aplicación como fuente de microondas estable y económica.

CI controlador para memorias intermedias FIFO

Un CI controlador en técnica LSI arregla chips RAM formando registradores FIFO de hasta 4K palabras de cualquier longitud. La velocidad de datos puede superar los 8 MHz sin sufrir estorbos por los retardos de "fall-through" inherentes a los chips FIFO. Una lógica de arbitraje interna evita los conflictos de escritura-lectura, aplicando el principio de primero a llegar, primero a tratar. Mediante señales de estado se indica si el registro está lleno, semilleno o vacío.

Detectores para termoimaginación

Siquiera sea poco probable que se pueda prescindir de la refrigeración criogénica, los recientes desarrollos en materia de detectores infrarrojos prometen una simplificación considerable de los sistemas ópticos y de procesado de señales asociados a los termoimaginadores. Ya son realidad los elementos fotoconductores que han hecho supérfluos los circuitoa de retardo a integración que se requerían en los exploradores en serie, y con los dispositivos de mosaico actualmente en fase de desarrollo avanzada también quedará eliminada la exploración óptica.

Authors

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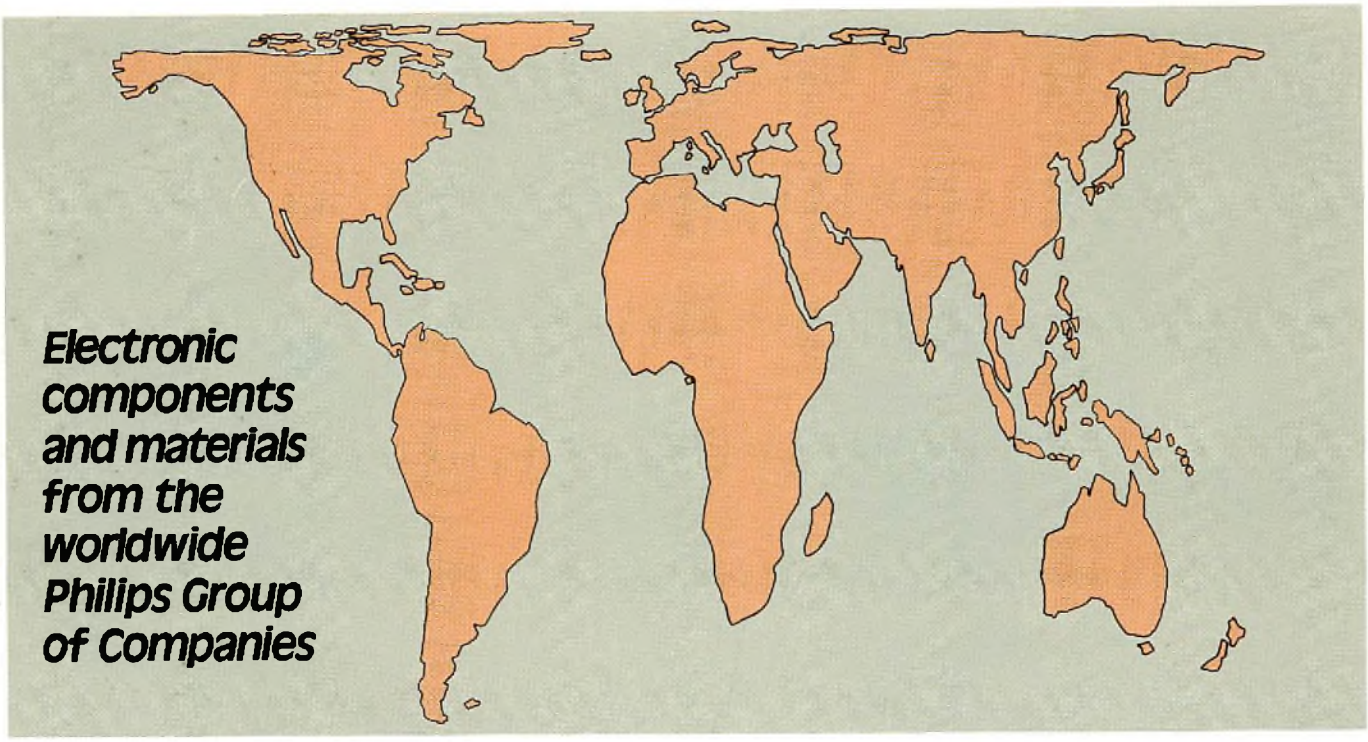

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