

Electronic components & applications

Vol. 5, No1
November 1982



Electronic components & applications

Volume 5, No. 1

November 1982

Contents

Editors

William E. Martin
Michael J. Prescott (Mullard)

Design and production

Cees J. M. Gladdines
Bernard W. van Reenen
Jacob Romeijn
Michael J. Rose

Design consultant

Theo Kentie



Lightning, here striking the shore of Lake Lugano, is but one of the many hazards threatening the intricate telecommunications networks that knit today's global village together. While advances in solid-state have added greatly to what those networks can do, they have also increased their vulnerability. Safeguards that served in the days of electromechanical exchanges and rotary-dial, carbon-microphone subscriber sets are no longer adequate; the ICs in modern telephone systems are far more sensitive to excess voltages and currents. The article beginning on page 2 offers some useful suggestions about how to protect them against not only lightning-induced transients but other common hazards as well.

Non-linear resistors for protection of telephone equipment <i>J. P. Coulmance and J. C. van Loon</i>	2
D.C. controlled volume and tone control ICs <i>W. Eckert</i>	7
Small area networks for serial data transfer <i>A. Goldberger, C. Kaplinski and A. P. M. Moelands</i>	15
High-speed CMOS <i>R. Croes</i>	23
Long-term reliability of linear bipolar ICs <i>F. W. Ohlenroth</i>	33
Semiconductor laser with collimating optics <i>L. J. van Ruyven</i>	42
Dual-gate MOSFETs for u.h.f. and v.h.f. applications <i>J. Houthoff and T. H. Uittenbogaard</i>	46
One IC and a SAW filter in a high-performance vision i.f. channel <i>P. J. M. Sijbers and J. Zeelen</i>	56
Abstracts	62
Authors	64

Voltage-dependent resistors can guard solid-state circuits in telephone equipment against overvoltage and overcurrent hazards due to lightning-induced transients. A new composite device combining voltage and temperature dependent resistors can extend the protection to cover accidental contact with the mains.

Non-linear resistors for protection of telephone equipment

J. P. COULMANCE and J. C. F. VAN LOON

The rapid adoption of solid-state electronics in telephony has radically altered the protection requirements for both exchange and subscriber equipment. Traditional safeguards dating from the era of electromechanical exchanges and rotary-dial, carbon-microphone subscriber sets are no longer adequate. Safety thresholds are much lower now and the time in which safeguards must take effect much shorter.

The hazards to be guarded against – overvoltage, overcurrent, and overpower – may have any of the following causes.

Lightning, which may induce fast-rising, high-amplitude voltage transients on the line. Nearby electric-railway conductors in which sudden large current variations occur frequently may have a similar effect.

High-tension lines which often run close to unshielded telephone lines. An overload or short circuit on a high-tension line can induce an over-voltage on a telephone line that may last several hundred milliseconds before the circuit breaker in the high-tension line operates.

Contact with outside voltages, which is unusual but does happen; the likeliest voltage is the mains, 115 V to 250 V r.m.s., depending on the country. The maximum current due to such a contact, and its duration, are unpredictable.

Short circuits between wires, which may be due to incorrect wiring or accidental contact with tools during maintenance or testing. The resulting voltage on any wire may be

- the battery voltage (36 V, 48 V or 60 V in Europe)
- the ringing voltage (which can be as high as the battery voltage plus 100 V r.m.s.)

- the booster voltage for long lines (from 48 V to 104 V, depending on the country).

The voltage between the two wires of the line can be any combination of these. Often the current due to the battery or ringing voltage is not limited in any way except by the resistance of the line circuit.

Short circuits between wires are frequent and can last several hours.

Protection standards differ from country to country and, in general, do not distinguish between hazards other than lightning-induced transients and contact with outside voltages. The various national standards are embodied in specified tests.

TESTS

Lightning induced transients

Figure 1 is a generalised diagram of the circuit universally specified for testing the vulnerability of both exchange and

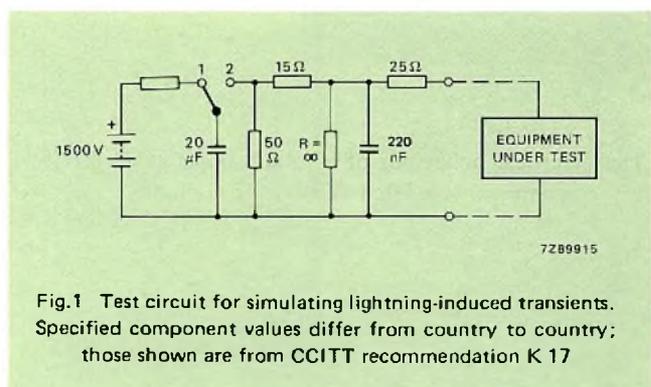


Fig.1 Test circuit for simulating lightning-induced transients. Specified component values differ from country to country; those shown are from CCITT recommendation K 17

subscriber equipment to lightning-induced transients. The battery voltage and resistance and capacitance values differ from country to country; those shown in the figure are the recommendations of CCITT.

The capacitor C is first charged to the battery voltage (switch position 1), then discharged (switch position 2) via the test circuit and the equipment under test. The test is repeated several times at both polarities. Figure 2 shows the shape and specified measuring parameters of the resulting current waveform. The peak value of I and the values of t_r and t_d depend on the characteristics of the equipment under test and whatever protection it incorporates. The permissible effect of the test on the equipment is differently specified in different countries, but in general no damage is permitted.

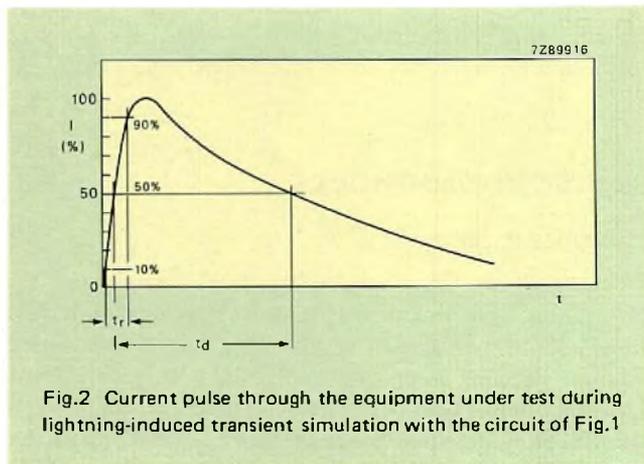


Fig.2 Current pulse through the equipment under test during lightning-induced transient simulation with the circuit of Fig.1

Outside voltages

Standards for vulnerability to outside voltages differ widely from country to country. Most national authorities specify tests with both differential and common-mode voltages, but apart from that there is little agreement. Specified test durations vary from 1 second to 15 minutes, and test voltages from 60 V to 2000 V. Some countries specify a.c., others d.c., and others a.c. plus d.c.

PROTECTION WITH NON-LINEAR RESISTORS

Most protection requirements in both exchange and subscriber equipment can be met by non-linear resistors, particularly voltage-dependent ones, in some cases augmented by diodes.

The electrical behaviour of a voltage-dependent resistor (VDR) is comparable to that of two zener diodes back-to-back. When the VDR is conducting, the voltage across it remains nearly constant over several orders of magnitude change in current. Thus, when a VDR is exposed to a high-voltage transient, its impedance changes from a near open-circuit to a few ohms, clamping the transient to a safe level within a few nanoseconds.

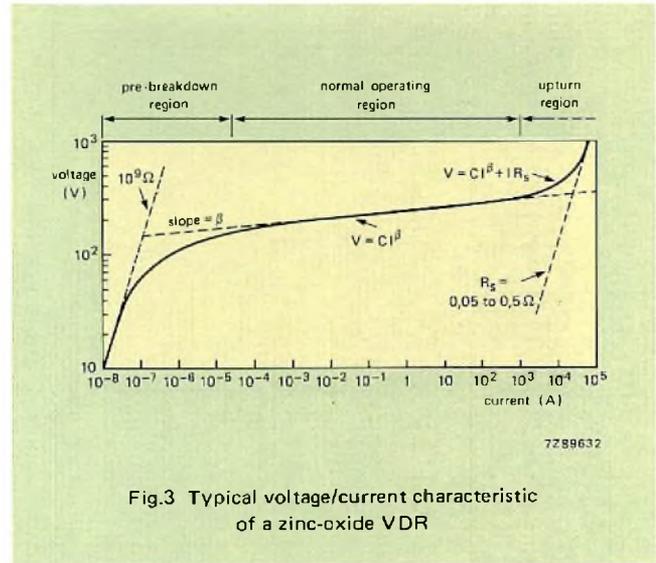


Fig.3 Typical voltage/current characteristic of a zinc-oxide VDR

The voltage/current characteristic of a VDR in the breakdown region (Fig.3) follows the law

$$V = CI^\beta + IR_s$$

where C, which determines the voltage range at small currents, depends on the resistor construction; β , the non-linearity index, depends on the resistor material; and R_s is a small, non-voltage-dependent component of resistance.

The best VDRs for telephone protection are made of zinc oxide, for which β is in the range 0.02 to 0.035. This means that if the current through a zinc-oxide VDR increases tenfold in the part of the characteristic where the effect of β predominates, the voltage across it will increase by a factor of only 1.05 to 1.08 (see Ref.).

A composite non-linear resistor that is especially useful for protecting both exchange and subscriber equipment against large differential voltages is the new PVP module, which consists of a VDR sandwiched between two PTC (positive temperature coefficient) thermistors (Fig.4). The VDR limits the voltage during transients and the thermistors limit the current due to a continuous differential voltage (Fig.5, 6 and 7). The thermal coupling between the VDR and the two thermistors is essential to the operation of the device. Characteristics of two types of PVP module are listed in Table 1.

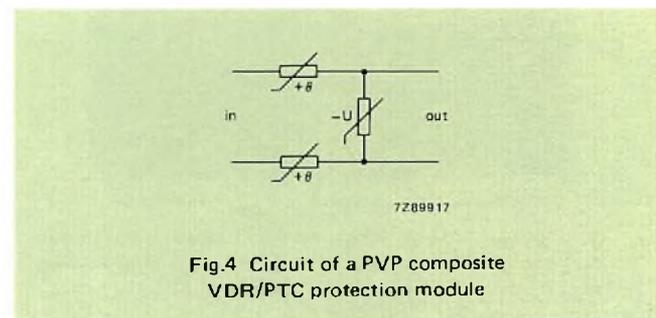
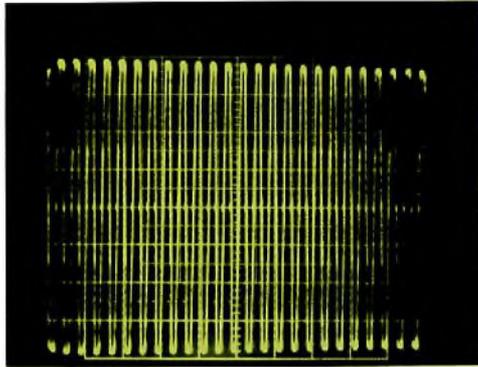
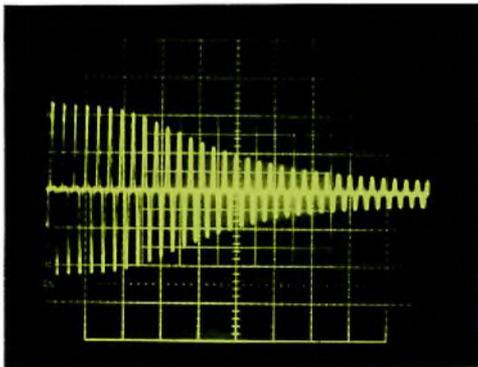


Fig.4 Circuit of a PVP composite VDR/PTC protection module



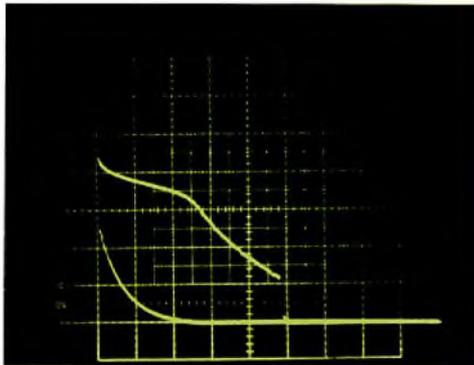
V = 50 V/div.; T = 75 mS/div.

Fig.5 Voltage across the VDR of a PVP module when 200 V a.c. is applied to the input



I = 2 A/div.; T = 75 mS/div.

Fig.6 Current through one of the PTC thermistors of a PVP module when 200 V a.c. is applied to the input



V = 50 V/div.; I = 10 A/div.; T = 75 mS/div.

Fig.7 Current through (lower trace) and voltage across (upper trace) the VDR of a PVP module during lightning-induced transient simulation

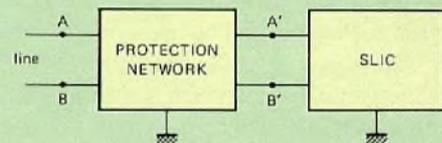
TABLE I
Characteristics of PVP protection modules

PVP type number	2322 599 91001	2322 599 91002
VDR voltage		
minimum at 1 mA	135 V	180 V
maximum at 25 A	250 V	310 V
PTC continuous maximum output current at T _{amb} = 70 °C	60 mA	60 mA
response time at I = 1.5 A	< 3 s	< 3 s
PTC current after switching at 220 V r.m.s., typical	12 mA	12 mA

PROTECTION NETWORKS

Exchange equipment

The part of an electronic exchange that determines the protection requirement is the subscriber-loop interface circuit (SLIC). This must be protected against overvoltage without affecting its performance under normal conditions. The overvoltages that occur may be differential (between A and B, Fig.8), common mode (between A or B and earth), or a combination of both.



7289918

Fig.8 A subscriber loop interface circuit (SLIC) must be protected against both differential and common-mode excess voltages

When no overvoltage is present, the balance between the two lines should be preserved so that voice signals at points A and B are transferred as equally as possible to points A' and B', undegraded by noise, crosstalk or distortion. The differential ringing voltage (70 V or 90 V r.m.s.) should also be transferred without clipping. When an overvoltage does occur, the protection network must ensure that the voltages at points A' and B' do not exceed the maximum ratings of the SLIC.

TABLE 2
Characteristics of the VDRs used in the network in Fig.9
 (see text for protection voltages)

	type number	small current operation		transient operation	
		V_{\min}	at I	V_{\max}	at I
VDR1	2322 594 90011	150 V	1 mA	300 V	50 A
VDR2	2322 594 90009	100 V	1 mA	230 V	50 A
VDR3	2322 594 90009	100 V	1 mA	230 V	50 A
VDR4	8222 298 12194*	133 V	1 mA	190 V	1.5 A
VDR5	8222 298 12195*	41 V	1 mA	90 V	7 A
VDR6	8222 298 12196*	92 V	1 mA	140 V	4.5 A

* Development type numbers.

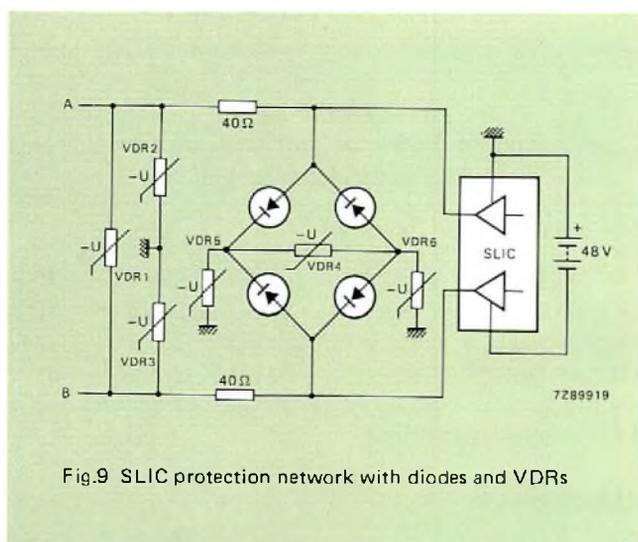


Fig.9 SLIC protection network with diodes and VDRs

Figure 9 shows a protection network for a SLIC having permissible overvoltages at its line terminals up to +90 V and down to -140 V, but with no more than 190 V differential voltage. Table 2 lists the type numbers and characteristics of the VDRs used.

- VDR1 provides a first line of protection against differential overvoltage between A and B, limiting it to 300 V at 50 A.
- VDR2 and VDR3 protect against common-mode currents up to 50 A and limit the voltage between A or B and earth to 230 V.
- VDR4, VDR5, and VDR6 provide a second line of protection; VDR4 limits the differential voltage between the terminals of the SLIC to 185 V, and VDR5 and VDR6 limit the voltage between the terminals and earth to 85 V and 133 V respectively (the difference being the 48 V battery voltage).

The 40 Ω linear resistors must be accurate enough to ensure that the required line balance is maintained.

Figure 10 shows the line current and the voltages across the six VDRs as functions of time, measured with a test circuit as in Fig.1 but with a battery voltage of 2300 V.

The Fig.9 network can be adapted to various SLIC configurations and other VDRs are available to adapt it to other voltages. If the SLIC also has to be protected against the risk of mains voltage across the lines, a PVP module can be added.

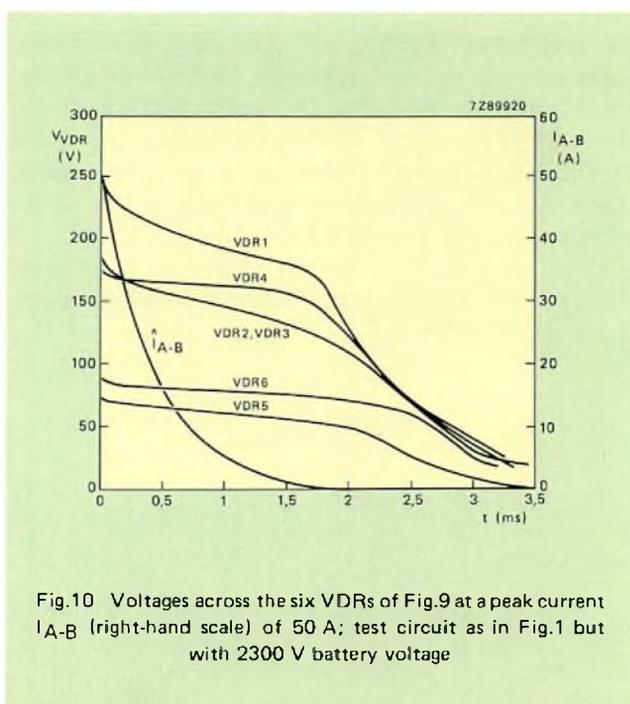


Fig.10 Voltages across the six VDRs of Fig.9 at a peak current I_{A-B} (right-hand scale) of 50 A; test circuit as in Fig.1 but with 2300 V battery voltage

Subscriber sets

To begin with, a subscriber set needs to be guarded against wrong line-voltage polarity. A plain silicon-diode bridge will usually do, but if the forward voltage drop has to be especially low, Schottky diodes (e.g. BAT85) or transistors are preferable.

Overvoltage and overcurrent protection requirements differ according to whether the set has

- dual-tone multi-frequency (DTMF) dialling
- interrupted current-loop (pulse) dialling or register recall (flash)
- an electronic ringer.

Sets with electronic DTMF dialling have to be protected against voltages that exceed the breakdown voltage of the ICs used, 12 V to 15 V. VDRs for that voltage range are not yet available but zener diodes with good transient suppression characteristics are.

For sets with interrupted current-loop dialling or register recall, two fundamental constraints are that the protection must not affect the shape of the current pulses and must not conduct at the exchange battery voltage (36 V, 48 V or 60 V). Since the self-inductance of the exchange feeding bridge causes ringing during current interruptions, the threshold at which protection starts to conduct must be high – preferably above 100 V. But, on the other hand, the voltage across it must never exceed the breakdown voltage of the interrupt switch. Bipolar semiconductors and VDRs can both meet these requirements, but in most cases VDRs are cheaper. Table 3 lists four VDR types designed for the purpose; Fig.11 shows the current and voltage characteristics of one of them.

Specifications regarding the protection of electronic ringers are more rigorous; whereas a dialling circuit is connected to the line only when the handset is off the cradle, the ringer is connected all the rest of the time. Some authorities also require ringers to be protected against contact with the mains. Here again, zener diodes are indicated; a good choice is the BZW03 series.

Where the applicable standards require a subscriber set to be protected against damage due to differential voltages of, say, 200 V, a PVP module can be used.

ACKNOWLEDGEMENT

The authors are grateful to A.J.Nijman and F.A.C.M. Schoofs of Philips' Research Laboratory, Eindhoven, for their valuable contribution to the work on which this article is based.

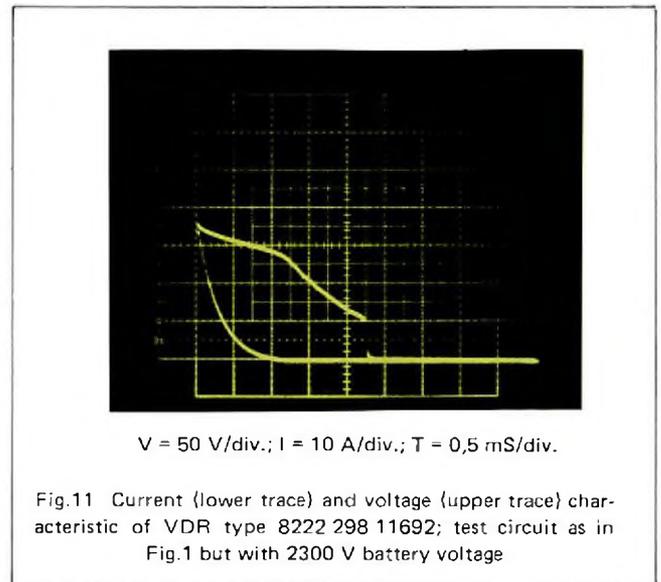


TABLE 3
Characteristics of VDRs for protection of subscriber sets with current-loop interruption

type number	V_{\min}	at	I	V_{\max}	at	I
2322 595 90001	130 V		1 mA	285 V		20 A
2322 593 90001	90 V		1 mA	200 V		22 A
2322 594 90005	103 V		0.1 mA	200 V		22 A
8222 298 11692*	105 V		0.1 mA	200 V		35 A

* Development type number.

REFERENCE

"Zinc oxide voltage-dependent resistors", Philips Technical Publication 046, March 1982, ordering code 9398 021 70011, Mullard Technical Publication M82-0044.

The TDA1074A contains four d.c.-controlled electronic potentiometers which facilitate the control of audio functions such as volume, loudness, tone and balance. Since each potentiometer incorporates an op-amp at its output, the desired transfer function is determined by a feedback network so that THD is minimal. The d.c. control allows increased positioning flexibility for the control element and also facilitates remote control.

DC-controlled volume and tone control ICs

W. ECKERT

Passive volume and tone control circuits in audio equipment require few components but suffer from several disadvantages. They are adjusted by potentiometers which, in stereo equipment, must be tandem types. These are bulky, expensive and, since they must be positioned on the front panel, they are usually connected to the circuitry by screened wires. This restricts styling flexibility and can cause spurious signal pickup, feedback and degradation of stereo channel separation. Although passive tone controls can provide frequency-dependent boost as well as cut, they are in fact only frequency-selective a.c. voltage dividers. Their insertion loss is therefore at least equal to the required amount of bass or treble boost (usually 20 dB), so a recovery amplifier must be used to restore the signal level. This can increase THD and degrade the signal-to-noise ratio. Another severe disadvantage of passive controls is that they are not compatible with remote-control systems.

Active volume and tone controls using operational amplifiers have many advantages over passive controls. They can provide adjustable linear or frequency-dependent amplification or attenuation which is inherently symmetrical about the 0 dB axis and, since the gain determining components are in the negative feedback loop of the gain block, THD is low. They still, however, require potentiometers in the signal path.

We have therefore developed a dual tandem potentiometer integrated circuit TDA1074A which consists of two ganged pairs of electronic potentiometers with the eight inputs connected via impedance converters, and the four outputs driving individual operational amplifiers. The setting of each electronic potentiometer pair is controlled by an individual d.c. control voltage. The potentiometers operate by current division between the arms of cross-coupled long-tailed pairs. The current division factor is determined by the level and polarity of the d.c. control

voltage with respect to an externally available reference level of half the supply voltage. Since the electronic potentiometers are adjusted by a d.c. control voltage, each pair can be controlled by a single linear potentiometer which can be located in any position dictated by the equipment styling. The d.c. control also facilitates remote control via D-to-A converters in systems such as the Radio Tuning System (RTS) described in Ref.1.

Versatility and high performance are strong features of the TDA1074A. Formerly, two or more dedicated ICs were needed for bass/treble and volume/loudness control. Now, since the input and feedback impedances around the op-amp gain blocks are external, the TDA1074A performs all these functions, and can also be used as a low-level fader to distribute the sound between the front and rear loudspeakers in car audio installations.

Outstanding features determining the high performance of the TDA1074A are:

- high-impedance inputs to both 'ends' of each electronic potentiometer
- ganged potentiometers track within 0.5 dB
- electronic rejection of supply ripple
- internally generated reference level available externally so that the control voltage can be made to swing positively and negatively around a well-defined 0 V level
- the op-amps have push-pull outputs for wide voltage swing and low current consumption
- the op-amp outputs are current limited to provide output short-circuit protection
- although designed to operate from a 20 V supply (giving a maximum input and output signal level of 6 V), the TDA1074A can work from a supply as low as 7.5 V with reduced input and output signal levels.

TABLE 1
Typical brief data for the TDA1074A

supply voltage V_p	20	V
supply current I_p	20	mA
maximum input voltage $V_{i\text{ rms}}$	6	V
maximum output voltage $V_{o\text{ rms}}$	6	V
total harmonic distortion d_{tot}	0.05	%
unweighted output noise voltage $V_{\text{noise rms}}$ of one potentiometer operating at unity gain, $V_c = V_{\text{ref}}$	50	μV
control range	110	dB
channel separation	80	dB
100 Hz ripple rejection	46	dB
tracking of ganged potentiometers	± 0.5	dB

(all data valid for $V_p = 20\text{ V}$)

ELECTRONIC POTENTIOMETER PRINCIPLES

Figure 1 shows the basic principle of current division with a long-tailed pair. Transistors TR₁ and TR₂ are connected as a long-tailed pair differential amplifier in which emitter current I is controlled by current source TR₃ driven by a constant voltage V_{b3} . The sum of the emitter currents of TR₁ and TR₂ is equal to the collector current (I) of TR₃ and is divided between TR₁ and TR₂ in proportion to the voltage difference between their bases (control voltage $V_c - V_{\text{ref}}$). The division ratios δ and $1-\delta$ can be calculated according to the equation in Fig.1 but, for convenience, are listed in Table 2.

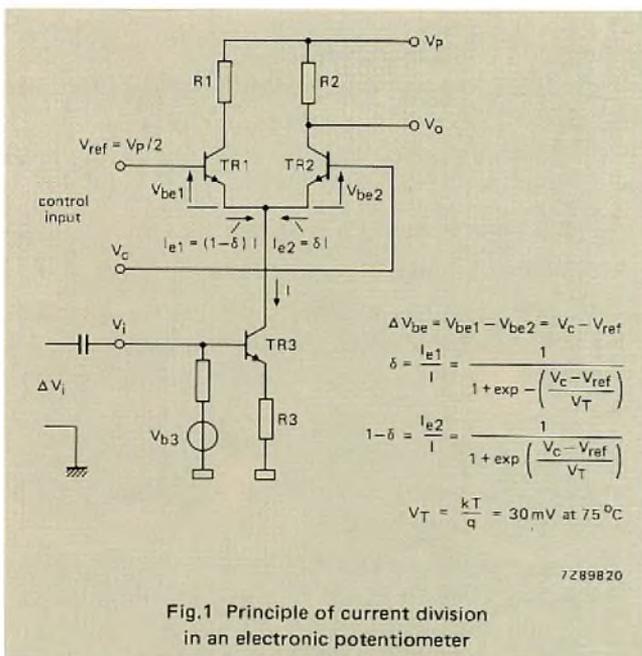


Fig.1 Principle of current division in an electronic potentiometer

TABLE 2
Current division factors based on $kT/q = 30\text{ mV}$ at 75°C

$V_c - V_{\text{ref}}$ (mV)	δ	$1 - \delta$
200	0.999	0.001
175	0.997	0.003
150	0.993	0.007
125	0.985	0.015
100	0.965	0.035
75	0.924	0.076
50	0.841	0.159
25	0.697	0.303
0	0.5	0.5
-25	0.303	0.697
-50	0.159	0.841
-75	0.076	0.924
-100	0.035	0.965
-125	0.015	0.985
-150	0.007	0.993
-175	0.003	0.997
-200	0.001	0.999

If V_{b3} is modulated by an audio-frequency input signal V_i , current I is also modulated and causes an output voltage variation $V_o = \delta I R_2$. The voltage variation across R_1 is $(1-\delta)I R_1$ and does not contribute to the output voltage. The circuit thus acts as an electronic potentiometer in which the amount of signal current flowing through collector load resistor R_2 is a function of δ which is determined by the control voltage between the bases of TR₁ and TR₂ ($V_c - V_{\text{ref}}$). Unfortunately, this circuit cannot be used as a practical potentiometer in the TDA1074A because the d.c. current flowing through R_2 is also dependent on the control voltage $V_c - V_{\text{ref}}$.

ELECTRONIC POTENTIOMETER USED IN THE TDA1074A

One of the four electronic potentiometer circuits in the TDA1074A is shown in Fig.2. Transistors TR₁, TR₂, TR₃ and TR₄ constitute two cross-coupled long-tailed pairs. The direct currents $I_1 = I_2$ are set by equal value emitter resistors R instead of by current sources. Since the sum of the direct currents through the collector resistor of TR₄ is now δI_1 via TR₂ plus $(1-\delta)I_2$ via TR₄, it is now equal to $I_1 = I_2$ and is independent of δ and therefore independent of the control voltage $V_c - V_{\text{ref}}$.

Two audio-frequency input signals V_{i1} and V_{i2} can be injected into the emitters of TR₁/TR₂ and TR₃/TR₄ via impedance converters OP1 and OP2 which provide high impedances at the potentiometer inputs. The a.c. output signal developed across the common collector resistor of

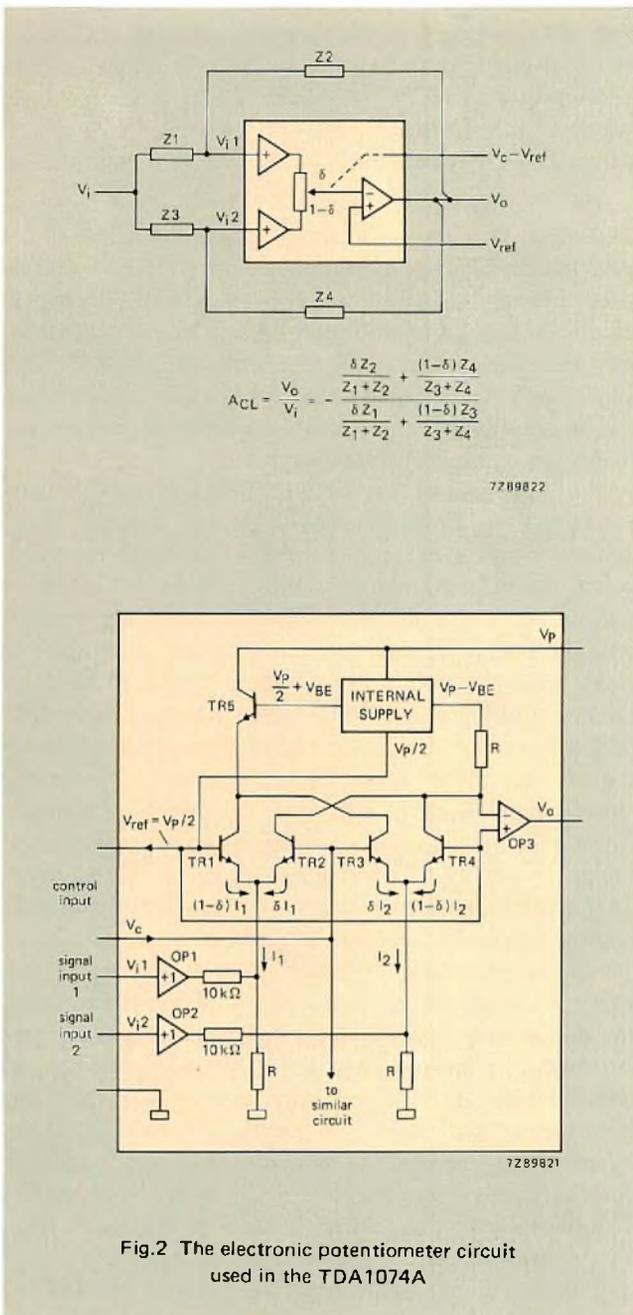


Fig.2 The electronic potentiometer circuit used in the TDA1074A

TR₂ and TR₄ (wiper of the electronic potentiometer) drives the inverting input of op-amp OP₃ which has a maximum open-loop gain of 80 dB.

The bases of TR₁ and TR₄, and the non-inverting input of OP₃ are connected to an internally generated reference voltage of half the supply voltage ($V_{ref} = V_p/2$). The control voltage $V_c - V_{ref}$ (0 to ± 250 mV) thus appears between the bases of each long-tailed pair.

When the control voltage $V_c - V_{ref}$ is +250 mV (δ almost unity, $1-\delta$ negligible), TR₂ and TR₃ fully conduct and input signal V_{i1} is passed to the output via TR₂. Input signal V_{i2} is diverted to V_p via TR₃ and TR₅, and does not contribute to the output.

When the control voltage $V_c - V_{ref}$ is -250 mV, (δ negligible, $1-\delta$ almost unity), TR₁ and TR₄ fully conduct and input signal V_{i2} is passed to the output via TR₄. Input signal V_{i1} is diverted to V_p via TR₁ and TR₅, and does not contribute to the output.

The functional block diagram of this electronic potentiometer/op-amp combination and its closed-loop gain equation are given in Fig.2. In the block diagram, δ is the fraction of V_{i1} which contributes to the output and $1-\delta$ is the fraction of V_{i2} which contributes to the output. It is clear from the closed-loop gain equation that, if $Z_1 = Z_4$ and is less than $Z_2 = Z_3$, the closed loop gain will be unity when δ and $1-\delta$ are equal. With this arrangement, the circuit will amplify the input when $\delta > 1-\delta$ and attenuate it when $1-\delta > \delta$. This is the configuration that is extensively used in the tone and volume control circuits described in the remainder of this article. Figure 3 is the functional block diagram of the TDA1074A.

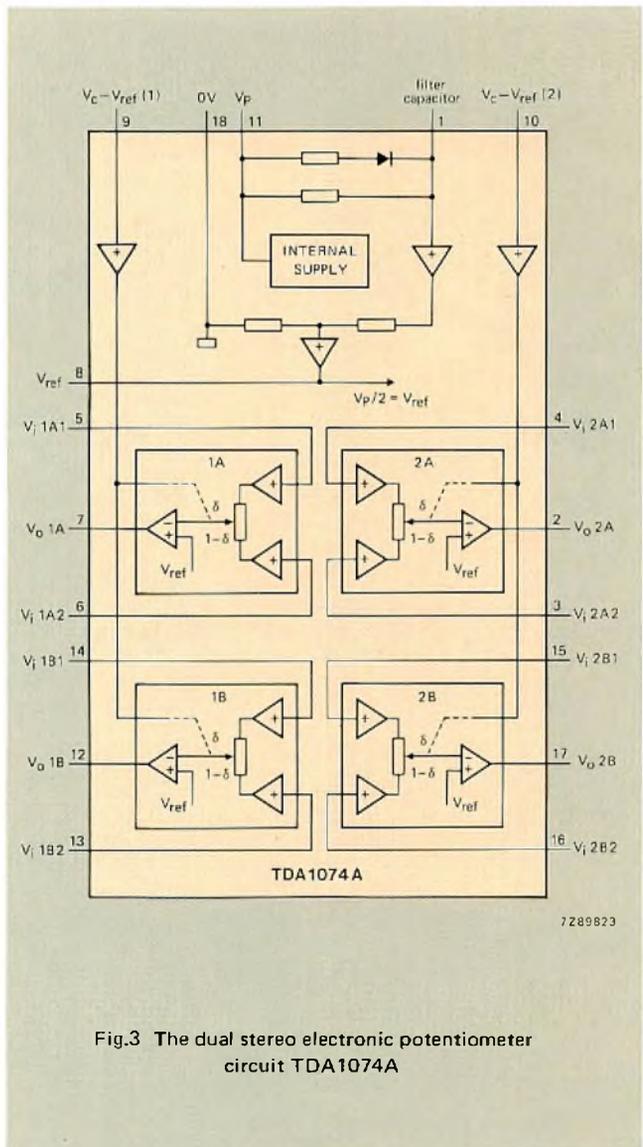


Fig.3 The dual stereo electronic potentiometer circuit TDA1074A

BASIC OP-AMP CIRCUITS FOR CONTROL OF AUDIO VOLUME AND TONE

In an ideal op-amp, the voltage gain and input impedance are infinite, the output is inverted, and the output impedance is zero. Although this ideal cannot be achieved in practice, the very high voltage gain (80 dB), low output impedance (0.5 Ω) and high input impedance (>10 MΩ) of the electronic potentiometer/op-amp combinations in the TDA1074A allow negative feedback to be applied as shown in Fig.4(a) so that only the values of the two resistors determine the closed-loop gain. In Fig.4(a), the current flowing into the high impedance input of the op-amp is

negligible compared to that flowing in R₁ and R₂ and can be discounted so that I₁ = -I₂. The sum of the currents flowing in each of the two resistors is therefore zero; the whole of V_i appears across R₁, and the whole of V_o appears across R₂. The closed loop gain is therefore expressed as:

$$ACL = -V_o/V_i = -(I_2 R_2)/(I_1 R_1) = -R_2/R_1.$$

The circuit in Fig.4(a) contains no reactive elements and so gives frequency independent gain when R₂ > R₁ or attenuation when R₁ > R₂. By referring back to the block diagram of the electronic potentiometer/op-amp in Fig.2, it can be seen that, if Z₁ and Z₂ are replaced by resistors (R₁ < R₂), and Z₃ and Z₄ are replaced by resistors (R₃ > R₄), a continuously variable volume control which can provide amplification or attenuation is obtained.

For tone control, the circuit in Fig.4(a) must be converted into a first-order (20 dB/decade ultimate slope) active network with a corner (±3 dB) frequency one decade below the highest audible frequency for treble control, or one decade above the lowest audible frequency for bass control. This is achieved by simply adding a capacitor in series or parallel with either the input resistor or the feedback resistor. The remainder of Fig.4 illustrates this principle.

The circuit for treble boost is Fig.4(b). C₁ progressively reduces input impedance Z₁ with increasing frequency above corner frequency 1/(2πR₁C₁), thereby amplifying the treble. At more than one octave below the corner frequency, the gain is R₂/R₁ = 0 dB and is independent of frequency. The circuit for treble cut is Fig.4(c). Here C₂ progressively reduces feedback impedance Z₂ with increasing frequency above corner frequency 1/(2πR₂C₂), thereby attenuating the treble. At more than one octave below the corner frequency, the gain is R₂/R₁ = 0 dB and is independent of frequency.

The circuit for bass boost is Fig.4(d). Capacitor C₂ progressively increases feedback impedance Z₂ with decreasing frequency below corner frequency 1/(2πR₂C₂), thereby amplifying the bass. At more than one octave above the corner frequency, the gain is R₂/R₁ = 0 dB and is independent of frequency. The circuit for bass cut is Fig.4(e). Here, C₁ progressively increases input impedance Z₁ at frequencies below corner frequency 1/(2πR₁C₁), thereby attenuating the bass. At more than one octave above the corner frequency, the gain is R₂/R₁ = 0 dB and is independent of frequency.

Referring back to the block diagram of the electronic potentiometer/op-amp in Fig.2, it can be seen that, if Z₁ and Z₂ are replaced by the circuit of Fig.4(b), and Z₃ and Z₄ are replaced by the circuit of Fig.4(c), a continuously variable treble boost/cut control is obtained. Similarly, if the circuits of Fig.4(d) and 4(e) are inserted into the block in Fig.2, a continuously variable bass boost/cut control is obtained. In practice, additional resistors are connected in series with the capacitors (treble control), or in parallel with the capacitors (bass control), to limit the maximum boost and cut to ±20 dB beyond the limits of the audible frequency spectrum.

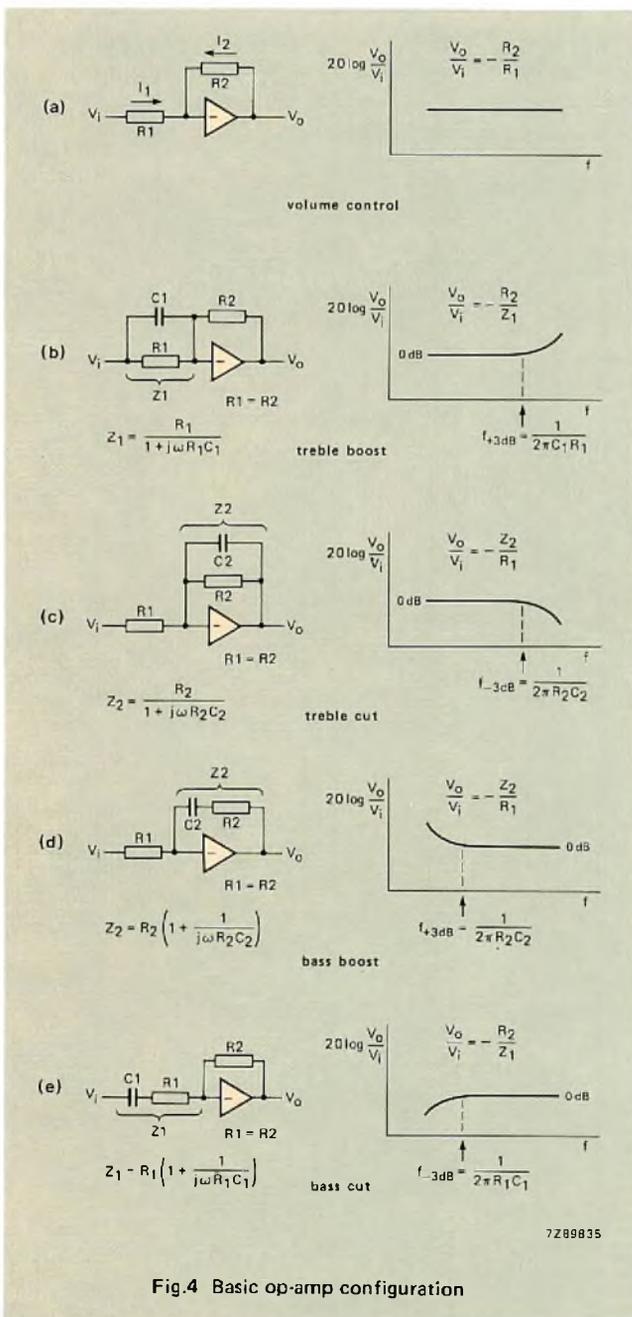


Fig.4 Basic op-amp configuration

PRACTICAL CIRCUITS

Stereo volume/loudness/balance control

Since the TDA1074A contains two ganged pairs of electronic potentiometer/op-amps and the TDA1527 contains

two switches, one of each of these ICs is sufficient to construct a complete stereo volume/loudness/balance control circuit with electronic switching of loudness as shown in Fig.5.

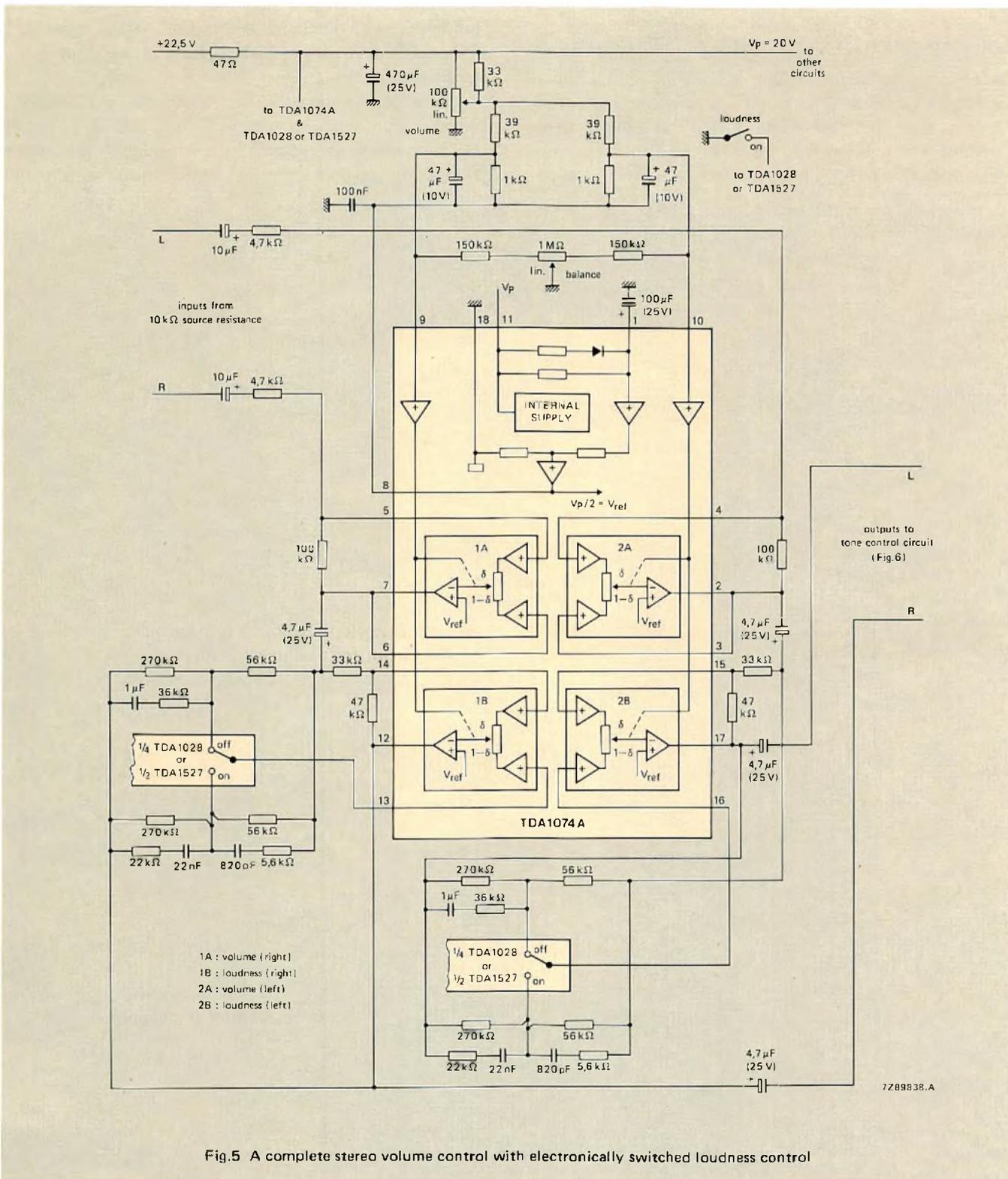


Fig.5 A complete stereo volume control with electronically switched loudness control

Stereo tone control

A single TDA1074A is also sufficient to construct a complete stereo tone control circuit as shown in Fig.6. This circuit provides up to 20 dB bass/treble boost/cut and has unity gain at 1 kHz regardless of the control settings.

Low-level fader for stereo audio installations in cars

In car stereo audio installations with front and rear loudspeakers, a fader can progressively transfer the sound from front to rear (and vice versa), thereby allowing a more agreeable sound balance to be achieved than can be obtained with only a stereo balance control.

A commonly used type of fader is a power potentiometer connected between the power amplifier output and the front and rear loudspeakers (high-level fader). Where high power outputs are required, however, the low level of available supply voltage (12 V) dictates the use of separate low-impedance output amplifiers mounted close to the loudspeakers to minimise loudspeaker wiring losses. It is then necessary to use a low-level fader at the inputs to the power amplifiers.

The circuit of a low-level fader using half a TDA1074A for one stereo channel is given in Fig.7. It consists of two of the four electronic potentiometer/op-amp blocks of the TDA1074A operated by the same control voltage and

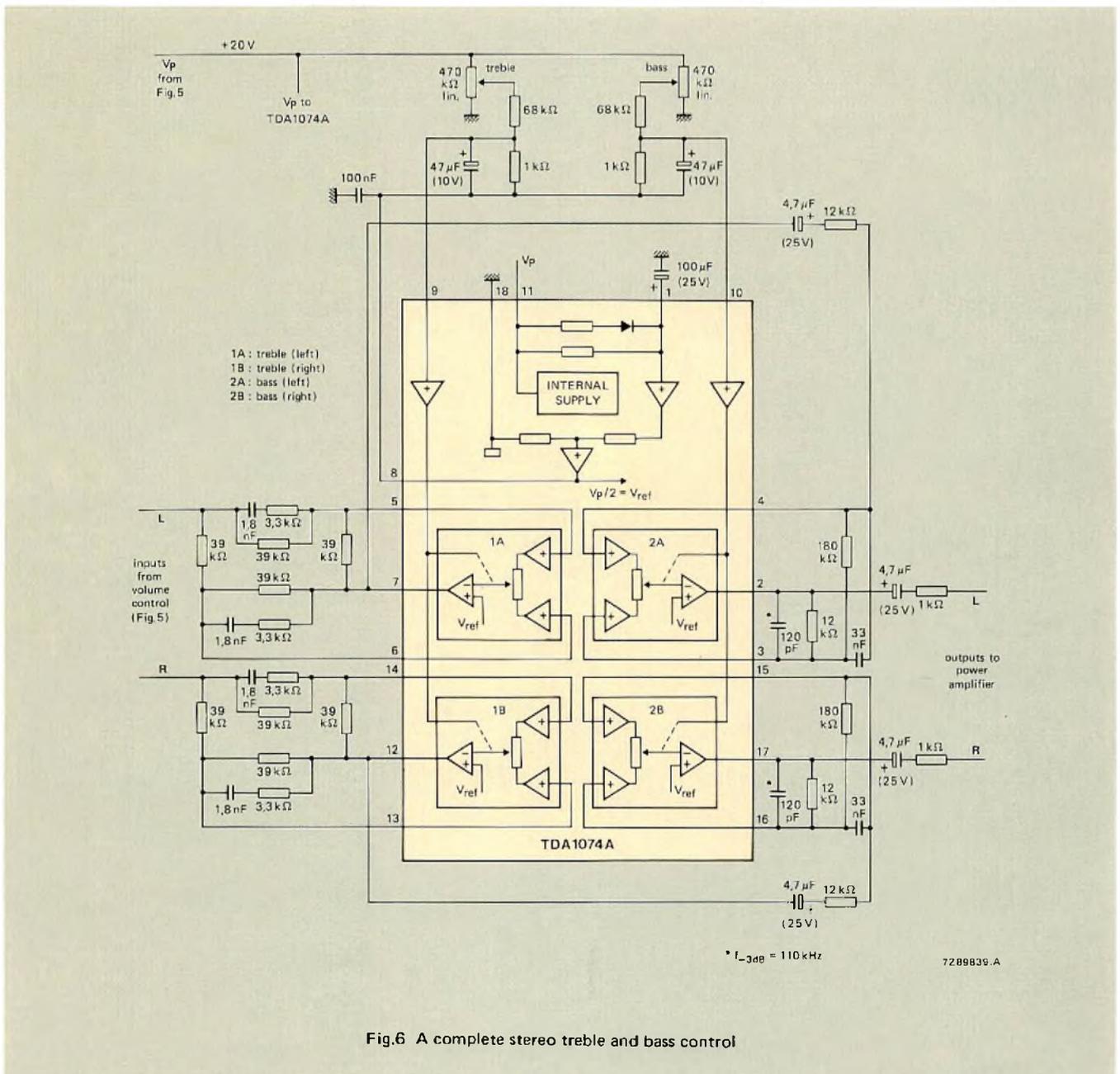


Fig.6 A complete stereo treble and bass control

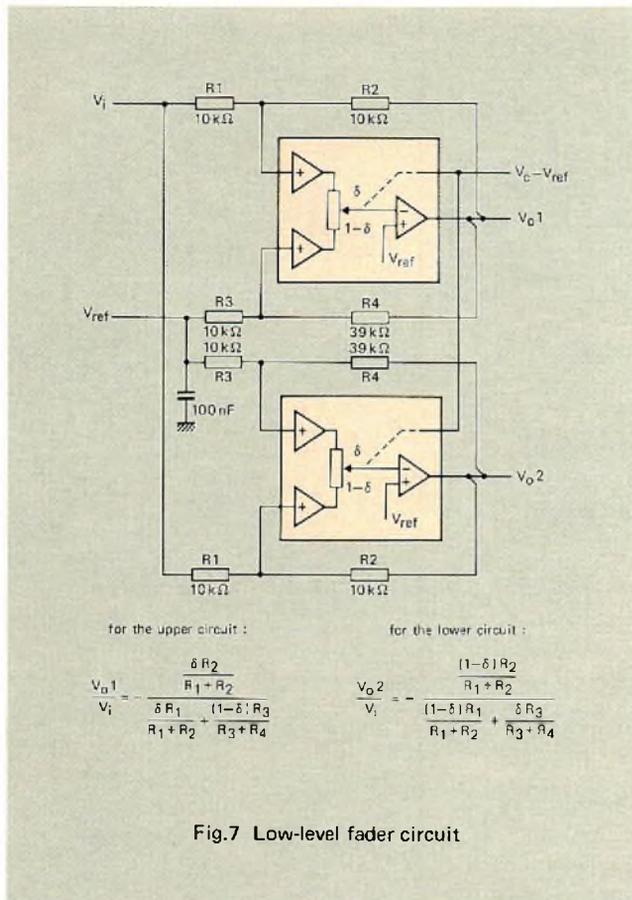


Fig.7 Low-level fader circuit

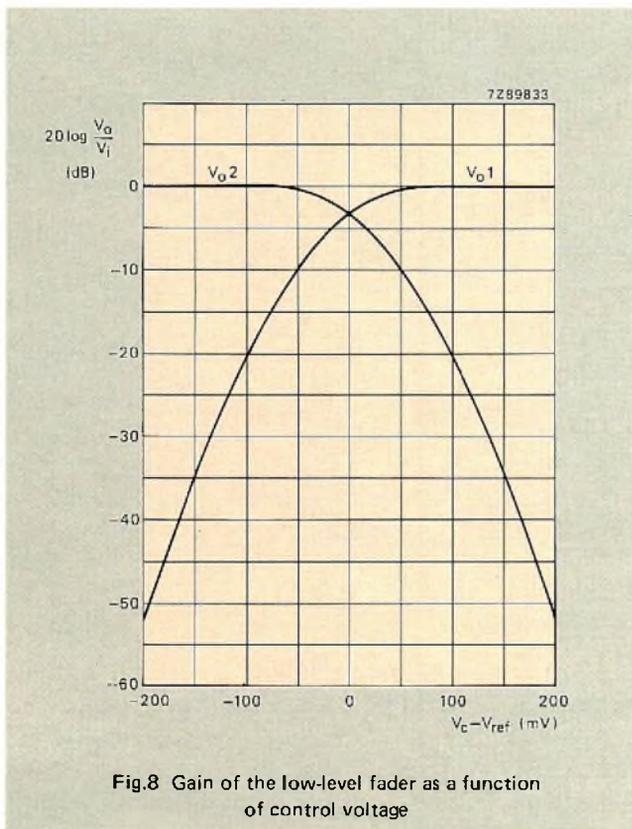


Fig.8 Gain of the low-level fader as a function of control voltage

connected back-to-back so that, when the attenuation of one block is maximum, the attenuation of the other is minimum.

With a control voltage $V_C - V_{ref}$ of 175 mV ($\delta = 0.997$ and $1-\delta = 0.003$), the gain V_{o1}/V_i is $R_2/R_1 = 0$ dB and, from the gain equation in Fig.7, the gain V_{o2}/V_i is -43 dB. With a control voltage $V_C = V_{ref}$, $\delta = 0.5$ and $1-\delta = 0.5$. The gain between the input and both outputs is then -3 dB so that the same input is applied to both power amplifiers. With a control voltage $V_C - V_{ref} = -175$ mV, the gain V_{o2}/V_i is 0 dB and V_{o1}/V_i is -43 dB. The gain of the two fader sections is plotted as a function of control voltage in Fig.8.

Since the TDA1074A contains two ganged pairs of electronic potentiometer/op-amps, one of these ICs is sufficient to construct a complete stereo low-level fader as shown in Fig.10. The performance specification for this circuit is given in Table 3.

TABLE 3
Performance of the low-level fader circuit in Fig.10

supply voltage	8.5	V
maximum voltage gain	0	dB
voltage gain with $V_C = V_{ref}$ (V_{O} front = V_{O} rear)	-3	dB
noise voltage with $V_C = V_{ref}$		
unweighted (r.m.s.)	54	μ V
unweighted (peak)	90	μ V
weighted A (r.m.s.)	36	μ V
weighted CCIR 468 (peak)	175	μ V
total harmonic distortion at 1 kHz		
output voltage $1.5 V_{rms}$	0.045	%
1 V_{rms}	0.03	%
0.5 V_{rms}	0.019	%

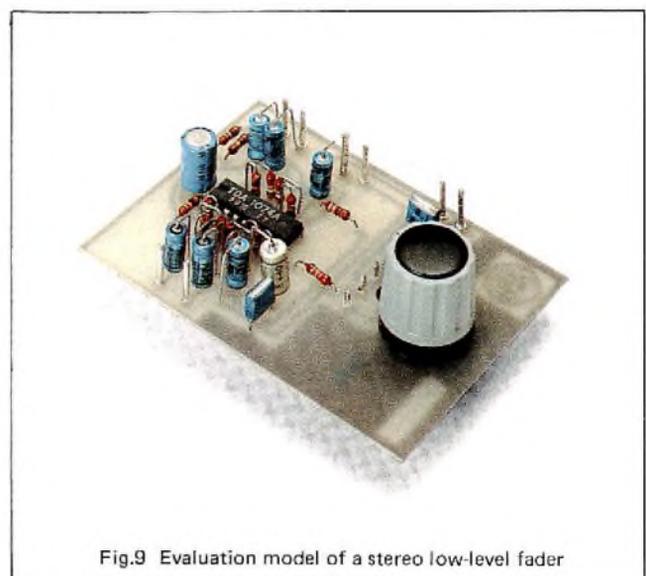


Fig.9 Evaluation model of a stereo low-level fader

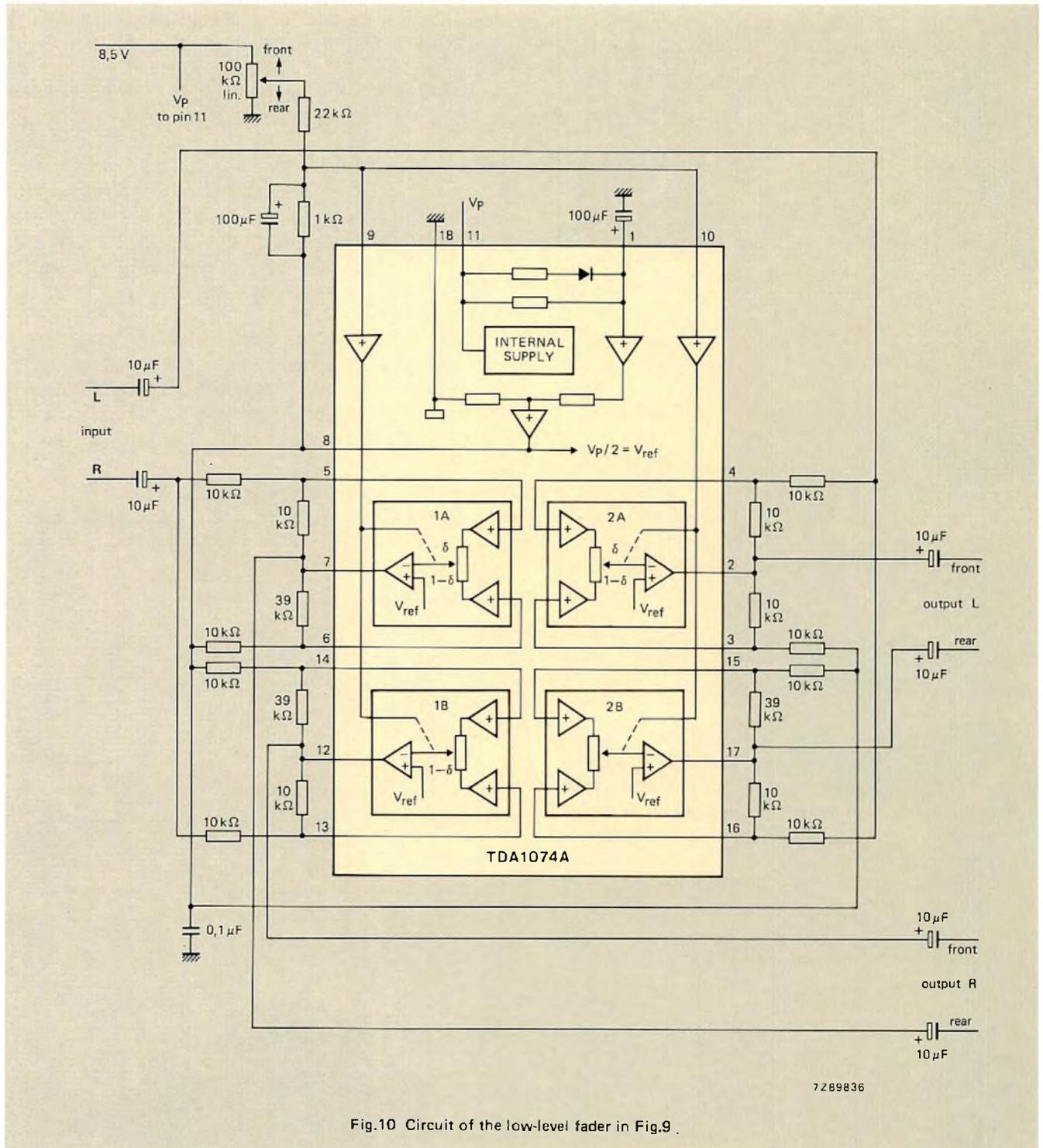


Fig.10 Circuit of the low-level fader in Fig.9 .

FURTHER INFORMATION

More comprehensive information regarding the design and performance of the circuits described in this article is available in Ref.2.

REFERENCES

1. SCHILLHOF, U., 'Displays and control of analogue functions with RTS', *Electronic Components and Applications*, Vol.2, No.1, November 1979, pp.2 to 15.
2. ECKERT, W. and KILIAN, E. A., 'D.C.-controlled audio functions', Philips Technical Publication 061, ordering code 9398 039 80011.

When you need to exchange digital data between a number of sources and users, or over any distance, serial transfer may well be your best choice. Serial bus protocols and dedicated hardware to implement them now make it possible to extend digital techniques into many consumer and semi-professional application where the constraints of parallel transfer previously constituted a barrier.

Small area networks for serial data transfer

A. GOLDBERGER, C. KAPLINSKY, and A. P. M. MOELANDS

The attraction of serial data transfer is that it requires fewer lines – and, at least equally important, fewer line drivers, receivers, and signal-processing circuits – than parallel transfer. There are already many applications in which this is a decisive consideration, and with the inroads of digital electronics into homes, motor cars, and small businesses many more are in prospect.

Because microprocessors and microcomputers work with data in parallel form, parallel transfer is still the method of choice where distances are short and the number of devices sharing a communication channel is small. It is straightforward and fast, and in the disciplined environment of most computing and data-processing equipment the multiplicity of conductors required is unobjectionable. But in many other applications of digital data transfer that is not so.

The answer is then to sacrifice speed for simplicity and flexibility, and to opt for serial instead of parallel transfer. Two conductors are usually sufficient, and the additional requirement it imposes for parallel-to-serial and serial-to-parallel converters can be easily met by today's LSI.

SERIAL DATA LINKS

Figure 1 shows three types of serial data link.

A point-to-point link, joining only two stations, may be half-duplex, with transmission alternately in each direction, or full-duplex with transmission simultaneously in both directions. A loop network is a special type of point-to-point link in which data circulates in one direction only between a number of stations operating in half-duplex mode.

A multipoint network joins several stations; one is always the primary or master, controlling all transmission, and the

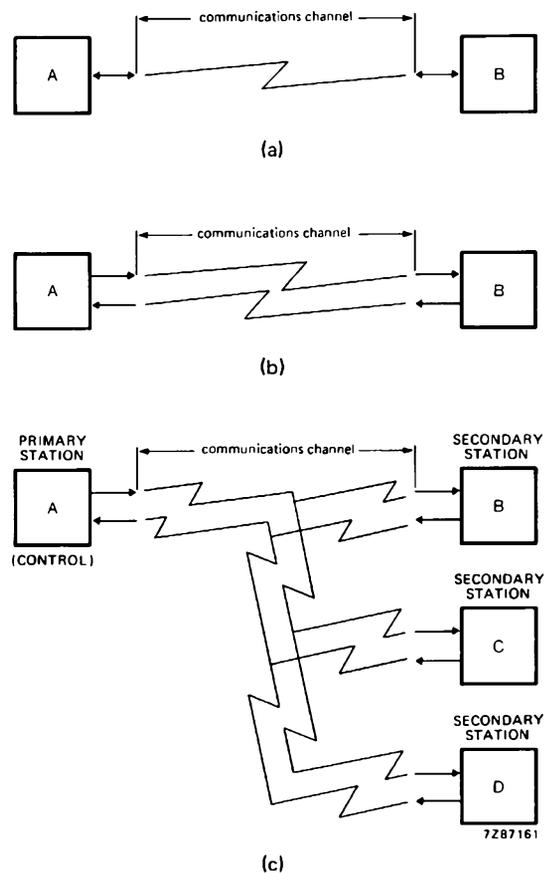


Fig.1 Three types of non-switched serial data link:
 (a) point-to-point half duplex,
 (b) point-to-point full duplex,
 (c) multipoint duplex

others are secondaries. The stations may operate in half or full-duplex mode, and whenever transmission is in progress between the primary and one of the secondaries the others are idle.

Serial communication formats

Serial data can be transferred asynchronously (unclocked, Fig.2(a)) or synchronously (clocked, Fig.2(b)).

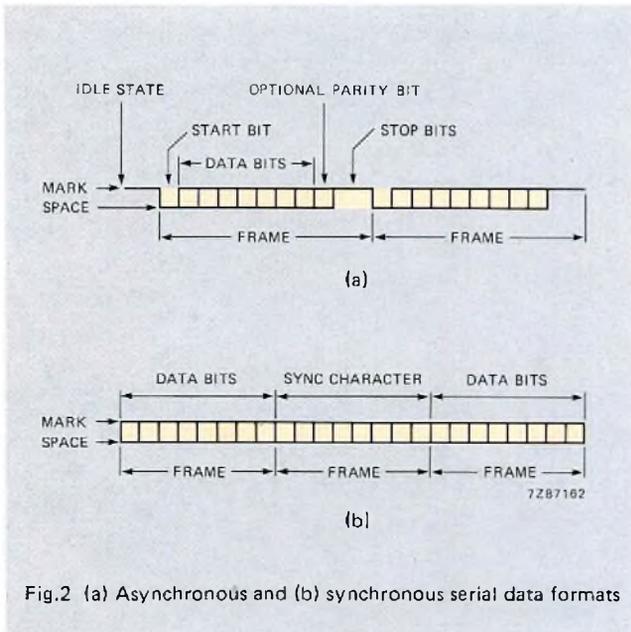


Fig.2 (a) Asynchronous and (b) synchronous serial data formats

Asynchronous data typically originates from low-speed terminals with rates of less than 1200 bits per second. When idle, the transmission line is at mark (binary 1); a start bit, or transition from mark to space (binary 0), signals the beginning of each character, and one or more stop bits its end. This sequence is repeated character by character till the whole message has been sent; the start and stop bits enable the receiver to synchronise itself character by character with the transmitter. The character lengths depend on the code used: five bits for Baudot code, seven (plus an optional parity bit) for ASCII, eight for EBCDIC.

In synchronous transmission the clock signal that synchronises transmitter and receiver may be carried on a separate wire or incorporated in the data stream by one of several codes (NRZI, Manchester, FM, etc.). Once the receiver senses a synchronisation character, data proceeds character by character with no intervening start or stop bits. A special ending character or a specified character count tells the receiver when the message is over.

A message block usually consists of one or two synchronisation characters, a number of data and control characters (typically 100 to 10000), and one or two error-control characters. Between transmissions the line may idle in sync characters or be held at mark.

Asynchronous transmission is advantageous when the data flow is irregular, as from a keyboard operator's typing speed. Because of the simplicity of the interface logic and circuitry, it is also cheap. Synchronous transmission, on the other hand, makes far better use of the communication channel capacity by eliminating start and stop bits between characters. Furthermore, when using modems, it is suitable for multi-level modulation schemes which combine two or four bits in one signal element.

Protocols

To communicate with each other, all stations sharing a data link must of course use the same character code and the same syntax for assembling characters into messages; and to regulate traffic there must be a uniform set of control procedures, or protocols.

Data communication protocols break down into several levels, or layers, that define different types of function or operation. Each level is designed to be functionally independent of the others, but each depends on correct operation of the previous level. Protocol levels range from those that define the physical characteristics of the link (RS232C or CCITT V.35 for instance) to those responsible for functions such as message buffering, code conversion, fault recognition and reporting, communication with a host mainframe, and network management. The protocols are implemented by software packages such as IBM's Systems Network Architecture (SNA), CCITT's X.25, and DEC's DECnet.

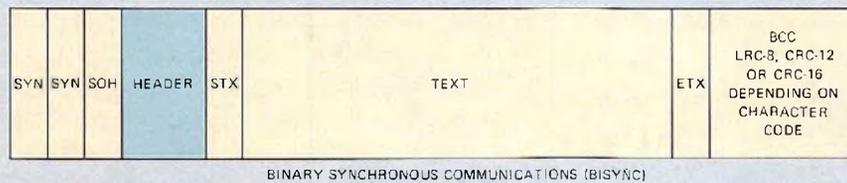
Data link control protocols (DLCs) are the sets of rules necessary to ensure effective communication between the stations sharing a link; their basic functions include

- making and breaking contact between two stations
- ensuring message integrity by error detection, requests for retransmission, and positive or negative acknowledgements
- identifying sender and receiver by polling or selection
- performing special control functions such as start and disconnect.

COPs and BOPs

Data link control protocols can be classed as character-oriented protocols (COPs) and bit-oriented protocols (BOPs).

In COPs a set of control characters forming part of an information code, such as ASCII or EBCDIC, governs the operation of the link. COP messages are transmitted in blocks consisting of a header or control field, a body or text field, and a trailer or error-checking field (Fig.3); special characters mark the block boundaries. Examples of COPs are IBM's Binary Synchronous Communication (BISYNC) and DEC's Digital Data Communications Message Protocol (DDCMP).



SYN SYNCHRONOUS IDLE
 SOH START OF HEADING
 STX START OF TEXT
 ETX END OF TEXT
 BCC BLOCK CHECK CHARACTER
 LRC LONGITUDINAL REDUNDANCY CHECK
 CRC CYCLIC REDUNDANCY CHECK
 FCS FRAME CHECK SEQUENCE

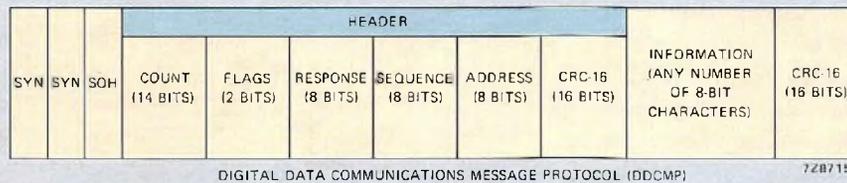


Fig.3 Block formats for character-oriented protocols BISYNC and DDCMP

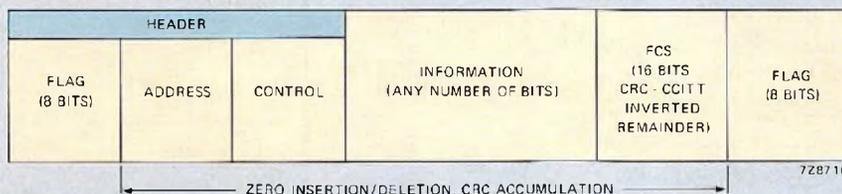


Fig.4 Bit-oriented-protocol block format

BOPs use only two or three control characters to govern operation of the link. These signal the beginning (FLAG) and end (FLAG, ABORT, GA) of a message frame. The fields comprising the bit sequence that follows the opening FLAG are transmitted in a set order of significance (Fig.4): address, control, text, and frame check. The lengths of the address, control, and frame-check fields are fixed; that of the text field is variable and may be zero. Examples of BOPs are ANSI's Advanced Data Communication Control Procedure (ADCCP), IBM's Synchronous Data Link Control (SDLC), ISO's High-Level Data Link Control (HDLC), and Burroughs Data Link Control (BDLC); the last three can be regarded as subsets of ADCCP.

LOCAL AREA NETWORKS

Local area networks (LANs) are more versatile than serial data links. Although the functional differences between the most advanced of the serial data links and the least advanced of the local area networks are small, there is nevertheless a fundamental distinction between them.

The essential characteristic of a serial data link is that it is autocratic; it relies on a master or primary station to control all communication on the link. Even if the data from one secondary station is meant not for the primary but for another secondary, the primary must first store the

data, poll the intended secondary to determine whether it is ready to accept the data, and then retransmit the data. Although this method works, it has several disadvantages:

- It does not adapt easily to changing conditions. If some stations have periods of peak activity, elaborate software algorithms must be written to take that into account. Moreover, if the system characteristics are ever changed, those algorithms have to be updated.
- It does not adapt easily to changing requirements. As all activity is centrally controlled, adding or removing secondary stations necessitates changing the software that controls the primary. This is so even if the secondaries affected need only to communicate with each other and not with the primary.
- The reliability of the entire system depends on that of the primary; if for any reason it fails, the entire system fails.
- If the system is one that relays control information to a decision-making centre, its data-gathering and status monitoring secondaries have to be polled continually. Often, however, the polling indicates no change and so returns little real information; thus, the overhead due to the polling protocol is high in relation to the data acquired. (This problem is dealt with differently in a computer. There, a peripheral unit takes the initiative and interrupts the computer when it requires attention.

As serial data links lack that facility, they must often be designed with much more capacity than their actual data rate requires, merely to accommodate the polling protocol).

These limitations of serial data links derive primarily from the fact that they are based on old electromechanical principles and do not take advantage of the opportunities now offered by VLSI.

Local area networks, by contrast, do not rely on a central controller; they are democratic, not autocratic. Any unit can take control of the network whenever it needs to and can transmit directly to any other. When two units require control simultaneously they arbitrate to determine which gets it. Local area networks therefore have the following advantages over serial data links:

- The network is self-adapting to conditions, since the attached units request to use it only when they need to; if necessary, some can be assigned higher priorities than others.
- Like a telephone exchange, the network can easily be adapted to changing requirements. Any unit can call any other or group of others (conferencing). New units can be added without disturbing existing ones, provided that the total data rate never exceeds the network capacity.
- Since control is not central, communication does not depend on any single unit.
- Since any unit can take control and address any other, the network in effect allows one unit to interrupt another. In a monitoring and control system, therefore, the network capacity need be scarcely larger than the required data capacity.

Local area networks are essentially electronic in character and do not rely on principles carried over from the electro-mechanical era.

Ethernet and IEEE 802

Local area networks already in use, or about to be, include Ethernet, Wangnet, Arcnet, and IEEE 802. Being intended for data rates of 10^6 to 10^7 bits per second over distances of 400 to 2000 metres, these are all overqualified for tasks such as transferring data between a terminal and a slow printer or between a floppy-disc file server and a terminal. They are well suited, however, to transferring data between two large computers with their own files or to carrying digitised voice communication as well as data. The latter application is one that typifies an important distinction between the two LANs currently enjoying the most support, Ethernet and IEEE 802.

In Ethernet any unit may seek access to the network whenever it detects no other activity on it. Since the propagation speed in the network is finite, however, it is possible for two units to test the network, find it idle, and start transmitting before either of them can detect the

transmission of the other. Both will then encounter garbled messages. When that happens, both retire for random periods, then try again. The net effect of this method, known as Carrier Sense Multiple Access/Collision Detection (CSMA/CD), is that no unit can be guaranteed access to the network for any length of time. Ethernet's detractors argue that this restricts the use of the network to few if any channels of digitised voice communication, for if too many units attempt to use the network, voice users will notice gaps in the conversation.

IEEE 802 uses a different access procedure. A token is passed from unit to unit in circular fashion. When a unit receives the token it either uses the network for a time not exceeding a set maximum or passes the token on to the next unit in line. The maximum time that any unit has to wait for access is specified by a network manager. This makes it possible to design units for a certain maximum data throughput and leads advocates of the IEEE 802 protocol to argue that it is suitable for a wider variety of applications than Ethernet – including digitised voice communication.

SMALL AREA NETWORKS

Small area networks (SANs) can be regarded as less expensive, lower-performance counterparts of LANs. Their application areas include

- the home, where they can be used to transfer control, information, and security signals
- business, where they can deal with traffic insufficient to justify a LAN or can serve as feeder networks to a LAN
- certain self-contained units, such as motor cars, where sensors, actuators, and services are necessarily remote from the operator's displays and controls.

Apart from size and performance, SANs differ from LANs in another important respect: LANs are big enough to justify professional managers to configure and administer them; SANs are not. A SAN should require no adaptation when units are added to the network or removed from it.

Two SANs that provide all the facilities of a LAN but on a much smaller scale have established themselves in the past two years, the Inter-IC bus (I²C) and the Digital Data Bus (D²B). Both are designed to cover only limited distances. The procedure for a unit attempting to use the bus is as follows:

- Wait until no activity is detected on the bus.
- Then issue a start bit which is unique and recognisable as such. (If a unit detects another's start bit just as it is about to issue one of its own, it retires and synchronises its internal clock on the edge of the detected start bit.)
- After the start bit, issue message bits serially, most significant bit first.

I²C and D²B are both wired-AND buses, which is essential to their method of resolving conflicts. Consider the situation when two units, A and B, happen to transmit simultaneously. Say A attempts to issue the signal 1101, and B the signal 1110. Both issue the first bit, a 1, and monitor the bus; both see a 1, so both proceed. The same occurs again on the second bit. But on the third bit A issues and sees a 0, while B issues a 1 and sees a 0 because of the wired-AND. This is a signal to B to retire immediately, as it has lost the arbitration. (The retirement must be immediate, otherwise a similar situation would occur again on the fourth bit, but in that case with A losing.) This method of arbitration works because the shortness of the bus sets a limit to the propagation time between any two units on it.

Besides using the same principle for arbitration, I²C and D²B are also similar in other respects. They both distinguish between master and slave and transmitter and receiver. The master is the unit that initiates an exchange with a slave. If it requests a slave to supply data, it is the receiver and the slave is the transmitter. If it supplies data to a slave, it is the transmitter and the slave is the receiver. Not every unit on the bus has to be able to function as a master; slave-only units are also permissible and are of course cheaper.

Another similarity is in the method of acknowledging correct receipt, whether of data or address. The line is an open collector one, and while the transmitter awaits acknowledgement it lets the line stay high. If the receiver does not pull it low within a prescribed time, the transmitter interprets that as a NACK (Negative ACKnowledge) indicating that what was sent was not correctly received. If a non-existent unit is addressed, the addresser will automatically see a NACK.

Apart from these similarities, I²C and D²B differ significantly in function, application area, and throughput characteristics.

I²C

The I²C bus is designed to provide the facilities of a local area network within a single system or equipment. It enables the system designer to distribute the system functions where they are most needed or convenient, without having to pay more than cursory attention to interconnection problems.

The bus consists of two lines, Serial Clock (SCL) and Serial Data (SDA), and, unlike other buses, permits more than one unit to drive the clock. This is possible because SCL is an open-collector line on which several units with their own internal clocks can operate together and synchronise with each other (Fig.5).

Normally, the SDA line changes only when SCL is low, so that the receiver can sample data on the rising edge of the next clock pulse. To generate a start condition however, SDA goes from high to low while SCL is high (Fig.6); this is a unique occurrence which enables all units to recognise the

start of a message. The stop bit is similarly unique: SDA goes from low to high while SCL is high.

A complete message on the I²C bus consists of the following fields:

START	SADD	R/W	ACK	DATA BYTE	ACK		STOP
-------	------	-----	-----	-----------	-----	--	------

- START Start condition (also called start bit)
- SADD Slave address, a 7-bit field identifying the slave to be addressed and the priority of the message.
- R/W Read/write, a single bit indicating whether the addressed slave is to be read from or written to.
- ACK Acknowledge bit for the preceding field.
- DATA A series of 8-bit characters, each followed by an ACK. There is not set limit to the number of characters in this field, although one may be imposed in certain implementations.
- STOP Stop condition (also called stop bit).

There are no hard and fast limits to the length of the bus or the number of units that can be attached to it; there are implicit limits, however, due to the 400 pF maximum capacitance that can be connected to either the SCL or the SDA line.

The I²C bus can be monitored and driven either by specialised hardware or, more slowly, by software in a microcomputer. In the latter case, the start bit is followed by a start byte of the form 00000001 to give slaves which have the system algorithm implemented in software rather than hardware time to poll the data line. Once such a slave

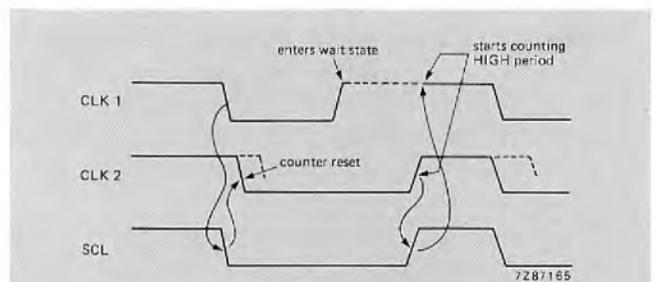


Fig.5 Clock synchronization on the I²C bus

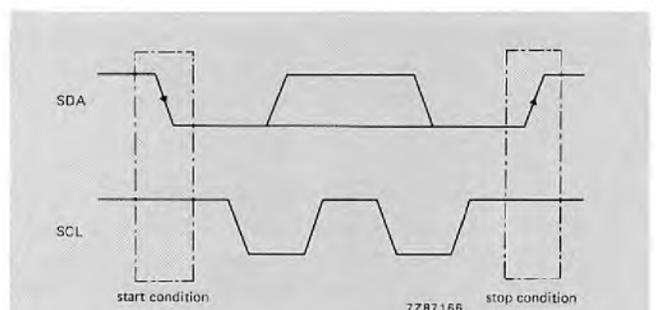


Fig.6 Start and stop conditions on the I²C bus

detects a low value on the SDA line, it switches to scanning the line more frequently.

The maximum bus throughput rate is 100 k bits per second, corresponding to about 11 k characters per second; lower rates can be achieved with slower devices making use of the clock synchronisation principle.

Typical applications of the I²C bus take advantage of the ease with which units can be added to or removed from it. As an example, consider the tv set illustrated in Fig.7. The 'standard' set includes the blocks on the right of the diagram. The control microprocessor has master capabilities and communicates with slave-only units in the keyboard, tuning control, tuning memory, and tuning display. The optional units on the left can be added or removed at any time; the ACK/NACK facility of the bus automatically tells the control microprocessor whether they are there or not.

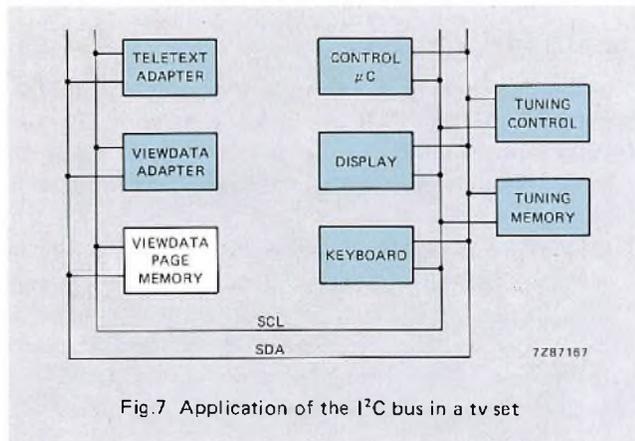


Fig.7 Application of the I²C bus in a tv set

The optional page memory for viewdata is an example of the ability to communicate on the bus without the controller even having to be aware of the unit's existence. Only the viewdata unit needs to communicate with the page memory, and, provided it has bus-master capability, it can do so directly.

The bus gives the set designer freedom to place the various units wherever is functionally best – the display and keyboard on the front panel, the tuning control away from heat sources, and the others where they can most easily be installed later as extras. It also gives him the freedom to redesign units to reduce cost, improve operation, or take advantage of new technology without worrying about the impact on other units in the system; only the two-wire interface and the command set need remain the same.

D²B

The requirements observed in the specification of the D²B include low cost, ease of use, distributed control, ability to work in noisy environment, low interference radiation, flexibility, and expandability. D²B differs from I²C in both protocol and method of transmission.

Part of the flexibility requirement is that units with different throughput rates must be able to share the bus.

Furthermore, low-throughput units should be less expensive to accommodate than high-throughput ones, and faster units should be switchable to slower speed for exchanging messages with slower ones. To meet these requirements the D²B has three operating modes, designated 0, 1 and 2 in ascending order of speed and cost.

Mode 0, the slowest, can be implemented by programming a microcomputer and providing suitable drivers and receivers. Mode 1 requires dedicated hardware but can work with a simple RC clock accurate to within 25%. Mode 2 requires a clock accurate to within 0.1%.

The bus can be up to 150 metres long and can accommodate as many as 50 units. All messages are limited to about 9 ms; in that time one data byte can be transferred in mode 0, 22 in mode 1, and 75 in mode 2. This corresponds to the following throughput rates if the bus is fully utilised and each transfer contains the maximum permissible number of data bytes:

	mode 0	mode 1	mode 2
bytes per second	110	≈2400	≈8200

These rates apply whether the bus is controlled continuously by one master or switched between several.

A message consists of the fields shown in Fig.8:

- A unique start bit to open the message and synchronise all units.
- One or more bits to identify the required operating mode. Mode arbitration works similarly to the address arbitration of the I²C; if two masters compete for the bus, the one using the lower mode prevails.
- Twelve bits to identify the address of the master and establish priority between competing masters. As the bus can accommodate only 50 units, the extra capacity of this field can be utilised to identify units as to type (f.m. tuner, VCR, amplifier, etc.).
- Twelve bits to identify the address of the slave.
- An acknowledge bit to confirm that the slave is on line and functioning.
- Four control bits to specify whether the transfer is to be a data, address* or status transfer, a read or a write, and whether the slave is to be locked onto a certain master.
- An acknowledge bit to confirm that the slave is able to perform the function required of it.
- One or more data bytes. Each character consists of 11 bits: the 8 data bits, a parity bit, an acknowledge bit, and an EOD (End Of Data) bit to show whether the message is over or more is to follow.

* Each unit on the bus can include a memory accessible to all the others which contains information on what the unit is and how to control it; i.e., a digital instruction manual. This information can be used by the interrogating unit and can also be transmitted in a form readable by the user of the system.

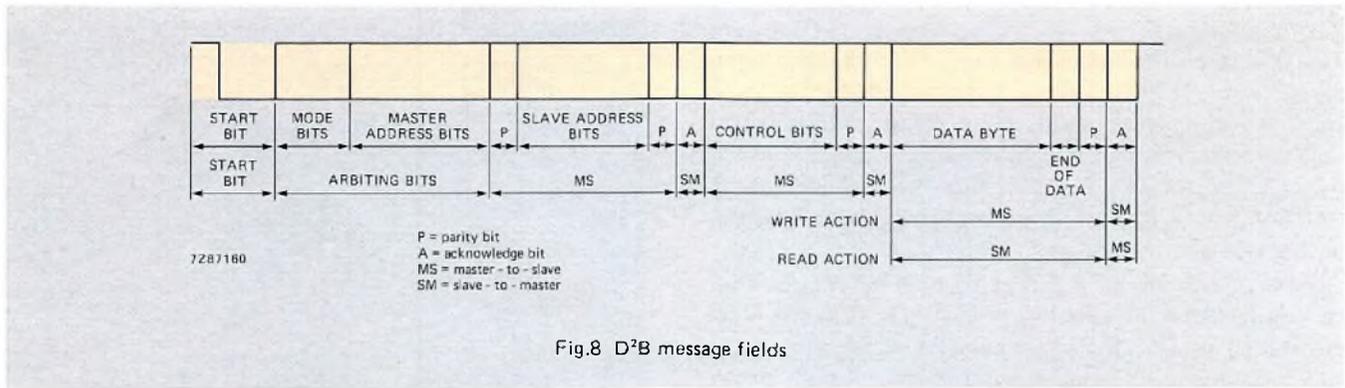


Fig.8 D²B message fields

Note that all except the start and mode-selection fields and acknowledge bits are followed by a parity bit.

The D²B uses only one line (actually a twisted pair, since signal transmission is differential) on which clock and data are time-division multiplexed. Each bit consists of the five parts shown in Fig.9:

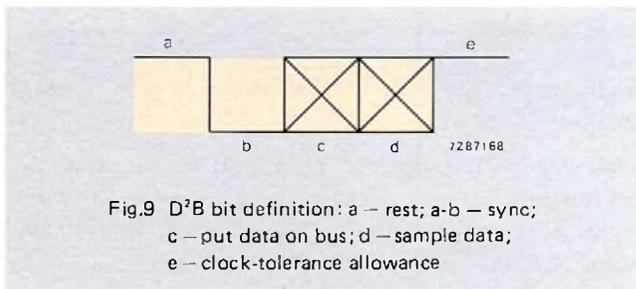


Fig.9 D²B bit definition: a – rest; a-b – sync; c – put data on bus; d – sample data; e – clock-tolerance allowance

- a – Rest time, to ensure that all units see a high level before the bus goes low.
- b – The high-to-low transition a-b is generated by the bus master and synchronises the clocks of all slave units.
- c – The time during which the transmitter puts data on the bus.
- d – The time during which the receiver samples the data.
- e – Allowance for unit-to-unit clock tolerances.

The specification of a bit in D²B, unlike that of most other systems, differs according to the function of the bit and takes account of all timing differences between units.

Timing

Consider Fig.10; by the time a square edge at the input of driver of unit A is clocked into unit B it will have been degraded by the following factors:

- the time through the driver of unit A
- the propagation time down the bus
- the RC rise or fall time
- the difference in clock phase between A and B
- the difference in clock frequency between A and B.

During an arbitration bit (mode or master-address field) unit A may generate the transition a-b (Fig.9), another unit may be putting data on the line (c), while a third may be sampling data (d). After the arbitration is completed only two units remain active on the bus and need be considered, the master and the slave.

The timing of a data transfer from master to slave is not the same as from slave to master. In a master-to-slave transfer the difference between the best and worst case in the master determines the timing. In a slave-to-master transfer the worst combinations of master and slave have to be taken into account, for the a-b transition that initiates each bit is always generated by the master.

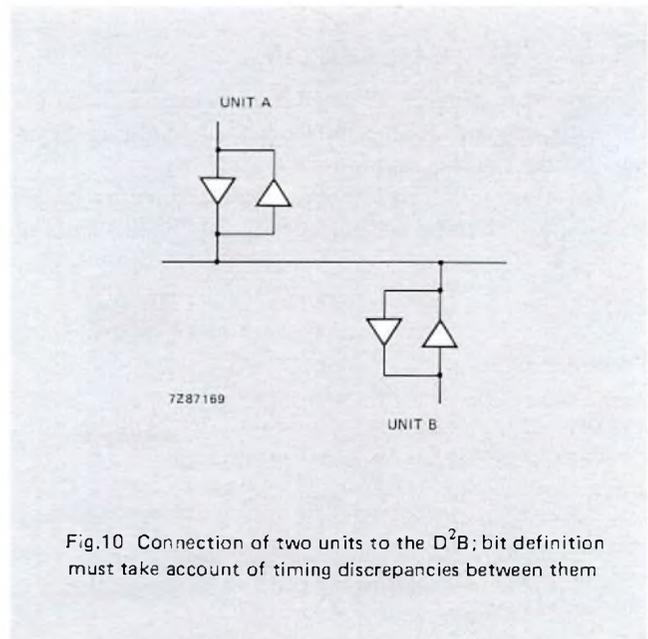


Fig.10 Connection of two units to the D²B; bit definition must take account of timing discrepancies between them

The bit timing specification must therefore be calculated for all combinations of master and slave: best/best, best/worst, worst/best, and worst/worst. The D²B is therefore specified at the bit level by the duration of the various phases of a bit, not only for the different message fields but also for the three operating modes.

Applications

The D²B is designed primarily as a device-to-device interconnection, although it could also be used in certain self-contained equipment where some of its characteristics, such as low radiation and greater length, might make it preferable to the I²C. It is currently being considered by CENELEC as a possible European standard for interconnection of electronic apparatus in the home.

A good example of a D²B application is the control of electrical services in a motor car (Fig.11). As in the tv-set application of I²C, the bus eliminates wiring constraints and facilitates placement of controls and displays where they are most convenient to the user. Master control panels within easy reach of the driver could control engine, entertainment, safety, comfort, and other services. Slave units at the sites of the services would decode the signals on the bus and perform the required functions. Options and extras would become easier to add; a power-controlled antenna, for example, could be installed without extensive rewiring. Diagnostic sensors could also be incorporated so that a computer connected to the bus could analyse such functions as ignition timing, carburetion or fuel injection, fuel consumption, combustion efficiency, lubrication efficiency, temperature control, and electrical system performance. It is conceivable that the widespread adoption of such a bus could lead to a fundamental reconsideration of many of the concepts that have dominated motor car design for most of the past century.

HARDWARE AVAILABILITY

The potential benefits of small area networks, both I²C and D²B, depend on the availability of hardware incorporating the bus logic and interfaces.

Hardware for I²C is already being marketed by Philips companies in Europe and includes the MAB8400 series of

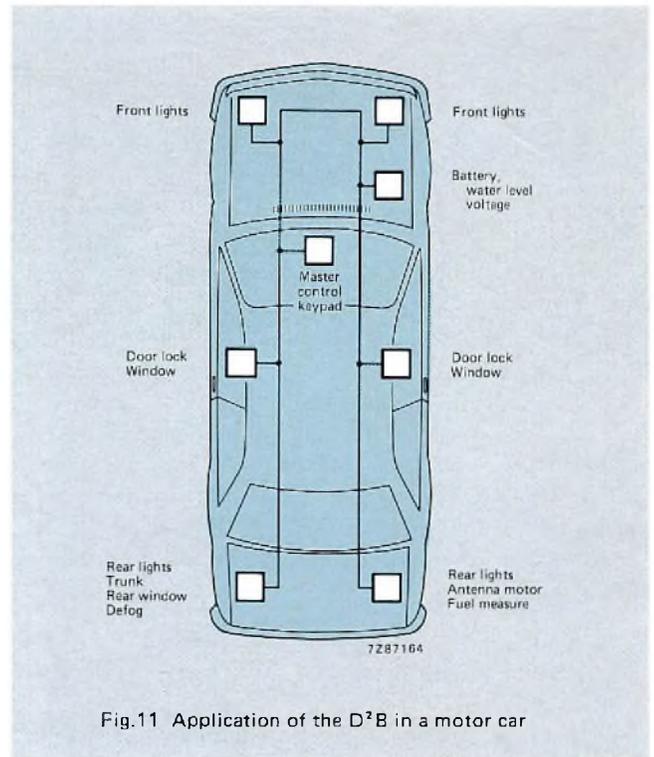


Fig.11 Application of the D²B in a motor car

single-chip microcomputers. Peripherals incorporating the bus interface are also available and more are being developed. They include display drivers, memories, timers, tuning systems, A/D and D/A converters, and a CMOS gate array for specialised functions.

A recent licensing agreement between Philips, Signetics, and Intel will result in widespread availability in both Europe and North America of PCF80C48 and PCF80C51-based microcomputers incorporating the I²C and D²B buses, as well as development support products such as assemblers and in-circuit emulators.

ACKNOWLEDGEMENT

Part of this article originally appeared in the November 3 issue of Electronics, copyright 1982, McGraw-Hill Inc.

The new PC54/74 range of high-speed logic integrated circuits are lower power replacements for LSTTL logic, and faster alternatives to earlier CMOS circuits. Their manufacture is based on proven silicon-gate CMOS processes and manufacturing facilities and, since they can operate from a supply as low as 2 V, they will be compatible with future generations of memories and microcomputers which will require a supply of less than 5 V.

High-speed CMOS

R. CROES

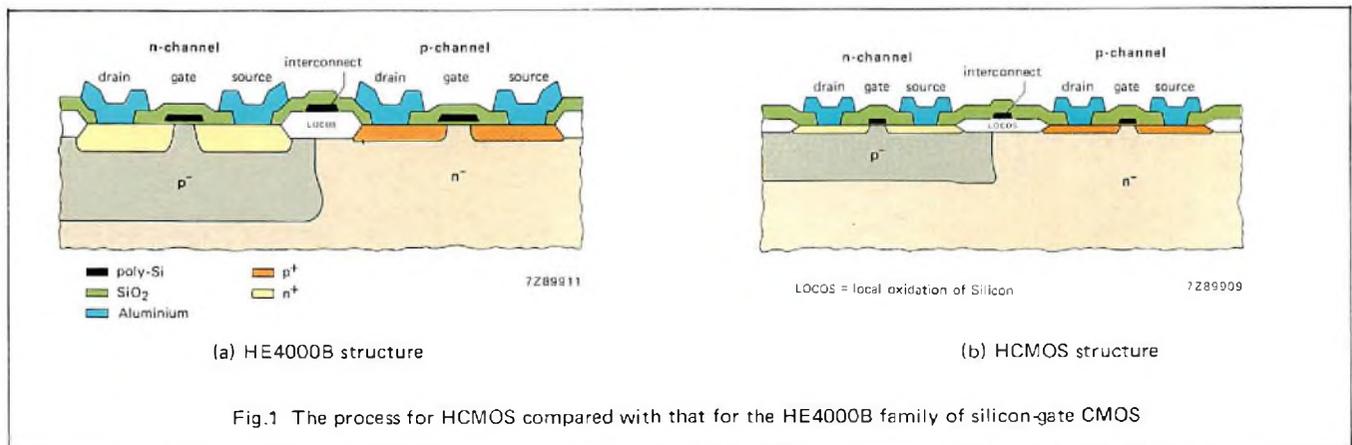
Manufacturing processes for complex single-chip integrated circuits such as microcomputers and large-capacity memories have been so refined that these circuits are now faster and/or less power consuming than the discrete CMOS and LSTTL circuits available to interconnect them. This anomaly severely restricts achievable overall system performance and has highlighted the vital importance of our continuing development programme to reduce the power consumption and increase the speed of discrete logic circuit elements.

In the '70s, we used the self-aligning 6 μm (and later 4 μm) polycrystalline silicon-gate CMOS process and our technique for the local oxidation of silicon (LOCOS) to manufacture the HE4000B family. These p-well silicon-gate CMOS circuits were nearly three times as fast as the then available metal-gate CMOS circuits and yet consumed only about 65% of the dynamic power. Now we are using the same proven CMOS manufacturing facilities and process, but with tighter layout rules, a 3 μm gate structure and thinner oxide in the gate region, to obtain a further fivefold speed increase and a tenfold increase of drive capability for

our new PC54/74 high-speed CMOS family of logic integrated circuits.

This enhancement of the CMOS process endows the PC54/74 family with the low power consumption, high input noise immunity and wide operating temperature range of earlier silicon-gate CMOS, combined with the high speed and drive capability previously only attainable with bipolar LSTTL. The PC54/74 family therefore eliminates the need to compromise between speed and power consumption and allows optimisation of the performance of new CMOS logic designs. Also, in existing designs, PC54/74 circuits can directly replace some or all of the logic elements from other families, both CMOS and bipolar LSTTL, without interfacing problems. This can considerably reduce costs by simplifying power supply and cooling requirements, allowing higher packing density, increasing reliability and extending the operating life of equipment.

The initial PC54/74 family, which will be extended in the future, comprises 117 circuits, all of which are available in two versions. Circuits with the type number suffix HC



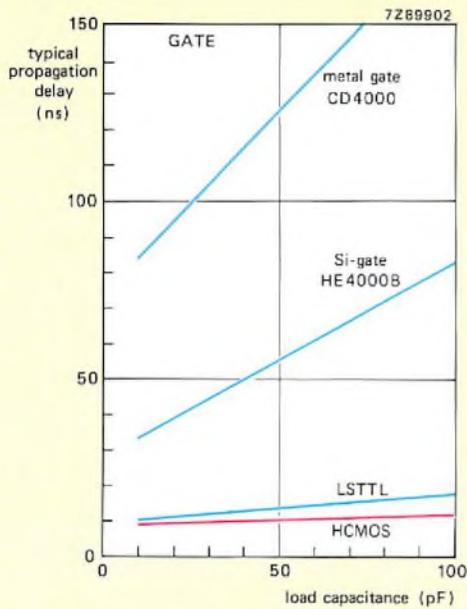


Fig.2 As its name suggests, high-speed CMOS is fast. Gate propagation delay with a 50 pF load is 1/6th of that of earlier silicon-gate CMOS and 1/12th of that of metal gate CMOS

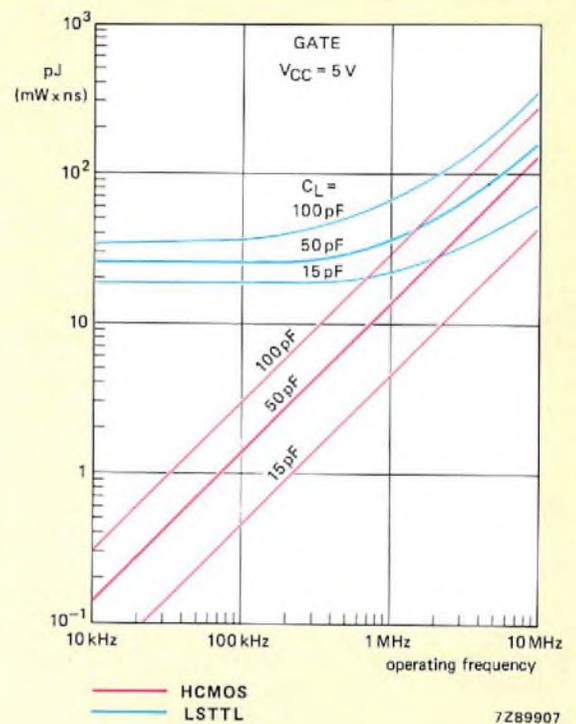


Fig.3 Power/speed product for HCMOS and LSTTL gate shows the advantage of HCMOS at frequencies below 10 MHz

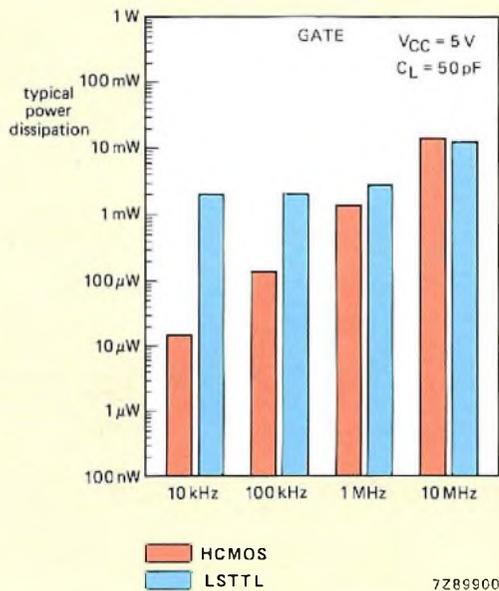


Fig.4 Typical dynamic power dissipation as a function of frequency for a single gate

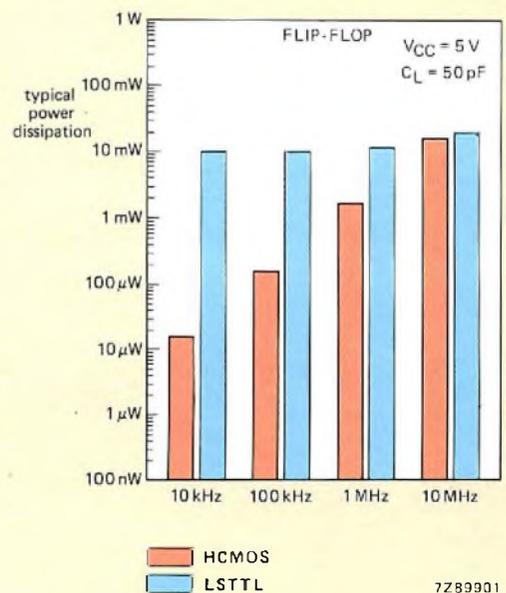


Fig.5 Typical dynamic power dissipation as a function of frequency for a single flip-flop

Comparison of digital ICs comprising four NAND gates

	metal gate CD4000	Si-gate HE4000B	LSTTL 54/74LS	HCMOS PC54/74
Supply voltage range (V_{CC})	3-18 V	3-15 V	5 V \pm 5% (com.) 5 V \pm 10% (mil)	2-6 V (HC/HCU) 5 V \pm 10% (HCT)
Typical quiescent dissipation per gate	2.5 nW	2.5 nW	2 mW	2.5 nW
Max. quiescent current per package at 85 °C	7.5 μ A	7.5 μ A	3 mA*	20 μ A
Typical power dissipation per gate ($V_{CC} = 5$ V, $C_L = 50$ pF)				
at 10 kHz	25 μ W	16 μ W	2 mW	14 μ W
at 100 kHz	250 μ W	160 μ W	2 mW	140 μ W
at 1 MHz	2.5 mW	1.6 mW	2.8 mW	1.4 mW
at 10 MHz	—	—	12.5 mW	14 mW
Typical propagation delay				
$C_L = 15$ pF	90 ns	36 ns	10 ns	9 ns
$C_L = 100$ pF	175 ns	83 ns	17 ns	11.5 ns
Fan-out (TTL loads)	1	1	10	10
Max. operating frequency with $C_L = 15$ pF	3 MHz	5 MHz	25 MHz	25 MHz
Worst-case noise margin				
V_N LOW (% V_{CC})	29	29	8	18
V_N HIGH (% V_{CC})	29	29	14	28
Operating temperature range				
standard (°C)	-40 to +85	-40 to +85	-0 to +70	-40 to +85
extended (°C)	-55 to +125	-55 to +125	-55 to +125	-55 to +125

* 50% of gates in the HIGH state.

are fully buffered, with CMOS input switching levels for high noise immunity, typical gate operating current of 3 μ A at 10 kHz, negligible quiescent supply and input current, typical gate propagation delay of 9 to 11.5 ns (capacitive load 15 to 100 pF), and operate from a supply of 2 V to 6 V; their main role is as faster CMOS replacements for new designs. There are also unbuffered inverters available (HCU suffix) for constructing RC or crystal oscillators and other feedback circuits operating in the linear mode.

Circuits with the type number suffix HCT are also fully buffered, with the same features and functions as HC types, but have TTL input switching levels, operate from a supply voltage range of 5 V \pm 10%, and are pin-compatible with most popular LSTTL circuits. Their main role is replacing LSTTL circuits to reduce power consumption without reducing speed.

To summarise, outstanding features of high-speed CMOS PC74/54 family are:

- Low power dissipation. Typical quiescent current per package is 2 nA for gates, 4 nA for flip-flops and 8 nA for MSI. For gates, maximum quiescent current per package at 85 °C is 20 μ A. Typical gate operating current is 3 μ A

at 10 kHz, 30 μ A at 100 kHz and 300 μ A at 1 MHz. This compares with LSTTL operating currents of 400 μ A up to 100 kHz and 560 μ A at 1 MHz for each gate

- Typical operating frequency up to 50 MHz (15 pF, 25 °C). With a 5 V supply, typical propagation delay for a gate is 9 to 11.5 ns for either HIGH to LOW or LOW to HIGH transitions into capacitive loads of between 15 and 100 pF. This is a quarter of the gate propagation delay for earlier silicon-gate CMOS
- Functions and pinning identical to popular LSTTL and HE4000B circuits
- Types for high speed in new CMOS designs (HC/HCU suffix) operate from a 2 V to 6 V supply and have standard CMOS input switching levels for high noise immunity (twice the d.c. noise margin of LSTTL)
- Types with TTL input switching levels also available (HCT suffix). These circuits operate from a 5 V \pm 10% supply and are mainly for use as pin-compatible CMOS replacements for LSTTL to reduce power consumption without loss of speed. These types are also suitable for converting switching levels from TTL to CMOS

- Fan-out of 10 LSTTL loads (4 mA) for standard outputs, 15 LSTTL loads (6 mA) for bus driver outputs. This is ten times more drive capability than earlier CMOS circuits
- Standardised output buffers allow symmetrical output current sourcing and sinking for equal output rise and fall times (7.5 ns for standard outputs, 6 ns for bus driver outputs). This results in simplified design combined with optimum speed and performance.
- High immunity to electrostatic discharges
- Wide operating temperature range:
 - Standard (PCF74 type number prefix):
-40 °C to +85 °C
 - Extended (PCC54 type number prefix):
-55 °C to +125 °C
- Virtually latch-up free
- Available packages:
 - plastic DIL and mini-pack (SO)
 - ceramic (cerdip) DIL
- Alternate source is RCA

HCMOS CHARACTERISTICS

Supply Voltage

Since the HCMOS circuits with the type number suffix HC or HCU are faster alternatives to earlier CMOS types for new designs, the lower supply voltage limit has been extended to 2 V, giving an overall range of 2 V to 6 V. This gives an important advantage over earlier CMOS circuits because it will permit the continued use of the HCMOS circuits in conjunction with future generations of memories and micro-computers which will require a supply voltage of less than 5 V. The 3:1 ratio between the lower and upper limits of the supply voltage allows the use of simple power supplies, facilitates battery operation and allows the use of a lithium battery as a back-up supply.

HCMOS circuits with the type number suffix HCT are pin-compatible with equivalent LSTTL circuits and are intended to replace them to reduce power consumption in existing circuits. The HCT circuits therefore retain the traditional LSTTL nominal supply of 5 V, but the range has been extended from $\pm 5\%$ to $\pm 10\%$ for both temperature ranges. This allows LSTTL circuits from the extended temperature range to be replaced by HCMOS circuits from the standard temperature range.

Power dissipation

One of the most important requirements for any logic system is low power dissipation. Apart from conserving energy, low power dissipation minimises system cost and

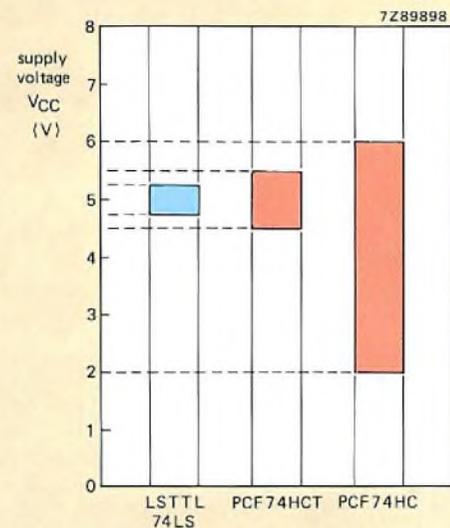


Fig.6 Supply voltage ranges show that standard temperature range HCMOS (HCT) circuits have $\pm 5\%$ more margin than standard temperature range (74LS) LSTTL circuits. HCMOS circuits with the type number suffix HC work with a supply voltage as low as 2 V

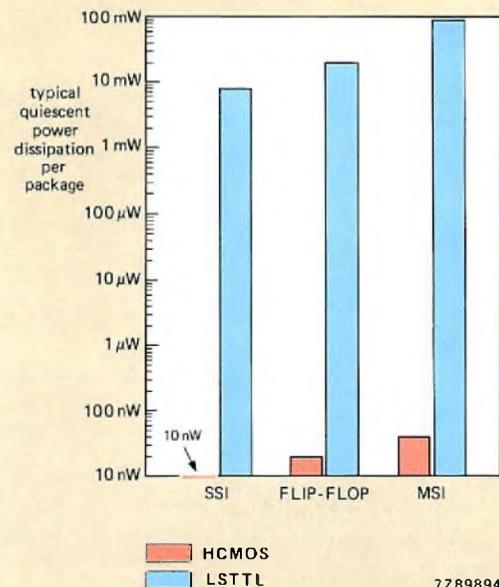


Fig.7 Unlike LSTTL circuits, HCMOS circuits consume very little power when they are not switching

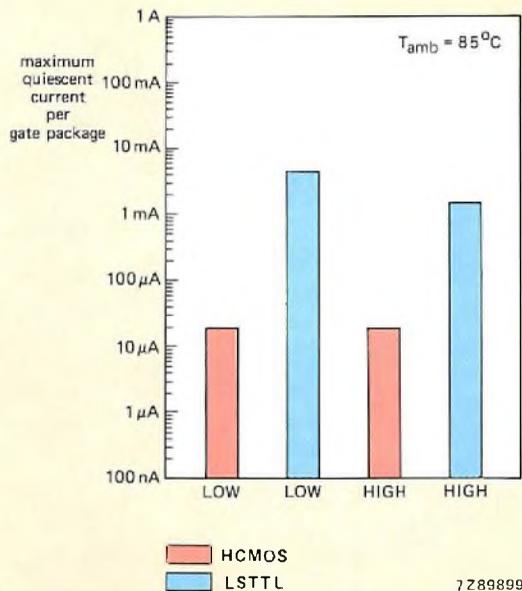


Fig.8 Even a total HCMOS package of four gates under worst-case static conditions consumes more than two orders of magnitude less power than an equivalent LSTTL gate package

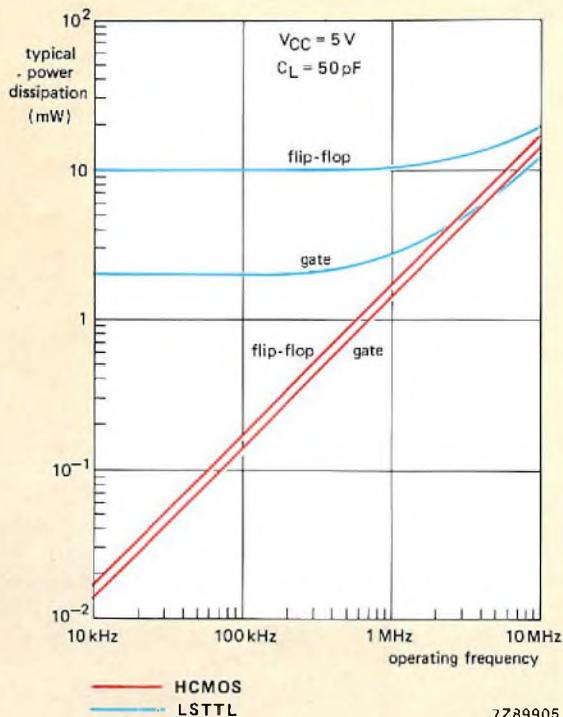


Fig.9 The power cross-over frequency is about 5 MHz for a single gate and above 10 MHz for a single flip-flop

improves reliability because it reduces heat. It simplifies power supplies (to the point where batteries can be used in some cases), and can eliminate hardware such as heatsinks and fans. In turn, cooler boards allow higher component packing densities with consequent reduction of equipment size and weight.

Considering quiescent power dissipation first, Fig.7 shows that all HCMOS functions dissipate more than five orders of magnitude less power than equivalent LSTTL functions. This is because, unlike TTL circuits, CMOS circuits only dissipate negligible power due to leakage currents when they are not switching. Fig.8 shows that the maximum quiescent current of complete HCMOS packages of 4 gates held in the HIGH state at 85 °C is only 1.3% of that of a similar LSTTL package.

Figure 9 compares the dynamic dissipation of single HCMOS and LSTTL gates and flip-flops driving a 50 pF load and indicates a wide power differential at lower frequencies. This is because the high quiescent current of the LSTTL circuits predominates over their transient current and makes the power dissipation independent of frequency below about 1 MHz. Conversely, in the HCMOS circuits, the quiescent current is so low that the transient current predominates and their power dissipation is therefore directly proportional to frequency. The power crossover frequency (the frequency at which the HCMOS circuit starts to dissipate more power than its LSTTL counterpart) is about 5 MHz for a gate, and above 10 MHz for a flip-flop. However, the graphs are only for one gate and one flip-flop. If the dynamic power dissipation is considered for a total package of four gates with only one gate switching, the situation changes considerably. Since all four LSTTL gates draw current regardless of whether they are switching or not, the power dissipation for the single LSTTL gate in Fig.9 must be increased by 6 mW (three static gates) at all frequencies. In the case of the HCMOS package, only the gate that is switching will draw current. The HCMOS plot in Fig.9 therefore also holds good for the total package of four gates. It is thus clear that, if Fig.9 is considered for the total package, the power crossover frequencies increase to well above 10 MHz.

It is interesting to note that, in a more complex circuit comprising a chain of ten flip-flops, the power crossover frequency increases beyond the upper limit of the operating frequency range for HCMOS. This is because, in the HCMOS divider, each flip-flop dissipates half the power of its predecessor because it is operating at half the frequency. In the LSTTL divider, all 10 flip-flops dissipate the same power. The power crossover frequency is therefore extended to the upper limit of the LSTTL and HCMOS operating frequency.

From the foregoing, it is obvious that HCMOS circuits are far less power hungry than their LSTTL equivalents. HCMOS circuits dissipate about the same power as earlier silicon-gate CMOS circuits as shown by the Table on page 25. This is because HCMOS output buffers are made large

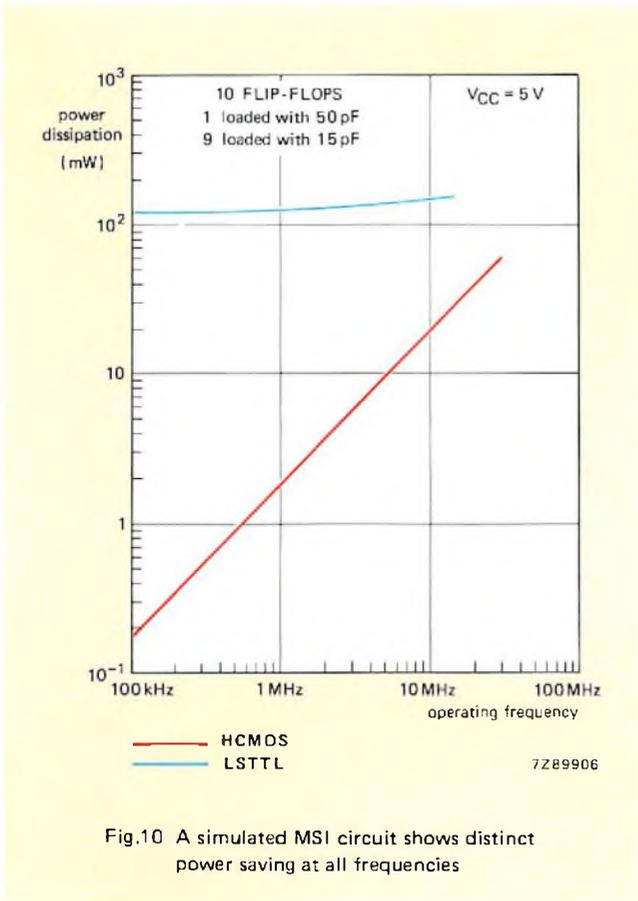


Fig.10 A simulated MSI circuit shows distinct power saving at all frequencies

enough to source and sink LSTTL currents. Nevertheless, HCMOS circuits still retain an important advantage because they are five times as fast as the earlier silicon-gate CMOS circuits.

Input levels and noise immunity

For HCMOS circuits with the type number suffix HC and with standard outputs, the LOW level noise immunity with a 5 V supply is 18% of V_{CC} , and the HIGH level noise immunity is 28% of V_{CC} . This is a considerable improvement over LSTTL where the margin in the LOW state is only 8% of V_{CC} , and the high level margin is 14% of V_{CC} . As shown in Fig.11, the margins are even greater for HCMOS with a higher supply voltage. HCMOS circuits are therefore ideally suited for use in noisy environments such as are encountered in many applications such as industry, telephony and mobile equipment.

Because the input voltage of CMOS circuits is not compatible with that of TTL circuits, it is normally necessary to sacrifice noise margins, speed and quiescent power dissipation to achieve an interface in mixed technology designs. This is not so with the PC54/74 family because it includes many circuits with TTL compatible input levels (HCT type number suffix) so that they can directly replace their LSTTL counterparts without the addition of pull-up resistors at the LSTTL outputs.

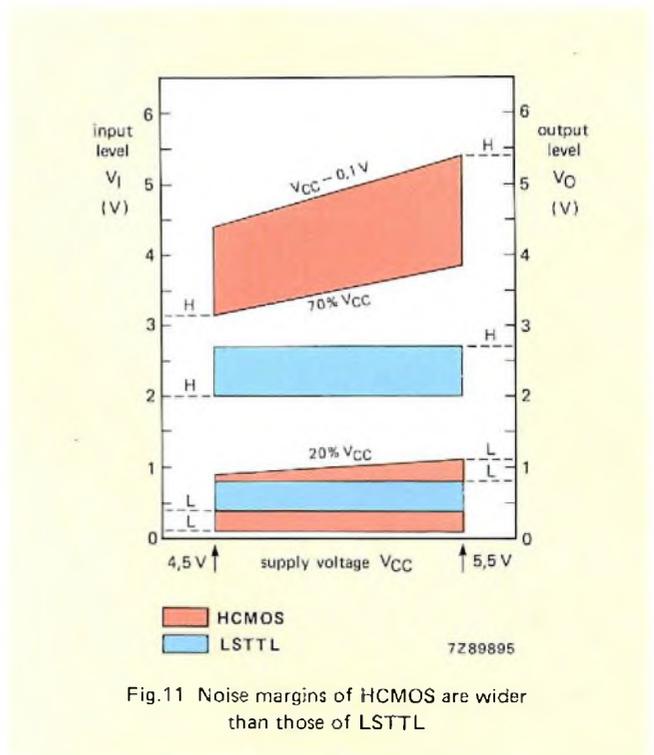


Fig.11 Noise margins of HCMOS are wider than those of LSTTL

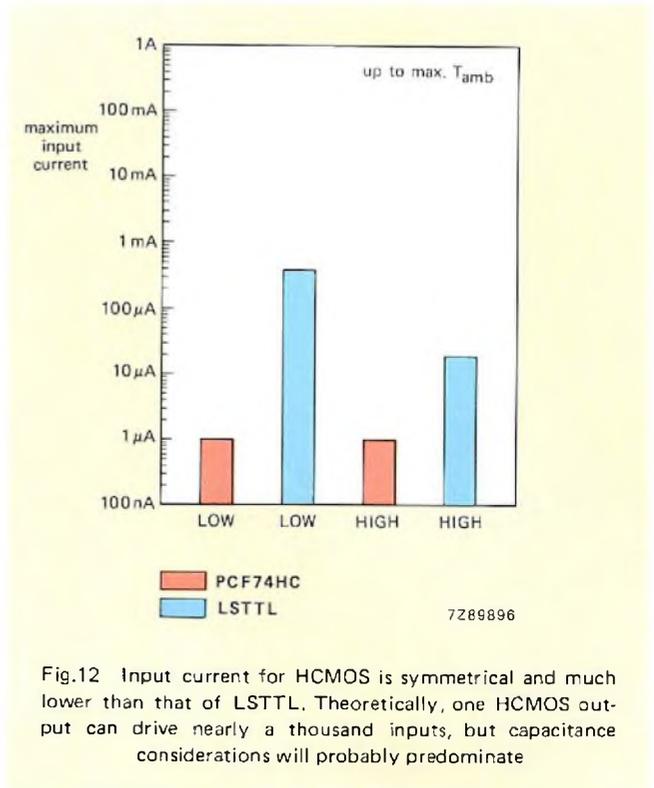


Fig.12 Input current for HCMOS is symmetrical and much lower than that of LSTTL. Theoretically, one HCMOS output can drive nearly a thousand inputs, but capacitance considerations will probably predominate

Another important advantage of HCMOS is the low level of input current. As shown in Fig12, the PC54/74 family draw only 1 μA of drive current in either the LOW or HIGH state. This is only 1/400th of the LSTTL input current in the LOW state.

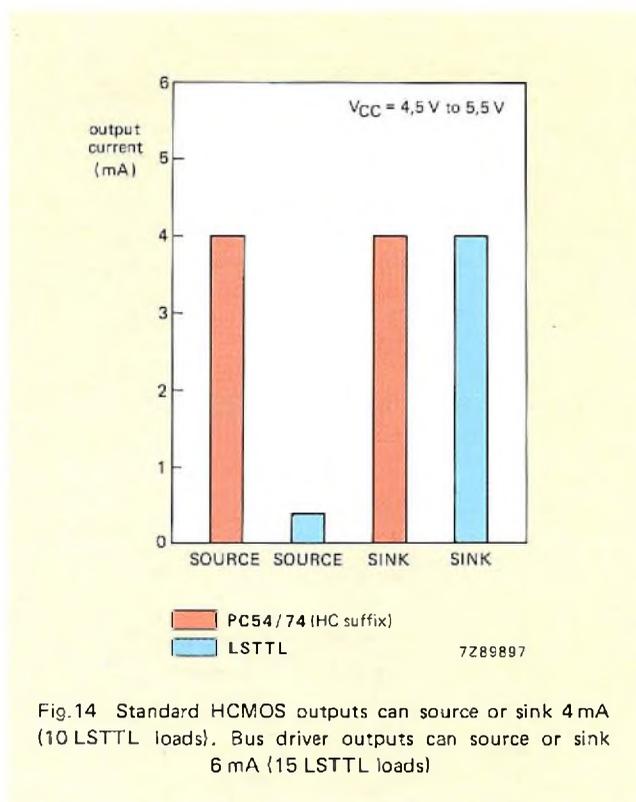
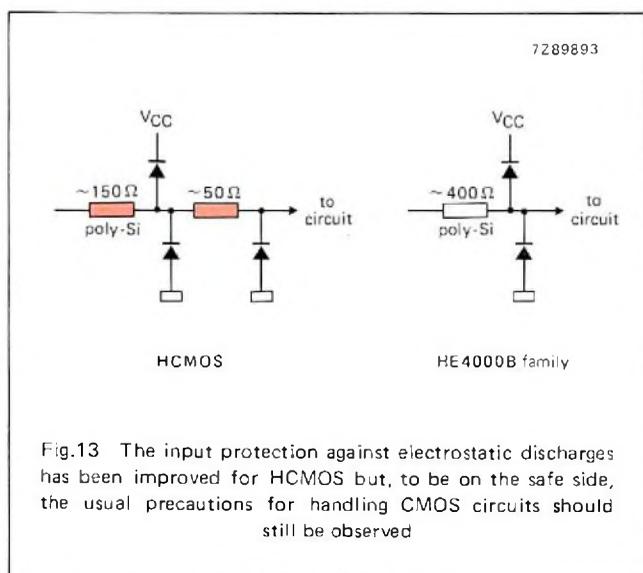
Propagation delay

A key feature of the PC54/74 family is its speed, which is generally compatible with equivalent circuits from the LSTTL range. This makes the new HCMOS circuits eminently suitable as comparable speed, lower power replacements for LSTTL to meet many market requirements which have hitherto excluded the use of available CMOS circuits because they were too slow. The unique combination of high speed and low power dissipation for the new family has been obtained by using a new single polysilicon CMOS integration process with an enhanced $3\ \mu\text{m}$ gate structure to obtain the optimum propagation delay and rise and fall times.

As indicated by the Table on page 25, the propagation delay for a single gate is 10 ns and is only 8% of the delay of metal-gate CMOS, 17% of that of earlier silicon-gate CMOS, and about the same as LSTTL. The typical switching frequency limit for a flip-flop is 50 MHz. Moreover, due to the high current drive capability of the low impedance outputs of HCMOS, the gate propagation delay variation is only 9 ns to 11.5 ns over a load capacitance range of 15 pF to 100 pF. This variation of propagation delay with load is much less than with any other digital ICs.

Input protection

The improved CMOS integration process used for the PC54/74 family also allows polysilicon to be used as a resistor structure at all inputs to slow down fast input transients caused by electrostatic discharges and dissipate some of their energy. Although this, together with two stages of diode clamping provides improved protection for the input gates of HCMOS devices, the usual CMOS handling precautions should still be observed.



Fan-out

Although the PC54/74 family has the low input drive current which is characteristic of CMOS circuits, it is capable of providing the same output current levels as LSTTL without sacrifice of speed or noise immunity. However, unlike LSTTL circuits, all HCMOS circuits, except devices with the type number suffix HCU, have standardised output buffers which allow symmetrical output current sinking and sourcing to obtain equal rise and fall times. This simplifies design and results in optimum speed and a.c. performance.

The outputs of all standard temperature range devices (PC74 series) except bus drivers can source and sink up to 4 mA (10 LSTTL loads). The outputs of bus drivers in the standard temperature range can source and sink up to 50% more current (6 mA = 15 LSTTL loads) in keeping with their intended application. The drive capability of HCMOS circuits in the extended temperature range (PC54 series) is 3.4 mA (8 LSTTL loads) for all devices except bus drivers which can source or sink up to 5.1 mA (12 LSTTL loads). All the drive currents quoted remain valid over the entire temperature range. The HCMOS drive capability is thus ten times that of earlier silicon-gate CMOS circuits and, since the required input current for HCMOS circuits is so low, the fan-out when driving other CMOS or HCMOS circuits is only limited by load capacitance considerations and not by the available drive power. When driving LSTTL loads, the fan-out of HCMOS is equal to that of LSTTL.

Tentative performance data

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).
Voltages are referenced to GND (= 0 V).

d.c. supply voltage range	V_{CC}	-0.5 to +7 V
d.c. input voltage range	V_I	-0.5 to $V_{CC} + 0.5$ V
d.c. output voltage range	V_O	-0.5 to $V_{CC} + 0.5$ V
d.c. input current (any input)	$\pm I_I$	max. 20 mA
d.c. output current		
standard outputs	$\pm I_O$	max. 25 mA
bus driver outputs	$\pm I_O$	max. 35 mA
d.c. V_{CC} or GND current		
standard outputs	$\pm I_{CC}; \pm I_{GND}$	max. 50 mA
bus driver outputs	$\pm I_{CC}; \pm I_{GND}$	max. 70 mA
storage temperature range	T_{stg}	-65 to +150 °C
power dissipation per package		
for standard temperature range		
-40 to +85 °C; PCF74HC/HCT/HCU		
plastic and ceramic (cerdip) DIL	P_{tot}	max. 400 mW, above 60 °C derate linearly with 8 mW/K
plastic mini-pack (SO)	P_{tot}	max. 200 mW, above 70 °C derate linearly with 5 mW/K
for extended temperature range		
-55 to +125 °C; PCC54HC/HCT/HCU		
ceramic (cerdip) DIL	P_{tot}	max. 400 mW, above 100 °C derate linearly with 8 mW/K

RECOMMENDED OPERATING CONDITIONS

Voltages are referenced to GND (= 0 V)

parameter	symbol	min.	typ.	max.	unit
d.c. supply voltage range*					
PCF74HC/HCU; PCC54HC/HCU	V_{CC}	2	5	6	V
PCF74HCT; PCC54HCT	V_{CC}	4.5	5	5.5	V
d.c. input voltage range	V_I	0	-	V_{CC}	V
d.c. output voltage range	V_O	0	-	V_{CC}	V
operating ambient temperature range					
PCF74HC/HCT/HCU	T_{amb}	-40	-	+85	°C
PCC54HC/HCT/HCU	T_{amb}	-55	-	+125	°C
input rise and fall times					
except for Schmitt trigger inputs	$t_r; t_f$		6	500	ns

* d.c. parameters are specified at $V_{CC} = 4.5$ to 5.5 V; the truth table is applicable from V_{CCmin} to V_{CCmax} .

D.C. CHARACTERISTICS

For PCF74HC/HCT/HCU, PCC54HC/HCT/HCU. V_{CC} ref. to GND.

parameter	symbol	limits			unit	conditions
		PCF74/ PCC54		PCC54		
		T_{amb} ($^{\circ}C$)				
		+25	-40 to +85	-55 to +125		
		max.	max.	max.		
quiescent device current						
SSI, gates	I_{CC}	2	20	40	μA	$V_I = V_{CC}$ or GND $V_{CC} = 6 V$
flip-flops; latches	I_{CC}	4	40	80	μA	
MSI	I_{CC}	8	80	160	μA	
input leakage current	$\pm I_{IN}$	0.1	1.0	1.0	μA	$V_I = V_{CC}$ or GND $V_{CC} = 6 V$
3-state output leakage current	$\pm I_{OZ}$	0.5	5.0	10	μA	$V_O = V_{CC}$ or GND $V_{CC} = 6 V$
bilateral switches input/ output switch leakage current per channel	$\pm I_{IS}$	0.1	1.0	10	μA	$V_I = V_{CC}$ or GND $ V_{CC} $ across channel $V_{CC} = 5 V \pm 10\%$

For PCF74HC/HCT/HCU, PCC54HC/HCT/HCU. V_{CC} ref. to GND.
Limits apply across the ambient temperature range.

parameter	symbol	limits		unit	conditions
		min.	max.		
PCF74HC/PCC54HC					
HIGH level input voltage	V_{IH}	3.15		V	$V_{CC} = 4.5 V$
HIGH level input voltage	V_{IH}	3.85		V	$V_{CC} = 5.5 V$
LOW level input voltage	V_{IL}		0.9	V	$V_{CC} = 4.5 V$
LOW level input voltage	V_{IL}		1.1	V	$V_{CC} = 5.5 V$
PCF74HCU/PCC54HCU					
HIGH level input voltage	V_{IH}	3.6		V	$V_{CC} = 4.5 V$
HIGH level input voltage	V_{IH}	4.4		V	$V_{CC} = 5.5 V$
LOW level input voltage	V_{IL}		0.9	V	$V_{CC} = 4.5 V$
LOW level input voltage	V_{IL}		1.1	V	$V_{CC} = 5.5 V$
PCF74HCT/PCC54HCT					
HIGH level input voltage	V_{IH}	2.0		V	$V_{CC} = 5 V \pm 10\%$
LOW level input voltage	V_{IL}		0.8	V	$V_{CC} = 5 V \pm 10\%$

For PCF74HC/HCT, PCC54HC/HCT at $V_I = V_{IH}$ or V_{IL} . V_{CC} ref. to GND.

parameter	symbol	PCF74/PCC54		limits PCF74		PCC54		unit	conditions
				T_{amb} (°C)					
		min.	max.	min.	max.	min.	max.		
		+25		-40 to +85		-55 to +125			
HIGH level output voltage standard and bus driver outputs	V_{OH}	V_{CC} -0.1	-	V_{CC} -0.1	-	V_{CC} -0.1	-	V	$V_{CC} = 5\text{ V} \pm 10\%$ $-I_O = 20\ \mu\text{A}$
standard outputs	V_{OH}	3.8	-	3.7	-	3.5	-	V	$V_{CC} = 4.5\text{ V}$ $-I_O = 4\text{ mA}$
bus driver outputs	V_{OH}	3.8	-	3.7	-	3.5	-	V	$V_{CC} = 4.5\text{ V}$ $-I_O = 6\text{ mA}$
LOW level output voltage standard and bus driver outputs	V_{OL}	-	0.1	-	0.1	-	0.1	V	$V_{CC} = 5\text{ V} \pm 10\%$ $I_O = 20\ \mu\text{A}$
standard outputs	V_{OL}	-	0.32	-	0.4	-	-	V	$V_{CC} = 4.5\text{ V}$ $I_O = 4\text{ mA}$
standard outputs	V_{OL}	-	-	-	-	-	0.4	V	$V_{CC} = 4.5\text{ V}$ $I_O = 3.4\text{ mA}$
bus driver outputs	V_{OL}	-	0.32	-	0.4	-	-	V	$V_{CC} = 4.5\text{ V}$ $I_O = 6\text{ mA}$
bus driver outputs	V_{OL}	-	-	-	-	-	0.4	V	$V_{CC} = 4.5\text{ V}$ $I_O = 5.1\text{ mA}$

For PCF74HCU, PCC54HCU at $V_I = V_{IH}$ or V_{IL} . V_{CC} ref. to GND.

parameter	symbol	PCF74/PCC54		limits PCF74		PCC54		unit	conditions
				T_{amb} (°C)					
		min.	max.	min.	max.	min.	max.		
		+25		-40 to +85		-55 to +125			
HIGH level output voltage	V_{OH}	V_{CC} -0.5	-	V_{CC} -0.5	-	V_{CC} -0.5	-	V	$V_{CC} = 5\text{ V} \pm 10\%$ $-I_O = 20\ \mu\text{A}$
HIGH level output voltage	V_{OH}	3.8	-	3.7	-	3.5	-	V	$V_{CC} = 4.5\text{ V}$ $-I_O = 4\text{ mA}$
LOW level output voltage	V_{OL}	-	0.5	-	0.5	-	0.5	V	$V_{CC} = 4.5\text{ V}$ $I_O = 20\ \mu\text{A}$
LOW level output voltage	V_{OL}	-	0.32	-	0.4	-	-	V	$V_{CC} = 4.5\text{ V}$ $I_O = 4\text{ mA}$
LOW level output voltage	V_{OL}	-	-	-	-	-	0.4	V	$V_{CC} = 4.5\text{ V}$ $I_O = 3.4\text{ mA}$

Since 1980, concerted action involving four geographically separate production centres has effectively halved the failure rate of linear bipolar ICs coming from five different production lines.

Long-term reliability of linear bipolar ICs

F. W. OHLENROTH

Due to steadily-increasing repair costs, and lengthening guarantee periods combined with growing market awareness, the reliability demanded from equipment and, consequently, the components that comprise it, is increasing. Moreover, the period over which reliability is required to remain high is also increasing.

As ICs now contain the majority of the circuitry in most types of electronic equipment, their reliability is of prime importance. The purpose of the investigation described here was to extend the information available on the long-term reliability of ICs, especially those intended for consumer applications. The investigation was primarily aimed at identifying the principal failure mechanisms and establishing data for long-term reliability prediction under normal service conditions.

FAILURE RATE AND RELIABILITY

Reliability is that attribute of quality that describes the ability of an item to perform a required function under stated conditions for a stated period of time (Ref.1). The practical measure of reliability is failure rate, λ , the ratio of the total number of failures in a sample to the cumulative observed time (the device-hours) on that sample.

The observed failure rate of a sample of electronic components generally varies with time in the manner shown in Fig.1, the familiar bathtub curve. Failure rate is initially high, due mainly to components with manufacturing flaws: components with weaknesses that were not revealed at final inspection. There then follows a period of fairly uniform failure rate, after which failure rate rises sharply as wearout sets in.

Mathematically, reliability R is the probability of a component surviving for a given period of time t . Where failure rate λ is constant,

$$R = e^{-\lambda t}.$$

In order that observed failure rates should be a useful basis for product comparison, and for prediction of performance in service, the conditions under which they are obtained must be clearly defined. Moreover, it is also necessary to define exactly what constitutes failure.

The number of failures observed directly from life testing is generally artificially increased to obtain an assessed failure rate. The amount of the increase is calculated on the basis of the Poisson distribution so that there is a certain probability (the confidence level) that the true failure rate of the whole population of similar components will be less than that quoted for the sample tested. A confidence level of 60% is usually chosen.

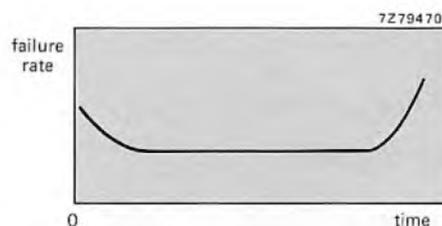


Fig.1 The 'bathtub' curve of failure rate against time showing the falling rate of early failures, the constant-failure period, and, finally, the rising rate of wearout failures

THE TEST PROGRAMME

The life-test programme providing the results from which the reliability data was derived was initiated in 1978. ICs and facilities from five production lines were used.

ICs tested

A total of 53 different IC types were used in the investigation, 49 of them in plastic DIL 16 (SOT-38S) packages. Their principal characteristics relevant to interpretation of the results were as follows.

The ICs were assembled in all five of the production lines. Three epoxy encapsulants were used, MH15/W645, MH15/FO129, and P410BSG. Die attach was by hard (eutectic) soldering or by adhesive. Die areas were up to 13 mm². Die passivation was vapox or Ucarsil lacquer. Internal bond wires were 25 μm or 38 μm gold, TC or TS bonded. Operating voltages were up to 18 V.

Test conditions

All ICs were tested at maximum power dissipation at maximum rated voltages. The actual dissipation was calculated for each type.

To allow for the effect of air circulation, IC junction-to-ambient thermal resistance was measured in the life test ovens themselves.

The actual junction temperatures used for the life tests were 95 °C, 110 °C, 125 °C, 135 °C, 140 °C, 150 °C, 160 °C, and 175 °C.

Failure definition

Failure was defined as lack of the required function: that is, failed ICs were either inoperatives, or had undergone changes in electrical characteristics such as to result in malfunction in the intended application.

Test facilities

All life tests were conducted using the facilities of the Quality Departments associated with the production lines. An attempt was made to minimise differences in test methods and interpretation of results between the various test facilities. Particular attention was paid to

- test duration
- test method
- junction temperature determination
- failure analysis procedures.

ANALYSIS OF RESULTS

Temperature grouping

In order to obtain sufficient data (particularly, observed failures) for reliable analysis of the life-test results, it proved

necessary to limit the number of temperature groups. This was achieved by combining adjacent temperature groups. Several trial groupings were made:

Trial 1

- 110 °C group comprising 95 °C and 110 °C test results
- 125 °C group comprising 125 °C test results
- 137 °C group comprising 135 °C and 140 °C results
- 150 °C group comprising 150 °C results
- 175 °C group comprising 175 °C results.

Trial 2

- 110 °C group comprising 95 °C and 110 °C results
- 125 °C group comprising 125 °C results
- 140 °C group comprising 135 °C, 140 °C and 150 °C results
- 175 °C group comprising 175 °C results.

This latter grouping yielded the most coherent results, as tabulated in Appendix 2. Weibull plots based on this grouping are given in Appendix 3.

Confidence bands

A computer-generated table of the combined test results showing averages and upper and lower limits for the two-tailed 60% confidence interval is given in Appendix 2. As is usual with electronic components, only the 60% confidence limits have been taken into account, and these are indicated in the plots in Appendix 3. It is apparent that the confidence band remains rather wide over the entire test period.

During the early stages of the life tests up to about 1000 hours, the wide band is caused by the small number of device hours. After 1000 hours for the 175 °C group, the band remains wide because only few devices were kept on test, and thus, the number of device-hours was limited. In view of the wide confidence bands, which sometimes overlap those of other groups, the plots of Appendix 3 were considered to be the best straight-line fits.

Failure-rates

Weibull plots

Where failure rate is varied with time, as in the bathtub curve of Fig.1, its behaviour is generally described in terms of the Weibull formula:

$$\lambda(t) = \beta \lambda_t^{\beta} t^{(\beta-1)}$$

Where $\beta < 1$, failure rate decreases with time: characteristic of the early failure period. Where $\beta = 1$, failure rate is constant: the constant-failure rate period.

Where $\beta > 1$, failure rate increases with time: the wear-out period. In Weibull plots of cumulative failures against time, the slope of the plots is the value of β .

Early failures

From the Weibull plots given in Appendix 3, it is evident that, although the plots for 140 °C and 175 °C clearly show regions of $\beta < 1$, those for 110 °C and 125 °C do not. This might suggest that weak devices were more temperature-dependant, but insufficient failures occurred in the early period at lower temperature to support any clear conclusion. The 140 °C and 175 °C plots, on the other hand, clearly show regions of early failure. It is interesting that the 140 °C early-failure period extends to 1500 hours, whereas that for 175 °C extends to 2500 hours – both periods much greater than expected. Moreover, theory predicts that the early-failure period should become shorter as temperature increases. Again, no clear explanation has been found.

TABLE 1
Average failure rates from Appendix 3

temperature group (°C)	failure rates ($\times 10^{-6}/h$)			
	all types		DIL-16 types only	
	1000 h	8000 h	1000 h	8000 h
110	1.6	1.7	1.7	1.6
125	2.3	2.5	2.0	2.0
140	4.1	3.5	4.0	3.1
175	16.0	8.1	16.0	7.7

Wearout failures

The results show no evidence of any wearout failures within the time periods and temperature range covered.

Cumulative failures and failure rates

Table 1 is derived from the plots of Appendix 3 and shows cumulative failure percentages and average failure rates, respectively.

Activation energy

Failure rate and temperature

The effect of temperature on failure rate can be derived from Arrhenius' Law:

$$\lambda \sim e^{-E_a/(kT)}$$

where E_a is the activation energy, k is Boltzmann's constant, and T the absolute temperature.

Calculated value

It is evident that the activation energy for the failure modes in the bipolar ICs tested can be calculated from the observed failure rates at the various temperatures.

The results so far obtained do not justify any departure from the activation energy of 0.7 eV assumed in MIL-HDBK-217D. This value had also been assumed in the derivation of the lifetime prediction curves of Fig.2 from the results obtained in a previous exercise.

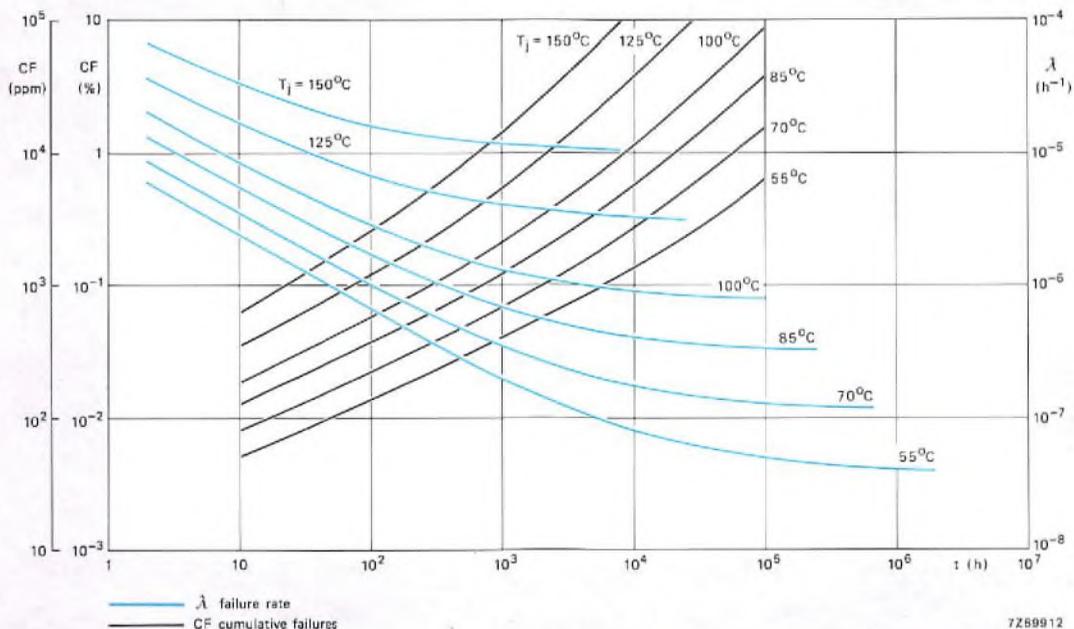


Fig.2 Life expectancy curves calculated for bipolar ICs using an activation energy of 0.7 eV

ANALYSIS OF FAILURES

All failed devices were analysed to determine the cause of failure. Table 2 lists the causes of failure found and their distribution in time

Stability failures

The distribution by temperature of stability failures is given in Table 3. There it can be seen that there may be some increase in the incidence of stability failure with both time and temperature.

Holes in oxide

The distribution of failures due to holes in oxide layers is given by test temperature in Table 4. It can be seen that

devices with oxide-layer defects fail earlier at higher temperatures, as expected. It is noteworthy that devices with oxide holes can survive for up to 4000 h.

Masking defects

One failure due to masking defects was observed after 168 h at 150 °C; one after 500 h at 110 °C; and one device survived 4000 h at 110 °C despite the masking defect.

Micro-alloying failures

Micro-alloying failures are due to holes in the flowglass caused by electrical overstress. Aluminium flows through these holes to short circuit the aluminium interconnect to

TABLE 2
Causes and occurrence of failure

failure		number of failures by test duration (h)									
mode	cause	168	500	1000	2000	3000	4000	5000	6000	8000	total
die	stability	1	—	—	—	—	2	—	4	9	16
faults	holes in oxide	5	—	1	—	—	2	—	—	—	8
	mask faults	1	1	—	—	—	1	—	—	—	3
	metallisation	—	2	1	—	—	—	1	1	2	7
	micro-alloy	—	—	3	—	—	—	—	—	2	5
	assembly	bond failures	—	—	—	—	1	—	1	—	—
faults	broken wires	1	—	—	1	—	2	—	3	—	7
	broken dice	1	—	1	—	—	1	—	—	—	3
	unknown	5	1	4	1	1	—	1	—	2	15
	not analysed	1	—	2	1	—	—	—	—	—	4
failures		15	4	12	3	2	8	3	8	15	70
total device-hours (×10 ⁶)		2.2	6.1	11.7	15.2	18.2	21.1	26.0	27.9	31.5	

TABLE 3
Temperature distribution of stability failures

temperature (°C)	number of failures by test period (h)									
	168	500	1000	2000	3000	4000	5000	6000	8000	total
100	1	—	—	—	—	1	—	—	1	3
135	—	—	—	—	—	1	—	1	3	5
160	—	—	—	—	—	—	—	3	5	8
failures	1	—	—	—	—	2	—	4	9	16
device-hours (×10 ⁶)	2.2	6.1	11.7	15.2	18.2	21.1	26.0	27.9	31.5	

TABLE 4
Temperature distribution of oxide holes

temperature (°C)	number of failures by test duration (h)			
	168	1000	4000	total
110	–	1	1	2
125	1	–	–	1
135	–	–	1	1
175	4	–	–	4
failures	5	1	2	8
device-hours ($\times 10^6$)	2.2	11.7	21.1	

TABLE 5
Distribution of micro-alloying failures by temperature and test facility

temperature (°C)	number of failures by test duration (h)	
	1000	8000
110	1	–
125	1	2
150	1	–
total failures	3	2
device-hours ($\times 10^6$)	11.7	31.5

an adjacent region of the IC. Occurrence in linear ICs is known to depend to some extent on type, and to be associated with circuit transients and electrostatic discharge.

Table 5 gives the failures due to micro-alloying observed during the test programme, as distributed by operating temperature and test facility. It is possible that some failures were due to repeated handling and testing of devices on test.

Wire and wire bond failures

Failures due to broken internal wires and wire bonds were randomly distributed throughout the test. Their distribution is shown in Table 6, where sudden increase in failures at 135 °C is evident; this was traced to an aberration in one of the production lines. These failures were evenly distributed over a number of IC types.

Metallisation defects and aluminium smear

The distribution of failures due to metallisation defects and aluminium smear is given in Table 7. These results suggest a random distribution over life of failures of this nature.

Cracked dice

Table 8 gives the distribution of failures due to cracked or broken dice. Failures due to this cause were randomly distributed over the test period.

Unassigned failures

The causes of 19 failures were not established. These included ICs that exhibited no visible defect but were either electrically defective or had no electrical defect after the encapsulation was removed. However, the success of failure analysis also depends on the skill of the analyst and the time available for the analysis.

TABLE 6
Wire and wire-bond failures by temperature and test facility

temperature (°C)	number of failures by test duration (h)						
	168	2000	3000	4000	5000	6000	total
110	–	1	–	–	–	–	1
125	–	–	1	–	–	–	1
135	1	–	–	1	–	3	5
160	–	–	–	1	–	–	1
175	–	–	–	–	1	–	1
total failures	1	1	1	2	1	3	9
device-hours ($\times 10^6$)	2.2	15.2	18.2	21.1	26.0	27.9	

TABLE 7
Distribution of failures due to metallisation defects
and aluminium smear

temperature (°C)	number of failures by test duration (h)					total
	500	1000	5000	6000	8000	
110	—	—	—	1	—	1
125	2	1	1	—	—	4
160	—	—	—	—	2	2
total failures	2	1	1	1	2	7
device-hours (×10 ⁶)	6.1	11.7	26.0	27.9	31.5	

TABLE 8
Distribution of failures due to cracked dice

temperature (°C)	number of failures by test duration (h)			
	168	1000	4000	total
125	—	1	—	1
135	1	—	1	2
total failures	1	1	1	3
device-hours (×10 ⁶)	2.2	11.7	21.1	

TABLE 9
Distribution of failures for which no cause was established

temperature (°C)	number of failures by test duration (h)							total
	168	500	1000	2000	3000	5000	8000	
95	1	—	—	—	—	—	2	3
110	—	—	1	—	—	—	—	1
125	3	—	4	1	1	1	—	10
140	1	1	—	—	—	—	—	2
150	1	—	—	1	—	—	—	2
175	—	—	1	—	—	—	—	1
total failures	6	1	6	2	1	1	2	19
device-hours (×10 ⁶)	2.2	6.1	11.7	15.2	18.2	26.0	31.5	

The distribution of these unassigned failures is given in Table 9. In accordance with usual practice, all unassigned failures were included with die faults for the purposes of analysis.

Review of failure causes

Table 10 shows the distribution of all failures observed in the test programme, divided between die and assembly faults. It appears that early failures are mainly due to die faults, and that the early failure period extends to about 1000 h. Die faults increase again after about 4000 h operation. Assembly faults were randomly distributed throughout the test programme.

With the exception of the stability failures, the principal die faults were due to deficiencies in oxide and metallisation layers. Assembly faults were mainly broken wires.

Within the limits of the investigation, failure cause appeared independent of IC type and complexity.

CONCLUSIONS

From the spot comparisons given in Table 11, the results obtained from this test programme show a factor of 2 or more improvement compared with the life-expectancy curves published in Ref.2 in 1980 and given in Fig.2. This illustrates the improving trend in quality and reliability resulting from continuous attention to all aspects of quality improvement.

The curves of Fig.2 were originally constructed from test data employing an activation energy of 0.7 eV as used in MIL-HDBK 217D. The latest results do not suggest any basis for changing that value.

Further test programmes are planned.

TABLE 10
Die and assembly fault distribution

	number of failures by test duration (h)									
	168	500	1000	2000	3000	4000	5000	6000	8000	total
die faults	11	4	11	2	1	5	2	5	15	56
assembly faults	2	—	1	1	1	3	1	3	—	12
failures	13	4	12	3	2	8	3	8	15	68
device hours ($\times 10^6$)	2.2	6.1	11.7	15.2	18.2	21.1	26.0	27.9	31.5	

TABLE 11
Cumulative failure percentages

temperature group	1000 h		8000 h	
	these tests	Ref.2	these tests	Ref.2
110 °C	0.17%	0.35%	1.3%	1.8%
125 °C	0.20%	0.55%	1.6%	3.2%
140 °C	0.40%	0.95%	2.5%	6.5%

REFERENCES

1974. *List of basic terms and definitions and related mathematics for reliability*. IEC Publication No.271, second edition.
1980. *Integrated quality – consumer bipolar ICs*. Philips' Technical Note No.159; ordering code 9398 016 40011.

APPENDIX 1

Details of IC types used in the life-test programme and the dissipation at which they were tested.

types	die area (mm ²)	voltage (V)	dissipation (W)	types	die area (mm ²)	voltage (V)	dissipation (W)
DIL-16							
TAA630	3.5	12	0.55	TDA1005A	5.8	18	0.30
TBA510	2.5	12	0.55	TDA1025	4.5	22	0.45
TBA520	3.5	12	0.55	TDA1026	5.2	12	0.29
TBA530	1.4	12	0.40	TDA1028	5.4	23	0.80
TBA540	3.5	12	0.78	TDA1029	4.6	23	0.80
TBA570	2.7	18	0.59	TDA1038	3.7	12	0.48
TBA750	3	12	0.34	TDA1039	4.6	12	0.55
TBA850	1.8	12	0.30	TDA1050	2.6	12	0.35
TBA860	1.8	12	0.23	TDA1070	6.2	12	0.16
TBA920	4.7	12	0.60	TDA1071	4.2	12	0.15
TBA970	2.3	12	0.75	TDA1072	5.2	15	0.88
TCA270	4.9	12	0.70	FDA1074	8.7	20	0.80
TCA420A	2.8	15	0.72	TDA2510	4.9	12	0.48
TCA530	2.3	68	0.50	TDA2520	6.5	12	0.60
TCA550	2.3	12	0.14	TDA2521	6.7	12	0.60
TCA730	4.6	15	0.86	TDA2522	6.3	12	0.60
TCA740	4.4	15	0.86	TDA2523	6.3	12	0.60
TCA760B	2	13	0.11	TDA2524	7.8	12	0.80
TCA800	6.3	12	0.75	TDA2525	7.8	12	0.80
TDA1001	2	18	0.30	TDA2530	4.4	12	1.0
TDA1005	5.8	18	0.30	TDA2532	6.0	12	1.0

Appendix 1 (continued)

types	die area (mm ²)	voltage (V)	dissipation (W)
TDA2541	5.9	12	0.90
TDA2560	5.9	12	0.90
TDA2581	4.1	12	0.34
TDA2590	7.7	12	0.90
TDA2591	7.7	12	0.88
TDA2593	7.7	12	0.80
TDA2620	3.6	36	0.50
TDA2630	6.4	15	0.50
TDA2640	3.8	12	0.15
TDA2710	3.6	12	0.62
TDB1033	4.6	12	0.55

types	die area (mm ²)	voltage (V)	dissipation (W)
DIL-24			
SAA5030	13	12	1.2
TDA2771	5.0	12	0.56
SIL-9			
TDA1010	2.7	20	2.6
TDA2611A	2.6	35	2.0
Die-attach methods: hard (eutectic) soldered or glued			

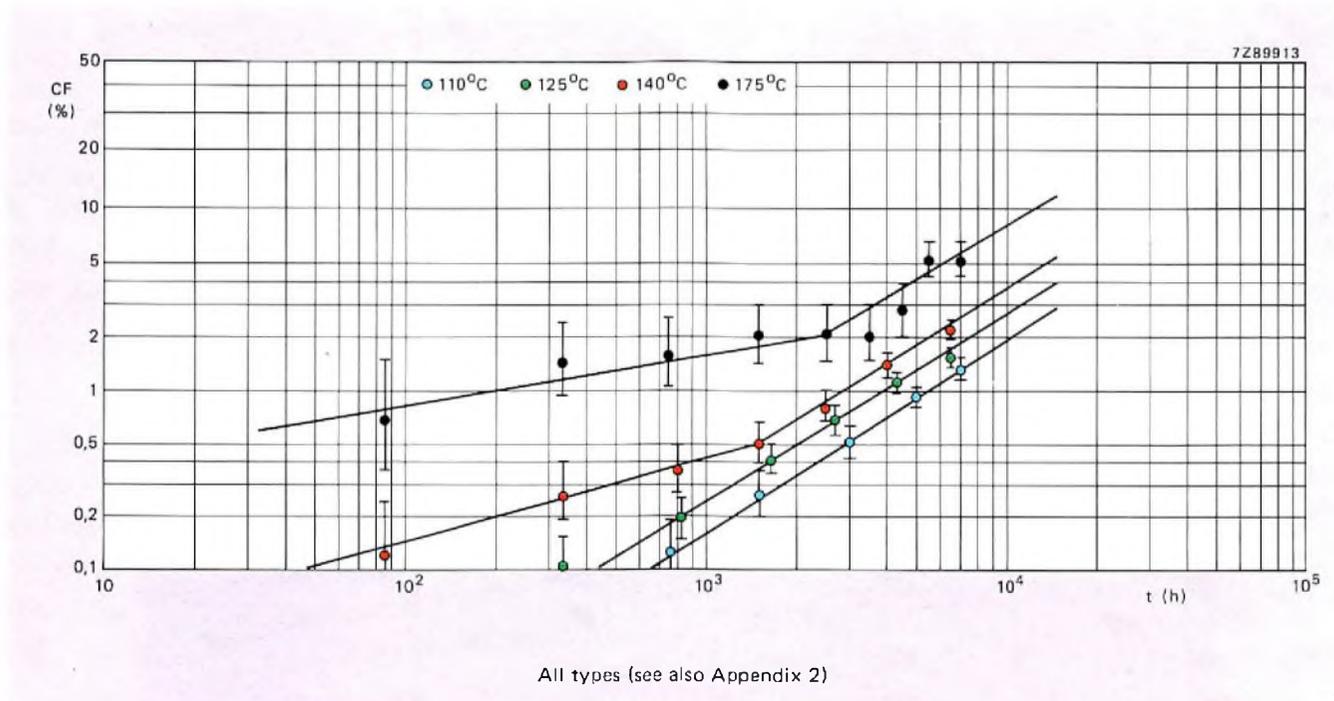
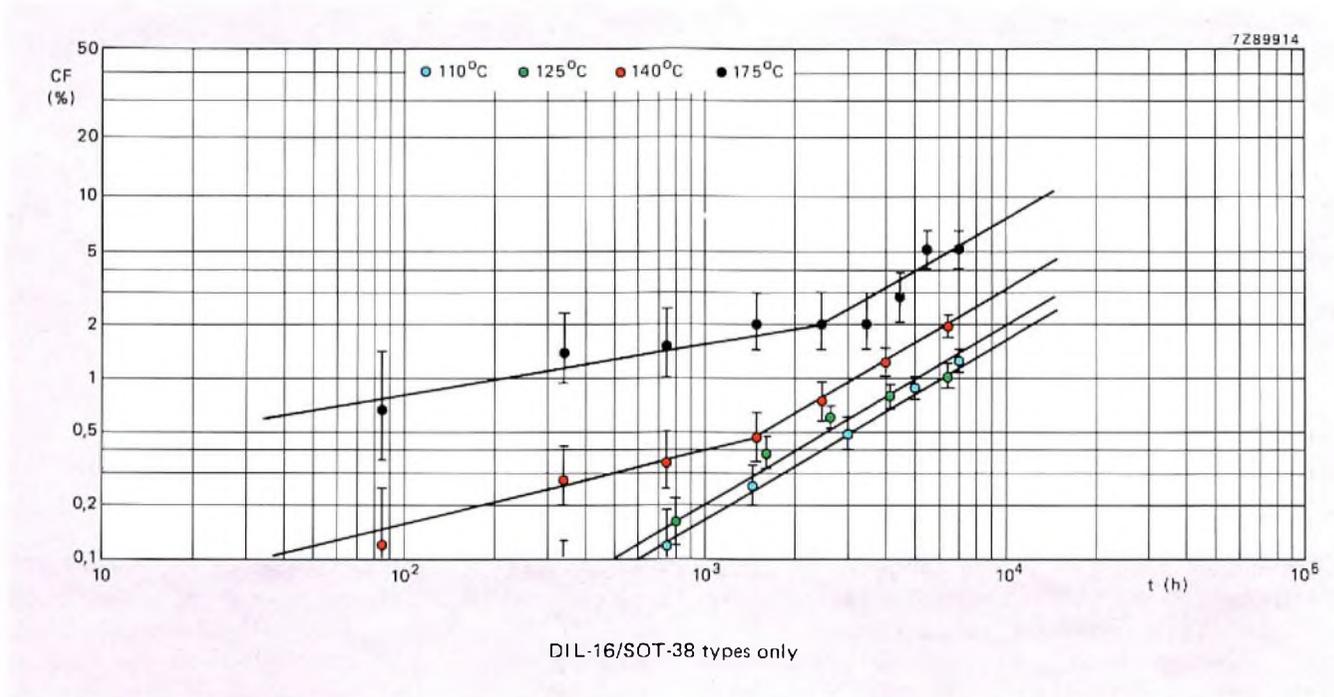
APPENDIX 2

Failure percentages and confidence limits, for all types.

temp. (°C)	time (h)	sample	failures	lower (60%) limit (%)	average (%)	upper (60%) limit (%)
100	168	4214	2	0.01	0.03	0.09
	500	3960	1	0.04	0.07	0.13
	1000	3921	3	0.08	0.12	0.19
	2000	869	1	0.20	0.26	0.35
	4000	830	3	0.41	0.50	0.62
	6000	541	2	0.77	0.89	1.04
	8000	485	2	1.15	1.29	1.47
125	168	6809	4	0.02	0.03	0.07
	500	5992	4	0.07	0.10	0.15
	1000	5900	7	0.15	0.19	0.25
	2000	1753	5	0.35	0.41	0.49
	3000	1540	5	0.63	0.72	0.82
	5000	1374	5	1.00	1.10	1.22
	8000	924	4	1.42	1.55	1.69
140	168	2699	6	0.07	0.12	0.23
	500	1899	1	0.19	0.26	0.40
	1000	1840	2	0.26	0.34	0.49
	2000	1165	2	0.39	0.50	0.66
	3000	1083	5	0.68	0.82	1.01
	5000	1007	6	1.17	1.35	1.58
	8000	642	6	1.90	2.13	2.41
175	168	329	4	0.36	0.67	1.49
	500	245	0	0.92	1.40	2.37
	1000	245	1	1.02	1.53	2.52
	2000	136	0	1.42	2.01	3.09
	3000	96	0	1.42	2.01	3.09
	4000	94	0	1.42	2.01	3.09
	5000	84	1	1.99	2.69	3.85
	6000	27	0	4.08	5.05	6.49
8000	18	0	4.08	5.05	6.49	

APPENDIX 3

Weibull plots of the tested ICs.



ACKNOWLEDGEMENT

The author gratefully acknowledges the contributions of R. Allaire of R.T.C. – La Radiotechnique-Compélec, J. Ingham of Mullard Ltd., and G. Schonk of Philips Nijmegen to the joint exercise reported here.

To provide the collimated laser beams needed in digital-optical recording systems, a semiconductor laser is now available together with its collimating optics combined in a single capsule. The laser's characteristics have been optimised to take full advantage of the optical system which comprises a collimating triplet lens and a cylindrical lens to correct for astigmatism.

Semiconductor laser with collimating optics

L. J. VAN RUYVEN

Digital-optical recording systems store information digitally as a series of pits formed in a spiral track by the modulated beam of a high-power pulse laser. To access the information, a read-out system directs a continuous laser beam at the rotating track, and monitors the variation in intensity produced by interference between incident and reflected beams.

For both read and write applications, semiconductor lasers offer many important advantages over the more conventional helium-neon laser. They are small, highly efficient and require a supply of only a few volts (compared with say 1500 V for the helium-neon laser). And especially when operating in pulse-mode, they are easy to modulate and are capable of producing quite high powers (of around 50 mW).

An earlier article (see Ref.) described a new double-heterojunction semiconductor laser, the CQL10, based on

AlGaAs; and showed how it could be incorporated in a digital-optical readout system. As explained in that article, the CQL10, in common with all semiconductor lasers, produces a strongly divergent beam that must be collimated optically. To spare the user the task of setting up and aligning the collimating system, the CQL10 is now available with collimating optics combined in a single capsule.

This new device, known as the *collimator pen*, has been developed primarily for DRAW (Direct Read After Write) systems, which make use of two parallel, monochromatic light sources of different wavelength – one to write the information, the other to check that the information has been written correctly.

A description of this device, including the way in which the laser characteristics are optimised to take full advantage of the optical system, is the subject of the present article.

Collimator-pen incorporating the CQL10A semiconductor laser



LASER CHARACTERISTICS

The beam emitted by the standard CQL10 is both highly divergent and elliptical in cross section, with a beam divergence of around 60° perpendicular to the active layer, and around 34° in the plane of the layer.

Moreover, the CQL10 being a gain-guided laser, its beam is astigmatic, diverging from a virtual source located 20 to $30\ \mu\text{m}$ behind the emitting window in the plane of the active layer, and from the window itself normal to the layer.

Astigmatism in gain guided semiconductor lasers is caused by the fact that, in these devices, the mechanism for constraining the light beam in the plane of the active layer differs from that in the plane normal to it. In the former case, the light beam is constrained solely by the electric current profile (which creates the conditions for population inversion), whereas in the latter case, it's constrained by internal reflections at the layer boundaries.

Index guided lasers constrain the beam in both planes by internal reflection, so these lasers don't exhibit astigmatism. Their major drawbacks for digital-optical recording, however, lie in their long coherence length, which can give rise to noise (caused by optical feedback), and in the fact that they emit a strongly asymmetric beam.

Optimising laser characteristics

To make full use of the collimating system, the laser should emit a beam of circular cross-section, i.e. with equal far-field angles parallel and perpendicular to the active layer. In gain

guided lasers like the CQL10, this condition is not difficult to approximate.

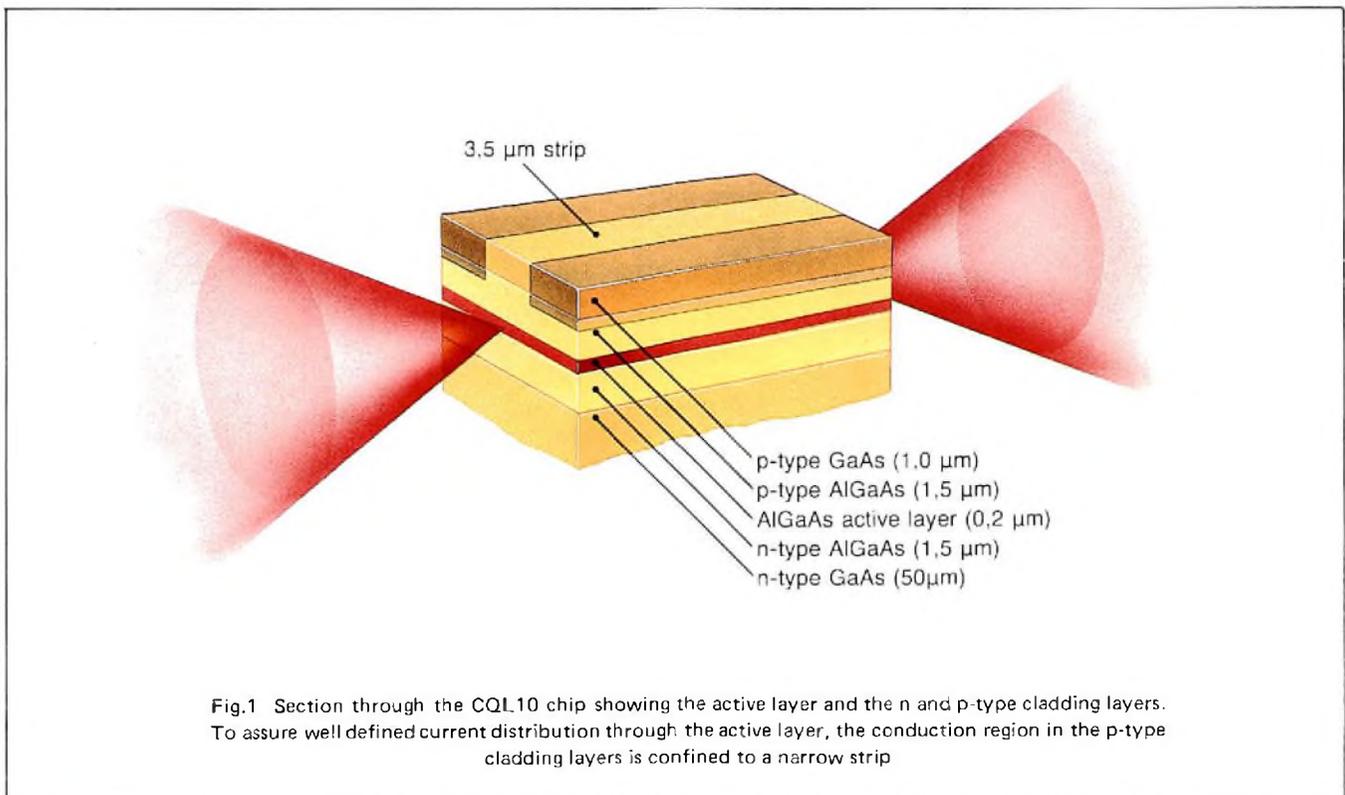
Figure 1 shows the laser chip. The active layer is sandwiched between n-type and p-type cladding layers. To assure precisely defined current flow across the active layer, proton implantation of the p-type layers confines the conduction region to a narrow strip.

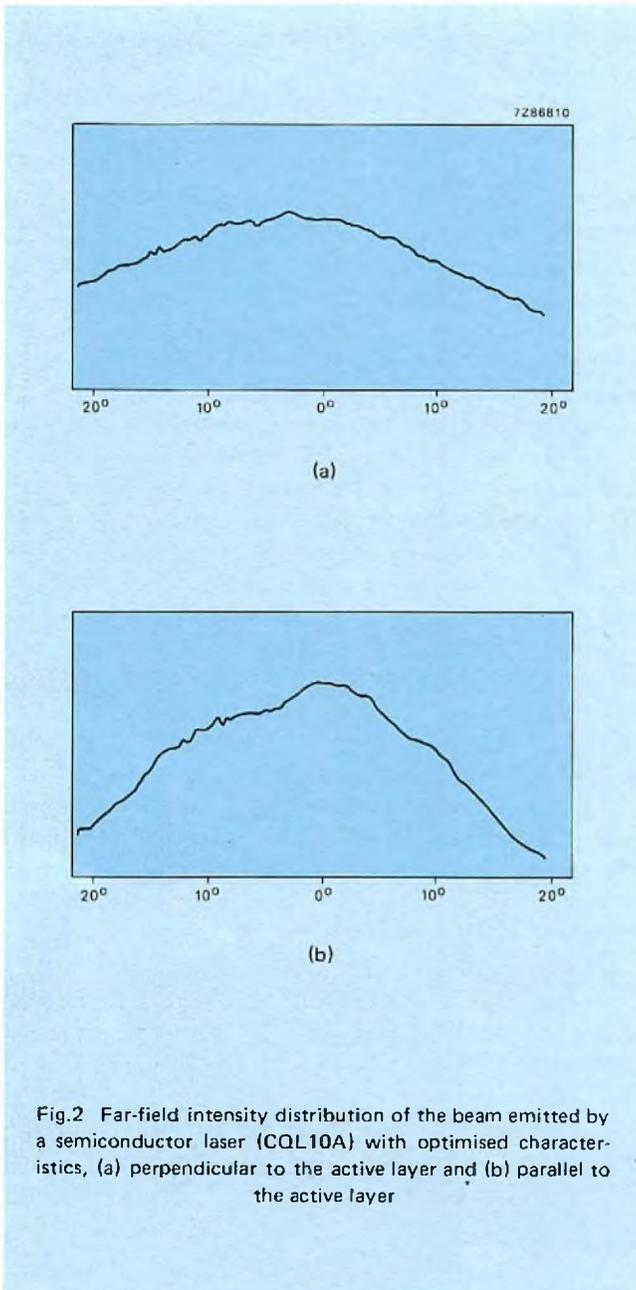
The width of the conduction strip and the degree of current spreading in the p-type cladding layers govern the astigmatic difference (the distance between the principal astigmatic foci). This in turn governs the far-field angles (which increase with decreasing astigmatic difference).

The far-field angles also depend upon the thickness of the active layer. This can be understood by bearing in mind that the active layer is typically around $0.2\ \mu\text{m}$ thick, which is small compared with the emitting wavelength ($0.82\ \mu\text{m}$). So a fraction of the light energy passes through the cladding layers (which have a lower index of refraction than the active layer), thereby narrowing the far-field.

It is therefore possible to adjust the width of the conduction strip, the degree of current spreading in the p-type cladding layers (by adjusting their resistivities), and the thickness of the active layer to give approximately equal far-field angles in the two perpendicular directions.

Figure 2 shows the far-field intensity distribution for a laser with optimised characteristics (designated CQL10A). Although not perfectly circular, the far-field of this new optimised laser is, nevertheless, more than adequate for the requirements of the collimator pen.



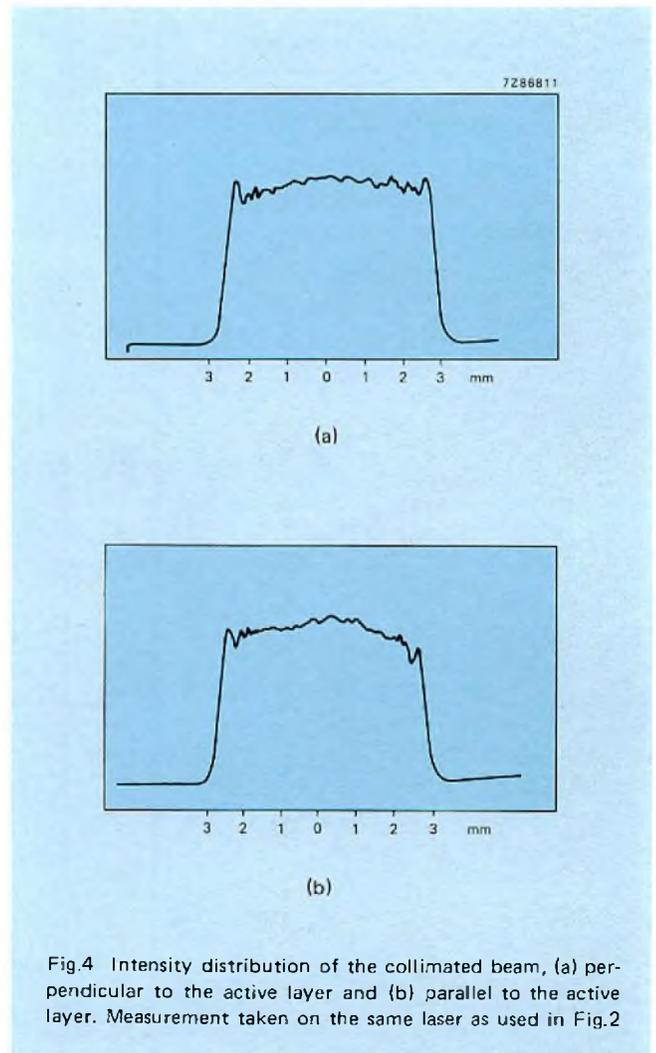
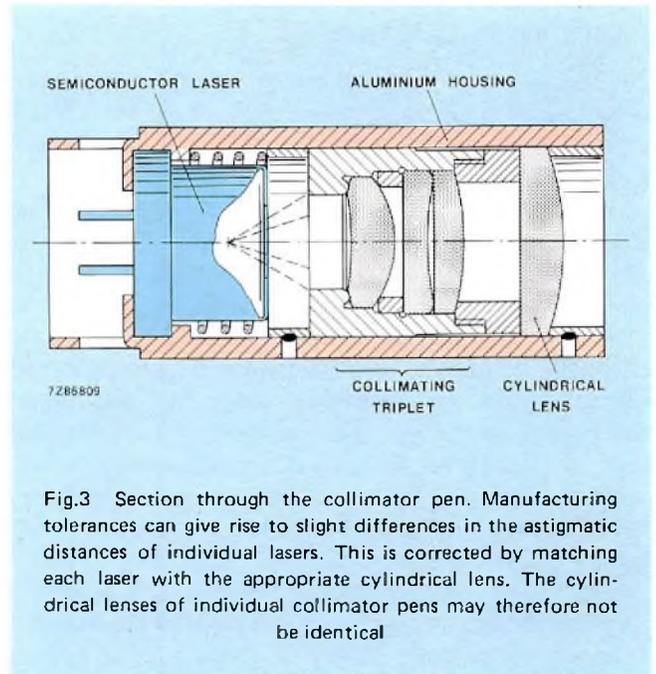


OPTICAL SYSTEM

Figure 3 shows the complete setup, including optics, and semiconductor laser in standard SOT148 encapsulation.

A triplet lens system with a numerical aperture of 0.3 and a quality (wavefront variance relative to the Gaussian sphere) better than $\lambda^2/500$ collimates the divergent beam, and a cylindrical lens corrects for the astigmatism.

Figure 4 shows the intensity distribution of the collimated beam in planes parallel and perpendicular to the active layer. The optics have been optimised for digital-optical recording systems, with a beam diameter of 5.4 mm, a beam divergence better than 0.3 mrad and an optical coupling efficiency of around 50%.



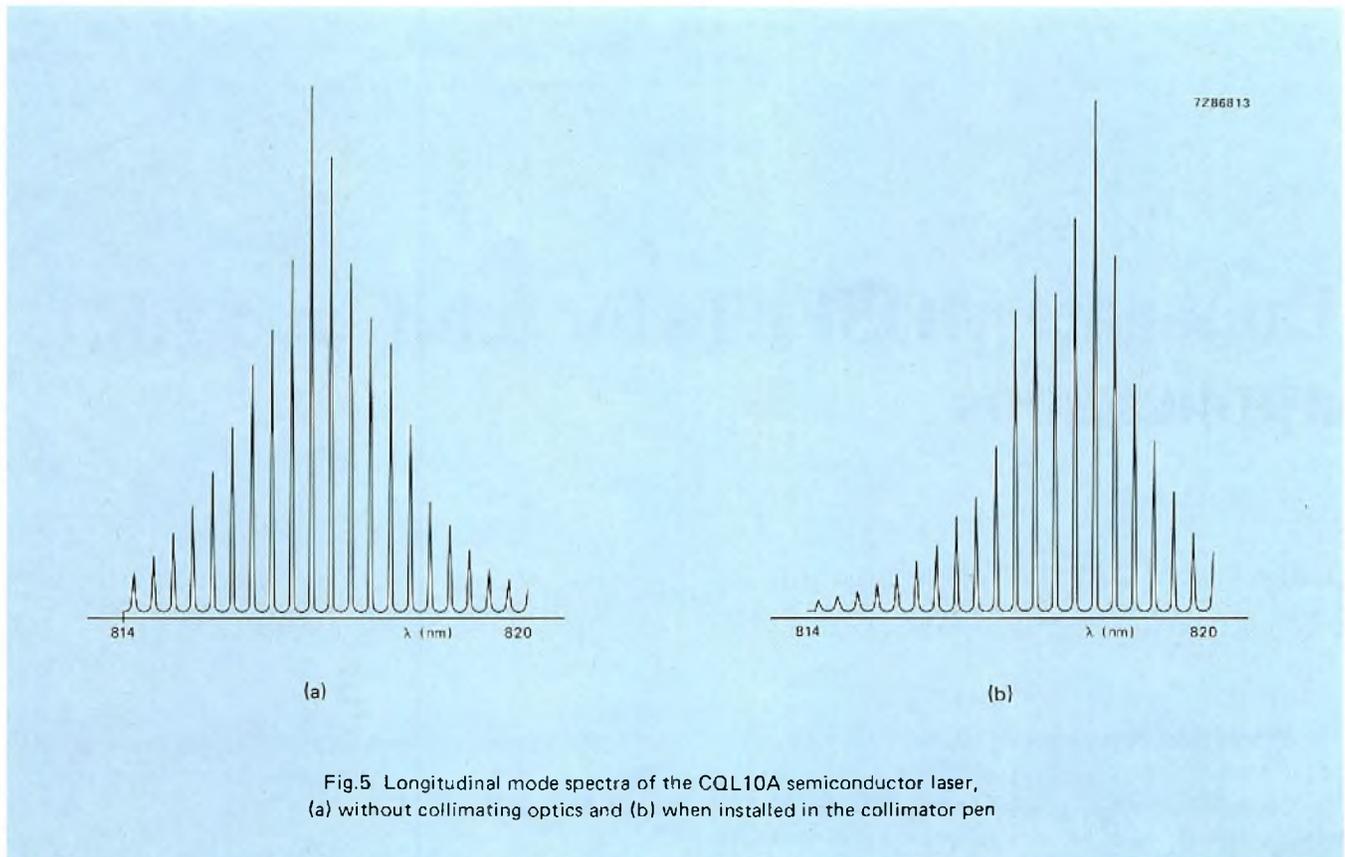


Fig.5 Longitudinal mode spectra of the CQL10A semiconductor laser, (a) without collimating optics and (b) when installed in the collimator pen

Figure 5 shows the longitudinal mode spectra of the basic CQL10A, and of the same laser combined with its collimating optics. The slight shift in wavelength is due to interference effects caused by reflections at the lens surfaces.

At present there are three versions of the collimator pen available for read-out applications — peaking at 790 nm, 820 nm and 870 nm. All have a maximum rating of 2 mW (continuous wave), and an operating temperature range from 10° to 60°C. At maximum rating, their operational life exceeds 2000 hours.

PULSE MODE LASER FOR WRITE APPLICATIONS

Write applications require higher powers than are possible with a continuous laser like the CQL10A. For this reason two versions of the collimator pen are also available with a high-power pulse laser. These devices, which are rated at 20 mW (at 60°C, 10% duty cycle), peak at 820 nm and 850 nm, and have an operational life (at maximum rating) exceeding 1000 hours.

REFERENCE

“CQL10 semiconductor laser for information readout”.
Electronic Components and Applications 3, 2-5 (No.1).

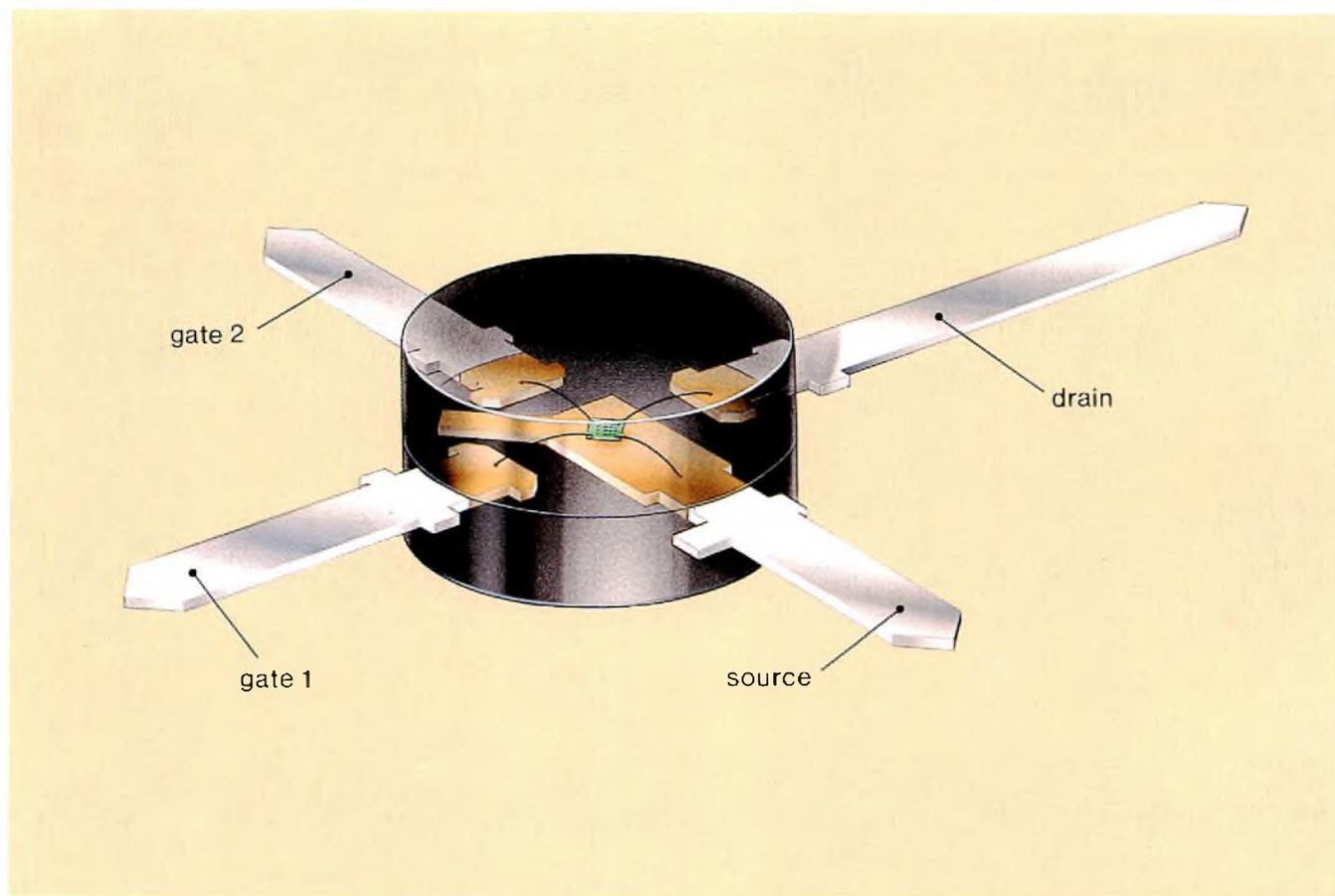
New MOSFETs with pinch-off voltages around -1 V , low output capacitance, high transfer admittance, and low noise are well suited for use in high-quality v.h.f./u.h.f. tuners.

Dual-gate MOSFETs for u.h.f. and v.h.f. applications

J. HOUTHOFF and T.H. UITTENBOGAARD

The BF980 and BF982 dual-gate MOSFETs (Fig.1) are two of the latest devices to take advantage of recent refinements in MOS technology. With pinch-off voltages of around -1 V (compared with -3 to -5 V in former devices), these new

MOSFETs can easily operate from a supply as low as 8.5 V , and can, even at this low supply voltage, provide effective automatic gain-control.



Both devices are intended for use in high-quality u.h.f./v.h.f. tv tuners. The BF980 is primarily a u.h.f. device that can also be used for v.h.f. S-band applications, and the BF982 is a v.h.f. device that is also well suited for use in mixers and in f.m. radios (car radios in particular). Besides the above, the most notable advantages these new MOSFETs offer over former MOS devices are:

- lower output capacitance C_{os} – particularly important for the BF980, making it well suited to uses in v.h.f. tuners with extended frequency bands (S-band tuners)
- higher transfer admittance Y_{fs} (Fig.2) – allowing looser coupling between input filter and r.f. amplifier, further reducing intermodulation and improving first repeat-spot suppression
- lower noise – making it possible to design low noise MOSFET tuners despite the degrading effect inevitably introduced by the tuned input circuitry
- better input and output characteristics – leading to improved selectivity in the bandpass filter between r.f. and mixer stages, and hence to lower cross modulation, and better first repeat-spot suppression and image rejection
- lower spread in pinch-off voltage (Fig.3) and lower spread in a.g.c. characteristics (Fig.4).

TABLE I
Some important data on the BF980/BF982 MOSFETs

	BF980	BF982
max drain-source voltage (V_{DS})	18 V	20 V
max drain current (I_D)	30 mA	40 mA
typical transfer admittance (at 1 kHz)	19 mA/V ¹	25 mA/V ²
typical feedback capacitance (at 1 MHz)	25 fF ¹	30 fF ²
typical input capacitance (at 1 MHz)	2.6 pF ¹	4 pF ²
typical output capacitance (at 1 MHz)	1.1 pF ¹	2 pF ²
gate-source cut-off voltages ³ :		
$-V_{(P)G1-S}$ (at $V_{G2-S} = 4$ V)	<1.3 V	<1.3 V
$-V_{(P)G2-S}$ (at $V_{G1-S} = 0$ V)	<1.1 V	<1.1 V
noise figure	2.8 dB ^{1,4}	1.2 dB ^{2,5}
max power dissipation (at $T_{amb} \leq 75^\circ\text{C}$)	225 mW	225 mW
max junction temperature	150 °C	150 °C

Notes:

1. $I_D = 10$ mA, $V_{DS} = 10$ V, $V_{G2-S} = 4$ V
2. $I_D = 15$ mA, $V_{DS} = 10$ V, $V_{G2-S} = 4$ V
3. $I_D = 20$ μ A, $V_{DS} = 10$ V
4. source conductance = 5 mA/V, $f = 800$ MHz.
5. source conductance = 2 mA/V, $f = 200$ MHz.

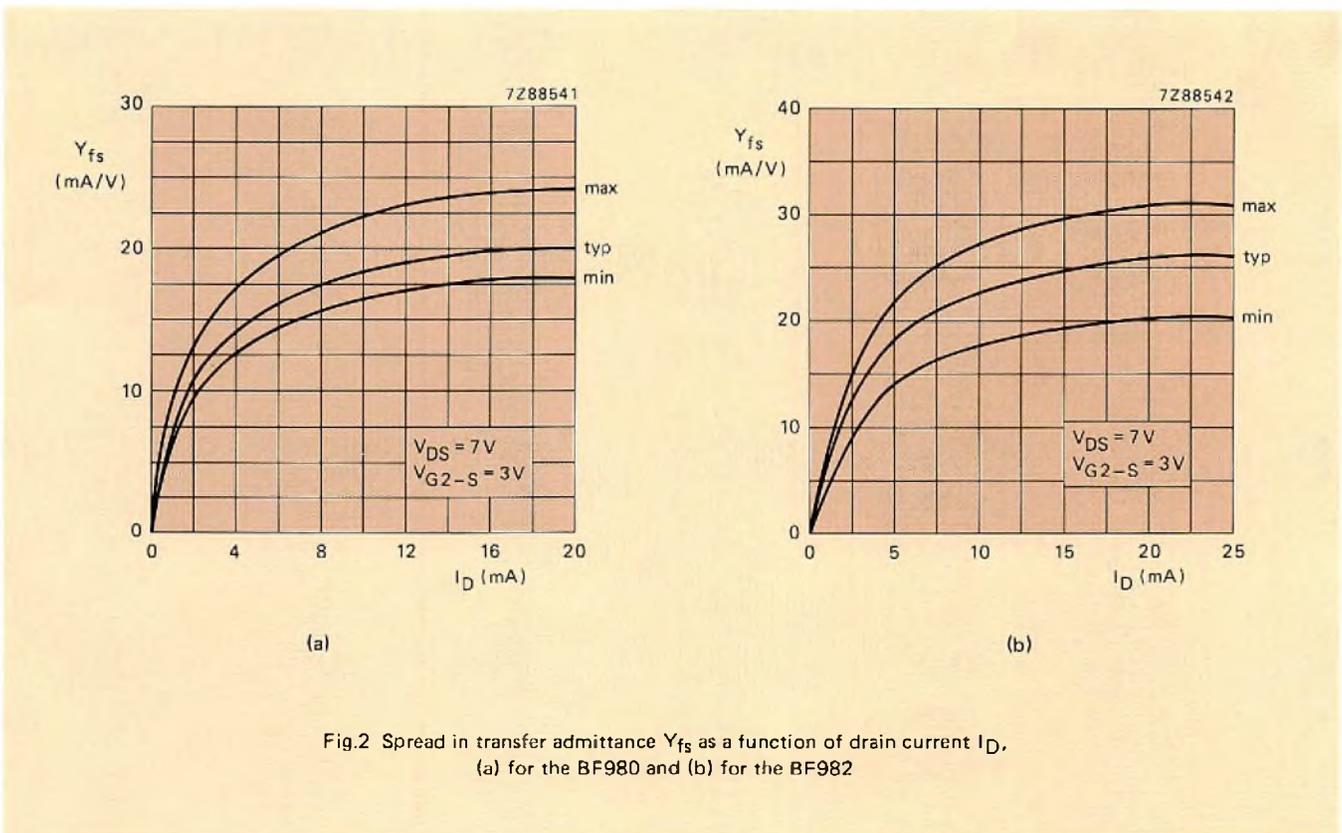


Fig.2 Spread in transfer admittance Y_{fs} as a function of drain current I_D .
(a) for the BF980 and (b) for the BF982

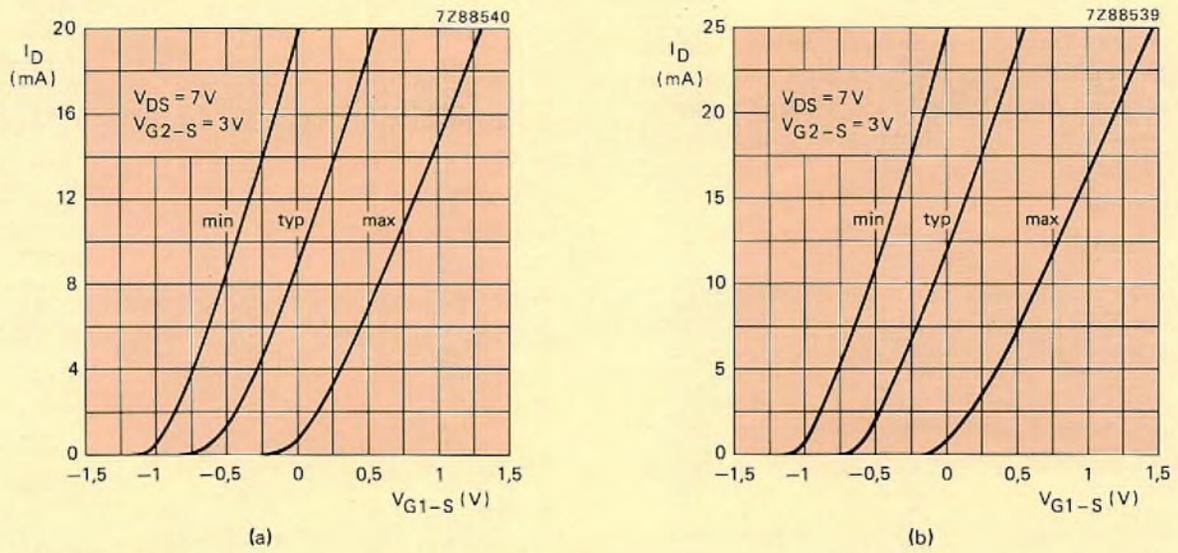


Fig.3 Spread in V_{G1-S} as a function of drain current I_D ,
 (a) for the BF980 and (b) for the BF982

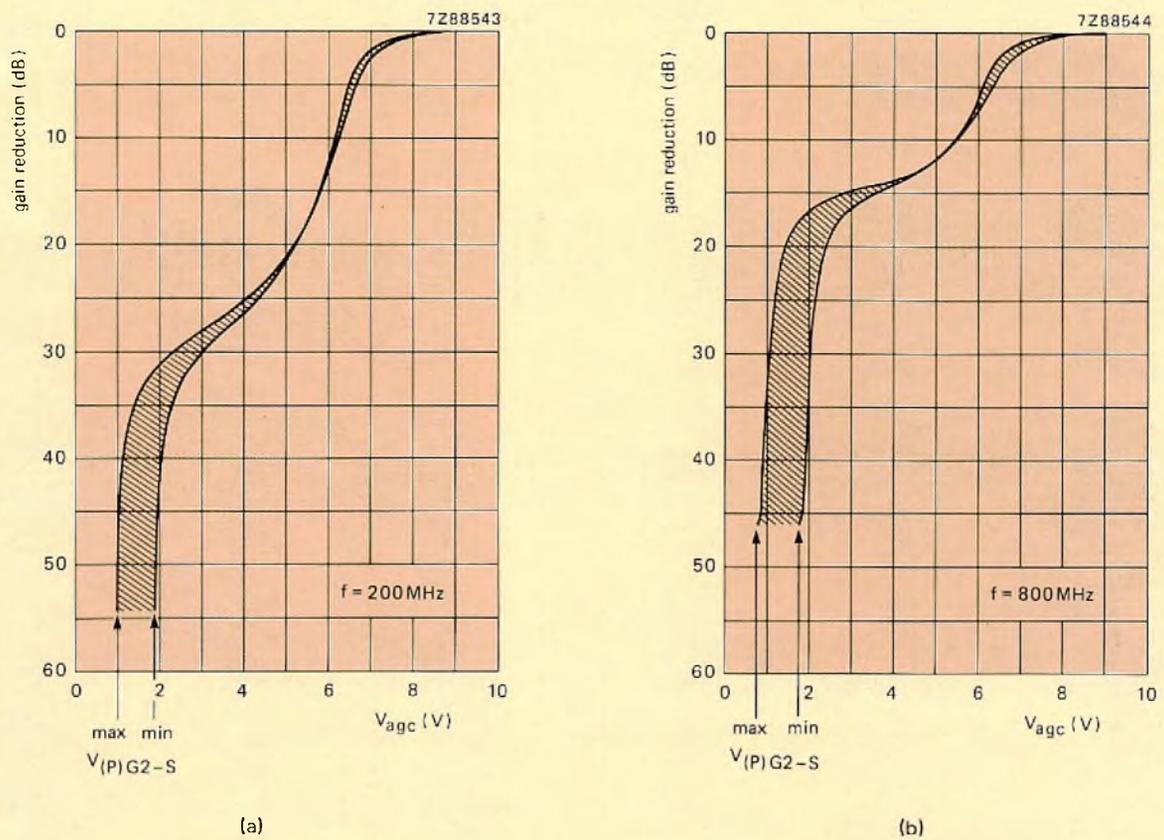


Fig.4 Automatic gain control characteristics and spread in characteristics,
 (a) for the BF982 and (b) for the BF980

MANUFACTURE

The BF980/BF982 MOSFETs are manufactured using the latest MOS production techniques.

After selective shallow p^+ diffusion of the p^- silicon slice and diffusion of the drain and source regions, the slice is covered with phosphorus-doped silicon oxide into which the gates are etched.

The gates are then given a thin oxide layer ($0.053 \mu\text{m}$) in a furnace at 1050°C (first in dry oxygen then in dry nitrogen), after which drain and source contacts are etched through the phosphorus doped oxide.

Then follows aluminium metallisation of the whole slice (to a thickness of $0.9 \mu\text{m}$), selective etching to form the contacts, and annealing in wet nitrogen at 500°C .

Finally, the whole slice is sealed with silicon nitride through which the contact windows are etched.

Performance-governing factors in manufacture

Pattern definition. In the BF980/BF982, improvements in pattern definition, resulting from the use of higher-grade masks, have led to a significant reduction in channel length,

and hence to reduce input capacitance and increased transfer admittance. Formerly, channel lengths of around 2 to $3 \mu\text{m}$ were the norm – in the BF980 channel length has been reduced to between 1.7 and $1.9 \mu\text{m}$. Besides reducing channel length, use of higher-grade masks is a major factor reducing the spread in device characteristics.

Oxide-layer charge Q_{OX} . Given a predetermined channel length and resistivity (of oxide layer), Q_{OX} is the most important factor governing the pinch-off voltage of a MOSFET. With a channel length of say $1.8 \mu\text{m}$, a Q_{OX} of $10^{11} |e|$ (e = electronic charge) gives a pinch-off voltage around -1 V . Experience indicates that a strictly controlled oxidation process in a clean furnace is the best way of assuring low Q_{OX} .

Number of surface states in the channels. The capture and random release of electrons in the channels by surface states between oxide and silicon gives rise to noise. To minimise this noise, the number of surface states must be kept as low as possible. This is assured in the BF980/BF982 by a combination of low Q_{OX} and a well controlled annealing temperature (500°C).

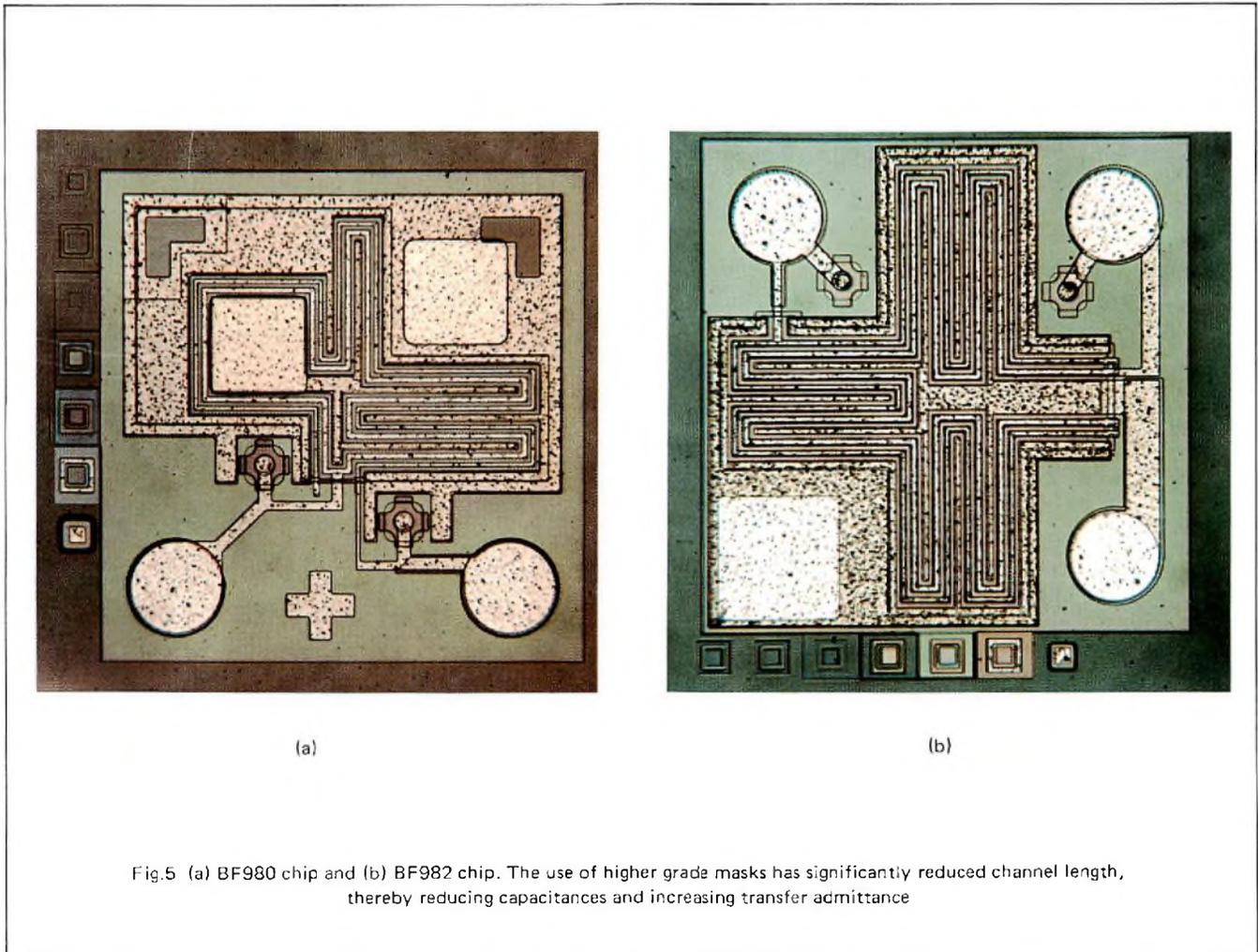


Fig.5 (a) BF980 chip and (b) BF982 chip. The use of higher grade masks has significantly reduced channel length, thereby reducing capacitances and increasing transfer admittance

THE BF980/BF982 IN CIRCUIT

The two circuits described below demonstrate the use of the BF980/BF982 in tuner applications and illustrate their versatility.

Car radio preamplifier using the BF982

One of the major advantages of using dual-gate MOSFETs is the ease with which a.g.c. can be incorporated in the circuit. The BF982 is particularly effective in this respect owing to its low spread in a.g.c. characteristics, allowing the production of preamplifier circuits with highly reproducible a.g.c. performance.

Preamplifier circuit

Figure 6 shows the preamplifier circuit. The most important requirements of a preamplifier are low noise and high stability, as well as good signal handling – which effectively means good selectivity of the tuned input circuit.

This last requirement can be realised by loose coupling between antenna and tuned input circuit, at the cost, however, of increased noise (due to increased losses in the tuned input circuit itself). So to provide a reasonable compromise

between low noise and good selectivity, the tuned input circuit in Fig.6 has been designed with an unloaded bandwidth of 0.93 MHz, and a loaded bandwidth of 2 MHz. This limits the losses in the tuned input circuit to around 2.7 dB.

For high stability, the BF982 is provided with low source resistance by a tapping from the tuned input circuit. This tapping also improves signal handling and reduces the effect of transistor parameter variations (during gain control) on the characteristics of the tuned input circuit. Moreover, in spite of this tapping, which inevitably gives some reduction in gain, the overall gain of the preamplifier will be high thanks to the high transfer admittance of the BF982.

The drain of the BF982 is directly coupled to the output tuned circuit, which has an unloaded bandwidth of 0.81 MHz.

Bandwidth variations in the tuned circuitry are prevented by inductively coupling the antenna and load to the input and output tuned circuits respectively.

A 33 Ω resistor between decoupling capacitor C3 and gate G2 (as close to the latter as possible) suppresses high-frequency parasitic oscillations. Note, for this resistor to be effective, its parasitic capacitance must be as low as possible. This is assured by, for example, locating it well away from earth points in the circuit.

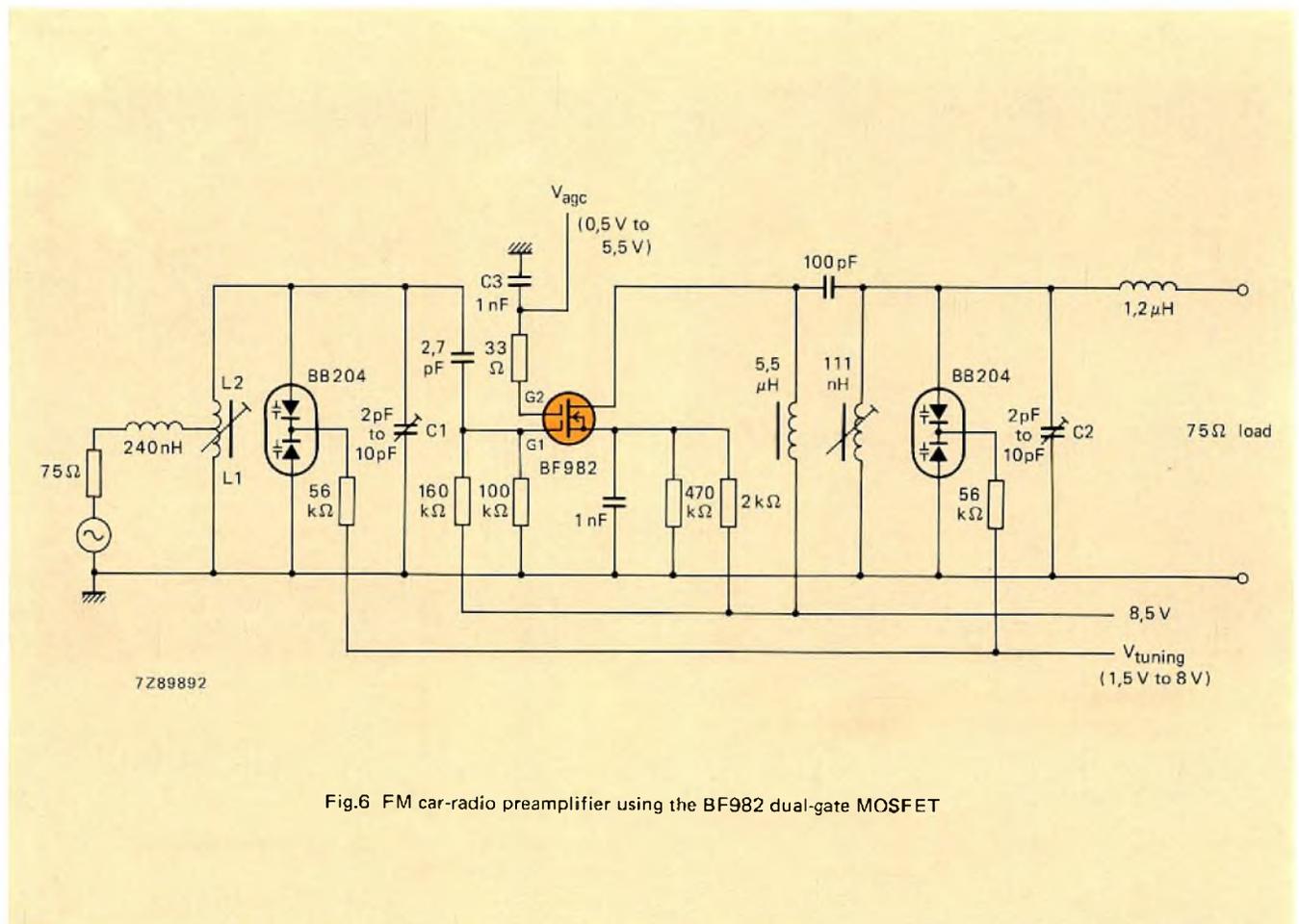


Fig.6 FM car-radio preamplifier using the BF982 dual-gate MOSFET

Preamplifier performance

Figure 7 shows the gain and noise figure of the preamplifier as functions of frequency, and Fig.8 shows the bandwidth. The preamplifier has a gain typically greater than 20 dB between 87 and 105 MHz, and a noise figure less than 4 dB.

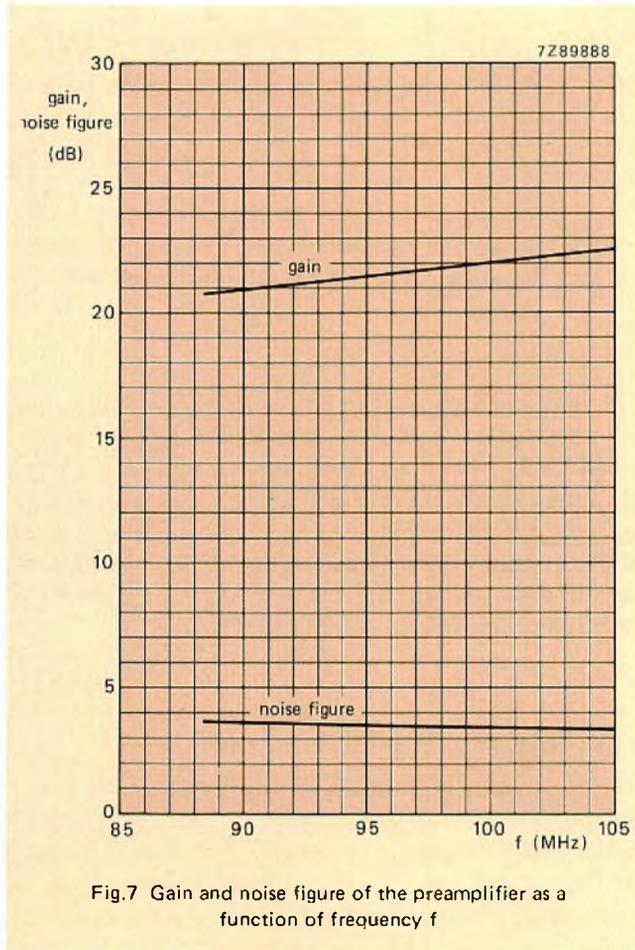


Fig.7 Gain and noise figure of the preamplifier as a function of frequency f

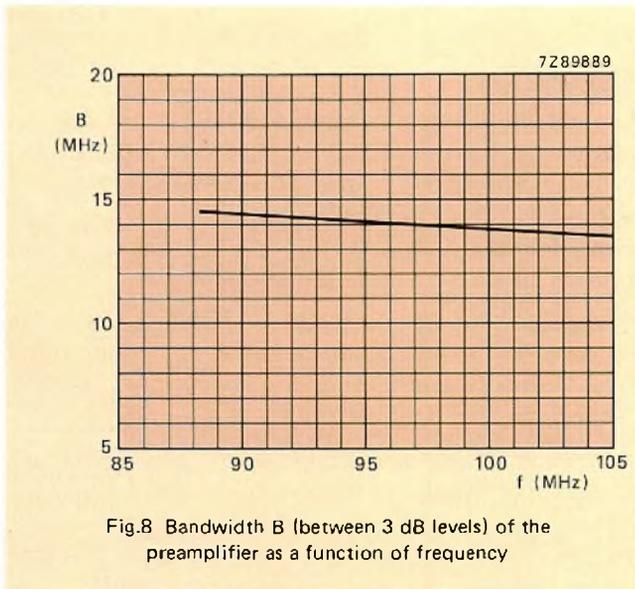


Fig.8 Bandwidth B (between 3 dB levels) of the preamplifier as a function of frequency

Figure 9 gives the a.g.c. characteristics of the preamplifier. The circuit has an a.g.c. range of around 60 dB for an a.g.c. voltage variation between 5.5 V and 0.5 V (maximum gain control).

Finally, Fig.10 shows how gain control affects the bandwidth and tuning (both at 96 MHz).

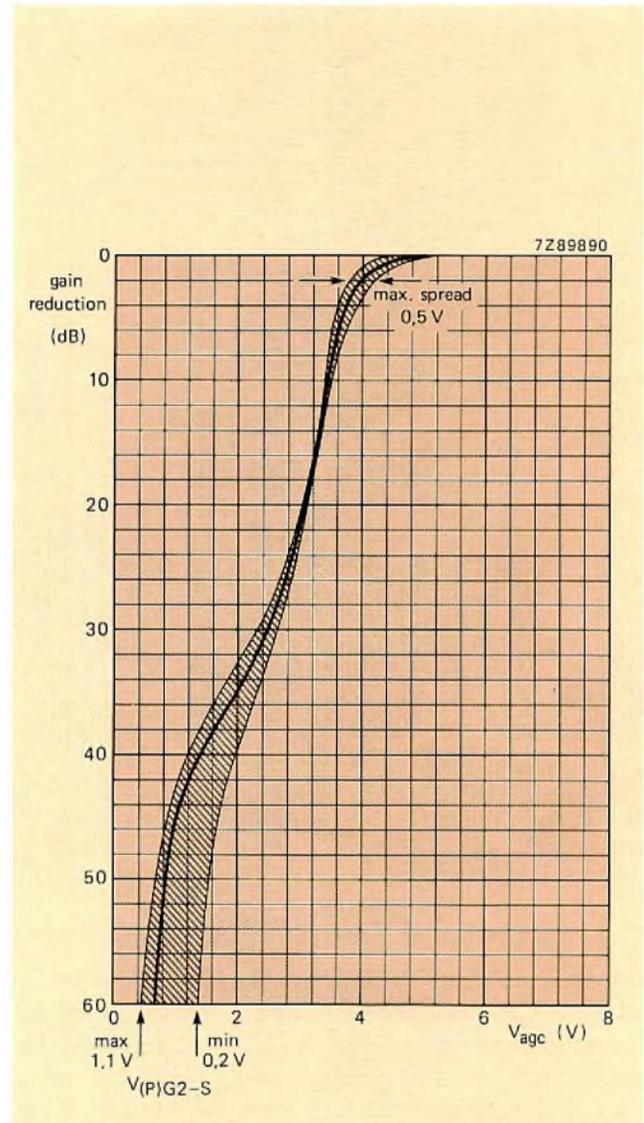
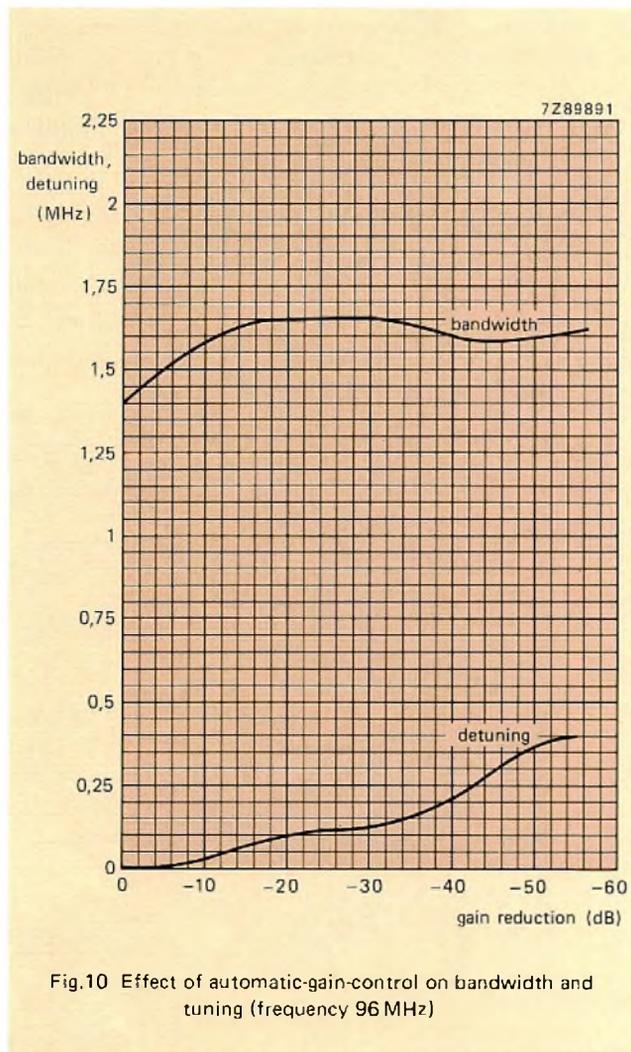


Fig.9 Automatic gain control characteristics of the preamplifier (frequency 96 MHz). The figure shows gain reduction as a function of a.g.c. voltage ($V_{a.g.c.}$) and the spread in characteristics. The figure also shows the corresponding spread in pinch-off voltage $V(P)G2-S$. The amplifier has an a.g.c. range of around 60 dB for an a.g.c. voltage variation between 5.5 V and 0.5 V



12 V u.h.f./v.h.f. tv tuner using the BF980/BF982

With their low drain-source voltage (Table 1) and low pinch-off voltage, the BF980/BF982 are well placed to meet the current demand of tv manufacturers for components that operate from a 12 V supply. Figure 11 shows a 12 V v.h.f./u.h.f. tv tuner circuit using a BF982 and BF980 in the (v.h.f. and u.h.f.) r.f. stages, and a BF982 in the v.h.f. mixer stage. The tuner also uses two bipolar transistors – a BF926 in the v.h.f. oscillator and a BF970 in the u.h.f. mixer/oscillator stage.

v.h.f. section – r.f. stage

Antenna tuned circuit. A tunable input filter, comprising a matching section plus the parallel tuned circuit L7, L8, C6 and D2, improves selectivity and significantly reduces cross-modulation (compared with a corresponding bipolar stage which uses a broadband input filter). Although the losses in the tunable filter are greater than those of a broadband filter, the low noise of the BF982 means that the overall noise of the tuner is considerably less.

For good signal handling, the r.f. amplifier is loosely coupled to the parallel-tuned circuit, via capacitor C13.

r.f. amplifier. The voltage on gate 2 of the BF982 controls the gain of the r.f. amplifier. The a.g.c. characteristic is governed by the source bias and by the nominal drain current I_D . The system provides a control range of about 55 dB for an a.g.c. voltage variation between 9 V and 1 V.

r.f. bandpass filter. An r.f. bandpass filter, between the r.f. amplifier and mixer, is used for channel selection. The filter, which comprises L10, L11, L13 and L14 tuned by C16, D4 and C23, D5, uses inductive foot coupling for both bands (L12 for band I and L16 for band III), and includes a correction capacitor C19 to compensate, at least partially, for changes in bandwidth incurred when tuning over band III.

v.h.f. section – mixer stage

The tuner employs additive mixing. The r.f. and local oscillator signals are applied to gate 1 of the BF982 mixing MOSFET Tr2. The drain current is set at about 2.5 mA, and to assure high conversion gain and good first repeat-spot suppression, the oscillator voltage at gate 1 is set between 300 and 500 mV by means of C31. The i.f. is coupled out via the tuned circuit L18, C28, the oscillator signal at the i.f. output being filtered out by L20.

v.h.f. section – local oscillator stage

The local oscillator uses a silicon pnp BF926 transistor Tr3. L24 and C32 form a feedback loop that behaves capacitively in both bands. The tank circuit comprises L22, L23 tuned by D8 and C37, the capacitor facilitating tracking of the r.f. and oscillator frequencies. The oscillator combines excellent mixer drive properties with low shift and drift.

u.h.f. section – r.f. stage

A tunable input filter, comprising L27, D11, C41 and C42, matches the input impedance of the BF980 MOSFET Tr4 to the antenna. Gate 1 of BF980 is provided with a variable tapping at the junction of D11 and C42, coil L28 being included to compensate for loss of gain at the top end of the band incurred as a result of this tapping.

r.f. amplifier. The a.g.c. of the BF980 MOSFET operates in the same way as that described in the v.h.f. section. The circuit provides a control range of at least 35 dB.

r.f. bandpass filter. The r.f. bandpass filter comprises L31 and L33, tuned by D12 and D13, plus a common earth path on the print board (providing inductive foot coupling). Capacitor C50 in combination with L32 improves image rejection, whilst L29 and C47, tuned to about 400 MHz facilitate matching between the filter and the BF980.

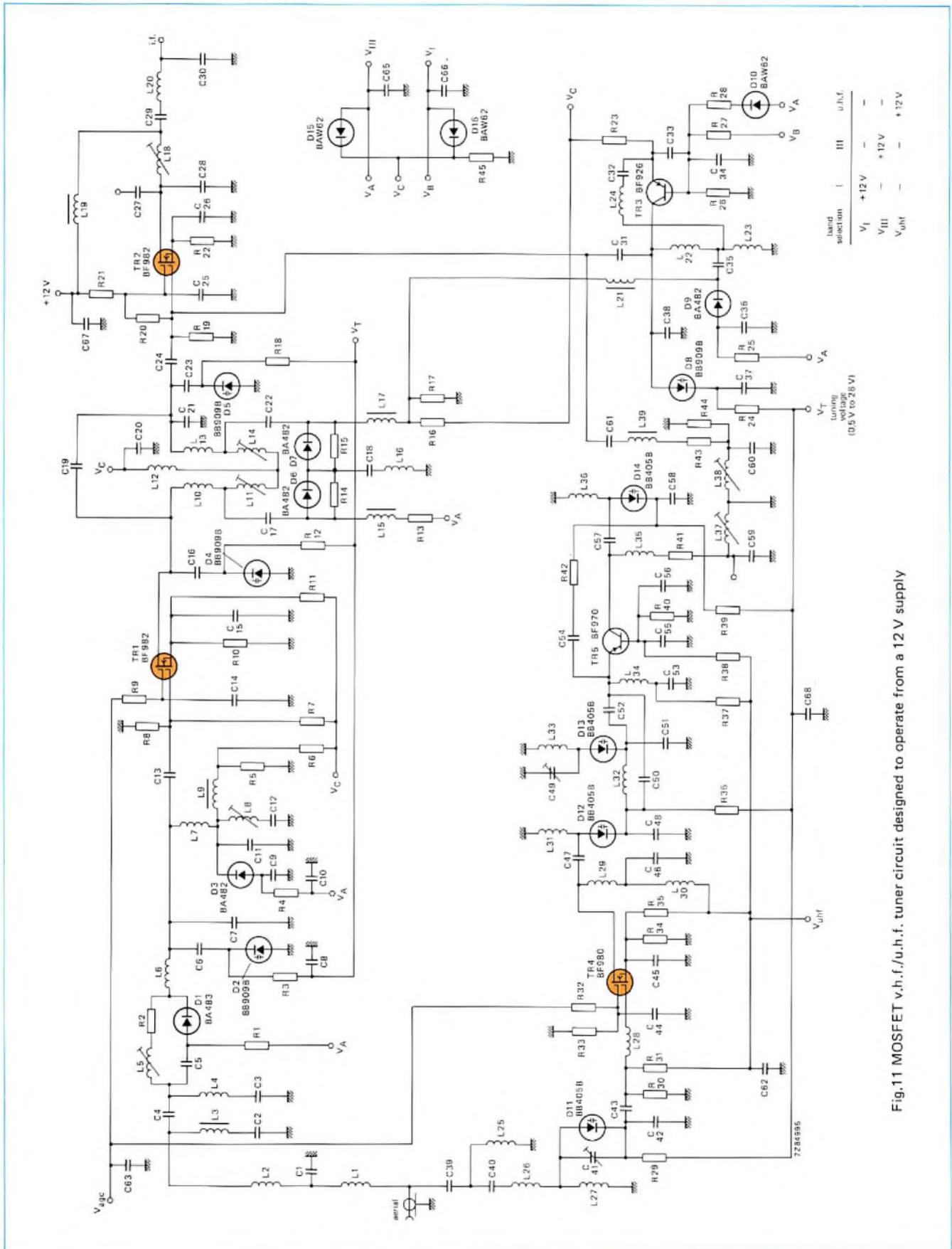


Fig.11 MOSFET v.h.f./u.h.f. tuner circuit designed to operate from a 12 V supply

u.h.f. section – mixer-oscillator stage

A BF970 pnp transistor Tr₅ operates as the u.h.f. mixer-oscillator. The tank circuit comprises L₃₆, D₁₄ and C₅₈, and the feedback loop comprises C₅₄ and R₄₂.

The series resonant circuit L₃₄, C₅₃ provides the mixer with low i.f. input impedance. The i.f. signal is tapped off via L₃₅, R₄₁ and the i.f. bandpass filter L₃₇, L₃₈ (inductively coupled), and passes to the input of the v.h.f. mixer Tr₂ which acts as an additional i.f. amplifier at u.h.f.

Tuner performance

Tables 2 and 3 summarise the performance of the v.h.f. and u.h.f. sections, and Table 4 gives the cross-modulation performance of the tuner. Unless otherwise stated, the figures apply to the tuner operating with a 12 V supply, at nominal gain and at an ambient temperature of 25 °C.

TABLE 2
Summary of tuner performance – v.h.f. section

	E ₂	E ₃	E ₄	C	E ₅	E ₇	E ₉	E ₁₁	E ₁₂
tuning voltage (V)	2.7	4.9	7.1	21.2	8.8	10.8	13.4	18.1	23.7
power gain (dB)	26	28	30	33	27.5	28.5	29.5	30	30
noise figure (dB)	4.3	4.1	3.9	4.2	4.0	3.8	3.7	3.7	3.8
a.g.c. range (dB)	>55	>55	>55	>55	54	53	53	53	53
vswr									
centre frequency	1.8	1.8	1.9	1.9	1.7	1.7	1.6	1.7	1.7
picture carrier	2.3	2.1	1.9	1.6	2.2	2.1	1.8	1.7	1.8
i.f. rejection at picture carrier (dB)	54	64	70	78	>80		>80		>80
image rejection (dB)	84	82	77	83	80	78	85	88	79
pulling (dBμV)	93	89	85	80	88	87	80	82	85
1st repeat-spot rejection (dBμV)	>100		>100		96		96		
shift (kHz)									
V _B + 5%	-16	-113	-97	-89	-121	-133	-74	-8	+4
V _B - 5%	+32	+126	+111	+90	+125	+119	+34	+20	-6
drift from 25 to 40 °C (kHz)	+109	+24	+47	+147	-91	-103	-94	-26	+53

TABLE 3
Summary of tuner performance – u.h.f. section

	474 (MHz)	500 (MHz)	550 (MHz)	600 (MHz)	650 (MHz)	700 (MHz)	750 (MHz)	800 (MHz)	858 (MHz)
tuning voltage (V)	1.0	2.0	4.3	6.8	9.2	11.6	14.2	17.4	23.2
power gain (dB)	32	31.5	30	29.5	29	29	29.5	30	30.5
noise figure (dB)	5.6	5.5	6.0	6.3	6.9	7.0	6.8	6.8	6.9
a.g.c. range (dB)	53	51	50	56	57	54	48	46	46
vswr	<3	<3	<3	<3	<3	<3	<3	<3	<3
i.f. rejection (dB)	>80	>80	>80	>80	>80	>80	>80	>80	>80
image rejection (dB)	58	60	62	58	56	53	52	51	56
pulling (dBμV)		84		80		81			75
1st repeat-spot rejection (dBμV)		85		87		86		80	
N+4 interference (dBμV)		91		90		92		88	
N-4 interference (dBμV)		83		81		79		77	
shift (kHz)									
V _B + 5%	-341	-120	-165	-54	+9	-185	-473	-431	-192
V _B - 5%	+302	+117	+159	+52	-25	+162	+455	+400	+122
drift from 25 to 40 °C (kHz)	-139	-339	-180	-310	-428	-274	+107	+207	-165

TABLE 4
In-channel and in-band cross modulation of the tuner

wanted signal	unwanted signal	in-channel cross-mod.		in-band cross-mod.	
		at nom gain (dB μ V)	40 dB a.g.c. – v.h.f. 30 dB a.g.c. – u.h.f. (dB μ V)	at nom gain (dB μ V)	40 dB a.g.c. – v.h.f. 30 dB a.g.c. – u.h.f. (dB μ V)
v.h.f. section					
VC of E ₂	SC of E ₂	72	101		
VC of E ₃	SC of E ₃	71	103		
VC of E ₅	SC of E ₅	74	106		
VC of E ₉	SC of E ₉	74	112		
VC of E ₁₂	SC of E ₁₂	72	107		
E ₂	E ₄			103	110
E ₄	E ₂			101	110
E ₅	E ₈			94	113
E ₉	E ₁₂			91	117
E ₉	E ₆			93	117
E ₁₂	E ₉			93	118
u.h.f. section					
VC of E ₂₁	SC of E ₂₁	70	98		
VC of E ₃₈	SC of E ₃₈	70	94		
VC of E ₆₉	SC of E ₆₉	69	88		
E ₂₁	E ₂₆			95	107
E ₃₈	E ₄₃			95	98
E ₃₈	E ₃₃			98	100
E ₆₉	E ₆₄			93	94

TABLE 5
Our complete range of dual-gate MOSFETs for v.h.f./u.h.f.

SOT-103	SOT-143	application area
BF960	BF989	u.h.f. } 1st generation
BF981	BF991	v.h.f. }
BF966	BF996	u.h.f. } 2nd generation
BF964	BF994	v.h.f. }
BF980	BF990	u.h.f. } special properties
BF982	BF992	v.h.f. } described in this article

ACKNOWLEDGEMENT

The authors wish to acknowledge the work of Messrs L. Bruntink and G. van Werven, who were responsible for developing the tv tuner circuit described in this article.

The vision i.f. circuits are at the heart of a tv receiver and play a very important role in its overall performance. The TDA3540 and TDA3541 perform all of the functions between the tuner i.f. output and the video amplifier with a standard of performance hitherto unobtainable with integrated circuits.

One IC and a SAW-filter in a high-performance vision i.f. channel

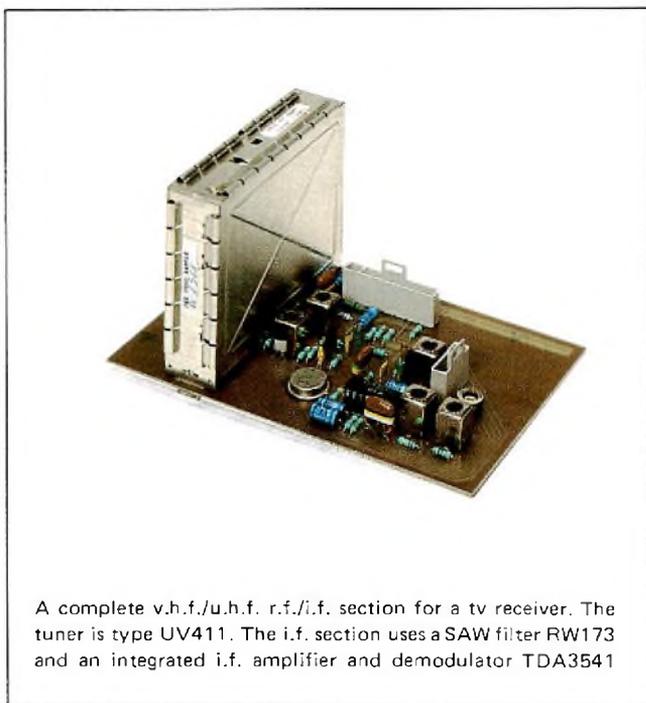
P. J. M. SIJBERS and J. ZEELLEN

The vision i.f. circuits are at the heart of a tv receiver and play a very important role in its overall performance. The TDA3540 and TDA3541 perform all of the functions between the tuner i.f. output and the video amplifier with a standard of performance hitherto unobtainable with integrated circuits.

The TDA3540 and TDA3541 are higher-performance, pin-compatible successors to the tv vision i.f. and demodulator integrated circuits TDA2540 and TDA2541. They are suitable for all classes of tv receiver from black-and-white to high-quality colour. The two circuits are

identical except that the TDA3540 provides increasing a.g.c. voltage for tuners with npn r.f. stages and the TDA3541 provides decreasing a.g.c. voltage for tuners with pnp or MOSFET r.f. stages. The new circuits perform the same functions as their predecessors but, for optimum performance, they require different external components and incorporate the following improvements:

- intermodulation reduced
- a.f.c. and a.g.c. performance improved
- input sensitivity increased to $60\mu\text{V}$ at 38.9 MHz for onset of a.g.c.
- i.f. bandwidth increased. The input sensitivity for onset of a.g.c. at 45.75 MHz is only 1 dB less than that at 38.9 MHz
- the video switch input is now CMOS compatible and can be activated by either a high voltage level (10.9 V min) or a low voltage level (1.5 V max)
- maximum crystal temperature increased to 150°C .



Typical brief data for the TDA3540 and TDA3541

i.f. gain control range	64 dB
signal-to-noise ratio ($V_{in} = 10\text{ mV}$)	58 dB
intermodulation at 1.1 MHz	-60 dB
slope of a.f.c. characteristic	140 V/MHz
video output level (top sync)	3 V
video output amplitude (white to top sync)	2.7 V
input sensitivity at 38.9 MHz for onset of a.g.c.	$60\mu\text{V}$

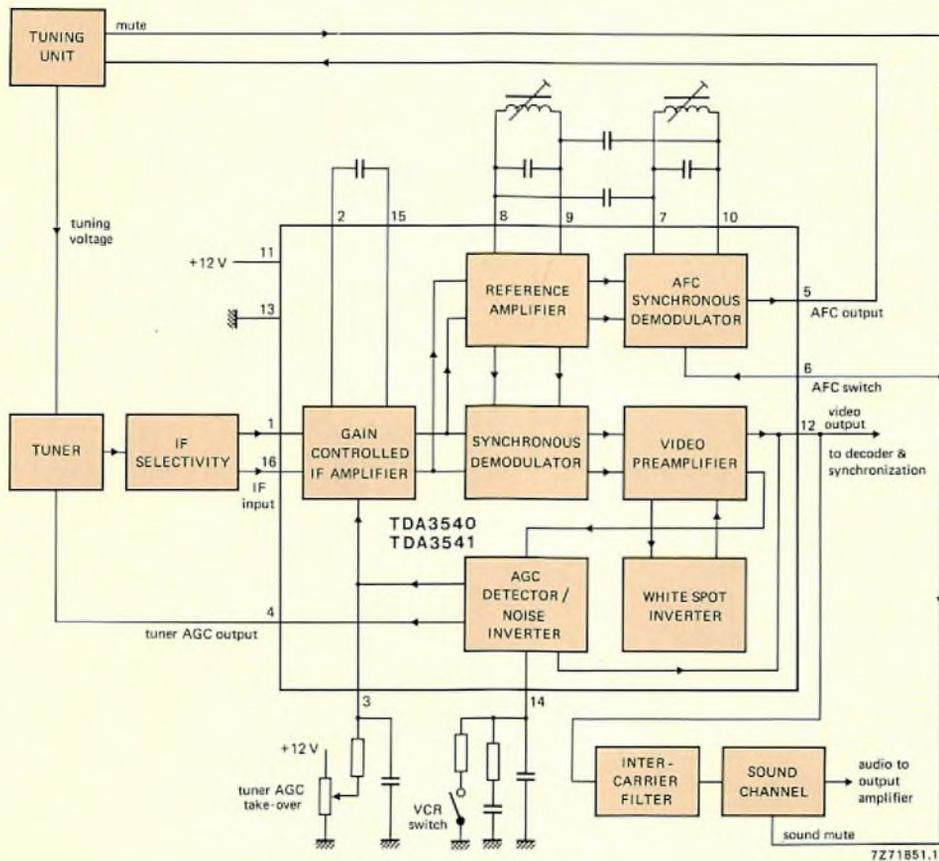


Fig.1 Block diagram of the TDA3540 and TDA3541

Figure 1 is a block diagram of the circuits. For more comprehensive information, refer to the data sheets and to Ref.1.

A PRACTICAL CIRCUIT USING THE TDA3541

Figure 2 is the circuit diagram of a complete front-end for a tv receiver. Since the UV411 is a v.h.f./u.h.f. tuner with MOSFETS in the r.f. stages, the TDA3541 is used as the i.f. circuit because it generates positive-going a.g.c. current at pin 4 for conversion into a negative-going control voltage for the tuner. The bandpass characteristic of the front-end is defined by a surface acoustic wave (SAW) filter type RW173 which replaces the conventional LC circuits, thereby improving the amplitude and group delay characteristics, reducing the size of the circuit and simplifying alignment. To maintain the sensitivity and signal-to-noise ratio of the tuner, the insertion loss of the SAW filter is compensated by an i.f. preamplifier using a discrete transistor type BF370 (see Ref.2). The mixer output is coupled to the preamplifier via a double-tuned bandpass filter. A 40.4MHz notch filter is included at the input to the preamplifier to

meet the signal handling requirements of the German post office. An intercarrier sound trap is incorporated at the video output from the TDA3541. The performance of the circuit is as follows.

Sensitivity

The sensitivity of the front-end is $12 \mu\text{V}$ e.m.f. from a 75Ω source for the onset of i.f. a.g.c. action. The signal levels at other points in the circuit at the onset of tuner a.g.c. and when the amplitude of the composite video output is 2.7 V (3 V to 5.7 V) at maximum gain are given in Fig.3.

Signal-to-noise ratio

The signal-to-noise ratio of the front-end as a function of aerial e.m.f. is shown in Fig.4. The signal-to-noise ratio is defined as:

$$S/N = 20 \log \frac{V_{0(b-w)}}{V_{\text{noise(rms)}}$$

where $V_{0(b-w)}$ is the black-to-white amplitude ($0.65 \times 3 \text{ V} = 1.95 \text{ V}$). The noise bandwidth is 5 MHz .

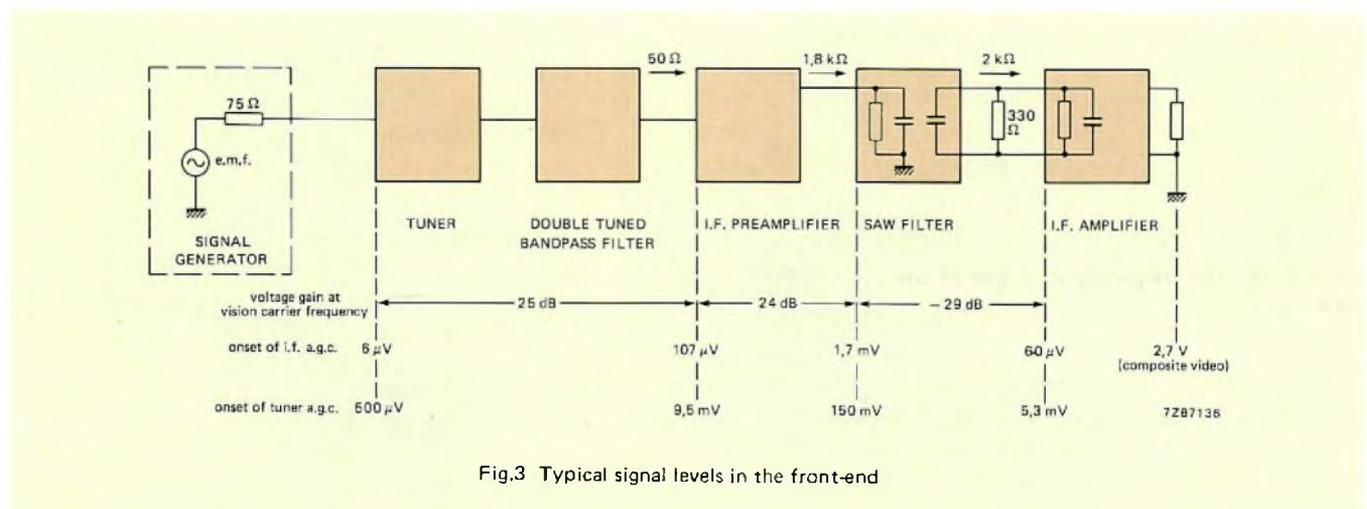
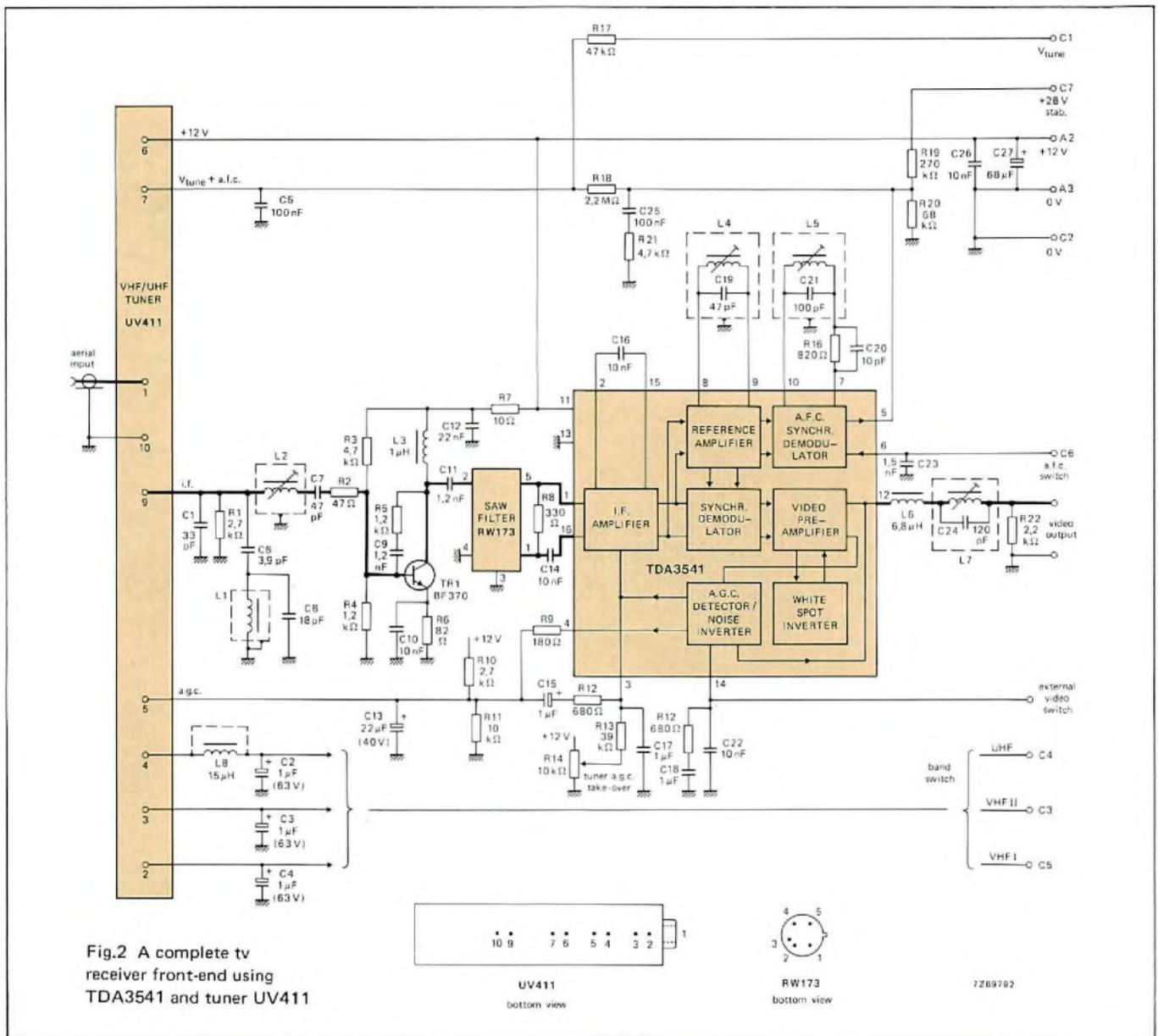


Fig.3 Typical signal levels in the front-end

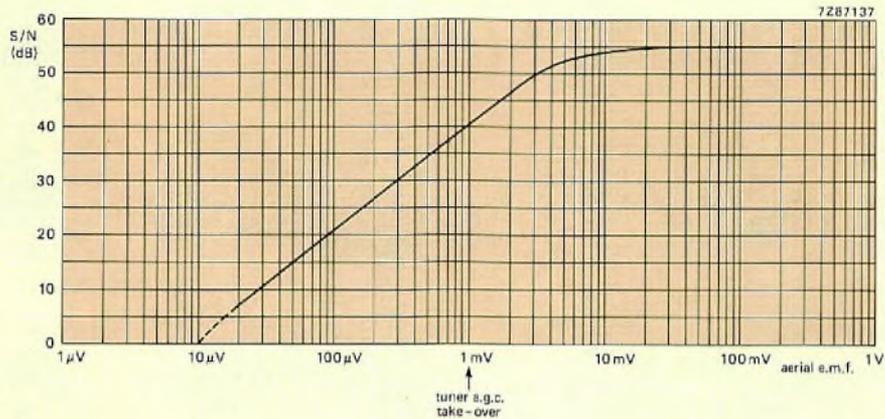


Fig.4 Signal-to-noise ratio as a function of the aerial e.m.f. on channel 5

Noise contributed by the i.f. section of the circuit

Figure 5 shows that the performance of the TDA3541 is not the limiting factor for the overall signal-to-noise ratio of the front-end. The integrated circuit alone gives a signal-to-noise ratio of more than 60dB at the end of the a.g.c. range. The noise contribution of the i.f. amplifier is only 0.5 dB.

Bandpass response

The bandpass response of the front-end is shown in Fig.6. Curves (a) and (b) were measured on v.h.f. band III channel 5 between the aerial input of the tuner and the reference amplifier tuned circuit at pins 8 and 9 of the TDA3541. Curve (c) is the overall video response measured on u.h.f. channel 30.

A.G.C. characteristics

The tuner and i.f. amplifier a.g.c. characteristics are shown in Fig.7. To meet the requirements of the German post office (Amtsblatt 69/1981 item 5.1.2. "Eingang-Storfestigkeit"), tuner a.g.c. take-over is set to occur with an aerial input of 1 mV e.m.f. from a 75 Ω source. The change of tuner output level after tuner a.g.c. take-over (i.f. slip) is about 2 dB. The frequency response of the a.g.c. system is shown in Fig.8.

A.F.C. catching and holding ranges

The a.f.c. catching and holding ranges in the Table were measured with a standard pulse and bar modulated aerial input signal with a top sync level of 1 mV e.m.f. from a 75 Ω source. The picture to sound carrier ratio was 10 dB.

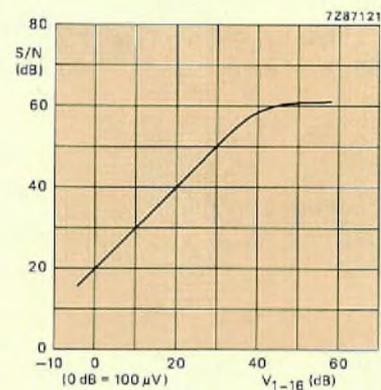


Fig.5 Typical signal-to-noise ratio of the TDA3540 and TDA3541

channel	a.f.c. holding and catching ranges				correction factor
	holding range (MHz)		catching range (MHz)		
	+	-	+	-	
4	0.40	0.40	0.40	0.40	11
5	1.0	1.1	1.0	1.0	30
9	0.8	0.8	0.8	0.8	21
30	2.5	2.4	1.8	1.2	70
40	3.3	3.1	1.6	1.1	90
60	1.9	2.0	1.8	1.2	50

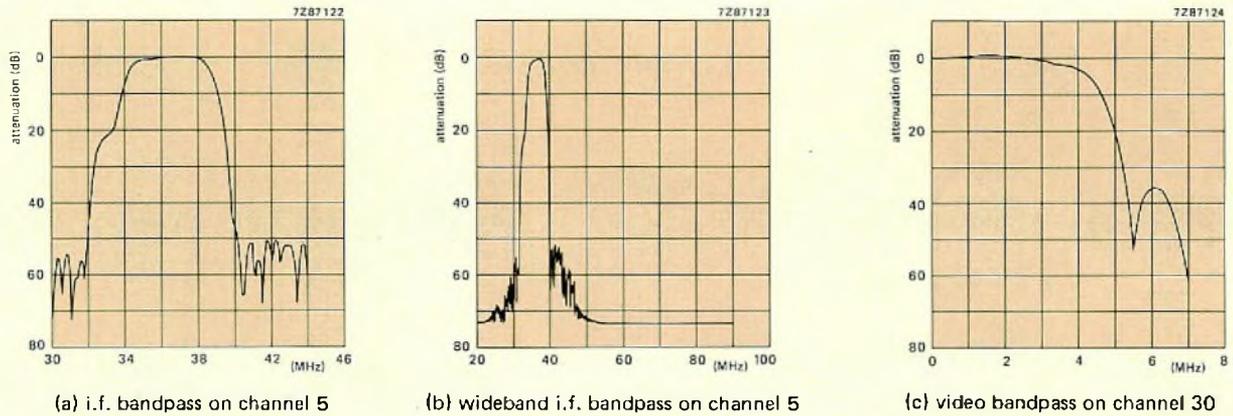


Fig.6 Bandpass characteristics

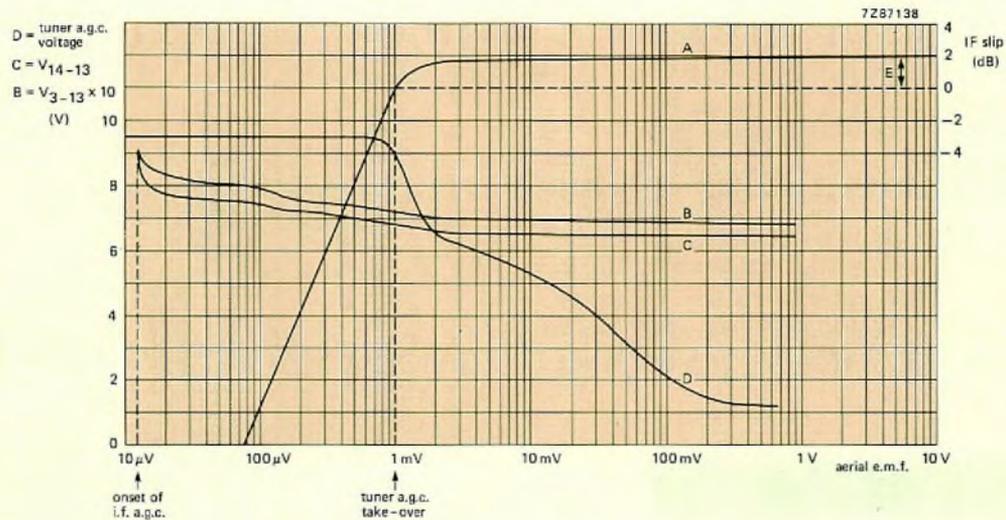


Fig.7 A.G.C. characteristics. Curve A is the output from the video preamplifier. Curve B is the i.f. a.g.c. voltage at pin 3. Curve C is the a.g.c. voltage at pin 14. Curve D is the tuner a.g.c. voltage. E is the i.f. slip

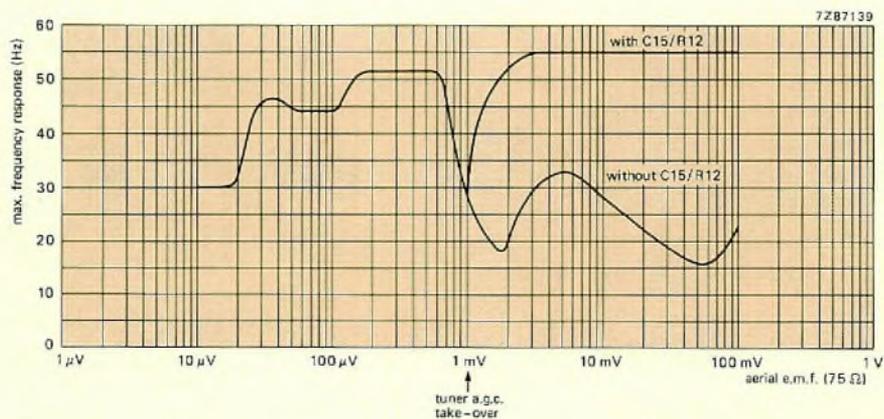
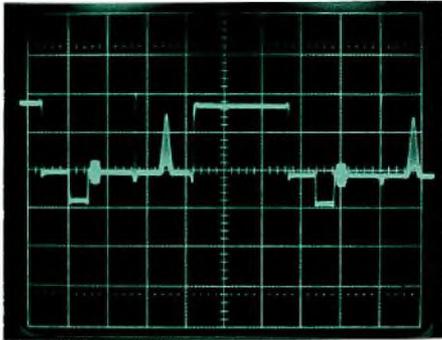
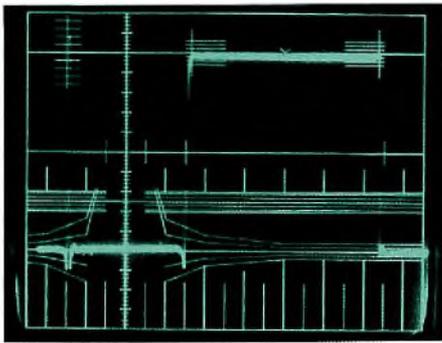


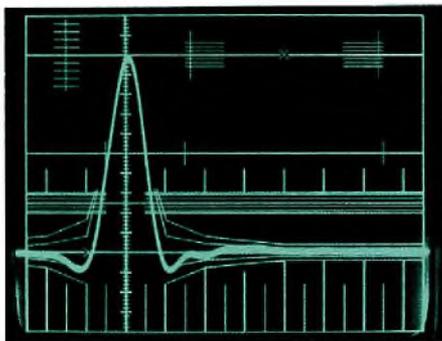
Fig.8 Frequency response limit of the a.g.c. system to an r.f. signal with sinewave amplitude modulation $m = 0.33$ (aircraft flutter)



(a) 2T + 20T pulse and bar modulation.
Horizontal scale 10 μ s/div



(b) 2T pulse and bar response with
superimposed k-rating graticule



(c) 2T pulse response with
superimposed k-rating graticule

Fig.9 Video output signals

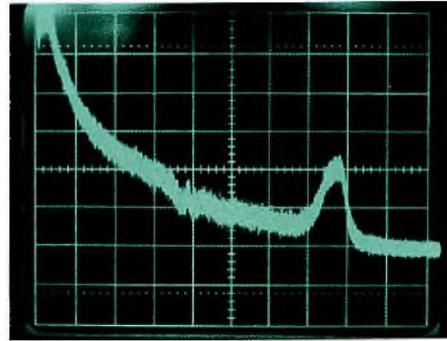


Fig.10 Noise spectrum at the video output.
Vertical scale 10 dB/div, horizontal scale 10 MHz/div

Video response

The video output signal obtained when the input vision carrier is modulated with a 2T + 20T pulse and bar is shown in Fig.9(a). Figures 9(b) and (c) show the video response to a 2T pulse and bar with a superimposed k-rating graticule. In Fig.9(c), the k-factor is about 2%.

Stability

If the circuit is stable, the noise spectrum at the video output decays smoothly with increasing frequency and is free of subharmonics of the i.f. The stability of the circuit can therefore be checked by analysing the noise spectrum at the video output. The noise spectrum at the video output, as displayed on a spectrum analyser, is shown in Fig.10. Good stability is indicated by the lack of subharmonics of the carrier frequency. Stability can also be checked by verifying that the signal-to-noise ratio at low signal levels is proportional to the input signal.

REFERENCES

1. "TV vision i.f. and demodulator circuits TDA3540 and TDA3541" Philips Technical Publication 057, ordering code 9398 039 30011.
2. "BF370 transistor in a surface-acoustic-wave (SAW) filter preamplifier" Philips Technical publication 018, ordering code 9398 018 70011.

Abstracts

Non-linear resistors for protection of electronic telephone equipment

Increasing use of electronics in telephone equipment creates new protection requirements that are not adequately met by traditional protective devices. However, simple networks of voltage-dependent resistors, diodes, and a new device which combines two positive temperature-coefficient resistors in thermal contact with a voltage-dependent resistor, can satisfy most of the new protection requirements in exchange as well as subscriber equipment.

D.C.-controlled volume and tone control ICs

The dual tandem potentiometer IC TDA1074A is for continuous d.c. control of volume and tone in home and car radio equipment. When audio functions are d.c. controlled, expensive tandem potentiometers are eliminated from stereo equipment and performance is increased because there are no electro-mechanical components in the signal path. It also becomes a simple task to add remote control.

Local and small area networks for serial data transfer

Although microprocessors and microcomputers commonly work with parallel data, transferring data in parallel form is awkward or inconvenient in many applications. The alternative is serial transfer, for which a number of bus protocols, and the corresponding hardware and software, are now available. Among these are the Inter-IC bus (I²C) and the Digital Data Bus (D²B) which, by virtue of their simplicity and adaptability, are well suited to small industrial, business, and consumer applications.

High-speed CMOS

The PC554/74 family is a new range of high-speed CMOS digital integrated circuits which can at last match the performance of the microcomputers and high-capacity memories which they are intended to interconnect. They will doubtless replace many presently available digital ICs in a wide range of applications because they consume only 5% of the power of LSTTL and can operate at five times the speed of conventional silicon-gate CMOS.

Semiconductor laser with collimating optics

The laser read and write units in digital-optical recording systems should ideally emit collimated beams. To meet this need, the CQL10A semiconductor laser is now available together with collimating optics in a single capsule. The characteristics of the laser itself have been optimised to produce a symmetrical, divergent beam. A triplet lens system collimates this beam and a cylindrical lens corrects for astigmatism. Units incorporating the CQL10A are for read-out applications only; other units incorporating a high-power pulse laser are available for write applications.

Dual-gate MOSFETs for u.h.f. and v.h.f. applications

The BF980/BF982 dual-gate MOSFETs are two of the latest devices to take advantage of recent refinements in MOS technology. With drain source voltages typically around 7 V and pinch-off voltages of around -1 V, they are ideal for low voltage v.h.f./u.h.f. applications. And their low output capacitance, high transconductance and low noise gives these new MOSFETs a distinct advantage over former devices, especially in high-quality u.h.f./v.h.f. tuners.

One IC and a saw filter in a high-performance vision i.f. channel

The TDA3540 and TDA3541 are higher-performance, pin-compatible successors to the tv vision i.f. and demodulator integrated circuits TDA2540 and TDA2541. They are suitable for all classes of tv receiver from black-and-white to high-quality colour. The two circuits are identical except that the TDA3540 provides increasing a.g.c. for tuners with npn r.f. stages and the TDA3541 provides decreasing a.g.c. for tuners with pnp or MOSFET r.f. stages.

Nichtlineare Widerstände zum Schutz elektronischer Fernsprechanlagen

Der zunehmende Einsatz der Elektronik in Fernsprechanlagen schafft neue Schutzanforderungen, für die herkömmliche Schutzmassnahmen nicht ausreichen. Es ist jedoch möglich, mit einem einfachen Netzwerk, bestehend aus VDR-Widerständen, Dioden und einem neuen Bauelement, welches aus zwei Widerständen mit positivem TK-Wert in thermischem Kontakt mit einem VDR-Widerstand gebildet wird, die meisten der zusätzlich entstandenen Schutzanforderungen zu erfüllen. Dies gilt sowohl für Einrichtungen bei der Vermittlungsstelle als auch beim Teilnehmer selbst.

Gleichspannungsgesteuerte Lautstärke- und Klangeinsteller

Die integrierte Schaltung TDA1074A ist eine gleichspannungsgesteuerte zweifache Tandem-Potentiometerschaltung für die stufenlose Einstellung von Lautstärke und Klang in Heim- und Autoradios. Wenn Audiofunktionen mit einer Gleichspannung gesteuert werden, entfallen die teuren Tandempotentiometer in einer Stereoanlage, und die Betriebseigenschaften werden verbessert, weil der Signalweg keine elektromechanischen Komponenten mehr enthält. Auch eine Fernbedienung ist auf diese Weise leicht möglich.

Kleinflächige Verbindungsnetze für serielle Datenübertragung

Mikroprozessoren und Mikrocomputer verarbeiten die Daten normalerweise parallel; eine Übertragung der Daten in paralleler Form ist in vielen Fällen jedoch unhandlich und unvorteilhaft. Die Alternative ist eine serielle Übertragung, für die nun eine Reihe von Bus-Protokollen sowie die entsprechende Hardware und Software zur Verfügung stehen. Hierzu gehören der Inter-IC-Bus (I²C) und der Digital Data Bus (D²B), die wegen ihrer Einfachheit und Anpassungsfähigkeit für kleinere Anwendungen in Industrie, Handel und Gewerbe sowie auf dem Konsumsektor bestens geeignet sind.

Neue schnelle CMOS-Logikfamilie

Die PC554/74-Familie ist eine neue Serie von schnellen CMOS digitalen integrierten Schaltkreisen, die endlich den Anforderungen der Mikrocomputer und Grossspeicher genügen, die sie verbinden sollen. Sie werden zweifellos in den unterschiedlichsten Anwendungsbereichen viele der derzeitig verwendeten digitalen ICs ersetzen, weil sie nur 5% der Leistung von LSTTL aufnehmen und 5mal schneller als die konventionellen Silizium-Gate CMOS sind.

Halbleiter-Laser mit Kollimationsoptik

Mit Lasern bestückte Lese- und Schreibeinheiten von digitalen optischen Aufzeichnungssystemen müssen sehr gut kollimierte Lichtbündel aussenden. Hierfür ist nun der Halbleiter-Laser CQL10A zusammen mit einer Kollimationsoptik in einem Gehäuse verfügbar. Der Laser selber wurde so aufgebaut und optimiert, dass er ein symmetrisches, divergentes Bündel aussendet. Ein Drei-Linsensystem kollimiert dieses Bündel, und mit Hilfe einer zylindrischen Linse wird der Astigmatismus korrigiert. Die mit CQL10A bestückten Einheiten sind nur für Lesezwecke vorgesehen; für Schreibzwecke sind andere Einheiten mit Hochleistungs-Impuls-Lasern verfügbar.

Dual-Gate MOSFETs für UHF und VHF

Die Dual-Gate MOSFETs BF980/BF982 sind die beiden neuesten Produkte der vor kurzem verbesserten MOS-Technologie. Mit ihren Drain-Source-Spannungen von typisch etwa 7 V und ihren Pinch-off-Spannungen von etwa -1 V sind sie ideal für VHF- und UHF-Anwendungen mit niedrigeren Betriebsspannungen geeignet. Wegen ihrer kleinen Ausgangskapazität, ihrer hohen Vorwärtsteilheit und ihres geringen Rauschens sind diese neuen MOSFETs den früheren Typen deutlich überlegen, vor allem bei hochwertigen UHF/VHF-Tunern.

Bild-ZF-Kanal hoher Leistungsfähigkeit mit einer integrierten Schaltung und einem Oberflächenwellenfilter

Die integrierten Schaltungen TDA3540 und TDA3541 sind die verbesserten pinkompatiblen Nachfolgetypen der Video-ZF-Verstärkerschaltungen TDA2540 und TDA2541 für die Verstärkung und Demodulation des Bild-ZF-Signals. Sie sind für alle Fernsehempfänger geeignet, vom einfachen Schwarzweiss- bis zum hochwertigen Farbgerät. Die beiden Schaltungen unterscheiden sich nur in einem Punkt: TDA3540 ist für Tuner mit NPN-HF-Stufen mit Aufwärtsregelung und TDA3541 für Tuner mit PNP- oder MOSFET-HF-Stufen mit Abwärtsregelung bestimmt. Die neuen Schaltungen erfüllen dieselben Funktionen wie ihre Vorgänger, müssen jedoch, wenn alle Verbesserungen ausgenutzt werden sollen, extern anders beschaltet werden.

Résistances non-linéaires pour la protection des équipements téléphoniques électroniques

L'utilisation croissante de l'électronique dans les équipements téléphoniques suscite de nouvelles exigences en matière de protection, auxquelles les dispositifs classiques n'apportent pas de réponse appropriée. Cependant, de simples varistances VDR ou diodes, ainsi qu'un nouveau dispositif combinant deux thermistances à coefficient de température positif en contact thermique avec une varistance VDR, sont susceptibles de satisfaire à la plupart des exigences en matière de centraux ou de terminaux de lignes téléphoniques.

Dispositifs à courant continu pour le réglage du volume et de la tonalité

Le potentiomètre double en tandem IC TDA1074A est destiné au réglage par tension continue du volume et de la tonalité des appareils audio (HiFi ou autoradio). La commande des fonctions audio par tension continue permet d'éliminer les coûteux potentiomètres en tandem du matériel stéréo et d'améliorer les performances grâce à l'absence de composants électromécaniques sur le trajet du signal. En outre, l'addition d'une télécommande devient aisée.

Petits réseaux pour le transfert en série des données

Bien que les Microprocesseurs et Microordinateurs travaillent habituellement sur des transferts de données en parallèle, ce mode de transfert est mal adapté dans de nombreux cas d'applications. Le transfert en série est une autre solution pour laquelle on dispose maintenant de plusieurs protocoles de Bus, ainsi que du matériel et du logiciel correspondants. Citons le Bus I²C (Inter-Integrated Circuits) et le Bus D²B (Digital Data Bus), qui, en raison de leur simplicité et de leur facilité d'adaptation, conviennent bien aux petits réseaux en applications industrielles, commerciales et Grand Public.

Nouvelle famille de circuits logiques CMOS ultra rapides

La famille PCF54/74 est une nouvelle gamme de circuits intégrés numériques CMOS ultra rapides qui sont enfin aussi performants que les microordinateurs et mémoires à grande capacité qu'ils sont destinés à interconnecter. Il ne fait pas de doute qu'ils remplaceront nombre de circuits intégrés numériques actuels dans une large gamme d'applications. Leur consommation d'énergie n'est que 5% de celle des TTL/LS et ils peuvent fonctionner cinq fois plus vite que les CMOS conventionnels.

Laser à semiconducteur avec collimateur optique

Pour un fonctionnement correct, il est souhaitable que les unités de lecture et d'écriture à laser des dispositifs d'enregistrement optique digital émettent des faisceaux collimatés. Cette condition est satisfaite par le laser à semiconducteur CQL10A, équipé d'un collimateur optique contenu dans le même boîtier. Les caractéristiques du laser proprement dit conduisent à un faisceau divergent et asymétrique. Un ensemble de trois lentilles permet la collimation de ce faisceau et une lentille cylindrique corrige l'astigmatisme. Les modules équipés du CQL10A sont destinés aux seules applications de lecture; des versions pour fonctionnement en impulsion à puissance élevée sont aussi disponibles pour l'écriture.

Transistors MOSFET à double porte pour applications UHF et VHF

Les transistors MOSFET à double porte BF980 et BF982 sont deux nouveaux dispositifs exploitant les perfectionnements récents de la technologie MOS. Possédant des tensions Drain-Source typiques de l'ordre de 7 V et des tensions de pincement de l'ordre de -1 V, ils conviennent parfaitement aux applications UHF/VHF à basse tension. Par ailleurs, leur faible capacité de sortie, leur transconductance élevée et leur faible bruit donnent à ces nouveaux MOSFET un net avantage sur les dispositifs antérieurs, en particulier dans les Tuners UHF/VHF de haute qualité.

Un circuit intégré unique et un filtre à ondes de surface dans un canal de vision I.F. à hautes performances

Le TDA3540 et le TDA3541 sont des successeurs plus performants, compatibles broche à broche, des circuits F.I. Vision et démodulateurs pour téléviseurs TDA2540 et TDA2541. Ils sont utilisables sur des téléviseurs de toutes catégories, du Noir et Blanc à la Couleur de haute qualité. Les deux circuits sont identiques, sauf en ce qui concerne la C.A.G. (sélecteur NPN pour le TDA3540, PNP ou MOSFET pour le TDA3541).

Resistencias no lineales para proteger aparatos de teléfono

El empleo cada vez mayor de aparatos electrónicos de teléfono hace necesarios nuevos requisitos de protección que no reúnen los tradicionales dispositivos protectores. Sin embargo, simples circuitos de resistencias dependientes de la tensión, diodos y un nuevo dispositivo que combina dos resistencias de coeficiente de temperatura positivo en contacto térmico con una resistencia dependiente de la tensión, pueden satisfacer la mayoría de los nuevos requisitos de protección utilizados tanto en las centralitas como en los aparatos de los abonados.

Controles de tono y volumen por c.c.

El C.I. doble de potenciómetro en tandem TDA1074A está diseñado para el control continuo por c.c. del volumen y tono en equipos de audio en hogar y en el automóvil. Cuando las funciones de audio están controladas por c.c. se suprimen los costosos potenciómetros tandem de equipos estereofónicos y se mejora el rendimiento por no haber componentes electromecánicos por los que tenga que pasar la señal. También constituye una labor sencilla el dotar al aparato de mando a distancia.

Redes pequeñas para la transmisión de datos en serie

Si bien los microprocesadores y microordenadores funcionan normalmente con datos en paralelo, su transferencia en esa forma puede resultar en muchas aplicaciones engorrosa e inconveniente. En esos casos, la alternativa es la transmisión en serie, para la cual existen en la actualidad varios protocolos de barra colectora y el correspondiente "hardware" (equipo) y "software" (programas). Entre ellos podemos citar la barra colectora Inter-IC (I²C) y la Digital Data Bus (D²B), las cuales, gracias a su sencillez y adaptabilidad, son muy adecuadas para pequeñas aplicaciones industriales, comerciales y de consumo.

Circuitos CMOS de alta velocidad

La familia PC554/74 es una nueva serie de circuitos integrados numéricos CMOS de alta velocidad que puede, por fin, armonizar con las prestaciones de los microordenadores y memorias de alta capacidad que interconectan. No cabe duda de que reemplazarán a muchos de los actuales C.I. digitales existentes en una amplia gama de aplicaciones, ya que consumen sólo el 5% de la potencia LSTTL y son capaces de funcionar cinco veces más rápidos que los CMOS normales con puerta de silicio.

Laser semiconductor con lentes colimadoras

Las unidades de lectura y escritura laser en sistemas digitales de grabación óptica han de emitir, en condiciones óptimas, haces colimatados. Para cumplir este requisito existe actualmente el laser semiconductor CQL10A con las lentes colimadoras en una sola cápsula. Las características del laser propiamente dicho se han perfeccionado al máximo para obtener un haz divergente simétrico. Un sistema de tres lentes colima este haz mientras que una lente cilíndrica corrige el astigmatismo. Las unidades que incorporan el CQL10A sirven sólo para fines de lectura; existen otras unidades que incorporan un laser de impulsos de alta potencia para fines de escritura.

MOSFETs de doble puerta para uso en UHF/VHF

Los MOSFETs de doble puerta BF980/BF982 son dos de los últimos dispositivos que permiten aprovechar los perfeccionamientos más recientes en la tecnología MOS. Con tensiones fuente/drenador de unos 7 V y tensiones de codo de 1 V aproximadamente, son ideales para aplicaciones VHF y UHF de baja tensión. Y su baja capacidad de salida, elevada transconductancia y bajo ruido les dan a estos nuevos MOSFETs una ventaja distinta a la de los dispositivos anteriores, sobre todo en sintonizadores de alta calidad de UHF y VHF.

Circuito integrado y filtro de onda superficial (SAW) en un canal f.i. de video de altas prestaciones.

El TDA3540 y TDA3541 son circuitos de altas prestaciones, sucesores de los circuitos integrados de F.I. de video demoduladores TDA2540 y TDA2541, y con terminales compatibles con ellos. Son adecuados para toda clase de televisores, desde blanco y negro hasta los de excelente calidad de color. Los dos circuitos son idénticos excepto que el TDA3540 proporciona un mayor c.a.q. para sintonizadores con etapas de r.f. npn, y el TDA3541 proporciona un c.a.g. más reducido para sintonizadores con etapas de r.f. pnp y MOSFET.

Authors



J.P. Coulmance, born in Neuilly, France, in 1944, graduated in electronics and, soon after, joined Sud Aviation where he worked on telemetry for the first French satellite launching. Later, he was engaged for about seven years in medical electronics development for Massiot Philips, and since 1974 he has been with RTC - La Radiotechnique-Compélec, in Paris, where he is now a member of the telecommunication group.



Rob Croes, born in Nijmegen, graduated in electrical engineering at 's Hertogenbosch in 1963. After military service he joined the IC development group of Philips Electronic Components and Materials Division, Nijmegen, where he worked on the design of bipolar digital ICs and is now involved in development of CMOS gate arrays and the new high-speed CMOS family.



W. Eckert was born in Neusalz/Oder in 1943 and took his degree in electrical engineering in 1969. Since then he has been with Valvo, UB Bauelemente der Philips G.m.b.H., where he is now a member of the radio group of the application laboratory.



Alex Goldberger, who gained his MSEE at the Polytechnic Institute of Brooklyn, was design manager for the first large-scale integrated circuit for data communications. As applications manager for the microprocessor division of Signetics Corporation, Sunnyvale, he is responsible for application support, new product planning, and technical marketing support for microprocessor products.



J. Houthoff was born in Amsterdam, the Netherlands, in 1932 and graduated in mechanical engineering at the University of Technology, Amsterdam, in 1954. He joined Philips Electronic Components and Materials Division, Nijmegen, in 1960, initially working on diode and transistor development. Since 1965 he has been involved in the development of field-effect transistors.



Cecil Kaplinski took his M.Sc. in theoretical physics at the University of Cape Town in 1965. After ten years in various scientific posts at English universities, he joined Philips Data Systems, where he worked on operating systems. After that he worked on the application of software techniques to hardware design, initially at Philips Data Systems and Video divisions and now at Signetics.



J. C. F. van Loon was born at Tilburg, The Netherlands, in 1948. After studying electronic engineering at Philips' Technical School he joined the central application laboratory of the Philips Electronic Components and Materials Division where, as a member of the telephony group, he is engaged in design of electronic circuits for telephone apparatus.



A. P. M. Moelands was born at Breda, The Netherlands, in 1951. After graduating in electrical engineering at the University of Technology, Eindhoven, in 1976, he joined Philips Electronic Components and Materials Division where he was instrumental in the development of the 8400 serial I/O. He is now a member of the product marketing group *MOS microprocessors*.



Frans Ohlenroth graduated in electronics at Amsterdam Polytechnic and, after military service as a radar specialist, joined Philips in 1960. During his career he has been responsible for the development of transmitting transistors and for international coordination of the semiconductor development laboratories of the Philips Electronic Components and Materials Division. He is now responsible for quality and reliability assurance in the bipolar IC group.



Lodewijk J. van Ruyven received his PhD in solid-state physics from the University of Technology, Eindhoven in 1964. After a period of postdoctoral research at the University of Delaware, he spent several years working at the Research Division of American Cyanamid. He joined Philips in 1969, and is currently head of Solid-State Laser Development, Philips Research Laboratories, Eindhoven.



Peter J. M. Sijbers joined Philips Electronic Components and Materials Division after graduating in electronic engineering at the Venlo Polytechnic. As a member of the central application laboratory he has worked on television tuners and i.f. integrated circuits and is now concerned with the design and application of ICs for telephone equipment.



T. H. Uittenbogaard was born in Wageningen, the Netherlands, in 1942. He joined Philips Electronic Components and Materials Division in 1961, initially working in the quality laboratory, electron tubes, and from 1963, at the u.h.f. tubes laboratory. Since 1965 he has been a member of the tv tuner group of the application laboratory at Nijmegen.



Jos Zeelen joined Philips Medical Systems Division in 1970 and, in 1974, moved to the central application laboratory of the Electronic Components and Materials Division, where he was a member of the radio group till 1982. Since then, as a member of the television group, he has been concerned with integrated circuits for i.f.

Philips Electronic Components & Materials

Philips Electronic Components and Materials Division (Elcoma) embraces a group of companies with sales and manufacturing facilities in every major component market.

Together we offer OEMs the greatest in-depth support in component technologies, in systems application and in the widest range of components. Fundamental support in providing the latest technologies comes from Philips Research Laboratories - recognised throughout the world for their contributions to science and industry.

The components and materials we supply cover the entire range of present-day electronics.

DISPLAY SYSTEMS

B & W tv display systems
Colour tv display systems
Data graphic display systems

INTEGRATED CIRCUITS

Bipolar analogue
Consumer circuits
● video & radio/audio circuits

Industrial circuits
● opamps ● voltage regulators
● comparators ● D/A & A/D converters
● amplifiers ● interface circuits

Bipolar digital
Standard logic families
● TTL/STTL ● ECL 10K/100K

LSI circuits
● gate arrays ● interface circuits

8-bit Microprocessors

Memories
● RAMs/PROMs ● Fuse logic

NMOS
8 and 16-bit Microprocessors & peripherals

Logic systems
● video & radio/audio circuits
● text decoders

ROM memories

CMOS
Standard logic families

LSI circuits
● gate arrays ● clock circuits

8-bit Microprocessors

Hybrid integrated circuits
LF, VHF, UHF & microwave circuits
D/A converters
Proximity switches
Custom-designed circuits

ELECTRO-OPTICAL DEVICES

Image intensifier devices
Infra-red image detectors
Camera tubes
Imaging devices

SEMICONDUCTORS

Small-signal diodes
Medium and high-power diodes
Controlled rectifiers
LF & HF small-signal transistors
LF & HF power transistors
Microwave semiconductors
Opto-electronic semiconductors
Semiconductors for hybrid ICs
Semiconductor sensors

PROFESSIONAL TUBES

Industrial cathode-ray tubes
Photomultiplier tubes
Geiger Müller tubes
Transmitting tubes
Microwave devices
Reed switches

MATERIALS

Ferroxcube products
Permanent magnets
Piezoelectric products
White ceramic products

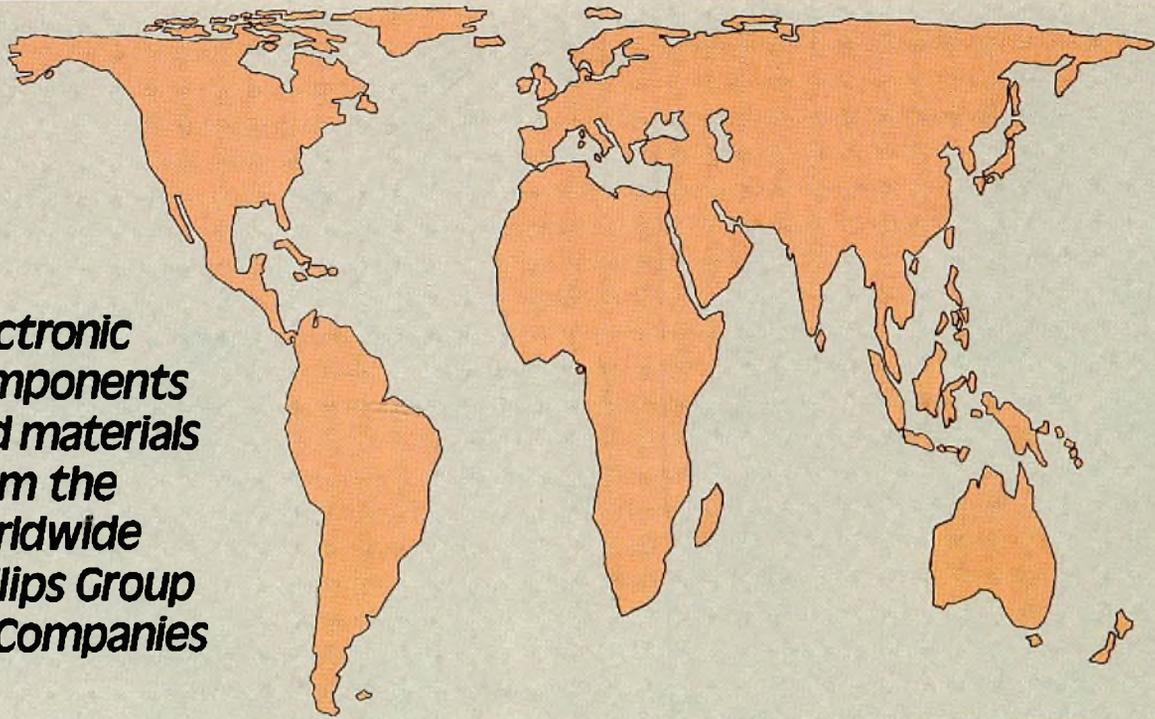
PASSIVE COMPONENTS

Ceramic, film and foil capacitors
Electrolytic capacitors
Fixed resistors
Variable capacitors
Potentiometers and resistor trimmers
Non-linear resistors
Delay lines
Piezoelectric quartz devices

ASSEMBLIES

Electric motors
Loudspeakers
Tuners
Connectors
Printed circuit boards
Variable transformers
Thumbwheel switches
Industrial microcomputer systems
Microwave sub-assemblies

**Electronic
components
and materials
from the
worldwide
Philips Group
of Companies**



- Argentina:** PHILIPS ARGENTINA S.A., Div. Elcoma, Vedia 3892, 1430 BUENOS AIRES, Tel. 541-7141/7242/7343/7444/7545.
- Australia:** PHILIPS INDUSTRIES HOLDINGS LTD., Elcoma Division, 67 Mars Road, LANE COVE, 2066, N.S.W., Tel. 427 0888.
- Austria:** ÖSTERREICHISCHE PHILIPS BAUELEMENTE Industrie G.m.b.H., Triester Str. 64, A-1101 WIEN, Tel. 62 91 11.
- Belgium:** N.V. PHILIPS & MBL ASSOCIATED, 9, rue du Pavillon, B-1030 BRUXELLES, Tel. (02) 242 74 00.
- Brazil:** IBRAPE, Caixa Postal 7383, Av. Brigadeiro Faria Lima, 1735 SAO PAULO, SP, Tel. (011) 211-2600.
- Canada:** PHILIPS ELECTRONICS LTD., Electron Devices Div., 601 Milner Ave., SCARBOROUGH, Ontario, M1B 1M8, Tel. 292-5161.
- Chile:** PHILIPS CHILENA S.A., Av. Santa Maria 0760, SANTIAGO, Tel. 39-4001.
- Colombia:** SADAPE S.A., P.O. Box 9805, Calle 13, No. 51 + 39, BOGOTA D.E. 1., Tel. 600600.
- Denmark:** MINIWATT A/S, Emdrupvej 115A, DK-2400 KØBENHAVN NV., Tel. (01) 69 16 22.
- Finland:** OY PHILIPS AB, Elcoma Division, Kaivokatu 8, SF-00100 HELSINKI 10, Tel. 1 72 71.
- France:** R.T.C. LA RADIOTECHNIQUE COMPELEC, 130 Avenue Ledru Rollin, F-75540 PARIS 11, Tel. 355-44-99.
- Germany:** VALVO, UB Bauelemente der Philips G.m.b.H., Valvo Haus, Burchardstrasse 19, D-2 HAMBURG 1, Tel. (040) 3296-0.
- Greece:** PHILIPS S.A. HELLENIQUE, Elcoma Division, 52, Av. Syngrou, ATHENS, Tel. 9215111.
- Hong Kong:** PHILIPS HONG KONG LTD., Elcoma Div., 15/F Philips Ind. Bldg., 24-28 Kung Yip St., KWAI CHUNG, Tel. (0)-24 51 21.
- India:** PEICO ELECTRONICS & ELECTRICALS LTD., Elcoma Div., Ramon House, 169 Backbay Reclamation, BOMBAY 400020, Tel. 295144.
- Indonesia:** P.T. PHILIPS-RALIN ELECTRONICS, Elcoma Div., Panim Bank Building, 2nd Fl., Jl. Jend. Sudirman, P.O. Box 223, JAKARTA, Tel. 716 131.
- Ireland:** PHILIPS ELECTRICAL (IRELAND) LTD., Newstead, Clonskeagh, DUBLIN 14, Tel. 69 33 55.
- Italy:** PHILIPS S.p.A., Sezione Elcoma, Piazza IV Novembre 3, I-20124 MILANO, Tel. 2-6752.1.
- Japan:** NIHON PHILIPS CORP., Shuwa Shinagawa Bldg., 26-33 Takanawa 3-chome, Minato-ku, TOKYO (108), Tel. 448-5611.
(IC Products) SIGNETICS JAPAN LTD., 8-7 Sanbancho Chiyoda-ku, TOKYO 102, Tel. (03)230-1521.
- Korea:** PHILIPS ELECTRONICS (KOREA) LTD., Elcoma Div., Philips House, 260-199 Itaewon-dong, Yongsan-ku, C.P.O. Box 3680, SEOUL, Tel. 794-4202.
- Malaysia:** PHILIPS MALAYSIA SDN. BERHAD, No. 4 Persiaran Barat, Petaling Jaya, P.O.B. 2163, KUALA LUMPUR, Selangor, Tel. 77 44 11.
- Mexico:** ELECTRONICA, S.A. de C.V., Carr. Mexico-Toluca km. 62.5, TOLUCA, Edo. de Mexico 50140, Tel. Toluca 91(721)613-00.
- Netherlands:** PHILIPS NEDERLAND, Marktgroep Elcon, Postbus 90050, 5600 PB EINDHOVEN, Tel. (040) 79 33 33.
- New Zealand:** PHILIPS ELECTRICAL IND. LTD., Elcoma Division, 2 Wagener Place, St. Lukes, AUCKLAND, Tel. 894-160.
- Norway:** NORSK A/S PHILIPS, Electronica Dept., Sandstuveien 70, OSLO 6, Tel. 68 02 00.
- Peru:** CADESA, Av. Alfonso Ugarte 1268 , LIMA 5, Tel. 326070.
- Philippines:** PHILIPS INDUSTRIAL DEV. INC., 2246 Pasong Tamo, P.O. Box 911, Makati Comm. Centre, MAKATI-RIZAL 3116, Tel. 86-89-51 to 59.
- Portugal:** PHILIPS PORTUEGESA S.A.R.L., Av. Eng. Duarte Pacheco 6, LISBOA 1, Tel. 68 31 21.
- Singapore:** PHILIPS PROJECT DEV. (Singapore) PTE LTD., Elcoma Div., Lorong 1, Toa Payoh, SINGAPORE 1231, Tel. 25 38 811.
- South Africa:** EDAC (Pty.) Ltd., 3rd Floor Rainer House, Upper Railway Rd. & Ove St., New Doornfontein, JOHANNESBURG 2001, Tel. 614-2362/9.
- Spain:** MINIWATT S.A., Balmes 22, BARCELONA 7, Tel. 301 63 12.
- Sweden:** PHILIPS KOMPONENTER A.B., Lidingsvägen 50, S-11584 STOCKHOLM 27, Tel. 08/67 97 80.
- Switzerland:** PHILIPS A.G., Elcoma Dept., Allmendstrasse 140-142, CH-8027 ZÜRICH, Tel. 01 488 22 11.
- Taiwan:** PHILIPS TAIWAN LTD., 3rd Fl., San Min Building, 57-1, Chung Shan N. Rd, Section 2, P.O. Box 22978, TAIPEI, Tel. (02)-5631717.
- Thailand:** PHILIPS ELECTRICAL CO. OF THAILAND LTD., 283 Silom Road, P.O. Box 961, BANGKOK, Tel. 233-6330-9.
- Turkey:** TÜRK PHILIPS TICARET A.S., EMET Department, Inonu Cad. No. 78-80. ISTANBUL, Tel. 43 59 10.
- United Kingdom:** MULLARD LTD., Mullard House, Torrington Place, LONDON WC1E 7HD, Tel. 01-580 6633.
- United States:** (Active Devices & Materials) AMPEREX SALES CORP., Providence Pike, SLATERSVILLE, R.I. 02876, Tel. (401) 762-9000.
(Passive Devices) MEPCO/ELECTRA INC., Columbia Rd., MORRISTOWN, N.J. 07960, Tel. (201)539-2000.
(Passive Devices & Electromechanical Devices) CENTRALAB INC., 5855 N. Glen Park Rd., MILWAUKEE, WI 53201, Tel. (414)228-7380.
(IC Products) SIGNETICS CORPORATION, 811 East Arques Avenue, SUNNYVALE, California 94086, Tel. (408) 739-7700.
- Uruguay:** LUZILECTRON S.A., Avda Uruguay 1287, P.O. Box 907, MONTEVIDEO, Tel. 91 43 21.
- Venezuela:** IND. VENEZOLANAS PHILIPS S.A., Elcoma Dept., A. Ppal de los Ruices, Edif. Centro Colgate, CARACAS, Tel. 36 05 11.

For all other countries apply to: Philips Electronic Components and Materials Division, Corporate Relations & Projects, Building BAE3, 5600 MD EINDHOVEN, The Netherlands, Tel. +31 40 72 33 04, Telex 35000 phic nl.

A31