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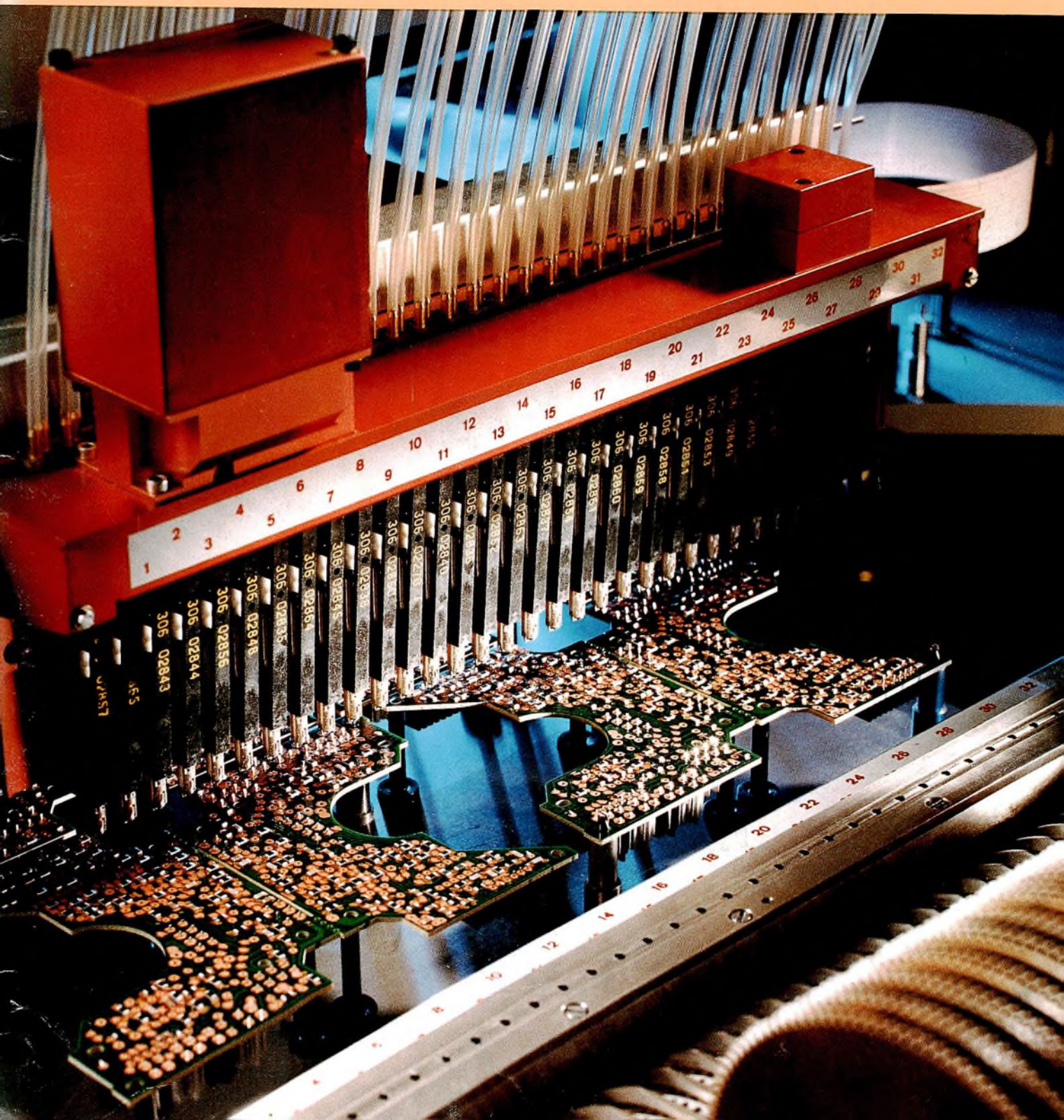

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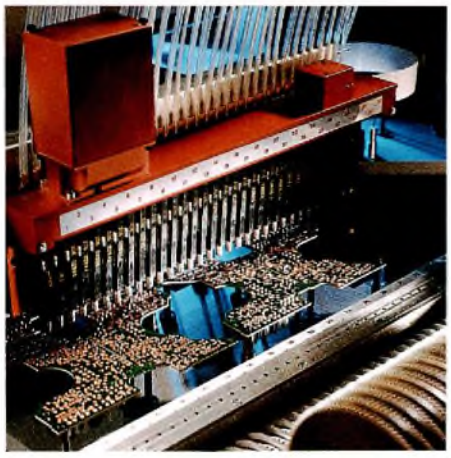


Surface-mounted devices are changing the shape, the production technology, and the economics of printed circuitry. Tomorrow's boards, assembled automatically by machines capable of placing upwards of a quarter million components an hour, will be smaller, more densely packed, and more reliable. For an overview of the present state and future prospects of surface-mounted assembly, see the article beginning on page 66.

Surface-mounted devices in printed circuit board assembly

Spurred by considerations of economy, quality, and miniaturization, the technology of printed circuit board assembly – and indeed the printed circuit board itself – is undergoing radical change. Although leaded components still predominate in most of today's boards, the future clearly belongs to surface-mounted devices (SMDs): miniature, mostly leadless, components that can be soldered direct to the surface of a board.

Since its introduction in the labour-intensive assembly of hybrid circuits in the '60s, surface mounting has evolved into a mature production technology. By the end of the '80s at least half the boards in production are expected to use it predominantly. Among the reasons for that expectation are that surface mounting can be extensively automated, from component stock-keeping to the soldering of finished boards; that it allows denser component packing; and that it gives a higher-quality product. Incidental but no less important is a considerable gain in high-frequency performance due to the absence or extreme shortness of leads.

With surface mounting, assembly costs can in many instances be halved. Moreover, because of the denser packing, boards can often be shrunk to as little as a third their normal size, economizing on material and enabling the size and weight of equipment in which they are fitted to be reduced too. In respect of quality, line rejects as low as 50 ppm for finished boards can be regarded as a realistic target.

Our range of components for surface mounting is sufficient to cover 80% of today's circuit requirements. Even if the range were not enlarged, the percentage for tomorrow's circuits will be still higher, for the accelerating trend to replace analogue functions by digital will substantially lessen the requirement for components such as potentiometers and inductors. Eventually, leaded components will survive only in power and small-production custom circuits.

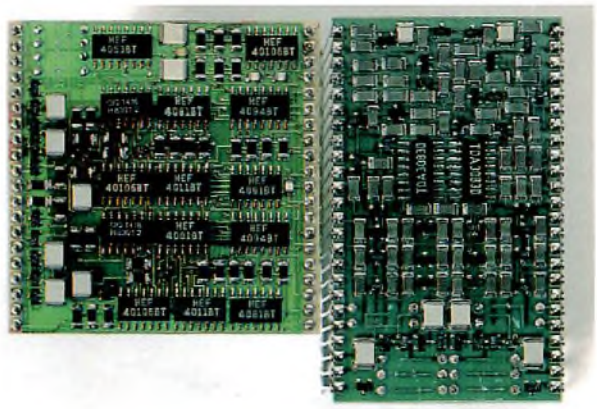


Fig.1 Examples of the component density that can be obtained with surface-mounted assembly

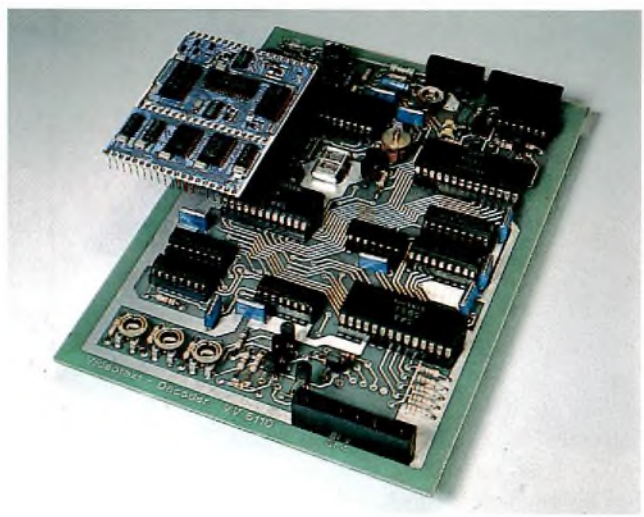


Fig.2 Two versions of a videotext decoder; the one using SMDs occupies less than a quarter the space of its counterpart with leaded components

SURFACE-MOUNTED ASSEMBLY

In conventional circuit board assembly, components are mounted by inserting their leads into holes in the board and soldering them to printed conductors; the components are usually on one side of the board and the conductors on the other. In surface-mounted assembly, the components are first positioned on the conductor patterns and held in place by solder paste or glue. Then they are soldered: by reflow soldering if they are attached by solder paste; by some form of immersion soldering if they are glued – SMDs are designed to withstand the immersion.

Holes

Unlike those with leaded components, boards using solely SMDs do not require drilled or plated holes to locate, hold or connect the components. It is feasible, however, to put SMDs on both sides of a board, and in that case plated-through holes can be used to make connections between conductors on opposite sides.

Depending on the design of the board, small vent holes may sometimes be required in critical areas to relieve the pressure of flux gases liberated by the heat of soldering.

Mixed prints

If necessary, leaded components and SMDs can be combined on a single board. Though this sacrifices some of the advantages of surface mounting, it is sometimes unavoidable, as when certain essential components, such as crystals, inductors or potentiometers, are not available as SMDs. The usual, and generally the most advantageous, way is to put the leaded components on one side of the board and the SMDs on the other; often, both can then be wave soldered in one operation.

It is also possible to mix leaded and surface-mounted components on one side of a board; then, it is usually most convenient to place whichever type is the more numerous first.

PLACEMENT SYSTEMS

Currently available automatic placement systems for SMDs fall into four classes.

In-line systems have a number of dedicated heads, each of which places an SMD in a set position on each board as it passes underneath; by the time the board reaches the end of the line of heads, all the required SMDs have been placed. Though simple, such systems have two drawbacks: resetting them for different boards is time consuming; and, if the number of SMDs per board is large, the line becomes impractically long.

Sequential systems place SMDs one after another in positions determined by software control of the movement of either the placement head or the circuit board. Reprogramming can be done quickly, but, since the system places only one component at a time, the time per board is long.

Simultaneous systems place a number of SMDs at a time and can often fill a board, or a large part of one, in a single step. Such systems have high output but long resetting time.

Simultaneous/sequential systems combine the high output of simultaneous systems with the quick reprogrammability of sequential ones. Some of today's simultaneous/sequential systems can handle more than a thousand circuit boards and 200 000 SMDs an hour.

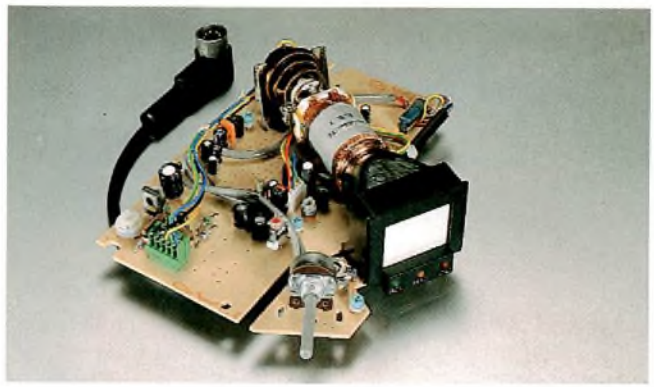
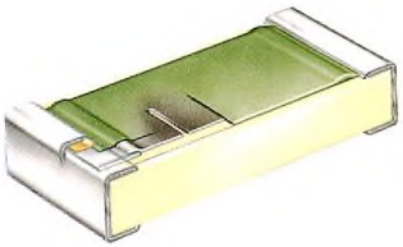


Fig.3 Typical example of a mixed print: in this video camera viewfinder, leaded components are on one side of the board and SMDs on the other

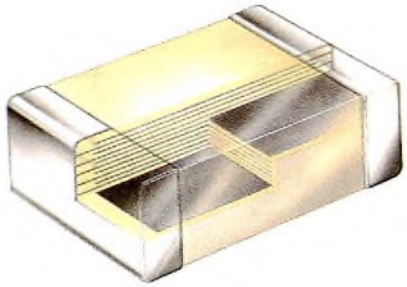
Fig.4 Simultaneous/sequential placement machine with a capacity of more than 200 000 SMDs an hour. Each of the quick-change tape magazines has a capacity of 32 reels with up to 10 000 SMDs per reel

THE NEW LOOK IN ELECTRONIC COMPONENTS

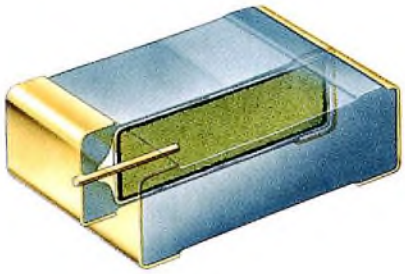
The essential difference between surface-mounted devices and their leaded counterparts is in package configuration and size. The technology is based on proven principles that have been developed, refined, and proved over the history of electronic component manufacture.



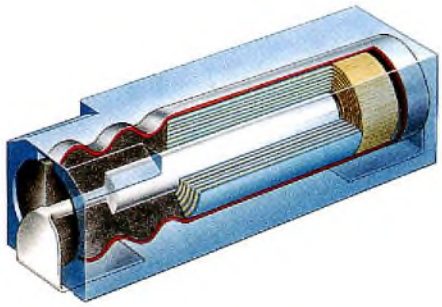
Resistor. The resistive layer is applied as a paste formulated to cover a range of resistances; after firing, the layer is laser trimmed to the required value. 1 Ω to 10 MΩ; ±5%, ±10%, ±20%; 0,125 W.



Ceramic-chip capacitor. Electrodes are screened onto ceramic plates which are then stacked and laminated under pressure and cut into blocks, after which the binder is burnt off and the blocks are fired. 0,47 pF to 0,47 μF; ±5%, ±10%; 50 V (EIA), 63 V (IEC).

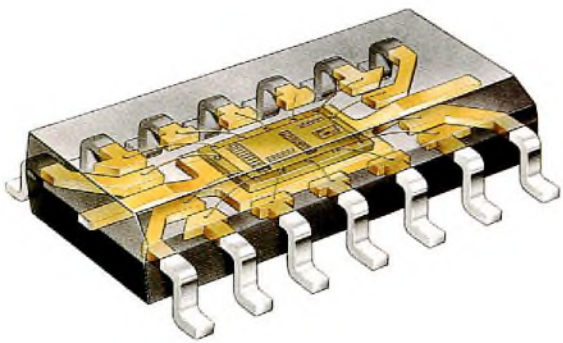


Solid tantalum capacitor. High-purity sintered tantalum anode with electrolytically formed oxide dielectric. 0,1 μF to 100 μF; ±5%, ±10%, ±20%; 4 V to 50 V.



Aluminium electrolytic capacitor. Etched aluminium foil electrodes rolled with paper separators, impregnated with electrolyte, enclosed in an aluminium can and cased in moulded plastic; terminals turned under for soldering. 0,1 μF to 22 μF; −10% to +50%; 6,3 V to 63 V.

Diodes and transistors. Virtually any of the standard leaded types can be made available in SOT-23, SOT-89, SOT-143 or SOD-80. Crystals identical to standard types; smaller header and package reduce allowable dissipation.

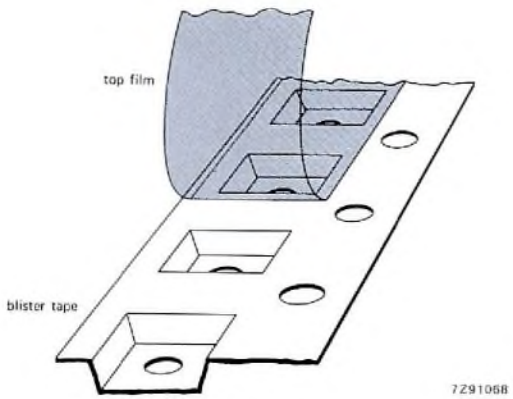


Integrated circuits. A wide range of bipolar and CMOS types, including microcomputers, in SO-8, -14, -16, -16L, -20, -24, -28 and VSO-40. Crystals identical to their larger counterparts.

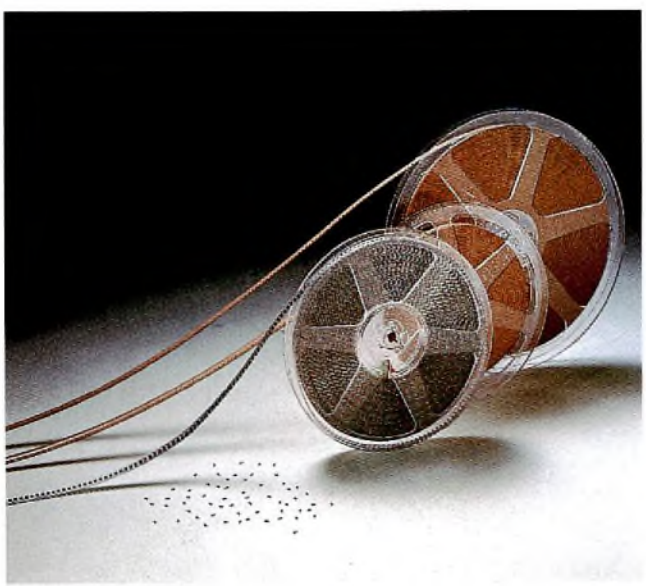
SMD packaging

Packaging is an integral part of surface-mounted assembly; one of its important functions is to ensure that SMDs are presented to the placement machines at a controllable rate and in known orientation. The preferred packaging is blister tape (Fig.5) with a 4 mm sprocket-hole pitch; the tapes are normally supplied on 180 mm or 250 mm reels holding, respectively, 4000 or 10 000 SMDs.

An IEC standard for 8 mm wide tape is already generally accepted; standards for 12 mm, 16 mm and 24 mm tapes are under consideration.



(a)



(b)

Fig.5 (a) Blister tape; (b) standard 180 mm and 250 mm tape reels (respectively, 4000 and 10 000 SMDs per reel)

Sticking

SMDs can be stuck to a board either by glue or solder paste. For large scale production on plastic boards, thermosetting epoxy glue is preferred; it can be applied by screening, by automated syringes, or by pin-transfer. Screening can only be done on an absolutely flat surface and so is not practical for boards to which leaded components are already attached. Automated syringes are expensive and complicated if glue is to be deposited at many placement sites simultenously. In nearly all cases, pin-transfer (Fig.6) is the most efficient and economical method; a jig with glue-transfer pins corresponding to all the placement sites on a board can deposit accurately controlled dots of glue for all the SMDs at once.

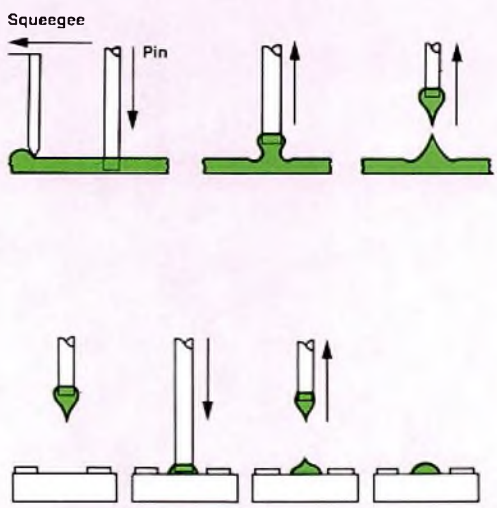


Fig.6 Pin-transfer glue applications: a squeegee levels the surface of the glue; each pin dips into the glue, withdraws with a droplet attached, transports the droplet to the circuit board, and deposits a glue dot between SMD contact pads. Control of glue consistency and dipping depth ensures uniformity of the deposited dots. An array of pins matching the SMD placement positions can deposit glue for many SMDs at once

SMDs that are to be attached to ceramic substrates can also be glued, either with ordinary epoxy glue in the space between the contact pads or with conductive glue on the contact pads. If the SMDs are to be reflow soldered, they are usually stuck with solder paste screened onto the contact pads.

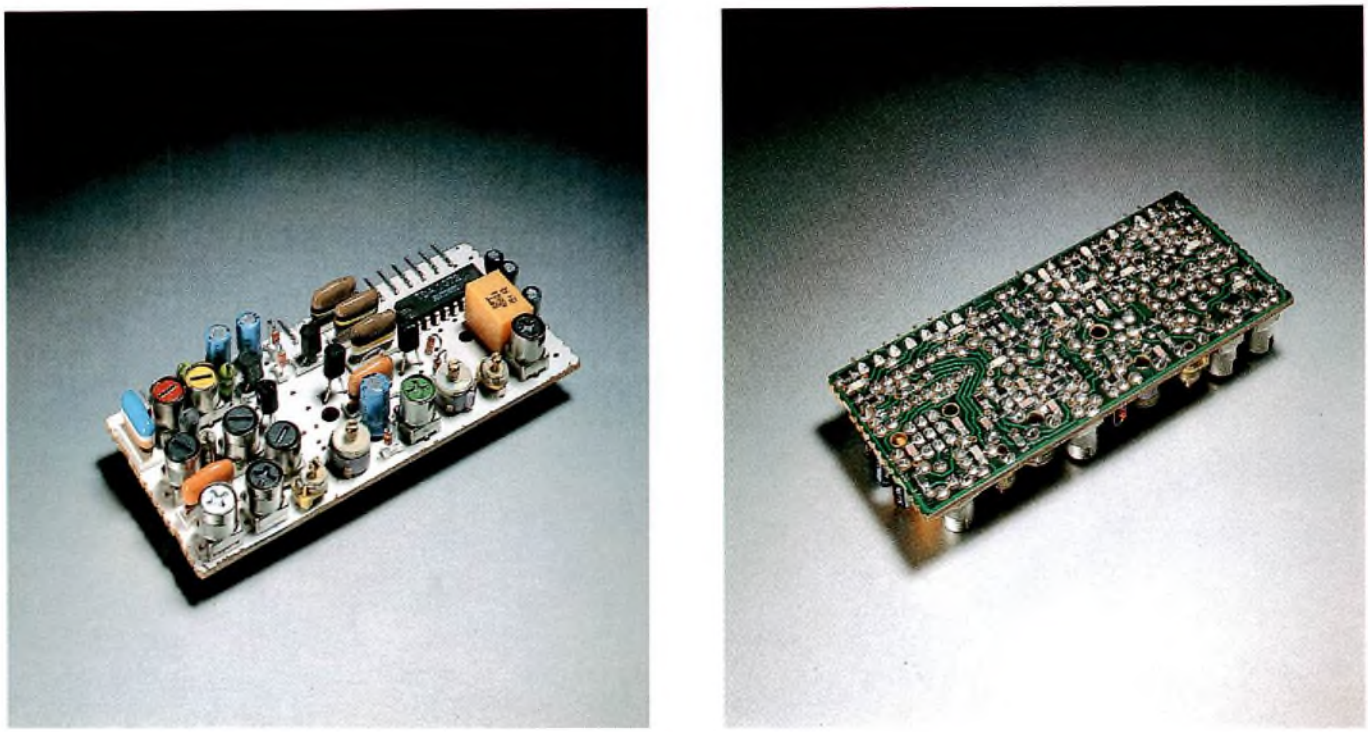


Fig.7 Complete a.m. radio with all leaded and adjustable components on one side of the board, all SMDs on the other

DESIGNING WITH SMDs

Adapting a circuit for surface-mounted assembly is not a matter of merely substituting SMDs for leaded components. Electronic, mechanical, and production engineering aspects must all be taken equally into account. The layout of the board, for instance, depends on the dimensional tolerances of the SMDs and the accuracy of the placement machinery, and even on the type of glue and method of soldering. It also depends on whether all the components required are available as SMDs. If they are not, it may still be practical to use one board with SMDs on one side and leaded components on the other. In other cases it may be more advantageous to partition the functions anew, putting those that require leaded components on a separate board.

As with the changes already brought about by integrated circuits, surface-mounted assembly will also have far-reaching effects on product design. The savings in size, weight and cost, together with the gain in reliability and high-frequency performance that it puts at the designer's disposal will in most cases justify a fundamental rethink of product philosophy.

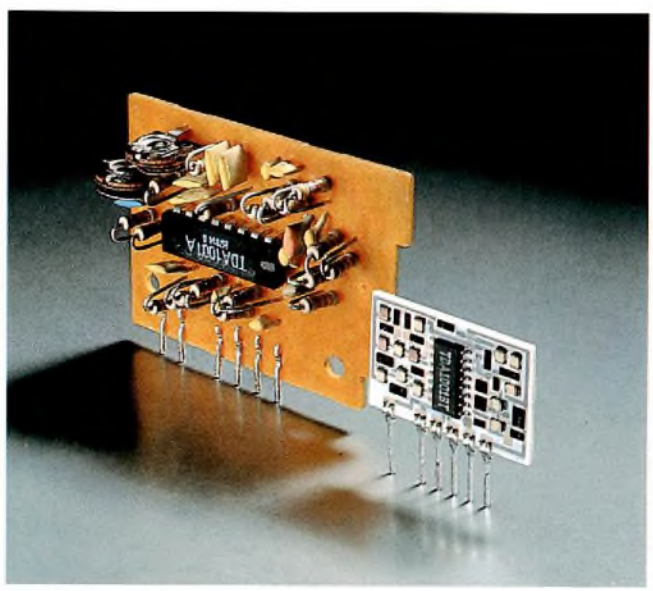


Fig.8 Interference suppression circuit for an f.m. receiver. Left, with leaded components. Right, the same circuit with SMDs; only the two potentiometers have been moved to a separate board

Video display and attributes controller ICs

H. ENG, A. GOLDBERGER and J. GOODHART

Over the past few years, LSI has dramatically expanded the capabilities of CRT terminals, transforming them from simple 'glass' typewriters into computer subsystems in their own right. At the same time, it has lowered their power consumption and cost and upped their reliability. Now, two new ICs, the SCN2674 video display controller and SCB2675 video attributes controller, extend even further the capabilities that can be economically designed into a CRT terminal.

Among the advanced features offered by the SCN2674 are row-table addressing, automatic soft scrolling, double-height and double-width rows, bit-mapped graphics accessing, and display-memory addressing (64 Kwords). To these, the SCB2675 adds colour and multilevel monochrome modes, double-width characters, and dot-stretching and dot-width control. A typical CRT terminal system architecture designed around the chip set comprises four main sections, with each section embodied in a single chip (Fig.1).

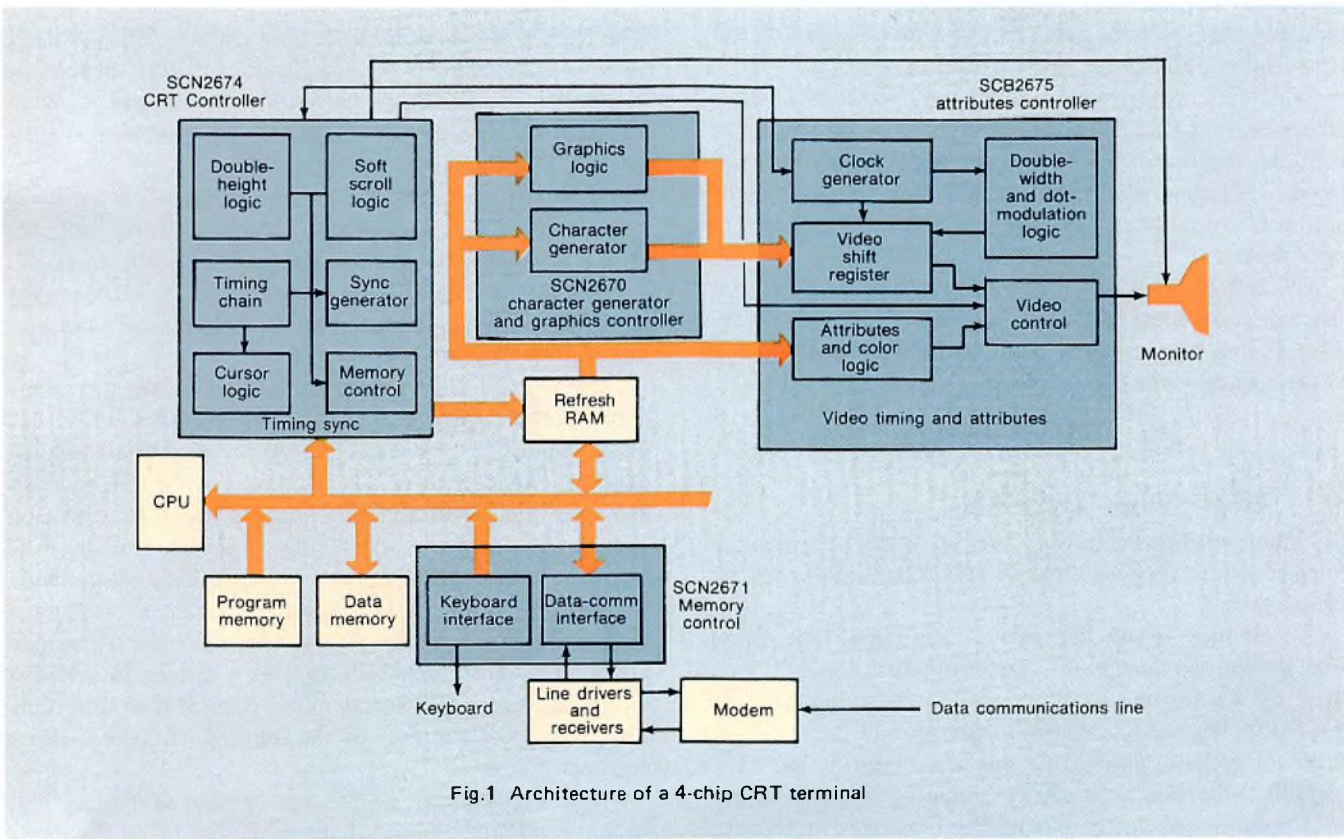


Fig.1 Architecture of a 4-chip CRT terminal

The SCN2674 incorporates the major CRT controller functions – timing chain, sync generator, cursor logic, and memory-addressing control – plus two sections to provide soft scrolling and double-height top and bottom rows. The SCB2675 attributes controller encompasses the high-speed video logic section for the CRT terminal. It contains the dot-clock divider, which divides the externally generated dot clock into the character clock required by other portions of the terminal; the parallel-to-serial shift register; attribute logic, including colour control in the colour mode; and double-width and dot-modulation logic. Two additional ICs, the SCN2670 and SCN2671 described in EC&A Vol.4 No. 1, provide the character generator, UART, and keyboard encoder portions of the terminal.

Programmable features

The CRT controller's basic functions include generation of timing pulses for the CRT (horizontal and vertical sync) and the addressing of the video memory. Addressing must be synchronized with the scanning action of the display. The terminal must also display a cursor and arbitrate between itself and the CPU for access to the video memory.

The SCN2674 not only performs these basic functions, it provides a host of programmable features that allow a user to configure a wide variety of display systems. Programmable parameters include screen format (characters per row, rows per screen, and scan lines per row), horizontal and vertical timing (front porch, sync width and back porch), cursor characteristics (size and blink rate), and interlaced or non-interlaced operation.

Since the entire system is under the control of a microprocessor, many features can be provided in software. For example, the user can program the region, direction, and speed of scrolling. Additional peripheral chips, like disk or protocol controllers, can further enhance the system capabilities.

The SCN2674 also produces interrupts based on several internal conditions. Although interrupts are not always needed, they allow real-time intervention with the display so that special features can be implemented.

CPU/video-memory interfacing

Depending on the application, interfacing the CPU with the video memory can be critical. The SCN2674 allows several schemes.

The simplest – and least expensive in terms of hardware – is the independent buffer mode, in which the CPU uses the CRT controller for all accesses to the video memory (Fig.2(a)). Because there is no contention in this mode, it does not require address multiplexers. Instead, the CRT controller directs the transfers required by the CPU during blanking intervals so that there are no visual disturbances on the display. Data for each transfer is written into or read from a bidirectional latch that serves as the interface between the CPU bus and the video memory.

Transparent and shared modes allow the CPU to access the video memory directly, either during blanking intervals or immediately, but require additional circuitry (Fig.2(b)). A fourth mode, the row-buffer mode, fetches the video data during DMA cycles from a designated area in the CPU memory and stores it in row-buffer RAM during a scan of the first line of each row (Fig.2(c)). During this scan, data is sent both to the row buffer and to the display's character generator. During subsequent scans of the other lines of the character row, the row buffer provides the character generator with the data, thus giving the CPU full access to the video memory during the scan of all but one line of each character row, or typically 90% or more of the time.

Interleaved access (Fig.2(d)) is the most flexible method of all. Here, both the display controller and the CPU can access the video memory during any clock cycle. One half of each cycle is reserved for controller accesses, the other half for CPU accesses.

Although this method provides transparent CPU access, it requires multiplexing circuits, and the controller and the CPU must operate from the same clock. The required RAM access time is half of what is needed by the other methods.

Getting RAM data

The SCN2674 can address the data contained in the RAM in several ways. For simple applications, addressing can be sequential. Here, the user places the data to be displayed in consecutive locations in the RAM, corresponding to the character positions on the screen (Fig.3).

The starting address in the video memory is loaded into one of the CRT controller's internal registers, and the device addresses the RAM sequentially starting from this location in each field. Data can be scrolled by changing the specified starting address by an amount corresponding to the number of characters per row.

Although sequential addressing is adequate for simple displays, other applications demand more flexibility. For those, the SCN2674 offers two other addressing methods: sequential-split and row-table. In the first, the user specifies the row where the sequential address jumps to a location programmed into one of the chip's registers. This splits the screen into two parts, each of which can be manipulated independently, say, in a status-line display in which the display part of the screen can scroll while the status line stays fixed. One such split can be programmed into the chip's hardware; for several splits, the real-time interrupts can change the contents of the split-row and split-address registers.

Some applications require yet another technique. For example, on-screen editing in the sequential-addressing mode

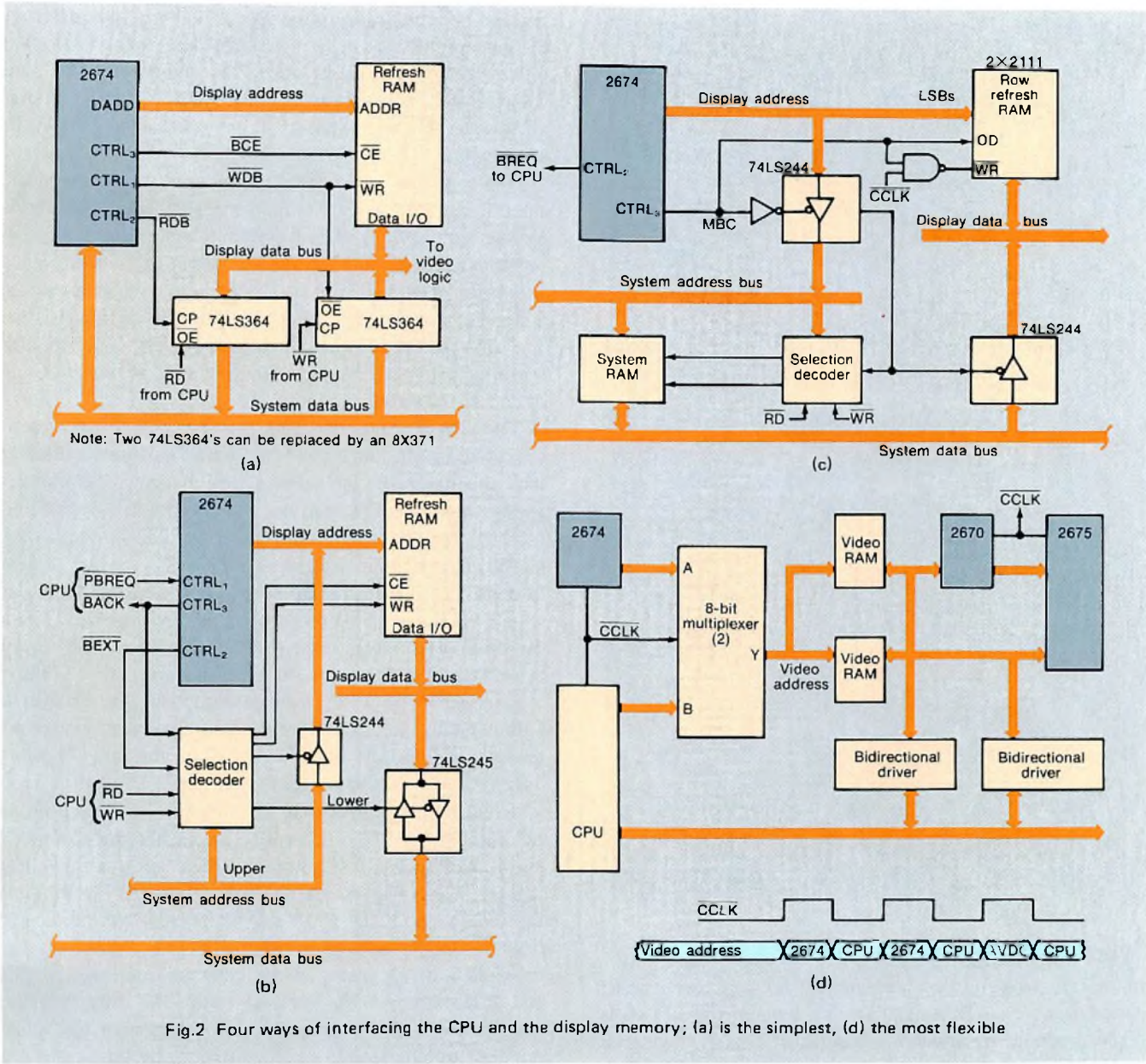


Fig.2 Four ways of interfacing the CPU and the display memory; (a) is the simplest, (d) the most flexible

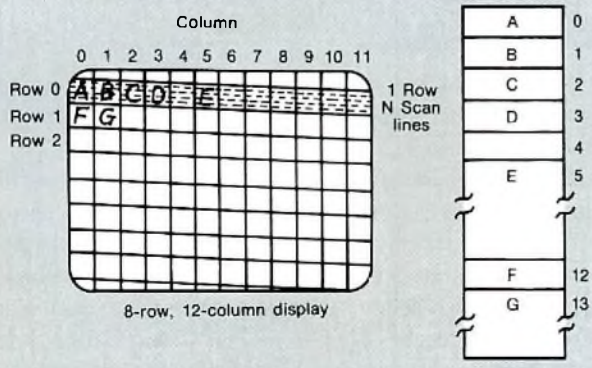


Fig.3 Sequential addressing; consecutive RAM locations correspond to consecutive character positions on the screen

requires that the CPU move the data within the video memory when a row is to be added or deleted. To eliminate this time-consuming task, the controller offers row-table addressing.

Here, each character row's starting address is defined in a table of row-start pointers (Fig.4). The table resides anywhere in memory and is pointed to by the controller's screen-start register 2, which in this mode serves as a table-start register. At the beginning of each new row, the controller automatically fetches the pointer from the table and addresses the video RAM starting at that location. Now it is a simple matter to add, delete, or move a row – the CPU need only change the organization of the row table, not move the display data. For other applications, several row tables could be set up so that a simple change of the table pointer changes the display completely.

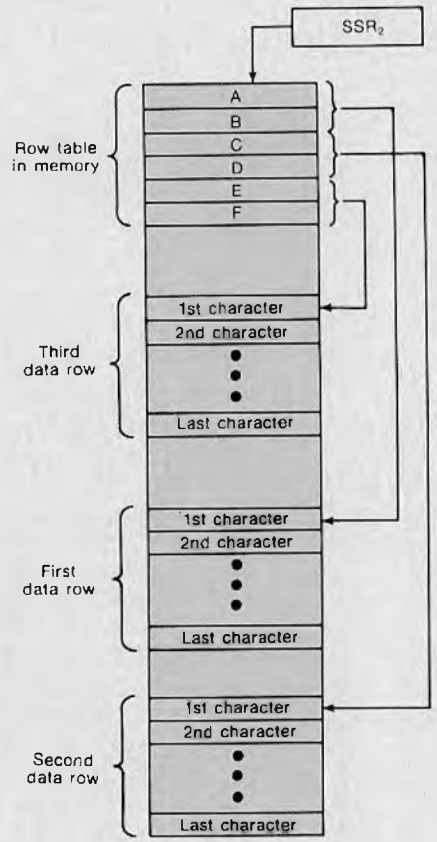


Fig.4 Row-table addressing

Smooth scrolling

In effect, scrolling provides an endless page for writing data. Once a page fills up, space for the next row of data is made available by removing the top row and moving all remaining rows up by one. New data can go into the blank row left at the bottom of the screen. (The process can be reversed if new data is to be written at the top of the screen).

Although this procedure is perfectly satisfactory for data input, readability breaks down when the data comes in quickly from an external source, causing the rows to jump up or down. Smooth (soft) scrolling remedies that by moving the data in scan-line increments instead of in whole-row jumps, thus creating the effect of a sheet of paper slowly moving through the viewing area.

One system restriction in providing smooth scrolling is that the data input rate cannot exceed the rate of display motion. Thus successive line feeds must be separated by a number of real or 'fill' characters to allow the display to keep up with received data. The number of fill characters is a function of the scan lines in each row, the scroll rate, and the communications-line speed. It also may be affected by system software or hardware features, such as the data buffer found in some terminals that stores received data while scrolling takes place, or the XON/XOFF protocol that advises the sender to start or stop sending as the buffer fills and empties.

The controller's dedicated registers not only off-load the smooth-scrolling task from the CPU, they allow the user to choose from among several scrolling region variables: size, position, and the number of scan lines at any instant. Since the region is normally fixed, its specifying registers usually are programmed only during the chip initialization routine. The split-screen facilities, in conjunction with the smooth-scroll logic, provide a split to a new address at the beginning or end of the scrolling region.

To achieve a smooth scroll, the CPU merely sets a bit in one of the controller's control registers and puts a number into the lines-to-scroll register. By changing the number periodically, the CPU can control the speed and direction of the scroll. For example, setting the lines-to-scroll to 1 initially, then incrementing during every vertical retrace interval, will result in scrolling up at 50 scan lines per second (assuming the controller is programmed for a 50 Hz vertical rate); incrementing the value only every other retrace will reduce the scrolling speed to 25 lines a second. Since the CPU controls the speed, it can adjust it automatically as a function of the number of characters received in the last row, thus speeding the rate for short lines and slowing it for long ones.

Even more sophisticated scrolling schemes are possible by combining interrupts with the capabilities described above. Consider, for example, a system with two scrolling regions. The CPU sets up the parameters for the topmost scrolling region (start-scroll row, end-scroll row, number of lines to scroll) during the vertical retrace interrupt. The controller is programmed to issue an interrupt at the end-of-scroll row. The service routine for this interrupt then reprograms the appropriate registers with the values required for the second scrolling region. By this means it is possible even to scroll the two regions simultaneously at different rates or in different directions.

Additional features

The SCN2674 offers still more: double-height and double-width character displays, and alphanumerics, or bit-mapped graphics addressing.

Stretching characters is most effective with the row-table addressing mode because the pointer for each character row contains two extra bits that can be called on to specify that row as normal, double-height, double-width, double-height tops or double-height bottoms. Row-table addressing yields double-height characters (the combination of a double-height-tops row and a double-height-bottoms row, in consecutive order) that can be displayed without repeating the data in the video RAM. That is, only the table

entry must be duplicated, with appropriated modification of the control bits.

When double height is specified, the scan-line count outputs delivered by the controller to the character generator are incremented only every other scan line. If the double width is to apply to every character in the row, the double-width command should be routed to an output pin for use by the attributes controller. Alternatively, an extra bit in the video attributes RAM can tell the attributes controller to specify double width on a character-by-character basis, thus allowing normal and double-width characters to be mixed on the same row. If row-table addressing is not used, a register in the controller can program the beginning and end rows for characters with double height or width. However, this will not be as convenient as the row-table method because data will have to be repeated twice in the video RAM, and the control registers reprogrammed each time the display is scrolled.

A terminal can be given both alphanumeric and advanced graphic capability – like graphs and pie charts – by programming the SCN2674 to operate in its bit-mapped addressing mode. In that mode, the address outputs sequentially change with each scan line instead of only at character-row boundaries. It is possible to combine both modes, so that a portion of the screen is scanned for normal alphanumeric mode and the rest operates in the bit-mapped graphics mode. A control output signals external circuitry to address appropriate memory (Fig.5).

While the SCN2674 controls the monitor timing and addressing of the video RAM, the SCB2675 pursues equally important tasks – it generates the basic clock for the SCN2674 from the dot clock, takes the parallel data from the character generator or bit-mapped memory, applies specified attributes, and generates the video signals for the monitor. Since the attributes controller operates at the faster dot rate instead of the slower character rate, it is a bipolar part.

Colour and monochrome

The SCB2675 operates in two modes: colour or monochrome. Each mode supports an array of visual attributes. In the colour mode, apart from the underline, double-width and blink attributes, the foreground and background of each character can be specified independently as one of eight colours. Colour outputs include red, blue, and green video, plus a luminance output asserted for every character dot on display. The luminance output can be used to select a set of foreground colours different from the background, or to drive a monochrome display simultaneously with the colour display.

In the monochrome mode, the attribute characteristics of the SCB2675 – which emulate DEC's popular VT-100 and VT-200-series terminal – include reverse video, blank and highlight, in addition to underlining, character width stretching, and blinking. Each of these can be applied to each character independently. The SCB2675's two video outputs control screen intensity while two general-purpose attribute outputs tell the state of two corresponding input pins at the moment the character dot data is loaded into the SCB2675. Those video outputs can implement attributes that the chip does not support.

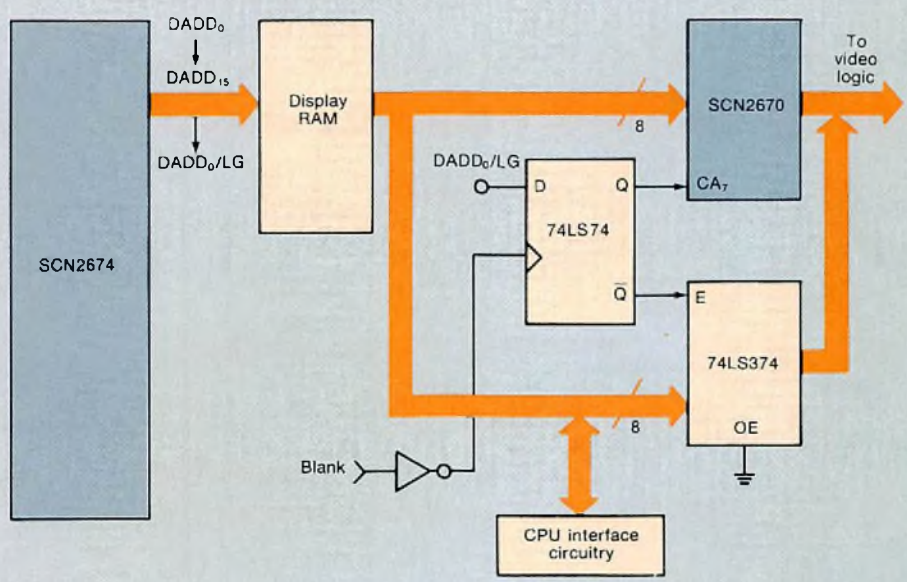


Fig.5 Arrangement in which one part of the screen is used for alphanumeric display and the other for bit-mapped graphics

A special retrace blanking input on the SCB2675, when held high, automatically forces the video outputs to low during the blanking interval, creating a black border around the display. Pulsing the input brings the light background closer to the CRT's edges, eventually eliminating the black border. In the colour mode, an external multiplexer can be added to create borders of any colour.

Dot stretching

A feature of the SCB2675 is that it overcomes some of the limitations and problems that occur when terminals are asked to 'extend' themselves.

For instance, as dot speeds increase to stretch display resolution, more bandwidth is required than most low-cost monitors have. For a single dot input, the beam current then does not reach full intensity, as it does for a group of consecutive dots. The result – especially with characters in which vertical members are only one dot wide – is that the horizontal lines are brightest.

The SCB2675 alleviates this problem by automatically appending an extra dot to each single dot or contiguous group of dots fed into the video shift register. The resulting video output is always at least two dots wide, considerably reducing the needed bandwidth and the corresponding cost of the monitor.

Independent buffer mode

To minimize chip count, a typical colour display can take advantage of the SCN2674's independent buffer mode (Fig.6). The SCN8051 microcomputer contains the operating program in its internal 4-Kbyte ROM, and its 256-byte RAM provides the temporary storage required by the program. The interface to the unit's keyboard is handled by the 8051's internal UART. Auxiliary communications take place over one channel of the SCN2681 dual UART; the second channel communicates with the host computer through RS232 interfaces.

The CRT controller, responding to commands from the microcomputer, completely controls the data transfers

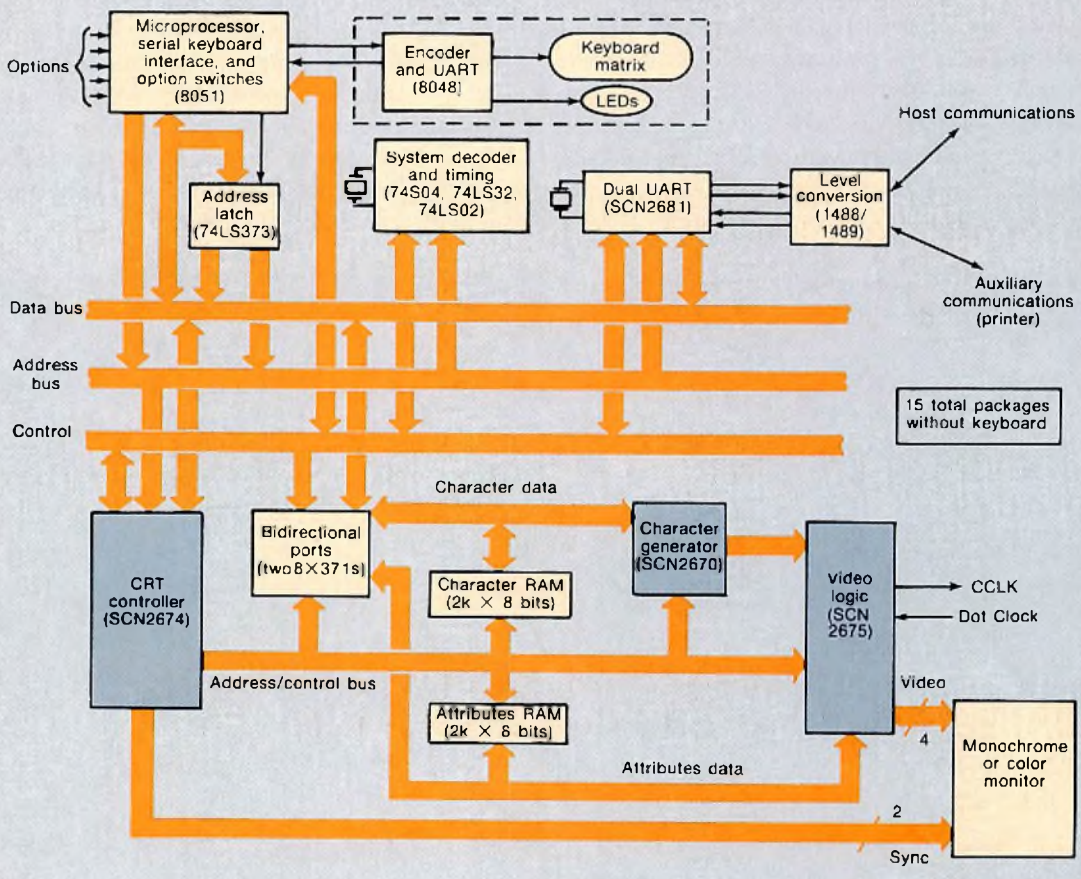


Fig.6 Practical CRT terminal system in which an 8051 microcomputer contains both the display firmware and the keyboard interface circuitry

between the CPU and the video RAM: to avoid display interference, these transfers occur only during display blanking intervals. For full screen updates, say, to clear the screen, the CRT controller can be commanded to write a designated character and attribute from a starting address (cursor) to an ending address (pointer). In this operation, the chip will execute as many writes as possible during successive blanking intervals, thereby maintaining a normal display of screen data until the command is completed.

The video RAM consists of two 2K8 static RAMs arranged in a 2K16 format, adequate for a display of 24 lines of 80 characters, with sufficient RAM available for the extra character row required during smooth scrolling. The 16 bits of RAM provide a seven-bit character code, one bit to select dot-matrix characters or block-graphics from the SCN2670 character generator, and eight attribute bits: character colour (3), background colour (3), blink, and underline. A pair of bidirectional latches forms the interface between the CPU data bus and the video data and attribute buses.

The CPU writes the data and corresponding attributes into the latches, writes the video RAM address into the CRT controller's cursor register, and then instructs the controller to execute the transfer. An interrupt informs the CPU when the operation is completed so that it can process the next character. The chip can automatically increment the cursor address, so that the cursor load need not be performed each time when characters are written into successive screen locations. Likewise, the attribute latch needs updating only when the attributes change from the previously written character.

The 17,5-MHz dot rate clock (generated by a crystal oscillator) is divided by nine internally and supplied as the character rate clock to the CRT controller and the character generator. The CRT controller receives the dot data from the character generator, the character attributes from the attribute-RAM, and a latched double-width row attribute from the SCN2674. It pipelines the attributes for one character period to compensate for the one character time delay through the character generator, then combines the serialized dot data with the attributes to deliver the red, green, and blue video streams, and the luminance control that gives the foreground characters a different intensity from the background.

Software considerations

With the majority of the terminal's functions contained within the VLSI chips, the hardware implementation is greatly simplified and the largest task becomes the design of the system's software and firmware.

Software for a microcomputer-based CRT terminal obviously is closely tied to the system hardware configuration and its characteristics (Fig.7). If multiple interrupt driven sources are required, the system hardware and software designs must be able to prioritize the interrupts to ensure proper servicing of the different sources. A typical system will include three interrupting sources: the keyboard, the communications interfaces, and the CRT controller. (The last may require the highest priority, with real time interrupts for special scrolling and display formats.). The keyboard and communications interrupts can, in most cases, tolerate some delay before servicing since they include one or more data buffering levels.

Upon power-on, the microcomputer initializes the scratchpad RAM; the SCN2674, for the desired screen format, monitor timing, and so on; and the communications interfaces and keyboard. The microcomputer then reads any mode switches (full or half duplex, baud rate, cursor type, etc.) and sets the appropriate system parameters. The processor can now enable its interrupts and wait

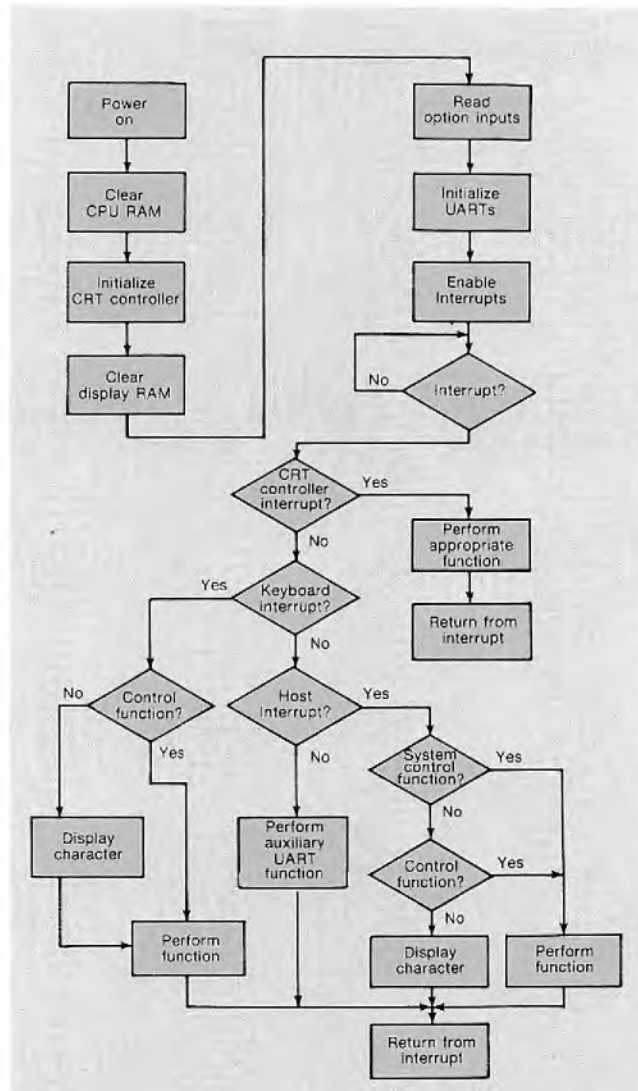


Fig.7 The terminal arrangement and desired functions determine the system software; the program is largely shaped by the nature and number of interrupts

in a loop for an interrupt to occur. When it does, the processor first determines the source, then performs the required service operation.

An interrupt from the keyboard may be a displayable character or a control function. Displayable characters are usually transmitted to the host computer and placed in the display memory for presentation on the screen. Certain control characters such as cursor movement or keyboard errors cause only local actions, while others require transmission to the host.

An interrupt from the CRT controller is usually a request for scrolling or split-screen presentation. For scrolling, the processor programs the SCN2674 to generate an interrupt at the beginning of the vertical retrace interval. When the VBLANK interrupt occurs, the processor increments the screen start address value by the number of characters per row (cutting off the top row), and the new bottom row is cleared to nulls. When soft scrolling is selected, the additional functions described earlier are performed.

When the SCN2674 operates in the row-table addressing mode, each character row on the screen will have its starting address in a table of addresses residing in either the processor's memory or in the display memory. Smooth scrolling is available in this mode, but some of the chip's automatic operations in the sequential-addressing mode must be accounted for by modifying the row table during scrolling. In essence, the split-screen capabilities must be incorporated into the row-table function.

During smooth scrolling, an extra (partial) row is displayed. Therefore, the processor updates the table of starting addresses held in the row table to include the starting address of the partial row scrolling onto the screen. This is similar to the procedure required for a character-row insertion. When scrolling up, the processor inserts the new table entry after the entry of what was the last row of the scrolling area. For scrolling down, the new table entry is inserted before the entry of what was the first row of the scrolling area.

The 68000 microprocessor design philosophy

M. KLEWER and B. VERNOOIJ

The 68000 is the most powerful microprocessor available, yet remains one of the easiest to program. The reasons for this can be found in its revolutionary design philosophy. A philosophy that gave first priority to speed and the needs of present-day programmers. And one that made ample allowance for future expansion.

When designing a microprocessor, many questions must be answered. For example:

- should it be compatible with existing 8-bit microprocessors. This affects the whole architecture
- how long should the op code be; the longer the op code, the greater the flexibility
- how should the register set be arranged
- how should the memory be accessed.

This article shows how these questions are answered in the 68000 to allow maximum flexibility to meet the requirements of a wide variety of users.

COMPATIBILITY

Retaining software compatibility with previous 8-bit microprocessors would allow many users to continue using their existing software, but it does have drawbacks. Architectures of early 8-bit microprocessors were rather basic with a hardware-oriented instruction set. This meant they were difficult to update and improve to incorporate new techniques without making them incompatible with the original. Severe design limitations would therefore be placed on a new 16-bit microprocessor based on such an architecture. So to give the 68000 the required power and flexibility, a totally new architecture was developed allowing concepts to be incorporated that have never before been available in microprocessors.

The one area, however, where 8-bit compatibility is advantageous to the 68000 is in peripherals. Since many I/O operations are 8-bit oriented, it was logical to retain this I/O hardware compatibility, even though the 8-bit interface operates at about half the speed of a 16-bit interface.

68000 – computing power for Hewlett Packard's HP9816

HOW MANY BITS FOR THE OPERATION CODE

The flexibility of the 68000 stems mainly from its 16-bit op code. The ADD instruction op code shown in Fig.1 illustrates the power and flexibility available – more than 64 000 different instructions are possible using the 16-bit code.

Existing 8-bit processors use an 8-bit op code that provides only 256 instructions. This may at first appear to be a lot, but consider the example given in Fig.2. The 8-bit op code provides:

– 5 bits that can encode 32 operations – more than adequate for most applications

– 1 bit for selecting one of two registers

– 2 bits for addressing-mode selection

– two data bus transfers to pass instruction and address.

However, if more addressing modes or registers are required, more bits from the op code must be used for selection, reducing the number of bits available to encode instructions and thereby reducing the number of instructions to an unacceptable level.

Compare the 8-bit op code with the 16-bit op code of the 68000. This provides:

- more bits to encode operations – more than 64 000 possible instructions
- one data bus transfer to transfer instruction and address, almost doubling speed
- more registers and addressing modes can be specified without reducing the number of instruction encoding bits to an unacceptable level.

THE REGISTER SET ARRANGEMENT

The 68000 has a general-purpose register set, allowing any instruction to use any register as the source or destination operand or as a pointer in any permitted address mode. This gives considerable programming flexibility.

Registers were originally implemented in microprocessors to speed up manipulation of data. In calculations, most data is operated on several times before a result is obtained, and repeatedly fetching data from external memory is time-consuming. Storing data in internal registers was a simple way of increasing speed, but as soon as one or two registers were introduced, programmers naturally demanded more. The reason for this is obvious. Loading and storing register contents usually means time lost, and if there are only a few registers, this has to be done repeatedly within a program. If more registers are introduced, it is less likely that data will need to be continually transferred between the registers and the memory, and so processing time is reduced.

Two types of register are available to the microprocessor designer, dedicated registers and general-purpose registers, each with its own advantages and disadvantages.

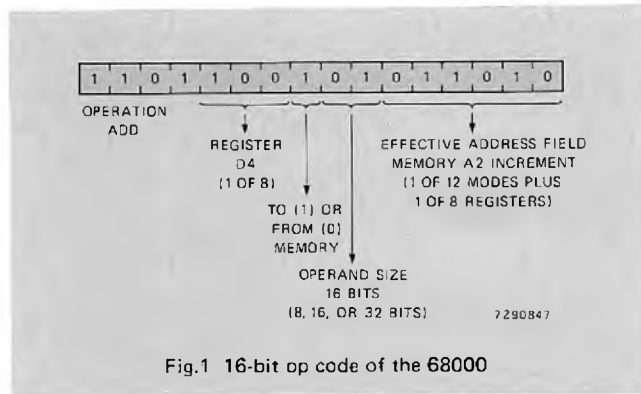


Fig.1 16-bit op code of the 68000

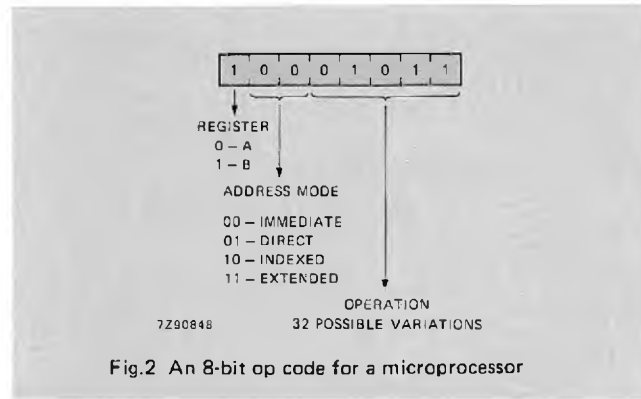


Fig.2 An 8-bit op code for a microprocessor

With dedicated registers, an instruction includes the address of the data to be operated on in a specific register. For example, the ADD instruction can only add the contents of a memory location to one register. If the value to be added to is not in the register then it must be placed there, and the value already there may have to be stored. This has the same effect as having insufficient registers and can be quite troublesome.

Contrast this with the 68000's general-purpose registers where the ADD instruction can add the data in any memory location to that in any internal register. The programmer specifies the register to be operated on in the instruction and avoids transferring data between registers and memory by specifying a free register or a register where the contents can simply be overwritten. Also, the 68000 generally executes an operation faster than a dedicated-register machine. Sixteen general-purpose registers (8 data and 8 address) are built into the 68000. This means that almost any sizeable program can be run without the need to transfer information in the registers just for temporary storage. Also, future development and expansion are not restricted.

Separate address registers for extra safety

When data is moved to or from a register, or is operated on within a register, all condition codes from the operation are important and should be set correctly after the operation. These condition codes can be used to branch or jump or can be used in other data operations.

Moreover, when placing an address in a register, removing an address from a register, or modifying the address by incrementing or decrementing, it is important that the condition codes remain unchanged. Often, in the middle of a long or complex data operation, a new address must be brought in or an existing one modified. If the condition codes were changed then, there would be a risk of disrupting the data operation. In the 68000, this is prevented by using separate address registers so that loading, removing or modifying addresses does not affect the condition codes, or the data registers.

32-bit data registers

Since the 68000 uses 32-bit virtual memory addresses, it obviously requires 32-bit address registers. Experience with 8-bit microprocessors that have 8-bit accumulators and 16-bit index registers has shown up problems caused by having two different register sizes. Getting the two halves of the 16-bit value into the two 8-bit accumulators is awkward enough, but things get worse trying to produce aritmetic-carries from the lower to upper halves.

8-bit processors that could handle 16-bit data had eventually to be updated to handle 16-bit operands. This experience together with that of 16-bit minicomputer users who required 32-bit operations, led to the decision that the 68000 should be able to handle 32-bit operations from the outset.

Once a few 32-bit operations are introduced into a microprocessor, a whole series of 32-bit operations are required. If the multiplication operation results in a 32-bit value then more 32-bit operations are required to do anything else with the value. And so, for consistency (making some software design easier) and speed (any 32-bit operation can be performed with a single instruction), 32-bit data registers were chosen for the 68000.

Memory access

The 68000's 32-bit address registers provide direct access to the contiguous virtual memory. To the programmer, direct access is by far the simplest. It gives a linear view of the memory, and any location can be accessed by using a single address.

With the ever increasing memory capacity required by systems, it was evident that the 16-bit, 64 Kbyte memory addressing range usually adopted for 8-bit microprocessors would be insufficient for the 68000.

In early computers and minicomputers, paging was used to extend the memory addressing range beyond 16 bits by simply adding some bits onto the most significant end of the address. These additional bits were usually stored in page registers. Paging has the advantages of being quite simple and of requiring no real circuit change since the page bits are simply added on to the core. Another advantage is that because only 16 bits of the address are carried in the instruction, the code is fairly dense, saving memory space.

However, paging has many disadvantages, the main one being that pages can only be accessed one at a time. A page register check must therefore be made to ensure that the correct page is being accessed, with the possibility of having to store the current register contents and loading the new page identifier. The page-checking program will require additional software, probably taking up the space saved from carrying only 16-bits in the instruction. Furthermore, the page checking procedure is time-consuming.

To overcome the single page access limit, a number of page registers can be provided (multi-paging). The different access instructions then determine which page register is active. Although multi-paging allows access to more than one page at a time, only one page can be reached by each access instruction without changing the contents of the page register concerned.

A further extension of paging, segmentation, has segment numbers instead of page numbers, and these are added to the 16-bit core address. This allows the core address to be relocated, but the programmer must still ensure that the correct segment is accessed. Another limitation of segmentation is the maximum segment length of 64 Kbytes.

For programming, the simplest addressing method is undoubtedly direct access, as used in the 68000. It provides a linear view of the memory and allows fast access to any location via a single address. Since there is no paging or segmentation, no time-consuming page or segment check is necessary. Simple though it is, direct addressing still allows for more advanced operations such as memory management.

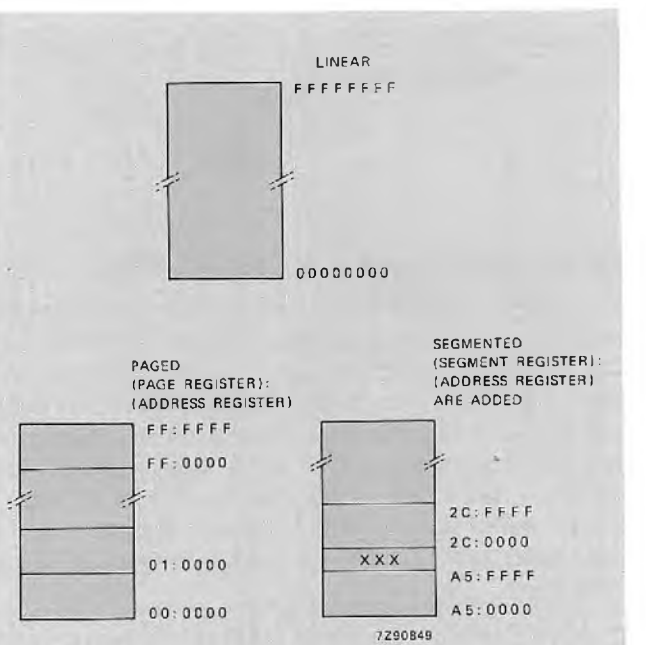


Fig.3 Memory access techniques

Memory management

Memory management is a way to augment the memory accessing method of a processor. In more sophisticated systems, memory management is used to dynamically relocate or to control the various blocks of memory. In large systems, this relocation and control is used for work space protection. Together with the operating system, a separate memory management unit (MMU) adds to or translates an address to prevent illegal access to one user's memory space by another user, whether by fault or design. Memory management may appear to be the same as paging or segmentation, but with memory management, the divisions do not impose any limitations on memory access and so the programmer is unaware of their existence. The programmer can therefore write software as if the entire memory were available. In the 68000 family, the memory management unit is the 68451.

The 32-bit address in the 68000

A 32-bit direct address was chosen for the 68000. A 24-bit address was considered but it was rejected because the odd byte would have been awkward for the 16-bit processor to handle and because in the near future, even 16 Mbytes of directly addressable memory may be insufficient for many systems. Also, since any extension beyond the 16-bit address normally used in 8-bit processors would require two data bus transfers, two complete 16-bit transfers may as well be made. The 32-bit address can, moreover, handle up to 4 Gbytes of memory, leaving ample room for future expansion.

From a packaging viewpoint, 32 address signal lines are a lot to handle. Since few systems require an addressing range of more than 16 Mbytes, only the least significant 24 lines have external connections.

PROCESSING DATA AND ADDRESSES

The 68000 contains three 16-bit arithmetic logic units (ALUs) to process addresses and data. One ALU handles all 16-bit data calculations at a single pass and 32-bit data at two passes, one for the lower word and one for the upper word. This means that 32-bit data operations take about twice as long to perform as 16-bit data operations. The other two ALUs are generally used together for the various 32-bit address manipulations of 32-bit operand effective addresses (EA).* Calculating the EA can be time-consuming. To maintain the speed of the 68000 it is therefore important that this be performed as quickly as possible. For this reason, the calculation is done by two CPUs simultaneously. Since the data ALU works in parallel with the two address ALUs, a 32-bit address and a 16-bit data calculation can both take place at once, considerably speeding up operation.

Another important contribution to the 68000's exceptionally high speed is the use of the prefetch queue, which makes more efficient use of the data bus. This gathers all the necessary instruction information in advance of the instruction, and is then ready to execute the instruction at the appropriate time. In gathering information, the microprocessor uses the otherwise idle bus to fetch information from memory before it is actually required. The prefetch queue therefore saves time, since operations are not delayed by instructions waiting for information. Also, the data bus is used more efficiently with the prefetch queue.

The program space, where the prefetch queue collects information, contains op code and addressing details. The prefetch queue can contain sufficient information to execute one instruction, decode the next instruction, and fetch the following instruction – all at the same time. For example, when a conditional branch instruction is detected, the prefetch is either ready to branch or not by the time the decision is made. The queue tries to fetch both the op code following the branch instruction and the op code at the destination of the branch. Then, when the conditions are compared and a decision made whether or not to branch, the processor can begin immediate execution of either instruction, ignoring the other unnecessary op code.

The prefetch queue can also be used in other ways to increase operating efficiency. For example, in repetitions instructions the prefetch queue is used to speed up successive data transfers. It allows many instructions that are used repeatedly to be executed in the time it takes for the queue to collect the next op code.

* An effective address (EA) is the location determined with respect to the selected addressing mode. In the 68000, in the program-counter-relative-with-offset addressing mode for example, the EA would be the result of adding a 16-bit displacement to the contents of the program counter.

COMPATIBILITY WITH FUTURE DEVELOPMENTS

In every aspect of the 68000 design, ease of programming and speed were given highest priority. Today, in the 68000, we have the fastest, most powerful microprocessor available and yet one that is still simple to program. And in the 68000, we have a microprocessor that is safe from future-shock, whose architecture has plenty of room for expansion. Moreover, future developments will be fully compatible with the 68000. Devices already available in the 68000 family include, enhanced communications and direct memory access interfaces, a multi-protocol communications controller, and a dual asynchronous receiver/ transmitter. In the 68000 family, we have a series of devices for today's and tomorrow's applications.

VHF power amplifiers with broadband input circuitry

HANS FIEDELDIJ

In recent years the demand by broadcasting authorities for transmitter systems with fewer amplification stages has led to a new generation of high-power (up to 30 kW) high-gain power tetrodes. Among these the YL1610, YL1630 and the YL1631 hold a unique position. With their latest computer-aided-designed electrode configuration, combined with new cavities incorporating a specially designed two-stage impedance transformer, these tubes can operate, without tuning, over exceptionally broad input bandwidths – 82 to 110 MHz in band II and 170 to 250 MHz in band III.

The advantages of broadband input circuitry are obvious, and include

- easier transmitter operation
- easier transmitter servicing and maintenance, and longer intervals between servicing
- easier tuning (with no input tuning needed)
- and simplified transmitter circuitry.

Moreover, with these new cavities, the need for frequency dependent (i.e. adjustable) neutralization is completely eliminated.

This article describes these new tetrode/cavity combinations – which for broadband operation work in the grounded-grid/grounded-screen-grid mode – in particular the design of the transformer sections that allow broadband operation. The tubes find application in the following areas:

VHF tv band III

YL1610 – 10 kW peak sync (vision stage)
YL1630 – 30 kW peak sync (vision stage)
YL1631 – 10 kW peak sync (combined vision and sound).

FM radio band II

YL1631 – 10 kW.

THEORETICAL BASIS

The principle of impedance transformation using quarter-wave stepped transformer sections is well documented and need not be discussed in detail. It's sufficient here simply to point out some of its important features and to show how such a transformation is realized with the YL1610, YL1630 and the YL1631.

When a quarter-wave transmission line of characteristic impedance Z_0 is terminated with an impedance Z_1, its input impedance will be Z_0^2/Z_1. So an impedance Z_2 can easily be transformed to an impedance Z_1 by connecting a quarter-wave line of impedance $\sqrt{Z_1 Z_2}$ between them. If, however, Z_1 and Z_2 differ considerably, the transformation will be frequency sensitive, i.e. correct matching will occur at one frequency only, f_0 say. This is apparent from the following expression relating vswr S at the transformation to frequency deviation Δf from f_0

$$S = 1 + \frac{\pi}{2} \frac{|\Delta f|}{f_0} \left| \sqrt{\frac{Z_2}{Z_1}} - \sqrt{\frac{Z_1}{Z_2}} \right|$$

For given values of Z_1 and Z_2, S increases linearly with $|\Delta f| / f_0$. For a two-stage transformer, the expression becomes

$$S = 1 + \frac{\pi^2}{4} \left(\frac{\Delta f}{f_0}\right)^2 \left| \sqrt{\frac{Z_2}{Z_1}} - \sqrt{\frac{Z_1}{Z_2}} \right|$$

which because the factor $(\Delta f/f_0)$ is squared, is far less frequency sensitive. So for broadband matching, the impedance transformation from Z_2 to Z_1 should be done in two (or more) stages.

Furthermore, if operating requirements place an upper limit for S of 1.4 say, over a passband of 60 MHz centred on 200 MHz (band III operation), the impedance transformation by two successive quarter-wave transformers should not exceed a factor 4, i.e. $Z_2/Z_1 \leqslant 4$ over each stage.

Based on the work of J. J. Warringa and H. Piepers of Philips Development and Application Laboratory for transmitting tubes.

BROADBAND MATCHING WITH THE YL1610, YL1630 AND YL1631

Figure 1 shows schematically the interior grid-to-filament (evacuated) region of a VHF tetrode. The interaction space between the active parts of the grid and filament assembly is represented by capacitor C and resistor R (r.f. drive-voltage/filament-current in a grounded-grid circuit). Two coaxial line sections of wave impedances Z_{01}, Z_{02} represent the electrode supports and their connections to the outer tube seals, and capacitor C_1 represents the ceramic insulation between grid and filament.

In a high gain tetrode, a typical value for R would be around 15 Ω. In the YL1610, YL1630 and YL1631 tetrodes, the transformation from the interior grid-filament assembly to the 50 Ω r.f. input is done in two steps:

- a down-transformation to the external filament and grid electrodes, performed in the cavity by adding a capacitive element C_t (broken line in Fig.1) in parallel with C_1, C_t being formed by a low impedance coaxial line section between the external grid and filament seals (at the input of this line the impedance is purely resistive)
- and an up-transformation to 50 Ω, performed in the cavity by a two-stage impedance transformer section (Fig.2). The first stage consists of six quarter-wave coaxial lines connected between the filament and grid electrode contacts, at equal intervals around their circumference. These connect, in two groups of three, with two quarter-wave sections forming the second stage.

The down transformation is effectively an intermediate stage needed to transform the resistance R of the interior filament-grid assembly to a resistance R_1, that can be transformed to 50 Ω by the two-stage section.

By splitting the first stage of the transformer section into six parts, the coaxial nature of the signal path is preserved in the cavity.

Consider now Fig.2. The first transformer stage splits R_1 into six resistors in parallel, each of value $6R_1$. Each of these is transformed by a quarter-wave line of characteristic impedance Z_0 to a resistance $Z_0^2/6R_1$. The parallel combination of these resistances, in two groups of three along the first transformer section, produces two resistances of $Z_0^2/18R_1$. These are then transformed by the second transformer section to resistances $18R_1$, and the parallel combination of these resistances gives a value of $9R_1$.

This final resistance will be 50 Ω provided $R_1 = 5{,}5\ \Omega$, and this value is assured by appropriate choice of C_t in the external grid-filament seals.

Furthermore, the first and second transformer stages provide impedance ratios of 2,3 and 3,9 respectively, which more than meet the above requirement for a vswr ⩽ 1,4 over a 60 MHz bandwidth.

Figure 3 shows a section through a YL1610 and its cavity. The transformer sections are formed by 50 Ω coaxial lines, only one of which is shown in the figure. The

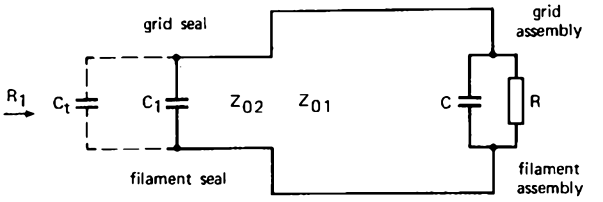


Fig.1 The interaction space between the active parts of the grid and filament assembly of a transmitting tetrode may be represented by a capacitance C in parallel with a resistance R. Two coaxial line sections of wave impedances Z_{01}, Z_{02} represent the electrode supports and their connections to the outer tube seals, and capacitance C_1 represents the ceramic insulation between grid and filament. Capacitance C_t in parallel with C_1 transforms resistance R to R_1

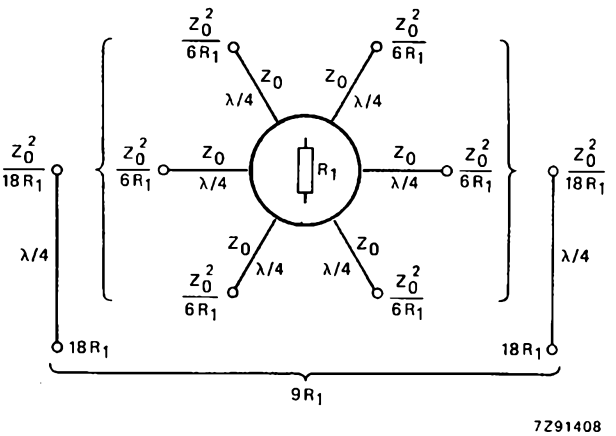


Fig.2 Up transformation from R_1 to 50 Ω is done in the cavity by a two-stage impedance transformer section. The first stage consists of six quarter-wave coaxial lines connected between the filament and grid electrode contacts, at equal intervals around their circumference. These connect, in two groups of three, with two quarter-wave sections forming the second stage. The final resistance of $9R_1$ equals 50 Ω provided R_1 is 5,5 Ω

conductor of each line in the first section connects with the filament contact in the cavity, and the screen connects with the grid contact.

Capacitive element C_t is formed in the cavity by a low-impedance transformer section in which coupling and blocking capacitors are integrated.

The control circuitry within the cavity is shown in Fig.4, and Fig.5 shows the YL1630 cavity with its side removed to show the first transformer section.

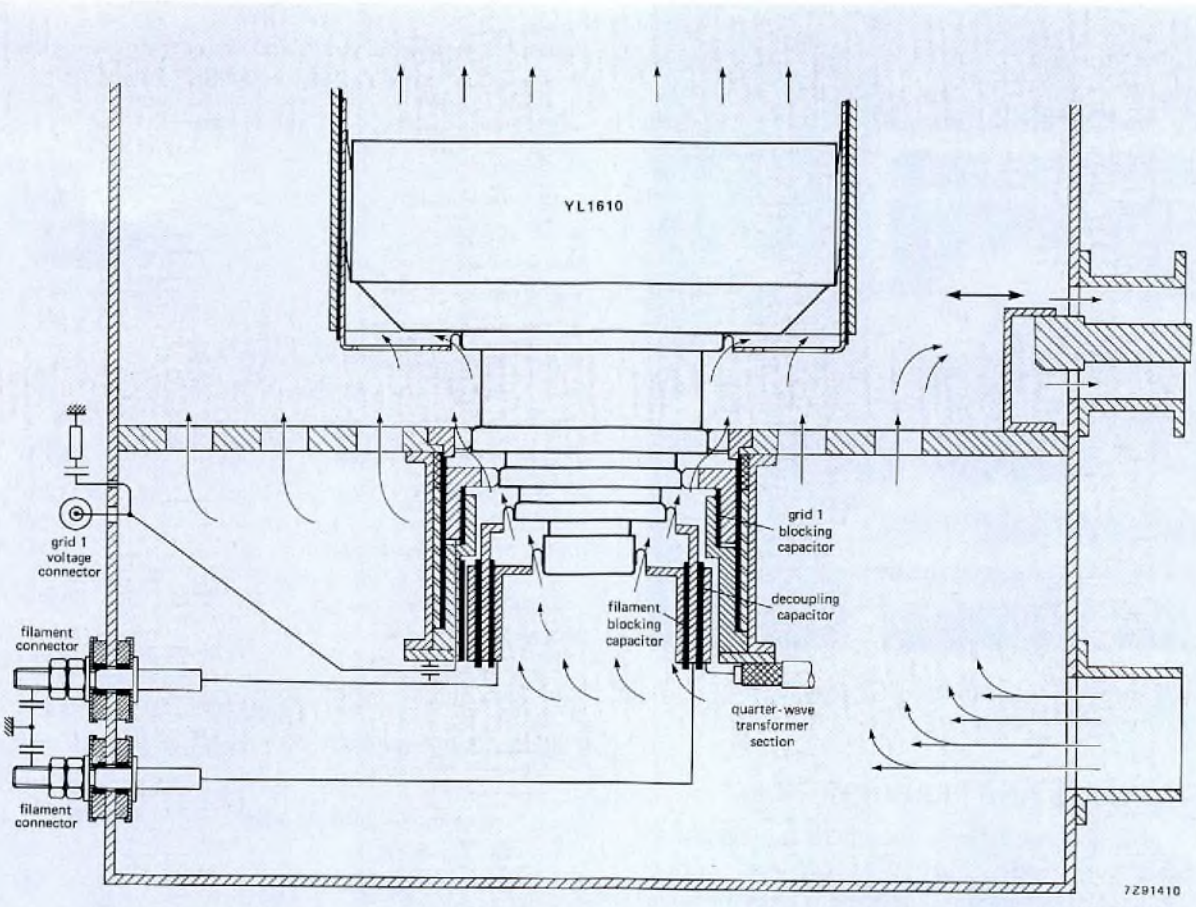


Fig.3 Section through a YL1610 and its cavity. The transformer sections are formed by 50 Ω coaxial lines, only one of which is shown in the figure. The conductor of each line in the first section connects with the filament contact in the cavity, and the screen connects with the grid contact. Capacitance C_t is formed in the cavity by a layer of dielectric on the inner surface of the grid connector, extending partly around the circumference

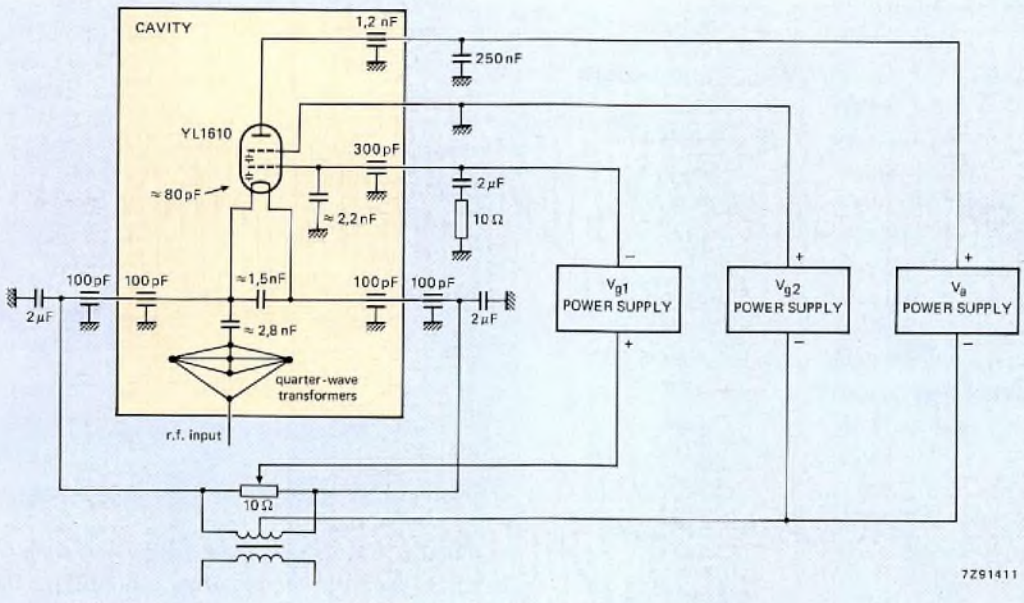


Fig.4 Control circuitry for the YL1610

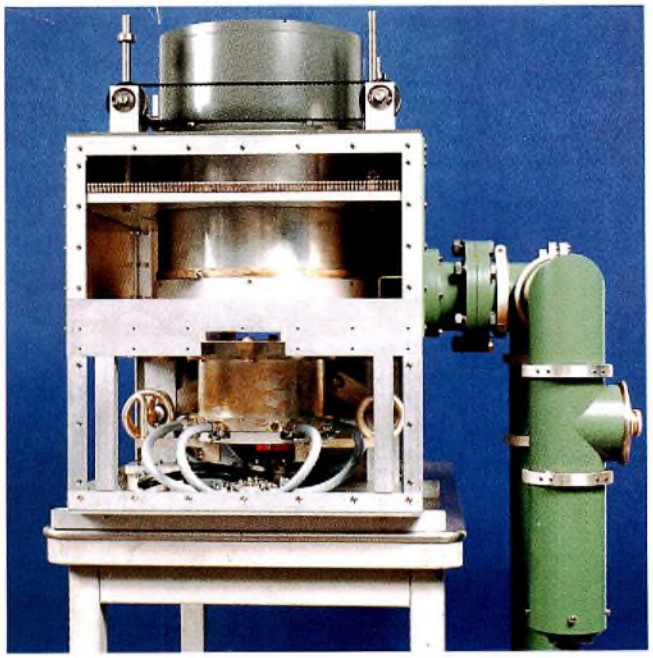


Fig.5 YL1630 cavity with its side removed to show the first transformer section.

SPECIFICATIONS AND PERFORMANCE

Tables 1 and 2 give respectively the operating conditions and specifications of the YL1610/YL1630 and of the YL1631 for band III operation, and Table 3 gives the same information on the YL1631 for band II (FM) operation.

TABLE 1
Class AB vision amplifier with the YL1610 in 40787 cavity, and YL1630 in 40786 cavity

double-tuned anode circuit, cathode driven	YL1610	YL1630
frequency of vision carrier	up to 250 MHz	up to 250 MHz
bandwidth (−1 dB)	8 MHz	8 MHz
anode voltage	5,5 kV	7,0 kV
grid 2 voltage	500 V	500 V
grid 1 voltage	50 V	50 V
anode current, zero signal	1,2 A	1,2 A
anode current, black level	2,9 A	5.7 A
grid 2 current, black level	100 mA	150 mA
grid 1 current, black level	20 mA	180 mA
output power in load, sync	11 kW	30 kW
output power in load, black level	6,6 kW	18 kW
gain, black level	17 dB	18 dB
sync compression	30/25	30/25
differential phase	$<3°$	$<5°$
differential gain	$\geqslant 90\%$	$\geqslant 90\%$
l.f. linearity	$\geqslant 90\%$	$\geqslant 90\%$
filament voltage	8 V	8 V
filament current	113 A	185 A

TABLE 2
Class AB combined vision and sound (10:1) amplifier with the YL1631 in 40786A cavity

double-tuned anode circuit, cathode driven	
frequency	up to 250 MHz
bandwidth (−1 dB)	8 MHz
anode voltage	7 kV
grid 2 voltage	900 V
grid 1 voltage	100 V
anode current, zero signal	1,8 A
anode current, black level + line sync pulse	3 A
grid 2 current, black level + line sync pulse	50 mA
grid 1 current, black level + line sync pulse	0
output power in load, sync	10 kW
drive power, sync	$\leqslant 250$ W
power gain	$\geqslant 16$ dB
intermodulation products	$\leqslant -54$ dB
filament voltage	10,4 V
filament current	115 A

TABLE 3
Class AB FM amplifier with the YL1631 in 40788 cavity

frequency	80 to 250 MHz
bandwidth (−3 dB), 80 MHz	2,5 MHz
anode voltage	7,5 kV
grid 2 voltage	700 V
grid 1 voltage	−100 V
anode current, zero signal	0,5 A
anode current	2,1 A
grid 2 current	50 mA
grid 1 current	10 mA
anode input power	16 kW
anode efficiency	69%
drive power	200 W
power gain	17 dB
output power in load	11 kW

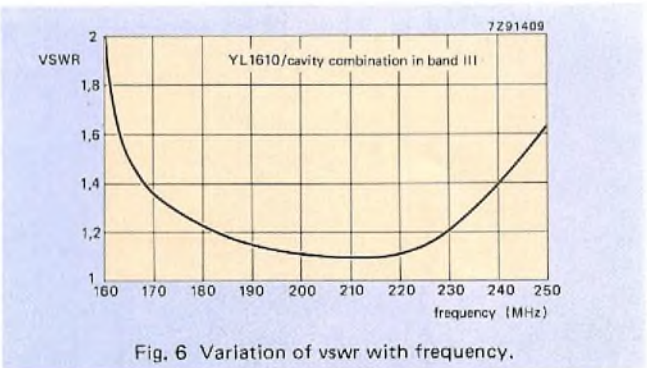


Fig. 6 Variation of vswr with frequency.

Finally, Fig.6 shows how vswr varies with frequency for a YL1610/cavity combination operating in band III. The system maintains a vswr of less than 1,4 between 170 and 240 MHz.

Two-chip modem for FSK data transfer

R. BLAUSCHILD and R. FABBRI

Until now, designers who wanted to send frequency-shift-keyed data over local networks at high speeds had to do so using board-level modems. But an FSK modulator and demodulator chip set that works at up to 2 Mbit/s in half-duplex operation – the highest rate of any FSK modem – has dramatically changed that. What's more, the NE5080 transmitter and NE5081 receiver relay information over 30 km of 75 Ω cable without signal refreshing – and with greater noise immunity and lower cost and bit error rates than many other data transmission schemes. Furthermore, although the chip set's data rate is lower than Ethernet's 10 Mbits/s, when used in a deterministic system the pair can handle a comparable throughput.

OPERATING MODES AND OPTIONS

The modem transmits and receives data over a single phase-continuous channel in accordance with IEEE P802.4, which establishes the specifications for token-passing bus networks that use 75 Ω coaxial cable. Token passing allows a large number of modem taps along the cable. The bit-error rate for data transmitted through a tap is 1 in 10^{12}, well within the limit of 1 in 10^9 established by P802.4.

The chip set, however, is not meant exclusively for token-passing networks. It can also implement simple point-to-point communications systems. In such systems, the transmitter drives a sine-wave carrier onto the coaxial cable and is capable of putting 2 V peak to peak across a 37,5 Ω load (two 75 Ω loads in parallel at the transmitter) with a typical sine-wave distortion of 2%. Once set, the stable carrier frequency will drift less than 200 ppm/K.

By using different carrier frequencies and data rates, the performance of a point-to-point system can be tailored to further extend communication. The carrier frequencies are set by a 130 pF capacitor, and the receiver is tuned with a 40 μH choke. Transmission distance, however, is a function of both the data rate and the type of cable used, as well as of the carrier frequency (see table). With RG-59 cable and a 2 Mbit/s rate, for example, the maximum transmission distance is about 1300 m. At 500 Kbit/s and using JT 4750J cable, on the other hand, data can be sent nearly 16 km. Furthermore, since FSK transmission operates over a narrow frequency band, where the propagation velocity is constant, coaxial cable equalization is unnecessary. However, the chip set is not limited to using only coaxial cable. At a carrier frequency of 280 kHz, for instance, it can operate at 56 Kbit/s over almost 2,5 km of twisted-pair wire.

Maximum cable lengths for an FSK local network

data rate (Mbit/s)	f.m. carrier frequency (MHz)	cable type				
		RG-59	RG-11 (foam)	JT4412J	JT4750J	T41000J
0,5	1	1,8 km	6,4 km	10 km	15 km	30 km
1,0	3	1,5 km	3,6 km	6 km	9,8 km	15 km
2,0	5	1,3 km	2,9 km	4,5 km	7,6 km	11,4 km

Because an FSK modem employs carrier frequency shifts (upward or downward) from a specific baseband frequency rather than a change in signal amplitude to signify data bits, it is relatively independent of the amplitude or voltage level of the received signal. Thus the modem functions over a much longer distance than a digital transceiver can. In addition, transmissions using FSK modulation introduce fewer bit errors than digital baseband transmissions, such as those used for Ethernet, because the spectral bandwidth of an FSK transmission is in an r.f. region where coaxial signal delays vary linearly and relatively long cables produce undistorted waveforms.

Frequency-shift keying's relative insensitivity to voltage levels means that it has a high degree of environmental noise immunity. That is particularly important in nuclear power plants, electrical switchyards, and other settings where random high-voltage spikes are commonly generated. In fact, the Computrol 30-0078 FSK modem board, which is the predecessor of the chip set, has attained a bit error rate of less than 1 in 10^{12} in high-noise electrical environments, for a signal-to-noise ratio of 20 dB. Implementing such systems in silicon in the NE5080 and NE5081 reduces both power dissipation and component count and adds functions that make possible compatibility with P802.4. A two-chip implementation, in addition, avoids some of the thermal and ground loop problems that would result from placing the transmitter and receiver on one IC. Moreover, going to two chips means that low-cost DIPs can be used for both.

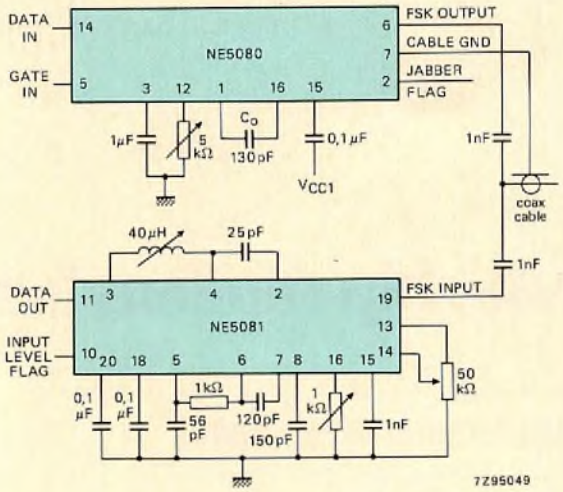


Fig.1 NE5080 and NE5081 connected as a half-duplex FSK modem. With the external components shown the modem operates at a carrier frequency of 5 MHz and a data rate up to 2 Mbit/s

Point-to-point service

Point-to-point systems are typically half-duplex, using a transmitter and receiver pair on a 75 Ω coaxial cable (Fig.1). P802.4 requires that the transmitter output mark frequency (data 1) be set at 6,25 MHz. This is done by grounding the Jabber Control and the Transmission (TX) pins (3 and 5, respectively), applying a TTL high to the data input (pin 14), and adjusting the 5 kΩ potentiometer (pin 12). An internal resistor ratio within the NE5080 automatically sets the space frequency (data 0) to 3,75 MHz, ±80 kHz. The receiver is tuned by adjusting the choke (between pins 3 and 4) for minimum jitter at the data output with an FSK pseudo-random data-pattern input.

Network service

Ways of interfacing with a coaxial cable in a token-passing local network with a bus architecture are shown in Fig.2. As specified by P802.4, a passive tap uses a simple T connector on the 75 Ω cable, with a short stub (45 cm) to the modem. The modem, in turn, provides a TTL interface to the node.

Active taps can also be implemented by putting the modem on the cable and using RS-422 drivers and receivers to send data to and from the node over twisted-pair wire. The maximum transmission rate over a twisted-pair cable, however, is limited to 1 Mbit/s.

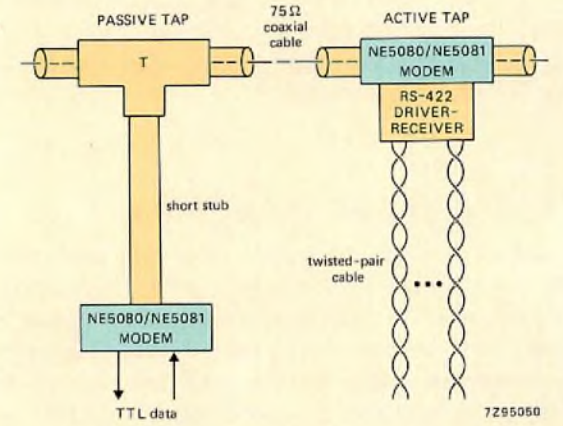


Fig.2 Passive and active coaxial-cable taps. The active tap uses an RS-422 driver-receiver for communication with peripherals remote from the cable

An example of such a system, an office automation network, is shown in Fig.3. Some modems are connected, through RS-422 interfaces, to distributed computing subsystems up to a hundred metres away from the network's coaxial cable; an intelligent cluster controller makes each subsystem unaware that it shares a single modem to the system's 75 Ω coaxial cable.

A designer's choice between the two main branches of the IEEE P802 specification is typically one between deterministic and probabilistic networks. The former are token-passing schemes; the latter, carrier-sense multiple access with collision detection (CSMA/CD).

In a deterministic network, only one transmitter has access to the line at any one time. In a CSMA/CD network – typified by Ethernet – access to the cable is available on a probabilistic basis. In other words, there is only a *probability* that the line is free at any time – even with no carrier sensed. That probability can be estimated from the ratio of the bus propagation delay to the packet transmission time (see the graph fpr Ethernet systems). The larger this ratio, the greater the chance of collision. Consequently, long packets create fewer collisions whereas short packets create more.

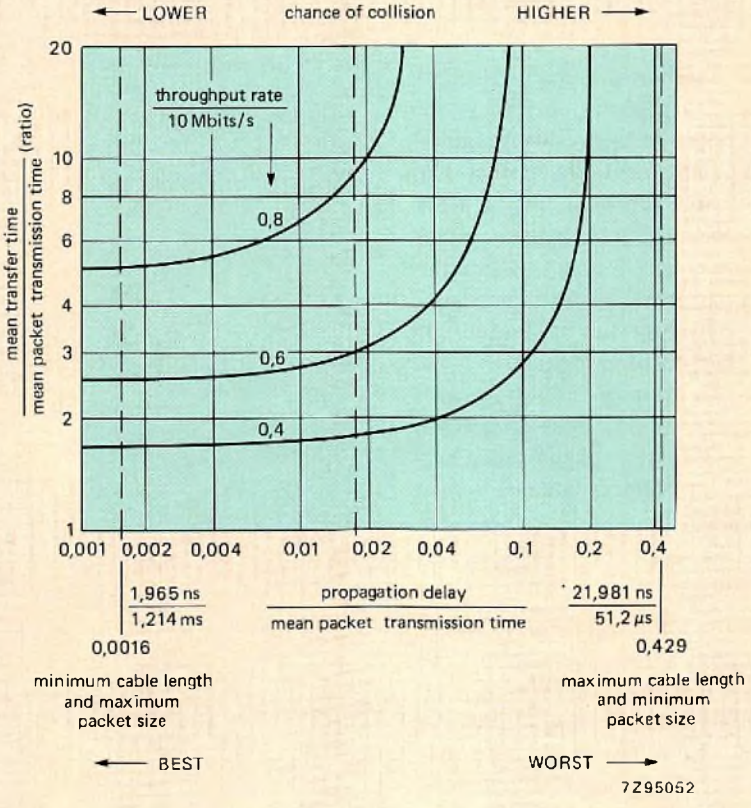
The probability of collisions also increases with more frequent requests from nodes. As demand increases, the shorter packet transmissions will force the bus arbitration time and the queue for all transmissions to increase exponentially. To prevent the line from going "unstable" (which occurs when the waiting time reaches infinity), demand must be kept well below 40% of the available channel bandwidth.

Ethernet's popularity has largely been a consequence of its use in office automation networks that are relatively noise-free and insensitive to transmission delays. Users in these settings can afford to wait for access to the line; in fact, the typical demand level for office networks is 1%, and the worst-case average demand is 8%. That means that Ethernet's 10 Mbit/s aggregate throughput is practically never achieved with heavy cable loading conditions.

Token-passing networks in contrast, handle access rights by passing them from node to node; only a node that receives a token is allowed to transmit. Under worst-case conditions, the P802.4 token-passing network operates with a bandwidth efficiency of nearly 98%. The very efficient use token passing makes of its bandwidth means that a deterministic network with a 1 Mbit/s data rate – such as the one implemented with the NE5080 and NE5081 FSK modem chip set – can surpass the performance of an Ethernet system.

In other words, an FSK token-passing network with 97,6% of its 1 Mbit/s channel in use will deliver 970 kbit/s, whereas an Ethernet system with 8% efficiency on a 10 Mbit/s channel delivers only 800 kbit/s.

Up till now, deterministic network schemes have been most widely used in industrial control, factory automation, and military and aerospace environments where real-time control of the communications line is critical. The relative ease with which a determinsitic token-passing network can be implemented using the 5080 and 5081 modem chips, its relative freedom from noise, and its longer transmission distance – plus its lower cost – may pave the way for deterministic schemes in offices of the future as well.



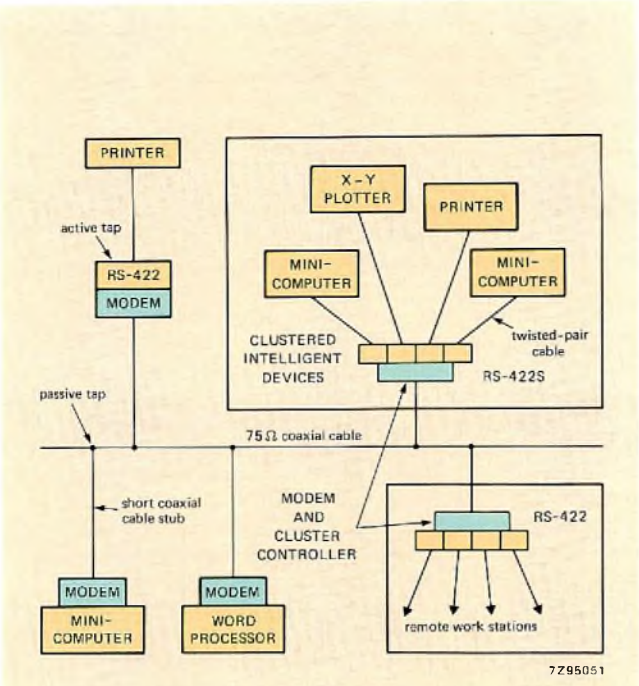


Fig.3 A token-passing network with bus architecture (IEEE P802.4) can accommodate many modems and any combination of active and passive taps. Intelligent controllers can direct traffic via RS-422 driver-receivers to clustered users

This technique reduces the number of taps on the cable and is especially useful where intelligent subsystems are clustered in a distributed processing environment. An added advantage of a token-passing implementation is that any mixture of active and passive taps can exist on the same 75 Ω cable. Thus a user can economically configure a system by specifying low-cost passive taps at nodes where the distance from the cable to a peripheral is short, and more expensive active taps where a longer run is needed for clustered layouts or for other architectural reasons.

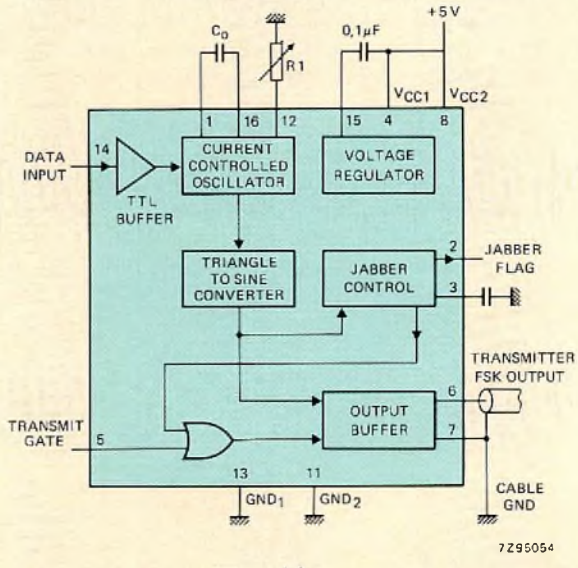
By contrast, Ethernet systems must be fitted only with active taps and must use expensive 50 Ω cable. Moreover, although Ethernet works at 10 Mbit/s, a token-passing network – even one with just a 1 or 2 Mbit/s data rate – may offer a higher aggregate throughput.

Adjusting the carrier frequency

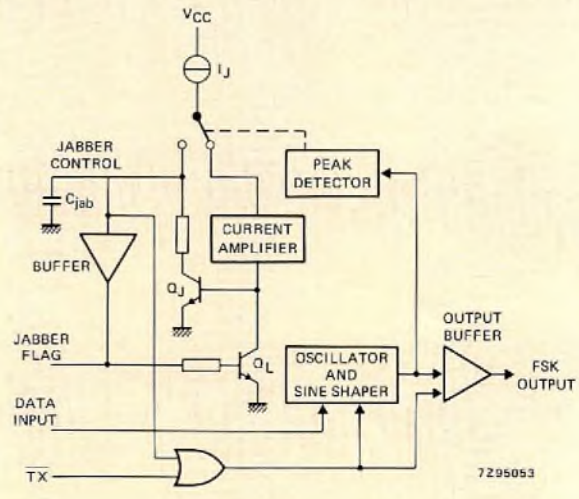
The carrier frequencies of the NE5080 and NE5081 can be adjusted for other applications simply by altering the charging time constant of the capacitor C_O. With 130 pF for C_O, for example, the transmitter conforms to P802.4 specifications with a 5 MHz center frequency, 3,75 MHz data 0, 6,25 MHz data 1, and 2 MHz maximum switching rate. Simply changing C_O from 130 pF to 0,013 μF, however, will convert a 2 MHz transmitter into a 50 kHz twisted-pair cable driver.

Output gating

The output buffer can drive 2 V peak-to-peak into a 37,5 Ω load during transmission or can be gated into a high impedance state under network control. Figure 4 shows the logic that gates the transmitter output. A high at the TTL-compatible TX input shuts down the oscillator as well as the output buffer. This eliminates any possibility of the carrier signal feeding through to the output with the buffer turned off. The design of the gate structure allows the oscillator to go from shutdown to a stable carrier frequency within 1 μs of the beginning of a transmit signal (logic low at the TX input).



(a)



(b)

Fig.4 (a) Block diagram of the NE5080 transmitter; (b) output buffer and jabber control

Jabber control

In a token-passing network, it is imperative that only one transmitter operate at any given time. If a fault occurs at a node, causing the transmitter line to remain low indefinitely, its associated transmitter could remain active (a condition known as jabbering) and tie up the network. For this reason, a redundant Jabber Control pin is provided, which can turn the transmitter off using either an external system's logic or an internal fault detector.

The transmitter, in addition, has a built-in watchdog timer that shuts it off after a specified transmission length (400 ms for P802.4) if the TX line has not otherwise been pulled high. A peak detector, used to sense when the oscillator is active, controls a current source, Q_J, that under ordinary conditions holds the Jabber Control low.

However, if the TX line is not pulled high by the time it takes integrating capacitor C_{jab} to charge to a TTL high level, the Jabber Control goes high, disabling the output buffer, shutting down the oscillator, and throwing up a Jabber Fault Flag. The transmitter remains off until the Jabber Control pin is pulled low by external means.

The maximum allowable time that the transmitter is on, however, can be adjusted by changing the value of C_{jab}. Alternatively, the Jabber Control function can be disabled for continuous transmission by grounding the Jabber Control pin.

NOISE AND DYNAMIC RANGE CONTROL

The receiver uses a quadrature detection path consisting of a limiter, phase-shifter, precision analog multiplier, low-pass filter, and a comparator (Fig.5(a)). It is tuned by adjusting the tank circuit of the phase shifter to resonate with the incoming carrier center frequency.

Although the design of the chip set provides a high degree of noise immunity, external passive low-pass filter components help optimize system performance for a variety of applications. The design of the filter is important since less roll-off will allow higher measurable noise levels; a sharper roll-off will introduce phase distortion and jitter at the data output.

Since the limiter and multiplier combine to yield a gain greater than 80 dB, a level sensor is used to prevent noise at the input from being sent to the output TTL buffer as valid data (Fig.5(b)). The levels on pins LD_1 and LD_2, in fact, determine the minimum acceptable FSK input level, as well as the dynamic range of the receiver.

Dynamic range selection

The widest input dynamic range, about 47 dB, is obtained by grounding LD_1. The system then accepts any signal above the 6 mV peak-to-peak hysteresis level of the input comparator. Since this renders the system susceptible to

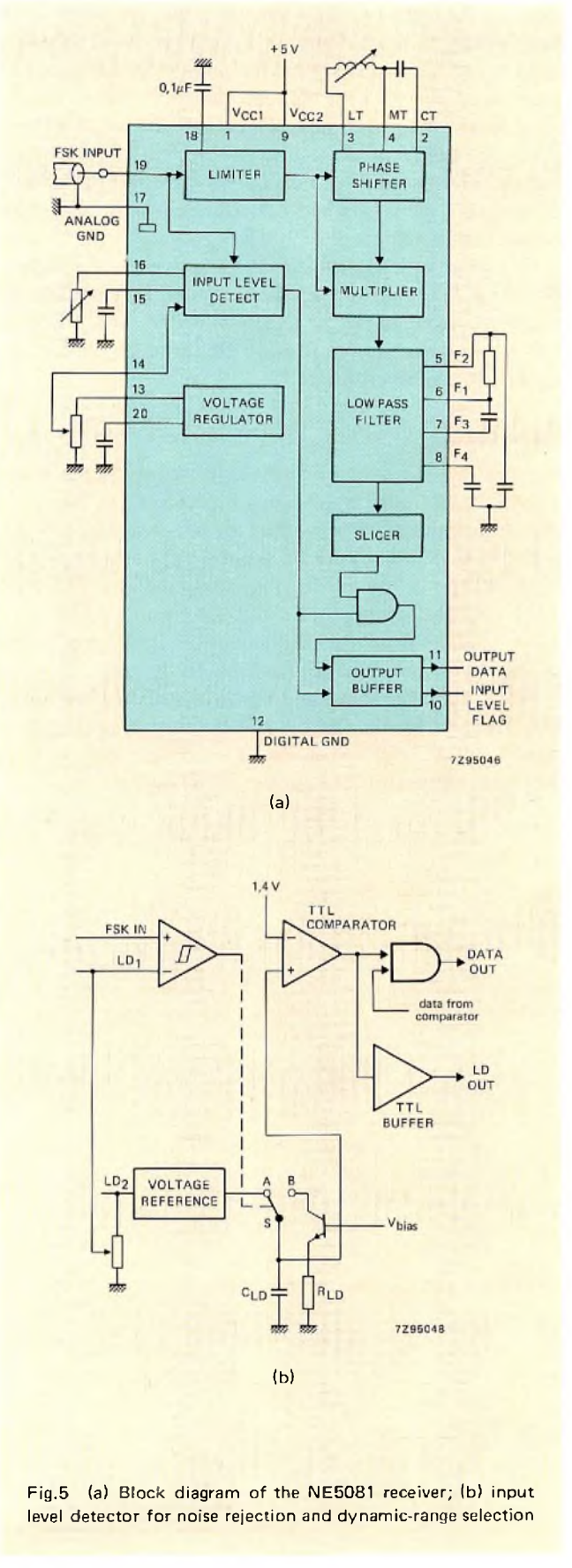


Fig.5 (a) Block diagram of the NE5081 receiver; (b) input level detector for noise rejection and dynamic-range selection

noise on the cable (with an associated increase in bit-error rate), it may be more desirable to limit the input dynamic range to the minimum required for a particular cable length, which is calculated from the maximum transmitter output variation (6 dB for this modem), the attenuation characteristics and length of the cable, and the background noise level of the environment. For low bit-error rates in a noisy environment, pins LD_2 and LD_1 can be wired together to produce a dynamic range of 20 dB.

For applications in which the output is gated independently of the input levels, the detection circuitry can be disabled by connecting the C_{LD} pin to V_{CC}. This produces a dynamic range greater than 60 dB, although with a predictably higher bit-error rate.

Noise gating

In operation, the limiter and multiplier combination in the receiver is controlled by charging capacitor C_{LD}. When the peak FSK input signal is less that the preset voltage at LD_1, switch S remains in position B and C_{LD} holds no charge. In effect, the voltage on C_{LD} is considered as a TTL level by the internal comparator and is used with an AND gate to prevent data from reaching the output. In this way, noise on the cable is not mistaken for a low-level signal.

When the peak FSK input signal exceeds the voltage at LD_1, S_1 moves to position A and the C_{LD} is charged to a known voltage level well above a 1.4 V TTL reference. Data from the comparator then appears at the output.

Although the charging takes place rapidly, the discharge time is controlled by the values chosen for R_{LD} and C_{LD}. The discharge time should match the delay path through the receiver from the FSK input to the comparator's output. If the discharge rate is too fast, the receiver cuts off before the valid data has passed completely through the low-pass filter and information is lost. If the discharge rate is too slow, noise is gated through the system following a valid transmission.

The receiver tolerates up to a half period of the lowest transmission frequency. The delay time can be optimally adjusted, however, for about five periods of the lowest transmission frequency. That affords the user a considerable amount of flexibility: an additional range is selecting level-detection settings and low-pass filter delays.

Acknowledgement

The authors would like to acknowledge the contribution of Robert G. Meyer, professor of electrical engineering at the University of California at Berkeley, for his design of the NE5080/NE5081 FSK modem chip set, and Sheldon Pearlman, vice president of Engineering, and Gunther Martin, Senior Analog Engineer of Computrol Division of Kidde Automated Systems (Ridgefield, Conn.), for their substantial contributions to the designs and this article.

The BTV60 first in a new generation of GTOs

ARTHUR WOODWORTH

Much has been written on the power and versatility of the GTO (Refs 1 to 3). On how, for example, it combines the high blocking voltage and high overcurrent capability of the thyristor with the fast switching of the bipolar transistor. And on its modest drive-power requirements and simple drive circuitry, which (in contrast to the thyristor) has no need of auxiliary commutating switches, chokes and capacitors.

Much has been written too, about its limitations. Its forward voltage drop, for instance, which at switching frequencies up to 1 kHz is likely to be a major source of loss. And its turn-off losses, appreciable at frequencies over 2 kHz and a major limitation on its re-applied dV/dt – which in turn places limits on the maximum power it can switch.

Now, however, the introduction of a second generation of GTOs, heralded by the BTV60, allows fast, efficient switching, at up to three times the power of equivalent first generation GTOs. This article describes this new generation of GTOs, characterized by a much finer cathode structure, and shows how these new devices offer a real and attractive alternative to former devices.

FINE CATHODE GEOMETRY ALLOWS FOR HIGHER CURRENT SWITCHING

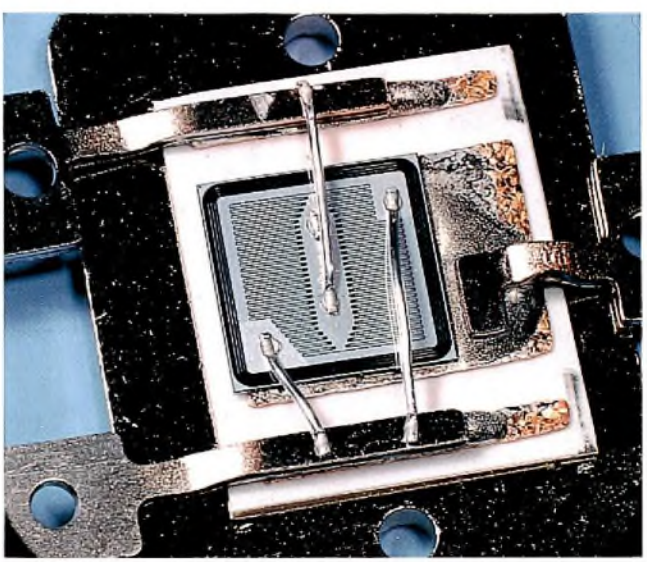
To increase the anode current that a GTO can switch it's necessary to extract higher gate currents. The maximum current $I_{GR\,max}$ that can be extracted from the gate is related to the cathode finger width S, the gate-cathode breakdown voltage V_{br}, and the average resisitivity ρ_{sc} of the p-base by

$$I_{GR\,max} \sim V_{br}/[\rho_{sc}\,S]$$

To maximize I_{GR}, therefore, a choice must be made between increasing V_{br}, reducing ρ_{sc} and reducing S.

The first choice would deprive the GTO of one of its major advantages, i.e. its ability to be switched by low voltage sources. The second choice, i.e. reducing ρ_{sc}, means increasing the width and doping level of the p-base. But this would reduce α_{npn}, increasing the on-state losses and, in particular, increasing the turn-on gate current required.

In contrast, the third choice, i.e. reducing cathode finger width, has none of the accompanying disadvantages of the other two choices. It does, however, have profound effects on device design.



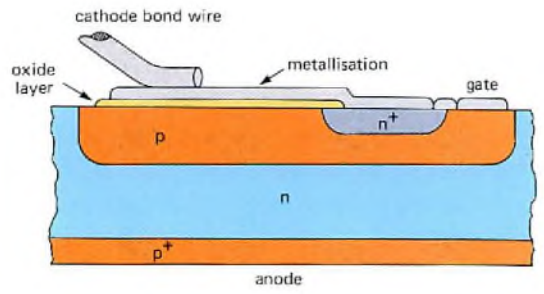
The BTV60 chip is characterized by a much finer cathode structure than equivalent first-generation GTOs, and can switch up to three times the power

DESIGN CONSIDERATIONS

The cathode fingers in the BTV60 (see photograph) are between 1/3 and 1/4 the width of those in former GTOs. Such fine geometry places quite severe demands on the photo-lithographic manufacturing processes, with the result that the new devices must be manufactured using planar technology, rather than the mesa-trough technology used for conventional GTOs.

Cathode contacts

Figure 1 shows a section through the BTV60 chip. With its fine cathode structure, a single wire contact direct to the cathode is impracticable, since such a wire, which must be capable of handling average currents of around 25 A, would be about five times the width of a single finger. Instead, the wire contact is bonded to a separate bonding pad that connects directly with the cathode structure. An oxide layer isolates the bonding pad from the underlying p-layer to prevent it acting as a single cathode finger (which would severely limt I_{TCM}).



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Gain control

In first-generation GTOs, anode-shorts aligned with the cathode fingers are used to set the gain. The finer cathode structure of the BTV60, however, would make alignment of these shorts difficult. We have therefore dispensed with them, and we set the gain in the BTV60 during manufacture by a combination of controlled diffusion of the n^+/p region, and gold doping to limit residual-charge recombination time.

Passivation

The glass-passivation techniques used with first-generation GTOs are unsuitable for the flat, thin chip of the BTV60. Instead, we use guard rings, sometimes known as Kao's rings (Ref.4) to passivate the chip. These are concentric rings (see photograph of chip and also Fig.2) spaced from the main junction such that, as the blocking bias increases, the depletion region punches through to the first (inner) ring before the planar breakdown voltage is reached.

Further increase of blocking bias increases the ring depletion region until the next ring is reached – and so on. Once punch-through is reached, the field intensity at the main junction edge is significantly reduced thanks to the enlarged radius of curvature.

The spacing between rings is critical to their operation. A spacing that's too narrow will lead to premature breakdown at the outer ring. One that's too wide will cause breakdown of the central region. For the BTV60, we've determined the precise spacing and the optimum number of rings by computer modelling techniques.

As an extra safety feature, we've terminated the chip with a channel stopper that prevents the depletion layer from reaching its edge.

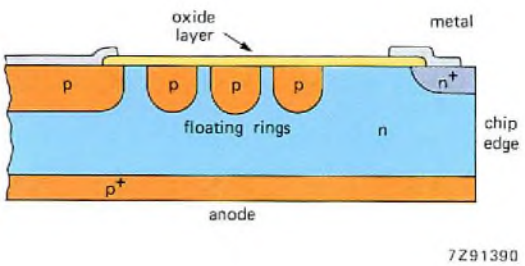

Fig.2 In the BTV60, guard rings are used to passivate the chip. These are concentric rings spaced from the main junction such that, as the blocking bias increases, the depletion region punches through to each ring in turn before the planar breakdown voltage is reached. As an extra safety feature, the chip is terminated with a channel stopper that prevents the depletion layer from reaching its edge

DRIVE CIRCUIT

Figure 3 shows a practical drive circuit for the BTV60. The gate signal is controlled by transistors TR_1, TR_2 in darlington configuration. With TR_1 and TR_2 turned off, gate-drive current passes from the positive supply rail to the GTO via transistor TR_3. With TR_1 and TR_2 turned on, TR_3 turns off and gate current passes to the negative supply rail via TR_2. A speed-up network (C_1, R_1) assures rapid turn-off of the darlington pair and hence rapid turn-on of the GTO.

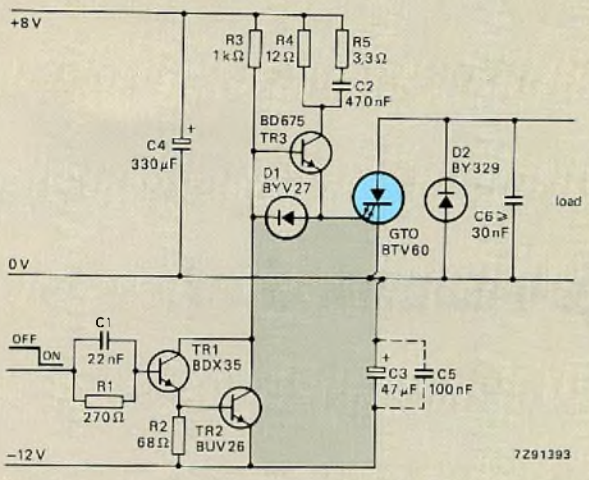

Fig.3 Practical drive circuitry for the BTV60. The turn-off loop (shaded) should have minimum inductance, and the high-frequency by-pass capacitor C_5 should (if used) be wired as close as possible to the electrolytic C_3

The maximum anode current I_{TC} that the GTO can switch depends on the peak current I_{GRM} extracted from the gate. This in turn depends on the internal gate-cathode resistance of the GTO, and on the series impedance of the turn-off loop – the most important contribution of which comes from the stray series inductance. So for maximum I_{TC}, the turn-off loop (shaded area in Fig.3) must be designed for minimum series inductance. In particular, high-frequency bypass capacitor C_5 should (if used) be wired as close as possible to the electrolytic capacitor C_3.

PERFORMANCE

Figure 4 shows the turn-off switching losses of the BTV60 as a function of anode current, with dV/dt as parameter.

Finally, Fig.5 compares the switching performance of the BTV60 with that of an equivalent first-generation GTO. The figure shows that although the maximum current both devices can switch is the same, i.e. around 100 A (this being primarily a function of crystal size), the second-generation device maintains this maximum current over a much greater dV/dt range (up to 300 V/μs).

Possibly of greater interest, however, is the new GTO's performance at higher dV/dt values (say around 500 V/μs) since in many applications, especially with inductive loads, a high dV/dt may be a major design parameter. Figure 5 shows that for a dV/dt of 500 V/μs, the second-generation BTV60 can still switch around 90 A, more than 3 times that of the first-generation device.

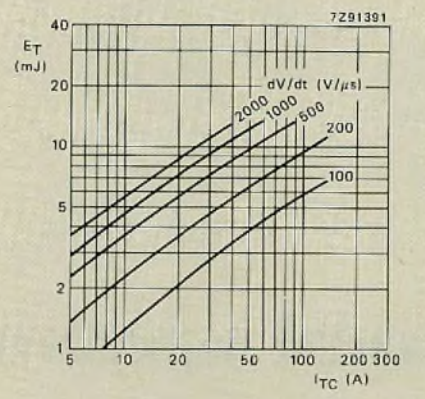

Fig.4 Turn-off losses E_T versus controllable anode current I_{TC} for the BTV60 with dV/dt as parameter. (Junction temperature 120 °C, reverse gate bias 10 V, on-state gate current 0,5 A)

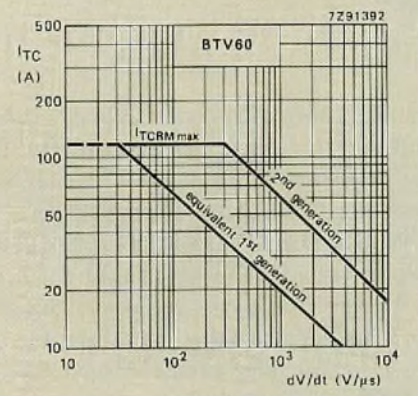

Fig.5 Switching performance of the BTV60 (with an inductive load) compared with that of an equivalent first-generation GTO. The figure shows the repetitive-peak-current I_{TCRM} that the devices can switch as a function of re-applied dV/dt. (Junction temperature 120 °C, reverse gate bias 10 V). The maximum value of this current is limited more by crystal size and by the current the bonding wires can handle than by the cathode structure

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Thermal aspects of flange-mounted r.f. power transistors

J. G. A. SCHOLTEN

R.F. power transistors often operate under conditions of severe mismatch. This often increases collector dissipation and consequently junction temperature. Failure mechanisms in high power transistors (breakdown, degradation, electromigration, thermal fatigue) are highly temperature dependent, so proper attention must be paid to their thermal conditions. However, it is an area where calculations are difficult and misunderstandings abound; this article is intended to clear up some of the misunderstandings and correct a number of misconceptions.

Practical points:

- The central area of the flange directly under the crystal contributes much less to heat transfer than has hitherto been thought;it is the area under and around the mounting bolt heads that conducts the bulk of the heat away.
- Although lapping the contacting surfaces of both heatsink and flange does improve thermal conductivity, the improvement is less than if a very thin layer of heatsink compound is used.
- Both of the commonly used bolts (M3 and UNC4-40) provide sufficient pressure when torqued to between 0,6 and 0,75 Nm. Using higher torques with a view to improving thermal contact resistance is counterproductive. Thermal contact resistance is more likely to increase.
- Except in the case of the UNC4-40 bolt, the maximum pressures encountered under these conditions do not cause excessive plastic deformation of the underside of the flange, and the minimum is sufficient to provide good thermal contact throughout life.

THERMAL MODELS

Many thermal models have been proposed in efforts to provide an analytical base from which to calculate the thermal behaviour of operating transistors. Because of the number of assumptions that have to be made, none survive comparison with actual measurements. Particularly with regard to hot-spotting and thermal contact resistance, theory and practice often differ by a factor of three.

The most dangerous assumption is probably that the chip surface temperature can be averaged and, therefore, that a uniform heat flux exists on the surface of the silicon chip. Although a large number of small base areas *are* distributed over the chip surface in order to promote even heat distribution, this assumption assigns too low a temperature to certain critical points on the chip surface. Because the hottest point presents the highest reliability risk, averaging leads to this risk being underestimated.

The situation is made clearer if we consider the power dissipation per unit area and the temperature gradients in and near the crystal of a high power transmitting transistor. In the crystal itself, in the base area a few micrometres under the emitter fingers the dissipation is about 500 W/mm^2 with a temperature gradient of about 5000 K/mm; in the BeO disc, about 5 W/mm^2 with a gradient of 25 K/mm; and in the flange, 2 W/mm^2 with a gradient of 5 K/mm. Efficient heat distribution is, therefore, essential if junction temperature is to be held below 200 °C.

Other assumptions that undermine the validity of current thermal models are: that heat distribution is uniform; and that the base of the transistor flange and the heatsink surface are isothermic.

Figures 1 to 6 show known models. These illustrate the difficulties of calculating thermal resistance when boundary conditions have to be assumed. It is clear that the influence of the finite thermal resistance of the heatsink is great, as is that of the mounting base. The most important result is that for a thick heatsink the contact area formed by the annulus between 0,8r and r largely determines the thermal resistance of the whole contact area. These results are confirmed by measurements (described in the Appendix) that show that removing metal from the flange centre barely affects the thermal resistance of the contact area. Other reasons for the bolt head area being important are discussed below.

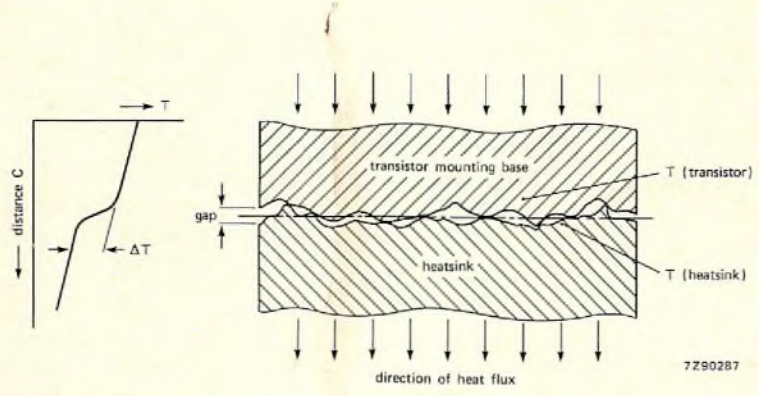


Fig.1 This rather simplified case is often mentioned in the literature to describe contact surface thermal resistance. It assumes a constant heat flux normal to the contact area. Thermal resistances can be calculated using the average gap between the surfaces (caused by micro-asperities, see *Thermal contact)* which is filled with air or heatsink compound. Ref. 1, 2

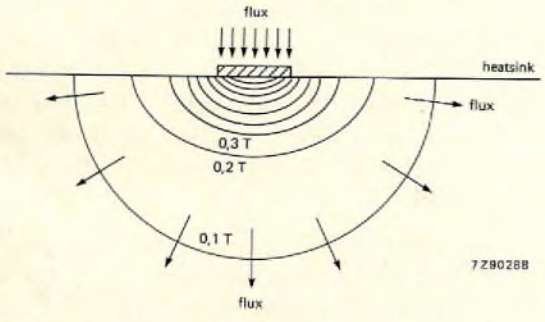


Fig.2 This theoretical approach assumes an infinite heatsink with a uniform constant heat flux normal to a circular contact area. The temperature distribution on the heatsink surface requires the solution of complete elliptic integrals. The results are plotted in Fig.3. The most important facts emerging from this approach are: the average angle of the heat flux in the heatsink is >60° to the direction of the assumed transistor heat flux; and that the thermal resistance of the heatsink is inversely proportional to the radius of the heat flux and *not* to the surface area of the heat flux. Ref.3, 4

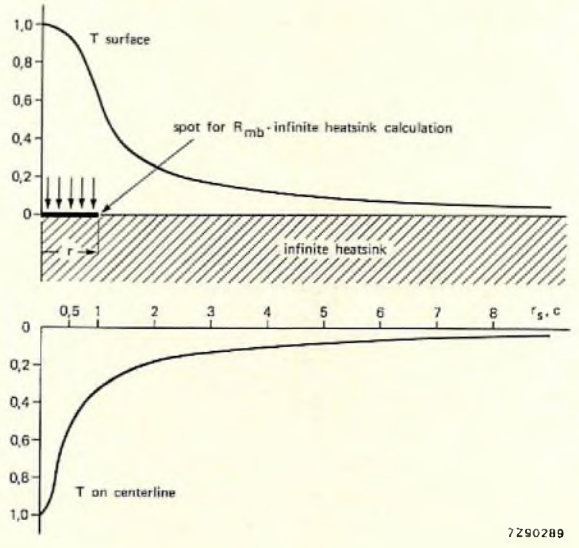


Fig.3 Temperature of (a) the heatsink surface and (b) the centre of the body of the heatsink normal to the surface, as calculated using the approach of Fig.2

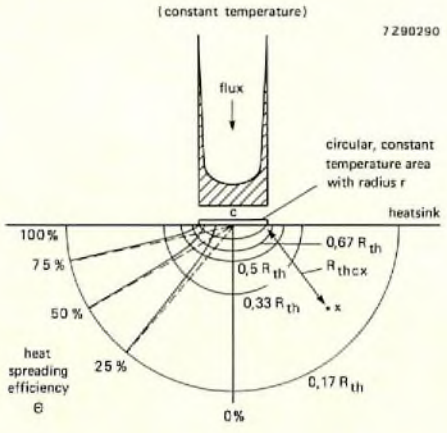


Fig.4 This approach assumes a constant mounting base temperature and a low contact thermal resistance. This also requires the solution of complete elliptic integrals, but with a simpler result for calculating the temperature at a distance x from the centre; Ref.5, 6. For large distances the results are the same as for Fig.2. For an elliptic contact area (or, with slight error, for a rectangular flange) a form factor can be applied. The main difference with Fig.2 is in the flux, which has infinite intensity at the edge of the contact area. The most important result of this is that 50% of the total heat flux passes through an annulus of r — 0,9r; i.e., if a circle of 0,9r is removed from the contact area, thermal resistance is only doubled

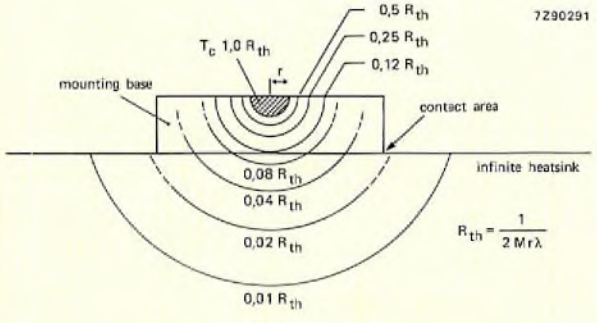


Fig.5 The fourth approach is to assume a small hemispherical heat source of constant temperature half buried in the upper surface of the flange. If flange and heatsink are of the same material and the thermal contact resistance is low, the isothermals will be hemispheres passing through flange and heatsink and temperature will decrease with the square of the distance

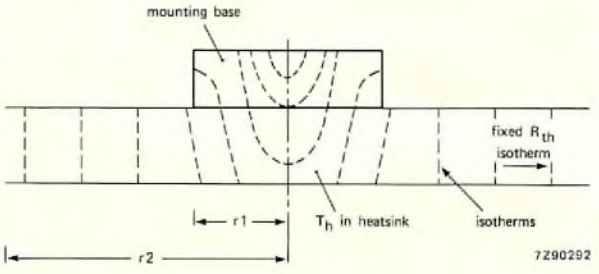


Fig.6 If, in the case of Fig.5 we assume the heatsink to be thin (thickness <r), the thermal resistance will be infinite if the heatsink is not connected to a point of fixed thermal resistance such as fins or water jacket. If, at a distance r_2, such a (circular) connection does exist, the isotherms will be concentric circles on the surface of the heatsink and, if $r_2 \approx 2r_1$, heat flux will decrease linearly with distance. The R_{th} of the transistor will be higher because the heat spreads differently

SURFACE CONDITIONS

Because of irregularities in their surfaces two apparently flat objects will probably contact over less than a thousandth of their common surface area when pressed together. Three types of surface irregularity are of interest to us here:

- Waviness, i.e., deviation from flatness (see Fig.7(a)). This includes the plastic deformation of the transistor flange caused by the differing coefficients of expansion of BeO and Cu. After the BeO disc has been attached the two materials contract at different rates, setting up stresses that deform the flange, making it slightly concave. Although the flange is subsequently ground, residual stresses cause the copper to creep and the flange is therefore very slightly concave (typically 7 μm) when delivered (see Fig.15).
- Grooving, a repetitive form of deformation that is usually the result of milling, turning, grinding, etc. This is rarely a problem in transmitting transistor flanges but may occur in heatsinks, especially those of poor quality. (See Fig.7(b)).
- Non-repetitive micro-asperities, a random phenomenon that is reduced but not entirely removed by lapping or polishing. It is characteristic of all normal surfaces. (Fig.7(c)).

Surface irregularities of the last two types are usually expressed in terms of average roughness (r_a), as shown in Fig.7(c). Instead of arithmetic average, the r.m.s. value (a slightly higher value) is often used in the USA. Although most suited to defining the smoothness of sliding surfaces, r_a does not indicate the intimacy of contact between two

surfaces, which is what concerns us here. A more useful way of expressing roughness for our purposes, one rarely used for transistor flanges, would be that of DIN 4762, i.e., the percent bearing surface (t_p) at a given depth (c). Figure 8 compares r_a and t_p for a selection of surface profiles.

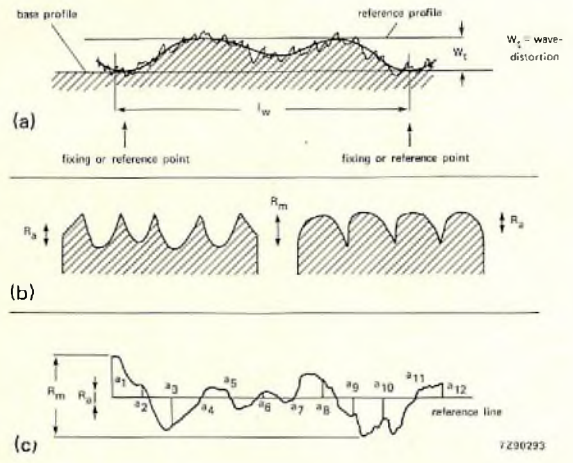


Fig.7 Three types of surface distortion of interest in thermal contacts. That of (a) can be cured by lapping or polishing whereas those of (b) and (c) can only be reduced

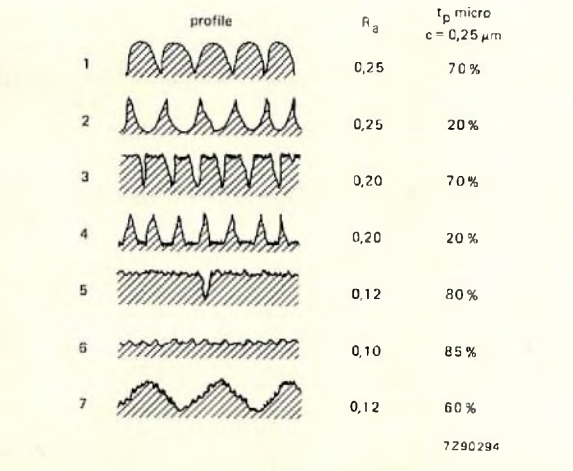


Fig.8 Although R_a is a good indication of the frictional behaviour of mating surfaces, it is less effective in defining the intimacy of contact as is needed for our purposes. A better indication is given by percent bearing surface, t_p, at a given depth, c, in this case 0,25 μm

THERMAL CONTACT

From the foregoing it will be seen the contact conductance between two surfaces is the sum of the conductances of a very large number of metallic contacts in parallel with a similar number of air gaps (perhaps filled with heatsink compound). $R_{th\,mb\text{-}hs} = 1/h_t$ where $h_t = h_m + h_f$: h_m and h_f being the conductance of the metallic paths and of the air (or heatsink compound) paths, respectively.

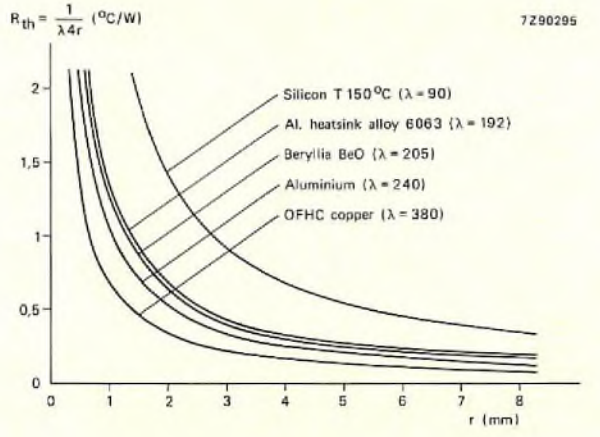


Fig.9 Thermal resistance of various materials as a function of distance measured from the edge of a circular heat flux into an infinite heatsink. The thermal resistance in the centre of the heat flux is higher by a factor of 1,57

Of course, the contacting surfaces of heatsink and transistor flange will not remain unaffected by the pressure when the two are clamped together. Where the pressure is greatest the asperities will, naturally, be to some extent crushed, thus increasing the area of metallic contact at these points. It is worth examining how the applied pressure is distributed.

PRESSURE DISTRIBUTION

Because the transistor flange is flexible the pressure imparted by the clamping bolts is not distributed uniformly over it. Accurate calculation of the actual pressure distribution is impeded by a number of difficulties:

- the flange is not perfectly flat
- its shape is irregular
- the modulus of elasticity is higher in the centre of the flange than elsewhere.

In fact about 90% of the clamping force is exerted in an area twice that of the screw head (or washer, if used). Away from this area the force falls rapidly, its approximate value being given by:

$$F = F_i \left(\frac{Ph^3}{L^3} + \frac{K}{L^3} \right)$$

here:

- F = pressure
- P = the product of modulus of elastically, mass moment of inertia, shape factor and roughness factor
- K = waviness factor (which may be negative)
- h = height of flange
- L = distance from fixing point
- F_i = force under bolt head.

Because the denominator includes the third power of the distance, pressure falls off rapidly with distance from the fixing point and may even become negative. This is confirmed by the fact that the centre of a transistor flange lifts away from the heatsink when too high a torque is applied to the bolts. Figure 10 illustrates how pressure is distributed over the flange. In the following we shall see what actual forces are involved.

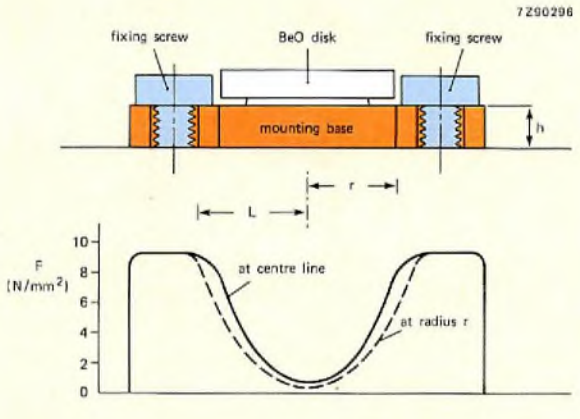


Fig.10 Pressure distribution over the mounting surface of an ideal (flat) flange. The highest pressure occurs round the bolt heads

FORCE UNDER THE BOLT HEAD

The equation for clamping force would be simple were it not for the effects of friction. Friction enters in two ways: friction between bolt head and flange, and friction between the external and internal screw threads. The coefficient of friction depends on the two materials in contact and the degree of lubrication. Table 1 shows the coefficient of friction for the materials of interest, the bolts being usually of steel and the heatsink either of copper or aluminium. Sometimes a steel nut is used.

TABLE 1

material	coefficient of friction			
	unlubricated		lubricated	
	min.	max.	min.	max.
steel – copper	0,5	0,8	0,2	0,6
steel – aluminium	0,5	1,3	0,2	0,6
steel – steel	0,3	0,7	0,1	0,2

Note: At higher contact pressures the coefficient of friction increases due to atomic adhesion and gouging.

The relation between torque and the force under the bolt head is:

$$F_i = \frac{2T}{D_m f_b + D_p \frac{\tan (B + \phi)}{\cos \alpha}}$$

where:

- T = applied torque (0,6 to 0,75 newton metres)
- D_m = mean bearing diameter of bolt (M3 = 4,2 mm; UNC4-40 = 3,9 mm)
- D_p = pitch diameter of thread (M3 = 2,675 mm; UNC4-40 = 2,433 mm)
- B = helix angle of thread (M3 = 3,41°; UNC4-40 = 4,77°)
- f_b = coefficient of friction between bolt head and flange (0,5 – 0,8)
- ϕ = friction angle ($\phi = \tan^{-1} f_t$, where f_t, the coefficient of friction between the screw threads, is 0,3 to 1,3)
- α = half thread profile (30° for both threads).

Table 2 shows the maximum and minimum figures for the two bolts in question and the three materials into which the bolts are screwed. In all cases friction between bolt head and flange is assumed to be steel-to-copper. The minimum values were calculated using minimum torque and maximum coefficient of friction. Estimating probable maximum values is less straightforward. Friction will increase, even from the minimum value, as pressure increases. The chance of some lubricant (in the form of heatsink compound) being present is quite high, even if care is taken. On the basis of experience, we have taken a median value for coefficient of friction to arrive at the maximum force values in Table 2.

TABLE 2

material into which bolt is screwed	force under bolt head (newtons) M3 min.	M3 max.	UNC4-40 min.	UNC4-40 max.
copper	308	385	322	403
aluminium	308	385	322	403
steel	369	461	394	493

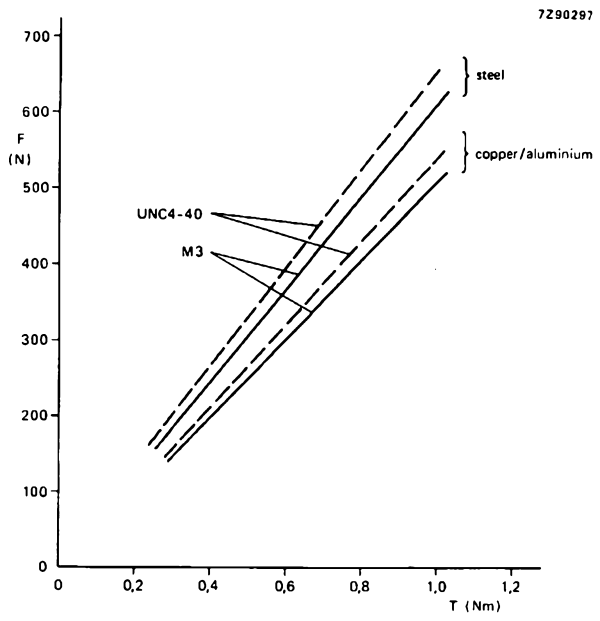


Fig.11 Force under the bolt head as a function of applied torque. Note that the UNC4-40 bolt gives a slightly higher force than the M3

These results are plotted in Fig.11. The curves are extended to higher torque values to take account of torquing error. Depending on the type of tool used and the speed of operation, the bolts may be over-torqued by a factor of up to 1,6.

It is clear that the UNC4-40 bolt gives a somewhat higher force under the head than the M3. The difference in pressure is even greater because the UNC4-40 bolt head is smaller than the M3.

It should be borne in mind that the relation and curves are only valid up to certain limits. At some point the bolt head starts biting into the material under it and the threads start biting into each other. At the limit either the threads strip or the bolt shears. So, instead of being straight lines the curves will flatten out.

MOUNTING PRESSURE

We can derive the actual mounting pressure from the contact area between bolt head and flange.

Bearing area
= bolt head area – flange hole area

Minimum bearing area
= minimum head area – maximum hole area

Maximum bearing area
= maximum head area – minimum hole area.

The lowest and highest pressures are then obtained by combining the above results with the force values from Table 2.

$$\text{Minimum pressure} = \frac{\text{minimum force}}{\text{maximum area}}$$

$$\text{Maximum pressure} = \frac{\text{maximum force}}{\text{minimum area}}$$

DEFORMATION

Metals, particularly copper which is highly ductile, deform when loaded. Up to a specific stress this deformation is elastic, i.e., remove the load and the metal returns to its original shape. Above this point permanent deformation occurs. Compared with metals such as steel, the elastic limit of copper is quite low: depending on its production history, plastic deformation can begin at stresses of about 20 N/mm^2.

The production history of the flange copper is not published. However it is reasonable to assume that it is cold rolled with some consequent work hardening. Brazing on the BeO disc at a temperature of about 800 °C will cause annealing. Under the disc, however, the differing expansion coefficients of copper and beryllium (18 compared with 5,8) will cause stresses. The copper, being the more ductile of the two, will deform with consequent work hardening around the centre. Machining flat will also cause some work hardening. The result is that the material properties of the flange lie somewhere between those of cold drawn copper and fully annealed copper.

Figure 12 shows the probable stress/strain curve for these conditions. Inserting the stress values obtained in Table 3, we get the expected degree of deformation. The highest stresses occurring with M3 bolts (±35 N/mm^2) are just over the border of elastic deformation (strain not exceeding 0,05%). Even with a factor of 1,6 to allow for over-torquing we are still within safe limits, below, say, 0,08%. With UNC4-40 the stresses are much higher than this and, if an allowance of 1,6 is made for torquing error, strains of up to 1,0% (and not less than 0,04%) are likely. Where possible this should be avoided, if necessary by fitting a 5,5 mm washer under the head.

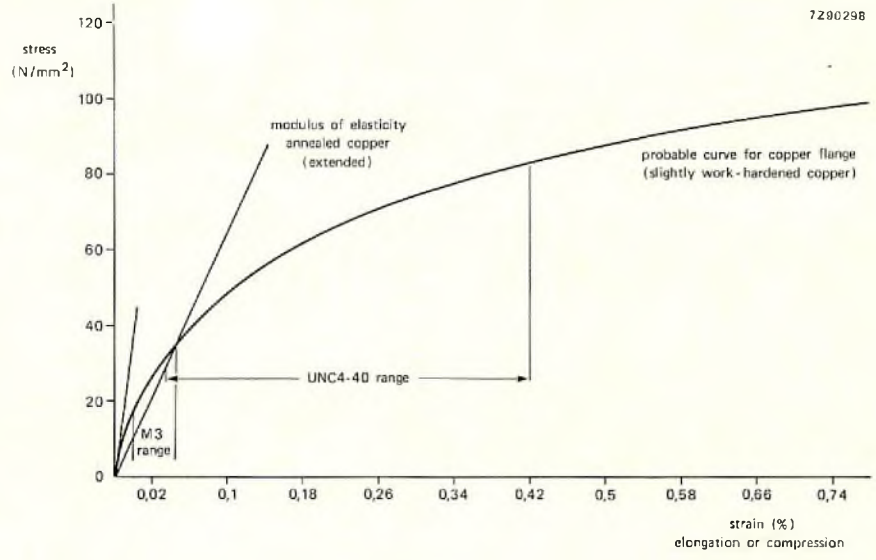


Fig.12 Stress/strain curve for the copper flange. The smaller head diameter of the UNC4-40 bolt leads to much higher strains than with the M3. When maximum torque is applied a washer will reduce strain to an acceptable level

TABLE 3
Pressure in newtons/mm² *

material	M3		UNC4-40	
	min.	max.	min.	max.
copper	18	29	30	68
aluminium	18	29	30	68
steel	22	35	36	83

* 1 newton/mm² = 1 MPa.

EFFECTS OF DEFORMATION

Because the copper flange is compressed between bolt head and heatsink, displaced metal can only escape radially. Some will escape toward the centre, but most will flow outward. Along the axis between the bolts two stresses will be operating from opposite directions. The metal can only escape by lifting the centre of the transistor flange away from the heatsink, as shown in Fig.13.

Figure 14 shows the results of tests in which a flange was mounted by high tensile steel M3 bolts to a thick tool-steel heatsink with polished surface. The M3 bolts were screwed into steel nuts, a friction coefficient of about 0,3 being applicable. The torque on the bolts was increased in steps of 0,2 Nm from an initial 0,4 Nm. After each step the flatness was measured along the dotted line. The enlarged curve for a torque of 0,8 Nm shows that the centre of the flange has lifted by 7 μm. This lifting will increase contact

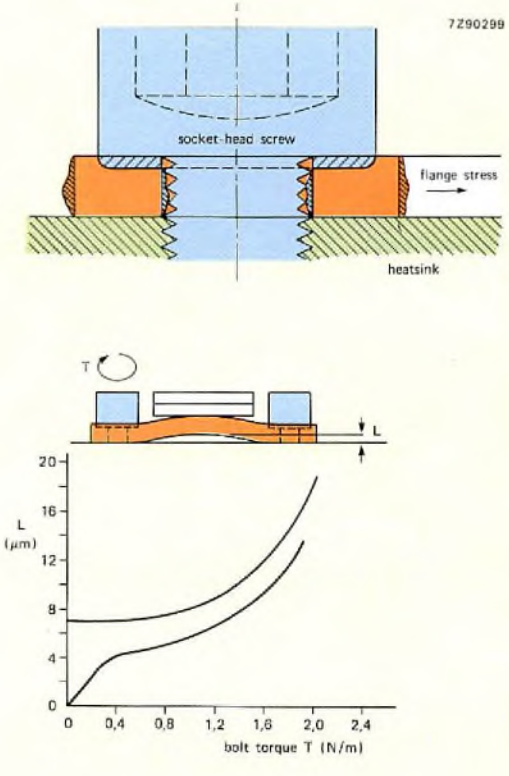


Fig.13 Above, plastic deformation in the flange. Below, how the centre of the flange tends to lift under excessive pressure

thermal resistance and as, in any case, normal heatsinks are not perfectly flat, it is clear that torques of 0,75 Nm should not be exceeded. It is worth noting that even though the tests extended to torques as high as 2,0 Nm, in no case was a beryllium oxide disc damaged.

Among the conclusions to be drawn from the above are that high torques do not improve contact thermal conductivity and that once a transistor has been mounted it should never be removed to another heatsink. For one thing it has adapted to the footprint of the heatsink it was first mounted on, and further, because of tolerances, the pitch of the mounting hole threads will differ.

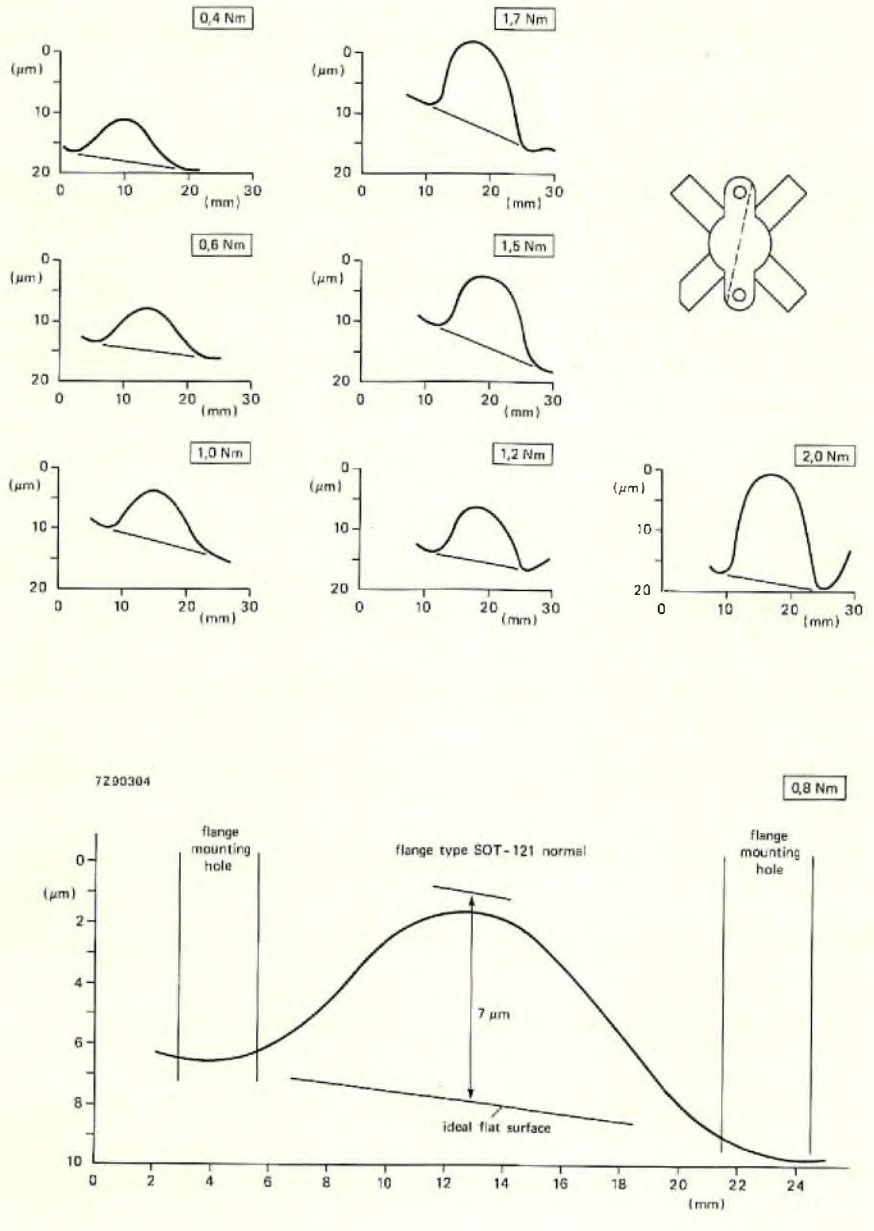


Fig.14 Measured deformation in an unlapped flange when steel M3 bolts are torqued in steps to 2,0 Nm. The curves have been smoothed to remove the effects of micro-asperities. The enlarged curve is for a torque of 0,8 Nm and shows a deformation of 7 μm at the centre

CREEP

The deformation just described occurs immediately the stress is applied; under continued stress there is a further slow deformation that tends to reduce the applied stress. This slow deformation is known as creep.

Creep causes plastic strain to increase with time and, because the strain in a mounted transistor flange is constant, elastic strain decreases. Stress decreases as the elastic strain decreases. Figure 15 shows how stress reduces over time. It is, however, no more than an indication because relaxation speed is highly dependent on temperature, cyclic strain, work hardening and recrystallization. Under normal operating conditions temperature cycling will cause work hardening which will promote resistance to stress relaxation. On the other hand the cyclic strain imposed by temperature variations and the (more or less) elevated temperature of the flange during operation will tend to increase stress relaxation.

Our experience in temperature cycling (thermal fatigue) tests shows that relaxation reaches 30% in the first 100 hr and 50% in the first thousand. These tests are, of course, severer than normal operating conditions.

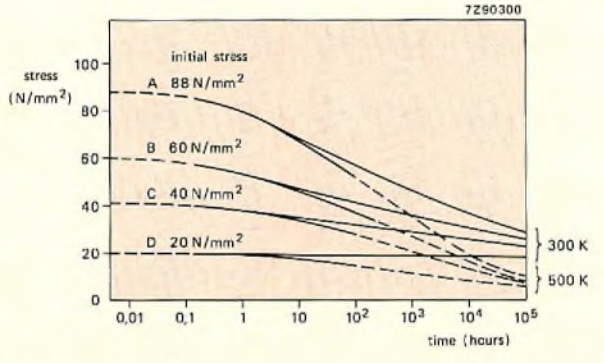


Fig.15 Typical creep curves in oxygen-free high conductivity copper. These are representative for the transistor flange copper but can only be considered as indicative because creep is also influenced by cyclic strains (temperature) such as occur in an operating transistor

APPENDIX

Cavity test

The transistors were mounted on a water-cooled copper rod (30 mm dia.), the centre of the upper surface of which was maintained at 70 °C. The upper surface was lapped to a flatness of $<3\,\mu m$ and a roughness $r_a < 0{,}4\,\mu m$. The flange of one transistor was lapped to a flatness of $<1\,\mu m$ and a roughness $r_a < 0{,}2\,\mu m$. The other transistor was not lapped and its flatness was $6\,\mu m$ and its roughness $r_a < 0{,}8\,\mu m$. Dow Corning DC340 heatsink compound was used, except in one case where it was omitted to prove its efficacy. The transistors were adjusted to dissipate 150 W.

A circular cavity 1 mm deep was milled in the centre of the base of the flange. Initially it was 4 mm diameter and was increased in steps of 1 mm, burrs being removed at every stage. The percentage non-contacting surface area as a function of cavity diameter is shown in Fig.16. The amount of metal removed (1 mm depth) was insufficient to affect the bulk thermal properties of the flange.

Crystal temperatures were measured with a specially calibrated infra-red microscope. Heatsink and flange temperatures were measured with thermocouples placed as in Fig.17. Thermocouple 1 was used as monitor and maintained at 70 °C.

Crystal temperatures were plotted, a typical scan being shown in Fig.18 (left), and average peak temperatures entered on thermal maps as in Fig.18 (right). Finally, curves were plotted of peak average temperatures at given points on the crystal against cavity size. The highest and lowest curves are those shown in Fig.19. Intervening curves have been omitted for clarity.

It will be seen that at a cavity size of 7 mm, junction temperature has risen by less than 10 K and that it is not until the cavity is 9 mm or more that maximum junction temperature is exceeded. Clearly, lapping the transistor flange does reduce $R_{th\ mb\text{-}hs}$, but using heatsink compound has an even greater effect.

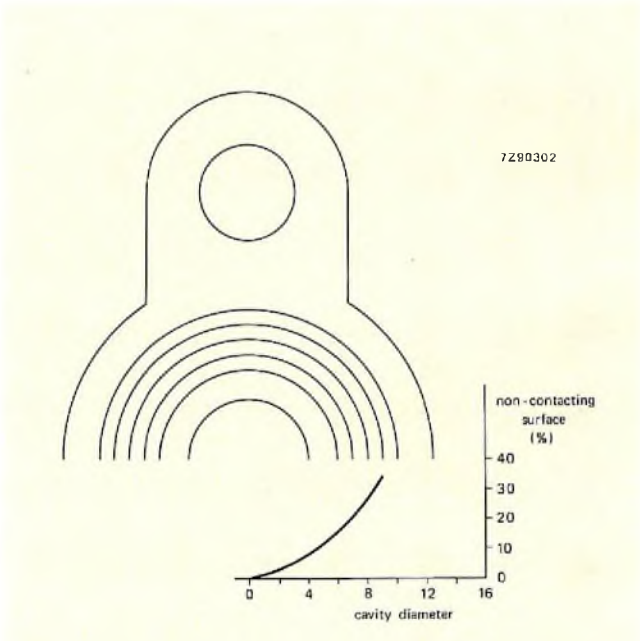


Fig.16 Contact surface area as a function of cavity size

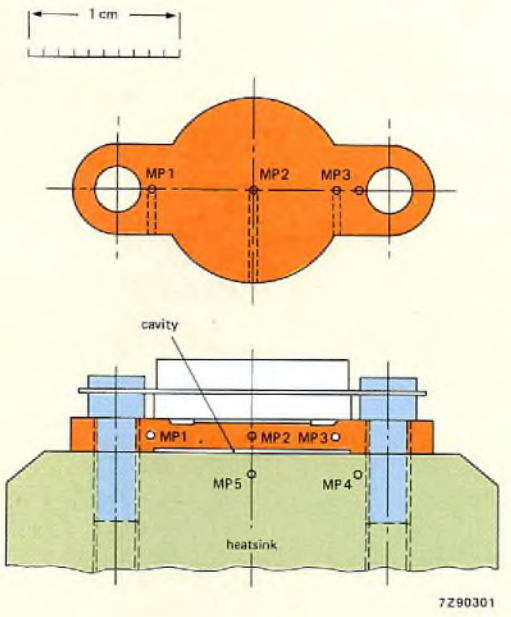


Fig.17 Placement of thermocouples for monitoring heatsink temperature

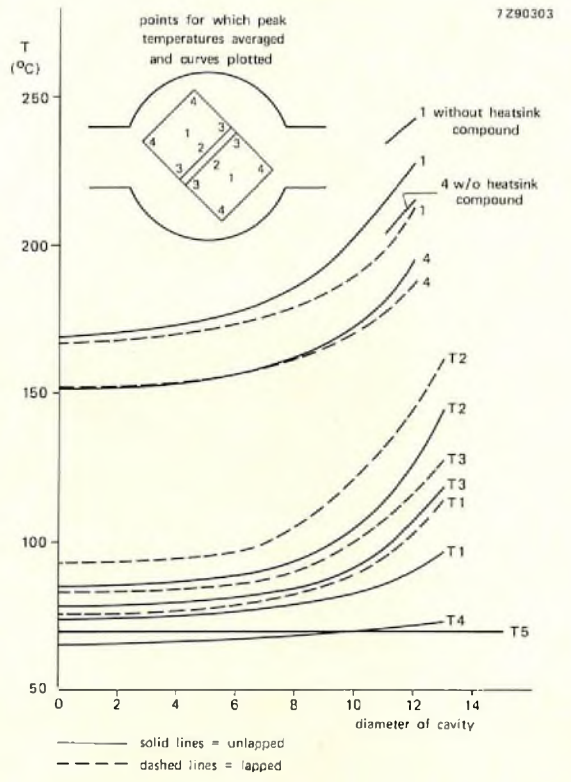
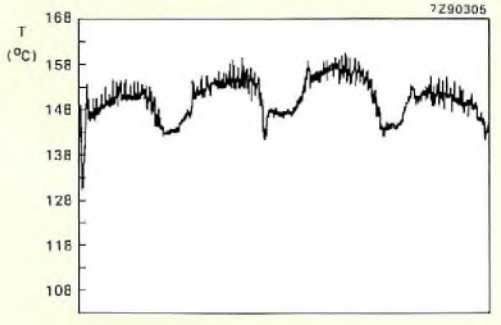


Fig.19 Curves of junction temperature against cavity size for a lapped transistor (solid line) and an unlapped transistor (broken line). It is not until the cavity is about 7 mm in diameter that junction temperature rises more than about 10 K



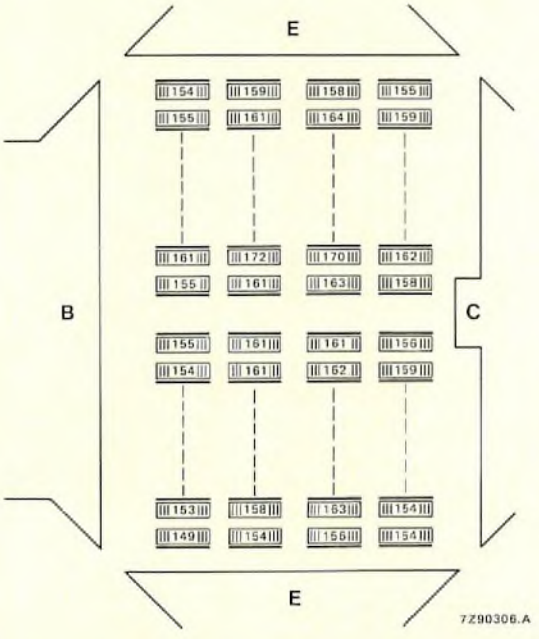


Fig.18 Junction temperature measurements. Left, a typical scan with the infrared microscope and right, a partial thermal map of average peak temperatures

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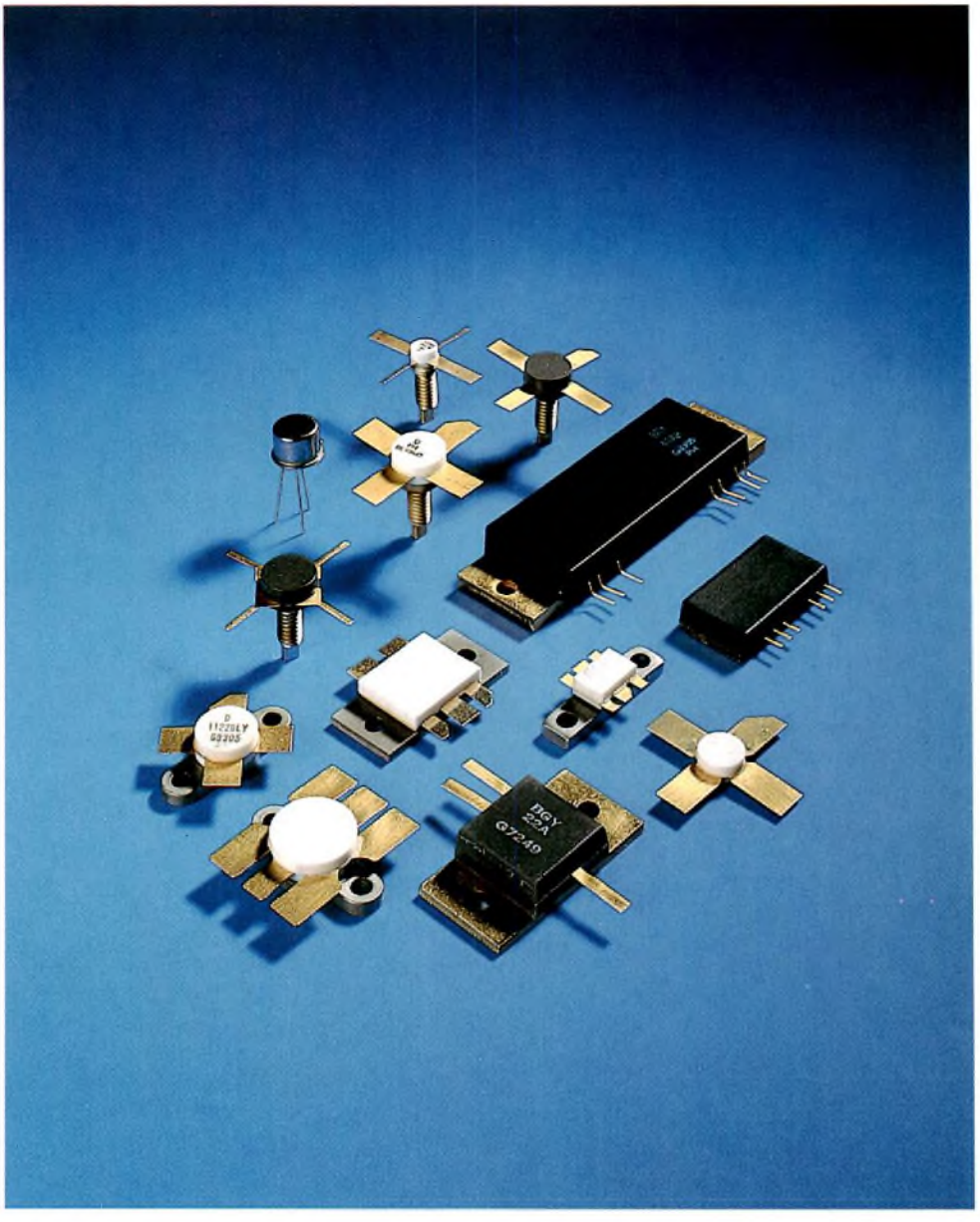


This article originally appeared in the February issue of Microwaves & RF.

New stereo decoder IC suits all classes of radio

W. H. A. VAN DOOREMOLEN

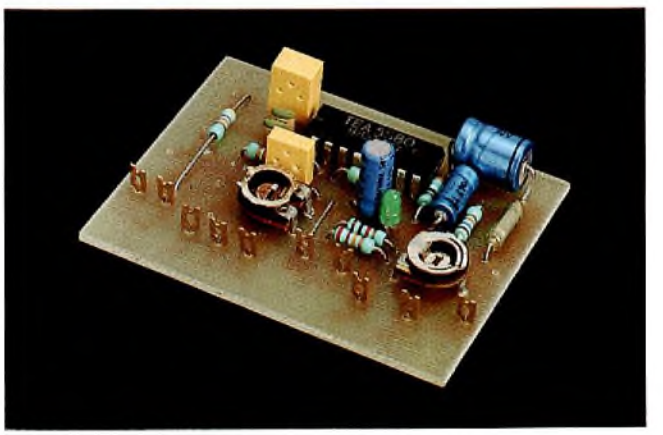
Our radio/audio integrated circuits are renowned for their economy, high performance, quality and replacement value. But these attributes alone are not enough. We know that radio manufacturers need ICs that are also flexible enough in application to fit into standardized designs that can be easily adapted to suit portable radios, radio/recorders, mains-powered radios and car radios. This is why we developed our versatile integrated time-division multiplex PLL stereo decoder TEA5580. Naturally, it performs all the basic stereo decoding functions and needs only a very simple peripheral circuit of a few passive components. Unlike other decoders however, it also offers a host of additional features, requires no adjustment of channel separation (a boon in economy sets), and operates from a wide range of supply voltages.

The basic stereo decoding functions performed by the TEA5580 are:

- provision of a pilot-tone reference frequency and a regenerated subcarrier derived from a PLL comprising a voltage-controller oscillator (VCO), frequency dividers and a pilot phase detector
- automatic mono/stereo switching and stereo indication using a pilot-tone presence detector and a LED indicator driver
- synchronous demodulation of the subcarrier L−R information
- matrixing of the demodulated main and subchannel information to provide L and R output signals.

Additional features provided by the TEA5580 are:

- adjustable degree of pilot-tone cancellation, and adjustable level for mono/stereo switching
- smooth d.c. control of channel separation which can be made dependent on the strength of the received signal, and therefore on the signal-to-noise ratio
- internal suppression of adjacent channel interference due to the modulation frequencies of adjacent channels mixing with the 3rd harmonic of the 38 kHz regenerated subcarrier
- internal suppression of intermodulation products due to 57 kHz traffic information service signals
- optimal channel separation by compensating a droop in the frequency response at 38 kHz due to the typical roll-off of the frequency response of the preceding i.f. amplifier/f.m. detector
- output levels adjustable up to 900 mV r.m.s.



This versatile new stereo decoder can be used with the same simple peripheral circuit in every conceivable type of radio from a battery-powered portable to a high-performance tuner or a car radio

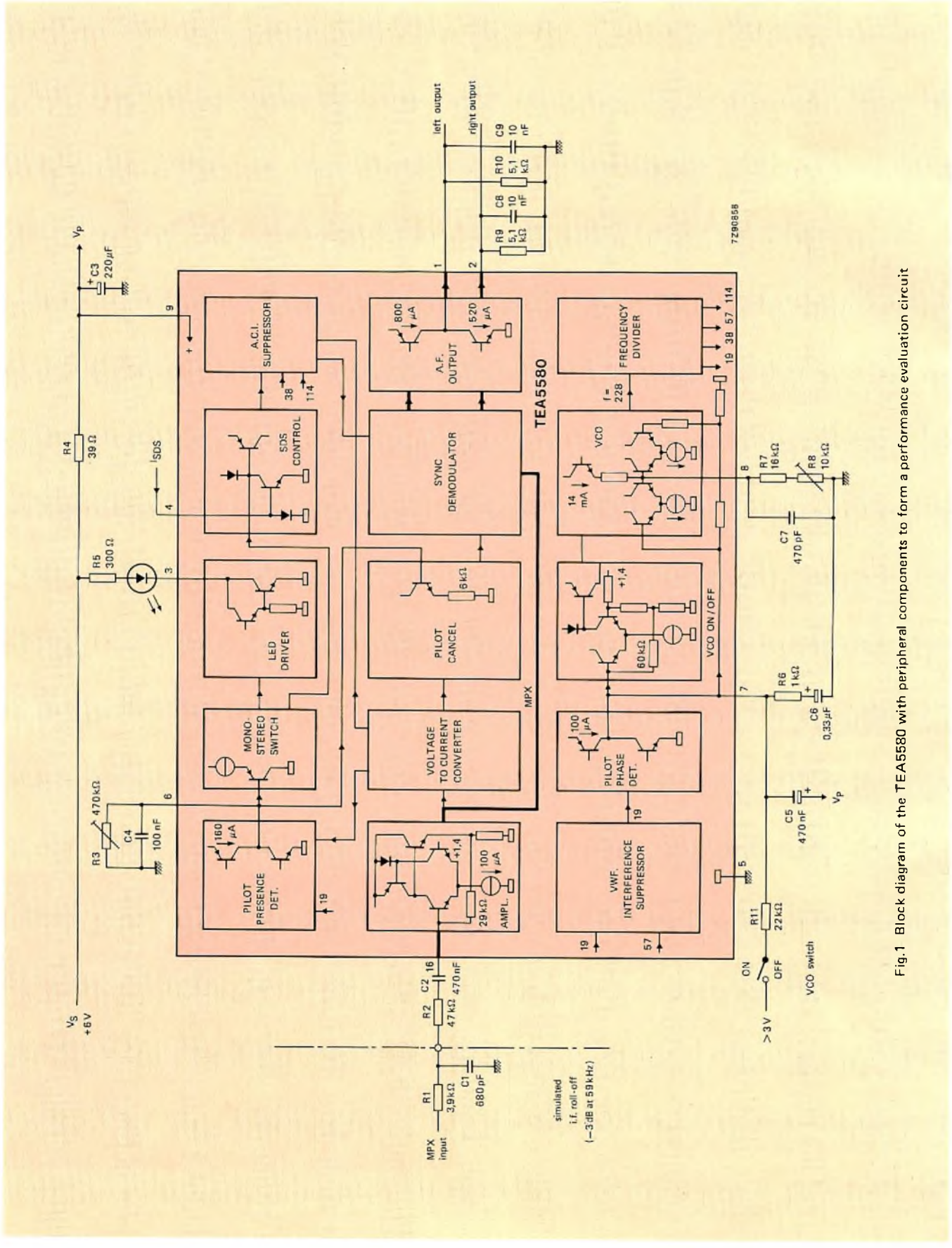


Fig.1 Block diagram of the TEA5580 with peripheral components to form a performance evaluation circuit

CIRCUIT DESCRIPTION

This description is based on the block diagram of the TEA5580 which is shown with peripheral components to form a performance evaluation circuit in Fig.1.

Supply voltage stabilizer

An internal supply voltage stabilizer allows the decoder to operate from supply voltages between 3,6 V and 16 V. The typical total quiescent supply current is 10 mA from a 6 V supply.

Input circuits

The composite demodulated stereo multiplex (MPX) input signal at pin 16 is internally amplified by an inverting operational-amplifier. The overall gain of the circuit is determined by the ratio of the value of the internal feedback resistor of the op-amp to the value of the external input resistance, and by the value of output load resistors R_9 and R_{10}. The overall gain can be set between 0 dB and 20 dB by selecting the value of R_2 in series with the input at pin 16. In the performance evaluation circuit of Fig.1, with $R_2 = 47\ \Omega$ and $R_9 = R_{10} = 5{,}1\ \Omega$, the overall gain is unity. Low-pass filter R_1/C_1 simulates the frequency response of an i.f. amplifier/f.m. demodulator with a frequency response roll-off point (–3 dB) at 59 kHz. Attenuation of the sub-channel at 38 kHz due to this roll-off is internally compensated in the decoder matrix. In the event of frequency response roll-off at lower frequencies (for example, in car radios incorporating an interference suppression circuit like the TDA1001B), channel separation and audio fidelity can be maintained by adding high-frequency emphasis with a parallel RC network in series with the input at pin 16.

Phase-locked loop

In the PLL, the VCO frequency is set to 228 kHz by the external RC network at pin 8, and divided to provide 114 kHz for suppression of ACI (adjacent channel interference), 57 kHz for suppression of VWF (Verkehrs Warnfunk = 57 kHz West German traffic information service) intermodulation products, 38 kHz as a regenerated subcarrier, and 19 kHz as a pilot-tone reference frequency and for pilot-tone cancellation. The typical uncompensated temperature coefficient of the VCO is 400 ppm/K.

The 19 kHz output from the frequency divider passes, via the VWF suppressor, to one input of a pilot phase detector. The amplified MPX signal is fed to the other input. The d.c. output from the pilot phase detector at pin 7 is 1,7 V when the VCO frequency is correct (228 kHz), and varies with a slope of 2,5 mV/kHz for VCO frequency variations. This error signal is fed back as a tuning voltage for the VCO to maintain its frequency at precisely 228 kHz.

The external loop filter at pin 7 suppresses a.c. components at the PLL output and also influences the capture range of the loop. With $C_5 = 470$ nF, the capture range is 5% of the nominal frequency of the VCO. For car radios, which must operate over an extended temperature range, we recommend that the value of C_5 be reduced to 220 nF, thereby increasing the capture range of the loop to 8% of the nominal frequency of the VCO.

A d.c. level of greater than 3 V can be applied to pin 7, via a 22 kΩ resistor, so that the VCO on/off switch inhibits the VCO during a.m. reception in an a.m./f.m. radio.

VWF interference suppression

When a composite f.m. stereo signal incorporating VWF information is transmitted, there is a constant phase relationship between the 57 kHz VWF carrier and the 19 kHz stereo pilot-tone. In the stereo decoder however, this phase relationship may be altered due to phase shifting of the 57 kHz VWF carrier that occurs before the stereo decoder, and to small phase shifts in the decoder PLL. There is therefore a possibility of the third harmonic of the 19 kHz pilot-tone mixing with the 57 kHz VWF carrier and transferring the VWF modulation, via the VCO, to the regenerated 38 kHz subcarrier. This would cause crosstalk and intermodulation products at the stereo outputs of the decoder. To prevent this, the VWF suppressor eliminates the third harmonic of the 19 kHz reference frequency before it is compared with the stereo MPX signal in the pilot phase detector.

Pilot presence detection and mono/stereo switching

The amplified MPX signal and the 19 kHz reference frequency from the VCO dividers are applied to the inputs of a symmetrical quadrature demodulator acting as a pilot presence detector. When the PLL is locked, the d.c. output from the pilot presence detector activates the mono/stereo switch. As shown in Fig.2, the switching hysteresis is about 2 dB and the switching level is dependent on the voltage at

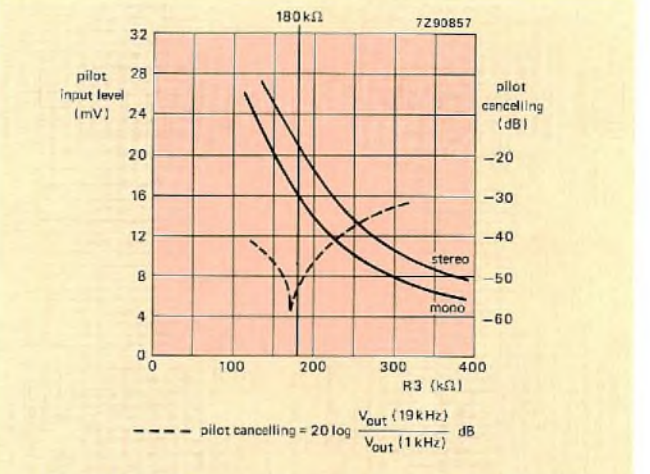


Fig.2 Mono/stereo switching level and degree of pilot-tone cancellation as functions of the value of R_3

pin 6 as set by the gain of the input amplifier and the adjustment of R_3. The resistor is set for optimum pilot-tone cancellation and may result in insufficient sensitivity for mono/stereo switching. This should not be remedied by re-adjusting R_3 but by increasing the overall gain of the circuit by reducing the value of input resistor R_2 as explained earlier.

The mono/stereo switch has two functions during stereo reception. One function is to activate the LED driver which can sink up to 50 mA from the supply via a LED stereo indicator connected to an open collector at pin 3; the other function is to activate the Signal Dependent Stereo (SDS) control so that the 38 kHz regenerated subcarrier from the VCO is passed, via the ACI suppressor, to the synchronous demodulator/matrix which decodes the stereo L and R signals.

SDS control

The transition from mono to stereo operation (stereo channel separation) can be smoothly controlled by varying the amplitude of the regenerated 38 kHz subcarrier applied to the synchronous demodulator. This is done by varying the direct current flow into the SDS circuit via pin 4 within the range 10 μA to 200 μA as shown in Fig.3. If this current is made dependent on field strength (by deriving it from a level detector in an f.m. i.f. amplifier/detector such as the TEA5570), a sudden increase of about 20 dB in the noise level at the instant of mono/stereo switching can be avoided by having minimum stereo channel separation when the signal-to-noise ratio reaches a certain threshold (46 dB for example), and then progressively increasing it with increasing field strength. The SDS function can be inhibited (forced mono) by connecting to a resistor between pin 4 and the supply voltage ($I_4 \approx 400\,\mu A$).

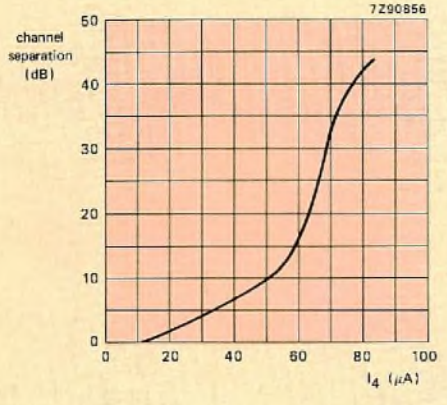


Fig.3 Channel separation as a function of the current into pin 4

ACI suppression

The main cause of adjacent channel interference is mixing of the third harmonic of the 38 kHz regenerated subcarrier (114 kHz) with the modulation frequencies of adjacent channels spaced at 100 kHz from the required channel. To prevent this interference, the third harmonic is eliminated from the 38 kHz regenerated subcarrier. To do this, a 114 kHz output from the VCO frequency divider switches a current (I) in the ACI suppressor. This is then added to a current (3I) which is switched by the 38 kHz regenerated subcarrier from the VCO. If it is also necessary to eliminate interference caused by the fifth harmonic of the regenerated subcarrier mixing with adjacent channels spaced at 200 kHz or 300 kHz, an RC low-pass filter can be used at the MPX input. For example, if R_2 is reduced to 39 Ω and preceded by an RC low-pass filter (8,2 kΩ/330 pF), the overall gain of the circuit will remain unchanged and the attenuation at 186 kHz will be increased from 68 dB to 78 dB.

Pilot-tone cancellation

The pilot cancel circuit is activated by the pilot presence detector during the reception of stereo broadcasts. It eliminates the 19 kHz pilot-tone before the MPX signal is demodulated. As shown in Fig.2, the degree of pilot-tone cancellation is controlled by external variable resistor R_3. The setting of R_3 also affects the sensitivity of the mono/stereo switching but, if it is adjusted for optimum pilot-tone cancellation, the required mono/stereo switching sensitivity can be attained by adjusting the overall gain of the circuit (by changing the value of input resistor R_2 as previously described).

Synchronous demodulation and matrixing

In the synchronous demodulator, the L−R information from the sub-channel is recovered by a.m. demodulation in which the MPX signal (with suppressed pilot-tone) is switched at the regenerated subcarrier frequency (38 kHz). A matrix circuit then extracts the sum and difference of the recovered L−R signal and the main channel L+R signal to obtain L and R outputs. Attenuation at 38 kHz (due to the frequency response roll-off of a typical i.f. amplifier/f.m. detector) would reduce the amplitude of the sub-channel information relative to that of the main channel information, thereby reducing the channel separation. The droop in the frequency response of the stereo decoder at 38 kHz due to the i.f./detector frequency response roll-off (−3 dB at 59 kHz) is therefore compensated by the matrix circuit to give channel separation of at least 30 dB. A parallel RC network can be connected in series with the MPX input at pin 16 to provide slight h.f. emphasis for compensation of more i.f. roll-off or to achieve maximum channel separation.

Output stages and de-emphasis

The amplified stereo outputs from the matrix are available via current sources (I = 270 μA). External capacitors connected in parallel with the output load resistors provide the 50 μs de-emphasis for the output signals.

The performance evaluation circuit in Fig.2 is optimized for use in 6 V portable radios where the minimum supply voltage is 3,6 V. In this case, with the input amplifier set to about unity gain (R_2 = 47 kΩ), the output levels (with 0,5% THD) into a 5,1 kΩ loads are typically 570 mV r.m.s. for an MPX input level of 1,5 V_{p-p}. For applications with a higher supply voltage (for example car radios with a supply of 7,5 V), the total output loads can be increased to 9,5 kΩ (12 kΩ loads resistors in parallel with 50 kΩ a.c. loads). Output voltages (0,5% THD) up to 900 mV r.m.s. can then be obtained for an input level of 800 mV_{p-p}.

PERFORMANCE OF THE EVALUATION CIRCUIT

The following performance figures were measured in the performance evaluation circuit shown in Fig.1 using a random specimen of the TEA5580. Unless stated otherwise, the measuring conditions were as follows: supply voltage = 6 V, MPX input signal = 1 V_{p-p}, MPX signal (L = 1), f_m = 1 kHz; 10% pilot-tone; R_3 set to 180 Ω.

parameter	value	unit
Pilot-tone input level for mono to stereo switching		
overall gain = 0 dB	20,5	mV
overall gain = 10 dB	6,5	mV
Pilot-tone input level for stereo to mono switching		
overall gain = 0 dB	16	mV
overall gain = 10 dB	5	mV
Pilot-tone cancelling	52	dB
Input level for THD = 0,3% at output	380	mV
Channel separation		
f_{mod} = *200 Hz to 8 kHz*	>30	dB
f_{mod} = *500 Hz to 2,5 kHz*	>40	dB
PLL capture range with 32 mV pilot level		
C_5 = *470 nF*	5	%
C_5 = *220 nF*	8	%
VCO frequency change for supply voltage variation from 6 V to 3,6 V	2,5	%
Temperature coefficient of the VCO	400	ppm/K
Output spectrum referred to 1 kHz output, left channel		
at 19 kHz	−52	dB
at 38 kHz	−46	dB
at 57 kHz	−50	dB
at 76 kHz	−68	dB
at 95 kHz	−64	dB
at 114 kHz	−71	dB
100 Hz ripple rejection (including rejection of supply filter)	50	dB
ACI suppression with 1% spurious signal		
(f = 110 kHz)	98	dB
(f = 186 kHz)	68	dB
Intermodulation products		
1 kHz intermodulation referred to output due to 1 kHz modulation		
f_{mod} = *10 kHz*	−59	dB
f_{mod} = *13 kHz*	−58	dB
VWF suppression		
5% spurious signal, f = 57 kHz, f_{mod} = 23 Hz (m = 0,6)	88	dB
Output level (THD = 0,5%)		
gain = 0 dB, V_S = 6 V, R_{load} = 5,1 kΩ, $V_{i\,p-p}$ = 1,5 V	570	mV
gain = 6 dB, V_S = 7,5 V, R_{load} = 10 kΩ, $V_{i\,p-p}$ = 0,8 V	900	mV
SDS control current at pin 4 (see Fig.3)		
for 0 dB channel separation	<14	μA
for 26 dB channel separation	65	μA

Quality of small-signal, low and medium power diodes

GRAHAM HINE

Increasing circuit complexity and rising maintenance costs make the use of high quality components in electronic equipment an economic and practical necessity. High quality is achieved for our small-signal, medium and low-power diodes by using advanced production techniques and a strict quality control procedure. These diodes handle currents up to 3,5 A and their high initial quality is combined with low infant mortality and long-term reliability. They are manufactured under CECC-approved conditions and many of them have full CECC release. Factors contributing to their high quality are a rugged, hermetically-sealed structure which is virtually immune to thermal fatigue, and junction passivation which results in very stable characteristics. Furthermore, their glass encapsulation overcomes the limitations of plastic encapsulation and ensures non-flammability.

GENERAL QUALITY ASPECTS

Although the construction and applications for glass-bead rectifiers and glass encapsulated diodes are completely different, the quality control procedures for the two types of components are principally the same. The actual test conditions however, reflect the differences between the diode technologies.

Definitions

The terms used in this article are from the relevant IEC publications. From IEC Publicatios no. 134.

- "Ratings" are values which establish either a limiting capability or a limiting condition for an electronic device Limiting conditions may either be maxima or minima.
- "Absolute maximum ratings" are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, and must not be exceeded under worst-case conditions. Limiting values are chosen by the manufacturer to ensure acceptable serviceability.

Definitions used in association with life testing and reliability determination are from IEC Publication No. 271:

- A "failure" is the termination of the ability of an item to perform its required function. Various degrees of failure are defined.
- A "partial failure" is a failure resulting from deviations of characteristics beyond specified limits, but not such as to cause a complete lack of the required function. It is common to divide "partial failures" into major and minor categories according to the degree of deviation of the characteristics.
- A "complete failure" is a failure resulting from deviations of characteristics beyond specified limits such as to cause a complete lack of the required function.

Reliability is defined as the ability of an item to perform a required function under stated conditions for a stated period. Its practical measure is "failure rate" which is the ratio of the total number of failures in a single sample to the total cumulative observation time for that sample. Two "failure rates" are generally quoted. One is "observed failure rate" which is the number of failures divided by the total device-hours. The other is "failure rate at a given confidence level" (usually 60%). This gives the probability that the quoted "failure rate" will not be exceeded by the products from which the tested sample was drawn.

Quality built-in

It is recognized that quality cannot be ensured by testing alone. A product must have the required quality designed-in, proved during development, and realized in production by the use of high-grade materials in a well-controlled process. The process is controlled by a stringent system of Quality Control that gathers data from line inspection, laboratory testing and field experience, and uses it to correct processing deviations.

Successful Quality Control is cost-effective for both manufacturer and customer. Unsatisfactory designs and technologies are prevented from reaching full production by Quality Control during development. In production, potentially-defective components are screened out at an early stage while their costs are still low. Deviations of processing conditions are detected and rectified before yields suffer. The low level of rejects, and the high reliability of the delivered products ensure correspondingly low fall-off and service call rates for the equipment manufacturer.

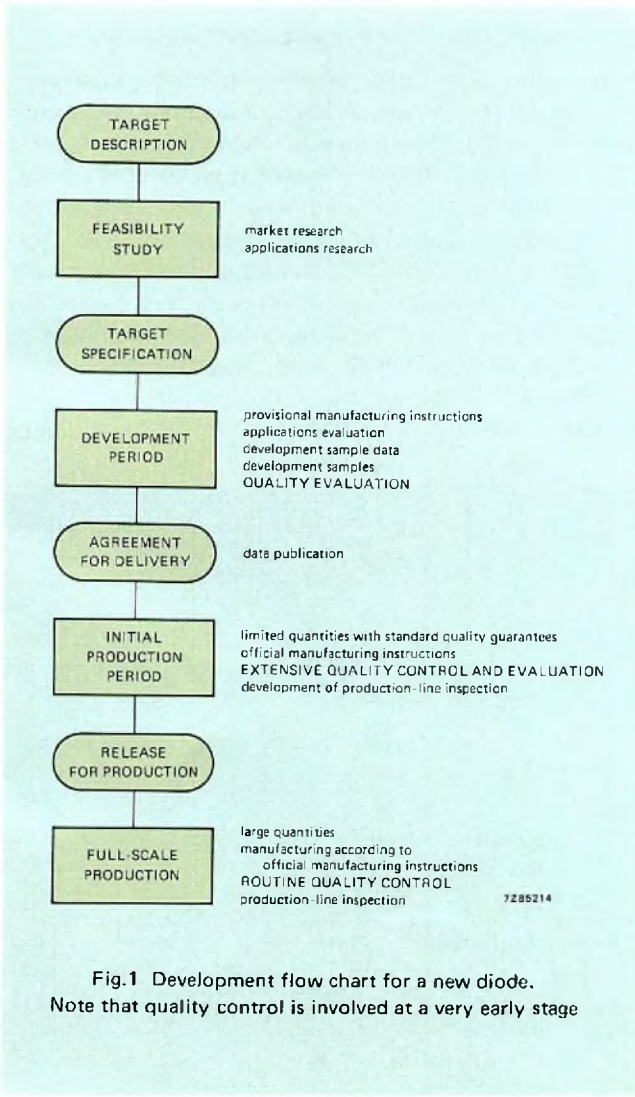


Fig.1 Development flow chart for a new diode. Note that quality control is involved at a very early stage

Quality in development

Figure 1 shows the principal stages through which each new diode type must pass before it is accepted for full-scale production. Our Quality Department becomes involved at the earliest possible stage.

Samples of each new diode type are checked against the target specification for performance and reliability, and the design proved by climatic, mechanical and life testing. The data obtained are used to progress the new diode through a formal approval procedure which thoroughly explores all aspects of a new product before production commences.

Once performance and quality requirements are confirmed on samples from pilot production, the new diode type is granted formal Agreement For Delivery and goes into limited production. At this stage, extensive quality determination exercises establish whether the diode characteristics are sufficiently reproducible, and its performance sufficiently reliable for full production. Only after these conformance and reliability requirements have been satisfied is formal Release For Production granted so that full production can commence.

Quality in production

The production-line flow chart of Fig.2 shows how inspection and Quality Control are integrated into the manufacturing process at all stages. Line inspection is part of the manufacturing process but acceptance tests and control inspections are carried out independently by the Quality Department.

Quality in final inspection

Following the 100% final inspection, the Quality Department takes samples from all batches of diodes and subjects them to a variety of electrical tests with the aim of maintaining and improving product quality. The Quality Department also examines the spreads of all published characteristics, and subjects the diodes to a number of mechanical and environmental tests and life tests under conditions that include operation at Absolute Maximum Ratings.

CECC

Our diodes are manufactured in a CECC approved factory, and, as shown in Appendix 3, several types can be supplied with full CECC release. Additional routine testing according to CECC requirements is carried out by the Quality Department on samples from all batches with CECC release. Certified test records are maintained.

AQL definition

The "Acceptable Quality Level (AQL)" is the maximum percentage of defective components that, for purposes of sampling inspection, can be considered satisfactory as a process average.

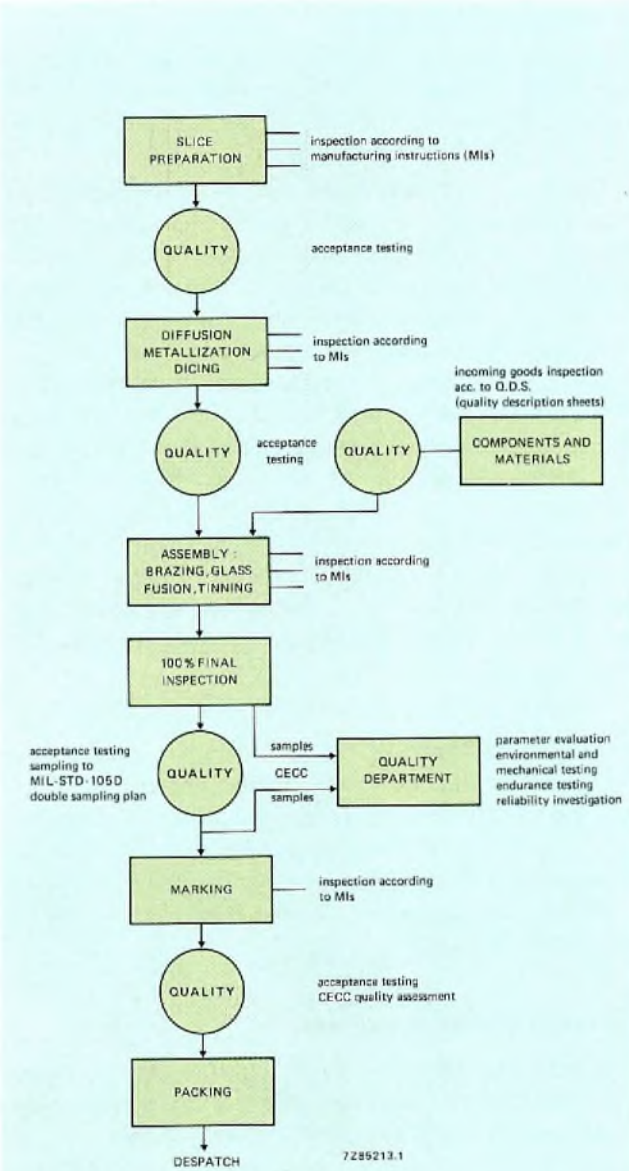


Fig.2 Production flow chart for a diode showing the involvement of quality control at all stages

Conformance

The Quality Department carries out acceptance testing to determine the conformance (or zero-hour quality) level on a statistical basis. Tests establish whether each batch meets the required Acceptable Quality level (AQL). Our standard AQLs are given in Table 1. The Quality Department also monitors process average (ppm levels).

PPM schemes

An effective way to confirm the quality of a product is a PPM (parts per million) scheme of which there are many with a wide variety of names. Ideally, a large-scale user accurately records the number of rejects in each position in his equipment. This allows the gross number of rejects per type number and per position to be recorded. To make this information effective, a frank relationship must exist between the customer and the supplier to allow exchange of information. This allows both parties to expose both strong and weak points.

An excellent PPM scheme used by one of our customers operates as follows:

1. The reject levels at each position are expressed in ppm. The number of rejects may be different for identical components in different positions.
2. Positions with the highest reject levels are chosen for analysis.
3. The components are analysed to determine the cause of failure. Usually this results in equal numbers of failures due to supplier's fault, user's fault and external causes.
4. The user and supplier together determine what actions can be taken to decrease the number of faults for which each is responsible.
5. New target PPMs with a time-schedule are agreed.

We are very satisfied with the results of this manufacturer/user cooperation because it helps us improve our quality and shows us how we compare with our competitors. Table 2 shows the failure figures obtained from the PPM scheme. Since a PPM scheme is a continuous process however, the failures can be expected to gradually decrease. Table 2 was compiled at the end of 1982. To simplify the survey, only the figures for families of types have been given. Figures for individual types may be different. Also, since the figures in Table 2 are the results obtained from a specific PPM scheme, they may not be the same as figures obtained with other schemes.

TABLE 1
Standard AQLs for diodes

Inspection criterion	AQLs		inspection level
	individual	combined	
Inoperatives			
mechanical	0,1%	0,1%	II
electrical	0,1%		II
Mechanical/visual			
major dimensions	0,65%	–	S2
other dimensions	6,5%	–	S2
visual	0,65%	2,5%	II
Electrical characteristics			
major	0,4%	0,65%	II
other	2,5%	–	S2

TABLE 2
Average failures indicated by a ppm scheme

	DO-34/35 Signal Diodes	DO-35 Zeners	Glass bead rectifiers	unit
Incoming inspection at equipment manuf.	20	15-40	40	ppm
Nett line rejects at equipment manuf.	10	40	10	ppm

GETTING THE BEST FROM OUR DIODES

Naturally, the test conditions used by our Quality Department are so chosen that they are as representative as possible of the general conditions of use, and can, by suitable manipulation, be used to predict reliability in service. Ultimately, however, the high reliability of which our diodes are capable can only be realized in practice if proper care is taken in the design and manufacture of the equipment in which they are used. Three areas require special attention.

Component selection

It is important that both the performance and quality specifications of a diode are suited to the application. Ratings should be as generous as possible. Operation above the ratings drastically reduces reliability.

Environment

The diodes must be suitably located and mounted. Allowances must be made for voltage transients and current surges. Sufficient cooling is vital. Check that the printed-wiring board track dimensions are adequate. Thermal-conductivity data for various mounting methods are given in the diode data. Due consideration must also be given to equipment working conditions such as shock, vibration, ambient temperature and atmospheric conditions.

Circuit design

Operating conditions must be determined with regard to overall component, circuit, and environmental tolerances. The effect of a component failure on other components should be considered.

GLASS-BEAD RECTIFIERS

Construction

Glass-bead diodes were designed to eliminate the following major causes of plastic rectifier failures:

- open-circuits due to thermal fatigue (power cycling)
- open-circuits due to stresses during handling and circuit assembly
- short-circuits due to faulty junction passivation or overstess.

The general arrangement of a glass-bead rectifier, with its main quality-oriented features, is shown in Fig.3. A round, bevelled, double-diffused die is alloyed to two molybdenum studs. A bead of cavity-free glass, whose temperature coefficient matches that of the studs, passivates and protects the junction and imparts mechanical strength to the diode. Axial leads are brazed to the studs for good thermal conductivity, copper-plated for corrosion resistance and tinned for good solderability.

Important features of glass-bead diode construction are:

- mechanical strength
- hermetic sealing which also eliminates flammability problems
- small size which allows high packing density
- high-temperature metallurgical bonds (no soft solder)
- well-matched coefficients of expansion of component materials.

The performance of the semiconductor die is improved by:

- bevelled edges
- glass passivation of the junction
- measures taken to control avalanche behaviour.

Fig.3 Glass-bead rectifier

The performance of glass-bead diodes is characterized by:

- high stability
- no thermal-fatigue failures
- no temperature-cycling failures
- high tolerance to reverse-voltage transients
- good forward-surge and inrush-current behaviour

The failure rate of glass-bead rectifiers is between one fifth and one tenth of that for rectifiers with plastic encapsulation.

Product range

Our glass-bead diodes are currently available in the three envelopes shown in Fig.4: the SOD-57, for currents up to 2 A, the larger SOD-64 for currents up to 3,5 A, and the SOD-72, up to 1 A. The present range includes:

- controlled-avalanche rectifiers
- very fast soft-recovery avalanche diodes
- parallel efficiency diodes for tv deflection circuits
- e.h.t. soft-recovery avalanche diodes
- voltage regulator diodes
- transient suppressor diodes.

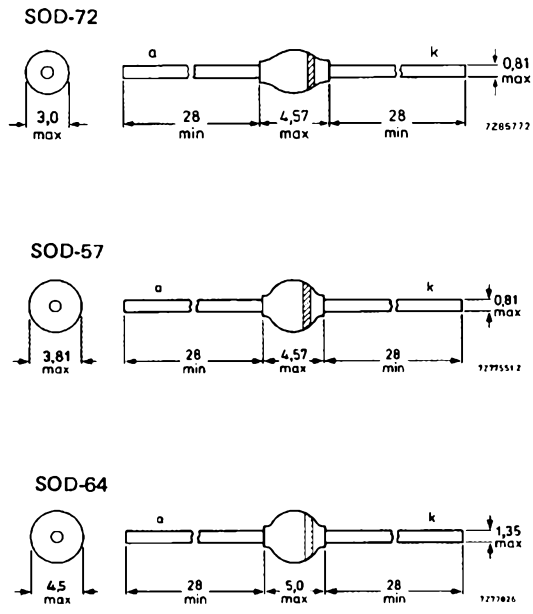


Fig.4 Glass-bead diode packages. (Dimensions in mm)

Test methods and results

Parameter evaluation. Production line inspection relies on the measurement of certain critical diode properties. To ensure that these measurements adequately verify all published electrical characteristics, additional measurements are made by the Quality Department.

Mechanical and environmental testing. One aspect of the reliability of glass-bead diodes is their ability to withstand the mechanical stresses and temperature changes experienced during handling and circuit assembly. While the diodes are in limited production, several test methods are selected to effectively monitor the quality that will be achieved in production. Each week, twenty diodes sampled from the production of each envelope type are subjected to the following sequence of tests:

- electrical measurements according to the published data
- examination for visible defects according to the visual specification
- ability to withstand soldering heat: 300 °C applied to the lead for 10s, 1,5 mm from the body
- lead fatigue: leads bent 90° four times with 5 N applied to each lead; checks the stength of the brazing, sealing glass, and the leads
- temperature cycling: 5 cycles from −65 °C to +175 °C; checks the structural integrity of the assembly
- tension: 75 N for 3s: checks the stud-to-die bond
- damp heat: 6 cycles, each comprising 16 h at 55 °C with a relative humidity of 95% to 100% followed by 8 h at 25 °C with a relative humidity of 80% to 100%; checks hermeticity after the mechanical tests and temperature treatments
- electrical measurements according to the published data.

The following additional tests are performed at regular intervals:

1. Solderability before and after ageing
2. Shock, vibration and acceleration
3. Lead torque and tension
4. Extreme temperature cycling.

Results of mechanical and environmental tests performed since the start of production are given in Appendix 1.

Life tests. As with the mechanical and environmental tests, the appropriate life-test methods are selected during the initial production period. Glass-bead diodes are, where possible, tested at absolute maximum ratings, as defined in IEC Publication No. 134. Tests are performed under the following conditions:

- resistive load
- V_R continuous (high temperature reverse bias) } at T_j max.
- I_F continuous
- high and low temperature storage.

Results of life tests performed since the start of production are given in Appendix 1.

Failure rates. For glass-bead diodes, the initial 168 hours of operation at Absolute Maximum Ratings is the early or infancy failure period of the bathtub curve. Appendix 1 gives the results of life tests during the early failure period. Only complete failures are given. After 168 h operation at absolute maximum ratings, the failure rates become virtually constant. Appendix 1 also gives the results of life tests during the constant failure period. Both observed failure rates and assessed failure rates with 60% upper confidence level are given.

Effects of derating

Increasing stress decreases reliability. The various chemical and physical changes that contribute to failure mechanisms generally accelerate with increasing temperature. Excessive currents and voltage contribute to device failure. Derating devices to operate at lower stress levels:

- can considerably increase component life
- reduces the probability of the failure of borderline components
- leaves a greater safety margin within which components can withstand extraordinary stresses (transients and surges) that might otherwise be damaging or destructive
- improves long-term stability of component characteristics.

Figure 5 gives the failure-rate multiplication factor for glass-bead diodes as a function of operating junction temperature. This curve assumes that the failure cause will be reverse instability, which has an activation energy of 1,4 eV to 2,0 eV. The construction of glass-bead diodes is such that, even under high stress levels, thermal fatigue failures have not been found after 200 000 cycles with a temperature change of 200 °C.

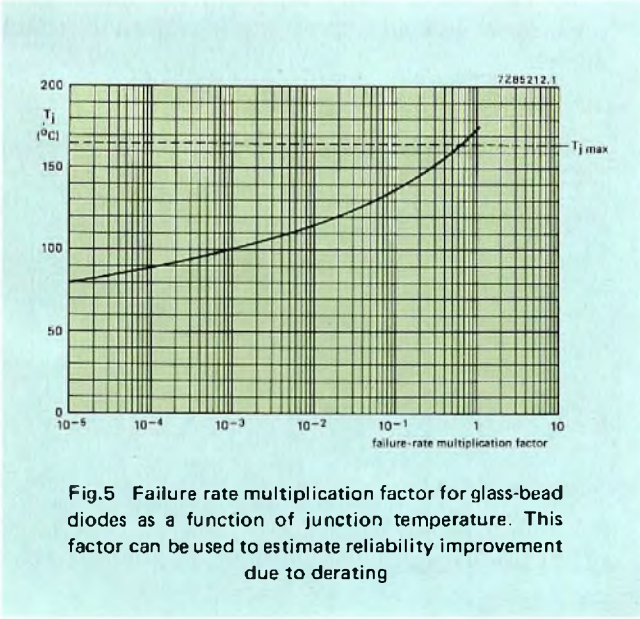


Fig.5 Failure rate multiplication factor for glass-bead diodes as a function of junction temperature. This factor can be used to estimate reliability improvement due to derating

The assumptions of Fig.5 and the results in Appendix 1 allow determination of the effect of derating to an operating junction temperature of 100 °C on failure rates of glass-bead diodes under the test conditions used for life testing. At 100 °C, glass-bead diode failure rates are of the order of 10×10^{-9}/h. The period 10^9 h is now known as "Time Standard" for reliability. Thus a failure rate of 10×10^{-9}/h can also be expressed as 10 Failures In Time Standard (10 FITS).

SMALL-SIGNAL AND LOW-POWER DIODES

Construction

The general arrangement of these diodes is shown in Fig.6. They are made by clamping a semiconductor diode chip between two metal (Dumet) studs and shrinking on a glass tube. Titanium silver metallization of the chip ensures stability and high reliability of the contacts. The glass clamps the studs against the chip with sufficient pressure to ensure reliable electrical contact. Thermal expansion coefficients of the chip, studs and glass tube are carefully matched to ensure a constant contact pressure over a wide range of temperature.

Our experience of glass technology has been obtained over many years and allows us to achieve virtually hermetic glass-to-metal seals. Consequently, our small-signal and low-power diodes are stable, robust devices with low leakage currents, even with high reverse voltages and at high temperatures.

Fig.6 Glass encapsulated diode

Figure 6 shows the construction in a cut-away view of the DO-35 package. Dimensions of this and other similar diode packages are given in Fig.7.

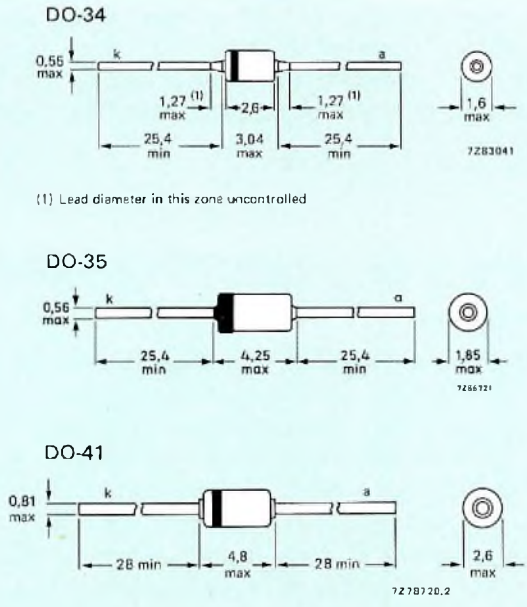


Fig.7 Standard glass encapsulations. (Dimensions in mm)

Advantages of the simple, sturdy construction are:

- high immunity to surges
- high resistance to mechanical shock
- efficient heat transfer
- hermetic encapsulation
- ability to withstand high junction temperature.

Chip technology

We manufacture both planar and mesa processed diodes, the chip constructions of which are compared in Fig.8. The mesa types, with their large junction area are typified by the BAS11 (V_{Rmax} = 300 V, I_{Fmax} = 350 mA).

The planar types are processed with the same advanced techniques which are well-established for transistors and integrated circuits. The planar technology, with its close-tolerance dimensions and accurately controlled impurity profiles, results in design features such as controlled breakdown, very low capacitance, fast switching and low, stable, reverse leakage current.

Process control

As a result of failure and inoperative-diode analysis, we have developed production techniques which have greatly improved quality. The most important improvements are those connected with the elimination of 'flakes', which are conductive particles would cause trouble if they entered the diode packages. The occurrence of flakes is minimized by:

- tightly controlling chip metallization
- replacing diamond scribing by laser scribing which results in finer scribed lines and a smaller area of exposed silicon
- working in well-controlled and dust-free manufacturing conditions
- rinsing and sieving of the chips
- vacuum cleaning of leads, glass tubes and chips during assembly in jigs.

Product range

Most of our small-signal and low-power diodes are in one of the three packages shown in Fig.7; the mini diode package DO-34, the standard DO-35 and the DO-41 for high dissipation diodes. Available types of diode include:

- small signal general purpose and high-speed switching diodes
- Schottky-barrier switching diodes
- variable-capacitance tuning diodes for radio and television

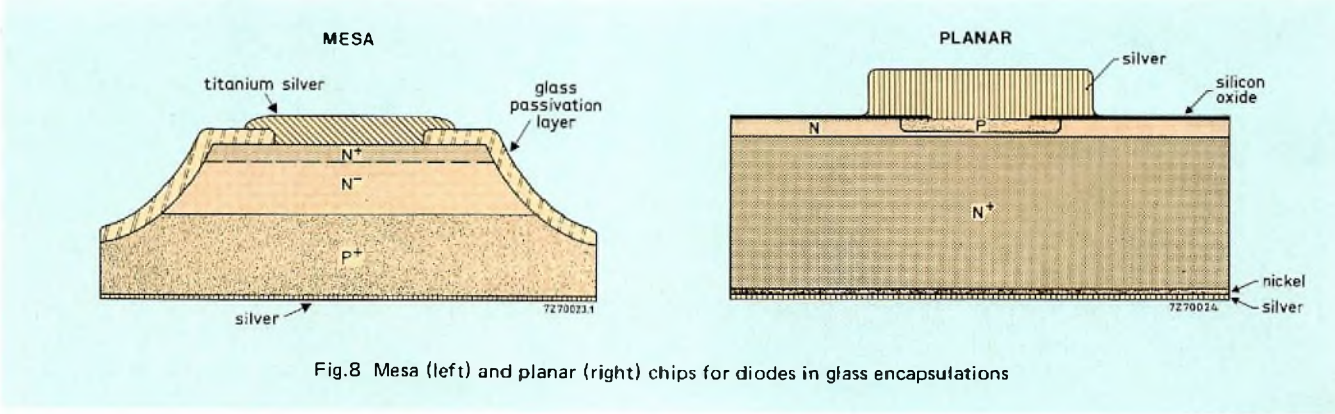


Fig.8 Mesa (left) and planar (right) chips for diodes in glass encapsulations

- band-switching diodes for radio and television
- Schottky-barrier diodes for u.h.f. mixers and f.m. ratio detectors
- voltage-reference diodes and stabistors
- voltage-regulator diodes
- low leakage diodes.

For full details of our range of diodes, refer to the current edition of data handbook S1.

Test methods and results

Quality Department tests check that the 100% line inspection standards are maintained. The results are used to correct production variations and indicate modifications that could improve quality.

Mechanical and environmental tests. When a new diode is put into full production, methods of testing to monitor and maintain quality are developed. Some of the tests are mechanical and environmental. Although fairly easy to perform, they are adequate to detect deviations from the original design specification. The tests are performed in two groups and in the following sequences.

Group I
(performed weekly on 20 diodes in each type of encapsulation)

1. 'Bomb' test: 16 h immersion in ethyl-alcohol at an absolute pressure of 497 kPa (kN/m^2).
2. Electrical measurements according to type.
3. Soldering heat: both leads immersed in 60/40 tin/lead solder at 300 °C to within 1.5 mm ± 0.5 mm of the body of the diode for 10 ± 1 s.
4. Lead fatigue (bending): with the body clamped and 5 N weights attached to the leads, each lead is bent through 90° four times.
5. Tension: one lead is clamped and a tension of 25 N is smoothly applied to the other for 3 s.
6. Repeat of test 1.
7. Repeat of test 2.

Group II
(performed weekly on 50 diodes in each type of encapsulation)

1. Electrical measurements according type.
2. Boiling water test: diodes immersed in boiling water (100 °C) for 48 h.
3. Repeat of test 1.

The results of Group I and II tests are summarized in Appendix 2. The following additional tests are performed at regular intervals:

damp heat

solderability

vibration

acceleration

temperature cycling.

Life tests. We life-test our small-signal and low-power diodes at their absolute maximum ratings under the following conditions:

- resistive load
- V_R continuous (high temperature reverse bias) } at $T_{j\,max}$.
- I_F continuous
- high and low temperature storage.

In some cases $T_{j\,max.}$ is attained by adjusting the ambient temperature. For example, with V_R applied, T_{amb} is set to $T_{j\,max}$. The number of diodes and the frequency with which they are tested depends on the type and intended application. Usually, a batch of 10 diodes will be subjected to these tests for 1 week (168 h). Other batches are tested for 6 weeks (1000 h) and 8000 h.

Results of life tests are given in Appendix 2.

Effects of derating

The failure rates given in Appendix 2 were obtained under conditions that caused the maximum permissible junction temperatures. Failure rates are reduced at lower junction temperatures. Figure 9 gives the failure-rate multiplication factor as a function of operating junction temperature. In the region 20 °C to 175 °C, this curve is based on data given in MIL/HDBK/217B of September 1976. The region 175 °C to 200 °C is obtained by extrapolation using Arrhenius charts.

Field results

Although our diodes are used in very large quantities in many applications, it is often difficult to obtain information about service failures under conditions which are sufficiently controlled to make the data useful. However, some very useful data, derived from failure analysis of telecommunication equipment in the period 1974 to 1980, are given in Table 3. The diodes were operated well within their ratings. Junction temperatures were always below 100 °C and maximum load was always less than 50% of the permissible maximum. Since the operating conditions and definitions of failure were different from those used in the life tests reported in Appendix 2, the two sets of data are not directly comparable. The figures in Table 3 do, however, illustrate the very low failure rates obtainable by derating, and confirm the derating curve of Fig.9.

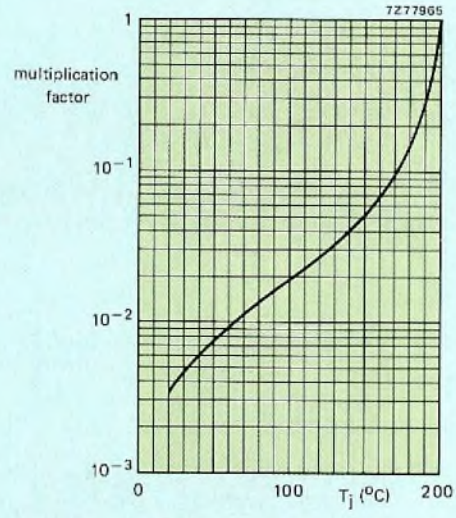


Fig.9 Failure rate multiplication factor for diodes in standard glass encapsulations as a function of junction temperature. This factor can be used to estimate reliability improvement due to derating

TABLE 3
In-service reliability of small-signal and low-power diodes

type	number in service	device hours (× 10^6)	failures*	failure rate (60% conf.)
BAV10	1 357 913	47 457	4	0,11 × 10^{-9}/h
BAX12(A)	3 953 388	130 500	46	0,37 × 10^{-9}/h
BAV21	812 985	18 274	3	0,23 × 10^{-9}/h
BZX79	264 022	8 889	11	1,4 × 10^{-9}/h

* Failure criteria: open/short-circuit or sufficient drift of characteristics to prevent correct operation of the system.

SURFACE-MOUNTED DIODES

In addition to glass encapsulated diodes with axial leads, we manufacture a range of diodes for surface mounting. These diodes are encapsulated in plastic packages type SOT-23, SOT-89, SOT-143 and glass package SOD-80. The diodes in SOT encapsulations are assembled in a similar way to transistors (die attach and wire bonding) but those in the SOD-80 encapsulation are assembled in the same way as diodes in the standard DO-34 glass encapsulation. Much of the quality information which has been given for our small-signal and low-power diodes is therefore also valid for surface mounting diodes in the SOD-80 encapsulation.

APPENDIX 1 – TEST RESULTS FOR GLASS-BEAD DIODES

Mechanical and environmental tests

Failure criteria

	minor partial failures	major partial failures	complete failures
BYW56:			
V_F at I_F = 5 A	>1,35 V	>1,50 V	>2,70 V
I_R at V_R = 1000 V	>1 μA	>2 μA	>5 μA
$V_{(BR)R}$ at I_R = 0,1 mA	<1100 V <1600 V	–	–
BY228:			
V_F at I_F = 5 A	>1,50 V	>1,65 V	>3,00 V
I_R at V_R = 1500 V	>1 μA	>2 μA	>5 μA
Tension test only (both types)			
V_F at I_F = 1 A	ΔV_F > 20 mV	–	broken

Results

type	envelope	number tested	minor partial failures	major partial failures	complete failures
BYW56	SOD-57	2980	12 (0,4%)	9 (0,30%)	11 (0,37%)
BY228	SOD-64	1660	12 (0,72%)	3 (0,18%)	8 (0,48%)

Life tests

The following tables show complete failures (F), test duration in thousands of hours (kh), observed failure rate (FR_0) and assessed failure rate (FR_{60}) at an upper confidence level of 60% (UCL = 60%). All tests were at *absolute maximum ratings.*

Constant failure period

Since the data were obtained from tests with a duration of 1000 hours or more, they apply to the constant failure period.

BY228, test period 1980 - 1982

test	F	kH	FR_0 $\times 10^{-6}$/h	FR_{60} $\times 10^{-6}$/h
V_R continuous (HTRB)	5	360	13,9	17,4
I_F continuous	0	260	0	3,5
high/low temp. storage	0	350	0	2,6

BY448, test period 1979 - 1982

test	F	kh	FR_0 $\times 10^{-6}$/h	FR_{60} $\times 10^{-6}$/h
V_R continuous (HTRB)	2	400	5,0	7,7
I_F continuous	0	430	0	2,1
high/low temp. storage	0	310	0	3,0

BYV27, test period 1980 - 1982

test	F	kh	FR_0 $\times 10^{-6}$/h	FR_{60} $\times 10^{-6}$/h
V_R continuous (HTRB)	0	310	0	3,0
I_F continuous	0	290	0	3,2
high/low temp. storage	0	210	0	4,4

BYV28, test period 1980 - 1982

test	F	kh	FR_0 $\times 10^{-6}$/h	FR_{60} $\times 10^{-6}$/h
V_R continuous (HTRB)	1	440	2,3	4,6
I_F continuous	0	330	0	2,8
high/low temp. storage	0	390	0	2,4

BYV95C, test period 1980 - 1982

test	F	kh	FR_0 $\times 10^{-6}$/h	FR_{60} $\times 10^{-6}$/h
V_R continuous (HTRB)	2	480	4,2	6,4
I_F continuous	0	400	0	2,3
high/low temp. storage	0	330	0	2,8

BYV96E, test period 1980 - 1982

test	F	kh	FR_0 $\times 10^{-6}$/h	FR_{60} $\times 10^{-6}$/h
V_R continuous (HTRB)	0	370	0	2,5
I_F continuous	0	280	0	3,3
high/low temp. storage	0	420	0	2,2

BYW54/55/56, test period 1977 - 1982

test	F	kh	FR_0 $\times 10^{-6}$/h	FR_{60} $\times 10^{-6}$/h
R and RC loads	1	634	1,6	3,2
V_R continuous (HTRB)	5	750	6,7	8,4
I_F continuous	0	843	0	1,1
high/low temp. storage	0	806	0	1,2

BYW95C, test period 1980 - 1982

test	F	kh	FR_0 $\times 10^{-6}$/h	FR_{60} $\times 10^{-6}$/h
V_R continuous (HTRB)	1	480	2,1	4,2
I_F continuous	1	400	2,5	5,0
high/low temp. storage	0	330	0	2,8

BYW96E, test period 1980 - 1982

test	F	kh	FR_0 $\times 10^{-6}$/h	FR_{60} $\times 10^{-6}$/h
V_R continuous (HTRB)	0	440	0	2,1
I_F continuous	0	160	0	5,7
high/low temp. storage	0	290	0	3,2

BZT03, test period 1982 - 1983

test	F	kh	FR_0 $\times 10^{-6}$/h	FR_{60} $\times 10^{-6}$/h
dissipation	0	900	0	1,0
high/low temp. storage	0	270	0	3,4

Results for all types of diode, classified by test type are:

All types, test period 1977 - 1982

test	F	kh	FR_0 $\times 10^{-6}$/h	FR_{60} $\times 10^{-6}$/h
R and RC loads	1	634	1,6	3,2
V_R continuous (HTRB)	16	4030	4	4,4
I_F continuous	1	3393	0,29	0,6
high/low temp. storage	0	3706	0	0,25

Early failures

The following are the percentages of complete failures which occurred during the first 168 hours of all life tests of that duration or longer. All tests were at *absolute maximum ratings.*

type	number tested	early failures	% failures observed	% failures at 60% UCL
BY228	1150	4	0,35	0,46
BY448	1220	6	0,49	0,60
BYV27	530	0	0	0,17
BYV28	580	0	0	0,16
BYV95C	870	3	0,34	0,47
BYV96E	770	3	0,39	0,54
BYW54/55/56	5281	10	0,19	0,22
BYW95C	880	1	0,11	0,23
BYW96E	490	3	0,61	0,85
BZT03	1170	2	0,17	0,27

The early failures for all types, classified by test type were as follows:

test	number tested	early failures	% failures observed	% failures at 60% UCL
practical circuits	660	3	0,45	0,63
R and RC loads	2172	5	0,23	0,29
V_R continuous (HTRB)	3890	21	0,54	0,59
I_F continuous	3403	1	0,03	0,06
high/low temp. storage	1916	0	0	0,05

APPENDIX 2 – TEST RESULTS FOR SMALL-SIGNAL AND LOW-POWER DIODES

Mechanical and environmental tests

Failure criteria

	minor partial failures	major partial failures	complete failures
BAW62:			
V_F at I_F = 100 mA	>1000 mV	>1100 mV	>2000 mV
I_R at V_R = 20 V	>25 nA	>50 nA	>250 nA
I_R at V_R = 75 V	>5 μA	>10 μA	>50 μA
BZV85:			
I_R at published V_R	>USL	>2 x USL	>10 x USL
V_F at I_F = 50 mA	>1000 mV	>1100 mV	>2000 mV
V_Z at published I_{Ztest}	>USL	$\Delta V_Z \pm 5\%$ of V_{Znom}	>1,1 x USL
	<LSL		<0.9 x LSL

In addition, diodes that have a forward voltage deviation of more than 10 mV with a forward current of 100 mA are classified as minor partial failures during the Group I tension test.

Results

	BAW62 DO-35 (SOD-27)		BZV85 DO-41 (SOD-66)	
	number	%	number	%
Group I tests				
tested	8070	100	1560	100
mechanical leakage	4	0,05	0	0
broken leads during bend test	5	0,06	0	0
complete failure on I_R	4	0,05	2	0,13
complete failure on V_F	11	0,14	0	0
minor partial failure on I_R	4	0.05	11	0,71
minor partial failure on V_F	122	1,51	1	0,06
Group II test				
tested	19250	100	2950	100
mechanical leakage	33	0,17	0	0
complete failure on I_R	24	0,12	8	0,27
minor partial failure on I_R	20	0,10	12	0,41

Life tests

The following tables show complete failures (F), test duration in thousands of hours (kh), observed failure rate (FR_0) and assessed failure rate (FR_{60}) at an upper confidence level of 60% (UCL = 60%). All tests were at *absolute maximum ratings.*

Constant failure period

Since the data were obtained from tests with a duration of 1000 hours or more, they apply to the constant failure period.

BAS11, test period 1980 - 1982

test	F	kh	FR_0 $\times 10^{-6}$/h	FR_{60} $\times 10^{-6}$/h
V_R continuous (HTRB)	1	540	1,9	3,7
I_F continuous	2	260	7,7	11,9
thermal fatigue	1	410	2,4	4,9
high temp.	0	330	0	2,8

BAV10, test period 1974 - 1982

test	F	kh	FR_0 $\times 10^{-6}$/h	FR_{60} $\times 10^{-6}$/h
R load	2	1180	1,7	2,7
V_R continuous (HTRB)	1	1460	0,68	1,4
I_F continuous	0	890	0	1,0
high temp. storage	0	1030	0	0,89

BAV21, test period 1974 - 1982

test	F	kh	FR_0 $\times 10^{-6}$/h	FR_{60} $\times 10^{-6}$/h
R load	2	1240	1,6	2,5
V_R continuous (HTRB)	1	1680	0,62	1,3
I_F continuous	1	970	1,0	2,1
high temp. storage	0	1368	0	0,67

BAW62, test period 1974 - 1982

test	F	kh	FR_0 $\times 10^{-6}$/h	FR_{60} $\times 10^{-6}$/h
R load	3	1310	2,3	3,2
V_R continuous (HTRB)	1	2040	0,49	0,99
I_F continuous	0	970	0	0,94
high temp. storage	0	1620	0	0,56

BAX12A, test period 1978 - 1982

test	F	kh	FR_0 $\times 10^{-6}$/h	FR_{60} $\times 10^{-6}$/h
R load	4	500	8,0	10,5
V_R continuous (HTRB)	3	940	3,2	4,4
high temp. storage	0	680	0	1,3

BZV10/BZV37/BZX90/1N821, test period 1979 - 1982

test	F	kh	FR_0 $\times 10^{-6}$/h	FR_{60} $\times 10^{-6}$/h
dissipation	0	440	0	2,1
thermal fatigue	4	470	8,5	11,0
high temp. storage	0	300	0	3,0

BZV46, test period 1981 - 1982

test	F	kh	FR_0 $\times 10^{-6}$/h	FR_{60} $\times 10^{-6}$/h
V_R continuous (HTRB)	2	140	14,3	22,0
I_F continuous	0	230	0	3,9
thermal fatigue	0	240	0	3,8

BZV85, test period 1979 - 1982

test	F	kh	FR_0 $\times 10^{-6}$/h	FR_{60} $\times 10^{-6}$/h
dissipation	1	1365	0,73	1,5
thermal fatigue	2	980	2,0	3,2
high temp. storage	5	515	9,7	12,2

BZX79, test period 1974 - 1982

test	F	kh	FR_0 $\times 10^{-6}$/h	FR_{60} $\times 10^{-6}$/h
dissipation	1	4958	0,20	0,41
thermal fatigue	4	2690	1,5	2,0
high temp. storage	0	4034	0	0,23

BAX12A, test period 1978 - 1982

BAX12A diodes were also tested in reverse-avalanche pulse circuits. The column SA denotes the number of switching actions.

test	F	SA $\times 10^6$	FR_0 $\times 10^{-6}$/SA	FR_{60} $\times 10^{-6}$/SA
I_R 100 mA pulse	7	1880	0,004	0,005
I_R 600 mA pulse	26	1880	0,014	0,015

Results for all types of diode, classified by test type are:

All types, test period 1974 - 1982

test	F	kh	FR_0 $\times 10^{-6}$/h	FR_{60} $\times 10^{-6}$/h
R load	11	4230	2,6	3,0
V_R continuous (HTRB)	9	6728	1,3	1,6
I_F continuous	3	3320	0,90	1,3
dissipation (zeners)	2	6763	0,30	0,46
thermal fatigue	11	4790	2,3	2,7
high temp. storage	5	9877	0,51	0,64

Early failures

The following are the percentages of complete failures which occurred during the first 168 hours of all life tests of that duration or longer. All tests were at *absolute maximum ratings.*

All types, test period 1974 - 1982

test	number tested	early failures	% failures observed	% failures at 60% UCL
R load	9540	17	0,18	0,20
V_R continuous (HTRB)	11554	22	0,19	0,21
I_F continuous	3710	6	0,16	0,20
dissipation (zeners)	13252	30	0,23	0,24
thermal fatigue	2590	7	0,27	0,33
high temp. storage	3983	5	0,13	0,16

Results for all types of diode, classified by test type are:

type	number tested	early failures	% failures observed	% failures at 60% UCL
BAS11	900	2	0,22	0,34
BAV10	7240	4	0,055	0,073
BAV21	6910	29	0,42	0,45
BAW62	9450	5	0,053	0,067
BAX12A	2500	5	0,20	0,25
BZV10 etc.	920	1	0,11	0,22
BZV46	810	1	0,12	0,25
BZV85	2980	6	0,20	0,25
BZX79	14701	34	0,23	0,25

Acknowledgement

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APPENDIX 3 – CECC APPROVALS

Types with CECC approval

NL-CECC 50 001-020	CV8805
	CV8308
NEN-CECC 50 001-021	BAW62
	1N4148
	1N4149
	1N4446
	1N4447
	1N4448
	1N4449
	1N914
	1N916
	CV8617
	CV9637
	CV7376
	CV7368
	CV7756
	CV7757
NL-CECC 50 011-022	BAV21
	BAV20
	BAV19
	BAV18
	BAX17
	BAX16
	CV8790
NL-CECC 50 001-026	BA314
	PO33
NL-CECC 50 001-037	CV9638
NL-CECC 50 001-038	CV7875
NL-CECC 50 005-005	BZX79C2V4 to BZX79C76 inclusive
	BZX552V4 to BZX55C75 inclusive
	BZY88C2V7 to BZY88C33 inclusive
	CV7099 to CV7106 inclusive
	CV7138 to CV7146 inclusive
NL-CECC 50 005-010	BZV85C3V6 to BZV85C75 inclusive
NL-CECC 50 005-017	BZT03C7V5 to BZT03C270 inclusive
NL-CECC 50 005-019	BZW03C9V1 to BZW03C270 inclusive
NL-CECC 50 008-015	BYW54
	BYW55
	BYW56
	1N5059
	1N5060
	1N5061
	1N5062
	CV7026
	CV7027
	CV7028
	CV7029
	CV7030
	CV7476

Types awaiting CECC approval

NEN-CECC 50 008-016	BYV27 series
NL-CECC 50 008-017	BYV95A, B and C
	BYV96D and E
NL-CECC 50 008-018	BYW95A, B and C
	BYW96D and E
NL-CECC 50 008-019	BYV28 series

Abstracts

Surface-mounted devices in printed circuit board assembly

The advent of leadless components that can be soldered direct to the surface of a printboard is changing the technology of circuit assembly: raising production rates, lowering costs, and improving reliability and high-frequency performance. Surface-mounted devices now available can satisfy 80% of today's circuit requirements; by the end of the decade, at least half the boards in production are expected to use surface mounting predominantly.

Video display and attributes controller ICs

A set of four ICs controls a colour or monochrome video display terminal incorporating such features as double-height and double-width character options, dot stretching, soft-scrolling, and bit-mapped graphics accessing. With the majority of the terminal's functions contained within the ICs, the hardware implementation is greatly simplified and the largest task becomes the design of the system's software and firmware.

The 68000 microprocessor design philosophy

The 68000 is the fastest, most powerful 16-bit microprocessor and yet one of the easiest to program. This article describes the architectural features of the 68000 that give the processor its speed, power and programming simplicity. The alternatives available to the design team are discussed and this illustrates why the 68000's architecture was chosen.

VHF power amplifiers with broadband input circuitry

With their latest computer-aided-designed electrode configuration, combined with new cavities incorporating a specially designed two-stage impedance transformer, the YL1610, YL1630 and YL1631 vhf transmitting tetrodes can operate, without tuning, over exceptionally broad input bandwidths – 82 to 110 MHz in band II and 170 to 250 MHz in band III. This eases transmitter operation, maintenance and tuning, and simplifies transmitter circuitry.

Two-chip modem for FSK data transfer

Operating at a carrier frequency of 5 MHz on 75 Ω coaxial cable in a token-passing network, a frequency-shift keyed modem using separate transmitter and receiver ICs can handle a data throughput comparable to Ethernet's. Automatic jabber control prevents an inactive transmitter from preempting the line. The carrier frequency can be adapted to the type of service intended and cable employed; at a carrier freqiency of 280 kHz, for instance the modem can operate at 56 kbit/s over 2,5 km of twisted-pair.

The BTV60 – first in a new generation of GTOs

A new generation of GTOs, heralded by the BTV60, can switch up to three times the current of former devices. The new devices are characterized by a much finer cathode structure, which means that they must be manufactured in planar technology rather than the mesa-trough technology of former GTOs.

Thermal aspects of flange-mounted r.f. power transistors

The impracticability of exact heat-flow analysis has led to misunderstandings about the mounting of r.f. power transistors. Detailed experimental studies now yield rules for thermally effective mounting that correct certain widespread misconceptions. For example, it is clearly demonstrable that torquing the mounting bolts beyond about 0.75 Nm increases the thermal resistance, and that lapped mounting surfaces are less effective that a thin layer of heatsink compound.

A new stereo decoder IC suits all classes of radio

A new integrated PLL stereo decoder, the TEA5580, not only performs all the basic stereo decoding functions with the minimum number of passive peripherals. It is also flexible enough in application to suit all conceivable types of radio from battery-powered portables to mains-powered hi-fi tuners. Additional features are: adjustable internal gain up to 20 dB, smooth d.c. control of mono/stereo switching (channel separation), pilot-tone cancellation, internal suppression of adjacent channel and VWF interference, i.f./detector roll-off compensation, and output levels that can be adjusted up to 900 mV.

Quality of small-signal, low and medium-power diodes

This article describes how high initial quality, combined with low infant mortality and long-term reliability, is achieved for our small-signal, medium and low-power diodes by using advanced production techniques and a strict quality control procedure. Factors contributing to the high quality of these components are a rugged, hermetically-sealed structure which is immune to thermal fatigue, and junction passivation which results in very stable characteristics.

Surface-Mounted Devices für die Montage auf Leiterplatten

Die Einführung von Bauelementen ohne Anschlussdrähte, die direkt auf die Oberfläche von Leiterplatten gelötet werden, revolutioniert die Schaltungsmontage: steigende Produktion, sinkende Kosten, erhöhte Zuverlässigkeit und verbessertes Hochfrequenzverhalten. Die jetzt verfügbaren Surface-Mounted Devices können 80% der heutigen Schaltungsanforderungen erfüllen; zum Ende des Jahrzehnts wird erwartet, dass wenigstens die Hälfte der produzierten Leiterplatten vorwiegend mit Surface-Mounted Devices ausgerüstet sein wird.

Video- und Attribute-Steuer-ICs für Datensichtgeräte-Controller

Ein Paket von vier ICs steuert ein Farb- oder Schwarzweiss-Datenterminal mit modernen Leistungsmerkmalen, wie doppelte Zeichenhöhe, doppelte Zeichenbreite, Punktdauer-Steuerung, langsamer Bilddurchlauf (soft-scrolling), Reihentafel-Addressierung und "bit-mapped"-Grafik. Da die Mehrzahl der Terminalfunktionen bereits in den ICs enthalten ist, vereinfacht sich die Hardware-Implementierung erheblich. Die Hauptarbeit besteht daher in der Entwicklung der System-Software und -Firmware.

Zum Entwurf des Mikroprozessors SC68000

Der SC68000 ist der schnellste und leistungsfähigste 16-bit-Mikroprozessor. Dennoch ist seine Programmierung einfach. Der Artikel beschreibt die Architektur-Merkmale des SC68000, die diesem Prozessor seine Geschwindigkeit, seine Leistungsfähigkeit und seine einfache Programmierbarkeit verleihen. Die Alternativen, die beim Entwurf des SC68000 möglich waren, werden besprochen. Dies lässt erkennen, weshalb seine Architektur in dieser Form gewählt wurde.

VHF-Leistungsverstärker mit Breitband-Eingangsschaltung

Die neuen VHF-Tetroden YL1610, YL1630 und YL1631 – mit modernsten und mit Rechnerunterstützung (CAD) entwickelten Elektrodensystemen – ermöglichen den Aufbau von Leistungsverstärkereinheiten grosser Bandbreite. Die beschriebenen Verstärkereinheiten enthalten spezielle zweistufige Impedanztransformatoren am Eingang, so dass sie von 82 MHz bis 110 MHz im Bereich I und 170 MHz bis 250 MHz in Bereich III ohne Abstimmassnahmen betrieben werden können. Der Senderaufbau wird vereinfacht, und der Betrieb, die Wartung und die Abstimmung des Senders werden erleichtert.

2-Chip-Modem für FSK-Datenverkehr

Ein FSK-Modem (FSK = Frequency Shift Keyed) mit getrennten Sende- und Empfangs-ICs kann in verteilten Systemen über 75 Ω-Koaxialkabel bei einer Trägerfrequenz von 5 MHz einen Datendurchsatz bewältigen, der dem von Ethernet vergleichbar ist. Eine automatische Verkehrsüberwachung vermeidet die vorzeitige Leistungsbelegung durch einen inaktiven Sender. Die Trägerfrequenz lässt sich an die Art des gewünschten Dienstes sowie des Kabels anpassen: bei einer Trägerfrequenz von 280 kHz z.B. kann das Modem mit einer Datenrate von 56 kbit/s über eine 2,5 km lange verdrillte Doppelleitung arbeiten.

BTV60 – der erste Typ einer neuen Generation von GTOs

Eine neue Generation von GTOs, angeführt vom Typ BTV60, kann Ströme schalten, die dreimal so hoch sind wie der bisherigen Typen. Die neuen GTOs sind durch eine wesentlich feinere Katodenstruktur charakterisiert, die die Herstellung in Planar-Technologie, im Gegensatz zu der bisher verwendeten Mesa-Technologie, erforderlich macht.

Thermische Aspekte zu HF-Leistungstransistoren in Flanschgehäusen

Die Schwierigkeit, exakte Wärmefluss-Analysen zu erstellen, hat zu Missverständnissen, bezüglich der Montage von HF-Leistungstransistoren geführt. Eingehende experimentelle Untersuchungen haben nun Regeln für eine thermisch günstige Montage ergeben, durch die gewisse weitverbreitete Fehlvorstellungen korrigiert werden. Beispielsweise hat sich klar ergeben, dass die beim Anziehen der Befestigungsschrauben ausgeübten Drehmomente, wenn sie grösser als 0,75 Nm sind, den thermischen Widerstand erhöhen. Auch wurde festgestellt, dass geläppte Montageflächen weniger wirkungsvoll sind als eine dünne Schicht Wärmeleitpaste.

Ein neuer, in allen Klassen von UKW-Rundfunkempfängern einsetzbarer Stereo-Decoder

Der neue integrierte PLL-Stereo-Decoder TEA5580 benötigt für die Stereo-Decodierung nur ganz wenige periphere Bauelemente. Die Schaltung ist so flexibel ausgelegt, dass sie in allen Typen von UKW-Radios verwendet werden kann, von batteriebetriebenen Taschenradios bis zu netzbetriebenen HiFi-Empfängern. Der Stereo-Decoder zeichnet sich durch folgende Besonderheiten aus: interne Verstärkung wählbar bis zu einem maximalen Wert von 20 dB, kontinuierlich zwischen Mono- und Stereo-Wiedergabe wählbarer Übergang (einstellbares Übersprechen zwischen den Tonkanälen), Pilotton-Unterdrückung, interne Unterdrückung von Nachbarkanal- und Verkehrswarnfunk-Signalen, Kompensation des ZF-Detektor-Frequenzgangabfalls sowie NF-Ausgangspegel wählbar bis max. 900 mV.

Qualitätsaspekte von Kleinsignaldioden für kleine und mittlere Leistungen

Dieser Artikel beschreibt, wie wir bei unseren Kleinsignaldioden für kleine und mittlere Leistungen ein hohes Qualitätsniveau, verbunden mit geringer Neigung zu Frühausfällen, durch leistungsfähige Produktionstechniken und kompromisslose Qualitätssicherung erreichen. Ein widerstandsfähiger, hermetisch dichter Aufbau, der frei ist von thermischer Ermüdung, sowie die Passivierung der Übergänge zur Stabilisierung der Eigenschaften tragen wesentlich zu dieser hohen Qualität bei.

Composants pour montage en surface (C.M.S.)

L'apparition de composants sans fils pouvant être soudés directement à la surface d'un circuit imprimé bouleverse la technologie de l'assemblage des circuits: augmentation des cadences de production, diminution des coûts, et amélioration de la fiabilité et des performances aux hautes fréquences. Les composants pour montage en surface actuellement disponibles sont en mesure de satisfaire 80% des besoins; on prévoit qu'à la fin de la décennie, cette technique sera généralisée pour au moins la moitié des circuits produits.

Circuits intégrés de commande de visualisation et d'attributs

Un jeu de quatre circuits intégrés commande un terminal de visualisation couleur ou monochrome, offrant plusieurs possibilités telles que le choix de caractères à double hauteur et double largeur, la largeur des points programmables, le défilement lent et le mode graphique point par point. La majorité des fonctions du terminal étant contenue dans les circuits intégrés, la réalisation du matériel est grandement simplifiée et il reste surtout à concevoir le logiciel et le "firmware" du système.

La philosophie de conception du microprocesseur 68000

Le 68000 est le microprocesseur 16 bits le plus rapide et le plus puissant et pourtant il est aisé à programmer. L'article décrit les caractéristiques architecturales qui donnent au processeur sa rapidité, sa puissance et sa simplicité de programmation. Les alternatives qui s'offraient à l'équipe de conception sont présentées en vue d'expliquer le choix de l'architecture du 68000.

Amplificateurs de puissance VHF avec circuit d'entrée large bande

Grâce la configuration évoluée de leurs électrodes, fruit de la C.A.O., associée à de nouvelles cavités incorporant un transformateur d'impédance à deux étages de conception spéciale, les tétrodes émettrices VHF YL1610, YL1630 et YL1631 peuvent fonctionner sans accord sur des bandes d'entrée très larges 82 à 110 MHz dans la bande II et 170 à 250 MHz dans la bande III. Ceci facilite l'utilisation des émetteurs, l'entretien et l'accord, et simplifie leurs circuits.

Modem à deux puces pour transfert de données FSK

Fonctionnant à une fréquence porteuse de 5 MHz sur un câble coaxial de 75 Ω dans un réseau de transmission à "jetons", un modem à clé par décalage de fréquence, utilisant des circuits intégrés separés pour l'émission et la réception peut fournir un débit de données comparable à celui des Ethernets. Le contrôle automatique empêche l'occupation de la ligne par un émetteur inactif. La fréquence porteuse peut être adaptée au type de service prévu et aux câbles employés; à une fréquence porteuse de 280 kHz, par exemple, le modem peut fonctionner à 56 kbit/s sur 2,5 km de paire torsadée.

Le BTV60, premier d'une nouvelle génération de commutateurs à grille de contrôle (GTO)

Le BTV60 est le premier composant d'une nouvelle génération GTO. Il est capable de commuter des intensités trois fois plus élevées que les anciens dispositifs. Se caractérisant par une structure bien plus fine de la cathode, cette nouvelle famille doit être fabriquée en technologie planaire plutôt qu'en technologie "mesa" comme les anciens GTO.

Problèmes thermiques associés aux transistors de puissance R.F. à montage par bride

L'impossibilité pratique d'une analyse exacte des flux thermiques est à la source de malentendus sur le montage des transistors de puissance R.F. Des études expérimentales détaillées ont permis d'établir des règles pour un montage thermique efficace, règles qui vont à l'encontre de certaines idées fausses largement répandues. On peut démontrer, par exemple, que le serrage des boulons de fixation à plus de 0,75 Nm augmente la résistance thermique, et que des surfaces de montage rodées sont moins efficaces qu'une mince couche de graisse à base de silicones dissipatrice de chaleur.

Un nouveau décodeur stéréo sur circuit intégré adapté à tous les types de radio

Un nouveau décodeur stéréo PLL intégré, le TEA5580, ne se contente pas d'assurer toutes les fonctions de décodage stéréo de base avec un nombre minimum de périphériques passifs. Il possède en outre une flexibilité d'utilisation suffisante pour convenir à tous les types de radio imaginables, des récepteurs portatifs alimentés par piles aux tuners HiFi fonctionnant sur secteur. D'autres avantages sont: gain interne réglable jusqu'à 20 dB, commande douce par courant continu de la commutation mono/stéréo (séparation des canaux), suppression interne du canal adjacent et du parasitage VWF, compensation d'atténuation du détecteur à fréquence intermédiaire, et niveaux de sortie réglables jusqu'à 900 mV.

Aspects qualitatifs de diodes faible et moyenne puissance pour signaux faibles

L'emploi de techniques de production évoluées et l'application d'un contrôle de qualité strict a permis de donner à nos diodes faible et moyenne puissance pour signaux faibles une qualité initiale élevée, associée à un taux faible de défauts de jeunesse et à une fiabilité élevée de grande durabilité. Deux facteurs contribuent à la qualité élevée de ces composants: leur structure robuste et étanche les rend insensibles à la fatigue thermique, et la passivation des jonctions assure des caractéristiques très stables.

Dispositivos montados en superficie en el montaje de placas de circuito impreso

La aparición de componentes sin terminales que pueden ser soldados directamente a la superficiede una placa de circuito impreso está cambiando la tecnologia del montaje de circuitos: aumenta la tasa de producción, bajan los costes, y mejora la fiabilidad y el funcionamiento a alta frecuencia. Los dispositivos montados en superficie disponibles ahora pueden satisfacer el 80% de los requisitos de los circuitos actuales. A finales de la década, se espera que por los menos la mitad de la placas en producción utilicen predominantamente montaje en superficie.

Circuitos integrados visualizador de video y controlador de atributos

Un conjunto de cuatro circuitos integrados controla un terminal visualizador de video monocromático o de color, que incorpora características tales como opciones de caracter de doble anchura y doble altura, alargamiento de punto, rotación suave, y acceso a gráficos de mapas de bits. Con la mayoria de las funciones del terminal contenidas dentro de los circuitos integrados, la implementación del hardware se simplifica mucho y la tarea mas larga pasa a ser el diseño del software y firmware del sistema.

Filosofia de diseño del 68000

El 68000 es el microprocesador de 16 bits más rápido, de más potencia y fácil de programar. Este artículo describe las características arquitectónicas del 68000 que dan al procesador su velocidad, potencia y simplicidad de programación. Se discuten las alternativas disponibles para el diseño del equipo y se ilustra por qué se ha elegido la arquitectura del 68000.

Amplificadores de potencia de VHF con circuiteria de entrada de banda ancha

Con su última configuración de electrodo diseñado con ayuda de ordenador combinado con las nuevas cavidades que incorporan un transformador de impedancias de dos etapas especialmente diseñado, los tetrodos de transmisión de VHF, YL1610, YL1630 e YL1631 pueden operar, sin sintonía, sobre anchos de banda de entrada excepcionalmente amplios – 28 a 110 MHz en la Banda II y 170 a 250 MHz en la Banda III. Esto facilita la operación del transmisor, mantenimiento y sintonía, y simplifica la circuiteria del transmisor.

Modem de dos circuitos para transferencia de datos FSK

Operando con una frecuencia portadora de 5 MHz sobre un cable coaxial de 75 Ω en una red de paso con testigo, un modem FSK, que utiliza circuitos integrados separados para transmisor y receptor, puede manejar un flujo de datos comparable al Ethernet. Un control Jabber automático evita que un transmisor inactivo atrape la linea. La frecuencia portadora puede adaptarse al tipo de servicio deseado y al cable empleado: por ejemplo, con una frecuencia portadora de 280 kHz, el modem puede operar a 56 kbits/s sobre 2,5 km de par retorcido.

El BTV60 – primero en una nueva generación de GTO's

Una nueva generación de GTO's, encabezada por el BTV60, puede conmutar hasta tres veces la corriente de dispositivos formadores. Los nuevos dispositivos se caracterizan por una estructura de cátodo mucho mas fina, por lo que puede fabricarse en tecnologia planar en vez de la tecnologia mesa de los GTO's formantes.

Aspectos térmicos de transistores de potencia de R.F. montados en bridas

La impractibilidad del análisis exacto del flujo de calor ha conducido a una idea equivocada acerca del montaje de transistores de potencia de R.F. Estudios experimentales detallados conducen ahora a reglas para un montaje térmicamente efectivo que corrige los falsos conceptos generales. Por ejemplo, es claramente demostrable que girando los ejes de montaje más allá de unos 0,75 Nm aumenta la resistencia térmica, y que las superficies de montaje pulidas son menos efectivas que una delgada capa de compuesto radiador.

Nuevo CI decodificador estéreo adecuado a todos los tipos de radio

Un nuevo decodificador estéreo PLL integrado, el TEA5580, no sólo realiza todas las funciones básicas de decodificación estéreo con el mínimo número de periféricos pasivos. Es suficientemente flexible para acomodarse a todos los tipos posibles de radio, desde las portátiles alimentadas por baterias a sintonizadores de Hi-Fi alimentados por la red. Sus características adicionales son: una ganancia interna ajustable de hasta 20 dB, control suave de c.c. de conmutación mono/estéreo (separación de canales), anulación del tono piloto, supresión interna del canal adyacente e interferencias de VHF, compensación progresiva detector/F.I., y niveles de salida que pueden ajustarse hasta 900 mV.

Calidad de los diodos de pequeña señal de media y baja potencia

Este artículo describe como se logra la alta calidad inicial, combinada con una baja mortandad precoz y fiabilidad a largo plazo, de nuestros diodos de pequeña señal de potencia media y baja, utilizando técnicas de producción avanzadas y un procedimiento estricto de control de calidad. Los factores que contribuyen a la alta calidad de estos componentes son: una robusta estructura hermética que es inmune a la fatiga térmica y la pasivación de la unión que da lugar a unas características muy estables.

Authors

Bob Blauschild joined Signetics in 1973 after receiving an MSEE degree from the University of California, Berkeley. Since 1977 he has been directing analog circuit research and is currently Manager of Advanced Product Development for the Linear LSI Division. His group specializes in working with new technologies, including high-speed bipolar, dense CMOS, and combined bipolar high-voltage DMOS processes.

Graham Hine, born 1954 in Cheshire, attended Darwin College, Cambridge, and in 1980 gained his doctorate there in experimental physics with a dissertation on radio astrophysics. The same year he joined Mullard Ltd. at Hazel Grove where, as a member of the development team for discrete power semiconductor devices, he specialized in fast Schottky diodes. In 1983 he moved to Philips Electronic Components and Materials Division in Eindhoven and is now in commercial product management for glass diodes. Graham has previously published in Nature and the Monthly Notice of the Royal Astronomical Society.

Wim van Dooremolen was born in Eindhoven, The Netherlands, in 1937 and joined Philips in 1956 to work on ultra-short-wave transmitting tubes. Since 1965 he has been working in the radio/audio section of the central application laboratory of the Electronic Components and Materials Division, where he is currently engaged in the design and application of bipolar integrated radio circuits.

Michael Klewer was born in Wuppertal, Germany in 1949 and graduated in physics from the University of Munster in 1974. After 5 years with Euratom and the FOM Institute for Atomic and Molecular Physics in Amsterdam, he received a PhD in physics from the Free University of Amsterdam in 1979. In 1982 he joined Philips Electronic Components and Materials Division and is currently marketing manager responsible for building up the VMEbus/68000 product line.

Rich Fabbri was born in Brooklyn, N.Y., in 1945. He gained a BA in physics from Hunter College, New York, in 1966, and an MS in physics from New York University in 1971. Since then he has worked for Schlumberger-Doll in Connecticut, and he was for 5 years a section head at CBS Laboratories. He joined Signetics in 1976, initially as a field applications engineer, and is now Signetics Technical Program Manager for worldwide IBM design activities.

J. G. A. Scholten was born at Eindhoven in 1946 and gained his education in electronic engineering at Eindhoven and Arnhem. After joining Philips in 1966 he worked first in production mechanization and later in transistor development. He is now at the crystal laboratory in Doetinchem, where he is engaged in quartz crystal and crystal oscillator development.

Alex Goldberger gained his BSEE degree at the City College of New York and his MSEE at the Polytechnic Institute of Brooklyn. He has worked in integrated circuits since 1969 and was design manager for the first large-scale integrated circuit for data communications. As applications manager for the microprocessor division of Signetics Corporation, Sunnyvale, California, he was responsible for technical marketing support for microprocessor products. Alex is now with Exel Microelectronics, Inc.

Bart J. M. Vernooij was born in Bennebroek, The Netherlands in 1955. He studied Physics at the Technical University of Delft and after military service joined Philips Electronic Components and Materials Division where he is engaged in the marketing of the 68000 microprocessor family.

Hans Fiedeldij was born in Utrecht, The Netherlands, in 1942, and joined Philips Lighting Division in 1964. Later, in 1970, he moved to the Electronic Components and Materials Division, and since 1979 he has been marketing manager responsible for transmitting tubes.

Arthur Woodworth was born in Manchester in 1945. He took a B.Sc. in electrical Engineering at Salford University in 1968 and later that year joined Mullard, Stockport, where he is now head of the Electrical Development Department responsible for the specification and evaluation of a wide range of rectifiers, thyristors, triacs, and GTOs.

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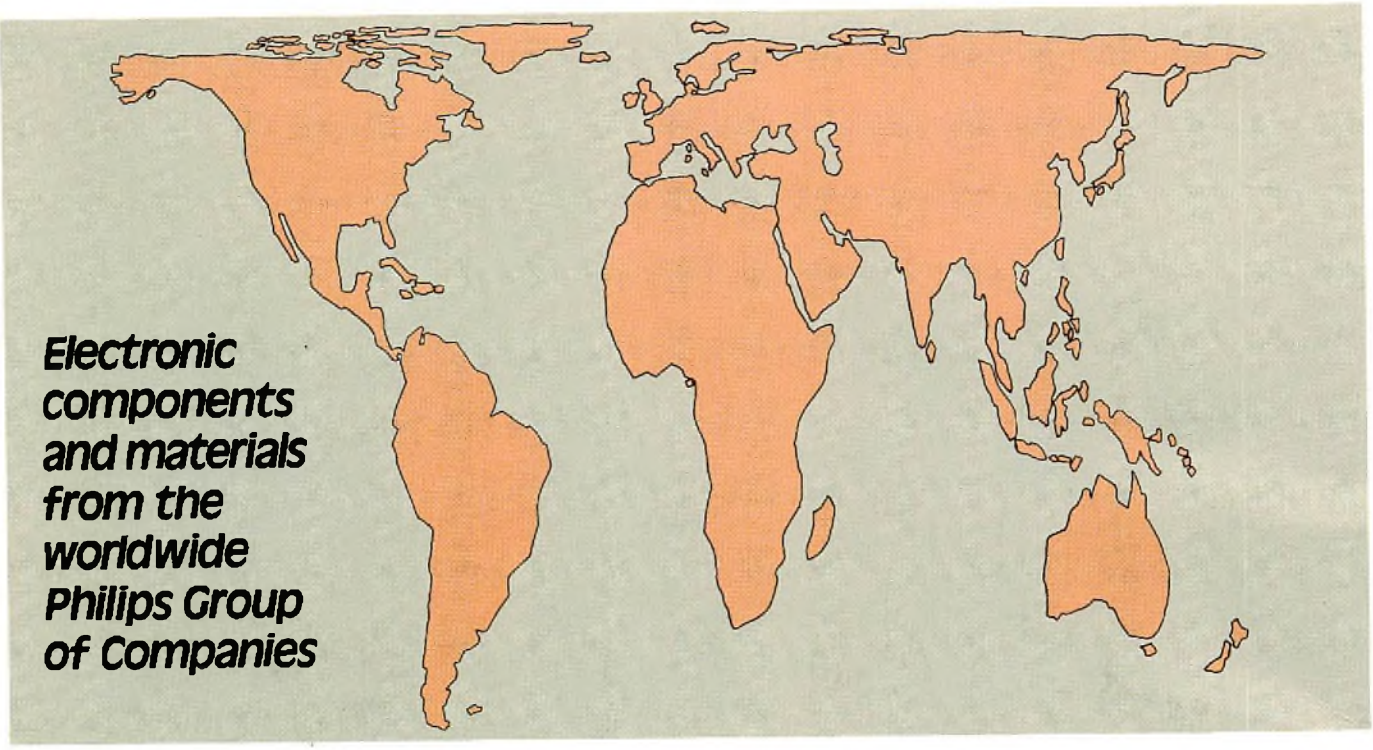

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