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To stay ahead in the fast moving world of CMOS commodity logic, IC manufacturers must constantly surmount new obstacles. The first breakthrough came thirteen years ago with the development of the silicon-gate CMOS process and our own technique for the local oxidation of silicon (LOCOS) which led to the birth of our 6 µm HE4000B family of CMOS logic ICs. Within seven years, technology refinements allowed us to shrink the minimum dimensions of these ICs to 4 µm and clear the 35 ns propagation delay hurdle. But the steeplechase hadn't yet run its course. We tightened the layout rules, thinned the oxide in the gate region and built a 3 µm gate to safely clear the 9 ns fence with HCMOS in 1985. Since then, we've taken advantage of the latest technological advances to develop our new Advanced CMOS Logic (ACL) family. With a 1 µm effective gate length and an incredible 3 ns propagation delay, these ACL throughbreds are all set to pass the winning post at speeds up to 150 MHz.

Contents

ACL...Advanced CMOS Logic that lengthens the stride of low-power systems

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There's little doubt that CMOS will unseat bipolar technology as the mainstay of integrated commodity logic. Advancing technology is rapidly eliminating the old trade-offs between speed and power dissipation (Fig.1), and problems peculiar to CMOS such as latch-up and ESD sensitivity have already been solved. However, until now, CMOS logic ICs haven't been able to match the high speed and the high current output of TTL technologies which is essential for operation in the bus or transmission-line environment of the fastest logic systems.

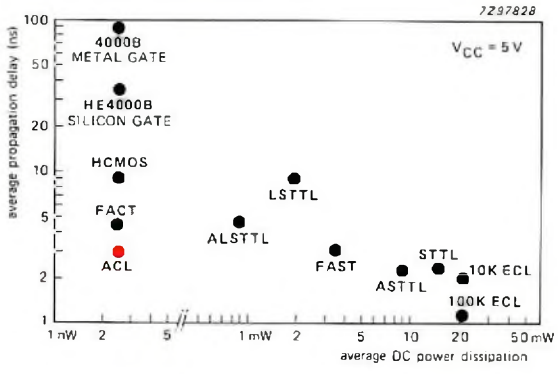


Fig.1 The logic family speed/power spectrum

The introduction of the Advanced CMOS Logic (ACL) family of ICs overcomes this hurdle. ACL is fabricated in a 1 μm twin-well CMOS process with recessed local oxidation and a titanium disilicide (salicide) layer on the source/drain and gate areas to reduce the contact and interconnect resistance. This, together with oxide gate sidewall spacers for reduced capacitance, leads to increased drive and speed that equals that of the fastest bipolar TTL logic. With an average propagation delay of 3 ns (150 MHz operation) and 24 mA output sink/source capability, ACL supplements the HE4000B and HCMOS logic IC ranges to allow designers to implement the outstanding CMOS benefits of wide and symmetrical noise margins, wide operating temperature range, high reliability, and reduced power dissipation across the whole speed spectrum of logic circuitry.

The inevitable fast edges associated with the exceptionally high speed of ACL required one final hurdle to be tackled: the problem of bonding-wire and leadframe inductance causing ground bounce, especially when multiple outputs of one IC are simultaneously switched. This problem, which also hinders fast switching bipolar logic, reduces system noise margins, causes loss of stored data and reduces system speed. It is solved for ACL by the simple expedient of discarding the traditional corner supply pinning arrangement and simultaneously adopting a flow-through architecture. ACL has multiple supply pins at the centre of each side of the package (where the internal inductance is minimum), all the input pins are on one side of the package, all the output pins are on the other and control pins are at the corners. Although this solution means that ACL isn't pin-compatible with its TTL and HCMOS counterparts, it has the major advantages of improving system reliability, simplifying pcb design and reducing board area.

ACL ICs are fully-buffered, have outputs that are both CMOS and TTL compatible, and have a standard operating temperature range of $-40\,^{\circ}C$ to $+85\,^{\circ}C$. A wider temperature range of $-55\,^{\circ}C$ to $+125\,^{\circ}C$ is available as an option. They're all available in two versions:

- 74AC types with CMOS-compatible input switching levels (typically $V_{CC}/2$) and a supply voltage range of 2 V to 5,5 V for all-CMOS systems
- 74ACT types with TTL-compatible input switching levels (typically 1,5 V) and a supply voltage range of 5 V ± 10% for interfacing with TTL systems.

The type number nomenclature of these centre supply pin ACL ICs follows that of their bipolar counterparts but consists of a 3-digit function code preceded by the centre supply pin designator 11. For example, the type number of hex inverter '04 with CMOS-compatible input switching levels is 74AC11004.

Since the low power dissipation of ACL ICs makes them ideal for circuitry on densely packed boards in small enclosures, they must be suitable for use with surface mounting technology, which is being increasingly used for automated assembly of electronic equipment to achieve significant reduction of its size and weight. Production quantities of all our ACL ICs are available in DIL packages and in SO (small outlines) packages. The dimensions of the latter were originally developed by us and now form the basis of JEDEC standard publication 95 (also published in IEC standard document 191-2, family A76).

Finally, ACL ICs are completely latch-up free, and have complete protection against electrostatic discharge (ESD) at their inputs and outputs.

ACL FEATURES

ACL has all the well-known attributes of our HCMOS family combined with faster operation and increased drive capability. The main outstanding features of the family are:

- A comprehensive type range from simple gates to shift registers and counters
- Available with specifications valid for an operating temperature range of −40 °C to +85 °C, with options for −55 °C to +125 °C operating temperature range and for military processing, both MIL-STD-883 and MIL-M-38510
- All types available in 74AC versions (CMOS input switching levels) and 74ACT versions (TTL input switching levels
- The input switching threshold level is subject to a variation of only ±60 mV over the entire temperature range. Much less than the ±300 mV specified for bipolar logic
- All types available in SO (small outline) and DIL packages
- Completely latch-up free and guaranteed ESD protection against positive and negative transients up to 2 kV (human body model) at all inputs and outputs
- Low power dissipation. Only a few nW when quiescent, rising to a mere 1,2 mW at 1 MHz
- Symmetrical 24 mA sink/source current for equal output rise and fall times. For incident wave switching, 50 Ω and 75 Ω loads are permissible
- More than three times the noise immunity of TTL logic families
- Wide supply voltage range; 2 V to 5,5 V for 74AC ICs and 5 V ± 10% for 74ACT ICs
- Average propagation delay for the 74AC11000 gate is 3 ns for either HIGH-to-LOW or LOW-to-HIGH transitions. Typical operating frequency limit at 25 °C is 150 MHz
- Centre supply pins to minimize ground and supply rail glitches during simultaneous switching of multiple outputs. A flow-through architecture to simplify board layout
- Outputs have edge control circuitry to reduce the effective dv/dt, thereby further reducing switching noise
- Inputs have a small d.c. hysteresis to render them less susceptible to slow input edges. Furthermore, clock inputs have additional proprietary dynamic hysteresis which doesn't incur a speed trade-off
- Alternate-sourced by TI.

A CLOSER LOOK AT ACL

Supply voltage

ACL ICs with the type number prefix 74AC operate from a supply voltage range of 3 V to 5,5 V, meeting the new industry JEDEC standard No. 8 which specifies 3,3 V ± 0,3 V for regulated power supply systems. The internal logic of 74AC ICs will, however, maintain its state with a supply voltage as low as 2 V; this facilitates the use of a lithium battery as a back-up supply. ACL ICs with the type number prefix 74ACT operate from a supply voltage of 5 V ± 10% which is consistent with the supply voltage for the TTL logic circuits with which they are intended to interface.

Power dissipation

One of the most important requirements for any logic system is low power dissipation because it minimises system cost, allows higher packing density and results in improved reliability because of lower operating temperature.

The typical quiescent power dissipation of an ACL gate (2,5 nW) is more than six orders of magnitude less than that of a bipolar TTL gate. This is because, unlike TTL, CMOS logic dissipates only negligible power due to leakage currents when it isn't switching. The maximum quiescent current per ACL package for SSI (40 μA) is less than 1% of that of an equivalent TTL package with 50% of the gates in the HIGH state. As shown in Fig.2, the typical dynamic power dissipation of ACL gates is also very low. With a 50 pF load and a 5 V supply, it is 0,18 mW at 100 kHz rising to only

180 mW at 100 MHz, two-thirds of which is dissipated in the load capacitance. This is considerably lower than that of the fastest TTL logic, particularly at lower frequencies where its high quiescent current predominates over its dynamic current.

The power merging frequency where ACL and TTL dissipate the same power is about 10 MHz for a gate, and more than 20 MHz for a flip-flop. However, in a practical logic system, only a few of the logic elements operate at the maximum clock frequency, so the average operating frequency is much lower, giving ACL an even greater advantage over advanced TTL. Figure 3 shows that, in a more complex system comprising a divider chain of six flip-flops with their Q outputs loaded with 50 pF, the power merging frequency no longer exists. At 30 MHz, ACL still dissipates only one third of the equivalent advanced TTL dissipation. If the divider chain is lengthened, or the system complexity increased, the power-saving increases yet further.

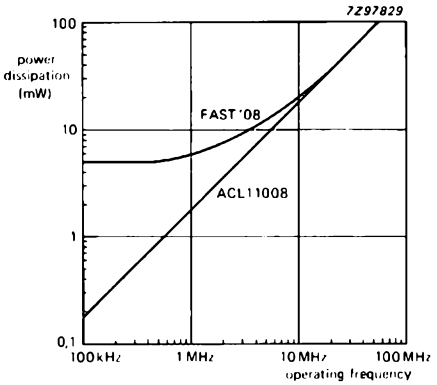


Fig.2 The power dissipation of an ACL quad 2-input AND gate with all outputs switching and with $V_{CC} = 5$ V, $C_L = 50$ pF and $T = 25$ °C is considerably lower than that of the fastest TTL circuits

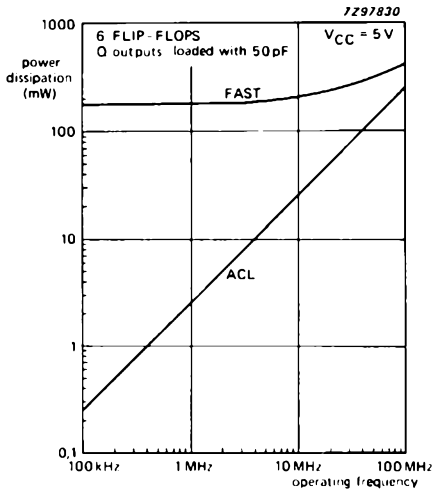


Fig.3 A simulated logic system shows the distinct power saving of ACL at all frequencies

Propagation delay

The on-chip propagation delay for a single ACL gate is only 0,5 ns. From input pin to output pin of a 74AC11000 gate with a 50 pF load it is 3 ns typical for HIGH-to-LOW or LOW-to-HIGH transitions. Moreover, propagation delays are specified over the entire operating temperature range and at two system supply voltages (3,3 V ± 0,3 V and 5 V ± 0,5 V). For user convenience, the minimum propagation delay is also specified. The specified limits are comparable to those for the fastest TTL logic families. Due to the high drive current capability of the low-impedance ACL outputs, propagation delay variation as a function of load capacitance is much less than that of most other logic ICs. Moreover, unlike the fastest TTL circuits, all ACL ICs have standardized output buffers which allow symmetrical output current sinking and sourcing to obtain equal rise and fall times (3 ns). This simplifies design and results in optimum speed and a.c. performance. The typical switching frequency limit for ACL is 150 MHz at 25 °C and is specified with a 50% duty factor so, unlike with TTL, it's not necessary to tweak the pulse widths.

Noise immunity

The input switching levels are between 30% and 70% of V_{CC} for 74AC ICs and between 0,8 V and 2 V for 74ACT ICs. Output swing for both 74AC and 74ACT ICs is from 0,1 V to $V_{CC} - 0,1$ V with a load of 50 μA (fifty CMOS inputs) and from 0,5 V to $V_{CC} - 0,8$ V with a load of ±24 mA. For 74AC ICs driving fifty CMOS inputs, the LOW- and HIGH-level noise immunity with a 4,5 V supply is therefore 28% of V_{CC}. The LOW-level noise immunity of 74ACT ICs with a maximum load of 24 mA matches that of TTL at operating temperatures up to 125 °C and exceeds it at 70 °C. The HIGH level noise immunity of 74ACT ICs is three times that of TTL. ACL ICs are therefore ideal for use in electrically noisy environments such as those encountered in industry, telephony and automotive applications.

Drive capability

ACL ICs have the low input current (only 1 μA max. in the HIGH or LOW state) which is a characteristic of CMOS technology and is essentially zero compared with the input current of TTL technologies. They can, however, sink/source output current of up to 24 mA over the entire operating temperature range whilst still matching or exceeding the noise immunity of TTL logic. The fan-out when driving other CMOS circuits is therefore only limited by load capacitance considerations and not by the available drive power.

In the fastest logic systems, ACL ICs will probably be working in a transmission line environment where their low output resistance (20 Ω max.) is of particular significance for reducing a system's susceptibility to crosstalk and

induced noise, and for guaranteeing incident wave switching to optimize system speed. For example, to guarantee incident wave switching over the standard temperature range, the dynamic output current sink/source capability of ACL with a 5,5 V supply is 75 mA at V_O = 1,65 V (LOW) or 3,85 V (HIGH) which allows terminated lines with a characteristic impedance down to 50 Ω to be driven. Over the optional extended temperature range, the dynamic output current sink/source capability is 50 mA at the same output voltage levels, so lines with a characteristic impedance of down to 75 Ω can be driven.

ESD protection

The ACL input network shown in Fig.4(a) incorporates reverse-biased diodes between the positive rail, input pins and ground for clamping the input voltage to provide ESD protection and limit the amplitude of ringing. These diodes have typical forward voltage drops of 0,9 V and reverse breakdown voltages of 17 V. ACL inputs can withstand positive and negative ESD transients of up to 2 kV from the 'human body model' (1,5 kΩ, 100 pF, 13 ns pulse rise time) shown in Fig.4(b). This meets MIL-STD-883B, Method 3015.

Large inherent diodes formed by the drain surfaces of ACL output transistors allow positive and negative ESD up to 2 kV to be sustained without damage to outputs.

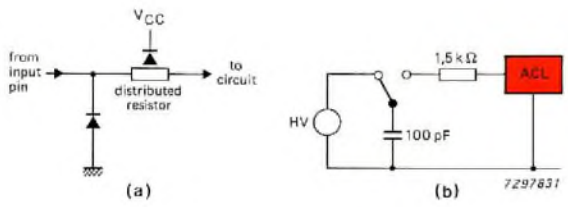


Fig.4 The inputs of ACL ICs are fully protecetd against ESD
(a) ACL input protection network
(b) 'human body model' test arrangement

ACL is latch-up free

Latch-up can be reduced by the use of extensive guard rings, but at the expense of increased chip area. During fabrication of our ACL ICs, a high-resistivity p^- epitaxial layer is grown on a very low-resistivity p^+ substrate. This diverts lateral current flow through the p^+ layer, thereby preventing parasitic bipolar transistors from being forward biased. This, plus proprietary layout rules and process parameters that even further reduce the gain of the parasitic bipolar transistors, means that ACL ICs are completely latch-up free.

ACL ICs have been subjected to the latch-up tests described by JEDEC with ratings far exceeding the maximum limits. In no case did latch-up occur. For example, inputs/outputs can withstand currents as high as 100 mA d.c. or 650 mA pulsed.

When testing ACL ICs for latch-up initiated by supply overvoltage, the voltage required to cause V_{CC} breakdown far exceeds the maximum V_{CC} rating (6 V). ACL ICs have been subjected to tests to discover the conditions for V_{CC} breakdown and to determine whether or not the supply voltage would snap-back to more than 6 V. The results of the characterization all concur with the design goals and reveal that a supply voltage of at least 18 V and a current of several tens of milliamps is required to cause the first snap-back (secondary breakdown). Since the snap-back voltage was never less than 10 V, ACL ICs are SCR (Silicon Controlled Rectifier) latch-up free. Since other CMOS logic with a 5 V supply goes into SCR latch-up with a snap-back voltage of only 2 V, it remains latched-up until the supply is switched off. It should be noted that, during latch-up characterization, there is a possibility that the IC will become severely overheated. A close eye should therefore be kept on the supply voltage/current product.

54/74ACT – FOR INTERFACING WITH TTL

Since the entire type range of ACL ICs is also available in 74ACT versions, it is easy to drive ACL from ALSTTL, ASTTL or FAST-TTL outputs without using power consuming pull-up resistors at the bipolar logic outputs to maintain adequate noise margins.

All the advantages previously described for 74AC ICs naturally also apply to the 74ACT versions. The only differences are that the propagation delay is slightly longer and the nominal supply voltage and input structure of the 74ACT types have been modified to match TTL characteristics. The modified input structure not only adapts to TTL input switching levels, but also reduces power consumption when a minimum TTL HIGH output level of 2,4 V is applied to a 74ACT input. For TTL compatibility, the supply voltage for 74ACT ICs is 5 V ± 10%. Unlike 74AC ICs which have an input switching threshold of 50% of V_{CC}, the nominal input switching threshold of 74ACT types is 1,5 V, and the inputs switch between the same levels as TTL (V_{ILmax} = 0,8 V. H_{IHmin} = 2 V). The temperature sensitivity of the input switching threshold, however, is only ±60 mV over the entire temperature range, so the noise margins also remain very stable over the temperature range. With a 4,5 V supply and an output current of 50 μA (50 ACL inputs), a 74ACT output swings between 0,1 V and V_{CC} – 0,1 V. With the maximum output current of 24 mA, it swings between 0,5 V and V_{CC} – 0,8 V. So, for a 74ACT IC with a 4,5 V supply driving fifty ACL inputs, the noise margins are 53% of V_{CC} (HIGH) and 15,5% of V_{CC} (LOW). For a similar TTL IC, they would be only 15% of V_{CC} (HIGH) and 8% of V_{CC} (LOW). Even when a 74ACT IC is delivering 24 mA, the noise margins are 42% of V_{CC} (HIGH) and 6,6% of V_{CC} (LOW).

Safe driving – interface requirements

from \ to	HC/AC 5 V supply	HCT/ACT 5 V supply	HE4000B 5 V supply	HE4000B 5 V supply	TTL* 5 V supply	ECL 10K
HC/AC 5V supply	direct	direct	direct	4104	direct	10124
HCT/ACT 5 V supply	direct	direct	direct	4104	direct	10124
HE4000B 5 V supply	direct	direct	direct	4104	direct	10124
HE4000B 6-15 V supply	4049 or 4050	4049 or 4050	4049 or 4050	direct	4049 or 4050	transistor
TTL* 5 V supply	pull-up resistor	direct	pull-up resistor	4104	direct	10124
ECL 10K	10125	10125	10125	transistor	10124	direct

* includes LS, S, STD, FAST, ALS and AS.

direct = without interface components
4104 = LOW to HIGH level shifter from the HE4000B family
10124 = TTL to ECL translator from the ECL 10K and 100K families
10125 = ECL to TTL translator from the ECL 10K and 100K families
4049/4050 = HIGH and LOW level shifters from the HE4000B family.

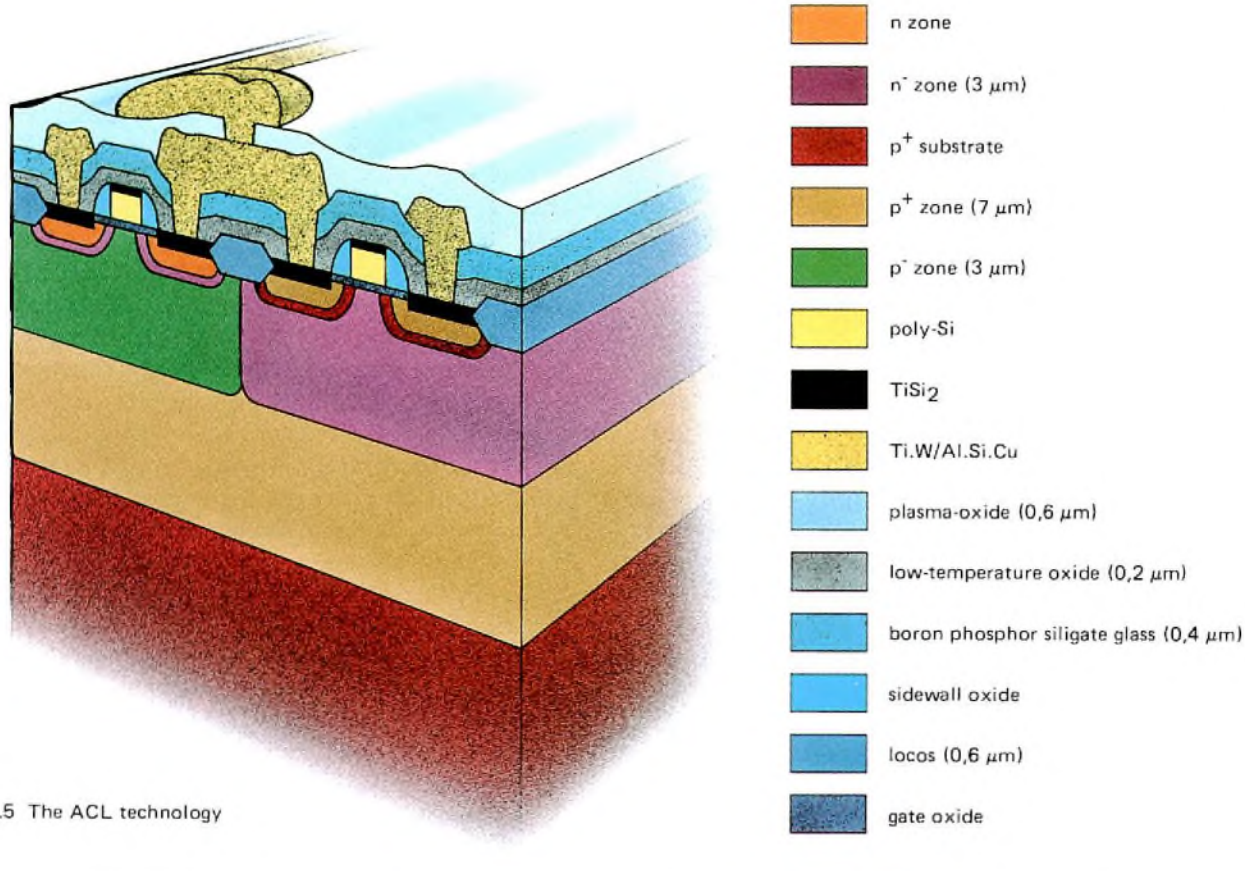


Fig.5 The ACL technology

ADVANCED TECHNOLOGY MAKES IT POSSIBLE

The 9-mask ACL construction shown in Fig.5 is a result of a continuing development programme to enhance the proven polycrystalline silicon (polysilicon) gate CMOS process. It incorporates several technological innovations for increasing packing density, speed, and reliability.

The twin-well p^-/n^- structure and double-layer metal interconnects allow a high packing density which will also facilitate development of future MSI/LSI circuitry.

Three main features contribute to the exceptionally high speed of ACL. Firstly the effective length of the transistor gate is only 1 μm, resulting in an on-chip propagation delay of only 0,5 ns. Secondly, there is a self-aligned titanium disilicide (salicide) layer on the source/drain and gate to reduce their series resistances and the resistance between the contacts and junctions. Thirdly, gate sidewall spacers minimize the gate/source and gate/drain capacitances.

Electromigration is reduced by using copper-doped aluminium interconnects on a tungsten layer. Furthermore, a p^- epitaxial layer on a low-resistivity p^+ substrate results in a high degree of latch-up immunity.

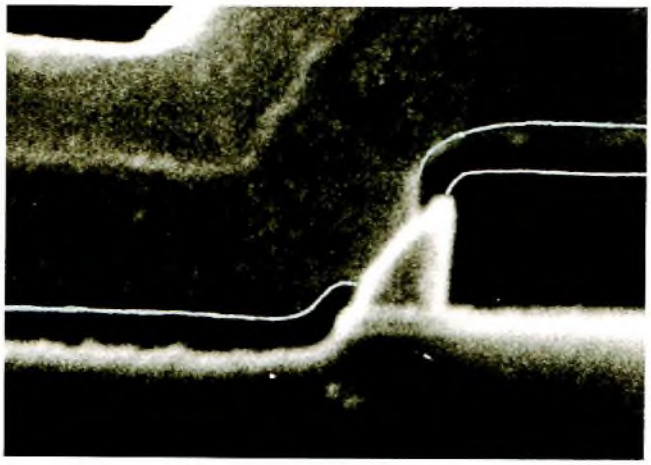


Fig.6 SEM photograph of a vertical cross-section through part of a salicided ACL transistor. Advanced processing using a salicide technique and gate spacers results in minimal dimensions and excellent electrical properties

NEW PINOUTS FOR ACL ADD RELIABILITY AND SIMPLIFY DESIGN

The fast rise and fall times associated with high speed logic can lead to noise problems when one or more outputs of an IC switch from one logic state to another. As shown in Fig.7, this discharges the load capacitances through the inductance of the internal supply connections, thereby causing a transient that lifts up the on-chip ground and reduces the effective supply voltage to the chip. The problems are particularly severe in CMOS logic because the outputs can switch almost from one supply rail to the other. Referred to as simultaneous switching noise, the transient appears on any unswitched output(s) of the switching IC and has a peak amplitude directly proportional to the number of outputs simultaneously switched and to the inductance of the internal IC supply connections. This lifting-up of the chip ground and consequent reduction of supply voltage degrades system reliability by reducing noise margins, reducing speed, causing loss of standard data and causing false switching.

It is a common misconception that supply decoupling capacitors located adjacent to each IC will eliminate simultaneous output switching transients. The output-capacitance discharge noise is related to the absolute inductance of the supply connection between the chip in the IC and the external supply/groundplane. Since multilayer boards provide excellent supply/groundplanes, improvement can only be achieved by manufacturers taking measures to reduce the supply/ground lead inductance within the IC. Supply line decoupling should be similar to that used for TTL systems operating at comparable speed.

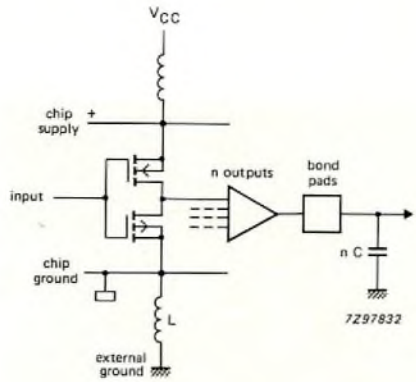


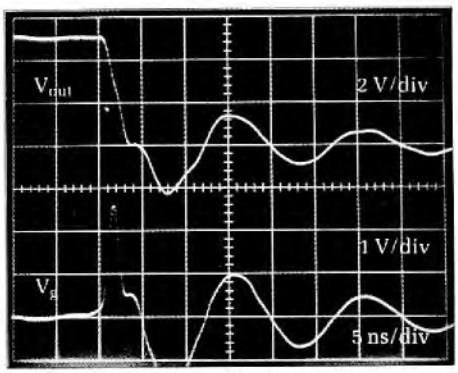
Fig.7 Equivalent circuit of a CMOS output. When outputs switch from HIGH to LOW, nC discharges through L causing a voltage spike with a peak amplitude of L di/dt

In the early days of integrated logic, manufacturers were forced to position IC supply pins at diagonally opposite corners of the package because of layout restrictions imposed by single-sided print-boards which were in universal use at that time. However, in today's world of double-sided and multilayer print-boards and much faster logic, placing the supply pins at diagonally opposite corners of the package where the long bonding wires and lead frame segments have the maximum inductance can no longer be considered to be good engineering practice. It's the worst possible positioning from the point of view of simultaneous switching noise. So, for ACL ICs, the GND and V_{CC} pins are relocated in the middle of opposite sides of the package where their inductance is minimum. ACL ICs with multiple outputs that can switch simultaneously have multiple supply pins to reduce their inductance yet further.

All ICs with one or two outputs have single GND and V_{CC} pins; 16-pin ICs with 3 or 4 outputs that can switch simultaneously have two GND pins and two V_{CC} pins; 20, 24 and 28-pin ICs with 3 or more outputs that can switch simultaneously have four GND pins and two V_{CC} pins.

As shown in Fig.8, tests performed on an octal ACL IC with four centre supply pins reveal that, when seven of the outputs are simultaneously switched from HIGH to LOW, the amplitude of simultaneously switched noise on the eighth (LOW) output stays well below the maximum LOW input switching level and is only about 30% of that for a comparable IC with corner GND and V_{CC} pins. Consequently, the effective reduction of supply voltage to the chip is very small, so signal integrity is maintained and loss of speed is minimal.

The positioning of the I/O and control pinning of ACL ICs has also been rationalized as shown in Fig.9. All the inputs surround the V_{CC} pin(s) on the side of the package with the highest pin numbers, and all the outputs surround the GND pin(s) on the other side of the package. The control pins are strategically placed at the corners of the package. This ACL flow-through architecture, which is used for all ACL ICs in both DIL and SO packages, reduces the total inductance of outputs (bonding wire plus lead frame and output pin) between the chip and the printed wiring tracks. It also facilitates positioning of decoupling components, simplifies pcb design and fault-finding, and decreases the area of print-board required.



(a) IC with corner supply pins.

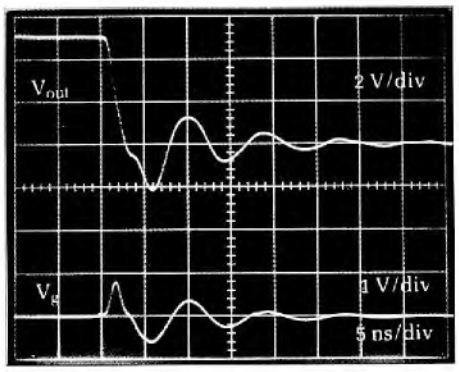


Fig.8 Ground bounce comparison when 7 outputs of octal 74AC240 and 74AC11240 ICs in DIL packages are simultaneously switched (V_{CC} = 5 V, T_{amb} = 25 °C). The bounce is measured on the 8th output which is held LOW. Note that the frequency of the ringing in the upper picture is lower than that in the lower picture due to the higher total inductance of the ground lead

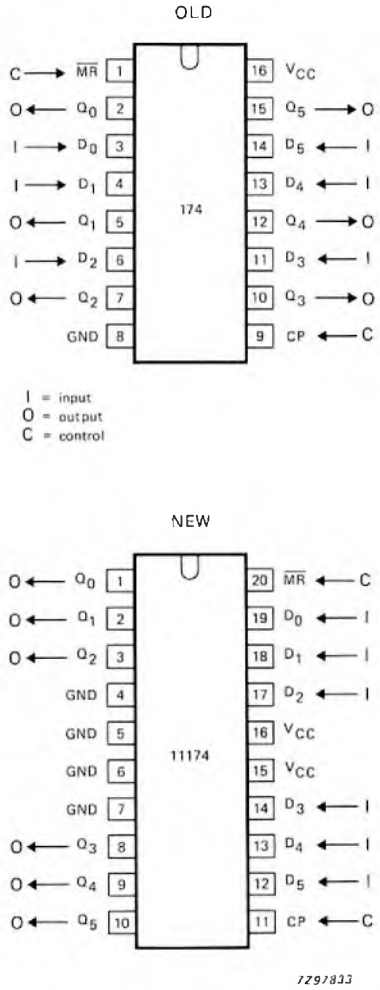


Fig.9 Flow-through architecture of 74AC11174

ACL PACKAGES

All ACL ICs are available in SO (small outline) packages as well as in DIL, so you can use surface-mounting techniques to increase pcb packing density. ACL ICs with 14 or 16 pins are in the narrower 150 mil (3,8 mm) SO packages packed on 16 mm tape on two sizes of reels: 7 in. (1000 ICs) or 13 in. (2500 ICs) diameter. ACL ICs with 20, 24 or 28 pins are in 300 mil (7,6 mm) wide SO packages packed on 24 mm tape with 500 ICs on a 7 in. reel, and 1000 ICs on a 13 in. reel. The body width of all the DIL packages (14 to 28 pins) is 300 mil (7,6 mm).

Absolute maximum ratings

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

symbol	parameter	min.	max.	unit	conditions
V_{CC}	d.c. supply voltage	−0,5	+6	V	
$\pm I_{IK}$	d.c. input diode current		20	mA	for $V_I < 0$ V or $V_I > V_{CC}$
or V_I	d.c. input voltage	−0,5	V_{CC} + 0,5	V	
$\pm I_{OK}$	d.c. output diode current		50	mA	for $V_O < 0$ V or $V_O > V_{CC}$
or V_O	d.c. output voltage	−0,5	V_{CC} + 0,5	V	
$\pm I_O$	d.c. output source on sink current		50	mA	for −0,5 V < V_O < V_{CC} + 0,5 V
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				
	plastic DIL		500	mW	above +70 °C: derate linearly by 12 mW/K
	plastic mini-pack (SO)		400	mW	above +70 °C: derate linearly by 6 mW/K

Note

1. The absolute maximum V_{CC}/GND current is the sum of the maximum rated active HIGH (I_{OH}) or LOW (I_{OL}) output currents as specified in the appropriate DC characteristics table. Its absolute maximum value is at least 100 mA.

Recommended operating conditions for 74AC/ACT

symbol	parameter	74AC			74ACT			unit	conditions
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	d.c. supply voltage (note 1)	3,0	5,0	5,5	4,5	5,0	5,5	V	
V_{IH}	HIGH level input voltage	2,1							V_{CC} = 3 V
		3,15			2,0			V	V_{CC} = 4,5 V
		3,85			2,0				V_{CC} = 5,5 V
V_{IL}	LOW level input voltage			0,9					V_{CC} = 3 V
				1,35			0,8	V	V_{CC} = 4,5 V
				1,65			0,8		V_{CC} = 5,5 V
V_I	d.c. input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	d.c. output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	

Note

1. For battery back-up a 2 V data retention supply is allowed. This implies that a device output will maintain a previously established valid logic state. No parameters or switching characteristics are specified at V_{CC} less than 3 V.

DC characteristics for 74AC

Voltages are referenced to GND (ground = 0 V)

symbol	parameter	T_{amb} (°C)					unit	test conditions		
		+25			−40 to +85			V_{CC} V	V_I	other
		min.	typ.	max.	min.	max.				
V_{OH}	HIGH level output voltage	2,9			2,9		V	3,0	V_{IH} or V_{IL}	$-I_O$ = 50 μA
		4,4			4,4			4,5		$-I_O$ = 50 μA
		5,4			5,4			5,5		$-I_O$ = 50 μA
		2,58			2,48		V	3,0	V_{IH} or V_{IL}	$-I_O$ = 4 mA
		3,94			3,8			4,5		$-I_O$ = 24 mA
		4,94			4,8					$-I_O$ = 24 mA
V_{OH}	HIGH level output drive (note 1)				3,85		V	5,5		$-I_O$ = 75 mA
V_{OL}	LOW level output voltage			0,1		0,1	V	3,0	V_{IH} or V_{IL}	I_O = 50 μA
				0,1		0,1		4,5		I_O = 50 μA
				0,1		0,1		5,5		I_O = 50 μA
				0,36		0,44	V	3,0	V_{IH} or V_{OL}	I_O = 12 mA
				0,36		0,44		4,5		I_O = 24 mA
				0,36		0,44		5,5		I_O = 24 mA
V_{OL}	LOW level output drive (note 1)					1,65	V	5,5		I_O = 75 mA
$\pm I_I$	input leakage current			0,1		1,0	μA	5,5	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current			0,5		5,0	μA	5,5	V_{IH} or V_{IL}	V_O = V_{CC} or GND
I_{CC}	quiescent supply current									
	SSI			4		40	μA	5,5	V_{CC} or GND	I_O = 0
	MSI			8		80	μA	5,5		I_O = 0

Note

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second. This parameter has been introduced to meet the requirements of incident wave switching of 50 Ω loads.

DC characteristics for 74ACT

Voltages are referenced to GND (ground = 0 V)

symbol	parameter	T_{amb} (°C)					unit	test conditions		
		+25			−40 to +85			V_{CC} V	V_I	other
		min.	typ.	max.	min.	max.				
V_{OH}	HIGH level output voltage	4,4			4,4		V	4,5	V_{IH} or V_{IL}	$-I_O$ = 50 μA
		3,94			3,8		V	4,5		$-I_O$ = 24 mA
V_{OH}	HIGH level output drive (note 1)				3,85		V	5,5	V_{IH} or V_{IL}	$-I_O$ = 75 mA
V_{OL}	LOW level output voltage			0,1		0,1	V	4,5	V_{IH} or V_{IL}	I_O = 50 μA
				0,36		0,44	V	4,5		I_O = 24 mA
V_{OL}	LOW level output drive (note 1)					1,65	V	5,5	V_{IH} or V_{IL}	I_O = 75 mA
$\pm I_I$	input leakage current			0,1		1,0	μA	5,5	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current			0,5		5,0	μA	5,5	V_{IH} or V_{IL}	V_O = V_{CC} or GND
I_{CC}	quiescent supply current									
	SSI			4,0		40,0	μA	5,5	V_{CC} or GND	I_O = 0
	MSI			8,0		80,0	μA	5,5		I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for a unit load coefficient of 1 (note 2)		tbd*	tbd		tbd		4,5 to 5,5	V_{CC} or GND	I_O = 0

Notes

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second. This parameter has been introduced to meet the requirements of incident wave switching of 50 Ω loads.
2. To determine ΔI_{CC} per IC, multiply this value by the unit load coefficient given in the individual data sheets.

* to be determined.

Microcontroller eases I/O processing burden

S. BALIGA, G. GOODHUE and J. JENKINS

High-speed control applications are characterized by the need to test and perform operations on system inputs that are not necessarily in a fixed format or a given length. Typical system requirements are testing one or more flags on a polled or interrupt-driven basis, setting or clearing of subfields within a byte boundary, transferring large amounts of data in a short time and controlling peripheral devices. Concurrent with these operations is the need for predictable real-time response, accurate and tight timing loops, fast conditional branching and basic computational ability. These attributes must be performed at speeds that may be beyond the operating ranges of conventional microcontrollers.

The 8X401 microcontroller (Fig.1), which uses the Harvard architecture, allows pipelining address generation and instruction fetching with parallel instruction decoding and execution. This concurrency results in consecutive read-modify-write cycles, using either external or on-chip memory as either source or destination. The result is executed in a minimum of 150 ns.

The 8X401 is a monolithic CPU implemented in Emitter-Coupled and Emitter-Follower Logic (ECL and EFL). It controls a series of peripheral devices attached to it by means of a standard 8-bit I/O bus. The 8X401 can be integrated into most support systems using the 8X300 and 8X400 family support devices.

The 8X401 has a fixed instruction set with full on-chip decoding. The user is thus spared from the details of writing or understanding microcode, as in bit-slice microcontrollers. It has 32 instructions (Table 1), which besides such general arithmetic/logic operations as ADD and XOR, includes a variety of conditional jumps and returns.

All instructions are 20 bits long, and instruction memory is 8 Kwords deep. Arithmetic/logic operations may be performed on 1 bit to 8 bits of the operand data subfield. Thus, a subfield (from a data byte) can be selected, an operation performed on it and the result written back to the source byte without disturbing the other bits. To expedite such operations, the 8X401 has an 8-bit ALU with full rotate/merge capabilities. A selectable wrap-around carry is present, allowing multiple byte additions. When a data byte represents the control signals to a peripheral, the 8X401's subfield manipulation ability obviates the need to read the entire byte back to the destination field.

The 8X401 has an independent address section with an independent 13-bit address arithmetic unit and a four-level push-down stack. The chip has status flags (Carry, ALU Not Zero, User Programmable Status Bit and Interrupt Receivable) pinned out as well as register addressable. A Status Input pin is provided which is sampled every cycle and can be used as a serial input, simplifying interprocessor communications.

For parallel transacting, three bank-select signals are provided, acting as ninth address bits when accessing data memory. These can switch between the input and the output phases of the same instruction to avoid addressing data memory when executing read-modify-write cycles on external memory. Only one of these signals is active during a peripheral read cycle, but one or two may be active during a write cycle, allowing data to be simultaneously written to two different addresses in external memory – particularly useful during initialization. The information conveyed by the 8X401 I/O interface is sufficient to allow 8X400 and 8X300 family peripherals to be attached

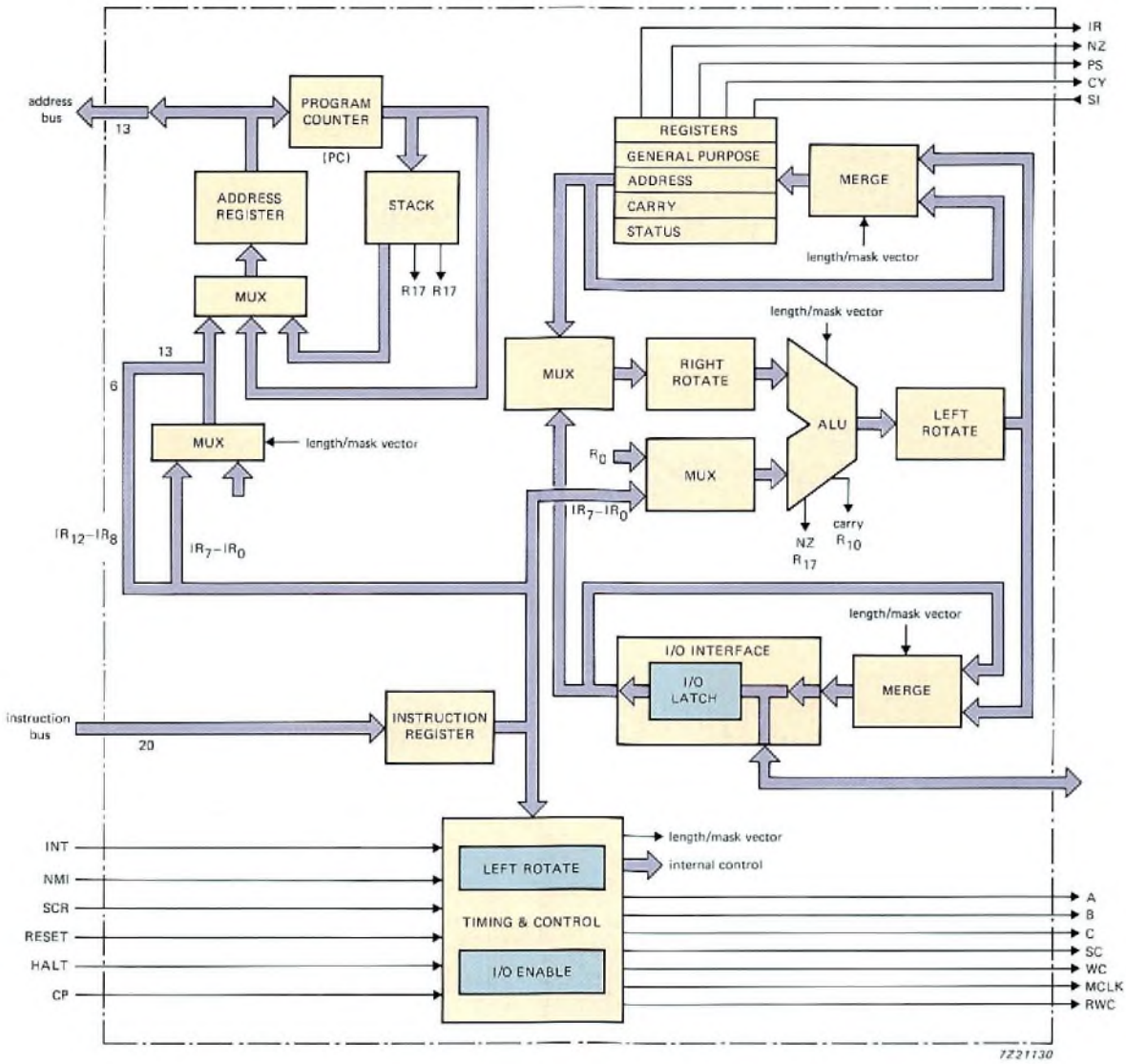


Fig.1 The 8X401 microcontroller uses Harvard architecture and allows pipelining address generation and instruction fetching with parallel instruction decoding and execution

directly to the 8X401 with no decoding or multiplexing/buffering. High-speed, high-throughput systems with minimal chip counts can then be configured with the 8X401 microcontroller.

To complement the 8X401 and to provide compatible interface functions, both the 8X470 I/O port and the 8X450 256-byte RAM fit directly on the 8X401 DA bus. The 8X470 I/O port may have each bit independently fuse programmed as a driver, receiver or latch (from either side) and may supply a status bit to the 8X401 on any specifically programmed bit. This feature, called multiport polling, allows clusters of 8X470s to make up a composite virtual status register.

The 8X450 is a high-speed static RAM which may be viewed as a register array extension, data buffer or general scratch pad. Two addressing modes allow direct 8X401 interfacing whereas another mode allows it to be used easily with other standard microcontrollers and microprocessors.

When not using 8X401 family peripherals, the 8X401 microcontroller has an input signal termed Slow Clock Request (SCR) which doubles the execution time of one instruction to transact with slower peripherals. Thus, the entire I/O family of 8X305 and 8X300 microcontrollers may directly interface with the 8X401.

THE 8X401 AS AN I/O PROCESSOR

Personal computers are growing increasingly more powerful, and computers that support a variety of peripherals and provide colour graphics and network capability are not uncommon. In many of these systems the main processor is called upon to perform routine I/O control operations, in addition to running the user's application program. System performance would be improved if any of the tedious I/O control tasks could be off-loaded from the main processor.

With its bit-manipulation orientated instruction set, and its 150-ns instruction cycle time, the 8X401 is suited for I/O control applications. It can also be used as an I/O processor in personal computer applications (Fig.2).

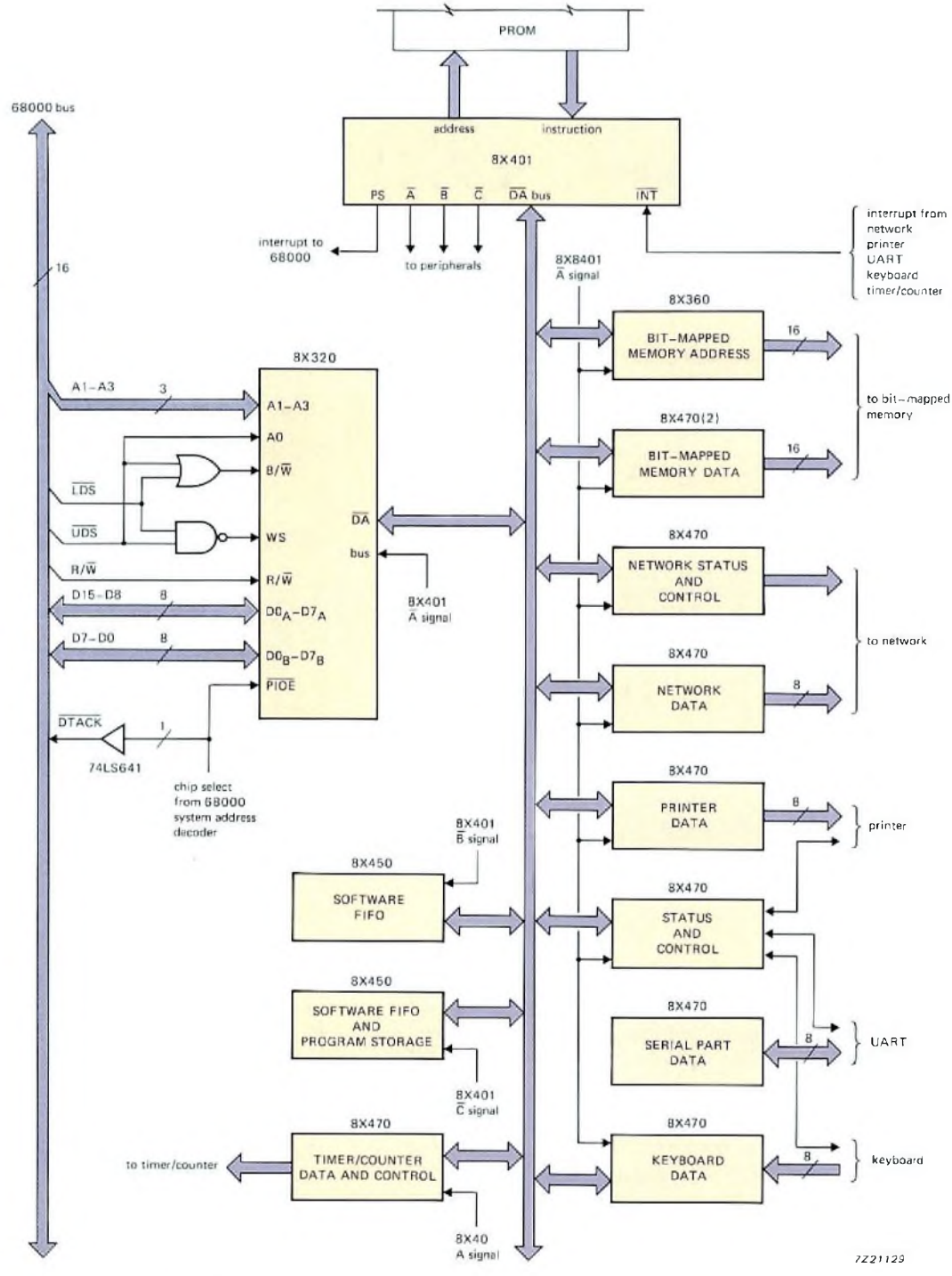


Fig.2 The 8X401 may be used as an I/O processor in personal computer applications

SYSTEM DESIGN

The 8X401 offloads various I/O control tasks from the host processor (Fig.2). These I/O tasks, which are controlled by the 8X401, include a 640 x 320 colour display, a high-speed network, a parallel printer, a serial port and a keyboard. The host processor in this system is a 68000 microprocessor. The 8X401 presents a high-level software interface to the 68000. Host commands on I/O devices, such as DRAW LINE and TRANSMIT TO NETWORK, are implemented by the 8X401.

The hardware interface between the 8X401 and the 68000 is an 8X320 Bus Interface Register Array chip. The 8X320 can be thought of as a mailbox; it interfaces two independent ports, a primary and a secondary port, using either 14-byte or seven-word addressable data registers. Also within the 8X320 is a 16-bit flag register, which also can be either byte or word accessed. The 8X320 maps one status flag for each of its 14-byte data registers. When either the 68000 or the 8X401 writes to a data register, the appropriate flag is set. The status flags can then be polled to facilitate interprocessor communications.

The secondary port of the 8X320 is tied directly to the 8X401 I/O bus and is mapped onto its A bank. No external "glue" gates are needed. The primary port of the 8X320 is tied to the 68000's local bus. This interface requires the addition of only three "glue" gates, one OR gate, one NAND gate and one open collector buffer. The 68000 can then access the 8X320 either in byte or word mode. With byte-mode addressing, odd-address bytes are transferred over the 68000's lower data lines D0-D7. Even-addresses are transferred over the 68000's upper data lines D8-D15. With word-mode addressing, data is transferred over the entire 16-bit data bus of the 68000. Both read-modify-write and test-and-set classes of instructions are supported at the 68000/8X320 interface.

The various I/O devices of Fig.2 interface to the 8X401 through eight 8X470 programmable I/O ports and one 8X360 Memory Address Director (MAD). The 8X360 and two of the 8X470s are used to interface to the bit-mapped graphics memory. These peripheral devices are all mapped onto the 8X401's A bank. The 8X360 and the two 8X470s tie directly to the 8X401's I/O bus; no external "glue" or buffering is needed. The 8X360 generates the address needed to access pixel information contained in the bit-mapped memory. Data that can be either written to or read from the graphics memory is held in two 8X470s.

Two 8X470 I/O ports are needed to interface the 8X401 to the high-speed network. One 8X470 contains data to be sent to or received from a serializer/deserializer. The other 8X470 monitors and controls various other signals needed to implement the network interface.

Because the printer used in Fig.2 is a parallel printer, the 8X401 requires one 8X470 port to send 8-bit ASCII data to the printer. Printer control and status lines are integrated into the system through a second 8X470. This second control and status 8X470 has additional capability above and beyond the printer interface. This excess is consumed by the serial port and keyboard interfaces.

The two remaining 8X470s complete the UART and keyboard interface. One 8X470 is used to send or receive data from the UART. The second 8X470 is used to receive parallel data from the keyboard. In addition to the eight I/O 8X470s, the system contains one timer/counter 8X470. This port is used to interface the 8X401 to the timer/counter, which is used in system operation.

To improve system performance, it's desirable to provide first-in, first-out (FIFO) buffering for the network, the printer, the UART and the keyboard. The 8X401 implements FIFO buffers for these devices using an 8X450 256-byte RAM and software. This 8X450 is allocated all 256 locations on the B bank.

The 8X401 has 13 general-purpose registers on-board. To allow additional temporary storage capability, an 8X450 RAM has been added to the system (Fig.2). With devices already residing on the 8X401's A and B banks, the 8X450 is mapped onto the C bank. If desired, portions of this program storage 8X450 can be reassigned for additional FIFO storage.

The software configuration of the system is resident in the 8X401 program PROMs. The software consists of a basic real-time operating system and five applications modules (device drivers), one for each I/O device. The device drivers contained in PROM perform the actual control of each of five I/O devices.

The operating system has three major parts, a process scheduler, an interrupt handler and a 68000 communications package. The I/O system may have multiple I/O devices active simultaneously. For example, the 68000 may have instructed the 8X401 to send data to both the printer and the serial port. The system may then have multiple device drivers simultaneously active.

To provide each I/O applications module with some processing time, process scheduling with a time-slice algorithm is used. The process scheduler selects which active process is allowed to run next. Depending upon its priority, this selected process is allocated a specific amount of microcontroller time. The allocated time is loaded into the timer/counter 8X470 on the A bank, and the process is allowed to run. When the allocated time expires, an interrupt is generated by the timer/counter. The applications program is then interrupted and control is returned to the operating system.

In addition to handling interrupts from the timer/counter, the 8X401 must handle interrupts from the network, the UART and the printer. The interrupt handler determines the highest priority interrupt pending and takes the necessary action.

The last major part of the operating system is the 68000 communications package. Communication between the two

processors is bidirectional, with both the 68000 and the 8X401 communicating with each other through the 8X320. This communications package can be divided into two portions: a 68000 command module and an 8X401 request module. The 68000 command module, at every time-slice interrupt, polls the 8X320 to determine if any 68000 I/O commands have been given. If a command has been input to the 8X320, the 8X401 takes the appropriate action.

Only the 8X401 request module is allowed to communicate with the 68000. Any device driver needing to communicate with the 68000 will make a system call. These system calls are responded to at time-slice boundaries, with the 8X401 request module activated. This module polls the 8X320 to determine if space for the device driver's message is available. If space is available, the message is stored in the 8X320 and a 68000 interrupt is generated. This interrupt is asserted using the 8X401's Programmable Status (PS) output pin. When the 68000 acknowledges this interrupt, through the 8X320, the 8X401 releases PS, removing the interrupt. If there is no space available in the 8X320, all messages from device drivers are stored in the 8X450 mapped on bank C.

As power increases in personal computers, greater burden will be put on the main system microprocessor. The 8X401, implemented as an I/O processor, can help relieve some of this increased burden on host processors, improving overall system performance as well as price/performance ratio.

ACKNOWLEDGEMENT

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The 8X401 has a variety of instructions that includes conditional jumps and returns

instruction type	variation	description
ADD	ADD	ADD
	ADC	Add with Carry
	AD8	ADD Immediate 8
	AD5	ADD Immediate 5
AND	AND	AND
	AN8	AND Immediate 8
	AN5	AND Immediate 5
JUMP	JIF NS	JUMP IF SI = 0
	JIF S	JUMP IF SI = 1
	JIF NC	JUMP IF Carry = 0
	JIF C	JUMP IF Carry = 1
	JIF Z	JUMP IF ALU = 0
	JIF NZ	JUMP IF ALU < > 0
	JSR	JUMP to Subroutine
	JMP	JUMP
	PSJ	POP STACK AND JUMP
MOV	MOV	MOVE
RETURN	RIF NS	RETURN IF SI = 0
	RIF S	RETURN IF SI = 1
	RIF NC	RETURN IF Carry = 0
	RIF C	RETURN IF Carry = 0
	RIF Z	RETURN IF ALU = 0
	RIF NZ	RETURN IF ALU < > 0
	RTN	RETURN
	RCC	RETURN and Clear Carry
	RSC	RETURN and Set Carry
XEC	XEC	Execute
XMIT	XT8	Transmit Immediate 8
	XT5	Transmit Immediate 5
XOR	XOR	Exclusive OR
	XR8	Exclusive OR Immediate 8
	XR5	Exclusive OR Immediate 5

Breakover diodes for protection of telephone equipment

D. F. HASLAM and M. J. HILL

A new transient suppressor for protecting telephony equipment from line voltage-transients has been developed – the breakover diode (BOD). The BOD is suitable for protecting subscriber equipment and exchange equipment such as:

- subscriber loop interface circuits (SLICs)
- modems
- answering machines
- telex machines
- facsimile machines
- private branch exchanges.

Outside telephony, the BOD can be used to protect data terminals connected to local area networks and a variety of digital communication equipment. Breakover diodes are not intended for suppressing mains transients or for use with high-current d.c. supplies.

Our BODs are available as single or dual types. The dual BODs are ideal for two-line-to-earth protection, see Fig.1. BODs with either a symmetrical characteristic (for bi-directional operation) or an asymmetrical characteristic (that is, forward breakover and reverse conducting for uni-directional operation) are available. In many cases, heat-sinks aren't needed, the low thermal impedance in free-air of a BOD enabling transient peak currents up to 40 A to be handled*. And for these applications, we intend to manufacture BODs in the small glass implosion encapsulation, SOD-84, in the near future.

* acc. to CCITT Rec. K17.

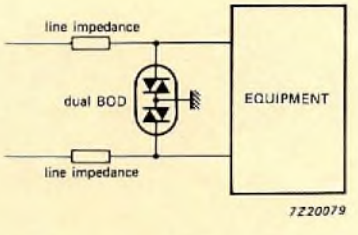


Fig.1 Two-line protection of telephone equipment using one dual breakover diode (BOD)

Lightning is but one of many hazards threatening today's telecommunications networks. Breakover diodes, introduced in this article, are transient suppressors that can protect telephony equipment against not only lightning-induced transients but other common hazards as well. High peak-current handling capability and stable characteristics make breakover diodes attractive alternatives to zener diode and voltage-dependent resistor suppressors (Photo courtesy of Ir. H. Aaftink)

CHARACTERISTICS

A BOD can be compared with transient suppressors such as zener diodes and voltage-dependent resistors. However, unlike a zener diode, where a transient is absorbed at a zener voltage, a breakover diode absorbs a transient at a much lower voltage, V_T, of typically 2,5 V (see Fig.2). This is why a BOD has a high peak-current-handling capability. And unlike a VDR, there is no deterioration of performance over a BOD's operating life.

Let us now look at the characteristic of a BOD in more detail, see Fig.3. Under normal operating conditions, the voltage across a BOD, for example the telephone line voltage, is less than the breakdown voltage V_{BR}. The BOD passes only a very small current, typically 50μA at the stand-off voltage V_D (85% V_{BRmin}). When a voltage transient reaches the BOD, the voltage across it is initially clamped by avalanche conduction. When the avalanche current exceeds the switching current I_S, the BOD switches to a low-resistance high-conduction state, the transient current being conducted at a low on-state voltage V_T, and the BOD is 'latched'.

When the transient is over, normal line conditions resume as the BOD switches off when the fault current falls below the holding current I_H, the BOD being chosen such that the normal d.c. line current is less than the minimum holding current specified for the device.

A glossary of the most important terms used to describe a BOD appears at the end of this publication.

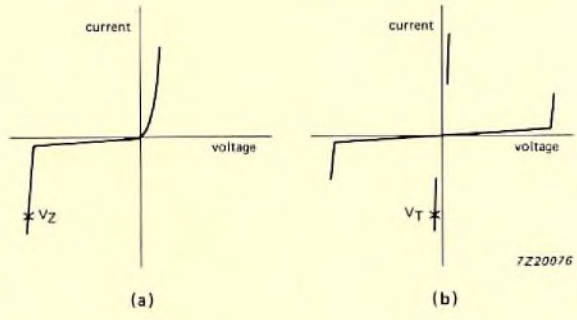


Fig.2 (a) Characteristic of a zener diode (transient suppression at zener voltage V_Z) and (b) characteristic of a symmetrical BOD (transient suppression at a voltage V_T; $V_T \ll V_Z$)

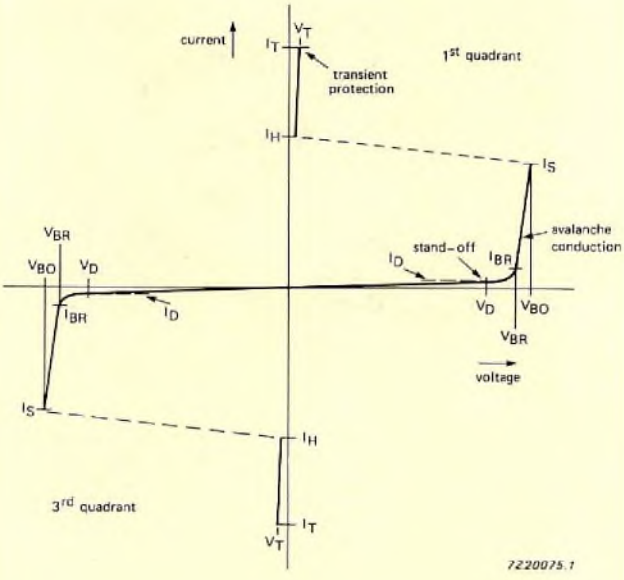


Fig.3 Characteristic of a symmetrical BOD

PRODUCT RANGE

The following BODs are available (all in the TO-220 encapsulation):

- BR210 series (single symmetrical BODs)
- BR216 (dual monolithic asymmetrical reverse-conducting BOD)
- BR220 series (dual monolithic symmetrical BODs).

Table 1 gives brief data on these BODs. The BR210 series of single BODs will also be available in the axial-leaded SOD-84 glass encapsulation.

The dual asymmetrical BOD, BR216, is for protecting 50 V lines. It has a breakover characteristic in the first quadrant, and the characteristic of a normal rectifier diode in the third (see Fig.4(b)).

The BR220 series of dual symmetrical BODs are particularly suitable for shunt protection of two lines to earth, the earth being connected to the centre lead of the TO-220 encapsulation (Fig.1).

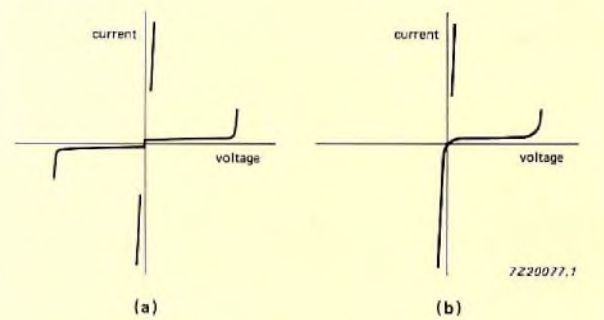


Fig.4 Characteristics of (a) a symmetrical BOD and (b) an asymmetrical BOD (reverse conducting)

TABLE 1
Brief data on our range of breakover diodes; T_{amb} = 25 °C

		BR210 series	BR220 series	BR216	unit
breakover voltage (12% tol.)	V_{BO}	100 to 280[1])	100 to 280[1])	<78	V
holding current	I_H	150	>150	>150	mA
transient peak current[2])	I_{TRM}	40	40	40	A
r.m.s. on-state current	$I_{T(RMS)}$ max.	8	8	8	A
non repetitive peak on-state current at T_j = 100 °C[3])	I_{TSM}	40	40	40	A
rate-of-rise of turn-on current	dI_T/dt	100	100	50	A/μs
thermal resistance junction-to-ambient	$R_{th\ j\text{-}a}$	60	60	60	K/W

[1]) in 20 V steps.

[2]) 10/320 μs impulse (owing to the breakover characteristic of a BOD, this is equivalent to 10/700 μs, 1.6 kV voltage impulse according to CCITT, Vol. IX, Rec. K17).

[3]) 10 ms half sinewave.

CONSTRUCTION AND OPERATION

A BOD has a four-layer pnpn thyristor construction which enables transients to turn the diode on. It is manufactured using a similar process to that used for our thyristors and triacs.

Figure 5(a) shows a section through a symmetrical BOD. When the potential of the upper electrode is negative with respect to that of the lower one, junctions J1 and J3 are forward-biased, but junction J2 is reverse-biased. Provided the potential across the BOD is less than the breakdown voltage V_{BR}, (normal conditions), only a small leakage current flows. When the potential across J2 approaches the designed breakdown voltage as a result of a transient, an avalanche effect is initiated which produces electrons and holes as shown in Fig.5(b). Under the influence of the applied potential, the electrons collect in the n-region between J2 and J3 and increase the forward bias across J3, enabling J3 to emit holes towards J2. Simultaneously, the holes from the left half of J2 reach the upper electrode by moving through the p-type base below the n^+-emitter. The resistance of this base, R, shown schematically in Fig.5(c) and (d), produces a voltage drop (I_eR) that increases the forward bias across junction J1, enabling J1 to emit electrons towards J2. With both J1 and J2 emitting charge carriers, junction J2 breaks down completely and the 'thyristor' switches to the low-voltage on-state.

For transients of opposite polarity, the right half of the BOD shown in Fig.5 turns on by means of the same mechanism, only now J3 is the junction that breaks down.

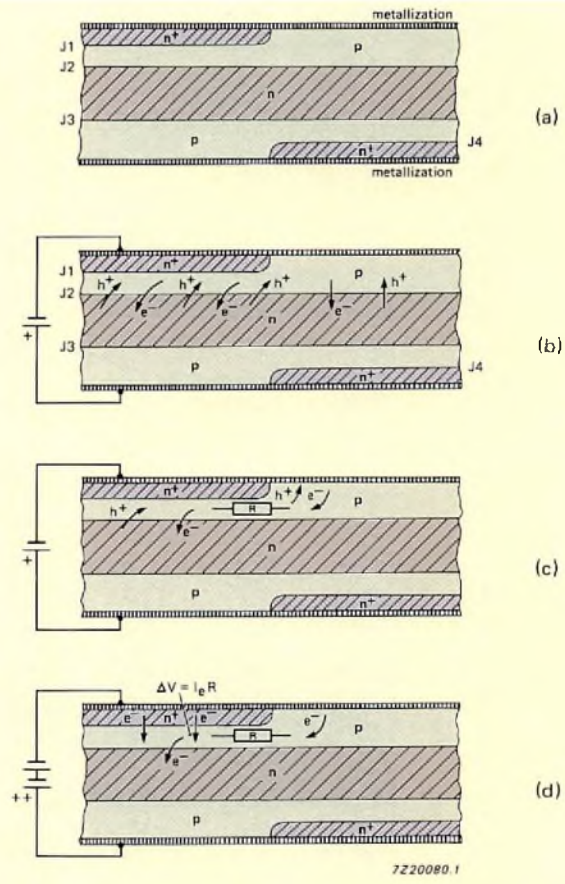


Fig.5 Section through a symmetrical BOD showing (a) the construction, (b) and (c), the movement of the charge carriers associated with the avalanche conduction, and (d), the electron injection which ultimately causes breakdown of the junction J2, turning the diode on (see main text). The BOD shown is symmetrical; dependent on the polarity of the voltage transient, junction J2 or junction J3 will break down

For well-defined switching and holding, the resistivity of the p-layers is carefully controlled, since it has a direct effect on the potential in these layers (Fig.5(c)). In addition, the depths of the p and n^+-layers are kept within tight tolerances by using the most advanced diffusion and ion implantation techniques.

The construction of a practical BOD differs slightly from that shown in Figs 5 and 6, for which the location of the initial electron injection from the upper n^+-layer into the p-layer is not well-defined. For optimum latching, several p-material 'short-circuits' to the upper electrode are formed within the n^+-layer, the short-circuits determining precisely where latching will occur, (see Fig.7). This construction ensures a well-defined breakover voltage V_{BO} and reproducible switching and holding currents – essential attributes for reliable protection.

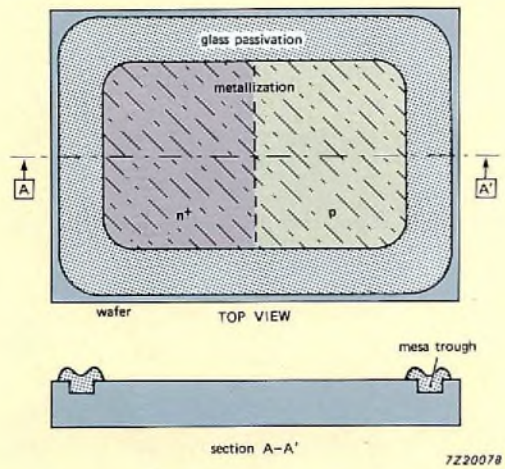


Fig.6 Top view of a basic BOD. All our BODs are glass-passivated

AVALANCHE DISSIPATION

The published dissipation ratings are not valid for prolonged operation of a BOD in the avalanche region when the BOD doesn't breakover, for example, when the load impedance is between 500 Ω and 5 kΩ. In this case, avalanche currents can flow that are insufficient to cause breakover, but which can overheat a BOD. This situation does not arise when the load impedance is less than 500 Ω, because there is then always sufficient avalanche current to cause breakover. When the load impedance is more than 5 kΩ, although there is insufficient avalanche current to cause breakover, the avalanche dissipation remains well within published ratings.

Note that the temperature-dependence of a BOD's characteristics may help to prevent overheating. Since the switching current of a BOD decreases as the diode heats up, it may eventually decrease sufficiently for the diode to breakover, halving the avalanche dissipation immediately.

AMBIENT OPERATING TEMPERATURE/ JUNCTION TEMPERATURE

Our BODs are designed to operate at ambient temperatures between 0 and +70 °C. For most applications, they don't require heatsinks, the transient thermal impedance of a BOD enabling it to handle high non-repetitive transient currents.

For reliability and to keep the off-state current within reasonable limits, the junction operating temperature of a BOD should not exceed 125 °C (off-state). However, during mains contact overloads, the junction temperature is allowed to rise to 150 °C.

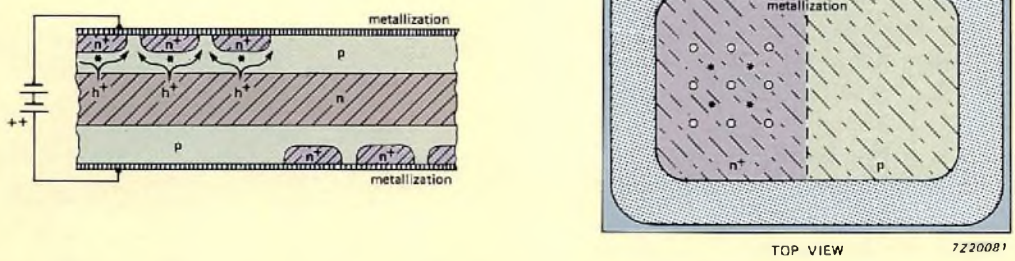


Fig.7 For well-defined latching, the n^+ region of a BOD is perforated with p-material from the underlying base region, latching occurring at the locations marked with an asterisk

TEMPERATURE-DEPENDENCE OF CHARACTERISTICS

Details of the temperature-dependence of a BOD's characteristics are given in the published data sheets. These are calculated for worst-case conditions to ensure reproducible protection over the complete operating temperature range.

V_{BR} and V_{BO} are published for a junction temperature of 25 °C. Both V_{BR} and V_{BO} increase with temperature by about 0,1%/K. However, because the switching current decreases with temperature, the actual switching point at V_{BO} does not increase by quite as much as V_{BR}. The published 12% tolerance on these two parameters at 25 °C is sufficient for most applications.

Figures 8, 9 and 10 show typical curves of the maximum off-state current, the switching current and the minimum holding current as functions of junction temperature. A quality design and stringent process control during manufacture limit the device spread of switching current to less than 500 mA (typ.) for a BOD rated at 40 A transient peak current.

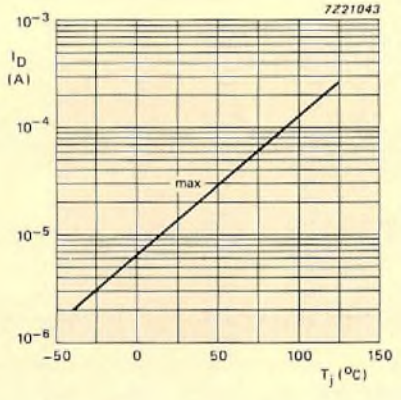


Fig.8 Maximum off-state current of a BR220 series BOD as a function of junction temperature

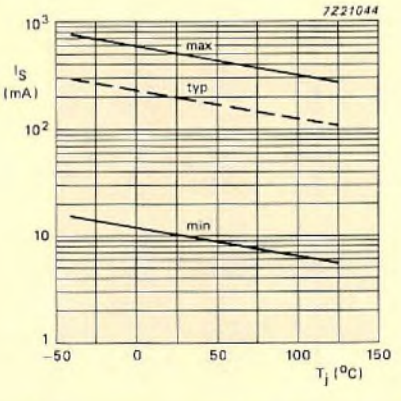


Fig.9 Switching current of a BR220 series BOD as a function of junction temperature

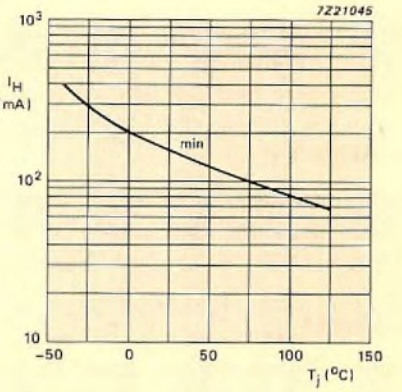


Fig.10 Minimum holding current of a BR220 series BOD as a function of junction temperature

CAPACITANCE

A BOD introduces an extremely small capacitance (which can usually be neglected) across the circuit it is protecting. In the off-state (with no bias), the junction capacitance of a BOD is less than 350 pF for the symmetrical BODs, less than 500 pF for the BR216.

MAINS CONTACT FAULTS

Because of its relatively low breakover voltage, the BOD is not intended to protect equipment from mains voltage transients. And in cases of mains contact, the allowable avalanche dissipation may be exceeded. Nonetheless, a BOD will provide a degree of protection when there is accidental mains contact. In some cases, the BOD will protect and survive without degradation after the mains fault clears. In other cases, the BOD may be damaged. If damaged, the BOD becomes a short circuit, still protecting the equipment behind it, even though the BOD will have to be replaced afterwards.

GLOSSARY FOR BREAKOVER DIODES

Breakover voltage V_{BO}

The nominal voltage which will cause a BOD to breakover ($I = I_S$). The voltage which will cause all BODs to breakover V_{BOmax} is about 12% higher than the nominal breakover voltage.

Minimum avalanche voltage V_{BRmin}

The voltage below which no BOD will conduct more than a specified avalanche breakdown current I_{BR} (usually 10 mA). V_{BRmin} is about 88% of the nominal V_{BR}. A BOD should be chosen with such a V_{BR} that overvoltage transients are adequately suppressed while all required signals are not clipped during normal operation (e.g. the ringing tone in telephony).

Stand-off voltage V_D

The voltage at which the maximum off-state current I_D is specified. V_D is specified for blocking operation. At V_D, there is virtually zero insertion loss. $V_D = 0{,}85\ V_{BRmin}$.

On-state voltage V_T

The maximum instantaneous voltage at a specified current once the diode has been switched on by an overvoltage transient. V_T is less than 3 V at a peak diode current of 10 A.

Off-state current I_D

The maximum leakage current normally quoted at or below V_D. I_D is less than 50 μA at 25 °C. Published data gives the temperature-dependence of I_D for calculating insertion loss.

Holding current I_H

The minimum on-state current below which all BODs will switch to the off-state. An I_H higher than the normal d.c. line current is chosen, otherwise the diode will not return to the off-state after suppressing a transient.

Switching current I_S

The maximum avalanche breakdown current a BOD can sustain before switching to the on-state. I_S is normally specified for a 100 μs pulsed load condition. The minimum value specified indicates the immunity of the breakover diode to very-low-energy transients. It can be used to select a BOD that won't suffer from nuisance tripping. The maximum value indicates the current that is guaranteed to switch on the BOD.

For transient currents less than the switching current, a BOD behaves like a zener diode type of transient suppressor.

RMS on-state current $I_{T(RMS)max}$

The maximum rated r.m.s. current that the BOD can withstand at a specified encapsulation temperature.

Rate-of-rise of on-state current dI_T/dt

The maximum rate-of-rise of on-state current, dI_T/dt, is the rate of current increase following breakover above which there is the likelihood that the BOD will be damaged due to localised overheating of the silicon chip. As for thyristors, hot-spots can damage the blocking junctions.

For thyristors, dI_T/dt is usually specified for gate-triggered operation; for BODs, turn-on is initiated by avalanche current, a good chip design ensuring the BOD turns-on uniformly over all of the active area of the chip.

Published values of dI_T/dt are more than adequate for most applications where the line inductance will limit dI_T/dt to much lower values.

A BOD can even withstand discharging some capacitance connected across it, since to a large extent, a BOD limits its own turn-on rate-of-rise of current.

Transient peak current I_{TRM}

BODs have exceptionally high impulse current ratings. The data sheets specify the transient peak currents for an 8/20 μs impulse and for a 10/320 μs impulse (see Fig.11), the latter being equivalent to a 10/700 μs, 1,6 kV voltage impulse according to CCITT Rec. K17.

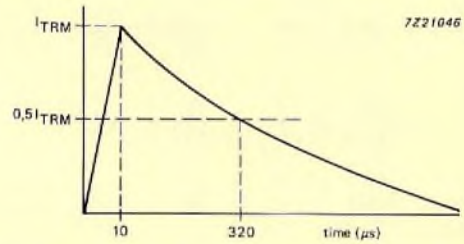


Fig.11 Impulse equivalent to that of CCITT Rec. K17 for determining the transient peak current rating of a BOD

Non-repetitive peak on-state current I_{TSM}

The maximum rated 10 ms half sinewave current that the diode can withstand.

Quality - dry reed switches

F. A. PIETERS

Proven in telephone equipment and now selected by major manufacturers for automobile, computer and test-gear application, our dry reed switches have quality built in right from development. Their quality potential is realized consistently by a zero defect-oriented production environment.

Constant quality improvement has resulted in continual AQL reduction. Dynamic-contact-resistance process-average reject levels, currently in the region of a few hundred parts per million, are steadily improving, as is the quality of all other important characteristics.

Reliability now approaches $2{,}5 \times 10^{-9}$/operation.

Clean process conditions make a vital contribution to both the exceptional conformity and reliability of our reed switches

Our dry reed switches are both designed for and used in the most demanding applications, including computer keyboards, telephone equipment, automatic test equipment and automobiles. Thus, their quality – both conformity and reliability – must be exceptionally high. We build this quality into our reed switches, at every stage in their design and manufacture.

This article describes the quality philosophies, routines and methods that we employ, and gives results of both Quality Control tests and field experience. Terms and definitions used are those of IEC Publication 255-9 as used in our Data Handbook (Vol. T15). Quality methods are generally in accordance with IEC Publication 68; with procedures corresponding to CECC 19000 (although CECC Release is not available).

ORGANIZED FOR QUALITY

The foundation of the exceptional quality of our reed switches lies in the comprehensive organization that lies behind every step of their design, development, manufacture, and application. Responsibilities and communication paths are well defined; Quality Control is independent, but integrated with production and development; the importance of continual education and training is fully recognized and implemented. The quality achieved is evidence by:

- uniform product characteristics from batch to batch
- rugged construction
- long useful life
- low early-failure rate
- low AQLs (from 0,1%) ensuring that only good products are shipped
- process-average reject levels well below AQLs.

Not only is the quality of our reed switches already high, but it is constantly being improved. Our comprehensive quality-improvement programme features:

- close collaboration with customers to satisfy specific application requirements, and solve problems
- production-processing spread reduction
- stabilization of process conditions with rigorous significant change procedures
- involvement of everyone in improvement activities
- statistical process control
- well-understood quality indicators.

Our working environment is designed to encourage quality awareness, with:

- close collaboration between individuals and departments, especially
- close cooperation between Marketing, Quality, Development and Production
- clearly-defined responsibilities
- AQAP-1 procedures guiding all activities
- in-depth training
- high-grade support from service departments
- effective dissemination of information at all levels.

Reed switches type selection

series		RI-22	RI-23	RI-25	RI-27	RI-45	RI-46	
description	unit	general purpose micro-reed	general purpose micro-reed	high power micro-reed	general purpose pico-reed	mains voltage switching micro-reed	high power micro-reed	
operate-values	amp. turns	8-70	8-70	8-32	10-34	27-59	10,5-28	24-70
release-values	amp. turns	4-32	4-32	4-22	4-19,5	8-21	4-16	8-22,5
contact resistance	mΩ	max. 90	max. 100	max. 100	max. 115	max. 90	max. 90	max. 90
insulation resistance	Ω	min. 10^{12}	min, 10^{12}	min. 10^{12}	min. 10^{12}	min. 10^{12}	min. 10^{12}	min. 10^{12}
switched power	W	10	10	8 to 25	10	40	30	40
switched voltage	V	200 d.c. 140 a.c.	200 d.c. 140 a.c.	200 d.c. 140 a.c.	200 d.c. 140 a.c.	250 a.c.	200 d.c. 250 a.c.	200 d.c. 250 a.c.
switched current	mA	500	500	1000	500	1000	1000	1000
bounce time	μs	typ. 150	typ. 150	typ. 150	typ. 50	typ. 150	typ. 150	typ. 150
wire diameter.	mm	max. 0,65	max. 0,60	max. 0,60	max. 0,50	max. 0,65	max. 0,65	max. 0,65
glass diameter.	mm	max. 2,8	max. 2,54	max. 2,54	max. 1,8	max. 2,8	max. 2,8	max. 2,8
glass length	mm	max. 15,0	max. 15,0	max. 15,0	max. 13,5	max. 21,5	max. 21,5	max. 21,5
total length	mm	46 ± 0,5	46 ± 0,5	46 ± 0,5	46 ± 0,5	54,8 ± 0,5	54,8 ± 0,5	54,8 ± 0,5

QUALITY PROCEDURES

Properly documented procedures are essential to the achievement, maintenance and improvement of high product quality. They help us ensure that all aspects of our reed-switch activity, from development to customer service, are carried our thoroughly, and that maximum information is available to refine designs and processes and generate new designs.

Release procedure

Before new reed switch types can be delivered, even as samples, to customers they must have obtained an Approval for Delivery (AFD), according to our Release Procedure. This is obtained at a meeting that includes representatives of the Development, Marketing, Production and, especially, Quality Departments at which data obtained from samples is reviewed.

Once AFD is granted, small-scale production is sanctioned. Quality evaluation during this stage provides data for a Release Report. This Report is examined at a Release Meeting, before Release for (full-scale) Production (RFP) is granted. Release for Production is also required for new cut and/or bent-lead versions of existing reed-switch types.

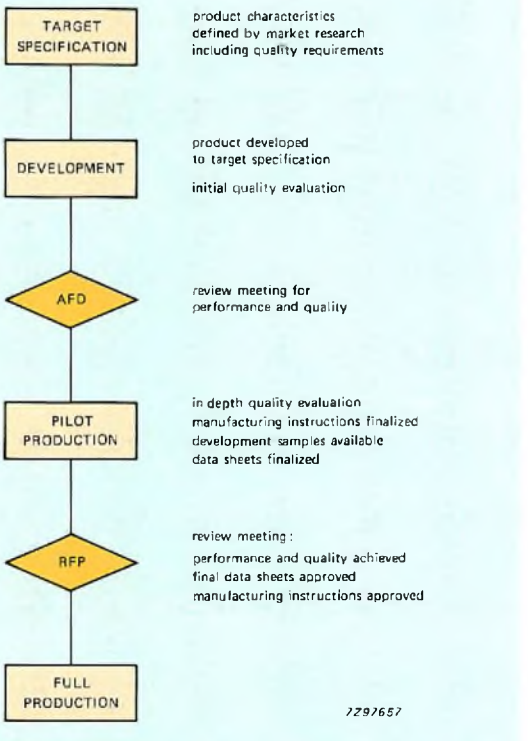
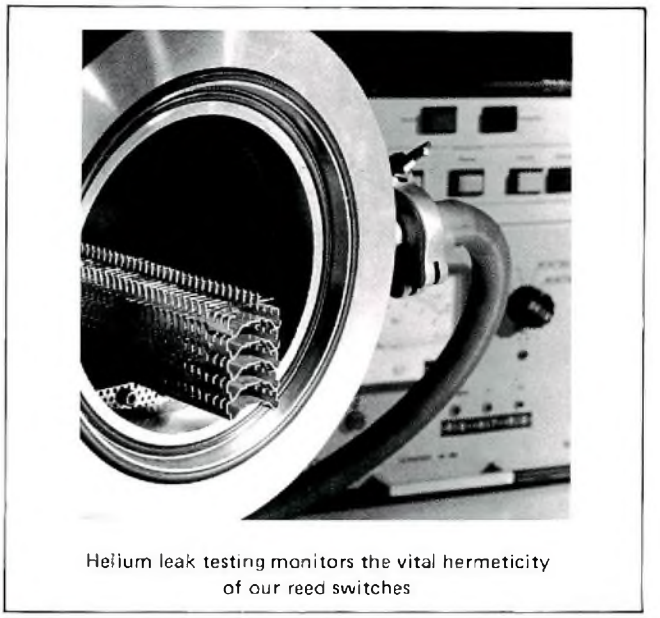


Fig.1 Release of new reed switch types for delivery and production is controlled by this formal Release Procedure. By ensuring that intermediate quality requirements are fully met before new designs proceed to full production, we ensure that their quality potential meets the high standard required in modern equipment. Similar procedures apply to new processes or materials, and to significant design or production changes



Helium leak testing monitors the vital hermeticity of our reed switches

Strict adherence to the Release Procedure, Fig.1, ensures that new types of reed switch are capable of meeting our stringent Quality requirements from the outset.

Manufacturing instructions

The routing of our reed switches through the production process is fully documented in the Manufacturing Instructions for each type. These Instructions also describe incoming and in-line inspection and Quality Control methods and requirements.

Calibration procedures

Accurate test and measuring equipment is an essential prerequisite for the maintenance and improvement of product quality. Calibration procedures are laid down in the plant Quality Manual. Basic requirements include regular calibration of all equipment, with clear reporting of accuracy.

Deviations from the required accuracy of any equipment must be clearly reported and acknowledged. Nature of the deviation must be specified and responsibility for the equipment defined, so that its rectification can be verified.

Quality reporting

Quality reporting requirements are laid down for:

- incoming material and components inspection
- production yield
- sampling inspection (Quality Control) results
- customer returns
- quality improvement planning
- process and performance changes.

These vital aspects of our reed switch production will now be described in detail.

QUALITY IN REED-SWITCH PRODUCTION

Figure 2 shows how inspection and quality control are integrated into our reed switch production. Quality Control inspections are carried out both by the operators and by line inspectors; the Quality Department monitors Quality Control inspection and process conditions, and carries out final Acceptance and Qualification testing. Test equipment is checked by line inspectors, and calibrated by the Quality Service Department.

Incoming inspection

Wire for reed contacts is checked for:

- appearance
- diameter
- circularity
- chemical composition
- magnetic characteristics
- scoring and cracking.

Following annealing, the expansion coefficient of the wire is checked, and the magnetic characteristics measured again.

Glass tubing for reed switch bodies is checked for:

- appearance
- dimensions

before being ultrasonically cleaned and dried.

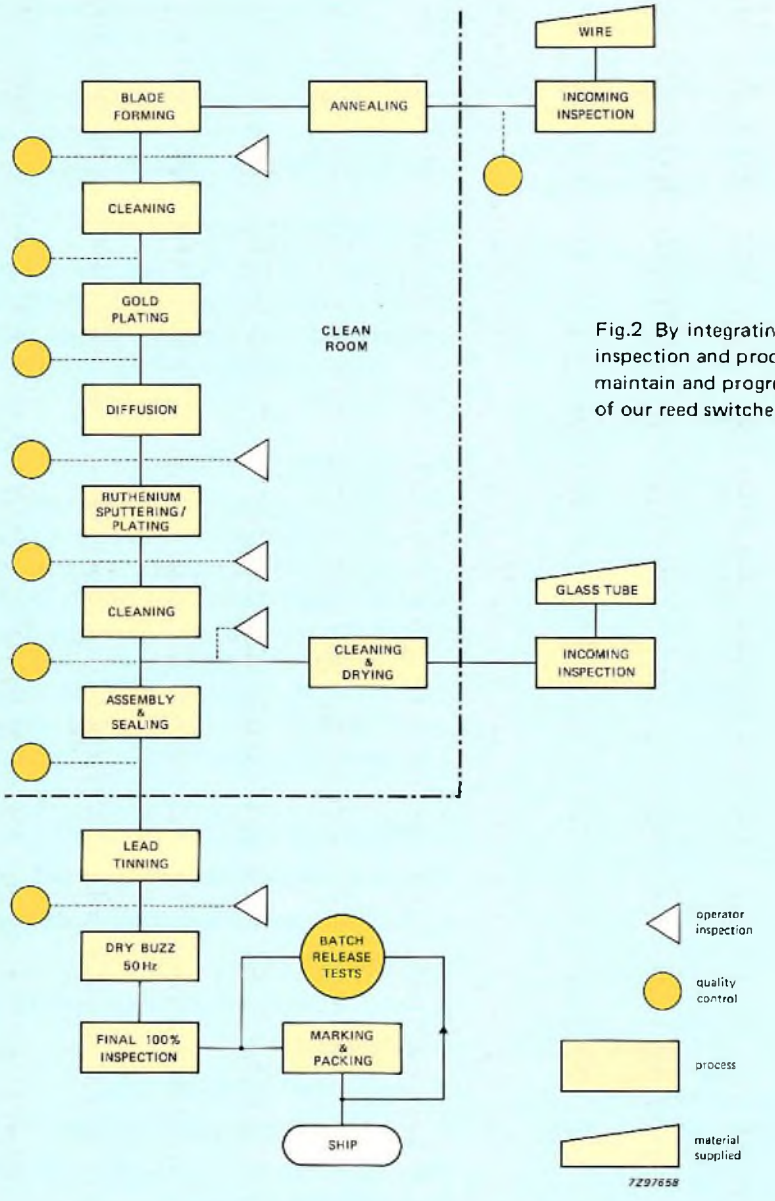


Fig.2 By integrating Quality Control fully with inspection and production, we are able both to maintain and progressively improve the quality of our reed switches

TABLE 1
Acceptance tests for RI-22AA reed switches
(symbols are listed in Table 2)

test	conditions	limits	AQL	level
(a)				
CR dynamic	$I_c < 50$ mA, $V_{bc} < 0{,}02$ V E = 1,25 times max 'must operate' amp. turns. f = 3 Hz, CR dynamic is measured after 2 ms and for 2,5 ms	<110 mΩ	0,10	I
must not release	$I_e < 10$ mA	<17 At	0,40	I
must release		>8 At		
must not operate	$V_{be} < 0{,}02$ V	>14,5 At		
must operate		<22,5 At		
CR static	$I_e < 10$ mA, $V_{be} < 0{,}02$ V E = 25 At	<80 mΩ	0,10	I
(b)				
visual	magnification 20 times		1,5	S4
solderability	IEC 68-2-20 test T_a method 3, 235 °C/4 hrs. steam.		1,5	S3
gauge (dimensions)	acc. to published dimensions		1,5	I
hermeticity		10^{-6} torr. ℓ/s ($1{,}33 \times 10^{-6}$ Paℓ/s)	0,25	II

TABLE 2
Symbols used in Table 1

symbol	unit	description
CR	mΩ	contact resistance
E	At	coil energization
I_c	mA	contact current
V_{bc}	V	open contact voltage

Quality Control inspection

As Fig.2 shows, inspection of Quality Control is performed after each mechanical or chemical process stage. Moreover, to ensure product uniformity, the Quality Department constantly monitors the critical process conditions of:

- gold plating
- gold diffusion
- ruthenium plating or sputtering
- sealing
- appearance
- dust level in the dust-free room.

Acceptance testing

Following final inspection, samples of reed switches are taken from each batch according to the requirements of MIL-STD-105D (ISO 2859). These samples are subjected to in-depth evaluation to ensure that all requirements are fully met before despatch.

Acceptance tests

Using a standard test coil, samples of reed switches from each batch sampled are tested for:

- dynamic contact resistance
- 'must not release' ampere-turns value
- 'must release' ampere-turns value
- 'must not operate' ampere-turns value
- 'must operate' ampere-turns value
- static contact resistance.

These tests are listed, together with limit values, for our RI-22AA reed switches in Table 1(a). The limits used for these tests are normally within the published or specification limits.

Further samples from each batch of reed switches are submitted to the following tests:

- visual inspection
- solderability
- gauge check (dimensions)
- hermeticity.

These tests are detailed for RI-22AA reed switches in Table 1(b).

TABLE 3
Life tests for reed switches

conditions[3])	operations	monitored for CR and sticking	status of tests	type
12 V, 2 mA (100 mA peak)	10^7	yes[1])	batch release	RI-22 series RI-23 series
12 V, 4 mA (15 mA peak)	5×10^7	yes[1])	batch release	RI-22 AA RI-27 series
20 V, 500 mA	$2{,}5 \times 10^7$	yes[1])	batch release	RI-46 series
5 V, 100 mA	$5{,}10^7$	yes[2])	batch release	RI-27 series
no-load	10^8	yes[2])	periodic	RI-22 series RI-23 series RI-46 series
no-load	2×10^8	yes[2])	periodical	RI-27 series

[1]) CR dynamic 2 Ω.
[2]) CR dynamic 1 Ω.
[3]) Coil energization = 1,25 times the maximum published must operate ampere turns for the selection group.

Life tests

Further samples of reed switches from each batch are subjected to the life tests described in Table 3. All failures are analysed to provide additional corrective-action data.

Note that, due to wiring inductance and capacitance, switching waveforms in loaded life tests include an initial, very short, high-current pulse component. Since the amplitude of this pulse can have a large effect on the life test results it is necessary to specify and control it.

Modern, computer-controlled test equipment, such as the plating-thickness measuring facility, plays a vital part in our quest for even higher quality reed switches

Laboratory tests

Every four months samples are tested for conformance to the published data and the results recorded. They are tested for:

- operate and release ampere-turns
- ratio operate: release ampere-turns
- dynamic and static contact resistance
- static contact resistance change
- insulation resistance
- capacitance
- operate, bounce and release times
- break-down voltage with and without pre-ionisation
- remanence
- bend, tensile and torsion strain
- dimensions

Regular tensile stress testing of our reed switches helps ensure that their high performance will be unimpaired by the handling they receive during assembly into finished products

Quality measured

Figure 3 to 8 give examples of the Quality (both conformity and reliability) obtained from Acceptance and Life testing of our reed switches during the period 1982 to 1986. Not only is the quality of most characteristics well within our AQL values, but the improving trend due to our Quality Improvement programme is clear.

Reliability, a vital factor in modern, complex equipment, is excellent. Failure rates approach $2{,}5 \times 10^{-9}$/operation in loaded condition, and $0{,}25 \times 10^{-9}$/operation un-loaded.

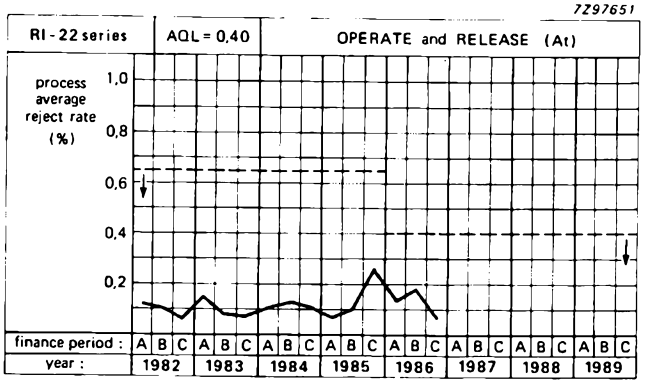


Fig.3 Results of operate and release ampere-turns testing of RI-22 reed switches, 1982 to 1986

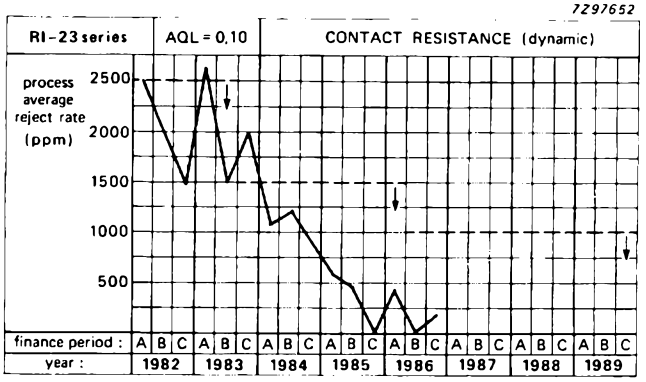


Fig.4 Results of dynamic contact resistance testing of RI-23 reed switches, 1982-1986

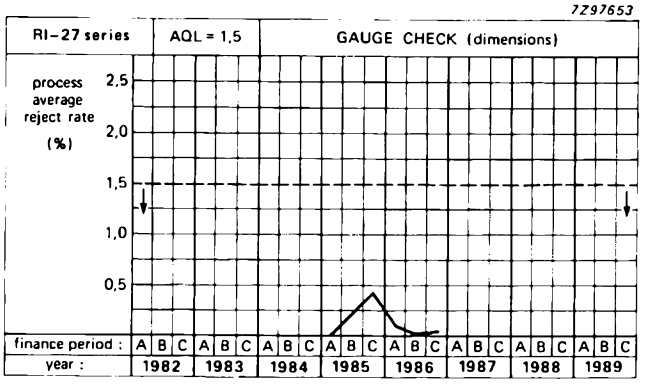


Fig.5 Results of gauge check (dimensions) of RI-27 reed switches, 1985-1986

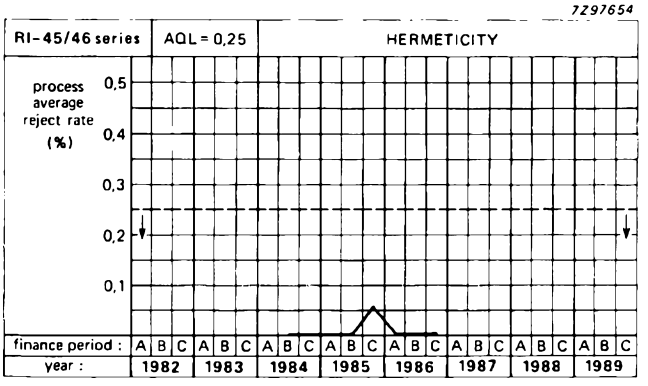


Fig.6 Results of hermeticity testing of RI-45/46 V reed switches, 1984-1986

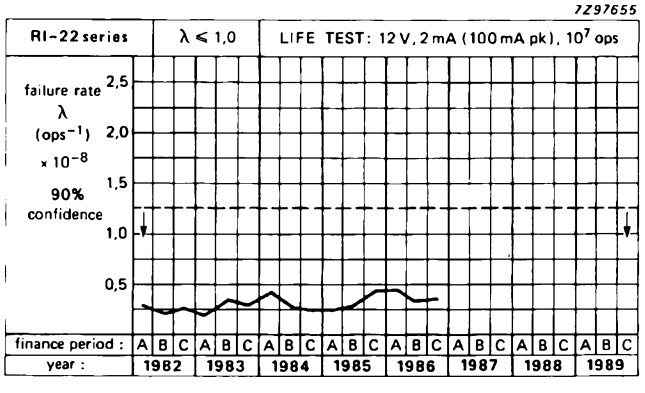


Fig.7 Results of life testing of RI-22 reed switches with a 12 V, 2 mA (100 mA initial pulse) load, 1982-1986.

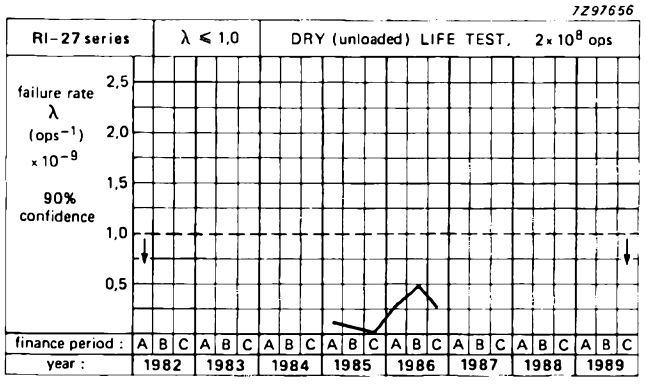


Fig.8 Results of no-load (dry) life testing of RI-27 reed switches, 1985-1986

Packing and labelling

After a batch is accepted according to the specification, the reed switches are packed and labelled with the production week number for traceability.

CUSTOMER RETURNS

We regarded the efficient processing of reed switches returned by customers as vitally important, both to our customers and to ourselves. Our in-depth examination of rejected switches provides valuable additional data for our own Quality Improvement activities, helps guide the development of new or improved switches, and extends our knowledge of their behaviour in real applications.

As the quality of our reed switches improves, so feedback from OEMs and the field becomes an increasingly important source of data for further improvement. For this reason, we have developed the elaborate procedure shown in Fig.9 to ensure that not only are any complaints processed quickly and effectively, but also that all possible data are extracted from rejects.

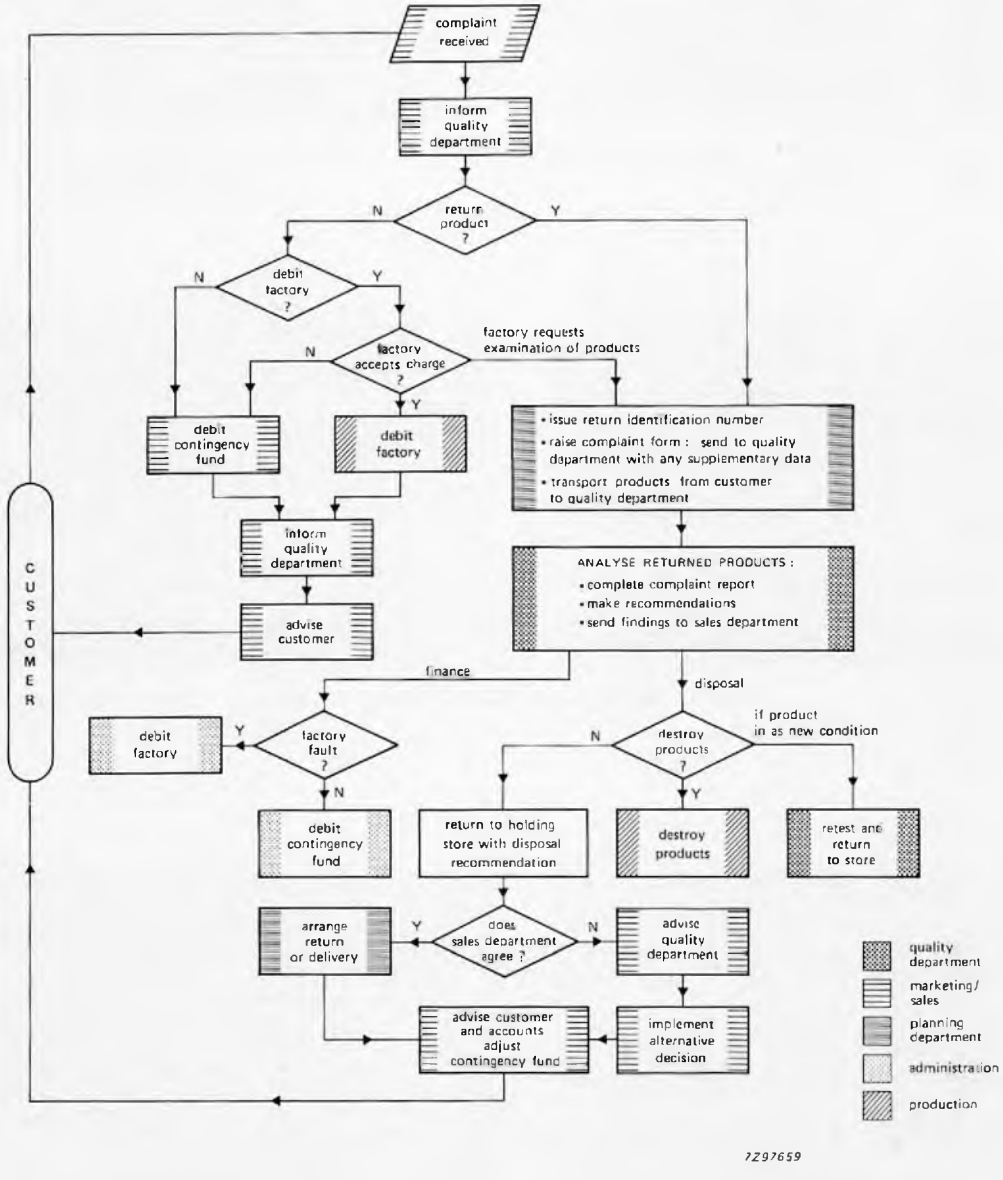


Fig.9 Our elaborate Complaint Procedure is designed not only to provide the best possible service to customers, but also to extract the maximum amount of data for corrective action

The SCC68070: a monolithic 68000 CPU and peripherals

GRAHAM CONN

The recently launched SCC68070 comprises a 68000 central processor and five of the most commonly used peripherals, in a single 84 pin PLCC package dissipating less than 1 W.

In order to reduce design effort and capitalise on existing support tools, device handlers and operating systems, each of the SCC68070's functional blocks is based on an industry standard chip (see Table).

The SCC68070 is highly cost effective in a wide range of applications. With the addition of memory and a CRT controller the device provides all the IC functions necessary to make a simple personal computer or a workstation (see Fig.1). In more powerful machines the SCC68070 makes a suitable front-end processor managing peripheral tasks. Furthermore its two-wire control bus and versatile counter timer section make it suitable for many general purpose control duties.

Before describing each of the major functional blocks it's desirable to have an appreciation of the internal bus structure and the clock circuitry.

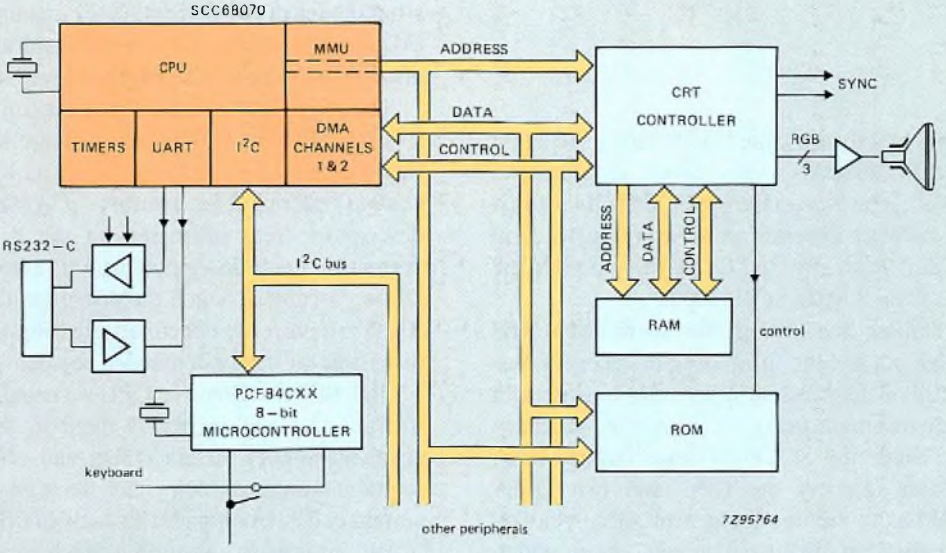


Fig.1 A 68070 minimal system configuration

Compatibility cross reference

68070 function	Related chip
Central Processor Unit	68000/68010
Memory Management Unit	68905/68910
Direct Memory Access	68430/68440/68450
I²C Bus	MAB8400
Uart	2661/2641/2691
Timer	68230/6840

Each of the on-chip peripherals is connected to the CPU via an internal bus. The CPU communicates with these peripherals by asserting supervisor-only mode and encoding additional internal high order address lines. Therefore none of the processor's 16 Mbyte address space is sacrificed for on-chip peripherals, giving the SCC68070 a larger effective addressing range than the SCN68000.

The SCC68070 has an in-built crystal oscillator and clock generation circuit which accepts a maximum crystal frequency of 20 MHz. Internally the crystal frequency is fed into a divider chain before being presented to the functional blocks. The CPU, MMU and DMA sections are driven at half the external clock rate, this frequency (nominally 10 MHz) is also available as an output for external device synchronisation. The serial I²C bus and UART elements are clocked at a quarter of the crystal speed, although the UART can be optionally fed from a separate clock source. A final divider chain allows the timer section to work to a resolution of 10 μs.

CPU

The CPU section has exactly the same register and instruction set as the standard SCN68000, so any 68000 program can run on the SCC68070. However, since the SCC68070 is fabricated in CHMOS and has a different architecture, instruction execution times differ. Typically the SCC68070 will yield the same performance as an 8 MHz SCN68000.

The chip has similar bus timing characteristics to the 10 MHz SCN68000, but has the full bus error recovery feature of the SCN68010. This is essential in order to support a virtual memory environment using the integrated memory management unit. Since the SCC68070 incorporates three possible bus masters, namely the CPU and two DMA channels, the CPU has to enforce a bus arbitration priority protocol. This is realised in the form of a daisy chain, which can be extended off-chip. the priority order is as follows: DMA channel 1, DMA channel 2, external devices and the CPU, as the system arbiter, last.

Probably the most significant and most welcome departure from the SCN68000 design is the SCC68070's simplified interrupt structure. Unlike the SCN68000, interrupt request encoding and interrupt acknowledge decoding logic is performed by an internal interrupt handler. The SCC68070 provides seven interrupts, four of which, including NMI, are brought out of the device and reside on fixed interrupt levels. Each of the four external interrupt request lines has a dedicated interrupt acknowledge signal. Two additional latched interrupt inputs (INT1 and INT2) can be programmed to any level but must have auto-vectored responses. Interrupts from on-chip peripherals can be programmed to any level and can therefore be stacked with other internal or external interrupts. In these instances the SCC68070's interrupt daisy chain logic determines the order of priority.

MEMORY MANAGEMENT UNIT

In situations where large amounts of memory are required, such as multi-tasking or multi-user applications, the SCC68070's memory management unit (MMU) offers secure and economic support. As previously stated the chip has the bus error recovery capability required by virtual environments, allowing information to be held on disc and swapped into main memory on demand.

When enabled, the MMU translates from logical CPU addresses to physical memory locations; however, on-chip peripheral and interrupt acknowledge addresses are not translated. The MMU divides the memory space into contiguous segments and is therefore compatible with one of the operating modes of the SCC68910/20 memory access controllers (MAC). The memory protection and attribute schemes are also a subset of the methods employed by the MAC.

The MMU can operate with a maximum of either 8 or 128 segments, whose lengths are variable in 1 Kbyte multiples. Rapid address translation is achieved by an on-chip area of content addressable memory (CAM), which holds the descriptors (real addresses) of the 8 most recently used segments. Each descriptor has an associated flush ($\overline{F}$) bit. During a context switch the discarded descriptors have their 'flush' bits zeroed, effectively clearing CAM entries to make provision for newly demanded segments.

The MMU reads the CPU's virtual addresses from the internal bus and interprets them in three fields, namely: segment number, displacement and offset (see Fig.2). The segment number, which yields the segment's base address, is simultaneously compared to each CAM entry for which the 'flush' bit is false. Assuming that a match is established the displacement field selects a particular 1 Kbyte block within the segment. Finally the offset field is presented directly to memory and selects the required word.

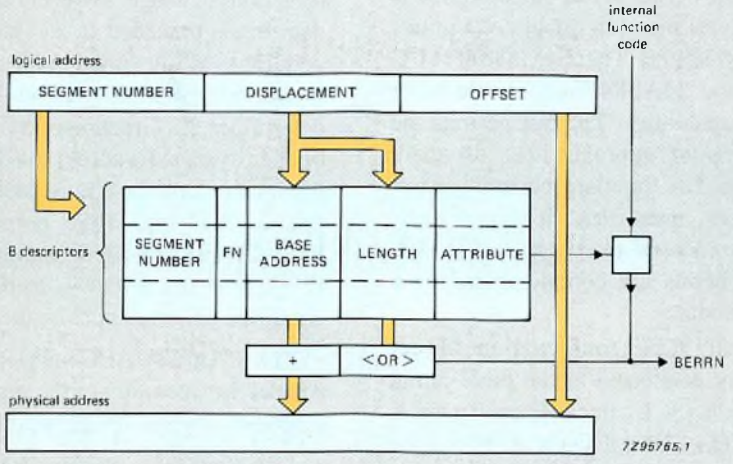


Fig.2 MMU address translation

During an address translation cycle there are two possible causes of a bus error. Either the segment's descriptor is not held on the chip or there has been a violation of one of the protection mechanisms. In response to the $\overline{\text{BERR}}$ signal, the CPU interrogates the MMU's status register to ascertain the cause and subsequently initiates the relevant exception process to remedy the situation. If the error was due to a description cache miss, possibly as a result of a context switch, the exception process has to retrieve the mapping information from system memory. The new descriptor is located in main memory, using the segment table as the base address and the segment number as the offset. A VALID/PRESENT (V/P) bit of the 8-byte descriptor indicates whether the segment is resident in main memory or mass storage. In the latter case, the entire segment has to be down-loaded prior to setting the V/P bit and writing the descriptor into a, preferably unoccupied, MMU cache slot. To avoid access to an incomplete descriptor, the segment number is fully loaded before being validated by negating the flush bit.

Protection scheme

The MMU section offers the normal protection schemes, namely: READ, WRITE, EXECUTE and SUPERVISOR. Access permission rights, as indicated on the internal function code lines, are checked against the segments attribute field. Any violation results in a bus error. In addition the SCC68070 provides a stack attribute which allows stack segments to grow dynamically from high to low addresses. Therefore, when the MMU calculates an address it has to decide whether the displacement is positive or negative, as well as checking that the displacement is within the range of the selected segment.

DIRECT MEMORY ACCESS

Direct memory access (DMA) is a common requirement of many processor-based designs, since it maximizes data throughput without loading the microprocessor. The SCC68070 answers this need by providing two channels of DMA. Channel 1 is capable of memory-to-device transfers. It comprises a 24-bit counter for memory addressing and a 16-bit counter for executing block transfers. Channel 2 has an additional 24-bit address counter giving it the further ability to conduct memory-to-memory transfers. The DMA operates in either cycle-steal or burst mode, at a maximum rate of 1,6 Mbytes/s. Both byte and word transfers are supported and therefore the DMA handles 8- and 16-bit devices.

The DMA section is fully software compatible with currently available 68430/40/50 DMA controllers, and has a similar device interface. The interface has five control signals, namely: $\overline{\text{REQ1/2}}$, $\overline{\text{ACK1/2}}$, READY ($\overline{\text{RDY}}$), DONE and DEVICE TRANSFER COMPLETE ($\overline{\text{DTC}}$). $\overline{\text{REQ1/2}}$ is asserted by a peripheral when it requires servicing, and is answered by $\overline{\text{ACK1/2}}$ indicating that the DMA has successfully arbitrated for the bus on the peripheral's behalf. $\overline{\text{ACK1/2}}$ implicitly addresses the peripheral and may also be used to gate the bus buffer circuits. In burst mode $\overline{\text{REQ1/2}}$ is an active low input. If this signal remains low at the end of the current transfer, as indicated by $\overline{\text{DTC}}$, it is interpreted as a valid request for another transfer. In cycle-steal mode, $\overline{\text{REQ1/2}}$ is recognised on its falling edge. The peripheral uses the DMA's $\overline{\text{RDY}}$ input to indicate that data is valid on the bus, or stored on the device. $\overline{\text{DONE}}$ is a bi-directional line which is asserted by the channel when the transfer count has been exhausted and the last $\overline{\text{ACK1/2}}$ has been received. When asserted by the device, $\overline{\text{DONE}}$ terminates the operation after the transfer of the current operand.

I²C BUS

I²C is a simple two-wire multi-master serial bus designed to send data and control messages between integrated circuits at a maximum rate of 100 kbit/s. The SCC68070's I²C interface is modelled on the MAB8400 microcontroller giving it master and slave capabilities. The bus permits the SCC68070 immediate access to approximately 30 extra external peripheral functions. The functions currently available include: calendar clocks, memories, display drivers, A/D-D/A converters and numerous telephony, audio and video chips. The I²C peripherals are complemented by a range of standard software modules.

Figure 3 illustrates a typical I²C bus configuration. Master and slave devices are simply connected to the bus's Serial Data (SDA) and Serial Clock (SCL) lines. Each device is allocated a unique 7-bit address, and if devices are addressed simultaneously, the lower the address the higher the priority. The current bus master is the device which initiates the transfer, either transmit or receive, and supplies the clock. To avoid a clash when two or more masters simultaneously initiate a transfer, the bus is designed to be self arbitrating. Arbitration is accomplished by making SCL and SDA wired-AND signals. Potential masters, such as the SCC68070, require the ability to listen while sending, so if a '0' is detected when a '1' was transmitted the device recognises that it has lost arbitration to a contending master. In this way arbitration is performed automatically on all data bits. Data bits are strobed, and must therefore remain stable, during each clock HIGH period. If SDA does change state while SCL is HIGH, this is interpreted as a 'start' or a 'stop' condition, depending on the direction of change. Transfers consist of a series of address and data fields preceded by a 'start' and terminated by a 'stop' condition, as illustrated in Fig.4. The address byte uses 7 bits to specify the slave device, the eighth and least significant bit determines the direction of transfer, either read or write. It is obligatory that all address and data fields are acknowledged by the receiver. At the end of each byte transfer, the transmitter sets the SDA line HIGH permitting the receiver to pull the line LOW in acknowledgement, during the ninth clock period. If a byte is not acknowledged, the master asserts the 'stop' condition prior to aborting the transfer.

The SCC68070's I²C interface comprises 5 registers which control the operation of the protocol. The registers and their functions are now briefly described.

- Data Register – converts from the CPU's parallel format to the bus's serial format and vice versa.
- Address Register – basically a comparator which holds the 68070's slave address and recognises when the device has been addressed as a slave.
- Status Register – specifies the operating mode, master or slave, transmitter or receiver, and also reveals the bus status, advising the processor of further actions to be taken.
- Control Register – the main function is to enable and disable the chip's I²C interface.
- Clock Register – selects one of 31 permissible bus clock speeds.

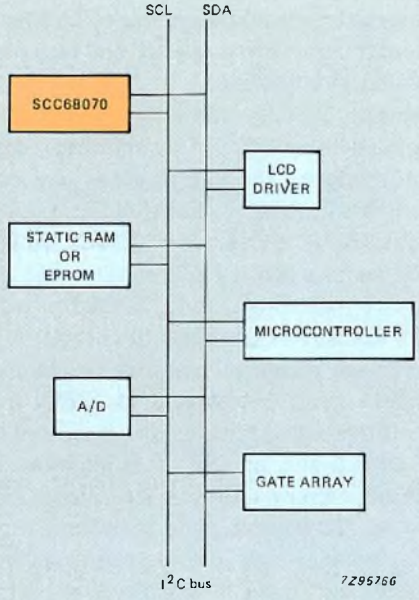


Fig.3 Typical I²C bus configuration

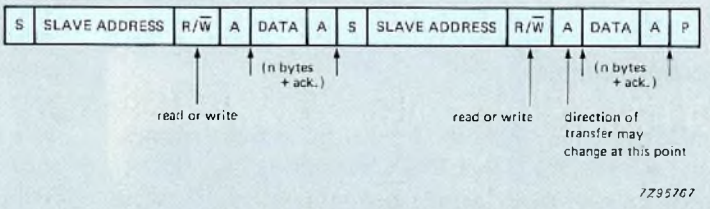


Fig.4 I²C Data transfer frame

UART

Serial communication is an essential ingredient in any modern microprocessor design. Even if the equipment is not intended to communicate remotely, a link to a control or diagnostic console is invariably required. The SCC68070 incorporates a single channel asynchronous controller (UART) based on the Signetics 2661. The asynchronous, rather than synchronous standard was favoured since the former accounts for about 80% of all current communication needs.

In compliance with the asynchronous protocol, the UART converts between serial and parallel formats, frames characters with the necessary start and stop conditions, and conducts parity generation and checking. The device works in full or half duplex modes, and can be polled or interrupt driven. When interrupt driven, the priority levels of the receive and transmit channels are defined in one of the SCC68070's interrupt Control registers. To increase throughput, the receive and transmit paths each have a character holding register.

The controller's functional block diagram is shown in Fig.5. The Operation Control and Clock Control functions merit some discussion. The Operation Control circuit comprises three registers, namely: Mode, Command and Status, which basically dictate and control the protocol's format.

The UART, via the Mode register, can be configured to operate in any of the four following ways: normal, auto-echo, local loopback and remote loopback. In normal mode, the transmit and receive paths operate independently, in all other modes the paths are in some way tied. When programmed for auto-echo, the receiver operates normally, but the CPU-to-transmitter link is disabled. The transmitter simply reflects the received data either back to the sender or possibly on to a VDU screen for the benefit of the operator. The two remaining modes are diagnostic development aids. Local loopback internally connects the transmit output to the receive input, providing a self-check mechanism. In remote loopback mode the device is used to terminate a remote unit. Instead of the received data being passed on to the CPU, it is retransmitted back to its source, thereby testing the transmission path.

The Clock Select register in the clock control functional block decides whether the transmission rate is derived from the SCC68070's system clock or from an external source. When used with a 19,66-MHz system clock or a 4,9152-MHz external clock, the register selects independent receive and transmit rates from one of 8 standard speeds. The baud rates, which are internally generated, lie in the range of 75-19200 baud. Non-standard baud rates can be accommodated using an appropriate external clock frequency.

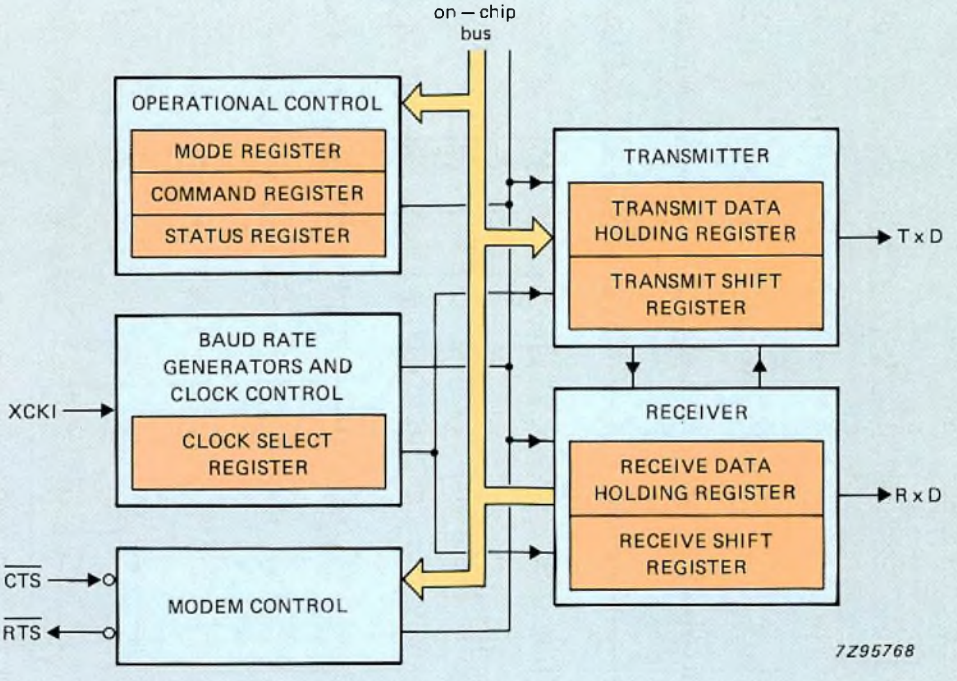


Fig.5 UART functional block diagram

TIMER

The Timer section is closely related to the 6840, and similarly comprises three 16-bit counter times (see Fig.6).

TO is a continuous counter which is automatically primed, on over-flow, with the value held in its associated reload register. T1 and T2 are identical but totally independent capture counter registers, each having a single bi-directional I/O port line. The timer block operates in one of four modes as specified in the timer control register. Dependent upon the selected operating mode the timer's status register will record the occurrence of internal or external events. All status bits, for all timers, share a single interrupt line, the enabling and prioritising of which is under CPU control. The flexibility of the architecture makes the unit applicable in virtually any design. Furthermore, since all registers can be accessed 'on the fly' the timer can switch discriminately between the four modes.

The modes which are 'Continuous', 'Match', 'Capture' and 'Counter', are now described.

In Continuous mode, timer TO is incremented every 9,6 μs. When the timer overflows it automatically restarts at the value stored in the reload register. The overflow condition (OV) appears in the status register and can, if desired, interrupt the processor.

Match mode generates pulses and can therefore replace astable and monostable circuits. The mode uses timer TO together with either of the capture counters T1 or T2, the relevant port line being configured as an output. When TO reaches the value stored in the capture register the status register's match flag (MA) is asserted and the output port is forced LOW. When TO overflows, the overflow flag is set forcing the output port HIGH. The pulse period is therefore dependent on the value in TO's reload register, while the mark-to-space ratio is governed by the match value stored in T1 or T2.

Capture mode measures external events, and again uses TO in conjunction with either counter T1 or T2. In this instance the selected timer's port line becomes an input which can monitor HIGH to LOW, LOW to HIGH or both transitions of an external signal. When the prescribed transition is recognised, the value of TO is stored in the capture register, and the capture flag (CAP) is set, interrupting the processor if desired. The actual time taken for the event to occur is calculated from the number of times TO has overflowed plus the value held in the capture register.

The final operating method, Counter mode, only requires the use of T1 or T2. As with the previous mode the port line behaves as an input which senses either or both transitions of an external logic level. If a specific number of transitions is being sought the counter can be pre-loaded so that an over-flow occurs when that number has been attained. Otherwise the counter is initially zeroed and polled by the CPU to ascertain the current number of transitions.

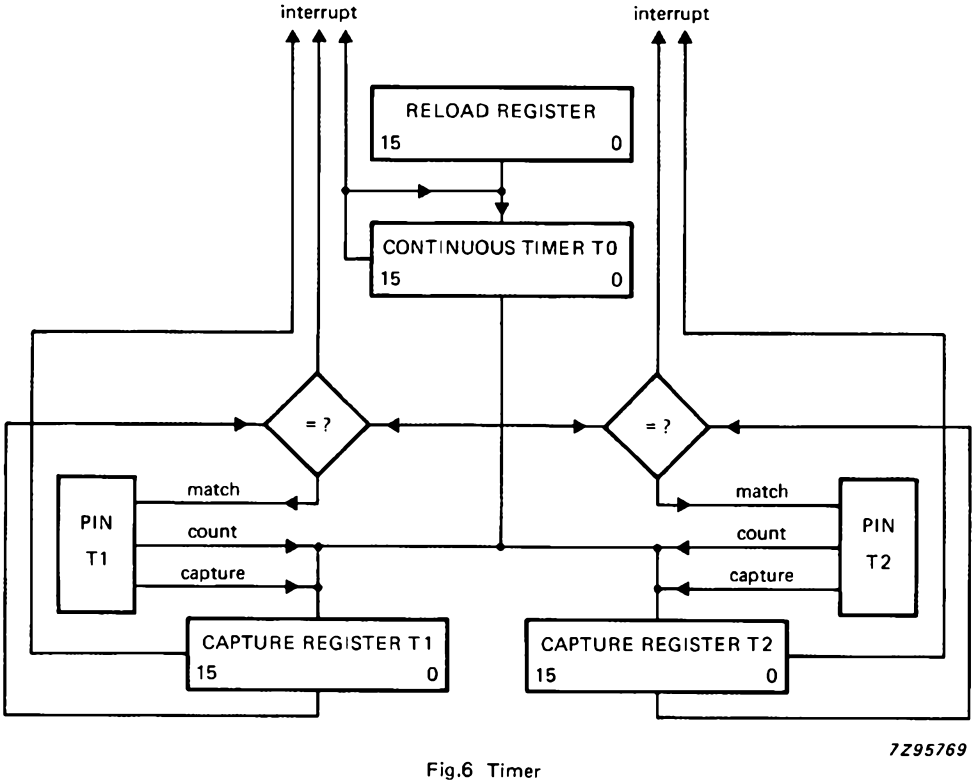


Fig.6 Timer

Cascode-driven SMPS with high-voltage darlington transistors

T. v. d. WOUW

Year by year, semiconductor manufacturers have steadily improved power transistor performance, particularly switching speeds. Higher switching frequencies have enabled designers of SMPS and h.v. converters to use smaller, cheaper wound components, but transformers and chokes are still the largest single component cost in SMPS circuits. Designers are, therefore, always looking for ways to reduce costs even further. One SMPS circuit which is very economical is the emitter drive or cascode switch. This article describes the benefits of employing high-voltage, monolithic darlington transistors in cascode driven SMPS and h.v. converters. Experiments have shown that cascode-driven switches of around 400 to 450 V which use darlington transistors are very elegant, cost-effective alternatives to base-driven switches.

PRINCIPLES OF THE EMITTER-DRIVE (CASCODE) SWITCH

First, let's examine briefly how the basic cascode circuit, shown in Fig.1, works. A low voltage power MOS or bipolar transistor (TR1) is used to interrupt the emitter current of a high-voltage transistor (TR2) to turn it off. Base current for TR2 is usually supplied from a power rail (V_B) via a resistor R. When transistor TR1 is turned on, capacitor C delivers a high base current to TR2 for fast turn-on. When TR1 is switched off, the emitter current of TR2 immediately becomes zero and the residual hole charge from the collector appears as a negative base current which first charges C before flowing through the zener diode. I_C and I_B are equal during turn-off to give a short storage time.

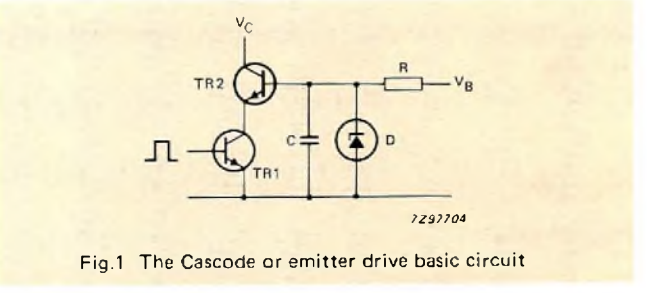


Fig.1 The Cascode or emitter drive basic circuit

Since TR1 has relatively high gain, less current is required to drive the switch than with a base driven circuit, a negative voltage is not needed for turn-off and a simple drive circuit is sufficient for TR1.

COMPARISON OF BASE AND EMITTER DRIVE BEHAVIOUR

The crucial difference between a base-driven and cascode circuit is how the output transistor is turned off. A base-driven output transistor is turned off by applying a negative base current to remove the charges in the transistor quickly while the emitter is still injecting electrons. The available conducting area around the emitter is reduced and the current density rises to a peak. The trick is to apply the negative base current sufficiently quickly to get a fast turn-off, but slow enough to avoid a large charge remaining in the collector area before the emitter stops conduction. An excessive negative base current can lead to too rapid a contraction of the conductive area under the emitter. V_{CE} then rises too quickly and a large charge is trapped in the collector region which leads to a current tail during turn-off.

In contrast, when the drive transistor of the cascode circuit is turned-off, injection of electrons ceases immediately and charge under the emitter finger flows evenly to the base contact (see Fig.2). There is no "pinching" of the conducting area and thus no peak turn-off current density. As a result, the reverse breakdown Safe Operating ARea (SOAR) for the emitter drive extends almost to V_{CESmax}.

Figures 3(a) and 3(b) show the reverse-bias SOAR characteristics for a BUW11 transistor and the BU826 darlington for both base-driven and emitter-driven circuits; the BUW11 having a similar voltage rating to that of the BU826. The cascode circuit allows higher dV_{CE}/dT and hence lower snubber losses.

Since the thickness of the collector region of a transistor is set by the rated breakdown voltage, the time needed to remove the charge increases with V_{CEmax} ratings. This leads to worse turn-off characteristics, including long current tails, in highly saturated, high-voltage transistors. In lower voltage transistors, if the ratio of V_{CEO} for the output stage and switch is small, there is little gain in overall performance obtained from a cascode configuration. From experiments on different transistor types, switching frequencies and voltage range, the cascode switch is most effective for transistors with a V_{CEO} of about 400 to 450 V and operating frequencies from 40 to 100 kHz.

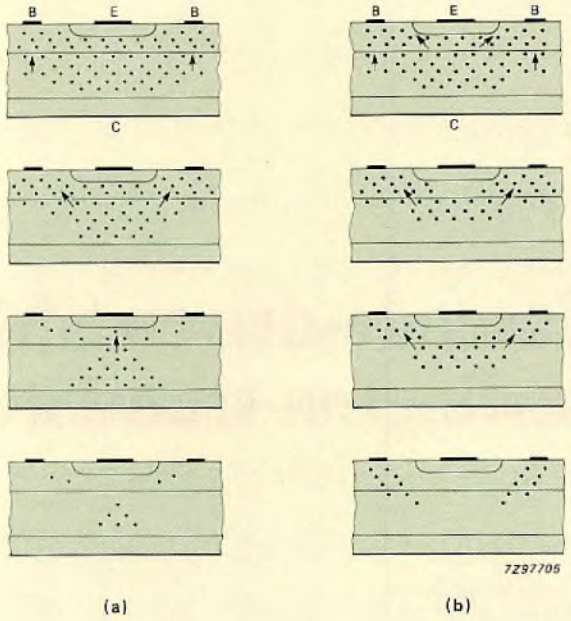


Fig.2 Turn-off behaviour
(a) for base drive, (b) for cascode drive

DARLINGTONS VERSUS TRANSISTORS

Higher gain

In a cascode configuration, we can choose a single transistor or a monolithic darlington for the output device (see Fig.4).

A darlington has an overall current gain, h_{FEdar}, that is high compared with a single transistor, and:

$$h_{FEdar} = h_{FE1} + h_{FE2} \times (h_{FE1} + 1).$$

Obviously, a much lower base current is needed to drive a darlington than the equivalent single transistor of the same output power. This is important in SMPS applications, because, at high voltages, single transistors have very low current gain. Any practical circuit design employing a single transistor must ensure that, for normal spreads in gain, the lowest gain transistor is fully turned on, which means that most transistors are significantly overdriven. A darlington also operates with a desaturated output transistor which reduces losses and shortens switching times.

Figure 5 shows the circuit diagram for a typical darlington – the BU826. In addition to the transistor pair (TR1, TR2), the darlington has a speed-up diode (D1) for fast turn-off and an efficiency diode (D2). Resistors R1 and R2 have been included to minimise leakage currents and damp the driver circuit to prevent overinging. The minimum h_{FE} of the BU826 is 45 and is typically 80 at $I_C = 2{,}5$ A.

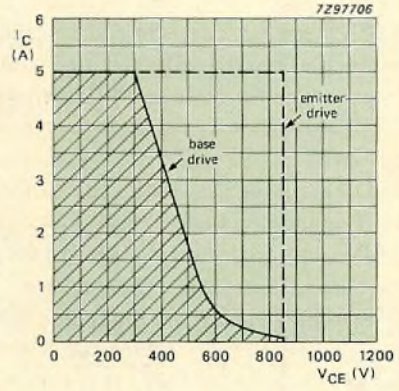


Fig.3(a) R.B. SOAR for the BUW11 transistor

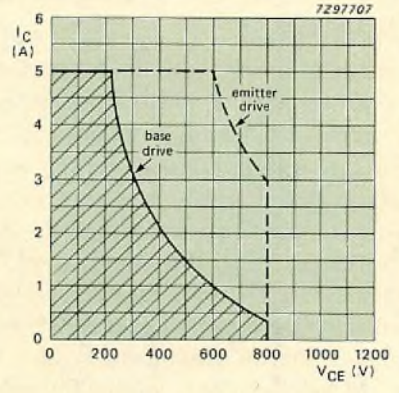


Fig.3(b) R.B. SOAR for the BU826 darlington

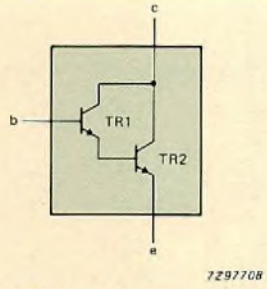


Fig.4 Darlington transistor circuit

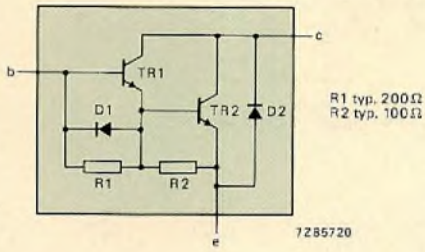


Fig.5 Circuit diagram of the BU826 darlington

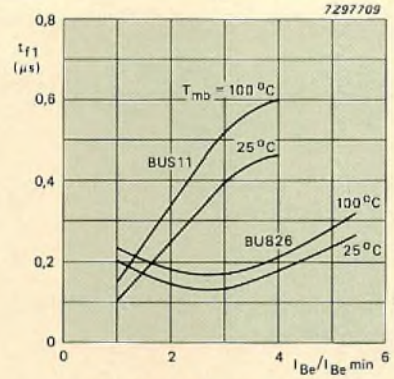


Fig.6(a) Fall time versus I_{BE} for BUS11 transistor and BU826 darlington

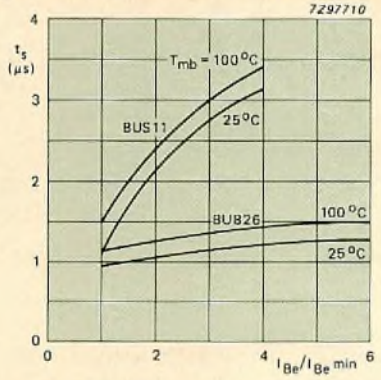


Fig.6(b) Storage time versus I_{BE} for a BUS11 transistor and BU826 darlington

I_C = 2,5 A for both BUS11 and BU826
I_{BEmin} = 250 mA for BUS11
I_{BEmin} = 30 mA for BU826

Turn off behaviour

In single transistor switches, the transistor is usually hard-saturated, a larger charge than that necessary to maintain conduction being stored in the collector region. The higher charge lengthens storage time (t_s) and fall time (t_f) during switching. In addition, a larger negative base current is needed to extract the storage charge during turn-off. The relationship for t_f, t_s and the amount of base overdrive is shown in Figs 6(a) and 6(b) for both the BUS11 transistor and the BU826 darlington.

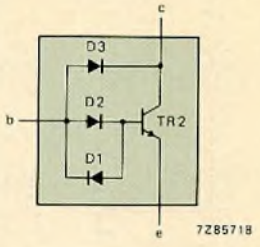


Fig.7 Simplified darlington equivalent circuit

In a darlington, the driver transistor desaturates the output transistor and prevents severe overdrive. Figure 7 shows a darlington with the driver circuit expressed as a pair of diodes D2 and D3, D2 being the base-emitter diode and D3 the base-collector diode. D1 is the speed-up diode, as before. When a darlington is turned-off, first the driver transistor will lose its main charges, then the output transistor switches and, during its storage time, the driver can lose its rest charges. As the output transistor is desaturated, its switching properties are not sensitive to the overdrive conditions shown in Fig.6.

BASE/EMITTER DRIVES COMPARED IN A 240 W CONVERTER

To assess the relative merits of base-driven and emitter-driven switching, a standard 240 W converter (Fig.8) was re-built with a sophisticated base drive circuit (Fig.9) and with an emitter driver (Fig.10). Measurements were performed at 40, 60 and 80 kHz with and without a desaturation circuit.

The sophisticated base-drive and emitter-drive versions have virtually identical performance, but the cascode circuitry is much simpler. The waveforms for base drive and emitter drive are shown in Figs 11(a) and (b).

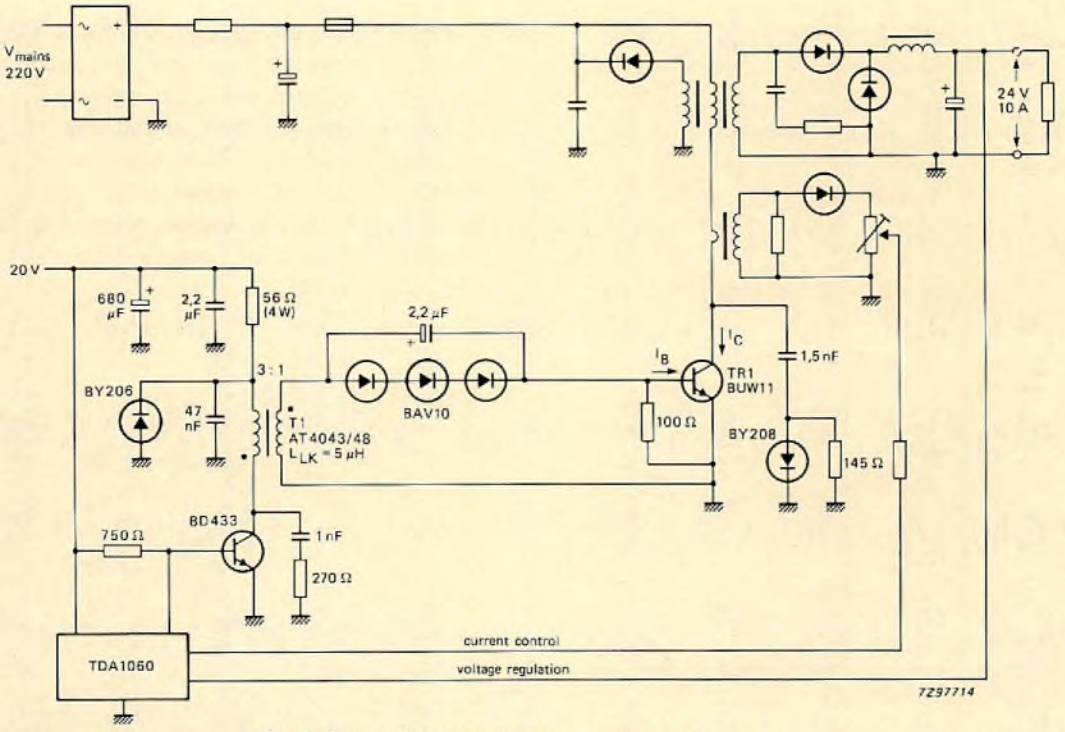


Fig.8 Original 240 W converter used for experiments

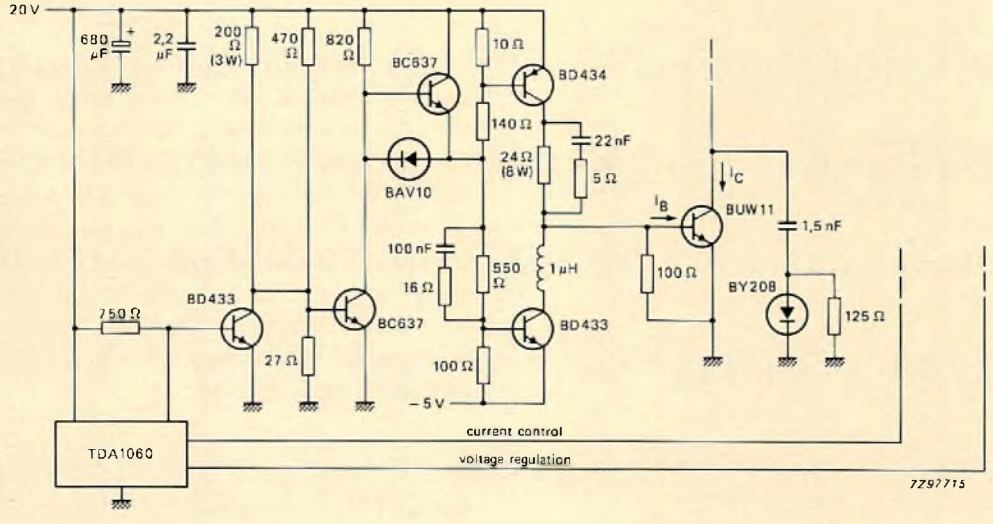


Fig.9 Improved base drive circuit

Notice how the turn-on performance of the emitter drive is better because of the booster capacitor C1. Storage time was better also: only 0,7 µs for the emitter-driven version, 2,2 µs for the base drive. Power losses for both versions are shown in Figs12(a) and (b). Differences in performance are marginal for a saturated output drive, but the emitter drive with a desaturation circuit has lower losses.

Clearly, cascode driven SMPS's have lower losses if a desaturated output circuit is included in the design, hence the reason for using a darlington, especially at high frequencies. The data yielded by these experiments was used to build a practical 200 W SMPS operating at 40 kHz. A second 100 W SMPS operating at 100 kHz has also been constructed with a BUZ71 FET as the emitter switch.

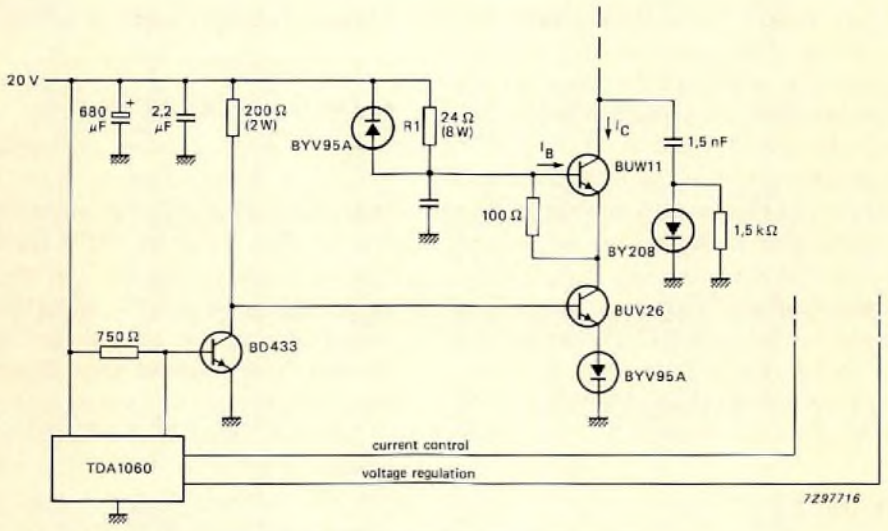


Fig.10 Cascode version of 240 W converter

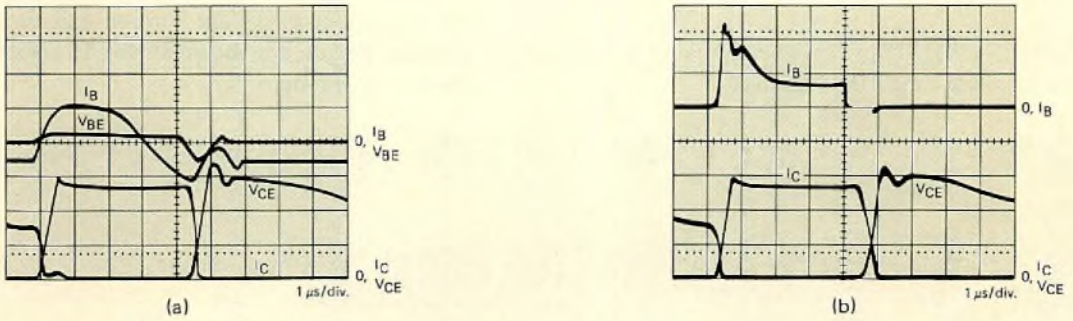


Fig.11 Switch waveforms of the BUW11,
(a) in the converter with base drive; (b) in the cascode version of the converter.
Scale: I_B and I_C = 1 A/div; V_{CE} = 200 V/div; V_{BE} = 5 V/div

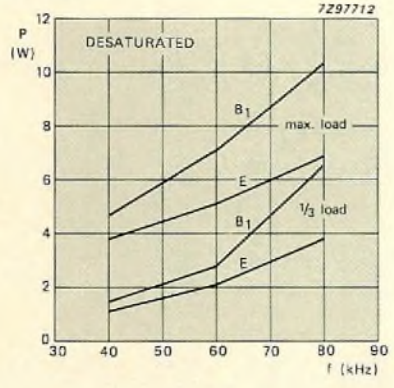


Fig.12(a) Power losses in desaturated base/cascode circuits
B_1 = base-drive circuit, E = emitter-drive circuit

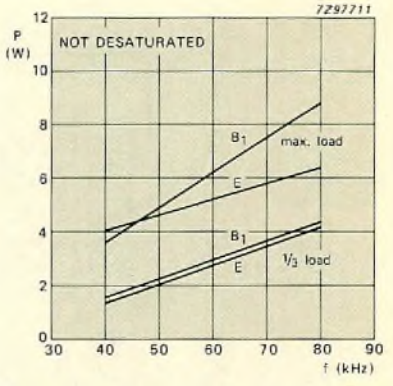


Fig.12(b) Power losses in saturated base/cascode circuits
B_1 = base-drive circuit, E = emitter-drive circuit

200 W 40 kHz CASCODE DRIVEN SMPS

Figure 13 is the circuit diagram for a 200 W SMPS. The power switch is a BU826 darlington transistor with an integral speed-up diode. The emitter of the power switch is driven by a BUV26 transistor, the switching duty factor of which is controlled by the TEA1039 IC. Diode D7 is incorporated in the emitter circuit of the BUV26 because the TEA1039 has an integral darlington output stage. The voltage developed across R13 is used as an overcurrent protection input for the TEA1039. The base circuit of the BU826 comprises base-current limiting resistor R11, C8 for providing turn-on boost current, and R12 for limiting the turn-on base current to 2 A. Diode D5 provides a current path for feeding the excess turn-off charge from the BU826 back to supply line V_S. The main properties of this SMPS design are:

- Output of 5 V/4A (max.).
- At 40 A output, 46 W losses (diode losses = 20 W).
- Efficiency = 81%.
- Current feedback to TEA1039 gives complete short-circuit protection.
- Output ripple 40 mV max.
- Transient response time = 0,45 ms max.
- Output voltage transient 0,2 V max.
- Load regulation = 0,45% max.
- Line regulation = 0,25% max.

When the mains supply is first applied to the circuit, TR1 delivers a starting current to the IC via R4. The 1 A output stage of the TEA1039 then starts the SMPS by driving the base of TR3. When the SMPS reaches steady-state operation, a secondary winding on the transformer provides supply V_S via D6 and C7, and TR1 is cut-off. Even under output short-circuit conditions, the brief current pulses through the transformer are sufficient to keep TR1 cut-off. The TEA1039 can be used to control either the frequency or the duty factor of the SMPS switching, dependent on whether pin 6 is connected to ground or left open-circuit. The RC network at pins 4 and 5 controls the switching frequency. The upper limit of the switching frequency or duty factor is set by the RC network at pin 2. The required error signal is derived from the output winding of the transformer and compared with a reference level from a μA78L02 IC before being applied to pin 3 of the TEA1039 via an opto-coupler. The turn-on and turn-off waveforms for this circuit are shown in Fig.15. Note the peak base current at turn-on.

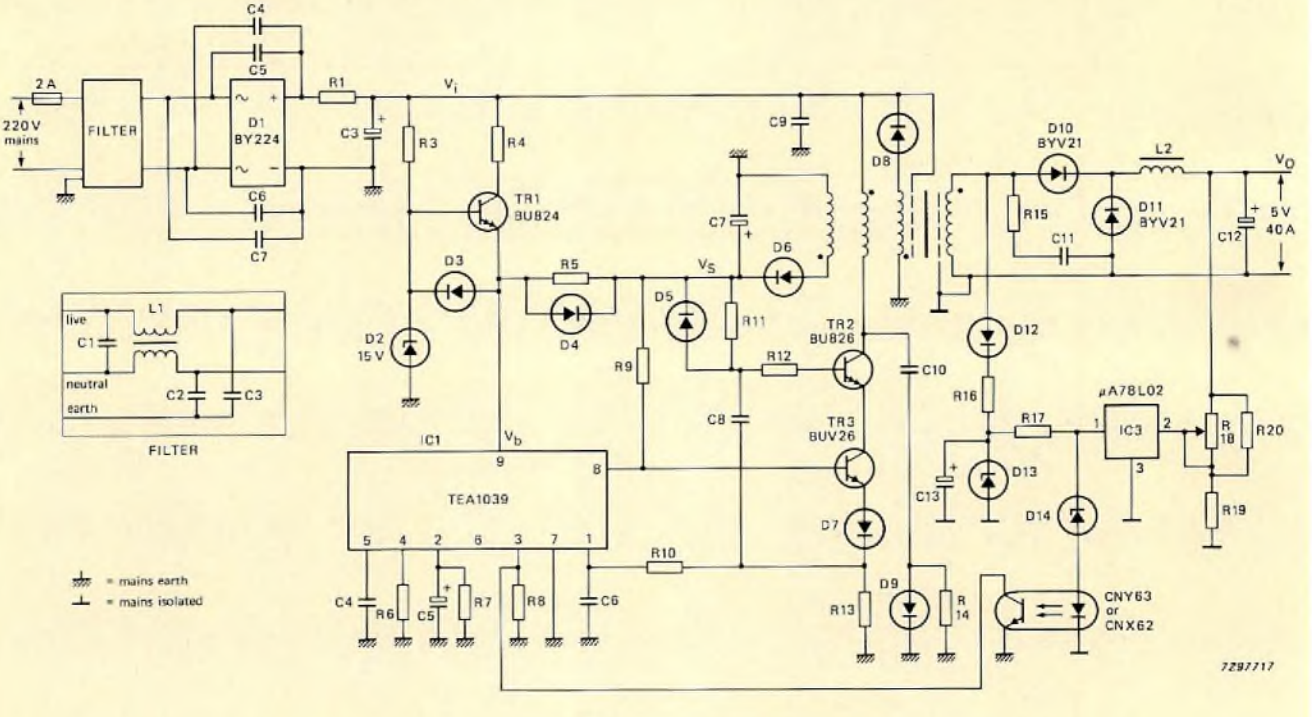


Fig.13 200 W emitter-driven forward converter using the BU826 darlington

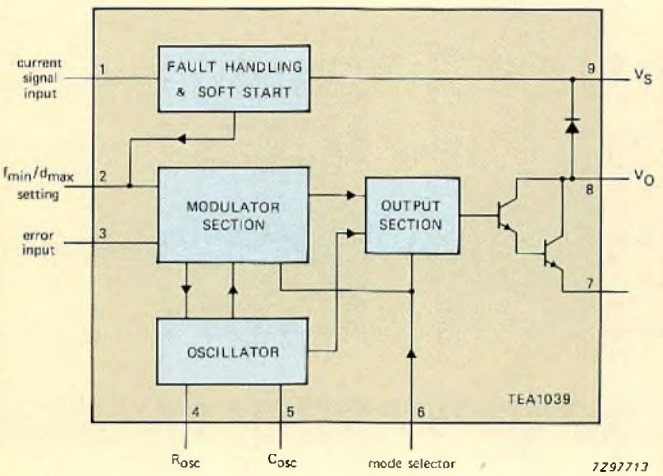


Fig.14 TEA1039 block diagram

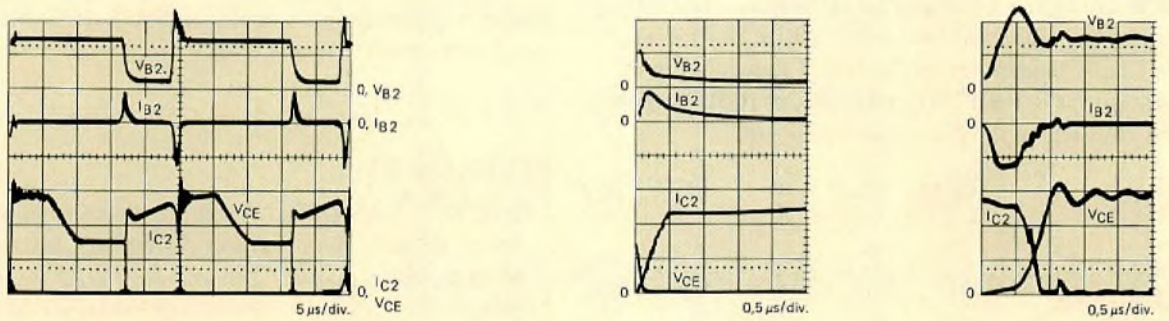


Fig.15 Turn-on/turn-off waveforms of the BU826 for the 40 kHz SMPS
Scale: V_{B2} = 20 V/div; I_{B2} = 2 A/div; V_{CE} = 200 V/div; I_{C2} = 1 A/div

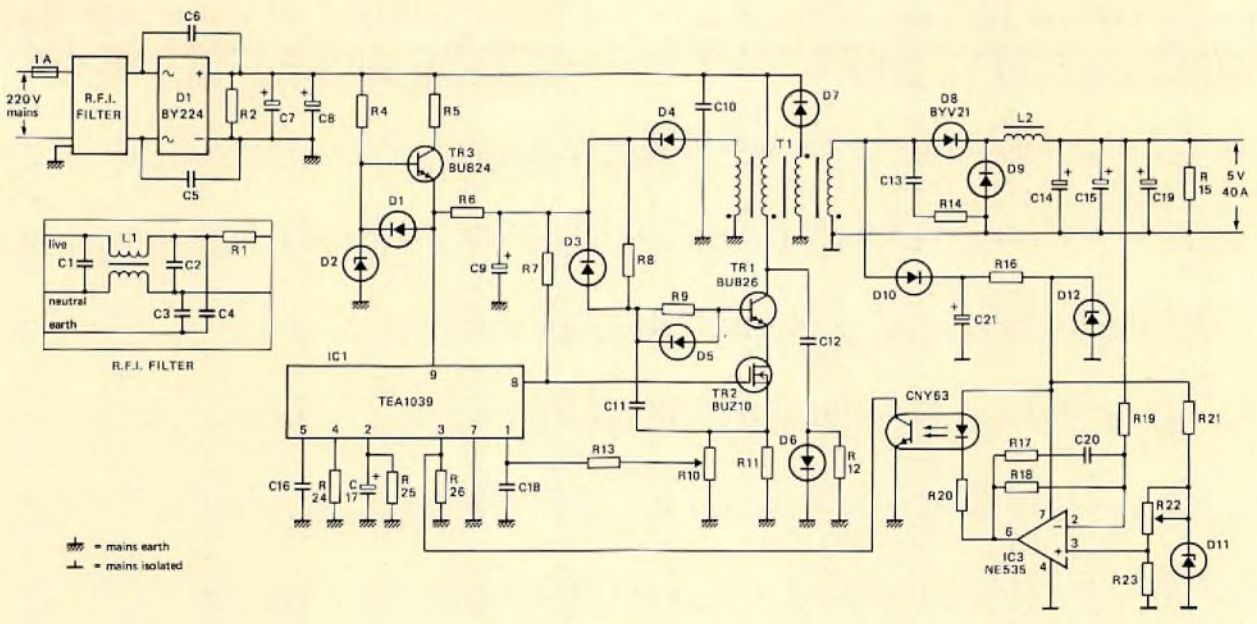


Fig.16 100 W/100 kHz cascode driven SMPS

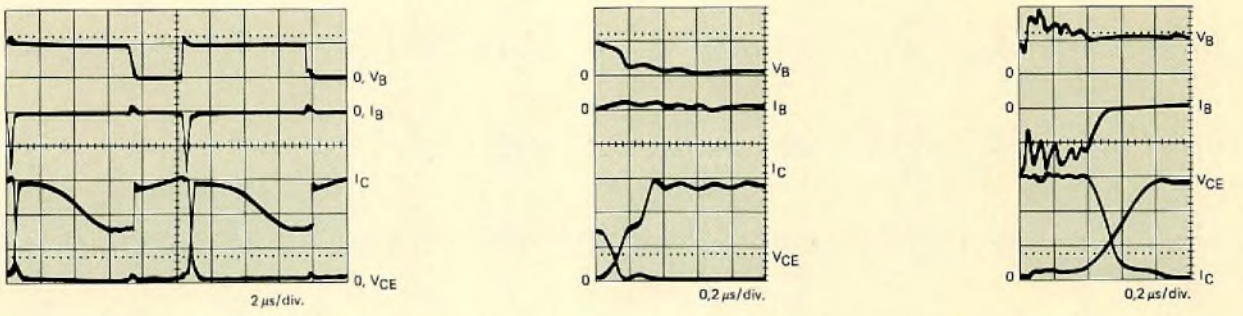


Fig.17 Waveforms for 100 kHz cascode driven SMPS
Scale: V_B = 20 V/div; I_B = 1 A/div; I_C = 0.5 A/div; V_{CE} = 200 V/div

100 kHz VERSION OF 100 W SMPS

The same basic circuit for the 40 kHz SMPS described above was used to study the behaviour of an SMPS at 100 kHz. To reduce losses in the emitter driver, a BUZ71 FET was used. The circuit diagram for this version is shown in Fig.16 and the waveforms in Fig.17. The efficiency at 100 W output power was 76%, where the diode losses were 10%.

CONCLUSIONS

The emitter-drive or cascode circuit is very effective for SMPS and h.v. conversion applications when the output stage uses a darlington transistor. The cascode circuit turns off better than a base-driven power supply and it avoids most of the current crowding problems that are a drawback of base-driven SMPS and voltage converters. The circuit is most effective for transistors with V_{CEO} between 400 V and 450 V and at frequencies above 40 kHz.

A cascode circuit is essential if bipolar devices are used at frequencies around 100 kHz for the output stage. The combination of darlington devices and the cascode switch produces a very simple and elegant SMPS design with a low component count.

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Fast controller converts large static RAMs to FIFO buffers

N. SIDDIQUE and F. KRUPECKI

Establishing channels of communication between asynchronous systems calls for first-in, first-out (FIFO) buffers to compensate for speed variations between, say, a fast processor and a slow printer. A common approach is to rely on a static RAM as the FIFO buffer. RAM buffers are relatively small, simple, and free of fall-through delays. Moreover, unlike a standard FIFO buffer, they can access memory locations at random. Such an approach, however, requires a sophisticated buffer-management scheme.

That scheme is supplied by the 74LS429, a FIFO-RAM controller that arbitrates between read and write inputs, and generates the control signals that a RAM needs. The chip is the smallest controller to directly address RAMs that have up to 65 536 addresses. Its 28-pin package cuts the space filled by FIFO RAMs. At its maximum speed of 20 MHz, the controller is also the fastest unit around.

In practice, standard LSI parts with small memories (typically 64-by-4 bits, with some 512-by-9) adequately serve systems with modest FIFO-buffering needs. Unfortunately, such standard FIFO buffers cannot handle truly "buffer-hungry" applications like data and disk systems. The number of FIFO chips required to buffer a communication-channel packet or a disk sector would be too high. System efficiency also would suffer from an inherent fall-through delay (the time it takes for data to move from input to output) incurred by each FIFO buffer.

In a RAM-based design controlled by the 74LS429 chip, however, the user can build up FIFO-buffer depth in multiples of two. Thanks to the chip's distinctive architecture, the device can join others to handle larger addressing needs. Two devices can address up to 16 megawords.

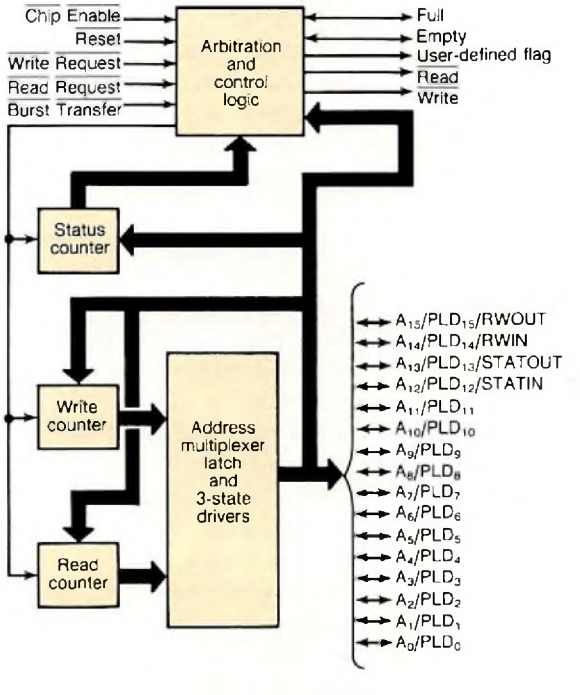


Fig.1 74LS429 FIFO-RAM controller includes read and write up-counters for generating memory addresses and a status up- and down-counter that drives full, empty, and user-defined flags. When read and write requests occur asynchronously, the arbitration logic gives priority to writing

The user can read or write data starting from any memory location, not just from address zero as in conventional FIFO-RAM controllers. The controller's preload feature makes this possible by letting the user initialize the device's counters at any value. In addition, the system designer can program the half-full, or user-defined flag (UDFLAG), to show any level. All address outputs are three-state and can drive 16 mA. The device works with any semiconductor memory.

Besides generating the control signals needed by a RAM, the chip issues full, half-full, and empty status flags, reflecting the FIFO buffer's contents. The user can also override the full and empty flags. If the full output is forced low, the next Write Request, $\overline{WR}$, removes the full flag, which stays low until the controller again detects a full condition. Similarly, if the empty output is forced low, the next Read Request, $\overline{RR}$, removes the empty flag until the device again detects an empty state.

The controller has three 16-bit counters, arbitration logic, multiplexing and latching circuitry, and the logic that generates the status flags and control signals (Fig.1). The read and write counters are up-counters that generate memory addresses. The status counter is an up- and down-counter responsible for the status flags. The chip's arbitration logic minimizes metastable conditions.

ARBITRATION PRIORITIES

Although read and write requests may occur asynchronously, the controller responds to only one at a time. The arbitration logic chooses between the two, with $\overline{WR}$ receiving priority. In fact, a device must activate an $\overline{RR}$ a certain minimum time before $\overline{WR}$, or the controller will always select $\overline{WR}$.

When a write operation starts, the contents of the write counter go to the address bus. The $\overline{Write}$ output is then asserted. To end the write cycle, the controller forces $\overline{WR}$ high, which negates the $\overline{Write}$ output and latches the address bus. The address bus outputs, however, remain valid until another read or write is requested.

When $\overline{WR}$ is disabled, the write and status counters are incremented and the read counter is unchanged. The incremented value of the write counter appears on the address bus only after a device requests another write cycle.

A read cycle is very similar to a write cycle: The controller puts the read counter's contents on the address bus and asserts the $\overline{Read}$ output. When $\overline{RR}$ is disabled, the controller increments the read counter and decrements the status counter, and the write counter does not change. As with the write cycle, the controller does not place the incremented value onto the address bus until another read cycle is requested.

The controller also has a burst transfer mode. Since this mode disables either the controller's read or write address generator, the device operates only as one or the other. This mode is handy when, for example, a fast processor and slow peripheral try to access the FIFO buffer.

In this case, the processor, while making a read or write request, forces the Burst Transfer (BT) input low, effectively blocking the peripheral's access. The processor continues reading or writing without sharing cycles with the slower peripheral. The peripheral gets access to the buffer only after the processor is finished and negates the BT input.

When the controller is reset, all counters initialize to zero. The user, however, can preload the counters with other values. For that, the address outputs become inputs that accept the preloaded data. For example, the full, empty, and user-defined flags automatically adjust according to the different preload values and the FIFO-register depths.

Designers may cascade any number of FIFO-RAM controllers. Two connected devices, for example, can address 16 megawords. In the cascade mode, the four most significant address outputs, $A_{12} - A_{15}$, transfer register information from the previous least significant device, LSD, to the next most significant device, MSD (Fig.2). As a result, they can no longer serve as address outputs. Address line A_0 of the next MSD serves as A_{12} of the previous LSD.

Each cascaded FIFO-RAM controller must know its own order in the RAM array – that is, least significant, next most significant, or most significant. Differentation is automatic when a Reset is issued while the $\overline{BT}$ input is held low. The devices with pin A_{12}/PLD_{12}/STATIN tied high become the least significant devices; those with pin A_{13}/PLD_{13}/STATOUT tied low become the most significant devices.

CASCADE FUNCTIONS ARE DIFFERENT

Output signals A_{14} and A_{15} function differently in a cascade setup. Signal A_{14} becomes Read Write Input, RWIN, and A_{15} becomes a Read Write Output, RWOUT. RWOUT sends information from a lower-order device to the next-high-order controller's RWIN so that the read and write counters of the higher-order unit increment properly – that is, they enable and disable at the right times. In other words, RWOUT of the LSD connects to RWIN of the next MSD. Exceptions are RWOUT of the MSD, which may be left unconnected, and RWIN on the LSD, which should be tied high.

Each controller's $\overline{Reset}$, $\overline{CE}$, $\overline{BT}$, $\overline{WR}$, and $\overline{RR}$ signals connect to the other device's corresponding inputs. Similarly, the three output flags connect to the other device's output flags. Either device's $\overline{Read}$ and $\overline{Write}$ outputs can assert a read or write to the memory. A $\overline{Reset}$ signal issued while $\overline{BT}$ is low initializes the cascaded devices.

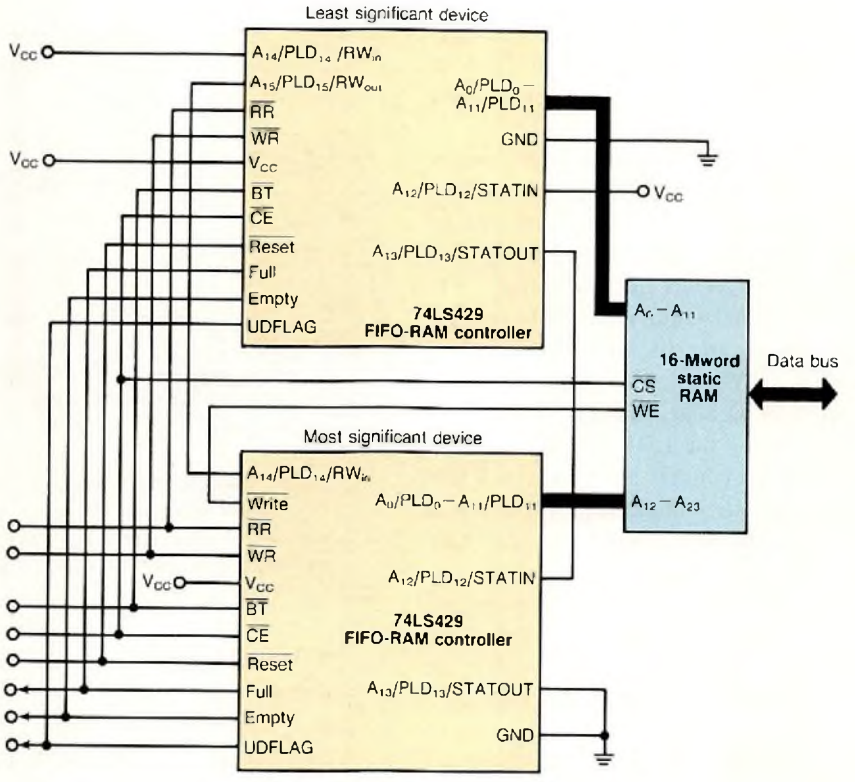


Fig.2 Cascaded controllers can increase the addressing range. For instance, a two-controller circuit can address up to 16 megawords. Cascading requires that the least significant device has its $A_{12}/PLD_{12}/STATIN$ pin tied high, while the most significant devices has its $A_{13}/PLD/STATOUT$ pin tied LOW

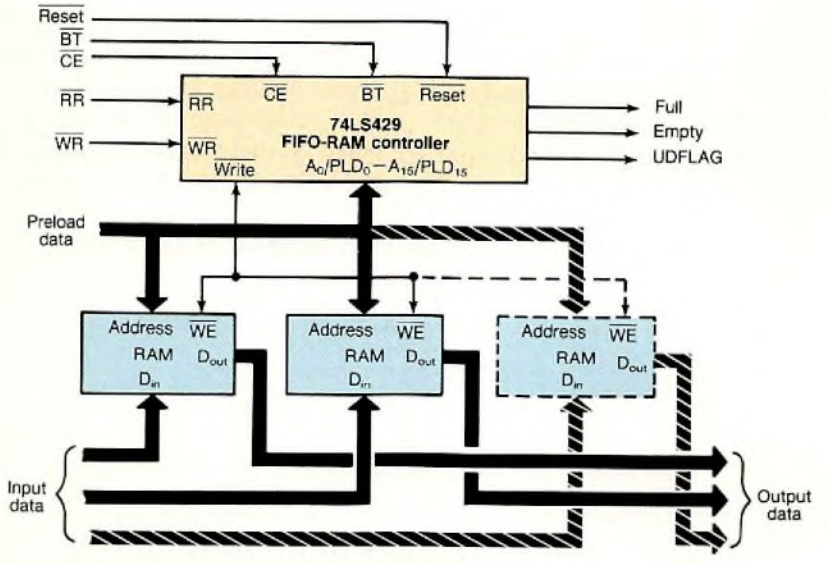


Fig.3 The length of the word the system must handle determines the number of RAMs needed. To expand word length, the static RAM chips are connected in parallel. If the address space of the RAM satisfies the desired FIFO-buffer depth, then two chips with 8-bit data buses can handle 16-bit words

At the same time, the user may preload the device's internal registers, since the STATOUT and RWOUT of every controller connected to the next MSD is low. The only difference from a one-controller system is that Pre-load Data 12, PLD_{12}, of the LSD is presented to PLD_0 of the next MSD, and so on.

The controller's read, write, and status counters cannot clock when the device's STATIN and RWIN inputs are low. After a $\overline{\text{Reset}}$, therefore, the LSD is the only device with its read, write, and status counters enabled, owing to the fact that it is the sole device with STATIN and RWIN high.

When the LSD's read counter is full or its write counter is empty, the next low-to-high transition of the $\overline{\text{RR}}$ or $\overline{\text{WR}}$, as is appropriate, generates RWOUT. This signal drives the RWIN input of the next MSD high, enabling its read and write counters. Similarly, when the LSD's status counter is full and $\overline{\text{WR}}$ is active (or the counter is empty and $\overline{\text{RR}}$ is active), the STATOUT output will go high. This signal drives the STATIN pin of the next MSD high, letting its Status counter increment or decrement.

The status flags go high only when the appropriate condition is true for the FIFO-RAM array as a whole. This is because the device's output flags have open collectors that are connected together, allowing an output flag high only when all outputs are high.

In a simple application, the device's address lines connect directly to the address inputs of two or more static RAMs serving as FIFO memories (Fig.3). The $\overline{\text{Write}}$ strobe asserts Write Enable, $\overline{\text{WE}}$, on the RAMs, leaving the $\overline{\text{Read}}$ strobe unconnected in this example.

Word length determines the number of RAM chips needed. If, for example, the addressing space of each chip equals the desired FIFO depth, and each data bus is 8 bits wide, two devices in parallel handle 16-bit words.

The preload data path lets a user initialize the controller's internal registers and program the UDFLAG to a desired level. The preload path is particularly useful in larger systems. One example contains a large FIFO memory shared among several peripherals (Fig.4). In practice, the FIFO RAM can be a main memory.

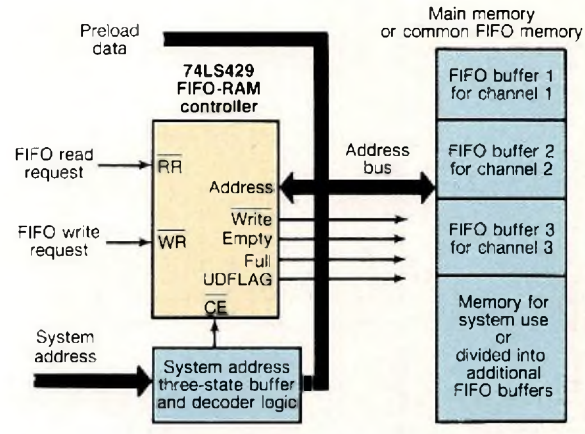


Fig.4 The controller's ability to preload data allows division of a large FIFO buffer or main memory into sections. Each section serves a different peripheral and the controller handles one segment at a time in a time-multiplexing scheme

In either circumstance, the memory consists of several segments, each serving one peripheral or channel. Using time multiplexing, one controller handles all the segments. A data packet from channel 1, for example, may arrive for storage in location FIFO 1 at address 00. If the packet does not fill FIFO 1, the controller must keep track of the external read, write, and status pointers.

The next packet may come from any channel, but the controller must store it in the appropriate memory area. Initializing the system to any starting and ending address with the preload capability makes such storage possible.

Preloading is also useful when the FIFO buffer connects two local-area networks having different packet formats. In such a case, the user must make portions of one network's message conform to a second network's format. With preloading, the user can program the controller to point to the desired portions of the message without sequencing through the entire FIFO buffer.

Managing graphics displays using a microcontroller

S. BALIGA

Of the various display technologies for computer graphics, raster scanning is by far the most popular. It does, however, demand a large memory capacity and the rapid execution of many instructions for even the simplest operation. Recent moves towards using high resolution colour graphics in CAE systems have further increased system speed requirements.

The use of an 8X401A microcontroller for refreshing and updating the screen can provide a means of both meeting these new demands and of simplifing system design. The 8X401A, one of the most complex ECL chips to be so far developed, has a powerful set of instructions for manipulating the bit-mapped memory that stores the display image. These efficient instruction sets can create graphic designs more easily than the multi-chip microcoded bit-slice approach and faster than MOS monolithic display processors.

THE 8X401A IN ACTION

The chip's power and resources are eminently demonstrated in a high-resolution colour display designed for graphics workstations (Fig.1). In this application, the workstation should be capable of displaying 16 colours simultaneously (out of a palette of 4096), each of which must be refreshed 60 times a second. The 1024-by-1024 pixel screen is non-interlaced, making the retrace time of the electron beam 25% of the total frame time. The pixel rate required for such a display is then 75% of the frame period (0,75 × 1/60 s) divided by the total number of pixels (1024 × 1024), or 83 MHz. Thus a pixel must be taken from memory to refresh the screen every 1/83 μs (i.e. every 12 ns).

The microcontroller must perform all these update and refresh tasks and must also set up a high-level software interface to a 16-bit host. Using software to select peripherals will reduce costs; hardware selection is then used only for time-critical accesses. (The chip count should be minimized to improve reliability and reduce system cost).

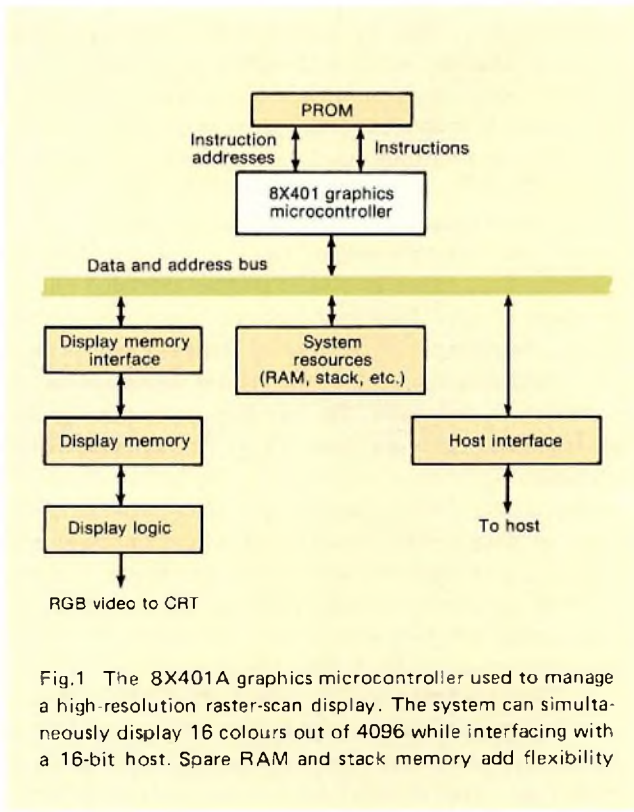


Fig.1 The 8X401A graphics microcontroller used to manage a high-resolution raster-scan display. The system can simultaneously display 16 colours out of 4096 while interfacing with a 16-bit host. Spare RAM and stack memory add flexibility

MICROCONTROLLER OPERATION

The microcontroller separates its I/O into three banks. The A and B banks are reserved for the display memory, while the C bank is assigned to host interface requirements and other system functions.

Given the display's high resolution, the workstation must be capable of storing information on over a million pixels. For the display of 16 colours, each pixel requires four bits, and the pixels themselves are arranged in groups of eight. The display memory, totalling 512 kbytes, is broken up into eight 64-kbyte planes, four each for banks A and B (Fig.2). The system can then take full advantage of the chip's bank-to-bank transfers and dual bank outputs.

The display memory sub-system is composed of 64 dual-port dynamic RAMs and two dynamic RAM controllers. The controllers generate all timing and refresh signals required by the RAMs, thereby offering a transparent memory interface with the microcontroller chip.

Accessing four planes of 64 kbytes each necessitates 16-bit addresses. Two 8X470 programmable I/O ports serve as address registers to generate the 16-bit values for each bank. Pixel addressing relies on the physical addresses contained in the port chips. However, since the host accesses pixels according to their logical X-Y addresses, the microcontroller must translate these values into physical addresses. With the display's 1024-by-1024-pixel resolution, the host uses 10 bits each for the X and Y coordinates. The microcontroller translates the 20 bits into a bank selection bit, a 16-bit byte address, and a 3-bit pixel address.

Inputs to the memory controllers are the outputs from the address ports and the $\overline{\text{Read}}$ and $\overline{\text{Write}}$ lines. Outputs include the Memory Address Complete line ($\overline{\text{CMPLT}}$) and the Access Request Acknowledge line ($\overline{\text{ACK}}$). Read/write logic ensures that $\overline{\text{Read}}$ and $\overline{\text{Write}}$ commands are removed within 50 ns of a memory cycle's completion (indicated by asserting $\overline{\text{CMPLT}}$); $\overline{\text{ACK}}$ is asserted within 50 ns of every memory access request that is granted immediately.

Since the microcontroller lacks a microprocessor's $\overline{\text{Read}}/\overline{\text{Write}}$ line, either an 8X470 port or extended microcode must be used to generate access commands for the memory controllers. For the sake of screen dynamics, two bits of extended microcode generate the $\overline{\text{Read}}$ and $\overline{\text{Write}}$ commands for each bank. The two bits are latched by the read/write logic and are then fed to the dynamic RAM controllers.

Another four 8X470s, used here as data ports, hold the 32 bits of data flowing between the microcontroller and the display memory. The time-critical access needs of the data ports are much less than those of the address ports, so that normal software selection procedures may be used to reduce system costs. Each data I/O port holds two 4-bit pixels. The translation of the host's logical addresses includes a 3-bit pixel address: the first two bits select one of the four data ports on a bank, and the least significant bit chooses one of the two 4-bit pixels within the selected port.

The organization of the data ports to hold two 4-bit pixels is different from that of the display memory. A byte in the display memory contains one bit for each of eight consecutive pixels. This reformatting of data between the data ports and the display memory is then just a matter of appropriate cross-wiring between the ports and the display memory; no additional circuitry is needed.

TIMING IS EVERYTHING

The display memory's dynamic RAMs have a 200 ns access time and a 300 ns cycle time. With the propagation delay through the dynamic RAM controller being 100 ns, the 8X401A controller's memory access path becomes 300 ns and the cycle time now totals 400 ns. With multiple memory accesses, the 100 ns dynamic RAM precharge time of the current access can be overlapped with the memory controller's propagation delay of the next cycle, giving access to the display memory every 300 ns.

Since the access path of the memory is relatively slow compared with the 100 ns instruction cycle of the microcontroller, it's inefficient to force the chip to wait for the completion of the memory cycle. For optimal performance the microcontroller should initiate a memory request and then proceed with another task. It can then return three instructions, or 300 ns later when the memory access should be complete.

However, if the microcontroller's memory request is delayed by a conflict with RAM refreshing, then the 300 ns time is no longer valid. To ensure proper operation in this case, the RAM controller refuses to assert $\overline{\text{ACK}}$, thereby halting the 8X401A and effectively causing a wait state. Then, when $\overline{\text{CMPLT}}$ is asserted, the microcontroller restarts.

The dynamic RAM input $\overline{\text{TR}}/\overline{\text{QE}}$ differentiates between row accesses for refreshing the display and random accesses for updating it. $\overline{\text{TR}}/\overline{\text{QE}}$ also enables data output for random access read cycles.

Two extended microcode bits (one for each bank) select $\overline{\text{TR}}/\overline{\text{QE}}$ for row accesses, which are required once per raster line. With a line scanned every 23 μs, the microcontroller accesses a row in display memory every scan, and is interrupted once every 23 μs to initiate the screen display process.

After the row data has been sent to the shift register of the dynamic RAMs, it can be serially shifted out to refresh the screen. Each shift delivers a new byte of information per plane, and each plane has an 8-bit shift register into which the RAM's serial output data is loaded.

The screen is refreshed from only one bank at a time. For instance, logic associated with the C bank selects bank A to refresh half the screen (say, the upper half) while placing bank B in a three-state condition (Fig.3). The bank being displayed is switched whenever a microcontroller select cycle runs on bank C at hexadecimal address FF.

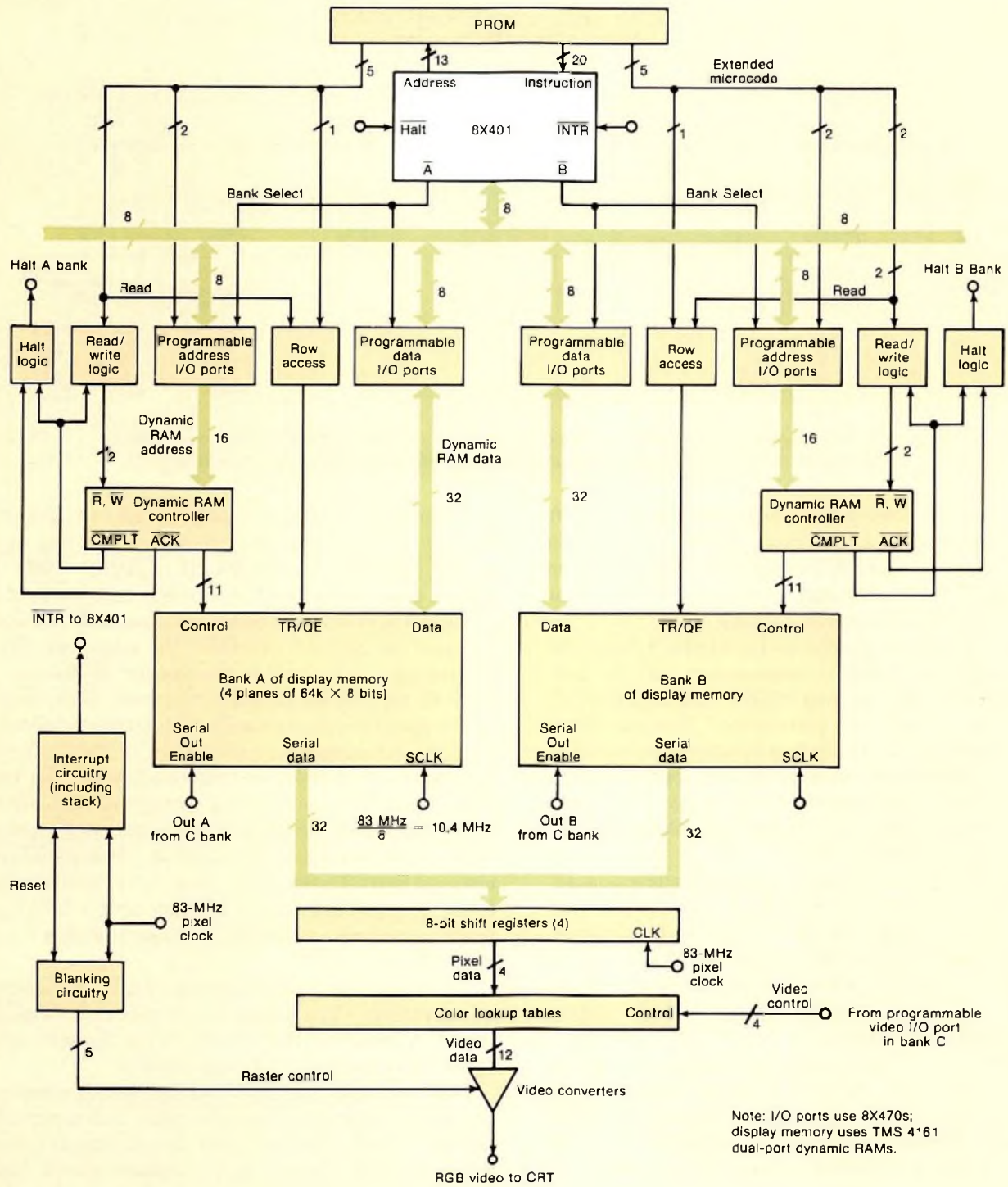


Fig.2 The 512-kbyte display memory of the display control system is divided into two banks, A and B, matching the upper and lower halves of the screen. To deliver 4-bit pixels, four 64-kbyte planes are stored in each bank, with transfers between banks controlled by the 8X401A. Data transfer between the graphics microcontroller and the two banks is via programmable I/O ports

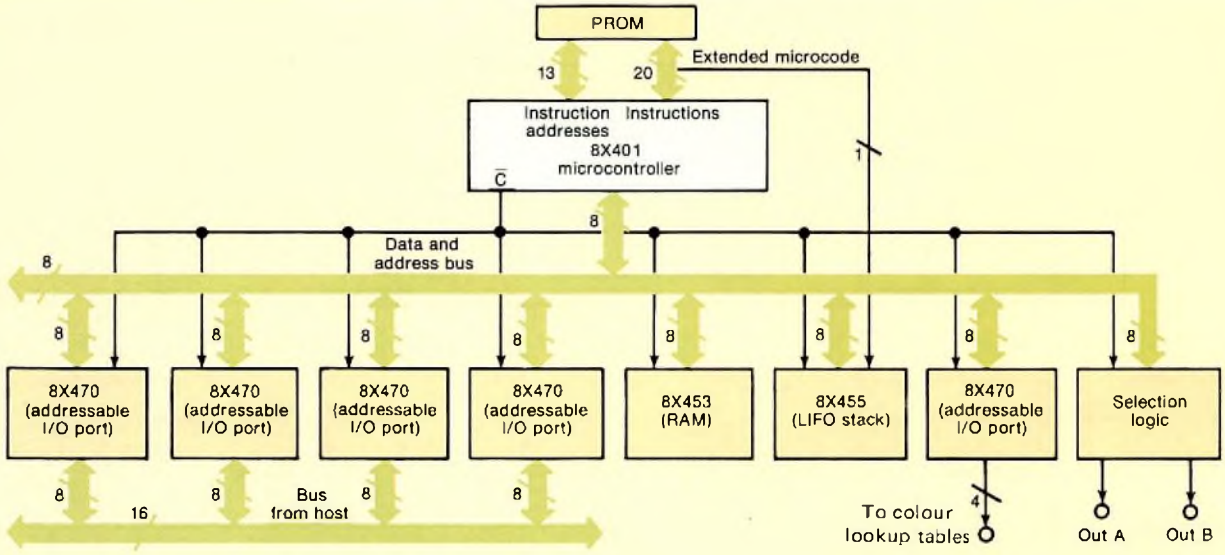


Fig.3 The display controller interfaces with the host through a third bank, C. Four 8X470 programmable I/O ports provide this function. Additional functions include the logic to select bank A or bank B

The four data bits shifted out of the high-speed shift registers combine to form a pixel, which is then sent to colour lookup tables as a 4-bit address. The output from the tables then flows into digital-to-analog converters that create the RGB video signal for the CRT.

The C bank is the graphics microcontroller's link to the host. This 16-bit processor communicates with the 8-bit microcontroller through four 8X470 programmable I/O ports on the C bank. Two ports in the C bank pass 10-bit logical addresses between the host and the microcontroller. One carries host commands while the other carries 8X401A requests. The microcontroller must access the colour lookup table to display any colour in the palette. Bank C's video port permits this access.

The 8X401A has 13 general purpose registers, and, for extra storage, an 8X453 32-byte RAM can be used in bank C. To allow the interrupt handler to save the processor state, an 8X455 stack is also used in bank C. The stack is selected by extended microcode, ensuring that the update process waits the shortest time possible for the display process to be completed.

The microcontroller's graphics system software package is less than 4 Kwords. The instructions are 31 bits long: 20 for the chip itself and 11 for extended microcode. Four 4k-by-8-bit PROMs build a 32-bit instruction word; the extra bit is reserved for future expansion of the system.

SYSTEM OPERATION

System operation is straightforward. When the microcontroller acts as the display processor, it concerns itself chiefly with updating the picture stored in the display memory. To do so, it must specify a RAM address and then manipulate RAM data. Firstly, the chip accesses either the high or the low address I/O port by asserting its extended microcode bit (ADDR HI or ADDR LOW). Secondly, it accesses a data I/O port, which it preselects. To define a read or write operation, the appropriate microcode bit must be asserted. Whenever the microcontroller is interrupted, a row access to the dynamic RAMs must be made by asserting the extended microcode signal, $\overline{TR}/\overline{QE}$.

The graphics application software for this system benefits from the bit-manipulation orientation of the controller's instruction set. With an on-board stack facilitating interrupts and calls to subroutines, along with the Execute instruction (XEC), powerful graphics code can be written. XEC is a data-dependent instruction in which one to eight bits of an internal register can replace the lower one to eight bits of an immediate address. Program control shifts to the newly formed address, and the instruction residing there is executed.

To execute the host command "Paint", the graphics microcontroller fills a portion of the screen with a specific colour. A subset of this routine, "Clear Screen", writes 0000 to every pixel in the display memory.

With the display memory's two segments, it is better to clear both segments simultaneously rather than sequentially, in half the time. Writing to both memory banks requires updating of the addresses in the registers in both banks. With the microcontroller's read-modify-write capability, coupled with its dual bank outputs, this updating takes only two instructions. The first reads an address from the low address port on the A bank. The microcontroller increments by one the ADDR LOW bit and returns the result to the low port on both the A and B banks. The second instruction reads an address from the high address port on the A bank. It then adds the carry from the ADDR

LOW operation and sends the result to the high port on both the A and B banks.

A third instruction checks bounds. Together the three instructions make up the inner loop of the algorithm for the Clear Screen routine (Fig.4 and the program). The inner loop of the routine is executed once every 16 pixels, and with over 1 million pixels in the system, the loop is executed $(1024)^2/16 = 65\,536$ times. With three instructions per loop, 196 608 instructions are executed. Ignoring the few instructions outside the loop, the calculation yields a total execution time for the Clear Screen routine of about 19,7 ms. The average clearing rate is then $(1024)^2/19{,}7$ pixels/ms or 53 million pixels per second. With extended microcode ($ABAR_L$ and $ABAR_H$) to select the A and B bank address registers, the updating of these registers can overlap the memory access time, preventing the dynamic RAMs from remaining idle between accesses. Without extended microcode, four additional instructions would be required (two each for selecting the low and high address ports). The RAMs could not then be cycled through continuously every 300 ns, reducing the average clearing rate to a much slower 23 million pixels per second.

Besides executing host commands, the graphics microcontroller IC must also refresh the CRT screen interrupt. It sets the interrupt mask, pushes the program counter onto the stack, and initiates the interrupt handler. The entire procedure takes 200 ns. The interrupt handler saves this interrupted state and then accesses a row of display memory, switching display banks through bank C if required. Finally it restores the interrupted state and clears the interrupt mask before exiting.

Servicing an interrupt takes up to 2,7 μs, making the display overhead at worst 2,7 μs/23 μs, or 12% of the time. In other words, using the design based on the 8X401A microcontroller the update process can access the display memory 88% of the time – not the 25% associated with many other designs.

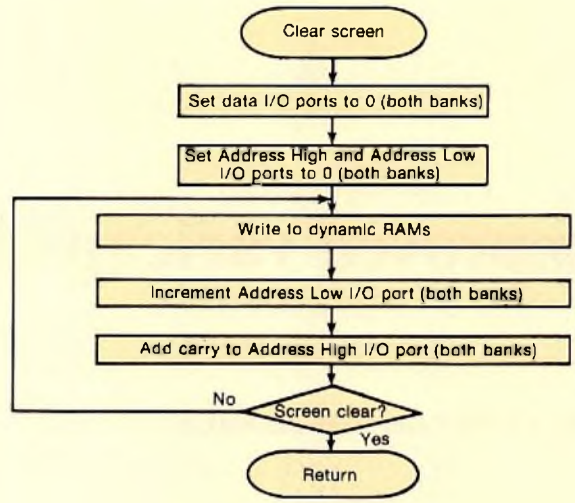


Fig.4 As can be seen from this flow chart, the Clear Screen algorithm permits both banks of the display memory to be cleared simultaneously. Sequential clearing would take twice as long

Program code for clearing the screen

```
CLEAR_SCREEN: [Select bit]    XT8     #0, R0          *R0 = 0
                              XT8     #DATA0, RC      *select DATA0 I/O port on A bank
                              XT8     #DATA0, RD      *select DATA0 I/O port on B bank
                              XT8     #0, R11         *above I/O ports = 0
                              XT8     #DATA1, RC      *
                              XT8     #DATA1, RD      *as above except
                              XT8     #0, R11         *    DATA1 I/O port
                              XT8     #DATA2, RC      *
                              XT8     #DATA2, RD      *as above except
                              XT8     #0, R11         *    DATA2 I/O port
                              XT8     #DATA3, RC      *
                              XT8     #DATA3, RD      *as above except
                              XT8     #0, R11         *    DATA3 I/O port
                              XT8     #NONE, RC       *deselect A bank
                              XT8     #NONE, RD       *deselect B bank
        ABAR_L = 1            XT8     #0, R11         *ADDR LOW I/O port on A, B banks = 0
        ABAR_H = 1            XT8     #0, R11         *ADDR HIGH I/O port on A, B banks = 0
(*Falling edge of WRITE* latches address at dynamic RAM controller*)
LOOP:   WRITE = 1
        ABAR_L = 1            ADI     R11, 1          *increment ADDR LOW I/O port on A, B banks
        ABAR_H = 1            ADC     R11, R11        *add carry to ADDR HIGH I/O port on A, B banks
                              RIF     C, LOOP         *if entire screen is not clear, go back
EXIT:
```

Note: XT8 indicates software selection; ABAR hardware selection.

Improved varicaps for tv tuners

D. ECKSTEIN and R. W. STAMER

In a modern tuner, the tv signal is fed from the aerial via tuned input filters and a MOSFET amplifier to a tuned circuit, the resonant frequency of which is adjusted by varicaps. Normally, the tuned circuit comprises a double-tuned bandpass filter whose output is then mixed with that of the local oscillator, also tuned by a varicap, to generate the required i.f. signal. For a constant i.f., the local oscillator signal has to track the filter signal, requiring matched varicaps in both tuned circuits.

In the local oscillator, the voltage (across the varicap) is the largest a.c. voltage in the tuner. The voltage can be so large that tuning non-linearity, due to the shape of the varicap's capacitance/voltage (C/V) characteristic, can cause a net deviation from the resonant frequency, detuning the circuit. This causes amplitude distortion of the i.f. mixer output signal due to mistracking of the tuned bandpass filter circuit.

Tuning non-linearity in the filter can also be a problem. Here the amplified r.f. aerial signal is at its highest level and detuning can result in cross-modulation of the signal with adjacent channels.

In the past, the effect of non-linearity was not so important; to prevent amplitude distortion, a broad filter bandwidth was used. However, to meet today's stringent interference requirements, narrower filter bandwidths are required which call for improved varicaps to increase both the Q of the filter and tuning linearity.

Some manufacturers have tried to get over this problem simply by reducing the series resistance of a varicap to increase the Q of the filter. However, this by itself is of no use since without a corresponding increase in tuning linearity, amplitude distortion increases. The real solution is to increase tuning linearity as well by optimizing the C/V characteristic, thereby reducing non-linear distortion and cross-modulation.

Over the past 20 years, new technologies and manufacturing techniques have evolved for varicaps that both reduce their series resistance and increase tuning linearity. Hand-in-hand with these improvements have come others such as:

- higher capacitance ratios for a wider tuning range
- higher frequency operation
- lower cost
- improved reliability
- closer tolerances which allow for larger groups of matched diodes.

However, improving a varicap involves a trade-off between some of these parameters. For example, shortening the depth of the epitaxial layer under the pn-junction reduces series resistance but also reduces both the breakdown voltage and the capacitance ratio. For our BB405 and BB909 varicaps we have therefore made a compromise between:

- capacitance level and capacitance ratio (tuning range)
- series resistance (Q)
- optimization of the C/V characteristic
- breakdown voltage.

LINEARITY AND THE C/V CHARACTERISTIC

The capacitance of a reverse-biased pn-junction falls as the bias is increased because the depletion regions of the junction increase, analogous to pulling the plates of a parallel-plate capacitor apart. The fall in capacitance depends upon the doping level at the depletion region boundary, and since this boundary moves with bias voltage, it also depends upon the doping profile in the semiconductor.

To determine what exactly "ideal" C/V behaviour is for a varicap diode, consider its application in the tuned circuit. With a signal voltage applied, the voltage which sets the capacitance of the varicap is the sum of the bias (d.c.) voltage and the signal (a.c.) voltage. As a result, the capacitance and the centre tuned frequency vary with signal (a.c.) amplitude. Varicap diodes that have not been optimized to allow for this produce a signal frequency that changes more during one half cycle of the signal than the other, giving a net deviation from the resonant frequency ($\Delta f = |f - f_0|$) of the tuned circuit. Figure 1 illustrates this deviation, which noticeably worsens as the signal amplitude increases.

Two problems are caused by this effect when the varicap is used in tuner circuits:

- modulation distortion of the applied signal (non-linear distortion/cross-modulation)
- detuning of the resonant circuit by signals with relatively large amplitudes (increasing the effect of tracking errors – mistracking).

So the "ideal" is a C/V characteristic giving a zero frequency deviation in the tuned circuit, irrespective of signal amplitude.

It is important to highlight the difference between linear tuning and tuning non-linearity. The former is obtained from a quadratic C/V relation, i.e. $C \propto 1/V^2$. Then since $f \propto 1/\sqrt{C}$ in a tuned circuit, $f \propto V$, i.e. a linear relation between frequency and d.c. tuning (bias) voltage.

Linear tuning has certain advantages but is not related to tuning non-linearity. This refers to the frequency deviation of a signal (superimposed on the d.c. bias) caused by non-linear effects of the C/V curve. For a small amplitude signal (as found in the older type low-Q tuned bandpass filters) a quadratic C/V relation is acceptable as the frequency deviation is negligible. However, for large signal voltages (found in local oscillators and modern high-Q tuned bandpass filters), even with a quadratic C/V relation, a frequency deviation will occur causing modulation distortion of the applied signal. Clearly, therefore, a purely quadratic relation is unsatisfactory and a more comprehensive one has to be found.

A mathematical study of varicaps shows that the normalized frequency deviation for a sinusoidal signal (and d.c. tuning voltage) across a varicap, of peak-to-peak voltage $\hat{V}$, can be approximated by:

$$\frac{\Delta f}{f} = \frac{\hat{V}^2}{2}\left[\frac{1}{8}\left(\frac{d^2C/dV^2}{C}\right) - \frac{1}{6}\left(\frac{dC/dV}{C}\right)^2\right]$$

Frequency deviation at any tuning voltage therefore depends upon the first and second derivatives of the C/V characteristic. The frequency deviation becomes zero only if:

$$C\,\frac{d^2C}{dV^2} = \frac{4}{3}\left(\frac{dC}{dV}\right)^2$$

The C/V relation which satisfies this equation is given by:

$$C = \frac{A_1}{(A_2 + V)^3}$$

where A_1 and A_2 are known constants of integration that

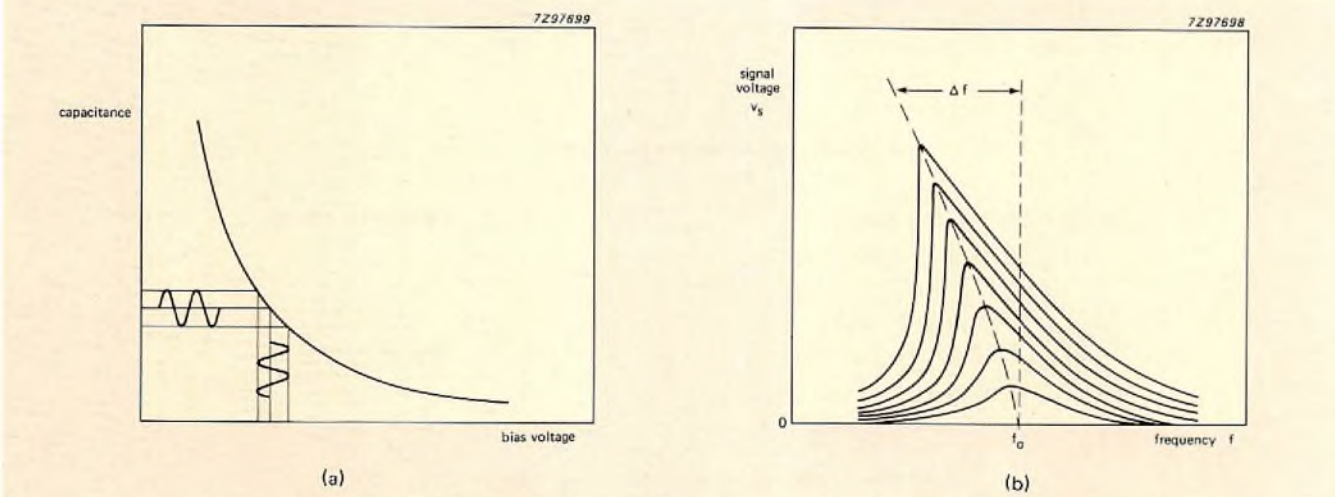
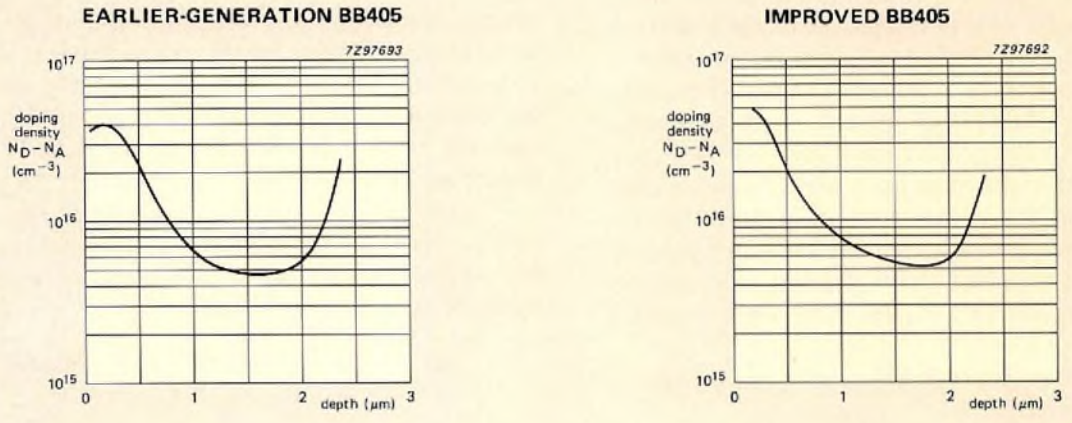


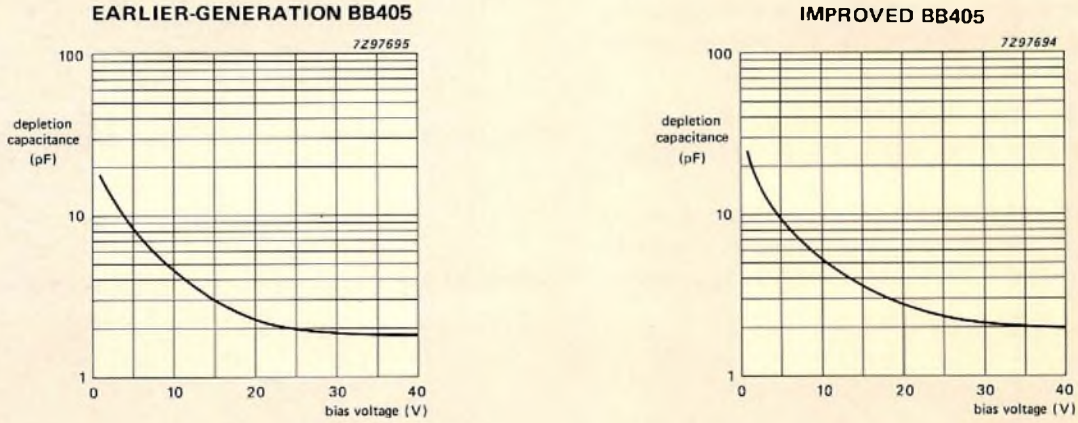
Fig.1 (a) Distortion of the signal due to a non-linear C/V characteristic; (b) Frequency deviation for sinusoidal signals of different amplitudes (depending upon the C/V characteristic the deviation can be to the left or right)

depend on production spreads, capacitance level, breakdown voltage and maximum series resistance. It's not possible to fabricate a varicap that satisfies this relation, but nevertheless it can be used to calculate a doping profile that's as near as possible to the ideal. As a result, our improved diodes have a frequency deviation that's small and nearly constant at all tuning voltages, even for large signals, whilst other parameters remain acceptable for tuner applications. Since this small deviation is almost constant, it can be compensated in the external circuit.

Figure 2 shows the doping profiles, C/V curves and large-signal frequency deviations of the earlier-generation BB405 (single n-type implanted) and the current BB405 (double n-type implanted). Although the difference in the C/V curves is not obvious on the logarithmic scales, the difference in frequency deviations is quite apparent (Fig.2(c)).



(a) Doping density as a function of distance from device surface



(b) Capacitance/voltage characteristics

(c) Frequency deviation/bias voltage characteristics

Fig.2

PRACTICAL DIODE STRUCTURES AND FABRICATION TECHNIQUES

The most common structure for a varicap diode is the hyper-abrupt junction: a thin highly-doped p-region and a thick n-region where the doping density decays rapidly away from the junction. This structure provides the widest possible capacitance range and high sensitivity to changes in bias voltage. Additionally, with this structure, the region with the highest series resistance lies in the high mobility n-region, minimizing the series resistance of the overall diode.

The BB405 is a hyper-abrupt device with an accurately profiled n-region that gives it high linearity (see Fig.3).

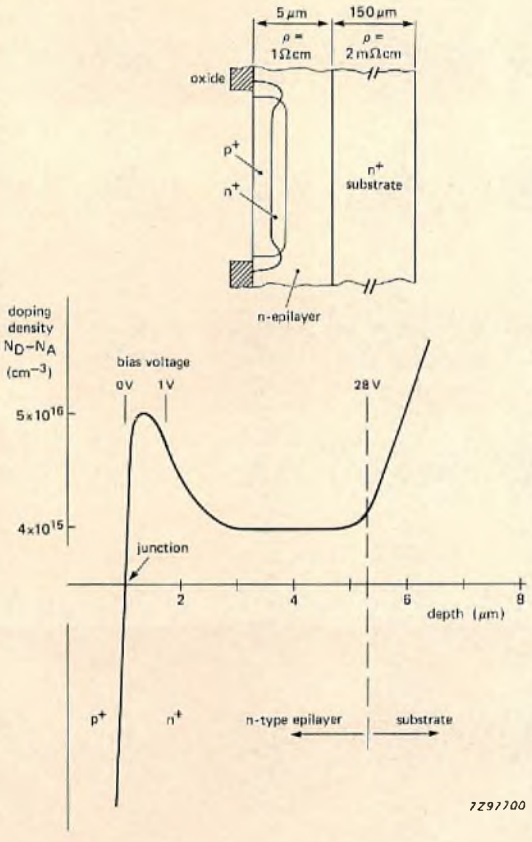


Fig.3 Structure and doping profile of the BB405

The desired n-profile is realized in two ways. Firstly, an n-type uniform low-doped epitaxial layer is grown on a highly-doped n-type silicon substrate using vapour-phase epitaxy. The thickness of the layer is that of the desired profile length (plus a little extra in which to form the p-region and to allow for silicon consumption during oxidation); any longer and the series resistance will be too high (lower Q), any shorter and the breakdown voltage will be reached before the minimum capacitance occurs. The second n-type contribution comes from two ion-implantations into the epitaxial layer followed by accurately controlled heat treatment in a diffusion furnace after each implantation. The doping density must be sufficiently high to give the correct capacitance level but not so high that it also allows the breakdown voltage to be reached before the minimum capacitance.

The dopant atom concentration of an implantation has a Gaussian distribution through the epitaxial layer. The heat treatments cause diffusion of the dopant atoms away from the distribution peak. So the final n-type doping profile is the superposition of the two implanted Gaussian profiles with a controlled redistribution, and the uniform dopant level of the epitaxial layer. The diffusion furnace also anneals crystal damage caused by the implantation.

Ion implantation has two major advantages over other doping methods – it allows independent and accurate control of the depth, spread and density of the dopant, which are particularly important in the high-field area of the junction. It also means improved linearity for negligible extra processing costs. After the first diffusion, the second implantation is made by simply resetting the energy and dose on the ion-implanter.

DIODE FABRICATION

The diode is fabricated by growing an oxide layer on top of the epitaxial layer, prior to implantation. Windows are then etched in the oxide at intervals over the wafer surface to allow the oxide to act as an implantation mask. The n-type ion beam is scanned across the wafer surface and the individual diodes are then defined by the windows. The same windows are used for the second n-type implantation. For the shallow p-type implantation, larger windows are etched in the oxide, and the process is then repeated with a p-type ion beam to give an "overlapping-p structure". This structure increases the breakdown voltage of the diodes by reducing the field around the edge of the device. Conventional and overlapping p-structures are compared in Fig.4.

Another oxide layer is then formed over the whole wafer and windows are etched around the individual diodes. This time the oxide is deposited, rather than thermally grown, to prevent any interference with the diode structure. Phosphorus is then diffused through these windows to form a "channel stopper" in the diodes and also to form phosphor glass on the wafer surface which acts as a getter. This removes charged particles (caused by contamination by metal atoms during processing) from the oxide, preventing conductive channels from forming and thus keeping the leakage current low.

The surface of the wafer is then hermetically sealed with a nitride layer and holes are etched through to the silicon for the device contacts. Following this, a titanium-silver layer is evaporated onto the surface and then silver plated to 30 μm thickness to form the contacts. Figure 5 shows schematically the main processing stages.

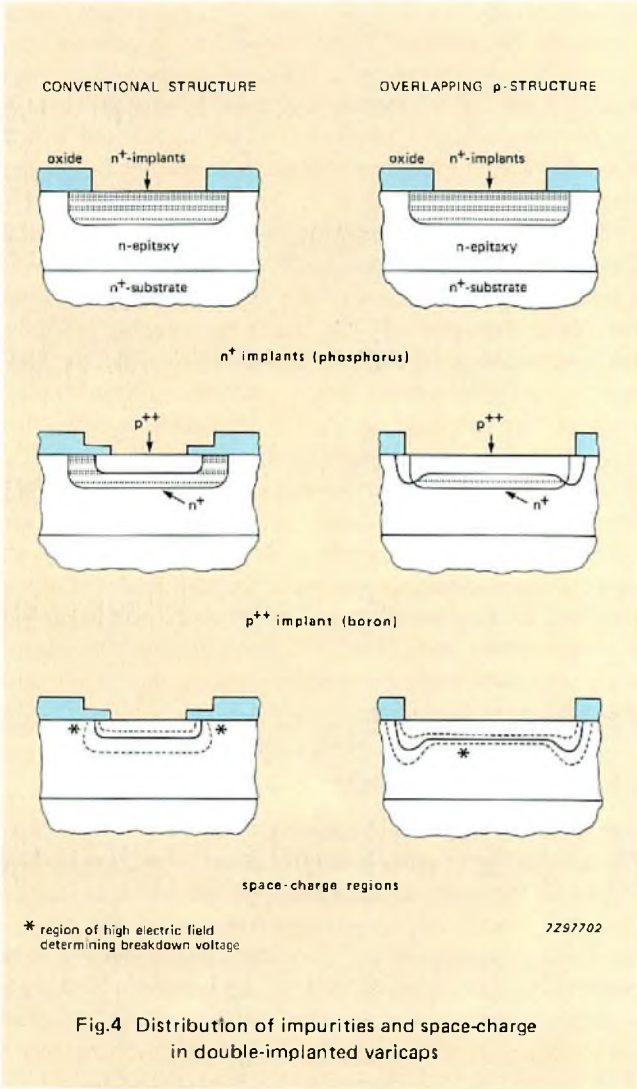


Fig.4 Distribution of impurities and space-charge in double-implanted varicaps

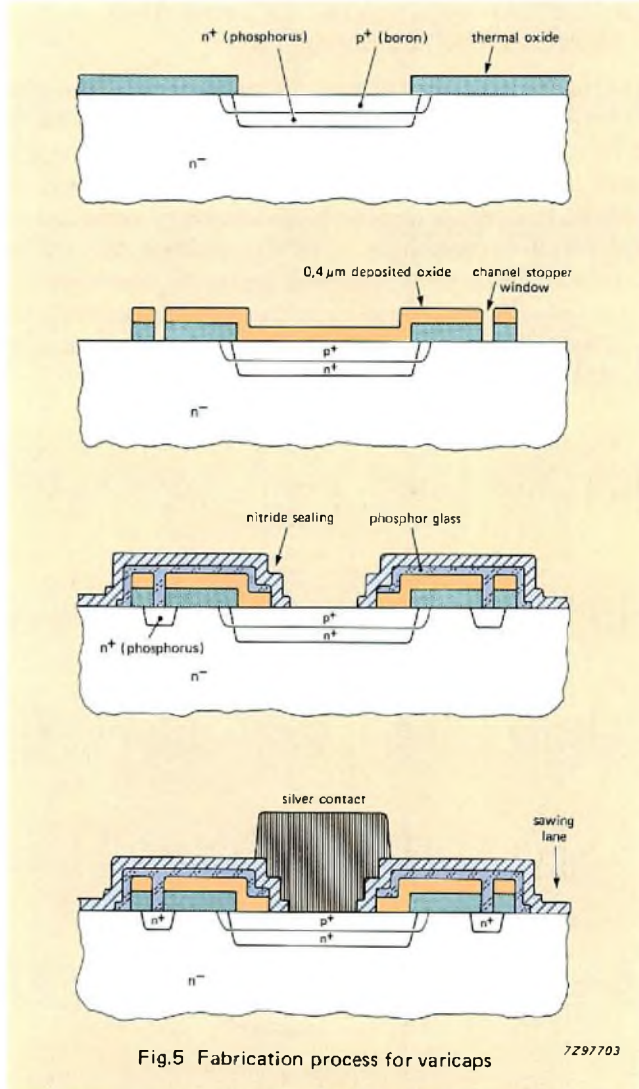


Fig.5 Fabrication process for varicaps

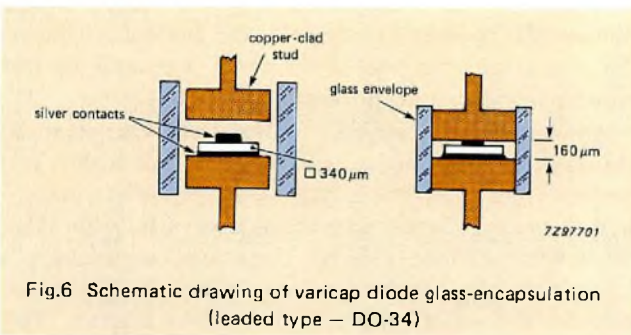


Fig.6 Schematic drawing of varicap diode glass-encapsulation (leaded type – DO-34)

Finally, the wafer is sawn into individual diodes which are then encapsulated in either glass or plastic packages. An example of a glass encapsulation is given in Fig.6. The diodes are mounted between two copper-clad studs inside a glass tube. The encapsulation is done in a hot environment so that when the diode is cooled to ambient temperature, a strong pressure contact is formed by the contraction of the envelope and the diode is hermetically sealed. The leads are then tinned electrolytically to prevent oxidation.

Post-encapsulation cooling of glass packages – contraction of envelope forms pressure contacts on varicap chip

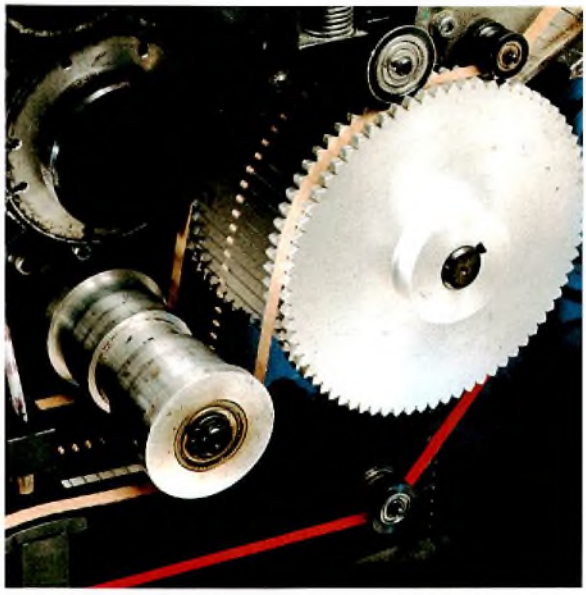
QUALITY

Every stage of the manufacturing process is subject to rigorous quality control. The silicon wafers are monitored visually, electrically and mechanically as is every completed diode. Electrical testing includes four-point probe measurements of the wafer to check sheet resistance and breakdown voltage after the implantation and diffusion stages. Also, a mercury probe is used to test the quality of the epitaxial layer and the oxide and nitride layers.

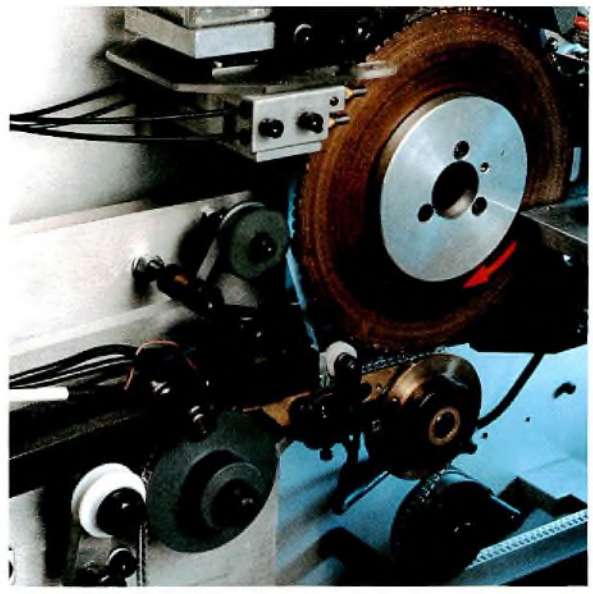
The finished varicaps are sorted into groups by computer on the basis of capacitance ratio. They're checked so that the capacitance difference between any two diodes in the same group is within 2 or 3%, over the whole voltage range. By the time the diodes are packaged into tape reels, every one will have been tested at least ten times at various grouping stages. Also, diodes in the tape reels are periodically tested. A final check ensures that all diodes in the tape are aligned with the same polarity.

Our improved varicaps for tv tuners are available in several different encapsulations, including SMD packages, see below. Full technical details are available in Data Handbooks S1 and S7.

Computer-controlled sorting of varicaps into groups with similar capacitance ratio

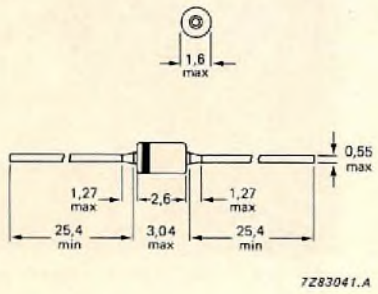
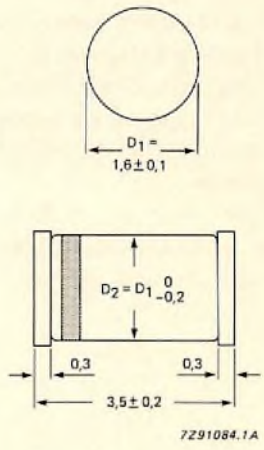
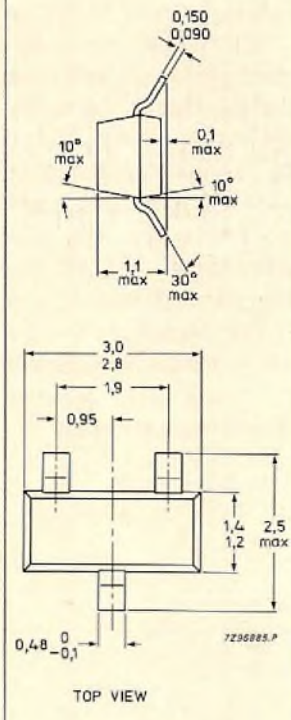


Taping of leaded varicaps (DO-34 encapsulations)



Taping of surface-mounted varicaps (MELF SOD-80 encapsulations)

Improved varicap diode range

application	leaded types	surface mounted types	
UHF VHF satellite-tv	BB405 BB909	BB215 BB219	BBY31 BBY42 BBY39
			
	DO-34	MELF SOD-80	SOT-23

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2. "Single variable-capacitance diode for a.m. car radios", Technical Publication 076, Philips Elcoma, 1982. Ordering code 9398 038 20011.

Abstracts

ACL . . . Advanced CMOS Logic that lengthens the stride of low-power systems

Advanced CMOS Logic (ACL) is fabricated in an advanced 1 μm twin-well CMOS process with recessed local oxidation, a titanium disilicide layer on the gate, source and drain areas to reduce the contact and interconnect resistance, and oxidation of the gate sidewalls for reduced capacitance. This leads to increased drive and speed equal to that of the fastest bipolar TTL logic. With 150 MHz operation and 24 mA output sink/source capability, ACL supplements the HE4000B and HCMOS logic IC ranges to allow designers to implement the outstanding CMOS benefits of wide and symmetrical noise margins, high reliability, and reduced power dissipation across the whole speed spectrum of logic circuitry.

Microcontroller eases I/O processing burden

Conventional microcontrollers are often too slow to perform the many concurrent operations necessary in modern control applications. Typical operations are testing flags on a polled or interrupt-driven basis, setting or clearing subfields within a byte boundary, high-speed data transfer, all concurrent with the need for real-time response. The 8X401 handles all these problems with its Harvard architecture which allows pipelining address generation and instruction fetching with parallel instruction decoding and execution. This concurrency results in consecutive read-modify-write cycles executed in a minimum of 150 ns, using either external or on-chip memory as either source or destination.

Breakover diodes

Breakover diodes are transient suppressors for protecting telephony equipment (subscriber and exchange) from line voltage-transients. Their operation can be compared with that of zener-diode and voltage-dependent resistor suppressors. However, unlike a zener diode, a BOD absorbs a transient at an extremely low voltage, so a BOD has a high peak-current-handling capability (40 A in air). And unlike a voltage-dependent resistor, there is no deterioration of performance over a BOD's life. Outside telephony, BODs can be used to protect terminals connected to LANs and a variety of digital communication equipment.

Quality– dry reed switches

Proven in telephone equipment and now selected by major manufacturers for automotive, computer and test-gear applications, our dry reed switches have quality built in right from development. Their quality potential is realized consistently by a zero-defect oriented production environment with constant quality improvement resulting in continual AQL reduction. Reliability of these switches now approaches $2{,}2 \times 10^{-9}$/operation.

The SCC68070: a monolithic 68000 CPU and peripherals

The recently launched SCC68070 comprises a 68000 CPU plus five of the most commonly used peripherals in a single PLCC package. With the addition of memory and a CRT controller, the device provides all the IC functions necessary for a simple personal computer or workstation. For more powerful systems, the SCC68070 is ideal as a front-end processor managing peripheral tasks.

Cascode-driven SMPS with high-voltage darlington transistors

Higher switching frequencies have enabled designers of SMPS and h.v. converters to use smaller, cheaper wound components, but transformers and chokes are still the largest single component cost in SMPS circuits. Designers, therefore, are always looking to reduce costs even further and one way of doing this is with the emitter drive or cascode switch. This article describes the use of high-voltage, monolithic darlington transistors in cascode driven SMPS and h.v. converters.

Fast controller converts large static RAMs to FIFO buffers

Static RAMs are often used as FIFO buffers to compensate for differences in speed between fast processors and peripherals, but their use requires a sophisticated buffer management scheme. This is supplied by the 74LS429 FIFO-RAM controller that arbitrates between read and write inputs and generates the RAM's control signals. The chip is currently not only the smallest controller to directly address RAMs with up to 65 536 addresses, but at its maximum speed of 20 kHz, it's also the fastest. In a RAM-based design controlled by the 74LS249, the user can build up FIFO-buffer depth in multiples of two, and its distinctive architecture allows the chip to join with others to handle large addressing needs.

Managing graphics displays using a microcontroller

Raster scanning is the most popular display technique for computer graphics but it does require a lot of memory and a great many instructions for even the simplest operation. Use of the 8X401A microcontroller to refresh and update the screen, however, provides a means of both meeting these requirements and of simplifying system design. One of the most complex ECL chips developed to date, the 8X401A has a powerful instruction set for manipulating the bit-mapped memory that stores the display image, and for creating graphic designs more easily than the multi-coded bit slice approach and faster than MOS monolithic display processors.

Improved varicaps for tv tuners

New fabrication techniques for our varicap diodes have increased their tuning linearity, reduced their series resistance and increased their capacitance ratio. For a tv tuner, they significantly reduce non-linear distortion and cross-modulation of the tv signal, offer a wider tuning range and allow higher-frequency operation. Moreover, they are less expensive and more reliable than varicaps produced by conventional fabrication techniques.

ACL: Advanced-CMOS-Logik, die den Anwendungsbereich von Systemen geringer Leistungsaufnahme erweitert

Advanced-CMOS Logik (ACL) wird in einem modernen 1-μm-CMOS-Prozess mit Zwillingswannen und lokalem Oxid hergestellt. Titansilizid-Schichten auf den Gate-, Source- und Drainelektroden reduzieren die Widerstände der Kontakte und Verbindungsleitungen. Das Seitenwandoxid des Gates minimiert parasitäre Kapazitäten. Dies führt zu einer erhöhten Treiberfähigkeit und zu einer Geschwindigkeit, die derjenigen der schnellsten bipolaren TTL-Logik gleichkommt. Mit einer maximalen Betriebsfrequenz von 150 MHz und einem Ausgangstreibervermögen von ±24 mA ergänzt ACL die Logikreihen HE4000B sowie PC74HC/HCT und gestattet dem Entwickler, die für CMOS-Logik typischen Vorzüge (breite u. symmetrische Störspannungsabstände, hohe Zuverlässigkeit und geringe Verlustleistung) im gesamten Frequenzspektrum von Logikschaltungen auszunutzen.

Microcontroller erleichert die E/A-Verarbeitung

Konventionelle Microcontroller sind oft zu langsam für die vielen, miteinander konkurrierenden Operationen, die in modernen Steuerungen ausgeführt werden müssen. Typische Operationen sind Test-Flags auf Abruf- oder Interrupt-Basis, das Setzen oder Löschen von Teilfeldern innerhalb einer Byte-Grenze und schnelle Datenübertragung, alles entsprechend dem Bedarf für Echtzeit-Betrieb. Der Mikrocontroller 8X401 bewältigt alle diese Probleme mit seiner Harvard-Architektur, die das "Pipelining" von Adressenerzeugung und Befehlsabruf mit paralleler Befehlsdecodierung und -ausführung gestattet. Diese Gleichzeitigkeit erlaubt die Ausführung eines kompletten Lese-Modifizier-Schreib-Zyklus in einer Mindestzeit von nur 150 ns. Dabei können entweder externe Speicher oder On-Chip-Speicher als Quelle oder Ziel dienen.

Breakover-Dioden

Breakover-Dioden (BOD) sind Bauelemente zum Schutz von Telefonie-Einrichtungen (beim Teilnehmer oder in Vermittlungsstellen) vor Spannungstransienten auf den Leitungen. Ihre Funktion kann mit derjenigen einer Zener-Diode oder eines spannungsabhängigen Widerstands verglichen werden. Anders als eine Zener-Diode unterdrückt eine BOD die Transienten jedoch bei einer extrem kleinen Spannung; sie ist daher in der Lage, hohe Stromspitzen (40 A in Luft) aufzunehmen. Im Gegensatz zu einem spannungsabhängigen Widerstand tritt bei der BOD keine Verschlechterung der Leistungsfähigkeit mit fortschreitender Betriebsdauer auf. Ausser in Telefonie-Einrichtungen finden BODs Anwendung in Terminals, die zu lokalen Netzen gehören, sowie in einer Vielzahl von anderen Geräten der digitalen Kommunikation.

Qualität von trockenen Reed-Kontakten

Unsere in Telefonanlagen bewährten und jetzt von grossen Herstellern für Anwendungen in Kraftfahrzeugen, Computern und Messgeräten ausgewählten Reed-Kontakte zeichnen sich durch ihre Qualität aus, die schon vom Entwicklungsstadium an überwacht wird. Diese Qualität wird durch Nullfehler-orientierte Produktion mit ständiger Verbesserung gewährleistet, womit sich eine fortgesetzte Senkung des AQL ergibt. Die Ausfallrate dieser Kontakte erreicht jetzt $2{,}2 \times 10^{-9}$ pro Schaltvorgang.

Der SCC68070, eine monolithische 68000 CPU mit peripheren Einheiten

Der kürzlich eingeführte Mikroprozessor SCC 68070 in CMOS-Technologie enthält eine 68000 CPU sowie fünf der am häufigsten verwendeten peripheren Einheiten in einem einzigen PLCC-Gehäuse. Zusammen mit einem Speicher und einem CRT/System-Controller sind alle IC-Funktionen für einen einfachen Personal Computer oder eine Workstation vorhanden. Für leistungsfähigere Systeme ist der SCC68070 ideal als Controller für Peripherie-Geräte geeignet.

SMPS mit Kaskodentreiber und Hochvolt-Darlington-Transistoren

Höhere Schaltfrequenzen haben die Entwickler von SMPS und Hochvoltkonvertern in die Lage versetzt, kleinere, kostengünstiger gewickelte Bauelemente zu verwenden, aber die Transformatoren und Drosseln sind noch immer die teuersten Einzelteile in SMPS-Schaltungen. Die Entwickler suchen daher ständig nach Wegen zur weiteren Kostensenkung, und eine Möglichkeit hierzu ist der Emittertreiber oder Kaskodenschalter. Dieser Artikel beschreibt die Anwendung monolithischer Hochvolt-Darlington-Transistoren in SMPS mit Kaskodentreibern und Hochvoltwandlern.

Schneller Controller verwandelt grosse statische RAMs in FIFO-Puffer

Statische RAMs werden oft als FIFO-Puffer verwendet; sie gleichen dabei Geschwindigkeitsunterschiede zwischen schnellen Prozessoren und Peripherieschaltungen aus. Dieses lässt sich nun mit dem FIFO-RAM-Controller 74LS429 bewerkstelligen, der zwischen Lese- und Schreibeingängen entscheidet und die Steuersignale für das RAM generiert. Der Chip ist zur Zeit nicht nur der kleinste Controller, der direkt auf RAMs mit bis zu 65536 Adressen zugreifen kann, sondern bei einer maximalen Geschwindigkeit von 20 kHz auch der schnellste. In einer Schaltung auf RAM-Basis, die vom 74LS249 gesteuert wird, kann der Anwender einen FIFO-Puffer mit Speichertiefen in Vielfachen von zwei aufbauen. Dabei kann der Chip aufgrund seiner speziellen Architektur zur Bearbeitung grosser Adressenmengen mit anderen Chips zusammenarbeitern.

Management von Grafik-Displays mit Hilfe eines Mikrocontrollers

Als geläufigstes Display-Verfahren im Bereich der Computergrafik wird Rasterdarstellung verwendet; diese erfordert jedoch viel Speicherplatz und selbst bei einfachen Operationen eine grosse Befehlsmenge. Wird ein Mikrocontroller 8X401A zum Erneuern und Fortschreiben des Schirmbildes eingesetzt, lassen sich diese Aufgaben erfüllen und lässt sich darüber hinaus der Systemaufbau vereinfachen. Eines des komplexesten ECL-Chips, die gerade entwickelt worden sind, der Mikrocontroller 8X401A, verfügt über einen leistungsfähigen Befehlssatz. So lassen sich der Bit-Mapped-Speicher, der das dargestellte Bild speichert, einfacher betreiben und grafische Entwürfe einfacher realisieren als mit der vielfach-kodierten Bit-Slice-Lösung und schneller als mit monolithischen MOS-Display-Prozessoren.

Verbesserte Kapazitätsdioden für Fernsehtuner

Durch neue Fertigungstechniken wurde die Abstimmlinearität unserer Kapazitätsdioden erhöht, ihr Serienwiderstand verringert und ihr Kapazitätsverhältnis vergrössert, In einem Fernsehtuner tragen sie wesentlich zur Herabsetzung der nichtlinearen Verzerrungen und der Kreuzmodulation des Fernsehsignals bei, bieten einen grösseren Abstimmbereich und gestatten den Betrieb bei höheren Frequenzen. Ausserdem sind sie billiger und zuverlässiger als Kapazitätsdioden, die nach konventionellen Verfahren hergestellt werden.

ACL . . . Une logique CMOS évoluée qui améliore les performances des systèmes basse puissance

La logique ACL (Advanced CMOS Logic) est réalisée selon un procédé CMOS evolué à double puits 1 μm avec oxydation locale, couche de disiliciure de titane sur les zones grille, source et drain pour réduire la résistance de contact et d'interconnexion, et oxydation des parois latérales de la grille pour réduire la capacité. Cela lui donne une puissance de sortie et une rapidité égales à celles de la logique TTL bipolaire la plus rapide. En fonctionnement à 150 MHz avec une capacité de sortie puits source de 24 mA, l'ACL complète les gammes de circuits intégrés logiques HE4000B et HCMOS, permettant ainsi aux concepteurs d'exploiter les avantages de la technologie CMOS: marges de bruit larges et symétriques, grande fiabilité et dissipation de puissance réduite dans la totalité du spectre de rapidité des circuits logiques.

Un microcontrôleur simplifie le traitement des entrées/sorties

Les microcontrôleurs classiques sont fréquemment trop lents pour exécuter simultanément les nombreuses opérations qu'exigent les applications de régulation de processus industriels modernes. Des exemples de ces opérations sont le test des drapeaux par interrogation ou avec déclenchement par interruption, la mise en place ou l'effacement de sous-zones à l'intérieur d'un octet, le transfert de données à grande vitesse, cela simultanément à des résponses en temps réel. Le 8X401 résout tous ces problèmes à l'aide de son architecture Harvard, qui autorise le traitement "pipeline" de la génération d'adresses et l'appel d'instructions avec en parallèle, leur décodage et leur exécution. Grâce à cette simultanéité, des cycles de lecture-modification-écriture consécutifs sont exécutés en un temps minimum de 150 ns, avec la possibilité d'utiliser une mémoire externe sur puce comme source ou comme destination.

Diodes BOD (Breakover Diodes)

Les diodes BOD sont des suppresseurs de transitoires destinés à protéger les équipements téléphoniques (d'abonnés et de centraux) contre les transitoires de tension de ligne. Leur fonctionnement est comparable à celui des suppresseurs à diode Zener et à varistor. Toutefois, contrairement aux diodes Zener, les BOD sont capables d'absorber des transitoires sous des tensions extrêmement faibles, de sorte qu'elles supportent des intensités de crête élevées (40 A dans l'air). Par ailleurs, contrairement aux varistors, leurs performances ne s'altèrent pas pendant leur durée de vie. En dehors de la téléphonie, les diodes BOD peuvent servir à protéger des terminaux connectés à des réseaux locaux et divers matériels de communication numérique.

Des interrupteurs à lame souple de qualité

Nos interrupteurs à lame souple, conçus pour un haut niveau de qualité, ont fait leurs preuves dans des matériels téléphoniques, et sont maintenant utilisés par d'importants fabricants dans des applications automobile, informatique et mesure. Leur qualité potentielle est concrétisée régulièrement par une production orientée vers l'absence totale de défauts et l'amélioration constante de la qualité se traduit par une réduction continuelle du NQA. La fiabilité de ces interrupteurs est actuellement voisine de $2{,}2 \times 10^{-9}$/opération.

Le SCC68070: une unité centrale 68000 monolithique avec périphériques

Le SCC68070, lancé récemment, est présenté en un seul boîtier PLCC logeant une unité centrale 68000 plus cinq des périphériques les plus couramment utilisés. Complété par une mémoire et un contrôleur vidéo, le circuit fournit toutes les fonctions integrées nécessaires à un simple ordinateur personnel ou poste de travail. Pour des systèmes plus puissants le SCC68070 est idéal comme processeur maître gérant des tâches périphériques.

Une alimentation à découpage commandée par cascode et équipée de transistors Darlington à haute tension

L'emploi de fréquences de commutation élevées a permis aux concepteurs d'alimentations à découpage et de convertisseurs haute tension d'employer des composants plus petits et moins coûteux à bobiner, mais les transformateurs et selfs constituent toujours l'élément le plus onéreux des circuits. Les concepteurs s'efforcent donc constamment de réduire davantage les coûts. Un moyen est l'emploi du commutateur d'émetteur ou commutateur à cascode. Cet article décrit l'emploi de transistors Darlington monolithiques à haute tension dans des alimentations à découpage et convertisseurs haute tension commandés par cascode.

Un contrôleur rapide convertit de grandes mémoires vives statiques en mémoires tampons FIFO

On utilise souvent des mémoires vives statiques comme tampon FIFO pour compenser les différences de rapidité entre les processeurs rapides et les périphériques, mais cela demande un système complexe de gestion du tampon. Le contrôleur FIFO-RAM 74LS429, qui joue le rôle d'arbitre entre les entrées lecture et écriture et génère les signaux de commande de la mémoire vive, répond à cet impératif. La puce sur laquelle il est réalisé est actuellement à la fois le plus petit contrôleur capable d'accéder directement à des mémoires vives jusqu'à 65 536 adresses, et aussi, à sa vitesse maximale de 20 kHz, le plus rapide. Dans un ensemble à mémoire vive commandé par le 74LS249, l'utilisateur peut augmenter la profondeur des tampons FIFO par multiples de deux et l'architecture particulière de la puce permet de l'associer à d'autres pour satisfaire de gros besoins en adressage.

Gestion de la visualisation graphique à l'aide d'un microcontrôleur

Le balayage récurrent est le procédé de visualisation le plus populaire pour l'informatique graphique, mais il nécessite beaucoup de mémoire et un grand nombre d'instructions, même pour les opérations les plus simples. Toutefois, l'emploi du microcontrôleur 8X401A pour générer et mettre à jour l'écran permet à la fois de satisfaire ces exigences et de simplifier la conception du système. Le 8X401A, une des puces les plus complexes développées à ce jour, est doté d'un puissant jeu d'instructions permettant de manipuler la mémoire de l'image en mode point et de créer des conceptions graphiques plus aisément que par la méthode à découpage bit par bit multicode et plus rapidement qu'avec les processeurs de visualisation monolithiques MOS.

Varactors améliorés pour tuners de téléviseurs

Grâce à l'emploi de nouvelles techniques de fabrication, nous avons pu augmenter la linéarité d'accord, réduire la résistance série et augmenter le rapport capacitif de nos diodes à capacité variable. Utilisées dans un tuner de télévision, elles réduisent sensiblement la distorsion non linéaire et la transmodulation du signal, elles augmentent la gamme d'accord et autorisent un fonctionnement à plus haute fréquence. En outre, elles sont moins coûteuses et plus sûres que les diodes à capacité variable produites par les procédés classiques.

ACL: Lógica CMOS avanzada que mejora los sistemas de baja potencia

Los circuitos lógicos ACL se fabrican mediante un moderno procedimiento CMOS de doble pozo de 1 µm con oxidación local rebajada, revestimiento de bisilicato de titanio en la puerta, fuente y drenador para reducir la resistencia de contacto e interconexión, y oxidación de las paredes laterales de la puerta para reducir la capacitancia, lo que produce una excitación mayor y una velocidad igual a la de los circuitos lógicos bipolares TTL más rápidos. Funciona a 150 MHz y 24 mA de capacidad de salida de sumidero/fuente, y completa la gama de circuitos integrados lógicos HE4000B y HCMOS para que los diseñadores puedan aprovecharse de los beneficios CMOS más sobresalientes de márgenes de ruido amplios y simétricos, gran seguridad, consumo reducido en todo el espectro de velocidad de los circuitos lógicos.

Microcontrolador que facilita el procesado de señales de E/S

Los microcontroladores convencionales suelen ser demasiado lentos para realizar las diversas operaciones simultáneas necesarias en las aplicaciones modernas de control. Las operaciones típicas son banderas de prueba sobre una base de sistema línea compartida por interrogación o de interrupción/excitación, establecimiento o borrado de subcampos dentro del límite de octeto, transferencia de datos de gran velocidad, todas simultáneas con la respuesta necesaria en tiempo real. El 8X401 soluciona todas esas dificultades con su arquitectura Harvard, que permite canalizar la generación de direcciones y la búsqueda de instrucciones en paralelo. Esta simultaneidad produce ciclos consecutivos de lectura-modificación-escritura que se ejecutan en un tiempo mínimo de 150 ns, empleando bien una memoria exterior o la memoria incorporada en chip como fuente o destino.

Diodos de sobre-ruptura

Los diodos de sobre-ruptura son supresores de sobretensiones que se producen en la red para la protección de aparatos telefónicos (de abonado y centralita). Su funcionamiento es comparable al de los diodos zener y a los supresores de resistencia dependiente de la tensión. Sin embargo, a diferencia de los diodos zener, este tipo de diodos (BOD) arsorbe un transitorio con una tensión extremadamente baja, es decir, tiene una capacidad de manejo de corrientes de pico elevadas (40 amperios en el aire). Y a diferencia de las resistencias dependientes de la tensión, no hay deterioro del rendimiento en su vida útil. Aparte de la telefonía, estos diodos se emplean para la protección de terminales conectados a LAN y a diversos equipos digitales de comunicación.

Calidad – conmutadores de láminas

Demostrado en aparatos telefónicos y elegido en la actualidad por los principales fabricantes de automóviles, en aplicaciones para ordenador y equipos de ensayo, nuestros conmutadores de láminas tienen calidad incorporada desde su diseño. Su potencial de calidad se realiza consistentemente en un ambiente de fabricación orientado al logro de una producción sin defectos con constante mejora de la calidad, que resulta en una reducción continua del AQL. La seguridad de estos conmutadores se acerca hoy al funcionamiento $2{,}2 \times 10^{-9}$/operación.

SCC68070: CPU 68000 monolítica y periféricos

Presentado recientemente, el SCC68070 incluye una unidad central de proceso 68000 y cinco de los periféricos más empleados en un único encapsulado PLCC. Con la adición de memoria y de un controlador TRC, este dispositivo proporciona todas las funciones de circuito integrado necesarias para un ordenador personal sencillo. En sistemas de mayor capacidad, el SCC68070 es ideal como procesador de entrada que gobierna las funciones de los periféricos.

Fuentes de alimentación conmutadas excitadas por cascodo con transistores darlington de alta tensión

Las frecuencias de conmutación más elevadas han permitido a los diseñadores de fuentes de alimentación y de convertidores de alta tensión el empleo de componentes bobinados más pequeños y más baratos, pero los transformadores y los choques siguen representando el mayor coste unitario de componentes en los circuitos SMPS. Los investigadores, por tanto, tratan constantemente de reducir costes, y un medio para este fin es el empleo de excitadores de emisor o conmutadores de cascado. Este artículo describe el empleo de transistores darlington monolíticos de alta tensión en fuentes de alimentación excitadas por cascodo y convertidores de alta tensión.

Controlador rápido que convierte las RAM grandes estáticas en memorias intermedias FIFO

Las memorias RAM estáticas se emplean a veces como memorias intermedias FIFO para compensar las diferencias de velocidad entre los procesadores rápidos y los periféricos, pero su empleo exige un esquema de gobierno de la memoria intermedia muy complejo. Este es proporcionado por el controlador FIFO-RAM 74LS499 que decide entre las señales de lectura y escritura y genera las señales de control de las RAM. El chip no sólo es el controlador más pequeño que direcciona directamente las RAM hasta 65.536 direcciones, sino que, a su velocidad máxima de 20 kHz, también es el más rápido. En un diseño basado en RAM controlada por el 74LS249, el usuario puede construir una profundidad de memoria intermedia FIFO en múltiplos de dos, y su característica arquitectura permite unir el chip a otros para manejar mayores necesidades de direccionamiento.

Manejo de visualizadores gráficos con microcontrolador

La técnica más extendida de visualización de gráficas de ordenador es la exploración de la trama, pero necesita gran cantidad de memoria y muchas instrucciones, incluso para la operación más sencilla. Sin embargo, el empleo del microcontrolador 8X401A para regenerar y actualizar la pantalla proporciona un medio que satisface estas exigencias y simplifica el diseño del sistema. El 8X401A, uno de los chips ECL más complejos que se han fabricado hasta la actualidad tiene un potente juego de instrucciones para manipular la memoria cartografiada de bits que retiene la imagen en el visualizador, y para crear gráficos con mayor facilidad que con el método de sección de bits multi-codificados y con mayor velocidad que la mayor parte de los procesadores de visualización monolíticos de estructura MOS.

Nuevos condensadores de capacidad variable para sintonizadores de TV

Las nuevas técnicas de fabricación de nuestros diodos de capacidad variable aumentan su linealidad de sintonización, reducen la resistencia en serie y aumentan la relación de capacitancia. En sintonizadores de televisión, reducen considerablemente la distorsión no lineal y la intermodulación de la señal de televisión, ofrecen una banda de sintonización más amplia y funcionamiento a frecuencias superiores. Además, son menos caros y más seguros que los que se fabrican con técnicas normales.

Authors

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Rob Croes was born in Nijmegen, and graduated in electrical engineering at 's Hertogenbosch in 1963. After military service he joined the IC development group of Philips Electronic Components and Materials Division, Nijmegen, where he is now involved in the development of CMOS commodity logic.

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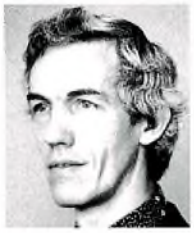

Fred Pieters was born in Eindhoven, The Netherlands, in 1932, and graduated in electronic engineering in 1968. In 1971 he became quality assurance manager for Philips dry read switches at Heerlen, The Netherlands, and since 1984 he has been marketing and quality manager for this product.

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Tinus v. d. Wouw was born in Vlijmen, The Netherlands, in 1949. After receiving an MSc degree in electronic engineering from the University of Technology, Eindhoven, he joined Philips' Electronic Components and Materials Division, Nijmegen, in 1979, initially working in the development group for high-voltage transistors. He is currently working in the applications group for high-voltage devices at Mullard, Hazel Grove, with particular interest in high-voltage transistors and darlingtons.

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PROFESSIONAL TUBES

Industrial cathode-ray tubes
Photomultiplier tubes
Geiger Müller tubes
Transmitting tubes
Microwave devices
Reed switches

MATERIALS

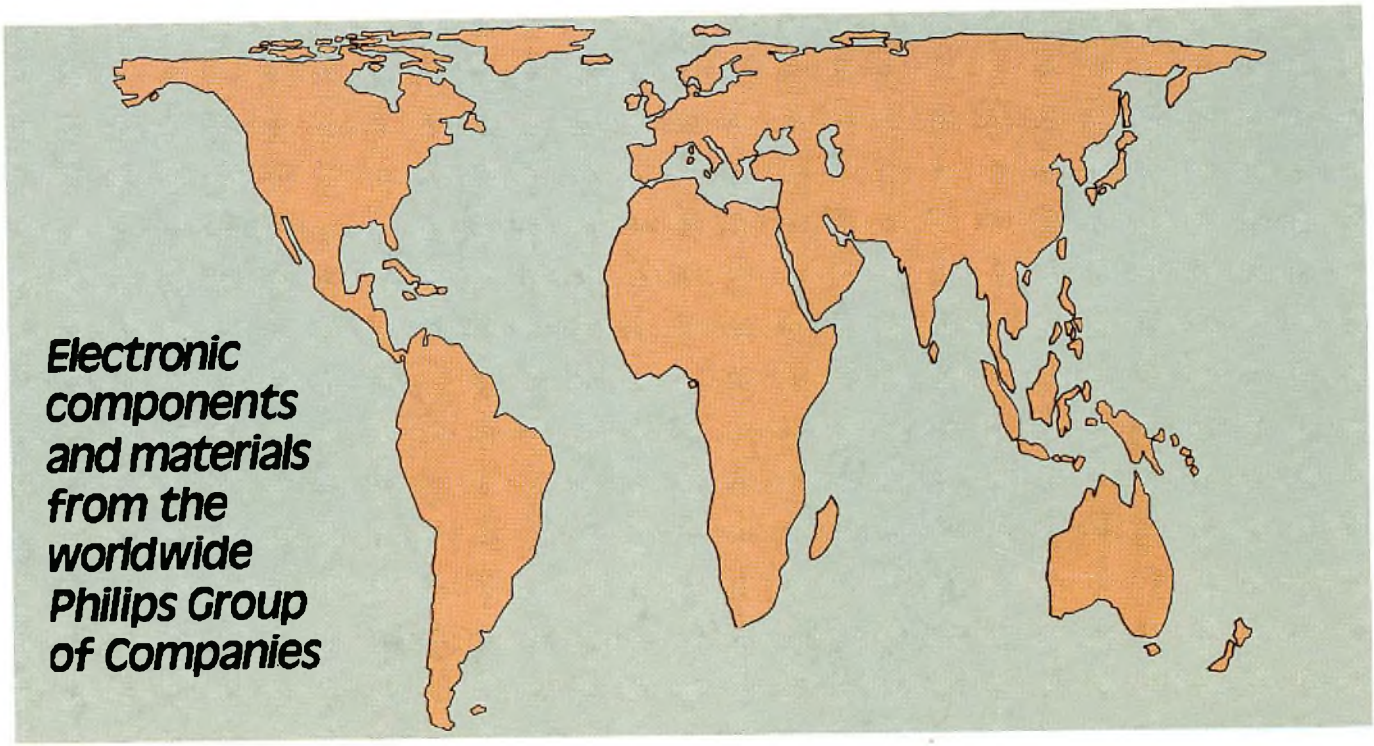
Ferroxcube products
Permanent magnets
Piezoelectric products
White ceramic products

PASSIVE COMPONENTS

Ceramic, film and foil capacitors
Electrolytic capacitors
Fixed resistors
Variable capacitors
Potentiometers and resistor trimmers
Varistors, thermistors and sensors
Delay lines
Piezoelectric quartz devices

ASSEMBLIES

Loudspeakers
Tuners
Printed circuit boards
Variable transformers



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