



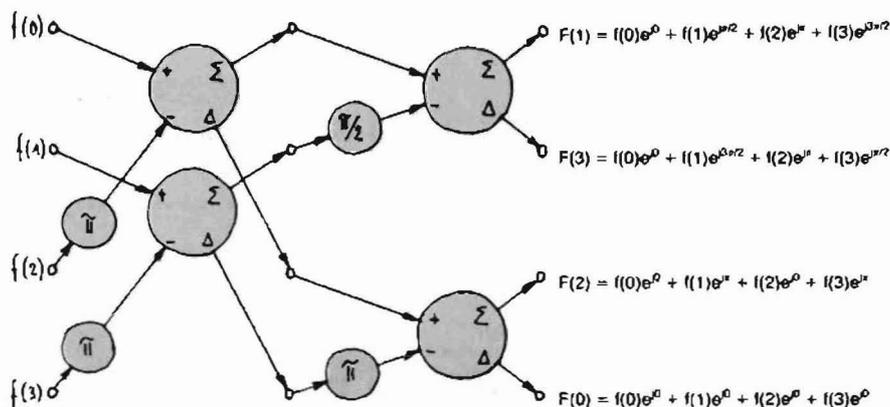
VHF

# communications

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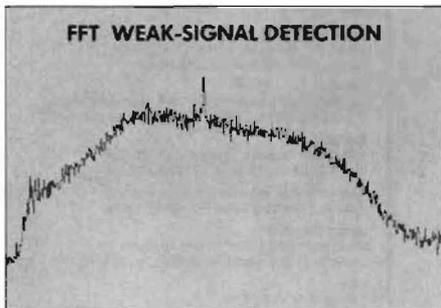
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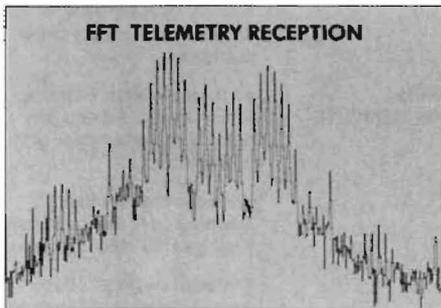
FFT BUTTERFLY OPERATION

# DSP

FFT WEAK-SIGNAL DETECTION



FFT TELEMETRY RECEPTION





# VHF communications

A Publication for the Radio Amateur  
Especially Covering VHF, UHF, and Microwaves

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Dear reader,

with effect from the first edition 1991, KM PUBLICATIONS, our former English representative, will take over the production and publication of VHF COMMUNICATIONS. The representatives in the various countries will remain the same.

In addition to continuing the production of the German parent magazine "UKW-BERICHTE", the firm of T. Bittan OHG will be one of the representatives of KM PUBLICATIONS. VHF COMMUNICATIONS back issues and the blue binders, as well as kits and ancillary equipment are still obtainable from us or via our representatives.

The customers who paid already for the 1991 and/or the 1992 subscription will be supplied by us without request.

I wish you happy hours in reading VHF COMMUNICATIONS.

With kind 73,

Corrie Bittan, editor





Matjaž Vidmar, YT3MV

## Amateur-Radio Applications of the Fast Fourier Transform Part 2 a

### 3. THE FAST FOURIER TRANSFORM (FFT) ALGORITHM

The Discrete Fourier Transform supplies a very useful result, but unfortunately requires a very large number of computations on a digital computer or a very large number of components if performed by an analog circuit. A more efficient algorithm that provides exactly the same result as DFT with a considerably smaller effort required is called the Fast Fourier Transform. As an example, to compute a 1024 data point DFT the FFT algorithm requires about 200 times less computations (or analog components) than a straight-forward DFT. Further, the number of compu-

tations required in the FFT algorithm is only proportional to  $N/2 \cdot \log_2(N)$ . The FFT algorithm can therefore be performed on a very large number of data samples without significantly increasing the number of computations per sample.

The basic building block of the FFT algorithm is called a "butterfly" operation. A "butterfly" operation consists of a phase-shift operation and a sum/difference operation. It operates on two input variables and produces two results. A single "butterfly" operation can already compute a 2-point FFT, as shown in **fig. 3.1**. In the case of a 2-point FFT, the two input variables are the input data to the FFT algorithm and the two results are already the result of the algorithm. The phase shift is equal to  $\pi$  in this case.

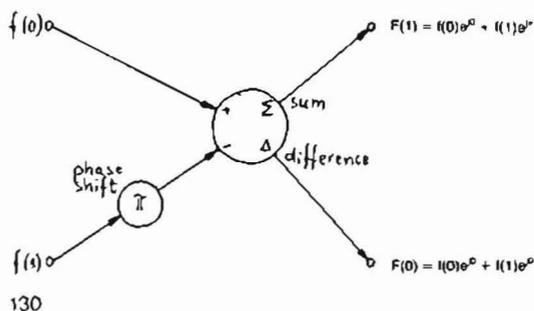


Fig. 3.1.:  
Two-point FFT – a single  
"butterfly" operation

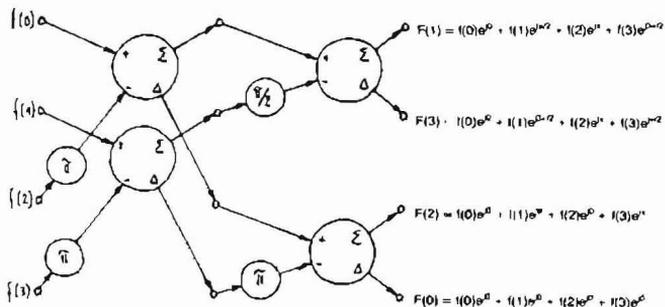


Fig. 3.2: Four-point FFT, computed each using two "butterfly" operations

Fig. 3.2. shows how a 4-point FFT works. A 4-point FFT is computed in two stages. Each stage includes two "butterfly" operations. In the first stage, all phase shifts are equal to  $\pi$ . In the second stage, the phase shifts are  $\pi/2$  and  $\pi$ . Note that each output of the first stage "butterflies" is fed to exactly one input of the second stage "butterflies". Considering the periodicity of the complex exponent function, the four outputs correspond exactly to the result obtained with a straightforward DFT, the latter, however, requires

16 phase shifts (8 if one does not consider zero phase shifts) compared to the 4 phase shifts of the FFT algorithm.

Similarly, a 8-point FFT is computed in three stages as shown in fig. 3.3. Each stage includes 4 "butterfly" operations. Again, in the first stage all phase shifts are equal to  $\pi$ . In the second stage the phase shifts are  $\pi/2$  and  $\pi$ . In the third stage the phase shifts are  $\pi/4$ ,  $\pi/2$ ,  $3\pi/4$  and  $\pi$ . The algorithm block diagram follows a regular pattern too, suggesting that a FFT algorithm working on

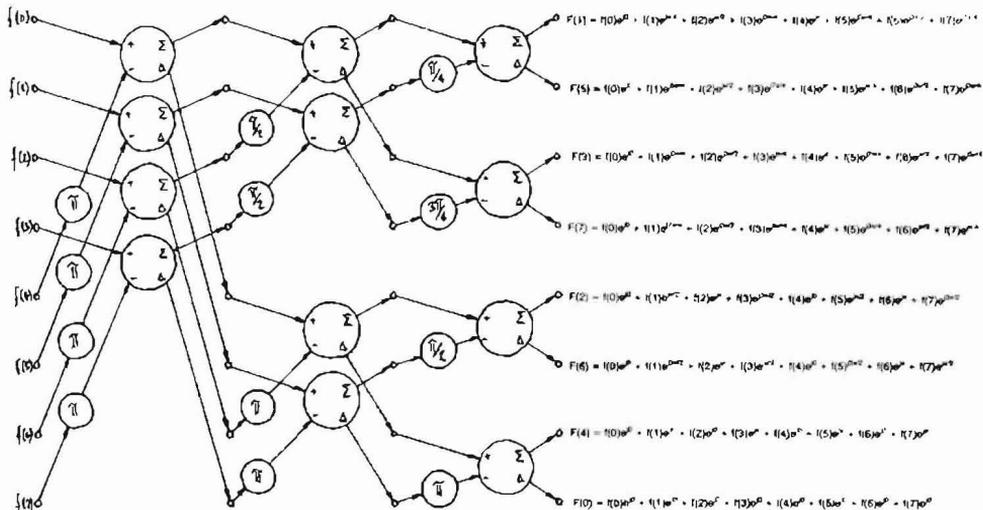


Fig. 3.3.: Eight-point FFT, computed in three steps, each using four "butterfly" operations

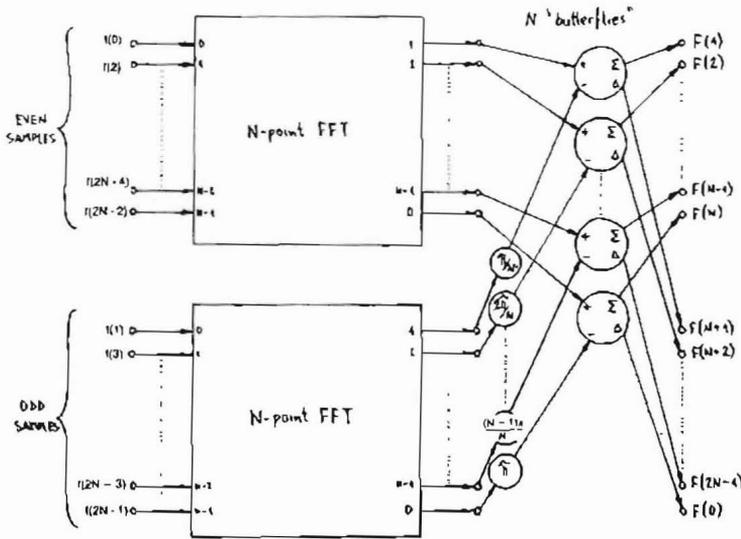


Fig. 3.4.:  
Obtaining a double-length (2N) FFT from two single-length (N) FFTs

an arbitrary large number of samples could be designed in a similar way. In the case of an 8-point FFT, only 12 "butterflies" are required compared to the 64 shift/add operations of a straightforward DFT algorithm to get the same result.

To design FFT algorithms, operating on an even larger number of data samples, one should therefore investigate the possibility of combining several FFTs computed on a smaller number of samples. Fig. 3.4. shows how to combine two N-point transforms (not necessarily computed using the FFT algorithm) into one single transform on  $2N$  (twice the number of) points. In addition to the two N-point transforms,  $N$  "butterflies" are required. These "butterflies" require  $N$  different phase shifts ranging from  $\pi/N$ ,  $2 * \pi/N$ ,  $3 * \pi/N$ ...  $(N - 1) * \pi/N$ ,  $\pi$  in steps of  $\pi/N$ .

The principle shown in fig. 3.4. is in fact used to design a FFT algorithm operating on any data length  $N$  that is a power of 2. A FFT algorithm can thus operate on 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024... data points. The 4-point FFT can be derived from the 2-point FFT, the 8-point FFT can be derived from the 4-point FFT, the 16-point FFT can be derived from the 8-point FFT etc...

Each doubling of the data points only requires an additional stage so the total number of stages is equal to  $\log_2(N)$ . Each stage requires  $N/2$  "butterflies". The total number of "butterfly" operations is therefore equal to  $N/2 * \log_2(N)$ .

A quick Look at fig. 3.3. shows that the results do not appear in any reasonable order at the output of the FFT algorithm: 1, 5, 3, 7, 2, 6, 4, 0. Considering the construction principle shown in fig. 3.4., a very simple rule to find the desired output can be found. This rule is called bit-reversed addressing and it is shown in fig. 3.5. for the 8-point FFT example. To find an output number one has to take the corresponding input number, write this number down in binary format, reverse the order of bits, convert the number back to decimal and add 1. This rule can be easily implemented in digital hardware (dedicated DSP microprocessors), where data is stored in consecutive memory locations.

To implement the FFT algorithm, a number of "butterfly" operations have to be performed. An analog implementation called the "Butler matrix" uses delay lines to obtain phase shifts and "rat-race" hybrids or 3 dB directional



couplers for the add/subtract operations. The inputs of the FFT circuit are connected to the elements of a linear antenna array and the outputs of the FFT circuit to receivers and/or transmitters. Since the required phases and magnitudes of the signals feeding an antenna array are the Fourier transform of the desired radiation pattern, the outputs of the FFT circuit correspond directly to beams in the various directions.

Implementing the FFT algorithm on a digital computer most operations are performed with complex numbers. Although phase shifts are easier to perform if complex numbers are held in a magnitude/phase format, sums and differences require a real/imaginary-component number format. Since conversions from one number format to another are very time-consuming, all computations are usually done in the real/imaginary-component format. In this case a phase-shift operation requires four real multiplications with coefficients from a precomputed table of phase shifts and two additions. Each summation of two complex numbers requires two real summations and each complex difference requires two real differences.

The phase-shift coefficients are precomputed and stored in memory, since only  $N$  different coefficients are required in all stages of a  $N$ -point FFT. The same coefficients can be used in the following FFT, if a number of FFTs have to be computed on changing data. Finally, the phase-coefficient table includes sines and cosines which are much more time-consuming to compute than the multiplications and additions required for the FFT itself.

If a FFT is computed on real data, then only half of the outputs contain interesting data, the other

half are just complex conjugates. To use the algorithm more efficiently, another set of input data can be fitted into the imaginary part of the input variables. After the FFT algorithm is performed, the two results can be separated by simple additions and subtractions using the symmetry laws of the Fourier transform. If desired, the two results can be further combined into a single, double length FFT.

The inverse DFT can easily be performed using the FFT algorithm in the reverse direction. The number of mathematical operations is identical except for an additional division by  $N$  for each data point to obtain the original magnitude back.

There are even more efficient algorithms to compute a DFT or its inverse. All of them are, however, based on the FFT principle described above and require a little more programming efforts to further reduce the number of computations required.

---

#### 4. SPECTRUM ANALYSIS USING THE FFT ALGORITHM

---

One of the most obvious applications of the FFT algorithm is a FFT spectrum analyzer. The FFT algorithm itself is performed on a digital computer, usually a DSP microprocessor. The input signal is provided in a digital format from an A/D converter. The microprocessor itself can display the result in a variety of formats.

However, to build a digital FFT spectrum analyzer some additional functions are required. A block

$f(0)$	>>---->	0 = 000B	>>---->	000B = 0	$0 + 1 = 1$	>>---->	$F(1)$
$f(1)$	>>---->	1 = 001B	>>---->	100B = 4	$4 + 1 = 5$	>>---->	$F(5)$
$f(2)$	>>---->	2 = 010B	>>---->	010B = 2	$2 + 1 = 3$	>>---->	$F(3)$
$f(3)$	>>---->	3 = 011B	>>---->	110B = 6	$6 + 1 = 7$	>>---->	$F(7)$
$f(4)$	>>---->	4 = 100B	>>---->	001B = 1	$1 + 1 = 2$	>>---->	$F(2)$
$f(5)$	>>---->	5 = 101B	>>---->	101B = 5	$5 + 1 = 6$	>>---->	$F(6)$
$f(6)$	>>---->	6 = 110B	>>---->	011B = 3	$3 + 1 = 4$	>>---->	$F(4)$
$f(7)$	>>---->	7 = 111B	>>---->	111B = 7	$7 + 1 = 8$	>>---->	$F(0)$

Fig. 3.5.: Output bit-reversed mapping for a eight-point FFT

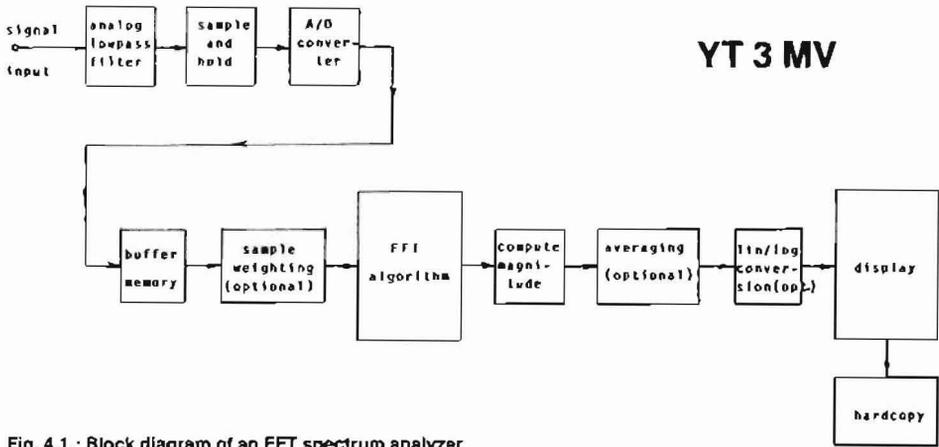


Fig. 4.1.: Block diagram of an FFT spectrum analyzer

diagram of a DSP microprocessor-based spectrum analyzer is shown in fig. 4.1. The analog input signal is first sent to an analog lowpass (bandpass) filter to prevent aliasing like in any DSP application. The analog filter is followed by a sample-and-hold and an A/D converter. The A/D converter feeds a buffer memory, since the FFT algorithm operates on blocks of data. Before the FFT the signal samples may be weighted optionally. The complex spectrum provided by the FFT algorithm is used to compute the magnitudes of the spectral components, the phase information is discarded. Averaging is used to improve the signal-to-noise ratio in some measurements. An optional linear-to-logarithmic conversion is standard for all spectrum analyzers. Finally, the result can be dis-

played in different formats and a conventional computer printer can be used to obtain a hardcopy.

The performance of a DSP FFT spectrum analyzer is mainly limited by the performance of the A/D converter used. The conversion speed of the A/D converter defines the maximum bandwidth and the resolution of the A/D converter defines the available dynamic range. After the A/D converter the digitized input signal can be conveniently stored in memory if the microprocessor is unable to process the data in real time. Also all suitable microprocessors offer a computational accuracy of at least 16 - 24 bits allowing a much wider dynamic range than any A/D converter.

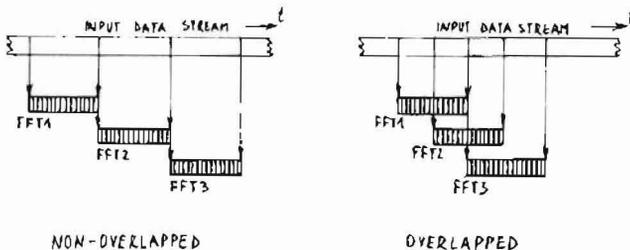


Fig. 4.2.:  
Overlapping FFTs

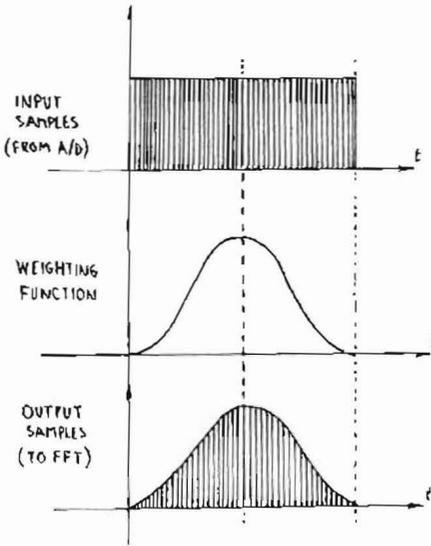


Fig. 4.3.: Weighting signal samples

Even if the DSP microprocessor is fast enough to process all of the data in real time, the input data stream has to be sent to a buffer memory first, since the FFT algorithm operates on blocks of data, not on single samples. Without weighting FFTs are usually performed on contiguous, but non-overlapping blocks of data to obtain almost all of the spectral information contained in the input signal.

In the case of input signal weighting, the contribution of the samples at the beginning or at the end of a block is very limited. To use all of the information contained in the input signal overlapped FFTs have to be performed. Both cases are shown in fig. 4.2. In the second case the overlap is set to about 50 % for a raised-cosine weighting function.

If the FFT algorithm is performed on a raw, unweighted block of data, the corresponding spectrum is distorted. Since the FFT does not consider any data samples before the block nor any data samples after the processed block of data, the actual input signal to the FFT algorithm corresponds to the real input signal modulated with a rectangular impulse of the length of the data block. A rectangular impulse with steep

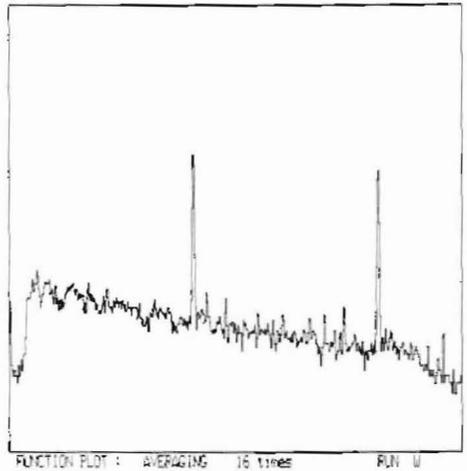
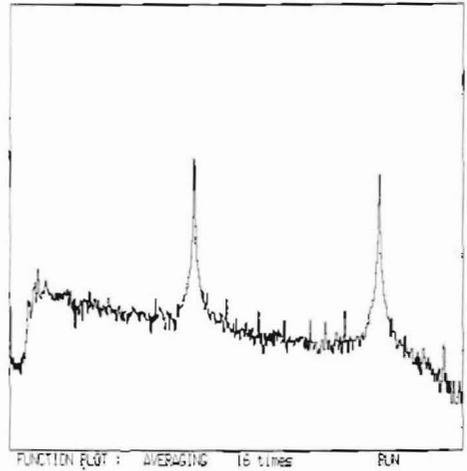


Fig. 4.4.: No weighting (above) versus raised-cosine weighting (below), same input signal, LOG vertical scale

leading and trailing edges has a very wide frequency spectrum of the form  $\sin(X)/X$ . The resulting output will be the real signal spectrum convoluted with the  $\sin(X)/X$  function.

Although the real signal spectrum can not be obtained since it requires an infinite amount of time, a much more accurate spectrum can be obtained by weighting the signal samples as shown in fig. 4.3. Weighting means multiplying



each signal sample with a constant whose value depends on the position of the sample inside the input data block. The practical effect of weighting is to replace the abrupt ON/OFF transitions with smooth transitions at the beginning and at the end of the data block. Weighting functions are selected to minimize the distortion of the signal spectrum. Raised-cosine and Gaussian functions are usual choices, since they have a very narrow own spectrum with low side lobes.

The effects of no weighting versus weighting are shown in fig. 4.4. The two plots show the spectrum of the same signal obtained in two different ways. A linear 512-point frequency scale is used on the horizontal axis and a logarithmic amplitude scale (15 bits or 90 dB/full scale) is used on the vertical axis. All the parameters, including the input signal, are the same for both plots except for weighting: the plot above was obtained without any weighting

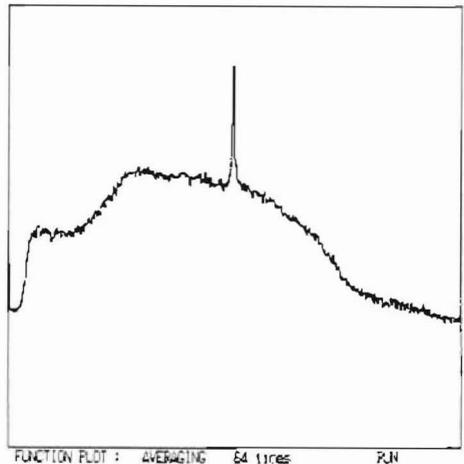
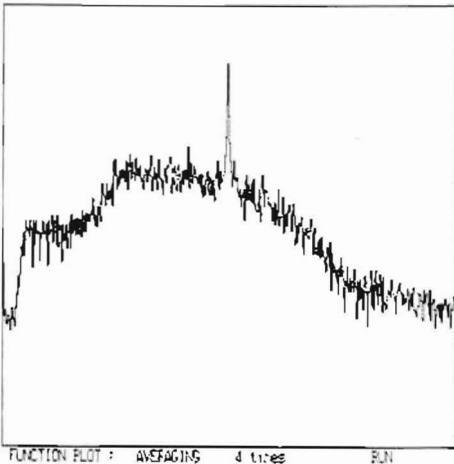
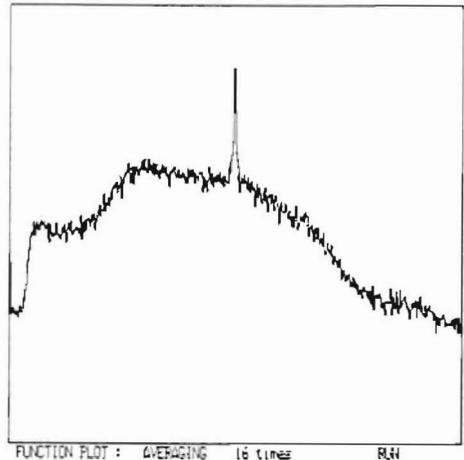
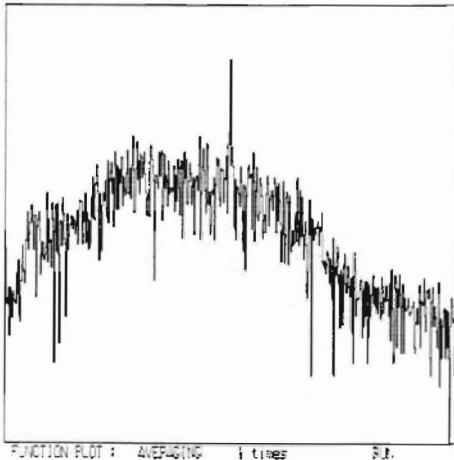


Fig. 4.5.: No averaging (above), averaging 4 times (below), same input signal and other settings as in fig. 4.6.

Fig. 4.6.: Averaging 16 times (above) or 64 times (below), same input signal and other settings as in fig. 4.5.



while the plot below was obtained with a raised-cosine weighting. Raised-cosine weighting clearly provides much more clear spectral lines, with no INEXISTENT sidebands. On the other hand, weighting slightly reduces the frequency resolution making the peaks broader. Selecting weighting or not is therefore a tradeoff between dynamic range and frequency resolution.

If a measurement is affected by random noise, averaging among a number of otherwise identical measurements improves the accuracy of the result. Automatic averaging is very easy to implement on any microprocessor-controlled test equipment. Averaging is used in spectrum analyzers to improve the signal-to-noise ratio of the displayed data. The improvement that can be obtained by averaging is shown in fig. 4.5. and fig. 4.6. All four plots were obtained from the same input signal in an identical way except for different amounts of averaging.

The linear-to-logarithmic conversion includes the computation of a logarithm for each spectral component. Since the logarithm is a rather "slow" function on digital computers, a look-up-table algorithm or a similar approach has to be used to avoid unnecessary loading of the computer. The same constraint applies to the display procedure: most computers require more time to draw a high-resolution plot than to compute the FFT algorithm. The display routine and/or dedicated hardware has to be quick enough to avoid slowing-down the spectrum analyzer. On the other hand, a hardcopy of the video display is usually very easy to obtain on any computer using a standard printer or plotter, at least when compared to analog instrumentation with CRT displays.

Besides the conventional frequency/amplitude function plot other types of display are possible on digital computers. A practically very useful type of display is the intensity spectrogram. In the latter frequency is still plotted on the horizontal axis. Each FFT result is, however, represented by a single-image line and the pixel brightness is used to represent the magnitude of a spectral component. The results of successive FFTs are plotted on successive lines, showing the results of a large number of consecutive measurements on just one computer screen.

Intensity spectrograms are useful when analyzing continuously changing signals

The display of a FFT spectrum analyzer usually includes the complete frequency range covered by the FFT algorithm: from zero to half the signal sampling frequency. The frequency resolution is then simply equal to the frequency span divided by the number of lines displayed. The frequency resolution may be slightly worse if weighting is used in front of the FFT algorithm. Of course partial displays are possible too, showing just a subset of spectral lines computed by the FFT algorithm. The sample-and-hold circuit in front of the A/D converter is an excellent harmonic mixer. It is therefore possible to observe a different frequency band just by replacing the input lowpass filter with a bandpass filter for the selected frequency range.

Finally, a comparison has to be made between a FFT-based spectrum analyzer and a scanning-receiver type spectrum analyzer (conventional analog RF spectrum analyzer). Of course a scanning-receiver type spectrum analyzer could be implemented on a digital computer as well. A FFT-based spectrum analyzer has, however, a very important advantage over a scanning-receiver spectrum analyzer: regardless of the hardware used the FFT spectrum analyzer uses the available spectral information in a much more efficient way resulting in a much quicker operation.

As an example, consider that a 5 kHz wide frequency band has to be analyzed to a resolution of 10 Hz. A scanning receiver with a 10 Hz bandwidth has to dwell on each 10 Hz frequency step for about 0.1 seconds, resulting in a total sweep time of about 50 seconds! On the other hand, a FFT-based spectrum analyzer needs to sample a 5 kHz wide signal with a sampling frequency of 10 kHz. A 1024-point FFT has to be used to obtain a 512-point display, so the total "scanning" time is 0.1024 seconds!

In the above real-world example the FFT spectrum analyzer is about 500 times faster! The reason for this is that a conventional scanning-receiver spectrum analyzer only uses the information contained in its receiver bandwidth, all the other information contained in the signal



is simply rejected! On the other hand, the FFT-based spectrum analyzer uses all of the information contained in the signal since the FFT algorithm corresponds to a bank of 512 parallel bandpass filters in the above example. Such a bank of filters would be prohibitively expensive and difficult to make using conventional analog technology.

A FFT-based spectrum analyzer can therefore be used in applications where a conventional scanning-receiver type spectrum analyzer is not practical due to the too long scanning time or completely useless since the signal is not available for the scanning time period required. Even in the case when the scanning-receiver type can be used, the FFT-type can provide a much more accurate result in the same time, averaging among a large number of measurements.

Unfortunately the bandwidth and dynamic range of digital FFT spectrum analyzers are severely limited by the available hardware, mainly A/D converters. It is therefore necessary to understand the advantages and disadvantages both techniques to select the most suitable one for a particular problem, since the two techniques are complementing each other rather than competing at the present state of technology.

**Will be continued!**

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# Universal Synthesizer for Frequencies up to and above 1000 MHz Part 2 (Conclusion)

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## 2. CIRCUIT DESCRIPTION

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Integrated circuits for use in synthesizers are offered by a number of firms; the choice fell here upon an IC-family from Plessey. These chips contain the most interesting phase detectors (to be precise two – one digital and one analogue – which share the work), moreover, the synthesizer processor employed has the means to control an EPROM automatically in order to obtain all operational information there. The chip also contains the sequence control together with almost all the components belonging to a PLL circuit. It can be so connected, that in normal operation, no access to the PROM is carried out thereby minimising interference signals on the output caused by internal control signals. The pre-scalers are also from Plessey in order to eliminate the possibility of interface problems. There is deliberately no description of similar chips from this series with micro-processor control as the required control computer would restrict the circle of users. **Figure 6** shows the central part of the circuit with pre-scaler, PLL IC, EPROM and loop filter.

The RF signal from the oscillator is taken via a buffer amplifier with variable pre-scaler. The amplifier is not used here to increase the level (the IC is relatively sensitive), but should improve the isolation between the analogue and digital sections of the circuit. It is important that decoupling arrangements are employed in the supply line in the interests of obtaining a clean output signal. Many tests have proved that the dual-gate MOSFET circuit has the highest isolation properties from output back to input. A BF981, or equivalent, is satisfactory up to about 200 MHz but for higher frequencies the later types, such as the BF966 or the BF988, are particularly suitable. The divided signal is taken directly to the PLL IC. This contains, as already mentioned, all the other parts of the PLL. In this circuit, the built-in crystal oscillator is also used.

In order to reach frequencies which are located between two step frequencies, one varicap diode is connected across the crystal. For a simple manual tuning operation this circuit is sufficiently linear. The reference crystal is taken to be 4 MHz. According to the data sheet, frequencies up to 10 MHz are possible; the reference divider must then be programmed somewhat differently. The complete programme information is contained in





an EPROM. It is so programmed that the receive frequency is selected directly at the switch. For send/receive switch-over, and for relay operation, further address lines can be used to change-over to the requisite set of data.

As mentioned previously, the IC contains two phase detectors. The digital phase detector is responsible for the control of large frequency differences, small deviations result in the sample-and-hold detector being engaged. This in its characteristic analogue PD has only a very small sample of the reference so that the spectral lines in the comb of frequencies are suppressed. Apart from that, it attenuates switching noises of all types from the digital section.

Both detectors in the IC are externally paralleled at their inputs, the auto switch-over is accomplished by the antiparallel connected diodes. If silicon diodes are employed for this purpose, the switch-over is carried out at a control-voltage surge of more than 0.7 V. The resistor RB and capacitor CB determine the loop gain of the sample-and-hold phase detector. The capture and control range of the phase detector and its response time are thereby determined. The values employed should be a good compromise for use in radio-equipment synthesizers. That is also, in general, applicable to loop filters.

As the oscillator trans-conductance always varies from one construction to another, there must be some attempt at matching for optimum operation. The first function is always possible with the dimensions as given. The annex contains some formulae with which calculations may be carried out. Further information can be found in the data-sheets/books (5) and (6) whereby the formulae in (6) are partially defective.

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### 3. OSCILLATORS

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#### 3.1. Decoupling Arrangements

At this point, there must be some discussion about decoupling of the oscillator from the rest

of the circuit, especially from the PLL chip, before going on to the actual oscillator description.

With a Voltage Controlled Oscillator (VCO), the tuning rate-of-response  $K_{VCO}$  (Hz/V) must be kept firmly in mind. As an example, it will be supposed that the 70 cm band should be covered by both the transmitter and the receiver. Using an IF of 21.4 MHz, the final frequency minimum tuning range is 408.6 MHz to 440 MHz. This means a total range of altogether 31.4 MHz (highest transmit frequency 440 MHz to lowest receive frequency of 430 MHz minus the IF). At an available loop control voltage amplitude of 10 V (12 V minus the OP-amp. off-set voltage and an allowance for variations) result in a VCO sensitivity of 3.14 MHz/V. A loop-voltage variation of only 1 mV would result in a frequency change of 3.14 kHz! Loop voltage contamination of this order would result in an unusable input signal (FM noise modulation).

Included in these disturbing influences are variations in the supply voltage caused by mechanical vibrations (microphony) and changes in the load caused, for example, by internal changes to the switching divider which changes its resistance according to its input conditions. The supply-voltage fluctuations must be minimised with the aid of IC stabilizers. The self-generated noise of the latter must not be overlooked; see (7). The effect of load variations is avoided by using buffer stages at appropriate points. It is also helpful to reduce the coupling to the buffer stages to as low a value as possible. The resulting low loading also improves the quiescent stability of the circuit. The decoupling arrangements around the PLL IC are of the utmost importance.

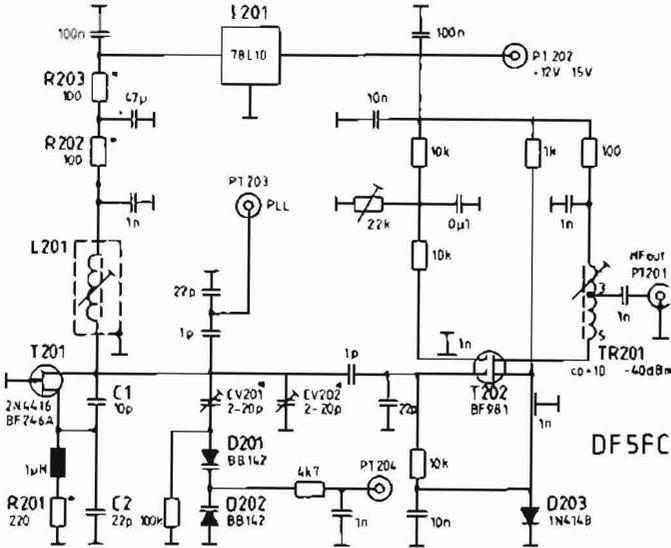
#### 3.2. FET Oscillator up to 200 MHz

In practice, two separate oscillators are usually employed to cover the requisite frequency range. Up to about 200 MHz, the FET oscillator shown in fig. 7 has been proved successful.

Tests have shown that the specified Neosid inductor should be used in the interests of stability. With CV201, the tuning range of the oscillator, and thereby its tuning sensitivity, is made



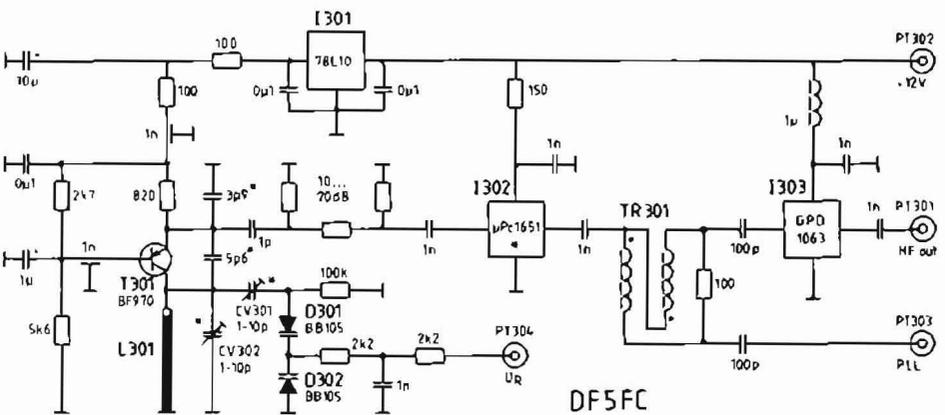
**Fig. 7:**  
FET-Oscillator usable  
up to 200 MHz



adjustable. With CV202 and L201, the basic frequency range can be set.

After the oscillator, the signal is fed to a capacitive divider on the PLL buffer stage and then on to the oscillator amplifier. The oscillator ampli-

fier has a dual-gate MOS-FET which allows a relatively large adjustment range of the output voltage and also possesses a high isolation to return signal energy. The power can be varied over a range from +10 dBm to -40 dBm.



**Fig. 8:** Oscillator circuit for frequencies up to, or above 1 GHz (according to construction).  
The tuned circuit can be realized from a length of semi-rigid cable, the length of which must be determined experimentally - start with 30 mm



The core of the output transformer can be any that is suitable for VHF, e.g. Neosid or Siemens. Tests have confirmed that double-hole ferrite beads have proved themselves – they are used in the DJ7VY-amplifier, as well as the usual ring cores. The number of turns may remain unchanged between 50 MHz and 200 MHz.

### 3.3. Bi-Polar Oscillator up to ca. 1300 MHz

In the frequency range above 200 MHz, a circuit with a PNP transistor has proved itself in many tests. The advantage of the circuit shown in **figure 8** is that the tuned-circuit inductor is grounded at one end. This obviates trouble with the parasitic series inductance inherent to decoupling capacitors which is prone to cause spurious oscillations. The whole circuit construction must be carried out in accordance with VHF practice. This means, in particular, that the base and the cold end of the emitter resistor must be fitted with multi-layer chip capacitors sunk into the board. Careless work can result in drop-outs in the tuning range or reversal spots in the progression of tuning. This leads to completely unpredictable behaviour of the PLL. The decoupling capacitors must be located as close as possible to the transistor. The transistor should be one of the given types, especially when working at the upper frequency limit. In any case, the various connecting sequences must be adhered to.

A length of short-circuited, semi-rigid coaxial cable is normally used with this type of oscillator which then functions as a capacitive shorted  $\lambda/4$ -wave tuned circuit. As both the inner and outer conductors of the line are bound rigidly together by the dielectric, the oscillator possesses excellent mechanical stability and shows little sign of microphony effects. The cable (e.g. Suhner type SR3), can be of either 50  $\Omega$  or 75  $\Omega$  characteristic impedance. The circuit can also operate either with a Lecher line or with a wound-inductor tuned circuit. The values given are dimensioned for a 70 cm equipment using a 21.4 MHz IF with the send frequency being produced directly. For other frequencies, the capacitors around the oscillator transistor, together with the varicap diodes' coupling capacitor, must be altered accordingly. Trimmer CV301 controls the fre-

quency coverage of the oscillator and CV302 the basic frequency.

The buffer stage, in this case, comprises a 10 dB to 20 dB attenuator pad and an IC wideband amplifier, the NEC  $\mu$ PC1651. The circuit is designed so that there is at least 1 mW to 2 mW at the output of the amplifier.

Of course, other types of oscillators can be used here, among them the wide-range oscillators published in (8) or the semi-rigid VCOs in (9). Also of utility are the ceramic-resonator oscillators described in (10).

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## 4. PROGRAMMING THE NJ8820

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### 4.1. The IC's Internal Construction

The internal block schematic of the IC is shown in **figure 9**. The NJ8820 contains an 11-bit reference counter, a 7-bit A-counter and a 10-bit M-counter whereby the maximum division factors are set. The A- and the M-counter together control the switchable dividers via a logic circuit. When programming the reference counter (this controls the step frequency), care must be taken that the variable counter is followed by a fixed divide-by-two scaler.

All counters are equipped with registers connected with each other in order that 4-bit words can be registered externally. All bits together represent a 28-bit long word. To this 28-bit word, four make-up bits are added to make a total of 32 bits. This is split-up into eight 4-bit words which address the IC, via appropriate address logic, with a 3-bit wide address bus. The correct order of these bits is, of course, important for the correct control. The signal-timing schematic of **figure 10** shows the exact arrangement. The individual dividers will be treated with examples. The 00 stands for the make-up bits.

### 4.2. Deriving the Division Factors

#### 4.2.1. Reference Counter

The internal oscillator circuit is able to work with crystals of over 10 MHz. In order to determine

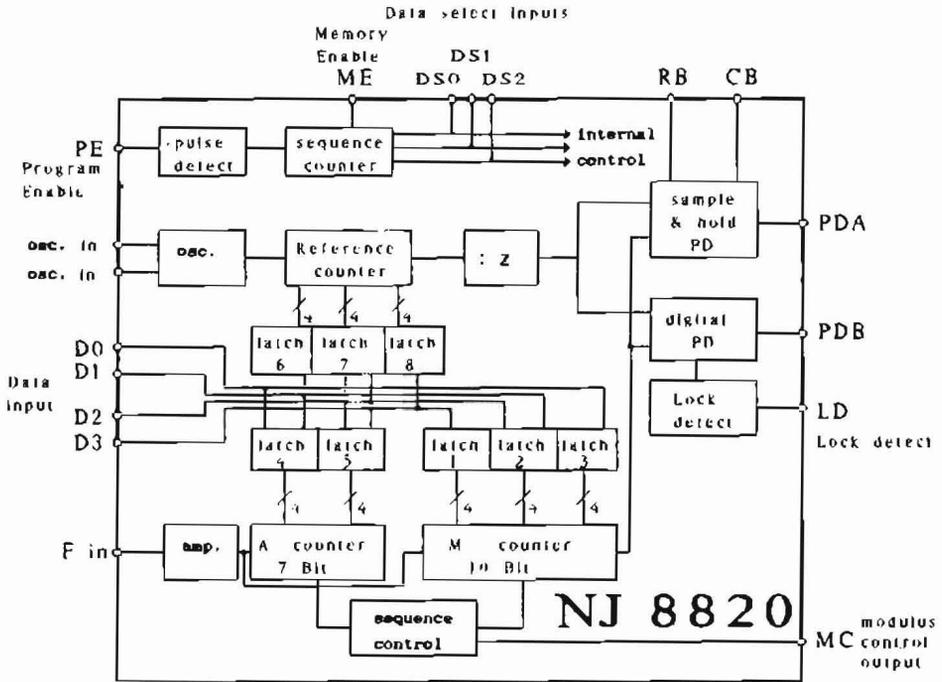


Fig. 9: Interior of the PLL-chip module. It contains all the required dividers and control circuits

the required division factor, the crystal frequency must be halved (internal : 2) and then divided by the reference frequency. The result must be a whole number. The division factor must then be expressed as a binary word.

$$R = f_{\text{Quartz}} / (2 * f_{\text{step}}) \quad (5)$$

Example:  $f_q = 4 \text{ MHz}$ ,  $f_s = 10 \text{ kHz}$   
 $R = 4 \text{ MHz} / (2 * 10 \text{ kHz}) = 200 \text{ } \approx \text{ } 00011001000$   
 (sequence R10..R0) = 11 bit

#### 4.2.2. The A- and M-Control Counters

From the ratio of output frequency to reference frequency, the total division factor N is determined. For an N divider with a switchable prescaler the following expression applies:

$$N = f_{\text{out}} / f_{\text{step}} = (P * M) + A \quad (6)$$

If N is divided by P the result is not a whole number. The value before the comma is substituted for M, the value after the comma is multiplied by P and the result is then A. Each value for M and A are transformed again into binary words and put into the appropriate places in the table (see para. 1.4.).

Example:  
 $F_{\text{VCO}} = 430 \text{ MHz} - 439,99 \text{ MHz}$   
 channel step = 10 kHz ( $f_{\text{step}}$ )  
 $N_{\text{max}} = 439,99 \text{ MHz} / 10 \text{ kHz} = 43999$   
 $P = 80 \text{ (SP 8719)}$

$M = N/P = 43999/80 = 549,9875$   
 $= 549 \text{ } \approx \text{ } 225 = 10/0010/0101$   
 (series M9...M0) = 10 bit

$A = 0,9875 * 80 = 79 \text{ } \approx \text{ } 4f = 100/1111$   
 (series A6...A0) = 7 bit

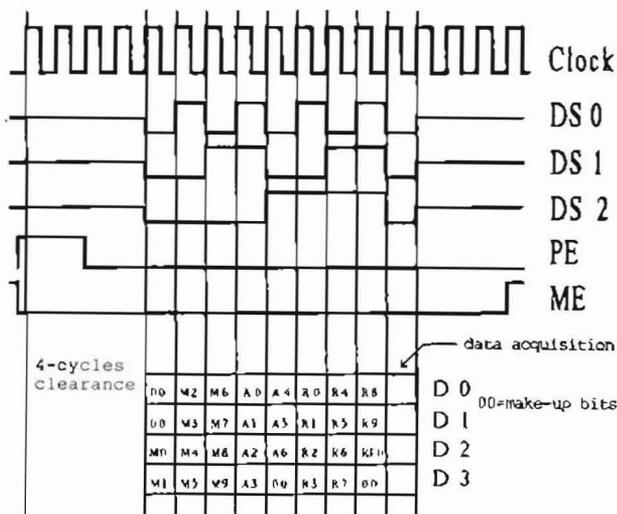


Fig. 10:  
Arrangement of the individual programming bits with respect to the PLL-ICs control signals

#### 4.3. Programming Units

The IC used here, retrieves the programming information automatically from the PROM or EPROM. In this manner, the PROMs for the receiver and transceiver are so programmed that in each case the transmit frequency is adjusted at the BCD switches. The switch-over to "transmit" and to "relay" operation is accomplished by changing the top address bits. The PROMs used here are only half exploited (4-bit words, for full exploitation a multiplexer must be connected to the data line).

The programming algorithms for such PROMs would be going a little too far for an article such as this as a good knowledge of mathematics is required. Ready-made PROMs for some standard applications (2 m with 10.7 MHz IF, 70 cm with 10.7 MHz IF with and without LO multiplier, 70 cm with 21.4 MHz IF with and without multiplier, simple 23 cm FM transceiver with 35 MHz IF) are available and the range will be expanded.

For the testing of the actual synthesizer function, particularly if it has not been pre-programmed, the circuit of figure 11 has been developed.

The control signals of the synthesizer IC are used for addressing a total of 32 circuits. It can be

seen that there are two blocks each having 16 bit and connected together with another multiplexer. In the prototype construction, DIL switches were employed in bunches of eight. When using toggle switches, 28 are enough, of course, but the four make-up bits should not be forgotten irrespective of whether they are 1 or 0. At the switches, the binary words are set to those values arrived at from the dividers (note the correct order). If available, hexa-decimal coded switches can be used whereby the correct arrangement of the bits must be observed.

When using the setting-up programming circuit, the signal lines must not be taken via feed-through capacitors as the impulses would be distorted during dynamic addressing operations. It is recommended that for this case a DIL plug is constructed, which is compatible with the PROM socket, and connect this, using a short flat-band cable, to the programming device.

At this juncture, a very important feature of the IC must be considered. All the transmitted bits are internally registered so that every 32-bit word is only needed to be sent once. The IC has an input (pin 14) at which can be switched to a permanent state of either address or read-in. If this input is returned to ground, the memory is permanently

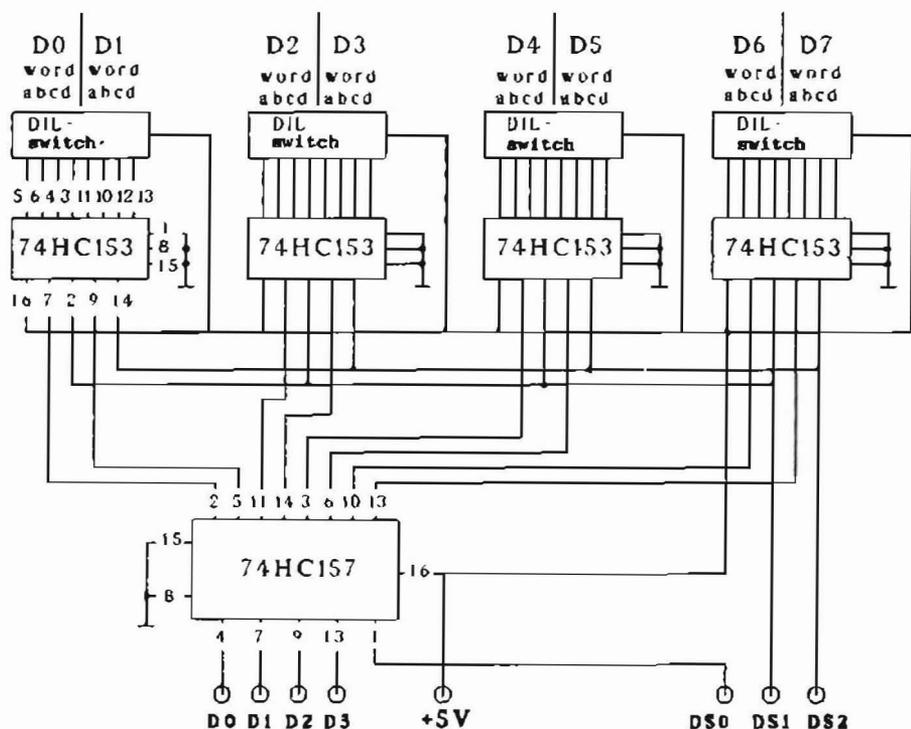


Fig. 11: Auxiliary programming unit for the PLL-IC (only required if working without the E-PROM is required, e.g. for tests etc.)

read out. It is also possible to apply a pulse at this input (either positive or negative) simultaneously with the arrival of the fresh input data.

Many circuits spring to mind for this sort of purpose. In the proposed synthesizer circuit, the lowest value bit is assessed from every BCD switch. As this is changed from 1 to 0 (or vice versa), the polarity across the capacitor also changes and its charge/discharge energy can be used as an impulse. Unfortunately, it turned out that the type of BCD switch chosen, operated too slowly. The resulting pulse, therefore is a little truncated and the IC does not respond. To improve this, a CMOS Schmitt trigger IC, type 74HC(T)14 was provided. The capacitor for the differentiation is located right behind this circuit.

Before the gate inputs, there are integrators with a charge time of  $\tau \approx 200$  ms in order to eliminate contact bounce in the BCD switches. This value seemed to be satisfactory for all types tried. If, however, there are some difficulties (false locks), the value can be increased to 1 s. Such a long time could cause problems on transmit/receive switch-over. The only real remedy is to try a better type of switch!

After these measures, no more difficulties were experienced. Of course, any type of Schmitt trigger-IC could have been tried in this position. When the synthesizer is in operation with the auxiliary programmer, the IC should be switched to either permanent interrogation or an additional push-button switch must be fitted.



A further important feature is the lock detector "LD". It lies at ground potential when the loop is in lock. For the control of external modules, it is taken out of the module. At PT 29, the original signal is available having an internal resistance of 1 k $\Omega$ , at PT 28, an open-collector output is available in order to drive an LED – as a simple application. Under transmit conditions, the transmitter should be suppressed by one of these outputs when frequency changes are being undertaken in order to avoid unwanted transmitter outputs.

## 5. CONSTRUCTION AND ALIGNMENT

Printed circuit boards have been developed for the actual synthesizer as well as for both

oscillators. All three PCBs are double-foil, 1.5 mm thick epoxide-resin (imperative for HF). At least the synthesizer board should be provided with through-contacting as the component count is very high in some parts of the board. Experience has proved the value of using these professional practices in order to obviate the frustration caused by tracing grounding problems – such trouble quickly exceeds the extra expense.

The synthesizer board (layout plan in fig. 12) is of 70 cm x 70 cm dimensions and fits a standard tin-plate box. This type of construction is sufficient for the stability requirements of normal oscillators. The dimensions of both oscillator boards are identical at 70 cm x 35 cm (figs. 13 and 14), also fitting proprietary standard boxes. Furthermore, it is possible to solder them, complete with PCBs, into a yet larger enclosure.

All the DC-supply potentials are fed into the enclosures via feed-through capacitors. This also

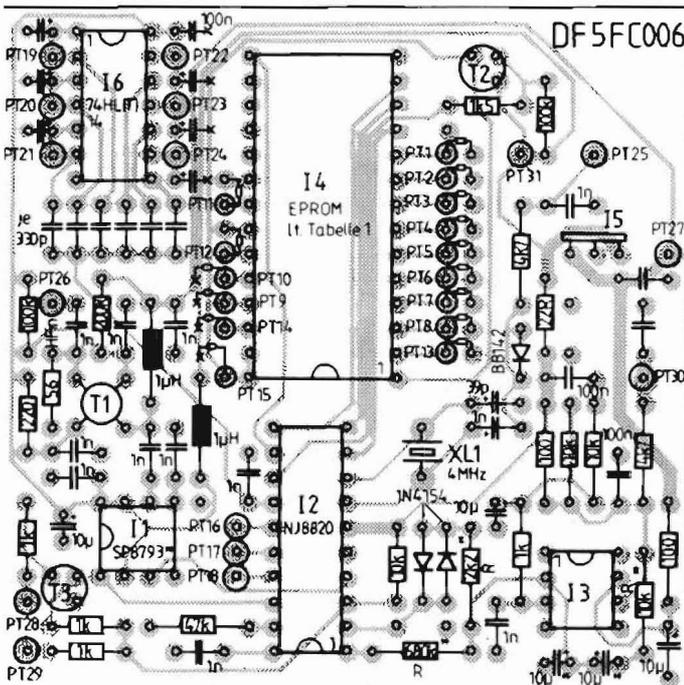


Fig. 12: Synthesizer PCB component layout plan

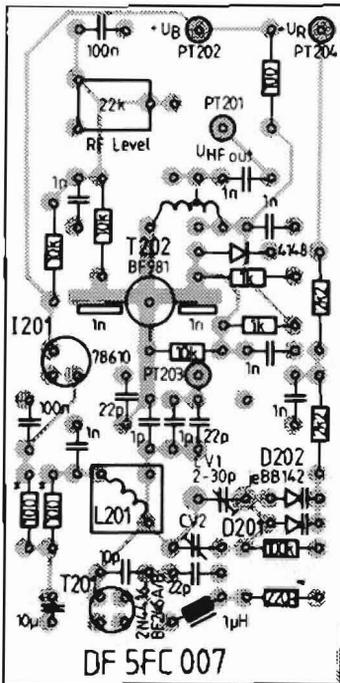


Fig. 13: FET-oscillator PCB component layout plan

applies to the loop control line. The RF connections use miniature coax connectors such as the well proven SMB or SMC series. Of course, the RF connection can just as well be soldered directly without using any connectors. The use of PTFE coaxial cable is recommended but this is more a question of price and availability.

Now for the actual construction. The synthesizer contains no internal adjustment possibilities! It has proved convenient to first of all solder the PCB into the pre-drilled housing and then load it later with components. This reduces the risk of a hot death for some components! The pre-scaler is soldered directly into the board but the other ICs can use sockets. Where the boards have not been designed to have circuit tracks on both sides, the removal of foil from around the non-grounded component pins should not be forgotten.

The board has been so designed, that the programme input pull-down resistors are soldered in an upright position. In this procedure, the resistor body is bent towards the groundplane. The free end is then taken to the feed-through capacitor (see fig. 15).

In this manner, many solder points and space is saved. Similar treatment is accorded to the Schmitt-trigger input resistors. They are connected by only one leg to the PCB, the second being connected directly with the appropriate

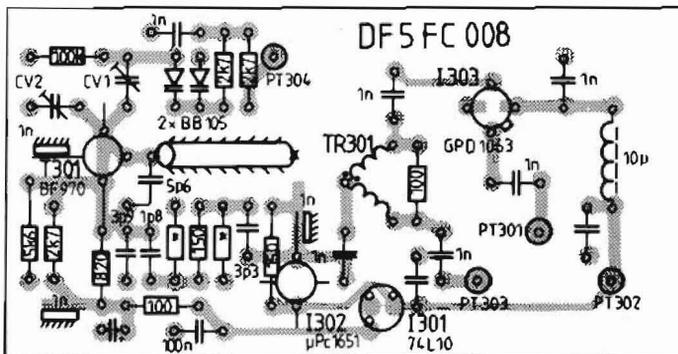


Fig. 14: GHz-oscillator PCB component layout plan. The resistors marked \* belong to the attenuator pad and should only be equipped if required. Try semi-rigid cable 3 mm dia. Experiment with length!



feed-throughs. Furthermore, the EPROM address lines are taken through the board but directly to solder points so that they can be wired according to the type of PROM employed and the desired function of the sampling bits. It is important that the three bits that arrive via the switch, are connected to DS0, DS1 and DS2. The next bit is for the TX/RX switching, and the highest bit for the relay switching. This hierarchy is crucial for correct functioning and the "standard applications" are made clear in table 1.

The PCB for each oscillator should also be installed into the housing before loading with components. The construction of the oscillators must be carried out using great care. The drain voltages and currents of the FET oscillators are adjusted after installation. The best of adjusting them is to short out the drain resistor completely and change the source resistor until a current of 6 to 8 mA is obtained. Then, the source voltage is measured. To this value, 6 V are added as FET drain/source voltage and the total value of the matching drain is given by:

$$R_D = \frac{10 \text{ V} - (U_D + 6 \text{ V})}{I_D} \quad (7)$$

The resistor before the tantalum decoupling capacitor should always be more than 30  $\Omega$ . Since the FET, in the DC range, should always simulate a constant-current generator this procedure is permissible. The oscillator itself, has a very good phase-noise characteristic and lends itself well to other projects – in which case it may be worthwhile to employ high-grade voltage regulators (REF01 etc.)

The bipolar oscillators should oscillate immediately assuming that the components have been

correctly installed. The PCB has been designed around the BF970 as the oscillator transistor. With other transistor types, the lead pin-outs must be observed.

The RF alignment is identical for the two types of oscillator. The trimmer CV01 determines the coupling of the varicap diodes and the CV02 the basic frequency. For the basic tuning, 5.5 V are applied to the voltage regulator input and CV01 is turned half-way.

### 5.1. FET Oscillator

The mid-frequency of the desired range is adjusted by L 201 with CV02 at about a third of its capacity. Trimmers CV201 and CV202 must now be iterated in order to achieve a tuning voltage range from 1 V to 11 V of the required frequency range plus an allowance of at least 1 MHz overlap. Taking a 2 metre application, this would mean a range of 132 MHz to 147 MHz. If the tuning range is not sufficient CV202 must be made smaller, CV201 must be enlarged and the alignment repeated. Altogether, the tuning range should be trimmed to be only as large as is necessary in order that the tuning sensitivity of the oscillator is not too great.

### 5.2. Bi-Polar Oscillator

The bi-polar oscillator has only two trimmers to align so that for the basic frequency adjustment, only CV302 is available. Both trimmers, again, must be iterated in order that the required tuning range is covered. This being for a 70 cm equipment 402 MHz to 442 MHz.

The PLL-filter calculations in the appendix are valid for these VCO sensitivities.

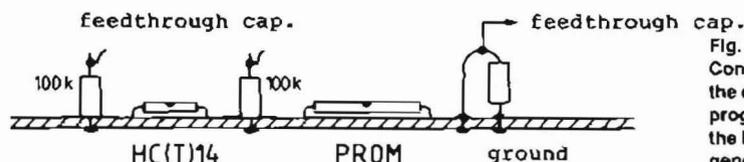


Fig. 15:  
Constructional details for the connection of the program selector switch to the E-PROM and the impulse generator





When this function is fulfilled, the PLL is considered as checked. A mid-frequency is selected and the PLL loop closed. With a correct functioning a mid-voltage will be measured and the correct frequency indicated on the counter. Also the "lock" LED must be extinguished. Check now (with an oscilloscope) the control voltage range by selecting various frequencies in the band. There must always be a DC voltage present for each selection. An alternating voltage component indicates an out of lock condition. If necessary, the tuning range can be trimmed with CV301 and CV302.

As can be seen from the circuit diagram, the reference crystal can be pulled on frequency by a varicap diode. In this manner, it is possible to realise a quasi-continuous tuning range. Some crystals are not able to be pulled to their nominal frequency. This is due to the deficit of coupling via the diode. In order to be able to achieve con-

tinuous operation, the PROM must be manufactured such that a frequency is always generated which lies one or two channels lower than the one displayed. If necessary, a little experimentation will have to be undertaken

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## 6. PARTS LIST

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### 6.1. Synthesizer Board

- 11: SP 8792/A —: 80/81 up to 200 MHz  
 SP 8793/A —: 40/41 up to 200 MHz  
 SP 8716 —: 40/41 up to 520 MHz  
 SP 8718 —: 64/65 up to 520 MHz  
 SP 8719 —: 80/81 up to 520 MHz  
 according to frequency range

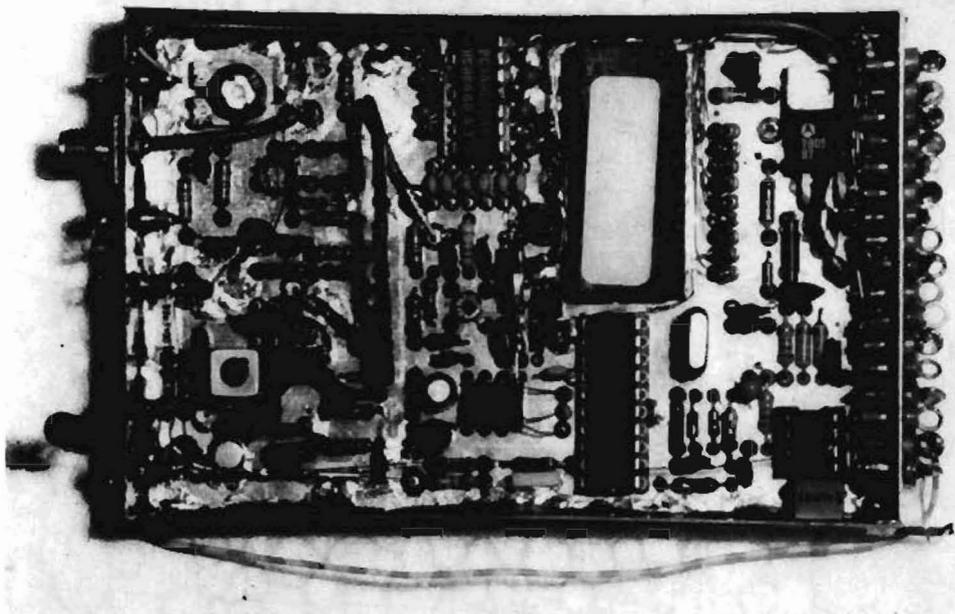


Fig. 16: Sample construction according to figs. 12/13



- I2: NJ 8820  
 I3: NE 5534 or equiv. **low-noise** type!  
 I4: EPROM according to Table 1  
 I5: 7805  
 I6: 74HC(T)14  
 T1: BF 900/981 or equiv. up to 200 MHz  
     BF 966/988 or equiv. up to 1000 MHz  
 T2: BC 557 **B** (!) or equiv.  
 T3: BC 547 **B** (!) or equiv.

All capacitors have a 5.08 mm lead spacing and the resistors should suit a 7.62 mm grid.

$\mu$ T means Tant. capacitors.

C2 should be a good quality foil type.

The values of R1, R2, R3 and C1/C1' depend upon the results of the loop-filter calculation.

### 6.2. FET-Oscillator

- T201: 2N4416 or BF246A or B  
 T202: BF 900/981/963 or equiv.

- I201: 78L10 (Ref 01, not adjusted for this project)

- CV201: 2...40 pF  
 CV202: 2...20 pF — try a fixed value 8.2 pF

- R201: }  
 R202: } adjustment i.a.w. text —  
 R203: } values given as a guide

- TR201: 8-turns with tap at 3-turns on VHF core

- D201/202: BB 142, BB 809

### 6.3. Bi-polar Oscillator

- T301: BF 970 up to ca. 700 MHz  
       BFQ 23 } up to 1300 MHz but  
       BFQ 32 } different pin-out!

- I 301: 78L10  
 I 302: Wideband amplifier e.g. NEC  $\mu$ PC1651  
       MAR-4 (Industrial Electronics)  
 I 303: Wideband amplifier GPD 1063  
       (AVANTEK)

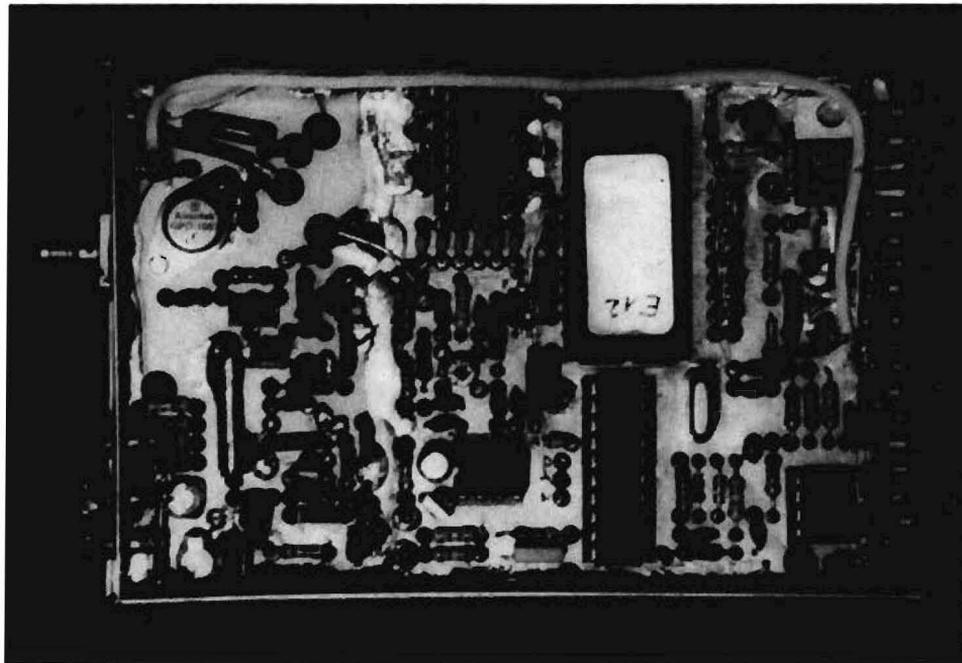


Fig. 17: Sample construction according to figs. 12/14

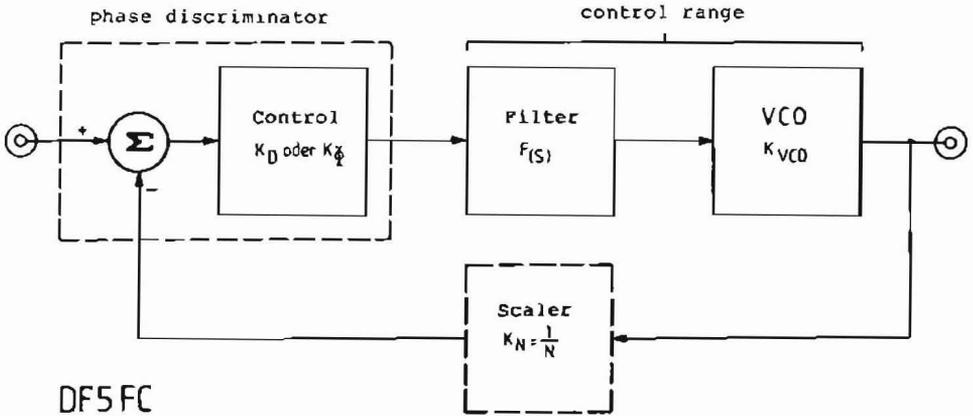


Fig. 18: Basic circuit of a PLL-loop with the individual frequency dispositions

TR 301: 2 x 4 turns on UHF core e.g. Siemens double-hole core  
 D 301 - 302: BB105

bilities (e.g. signal generators), which until now have only been available in commercial test equipment.

**7. SUMMARY**

Pictures 16 and 17 show the author's specimen construction. This is a universal and versatile synthesizer circuit which is able to be integrated into many oscillator projects and can also be retro-fitted into other equipments. An enhancement of the control, using a  $\mu P$  together with the appropriate software, opens up other possi-

**8. APPENDIX LOOP FILTER – BASIC CALCULATIONS**

A Phase-Locked-Loop (PLL) is a control structure in which a portion of the output signal is compared against a reference signal and from the result a correction factor for the output signal is derived (fig. 18).

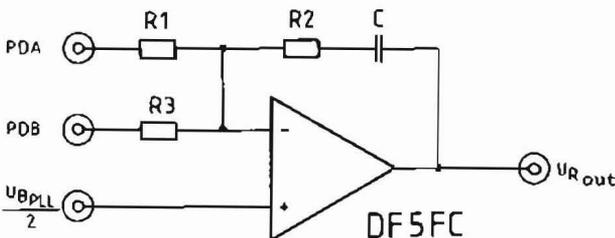


Fig. 19: Basic circuit of an active loop-filter



The behaviour of this loop, when input quantities are varied, is determined by quite a number of parameters. Many of these parameters are determined by the type of circuits selected for the oscillator, the phase detector and the divider. The only possibility in order to influence the behaviour of the loop, without going to a great deal of trouble, is to alter the loop filter. This filter can be either active, using an operational amplifier, or a passive RC network. The basic mathematics are thoroughly treated in (11). This describes the conditions suitable for the type of filter employed. The circuit under consideration here, uses an active filter employing a relatively low-noise OP. The basic circuit is shown in fig. 19.

The resistors R1 and R2 together with the capacitor C represent the universally known filter in the reference. The supplementary resistor R3, is employed for the double phase-detector. Such a filter offers the possibility of adjusting the so-called loop circuit-frequency ... and the attenuation D independently from one-another. With these quantities, the oscillatory conditions can be determined e.g. following a frequency change. If the circuit loop frequency is too low, the search time for the newly selected frequency will be high: when the attenuation is too small, it can occur that the loop doesn't lock in. The attenuation should amount to an aperiodic limit of between 0.7 and 1. The loop frequency can be very well approximated by the following expression: -

$$\omega_n = 2 * \pi * f_n \quad (8)$$

$$f_n = \frac{f_{ref}/100}{\sqrt{1 + 2 * D^2 + \sqrt{(1 + 2 * D^2)^2 + 1}}} =$$

$$\frac{f_{ref}/100}{2.48} \text{ for } D = 1 \quad (9)$$

from this follows the dimensioning equation

$$\omega_n = 2 * \pi * f_{ref}/248 \quad (10)$$

Both these quantities allow the component values for the PLL to be arrived at.

$$\omega_n = \sqrt{\frac{K\Phi * K_{VCO}}{N * \tau_1}} \quad (11)$$

$$\tau_1 = R_1 * C \quad (12)$$

$$D = \frac{\tau_2}{2} * \omega_n \quad (13)$$

$$\tau_2 = R_2 * C \quad (14)$$

These four equations are generally applicable for any kind of PLL loop. The quantity  $K_\Phi$  is the sensitivity of the phase-detector i.e. its output voltage per degree of phase difference between the input signals. The oscillator sensitivity is given by  $K_{VCO}$  and is defined as the frequency alteration in Herz per volt of loop voltage change times  $2\pi$ .

In the circuit under discussion, the actual task of control is left to the analogue PD (A). When the circuit has achieved lock, it carries out the fine tuning control. Owing to the peculiarities of the design, the circuit noise is very well suppressed. A series of component formulas is now given:

$$C * R_2 = \frac{K_a * K_{VCO}}{\omega_n^2 * N} \quad (15)$$

$$R_1 \geq \frac{5 * R_2}{K_a} * \left( \frac{2 * D}{\omega_n} + 1 \right) \quad (16)$$

$$\frac{R_2}{R_3} = \frac{K_a * K_{VCO}}{2 * D * \omega_n * N} \quad (17)$$

$$K_{VCO} = \frac{\Delta f}{\Delta U} * 2 * \pi \quad (18)$$

where,

$f_n$  = working frequency of loop

$\omega_n$  = loop BW frequency

$K_a$  = PD (analogue) sensitivity

$K_d$  = PD (digital) sensitivity

$K_{VCO}$  = VCO tuning sensitivity ( $2 * \pi * \text{Hz/V}$ )

D = attenuation normally unit but optionally 0.7

N = total division factor

According to the Plessey data-book (5), the sensitivity of other analogue PDs can be extracted from the circuit data as follows: -



$$K_a = 10 * \frac{U_B - 0,7 - 89/\sqrt{R_b}}{2 * \pi * 50 * 10^{-12} * R_b * f_r} \quad (19)$$

where,

- R<sub>b</sub> = the external resistor at pin 2
- f<sub>r</sub> = step frequency (10 kHz in example)
- U<sub>B</sub> = PLL-IC supply voltage

He who wishes to experiment further, will find all the necessary information in the references given.

Following this basic discussion, the calculation of all the important quantities specifically for the two important frequency bands, 2 metres and 70 cm will be carried out.

**8.1. 2 m Synthesizer with a 10.7 MHz IF**

VCO range for the transmitter:

144 MHz - 145.990 MHz

VCO range for the receiver:

133.3 MHz - 135.3 MHz

The total tuning range should have a minimum of 133.3 MHz to 145.99 MHz i.e. overlapping the required range by at least 1 MHz. From this results a Δf of 15 MHz. The range of the tuning voltage should be from +1 V to +10 V (supply voltage minus the OP limits), ΔU is therefore 9 V. The average sensitivity of the oscillator, as given by formula (18), is:-

$$K_{VCO} = 2 * (5/3) * \pi * 10^6 \quad \text{rad/Vs}$$

From (19), the sensitivity K<sub>a</sub> = 300 of the phase detector A can be determined. The reference frequency, i.e. the step frequency, should amount to 10 kHz. From formulae (8) to (10) ω<sub>n</sub> to 250 1/s is obtained, whereby the actual value is rounded off from (253.35 1/s). The maximum division factor, from (3), is N<sub>max</sub> = 14599, with this value, the worst case must be dimensioned. All the limit values have now been enumerated and the filter can now be calculated:

From (15) is obtained C \* R<sub>2</sub> = 3.56 and from (17) R<sub>2</sub>/R<sub>3</sub> = 445.6. With the result from (17), R<sub>2</sub> can now be determined. It should not be above 1 MΩ as the input resistance of the operational amplifier cannot be neglected. As a good compromise, the value of 910 kΩ can be taken (standard value), whereby R<sub>3</sub> has a value of 2.042 kΩ. For the time being, the larger standard value of (2.2 kΩ) should be employed. With (16), the minimum value of R<sub>1</sub> can be calculated. This should be larger than, or equal to 18.345 kΩ, this means a standard value of 22 kΩ. Finally, the result of (15) and the determination of R<sub>2</sub>, the integration capacitor C = 3.9 μF can be calculated (4.7 μF used).

All the component values have now been evaluated and the loop should function optimally. Unfortunately, there are component tolerances that must be taken into consideration and the fact that all calculations based upon an OP have assumed that it is an ideal amplifier. This means

N <sub>min Tx</sub> = 14400	M = 360	Δ = 01/0110/1000	A = 0	Δ = 000/0000
N <sub>max Tx</sub> = 14599	M = 364	Δ = 01/0110/1100	A = 39	Δ = 010/0111
N <sub>min Rx</sub> = 13330	M = 333	Δ = 01/0100/1101	A = 10	Δ = 000/1010
N <sub>max Rx</sub> = 13529	M = 338	Δ = 01/0101/0010	A = 9	Δ = 000/1001

Table 2

N <sub>min Tx</sub> = 17200	M = 215	Δ = 00/1101/0111	A = 0	Δ = 000/0000
N <sub>max Tx</sub> = 17599	M = 219	Δ = 00/1101/1011	A = 79	Δ = 100/1111
N <sub>min Rx</sub> = 16344	M = 204	Δ = 00/1100/1100	A = 24	Δ = 001/1000
N <sub>max Rx</sub> = 16743	M = 209	Δ = 00/1101/0001	A = 23	Δ = 001/0111
Series	M9..M0		A6	.A0

Table 3



that an inspection of the output signal with a spectrum analyzer, or a receiver, and possibly some cut and try work may be necessary. Individual cases may call for some experimentation, as there can be no general recipe for an optimal solution.

The reference oscillator is equipped with a 4 MHz crystal. According to formula (5), the reference divider must be adjusted to the value  $R = 200$ . Expressed as a binary word, this amounts to:  $R = 200$  (binary): 000/1100/1000 in the series R10...R0.

The divider factors for the programming device are determined according to the expressions (3), (4) and (6). Their respective binary values are appended. Only the limit frequencies have been calculated ( $P = 40$ ) (table 2).

### 8.2. 70 cm Synthesizer with a 21.4 MHz IF

Send frequency: 430 MHz - 439.975 MHz

Receive frequency: 430 MHz - 418.575 MHz

Frequency span:  $\Delta f = 36$  MHz

Tuning voltage range:  $\Delta U = 9$  V

Oscillator sensitivity (from 18):  $K_{VCO} = 2 \cdot \pi \cdot 10^6$   
rad/Vs

Phase-detector sensitivity (19):  $K_a = 300$

Loop frequency (10):  $\omega_n = 600$  1/s

Reference (step) frequency:  $f_{ref} = 25$  kHz

maximal division factor from (3):  $N_{max} = 17599$

Hence:

from (15):  $C \cdot R_2 = 1.19$

from (17):  $R_2/R_3 = 357$

$R_2$  rounded to 680 k $\Omega$ ,  $R_3$  to 2 k $\Omega$

$R_1$  must equal or be greater than 12 k $\Omega$ , 15 k $\Omega$  used

$C$  = determined from (15) and the value of  $R_2$   
1.75  $\mu$ F, 2.2  $\mu$ F used

Finally, the division factors for the programming device are given in table 3.

The reference oscillator also uses a 4 MHz crystal. From (5)

$R = 80 \cong 000/0101/0000$  series R10...R0

## 9. LITERATURE

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# 4-Channel 140 MHz Oscilloscope Part 2 (Concluding)

## Salient Circuit Details

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### 2. PRE-AMPLIFIERS

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Fig. 2.1. shows the arrangement of the input voltage dividers and the pre-amplifiers. Y amplifiers for oscilloscopes are usually designed as differential amplifiers. This principle is adhered to in this case but they extend right up to the inputs. This eliminates the irritating requirement for the summation of two channels (one of which must be inverted) when making differential measurements. All channels for this mode are available.

An unused input can be switched to ground for reference purposes by means of S1. Switch S2 serves to switch between DC, AC and 50  $\Omega$  inputs. In the 50  $\Omega$  position, AC coupling has also been provided but with a lower frequency limit of 1.2 MHz. This is advantageous when measuring signals with a high DC component as, for example, in ECL circuits. This makes the switching simpler and also reduces the stray capacitance. At the input socket is located a contact plate K which switches a signal to the character generator when a suitable divider probe is plugged in. This alters the indicated range by a factor of 10.

The input signal is taken to a compensated voltage divider, having division factors of 10 and 100 and selected by miniature relays. They are so constructed that both the input capacitance and the input resistance remain constant during switching. The compensation is adjusted by C3 and the input capacitance by C2. Capacitor C4 serves as a load capacitance for balancing the adjustment range. The combination R4/R5 protect the input transistor pair. It is compensated by C6.

Following T1/T1', the signal is divided in 2 and 5 steps by a low-ohm divider circuit before being fed to the trigger or Y amplifiers. The resistors R6 and R7 damp out any tendency for UHF spurious oscillations to occur in the pre-amplifier when it is subjected to certain input terminations.

This arrangement of the range switching has its advantages and also its disadvantages. Amongst the latter is the tendency of the null-line and various common-mode input ranges in the differential mode, to be offset during range switching in 1-2-5 steps. The overwhelming advantages that a lower number of dividers directly at the input are required and that a simple 2-5 division factor requiring only one compensation capacitor suffices.



Using relays for range switching proved enormously successful but only high-quality relays using gold-plated contacts should be used. The stray capacitance to ground from the relay contacts, at 7 pF per relay, is relatively high which is the reason why only two dividers lie directly at the input.

### 3. Y- AND TRIGGER-BUS MANAGEMENT

Fig. 3.1. shows the type of structure which is required to switch the various signal sources to one of the buses – dependent upon priority signals. A switching sequence must not take longer than 100 ns to perform and this dictates that the use of unsaturated logic and current control is mandatory

Both Y- and trigger-bus are terminated with 470  $\Omega$  resistors (R1 and R2 for the Y-bus shown here). They serve as load resistors for the active amplifier output represented by T1, T2, D1 to D4 and R3. As long as the control line inhibits current through R3, the total collector currents of T1 and T2 is diverted through D2 and D3. This is so small that the collector potential is greater than the bus potential blocking D1 and D4 thus isolating the amplifier from the bus.

If a control current of, in this case 36 mA, is flowing, the potential at the anodes of D2 and D3 is lower than the bus potential and T1 and T2 deliver the signals via D1 and D4 to the bus.

#### 3.1. Enabling the Control Current with Priority Switching

Both the Y- and the trigger bus have two priority circuits provided: T3 to T8 and T9 to T13 respectively. The conditions of T3 to T8 are considered first. The transistor with the highest base voltage delivers current via R9 to the appropriate control line. The sequence is defined by means of the various high H-levels at their bases. This gives priority to character display over the normal oscilloscope operations. All the other control

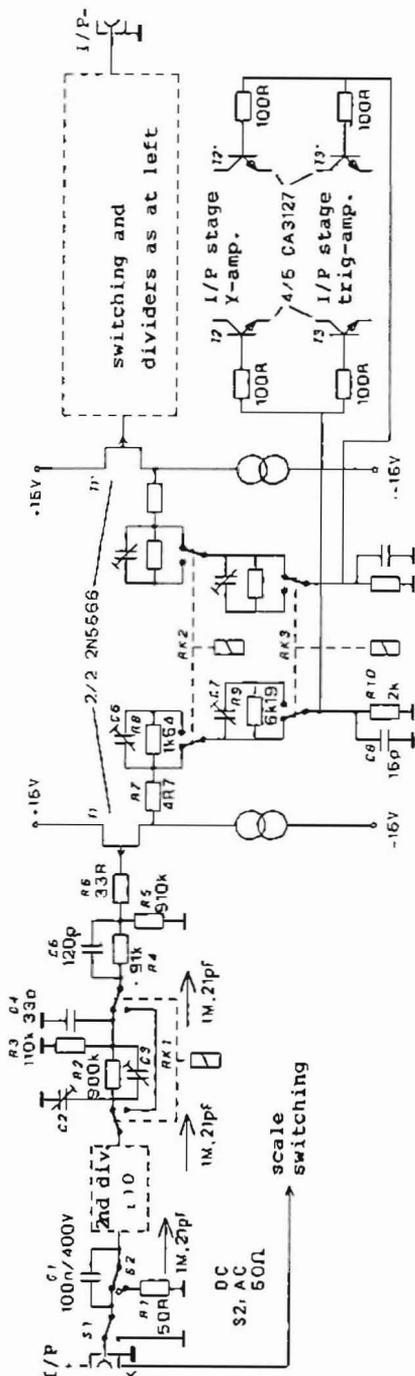


Fig. 2.1.: Pre-amplifier input stage

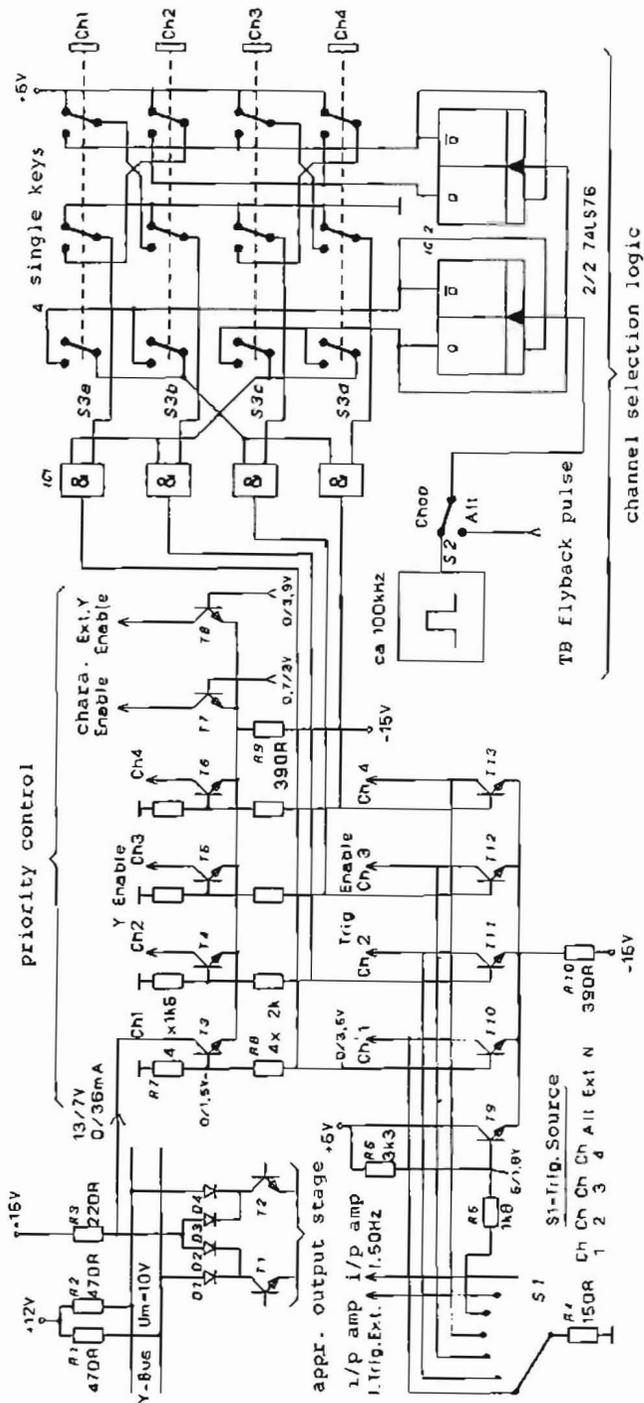


Fig. 3.1.: Bus management

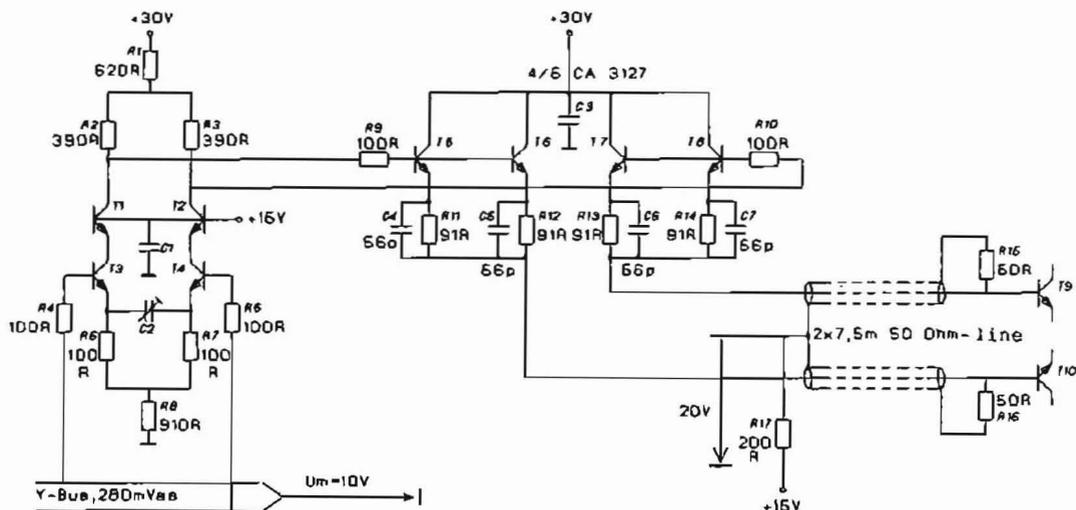


Fig. 4.1.: Cascode amplifier and delay-line driver

sources are isolated via T8 from the Y-bus by application of an external signal applied to the X-Y-Z-socket. Thus, only external Y-signals are forwarded. Transistors T3 to T6 switch the lowest priority stages to the selected input amplifier.

The trigger bus organization is determined by the position of S1 and the channel selection. If S1 is in position CH1 to CH4, transistor T9 conducts through R10 to the +5 V supply rail. The current through R4 determines the channel trigger source but it cannot be a channel connected to the Y-bus. On position ALT, transistor T9 is blocked and the signals from the channel selection logic determine the trigger source. When alternate beam operation is selected, the triggering is always active at the input actually in use. This enables a stationary trace to be obtained even with signals of differing frequency.

Two further positions of S1 serve to select the external trigger (EXT) or triggering from the mains frequency.

### 3.2. Channel Selector Switch

The sequential switching of the input amplifier can be carried out from two sources: a 100 kHz

generator for CHOP-operation and the time-base fly-back pulse on the ALT-mode. This is selected by switch S2, which takes the signal on to two divider flip-flops having a total of four outputs.

The switches S3a to S3d together with the AND-gates of IC1, interconnect these outputs such that, by the operation of push-button switches, the appropriate channel is always active in the correct sequence. It is also possible to switch a channel in or out which represents a considerable simplification in control over that offered by proprietary 4-channel oscilloscopes.

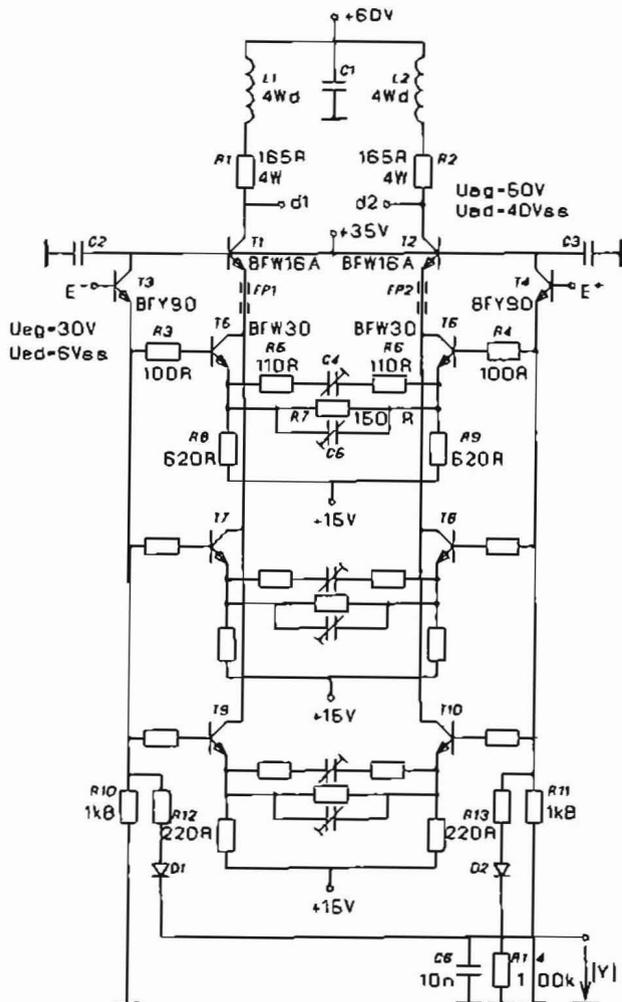
## Y-AMPLIFIER AND DELAY LINE

### 4.1. First Amplifier Stage and Delay-Line Driver

In the arrangement of fig. 4.1., the extreme left-hand stage is an amplifier which magnifies the signals from the Y-bus. This is a cascode differential amplifier with a voltage amplification  $V_u = 3.9$ . It consists of R1 to R8, T1 to T4, the decoupling capacitor C1 and the compensating



Fig. 4.2.: Y-plate final amplifier



capacitor C2. Resistors R4 and R5 serve to dampen VHF-self oscillations.

The 10 V DC-pulses act through R6, R7 and R8 to produce identical quiescent currents through both transistor branches T1/T3 and T2/T4. These currents are little affected by the absolute amplitude of the DC-pulses owing to the relatively high value of R8. A common resistance of 200  $\Omega$  lies between the emitters of T3 and T4 which serves

for the distribution of the transistor quiescent currents under differential input signal conditions.

Neglecting base currents, the collector currents through T1 and T2 equal the current flowing through T3 and T4. Any current difference produces a differential PD across R2/R3 which is available as an amplified signal. Resistor R1 serves to adjust the correct output pulse level to approximately 22 V. Transistors T1 and T2

prevent any feedback from output to input because the differential signal potential at their emitters is practically zero. They perform the same sort of shielding function as the screen grid does in a tetrode electron-tube.

The signal from the cascode stage is taken to two emitter follower pairs (T5 to T8) which utilise a common substrate and are therefore in close thermal contact with each other. Owing to the relatively high currents and low-level signals used in this application, there arises the problem of drift following voltage surges. The emitter currents of each transistor pair are added across resistors R11/R12 and R13/R14 and flow into the delay line. The delay-line terminations R16 and R18 have the drive voltage for the following stage impressed across them. Both current components are taken via R17 to the +15 V supply rail. The latter also supplies other stages.

Capacitors C4 to C7 lift the frequency response above about 30 MHz. This affects the input termination but this is of little consequence as the lines are terminated at their outputs and therefore there is no return energy.

#### 4.2. Y-Final Amplifier

Following two more stages of differential amplification (not shown), the Y-signal is taken to the final stage shown in fig. 4.2. Again, this employs a cascode circuit but in this case, the lower transistors comprise three pairs (T5 to T10). These serve as a higher level of isolation for the emitter followers (T3/T4). The form of current division has the advantage of increasing the limit frequency above that offered by the previously described stage. Single transistors with the necessary dissipation and limit frequencies are also available but at a fairly high purchase price.

The emitter circuit of the individual pairs are comprehensively compensated in order to ensure a flat frequency response over the desired frequency range of the instrument. Inductors L<sub>1</sub> and L<sub>2</sub> have the effect of increasing the limit frequency from 130 MHz to 140 MHz. This is the stage which has, in fact, the lowest bandwidth since it has to provide sufficient gain for the high-level output

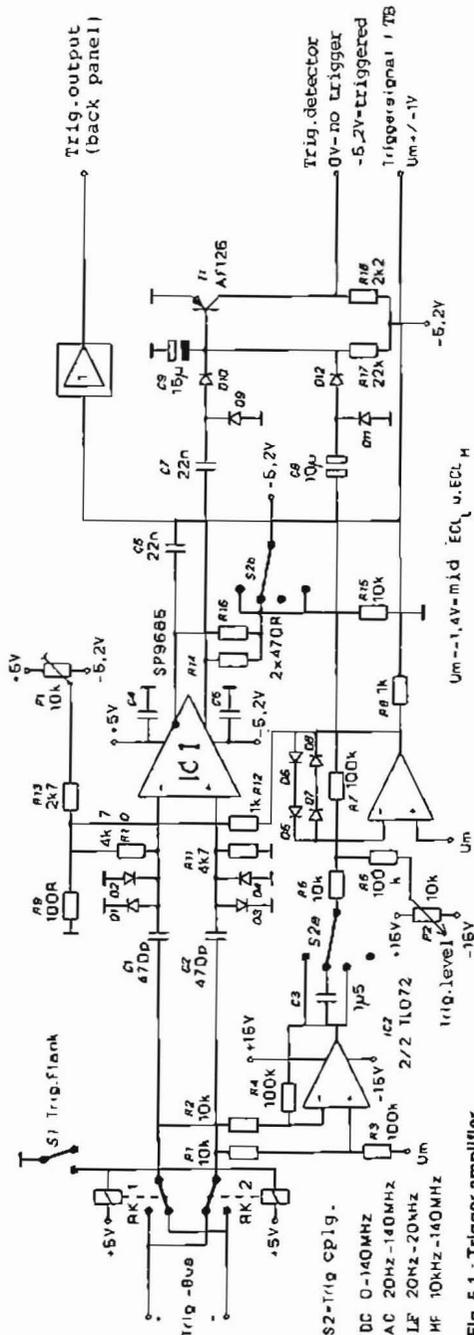


Fig. 5.1.- Trigger amplifier



voltage. This means that the 140 MHz band limit can be achieved but at half the trace response. At greater amplitudes, the rise time begins to deteriorate.

The emitter current of T5 to T10 is taken to the +15 V supply via the line driver (see fig. 4.1.). This double utilization of energy, results in a reduction in the unit's consumption and thereby the final-stage temperature.

The emitter followers T3 and T4 also drive a circuit for the composition of the Y-signal. Components D1 and D2, C6 and R14, R12 and R13 serve to limit the current. The composition component is taken to a comparator and then on to a micro computer. It can then, with the help of a trigger status signal, provide a voltage for the automatic range-switching of the input amplifier.

The composite value reaches its highest point during the character display, as these are located at the extreme upper edge of the CRT screen. C6 and R14 are so chosen that this peak is truncated before the next line display and the true Y-value is read by the controller.

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## 5. TRIGGER AMPLIFIER

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The trigger amplifier schematic is shown in fig. 5.1. The trigger bus is first taken to two low-capacity Reed relays which select the trigger flank polarity. The signal then splits into an HF- and a DC/LF-path. Both paths are conceived as differential amplifiers.

The HF-path comprises C1, C2, the limit diodes D1 to D4, R9 to R16, P1, C5 and IC1, and is activated with S2b. The fast-acting comparator IC1 possesses two complementary ECL open emitter outputs which are shut-off when the emitter resistors R14 and R16 are taken to ground via R15. Only when the bias lies at -5.2 V do the output transistors conduct. The output transistors are adjusted by R12 from the output of the DC/LF path which makes it partly dependent upon the setting of the trigger-level pot-meter. More on

that later. The zero points of both paths are equalized by P1 and R13.

The signal from the negated output is taken via C5 to a summation point which then represents the combined trigger signal. A signal from the non-negated output is taken to the Villard doubler, D9 and D10, which, when correctly controlled by IC1 develops a 0.5 V potential across C9. Transistor T1 is, in turn, blocked off and a signal can be taken from its collector to indicate the trigger state. Diodes D9 and D10 must be the fast Schottky type, as the potential at the cathode of D10 in the quiescent state can only be some -0.6 V. This can allow T1 to conduct safely as it is an old germanium type.

The DC/LF path comprises two op-amps, the first of which is connected as a differential amplifier with a voltage gain of 10. Switch S2a determines the coupling, AC or DC, to the following stage. The second stage has a gain of 10 also but the output signals are limited to  $2 V_{pp}$  by means of diodes D5 to D8. The pot. P2 and R6 control the trigger-level setting. The reference voltage for this path is  $U_m = -1.4$  V and at the output there is an ECL-compatible signal. This is taken to the summing point via R8 and via C8 to the Villard doubler both having the same functions as previously described.

The correct signal control is only possible when, as in this case, the signals are in the specified frequency range with equal amplitudes and phases. The summation point also must be at a high impedance in this range. This ensures that signals in the overlap range can be handled by both paths in the same fashion.

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## 6. TIME BASE

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There are two time bases provided, they operate as follows: -

- TB1: Only the first time base is displayed  
 MIX: From a freely settable point on the X-position, a second (faster) time base is initiated: expanded trace

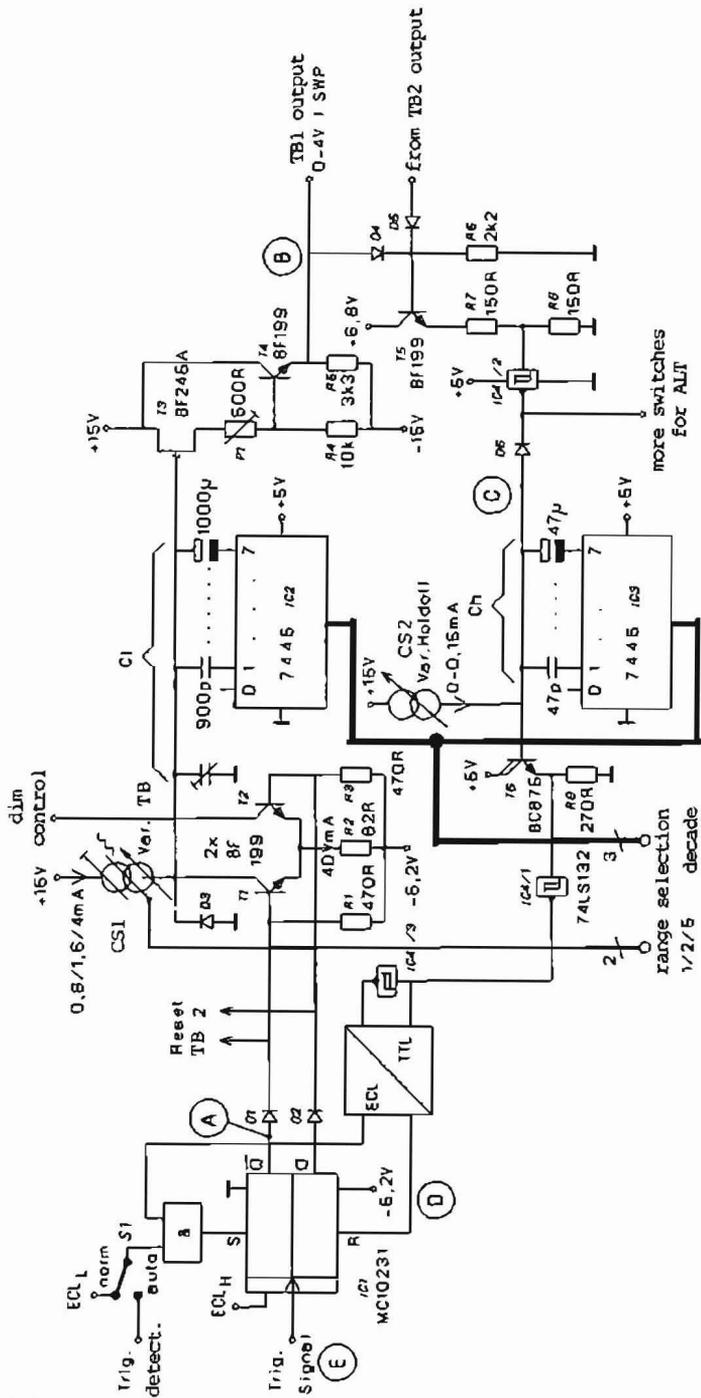


Fig. 6.1.: Circuit diagram of time base 1 (TB1)



**SEARCH:** The second time base after its initiation is given an intensive illumination "bright-up".

**TB2:** The "bright-up" conditions on TB2 occupy the whole of the trace.

The functioning of both time bases is identical, only their initiation is different. The horizontal fly-back occurs if one of the two time bases has reached its end value.

### 5.1. Time base 1

**Fig. 6.1.** shows the circuit schematic which depicts the minor functions in block form. The heart of the linear ramp is the switchable timing capacitor  $C_t$ . The latter is charged via an adjustable current source  $CS_1$ . It can be varied in three ways: A calibration function, a range control in 1-2-5 switchable steps and a continuously variable control for the time base.

The decade selection is effected by the switching of  $C_t$  with the open-collector outputs of the 7445 decoder. This elegant remote-control solution functions perfectly, discharging  $C_t$  by quickly biasing the conducting transistor from its active condition. In order to ensure a complete discharge, however, the pause between every second sweep – the "hold-off" time – is made slightly longer. The stray (damaging!) capacity of all the outputs combined amounts to some 40 pF and is independent upon the saw-tooth waveform voltage. The linearity is therefore satisfactory, even at the highest sweep speeds. The capacitor for the highest sweep-speed range is smaller than its reference value (100 pF) and must be selected for the individual decoder in use.

In order that the constant current source ( $CS_1$ ) is not loaded excessively, the ramp is buffered by high impedance T3 and T4 in a voltage follower configuration, the offset of which is adjusted by P1. This sets the output voltage on a reset time base to zero.

The considerations to follow rely heavily upon the timing diagram of **fig. 6.2.** for their explanation. This diagram indicates numerically the timing sequence.

A Schmitt-trigger IC4/2 is activated via D4, T5, R7 and R8 as soon as the ramp at the emitter of T4 has attained its final value. The hold-off capacitor  $Ch$  is discharged via D6 (1) and the trigger flip-flop IC1 (2) is reset via T6, IC4/1, IC4/3 and the TTL-ECL level changer. This results in the potential on T1 base being higher than at the base of T2 (3). The discharge current (determined by R2) of  $C_t$  is considerably larger than the charge current from  $CS_1$  (4). The fly-back time is accordingly, for a given  $C_t$ , always the same so that the hold-off time can be no smaller than any decade division. Diode D3 limits the voltage on  $C_t$ , following the discharge, to a definite start value for the ramp to maintain.

When the voltage at the emitter of T4 falls because  $C_t$  is discharging, a logic 1 (5) will occur at the output of IC4/2, as soon as the discharge state has reached a certain value.  $Ch$  is now charged via SC2 and when the threshold of IC4/1 has been exceeded, the reset pulse for the trigger flip-flop is ended (6). The following sequence of events depends upon S1 and the input "Trig. verify".

In position "norm" the left input of the AND-gate is at logic 0 and there is therefore no set pulse at the trigger flip-flop. It will only be set by a positive flank at the sync input which replaces the H-level at the D-input (7). As a consequence, T1 is blocked and the ramp begins (8). If S1 is in position "AUTO" and there is no trigger signal (trig. verify = logic 1) the end of reset pulse of the S-input is activated and the ramp starts again immediately. The sequence of events as in the "norm" position can only occur when a trigger signal has been verified.

The voltage at the collector of T2 is used during the ascending ramp period to control the fly-back sampling circuit. Diode D5 monitors the output voltage of time base 2. If this is in operation, the flyback is initiated from that, it then reaches its final value much faster.

Diodes D1 and D2 serve the level shifting in order that T1, at the resetting of  $C_t$ , does not saturate and so ensuring a prompt start of the ramp.  $CS_2$  is variable from zero to its end-value and the hold-off time can thereby be extended indefinitely. This is very useful for the display of very complicated signal sequences.

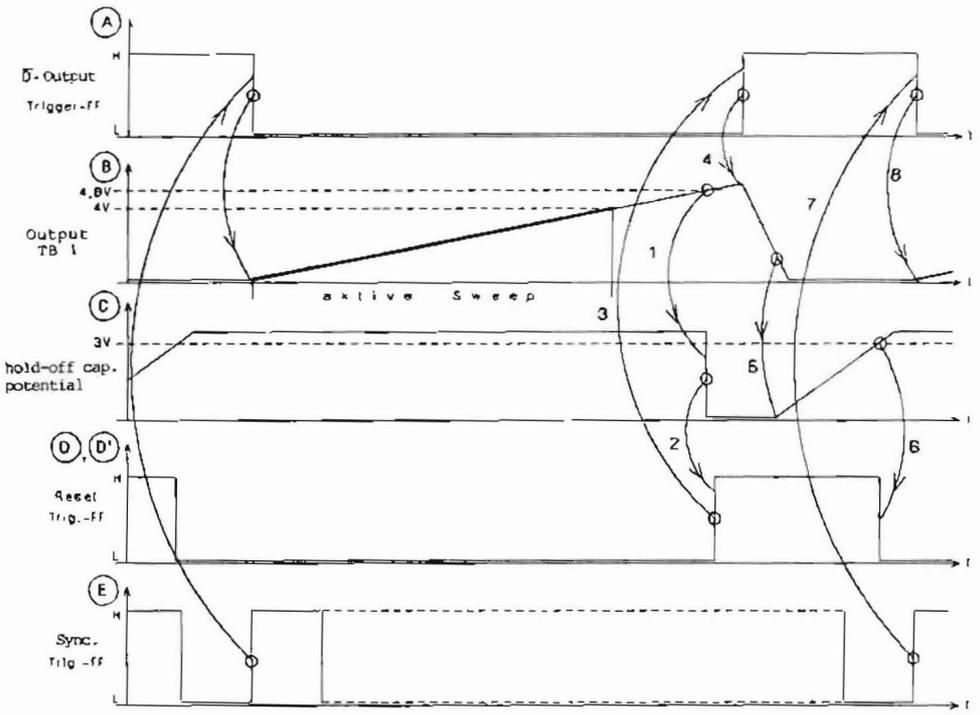


Fig. 6.2.: Timing diagram for time base 1

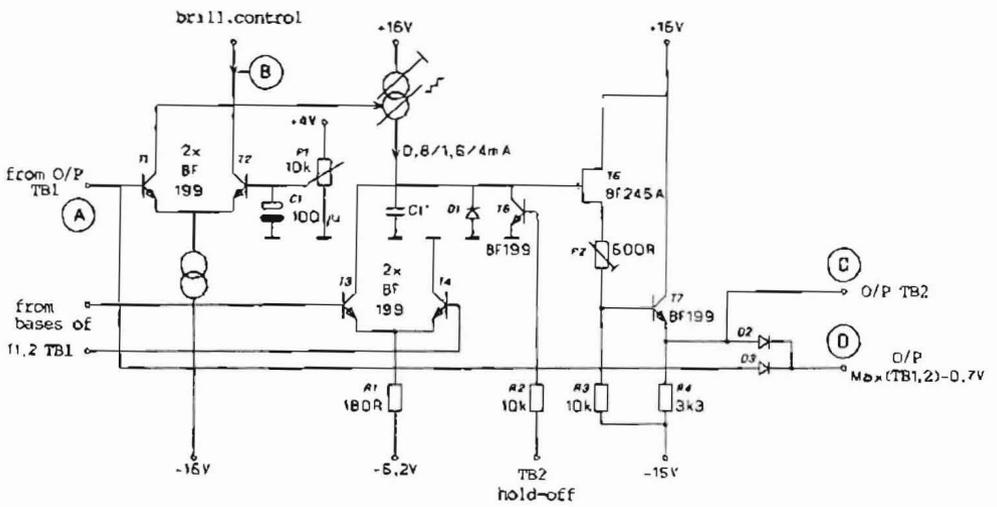


Fig. 6.3.: Time base 2 circuit diagram

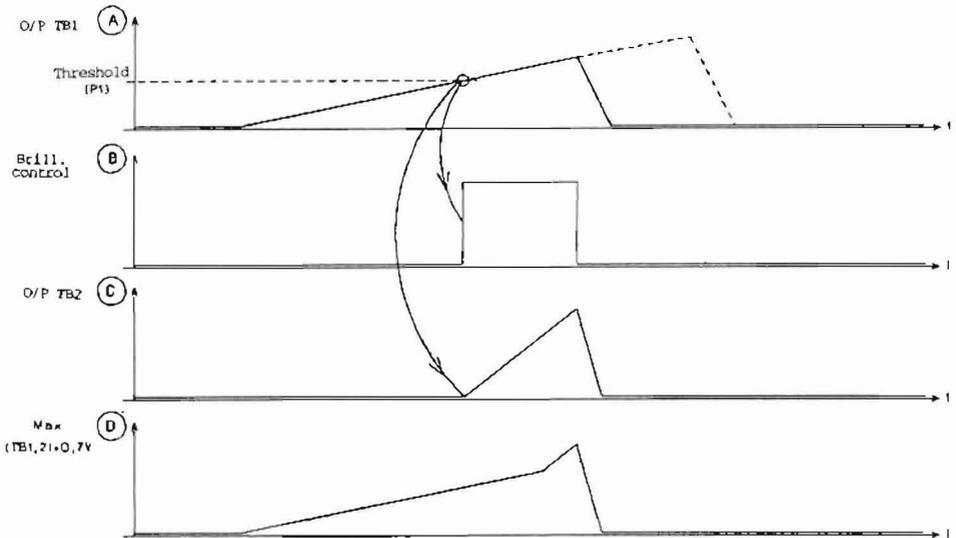


Fig. 6.4.: Timing diagram for the various time base modes

## 6.2. Second Time Base

The circuit of fig. 6.3. shows that for the production of the ramp, the output amplifier and the reset mechanism, the same principles apply to TB2 as to TB1. The current source in TB2 can, however, be switched-off. It is first of all activated when the voltage at the output of TB1 exceeds that at the wiper of P1. Transistor T1 then starts conducting thus cutting off T2. This can be used for the brilliance control of the CRT beam. The maximum value of both time bases is formed by diodes D2 and D3 and this is used in the MIX-mode for the horizontal sweep. Transistor T5 blanks TB2. A few important points in the sequence of the ramp timing is given in fig. 6.4.

The brilliance control, pulse B, is used for the "SEARCH-mode". At the same time, the TB2 ramp goes from zero to its end value. This may be seen on the trace when TB1 ramp is cut short and the presentation then ends at the right-hand edge of the bright-up trace.

The wave form D shows that the similarity of both time bases is achieved after a longer time fol-

lowing the start of TB2. The expanded portion in the "MIX-mode" is therefore not identical with the bright-up trace of the "SEARCH-mode".

## 6.3. X-Mode Switching

The circuit schematic of fig. 6.5. shows the switch S1 which has one wafer, but carries out all the necessary switching functions to enable normal operations (as described in chap. 6) to be switched over to the X/Y-mode. This includes the influence on the time bases and the brilliance control, but above all, the selection of the correct signals for the X-final amplifier. At this stage, the horizontal character components and the external (EXT-X) are superimposed. Fig. 7.1. shows the diode switch for this purpose. This can switch signals up to about 20 MHz in a time of 200 ns. This high-switching time is only necessary for the display of characters.

The current, controlled by R17, is taken via a priority control (T2 to T7) similar to that described in chap. 3, to one of six lines in each collector. It

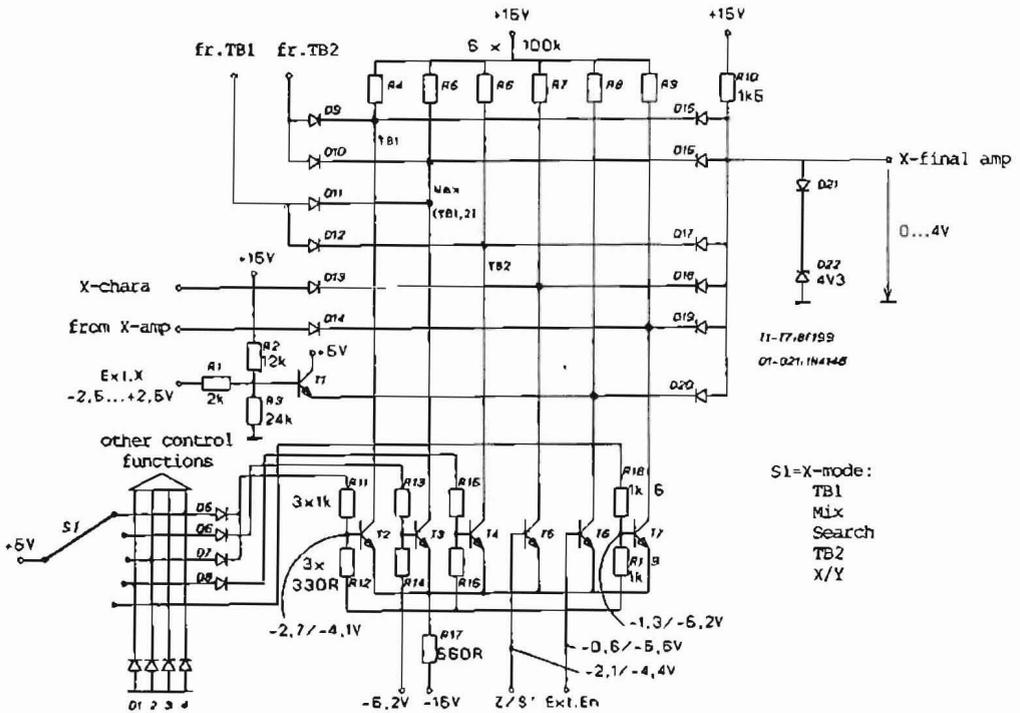


Fig. 6.5.: X-signal priority control and diode switch

divides between a left diode and a right diode, D9 and D15. The current through D15 is determined by R10 and the current through D9 flows through the low-resistance output of TB1. The currents through the diodes are then unequal and dependent upon the input signal. Owing to the steep transfer characteristics of the diodes, no harmful non-linearity effects are evident. Also, the output signal wave form approximates very closely that of the input signal.

Transistors T2 to T4 control the TB1, max (TB1, 2) and TB2 signals but at low priority. They are controlled by the position of S1 via a diode logic having an appropriately low base level. Diodes D5 and D7 form an OR-function, D6 and D8 serve to equalize the base potential for T3 and T4. Diodes D1 to D4 clamp the L-level to the contacts of S1 at -0.7 V in order to provide definite conditions for the other control functions.

Transistor T5 is controlled by a level-delayed Z/S' signal from the micro controller. The H-level, at -2.1 V provides for the next highest priority - as in the Y-signal switching. The next level is achieved by the selection of X/Y-mode with S1 and T7. This switches off the character display. In this mode, the signal from the trigger bus is taken via the X-amplifier to D14 and on to the X-final stage. It then lies at a point at the X-axis which has been selected by the channel selection for the Y, as a trigger source. The X-amplifier matches the scaling in the X- and Y-directions. The axis drives are, of course, dissimilar, because the CRT display area is not square.

The external X/Y/Z-modes have priority above all other scope-functions. It is activated with a switching signal from the EXT. X/Y/Z terminal via T6. The EXT.-X signal is taken via a matching network, R1 to R3, at the correct working level



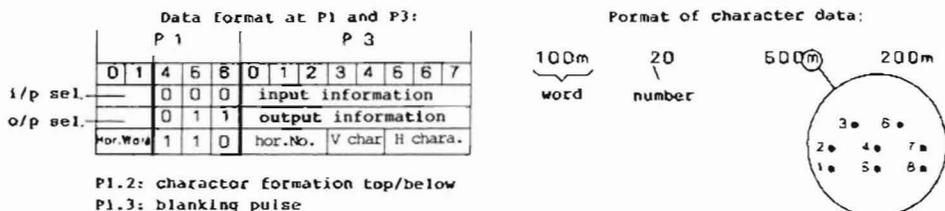


Fig. 7.2.: Data format at P1 and P3

for the X-final amplifier. Instead of using a diode, the network is buffered by an emitter follower T1. The input terminal EXT.-X, as also EXT.-Y, has a deflection sensitivity of 0.5 V/cm balanced about the zero point.

In order to prevent the over-driving of the X-final amplifier in X/Y and in external operation, D21 and D22 have been provided

## 7. MICRO CONTROLLER AND CHARACTER GENERATOR

The micro controller 8051 has the job of reading the keys, changing the measurement ranges and the delivery of the characters onto the screen. In the AUTO-range mode, it monitors the trigger and Y-signal for the range changing of the active pre-amplifier. Another circuit is responsible for the adjustment of the time bases. It counts the number of oscillations per sweep and retains them. The AUTO-range mode is only possible on one channel and on one time base, as otherwise there would be very large technical problems to overcome. In addition, the beam position would have to be digitally controlled.

The circuit of the 8051 is shown in fig. 7.1. P3 has the function of a databus, P1 has a control function. There are 32 inputs and outputs available with the input multiplexer IC1 to 4 and the output registers IC7 to 10. Of these outputs, 4 x 4 are used for the pre-amplifier range relays and 2 x 5 for the control of the timing capacitors and the time-base current source.

The input- and output-power group selection is carried out by P1.0 and P1.1, P1.5 switches an input group to P3, P1.6 initiates the writing into an output register from P3. P1.4 delivers signal S/Z and initiates thereby a switch-over into the character display. In the horizontal axis, the positions of 256 pixels are determined. The signal for the X-axis is formed with a DAC, IC11, and matched in amplitude and nulled in two op-amps.

In the vertical axis, the individual characters have only four pixel positions which are controlled by P3.3 and P3.4. P1.2 determines whether above (range indicator pre-amp.) or below (range indicator: time base) is displayed. The generation of the requisite analogue signal is achieved with T1 and R1 to R4. When T1 is blocked, there is a PD of 0.7 V across R1 which means that a symmetrical drive to the emitter is developed. The Y-components are also processed, in terms of both amplitude and sense, by means of two operational amplifiers.

The control of IC11 and for the Y-display component generator, at first seem to be somewhat complicated but there is quite an elegant software implementation available. P1.5 gives a blanking pulse which is used to make the transistors between characters invisible on the screen. The time available for a pixel is about 3  $\mu$ s for a flicker-free display, at a 50 Hz picture rate, and the necessary relationship between the time for the characters and for the normal scope display. All the components in the signal path must therefore have a correspondingly short decrement and the display sequence of the pixels so chosen that the smallest transitions are required.

Figure 7.2. shows, against the indicated hardware, the resulting data format at P3, dependent

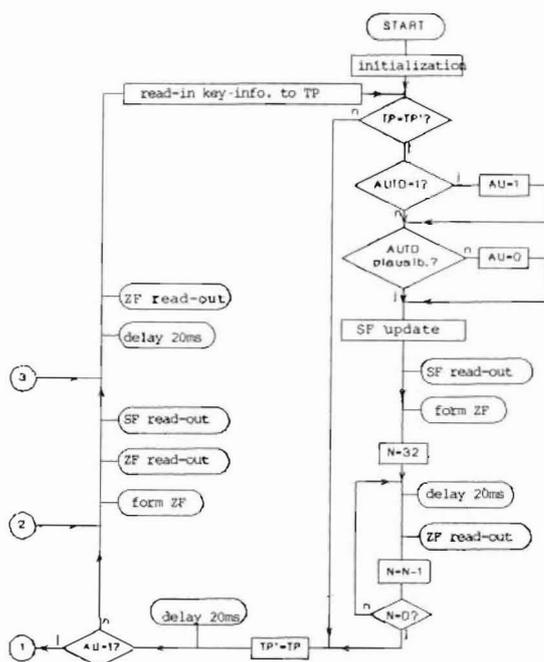


Fig. 7.3.: Flow diagram for keyboard request, range change and read-out of switch- and character field

upon P1. To the right of the diagram, is the formation of the words and figures from pixels. It can be seen that during the character display, the upper five bits from P3 represents the whole of the information for a character. The required short pixel time can only be achieved by using a linear command sequence, the pixel position being immediate data. Further switching of a figure position is achieved in increments from P3 and in a word position by increments from P1.

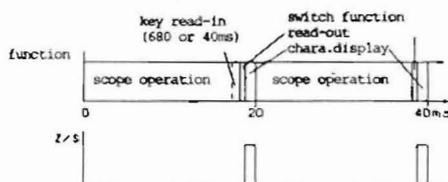
### 7.1. Program Sequence in Normal Manual Operation

In compiling the program it must be borne in mind that the presentation of the characters must be equally disposed to one another irrespective of any other functions which are in progress. This is achieved by tailoring the delay time-constants for key debouncing etc with 20 ms display cycles. In every cycle, the number of pixels necessary are

#### Variables and fields

TP = keyboard buffer, new value  
 TP' = keyboard buffer, old value  
 AU = auto range flag, H=active  
 SF = switch field, store area for pre-amp and TB range switching  
 ZF = character field, store area for character read-out

#### Timing diagram



read out (600  $\mu$ s max.) and inserted into the scope mode for a period of 20 ms. The controller reads out only the measurement range of the active channels or time bases, the others are blanked.

For a minimum delay for the call-up of the character pixel chain, a byte is made available for each word in the so-called character field (CF). This contains pre-arranged, (by suitable mask-programming) easily convertible information. Other criteria are necessary for activation of the range determining elements, for which, a switching-field is prepared. In this field, single bytes contain the nulls and ones which are connected to the control lines. Upon range changing, the switching-field is change and the corresponding character field is formed by a sub-routine.

Fig. 7.3. shows the flow diagram for a normal function sequence.

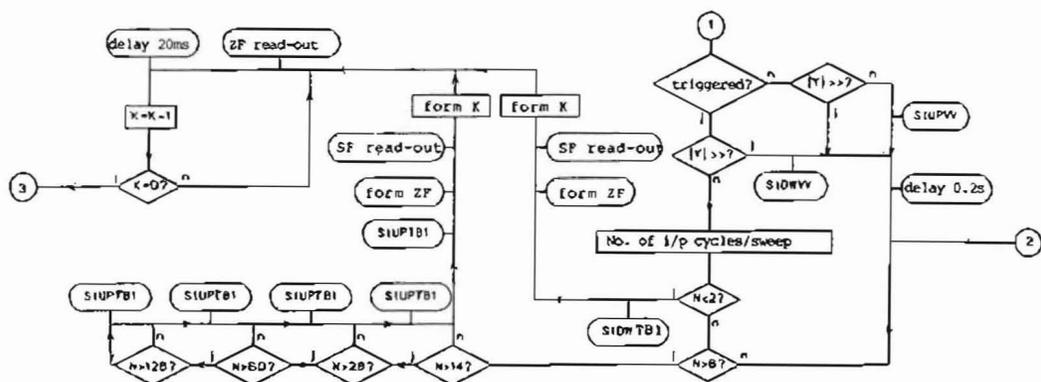


Fig. 7.4.: Flow diagram of AUTO-range operation

Contact de-bouncing is carried out by a key buffer which is shifted prior to every read-in. In this manner, the old value may be directly compared to the new one. When they are equal, the corresponding function is triggered. First of all, the key is checked for correct operation of the AUTO-range function, if yes, the "AUTO flag" is set. Afterwards, a check is made to see that only one input and one time base has been activated (AUTO plausible?), if not, the "AUTO flag" is redundant.

For the next step, the switching field is up-dated and read-out and the character field is formed. Upon changing the switching field, the range limits are monitored, especially time base 1 must not be allowed to become faster than time base 2. When they are equal, a lock-in of the second time base is carried out – as normal with mechanical pendants. In the switching field, only active channels or time bases are changed, the over-lapping of the time bases is also prevented.

After these functions, the program runs in a delay loop of 32 read-out cycles where the next key-board request is awaited. This is also the time constant for the repeat function should the key be constantly pressed. The update of TP, a delay and a request of "AUTO flags" are following. If deleted, the character field is reformed and read out. This seems to be a little superfluous but it is necessary for AUTO-range operation after

the engagement of connector 2. After a further read-out cycle, the program returns to its starting point.

## 7.2. Program Sequence in the AUTO-Range Operation

In this operational condition the input amplifier range is selected. Only then, if a valid trigger signal is obtained, the appropriate time base is switched over. The design of the first function posed some difficulty in finding well defined switching criteria. A transitory peak value, in any direction, is relevant for a maximum amplitude – stored in a capacitor. On the other hand, for the minimum amplitude, which is responsible for the good visibility of the signal on the screen, an AC-voltage amplitude must be measured, as this alone, does not affect the beam position.

To realize both methods of measurements for the specified bandwidth, seemed to be a little too much. Therefore, for the minimum amplitude, an available trigger signal was chosen as the criterion. A trigger signal must be present, in any case, for the correct oscillation count for the time-base switch-over. If the trigger level is too high, it can lead to iteration between the two ranges.

Fig. 7.4. is a flow diagram which shows the operation of the AUTO-range function. From



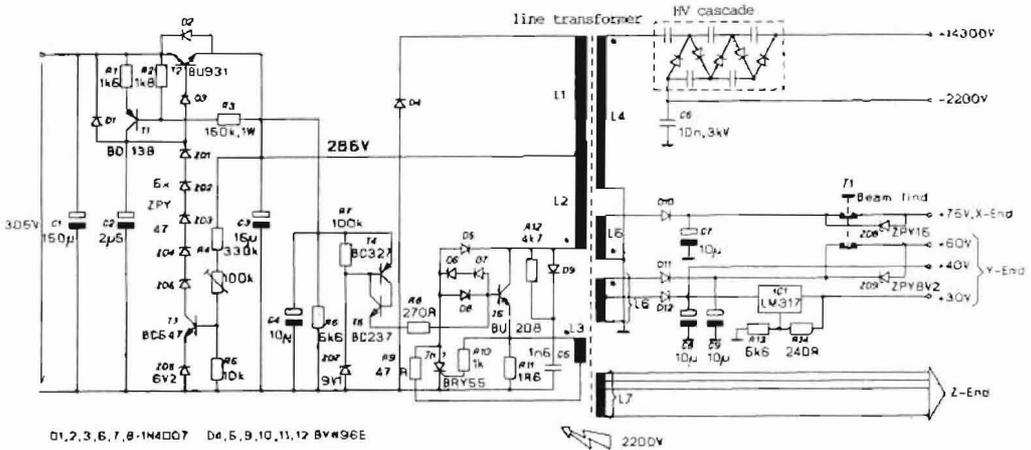


Fig. 9.1.: Power supply unit

order to modulate the beam, the signals for the brilliance control and blanking must be translated to this region. They are then amplified for the driving of the tube.

The blanking is carried out by increasing the cathode's potential and the brilliance control by increasing the potential on the Wehnelt tube. The signal path of the brilliance control is considered first of all in fig. 8.1.

The current from TB2 controls the fast opto-coupler IC2. Its open-collector output causes a current through T3, via R7, when it is conducting, which, as in a cascode stage, is used for isolation purposes. There is then a PD across R9 which is taken to the Wehnelt tube via ZD1 and C4, P1 and the speed-up capacitor C5. The potential across ZD1 and the position of P1 determine the working point between the Wehnelt tube and the cathode and therefore the basic brilliance of the CRT.

The base of T3 is held 0.7 V under the reference potential by means of D3 and R6 together with D2. The object is to prevent saturation and thereby sharply decrease the switching time. The part of the circuit for blanking is similar,

except that the switching time must be even faster. This is accomplished by increasing the control current by reducing the collector resistance of T2. The emitter follower T1 passes this high current via R5. A speed-up capacitor C1 lies across the opto-coupler IC1. In order that this has a sufficiently high signal voltage, the level difference is increased in the primary side of IC1 with R1 and R2.

The frequency over which C1 will be effective, must be well over the 20 kHz switching of the -2200 V supply in order that the residual AC components do not become visible as brilliance modulation. Even 2 V<sub>DP</sub> would cause this! It is for this reason that a very fast opto-coupler is used here.

The other electrodes of the CRT are driven in a very simple fashion, largely thanks to the in-built, finely adjusted, correcting magnets. Only the astigmatism and focus needed to be dealt with, the latter only at high brilliances. The focussing is achieved by an adjustable voltage divider R10, R11 and P2 across the -2200 V supply. The astigmatism correction voltage is controlled by P3 and taken from a 50 V supply which is the mid-potential between the four deflection plates.



## 9. POWER SUPPLY

The power supply is shown in fig. 9.1. and has no voltage regulator, as such, for the higher voltages. It really comprises a series regulator which produces a stable 285 VDC supply and a following switched-mode supply.

The HV-Darlington T2 is the series-regulator transistor. Its base is raised above the potential on the current supply R1 to R3 and T1, for as long as the base of T3 takes to reach a value of 6.9 V (via R4, P1 and R5). Transistor T1 then conducts and sinks T3's base potential via ZD1 to ZD5. This old principle is only used here in a modified form, using the zeners and selected transistors, on account of the high voltages involved. The combination of the B-E junction of T3 and the 6.2 V zener diode, results in an ideal temperature compensation.

The current supply using T1 is necessary in order to limit the power dissipation in the ZD1 to ZD5 diodes to within the range of input voltages in question. Reverse-connected diodes, D1 to D3, protect against back-EMFs which occur during the off-switching of the instrument.

The chopper functions in a feedback circuit principle utilizing T6, L2 and L3. A completely freely-oscillating feedback oscillator would result in an insufficient decay time due to storage effects, thus endangering the transistor's SOAR. For this reason, a switch-off mechanism is provided comprising R10, R11 and Th1 which rapidly conducts away the base current of T6 as soon as a certain emitter current has been reached. This prevents the onset of saturation and the circuit is further speeded by components L3, R9, D6, and D7.

Diodes D5 and D8 prevent the saturation of T6 by conducting when the collector potential falls under 0.7 V thus diverting the base current via D6. Transistor T6 cannot then be driven any further. Components D9, C5 and R12 form a further protection circuit: during the switch-off process, D9 conducts and current from L2 fleetingly flows through C5. During this time,

the current from the storage capacitor flows through T6 which, again, tends to considerably lower the transistor's safe operating area.

When T6 is cut off, the voltage across L2 rises until the onset of conduction of D4. The relationship between the switch-on and the cut-off conditions is defined by the turns ratio of L1 to L2. This is so chosen that, with L4 and the cascade, the correct operating potentials for the CRT are obtained. This operating condition for the line transformer is only possible when the magnetizing energy during the conduction phase is greater than that during the cut-off (energy to load) phase, as only the charge on C4 is available. The residual energy is taken to C3 which holds the voltage for the next conduction phase. Following the clearance of the magnetizing energy from the line transformer, the voltage suddenly falls and triggers off a new conduction phase.

The circuit comprising T4, T5, C4, R6 to R8 and ZD7 form an oscillation starting circuit. When the voltage across C4 is greater than 9.8 V, the thyristor, formed from T5 and T4, fires and conducts a short current pulse to the base of T6.

The secondary voltage is delivered by means of the transformer secondary windings; small tertiary windings are also provided. The secondary output voltage is sufficiently stable, largely due to the constant nature of the load (mainly class-A stages) and the fixed voltage applied across L1 and L2. The chopper circuit is inherently free from overloading due to the monitoring function of the current during every conduction phase of the switching transistor. The switching frequency is increased as the load increases until oscillation ceases due to insufficient feedback. This feature could be regarded as a life saver in the event of inadvertent contact with the HV-line but the author decided not to try it out.

Only the 30 V output for the power driver stages, after rectification and filtering, is applied to a series-pass transistor and provided with a voltage regulation circuit. The final amplifier inputs are fitted with push-button actuated zener diodes which limit the amplification and so provide a beam-find facility. The outer winding of the line

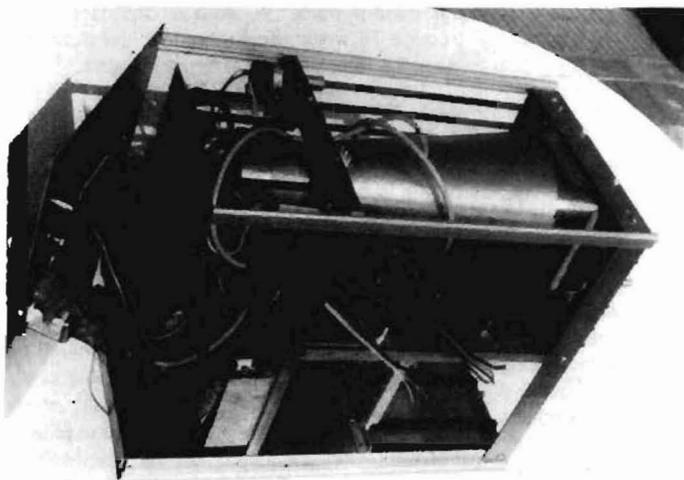


Fig. 10.1.:  
Side view of  
instrument without  
plug-in unit

transformer is occupied by L7 which is the supply to the brilliance amplifier. This must be insulated to at least 2500 V with respect to the transformer core.

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## 10. MECHANICAL CONSTRUCTION

---

The chassis is constructed largely from four sections of metal-plate as may be seen from the photograph in fig. 10.1. The material is semi-hard, 1.5 mm aluminium which is easily bent, drilled and cut. The rear part of the chassis contains the power supply which is normally covered by a U-shaped protection plate. The rear wall has been partially removed for better viewing. The main transformer can be seen in the lower section and above it the HV-cascade.

The leads from the HV and mains components (mains on/off, focus and brilliance controls) are taken via plastic supports which can be seen behind the CRT. The horizontal members of the chassis are made from angle section which are mounted on the chassis and the side walls are slid into them.

On the middle deck, beneath the CRT, is mounted the main PCB containing the circuits for the line drivers, the channel selectors, the trigger selectors, the priority control, the final stages, the trigger- and X-amplifiers, the trigger flip-flop and the counter for the oscillator sweep. Under this deck is located a PCB which contains circuits for the micro controller, the beam selector logic and a few auxiliary circuits, such as the calibration generator etc. On the right of the CRT, a PCB containing a time base is mounted vertically.

In the space under the centre deck, the plug-in unit rails can be seen together with the appertaining plugs and bus leads. Behind them is a space for the Y-delay line. The deck is L-shaped on the front side and supports the operating components. For this reason it has been set back by 10 mm from the front panel. This is also the case for the pre-amplifiers and the control-board elements and provides the means for an convenient termination for the control knobs (from an appearance point of view) on the front panel.

To round off the illustrations, figs. 10.2. and 10.3. show photographs of the main board and components as well as the mechanical arrangements of a pre-amplifier plug-in unit. It can be seen that the track side of the board is uppermost

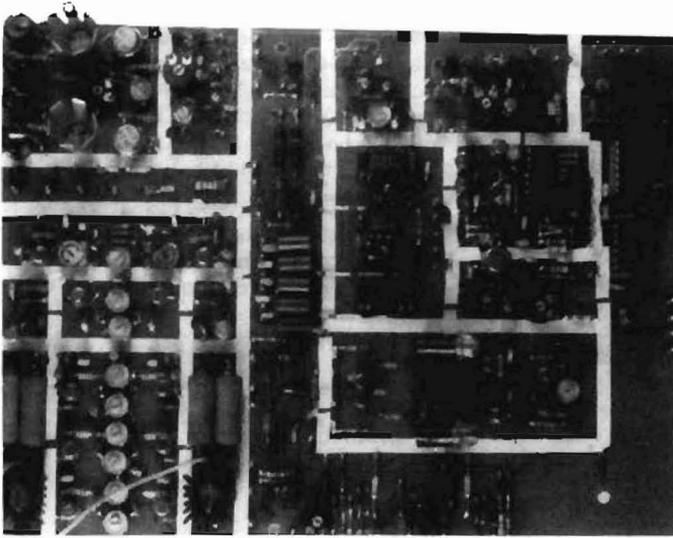


Fig. 10.2.:  
Top view of main  
component board

and the components are soldered directly on to them. This could be very well accomplished with SMD-technology components. The under side of the board is a continuous ground-plane, connections to which must be by drillings. Prominent on the board can be seen white strips (typewriter correction tape). These serve as insulation spacers for screen plates which are normally fitted. The latter is needed not so much for reasons of stability, but for mutual cross-talk affecting low-level signals.

The RF characteristics of this arrangement are perfectly satisfactory. In order that the PCB-tracks are not torn out, only very small connector pins are used which are inserted in a conventional fashion. It could be wondered why this form of construction is not employed more frequently by amateur constructors, as the need to drill the board is minimized and the mechanical stability is adequate for most purposes. It only needs to be provided for, prior to the exposure phase of the PCB's manufacture.

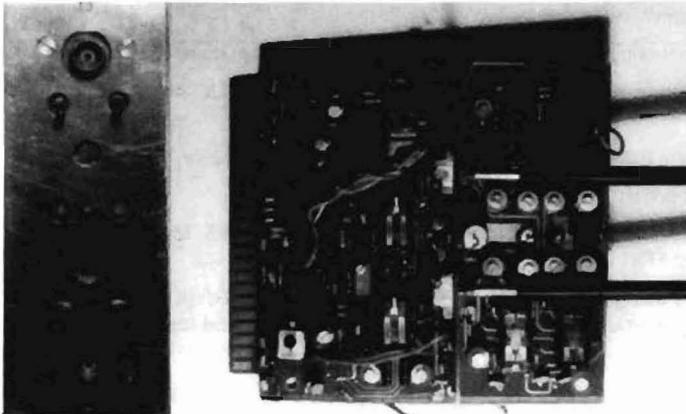


Fig. 10.3.:  
View of a pre-amplifier  
plug-in unit



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## 11. PROSPECTS

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He, who, after following the foregoing description, has an inclination to build this instrument, can obtain all the necessary mechanical drawings, layouts, component plans, setting-up instructions, component specifications and acquisition sources, EPROM-hexdump etc. all with further photographs, from the author, via the publishers, for DM 30. Prospective constructors should practice a little metal work and possess some HF-constructional experience but it is anticipated that readers of this periodical will find no difficulty in these respects.

Owing to the predominantly HF-nature of the circuits, the construction has tended to err on the side of stability. Also, the components have been selected for their general availability as well as for their electronic suitability. Unfortunately this could not apply to the double-FETs

required for the pre-amplifiers as they are definitely not available on the hobby market. The total price of the project depends largely upon the components available but it will not be less than DM 1500, of which DM 800 is reserved for the CRT (with screen) alone. This price, in view of the performance, must be regarded as very reasonable.

Perhaps constructional articles, or suggestions, will appear from the readership upon how the range of plug-in units can be extended to cover a wider variety of measurement? The author will find them very welcome.

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## 12. REFERENCES

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## Microwave Lens Antennas

In order that directivity may be enhanced in the THz range of frequencies, i.e. light, two properties are used most frequently. These are reflection, as from the surface of a mirror, and refraction, as in a refractor telescope lens. The basic differences in the two properties are shown clearly in figure 1. In the microwave range, by far the most common concentration techniques use the properties of reflection, but there is no reason why refraction cannot be used just in the same manner as it is in optics.

### 1. SOME BASIC OPTICS

The phenomenon that is usually associated with the property of refraction is caused by the dispersal of electromagnetic waves through media possessing differing densities and therefore at different speeds. In vacuum, the speed of an EM-wave is  $300 \times 10^8$  m/s and through air it is almost same. In other dielectrics, such as optical glass, the speed of light is very much smaller than through air and vacuum and the same applies to dielectrics such as plastics, ceramics, wax etc. All materials have their own characteristic relative permittivities which directly affects the speed of light passing through them. Table 1 gives a few examples of the relative permittivities  $\epsilon_r$  of a few common materials:

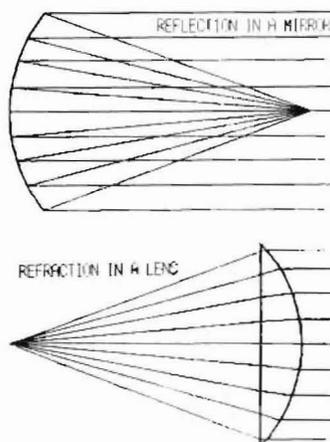


Fig. 1: Concentration through reflection in a mirror and through refraction in a lens

Air	1
Polystyrene foam	1
PTFE (Teflon)	2
Wax	2.2
Glass	2 - 5
Ceramic	4.4
Crystal	4.5
Mica	8

Table 1: Relative permittivity of some materials

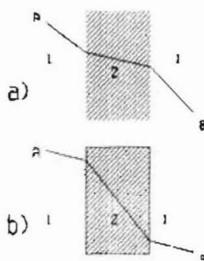


Fig. 2: Every electro magnetic takes the path having the shortest transit time

When a wave passes from point A to point B through two mediums having differing refractive indexes (fig. 2), it will always take the path which gives it the shortest transit time. If then, the propagation time through medium 2 is smaller than that through medium 1 (fig. 2a), the path length through the medium 2 is minimized. This could be the case if one medium 1 were air and the other medium were, say, glass. If, on the other hand, medium (1) were glass and medium (2) were air, as in (fig. 2b), then the EM-wave would be propagated largely through air as it would then be faster.

It is analogous with a situation where one wanted to go from a point A to a point B in the shortest possible time, and that medium 1 is solid ground and medium 2 is water. As one can (normally) walk faster than one can swim, then the route shown in (fig. 2a) would be traversed. If the positions of ground and water were transposed, route 2b would be the natural course to follow.

It could be asked at this stage: why then can't optical lenses be made from wax or ceramic? The answer is, that these two materials are impervious to light, i.e. they have high losses at this wavelength. But what goes for light wavelengths does not necessarily apply to other wavelengths. Both wax and ceramic are excellent for wavelengths corresponding to 10 GHz. Unfortunately, these two materials are not very good to work with and would be very unpracticable as

materials for an amateur lens. A better material is polystyrene foam which is very easy to work with and exhibits very low losses. As "sods law" would have it, however, this material has a relative permittivity ( $\epsilon_r$ ) very close to that of air since it is very largely composed of air. This rules it out for 10 GHz work since a small diameter polystyrene lens would have no influence on the microwaves passing through it. The transit time has not been appreciably altered.

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## 2. METAL-PLATE LENSES

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There is a practical means for radio amateurs to fabricate microwave lenses. This makes use of the "metal-plate lens". This is made from thin metal plates, cut to a predetermined form, and then placed in parallel juxtaposition at a constant distance from each other. The lens shown in (fig. 3) is a possible configuration and is known as the **planar-concave** lens because the virtual outline surface of the combined metal plates is plane on the rear side and concave on the front side as in (fig. 4).

It is nevertheless a **spherical** lens since the front face is (almost) a **spheroid**. Actually, this is an over-simplification as it must be an exact **hyperboloid** in order that it can focus the incoming EM-wave to a single point. The difference between the two forms is very small when the diameter of the lens is large in terms of a wavelength. The lens is easier to make if the surface is spherical and if made large enough, it will focus the EM-wave to a point. That is, parallel rays from an extremely distant point source will be converted into a point source and also the reverse is true, a point source at the focal point will be converted to parallel rays of energy.

As may be further seen in figure 3, every plate has its own individual form and size from that of its neighbour. If all plates were identical, then the result would be a **planar-concave cylindrical** lens (figs. 5 and 6). In this case, the front surface of the lens is a segment of a cylinder and the

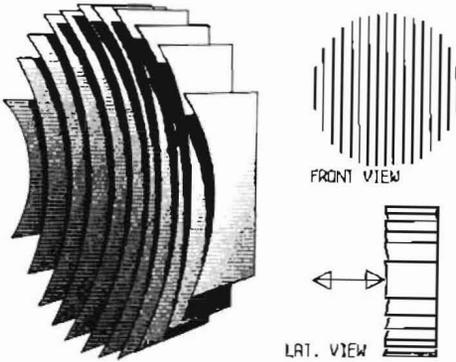


Fig. 3: Three views of a spherical metal-plate lens

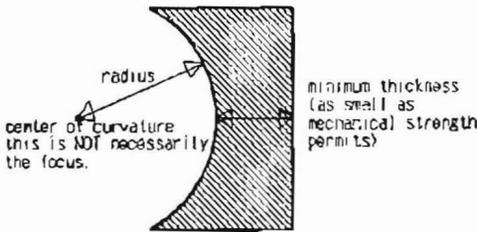


Fig. 4: Form of an elemental metal plate. The focus of radius is not necessarily coincident with lens focus point.

focus is a line parallel to the line that joins all curve centre points.

The lenses shown in figs. 5 and 6 are not equivalent: their insertion loss is dependent upon the polarization of the incident wave - it is at a minimum when the polarization is parallel to the plates.

These metal-plate lenses are known as **acceleration lenses** and represent a basic difference to the classical dielectric lens of the stamp-collector's magnifying glass which delays the incident light waves. When the waves are distributed between the metal elements of a plate lens, they are actually accelerated. Of course, this explanation is necessarily simplified in order to make the comprehension a little easier as it is known, from the theory of relativity, that nothing travels faster than the speed of light.

Following this reasoning, it can be seen that plate lenses have a reversed effect upon waves than that of the dielectric lenses. This means that a concave plate lens has a converging effect and a convex plate lens has a diverging effect. In fig. 7, the lens types are shown together for purposes of contrast.

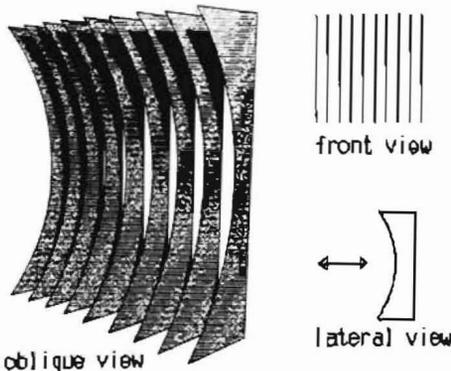


Fig. 5: Three views of a planar-concave, cylindrical metal-plate, vertically-polarized lens.

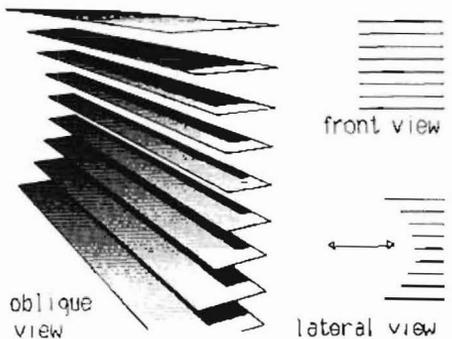


Fig. 6: Three views of a planar-concave, cylindrical metal-plate, horizontally-polarized lens.

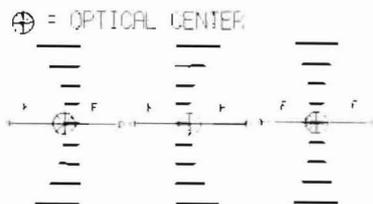
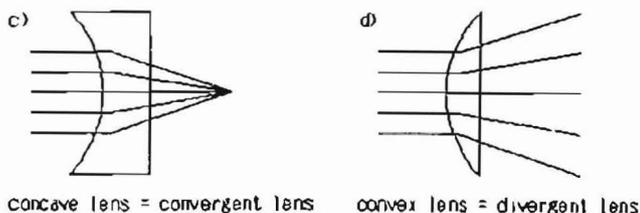
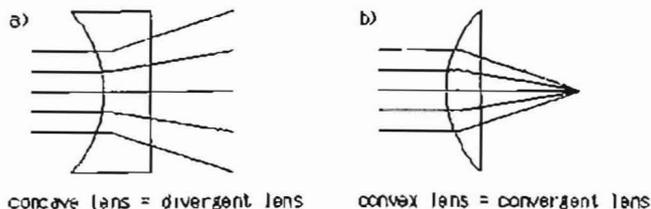


Fig. 7:  
Above: dielectric lenses  
("delay-lens").  
Centre: metal-plate lens  
("acceleration-lens").  
Below: optical centres,  
F = Focus length

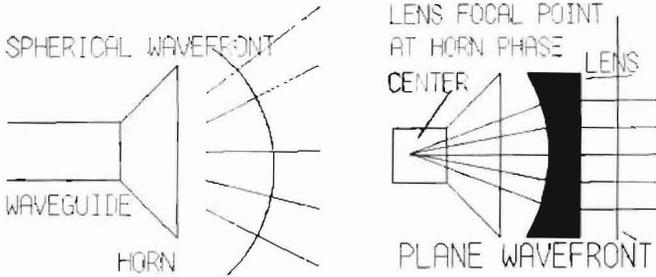
A wave which is distributed from the focus point in a ball-shaped wave, becomes a planar wave when it has encountered a spherical concave metal-plate lens (fig. 7c). That would be the case for transmission of a wave. If, on the other hand, a planar wave is intercepted by this lens, it is transformed into a spherical wave and concentrated at the focal point of the lens. This is the case for the reception of a wave.

It will be noticed that the lens effect is independent upon direction from which the wave arrives – see figure 7e: in both left-hand diagrams the same lens is depicted, one with the waves arriving from the concave side and the other with the waves coming from the convex side. The points at which the waves are concentrated – the focus – is always at the same distance from the optical

centre. The optical centre is an important point because the focal length is measured from here.

It can be seen in fig. 7e that the optical centre lies on the optical axis – namely in the middle of surfaces of the two lenses, assuming the lenses are symmetrical (bi-concave or bi-convex). With an unsymmetrical lens (plane concave or plane convex), however, the optical centre lies on the optical axis near the lens but the exact location must be determined experimentally.

If the focal point is measured from the optical centre and not from the surface of the lens, then it will be found to be equal on both sides of the lens. The three lenses depicted in fig. 7e have the same focal length and can therefore be considered to be equivalent.

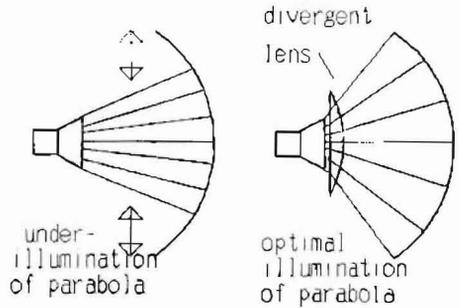


**Fig. 8:** Enhancing the directivity of a small horn by using a lens. The divergent beam from the horn is focussed by a suitably placed lens.

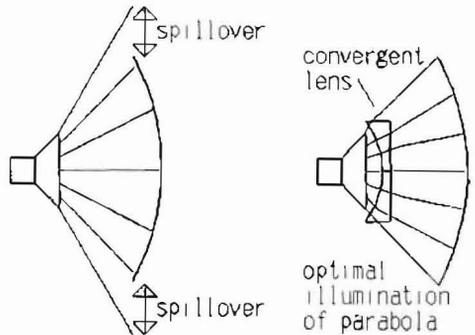
The same occurs, incidently, with the concave paraboloid only the waves do not pass through the lens but are reflected from it.

As possible applications for microwave plate lenses, the following are offered: -

- \* Increase the directivity, and therefore the gain, of a small antenna e.g. a horn, without much of an increase in its overall dimensions (fig. 8).
- \* Optimizing the illumination of any given parabolic reflector and radiator which would otherwise be incompatible with each other (fig. 9). This should be of interest to radio amateurs as they often use surplus feed horns and/or parabolic reflectors. A plate lens is much easier to fabricate than a cassegrain sub-reflector to serve the same purpose.



**Fig. 9 a:** Optimizing the illumination of a parabolic reflector by the use of a horn lens.



**Fig. 9 b:** Optimizing the illumination of a parabolic reflector by converging the radiation by means of the lens in order to minimize stray radiation.

### 3. DIMENSIONING A METAL-PLATE LENS

A lens is characterised by the following dimensions:

- 1) The focal length
- 2) The diameter (aperture)
- 3) The insertion loss

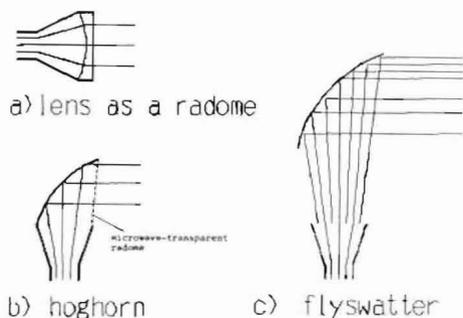


Fig. 10: Three methods of improving the directivity of a horn antenna:  
 a) lens forms a radome  
 b) parabolic horn (hoghorn)  
 c) "flyswatter" antenna

### 3.1. The Insertion Loss

This depends upon three parameters:

- The angle between the wave's polarization in the E-plane and the metal plates. The insertion loss is at a minimum when the E-plane lies parallel to the plates.
- The thickness of the lens
- The materials used in the construction.

The insertion loss is one of the reasons why this type of lens finds little use in commercial practice. In order to increase the directivity and the gain of horn antennas, there are several possibilities which may be considered. The lens could be located in front of the horn (fig. 10a) with a consequent increase in the insertion loss. Alternatively, a hog-horn antenna could be used (fig. 10b). This is a combination of a horn and a parabolic reflector which is often employed for terrestrial radio links. The flyswatter antenna (fig. 10c) is also in common use.

Another important point concerns both the horn and the reflector (planar or parabolic); they are inherently broad-banded whereas the characteristics of lenses are essentially frequency dependent. Since radio amateurs are usually interested in small frequency ranges, this point is of little consequence. In addition, the fabri-

cation of amateur horn-parabolic antennas is somewhat difficult (5) as the parabolic elemental segments must be quite accurate.

### 3.2. The Lens Aperture

This is the same dimension as for the combination of both feed horn and lens, and it is that (or slightly larger) of the horn aperture.

A good method is to combine the lens with the horn as shown in fig. 10a. The focal point must lie on the phase centre of the horn – the latter being approximately in the (virtual) apex of the pyramid. In this case, the spherical wave will be refracted by the lens into a plane wave with the focus point being at an infinite distance – its centre being that of the phase centre of the horn.

In the configuration shown in fig. 11, the lens serves also as a radome – the space between the lens elements being filled by a material having a low relative permittivity  $\epsilon_r$  and low loss, such as polystyrene foam. This keeps the weather from the horn and the wave-guide components – a most useful characteristic. It will be remembered that polystyrene foam does not change the characteristics of the lens.

### 3.3. The Focal Length

By the help of a little mathematics, the focal length can be determined. As with every lens, the focal length of the metal-plate lens depends upon:

- The refractive index
- The curve radius of both front and rear lens surface

The refractive index  $n$  is calculated according to formula (1)

$$n = \sqrt{1 - \left(\frac{\lambda}{2d}\right)^2} \quad (1)$$

where,

$\lambda$  = free-space wavelength  
 $d$  = distance between plates



Fig. 11: A physical combination of horn and lens

It can be seen from the formula, that the refractive index  $n$  for microwave plate lenses (i.e. acceleration lens) are always smaller than unity. Dielectric lenses, on the other hand, always possess refractive indexes which are greater than one.

Further interesting relationships are as follows:

$$n = \sqrt{\frac{\epsilon}{\epsilon_0}} = \sqrt{\epsilon_r} \quad (2)$$

where,

$\epsilon_0$  = Permittivity of a vacuum

=  $8.859 \times 10^{-12}$  Farads per metre

$\epsilon$  = Absolute permittivity of the medium in question

$\epsilon_r$  = Relative permittivity (as in table 1)

Furthermore:

$$n = c/v_0 \quad (3)$$

where,

$c$  = velocity of light in a vacuum ( $300 \times 10^6$  m/s)

$v_0$  = velocity of light in the refractive medium in question

Table 2 gives examples of refractive indexes of metal-plate lenses for three frequencies corresponding to the 3 cm amateur band and five differing spacings  $d$  between two plates.

Frequency	10.0 GHz	10.25 GHz	10.5 GHz
$d = 18$ mm	$n = 0.55$	$n = 0.58$	$n = 0.61$
$d = 19$ mm	$n = 0.61$	$n = 0.64$	$n = 0.66$
$d = 20$ mm	$n = 0.66$	$n = 0.68$	$n = 0.70$
$d = 23$ mm	$n = 0.75$	$n = 0.77$	$n = 0.78$
$d = 25$ mm	$n = 0.80$	$n = 0.81$	$n = 0.82$

Table 2

Now that the refractive index of the lens is known, the focal length can be calculated using formula (4):

$$\frac{1}{f} = (n - 1) \cdot \left( \frac{1}{R_1} + \frac{1}{R_2} \right) \quad (4)$$

where,

$f$  = focal length

$n$  = refractive index

$R_1$  and  $R_2$  = curve radii of the front or rear surfaces of the lens. A convex surface is expressed by  $R > 0$ , a concave surface by  $R < 0$

The fact that the surfaces are described with curved radii means that they are spheroids whereas a perfect lens would have hyperboloid surfaces. According to (1), they could be provided with one spherical and one hyperbolic surface. In any case, the spheroid represents an approximation which is sufficiently accurate where the radius is not too small. Spheroid lenses are easier both to calculate and to fabricate.

Turning again to formula (4): Assuming that one of the lens surfaces is flat,  $R_2$  would represent an infinite radius. Formula (4) may be simplified as follows:

$$\frac{1}{f} = \frac{n - 1}{R_1}$$

therefore

$$f = \frac{R_1}{n - 1}$$

therefore

$$R_1 = f(n - 1) \quad (5)$$

If it is assumed, on the other hand, that both surfaces are identical and having the same radius, as for example, in a bi-concave lens, formula (4) may be simplified as follows:

$$f = \frac{R_1}{2(n - 1)}$$



therefore,

$$R1 = 2f(n - 1) \quad (6)$$

In order to manufacture lenses to predetermined characteristics, it is recommended to assume a plate spacing of between 19 mm and 25 mm for the 3 cm band. This entails refractive indexes of between 0.61 and 0.80. For the other microwave bands, the spacings can be calculated from formula (1). As it may be seen, the refraction of the lens is inversely proportional to the spacing of the plates. For a given focal length, a relatively large lens radius will have to be given in order that its construction is rendered easier. It must always be remembered, however, that the refractive index must be held within the given boundaries.

#### 4. EXAMPLES

In order to increase the gain of any given horn antenna, a matching plate lens is to be constructed. The 3 cm horn antenna has an aperture of 78 mm x 56 mm and a length of 135 mm (fig. 12).

As usual, the horn should be operated in the horizontal plane. For the minimum insertion loss, the plates of the lens are mounted horizon-

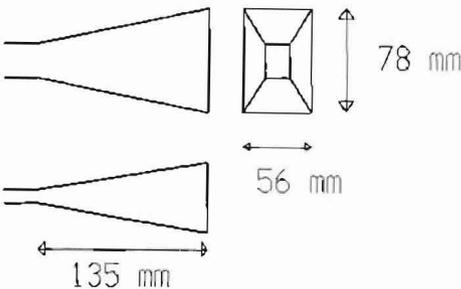


Fig. 12: Horn dimensions for calculation In example

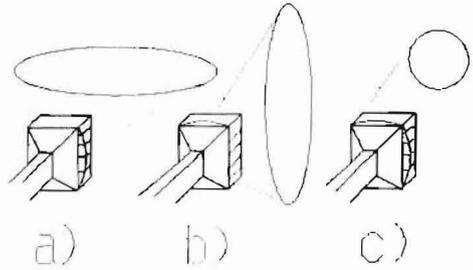


Fig. 13: Three methods of achieving directivity by means of a lens

tally, as shown in fig. 6. The metal plates are rectangular in form for ease of manufacture – easier than those of figs 3 or 5 for example.

It is possible to increase the directivity (gain) in either the horizontal plane or the vertical plane by using cylindrical lenses, as in figs. 13a or 13b. The directivity may be increased in both planes by the use of a spherical lens as in fig. 13c.

The cylindrical lens of fig. 13a is now considered for the first example as this is easier to fabricate than the spherical lens. In the horizontal plane, the lobe is not concentrated and therefore the gain will be lower than with a spherical lens, but still higher than that with the horn alone. In practical transmit operation, this may be advantageous as all the other stations will be on or over the horizon thus making the operational alignment of the antenna less critical. In this arrangement, the valuable microwave energy, which was uselessly radiated into the ground or into the sky, is now concentrated onto the horizon.

The required focal length must now be determined. The phase centre of the horn can be determined in a dimensional drawing: It is approximately 170 mm away from the aperture. Since the lens will be a few centimetres thick, and the focal length is measured from the optical focal point, which lies somewhere inside the lens and on the optical axis, 30 mm must be added to the 170 mm: a lens of 200 mm focal length is required.

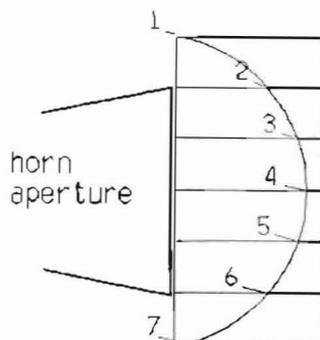


Fig. 14: Lens made with 20 mm thick expanded polystyrene

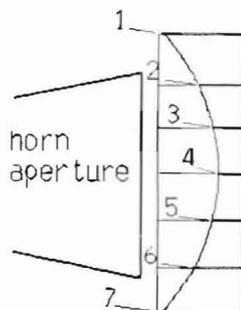


Fig. 15: Lens made with 18 mm thick expanded polystyrene

The lens is made from rectangular plates of aluminium kitchen foil which is about the thinnest metal foil available. The thinner the plates, the less the obstruction they offer to the passage of the microwaves so that the insertion loss is minimized. For mechanical stabilization, the spaces between the foils are filled with polystyrene heat-insulating sheets and glued together. This material is easily obtainable in thicknesses of 20 mm, does not refract microwaves and has little attenuation. The adhesive at 10 GHz, however, can be very lossy and so as little as possible should be used – just enough to keep the assembly in one piece. A glue which does not dissolve polystyrene foam should, of course, be used.

From formula (1), a refractive index of 0.690 can be obtained at 10.368 GHz for this lens.

The radius of the concave surface of the lens is from formula (5), 62 mm.

The plate widths are:

- Nos 1 and 7: 58 mm
- Nos. 2 and 6: 22 mm
- Nos. 3 and 5: 10 mm
- No. 4: 7 mm

The length of the metal plates should be 120 mm or more.

Six polystyrene sheets of dimension 65 mm x 120 mm x 20 mm are now required.

Figure 14 shows the lens. Only the bold horizontal lines of the drawing represent the metal foil plates.

If the curve radius appears to be somewhat small, the 18 mm thick polystyrene sheeting should be tried: the refractive index at 10.368 GHz then becomes 0.595 and the radius 81 mm. The plate widths then become:

- Nos. 1 and 7: 31 mm
- Nos. 2 and 6: 19 mm
- Nos. 3 and 5: 12 mm
- No. 4: 10 mm

The six polystyrene sheets are dimensioned 35 mm x 110 mm x 18 mm. This lens is shown in fig. 15 and with the small plate spacings, the lens refracts more strongly so that the radius is increased and the lens becomes thinner.

What should be done now if the radius still appears to be too small? The plates cannot be arranged to be any tighter because the minimum recommended refractive index of 0.6 has already been reached.

The lens can be made with a larger radius if it is bi-concave in construction. If both surfaces have the same radius, the previously calculated radius from formula (6) must merely be multiplied by two: that results, using 20 mm polystyrene, in 124 mm and the plate width then becomes

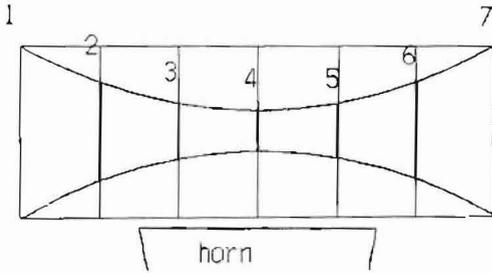


Fig. 16: Bi-concave metal-plate lens:  
Radll = 124 mm. Plate spacing = 20 mm

- Nos. 1 and 7: 40.5 mm
- Nos. 2 and 6: 23.5 mm
- Nos. 3 and 5: 13 mm
- No. 4: 9 mm

The lens is depicted in fig. 16.

If 18 mm polystyrene is used, the radius of both concave surfaces becomes 162 mm.

Should even this radius be too small, a larger focal length will have to be accepted in order that it can be enlarged. For example 400 mm. Using formula (6), for refractive index of 0.690, a radius for both lens surfaces of 248 mm is obtained (20 mm polystyrene sheeting). This lens is shown in fig. 17 where it can be seen that the aperture of the lens has been doubled. This influences all microwaves emanating from the horn (or into it). This lens is rather thick.

If a small focal length together with a thin lens is required, a multi-lens system can be adopted as shown in fig. 18. The total focal length *f* is calculated according to formula (7) from the focal lengths of the individual lenses, *f*<sub>1</sub>, *f*<sub>2</sub>, ... *f*<sub>*n*</sub>:

$$1/f = 1/f_1 + 1/f_2 + 1/f_3 + \dots 1/f_n \quad (7)$$

If it is desired that the radiation is beamed in both planes and the gain is then maximized. A bi-concave spherical lens as shown in fig. 13c can be used. The metal plates must then have a

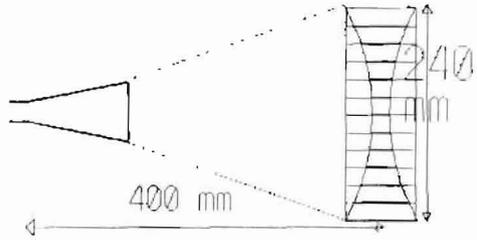


Fig. 17: A 400 mm focal length lens

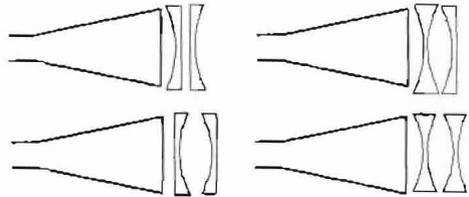


Fig. 18: Various lens combinations

spacing of 20 mm, a focal length of 200 mm and have a form as depicted in fig. 19. This is the bi-concave-spherical version of the bi-concave cylindrical lens as shown in fig. 16.

When commissioning this combination of feed horn and lens, only the distance between the horn aperture and lens needs to be adjusted. The highest gain is achieved when the focal point of the lens is coincident with the phase centre of the horn.

For 24 GHz, 10 mm thick polystyrene sheets can be used as distance spacers between the aluminium plates. In this case, the refractive index would amount to approximately 0.78 (it is frequency dependent!).

After these many theoretical considerations, I have resolved to commence the construction and testing of a metal-plate lens, together with other local amateurs, without delay. The results will be published as soon as they become available. I hope that many readers will find the inspiration to build and experiment with this form of antenna!

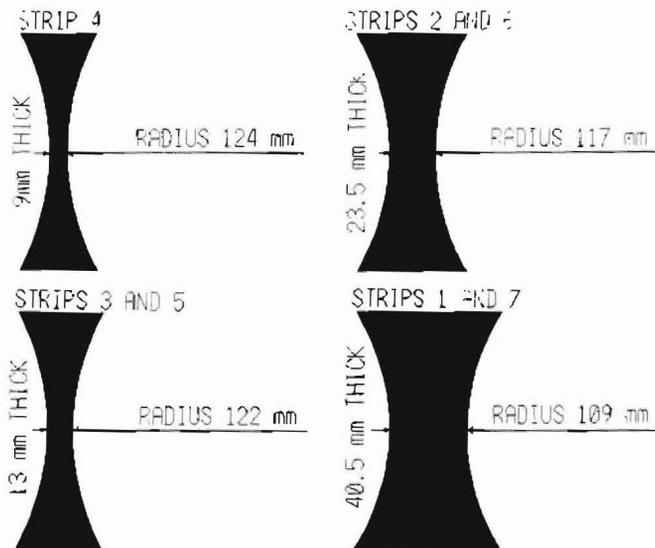


Fig. 19:  
A spherical convergent  
metal-plate lens (scale 2 : 1)

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ISBN 3-9801367-0-1  
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*Andreas Schaumburg, DF 7 ZW and Dr. Jochen Jirmann, DB 1 NV*

## Practical Tips for the Amateur Spectrum Analyzer

This article will set down some hints and tips, for the benefit of prospective constructors, based upon a few practical experiences in the construction of the amateur spectrum analyzer. DF7ZW has successfully completed two of these instruments and has spoken to two other constructors of this project. The material has been collected for the magazine so that it can be presented in a comprehensive article.

First, a brief identification of the publications carrying the relevant articles – they should be studied carefully:

VHF COMMUNICATIONS editions 3 and 4/87 as well as 3/89 and 1/90.

---

### 1. HF/IF MODULE DB 1 NV 006

---

It is easy to forget that pin 5 of the IF-IC TDA 1576 should be taken to ground!

The frequency response of the analyzer is improved if a 3 dB pad (exact value uncritical) is placed between the ring mixer I1 and the pre-selector (see part 3b). This frequency response is gained, however, at the expense of a 3 dB loss in sensitivity but the mixer is better terminated.

The Neosid inductor type 0051-4831 is very suitable for the oscillatory circuit of the 2nd LO (L2) but it must be fitted with a brass slug. On no account should a ferrite one be used.

---

### 2. LO/PLL MODULE DB 1 NV 007

---

Although it was mentioned that the supply voltage for this unit should be highly stable, this in fact, was not provided. It can be rendered more stable in the area where it counts by including a filter unit in the supply line to the VCO. This consists of a RC-network of 27  $\Omega$  resistor and a 220  $\mu$ F capacitor. It will ensure that the noise produced by the 15 V regulator chip is considerably reduced thereby making the VCO noise modulation smaller. This will have a positive effect upon the narrow-band resolution of the analyzer. The modification will affect the 2nd LO on PCB 006.

Before installing the reed relay, check its pin-out – the one DF7ZW installed had to be turned through 180° in order to suit the board connections.

The resistance between the pin "filter in" and transistor T7 is shown with the wrong value on the component layout plan 007. The correct value should be 47  $\Omega$ . DF7ZW used 27  $\Omega$  in order to ensure a positive switching.



The capacitive part of the tuning voltage filter comprising a 10  $\mu$ F and a 10 k $\Omega$  resistor, should be a foil capacitor. Although DB1NV has experienced no problems with high-grade tantalums or electrolytics, DF7ZW has noticed frequency instability caused by the temperature dependent, high-leakage current through these types of capacitor. Using a 1  $\mu$ F foil capacitor will ensure that the PLL stays for hours on the same frequency selection.

The coupling of the frequency divider I2 (SDA 4211) should, in general, be as loose as possible otherwise the divider output frequency will get into the VCO and cause spurs at intervals of a few megahertz. The spectral purity of the VCO should be checked with another spectrum analyzer when setting up and commissioning the instrument.

The bi-stable I6 ( $\frac{1}{2}$  74LS221) in the control loop can be the cause of some non-linearity in the tuning characteristic. In particular, some examples from Fujitsu display this effect. It can be readily seen with a marker generator. Examples from Motorola were found to be the best in this respect 74HC-types seem to be better for the linearity but have the disadvantage of producing more noise making the VCO noise pedestal, in its free-working condition, much higher.

---

### 3. CRYSTAL FILTER MODULE DB 1 NV 008

---

Perhaps this may be considered as an exceptional piece of bad luck, but in the locality of DF7ZF (Frankfurt) there are many high-power broadcast stations

The problem occurs when the filter is switched in, there was a rather suspicious noise at a level of -50 dB rel. full signal display. The cause turned out to be direct radiation from a short-wave broadcast station at about 8 to 10 MHz into the logarithmic voltage detector, I3 (TDA1576). This detected the signal which then appeared as noise. The remedy was found to be the inclusion of 33  $\mu$ H RFCs in all the supply lines to the module

together with 100 nF ceramic, multi-layer, by-pass capacitors.

---

### 4. CONTROL MODULE DB 1 NV 009

---

Both inputs of the op-amp I3 (741) are interchanged on the board. Pin 2 and pin 3 must therefore be crossed over by the use of wire bridges.

---

### 5. GENERAL

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If one is able to ignore the cost element, both in terms of time and money, and successfully completes this project, then a really outstanding test instrument will be obtained. DF7ZW used a Hewlett Packard spectrum analyzer (8554b) plug-in for his work on the project. Naturally, it cannot be claimed that the subject instrument is the equal of the professional equipment but in terms of cost effectiveness and pride of achievement in its construction, the odds begin to even up.

The sensitivity of the authors instrument is -20 dBm for full deflection. The dynamic range, measured with two-tones signal spaced by 20 kHz at a frequency of 5 MHz, was approx. 70 dB. The sensitivity can be improved by using, as a pre-amplifier, an Avantek wideband amplifier module from the MSA series. There are no additional spurious signals produced as a result of adding this Avantek amplifier as would be the case if the gain was improved by increasing the IF amplification: see part 3b. These particular amplifiers are very good and they are very easy to retrofit into the instrument. Its frequency response is rated flat from 5 to 500 MHz but, in practice, goes much higher. When installed in a tin-plate housing, there are no signs of self- or spurious oscillations. Cascading the amplifiers could result, without any problems, in a gain of some 30 dB or more.



## MATERIAL PRICE LIST OF EQUIPMENT

<b>DJ4LB</b>	<b>A Universal Sound-Vision Unit for FM-ATV Transmitters</b>	<b>Art.No.</b>	<b>Ed. 2/90</b>
PC-Board	DJ4LB 010 Europe format (100 x 160 mm)	6115	DM 35.00
<b>DC9DO</b>	<b>SAT-X Receiver for the Satellite IF Band 900 - 1700 MHz</b>	<b>Art.No.</b>	<b>Ed. 1/90</b>
<b>DC9DO 001</b>	PC-Board	6364	DM 38.00
<b>DC9DO 001</b>	Special components: BFQ 69, 3 x MSA 0304, 7805, SL 1452, TL 082, SO42P, 5 x BB505B, BB405B, 5 x 1N4151, ZBV2, Z5V1, LED red; trimmpoti (horiz): 100 Ω, 470 Ω, 47 k, (upright): 2 x 47 k, 4.7 k, foil trimmer 3 x, 4 mm coil former with ferrite core 3 x, CuL wire, silvered wire; RFCs: 33 μH, 22 μH, 15 μH, 3 x 100 μH; tin-plate box	6365	DM 120.00
<b>DF9DA</b>	<b>Compact METEOSAT Converter</b>	<b>Art.No.</b>	<b>Ed. 1/1990</b>
<b>DF9DA 001</b>	kit with all components ready-to-operate module	6510 3029	DM 395.00 DM 575.00
<b>DF9DA 002</b>	<b>Compact Weather-Satellite FM Receiver</b>		<b>Ed. 2/1990</b>
<b>DF9DA 002</b>	kit with all components, with 1 crystal for 137.5 MHz Receive crystal for 134.0 MHz (METEOSAT-ch. 2) Receive crystal for 137.62 MHz (NOAA-9 and 11) Ready-to-operate module (with 3 crystals)	6511 6512 6513 3310	DM 445.00 DM 34.00 DM 34.00 DM 890.00
<b>YT3MV</b>	<b>DSP Computer for Radio Amateur Applications</b>		<b>Ed. 2/1988, 1 + 2/1989</b>
<b>Set of PCBs,</b>	<b>progr. EPROM with authentic documentation</b> Contains: PCBs YT3MV 003 (bus), 004, 005, 006 (4 x), 007, 008 and 009; a programmed EPROM (operating system with Compiler, Editor), a set of copies of all diagrams and component lay-out plans (in A4), the operating-system manual.	6004	DM 599.00
<b>YT3MV 010</b>	<b>Interface for KR-5600 Rotators</b> PCB, progr. EPROM, together with A4 copies of circuit schematics and comp. loc. plans	6003	<b>Ed. 1+2/1989</b> DM 100.00
<b>User software</b>	Several software packages complete with image examples on 3.5" floppy disks		<b>Ed. 3+4/1989 2+3/1990</b>
		6002	DM 145.00





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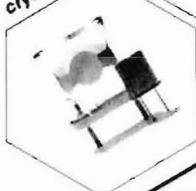


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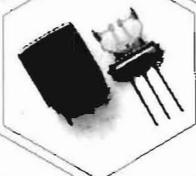
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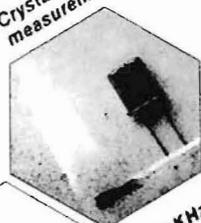
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