SPECIAL ANALOG ISSUE

ELECTRONIC DESIGN

FOR ENGINEERS AND ENGINEERING MANAGERS-WORLDWIDE

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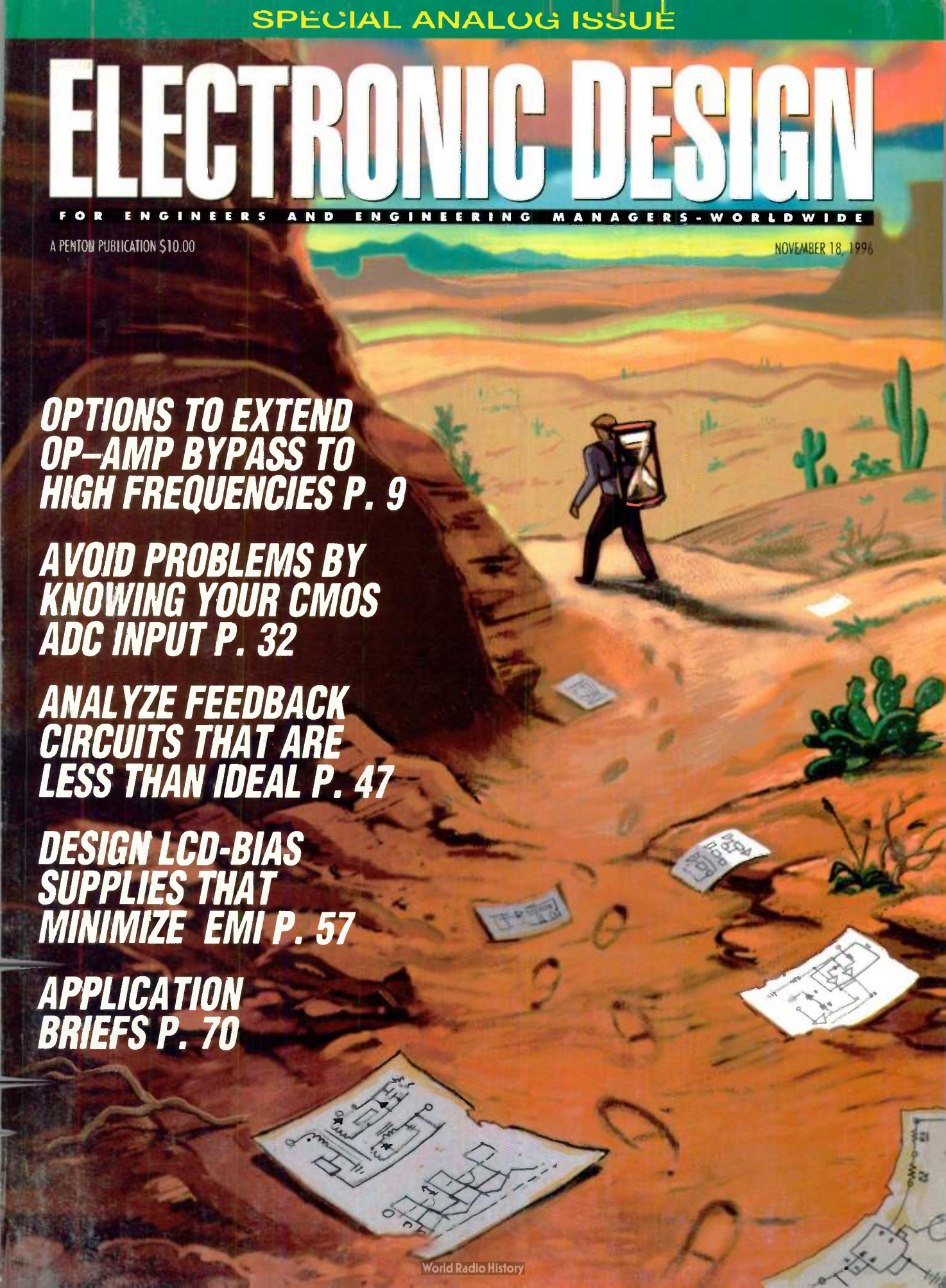
NOVEMBER 18, 1996



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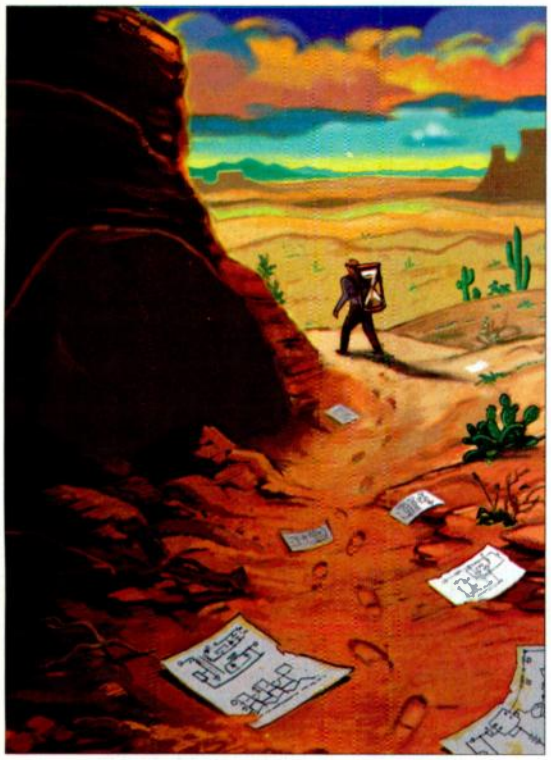

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JMS-1MH	+13	2-500	DC-500	5.75	60	45	9.45
JMS-1H	+17	2-500	DC-500	5.90	50	50	11.45
JMS-2L	+3	800-1000	DC-200	7.0	24	20	7.45
JMS-2	+7	20-1000	DC-1000	7.0	50	47	7.45
JMS-2LH	+10	20-1000	DC-1000	6.5	48	35	9.45
JMS-2MH	+13	20-1000	DC-1000	7.0	50	47	10.45
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Read My Lips, They're Analog

I'm a meter man. No, not the guy that pops across your lawn once a month and looks into your electricity consumption; and no, not someone who measures everything metrically rather than with a yard stick—although I do mentally think and measure in *meters*. I mean, I am the sort of person who likes to see the needle move across a scale, calibrated to the best accuracy. I still miss putting together and tuning up high-power transmitters; squeezing the last milliwatt into the feeder, getting those dips exactly where they should be. There is considerable adrenaline generated when you "turn up the wick" on a frequency-agile, 100-kW, short-wave transmitter and it does all you wanted it to do, with no arcs or sparks.

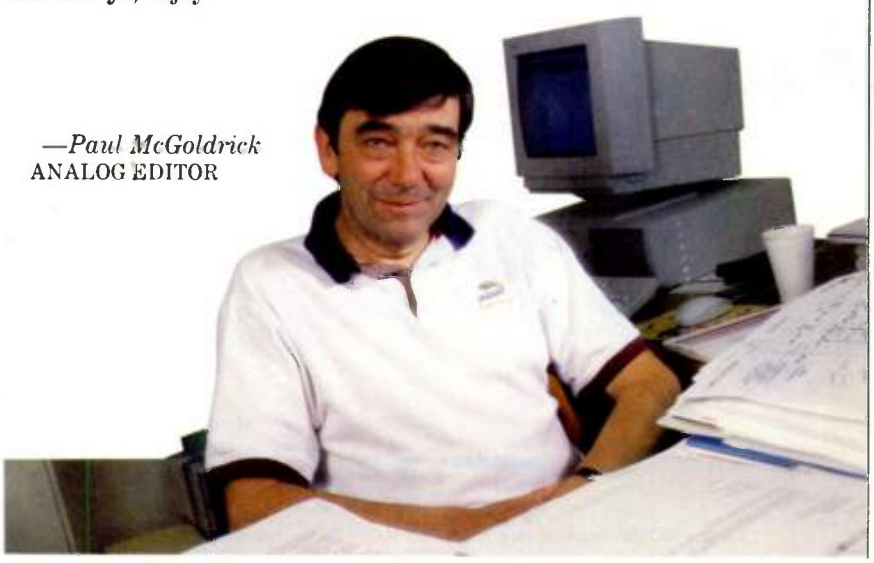
The same is true of the majority of the population when it comes to the instrumentation in front of you in a vehicle, where the manufacturers have found considerable resistance to digital displays. In the heydays of the TWX machine, I was actually able to read the punched paper tape quite quickly, but I don't know anyone able to read ASCII in the raw. Do you? So, for your convenience, this special analog supplement has been inputted by analog, processed in 8-bit ASCII, and delivered to you in a nice, neat analog printout. Boy, are we biased or what!

In this, our private world just for the analog cognoscenti, we can again delight in some of the ways we are needed. A piece from John Wettroth at Maxim looks at supplying the power needs of LCDs, while Jerry Graeme and Bonnie Baker of Burr-Brown consider the problems of adequately bypassing high frequency op amps. Jerome Johnston of Crystal takes a hard look at how to drive CMOS ADCs, and Brooktree's Agustin Ochoa demystifies feedback design. There are some familiar names in the special briefs, and we also have some new and welcome additions. The piece from Audio Precision, for example, on fooling an ADC, is something we all wish we had thought of; Dallas Semiconductor's use of a digital potentiometer leads to other thoughts about where it might be employed; TelCom's fan-speed control is delightfully simple, and cheap. And, of course, there is always more to be told about ADCs, op amps, sensors and those weird power supply needs that only you thought you had to deal with.

There also is a new departure in looking at an analog simulation model. Sure, it's not really an application, but we are heading for better and better models in the analog world as vendors realize that analog engineers have needs as well. Our end of things is more difficult to simulate than digital, but the process of catching up has begun, and we all need to be a little more aware of the whys and hows.

As always, enjoy.

—Paul McGoldrick
ANALOG EDITOR



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NF (dB)	8.6*	8.0
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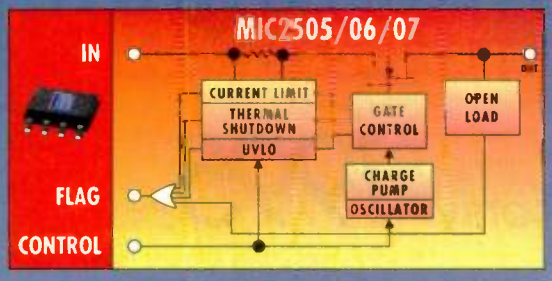

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Fast Op Amps Demand More Than A Single-Capacitor Bypass

Several Options Extend Op-Amp Supply Bypass To High Frequencies.

JERALD GRAEME
Graeme Consulting

BONNIE BAKER
Burr-Brown Corp.

Today's high-frequency op amps demand more than the simple, single-capacitor bypass that serves general-purpose op amps so effectively.[1] Inductive effects become far more serious at high frequencies, requiring greater attention to frequency stability and supply-noise coupling. Consequently, the parasitic inductance of the large-value, single-bypass capacitor defeats the bypass purpose at higher frequencies, requiring the addition of a smaller, secondary capacitor. More severe cases also may require resistive detuning of the bypass impedance, or the addition of series line impedance to form a decoupling filter. But for each of these cases, there are simple design equations to help guide component selection.

The need for power-supply bypass arises from parasitic supply-line impedances that degrade noise performance and stability. Line impedance reacts with currents drawn by the amplifier and other circuitry powered from the same supply lines, producing parasitic supply-line signals. These signals represent noise at the amplifier supply connections that couples through the amplifier's finite power-supply rejection ratio (PSRR) to create noise at the op-amp inputs. The portion of the supply noise resulting from the amplifier itself constitutes a parasitic feedback signal capable of producing oscillation.

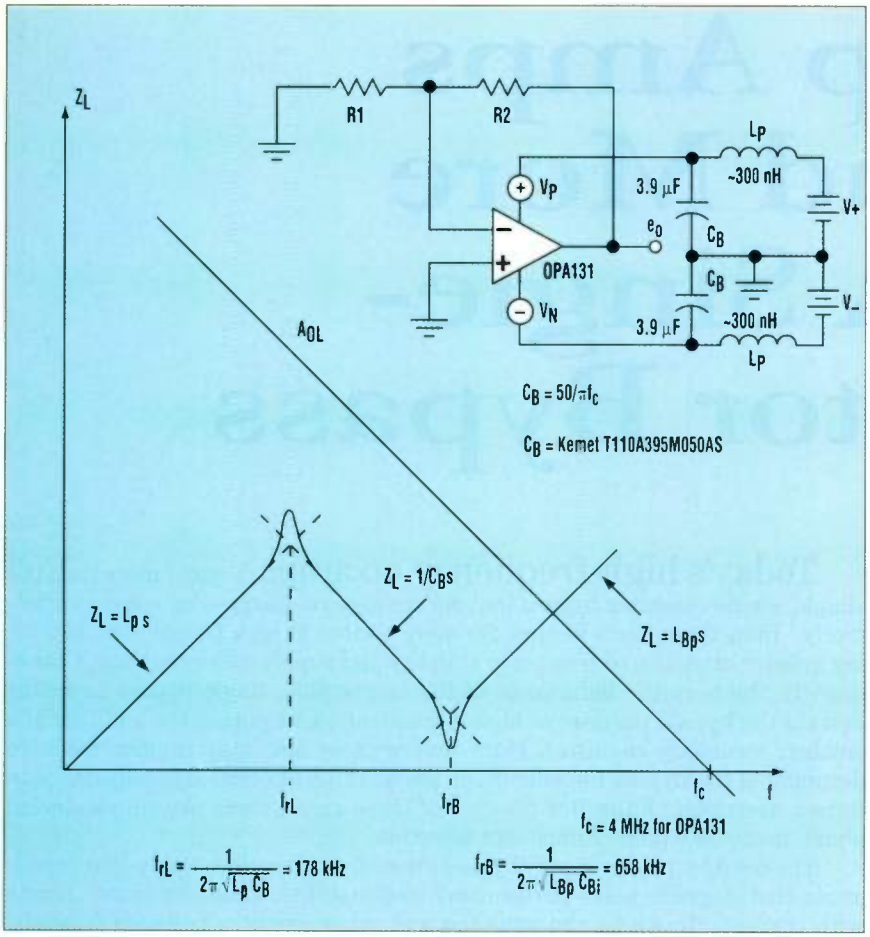
Analysis of the bypass impedance gives insight into the multiple effects of supply bypass that produce noise-coupling and stability problems. This analysis reveals inductive effects and multiple impedance resonances that compromise the capacitance shunting desired of bypass. An evaluation of these bypass deficiencies yields simple design equations that optimize bypass selection. A previously published article explored the nature of power-supply noise coupling and the multiple effects of a single bypass capacitor.[2] This article now extends the bypass process with dual bypass capacitors and supply decoupling that overcome the limitations of the single-capacitor solution.

Single Bypass

Single bypass capacitors serve the general-purpose op amp, given careful selection and placement *(Fig. 1)*. Figure 1 shows the basic bypass case with a circuit model and a response plot of the supply-line impedance, Z_L. The amplifier's open-loop gain is superimposed over this response to provide a relative frequency comparison. For this basic case, single capacitors can bypass the parasitic L_p inductances of the two power-supply lines. To be effective, the capacitors must be placed right at the amplifier supply pins where they essentially bypass all of the line inductance. That inductance dominates the line impedance at lower frequencies, producing the rising $Z_L = L_p s$ region in Figure 1's response plot.

At slightly higher frequencies, the bypass capacitance reverses the slope of this response, but only temporarily. At first, the bypass transfers the impedance response from $Z_L = L_p s$ to $Z_L = 1/C_B s$ while capacitive shunting overrides the effect of the L_p inductance. Later, the Z_L response returns to a

OP-AMP BYPASS DESIGN



1 Power-supply bypass initially rolls off a rising Z_L line impedance, but the parasitic inductance of the capacitors later returns Z_L to a rising response.

rising curve when the capacitor's own parasitic inductance overrides its capacitive shunting. The latter transfers the impedance response to $Z_L = L_{Bp}s$, where L_{Bp} is the inductance of the C_B capacitors. Response resonances at f_{rL} and f_{rB} mark the transition points separating the three Z_L regions. The first resonance results from the reaction of the L_p line inductance with the C_B capacitance, and occurs at:

$$f_{rL} = \frac{1}{2\pi\sqrt{L_p C_B}}$$

The second resonance results from the reaction of C_B's ideal capacitance, C_{Bi}, with L_{Bp}. This defines f_{rB} as:

$$f_{rB} = \frac{1}{2\pi\sqrt{L_{Bp} C_{Bi}}}$$

Careful selection of the C_B capacitors positions these transition points to optimize the overall impedance response. The capacitors must control the Z_L impedance over the entire amplifier response range, but especially in the two upper Z_L regions. There, a declining amplifier PSRR increases the circuit's susceptibility to supply-line coupling. A designer's first intuition may suggest making the bypass capacitors large to minimize the net line impedance. As expected, increasing C_B moves the f_{rL} point to the left, reducing the line impedance in the $Z_L = 1/C_B s$ region. On the other hand, increasing C_B also adds to the capacitor's parasitic inductance, L_{Bp}, and moves f_{rB} to the left as well. The latter move increases the line impedance in the $Z_L = L_{Bp}s$ region, degrading the bypass in that region.

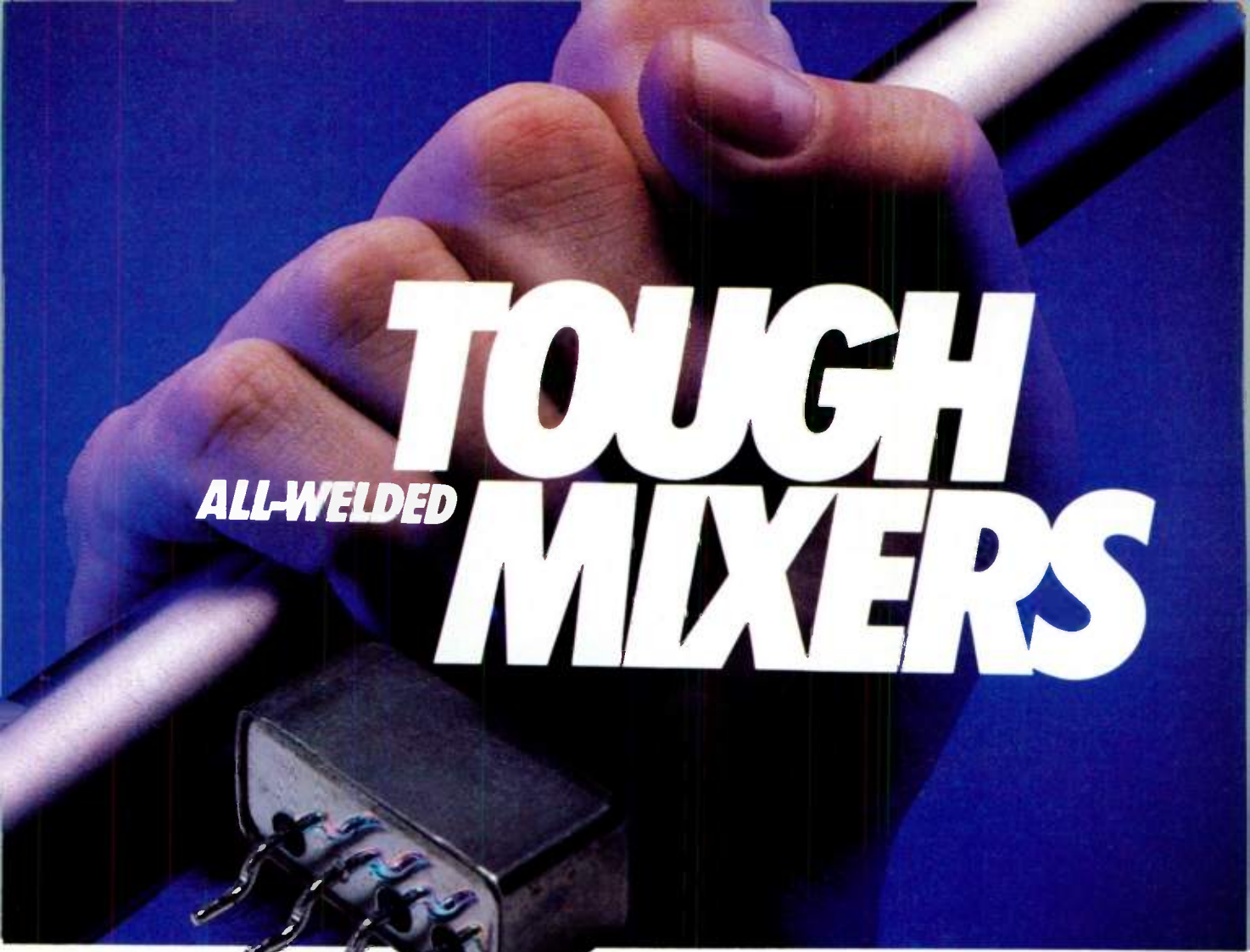
A compromise is to select C_B for $Z_L = 1/C_B s = 1\ \Omega$ at $f = f_c/100$, optimizing the bypass for general-purpose amplifiers.[3] The f_c parameter is the unity-gain crossover frequency of the op amp. This selection produces the design equation $C_B = 50/\pi f_c$, and ensures frequency stability in the $Z_L = 1/C_B s$ region for all amplifiers.

For general-purpose amplifiers, this capacitor choice also ensures stability in the later $Z_L = L_{Bp}s$ region because of practical amplifier and capacitor conditions. These amplifiers roll-off the open-loop gain (A_{OL}) response at a moderate frequency, reducing sensitivity to the $Z_L = L_{Bp}s$ rise. Practical capacitors that also are selected with the $C_B = 50/\pi f_c$ design equation have low enough inductance to limit the Z_L rise within this A_{OL} range.

Dual Bypass

Today's higher-frequency op amps expand the meaningful range of the $Z_L = L_{Bp}s$ impedance rise, which jeopardizes stability and increases supply-noise coupling. Their greater amplifier bandwidths encompass more of the high-frequency end of this rise, and require secondary bypass to counter the inductance of the primary bypass. A smaller capacitor added in parallel with the first commonly bypasses this new inductance limit. But simply adding the secondary bypass does not automatically resolve the line-impedance issue. The secondary capacitor has inductance of its own, producing another bypass compromise at a somewhat higher frequency. Further, the secondary capacitor reacts with the inductance of the first, producing a resonant increase in the supply-line impedance. Careful selection of the second capacitor produces a compromise solution that retains low bypass impedance throughout most of the amplifier's frequency range. Analysis of the net bypass impedance produces two simple design equations that guide capacitor selection.

Adding a secondary bypass capacitor in parallel with the first restores a low bypass impedance for the full response range of most high-frequency amplifiers. This produces a net $C_B = C_{B1} + C_{B2}$. Setting $C_{B2} << C_{B1}$ generally ensures that the C_{B2} self-resonance occurs outside the amplifier's response range. Both the lower capacitance value of C_{B2} and the accompanying lower parasitic inductance produce this higher resonant frequency. For even higher-frequency applications, a third capacitor also may be required. But whether using two or three capaci-



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TUF-3	7	0.15-400	4.98	0.34	46	5.95
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TUF-3MH	13		5.0	0.33	46	8.95
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TUF-1	7	2-600	5.82	0.19	42	3.95
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TUF-1MH	13		6.3	0.12	50	6.95
TUF-1H	17		5.9	0.18	50	8.95
TUF-2	7	50-1000	5.73	0.30	47	4.95
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TUF-2MH	13		6.0	0.25	47	7.95
TUF-2H	17		6.2	0.22	47	9.95
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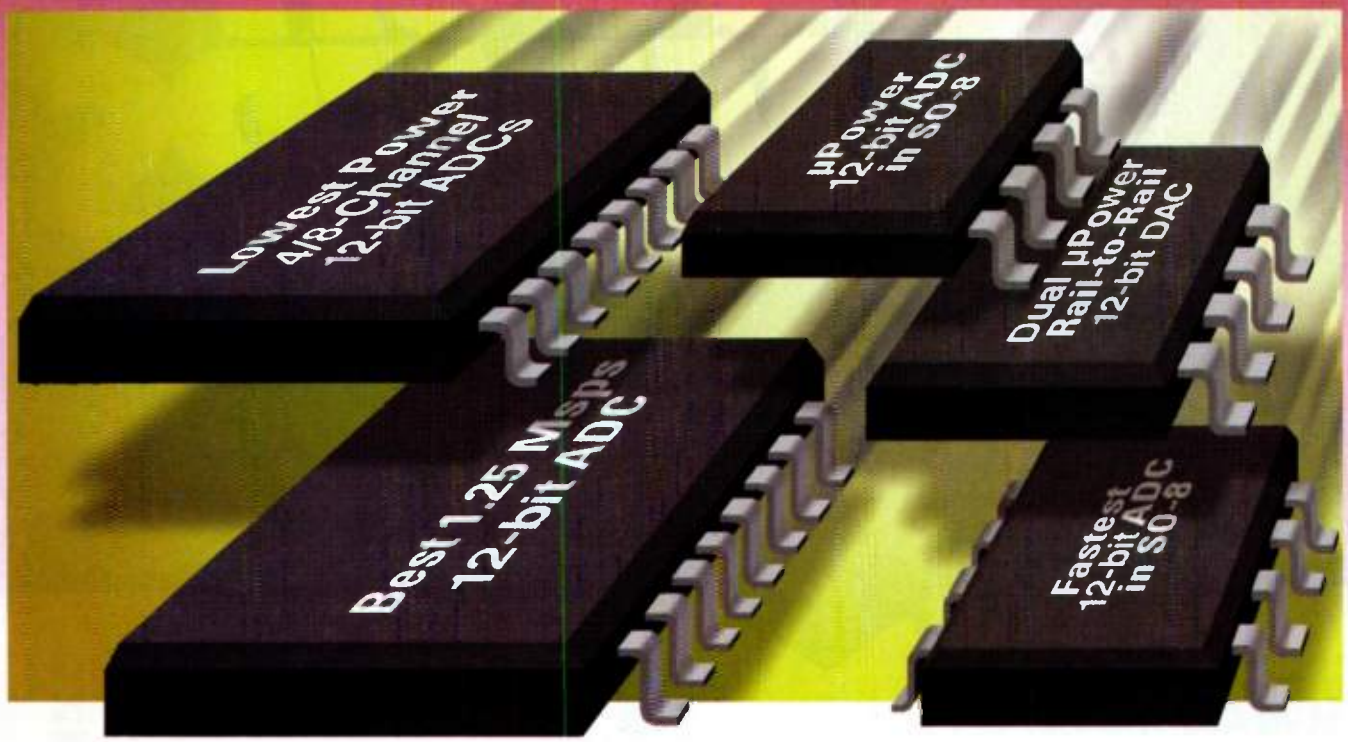

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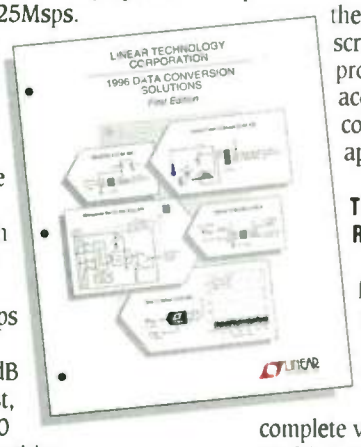

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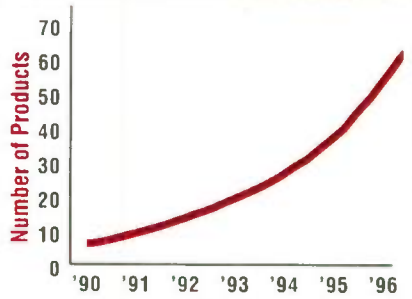

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tors, examination of the dual-bypass case uncovers the impedance characteristics that guide the bypass selection process.

Adding secondary bypass capacitors restores the declining frequency response of the Z_{CB} bypass impedance, but with new complications. This solution introduces two additional resonances—one from the self-resonance of the secondary capacitor and the other from the reaction of the secondary capacitance with the inductance of the first capacitor *(Fig. 2)*.

Figure 2 illustrates the first new resonance with a circuit model and its corresponding impedance responses. This simplified circuit model shows only those elements pertinent to the dual-bypass discussion. The positive supply bypass serves to illustrate the concepts, but designers must be aware that an identical bypass would be connected to the negative supply line. The model also neglects the L_p line inductance and power supply. Only the capacitors affect the Z_L response in the upper frequency range, where dual-bypass considerations occur. This is the range above f_{rL} in Figure 1. Consequently, the Figure 2 circuit model represents the supply line with the ideal capacitances and their associated parasitics.

Two curves in Figure 2 display the resulting capacitor impedances: Z_{CB1} and Z_{CB2}. At lower frequencies, a declining Z_{CB1} provides the lower impedance bypass shunt. However, Z_{CB1} later resonates and begins to rise at f_{rB1}. At higher frequencies, Z_{CB2} bypasses this rise and initially restores a declining bypass impedance. Later, the self-resonance of C_{B2} at f_{rB2} again produces a rise, but this time at a lower impedance level than provided by the Z_{CB1} curve. While the resonances remain inevitable, their careful placement optimizes the overall bypass effect. To aid in this placement, a third curve of the graph shows the amplifier's open-loop gain response, A_{OL}. A comparison of the graph's three responses guides the secondary-capacitor selection in a manner that ensures frequency stability for the amplifier.

Bypass Values

Selection of the primary C_{B1} capacitor indirectly defines the C_{B2} capacitance value through impedance interaction. The fundamental bypass requirement defines C_{B1} (as was previously described for the single-bypass case: $C_{B1} = 50/\pi f_c$). This selection reduces the line impedance to 1 Ω at a frequency well within the amplifier's response range. The addition of C_{B2} then bypasses the higher-frequency impedance rise produced by the L_{Bp1} inductance of C_{B1}. Selecting C_{B2} to limit this rise to the same 1 Ω guideline defines this secondary capacitor's value.

In Figure 2, the net bypass impedance of the C_{B1}-C_{B2} parallel combination peaks at f_{iB}, the intercept of the rising Z_{CB1} curve and the falling Z_{CB2}. For higher-frequency amplifiers, this peak would typically occur within the amplifier's response range. Selecting a value for C_{B2} that limits this peak to 1 Ω continues to ensure stability, as described before for the C_{B1} selection.

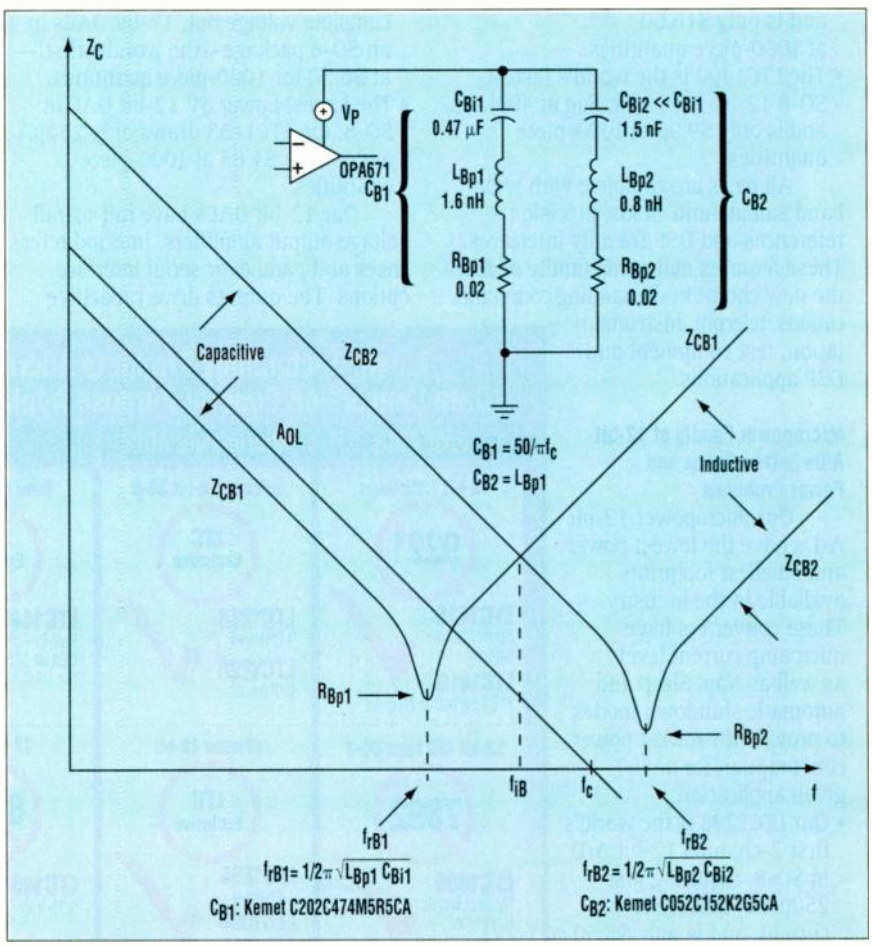
At their f_{iB} intercept, the two Z_{CB} curves occupy the same point on the graph, making $Z_{CB2} = Z_{CB1}$. There, inductance controls $Z_{CB1} = 2\pi f_{iB} L_{Bp1}$ and capacitance controls $Z_{CB2} = 1/2\pi f_{iB} C_{Bi2}$. Equating the two impedance expressions defines the intercept frequency as:

$$f_{iB} = \frac{1}{2\pi\sqrt{L_{Bp1} C_{Bi2}}}$$

As a result, the parasitic inductance of C_{B1} and the ideal capacitance of C_{B2} combine to define the frequency of the bypass impedance peak.

Translating this f_{iB} expression into a C_{B2} design equation requires one further step. At f_{iB}, the Z_{CB2} curve follows its capacitive roll-off as expressed by $Z_{CB2} = 1/2\pi f C_{B2}$. Setting $Z_{CB2} = 1\ \Omega$ and $f = f_{iB}$ produces $f_{iB} = 1/2\pi C_{B2}$. Equating this result with the previous f_{iB} expression yields the C_{B2} design equation:

$$C_{B2} = L_{Bp1}$$



2 Adding a second, smaller bypass capacitor rolls off the inductive impedance rise caused by the first capacitor.

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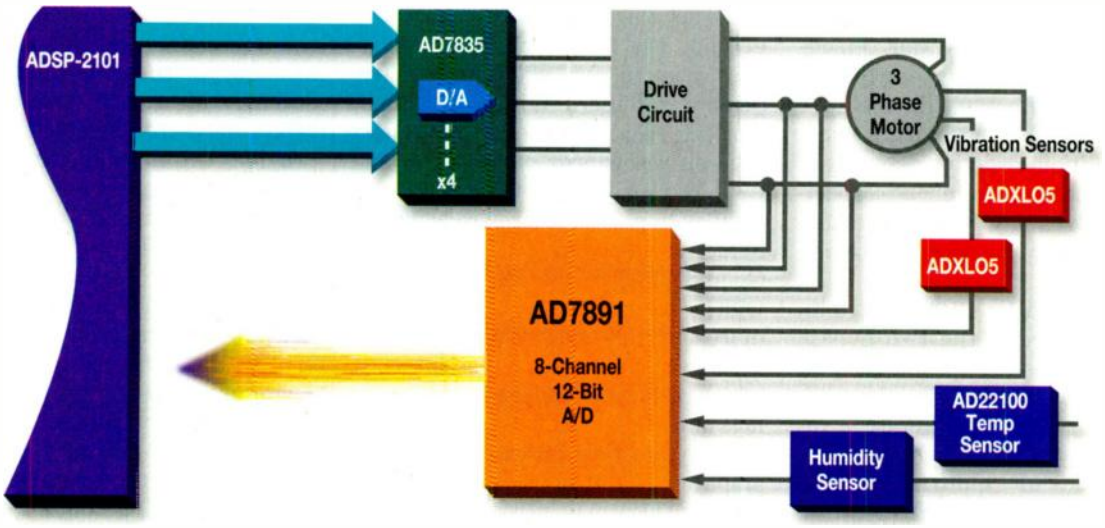

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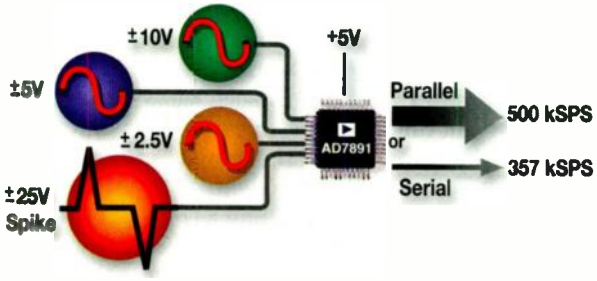

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Therefore, simply making the magnitude of the C_{B2} capacitance equal to that of C_{B1}'s parasitic inductance transfers line-impedance control from Z_{CB1} to Z_{CB2} at 1 Ω. In actuality, a resonance that will be described later raises the peak impedance above 1 Ω at f_{iB}, but temporarily ignoring this effect yields the best starting point for the bypass selection. In addition, resistive detuning of this resonance or an alternate capacitor type solves any related problem without altering the aforementioned design equation.

For the 35-MHz OPA671 op amp shown in Figure 2, the two bypass design equations first produce $C_{B1} = 50/\pi f_c = 0.455$ µF. Selecting the 0.47-µF capacitor shown in Figure 2 results in $L_{Bp1} = 1.59$ nH. Then, selecting $C_{B2} = 1.5$ nF approximates the ideal $C_{B2} = L_{Bp1} = 1.59$ nF with the closest available capacitance value.

The C_{B2} design equation requires knowing the value of L_{Bp1}. Impedance measurement provides the most reliable determination of this inductance because capacitor data sheets rarely specify this parasitic. Some data sheets specify this inductance through an impedance-versus-frequency curve. There, the higher-frequency, rising portion of the curve yields parasitic inductance through the simple calculation $L_p = Z_C/2\pi f$.

Unfortunately, even these curves can fail to communicate the actual inductance condition of practical applications. For packaged capacitors, the curve includes the parasitic inductance of package leads that are usually removed upon installation. Chip capacitors avoid this lead effect, but their response curves still don't include the effect of the circuit-board traces that connect the capacitor. Fortunately, today's impedance analyzers accurately measure the frequency response of a given capacitor and its approximated connection length. Using such measurements, the rising portion of the impedance curve will then accurately define the actual inductance through the $L_p = Z_C/2\pi f$ relationship.

Bypass Alternatives

The preceding discussion outlines the bypass selection that adequately serves most applications. However, there are special conditions that may require additional attention to supply-line coupling. For these conditions, a third bypass capacitor, filtering, or resistive detuning further reduce the coupling effects.

The third-capacitor alternative extends the frequency range of bypass control for even higher frequency amplifiers. With these amplifiers, the A_{OL} response can encompass the self-resonances of both C_{B1} and C_{B2}. Then, adding a third and even smaller bypass capacitor rolls off the inductive impedance of C_{B2}, just as C_{B2} did for C_{B1}. Amplifiers with bandwidths exceeding 30 MHz may require this third capacitor.

A second alternative is filtering, which removes supply-coupled signals outside the useful PSRR (power-supply rejection ratio) range of the amplifier. More specifically, co-resident circuitry may introduce high-frequency supply-line signals that couple through the amplifier with little PSRR attenuation. Beyond the PSRR's unity-gain crossover, such signals typically couple straight through the amplifier to its output. Fortunately, this PSRR crossover typically resides near the amplifier's A_{OL} crossover, presenting a filtering opportunity. The A_{OL} crossover marks the endpoint of the amplifier's useful frequency range. Thus, low-pass filtering, applied after the amplifier, can often remove the effect of high-frequency PSRR coupling without restricting the useful bandwidth of the application. However, intermodulation effects can circumvent the filtering, as will be described later in this article.

Adding Resistance

Resistive detuning of the bypass impedance offers a third alternative for the reduction of supply-coupling effects. The dual-bypass configuration potentially produces a critical resonance that degrades stability at surprising frequencies. This may occur at a frequency above or below the amplifier's response crossover at f_c. Below f_c, the previously selected C_{B2} restores a line impedance below the 1-Ω guideline level, presumably preserving stable operation. However, the C_{B2} resonance reacting with L_{Bp1} can raise the net line impedance well above this level, producing oscillation.

The resonance occasionally produces oscillation at frequencies above f_c. In such cases, diminished amplifier gain limits the parasitic feedback loop, and would seem to prevent instability. However, the resonant impedance rise can counteract this limit. When necessary, resistive degeneration detunes this new resonance. Appropriate capacitor selection generally provides this detuning through parasitic resistance.

Interaction between the two capacitors of the dual-bypass configuration develops this critical resonance. The secondary capacitance reacts with the inductance of the primary in another LC tank configuration *(Fig. 3)*. Figure 3 illustrates this effect with the bold Z_{CB} response curve, which represents the net impedance of the parallel-connected bypass capacitors. Notice that Z_{CB} follows the Z_{CB1} curve of C_{B1} at lower frequencies, and later follows the Z_{CB2} curve of C_{B2}. The transition between the two occurs at their f_{iB} intercept, where the bypass combination produces a resonance of its own. This resonance increases the Z_{CB} magnitude, and produces a 180° transition in the phase of Z_{CB}. The magnitudes and phases of the amplifier's PSRR and A_{OL} responses combine with these Z_{CB} characteristics to produce a complex parasitic feedback condition.

Some combinations of application conditions make the magnitude and/or phase of this resonance degrade stability. In such cases, attention to the more conventional stability determinant, the amplifier's 1/β intercept, fails to identify the problem. Similarly, adding a third bypass capacitor produces no improvement. The third capacitor only reduces the line impedance at frequencies above this interaction resonance. In these instances, bypass degeneration moderates the PSRR error signal by reducing both the magnitude and phase shift of the supply-line impedance. Careful selection of the degeneration resistance improves stability without increasing the supply-line impedance in the critical higher frequency ranges.

Graphical evaluation of this f_{iB} resonance reveals its underlying causes, and displays the cure provided by the resistive degeneration. The resonance results from the reaction of

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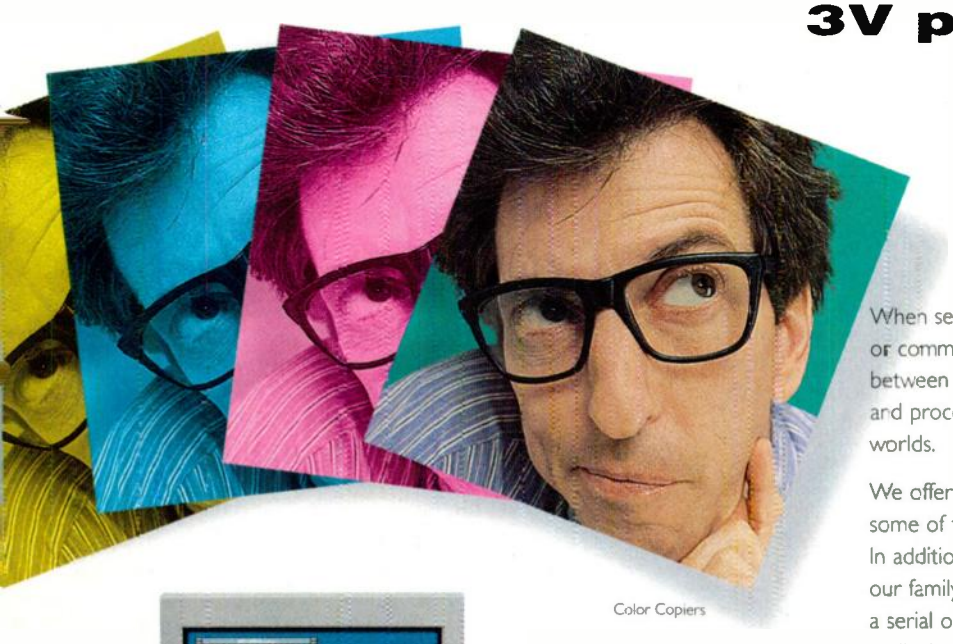

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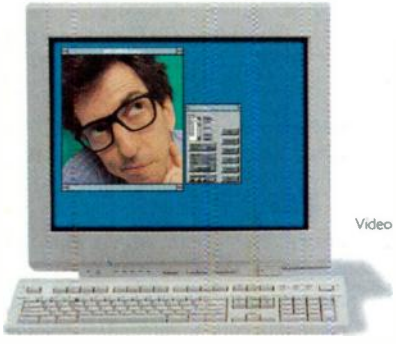

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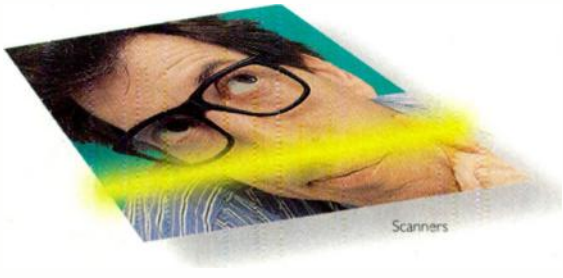

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C_{B1}'s parasitic inductance with C_{B2}'s capacitance. At the f_{iB} shown in Figure 3, Z_{CB1} follows a rising impedance response that's controlled by L_{Bp1}, and Z_{CB2} follows a declining response controlled by C_{Bi2}. At the crossing of the two responses, resonance results due to the equal magnitudes and opposite phases of the Z_{CB1} and Z_{CB2} impedances.

The crossing or intercept of the two curves marks the point of equal impedance magnitudes (because both curves occupy the same point in the graph). At that point, neither impedance dominates the parallel combination, in contrast to the impedance conditions at points other than f_{iB}. The magnitudes of Z_{CB1} and Z_{CB2} contribute equally to the combined Z_{CB} impedance, also making the phase shifts of the two equally significant.

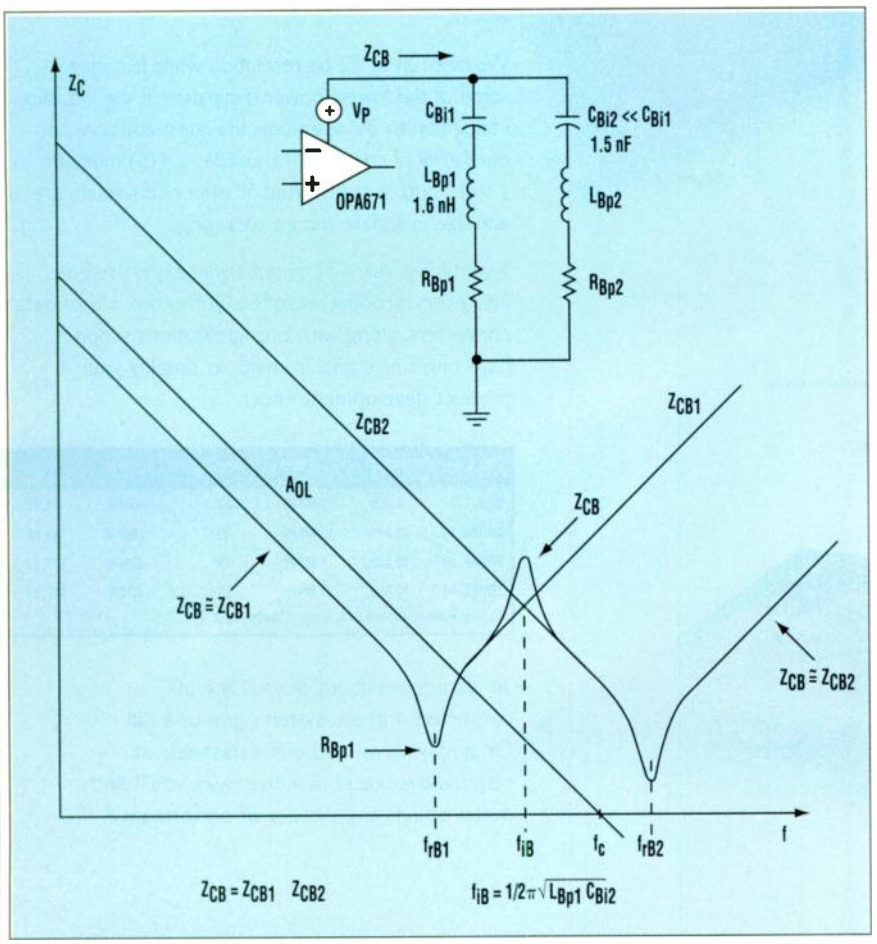
The single-zero rise of the Z_{CB1} curve corresponds to a 90° phase lead, and the single-pole decline of Z_{CB2} corresponds to a 90° phase lag. The 180° phase difference and equal impedance magnitudes inherently produces a resonance.

Adding a small resistance in series with C_{B1} detunes this resonance to ensure stability *(Fig. 4)*. In practice, just choosing a different capacitor type for C_{B1} often serves the same purpose through the capacitor's parasitic resistance. This added resistance does increase the Z_{CB} magnitude in a lower frequency range, but it also decreases Z_{CB} in the higher, more critical frequency range of f_{iB}. Figure 4 illustrates the optimal bypass configuration with degeneration resistance R_{D1} added in series with the other impedance elements of C_{B1}.

As in Figure 3, the bold Z_{CB} curve begins by following Z_{CB1} and ends by following Z_{CB2}. But unlike Figure 3, the Z_{CB} curve in Figure 4 now makes a gradual, rather than resonant, transition between Z_{CB1} and Z_{CB2} at their f_{iB} intercept. The addition of R_{D1} actually detunes two resonances—first the self-resonance of C_{B1}, and then the interactive resonance of C_{B1} and C_{B2}. Comparing Figure 4 with Figure 3 reveals the overall effect of this resistance. Previously, the self-resonance of C_{B1}, at f_{rB1} in Figure 3, produced a resonant impedance drop to the level of parasitic resistance R_{Bp1}.

In Figure 4, the addition of R_{D1} removes this drop and raises this level to (R_{D1} + R_{Bp1}). This actually raises the bypass impedance in the region that previously was the f_{rB1} resonance. However, the amplifier generally retains a high PSRR in this frequency range for sufficient attenuation of supply-line effects.

Further, the Z_{CB} curve now makes a smooth, rather than resonant, transition to this new limit level. The reduced Z_{CB} response slope indicates a greatly reduced phase transition at the frequency of the previous f_{rB1} resonance. This reduces the potential phase combinations with amplifier gain and PSRR effects that could degrade stability. Accepting this temporary Z_{CB} increase allows R_{D1} to detune the more critical resonance at f_{iB}. The Z_{CB} curve no longer displays a resonant peak, indicating a greatly reduced Z_{CB} magnitude and phase transition at f_{iB}.



3 Dual bypass capacitors introduce a new resonance at their f_{iB} intercept, where C_{Bi2} reacts with L_{Bp1} to increase the net Z_{CB} impedance.

Impedance Analysis

Detuning resistance R_{D1} should be large enough to prevent the resonant impedance rise at f_{iB}, but not so large as to unnecessarily raise the Z_{CB} impedance at lower frequencies. Graphical analysis of Figure 4 helps reveal this optimum condition and define an R_{D1} design equation. The curves identify this optimum condition through the magnitudes and slopes of the impedance responses.

Detuning the Figure 3 resonance at f_{iB} requires reducing the slope difference, or rate-of-closure, of the Z_{CB1} and Z_{CB2} curves at their f_{iB} intercept. This rate-of-closure criteria follows from op-amp stability analysis where the slopes of intersecting response curves reflect phase differences and the potential for circuit oscillation.[4] In this impedance analysis, the slopes of the Z_{CB1} and Z_{CB2} curves similarly reflect phase differences and the potential for resonance. Adding R_{D1} decreases this slope difference at the f_{iB} intercept of Figure 4, detuning the resonance. The added resistor pro-

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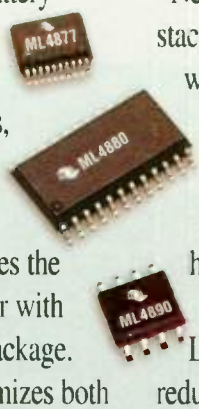

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High Voltage PFC Controller Saves Power

MC33368. A high voltage GreenLine™ active Power Factor Correction (PFC) controller functioning as a boost preconverter in off-line power supply, lamp ballast and battery charger applications. Integration of the high voltage startup function typically saves 0.7 W of power compared to resistor bootstrapped circuits. The MC33368 limits EMI to agency requirements, can be turned on/off and has control/protection features including under-voltage lockout, output overvoltage sensing allowing no-load operation, cycle-by-cycle current limiting, and a programmable output switching frequency clamp.

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Octal Serial Switch has SPI Input/Output

MC33298. This eight output low side power switch interfaces directly to a microcontroller, with control and fault reporting through an 8-bit Serial Peripheral Interface (SPI) port. Used to control various inductive and incandescent loads in automotive or industrial applications as well as control systems for robotics, each switch has a 3.0 A peak current output. Using SMARTMOS technology, the MC33298 has very low standby current, cascadable fault reporting, an internal 65 V clamp on each output, independent shutdown of the outputs, and output-specific diagnostics.

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ICs Manage Power for GaAs MESFETs

MC33169. A support IC for GaAs Power Amplifier Enhanced FETs used in portable phones such as GSM, PCN and DECT. The device provides negative voltages for full depletion of MESFETs as well as a drain switch priority management circuit to protect the power amplifier.

MC33128. A power management controller for battery powered pagers and cellular phones. It has a low dropout voltage regulator with power-up reset for MPU power, two low dropout regulators to power analog and digital circuitry independently, and a negative charge pump regulator for full depletion of GaAs MESFETs.

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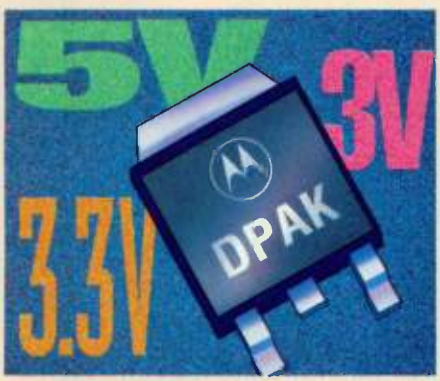

Low Dropout Regulators Power Portables

Our family of LP2950/2951 micropower low dropout voltage regulators has grown. We've added 3.0 and 3.3 V fixed and adjustable voltage versions to our previous 5.0 V offerings. In addition, all three fixed voltage versions of the LP2950 series are now *uniquely* offered by Motorola in the DPAK surface mount power package. The low input-to-output differential voltage of 380 mV at a 100 mA load current, with a low bias current of 75 µA, makes these devices ideal for battery operated and portable electronics such as cellular and portable phones, two-way radios, laptop computers, PDAs and camcorders.

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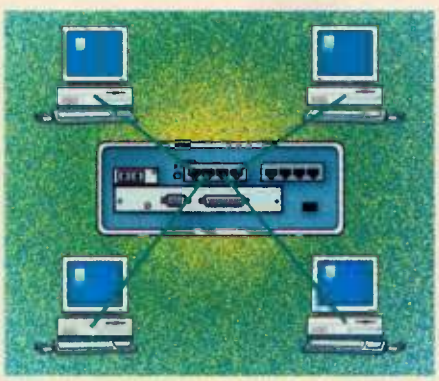

EEST Enables Two-Chip Ethernet Solutions

MC68160. Enhanced Ethernet Serial Transceiver (EEST) combines a serial interface adapter with an Ethernet transceiver. The EEST gluelessly interfaces to any one of Motorola's family of Integrated Communications Controllers, including the MC68EN302, MC68EN360 or MPC860EN, to provide a simplified two-chip solution for a completely functional Ethernet interface. The two chips offer the perfect internetworking solution for smart Ethernet hubs, branch offices and multi-protocol routers, remote access routers and industrial control networking.

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Hard Disk PRML Read Channel IC Achieves 200 Mbps Data Rate

The MC34250 is a fully integrated Partial Response Maximum Likelihood (PRML) 5 V hard disk drive read/write channel IC for high end mass storage applications. Using our advanced mixed mode 0.5 micron BiCMOS process technology, this analog implementation achieves 50 to 200 Mbps data transfer rates with only 800 mW of power dissipation in a single 10mm by 10mm 64-pin thin quad flat pack (TQFP). The IC is designed for zoned-recording applications requiring high linear densities and spindle speeds of up to 10,000 rpms.

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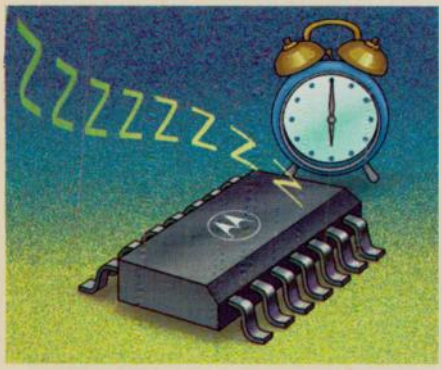
Product Review



1.8 V Rail-to-Rail™ Sleep-Mode™ Op Amp

The MC33304 quad op amp not only operates with a single 1.8 V supply, but can operate in a low standby power "sleepmode" state with a drain current of only 110 µA per amplifier. When an input signal causes an amplifier to source or sink at least 200 µA, it automatically switches to the "awakemode" state, allowing it to source or sink 70 mA to the load. The amplifier will automatically revert to the sleepmode when I_{out} drops below the threshold, and still operates as a micro-power amplifier. The MC33304 can swing within 100 mV of the input and output rails.

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Narrowband FM IF Receiver Eliminates Coil

MC13150. This narrowband FM IF subsystem IC has a coilless demodulator that eliminates the need for a conventional tunable quadrature coil, while providing better noise, linearity and AM rejection than traditional circuitry. The device allows many adjustments with non-precision external resistors and capacitors. Targeted at cellular and other narrowband applications such as PCMCIA wireless modems, the MC13150 provides a high level audio output of up to 2 V with a 3 V supply at a very low drain current of less than 2 mA, and an outstanding 0dBm input IP3.

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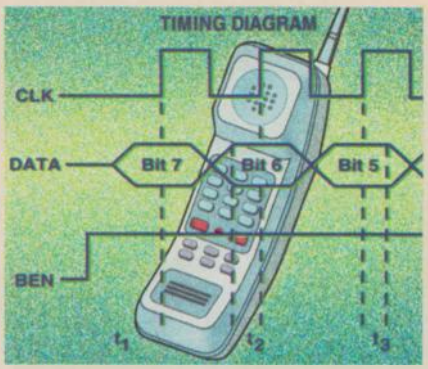

Programmable Line Interface IC for Cordless Phones and Digital Systems

The MC34016 is an ideal interface between an analog phone line and a codec in digital systems. Useful in digital cordless phones or modems, the IC provides improved noise and distortion figures. The adjustment of transmission parameters to conform to a variety of international standards is done with two 8-bit registers, accessible via a SPI bus and with external components. The device has double sidetone architecture and supports passive or active AC set impedance applications.

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PIP IC Provides TV Feature at Low Cost

The MC44461 Picture-In-Picture (PIP) controller IC provides a single-chip, low cost solution to a very complex, value-added TV feature. Designed with our 0.8 µm BiCMOS process, the device contains all the analog signal processing, control logic and memory necessary for the overlay of a small picture from a second non-synchronized source onto the main picture of a TV. The MC44461 is NTSC compatible with all control and setup functions for the IC accomplished via a standard two-pin IIC bus interface. The IC implements switchable main and PIP video signals and two PIP sizes.

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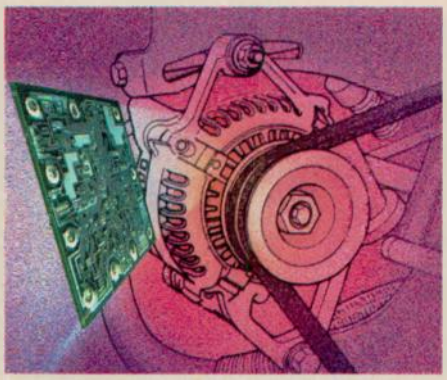

Alternator IC Works in Harsh Environment

MCCF33095/MC33095. Flip-Chip/Surface Mount regulator control ICs are designed for use in automotive 12 V alternator charging systems, and need only a few external components for full system implementation to control the field current of a variety of alternators. Both ICs have internal detection and protection features to help withstand harsh physical and electrical automotive environments. Flip-Chip technology allows the MCCF33095 to operate at higher ambient temperatures than the SOIC version, and both withstand vibration and thermal shock with high reliability.

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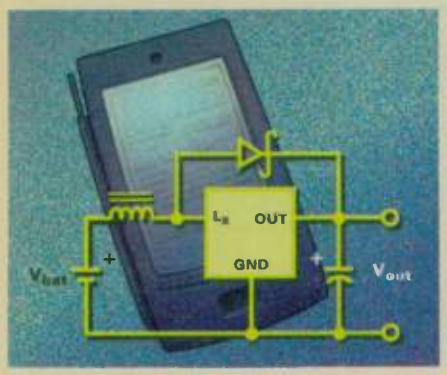

Micropower CMOS DC-DC Converters Simplify Design of Portable Products

The MC33463/33466 series of micropower switching voltage regulators are available in 3.0, 3.3 and 5.0 V options, and are ideally suited for battery powered computer, consumer and industrial equipment. Both families are available in three-pin SOT-89 packages, with either an on-chip switch transistor or provisions for an external switch. The MC33463 devices are Variable Frequency Modulation controllers with a quiescent bias current of 4 µA, while the MC33466 devices are Fixed Frequency PWM switchers with a quiescent current of 15 µA.

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Three Families of CMOS Micropower Linear Regulators have Ultra-Low I_Q

MC78LCxx/78FCxx/78BCxx. Three series of micropower linear voltage regulators are designed for use in cameras, camcorders, VCRs, and hand-held communication products, and include voltage options of 3.0, 3.3, 4.0 or 5.0 V. The MC78LCxx series has an 80 mA output current, a dropout voltage of 0.7 V at 40 mA, and is available in SOT-23 or SOT-89 packages. The MC78FCxx family has an output current of 120 mA, dropout of 0.2 V, in a SOT-89. The MC78BCxx series is available in a SOT-23 and is designed for use with an external power transistor for higher output currents.

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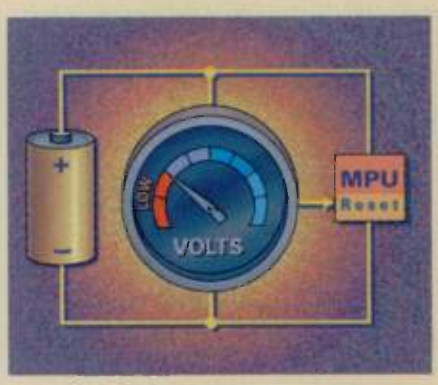

CMOS Micropower Undervoltage Sensing Circuits Monitor MPU/Logic Supplies

The MC33464/33465 families of micropower undervoltage sensing ICs are designed for direct monitoring of MPU/logic power supplies in portable, appliance, automotive and industrial equipment. Both series are available with threshold voltages of 0.9, 2.0, 2.7, 3.0 and 4.5 V with a choice of open drain or complementary CMOS reset output configurations. The MC33464 family has a low quiescent current of 0.8 µA and is available in SOT-23 or SOT-89 packages. The MC33465 series adds a programmable time delayed output, has a quiescent current of 1.0 µA, and is packaged in a SOT-23.

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High Voltage Switching Regulators Simplify Design of Off-Line Supplies

MC33362/33363. These ICs are designed to operate from a rectified AC line source for off-line power supplies, or from a high voltage source for DC-DC converter applications. The MC33362 is designed for rectified 120 Vac line operation and features an on-chip 500 V, 2.0 amp SenseFET™ power switch. The MC33363 is designed for 240 Vac rectified line operation with a 700 V, 1.0 amp SenseFET. Both devices are available in 16-lead through-hole and surface mount packages with pins eliminated to achieve high voltage spacing requirements.

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Battery Fast Charge Controller Simplifies NiCd and NiMH Charging

The MC33340 is specifically designed for fast charging of Nickel Cadmium (NiCd) and Nickel Metal Hydride (NiMH) batteries using negative slope voltage detection. Accurate charge termination is ensured by an output that momentarily interrupts the charge current for precise voltage sampling. The IC also supports secondary charging methods of either programmable time or temperature limits. Protective features include battery over and undervoltage detection, latched over temperature detection, and power supply input undervoltage lockout. A rapid test mode enhances end product testing.

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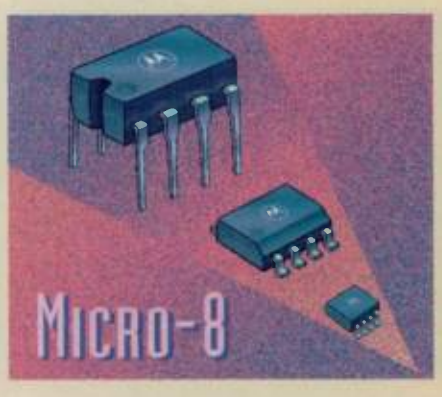

Subminiature Package Trims Board Space

We offer a variety of products in the new Micro-8 subminiature surface mount package. This package uses 50% of the board area of a traditional SO-8 surface mount package, and is narrower than TSSOP miniature packages. The LP2951 adjustable micropower low dropout voltage regulators, and MC33264 low dropout micropower regulators with on/off control are available in the Micro-8 package. The MC34064/34164 undervoltage sensing/micropower undervoltage sensing circuits, and the TL431,A,B programmable precision references are also available in this space-saving package.

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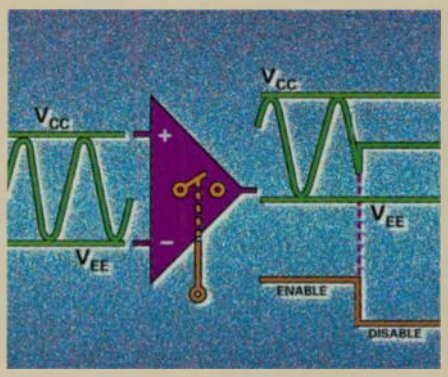
Product Review



Dual/Quad 1.8 V Rail-to-Rail Op Amps have Enable Feature to Extend Battery Life

MC33206/33207. These dual/quad op amps not only have input *and* output rail-to-rail capability, but also an enable mode that can be controlled externally. Typical drain current is ≤1.0 µA per amplifier in the standby mode, saving power and extending battery life. Each op amp in the MC33206 has its own enable pin, and the op amps in the MC33207 are enabled in two pairs. These amplifiers can operate with supplies as low as 1.8 V and ground, yet can still operate with a single supply voltage as high as +12 V.

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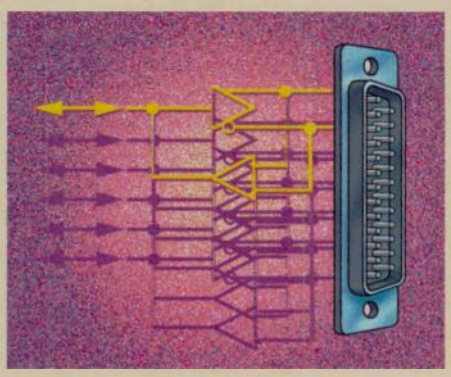

Hex Transceiver Meets SCSI-3 Fast-20 Specs

The new MC34059 contains six differential driver and receiver pairs in a 48-pin QFP for transmission of differential signals at 20 MBPS, meeting the requirements for SCSI-3 Fast-20 transmission systems. Control lines can enable/disable each driver and receiver as required, and an over-temperature sensing circuit will shut down any driver that gets too hot due to ambient temperature or a prolonged short circuit. The low quiescent current of 18 mA saves power in hard disk drive, backplane communications, and computer-to-computer data transmission applications.

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Low Cost FM Communications Receivers

MC13135/13136. These low cost, single chip, dual conversion FM receivers can be used as stand-alone VHF receivers or as the lower IF of a triple conversion system, with a low 2.0 V supply. The MC13135 is designed for use with an LC quadrature detector, while the MC13136 can be used with either a ceramic discriminator or an LC quad coil. Applications include cordless phones, radio controlled toys, baby monitors, walkie-talkies and scanners.

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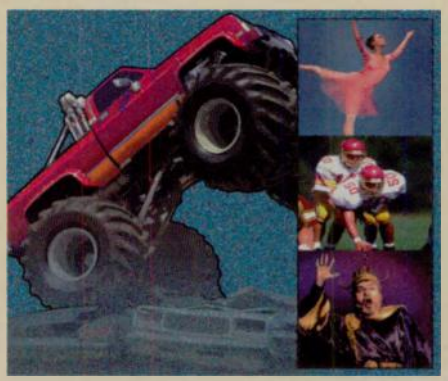

New PIP IC Enables TV Feature Versatility

The MC44463 Picture-In-Picture (PIP) controller IC provides a wide variety of feature options that are all *software programmable,* requiring no printed circuit board changes. When combined with external memory, the device controls a replay mode of up to eight seconds that can be played back at four different speeds. The IC provides options of a single PIP, in either active or replay mode; and three or four PIPs, with one active and the remaining PIPs in a freeze-frame mode. In the multi-PIP mode, the user can choose which of the three or four PIPs is active.

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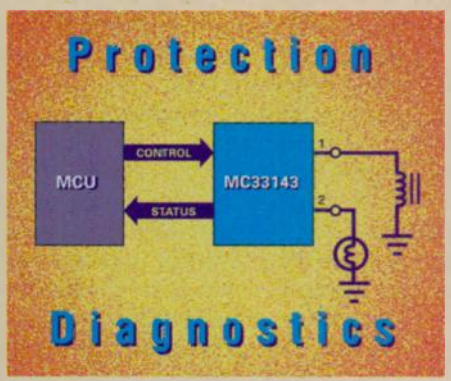

Dual High Side Switch has Protection and Diagnostic Features

The MC33143 dual high side switch is designed for solenoid control in harsh automotive applications, but can also be used to control incandescent lamps, relays, and small motors. This SMARTMOS™ IC has an on-chip charge pump to enhance switch performance, and an externally controlled Sleep-Mode™ for power savings. Each output has individual overcurrent and over temperature shutdown with automatic retry. The device detects and shuts down globally with any overvoltage condition. It also detects and indicates an open load or output short to the supply.

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duces the level, zero-slope portion of the Z_{CB1} response that reflects zero phase shift. At the f_{iB} intercept, Z_{CB2} still follows its single-pole roll-off, reflecting a 90° phase lag for a net 90° phase difference at the intercept. This greatly reduces the phase difference from the 180° required for resonance, and would absolutely remove the resonant reaction of Z_{CB1} and Z_{CB2}.

On the other hand, bypass optimization produces a compromise favoring a somewhat greater phase difference at f_{iB}. The (R_{D1} + R_{Bp1}) resistance, which produces the level region of the Z_{CB1} response, eventually loses control and returns the response curve to a single-zero rise. In the Figure 4 example, the L_{Bp1} impedance overrides that of R_{D1} just at the f_{iB} intercept. Phase shift accompanies the rise. Intuition may first suggest increasing the R_{D1} resistance to move the Z_{CB1} rise and its phase shift well beyond the f_{iB} intercept. On the other hand, such a choice would unnecessarily increase the impedance magnitude of Z_{CB}'s new level region at (R_{D1} + R_{Bp1}). And a continued increase of R_{D1} would eventually increase, rather than decrease, the impedance at f_{iB}. In compromise, setting the (R_{D1} + R_{Bp1}) level at the intercept magnitude still detunes the resonance while also restraining the impedance increase of the level region.

As illustrated in Figure 4, this optimum level places the zero of the Z_{CB1} rise at the f_{iB} intercept. Then, Z_{CB1} introduces 45°, rather than the ideal 0°, of phase shift at the intercept. This increases the net phase difference with Z_{CB2} from 90° to 135°, but still avoids the 180° that produced the resonance before.

For this compromise, R_{D1} + R_{Bp1} = Z_{CB2} at f_{iB}. Then, R_{D1} + R_{Bp1} = $1/\omega_{iB}C_2$, where:

$$\omega_{iB} = 2\pi f_{iB} = \frac{1}{\sqrt{L_{Bp1}C_{B2}}}$$

Combining these expressions and solving for R_{D1} yields:

$$R_{D1} = \sqrt{L_{Bp1} / C_{B2}} - R_{Bp1}$$

From before, the 1-Ω impedance guideline defines $C_{B2} = L_{Bp1}$, and substitution yields the design equation:

$$R_{D1} = 1 - R_{Bp1}$$

Expressed differently, this equation prescribes that R_{D1} + R_{Bp1} = 1 Ω for a total 1-Ω resistance in the C_{B1} path. This repeats the 1-Ω guideline underlying bypass selection.

Typically, the above R_{D1} equation defines difficult resistance values of a fraction of an ohm. Such resistors exist, but can be expensive and difficult to acquire. However, when required, only this solution removes the effects of the f_{iB} bypass resonance. Fortunately, just choosing a different capacitor for C_{B1} generally provides an adequate detuning resistance. Choosing a C_{B1}' with $R_{Bp1}' \approx 1\ \Omega$ detunes the f_{iB} resonance, but still avoids exceeding the 1-Ω guideline. Fortunately, this resistance doesn't have to be precise to provide sufficient detuning of the f_{iB} resonance. Often, just switching C_{B1} from ceramic to tantalum serves this purpose.

Note that the C_{B1} switch also requires changing the secondary bypass value, C_{B2}. A tantalum C_{B1}' substitutes an increased L_{Bp1}' for L_{Bp1}, requiring re-computation of the corresponding $C_{B2}' = L_{Bp1}'$. Increasing C_{B2} theoretically increases its inductance and would degrade higher frequency stability. However, practical limitations generally leave the net inductance condition unchanged.

In practice, some minimum lead length and inductance always accompany a capacitor construction and installation. Just the lead length from an amplifier package pin to the internal chip will be about 0.05 in. and introduce about 0.8 nH. Chip capacitors serving the secondary-bypass function typically display similar inductances, independent of the capacitor value. Therefore, increasing C_{B2} to accommodate the C_{B1} change does not significantly degrade stability.

Adjustments to the Figure 2 example illustrate this alternative. In the example, a very low parasitic resistance accompanies the C_{B1} that's shown. With that capacitor, R_{Bp1} = 0.02 Ω, thanks to the more ideal capacitor permitted by ceramic construction. However, this low resistance does little to detune the resonances previously described. Switching to a less ideal capacitor (the tantalum Kemet T421B474M050AS) raises this resistance to 0.8 Ω for an adequate approximation of the desired 1-Ω optimum. This capacitor switch also raises L_{Bp1} from 1.6 nH to 16 nH, requiring a corresponding increase in C_{B2}. Switching C_{B2} to the 15-nH Kemet C052C153K2G5CA makes the adjustment for the required 10:1 increase. The latter switch leaves the parasitic inductance of C_{B2} unchanged at 0.8 nH.

Supply Decoupling

Power-supply bypass provides the best first defense against supply-coupled noise and related instability. However, sometimes the bypass that preserves stability does not sufficiently reduce the noise coupled from other circuitry. At that point, supply decoupling filters may be required. This typically occurs when the supply-line noise contains frequencies above the amplifier's useful PSRR range. Then the lack of PSRR often couples supply-line noise straight through the amplifier to its output. Subsequent filtering would remove this noise, but not the intermodulation effect of this higher frequency noise.

As described before, the filtering effectively removes the direct effect of this higher frequency error signal without restricting signal bandwidth. But this filtering can't similarly remove noise components that intermodulation distortion down shifts into the amplifier's useful frequency range. Consequently, the higher frequency supply noise reacts with the amplifier's signal and distortion sources, producing error signals in the lower frequency range of the amplifier.

In this case, prevention must supersede cure in the reduction of supply-coupled noise. Power-supply decoupling filters prevent the higher frequency signals from even reaching the amplifier. The simplest decoupling alternatives include RC, LC, or RLC lowpass filters *(Fig. 5)*. The three lowpass-filter configurations shown in Figure 5 represent decoupling circuits placed between a power-supply source (V_+) and the amplifier's positive supply pin (V_P). While shown as a single capacitor, C_B represents the combined capacitance of all capacitors used for the supply bypass of V_P.

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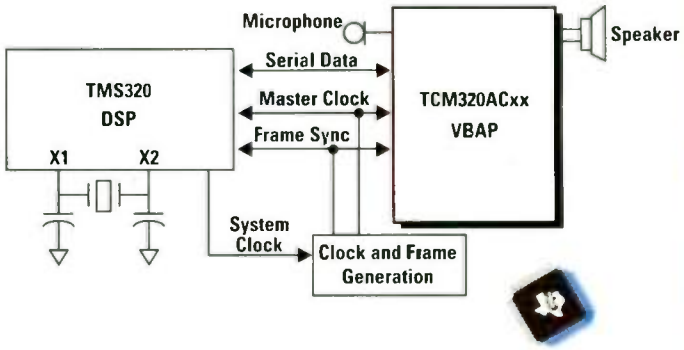
	TCM320AC36	TCM320AC37	2.048	5 V
IS-19, IS-54/136 Digital Cordless, CO and PBX, (Noise Cancellation Disabled)	TLV320AC56	TLV320AC57	2.048	3 V
	TCM320AC56	TCM320AC57	2.048	5 V
DECT	TLV320AC40	TLV320AC41	1.152	3 V
GSM	TCM320AC38	TCM320AC39	2.600	5 V



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In practice, the negative supply line would have an identical filter. But the positive supply case shown in Figure 5 serves to illustrate the decoupling principles.

Each of the three filter alternatives adds series impedance in the supply line to combine with the bypass capacitance C_B and form a low-pass filter. Then, the high-frequency noise contained in V_+ drops across the series impedance rather than transferring to the V_P supply pin of the op amp. The added series impedance doesn't have to be mounted close to the amplifier to provide the desired decoupling. But it should be placed so that it doesn't conduct the supply current drain of any circuitry other than that of the amplifier.

The type of impedance that is added determines the relative cost and decoupling effectiveness. And this effectiveness depends upon both the filter response and the line impedance presented to the amplifier. The RC solution offers the lowest cost and still produces appreciable decoupling results *(Fig. 5a)*. With this circuit, decoupling resistance R_D absorbs and dissipates the higher frequency, transient energy, transferring a more stable voltage to the C_B capacitance. Analysis of the decoupling circuit in Figure 5a reveals this action in the classic RC-filter response:

$$V_P = V_+/(1 + R_DC_Bs)$$

This response rolls off the supply-line noise with a single pole at $1/2\pi R_DC_B$.

At lower frequencies, however, this simple RC decoupling increases the supply-line impedance, potentially increasing the PSRR error. To calculate this impedance effect, assume that the V_+ power supply presents zero output impedance, effectively placing R_D in parallel with C_B. This sets the decoupling impedance that's seen from the V_P terminal as:

$$Z_{Da} = R_D/(1 + R_DC_Bs)$$

At low frequencies, the RC filter increases line impedance by the amount R_D. To limit this effect, the R_D resistance must be kept low. A discussion later in this article describes R_D value selection.

Alternately, LC filtering removes this impedance increase and produces a double-pole, rather than single-pole, roll-off of supply-line noise. However, this alternative introduces another impedance increase through a supply line resonance *(Fig. 5b)*. Figure 5b illustrates this case with inductor L_D simply replacing the previous resistor R_D. Then, the LC filter presents the low impedance of the inductor to the lower frequency current demands from the V_+ power supply. The filtering response of this alternative rolls off supply-line noise with a double pole at:

$$f = \frac{1}{2\pi\sqrt{L_DC_B}}$$

that's described by:

$$V_P = V_+/(1 + L_DC_Bs^2)$$

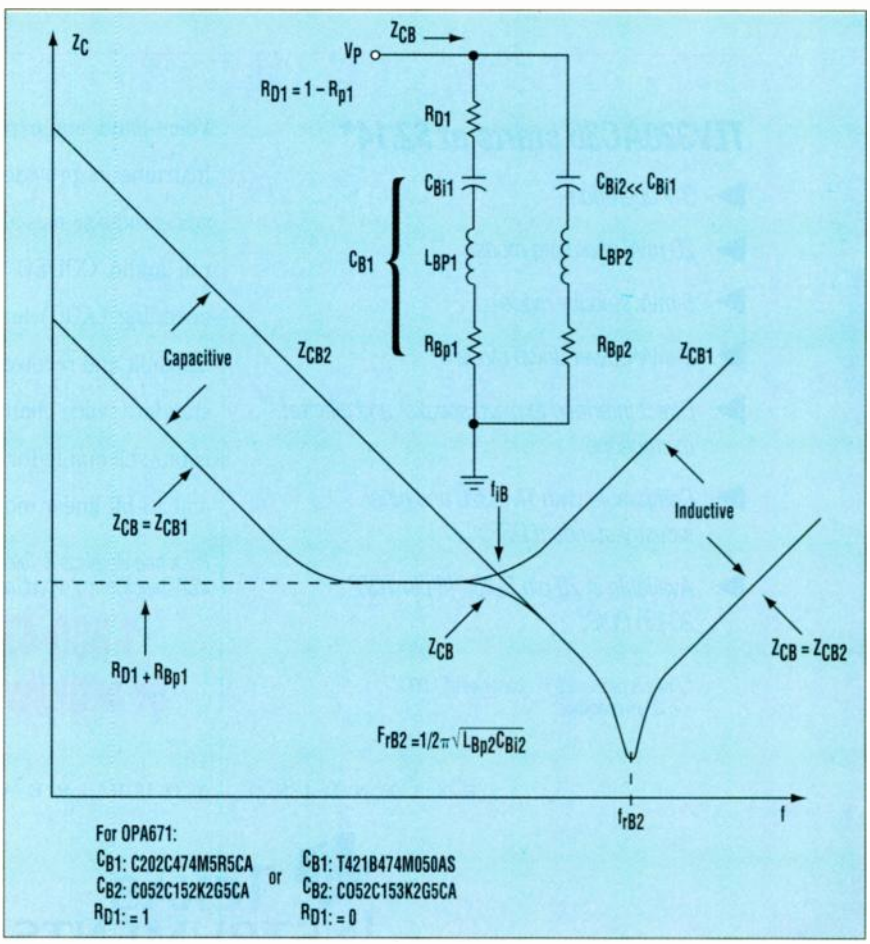
In contrast to the RC filter, the LC filter does reduce the supply-line impedance, but only at lower frequencies. The impedance seen from the V_P terminal becomes:

$$Z_{Db} = L_Ds/(1 + L_DC_Bs^2)$$

At lower frequencies, the s term of the Z_{Db} numerator ensures low impedance. But this term tends to increase Z_{Db} at higher frequencies. Counteracting this increase, the s^2 term of the denominator returns the net impedance response to a single-pole roll off like that attained with the RC filter.

Therefore, the LC filter offers two-pole roll off of supply-line noise and reduced low-frequency line impedance. But at an intermediate frequency, the Z_{Db} impedance increases due to a new LC resonance. From an energy perspective, the L_D inductor stores, rather than dissipates, the transient energy of supply-line noise, giving rise to this resonance.

At most frequencies, the inductor simply releases its stored energy to the bypass capacitance and the ampli-



4 Adding resistance R_{D1} in series with C_{B1} detunes two of the resonances shown in Figure 3, but at the expense of an elevated Z_{CB} level for intermediate frequencies.

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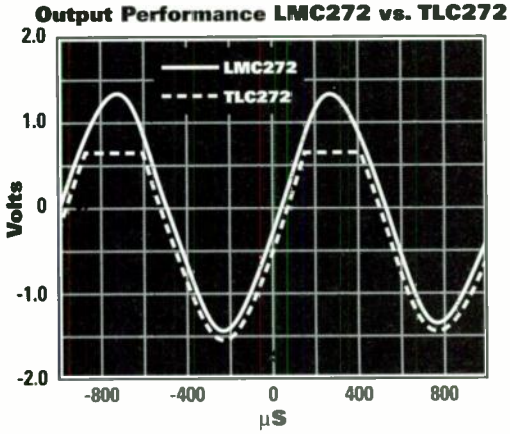

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fier in a more gradual manner than initially presented by a supply noise transient. This smoothing of the energy release protects the amplifier from supply-line noise by reducing the associated frequency content to a range where amplifier PSRR remains high. But at the inevitable LC resonance, the Z_{Db} impedance rises and the filtering fails. As indicated by the Z_{Db} denominator ($1 + L_DC_Bs^2$), the L_D-C_B combination produces a double pole and a resonance at:

$$f_{rDb} = \frac{1}{2\pi\sqrt{L_DC_B}}$$

This resonance increases, rather than decreases, the line impedance in the vicinity of f_{rDb}.

Resonance makes the simple LC decoupling filter an uncertain alternative for op-amp circuits having high noise gains. At resonance, energy stored in the inductor by supply-line transients circulates between the capacitor and inductor until dissipated by some energy drain.

In the ideal LC case, this circulation continues indefinitely, sustaining an oscillation signal. In practice, even though parasitic resistances and the amplifier help absorb that circulating energy, the amplifier's PSRR error and gain offer replenishment to support the oscillation. Supply-voltage transients or noise containing frequency components in the range of the f_{rDb} resonance can initiate this oscillation condition.

Adding a detuning resistor removes the resonance and the oscillation uncertainty, but also reduces the noise roll-off. This alternative combines the R_D and L_D series impedances of the two preceding cases *(Fig. 5c)*. The combination provides both the energy absorption of the RC filter and the reduced low-frequency impedance of the LC filter. The filtering response for this RLC combination is defined by:

$$V_P = \frac{\left[1+(L_D/R_D)s\right]V_+}{1+(L_D/R_D)s+L_DC_Bs^2}$$

The s^2 term of the denominator initially continues the two-pole roll-off advantage of the basic LC case. However, the s term of the numerator indicates a response zero that returns this roll off to single-pole. Therefore, adding R_D to the LC filter reduces the filter attenuation.

Still, R_D improves the decoupling's effectiveness by detuning the line-impedance resonance that otherwise adds gain to the parasitic PSRR feedback loop. Analysis of the Z_{Dc} impedance, as seen from the V_P terminal, yields:

$$Z_{Dc} = \frac{L_Ds}{1+(L_D/R_D)s+L_DC_Bs^2}$$

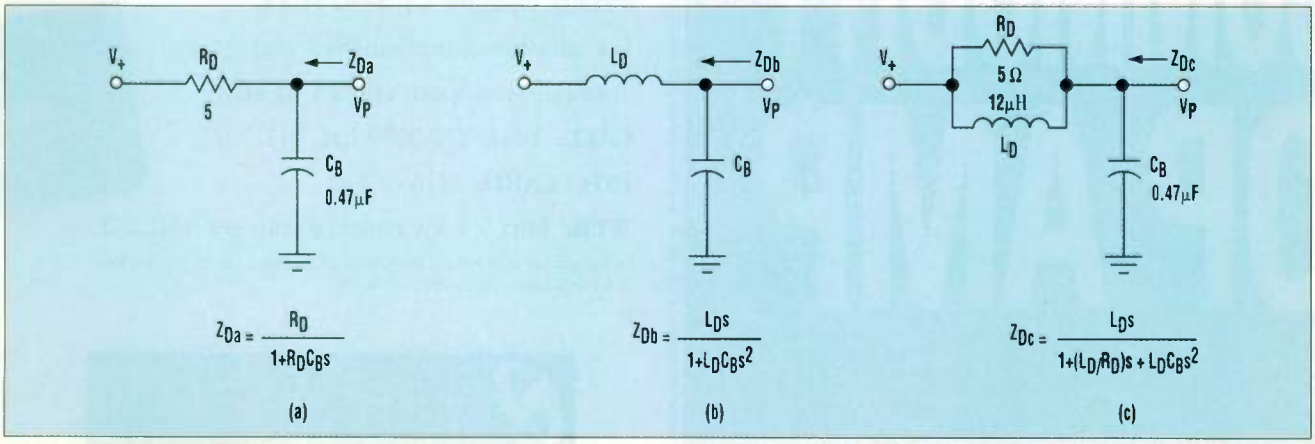
This expression repeats that of the previous Z_{Db}, except for the $[(L_D/R_D)s]$ term in the denominator. That term separates the circuit's two poles to detune the characteristic LC resonance and remove the associated impedance rise.

Line Impedance Control

Two compromises guide the selection of the decoupling filter components. The first is a repeat of the bypass-capacitance selection described earlier—optimizing the value of C_B to maintain frequency stability. Design equations that were developed earlier in the article guide this selection. The second compromise guides the selection of the series impedance to limit noise coupling without significantly degrading other performance.

The series impedance, R_D or the R_D-L_D combination, must be large enough to intercept high-frequency line transients but not so large as to compromise the circuit's lower frequency PSRR error signal. Power-supply decoupling reduces the supply-line noise produced by other circuitry, but can increase the parasitic feedback produced by the amplifier itself. At lower frequencies, the bypass capacitors fail to roll-off the line impedance, and adding the series impedance increases the supply-line impedance seen by the amplifier. The discussion accompanying Figure 1 describes the noise-coupling effect of this impedance. The net effect upon circuit performance remains a function of multiple variables which discourage analysis.

On the other hand, following the previous bypass-capacitor selection guidelines and setting R_D equally to about 5 Ω serves most amplifiers that supply output currents in the 10-mA range. This 5-Ω guideline, combined with the 1-Ω guideline for C_B, produces a filter with at least a 6:1 reduction of higher frequency noise. Also, adding just 5 Ω generally retains lower frequency line impedance at an acceptable level. Amplifiers supply-



5 Power-supply decoupling places series impedance between the output of a power supply (V_+) and the op amp's supply terminal (V_P) to intercept high-frequency supply-line transients. The simplest decoupling options are RC (a), LC (b), and RLC (c) lowpass filters.

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ing greater output current require correspondingly lower values for R_D. For RC filters, this R_D selection completes the decoupling design.

For RLC filters, selection of L_D still remains. Adding the L_D inductor of Figure 5c benefits performance as long as the inductance chosen forms a detuned resonant circuit with the C_B and R_D that have been chosen. Making L_D larger minimizes the line impedance at lower frequencies, but potentially increases it at the LC resonance. For optimum detuning of this resonance, the L_D impedance should equal R_D at the frequency of the potential resonance. From the discussion of Figure 5b, the undamped resonance would occur at the frequency:

$$f_{rDb} = \frac{1}{2\pi\sqrt{L_D C_B}}$$

The impedance of L_D is:

$$Z_{LD} = 2\pi L_D f_r = \sqrt{L_D / C_B}$$

Setting this equal to R_D yields:

$$L_D = R_D^2 C_B$$

Capacitance C_B represents the combined value of the bypass capacitors connected to the associated supply terminal. ED

References:

1. Graeme, J., "Design Equations Help Optimize Supply Bypassing For Op Amps," *Electronic Design Special Analog Issue*, June 24, 1996; pp. 9-25.
2. *Ibid.*
3. *Ibid.*
4. Graeme, J., "Feedback Plots Offer Insight Into Operational Amplifiers," *EDN*, January 19, 1989; p. 131.

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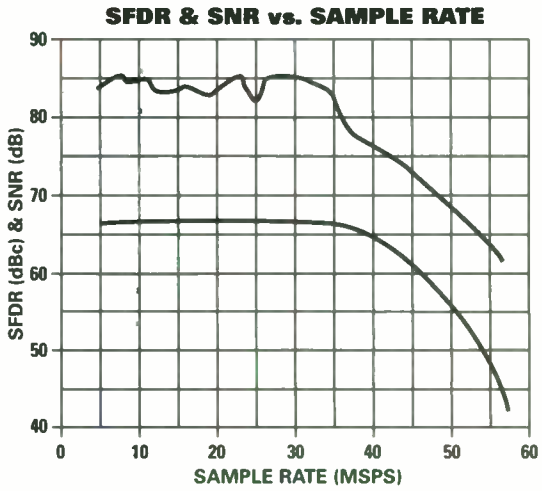

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An Ounce Of Prevention: Know Your ADC Input

Understanding The Input-Impedance Characteristics Of CMOS ADCs Early On Helps Avoid Problems Later.

JEROME E. JOHNSTON
Crystal Semiconductor

It should come as no surprise that CMOS is a popular mixed-signal technology for many of today's analog-to-digital converters (ADCs)—after all, it offers lots of digital logic density, good analog switches, fast slew amplifiers, and high-quality capacitors (although limited in size). The combination of these mixed-signal capabilities has resulted in a number of different ADC architectures. However, many of the CMOS-based sampling converters have similar analog input structures that are constructed with analog switches, sampling capacitors, and in some devices, buffer amplifiers *(Fig. 1)*.

The circuits in Figure 1 illustrate three common input configurations. These basic inputs are found in capacitive-based successive approximation register (SAR) converters and in delta-sigma converters. Understanding these structures and their operation can help the ADC system designer maximize the circuit's performance and avoid application pitfalls.

An unbuffered capacitor sampler is the most basic of the three input configurations *(Fig. 1a)*. Each time switch S1 is on, the capacitor is charged by the external signal source. When S1 turns off and S2 turns on, the capacitor transfers a specific amount of charge. This switching process is repeated at a high frequency. The severity of the dynamic load seen by the external driving amplifier will be determined by the size of the capacitor and the frequency of the switch closure. In other words, the dynamic operation of the sampler determines the input impedance seen by the external driving circuitry. The fundamental equations for charge can be used to derive either the effective input resistance to the sampler or the input current. The basic charge equations are:

$$i = \Delta q/\Delta t \text{ and } q = cV$$

The instantaneous current (i) is equivalent to the charge (q) per unit time (t), and charge (q) is equivalent to the product of the capacitance (c) and the voltage (V). From these basic equations, the input current to the unbuffered sampler of Figure 1a is defined as:

$$i = Vc/t \text{ or } i = Vfc$$

where $f = 1/t$

Notice that the input current into the device is proportional to the sig voltage to be measured. By rearranging the input current equation, the in resistance is shown to be:

$$r = V/i = 1/fc$$

The equation for the input resistance also indicates that the effective impedance of the sampler decreases as the sample clock frequency is incre or as the size of the sampling capacitor is increased.

If the size of the sampling capacitor is large, or if the sampling frequ is high, the unbuffered sampler can present a significant dynamic lo

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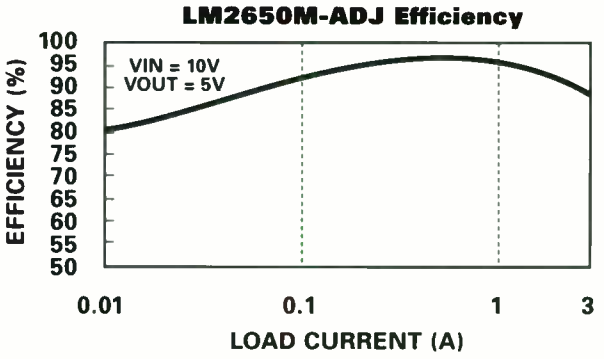

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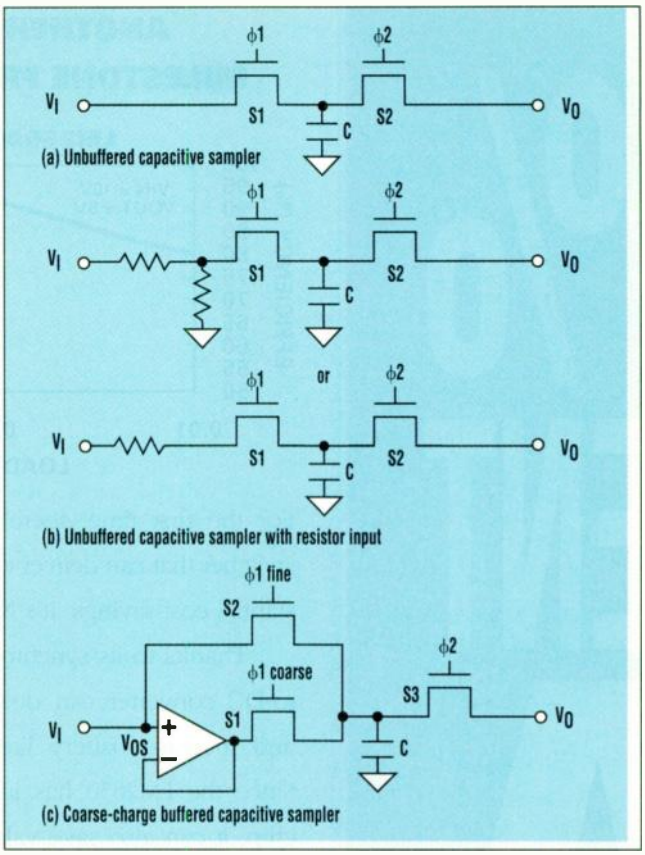
high-frequency transient current) to the external driving circuit. Some ADC input structures include a resistor to reduce the transient effect of the sampling current on the external driving amplifier *(Fig. 1b)*. Resistors also are included in some sampling architectures to perform voltage reduction (for example, to reduce ±10 V to ±2.5 V), and/or for level shifting. Level shifting makes it possible to perform conversion on a dual-polarity input signal with the ADC running off of a single +5-V supply. The compromise is that the resistors can introduce drift.

The third input configuration is a coarse-charge buffered capacitive sampler *(Fig. 1c)*. A sampler with a coarse-charge buffer uses a two-step sampling cycle. When the coarse switch is on (fine is off), the buffer charges the sampling capacitor to a voltage that's a coarse approximation of the input source voltage (V_I). The voltage output from the buffer includes the buffer's offset as well as the input signal. But the buffer supplies the majority of the current needed to charge the sampling capacitor, which greatly reduces the current demand from the source outside of the chip.



1 CMOS technology produces good analog switches and capacitors with low dielectric absorption. These two devices are the fundamental components needed in ADC sampling circuits. The most simple sampling circuit consists of an analog switch and a capacitor (a). The sampling capacitor must be fully charged each time the input signal is sampled, and the input driver must handle the resulting dynamic load. Sometimes, the sampling capacitor is isolated with an input resistor (b). The resistors also may be used for level shifting the input signal. Dynamic-load currents seen by the simple sampler (a) can be reduced by adding a coarse-charge buffer to the circuit (c). The sampling capacitor is charged by the buffer, then connected directly to the input signal so that it can be charged to its final voltage. This greatly reduces the dynamic current seen by the external driver.

The sampler then enters into the fine-charge sampling phase. Fine charge (fine switch is on, coarse switch is off) bypasses the buffer and connects the external source directly to the sample capacitor. This enables the sampling capacitor to be charged to a voltage equal to the input voltage. The amount of current sourced during fine charge will be a function of the offset voltage of the coarse-charge buffer. The input current for the buffered sampler is:

$$i = V_{OS}/(1/fc) = V_{OS}fc$$

where V_{OS} is the offset of the buffer, f is the sampling frequency, and C is the sampling capacitor. The input current for the buffered sampler is not a function of the input voltage; instead, it is constant as long as the V_{OS} of the buffer, the sampling frequency, and the sampling capacitor remain constant. Note that the polarity of the input current in the buffered sampler will be determined by the polarity of the offset voltage of the coarse-charge buffer. The buffered sampler significantly reduces the current required from the input circuit when compared to the unbuffered sampler with the equivalent sampling capacitors and sampling frequency.

ADC Behavior

Now that some of the basic input structures of CMOS ADCs have been described, let's examine how the behavior of these circuits can interact with other system-level components to introduce some application pitfalls. Then we'll look at how some imperfections that occur in these sampler circuits in real-world silicon manifest themselves as measurement inaccuracies in high-resolution (usually 16 bits and above) measurement systems. Keep in mind that some of the application examples will illustrate some common system-level application issues that may be vendor specific. There are many subtle "gotchas" that one can encounter when pursuing perfection in high-resolution measurement.

Let's look at the basic input sampling structure for Crystal Semiconductor's CS5016 50-kHz, 16-bit, self-calibrating SAR converter *(Fig. 2)*. The converter's input is being driven directly from an OP-27 (generic brand) op amp *(Fig. 2a)*.

When the CS5016 is configured to run at 50 kHz, the sampler is clocked at 1 MHz. The offset of the coarse-charge buffer is typically 20 mV. When the sampler switches from coarse charge to fine charge, the OP-27 op amp is instantly loaded by a 150-pF capacitance inside the ADC and asked to provide an instantaneous transient current.

Just how will the OP-27 behave when loaded with a repetitious transient capacitance at a 1-MHz switching frequency? Not all OP-27 amps will behave the same, because not all OP-27 amps are the same. The OP-27 op amp can be purchased from several different manufacturers, and the device number (OP-27) doesn't guarantee that devices from different manufacturers are designed with identical open-loop phase-gain characteristics, or with identical output-stage structures. Both of these can influence how a particular brand of OP-27 reacts to a high-speed transient load.

The phase-gain characteristics of the typical OP-27 operational amplifier

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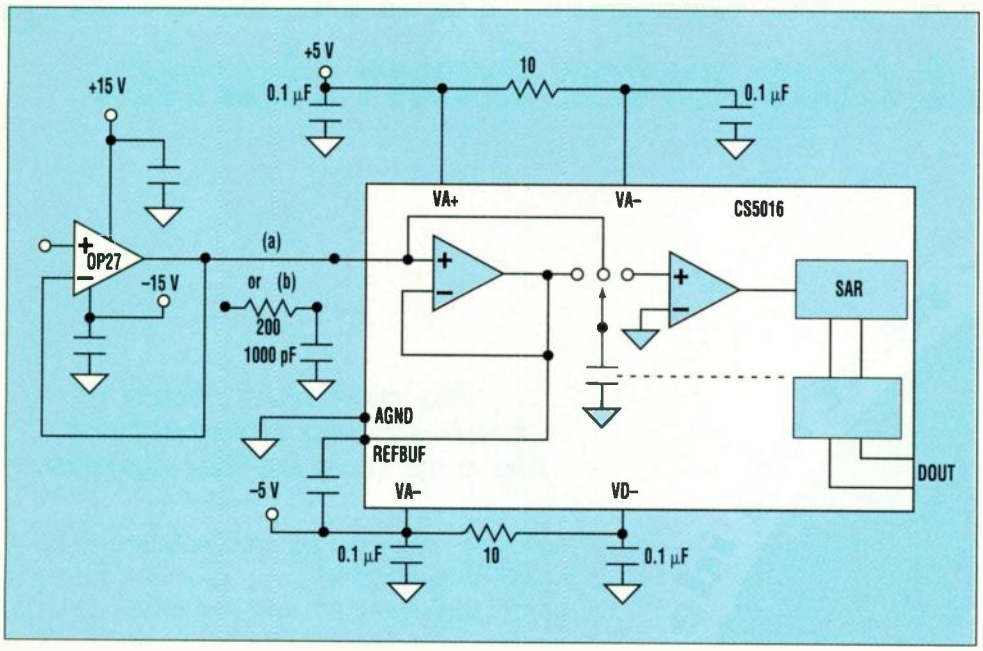
ADC INPUT CONFIGURATIONS



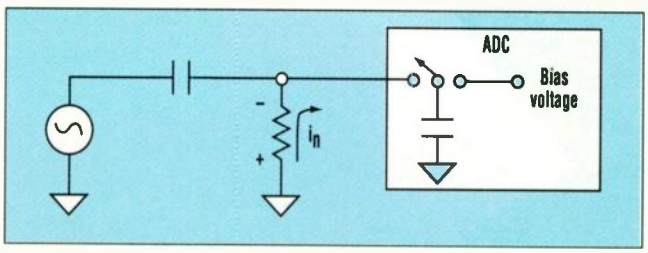
2 Switched-capacitor samplers prefer an RC at the input. Some popular op amps like the OP-27 can have difficulty driving the dynamic-load requirement of a sampling capacitor. An RC network between the op amp and the ADC's sampler circuit is recommended by ADC manufacturers. This provides a low dynamic-source impedance to the sampler while also supplying the op amp with a more resistive load.

can result in gain peaking in the region between 2 and 7 MHz when the amplifier is connected in a low-gain (under 20 dB) configuration. The output of an amplifier with gain peaking can ring when subjected to a transient load, especially a transient load capacitance. The exact behavior may vary among brands of amplifiers, and may also vary from one production lot to the next.

One of the more peculiar behaviors is that the OP-27 amplifier may operate properly over a range of output voltages, but ring when attempting to source output voltages near zero volts. When a system designer encounters this problem, he or she can mistakenly conclude that the ADC has missing codes near bipolar zero if he only examines the output codes from the converter. But the actual cause of the problem is that the op amp's output is unable to remain stable when attempting to source voltages near zero into a dynamic load. The amplifier output rings and the sampler actually captures some point on the magnitude of this ringing output.

It's common for manufacturers of SAR and delta-sigma converters to recommend a specific RC filter to place in front of the sampler inputs *(Fig. 2b)*. The R value is chosen to isolate the driving amplifier from the transient capacitive load of the sampler. The C value is selected to provide a very low source impedance to the sampler transient, while also providing a reservoir of charge. In addition, the RC time constant is chosen to be short enough to allow the sampler to settle to full accuracy in the allotted sample time.

Some users mistakenly think the purpose of the RC filter is to provide some level of antialias filtering. In an attempt to get better bandwidth reduction, these users will increase the RC component values. This is a mistake, and results in making the RC time constant so long that the settling time exceeds the time the sampler needs for proper settling. The increased settling time of the RC filter will manifest itself as a measurement inaccuracy. We'll look more closely at this problem later in this article.



3 Capacitive samplers will charge an ac-coupling capacitor. In some audio applications, designers prefer ac coupling the signal path to prevent the signal-conditioning circuit's dc offsets from getting into the ADC. However, the ADC's sampler circuit may charge the ac-coupling capacitor to an offset of its own.

PROPER DIELECTRIC

Besides using the correct RC component values, be certain to use a capacitor with an appropriate dielectric. The high-K dielectrics of certain ceramic capacitors (X5F and Z5U) can exhibit dielectric absorption problems. Some monolithic ceramic capacitors also can exhibit absorption problems. In an instrumentation application, this absorption can sometimes introduce obscure errors. If the input to the sampler is a constant dc value, the effects of the absorption could go unnoticed. Errors due to dielectric absorption may only become obvious in a multiplexed application in which the input voltage for each subsequent sample is changing by large amounts. This can reveal rather large errors that result from having inadequate settling time.

Capacitors with high-K dielectrics exhibit a large change in capacitance versus applied voltage. For signal-processing applications, this can introduce distortion. Therefore, if designers want to achieve top performance in signal-to-distortion (S/D) ratio, they should use ceramic capacitors with stable capacitance versus voltage characteristics, such as aC0G dielectric. Distortion caused by the capacitor dielectric characteristics is especially evident in high-dynamic-range ADCs such as Crystal's CS5321/CS5322 delta-sigma chip set (120-dB signal-to-noise at 1-kHz sample rates). A good circuit-board layout allows this chip set to achieve typical signal-to-distortion that's better than 116 dB with C0G capacitos. Use of ceramic caps with a X7R dielectric, considered to be a fairly stable dielectric, can reduce S/D performance to about 108 dB. Other dielec-

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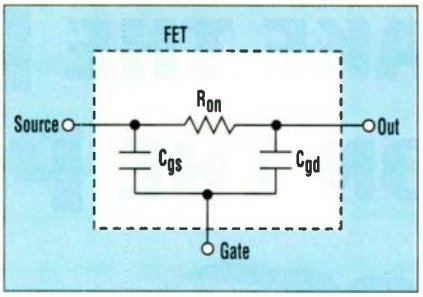
trics may cause even greater performance degradation than the X7R dielectric. Be certain to follow the semiconductor manufacturer's recommendations for any RC components in front of sampler inputs, including both component values and dielectrics.

Certain ADC applications use only ac signals. These systems call for the removal of any dc offset in the signal to be digitized. In an attempt to keep any dc offsets from reaching the input to the converter, some users will place an RC high-pass filter at the ADC input *(Fig. 3)*. The charge input demanded by the sampler will charge the coupling capacitor with an offset voltage. This offset voltage is a function of the internal bias voltage into which the sampler dumps its charge. In ADCs that operate from dual supplies (+5 and –5 volts), the bias voltage may be near ground. In converters that operate from 0- to +5-V supplies, the bias voltage can be near +2.5 volts. However, the tendency for the sampler to charge the input coupling capacitor can introduce its own offset error in the sampled result. One needs to be aware that a capacitively coupled input may remove offset from the signal, but this doesn't eliminate the possibility of the sampler introducing an offset voltage of its own.

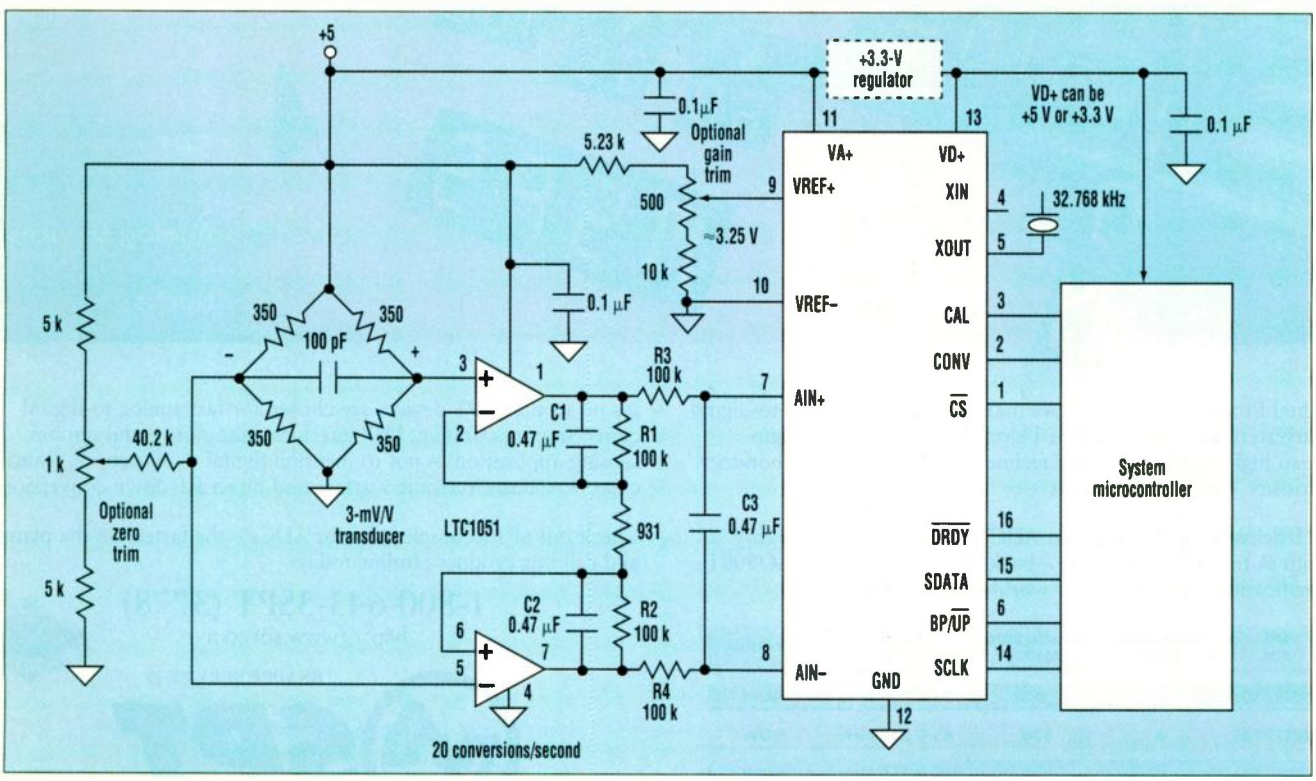


4 A simplified MOSFET model shows the intrinsic capacitances that allow for charge injection. Charge injection occurs in the transistors that make up analog switches. Whenever the gate-control voltage is switched, this transition is coupled through the intrinsic capacitances to the transistor's drain and source connections.

The latest generation of audio ADCs solve this offset problem. First, the converter runs from a single +5 V supply. The signal input is specifically designed to be capacitive-coupled as this allows the ground referenced input signal to be level shifted to a reference value near +2.5 volts. Also, a digital high pass filter may be included to remove any offset at the front end of the converter from the output conversion words.

Several manufacturers have introduced delta-sigma ADCs intended for low-level (< 1 volt) instrumentation applications. Some of these converters include gain-ranging circuits and programmable output word rates. Users of these devices need to understand the various means by which gain ranging and programmable output rates are accomplished.

Some architectures with on-chip programmable-gain amplifiers change the size of the sampling capacitor or the frequency at which the sampler operates to achieve an effective change in the signal gain. Changing the output word rate of the converter can affect the frequency at which the input-sampling circuitry operates. Remember from the equations discussed earlier that the input impedance is a function of the sampling frequency and the size of the sampling capacitor. If the size of the sampling capacitor or the frequency of the input sampler is changed to implement a gain change or to change the output



5 High-valued resistors can introduce new error components at the sampler's input. The source impedance at the input of a CMOS sampling ADC is usually dominated by an RC network. Don't exceed the manufacturer's recommended values for R and C. In this figure, the designer has used large R and C values to add another low-frequency filter corner to the input-signal-conditioning circuitry of the CS5509. These R and C values can introduce new sources of offset error and drift.

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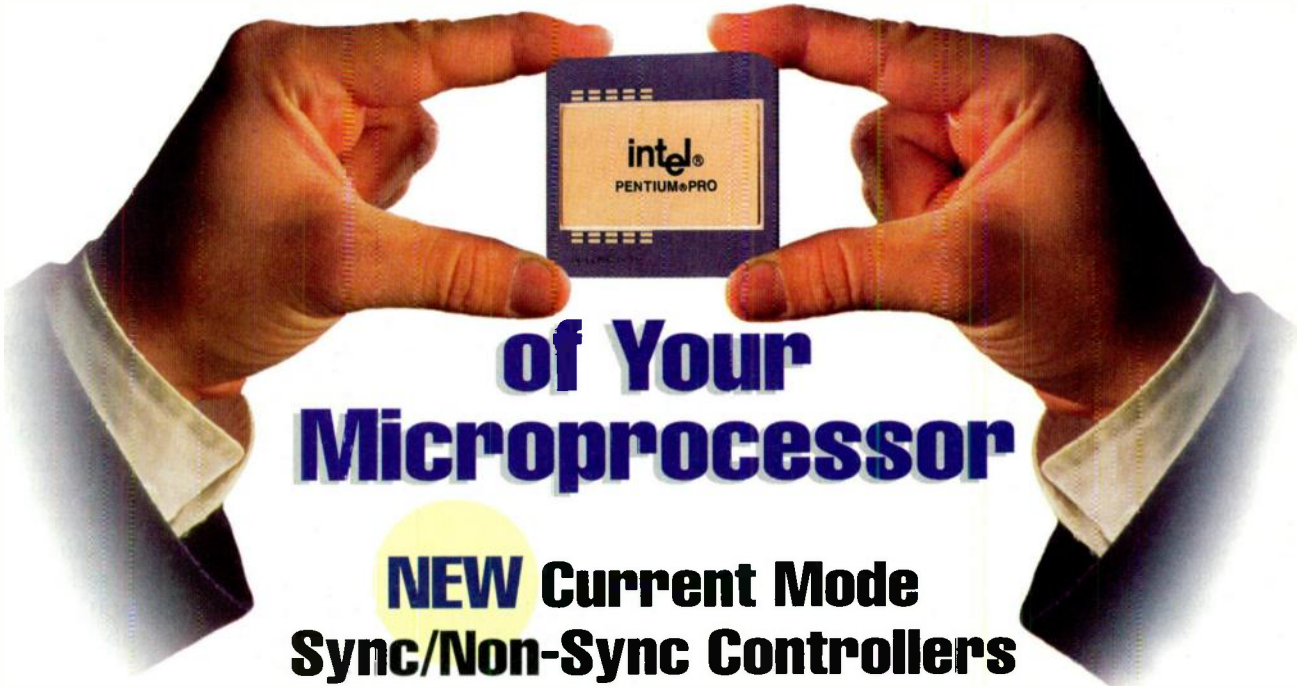

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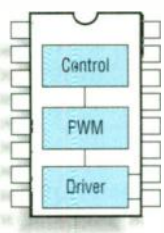

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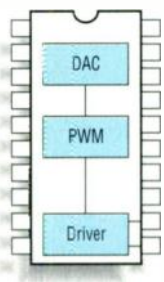

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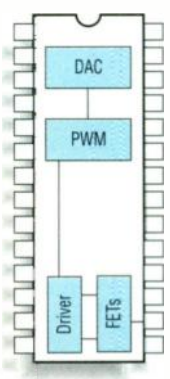

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word rate, the magnitude of the input impedance to the converter will also change. And this input impedance will be modified each time a new gain range or output word rate is selected.

Just how severe is this impedance change? The impedance can scale proportionally to the change in gain, or proportionally to the change in output word rate. For example, if the gain is doubled, the input impedance can be cut by half. If the output word rate is doubled, the input impedance can be cut by half. This large change in input impedance can interact with the external-driver source impedance to introduce magnitude changes in the input signal any time gain or output word rate is changed.

Fixed-Gain Input

Some converter designs maintain a stable input impedance even when a gain change is invoked. This is accomplished by having a fixed-gain input stage in which the sample capacitor and sampling frequency never change, followed by a second stage where the gain ranging is accomplished. In this architecture, users will always see a stable input impedance when the gain is changed.

A stable input impedance also can be achieved in converters that offer multiple output word rates. The converter can be designed to maintain a fixed sample frequency in the input stage, with all sample-rate changes accomplished by changing the decimation rate of the digital filter. Because the sample rate of the input stage is maintained at a constant frequency, users see a stable input impedance.

When selecting a delta-sigma converter with variable-gain selections, or with output-word-rate selections, be sure to understand the means by which these variable features are accomplished. Those devices that alter the input stage of the sampler can result in unexpected measurement errors if users aren't aware of the possible results that occur due to changes of input impedance.

In very-high-resolution delta-sigma ADCs intended for instrumentation applications, there are mechanisms in the input circuitry that could potentially introduce microvolt errors if not properly understood. Nonlinearity mechanisms are possible due to the imperfections in analog switches, and in the coarse-charge buffer. The input stage for many instrumentation-type ADCs may include some form of chopper stabilization. The chopping is intended to reduce offset error and offset drift, but the switches that perform the chopping can be a source of charge injection. Charge injection also can occur in the sampling switches of the capacitive sampler.

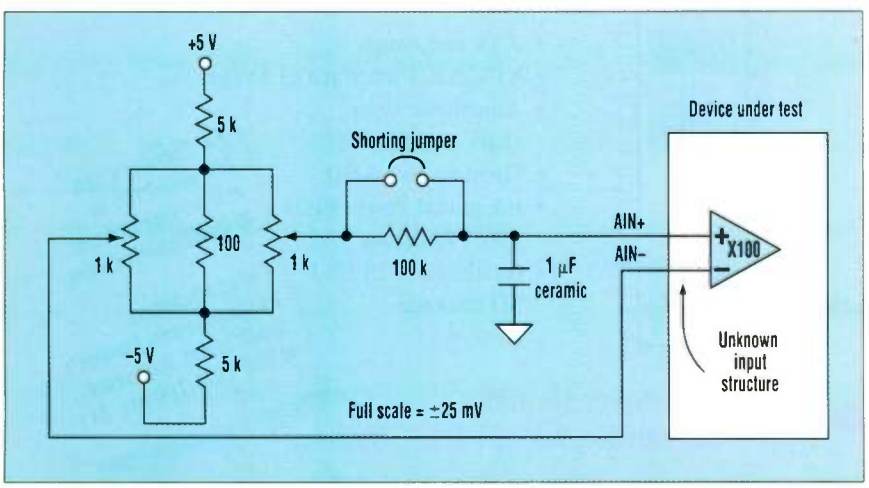
Let's look at the analog switch and examine how charge injection occurs *(Fig. 4)*. The figure illustrates a basic MOS-transistor switch, and shows how it includes capacitors from the gate to the source and from the gate to the drain of the device. Whenever the control voltage to the switch transitions from either high to low or low to high, the capacitors that are inherent in the construction of the device couple this voltage transition into the impedances on the source and drain leads of the device. The amount of the charge injection is dependent on the geometric dimensions of the transistor, as this affects the size of the capacitors, the magnitude and frequency of the control voltage, and the impedances connected to the source and drain leads of the device. The magnitude of the input signal passed through the switch also can influence the amount of charge injection, because this voltage will have some effect on the control-voltage threshold at which the transistor turns on or off.

Whenever designers use a discrete analog switch, or an individual field-effect transistor as an analog switch, an investigation of the charge injection introduced into the circuit by the switch is standard practice. But once this analog-switch function is internal to a more complex IC, system designers tend to forget about analog-switch imperfections. After all, wasn't the chip designer supposed to take care of all of that?

Chopper Circuit

For example, in a well-designed chopper circuit for low-level signals (+100 to −100 mV), charge injection may introduce an input current of 1000 pA with a 0-V input signal (the actual value will depend upon the specific design of the chopping switches). As the input signal is changed from +100 to −100 mV, the bias on the chopper switches is changed. This, in turn, changes the input current caused by charge injection.

While the change may be minute, it can be nonlinear with the input signal. For example, the input current could change from 900 pA at +100 mV to 1100 pA at −100 mV with a somewhat nonlinear characteristic. This change in input current with signal level will result in a voltage drop across any external source resistor, and the resulting voltage drop will introduce a nonlinearity that is a function of the input current. The magnitude of the nonlinearity seen by the ADC is greatly influenced by the choice of input resistance in front of the ADC. The data sheet for a specific ADC may recommend certain values for the RC components at the part's input. If larger values are used, the system



6 Shown is a test setup for measuring sampler input current. The ADC is used to measure the offset produced across a known input resistor. The input current can be evaluated for voltages across the entire span of the converter by using a potentiometer to adjust the magnitude of the input signal.

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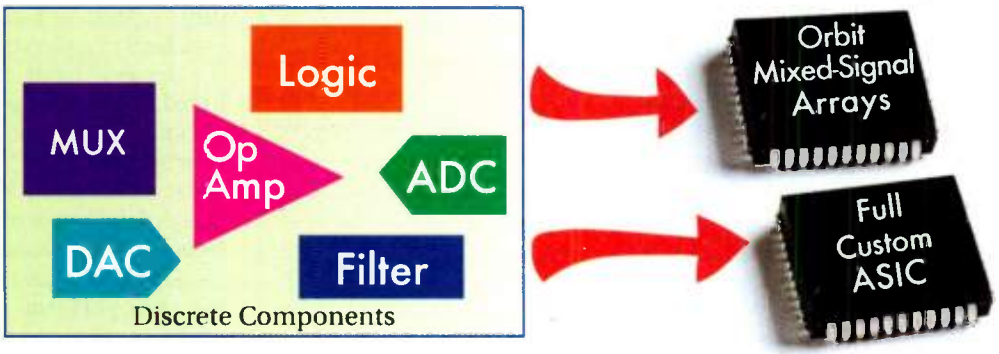

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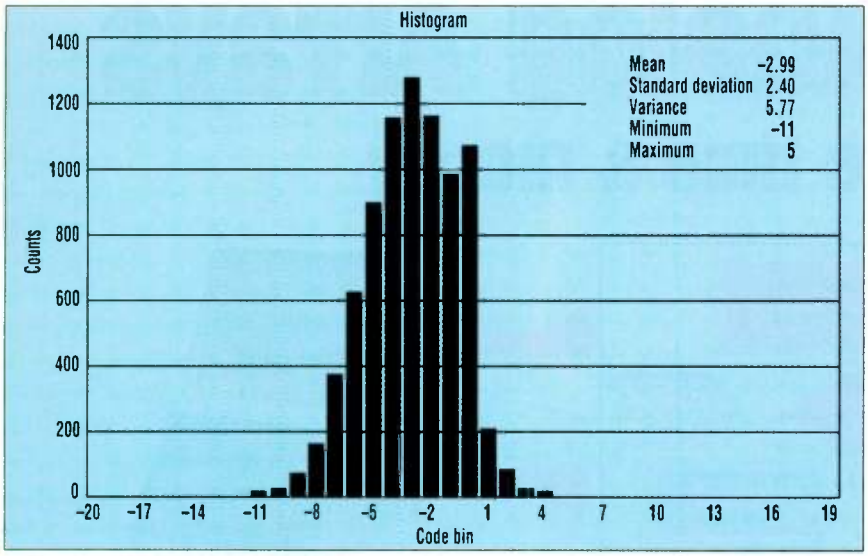

7 A visual histogram display adds confidence to data-set collection. When using the test setup of Figure 6, it may take several seconds for the RC network to settle to a final output value whenever the potentiometer is changed, or whenever the shorting jumper is removed. If multiple conversion words are collected (500 to 1000 preferred), a pictoral histogram of the conversion words can give users added confidence that the input has settled and that the statistical results are for a stabilized input.

performance can be degraded by these imperfections inside the device.

Designers can encounter similar limitations to measurement accuracy when using a converter with a coarse-charge buffered sampler. While the coarse-charge buffer achieves a significant reduction in the magnitude of the dynamic input current, the buffer also can introduce some surprises to the unwary. The magnitude of the dynamic input current into a coarse-charge buffered sampler is a function of the buffer's offset voltage, which may be of either polarity. The consequence here is that the dynamic input current may actually flow either into or out of the device.

The magnitude and the polarity of the offset can vary from device to device, and can also drift with temperature. Consequently, the dynamic current's magnitude and polarity can change over temperature. This is of no consequence if the input to the converter is driven from a low source impedance. But, there are applications where a large source impedance could be preferred.

For example, look at a weigh-scale digitizer in which the signal from the load cell is amplified and filtered before being input into the Crystal Semiconductor CS5509 ADC *(Fig. 5)*. In many static weighing applications, it's preferable to band limit the load cell signal to frequencies below 3 Hz. This is done to remove vibrations on the scale and to provide good rejection of the ac line frequency (50 or 60 Hz). It's common to use a two- or three-pole filter for this purpose. In the circuit shown, the differential input-differential output amplifier uses the RC elements R1C1, R2C2, and R3R4C3 to provide low-pass filtering of the input signal *(Fig. 5, again)*. But the large source resistances of R3 and R4 in front of the ADC can interact with the dynamic input current to introduce measurement inaccuracy into the system.

The fact that there's a dynamic current doesn't by itself cause a problem. The average value of the dynamic current will flow through R3 (and R4 for the other input) and produce a voltage drop. This initially introduces an error whose value can be calibrated out. But as the temperature changes, the dynamic current may change slightly in magnitude, and possibly even in polarity. Although the change in the magnitude of the current is small, it can introduce several microvolts of error if the value of the resistor is large. To put some numbers on this, the offset of the coarse-charge buffer may drift at about 20-30 μV/°C. This will result in an average input-current change of 5 to 8 pA/°C. And the resulting voltage drop across the input resistor can introduce a drift component of a few microvolts/°C. The error introduced by this mechanism could be avoided by not using such a large RC combination at the ADC's input.

To obtain the best linearity and stability in a high-resolution ADC that uses capacitive-based sampling, it's beneficial to understand the behavior of the dynamic input current when subjected to different operating conditions. Manufacturers specify their products when driven from low source impedances. With a low source impedance, many of the low-level input-current effects are of no consequence.

There are tests system designers can perform if they want to evaluate the behavior of the dynamic input current *(Fig. 6)*. Illustrated is a test setup for evaluating the input-current behavior of a high-resolution ADC. The divider-resistor values are chosen so that each of the potentiometers can be adjusted over the full bipolar input of the converter (this assumes the ADC has a fully-differential input. One ADC input is chosen as the reference, and is connected to its low-impedance potentiometer tap without a large series resistance or a filter capacitor. This allows that particular sampling input to fully settle when it samples.

The potentiometer on the second input (the Sig+ input) is then adjusted to give the desired output code from the converter with the large input resistor shorted out *(Fig. 6, again)*. The output code of the converter is recorded. The shorting jumper across the large measurement resistor is then removed and the output code for this condition is recorded. The measurement resistor is chosen to be 100k in this case. This will yield a voltage change across the resistor of 100 μV for each nA of current through it. It may be desirable to increase this resistor value if the input current to be measured is at the pA level.

Let's look at an example of this input test on a generic ADC. The ADC is a 16-bit device (65536 codes) operating in bipolar mode. The device uses a 2.5-V reference, but has an internal amplifier with a gain of 100. The gain has been system calibrated per the directions given in the manufacturer's data sheet. This yields an input span

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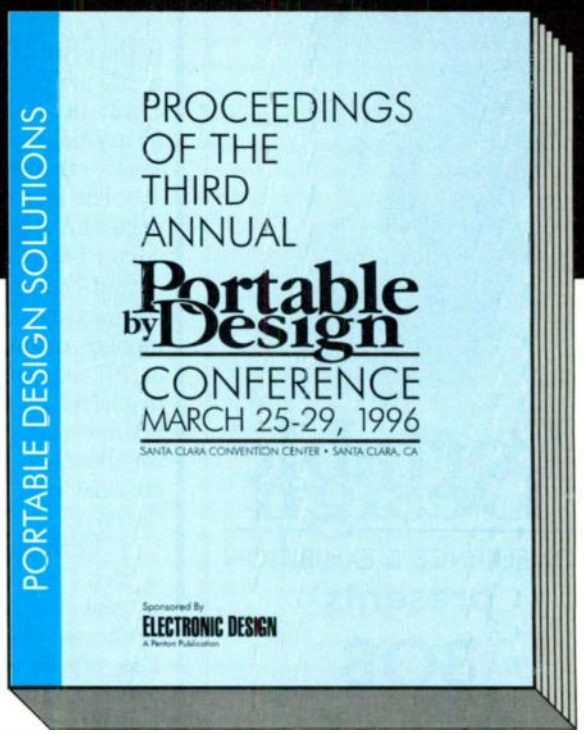

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to the converter of 2.5 V/100 = 25 mV, or ±25 mV for bipolar. Therefore, each count in the converter represents 50 mV/65536 = 763 nV.

Shorting Jumper

The shorting jumper is removed once the input voltage to the converter is adjusted to give the desired output code from the converter with the measurement resistor shorted. In bipolar mode, the converter spans 32,767 codes positive and 32,768 codes negative. In our example, the input voltage with the measurement resistor shorted is adjusted to give a bipolar zero code (code 00000), and then the shorting jumper is removed.

The time constant of the input RC is such that it averages the dynamic current and produces an offset voltage across the measurement resistor. The offset error across the 100k source resistance will be reflected by a change in the converter's output codes. In this case, the output code changed from code 00000 to 02116. This indicates a positive increase of the input voltage into the converter, and therefore represents a current flowing out of the converter's input pin with a value of (763 nV × 2116)/100k = 16.1 nA.

There are some precautions to consider when making these measurements. A high-resolution ADC will have noise in its output codes. Therefore, it's recommended that a number of output codes be averaged to compute the mean value of the output samples. To remove statistical uncertainty, the number of points to be averaged should be more than 500 (with about 1000 preferred). It's very helpful if a histogram of the conversion words can be displayed for each data set being collected *(Fig. 7)*. This histogram can visually give a confidence factor that the data is being collected in a satisfactory manner. Another precaution is to continue collecting repeated data sets until the results become repeatable from one data set to the next. Following this precaution will remove some uncertainties, such as whether the RC filter at the front of the converter has actually settled.

In doing testing in the lab, I've used a dc-voltage calibrator in place of the potentiometer shown in Figure 6. The calibrator was more convenient than the potentiometer because it had a keyboard on the front panel to enter the desired voltage. But, each time the output voltage was changed, the calibrator took almost 20 seconds to settle before its output could be considered stable to the 100-nV level. Taking repeated data-set collections out of the ADC, displaying the data set's histogram, and computing the mean value of the data set gave me confidence that the measurements were being taken properly. Once the input voltage from the calibrator had stabilized, the histogram plot and the calculated mean were repeatable.

Once the test setup is constructed, the current into the converter can be measured for different input voltages across the entire span of the converter. Some applications may call for measuring the current on both of the input pins to the converter. If a differential input signal is to be applied to the converter, it may be important to know how well the two inputs track. Depending on the quality of the converter's design, many factors may influence the input current's behavior. These include things such as temperature, power-supply voltage variation, common-mode voltage variation, changing the output word rate, or changing the gain if the ADC has gain-ranging on-chip.

The characteristics of the input current in a particular device may vary somewhat from manufacturing lot to lot. Making a measurement of the magnitude and behavior of the input current over the full input range of a converter can give users a first order estimate of what to expect. Investigating the input current of a sampling ADC and measuring the current's magnitude will reveal whether the ADC's input structure is a simple sampler or a coarse-charge buffered input. Understanding the various input structures, and the behavior of these structures, can help designers avoid causing significant system errors. ED

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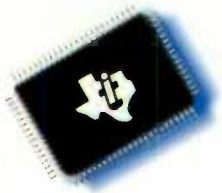
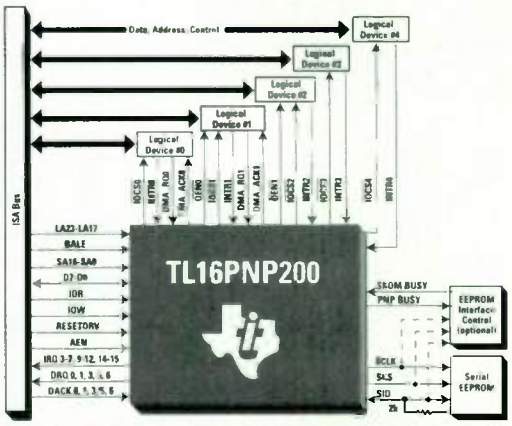
DMA Support	No	No	Yes
Package	44-pin PLCC 48-pin TQFP	68-pin PLCC	80-pin PLCC





NOTES: In mode 0, only logical device 0 and 1 are used. Any five DMA channels can be used in mode 1 and any three in mode 0. OEN0 and OEN1 can be used with any two logical devices in mode 1 and OEN0 can be used with either logical device in mode 0. BALE and LA23-LA17 are only used in mode 0.

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Analyzing Feedback In Circuits That Are Less Than Ideal

A Technique Using Driving-Point Impedance And Signal-Flow Graphs Makes Analysis Of Feedback Circuits Clear And Easy.

AGUSTIN OCHOA
Rockwell Semiconductor Systems, Brooktree Div.

Feedback is a useful tool that lets analog circuit designers reduce the sensitivity of a circuit's response to changes in active-element parameters caused by process variations, aging, and environment. Feedback allows the design of highly accurate gain stages defined by ratios of passive elements that are under better control by design or by selection, rather than by the properties of the active elements, like MOS transistor transconductance.

The topologies used in these circuits trade off excess gain for control by combining a fraction of a circuit's output with the input *(Fig. 1)*. In these circuits, the overall system transfer function, H(s), is defined for the ideal blocks by the cell's open-loop amplifier gain, $A_{ol}(s)$, and the system feedback factor, f:

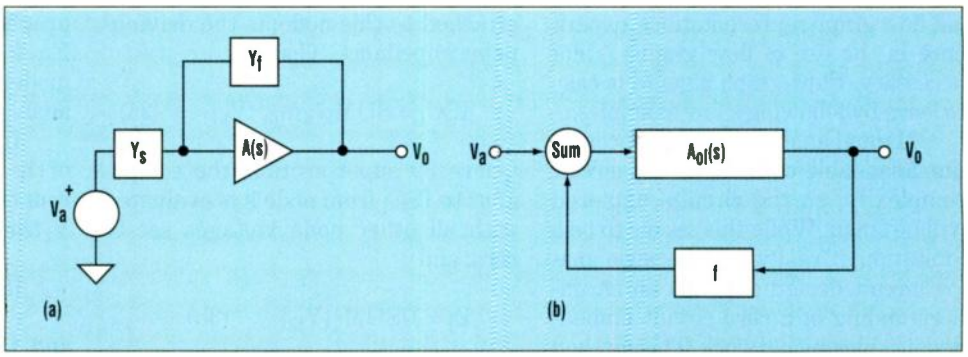
$$H(s) = A_{ol}(s)/[1-f\times A_{ol}(s)] \qquad (1)$$

When the magnitude of $f\times A_{ol}(s)$ is much greater than 1, Eq. 1 becomes asymptotic to -1/f, independent of the characteristics of $A_{ol}(s)$.

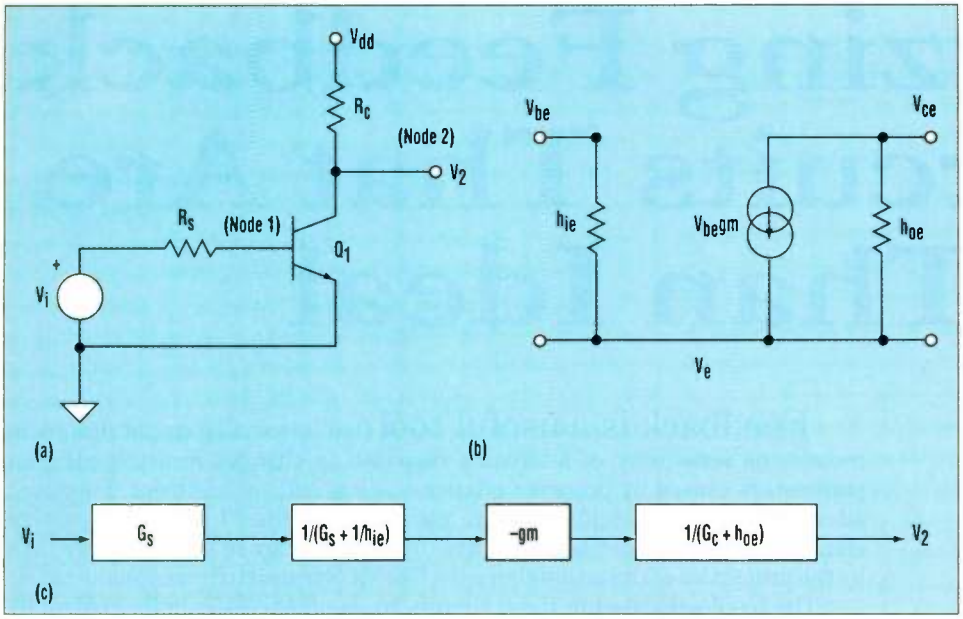
Eq. 1 works very well with op amps that have extremely high gains, high input impedance, and very low output impedance. Using these op amps, board designers and serious hobbyists quickly and easily produce well controlled functions.

The difficulty arises in identifying the block elements $A_{ol}(s)$ and f when the blocks are not quite ideal. Then the designer must include the loading effects at the amplifier's input and output due to source, load, and feedback impedances. The engineer putting together a discrete system or designing analog functions in an IC quickly finds that the 10-transistor amplifier circuit used to save area or ensure quick soldering simply does not behave "properly." This article deals with this non-ideal case.

First, a change in notation is appropriate, both for emphasis and to contrast with the ideal case. The system open-loop gain will be shown to be a misnomer in that it does not arise by simply opening the circuit's feedback loop. Instead, it arises from opening the feedback loop in the system's signal-flow graph. Remaining in the graph operation will be the loading effects of the feedback



1 Adding feedback to a circuit trades off excess gain for added control (a). The system transfer function typically is represented by the ideal blocks for the open-loop gain, A_{ol}, and feedback factor, f (b).



2 A single-stage amplifier using a bipolar transistor (a) can be represented by a small-signal model (b). The flow graph for the circuit shows the relationships between the circuit elements (c).

element on the input and output nodes and a feedforward current potential.

So to keep the notation straight, this article uses open-graph gain, $A_{og}(s)$, instead of A_{ol}. $A_{og}(s)$ is the proper relation and A_{ol} will converge to $A_{og}(s)$ as the amplifier block parameters become more ideal in comparison to the feedback admittance. This analysis becomes useful in identifying directly the factors in Eq. 1 in a form that allows the designer to understand how ideal his design really is.

Before analyzing the feedback circuits, it's a good idea to discuss the methodology, a few definitions, and an example circuit. After the technique, called the Driving-Point Impedance/Signal-Flow Graph (DPI/SFG) methodology, is defined and demonstrated, it is applied to three feedback circuits. Although the method uses signal-flow graph representations, experience in the use of flow graphs is not necessary. Flow-graph algebra is easy to learn by following a few examples.

Manual analysis quickly becomes unmanageable with increasing circuit complexity, so the circuits explored will be small. While this seems to be a limitation, it really isn't because analog circuit design depends on an understanding of a core circuit embedded in a biasing network. This method is very useful for analyzing the core. The simplified circuits produce flow graphs that can be analyzed directly or by the mechanical application of Mason's Rule[1].

THE DPI/SFG METHODOLOGY

An earlier paper presented the DPI/SFG methodology as a useful general circuit analysis technique able to handle feedback and the inclusion of cells while accounting for loading effects at input and output nodes of these blocks.[2] This is done by breaking the signals into primitive components of nodal voltages: short-circuit currents and nodal driving-point impedances. A node voltage in this decomposition is:

$$V_j = ISC_j \times Z_j \qquad (2)$$

where ISC_j is the current flowing into a short circuit at the jth node due to adjacent node voltages, and Z_j the reciprocal of the sum of the admittances attached to this node, is the driving-point impedance. That is,

$$ISC_j = SUM_k\{gm_{jk} \times V_k\} \qquad (3a)$$

where by superposition, the component to ISC_j from node k is evaluated with all other node voltages set to zero, and

$$Z_j = 1/SUM_k\{Y_{jk}\} \qquad (3b)$$

Eq. 3a states that each node in the circuit can contribute to the jth node's short-circuit current through a coupling element, the transconductance gm_{jk}. Eq. 3b states that the relevant nodal impedance at the jth node is due to the parallel combination of all admittances attached to this node. These equations are a direct consequence of applying the driving-point impedance technique with auxiliary voltage sources at each node.[2,3] These equations provide the circuit relations needed to produce a signal-flow graph. Once the graph is produced, algebra is peformed on the graph to evaluate transfer functions from source to output.The standard analysis procedure for circuits with active elements is to first create an equivalent small-signal circuit substituting a small-signal model for the transistors. Power supplies become ac grounds. Then comes a system of equations derived from node and loop laws using the unknown state variables of node voltages and loop currents. Substitution or matrix algebra solves the equations.

The DPI/SFG methodology, however, bypasses mosts of these steps and uses Eq. 3a and 3b to produce a signal-flow graph, from which all circuit relations are found.

Consider a simple example using a bipolar transistor *(Fig. 2a)*. The transistor can be modeled with an input impedance, h_{ie}; an output conductance, h_{oe}; and a transconductance element, $gm = \alpha/r_e$, that couples input voltages to produce an output current *(Fig. 2b)*. Instead of drawing a new circuit, the engineer can mentally substitute these attributes into a flow graph defined by Eq. 3a, Eq. 3b, and Eq. 2 as shown below. Higher-order models can be incorporated into the analysis in an identical fashion.

Imagine a short applied to node 1 of the circuit *(Fig. 2a again)*. The current out of this node due to the source V_i through G_s (or $1/R_s$) is:

$$ISC_1 = V_i \times G_s \qquad (4a)$$

and the nodal driving-point impedance (with node 2 held at ground) is:

$$Z_1 = 1/(G_s + 1/h_{ie}) \qquad (4b)$$

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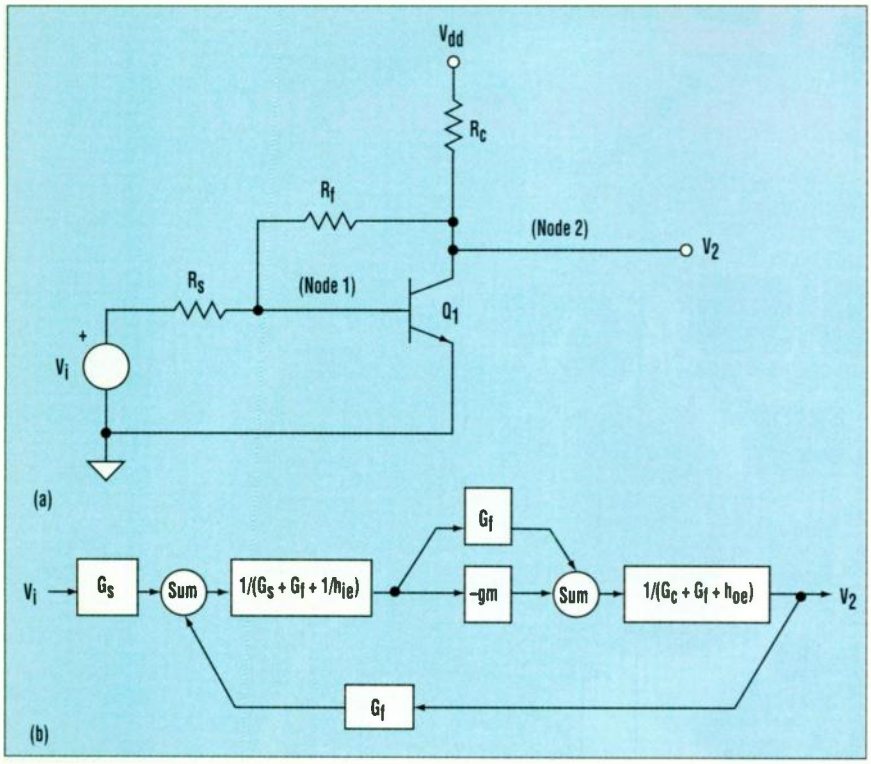


3 When a feedback resistor, R_f is added to the amplifier (a), the transconductance G_f must be included in the nodal driving-point impedances (b).

Similarly, node 2 produces:

$$ISC_2 = -V_1 \times gm \qquad (5a)$$

and

$$Z_2 = 1/(G_c + h_{oe}) \qquad (5b)$$

These two sets of equations are in a particularly nice form to generate the signal-flow graph *(Fig. 2c)*.

A flow graph is a directed net with signals flowing in the direction of the arrows. The relation expressed in Eq. 4a is depicted as the arrow out of the first block at the left side of the diagram. The input to a block is multiplied by the block's contents in flow-graph representation to produce the output.

In this case, the signal source, V_i is multiplied by G_s to produce ISC_1. This signal becomes the input to the next block, which represents Eq. 4b, and produces the voltage at node 1 as defined by the product of the node's short-circuit current and driving-point impedance, $ISC_1 \times DPI_1$ (Eq. 2). Voltage 'V_1 is the input to the next block, which represents Eq. 5a, and is followed by Eq. 5b. The final output is V_2, which is the circuit's desired output voltage.

Graphical algebra is used to find the transfer functions from a source point to an output point. In this case, the output voltage V_2 is the cumulative product of the blocks from input to output:

Equation 6 (see equation listing 1)

The s parameter is needed because Eq. 6 is derived in the transform Laplace space.

A Single-Stage Example

Adding a feedback element to this simple circuit produces a single-stage feedback amplifier *(Fig. 3a)*. Two factors complicate the circuit's flow graph: There are two new current paths, $V_1 \times G_f$ and $V_2 \times G_f$, which account for the additional component of short-circuit current to the nodes, and the DPI blocks now include the term G_f, which accounts for loading at the nodes due to the feedback element *(Fig. 3b)*. The graph now has a loop showing that a fraction of the signal is being fed back, creating a self-modifying feedback system.

Using graph algebra, the complete input/output transfer function at the collector with no approximations beyond those contained in the transistor model is:

Equation 7 (see equation listing 1)

Comparing Eq. 7 to Eq. 1, you can see that the numerator is the gain factor, now renamed A_{og}. This factor is found by opening the loop in the flow graph and finding the resulting transfer function. This is where the open-loop gain, A_{ol}, is seen to be incomplete in Eq. 1. Instead, the open-graph gain, A_{og}, is needed and is easily obtained from the graph:

Equation 8 (see equation listing 1)

Multiplying the term subtracted from 1 in the denominator of Eq. 7 by G_s/G_s, completes the factor A_{og} with the remainer now identified as the feedback factor, f:

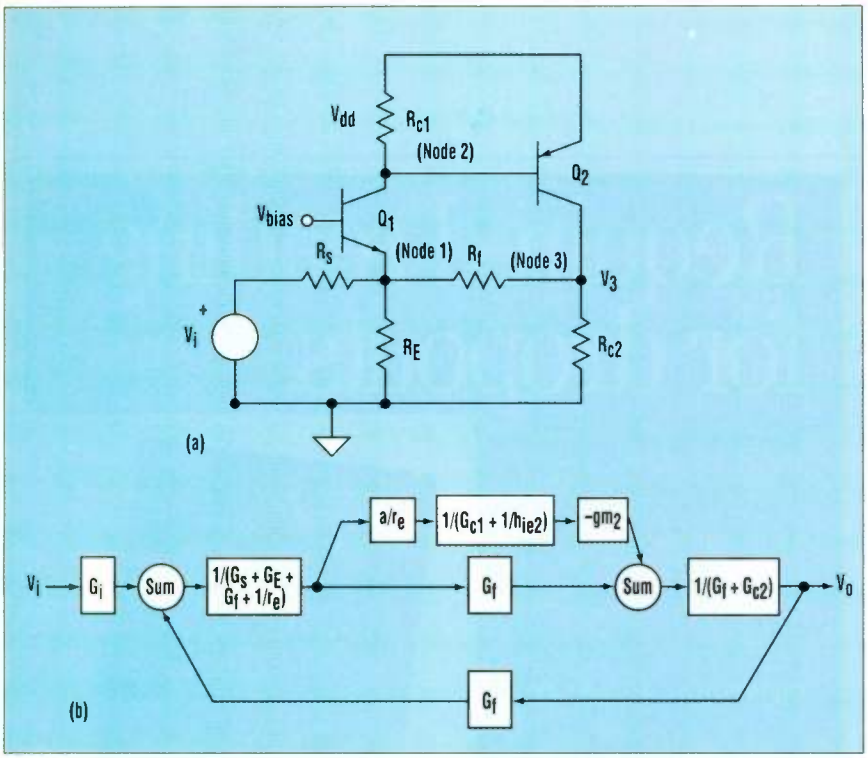
$$f = G_f/G_s \qquad (9)$$

This factor modifies the output voltage V_2 to an equivalent input-referred version of the output voltage when viewed as a drive source.

To summarize the analysis to this point, the DPI/SFG technique has produced a flow graph directly extracted from the circuit. The flow graph is an algebraic representation of the circuit relations containing only those approximations used in the modeling of the circuit elements. Operations on the flow graph produced the system transfer function directly with no additional approximations.

The result (Eq. 7) contains loading effects of the feedback element explicitly. Finally, comparing Eq. 7 to the transfer function obtained from ideal blocks identified equivalent factors: a gain factor A_{og} found by opening the graph loop (rather than opening the circuit loop) and a feedback factor, f, which is the ratio of the feedback admittance to the source admittance.

These results are completely general. Replacing the BJT with an MOS transistor in the example circuit changes some block values due to differences in device model parameters. As a result, Eq. 7 changes also. The



4 A three-node feedback circuit provides a larger open-graph gain than the two-node amplifier and comes closer to meeting the desired system gain.

appropriate blocks in the flow graph are also modified, but not the form of the graph itself nor of the transfer function. The same is true if the BJT is replaced with a different BJT, an op amp, or a vacuum tube.

This illustrates the utility and universality of the methodology. Adding nodes, however, does complicate the algebra, but it remains straightforward. Additionally, because the transconductances and DPIs are in the Laplace space, the algebra is in a form suitable for insertion into computer programs such as MatLab for analysis on the complex plane.

A Design Example

As noted, a well designed feedback system is defined by the properties of the passive components in the feedback factor and not by those of the amplifier. The first design example uses the circuit in Fig. 3a. It is designed to have a feedback factor of 0.2 and the results are compared to the ideal behavior for the voltage transfer function of -1/f = -5.

The first step is to obtain model parameters. The bipolar transconductance is a well-defined parameter due to the exponential dependence of the emitter current on the base-emitter voltage. For a 1-mA emitter current, the emitter resistance is:

$$r_e = kT/(q \times I_E)$$
$$= 0.026/I_E = 26\ \Omega \qquad (10)$$

and the transconductance is:

$$gm = \alpha/r_e \approx 3.85\ \text{mMhos} \qquad (11)$$

The input impdeance, h_{ie}, is:

$$h_{ie} = (\beta+1) \times r_e \qquad (12)$$

Assuming a transistor similar to the popular 2N2222 with a current gain, β, ranging between 100 and 300 ($\alpha \approx 1$) and h_{oe} approximately 0, the range for h_{ie} is:

$$2600 < h_{ie} < 7800\ \Omega$$

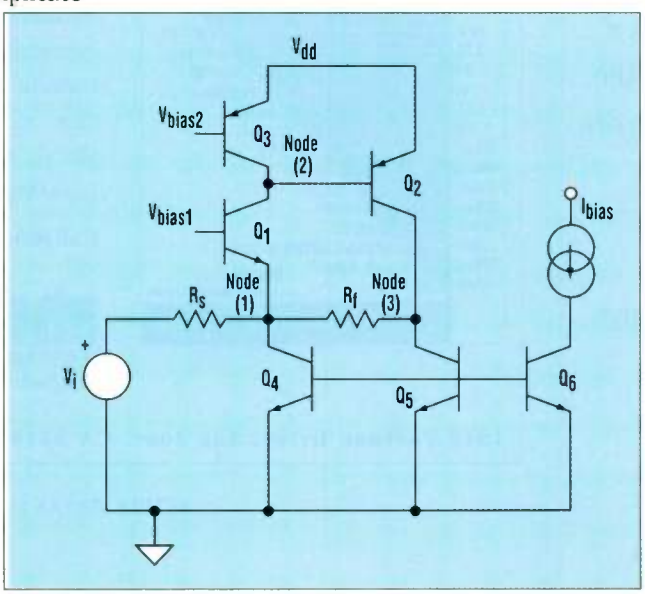
And for V_{CC} = 5 V, R_c must be approximately 2500 Ω for V_O to be 2.5 V.

Resistances R_s and R_f are needed to complete the design. To calculate them easily, two approximations can be made in Eq. 8. G_f can be dropped in the factor (G_f - gm), and h_{oe} can be ignored in the last factor. Next, the design objective says that the feedback conductance will be set at 0.2 times the value of the source conductance. So substituting $G_f = 0.2 \times G_s$ into the simplified Eq. 8 and rewriting it in terms of R_s gives:

Equation 13 (see equation listing 1)

Using h_{ie} = 2600 and R_c = 2500 Ω,

Equation 13a (see equation listing 1)



5 Substituting active loads in the circuit of Figure 4 increases R_{c2} to the megohm range. The result is a system gain within 1% of the target figure.

The peak A_{og} is 40.86 and occurs when R_s is approximately 1250 Ω, which makes R_f = 6250 Ω. This result shows that G_f is much less that gm, confirming the decision to drop G_f from the factor in Eq 8.

Inserting A_{og} and the design feedback factor of 0.2 into Eq. 1 (remembering that A_{ol} is now A_{og}), gives the system gain:

Equation 14 (see equation listing 1)

This value is 11% off of the desired value of -5 (= -1/f), and it will vary with h_{ie}. The problem is that A_{og} is not high enough for a good design that is defined by the

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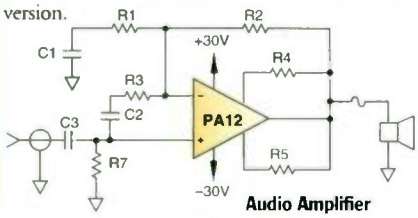

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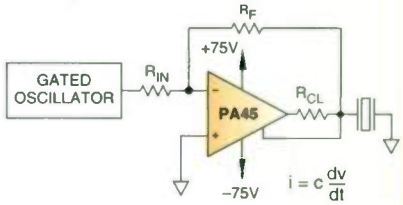

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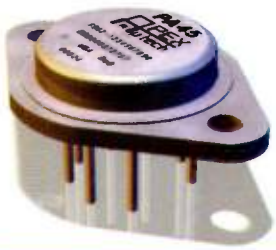

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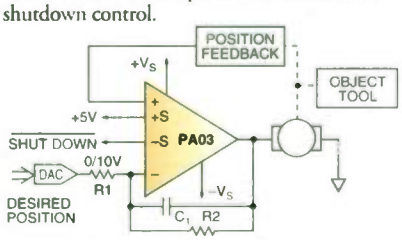

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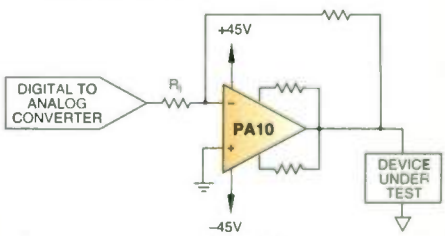

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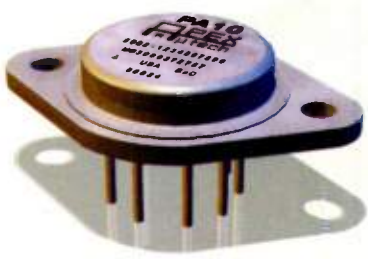

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feedback factor and that is not sensitive to device parameters. If these values are used to calculate $A_{ol,\,ol} = 48$ and H = 4.75. The higher amplifier gain predicted is incorrect due to the effect of the feedback element of the nodal impedance.

Generalizing a bit, the transfer function $H_2(s)$ of node 2 (Fig. 3a again) due to the input signal is expressible in the notation of Eq. 3a and Eq. 3b as:

Equation 15 (see equation listing 1)

As a result,

$$A_{og} = gm_{a1} \times Z_1 \times gm_{12} \times Z_2 \qquad (16)$$

and

$$f = gm_{21}/gm_{a1} \qquad (17)$$

where gm_{a1} is the transconductance coupling of signal source "a" to node 1, gm_{21} that from node 2 to node 1 and so forth.

These results are completely general and valid for all two-node, single input circuits, with no approximations at this point.

Adding Complexity

The second example is a circuit with three internal nodes *(Fig. 4a)*. The flow graph shown is specific to the circuit and not in the universal notation of Eq. 15 *(Fig. 4b)*. Note that some transconductance elements are zero and so are not shown: Node 2 does not couple to node 1 making $gm_{21} = 0$, and node 3 does not couple to node 2 making $gm_{32} = 0$. Ignoring h_{oe} in the transistors to simplify the algebra, the open-graph gain and feedback factor to V_3 are:

Equation 18 (see equation listing 1)

$$f = G_f/G_s \qquad (18b)$$

Sustituting Eq. 18a and Eq. 18b in equation 1 gives the complete transfer function to node 3. This relationship is reduces to the ratio $-R_f/R_s$ if $A_{og} \times f$ is large.

At this point, additional terms can be dropped to simplify the relationship:

Equation 19 (see equation listing 1)

Note that this process produces the transfer functions directly and easily. It's also a simple way to derive the feedback factor and the open-graph gain relationships without approximations beyond those included in the transistor models. Loading effects of the feedback element at both ports are included. Once the complete transfer function is obtained, simplifying approximations are made on the algebra rather than on

EQUATION LISTING 1

$$H(s) = V_2(s) / V_1(s)$$

$$H(s) = G_s \times \left[\frac{1}{\left(G_s + \frac{1}{h_{ie}}\right)}\right] \times (-gm) \times \left[\frac{1}{(G_c + h_{oe})}\right] \qquad (6)$$

$$H(s) = \left[\frac{G_s}{\left(G_s + G_f + \frac{1}{h_{ie}}\right)}\right] \times \frac{(-gm + G_f)/(G_c + G_f + h_{oe})}{1 - \left[\frac{G_f}{\left(G_s + G_f + \frac{1}{h_{ie}}\right)}\right] \times \left[\frac{(-gm + G_f)}{(G_c + G_f + h_{oe})}\right]} \qquad (7)$$

$$A_{og} = \left[\frac{G_s}{\left(G_s + G_f + \frac{1}{h_{ie}}\right)}\right] \times \left[\frac{(-gm + G_f)}{(G_c + G_f + h_{oe})}\right] \qquad (8)$$

$$A_{og} = \left[\frac{h_{ie}}{R_s + (1.2)(h_{ie})}\right] \times (-gm) \times \left[\frac{5R_cR_s}{(5R_s) + R_s}\right] \qquad (13)$$

$$A_{og} = \left[\frac{2600}{R_s + (1.2)(2600)}\right] \times (-1/26) \times \left[\frac{(5)(2500)R_s}{(5R_s) + 2500}\right] \qquad (13a)$$

$$H = \frac{-40.86}{1 + (40.86 \times 0.2)} = -4.45 \qquad (14)$$

$$H_2(s) = \frac{(gm_{a1})\,Z_1\,(gm_{12})\,Z_2}{1 - (gm_{12})\,Z_1\,(gm_{21})\,Z_2} = \frac{A_{og}}{1 - (f \times A_{og})} \qquad (15)$$

$$A_{og} = \left[\frac{G_s}{G_s + G_c + G_f + \frac{1}{r_e}}\right] \times \frac{\left[G_f - \frac{(gm_2)\frac{a}{r_e}}{G_{e1} + \frac{1}{h_{ie2}}}\right]}{G_f + G_{e2}} \qquad (18a)$$

$$A_{og} = G_s \times \frac{\left[\frac{-gm_2}{G_{e1} + \left(\frac{1}{h_{ie2}}\right)}\right]}{(G_f + G_{e2})} \qquad (19)$$

$$\left(\frac{1}{R_s}\right) \times \left(\frac{R_{e1} + h_{ie2}}{R_{e1} + h_{ie2}}\right) \times (gm_2) \times \left(\frac{R_f \times R_{e2}}{R_f + R_{e2}}\right)$$

the circuit. Some terms can be dropped after considering their relative weight independent of their functions in the circuit.

In this second example, the feedback factor is again 0.2. To simplify the discussion, 1-mA emitter-bias currents will be used for both BJT devices, making the transconductances 3.85 mMhos.

R_{c1} now develops a voltage V_{be} across it. Assuming that to be 0.7 V makes R_{c1} = 700 Ω.

To have dc operating points of 2.5 V at nodes 1 and 2, R_E and R_{c2} must be 2500 Ω. The design task is reduced to finding a suitable value for R_s and making $R_f = 5 \times R_s$, to create the feedback factor of 0.2.

The process starts again with the equation for A_{og}, Eq. 18a. First, replace G_f with $0.2 \times G_s$ and set about maximizing A_{og}. Since $1/r_e$ dominates the denominator in the first bracketed factor, everything but the $1/r_e$ term can be dropped. Note also that G_s should be less than about $0.1/r_e$. With the transistor current gain, β, greater than 100, α in the second bracket can be set to 1. In the numerator of the second bracket, G_f is much smaller than gm and so can be dropped.

The relation is now reduced to:

Equation 20 (see equation listing 2)

Thus, making R_s as small as possible will maximize A_{og}. But the lower limit on R_s is defined by the need to make it large compared to r_e. So R_s is set to 260 Ω, and R_f becomes 1300 Ω, yielding:

$$A_{og} \approx -69.8 \qquad (21)$$

and

$$A \approx -69.8/(1+69.8\times0.2) = -4.66 \qquad (22)$$

This is off from the desired gain of -5 by 6.8%. The one-transistor circuit of example 1 was off by 11%, so increasing the magnitude of the open-graph gain from about 40 to about 70 improved the desired gain by a few percent.

The designer can now examine the equations for ways to improve the results. Clearly the larger the open-graph gain the better the result. The problem lies in the impedance required to meet the dc conditions on the circuit. Increasing R_{c2} while maintaining the correct bias level would increase the gain needed. This can be done by using active loads. An increase in R_{c2} from 2500 Ω to the megohm region is easily accomplished by using current-mirror biasing. Also, the factor showing the parallel impedance of R_{c1} with h_{ie2} can be improved by using an active load.

These changes require some circuit modifications *(Fig. 5)*. The open-graph gain now becomes:

$$A_{og} \approx -[1/R_s)]\times r_e(\alpha/r_e)\times h_{ie2}\times gm_2\times R_f \qquad (23)$$
$$= -(\beta+1)\times R_f/R_s$$
$$\approx -505$$

and

Equation 24 (see equation listing 2)

The big increase in A_{og} has improved the gain function so that it is off by only 1% from the target. The limiting factor in Eq. 24 is the current gain, β. Substituting active loads for the collector resistors created high, unloaded amplifier gains. But the loading effect of R_f at the output node does not allow high open-loop gains, so this loading must be considered.

If a 1% worst-case transfer function is acceptible, the modified circuit is a useful feedback system. The result can be improved further by using transistors with higher current gain. Additionally, a Darlington configuration would boost β considerably, improving A_{og} by two orders of magnitude and creating a stabilized overall gain within 0.01% of the ideal result of 1/f. □

EQUATION LISTING 2

$$A_{og}(s) = \frac{(G_s r_e)\left[\frac{(-gm_2)\left(\frac{1}{r_e}\right)}{G_{c1}+\left(\frac{1}{h_{ie2}}\right)}\right]}{[(0.2)G_s]+G_{c2}} = \left[\frac{(-gm_2)(h_{ie2})(R_{c1})}{(R_{c1}+h_{ie2})}\right]\times\left[\frac{(R_{c2})(5)}{(R_{c2}+5R_s)}\right] \qquad (20)$$

$$= \left(-\frac{1}{26}\right)\left[\frac{(700)(2600)}{(700+2600)}\right]\times\left[\frac{(2500)(5)}{(2500+5R_s)}\right] = \frac{-265{,}200}{2500+5R_s}$$

$$H = \frac{-(\beta+1)\left(\frac{R_f}{R_s}\right)}{1+\left[(\beta+1)\left(\frac{R_f}{R_s}\right)\left(\frac{R_s}{R_f}\right)\right]} = \frac{-(\beta+1)\left(\frac{R_f}{R_s}\right)}{1+(\beta+1)} \qquad (24)$$

$$= -\left(\frac{R_f}{R_s}\right)\left(\frac{\beta+1}{\beta+2}\right) = \frac{(-5\times101)}{102} = \frac{505}{102} = 4.95$$

References:

1. See, for example, Chirlian, P.M., *Analysis and design of Electronic Circuits*, McGraw-Hill Book company, NY, 1965.
2. Ochoa, Agustin, A Systematic Approach to the Analysis of General and Feedback Circuits and Systems Using Signal-Flow Graphs and Driving-Point Impedance, to be published.
3. Kelly, R.D., Electronic circuit analysis and design by driving-point impedance techniques, IEEE Trans. on Education, Vol. E-13 No. 3, Sept. 1970.

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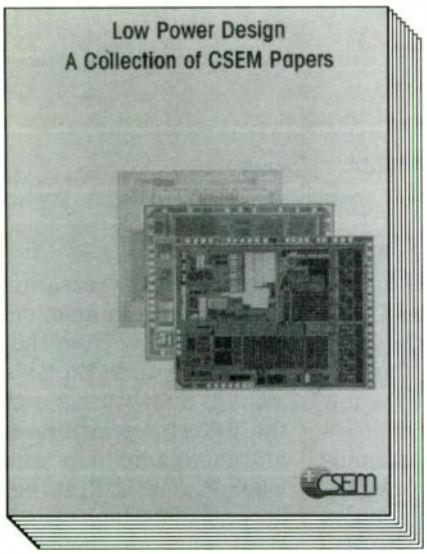

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LCD-Bias Supplies: Here's Some Tips For Turning Out Successful Designs

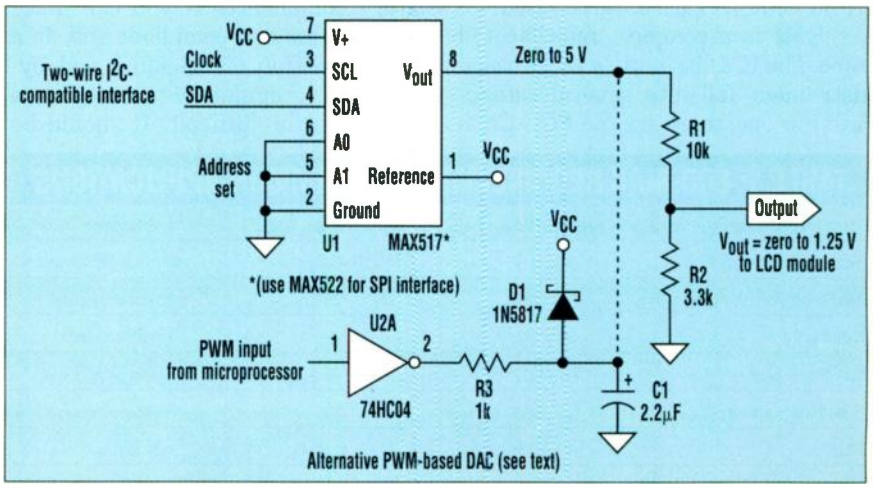
Don't Despair: You CAN Design LCD-Bias Circuits That Do Their Job While Avoiding Problems With EMI Compliance And Supply Sequencing.

JOHN WETTROTH
Maxim Integrated Products

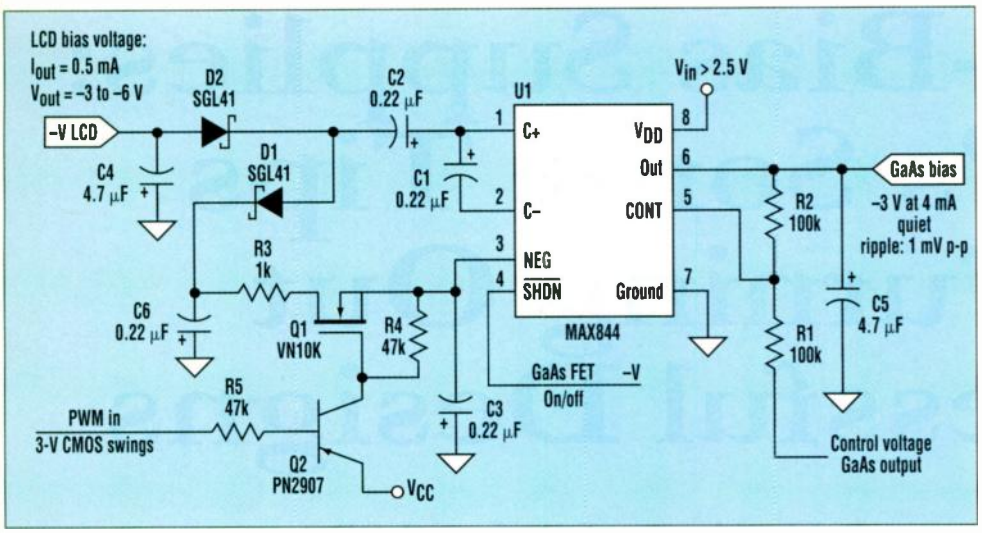
Liquid-crystal displays (LCDs) are the low-power display of choice for today's notebook computers, cellular telephones, and pagers. These displays almost always require adjustable bias. This bias voltage is usually outside the value of typical logic-supply rails, ranging from -5 V for small graphic pagers to æ30 V for notebook displays. And to compensate for temperature and viewing angle, the bias must be made adjustable over a range of about 3:1.

Analog engineers have received little help in terms of articles and application notes about designing LCD-bias supplies for displays that aren't for notebook computers. This article seeks to fill that gap by offering some background on the drive requirements for LCDs, and some general guidance for designing bias circuits that are small, quiet, and efficient. Though the example circuits are illustrated with specific part numbers and component values, the circuits are intended as examples to be modified according to the needs of specific applications.

LCD applications generally fall into three categories: Text modules, smaller displays (–10-V bias or less), and large displays *(see table 1)*. The table illustrates some common applications and their LCD-bias requirements. In most cases, the required bias voltage is negative. In these systems, the negative voltage requirement (V_{LCD}) is lessened by referencing the required bias ($V_{CC} - V_{LCD}$) to the positive rail. In the case of 5-V text modules, a compromise is often made that enables them to operate without a negative supply. Modules running from 3.3 V typically require a few negative volts. Dropping V_{CC} from 5 V to 3.3 V usually calls for an increase in V_{LCD} to maintain the same ($V_{CC} - V_{LCD}$) bias. The basic physics behind this are easily explained *(see "Why LCDs Require Adjustable High Voltages," p. 62)*.



1 Commodity text modules require an adjustable source from 0.4 to 1.25 V. A DAC or filtered pulse-width- modulated DAC can be scaled to obtain these voltages.



2 Cellular phones with GaAs FET power amplifiers require negative gate bias. This bias generator also can be enlisted to provide LCD-bias voltages.

Lately, manufacturers have begun offering LCD modules that include the bias supply. These "single-supply" modules may be convenient, but an external supply provides lower cost, greater flexibility, and higher efficiency—especially in high-volume or low-power applications.

Before delving into the circuits for generating LCD bias, one should have in mind several global constraints and trade-offs. These are the issues associated with electromagnetic interference (EMI), adjustment method, and power-supply sequencing. With the proliferation of wireless equipment, EMI has become especially important. Your pager must not interfere with your cellular phone (or anyone else's), and your notebook computer must not fail to support a GPS PCMCIA card as advertised.

EMI is a complex, multifaceted topic. The EMI issues in a LCD-based instrument fall into several categories. For one, there are the FCC Class A or B regulations. Class A limits are for industrial or office equipment and are relatively easy to meet. Class B limits are for items that may be used in the home and are quite stringent. The digital interfaces, CPU, and main power supply are the dominant factors in meeting Class B limits. The EMI problems that are generally bigger headaches are associated with self-compliance issues. These are EMI problems where one portion of the circuit interferes with the operation of another portion. Noise must be kept out of audio, wireless, and sensitive analog circuits. This can be especially difficult in systems like notebook computers that support PCMCIA. Today, almost any function can be found on a PCMCIA card.

The fixes for self-compliance are generally the same as those for regulatory compliance. If you can make your system self-compliant and do a reasonable job of shielding and bypassing, regulatory compliance should not be difficult. It should be remembered that the LCD-bias supply generally involves a low-power switching supply of some kind that will produce EMI. Care should be taken in design, layout, and shielding to minimize the impact of the bias supply on compliance. One specific issue that is commonly overlooked arises because the bias supply is often located close to the display. As a result, the display viewing area creates a large port from which radiated EMI can escape. A switching power supply operating at 100 kHz with fast rising and falling edges will generate EMI harmonics into the low-megahertz range. The LCD-bias supply would be better located near the main supply with input and output bypassing of circuitry leaving the area of the main supply. Additional bypassing should be installed near the display to minimize radiation and to reduce ac impedance along the trace path.

In wireless systems, the primary self-interference problems are typically manifested as a loss in receiver sensitivity. This is because the noise generated in the system will raise the minimum discernible signal level that the system can receive reliably. A similar reduction in dynamic range occurs in sensitive analog equipment. The key parameter for receivers and analog data-acquisition systems is signal-to-noise ratio. If you add noise, you reduce this ratio as well as dynamic range.

There are two interference pathways for EMI generated by switching supplies: Radiated emissions within the box, and conducted emissions that contaminate V_{CC} on the input supply. Radiated emissions are generally controlled with mechanical measures such as shielding and careful layout. The bias supply should be located away from sensitive circuits. If this isn't possible, it should be shielded and well-grounded. In supplies that use inductors, it's prudent to use devices with a closed magnetic path such as toroids, pot cores, or shielded inductors. The power level and peak currents should be limited to what the display requires, with some design margin. Higher currents produce larger fields. At the extreme, saturated induc-

TABLE 1: LCD BIAS REQUIREMENT FOR COMMON APPLICATIONS

Application	Typical Pixels	Typical Bias Reg.	Notes
Text module—low end	80 × 16	+0.5	Narrow temp range
Text module—high end	80 × 16	-5	Wide temp range
Cell phone	96 × 32	-5	Small/efficient
Graphic pager	128 × 32	-6	Very small/efficient
Small instrument	128 × 64	-9	Wide temp range
PDA	160 × 320	-18	Small
Large instrument	320 × 240	-20	Wide temp range
Notebook PC	640 × 480	-24 or +30	High current generally

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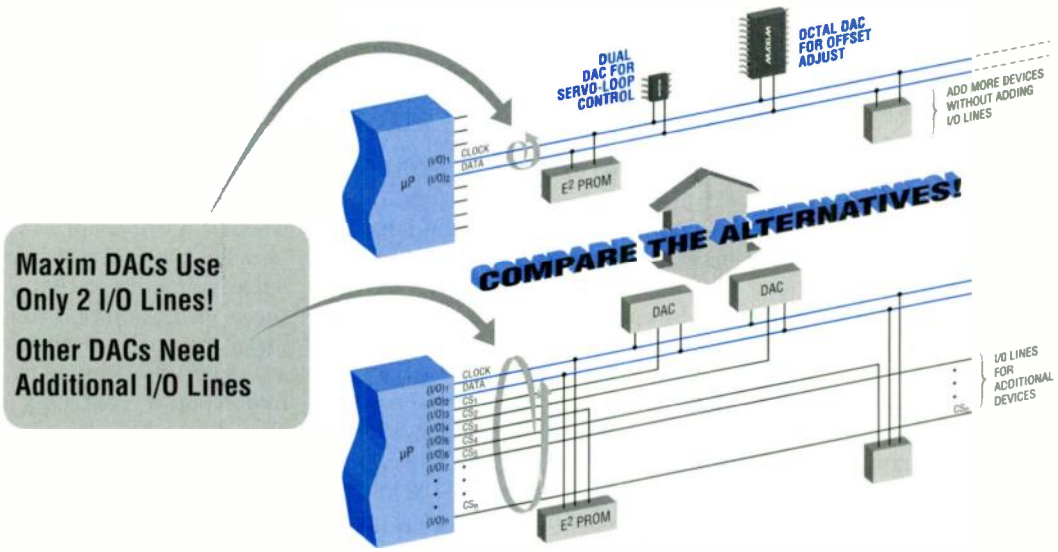

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tors will produce tremendous amounts of EMI and harmonic content.

Conducted emissions are controlled by isolating the input supply with a filter network that includes a high-quality capacitor and a ferrite bead that provides loss at frequencies above 400 kHz. This frequency limit is significant for several reasons. First, it's above the frequency of most switching power supplies. Second, it's below the common IF frequency of 455 kHz used in wireless equipment. It's also below the 450-kHz limit at which FCC conducted-emissions testing begins. If the supplies within a system can be isolated from the system's own input, then overall compliance at the system level will be much easier. When designing input-filter networks, remember that the input current for a switching supply is often many times higher than the output current, especially at startup. In general, you should incorporate EMI constraints early in the design cycle because they are difficult to add later on.

Most LCD-bias supplies must include a provision for V_{out} adjustment. Only a few systems with a well-controlled ambient-temperature environment or viewing angle can afford to dispense with this feature completely. The display in a gas pump, for example, is exposed to wide variations in temperature but has a relatively fixed viewing angle. Manual adjustments are not practical, so active and automatic temperature correction by a microprocessor might be appropriate in that application.

The simplest means of V_{out} adjustment is use of a potentiometer. The pot's electrical simplicity, however, is generally outweighed by the mechanical headaches it can cause. For most of the circuit examples shown, the option for adjustment with a potentiometer will be obvious. All the circuits and techniques to be discussed offer adjustment by means of software.

There's one class of application, however, that is an exception to the no-pots rule. Consider an interface based on a touch screen in which the contrast is way out of adjustment. It may be impossible to readjust by clicking an appropriate screen icon, because the contrast might be so far out of adjustment that you can't see the icon. In addition to software adjustment, such a system may require an override similar to the "beam finder" on a Tektronix oscilloscope. This might be a "triple click" in the upper right corner, for example, to bring the LCD contrast to mid-scale.

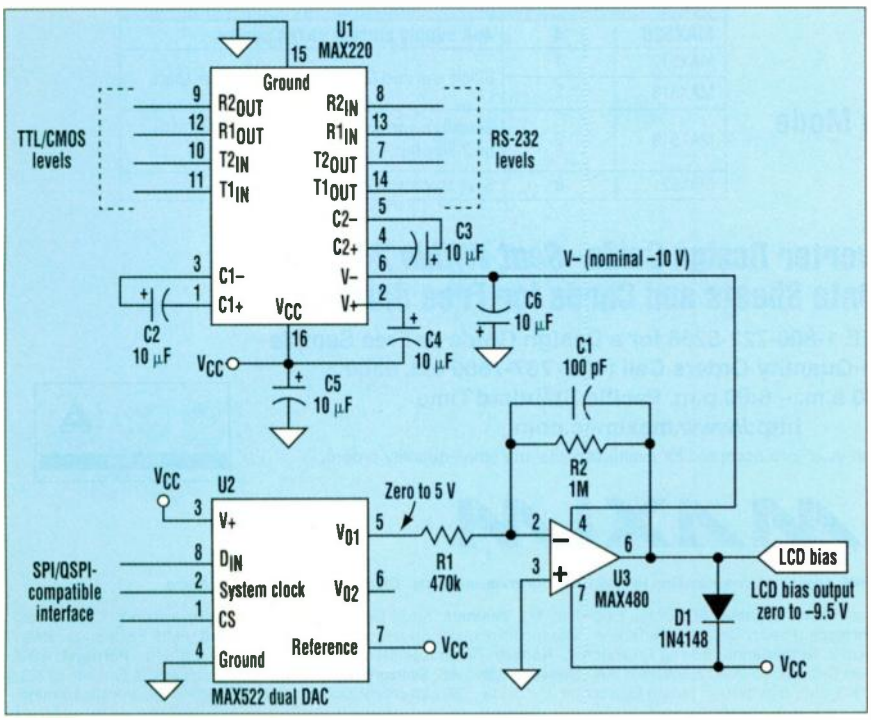
There are several general techniques that can be used for V_{out} adjustment. A negative voltage can be linearly regulated by an op amp that's driven by a digital-to-analog converter (DAC). The DAC can be an IC type or a filtered, pulse-width-modulated logic signal from a microcontroller in the system. This technique is used widely for smaller displays because the currents are low and overall power dissipation is minimal. For larger displays that draw a bit of power, the preferred method is to use switching regulators with DACs setting the reference for the feedback loop. This results in higher efficiencies. There are other techniques as will be seen in the circuit examples.

Another issue related to adjustability is the requirement for an LCD-contrast supply that is jumper-selected between positive and negative output, either when the display is installed or during manufacturing. Remember that most displays require negative bias, but some require positive bias. In many cases, this is a matter of whether the system is to include a passive-matrix color displays or a monochrome display. It's often convenient for a system vendor to offer a monochrome or color version of their system with identical internal circuitry except for the display and a jumper or two. There are two circuits

TABLE 2: CHARACTERISTIC VOLTAGES FOR COMMON MULTIPLEXING SCHEMES*

Order N	V_{ON}/V_{OFF} ratio	V_{LCD} (mV/°C)	$V_{CC}-V_{LCD}$	V_{LCD} (5V system)	V_{LCD} (3V system)
8	1.447	-50	-12	-7	-9
16	1.290	-65	-15.6	-11	-13
32	1.196	-88	-21	-16	-18
64	1.134	-120	-28	-23	-25

*Assumes standard waveforms per definitive paper by Alt and Pleshko—with V_{th} = 2V, T_C = -10mV, and temperature range 0° to 50°C (20% margin).



3 In an instrument with a need for RS-232 communications, raw negative bias voltage can be taken from the RS-232 IC and scaled to the proper level.

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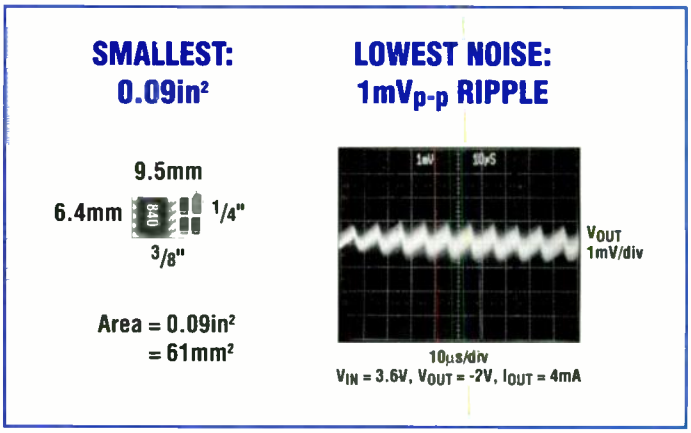

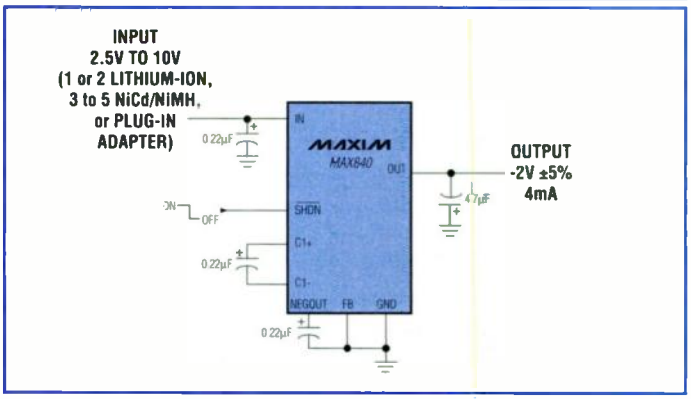

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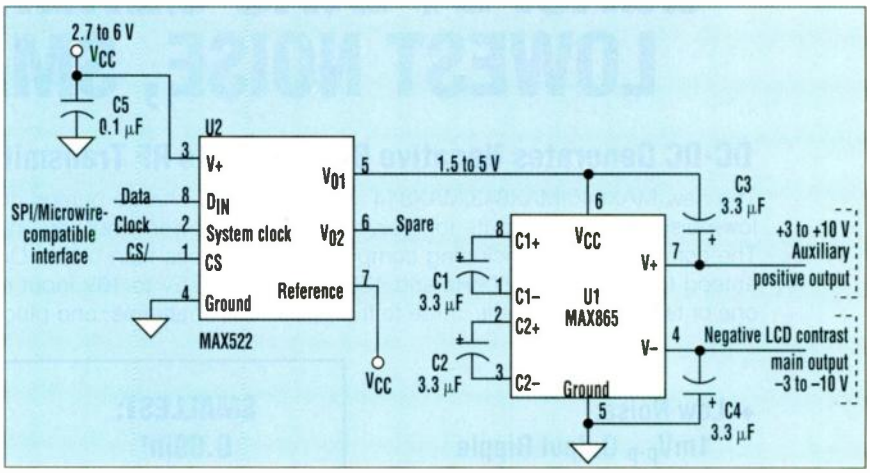
that cover this general requirement which will be discussed later. This option is not generally difficult to allow for and should be considered in the system design of your equipment.

Most displays require some form of power-supply sequencing. The logic supply should be powered-up first, followed by the LCD-contrast supply. This sequence should be reversed on power-down by first removing the bias supply and then removing the logic supply. Some display modules contain internal circuitry to accomplish this sequencing. Often, the correct sequence can only be deduced by a careful reading of the absolute maximum ratings on the display's data sheet.

There are two potential consequences to ignoring these sequencing rules, and neither is very pretty. Dc voltage is the enemy of any LCD. If the contrast bias voltage is present without the logic supply, the ac waveforms will not be generated by the controller, and dc voltage will be applied to the LCD. If these applications are of relatively short duration, their cumulative effect will be a reduction in the display's lifespan. A long-duration application of dc voltage will ruin the display in very short order. The other hazard is latchup of the LCD drivers. For many displays, failure to properly sequence the supplies can put the LCD's row-and-column driver ICs into an SCR-latchup condition that's typically destructive.



4 This clever circuit runs a charge pump directly off the output of a DAC, which inverts and doubles its input supply to create an easily adjustable negative supply.

Power sequencing is simple for most systems. The DAC or setting mechanism should start out at a safe voltage until main V_{CC} is established on the display, and then should be set to the proper bias value. Power-down sequencing also should be addressed. At the very least, the bias supply should be clamped so that it collapses when V_{CC} collapses. An npn switch and a PNP-level shifter with a few resistors can be used to switch a negative LCD supply from a microprocessor's port pin.

For critical applications, there is one scenario that should be considered. What if power is applied to the LCD controller, but it fails to start up and generate the required ac waveforms? In this case, some form of watchdog on the horizontal-scan frequency from the display should be used. A microprocessor supervisor or counter input on a microcontroller can be used to implement this watchdog function.

Handling Small Modules

Turning to applications associated with specific types of equipment, we find two classes of modules for text-only LCDs. The first is a small commodity component that has a usable temperature range of about 10°C to 40°C and requires a positive bias of only 0.5 V. The second type has a usable range of about –10°C to +50°C, and requires a negative bias of about

WHY LCDs REQUIRE ADJUSTABLE HIGH VOLTAGES

The magic of an LCD lies in the fluid it contains, which exhibits a 50%-contrast point (transition voltage) of approximately 2 V rms with a temperature coefficient of 10 mV/°C. Dc voltages cause the fluid to undergo electrolysis and be ruined, so the control voltage must be ac. Higher rms levels produce better contrast.

Very simple displays with only a few segments can include a drive line for each segment (pixel), plus a backplane common to all pixels and be driven with a square wave. Pixels are then turned off by control signals in-phase with the backplane, and turned on by control signals out-of-phase with the backplane. This "direct-drive" scheme becomes unwieldy for all but the simplest displays.

Most LCDs are therefore multiplexed to reduce circuit complexity, pin counts, and interconnects in the display and in the controller. The LCD controller generates complex ac waveforms that produce a high rms voltage for "on" pixels and a lower (but non-zero) rms voltage for "off" pixels. These rms voltages are several times lower than the bias voltage produced by the LCD-contrast supply. Each multiplexing scheme has an "order" or "N ratio," which is the ratio of driven pixels to drive lines. Therefore, N represents efficiency in a general sense. N involves trade-offs: Higher N lowers the ratio of on-pixel to off-pixel voltage, and it increases the ratio of peak to rms voltage *(see table 2)*.

The table offers several insights. The N = 64 case, for example, has a V_{ON}/V_{OFF} ratio of only 13%, and its temperature coefficient corresponds to 0.4%. This means that a temperature change of 30°C would turn an off pixel to on. Much smaller temperature changes, however, are quite noticeable in the display and therefore require active compensation or user adjustment. For N = 8, the improvements in V_{ON}/V_{OFF} ratio and temperature coefficient produce a more stable display at the cost of additional pins and complexity. As a result, for wide-temperature-range displays in which cost is not a primary concern, lower multiplex ratios are more suitable.

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- **No Inductors Needed; Only 4 Small Capacitors**
- **±10mA Output Currents**
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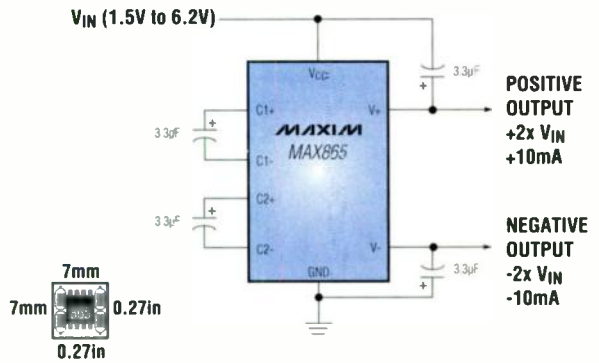

The MAX865 creates split supplies from a single supply for analog circuits, allowing low-cost ground sensing and improved resolution.

PART NUMBER	SWITCHING FREQUENCY (kHz)	RECOMMENDED CAPACITORS (µF)	QUIESCENT INPUT CURRENT (mA)
MAX865	25	3.3	0.6
MAX864	5	33	0.6
MAX864	35	6.8	2.4
MAX864	100	2.2	7
MAX864	200	1	12

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–5 V. The latter bias requirement is similar to that of a small LCD graphics display covered in the next section.

For commodity text modules, you generate the desired adjustment range (zero to 1.25 V) by scaling down a zero-to-5-V signal obtained either from a DAC or by filtering a PWM signal *(Fig. 1)*. A benefit of using the DAC is that it's a quiet dc device and draws less power. The diode is used in the PWM case for crude supply sequencing and to prevent latchup on power-down. It discharges the output capacitor when the main supply is switched off. The DAC approach sidesteps this issue because the DAC's output collapses as V_{CC} falls.

Small Graphics Modules

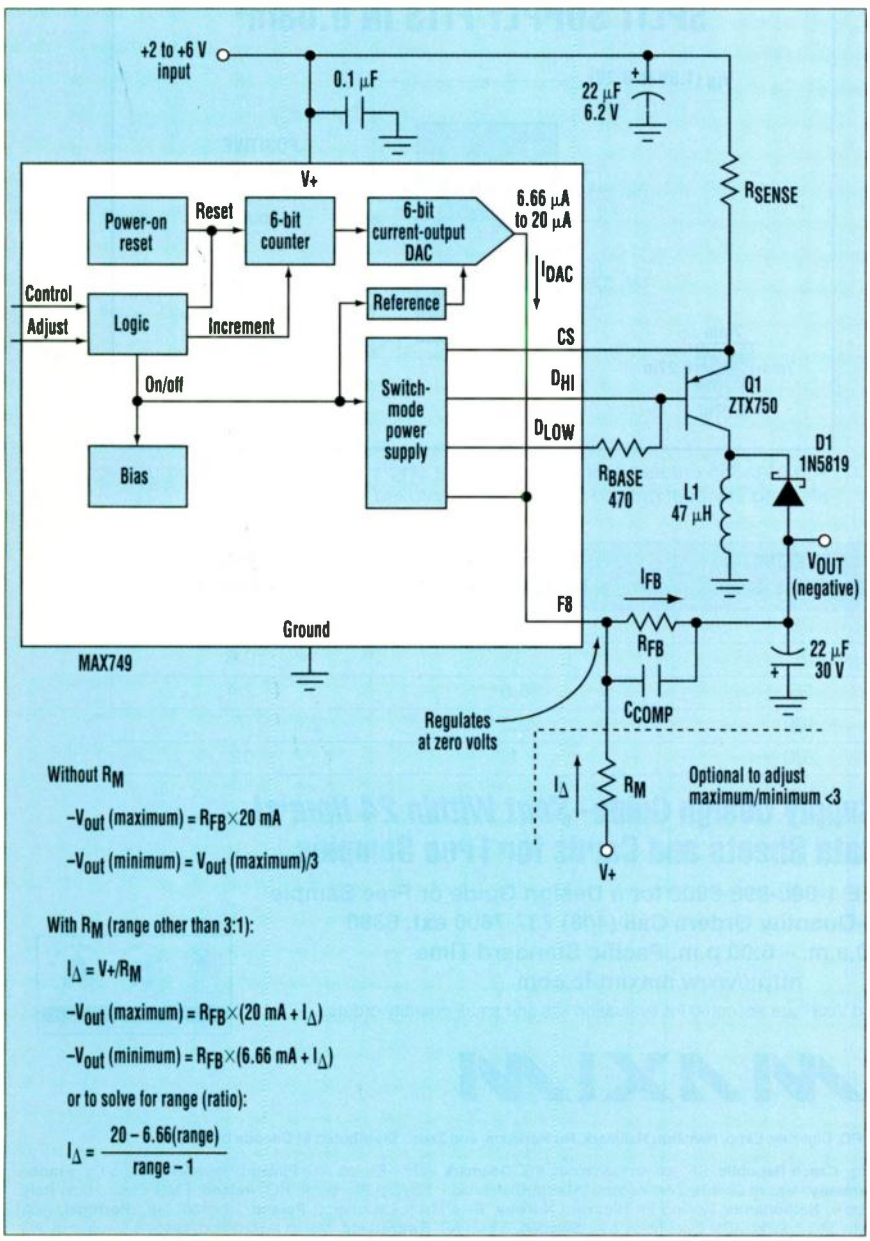
Cellular phones, pagers, and other small instruments represent a class of LCD-bias circuits that are common but not well supported by application-specific ICs. In general, the bias requirement is a voltage between –5 V and –10 V that delivers very low current that is easily met with a capacitive charge pump. The resulting circuit is typically smaller and less costly than an inductor-based switch-mode supply. In some cases, as will be shown, clever design techniques can derive the required bias voltage from other parts of the system.

The bias circuit shown is specific to cellular phones and two-way pagers that incorporate a GaAs FET-based power amplifier in the transmitter *(Fig. 2)*. GaAs FETs require a very quiet negative gate bias. The bias generator in this circuit (IC1) includes a charge-pump voltage inverter and low-noise negative linear regulator that generate negative bias at the main output. A voltage equal to the negative of V_{in} (available at IC1's NEG negative-output pin) is directly usable for some low-voltage displays.

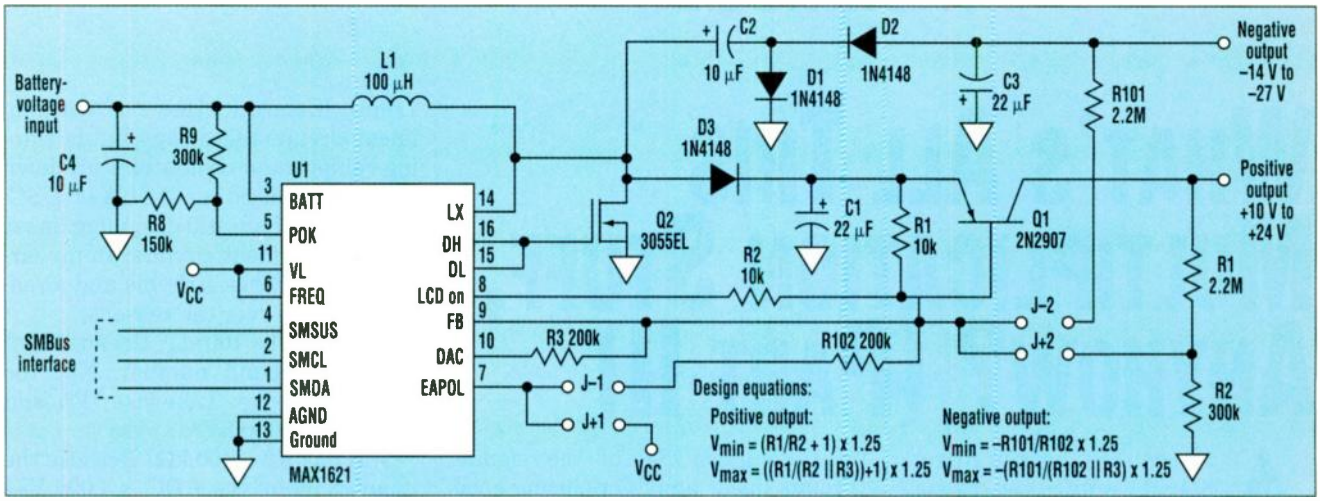
In this particular example and in most others, however, the voltage at NEG is insufficient. The charge-pump output is therefore applied to an external diode-pump doubler that produces an output of –6 V. This charge pump is controlled from a PWM signal from the cellular telephone's microcontroller for adjustment. The PWM varies the output from minus one times the input to minus two times the input by varying the amount of charge the second stage of the charge pump is allowed to transfer. The pump can be operated "wide open," if desired, by eliminating the MOSFET and PWM input. IC1 enables the GaAs FET bias to be turned off while the charge pump remains on, at a power-saving lower frequency, to generate the LCD bias.

A second LCD-bias circuit suitable for small displays with requirements of –5 V to –10 V is suitable for portable instruments that include an RS-232 port *(Fig. 3)*. To ensure the minimum-specified output of ±5 V, most single-supply RS-232 transceivers generate ±10 V internally. The negative charge-pump output can be tapped and amplified with a low-quiescent-current op amp. The IC shown (MAX220) is a low-current version of the original, standard MAX232. You can use the MAX232 if low current is not an issue, but the op amp should remain a low-current type: At high data rates, the current available for external use (from IC1, pin 6) is only about 5 mA.

The last circuit in this category uses an unusual method of adjustment. A low-power DAC can generate the input V_{CC} voltage for a charge pump directly *(Fig. 4)*. IC1 is essentially the charge-pump circuitry from Maxim's MAX232 transceiver, made available in a tiny 8-pin μMAX package. Accepting an input on pin 6, it produces ±2 V_{in} as



5 Capable of generating the high negative voltage required in PDAs and notebook displays, this one-chip solution also contains its own DAC.



6 This single-chip solution is capable of generating positive or negative voltage with a jumper change. Often, the same unit must support both polarities for color and monochrome LCD versions.

separate outputs on pins 7 and 4, forming a simple adjustable power supply. The major limitation is IC1's minimum V_{in} of 1.5 V, which sets the minimum outputs at ±3 V. You can replace the DAC with a PWM signal and passive RC filter followed by an op-amp buffer to maintain reasonable component sizes. Remember the sequencing issues that were covered in the first example for the stored charge of the PWM filter capacitor in this case. A simple diode from the filter capacitor to V_{CC} should be used to discharge the capacitor as V_{CC} falls.

LARGE-DISPLAY SUPPLIES

High-end notebook computers feature a direct-drive TFT LCD, which doesn't require field adjustability by the user. Dual-scan, twisted-nematic displays (DSTNs) are multiplexed and require adjustment by the user for temperature and viewing angle. In many cases, a system such as a notebook computer might be available with either type of display. So they'll often still require an adjustable LCD bias. Notebooks represent a high-volume, mainstream application for which manufacturers have produced single-chip solutions for the LCD-bias requirement.

Such standard ICs fit the majority of notebooks, but they may not be directly suitable for PDAs and other instruments. For these, the designer often needs a different V_{out} range, a lower quiescent current, or some kind of "non-notebook" interface. Two such circuits are presented, along with design equations for modifying the V_{out} range *(Figs. 5 and 6)*. In each case, the switch-mode controller features an external switch and an internal adjustment DAC.

Each circuit is capable of generating the high voltages required in these applications, and each includes simple "hooks" for the V_{out} adjustment. Though convenient, these circuits require an external transistor that makes them less suitable for low-voltage applications. EMI is a major issue for notebook and wireless devices, so the circuit in Figure 6 includes a frequency-select pin that lets you modify the operating frequency or synchronize it to an external source.

The IC in Figure 5 includes a 6-bit DAC and employs pulse-frequency modulation (PFM) to regulate the current-limited negative output. The DAC is incremented on positive edges on the CTRL pin. The edges are generated by a keyboard controller or debounced pushbutton switch. For standard applications, the minimum V_{out} is set at one-third of the maximum by IC1. To increase this range, you can inject current at the FB terminal (a virtual-ground summing junction) by means of RM and V+ as shown. V+ should be a relatively stable voltage. In some cases, V_{CC} may not be directly suitable for this purpose, because the 5 to 10% variations that can occur when, for example, a hard disk spins up, can cause unwelcome changes of contrast in the LCD. Typically, a stable source will be available in the system either as V_{CC} or as a reference.

A jumper-selectable positive or negative bias circuit for notebook LCDs is illustrated *(Fig. 6, again)*. This method is more efficient because the controller IC operates directly from the notebook battery (instead of a regulated 5-V source as in Fig. 5). It also includes a dc-dc converter and DAC, but offers greater flexibility in setting the output polarity, output range, and operating frequency *(Fig. 5, again)*. Though part of a family that includes other types of communication interfaces, this particular IC controls the internal DAC by means of a serial interface now common in notebook computers—the SMBus. Because of its frequency-control input, this circuit also is suitable for wireless applications.

The external switch for both of these notebook supplies can be a bipolar transistor or a FET *(Figs. 5 and 6, again)*. Both ICs can drive either type of switch. At higher currents, the trade-off is between low cost (bipolar transistor) or efficiency (FET). To drive a FET, the designer would tie the two driver outputs (DH and DL) together. To drive a bipolar transistor, it's a matter of connecting one output directly to the base (the one that removes base charge in the off state) and adding a current-limiting resistor in series with the output that turns the transistor on. ED

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WHAT'S ALL THIS MULTIPLICATION STUFF, ANYHOW? (PART II)

As I promised back in August 8, 1991*—YES, you can easily make a 0.02%-accurate analog multiplier, IF you have signals in a limited range. If each of your analog signals runs the range from +5 V to –5 V, it's hard to get enhanced accuracy. But if one of your signals only runs from 5 V to 9 V or 2.5 V to 3.5 V, then it's a lot easier to design improvements. Back in 1991, I got samples of an MPY534KD analog multiplier, rated to 0.5% accuracy. I put them into my trick circuit—and it worked well, with less than 0.02% accuracy. But I always wondered, what if we made the multiplier out of an analog-to-digital converter driving a multiplying digital-to-analog converter—an ADC and an MDAC??

BOB PEASE
OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

It turns out that an ADC plus an MDAC costs about one-third to one-half as much as an analog multiplier, and can provide better accuracy if you are trying to do better than 0.05%. If you are trying to do less accuracy, or more, you have to engineer it. There is nothing simple.

Let's look at the example in Figure 1, using an ADC1241 and a DAC1210. These parts are some of the cheapest grades of 13-bit ADC and 12-bit MDAC. As I said, we can get good accuracy over a *limited range* of V_{in} by running MOST of the signals through linear amplifiers, using good resistors. The output of the multiplier is attenuated by a factor of 31—notice the ratio of R102 to R101. Since these ADCS and DACs have an accuracy better than 0.1%, then the output accuracy is limited mainly by the precision resistors. If you want to buy 1% resistors, that's crummy but can give fair accuracy; if you buy 0.1% or 0.01% metal film or wire-wounds, you can achieve very good accuracy.

NOW, I am not going to worry a lot about the equations. I could have set up a BOX of equations, the same as I did in 1991. BUT, let me EXPLAIN how we ENGINEER the values of the resistors. I don't require fancy equations. I do my whole design on the basis of something I learned at MIT 35 years ago from Assistant Professor Lenny Kleinrock. He's not teaching linear circuits these days, but he's doing complicated computer stuff down somewhere at either UCLA or USC. Meanwhile, I am still designing linear and almost-linear circuits. In my circuit, every R has a rhyme and a reason. Let's go over the reasons.

WHY is R1 = 100 kΩ? Because that is a nice round number. Not too heavy to drive. Likewise, R5 and R101 are 100 kΩ.

WHY is R2 = 400 kΩ? Because the input range of the ADC is 4.096 V—just a bit larger than 4 V, so we need a gain of 4 to get the input signal range of 1 V p-p up to 4 V p-p.

WHY is R3 = 116.695 kΩ? Well, I decided that I want the working input range of V_{in1} to be from exactly 2.50 V to 3.00 V to 3.50 V to 3.51 V. When V_{in1} gets to 3.51 V, the ADC will see 0 V, and cannot respond. But in the range 2.5 V to 3.5 V, V_x will be in the range 0.040 V to 4.040 V, so the output code will still respond. In other words, we have to set the offset properly by using:

$$V_{in1} = 3.51\ V/R1 = 4.096\ V/R3 = 35.1\ \mu A.$$

WHY is R4 = 640 kΩ? Hold off on this question; I'll answer this in a second.

WHY is R5 = 100 kΩ? Same as R1.

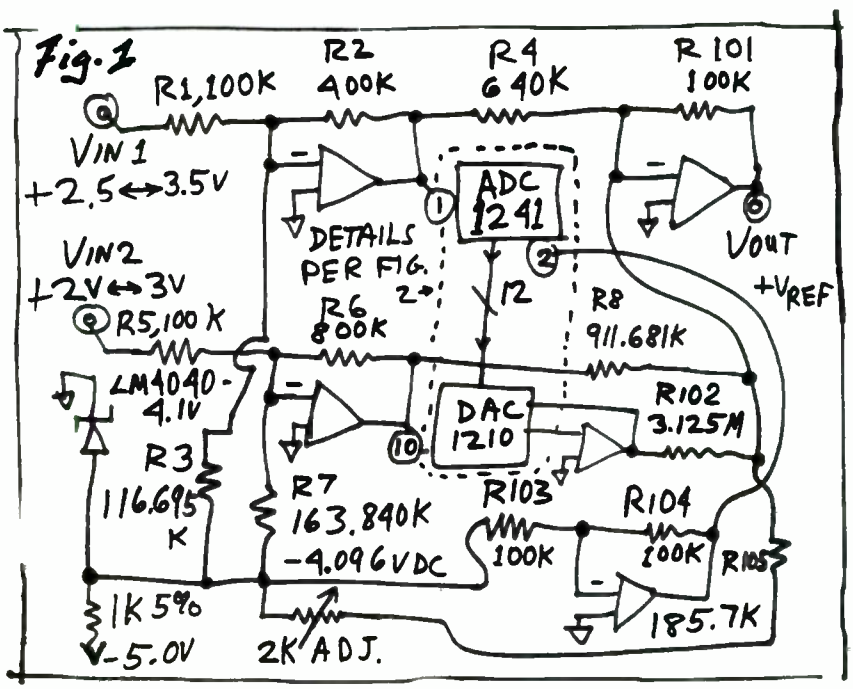

TABLE 1: OUTPUT VOLTAGE OF MDAC (at pin 11) AS A FUNCTION OF Vin1 AND Vin2

		V_{in2} = +3.000 V	V_{in2} = +2.500 V	V_{in2} = +2.000 V
V_{in1}	V_x	V_y = –4.000 V	V_y = 0.000 V	V_y = +4.000 V
+3.510 V	0 mV	0.000 V	0.000 V	0.000 V
+3.500 V	40 mV	+39.0625 mV	0.000 V	–39.0625 mV
+3.000 V	2040 mV	+1.99219 V	0.000 V	–1.99129 V
+2.500 V	4040 mV	+3.94531 V	0.000 V	–3.94531 V

NOTE: V_x is the amplified signal fed into the ADC at pin 1; similarly, V_y is the voltage fed into the MDAC at pin 10. The multiplier may have errors as large as 2 or 3 mV, but these errors will be attenuated by 31 before they get to the output.

WHY is R6 = 800 kΩ? Because we want V_y (the input of the DAC1210 at its pin 10) to cover the broadest possible analog range, from +4 V to –4 V, while V_{in} only covers a 1-V range. So we need a gain of 8. Thus, R6 = 8 × R5 = 800 kΩ.

WHY is R7 = 163.840 kΩ? When V_{in2} is 2.50 V, we want V_y to be 0.000 V. So 2.50 V/100 kΩ = 4.096 V/R7. This defines R7.

WHY is R8 = 911.681 kΩ? Very simple. If you look at every value of V_{in1}, V_{in2}, and V_{out}, you could compute the best value for R8. But you don't have to look everywhere. The easiest place to analyze is according to Table 1: When V_{in1} is 3.51 V, the ADC has all codes OFF, and the MDAC's output is 0 no matter what V_y is. In that case, per Table 1 and Table 2, the gain to V_{out} from V_y must be 0.8775 V/8.000 V, or 0.1096875. Thus, R8 = 911.681 kΩ (the reciprocal of that gain).

Similarly, now let's analyze R4. When V_{in2} is 2.5 V, the gain from V_{in1} to the output is supposed to be 1/0.625. When V_{in2} is 2.5 V, there is ZERO input to the MDAC, so it will have no gain. So to get this gain, we just have to set R4 at 640 kΩ (= 400 kΩ /0.625). If you avoid matrices or fancy computers, it's easy to develop an intuitive feel for this kind of circuit.

How do we find the value of R101 to be 3.125 MΩ? Easy. After we chose R8 to be 911.681 kΩ, that sets the gain for the case when V_{in1} = 3.51 V. Per Table 1, when V_{in1} is at 2.5 V, only R101 = 3.125 MΩ meets the gain requirements. The good news is that 3.125 MΩ = 31.25 × R101, a relatively large ratio. If the output of the MDAC is reasonably accurate, its errors are attenuated or "smallified" by a factor of 31. That's what we are shooting for.

The ADC needs a certain amount of "glue logic" to enable it to convert and then spit out its data to the MDAC, as shown in Figure 2. The MM74HC4060 counter and the gates put out these needed pulses, CS and RD and WR, and an initial calibrate pulse CAL, when power is first turned on. If you want to see how I choreographed these signals, send me a SASE.

Note: One engineer estimated that maybe I had put in more than the minimum necessary amount of glue logic, so if you are going to build 1000 of these, you may be able to simplify that somewhat... This version used one can of 74HC14s and two of 74HC00s.

When we built this little fellow, it worked the first time we powered it up. See the observed data in Table 3—comparable to the Chart of data that we ran back in 1991. The accuracy is quite good. What else can we say?

Another advantage of this scheme is that if you need several channels of signal multiplied by one signal, you may be able to use several MDACs and just one ADC. This could save a lot of space—and money.

WELL, nobody in the WORLD will need this circuit I just designed. But other people may need a similar multiplier, with high accuracy. Or, the concept that multipliers can do useful things. The best, cheapest way is to put most of the signal through linear amplifiers, using inexpensive precision op amps such as LMC6482A or LF411As, and put just the nonlinear part of the signal through the multiplier. If you need to multiply (±5 V) × (±5 V), then R4 and R8 have to become open-circuits, R102 becomes 100 kΩ, and this circuit provides ZERO improvement.

If you have to multiply (±3 V) × (+3 V to +4.5 V), for example, and you need an improvement in accuracy, this can help a lot. I am not arguing you couldn't put in one or two high-resolution ADCs and do the whole thing digitally. But it would cost a lot for the high-resolution ADCs, and it would be a little slower. Keeping most of the signal in the linear domain gets you cheapness and speed.

Speed? I set up this converter with the laziest possible set-up, and high resolution. The conversion rate in this case is

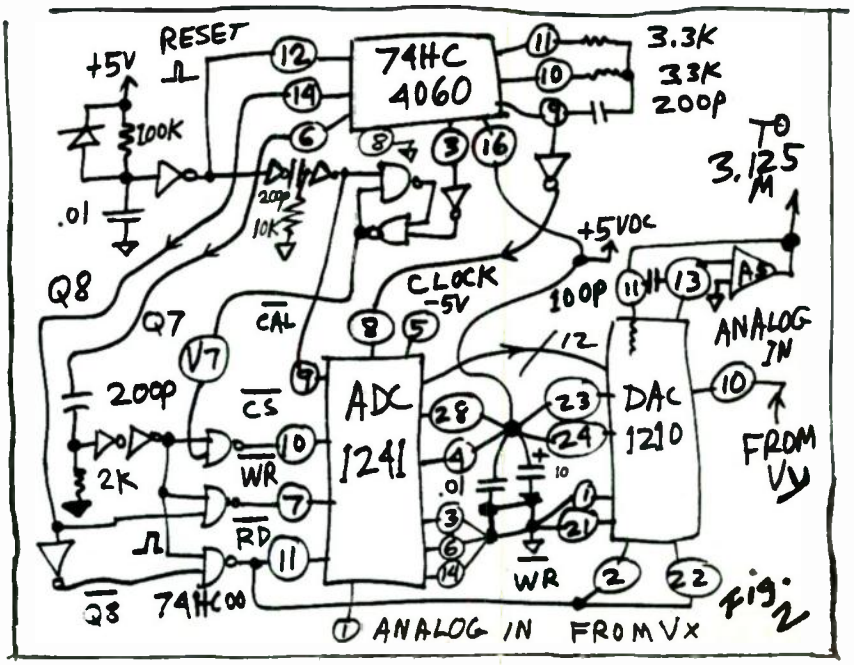

TABLE 2: OUTPUT VOLTAGE AT Vout (THEORETICAL) FOR ALL VALUES OF Vin PER THE EQUATION: Vout = Vin1 × Vin2/4.000 V

	V_{in2}		
V_{in1}	+3.000 V	+2.500 V	+2.000 V
+3.510 V	+2.6325 V	+2.19375 V	+1.7550 V
+3.500 V	+2.6250 V	+2.1875 V	+1.7500 V
+3.000 V	+2.2500 V	+1.8750 V	+1.5000 V
+2.500 V	+1.8750 V	+1.5625 V	+1.2500 V

about 8 kHz, or one update per 120 µsec. The output accuracy is no better than 100 µV, but the resolution is better than 40 µV—WELL below 20 ppm of the output signal. If you figure out that you need accuracy that is merely better than 1 mV, you can get away with a 10-bit ADC and MDAC, and that would save you a lot of pennies. If you can get away with 1% accuracy, you may be able to use cheap 7-bit or 8-bit converters at any imaginable speed. And while fast ADCs are not exactly cheap or low power, if one channel is slow—put that into the ADC, and the MDAC can be pretty quick—faster than a MegaHertz. Do you need 5 MHz? Let's discuss...

Got the picture? This is a VERY nonlinear kind of system. There is no simple formula or procedure to predict where you can save $$ or accuracy or speed. But if most of the signal can go through ordinary resistive paths, you can generate real advantages.

I got a letter from an engineer just the other day, criticizing my old 1991 multiplier circuit. He said that at several of the output voltages, the output error was worse than 0.01% or 0.02% of the output voltage. He said I could never hold 0.02% accuracy, because the resistor ratios were already as bad as 0.02%, and because the errors of the multiplier in that circuit were *not* attenuated by a factor of 25.

Well he DID point out an error in that write-up: I neglected to point out that the expected accuracy was not 0.02% of the output signal, but 0.02% of full scale. In that circuit, the largest signal was 8 V × 9 V/ 10 V = 7.2 V. None of the errors was as large as 0.72 millivolts—all smaller than 0.01%. And that was without any particular optimization. That was what we got the first try. But with analog multipliers, it is customary to specify the accuracy as a percentage of full scale. Obviously, nobody can make an error better than 0.02% of the output voltage when V_{out} is around zero volts!!

He observed that if the ratio of the 14.2857 kΩ to the 10 kΩ resistor could be as bad as 0.02%, the accuracy would be lousy. No, because only a little bit of the signal came through those resistors. Most of the output voltage was established by the dc offset path, which gets trimmed.

In our case, for example, the 640 kΩ resistor R4 is in a path where the total gain error can be as big as 0.04%, due to the cascaded tolerances of R1, R2, R4, and R101. But that does no harm to the overall accuracy. If we swapped one R4 that was 0.01% high for one that was 0.01% low, all we have to do is tweak the 2 kΩ Output Offset Adjust pot, and the output would still be in spec. And, the errors in the output of the MDAC really *are* attenuated by 31. Gotta be! Absolutely.

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

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* "What's All this Multiplication Stuff, Anyhow?", *Electronic Design*, August 8, 1991; reprinted in August 19, 1996, *ED* Supplement, p. 55.

NOTES for Figure 1: First, I tried OP-07s running on separate ±7-V supplies, because they are cheap and have as good as 60 µV offset voltages. Then I evaluated LF411A's with V_{offset} less than 0.5 mV. Finally, I evaluated LMC6482s, as they had rail-to-rail outputs, so they could put out ±4.5 V or better, even with ±5-V supplies drooping as low as 4.75 V. Their offset voltage is only as bad as 0.35 mV max. However, the amplifier used with R104 was left as an LF411A, because it could drive the 2-µF bypass cap I had to add at the Reference input of the ADC at pin 2. I put a 1-kΩ pull-up from that point to the +5-V supply, so the LF411 only has to sink current, not source it.

All op-amps had feedback capacitors of 50 pF. Increasing this C_f can help cut down noise, if you don't need much bandwidth. All power supplies were bypassed with 0.1 µF ceramic and 2 µF electrolytic capacitors.

All resistors were ±0.01% precision film or wire-wound, except R102 (3.125 MΩ) and R105 (185.7 kΩ) at 0.1%.

I sent in the artwork before I had the whole circuit built. So if you want to build this, be sure to ground pins 3, 12, and 14 of the DAC, as well as pins 1 and 21. Also, add a couple microfarads from the ADC's Pin 2 to ground.

NOTE: Table 3 shows what we measured for V_{out}, using LMC6482AINs, with the error from the theoretical value below the V_{out} data. Power supplies were set at ±4.76 V. The errors tend to get a little better at 5 V. Not sure why. /rap

TABLE 3: OUTPUT VOLTAGE AT Vout (MEASURED)

	V_{in2}		
V_{in1}	+3.000 V	+2.500 V	+2.000 V
+3.500 V (error)	+2.6251 V (+0.1 mV)	+2.1876 V (+0.1 mV)	+ 1.7502 V (+0.2 mV)
+3.000 V (error)	+2.2501 V (+0.1 mV)	+1.8750 V (0.0 mV)	1.5000 V (0.0 mV)
+2.500 V (error)	+1.8754 V (+0.4 mV)	+1.5626 V (+0.1 mV)	+1.2500 V (0.0 mV)

NOTE: The worst observed error was 0.015% of the full-scale output of 2.625 V.

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Pre-Process Audio With Notch Filter To Improve FFT Dynamic Range

TOM MINTNER, *Audio Precision Inc., PO Box 2209, Beaverton, OR 97075; (503) 627-0832.*

The total harmonic distortion plus noise (THD+N) of a system is typically measured by feeding a single sine-wave stimulus into a device under test and measuring distortion on the output using a distortion analyzer. Within the analyzer, a sharp notch filter is tuned to the frequency of the stimulus sine wave to effectively null out the fundamental frequency. A voltmeter then measures the sum of the distortion products and noise within the bandwidth of the instrument settings. Expressed in percent or dB relative to the amplitude of the fundamental, this gives a useful single number for distortion and noise (THD+N) that fairly represents the overall performance of the device.

But it is often desirable, or necessary, to view the harmonic content and noise versus frequency to evaluate the harmonic balance of the distortion products, to check for the presence of hum components, or to analyze the character of the noise floor. This is usually done with a fast Fourier transform (FFT) spectrum analyzer. Because the FFT process is inherently digital, a high-quality analog signal must first be converted to the digital domain before spectrum analysis can take place.

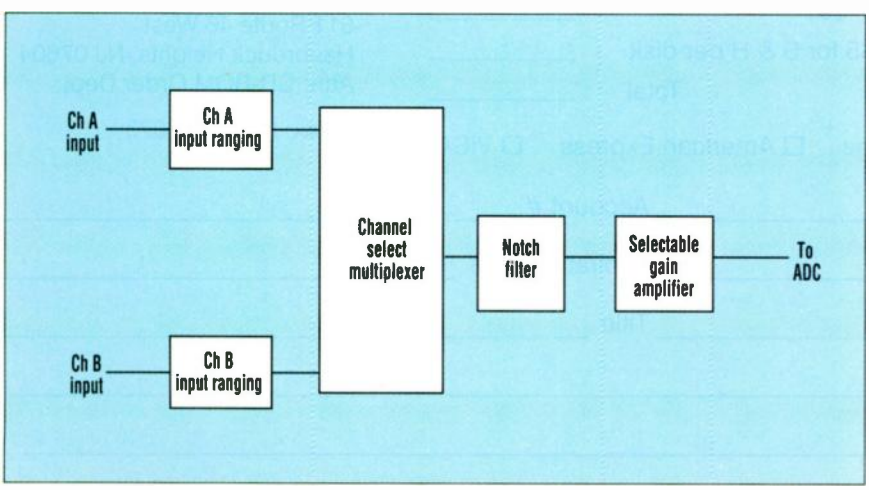
On the other hand, the performance of standalone FFT analyzers is limited by their analog-to-digital converters (ADCs), to the detriment of the low-level distortion and noise measurements desired. Even 16-bit or greater converters lack enough dynamic range to handle high-performance analog audio signals without degradation. This, in turn, will affect residual readings. A typical example would be measuring the analog performance of a 16-bit digital-to audio converter (DAC) with an FFT of its analog output. Even a 16-bit ADC on the FFT analyzer would fail to provide sufficient performance margin for measurements on the converter under test.

Similarly, other higher performance analog audio channels might achieve THD+N of –100 dB or better relative to fundamental, but the theoretical maximum dynamic range of the 16-bit converter used in the FFT analyzer remains only 98.06 dB, with typical 16-bit ADC system distortion + noise at perhaps –90 to –93 dB. In fact, a glance at specification sheets for many standalone FFT or network analyzers shows typical residuals (total in-band content, not displayed average noise levels) of –80 dB or worse.

In the single sine wave case above, the sine wave fundamental must be scaled to just below full-scale input value of the ADC. If higher, the signal will be clipped in the conversion. If lower, the low-level distortion components will begin to be buried in the noise floor of the converter. Preprocessing with a notch filter will solve the problem. By intelligently combining the notch filter from the distortion analyzer described above with an FFT analyzer, the full dynamic range of the ADC for the FFT may be utilized for the distortion and noise residuals alone *(Fig. 1)*.

The amplitude of the sine-wave fundamental is measured and stored for later use as a reference level for the residual distortion and noise readings. The distortion analyzer's notch filter will then remove the fundamental, at least to the depth of the notch itself—which will be 100 to 120 dB in an excellent analyzer. The remaining distortion components + noise have a much smaller total dynamic range, typically about 30 dB on a low distortion device under test (DUT). A low-noise selectable-gain amplifier in the distortion analyzer optimizes the level of this distortion + noise residual signal for conversion by the ADC. The worst distortion component is now nearly at full-scale of the FFT analyzer's ADC, making the converter's intrinsic noise and distortion negligible. The distortion components are now 30 to 40 dB above the noise floor of the ADC. Assuming a well-designed system with a 16-bit ADC, the resultant FFT will display distortion components at –130 dB and better.

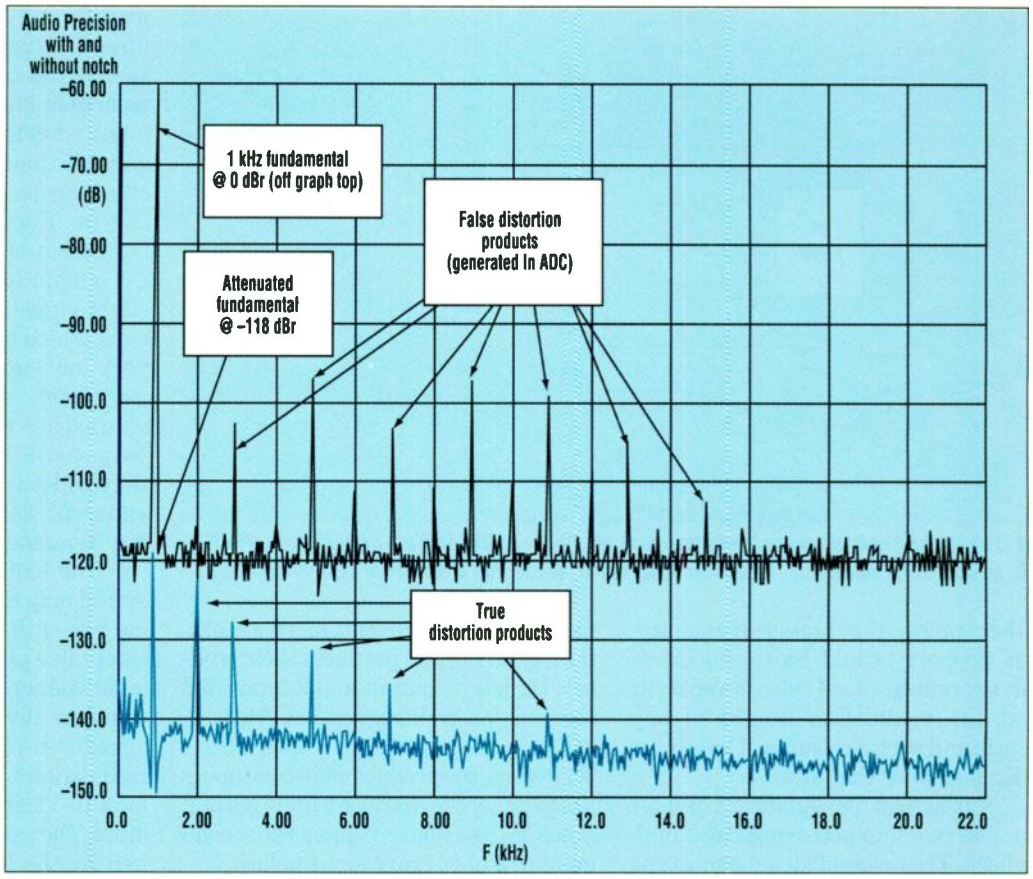
A comparison of FFT analysis—with and without notch filter pre-processing—of an extremely low distortion sine-oscillator indicates that with the notch filter, even extremely low-level harmonics may be observed out to the 11th harmonic and beyond *(Fig. 2)*. If the FFT analyzer also is capable of



1 **Dynamic range for measuring the spectral components of harmonic distortion is significantly increased by using a notch filter to remove the test signal fundamental. The remaining low-level distortion and noise components now fit within the dynamic range of an FFT analyzer's ADC.**

averaging data from multiple FFTs, then even finer detail may be resolved at these levels. If the analyzer uses a 20-bit or greater converter, even more impressive results may be obtained.

The general principle will work for any set of measuring devices, as described, provided that the noise and distortion residuals of each device are sufficiently low. But if all the measuring components are contained in one analyzer system the entire measurement process may be managed at once. Input auto-ranging, notch tuning, gain amplifier setting and internal ranging, as well as reference levels and measurement units are internally coordinated to produce automatic readings. ED



2 The instrument's ADC creates false distortion products that limit the measurement range (upper trace). Using a notch filter produces meaningful measurements out to the eleventh harmonic, which is 140 dB down.

Instantaneous, Filterless AM Demodulation With An Analog Divider

EBERHARD BRUNNER and BARRIE GILBERT, *Analog Devices, 804 Woburn St., Wilmington, MA 01887; (503) 690-1333.*

Amplitude Modulation (AM) is implemented by multiplication; it follows that demodulation ought to use division. In practice, however, the required element—a low-cost four-quadrant divider (4QD)—has not been available.

The common approach to AM demodulation has been to rectify the received signal and to then low-pass filter it to remove the carrier and leave only the modulation envelope. It also is achieved at times by using synchronous detection, which requires a balanced modulator (±1 function) clocked by a local oscillator that is at the same frequency and phase as the transmitted carrier. Low-pass filtering of the demodulated signal, however, is still required. The two detectors are identical when the modulation envelope never goes negative. The 4QD resembles the use of synchronous demodulation because it requires the carrier information to be recovered at the receiver and can demodulate to any depth. On the other hand, it differs in that it does not require low-pass filtering and can, therefore, provide *instantaneous* demodulation.

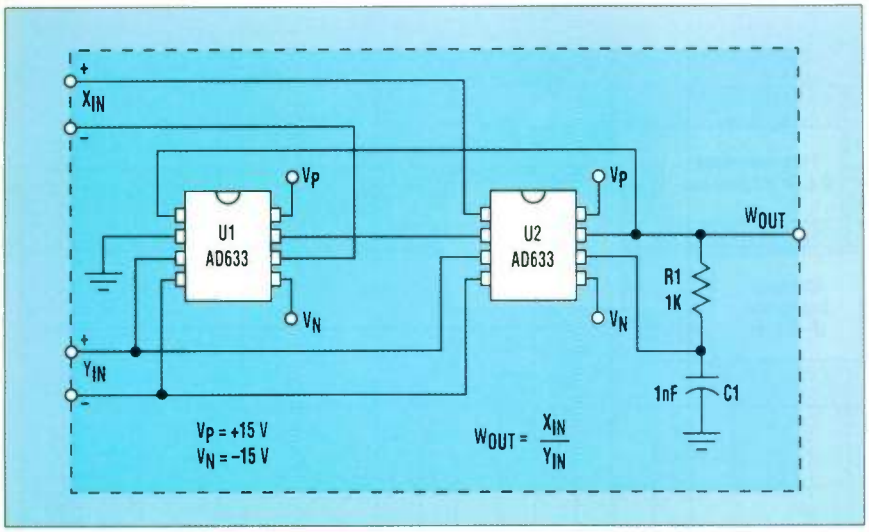
If we define the modulating signal as $E_m f_m(t)$ and the sinusoidal carrier as $E_c \sin(\omega_c t)$, where E_m and E_c are the amplitudes of the modulation and carrier waveforms, respectively, and $f_m(t)$ is some arbitrary modulation waveform, then the modulated waveform will be:

$$s(t) = E_c E_m f_m(t) \sin(\omega_c t)$$

To recover the modulation envelope, we can divide s(t) by a signal at the same frequency, with some general amplitude, E_r, which is exactly in-phase with the carrier:

$$V_{out}(t) = \frac{s(t)}{E_r \sin(\omega_c t)} = \frac{E_c E_m f_m(t) \sin(\omega_c t)}{E_r \sin(\omega_c t)} = \frac{E_c E_m}{E_r} f_m(t)$$

It's important to note that this process of division is instantaneous. Simply put, no filtering is required. Furthermore, it is symmetrical, meaning that the carrier and modulating frequencies can be reversed, with



1 Two low-cost multipliers can form a four-quadrant divider for filterless AM demodulation. The RC network at the output compensates for unacceptable phase shift at maximum input voltage levels.

either being the higher frequency; this property could be useful in resolver applications. It also is apparent that the modulation can be of any depth, and such a circuit can have gain if E_r is smaller than E_c.

A practical four-quadrant divider can use two inexpensive AD633 multipliers. The original idea for this type of divider was pesented in a paper in 1976.[1] *(Fig. 1)*. The AD633 generates the output:

$$W = X Y + Z$$

where X = (Vx1 – Vx2)/10 V, Y = (Vy1 – Vy2)/10 V, Z = Vz/10 V, and W = Vw/10 V. The 10 V scaling voltage is determined by an internal reference of the AD633.

The divider works as follows: U1 is connected in its standard multiplier mode and takes the output W_{OUT} plus the signal Y_{IN} and produces their product. U2 has its output and Z input tied together at low frequencies. This results in U2 operating "open loop." Therefore, the product of its two inputs has to be zero to produce a finite output. Since Y_{IN} is a nonzero input, the second input must be zero, which implies:

$$X_{IN} - Y_{IN}W_{OUT} = 0$$

and therefore,

$$W_{OUT} = X_{IN}/Y_{IN}$$

The input to the divider and the demodulated output (lower waveform) have a 10:1 frequency ratio with the carrier at 10 kHz (at 10-V amplitude) and the squarewave modulating signal at 1 kHz (at 5 V amplitude with a +3 V dc offset added *(Fig. 2a, upper waveform)*. The input signal was set up so as to require four-quadrant division as can be seen by looking at the polarities and phase changes on the input waveform. Note the equal rise and fall times, demonstrating the instantaneous demodulation.

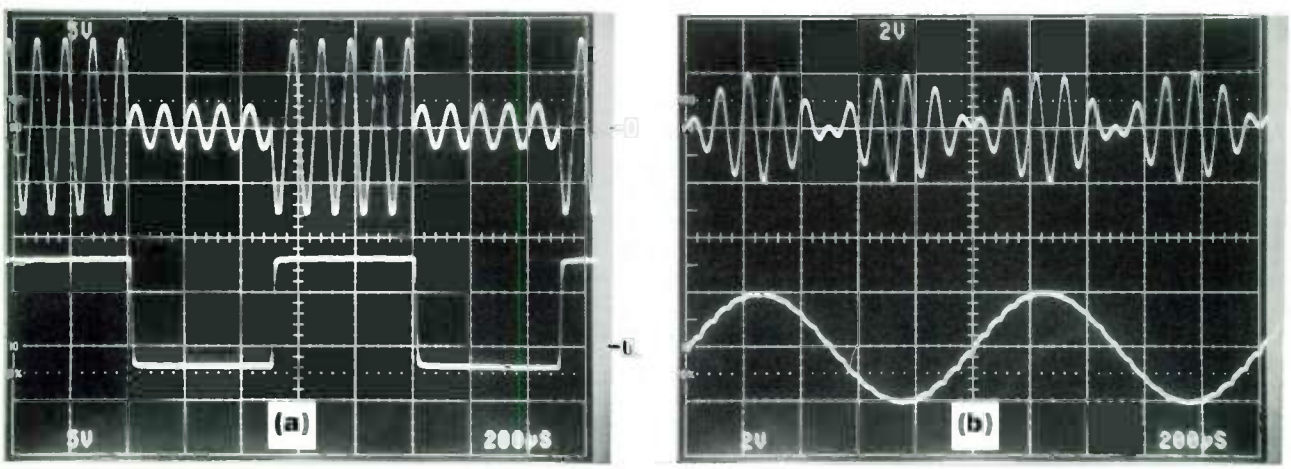
In Figure 2b the modulating waveform is now a sinewave with a 2-V amplitude and zero offset with a slight ripple caused by multiplier errors, which becomes apparent only at very-low signal levels *(Fig. 2b, lower waveform)*. Every time the divider approaches zero-divided-by-zero, the output will become distorted unless the divider is perfect. This error is less apparent as the carrier-to-modulating-frequency ratio increases.

The AD633 was designed to be operated only in certain modes. Connecting two of them in series results in unacceptable phase shift at the maximum input voltage levels. To compensate the complete divider, the RC network is introduced *(Fig. 1, again)*. The usable modulation bandwidth is dc to 20 kHz for a 10-V carrier amplitude at the Y_{IN} input. The carrier frequency is only limited by the bandwidth of the divider, roughly 500 kHz.

To summarize, This brief shows how a filterless, instantaneous, demodulator can be built using just two AD633s. The same approach can be used with higher bandwidth multipliers like the AD734. ED

References:

1. B. Gilbert, "New Analogue Multiplier Opens Way To Powerful Function-Synthesis," *Microelectronics*, Vol. 8, No. 1, London, 1976.



2 The upper waveform depicts a 10-kHz carrier modulated with a 1-kHz squarewave, while the lower waveform represents the demodulated output (a). When the carrier is modulated with a 1-kHz sine wave (upper waveform), the demodulated output (lower trace) exhibits a slight ripple due to multiplier errors (b).

Battery Charging Made Easy

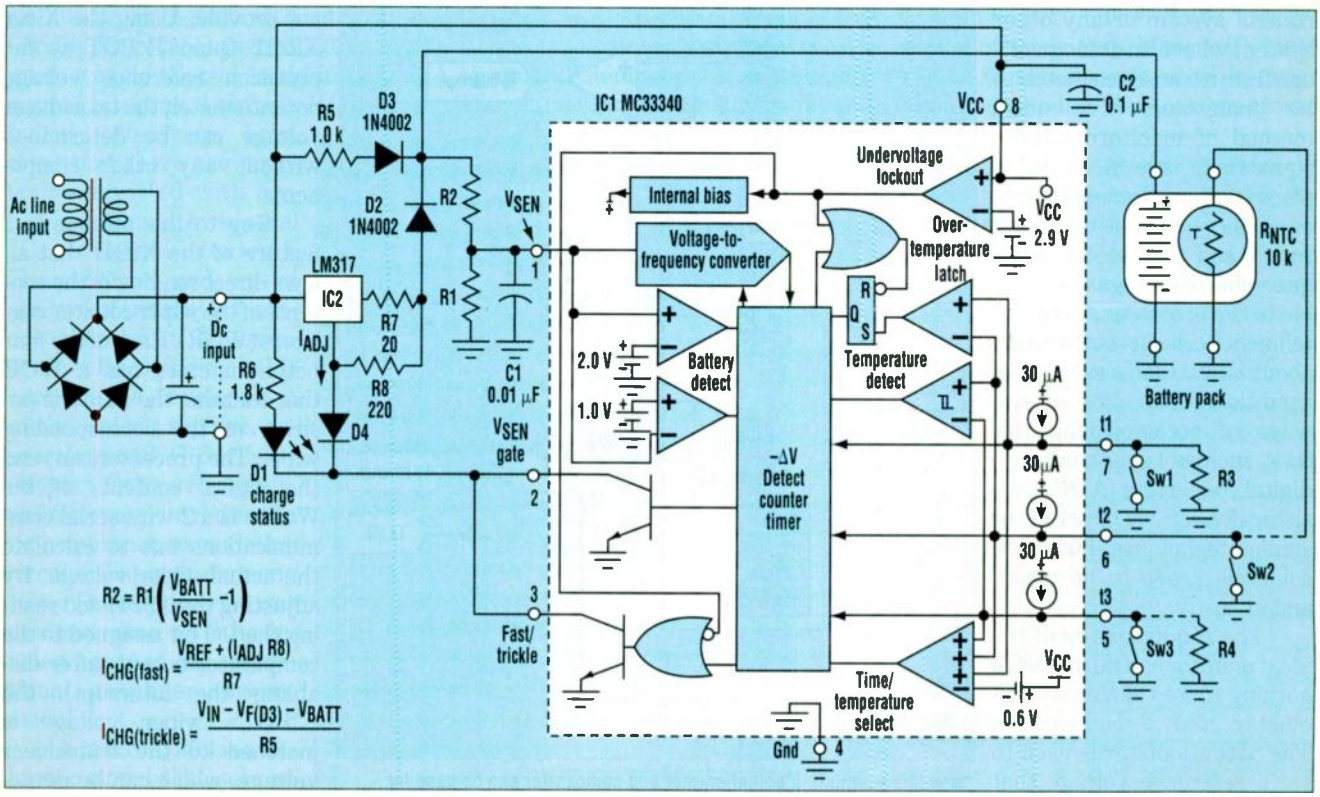
JADE ALBERKRACK and THOMAS SOMERVILLE, *Motorola Semiconductor Products Sector, 3102 N. 56th St., Phoenix, AZ 85018; (602) 413-3873, -5053.*

The growth in portable applications has brought renewed interest in more cost-effective battery technology and, consequently, the battery chargers designed to keep these batteries in service. A number of parameters must be controlled to provide safe operation, ensure maximum battery life, and charge the battery in the least amount of time. Previously, charging circuits have been designed from the simple to the more complex for smart batteries. However, the most cost-effective methods have not always been the most accurate. A charge-control circuit has been designed to simplify battery charger design for both nickel cadmium and nickel-metal-hydride batteries that addresses the need for accuracy without a hefty cost premium. This circuit provides a number of options to the battery charger designer.

A representative system uses a MC33340 controller core in an isolated, linear-regulator charging application *(see the figure)*. (The controller also could be used in switch-mode control or fast chargers.) The battery voltage is monitored by the V_{SEN} input that internally connects a voltage-to-frequency converter and counter for detection of a negative slope ($-\Delta V$) in battery voltage. A timer with three programming inputs is available to provide backup-charge termination. Alternatively, these inputs can be used to monitor the battery-pack temperature and to set the over- and undertemperature limits for backup-charge termination.

Two active, open-collector outputs are used to interface the controller with the charging circuit. The first output, V_{SEN}-gate, furnishes a gating pulse that momentarily interrupts the charge current. This allows an accurate method of sampling the battery voltage by eliminating voltage drops that are associated with high charge currents and wiring resistance. It also eliminates any noise voltages generated by the charging circuitry. The second output, fast/trickle, is designed to switch the charging source between fast and trickle modes depending on the voltage, time, or temperature.

When the V_{SEN} input is between 1.0 and 2.0 V, the one-cell equivalent is within the fast-charge voltage range. The charger switches from trickle- to fast-charge mode as V_{SEN} enters the voltage range. The reset signal is applied to the timer and the overtemperature latch is released. A change in operation occurs when the V_{SEN} input is still between 1.0 and 2.0 V and two consecutive $-\Delta V$ events are detected after 160 seconds. The battery pack has reached full charge and the charger switches from fast to latched-trickle mode. A reset signal must be applied and then released for the charger to switch back to the fast mode. The reset signal is applied when either V_{SEN} <1.0 V or >2.0 V, or V_{CC} <2.86 V. The signal is released



In this example, R7 sets the fast charge, while R5 sets trickle in a charge controller used in a line-isolated linear regulator charger. The R2/R1 divider is set so that V_{SEN} <2.0 V when the battery is fully charged.

other macromodels of circuits? Are there features in some Spice simulators that help in the creation process?

To answer these questions and to illustrate the creation process, consider the development of a macromodel for an adjustable voltage regulator such as National Semiconductor's LM117. The first step in developing a macromodel is to find a functional block diagram, which in this case is included in the data sheet *(see the figure, a)*. If this were not the case, it would be necessary for the designer to determine the functional behavior of the various stages of the IC.

It is important in building a macromodel that the components connected to the pins of the model are similar to those connected to the pins of the chip. This will help mimic the nonlinearities seen by loads connected to these pins. The transient response of this and many ICs is a result of the ac and dc effects interacting. It is advisable to model the ac specifications first and then the dc specifications. A first-pass macromodel has a simplified pass transistor with some of its ac characteristics removed and controlled by a series resistor and capacitor (R_{BC}, C_{BC}) *(see the figure, b)*. The amplifier portion of the IC is modeled with a dominant pole amplifier. The dc input bias current is modeled with a current source, and the reference voltage with a voltage source. Developing the design equations for this circuit is done by finding the poles and zeros of the ac ripple rejection and output impedance with a Spice simulator such as the Electronics Workbench EDA (Version 5.0) tool from Interactive Image Technologies.

The next step in the creation process is to build-in the nonlinear dc effects *(see the figure, c)*. For this regulator, that would be the dropout voltage (D_{BK}), the short-circuit current (polynomial-controlled source, E_{SC}), and the foldback current (polynomial-controlled source, E_{FB}). This macromodel was then tested for its transient response and although the line regulation and load regulation transient responses had not yet been considered in the modeling process, the model predicted these responses to within ±10% in amplitude and time—a consequence of the ac and dc specifications being modeled accurately.

Probably the most important step in the modeling process is testing. The developed model must capture the overall behavior and must not introduce any new phenomenon. This is why the ability to change component values during simulation and to do a model parameter sweep is an important functionality of the software. This allows testing various loads to see if the model responds properly, and gives the designer the opportunity to create a virtual data sheet for the new model.

Model creation is an ongoing process that must track the proliferation of analog and mixed analog/digital ICs and there is a need to develop new core macromodels. The Boyle op amp macromodel has been used to model hundreds of op amps. The adjustable voltage regulator macromodel is currently being used to model dozens of voltage regulators for the Electronics Workbench EDA model libraries. ED

Boost Converter For TV Tuners: 5 V-30 V

BOB KELLY, *Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086; (619) 486-6668.*

Because of the present limitations in varactor diodes, the tuner module in a satellite- or cable-TV receiver often requires 30 V for proper operation. This voltage is generally unavailable for tuners that are to be embedded in existing equipment, so the design engineer must develop a low-cost circuit that derives 30 V from the available supply voltage—usually 5 or 12 V.

Circuit designs published by IC vendors tend to focus on size, efficiency, and power consumption, rather than cost. The design shown here, on the other hand, has been optimized for cost with an emphasis on commonly-available components *(Fig. 1)*. It features an efficient boost controller (IC1) that operates on 5 V, generates a 30 V output, and delivers output currents to 12 mA. The current-sense resistor (R4) causes V_{OUT} to rapidly drop for output currents above 12 mA, but most tuner modules require only 5 mA. The circuit is a conventional boost converter, but various parts substitutions have been made to reduce cost. The lossy-leaded inductor, for example, costs four to five times less than surface-mount types.

Note that IC1's output stage (the Ext pin, designed for driving MOSFET gates) is specified for 55 ns rise and fall times with 1000 pF of load capacitance. This application, however, drives the base of an npn transistor through a 470-Ω resistor—an inefficient arrangement in which Q1's slow turn-on and turn-off significantly increases the switching losses. The usual antidote is to connect a "speed-up" capacitor across the resistor, which speeds the turn-on and turn-off times by rapidly conveying charge to and from the base. Because this circuit tolerates poor efficiency, the layout can be simplified by omitting that capacitor, which, as a result, reduces cost.

Consequently, instead of using an n-channel MOSFET power switch, the 2N2222A transistor does the job at very low cost. Similarly, the rectifier function is handled nicely with an inexpensive 1N4148 diode instead of the usual Schottky or fast-recovery diode.

Not all substitutions are acceptable, however: A 1N4001 diode, which turns off too slowly when reverse bias is applied, would actually draw energy from the output capacitor and prevent it from charging to 30 V. In addition, the output capacitor should have low equivalent series resistance (ESR). Skimping in this area may produce greater output ripple, causing the tuner to fail its specifications. The

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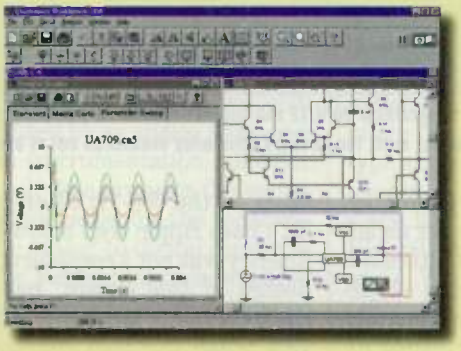

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temperature readings. The ratio of the voltage divider, R2/R4, is calculated to equal the drift of the thermocouple (58 μV/°C) in relation to the diode drift (–2.1 mV/°C). The noninverting input range of the ADS7816 is equal to V_{IN} to V_{REF}.

R6 is used as an open-circuit indicator, having a high resistance value such as 1 MΩ. In the event that the thermocouple is open-circuit, the inverting input to the ADC immediately becomes the voltage at the diode, approximately 0.6 V. This exceeds any voltage that the thermocouple could generate as a result of high temperature exposure. The digital conversion of the diode voltage produces a full-scale output, which is interpreted as an error condition by the 80C51 μP (U4).

The ADS7816 is a 12-bit ADC with a fully-differential sampling input. Reducing V_{REF} operates in the application as a gain control, where the ADC's input range is decreased, while the converter continues to have 12-bit resolution. The multiplexer (U3) uses levels from a voltage divider across the power supply. The range and absolute values of the voltages at the input of the multiplexer are tailored to the thermocouple type and temperature range of the application; for a temperature range of 0 °C to 1000 °C, the delta-voltage of the "E"-type thermocouple is 58 mV. The output voltage of the multiplexer is filtered and buffered with a single-supply op amp (U2) before it is presented to the ADC.

EFFECTIVE RESOLUTION VS. REFERENCE VOLTAGE V_{REF}

VREF input	LSB voltage	Effective resolution to 5 V FSR	Effective gain
5.000 V	1.22 mV	12 bits	1.00
3.750 V	916 μV	12.5 bits	1.33
2.500 V	610 μV	13 bits	2.00
1.250 V	305 μV	14 bits	4.00
0.500 V	122 μV	15.3 bits	10.00
0.300 V	73.2 μV	16 bits	16.67
0.237 V	58.0 μV	16.4 bits	21.10
0.200 V	48.8 μV	16.7 bits	25.00
0.100 V	24.5 μV	17.6 bits	50.00

The resolution increases are possible only if special care is taken to reduce the noise from the input sensor, voltage reference and power supply *(see the table)*. Although the clock frequency to the ADC is relatively fast for a thermocouple-sensing application (3.2 MHz), power dissipation is kept to a minimum by reducing the frequency of conversions. (For example, the power at a sample rate of 100 kHz is about 1 mW, while at 1 kHz, it reduces to about 20 μW.)

Although a thermocouple was used to illustrate the functionality of this circuit, other sensors also can be used. The gain range of this simple circuit, using the low-power ADS7816 and multiplexer, can vary from 1 to 50. ED

Remote Gain Control With A Digital Pot

RICK DOWNS, *Dallas Semiconductor Corp., 4401 S. Beltwood Pkwy., Dallas, TX 75244; (972) 371-4447, e-mail: rick.downs@dalsemi.com.*

Digital gain control has previously been accomplished using voltage-controlled amplifiers (VCAs) and digital-to-analog converters (DACs), or by using multiplying DACs as the feedback element of an op amp. For balanced-input amplifiers, such as for instrumentation, these approaches have their drawbacks: A balanced VCA is complex, and a multiplying DAC usually must be ground-referenced, while the gain-setting element of the traditional three-op-amp instrumentation amplifier must float with the input. A digital potentiometer can provide the solution to these limitations as well as extra functionality.

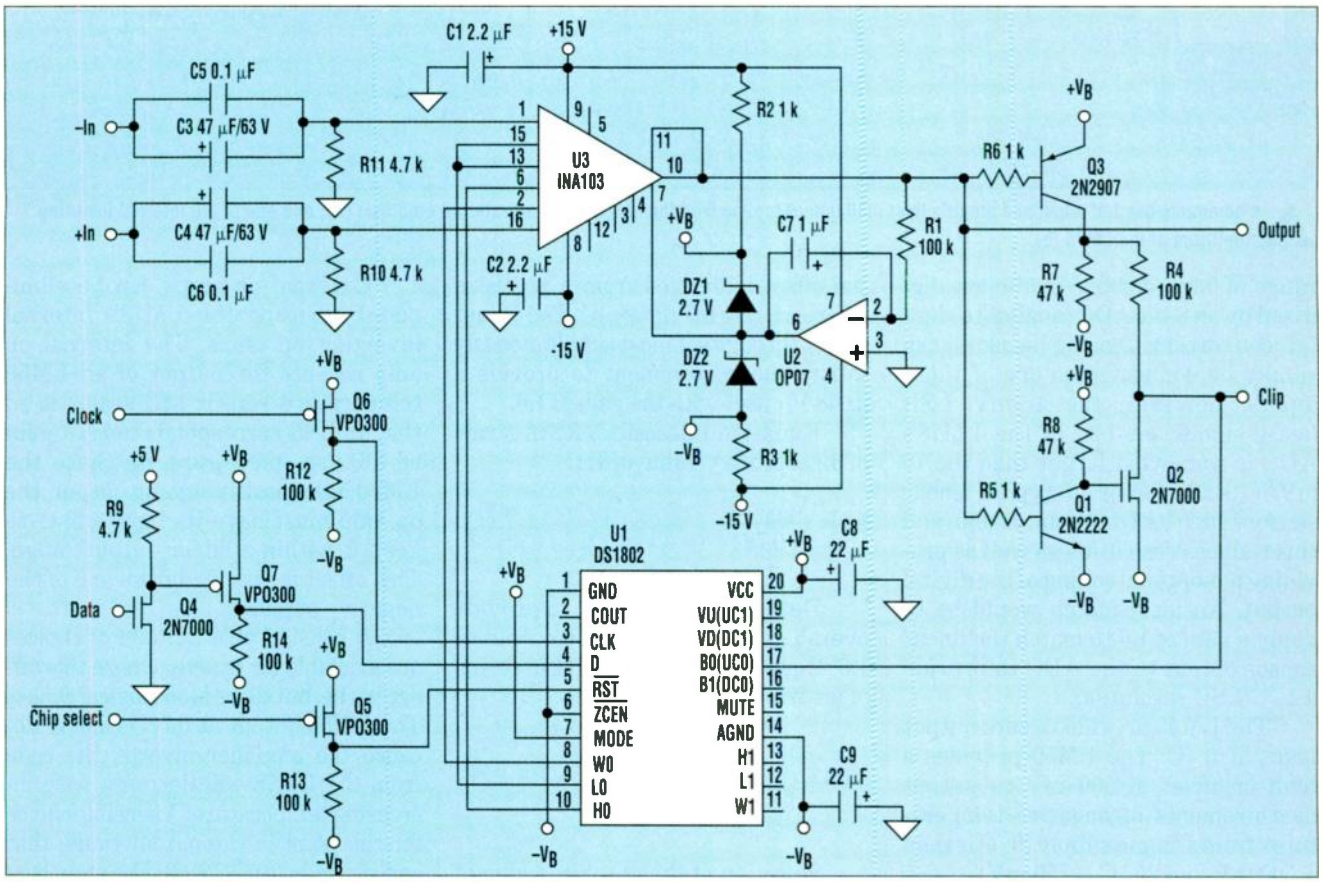
A digital potentiometer can be thought of as a resistive ladder with taps, with the taps being selected by an analog multiplexer under digital—normally serial—control with the value routed to a "wiper" terminal, much like a conventional potentiometer. Within the ratings of the device, the two ends of the digital potentiometer can be tied to any voltage in the circuit, as can the wiper. This is a significant advantage over multiplying DACs, and provides the opportunity to use a digital potentiometer as the gain setting element of an instrumentation amplifier. Digital potentiometers are available in a variety of formats, including a choice of linear or log tapers, single or multiple, and volatile (wiper settings are lost on power-down) or nonvolatile (the last wiper setting being saved in some form of nonvolatile memory, typically EEPROM). In addition, many are optimized for use in audio applications, and have excellent audio specifications.

This combination of features makes it tempting to use the device to provide remote gain control for a high-quality microphone preamplifier *(see the figure)*. There are several notable features to this circuit, using a Dallas DS1802 log-taper potentiometer, one of which is that the circuit also provides output limiting.

The primary gain element in this design is a Burr-Brown INA103 instrumentation amplifier optimized for audio applications. The balanced-microphone input is coupled to the INA103 through C3, C4, C5, and C6, which provide isolation from phantom-powered microphones. R10 and R11 provide a dc bias current return path for the INA103. The output of the INA103 is fed back through an amplifier built around U2, providing a dc servo to U3 (eliminating dc output offset) and creating, in conjunction with DZ1 and DZ2, the bias supply voltages (Vb) for the DS1802, which is rated at 7-V maximum. Using the dc servo output, the supplies for the DS1802 float with the dc offset, ensuring that the DS1802 will always have rails that meet the input signal conditions. The DS1802 is used to set the gain of the INA103 with control through the three-wire serial interface. Clock, data, and chip select signals are level-shifted from TTL to the floating supplies of U1.

The DS1802 does have its limitations on signal swing. The voltage level across the potentiometer cannot exceed its power supply rails; otherwise, clipping will result. Q3 is used to sense when the output from the INA103 swings to within 0.7 V of the positive supply voltage to the DS1802, while Q1 senses swings to within 0.7 V of the negative supply. The outputs of these two sense circuits use Q2 as an OR gate, providing a low output when the signal is approaching clipping, which can be used to enable a clip indicator. The DS1802's pushbutton control inputs and three-wire serial input can be used simultaneously, so one of these inputs can be used with this CLIP signal to provide automatic limiting.

This microphone preamplifer circuit provides 60 dB of digital-gain control in 1-dB steps. Its output level is limited by the DS1802 to about +6 dBu (about 4.5 V peak-to-peak), which is adequate for many systems, particularly for digital-audio ADCs which have a similar input range. The circuit has been built on a less-than-ideal solderless breadboard, yet still provided distortion figures of 0.01%, and an equivalent input noise less than -110 dBu. ED



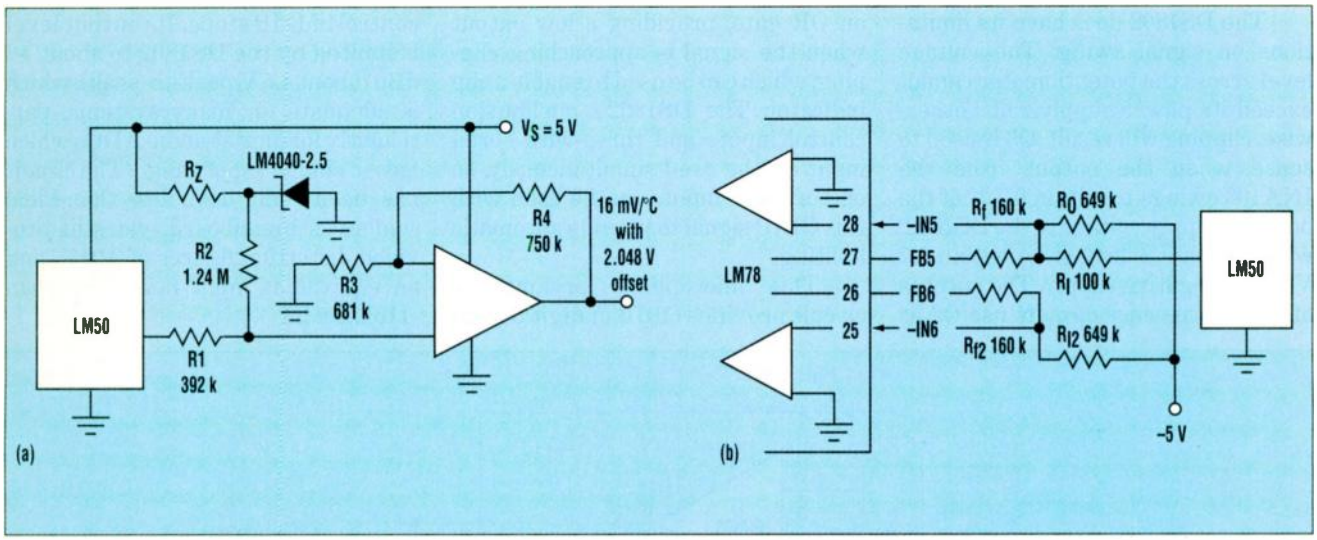
The remote gain control and limiting of an instrumentation amplifier (U3) can be implemented by using a digital potentiometer (U1).

Interfacing Linear Temperature Sensors With Computer Sensor

JERRY STEELE, *National Semiconductor Corp., 6377 E. Tanque Verde Rd., Suite 101, Tucson, AZ 85715; (520) 751-2380.*

Used for hardware monitoring of microprocessors, National Semiconductor's LM78 provides an internal temperature sensor as well as an input for thermostat-type sensor outputs, which are defined as trip-point outputs from sensors equipped with internal comparators and setpoints. Examples of thermostat sensors include the LM56 analog thermostat-type sensor and the O.S. (Overtemperature Shutdown) output of the LM75 digital sensor. While the addressability and digital output permits multiple LM75s to be used along with the LM78 in systems, many designers are attracted to the smaller size (SOT-23), lower power consumption, and lower cost of analog output sensors such as the LM45 or LM50.

The LM78 provides for five positive analog inputs with a full-scale



An op amp is used to offset and amplify the LM50 output for use with the LM78 using an external amplifier (a), and one of the internal inverting amplifiers of the LM78 (b).

range of 0 to +4.096 V. These are digitized by an 8-bit ADC (analog-to-digital converter). Analog sensors can simply be connected to one of these inputs; however, the 16-mV LSB (least significant bit) of the LM78's ADC is somewhat larger than the 10 mV/°C scale factor of typical linear sensors such as LM45 and LM50, and this reduces resolution as well as providing nonoptimal coding of the digital output. An ideal match would be to apply a gain of 1.6 to match the linear sensor output to the ADC to provide a 1 °C/LSB resolution.

The LM45 provides a zero output point at 0 °C. The LM50 provides a built-in offset of 500 mV to permit measurements of negative temperatures from a single supply (0 °C is then = 500 mV and 25 °C = 750 mV).

A sensible arrangement for the digital coding should make the 0 °C output occur at one-half the full-scale range of the LM78's ADC, or at 2.048 V. The table lists the digital output codes for several points in the range *(see the table)*.

This coding is like a two's-complement with an inverted-sign bit. An implementation uses an operational amplifier external to the LM78 and the offset is derived from a precision reference *(see the figure, a)*. The values for R1 through R4 must simultaneously satisfy the requirement to provide a 2.048 V offset with the gain of 1.6.

Equation 1 describes R2 in terms of an arbitrary value of R1:

$$R2 = \frac{V_{BIAS}\,R1}{0.78} \qquad (1)$$

Determine R3 and R4 to provide overall gain from the LM50 output of 1.6. Equation 2 describes R4 in terms of an arbitrary value of R3:

$$R4 = \left\{\left[1.6 \times \left(\frac{R1+R2}{R2}\right)\right] - 1\right\} \times R3 \qquad (2)$$

Selection of the absolute value of the offsetting resistors R1 and R2 must take into consideration the 2 kΩ output resistance of the LM50. Select R1 to be at least one order of magnitude greater than the LM50 output impedance; even better, make it more than two orders of magnitude, suggesting a resistor value of around 392 kΩ as the nearest standard 1% value. The values shown are based on 392 kΩ for R1 *(see the figure, again)*.

External op amps can be eliminated by using the LM78's internal inverting op amps. The internal op amp accepts the output of an LM50 temperature sensor and scales it so that an LSB corresponds to 1 °C (gain of 1.6) *(see the figure, b)*. Since the LM50 has a positive-going output, the op amp must have its input offset to keep it within a linear output range. This offset is obtained from one of the negative supplies.

A considerable latitude of choices are available for exactly where this offset can be, but there is one logical choice. The LM50 output at 0 °C is 0.5 V. Because the amplifier inverts, the code from the LM78 will decrease with increasing temperature. A sensible choice for the point in the output range that corresponds to 0 °C would be at an output code corresponding to decimal 127:

Code at –1 °C: 1000 0000
Code at 0 °C: 0111 1111
Code at 1 °C: 0111 1110

In order to provide this inverted two's-complement coding, the op amp output, when the LM50 is at 0 °C, should be equal to 127 × 16 mV, or 2.032 V. The choice of values for R_F and R_I are a function of the gain of 1.6 required, so R_O can be found from:

$$R_O = \frac{V_O}{\left(\frac{2.032}{R_F}\right) - \left(\frac{0.5}{R_I}\right)} \qquad (3)$$

where V_O is the voltage or power supply used to provide the offset,

DIGITAL OUTPUT CODES FOR LINEAR TEMPERATURE SENSOR

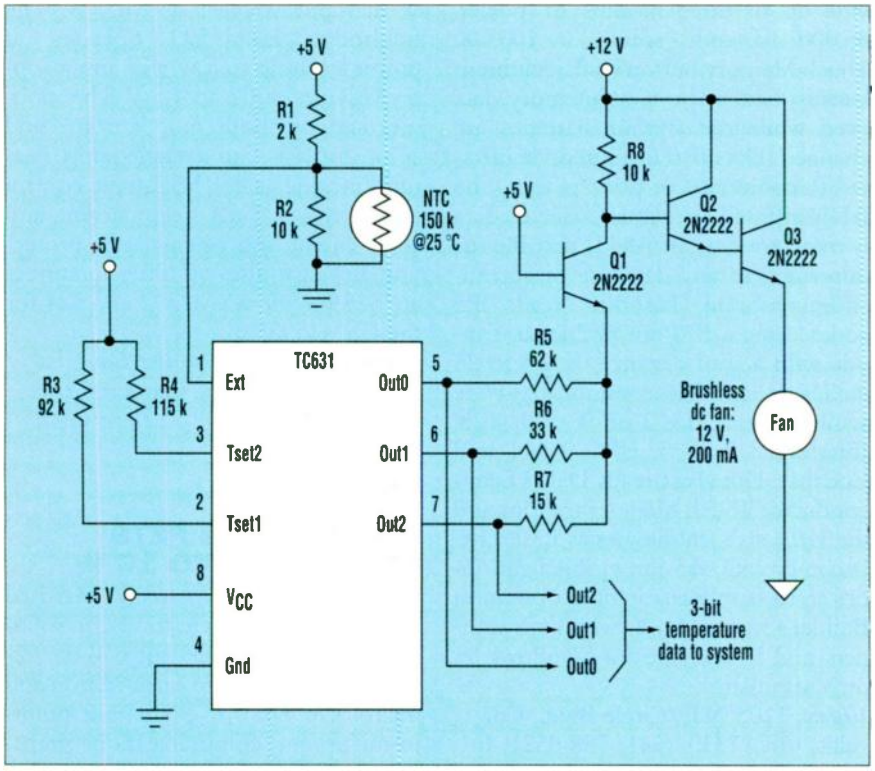
Temperature	LM50 output	LM78 analog input	Digital code from LM78
–25 °C	250 mV	1.648 V	0110 0111
0 °C	500 mV	2.048 V	1000 0000
25 °C	750 mV	2.448 V	1001 1001
125 °C	1.75 V	4.048 V	1111 1101

most likely the –5 or –12 V supply.

In this example, since the –5 V supply is used, R_O is 649 k. With this circuit arrangement, use the second amplifier for sensing the same negative supply that provides the offset. Configure the second voltage-sensing amplifier to have an identical gain with respect to the offsetting supply as the temperature sensor amplifier. Accomplish this by making both feedback resistors the same value, and the input resistor, R_{I2}, the same value as the offset resistor, R_O. In software, subtract the output of the supply-sensing amplifier from the temperature-sensor amplifier to null out any effects of power supply variation. ED

Fan Speed Control Adjusts To Temp.

DON ALFANO, *TelCom Semiconductor Inc., 1300 Terra Bella Ave., Mountain View, CA 94039; (512) 873-7100.*



This temperature-proportional fan-speed control for a brushless dc motor uses TelCom Semiconductor's TC631.

Why is it that electronic equipment manufacturers run their system cooling fans continuously and at full speed? This not only wastes supply current, but generates objectionable acoustic noise. In addition, continuous full-speed fan operation inevitably causes fan-bearing failure. (You remember fan-bearing failure? That's when the fan emits a blood-chilling squeal, second only to fingernails scraping across a blackboard!) If you have a fan in your system, you also should provide temperature-proportional fan speed control. This fan control methodology saves supply current and significantly reduces acoustic noise. Fan life also is dramatically extended; for example, operating the fan at 90% of its rated speed can as much as double fan-bearing life.

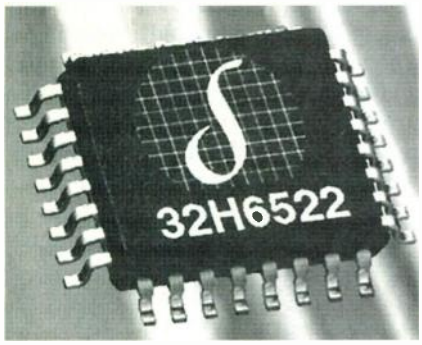
A temperature-proportional fan-speed control circuit can be based on TelCom's TC631 3-bit temperature detector *(see the figure)*. The circuit supports 12-V, brushless, dc fans having a maximum operating current of 200 mA, but higher current and/or 5-V or 24-V fans can be used if the values of R5 through R8 and the power rating of Q3 are adjusted accordingly. The user programs the TC631 upper and lower temperature range measurement limits (Tset1 and Tset2) with resistors R3 and R4. The TC631 divides this programmed range into six equally-spaced states (plus under-range and over-range states) and assigns a binary output code (000 to 111) to each one. The values of R3 and R4 shown program Tset1 at 40°C and Tset2 at 85°C; the TC631 output code therefore advances one count every 7.5°C temperature rise above 40°C.

The temperature sensing voltage to the TC631 is provided by a low-cost NTC thermistor and resistors R1 and R2. This network generates a TC631-compatible voltage range of 4.08 V to 3.86 V for the corresponding temperature range of 40 °C to 85 °C. The outputs of the TC631 connect to a fan-driver circuit consisting of resistors R5 through R8 and transistors Q1, Q2, and Q3. At temperatures below 40°C, all three outputs of the TC631 are low, maximizing the current through the collector of Q1 and minimizing the output voltage applied to the fan. In this state, it is at about 6 V, causing the fan to run at roughly 50% of its rated speed. The fan is operated at a minimum speed of 50%, assuring stall-free operation. As the temperature increases, the TC631 output code advances, causing a higher voltage to be applied to the fan. This continues until the output code 111 is reached, at which time Q1 is completely turned off, and the fan is operating at approximately 90% of full speed.

Circuit construction is straightforward, although care must be taken to keep the supply and ground lines of the fan separate from those of the TC631. The supply line of the TC631 should be adequately bypassed and TelCom Semiconductor offers a preassembled version of the circuit for evaluation. ED

DEMODULATOR EXPANDS DISK-DRIVE CAPACITY

By improving the accuracy of hard-disk drive servo-positioning systems, the 32H6522 6-burst servo demodulator chip enables servo designs to exploit the narrower recording track widths of advanced MR heads to boost overall drive capacity without further modification. The demodulator ac-



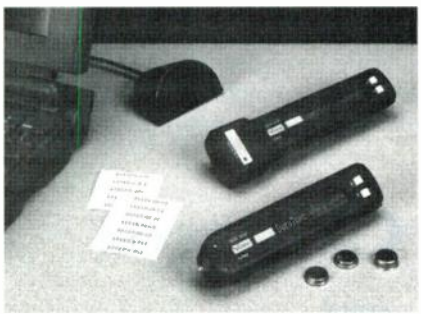
cepts multiphase analog differential-burst-encoded, position-error signals from a read-channel IC, performs an area integration and comparison, and sends the result in digital bit-serial format to a digital servo-timing controller or DSP. From three to six consecutive servo bursts can be captured at any time to allow optimal trade-offs between positioning accuracy and servo burst overhead. Two additional analog channels are available for other functions such as calculating digitized performance measurements for a read channel. The 32H6522 includes an area-regulating AGC loop, an area detector, and a 10-bit 1.2-μs analog-to-digital converter for digitizing burst areas. An analog multiplexer directs the burst area information to one of six track-and-hold circuits with an on-chip capacitor for temporary storage. To minimize servo channel mismatch, the 32H6522 uses a single capacitor for servo burst-area detection. The IC is available in a 32-pin TQFP for $4.00 each in quantities of 1000.

Silicon Systems Inc., 14351 Myford Rd., Tustin, CA 92680-7022; (800) 624-8999, ext. 151.

CIRCLE 80

BAR-CODE READERS ARE CORDLESS

LaserLite and DuraTrax from Videx are portable battery-powered bar-code readers housed in water- and dust-resistant aluminum housings. Each reader contains 128 kbytes of battery-backed memory and an internal clock that automatically records the time and date for each transaction. A 2-by-16 LCD display prompts and verifies information during data collection. Battery power is checked by requesting an LCD display. Three buttons are provided for scanning, scrolling forward,



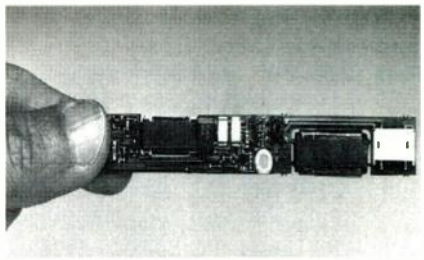
and scrolling backward through the data. LED indicators and audio tones provide feedback with each successful read operation. The readers use four standard AA alkaline batteries that provide up to three months of power, 35,000 bar-code scans, or 100,000 Touch Memory button reads. A lithium backup battery protects memory data even while the alkaline batteries are changed. Data is transmitted via infrared to computers or printers using the IrDA infrared standard. Collected data is transferred as an ASCII text file for importing to any database or spreadsheet program. LaserLite reads bar codes using a 670-nm visible laser diode with a scan distance of 2.5 to 24 inches. It reads six common bar-code symbologies: Code 3 of 9, Code 128, Interleaved 2 of 5, UPC, EAN, and Codabar. DuraTrax reads Dallas Semiconductor Touch Memory buttons and the same six symbologies as LaserLite. It comes with 655-nm visible light optics and a sapphire scan tip. Application Builder software works with both scanners and is available for Windows 95 or Macintosh.

Videx, 1105 N.E. Circle Blvd., Corvallis, OR 97330; (541) 758-0521; Internet: http://www.videx.com.

CIRCLE 81

BACKLIGHT INVERTERS IMPROVE EFFICIENCY

Two single-stage cold-cathode fluorescent lamp (CCFL) inverter modules from Linfinity Microelectronics employ the company's Current Synchronous Zero Voltage Switching (CS-ZVS) technology for the design of more efficient dimmable CCFL inverter circuits. The 8-mm high modules offer a light-efficiency improvement of up to 48% over older Buck-Royer de-



signs, and improved magnetics reduce size and power requirements. The LXM1592 and LXM1593 convert unregulated dc voltage from a battery or ac wall adapter to the high-voltage, high-frequency sine wave required to ignite and run a CCFL. They regulate the line voltage and lamp current and permit lamp dimming using a single synchronous power stage built from a pair of complementary power MOSFETs. The half-bridge LXM1592 operates with lamps needing less than 5 W at input voltages above 7 V. The full-bridge LXM1593 operates at power levels up to 5 W with input supply voltages down to 4.5 V. The modules support both monochrome and color displays with a single lamp. Features include analog brightness control inputs, typical 3 μA sleep current, and short-circuit and open-circuit protection. For quantities of 1000, unit prices are $25 for the LXM1592 and $24 for the LXM1593.

Linfinity Microelectronics Inc., 11861 Western Ave., Garden Grove, CA 92641; (714) 898-8121 or (800) 877-6458.

CIRCLE 82

POWER GaAs FETS DELIVER UP TO 16 W

A family of internally matched power GaAs FETs are for use in solid-state power amplifiers for 6.4- to 7.2-GHz C-band satellite earth-station and microwave point-to-point and point-to-multipoint communications transmitters. Class A linear operation makes these transistors suitable for digital signals. The IM6472 series of devices combine high power output with ±0.3-dB gain flatness and high linearity (–45-dBc third-order intermodulation distortion at specified single-carrier levels). Transistor performance can help reduce the level of intermodulation distortion and harmonic spurious signals for higher-linearity power amplification. Internal 50-Ω input- and output-matching networks eliminate the need for RF matching and eliminate

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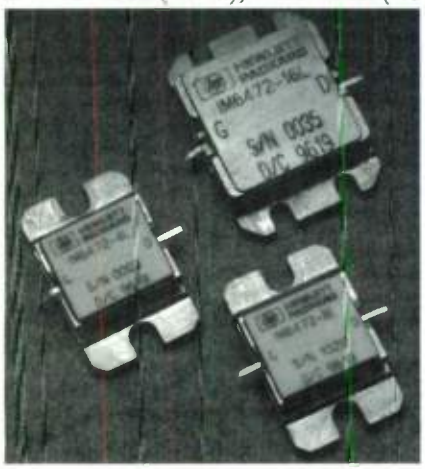
the handling and die-attach problems associated with using large-geometry, high-power chip transistors. Typical power output at 1 dB gain compression is +36.5 dBm (4.5 W), +39.5 dBm (9.0



W) and +42.5 dBm (18.0 W) for the IM6472-4L, IM6472-8L, and IM6472-16L, respectively. Unit prices for quantities up to 9 units are $194 (IM6472-4L), $366 (IM6472-8L), and $720 (IM6472-16L). Delivery is 4-6 weeks ARO.

Hewlett-Packard Co., 5301 Stevens Creek Blvd., P.O. Box 58059, Santa Clara, CA 95052-8059; (800) 537-7715, ext. 1927.

CIRCLE 83

16-BIT SAMPLING ADC BOASTS 4-CHANNEL MUX

The ADS7825 16-bit sampling analog-to-digital converter (ADC) comes complete with a four-channel input multiplexer, sample/hold, reference, clock, and a parallel/serial output microprocessor interface. It can be configured in a continuous conversion mode to sequentially digitize all four channels for industrial process-control, test and measurement, and analytical instrumentation applications. The ADS7825 can acquire and convert 16 bits to within ±2 LSB in 25 µs while consuming only 50 mW. Laser-trimmed scaling resistors provide a ±10-V input range and channel-to-channel matching of ±0.024%. Key specifications include ±2 LSB maximum INL, 16-bit DNL with no missing codes, operation from a single +5-V supply, and a 50-µW power-down mode. Priced at $34.50 each in lots of 1000, the converter is available for the industrial temperature range in a 28-pin, 0.3-in. plastic DIP or a 28-lead SOIC.

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Burr-Brown Corp., 6730 S. Tucson Blvd., Tucson, AZ 85706; (800) 548-6132.

CIRCLE 84

HIGH-OUTPUT OP AMP USES LOW POWER

Consuming just 7.5 mW, the CLC450 current-feedback op amp is optimized for low-power portable equipment. The device has a small-signal bandwidth of 100 MHz (A_V = +2 V/V) and a slew rate of 280 V/µs while operating from a single +5-V supply. Using a buffer-driven common-emitter output, the CLC450 can source or sink 100 mA and drive a 100-Ω load within 1.2 V of either supply rail. The op amp is ideal for applications such as video line-driving through coaxial cable, and for signal-boosting applications such as driving single-ended transformers. Other applications include 8- to 10-bit video ADC (analog-to-digital converter) driver and DAC (digital-to-analog converter) buffer designs, portable test and measurement equipment, and high-speed modems. Performance is further enhanced in ±5-V systems where bandwidth increases to 135 MHz and slew rate jumps to 370 V/µs. Available in industrial temperature range 8-pin plastic DIP, plastic SOIC, and plastic SOT-23 packages, the op amp costs $1.39 each in lots of 1000.

Comlinear Corp., 4800 Wheaton Dr., Fort Collins, CO 80525-9483; Deborah Reinert, (970) 226-0500.

CIRCLE 85

5-MHz SAMPLING ADC MERITS MIL-STD-883

Fully qualified to MIL-STD-883, the ADS-944/883 is a 14-bit, 5-MHz sampling analog-to-digital converter (ADC) with guaranteed no missing codes to the 14-bit level over the military temperature range of −55°C to +125°C. Signal-to-noise ratio is 76 dB and total harmonic distortion (THD) is −77 dB. Packaged in a hermetically-sealed 32-pin ceramic DIP, the converter typically consumes 2.95 W. Superior differential linearity, SNR, and harmonic distortion performance qualifies the device for use in time-domain and frequency-domain applications such as FPA- and CCD-based imaging, digital communications, radar, and sonar. Initiation of the conversion process requires only the rising edge of a single start pulse, and the device does not have a pipeline delay. Complete with internal sample/hold amplifier, reference, timing/control logic, and error-correction circuitry, the ADS-944/883 is priced at $849 each in lots of 100. Delivery is 12 to 16 weeks ARO.

Datel Inc., 11 Cabot Blvd., Mansfield, MA 02048; (508) 339-3000, ext. 227 or 221.

CIRCLE 86

POWER NMOSFETS HAVE LOW ON-RESISTANCE

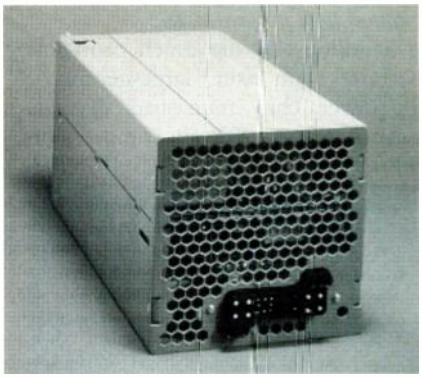
Two n-channel 30-V power MOSFETS, the IRL3103 and IRL3303, offer improved efficiency over previous 60-V parts that are commonly used in dc/dc converter circuits. With the proliferation of Pentium-based and other 3.3-V microprocessors, 30-V Gen5 MOSFETs are ideal for either on-board or voltage-regulator mode dc/dc converters. Other applications include 12-V UPS systems, and automotive systems such as ABS, power steering, and HVAC systems. Lower voltage and on-resistance allow the use of a single IRL3103 or IRL3303 instead of two IRFZ44s or two IRFZs in parallel, respectively. Both devices are logic-level parts with on-resistance ratings at V_{GS} = 10 V and 5.5 V. At V_{GS} = 10 V, the IRL3103 has an $R_{DS(on)}$ of 0.014 Ω and I_D of 56 A. The respective IRL3303 ratings are $R_{DS(on)}$ = 0.026 Ω and I_D = 34 A. For quantities of 1000, pricing for through-hole TO-220 versions of the IRL3301 and IRL3303 are $2.06 and $1.19, respectively. Similar quantities for surface-mount versions cost $2.38 and $1.50, respectively.

International Rectifier, 100 N. Sepulveda Blvd., El Segundo, CA 90245-4359; (310) 252-7161.

CIRCLE 87

HOT-PLUGGED SUPPLY DELIVERS 3000 W

The PM33211BP-5 power supply, with isolated front end, can deliver up to 3000 W. In a 5 by 5 by 11.5-in. case and weighing only 10.5 pounds, it is ideal for unattended operation in a remote system. The hot-pluggable design with power factor correction is ideal for use in N+1 fault tolerant applications. Standard output voltages of 24, 26, 28, and 48 VDC are available. Full power is provided at input voltages from 170-264 VAC, 43-63 Hz, at ambient temperatures from 0 to 50°C, or −30°C to +70°C as an option. Overcurrent, overvoltage, and overtemperature protection are standard features. It is approved to UL, CSA, and VDE safety specifications, and meets VDE and FCC EMI requirements. Delivery time is approximately 10 weeks for most models.



Pioneer Magnetics Inc., 1745 Berkeley St., Santa Monica, CA 90404; (310) 829-6751.

CIRCLE 88

DC-DC CONVERTERS AIM AT BATTERY DESIGNS

Two dc-dc converter ICs track the trend to lower supply voltages for ICs used in battery-powered products. The output voltage of the ML4950 converter is programmable from 2.0 V to 3.0 V via two external resistors. A small inductor and two capacitors are the only other external components required. The chip supplies up to 100 mA of output current. The ML4850 dc-dc converter has a fixed output of either 2.2 or 2.5 V and requires no external programming resistors. Both devices convert and regulate voltage from a single alkaline battery in the range between 1.5 and 1.0 V with an accuracy of ±3% and an efficiency exceeding 90%. The chips also work with single-cell batteries such as NiMH and NiCd. High efficiency results from the use of synchronous rectification. This technique replaces the traditionally used catch diode with an intelligent circuit that switches a built-in MOSFET to conduct inductor flyback current. Both devices generate a low-battery signal with a programmable threshold that is set with a resistor pair. This signal can activate a battery-low indicator or initiate a low-battery routine in a microcontroller. Available in an 8-pin SOIC package, the ML4950 and ML4850 cost $2.05 and $1.95, respectively, in quantities of 1000.

Micro Linear Corp., 2092 Concourse Dr., San Jose, CA 95131; Doyle Slack, (408) 433-5200.

CIRCLE 89

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LOW-PASS FILTER OFFERS COMPACTNESS

The LTC1096-1 is a monolithic 8th-order elliptical low-pass filter that requires no external components except power-supply bypass capacitors. It operates from a single supply of 3.3 to ±5 V and provides 72 to 80 dB of dynamic range for precision telecommunications and anti-aliasing applications requiring a compact solution. Programmed by an external clock, cutoff frequency is equal to the clock frequency divided by 100. Typical passband ripple is ±0.15 dB. The stopband attenuation has a progressive elliptic response reaching 52 dB at 1.4 times the cutoff frequency and over 70 dB at twice the cutoff. The filter can be clock-tuned to cutoff frequencies up to 12 kHz with ±5-V supplies, 8 kHz with a single 5-V supply, and 5 kHz with a single 3.3-V supply. Power consumption is 2 mA on a single 3.3-V supply and 3.8 mA with a ±5-V supply. Maximum cutoff frequency is 12 kHz with a ±5-V supply. Signal-to-noise+THD is over 70 dB for an input voltage range of 0.3 to 2.5 Vrms. Commercial and industrial versions are available in 8-lead PDIP or SO-8 surface-mount packages. Pricing begins at $4.70 each in quantities of 1000.

Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035-7417; (408) 432-1900.

CIRCLE 90

IC INTERFACES POWER SWITCH AND SENSOR

The LS6501 CMOS IC is a complete motion detection interface between a PIR sensor and a relay or triac switch. It includes a two-stage amplifier, window comparator, and digital filter to amplify and noise-filter the input from a PIR sensor. Gain and bandwidth are externally controlled to allow customization of the motion-detection waveform. Features include single- and dual-pulse mode, programmable timer, selectable dead time, ambient light-level inhibit, regulated 5 V for the PIR sensor, and a motion-detection LED indicator. An output driver powers a relay in dc mode or a triac in ac mode. Applications include automatic lighting controls and intrusion alarms. The LS6501 comes in a 16-pin plastic DIP at $1.45 each in 1-k lots. A 16-pin wide-body SOIC costs slightly more.

LSI Computer Systems Inc., 1235 Walt Whitman Rd., Melville, NY 11747; (516) 271-0400.

CIRCLE 91

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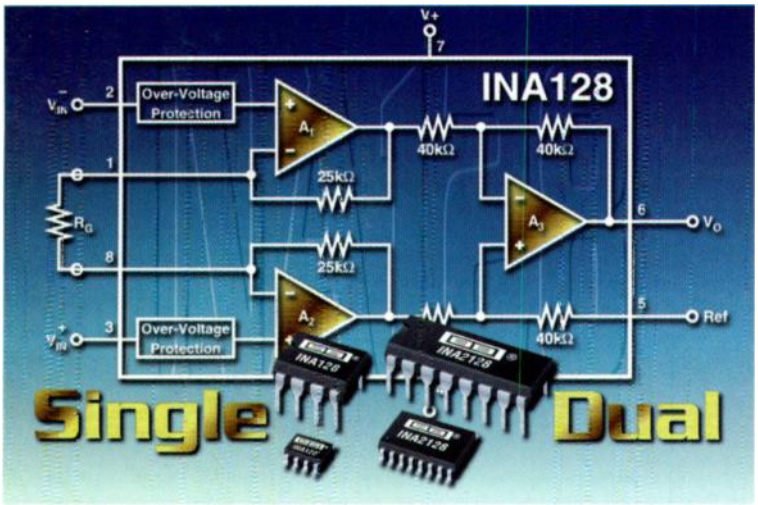

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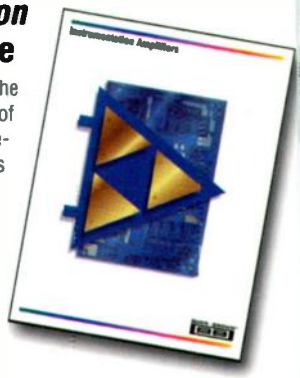

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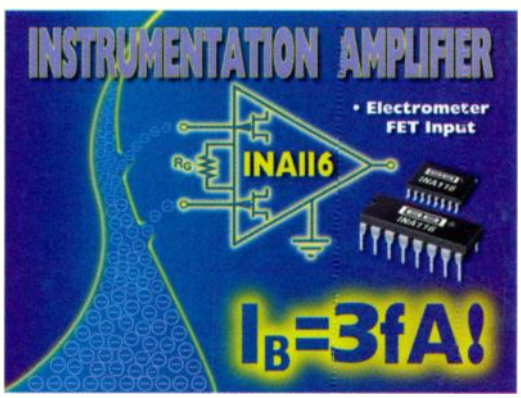

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