ELECTRONIC DESIGN

FOR ENGINEERS AND ENGINEERING MANAGERS-WORLDWIDE

A PENTON PUBLICATION $10.00

JANUARY 20, 1997

200-Msample/s ADC Zips Through Color Conversion p. 67

Advanced Microprocessors Demand Amperes Of Current At <2V p. 31

Designing Power Systems Around Processor Specifications p. 53

Commercial Use Of Silicon MEMS Technology Is Coming Of Age p. 75

New Parasitic-Extraction Tools Needed For DSM Flows p. 111

Intelligent I/O Architecture Enables Faster, More Flexible Systems p. 125

Helpful Hints For Making Oscilloscope Measurements p. 143

The 100,000 Gater.

NOW SHIPPING

Introducing Altera's EPF10K100. The highest-density Programmable Logic Device ever.

With 100,000 gates, Altera signals a new era for programmable logic. Big enough to handle most gate array designs and larger than any FPGA, the EPF10K100 satisfies even the most ferocious appetite for density. From prototyping through production, you get all the benefits of programmability plus new design capabilities.

The secret to the EPF10K100 is below the surface.

The EPF10K100 features the industry's first embedded array architecture. Fast and efficient embedded array blocks can pack up to 24K bits of on-chip RAM, with room for other complex megafunctions such as microcontrollers and DSP and PCI functions*. These megafunctions shorten design cycles and allow for design re-use and re-targeting.

To help you attack your high density designs, our MAX+PLUS II development tools are completely compatible with leading EDA vendors, such as Synopsys, ensuring seamless integration with your existing design environment.

It's time to give your designs more bite.

If high density, exceptional performance, and megafunction support will help you tackle your biggest design challenges, you're ready for the 100,000 Gater. Call us today at 800-9-ALTERA (800-925-8372), Dept. A10NAP2. We'll send you a free FLEX 10K information kit. Or, find us at http://www.altera.com on the world-wide web.

The ALTERA Advantage

*Developed through AMPP (Altera Megafunction Partners Program)

See us at Design Supercon

Complete Gigabit Ethernet solutions that go the distance.

HP's low-cost fiber optic transceiver modules and ICs enable you to accelerate the development of your Gigabit Ethernet products.

Whether you're designing products for intra-building or campus links, HP offers the most complete range of physical-layer Gigabit Ethernet solutions available. Our drop-in optical transceivers offer total flexibilty in link length, fiber type (MMF and SMF) and cost, and pair with our Serializer/Deserializer IC to complete your solution.

HP's 850nm VCSEL transceiver addresses standard multimode backbone applications at longer distances, higher reliability and lower costs relative to existing gigabit solutions. And our 1300nm controlled mode launch laser transceiver, proven in both datacom and telecom, drives MMF applications to over 500m and SMF applications up to 3km.

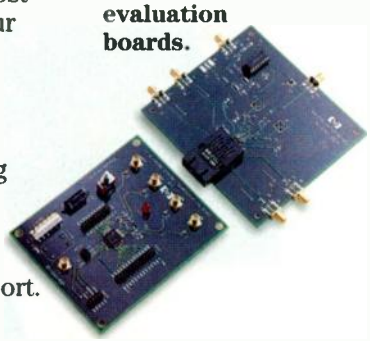
Add to this our 10-bit SERDES IC– a low-cost, low-power, field proven 3.3V bi-polar IC– and you have a complete, cost effective phy-layer solution for all your network interface needs.

Of course, both HP transceivers are Class-1 eye safe and continue in our tradition of providing industry-leading technology that results in lower-cost, technically advanced products– such as our 1.5GBd module– all with HP's superior service and application support.

Gigabit Ethernet from HP. Because we go the distance.

HEWLETT PACKARD

Sampling now! Call 1-800-537-7715 ext. 2260 for *free* product literature and a special offer for discounted evaluation boards.

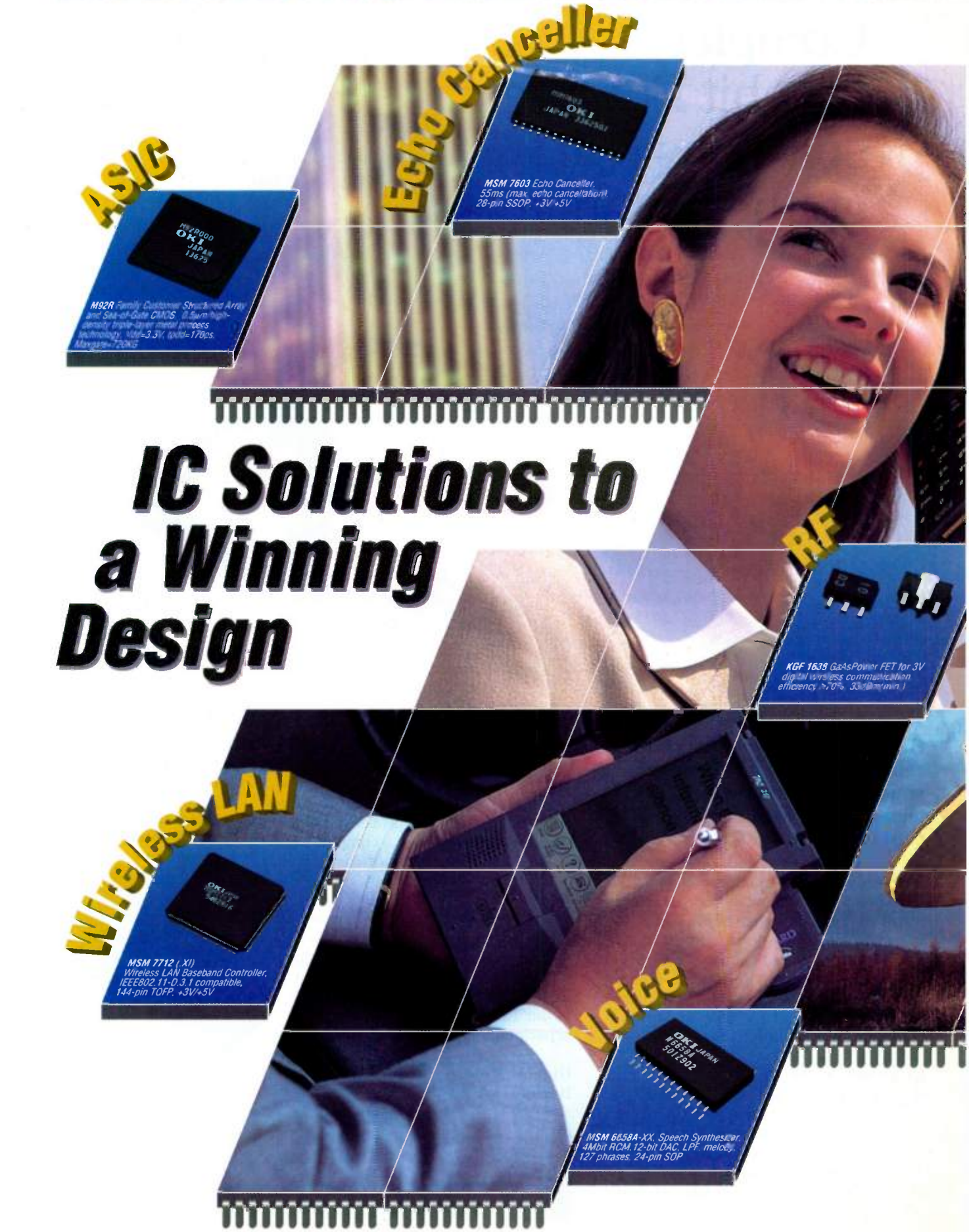


Visit our Web site at www.hp.com/go/fiber

Call 1-800-450-9455 for a list of technical literature available by fax (U.S. and Canada).

CGOC9701

READER SERVICE 105


Echo Canceller
MSM 7603 Echo Canceller, 55ms (max. echo cancellation), 28-pin SSOP, +3V/+5V
ASIC
M92R Family Customer Structured Array and Sea-of-Gate CMOS, 0.5um high-density triple-layer metal process technology, Vdd=3.3V, tpdd=170ps, Maxgate=720K
IC Solutions to a Winning Design
RF
KGF 1639 GaAsPower FET for 3V digital wireless communication, efficiency >70%, 33dBm(min.)
Wireless LAN
MSM 7712 (XI) Wireless LAN Baseband Controller, IEEE802.11-0.3.1 compatible, 144-pin TQFP, +3V/+5V
Voice
MSM 6658A-XX Speech Synthesizer, 4Mbit RCM, 12-bit DAC, LPF, melody, 127 phrases, 24-pin SOP

Optimizing products for a wireless world

If you're working on the "next big thing" in the wireless market, Oki will support you with key IC solutions from concept to assembly.

With 115 years experience in manufacturing telecommunication and information systems, Oki has the expertise to help you to complete a winning design.

In digital cordless phones, digital and analog cellular communications, wireless LAN, PCS and more, Oki devices enhance product value with special features that end users notice and appreciate. You'll find features such as clear and natural ADPCM sound, high-efficiency, high-output, ultra small GaAs chips; small, 3-V telecom LSIs and 3-5V flexible interface ASIC devices with equally flexible design support.

We will assist your effort with close, person-to-person partnership plus product development and field engineers dedicated to serving your needs.

Call Oki and finish on the winning side of wireless.

OKI
People to People Technology

For more information, Contact:

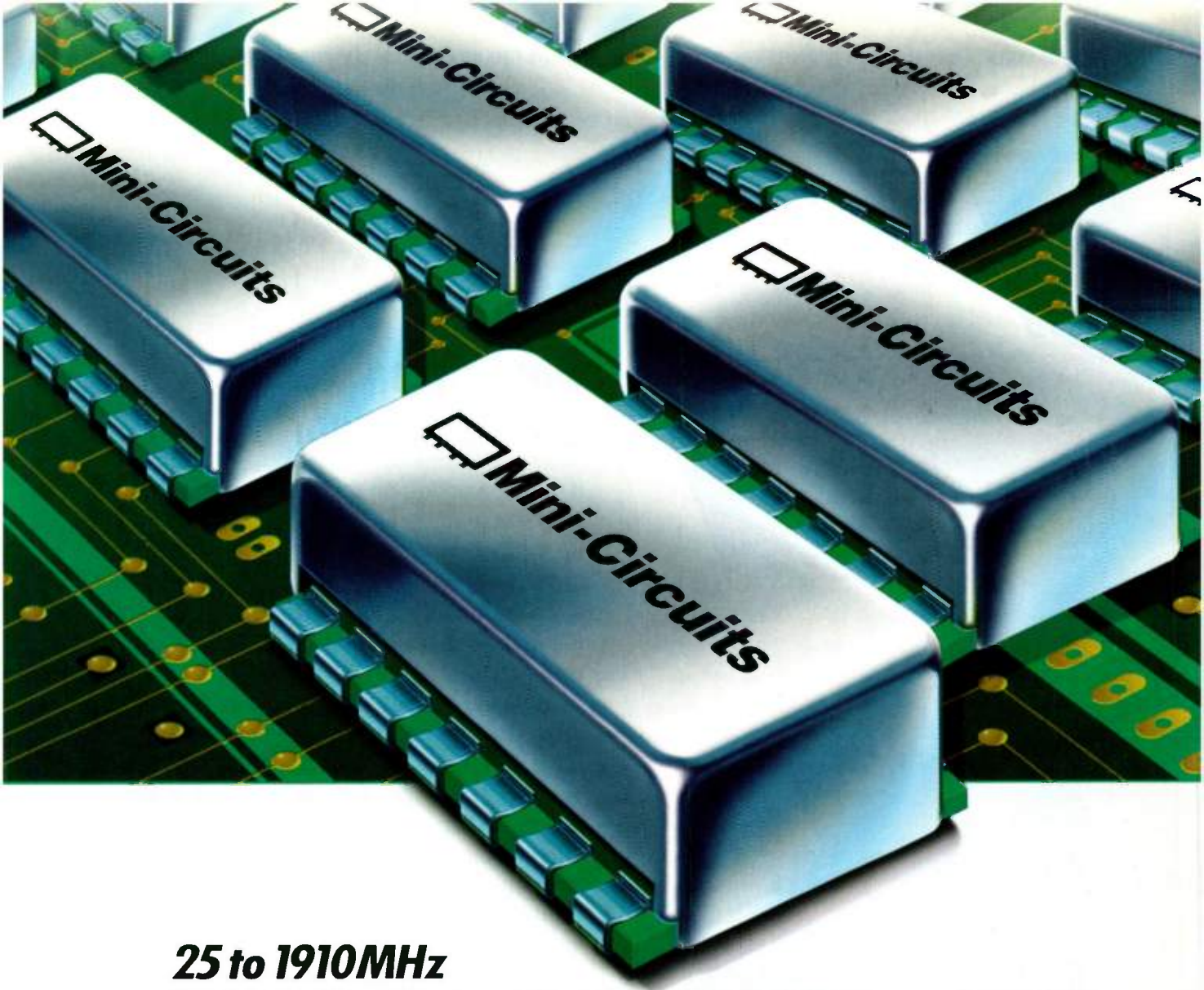
Oki Electric Industry Co., Ltd.
Electronic Devices Group,
Overseas Marketing Dept.
10-3, Shibaura 4-chome
Minato-ku, Tokyo 108, Japan
Tel: 81-3-5445-6000
Fax: 81-3-5445-6060

Oki Semiconductor Group
785 North Mary Avenue, Sunnyvale,
CA 94086-2909, U.S.A.
Tel: 408-720-1900
Fax: 408-720-1918

Oki Electric Europe GmbH
Head Office
Hellersbergstraße 2
D-41460 Neuss
Germany
Tel: 49-2131-15960
Fax: 49-2131-103539

Oki Electronics (Hong Kong) Ltd.
Suite 1901-9, Tower 3,
China Hong Kong City 33 Canton Road,
Tsim Sha Tsui, Kowloon Hong Kong
Tel: 852-27362336
Fax: 852-27362395

READER SERVICE 141



25 to 1910MHz

SURFACE MOUNT VCO's from $13.95

Time after time, you'll find Mini-Circuits surface mount voltage controlled oscillators the tough, reliable, high performance solution for your wireless designs. JTOS wide band models span 25 to 1910MHz with linear tuning characteristics, low -120dBc/Hz phase noise (typ. at 100kHz offset), and excellent -25dBc (typ) harmonic suppression. JCOS low noise models typically exhibit -132dBc/Hz phase noise at 100kHz offset, and phase noise for all models is characterized up to 1MHz offset. Miniature J leaded surface mount packages occupy minimum board space, while tape and reel availability for high speed production can rocket your design from manufacturing to market with lightening speed. Soar to new heights...specify Mini-Circuits surface mount VCO's.

ACTUAL SIZE

Mini-Circuits...we're redefining what VALUE is all about!

JTOS/JCOS SPECIFICATIONS

Model	Freq. Range (MHz)	Phase Noise (dBc/Hz) SSB@ 10kHzTyp.	Harmonics (dBc) Typ.	V_{tune}** 1V to:	Current (mA) @+12V DC Max.	Price $ea. (5-49)*
JTOS-50	25-47	-108	-19	15V	20	13.95
JTOS-75	37.5-75	-110	-27	16V	20	13.95
JTOS-100	50-100	-108	-35	16V	18	13.95
JTOS-150	75-150	-106	-23	16V	20	13.95
JTOS-200	100-200	-105	-25	16V	20	13.95
JTOS-300	150-280	-102	-28	16V	20	15.95
JTOS-400	200-380	-102	-25	16V	20	15.95
JTOS-535	300-525	-97	-28		20	15.95
JTOS-765	485-765	-98	-30	16V	20	16.95
JTOS-1025	685-1025	-94	-28	16V	22	18.95
JTOS-1300	900-1300	-95	-28	20V	30	18.95
JTOS-1650	1200-1650	-95	-20	13V	30	19.95
JTOS-1910	1625-1910	-92	-13	12V	20	19.95
JCOS-820WLN	780-860	-112	-13	20V	25 (@9V)	49.95
JCOS-820BLN	807-832	-112	-24	14V	25 (@10V)	49.95
JCOS-1100LN	1079-1114	-110	-15	20V	25 (@8V)	49.95

Notes: *Prices for JCOS models are for 1 to 9 quantity. **Required to cover frequency range. See "RF/IF Designer's Guide" or "VCO Designer's Handbook" for complete specifications.

DESIGNER'S KITS AVAILABLE
K-JTOS1 1 of each (10 pieces): JTOS-50, 75, 100, 150, 200, 300, 400, 535, 765, 1025, only $149.95
K-JTOS2 1 of each (7 pieces): JTOS-50, 100, 200, 400 535, 765, 1025, only $99
K-JTOS3 2 of each (6 pieces): JTOS-1300, 1650, 1910, only $114.95

Mini-Circuits®

US 132 INT'L 133
CIRCLE READER SERVICE CARD

P.O Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500 Fax (718)332-4661 *INTERNET* http://www. minicircuits. com
For detailed specs on all Mini-Circuits products refer to • 740- pg. HANDBOOK • INTERNET • THOMAS REGISTER • MICROWAVE PRODUCT DATA DIRECTORY • EEM
CUSTOM PRODUCT NEEDS...Let Our Experience Work For You.

F 234 Rev Orig

ELECTRONIC DESIGN

January 20, 1997 Volume 45, Number 2

EDITORIAL OVERVIEW

TECH INSIGHTS

ANALOG OUTLOOK

COVER FEATURE

ANALOG OUTLOOK

EDA

ELECTRONIC DESIGN (USPS 172-080; ISSN 0013-4872) is published twice monthly except for 3 issues in May and 3 issues in October by Penton Publishing Inc., 1100 Superior Ave., Cleveland, OH 44114-2543. Paid rates for a one year subscription are as follows: $105 U.S., $185 Canada, $210, $255 International. Second-class postage paid at Cleveland, OH, and additional mailing offices. Editorial and advertising addresses: ELECTRONIC DESIGN, 611 Route #46 West, Hasbrouck Heights, NJ 07604. Telephone (201) 393-6060. Facsimile (201) 393-0204. Printed in U.S.A. Title registered in U.S. Patent Office.

When you think of QT Optoelectronics, you probably think of optocouplers. But, QT is also a leading supplier of LEDs.

We've got a complete line of high-quality, reliable LED lamps and displays. And our authorized distributors — in hundreds of cities around the world — can deliver the products you need on time and at a good price.

Don't go barking up the wrong tree for your LEDs.

Call **800-LED-OPTO** today for more information and the phone number of your nearest QT Optoelectronics distributor.

READER SERVICE 161

QT OPTOELECTRONICS

United States 800-533-6786

France 33 01/43.99.25.12

Germany 49 089/96.30.51

United Kingdom 44 01296/39.44.99

Asia/Pacific 603/735-2417

YOUR TOP DOG FOR LEDs

ELECTRONIC DESIGN

January 20, 1997 Volume 45, Number 2

EDITORIAL OVERVIEW

EMBEDDED SYSTEMS

TEST AND MEASUREMENT

QUICKLOOK

DEPARTMENTS

COVER ILLUSTRATION BY: BRUCE JABLONSKI

Jesse H. Neal Editorial Achievement

1967 First Place Award	1978 Certificate of Merit
1968 First Place Award	1980 Certificate of Merit
1972 Certificate of Merit	1986 First Place Award
1975 Two Certificates of Merit	1989 Certificate of Merit
1976 Certificate of Merit	1992 Certificate of Merit

ELECTRONIC DESIGN

NORTH AMERICAN EDITION

Executive Editor: **ROGER ALLAN** (201) 393-6057 rallan@class.org
Managing Editor: **BOB MILNE** (201) 393-6058 bmilne@class.org

Technology Editors:

Analog: **PAUL McGOLDRICK** (San Jose) (408) 441-0550, ext. 113; 102447.346@compuserve.com
Analog & Power: **FRANK GOODENOUGH** (617) 227-4388 75410.2361@compuserve.com
Communications: **LEE GOLDBERG** (201) 393-6232 leeg@class.org
Components & Packaging: **PATRICK MANNION** (201) 393-6097 pcmann@ibm.net
Computer Systems: **RICHARD NASS** (201) 393-6090 richnass@class.org
Design Automation: **CHERYL AJLUNI** (San Jose) (408) 441-0550, ext. 102; cjajluni@class.org
Digital ICs: **DAVE BURSKY** (San Jose) (408) 441-0550, ext. 105; dbursky@class.org
Embedded Systems/Software: **TOM WIILIAMS** (Scotts Valley) (408) 335-1509 tomwillm@ix.netcom.com
Test & Measurement: **JOHN NOVELLINO** (201) 393-6077 jnovelli@class.org
New Products: **ROGER ENGELKE JR.** (201) 393-6276 rogere@csnet.net
Contributing Products Editor: **MILT LEONARD**

Editorial Headquarters:

(201) 393-6060 Fax: (201) 393-0204 E-mail: edesign@class.org
P.O. Box 821, Hasbrouck Heights, N.J. 07604

Field Correspondents:

West Coast Executive Editor:
DAVE BURSKY (San Jose) (408) 441-0550, ext. 105; dbursky@class.org
Western Regional Editors:
CHERYL J. AJLUNI (San Jose) (408) 441-0550, ext. 102; cjajluni@class.org
PAUL MCGOLDRICK (San Jose) (408) 441-0550, ext. 113; 102447.346@compuserve.com
TOM WILLIAMS (Scotts Valley) (408) 335-1509 tomwillm@ix.netcom.com
2025 Gateway Place, Suite 354, San Jose, CA 95110
(408) 441-0550 Fax: (408) 441-6052

London: **PETER FLETCHER**
16 Maylons Road, Hextable, Kent, UK
44 1 322 664 355 Fax: 44 1 322 669 829 E-mail: panflet@cix.compulink.uk.co

Munich: **ALFRED B. VOLLMER**
Eichenstr. 6, 82024 Taufkirchen (near Munich) Germany
49 89 614-8377 Fax: 49 89 614-8278 E-mail: 75162.1246@compuserve.com

Chief Copy Editor: **MICHAEL SCIANNAMEA** (201) 393-6024 mikemea@class.org
Copy Editor: **DEBRA SCHIFF** (201) 393-6024 debs@csnet.net
Consulting Editor: **LISA MALINIAK**
Ideas For Design Consulting Editor: **JIM BOYD**
Contributing Editors: **RON KMETOVICZ, ROBERT A. PEASE, WALT JUNG, HOWARD JOHNSON**
Production Manager: **PAT A. BOSELLI,** Production Coordinator: **WAYNE M. MORRIS**

Group Art Director: **PETER K. JEZIORSKI,** Associate Group Art Director: **TONY VITOLO**
Staff Artists: **LINDA GRAVELL, CHERYL GLOSS, JAMES M. MILLER**
Editorial Support Supervisor: **MARY JAMES**
Editorial Assistant: **ANN KUNZWEILER, BRADIE SUE GRIMALDI** (San Jose)

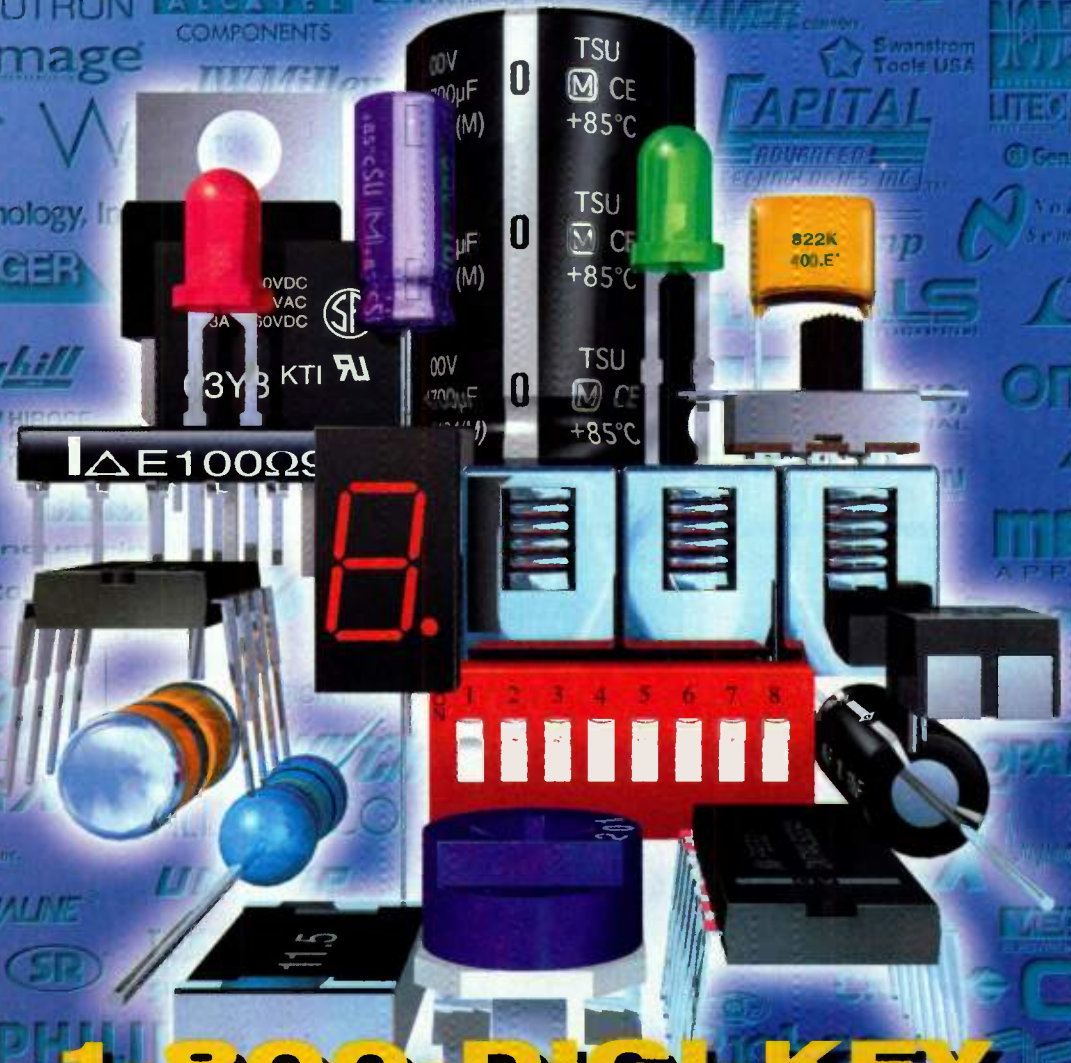
Advertising Production:

(201) 393-6093 or Fax (201) 393-0410
Production Manager: **EILEEN SLAVINSKY,** Assistant Production Manager: **JOYCE BORER**
Production Assistants: **MYLAN CHU, BARBARA LATORRE, DORIS CARTER, JANET CONNORS, LUCREZIA HLAVATY**
Circulation Manager: **BARBARA TILLETT** (216) 931-9158
Reprints: **ANNE ADAMS** (216) 696-7000, ext. 2626

Published by Penton Publishing

Electronic Design Information Group:
Editorial Director: **STEPHEN E. SCRUPSKI** (201) 393-6070
Publisher: **JOHN G. FRENCH** (201) 393-6055

One Source
One Solution
One Number



1-800-DIGI-KEY

Call, write, fax or visit us on the Internet for your FREE CATALOG today!

Digi-Key®

SUPERIOR QUALITY ELECTRONIC COMPONENTS SERVICE

Digi-Key Corporation, 701 Brooks Ave. South, Thief River Falls, MN 56701-0677

Toll-Free: 1-800-344-4539 • Fax: 218-681-3380

READER SERVICE 101

Visit us on the Internet • http://www.digikey.com

On orders entered by 5:00 pm central time

SAME-DAY SHIPMENT

JANUARY 1997

Asia & South Pacific Design Automation Conference with EDA Technofair (ASP-DAC '97), Jan. 28-31. Makuhari Messe Convention Center, Chiba, Japan. Contact Yoko Nishikawa, ASP-DAC '97 Secretariat, CONVEX Inc., Ichijoji Bldg. 2-3-22 Azabudai, Minato-ku, Tokyo 106 Japan; (81) 3 3589 3355; fax (81) 3 3589 3974; e-mail: convex@po.iijnet.or.jp; Internet: http://www.jesa or jp/ASPDAC/.

Second Annual Pan Pacific Microelectronics Symposium, Jan. 29-31. Sheraton Maui Resort, Maui, HI. Contact JoAnn Stromberg, Pan Pacific Symposium, 5200 Wilson Rd., Suite 215, Edina, Minnesota 55424; fax (612) 929-1819.

FEBRUARY

IEEE Aerospace Conference, February 1-8. Snowmass at Aspen, Colorado Contact Stephen Franklin, Deputy Program Chair, 4800 Oak Grove Drive, Pasadena, California 91109; (818) 393-0814; fax (818) 393-0530; e-mail: stephen.f.franklin@jpl.nasa.gov.; Internet: http://chirp.plk.af.mil:1050/ieee/index.html.

IEEE Power Engineering Society Winter Meeting, February 2-6. New York Hilton & Towers, New York. Contact Frank E. Schink, 14 Middlebury Ln., Cranford, New Jersey 07016-1622; (908) 276-8847; fax (908) 276-8847.

IEEE International Solid-State Circuits Conference (ISSCC '97), February 6-8. San Francisco Marriott Hotel, San Francisco, California. Contact Diane Suiters, Courtesy Associates, 655 15th St. N.W., Suite 300, Washington, DC 20005; (202) 639-4255; fax (202) 347-6109; e-mail: isscc@mcimail.com.

Third Annual Conference on Business Opportunities & Operational Requirements for Utilities in Telecommunications (Utilicom '97), Feb. 19-21. Washington Vista Hotel, Washington, DC. Contact (800) 822-6338 or (202) 842-3022 ext. 317, or http://www.brp.com.

Second International Conference on Chip-Scale Packaging, February 20-21. Sunnyvale Hilton Inn, Sunnyvale, California. Contact Subash Khadpe; (610) 799-0419; fax (610) 799-0519; e-mail: skhadpe@semitech.com.

(Actual size.)

One tiny footprint. A GIANT LEAP FOR POWER MOSFETS.

TEMIC's newest LITTLE FOOT® is the smallest power package available.

Part No.	Maximum Ratings V_{DS} (V)	$r_{DS(on)}$ (Ω) V_{GS} = 10 V	$r_{DS(on)}$ (Ω) V_{GS} = 4.5 V	I_D (A)	Gender
Si3454DV/X	30	0.065	0.095	±4.2	N-Ch
Si3455DV/X	30	0.100	0.19	±3.5	P-Ch
Part No.	**V_{DS} (V)**	**V_{GS} = 4.5 V**	**V_{GS} = 2.5 V**	**I_D (A)**	**Gender**
Si3442DV/X	20	0.07	0.095	±4.0	N-Ch
Si3441DV/X	20	0.10	0.135	±3.3	P-Ch

(Almost actual size.)

We've added an even smaller package to our popular line of LITTLE FOOT power MOSFETs, the TSOP-6. At one quarter the footprint of an SO-8 and with cool thermal characteristics, this new LITTLE FOOT MOSFET jumps way ahead of the competition for immediate application in portable phones and computers.

For today's ever shrinking designs, these TSOP-6 products are low enough in resistance and high enough in power to allow you to make small, high-efficiency dc/dc converters and power management circuits.

In fact, this new single LITTLE FOOT TSOP-6 has the same resistance and power ratings as today's standard, the dual LITTLE FOOT SO-8, which means less board space for equal performance. And since these new power MOSFET products are dual sourced by TEMIC and Motorola, we're already a step ahead of demand.

So take the first step toward your smallest, most efficient designs ever. Call your local TEMIC sales office today, or call **1-800-554-5565 ext. 515** for more information.

TEMIC
Semiconductors


S P G

It's no longer system-on-a-chip *or* time-to-market. With SPGAs, it's both.

System Programmable Gate Arrays... The new direction in high-level logic design.

Scream onto the new design highway called System Programmable Gate Arrays (SPGAs). Designing with programmable logic has never been like this!!

Talk about open road, SPGAs will begin at 50,000 gates and go up to 1,000,000. That's big enough to handle a complete system–logic, memory, and processor cores–on a single chip.

Take the express lane to fast time-to-market. SPGAs will be the most advanced, cost-efficient programmable targets for reusable soft IP blocks or hard-wired IP cores.

Drive your next system level design onto an SPGA. Feel the functionality, performance and cost-effectiveness never before achievable on a single programmable device.

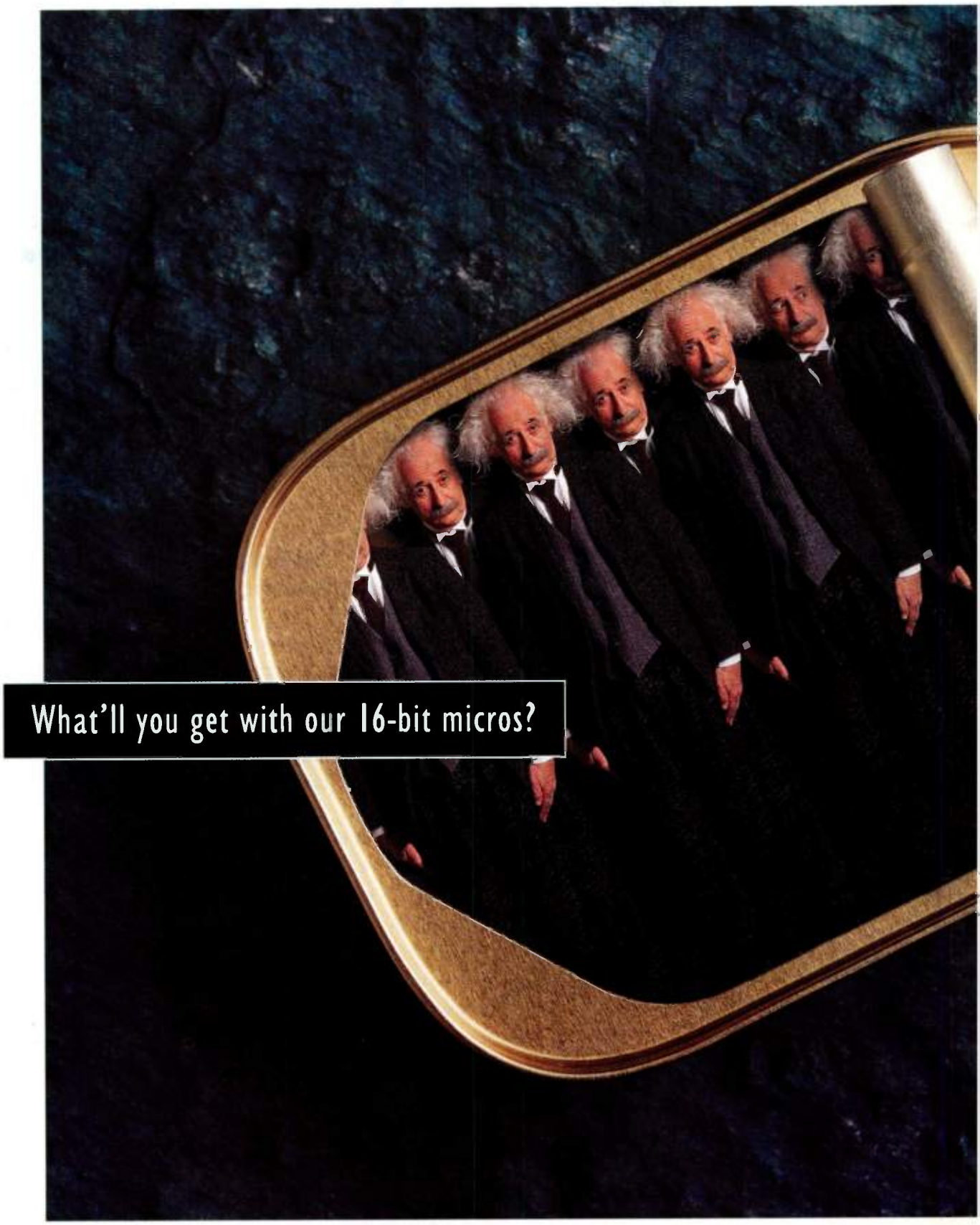
Follow the signs to SPGAs. It's the high road to fast time-to-market *and* system-on-a-chip design.

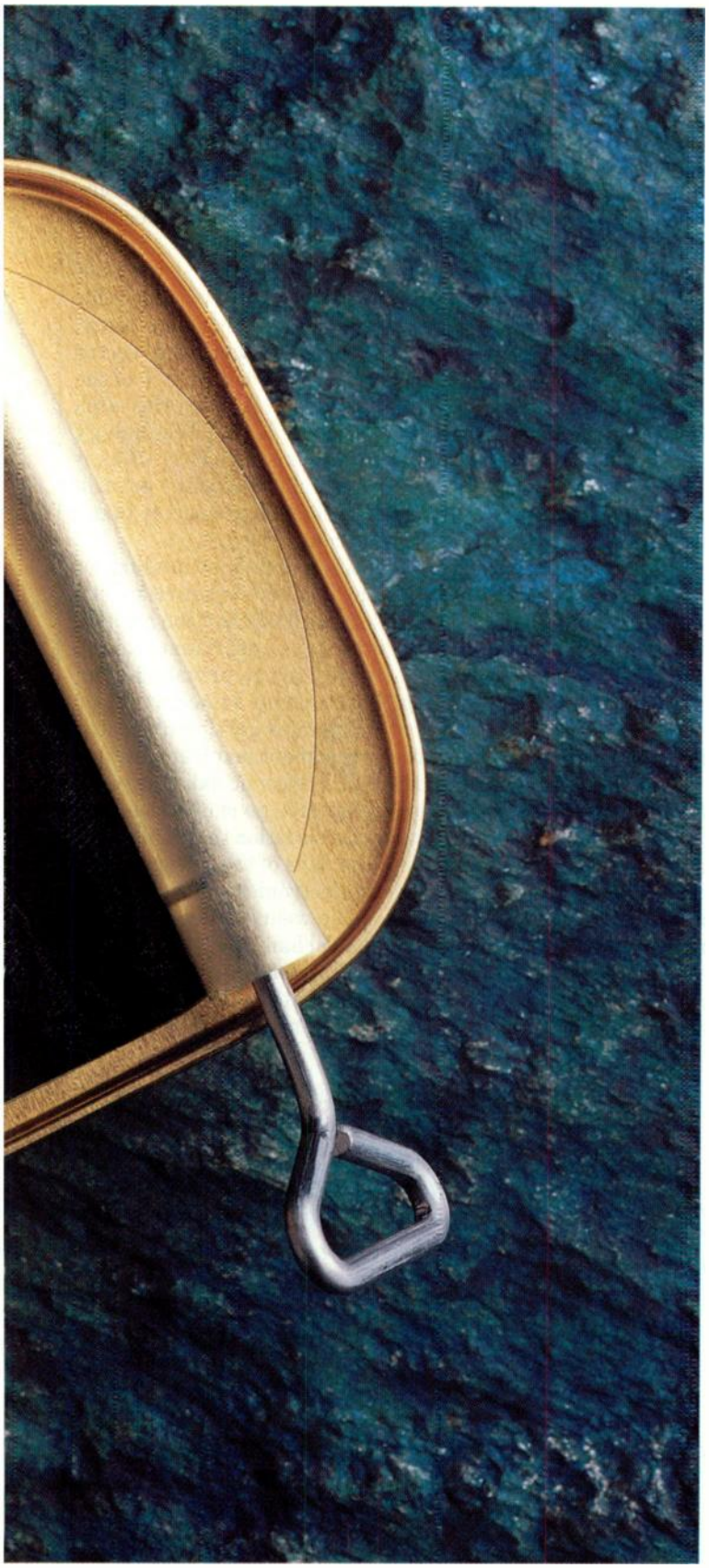
WWW.ACTEL.COM

To learn more about SPGAs, visit our Web site at *www.actel.com*.

Actel

Take it to a higher level.


What'll you get with our 16-bit micros?



More code efficiency

Our TLCS-900 microcontrollers save space by letting you write more instructions in the same memory block.

High performance

While on-board peripherals and a 25MHz clock rate take portable applications places they've never been.

Low power

With operating requirements from 2.7 to 5.5V, it's flexible enough for today's mixed-voltage world.

Highly concentrated intelligence

And has all the brainpower you need for those amazing new breakthroughs.

www.micro16.toshiba.com

TOSHIBA

TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC.

1-800-879-4963

ISO9001 CERTIFIED

EDITORIAL

The Government And R&D Funding

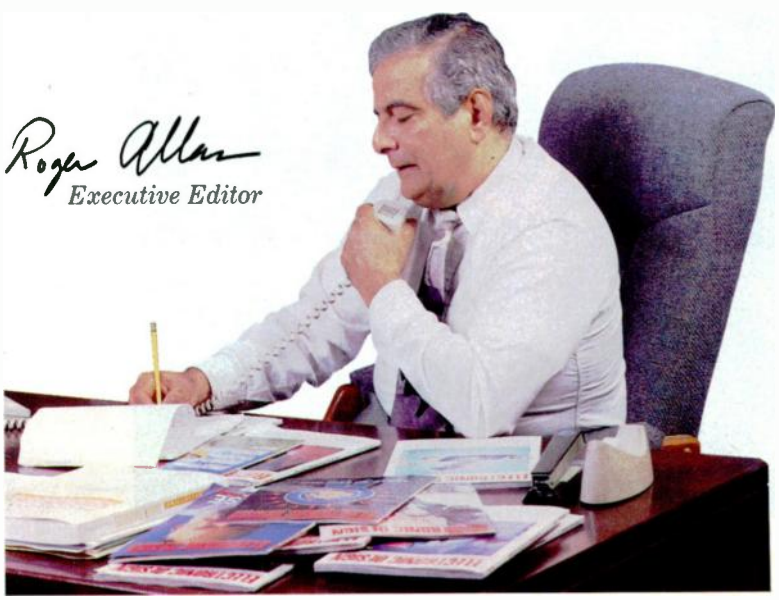
According to "Science & Engineering Indicators 1996," a U.S. National Science Foundation (NSF) publication, total R&D funding in the U.S. reached a high of $171 billion in 1995, representing a 2% real decline over 1990 funding. Moreover, federal outlays, representing 36% of total R&D outlays in 1995, have been falling annually since 1987. The report concludes that U.S. R&D funding can do better.

This is a troubling trend, especially at a time of tightening corporate budgets and the globalization of the economy. Unlike the U.S., R&D budgets for other countries have steadily increased, and many national, regional, state, and local governments are providing help to companies in the private sector to develop products for the commercial market. But in the U.S., much of the government's funding, provided via the NSF, the Defense Applied Research Agency (DARPA), the National Institute of Standards and Technology (NIST), and the National Aeronautics and Space Administration (NASA), is for the development of products and systems for the military and the government. The portion of the government's funding to the private sector to develop products for the commercial market pales in comparison.

Many in the private sector would argue against government funding for the private sector, correctly pointing out the many pitfalls they envision and examples of past government-sponsored "boondoggles." But how long can we really afford this "hands-off" approach? An industry consortium like Sematch, has shown that it can contribute positively to the private sector, thanks to some government funding. In this global economy, we seem to be on an uneven playing field, with many overseas companies getting unlimited government help while we cry out against any government involvement. Is it any wonder that technologies developed in the U.S. like semiconductor memories, robotics, flat-panel displays, TVs, and VCRs, have gone overseas, and have rapidly found applications in foreign markets, a situation that continues?

The U.S. economy has come a long way since the days of the space age and unlimited defense spending, when almost every electronics company had a government contract. Many private companies have weaned themselves off government funding for defense purposes and have channeled their efforts into profitable commercial markets. But that's no reason to espouse an inherent "distrust" of the government, as some in the private sector would have you believe. It's time to rethink this position before it may be too late. What do you think? *rallan@class.org.*

Roger Allan
Executive Editor



In Wireless Communications, Team Up With The Frontrunner.

That's Oki.

Competition is relentless in wireless design. So the best place to start is far ahead. With Oki. Whether you design products for use around the home, around town or around the world, only Oki has the advanced 3 Volt technology you need. Everything from CMOS baseband to the most efficient GaAs RF— complete system solutions for 3 Volt cordless, cellular and wireless LAN applications. No surprise. Oki's been offering wireless communications products from the industry's inception. That's why you find Oki's leading-edge technology in products from major communications manufacturers worldwide. Once you begin partnering with the wireless leader, you'll never look back. To find out more, visit our communications products corner, with application notes, on the Oki Web site at http://www.okisemi.com. Or call 1-800-OKI-6388.

Oki Semiconductor

SERIOUS PRODUCT

Contour Defibrillator
Manufactured by Ventritex, Inc.
Sunnyvale, CA

SPECIAL PROCESS, SPECIAL CUSTOMER

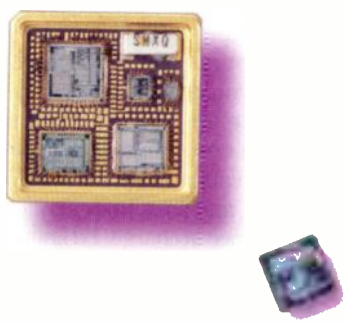
MANUFACTURING MADE SIMPLE

Orbit offers the total solution to your manufacturing needs by providing a unique combination of process development and manufacturing efficiencies. Whether you need ten or ten million pieces, Orbit's process development programs can significantly reduce your non-recurring engineering expenses. Our proven manufacturing expertise can provide production units in tested wafer form, raw die or packaged parts. We provide processes that meet or exceed the stringent requirements of either the aerospace/defense industry or the FDA. With our established on-site manufacturing facilities, Orbit is able to keep your manufacturing costs down, even at low volumes. And with a customer service organization that follows and protects your project throughout the entire manufacturing process, you have Orbit's total commitment.

We guarantee success. For more information contact Betty Newkirk, Vice President Customer Service or visit our web page at www.orbitsemi.com.

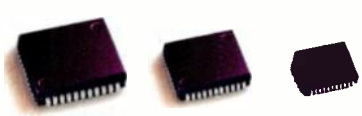
CONTRACT MANUFACTURING

SERIOUS SUPPLIER



TEN TO TEN MILLION PIECES

- 0.5µ - 5µ Processes
- Low NRE Costs
- Guaranteed Delivery*
- Military/FDA Standards
- Any Commercial Package
- Raw Die
- Tested or Untested Wafers



*Orbit provides financial guarantees on delivery dates See your Orbit representative for more details.

ORBIT SEMICONDUCTOR, INC.

A DII GROUP COMPANY

Orbit Semiconductor, Inc. 169 Java Dr., Sunnyvale, CA 94089 408-744-1800 Fax 408-747-1263 http://www.orbitsemi.com

800-331-4617

READER SERVICE 174

To Infinity And Beyond!

OK, call me a hypocrite, a supporter of corporate welfare, but I'm nuts for the space program. Despite its waste and inefficiency, I get a lump in my throat when watching a launch, knowing that it's *my* tax dollars that NASA's burning. When my sensible friends ask me to justify the billions spent on heaving a few dozen souls and a few tons of hardware into the void, I mumble pious words about technical spin-offs and scientific discoveries, but it's all nonsense. I've finally realized that the only honest justification for it is that it's a really cool thing to do—and that it gives us a chance to dream.

Of all the breakthroughs and marvels that the space program gave us, its biggest contribution may have been inspiring generations of nerdy kids to crack their books, do their homework, and dream about one day going to the stars. Like our athletic counterparts, most of us fell short of playing in the major leagues. But, a lucky few made it, with the rest of us cheering them on from the sidelines —and we were all better off for having made the attempt.

It would be great to give today's kids a chance to dream about the stars again. Somehow, NASA has to regain the public support and sense of purpose it had back in the sixties, and I've got a plan.

LEE GOLDBERG
Communications

The recent flurry of interest in Mars and the spectacular science the Hubble telescope is delivering makes us ripe for a renaissance of the space program. All that's needed is to gently nudge public opinion in the right direction and the politicians would be falling all over themselves to support the long-term programs that would lead us toward becoming a true spacefaring nation.

You can help by writing Dan Goldin, Director of NASA, and ask him to name me head of public relations. Once in charge, I'd launch a campaign to turn the space program into a spectator sport that rivals the popularity of baseball, football, or basketball.

First, I'd overhaul the NASA channel and market the distribution rights to the television networks. My version of launch coverage would be a blend of MTV and Monday Night Football, with a touch of Mr. Wizard. If the networks can make a bunch of guys knocking the stuffing out of each other look interesting, think of what we can do with something as exciting as a rocket launch!

Every launch would be covered with play-by-play analysis and the same mania for trivia that accompanies a baseball telecast. Coverage would begin an hour or more ahead, complete with color commentary from retired astronauts and scientists. As with other sports, they could analyze each team member's "stats" —number of missions, EVAs, total hours in space, etc. We could even compare them with their Russian counterparts. Can astronaut trading cards and NASA jerseys be far behind?

Rather than the bland, content-free babble that accompanies most launches, we could get lively, knowledgeable science personalities like Stephen Jay Gould or Bill Nye (The Science Guy) to interview NASA scientists and get plain-English explanations of the experiments to be conducted during the mission. And I'll bet that most aerospace companies would jump to pay for producing and airing videos that would give people a better understanding of the technical wizardry inside the launch vehicle or spacecraft that they've built. What about a national call-in show segment? Once we have viewership, the possibilities are endless.

If we start now, we can still give our children a chance to dream. We probably can't spend any more money on space each year than we do now, but a well-managed program with a long-range plan and public support could accomplish much in the next few decades. So get those cards and letters off to Mr. Goldin today! I look forward to seeing my child (and yours!) take her first steps onto the red sands of Mars. Comments can be sent to *leeg@class.org*.

OVER 100,000 PARTS IN STOCK, OVER 275 MANUFACTURERS, OVER 80 OFFICES NATIONWIDE!

1-800-433-5700

Allied Engineering Manual and Purchasing Guide

Multimedia Catalog on CD-ROM

24-Hour Modem Instant Access to Stock Inventory and Pricing: 1-800-433-5003

Same Day Shipment

On The Internet — Order Entry, Stock Inventory and Pricing: http://www.allied.avnet.com

ALLIED ELECTRONICS, INC.

AN AVNET COMPANY

READER SERVICE 164

Industry standard pin to pin capability has just landed!

Signal's new Low Profile Transformers deliver all these additional benefits at no extra cost:

- Construction designed to meet VDE/IEC/UL/CSA
- Hermetically sealed for wave soldering processes
- Encapsulated design provides superior protection in harsh environments
- Rigid pin construction for easier board insertion
- Mounting holes for easier installation and greater shock/vibration resistance
- Improved electrical characteristics including regulation, temperature rise, efficiency, etc.
- Dielectric strength test — 4000 VRMS Hipot

Add it all up and you simply won't find a low profile transformer that delivers all the benefits that Signal's does. Whether your product is designed for domestic or international markets, Signal's new low profile transformers deliver lower initial cost, lower installed cost and superior performance. Signal Transformer. Your competitive edge... around the world.

Call us for our detailed product literature and complete specs today.

Signal Transformer

Signal Transformer Co., Inc.
Insilco Technologies Group
500 Bayview Avenue
Inwood, NY 11096-1792
Call: 516-239-5777
Fax: (24 hrs) 516-239-7208

READER SERVICE 150

Chip Speeds Genetic Studies With Its Gene-Scanning Ability

Genetic discoveries may arrive at a much more furious pace thanks to a new technique that gathers clues about the functions of thousands of different genes all at once. Stanford University researchers use what's called a "GeneChip," which is a thumbnail-sized silicon chip designed to carry a neat array of up to 100,000 DNA fragments.

The researchers are labeling the thousands of genes that make up an organism with distinguishing DNA tags. These will serve as "molecular bar codes" that can be detected simultaneously using the GeneChip. The technique should hasten the process and reduce the cost of key research areas, such as disease diagnosis, basic biological research, and the hunt for new drugs to fight infections.

The actual GeneChip, developed by Affymetrix, Santa Clara, Calif., combines two powerful technologies—photolithography methods used in the semiconductor manufacturers to layer microscopic structures on small silicon chips, and standard DNA-making techniques perfected by genetic researchers. With the chip's bar-code reading capability, scientists will be able to figure out which genes are important for survival under particular environmental conditions or at a given moment in an organism's life.

One of its first applications will be to determine the function of the estimated 6000 genes that are in baker's yeast. The reason yeast was chosen because its the most complex organism whose entire genetic sequence is already known. For more information, contact Stanford's Medical Center at (415) 725-5374 or (415) 723-6912. *RE*

Acoustic Methods Used To Identify Defective Heart Valves

Money granted from a class-action lawsuit settled in 1994 was poured into a research project that now may wind up helping thousands of people. Studies at Lawrence Livermore National Laboratory, Livermore, Calif., along with other research institutions, have focused on using acoustic differences to identify which mechanical heart valves manufactured by Shiley Inc. are susceptible to failure.

The recurring problem with Shiley Inc.'s Bjork-Shiley Convexo-Concave heart valves are "single leg separations," which occur when one leg of the valve's outlet strut breaks free. When both legs break, the strut is said to fracture, a condition that causes the heart valve to lose control of blood flow to the heart. Consequently, the research, funded by Shiley through the lawsuit, is to detect, without surgery, such separations of the valves. As of November 1996, there were 596 reported fractures of these heart valves, which lead to death in about two of three cases. About 42,500 convexo-concave valves (marketed between 1979 and 1986) are estimated to be implanted in patients now living.

Livermore's research project is split into two parts. First, there's an underwater study of the sounds made by normal and separated values. Scientists are studying the sounds of the two valves in an echoless chamber to observe how the values sound apart from biological sounds, such as fluids, heart beats, or tissue.

The second part involves a "blind test" with approximately 40 people using audio recordings to identify the different valves. The recordings were made by placing a microphone on the subject's chest and then using a digital audio tape to record, over a three-minute span, the opening and closing sounds of their heart valves.

"Finding the opening sound caused by a single leg separation heart valve is somewhat like searching for a single violin string that is out of tune in an entire orchestra of sounds," says Jim Candy, project co-leader. "It requires sophisticated signal-processing techniques to extract this sound because it is deeply buried in the noise." So far, Livermore engineers have employed computer workstations to pore through nearly 13 billion bytes of heart-valve acoustic data, the equivalent of almost 11,000 novels. *RE*

Hardware Vendors Can Develop Hot-Pluggable PCI Systems

Independent hardware vendors (IHVs) can take advantage of the Hot Plug PCI development platform to build PCI cards that can be installed in backplanes without powering down the entire system. This type of system would include fault-tolerant servers that can't tolerate any down time. Such functionality was previously available in proprietary platforms.

The development platform lets the IHVs develop their PCI-based software drivers. Engineered by Compaq Computer Corp., Houston, Texas, the platform is being delivered simultaneously with the first draft of a specification to create an open standard for hot-plug PCI technology. The draft, called Hot Plug Replacement, has been submitted to the PCI Hot Plug workgroup for review. Follow-on standards, specifically the Hot PCI Upgrade and Hot PCI Expansion, will make it possible for users to upgrade existing PCI peripherals and drivers without having to power down their systems. For more information, contact Compaq at (800) OK-COMPAQ, or on the Internet at http://www.compaq.com. *RN*

I_2O Systems, Peripherals, And Software Are Starting To Arrive

The Intelligent I/O (I_2O) architecture improves I/O throughput and overall system performance by relieving host resources, such as the microprocessor, memory, and system bus, of interrupt-intensive tasks that cause data bottlenecks. Defined as a software layer, I_2O also provides an open, standards-based approach for intelligent I/O subsystems.

Systems based on I_2O now are starting to appear on the market. Recently, vendors participated in a demonstration sponsored by the I_2O Special Interest Group (SIG) to show their compatible products. The products included servers developed by Compaq and Hewlett-Packard; networking and storage devices from Adaptec, 3Com, and Symbios Logic; and operating systems from Microsoft, Novell, and SCO. Most of the products on display will be available in the early part of this year. For more information about I_2O, contact the SIG at (415) 750-8352 or on the Internet at http://www.i2osig.org. *RN*

New Class Of Polymer To Boost Low-Cost MCM Manufacture

A new class of packaging materials derived from polymers of cyclic olefins is being developed by the low-cost MCM research area of Georgia Tech. According to Dr. Paul A. Kohl and Dr. Sue Ann Bidstrup, both faculty members of the School of Chemical Engineering, the unique properties of these polymers are characterized by; a Tg (glass transition temperature) greater than 350°C, dielectric constant of less than 2.4 to 2.6, low moisture absorption of 0.1 %, and good ductility.

The materials were modified to have excellent adhesion to commonly used materials such as silica and aluminum, while also fusing well with copper and noble metals like gold and silver. The polymers require no adhesion promoter or adhesion layer such as titanium, tantalum, or chromium, and they do remain as adherent films even after being placed in boiling water for two hours.

Sponsored by BF Goodrich and conducted by Bidstrup and a group of graduate students, the results of the research are expected to "demonstrate utility in both semiconductors and packaging by offering superior performance over traditional materials, while reducing manufacturing cost," says Kohl. Contact Dr. Paul A. Kohl at (404) 894-2893 or paul.kohl@che.gatech.edu; or Dr. Sue Ann Bidstrup at (404) 894-2872 or sue.allen@che.gatech.edu. *PM*

All-Silicon System Processes Light As Well As Electricity

For the first time, engineers were able to integrate a porous silicon LED into conventional microelectronic circuitry, making possible an all-silicon system that can process light and electricity. A team of engineers from the University of Rochester and the Rochester Institute of Technology (RIT), both from N.Y., achieved this milestone by creating a sturdier form of porous silicon that can withstand the rigors of today's manufacturing environment. It's the first time that silicon was used for both the electronic and optical components on a single chip. Consequently, this eliminates the need for other materials or special processes during fabrication.

Of course, silicon has become synonymous with much of the electronics industry (read: Silicon Valley). But, as is also well known, it does have one major flaw—it emits light rather feebly. This flaw has magnified of late as scientists turn to light to carry the increasing amount of digital data traveling worldwide. To meet such a demand, companies have laid miles upon miles of fiber-optic cable because it transmits significantly more information cleaner and faster than electricity.

To provide these optical capabilities, engineers have turned to gallium arsenide or organic polymers, but they're costlier and/or extremely fragile. When porous silicon arrived on the scene in 1990, there was much anticipation because it could emit light. However, the porosity was too fragile to withstand conventional manufacturing techniques, rendering virtually useless to the electronics industry.

The Rochester team finally was able to strengthen the material by removing hydrogen atoms from the outer layer of tiny silicon nano-particles less than 100 Å wide—about one-thousandth the width of a human hair. They replaced the hydrogen with a double layer of silicon oxide to create a modified form of porous silicon known as silicon-rich silicon oxide. With these steps, the material, which is about three-quarters air and only one-quarter silicon, can withstand temperatures of 900°C, which is typically reached in the fabrication process.

The group holds the record for the most stable porous silicon LED. They were able to power the device for 11 straight days before stopping the experiment. Its brightness was about 1 mW per square centimeter and could flash up to 10 million times per second.

According to Philippe Fauchet, leader of the group, more improvements are needed before porous silicon becomes a standard material. For instance, researchers are looking to boost the efficiency 10-fold (to 1%), and increase frequency 100-fold, to one billion flashes per second. *RE*

The C.A.N. Transceiver Everybody Likes

...From The Linear IC Company Everybody Follows

Device networks just got better with our new **UC5350** C.A.N. compatible transceiver. Everybody likes this rugged plug and play network solution because it saves money, reduces design time, increases production line reliability and minimizes down time. With the UC5350, cross-wiring and loss of ground device faults will no longer destroy costly systems, causing extended line down situations. And no other C.A.N. transceiver meets the industrial node protection standards while minimizing per node propagation delay and signal loading. You can't afford not to update your network, and the new UC5350 makes automating more affordable than ever before.

For free samples and application information call today!

The UC5350 Advantage

- ISO 11898, SDS, DeviceNet Compatible
- Cross Wire Protection
- Loss of Ground Protection
- 50nS Propagation Delay Maximum
- 30kohm Minimum Input Impedance

UNITRODE

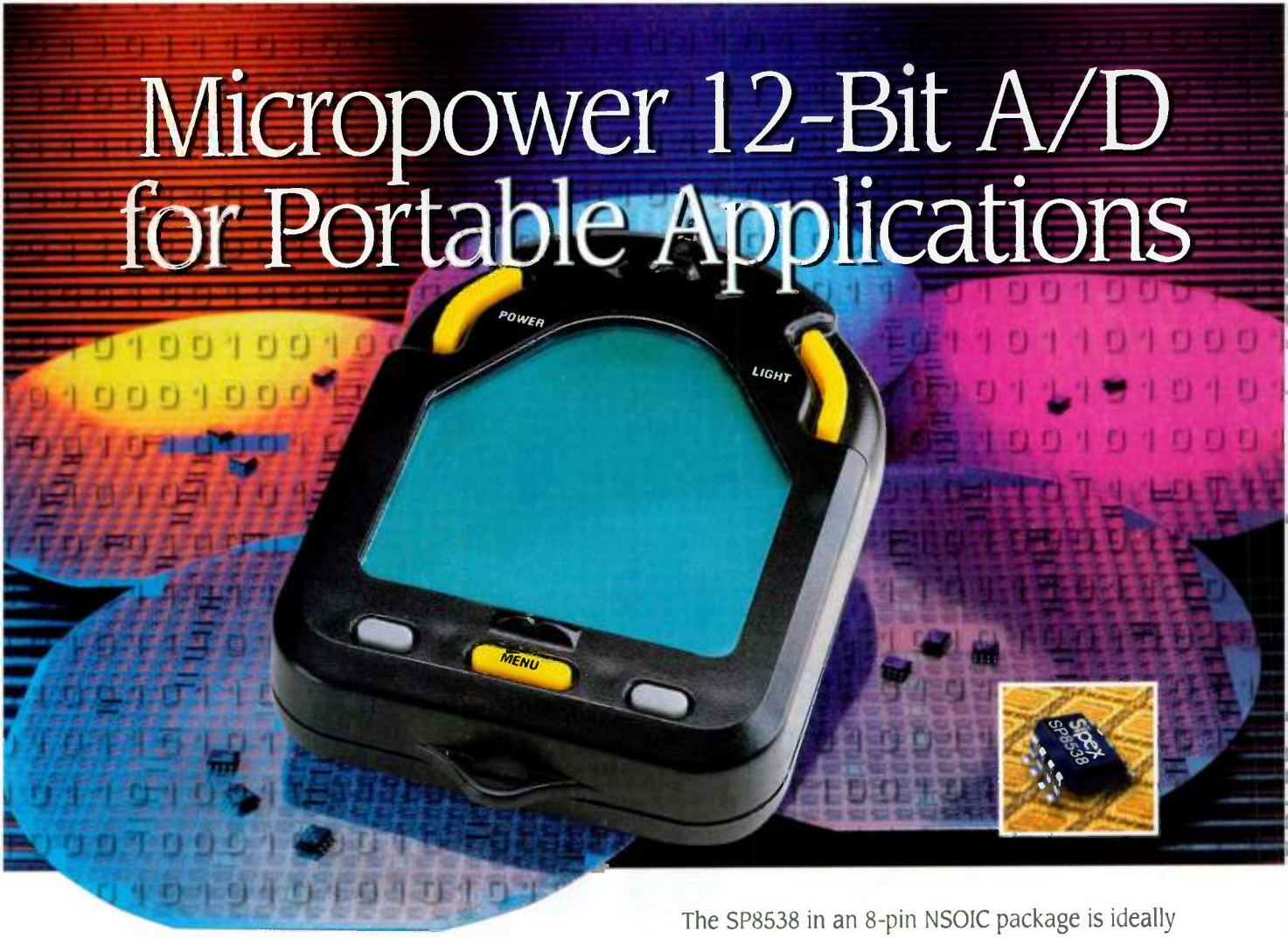
TEL: (603) 429-8610

http:/www.unitrode.com • FAX: (603) 424-3460

7 Continental Boulevard • Merrimack, NH 03054

READER SERVICE 155

Micropower 12-Bit A/D for Portable Applications



Introducing the new SP8538, 12-bit ADC that redefines price/performance leadership in the micro-power range. It delivers dynamic performance of

Benefits	Sipex	Linear Tech	Condition
Cost	$4.20	$5.20	@1k qty
Power	0.56mW	2.2mW	@5v and 90µs
Complete Cycle Time	40µs	90µs	@5v
Inputs	True Differential	Pseudo Differential	
Linearity	1 LSB	2 LSB	
Crosstalk	-120dB	-66dB	CH1 = 1MHz sqr wave, CH0 = 4.5v

SP8538 is a direct replacement for (Linear Tech) LTC 1298.

73dB Signal to Noise Ratio at a mere 1.25mW. Plus, the simple 3-wire SPI serial interface works easily with a wide range of microprocessors and micro-controllers. Noisy environments? The SP8538 with its "True" differential inputs and a Common Mode Noise Rejection (CMR) of 110dB @ 60Hz is the solution to your problem.

The SP8538 in an 8-pin NSOIC package is ideally suited for Battery-Operated Systems, Portable Data Acquisition Instrumentation, and Remote Sensing.

If your application calls for best-in-class performance at micropower, you need to select an IC from SIPEX's broad line of 12 Bit A/D and D/A converters. For data sheets and technical information, contact SIPEX at the number or web site listed below.

Sipex

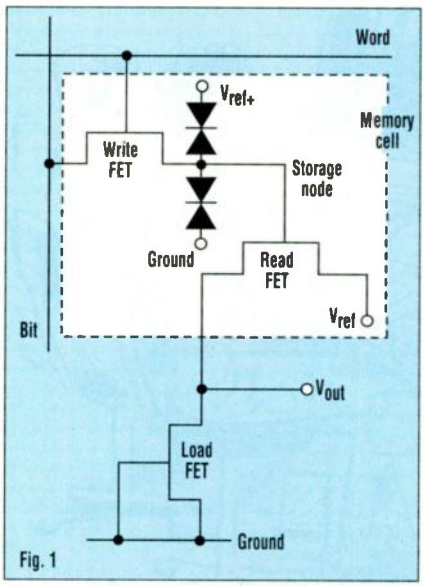
22 Linnell Circle, Billerica, MA 01821
Tel. 508-667-8700 Fax 508-670-9001
web site: www.sipex.com

READER SERVICE 151

Low-Standby-Power SRAM Cell Promises High-Density Memories

Researchers at Texas Instruments Inc., Dallas, have devised an advanced memory cell that reduces the standby power of static-RAM memory cells used in III/V- or silicon-based circuits. The development promises to allow much higher levels of integration for high-speed circuits. The advanced memory cell consumes a record low 50 nA of standby current (almost 100 times less than currently achieved). Although initially fabricated on an indium-phosphide (InP) substrate, the same approach, according to the researchers, will be readily transferable to gallium-arsenide (GaAs) technology, since the materials have similar characteristics.

Described at last December's International Electron Devices Meeting (IEDM) in San Francisco, Calif., the cell, referred to as a tunneling-based SRAM, combines two heterostructure field-effect transistors—a read FET and a write FET—and two resonant-tunneling diodes *(Fig. 1)*. The low-current-density resonant-tunneling diodes are used in a latch configuration to create two stable voltage levels in the storage node. The diodes are connected to the gate of an HFET, which can easily drive the bit line while not disturbing the storage node. When the word line is low (the cell is not selected), the gate leakage of either the write-HFET or the read-HFET steers the storage node voltage either low or high, depending on which of these currents is larger.



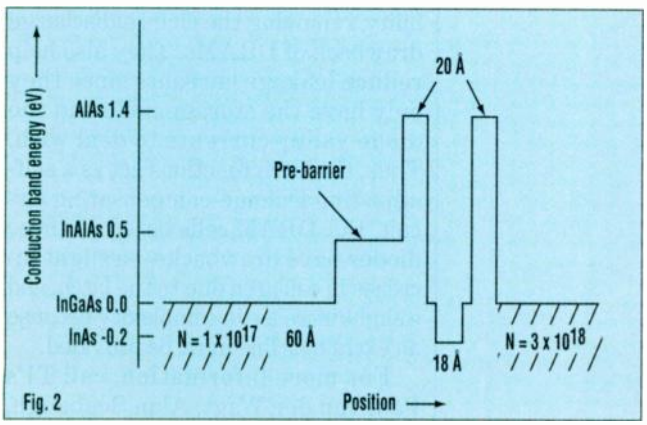
1. A simple static ram cell with ultra-low standby power can be created with just two heterostructure FETs and two resonant-tunneling diodes.

The resonant-tunneling-diode latch can maintain two stable storage node voltage levels as long as the diode peak current is larger than the HFET leakage currents plus a diode valley current. This structure keeps the leakage currents to less than 100 nA for the read HFET device with a gate area of 50 by 0.5 μm^2, and less than 10 nA for the 5-by-1-μm^2 gate write HFET (-2 V< V_{GS} <0 V, and V_{DS} <1 V). Additionally, the diode currents hit peak values of just over 150 nA.

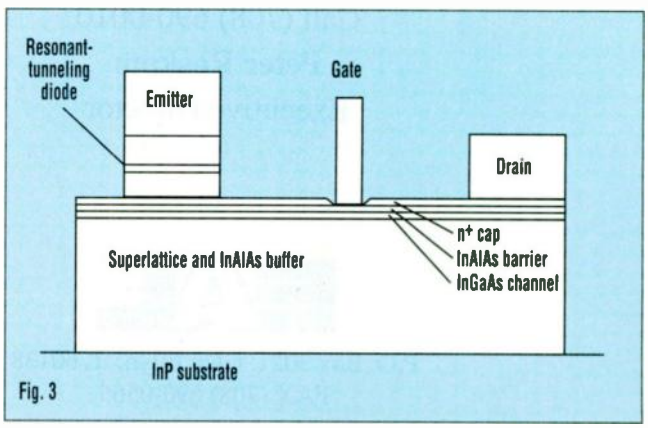
Although the initial cell structure provides two states (1 bit), a three-state version of the cell also can be implemented by increasing the number of vertically-integrated resonant-tunneling diodes. This arrangement allows the designer to achieve even higher storage densities. The same techniques can be applied in any materials system in which low-current-density, negative-differential-resistance devices can be fabricated. Assuming that such devices can be fabricated in silicon, the addition of two resonant-tunneling diodes to a DRAM cell converts the cell into an SRAM cell. That, in turn, can dramatically reduce the power waste associated with the refresh operation—a problem that is looming as chip densities approach the gigabit domain.

The resonant-tunneling diodes form the heart of the low-power memory cells, and are the critical elements that must be fabricated. To build the structures, TI's designers incorporated pseudomorphic aluminum-arsenide (AlAs) barriers, an indium-arsenide (InAs) well, and an indium-aluminum-arsenide (InAlAs) thin pre-barrier for current reduction *(Fig. 2)*. The peak current density depends exponentially on the pre-barrier thickness.

To fabricate the cell, TI's designers crafted a new process that allows them to monolithically form both the HFETs and the diode structures in the indium-gallium-arsenide/indium-aluminum-arsenide (InGaAs/InAlAs) materials on top of an InP substrate *(Fig. 3)*. The process also incorporates various improvements over previous processes that reduce, by an order of magnitude, the HFET gate leakage



2. The conduction bands of the pseudomorphic resonant-tunneling diodes show the half-step energy band value of the pre-barrier layer.



3. The combined HFET and RTD structures are formed on the surface of a superlattice and buffer layer of InAlAs deposited on an InP substrate.

SRAM CELL

current, setting a new low.

For high uniformity, selective etches are performed to create the diode mesas as well as the HFET channel recesses. Non-alloyed contacts—TiPtAu and InP etch-stop layers—provide a uniform, reproducible, and low-leakage process.

When applying this concept to DRAM cells, most of the attention is focused on reducing power during refreshing since the cells already have a low intrinsic leakage current. During refreshing, most of the power is consumed by the charging/discharging of the bit lines, and by the small percentage of cells that end up with the worst-case leakage-current variances. Additionally, the refresh operations must be able to function at 85°C.

The conceptual DRAM cell combines a standard single-transistor storage cell, plus the resonant-tunneling-diode latch connected at the same point as the storage capacitor. To function, the diodes must have extremely low current densities. However, silicon resonant-tunneling diodes do not yet exist, although research at TI into such structures is currently underway. Both the read and write operations execute exactly the same as the read and write in the standard DRAM cells. The difference lies in the storage function. A resonant-tunneling-diode latch has two stable voltage points, and as long as its peak current is larger than the total leakage current of the storage node plus the resonant-tunneling-diode valley current, the diodes will hold the storage node close to one of the two stable points.

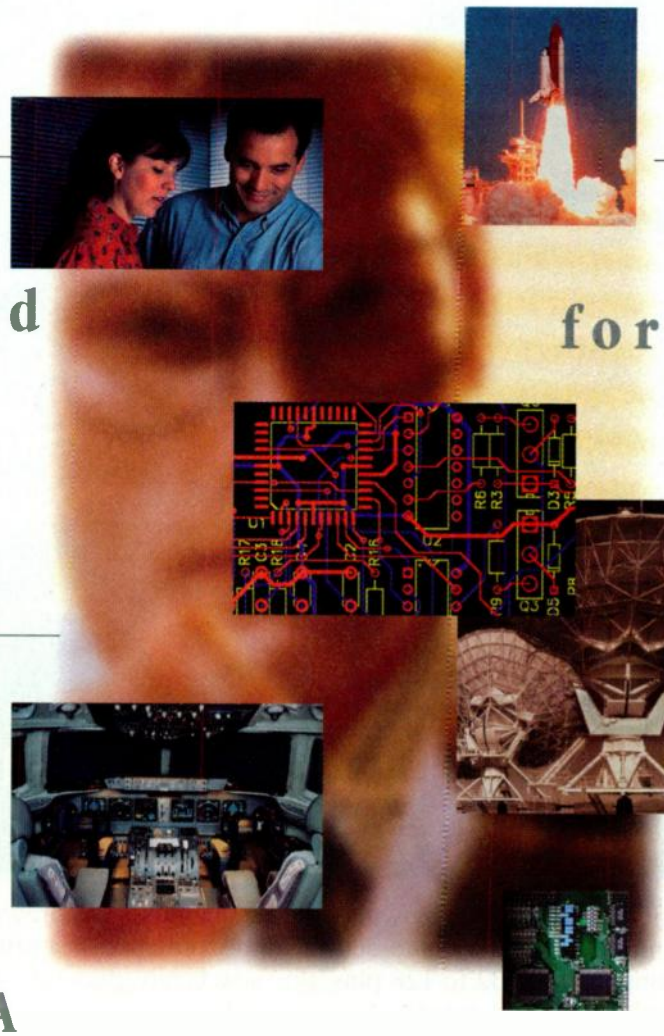
The resonant-tunneling diodes provide a local continuous refresh capability, removing the charge/discharge drawback of DRAMs. They also help reduce leakage currents since they only have the storage node and the diode valley currents to deal with. Thus, the latch functions act as a self-adjusting leakage-compensating circuit. But DRAM cells based on these diodes have drawbacks—a slight increase in cell area due to the latch, and a slight increase in complexity because an extra bias line must be provided.

For more information, call TI's Paul van der Wagt, Alan Seabaugh, or Ed Beam II at (972) 995-2011.

Dave Bursky

Designers set standards for excellence in our most critical industries. Often, lives and livelihoods depend on the circuits you design. Your goal: design better circuits faster. Since our inception, MicroSim has been setting the standards for desktop EDA systems that enable you to do just that. Try our evaluation software. See how MicroSim can help you set tomorrow's standards.

Setting the standard for desktop EDA



SCHEMATIC ENTRY

ANALOG/DIGITAL SIMULATION

PROGRAMMABLE LOGIC SYNTHESIS

PC BOARD LAYOUT

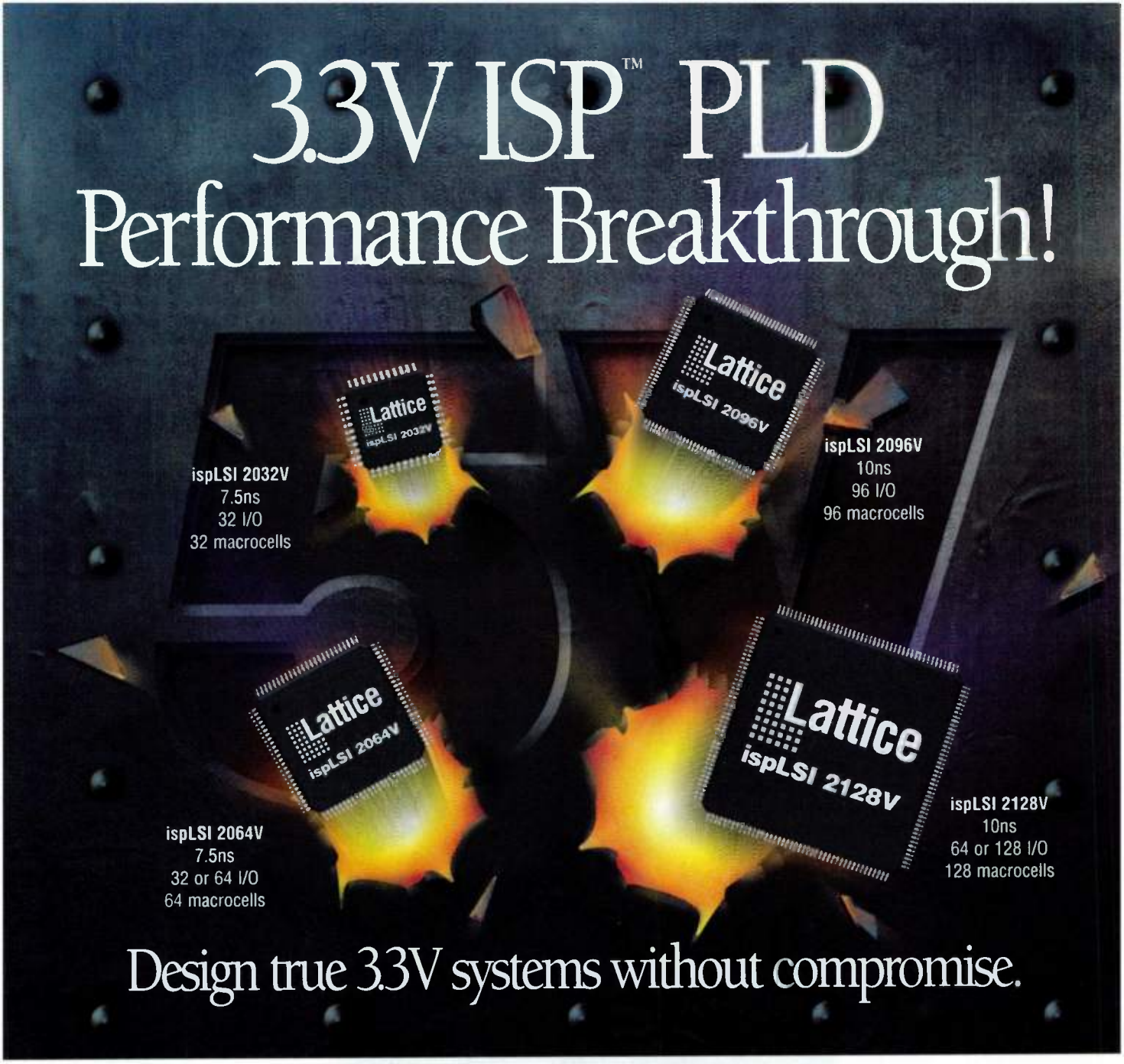
MicroSim®

Contact MicroSim at 1.800.245.3022 *or* 714.770.3022

You can visit our Web site: http://www.microsim.com *or call our faxback number:* 714.454.3296 *E-mail:* sales@microsim.com

READER SERVICE 300

3.3V ISP™ PLD Performance Breakthrough!



Design true 3.3V systems without compromise.

Smash the 3.3V high-density PLD speed barrier with Lattice's new in-system programmable ispLSI® 2000V Family—the first 3.3V programmable logic devices to deliver 5V performance. Featuring logic densities from 32 to 128 macrocells and I/O options from 32 to 128 pins, this new family gives you all the logic options you need to design 3.3V systems with breakaway speed.

FREE
ISP™ Design Software & Lattice ISP™ Encyclopedia

Includes: Software, Data Book, Handbook, ISP Manual on CD-ROM

All ispLSI 2000V devices are available in space saving thin quad flat pack (TQFP) packages that maximize PCB space. And every ispLSI 2000V device is in-system programmable using only a 3.3V power supply—an industry first! So manufacturing with high-density ispLSI devices saves you both time and money.

Give yourself a break and come up to speed with ispLSI 2000V PLDs. Call us today at **1-888-ISP-PLDS** and ask for information packet 331 or check out our web site at **www.latticesemi.com.**

Lattice™ Semiconductor Corporation

The Leader in ISP™ PLDs

Corporate Headquarters: Tel: (503) 681-0118, Fax: (503) 681-3037 • **France:** Tel: (33) 1 69 33 22 77, Fax: (33) 1 60 19 05 21 • **Germany:** Tel: (49) 089-317-87-810 Fax: (49) 089-317-87-830 • **Hong Kong:** Tel: (852) 2319-2929, Fax: (852) 2319-2750 • **Japan:** Tel: (81) 3-5820-3533, Fax: (81) 3-5820-3531 • **Korea:** Tel: (822) 583-6783, Fax: (822) 583-6788 • **Taiwan:** Tel: (8862) 577-4352, Fax: (8862) 577-0260 • **United Kingdom:** Tel: (44) 1932 831130, Fax: (44) 1932 831181

TECHNOLOGY INSIGHTS

Exploring power-management design issues for advanced microprocessors

Advanced Microprocessors Demand Amperes Of Current At <2 V

Switching-Regulator Controllers Drive Power MOSFETs To Provide Regulated Power For Advanced Microprocessors At 1.3 To 3.5 V.

Frank Goodenough

SPECIAL REPORT

Gate lengths for CMOS FETs in advanced microprocessors have shrunk rapidly in the last two years. This trend has followed the roadmap drawn by the Semiconductor Industry Association (SIA) for semiconductor device growth. Coupled with the demand for lower power, supply rails have dropped. Cutting supply voltages cuts the loss factor V (volts) in the equation:

$P = 1/2f\,CV^2$

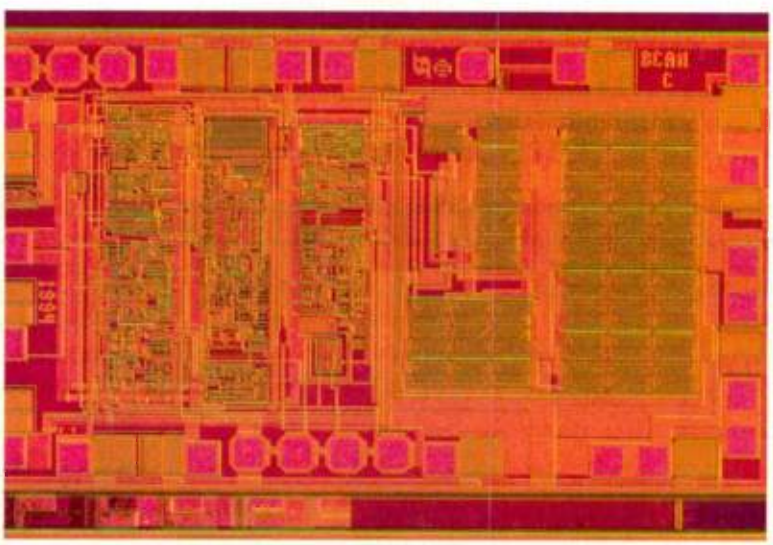
where

P = power dissipation

f = frequency (clock rate)

V = voltage

Both the f and the number of FETs per processor, as well as the supply currents, keep climbing at similarly fast rates. That is, power does not usually fall. The extra FETs use more current while enabling the processor to perform additional sophisticated functions.



Courtesy: Temic Semiconductor

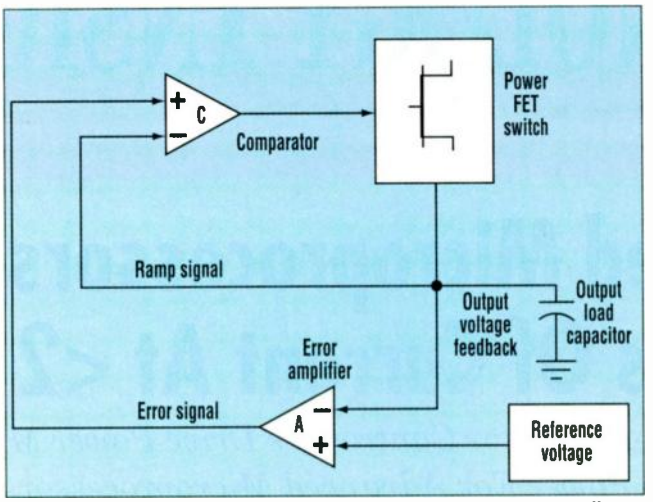
Complicating matters further at the system design level, Intel, since it introduced the Pentium, has let each microprocessor determine its own supply voltage. The P-6 Pentium Pro has four pins, each of which is either open or shorted. They represent a 4-bit code that calls out the supply voltage required by the processor in 100-mV steps between 2.1 and 3.5 V. The supply must read the code and provide the required voltage. Five-bit codes are on the way in next-generation processors.

To make the task of the system designer a little simpler, Intel has defined a family of standard plug-in supplies for their processors called voltage regulator modules (VRMs). The VRM reads the code and sets the output voltage (*see "VRMs: Technological First Aid, But For How Long?" p. 44*). Each processor type (P54/P55/P-6) has its own unique standard plug. The standard plug for the VRM goes on the PC's motherboard. If the processor has been changed and now demands a different supply voltage, only the VRM is changed, not the motherboard. Power-supply companies and several semiconductor companies are building VRMs. A number of semiconductor suppliers (including those building VRMs) are building some of the active semiconductor guts for VRMs and motherboard-based power supplies. Supplies for these processors must regulate line and load voltages to within ±5%, and hold their accuracy specifications over time, temperature, and load transients.

The supplies also must continue to meet their specifications while handling these ultra-fast transients produced when, in order to save power, most of the microprocessor's FETs are repeatedly turned off and on by software. One example of that situation is word-processing software that disables FETs between key strokes. Often, the supply must pull its output into regulation within a few clock cycles at rates

approaching more than 500 MHz. The latest Pentiums demand that the supply provide 5 A of current in 20 ns. However, the basic specification most supplies are designed to meet states that the output must hold within ±5% of the specified value over time, the environment, and transients.

Some split-plane processors are powered by two separate supply voltages. The logic and I/O run off 3.3 V, and the processor core runs off less than 3 V. Besides the Intel processor family, there are upcoming genrations of Sparc, Alpha, PowerPC, the AMD/NextGen machine, the MIPS-R server, and devices from Cyrix that have this arrangement.



1. A proprietary circuit technique in Cherry Semiconductor's controllers uses the voltage dropped across a switcher's load-capacitor's ESR by current flowing into the capacitors to handle severe load transients by putting the output in a 0 or 100% duty cycle mode. The V^2 technique does not depend on the gain-bandwidth product of the error amplifier.

Although designers are busy adding power-hungry bells and whistles to their systems, maximum efficiency is demanded at both low- and full-load conditions. The supplies have generated a succession of moving target challenges for analog IC designers who have come up with many different architectures to meet these challenges.

Science Fiction

Expect one day to see processors demanding over 100 A of current. Within the near future, 50 A or more will be common. Some Intel processors will soon demand 17 A at less than 2 V. Four of them in a server will call for close to 70 A. At 100 A, a 1-mΩ copper trace on a pc board drops 100 mV and dissipates 10 W. A 100-mV drop, even from a 5-V rail, is not significant. But from a 1-V rail, where it's 10% of the voltage, it will be significant. The pc board and copper trace may handle that power, but can the system? A look at the power requirements of some of the past, present, and near-future processors represents a possible baseline from which to make projections for the future *(see the table)*.

It's easy to come up with numbers like >70 A. Put more than two million CMOS FETs on a chip and assume each FET pair nominally switches 50 µA. That's a total of 100 A—procesors have been built with five times that many FETs. If supplies for such processors are putting out less than 1.5 V, then holding ±5% regulation means holding the output voltage within ±50 mV. That's a significantly tighter specification than the ±250 mV required by a 5-V ±5% rail. Some supplies (regardless of the architectures they use), handle the transient specification by letting the output swing its full ±5% for the transient, and holding the basic dc value of t[he] output an order of magnitude cl[oser]. This arrangement requires tha[t the] regulator circuit sport a very l[ow] open-loop gain and a very stabl[e in]ternal dc reference. Performa[nce] must be combined with fast re-sponse.

Change The Silver Boxes

There are several ways to get well-regulated voltages below 5 V, at relatively high currents, for systems running off the ac line such as desktop PCs and servers. The obvious way of redesigning the silver box so it converts the ac line voltage to dc voltages below 5 V has not appeared, yet. There are several reasons for this. First, systems have not moved completely to voltages below 5 V. Second, disk drives and other peripherals still need more than 5 V. Third, no sub-5-V standard exists. Additionally, given the SIA roadmap and the advanced processors showing up

A SAMPLING OF MICROPROCESSOR SPEED AND POWER NEEDS*

Processor	Clock Rate (MHz)	Current (core) (A)	Supply voltage(s) (V)	Code (bits)
P-54 Pentium	60/200	4	3.5 to 3.525	None
P-55 Pentium	150/250	5.7	Split plane (2.8 for core, 3.3 for I/O)	None
P-6 Pentium Pro	150/200	12.4	Split plane (2.1 to 3.5 in 100-mV steps for core, 3.3 for I/O)	4
P-6 Klamath	200/500	14	Split plane (1.8 to 3.5 in 100-mV steps for core, 3.3 for I/O)	5
P-7	Not available	17	Not available	Not available
AMD K5	Not available	4	2.38 to 3.6	None
PowerPC	Not available	3	3.6	None
Cyrix Cx486DX2-V80	Not available	2	4	None
Nexgen NX586	Not available	7	4 ±3%	None
AMD DXL2, DXL4	75/100 66/80	3	3.3	None

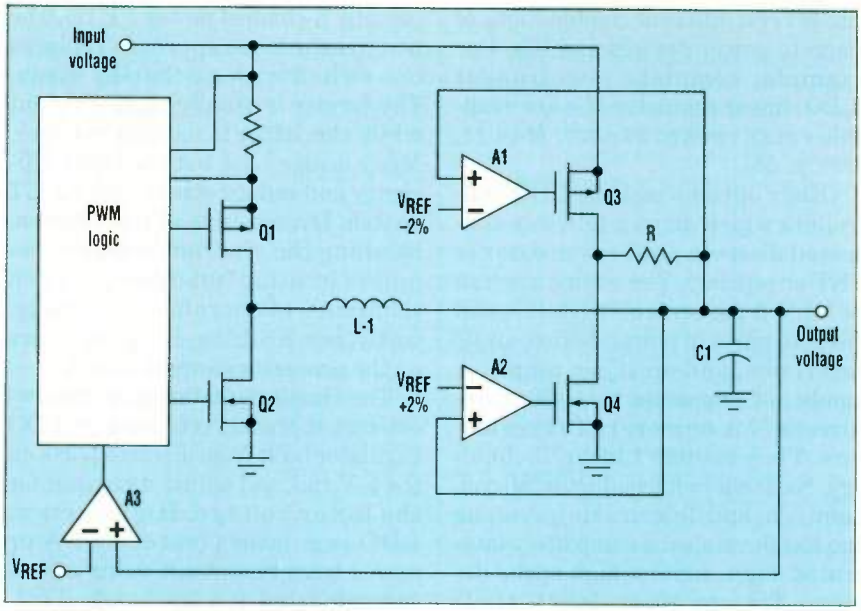
*All information in this table was obtained from discussions with supplers of the chips described in this report.

on the market, few off-line-to-high-current sub-3.3-V supplies will appear soon. The voltage is a moving target, consequently the power supply industry saw no reason to come up with new silver boxes.

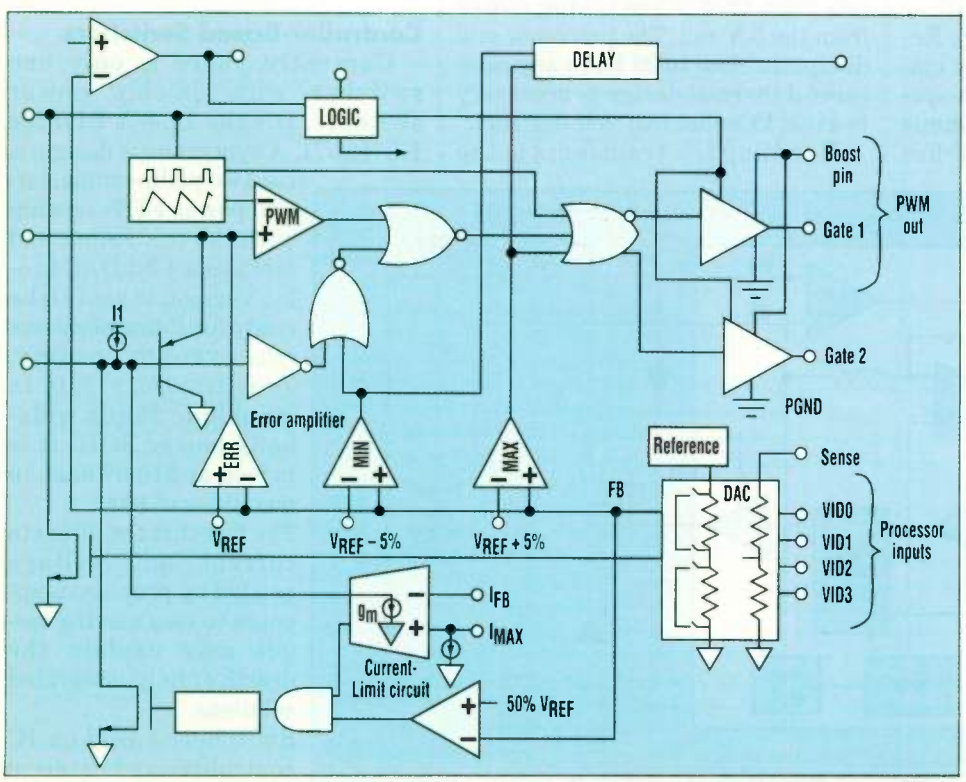
Rather, system designers took advantage of the already well-regulated 5- and 12-V rails, using linear regulators and switchers to convert them to voltages below 5 V. Most of the time, they used the existing high-current 5-V rail as a power-distribution bus, albeit a very inefficient one. If a system needs 10 A at 3.3 V, that translates to over 6 A at 5 V, and 100 A at 1.5 V still translates to 30 A at 5 V. As noted earlier, at those kinds of currents, voltage drops and power losses along the bus can be significant.

The industry has not implemented efficient distributed power in PCs and PC-based systems, despite the fact that mainframes and other large systems have been using distributed power for years. In fact, some mainframes distribute over 300 V.

For example, PCs could distribute the telecommunication industry's 48 V, 24 V, or even 12 V (100 A at 1 V translates to just under 2 A at 48 V or less than 4 A at 24 V). Since they have 12 V available for disk drives, some PC-based systems distribute it to low-power applications, and/or run power-management circuits such as switcing regulators off the regulated 12-V rail. Many of the available solutions can run off 5- or 12-V rails.



3. To handle fast transients, Maxim added a complementary half-bridge circuit (built from Q1 and Q2) to their controllers. When the output differs from the reference by more than 2%, gain blocks A1 and A2 turn on the upper or lower FET in the half-bridge circuit. The FET will either dump current into the the load capacitor or take current from of the load capacitor to ground.



2. Two fast comparators, min and max, were added by Linear Technology to their controller ICs. They fire when the feedback voltage exceeds the reference voltage by 2%, putting the output in either a 0 or 100% duty cycle mode. The technique does not depend on the gain-bandwidth product of the error amplifier.

However, a move toward a standard distributed power bus would have taken cooperation between system, power-supply, IC, and power-switch designers. In such a system of distributed power, the silver box would put out one or more well-regulated dc voltages for distributuion. Similar to current circuits that convert 5-V rails to 3.3 V or lower, at each major point of use an efficient buck regulator converts the distributed voltage to the required voltage. Very low-current, or higher-voltage applications (but lower than the bus voltage), can use linear regulators.

Assuming the use of a 5-V rail for power distribution, a system designer can draw on either of two basic circuit techniques to get from 5 to 3.3 V, or lower voltages—linear or switching regulators.

Linear regulators tend to be less costly, but less efficient than switchers. Each type of regulator can be partitioned

into several different combinations of discrete power devices and ICs. For example, complete low-dropout (LDO) linear regulator ICs are available *(ELECTRONIC DESIGN, May 13, 1996, p. 65)*.

Other options include LDO controllers which drive a follower-connected discrete power transistor (a FET or bipolar). The circuit also can be built from scratch with ICs and discrete parts (a power device, an IC reference, and an IC op amp.). A number of companies now offer high-current (7 A or more) LDO regulators. They include Linear Technology, National Semiconductor, Micrel, Semtech, and Telcom. However, no one has developed a completely integrated, high-current, high-speed device. Telcom does label their TCL1584 through TCL1587 series of regulators rated at 7 to 3 A as "fast response," but no transient response specifications are provided.

Low-Cost Power

Most switching regulators are built with IC controllers and discrete power switches which tend to be power FETs. In addition, a few devices are available with the power switches on the controller chip. Regardless of the approach, they employ either synchronous or non-synchronous designs. Synchronous designs use two power switches (usually n-channel power FETs). The non-synchronous approach replaces one switch with a Schottky diode. The former is usually more efficient while the latter is usually cheaper. Many designs use both to boost efficiency and reduce stress on the FET switch. Irrespective of the solution, handling the transients usually requires locating hundreds, or even thousands of microfarads of bulky, costly, low-ESR/low-ESL capacitors on the processor's supply pin(s).

The simplest, and usually the lowest-cost approach, is to hang an LDO regulator built from discrete parts on the 5-V rail, and adjust its output for the lower voltage. High-current LDO regulators (rated at 1 A or more) have been built using a low-current (rated at a few hundred milliamperes) LDO regulator as a controller driving a pnp transistor. But, like most supplies for the high-speed processors, these regulators have trouble handling the transients.

While not as efficient as a switcher, an LDO regulator lends itself to the Pentium which needs no more than 4 to 6 A. At 6 A and an output of 3.3 V, power dissipation runs less than 11 W when taking power from the 5-V rail. The processor still dissipates close to 20 W. In any case, careful thermal design is necessary to avoid PCs that may self-destruct.

Handling the transients is the problem to beat. To solve it for Pentium-class processors, Linear Technology recently came up with the LT1575 and LT1576, a pair of fast-response LDO controllers *(ELECTRONIC DESIGN, Nov. 18, 1996, p 162)*. Designed to drive an n-channel MOSFET, the LT1575 is used in applications such as the P-54 Pentium, which needs only one power rail below 5 V. The dual LT1576 is aimed at the split-plane P-55. Requiring just 24, 1-μF ceramic capacitors on its output pin, these controller ICs and their power FET cohorts eliminate virtually all the bulk capacitance usually needed to handle 250-A/μs load-current transients.

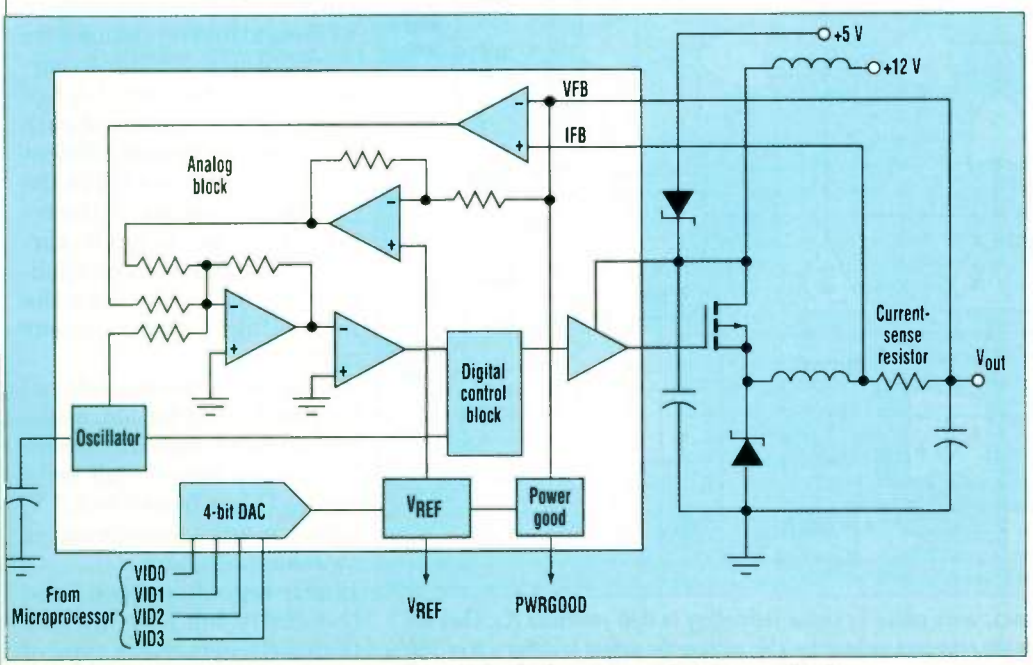
Six versions of each are available offering fixed outputs (5, 3.3, 3.5, 2.8, and 1.1 V), as well as an adjustable output version. By choosing the proper FET, higher currents and input voltages can be handled. The single versions come in 8-pin DIPs and SOICs; the duals come in 14-pin DIPs and SOICs. These regulator-controllers achieve their speed through careful wideband design in the error amplifier, and the use of a high-speed bipolar process.

Controller-Based Switchers

Currently, there is only one switcher with on-chip power switches. It's the 12.4-A Elantec EL7560/71. A synchronous design, it has two plain-vanilla, lateral power FETs on-chip with the controller, and contains a 4-bit DAC [a 5-bit version is said to be ready for P-6 applications *(ELECTRONIC DESIGN, June 24, 1996, p. 55)]*. In its unique 28-pin wide-body power SOIC it is priced at $10.67 each in quantities of 1000.

The fact that the ultimate current and voltage needed by processors appears to be a moving target may explain the dearth of fully-integrated solutions.

Switchers based on IC controllers and external power devices definitely appear to be the way to go. At least nine con-



4. To handle fast transients, Raytheon controllers employ both analog and digital control blocks.

Kepco deals the OEM a powerful hand.

MODEL MRW 145KV
28 WATTS, DUAL OUTPUT

2" x 8" footprint
50 x 200 mm

MODEL MRW 171KV
65 WATTS, TRIPLE OUTPUT

3.94" x 6.3" footprint
100 x 160mm

MODEL KRW 352KV
40 WATTS, TRIPLE OUTPUT

3" x 5" footprint
76 x 127 mm

CARD-STYLE POWER SUPPLIES
producing 35-65 Watts and featuring universal inputs.
+5V and +3.3V primary outputs combined with ±12V and ±15V.

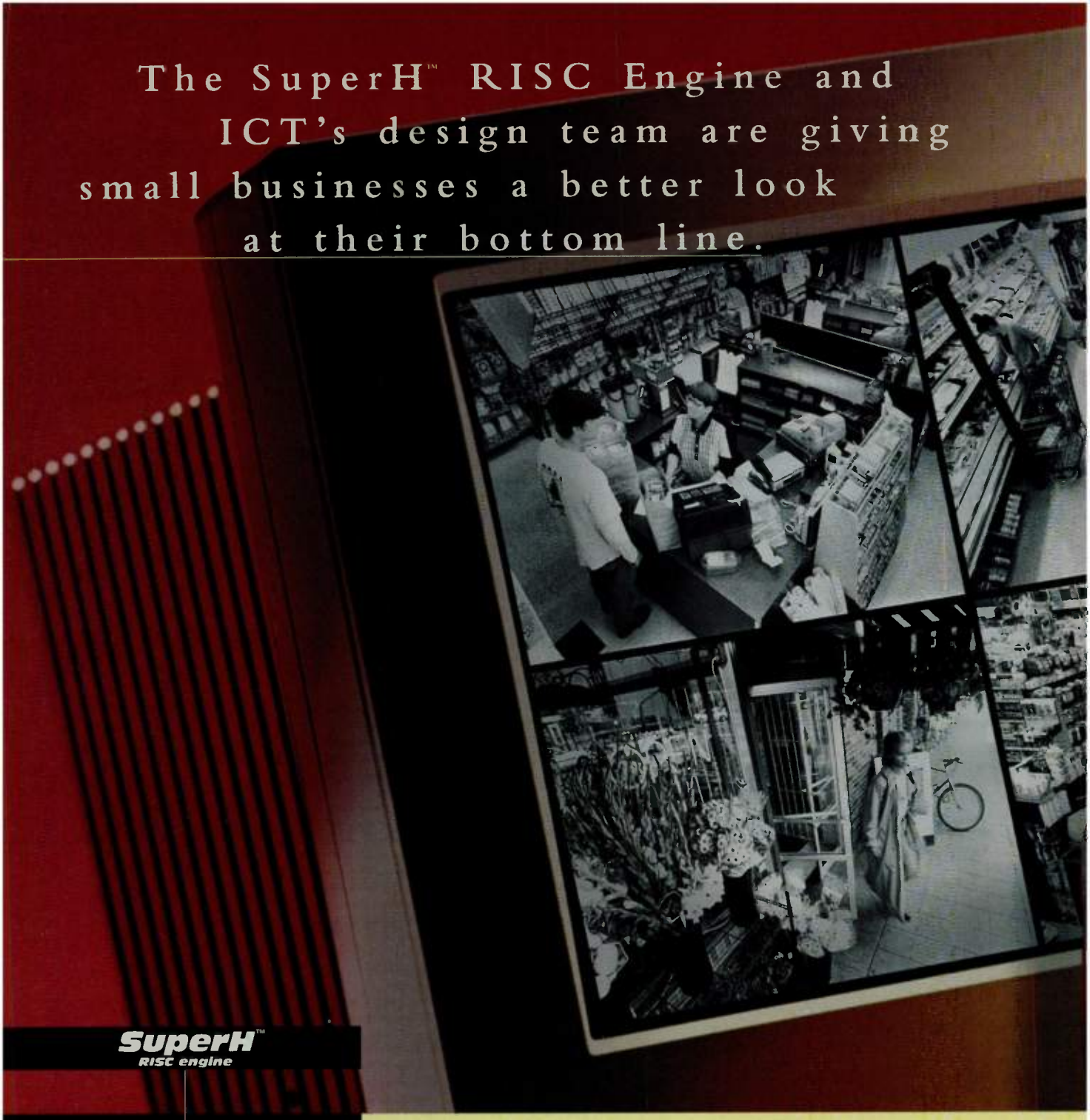
- Series KRW are on 3" x 5" PC cards, 40 Watts, triple output.
- Series MRW are in the popular 100x160 mm (3.94" x 6.3") footprint (except for the new model MRW 145KV, which is 2" x 8"), with especially low profiles for hard-to-fit places, 28-65 Watts, dual and triple output.
- Both series are produced in ISO 9001 certified facilities, are fully approved by TÜV/UL/CSA to the EN 60950 safety specification, and are fitted with Class B EMI filters.

KEPCO
THE POWER SUPPLIER™
SINCE 1946

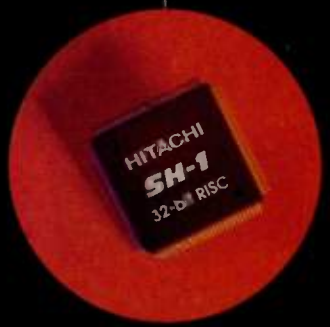
1946 KEPCO 50 1996

Kepco, Inc. HQ / Eastern Region, 131-38 Sanford Avenue • Flushing, NY 11352 USA • Tel: (718) 461-7000 • Fax: (718) 767-1102
E-Mail: hq@kepcopower.com • URL: http://www.kepcopower.com
Western Region, 800 West Airport Freeway, Suite 320, LB 6018, Irving, TX 75062 USA • Tel: (972) 579-7746 • Fax: (972) 579-4608

The SuperH™ RISC Engine and ICT's design team are giving small businesses a better look at their bottom line.



SuperH™ RISC engine



Limited Time Offer:
$99 SH-1 Evaluation Board
www.hitachi.com

The SH-1 embedded processor allowed ICT to build a remote-controlled, 16-camera, 32-bit video surveillance system that provides remote access to people who could never before afford it.

A Better Way to a Bigger Market. Designers at International Communication Technology (ICT) of Los Angeles, Calif. were justifiably proud of their PC-accessible, remote-controlled, video-surveillance system. But in defining their system roadmap, ICT realized that with a few added key features, and a lower system cost, they could hit the sweet spot in American business: the more than seven million small- to mid-size organizations that normally couldn't afford a system like theirs.

Custom logic was too expensive, used too much space and took too long to meet ICT's next-generation target. So they got creative. With the Hitachi SH-1 processor, ICT found they could solve their problem with software and a powerful, cost-effective RISC processor that offered a very high level of integration.

A Highly Integrated RISC Processor. A single SH-1 device, using its on-board memory and rich set of integrated peripherals, could do all of the transmitter-side work: picture compression, advance dial access, user I/F; as well as control the transmission system, function timers, I/O and DRAM for image storage.

With the Hitachi SH processor, it was possible to give their system wireless capability, add live audio, allow for three-second scene refresh, full rotational control of cameras *and* provide for automatic dial-up when triggered by fire, perimeter or call alarms.

A Bottom Line with a Future. ICT can sell their new PRO System 3A for just a quarter of the cost of its closest competitor! For ICT, there's another bottom line: without sacrificing their investment in code, their product roadmap now includes the ability to migrate performance or features upward or downward, virtually without limits.

A Broadly Successful, Easy-to-Prove Approach. From multimedia game machines to global positioning systems, SH chips have fueled success. Reason enough for them to be number one in RISC shipments. And a very good reason for you to put them through their paces in your own application.

The $99 SH-1 Evaluation Board. We'll make it easy on you: for a limited time, our fully-equipped board is only $99.

After all, we're concerned about your bottom line.

Call for information on our Evaluation Board or the Hitachi SuperH RISC Engine: 1-800-446-8341, ext. 700, or get full details on these and other products at **www.hitachi.com.**

troller ICs (or families of ICs) aimed at the Pentium, the Pentium Pro, and its kin are available. Each offers its own combination of total-system price, response time, regulation, flexibility, and features. Usually based on a unique design feature or a unique partitioning of the circuit, each scrambles to meet the Intel-processor requirements and guidelines. The following organizations are now producing these switchers: Cherry Semiconductor, Harris Semiconductor, Linfinity Microelectronics, Linear Technology, Maxim Integrated Products, Microlinear, Raytheon Semiconductor, Temic Semiconductors, and Unitrode.

Most switchers regulate voltage by pulse-width modulation (PWM). The control signal is set by the difference between a ramp voltage and an error signal, and power switch is then set by the control signal. The modulated pulse width of the control signal and/or the duty cycle of the power switch keep the output voltage constant despite variations in line and load.

The control method determines how the ramp voltage is generated. Voltage-mode controllers generate a ramp signal with an oscillator. The error-signal loop sets the switcher's small-signal transient response because its output directly triggers the power switch. Therefore, cutting loop-response time demands raising the switching frequency, which in turn increases switching losses in the FETs.

In conventional, peak current-mode control, the circuit's inductor generates a linear ramp, and usually demands a current-sensing element. The ramp's slope changes with input voltage, removing the error-amplifier's crossover characteristic from the effect of input transients. But, as in the case of voltage-mode control, the error amplifier handles load transients. Other techniques such as feed-forward, average current, and hysteretic-mode control offer other improvements. But, the performance still relies on the regulator's small-signal response.

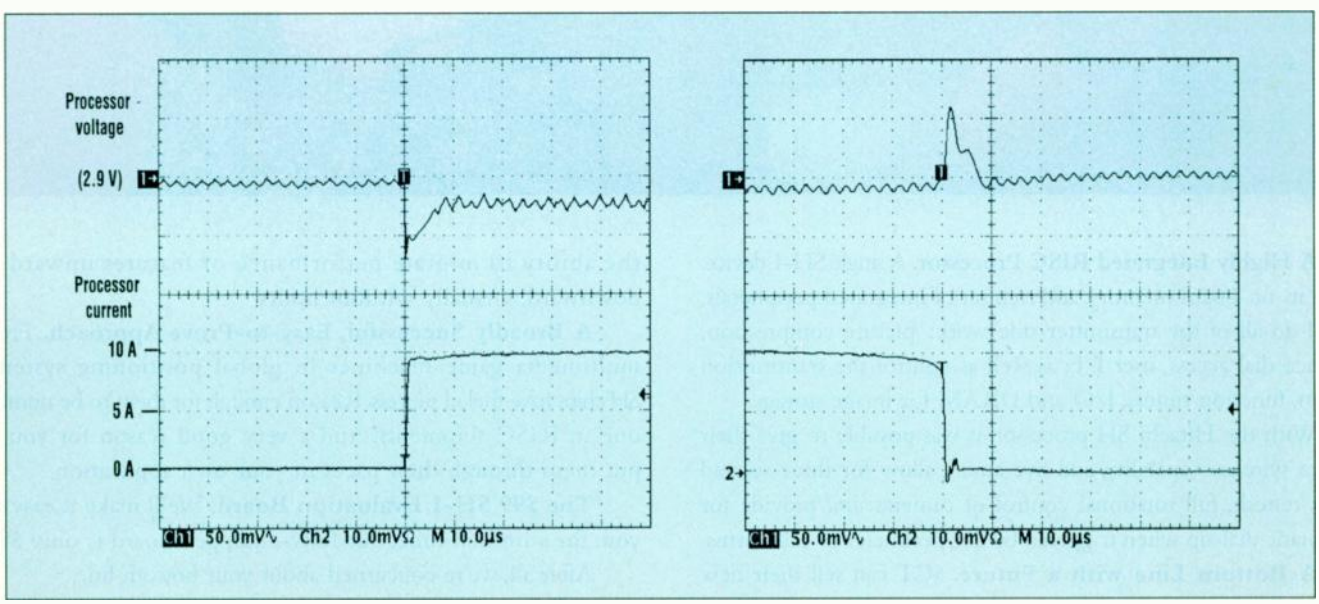
Different Strokes

Cherry Semiconductor offers a family of four controllers: the CS-5150, CS-5151, CS5155, and CS5156. The CS5150, a synchronous controller, is designed with 4-bit DACs to handle a 4-bit input code from a processor. The CS-5151, a non-synchronous controller, also handles a 4-bit code. The CS-5155 and CS-5156 are synchronous and non-synchronous, respectively. They are designed to handle 5-bit codes with their internal 5-bit DAC. The 4-bit chips provide output voltages from 1.24 to 3.54 V in 100-mV increments. The 5-bit chips provide output voltages from 1.34 V ±13.4 mV to 3.54 V ±35.4 mV in 50-mV increments.

All four of these controllers employ Cherry's proprietary V^2 architecture to provide faster loop response and easy loop compensation. In addition, the architecture provides lossless short-circuit protection that negates the use of a large, expensive, current-sense resistor. According to Cherry, V^2 cuts the response time to load transients by a factor of 10 to 50.

The V^2 circuit generates the ramp with the ESR of the circuit's output capacitors *(Fig. 1)*. This ramp is proportional to the ac current through the inductor, and is offset by the dc output-voltage level. V^2 control inherently compensates for both line and load variations. A change in line voltage changes the ramp signal, in turn changing the duty cycle. Since the ramp contains the dc portion of the output voltage, the control circuit corrects for line and load transisents by modulating the power switch to any duty cycle between 0 and 100%. Because a change in inductor current also modifies the ramp signal, the design responds fast to line transients. In most applications this switcher is running off the usually well-regulated output of the silver box, therefore, it will see few large fast-line transients.

The load's transient response is set only by the comparator response time and the transition speed of the power switch. A sudden change in load current instantly flips the comparator, turning the power switch off



5. After load transients of 0 to 10 A and 10 to 0 A, Temic controllers pull their regulators back into specification in under 5 µs.

Say goodbye to dip switches, jumpers, IRQ settings, DMA channels, tangled cables and I/O addresses. And say hello to increased functionality and true plug-and-play capability. Introducing Intel's Universal Serial Bus products, designed with the new USB specification. Now you can connect up to 127 different peripherals (like keyboards, monitors and joysticks) to a PC at once, with an easy-to-use common connector that allows hot insertion and removal. We've implemented the USB specification into Intel PCI chip sets, as well as in a family of single-chip peripheral controllers. They all go through Intel's rigorous end-to-end validation process for reliability and compatibility. Sound interesting? Visit the Intel USB Web site for more technical information and to download Intel's latest USB development tools. And get totally plugged in.

▶ developer.intel.com/design/usb

PROUD PARTNER

150 1846–1996 Smithsonian

intel®

READER SERVICE 109

or on. Because the circuit's loop response to load transients is independent of the error signal, the loop has a low crossover frequency. This slow loop provides the dc accuracy and low noise immunity that permits long fedback traces for remote sensing of the output voltage. In addition, the fast-loop architechture needs no compensation, while the slow loop requires only a 0.1-µF capacitor, regardless of load or layout. This design saves significant cost and space.

Adapt Or Die

The Cherry controllers also incorporate a technique called adaptive voltage positioning. It automatically sets the output voltage within the processor-core's allowable ±5% logic voltage limit to further improve transient response. The technique raises the voltage at the regulator's output to give it more time to respond. When the load draws maximum rated current, the technique sets the output at the lower window value in anticipation of a rise in voltage as the load drops. At light loads, the controller sets the output near the top of the voltage window (+5%). This arrangement allows the output to drop at least 9% at a maximum load-current transient.

The Cherry controllers, and several others, sport a hiccup short-circuit protection scheme that insures minimum dissapition under a short-circuited load. The controller just shuts down the supply. After a time-out period it tries to turn it back on. If there still is a short, it cycles off again. If the short continues, the supply is off 97% of the time. In many controllers, this function is incorporated in a soft-start circuit.

Harris has announced a functionally similar family of four controllers. The HIP6002 and HIP6003 handle 4-bit processors, and the HIP6004 and HIP6005 handle 5-bit processors. The HIP6002 and HIP6004 handle synchronous designs while the HIP6003 and HIP6005 handle the nonsynchronous designs. The architecture achieves fast transient response through the use of a single, voltage-feedback loop. The voltage-mode control provides 100% duty cycle operation, allowing inductor current to ramp faster than with current mode. To further improve response, the error amplifier combines an open-loop gain of 600 with a gain-bandwidth product of 15 MHz. It slews at 6 V/µs. The controllers eliminate the expensive, bulky, current-sense resistor by sensing the on-resistance of the PWM FET switch (the upper FET in the 2-FET circuits).

Add A DAC

Linfinity took a different tack to partition their controllers. They started with the LX1660/LX1661, a pair of general-purpose synchronous controllers (the 1661 is optimized for fast response). Rather than including the very slow 4- and 5-bit DACs on the same chip, they came up with the DAC-like LX1670. They call it a 5-bit programmable reference. The LX1670, an LX1660/LX1661 controller, and a couple of FETs meet the Intel requirement. LinFinity builds VRMs with the LX1670 and the LX1661. For lowest-cost applications, the LX1660/LX1661 chips can be used without the LX1670. Output voltage can be set with a resistive voltage divider.

The controller uses voltage-mode off-time control to achieve fast response and simplify loop compensation. In this technique, the off time is modulated by the output voltage, and switching frequency becomes a function of the input-to-output voltage ratio. The controller also employs hiccup-mode over-voltage control. Supplies that employ crowbar switches for such control eventually go into current limit and blow fuses.

Linear Technology also offers a pair of synchronous controllers, the LT1552 for 4-bit applications and the LT1553 for 5-bit applications. However, both have on-chip DACs. They, too, implement voltage-mode switchers. To cut response time the designers added a pair of comparators in the chip's feedback loop. The min comparator compares the feedback signal (FB) to a voltage 60 mV (5%) below the internal reference *(Fig. 2)*. If FB is below the min comparator's threshold, it overrides the error amplifier and forces the loop to full duty cycle. Full duty cycle is set by the controller's oscillator to about 90%. Similarly, the max comparator forces the output to 0% duty cycle if FB is more than 5% above the internal reference. To save the need for cost, size, and power dissipation of a current-sense resistor, current limit is provided by sensing the on-resistance of the upper FET. The largest and most costly component in a switcher can be the current-sense resistor.

A pair of synchronous controllers from Maxim buck the trend to voltage mode with the MAX1624 and MAX1625. They feature current-mode control. To cut losses in the current-sense resistor, control is located in the input side of the circuit (between the drain of the high-side n-channel MOSFET and the input rail). Thus, power dissipation is cut in half as current flows only during the on time of the switch *(Fig. 3)*. To speed it up, the chip employs a unique circuit consisting of a half H-bridge, built from a pair of relatively small complementary MOSFETs (Q3 and Q4). Each is driven by a gain block (A1 and A2) and connected to the output through a low-value resistor. They resemble circuits using a linear-mode output to handle transients, but the output has to be biased at high currents, further raising size, cost, and heat generation to an unacceptable value. The circuit keeps these additional FETs turned off until a load transient triggers the controller.

If the output voltage drops more than 2% due to a transient load increase, A1 detects the error and turns on Q3 by driving its gate low. Current flows from the input supply directly into the output filter capacitor C1, recharging it, and bringing the voltage back into regulation. If the output rises more than 2% (generally due to energy stored in the inductor when the processor is put in a low-power mode), A2 detects the error and turns on Q4. Current is shunted from L1/C1 to ground. Ouput voltage variations of less than 2% are handled by the basic regulator controller. To up the response of the complete regulator demands high speed from A1 and A2.

A trio of synchronous controllers, the ML4900, ML4901, and ML4902, are available from Micro Linear. The first two handle 4-bit applications,

SIEMENS

Is your optocoupler an accident waiting to happen?

Don't fall for low-quality devices.

You can't afford optocoupler failures in your designs. That's why Siemens has pioneered advanced manufacturing procedures like over/under double molding to maximize coupling efficiency for high transfer ratios and low current applications. This ensures volume capacity — and the specifications to meet your circuit needs.

Get the tightest performance specifications available.

ISO 9001 Even on duals and quads, our devices have 2:1 min/max CTR ranges. And our products are UL recognized while meeting all international approvals, including IEC950 requirements.

Current Transfer Ratio (CTR) Ranges

		A	B	C	D
4-Pin Single	SFH615A	X	X	X	X
	SFH617A	X	X	X	X
	SFH6156	X	X	X	X
6-Pin Single	CNY17	X	X	X	X
	CNY17F	X	X	X	X
	SFH600	X	X	X	
	SFH601	X	X	X	X
8-Pin Dual	ILD615	X	X	X	X
16-Pin Quad	ILQ615	X	X	X	X

A : 40 min–80 max
B : 63 min–125 max
C : 100 min–200 max
D : 160 min–320 max

So call today for your free Siemens Optoelectronics databook. Ask for Ext. 4, Lit Pack #M23A003.

And safeguard yourself against optocoupler accidents for good.

1-800-77-SIEMENS
http://www.sci.siemens.com

while the third handles either 4- or 5-bit jobs. They use a two-chord DAC. In its upper range, the controller's output is set between 2.1 and 3.5 V, in 100-mV steps. In its lower range, its output is set between 1.8 and 2.05 V, in 50-mV steps. In comparison to the previously described controllers that have been designed to drive n-channel FETs, the ML4900 has been designed to drive complementary devices (a p-channel upper FET, and an n-channel lower FET.) These chips also use voltage-mode control and speed-up circuits.

A proportional control loop handles the regulation when the output is within 3% of the value called for by the DAC. When the output exceeds the called-for value by more than 3%, the transient control loop is energized, forcing a FET switch to either 100% or 0% duty cycle until the transient has been handled successfully.

Most of these controllers require a 12-V supply rail so they can drive standard MOSFETs, but a few 5-V units are limited to driving the more expensive, logic-level MOSFETs. Most of the 12-V devices take the power they control from the 5-V rail. Other controllers sport an on-chip charge pump or flying-capacitor bootstrap circuits to create the 10-to-12-V drive required by standard MOSFETs. Still others require an external charge pump or bootstrap circuit for the task. If a 12-V rail is available, most use it.

While most controllers are designed to take the input power for the power FETs in their regulator from the 5-V rail, Raytheon provides controllers such as the RC5043. The RC5043 is designed to run its FETs off 12 V *(Fig. 4)*.

Skip Dem Pulses

Raytheon's designers like those at Micro Linear and Maxim bucked the trend to voltage-mode operation and stuck to current mode. They use pulse-skipping techniques (pulse-frequency modulation or PFM) to optimize efficiency under low-load conditions. The controller senses the load level and automatically switches between PWM and PFM.

To optimize response to load transients, they employ an analog block and a digital block in the control loop. The analog block consists of signal-conditioning amplifiers feeding comparators which provide inputs to the digital block. The analog block takes signals from the IFB (current-feedback) and the VFB (voltage-feedback) inputs. The digital control block takes the comparator inputs and the output of the oscillator, and creates the pulses to drive the power FET or FETs (in a synchronous regulator).

Raytheon's RC5040 (synchronous) and RC5042 (nonsynchronous) are 4-bit controllers, while the RC5050 (synchronous) and RC5051 (nonsynchronous) are 5-bit controllers.

By using a very fast complementary bipolar CMOS process, Temic Semiconductor has come up with a voltage-mode, synchronous controller, the Si9140 *(Fig. 5)*. The high-speed process and careful design made possible a controller whose error amplifier has a 25-MHz unity gain bandwidth, providing a means to handle 10-A transients in 5 µs.

Unlike most of the other controllers, the Si9140 has no DAC. It does have an external reference input and external resistor networks that can be used to set the output voltage using the internal reference. Temic has the ability to put a DAC on a next-generation controller without upping their response time to transients. They also have the ability to tailor a power MOSFET to an application.

Unitrode has a large family of controllers; some with DACs and some general-purpose devices without them. For use with DAC-less devices they provide a 4-bit DAC chip, the UC3910. Their latest controller, the UCC1882, handles the 5-bit applications with average current-mode control. To handle the expected load transients, both the current and the voltage error amplifiers have gain-bandwidth products in excess of 5 MHz. An over-voltage comparator pulls the current amplifier's output voltage low to force 0% duty cycle when the system output voltage exceeds its specified value by more than 25%.

How Valuable	Circle
Highly	550
Moderately	551
Slightly	552

MORE POWER LESS SPACE 5A SIMPLE SWITCHER

THE NEW LM2587 5 AMP SIMPLE SWITCHER® FLYBACK POWER CONVERTER.

Now you can get high power in a small space plus the design simplicity of National's popular Simple Switcher family.

The device is the **LM2587** 5A flyback power converter. With a switching frequency of 100kHz, it can be used with smaller (off-the-shelf) external components. And it's available in a small TO-263 surface mount package.

Designed for flyback, forward and step-up converter applications, it's available in 3.3V, 5V, 12V and adjustable output voltage versions.

And like all of National's Simple Switcher products, the LM2587 makes designing extremely easy. Our Switchers Made Simple® design software does it all in minutes. And National guarantees the system performance, not just the silicon.

So when you need a lot of power in a little space, step up to the LM2587.

FREE SAMPLES—FAST.

For free datasheets, free samples, and application support, contact us at:

CALL: 1-800-272-9959 Ext. 711.

INFO CARD: Mail or Fax

WEB: http://www.national.com/see/lm2587

In Europe, fax us at +49 (0) 180-5-12-12-15; in Japan, call 81-43-299-2300; in Southeast Asia, fax us at 852-2376-3901.

National Semiconductor®

Moving and shaping the future.™

WRH

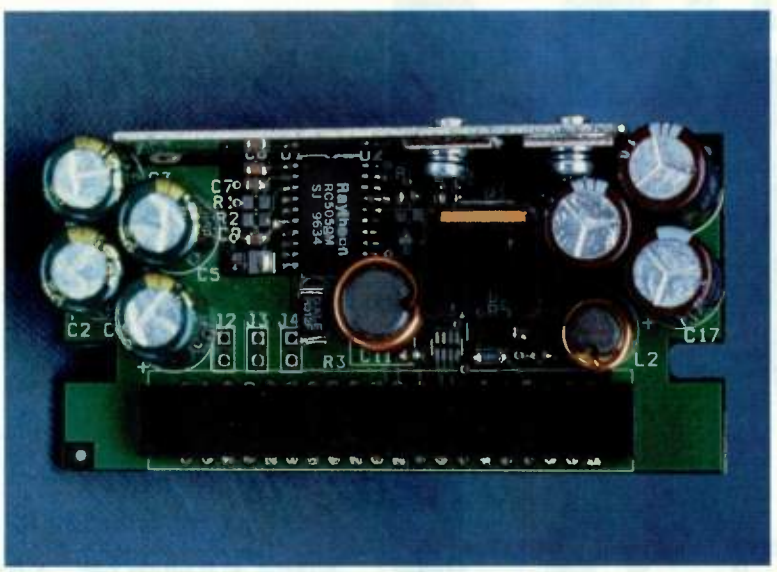
VRMs: Technological First Aid, But For How Long?

While These Off-The-Shelf Modules Can Satisfy Current Power Requirements, Future Processor Demands Could Spell The End Of Voltage Regulator Modules.

Patrick Mannion

SPECIAL REPORT

As the latest crop of high-end microprocessors hits the market, the migration to ever-lower voltages at higher currents has propelled the power-supply designer from the back end of the design process to the forefront. Previously an afterthought, getting sufficient clean power to these chips fast enough has designers jumping through hoops to overcome the increasingly complex analog design issues now facing them. For some, designing from scratch in-house remains the only viable solution. For others, off-the-shelf, fully-tested voltage regulator modules (VRMs) provide a quick-and-easy escape route from the black magic that is analog power design. In between lie the varying levels of cooperation between motherboard manufacturers and VRM vendors that have become necessary to satisfy custom requirements.



Courtesy: Raytheon Electronics (RCB004 voltage regulator module)

The path to power chosen by the board designer is the result of a careful evaluation of a number of factors including in-house resources, time-to-market restraints, cost, performance requirements, predicted product life cycle, and the level of flexibility required. In some instances, a combination of the two extremes—a VRM initially, followed by a fully-integrated design at a later stage—may prove to be the optimum path. In addition, the VRMs themselves must be examined carefully before a choice is made. Essential parameters to be considered include output levels, line and load regulation, temperature stability and handling, load transient response, ripple and noise, protection, and accuracy over time. In addition, the level of upgradeability or "futureproofing" designed into the module must be considered.

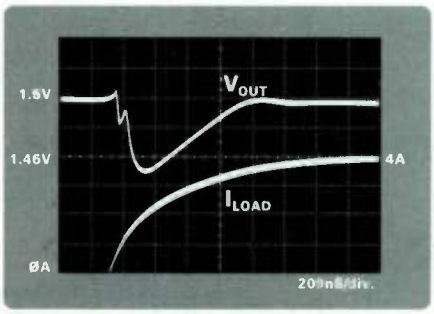
Why So Complicated?

The difficulties encountered in designing an appropriate power drive scheme for a CPU are relatively recent, and stem mainly from the exponential integration curve the electronics industry is riding. Due to the curve, the voltage levels must be lowered from the standard 5 V, to 3.5 V. This change will keep a tight rein on power consumption and avoid damaging the leading-edge, sub-micron silicon geometries now being used. In addition, the sheer quantity of gates in these devices, along with their operating speeds, have sent current requirements through the roof. The latest round of processors are demanding upwards of 14 A, and this is predicted to rise quickly to 20 or 30 A.

As in many areas at the leading edge of technology, standardization is practically nonexistent. The reduction of voltage levels is happening in a haphazard and inconsistent fashion. Currently, on the typical split-plane processor chip, I/O voltages range from 3.3 to 3.5 V, while internally they can range anywhere from 1.8 to 2.8 V, to the full 3.5 V, depending on the chip or the manufacturer. The decreases show no sign of slowing up or falling in step. To provide for the possible variations, initial split-plane-voltage processors, such as Intel's P55C, were catered to using external jumpers. Now processors such as the Pentium Pro use a four- or five-bit binary code which is set by a bonding operation in the packaging process. This code is detected by the power supply which then uses it to determine what its out-

HIGH CURRENT LOW DROPOUT REGULATOR VAUNTS VALUE AND VAROOM.

OUR LM3460 & LM3411 CONTROLLERS PROVIDE ENHANCED PERFORMANCE FOR HALF THE PRICE OF MONOLITHIC ICs.



LOAD TRANSIENT RESPONSE

Vis-à-vis monolithic IC solutions, our new regulator circuit packs an unparalleled price/performance punch for high-current power supplies.

As part of our complete LDO voltage-regulator circuit, the **LM3460** and **LM3411** controllers boast 1% accuracy and excellent transient response and load regulation. All with a minimum of input and output capacitance and zero EMI.

They're also very versatile, with an output voltage that's adjustable from 1.2V to 3.6V, and an output current that generates up to 8A. Plus, they're packaged in SOT23-5s. All of which makes them invaluable for your volume designs.

FAMILY OF CONTROLLERS

Part Number	V_{OUT}	Typical Application
LM3460-1.5	1.5V	GTL+ Bus Termination
LM3460-1.2	1.2V	GTL Bus Termination
LM3411-3.5	3.5V	CPU Power Supplies
LM3411-3.3	3.3V	5V to 3.3V Conversion

FREE SAMPLES—FAST.

For a datasheets, free samples, and application support contact us at:

CALL: 1-800-272-9959 Ext. 711.

INFO CARD: Mail or Fax

WEB: http://www.national.com/see/LM/LM3460

In Europe, fax us at +49 (0) 180-5-12-12-15; in Japan, call 81-43-299-2300; in Southeast Asia, fax us at 852-2376-3901.

National Semiconductor

Moving and shaping the future.™

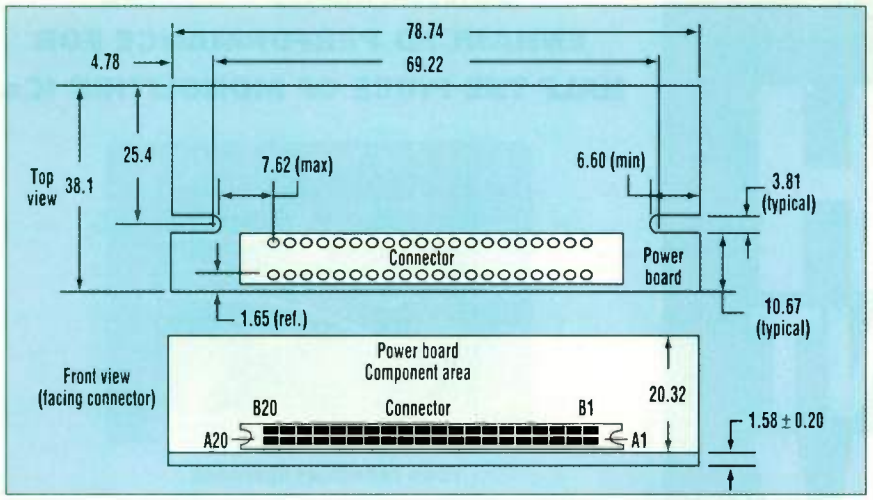


Fig. 1: An ideal solution for many applications, VRMs boast high-power-handling capability, flexibility, and off-the-shelf availability. However, their high cost, and potential to interfere with neighboring pc-boards is proving to be a deterrent. In addition, their ability to handle upcoming processor requirements is questionable.

put should be.

Lowering the operating voltages also has made staying within the 3.5-V ±5% voltage tolerance somewhat of an art form. At 10 A, only 0.0175 Ω of line resistance can be tolerated. Any more than that and the voltage drop will pull the supply voltage out of specification. Current-generation processors have reduced this tolerance to around 3%. Such tight tolerances can be met by carefully selecting the regulator, and by using resistors with 0.1 or 0.5% tolerance instead of the typical 2%.

However, that's not the whole story. With current requirements as high as they are, processors must reside in a standby mode for much of the time to avoid excessive heat and to limit power consumption. When the processor "wakes up," the supply must deliver the entire required current, at the proper voltage, within a few clock cycles. This change in current can be as high as 300 A/μs. At this rate of change, Ldi/dt becomes a serious consideration, since a typical board trace has an inductance of about 8 nH/cm. At 300 A/μs, a voltage drop of up to 2.4 V/cm can be expected due to inductance alone.

In addition, the regulator is not physically capable of delivering this current that quickly, hence high-quality, low equivalent-series-resistance (ESR) capacitors are required. These capacitors must be placed as close to the point of delivery as possible.

After evaluating the essential power requirements of these upper-echelon processors, design issues such as form of regulation (switching or linear) must be addressed. Reliability, too, becomes more of an issue because the high currents involved raise the problem of dissipating generated heat. Although fan-assisted heatsinks are effective, they are unreliable and costly. A better solution is to pay more attention to the heatsink design itself in the context of overall system airflow.

Three Pillars Of Good Design

Cost, cost, and cost. It's unfortunate, but true. Although the myriad of parameters only briefly outlined above might send most motherboard designers scurrying to the nearest VRM vendor for that quick-and-easy solution, they'll have to run the gauntlet through the accounting department first. It is here where the real decision as to whether or not to go with an embedded, roll-your-own design, or an off-the-shelf module is made.

The cost of designing an embedded solution can quickly add up when the added steps involved are considered. These extra steps include actual design and layout, accommodating the through-hole components (most components of a typical motherboard are surface-mounted), test and qualification. The actual design itself requires expensive in-house resources and expertise that many companies just don't have. For those that do have the capability, the ever-present pressure of a shrinking time-to-market window can make life a lot more difficult. In addition, embedded designs limit the flexibility to accommodate future processor upgrades.

Considering these factors, it is apparent that the cost of an embedded design can only be justified in high-end applications where off-the-shelf solutions just don't give the performance required, and where the target market can afford the extra costs involved. These applications include high-end servers and workstations

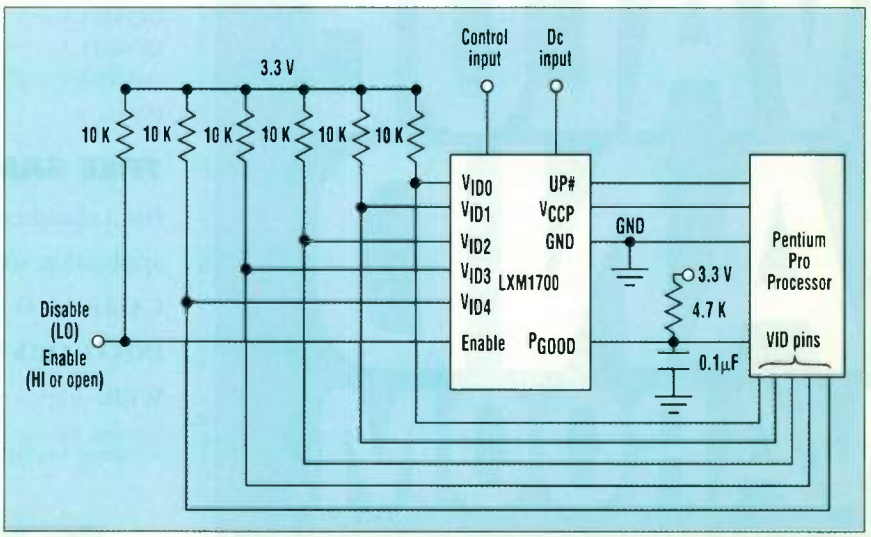


Fig. 2: The voltage identifier (VID) code pins on a typical VRM, such as the LXM1700 from LinFinity, provide for flexibility by allowing the module to accommodate any processor voltage requirement from 3.5 to 2.1 V in 100-mV steps, and from 2.1 to 1.8 V in 50-mV steps.

MINUSCULE POWER. (0.7µA)

MICROSCOPIC VOLTAGE. (2.0V)

TINY COMPARATOR (SOT-23 TinyPak™)

NOW THAT'S HUGE.

INTRODUCING THE LMC7215/LMC7225. THE INDUSTRY'S HIGHEST VALUE IN LOW-POWER COMPARATORS.

SPECIFICATIONS	OUR LMC7215/25	THE OTHER GUYS
MAX SUPPLY CURRENT @ 25°C	1.0µA	BIGGER
MIN SUPPLY VOLTAGE	2V	BIGGER
MAX OFFSET VOLTAGE (0-70°C)	8mV	BIGGER
PACKAGE	SOT23-5	BIGGER

(BUT OURS HAS A BIGGER COMMON MODE INPUT RANGE—RAIL-TO-RAIL)

With a unique combination of high-performance specs, National's **LMC7215/25** comparators allow you to design monitoring and analog signal conditioning applications for your portable products in ways—and at a cost—that just weren't possible before.

The LMC7215/25's extremely low supply current of 1µA maximum is optimized for portable equipment and is the lowest of any comparator on the market. Its 2V minimum operating voltage is ideal for low-voltage systems, while the LMC7225's open drain output lets you optimize your mixed voltage system designs. And the LMC7215/25's input common mode voltage exceeds supply voltage rails, making it perfect for systems required to monitor large input signals.

By extending National's industry-leading family of low-power comparators, the LMC7215/25 offers you a powerful way to optimize your design without sacrificing one iota.

And what could be bigger than that?

FREE SAMPLES—FAST.

For datasheets, free samples, and application support, contact us at:

CALL: 1-800-272-9959 Ext. 711.

INFO CARD: Mail or Fax

WEB: http://www.national.com/see/LMC7215_25

In Europe, fax us at +49 (0) 180-5-12-12-15; in Japan, call 81-43-299-2300; in Southeast Asia, fax us at 852-2376-3901.

National Semiconductor

Moving and shaping the future.™

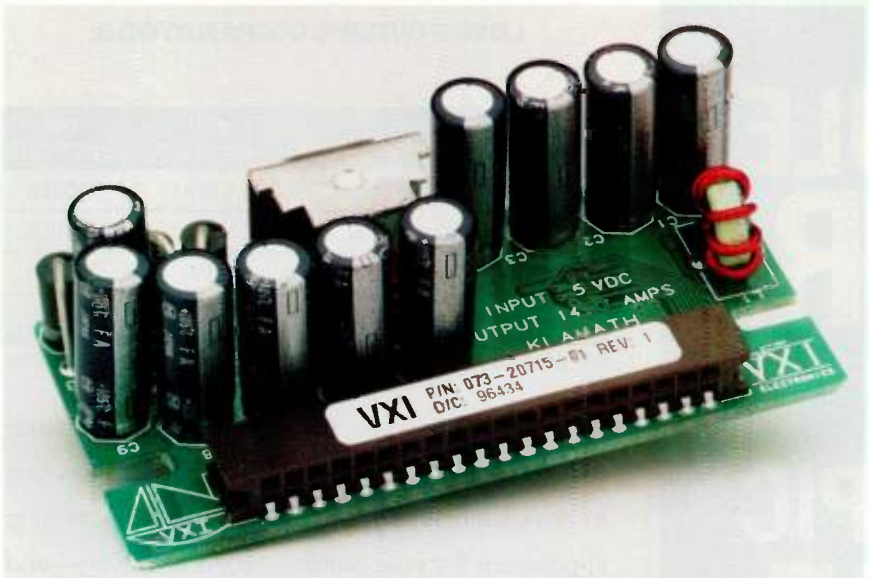


Fig. 3: The 073-20715-01 VRM from VXI Electronics provides essential capabilities such as 14-A output; 5-bit VID; and overvoltage, undervoltage, and overcurrent protection.

that combine high performance with slower technology turnover. Although this holds true for the most part, some companies a few notches down on the performance curve do embed their supplies on board. However, their target market population is in the hundreds of thousands—easily capable of absorbing the initial engineering and tooling expense. These designs also incorporate a certain degree of flexibility by designing in a VRM header that will allow the board to power any future processor upgrades. To beat the time-to-market pressure, some companies are even using a VRM on the first production runs to get the board out the door, and then designing it onto the motherboard as an embedded solution at a later stage. For some board runs however, "a later stage" never comes as new features quickly make initial designs obsolete.

It is due to this fast turnover that VRMs have found favor, despite their need for an extra socket and pc board, overall higher cost at upwards of $15 each, and their possible effect on neighboring system boards *(Fig. 1)*. Although initially specified for the Intel processor, the popularity of VRMs is underscored by their use with Sparc and other processor architectures, all of which face the same power, time-to-market, and cost pressures. Their incorporation into other architectures also has been helped by the fact that the Intel specification, while laying down a number basic requirements, added quite a few guidelines that are open to various interpretations. This situation has led to a certain degree of stretching of the specification.

When examining a possible candidate, the major parameters to focus on are the input and output voltages, current output, initial accuracy, slew rate, line and load regulation, load transient, efficiency, temperature stability, and protection features. Components used, particularly the capacitors, also must be examined. If the life cycle of the board is expected to be relatively short, high-end electrolytic capacitors with a low ESR are sufficient. However, for longer life spans, the tendency of an electrolytic capacitor's ESR to rise over time makes them unsuitable. No-wet electrolytics, such as Oscons, are preferable.

Another important consideration is the degree of support offered by VRM vendors. Some provide none, while others will hold your hand all the way through to final production. For everyday applications, where the performance envelope is not being pushed, all VRMs are pretty much the same, so support can be the deciding factor, along with a guarantee of specification conformance.

Specification guarantees come from companies such as LinFinity Microelectronics in their soon-to-be-released LXM1700-xx line of VRMs. Along with a guaranteed 14.0-A output, this high-end PentiumPro module features the 5-bit voltage identification (VID) coding to go from 3.5 to 2.1 V in 100-mV steps, and from 2.1 to 1.8 V in 50-mV steps *(Fig. 2)*. This voltage range and output current make the LXM1700-xx suitable for current, as well as upcoming processors, such as Intel's Klamath. The module can be powered from 5- or 12-V supplies.

Performance specifications include an initial accuracy within ±0.6 mV at 0.5 A; a load and line regulation of 15 and 1 mV, respectively; a load transient of 95 mV; and an efficiency of 80%. A high level of short-circuit, over-voltage, and under-voltage protection is built-in. Soft start eliminates turn-on overshoot.

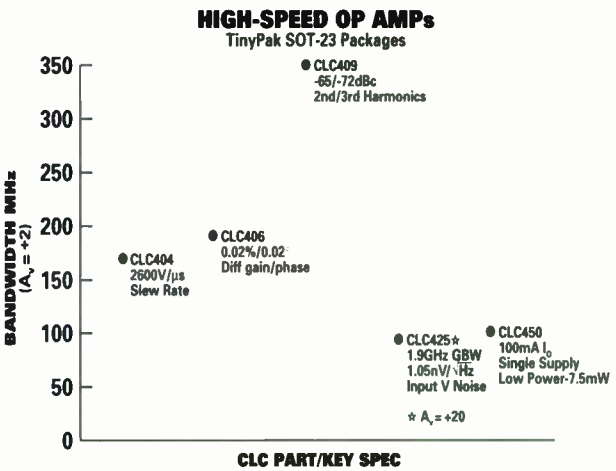
With its 14-A output, the LXM1700 meets Intel's current requirements however, even Intel considers that figure a bit high (for the moment). Many applications are quite safe with VRMs with current outputs as low as 10 A. Therefore, high-end VRMs that weigh in at under 14 A, such as Raytheon's RCB004, with an output current of 12.5 A (14 A peak), are not at any real disadvantage. Also available with a 5-bit VID, the RCB004, like the LXM1700-xx, provides the flexibility to support the entire Pentium Pro processor family with a single motherboard design. The module has an output-voltage selection range of 1.3 to 3.5 V, and offers a relatively high efficiency of greater than 84%. The set-point accuracy is typically within ±0.8 V, while the load and line regulations are typically within ±0.8 and ±0.1%, respectively. Short-circuit protection is provided.

Another Klamath-capable offering comes from VXI Electronics. Delivering PentiumPro VRMs since Q3 1995, VXI has recently rolled out its 5-bit, VID 073-20715-01 VRM with a programmable-voltage output from 2.1 to 3.5 V in 100-mV steps, and from 1.3 to 2.05 V in 50-mV steps *(Fig. 3)*. With an output current of 14 A, the module is ready for upcoming processor iterations. Overvoltage, undervoltage, and short-circuit protection are provided. The operating temperature range is 0 to 60°C.

Semtech Corp. has recently re-

WIDEBAND OP AMPS WITH MEGA PERFORMANCE (Up to 350MHz) AND MICRO FOOTPRINTS. (SOT-23 TinyPaks)

COMLINEAR TINYPAK OP AMPS CAN REDUCE SPACE, SAVE MONEY AND IMPROVE YOUR SYSTEM'S PERFORMANCE.



Strapped for space, but need big op-amp performance? Choose our 2600V/µsec **CLC404**† for high speed. The 0.02%/0.02° diff gain/phase CLC406 for video. The -65/-72dBc 2nd/3rd harmonics (20MHz) **CLC409**† for low distortion. For low input voltage noise, you can't beat the 1.05nV/√Hz **CLC425.** And for single-supply 5V designs requiring high output, and low power (7.5mW) pick the 100mA **CLC450.**

These TinyPak devices mirror their larger SOIC and DIP cousins in specs. They have most of the same features too. But they take less space, so you can tuck them away in tight spots, often boosting system performance. You'll find prices as low as *$1.39 in 1000s.

† Available 1Q 1997

FREE DEMO BOARD WITH TINYPAK.

For free samples, demo board, datasheets, and application support, contact us at:

CALL: 1-800-272-9959 Ext. 711.

INFO CARD: Mail or Fax

WEB: http://www.national.com/see/TinyPak

In Europe, fax us at +49 (0) 180-5-12-12-15; in Japan, call 81-43-299-2300; in Southeast Asia, fax us at 852-2376-3901.

National Semiconductor

Moving and shaping the future.™

leased its MP60 module with an output of 13 A and a 4-bit VID code for voltages from 2.1 to 3.5 V. A straightforward module with a minimum component count, the MP60 is designed for long-term reliability. Companies such as Semtech and LinFinity, with backgrounds in regulator IC design, can leverage their experience to bring to market a reliable, robust version of what is, essentially a larger regulator IC, as opposed to a scaled-down power supply. This advantage also helps them to optimize their particular IC design for best results.

The other benefit to having this background is the level of support these IC houses can offer the board designer. If an on-board solution is the final goal, IC houses-turned-VRM-vendors have the means to offer their particular regulator along with a circuit diagram, bill of materials, Gerber files, and any other form of help necessary to implement a partial to full board-level design.

At the extreme end of this complete solution offering, companies such as Celestica tend to actively avoid the regular, commodity end of the market, and instead focus on high-end custom applications. Key to Celestica's converters is the power ASIC (PASIC) that combines power, analog, and digital functions on a single chip. Using chip-on-board technology, the PASIC is soldered onto an insulated metal substrate, and wire bonded to form the electrical connections. This method gives a base reliability off the line of five million hours MTBF.

The company is prepared to back up its assertion of reliability and performance by providing extensive qualification testing at the system level. The latest design, the model UHR-005-BP4-029-SNV, takes a 5-V input, and provides up to 12.4 A with an output voltage that is 4-bit controlled in 100-mV increments from 2 to 3.5 V. Specifications include an efficiency of 83%; line and load regulations of 0.03% of the output voltage, and 100 mV, respectively; a transient response of 3.5% of the output voltage; and a ripple of 3 mV. Output overvoltage and overcurrent protection, as well as input undervoltage lockout are provided.

Such custom design work, for the most part, is unwarranted. Solutions such as the AA39 from Astec America Inc. are perfectly capable of meeting the di/dt requirements (up to 12.4 A) of the PentiumPro, with room to spare. Along with a 4-bit VID, the module comes with output crowbar and tracking overvoltage protection that varies as the output voltage is programmed.

Despite the high performance levels achieved by VRM manufacturers to date, the rapid advances in technology and the laws of physics are turning against them. It won't be long before symmetrical multiprocessing with two to four 20- to 40-A ultra-high-speed processors becomes the norm, breaking through the module's limitations. With the quick-and-easy solution no longer viable, other options, such as distributed power architectures, will be essential. In the meantime, VRMs will suffice for a number of board iterations to come.

For more information contact:

Astec America Inc.
Carlsbad, CA 92009
Collon Lee (619) 930-4706
CIRCLE 540

Celestica Inc.
North York, Ontario, Canada
Chris Stratas 800-461-2913
CIRCLE 541

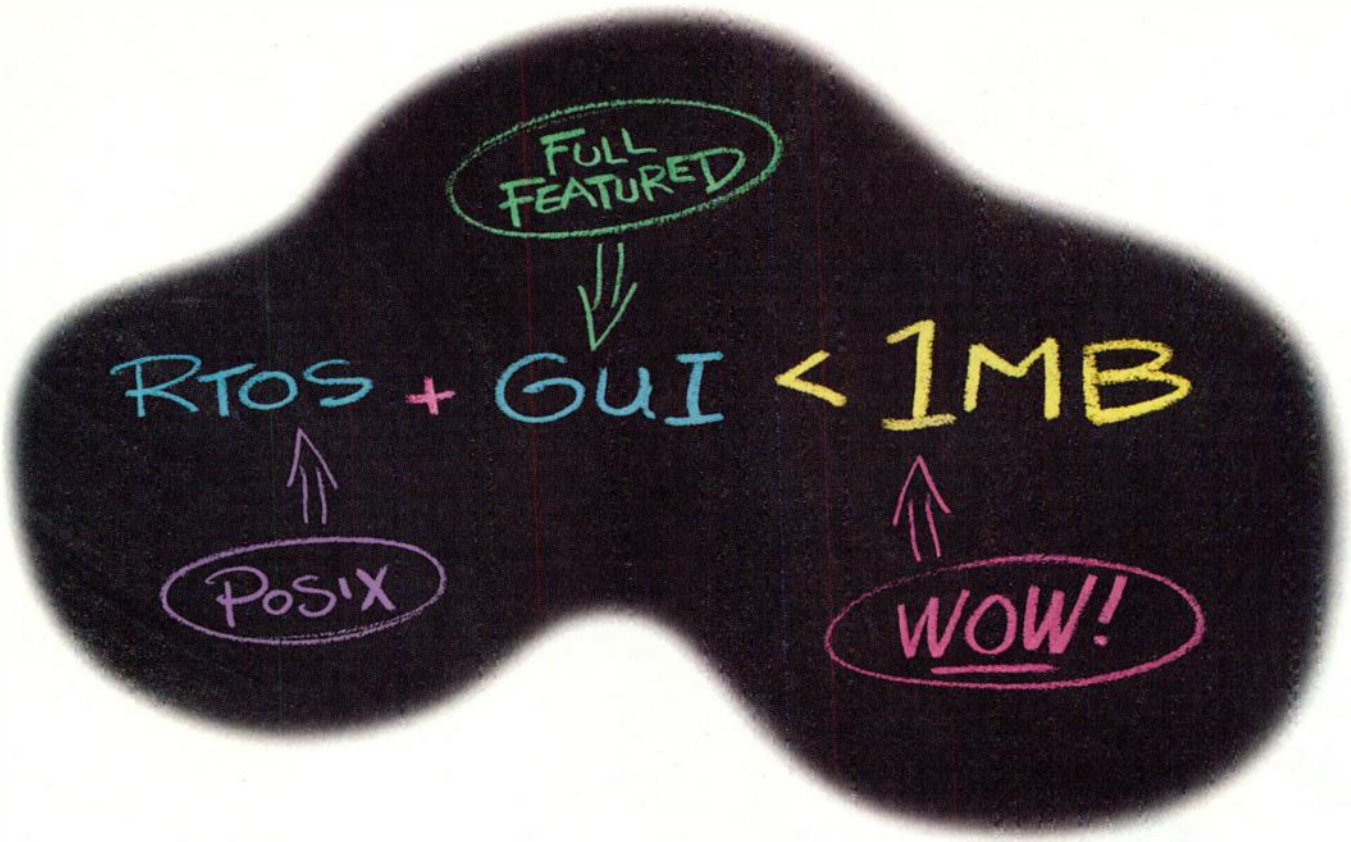
Linfinity Microelectronics Inc.
Garden Grove, CA 92641
Andrew Stewart (714) 898-8121
CIRCLE 542

Raytheon Electronics
San Diego, CA 92121
George Hill (415) 966-7819
CIRCLE 543

Semtech Corp.
Newbury Pk. CA 91320
Tony Armstrong (805) 498-2111
CIRCLE 544

VXI Electronics
Milwaukie, OR 97222
Joseph Chang (503) 652-7300
CIRCLE 545

How Valuable	Circle
Highly	537
Moderately	538
Slightly	539



Do more with less.

Most operating systems leave little room for important things. Like your application.

With the QNX realtime OS you'll pack more functionality into less memory. Achieve more performance with less-expensive CPUs. And deliver better solutions at a lower price.

Better yet, QNX supports more PC hardware than any other realtime OS. Whether it's PC/104 or PCMCIA, embedded X86 or the Pentium® Pro, QNX lets you use it right out of the box. Get to run time in less time!

More scalable than ever! From low-end to high-end, QNX offers you the ultimate in scalability. Even your deeply embedded systems can boast a scalable POSIX RTOS, thanks to our new, exceptionally small Neutrino™ microkernel.

And if you need to add the capabilities of a high-end GUI to your low-end system, you can. Our award-winning Photon microGUI™ gives you a phenomenal front end, with enough memory left over for important things . . . like your application!

www.qnx.com

Call 1 800 676-0566 (ext. 2240)
or email **info@qnx.com**

QNX®
The Leading Realtime OS for PCs

QNX Software Systems Ltd., 175 Terence Matthews Crescent, Kanata, Ontario, Canada K2M 1W8 Voice: 613 591-0931 Fax: 613 591-3579
Europe: 49 Dove Park, Chorleywood, Hertfordshire. Voice: (44)(0)1923 284800 Fax: (44)(0)1923 285868 Email: QNXeurope@qnx.com

READER SERVICE 146

They Didn't Settle for Second Best

Neither Should You.

Price/Performance Leadership

With a complete family of 32-bit RISController™ and 64-bit Orion™ microprocessors, as well as a host of development tools to choose from, IDT can make *your* next design a winner, too.

RISC without risk. To learn more about IDT's competitive RISC microprocessors, ask for the **RISC Technology White Paper**.

EZ EVAL Offer

Now it's easy to test IDT RISC CPUs. Call to qualify for a 60-day **EZ EVAL KIT** trial, which includes a 32- or 64-bit evaluation board, user manuals, and benchmarking software.

1 (800) 345-7015
ASK FOR KIT CODE 5271

WORLD WIDE WEB
www.idt.com Kit Code #5271

Integrated Device Technology, Inc.

Designing Power Systems Around Processor Specifications

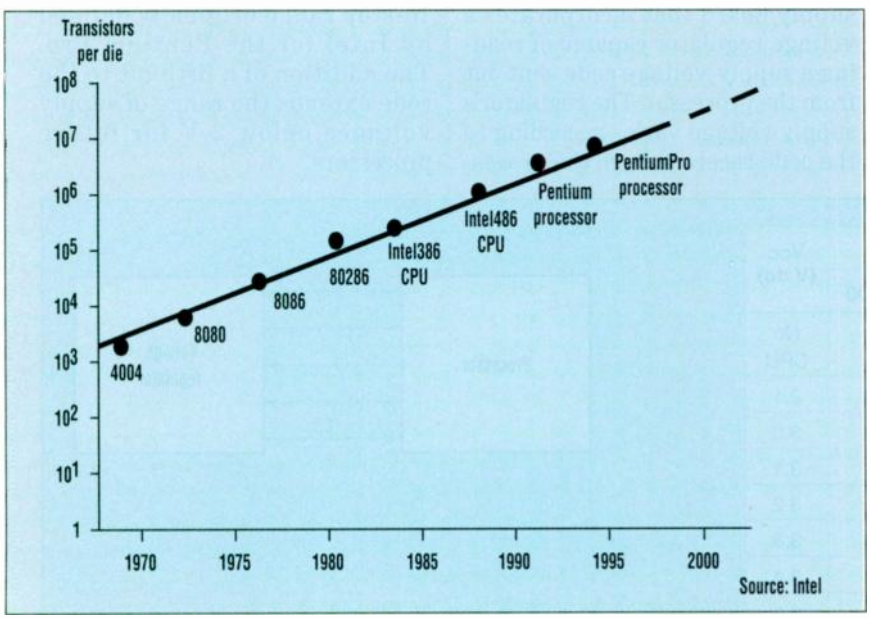
Bigger And Faster Microprocessors Demand Close Attention To The Rules For Power Conversion And Distribution.

STEVE GOODFELLOW and DON WEISS, Intel Corp. MS JF1-50, 2111 NE 25th Ave., Hillsboro, OR 97124; (503) 264-4110; fax (503) 648-4511.

A succession of trends in microprocessor technology is setting new ground rules for supplying power to these devices. The changeover began when the high-performance Pentium processor broke with the traditional model of a microprocessor, drawing its power from the 5-V plane on the system board.

With the advent of the Pentium about three years ago, two major changes occurred with respect to the way in which power is generated and distributed in a system. First, the lower voltages required by advanced chip fabrication processes drove supply voltages below 5-V. As a result, designers of systems and power conversion circuitry had to adapt to lower, non-standard (and sometimes variable) voltages. Second, the Pentium ushered in the need for aggressive power management for microprocessors running in desktop systems. Such advanced processors produce large, fast changes in the current they draw, forcing designers to use active voltage regulation closer to the load. Initially, this was not a problem because a simple solution for a load drawing less than 3 A was to place a linear voltage regulator near the microprocessor.

But microprocessor transistor counts and operating frequencies will continue to increase, leading to larger current swings and the need for developing design rules to handle new and more powerful devices. When properly followed, the appropriate design rules minimize problems and ensure that the processor's power supply will be a dependable part of the system. Designers of microprocessors, computer systems, and voltage regulation devices are utilizing these approaches to create solutions.



1. The number of transistors in microprocessors has increased steadily over the years as processing advances continue to permit smaller feature sizes. The latest Pentium processors contain over 1 million transistors and future devices may pack around 10 million.

Chip Changes

Microprocessor supply voltages will continue to fall as processor feature sizes continue on a steady downward path that has carried them below 1 micron now and a projected size of 0.2 to 0.3 µm in the next two years. Shrinking feature sizes allow many more devices to be packed on a chip, and transistor counts for Pentium processors are now in excess of 1 million and on the rise toward 10 million *(Fig. 1)*.

While processor geometries decline, the frequencies at which they operate have been rising since their introduction in 1971. The older Pentium processors run at better than 100 MHz and internal clock frequencies for the more advanced models are already at 200 MHz *(Fig.2)*. The growing number of devices on a chip together with increasing clock frequencies combine to produce larger currents than occurred with the earlier microprocessors, despite the shrinkage of feature sizes.

In just a few short years, processor current draw has increased tenfold, from about 1 A in 1992 to 10 A today . The shorter clock cycles resulting from higher clock frequencies mean that the processor is changing states faster. And the state changes include transitions back and forth between low- and high-power states leading to an increasing rate of change of current (di/dt) at the processor's power supply pins.

The tremendous changes in microprocessor architectures and comput-

ing power demand a new set of design rules to provide sufficient power for efficient and reliable operation, but such a trend has been underway for a few years. Power management—the ability of devices in a system to reduce their power consumption when at rest—began with mobile computers in response to user demand for longer battery life. The need accelerates as processors become faster and larger and thus consume more power. Power management moved to the desktop when government and commercial buyers sought computers that consumed less power during idle periods.

The result from a power supply perspective is that the supply must be prepared for a processor to shift between high and low current-draw in less than a microsecond. When desktop power management techniques began growing four years ago, processors typically drew about 1 A *(Fig. 3)*. Any increase or decrease in current was a manageable fraction of the of the several Amperes supplied by the bulk 5-V supply in typical systems. But then processors began to draw 2 to 3 A from a dedicated 3.3-V source. That meant that the total load seen by the supply could change quickly between levels approaching its minimum and maximum limits. With current loads rising even more in the latest processors, the potential current swings have grown accordingly.

System designers must power the processor from a source that maintains acceptable efficiency at the maximum load and remains stable at the minimum load. At the same time they must contend with the effects of current transients encountering the inductive elements of power distribution paths. An important design objective is to reduce the inductance in the distribution path and to increase the ability of power conversion circuitry to respond to current transients. The goal is to keep the supply voltage within processor specifications by controlling Ldi/dt voltage variations.

While computer system users seldom place a premium on power management, it is an important consideration from a designer's standpoint. The reason is that even if the system is programmed carefully to avoid power management states, load variations must be taken into account.

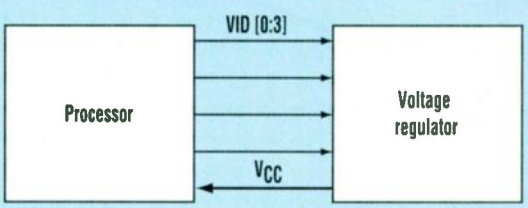
3.3 V: Here Today, Gone Tomorrow

Although Intel's top-of-the line Pentium Pro Microprocessor runs off a 3.3-V power supply and such supplies are very common in contemporary computer systems, this voltage level may not be around much longer. The prevailing trend among processor manufacturers is to get away from industry standard voltage levels like 3.3 V. Over the past few years, processor supply voltages have dropped from 5 V to 3.3 V and may go down as low as 1 V in years to come, so it becomes unlikely that a standard voltage level will work for all devices. The reason is that a processor must use a voltage that gives it an optimum mix of performance, which usually increases with a higher supply voltage, and power dissipation, which decreases with supply voltage.

To anticipate the likelihood that different processors could be used in systems depending on their performance/power requirements, designers should develop a power supply board that incorporates a voltage regulator capable of reading a supply-voltage code sent out from the processor. The regulator's supply voltage varies according to the code received from the processor. Pentium Pro processors, for example, use a 4-bit code to tell the regulator the voltage that they need *(see the figure and table)*.

A 150-MHz Pentium Pro operates from 3.1 V so it would send the regulator a 0100 code to get the proper voltage. A 180-MHz version of the device runs best at 3.3 V so its code to the regulator is 0010. The table illustrates part of the 16-step range originally defined by Intel for the Pentium Pro. The addition of a fifth bit to the code extends the range of supply voltages below 2 V for future processors.

Prcocessor pins				Vcc (V dc)
VID3	VID2	VID1	VID0	
1	1	1	1	No CPU
1	1	1	0	2.1
0	1	0	1	3.0
0	1	0	0	3.1
0	0	1	1	3.2
0	0	1	0	3.3
0	0	0	1	3.4
0	0	0	0	3.5



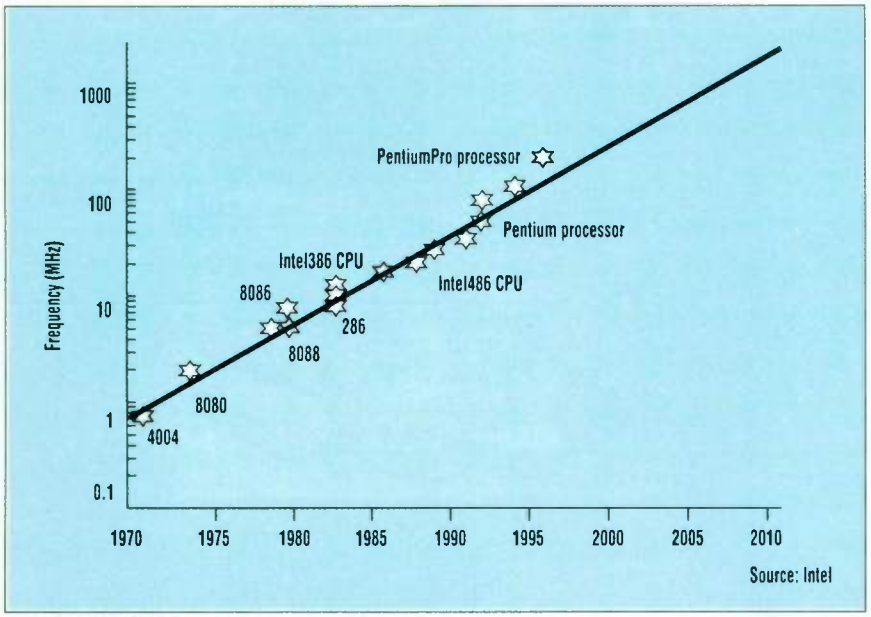
SOLUTIONS

AWARD WINNING SOLUTIONS. When it comes to selecting an electronics contract manufacturer, there's an advantage to having CELESTICA on your team – faster time to market. • Technological innovation. • Faster prototypes. • Design for manufacturability. • Cost-effective production. • Sophisticated testing. • World-wide procurement. • We're constantly fine-tuning our electronics contract manufacturing services to provide our customers with superior solutions. Put CELESTICA's know-how and resources to work for you today. CALL: **1-800-461-2913.**

Circuits Assembly
SERVICE EXCELLENCE AWARD 1995

CELESTICA™ CONTRACT MANUFACTURING SERVICES

READER SERVICE 99



2. Increasing clock frequencies improve the performance of Pentium processors, but higher-speed operation increases a chip's power dissipation. High-end Pentium processors are already at 200 MHz and the trend is clearly up for future devices.

Even without externally driven power management, large parts of the chip vary their current demands as they shift back and forth between active and idle states. As they do, the sum of their currents can show up as a sizeable current swing at the microprocessor's V_{CC} pins.

Develop Models

Early in the process, developing a power delivery system design requires accurate models for the die and package. The Premium Pro processor provides a good example for examining the delivery of power from the wall to the chip. The die and package models become part of an overall simulation model that includes interface connectors, system boards, voltage regulators and system power supplies and constitutes a power delivery system model *(Fig. 4)*. The simulation results will lead to design rules for the use and placement of high-speed and bulk decoupling capacitors, and performance and placement requirements for the voltage regulator.

The design consists of ensuring that, with a worst-case change in current demand, the voltage at the die remains within design levels. Figure 5 illustrates typical current waveforms at the interfaces. At the die level, voltage transients must be viewed as averaged over a processor clock cycle. Progressing outward from the die to the package to the board, granularity increases from nanoseconds to microseconds. At each point in the path, voltage specifications must ensure that transients at the die do not extend outside of the processor's specified minimum or maximum voltage.

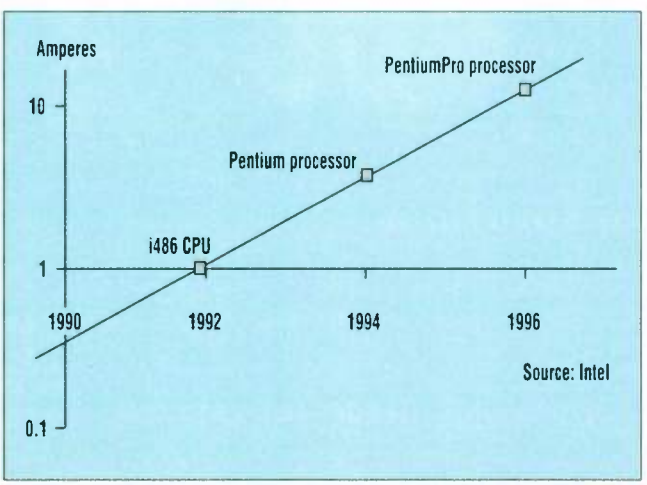
The measure of effective power delivery is the voltage at the heart of the die. If the supply voltage to devices in a critical path falls below a specified minimum during a critical clock cycle, the processor may malfunction. Voltages in excess of the specified maximum will threaten the high reliability users expect from the processor.

Meeting the V_{CC} voltage challenge begins with the chip manufacturer. High frequency design techniques call for a power distribution system that keeps voltage transients within specifications. The path requires low series resistance and inductance and low-inductance and low-resistance shunt capacitance. Since the die itself creates changes in current demand, on-die capacitors are required to handle these fast transients. This decoupling reduces the worst-case current demand at the package to approximately 4 A/ns. Decoupling on the package is designed to reduce the current ramp at the board to 1 A/ns.

The system designer must deal with this 1 A/ns worst-case transient on the board. For example, to ensure that the voltage level on the board does not vary by more than ±140 mV, the decoupling inductance is on the order of 140 pH since,

$$L = Vdi/dt$$
$$= 140 \times 10^{-3} (10^{-9}) = 140 \text{ pH}.$$

Available high-speed ceramic surface-mount decoupling capacitors have inductances on the order of 1 nH. Adding the board's trace and via inductances results in an effective decoupling-capacitor inductance of 3- to 4-nH. Approximately 30 such capacitors would be needed to achieve the desired inductance levels. A further concern is the distribution path from the decoupling capacitors to the voltage regulator. To ensure that Ldi/dt drops are within tolerable levels, the high-speed decoupling must be sufficient to reduce the effective current ramp seen by the voltage regulator to 30 A/μs. This requires that the



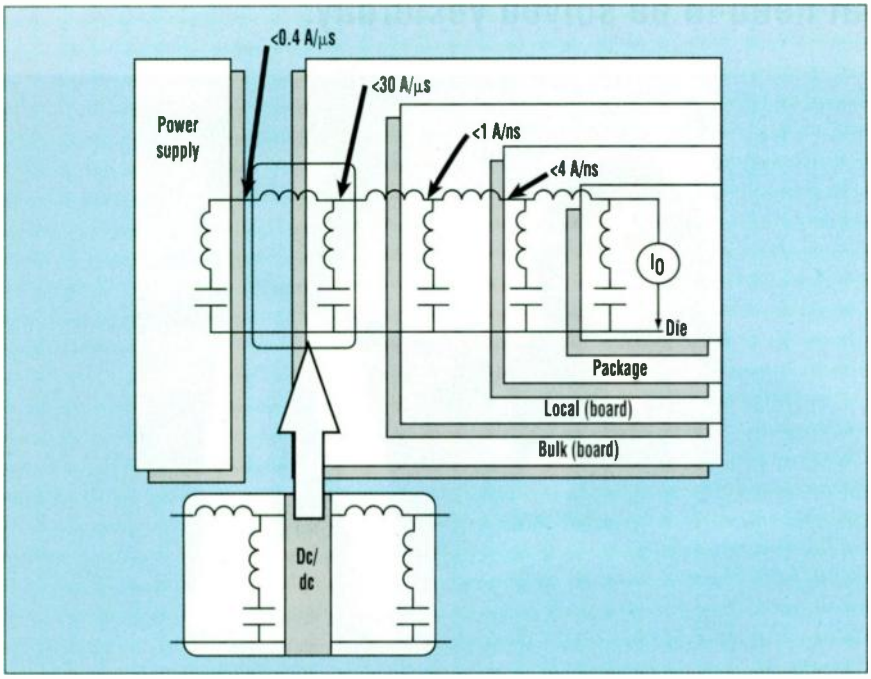
3. Dramatic changes in microprocessor current draw in the last few years are a result of increased packing density of transistors on a chip and higher operating frequencies. This places great demands on the performance of power-delivery systems, particularly with respect to current transients, which are many times greater than the steady-state value.

For today's problems that need to be solved yesterday.

The world's most powerful handheld scope.

When equipment goes down you need to fix it in a hurry, or get used to people looking over your shoulder. Fortunately, the 200 MHz THS730A handheld scope has the power to help you quickly solve the most complex design and troubleshooting problems. Its IsolatedChannel™ architecture lets you make floating measurements safely. It's the only handheld scope to offer 1 GS/s sampling rate on all channels. And it has advanced triggers for delay, pulse and video. For more information, call your Tektronix distributor today or call 1-800-479-4490, action code 727, or visit us at www.tek.com

Tektronix



4. A partitioned power-delivery system requires accurate models of the die, package and all of the boards, interconnects and other components that comprise the total simulation model. From this model comes the decision on where to place decoupling capacitors and voltage regulators.

high-speed capacitance provide about 30 µF of total filtering capacitance. The design implementation of this would consist of 30 1-µF ceramic decoupling capacitors on the board. As the microprocessor industry progresses to more sophisticated packages, the package can include these capacitors, eliminating the need for them to be mounted on the board.

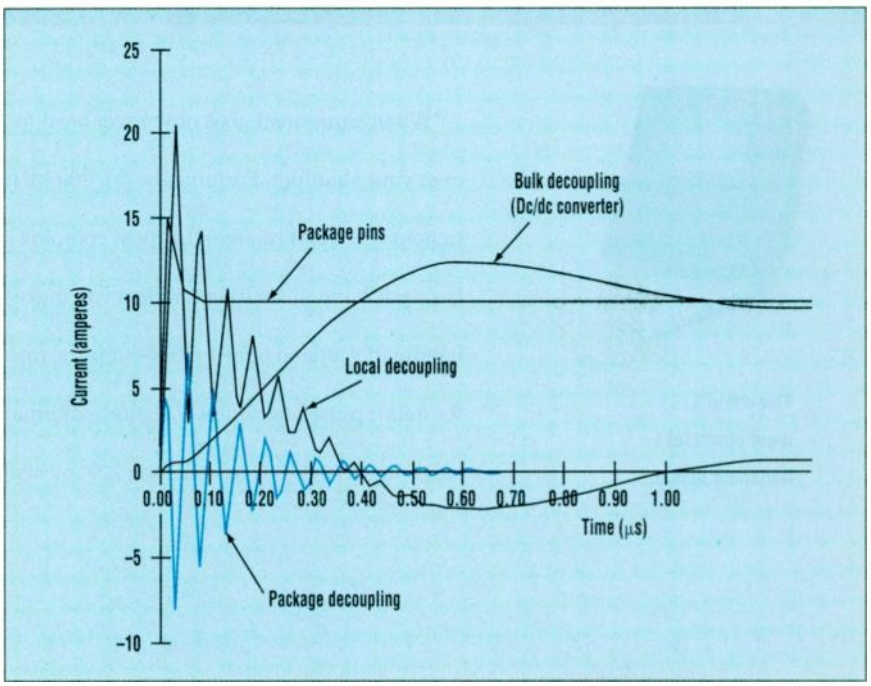
The voltage regulator supplies the current required by the processor while maintaining required voltage levels. A slew rate of 30 A/µs is beyond the capability of conventional, cost-effective regulators so low-ESR bulk capacitance is required. This capacitance will be typically on the order of tens of thousands of µF to meet slew-rate requirements, and with a parallel equivalent resistance of less than 10 mΩ. The actual amount of capacitance will vary with the response time of the regulator so an integrated approach is needed. In addition, the regulator must have additional bulk capacitance at its input to keep the current transient it presents to the system power supply within 0.04 A/µs to minimize supply transients. Otherwise, the regulator could induce transients on a 5-V input from the system power supply that would upset logic devices and cause random system errors.

Many system manufacturers meet these requirements with voltage regulator modules that contain the bulk capacitors. System designers can choose to put low cost, standard headers on their boards and use voltage regulator modules available from a number of vendors. A header provides an upgrade path for board implementations that can be adapted to future processors.

An obvious design goal is to place the voltage regulator as close as possible to the processor. However, a number of other devices should also be close to the processor, including those that must communicate with it across its high-performance bus. Maximum spacing from the regulator to the processor is a function of four factors: The overall voltage error "budget," the per-inch resistance and inductance of the interconnect, the maximum current level, and the worst-case current ramp.

Toward The Future

Advancing processor technology is pushing supply voltages down towards 1 V *(see "3.3 V: Here today, gone tomorrow," p. 54)*. Figure 3 suggests that maximum currents could be heading up towards 50 A within the next few years. This will strain power delivery technology and will require close cooperation between mi-

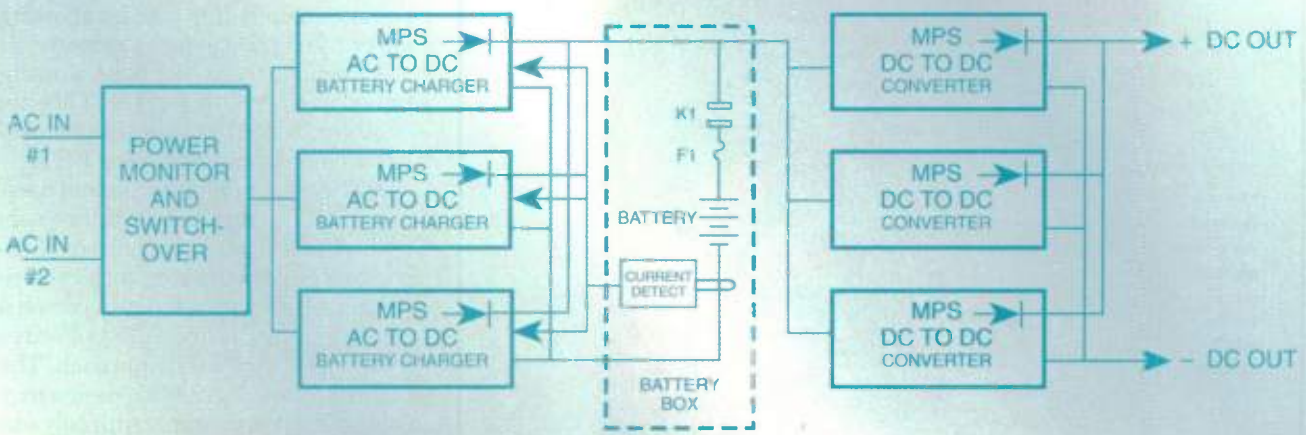


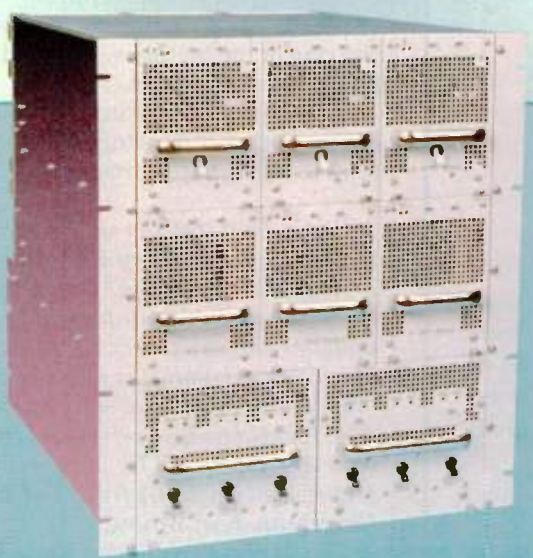
5. Typical current waveforms at the interfaces of the processor package and circuit board show that the steepest current transients occur closest to the die and reduce in severity moving outward towards the local voltage regulator. The key is to ensure that the voltage at the die does not exceed specified design levels.

MODULAR POWER SYSTEMS

FAULT TOLERANT POWER

FOR CRITICAL APPLICATIONS





Turn-Key Power Systems

- N+1 Redundant
- Battery Back-Up
- Hot Bus Plug-In
- Standard and Tailored Solutions
- From 500W to 100kW

A division of

Transistor Devices Inc.

Phone: (908) 850-5088
Fax: (908) 850-1607

36 Newburgh Road
Hackettstown, NJ 07840

www.transdev.com
info@mailer.transdev.com

READER SERVICE 180

croprocessor manufacturers such as Intel and the power conversion industry to develop solutions for the challenges ahead. These types of solutions must achieve the following goals:

- Advances in substrate technology and new capacitor designs will be required to decrease the effective inductance of on-board decoupling capacitors to less than 10 pH.
- Larger values of bulk capacitance will be required with no increase in capacitor volumes. Falling supply voltages help in this case by allowing lower rated voltage for capacitors.
- Regulator efficiency must be maintained at a level above 80%. This can only be achieved by the development of lower on-resistance switching FETs.
- The power delivery system itself also must be revisited. In future systems of this type, a centralized multiple-voltage power source, such as those that are already used today in personal computers, may not be as cost-effective as a more distributed approach. The optimal power distribution design may consist of a power source with only one or possibly two voltage outputs with the remaining voltages, supplied by point-of-load regulators.
- Finally, the solutions must meet the product cost structure of the systems using microprocessors.

Steve Goodfellow is Program Manager for Industry Enabling in Intel's Microprocessor Division 6. He works with developers of technologies such as power conversion, preparing to handle the needs of systems using advanced microprocesors. He holds a BS in electrical engineering from MIT, Cambridge, Mass., and an MBA from Indiana University, Fort Wayne.

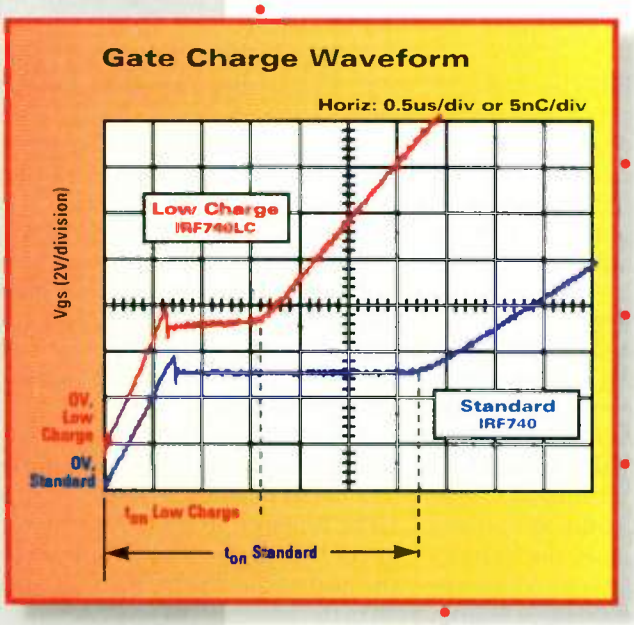
Don Weiss is a Senior Staff Design Engineer in Intel's Platform Architecture Lab. He is directly responsible for ensuring that the industry has economical power delivery solutions in place for Intel's leading-edge processors. He holds an MSEE degree from Stevens Institute of Technology, Hoboken, N.J.

How Valuable	Circle
Highly	563
Moderately	564
Slightly	565

Higher efficiency. Lower cost. Cleaner switching.

LOW CHARGE HEXFET® Power MOSFET

- *Optimized for high-frequency, high-voltage applications like power supplies and lighting ballasts.*
- *Dramatic cost and performance improvements for your designs.*
- *85% reduced Miller capacitance significantly improves dv/dt immunity.*



For the same gate drive, Low Charge HEXFET power MOSFETs cut switching time in half.

Higher Efficiency

By simply plugging in our Low Charge HEXFETs, your existing design will switch faster and with greater efficiency, thanks to a gate charge reduction of 40%.

Lower Cost

Or, on your next design, take advantage of the Low Charge HEXFET's improved dv/dt immunity to reduce or eliminate your snubber circuitry. Reduce your gate drive costs with its lower gate charge. And eliminate your gate clamping zeners with its 30V maximum V_{GS} rating.

Cleaner Switching

Or, if you have an existing design that rings or oscillates, you can use the Low Charge HEXFET (plus a larger gate resistor value) to achieve cleaner gate drive waveforms at the same frequency.

More Power To You.

Low Charge HEXFETs are the solution.

TO-220

IRF740LC–400V, .55Ω, 10A
IRF840LC–500V, .85Ω, 8A
IRFBC40LC–600V, 1.2Ω, 6.2A

TO-247

IRFP350LC–400V, .30Ω, 18A
IRFP360LC–400V, .20Ω, 23A
IRFP450LC–500V, .40Ω, 16A
IRFP460LC–500V, .27Ω, 20A
IRFPC50LC–600V, .60Ω, 13A
IRFPC60LC–600V, .40Ω, 16A

For a complete list of IR Low Charge HEXFETs, call our Fax-On-Demand system.

International IOR Rectifier

Fax-On-Demand: Doc #151
US 310-252-7100
UK 44 1883 733 420
Internet: http://www.irf.com

READER SERVICE 111

A 20-kHz Switcher Adapts UPSs For Consumer Use

By Changing From 60-Hz to 20-kHz Operation, A Flyback Switcher Cuts The Size, Weight, And Cost Of A 250-VA, 120-V Uninterruptible Power Source.

FRANK GOODENOUGH

Most of today's uninterruptible power supply (UPS) designs use a line-frequency (isolation) power transformer regardless of whether they have a high or low power rating. These transformers, consisting of bulky beige boxes have a reputation of being difficult to use and unsightly in a typical home-office environment.

In an effort to improve these devices, designers at American Power Conversion (APS) devised a low-cost and attractive 250-VA (150-W) UPS using high-frequency switching regulator techniques. Packaged as a new product called Back-UPS Office, the power source is readily manufacturable, and is contained in a rugged package with dimensions of just 2.7-in. high, 16.9-in. long, and 7.15-in. deep *(Fig. 1)*. The power source weighs in at just over eight pounds, fitting neatly under a desk or hanging on a nearby wall.

When utility power fails or goes into brown-out conditions, Back-UPS Office provides 250 VA of 115-V, of ac line power for up to six minutes. That's more than enough power to handle at least three system-critical components, such as a personal computer, monitor, and external storage device. In addition, this UPS provides surge protection for both ac and telephone lines. The latter protection is aimed at Internet users and network data lines. To facilitate this function, the unit includes a modem/10Base-T network cable port consisting of single-line- or network-compatible jacks.

Like most UPS devices, Back-UPS Office consists of five major functional blocks: a battery (sealed lead-acid type), a battery charger, an ac-dc inverter, an input-output surge protector and filtering, and a microprocessor-based controller.

Alternate Switching

As previously noted, in many of today's line-frequency UPS designs, the inverter's power FETs alternately switch the relatively low battery voltage (typically 12 or 24 V) across the primary winding of a step-up transformer at the line frequency. The transformer raises the battery voltage so that the ac line voltage appears across its secondary winding. The output waveshape is a rectanglar pulse with peak and rms values equivalent to the pure sinusoid provided by the utility.

To maximize flux coupling between the transformer's primary and secondary windings at the line frequency (60 Hz), the power supply must use a large, heavy transformer with a core of laminated iron. A typical 250-VA, 60-Hz transformer can run up to 36 in.^{3} in volume (about four inches per side), and can weigh several pounds.

To beat the weight and bulk problem, APC designers switched the operating frequency of the inverter from the typical 60-Hz line frequency to 20 kHz. That change allowed them to use a smaller and lighter, ferrite-core transformer. Instead of first converting the battery voltage to ac, and then raising it to the line voltage, the power supply first converts the battery voltage to a higher dc voltage using a 20-kHz flyback-topology dc-dc converter.

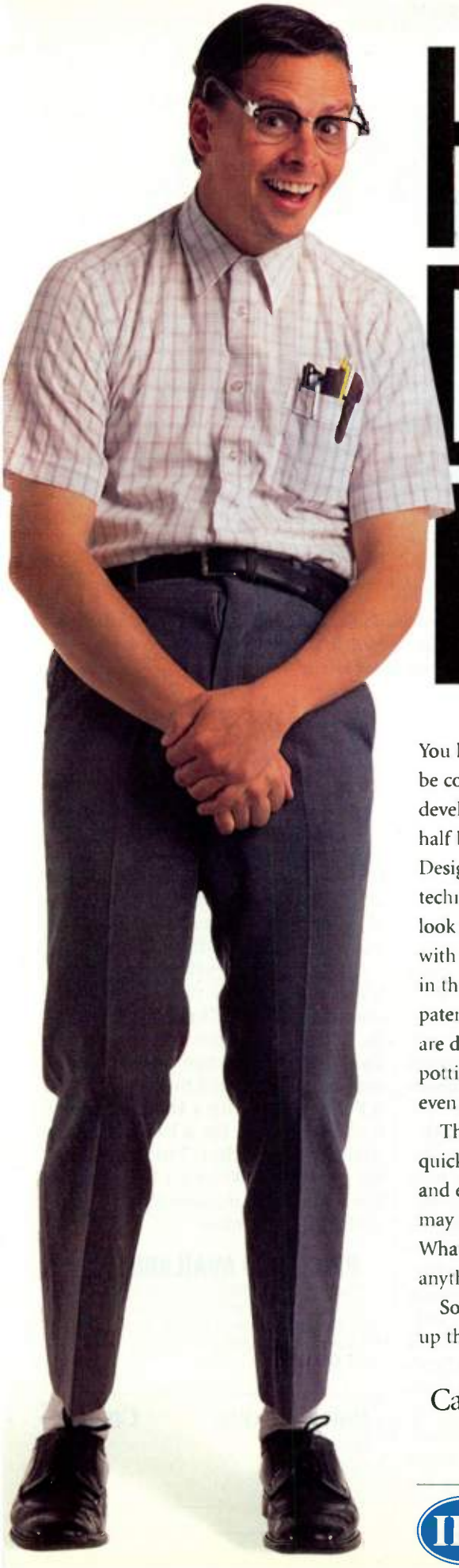
The dc output voltage of the flyback converter is set at the equivalent of the peak value needed by the UPS. A power MOSFET bridge connects this high-voltage bus across the load at the line frequency to perform the inversion to ac.

Some Squeeze

The new circuit also makes the UPS more manufacturable. The 20-kHz transformer is about nine cubic inches in volume (its dimensions are under two inches per side), and weighs only a few ounces *(Fig. 2)*. That's small enough for designers to make use of automated pick-and-place mounting on the pc board during manufacturing. The larger 60-Hz transformer usually requires bolting or riveting to a metal chassis, which adds more weight.

The final assemly process is performed manually due to the unruly flexible wires needed to connect the line cord and battery to the pc-board assembly. As a result, APC's designers fo-

1. The user-friendly UPS from American Power Supply, called Back-UPS Office, is a 250-VA uninterruptible ac-line power source that's designed for consumer use. It takes up less than 340 in.^{3} and weighs eight pounds.

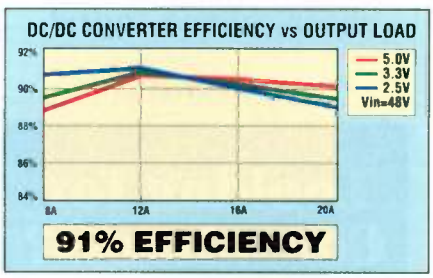


How Cool Do You Want to Be?

You know how important it is to be cool. So do we. That's why we developed new ultra high efficiency half brick DC/DC converters. Designed with advanced planar technology, these devices not only look interesting, but will provide you with the highest usable power density in the industry. In addition, our patented design is so rugged, units are delivered standard without lids or potting for optimal airflow. They're even water washable.

These half bricks are ready for quick plug-in with standard pin outs and electricals, and in many cases, may not need fans or heat sinks. What's also cool is that they'll outlive anything you've ever used before.

So what are you waiting for? Pick up the phone and give us a call today.



HE Series

50-100 Watt DC/DC Converters*

- Broad 34-75 Vdc Input Range
- Remote Sense
- Remote Shutdown
- Thermal Protection
- 1500V Isolation
- Constant Frequency
- Case Size: 2.0" x 2.28" x .490"
- Meets Worldwide Safety Requirements

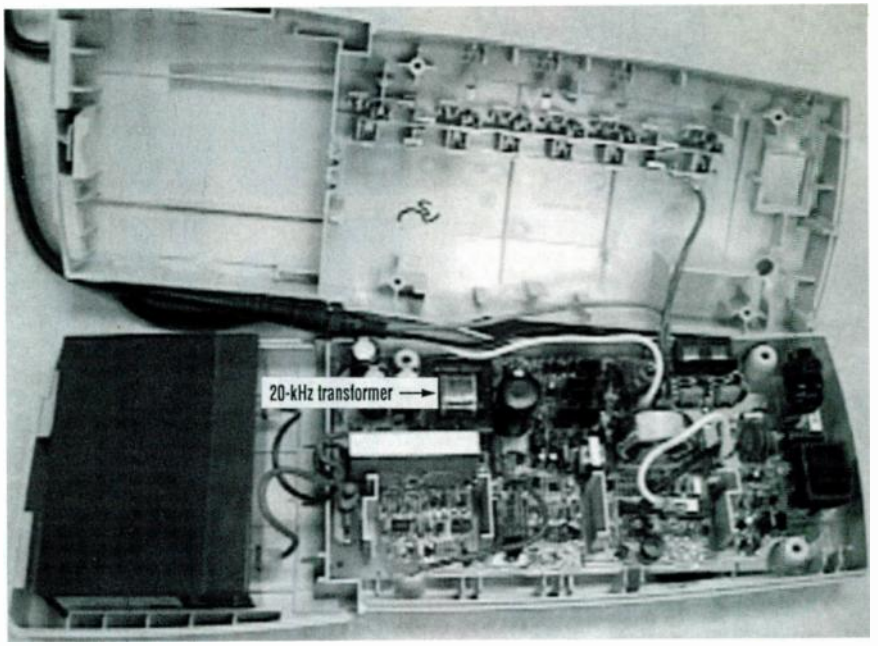
* Lower power units and smaller packages also available.

Call 617-782-3331 ext. 5146 and get all the details from one of our application engineers.

READER SERVICE 112

IPD™
International Power Devices, Inc.
20 Linden Street, Boston, MA 02134
Fax: 617-782-7416
e-mail: ipdsales@ipd-hq.ccmail.compuserve.com

Made In The USA
ISO-9001 Registered



2. Instead of using a 60-Hz step-up/isolation transformer at the output of its inverter, Back-UPS Office switched to a 20-kHz fly-back topology switcher. As a result, American Power Supply designers cut the size of their transformer from 36 in.^{3} to 9 in.^{3}.

cused on adding as much value as possible to the pc-board assembly and the enclosure early on in the design cycle. The end result is that no wires or fasteners are required to connect and mount bulky items such as the power switch, the circuit breaker, or the indicators.

Meeting Consumer Demands

Because Back-UPS Office is designed for consumer use in the home, battery replacment had to be implicitly safe and easy. It's impossible to switch a battery off, so using a battery meant that an inherent energy hazard had to be addresed. That is, designers had to make it impossible to short out the battery while it's being changed.

To solve this problem, APC's designers teamed up with battery vendors to design a battery whose terminals are recessed into its high-impact plastic case. To cut the risk of accidentally touching the connecting wires, shrouded quick-disconnect terminals are employed. The enclosure's battery compartment is covered by a lid that's removed by pushing two flexible locking tabs. Consequently, battery replacement is as simple as replacing the batteries in a TV remote control. There's no worrying about hazardous energies, or the need for complicated instructions or tools.

Back-UPS Office operates from an input-voltage range of 98 to 132 V ac and over an operating-temperature range of 5 to 113°F. It takes 6 ms (maximum) for the battery to kick in after line power fails. The surge energy rating/peak current capacity is 240 Joules/6500 A. In the course of operation, the UPS dissipates 27 BTU/hour on line, and 85 BTU/hour running from the battery.

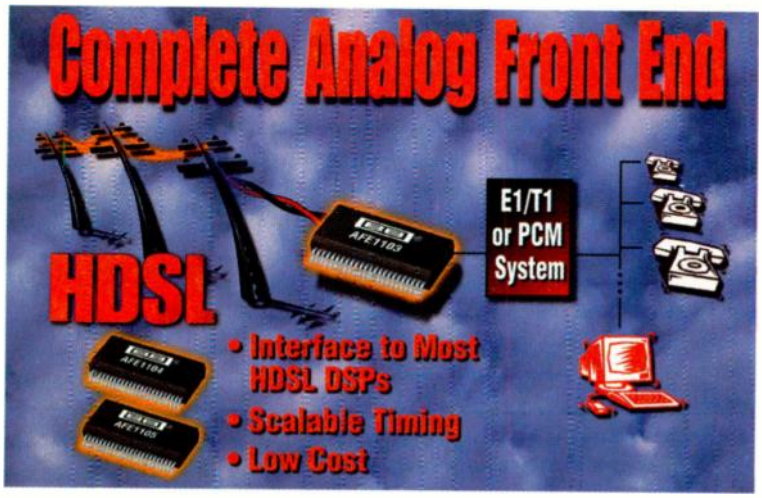
Battery recharge time can be from 8 to 12 hours. The most pertinent measure of a UPS's performance is its battery run time. A sampling of Back-UPS Office's run times for various PC products is: 5 to 6 minutes for a Pentium 133 with a 15-in. monitor; 6 to 10 minutes for a Pentium 125 with a 15-in. monitor; 7 to 13 minutes for a Pentium 100 with a 15-in. monitor; and 14 to 21 minutes for a 486/386 with a 14-in. monitor.

PRICE AND AVAILABILITY

The Back-UPS Office costs $179. American Power Conversion, P.O. Box 278, 132 Fairgrounds Rd., West Kingston, RI 01892; (401) 789-5735; fax: (401) 789-3710. **CIRCLE 556**

How Valuable	Circle
Highly	525
Moderately	526
Slightly	527

New Product Update



Analog Front End Chip for HDSL/MDSL Systems

AFE1103, **AFE1104**, and **AFE1105** are the first members of a family of Analog Front Ends (AFEs)—these single-chip solutions greatly reduce the size, cost and power requirements of an E1/T1 rate HDSL or MDSL system by providing the active mixed signal circuitry needed to connect an HDSL digital signal processor to the existing telephone company's twisted pair infrastructure. Designed for HDSL systems from PairGain Technologies, Brooktree, and Metalink, they feature a scaleable data rate to allow operation over a range of 196kbps to 1.168Mbps. Their transmit and receive filter responses change automatically with clock frequency. Each device is composed of transmit and receive sections. Applications for HDSL systems with these AFE chips include Internet access, T1/E1 transmission, MDSL, wireless base stations, network switches, routers, and internetworking. Key specs are: scaleable data rate, 250mW dissipation, and +5V single power supply. Packaged in a 48-pin SSOP and priced from **$13.40** in 10,000s.

Reader No. 81 FAXLINE No. 11331, 11330, 11346

12- & 16-Bit Sampling A/Ds with 4-Channel Multiplexer

ADS7824 and **ADS7825** are low power, monolithic 12- and 16-bit sampling A/Ds with 4-channel input multiplexer and a parallel/serial output µprocessor interface. Both can be configured in a continuous conversion mode to sequentially digitize all four channels—ideal for industrial process control, and test & measurement. Key specs: ±2 LSB max INL (ADS7825), 0.5LSB max INL (ADS7824), 16 bits DNL no missing codes, single +5V supply, and 50µW power down mode. Available in a 28-pin 0.3" DIP or 28-lead SOIC. **ADS7824** is priced from **$12.30** in 1000s; **ADS7825** from **$34.50**.

Reader No. 82 FAXLINE No. 11303, 11304

12- & 16-Bit, 100kHz Sampling A/Ds with 0-5V Analog Input Range

ADS7820 and **ADS7821** are 12- and 16-bit, 100kHz sampling A/Ds. Their 0 to 5V input range, combined with single 5V supply, make them ideal for industrial process control, test and measurement, and analytical instrumentation applications. ADS7820 key specs: 72dB SINAD with 45kHz input, and ±1/2 LSB INL/DNL. ADS7821 key specs: 86dB SINAD with 20kHz input, ±3 LSB max INL, and no missing codes. Available in a 28-pin 0.3" DIP or 28-lead SOIC. ADS7820 is priced from **$10.25** in 1000s; ADS7821 from **$28.70**.

Reader No. 83 FAXLINE No. 11322, 11323

1W Isolated DC/DC Converter in a Standard JEDEC Package!

DCP010505 is the first in a series of high efficiency, 5V input isolated DC/DC converters in industry standard JEDEC plastic molded packages. It can be assembled in high volume using standard processing and handling—no special reflow soldering processing required. Use it for point-of-use power conversion, digital interface power, ground loop elimination, data acquisition, and industrial control/instrumentation applications. Key specs: 1W power output at +100°C, 70% efficiency at full load, 1000Vrms isolation, and 400kHz switching. Packaged in a 14-pin DIP and priced from **$5.01** in 1000s.

Reader No. 84 FAXLINE No. 11336

New SoundPLUS Low Cost Stereo Audio D/A

PCM1720 is a **Sound***PLUS*, low cost stereo audio D/A complete with 3rd-order ΔΣ modulator, digital interpolation filter, and an analog output amplifier. It accept 16- 20-, or 24-bit input data in either normal or I²S formats, and operates at sampling frequency up to 96kHz. Key specs: 256fs or 384fs system clock, single +5V power supply, multiple sampling frequencies, and left, right, mono, mute output modes. Packaged in a small 20-pin SSOP (fine lead pitch) and priced from **$3.30** in 1000s.

Reader No. 85 FAXLINE No. 11333

Burr-Brown Corporation

BURR - BROWN®

IMPROVE
Your PCS Receiver's PERFORMANCE
With NEC's New Miniature 99¢ GaAs HEMTs

Need a high performance first stage LNA for your PCS, GPS, or WLAN receiver? Our new NE34018 GaAs HEMT delivers! You get low noise and high output IP_3 all in a low cost, superminiature SOT-343 plastic package. Nearly half the size of a conventional SOT-143 device, the NE34018 can help miniaturize your handheld wireless receiver design — while maximizing its performance. The NE34018 is just one in a family of new miniature plastic transistors from NEC.

If you'd like more information, call our CEL/FAX automated line. We can put data into your hands in minutes.

INTRODUCING THE NEW NE34018...

- *+30dBm Output IP_3 @ 2GHz*
- *-18dB Input Return Loss @ 2GHz*
- *0.8dB NF, 16dB Gain @ 2GHz*
- *99¢ in 100K quantities*

...IN ULTRAMINIATURE PACKAGES:

Housed in SOT-343 packages (right), these new HEMTs are nearly half the size of conventional SOT-143 devices.

PLUS TWO NEW SOT-343 MESFETs!

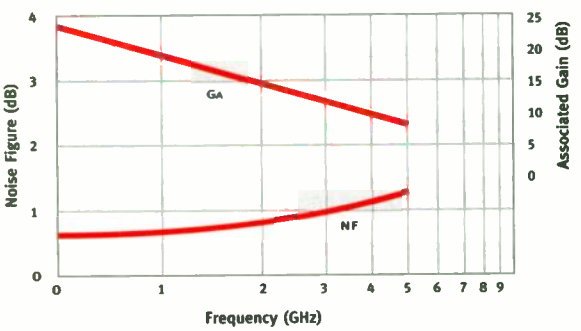
NE76118 MESFET

- *0.8dB Noise Figure @ 2GHz*
- *13.5dB Associated Gain @ 2GHz*
- *Use as an oscillator, 2nd stage LNA, or buffer amp*
- *72¢ in 100K quantities*

NE25118 Dual Gate MESFET

- *20dB Power Gain @ 900MHz*
- *1.1dB NF @ 900MHz Use as Mixer, AGC Amp, or LNA*
- *57¢ in 100K quantities*

NE34018 NOISE AND GAIN PERFORMANCE



For Instant Product Data by fax, call:

800-390-3232

For a data package call our 24 hour automated Fax number and request Document #144

(U.S. and Canada)

...or visit us at

http://www.cel.com

Booth 615 Wireless Show

NEC

CEL California Eastern Laboratories

4590 Patrick Henry Drive ▪ Santa Clara, CA 95054 ▪ 408 988-3500 ▪ http://www.cel.com

READER SERVICE 98

Architectural Breakthrough Moves Conversion Into The Mainstream

8-bit, 200 Msample/s ADC Dramatically Reduces The Number Of Comparators Needed, Die Size, And Power Consumption In Comparison With Flash Converter Technology.

Paul McGoldrick

Overcoming some of the basic limitations of the ECL-compatible flash converter has been a need of designers working in the high-speed arena. Power consumption of flash technology is relatively high and track-and-hold circuits (necessary to eliminate aperture uncertainty, or jitter) have generally been expensive and are external to the chip.

The AD9054 from Analog Devices is made on a new high-frequency process with an integral track-and-hold amplifier. It employs a novel architecture using a bit-per-stage string for the four most-significant bits (MSBs), with the four least-significant bits (LSBs) derived from a 4-bit flash converter *(Fig. 1)*. (In the few flash converters available with track-and-hold amplifiers on-chip, the power dissipation for the IC is higher than 5 W.)

Optimized For Speed

The AD9054 is an 8-bit monolithic analog-to-digital converter (ADC) optimized for high-speed operation, low-power dissipation, small size, and ease of use. The encoding rate is at least 200 Msample/s while the full-power (–3-dB) analog bandwidth is typically 380 MHz. The input interfaces directly to TTL, CMOS, or positive-ECL levels in either a single-ended or in a differential mode. With a built-in +2.5-V bandgap reference, most circuit applications will require only the provision of a +5-Vpower supply and an encoder clock source. Clock and control signals also can be driven in single-ended fashion or differentially at TTL, CMOS, or PECL logic evels.

The IC has two built-in track-and-hold amplifier stages with the first acting as a buffer in a master-slave arrangement *(Fig. 2)*. Input resistance is typically 65 kΩ with just 2 pF of input capacitance. The master-slave setup allows the input to be optimized while isolating the ADC from duty-cycle variations of the clock. The performance of the track-and-hold amplifier is better than that which could be identified as an external component to a flash converter, while novel circuit techniques have been designed to maintain harmonic distortion performance up through the Nyquist frequency in the all-npn process. Both second and third harmonic distortions are at –60 dBc for an input frequency of 10.7 MHz, and –56 dBc for 76 MHz, while two-tone intermodulation distortion is at –60 dBc.

A Patented Architecture

The bit-per-stage encoding is formed by a patented Analog Devices architecture called MagAmp (magnitude amplifier.) Each MagAmp determines one bit and passes a residue signal on to the next stage; the residual from the fourth MagAmp passes to a 4-bit flash converter *(Fig. 2, again)*.The segmentation between the MagAmp and the flash was determined as the best compromise between speed, power and die size. The number of comparators in a

flash analog-to-digital converter would be $2^n - 1$, which for an 8-bit converter would be $2^8 - 1 = 255$. With the MagAmp / flashconverter arrangement, the comparator count is dramatically reduced with $2^4 - 1 = 15$ comparators for the 4-bit flash plus one comparator for each MagAmp, yielding a total comparator count of 19. This is a dramatic savings in the comparator array design and gives large power reductions.

The MagAmp cell consists of a comparator cell plus an amplifier. The comparator determines the bit and sign of the signal with the amplifier creating the residue signal for the next stage or the flash. The output of the MagAmp is a folded replica of the input with the location of the fold being designated by the comparator trip point *(Fig. 3)*.

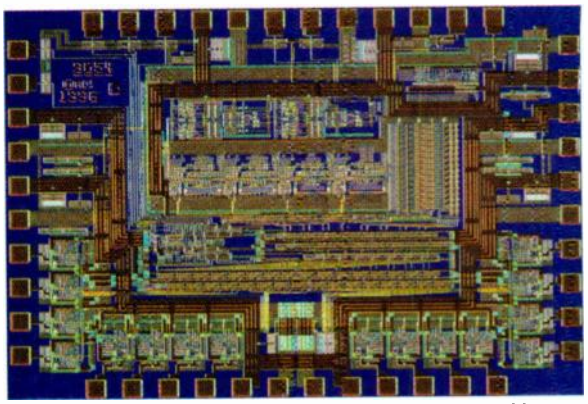
The same single-bit-per-stage architecture has been used in previous, but slower, Analog Devices' products such as the following devices: the AD9042 (12-bit, 41-Msample/s) for terrestrial base-stations; the AD9057 (8-bit, 60-Msample/s) for camcorders; and the AD9059 (dual-version of the AD9057.)

To maintain the highest possible bit-error rate (BER), the data from the MagAmp and flash sections of the encoder are in gray-scale format. A separate decoder converts the data into binary format and feeds them to a switchable 2:1 de-multiplexer, and is user-selected through a Format select line to give either dual- or single-channel outputs *(Fig. 2, again)*

. In the demultiplexed position the digital output is interleaved to the two 8-bit TTL output banks (each at one-half the clock rate) such that the ADC can be operated at the full 200-Msample/s conversion rate. With the demultiplexer switchedto the off,condition, the digital output is directed at only the A output bank and the data conversion rate is limited to 100 Msamples/s.

In the demultiplexed condition, the cost and speed of the external digital interfaces is considerably reduced by providing TTL-compatible outputs. This allows the converter to interface with standard TTL/MOS gates, including those in ASICs. Sixteen TTL outputs could, however, have produced a considerable drain on the power-supply rail so it was necessary to produce a design having variable-drive capability

The circuit determines drive current based on the difference between the internal control signal and the external data bit. Only small amounts of steady-state current are drawn and the output stages can switch 10 pF at 100 Msample/s. The data align input information from the user aligns the data with specific encode edges to ensure the outputs end up at the expected ports.

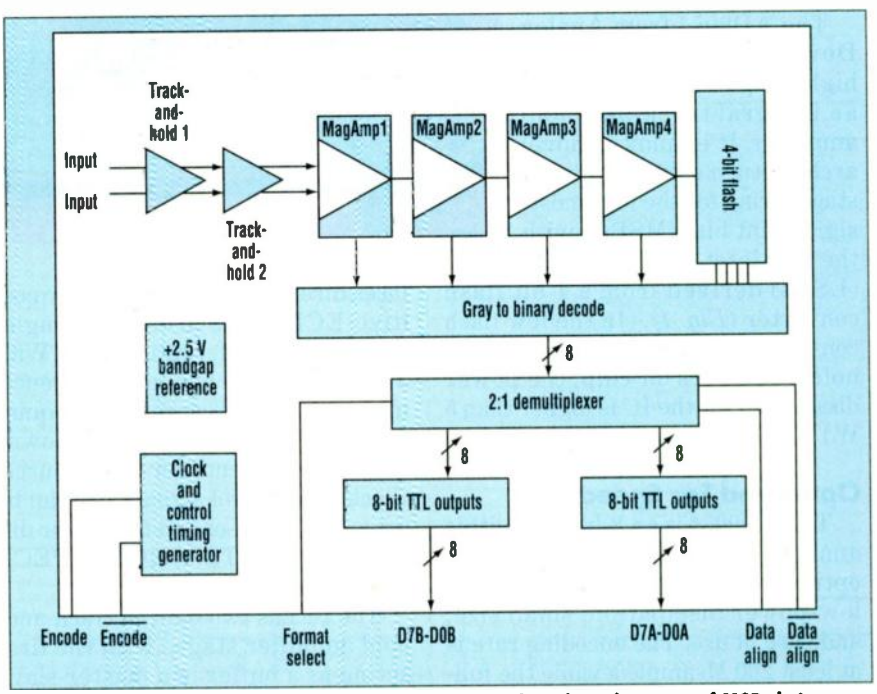


1. 200-MSample/S Analog-to-digital conversion is possible with this 8-bit, low-cost device from Analog Devices. The AD9054 employs a novel architecture that dramatically reduces the number of comparators needed, makes for a small die size, and cuts down on power consumption compared with flash technology.

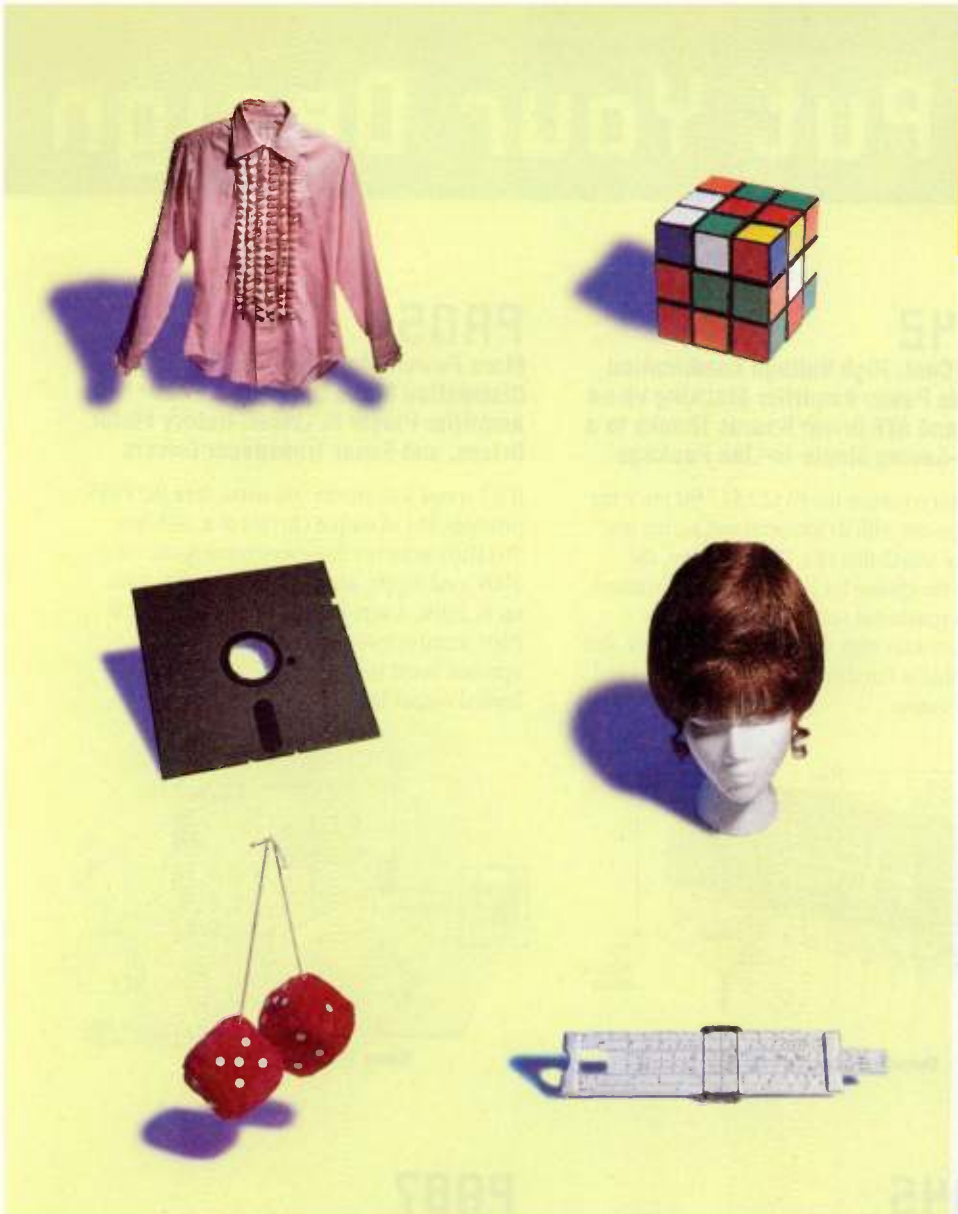
CMOS Without The Oxide

The AD9054 is being fabricated in a new high-frequency process, known as EP-107, in Analog Devices' wafer fab facility in Limerick, Ireland. The semiconductor process is actually a 0.6-µm biCMOS one with an f_T of 20 GHz produced on 6-in. wafers.

The performance of the npn transistors in the circuit gives the breakthrough encoding-rate speed and analog bandwidth of the IC. The oxides in the biCMOS process had, however, not been qualified at the time of the design of the ADC. As a result, the present circuit is completely fabricated in bipolar technology and it therefore can be compared directly with bipolar flash converters which typically dissipate 2 W at the 150-Msample/s mark but are burdened with the limitations of ECL output levels and external latch-and-hold, circuits compared to the 500 mW dissipation of the AD9054



2. Block diagram of the Analog Devices' AD9054 shows the split architecture of MSBs being encoded by MagAmps (magnitude amplifiers) and the LSBs by the flash.



FLUKE®

Some things come and go.

Others last a lifetime.

Introducing The Fluke Lifetime Limited Warranty For Multimeters.

Some things you buy on a whim. And regret later. But now we have something you'll never regret: genuine Fluke Digital Multimeters, backed by our new lifetime limited warranty.

Every member of our rugged and reliable Fluke 20, 70, and 80 Series DMMs now comes with our new lifetime warranty. That's a lifetime longer than standard warranties on the other bargain-basement meters.

Limited Lifetime Warranty! Keep your Fluke meter up and running

Which is reassuring. As is knowing that you've already purchased the DMM known for its unsurpassed quality, reliability, accuracy, and ruggedness.

Every Fluke multimeter is built in the United States, under a quality system certified to meet ISO 9001 requirements. They're easy to use, with faster response times that give you readings in seconds, and at a glance.

It's no wonder millions of professionals have chosen Fluke DMMs as the only name they trust.

For more information on the DMMs that last a lifetime, call Fluke today at 1-800-44-FLUKE. Or visit our website at www.fluke.com. It's one move you won't live to regret.

Fluke. *Keeping your world up and running.*

READER SERVICE 103

Power Amplifier Solutions

Put Your Design

With more than 80 models of high power, high voltage and PWM amplifiers, Apex Microtechnology has the off-the-shelf solutions to help trim your design time. You work smarter, faster. Besides a reduction in design time, you'll reduce your circuit's size and weight, reduce procurement time and costs. You'll also benefit from the higher reliability that's built into each Apex hybrid and monolithic power amplifier design.

Free Data Book and Application Notes

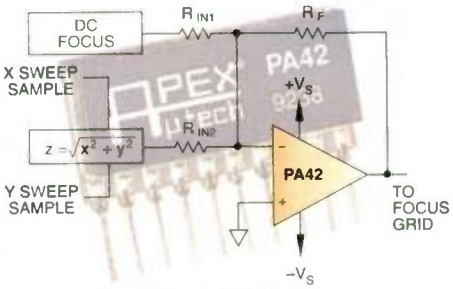
Information on all 80 models of Apex power and PWM amplifiers is provided in the new 7th edition Apex Power Integrated Circuits data book. To request your free copy, call 1-800-862-1021, fax 520-888-3329, or e-mail ProdLit@teamapex.com. Or visit our web site at www.teamapex.com.

www.teamapex.com

PA42

A Low Cost, High Voltage Combination has this Power Amplifier Stacking up on Piezo and ATE Driver Boards Thanks to a Space-Saving Single-in-Line Package

When you combine the PA42's $17.90 price tag in 10K pieces with its footprint measuring less than one fourth that of a TO-3 package, the PA42 is the choice for high density applications. Its 2mA maximum standby current is also consistent with high density, and remember, this monolithic is rated up to 350V total supply and 120mA output.

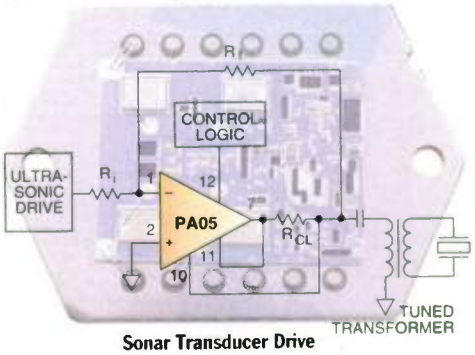


Dynamic Focus, CRT Display

PA05

More Power, More Speed, More Internal Dissipation Make the PA05 a Power Amplifier Player in Linear, Rotary Motor Drives, and Sonar Transducer Drivers

If it's speed with power you need, then the PA05 provides 30A of output current at a 100V/µs. The PA05 achieves this exceptional speed on a 100V total supply while it internally dissipates up to 250W. A very flexible power op amp, the PA05 features external shutdown control, optional boost voltage inputs and thermally limited output stages.

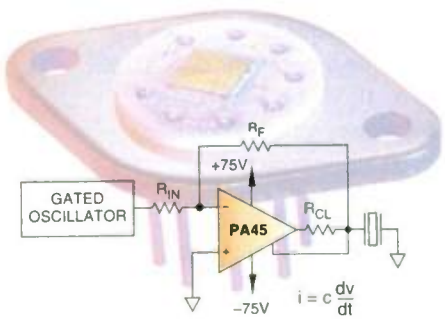


Sonar Transducer Drive

PA45

One Die does it All for this Monolithic Power Amplifier Rated at 5A Output, 150V Total Supply, Making it Ready to Drop into Transducer Drives And Magnetic Deflection Applications

Going beyond the realm of most hybrid power amplifiers, the monolithic PA45 pushes a 150V supply range while delivering up to 5A output current, and a 27V/µs slew rate. The PA45 is capable of 85W of power dissipation and is priced $17.90 in 10K pieces.

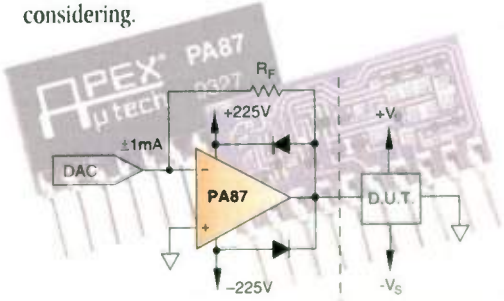


Simple Piezoelectric Transducer Drive

PA87

This Hybrid Keeps its Cool While Running on High Voltage Supplies and Delivering 200mA Continuous Current in Programmable Power Supplies and HV Instrumentation Applications

The PA87 combines a 450V total supply with 200mA of continuous output current while running cool with only 3.8mA max standby current. This makes the PA87 an attractive solution for driving large capacitive loads and powering piezoelectric applications. Its 10-pin hermetic SIP package makes the PA87 a solution that's easy to apply and certainly worth considering.



ATE Pin Driver

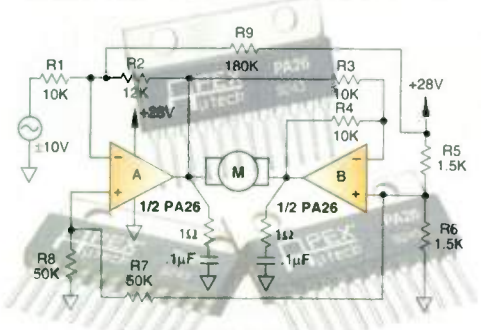
On The Fast Track

Power Amplifier Solutions

PA26

Two 2.5A Rated Amplifiers on One Die, in One Package, Priced $3.45*, Are the Many Reasons this Power Amplifier is a Popular Fit for Half, Full Bridge Motor Drivers

The PA26 saves valuable real estate by putting two 2.5A rated power amplifiers on a single die, in a single 12-pin SIP package. The PA26 provides the fit for bridge mode configurations or applications designed with multiple amplifiers per board. The PA26 is also extremely affordable priced at *$3.45 in 10K pieces.

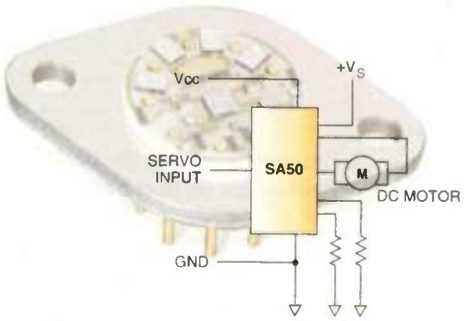


Bidirectional Small Motor Drive

SA50

This Low Cost, Complete H-Bridge Hybrid PWM Amplifier Is Available Fully Screened To MIL-H-38534

The SA50 offers full bridge operation up to 80V with 5A of continuous output. Rated 97% efficient, the SA50 delivers up to 400W to the load. Inside its hermetic, TO-3 package, this hybrid contains smart lowside/highside drive circuitry, as well as internal PWM generation to allow switchmode operation from an analog signal.

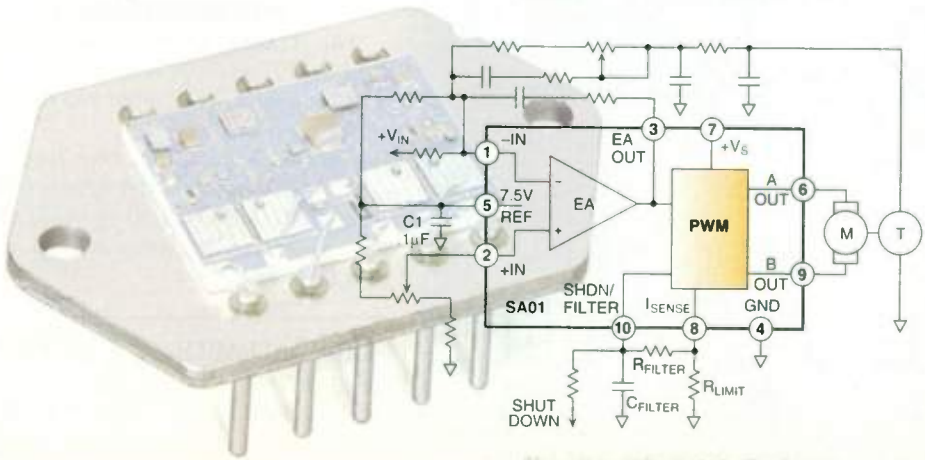


Servo Motor Driver

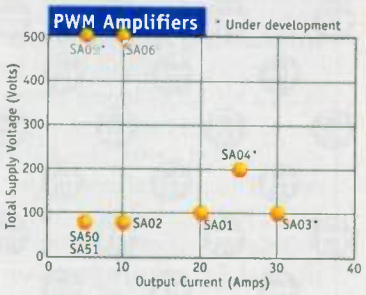
SA01

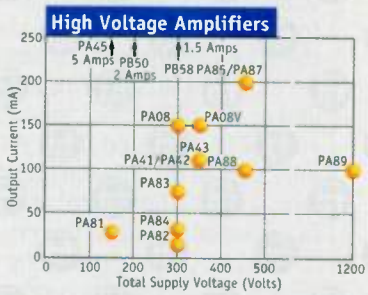
This Industry First Hybrid PWM Amplifier Switches Its Way To 97% Efficiency And 2000W of Power in Brush Type Motor Control, Reactive Load Applications

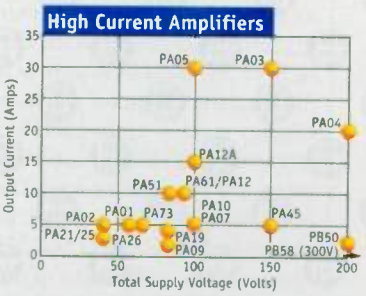
Also known as a switching or Class D amplifier, the SA01 is an industry first hybrid PWM (Pulse Width Modulated) amplifier. High efficiency is the beauty of PWM technology, and with a 97% efficiency rating, operational on single supplies up to 100V and capable of 20A continuous, the SA01 can deliver up to 2000W to the load while reducing the need for bulky, space consuming heatsinks. The SA01 is also loaded with thermal protection features inside its hermetic power-dip package measuring just 2in².



Motor Drive With Tach Feedback







For Immediate Product Information
Call **1-800-862-1021**
or FAX **(520) 888-3329**

To Request Our Free Data Book Online
E-Mail: **ProdLit@teamapex.com**
or **http://www.teamapex.com**

ISO9001 CERTIFIED

APEX µtech
DEDICATED TO EXCELLENCE

Apex Microtechnology Corp.
5980 N. Shannon Road
Tucson, Arizona 85741-5230

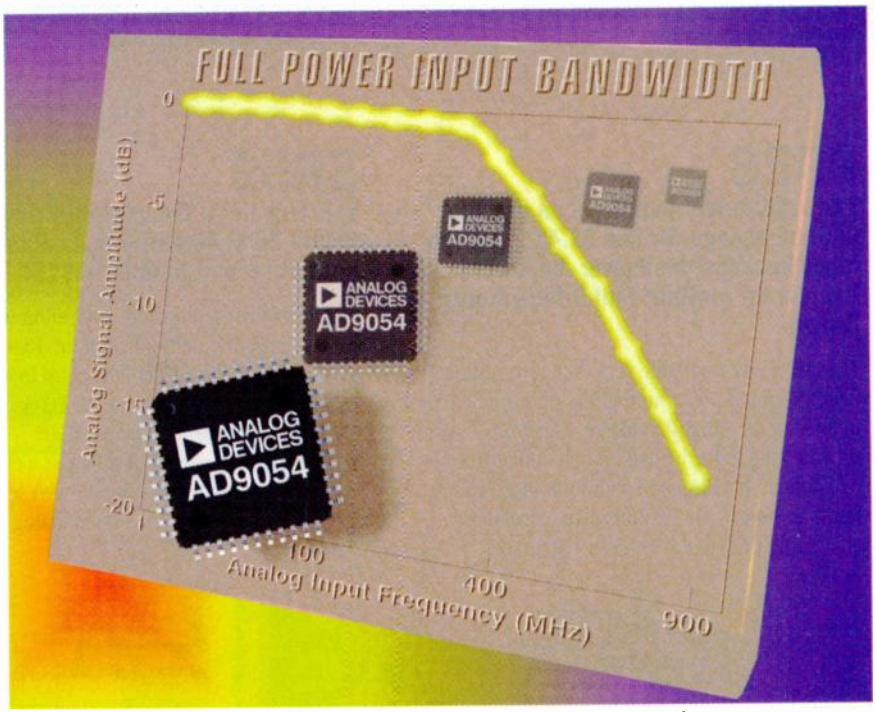
READER SERVICE 166

with the analog bandwidth secured internally.

Interesting Applications

The fact that the ADC is bipolar but is on a biCMOS-based process allows for some very interesting future design projects with the AD9054 at its core. The applications of the AD9054, as is, will include medical imaging processors, digital instrumentation, digital data storage channels and video processing. Those sound rather basic but there are some enormous implications. In digital instrumentation, for example, where the existence of the IC could open up a completely different, and larger, range of digital storage oscilloscopes, previously the cost of high-speed flash ADCs was only part of the implementation problem, with the input analog circuits being a major, separate, limitation.

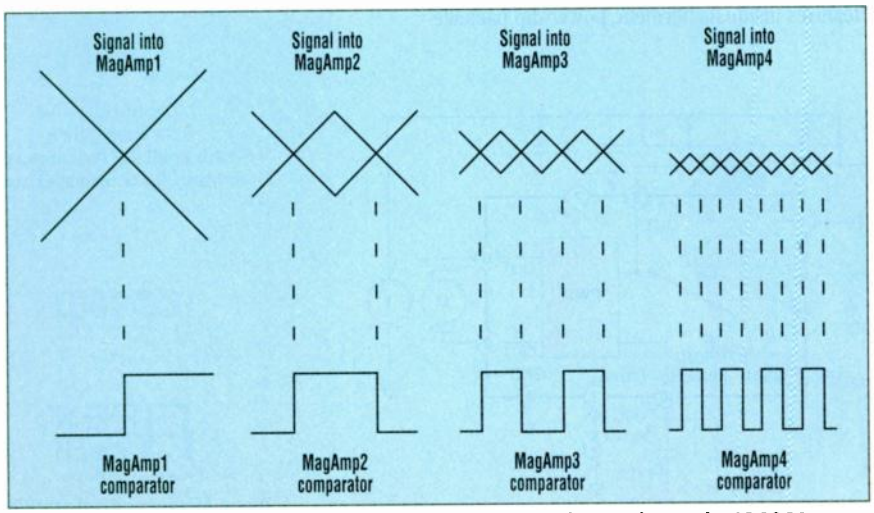
In video, 8-bit processing for RGB analog-to-digital conversions is currently sufficient for the display market, but the devices have not been available for the conversion of the higher pixel rates. With three channels of AD9054 ICs operating at 200 Msample/s, the pixel rate needs for all display modes up to 1280 by 1024 are covered, and most of the 1600-by-1200 rates are covered as well (frame rates of 75, 80 and 85 Hz produce pixel rates between 202.5 and 229.5 MHz.) This opens up the possibility of direct drive by analog RGB signals into high-resolution scan converters, LCD monitors in projection, and micro-mirror and plasma forms. It is expected that a number of video products that use the same process will be coming from the group in Limerick in the near future.



4. Performance curve for the AD9054 shows the plot of signal-to-noise + (distortion) ratio (SINAD) against the input frequency.

The ADC also opens up another segment of the direct-conversion market in the general communications sectors with quadrature-amplitude modulation (QAM) demodulators for cellular and satellite base-stations and the implementation of simpler, and cheaper, spread-spectrum receivers. The product also should allow the economic development of some medical imaging projects that have been languishing.

Other performance measures of the ADC are that there are guaranteed no missing codes, and both differential and integral nonlinearity are typically within 0.75 LSB. The converter also features zero-gain error. Aperture delay is typically 2 ns, while aperture jitter is typically 5 ps rms. The effective number of bits is typically 7.35 at 10.3 MHz and 6.70 at 76 MHz; signal-to-noise+(distortion) ratio (SINAD) slips from 46 to 42 dB from 10.3 to 76 MHz *(Fig. 4)*. For video uses, differential phase typically measures 0.8° and differential gain is 1.0%. The input voltage range is 1 V peak-to-peak centered at +2.5 V with no input offset voltage.



3. Signal and comparator waveforms of the four MagAmps in the encoding in the AD9054.

PRICE AND AVAILABILITY

The AD9054 is available in a 44-lead TQFP package and is sampling now. The part is priced at $25 each in 10,000-unit lots.

Analog Devices, Inc., One Technology Way, Norwood, MA 02062; (800) ANALOGD (262-5643) or (617) 461-3392; Internet: http://www.analog.com.

CIRCLE 503

How Valuable	Circle
Highly	534
Moderately	535
Slightly	536


Lack of Board Space Bugging You???




NEW SOT-23 Tiny Package Amps from the High Performance Amplifier Leader

Footprints about one-fourth of the board space compared to the SO-8

Actual Size

SOT-23 SO-8

EL2150C 125 MHz
5 mA, Single Supply Amp

- +3V to ±6V Operation
- Input/Output – Common Mode to Ground
- $2.29 in 1,000 units

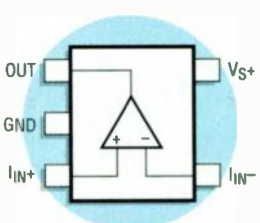
EL2170C 70 MHz
1 mA, Current Mode Amp

- +3V to ±6V Operation
- 100 mA Output Current
- $1.90 in 1,000 units

EL2180C 250 MHz
3 mA, Current Mode Amp

- +3V to ±6V Operation
- 1200 V/µs Slew Rate
- $1.99 in 1,000 units

Attention Designers!
E-mail us with your e-mail address so that we can keep you apprised of the most recent product info, and we'll send you our new 1997 Data Book.



Contact factory to find out about other amplifiers that will be available in the SOT-23 package

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Elantec's full amplifier product line is available in our 1997 Data Book, 1997 Short Form Selection Guide, or call our literature hot line at 1-(800)-882-2109, faxback service: 1-(800)-328-2113, e-mail: info@elantec.com, and our world wide web site: http://www.elantec.com – For samples/technical questions: 1-(888)-ELANTEC.

ELANTEC SEMICONDUCTOR, INC. ■ 675 Trade Zone Blvd. ■ Milpitas, CA 95035 ■ (408) 945-1323 ■ (800) 333-6314 ■ FAX (408) 945-9305
European Sales: 44-171-482-4596 ■ FAX 44-171-267-1026

Distributed by: Marshall Industries ■ Insight Electronics ■ Nu Horizons ■ Gerber Electronics ■ Zeus/Arrow

READER SERVICE 170

Silicon MEMS Technology Is Coming Of Age Commercially

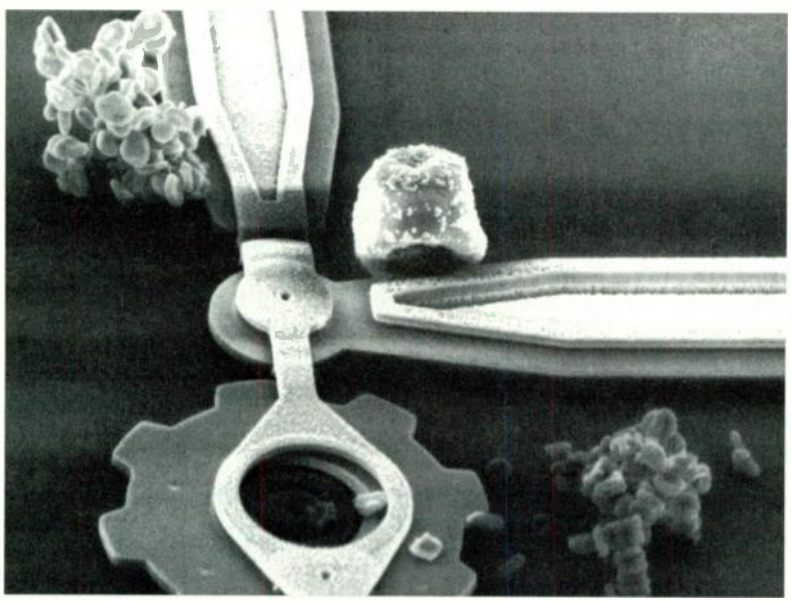
Micromachined Sensors And Actuators Are Expanding Into New Applications As They Tackle The Challenges of Scarce CAD Tools, And A Lack Of Standardized Packaging And Testing Methods.

Roger Allan

Microelectromechanical systems (MEMS) technology is coming of age. That was the message emanating from "The Commercialization of Microsystems '96" Conference, Oct. 6-11, Kona, Hawaii. The conference was cosponsored by Semiconductor Equipment Manufacturers International (SEMI) and the Engineering Foundation.

MEMS refers to a broad class of micromachined sensors, actuators, and systems that exploit electrical, mechanical, radiant, thermal, magnetic, and chemical phenomena. Although most MEMS chips are made of silicon, they also can be made of other materials (ceramics, quartz, polymers, plastics, thin films, magnetic metals, as well as other kinds of metals). While MEMS devices like pressure sensors, accelerometers, valves and spray nozzles have reached full commercialization,a host of equally-lucrative applications are alos awaiting full commercialization *(Fig. 1)*. They include chemical, biomedical, vibration, flow, temperature, and humidity sensors, pumps, gyroscopes, latches, mass-storage devices, microfluidic systems, relays, switches, micropositioners, active filters, displays, deformable optics, microoptical benches, active conformable surfaces, and military applications. And more applications opportunities are emerging *(Table 1)*.

SPECIAL REPORT



Output gear of a microengine developed by Sandia National Laboratories. Individual red-blood cells at lower right and upper left are shown for comparison. A grain of pollen sits in the center.

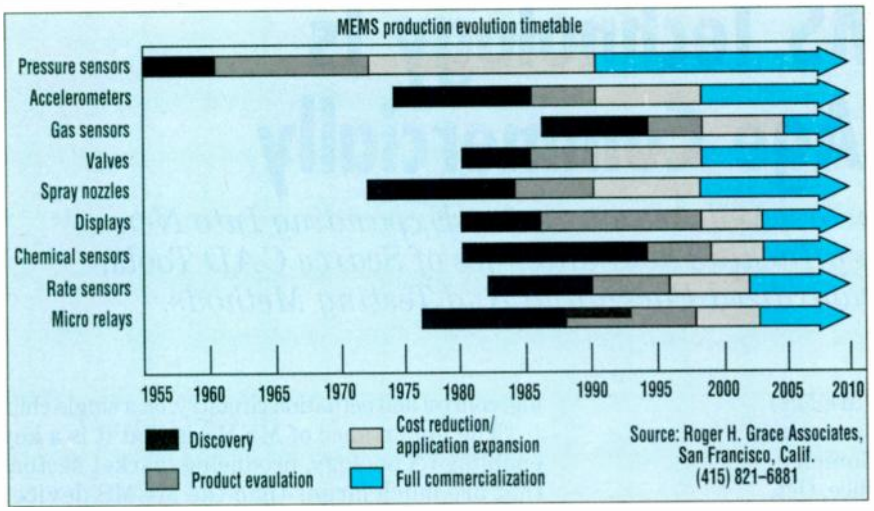
For the first time, MEMS devices are putting the digital electronic revolution "in touch" with real-world analog variables of pressure, temperature, speed, acceleration, humidity, fluid flow, and so on. The possibility now exists for a total closed-loop control system, complete with sensing, control and actuation circuitry, on a single chip.

"The importance of MEMS is that it is a key enabling technology, producing market sectors that are much larger than the MEMS devices themselves," according to Roger H. Grace, president of Roger H. Grace Associates, San Francisco, Calif., a technology marketing consulting firm. For example, micromachined tips for scanning-force microscopes, produced by many, cost only a few dollars, yet they're critical for the production of microscope systems costing upwards of $100,000. The micromachined accelerometer is another example. Used for air bags in autos, it costs only about $5, but it makes possible total air-bag systems costing around $200. He compares MEMS ICs as technology enablers to the microprocessor that enabled the computer revolution.

Even the most pessimistic estimates put the total MEMS market at several billion dollars. Dr. Guido Tschulena, sgt Sensor consulting, Wehrheim, Germany, estimates the MEMS market will go from $3 billion in 1995 to roughly $13 billion at the turn of the Century. And worldwide funding for MEMS R&D seems to support that view.

Applications Abound

In a harbinger of things to come, Motorola Semiconductor Products, Phoenix, Ariz., recently introduced one of the first low-cost commercial CO gas sensors, retailing for $10 each in what Motorola says "low-volume" quantities. The development was an international effort, involving a licensing agreement with the Swiss



1. By the turn of the century, more MEMS applications are projected to reach full commercialization. One promising application not shown is photonics/optoelectronics, for which there was insufficient data to project at the time this article was prepared.

company Microsens S.A. The sensor was developed and is manufactured at Motorola's Center of Excellence, Toulouse, France.

MEMS developments are worldwide, with Europeans mounting a strong effort *(Table 2)*. MEMS funding in Europe, Japan, and the Far East, is pervasive, with national, regional, state, and local governments providing programs and funds to MEMS companies and academic organizations. In the U.S., funding also has been forthcoming. However, much of it has involved money for large national and academic laboratories *(see "Needed: A greater U.S. commercial-funding effort," p. 80)*.

The European Commission has funded the Europractice project as part of the Espirit Program. Composed of four clusters of companies, the project's goal is to improve the competitiveness of the European microsystems technology (MST) effort through the use of the latest technological tools and techniques, with recent emphasis being put on greater commercialization of and better user access to MSTs *(Table 3)*. (Note: MSTs, as Europeans call them, include sensors, actuators and microstructures, as well as other microtechnologies that could be processed mechanically. MEMS is a major subset of MSTs).

One such company pushing the commercialization effort is Switzerland's CSEM in Neuchatel, a leader in producing microminiature structures. Last year, CSEM unveiled a coil-based micromachined sensor for automotive speed and position sensing, as well as a wireless transceiver that measures a car tire's pressure and temperature.

Automotive applications are the largest MEMS market, with medical (mostly disposable blood-pressure sensors) and industrial applications following suit. Recently, Analog Devices, Wilmington, Mass., spearheaded the development of surface micromachined automotive sensors with a MEMS automotive accelerometer.

German companies like Siemens AG in Munich, Robert Bosch GmBH in Reutlingen, and Temic GmBH in Helbronn (a subsidiary of Daimler-Benz) also are eyeing the automotive micromachined sensor market, particularly accelerometers for air bags.

As mentioned earlier, silicon is not the only micromachined material for automotive sensors. BEI Sensors and Systems Co., Campbell, Calif., micromachines quartz to produce an automotive gyroscope for General Motors' vehicles *(Fig. 2)*. The gyroscope employs the Coriolis effect, where a rotational motion about the sensor's longitudinal axis produces a voltage proportional to the rate of rotation. The sensor replaces the traditional spinning-wheel gyroscope which consumes a lot of power, is heavy, and has an operating lifetime of only a few thousand hours.

Analog Devices sees a number of other applications on the horizon for MEMS, besides automotive. These include low-g accelerometers for video pinball machines (to check for tilt), for virtual reality systems, and for the global-positioning satellite (GPS) market. It also sees vibrating-accelerometer applications in gyroscopes. The consumer white goods sector (household appliances) also is considered a promising one. The company has an ongoing codevelopment program with Northeastern University, Boston, Mass., for micromachined switches and relays.

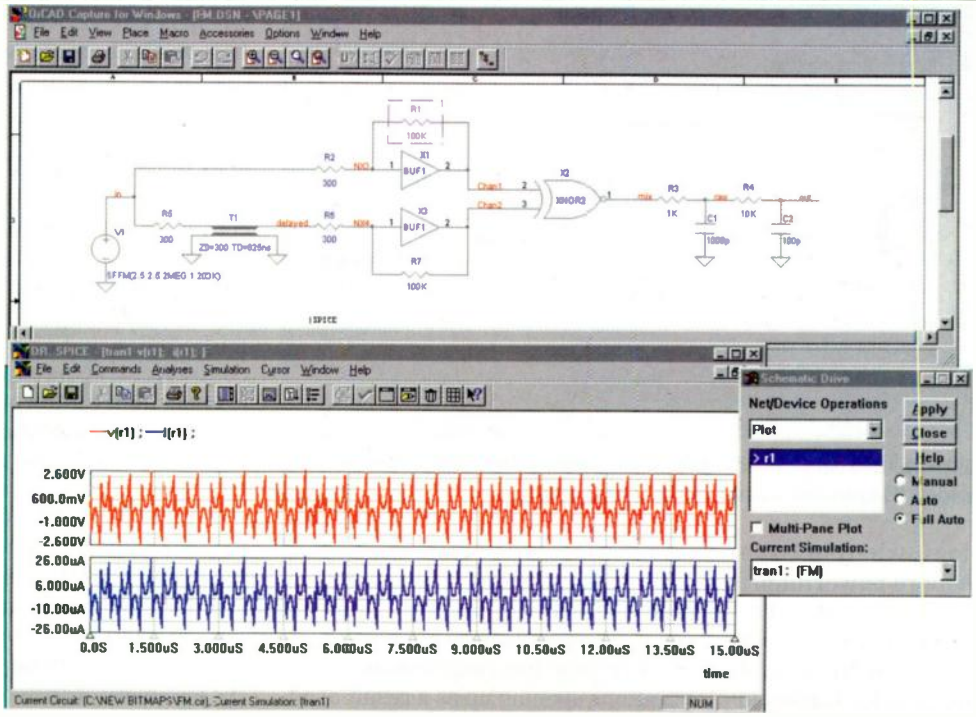
Another company commercializing MEMS devices using surface micromachining technology is Silicon Microstructures, Fremont, Calif., a wholly-owned subsidiary of Exar Corp. Late last year, it introduced an ultralow pressure sensor that can measure 0 to 0.15 psi full scale, and is priced between $1.00 and $2.00. The joining of forces by Silicon Microstructures and Exar is an example of a maturing

TABLE 1: MEMS PRODUCTS OPPORTUNITY LEVELS

Opportunity Level	Activity	Example	Result of success
1	Retrofit existing products at lower cost.	Lower-cost accelerometer.	• Reduce unit cost. • Increase profitability. • Provide market-sector entry.
2	Retrofit with performance enhancement.	Smart diaphragm gauge.	• Improve competitive position. • Increase revenue in an existing industry sector (automotive).
3	New application level I.	Automotive tire-pressure monitoring system.	Growth in a market subsector (within automotive).
4	New application level II.	Personal navigation system.	Creates a new market sector (personal navigation systems).
5	New application level IIII.	Microairplane with significant range and payload.	Probably would create a new industry.

From "Why Companies choose to use, or not use, MEMs technology," by Willliam N. Carr, NJIT, Newark, N.J. Presented at the "Commercialization of MEMS '96" Conference, Kona, Hawaii, Oct. 6-11, 1996.

Ten Important Reasons You Should Be Using Dr. Spice® 2000 A/D



1. Speed
Dr. Spice is fast - 2 times faster than other Spice simulators on average and up to 10 times faster on large or difficult circuits.

2. Ease of Use
Dr. Spice 2000 A/D is extremely easy to use for both beginners and experts. You can access all features by menus and dialog boxes. Every dialog box provides immediate access to extensive online help.

3. Superior convergence
In a test using the industry standard MCNC benchmark suite, Dr. Spice 2000 A/D ran over 93% of the circuits; the other leading brands ran just 87% and 62%, respectively.

4. Fast Built-in Mixed A/D
Dr. Spice 2000 A/D simulates even tightly-coupled mixed-signal designs. Its fast built-in mixed signal engine uses compiled C models for maximum performance. Primitives include gates, flip-flops, latches, state machines, comparators, decoders, multiplexers, adders, and RAM.

5. Schematic Driven Simulation
Dr. Spice links tightly with OrCAD, ProTel, and VIEWlogic. Select a net, component, or pin in your schematic and Dr. Spice plots its waveforms. By simply clicking on a component, you can also display its model parameters, operating point information, or run a parameter sweep. You can run simulations, set up stimulus, create plot windows or back annotate results onto your schematic, all from Capture menu items.

6. Non-Linear Magnetics for Power Supplies
Attention Power supply designers: Dr. Spice 2000 A/D provides the Chan non-linear magnetics model. This model is accurate, fast, and uses model parameters which come directly from the magnetics' data sheets. The Dr. Spice 2000 A/D model library includes over 2500 Chan magnetics models.

7. Library Support
Dr. Spice 2000 A/D has the largest library available, with over 20,000 parts, including virtually all manufacturers' libraries.

8. Automatically Generate Spice Models
Dr. Spice ModelMaker creates models of parts from data sheet parameters. Enter points graphically and ModelMaker automatically generates accurate SPICE models.

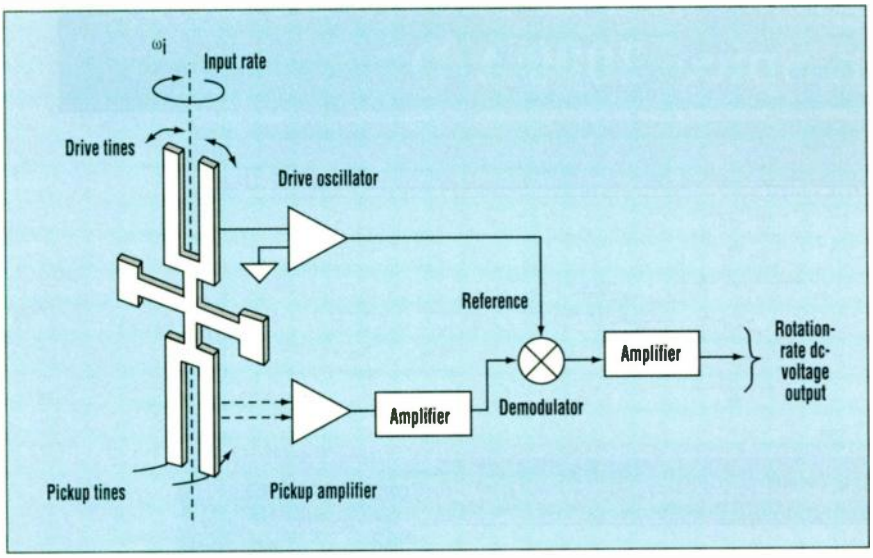
9. Automatically Calculate Power Dissipation
Dr. Spice automatically calculates the power dissipation of every device. You can also specify a maximum instantaneous power limit for any device in the circuit. If the device exceeds this power rating, an "alarm" occurs.

10. Parameter Sweeping
Sweep (or step) analysis allows you to examine the effects of varying sources, device or model specifications, temperature, or user-defined parameters.

Deutsch® Research

Deutsch Research 700 E. El Camino Real
Suite 130, Mountain View, California 94040
1-800-20 SPICE info@deutsch.com
www.deutsch.com

READER SERVICE 229



2. This gyroscope micromachined out of quartz by BEI Sensors and Systems resides in many General Motors' vehicles. Its operation is based on the Coriolis effect.

MEMS technology, wherein larger companies with more powerful processing resources (like Exar) purchase innovators in silicon micromachining technology (like Silicon Microstructures). That trend includes Lucas purchasing NovaSensor, EG&G purchasing IC Sensors, Microflow being acquired by I/O Sensors, a Japanese company purchasing Microsensor Technology, and BTI buying Sensym.

Disposable blood pressure sensors made by such companies as Lucas NovaSensor, Fremont, Calif., and EG&G's IC Sensors,Milpitas, Calif., have spearheaded the entry of MEMS devices into the biomedical field. A host of other applications for implantable biomedical MEMS devices including chemical sensors are on the horizon.

There also are many consumer applications opening up as a result of advances in silicon micromachined devices. One example is an "upscale" high-accuracy and long-life bathroom weighing scale made possible by an advanced pressure-sensor design from Measurement Specialties Inc., Fairfield, N.J. The scale is made up a nonbreakable and thick clear-glass platform with an LCD readout bonded to the bottom of it. The platform sits atop four load cells, one in each corner. The company also has penetrated the consumer market with inexpensive keychain tire-pressure sensors, complete with an LCD and a lifetime battery cell. Last year, the company made an important contribution to industrial pressure sensors with an all-media-compatible sensor, the MSP-300 series, at an OEM cost low enough that the company claims "it is virtually unmatched." According to Joe Mallon, MSI's president, a cofounder of NovaSensor, and a silicon micromachining pioneer, "the key was our revisiting an old technology of microfusion and combining it with a cost-effective package design and keeping tight control over labor costs."

An exciting potential market for optoelectronic ICs and micromachined structures is in communications. Micromechanical structures are useful here as fiber-optic aligners and reflective modulators for the implementation of residential "on-demand" movies. In fact, researchers at Bell Laboratories, Holmdel, N.J., already demonstrated the feasibility of an inexpensive moderate-performance micromachined modulator for use in fiber-to-the-home telecommunications systems. They fabricated a mechanical anti-reflection switch (MARS) that can be used in a wave-division-multiplexed (WDM) passive optical network *(Fig. 3)*.

Several MEMS experts interviewed for this report felt that the optoelectronic IC field is a potentially huge one

TABLE 2: WORLDWIDE MICROSYSTEM TECHNOLOGY EFFORTS

Country	Number of research centers involved in MSTs	Number of companies involved in MSTs	National funding
France*	25 laboratories or universities.	About 100 companies are developing microsystems in the frame of the national microsystem program.	About $13 million per year from 1993 to 1994. $14 million for ASIC development.
Germany*	More than 100 laboratories, Fraunhofers, universities.	More than 160 companies are developing microsystems in the frame of the national microsystems programs.	$66 million per year from 1994 to 1999(ASIC development included).
Switzerland*	15 federal schools and universities.	More than 100 companies will develop microsystems in the frame of the MINAST program.	$16 million per year from 1996 to 2000.
United Kingdom*	About 20 laboratories.	About 20 companies.	No specific funding.
Netherlands*	3 universities.	5 to 6 companies.	No specific funding.
United States*	More than 25 laboratories (national ones included).	Difficult estimation; certainly more than 100 companies (small- and medium-size entities and microelectronic companies).	$20 million per year from 1994 to 1997 (DARPA).
Korea	About 10 laboratories.	About 15 companies.	$5 million in 1995, $7.5 million in 1996, and $15 million forecast in 1997.
Japan*	13 institutes.	More than 30 companies (members of the Micro Machine Center).	$25 million per year (25 billion Yen in 10 years).

*Major activity. From "Microtechnologies, microsystems: Industrial applications and analysis of the U.S., Japanese, and European situation," presented by Jean-Christophe Eloy of CEA/Technologies Avencés, Grenoble, France, at the "Commercialization of MEMS '96" Conference, Kona, Hawaii. Oct. 6-11, 1996.

This Wallet May Not Exist Yet, But The Microprocessor For It Does.

To see the future of personal access to information, communication and entertainment, just check your hip pocket. Or look on your wrist. Or in your glasses.

Because that's where the electronics revolution is headed. Off the desktop and out into the world at large.

It's a journey that requires an entirely new microprocessor technology. One that does far more with far less in terms of power consumption, space requirements and cost.

Enter the Hitachi SuperH™ Series, a revolutionary RISC-based microprocessor that packs maximum functionality into minimum space. All while providing the low power and optimal price:performance required by portable, handheld products.

Not surprisingly, the SH leads the world in RISC processor shipments. Just one more example of Hitachi's commitment to research & development, an effort that's worldwide in scope. All part of our vision to make technology that fits the way you live.

www.hitachi.com

HITACHI

A TOTALLY NEW VISION

for MEMS devices acting as fiber aligners and connectors, switches, filters, and displays, as well as for printing applications. Texas Instruments, Dallas, which spent several years developing its digital micromirror device (DMD) technology using micromachining techniques, is now beginning to cash in on its advantages for displays and modulators in a broad range of applications. The company is developing a DMD system consisting of millions of individually controlled silicon micromirrors, each 17 μm on a side, that could be used for flat-panel high-resolution displays.

Data Storage On The Horizon

Data storage is another potentially large application for micromachined structures. An industry consortium initiated by the Universities of California at Berkeley and Los Angeles is developing a high-accuracy MEMS positioner for magnetic disk read/write heads. The positioner will allow for 0.1-μm servometer positioning accuracy and 100-Gbit/in.^{2} data densities.

IBM has developed a plastic-disk read/write-head technology where microdimples are created by a MEMS tip during the write operation. The read operation is similar to a record player reading of dimples. Densities of 20 Gbits/in.^{2} have been demonstrated and densities of 80 Gbits/in.^{2} are targeted.

An interesting MEMS application is in micronozzles for spray systems. Although silicon micromachined structures have made a quantum advance in ink-jet printers (one of the earliest efforts to develop micromachined nozzles for ink-jet printers was undertaken by Kurt Petersen, then of IBM Research Laboratories, San Jose, Calif.), it wasn't until SprayChip Systems Corp., Lanham, Md., brought its experience in atomizer concepts to bear on a microscopic scale that spray systems were revolutionized. The company micromachines a silicon chip with an array of very small microscopic-scale nozzles to produce a family of "designer sprayers" for automotive fuel injectors, medical nebulizers and inhalers, fire suppressors, biomedical cell sorters, and pharmaceutical paint-pigment and food-product powder production *(Fig. 4)*. A nozzle diameter of about 10 μm can have an array of spray holes with 25-μm center-to-center spacings.

Kurt Petersen, president of Cepheid, San Jose, Calif., a cofounder of NovaSensor, Fremont, Calif., and a silicon micromachining pioneer, sees a new market for MEMS in "micro instrumentation." Such instruments will not only serve medical applications, but also chemical, industrial, scientific, environmental, and geothermal applications as well. He sees a new class of micromachining-based microinstruments emerging for liquid and gas chromatography, flow cytometry, optical and mass spectroscopy, electrophoresis, polymerase-chain-reaction (PCR) and immuno assays, and for measuring water and soil contaminants.

Which Process Is Best?

Before the development of Analog Devices' surface-micromachined accelerometer two years ago, most MEMS devices were bulk micromachined, wherein material is removed from the silicon wafer through wet or dry etching. Surface micromachining, on the other hand, instead of penetrating the wafer, adds and removes various materials from the wafer. This technique is more compatible with standard processes for making analog and digital ICs and can yield smaller-size devices. It suffers, however, from the fact that it is essentially two-dimensional, a limitation for some applications.

A critical problem with surface micromachined devices is stiction (the sticking of a mechanically released part, such as a cantilever beam, to another surface). This reduces process yields. In general, the larger the MEMS device's aspect ratio (the ratio of the micromachining depth to the

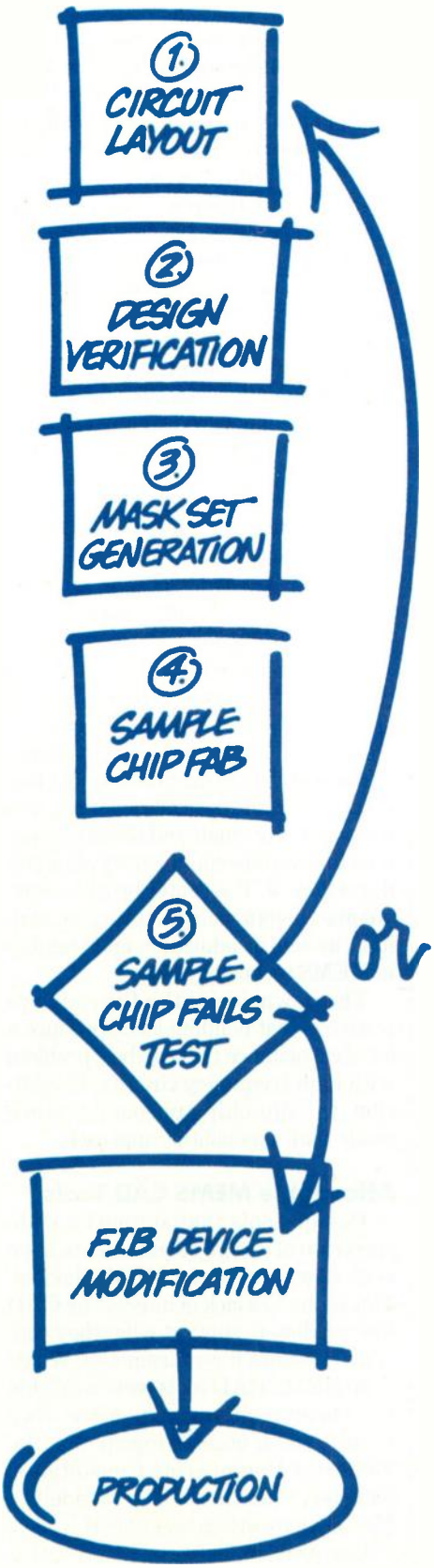
Needed: A Greater U.S. Commercial-Funding Effort

Over the last few years, the U.S. Government has boosted MEMS funding levels to over $20 million a year, up from $2 to $3 billion a year. DARPA also has active funding in MEMS dual-use development programs with millions of dollars for both the military and commercial sectors. But these are paltry sums compared with funding from other countries. Germany, for example, invests some $70 million a year in a variety of MEMS projects. Japan's Ministry of International Trade and Industry (MITI) funds the 10-year Micromachine Program with over $200 million a year.

Moreover, unlike the U.S., much of the funding by other countries is provided to industry. In the U.S., national laboratories like Sandia National Laboratories, Lawrence Livermore Laboratories, and the Jet Propulsion Laboratories, as well as university research facilities, are regularly provided much larger funding sums than private industry. These laboratories continuously develop notable advances in MEMS technology, but little of this translates into "practical" products in the commercial sector. As a result, the U.S. is constantly behind other countries in applying products based on leading-edge technologies like MEMS.

The automotive sector is a good example. In the last few years, automotive air-bag systems based on MEMS accelerators have been making driving in the U.S. safer. Micromachined sensors also are making for "smarter" vehicles. However, Europe and Japan have been applying MEMS technology to automobiles long before us, fostered in part by national and local government funding. The same can be said in the telecommunications sector.

What this all boils down to is that the U.S. has many great ideas when it comes to MEMS technologies, but little of that results in "down to earth" practical commercial applications. There are many in industry who are wary of government help, and some of the concerns they raise are legitimate. However, when viewed in an international context (and we are part of a global international economy) many of these concerns are secondary. Perhaps it's time for national, state and local governments to take stock of MEMS technology and provide the funding that will foster small- and large-company innovations. That will in turn create more commercial-market opportunities for MEMS technology.



To modify an IC, you can spend weeks going back to square one.

Or only hours going through a Micrion FIB system

An IC Modified By Focused Ion Beam Technology.

Until recently, if you wanted to modify an IC prototype, you had to go back to the circuit layout—and spend weeks redesigning, remasking and refabricating.

But now you can have a revised, fully functioning prototype in a matter of hours. All you need is a Focused Ion Beam system from Micrion. Like the market-leading Micrion 9000. It lets you perform microsurgery on your IC quickly and easily. It also gives you high resolution imaging for a better view of the device features, unparalleled system stability for more accurate machining, and our patented charge neutralization technology to prevent electrostatic discharge (ESD) damage.

So next time you need to rewire a prototype, don't go back to the drawing board. Go to your phone and call Micrion at 508-531-6464.

We'll save you some expensive, time-consuming steps. So you can get those new designs to market faster.

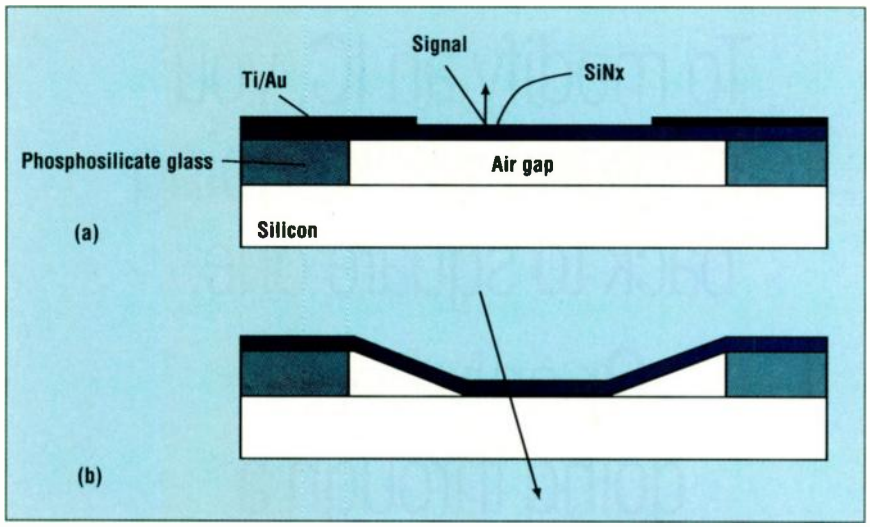
The Micrion 9000 Focused Ion Beam System.

Micrion

Where the future is in focus.

Micrion Corp., One Corporation Way, Centennial Park, Peabody, MA 01960-7990

READER SERVICE 128



3. Operating principle of the micromechanical anti-reflection switch (MARS), a micromachined modulator for fiber-to-the-home applications, was developed by Bell Laboratories. In one state, the membrane is suspended above an air gap, resulting in the light beam being reflected at a high rate (a). In the other state, the membrane is in contact with the substrate, resulting in an anti-reflection condition (b).

width), the less of a problem stiction poses. Thus, bulk micromachined devices, which have higher aspect ratios than surface micromachined ICs, have less of a stiction problem, and HARM (high-aspect-ratio MEMS) devices have the fewest stiction problems. HARM devices are generally micromachined using electron-beam sources, lasers, deep X-rays (the Germans use the acronym LIGA for this technique), and ultraviolet rays.

Another problem with surface micromachined devices is that they usually require thicker films to be deposited for the necessary mechanical behavior of the silicon. The thicker layers are a challenge for the reactive-ion etching (RIE) that is being used in bulk micromachined devices.

Nevertheless, many experts agree that surface micromachining technology holds the promise of higher levels of on-chip integration, with the sensing and/or actuation element residing on the same chip with signal-conditioning, control, and interface electronics, once these challenges are solved.

Janusz Bryzek, president of Intelligent Micro Sensor Technology, Fremont, Calif., and cofounder of NovaSensor, points out, "There are three major factors that make silicon micromachining technology attractive for the MEMS industry. Surprisingly to many, the potential of integrating an electronic circuit together with a sensor so far *was not* one of them."

The three factors Bryzek is referring to are silicon's excellent mechanical properties, its batch manufacturability, and an available IC industry infrastructure. To support his argument that on-chip integration has so far eluded the MEMS industry, he points out that only 8% of the largest MEMS market, pressure sensors, includes on-chip integrated signal conditioning. And only 12% of all micromachined accelerometers have on-chip integrated signal conditioning.

It's therefore not surprising that many makers of MEMS devices make use of hybrid approaches with separate signal-conditioning chips designed exclusively for that purpose. Companies such as MCA Technologies, Santa Clara, Calif., specialize in producing mixed-signal ASICs designed specifically for MEMS sensors and actuators.

However, a development out of Sandia National Laboratories, Albuquerque, N.M., may point to a solution of the integration problem. Researchers there developed a process that allows the monolithic integration of both micromechanical and CMOS devices on the same substrate *(Fig. 5)*. Sandia is presently negotiating with several major semiconductor IC vendors to license this technology. Sandia is also working with researchers at the University of California at Berkeley to minimize the stiction problem for the process it developed, for the case of MEMS devices with high aspect ratios.

Karen Markus, director of the MEMS Technology Applications Center at MCNC, Research Triangle Park, N.C., points out that "there's really no one process technology that's best." Like everything else in engineering, it's a matter of trade-offs *(Table 4)*. She advocates, at least for now, a flip-chip bonding approach developed at MCNC where two die, one containing the sensor/actuator and the other containing the signal-conditioning electronics, are solder-bumped together. She elaborates, "given that MEMS continues to evolve, the likelihood is that you'll want to change your MEMS design, and thus the flip-chip approach is probably the best one for the majority of applications which are presently small- and medium-volume ones." These applications include product designs with features that are constantly changing and with short life spans.

MCNC's MEMS Technology Applications Center serves as a focal point in the transition of MEMS technology from the research and concept stages to commercial applications. Acting as a manager of intellectual property, it is accessible by small and large companies for engineering prototyping and development. The center provides low-volume custom manufacturing capabilities, as well as education and training in MEMS technology.

The downside of the flip-chip approach is that bonding leads produce a lot of capacitance that can be a problem with high-frequency circuits. In addition, the flip-chip approach is more costly than a monolithic approach.

Affordable MEMS CAD Tools

Design tools that support a wide spectrum of design requirements have been slow to arrive for MEMS devices. This is due to a lack of interest by CAD tool vendors to support what they consider specialized requirements. Whatever MEMS CAD tools were available have been relatively expensive. As a result, small consulting firms, like Tesseract Engineering Consultants, San Jose, Calif., headed by Wendell E. McCully, have arisen to service this need.

One problem has been a perception by design-tool vendors that MEMS technology is similar to conventional IC technology. While there are many sim-

Give Your Scope State of the Art Differential Measurement Capability.

The **Model 1855** is a stand-alone 100 MHz differential amplifier designed to function as a signal conditioning preamplifier for your oscilloscope, digitizer or spectrum analyzer. The Amplifier's Gain, CMRR, Overdrive Recovery and Common Mode Range capabilities combine to allow direct measurement of such diverse signals as individual D/A LSB's or a switching supply's upper gate drive. Tiny aberrations in large signals can be viewed using the Differential Offset Generator which can extend the oscilloscope's display range to over ±150,000 divisions. The **Model 1855** is shown with the Preamble Instruments switchable **XC100** 10X/100X Differential Probes.

Measure Directly (in circuit):

- ❑ D/A Settling Time
- ❑ Power Transistor Saturation Characteristics
- ❑ Snubber Diode Turn-on Characteristics
- ❑ Small Ripple Riding on Large DC Voltages
- ❑ Small Signals in Noisy Applications
- ❑ Non-ground Referenced Control Logic Signals
- ❑ Floating Signals, Safely
- ❑ Differential Communication Signals

Amplifier Characteristics:

- ❑ 100 MHz Bandwidth
- ❑ Very Fast Recovery From Overdrive
- ❑ 100 μVolt Resolution Comparison Voltage Generator
- ❑ Common Mode Range up to the Probe's Maximum Rating
- ❑ 100,000 to 1 CMRR
- ❑ High Rejection of Fast dv/dt Common Mode Signals
- ❑ 1 Meg / 100 Meg Input Resistance
- ❑ 0.1% True Differential Offset
- ❑ High System Sensitivity (X10 Gain)

PREAMBLE INSTRUMENTS

Preamble Instruments, Inc
P.O.Box 6118
Beaverton, OR 97007-0118
(503) 646-2410, 800-376-7007
FAX: (503) 646-1604

INTERNATIONAL DISTRIBUTORS: AUSTRIA: Elsinco GmbH (43) 1-815-04-00; *BELGIUM:* Optilas B.V. (31) 172-43-12-34; *BULGARIA:* Elsinco h.e. Strelbishte (359) 2-58-61-31, *CZECH REPUBLIC:* Elsinco Praha spol. s r.o. (42) 2-49-66-89; *FRANCE:* Francaise d'Instrumentation (33) 25-71-25-83; *HUNGARY:* Elsinco KFT (36) 1-269-18-50; *ISRAEL:* Dan-El Technologies, Ltd. (972) 03-647-8770 *JAPAN:* TOYO Corporation, (81) 3-5668-6800; *KOREA:* Myoung Corporation, (82) 2-784-9942; *LUXEMBOURG:* Optilas B.V. (31) 172-43-12-34; *NETHERLANDS:* (31) 172-43-12-34; *POLAND:* Elsinco Polska Sp. zo.o (48) 22-39-69-79; *SLOVAKIA:* Elsinco Bratislava spol. s r.o. (42) 7-784-165; *TAIWAN:* Cha Wei Electric Trading Co, Ltd, (886) 2-561-2211, *UNITED KINGDOM:* TTI (44) (01480) 412451

READER SERVICE 159

ilarities between the two, MEMS devices are really a subset of conventional ICs, and as such should be considered custom devices. MEMS devices often require unique substrates. They need odd-orientation crystals and wafers, double-sided polished wafers with various diameters, thin, and ultra-thin substrate thicknesses, and bonded-wafer substrates as well.

Things are beginning to change for the better, however, with the realization by some CAD tool vendors that MEMS technology is on the verge of becoming a major enabler for large markets. Companies like Microcosm Technologies, Cary, N.C., and Tanner Research, Pasadena, Calif., are now providing high-level MEMS design tools, some of which can run on PC platforms, at affordable prices. A number of universities like the Massachusetts Institute of Technology (MIT), Cambridge, Mass., with their MEMCAD tools, and the University of Michigan in Ann Arbor with their CAEMEMS and Mystic tools, are also offering help. The multiuser MEMS Processes (MUMPS) of MCNC is designed to provide low-cost access to MEMS design tools. MCNC also makes available SmartMUMPS for integrated MEMS devices and LIGAMUMPS for high-aspect-ratio MEMS devices. All these tools are available over MCNC's TechNet via the World Wide Web.

Microcosm is a leader in MEMS software tools, devoting all of its efforts exclusively to CAD tools for MEMS. Headed by its chief technical officer Dr. John Gilbert, a renowned expert in MEMS modeling and simulation, it offers the MEMCAD suite of design tools *(Fig. 6)*. Its MEMCAD 3.1 is an integrated suite of design, visualization and analysis software tools architected to make possible complex MEMS devices. The environment combines the best industry and proprietary analytical software to offer solutions for multidomain problems such as electrostatics, mechanical, coupled mechanical, optical, and magnetostatics. Collobrative developments are underway to add mi-

TABLE 4: RELATIVE PROS AND CONS OF THREE PROCESSES FOR MICROMACHINED DEVICES

Process	Performance	Size	Yield	Cost	Simplicity
Hybrid	–	–	+	+	+
Monolithic	+	+	+/–	+/–	—
Flip chip	+	+/–	+	+	+

From "The Challenges of infrastructure: Supporting the growth of MEMS into production," Karen W. Markus, Director, MEMS Technology Applications Center, MCNC, Research Triangle Park, N.C. Presented at the "Commercialization of MEMS '96" Conference, Kona, Hawaii, Oct. 6-11, 1996.

TABLE 3: TECHNOLOGIES ON OFFERS IN EUROPRACTICE

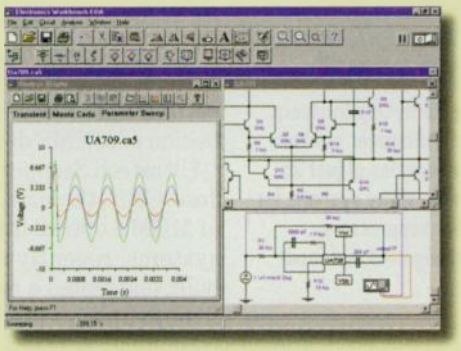
PARTNER / TECHNOLOGY	Manufacturing Cluster 1 Bosch, HL Planar, Fraunhofer Institute FhgISIT, GMA, Fraunhofer Institute FhgIMS, Microparts	Manufacturing Cluster 2 Sagem, Sextant, LAAS CNRS, CEA-LETI	Manufacturing Cluster 3 GEC Marconi Materials Technology, Rutherford Appleton Laboratory, CRL, TWI, Epigem	Manufacturing Cluster 4 CSEM, Twente Microproducts, Holland Signaal
Surface micromachining silicon	•	•	•	•
Bulk micromachining silicon	•	•	•	•
Micromachining on quartz		•	•	•
Laser trimming/ablation/drilling	•		•	•
Electroforming	•		•	•
LIGA	•		•	
Excimer laser			•	
Micromolding	•		•	
Electroplating	•		•	•
Polymer materials	•		•	
GaAs components			•	
ASIC design	•	•	•	•
Silicon on insulator		•	•	
Chip and wire assembly	•	•	•	•
Fllip chip solder bump	•		•	•
Multichip module	•		•	•
Anodic bonding/silicon bonding	•		•	•
Biosensitive layers	•		•	•
Magnetic layers	•		•	•
Piezoresistive layers		•	•	

From "MST markets and products in Europe," presented by Dr. Guido Tsculena at "The Commercialization of MEMS '96" Conference, Kona, Hawaii, Oct. 6-11, 1996. Table was originally part of an article entitled "Microsystems in the 4th Framework Programme" by Dirk Beernaert and J. Malcolm Wilkinson, Technology for Industry Ltd., Wilburton, Cambridgeshire, England.

NEW! Electronics Workbench EDA with analog, digital and mixed A/D SPICE simulation, a full suite of analyses and over 8,000 devices. Absolutely the easiest interface to learn and use. And priced for today's expense account, not next year's budget.

You'll be working productively in 20 minutes, and creating better designs faster. We guarantee it.

$995 ← GREAT PRICE!



High-End Features

MIXED ANALOG/DIGITAL	YES, INTERACTIVE
ANALOG ENGINE	SPICE 3F5, 32-BIT
DIGITAL ENGINE	NATIVE, 32-BIT
VIRTUAL INSTRUMENTS	YES
ON-SCREEN GRAPHS	YES
ANALOG COMPONENTS	OVER 100
DIGITAL COMPONENTS	OVER 200
DEVICE MODELS	OVER 8,000
TEMPERATURE CONTROL	EACH DEVICE
MONEY-BACK GUARANTEE	30-DAY
TECHNICAL SUPPORT	FREE

Powerful Analyses

DC OPERATING POINT	YES
AC FREQUENCY	YES
TRANSIENT	YES
FOURIER	YES
NOISE	YES
DISTORTION	YES
PARAMETER SWEEP	YES
TEMPERATURE SWEEP	YES
POLE ZERO	YES
TRANSFER FUNCTION	YES
DC SENSITIVITY	YES
AC SENSITIVITY	YES
WORST CASE	YES
MONTE CARLO	YES

30-DAY MONEY-BACK GUARANTEE
VERSION 5.0 FOR WINDOWS 95/NT/3.1.

FEATURES OF ELECTRONICS WORKBENCH EDA

GENERAL

Integrated Suite: Fully integrated schematic editing, SPICE simulation and waveform generation and analysis. Supports modifications to the circuit during simulation. Circuit analyses through virtual test instruments or 14 analyses listed below.

Simulation Engine: Interactive 32-bit SPICE 3F5, enhanced with native-mode digital and mixed analog/digital support. Automatic insertion of signal translation interface. Supports multiple reuse of hierarchical blocks. GMIN stepping for better convergence. No preset limits on circuit size or complexity.

Schematic Capture: Click-and-drag interface. Hierarchical workspace, automatic wire routing with manual adjustment, automatic reference designation. No preset limit on schematic size.

Analysis: Virtual test instruments for quick and simple analysis. Fourteen analyses for on-screen graphs and more flexible analysis (described below).

Design Encapsulation: All design information, including SPICE parameters, setup and models stored in the design file to simplify design sharing and reuse. Imports and exports standard SPICE netlists for use with other simulators or to implement designs. Imports manufacturers' SPICE models into reusable Electronics Workbench components. Exports to standard PCB layout packages such as OrCAD, Protel and Tango.

ANALYSES

DC Operating Point: Calculates DC operating point and reports voltage at each node.

Transient: Circuit voltages and currents over time at any number of nodes. Specify start and stop times.

AC Frequency Sweep: Small-signal gain and phase over range of AC frequencies at any number of nodes. Specify range type (decade, octave or linear) and resolution (number of steps) of frequency sweep.

Fourier: Magnitude and phase of DC and Fourier spectral components of transient response. Specify fundamental frequency and an unlimited number of harmonics.

Noise: Resistor and semiconductor noise contribution reported as RMS sum. Specify device of interest, output and reference nodes, and range type and resolution of frequency sweep.

Distortion: Small-signal steady-state harmonic and intermodulation products over a range of frequencies. Specify any number of nodes and sweep range type and resolution. Optionally exclude devices on an individual basis.

Parameter Sweep: DC, AC or transient behavior over a range of parameter values. Specify device and parameter to vary, and range type and resolution of sweep.

Temperature Sweep: DC, AC or transient response over a range of temperatures. Specify range type and resolution of sweep.

Pole Zero: Calculates poles and zeros of circuit's transfer function. Specify input and output nodes.

Transfer Function: Calculates small-signal gain, input resistance and output resistance. Specify output node and input source.

DC Sensitivity: Sensitivity of DC voltages or currents to changes in a specific device. Specify device and parameter of interest.

AC Sensitivity: Sensitivity of AC voltages or currents to changes in a specific device. Specify device and parameter of interest and range type and resolution of frequency sweep.

Worst Case: Maximal variance in DC, AC or transient response when all devices are varied within their tolerance. Specify definition of "worst" as maximum, minimum or maximum swing or falling value.

Monte Carlo: DC, AC or transient response when parameters are randomly varied within a tolerance. Specify number of runs, tolerance and uniform or Gaussian distribution.

VIRTUAL TEST INSTRUMENTS

Digital Multimeter: Autoranging multimeter measures AC and DC current, voltage, resistance and decibel loss.

Function Generator: Produces square, triangular and sinusoidal waves, from 1 Hz to 999 MHz. Adjustable duty cycle, amplitude and DC offset.

Oscilloscope: Dual-trace scope, time base range from seconds to nanoseconds. Internal or external triggering, positive or negative edge. Scrolling through time. Two digital cursors. Save data to ASCII file.

Bode Plotter: Plots magnitude and phase for a frequency sweep. Supports frequencies from mHz to GHz. Log or linear scales.

Word Generator: Acts as a digital stimulus editor to drive a circuit with up to 32K 16-bit words. Display and edit data as ASCII, binary or hex. Load, save, cut and paste words. Supports breakpoints and single step, burst and continuous modes. External trigger and data ready indicator for synchronization.

Logic Analyzer: Supports pre- and post-trigger. Internal or external clock, negative or positive edge. Clock qualifier to synchronize data. User-defined trigger patterns and trigger qualifier.

Logic Converter: Converts among gate, truth table and Boolean logic representations.

COMPONENTS

Sources: DC Voltage, DC Current, AC Voltage, AC Current, Voltage-Controlled Voltage, Voltage-Controlled Current, Current-Controlled Voltage, Current-Controlled Current, AM, FM, VHF, Clock, Pulse-Width Modulated, Frequency-Shift Keying, Polynomial, Piece-Wise Linear, Controlled Voltage, Controlled Oscillator and Nonlinear Dependent.

Basic: Resistor, Capacitor, Inductor, Transformer, Relay, Switch, Time-Delay Switch, Voltage-Controlled Switch, Current-Controlled Switch, Pull-Up Resistor, Variable Resistor, Resistor Pack, Polarized Capacitor, Variable Capacitor, Variable Inductor, Coupled Inductor and Nonlinear Transformer.

Diodes: Diode, Zener Diode, LED, Schottky Diode, Diac, SCR, Triac and Full-Wave Bridge Rectifier.

Transistors: NPN and PNP BJTs, N- and P-Channel JFETs, 3- and 4-Terminal Enhancement and Depletion N- and P-Channel MOSFETs.

Analog ICs: 3- and 5-Terminal Opamps, Comparator and Voltage Regulator.

Mixed ICs: A-to-D Converter, D-to-A Voltage and Current Converters, 555 Timer and Monostable.

Logic Gates: AND, OR, NOT, NOR, NAND, XOR, XNOR, Tristate Buffer, Buffer and Schmitt Trigger.

Digital: RS, JK, T, D and D Flip-Flops, Half and Full Adders, Multiplexer, Demultiplexer, Encoder and Decoder.

Indicators: Bulb, Voltmeter, Ammeter, Probe, Blow and Decoded 7-Segment Display, Buzzer and Raw and Decoded Bargraph.

Controls: Differentiator, Integrator, Gain Block, Transfer Function, Limiter, Multiplier, Divider and Summer.

Other: Fuse, Lossy and Lossless Transmission Lines, Crystal, DC motor, Vacuum Tube and Buck and Boost Converter.

74xx ICs: 7400, 7402, 7404, 7405, 7406, 7407, 7408, 7409, 7410, 7411, 7412, 7413, 7420, 7421, 7422, 7425, 7426, 7427, 7428, 7430, 7432, 7433, 7437, 7439, 7440, 7442, 7445, 7447, 7451, 7454, 7455, 7469, 7472, 7473, 7474, 7475, 7476, 7477, 7478, 7486, 7490, 7491, 7492, 7493.

74xxx ICs: 74107, 74109, 74112, 74113, 74114, 74121, 74123, 74125, 74126, 74132, 74133, 74134, 74138, 74139, 74145, 74147, 74148, 74150, 74151, 74153, 74154, 74156, 74157, 74158, 74159, 74160, 74161, 74162, 74163, 74164, 74165, 74166, 74169, 74173, 74174, 74175, 74181, 74190, 74191, 74192, 74194, 74195, 74198, 74199, 74238, 74240, 74241, 74244, 74251, 74253, 74257, 74258, 74273, 74280, 74290, 74293, 74298, 74350, 74352, 74353, 74365, 74367, 74368, 74373, 74374, 74375, 74377, 74378, 74379, 74390, 74395, 74445, 74465, 74466.

4xxx ICs: 4000, 4001, 4002, 4008, 4011, 4012, 4013, 4015, 4023, 4025, 4028, 4030, 4040, 4049, 4066, 4068, 4069, 4070, 4071, 4073, 4081, 4085, 4086, 4107, 4019, 4024, 4027, 4041, 4050, 4069, 4072, 4075, 4077, 4078, 4082, 4503, 4512, 4516, 40103.

MODELS

Digital: Models for ICs, Gates and Flip-Flops in HC totem-pole, HC buffer, HC open-drain, LS totem-pole, LS buffer, LS open-collector and LS open-collector buffer configurations.

Diodes: 2,700 models for Diodes, Zener Diodes, LEDs, Schottky Diodes and Diacs from Motorola, General Instruments, International Rectifier, Zetex and Philips.

Transistors: 2,600 models for NPN and PNP BJTs, JFETs, MOSFETs, SCRs, Triacs and IGBTs from Motorola, National Semiconductor, International Rectifier, Toshiba, Harris and Philips.

Analog ICs: 2,700 models for Opamps, Comparators and Voltage Regulators from Motorola, Texas Instruments, Maxim, Elantec, Analog Devices, Zetex, Burr-Brown and Linear Technology.

Other: Models for a variety of Relays, Transformers, Vacuum Tubes, Transmission Lines and Crystals.

FULL-FEATURED SPICE!

Electronics Workbench® EDA

CALL 800-263-5552

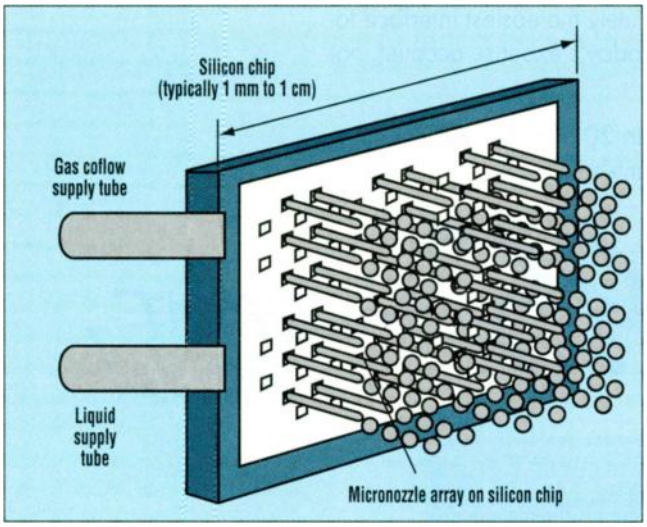
INTERACTIVE

INTERACTIVE IMAGE TECHNOLOGIES LTD., 908 Niagara Falls Boulevard, #068, North Tonawanda, New York 14120-2060/Telephone 416-977-5550

Fax: 416-977-1818 Internet: http://www.interactiv.com CompuServe:71333,3435/BBS:416-977-3540/E-mail:ewb@interactiv.com

crofluidic and macromodeling capabilities for system simulators. Microcosm has licensed core technology from MIT, where Dr. Gilbert was in charge of MIT's MEMCAD program. The company's collobrative efforts involve MIT, Carnegie-Mellon University, Pittsburgh, Pa., Stanford University, Stanford, Calif., the University of California, Berkeley, and the University of Pennsylvania, Philadelphia.

Tools like L-Edit Layout Editor from Tanner Research can run on PC, MAC and Unix machines to support polygons, arcs and curves. The company's tools support 2D layout design entry and 3D modeling generation and visualization, enhanced cross-section and visualization, all-angle design-rule checking, finite- and boundary-element multidomain analysis/results visualization, and behavioral-model creation. DARPA has funded Tanner with $5 million to develop design tools for commercialized MEMS devices. SOLIDIS is another useful CAD tool for MEMS. Developed at the Physical Electronics Laboratory of ETH, Zurich, Switzerland, it allows rapid and cost-effective optimizations of MEMS designs.



4. A micronozzle array on a silicon chip made by SprayChip Systems. The micronozzles can be closely spaced—a nozzle diameter of about 10mm yields a center-to-center spacing between nozzles of just 25 mm. These microscopic-scale nozzles make possible spray systems for fuel injectors, medical nebulizers and inhalers, fire suppressors, biomedical cell sorters, and pharmaceutical paint-pigment and food-product powder production.

Interface Efforts

Interfacing of MEMS devices to other electronic circuits is making impressive strides, particularly for industrial electronic applications. The International Electrotechnical Commission (IEC) has initiated a broad effort to create MEMS standards for sensor output signal formats and control-network communication protocols.

The IEEE also has proposed a draft standard for transducer-to-microprocessor interfacing, known as the IEEE-P1451.2 Draft Standard for Transducer to Microprocessor Communication Protocols and Transducer Electronic Data Sheets (TEDS) Formats. Released for balloting last August, it simplifies transducer connectivity to existing data networks.

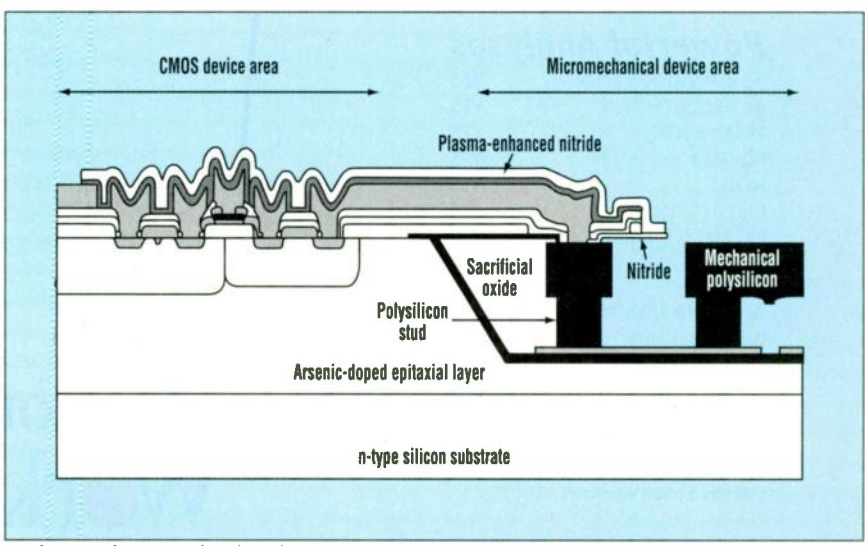
Process Tools Advance

MEMS devices would not have been able to reach their present status without the support of the right processing equipment. And equipment vendors have been paying attention to the growing MEMS market and are providing the needed advanced tools.

For example, MEMS devices often require rapid, nondestructive and accurate evaluation of the absolute and total thicknesses of unique substrates. With that in mind, Virginia Semiconductor, Fredricksburg, Va., developed a prototype optical micrometer capable of measuring a micromechanical silicon wafer's absolute thickness from 2 to 500 µm with 0.6-µm precision, and accuracy within 2.25 µm. Relative wafer total-thickness variation can be imaged over a 40-mm-diameter region with thickness resolution from 0.1 to 0.2 µm. Companies like GTE Equipment Technologies, Nashua, N.H., with its high-pressure supercritical CO_2 cleaner and KARL SUSS America Inc., Waterbury Center, Vt., with its wafer aligners, probes, bonders and coaters, are providing the impetus for greater commercialization of MEMS devices.

Ultratech Stepper Inc., San Jose, Calif., the leading vendor of MEMS optical lithography systems, recently designed, built, and tested a new optical lithography technology known as scanning array lens lithography (SALLY). SALLY is designed to project a large effective image field sized that spans the width of any substrate, thus allowing exposure in a single scan. The system has been optimized for a numerical aperture of 0.10, allowing large-aspect-ratio resist images to be achieved, an important development for HARM devices.

Presently, lithographic systems using ultraviolet-light exposures are ca-



5. This novel process developed at Sandia National Laboratories allows the monolithic integration of both micromechanical sensor/actuator mechanisms and CMOS electronics on the same silicon chip. The micromechanical devices are built in a trench. This trench is then refilled with oxide, planarized, and sealed to form the starting wafer for CMOS processing.

ONCE YOU'VE CREATED THE WORLD'S BEST BEERS,

FASTEST CARS AND STRANGEST

PANTS, WHAT DO YOU DO FOR AN ENCORE?

Introducing Integra Station™, the Windows-based PCB design solution from Mentor Graphics. German precision meets the ease of Windows.

In a country that's renowned for its quality, precision engineering and leather trousers, Integra Station is the undisputed market leader for designing PCBs on Windows 95 and Windows NT™ machines. Proven on 1,900 seats and counting, it's the board layout solution of choice when designers need unparalleled features, reliability and support, along with the ease and performance of the 32-bit Windows operating systems.

And now Mentor Graphics introduces Integra Station to the rest of the world.

Integra Station is the only product in its category to use a single database, ensuring that your layout matches your schematic every time. Variant technology lets you create hundreds of variations from a single design. You can also capture design data from schematics or layout as reuse modules, which can be stored as separate data elements for reuse in other designs.

Talk to your Mentor Graphics sales rep or call **1-800-547-3000,** dept. M814, for a free demo of Integra Station. You can also visit our web site at **www.mentorg.com**.

Soon you'll understand why Germans think it's the greatest thing since sliced *bratwurst*.

Mentor Graphics

THE POWER TO CREATE

READER SERVICE 127

pable of producing MEMS devices with aspect ratios from 3:1 to 5:1. Aspect ratios of 50:1 to 100:1 can be achieved with LIGA techniques like synchrotron exposure. However, depth-of-field focus problems need to be solved for such methods to be cost effective.

Testing Is A Challenge

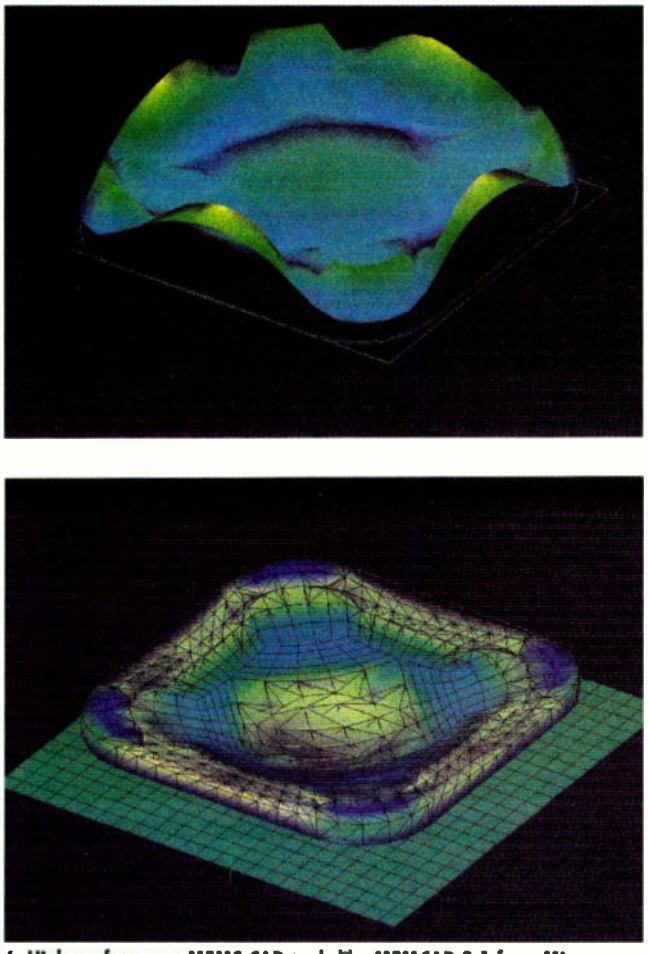
Testing MEMS devices is not an insignificant issue. Together with packaging, they constitute the largest part of the cost of producing a MEMS device. Not the least of the testing issues is a lack of standardized test methods and equipment. This is due to the fact that no two micromachined sensors are alike, even if they're functionally the same such as two pressure sensors. Most of the available test systems for MEMS devices are expensive and complex custom systems. Many are custom-built in-house systems.

There are no standard methods for testing, and for evaluating test results to the sensor's material properties. Nor are sensor-material mechanical properties adequately defined. The problem is compounded by the fact that functional testing of a sensor or actuator requires environmental control as well as the test electronics circuitry. Questions arise as to what needs to be tested and how? How do you define reliability levels and test for them? Reliability testing for conventional electronics circuits are inadequate for MEMS devices.

There's no basic set avaialable for parametric test structures for key MEMS process parameters. Methods for monitoring mechanical material properties like Young's modulus, poisson's ratio, fracture strength, etc., are still under development.

Most electronic circuits operate at either 3.3 or 5 V. Many MEMS devices, on the other hand, require higher operating voltages.

With such issues in mind, the integration approach using surface micromachining may look more favorable than other process techniques (testing one chip, for example, costs less than testing two or more chips in a flip-chip or hybrid approach).



6. High-performance MEMS CAD tools like MEMCAD 3.1 from Microcosm Technologies are making possible relatively inexpensive modeling and simulation of MEMS devices. Depicted above is the diaphragm of a pressure sensor displaying the slice-plane internal stress. Below is the same diaphragm displayed as a wire-mesh structure.

Packaging

Closely related to the testing challenge is packaging. According to many experts, packaging can represent up to 80% of a MEMS device's cost. Like testing, no two sensor packages are alike, although , companies like Motorola Semiconductor and others are trying to make inroads into developing standardized packages.

Packaging was a key consideration in the all-media-compatible pressure sensor Measurement Specialties produced for the industrial market at low cost, and mentioned earlier in this report.

Packaging of MEMS devices impacts system performance. Moisture creeping into a sealed package, for example, can create stiction and thus a failed sensor. Vacuum packaging is desirable for MEMS devices, but this may add to the cost. Moving parts within a MEMS device can experience vicious damping. The package itseif can affect a sensor's performance. For example, a PZT-based packaged sensor may already be sensing, even though no stimulus is present at its input, due to the strain on the device caused by the package. In developing the DMD mentioned earlier in this report, Texas Instruments had to tackle the large problem of how to get rid of the large amounts of heat generated within the DMD package caused by the light energy inside the device.

Some semiconductor vendors feel that for MEMS devices to achieve high-volume commercial applications, it is necessary that existing application-specific packages be standardized and thus packaging costs will be driven down. Thus far, only automotive, medical, and consumer white-goods sectors have been able to drive large-enough volume businesses to support customized packaging.

However, there are many small- to moderate-volume applications for MEMS devices in which the MEMS sensor/actuator is the enabling technology for a much larger market. Given this scenario, it may well be that large companies and organizations benefiting from MEMS devices in such sectors will collaborate with MEMS device manufacturers to solve the critical testing and packaging issues. It seems that the millions of dollars being spent on commercializing MEMS technology worldwide may produce testing and packaging solutions that are now confronting MEMS technology.

How Valuable	Circle
Highly	560
Moderately	561
Slightly	562

JUST LISTEN...

TOM BEAVER
Vice President
Worldwide Marketing
Motorola, Inc.

PHILIP WENNBLOM
Director, Strategic Planning
Mobile and Handheld Products Group
Intel Corporation

ROBIN SAXBY
President & CEO
Advanced RISC Machines
(ARM)

VAUGHN WATTS
Director of
Mobile Computing Architecture
Texas Instruments

. . . and you will hear four important industry leaders offer their views on the future of the portable industry.

One luncheon and you'll understand the importance of the designs you're now working on. Get a leg up on the trends and technology that will shape portable products in the twenty-first century. Attend the...

Portable by Design

CONFERENCE & EXHIBITION

MARCH 24-27, 1997

Keynote Luncheon • March 25, 1997

Santa Clara Convention Center, Santa Clara, Calif.

Contributing Sponsors: Benchmarq Microelectronics; Intel Corporation

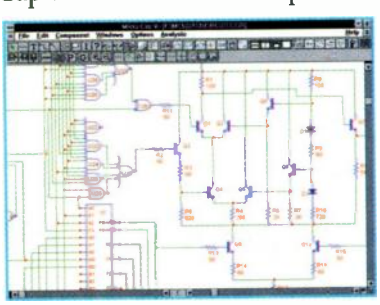
For Conference, Exhibition, or Luncheon information, call: 201/393-6075; fax: 201/393-6073

Micro-Cap V. Victory over the analog/digital simulation challenge.

The conflict's ended. And you're the winner—with this fifth generation of Micro-Cap, the industry's premier PC-based interactive CAE design tool. Incorporating a native digital simulator with PSpice®-compatible syntax, Windows-based Micro-Cap V™ seamlessly integrates analog/digital simulation and begins a whole new era.

Micro-Cap V gives you a sketch and simulate environment that's easier to learn, easier to use. Aided by familiar SPICE models and extensions, a multi-page hierarchical schematic editor and a massive device library with models for over 7500 parts, you work quickly and smoothly—one keystroke, for example, initiates on-line simulation.

Further, this triumph comes at a very acceptable cost—$3495—less than half the price of would-be contenders.



Yet, while cost is strictly contained, design power is prodigious. A few samples? Analog behavioral modeling. Parameter stepping. Monte Carlo analysis. Nonlinear magnetic modeling. An optimizing model generator. Lossy transmission lines. On-schematic node voltage/state display. Real-time waveform plotting. Individual device temperatures.

We could go on, but our free brochure and demonstration disk can give you all the details. Ask for them. And begin reaping the rewards of total victory.

spectrum

Spectrum Software
1021 S. Wolfe Road
Sunnyvale, CA 94086
(408) 738-4387
FAX (408) 738-4702

READER SERVICE 152

DESIGN APPLICATION

Video Quality Measurements In Modern Television Systems

In-Service Testing From Vertical Interval Signals Will No Longer Be Possible.

DAVID K. FIBUSH, Tektronix Inc., Howard Vollum Industrial Park, Beaverton, OR 97007-0001; (503) 627-6289; fax (503) 627-1707.

In the last 50 years, various methods of testing television systems and evaluating video quality have progressed from the use of general-purpose oscilloscopes to a well defined set of measurements using television-specific instruments. The introduction of digital techniques into the traditional analog television system over the past 15 years has increased the range of specifications to be evaluated, but has not changed the basic testing paradigm: Indirect measurements using test signals. The recent introduction of practical video compression techniques has added a whole new dimension to video-measurement methods and the need for instruments to directly measure picture quality.

With the explosion of video compression applications, there has been a tendency by some engineers to equate digital video with compressed video. Such a definition of digital video is certainly not accurate and can lead to improper operation of a system and ineffective use of that part of the system that uses compressed video. Beyond that, analog video is sometimes completely ignored, even though modern television systems use varying amounts of analog video, including at least the pickup device and display. The point is, in operating and testing a modern television system, the analog and full-bandwidth digital segments of the video path must be considered.

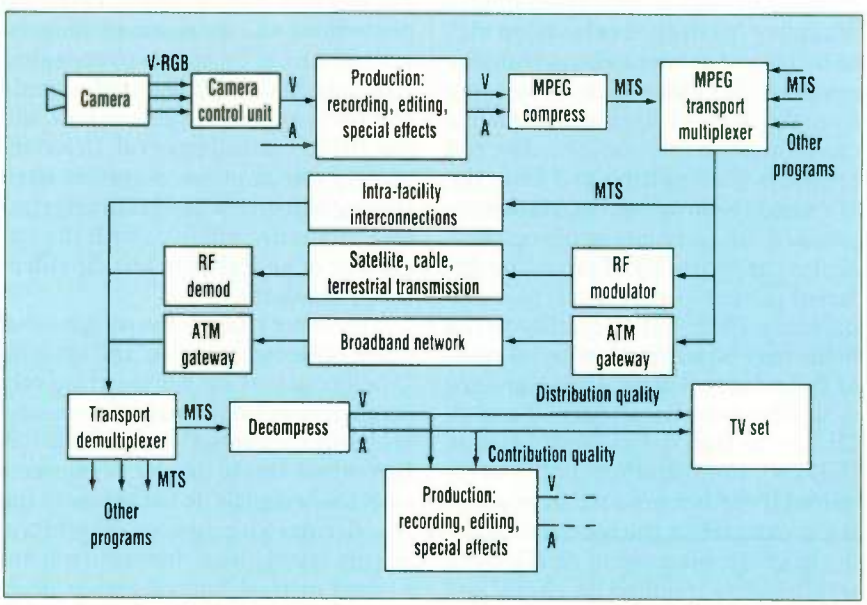
Composite analog television systems use a limited set of video signal types throughout the production and distribution chain. There are component red/green/blue (RGB) signals in the camera and display device with the composite PAL, SECAM, or NTSC signals predominant in most of the processing and distribution chain. Such systems are basically linear, which means that indirect measurement methods can be used. Degradation of appropriate test signals is measured to characterize a portion of the processing chain providing good correlation with picture quality results. Concatenation of measurement results from a series of processes also retains that correlation. Full-bandwidth digital video simply extends the concepts of analog video into a more robust signal form often including component mode operation instead of composite for further video quality improvement.

Modern Television System

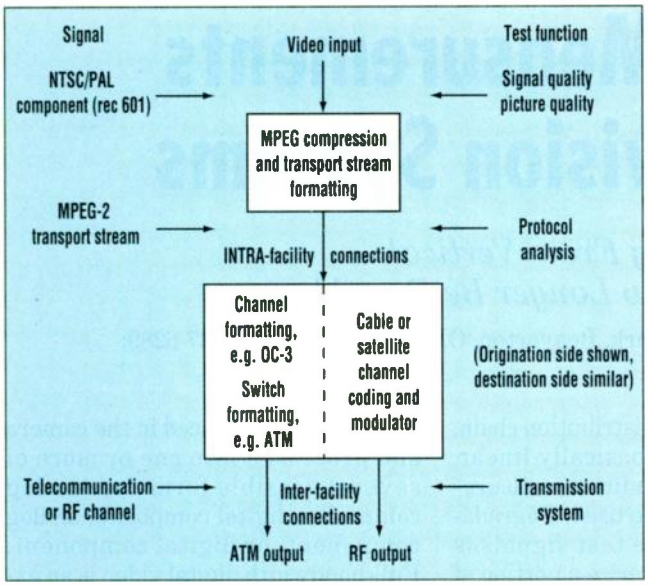
A complete modern television system is complex, requiring conversion of the video signal into a variety of signal types, including nonlinear compressed forms *(Fig. 1)*. Analog RGB video is produced in the camera and processed into one or more of several possible formats: Analog composite, digital composite, analog component, or digital component. Full-bandwidth digital video is an extremely important part of today's television system. Program-production processes must be full-bandwidth digital (or analog) in order to manipulate the audio and video to produce the desired artistic results.

Following program production, the television signal may be compressed for storage, efficient transmission, or intra-facility interconnection in digital form. Typically, this will be MPEG compression resulting in an MPEG transport stream (MTS) that may be multiplexed with other MPEG transport streams for transmission or interconnection.

Although frequency-division multiplexing is commonly used for RF



1. A modern television system is made more complex by the need to convert the video signal into a variety of signal types, including nonlinear compressed forms.



2. The need for multiple signal types also generates a requirement for multiple layers of testing.

transmission of television signals, new systems use time-division multiplexing (TDM) which is generally more robust for the same transmitted power and provides a suitable digital channel for compressed television signals. It is important to note even compressed digital video broadcasting to the home will start with full-bandwidth digital video to drive the bit-rate efficient, statistically-multiplexed compression system.

The broadband network provides a variety of transmission methods. Traditionally these have been voice-channel oriented with special data mapping for digital television signals. Use of asynchronous transfer mode (ATM) hides such formatting from the user. At the receive end of a transmission system, the desired program is demultiplexed from the MTS and the program data is decompressed. One advantage of compression is the capability of providing different picture quality levels based on bit rates. Distribution quality to the home may be adequate with bit rates of 2 Mbit/s to 8 Mbit/s for standard definition television (SDTV) and 20 Mbit/s for high definition television (HDTV). Contribution quality is required if further production processing is planned for the received signal; in that case, bit rates of 18 Mbit/s to 50 Mbit/s are required for SDTV and 270 Mbit/s to 400 Mbit/s for HDTV.

Video testing in this modern television system is not just a matter of developing new techniques for the difficult nonlinear compression process. The significant portion of the system using analog and full-bandwidth digital signals requires application of traditional analog and more recently developed digital test methods. A video-quality measurement system must take into account the various signal format changes affecting the video throughout the system before application of any picture quality measurement algorithm.

Testing Layers

Three key testing layers (uncompressed, protocol, and transmission) can be defined for the modern television system *(Fig. 2)*. Each has its own subset of more detailed testing layers. Quality measurements at the uncompressed level now consists of two parts, signal quality and picture quality. Signal quality measurements are indirect, that is, made with a suite of test signals whose resulting distortions will determine transmission-channel or video-processing characteristics. These test signals can be very short, such as just one line in the vertical interval. In a completely uncompressed system such testing will give a good characterization of picture quality (with the exception of helical-scan analog videotape recorders).

This is not true for the compression encoder/decoder part of the system. Traditional test signals are relatively simple compared to a natural scene and are easily compressed with little distortion or loss. Due to the ease of compression, these signals do not evaluate the encoder/decoder process. Therefore, picture quality measurements require a direct method, natural scenes, or an equivalent thereof, which are much more complex than traditional test signals. These complex scenes stress the capabilities of the encoder resulting in nonlinear distortions that are a function of the picture content.

Once the picture has been compressed, the resulting data is formatted for intra-facility connections. Some examples for the use of such connections include: Program interchange between video-disk servers, or several video/audio encoders sending single-program transport streams to a multiplexer to produce a multi-program transport stream for satellite broadcasting. This is an appropriate layer for protocol testing because the data formatting can be quite complex and is relatively independent of the nature of the uncompressed signals, or the eventual conversion to inter-facility transmission formats. Typical protocol-testing equipment will be both a source of known valid, or specifically invalid, signals and an analyzer which locates errors with respect to a defined standard and determines the value of various operational parameters for the stream of data.

There are a number of competing compression methods for video that use discrete-cosine transform (DCT) based coding. Other methods, such as fractiles and wavelets, are used for some applications. Picture quality testing should be designed to be coding-method insensitive whereas protocol testing is very much dependent on the coding and transmission methods. In order to send the television data to a remote location, one of many possible digital data transmission methods is used. This might be by cable or satellite using a suitable modulation system, or by the broadband network using a channel- or switch-formatting such as OC-3 or ATM packets.

Signal Quality Testing

Video systems are intended to display a picture that accurately represents the scene being scanned by the camera. With today's special effects' capabilities the displayed pictures may differ in an artistically-defined manner from the original. None-theless, at some point in the processing, where the artistic changes are complete, the resulting pictures are to be accurately transmitted to the final display device. To test the video system,

NEW
LOW COST
MICRO SIZE

Autoranging Rectifier Module

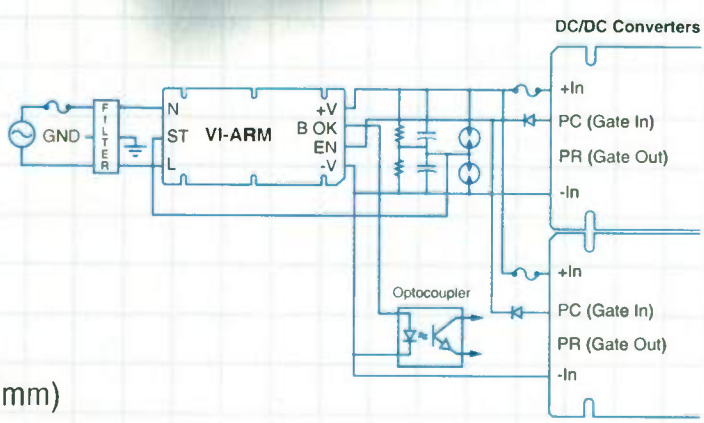
500W

Shown Actual Size

THE VI-ARM

For systems requiring a rugged, full featured, 500 Watt interface to the AC mains...in the smallest package ever.

- Autoranging: 90 to 132 VAC
- Microprocessor Controlled
- 500 Watts @ 90-132 VAC (100°C)
- 750 Watts @ 180-264 VAC (100°C)
- 96-98% Efficiency
- UL, CSA, TÜV, VDE, IEC 950
- AC OK, Module Enable
- Inrush Limiting (no external circuitry)
- 2.28" x 1.45" x 0.5" (57,9 x 36,8 x 12,7mm)



VICOR

Component Solutions For Your Power System

Vicor Corporation Andover, MA USA TEL: (508) 470-2900 • FAX: (508) 475-6715

http://www.vicr.com

WWW SITE VICOR

READER SERVICE 156

a logical sequence of tasks must be performed generally starting from the basic camera/display combination and working toward the more complex parts of the signal processing system. As each part of the system is tested to its specifications, an observer should still have a look to make sure nothing important or unusual was missed.

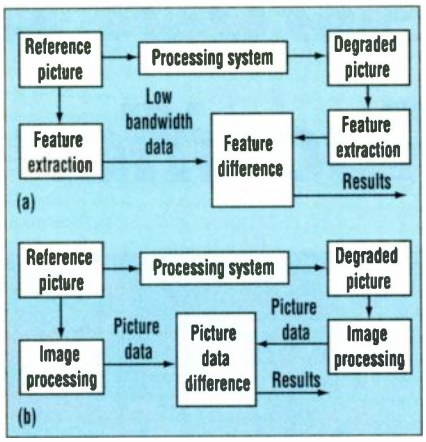
Signal quality of the uncompressed video remains critical for systems that use compression for several reasons:

- The input to a video compression codec must be accurate, in compliance with appropriate standards, and be of a high quality to provide for efficient encoding.
- Video processing such as adding titles and special effects cannot be accomplished in the compressed domain.
- Production facilities will not use full compression due to the cost and quality of compression codecs.
- The only way for different compressed formats to be interchanged is at the full bit-rate level.

This leads to a strong requirement for testing of the analog and full-bandwidth digital portions as well as the sophisticated compression and transmission systems.

Measurement practices for analog television systems are well-defined. They are based on the linear system premise that video distortions produced in a system may be accurately determined by passing suitable test signals through the same system. This is an indirect measurement method. A series of different tests are required to verify that the system will produce acceptable pictures. One test alone will not do the job.

A minimum set of tests for an analog system might be: luminance amplitude, rise/fall times, bandwidth, group delay, signal-to-noise ratio, and waveform non-linear distortions. For composite systems (PAL/NTSC) chroma amplitude, chroma phase, differential phase and differential gain are also important. A matrix of tests and specifications can be associated with different qualities of video signal transmission but no one number or mathematical combination of parameters will describe the resulting system operation.



3. Engineers can take two basic approaches to objective picture quality measurements, the use of extracted feature comparison (a) or picture differencing (b).

Processing and interconnecting video in a digital form eliminates most of the signal quality loss problems of an analog system. As the television industry transitions from analog to digital video combinations of composite and component systems, the preference is for all-component video operation. Until recently, transmission to the home viewer of this higher-quality digital signal has been accomplished by compression back to the composite analog domain while still providing a picture quality improvement over an all-analog system. With the advent of digital transmission it is now possible to deliver component-quality video to the home.

In a digital video system the component analog signal is converted to digital in accordance with the sampling standard, ITU-R BT.601 (formerly CCIR Rec 601). Formatting and studio interconnection of the digitized signal follow a related standard, ITU-R BT.656, leading to additional functional layers and a variety of tests to be performed. For operational purposes, the monitoring of equivalent analog video signal properties is still important due to the presence of operational controls in the digital chain.

Where testing of the analog signal required only that various parameters be measured on a single waveform, digital testing requires three types of analysis: Digital signal coding, digital data formatting, and parameters relating to the digital waveform. Although all three of these measurement types can be performed with a single instrument, there is significant processing between each pair of layers with different analysis methods for each layer as well. Again, a suite of appropriate test signals is required.

In a compressed video system, it is not just the compression method that determines the resulting picture quality. The quality of the video input to the compression system has a significant affect. Some of the factors to consider are:

- Incorrect amplitude or dc level may causing clipping of the picture or inefficient use of the 8-bit, 256 signal levels.
- If the bandwidth is limited (soft picture) it is actually easier to encode; however that may not represent the desired picture quality.
- Any defects that make the picture more complex will use coded bit rate in an inefficient manner. These could be such things as ringing, jitter, noise, or composite-component processing artifacts.
- Processing to remove noise or other artifacts can product better results through a compression system.

Within the compression system, complex pictures and motion are more difficult to compress. Although the specific encoding algorithm is key, the encoding parameters have a direct effect on quality, more bits, or longer GOPs (group of pictures) give better quality. A strength of MPEG is that the power of the compute engine and cleverness of the encoding can be improved over time while maintaining compatibility with older decoders that comply with the standard. This is because only the decoder is standardized, and the encoder design can be improved as increased compute power becomes available.

In a compression system there are a number of picture impairments that may occur. Loss of spatial resolution is often less noticeable, yet is the first to occur due to the coarse quantizing of the high spatial frequency components. Loss of temporal resolution most often occurs in low bit-rate systems, but also will occur in other systems where the motion estimation cannot cope with the speed or type of motion in the scene.

Think it.

It's just that easy – with LabVIEW. If you need to make measurements and analyze your data but don't have a lot of time, LabVIEW is just what you need.

Wire it.

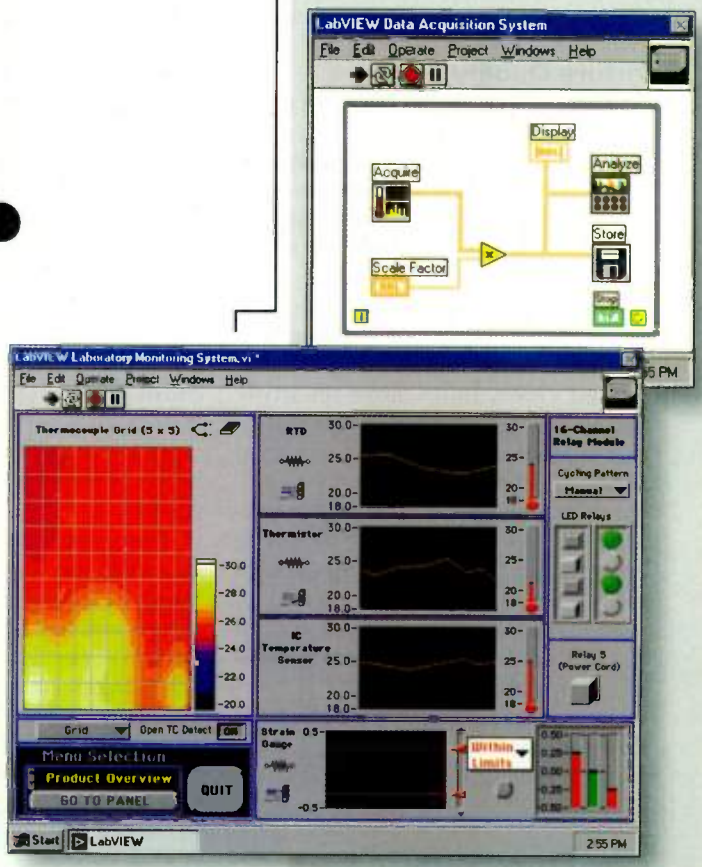
Create measurement and analysis systems in a fraction of the time it takes with any other software. Virtually every industry survey has shown that the G language in LabVIEW is the most popular development tool available for data acquisition, analysis, and presentation.

Run it.

More scientists and engineers are getting results faster and easier with LabVIEW.

Call today, and turn your ideas into reality.

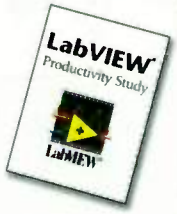
LabVIEW®
It's Just that Easy



NATIONAL INSTRUMENTS®
The Software is the Instrument

U.S. Corporate Headquarters
Tel: (512) 794-0100 • Fax: (512) 794-8411
info@natinst.com • www.natinst.com
Worldwide network of direct offices and distributors.

FREE PRODUCTIVITY STUDY



Call for your FREE LabVIEW Productivity Study today.

(800) 433-3488
(U.S. and Canada)

FREE evaluation software available.

READER SERVICE 136

Picture cropping can be intentional as with the MPEG-2 main profile at main level (MP@ML) or unintentional, in processing of the picture before the compression process. Typical DCT artifacts are blockiness (block or macroblock in size), edge "busyness," flat-area noise (sometimes called "mosquito noise"), and picture elements misplaced due to motion-compensation inaccuracies.

Picture Quality Testing

Although the term "picture quality" is commonly used, what is actually measured is picture degradation. A reference motion sequence is compared to an impaired motion sequence producing a difference value as a measure of picture quality.

Today, measurement of picture quality is accomplished by subjective methods, people evaluating the displayed video. In its more scientific forms this takes a large amount of time and resources. The widely-used ITU-R BT.500 was originally developed for non-compressed video systems. It has been, and continues to be, updated to include more aspects of human response to a variety of viewing situations and the types of defects possible in compressed television systems.

It is interesting to note that the development of more complete subjective testing methods emphasizes the fact that objective signal quality testing methods do not have perfect correlation with subjective results. In an operational broadcast environment, the subjective evaluation is generally accomplished only by expert observers, is still not calibrated in any meaningful manner, and is certainly not automatic.

What is desired is an objective picture quality measurement method. In development of such a method, three aspects should be considered: a measurement paradigm based on the complete video processing chain, an algorithm that correlates well with subjective measurements, and standardized test materials. A necessary, but not sufficient, requirement for meeting the correlation requirement is selection of an appropriate measurement algorithm. Choice of the algorithm alone is not sufficient because processing in the compression codecs or other parts of the system can have significant effects in calculation of the objective measurement results.

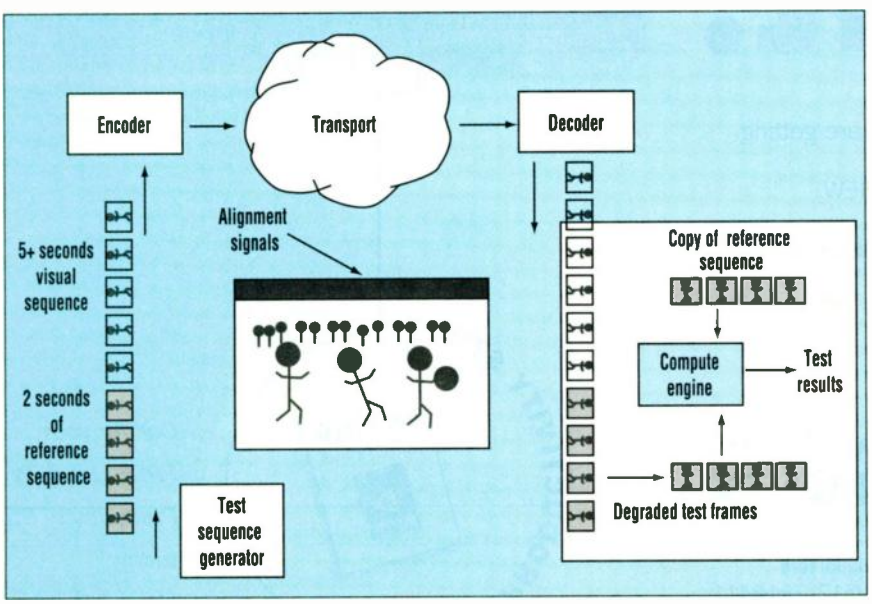
There are two basic approaches to objective picture quality measurements: Extracted feature comparison or picture differencing. The feature-extraction method has advantages for remote location measurements where the source pictures are not available *(Fig. 3a)*. However, results of experiments conducted at Tektronix indicate picture-quality measurement methods that use differencing of processed images at the measuring device provide the best correlation between subjective and objective measurements *(Fig. 3b)*.

A set of objective measurements has been standardized by the American National Standards Institute as ANSI T1.801.03. Some of the parameters measured by the standard are: Average gain, offset level, active video area, spatial shift, spatial information, temporal information, radial average of spatial frequencies, added/lost motion energy, added/lost edge energy, added/lost spatial frequencies, and peak signal-to-noise ratio (PSNR). All but one of these measurements, PSNR, can be accomplished using the feature-extraction method. PSNR is a very intuitive method—a calculation based on simply taking the absolute difference between video frames. Although PSNR can give misleading results in some situations it is still a benchmark measurement and can be useful for controlled experiments.

A combination of several T1.801.03 measurements was evaluated extensively for correlation between objective and subjective results. Unfortunately, the results of experiments did not show a high enough correlation to be included in the standard. Therefore, in the scope of the standard it states, "Experimental results indicate that the objective measures presented here are insufficient to predict viewer responses with the accuracy needed to discriminate similar systems. This standard is intended to be especially useful as a basis for comparing the present operational readiness of a system with the same system's past performance."

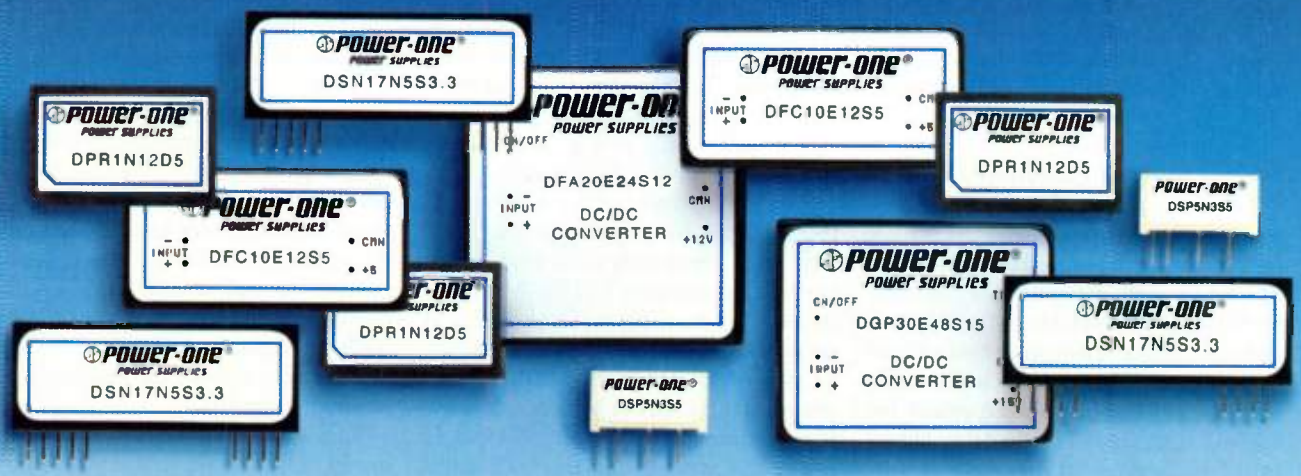
Although there are examples where a system is more or less invariant, the general case is change, either in the characteristics of the system such as changing the compressed bit rate or simply the concatenation of an uncontrolled variety of compression schemes during program production or transmission.

What is needed for picture quality measurement is an algorithm that is based on the human visual system. Such an algorithm has been developed by Dr. Jeffrey Lubin at Sarnoff Labs in Prince-



4. This proposed technique for objective picture quality measurement uses only about two seconds of video sequence, but it also allows for five or more seconds of continuous video that can be repeated or palindromed for longer viewing for subjective assessment.

DC/DC Just Got Better.



Introducing DC/DC from the number one name in AC/DC...Power-One.

POWER-ONE DC/DC CONVERTER AVAILABLE OUTPUTS

Series	Max Watts	Vin Range	Vout 3.3V	Vout 5V	Vout 5.2V	Vout 7V	Vout 12V	Vout 14V	Vout 15V	Vout 17V
Single Output products										
DSP1	1	4.5-5.5		•		•	•	•	•	•
DFA6	6	9-27, 20-60		•	•		•		•	
DFC6	6	3.5-16		•	•		•		•	
DFC10	10	9-18, 18-36, 36-72	•	•			•		•	
DGP12	12	3.5-16		•			•		•	
DFC15	15	20-60		•			•		•	
DSN17	17	4.5-6, 6.5-15.5	•	•						
DFA20	21	9-18, 18-36, 36-72	•	•			•		•	
DGP30	30	36-72		•			•		•	
Dual Output products provide the indicated Vout as one positive and one negative output										
DSP1	1	4.5-5.5		+/-		+/-	+/-	+/-	+/-	+/-
DFC10	10	9-36, 18-72		+/-			+/-		+/-	
DGP12	12	3.5-16		+/-			+/-		+/-	
DFC15	15	20-72					+/-		+/-	
DFA20	20	9-18, 18-36, 36-72		+/-			+/-		+/-	
Triple Output products provide a main output (•) and two symetrical outputs (+/-)										
DGP20	20	9-18, 18-36, 36-72		•			+/-		+/-	

- 100% dynamic load burn-in.
- CE Marking pending.
- ISO 9000 approved quality.
- Stocked by your distributor.
- Industry standard footprints and pinouts.
- Over 100 models.

POWER-ONE ISO 9000 CERTIFIED

Power-One® Power Supplies

Visit our web site at http://www.power-one.com

740 Calle Plano, Camarillo, CA 93012 (800) 765-7448 • FAX (805) 388-0476

Power-One logo and ISO 9000 logo are trademarks of Power-One, Inc.

READER SERVICE 178

ton, N.J. It is known as the "JND Image Quality Metric" where JND stands for just-noticeable difference. The reference and degraded digitized images are individually processed through several stages representing specific characteristics of the human eye. Following those processes the resulting picture data for the two images is subtracted providing a map whose intensity is related to the human perception of the differences between corresponding areas of the two pictures. Single number results of picture quality differences can be derived from the difference data using such calculations as peak or mean values. Inclusion of the JND Image Quality Metric in a suitable test instrument is expected to provide the foundation for standardization of objective picture quality measurement methods.

Measurement Considerations

In order to make objective measurements of picture quality it is necessary to ensure the two video sequences are presented to the instrument in much the same manner as required for subjective tests. That is, gain and dc level of both the luminance and chrominance must be closely matched. In addition, there must be temporal alignment and very accurate spatial alignment.

These latter two requirements are due to the need to do some sort of a differencing process between video frames as done with PSNR and the JND Image Quality Metric model. Another requirement is that the test material be such that the system being measured is working at or near the limits of its capabilities. This has always been done with traditional analog measurements (an example would be use of the 2-T pulse) and is even more important to stress the nonlinear characteristics of video compression systems. Again, as has been true in the past, one test sequence (signal) will not be sufficient. Therefore, a number of difficult test sequences must be used to test video compression systems.

Studies that compare subjective and objective picture quality measurements generally conclude there is a moderately wide variation in subjective results. This conclusion is often emphasized by one or more scenes whose subjective quality does not provide good correlation with objective measurements. It may be desirable to develop an objective method with no algorithm-breaking scenes; however, standardization of well-behaved and truly representative scenes should provide very useful results.

Considering that some program material does not conform to signal quality test results in today's analog systems (striped shirts at a frequency near color subcarrier) and that objective tests for compressed video systems are predicted to be only 90% to 95% accurate, it would seem appropriate for the industry to agree on a variety of standardized motion sequences for objective measurement of picture quality. This will allow development of very useful, if not perfect, picture quality measurement equipment.

Use of specific test scenes means that testing has to be "out-of-service." This paradigm for video testing will not be popular with those who have previously used vertical interval test signals (VITS). Although in-service testing with the actual program material would be logistically possible in some applications (monitoring a direct broadcast satellite system at the up-link location), it might not provide meaningful results for a majority of the program material that does not stress the system. Beyond that there is an operational parameter that may not be satisfactory with general program material.

The time needed to make the measurement is an important feature in test equipment. If the picture matching: gain, spatial alignment, etc., is to be done on program material, a large amount of compute time will be required to make correlation calculations. This is in addition to the time required to just make the measurement after the two video scenes are correctly matched. Therefore, it is proposed that some known alignment signals be added to the video sequences for rapid picture matching.

Objective measurements of picture quality including temporal aspects of the human visual system should be possible with about two seconds of video sequence. However, subjective assessment by an expert viewer may also be desired so the test-sequence source should provide five or more seconds of continuous video that may be repeated or palindromed for longer viewing *(Fig. 4)*.

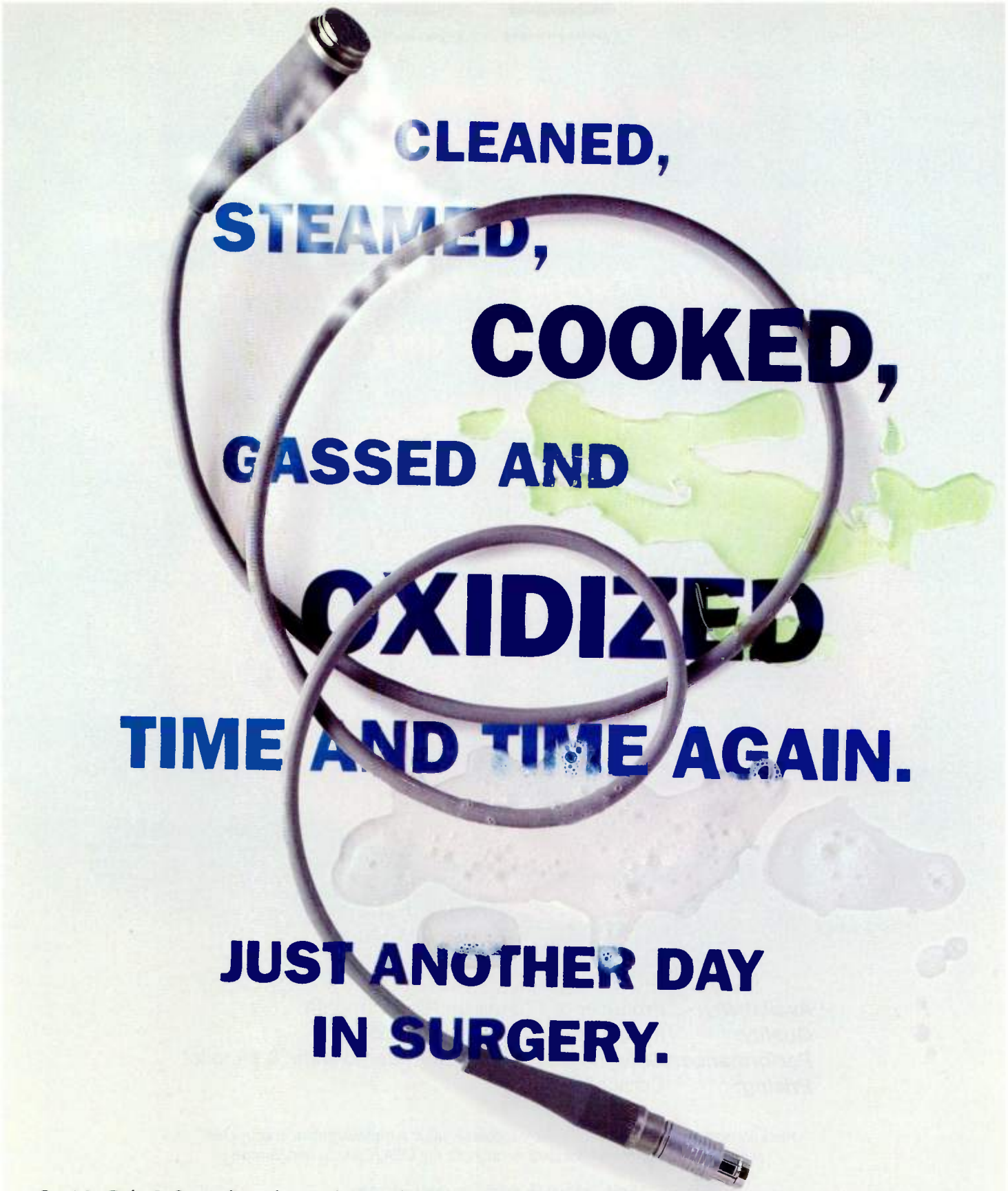
The video source could be a tape recorder of suitable quality; however, a test signal generator would be much more cost effective. Included in the video are suitable alignment signals to speed the measurement. After the video has passed through the system under test the appropriate two seconds are captured by the measurement instrument. Within the instrument is a copy of the reference sequence, thereby allowing end-to-end testing of a system where the source and destination are a great distance apart. Because of the compute power required for a temporal analysis, results are likely to take up to a minute or more to calculate.

Compressed video systems are subsets of a larger system that include traditional analog and digital video processing. The non-compressed part of the system must be attended to with care because the quality of the input to the compression system has a great affect on its ability to effectively perform its task, while both the input and output video processing can obscure the measurement of picture quality.

In addition to use of a picture-differencing algorithm, quality measurements require use of standardized test sequences to ensure strong correlation between objective and subjective results. Out-of-service testing using standard test sequences with alignment patterns will provide objective picture quality measurements suitable for comparison of different systems, as well as day-to-day operation of systems using concatenated compression methods and differing bit rates.

David Fibush is retired and consults with Tektronix in the area of MPEG-2 transport-stream testing and video quality testing for compressed television systems. He was formerly with Ampex Corp. A fellow of the SMPTE, he has spent 30 years in television engineering. Fibush has a BSEE and an MSEE from the University of California, Berkeley.

How Valuable	Circle
Highly	566
Moderately	567
Slightly	568



Steris™, Cidex™, Sterrad™ and autoclaving don't threaten the cable assemblies from Precision Interconnect. These high performance interconnect systems are engineered, manufactured and tested to withstand hours and hours of sterilization, plus the other physical abuse of the operating theatre. And still deliver power, light, and signal with RF/EM compatibility to hand-held and portable surgical devices every time. Have precise electronic requirements and unique mechanical and environmental challenges? Go ahead. Make our day.

PRECISION INTERCONNECT
an AMP company

Precision Interconnect, 16640 S.W. 72nd Avenue, Portland, OR 97224 (503) 620-9400 Fax (503) 620-7131.
Internet: http://www.precisionint.com Sales offices in U.S., Europe and Japan.

READER SERVICE 176

New JRC

...the world leader, delivers five million high quality Surface Mount Ingredients every single day!

ISO-9001 CERTIFIED ISO-9002

BIPOLAR: Operational Amplifiers
Comparators • Voltage Regulators • Audio
Video • Communications • Special Functions
CMOS: Operational Amplifiers • Comparators
Power Sources • Quartz Crystal Oscillators
Radio Communications Audio • Video & more. . .

Availability:	Producer of 170 million ICs per month
Quality:	Failure rate of one PPM typical
Performance:	Consistent to specs from wafer to wafer & lot to lot
Pricing:	Competitive

For information or to qualify for samples, please call our representative in your area.
NJR Representatives are located throughout the USA, Canada and Europe

Visit our web site: www.njr.com

JRC **NJR CORPORATION**
A SUBSIDIARY OF NEW JAPAN RADIO COMPANY, LTD.
440 East Middlefield Rd. • Mountain View, CA 94043
Phone (415) 961-3901 • Fax (415) 969-1409 • e-mail: sales@njr.com

READER SERVICE 157

Telecom Chip Set For STM-4 Solutions Is Complete To Bellcore Standards

The Latest Use Of High-Frequency Processes And Two Serial/Parallel Rate Conversions Are Now Offered In The 3.3-V Range.

PAUL McGOLDRICK

The 622-Mbit/s SDH/SONET (synchronous digital hierarchy/synchronous optical network) market is currently in a feeding-frenzy for integration and cost reductions. But in order for an IC manufacturer to be a player, they obviously need to have good high-frequency processes, either in silicon or gallium arsenide (GaAs). The higher degrees of integration are probably going to come from silicon and Maxim Integrated Products is now throwing its hat into the ring with a chip set covering the full range of applications on the high-frequency side of the transceiver.

Five Basic Blocks

The chip set cosnsists of five basic blocks which canbe grouped into three sections for the receiver and two for the transmitter *(Fig. 1)*. On the receive side, the ultra-low-power preamplifier (MAX3664) takes the fiber's signal current detected on a photodiode up to a voltage level sufficient to drive the clock-recovery and data-retiming IC (MAX3675).

From there, the recovered digital signal is fed into the deserializer IC. There are two versions of the latter—one converts the serial data into 4-bit-wide parallel data (1:4) at 155 Mbit/s (the MAX3681), and another converts the data into 8-bit-wide parallel data (1:8) at 77 Mbit/s (MAX3680). The difference is dependent on the particular carrier's overhead capabilities.

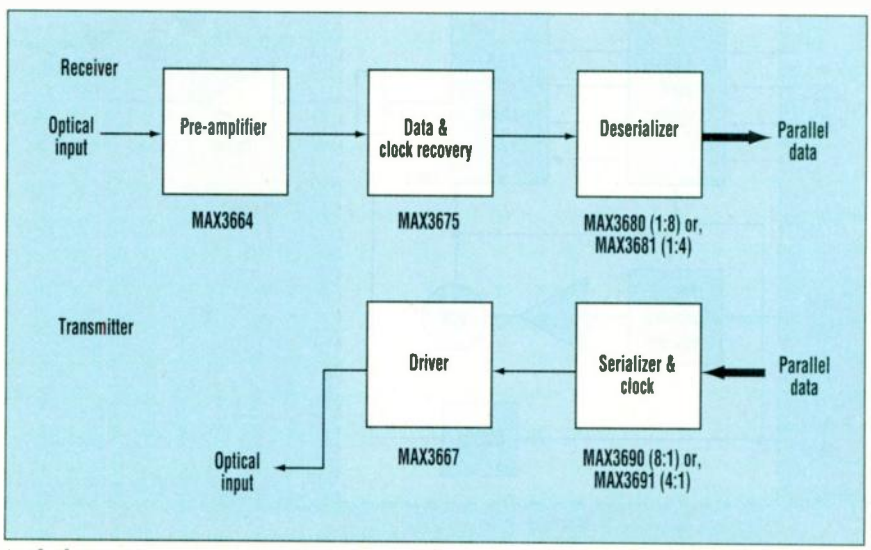
The reverse, but with only two ICs, happens on the transmit side. The parallel data words are serialized up to 622 Mbits/s from either 155 Mbit/s (MAX3691) or from 77 Mbit/s (MAX3690). In addition, each IC contains a fully-integrated PLL for clock synthesis. The output of the serializer goes to the laser driver IC (MAX3667). This last IC is the only one that requires pnp stages, and is manufactured on Maxim's CB-2 process, while the others all use Maxim's flagship GST-2 process. The entire line of integrated circuits are designed for single-rail 3.3-V power-supply operation.

Receiver Lineup

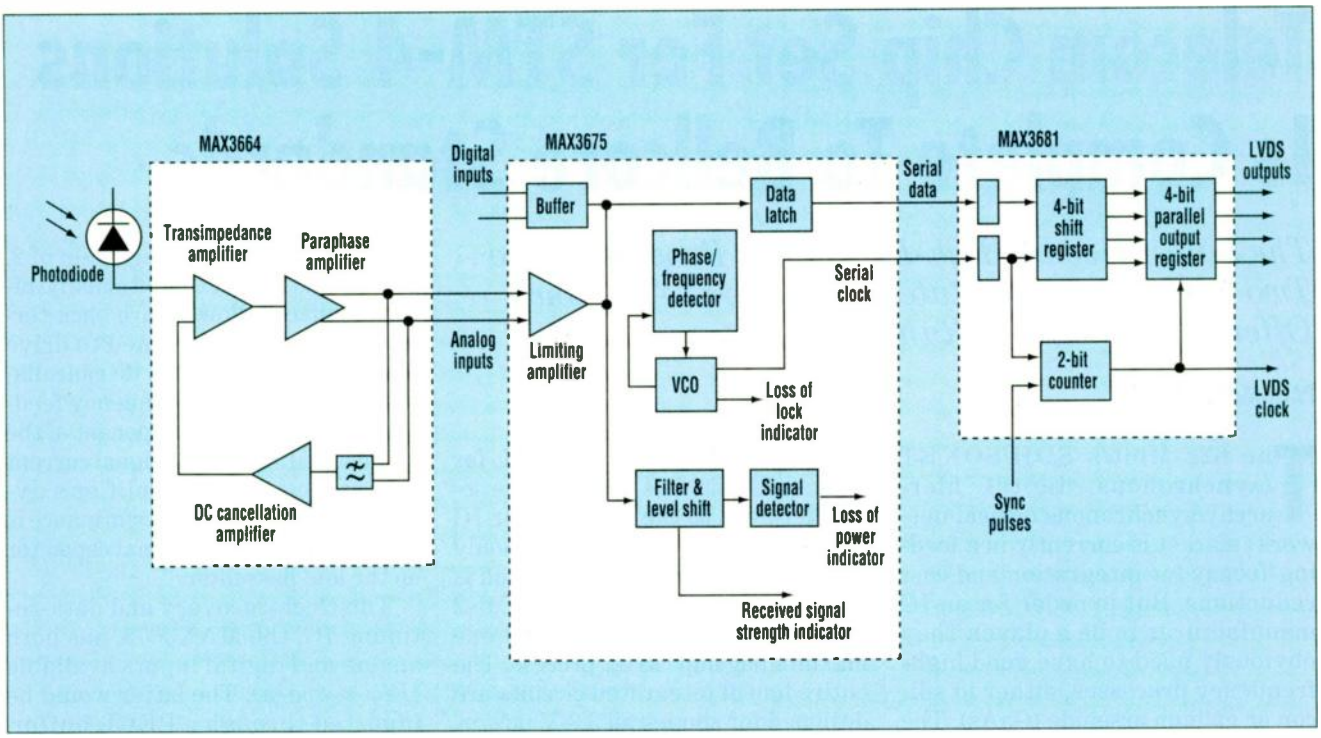
The MAX3664 is a transimpedance amplifier which has been designed for OC-12 applications *(Fig. 2)*. The small photodiode current at the summing node is converted to a measurable differential output voltage with the shunt feedback resistance. The gain is 6 kΩ for small signals while a feedback diode limits the output voltage with larger inputs. The paraphase amplifier converts the single-ended input into differential outputs with a voltage gain of 2. The outputs from the internally-biased emitter followers are back-terminated and are designed to drive loads down to 100 Ω.. A dc cancellation loop, using low-frequency feedback, cancels the dc component of the input signal so that the signal current is centered on the amplifier's dynamic range. The loop performance is determined by an external capacitor on the low-pass filter.

The clock-recovery and data-retiming IC, the MAX3675, has both analog and digital inputs available *(Fig. 2, again)*. The latter would be inputted through a PECL buffer. The analog inputs drive a limiting amplifier which consists of four full-wave logarithmic detector stages offering a small signal gain of about 42 dB with a 3-dB bandwidth in excess of 750 MHz.

The input signal can range from 3.6 mV to 1.2 V pk-pk. The limiting amplifier drives the clock/data-recovery block and also provides received-signal-strength indication (RSSI) and a loss-of-power indicator that can be programmed at any threshold voltage. In applications where the digital inputs are used, the



1. The basic arrangements of the Maxim SONET/SDH chip set for 622-Mbit/s transmissions from optical input to parallel data and vice versa.



2. Block diagram of the receive channel of the Maxim OC-12-compatible chip set.

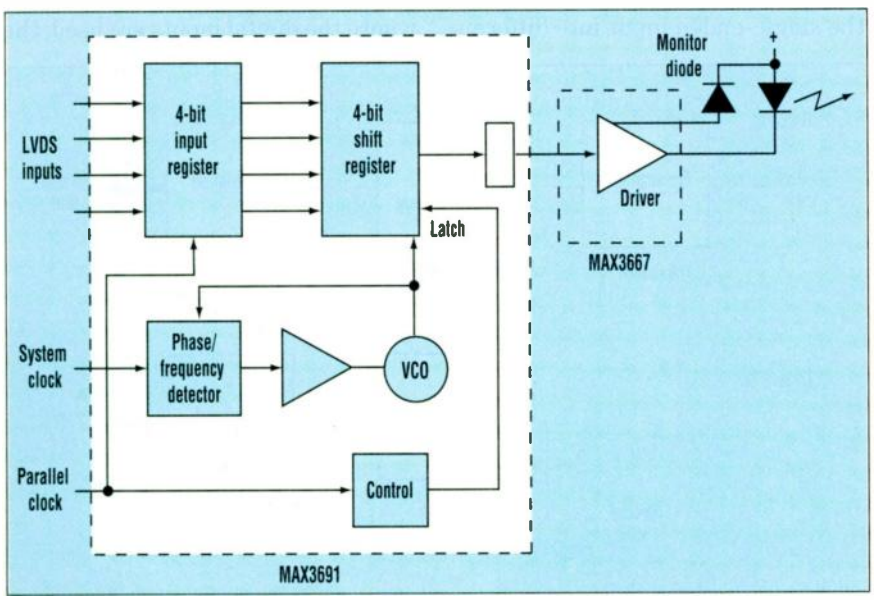
limiting amplifier block is powered down to conserve power.

The receiver's integrated phase detector produces a voltage which is proportional to the phase difference between the incoming signal and the internal 622.08-MHz clock. Its PLL drives the error voltage to zero, which aligns the recovered clock to the data. A frequency detection function is included in the loop to speed up the acquisition time when the data are outside the bandwidth of the system. The PLL has a second-order transfer function with the bandwidth set by the loop filter which is a transconductance amplifier with external filter components. The data latch provides serial data to the deserializer IC.

The MAX3681 is the 1:4 deserializer in the chip set, converting the 622-Mbit/s serial datat stream into half-bytes of 155-Mbit/s, 4-bit, parallel data. The MAX3680 uses the same basic arrangements for the conversion to 77 Mbit/s for users with slower applications who want to run their overhead at less than 100 Mbit/s. The 4-bit shift register clocks incoming data on the positive transitions of the serial clock, which also is fed to a 2-bit counter to be divided down to the parallel clock rate, latching the output register every four bits of incoming serial data.

Both the inputs and outputs of the MAX3681 are low-voltage differential signals (LVDSs) based on IEEE-1596.3 standard with 250 to 400 mV pk-pk differential swings giving fast transitions, good noise immunity and low power dissipation. Termination of the LVDSs is between the inverting and noninverting lines.

The parallel data lines together with the parallel clock would be fed off in the application to the overhead termination and management with microprocessor control and alarms.



3. The transmit channel of the Maxim MAX36XX chip set for 622-Mbit/s SDH/SONET transmissions.

Transmitter Lineup

On the transmit side, the opposite would be the case with data. Frame pulse and clocks being provided to an overhead control to produce a 155-Mbit/s parallel data stream.

The 4:1 serializer IC, the MAX3691, takes in the half-byte-width parallel data and their associated clock through the input register (clocked at 155 MHz) and shift-registers it to the 622-Mbit/s serial rate *(Fig. 3)*. The system clock can be a submultiple of 622.08 MHz and the PLL fully synthesizes the OC-12 clock with a maximum output jitter of 13 ps. The center frequency of the voltage-controlled oscillator (VCO) is set with laser wafer trimming.

The MAX3667 is a complete laser driver for 622 Mbit/s. It accepts differential PECL inputs and provides complementary output currents. Both modulation and bias currents can be set from 5 to 60 mA. A monitor diode can be set up in an automatic loop for control of average power (bias current) and modulation signal control over both the temperature range and lifetime of the diode.

Conclusions

Thanks to its careful attention to detail and efficient partitioning of functions, Maxim's design team has arrived at a cost-effective solution for the termination of high-speed optical communications links. As 622-Mbit/s links become more commonly used, these parts will help designers meet the increasing pressure to deliver equipment that climbs ever higher on a steepening price/performance curve.

PRICE AND AVAILABILITY

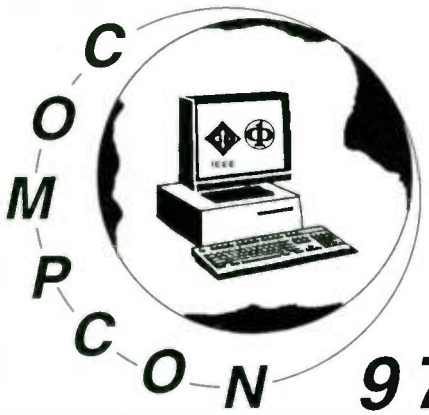
The MAX3664 is available in die form, in an 8-lead SO, and in 8-lead mMAX packages at $15 each. The MAX3675 is available in die form, and in 32-lead TQFPs at $45 each. The MAX3681 is available in a 24-lead SSOP at $19 each. The MAX3680 is available in a 28-lead SSOP, also at $19 each. The MAX3690 and MAX3691 are both available in 32-lead TQFPs at $50 each, as is the MAX3667, also available in die form at $15 each. All prices are in 1000-unit lots. The MAX3664, MAX3681, and MAX3680 are available now; the others will be available in March.

Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086; (800) 998-8800, or (408) 737-7600; Internet: http://www.maxim-ic.com.

CIRCLE 502

How Valuable	Circle
Highly	531
Moderately	532
Slightly	533

HOT Systems/COOL Software



97

"If you could only attend one technical conference a year to learn the overall state of the industry, COMPCON would be your choice." — Dr. Darrell Long, Conference Chair, Computer Science Professor, UC Santa Cruz

San Jose Hilton & Towers
Downtown San Jose, CA

February 23-26, 1997

INTERNET/INTRANET TECHNOLOGY
- Trends
- Environments
- Applications

SYSTEMS
- Superservers
- Mobility
- Software Architecture

MICROPROCESSORS
- High Performance
- Low Power

PERIPHERALS
- Mass Storage
- DVDs
- Display Technologies

MULTIMEDIA
- Technologies
- Software Environments
- Applications

PARALLEL/DISTRIBUTED SYSTEMS
- Applications
- Hardware
- Compilers

EMERGING TECHNOLOGIES
- GHz Devices
- Advanced Hardware
- Java

OPERATING SYSTEMS
- Object-Oriented
- Microkernels

INTERCONNECTS
- Parallel Computers
- LAN and WAN
- Wireless

VIDEO
- Advanced Displays
- Digital

TUTORIALS INCLUDE:
- 3-D Graphics
- Virtual Reality
- Web Site Design & Security
- Advances in Computer Architecture
- Java
- CORBA

PLENARY SPEAKERS INCLUDE:
- **Federico Faggin (Synaptics)**
  The Microprocessor: Its History & Future
- **Hector Garcia-Molina (Stanford)**
  Meta-Searching Across the Internet
- **David K. Gifford (MIT, OpenMarket)**
  The Future of Electronic Commerce
- **Ted Laliotis (Laliotis and Associates)**
  To Tax or Not to Tax Internet Transactions
- **Dave Nagel (AT&T)**
  Frontiers of Electronic Commerce
- **Prof. Randy Katz (UC Berkeley)**
  Is Wireless Dead?

REGISTRATION AND INFORMATION:

E-Mail: COMPCON@LBL.GOV
Fax: 510-422-2495
Phone: 510-422-2199

Mail: COMPCON 97
c/o Dave Hunt, L-130
LLNL, PO Box 808
Livermore, CA 94551

You can register on our Home Page. Corporate rates are available.

SPONSORED BY THE IEEE/CS

COMPCON has no marketing presentations or product exhibitions and is a non-profit technical conference sponsored by the Computer Society of the Institute of Electrical & Electronic Engineers.

COMPCON 97 CHAIRS

Darrell Long, General Chair
darrell@cse.ucsc.edu

Michael Harrison, Program Chair
harrison@cs.berkeley.edu

Theodore Laliotis, Steering Chair
laliotis@crl.com

COMPCON thanks Electronic Design magazine for the generous support it has provided to our conference.

"COMPCON has been consistently a valuable conference presenting a broad technical program on state-of-the-art computing technologies." — Dr. Joel Birnbaum, Vice President R&D and Director of HP Labs

COMPCON 97 Home Page: http://www.compcon.org

Monolithic IC Oscillator Has Near-Quartz Stability

A Tiny 200-kHz To 100-MHz IC Oscillator Offers ±1% Frequency Stability Over Commercial Temperature Range While Operating At 5 V ±10%.

FRANK GOODENOUGH

You're a system designer and you need a relatively precise oscillator in the frequency range between 200 kHz and 100 MHz. It's got to meet specifications over the commercial temperature range. You don't need crystal accuracy, nor can you afford it. Any conventional RC oscillator you might design can't cut your stability needs, and just as important, will take too much expensive pc-board area. In addition, you don't have a stable oscillator to phase lock to or to count down from.

Designers in need of such an oscillator may find what they're looking for from the folks at Dallas Semiconductor. They realized that there could be a variety of applications for that type of oscillator (analagous to the ubiquitous 555 timer), and therefore created the DS1075, a simple IC with the desired oscillator performance *(Fig. 1)*.

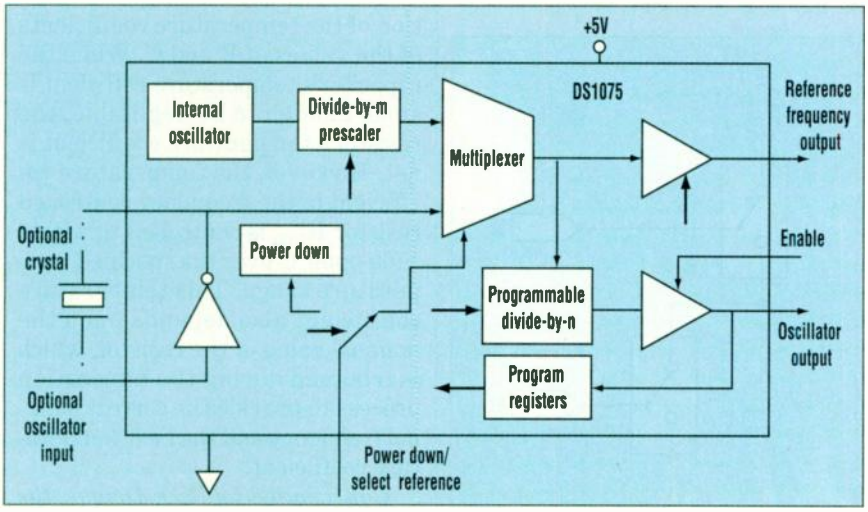
Called the EconOscillator, the chip is crammed into an 8-pin SOIC package and contains a novel oscillator circuit capable of operation from a few hundred kilohertz to beyond 100 MHz *(see "How Does The EconOscillator Work?" p. xx)*. The oscillator's stability approaches that of a crystal-based oscillator, and the EconOscillator does not require additional external components. In addition, its output frequency is user- or factory-programmable.

Typical applications range from backup system clocks to a handy lab clock/oscillator. This fixed-frequency oscillator permits the user to buy an off-the-shelf IC and digitally program it in the system during or prior to manufacture. Design changes are accomodated on-the-fly simply by programming different values into the IC (or by reprogramming previously-programmed devices).

The EconOscillator consists of an on-chip master oscillator factory programmed between 66 and 100 MHz *(Fig. 2)*. Variations in its output frequency due to changes in temperature and/or supply voltage are compensated for and combined with a programmable divider to provide a wide range of possible output frequencies. The value of the programmable divider is stored in EEPROM, which can be programmed at the factory by request, or may be configured by users to suit their individual preferences. The master oscillator is factory trimmed to be within 0.5% of the nominal value, and exhibits a variation over the commercial temperature range of less than ±1%. On-chip compensation for supply-voltage variation allows operation at 5 V ±10% with less than a ±1% variation in output frequency.

The accuracy, although not up to that of a crystal oscillator, is adequate for many applications. And for these applications, the instability is offset by the lower cost and smaller footprint of the 8-pin SOIC package when compared to that of metal-can crystal oscillators.

The DS1075 also offers features not found on other crystal oscillators. An output-enable function ensures that the output will only be disabled or in a high-impedance state when it's low, preventing pulse distortion as a result of the enable signal timing. Likewise, when the output is enabled, only full output pulses will be produced. In addition, a power-down command turns off most off the internal circuitry and reduces current drain to the microampere level. On power-up, this circuit combines with a power-on-reset function that inhibits the output until the oscillator has stabilized.



1. The DS1075 econoscillator from Dallas Semiconductor contains a unique programmable high-frequency (100-MHz) oscillator that offers stability close to that of a crystal oscillator over wide variations in temperature and supply voltage.

Timely Timing

Timing-reference options further enhance the flexibility of the EconOscillator. For instance, an external clock signal of up to 50 MHz can be fed to the DS1075's optional

The DS1075 EconOscillator contains a novel oscillator circuit capable of operating over a frequency range from below 200 kHz to over 100 MHz. Its stability runs close to that of a crystal oscillator. It uses a feedback topology similar to that of phase-locked loops (PLLs), but because it's a standalone oscillator, there's no reference frequency for the circuit to "lock" onto.

The circuit contains a voltage-controlled oscillator (VCO) whose output frequency, f_{out}, is the output for the EconOscillator *(Fig. 1)*. A divide-by-N (+N) circuit divides down the VCO's output to produce the feedback frequency, f_o. The feedback circuit stabilizes the loop and controls the DS1075's output frequency with f_o.

A control voltage for the VCO is derived from two resistors—R and R_{freq}—which are fed by a pair of identical current sources—I_1 and I_2. The voltages across resistors R and R_{freq} drive difference-amplifier A. Its output feeds a low-pass filter (LPF) that removes noise and becomes the control voltage (VC) for the VCO.

At the heart of the circuit lies the frequency-controlled resistor, R_{freq}. Actually, R_{freq} is a simple switched-capacitor circuit *(Fig. 2)*. The switches turn on and off with alternate phases ($\phi 1$ and $\phi 2$) of the feedback frequency, f_o.

The charge Q on the switched-capacitor C is given by the equation:

$$Q = CV.$$

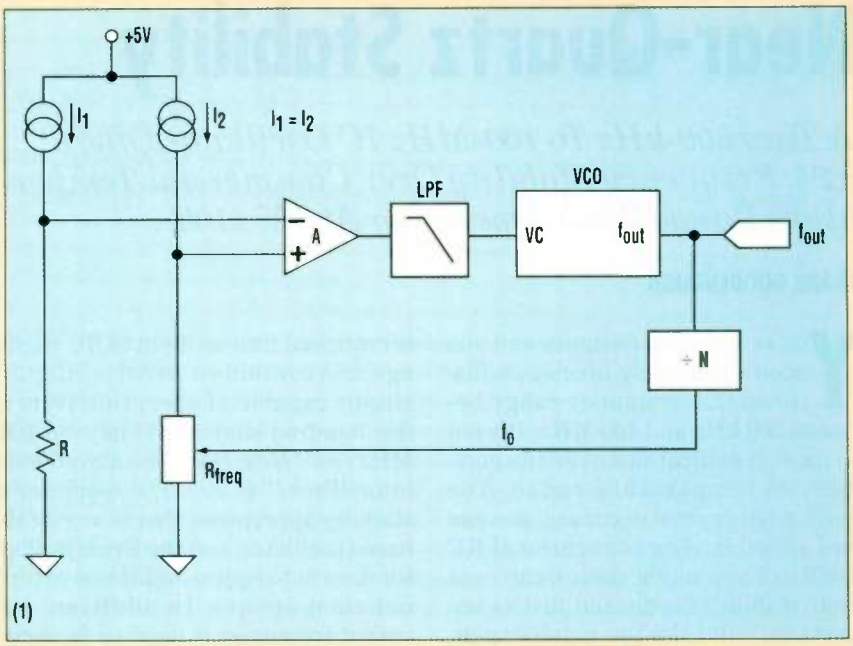
The current i running through C is expressed as:

$$C = C(dV/dT) = CV/T$$

where $T = 1/f_o$.

As a result, the current is equal to f_oCV.

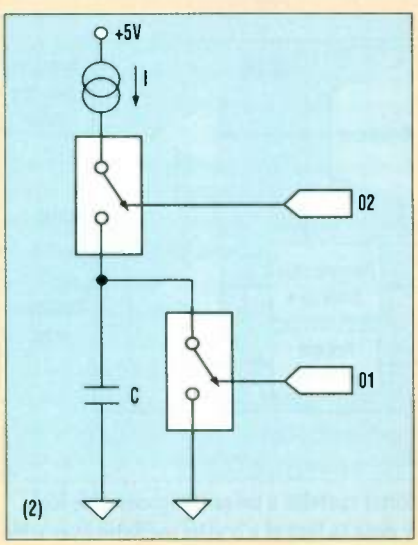
Because R = V/i, the effective resistance of $R_{freq} = 1/f_oC$, where C is the value of the capacitor in the switched-capacitor circuit. Therefore, when f_o rises, R_{freq} drops. As a result, the voltage at the plus input of the difference amplifier drops, reducing the value of the control voltage (VC) to the VCO.



The VCO's output frequency is directly proportional to its control voltage, so the output frequency drops when R_{freq} decreases. When R_{freq} equals R, VC remains constant and the output frequency also is constant. The output frequency f_{out} of the complete circuit is therefore given by the equation:

$$f_{out} = N/RC$$

EconOscillator's nominal frequency is set by the values of N, R, and C. In the DA1075, N and C are constant, and the value of R is trimmed with the programmable-resistor technology that's used in Dallas Semiconductor's silicon delay lines. These trim values are stored in EEPROM.



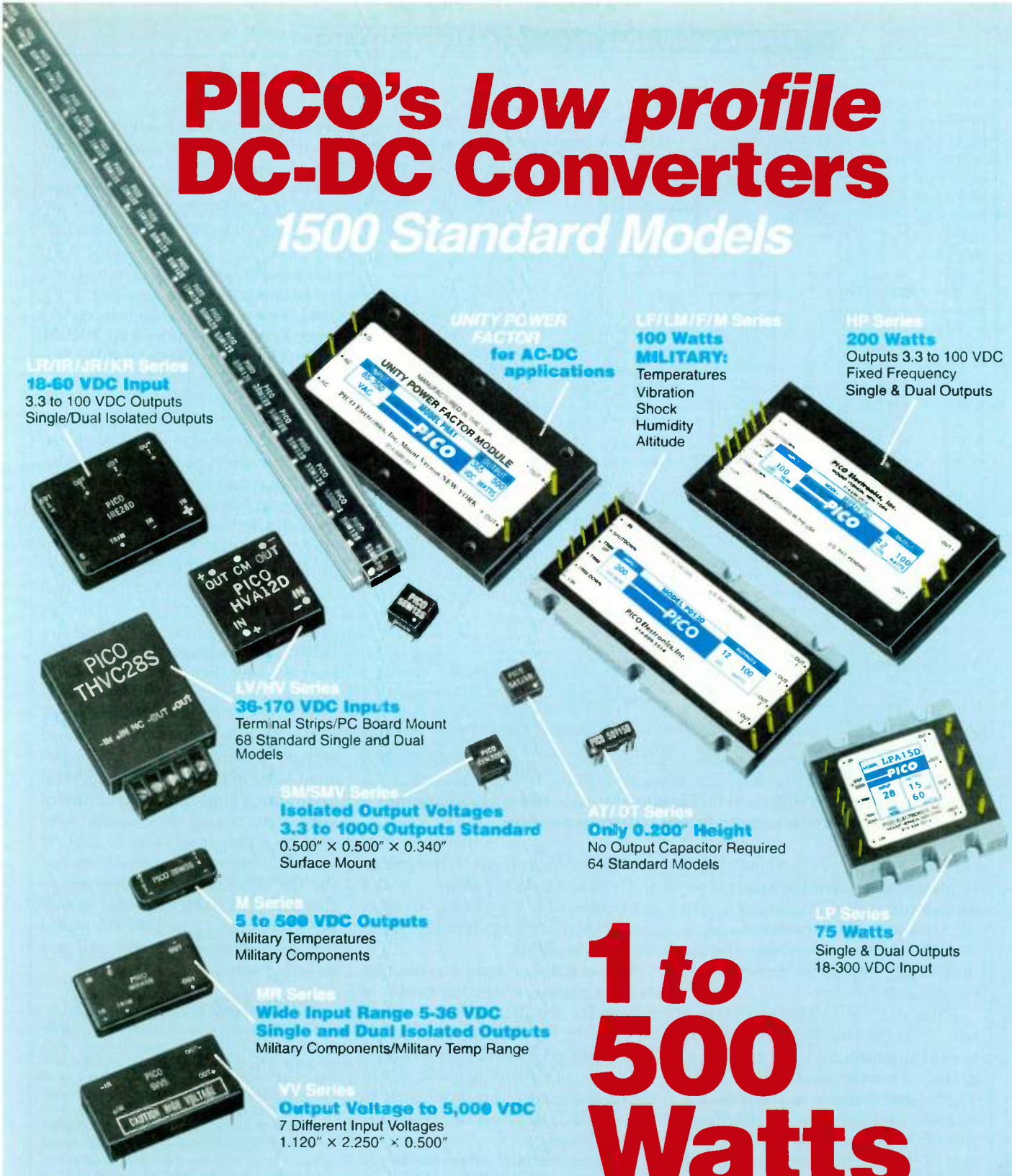
The oscillator's temperature and voltage coefficients are very low. Operating the two frequency-setting resistors from current sources and using the unique feedback-loop oscillator topology keeps the voltage sensitivity low as long as the op-amp's open-loop gain is high.

Temperature stability is a function of the temperature coefficients of the values of R and C. While the capacitor's temperature cofficient is small enough to be negligible, the resistor's temperature coefficient is not. However, the temperature coefficient of the frequency controlled resistor R_{freq} is controlled to within ±100 ppm/°C over the specified temperature range. This temperature coefficient also depends upon the nominal value of the resistor, which is trimmed during the fabrication process to provide the correct nominal frequency and the best temperature coefficient.

Contributed by Rick Downs, the applications development manager for Dallas Semiconductor Corp.

PICO's *low profile* DC-DC Converters

1500 Standard Models



LR/IR/JR/KR Series
18-60 VDC Input
3.3 to 100 VDC Outputs
Single/Dual Isolated Outputs

UNITY POWER FACTOR
for AC-DC applications

LF/LM/FM Series
100 Watts
MILITARY:
Temperatures
Vibration
Shock
Humidity
Altitude

HP Series
200 Watts
Outputs 3.3 to 100 VDC
Fixed Frequency
Single & Dual Outputs

LV/HV Series
36-170 VDC Inputs
Terminal Strips/PC Board Mount
68 Standard Single and Dual Models

SM/SMV Series
Isolated Output Voltages
3.3 to 1000 Outputs Standard
0.500" × 0.500" × 0.340"
Surface Mount

AT/DT Series
Only 0.200" Height
No Output Capacitor Required
64 Standard Models

LP Series
75 Watts
Single & Dual Outputs
18-300 VDC Input

M Series
5 to 500 VDC Outputs
Military Temperatures
Military Components

MR Series
Wide Input Range 5-36 VDC
Single and Dual Isolated Outputs
Military Components/Military Temp Range

VV Series
Output Voltage to 5,000 VDC
7 Different Input Voltages
1.120" × 2.250" × 0.500"

1 to 500 Watts

3.3 to 5000 VDC Output Standard

COTS/Industrial/Military
All with PIN to PIN Compatibility

Whether Your Requirements Are Board Level Or An Entire Power System, PICO Can Meet Your Needs With Our Catalog Items Or Optimize Your Circuit With Special Designs—Over 1500 Standard Models

Send direct for ***Free*** *PICO Catalog.*

For engineering assistance or to place an order ***Call Toll Free 800-431-1064***

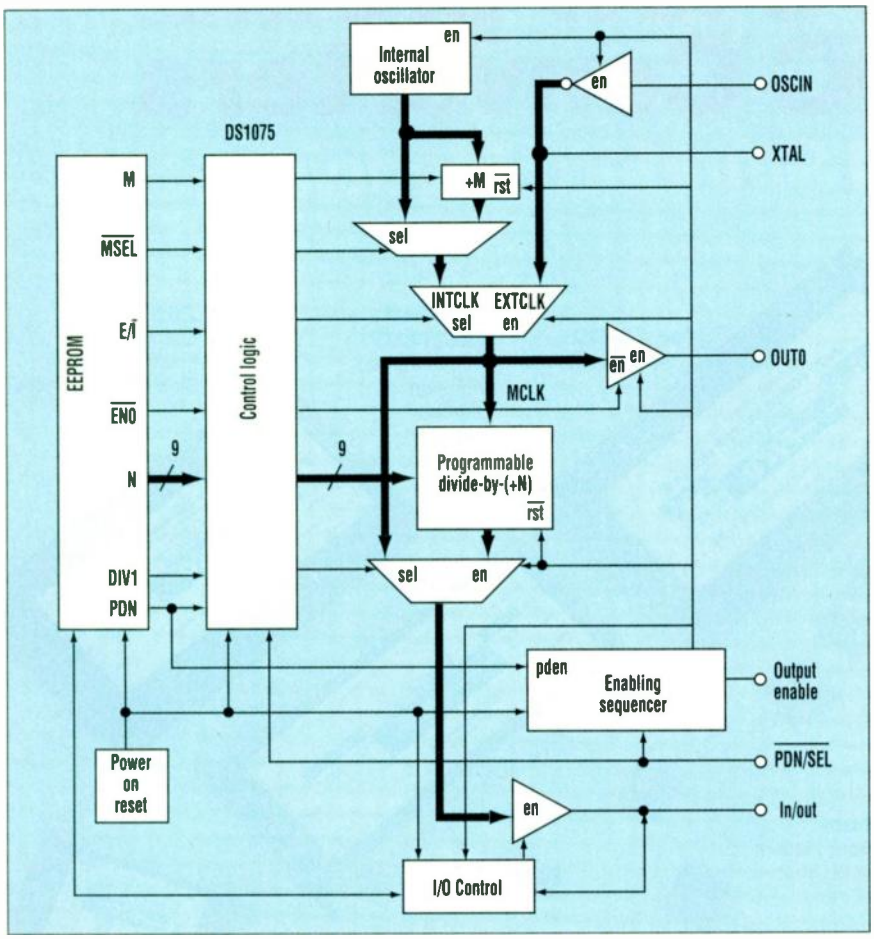
VISA & MasterCard
Visa and Master Charge Accepted

PICO Electronics, Inc.

453 N. MacQuesten Pkwy., Mt. Vernon, N.Y. 10552 • 914-699-5514 • FAX 914-699-5565

Delivery—stock to one week

READER SERVICE 181



2. Packages in a tiny 8-pin SOIC, the DS1075 EconOscillator can be used as a back-up system oscillator that's ready to cut in automatically if the system clock goes array.

oscillator input pin to be used as a reference instead of the internal oscillator (or used in conjunction with it). Alternatively, a crystal as high as 25 MHz can be connected to the optional input to produce a very stable reference frequency.

Either the internal reference or one of the previously mentioned external options can be user programmed via the on-chip EEPROM. The reference choice can be made pin selectable by using an alternate function of the power-down pin (the function of this pin is determined by the EEPROM).

A buffered output, derived from the external reference, is available and may be disabled to save power. Because the internal oscillator is running at a higher frequency than the external reference, a simple on-chip prescaler circuit divides down the internal oscillator to a similar frequency value. These features allow easy generation of submultiples of an existing stable reference, the generation of a stable reference, or the generation of a "limp home" clock in the event that a system clock becomes unavailable.

The available output frequencies and the various operating modes of the device are all programmed into an on-chip EEPROM. This EEPROM is programmed by powering up the device in a program mode, where the output serves as a serial input to the EEPROM using the Dallas 1-wire technology.

The programmed values can be set at the factory for volume orders, or can be user-programmed via a development board available from Dallas Semiconductor. This board, the DS1075K, connects to a standard PC running Windows 95, and lets the user easily set the various output frequencies and operating modes, experiment with changes, and program the desired parameters into the device. Once the device has been programmed, applying a 5-V supply to the device results in normal operation.

It's user-programmable option makes the DS1075 well suited for breadboarding new applications and for pre-production runs. Any changes can be quickly accomodated by reprogramming the parts by hand. For volume production, on the other hand, the required EEPROM values can be programmed at the factory prior to shipment.

The DS1075's reasonable accuracy with no external components, enable- and power-down modes, choice of timing reference, user programmability, small surface-mount packaging, and low cost combine to make the EconOscillator suitable for many applications. Based on the ease of implementation, the ability to reprogam almost instantaneously, and the savings in cost and board space, system designers may find the DS1075 to be a preferred alternative to crystal oscillators for many applications.

The cost of the DS1075 compares well with a typical metal-can-based crystal oscillator. However, to implement some of its features in a crystal oscillator would require additional logic circuitry that could up the total cost by a factor of two. In fact, it would be cheaper and easier to use the DS1075's crystal-reference option and just hang a crystal on one pin. In addition, the DS1075 would require less pc-board area and less assembly time.

PRICE AND AVAILABILITY

The DS1075 is available in 8-pin DIPs and 150-mil SOICs. In quantities of 1000, the 8-pin DIPs cost $1.62 each, and the 150-mil SOICs cost $1.70 each. Four versions of each package type are available. Their nominal output frequencies are factory programmed at 100, 80, 66, and 60 MHz. The development/evaluation kit (DS1075K), which allows programming and software control over the operating modes of the DS1075, is available from Dallas Semiconductor at approximately $60 each in unit quantities.

Dallas Semiconductor, 4401 S. Beltwood Pkwy., Dalllas, TX 75244-3302; contact Steve Brightman at (972) 371-3865.

CIRCLE 502

How Valuable	Circle
Highly	528
Moderately	529
Slightly	530

Highly Integrated Compact CCD Camera Targeted For PC/Desktop Video

The Micro Unit CCD is a hybrid combination of a CCD image sensor, sample-and-hold amplifier, ADC, and timing generator on a single ceramic carrier with a built-in

lens. The hybridunit produces digitized raw data that can be processed by the host computer. Or, if it's needed, the data can be processed with a camera signal-processing DSP to give a standardized, formatted digital Y, B-Y, R-Y.

Ideal applications for the unit would be when it is built into a PC for desktop video, or in a laptop or PDA. Other applications include portable video phones, vehicle cameras, door video phones, and toys. With a size of only 17.5-by-17.5-by-9.8 mm, the unit is easily installed as a embedded part. The fixed focal length lens of F2.8/f = 2.9 mm delivers a horizontal viewing range of 48° from 20 cm to infinity.

The part is mounted in a 64-pin ceramic LCC, with the CCD image sensor being the new ICX096 (for 525-line/NTSC) or ICX097 (for 625-line/PAL). These are interline transfer CCDs with a 1/6-in. optical format. They replace the ICX086/087 CCDs, reducing the chip size by 43% to 3.30-by-2.95 mm. Active pixel count is 510 (horizontal) by 492 (vertical) for the ICX096, and 500-by-582 for the ICX097.

The chips are fitted with a yellow/cyan/magenta/green complementary color mosaic filter. They can be shuttered at variable speeds, although they would be typically be operated at frame rates of 1/60 and 1/50 s for the ICX096 and 097, respectively. A low-noise amplifier is built into the chip.

Resolutions of up to 330 TV lines are possible with the basic chip, while the Micro Unit CCD operates with a 362-by-492 pixel configuration and a resolution of 200 TV lines, conforming to the Common International Format (CIF). It outputs 9-bit color CCD raw data. Power consumption is about 630 mW.

Production quantities will be priced at about $60 each. Commercial production will begin in the second quarter of 1997.

Sony Semiconductor Company of America
3300 Zanker Rd.
San Jose, CA 95134
(800) 288-SONY, or (408) 955-6572
fax (408) 955-5176;
Web at http://www.sel.sony.com.
CIRCLE 631

PAUL McGOLDRICK

10-A, Full-Bridge Output, Hybrid PWM Amplifier Delivers 94% Efficiency

The SA02 amplifier is an 80-V, 250-kHz pulse-width modulation (PWM) amplifier. It contains a full-bridge output circuit, which provides 10 A of continuous output drive

for applications from brush-type motor drives to hi-fi amplifiers. With a power bandwidth out to 25 kHz, other applications for the hybrid switching or Class-D amplifier could be in vibration cancellation, shaker tables, or high-speed linear microstepping motors.

The heat sink requirements for a PWM amplifier are reduced by a factor of about 5:1 compared to analog amplifiers. Moreover, the high switching frequency allows for smaller, lighter filter components, with efficiency at the 10-A, 80-V levels typically running at 94%. The output bridge is in an H-bridge format, and the four FETs are provided with individual temperature sensing. The bridge can be operated from 16 to 80 V with up to 800 W continuous output power and 1200 W peak power. The maximum thermal resistance junction-to-case is 1.6 °C/W, and the typical thermal resistance junction-to-air is 15 °C/W. The gain-bandwidth product is 4.5 MHz and the open-loop gain into 10 kΩ is a minimum of 94 dB.

The internal clock is available to drive other amplifiers, or it can be driven and locked by another amplifier or other external clock source. A separate integration amplifier is avaiable on-chip and can be used prior to the pulse-width modulation. The characteristics of the integrator can be externally varied.

The inputs to the modulator can be accessed externally for applications such as those in digital motion or sensing.tem. Current sensing can be separated out while a different pin is provided for logic-level controlled shutdown of all output bridge drivers in either a shutdown-current or shutdown-voltage mode.

The 18-pin steel package is hermetically sealed. An evaluation kit with a pc board and heat sink (EK02) is available for prototyping, while general assistance is available from the company in both the data sheet and their catalog. Pricing is $295 in 100-unit lots. Sample devices are from stock, production orders require six weeks.

Apex Microtechnology Corp.
5980 North Shannon Rd.
Tucson, AZ 85741
(520) 690-8608
e-mail:
PRODLIT@TEAMAPEX.COM
Web: http://www.teamapex.com.
CIRCLE 632

PAUL McGOLDRICK

This interactive, easy-to-use productivity tool is an EE's guide to the future.

1990-1994

$95

Five years of ELECTRONIC DESIGN on CD-ROM

Electronic Design on CD-ROM includes all of the articles, illustrations and line drawings that appeared on the pages of *Electronic Design* between 1990 and 1994. Complete with a search engine and hypertext links, it is a compendium of value added design information available nowhere else.

To order, simply complete, mail or fax this card or call: 201/393-6062; Fax 201/393-6073.

ELECTRONIC DESIGN's CD-ROM

Amount

☐ Single order: _____

☐ Multiple order: Quantity: _____ x $95 = _____

Please add $5 for S & H per disk _____

Total _____

Mail to:

Electronic Design CD-ROM
611 Route 46 West
Hasbrouck Heights, NJ 07604
Attn: CD-ROM Order Dept.

or fax: 201/393-6073

Method of Payment: ☐ Master Charge ☐ American Express ☐ VISA

Account Name _____ Account # _____

Signature _____ Expiration Date _____

Name _____ Title _____

Company _____

Company Address _____

City _____ State _____ Zip _____

Phone _____ Fax _____ E-mail _____

(Allow 6 to 8 weeks for delivery)

New Parasitic-Extraction Tools Needed For DSM Flows

IC Designers Face New Challenges As Geometries Migrate Toward 0.25-µm Design Rules.

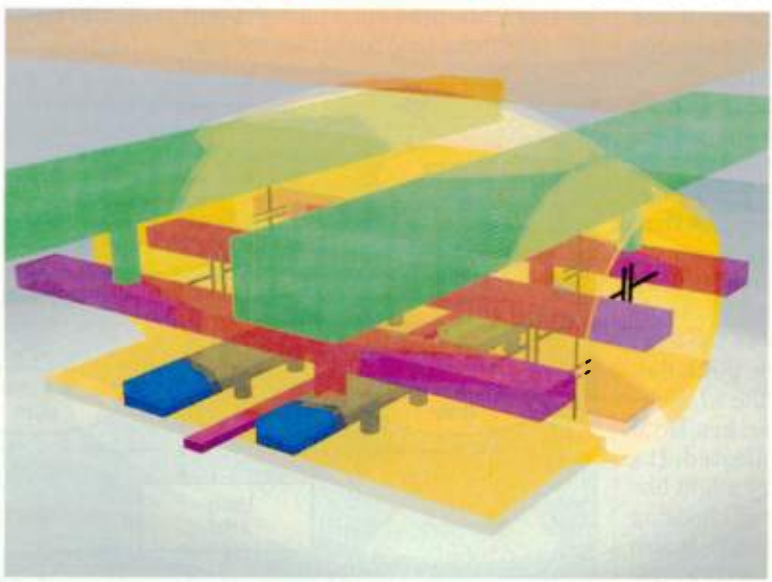
Cheryl Ajluni

SPECIAL REPORT

Today's IC designers need more from their design software than ease-of-use and flexibility. The software also must have good interfaces to other point tools and must be cost-effective. But bridging the gap between what designers want and what tool vendors deliver is only one of the challenges that designers must face. Don't forget about shortened design cycles, higher speed (50 MHz and above), and more complex designs. At 0.5-µm design rules these obstacles are manageable. But as geometries shrink, things can get quite difficult.

Many existing tool sets show signs of cracking at 0.35 µm. And at 0.25 µm, everything falls apart. This area, known as deep submicron (DSM), poses special challenges to designers who are used to the current design methodologies. The problems arise because issues such as capacitance and resistance, which in the past were not important, have now become crucial to the success of a design.

Parasitic extraction (PE) is the part of the design flow that takes these factors into effect. PE is now under heavy investigation by vendors hoping to provide DSM IC designers an easy, quick, and accurate method of dealing with the explosion of parasitic data that invariably occurs. Consequently, having the right parasitic-extraction tools has now become more critical than ever, leaving DSM designers to wonder, if the tools they have now can't do the job, then what will.



In deep submicron abstraction, context-based techniques can be used for 3D modeling. Art courtesy of Simplex Solutions Inc.

The issues that arise from design within a DSM environment and the reasons why they arise are relatively straightforward. At 0.5-µm and above, gate delays dominate over interconnect delays. The extent of parasitic extraction may be only on a few nodes and the information can, in fact, be an estimation. That is, the devices' resistive and capacitive effects can be viewed in terms of a lumped-RC model. These estimations are acceptable because the overall effects of the parasitics are small, and any resulting error between the lumped-RC model estimation and the true parasitic effects is trivial, causing no adverse affects to the design. Thus, multiple iterations let the design converge on itself to an answer.

Just the opposite is true, as the industry progresses to smaller geometries. At 0.35 µm the roles start to switch, and by 0.25-µm , the rift is evident, leaving current design methodologies to completely fall apart. Interconnect delays now dominate over gate delays, and the physics of the interactions between the device's components, such as metal layers, wires, and transistors, comes heavily into play. Consequently, designers can no longer estimate things like resistance or capacitance in terms of one lumped-RC model.

Roy McGuffin, president and CEO of Ultima

Interconnect Technology Inc., Cupertino, Calif., explains that "as geometries shrink into the 0.25-µm range, interconnect is the biggest challenge affecting circuits' performance and reliability, and accounts for as much as 70-80% of the overall performance. Typically RC interconnect delays are ignored or poorly approximated during design synthesis, and this results in designs that do not meet their performance goals." Instead, designers need very accurate values for the parasitics now affecting the design. What starts to become evident about design in the DSM area then is that success depends critically on two factors: Being able to extract good parasitics, and being able to accurately analyze the huge amounts of extracted data.

What complicates this situation more is that there's no easy migration path from today's design methodology to one that will work at 0.25 µm and below. Parasitic-extraction tools, which will play a central role in the development of new design methodologies have some maturity of use though, having been around for roughly five years. The most notable of these tools is Cadence's Dracula.

On the surface, it would seem easy enough to simply tweak current extraction tools to work in the DSM environment. In fact, many companies with existing tools are doing just that. But this process is not as easy as it sounds. Even startup companies dedicated to bringing extraction tools based on new technology to the market quickly have hit some pot holes. Part of the reason is that the whole issue of parasitic extraction in a DSM environment is so complicated. It's not, as some in the industry might like to believe, only a matter of choosing the right technology approach. It also involves being able to correctly implement that technology.

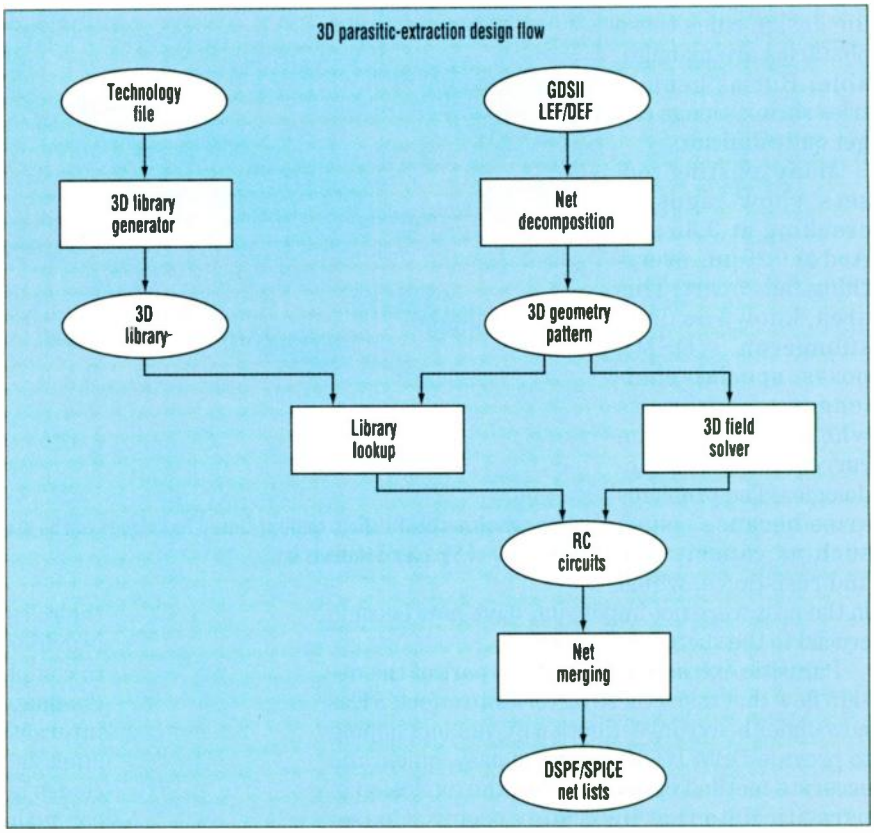
Designers and EDA tool vendors aren't used to dealing with the physics of parasitic interactions within a design. In fact, the interactions themselves are not always well understood. Try designing something when you're not sure what the design is, how it should work, and what it should look like. It's next to impossible.

Chi Won Low, a technology manager in Bell Labs quasi 3D development project Clover, explains, "In the past, people could live with a lumped-C model. At 0.35 µm, though, there is a turning point. For the first time, the metals cross-section becomes an issue because its width and height are equal. At 0.25 µm, the aspect ratio of height to width is 1:2, and the trend will continue. In the year 2010, the aspect ratio of 0.08-µm designs will be 1:4. The bottom line is that because of this, the lumped-C model won't work anymore. You just can't get it accurate enough. So, in the past where the designer had to worry about just one net, now that one net is broken up by resistors and capacitors. You, could, for example, now have ten resistors and/or capacitors for each net. And because you can no longer get an accurate, precalculated lumped-C value, the delay calculation is impacted, in effect, divorcing today's design methodology from reality."

To further complicate matters, in a DSM environment, capacitance is hard to extract and takes more time. On the other hand, chips are now bigger and more complex than before, so even if a machine runs faster it will still take more time to extract the parasitics. These two things don't make it any easier to shorten design cycles. One way to manage these delays is by first reducing the data. Consequently, all critical nets in a design can be identified, and then all parasitics can be extracted from these nets. Non-critical nets can then be dealt with using today's extraction methods.

Many technology approaches are bantered about to deal with critical-net parasitic extraction *(see "Deep-Submicron Extraction Techniques," p. 114).* And vendors seem to be lining up on both sides of the spectrum, either using the technology for implementation into modified versions of their current extraction tools, or using it in newly developed extraction toolsets.

While many of the companies frantically working to provide solid solutions in DSM parasitic extraction would argue about approaches and methodologies, most tend to agree on a few basic facts. One of the most important things that they all share is the belief that speed and accuracy are very closely linked, and that any successful tool will be able to empower the designer to trade-off how much



1. This flow chart details the steps involved in extracting parasitic information from a design using Ultima's newest tool offering—the Ultima-PE parasitic-extraction tool.

GALILEO™

Changing the world of FPGA design.

EXEMPLAR LOGIC, WITH ITS VISIONARY NEW GALILEO™ TOOL SUITE, DELIVERS ALL THE BENEFITS OF A HIGH-LEVEL DESIGN PARADIGM TO THE FPGA WORLD.

Today's complex FPGAs demand this complete, high-performance, standards-based environment for synthesis, simulation and timing verification.

COMPLETE HDL SYNTHESIS SUPPORT

Increase your design productivity and portability with our HDL Logic Explorer™ package, and gain Synopsys-compatible VHDL and Verilog language support.

BACK-ANNOTATED HDL SIMULATION

The industry's most popular VHDL simulator, V-System, is fully integrated with a complete back-annotated timing interface. V-System accelerates the Exemplar-provided, fully compliant VITAL libraries and VITAL netlists by up to 10X over non-accelerated versions.

EXPERT RESULTS OUT OF THE BOX

Galileo delivers the broadest FPGA device support with proven expert performance ***and*** ease of use. In fact, an independent benchmark shows first-time Exemplar users out-performing expert users on all other synthesis tools.

FULL TIMING VERIFICATION

Verify your design's timing constraints with Galileo's integrated timing modules: TimeScope™ the static timing analysis tool that lets you accurately evaluate post layout timing; and NetScope™ for easy schematic viewing of highlighted critical nets.

MAXIMUM DESIGN RE-USE

Take advantage of design reusability with our high-performance support libraries that automatically insert optimized, technology-specific implementations of high-level macros and operators.

EXEMPLAR LOGIC
An Antares Company
x'mpl'r

Call 1-800-861-FPGA or email: info@exemplar.com

http://www.exemplar.com

815 Atlantic Avenue, Suite 105 • Alameda, CA 94501-2274 • (510) 377-3700

READER SERVICE 175

time he wants the extraction process to take versus how accurate the results need to be. Of course, if a lot of accuracy is required, then the process will take longer than if the designer is willing to live with less accuracy.

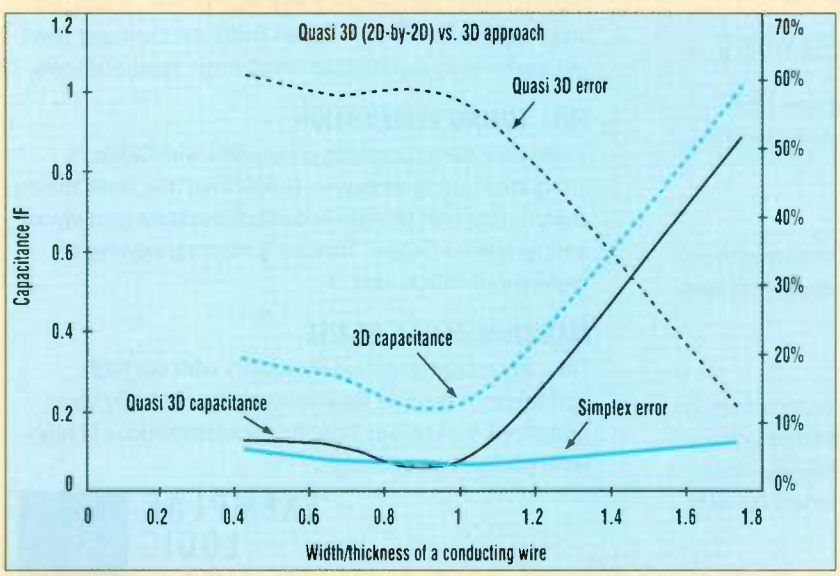
People also agree that net-by-net extraction in a design no longer works in DSM. Instead, the solution will require that different techniques be used to extract parasitics from critical versus non-critical nets. Regardless of whether or not a designer chooses to limit the amount of parasitic information from non-critical nets in a design, the virtual data explosion will still occur. The bottom line is that many designers are already working in a 0.35-µm design-geometry range, and 0.25 µm is just around the corner. These IC designers who will have no choice but to deal with the DSM issues are looking frantically to EDA-tool vendors to show them the right path and to deliver on a set of tools that will make DSM design possible.

SEMATECH, a non-profit R&D consortium of ten leading semiconductor companies, joined together to develop advanced software tools for chip parasitic extraction and signal-integrity verification. They've recently taken steps to address the issues associated with DSM design, effectively validating what many in the EDA industry have seen coming for quite a while—a major rift between what smaller geometry devices can potentially achieve in terms of performance and what current tools will allow to be designed. They've started the Chip Hierarchical Design System

Deep Submicron Extraction Techniques

The density of deep-submicron process technologies requires not only analysis of designed-in lumped electrical devices (transistors, precision resistors, diodes), but also the unintended distributed elements (resistance, capacitance, and inductance) in interconnect lines. Determining interconnect parasitics in a deep-submicron design requires two steps. The first step is process-technology characterization, as models or libraries, to construct estimates for the possible parasitics. The second is geometric full-chip extraction to determine the location of the parasitics and apply the models or libraries, then generate compliance reports or electrical networks for analysis.

Interconnect process characterization involves using field solvers to determine the magnitude of capacitance and resistance. Field solvers are calibrated with actual measurements on silicon. Field solvers discretize the layout structure in 3D (or 2D), and solve Laplace equations using finite element methods, finite difference, boundary element, random walk Monte Carlo, geometry-independent measured equation of invariance, and fast multipole methods. Because this type of analysis requires enormous compute time, it doesn't realistically scale to full-chip levels. To effectively handle full-chip extraction, designers need geometric layout extractors.



A. This graph, compiled by Simplex Solutions Inc., offers a comparison of error bounding 3D modeling versus the Quasi 3D approach.

Geometric layout extractors take three basic forms: Boolean, edge, or context-based. Boolean extractors analyze transistors and interconnect by applying Boolean operations to the polygon shapes of the design. The shapes are conditionally combined (OR, AND) to determine the distance between conductors and layers. Edge extractors identify the edges of transistors and interconnects by tracing the outer portions of the polygon shapes. In either case, rule-based extraction files are used to first identify the type of interconnect (lateral, area, fringing), and then apply the appropriate equation to calculate the capacitance. Boolean and edge-based approached are 2D (or 2D-by-2D).

For today's processes that contain six to seven metal layers and hundred of thousands of nets per chip, Boolean methods have a number of drawbacks. First, there's slow execution speed. The number of Boolean operations required to identify and capture all major parasitic components increases as conductor spacing decreases and additional layers are added. Also, complexity is a problem. Boolean rule files are definitionally complex and lengthy. Boolean operations in layout extraction are semantically limited to the identification of 2D structures. Lastly, pattern-dependence is a drawback. Capacitances are defined as a measure of identified

(CHDS) program, which is expected to culminate in the development of tools to speed submicron chips to market. Greg Ledenbach, SEMATECH 's director of design says, "Our aim is to establish a new Chip Hierarchical Design System that will enable our partners, and ultimately the entire industry, to have the open, standards-based tools and information to accelerate the speed of bringing products to market." In effect, this will allow end users to design chips with up to 28 million transistors. The CHDS program came about in response to the Semiconductor Industry Association (SIA) roadmap that highlighted a number of real show stoppers for the design-automation industry as it moves toward smaller and smaller geometries. With the number of transistors per chip growing at 21% per year, current design methods will soon reach a breaking point. As a result, three contracts were issued in 1996 specifically targeted at timing-driven design, standards for various interfaces, and on-chip parasitic extraction and signal integrity to get at physical parameters in a design. The last part of the program, focused on PE, was won by Bell Labs, a division of Lucent Technology, Murray Hill, N.J. This multimillion dollar, three-year contract headed by Bell Labs also will include efforts by OEA International Inc., Santa Clara, Calif., and Ultima Interconnect Technology Inc., Cupertino, Calif. Bell Labs' role as the prime contractor, will be to develop chip parasitic-extraction and signal-integrity verification tools for 0.25-µm designs, with a roadmap to 0.18-µm geometries. Deliverables of the contract will include a net parasitic-extraction tool based on the company's widely recognized Clover tool suite for layout extraction and verification.

One of the tool's benefits is its use of an internally developed, patented PVL algorithm for solving differential equations., a powerful mathematical function that takes huge amounts of interconnect net data and reduces it to a number that will give the end user the accuracy desired at the fastest speed possible. The critical nets can then be handed over to, for example, tools from OEA, which would do a careful modeling.

Bell Labs also has been charged with specifying and developing interconnect and compact electrical models to be used in the CHDS system, as well as a standard net interface with OEA's 3D NET-AN field solver integrated for high-accuracy parasitic extraction and Ultima's fast critical-net 3D extractor. The resulting CHDS tool will be made available to SEMATECH members, who will beta site the tools as early as the fall of 1997. Worldwide EDA users will get their opportunity around 1998.

Of the two subcontractors, OEA is best known for its accurate 3D solvers and power-analysis solutions, while Ultima's claim to fame is fast, yet not as accurate, critical net 3D extraction. OEA's contribution to the CHDS program will be in providing enhancements to its chip parasitic-extraction and signal-integrity verification (CPR&SIV) tools. The company will be working on a new technology evaluation tool with a variable accuracy whereby users can specify higher accuracy for the most critical nets, signal-integrity checks, process variables errors

patterns on a layer that doesn't account for multibody capacitance, a frequent occurrence in deep-submicron technology.

Recent approaches take cross sections of 2D geometries and construct a quasi-3D (or 2D-by-2D) view of interconnect *(see the figure)*. These quasi-3D profiles are stored in libraries along with their capacitances. During extraction, the patterns of interconnect are matched to the library patterns to calculate net parasitics. This approach suffers from aggregation errors that occur when the library elements are pieced together. If a match to structure is not found, then the process may revert to a 2D field solution producing disappointing run times.

Edge extractors are more efficient than Boolean methods, however, they still require an ever-expanding command set to identify the complex interconnect structures. Most edge extractors can't efficiently account for the third dimension of interconnect. Neglecting the third dimension seriously limits the predictability needed to bound the error of the results. Without error predictability, designers must increase guardbanding.

The newest extractors, like Fire & Ice from Simplex Solutions, are context-based. Context-based parasitic extractors look at each conductor in its natural three-dimensional surroundings and store both the transistor and connectivity of the physical design in specialized geographical data structures. These structures are optimized for fast range query operations so that the polygons can be quickly traversed to identify all the surrounding nearbody conductors.

The context-based technique is faster than the rule-based approaches because it identifies all types of capacitors at any given conductor in one data-structure lookup. The context-based method stores and retrieves information on all surrounding conductors without user elaboration of edge-detection rules or exercising Boolean operations.

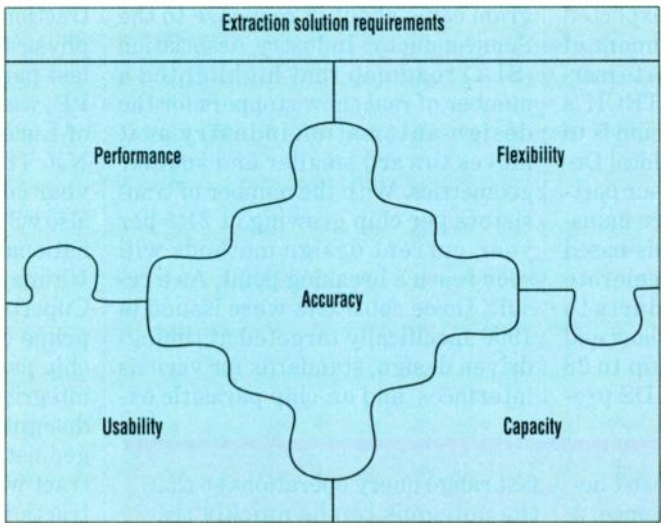
In the context-based technique, a halo region around each conductor of interest outlines the boundary of influence related to all other nearbody conductors *(see opening illustration)*. Once a capacitor is identified, the effect of the nearby conductors is accounted for in its total capacitance value. The range of the halo region and implementation issues are the only limitations on the accuracy of this method.

Context-based extraction is ideal for enhanced 3D models constructed from process information and field solvers. Three-dimensional analytical models bound the error in full-chip extraction to within 10%. This kind of accuracy gives full-chip timing and noise-analysis tools the appropriate information to enable designers of deep-submicron ICs to prototype electrical behavior before chip manufacturing.

Contributed by Shashank Goel, vice-president of verification products for Simplex Solutions Inc San Jose, Calif.

estimated, and with special net handling for power and clock nets. This tool will help IC designers make critical decisions in the entire deep-submicron process.

OEA's current field-simulator offering, the NET-AN 3D critical-net field solver, based on the internally developed Cheetah field solver, provides the end user seamless full-net extraction in an IC design. It works by reading a GDSII database and other information on a critical net. It then selects a set of nets and begins to build a 3D model. Following a full 3D field simulation, the output is in the form of a fully distributed RCL Spice subcircuit on the net. As part of the companies contract, expect to see many tool enhancements, including the addition of multi-net capability, an all-net extractor, and speed upgrades.



2. According to CADENCE, solving the parasitic-extraction issue brought about by the migration to smaller geometries is like fitting together all the pieces of a puzzle. Each puzzle piece must play an equally important role in order to offer the designer maximum flexibility.

Ultima's Roy McGuffinsays that DSM brings up some big problems. "Because of the amount of parasitics that must be extracted, you end up with a data explosion. So, when you try to simulate, the simulator dies. And, of course, it used to be that the designer could live with design inaccuracy, but now in DSM you can't because interconnect delays play such an important role in the design."

To address this issue, the company offers Ultima-PR, a parasitic-reduction tool that reduces the data file while maintaining accuracy. In addition, Ultima also developed the Ultima-DC delay calculator that solves for cell-interconnect dependency using a patent-pending proprietary model to drive the cells, and then take this data into account when calculating delays. Ultima-PR reduces extracted parasitic data to decrease the computational and storage burden of IC simulators with typically less than 1% accuracy loss, while Ultima-DC computes cell and interconnect delays for DSM IC designs.

Ultima's newest development is the Ultima-PE, a parasitic-extraction tool based on its 3D critical-net extraction technology that will fit into the existing design flows of Cadence, Epic, and Lucent *(Fig. 1)*. Ultima's approach to extraction is to take the nets and break them down into 3D cubes, generating a representation library of components that totals roughly 200 3D structures for each process. Closed-form lookup tables can then be used to match the values in libraries, providing extraction times similar to 2D-based solutions. Relying on technology that's similar to Chaco or partitioning algorithms where a complex problem is broken into smaller more easily solvable problems—and when recommended provides one solution more accurate then the sum of its parts, Ultima decomposes the nets and recombines them to minimize the boundary effects.

Ultima-PE incorporates a usage model to augment its rules-based extraction by allowing the results to identify critical nets to be extracted by Ultima-PR. Also, the net-based PE tool uses the high-performance GIMEI 3D solver, which gives results comparable to other solvers but 30-50 times faster than industry standards. The tool also has a re-meshing algorithm that provides solutions based on time or accuracy requirements.

For many EDA-tool vendors, parasitic-extraction tools are not new. Cadence, San Jose, Calif., has had its Dracula PE tool on the market for the past five years. And it has performed quite well. With DSM issues starting to come into play, though, the company has had to rethink its tool offering. While many in the industry feel that Dracula will still play a role, perhaps in the extraction of non-critical nets, ultimately it will be the companies' response to the extraction of critical nets that will be its defining factor. To that end, the company plans to make a major tool announcement later this year. While details are being kept quiet, the company does offer its understanding of what type of solution will be needed to address parasitic extraction in the DSM area.

Bernie Mills, Cadence spokesperson, explains that "parasitic extraction is part of the whole timing/interconnect problem, as well as an issue of capacitance. Our previous extraction tools provided solutions at the 2D level. But, for DSM, new models are needed. The tools need to become more sophisticated, such as with a 3D formula-based approach that takes a look at the multibody effects of capacitance. New technology development will be centered around this approach." Cadence differentiates its 3D formula-based approach from the more generic 3D method in that it uses 3D numeric solvers working on very small structures. Information obtained from these structures can then be used as input for a field solver. According to Cadence, "full chip 3D is unreasonable, because most field solvers, including 3D numeric field solvers, are prohibitively slow." Cadence though, is looking at taking the numeric approach and making it real-world applicable to generate coefficients for the rest of the extraction process.

Cadence has taken the position that how good a parasitic-extraction tool for DSM design is will be not just a measure of how much data it can handle, but how accurate the data is and whether or not it will have the capability to give the designer answers as to whether the chip will work or not. Tool usability and the ability of a tool to provide consistent answers is tops on the list of user priorities *(Fig. 2)*. To that end, the upcoming announcement promises delivery of a tool that will combine reduction technology coupled with extraction data.

In this manner, the designer has the flexibility to do either full-chip extraction or critical-path extraction. In addition, it will focus on an overall timing solution (does the entire chip meet timing requirements?).

Mentor Graphics, San Jose, Calif., another company offering parasitic-extraction capabilities as part of its Calibre toolset, like Cadence, plans to announce this year a parasitic-extraction tool for DSM design. Mentor, with much of its focus on system design and verification, is sure to bring to the table a tool that willbridge the gap between physical and implementation domains of a traditional design flow, creating an interface that will shrink overall cycle time.

Avant!, Sunnyvale, Calif., also has given a lot of thought to the need for new parasitic-extraction tools for use in DSM design. To that end, the company has developed a technology known as full-chip smart extraction. Using this simulation-based extraction technology, the designer has the ability, at any stage in the extraction process, to specify a desired delay accuracy. Smart extraction then automatically optimizes computer resource requirements to provide this accuracy. One of the prime benefits of this technique is that it significantly decreases computer runtimes and peak memory requirements by up to ten times that of full-chip extraction without the use of smart extraction technology. Other features that set this technology apart from other extraction techniques is its ability to enable delay-based sensitivity analysis to determine the level of RC detail required for each net and intelligent limiting of extraction detail to create a circuit file of useable size while still providing the delay accuracy of an exhaustive full-chip RC extraction.

The company's tool offering, StarR version 2.0, is based on the smart-extraction technology and is designed to seamlessly integrate into existing CAD environments by interacting with a host of industry-standard formats and interfaces *(Fig. 3)*. It can extract parasitic information and delays to within 5% of actual chip implementation, and analyze designs with more than 20 million transistors. The tool relies on the use of 3D field-solver process-simulation tools to automatically generate capacitance models. These extraction models can then be matched with actual silicon processes using a silicon-characterization and model-calibration service.

Another company well known for its extraction tool, Arcadia, is Epic Design Automation, San Jose, Calif. They are not just thinking about the issues brought up by DSM design in the next couple of years, but to the year 2000 and beyond. As the company puts it, getting nanometer ready. Says Les Speruiell, director of technology marketing, "in the past, designers could completely ignore the analog effects of design, which is why digital has taken off. But, at the 0.25-µm mark, silicon begins to rear its ugly head and says, "You can't ignore me anymore!" The result is that the designer has to pay more attention to the interconnect and not the design. The big question is how can the designer design in this way and still get the product to market quickly?

Toward that end, Epic sees hierarchy and the ability to manage data as chunks of hierarchy, as being a crucial part of the overall DSM solution tools. This not only helps designers do parasitic-extraction estimations very early in the design, but also makes it easier to bring back-end features to the front of the design cycle. Effectively, it's not necessarily the technology that will need to change to address many of the issues being raised by DSM design, but rather the technology implementation. The Arcadia tool, in keeping with this train of thought, offers four different tradeoffs of accuracy-versus-speed, giving the designer flexibility to choose the appropriate level.. Les adds that "the Arcadia tool is not in bad shape, but in the future some improvements will need to be made to bring up its capacity and performance."

Simplex Solutions Inc., San Jose, Calif., has a mission to make deep-submicron semiconductor technology accessible to the mainstream community of IC designers. The company takes its strength from looking at the whole picture: timing, signal integrity, and IR, as opposed to the rest of industry which is looking at pieces. These strengths are reflected in the company's tool offering for parasitic extraction. The tool, Fire and Ice, began shipping last October and has a two-part flow. According to Shashank Goel, vice-president of verification products, "The first part is T-Cad, a fast 3D analysis whose output is a set of adaptive models developed from the analysis of the device structures that are used in the extraction. The second part is physical data understanding of interconnects." In effect, the company offers not only the technology, but also a method of implementation that gives speed, accuracy, full-chip verification, full-chip capacitance extraction, and IR extraction. The tool uses standard formats and fits into existing design flows.

Bill McCaffrey, technical marketing director for High Level Design Systems, San Jose, Calif., says that "the synthesis process is part of a highly iterative deep-submicron design flow where rapid feedback of highly accurate parasitic extraction, parasitic reduction, and delay-calculation information is required. These tools need to give feedback in hours rather than days in order for deep-submicron designers to meet aggressive chip performance targets and design schedules."

HLDS' solution directly answers these concerns through the integration of solver-based technology to properly model parasitic effects. It not only features next-generation extraction that handles the increased design sizes and complexity of deep-submicron designs while providing very fast runtimes, but also provides designers with quick iterations between the logic and layout phases.

Compass Design Automation, San Jose, Calif., has a unique take on the whole issue of parasitic extraction. According to Steve Compolt, "Part of the problem with DSM is this issue of data explosion. Compass says just don't create the data explosion in the first place. To do this we have a two-fold approach: characterization of the transistors and characterization of the parasitics. Some people believe that you have to do both of these all at once and this creates the data explosion. So, you either deal with a capacity explosion problem or an inaccuracy problem. To deal with the inaccuracy problem people go to 3D. But, here again, you get a data-explosion problem. The real test is silicon correlation. This is why Compass takes a two-prong approach."

The company offers several extraction tools: Silicon Navigator, which has Extract 2 with a source-drain resistance option; Interconnect Extract; and Extract 2. Extract 2 has many features, including hierarchical short checking, overlap extraction, fringe and lateral capacitance, the extraction of inter-layer contact resistance through area/resistance lookup tables, and extended layer derivation that's enhanced to handle an unlimited number of layers. The company also offers the Phantom extract tool that extracts cell-interconnect parasitic information to within 1% of Spice. As Compolt explains, "The company's real differentiation is that it has real silicon test chips to validate the whole extraction process, and the extraction tools fit into existing design flows."

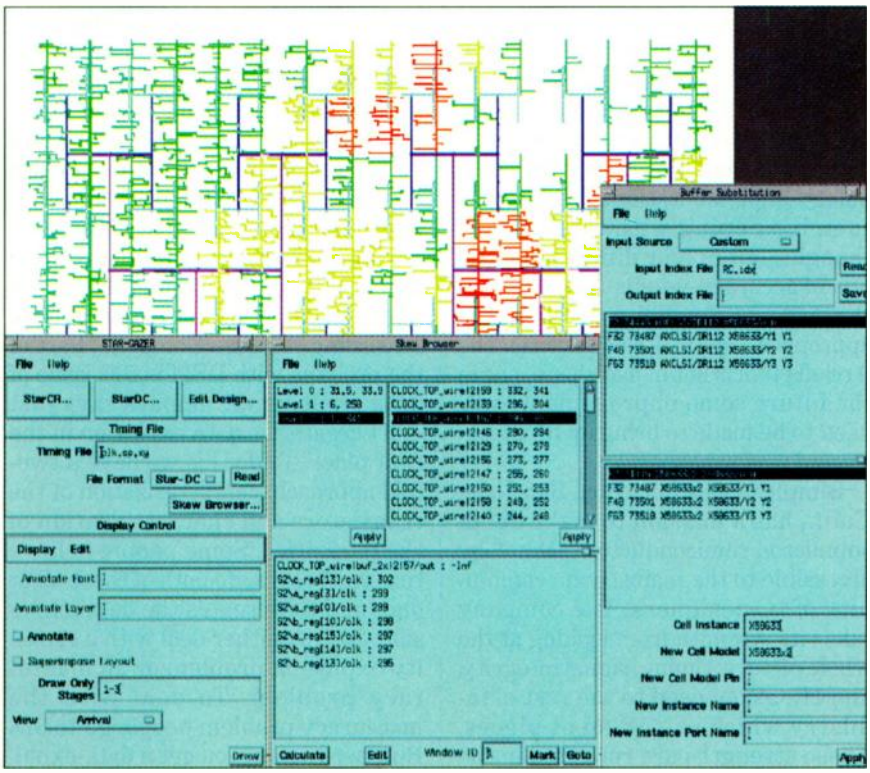
While a handful of EDA vendors struggle to find ways to handle parasitic effects of DSM design, other EDA software vendors are trying to figure out how to put these developments in the hands of IC designers quickly. According to Bruce Yanagida, director of the Design Tool Department at Cascade Design Automation, Bellevue, Wash., "Today, more than ever, with tools depending on the accuracy of the parasitic-extraction technology, is has become vitally important to be able to offer this technology to mainstream IC designers. Part of the problem though, is how to make the tools available. After all, academically developed technology and reality are two very different things, and if you can't implement the technology then what good is it?"

With this in mind, the company opted to partner with somone whose parasitic-extraction tools have received rave reviews rather than start at ground zero and develop PE technology from scratch. Its choice, the Arcadia tool from Epic Design Technology, seamlessly interfaced to Cascade's Epoch 8.0 Seamless Physical Design environment. Aradia's RC-extraction technology is actually embedded into the Cascade design environment, making it virtually invisible to the designer. The extraction technology enables highly accurate full-chip capacitance analysis, as well as net-by-net RC parasitic extraction including area, fringe, and coupling effects.

Extracted information using Epic technology is comparable to that from a full 3D field solve. But extraction time is considerably less. And, because the technology is embedded , IC designers are provided a push-button solution to extract critical paths using static timing-analysis tools, instead of examining parasitics on a net-by-net basis before putting information into a database for analysis. This embeddedapproach holds benefits for the mainstream designer as well, because it assumes that the company, not the designer, will try to understand how extraction technology works, how it can be used, and how it's applied. Bruce explains "Cascade sees mainstream designers today coming up against many of the so-called DSM issues, and we feel the solution we provide is adequate today to deal with these issues, as well as those that may arise in the next year with nothing more than some improvements to the accuracy of the extracted data."

Also taking this lead is Silicon Valley Research Inc., San Jose, Calif. Exclusively licensed to distribute the parasitic-extraction technology as packaged in the Clover tool developed by Bell Labs, it hopes to secure its position as an IC-design-tool provider for design in a DSM environment. As Cascade and SVR illustrate, key to successful DSM design is for mainstream designers to have a set of easily accessible and easily useable tools.

While most of the attention is focused on changing design methodologies in a DSM environment, IC designers will have at their disposal a variety of parasitic extraction tools to choose from. But, Shashank Goel relates that "with the issue of dealing with parasitic extraction of resistance and capacitance well underway, five years from now we can expect to see similar difficulties, only this time the issue will be inductance." SEMATECH is sponsoring a study on present and potential needs for modeling on-chip parasitic inductance for complex custom ICs. The study will be done by OEA as part of SEMATECH's CHDS program.



3. AVANT!'S parasitic-extraction product, called Star-R, is based on the patent-pending smart-extraction technology. Its high accuracy helps designers reduce costly iterations due to undetected timing problems common in deep-submicron IC designs.

How Valuable	Circle
Highly	553
Moderately	554
Slightly	555

EDA WATCH

Deep-Submicron Design—Changing The Landscape Of Design Automation

The world of Electronic Design Automation (EDA), or as some refer to it, Electronic Systems Design Automation (ESDA), is in the midst of tremendous upheaval. In the past, EDA companies existed in their own little worlds, content to carve out specific niches. But now, due to changing circumstances, they're getting involved in all areas of the design-automation process. The traditional design paradigms are starting to break down as geometries get smaller; completely breaking apart at 0.25 µm. This rift occurs in current design methodologies, which no longer are driven by gate delays. At 0.25 µm, interconnect delays now drive gate delays, and the physics of the components start to break apart, making modeling a non-trivial task at best.

The consequences of this design disparity has sent many companies scrambling to carve out a path for themselves for deep-submicron design (DSM) solutions. Toward that goal, two factions have evolved: Those companies heralding the all-in-one solution, and those opting for the open platform otherwise known as the "best-of-class point-tool solution."

The first approach focuses on providing one-stop shopping to the EDA end user. It requires that all interfaces between tools be seamless, that no translation of data be required, and that the end user be able to work in the same environment throughout the entire design cycle. MicroSim recently introduced a tool that accentuates the all-in-one approach. DesignLab not only provides support for analog and digital designs, but FPGAs as well. Fostering interoperability and completely seamless integration, it is reasonably priced at $13,500 in the U.S. Its benefits include a faster design cycle, easy movement from one function to another, fewer operation errors, and forward and backward concurrent access to all facets of the design cycle.

In keeping with the all-in-one design solution, it holds the promise of helping designers build better circuits, which according to MicroSim, will "drive change, setting the standard for what people end users will begin to expect from companies in the coming years." The company also claims that working with a product that is part of an integrated family of products gives the designer access to all facets of design. Consequently, if the designer gets to a point where a problem arises, it is possible to easily go back and fix it. The designer also can trade off different facets of the design; a function not available in the past with assembly line trade-offs.

On the other end of the spectrum is the approach offered by Protel, deemed an "EDA renegade." Motivated by the knowledge that one solution may not be a perfect fit for every conceivable design scenario, it began work three years ago on an open platform of tools known as the EDA Client. Available for roughly 15 months, the platform is heavily modeled after the current client server, multivendor, multiapplication, multitool platform. Specifically addressing the inability of point tools to work well together, it offers a user-friendly interface and eliminates integration gridlock. The platform, which allows small vendor startup companies to bring their EDA technology to the market quicker, radically changes the EDA tool delivery model. A vendor simply uses Protel's free development software to design its technology into a tool for the EDA Client platform. The platform then becomes like a software factory, where the designers can easily and quickly pick and choose the best tool for the job, capturing expertise in all areas of design from schematic capture, and simulation to pc-board layout, all within the same virtual design environment.

The open-platform approach enables the designer to gain quick access to new technology because the time to get new tools to the market is dramatically decreased. In fact, no contracts or nondisclosures are required to be signed. But, while the approach may sound palatable—a number of companies have already designed tools for the EDA Client platform—it remains to be seen whether or not it will be widely adopted. Likewise, the all-in-one method is not a bed of roses either. Although it offers many benefits, many questions remain unanswered. For example, how can one set of tools work well in every situation? And, assuming one set of tools can work in every design scenario, what happens when shrinking geometries begin to cause a breakdown in the current design methodology? Does the entire tool set have to change or just get modified to address the different obstacles? And ultimately, by what criteria can the designer decide which all-in-one solution is the best?

Some companies smartly anticipated the coming changes to design methodologies that DSM will bring, and have begun seeking out ways to improve their current product offerings. For some, in-house development is the answer. For others, the solution is to look outside their corporate structure. In fact, many of the acquisitions, mergers, and partnerships over the past year have been in direct response to these coming changes.

Avant!, for example, has seen much activity lately, acquiring companies with technologies specifically targeted at design in the DSM environment, and carving out a leadership position in the Integrated Circuit Design Automation (ICDA) arena. The ArcSys merger focused on place and route, floorplaning, and optimization, while the ISS deal targeted verification and extraction. Most recently, the mergers with Anagram and Meta-Software sought to target high-capacity circuit simulation, timing and power analysis, and accurate circuit simulation, circuit characterization, and process modeling, respectively.

Cadence recently acquired Cooper and Chyan Technology (CCT) and High Level Design Systems (HLDS). The CCT deal secures ownership of the most widely used autorouter, and picks up all of CCT's recent activity. Last year, CCT acquired Unicad, a supplier of pc-board electrical integrity, analysis, and optimization tools, and entered into a long-term agreement with Synopsys and IBM to help Sematech solve the challenge of designing chips with geometries of 0.25 µm and below. The HDLS merger specifically targets floor planning,

considered by some an issue crucial to a successful DSM design. As Intellectual Property (IP) comes of age and ASICs start to look like pc boards, system planning will get more critical.

Mentor Graphics has positioned itself to offer a key all-in-one solution for DSM designs. It acquired Royal Digital with its Sceptor technology to help tightly integrate the transfer of designs from pc-boardCAD tools to fabrication suppliers; and Interconnectix with interconnect synthesis to enable first-pass success by addressing interconnect problems caused by increasing percentage of critical nets in a design. Mentor Graphics formed a strategic business unit, Inventra, to deal with all aspects of the emerging IP. As part of this formation, the company acquired dQdt (Dimension in Quick Design Turnaround), a supplier of parameterized DSP soft cores and design services; CAE Technology, a developer of reusable soft cores for peripheral controllers; and Systolic Technology Ltd., a developer of reusable cores for telecommunications. The new unit will try to offer the largest variety of synthesizable, system-level building blocks (soft cores).

Viewlogic Systems recently teamed with Applied Microsystems and Eagle Design Automation to offer embedded system and ASIC development teams a complete hardware/software co-verification solution, and with Motorola to develop a next-generation ASIC design methodology to unify logical and physical design. An arrangement with Synopsys will enable a significant reduction in the time needed to create, distribute and support accurate, secure Verilog simulation models.

While not a full accounting of all the recent activity in the EDA community, these mergers, acquisitions, and partnerships show the great state of flux the EDA industry is in, and the extent to which vendors will go to strike a leadership position into the uncharted DSM design territory . This year may very well determine which approach will come out on top—the all-in-one or the open platform. Ultimately, the winning approach will surely be the one that puts the designer's needs first in the design-methodology flow, and not just those of the technology, simply for the sake of implementing it in a design.

CHERYL AJLUNI

System-Level Tool Upgrades For Team-Based Design

High-Level Systems Design Tool Offers Design-Team Management, Automated Optimization, And Virtual Troubleshooting/Debugging Capabilities.

CHERYL AJLUNI

These days, designing complex electronic systems is becoming more common than designing a single electronic function or system. But this requires a slew of new design capabilities for use early on in the design cycle. And even with these new capabilities in place, systems design can be a daunting task. In the past, design teams could work effectively in isolation simply by throwing their completed portion of the design over the wall to the next engineer. But the complexity of today's projects is forcing companies to use larger engineering teams to meet their goals, which means that designers can no longer work in serial fashion.

A parallel design flow requires keeping track of every team member's activity, and this is no easy task. And adding to the problem, ASICs are starting to look more like pc boards as geometries continue to shrink, making the use of intellectual property (IP) crucial. Systems designers and project managers who are finding it difficult to effectively design and manage large, complex systems by today's standards are left to ponder their options in an IP-prevalent, deep-submicron world.

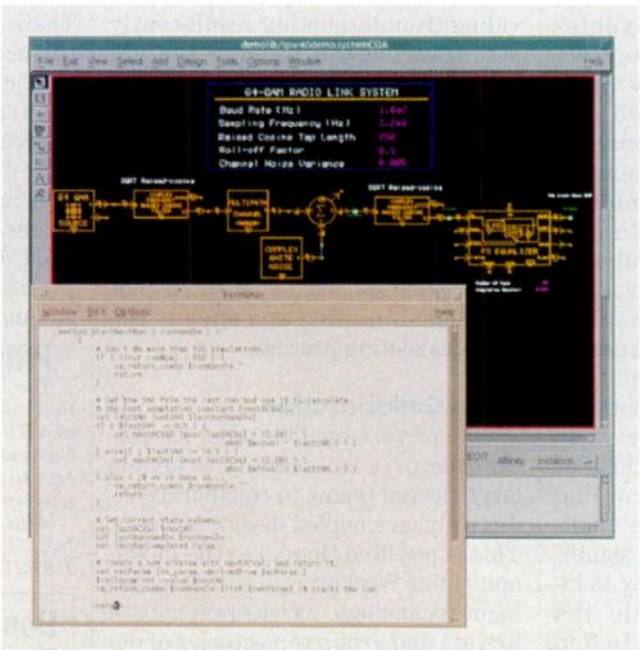
To address the growing requirements of systems designers and engineering managers, many electronic-design-automation companies have chosen to focus on what their next product offering will be. However, Alta Group, Sunnyvale, Calif., has opted for another route—they improved upon its existing SPW system design tool. Traditionally focused on individual-system design productivity for wireless, multimedia, and networking product design, the algorithmic-based tool enables designers to quickly evaluate and optimize alternative design ideas before committing to an implementation path.

Joining Forces

In light of the problems facing today's engineering managers, though, the tool has now been extended to focus on engineering collaboration for system-level design, with special emphasis on tool usability and design-team productivity. This move not only helps simplify the design of complex electronic systems, but with the inclusion of three key technology developments will, as Gary Smith, EDA analyst at Dataquest explains, "allow system-level design tools to move out of the lab and into the main design flow."

Version 4.0 of the SPW tool offers a number of benefits not previously possible. In the past, for example, system-level design tools have lacked the functional capability to allow for team collaboration or concurrent engineering across large cross-functional engineering teams. One prime benefit of SPW 4.0, however, is that it lets engineers from multiple disciplines, such as system architects, hardware and software engineers, and RF engineers, work together concurrently in system design. Subsequently, there's much less risk of getting caught at the back end of a design with an integration problem that could have been avoided by dealing with it much earlier in the design cycle.

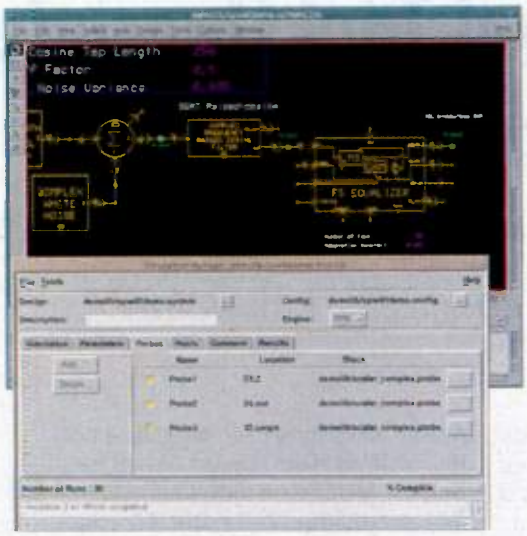
Time-to-market also is improved because the tool allows for automatic design-parameter optimization and rapid system integration. Both functions were previously unheard-of for main product design flows. Engineering managers, who in the past may have had difficulty keeping track of one project with a small number of design-team members, can now use SPW 4.0 to manage many different designs and revisions of designs at the same time. And they get the same result: A fully verified system-level design that can be handed off an to IC design-implementation group. Key enablers of these benefits are three technology developments featured within the SPW 4.0 tool. The first, called Intelligent Design Optimization (IDO), pro-



1. Intelligent Design Optimization allows systems designers to do optimization trade-offs by automatically and intelligently running sequences of simulations.

vides a means for the designer to identify the optimal combination of design parameters, even when faced with thousands of possible choices *(Fig. 1)*.

In the past, this highly iterative process would have been done by brute force, whereby designers were forced to evaluate and optimize designs manually and repetitively. With IDO, designers simply enter script in TCL/TK format to direct a simulation run. Accordingly, system-design parameters can be swept across ranges of values that are either defined by the designer or determined dynamically during the sequence of simulations. Then, with each subsequent simulation iteration, parameter values can be varied according to results obtained from the previous simulation. In this manner, the software is able to intelligently and automatically process complex sequences of simulations based on previous knowledge, not brute force.



2. The Interactive Virtual Prototyping feature simplifies and speeds the entire troubleshooting/debugging process by enabling real-time data probe collection and analysis.

Integrate And Debug

Interactive Virtual Prototyping (IVP), another feature of SPW 4.0, enables designers to rapidly integrate and debug complex system designs *(Fig. 2)*. It does this by virtually eliminating the need for batch-mode simulation, normally a tedious, costly and time-consuming prospect. Instead, using an interactive probing feature built into IVP, the designer can stop a simulation run at any point, and hook up various collection and analysis probes to any node in a system block diagram. Then, by resuming the simulation, and even running it in slow motion if desired, designers can effectively verify that everything is working at the critical system nodes according to plan. They can even do troubleshooting on the fly. This is significant because having the ability to investigate a problem while it's occurring enables designers to find out about any potential "show-stoppers" early in the design cycle, when there is still plenty of time to make necessary changes.

Unfortunately, the alternative would be to wait until a prototype of the design has been completed before any problems can be identified. At this point, troubleshooting is much more difficult and expensive. And today's complex systems design doesn't provide the flexibility in terms of time and project budget to accommodate this outdated option. IVP eliminates this practice by providing troubleshooting results early in the design cycle, when there's still time to make cost-effective changes. Once a problem is identified, SPW's interactive debugger lets designers set breakpoints, pause/step/resume simulations, highlight blocks where the simulation is halted, and display/modify signal values at currently active nodes. The result is that the tool simplifies and speeds the troubleshooting process.

Team Collaboration

One of version 4.0's most significant features is its ability to enable large design teams to collaborate effectively on complex design projects. This is possible thanks to the development of Workgroup/Data Management technology, which creates both private and group repositories of design data that are similar to read-only file folders. Control of access and modification privileges to these repositories can be determined by the engineering manager or among the members of a design team. This feature works directly to bridge the organizational gap, by mandating that everyone working on the project stays on the same track and that the project stays on schedule. Consequently, system-level designers and managers can control to varying degrees the design team members, the design project, and the design version.

Other capabilities offered by the Workgroup/Data Management software technology include the ability to view the status and history of current design revisions, and track data object modifications by other team members. Data-branch creation and merging, an advanced technique that enables members of a design team to independently modify system components, track changes, and subsequently reconcile them, and design-build management also are possible with this software.

In addition to the three key software developments, SPW 4.0 also has a number of other benefits. These include a network/protocol interface, processing control simulation, cycle-based simulation, cycle-accurate processor models, and static/dynamic data-flow simulation. Other features promise ease-of-use, such as design capture via block diagrams, finite state machines (FSMs), and C/C++ coding. Users also will enjoy fast, system-level simulation and advanced analysis capabilities.

PRICING AND AVAILABILITY

The SPW 4.0 tool will be available in the first quarter of 1997 on the SunOS, Solaris, and HP platforms. Pricing starts at $30,000. Current users of the SPW tool will have access to the new release under the maintenance program at no added cost.

Alta Group of Cadence Design Systems Inc., 555 N. Mathilda Ave., Sunnyvale, CA, 94086; (408) 733-1595. **CIRCLE 504**

How Valuable	Circle
Highly	546
Moderately	547
Slightly	548

Fast. Reliable. Affordable.

Needham's Device Programmers

Now the easiest and most cost-effective way to read, program and verify 2716 – 8 megabit EPROMS. Support for Micros, Flash, EPROM, 16-bit, PLDs, and Mach (call for support list for specific models, or download demos from our BBS or web site).

Easy to use menu driven software features on-line help, and a full-screen editor. Support for macros, read and save to disk, and split and set options.

For more information call

(916) 924-8037

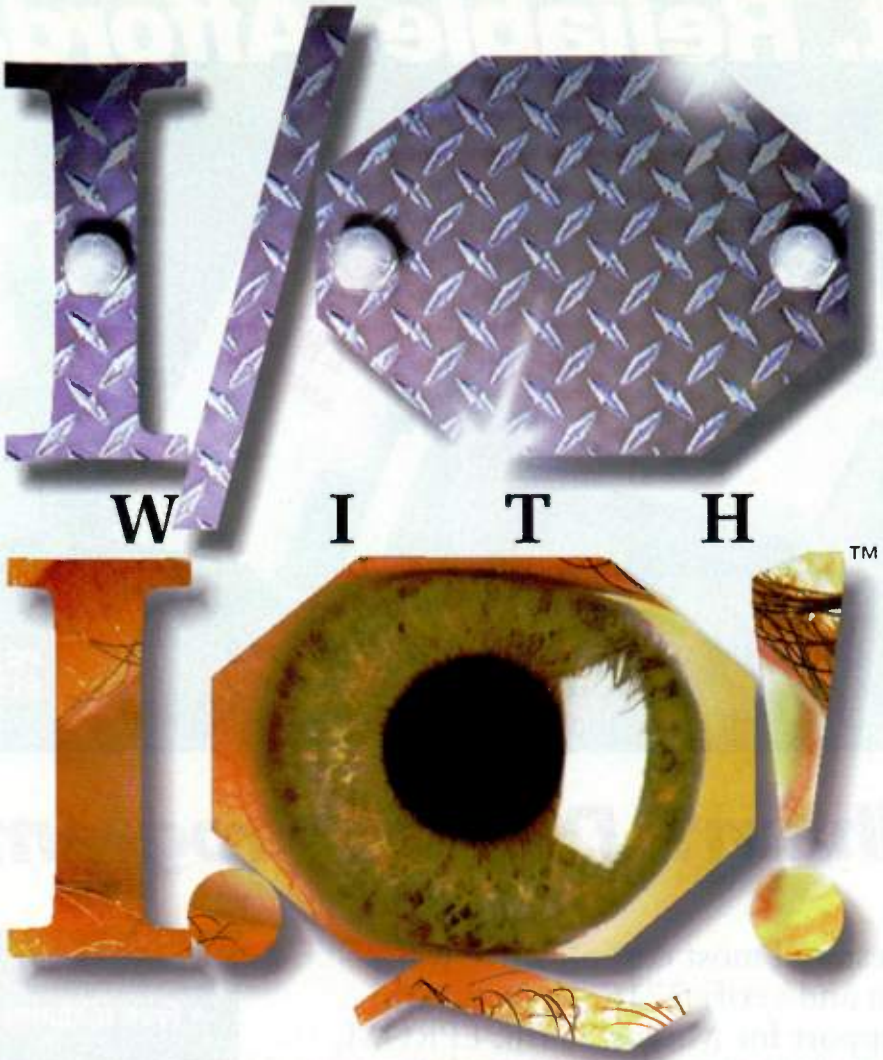
- **Free technical support**
- **Free software upgrades**
- **1 to 2 year warranty on all parts and labor**
- **30-day money-back guarantee**
- **Made in the U.S.A.**
- **All models include software, on-line help, cables, and power transformers (where applicable)**

NEEDHAM ELECTRONICS, INC.
4630 Beloit Drive, #20, Sacramento, CA 95838
FAX (916) 924-8065 • BBS (916) 924-8094
(Mon. – Fri. 8 am – 5 pm, PST)
http://www.needhams.com/

MasterCard VISA

CE

READER SERVICE 179



Palm-sized PC Microcontroller packs industrial I/O power with embedded PC control.

When a proven technological innovator emerges in any industry, it becomes the one to watch. Octagon Systems' new PC Microcontroller™ series blends I/O innovation with embedded PC control. The PC Microcontroller series not only provides a uniquely integrated hardware platform, but includes the industry's largest suite of embedded software in flash memory. You get the best of all worlds–a single card industrial solution that you can adapt to hundreds of applications without the compatibility problems of multiple card variations. Each of the Octagon PC Microcontroller cards includes DOS 6.22, but will run under QNX as well as many other popular real-time operating systems. They also include CAMBASIC, Octagon's fast multitasking control language that supports all the I/O on the card–no drivers to write. Each 4.9"x 4.5" package is rated from -40° to 85°C, plugs into an ISA bus slot or operates stand-alone with a 5V supply.

Octagon PC Microcontroller Series

CPU	40 MHz
Parallel Port	IEEE1284
Digital I/O	17-65 lines
COM Ports	2-4
Analog I/O	Up to 10
CAMBASIC	✔
Networking	✔
Diagnostics	✔
Flash File	✔
DRAM Supplied	2 MB
Flash Supplied	1 MB
SRAM Supplied	128K
Real Time Clock	✔
KBD/Speaker	✔
Prices Start at	$340/100s

The Octagon PC Microcontroller series. It's loaded with software. There's no memory to buy. You don't need a professional programmer. And it eliminates the headaches of mixing and matching the CPU, I/O and software from different sources. It's an irresistible new product family from Octagon Systems–I.O. with I.Q!–the latest innovation in our sixteen year history of success.

OCTAGON SYSTEMS®
6510 West 91st Avenue Westminster, CO 80030 USA
TEL: 303-430-1500 FAX: 303-426-8126 www.octa.com

READER SERVICE 173

Intelligent I/O Architecture Enables Faster, More Flexible Systems

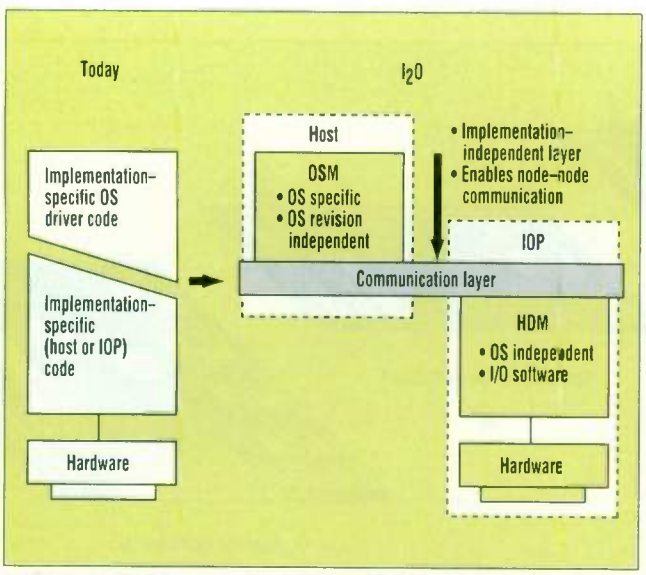
An Intelligent I/O Subsystem Eliminates The Need For Multiple Drivers For The Same Device And Offers Options For High-Speed Data Transfer.

Pauline Shulman, *Wind River Systems, 1010 Atlantic Ave., Alameda, CA., 95401; (510) 748-4100; fax (510) 814-2010.*

Great yogic masters have long known that the surest way to quiet the busy mind is to focus it on a simple, repetitive task. We can apply this ancient wisdom to the design of network servers by focusing on I/O, that is the inbound and outbound flows of information between the host CPU and the attached peripherals. Doing so rewards us with servers that are more powerful in terms of throughput, more flexible in the variety of devices they can use, and more available because they are able to isolate and recover from faults. Beyond these possibilities, it creates new I/O capabilities because increased intelligence is added to I/O processing.

The heart of I/O processing is the process of managing the many interrupts generated by peripheral devices competing for the host CPU's attention. Imagine the sound of popcorn popping. I/O activity in a server tends to follow a similar pattern with dramatic bursts and occasional stray interrupts hitting the host CPU. As the server gets busier, servicing these asynchronous interrupts tends to disrupt and slow execution of the user's applications, severely reducing throughput. We can make I/O activity more coherent and minimize asynchronous interrupts by splitting the device driver into two parts. One part handles all the operating-system-specific work. The other part handles all the hardware-device-specific work and manages the asynchronous interrupts.

In this split-driver model, the host issues high-level requests such as read or write. Only after the request, or a batch of requests is completed, is the host interrupted. The hardware-specific part is off-loaded to a separate, special-purpose processor. Ideally, this processor would be efficient at interrupt processing, capable of direct memory access, and adept at message passing. Off-loading more of the I/O-related work onto I/O subsystems is known as intelligent I/O. The architecture for a new standard for intelligent I/O (I_2O), has been developed and proposed by the Intelligent I/O Special Interest Group (I_2O SIG).



1. The I_2O split-driver model reduces the plethora of drivers required for hardware compatibility. Each operating system needs only one operating system server module (OSM) for each class of device (network, storage, etc.). Each peripheral, in turn, requires only one driver written to work with the OSM.

The I_2O Standard

The I_2O SIG is committed to establishing I_2O as the industry standard specification for high-performance I/O systems. The group also wants to attract the widest possible range of vendors to become members

of the consortium. A number of leading suppliers have worked closely to develop the I_2O Architecture Spec. More than 70 companies are on the I_2O SIG including steering-committee members 3Com, Compaq, HP, Intel, Microsoft, Net FRAME Novell and Symbios Logic.

The I_2O standard is comprised of two software specifications: the I_2O Shell and I_2O Core. The I_2O Shell provides a register level interface, a host-programming model, a messaging model and a message set tailored for various classes of I/O devices. The I_2O Core provides an event-driven model and a set of application-programming interfaces (APIs) that make up the operating environment within the I/O subsystem. The APIs include a message interface, system abstraction and transport services.

Reusable Device Drivers

Before I_2O, most server and adapter-card manufacturers followed the traditional device-driver model. A different driver is needed for every operating system supported by each hardware device. For example, a minimally-configured server provides a network adapter, video adapter and mass-storage adapter. This same server also supports Windows NT, Netware and Unix. So nine drivers must be developed and certified before shipping the system. This is complicated and expensive for OS suppliers and hardware makers.

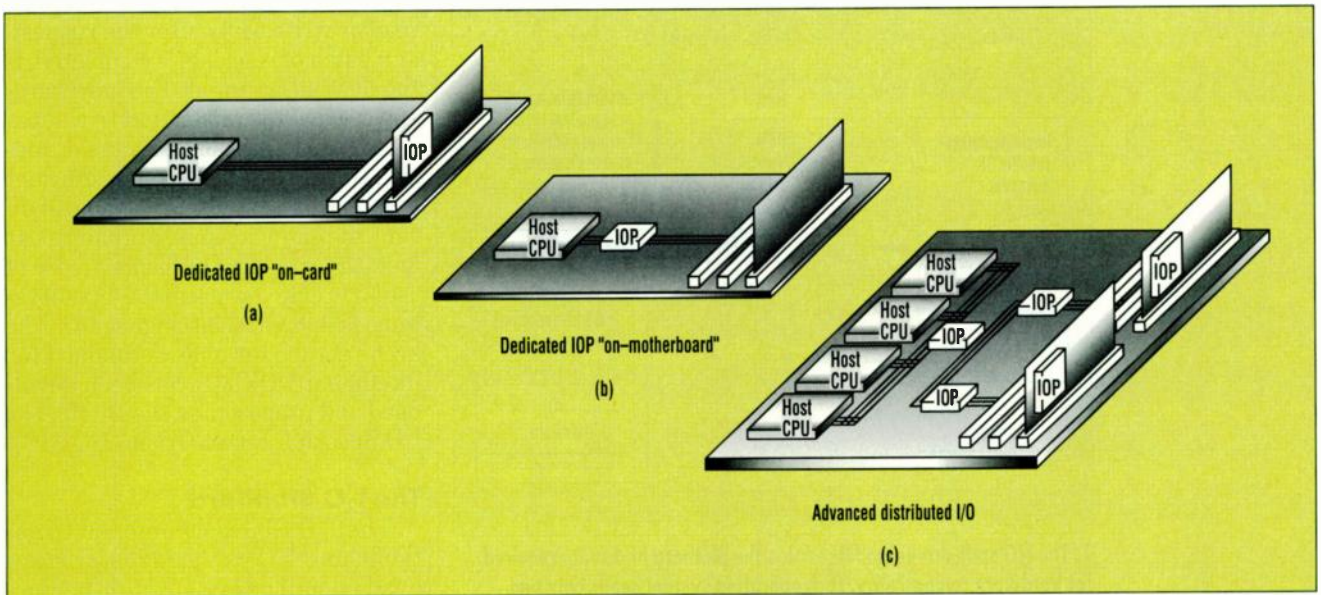
With the split-driver model, I_2O eases the burden by requiring only one driver per hardware device. If the same server mentioned above was equipped with I_2O, only three drivers would be required. Operating-system providers supply hardware-independent device drivers called OS Service Modules (OSMs). A single OSM will work with any device within its class. For example, a mass-storage OSM will work with any manufacturer's hard drive as long as it comes with an I_2O-compliant hardware-device module (HDM.) Peripheral manufacturers need only create a single HDM for each product *(Fig. 1)*. As Hewlett-Packard's Larry Shintaku put it, "Adopt I_2O as your standard, and you have to write another driver—but it will be your last one." Standardization and reusability of device-driver code, OSMs, and HDMs promises faster time-to-market for operating-system providers and system manufacturers, and more reliable software for users.

The I/O Processor

The intelligent part of intelligent I/O resides in the I/O processor (IOP), a special-purpose processor which can be on the host motherboard and/or on the I/O adapter card. It provides the operating environment for the HDM. The first I_2O implementations will be based on the Intel i960 RP and the PCI bus. As the first commercially-available IOP, the i960 RP is a highly-integrated, intelligent I/O subsystem on a chip. A complete RISC processor based on the i960 JF core, it also combines a number of peripherals essential to the I/O function, including a PCI-PCI bridge, DMA controllers, address translation units, an I/O APIC interface, an I^2C interface, a memory controller, and a messaging unit.

The i960 RP's on-board PCI-PCI bridge overcomes one of PCI's serious limitations—its ability to support only a limited number of slots for plug-in adapter cards. Bridging can extend the number of slots that a system can support. When the i960 RP is located on an adapter card, such as a high-speed, multi-channel adapter card, the bridge also can be used to decouple the on-board PCI bus from that of the host computer, reducing traffic and achieving better adapter performance.

Taking advantage of PCI commands, especially memory read line, memory read multiple, and memory write-and-invalidate, the i960 RP performs data transfers intelligently. In the case of PCI memory read multiple, by prefetching data from the PCI bus, the i960 RP achieves throughput near the theoretical



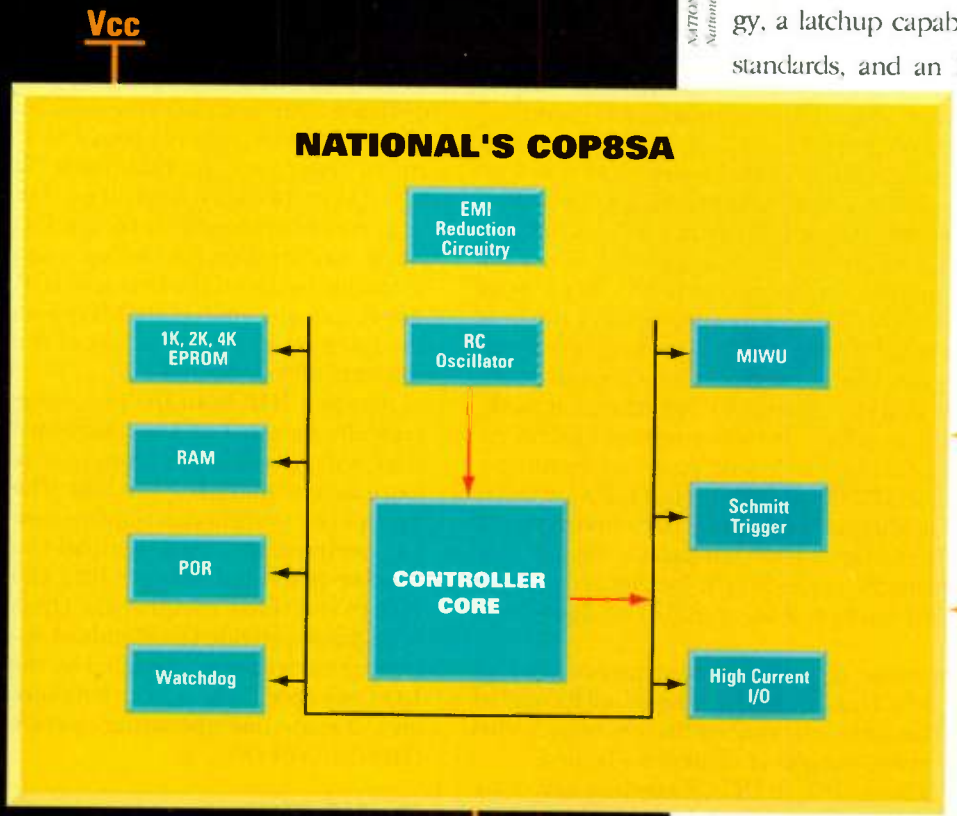
2. Several configurations are possible for I_2O systems using the IOP. Individual cards can be fitted with IOPs to plug into systems with I_2O-enabled operating systems (a). An IOP resident on the motherboard can handle multiple devices as long as they have I_2O drivers (b). In complex I/O subsystems, multiple IOPs could handle data transfers with no intervention from the host CPU (c).

ANY MORE INTEGRATED AND THIS 8-BIT MICROCONTROLLER WOULD BE DOING YOUR WORK FOR YOU.

INTRODUCING THE COP8SA SINGLE CHIP SOLUTION.

Oh, sure, you'll still have to connect the chip to the ground and the Vcc. But after that, you're pretty much done.

That's because the new **COP8SA** mid-range OTP microcontroller requires zero external components. Zip. Which means the R/C oscillator, power-on-reset (POR), pull-up resistors, schmitt-triggers, and protection diodes are all built in. Which means your life is instantly easier. There's even patented EMI technology, a latchup capability that meets stringent industry standards, and an ESD rating that's over twice the industry norm.



The result? The quality and reliability of a single-chip solution in an industry-standard footprint. Add easy-to-use development tools and an Evaluation and Programming Unit for under $99, and your product will be in the market before you know it.

The COP8SA. You're almost done already.

FREE INFO KIT—FAST.

To test the COP8SA, contact your local distributor. While you're waiting, give National a call and we'll get you started.

CALL: 1-800-272-9959 Ext. 738.

WEB: http://www.national.com/see/cop8sa

In Europe, fax us at +49 (0) 180-5-12-12-15; in Japan, call 81-43-299-2308; in Southeast Asia, fax us at 852-2376-3901.

National Semiconductor

READER SERVICE 184

maximum for PCI systems.

Four 64-byte FIFOs permit decoupling the two PCI buses from the i960's own local-memory bus. Each PCI bus has its own address-translation unit so that it can move around in the host's space without affecting the situation on the other side of the i960. To aid high-speed data transfers, there are three DMA channels capable of handling scatter-gather transfers. Scatter-gather DMA can be used to improve the performance of network packet processing. Instead of copying payload data so that a header can be prepended before transfer, the i960 can use scatter-gather DMA to transfer the header and payload from different areas of memory directly into an output buffer. The DRAM controller accommodates memory for local buffers and code storage. The i960 IOP can download its firmware from the host, simplifying code updates.

INSIDE AN IRTOS

The IRTOS (I/O real-time operating system) must provide for all the elements of the I2O Architecture Specification. These include an event-driven driver framework, host-message protocols, and executive modules for configuration and control. It greatly simplifies the writing of basic device drivers, provides NOS-to-driver independence, and provides a prioritized multi-threaded framework that allows I/O software from multiple vendors to coexist safely. It should be scalable across all I2O configurations, from dedicated on-card I/O processors to open on-motherboard implementations, to complex distributed I/O systems servicing multiple CPUs.

In addition, an IRTOS must contain a number of features that make advanced I/O subsystems possible. It allows for peer-to-peer communications, enabling two IRTOS-based systems to talk to one another without intervention, for greater offloading of the CPU. It manages hierarchical driver modules and intermediate service routines (ISMs)—software tasks such as network management and RAID control algorithms that are increasingly becoming the responsibility of the I/O processing system—despite being a step or two removed from the actual hardware functions.

The core of an IRTOS is the kernel. A well-designed kernel allows the real-time operating system to minimize system overhead and respond quickly to external events. Ideally, the kernel will support a full range of real-time features including fast multitasking with 256 priority levels, microsecond interrupt handling, and both preemptive and round-robin scheduling. It also would provide efficient intertask communication mechanisms and three types of semaphores for controlling critical system resources—binary, counting, and mutual exclusion with priority inheritance.

There are differences between an IRTOS and the typical RTOS which is aimed at accommodating the demanding I/O processor (IOP) environment. By taking advantage of the IOP hardware's message-passing capabilities, it is possible to both eliminate the inefficiencies of spin-locking and provide high performance in the symmetric multiprocessing (SMP) configurations that characterize many servers.

In addition, an IRTOS needs a robust object-oriented structure in which all objects are owned by other objects. If an object is destroyed, all its related objects must also be destroyed. This technique enables drivers to be loaded and unloaded on the fly without leaving vestiges of themselves behind.

Because DMA is so critical to efficient I/O, an IRTOS needs to have a sophisticated DMA model. Typically, the complexity and potential coordination problems of DMA have given rise to inefficient implementations, whereby a single driver will attach itself to a single DMA unit and keep it even though the unit sits idle for most of the time. Worse, other drivers are prevented from carrying out DMA operations because they are not attached to a particular DMA unit. An excellent solution would be a queued DMA structure. In this scheme, any driver can request a DMA operation, all the requests are queued, and each is processed in turn as soon as an appropriate DMA unit becomes available. Notification of the DMA completion is sent back asynchronously through the event queue mechanism. In addition to being far more efficient, this model also makes DMA much easier to use.

The IRTOS also shields the driver writer from detailed configuration issues, such as the number of interrupts hooked up in a particular peripheral, or the number of available DMA channels. The API is designed to hide all such specifics; in effect, the IRTOS acts as the BIOS for the IOP.

Dedicated Vs. Open IOPs

Two configurations of I/O processors are addressed by I_2O: these are dedicated IOPs and open IOPs. A dedicated IOP is an I/O processor included on a peripheral board that runs software only for that board. To be I_2O-compliant, a dedicated IOP only needs to conform to the I_2O Shell specification for the message protocols between the host and IOP. There are no constraints placed on the internal implementation of the software on a dedicated IOP.

An open IOP is an I/O processor typically included on a motherboard that will run drivers from one or more independent I/O vendors. The user of the system can acquire new I/O peripherals and download the vendor-provided drivers into the IOP to run those peripherals. Open IOPs must provide the standard operating environment specified by the I_2O Core specification, which defines an I/O real-time operating system (IRTOS) API *(Fig. 2)*.

The I/O RTOS

The IRTOS is the software running on the I/O processor which implements the I_2O Shell and the I_2O Core API. The IRTOS is the operating environment for the HDMs. The first implementations of I_2O will incorporate IxWorks from Wind River Systems. IxWorks I/O real-time operating system, is a special-purpose version of VxWorks *(see "Inside an IRTOS," this page)*.

In addition to implementing the I_2O Core API set, the IRTOS also supports the I_2O embedded-kernel-services API. This API provides the HDMs access to operating-system

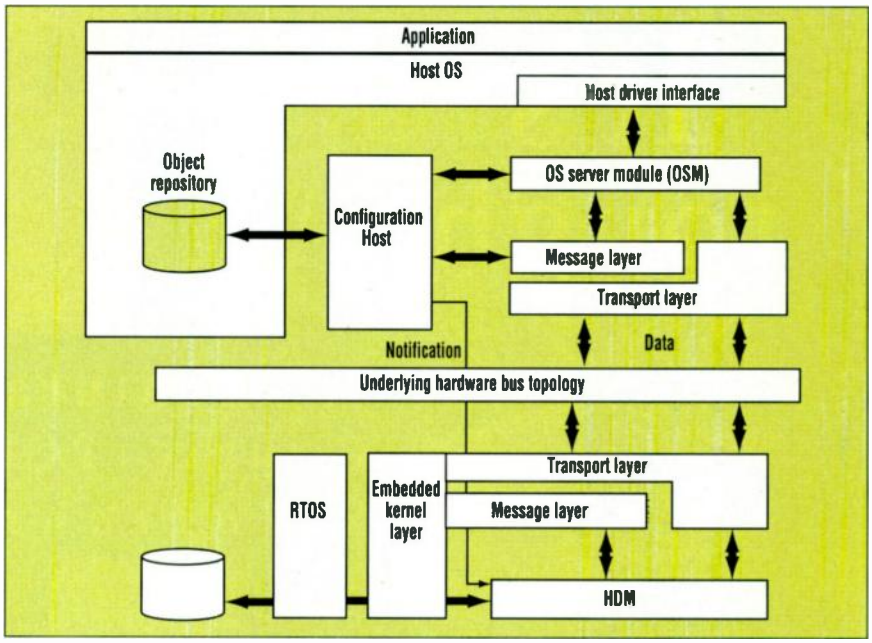
functions without exposing the underlying kernel's interfaces. This arrangement is important in meeting the I_2O SIG's objective of allowing HDMs to run in multiple-target execution environments. If an IOP other than an i960 IOP, and/or if an IRTOS other than IxWorks is used in future designs, existing HDMs, typically written in C, are reusable *(Fig. 4)*.

Message Passing

I_2O is composed of three components: the host side (eg. Windows NT), the IOP side, and the message protocols in-between. The message protocols have several layers, from the low-level message-passing protocol to the logical message content.

There is an important bit of hardware included in the I_2O specification for the IOP called a "hardware-assisted message-passing unit." It is a special section of memory on the IOP that implements FIFOs with atomic operations in hardware. Writing to one of these hardware FIFO locations will put the value being written into the associated FIFO, and increment the write index indivisibly. Likewise, reading from one of these locations will get the next value from the FIFO and increment the read index indivisibly. Thus the host can put or get message buffers from the IOP in a single write or read, respectively. This process is critical for the host-IOP communication because it does away with high-overhead communication mechanisms like test-and-set spin-locks, even where the host is an SMP configuration.

Layered on this hardware mechanism is a protocol for passing messages. The IOP allocates a configurable number of free-message buffers and puts their starting addresses in a FIFO of free buffers. *(Fig. 4, again)* When the host wants to send the IOP a message, it gets the starting address of a free buffer by reading from a free FIFO (a single read from the PCI bus), fills in the buffer, and puts its starting address in an input FIFO for the IOP (a single write to the PCI bus). Writing to the FIFO in the IOP generates an interrupt in the IOP which triggers the processing of input FIFOs. When the IOP is finished with the message, it returns its starting address to the free FIFO.



3. A standard kernel-level API isolates the underlying RTOS as well as the particular processor used as an IOP from the hardware driver. This arrangement makes I_2O an open specification that will be implemented with a variety of processors and real-time operating systems.

When the IOP wants to send a message to the host, it gets a buffer address from a free FIFO, fills it in, and adds it to the output FIFO for the host. The IOP also has mechanisms to interrupt the host CPU to trigger processing of the output FIFOs. The same protocol can apply to IOP-to-IOP communications as well. All messages have a fixed-length header that specifies source, destination, command, status, etc. The data comes in a variable-length part, called the message payload.

On top of this basic message passing, I_2O defines specific messages for each class of I/O device. Initially, messages have been defined for mass-storage devices and network devices. A single set of messages will apply to any particular device type. For example, all mass-storage devices will use the same mass-storage device message protocol.

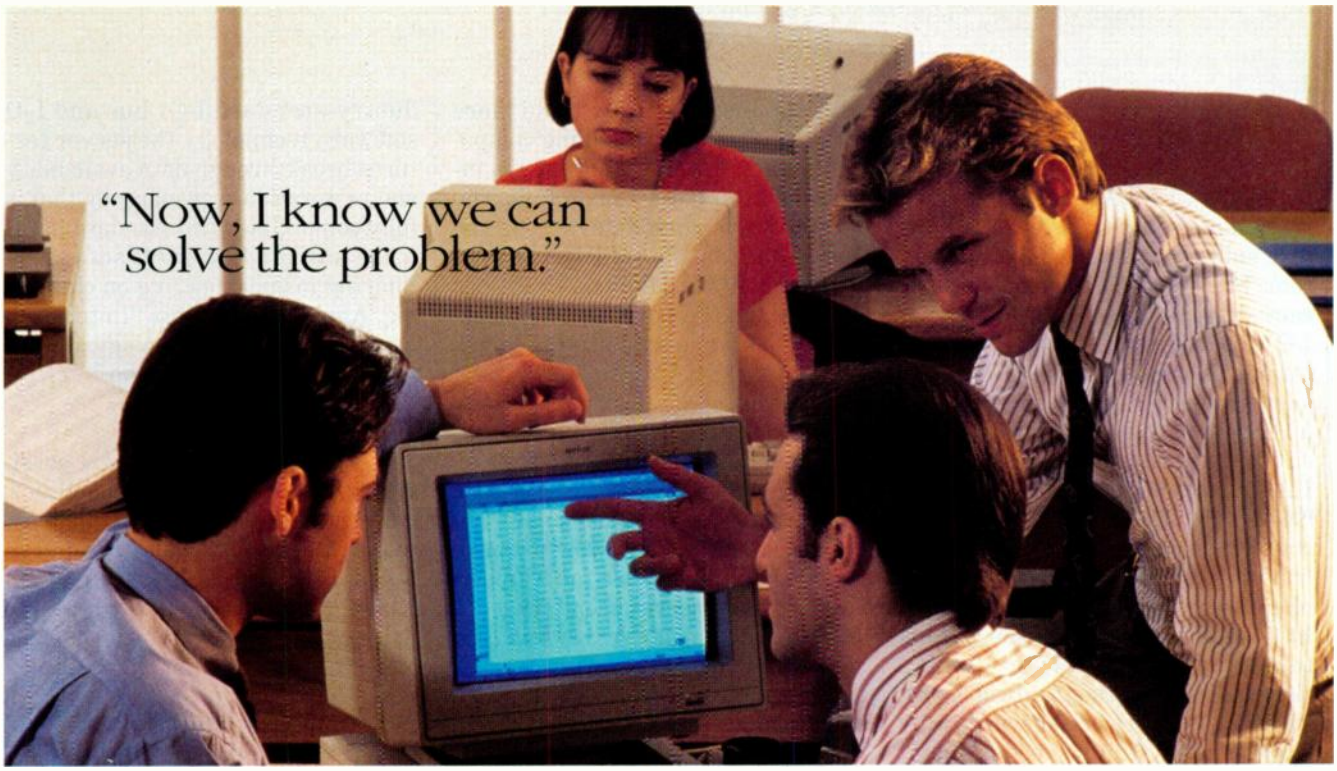
This design simplifies things on the host side since there will be a single driver for each of the device classes. In addition, the host OS would supply APIs for lower-level layers, e.g. direct message-passing functions, to allow development of custom devices, unusual IOP interactions, etc. On the IOP side, a considerable amount of platform software must be provided. This software includes basic RTOS functions, different levels of message protocol functions, an I/O driver framework, configuration, and initialization framework.

Higher Consciousness

We've already seen that splitting the work of I/O processing between the host processor and the I/O processor improves throughput in mainframes. Extending this improvement to industry standard PC-network servers is the next natural step. Writing, testing, and supporting fewer drivers also is easier and cheaper. Still, it is more evolution than revolution.

What if we let the IOP take on a life of its own? What if, besides being able to communicate with its host CPU, an IOP could communicate with other IOPs on the motherboard, on plug-in adapters, and even host CPUs and IOPs in other computers? Two breakthrough technologies have emerged from this idea: peer-to-peer and clustering. Both are covered in revision 1.5 of the I_2O Architecture Specification.

Peer-to-peer allows data transfers and, in some cases, complete I/O operations between I/O adapters



Introducing Three New Pentium® Tools

PowerPack® EA-Pentium®
High Performance.

PowerPack® SW-Pentium®
Fast Solutions.

PowerPack® ITP-Pentium®
In-target Probe for Software Development

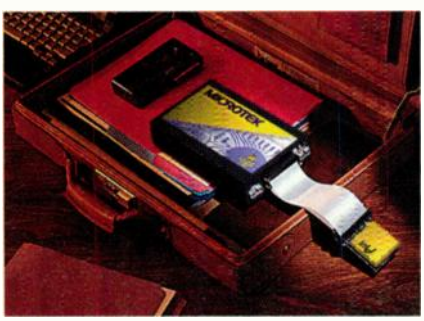
These new Pentium® in-circuit emulators show software and hardware events that are invisible with any other tools.

Software debuggers lack hardware event triggers and full-speed trace, making it difficult to isolate and identify real-time conflicts.

NEW **SWAT™ Software Analysis Tool**

Now you can check code coverage and monitor performance without inserting instrumentation tags into your source code.

Microtek's unique SWAT™ software analysis tool offers the same transparent interactive control you get with our high performance emulators.



"I was surprised to find that Microtek already has three different Pentium tools that fit into my briefcase."
Gary Rains
Development Systems Director

Clock-Edge Event Triggers
Microtek PowerPack® High Performance Emulators relate hardware events back to the source code with clock-edge resolution.

160-Bit Wide Trace
Now you can see what is happening in real-time without stopping the target. With 160-bits wide by 256k frames deep trace, virtually no target activity goes unrecorded.

Shrinking Probe Head
The new PowerPack® EA-Pentium emulator is only 7.2" x 4.6". And the probe tip is only 3" x 1.9", barely larger than the target microprocessor!

Microtek Emulators available for:

Pentium® • Intel486™ • National NS486™
AMD AM486™ • Intel386™EX • 386DX
386CX/SX • 80C186

68360 • 68340 • 68F333 • 68332
68331 • 68330 • 68HC16 • 68328 • ColdFire

To find the solutions to your problems, please call:

1 (800) 886-7333

(503) 645-7333

Email: info@microtekintl.com

Fax: (503) 629-8460

MICROTEK
IN-CIRCUIT EMULATORS

Web: www.microtekintl.com

without intervention by the host CPU. Xpoint Technologies of Boca Raton, Fla., has developed an I_2O-based disk-to-LAN solution which streamlines data transfers from the disk subsystem to the LAN subsystem. The solution avoids bottlenecks caused by traditional network-server I/O processing and host-memory limitations. Xpoint's BusBIOS software allows intelligent I/O adapters within a PC server to act as an intelligent subsystem. For example, multiple LAN adapters, each with an on-board i960 IOP running IxWorks, communicate with each other to provide high-bandwidth peer-to-peer and client-to-client operations across a standard PCI bus. The host processor is freed to perform client/server applications, and the overall bandwidth provided by the network server is fully scalable up to Gbit/s speeds. Xpoint has demonstrated a 275% improvement in performance over traditional I/O using disk-to-LAN software and adapters. Peer-to-peer also can be used for applications like on-line backup or disk-to-tape operations without taking down the host or degrading service.

"Clustering is the wave of the future," according to Carlton Amdahl, Chairman of the I_2O clustering working group. The goal of clustering is to make separate computers, interconnected with some form of high-speed network, presenting the image of a single system. With a cluster of systems, each server has its own resources, such as processors, I/O, memory, storage, and operating system. The server also may be responsible for its own primary set of users. In addition to providing varying levels of redundancy and fault tolerance to users of the other servers in the cluster, multiple servers may provide scalable performance and load balancing.

The key benefits of clustering to end users are scalability and availability. Scalability refers to the idea that by linking in additional computers and/or peripherals a user can incrementally build more powerful systems by adding components over time. Availability is increased because if a node fails, the system stays up and devices on the failed node can often still be used.

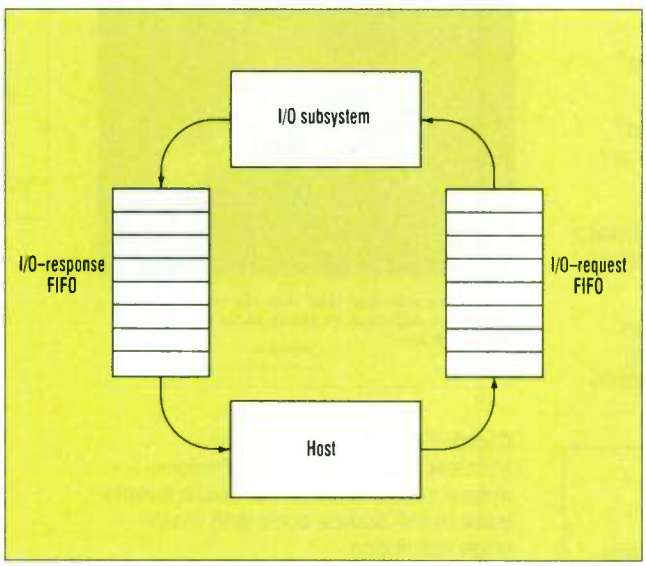
NetFRAME, Milpitas, Calif., has championed the effort to bring clustering to standards-based network servers. NetFRAME's ClusterData, software brings clustering technology to LANs using IntraNetWare Directory Services (NDS). ClusterData allows two servers to access the same data volume, although not simultaneously. One functions as the primary server while the other functions as the secondary server, monitoring the first. If the primary server fails, the secondary mounts the volume(s), setting up another path through which clients can access the data.

Servers can be cascaded so that one server may be set up to act as the backup for more than one primary, and a given server may be both a primary and a backup at the same time. Add to the picture NetFRAME's NF9000 network server. Based on industry-standard PCI bus and I_2O software technology the server features breakthrough data availability and restoration transparency that is fully compatible with standard hardware and off-the-shelf software. Sharing his perspective on clustering, Amdahl sums it up, "In terms of using commodity technology, it is almost the only right solution."

Enterprise Computing

I_2O opens the door to new possibilities by enhancing I/O capabilities. Easing development effort and cost will accelerate the development of new technologies. Distribution of I/O-intensive processing will lead to more-balanced system performance and dazzling system throughput. IOPs will take on more complex tasks such as running protocol stacks, and eventually their application will expand beyond the server market. Standards-based I/O will provide better variety of off-the-shelf solutions. More and more hosts will interconnect to other hosts and operate as a single, scalable, fault-tolerant system.

Bringing components and systems together in a highly integrated and effective way is an impressive feat. But perhaps even more impressive is bringing a group of competitors together, like the I_2O SIG. In a fiercely competitive industry, the idea of rival companies productively working together and sharing technology secrets, to forever change the computer industry for the common good, is phenomenal.



4. The host initiates a transaction by writing the address of the data structure used to transfer packets between the adapter and server memory into the I/O request FIFO. An interrupt is generated to the I/O processor only when the FIFO transitions from empty to full. The I/O processor reads the pointer and transfers the associated data structure to local I/O memory. Once the I/O processor has completed the request, it places the pointer in the I/O response FIFO. The host reads the pointer from the I/O response FIFO and completes the transaction. The data structure is then available to be reused for another host transaction. The I/O subsystem also can initiate transactions in a similar way. There are additional I/O request and I/O response queues for the I/O subsystem to initiate transactions to the host.

Pauline Shulman is Wind River Systems' product marketing manager for I_2O. Ms. Shulman has been an R&D software engineer for 18 years. Prior to Wind River, she developed network servers for Hewlett Packard and a variety of other products for Tandem Computers, Seagate Technologies, and National Semiconductor. Pauline has a Bachelor of Science Degree from San Jose State University.

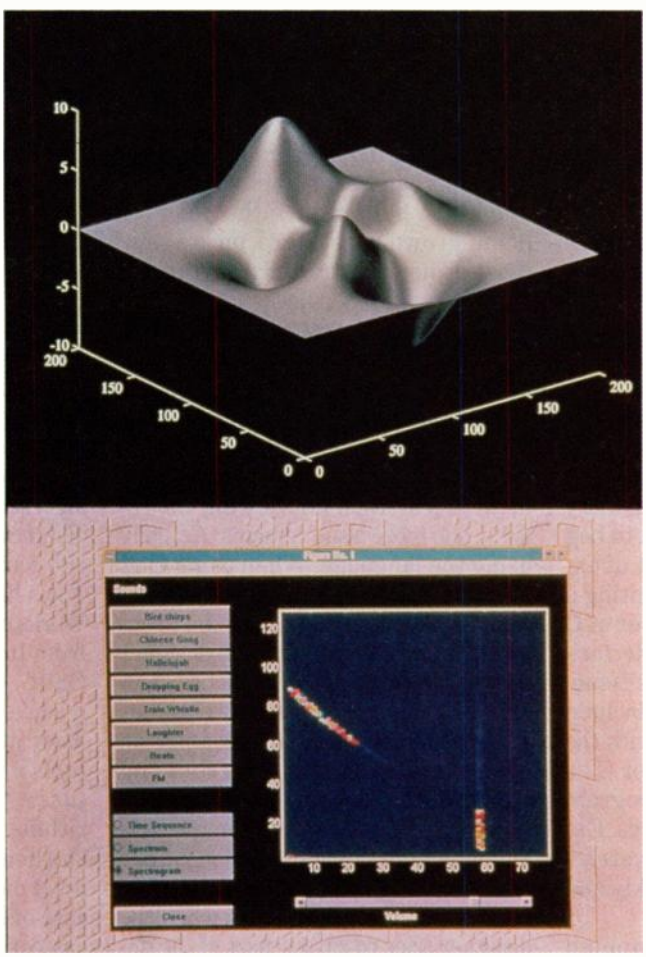
Advanced Software Tools Narrow The Prototyping-Implementation Gap

Developing complex algorithms for embedded systems requires experimentation and simulation. New development tools are helping engineers turn their ideas into code.

RANDY CONK, 9 Hawthorne Pl. #7M, Boston, MA 02114.

The majority of embedded systems developed today operate at higher degrees of complexity and include more mixed-signal circuits than ever before. Engineers of these systems have been struggling to balance the time-consuming, labor-intensive process of system-level design and languages such as C and C++ with the pressure to reduce cycle time. Generally, C and C++ are used for the speed at which the code is executed, as well as for the freedom they allow for implementing almost an unlimited number of data structure types. C and C++ also have been around for a long time and are now ANSI standards. Yet these languages can be tedious for new designers and for exploring multiple conceptual ideas in a design cycle. What is needed for concept and architectural testing is a simple and powerful way to implement ideas quickly in software while still being able to view results in a reasonable amount of time.

Many companies require software tools that enable engineers to manipulate and analyze complex mathematical computations and algorithms while presenting the results in an easy-to-interpret form. Aerospace companies testing the control systems of airplanes rely on such software as heavily as communications companies developing handheld devices do. These tools are often used to speed the processes of designing analog circuits and system-level architectures. Such tools also have been used to simulate complete systems in ways that were not available with conventional tools, such as in bit-error rate (BER) testing. The tools that are used surpass the capabilities offered by more general languages, both in features and in ease-of-use. Furthermore, they add value to the design process by allowing engineers to easily integrate their results with C and C++ code and ultimately to complete product design and prototyping within a single environment.



1. The vidualization features of MATLAB include the ability to graph functions in 3D (top). Here, a function of two variables is rendered using Gouraud shading and multiple light sources. The bottom display shows an audio spectrogram of a dropping egg. MATLAB provides a GUI that lets the end-user choose from several operations to perform on selected waveforms.

Doing It The Old Way

Before software tools for algorithm development became available, engineers often resorted to one of two approaches. They developed algorithms within an interactive environment, and then manually translated their work into C or some other language for implementation. Some of these interactive environments provided flexibility but lacked the power and speed of other languages.

Generally, these tools were not integrated with the rest of the development process. In essence, engineers were required to do their work using two or more different programs that did not speak to one another. This process of transferring the output between developing systems was not only time-consuming, but also error-prone. Alternatively, engineers developed their algorithms using a compiled lan-

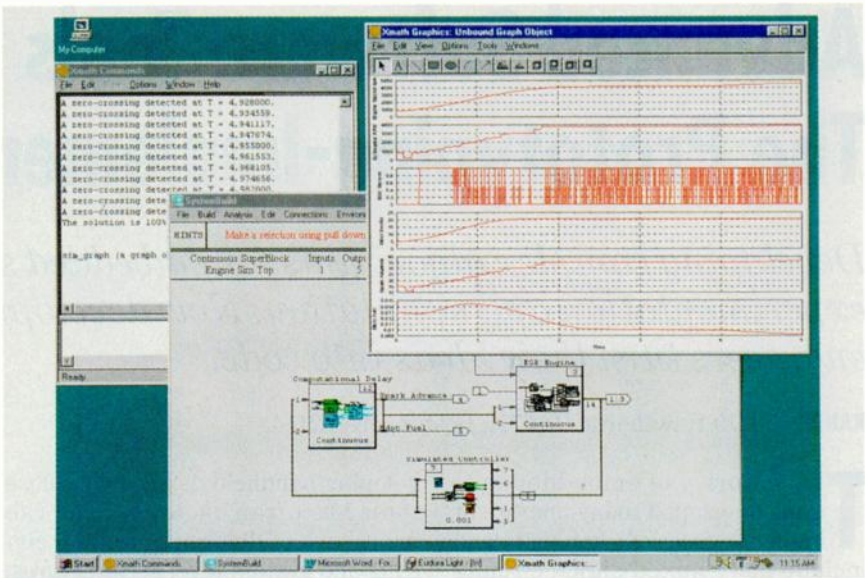
guage such as C, C++, and FORTRAN. This compiled-language approach removed the need for translation for implementation, but lacked the interactivity, graphics, and computational core provided by other software packages, thus limiting the opportunity for efficient problem-solving.

In the digital design world, high-level languages have been widely available for years, the two most common being Verilog and VHDL. Many digital designers have used these languages and software synthesis tools to develop actual circuits. However, these languages help only the electronic digital design community. When it comes to analog, mixed-signal, or system design, the utility of these languages drops off. Many creative engineers have used C and now C++ to model system level circuit designs. However, this approach still has the disadvantage of constantly having to deal with the intricacies of the programming language rather than the system design. Both C and C++ leave the designer with a large initial learning curve, a limited library of functions and constant concern with how to code the design in C or C++ instead of how to implement the design itself. In other words, the language gets in the way of solving the problem.

Dealing With The Issues

Initially, when attempting to use C or C++, the designer needs to spend a large amount of time up front to understand the structure and commands of either language. Pointers and memory management have been known to bog the new users down to a point of extreme frustration in implementing a new data structure. A new user of C and C++ also must deal with the variable, function and class scope issue. The designer must ask: Did I include the correct file? Am I linking with the correct library?. To a new C or C++ programmer, developing a program that works is an accomplishment. Experimenting with multiple system-level design architectures quickly and easily is unthinkable.

Having successfully tunneled through the initial learning curve, the next concern for a design engineer is the lack of standard library functions for both C and C++. More often than not, C and C++ programmers spend a fair amount of time creating functions and/or classes which implement tasks such as calculating an FFT, printing a form, or plotting a result. Classes and functions can be found or sometimes bought to help reduce the need for home-grown code. Here, once again, the designer is distracted from the real issue at hand, When designing a circuit or system, the designer is forced to consider issues like which functions to implement and how to view the results.



2. Functional blocks can be connected by users building embedded control systems with the MATRIXx SystemBuild facility. Here, the MATRIXx Xmath and SystemBuild tools display the results of a simulation. Using simulation, such a system can be evaluated and optimized prior to generating code.

After all is said and done, and the designer has learned C or C++, has built the additional libraries, and implemented a method for viewing the results, one more issue remains: Actually using the language. When using C or C++, the designer, at times, is more focused on the language than the problem at hand. For instance, the designer may ask: Should this variable be a double or a float? Should a new class for this structure be created, or is there an easier method? Pointer errors and memory leakage problems cause designers to completely focus on the code and language implementation rather than the design to be done. C and C++ also have inherent problems when the designer tries to rip out part of the design and simulate it without having to modify code. This task usually requires writing special test code and hooking it into the code to be modified.

What is needed is a programming and simulation environment that lets the system design engineer easily program and try out new system architectures without having to fight the programming language or spend weeks learning its intricacies. Once you have made the decision to use an advanced development tool, rather than just C/C++, you next have to decide which tool, or collection of tools, you want to use. Of course, that decision centers on what you are trying to build.

Some engineers want to develop device-level algorithms; others want to develop a system that may incorporate algorithms, but which also has an overall functional architecture showing how the various devices work together Tools like MATLAB from The Math Works of Natick, Mass., and MATRIXx from Integrated Systems, Sunnyvale, Calif., offer fourth-generation languages (4GLs) for defining algorithms. They also offer block-level modeling tools for describing system architectures. The 4GLs let you define algorithms relatively quickly, without all the headaches of C/C++. The block-level modeling tools (Simulink, in the case of MATLAB; System Build in the case of MATRIXx) let you model the architectures by drawing blocks representing various devices and software components and viewing the corresponding outputs and inputs among them *(see "The power of 4GLs: A case study," p. 135).*

The Power Of 4GLs: A Case Study

A handful of leading-edge organizations have found a solution to the C and C++ language problem: One major communications company, for example, concerned with losing valuable time and R&D engineers to the programming learning curve, is using advanced front-end application development tools that incorporate math, graphics, GUIs, and specialized functions that enable engineers to focus on the engineering task at hand, rather than on the intricacies of programming languages.

In designing local-area network transceivers, the engineers have been able to simplify, hasten, and improve the integration between architectural analysis and design by implementing their system-level simulations using the language provided within the MATLAB framework. In designing the transceivers, engineers depend upon the software to characterize how a signal travels down varying lengths of cable, to design the equalizer, and to test the product's different architectures for adaptation to varying conditions.

In the latter of these processes, the engineers needed to develop algorithms to simulate system behavior to make judgments about the feasibility and effectiveness of a particular architecture. To simulate the system within a reasonable time frame, the MATLAB compiler was used to autotranslate MATLAB programs into C code, which was then integrated into the original environment. This allowed the engineers to simulate more conditions and architectures than would otherwise have been possible without the speed of compiled code. Without the compiler, the engineers would still be simulating today. It greatly altered the engineers' end-result product because it sped up the design process to a point where they had the freedom to explore areas they otherwise couldn't have touched.

Until now, the use of compiled C code for system-level simulations has been limited to those few with the ability to learn C and create the code necessary to define the system. Engineers have not been given sufficient freedom to easily change code in an effort to explore architectural differences of solutions.

It also is important to recognize that while tools like MATLAB and MATRIXx can model the behavior of algorithms, they cannot model the actual implementation of algorithms into circuits. For that you might need a tool like Spice, a common industry standard for designing analog and digital circuits at the transistor level. Unfortunately, for large circuits, Spice simulations take far too long to execute. This is where analog behavior simulators are becoming more attractive. For example, SABER, from Analogy, Inc., is a tool for exploiting Analog Hardware Description Languages (AHDL) and behavioral modeling in circuit simulation.

With SABER's modeling capability, transistor-level circuits can be modeled in a way to maintain the electrical integrity of the designs (i.e., models do not violate Kirchoff's laws concerning current and voltage) while still maintaining simulation speeds that execute much faster than SPICE. Together, Spice and SABER can be used to create accurate, fast simulations of large circuits which have already been shown to work functionally in MATLAB or MATRIXx.

It also is important for embedded system engineers to realize that just because a product lets you do math on a computer screen or generate graphs from numeric inputs, doesn't necessarily make the product ideal for embedded systems programming. Two examples of products that provide very complex mathematics and graphing yet address different needs are MathCAD from MathSoft, Cambridge, Mass., and Mathematica, Wolfram Research, Champaign, Ill.

The applications that are addressed by these products just don't happen to be embedded-systems programming. MathCAD, for example, is oriented toward teaching math and doing math in a scratch-pad or white-board-type environment. MathSoft describes MathCAD as a "graphing calculator, a math-smart word processor, and an interactive encyclopedia." MathCAD may be effective for users who want to solve complex math problems and arrive at a numeric result. However, it does not provide a programming and systems modeling environment. Embedded systems people aren't looking to simply replace their calculators and drafting paper. They're looking to replace C, C++ and Fortran.

What MathCAD does for numeric computation, Mathematica does for symbolic computation, including graphing. Mathematica provides a white-board type environment, but this time, the white board is meant to reduce complex mathematical formulas to simple ones (the way a board full of equations reduces to $E = MC^2$).. But what MATLAB and MATRIXx provide is the ability to easily commit mathematics to external hardware.

One reason for using tools like MATLAB or MATRIXx is that they allow users to try ideas quickly without going through all the steps of creating a real circuit. Another is that they let you quickly develop algorithms that can be implemented and run as C/C++ programs in a computer. The question, "How quickly?" is often the basic measure that helps you decide which tool to use. There are several factors involved, including:

•Can the models be converted into C/C++? If a C/C++ program is what you are after, then the fastest way to get there from a 4GL is to have a compiler that translates the 4GL code directly to C/C++. The MATLAB programming language produces files called M files that can be executed in MATLAB. There is a code generator that can translate Mex files into C/C++ source code. MATRIXx has a code generator called AutoCode that produces C or Ada source code from functional blocks in its SystemBuild facility. SystemBuild lets users graphically connect functional blocks to design control systems and other embedded applications.

•Does the environment support interactive analysis of the model? In other words, once you build the model, can you feed it data and view the results? Can the way results are presented be manipulated by the user through the tool's graphical user inter-

face (GUI) while the model is "on?" This capability can go well beyond simply having access to a previously-built plotting function or a plotting program. MATLAB and MATRIXx , for example, offer powerful object-oriented 2D and 3D graphics that support visual data analysis *(Fig. 1)*. Users can create color graphics with modern 3D features, such as surface rendering, wire frame, pseudocolor, light sources, 3D contour, animation, and more.

•Does the tool offer application-specific extensions? An application-specific extension, called a tool box in MATLAB, supplies pre-defined functions, icons, graphs and other objects that are useful to an engineer working in a specific area. An inference viewer taken from MATLAB's Fuzzy Logic Tool Box, for example, can display the relationship between membership functions and decision rules. Other MATLAB tool boxes cover such areas as wavelets, digital signal processing, and statistics.

MATRIXx offers extensions (called modules) in areas that include signal processing, interactive system identification, and interactive control design. Such specialized tools are a major time-saver, not only compared to C/C++, but also compared to developing in an advanced environment that lacks these tools. Perhaps the most important advantage of an application-specific extension is that it gives the engineer-user instant access to the best insights of world's leading experts in that particular field of engineering. Not only does the engineer not have to reinvent the wheel, he or she can have the best wheel available.

•Does the tool come with productivity tools for the developer? Other features that reduce the time and increase the quality of the modeling include things like a GUI builder, a performance profiler, and a GUI-based debugger. Even with a 4GL, describing how a GUI works can be an arduous task in a procedural language. A GUI builder provides pre-built objects that the engineer can select from to create a graphical user interface. A performance profiler gives line-by-line feedback about the execution time of a function. This gives you insight into which sections of code might benefit from further optimization, allowing you to increase the overall execution speed of the routine *(Fig. 2)* A GUI-based debugger, as the name implies, is a debugger that employs a graphical user interface to highlight and manipulate program text needing rework — making fixes easier to do than when working in a text-only mode.

•Can the model be easily ported to new platforms? A portable model doesn't just mean, "Is the C/C++ code generated ANSI standard?" It also means "Can the resulting code be embedded within other applications developed outside the modeling environment?" That requires not just an ANSI standard compiler, but also the ability to call and be called by external code. Some applications also may require the visualization engine itself to be embeddable within an external application's runtime environment. In the case of MATLAB, for example, you may want to use some of that tool's graphics capabilities in your finished application's output—rather than having to create your own graphics output engine by writing your own C/C++ programs. For embedded applications, the MATRIXx AutoCode tool allows you to create different templates so that the same model can generate code for multiple hardware platforms. Another aspect of portability concerns compatibility with other tools. Moving a functionally modeled circuit from MATLAB or MATRIXx to SABER, for example, for circuit-level modeling is facilitated by the integration of the products.

Clearly, developers should expect more than the basics when evaluating development environments. In the race to market, it is no longer enough just to leapfrog developers who think they have to hand code everything in C/C++. These days, developers should be looking for real power tools that can help them see their application's potential more clearly and realize that potential more quickly and more accurately.

Randy Conk is a freelance technology writer who has written a number of articles for publications such as Electronic Design, IEEE Spectrum, Computerworld, and Information Week. He holds an MBA from Clark University.

How Valuable	Circle
Highly	573
Moderately	574
Slightly	575

UPDATE ON OBJECT NOTATION

Standard Graphical Notation Proposed For Object-Oriented Development

Object-oriented CASE tools have long been half-jokingly referred to as "bubbles and arrows" in reference to the many forms of graphical notation used to depict objects and the flow of control, data, and state transitions in a system. As developed by numerous university academics, there have been a confusing array of formalized notations all aimed at expressing the same basic concepts, albeit from different viewpoints. These concepts describe the the relationships between program elements and software components in object-oriented systems. Now, a standard notation for objects and control is emerging from the confusion with the proposal of a Unified Modeling Language (UML). UML is being submitted by a consortium of leading edge software companies to the Object Management Group (OMG), Framingham, Mass.

Rallying to the efforts of Rational Software, Santa Clara, Calif., a group of companies has been formed to propose the standard in response to OMG's Object Analysis and Design Request for Proposal. The companies include Microsoft,Redmond, Wash., Hewlett-Packard, Palo Alto, Calif., MCI Systemhouse, Schaumburg, Ill., Oracle Corp., Redwood Shores, Calif., and Texas Instruments Software, Dallas, Texas. The joint proposal was submitted to the OMG at the beginning of the year.

The UML proposal merges three major and popular notations into a single, unified notation that can express the three basic views of a system from a single model. While all three methodologies started out to aid in the description of complete systems, they place emphasis on different aspects.

The three methodologies are the use case or scenario method developed by Ivar Jacobsen; the Booch method developed by Grady Booch; and the object modeling technique (OMT) developed by James Rumbaugh. All three developers now work for Rational and are completing the definition of the UML. They have come to be known as the "Three Amigos."

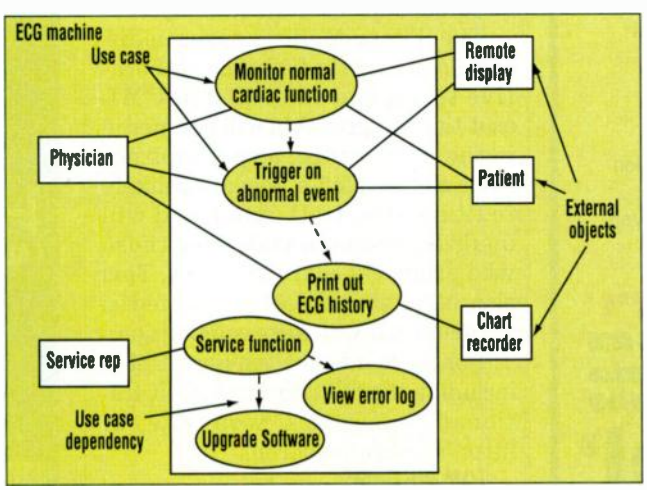
The Jacobsen or use case technique represents a system in terms of what happens when it is exercised. For example,asume a doctor sets up an electrocardiogram (ECG) machine and the patient undergoes some event that registers in the machine and causes it to monitor the patient, display, sound an alarm, or trigger on a given event *(see the figure)*

. The interactions between these events can be described in a sequence chart along with timing information related to the occurrence of each event. The use case technique develops scenarios of how a system is expected to work, and is therefore focused on requirements. The Jacobsen notation even includes a stick figure to represent a human user. However, use cases also can be represented as events like interrupts or sensor inputs that affect the system.

The Booch method is focused on iterative development by defining and successively refining a logical model. Booch diagrams concentrate on describing classes and the logical structure of a system. They show inheritance and dependency. Booch describes the detailed aspects of a design including message passing and object instantiation. Due to its hierarchical view of a system, objects created in the Booch notation can be defined at a high level of abstraction and then filled in with more precise details at the lower levels of hierarchy within them.

The Rumbaugh or OMT notation concentrates on partitioning the model among real-world objects which can be either in the form of hardware or software. Such objects can be physical devices such as sensors or controls. They also can be various types of software such as program modules and sections of code. The OMT view is toward defining how objects are related to the problem domain. Objects can include pieces of code that you don't write such as Active X control or Java applets that have their own interfaces. Finally,the UML will include a deployment view of the system that appears as a directory tree showing the relationship between all the elements in the code.

Rational Software is combining the UML with the latest version of its software development product-calledRational Rose 4.0. Rational Rose implements a technique the company calls "round-trip engineering," which grew out of the Booch method for iteratively refining the logical model. You start out by creating a fairly high-level conceptual or logical representation of the system. Once you have added sufficient detail to the abstract representations, the model can be used to generate source code in a variety of high-level computer languages including Ada, C++, and Java.



You can then go into the source code you've created and perform the familiar edit-compile-debug cycle to flesh out the software at the source-code level. The resulting code can then be used to update the model and its visual representation in the UML notation. This "round trip" cycle can be repeated until you're satisfied that the code generated by these iterations is ready for testing.

The other companies participating in the joint pro-

posal are making their own plans to integrate the UML in their software-development tools. Microsoft, for example, is expected to roll out UML with its next release of Visual Basic and to include it with subsequent releases of Visual C++ and J++. Once the proposal is adopted by the OMG, it is reasonable to assume that an even greater number of vendors will adopt the UML.

The one major school of notation that does not appear to be joining the UML bandwagon is the Shlaer-Mellor method. Shlaer-Mellor is primarily represented by the Bridgepoint development suite from Project Technology, Berkeley, Calif., and by Scientific and Engineering Software, Austin, Texas. Shlaer-Mellor does not follow the iterative approach but instead produces software through the technique of translation of analysis models. In Shlaer-Mellor, the analysis model—i.e., the formal description of the applications problem—is kept separate from the implementation of the translation. Models once sufficiently defined can be executed and their functioning examined in animation.

This separation of analysis from the underlying architecture of the system has two advantages. It allows the design and development of the architecture— namely the hardware and the operating-system environment—to take place independently of the task of application development, which can shorten the development cycle. In addition, it allows one given analysis model to be ported to different architectures. Shlaer-Mellor requires a complete and verified model before it can be translated into an actual implementation.

The Shlaer-Mellor approach differs so distinctly from the elaborative technique embodied in UML that the two probably will not merge in the near future, or perhaps not ever. Shlaer-Mellor appears unlikely to fit into the UML mold, and will doubtless remain viable for those who prefer its characteristics. This also means that if UML is adopted as a standard, it will have competition.

For more information abut UML, including the full document, visit Rational Software's web site at http://www.rational.com.

TOM WILLIAMS

UPDATE ON WEB SERVERS

Web Server-On-A-Card Enables Mobile "Virtual Networks"

A complete web server implemented on a PCMCIA card includes not only HTML pages, but an object-request broker, a corporate firewall and encryption, intelligent agents, and security. In addition, the same card provides communication services in the form of a 128-kbit/s ISDN basic-rate terminal NT1 adapter (BRI TA) and a 32.6-kbit/s analog modem service. The card incorporates an Intel 80486 CPU for overall functionality and a Motorola 68302 processor for communications. Called the WebHawk, the card will be produced by startup Menagery, Los Gatos, Calif. It is implemented as a PC Card type II, uses a 16- or 32-bit interface, and contains 4 Mbytes of nonvolatile memory and program RAM.

The idea behind the WebHawk is to provide an embedded and low-cost solution for mobile professionals to maintain communications via a private network that uses public and/or private communications services worldwide. The card can act as either a client or as a server, or can simply be used by other applications as a modem. If need be, the card can be removed from a laptop computer and with an ac adapter, can be left connected to a telephone line to operate in a stand-alone mode. The design also can be incorporated into other devices such as handheld personal data assistants (PDAs).

Menagery is creating two software technologies to achieve what it calls universal interoperability (UIO). The WebHawk includes full Internet protocols and a complete ISO network model, including a full TCP/IP stack It is based on the universal resource locator (URL) and is compliant with both the common object request broker architecture (CORBA) and Microsoft's ActiveX.

In addition, the software includes an architecture called AgentCy that enables users to create private and secure mobile networking. AgentCy defines an extension to CORBA called personal request broker (PRB) that supports intelligent agents called "flyers." Flyers can be sent to other AgentCy-enabled sites to actively search for and retrieve various types of information.

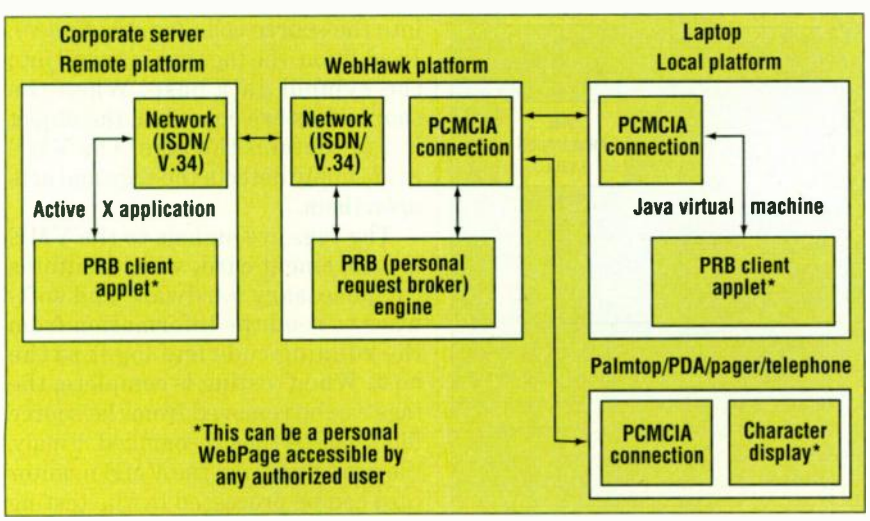
The PRB is a distributed live object software bus that combines both client and server functionality by providing equal object services to individual and work group users without dependence on a network server. Each PRB platform is capable of autonomous, self-hosted operations with remote PRB clients, direct operations with a local host (i.e., plugged into a PCMCIA slot), or simply as a PCMCIA ISDN or analog modem *(see the figure)*.

PRB platforms aggregated in a workgroup form a self-contained infrastructure. PRB applets can execute on any host that includes a PRB, in much the same way as Java applets can run on any Java virtual machine. Some of these applets can be flyers. A user may dial up either a server or another user's WebHawk, send a flyer and then log off. The flyer can perform whatever operations it is told to do at the other site, such as a doing a complex search of a database and putting together a report. The flyer would then dial back, send the results and log off, greatly reducing connect costs if the medium is a long-distance telephone line.

All copies of the device (expected to cost individually about $500) will be licensed to the customer. A network manager will set up the firewall and security with passwords and encryption keys. The manager can also set up web pages on the devices and on a corporate server if there is one. In effect, however, two WebHawks properly registered and encoded can form a private network that can connect over public channels. No other unregistered WebHawk or any other user can access that virtual network. One example of use could be that a traveling employee might leave the WebHawk attached to his hotel telephone line while taking his laptop along to a meeting. He would first send an update to the web site on the company server giving the telephone number. Anyone accessing the server could click on the link to his page and be connected. The employee could either dial into the WebHawk during the day and check messages with his browser or plug the card in on returning to his room and view his pages with the browser. While the first incarnation of the technology is in the WebHawk PC card, it lends itself to a wide variety of vertical applications such as privately networked appliances and instruments. Any device that is PRB-enabled can be accessed from another PRB platform and any human interface with an agent-based component interface can become a network computer system.

For more information, contact Menagery, 130A Knowles Dr., Los Gatos, Calif. 955030. (408) 866-8328.

TOM WILLIAMS



Board-based Tool Tests Complex Code That Runs In VME-Bus Systems

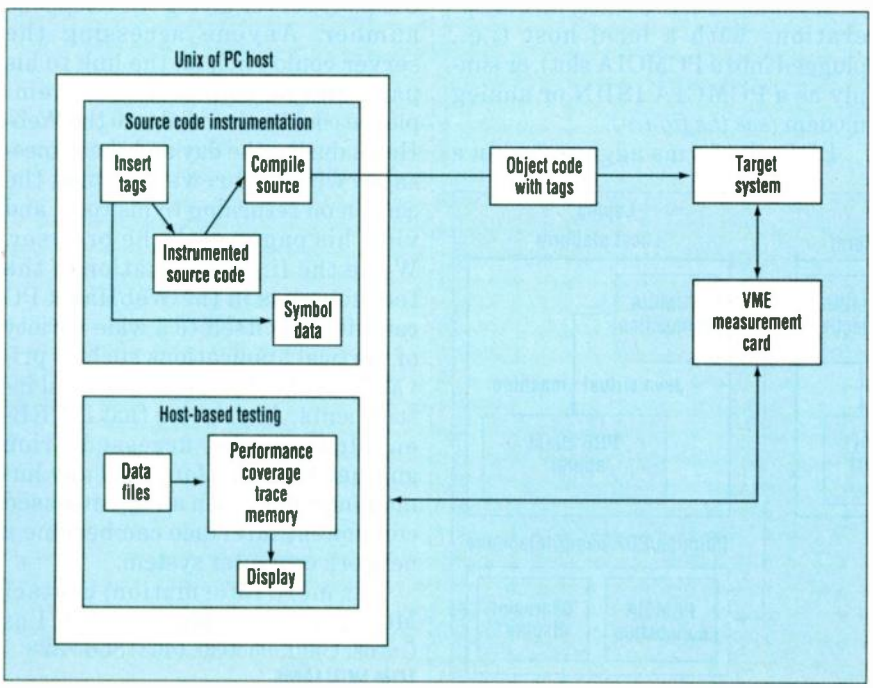
VMEbus systems are characterized by their complexity. They often involve multiple boards, multiple microprocessors, and large amounts of code—often in mission-critical applications.

A combination of VME hardware with software code instrumentation now makes it possible to run detailed tests and verify code coverage while an application is running in the target system. CodeTEST-VME, developed by Applied Microsystems, Redmond, Wash., uses its own VME board to monitor software that has had "tags" inserted into the code. The tags cause the VME test card to log data to a host system for testing and verification.

CodeTEST-VME can perform four types of tests on code running at full speed in the target: trace, performance, coverage, and memory. The trace tool displays software execution history at three levels. The highest level shows RTOS events and function entries and exits. There's a control flow level that lets you follow each decision point within each function. A source-level trace can focus on the C or C++ statements executed on a given processor, or it can display a high-level view of the system that shows the interoperation of multiple CPU boards. A rich set of triggering and storage features makes it possible to select the software context to be traced. Traces also are time-stamped automatically.

The performance test makes non-sampled measurements on the entire program. It can measure up to 32,000 functions at a time and the tool counts all pairs to measure the frequency with which each function calls other functions. Because the whole program is monitored, there's no need to pick out possible trouble areas. Functions are displayed in a table and can be sorted in various ways, such as by cumulative time or worst-case and best-case times.

The coverage test tool displays interactive coverage information as the program runs. Coverage can be displayed at the function, source, or summary level, highlighting the exact source code that's been executed. As a result, the areas that haven't been "forced" during the testing process can be picked out rather easily. The coverage tool also displays a graph that plots the amount of coverage over time so you can refine testing to improve coverage efficiency.



The fourth test, memory, looks for memory allocation and de-allocation errors, or memory leaks. These errors are easy to introduce with C++, but are extremely hard to track down. Such errors may not show up right away, but they can begin to unravel the code and cause a crash when the system is operating in a different part of the code. The memory test reports how many bytes are allocated by each allocation statement in the program.

CodeTEST memory displays histograms and tabular data that show the activity of each allocation statement. When an allocation error is detected, the context and time of the error is given. Because errors are often caused by something elsewhere in the program, the trace test tool can be used to look at the events that led up to the error.

Host-based testing tools often insert large amounts of instrumentation code into an application's object file to tell the system to log events and recognize errors. CodeTEST-VME calls upon the monitor computer on its 6U VME card to do the actual logging and communication with the host. The card can look at all the activity occurring in the systems over the VME bus. This means that the object code need only contain the "tags" that tell the VME card when to send data for the test programs to look at.

Rather than inserting instrumentation instructions into an object file (which can almost double its size), that will later need to be removed, CodeTEST-VME uses a host-based instrumenter program to insert tags into the source code *(see the figure)*. In addition, the tags are inserted into the symbol data base. When the source files are compiled, the object image contains the tags. The VME card simply detects the tags and acts upon them.

The tags are signals to the VME measurement card, which contains the necessary hardware and software to read the information from the running code and log it to the host. When testing is complete, the tags can be removed from the source file, which is then recompiled. Finaly, the data sent from the VME monitor card can be processed by the testing

programs on the host.

The CodeTEST-VME measurement card is priced at $9800, and licenses for each of the four test programs are $5000 each. Versions of the software are available for Sun, Hewlett-Packard and PC/Windows-based hosts.

Applied Microsystems
5020 148th Ave. NE
P.O. Box 97002
Redmond, WA 98073
(206) 882-2000
Web: http://www.amc.com.
CIRCLE 633

TOM WILLIAMS

Graphical Math Tool Aids Complex Algorithm Development and Generates C Code

A new mathematics-based development tool from The Math works, Natick, Mass., combines data modeling and analysis functions with the ability to interactively explore alternatives in complex-algorithm design. The math analysis functionality is supported by a set of graphical visualization tools In addition, the development tool called Matlab 5.0 supports the direct implementation of systems with mathematics tools for modeling and simulation as well as for code generation and optimization.

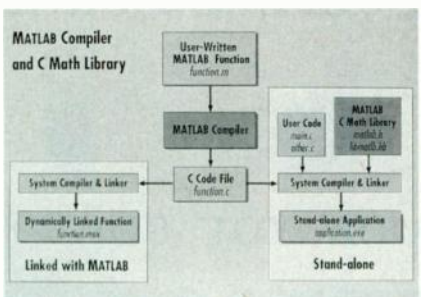
Matlab 5 builds on the extensive math libraries of its predecessor-Matlab 4, which also includes tools for numeric and symbolic computation, graphics and visualization and algorithm prototyping. What Matlab 5 adds to the mix is support for multidimensional arrays and user-definable data structures, multiple N-dimensional arrays, and integer bit manipulation functions.

New differential equation solvers let users tackle very large and complex problems with more efficient use of computer memory. The differential equation solvers use Matlab's sparse matrix for quick viewing of solutions on a graphical display.

Thanks to this interactive visualization capability of complex mathematical functions, developers and/or scientists can explore and develop ideas at an abstract or theoretical level and capture the resultant mathematical expression or equations for use in a later implementation. The files produced can be converted to C source code or compiled directly for use with other types of software *(see the figure)*.

There's no need to manually translate the concepts contained in the mathematical solution into a computer language such as C or C++.

Matlab 5 has an extensive graphical user interface development environment (GUIDE) for exercising the development tool's visualization and/or simulation tools. This enables a designer to set up modal and nonmodal dialog and message boxes. The Windows and Macintosh versions of the program also support 16-bit stereo sound.



A visual debugger makes possible real-time monitoring and debugging of Matlab programs. These programs are written in a Matlab 4GL language that produces an intermediate code called M files. The debugger together with 4GL allow interactive execution of any command during a debugging session—including operations such as loading data and displaying graphs.

In addition, a performance profiler provides line-by-line analysis of Matlab programs (M files), and lets users zero in on where code needs to be optimized. M files also are platform-independent and can be passed around and run on Windows, Macintosh, or Unix hosts running their native version of Matlab 5. Matlab programs can run interactively without the need for compilation. This capability coupled with the ability to interactively enter and execute commands, makes it easy for developers to modify algorithms.

Matlab 5 has a 3D graphical visualization tool allows for different camera views, and lighting and shading for viewing animated models. While graphic display programs can be used in simulation and visualization, M files also can be used to generate C code that's then compiled and employed in the final application.

To simulate the operation of physical systems that may be driven by software developed with Matlab, there's a simulation environment called Simulink 2. Simulink 2 can link M files to animated graphics of machines, robot arms, etc., and let you run evaluations of how code affects actual processes while retaining the ability to alter code on the fly to optimize operation.

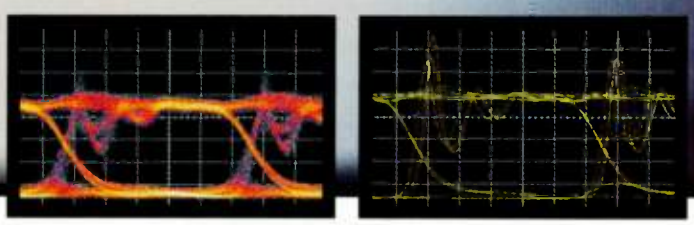
Matlab 5 has an improved object-oriented design for creating and using blocks, which are reusable code objects that can be graphically linked to form applications. The Math Works also supplies several block sets for special application areas. Developers can graphically link together functional blocks to form any applications, then perform simulations using Simulink to ultimately generate code. Block sets are available for DSP, fixed-point math, and for nonlinear control.

The Math Works also supplies over 20 "toolboxes,"which are packages containing Matlab programs for specialized application problem areas Toolboxes are different from block sets in that they have development tools and special displays for developing algorithms in advanced application areas such as control systems, fuzzy logic, neural networks, spectral analysis, and others. Several toolboxes, including the signal processing and control system toolboxes, are in the process of being updated for Matlab 5. Prices for Matlab 5 begin at $1695.

The Math Works
24 Prime Park Way
Natick, MA 01760
(508) 647-7000
Web: http://www.mathworks.com
CIRCLE 634

TOM WILLIAMS

How quickly you solve pattern-dependent problems all depends on how clearly you see them.



Let's get one thing perfectly clear.

Only HP's digital communication test equipment has Eyeline mode, which gives you a unique capability of viewing pattern-dependent effects. It also complements HP's high-speed BERT error location analysis feature, to give you the ability to determine where errors have occurred in your pattern.

Together, HP's high-speed BERT and digital communications analyzer allow you to quickly and accurately characterize and debug your designs with built-in measurements like: Jitter, Extinction Ratio, Rise Time, and Eye Height.

And, HP's high-speed BERT and digital communications analyzer are designed to work together so you won't have to patch together multiple pieces from different vendors, then hope and pray that they'll work together.

There is a better way.

If this looks like the clear choice for you, give us a call at 1-800-452-4844*, Ext. 1860 for more information.

And stop rubbing your eyes.

*In Canada call 1-800-276-8661, Dept. 285.

HEWLETT® PACKARD

Scope Tips: Some Helpful Hints For Making Scope Measurements

Oscilloscope users supply some practical ideas on how to make better measurements.

Last year Hewlett-Packard Co. offered oscilloscope users a booklet entitled "8 Hints for Making Better Scope Measurements." Along with the tips from lab engineers at HP's Electronic Measurements Div. in Loveland, Colo., the booklet contained an invitation to other engineers and technicians to send in their own tips for producing better scope measurements. The following ideas came from scope users in response to the invitation. Also included here are comments and suggestions added by HP.

The original booklet is still available. Call (800) 452-4844. The company is still soliciting scope hints, which can be e-mailed to meas_hints@col.hp.com or faxed to (719) 590-2193.

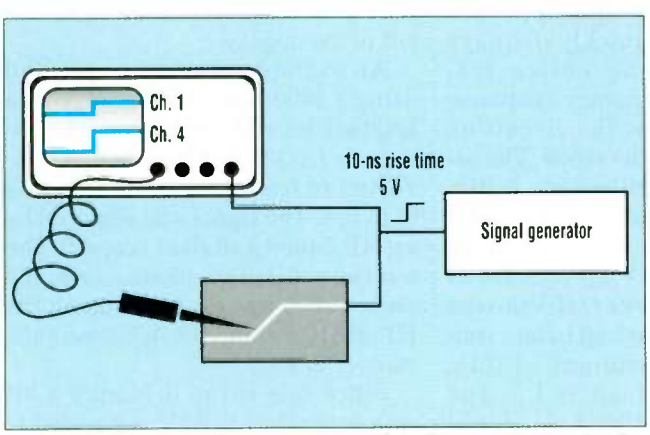
Find Breaks In Pc-Board Traces

Jeff Verive, Tellabs Operations Inc., Boling Brook, Ill.

The following technique for finding the break in a broken trace on an inner or outer layer of a pc-board has been extremely successful in the nondestructive verification of suspected bad boards. At home, the technique also proves successful for locating the discontinuity in a string of holiday lights.

Connect one end of the trace to an ac signal and the probe ground to the signal generator's return lead. The calibration signal on the front of the scope also works well and will eliminate the need for the return lead connection. Adjust the probe's sensitivity for a full-screen waveform and, starting near the signal generator connection, move the scope probe along the area of the trace without making contact, using only capacitive coupling for signal pickup. At the break in the trace, the waveform's amplitude will drop markedly.

In fact, this method of tracking signals is not limited just to finding open traces. You can trace any signal with a suitable risetime. However, you should exercise some caution when using this technique. Following are some additional tips from Don Whiteman, an R&D engineer at HP (Fig. 1).



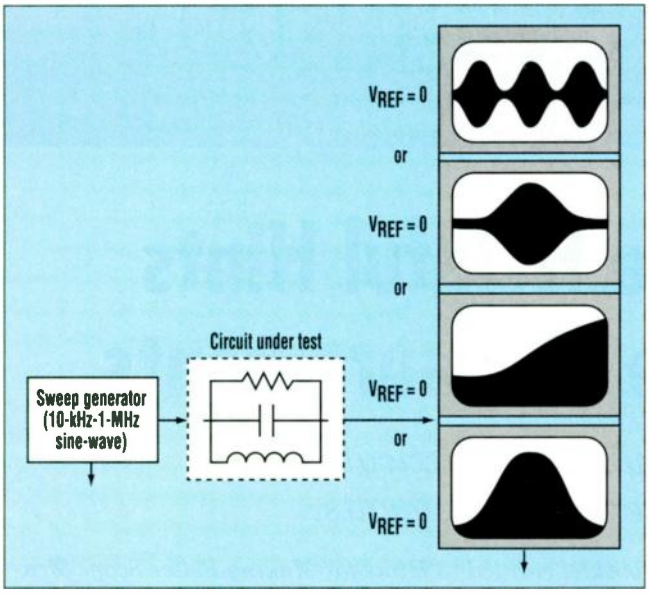
1. When looking for broken traces on a pc-board, the excitation signal should be a fairly high voltage with a fast risetime (for example, 5 V and 10 ns).

Disconnect the power source and excite only the portion of the board where you believe the broken trace might be. This prevents interference from other signals in the vicinity of the fault. And to make the coupled signal easier to measure, the excitation signal should be a fairly high voltage with a fast edge (for example, 5 V with a 10-ns rise time). Also, a 10-ns pulse will provide sufficient coupled energy into the scope probe so that it's not usually necessary to ground the probe.

To avoid the problem of losing trigger due to a change in the signal size as you move the probe, use the excitation signal to trigger the scope. This allows you to move the probe and still maintain the trigger.

If an external excitation signal cannot be used, find a unique portion of the signal exciting the node and use that to trigger the oscilloscope. While other signals will still be coupled into the probe, you should be able to find a suitable timebase range where the extraneous signals do not mask the capacitively coupled signal in the trace you're investigating. You can minimize the effects of extraneous signals by averaging.

You can improve sensitivity by using a probe with a very low tip capacitance, such as the HP 54701A with 0.6 pF at the tip.



2. A digital storage scope can be used to record a circuit's frequency-response curve.

Charting Frequency Response

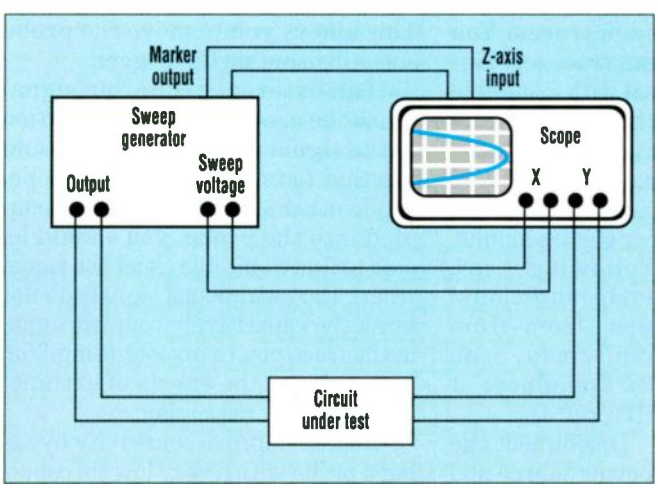
Rick Huffnagle, PSI Industries, Inc., Ivyland, Pa.

A digital storage oscilloscope can provide a simple method for charting the frequency response of a circuit *(Fig. 2)*. Set the scope's sweep speed to 1 sec./div. and the sweep generator to full sweep in 10 seconds, with df/dt = constant (that is, a linear increase in frequency). Apply the generator's output to the circuit under test, and trigger the scope to store on the first edge of the signal. The scope will plot a nearly solid graph of the frequency response of the circuit across the sweep generator's frequency range.

Adjust the scope's volts/div. setting to fit the image, and set the voltage reference as shown in the figure. Now you can print or save the results.

HP's Bob Witte notes that he uses the same technique with a slightly different twist to avoid possible triggering problem that could arise from using the scope's conventional timebase. The variation uses the generator's sweep voltage output and the scope's XY mode. The procedure is discussed in Witte's book, *Electronic Test Instruments*.

His procedure is to connect the swept sine wave of the generator to the input of the circuit under test and the circuit's output to the vertical channel of the oscilloscope, which is operating in the XY mode *(Fig. 3)*. The generator's sweep voltage drives the scope's horizontal axis. As the sweep generator sweeps in frequency, the sweep voltage of the generator ramps up in proportion to frequency, and a plot of the output of the circuit under test appears on the scope display.



3. Using the scope's XY mode for the frequency-response measurement avoids possible trigger problems.

This approach quickly displays the entire frequency response of the circuit on the scope. The oscilloscope is displaying V_{out}, and not the gain (V_{out}/V_{in}). However, if Vin was set up to be a convenient value, such as 1 V, the display could then be interpreted directly as gain.

Averaging Makes Precision Bit-Speed Measurements In Radio Systems

Bill Farmer, retired communications engineer, Rockville, Md.

A digital oscilloscope in the average display mode with center-screen triggering can make precise bit-speed measurements on random or unknown binary data streams–even when the signal is highly contaminated. This technique is helpful for adjusting communications circuits adversely affected by mark (1) or space (0) bias. (Space bias is the enlargement of a space bit at the expense of the mark bit.)

Bit-speed measurements can be difficult because HF propagation conditions result in slowly alternating mark and space bias conditions. What's more, a misaligned receiver or demodulator can introduce fixed amounts of mark or space bias, which further complicates data recovery. It's this natural phenomenon of constantly changing mark and space bias that makes the averaging method of determining bit speed an effective solution.

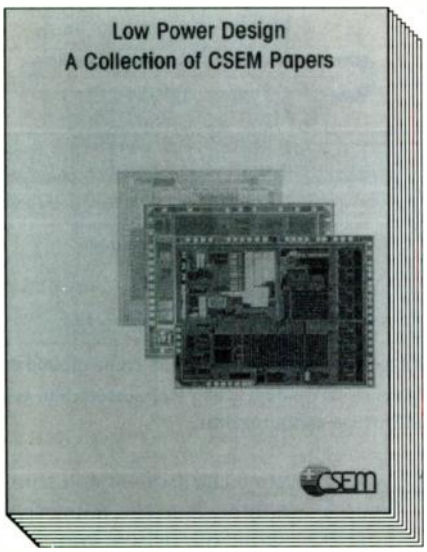
With the scope set to the average mode, the zero-crossing single-bits within a data stream tend to cluster and build up adjacent to the center triggering point, while data bits, which are larger than single bits, tend to average out to the right and left of the display.

An example of this was created using a 9600-bps data signal from a Digitech bit-rate generator. The bit-time is $(\Delta t)/2 = 104\ \mu s$; when converted to frequency ($f = 1/t$), that's 9615 bps. The signal was acquired by an HP 54600A digital scope in the average display mode, and the screen shot was captured using the HP 34810A BenchLink/Scope software *(Fig 4.)*.

Since this setup is simply a bit rate generator directly connected to a scope, no significant real-world distortion shows up. However, in the case of HF communications sig-

LOW-POWER DESIGN

A Collection of CSEM Papers



- *General Tutorial Papers*
- *Digital Circuits*
- *Devices and Analog Circuits*
- *Low-Power Systems*

Over the past decade, minimization of power consumption has become a critically important task in the implementation of electronics systems of all kinds, and especially for portable and battery-powered functions. The requirements for low-power will pervade systems and IC design to an ever increasing extent.

This collection of landmark CSEM (Center Suisse d'Electronique et de Microtechnique SA) papers has been produced as a handy, basic reference book.

Now Available For $125.

LOW-POWER DESIGN

☐ Single order, $125
☐ Multiple order: Quantity: _____ x $125 =

For S & H please add $6 for domestic or $25 for international per book

Amount
_____
_____
_____
Total _____

Mail to:
ELECTRONIC DESIGN
611 Route 46 West
Hasbrouck Heights, NJ 07604
Attn: Jeanne Sico
or fax: 201/393-6073

☐ Master Charge ☐ American Express ☐ VISA ☐ Check (payable to Electronic Design)

Account Name _____ Account # _____

Signature _____ Expiration Date _____

Name _____ Title _____

Company _____

Company Address _____

City _____ State _____ Zip _____

Phone _____ Fax _____ E-mail _____

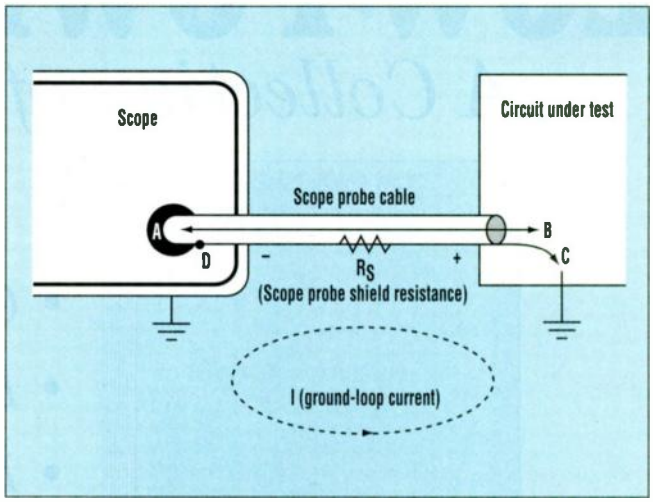
nals, where the transmission medium becomes highly contaminated, the percentage of distortion increases significantly.

A good example is an HF, 75 bps frequency shift keyed (FSK) signal displayed after being received off the air and demodulated into its component mark and space dc levels. The scope's delayed-sweep speed feature of the scope was used to get a closer view when adjusting the cursors for final measurement.

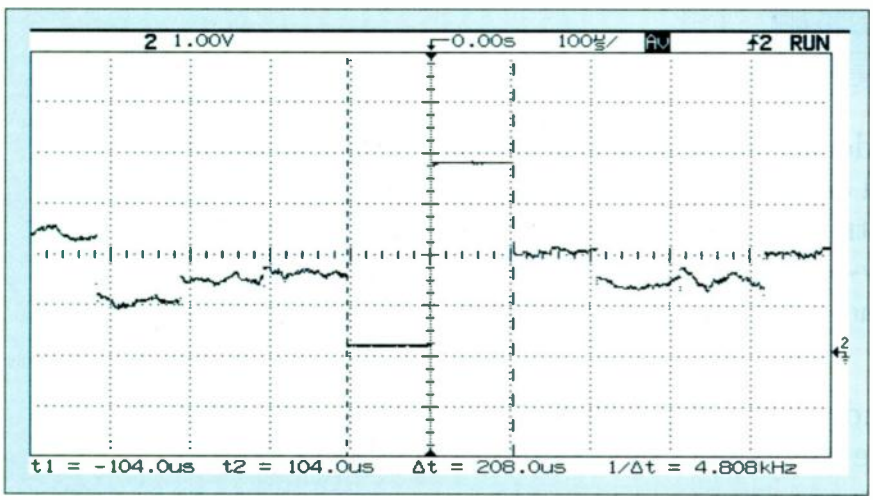
The cursors were placed over the half-power points of the leading/trailing edges of the centered mark and space bits *(Fig. 5)*. Notice how these edges are now nearly diagonal lines as opposed to the vertical lines in the undistorted signal. Even with a distortion rate of 13%, which is typical of good HF FSK signals, you can measure the bit speed accurately. The bit-time is $(\Delta t)/2 = 13.3$ ms, which translates to a frequency of 75.18 bps.

The signal in this example was selected because it is a known synchronous military crypto-covered FSK link that necessarily holds very tight bit-speed tolerances. This emphasizes the point that, in spite of signal distortion, you can easily determine accurate and repeatable bit speeds using the scope's center-triggering and the display average mode. The delayed sweep mode enhances the accuracy of the measurement.

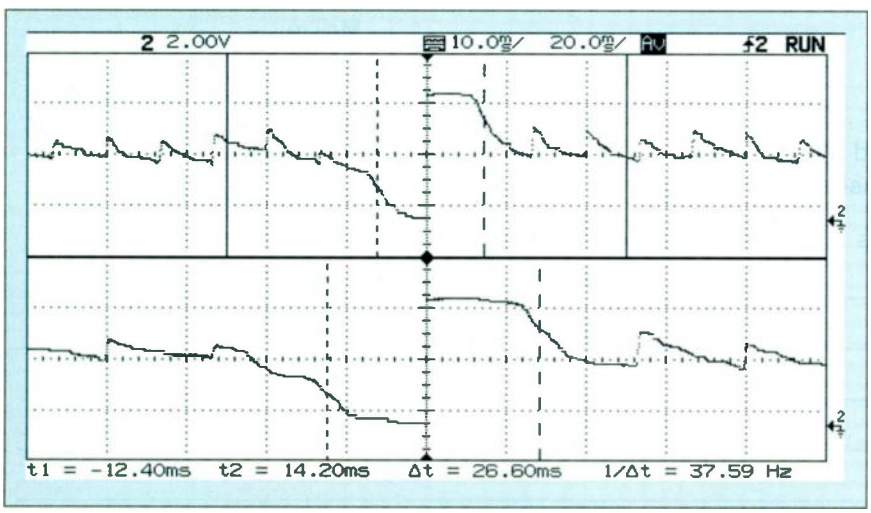
Remember that averaging is a mode available only on digital oscilloscopes. Also, averaging will slow the edges on jittering waveforms, as is apparent in Fig. 5.



6. The difference in potential between the scope ground and the circuit-under-test ground can create a group-loop current that causes noise that interferes with scope measurements.



4. This clean 9600-bps data signal direct from a bit-rate generator shows how the zero-crossing single bits tend to cluster adjacent to the center triggering point while data bits tend to average out to the right and left.



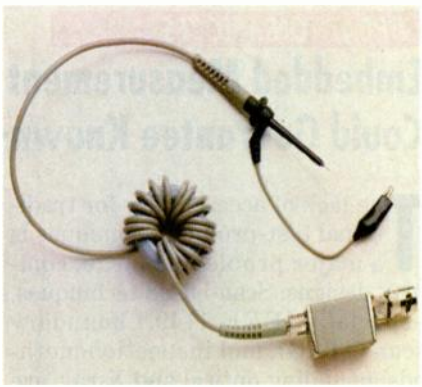
5. Even in the presence of distortion, as shown in this real-world HF, frequency shift keyed communications signal, the digital scope in the averaging mode can accurately measure bit speed.

Check For, And Reduce, Ground-Loop Noise

Joe Diederichs, Lake Stevens Instrument Div., Hewlett-Packard Co., Everett, Wash. (with credit to Jim Pietsch at HP's Microwave Instrument Div., Santa Rosa, Calif.)

It's important to look out for ground-loop noise when making oscilloscope measurements. The problem is that the common side of the scope input is at chassis ground, making the ground in the circuit being measured chassis ground as well (through the test probe and the scope). This setup can introduce noise into the measurement because of the difference in the potential of the circuit ground and the scope ground.

The scope probe shield cannot make these two potentials the same because a ground loop has been formed by the probe's cable shield and the "green-wire" grounds in the ac connections of the scope and the circuit under test. The size of the ground-



7. Wrapping the scope lead around a toroid made of high-permeability ferrite material raises the inductive impedance of the lead's shield and reduces ground-loop current.

loop current flowing in the scope probe shield depends on the potential difference between the two grounds and the resistance of the shield *(Fig. 6)*. This potential difference shows up in series with the voltage being measured in the circuit under test.

Fortunately, scope users can check for this problem by simply "measuring ground" in the circuit under test first. To do so, connect the scope probe's signal input and ground to the circuit ground. In this configuration, any measurement other than zero is ground-loop noise.

If this ground measurement does indicate noise is a problem, a common-mode choke may help. When I run into this problem, I use a 3-1/2-in. diameter toroid made of high-permeability ferrite material to raise the inductive impedance of the scope probe shield and impede the flow of the ground loop circuit. Simply wrap the scope probe cable around the toroid a number of times *(Fig. 7)*.

The common-mode choke will have a low frequency cutoff that depends on the core material and the number of times the scope probe cable is wrapped around the choke. Below this cutoff, the choke's effectiveness is diminished. Therefore, rejecting lower frequency components requires more turns of the scope probe cable around the toroid, or a higher-permeability toroid.

How Valuable	Circle
Highly	580
Moderately	581
Slightly	582

UPDATE ON ASIC TEST

Embedded Measurement Objects On ASICs Could Guarantee Known-Good Die For MCMs

The lack of accessibility for traditional test-probing techniques is a major problem in large, complex designs. Scan-based techniques, especially IEEE-1149.1 boundary scan (JTAG), and inspection methods, including optical and X-ray, are attempts to get around this limitation. The problem is particularly acute for manufacturers of multichip modules (MCMs), where the availability of known-good die are critical to success.

One solution may be to embed test and measurement structures onto the die itself. This approach allows both parametric and vector-based testing. In its initial development work, Tektronix Inc. embedded timing analyzers and analog probes in various configurations into a RISC processor.

The work is being done under a contract from the U.S. Defense Advanced Research Projects Agency (DARPA). Phase I of the project involved the demonstration of the basic technology of embedding the test structures. Tektronix selected LogicVision Inc., San Jose, Calif., to jointly develop the technology after the initial demonstration. Phase II involved the incorporation of the test structures into LogicVision's design object library. These objects, together with the associated LogicVision automation tools, will be used to customize the test objects and embed them into ASIC designs.

Currently underway, Phase III will create software needed by potential customers to actually use the embedded test objects. That will include the macro insertion software from LogicVision and the test execution platform and framework from Tektronix.

The Combination Of At-Speed Testing And Burn-In At The Wafer Level Ensure Known-Good Die And Greatly Reduce MCM Production Costs.

"The objective of this program is to develop a cost-effective method of providing known-good die for use in multichip modules," notes Arnold Frisch, manager of Tektronix's Integrated Instruments Laboratory and chief investigator for the DARPA contract. "The idea is to fully test the chip at the wafer level, so that when you separate the individual dice you know they're good." Frisch says the principle focus is on ASICs rather than very high-volume ICs.

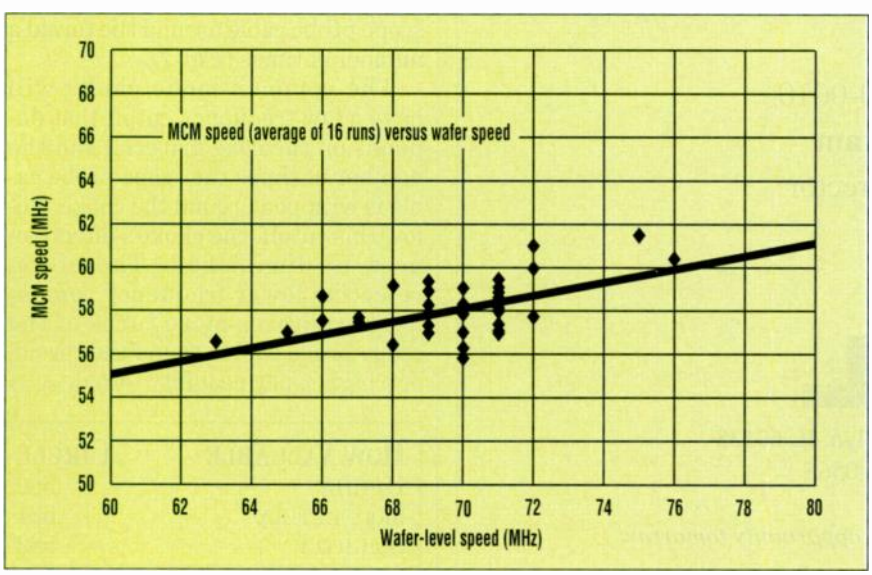
Besides the goal of embedded at-speed testing, the joint project includes development of technology for burn-in at the wafer level and for post-assembly diagnosis. The combination of at-speed testing and burn-in at the wafer level greatly reduce MCM production costs.

Tests were run to determine whether the new technology could accurately discern while the dice were still on the wafer the maximum speed at which the processors could run in the assembled MCMs. The processor used in the project was a RISC device, called Cypris, developed by Lockheed-Martin for cryptographic applications. It included a boundary-scan test-access port controller. Two timing analyzers and two embedded analog probes were added, which resulted in a 3% area overhead.

Tektronix performed the automated tests and sent the results to the monitoring government agency. All the reticles were then sent to an independent third party, says Frisch. A number of them were placed on MCMs and shipped back to Tektronix, which ran a similar set of tests on the assembled modules and sent those results to the government. After the government had both sets of results, the third party told the agency which chips were used on which MCMs, so the results could be compared *(see the figure)*.

"The tests show that we have a very accurate method of correlating wafer-level speed to the speed of the final assembly," says Frisch. Generally, the chips ran slower in the module, but that was expected due to factors like time-delay loading and interconnect loading, he says. Frisch also notes that neither Lockheed-Martin nor an independent testing laboratory could test the chips at a speed faster than 52 MHz, even though every chip ran faster than that.

Although the technique is not aimed at very high-volume chips,



there's no fundamental reason that it can't be used on them. Frisch says the project hasn't characterized the cost issues involved in testing very high-volume designs, but that the specific tests run on the demonstration chip might be too time-consuming for such devices.

The new test technology is fundamentally different than conventional built-in self-test (BIST), says Frisch. BIST gets its test coverage by running a fairly complete set of pseudorandom vectors generated by a state machine. But while BIST can functionally test a block of a chip at speed, Frisch says, it's difficult to get good coverage on the whole chip, especially a large one, because it may include multiple clock domains and speeds. The new embedded test technology, on the other hand, actually converts simulation data into a test program. It also can precisely measure timing, propagation delays, and analog voltages.

"We feel this embedded technology development is very promising," says Balaji Krishnamurthy, vice-president of central engineering for Tektronix's Measurement Business Div. "IC technology is rapidly advancing and devices are becoming increasingly more complex and tougher to access. We're exploring technologies that will measure those areas that are inaccessible by conventional methods. The development work we do with LogicVision in phases II and III of the contract will lay the foundation for a very successful embedded test and measurement methodology."

Phase III was scheduled to begin last November and will run for about a year. After that, says Frisch, the companies would be in a position to consider commercialization of the technology.

"With our recent introduction of memBIST-XT, we've taken BIST beyond the IC to the system level," said Vinod Agarwal, president and CEO of LogicVision. "Now, as a shared vision with Tektronix and a natural evolution of our BIST technology, we intend to go beyond BIST to provide complete automated solutions for embedded test, measurement, and diagnosis."

JOHN NOVELLINO

UPDATE ON WAFER PROBING

Durable Membrane-Based Technology Enhances Performance And Reliability Of Wafer Probe Cards

The conventional approach to wafer probing for IC production testing uses a needle-based probe card that, unfortunately, is difficult to handle without causing damage, requires notoriously high periodic maintenance, and is running out of bandwidth for leading-edge devices. An alternative technology uses a membrane probe card that is an improvement in every respect. It needs almost no maintenace and features a better than 2-GHz bandwidth.

The new membrane probe cards were developed jointly by Advantest Corp., Buffalo Grove, Ill., and Packard-Hughes Interconnect Co., Irvine, Calif., in response to a request from Fujitsu Microelectronics Inc.'s Gresham Manufacturing Div., Gresham, Ore., which produces 4-Mbit DRAMs. The card uses a membrane based on Packard-Hughes' patented Gold Dot technology. Advantest America's Custom Design Engineering Group customizes the technology to meet specific customer application requirements. Advantest will be the exclusive distributor worldwide for the memory automatic test equipment (ATE) market. In Japan, it will also be the exclusive distributor for logic ATE.

The membrane probe assembly employs two printed-circuit boards. The probe card printed-circuit board transmits test signals between the test system and the membrane probe assembly *(Fig. 1)*. A conductive elastomer supplies the path between the probe card printed-circuit board and the membrane, which is a flexible polymide printed-circuit board.

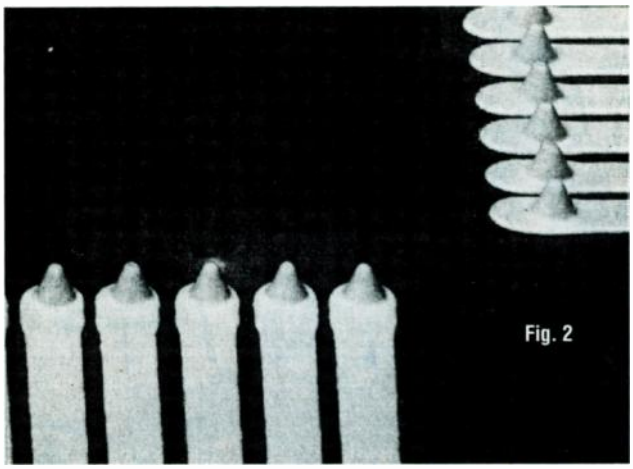


Fig. 2

Contact to the die wafer pads is actually made by bumps on the membrane *(Fig. 2)*. The contact force is determined by a mechanical spring and is transfered to the bumps through a glass pressure plate with an elastomeric backing. The bumps are at the end of traces that deliver a controlled impedance of 50 Ω right to the wafer pads. The resulting bandwidth of over 2 GHz helps increase device yield.

Another important advantage of the membranes is that, unlike needle probe cards, they are self-planarizing so they require no periodic maintenance for realignment. Advantest specifies the cards for greater than 250,000 touchdowns without degradation. Planarity (bump to bump) is specified at 2 µm and pattern stability (over temperature) is 25.4 µm. The contact bump height is 40 µm, and the bump diameter is 18 µm.

"With membrane probe cards, maintainability is excellent, requiring little operator intervention and no need for realignment, as with needles," notes Keith Lee, manager of Advantest's Custom Design Engineering Group. "We've found that membrane is a very viable probe technology and that it is effective in a high-production wafer environment."

After initial trials, a report by G. Gary Aalseth, a test engineer at Fujitsu Microelectronics, said that, "up to this point in the evaluation, the membrane probe card is performing far superior to the needle card in the same application." At that time, the membranes had made 80,000 touchdowns in production use. The report said more testing would be needed to determine their actual lifetime, which would, of course, affect the cost of using the technology.

The first trials used a membrane designed to mimic the existing needle card, which made direct comparisons easier. But the report said this arrangement may not have been the best for the new card. As a result, additional improvements might be possible by optimzing the device-under-test layout and circuit design for the membrane technology.

The report also commented on the membrane's durability, noting that, "damage from equipment malfunction or human error is hugely reduced." It cited an example in which a membrane during prober setup was inadvertantly subjected to a 1200-µm overdrive while being dragged more that 25 mm across the surface of a wafer. The wafer was destroyed, but the membrane suffered no damage and was returned to use in the trials. A needle card treated the same way would have been a total loss, according to the report.

JOHN NOVELLINO

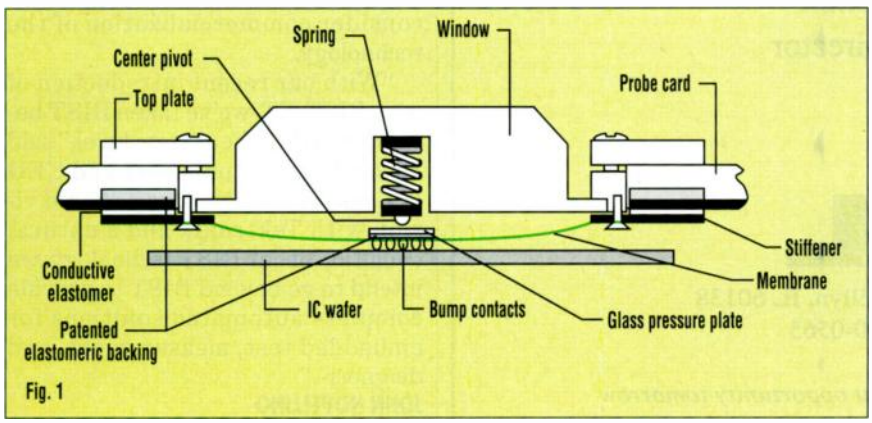


Fig. 1

Pocket-Size Emulator Handles 3-V Or 5-V Am186ER Designs

The SuperTAP Am186ER is a pocket-size emulator for systems employing the AMD Am186ER processor. The unit is self-contained and needs only to be connected to the target device. No hardware configuration is required, nor any change of probe tips or internal boards. The

unit automatically adapts to either 3- or 5-V systems.

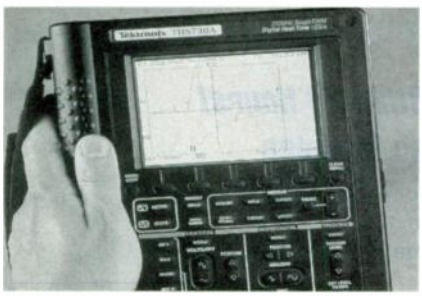
The SuperTAP supports 40-MHz bus speeds and runs internally if no target hardware is available. It uses a dual-processor architecture, so when the operator sends a command to the emulator, the target processor will not stop emulation to interpret information or execute other commands. Also, the emulator allows users to upload, trigger, and display trace, as well as modify event triggers without stopping the target processor. The SuperTAP comes with a 64k real-time trace subsystem, 1 Mbyte of overlay memory, an adapter, serial and high-speed communication capability, a debugger, and a linker/locator package for $9995. Delivery is in six weeks.

Applied Microsystems Corp.
P.O. Box 97002
Redmond, WA 97073-9702
(206) 882-2000
e-mail: info@amc.com
Internet: http://www.amc.com
CIRCLE 577

JOHN NOVELLINO

200-MHz, 1-Gsample/s Model Joins Family Of Handheld Digital Scopes

The latest in a family of handheld digital oscilloscope/multimeters, called the THS730A, features a 200-MHz bandwidth and a 1-Gsample/s digital real-time sampling rate. Another new model, the THS720P, offers harmonic measurement and motor and external



triggering capabilities for power electronics applications. Both instruments employ the proprietary Isolated Channel Architecture, which ensures the safety of both the user and the circuit and the fidelity of the bandwidth.

The THS730A has high-speed dual-channel/dual-digitizer measurement and triggering capabilities for quick timing-error detection. The unit supplies comprehensive and advanced triggering features like video trigger (line count and field select), as well as pulse, delay, and external triggering. It has a glitch-capture function and makes dB and dBm measurements. Two 200-MHz P6117 probes come with the THS730A.

The THS720P has a 100-MHz bandwidth and a 500-Msample/s digitizing rate. It offers harmonic measurement up to the 31st harmonic and has motor triggering capability for detecting motor control voltages. It comes with high-voltage probe able to measure 1000 V rms potential difference between the probe tip and the reference.

The THS730A and the THS720P are available from stock from authorized distributors for $2995.

Tektronix Inc.
(800) 479-4490, action code 723;
http://www.tek.com/measurement
CIRCLE 578

JOHN NOVELLINO

LATCHED, SOT VOLTAGE MONITOR PREVENTS BATTERY DEEP DISCHARGE

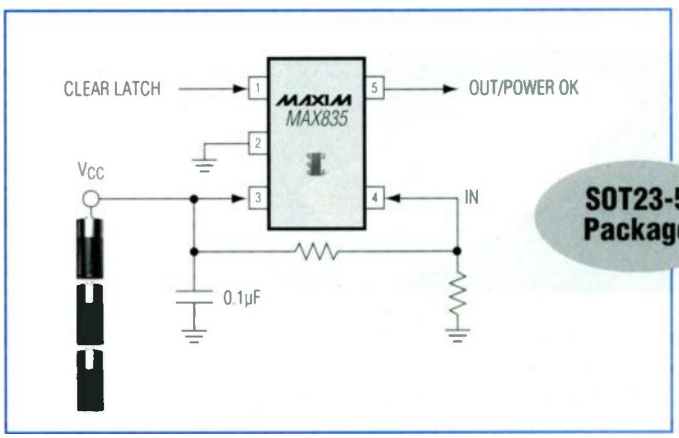
Prevent deep discharge of NiCd, NiMH, and lead-acid batteries by using the MAX834/MAX835 to disconnect the load when the battery voltage has reached the minimum safe discharge voltage.

The MAX834/MAX835 voltage monitors include a latched output that prevents a battery-powered system from being turned back on as the battery voltage recovers to a higher value after the load has been disconnected. When the battery voltage drops below the precision 1.25% threshold, the output is latched low, and stays low until reset by the Clear Latch input.

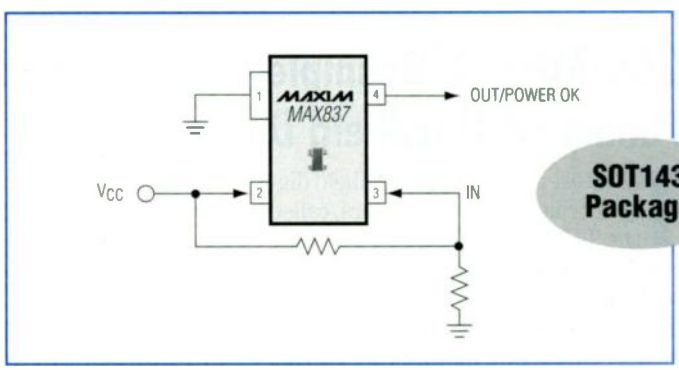
The MAX836/MAX837 voltage monitors are similar to the MAX834/MAX835, except they come in a 4-pin SOT143 package and do not have a latched output.

- **Precision ±1.25% Voltage Threshold**
- **<2.5µA Supply Current**
- **Latched Output (MAX834/5); Once Low, Stays Low Until Cleared**
- **Small Package:**
  SOT23-5 (MAX834/5)
  SOT143 (MAX836/7)
- **Guaranteed Over Temperature**

SIMPLE, SMALL, LOW POWER & LOW COST



The MAX835 has a push/pull output while the MAX834 has an open-drain N-channel output driver.



The MAX836 and MAX837 voltage monitors come in a 4-pin SOT package. They have 5mV of hysteresis and no latch.

FREE* µP Supervisory Design Guide – *Sent Within 24 Hours!

Includes: Data Sheets and Cards for Free Samples

CALL TOLL-FREE 1-800-998-8800 for a Design Guide or Free Sample
For Small-Quantity Orders Call (408) 737-7600 ext. 6380
6:00 a.m. – 6:00 p.m. Pacific Standard Time
http://www.maxim-ic.com

MasterCard® and Visa® are accepted for evaluation kits and small-quantity orders.

ISO 9001

MAXIM

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086, (408) 737-7600, FAX (408) 737-7194.

Distributed by Allied, Arrow, Bell, CAM RPC, Digi-Key, Elmo, Hamilton Hallmark, Nu Horizons, and Zeus. Distributed in Canada by Arrow.

Circle No. 120 - For U.S. Response
Circle No. 121 - For International

Circle 520

Single Pot Swings Amplifier Gain Positive Or Negative

S.J. PRASAD
National Semiconductor Corp., MS A1-555, 2900 Semiconductor Dr., Santa Clara, CA 95052-8090; (408) 721-7178; fax (408) 721-5100

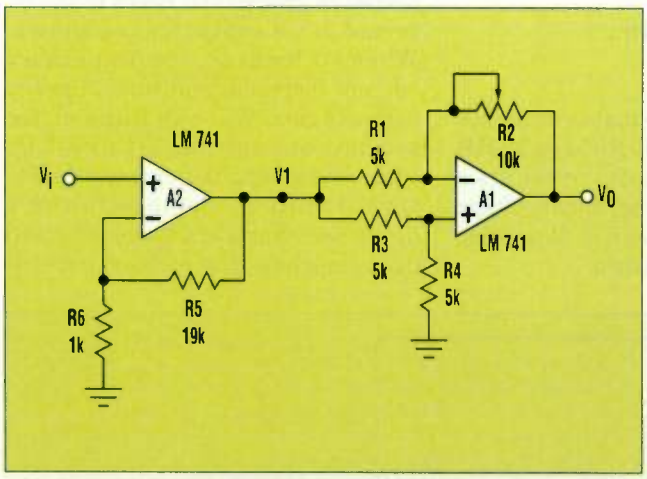
It comes in handy to have a gain block with a gain that can be varied smoothly from positive to negative with a single potentiometer. The circuit shown accomplishes this function with R2 *(Fig. 1)*. Op amp A1 is configured as a differential amplifier with both inputs tied together. Op amp A2 functions as a buffer. With R1=R3=R4=R=5k, the gain of the differential amplifier is given by:

$$A_{V_i} = \frac{V_O}{V_i} = \frac{1}{2}\left(1 - \frac{R2}{R}\right)$$

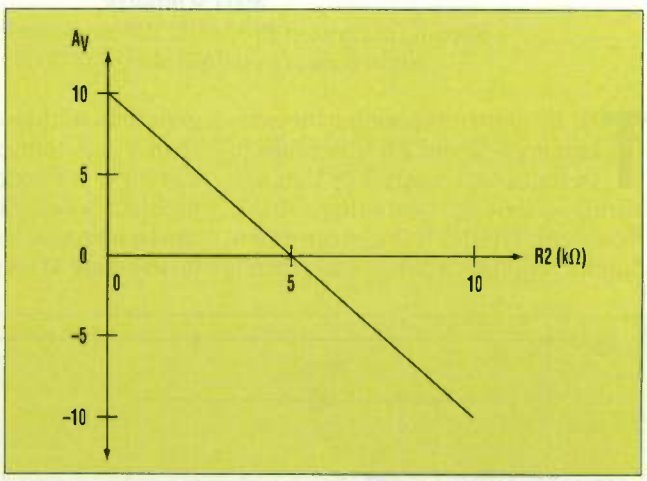
With the buffer amplifier gain of 20, the overall gain of the amplifier is given by:

$$A_V = \frac{V_O}{V_i} = 10\left(1 - \frac{R2}{R}\right)$$

By using a ten-turn potentiometer, the gain can be varied from positive to negative *(Fig. 2)*.



1. Amplifier gain varies linearly in this circuit with adjustment of potentiometer R2, providing positive and negative gains.



2. The R2 gain plot demonstrates the smooth variation from positive to negative gain in this gain block circuit.

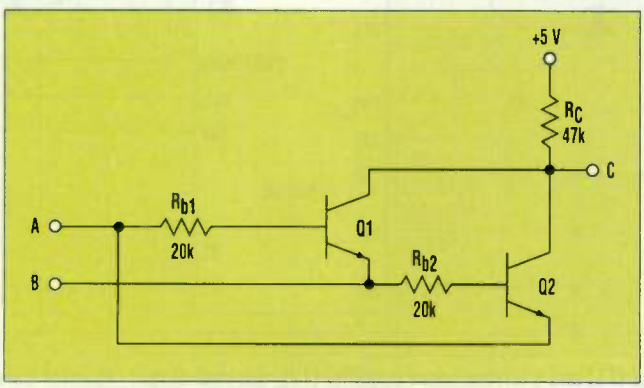
Circle 521

Inexpensive Two-Transistor XOR Gate

RON SWENSON
Digitech, Harman Music Group, 8760 South Sandy Pkwy., Sandy, UT 84070.

XOR gate chips sometimes can be prohibitive in applications because of cost or size. One alternative is the two-transistor combination shown, which forms an inverting XOR gate for just pennies *(see the figure)*. The set of conditions are simple: If both inputs A and B are low, both Q1 and Q2 are off and the output at C is high. Likewise, if both inputs are high, both transistors are turned off and again the output C is high. When A is high and B is low, Q1's base-emitter junction is forward-biased. This turns on Q1, pulling the output low, while Q2's base-emitter junction is reverse-biased.

The last condition is B high and A low. In this state, Q1's base-to-emitter junction is reverse-biased, but Q2 is forward-biased. This turns on Q2 and pulls the output low. The sink and source currents driving the two-transistor gate are very low when using the values shown. Even though the signals are driving the emitters of transistors, when the base and emitter are at the same potential (A and B are both high or both low), no current flows. When one of the transistors is



This two-transistor setup creates an inexpensive XOR gate.

turned on, the emitter drive must only be able to sink the base plus collector currents. This current will be approximately:

$I_e = I_b + I_c$

where:

$I_b \approx (V_H - V_{BE})/R_b$ and $I_c \approx (V_{cc} - V_{sat})/R_c$.

From this, V_H = TTL High output level = 3 V; V_{BE} = forward-biased base-emitter voltage ≈ 0.7 V; V_{CC} = 5 V typical; and V_{sat} = 0.2 V typical.

Also, for this example, R_b = 20k and R_c = 47k. Thus, $I_c \approx 215\ \mu A$.

VOTE!

Read the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a $300 Best-of-Issue award.

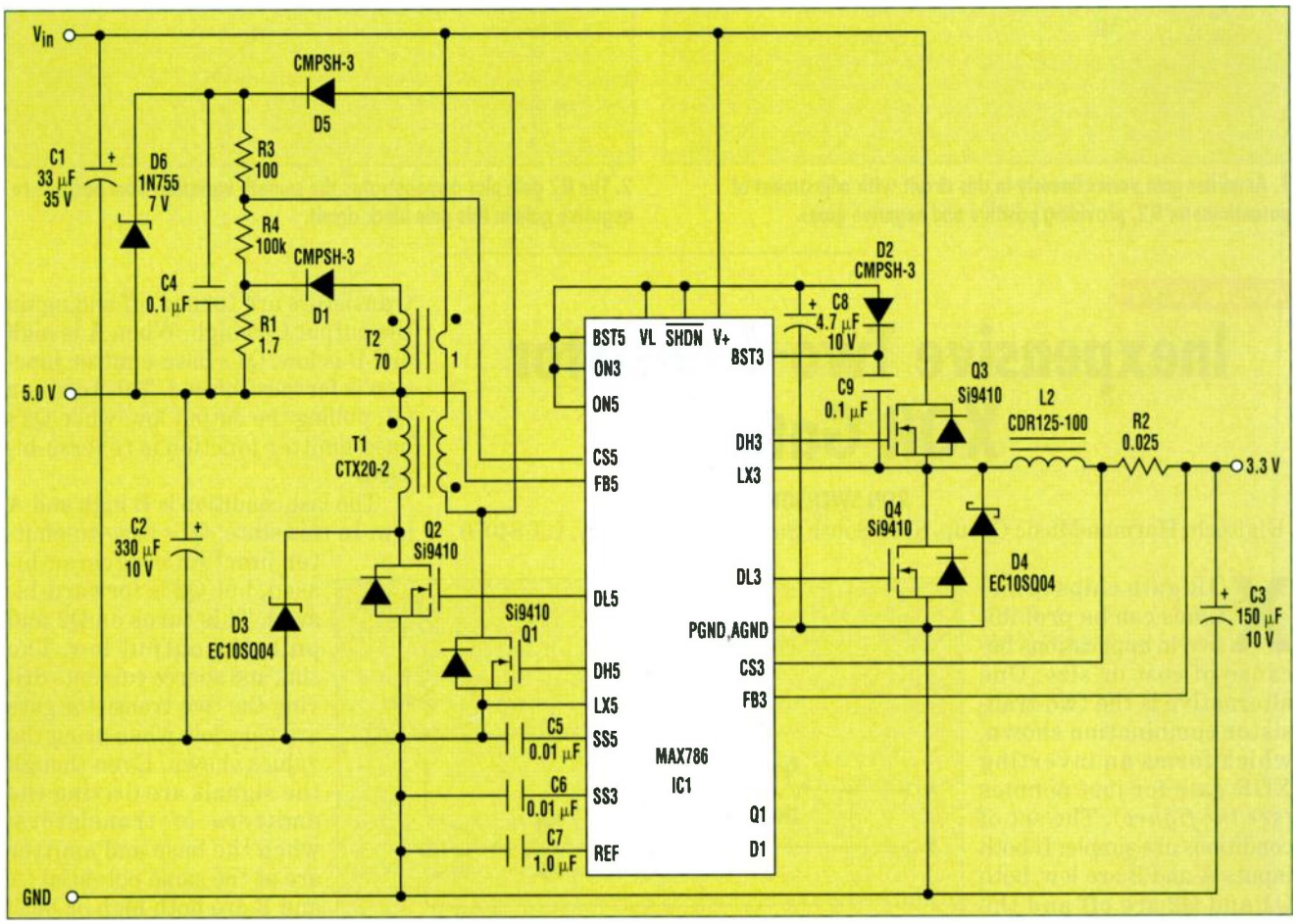
Circle 522

Derive 5 and 3 V From 4-Cell Input

MATT SCHINDLER
Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086; (408) 737-7600.

The IC shown is popular for generating 5 V and 3.3 V because it includes two controllers that are highly efficient (typically >90%). However, the IC has a step-down (buck) topology that usually can't generate voltages equal to or higher than V_{in}. A four-cell NiCd or NiMH battery, for example, presents a problem because its terminal voltage can be above or below 5 V, depending on the state of its charge.

This problem can be solved by designing in a flyback transformer, which allows V_{in} to range from 4 V to 7 V—above or below the regulated 5-V output *(Fig. 1)*. To ensure a proper gate drive to the external switching MOSFET (Q1), LX5 should be connected to ground and BST5 to the internal 5-V supply (V_L) as shown. When Q1 turns on, the T1 primary current increases and stores energy in the T1 core. When Q1 turns off, the synchronous-rectifier MOSFET Q2 turns on and enables current flow to the 5-V output. Compared with a diode rectifier, Q2's lower forward drop improves the conversion effi-



1. By employing a flyback transformer (T1) and a current-sense amplifier (T2), this dual-output regulator can accept input voltages above or below the regulated 5-V output, making it ideal for use in four-cell NiCd or NiMH battery-powered applications.

NEW ERA AMPLIFIERS

WOW! **DC to 8GHz** *(up to +18dBm output)*

From **$1.19** (1000 qty.)

Mini-Circuits ushers-in a new era of technology and economy with ERA monolithic GaAs amplifiers. Just check the specs! These surface mount and drop-in amplifiers cover your applications to 8GHz with higher gain, more output, and flatter response. Characterized with S-parameter data, these amplifiers are very easy to use. Simply sketch an interconnect layout, and the design is done. And ERA's are engineered with wider bandwidths to eliminate your need for costly compensation networks and extra gain stages. So, review your present design and replace with Mini-Circuits new ERA technology. Lower overall cost, wide bandwidth stability, and lots to...*gain!*

Mini-Circuits...we're redefining what VALUE is all about!

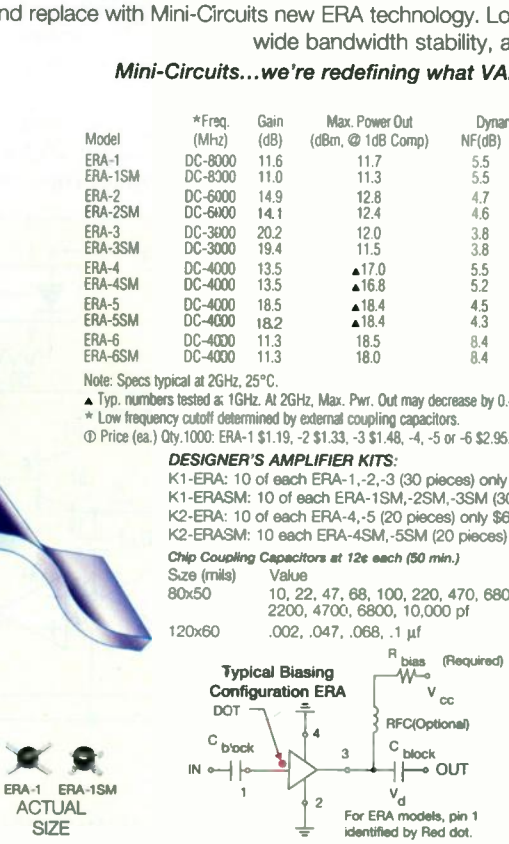
Model	*Freq. (Mhz)	Gain (dB)	Max. Power Out (dBm, @ 1dB Comp)	Dynamic Range NF(dB)	Dynamic Range IP3(dBm)	①Price $ ea. (10 Qty.)
ERA-1	DC-8000	11.6	11.7	5.5	26	1.80
ERA-1SM	DC-8000	11.0	11.3	5.5	26	1.85
ERA-2	DC-6000	14.9	12.8	4.7	26	1.95
ERA-2SM	DC-6000	14.1	12.4	4.6	26	2.00
ERA-3	DC-3000	20.2	12.0	3.8	23	2.10
ERA-3SM	DC-3000	19.4	11.5	3.8	23	2.15
ERA-4	DC-4000	13.5	▲17.0	5.5	▲32	4.15
ERA-4SM	DC-4000	13.5	▲16.8	5.2	▲33	4.20
ERA-5	DC-4000	18.5	▲18.4	4.5	▲33	4.15
ERA-5SM	DC-4000	18.2	▲18.4	4.3	▲32	4.20
ERA-6	DC-4000	11.3	18.5	8.4	36	4.15
ERA-6SM	DC-4000	11.3	18.0	8.4	36	4.20

Note: Specs typical at 2GHz, 25°C.
▲ Typ. numbers tested at 1GHz. At 2GHz, Max. Pwr. Out may decrease by 0.4dB & IP3 by 3 to 4dB.
* Low frequency cutoff determined by external coupling capacitors.
① Price (ea.) Qty.1000: ERA-1 $1.19, -2 $1.33, -3 $1.48, -4, -5 or -6 $2.95. SM option same price.

DESIGNER'S AMPLIFIER KITS:
K1-ERA: 10 of each ERA-1,-2,-3 (30 pieces) only $49.95
K1-ERASM: 10 of each ERA-1SM,-2SM,-3SM (30 pieces) only $49.95
K2-ERA: 10 of each ERA-4,-5 (20 pieces) only $69.95
K2-ERASM: 10 each ERA-4SM,-5SM (20 pieces) only $69.95

Chip Coupling Capacitors at 12¢ each (50 min.)

Size (mils)	Value
80x50	10, 22, 47, 68, 100, 220, 470, 680, 1000, 2200, 4700, 6800, 10,000 pf
120x60	.002, .047, .068, .1 µf



ACTUAL SIZE

Mini-Circuits®

P.O Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500 Fax (718)332-4661 *INTERNET* http://www. minicircuits. com

US 134 INT'L 135 CIRCLE READER SERVICE CARD

For detailed specs on all Mini-Circuits products refer to • 740- pg. HANDBOOK • INTERNET • THOMAS REGISTER • MICROWAVE PRODUCT DATA DIRECTORY • EEM

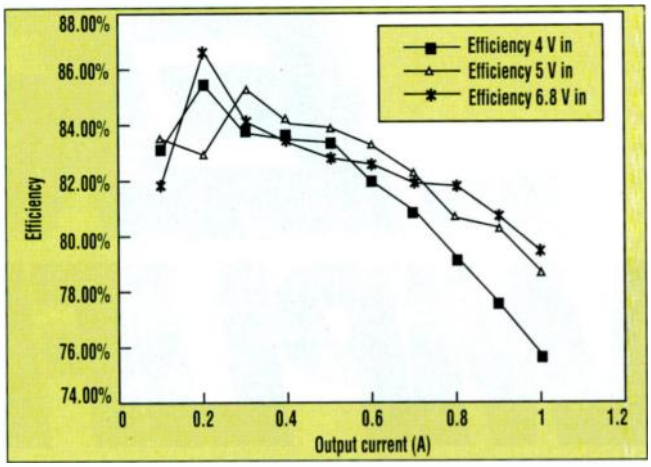
CUSTOM PRODUCT NEEDS...Let Our Experience Work For You.

F 214 Rev B

ciency.

For flyback circuits, I_{out} flows only when the rectifier (synchronous in this case) conducts. Yet, IC1 is a current-mode buck regulator for which I_{out} must be sensed while Q1 is on. The current-sense transformer T2 therefore measures the T1 primary current when Q1 is on, steps down the result with a 70:1 turns ratio, and develops a voltage across resistor R1.

To ensure that the synchronous rectifier Q2 remains on while Q1 is off, a simple charge pump (C4 and D5) and voltage divider (R3 and R4) provides a slight offset to the current-sense signal. Thus, Q2 remains on because the IC doesn't detect zero output current. V_{out} is regulated to 5 V, ±5%, and the maximum I_{out} is 1 A over the entire V_{in} range. The current in T1 is approximately the sum of the input and output current. Consequently, as V_{in} increases, I_{in} decreases, allowing an increase in the available I_{out}. The efficiency varies with V_{in} and I_{out} *(Fig. 2)*.



2. Supply efficiency for the 5-V output in Figure 1 is observed to be 80-85% (typical) across the operating range.

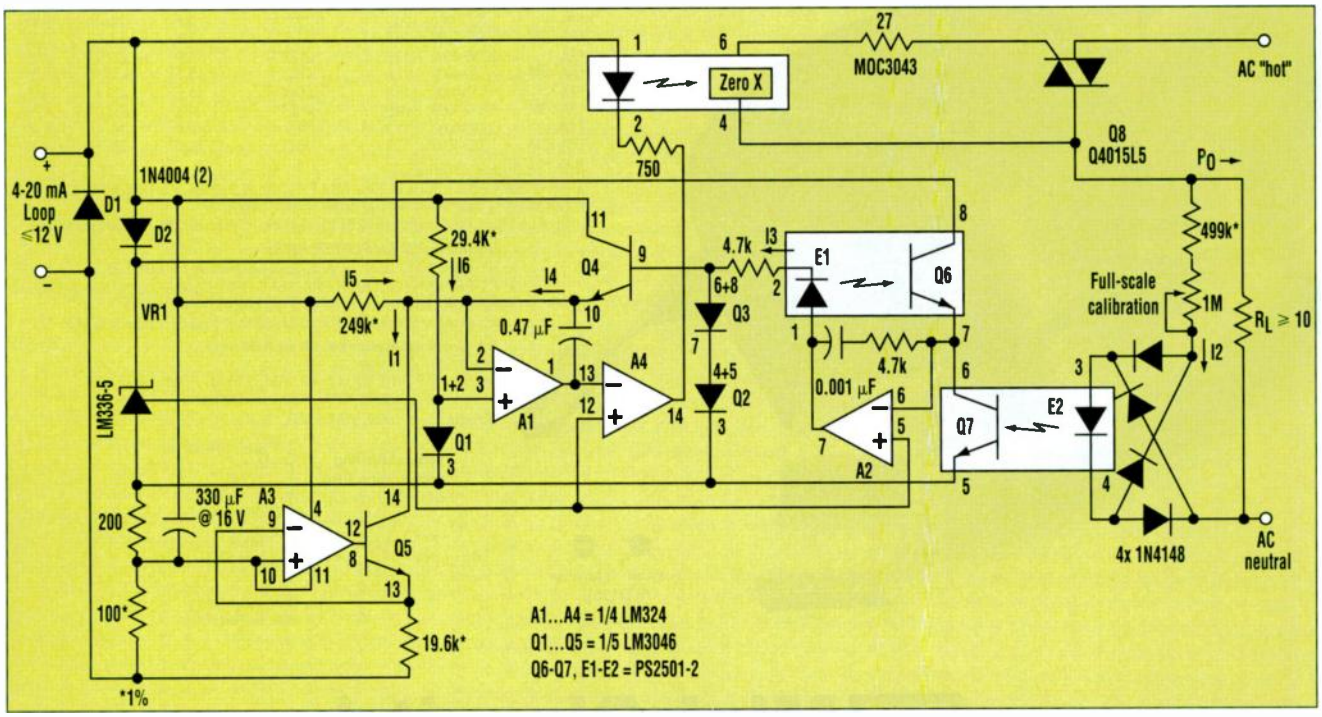
Circle 523

Linear True-Mean-Square Temperature Controller

W. STEPHEN WOODWARD
Venable Hall, CB3290, University of North Carolina, Chapel Hill, NC 27599-3290; Internet: woodward@net.chem.unc.edu.

Precision temperature control with large (>1 kW) heaters driven directly from the ac mains is simple and efficient, but sometimes problematic. If, for example, a standard time-proportioned on/off cyclic heating technique is used for power control, then the relationship between temperature controller command output (e.g., 4-to-20-mA current loop) and heat delivered will be nicely linear. But the on/off cycle period (often several seconds) may be so long compared to the thermal time constant of a fast-thermostatted system that unacceptable temperature ripple will result.

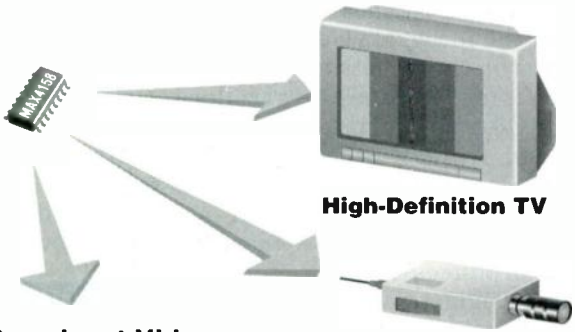
If, instead, a thyristor conduction-angle scheme is used, temperature ripple will be avoided, but heat deliv-



True-mean-square power is output to the heating elements in direct proportion to a 4-to-20-mA current-loop control input. Line-voltage variations and thermal ripple are cancelled, providing tightly-regulated delivered power to the load.

350MHz VIDEO MUX/AMPS PIXEL SWITCH IN 20ns

Drive 50Ω Coax, 0.1dB Gain Flatness of 130MHz



High-Definition TV

NO GLITCH WHEN YOU SWITCH!

Surveillance Video

- Broadcast Video
- High-Speed Signal Processing
- Video Signal Multiplexing
- Workstations
- Multimedia Products

The combination of fast input-signal multiplexing, excellent 0.1dB gain flatness, and low differential gain and phase errors make these mux/amps ideal for any broadcast-quality application. These amplifiers typically consume less than 100mW and are capable of driving a 50Ω load to ±2.5V.

Select the Ideal Video Mux/Amps for Your High Performance Video Application

PART	# OF CHANNELS	MINIMUM STABLE GAIN (V/V)	-3dB SMALL SIGNAL BANDWIDTH (MHz)	0.1dB GAIN FLATNESS (MHz)	DIFFERENTIAL GAIN/PHASE (%/°)	CHANNEL SWITCHING TIME (ns)	SLEW RATE (V/µs)	PACKAGE
MAX4158	2	1	350	100	0.01/0.01	20	700	8-pin SO, µMAX
MAX4159	2	1	350	100	0.01/0.01	20	700	14-pin SO, 16-pin QSOP
MAX4258	2	2	250	130	0.01/0.02	20	1000	8-pin SO, µMAX
MAX4259	2	2	250	130	0.01/0.02	20	1000	14-pin SO, 16-pin QSOP

FREE* Op Amp/Comparators Design Guide – *Sent Within 24 Hours!

Includes: Data Sheets and Cards for Free Samples

CALL TOLL-FREE 1-800-998-8800 for a Design Guide or Free Sample
For Small-Quantity Orders Call (408) 737-7600 ext. 6380
6:00 a.m. – 6:00 p.m. Pacific Standard Time
http://www.maxim-ic.com

MasterCard® and Visa® are accepted for evaluation kits and small-quantity orders.

ISO 9001

MAXIM

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086, (408) 737-7600, FAX (408) 737-7194.

Distributed by Allied, Arrow, Bell, CAM RPC, Digi-Key, Elmo, Hamilton Hallmark, Nu Horizons, and Zeus. Distributed in Canada by Arrow.

Circle No. 122 - For U.S. Response
Circle No. 123 - For International

ered will be an *extremely* nonlinear function of controller output. This may make it impossible to optimize PID loop-control parameters over a useful range of setpoints. Even worse, because of its unpredictability, is the effect of random ac line-voltage variations. Changes of 5% (or more) in rms line voltage are common and normal. But a sudden 5% change in voltage will cause a 10% change in (V^2/R) heating. Therefore, temperature can be lost until the consequent deviation is caught and corrected by the primary thermal control loop. The resulting excursion may totally bust the error budget of a high-performance thermostat.

The power-control circuit shown fixes all of these problems *(see the figure)*. It outputs true-mean-square power in direct proportion to a 4-to-20-mA current-loop control input. Delivered power is tightly regulated, thus cancelling line-voltage variations. In addition, it's proportioned on a fast 8.33-ms timebase, which avoids thermal ripple.

The circuit operates as follows: 4-to-20-mA control inputs are converted by A3 and Q5 to negative 20-100 µA (I1). I5 (fixed at +20 µA) zero-corrects I1 and the 0 to -80 µA difference is applied to the summing point of the A1 integrator. A4 compares the accumulated integral to a 2.5-V reference tapped from the "adjust" terminal of VR1 and, when the integral rises above that, turns on the 3043 triac trigger optocoupler. Zero-cross switching of the Q8 triac minimizes generated noise. Ac half-cycles through Q8 heat R1 and push load-monitor current I2 through LED E2.

To balance the resulting Q7 photocurrent, A2 produces I3 that causes matching conduction in the E1/Q6 optocoupler. Close tracking between sections of the 2501-2 dual optocoupler assures good proportionality between I2 and I3. Because I3 also biases series-connected Q2/Q3, the voltage applied to the base of Q4 will be 2[Xlog(Y*I2) + Z], where X and Z are constants common to all five transistors in the 3046 monolithic array, and Y is set by the "Fullscale Cal" pot. As a result, antilog transistor Q4's emitter current is closely given by $(Y*I2)^2/I6$. When integrated by A1, it gives an accurate prediction of true-mean-square power dissipated in R1.

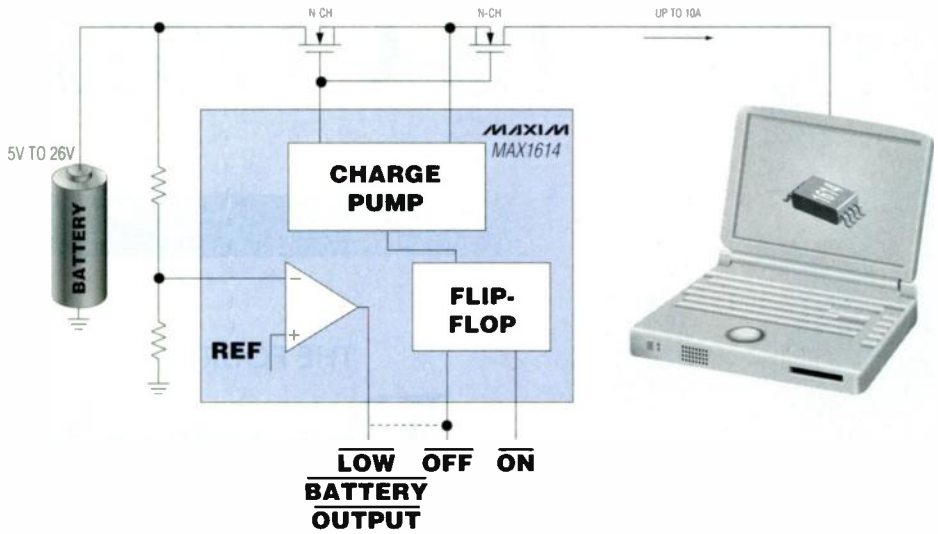
The resulting feedback loop acts to adjust Q8's duty cycle to regulate R1 power allowing the temperature controller to accurately and linearly track the 4-to-20-mA control input signal. Operating power for the circuit is developed from the 4-to-20-mA loop current, eliminating any need for another power source.

IDEAS WANTED

Address your Ideas for Design submissions to Ideas for Design Editor, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604.

WORLD'S LOWEST SUPPLY CURRENT HIGH-SIDE N-CHANNEL MOSFET DRIVER

Battery Switch Controller Draws Only 18µA Typical, 4µA Standby Current



- **Low Supply Current:**
  18µA Typical Quiescent Current
  4µA Typical Shutdown Current
- **1.5%-Accurate Low-Battery Detector**
- **Internal $\overline{ON}/\overline{OFF}$ Latch**
- **Internal Charge Pump:**
  Requires No External Components
- **Drives Single or Back-To-Back MOSFETs**
- **Space-Saving µMAX Package**

The MAX1614 drives high-side N-channel power MOSFETs to provide battery-power switching functions in portable equipment. The internal micropower regulator and charge pump that generate the high-side-drive output voltage require no external components.

A 1.5%-accurate low-battery comparator can be used to indicate a low-battery condition, provide an early power-fail warning to the system microprocessor, or disconnect the battery from the load to prevent deep-discharge battery damage. The MAX1614 typically draws only 18µA quiescent current, or 4µA shutdown current. It is available in the space-saving µMAX package that occupies about 60% less space than a standard 8-pin SO.

FREE* Notebook Design Guide – *Sent Within 24 Hours!

Includes: Data Sheets and Cards for Free Samples

CALL TOLL-FREE 1-800-998-8800 for a Design Guide or Free Sample
For Small-Quantity Orders Call (408) 737-7600 ext. 6380
6:00 a.m. – 6:00 p.m. Pacific Standard Time
http://www.maxim-ic.com

MasterCard® and Visa® are accepted for evaluation kits and small-quantity orders.

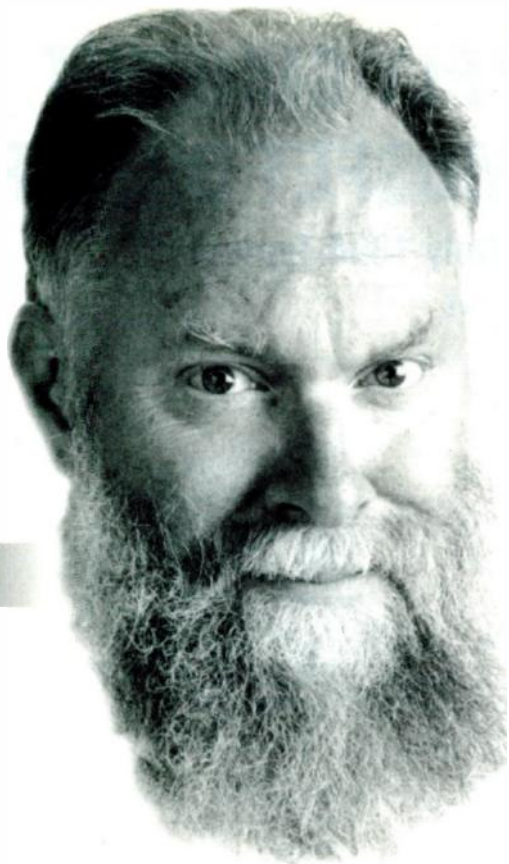
MAXIM

ISO 9001

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086, (408) 737-7600, FAX (408) 737-7194.

Distributed by Allied, Arrow, Bell, CAM RPC, Digi-Key, Elmo, Hamilton Hallmark, Nu Horizons, and Zeus. Distributed in Canada by Arrow.

Circle No. 124 - For U.S. Response
Circle No. 125 - For International



PEASE IS COMING!

THE FOURTH ANNUAL

Portable by Design

CONFERENCE & EXHIBITION

presents

BOB PEASE

in a special appearance at the 1997 show

Come to Portable by Design to meet and listen to the electronic industry's guru of analog engineering. Bob is National Semiconductor's analog design expert and popular columnist for *Electronic Design magazine*.

If you attend, you'll also receive a free autographed keepsake collection of columns from *Electronic Design's* well-read "Pease Porridge." Be there to ask Bob questions on technology—or even humanity, and we're sure you'll receive an answer that will be filled with wit, wisdom, and waggish observations.

Save the Date!

WEDNESDAY, MARCH 26, 1997

at the Santa Clara Convention Center
Santa Clara, Calif.

Exhibition Hall - 11:00 a.m.

For technical conference or exhibition attendee information, call Betsy Tapp at 201/393-6075; Fax 201/393-6073; E-mail: portable@class.org

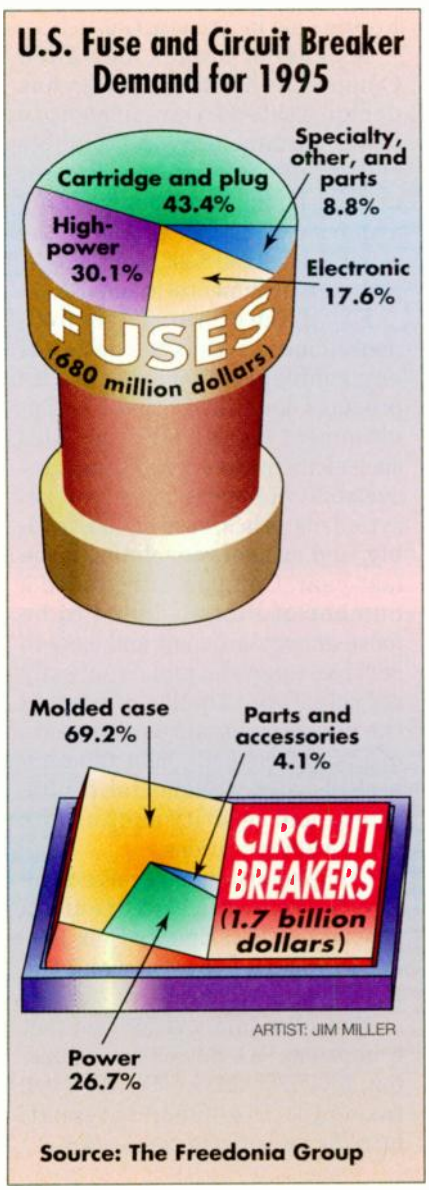
ELECTRONIC DESIGN QUICK LOOK

Edited by Mike Sciannamea and Debra Schiff

MARKET FACTS

Getting Their Big Break

Topping nearly $3 billion by the year 2000, demand for U.S. fuses and circuit breakers is expected to gain 4% annually over the next three years. According to The Freedonia Group's new study, "Fuses & Circuit Breakers," the demand for fuses in 1989 was $574 million. That year, the demand for circuit breakers was $1388 million. Net exports in 1989 were counted at $145 million, while fuse and circuit breaker shipments weighed in at $2107 million. In comparison, 1995 saw fuse demand at $680 million, up 3.3% in annual growth. Circuit breakers that year saw $1705 million in demand. 1995 net exports were down from 1989 at only $60 million, but combined fuse and circuit breaker shipments were up 2.5% in annual growth at $2445 million. Projections for the millennium put fuse demand at $850 million and circuit breakers at $2050 million. Shipments will increase 4.2% annually to $3000 million in 2000. The Freedonia Group expects that surface-mounted thin-film electronic fuses and molded case circuit breakers with solid-state switching mechanisms will push the U.S. fuse and circuit breakers demand through to the next century. These products are popular in the portable handheld electronic device market which is predicted to explode in the next century. The automotive electronic systems and subsystems markets also make use of the fuses, further boosting demand. Microprocessor-based circuit breaker products have been used to replace thermal and thermal magnetic circuit breakers in internal power distribution systems of industrial and residential facilities. It is predicted that the commercial aerospace equipment market will send the demand for fuses and circuit breakers skyrocketing in the future. The study is priced at $3400 and is available from The Freedonia Group Inc., 3570 Warrensville Center Rd.,# 201, Cleveland, OH 44122-5226; (216) 921-6800; fax (216) 921-5459.—DS



OFF THE SHELF

"Essentials of Project and Systems Engineering Management" explains key project management concepts and demonstrates how to apply them to the systems engineering process in order to optimize product design and development. Topics that are discussed in the book include project planning and scheduling; evaluative methods such as cost, situation, and sensitivity analysis; team building and interaction; and software engineering tools and integrative management trends. The 358-page book is priced at $59.95. Contact John Wiley & Sons Inc., 605 Third Ave., New York, NY 10158-0012; (212) 850-6336.

"Radio Frequency Electronics: Circuits and Applications" introduces the basic concepts and key circuits of radio-frequency systems. The book covers fundamental principles that apply to all radio devices, ranging from wireless data transceivers on semiconductor chips to high-power broadcast transmitters. Other topics discussed include filters, matching networks, transmission lines, and low-noise amplifiers. Applications of radio-frequency systems are described in areas such as communications, radio and television broadcasting, and radio astronomy. The 358-page book is priced at $49.95. Contact Cambridge University Press, 40 W. 20th St., New York, NY 10011-4211.

40 YEARS AGO IN ELECTRONIC DESIGN

World's Largest Electron Tube

A ten-foot, five-inch klystron developed by Eitel-McCullough, Inc., San Bruno, Calif. is measured by company executives. It will be used in radar, linear accelerator applications, and other high power operations. *(Electronic Design, January 1, 1957, p. 5) This baby obviously wasn't one of those tubes that you could take down to the local five-and-ten's tube tester to check for shorts or cathode emission. This brief picture-caption story certainly doesn't reflect the ongoing trend of miniaturization that began in earnest in the late '50s. However, although the story doesn't mention the operating frequency, the klystron's size probably indicates that it was intended for the lower-frequency, longer wavelength, region of the microwave band. And, when you need substantial amounts of power, bigger is usually better. Eitel-McCullough, also known as Eimac, was one of the major suppliers of vacuum tubes for RF and microwave applications.—SS*

New Books: Reference Data for Radio Engineers, International Telephone and Telegraph Corp., Publication Dept., 67 Broad Street, New York 4, N.Y., 1121 pages, 1000 illustrations. Price: $6.00.

Primarily a compilation of equations, graphs, tables, and similar data that are frequently needed in radio engineering. New material has been added on modern network design, magnetic amplifiers, feedback control systems, semiconductors, transistors, scattering matrixes, digital computers, nuclear physics, information theory, and probability and statistics. *(Electronic Design, January 15, 1957, p. 95)*

This handbook, also commonly known as the FTR Handbook (it was published by Federal Radio and Telegraph, which became a part of ITT), was a staple on many EEs' bookshelves beginning in the 1940s. This, the fourth edition, with its orange-yellow and green jacket covering a green binding with gold letters, probably was one of the most popular handbooks around because of its wealth of practical information on a broad variety of subjects. It was particularly strong on RF and microwave technology. It was followed by a fifth edition in 1968 and the sixth and final—and largest—edition was published in 1975.—SS

New Literature: Silicon Junction Transistors

Data sheets on NPN grown junction silicon transistors types 2N117, 2N118, 2N243, 2N244, 951, and 953 have just been released. The data sheets show illustrations, tables of typical design characteristics and curves, as well as grades and physical dimensions. The 2N117 and 2N118 transistors have been built to Navy Specifications, MIL-T-19112A (Ships). The types 2N243 and 2N244 feature controlled beta spreads of 3 to 1. The data sheets of the 951, 952 and 953 transistors have been revised and give additional information. A price list on all the transistor types is included. Texas Instruments Inc., 6000 Lemmon Ave., Dallas 9, Texas. *(Electronic Design, January 1, 1957, p. 101)*

Texas Instruments was on its way to becoming the premier supplier of silicon transistors, and the pace of developments in semiconductor technology was accelerating rapidly. Within two years, however, these 1956-vintage transistors would be followed by the first integrated circuit built by TI's Jack Kilby. Fairchild Semiconductor developed the planar process at about the same time, and after that, the electronics industry, as well as TI itself, would never be the same.—SS

An "EE" For Environmental Effort

One of the most significant trends this decade has been a greater concern for the environment. Companies worldwide are realizing that protecting the Earth's natural resources is not only good for its inhabitants, but also good for business. And they're beginning to be recognized for their efforts.

Compaq Computer Corp.has been recognized for Environmental Excellence by the National Association of Environmental Management (NAEM), an association dedicated to the advancement of environmental management. The announcement was made at the recent Environmental Management Forum held in Atlanta, Ga.

A panel of judges identified Compaq as a company who has demonstrated a commitment to the environment by the tangible results of their efforts. Rather than designing and manufacturing a number of "green" products, the company instead relies on a single, global environmental standard.

Key to the company's environmental initiatives is the design of environmental features into its products, know as Design For Environment (DFE). DFE includes such elements as energy usage, recyclability of materials, use of recycled materials, ease of disassembly, and ease of recycling. In the last year, Compaq introduced a number of PCs designed to be more energy-efficient and easy to service, upgrade, and eventually recycle. Compaq also expanded the environmental requirements of its suppliers and conducted comprehensive environmental, health, safety, and security audits of its worldwide operations.

Compaq also has received the Environmental Protection Agency's (EPA) Energy Star 1996 PC Partner of the Year and the EPA's WasteWi$e Award.

For more information, contact Compaq at P.O. Box 692000, Houston, TX 77269-2000; (713) 514-0484; fax (713) 514-4583; Internet: http://www.compaq.com.—MS

HOW MANY TOKO LL'S CAN YOU PLACE

ON THE HEAD OF A PIN?

TOKO & PENSTOCK
RF/MICROWAVE DISTRIBUTION
AN AVNET COMPANY

YOUR RF DESIGN TEAM

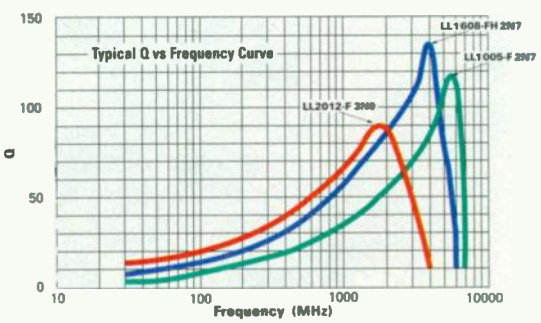
And how much board space can you gain?

Such a micro size may seem impossible, but not to Toko engineers. The LL1005 (inductance range 1.0 to 27.0 nH) is merely the latest addition to Toko's micro-miniature line of ceramic multilayer chip inductors available from Penstock. With an 0402 footprint and an 0.05 profile, *the LL1005 is the world's smallest*–by far.

Toko's cutting edge design and leadership in ceramic multilayer technology helps in other ways, too. Toko chip inductors offer higher current handling capabilities (up to 1 amp) and tolerance as low as 3% on some values. Plus:

- Available 0402, 0603 and 0805 packages assure wide flexibility
- E-12 series inductance from 1.0 to 470 nH makes design modification easy
- Reflow solderable
- Tape and reel packaging to ease manufacturing
- Pricing that's always competitive
- Quick delivery

As the world's largest RF/microwave distributor, Penstock is the design engineer's link to Toko's advanced technology. We inventory more than 5 million Toko parts –*in stock*– and serve the engineering community from over 25 sales offices throughout North America and Europe. With **Toko** and **Penstock**, you always know, there's nothing more advanced–or more readily available– anywhere in the world.

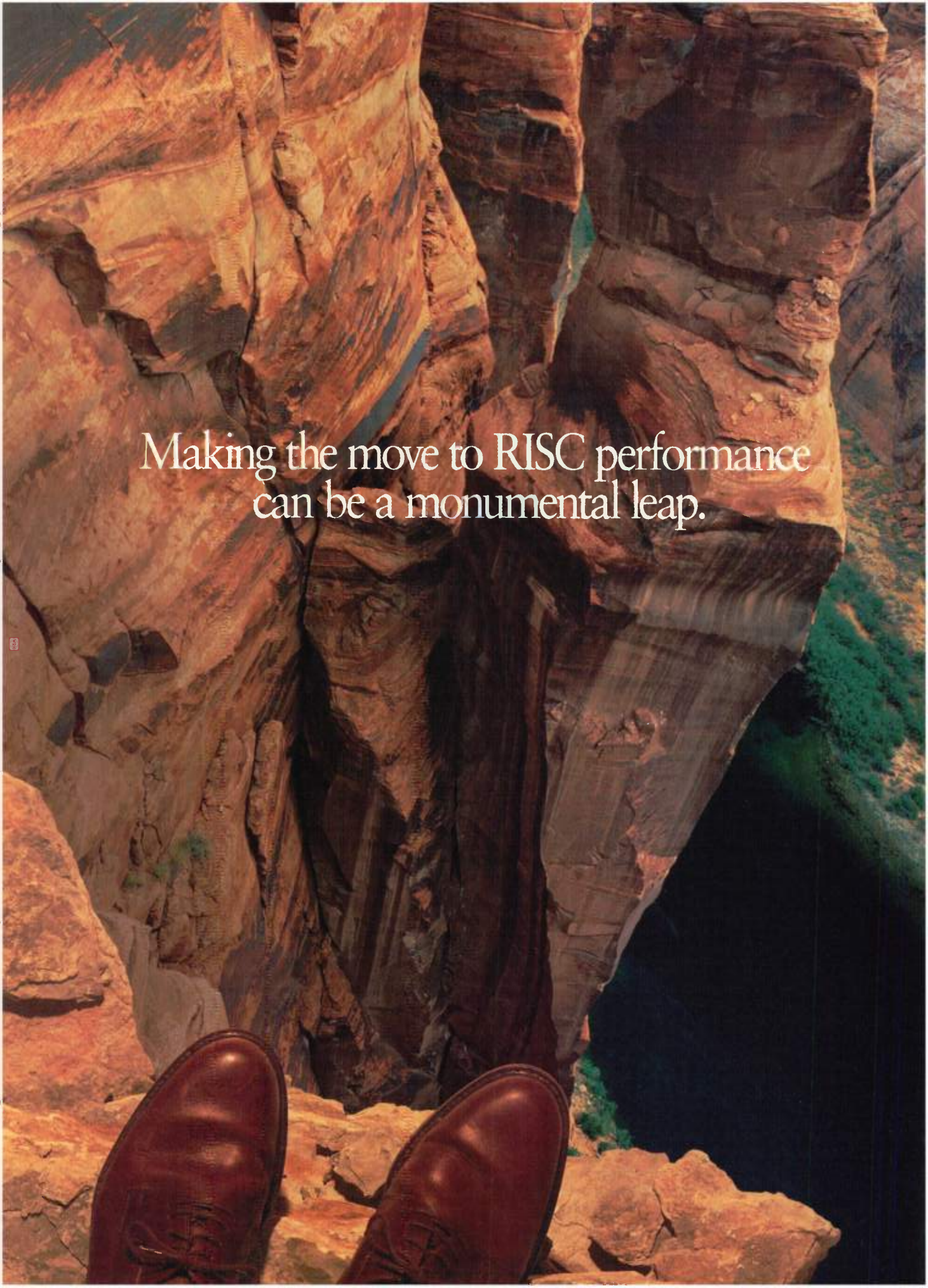


Toko LL Prototyping Kits Available

LL1005-F
LL1608-F, LL1608-FH
LL2012-F

Call: **1-800-PENSTOCK**
In Northern California call: 1-408-745-8190
In Canada call: 1-800-PENSTOCK

READER SERVICE 144


Making the move to RISC performance
can be a monumental leap.

Or one small step.

Moving from CISC to RISC can make anyone feel jumpy. Scrapping your code. Blowing a ton on memory. Delaying time to market. But with Motorola's ColdFire™ technology, RISC performance is just a step away. The cost-effective ColdFire architecture is derived from Motorola's 68K family. So you can build on current product designs and programming experience to get products to market faster, with a smaller investment. In addition, the ColdFire technology maximizes your code density, minimizes the memory required to store it, and delivers unprecedented price/performance levels for cost-sensitive applications. To learn more about Motorola's ColdFire microprocessor family, call 1-800-521-6274 (ref. #HP001). Or visit www.mot.com/coldfire.

It'll improve your design by leaps and bounds.

MOTOROLA

What you never thought possible.™

HOT PC PRODUCTS

The Mach V computer systems from Falcon Northwest will be using Diamond Multimedia's Monster 3D gaming accelerator, complete with 3 Dfx Interactive's Voodoo Graphics engine. Providing consistently high frame rates, the Monster 3D accelerator is a 3D-only pass-through subsystem. Monster 3D is PCI-buss compatible, capable of working with existing 2D graphics accelerators and Windows 95. In combination with the Voodoo Graphics technology, Monster 3D provides hard-core PC gamers with photorealistic quality at real-time frame rates. Features of the Mach V systems include a triangle setup exceeding one million texture mapped triangles per second, alpha blending, anti-aliasing, tri-linear filtering, Z-buffering, and level-of-detail MIP mapping. For more information, contact Diamond Multimedia, 2880 Junction Ave., San Jose, CA 95134-1922; (408) 325-7000; fax (408) 325-7070; Internet: http://www.diamondmm.com.

Expanding the Extensa family of mid-range mobile computers, Texas Instruments (TI) has introduced the Extensa 600CD/605CD and 650CD/650CDT/655CD Series. The 600 Series is designed with a dual chemistry battery system, including a standard Duracell DR35 NiMH PowerSmart Battery. Users can purchase the Duracell DR201 Li-Ion PowerSmart Battery as a replacement or spare. The 650 models feature TI's ThunderLAN architecture, enabling Extensa users to optimize their Advanced PCI cards' connection to speeds of 100BaseT or higher when the technology permits. All of the 600 Series notebooks weigh less than seven pounds. The 600CD/605CD models are priced at $2299, the 650CD and 655CD at $3299, and the 650CDT at $3799. For more information, contact Texas Instruments Inc., Personal Productivity Products, 7800 Banner Rd., Dallas, TX 75251; (800) TI-TEXAS; e-mail: swest@ti.com.

SmartPatent Workbench 4.1 is a software tool that allows businesses to electronically search, analyze, and organize patents according to individual strategies. Supporting a mapping and mining methodology, SmartPatent Workbench provides a means for companies to map their electronic patents into different groupings based on the tree structure. The mining process is an analysis of a company's cross-licensed patents and competitors' patents. SmartPatents also includes a custom electronic patent database culled from all patents filled with the U.S. Patent and Trademark office since 1972, for companies that purchase the Workbench software. For more information, contact SmartPatents Inc., 1975 Landings Dr., Mountain View, CA 94043; (415) 237-0900; fax (415) 237-0910; Internet: http://www.smartpatents.com.

The Envelope Please

In an announcement made by President Clinton and Commerce Secretary Mickey Cantor, ADAC Laboratories was named as one of the winners of the 1996 Malcolm Baldrige National Quality Award.

The award is given to those businesses that have made achievements and improvements in the areas of analysis and information, business results and customer focus, customer satisfaction, human resource development and management, process management, and strategic planning. Companies applying for the award submit performance management information to an independent board of business and quality experts for review.

ADAC Laboratories, founded in 1970, will be joining the three other winners of the Baldridge Award in the small business and service categories, in presenting the details of the company's strategies for quality improvement. The presentations will be made at the Quest for Excellence conference February 9-12, in Washington, D.C.

A manufacturer of products for the health care information systems, nuclear medicine, and radiation therapy planning fields, ADAC also designs, markets and supports products for the health care industry.

ADAC is a member of the Institute for Interconnecting and Packaging Electronic Circuits (IPC), Milipitas, Calif. The IPC is a trade organization with members in the assembly, design, and manufacturing sectors of the electronic interconnection industry.

Representing over 60 government agencies and semiconductor interests, the Semiconductor Research Corporation (SRC) has named its first recipient of its Aristotle Award. Acknowledging excellence in teaching, the Aristotle Award is given to outstanding faculty members who advise graduate students in SRC-funded research at universities in Canada and the U.S.

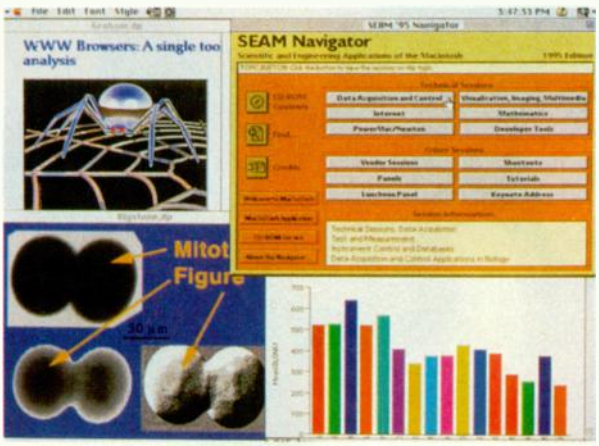
This year's Aristotle Award winner is the dean of the College of Engineering at the University of Michigan, Prof. Stephen W. Director. Former students of the professor, who are now working in the semiconductor industry, wrote letters of nomination to SRC, praising Director on his technique.

Director has been recognized for instilling his graduate students with creativity and technical skill. The professor has been a participant in SRC's research programs since 1982. Before joining the faculty at the Ann Arbor university in September 1996, Director was the dean of engineering at Carnegie Mellon University, Pittsburgh, Pa.

SRC research is performed at over 50 research institutions and universities across North America. The consortium has invested more than $340 million in semiconductor research since 1982.

Mac CD-ROM Showcases SEAM '95

MacSciTech, a professional association that produces technical conferences, journals, and CD-ROMs to support Macintosh users in the aerospace, manufacturing, medical, pharmaceutical, and university communities, has released "The Official Scientific & Engineering Applications of the Macintosh (SEAM) '95 Conference CD-ROM."



The CD-ROM features all of the abstracts provided at the symposium held in San Francisco, Calif. in January 1995. The association's third annual technical conference was aimed at engineers and research scientists, and covered topics such as data acquisition, developer's tools, imaging, the Internet, mathematics, multimedia, and visualization.

Containing nearly 600 Mbytes of information from SEAM '95, the CD-ROM includes all of the text of the original papers, as well as all of the data, movies, pictures, virtual instruments, and other items submitted to the conference by the authors. The CD-ROM has versions of the papers in both the authors' original formats and Common Ground, a universal format, so that the papers can be accessible to all users. The navigator features a search utility so that users may search the abstracts for information such as author contact information.

Adding another multimedia spin to the CD-ROM, MacSciTech has included QuickTime movie pieces of selected presentations given at the conference. One of the shorts spotlights Adam Engst, author of "The Internet Starter Kit," who was the Keynote Speaker at the symposium. Other featured speakers are Carl Manaster of Desert Sky Software and Dr. Dale Graham of the National Institutes of Health.

Available for $89 for nonmembers and $59 for members of MacSciTech, "The Official SEAM '95 Conference CD-ROM" provides a search utility and navigator for the user.

For more information, contact MacSciTech Users Association, 49 Midgley Ln., Worcester, MA 01604-3564; (508) 755-5242; Internet: http://www.macscitech.org/.

So Loud...
You Can Hear a Pin Drop

AKM's New Audio HiDS Captures the Loudest Louds and the Quietest Quiets

A jet engine roars. A pin drops. Both are sounds, both total opposites. Each demand uncompromising high-fidelity.

Now, AKM a worldwide leader in the design and manufacture of professional audio ICs, covers both ends of the audio spectrum in a new line of the world's best audio ADCs, DACs, and CODECs.

These wide dynamic range, low distortion, single supply, dual-bit audio ICs are known as HiDS converters. Wherever the HiDS logo is seen, be assured of the highest performance and quality.

HiDS HIGH DYNAMIC SOUND

Our HiDS product line includes: 24-bit ADC at 113dB DR (AK5391) and it's companion the 24-bit DAC (AK4324), 96kHz 20-bit 105dB DR ADC (AK5352), 20-bit 100dB DR CODEC (AK4520), and the highest performance multimedia CODEC (AK4531).

With AKM's aggressive new product release schedule, tremendous fab capacity, and numerous audio patents, we are the audio supplier to look for now and in the future.

And just to ensure that your experience is soothing, AKM stands behind its products with world-class service and support.

AKM HiDS Audio ICs		
ADC	AK5350	Enhanced dual bit ΔΣ 2 channel ADC HighPerformance 20 bit, 100 dB DR
	AK5351	100dB 20-bit 2 channel ADC, 48kHz
	AK5352	105dB 20-bit 2 channel ADC, 96kHz
	AK5391	113dB 24-bit ΔΣ 2 channel ADC
DAC	AK4320	High Performance 20-bit 2 channel DAC
	AK4321	High Speed (96kHz sampling), 20-bit 2 channel DAC
	AK4323	20-bit 2 channel DAC with analog PLL
	AK4324	106dB 24-bit 2 channel DAC, 96kHz
CODEC	AK4520	20-bit 2 channel ADC & DAC
	AK4531	2 channel audio ADC with 5 channel stereo mixer, 4 channel DAC
	AK7712	24-bit DSP+2 20-bit stereo DACs & 20-bit stereo ADC

For HiDS ADCs, DACs, and CODECs that let you deliver the lowest lows and the highest highs in audio, look to AKM.

AKM Semiconductor, Inc.

Call 408-436-8580 today for our Product Guide and more information on HiDS... http://www.akm.com

USA: AKM Semiconductor, Inc.
2001 Gateway Place, Suite 650 West, San Jose, CA 95110
Phone: (408) 436-8580 • Fax: (408) 436-7591
E-mail: ICinfo@akm.com

Japan: Asahi Kasei Microsystems Co., Ltd.
TS Building, 24-10, Yoyogi 1-chome
Shibuya-ku, Tokyo 151
Phone: +81-3-3320-2062 • Fax: +81-3-3320-2072

Europe: Asahi Kasei Microsystems Co., Ltd.
22 The Courtyards, Hatters Lane, Croxley Business Park
Watford, Herts, WD1 8YH, United Kingdom
Phone: +44 (0)1923-226988 • Fax: +44 (0)1923-226933

ISO 9001 Registered Company
Certificate Number FM31868

QUICKNEWS

Low-voltage Operation From Mid-range Op Amp—The LMC272 CMOS dual-operational amplifier from National Semiconductor uses rail-to-rail output stages to achieve a 2-15-V operating range.

Designed for the portable and battery-powered markets, the LMC272 offers guaranteed 2.7-, 5-, or 10-V operation. The 2-V end of the operating range will offer users reliable battery performance.

Product standouts include a high voltage gain of 88 dB, input common mode voltage range extending below the negative supply rail that allows ground sensing, input voltage range of -0.3 to 4.2 V, low supply current of 1 mA per amplifier, and unity gain bandwidth of 2.2 MHz.

The LMC272 is available in 8-pin DIP, plastic 8-pin MSOP, and 8-pin SOIC configurations. The plastic package is priced at $0.70 each in 1000-unit quantities, while the DIP and SOIC units sell for $0.50 a piece in 1000-unit orders.

For more information, contact National Semiconductor Corporation, 2900 Semiconductor Dr., P.O. Box 58090, Santa Clara, CA 95052; (800) 272-9959; Internet: http://www.national.com.

Testing. . . One, Two, Three—A new family of semiconductor testers, the HP 94000 Series, from Hewlett-Packard, features mixed-signal capabilities.

The HP 94000 Series is designed to handle a variety of testing situations such as asynchronous transfer mode, digital subscriber-line chips, digital versatile disks, graphics controller chips, hard disk drive devices, high-speed partial response maximum likelihood, and integrated personal computer audio chips. Other uses for the testers in the commercial device sector include analog-to-digital and digital-to-analog converters, baseband communications devices, and assorted mixed-signal chips. Future applications for the HP 94000 Series include broadband communication devices, cable-modem/set-top box chipsets, and gigabit ethernet devices.

Improving time-to-market, the tester family offers users a graphical interface for program generation. The Hewlett-Packard visual pin monitor, CAE/CAD links to simulation tools, and a graphical vector editor/logic analyzer all are included in the design to improve program generation 30 to 50%.

The HP 94000 Series pricing starts at $600,000.

For more information, contact Hewlett-Packard Company, Test and Measurement Organization, P.O. Box 50637, Palo Alto, CA 94303-9512; (408) 553-7056; fax (408) 241-0918; e-mail: anil_bhalla@hp.com.

Establishing The "Homework Hotline"

Located in northeastern Pennsylvania, the Delaware Valley School District recently implemented a complete multimedia network to provide Internet access, high-speed data transfer, videoconferencing, unified messaging, and wireless services throughout the entire school district.

The school district recently installed Nortel Communications Systems Inc.'s Magellan Passport ATM enterprise network switches to consolidate its voice, video, and data traffic over one high-speed network. The network connects the school district's main campus, comprising the Delaware Valley Elementary, Middle and High Schools, and Administration buildings, with three additional schools on remote campuses in the surrounding area. The school district now uses multiple T-1 lines, but soon plans to switch to an OC-3 ATM network.

The network enables the district's 4400 students to access he Internet, transfer files across the network, access CD-ROM servers and libraries, and send e-mails to foreign pen pals.

In addition, the district is upgrading the operating system software and instructional interface to allow teachers to manage the resources of the computer system in an educationally significant way. Teachers will be able to create and assign instructional plans containing on- and off-line activities, communicate with students and staff, and get basic student demographic information.

As part of its network upgrades, the school district also installed three Meridian 1 Communications Systems, complete with Meridian Mail voice messaging capabilities in each of the campuses. Teachers now have a phone in each classroom and can use the mail package to send messages to parents, including a "Homework Hotline" that allows parents and students to call anytime to find out the latest homework assignments. Meridian Mail also will be used to report school closings due to inclement weather.

Nortel's Messenger 2.0 package is used to provide unified messaging capabilities to organize voice mail, e-mail, and faxes into one electronic mailbox for each school administrator. The school district intends to use a fax-on-demand server to communicate to parents and students extracurricular activities such as sports game and practice schedules, band schedules, and other meetings.

Nortel's Companion in-building wireless telephone system provides immediate communication for emergencies and security needs. For example, teachers can alert school nurses of playground emergencies to obtain medical attention for students.

The school district also is using Nortel's desktop H320 multimedia conferencing solution to facilitate an administrator's meetings. Since the district is spread across a wide area of rural countryside, videoconferencing allows teachers and staff to communicate face-to-face. The district also offers distance learning from commercial services and will soon offer intra-district distance learning.

For more information on this multimedia network, contact Nortel, 2221 Lakeside Blvd., Richardson, TX 75082; (214) 684-8721; fax (214) 684-3726; Internet: http://www.nortel.com.—*MS*

New Multimedia Distribution Solution

Introduced at Fall Internet World, the Micro Webserver from Cisco Systems is a plug-and-play Internet server with a removable 100 Mbyte zip drive. The Webserver is designed to allow companies of all sizes to communicate via the Internet with their branch offices.

The device can be used with off-the-shelf, third party authoring packages, and is quickly configured using a Java graphical user interface management application. The Webserver packages both the hardware and the embedded Web software kernel within a small footprint, allowing the user to stack Webservers or keep one at desktop.

Using the language of the Internet to function in any networking environment, the server's Hyper Text Transfer Protocol 1.1 microkernel provides a secure embedded system. The microkernel features multiple user password protection.

The Webserver's Small Computer System Interface file system is capable of supporting up to five read/write peripherals simultaneously.

In addition to the Micro Webserver, Cisco has introduced its IP/TV multimedia networking software. Targeted at the corporate training and educational institution markets, IP/TV allows users to bring streaming networked multimedia to the desktop.

The real-time programming capable software is Internet Engineering Task Force compliant, providing users immediate access to public Internet Multicast Backbone broadcasts.

Developed by Precept Software Inc., IP/TV uses the Real-Time Transport Protocol standard to deliver the multimedia streams.

IP/TV consists of the Program Guide, Viewer, and Video Server. The Program Guide runs on any Windows NT server, and is the management and setup mechanism for the IP/TV application. The Viewer displays listings of the programs available, plays the video, and allows the user to manipulate a number of settings on the program screen. The Video Server can capture and send live video from remote devices or from prerecorded AVI video streams from storage.

The Micro Webserver is priced at $995 and the IP/TV software starts at $3500.

For more information, contact Cisco Systems Inc., 170 West Tasman Dr., Bldg. L-2, San Jose, CA 95134-1706; (408) 527-1732; Internet: http://www.cisco.com.

THE FIRST COMPLETE LINE OF 600W DC-DC CONVERTERS IS SHIPPING NOW.

Only Lambda has 600W DC-DC converters with 3, 5, 12, 15, 24, 28 or 48 volt outputs, all in stock for immediate delivery. Our new PH600 Series and our new, smaller 300W PH300 operate up to 100°C baseplate, for demanding telecom applications. And this is just the beginning. In June, we'll roll out 50, 75, 100, 150 and 200 watt models with the same state-of-the-art efficiency, high density and low cost/watt as the PH600 and PH300. We've made a commitment to leadership in DC-DC power. And we're delivering.

LAMBDA Electronics Inc.

1-800-LAMBDA-4

515 Broad Hollow Road, Melville, NY 11747-3700
Tel: 516-694-4200 Fax: 516-293-0519
http://www.lambdapower.com

WRH

READER SERVICE 177

TRUDEL TO FORM

Machine Age business was about routine. This, mostly, is still what they teach at our leading business schools. The union card for U.S. managers has become the MBA.

Machine Age methodology is one of workers and bosses, standard processes, incremental optimization, and the manipulation of financial abstractions. Recent Western management fads are based on repetitive process.

These companies resemble Newtonian machines, built from huge gears. The purpose of management is to keep the gears turning smoothly. A drop of oil here, a minor adjustment there, and all is well. That model won't work anymore.

JOHN D. TRUDEL
CONTRIBUTING EDITOR

The notion of sabotage came with the early Machine Age's need for order. Workers in France resisted management by throwing their shoes ("sabots") into the gears, stopping production. Factories could not tolerate the disruption of routine. Eventually, any who favored change risked being cast out as renegades.

Some renegades are legendary. This column was, until we tired of continual harassment by Lockheed's lawyers, originally named after Kelly Johnson's famous "Skunkworks." Many engineers revere him because he delivered wondrous, breakthough results.

Still, managers distrust renegades, and bureaucrats hate them. The Machine Age was a dangerous time for such people. Unfortunately, even Johnson's Skunkworks did not, except in name, outlast him.

Today, we need innovators. Evolutionary biologists know that the world follows "punctuated equilibrium." Species flourish for millennia until there is a discontinuity that makes them unable to compete. Then they quickly die off or decline.

The same is true in business and economics. We now face the greatest discontinuity in all of human history. We live in a time of upheaval and accelerating change. The Machine Age is ending. A new era is at hand, a time for innovative mavericks.

The new milieu, the Information Age, requires radically different business methods. Management is not production-oriented, but mission-oriented.

Hierarchies flatten. Not because computers and process can flatten the organization, as reengineering advocates would say. Not because sensitive managers suddenly favor democracy, though some may. They flatten because, to be effective, the deliverers of the next-thing-for-the-company are organized like commando units.

Today's winning businesses need small, fast teams that must be empowered by and report to (and defended by) the CEO.

Because a company's future survival depends on the success of these mission teams, they need free rein. They must be treated not as employees who obediently follow routine, but as equals in the business of the company's success.

Most Machine Age businesses will fail to adapt in time to the new era. Many have custodial upper management; people who did not create the machines that they run, and who don't really understand them. They fear taking any action beyond their basic duty of running the machine.

Some firms are beyond changing. Their mavericks, innovators, and change agents were the first to be downsized. One vice-president says: "What we have left are barracks officers. They look great on the parade ground, but are useless for combat."

When radical change is needed, traditional managers cling to the past, fearful for their career safety. "If I don't squeeze profits from this turkey, I will be replaced by someone who will." Future columns will discuss ways to allow effective change.

John D. Trudel, CMC, provides business development consulting and is the author of "High Tech with Low Risk." He is founder and director of The Trudel Group, 33470 Chinook Pl., Scappoose, OR 97056; (503) 640-5599; fax (503) 543-6361; e-mail johntrudel@aol.com; Internet: http://members.aol.com/johntrudel.

FREE STUFF

The new ***Microelectronic Relay (MER) Designer's Manual*** from International Rectifier (IR) is available free of charge to application and design engineers. The manual contains a selection guide, product data, specification and application information for IR's MER products, including photovoltaic and Gen 2 photovoltaic relays, ChipSwitch relays, and photovoltaic isolators. To obtain a copy of the manual, contact Carol Gajdos, IR, Technical Literature Dept., 100 N. Sepulveda Blvd., El Segundo, CA 90245-4359; (310) 252-7106; fax (310) 252-7171; Internet: http://www.irf.com.

Flip Chip Technologies (FCT) has released its Bumping Service Design Guide. The guide is available free of charge direct from the company, or by downloading it off of the company's web site. The introduction to the guide covers wafer requirements and minimum pitch capabilities. The bulk of the guide addresses flip chip design standards, including bump metallurgy, available solder alloys, and mask data requirements. A third section deals with developments such as fine pitch, interconnect capability, and 200-mm wafer capability. Contact FCT, 2821 S. 35th St., Bldg. D., Suite 5, Phoenix, AZ 85034; (602) 431-6020; fax (602) 431-6021; Internet: http://www.flipchip.com.

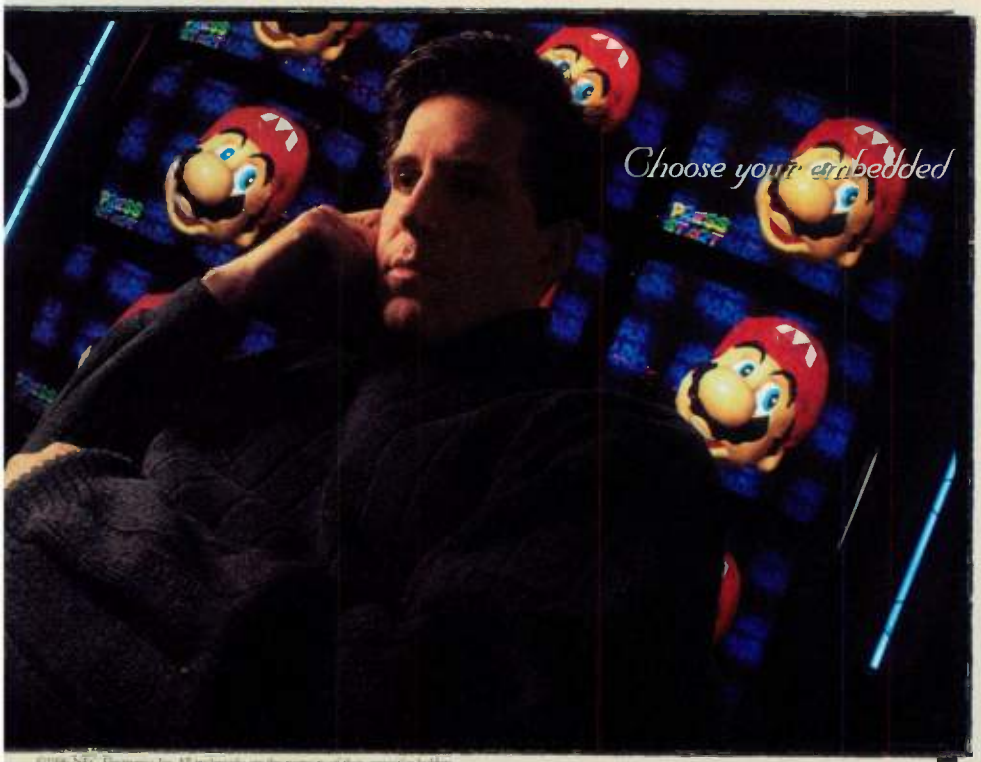
DROP US A LINE

We're very interested in hearing from you. One of our New Year's Resolutions is to begin printing letters sent to this section, so if you have a topic you'd like to see covered in QuickLook, a viewpoint on something you may have seen in this section, or even some praise (for our moms' to post on their refrigerators) about a piece we've printed here, please send it in. We welcome all correspondence. You can e-mail Mike Sciannamea at **mikemea@class.org** or Deb Schiff at **debras@csnet.net.** If you prefer to use the postal service, send your comments to The Copy Desk, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604. Our fax number is (201) 393-0204.

"I'VE HEARD IT SAID THAT YOU CAN NEVER GIVE A GAME DEVELOPER ENOUGH RESOURCES.

WELL, THIS IS ONE OF THOSE TIMES WHEN WE EXCEEDED THEIR *wildest* EXPECTATIONS."

DARREN SMITH, *Project Manager,* NINTENDO 64



"Getting a machine like the Nintendo 64™ to market was an amazing experience. For three years, I coordinated efforts between Nintendo, MIPS™ and the folks at NEC.

During that time, we looked at several versions of MIPS RISC processors. However, NEC's V_R Series™ processor shot to the top. Without question, it provided the most power for the price.

One great thing about the V_R Series processor is what it enables. You see, game developers no longer have to hold back. It's now possible to create fantastic revolutionary games at an unbelievably low cost. With power to spare for things like on-the-fly image decompression, and even things they've only dreamed about doing.

For the first time, developers can truly simulate reality. If they want something to happen, it will happen. Take, for example, WaveRace64.™ The NEC V_R Series allows for such incredibly smooth and realistic dynamics when riding on water, that you'd be well advised not to play if you get seasick.

Frankly, it's exactly what you'd expect from a Nintendo/NEC partnership. I just can't stress enough what a phenomenal job NEC does of keeping an eye on your bottom line. NEC clearly understands that every penny counts. In fact, they were able to reduce the number of pins. And in case you didn't know, every pin is another million dollars in our business.

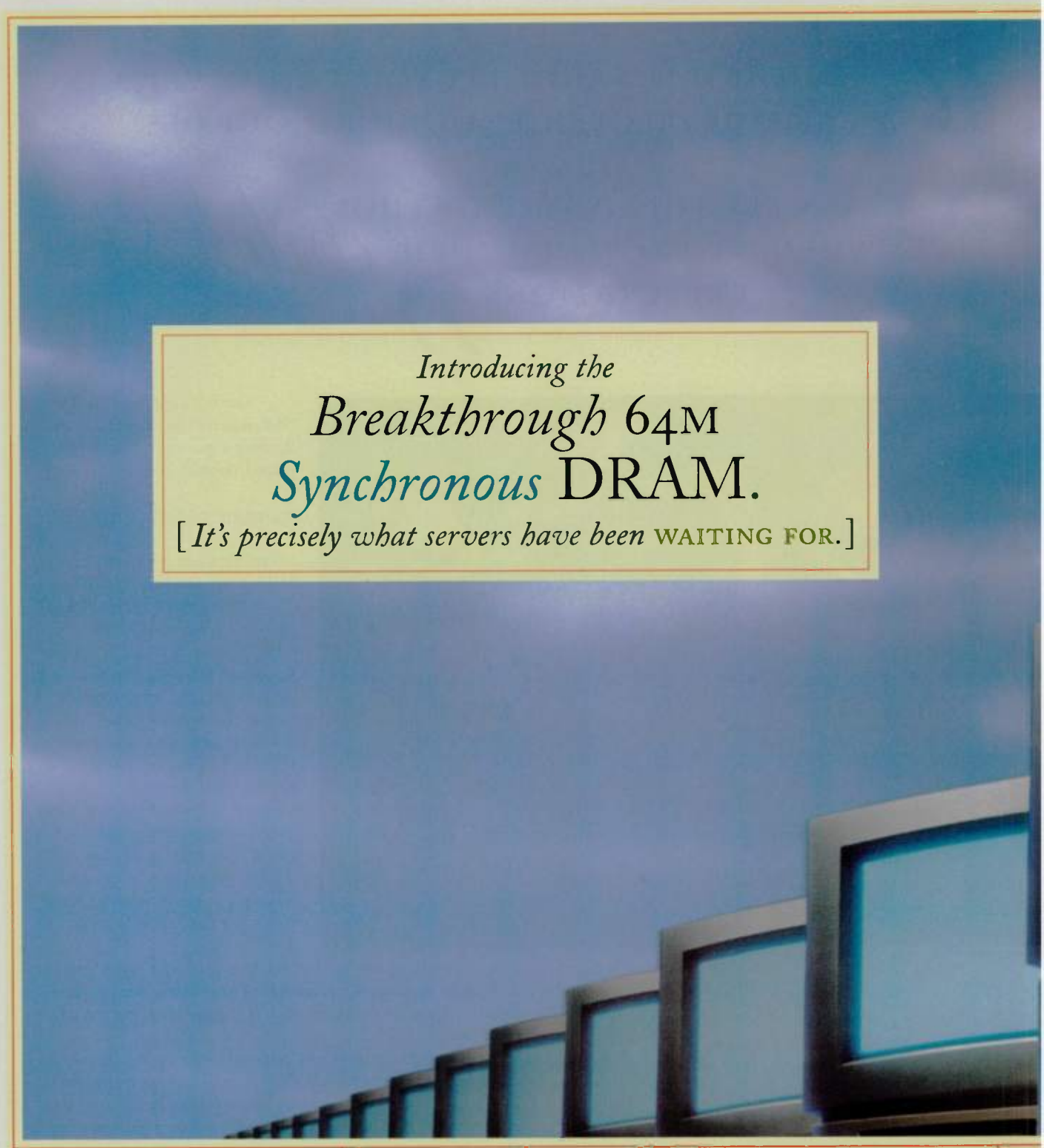
But it also means a lot to the kids. You see, the V_R Series processor is an evergreen design. So it won't be obsolete in two or three years. And that means Nintendo 64 devotees can put their allowances towards other things. Like buying books or planting trees. And hey, maybe they'll even buy a few more games."

For more information about NEC's V_R Series call *1–800–366–9782.* Ask for Info Pack #195.

"NEC's V_R Series processor has helped make the Nintendo 64 the most significant consumer electronics product since the VCR."

NEC

READER SERVICE 138



Introducing the

Breakthrough 64M *Synchronous* DRAM.

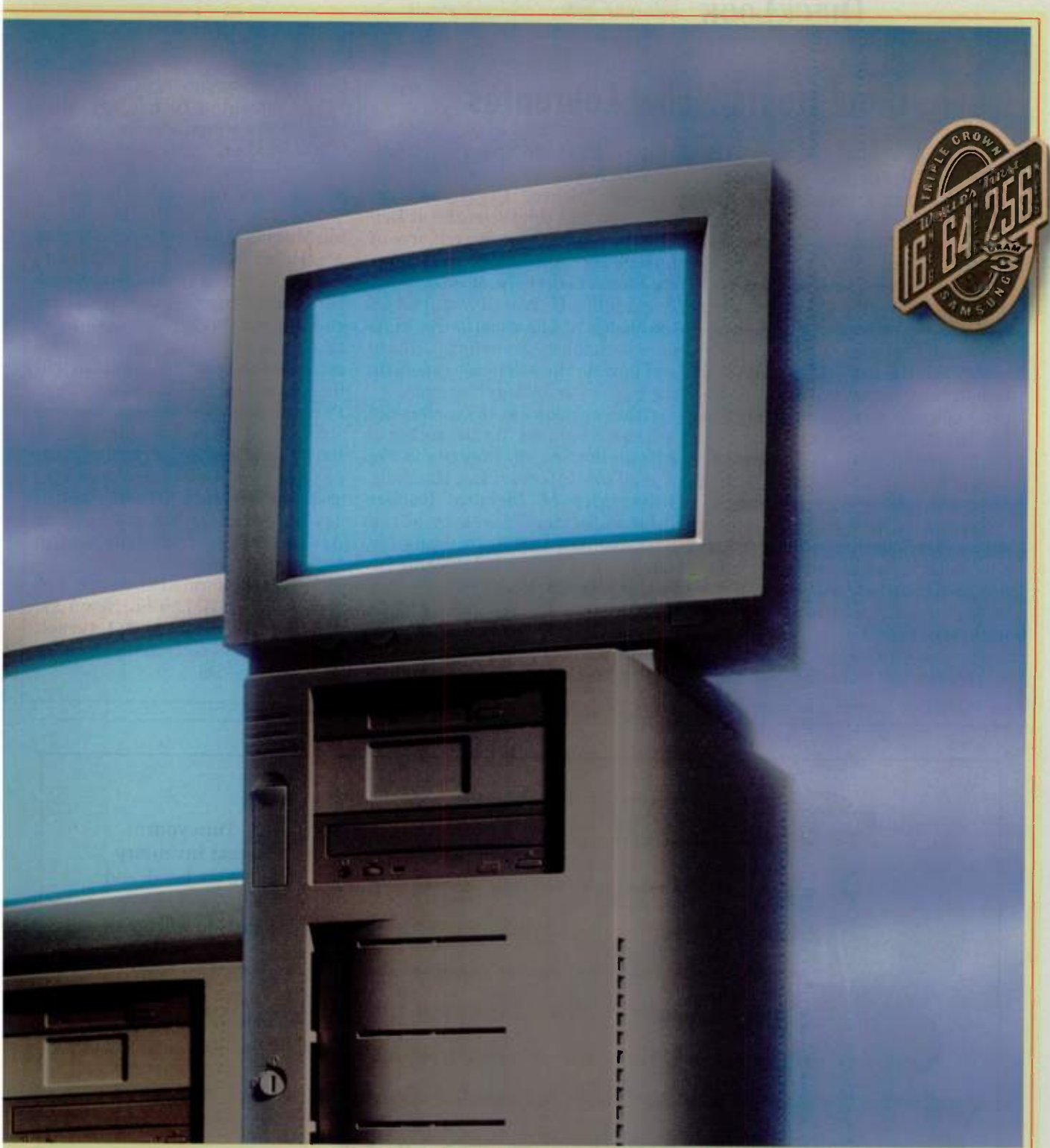
[*It's precisely what servers have been* WAITING FOR.]

You know something's up when you see a bunch of network servers voluntarily queuing up out in the street.

Well, what they seem to know is what you should too: the performance-boosting part that servers crave, the 64-meg Synchronous DRAM, is now available in volume production, or at least it is here at Samsung.

We've had working samples of this 100 MHz chip for some time. And just as we were with samples, we're ahead of the competition with actual production too.

What that in turn means is that you're now in a position to put yourself ahead of your own competition too. Because the 64-meg part gives you the density you absolutely require for servers (and in many cases for workstations), while also delivering the performance advantages you can only get from the new



Synchronous design.

Like we said: the part everybody's been waiting for.

At Samsung, we're proud of this breakthrough product because, like the first 16M, 64M, and even 256M DRAM, and like many of our leadership SRAMS, the new SDRAM helps extend our worldwide leadership in memory products.

But more than that, we're proud it can help our customers continue to attain leadership too.

And incidentally, we promise you won't have to wait in line.

For details on the new SDRAM, please call 1-800-446-2760 today.

Or write to SDRAM Marketing, Samsung Semiconductor Inc., 3655 North First Street, San Jose, California 95134.

SAMSUNG
SEMICONDUCTOR

Still A *Generation* Ahead.

READER SERVICE 158

New School Hosts Nobel Laureates

If you plan to be in the New York metropolitan area during January 16-18, you may want to drop in at the New School for Social Research's conference, "Technology and the Rest of Culture."

Exploring the many ways that today's technologies affect people's self-images, views of their environments, and social structures, "Technology and the Rest of Culture," will look at the positive and negative aspects of these changes. Speakers and participants will discuss the historical precedents and the enormous technological developments that have taken place in recent history.

Topics for discussion at the conference will include ethical and moral issues arising out of emerging technologies; imagination and technology as expressed in art, literature, and philosophy; and relationships between communications technologies and politics and technology.

Nobel Laureate Arno Penzias will give the Keynote Address, "Technology and Culture." Penzias is vice-president and chief scientist at Bell Laboratories, the research arm of Lucent Technologies. Nobel Laureate Joshua Lederberg, an emeritus of Rockefeller University, will sit on the Models of Life panel of the "How does technology transform science and how do the sciences transform the goals of technology?" session.

Other speakers at the conference will include Sherry Turkle, author of *Life on the Screen: Identity in the Eye of the Internet*; Ian Hacking, University of Toronto; Robert Adams, former Secretary of the Smithsonian Institute; Langdon Winner, Rensselaer Polytechnic Institute; Marvin Minsky, Massachusetts Institute of Technology; Alan Ryan, Oxford University; and George Kateb, Princeton University.

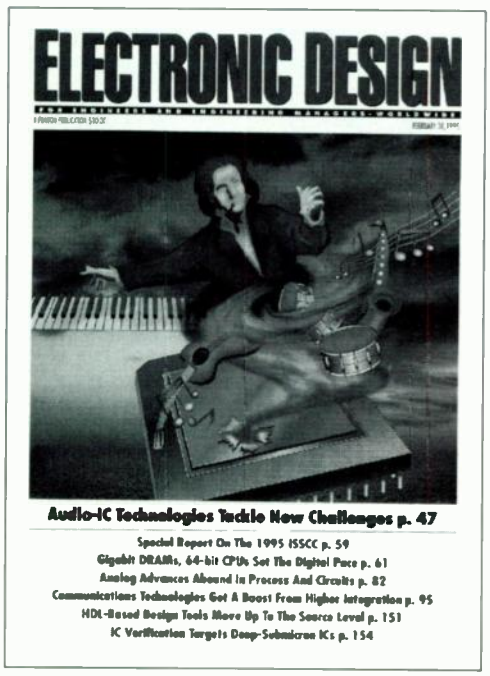
The "Technology and the Rest of Culture" conference agenda includes "The Concept of Technology: History, Definitions, and Critiques," "Case Studies," "Science," Political Life," "Imagination," and "Contemporary Moral and Political Issues."

The New School, The Metropolitan Museum of Art, the Academy of American Poets, and the Getty Information Institute of the Getty Trust have banded together to provide a forum for continuing discussions to take place this spring. Events at locations throughout Manhattan will include exhibits of cyberart at the Parsons School of Design, demonstrations of community planning at the Milano Graduate School of Management and Urban Policy, workshops on "Teaching Art and Technology" at The Metropolitan Museum of Art, and a film series dedicated to technocult at The New School.

For more information, contact The New School, 66 W. 12th. St., New York, NY 10011; (212) 229-2488; Internet: http://www.newschool.edu/whatsnew/techculture.htm.—DS

STRATEGIC PARTNERS WORKING TOGETHER

Information has always been a part of the developmental strategy needed for success in the OEM market. In today's fast-paced, competitive global market environment, technology information has become a priority. Systems designers not only want to know what their strategic supply partners are doing today, but where they're going. Designers and suppliers must now work in tandem to align enabling technology with the customer's system requirements. These strategies demand strong partnerships in the development of competitive products.



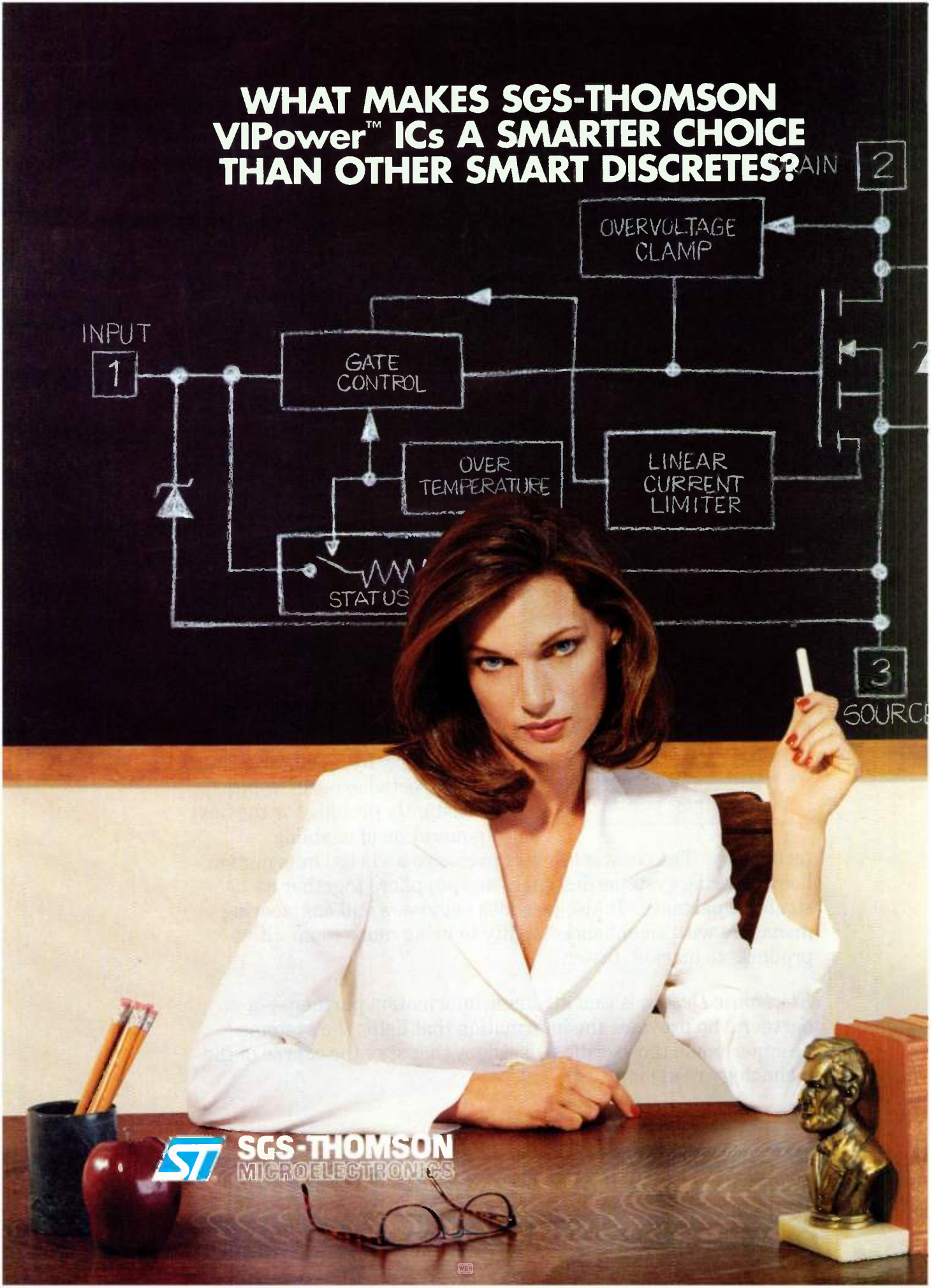
A third strategic partner completes this alliance. This partner's mission is to observe and report today's product availability by its editorial staff of respected experts, while constantly probing for the next generation of enabling technology. The constant flow of exclusive and vital information helps to bring systems designers and suppliers together as strategic partners. It also provides engineers and engineering managers with an enhanced ability to bring more competitive products to market, faster.

Electronic Design is that strategic information partner — a partner who provides the information that helps the systems designer make those critical decisions that stay the course of the technology road map.

Your Strategic Information Partner.

ELECTRONIC DESIGN

A · PENTON · PUBLICATION


WHAT MAKES SGS-THOMSON VIPower™ ICs A SMARTER CHOICE THAN OTHER SMART DISCRETES?
AIN
2
OVERVOLTAGE CLAMP
INPUT
1
GATE CONTROL
OVER TEMPERATURE
LINEAR CURRENT LIMITER
STATUS
3
SOURCE
SGS-THOMSON MICROELECTRONICS

WE'VE DONE OUR HOMEWORK

SGS-THOMSON took VIPower™, the industry's most flexible, most functional truly vertical-flow smart power technology, expanded the range and made it better.

Introducing the OMNIFET™! Fully autoprotected three-terminal Power MOSFETs that are definitely at the head of the class when it comes to performance.

OMNIFETs are based on the same leading edge VIPower technology that has given ST's intelligent high-side drivers bumper-to-bumper presence in the world's leading automobiles. Using ST's proprietary NMOS and DMOS structure, OMNIFETs bring intelligence and protection to industry standard "dumb" MOSFETs. In fact, OMNIFETs are becoming the power switches of choice in industrial applications where high reliability and safety are prime concerns.

OMNIFETs - Fully Autoprotected Power MOSFETs

As logic level devices, OMNIFETs offer more features than their predecessors — TEMPFET® and SENSEFET® — combined. With $R_{DS(on)}$ ranges from 12mΩ to 200mΩ and all industry standard through-hole and surface mount packages available, the OMNIFET product range can meet the most demanding power switching cost/performance parameters.

Do your homework and you'll get a real education on the unprecedented advantages of SGS-THOMSON VIPower devices. Be one of the first 500 respondents and receive a sample kit with complete data and actual devices. Fax 617-259-9442 or write SGS-THOMSON Microelectronics, 55 Old Bedford Rd., Lincoln, MA 01773. And visit our web site at **http://www.st.com**

Service and Technology

READER SERVICE 142

For More Info Turn Page

OMNIFET-VIPower. The Smarter Power.

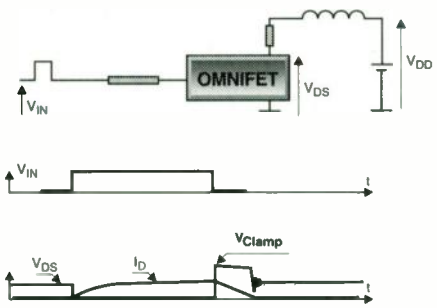
OVERVOLTAGE CLAMP

FEATURES

>Unrivaled energy handling
>Clamp internally set from 42V to 70V

BENEFITS

>No damage due to overvoltage spikes



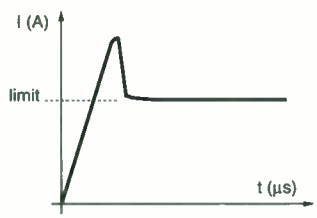
LINEAR CURRENT LIMITER

FEATURES

>Linear current limitation
>Fast step response

BENEFITS

>Load protection
>Adjustable current limit by changing the metal mask



GATE CONTROL

FEATURES

>Analog driving due to direct access to the gate of the Power MOSFET
>Logic-Level operation from a TTL/CMOS driver circuit

BENEFITS

>Pin to pin compatibility with standard MOSFET

OVER TEMPERATURE

FEATURES

>Short circuit protection
>Overtemperature protection
>Automatically restarts at 135°C

BENEFITS

>High safety in all environmental conditions

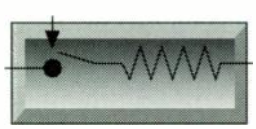
STATUS

FEATURES

>Overtemperature feed back through input pin

BENEFITS

>Real time monitoring



OMNIFETs - AUTOPROTECTED POWER MOSFETs

Type	V_{Clamp} (V)	$R_{DS(on)}$ (mΩ)	Package
VNW100N04	42	12	TO-247
VNW50N04	42	12	TO-247
VNP49N04	42	20	TO-220
VNP49N04FI	42	20	ISOWATT220
VNV49N04	42	20	PowerSO-10
VNB49N04	42	20	D2PAK
VNP35N07	70	28	TO-220
VNP35N07FI	70	28	ISOWATT220
VNV35N07	70	28	PowerSO-10
VNB35N07	70	28	D2PAK
VNP28N04	42	35	TO-220
VNP28N04FI	42	35	ISOWATT220
VNV28N04	42	35	PowerSO-10
VNB28N04	42	35	D2PAK
VNP20N07	70	50	TO-220
VNP20N07FI	70	50	ISOWATT220
VNV20N07	70	50	PowerSO-10
VNB20N07	70	50	D2PAK
VNP14N04	42	70	TO-220
VNP14N04FI	42	70	ISOWATT220
VNV14N04	42	70	PowerSO-10
VNB14N04	42	70	D2PAK
VNK14N04FM	42	70	SOT-82FM
VNP10N07	70	100	TO-220
VNP10N07FI	70	100	ISOWATT220
VNV10N07	70	100	PowerSO-10
VNB10N07	70	100	D2PAK
VNK10N07FM	70	100	SOT-82FM
VNP10N06	60	300*	TO-220
VNP10N06FI	60	300*	ISOWATT220
VNK10N06FM	60	300*	SOT-82FM
VND10N06	60	300*	DPAK
VND10N06-1	60	300*	IPAK
VNP7N04	42	140	TO-220
VNP7N04FI	42	140	ISOWATT220
VND7N04	42	140	DPAK
VND7N04-1	42	140	IPAK
VNK7N04FM	42	140	SOT-82FM
VNP5N07	70	200	TO-220
VNP5N07FI	70	200	ISOWATT220
VND5N07	70	200	DPAK
VND5N07-1	70	200	IPAK
VNK5N07FM	70	200	SOT-82FM

*V_{IN}=7V

For more information fax 617-259-9442
Complete product information at http://www.st.com

SGS-THOMSON MICROELECTRONICS

READER SERVICE 142

Take The A-Training Catalog

New from the Institute for Interconnecting and Packaging Electronic Circuits (IPC) are over 30 1996-1997 Publications and Training catalogs.

Included in the newly-developed publications and videos listed in the catalogs are comprehensive and up-to-date artwork and test boards, specifications, standards, and training for the electronics assembly, design, and printed circuit board fabrication industries.

Some examples of publications that are available include:

•J-STD-012, "Implementation of Flip Chip and Chip Scale Technology," describing the use of flip chip and chip scale technology in semiconductor packaging.

•J-STD-013, "Implementation of Ball Grid Array and Other High Density Technology," examines the interactions and requirements for printed board assembly processes for interconnecting high performance/high pin count IC packages.

•IPC-A-25A, "Multipurpose 1 Sided Test Pattern."

•IPC-A-47, "Composite Test Pattern Ten Layer Phototool."

•IPC-DRM-18, "Desk Reference Manual."

•IPC-T-50-F, "Terms and Definitions for Interconnecting and Packaging Electronic Circuits."

•IPC-SA-61, "Post Solder Semiaqueous Cleaning Handbook."

•IPC-AC-62A, "Aqueous Post Solder Cleaning Handbook."

•IPC-CM-770D, "Guidelines for Printed Boards Component Mounting."

•IPC-1720, "Assembly Qualification Profile."

•IPC-9201, "Surface Insulation Resistance Handbook."

•IPC-TR-465-3, "Evaluation of Steam Aging on Alternative Finishes, Phase 11A.

•IPC-D-279, "Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies."

•IPC-A-311, "Process Controls for Phototool Generation and Use."

•IPC-2141, "Controlled Impedance Circuit Boards and High Speed Logic Design."

In addition, the IPC catalog features a full line of training videos with demonstrations such as "Rework of J-Lead Components," "Handling in Electronic Assembly," "Solder Paste Printing," "ESD Control Training," "Introduction to Electronics Assembly," "Hand Soldering with Residue Flux," "Flexible Circuits Manufacturing," and "Ball Grid Array Rework."

For more information on the publications and training catalogs, contact IPC, 2215 Sanders Rd., Northbrook, IL 60062-6135; (847)509-9700; fax (847) 509-9798; Internet: http://www.ipc.org.

U.S. Factory Sales Approach $300 Billion By End Of Third Quarter 1996

Factory sales of electronics equipment and products in the United States reached $295.6 billion for the first nine months (Third Quarter) of 1996. The total represents an increase of 10% over 1995's total of $269.4 billion for the same period of time, according to data recently released by the Electronic Industries Association (EIA).

•The following is a breakdown of sales performance by industry sector, along with percentage of increase or decrease from the previous year-to-date (YTD):

•Electronic Components sales reached $82.4 billion, 9% over $75.5 billion in 1995 (YTD);

•U.S.-produced Consumer Electronics sales rose 5% from $6.9 billion in 1995 to $7.3 billion in 1996 (YTD);

•Telecommunications sales jumped from a total of $38.4 billion in 1995 to $44.6 billion in 1996 (YTD), an increase of 16%, the largest increase of any sector;

•Defense Communications sales decreased slightly (2%) to $20.7 billion in sales for 1996 from $21.2 billion in 1995 (YTD);

•Computers and Peripherals rose to $60.7 billion in 1996 from $53.2 billion in 1995 (YTD), a 14% increase;

•Industrial Electronics sales rose 7% to $26.6 billion in 1996 from $25 billion in 1995 (YTD);

•Electromedical Equipment sales reached $7.7 billion in 1996, an 8% increase from $7.2 billion in 1995 (YTD);

•The Other Related Products sector jumped 9% from $41.7 billion in 1995 to $45.3 billion in 1996 (YTD).

For more information, contact the EIA, 2500 Wilson Blvd., Arlington, VA 22201-3834; (703) 907-7500; fax (703) 907-7501.

ISDN Use Crawling Along

Integrated Services Digital Networks (ISDN) have begun to provide broadband solutions for business and home workers. On the other hand, its use has reached less than 1% of all lines installed worldwide. Thirty-five countries around the world currently use ISDN as a commercial service, but only Germany has reached a level of use at roughly 5%.

Second to Germany in level of ISDN use is France at 4.75%, followed by Switzerland at 2.79%. The United States' level of ISDN use is 0.46% out of a total of 157 million telecommunication lines, by far the most of any country. It is estimated that there are 650 million total telecommunications existent worldwide.

According to IGI Consulting (IGIC), Boston, Mass., as telecommunications markets become more competitive, the availability of information on actual lines sold, growth rates, penetration rates, etc., is sparse and hard to find.

To that end, IGIC is making available "ISDN Penetration in Selected Countries," a report that attempts to identify countries that have introduced ISDN into use and the number of subscribers and growth rates. The two-volume set on ISDN deals with actual lines sold, growth rates, penetration, tariffs, and contracts.

The U.S. volume specifically contains detailed tariff filings of each major telco, contracts, and identifies the Public Utilities Commission in each of the 50 states.

For more information, contact IGIC, 214 Harvard Ave., Boston, MA 02134; (617) 232-3111; fax (617) 734-8562.—**MS**

EYE ON ISO 9000

LeBow Products, a division of Eaton Corporation, has received ISO 9001 certification. The company markets, designs, and manufactures precision rotary in-line and reaction torque sensors, as well as fatigue-resistant and general-purpose load cells. Contact LeBow Products, P.O. Box 1089, Troy, MI 48099-1089; (810) 643-0220; fax (810) 643-0259.
CIRCLE 626

Edac Inc. has recently achieved ISO 9001 registration. The company designs and manufactures connectors of various sizes and styles, including rack and panel, waterproof, and D-subminiature connectors. Contact Edac Inc., 40 Tiffield Rd., Scarborough, Ontario, Canada M1V 5B6; (416) 499-3994; fax (416) 499-6640; Internet: http://www.edac.net.
CIRCLE 627

Lytron Inc. has received ISO 9001 certification. The company's cooling-equipment product line includes water chillers, ambient cooling systems, oil coolers, and heat exchangers. Contact Lytron Inc., 55 Dragon Ct., Woburn, MA 01801-1039; (617) 933-7300; fax (617) 935-4529. **CIRCLE 628**

Hybricon Corp. has achieved ISO 9001 certification. The company is a supplier of backplanes and enclosures to the electronics industry. Contact Hybricon Corp., 12 Willow Rd., Ayer, MA 01432; (508) 772-5422; fax (508) 772-2963; Internet: http://www.hybricon.com.
CIRCLE 629

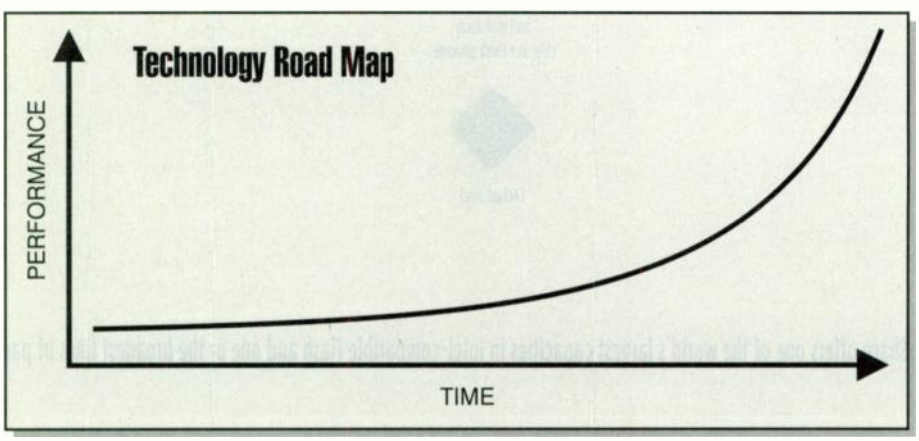
Vectron Laboratories Inc. has received ISO 9001 registration. A division of the Vectron International group, the company designs and manufactures crystal oscillators. Contact Vectron Laboratories Inc., 166 Glover Ave., P.O. Box 5160, Norwalk, CT 06856-5160; (203) 853-4433; fax (203) 849-1423; Internet: http://vectron-labs.com. **CIRCLE 630**

STRATEGIC PARTNERS WORKING TOGETHER

In today's competitive global marketplace, customers need to bring their supplier's enabling technology in alignment with their own systems requirements. Systems designers want to know, not just where their strategic suppliers are today, but where they are going.

But systems designers have another working-together partner, an objective strategic information partner who not only reports on what's available today, but who is constantly scanning the technology horizon to help engineers and engineering managers plan for their next designs; helping them figure out which technologies will be useful and which will end up on the scrap heap.

Electronic Design is that strategic information partner. By providing the information that helps the system designer walk the line between leading edge and bleeding edge, *Electronic Design* helps the engineer get a more competitive product to market, faster.



Your Strategic Information Partner.

ELECTRONIC DESIGN

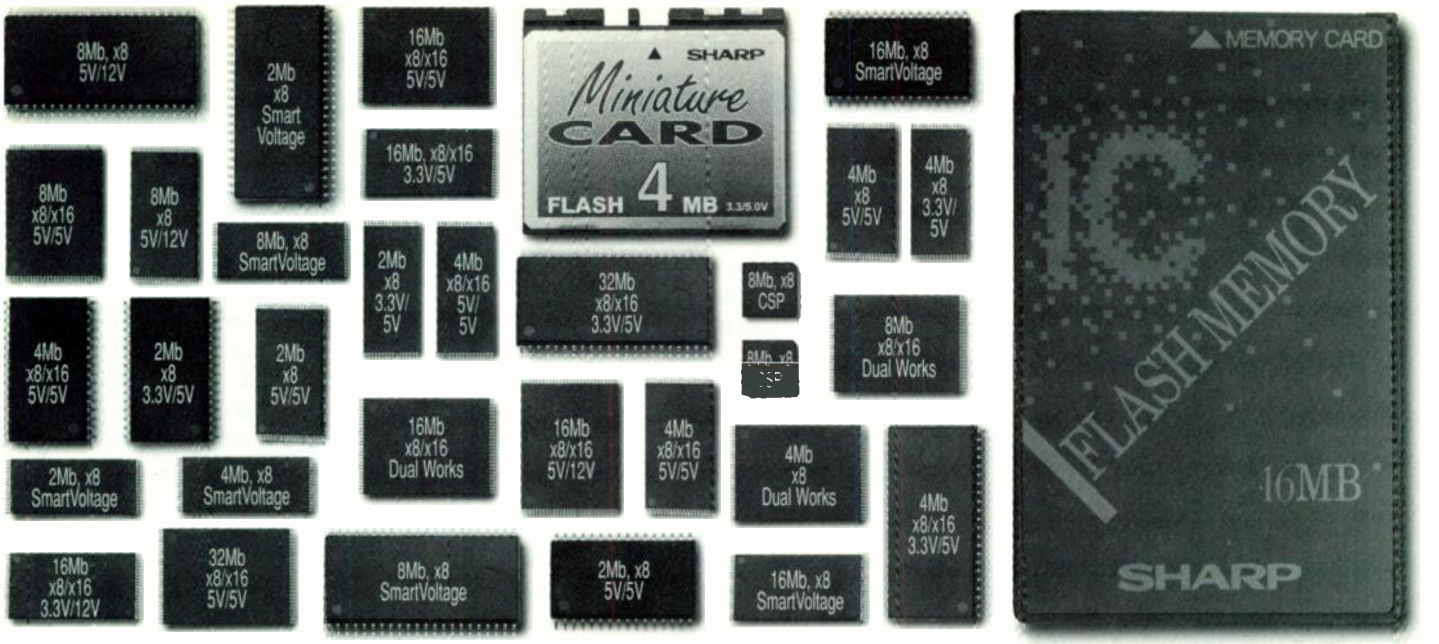
A · PENTON · PUBLICATION

The world's smallest Flash producer...

Sharp's 8x8mm, 8Mb,
ball grid array
chip-size Flash package.

(Actual size)

Commit this to memory: Sharp offers one of the world's largest capacities in Intel-compatible Flash and one of the broadest lines of packages and densities–including



is also the biggest.

ıe smallest chip-size package of all. For all the reasons to source your Flash from Sharp, call 1-800-642-0261, ext. 404. Or get detailed product data from our web site.

SHARP®

FROM SHARP MINDS COME SHARP PRODUCTS™

www.sharpmeg.com/flash

READER SERVICE 149

Inventor Documented In Smithsonian

The late H. Joseph Gerber, prolific inventor and founder of Gerber Scientific Inc., is now the subject of a documentary video taped for archival purposes by the Smithsonian Institution, Washington, D.C., on behalf of its National Museum of American History.

Gerber, who died in August of 1996 at the age of 72, has several of his inventions on display at the Smithsonian; inventions that have been cited as "key examples of technological and innovative development in U.S. history" by museum officials. He personally held more than 600 patents at the time of his death.

Peter Liebhold, curator of the National Museum of American History, visited Gerber Scientific Inc., the parent cooperation of Gerber Systems Corporation, this past fall to capture the essence of Gerber and his high-tech company via on-camera interviews with Gerber's colleagues, relatives, and friends. Liebhold first became aware of Gerber's contributions to the advancement of automated manufacturing in this country a few years ago, and has since spent a considerable amount of time researching the man and his accomplishments.

To thoroughly document the role Gerber and his inventions have played in promulgating factory automation domestically, Liebhold and his camera crew also visited the Chic blue jeans factory in Tennessee and General Motors Corp., Grand Rapids, MI, two of the largest installations of the Gerber-Cutter, one of Gerber's first commercial successes. Other technological advancements, which span nearly half a century, have created a legacy for Gerber and his corporation in electronics, graphic arts, commercial printing, sign making, and additional industries worldwide.

Those interested in more information on the documentary video on H. Joseph Gerber should contact Gerber Systems Corp., 83 Gerber Road West, South Windsor, CT 06074-3246; (860) 648-8187; fax (860) 649-7157; Internet: http://www.gerbersystemscorp.com.

Long Distance Research

With the help of the University of Pittsburgh's Library System, the Peking University Library now is the first Chinese academic library in the People's Republic that has the ability to electronically deliver research materials to libraries in the West.

The two libraries have formed a partnership to provide electronic document delivery across the Pacific for library patrons of both institutions. This marks one of the first such services between a North American library and a library in China. The Pittsburgh University Library System and Peking University Library successfully completed a test that transmitted full-text documents through Ariel software on the Internet. Pittsburgh University Library System Director Rush Miller initiated the international project while visiting Beijing in August.

"The successful establishment of an Internet linkage between the libraries of the University of Pittsburgh and Peking University, China's premier University, is a milestone in the long history of cooperation between the academic institutions of both countries," Miller said. "We anticipate that this ability will provide a significant enhancement to scholars on both sides of the Pacific Ocean. Now that we have demonstrated for the first time that this technology can be utilized for resource sharing with libraries in China, we plan to extend our partnerships to other major libraries in China."

Document delivery through cyberspace provides access to the vast information resources of both countries. University of Pittsburgh scholars now can receive full text materials in hard-to-find Chinese journals from Peking University Library through the Internet. At the same time, the University of Pittsburgh's Library System can provide reciprocal document delivery.

For more information on the partnership program between the libraries, contact the University of Pittsburgh, Office of Communications, 400 Craig Hall, Pittsburgh, PA 15260.

Business Projector Market Will Top $2 Billion By 1999

Recent studies show that the business projector market, comprising units that sell for $5000 to $15,000 and project large and bright images from video or computer signals, will continue to grow at a rapid rate. Pacific Media Associates, Mountain View, Calif., estimates that the worldwide market for these products will grow from a total of $1.235 billion in 1995 to $2.318 billion in 1999, an annual growth rate of 17%.

These findings are part of Pacific Media Associates' "LCD & DLP Projectors Market Report." The report provides a detailed analysis of the market, and also give estimates on a company-by-company basis. In addition, the report breaks down the total business projector market by resolution, basic design architecture, and product size.

Dr. William L. Coggshall, founder and president of Pacific Media Associates, believes that some portions of the market will grow strongly, while others may stagnate. "By 1999, we expect data-capable projects, those with at least VGA resolution and the capability to accept computer signals, to account for roughly 90% of the total ($2.318 billion)," he says. "The current hunger for SVGA resolution is just part of a longer-term trend toward higher resolutions that reflect the higher resolutions of computer monitors."

On the other hand, the market growth may not be large enough to sustain a number of companies that have targeted it. Due to intense competition, significant price increases are one major consequence. However, as is the case with most high-technology products, there is a pattern of decreasing manufacturing costs, so that manufacturers with critical mass and solid business strategies will prosper.

For more information, contact Pacific Media Associates at 1121 Clark Ave., Mountain View, CA 94040; (415) 948-3080; fax (415) 948-3092.

JOIN US AT CHINA'S LARGEST ELECTRONICS EXHIBITION

SEPTEMBER 24-28, 1997

The China International Exhibition Center
Beijing, China

CIEE '97 is known for its consistently high-quality base of attendees. These attendees are influenced by the show's organizers, CEIEC and CCPIT. The CEIEC is the US$2.5 billion import-export arm of the Ministry of Electronics Industry and the seventh largest trading company in China. Prior to the show, Exhibitors will be able to utilize the CEIEC's extensive network of 41 branch offices and over 100 affiliate electronics companies in China to distribute information and literature to buyers and specifiers of overseas electronics products throughout the country. Exhibitors will also have the inside track on import/export information and be able to take advantage of meetings and trade negotiations during the show.

AT THE 1995 SHOW:
502 EXHIBITORS
from over 15 Countries
Over 200,000 Attendees
from China's
electronics companies

Call your *ELECTRONIC DESIGN CHINA* sales representative today for complete details. Don't wait. Reserve your company's booth today. 408/441-0550, ext. 101; fax: 408/441-6052.

CHINA INTERNATIONAL ELECTRONICS EXHIBITION
CIEE '97 is sponsored by the Ministry of Electronics Industries (MEI) of the Peoples Republic of China and organized by the China National Electronics I/E Corp. (CEIEC) and the China Council for the Promotion of International Trade (CCPIT).

WHO SHOULD EXHIBIT?

CIEE '97 will showcase a wide range of electronic components, devices, and equipment. The profile of exhibitors includes manufacturers of the following:

- Surface-Mounted Components
- Semiconductor Devices
- Vacuum Devices
- Integrated Circuits
- Connectors
- Switches, Keys & Relays
- Wire & Cable
- Materials
- PCB
- Communications Equipment
- Production Assembly Equipment
- Test & Measurement Equipment
- Power supplies
- and more...

ELECTRONIC DESIGN CHINA
A PENTON PUBLICATION
Official U.S. Sales Representative for China's Largest Electronics Show

A Complete Solution for CPLDs & FPGAs!

Enhanced VHDL Synthesis for $99

It's surprising, but true. For only $99, Cypress's new *Warp2*™ Release 4.0 offers better behavioral synthesis than tools costing more than $20,000! New UltraGen™ technology uses module generation to provide the best VHDL synthesis for FPGAs and CPLDs, as well as providing area and speed optimization for precise synthesis control.

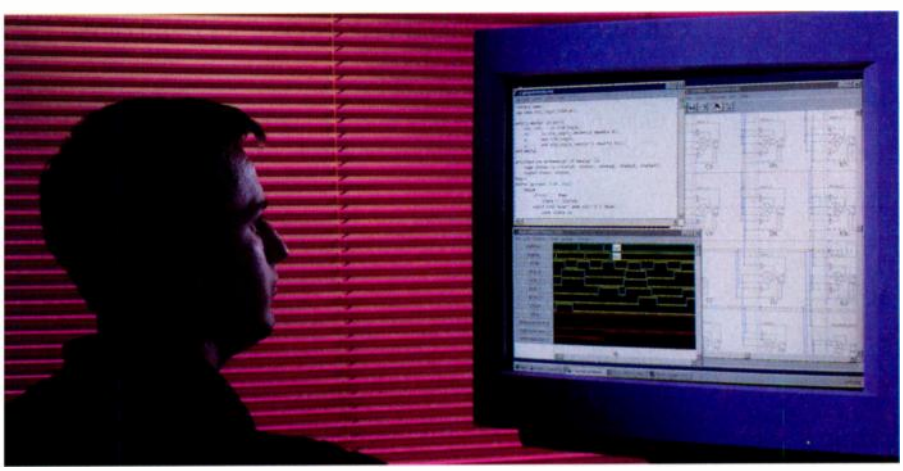
$20,000 VHDL SYNTHESIS FOR $99.00
Warp2 RELEASE 4.0

Everything You Need for Real VHDL Designs

Warp2 is a complete development system for all high-performance Cypress PLDs, CPLDs, and FPGAs.

The *Warp2* kit includes:

- IEEE standard behavioral VHDL synthesis
- Automatic fitting and place-and-route
- VHDL & Verilog timing simulation output
- NOVA functional waveform simulator
- "VHDL for Programmable Logic" book

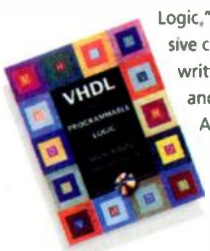


***Warp2* Release 4.0 Supports:**

pASIC380™ FPGAs	7C381/2 (1000 gates) 7C383/4 (2000 gates) 7C385/6 (4000 gates) 7C387/8 (8000 gates)
FLASH370i™ CPLDs	7C371i (32 macrocells) 7C372i (64 macrocells) 7C373i (64 macrocells) 7C374i (128 macrocells) 7C375i (128 macrocells)
MAX340™ CPLDs	7C344 (32 macrocells) 7C343 (64 macrocells) 7C342 (128 macrocells) 7C346 (128 macrocells) 7C341 (192 macrocells)
Simple PLDs	PALCE16V8 PALCE20V8 PALCE22V10

FLASH370i, MAX340, pASIC380, UltraGen, and *Warp2* are trademarks of Cypress Semiconductor.
All others are trademarks of their respective manufacturers.

Order *Warp2* today and receive a free copy of "VHDL for Programmable Logic," a comprehensive college textbook written by Cypress and published by Addison-Wesley.



Order the New $99 *Warp2* Kit Now!

Platform:

❑ PC (Windows 3.1, Win'95, NT)
❑ Workstation (HP-UX, SunOS, Sun Solaris)

Please bill my:

❑ VISA ❑ MasterCard

Name _____

Title _____

Company _____

Address _____

City _____ State ____ Zip _____

Phone _____

FAX _____

E-Mail _____

Credit Card # _____

Exp. Date _____

(Sales tax will be added as appropriate. $10 shipping & handling in the U.S., $15 in Canada)

FAX to: 1-408-943-6848

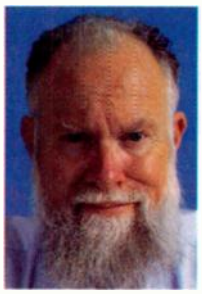
or call: **(800) WARP-VHDL, Kit #U021**

ULTRA LOGIC

CYPRESS

BOB PEASE

Bob's Mailbox



Dear Bob:

Earthing problems on cars can lead to strange phenomena. A while ago, my neighbor came rushing over to me saying when he pressed the starter switch on his car, all he got was clouds of smoke from the choke cable! This even puzzled me at first, but I soon discovered that as the engine is mounted on rubber mounts, the starter motor bolted to it relies on a heavy earthing braid to chassis. This was not making good contact, so the current found an alternate route down an oily choke cable. Hence the smoke.

MIKE DAVIES
England

P.S. I do enjoy your column, but sometimes it's excessively wordy We tend to be a bit more economical with our words over here.

Yes, troubleshooting cars can be challenging. When the problem gets gross enough, it's easy to find, solve, and fix. But the intermittent, rare, sparse problems are tough to find.

In your part of the world, are you familiar with the saying, "I didn't have time to write a short letter, so I wrote a long one?" When I am writing a column, it's not easy to edit down. If it fits on a page, we usually quit. I apologize for being too wordy at times.—RAP

Dear Robert Pease:

Your most recent column on matching transistors was fun. I worked for dbx in the late 70's, and our VCAs were (and today That Corp.'s, the licensee of dbx patents) based on log/antilog principles. We learned very well that a bipolar transistor's collector current, over at least a 140-dB range, is so related to the emitter-base voltage. But to build a good VCA you had to have good NPNs AND good PNPs. Something that was not done on ICs. So we bought transistors, matched them very carefully (at two temperatures!) and then put them into a ceramic holder.

Unfortunately, symmetry doesn't help here. All transistors must be at the same temperature for all errors to fall toward zero. In 1977, while at dbx, I developed a circuit to compensate for errors in the VCA. At that time we could buy dual transistors in a five-pin in-line configuration. We found that wrapping aluminum or copper tape around the package helped a great deal. Then we potted the whole thing in a soft compound inside a metal can. In fact, we even layered a sheet of ceramic in the bottom of the can, insulated with a piece of cardboard, before we put in the small board with our VCA on it. (Thermal conductor, insulator, conductor, insulator, etc.) When we got done, we could touch a soldering iron to the outside of the package for seconds without it causing additional distortion in the VCA. (In a regular VCA you could touch the transistor core, mounted in the ceramic heat sink, with your finger for 1/2 second and send the distortion meter off scale!)

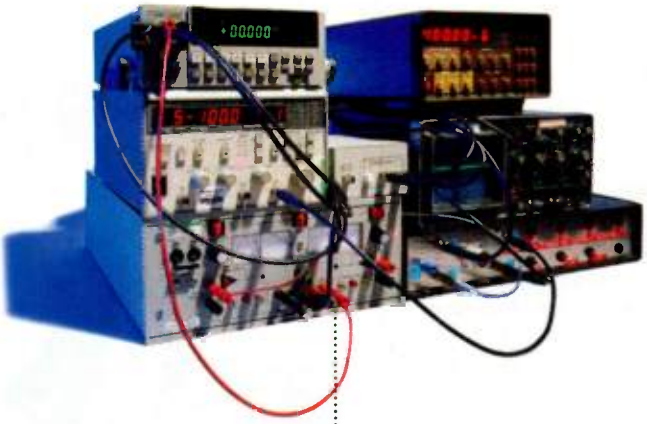
I've always felt that people doing high-end audio design are the best (low frequency) analog designers around. The challenges of getting audio performance to new highs seems harder than any other area I've seen. (This includes the voltmeter/instrument manufacturer that I worked at.) Designing a 6-1/2 digit voltmeter in 1983 was easier than the audio product design at dbx. Note that I don't think that all of the expensive audio gear today is necessarily high-end audio.

GARY BERGSTROM
Bergstrom Consulting
Chagrin Falls. Ohio

Yeah, 6-digit DVMs are almost easy—all they have to do is give some linear transfer. Transistors aren't nearly as easy to work with. Nor loudspeakers.—RAP

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

Address:
Mail Stop D2597A
National Semiconductor
P.O. Box 58090
Santa Clara, CA 95052-8090



Well, it works.

It works well.

The new Model 2400 Digital SourceMeter™ for DC testing and characterization. Stimulus. Measurement. Keithley support. All in one *little* package.

For production applications such as component testing, the Model 2400 Digital SourceMeter makes your life simpler. Easy to set up and use, it eliminates the connections and compatibility problems of two or more separate units, while providing convenient DMM-like operation. This high-throughput, high-accuracy, single-channel DC parametric tester combines a precision power supply and a highly repeatable 5½-digit DMM. When coupled with a Keithley 7000 Series Switching System, the Model 2400 gives you a complete multi-point test solution. *For a free brochure, contact Keithley today.*

KEITHLEY

SPEC DIRECT 1-800-936-3300 FAX 216-248-6168
TELEPHONE 1-800-552-1115
E-MAIL product_info@keithley.com
WEB http://www.keithley.com

Specifications

Range of operation:
20W max: ±20VDC @ ±1A, ±200VDC @ ±100mA

Resolution:
5½ digits (1µV, 10pA max)

Source output modes:
Fixed level, pulse, stair, logarithmic

1 year basic accuracy:			Max system speeds:		External interface:
	Source	Measure			
Voltage	0.02%	0.01%	Pass/fail = 500µs		IEEE-488 (SCPI)
Current	0.03%	0.02%	To memory = 500µs		RS-232
Resistance	—	0.04%	To IEEE-488 = 1000/s		Digital I/O
			Range change = 75/s		Component handler

HOWARD JOHNSON

The Jitters

Have you noticed what's happening in the world of clock specifications lately? It used to be that the only things that mattered in a clock specification were the frequency and the duty cycle. Between these two specifications, vendors were really just setting limits on the minimum time high and the minimum time low each period. A few complications arose with the advent of DRAM technology, like the need for maximum bounds on the clock period, but that was about it.

Recently the whole clock scenario has undergone massive change, due mostly to the widespread use of PLL-based clock recover schemes used in serial data communications equipment, PLL-based clock multipliers, and PLL-based clock regenerators. The basic premise of a PLL is that it carefully adjusts its own clock, called the "local oscillator," to bring it into precise alignment with some external signal, usually called the "reference clock."

The PLL concept was first developed for use in radio, and later adapted for use in serial data communications. In the serial data application, the reference clock is often embedded, sometimes in very subtle ways, in a stream of data bits. It is the job of the PLL in the clock recovery subsystem to align its local oscillator with the reference clock information embedded in the data stream. Once properly aligned, the local oscillator can be used to clock bits out of the data stream, sampling each data baud right in the center, at the point of maximum noise immunity.

In this application, any imperfections in the transmit clock used to construct the data stream may compromise the PLL's ability to properly align its local oscillator. Imperfections in the transmit clock are sometimes classified as frequency offsets, wander, and jitter.

"Frequency offset" refers to any long-term deviation between the actual transmitted clock frequency and the ideal. For example, crystal-controlled transmission systems are expected to attain frequency offsets as low as a few hundred parts per million. This specification is measured with a frequency counter, averaging all clock pulses over a period of perhaps many seconds.

A PLL-based clock recovery subsystem is designed to accurately lock-in to any reference signal within the permitted frequency offsets. The frequency offset specification has more to do with whether a PLL will lock-in than with the quality of clock recovery, once lock-in has occurred.

HOWARD JOHNSON

"Clock wander" refers to the tendency of a clock reference to exhibit short-term frequency variations. PLLs are designed to track the short-term wander, provided they don't slew too fast or wander too far afield. The permitted amount of wander, the rate at which a signal may wander up and down across the permitted frequency rate, and the slew rate of the wander are key to a good wander specification.

"Jitter" refers to the fastest variations in clock frequency. It comprises those variations too fast to expect the PLL to track. Therefore, jitter always directly affects the accuracy of the timing relation between the reference clock and the local oscillator. In a data communications application, excessive jitter causes bit errors.

O.K., so clock purity is important in data communications applications, we all knew that; but what does clock purity have to do with plain old digital design? Plenty, as we will see, because the same PLL-based clock recovery technology is being widely used to generate multi-hundred megahertz, very low-skew processor clocks in the latest generation of clock-generator chips from AMCC, Chrontel, PLX, Quality Semiconductor, Triquint, and many others.

These new devices are flexible, fast, and packed with features. Most incorporate three basic ideas: A reference clock, a PLL clock multiplication circuit, and a way of maintaining very low skew among multiple clock outputs.

In a typical clock multiplier application, the reference clock is often sourced at about 10 MHz from a traditional crystal oscillator. Ten MHz is a very comfortable range for crystals, and it's a good bet you already have one in your system.

To multiply the clock, it is run into a PLL-based clock multiplication circuit. In a multiply-by-ten circuit, for example, the PLL aligns every tenth edge of the local oscillator to the reference clock, thus generating a 100-MHz output. PLL technology also can be used to create zero-delay clock buffers, automatically adaptive skew correction circuits, and other neat features. The combination of PLL, output drivers, and skew correction circuitry is fabricated as a single chip.

What can go wrong? Plenty. Suppose we're feeding rotten power to the crystal source (it may have 100-KHz switching noise on it from the power system). If the crystal output violates the offset, wander, or jitter tolerance of the PLL circuit, the 100-MHz output goes nuts. It may fail to lock, drifting to one end or the other of its range, it may flagellate up and down, or, depending on the PLL architecture, it may detect an absence-of-lock condition and shut off.

What if the clock multiplier is built inside your processor (like with a Pentium processor)? Then, the quality of the incoming clock has everything to do with the quality of the resulting system.

If you're using a clock multiplier or a PLL-based clock regenerator, make sure to comply with the specifications for offset, wander, and jitter on the reference clock input. If you have the specifications, test them; if you don't, get them, and if your vendor won't fork them over, think carefully about the consequences before moving ahead with your system design.

Dr. Howard Johnson is president of Signal Consulting Inc., a high-technology consulting firm specializing in solving high-speed digital design problem. He regularly presents technical workshops for digital engineers, including courses for Oxford University and UC-Berkeley. He is the author of "High-Speed Digital Design: A Handbook of Black Magic" (Prentice-Hall, 1993). He can be reached at (206) 556-0800; fax (206) 881-6149; e-mail howiej@sigcon.com.

INSTRUMENTS

System Acquires Data Remotely Over Ethernet

The EDAS-1002E-1 multifunction system supplies 16 single-ended or eight differential analog inputs at 12-bit resolution, two 12-bit analog outputs, and 16 digital I/O channels. The unit's ADC samples waveforms at up to 100 kHz, and a programmable gain amplifier extends the input range with gains of 1, 10, and 100. A 16-bit counter channel performs frequency measurements and event counting to 250 kHz. EDAS systems communicate over any Ethernet LAN or over the Internet using a built-in TCP/IP protocol. This allows for management-level visibility of plant-wide and enterprise-wide processes. The EDAS-1002E-1 costs $1195. A FactoryView Starter Kit (EDAS-1002E-SK1) costs $1645. JN

Intelligent Instrumentation Inc., 6550 S. Bay Colony Dr., MS130, Tucson, AZ 85706; (800) 685-9911; (520) 573-0887; fax (520) 573-0522; Internet: http://www.instrument.com

CIRCLE 690

Analyzer Evaluates SCSI Fast-20 Buses

The SCSI-View Model SV-1620 notebook PC-based system offers complete analysis of wide and narrow SCSI systems that run at up to Fast-20 speeds and use either single-ended or differential interfaces. The unit also can analyze the SCAM protocol used in plug-and-play SCSI systems. Measuring 5.7 by 3.6 by 0.81 in., the analyzer comes with a cable that plugs into the PCMCIA Type 2 slot in the notebook (486- or Pentium-based). The timing view displays SCSI waveforms at 10-ns resolution and allows users to search for unique sequences. The performance view analyzes each SCSI device for data burst rate, command overhead, completion time, and tag queue depth. The SV-1620 costs $3995; the 10-ns timing waveform option costs $895. JN

Verisys Inc., 2901-B Research Park Dr., Soquel, CA 95073; (408) 464-4292; fax (408) 464-4290; Web: http://www.verisys.com

CIRCLE 691

Lab Supply Series Covers Extensive Range

The L Series power supplies are designed for benchtop and portable applications that don't require program mability. The family consists of 14 models, with outputs from 0 to 300 V at power levels from 90 to 375 W. They are four configurations: the LS (small output), LM (medium output), LH (high output), and LT (triple output). The latter models have three independent and isolated outputs, two adjustable from 0 to 100% of voltage and current rating and one fixed at 5 V and 3 A. The supplies automatically cross over between voltage and current sourcing based only on load demand. Remote analog programming of voltage or current is available on the LS series. The ac input is externally selectable for 100, 120, 220, or 240 V at 50 or 60 Hz. Prices start at $335. JN

Elgar Corp., Sorenson Div., 9250 Brown Deer Rd., San Diego, CA 92121; (800) 525-2024; (619) 450-0085; e-mail: sales@elgar.com

CIRCLE 692

EMBEDDED

Programming Language Targets Motion Control And Automation

MINT (Motion INTerpreter) is an advanced Basic-style programming language for motion control and automation applications. A powerful DSP engine and high-level motion commands make the system ideal for programming complex mechanical motions involving up to 64 axis. It supports cams, gears, helical interpolation, cubic splines, inverse kinematics and more. It also combines support for event-driven and scanned I/O tasks that feature advanced communications features for connecting to MMIs, host controllers, and other serial devices. CAN bus connectivity provides a 1-Mbit/s, high-security, machine-level network for simple distribution of motion and I/O with minimum wiring. Other features are an on-board editor and immediate command execution. ML

Optimised Control Inc., 3923 Coconut Palm Dr., Suite 107, Tampa, FL 3619; (813) 626-0780.

CIRCLE 693

Source-Level Debugger Features Multitasking

Based on the UDB debugger, Accelerated Technology's Nucleus UDB is available on the MIPS, i960, ARM, and 29K processors. As a source-level debugger for the embedded market, it incorporates all standard display and control facilities, including the ability to monitor C source code, assembly, registers, global variables, inspectors, and the like. Sophisticated breakpointing and tracing capabilities also are provided. Nucleus UDB runs on both Unix and Windows hosts. The multitasking facilities are currently available only on the Windows version of the product. Debugging is performed remotely by connecting the target environment to the host (Unix or Windows machine) by serial, Ethernet, or other medium. Per-seat pricing starts at $1995. ML

Accelerated Technology Inc., 720 Oak Circle Drive East, Mobile, AL 36685; (334)-661-5770 or 1 (800) 468-6853; e-mail ; sales@atinucleus.com.

CIRCLE 694

Windows NT Program Manages Data Libraries

Previously developed for the VAX Open VMS environment by Acorn Software Inc., Virtual Branches data library management and robotics control software now is available for Windows NT systems. Virtual Branches allows system administrators to use inexpensive optical storage to hold large amounts of data near-line, without consuming additional hard disk space. It's compatible with a range of optical and CD-ROM jukeboxes and enables users to view the library disks as simultaneously mounted virtual-disk volumes. Data can be retrieved from the disks regardless of their physical location. Virtual Branches can be downloaded from the company's website at http://www.acornsw.com. Free software is available for a 45-day trial period before purchasing a license. ML

Acorn Software Inc., 267 Cox St., Hudson, MA 01749; (508) 568-1618; e-mail: info@acornsw.com.

CIRCLE 695

READER SERVICE 97

meant that Bell Labs identified a select group of college campuses that were of primary importance to the hiring of new technical people and a second group of campuses of secondary importance. Each campus would be managed through teams of dedicated staff people—appropriately called Campus Managers—and supported by Campus Angels and Executives who were senior people in the research and business communities. The idea was to develop a close relationship with the school, and to have in-depth contact with potential recruits.

Hiring new technical staff right off the campus is a key philosophy in the Research group at Bell Labs. About 60% of all newcomers get their jobs in this way, with the remaining 40% being "market hires," or those with experience working for other companies. Why is recruiting tilted towards the campus? As Mel Cohen puts it, "Even though market hires are important for specific types of jobs, we feel that the energy and creativity for the future flows from the young people. But market recruiting will play a significant role in future hiring."

On-campus recruiting for the Research group concentrates heavily on candidates with Ph.D.s, but for the Development Labs, recruiting is more at the bachelors and masters levels. No matter what the degree however, Cohen says that the mix of technical disciplines required of new hires is changing to meet the demands of the fast-paced worlds of communications and computer technology. In the past, backgrounds in the physical sciences were stressed, but today's requirements are heavily weighted towards software design, networking, and computer sciences. This fact holds true not only in Bell Labs, but in Lucent's other business units as well.

In addition to a strong technology background, a Bell Labs job candidate must be a high-bandwidth person. This moniker means that the individual must be more well rounded than candidates of the past and have demonstrated leadership skills. At the colleges where the Labs recruit, most students should have taken leadership courses that cover the soft skills such as interpersonal communications, interacting with people and working in teams. These days, it is important, as Cohen points out, that a person not only have a strong scientific inclination, but an ability to work in team situations as well.

Once a candidate is hired at the Research group of Bell Labs, he or she will find no formal orientation or education program. However, the group is discussing a technical excellence initiative that will define a best practices training curriculum for all employees to attend. Instead of classroom training, the group offers an informal mentorship program whereby a new person is attached to a senior member of the staff, who may well be a world leader in a specific area of technology. This arrangement would not be unusual at Bell Labs considering that its members have established a long history of high achievement in science. Bell Labs professionals have won seven Nobel Prizes in Physics dating back to 1937 and five National Medals of Science, the most recent in 1993. Bell Labs also was the first winner of the National Medal of Technology in 1985.

Newcomers have access to top people in a variety of scientific disciplines, and it is fairly easy to cross disciplines and work in other areas. The atmosphere is technically intense, but geared towards business problems and business opportunities. Work at the labs is expected to have a real impact on the business.

Although Bell Labs pays its people competitively, it does not consider itself a leader in pay, compared to the high wages offered at some of the more glamorous startup companies. Nevertheless, turnover is not a big problem, in part because most of the work is on the cutting edge of technology. Staff members have many opportunities to cross into different disciplines where they can work with other engineers and scientists who are leaders in their fields. Those who do leave have contributed their advanced communications and computing knowledge to the numerous high-technology companies started over the last few years.

In addition to its campus recruiting program, Bell Labs makes wide use of the media to attract new people. This method includes tapping into various trade magazines, campus publications, and World Wide Web sites. Lucent Technologies' URL is: *http://www.lucent. com.* For specific employment opportunities and job descriptions go to: *http://www.careermosaic.com/cm/lucent.*

Other Opportunities

Like Bell Labs, other business units of Lucent Technologies are experiencing an increase in demand for their products, and an expansion of the customer base. Jobs are available, and hiring is brisk. Dewayne Rideout, director of Human Resources Facilities at the Microelectronics Division says, "Like Bell Labs, we have a strong campus interest with a college presence and a moderate need for experienced people." The Microelectronics Division manufactures ICs for telecommunications and computing applications, with many of its digital signal processor chips going into digital cellular telephones. The division also is the world's largest supplier of power systems and optoelectronics, and a leading supplier to the wireless industry. The majority of the customer base is OEMs external to Lucent, but the division serves internal business units as well.

With its heavy emphasis on ICs, Microelectronics is looking for electrical engineers to design ICs. Since it has its own wafer fabs, it's looking for engineers with a process technology background. There also are positions open for those with a technical undergraduate or graduate degree, and an MBA or marketing background. People with computer science degrees also are in demand, because the division writes a considerable amount of software.

Recruiting is done through the trade media, the World Wide Web, and job fairs. The Internet is a favorite technique for recruitment since it puts candidates within easy reach of the company 24 hours a day, every day of the year.

Gene Heftman is a free-lance technical writer specializing in advanced electronics technology including ICs, computer systems and software.

How Valuable	Circle
Highly	569
Moderately	570
Slightly	571

ELECTRONIC DESIGN

DIRECT CONNECTION ADS

New Products/Services
Presented By The Manufacturer.
To Advertise,
Call Kimberly A. Stanger
At 201/393-6080

PROTO EXPRESS

MULTILAYER PROTOTYPES
FROM THE INDUSTRY AWARD WINNER

2 PIECE PRICES FOR FR4 .062 Th

LAYERS		1	2	3&4	5&6	7&8
SQUARE INCH UP TO	15	$233	$292	$639	$787	$935
	30	264	330	724	891	1059
	60	311	389	853	1049	1137
	90	358	448	980	1207	1434
	120	385	486	1044	1311	1559

■ 5 PIECES X 1.34 ■ 5 DAY PRICES ABOVE
■ 10 PIECES X 1.67 ■ UL LISTED

EXTRAS
- Photo Plotting
- Testing
- Gold Contacts - $50
- 25 - Below 8 Mil Hole - Below 15 Mil Hole
- SMBOC & LPI - $50

DISCOUNTS
10% ON ALL COD ORDERS
5% ON CREDIT CARD SALES
VISA & MASTERCARD

JUDGED BEST OVERALL 2 YEARS IN A ROW!

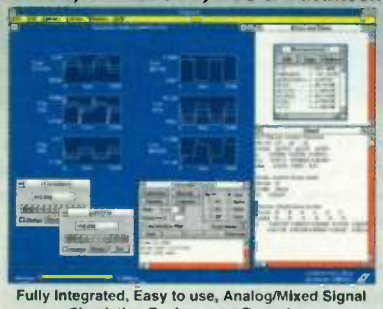
24 Hour Turn Around | Metal Core Boards
Mil P 55110-E | Gold Body Boards
Buried & Blind Vias | Up to 22 Layers
Polyimide Multilayer | Carbon Paste

CALL LAURA HOOK OR JOYCIE BAHL FOR QUOTES
(408)735-7137
FAX:(408)735-1408 MODEM:(408)735-9842
Internet/E-Mail:731-6799 @MCI MAIL.COM
http://www.sierraprotoexpress.com

CIRCLE 415

INTUSOFT

Analog Circuit Simulation
Windows, Windows NT, DOS & Macintosh



Fully Integrated, Easy to use, Analog/Mixed Signal Simulation Environment Featuring:
Integrated schematic entry, Extensive model libraries, the NEW Interactive IsSPICE4 simulator, and Real Time waveform graphics. Starting at $95 for IsSPICE 1.41 complete Windows and Macintosh systems are available for $2595.
Call Or Download For Your Free Demo and Information Kit!
www.intusoft.com P.O. Box 710 San Pedro
Tel. 310-833-0710 intusoft CA 90733-0710

CIRCLE 417

SIGNUM SYSTEMS

80C186
In-Circuit Emulators
80196 • 8051 • 80186 • Z8
DSP • HPC • 8085 • Z380

REAL TIME IN-CIRCUIT DEBUGGING & DEVELOPMENT
ON-THE-FLY ACCESS TO PROGRAM AND DATA MEMORY
REAL-TIME TRACE FILTERING
WINDOWS & MOUSE USER INTERFACE
FREE! 10-DAY TRIAL TRY BEFORE YOU BUY
FREE USER SUPPORT
EXTERNAL UNIT WITH NO PLUG-IN CARDS
OUTSTANDING PERFORMANCE AT A REALISTIC PRICE

SIGNUM SYSTEMS
FOR MORE INFO OR TO ARRANGE YOUR 10 DAY FREE TRIAL, CALL
1-800-838-8012

CIRCLE 420

MICROMINT

$29 Subminiature Control Computer

PicStics are low-cost industrial controllers that are pin-compatible with the Parallax BASIC Stamp I but offer enhanced capability, more instruction space, interrupts, two additional I/O lines, and still run fifteen times faster on the same program. PicStics can be programmed in compiled PBASIC, C, or PIC assembly language.
PicStic1 is a straight replacement for the BASIC Stamp I. PicStic2 adds a battery-backed, real-time clock/calendar. PicStic3 is a PicStic1 plus a 2-channel, 12-bit ADC.

PicStic™

- Small size: 0.6" × 1.4"
- Pin-compatible with Parallax BASIC Stamp I
- Low power: runs on 4.5 V to 18 V at less than 2 mA
- Uses 4 MHz PIC16C84 EEPROM processor
- Battery-backable, real-time clock/calendar (PicStic2)
- 2-channel, 12-bit, 0–5 V ADC (PicStic3)
- Ten bidirectional high-current I/O lines
- High-current onboard regulator
- Programmable in BASIC, C, and assembly language
- 300–9600 bps compiler-supported serial routines

BASIC Stamp® is a trademark of Parallax, Inc. PicStic™ is a trademark of Micromint, Inc.

MICROMINT, INC.
Tel: (860) 871-6170 Fax: (860) 872-2204
CALL 1-800-635-3355 TO ORDER!

CIRCLE 411

CACTUS LOGIC

In Circuit Emulators for

8051 | 68HC11 | Z80 | 6502 | Z180

- Over 50 Variants Supported
- Symbolic and source level debugging
- Supports all major compilers
- 30-day money-back guarantee
- Free single board computer with purchase
- Other processors available

Call 800-847-1998
Cactus LOGIC
14120 East Live Oak Ave. Suite A2
Baldwin Park, CA 91706
Telephone: (818) 337-4547
FAX: (818) 337-0689

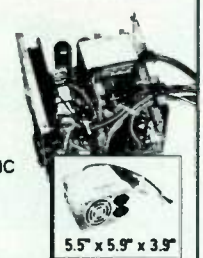
CIRCLE 402

ICP ACQUIRE, INC.

Industrial PC Power Supply

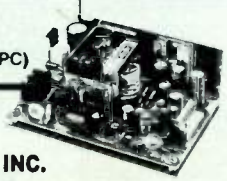
85~265VAC, -48VDC, +24VDC, +12VDC input

- 70W~350W output
- 60KHz PWM control IC
- 0~55°C operating
- MTBF > 20 years



5.5" x 5.9" x 3.9"

3" x 5" (designed for LCD/EL panel PC)



ICP ACQUIRE INC.
CALL: 1-888-168-1688
FAX: 415-428-1172

CIRCLE 405

JK MICROSYSTEMS

Flashlite™

Single Board Computer with DOS and Utilities $195

- 8 Mhz V-25 + Processor
- 512 KB RAM
- 256 KB Flash
- 2 Serial Ports

Ideal for embedded controller applications:
2 fast DMA channels • 8 analog inputs with programmable comparator levels • priority interrupt controller with vector or register bank switching.

Simple and quick software development:
Create on a PC compatible computer • download in .EXE or .COM format to flash disk • test and debug through the console serial port • modify the startup batch file to load and execute the application on reset or powerup.

JK microsystems
1275 Yuba Ave., San Pablo, CA 94806 • 510 236-1151
fax 510 236-2999 http://www.dsp.com/jkmicro

CIRCLE 419

REPEAT IT! REPEAT IT!

REPEAT IT!

You've developed a strong image for your market and you'd like to advertise your message in the industry's strongest publication. The recent Adams Study found that *Electronic Design* has the largest average issue audience among the industry's twenty leading publications-and *Electronic Design* was found to be the leading publication for technical information among design engineers.

Now's the time to project your image and reach the strongest specifying/buyer audience in the industry 165,000 strong. That's 165,000 opportunities for qualified leads. If you repeat your ad every issue (26 times), you can have 4,290,000 opportunities all qualified.

For more information, call Kimberly Stanger advertising representative at 201/393-6080 Fax: 201/393-0204

ELECTRONIC DESIGN

1997 CALENDAR

Issue Date	Closing
January 20	12/11/96
February 3	12/24/96
February 17	1/7/97
March 3	1/22/97
March 17	2/5/97
April 1	2/20/97
April 14	3/5/97
May 1	3/21/97
May 12	4/2/97
May 27	4/17/97
June 9	4/30/97
June 23	5/14/96
July 7	5/29/97
July 21	6/11/97
August 4	6/25/97
August 18	7/9/27
September 2	7/24/97
September 15	8/6/97
October 1	8/22/97
October 13	9/3/97
October 23	9/12/97
November 3	9/24/97
November 17	10/8/97
December 1	10/22/97
December 15	11/5/97

ELECTRONIC DESIGN ENGINEERING CAREERS

RATES. $171 PER COLUMN INCH, COMMISSIONABLE TO AGENCIES

DEADLINES

Space reservation: 5th of month preceding issue date
Ad material to: Penton Publishing, Classifieds Dept.
Attn.: Jon Eggleton, 1100 Superior Ave., Cleveland, OH 44114

SALES STAFF

Recruitment Sales Rep.: Jon Eggleton
(800) 659-1710, (216) 931-9832
FAX: (216) 696-8206

RECRUITMENT

CAREER OPPORTUNITIES NATIONWIDE

Engineers • Mngrs □ Tech Specialists
Software (C,C++, Unix, et als) LAN/WAN • CAD/CAE •ASIC•DSP•ATM•Embedded Systems•Analog/ Mixed Signals•RF•Satellite•Digital IC's•CATV• Wireless•Networks•Many Others Resume to: Peter Ansara, c/o ABF, PO Box 239, W. Spfld, MA 01090 Fax (413) 731-1486 Tel (413) 733-0791. Web site: http:// www.ansara.com E-mail: pa@ansara.com

For further information on placing an ad in **ELECTRONIC DESIGN** please contact ***Jon Eggleton*** at (216) 931-9832 or fax at (216) 696 - 8206

PROFESSIONAL SERVICES

DESIGN TEAM FOR HIRE
- ELECTRONIC DESIGN
- PRODUCT DEVELOPMENT
- TESTING & EVALUATION
- IN-HOUSE CAD & CAE
- COST REDUCTION FOR MASS MARKET
- ANALOG, AUDIO, & TELECOM

EFFECTIVE SOLUTIONS
908 493 9555 • FAX 908 493 9633
http://www.Effectivesol.com

a penton publication

CAREER OPPORTUNITIES

In Electronic Engineering

A special quarterly career insert in the February, May, August and November issues of

Microwaves & RF

WIRELESS SYSTEMS DESIGN

ELECTRONIC DESIGN

Reach 173,000 Electronic Engineers
Customized Editorial Environment
Bonus Distribution at Shows
To reserve space in the next available issue:
call Jon Eggleton at (216) 931-9832
or fax at (216) 696-8206

ELECTRONIC DESIGN

Chairman and CEO: Thomas L. Kemp
President and COO: Daniel J. Ramella
Chairman Emeritus: Sal F. Marino

Group President: James D. Atherton

Vice President Ancillary Product & Sales: Drew DeSarle

Publisher: John French
Hasbrouck Heights, NJ; (201) 393-6060
National Sales Manager: Russ Gerches
Hasbrouck Heights, NJ; (201) 393-6045
Director Of Marketing: WalkerJohnson
San Jose, CA (408) 441-0550, FAX: (408) 441-6052
Production Manager: Eileen Slavinsky
Hasbrouck Heights, NJ; (201) 393-6093
Marketing Research Administrator: Deborah Eng.
Hasbrouck Heights. NJ; (201) 393-6063

Advertising Sales Staff

Hasbrouck Heights: Judith L. Miller
Sales Asst.: Judy Stone Hernandez
611 Route #46 West, Hasbrouck Heights, NJ 07604;
Phone: (201) 393-6060TWX: 710-990-5071
Boston & Eastern Canada: Ric Wasley
Sales Support: Karen Harrison
60 Hickory Drive, Waltham, MA 02154;
Phone: (617) 890-0891FAX: (617) 890-6131
North California/Colorado: Chuck Signor (408) 441-0550
Chicago/Midwest: Lisa Zurick
Sales Assistant: Dawn Heili
180 N. Stetson Ave., Suite 2555 Chicago, IL 60601;
(312) 861-0880 FAX: (312) 861-0874
North California/Utah/N.Mexico/Arizona:
James Theriault (408) 441-0550
Los Angeles/Orange County/San Diego: Ian Hill
Sales Asst: Patti Kelly 16255 Ventura Blvd.,
Suite 200 Encino, CA 91436;
(818) 990-9000 FAX: (818) 905-1206
San Jose:
Jeff Hoopes, Chuck Signor, James Theriault
Sales Support: Liz Torres & Rachel Ross 2025 Gateway Pl.,
Suite 354 San Jose, CA 95110;
(408) 441-0550 FAX: (408) 441-6052 or (408) 441-7336
Pacific N.W. & Western Canada:
Jeff Hoopes (408) 441-0550
Texas/Southeast: Bill Yarborough
1557 Bracher St. Houston, TX 77055;
Phone: 713-984-7625. FAX: 713-984-7576
Direct Connection Ads & Direct Action Cards:
Kim Stanger (201) 393-6080

General Manager, European Operations: John Allen
36 The Green, South Bar Banbury. Oxford OX 16 9AE, U.K.
Phone: 44 (0)-1- 295-271003 FAX: 44 (0)-1- 295-272801
Netherlands, Belgium: Peter Sanders,
S.I.P.A.S. Rechtestraat 58 1483 Be De Ryp,
Holland Phone: 011-31-299-671303 Fax: 011-31-299 671500
France: Fabio Lancellotti
Defense & Communication
10 Rue St. Jean 75017 Paris France
Phone: 33-142940244. FAX: 33-143872729
Spain/Portugal: Miguel Esteban
Publicidad Internacional Pza.
Descubridor Diego de Ordas,
1 Escalera, 2 Planta 2D 28003 Madrid, Spain
Phone: 91/4416266 FAX: 91/4416549
Scandinavia: Paul Barrett
I.M.P. Hartswood, Hallmark House.
25 Downham Road, Ramsden Heath,
Billiricay, Essex, CM 11 1PV, UK.
Phone:44(0)-1-268-711560, Fax:44(0)-1-268-711567
Germany, Austria, Switzerland: Friedrich Anacker
InterMedia Partners GmbH Deutscher Ring 40
42327 Wuppertal, Germany
Phone: 49 202 711 091 Fax: 49 202 712 431
Hong Kong: Kenson Tse
IDG International Marketing Services
Suite 25F, One Capital Place,18 Luard Road,Wanchai, Hong Kong
Tel: 852-2527-9338. Fax: 852-2529-9956
Israel: Igal Elan, Elan Marketing Group
22 Daphna St., Tel Aviv, Israrl
Phone:972-3-6952967 FAX: 972-3-268020
Toll Free in Israel only: 177-022-1331
Japan: Hirokazu Morita,
Japan Advertising Communications
Three Star Building 3-10-3-Kanda Jimbocho
Chiyoda-Ku, Tokyo 101, Japan
Phone: 3 3261 4591. FAX:3 3261 6126
Korea: Young Sang Jo,
Business Communications Inc.
K.P.O. Box 1916, Midopa Building 146
Dangiu-Dong, Chongo-Ku, Seoul, Korea
Phone: 011-82-2-739-7840 FAX: 011-82-2-732-3662
Taiwan: Charles Liu, President,
Two-way Communications, Co., Ltd.
12F/1, No.99, Sec.2
Tun-Hwa South Road, Taipei, Taiwan.
Phone: 011-886-2-707-5828;FAX: 011-886-2-707-5825
United Kingdom: John Maycock
John Maycock Associates
Redlands, Tapton House Road
Sheffield, England S 10 5BY

INDEX OF ADVERTISERS

Domestic*
International **

THE WORLD'S LARGEST SELECTION

POWER SPLITTERS/ COMBINERS

2kHz-10GHz *from* $2.95

Choose from over 480 standard off-the-shelf models from 2-way to 48-way; 0°, 90° and 180°; 50 and 75 ohms; covering 2kHz to 10GHz. Mini-Circuits will also supply your special needs such as wider bandwidths, higher isolation, lower insertion loss, and phase matched ports...all at catalog prices with rapid turnaround time. Models include surface mount, plug-in, flat-pack and standard connectorized designs such as SMA, N, TNC, C, and F connectors as well as custom designs. Ultra-miniature surface mount units provide excellent solutions in cellular communications, cable systems and countless wireless applications. All units come with a 1year guarantee and "skinny" 4.5 sigma repeatability unit-to-unit and production run to production run. Catalog models are guaranteed to ship within one week.

Mini-Circuits...we're redefining what VALUE is all about!

Mini-Circuits®

P.O Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500 Fax (718)332-4661 *INTERNET* http://www. minicircuits. com

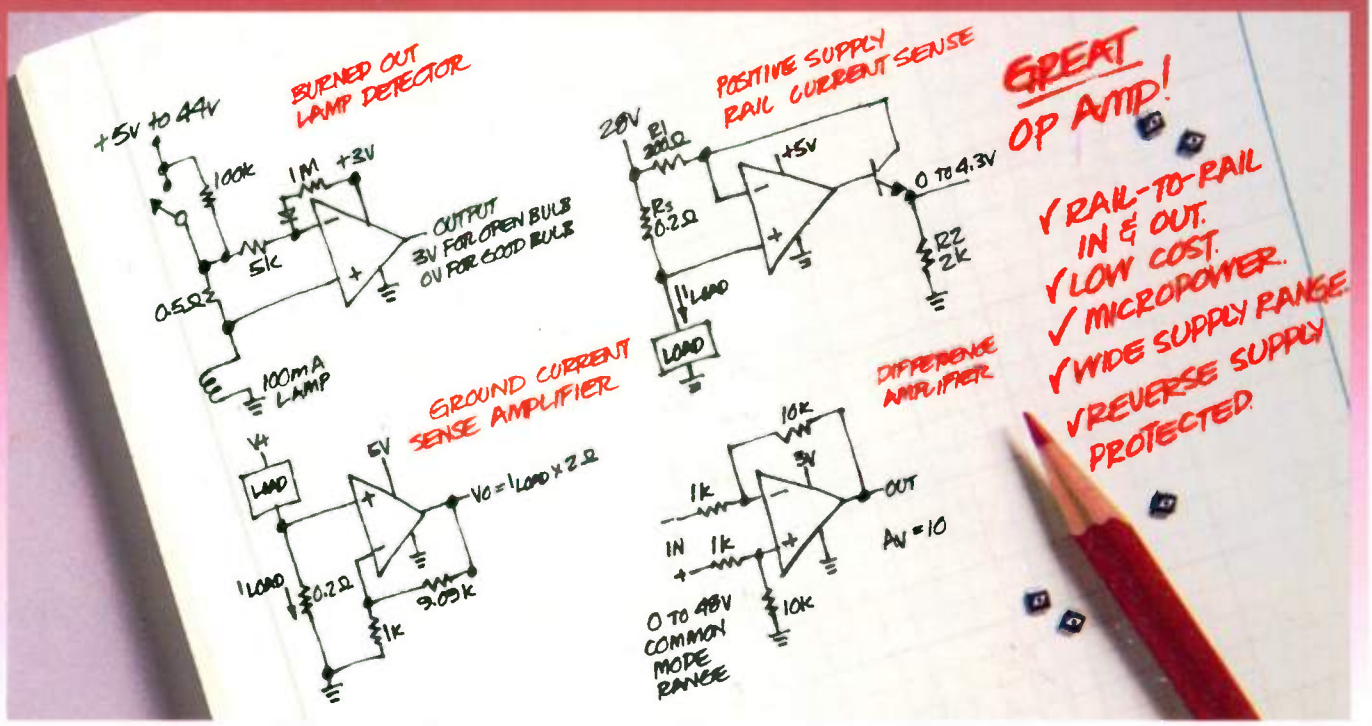
US 130 INT'L 131
CIRCLE READER SERVICE CARD

For detailed specs on all Mini-Circuits products refer to • 740- pg. HANDBOOK • INTERNET • THOMAS REGISTER • MICROWAVE PRODUCT DATA DIRECTORY • EEM

CUSTOM PRODUCT NEEDS...Let Our Experience Work For You.

F 202 Rev Orig

First Universal Micropower Rail-to-Rail Op Amp!



The LT1490: First dual op amp in the tiny MSOP package.

Actual Size

Linear Technology's LT1490 dual op amp is the first of a new generation of rail-to-rail input and rail-to-rail output general purpose op amps. The LT1490 operates from ±1.25 up to 44V and provides exceptional ruggedness to abnormal voltages.

LT1490 is a true rail-to-rail op amp — both its input and output operate to either rail. The output swings to within 25mV of either supply at light loads and to within 330mV even while driving 10mA. The inputs actually operate at voltages above the positive power supply. Input specifications and CMRR are guaranteed up to 44V even if the power supply is only 2.5V.

The LT1490 is one tough op amp— it is designed to handle abnormal voltages which would destroy most other op amps. It is internally protected for up to 18V of reverse power supply voltage, eliminating diodes normally required to protect against improperly connected batteries.

LT1490 OP AMP FEATURES

- ✓ Rail-to-Rail In and Out
- ✓ Supply Voltage: 2.5- 44V
- ✓ 40µA I_Q/Op Amp
- ✓ Reverse Supply Protected
- ✓ 20mA/5000pF Output Drive
- ✓ 220µV Input Offset Voltage
- ✓ 4nA Input Bias Current

The inputs can withstand voltages 44V above the negative rail to 22V below the negative rail without damage. In industrial environments where the input signals may appear before power-up, or where supplies may be improperly sequenced or reversed, the LT1490 ensures reliable operation.

Unlike many rail-to-rail op amps, the LT1490 does not give up operating supply voltage (2.5-44V), output drive (±20mA) or input error (220µV) to achieve reliability or ease of use.

The LT1490 is the new first choice in micropower op amps and it's the first dual op amp in the tiny MSOP package. It also comes in 8-lead PDIP and SO packages. Prices start at $1.95 in 1000-piece quantities. A 14-lead quad version, the LT1491, is also available. Good things *do* come in small packages. Contact Linear Technology Corporation, 1630 McCarthy Blvd., Milpitas, CA 95035-7417. 408-432-1900. Fax: 408-434-0507. For literature only, call **1-800-4-LINEAR**. www.linear-tech.com

LT, LTC and LT are registered trademarks of Linear Technology Corporation.

LINEAR TECHNOLOGY

FROM YOUR MIND TO YOUR MARKET
AND EVERYTHING IN BETWEEN

www.linear-tech.com

READER SERVICE 210