ELECTRONIC DESIGN

FOR ENGINEERS AND ENGINEERING MANAGERS-WORLDWIDE

A PENTON PUBLICATION $10.00

FEBRUARY 3, 1997

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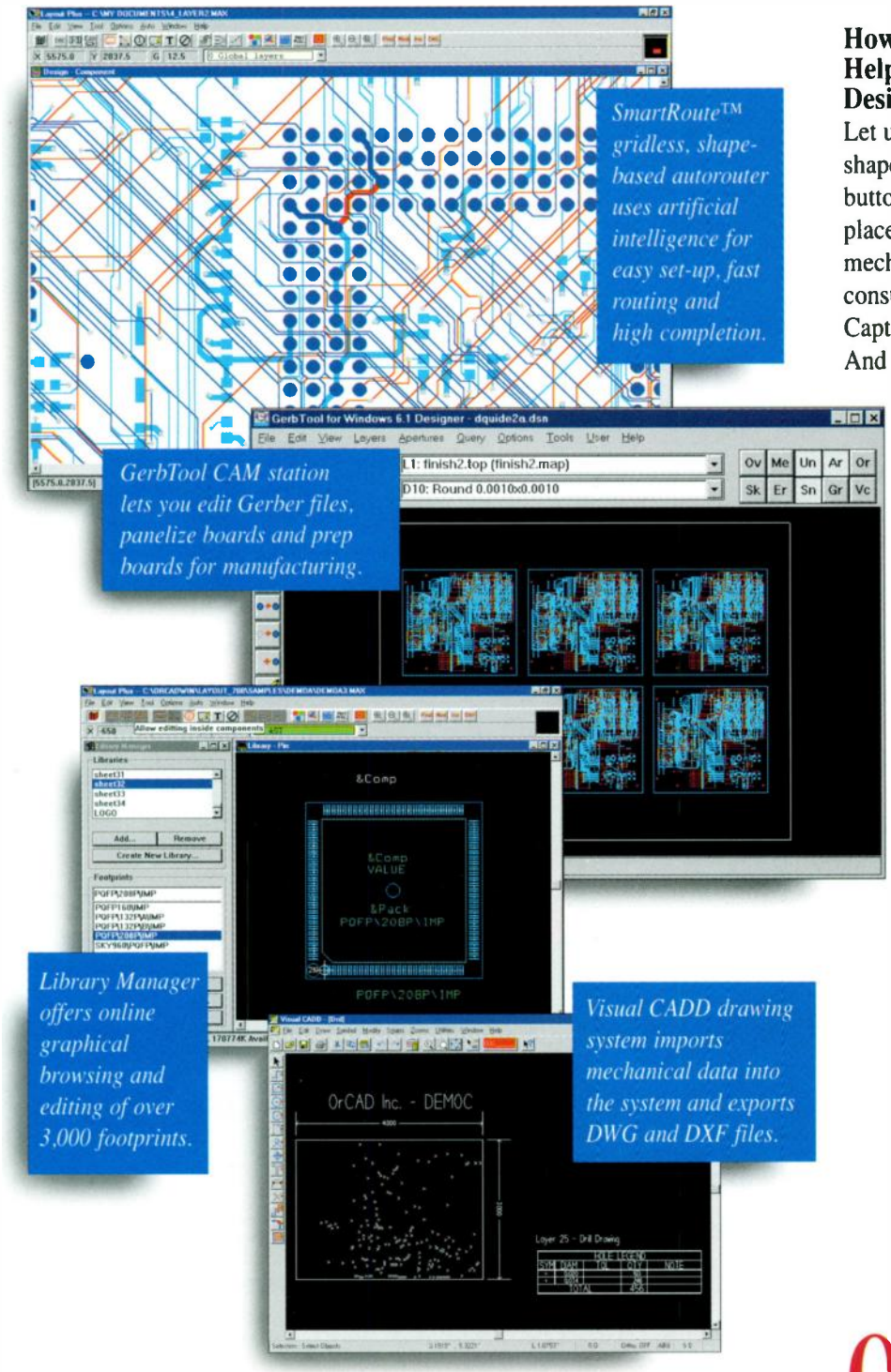

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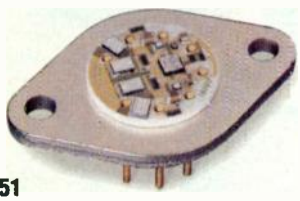

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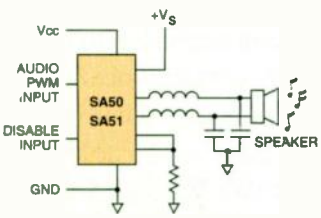

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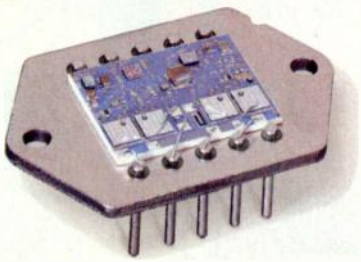

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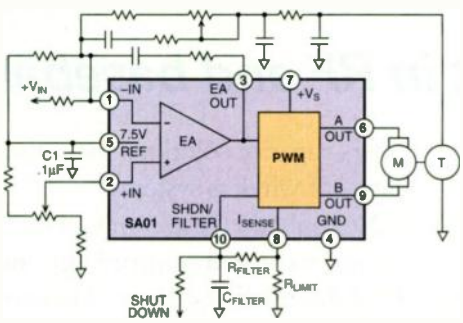

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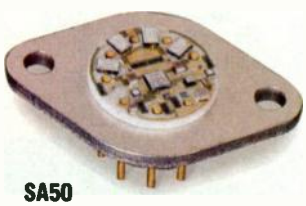

SA50

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- 97% efficient
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- 5A output continuous
- Internal PWM generation
- Full bridge output operation
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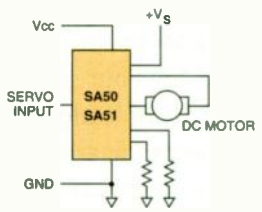

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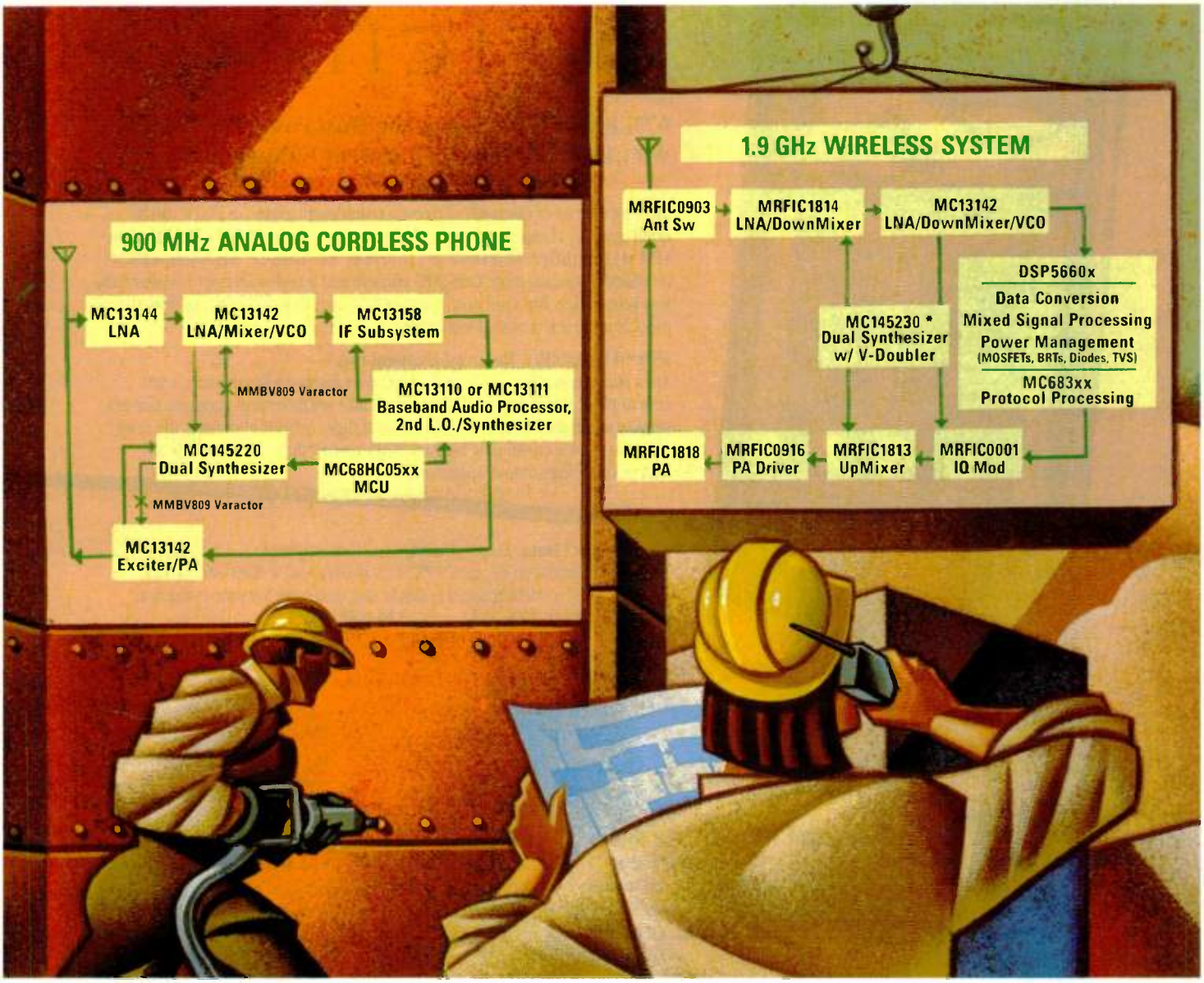

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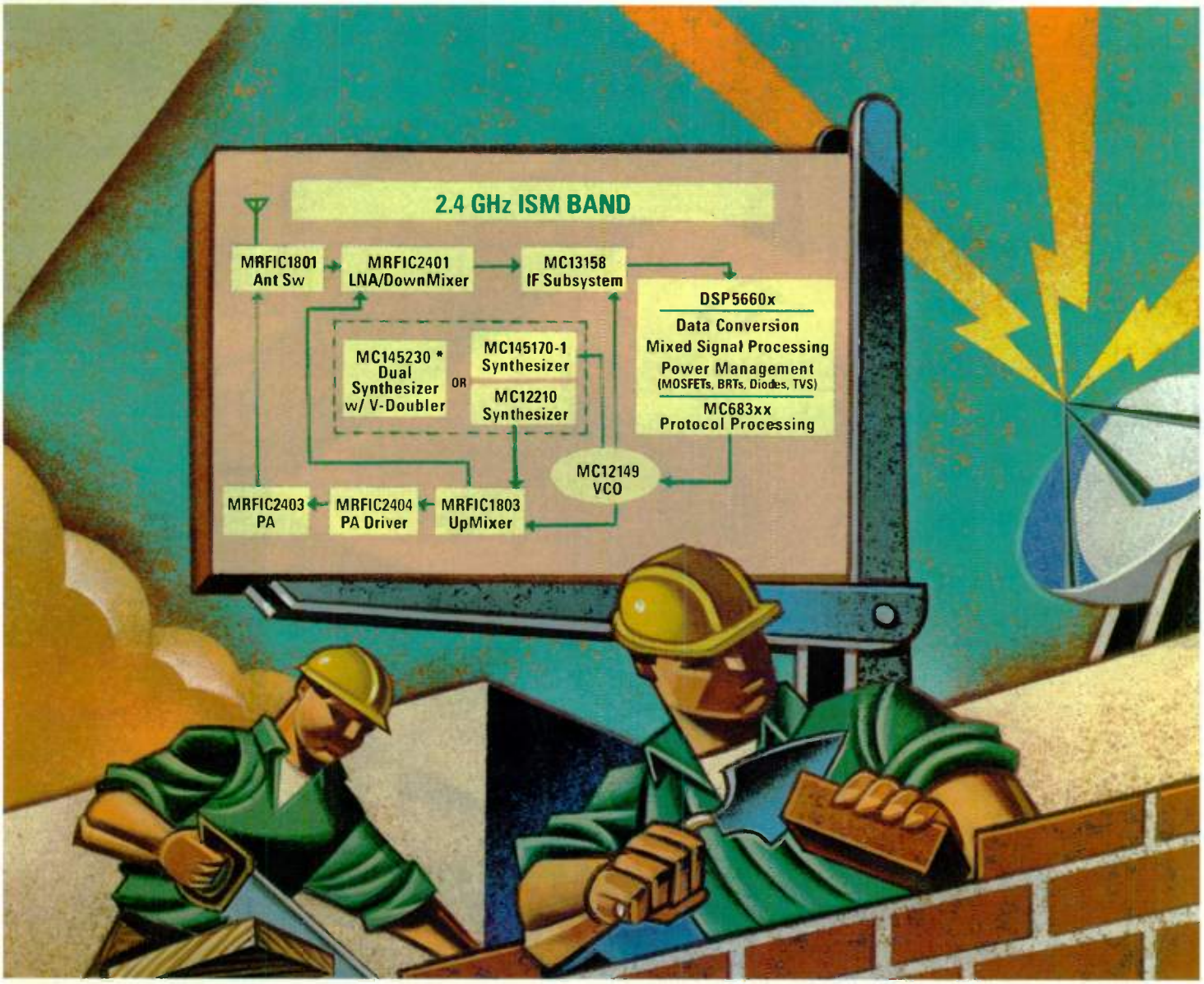

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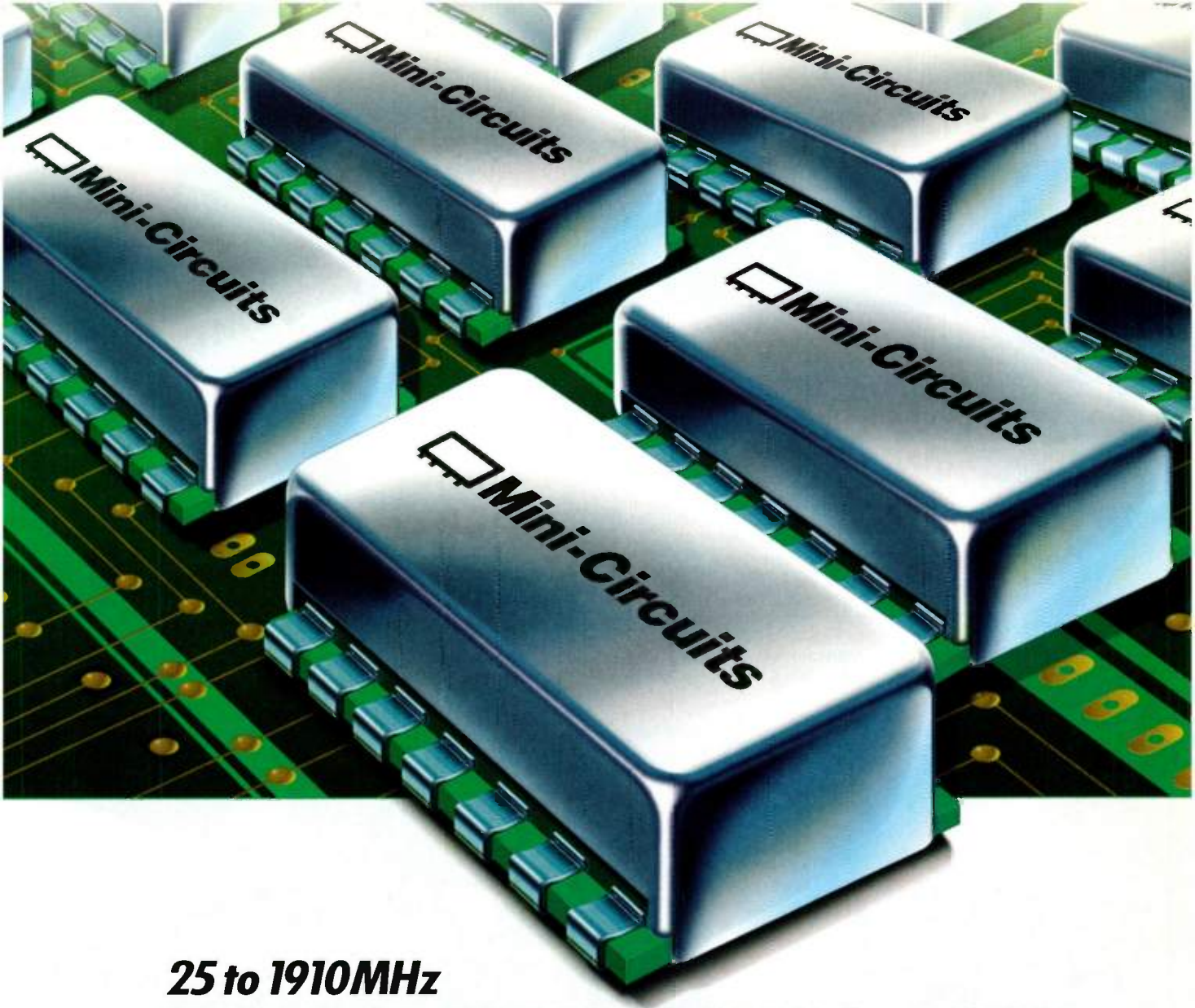

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JTOS-75	37.5-75	-110	-27	16V	20	13.95
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JTOS-150	75-150	-106	-23	16V	20	13.95
JTOS-200	100-200	-105	-25	16V	20	13.95
JTOS-300	150-280	-102	-28	16V	20	15.95
JTOS-400	200-380	-102	-25	16V	20	15.95
JTOS-535	300-525	-97	-28		20	15.95
JTOS-765	485-765	-98	-30	16V	20	16.95
JTOS-1025	685-1025	-94	-28	16V	22	18.95
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ELECTRONIC DESIGN

February 3, 1997 Volume 45, Number 3

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TECH INSIGHTS

COVER FEATURE

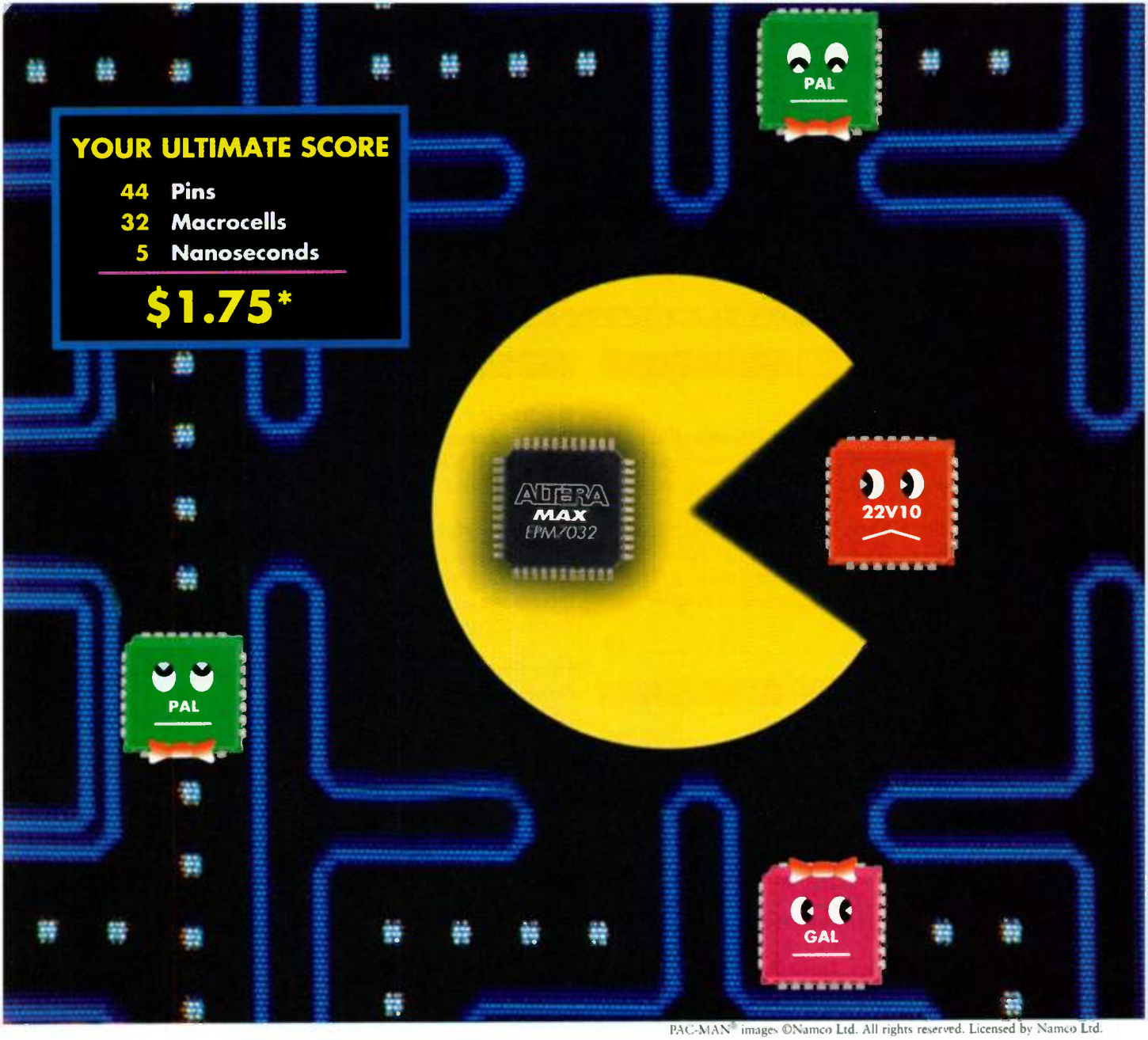
DSP

COMMUNICATIONS TECHNOLOGY

COMMUNICATIONS TECHNOLOGY

PIPS

ELECTRONIC DESIGN (USPS 172-080; ISSN 0013-4872) is published twice monthly except for 3 issues in May and 3 issues in October by Penton Publishing Inc., 1100 Superior Ave., Cleveland, OH 44114-2543. Paid rates for a one year subscription are as follows: $105 U.S., $185 Canada, $210, $255 International. Second-class postage paid at Cleveland, OH, and additional mailing offices. Editorial and advertising addresses: ELECTRONIC DESIGN, 611 Route #46 West, Hasbrouck Heights, NJ 07604. Telephone (201) 393-6060. Facsimile (201) 393-0204. Printed in U.S.A. Title registered in U.S. Patent Office.



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*100K unit price projection for the EPM7032LC-44-10.

ELECTRONIC DESIGN

February 3, 1997 Volume 45, Number 3

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PIPS

BOARDS & BUSES

QUICK LOOK

DEPARTMENTS

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Jesse H. Neal Editorial Achievement

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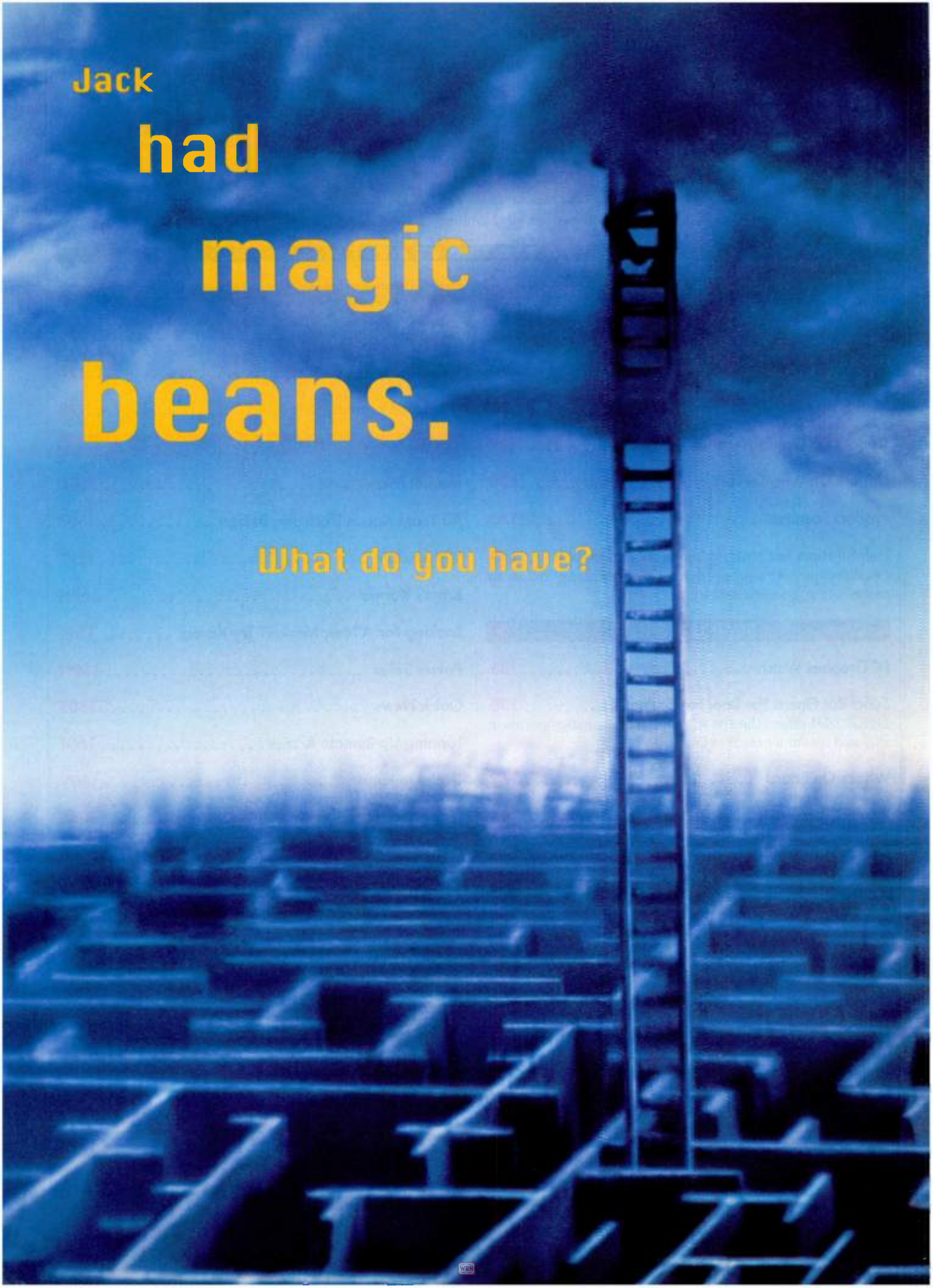
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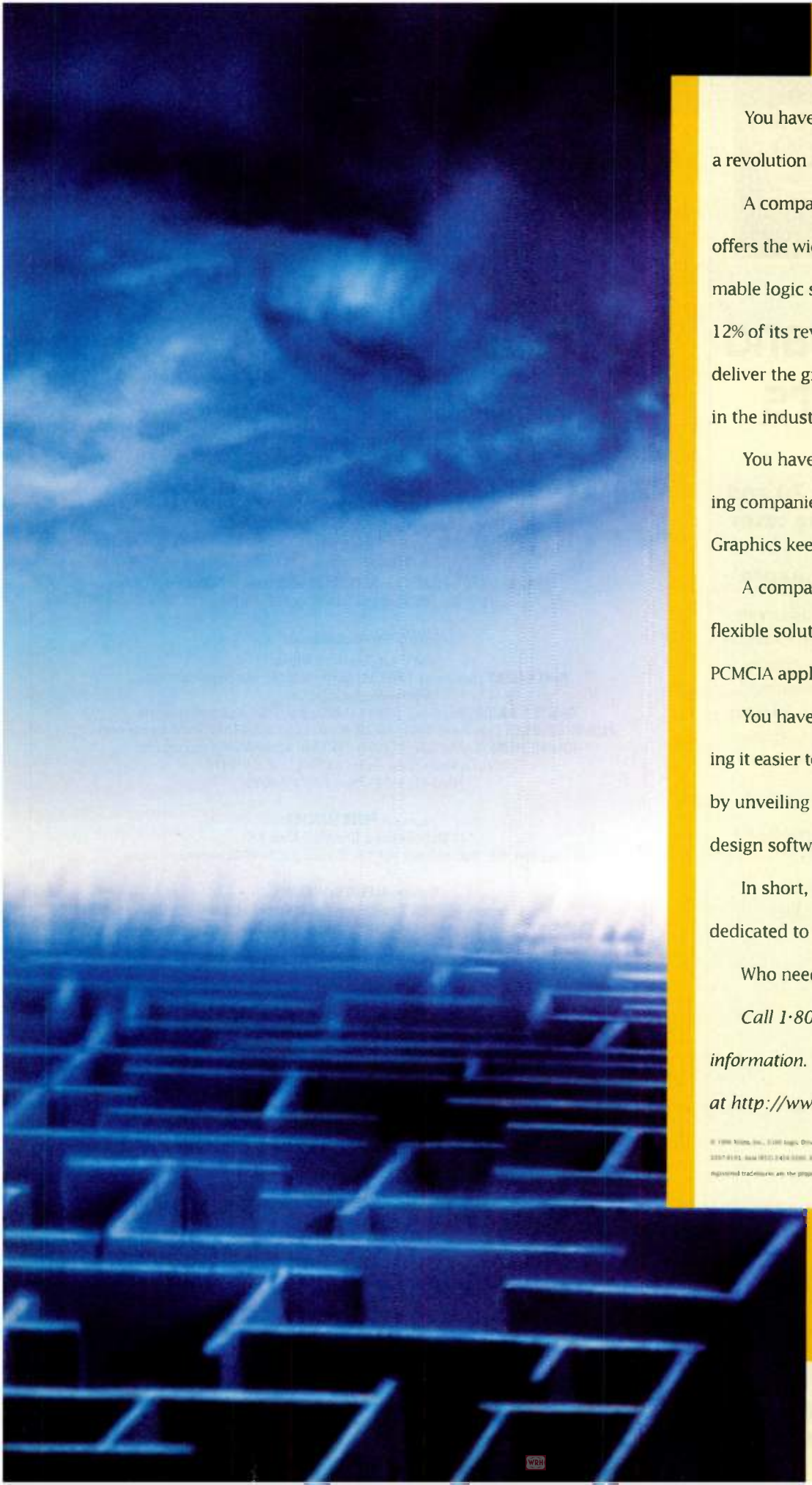

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Published by Penton Publishing

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Third Conference on Business Opportunities & Operational Requirements for Utilities in Telecommunications (Utilicom '97), Feb. 19-21. Washington Vista Hotel, Washington, DC. Contact (800) 822-6338 or (202) 842-3022 ext. 317; http://www.brp.com.

Second International Conference on Chip-Scale Packaging, Feb. 20-21. Sunnyvale Hilton Inn, Sunnyvale, CA. Contact Subash Khadpe; (610) 799-0419; fax (610) 799-0519; e-mail: skhadpe@semitech.com.

IEEE Applied Power Electronics Conference and Exposition (APEC 97), Feb. 23-27. Westin Peachtree Plaza Hotel, Atlanta, GA. Contact Pam Wagner, Courtesy Associates, 655 15th St., N.W., Suite 300, Washington, DC 20005; (202) 347-5900; fax (202) 347-6109.

MARCH 1997

Computer Telephony Expo '97, Mar. 4-6. Los Angeles Convention Center, Los Angeles, CA. Contact (212) 691-8215.

IPC Printed Circuits Expo 97 & 40th Annual Meeting, March 9-13. San Jose Convention Center, San Jose, California. Contact JoAnn Galluzzi (847) 509-9700; Internet: http://www.ipc.org.

Embedded Systems Conference East, Mar. 10-12. Hynes Convention Center, Boston, Massachusetts. Contact (617) 821-9222; e-mail: esce@exporeg.com.

PCB Design Conference West, Mar. 15-21. Santa Clara Convention Center, Santa Clara, CA. Contact PCB Design Conference, P.O. Box 472, Canton, Massachusetts 02021; (617) 828-9185; fax (617) 828-8198.

European Design & Test Conference (ED&TC '97), Mar. 17-20. CNIT Conference & Exhibition Centre, Paris-La Defense, France. Contact ED&TC Conference Secretariat, CEP Consultants Ltd., 43 Manor Pl., Edinburgh, EH3 7EB, UK; (44) 131-300 3300; fax (44) 131-300 3400; e-mail: edtc@cep.u-net.com.

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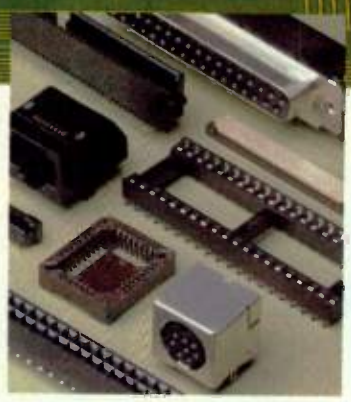

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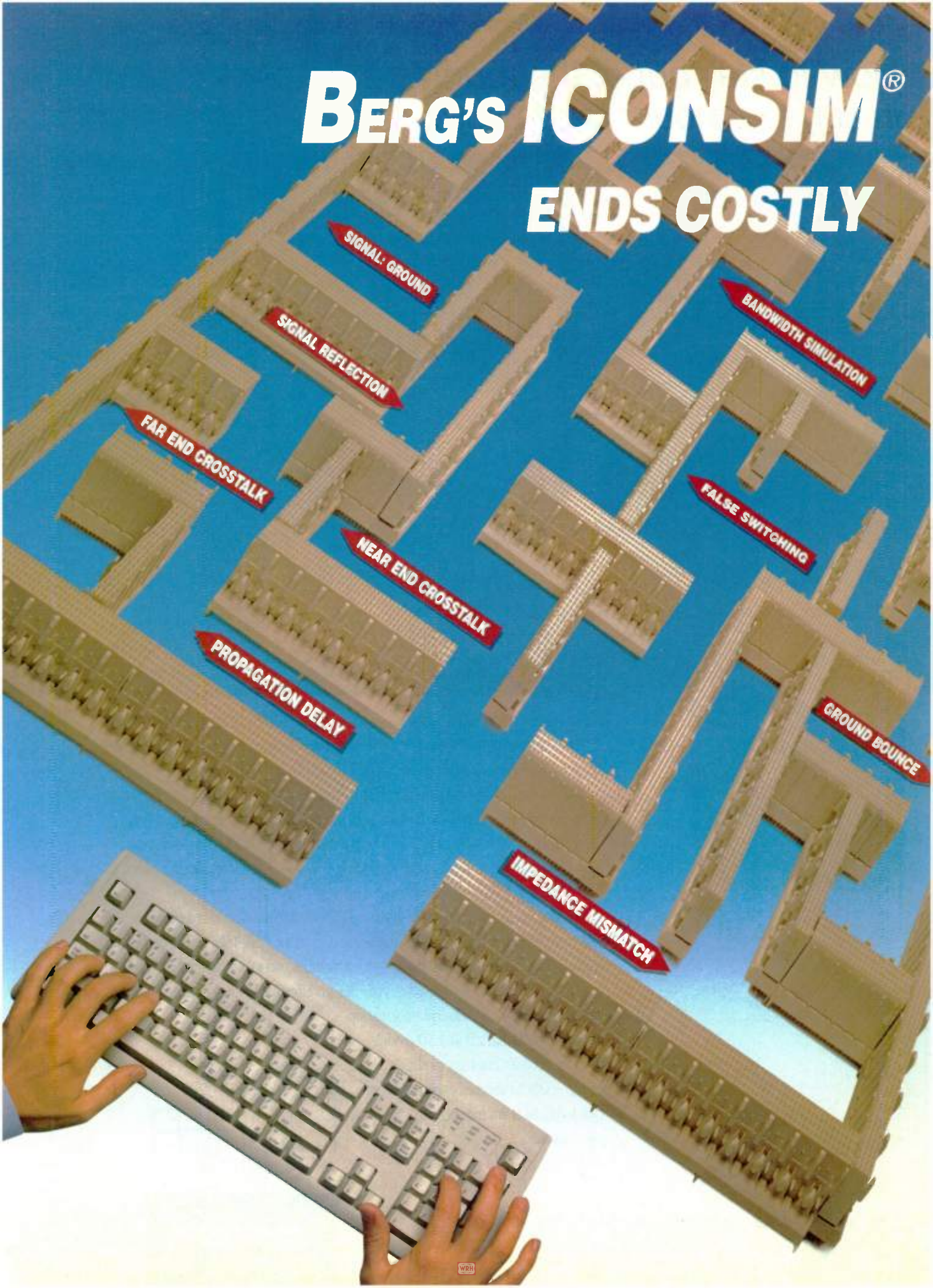
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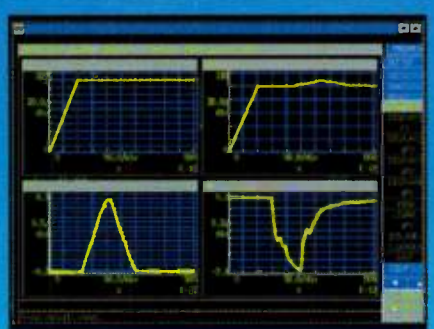
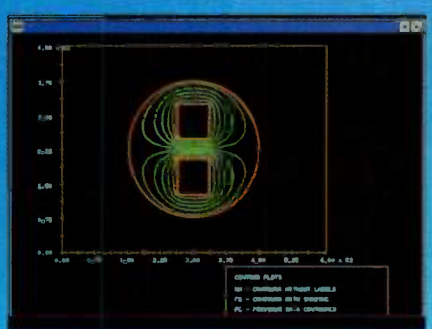


Crosstalk Characteristic Impedance



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MARCH

Antennas: Principles, Design, and Measurements (Short Course), Mar. 18-21. Mission Bay, San Diego, CA. Contact Kelly Brown, NCEE, 1101 Massachusetts Ave., St. Cloud, FL 34769; (407) 892-6146; fax (407) 892-0406.

Communication Design Engineering Conference, Mar. 24-26. Washington, DC. Convention Center, Washington, DC. Contact Denise Chan, Miller-Freeman Inc., (415) 278-5231.

Portable By Design Conference and Exhibition, Mar. 24-27. Santa Clara Convention Center, Santa Clara, CA. Contact Betsy Tapp, (201) 393-6075; fax (201) 393-6073; e-mail: portable@class.org.

Communication Design Engineering Conference, Mar. 25-27. Washington Convention Center, Washington, DC. Contact (617) 821-9219; e-mail: cdec@exporeg.com.

DSP World Spring Design Conference, Mar. 25-27. Washington Convention Center, Washington, DC. Contact Denise Chan, Miller Freeman Inc., (415) 278-5231; e-mail: dsp@exoreg,com.

SOUTHCON '97, Mar. 25-27. Raleigh Civic and Convention Center, Raleigh, NC. Contact Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045; (800) 877-2668 ext. 243; fax (310) 641-5117; e-mail: southcon@ieee.word.org.

Second Conference on The New Integrated Service Provider (Supercarrier '97), Mar. 26-28. Washington Vista Hotel, Washington, DC. Contact (800) 822-6338 or (202) 842-3022 ext. 317; Internet: http://www.brp.com.

Sixth International Verilog Conference, Mar. 31-Apr. 2. Santa Clara Convention Center, Santa Clara, CA. Contact MP Associates, 5305 Spine Rd., Suite A, Boulder, CO 80301; (303) 530-4562; fax (303) 530-4334; e-mail: ivcinfo@ivcconf.com.

APRIL

INTERMAG '97, Apr. 1-4. Hyatt Regency Hotel, New Orleans, LA. Contact John Nyenhuis, School of Electrical Engineering, Purdue University, West Lafayette, IN 47907-1285; (317) 494-3524; fax (317) 494-2706; e-mail: nyenhuis@ecn.purdue.edu.

Surface-Mount Technology Association, April 2. Gwinnett County Civic Center, Atlanta Georgia. Contact (770) 569-1822; e-mail: smta-info@t-tech.com; Internet: http://www.smta.org.

IEEE International Reliability Physics Symposium, April 7-10. Adams Mark Hotel, Denver, CO. Contact IRPS Publishing Services, P.O. Box 308, Westmoreland, NY 13490; (315) 339-3971; fax (315) 336-9134; e-mail: 103227.2074@compuserve.com.

IEEE Conference on Computer Communications (INFOCOM 97), Apil 7-11. Kobe, Japan. Contact Tatsuya Suda, Dept. of Information & Computer Science, University of California, Irvine, California 92717-3425; (714) 856-5474; fax (714) 856-4056; e-mail: suda@ics.uci.edu; Internet: http://www.ics.uci.edu/infocom/ (North America); http://arpeggio.ics.es.osaka-u.ac.jp/infocom.html (Japan).

Fourth ASAT Conference , April 14-16. San Francisco Airport Marriott, San Francisco, California. Contact Suzanne Graf, Project Manager, (541) 984-5204; fax (541) 343-7024; e-mail: SGraf@Advanstar-Expos.com.

IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP 97), April 21-24. Gasteig Cultural and Convention Center, Munich, Germany. Contact Bernd Girod, Lehrst.f.Nachrichtentechnik, Univ. of Erlangen Nuremberg, Cauerstr. 7, D-91058 Erlangen, Germany; (49) 91-3185-7101; fax (49) 91-3131-30840; e-mail: b.girod@ieee.org.

Sixth System Administration, Networking, & Security Conference, April 21-26. Baltimore Inner Harbor, Maryland. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, California 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

IEEE International Conference on Robotics and Automation, Apr. 21-27. Albuquerque Convention Center, Albuquerque, NM. Contact Jerry Stauffer, Intelligent Systems and Robotics Center, Program Office, MS0949, Sandia National Laboratories, Albuquerque, NM 87185-0949; (505) 845-8966; fax (505) 844-6161; e-mail: jdstauf@isrc.sandia.gov.

First Convergence Technology & IC Expo, Apr. 22-24. InfoMart, Dallas, TX. Contact Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045; (800) 877-2668, ext. 243; fax (310) 641-5117.

15th IEEE VLSI Test Symposium, Apr. 27-30. Hyatt Regency Monterey, Monterey, CA. Contact Y. Zorian; (408) 543-0146 ext. 227, e-mail: zorian@lvision.com.

MAY

IEEE Vehicular Technology Conference (VTC), May 5-7. Hyatt Regency at Civic Plaza, Phoenix, AZ. Contact Wendy Rochelle, IEEE Conference Services, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331; (908) 562-3870; fax (908) 981-1769; e-mail: w.rochelle@ieee.org.

International Test Synthesis Workshop, May 5-7. Santa Barbara, CA. Contact K. Wagner; (415) 694-4386; e-mail: kwagner@symopsys.com.

IEEE Custom Integrated Circuits Conference (CICC '97), May 5-8. Santa Clara, CA. Contact Melissa Widerkehr, Widerkehr & Assoc., Suite 270, 101 Lakeforest Blvd, Gaithersburg, MD 20877; (301) 527-0902; fax (301) 527-0994.

Electronics Industries Forum of New England, May 5-9. World Trade Center, Boston, MA. Contact Summit Exhibition Management Inc., Norwalk CT; (800) 322-9332; (203) 855-3000; fax (203) 855-3003.

IEEE Power Industry Computer Applications Conference (PICA), May 11-16. Contact T.C. Wong, American Electric Power, 1 Riverside Plaza, Columbus, OH 43215; (614) 223-2235; fax (614) 223-2205; e-mail: t.wong@ieee.org.

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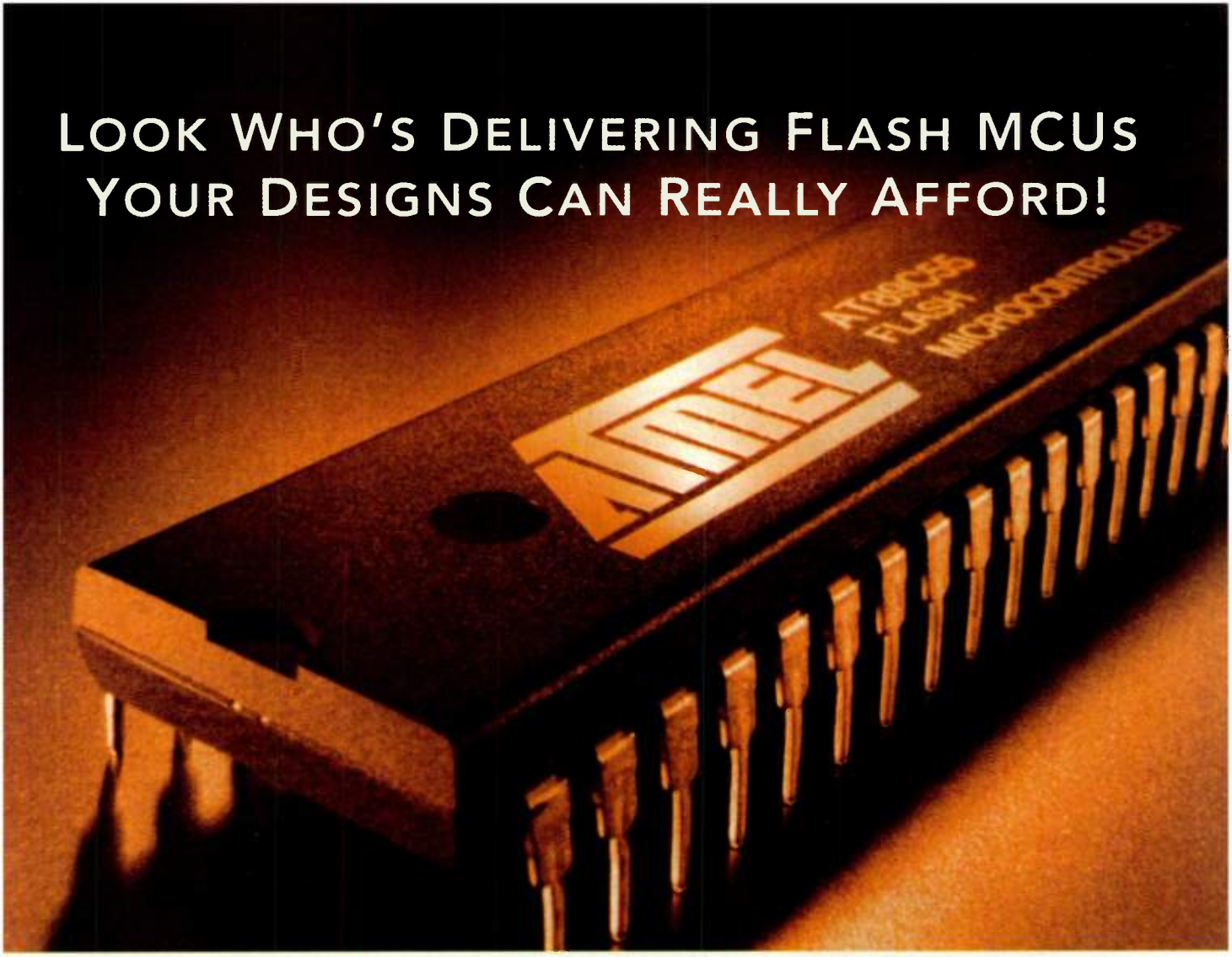

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S53	12K	256	No	Yes	Yes	2.7–6.0	0–24	3	40
C55	20K	256	No	No	Yes	2.7–6.0	0–33	3	40
C52	8K	256	No	No	Yes	4.0–6.0	0–24	3	40
LV52	8K	256	No	No	Yes	2.7–6.0	0–12	3	40
C51	4K	128	No	No	Yes	4.0–6.0	0–24	2	40
LV51	4K	128	No	No	Yes	2.7–6.0	0–12	2	40
C2051	2K	128	No	No	Yes	2.7–6.0	0–24	2	20
C1051	1K	64	No	No	No	2.7–6.0	0–24	1	20

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READER SERVICE 103

EDITORIAL

The Software Side Of Engineering

The news for engineers in recent years has seldom been good, what with company downsizing and reduced defense spending. But it appears that things might be improving. If you haven't had a chance to read it yet, take a look at the article "Employment Picture Is Looking Up In The Rte. 128-Boston Area," in our Jan. 6 issue in our new *EE Currents & Careers* section. The article centers on what's happening with jobs in the technology corridor circling Boston, but it also puts into sharp focus the major trend of the past several years: The growth of software and embedded systems and their move into the mainstream of electronic system design.

A couple of quotes in the article stand out:

"The majority of jobs are software-related, but generally, companies want EE backgrounds," says Jeff Rudzinsky, senior vice-president of an employment agency in Lexington, Mass.

"The ratio of software to hardware jobs is, I'd say, 5:1 or 4:1. The people recruiting software engineers are running into one guy with ten offers, whereas we're having one hardware guy with maybe two or three offers," says Norm Davis, account executive at another agency in Lexington.

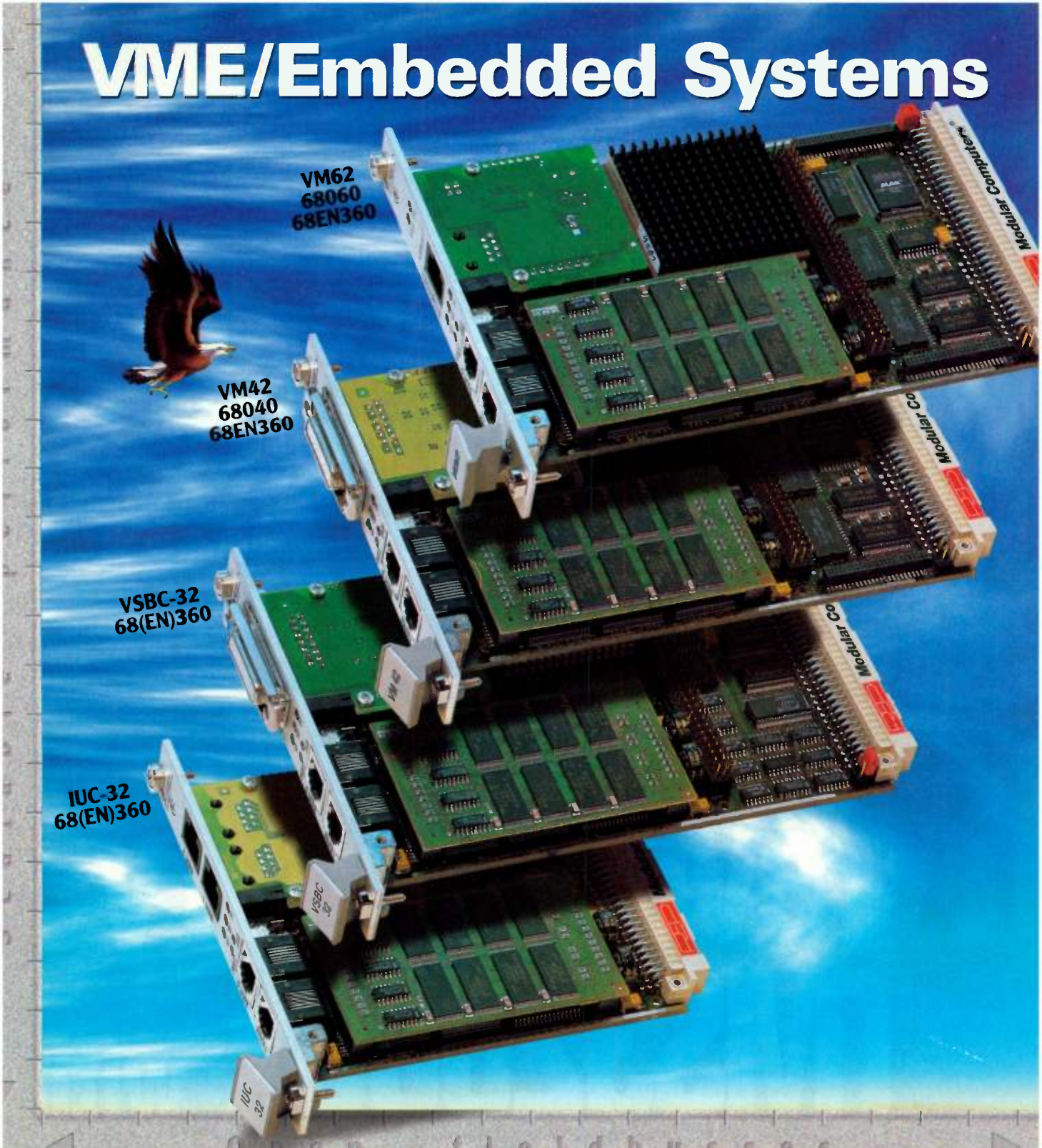
The essence of engineering is logical thinking applied to problem solving—which is exactly the process involved in writing embedded code. In a hardware-centered world, engineers have had to cope not only with solving the problems involved in the project at hand, but also with a strong self-preservation instinct—the critical need to remain current with the flood of new devices created by a rapidly advancing technology. In those situations, the experience gained with one set of components may not be directly transferable to the next generation of hardware. The value of mature engineering judgment often gets tempered with the need to get up to speed on the characteristics of one new set of components after another.

However, it may be that mature engineering judgment will maintain its value to a greater extent in a software-centered world. Here, the creativity and primary intellectual investment lies in the software itself, while the hardware is mainly the vehicle for delivering that added value.

The move toward software thus may bode well for engineering careers in the future, and it may mean an easing of the threats of career obsolescence caused by rapidly advancing technology. Software, in fact, may offer greater protection against engineering obsolescence than hardware, and it may be the very thing that leads the EE profession into the next century.

Stephen E. Scrupski
Editorial Director
Electronic Design
Information Group

VME/Embedded Systems



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* 25K unit production price.

Is USB A Bus In Search Of A Destination?

Every day, new ideas are touted as the next solution to some of the ills that plague the computer industry. Some solutions are tremendously successful, others have lukewarm acceptance, and others never make an impact. The universal serial bus (USB) is at a crossroads, with many proponents projecting a rosy future with billions of dollars in revenue. With both Intel and Microsoft behind the bus as the next low-to-moderate-speed interface that replaces everything from the keyboard port to serial and parallel I/O ports, and still other custom/proprietary interfaces, it offers tremendous promise.

Most new PCs manufactured with the latest motherboard logic chips have the USB ports hidden inside. But only a few of those systems currently have them actually wired to a connector on the rear panel because Windows 95 does not include USB driver software. The Win97 upgrade will include the driver software, and then it's a race to see who will succeed or fail in offering new systems that users will really want.

USB, or something like it, is sorely needed as the PC transitions into a home appliance. This "appliance" requires little knowledge on how it works—all users must know is that "Plug A goes into Socket A." USB-based peripherals will provide the incentive to move to USB, and systems designed in 1998-99 may do away with the RS-232 and Centronics-type ports in favor of USB.

DAVE BURSKY
DIGITAL ICs

But USB's popularity will develop slowly since it may take time for sufficient numbers of USB-active computers to arrive on user's desks. Meanwhile, what are peripheral manufacturers to do? Just let their designs sit on the shelf? Not likely. Some companies are considering postponing their mass-manufacturing of the products until enough machines are in users' hands to provide a viable market. Many are pondering alternate solutions: Go after the legacy systems market. Put USB into some of the 100 million-plus computers now running Windows, Windows 95 and Windows NT.

Designing hardware that adds USB ports or creates USB hubs is becoming a relatively simple task, with a number of silicon suppliers offering various chips and megacell building blocks that implement the USB interface for as low as $1 per port. Megacell suppliers such as CAE Technology and Lucent Technology will offer designers a way to create custom configurations. Standard silicon solutions from Atmel, CMD Technology, and Cypress Semiconductor, among others, offer fast time-to-market solutions.

The hardware issue is almost a moot point. So is the driver software that tells the PC it has a USB port. The BIG challenge is to craft applications that take advantage of USB and stir up user demand. For example, USB-based telephony, such as developed by Mitel Corp, Kanata, Ontario, Canada, is a step toward the application integration of new functions that would tempt users to add USB capabilities.

USB has many attractive features—it allows up to 127 devices to be simultaneously connected (each hot-pluggable), operates at data rates up to 12 Mbits/s, and can provide power and signals or just data signals over the simple cabling schemes. But unless applications drive the acceptance of USB in the legacy arena, the market may take longer to develop.

So put on your thinking caps—what types of software can take advantage of USB? Can you envision applications that require USB, or can provide value, if they could simultaneously use multiple pointing devices, multiple keyboards, or any mix of peripherals? Multiplayer games and some team/classroom educational/training applications are ideas that come to my mind. Perhaps a committee can focus on application-software development for USB-based hardware. Or, the industry may end up with a bus with no destination. *dbursky@class.org.*

Data Acquisition News

TAKE MEASUREMENTS, NOT ESTIMATES WITH NATIONAL INSTRUMENTS

VOL. 1, NO. 1

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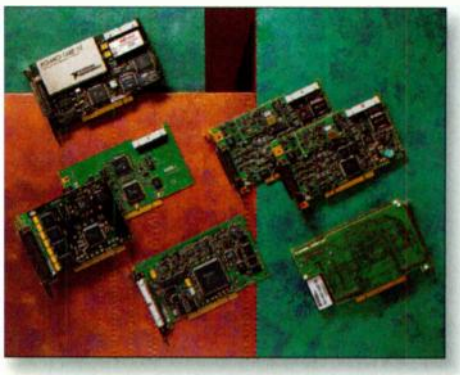

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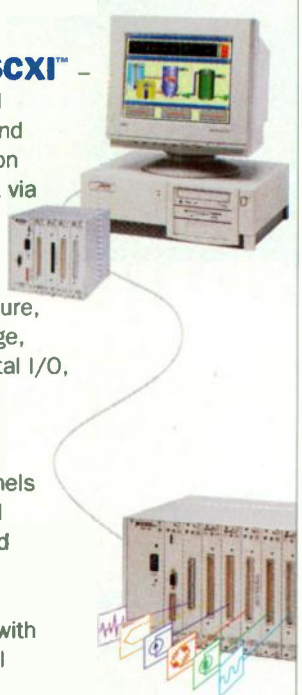

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**256K x 16 / 512K x 8	MT28F400B1	44	48
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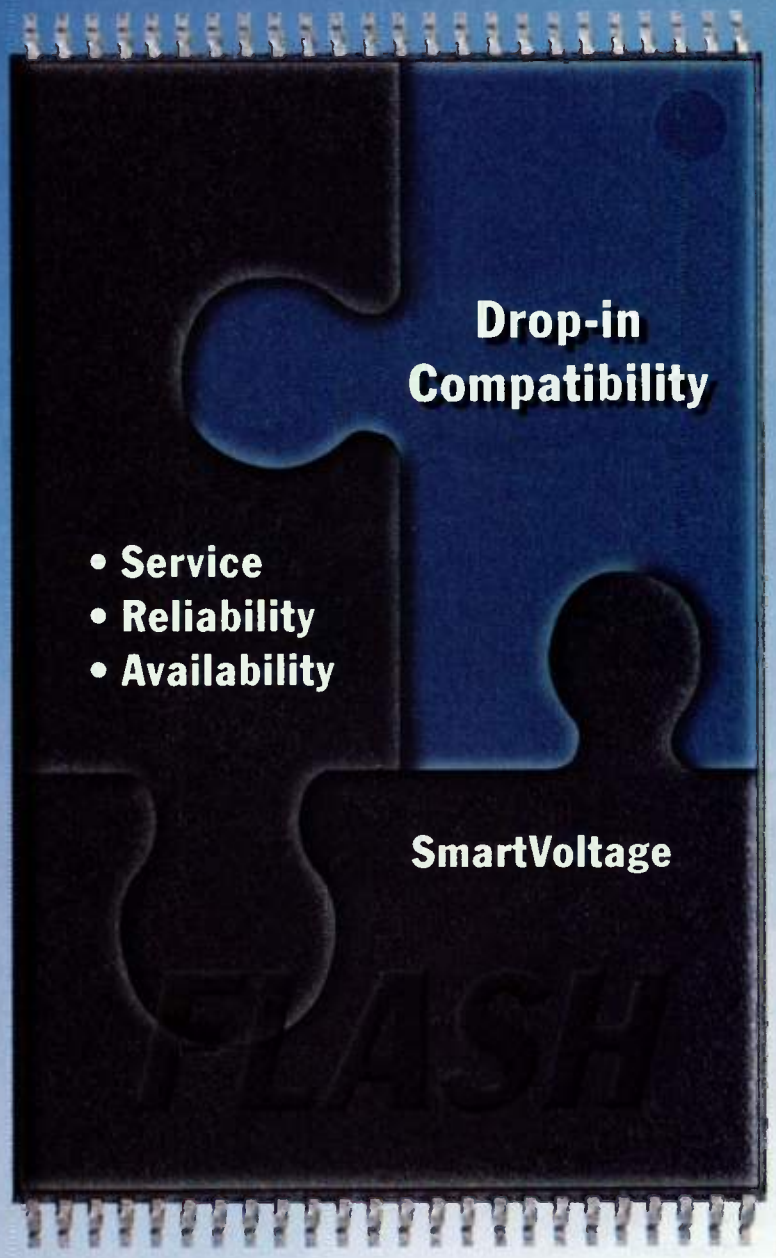

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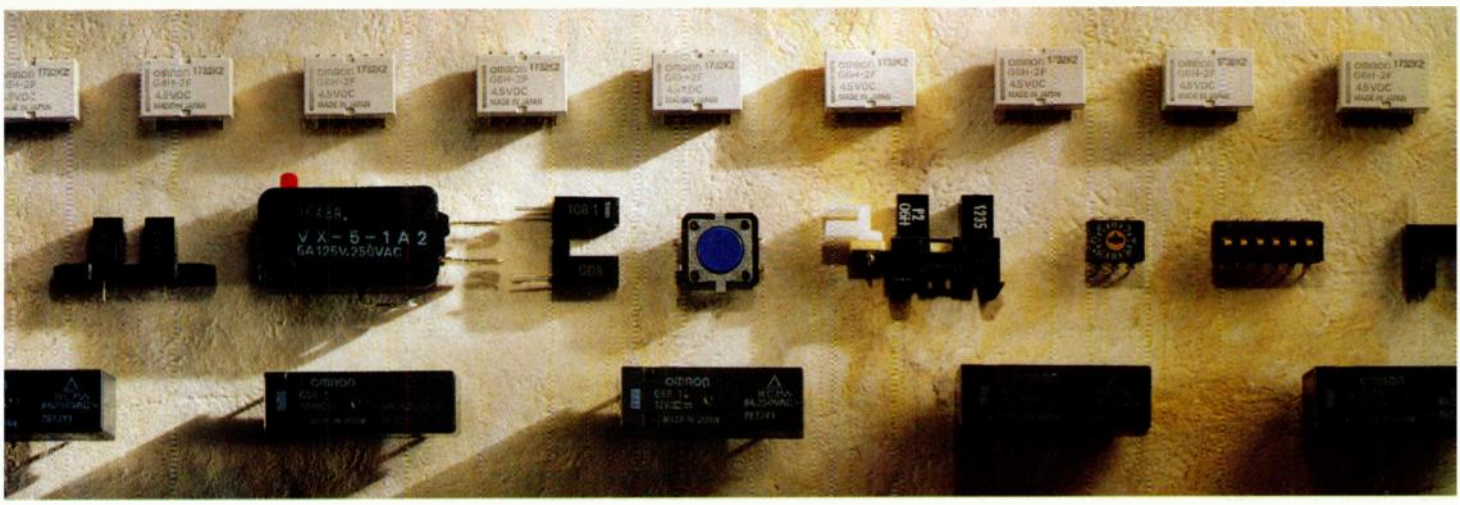

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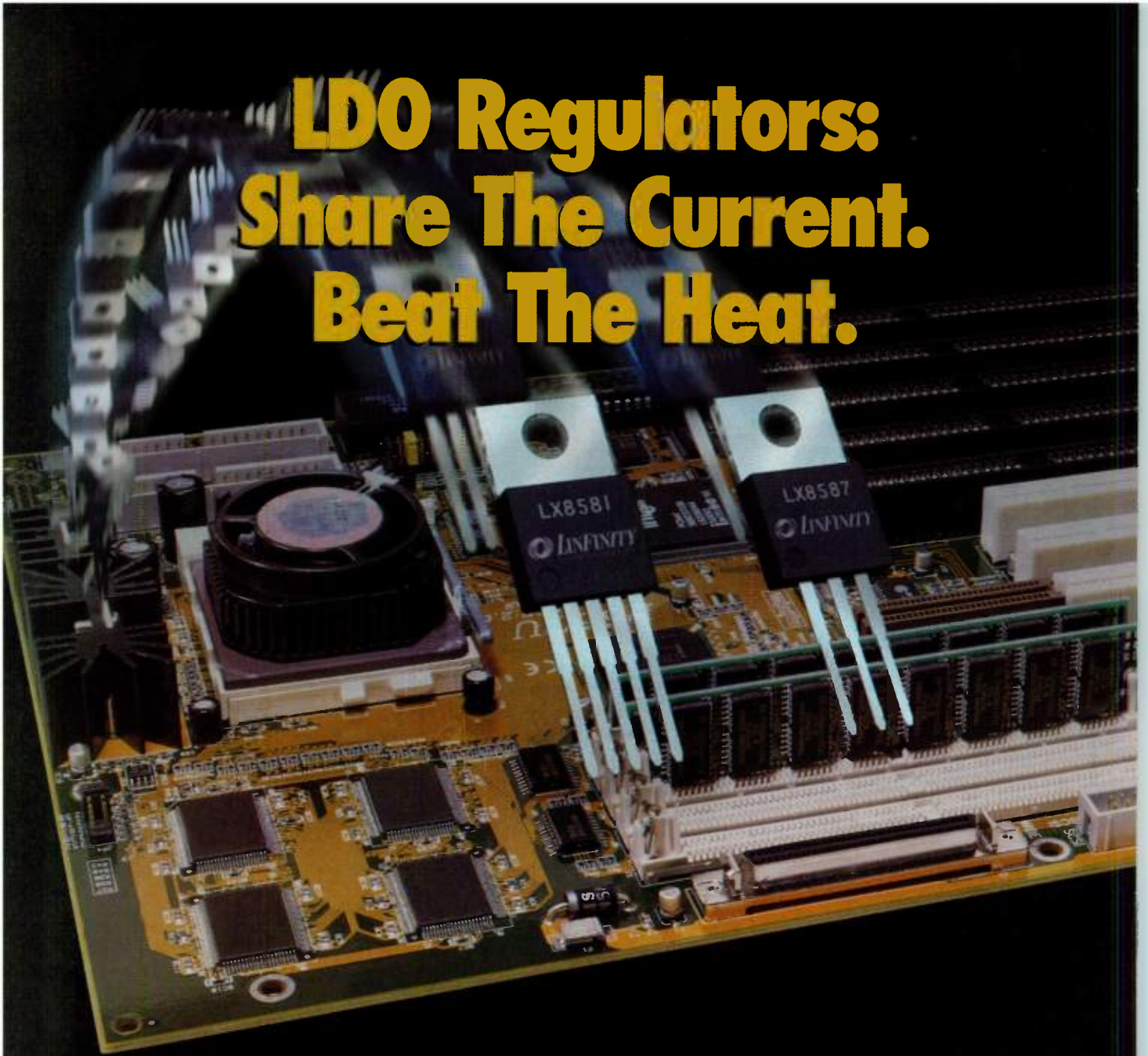

Device Type	Output Current(A)	Max Dropout Voltage (V)
LX8582	10	1.4
LX8592A	8.5	1.3
LX8583 A/B	7.5	1.5/1.3/1.3
LX8580	7	0.55
LX8584 A/B	7	1.4/1.2/1.4
LX8581	6	0.5
LX8596 A	6	1.3/1.1
LX8554	5	1.0
LX8584 A/B	5	1.5/1.3/1.3
LX8595 A	4.6	1.4/1.2
LX8587 A	3	1.3/1.2
LX8585 B	3	1.5/1.3
LX8586 A/B	1.5	1.5/1.2/1.3
LX8117	0.8	1.2

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READER SERVICE 113

Low-Cost Video-Port Standard Simplifies Implementation

With a burgeoning need for a low-cost, PC-based video interface standard, SGS-Thomson, Lincoln, Mass., devised the Video Interface Port (VIP) standard. Jointly developed with ATI, C-Cube, Cirrus Logic, LSI Logic, Philips, Trident, and S3, the VIP is an open, non-proprietary interface standard between video devices and a PC's graphics device. Aimed at multimedia PCs, possible applications include DVD, DSS, video capture, video phones, and Internet-based multimedia. The VIP architecture contains two separate ports, an ITU-R-656 video port and a simple host port. In a typical graphics chip configuration, the VIP requires just 13 pins for implementation. Because of the low pin count, the VIP employs the same 26-pin VESA feature connector for active signals and only adds one 14-pin connector for power and other miscellaneous signals. For more information, contact SGS-Thomson at (617) 259-0300 or on the Internet at http://www.st.com. *RN*

Focused Ultrasound Aims At Non-Surgical Cancer Treatment

In possibly five to ten years, physicians may have another weapon in their arsenal to treat cancer, namely forced ultrasound. Research taking place at the University of Michigan College of Engineering , Ann Arbor, could give physicians the ability to control and precisely focus ultrasound's ability to heat and destroy tissue.

High-intensity ultrasound in the frequency range of 500 kHz to 10 MHz produces heat as it passes through the tissue. Such ultrasound techniques have been used to heat tissue above the minimum temperature/time threshold required to kill cells. When heating is focused on a small area of soft tissue, effects on the patient are minimal. However, ultrasound heating in bone creates intense pain.

To that end, a computational model developed by graduate student Youssry Botros and researchers John L. Volakis, and Emad S. Ebbini was able to direct high-intensity ultrasound around solid objects and focus the field's intensity on small areas 1 to 15 cm deep within tissue. Botros states that their goal was to demonstrate the efficacy of high-intensity focused ultrasound for hard-to-reach areas, such as the liver.

"It is relatively easy to focus ultrasound's energy on small, deep areas of tissue," says Botros, "but not when the tumor is located beneath solid objects, such as the ribs, which is often the cases in liver cancer."

To validate the computational model, the three along with graduate student Philip Van Baren developed an experiment using wooden bars to approximate a rib cage enclosing a hypothetical tumor. The team used their model to calculate optimum placement and intensity levels using a 2D, 64-element ultrasound array. Experimental results agreed with the computational model: The 3-mm "tumor" was cooked in just a few seconds without damaging surrounding tissue. *RE*

Researchers Show Drives That Store 5 Gbits/In^2

A demonstration by the scientists and engineers at IBM's Almaden Research Center, San Jose, Calif., and Storage Systems Div., San Jose, Calif., displayed a bit density that was head and shoulders above anything that's near production—five billion bits/in^2. That specification is about three times the density of today's upper-end products. The test, data was read and written at product-level speed with acceptable accuracy (80 million bytes/s with one error in one billion bits). Using standard error-correction techniques, the researchers claim they can provide near-errorless data. One of the notable aspects of the demonstration was that mostly proven technologies were employed. For example, they used magnetoresistive (MR) heads and an ultra low-noise magnetic alloy disk coating. The company expects to be shipping drives with a density of 3 Gbits/in^2 within the next few years, with 5-Gbit/in^2 products following shortly thereafter. A 5-Gbit/in^2 density drive in a 2.5-in. form factor could hold about 6 Gbytes of information. A nine-platter, 3.5-in. model could store almost 55 Gbytes. For more information, contact IBM at (408) 927-1283 or on the Web at http://www.research.ibm.com. *RN*

0.13-μm Resolution Targeted By Joint Shared-Cost Program

ASM Lithography (ASML), Veldhoven, The Netherlands, and IMEC, Leuven, Belgium, have joined forces to launch a cooperative R&D program involving 193-nm-wavelength deep UV lithography. Using this technology, they hope to develop advanced optical processes that can produce line widths as small as 0.13 μm. Resolution in the 0.18-μm to 0.13-μm range will be vital when fabricating next-generation, high-density devices including 4-Gbit DRAMs and several generations of microprocessors beyond 686.

Leading semiconductor manufacturers are being invited to participate in the program. By pooling all of their technological resources, all participants will gain early process knowledge beyond today's 248 nm at a lower cost than individually funded R&D. The co-

operative program uses one of the first 193-nm scanning lithography systems to be built by ASML (at IMEC's Class 1 cleanroom facility).

According to Dr. Richard George, ASML's corporate director of step and scan marketing, "This next-generation scanning system will be based on 248-nm scanners currently in development at ASML's global headquarters in Veldhoven, the Netherlands." Process data and system performance results from the joint program will be incorporated in ASML's commercial 193-nm tool projected for market introduction in 1998.

Says Dr. Luc Van den hove, manager of IMEC's Micropatterning Group, "This unprecedented cooperative effort will shed light on the advanced optical patterning techniques needed to make tomorrow's memory and logic devices a reality." *RE*

Chamber-Cleaning Chemical Is Environment-Friendly

A recently identified chemical for oxide chamber cleaning reduces global-warming emissions by more than 95%. Trifluoroacetic anhydride, called EcoEtch-LF by Schumacher, Carlsbad, Calif., which discovered the chemical, cleans the process chamber faster and more efficiently, as well as uses less input chemical, than an equivalent C2F6 process.

C2F6 is a greenhouse gas used by the semiconductor industry as a source of fluorine for cleaning PECVD chambers. Approximately 60% of the C2F6 used during the clean process is unreacted by the process, and thus is exhausted into the atmosphere.

Motorola presented a paper during the Semicon Southwest Conference that described a feasibility study performed on an Applied Materials P5000 PE-TEOS reactor. According to the paper, EcoEtch-LF exhibits higher plasma-conversion efficiency and shorter clean times than a standard two-step C2F6 process. The process effluent contained less than 2 sccms (standard cubic centimeters per minute) C2F6 and less than 40 sccms tetrafluoromethane (CF4).

Cost-wise, EcoEtch-LF appears to be comparable to C2F6 used with a burn box. Overall, the results of the screening experiment indicate that the new chemical is a very promising candidate for further investigation as a replacement chemistry for C2F6. *RE*

BMDO Funding Leads To Results In ZnSe Thin Films...

North Carolina State University (Raleigh, N.C.) researchers, backed by funding from the U.S. BMDO (Ballistic Missile Defense Organization), have produced a set of coating technologies for compound semiconductors. These coatings are based on molecular beam homo-epitaxy to produce zinc-selenide thin films for making LEDs. The University licensed the technology to Eagle-Picher, Miami, Okla., which is using an award from the National Institute of Standards & Technology for work on blue and green LEDs and lasers.

The devices are based on compound semiconductor materials composed of precise atomic fractions of Type II and Type VI elements on the periodic table. So far, Eagle-Picher has developed a bright green LED using zinc-tellurium selenide (ZnTeSe). The greens are the brightest ever reported from a semiconductor material—at least 50 times brighter than commercial gallium phosphide. They operate at 512 nm and have operated for 675 hours at a current density of 50 A/cm^2. A blue LED also has been developed using zinc-cadmium selenide. Although weaker than the greens in output, it produces about 30 times more output than a blue silicon carbide LED. *PMcG*

...And The Acquisition Of Soviet Space Technology

Longer-life satellites and long-mission space vehicles are expected to outlast the life and endurance of solar cells. Deployment of solar-cell panels also has been one of the least reliable functions of launched vehicles. Consequently, nuclear space technology has been pursued in the U.S. under an R&D project called the SP-100 program. However, the players (the U.S. BMDO, NASA, and the U.S. Dept. of Energy) could not determine a near-term, space-qualified solution.

The former Soviet Union, on the other hand, successfully developed space-based electric-generating thermionic reactors at their science institutes. The heat source for the generators, the Topaz, is nuclear fuel. The initial result, called Topaz I, had been used successfully in two satellites. The latest version, Topaz II, then was bought by BMDO through International Scientific Products (San Jose, Calif.), which heads the marketing efforts for a joint-venture (called INERTEK) formed in Russia.

Negotiations, which began in 1990, resulted in delivery of the reactors in 1992 to the New Mexico Engineering Research Institute. At the Institute, they were tested with tungsten heaters instead of nuclear fuel. So far, the results have been positive enough for design studies to be undertaken on a 40-kW (peak) generator incorporating Topaz II technology.

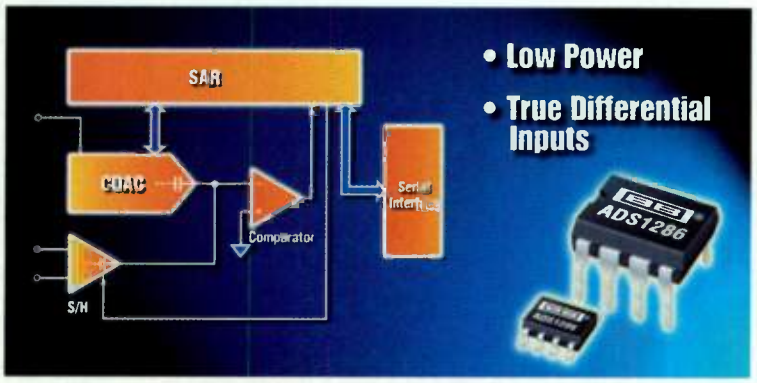
The SPACE-R system is being conceived by International Scientific Products and a sister company Space Power Inc. (also in San Jose). It's expected to weigh about half that of a comparable solar solution as well as occupy less than one-tenth the space. Sc versions are typically rated at only 6 kW (peak.) *P*

New Product Update

New, *microAmplifier*™ Single Supply Op Amp Series

OPA237 series is a new line of single supply, general purpose op amps featuring low offset voltage, low quiescent and bias current, and a wide supply range. This combination of "micro-sized" package options, excellent speed-to-power ratio, precision performance, and low cost makes them perfect for portable, battery-powered, and space limited applications such as PCMCIA cards. OPA237, single, is available in the micro-miniature 5-lead SOT-23 and SO-8 surface mount packages. OPA2237, dual, comes in a miniature MSOP-8 and SO-8 surface mount options. OPA4237, quad, is also available in a new compact package—the SSOP-16—it has the same body size as an SO-8, but with 16 leads. Key specs: 750µV max offset, 170µA/amp quiescent current, 1.4MHz bandwidth, and 2.7V to 36V or ±1.35 to ±18V supply range. Pricing in 1000s: OPA237 is **$.89**; OPA2237 is **$1.52**; OPA4237 is **$3.25**.

Reader No. 80 **FAX**LINE No. 11327



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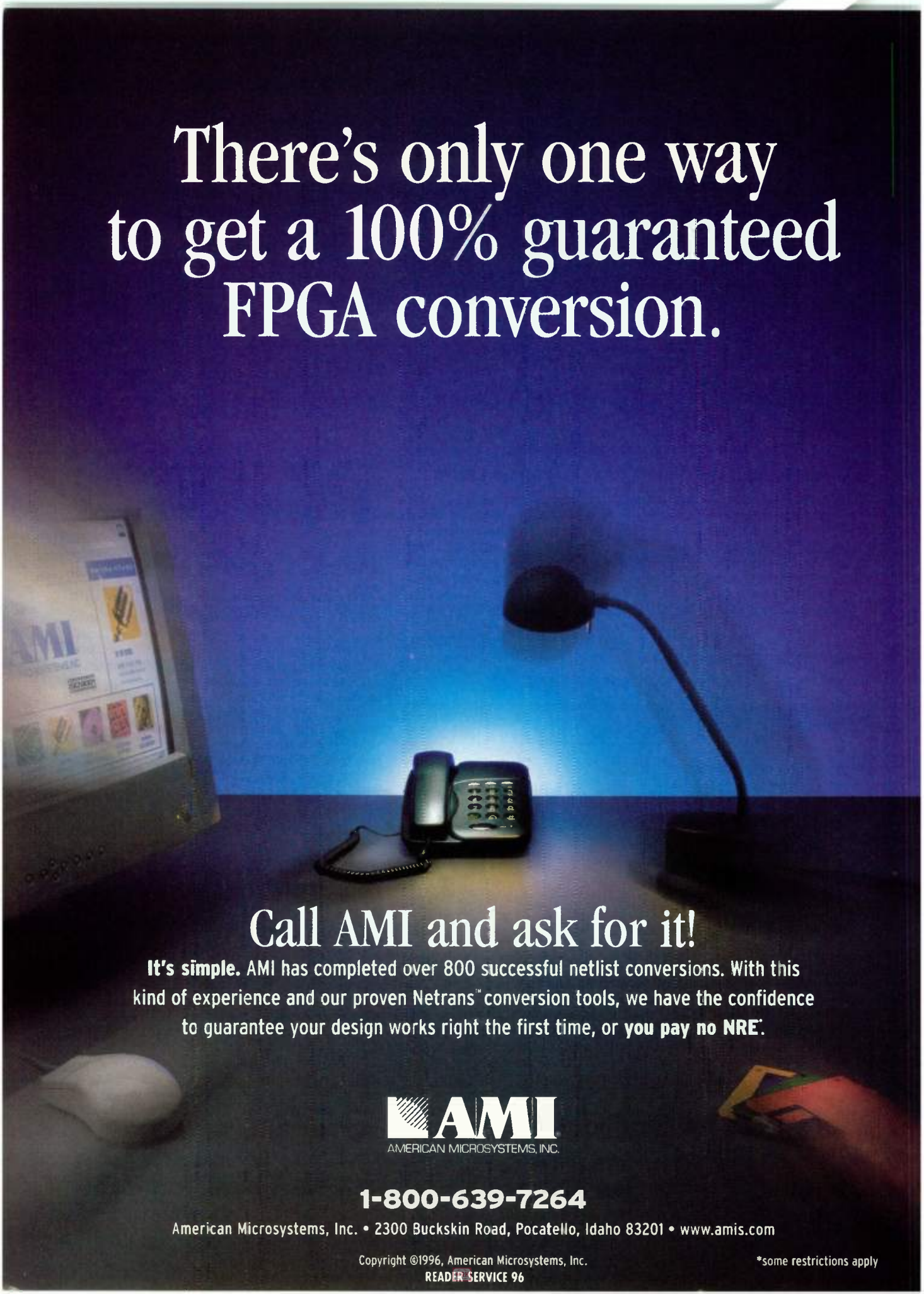
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READER SERVICE 96

Fractional Terabit ATM Switch Demonstrated: New Modular Architecture Accommodates User's Growing Bandwidth Needs

This fall, researchers at Lucent Technologies' Bell Laboratories demonstrated an experimental ATM switch with the capability of handling data transmissions up to 160 Gbits/s. The prototype system was constructed by tying together a cluster of Lucent's newest 20-Gbit/s, carrier-based backbone switches. When scaled up to Terabit-size, and used in a real network, this switch is capable of delivering 100,000 simultaneous digital video feeds, or giving as many as 10 million subscribers Internet access at ISDN speed.

While several commercially available ATM switches boast data rates of 20 Gbits/s or more, most experts agree that service providers will need Terabit-class switches to meet the demands of videoconferencing, Megabit Web access for consumers, and other bandwidth-hungry applications anticipated for the coming decade.

Currently, no real-world fiber link is yet capable of handling the output from a Terabit switch, but the writing is on the wall. Both Lucent and NEC have already demonstrated experimental fiber networks that have Terabit capacity, creating a significant opportunity for somebody who can deliver a commercially viable switch two or three years down the road.

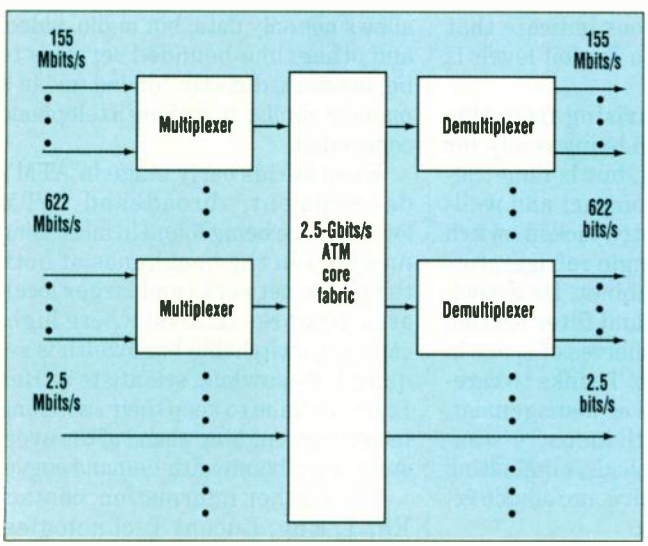
Rather than design the new switch from scratch, the Bell Labs team decided to take a modular approach based on the 2.5-Gbit/s, shared-memory technology found in their 20-Gbit/s GlobeView 2000, the flagship of Lucent Technologies' ATM product line. It employs a technique known as hierarchical multiplexing to aggregate streams of incoming ATM cells into a common high data rate which is then passed to a high-speed 2.5-Gbit/s, switching core *(Fig.1)*. The core itself uses a shared-memory architecture with a very wide data bus to switch large portions of an ATM cell in a single clock cycle.

As explained in their paper "A 160-Gbit/s ATM switch prototype using the concentrator-based growable switch architecture," (presented at the IEEE's ICC '95 Conference, June 18-22, 1995, Seattle, Wash.), individual lower-speed connections are multiplexed together and finally inserted at close to the full bandwidth of the switch. This allows the switch to run independently at its optimum speed while data feeds ranging from 51 Mbits/s (STM-1) and 155 Mbits/s (STM-3) right through 2.4 Gbits/s (STM-16) are folded seamlessly into the its data flow.

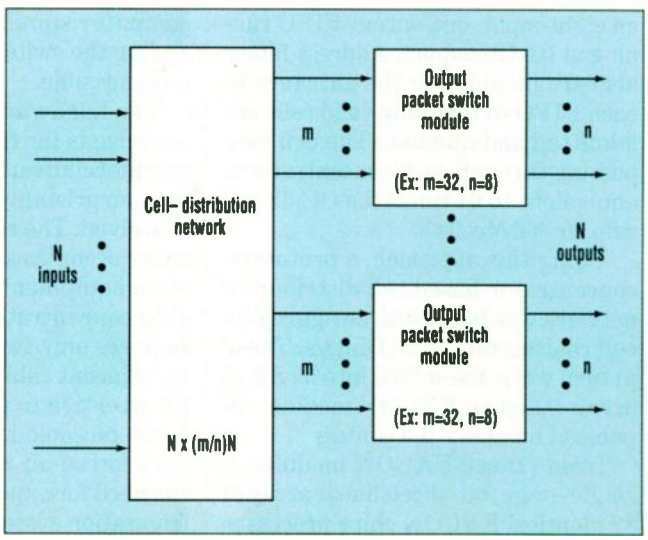
To create a 20-Gbit/s switch element, an 8-by-8 array of switch modules was assembled, fed by a memoryless cell distribution network *(Fig. 2)*. This 20-Gbit element became the principal building block in the project, from which a larger switching array was assembled.

When aggregating switch elements, one of the team's major challenges was to tie them together in a way that lets each module add its bandwidth to a common pool without getting in the other's way. Their solution was to develop a 64:8 traffic-concentrator/filter front end for each switch. The concentrator takes 64, 2.5-Gbit/s streams and aggregates them into 8, 20-Gbit/s streams *(Fig. 3)*. Since the switch modules have a 20-Gbit capacity, these concentrators allow traffic to be bundled neatly into groups of eight 2.5-Gbit streams.

Each 20-Gbit switch module has its own filter section which looks at the entire 160-Gbit data flow and only allows the traffic intended for its switch to pass. As each packet enters the concentrator, the filters read its header for routing information (virtual path, VP, and virtual channel, VC) and compares it against a table of connections collected from all of the switches *(Fig. 3, again)*. The filter then passes only the cells carrying the VP/VC addresses of connections that



1. The basic building block of the switch architecture is this 2.5-Gbit/s core fabric. It is fed by multiplexers which aggregate lower speed data and inserts them into the switch matrix at the full switching rate.

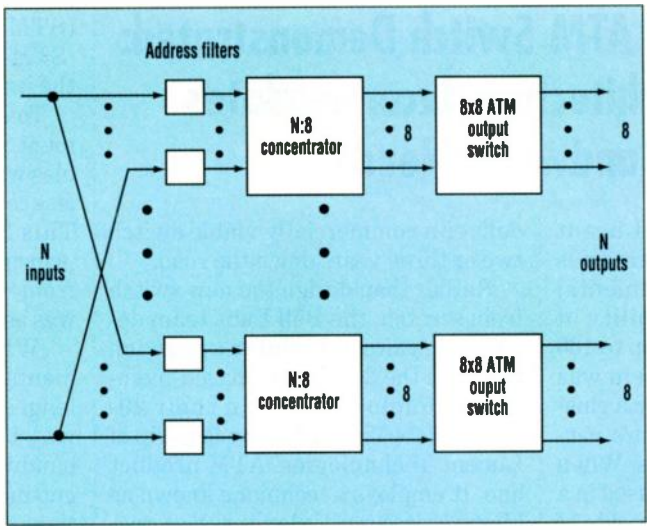


2. An N-by-N growable switch architecture can be built using 20-Gbit/s switch modules like this one. It consists of an 8-by-8 array of 2.5-Gbit/s switch modules fed by a common cell distribution network.

TERABYTE ATM SWITCH ARCHITECTURE

a particular switch is responsible for handling. In this manner, each switch has access to traffic from all 8 20-Gbit/s streams, giving the array a throughput of 160 Gbits/s.

The double-edged demands of scientific and commercial development created some interesting technical challenges for the team. Keeping size, power, and cost down, were balanced against maximizing performance to arrive at the final solution. While many elements of the switch were exported from current products, the concentrators themselves required the use of a high-speed, high-density VLSI chip to integrate enough functionality to keep the switches' size and power consumption within reasonable limits.



3. A closer look at a concentrator-based growable switch architecture also reveals that it uses an array of 20-Gbit/s switch modules, fed by data concentrators that, in effect, expose each switch module to the entire data stream. Address filters prevent a switch module from being overloaded by allowing it to see only the cells with the VP/VC addresses that it is assigned.

Using a standard 0.6-µm CMOS process, the team designed a VLSI circuit, known as an EXCON (expander/concentrator), that integrated eight 64:8 data concentrators. Each EXCON chip is an 8-by-8 device, processing 0.6 Gbits/s per port, for a total of 5 Gbits/s of cell traffic.

Cell traffic arriving at the EXCON chip is first broadcast via its 1:8 expanders, and then fed to eight parallel concentrators operating independently of one another. Each of these eight, 8:1 concentrators incorporates an eight-input, one-output FIFO running at 0.6 Gbits/port. Address filters also are included in the entrance to each FIFO so that only valid cells are admitted and queued. The cell rate passing through each concentrator is equivalent to 64 times the OC-48 cell rate, or 362 Mcells/s.

Using this approach, a prototype concentrator-based cell distribution network was built, with an aggregate cell routing rate of 20 Gbits/s. These in turn were assembled into an 8-by8 array called an EXCON module, capable of handling 160 Gbits/s.

Inside these EXCON modules, a single-stage, bit-sliced linear array of 32 identical EXCON chips processes the full bandwidth, allowing the board and device I/O bandwidth to be minimized. The pipeline for the switch matrix was now complete. Multiple 20-Gbit switching elements were interfaced to a 160-Gbit/s EXCON module, to form a prototype fractional Terabyte-class switch.

According to Kai Eng, head of Bell Labs' Broadband Systems Research department, the concentrators' 160-Gbit output can be cascaded into another 8:1 concentrator stage and another set of switches, resulting in a 1-Terabit switching array. Although time and funding did not permit its construction, Eng is confident that their empirical findings and computer simulations indicate that scaling the switch to Terabit levels is quite feasible.

The hardware arising from this exercise is far from being ready for commercialization, but is nonetheless surprisingly compact and well-conceived. The tightly packed switch array occupies a single refrigerator-sized equipment cabinet. Its associated concentrator and filter section requires only two shelves of space in an adjacent cabinet. Thanks to careful attention to power management, it can be cooled with industry-standard forced-air methods, eliminating the need for expensive, unreliable refrigeration systems.

The main cabinet also includes areas for plug-in line cards which can feed the switch with a variety of industry-standard line interfaces and data rates. These range from 51-Mbit/s twisted-pair copper lines and OC-3,155-Mbit/s fiber connections to optical trunk lines as large as 2.5 Gbits/s.

Reusing commercially available technology wherever possible helped reduce development costs and insure that the end product had a chance of being commercially viable itself. Equally important, developing a scalable switch architecture will allow users to avoid "forklift" upgrades, by buying a unit that meets their current requirements and adding bandwidth in 20-Gbit increments as needed. This may become an important strategy for network operators as they try to provision their systems for an uncertain future. Today's common wisdom is that bandwidth requirements will continue to increase for the foreseeable future, but opinions vary widely on the rate of increase, the types of traffic to be supported, and which network (PSTN, Internet, Intranets etc.) they will be travelling on.

Both Lucent and Bell Labs view high-capacity ATM switches as one of the key elements for enabling the widespread delivery of bandwidth-intensive digital multimedia services. The switched, cell-based, ATM traffic allows not only data, but audio, video, and other time-bounded services to be, in effect, directly "dialed up" in a manner similar to making a telephone connection.

Even at this early stage in ATM's development, broadband ATM switches are being found in increasing numbers in the backbones of both telephone networks and larger local-area networks (LANs) where high-capacity, switchable bandwidth is required. Meanwhile, scientists at Bell Labs continue to keep their switching technology one step ahead of the ever-steepening bandwidth-demand curve.

For further information, contact Kai Y. Eng, Lucent Technologies' Bell Laboratories, Holmdel, N.J., at (908) 949-3000.

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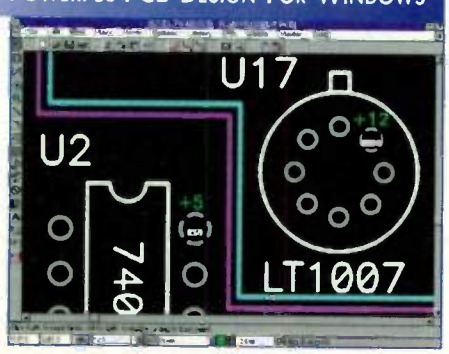

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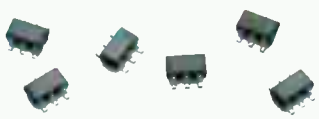

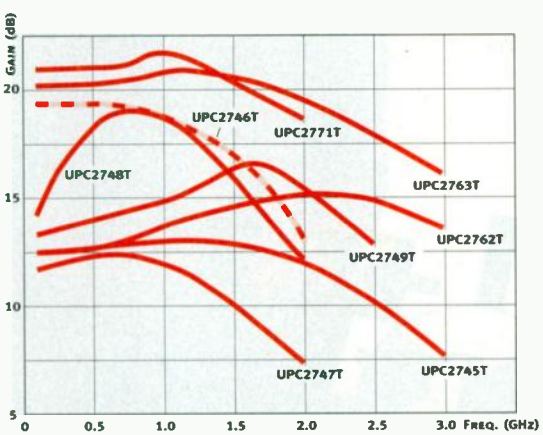

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UPC1678G	50 MHz–1.9 GHz	23	6	+15	49	500 MHz
UPC1688G	50 MHz–1.0 GHz	21	4	0	19	500 MHz
UPC2708T	50 MHz–2.9 GHz	15	6.5	+7.5	26	1.0 GHz
UPC2709T	50 MHz–2.3 GHz	23	5	+7.5	25	1.0 GHz
UPC2710T	50 MHz–1.0 GHz	33	3.5	+7.5	22	500 MHz
UPC2711T	50 MHz–2.9 GHz	13	5	-3	12	1.0 GHz
UPC2712T	50 MHz–2.6 GHz	20	4.5	-2.5	12	1.0 GHz
UPC2713T	50 MHz–1.2 GHz	29	3.2	-4	12	500 MHz

3V WIDEBAND MMIC AMPS—FROM 55¢

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UPC2745T	50 MHz–2.7 GHz	12	6	-3.7	7.5	500 MHz
UPC2746T	50 MHz–1.5 GHz	19	4	-4.5	7.5	500 MHz
UPC2747T	100 MHz–1.8 GHz	12	3.3	-11	5	900 MHz
UPC2748T	200 MHz–1.5 GHz	19	2.8	-8	6	900 MHz
UPC2749T	100 MHz–2.9 GHz	16	4	-12.5	6	1.9 GHz
UPC2762T	100 MHz–2.9 GHz	14.5	7	7	27	1.9 GHz
UPC2763T	100 MHz–2.4 GHz	19.5	5.5	6.5	27	1.9 GHz
UPC2771T	100 MHz–2.1 GHz	21	6	11.5	36	900 MHz

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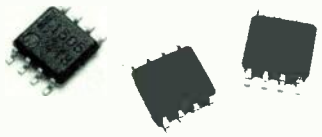

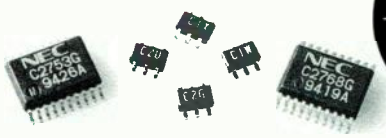

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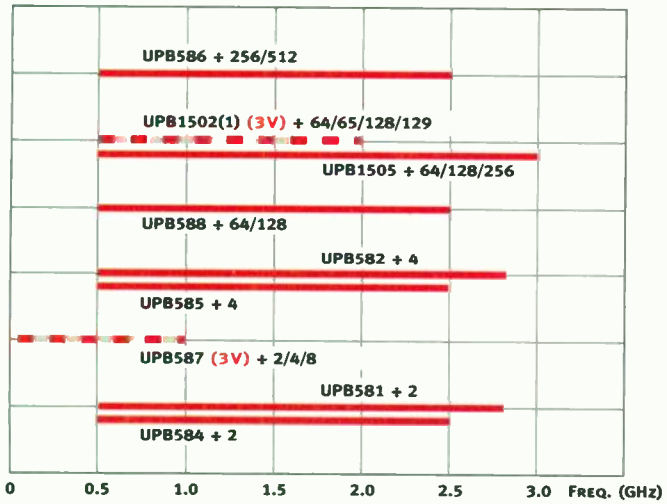

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UPC2758T[1]	100 - 2000	11	17	+6
UPC2753GR[1]	DC - 400	6.9	79	-17
UPC2768GR[1]	10 - 450	7	80	-17
UPC8106T[2]	100 - 2000	9	9	+1
UPC8109T[2]	100 - 2000	5	4	-4

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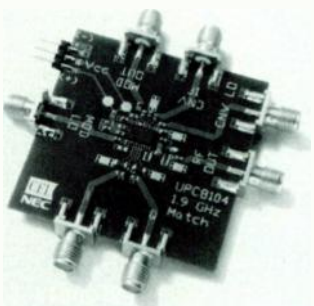

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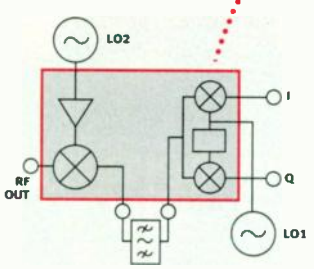

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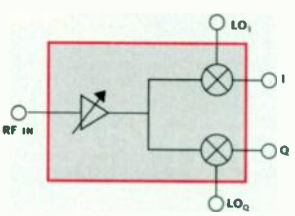

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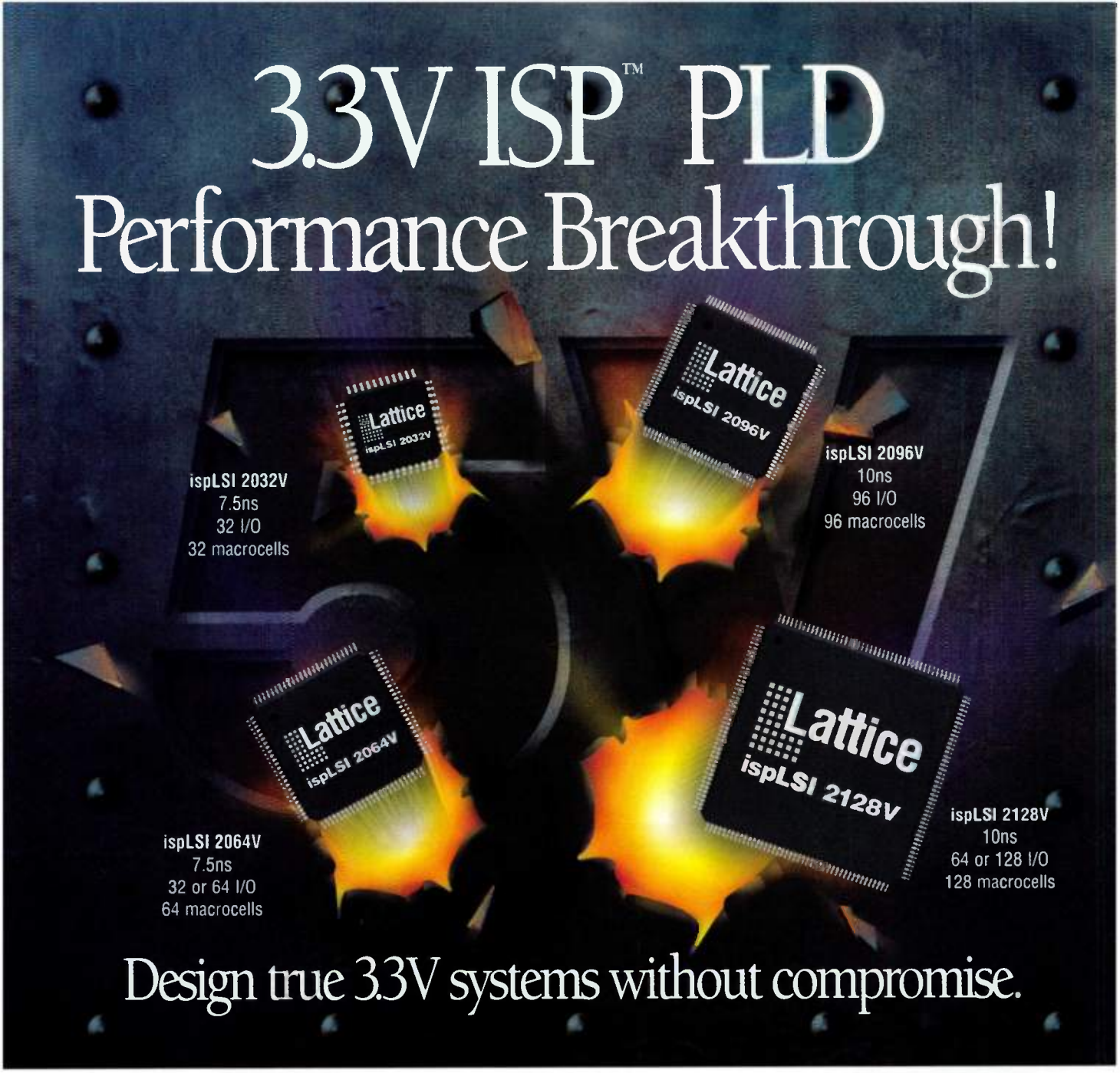

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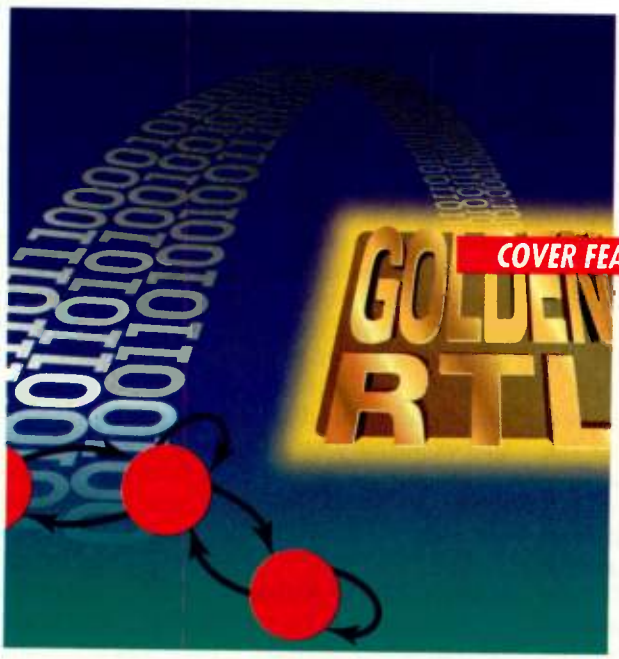
Formal Verification Tool Speeds Designers To Golden RTL

Modular Software Tool Family Enables RTL Verification To Bridge The Gap Between Functional Design And Implementation.

Cheryl Ajluni



COVER FEATURE

With IC complexity on the rise, ASIC and IC designers are facing a true verification crisis. It's becoming imperative that these designers must be able to conclusively verify a design's logic function during the register-transfer-level (RTL) specification, prior to functional and physical implementation. Without this assurance, the chance of a design failure significantly increases.

Today's designers use simulation for verification. But by using this technique, they are faced with the possibility of spending days, or even weeks, writing complex test vectors and trying to infer whether a design functions under all conditions (as well as trying to figure out what all the possible conditions are).

While inherently inconclusive, the simulation approach also has a number of other drawbacks. These drawbacks are compounded by the fact that there are a rising number of gates in a design—an estimated 5,000,000 gates by the year 2000—that make the simulation idea an inadequate one as the sole means of verification.

Primarily, the simulation method fails to tell designers when to stop running test cases. Rather, designers are forced to simulate with test vectors until they feel comfortable that they have tried every conceivable failure mechanism.

It's impossible, however, to predict every potential failure on a device. And, with rising gate counts, the number of possible design failure test cases and vectors to describe these cases are growing at an astronomical rate.

Even with faster simulators, pseudo-random vector simulation is quite slow. To make matters worse, even if one of the simulated test cases causes a failure to occur, it's often hard to figure out which vector showed the problem and how to fix it. Consequently, designers are left to grapple with the problem of how to achieve an adequate confidence level in a design up front, and also how to maintain that confidence level as the design evolves.

Modular Checkers

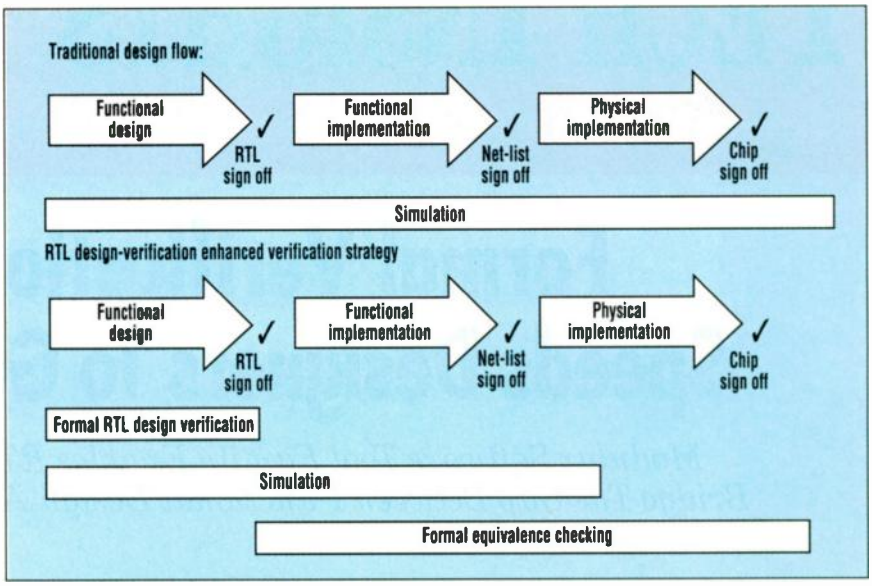
Realizing the overwhelming magnitude of the verification challenge, Chrysalis Symbolic Design Inc., North Billerica, Mass., has developed a family of modular formal specification-checking software products that ASIC and IC designers can use to validate RTL descriptions. As an addition to the company's current product offering, the Design Insight tool suite uses mathematical proofs, rather than simulation, to conclusively determine whether or not a design operates as expected at the functional level *(Fig. 1)*. Based on the company's proven symbolic-logic technology, the software tool can handle up to a million gates, has no logic-style or clock-scheme limitations, and offers a full range of logic states. The first module in the Design Insight software family, the State Machine Analyzer (SMA) model checker, specifically validates se-

quential RTL design specifications by treating any portion of the design as a finite state machine.

Design Insight's first available module, SMA, bridges the gap between formal verification ideas implemented in academic research tools and real-world design. It's not so much that these ideas were only thought to be possible in academia, but that no one had put them into practical tools specifically for commercial designers before. The bottom line, according to Scott Sandler, product manager, "is that completely validating RTL specifications is a hard proposition. Design Insight does it by providing conclusive answers to tough questions, and in a fraction of the time that would be required to simulate a meaningful set of vectors."

A number of earlier formal design-verification approaches, such as model checking and theorem proving, require the use of separate models or temporal logic relations and special languages, which are different than what designers are used to working with. Design Insight, which gives designers model checking capability, is able to read the exact model, or source file, that's going to be synthesized, rather than the same logic represented in a different model.

The Chyrsalis approach to the verification crisis has been to break the problem down into three parts—identifying any change that would alter the function of an original design; interactive formal tools to isolate the cause of such a problem; and RTL design verification (or specification checking) to help validate the design to produce a good reference. The company's first product offerings provide two pieces of the overall solution. These are: Design Verifyer, which uncovers inaccuracy and lets the designer know when the verification is done; and Design Explore, which grabs where the inaccuracy occurs and shows the designer the problem. Design Insight provides the last piece by allowing the designer to apply assertions to prove whether a design behaves correctly *(Fig. 2)*. Consequently, any design flaws, such as deadlock, livelock,, mutual exclusivity, or unexpected transitions, can be identified early in the design cycle when they are much easier to fix.



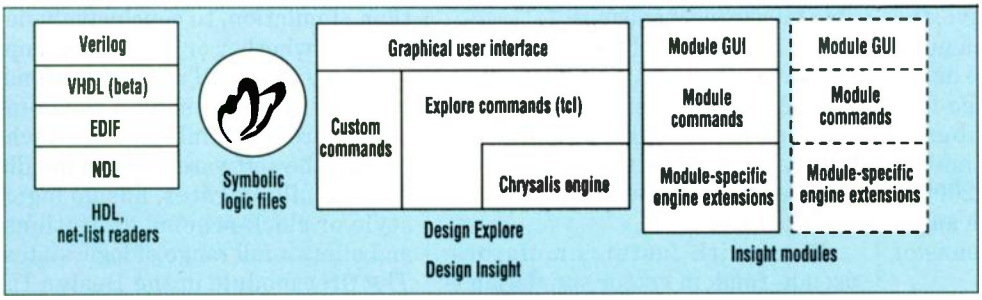
2. As opposed to the traditional design flow that espoused simulation as the only means of verification, Chrysalis' enhanced design flow incorporates formal RTL design verification and formal equivalence checking as part of the overall verification strategy.

Known Good Value

Because the RTL specification can be completely verified, it serves as a good reference against which design revisions such as changes to timing, test-logic insertion, or placement and routing, can be compared. Having this ability is crucial because it provides the solid reference models needed to make formal equivalency checking work properly.

According to Scott Sandler, " Designers use a number of tools other than verification tools to make design revisions such as timing modifcations, test logic insertions, and place and route. What they need is a solid regression testing method to make sure nothing got broken. Formal equivalence checking gives designers this method. DesignInsight provides the solid reference models to make it work." In addition, without having to use vectors and by limiting the use of simulation to instances where it's easy to make test cases, Design Insight can eliminate the time- and resource-intensive random-vector simulation currently used and provide a cheaper, quicker, and inherently easier path to "golden RTL."

To accomplish this, Chrysalis used the Design Explore tool as the foundation on which to base Design Insight. In doing so, Design Insight is able to leverage its general-purpose tcl scripting capability. The tcl language, currently being propagated by a grass-roots movement in the EDA in-



1. The Design Insight software tool from Chrysalis, which is based on the company's Design Explore product and its proven symbolic-logic technology, offers an RTL verification method that's significantly less time-consuming then traditional vector-based simulation.

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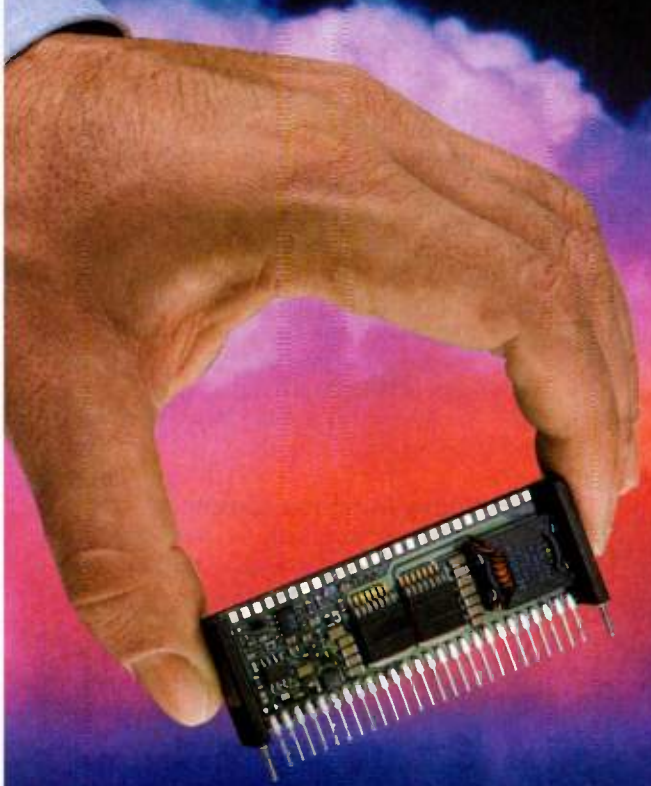

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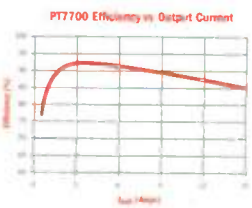

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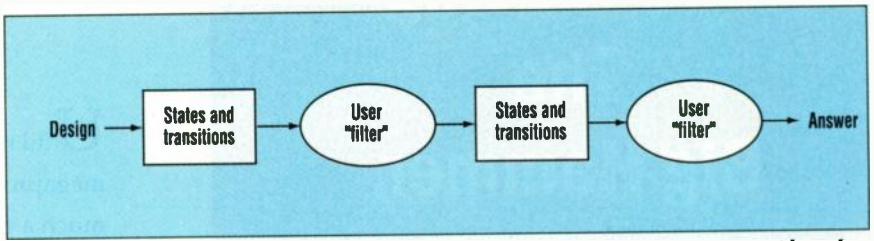
dustry, offers a flexible, standard syntax and execution environment for an electronic-design-oriented command-line interface. It includes all standard programming constructs, such as if/then, case, procedures, and file and terminal I/O.

The use of tcl script means that there's no need for designers to learn a complex temporal-logic language. Instead, the existing synthesizeable RTL is validated as is. Consequently, designers no longer have to recode design descriptions in an unfamiliar language—a procedure that often removes crucial model detail. The problem here is that while the validation on the model might be good, there is no correlation between this model and the one to be synthesized. Chrysalis' tool gets its value from reading the same model that will be synthesized and the use of the tcl tool makes this possible.Abstractions are produced automatically from scripted assertions entered on the command line. Literally, millions of vectors are replaced with a few lines of script. As Scott explains, "While the Design Insight tool doesn't replace the verification engineer, it's no longer necessary for the designer to throw the design over the wall to the verification engineer. For the first time, this tool puts formal verification capability on the desk of the actual designer. In doing so, it is the first step toward comprehensive understanding of correct-by-design RTL code."

Language-neutral compilation and the ability to customize the graphical user interface are two additional features enabled by the Design Explore foundation. The language-neutral compilation capability is unique in that it can read a designer's source descriptions, standard simulation libraries, and standard net lists at the gate and switch level, and then subsequently enables the encoded logic functions to be compiled into Chrysalis' symbolic-logic database. Whatever the input language is, the same mathematical structures (symbolic logic databases) are built. The compiled symbolic-logic database contains equations that include the clock, reset, and feedback terms vital to accurate representation of sequential logic. It contains these equations



3. Whereas vector-based simulation starts narrow and widens, the SMA starts very wide and uses constraints to narrow as the designer explores.

for every state bit and primary output of the design.

The Design Insight tool works by compiling a circuit into pure mathematical representation (symbolic logic) on which algorithms can operate.

The method in which the design's logic functions are checked by applying algorithms to the pure mathematical representation of the design's logic is part of the uniqueness of the tool. In the past, verification was done using vectors. Designers used these vectors to pose questions such as "does this vector cause this error to occur?" The difficulty with this line of questioning is obvious—if you don't ask the right questions, you could end up never getting the information you want. And, with millions of vectors to choose from, asking the right questions can be next to impossible. Design Insight, on the other hand, allows the designer to ask questions like "will a certain error condition ever occur, and if so, how?" More importantly, it allows these questions to be asked over the entire solution space and not just over the space of a few vectors.

Designers use a number of tools other than verification tools to make design revisions.

This method of specification checking is inherently easier than simulation because it enables designers to write assertions that specify correct behavior. Once an assertion has been entered, the software automatically attempts to prove that the design conforms to the assertion. If the design doesn't conform, a trace is produced showing the conditions under which the assertion does not hold. As an added benefit, once the logic functions have been compiled into the symbolic database and the appropriate validation scripts constructed, the designer can reuse them whenever a portion of the design is edited, providing an easy way to accurately replay important validation steps.

State-Machine Checker

The first module in the Design Insight family, the State Machine Analyzer (SMA) model checker, works by automatically extracting a state machine with all the associated states and transitions for a user-supplied list of state bits. This feature is especially beneficial because rather than requiring the designer to create state machines from a logic design, the module is empowered to work directly on the designer's RTL code to create automatic abstractions of state machines.

State machines, often used to express the behavior of complex designs as a set of state and transitions, have in the past posed an especially difficult validation problem. While a single state machine is relatively easy to design and validate, when designing large state machines and combinations of state machines, it's almost impossible to predict unexpected transitions that occur only under obscure conditions. However, if not planned for, these transitions could cause the design to deadlock or even go into a loop that could be broken only by resetting the entire design.

Design Insight's SMA completely eliminates the guesswork of predicting unexpected transitions by compiling a view of a state machine or

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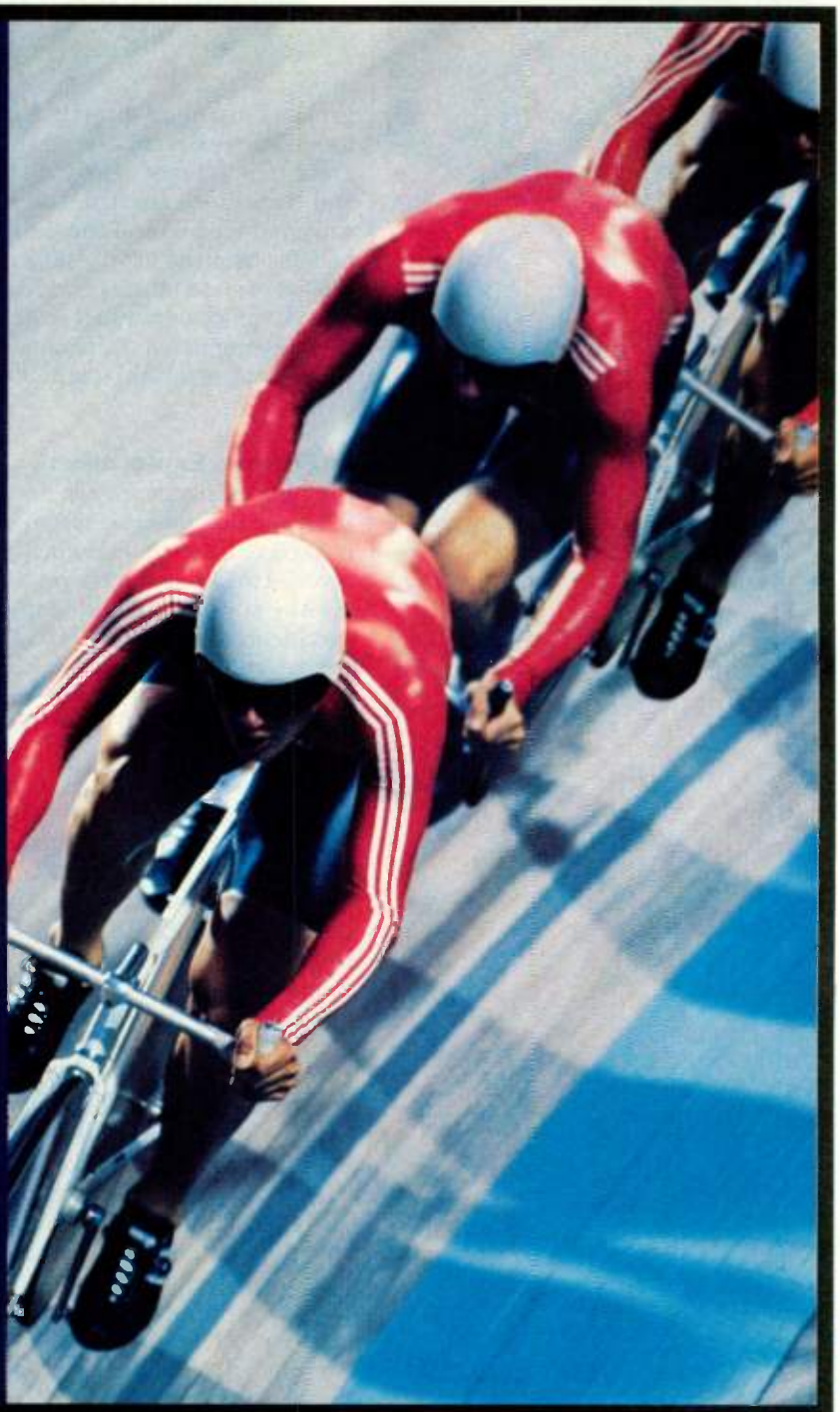

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group of machines directly from the user's source description and a list of state bits. Subsequently, all states and transitions are found automatically, independent of the designer's beliefs about the logic. And, because the list of state bits is provided separately, the designer can either analyze a combination of state machines or portions of a state machine in isolation.

Interactive Exploration

Once a design is compiled with the SMA and the state machine to be analyzed is extracted, tcl commands are invoked to begin interactively exploring the state space and identifying specific conditions of interest. When a condition has been identified, the software attempts to prove whether specific relationships between states always, or never, exist. All non-conformities show up as a trace. The investigation can be further refined using constraints, which are often included in scripts as an initialization step prior to validating a particular design function. These constraints limit the analysis to a particular range of input/state conditions, such as a particular mode of operation, or on a subset of a design's functions *(Fig. 3)*. When a constraint is set, constant values are applied to a small number of the designs signals. Then, as the software propagates these values through the design, constant-valued terms are factored out of the equations in the symbolic logic, making the design appear to be in a particular operating mode.

Because the SMA software can compile any combination of source descriptions, including synthesizeable RTL, gate-level, and switch-level net lists, the same proofs used to validate RTL models can be applied to any level of design abstraction. In addition, the designer can analyze the design or apply assertions at any level of the hierarchy without constructing a separate test bench. Constraints that are applied to signals of the block being tested set up conditions that would normally be provided by the surrounding logic. Consequently, functional relationships can be validated at any level of the hierarchy without the overhead of the surrounding blocks.

The benefits of Design Insight and State Machine Analyzer to the ASIC and IC designer are enormous. Designers can now thoroughly validate RTL descriptions using a combination of assertions that cover many of the detailed behavioral requirements of the design, and also simulations of only the design's fundamental operations. Given the ability to apply constraints, the designer can focus the verification analysis on a specific part of logic rather than having to conduct a lengthy verification of the entire design. And, because any RTL-based problems can be identified and debugged earlier in the design cycle, the chance of finding a failure later in the design cycle when it can be costly to repair, if not deadly to the design, is eliminated. With the time saved during verification, the designer can spend more time conceptualizing and optimizing the design function .

Chrysalis plans to develop other modules that will encompass elements from a range of formal-verification techniques, such as model checking and theorem proving. Targeted at specific RTL problems, the modules will focus on providing conclusive proof with less user guidance, as well as advanced multi-cycle debugging. In addition, they will seek to extend the commands available for proving correct design behavior. Consequently, users will be able to make assertions about expected behavior in terms of the pins of a design, and the software will automatically determine which state bits are implicated.

Price And Availability

The Design Insight specification-checking software is available now on Sun Microsystems SparcStations, Hewlett-Packard 9000/700, IBM RS/6000, and Digital Equipment Alpha workstations and servers. It sells for $35,000. The State Machine Analyzer, which is priced separately at $45,000, can be accessed through the Design Insight or Design Verifyer software.

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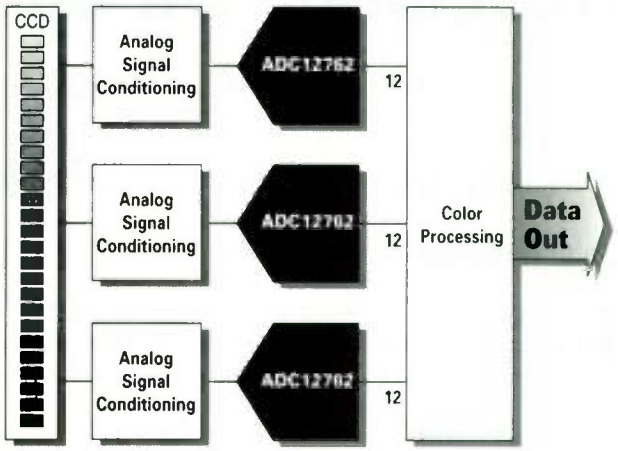

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Logic Analyzer Hits 500-ps Resolution On Up To 680 Channels

A New Modular System Architecture Makes Circuit Verification And Characterization Faster And Simpler.

John Novellino

Instrument manufacturers are constantly scrambling to keep up with advances in the signals that their customers must measure. Factors like signal complexity and dynamic range are often a problem, but frequency most often creates the hurdle, either in the form of bandwidth or "speed." Logic analysis is a good example. With processor speeds now well over 100-MHz, advanced digital logic circuitry is experiencing analog-like problems such as crosstalk and reflections. Consequently, designers need extremely high-resolution instruments to detect fast glitches and subtle timing problems.

Designed as an answer to that problem of high-speed digital design analysis, Tektronix (Tek) Inc., Beaverton Ore., has introduced a card-modular logic analyzer series that uses an asynchronous oversampling architecture to deliver 500-ps timing resolution (equivalent to a 2-GHz sampling rate) on up to 680 channels. The new sampling technique, called MagniVu, was derived from the Digital-Real-Time technology employed in Tek's TDS series of digital oscilloscopes.

The TLA 700 series of logic analyzer products includes two mainframes with color displays, the two-slot portable TLA 704 and five-slot benchtop TLA 711 *(Fig. 1)*. Users can equip the mainframes with logic analyzer modules offering from 34 to 136 channels and digital scope modules with up to four channels. In addition to the 2-GHz timing analysis on each channel, the logic analyzer modules provide 100- to 200-MHz state analysis simultaneously through a single probe. Memory depth is up to 512 kbits per channel. An optional high-density probe features a controlled impedance and only 2 pF capacitive loading.

Users can employ the 500-ps timing resolution to check out glitches or other problems by "zooming" from the state view to the timing view. If a glitch occurs, the analyzer will mark the data display, with 500-ns resolution, even if the operator is not looking for a glitch. The high-resolution samples are stored in a dedicated 2k-deep, 2-GHz memory separate from the main memory.

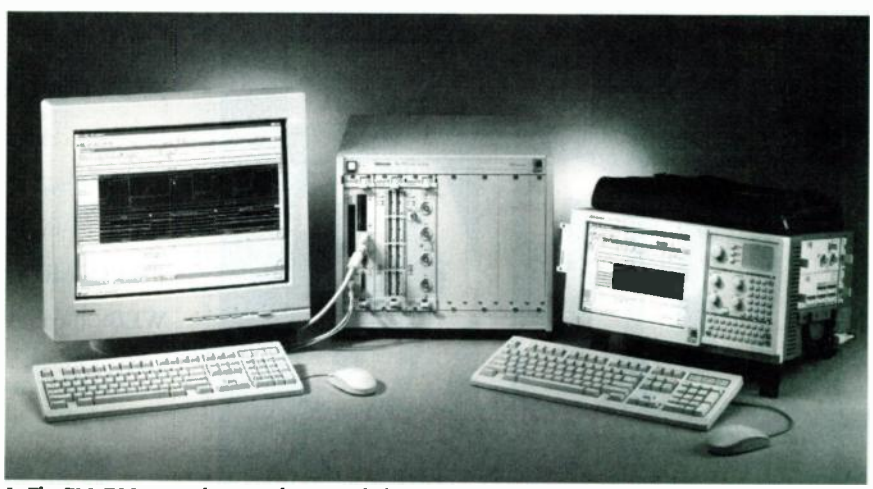
The scope modules offer a 1-GHz bandwidth, a 5-Gsample/s sampling rate, and a 15k record length (all on each channel). Advanced time-domain fault triggering allows users to capture both the digital and analog context of hard-to-find problems. Triggers include edge, pulse width, timeout, glitch, runt, setup and hold, slew rate, immediate, and logic and wait-for-system triggers.

Both mainframes come with Windows 95 fully integrated and embedded. As a result, the instruments' user interface is familiar to designers and is compatible with networks and printers through standard PCMCIA peripherals. Tek also offers a broad range of microprocessor support packages for the units.

Slow Clock, Fast Sampling

The beauty of MagniVu is that it relies on a clock rate of only 250-MHz to sample at 2 Gsamples/s. The heart of the architecture is a full-custom, digital sampling front end that acquires all signals, including clocks, asynchronously. The Digital-Real-Time technique used in the Tek DSOs is what allows the analyzer to sample at eight times its clock rate. Using the higher clock rate would have been much more difficult and more expensive.

Instead, Tek built a delay chain made up of eight 500-ps delays to clock a set of eight sampling circuits. For every 4-ns "tick" of the 250-MHz clock, the analyzer acquires eight samples at 500-ps intervals for each channel. After sampling, the data is



1. The TLA 700 series logic analyzers include a two-slot portable model (left) and a benchtop version with five slots available to users. Both come with Windows 95, so the user interface is familiar to designers.

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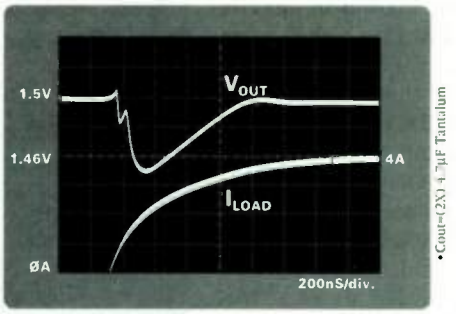

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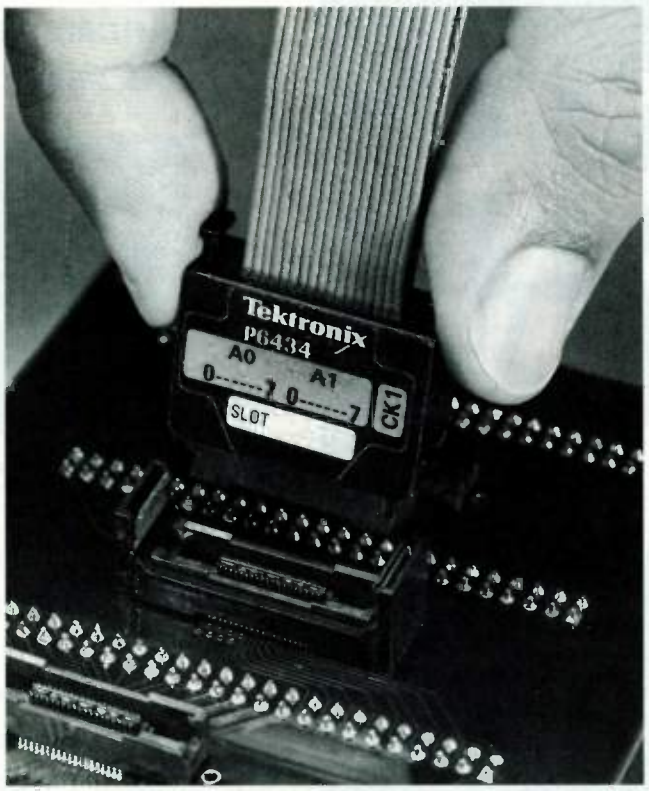
processed digitally, so the signal is not degraded and skew is minimal.

Each consecutive 8 bits of data are loaded in parallel every 4 ns into a shift register that feeds out selected pieces of the data to the off-chip 512k main memory, which consists of common RAM devices. The register feeds out the data based on user-defined clocking, triggering, and storage parameters. The RAMs can store asynchronously acquired data at up to 250 Msamples/s or synchronously acquired state information at up to 200 Msamples/s.

At the same time, the faster 2k-deep memory, which is implemented as a custom array on the chip, directly stores the unconditioned stream of data straight from the sampler for each channel. This high-speed memory is deep enough to store 1 µs worth of data for each channel, which is eight to 50 bus cycles worth of information for state-of-the-art systems.



2. The optional P6434 probe makes 34 signal connections in an area of only 1.09 by 0.39 in.

Simultaneous Acquisition

Note that these acquisitions are going on simultaneously. As the overall state activity is stored in the larger, slower memory, complete timing information is being directly captured in the faster memory. Consequently, only one set of probes is needed to supply one data stream to provide both 2-GHz timing and 200-MHz state analysis. Therefore, when an anomaly occurs, the designer can immediately take a closer look at a timing resolution of 500-ps without having to reacquire data. This capability is especially useful for problems that occur infrequently.

In addition, the glitch detector monitors the high-speed data stream out of the sampler, looking for glitches on every channel. A glitch will trigger the analyzer, so the designer can then switch to the MagniVu acquisition and actually see the number, width, and placement of glitches within the sample period with 500-ps resolution. The MagniVu technology also allows the analyzer to produce extremely precise time stamps, which is important for characterizing clock stability.

Another key feature of the TLA-series analyzers is their ability to recognize and trigger on setup-and-hold violations across all channels. The setup-and-hold checker detects transitions in the input signals after they are acquired by the high-speed sampler. The analyzer then adjusts for skew and flags the transitions if they occur within the interval defined by the user. The operator can setup a 2-ns setup-and-hold window and position it from -8.5 to +8.0 ns relative to the clock, again with 500-ps resolution.

The TLA series comes standard with the appropriate number of P6417 17-channel probes for the ordered configuration. The optional P6434 high-density probe connects to 34 signals, employing a mass-termination technology that makes four times as many connections in the same area as traditional square-pin probes *(Fig. 2)*. The 34 connections take up only 1.09 by 0.39 in. of board space. Four probes will handle a Pentium processor. Besides saving space, the high-density probe allows very fast setup of the instrument, compared to conventional probing techniques.

An optional latching capability adds very little additional size while keeping the connection from accidentally coming loose with up to 10 lbs. of pull. An easy release mechanism makes disconnection simple.

The P6434 also boasts superior electrical characteristics. A 2-pF capacitance and a controlled impedance improves dc and ac loading of fast signals and minimizes reflections. The probe offers isolation between channels and shielding against outside interference.

The TLA series' enhanced measurement capability allows engineers to perform comprehensive timing verification and characterization of their projects, where previously they had to rely on independent measurements of small sets of signals. Meanwhile, the single-probe capability and high-density probe makes setup faster and easier.

Price And Availability

The TLA 704 two-slot portable mainframe costs $9000; the TLA 711 five-slot benchtop mainframe is $14,000. Logic analyzer modules range from $5000 (34 channels, 2-GHz timing, 100-MHz state, 32k memory) to $39,000 (136 channels, 2-GHz timing, 200-MHz state, 512k memory). Four DSO modules come in two performance ranges: 500-MHz bandwidth, 2.5 Gsamples/s, 15k memory ($10,000 for two channels and $17,000 for four channels) and 1-GHz bandwidth, 5 Gsamples/s, 15k memory ($18,000 for two channels and $28,000 for four channels). The P6434 high-density probe costs $995. Support packages for more than 40 microprocessors are available, ranging in price from $1950 to $8950. Delivery is within eight weeks.

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PRODUCT FEATURE

Adding Standard Cell Blocks To ORCA FPGA Family Enables Gate-Array Density

With family members packing up to 225 kgates, Lucent Technologies' 3C series of SRAM-based FPGAs will allow designers to merge in standard cell blocks to achieve greater system functionality and higher levels of performance. As a result, designers will have at their disposal system ASICs with a large FPGA on-board. The combined technology will allow designers to define the key functions in the ASIC early and employ the programmable logic for last-minute logic implementation. The system ASICs can be implemented by using synthesis-based design tools—a capability that leverages Lucent's experience in the field.

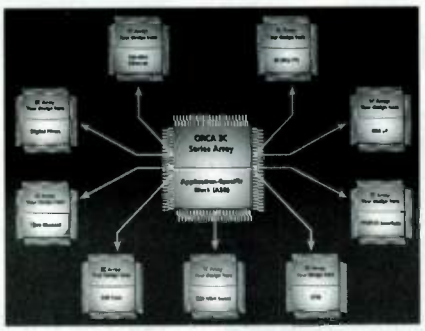
In many ways the architecture of the chips in the 3C family is an extension of the 2CA family—it's still a lookup-table-based architecture employing SRAM configuration elements. However, there are many enhancements that improve both performance and density. Thus, the chip can operate with system clock rates from 10 to 80 MHz, and internal blocks of RAM can be accessed at rates exceeding100 MHz.

To ease the system interface requirements, the chips include a dual-use microprocessor interface that can be employed to perform configuration, readback, device control, and device status. Glueless interface settings are available for the i960, PowerPC, and MC68xxx series CPUs.

One major enhancement to the internal logic architecture is the addition of new blocks called supplemental logic and interconnect cells (SLICs). These blocks have a complexity approximately equivalent to a 22V10 PAL. The SLICs look very much like small PALs, and thus give the 3C series a sort of combined FPGA and CPLD architecture.

These SLIC cells perform functions that FPGA cells can't efficiently implement—they can implement functions such as 10-bit decodes, or 10-bit AND/OR functions, or 8-bit three-state driver functions. For example, a decoder formed in a SLIC cell can take a signal from an input pin, through an 8-bit decode, and then off chip in just 7.5 ns. That's twice as fast as going though a lookup table.

Designers also improved the clock routing to boost the speed. Its system clock allows any input pin to serve as a clock. Thus, on the 3C family, the clock-to-output delay has been cut to just 6.8 ns. Also added to the 3C arrays are express clock lines that have a clock-to-output delay of 5.8 ns (one line is available on each of the four sides of the array). Each of these lines also includes a gated-clock capability (glitch free). These lnes would permit some degree of power management by using the gating signal.



At the highest level, each 3C family member consists of an array of programmable logic cells (PLCs) surrounded by programmable interface cells. The PLC, in turn, consists of a programmable function unit (PFU), various local routing resources, and one SLIC block.

Providing more functionality than its counterpart in the OrCA 2CA family, the 3C PFU contains what the Lucent refers to as a twin-quad level of functionality. Two sets (twin) of four (quad) lookup tables (LUTs) and two sets of four flip-flops are included, as is one additional flip-flop. All of these blocks can be controlled independently.

The output of one lookup table can be routed to another lookup table in the same block without going to the external routing pool. That results in a 30% speed improvement in critical paths with cascaded multiple lookup tables. In the 3C series, the chip designers added some diagonal routing capability for nearest-neighbor connections, thus allowing neighboring cells on a diagonal to be cascaded as well. That also creates a 30% speed improvement.

Thus, multiple LUTs also can be combined with the routing to form larger functions with minimal delays thanks to an enhanced soft-wiring approach. This enables functions of up to 21 inputs to be implemented in one PFU. Furthermore, two programmable clock managers are located on-chip.

The first chip in the 3C family will be the 3C55, which packs an 18-by-18 array of PFUs (32-72 kgates, depending on how much RAM is implemented), contains 324 SLIC blocks, and provides 288 user I/O lines (PFUs are estimated to contain 96 gates for logic-only designs, but RAM blocks are very efficient and up to a 32-word-by-4-bit RAM can be implemented in a PFU).

Scheduled for release shortly thereafter will be the 3C80 and 3C125. The FPGAs will pack 47-174 kgates and 352 or 448 I/O lines, respectively. The largest family member will be the OR3C225, which will offer from 140 to 320 kgates and up to 608 I/O lines. And when volume could justify it, the 3C-based logic can be converted into a fast-turn standard cell design flow that further reduces chip size and cost. Designers can either get 100% timing-compatible chips or higher speed.

In addition to the generic devices, the mixed standard cell/FPGA chips—the OR3T55, 80, 125, etc., will offer users more application-specific options—one chip will most likely pack a 66-MHz PCI bus interface. Another might offer a USB core, or still others can leverage all of the cells in Lucent's standard cell library.

The 3T55 will pack an array of 18 by 14 PFUs and about 80 kgates of prediffused standard-cell logic. A prime candidate for those 80 kgates is a high-performance PCI port with programmable FIFO buffers.

The 3C55 ORCA FPGA will sell for $159 apiece in lots of 1 to 25 pieces; samples are expected in mid 1997. The remaining family members will be released throughout the latter half

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PRODUCT FEATURE

of the year and in early 1998. Family members with less than 80 kgates will come in both a 5-V version and a 3.3-V optimized version (with 5-V tolerant I/Os) that's about 20% faster. Above 80 kgates, the family will only operate from 3.3-V supplies.

Configuration development can be done on standard CAD tools or on Lucent's ORCA foundry, which is based on the NeoCAD tool suite. The tools are available on CD-ROM, and will sell for $4995 (for PC version that covers all ORCA family chips). A workstation version of the family sells for $7995.

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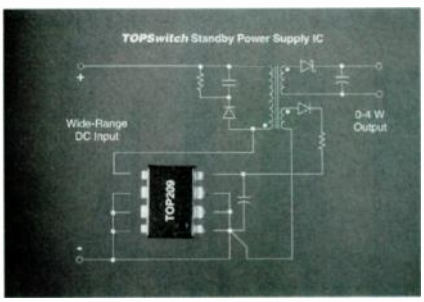
Low-Power Switching Supply IC Is Optimized For Standby Applications

Optimized specifically for low-power, standby, power-supply applications, the three-terminal TOP209 switch-mode power-supply off-line PWM switch can deliver up to 4 W from a 100/110/230-V ac input, or 2 W from a universal supply input of 85 to 265 V ac. The low-cost device, which is part of the *TOPSwitch* family of power-supply ICs, allows designers to build more cost-effective power supplies without the disadvantages of size and inefficiency inherent in alternatives based on linear and self-oscillating designs. According to Power Integrations, the device allows designers to build 80% smaller and lighter power supplies than linear designs, and 50% smaller and lighter supplies than discrete approaches. Only one external capacitor is needed for compensation, bypass, and startup/auto-restart functions.

The device integrates a PWM controller with a 70-kHz oscillator, and a 700-V n-channel power MOSFET on a single die, allowing it to fit into a standard 8-pin plastic DIP. The chip also contains a high-voltage startup bias circuit, a bandgap reference, and a bias shunt regulator/error amplifier for loop compensation and fault protection. It also includes thermal shutdown with hysteresis circuitry. To assist system integrators with a faster time-to-market, Power Integrations is providing the RD3, a reference design board that's configured as a complete power supply capable of delivering 2-W output (at 5 V dc) from a rectified and filtered ac voltage.

The RD3 provides a number of features specific to standby designs. Besides the 5-V output, it includes a non-isolated, 12-V output that can be used to provide power to the controller of the main power supply. Undervoltage lockout is implemented



by directly sensing the ac line voltage. With this feature, customers may be able to build power supplies that can be reset in less than one second. By replacing a handful of discrete components, the RD3 also can be reconfigured to provide 500 mW or 100 mW at even lower system cost.

The TOP209 switch is in production now and is priced at $0.89 each in quantities of 10,000 units. Samples are available through authorized Power Integrations sales representatives. The RD3 reference board is priced at $25.00 each in single-unit quantities.

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The DS80C323 is not just for 3-volt operation. The DS80C323 is a wide voltage device that can operate from power supply voltages ranging from a minimum of 2.7 up to a maximum of 5.5 volts. Got a system designed for 5-volt operation that you want to move to 3 volts? The DS80C323 can handle the job, both now and in the future.

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Need higher integration? The DS80C323 includes features such as two full-function serial ports, dual data pointers, a watchdog timer, three 16-bit timer/counters, and six external interrupts with three priority levels. Fewer external components saves board space. For further space savings, the DS80C323 is available in a 1.0 mm tall 44-pin TQFP, ideal for PCMCIA, portable, and other space-conscious applications. Other available package options include a 40-pin DIP and 44-pin PLCC.

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While operating from a 3-volt supply, the DS80C323 provides performance equivalent to a 50 MHz 8051. With a maximum clock frequency of 18 MHz and 3x the performance of a standard 8051, the DS80C323 provides processing power previously unavailable in a low-voltage device. It maintains 100% instruction set-compatibility with the original 8051, which means you can upgrade your existing design without throwing away your 8051 development tools.

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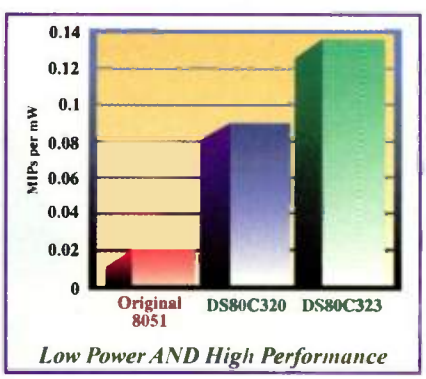

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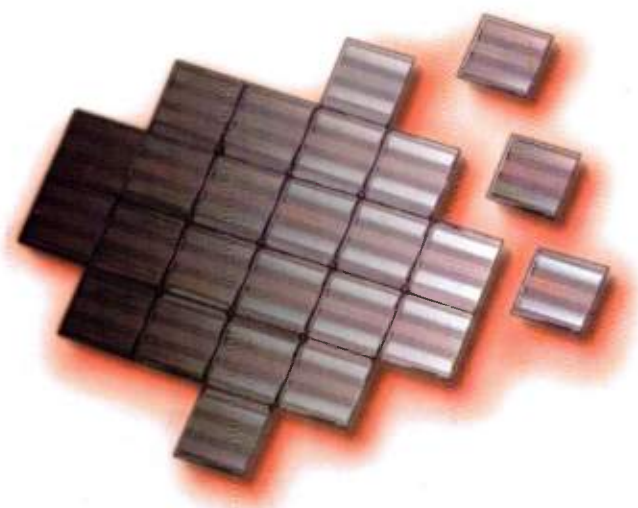

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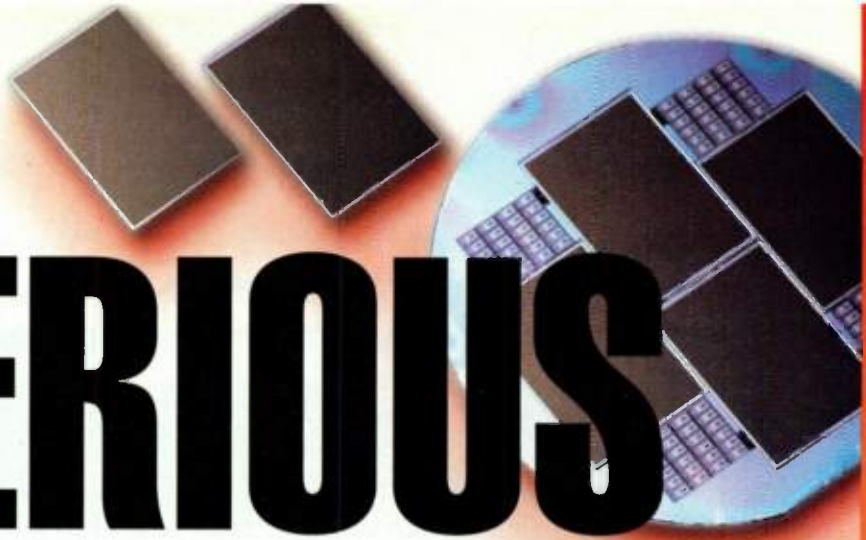

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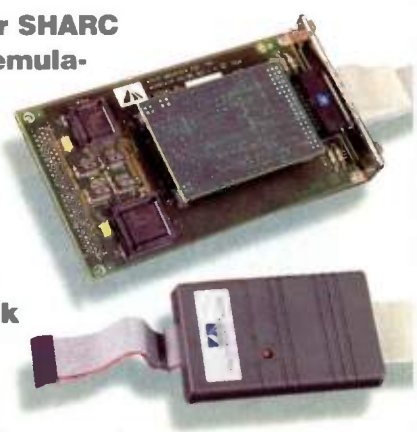

White Mountain DSP offers a full emulation and debug tool set for SHARC development. Another first in the industry, the Mountain-ICE/WS emulation system for Sun workstation platforms (shown) provides complete multi-DSP debugging support for both the ADSP-21060 (4 Mbit) and ADSP-21062 (2 Mbit) SHARC devices. And you know White Mountain DSP will continue to expand its range of options to enable you to work with SHARCs and not get bitten.

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Don't Design DSP Systems In Isolation

To Be Successful, Communications Design Must Account For Real-World RF Effects Like Channel Propagation And Amplifier Distortion.

CARTER SMITH, Hewlett-Packard Co., HP EEsof Div., 5601 Lindero Canyon Rd., Westlake Village, CA 91362-4020; (818) 879-6484; e-mail: carter_smith@hp.com.

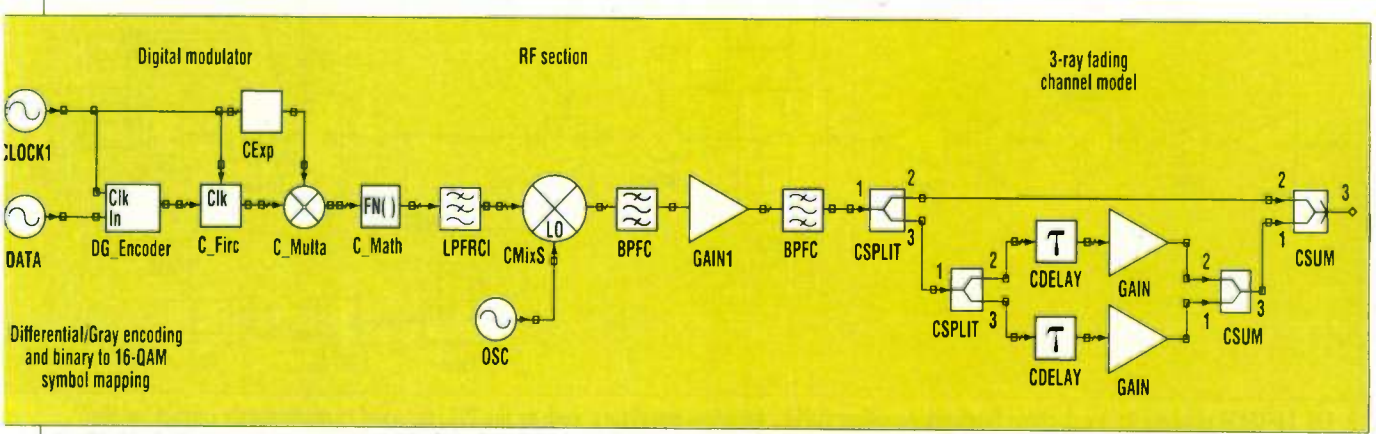
The trend toward higher data rates and increased bandwidth efficiency in today's digital-communications systems places a heavy burden on the digital-signal-processing (DSP) designer. These designers must use their bag of tricks to overcome such problems as RF nonlinearities and fading. Electronic-design-automation (EDA) software can assist the DSP or communications system designer by providing a flexible tool that helps create and optimize designs while also considering real-world RF problems. By mixing digital and RF simulation techniques, DSP designs can be verified in the target RF environment, increasing confidence and reducing design-cycle time. This article will describe the design of an adaptive equalizer for a 16-quadrature-amplitude-modulation (QAM) wireless system. Along the way, you'll pick up tips on avoiding traps and pitfalls during the design and application of DSP in a system that will be affected by real-world RF distortions and problems, such as channel propagation and impedance matching.

Why Consider RF?

Today's communications-system designers are trying to pack more information into less bandwidth by using elaborate modulation schemes. For instance, schemes such as 16 or 256 QAM and code-division multiple access (CDMA) strive to meet many of these goals. However, DSP designers can no longer work in ignorance of real-world RF problems if they intend to implement these bandwidth-efficient modulation schemes in a system and get a working design completed on time. To be successful in modern communications DSP and system design, real-world RF effects such as channel propagation and amplifier distortions must be considered. To demonstrate the interaction of RF distortions and DSP, we'll focus on a digital communications cable link that uses a 16-QAM modulation scheme. However, the concepts discussed in this article are applicable to any system design that uses digital signal processing.

System Description

The data link will be capable of transmitting and receiving data at 20 Mbits per second. It will broadcast in the 500-MHz band and must use only 6 MHz per channel. The system will be tested for proper performance by comparing simulated error rates to the theoretical symbol error rate of 10^{-2}, which is attainable at a signal-



1. This block diagram shows the 16-QAM digital modulator and transmitter with a fading-channel model.

to-noise ratio (SNR) of 15.7 dB without error correction coding. To meet these goals, the proposed system is made up of four basic sections: The DSP modulator, the RF transmitter, the RF receiver, and the DSP demodulator.

The data link's transmitter includes a DSP section, an RF section, and the channel-fading models that will be discussed later on *(Fig. 1)*. The DSP section contains a simulated data source that is first fed into the differential Gray encoder element. This element takes the 20-MHz bit stream, performs differential encoding, and maps the bits to a 16-symbol constellation. The 16-QAM symbols are then fed into a 64-tap raised cosine filter for pulse shaping to minimize system bandwidth.

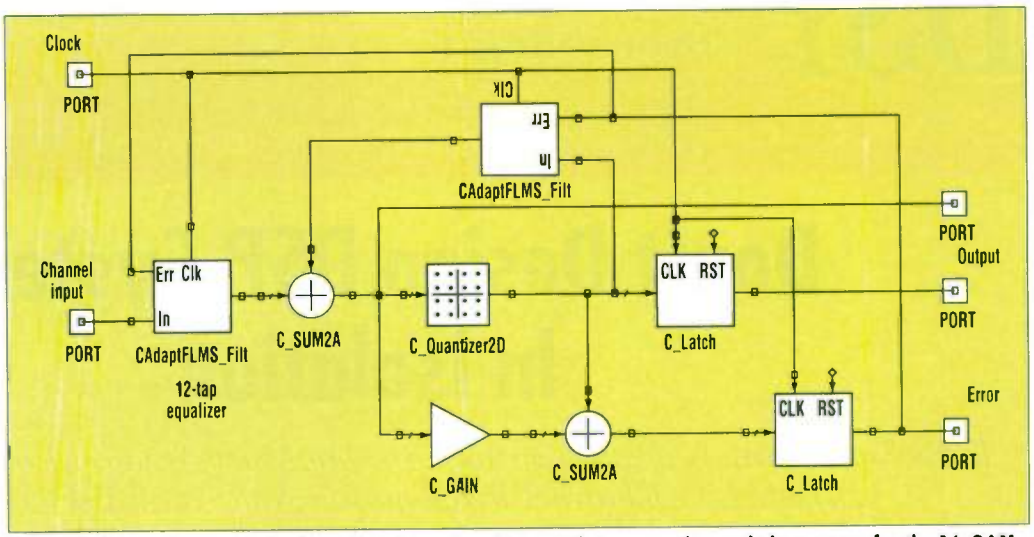
All the pulse-shaped 16-QAM symbols are then frequency-shifted from baseband to a 5-MHz IF using a DSP complex-multiplication process. The digital signal is then low-pass filtered to eliminate digital aliases. It's now ready for the RF section of the transmitter.

At this point, the RF transmitter section accepts the 16-QAM signal that has been frequency shifted to 5 MHz, shifts it to 500 MHz, and transmits it with enough power to meet symbol-error-rate requirements. The RF transmitter chain uses a standard sequence of mixer, filter, amplifier, filter to achieve this. Specifications for these components must be watched carefully as 16-QAM systems are very sensitive to phase noise (more on this in the RF section).

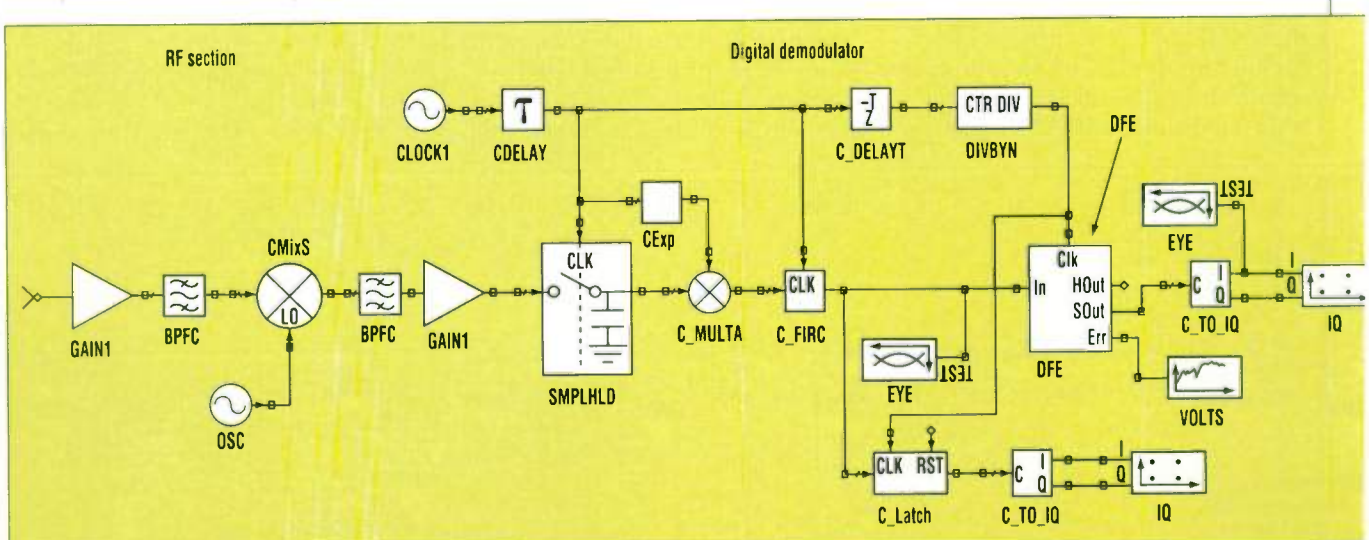
Our system also uses a standard RF receiver chain, which is mentioned in this article to illustrate how the chain distorts the digital signal. The RF chain downconverts and filters the signal and presents a 5-MHz 16-QAM signal to the input of the receiver's DSP section.

Next, the DSP section of the receiver samples the signal and band shifts it from 5 MHz back down to baseband. This baseband signal is then fed to a 64-tap FIR pulse-shaping filter to recover the original 16 QAM unshaped symbols. The unshaped, but channel distorted symbols are then fed into the decision feedback equalizer *(Fig. 2)*.

We use the decision feedback equalizer because the environment for our 16-QAM system is rich in multipath transmission problems. Multipath, or the reception of multiple signals at different amounts of transmission delay (time dispersion), causes a comb filtering effect that varies with time. Adaptive equalizers, such as the decision feedback



3. A well-designed and optimized equalizer is employed to greatly improve the symbol error rate for the 16-QAM wireless system. This diagram shows the system's decision feedback equalizer.



2. The 16-QAM receiver uses a decision feedback equalizer (DFE). Adaptive equalizers, such as the DFE, are used to continuously correct for the frequency-response distortions that are caused by multipath distortion.

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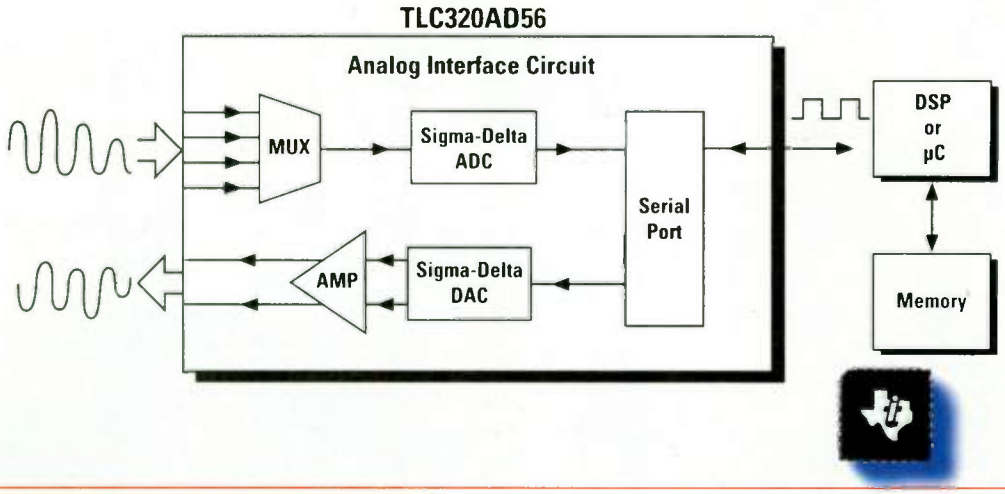

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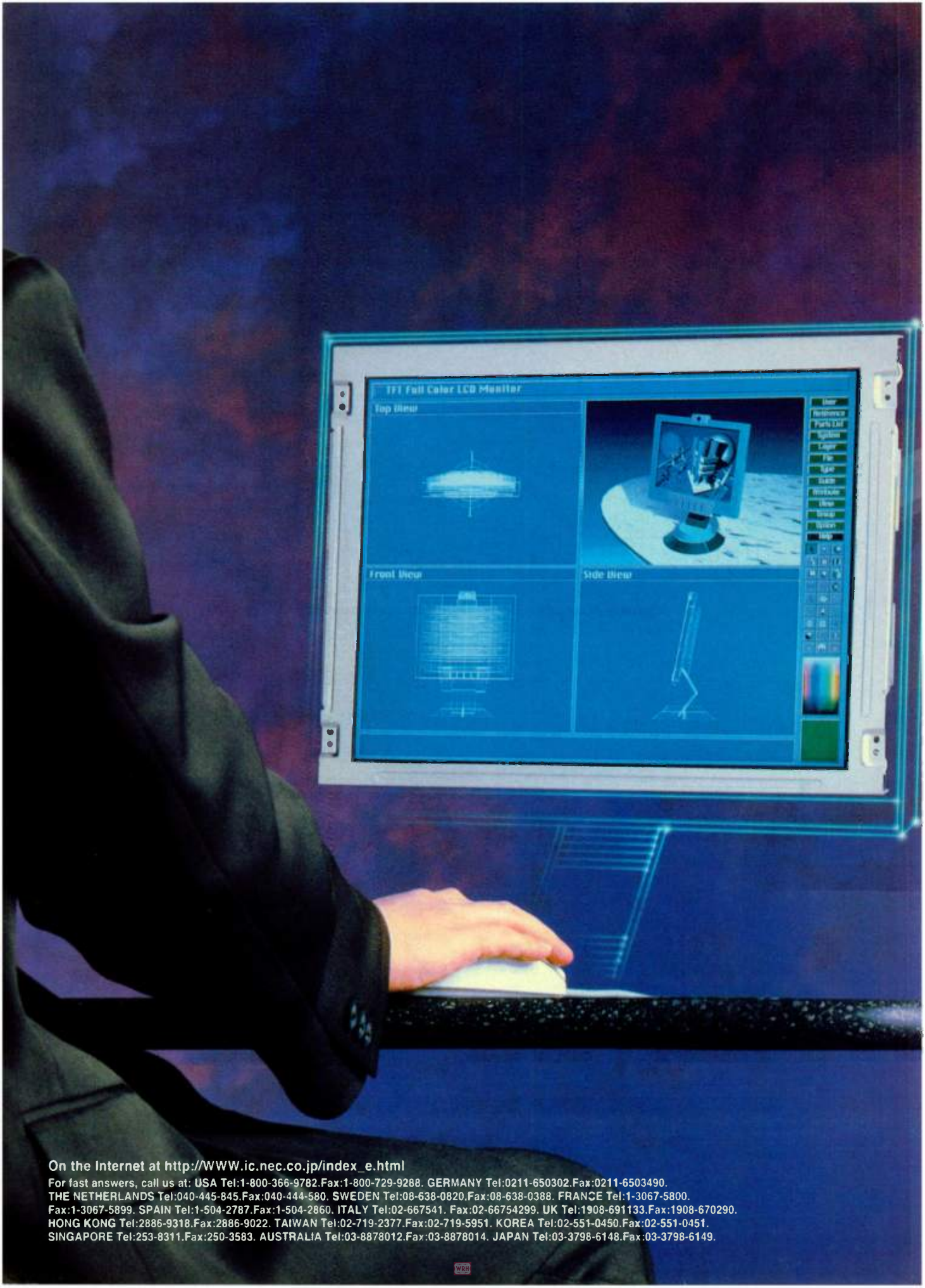

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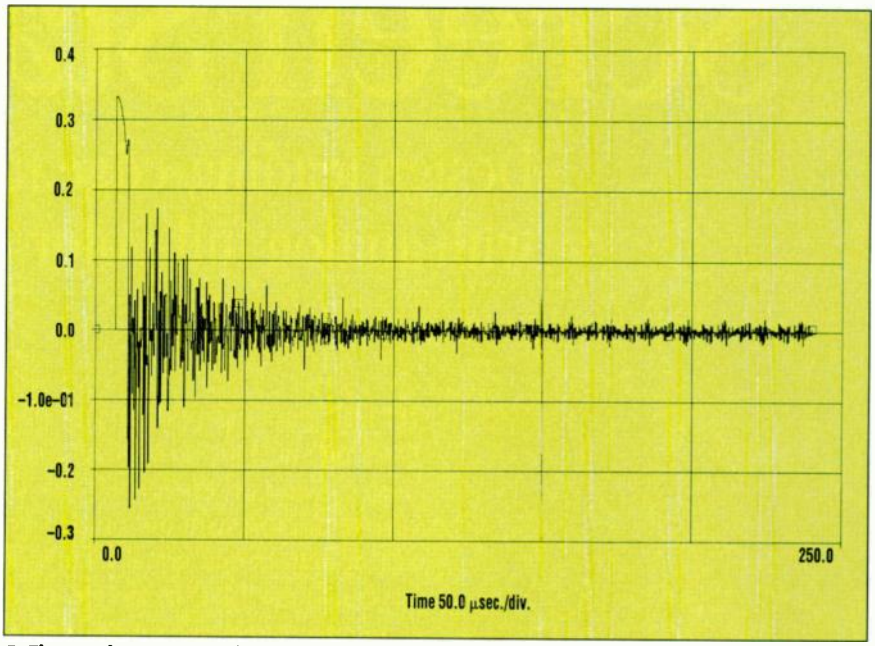
equalizer, are used to continuously correct for the frequency-response distortions that are caused by multipath. Each tap of the equalizer can be adaptively adjusted to minimize the frequency distortions, and thus inter-symbol interference, that is introduced in the RF and propagation channels. Further details on the operation and optimization of the equalizer are given in the equalizer sections of this article.

Now that the 20-Mbit/s communication system has been defined, we'll describe the decision feedback equalizer and discuss some of the pitfalls of the RF channel before getting into the actual optimization of the DSP design.

Equalizer Background

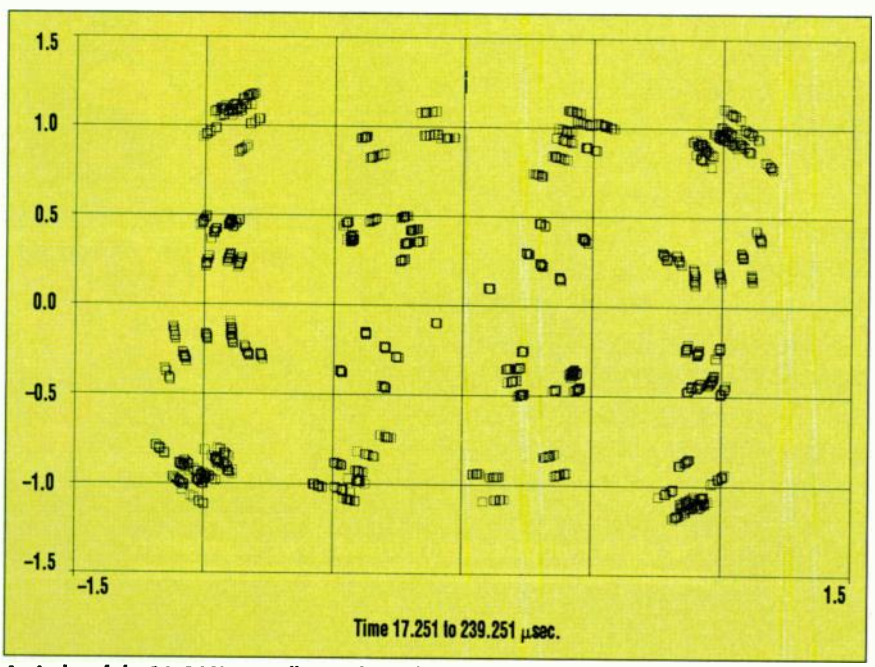
As previously stated, equalizers are needed in digital-communications systems to minimize the distortions caused by phenomenon such as time dispersions or frequency translation. When time dispersion occurs in a modern bandwidth-efficient communications system, the effects of a data symbol can extend well beyond the data symbol period in the form of ripple. This causes the symbols to overlap and interfere with each other, and is known as inter-symbol interference (ISI).



5. The equalizer must settle to a mean-square error (MSE) of less than 0.08 VRMS in a time period of less than 40 ms. This plot shows the DFE's mean-square-error voltage versus time.

Adaptive equalizers are commonly used in bandwidth-efficient digital communications systems to correct the ISI caused by time-varying dispersion in the propagation channel. Adaptive equalizers use a transversal or tapped delay line with the delay spacing equal to the symbol time interval.[1] This symbol spacing interval for the taps allows the equalizer to try to force the interference from other symbols to zero at the sample points. These linear transversal equalizers, as they are known, are combined with an algorithm to control the tap coefficients, which is based on minimizing the mean-square error.

The combination of the transversal equalizer, and the above mentioned mean-square-error minimizing coefficient algorithm, is known as a least-mean-square (LMS) equalizer. The LMS equalizer, the workhorse of adaptive equalizers, forms the basis for an improved ISI canceling equalizer known as the decision feedback equalizer (DFE).



4. A plot of the 16-QAM constellation shows fading, timing errors, phase noise, and RF-distortion effects The effects of the phase noise can be seen in the way the constellation has a rotational smearing of the symbol points

Decision Feedback

The DFE is used to correct such problems as frequency-dependent amplitude and multipath distortion that lead to inter-symbol interference. A well designed and optimized equalizer is employed to greatly improve the symbol-error rate for this 16-QAM cable system.

A DFE is chosen due to its ability to correct severe amplitude distortion problems while also canceling inter-symbol interference. Compared to a standard linear equalizer, the DFE can compensate for amplitude distortions with much less noise and less sensitivity to symbol phase off-

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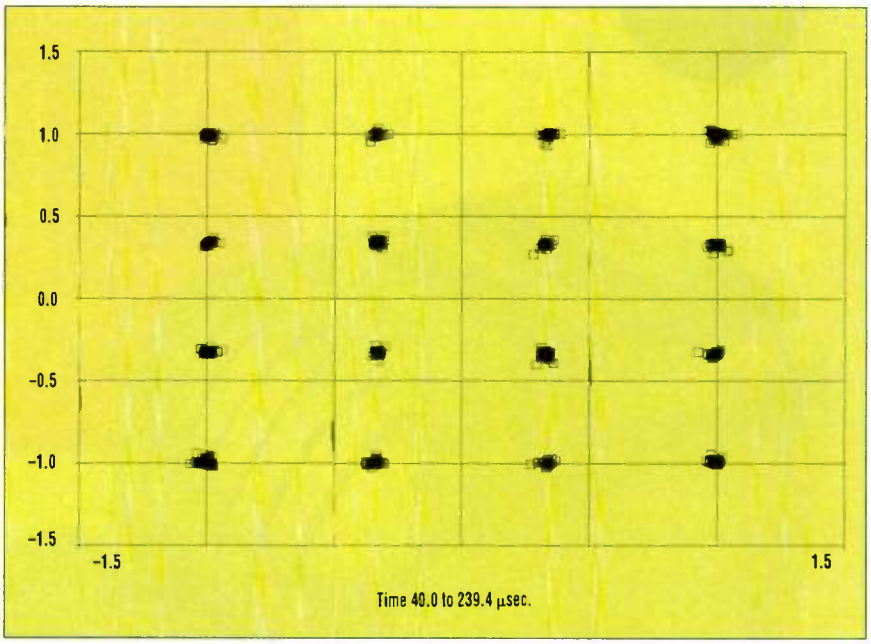
sets. Output from the DFE is the sum of the outputs of the forward and feedback portions of the equalizer. The forward filter is simply a standard linear transversal equalizer *(Fig. 3)*. Feedback travels through a linear transversal filter that uses the decisions made as its input data.

The equalizer functions as follows: If the value of the past symbol decisions are known and assumed to be correct, the ISI can be canceled exactly by subtracting the ISI contributed by these symbols using the appropriate weights in the second linear transversal filter. Filter coefficients for the forward and feedback filters are continuously adjusted in a control loop to minimize the mean-square error of the filter output.

Once the choice of a DFE is established, the designer must choose which algorithm will automatically update the filter coefficients. There are a number of faster algorithms that have been developed in the years following the original development of the LMS algorithm. These filter-coefficient calculation algorithms cause the equalizer to converge faster in environments where there is rapid variation in time dispersion, such as mobile wireless. Fast convergence algorithms include: Kalman, fast Kalman/fast transversal, and the recursive least squares (RLS) lattice. While these algorithms are all much faster at converging than the LMS, they also require significantly more calculations per tap adjustment iteration, and use up a lot more processing time. In addition, the RLS algorithms have a tendency to diverge when implemented in finite precision arithmetic.[2]

A high throughput rate is needed for this receiver, thus the signal-processing algorithm will be implemented in an ASIC. The least mean square (LMS) gradient algorithm is chosen for its relatively quick settling time, its stability, and its low computation overhead.

The LMS algorithm in the DFE filter requires the choice of a number of parameters, such as the coefficient calculation step size, the number of taps in the equalizers, and the word width. The 16-QAM receiver will be simulated to explore the DFE parameters and refine a solution that is cost and power efficient while meeting performance specifications in a RF-distorted environment.



6. A clean constellation diagram and an excellent BER are indications of the system's performnace. This diagram shows the constellation after equalizer correction of RF distortions.

RF Channel Modeling

In order to test and optimize the DFE portion of the 16-QAM receiver, it's first necessary to build up the analog sections of the design in the design tool. Figure 1 shows a 500-MHz transmitter with a propagation channel model. Simulation software (such as the OmniSys Design Suite from HP EEsof) allows analog-distortion effects to be added to the analysis of each block model to make the entire system reflect the real-world environment that the equalizer will be placed in.

These distortion effects include phase noise of the local oscillators, power amplifier nonlinearities, circuit voltage standing wave ratios (VSWRs), and filter nonlinear phase characteristics. The designer also should add accurate models for the antenna and propagation channel in order to take into account such channel distortions as frequency-selective fading and multipath distortion (which are present in real digital communications systems). Taking care to use accurate RF and channel modeling in simulations gives the DSP designer an additional tool to improve performance and eliminate problems before more costly hardware prototyping and testing begins.

RF Parameters

While there are a large number of RF parameters that one can play with in a simulation, it's important to focus on the parameters that have the greatest effect on your system. Try to include only the distortions that are most important because each distortion requires longer simulation time. In a QAM system, or any system that contains information in both the phase and the amplitude of the signal, it's most important to consider compression points on the amplifiers, phase noise, and multipath. These distortions have the biggest effect on a QAM system's performance.

There are amplifiers in any communications system that transmits over an RF channel. Unfortunately, amplifiers don't have unlimited amplifying capability. Every amplifier will run out of gas at some point and start clipping or compressing the signal. Compression and distortion are modeled using the 1-dB compression point and the third-order intercept point. The third-order intercept specifies a theoretical point where the amplifier's fundamental output intercepts the third-order distortion

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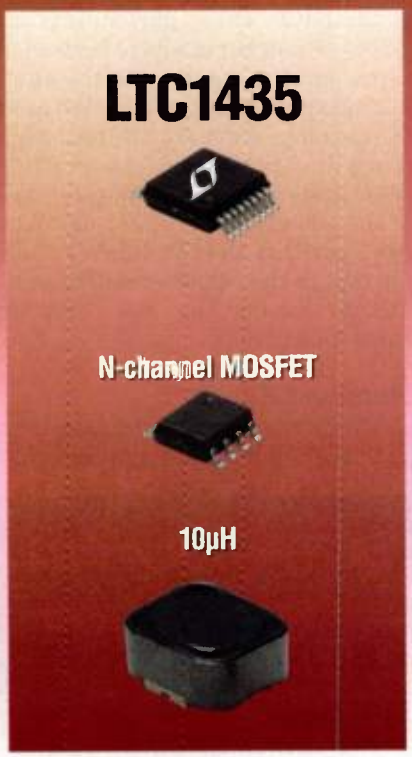

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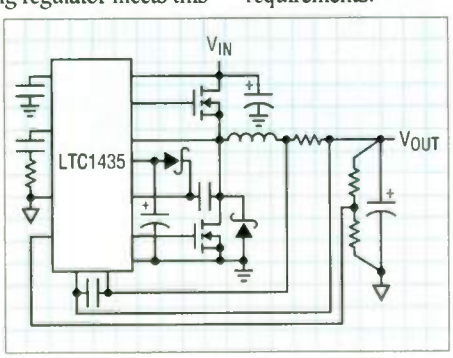

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products. The effects of the amplifier's third-order incept and 1-dB compression point should be included in simulation when designing DSP communications algorithms to avoid unexpected performance problems when the first prototype is built.

All oscillators in RF systems have phase noise. Essentially, phase noise is very small amounts of phase modulation on the oscillator that creates a "modulation envelope" rather than the theoretical single frequency that is expected. Excessive phase noise can raise havoc with any digital communications system that uses phase to transmit data, including the 16-QAM system being discussed in this article.

Low-phase-noise oscillators can be used to avoid this problem, but they tend to be much more expensive than their higher-phase-noise cousins. The simulator can do a system-trade-off study of the lower cost of using a higher-phase-noise oscillator versus the increased signal processing that may be necessary to still meet error-rate requirements. The oscillators used in the upconverter and downcoverter in the RF sections of our system will be set to a phase noise value of –65 dBc/Hz at 3-kHz offset. This value represents a typical oscillator for this type of application. The effects of the phase noise can be seen in the way the constellation has a rotational smearing of the symbol points *(Fig. 4)*.

The final RF distortion that should always be considered in any wireless or wired digital data link is multipath. Multipath causes intersymbol interference, and can therefore cause your system to fail symbol error-rate requirements. In our simulation, a propagation model is added to test the equalizer's capability to correct for time dispersion problems, thus cancelling ISI.

Including these three key RF distortions in our analysis will give us better results when we finally build a prototype. Figure 4 shows the RF distorted signal that is fed to our receiver to test and refine its performance. Simply seeing the distortion in these plots tells us that this will affect the receiver's performance, and it does. It's crucial to take the time to correctly model these RF distortions if you are to get a prototype that works in real-world conditions.

Design Optimization

With the system block diagram completed and the proper RF distortions added in, the EDA tool can now be used to optimize the parameters of the DFE. These parameters include the number of bits to be used to represent the numbers or the number of taps in the equalizer. We used the OmniSys software for the design described in this article. For our QAM system, values for the step size of the equalizer coefficient-calculating algorithm and the number of filter taps in the equalizer will be optimized based on the system simulation results.

Number Of Taps

The first step in simulating is to get your algorithms running using floating-point numbers. After the system is running, we perform a symbol error-rate check on a receiver that uses an equalizer with a large number of taps. This gives a theoretical best case to make sure it's possible to meet system specifications. This best case also will be used as a starting point for taking taps out of your equalizer to minimize implementation cost.

Excessive phase noise can raise havoc with any digital communications system that uses phase to transmit data, including the 16-QAM system being discussed in this article.

To determine the minimum number of taps we can use, we decrease the number of taps and re-simulate to check the symbol error rate. After iteratively simulating a number of times, it's determined 12 taps are sufficient to meet a symbol error rate of $10^{-1.54}$ at 15.5 dB SNR (without error correction). This compares favorably with the symbol error rate that's theoretically possible (10^{-2}) without the multipath, phase noise, and other RF distortions that we added to the model. Note that we expect a slight performance degradation when we implement the equalizer using fixed-point numbers in the actual system hardware.

Step Size

Each of the LMS equalizers contained in the DFE requires that a step-size coefficient be set. The larger the value of this coefficient, the quicker the equalizer converges on its proper setting. Smaller step sizes take longer to converge or settle, but have lower residual error. The step size for the LMS gradient-filter-coefficient calculation is now varied to determine its effect on the DFE's performance. This 16-QAM system won't provide a training mode to the receiver, and thus we need the equalizer to settle to a mean-square error (MSE) of less than 0.08 VRMS in a time period of less than 40 ms. The plot of the MSE shows the equalizer settling and demonstrates that with a step size of 0.009, the equalizer will meet the requirements *(Fig. 5)*.

Further simulation reveals that while this large step size will meet the initial settling criteria, the steady-state mean-square error remains at an unacceptably high level due to the large step size. Simulation also shows that a secondary step size of 0.002 will give the lower steady-state MSE that's needed. This second step size will be loaded into the equalizer after initial settling is completed in order to achieve both a quick settling time and a low steady-state MSE.

Word Length

With the equalizer functioning properly and meeting bit error-rate requirements, the finite word widths can now be considered. Word widths must be minimized to lower the cost and power consumption of the final DSP design. The design-automation

software can be used to automatically optimize the word width and check for the effects it has on the bit error rate. Simulation helps achieve an acceptable compromise between bit error rate and cost. The performance of the final system is demonstrated by an excellent bit error rate and a clean final constellation diagram despite the distorted constellation diagram that the receiver must process *(Fig. 6)*.

EDA software capable of mixed-signal simulation was shown to be highly beneficial in exploring the application and optimization of a DSP-based decision feedback equalizer with the presence of RF nonlinearities and propagation distortions . Through the use of system-level simulation, we selected the proper values for the number of taps and step size.

In addition, we met the BER performance requirements while minimizing the required cost and power of the design (example is available upon request). Considering analog and RF effects during the design and simulation of a baseband communications digital signal processor helps avoid many of the traps and pitfalls that often show up during hardware-prototype testing, resulting in the shorter development cycles that are a must in today's competitive communications market.

Carter Smith, a product manager with HP EEsof, specializes in communications system simulation and DSP. He received a BSEE and MSEE from California State Polytechnic University, Pomona. Carter is a registered professional engineer in the state of California.

References:

1. Lucky, R.W. , "Automatic Equalization for Digital Communication," The Bell System Technical Journal, April 1965, p 547- 588.

2. Qureshi, Shahid U.H., "Adaptive Equalization," Proceedings of the IEEE, Volume 73, No. 9, September 1985, p 1349-1387.

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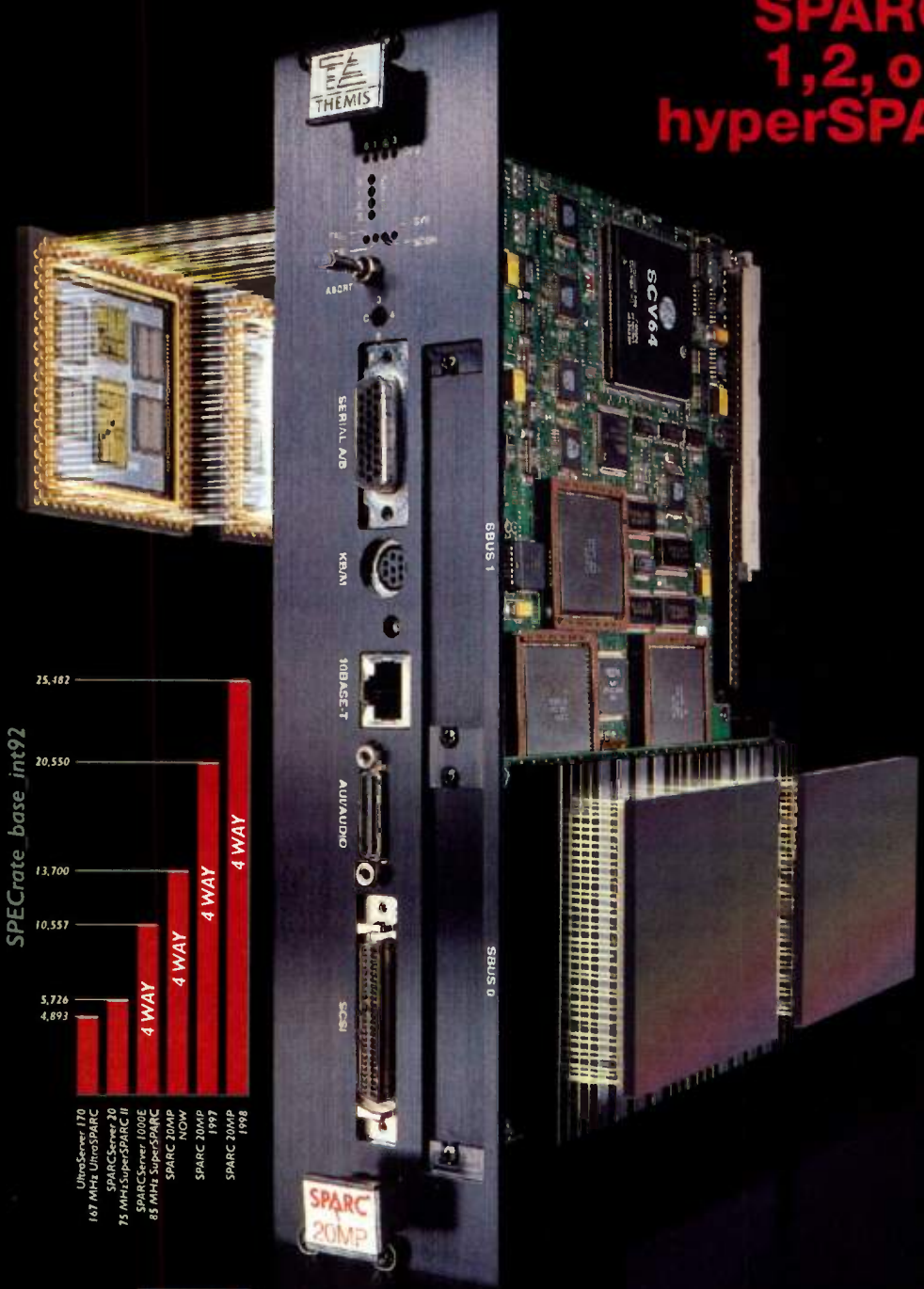

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Considerations For Upstream Channel Communications In CATV Systems

Understanding The Upstream Channel's Challenging Environment Is The Key To Building Robust Interactive Cable Networks.

Bruce Currivan and Bill Xenakis,

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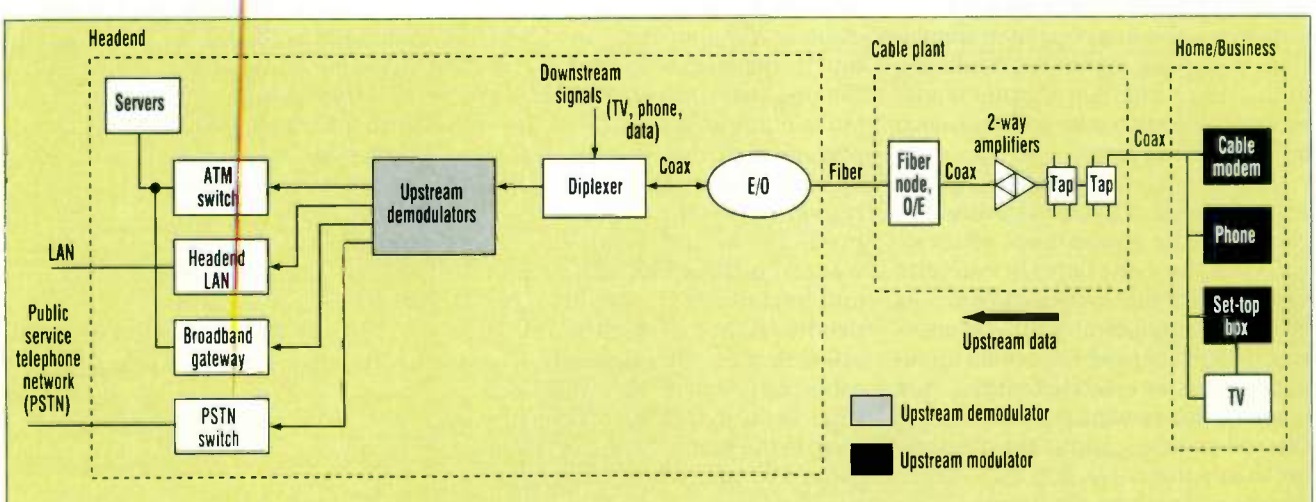
The cable television (CATV) industry is looking eagerly toward providing two-way, interactive communications over CATV networks. Potential applications include computer networking, Internet access, telephony, interactive multimedia, and entertainment such as video-on-demand. As a result, cable plants are being upgraded with hybrid fiber/coax (HFC) technology and two-way capability. Depicted is the upstream or reverse path in a typical HFC network (*Fig. 1*).

Broadcasting downstream to the home is straightforward (in relative terms) since CATV systems were originally designed for high-fidelity downstream transmission. The channel is relatively quiet, bandwidth is abundant (54 MHz up to 600/750/1000 MHz), and broadcasting permits continuous rather than burst transmission. However, some problems remain. For example, changing the channel on a TV or VCR can alter the multipath distortions in the downstream channel as seen by the cable modem in the same household.

Perhaps the greatest challenge for interactive services is the upstream channel from subscribers to the headend. The upstream funnels digital data and noise from tens, hundreds, or even thousands of subscribers over narrow bandwidth (5 to 42 MHz) to a single point. Burst modems, which are more complex than continuous modems, are needed to transmit packets in the time-shared upstream channel.

Upstream Impairments

The IEEE P802.14 LAN/MAN Standards Committee is developing a channel model that will permit designers to evaluate the performance of various CATV modulation techniques (*Fig. 2*). This article describes the channel model and how it is being applied to develop communications equipment for the upstream channel. The channel model is oriented in terms of signal-processing blocks



1. A typical bidirectional cable system consists of a headend, a cable plant, and a group of end users. Bidirectional systems differ from conventional cable systems because they have 2-way amplifiers in the cable plant to support traffic between the interactive services in the headend and the cable modems located at the subscriber's premises.

that act upon the subscriber signal as it travels toward the headend. The most serious problems, which are common to all modulation techniques, are ingress and impulse/burst noise.

Ingress—interference picked up by the antenna-like properties of the cable system—is caused by poorly constructed drops, connectors, and improper terminations. As a result, noise from radio transmissions and environmental RFI (e.g., motor noise) is amplified and transmitted along with the desired digital signal. A large number of narrowband sources, such as AM radio stations and CB radios can be identified on a spectrum analyzer plot of the upstream with no user signals present *(Fig. 3a)*. When a network of 37 time-division multiple-access/frequency-division multiple-access (TDMA/FDMA) user data signals is turned on, the signal-to-noise ratio (SNR) is still high enough to permit reliable QPSK data transmission *(Fig. 3b)*. The middle signal is left off to allow observation of the noise floor, including intermodulation products.

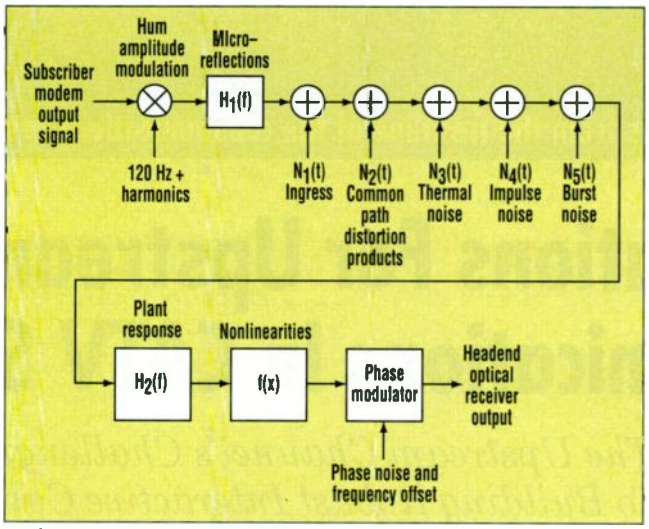
For the purposes of this study, a simple model for ingress has been developed which consists of a FIR filter with multiple narrowband resonances (spectral peaks) *(Fig. 4)*. When the filter is excited by white gaussian noise in a computer simulation, each peak fluctuates randomly, emulating a number of radio transmitters sharing a narrow band, such as a shortwave band.

Impulsive noise typically results from several sources: Corona discharges from power lines, often located on the same poles or conduits as the CATV cable; discharges across corroded connector contacts; automobile ignition; and household appliances, such as electric motors. It is modeled as a random periodic train of filtered impulses. Burst noise is similar to impulse noise, but with longer duration of each event. Burst noise is modeled as gated, filtered, additive white gaussian noise.

Microreflections are generated at every interface along the cable, where discontinuities cause part of the signal energy to be reflected. Robust waveforms such as binary phase-shift keying (BPSK) and quaternary phase-shift keying (QPSK) are forgiving of these microreflections below about 1 to 2 megasymbols/s. More complex waveforms such as quadrature amplitude modulation (QAM) are less robust and may require equalization.

Nonlinearities in amplifiers, the laser transmitter in the fiber node (considered the dominant effect), and the laser receiver in the headend limit the useful dynamic range of the channel. The amplifier can be driven into its nonlinear operating region in the presence of strong ingress or impulse/burst noise, or when allocated power constraints are not respected by users. Operating in its nonlinear region causes the amplifier to compress the signal, resulting in unwanted intermodulation products and harmonics. To avoid spurious products that may interfere with other services sharing the upstream cable plant, one of the evaluation criteria for design of the upstream protocol is the minimization of collisions caused by many users transmitting simultaneously.

Unintentional rectifiers in the cable system, caused by corroded connectors, for example, create common-path distortions. Downstream signals are demodulated by these junctions and reflected into the upstream channel. The model for common-path distortion is similar to the model for ingress.



2. This upstream channel model illustrates the common sources of distortion and interference found in bidirectional hybrid fiber-coax systems. It can be used to understand the phenomena behind signal degradation and to evaluate the performance of proposed upstream modulation techniques.

Phase noise and frequency offset most often occur in frequency-stacking multiplexers found in some return-path systems. Phase noise also may occur in laser cavities, but at a less significant level, and is produced in the subscriber and headend modem oscillators. It is modeled as filtered and integrated gaussian noise modulating the carrier phase.

Hum modulation is amplitude modulation caused when ac power is coupled through the system's power-supply equipment onto the signal envelope. This primarily affects QAM systems, which must track out the hum, whereas QPSK-based networks are relatively unaffected.

The equipment in the cable plant contains linear filtering elements that also affect the upstream signal. These effects are dominated by the diplex filters that separate upstream from downstream frequencies.

Choosing Access Techniques

TDMA is the preferred multiple-access technique for upstream transmission because of its high channel capacity and the fact that a single receiver can receive data from hundreds of subscribers. In order for a TDMA system to achieve near-theoretical capacity, the overhead time between burst transmissions must be minimized. This means spacing the subscriber signal bursts closely together and minimizing each burst's overhead (acquisition preamble, interburst gap, etc.).

QPSK (with option for 16-QAM) has become the preferred modulation format for the first generation of upstream-channel technologies because it is robust and economically sensible to implement.

High Performance Required

It is clear that meeting the requirements of the upstream-channel

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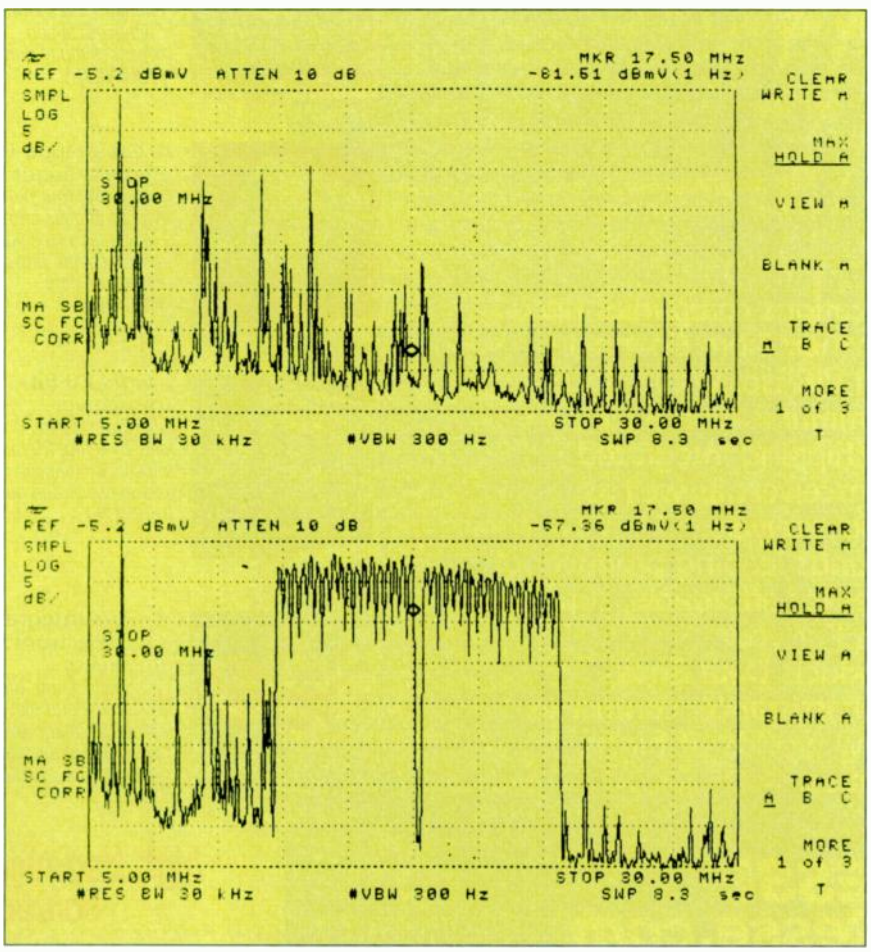
model requires a high-performance modem along with a high-performance multiple-access technique. Utilizing TDMA, with each subscriber transmitting only during a specific time slot, calls for a burst receiver with extremely fast signal acquisition that requires minimal spacing between bursts. Shown is an example of a test signal used in modem development to demonstrate the ability to receive closely spaced bursts (2-symbol inter-burst gap) with widely varying amplitudes (12-dB difference) *(Fig. 5)*. At the subscriber end, the transmitter, or modulator, must be able to support the precision burst timing control required in TDMA systems.

In addition to TDMA, FDMA is used to support multiple channels simultaneously in the upstream. In one recent test, 18 independent QPSK/TDMA/ FDMA channels were found to easily coexist with each other, even when one channel was 10 or more dB lower in amplitude than its neighbors

High performance necessarily means digital implementation. Advances in semiconductor technology have brought down the size, power consumption, and cost of digital components to the point where digital equipment has a distinct advantage. A digital receiver system that would have required an entire rack of equipment 10 to 15 years ago can now be implemented on a single silicon chip with a few peripheral analog components.

Similarly, while analog techniques used at the modulator for generating a QPSK or QAM modulated carrier are low in parts cost, they require critical adjustments during manufacture (and sometimes in service) to provide good performance. Digital modulators provide essentially perfect phase and amplitude balance, with no adjustments. They also can be agile in frequency with virtually instantaneous switching times.



3. Upstream ingress as actually measured on a spectrum analyzer at a typical headend is shown (a). In (b), a network of 37 signals is shown running successfully on top of the ingress noise using QPSK modulation.

Implementing The Technology

A standard board-level QPSK headend receiver provides robust performance in the presence of impulse noise and other channel degradations. The carrier phase-locked loop (PLL) normally used in the demodulator is replaced by a portion of an ASIC which performs the digital approximation of a PLL, but without the normal feedback loop. This function requires near-zero acquisition time, thus achieving coherent performance without having to wait for the loop to settle.

Performance results typically have deviated 1.5 to 2 dB from ideal coherent continuous theory at BER = 10^{-6} (there is no accepted "burst theory"). Multiple symbolrates (0.25 to 4 Msymbols/s) have been adopted by the IEEE 802.14 Standards Committee for users to optimize the use of the limited upstream bandwidth. A narrow-bandwidth (low-bit rate) signal may be selected in order to utilize a narrow "clean" portion of the cable spectrum, or for inherently low-bit-rate applications, such as pay-per-view ordering.

The companion component is a modulator on a single chip that can operate in either burst or continuous mode—for transmitting digital video, telephone, and data signals from the subscriber to CATV headend equipment *(Fig. 6)*. The combination offers 0.5 to 5 Mbits/s upstream that can support consumer web pages, interactive graphics, and other equally demanding applications for a large geographical user neighborhood.

Shaping Forces

In designing cable equipment for the upstream channel, both industry forces and cable channel characteristics must be considered. The following is a summary of key industry drivers and how they affect design of equipment.

• *A standard for CATV modulation format has not yet been established.* Implementing the equipment with QPSK provides an economical, inher-

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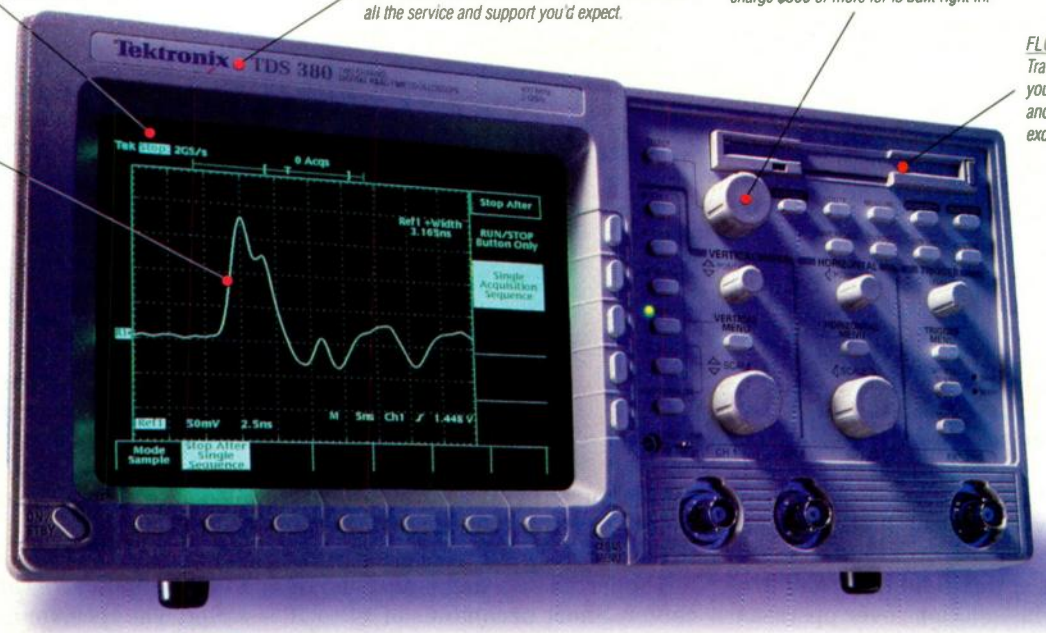

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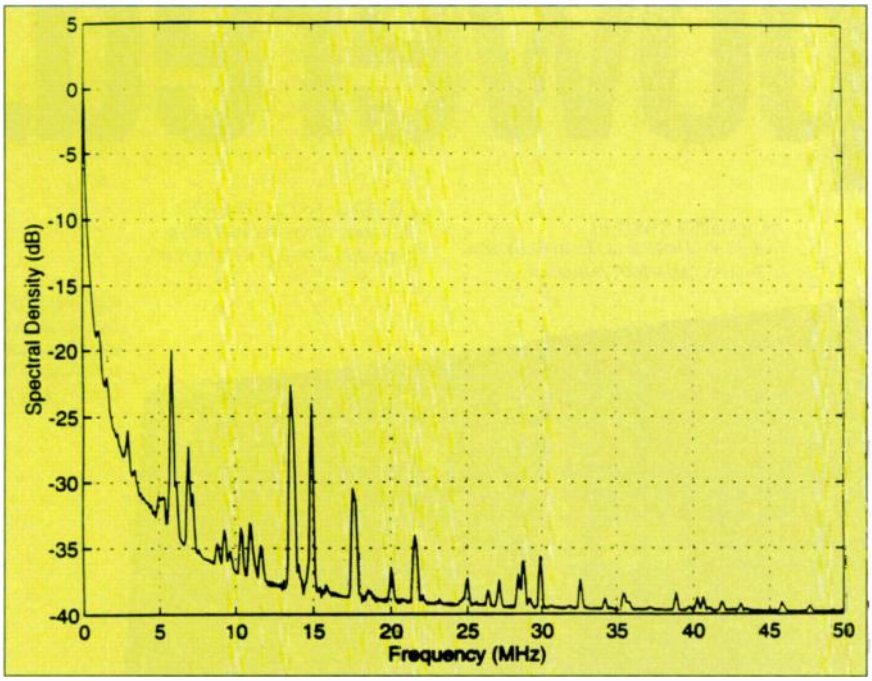


4. The spectral peaks shown in this filter's response can be used to simulate ingress noise.

ently robust format that has been proved over the years in the demanding environment of satellite communications and in field tests and preliminary installations over upstream HFC systems. QPSK has been selected by the Digital Audio-Visual Council (DAVIC) as the upstream modulation format. While the standard has not been released yet, QPSK (or 16-QAM) is the current selection as the IEEE 802.14 standard.

• *No standard exists yet for the medium access control (MAC) layer.* This is the standard governing shared media like TDMA and FDMA. By providing a programmable burst length, the equipment will be able to handle future transmission schemes, such as ATM, which requires 53 bytes plus overhead per cell, as well as Ethernet packets, which can be over 1500 bytes long.

• *A high upstream data rate is needed.* The equipment is able to transmit and receive data at the rate of 0.5 to 5 Mbits/s using QPSK.

• *Limited upstream bandwidth is available.* One solution to this problem is to use root-raised-cosine band-limited pulse shaping, which permits subscriber channels to be put very close together with great accuracy. Digital transmission means a very low level of spurious signals are transmitted. Short guard times between bursts and fast acquisition times are factors that relate directly to the number of subscribers who can be supported by a single-headend receiver. Short preambles of 14 to 16 symbols have been shown to be effective for synchronizing on a particular upstream channel.

• *Very low subscriber cost is needed.* Service providers measure costs per subscriber. By basing designs on emerging standards and by implementing a high level of digital integration, equipment costs can be kept low. The single-chip modulator uses 3.3-V CMOS technology for low-power applications such as line-powered, side-of-the house network interface units, and to reduce the cost of set-top boxes.

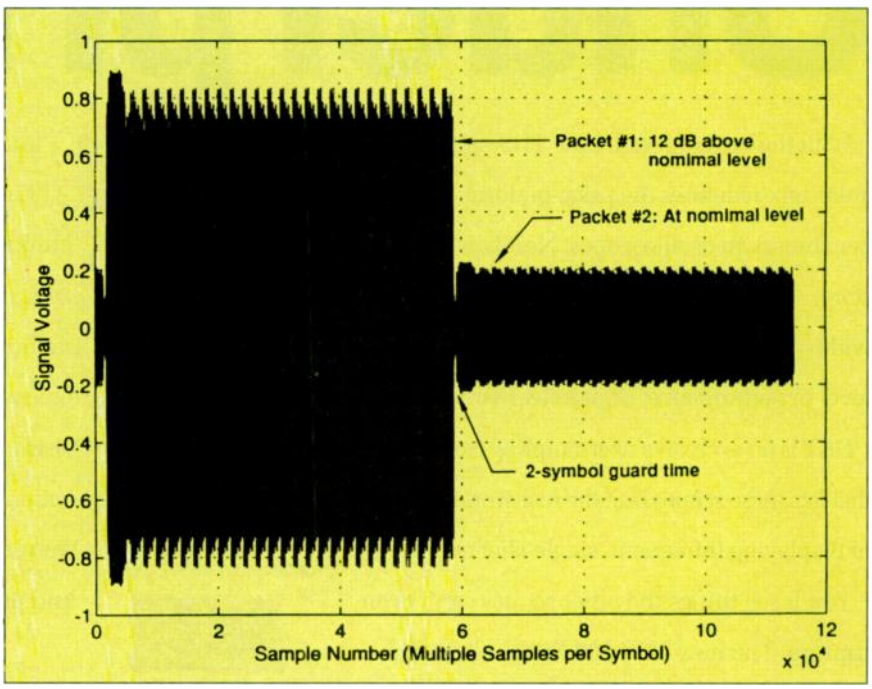
• *Cable plant characteristics vary widely.* A combination of equipment robustness and cleanup of the plant is needed to realize the potential of HFC broadband communications. As industry standards evolve, guidelines for acceptable channel impairments will likely be agreed upon in conjunction with requirements on equipment performance.

Channel Characteristics

The physical characteristics of the sub-split band also play an important role in shaping the design of a cable modem. Some of the more important factors include:

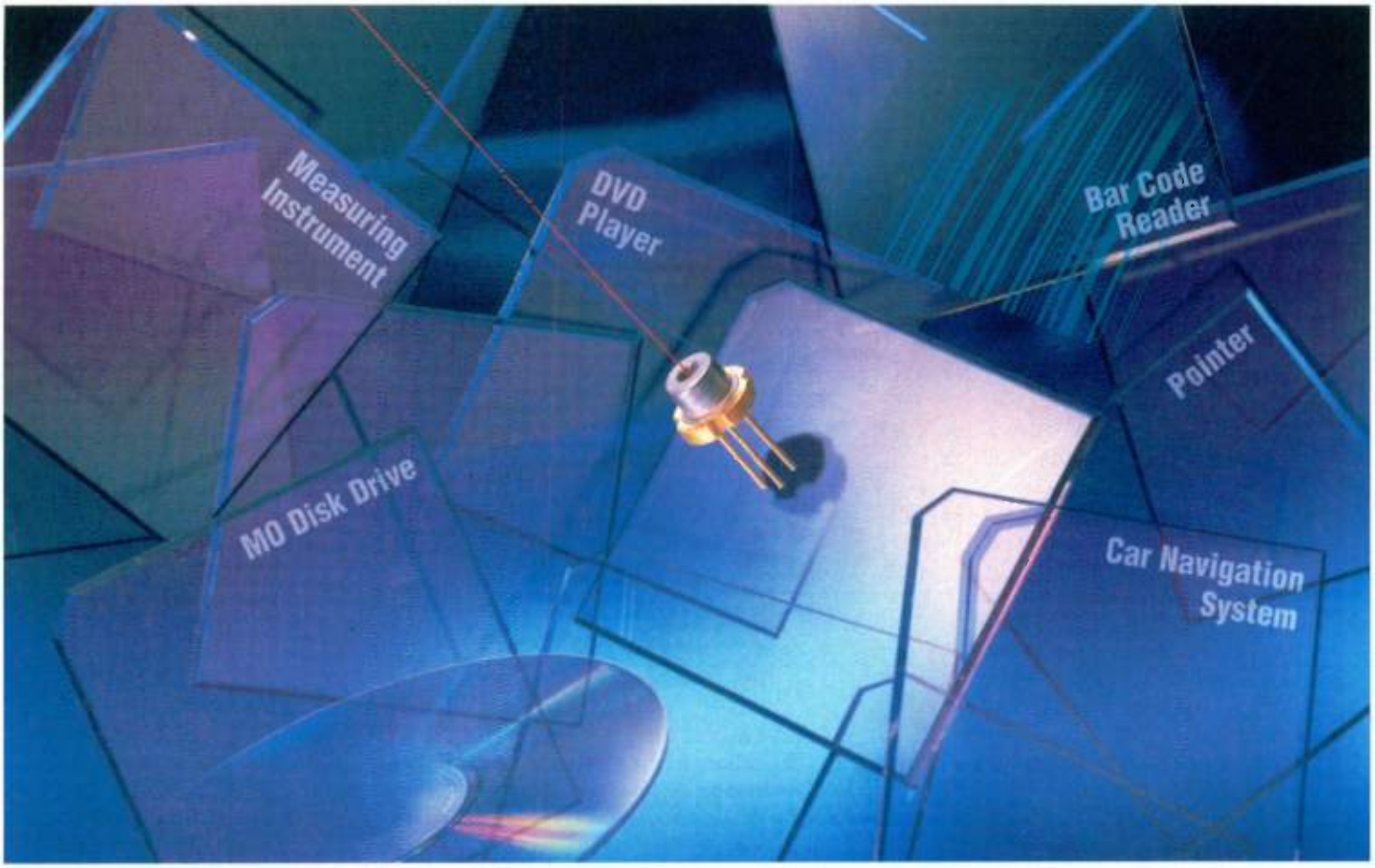
• *Extended subsplit frequency range.* The receiver and transmitter operate in the 5-to-40-MHz (in some cases 6-to-65 Mhz) carrier frequency range for flexibility.

• *Narrowband ingress.* By providing frequency agility, that is, the ability



5. A properly designed demodulator can receive packets with greater than 10-dB level difference and only 2 symbols of guard time between them.

Bright ideas for every shade of red



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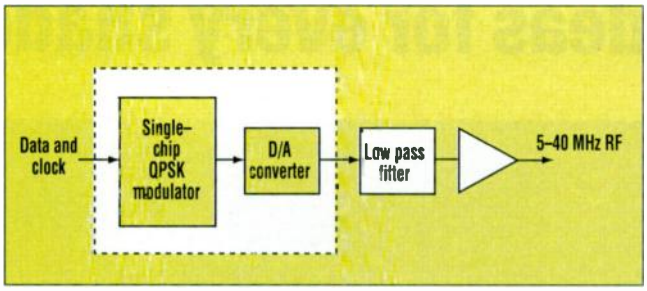
to tune a different frequency in microseconds (instead of hundreds of milliseconds), the upstream equipment reduces service interruptions. In addition, properly designed equipment provides near-theoretical noise performance to ride above low-level ingress (*Fig. 3b, again*).

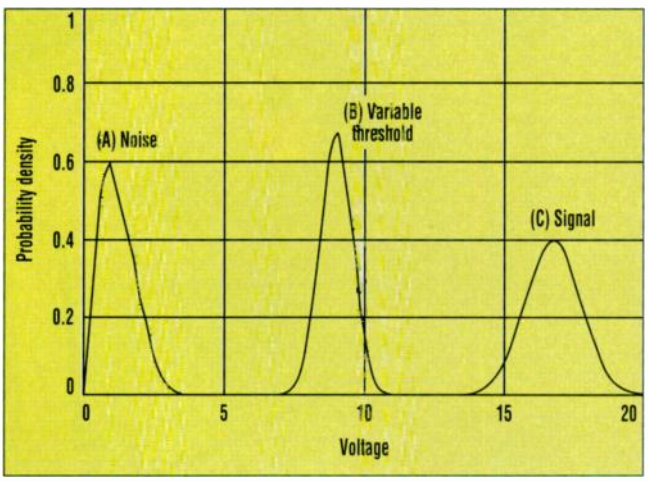
• *Impulse and burst noise.* Careful analog and digital design overcomes or reduces the problems caused by impulse and burst noise, which is considered by many to be the most significant impairment in the channel. A demodulator may be considered "robust" if it does not false-trigger or lose sync as a result of short, strong noise impulses or bursts, and if it incorporates appropriate forward error correction (FEC), such as Reed-Solomon coding,to correct errors caused by these events. Differential QPSK encoding, which is more robust than absolute encoding, is also recommended.

• *Variation in upstream plant gain.* To configure a new user in the network, as well as for ongoing transmit level control, it is important for the receiver to have a built-in power meter known as a received signal strength indicator (RSSI). This allows the system controller to vary the gain via the downstream control channel. In addition, the receiver needs to have a large instantaneous dynamic range of up to 20 dB to account for any variations in signal level.

• *Variable channel noise level.* An adaptive threshold technique permits the receiver to adjust to the average background noise level in a CATV channel. In the accompanying figure, distribution A is noise alone, distribution B is the adaptive threshold, and distribution C is the desired signal plus noise (*Fig. 7*). If the noise exceeds the threshold when no signal is present, a false alarm occurs. If a signal arrives at the receiver but is not strong enough to pass the threshold, a missed packet occurs. The adaptive technique causes the threshold to vary with the noise, which lowers the probabilities of false alarm and missed packets. In the case shown, both probabilities are less than 10^{-11}.



6. The STEL-1108 subscriber modulator chip digitally synthesizes the 5 to 40 MHz QPSK upstream signal. The new STEL-1109 with integrated DAC and 5-65 MHz output is shown within the dotted line. The new part also incorporates 16-QAM modulation and FEC capabilities.



7. Packet detection distributions. A false alarm occurs when A>B (noise exceeds threshold). A missed packet occurs when C<B (signal does not pass the threshold). The threshold varies with the background noise.

Conclusions

A three-pronged approach is needed for success in upstream transmission:

1. Knowledge and application of the channel model.
2. A strong technology base in burst demodulation.
3. A cost-effective single-chip modulator for subscriber terminals.

The successful execution of these approaches results in robust, reliable, and economical performance in the challenging upstream CATV channel.

Bruce Currivan is Technical Director, Cable Telecom Products, at Stanford Telecom, Sunnyvale, Calif. He also is Chairman of the IEEE 802.14 subgroups on upstream channel modeling and physical layer evaluation.

Bill Xenakis is Program Manager of Cable Telecommunication Products, at Stanford Telecom.

This paper was originally presented in the Society of Cable Telecommunications Engineers (SCTE) CableTec Expo '96 Proceedings Manual, pages 303-314.

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6. The STEL-1103, STEL-1108, and STEL-1109 modulator chips are covered by U. S. Patent number 5,412,352.

7. T. Williams, M. Chelehmal, and R. Prodan, "Field Evaluation of Reverse-Band Channel Impairments," *SCTE 1996 Conference on Emerging Technologies*, January, 1996.

8. The adaptive threshold technique is the subject of a pending patent.

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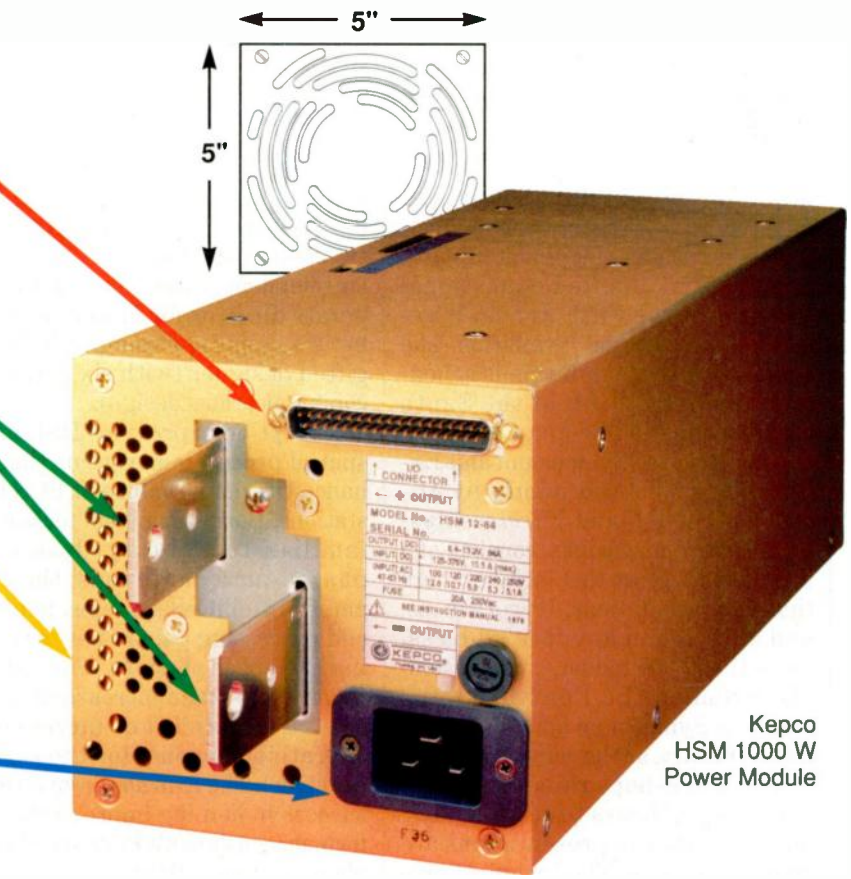

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Wireless Conference Points To Growth In Data/Voice Systems

Affordable High-Performance ICs Are Paving The Way For Application Growth In Cellular Communications, Personal Communications Services (PCS), And Wireless-Local-Area Networks (WLANs).

Lee Goldberg

Wireless technology embodies many different disciplines, including RF engineering, digital signal processing (DSP), and power-supply design. Engineers faced with integrating these disciplines into the development of wireless systems can find educational guidance at the Fifth Annual Wireless Symposium and Exhibition. The conference and exhibition is scheduled for Feb. 10-14, at the Santa Clara Convention Center, Calif.

The Wireless Symposium and Exhibition, sponsored jointly by *Microwaves & RF* and *Wireless Systems Design* magazines, consists of a technical program that includes more than 90 presentations, 10 workshops, and a luncheon keynote address. More than 6000 industry professionals attended the Fourth Annual Wireless Symposium and Exhibition last February, at the same location.

The workshops range in length from several hours to several days, and the technical presentations are 30 minutes each. The technical presentations have been carefully collected from leading engineers in the wireless design community, giving attendees a chance to learn from these presentations and exchange their own ideas during each question-and-answer period.

The half-hour technical sessions are officially launched with the keynote luncheon at noon on Feb. 10. The keynote address will be delivered by Dr. Martin Cooper, chairman of the board and chief executive officer of ArrayComm, Inc., San Jose, Calif. Following in the footsteps of such dynamic wireless keynote speakers as Dr. Irwin Jacobs of Qualcomm and new president of Motorola, Bob Growney, Dr. Cooper is best known for having guided the design team that created the first cellular telephone, while he was R&D corporate director for Motorola. While he is a capable manager, he's also gifted designer (with six patents in communications design).

ArrayComm provides DSP-based spatial processing systems that enhance the performance of PCS base stations. Borrowing from technology familiar to military designs of phased-array antennas, the company's IntelliCell systems, in effect, add processing gain to new or existing PCS base stations. This advantage results in an increase in coverage area (and an increase in operating economy for the service provider). The firm has enjoyed early success in helping improve the performance of Japan's Personal Handyphone System (PHS).

The choice of workshops at the conference has been expanded in recent years, providing attendees with an educational palette ranging from amplifier design to wireless regulations and standards. Randy Rhea has returned once again to present his popular one-day course on "Oscillator design for wireless applications." Professor Jack Holtzman is back for the fifth consecutive year, with his concise course on spread spectrum techniques.

The Wireless Symposium boasts a technical program with over 90 presentations and 10 workshops.

Other returning educators include Al Scott with his two-day "Wireless design made simple" course and Les Besser and Steve Cripps with their three-day "Wireless RF circuit design" course. The Besser and Cripps course also can be attended as separate one-day courses covering monolithic versus discrete, small-signal amplifier design; low-noise amplifier design; and high-efficiency/power amplifier design. Another returning educator from the Third Wireless Conference is Larry Burns, who offers a one-day course on "Wireless receiver design."

The conference features several new workshops, including a half-day session on regulations and standards, "Wireless datacom regulatory scene," presented by Wayne Meyers, vice president of Wincom, Santa Cruz, Calif. Mr. Meyers is an active member of the IEEE 802.11 standard committee (established to set specifications for wireless LANs). This important workshop will cover different standards and regulations, and how they impact the development of different wireless data-communications systems.

Morris Engelson, long associated with Tektronix, Beaverton, Oreg., has often been called "the father of the spectrum analyzer" by the many engineers who have learned from him about this RF/microwave workhorse instrument and its virtually unlimited measurement capabilities. The "Measuring the wireless transmission spectrum," course is designed for anyone working with

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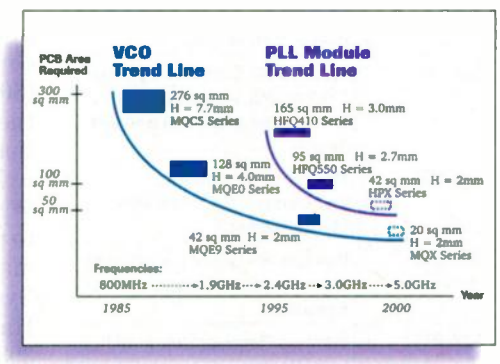

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wireless signals, or anyone working with a spectrum analyzer who would like to become more efficient in its use. The workshop addresses measurements on digitally-modulated wireless signals, EMI, RFI, pulsed signals, high-power signals, radio broadcast signals, TV signals, as well as effective ways to measure these signals with a spectrum analyzer.

Last, but not least, Sanjay Gupta, associate professor in the Dept. of Electrical and Computer Engineering, Illinois Institute of Technology, Chicago, has assembled an information-packed course that covers one of the most potentially explosive wireless markets: wireless LANs (WLANs). This half-day tutorial course will help design engineers understand different strategies for implementing WLANs, sensible spread-spectrum approaches, appropriate modulation, operating frequency options (other than the popular 2.4-GHz band), protocols usage between systems, and RF propagation for wireless data transmission. This course may provide invaluable insight for any engineer considering WLAN systems design.

The schedule of technical presentations includes several sessions on cellular/cordless and PCS design, still two of the fastest-growing application areas for wireless technology *(see the table)*. Several presentations offer ideas for leveraging existing infrastructures, such as the Global System for mobile communications, for digital cellular network, and the Digital European Cordless Telephone system, for wide-area-network and multimedia applications. Sessions on PCS design highlight the need for low-voltage (3-V dc) ICs for handsets, as well as low-phase-noise performance to minimize degradation of bit-error-rate performance.

Technical sessions at the symposium will also focus on emerging applications for video transmission in satellite communications, the importance of cost-effective substrate materials, high-power design, and methods for evaluating intermodulation distortion in wireless components and systems.

For more information about particular events at the Fifth Annual Wireless Symposium and Exhibition, contact Mary Begley, Trade Show Manager, at (201) 393-6297. Up-to-date information also can be accessed over the Internet: *http://www.penton.com/wireless*, or by using the conference's FAX-back services: (800) 561-SHOW (561-7469) within the U.S., (516) 222-4941 for international calls.

Readers unable to attend the Wireless Symposium who would like to purchase a copy of the proceedings may contact Dawn Prior, Wireless Systems Design, 611 Rte. 46 West, Hasbrouck Heights, NJ 07604; (210) 393-6286.

THE WIRELESS SYMPOSIUM AT A GLANCE

Technical Sessions

Day/Date	Time	Subject
Monday, February 10th	2:30 PM — 5:30 PM	RFID/Automotive Applications
	2:30 PM — 5:30 PM	Wireless Component Solutions
Tuesday, February 11th	8:30 AM — 12:00 PM	WANs and WLANs
	8:30 AM — 12:00 PM	Cellular/Cordless Design, I
	1:30 PM — 5:30 PM	Personal Communications Services (PCS) Applications
	1:30 PM — 5:30 PM	Test and Measurement Solutions
Wednesday, February 12th	8:30 AM — 12:00 PM	Modulation Techniques
	8:30 AM — 12:00 PM	Digital Communications Systems
	1:30 PM — 5:30 PM	Satellite Communications
	1:30 PM — 5:30 PM	Materials and Packaging Technologies
Thursday, February 13th	8:30 AM — 12:00 PM	Spread-Spectrum Techniques
	8:30 AM — 12:00 PM	Integrated-Circuit Solutions
	1:30 PM — 5:30 PM	Cellular/Cordless Design, II
	1:30 PM — 5:30 PM	High-Power Design
Workshops		
Monday, February 10th	9:00 AM — 5:00 PM	Wireless Design Made Simple with Al Scott
	9:00 AM — 5:00 PM	Oscillator Design For Wireless Applications with Randy Rhea
	9:00 AM — 12:00 PM	Spread Spectrum with Professor Jack Holtzman
	1:30 PM — 5:00 PM	Wireless Datacom Regulatory Scene with Wayne Moyers
Tuesday, February 11th	9:00 AM — 5:00 PM	Wireless Design Made Simple (Day 2) with Al Scott
	9:00 AM — 5:00 PM	Wireless RF Circuit Design, Part 1 (Monolithic versus discrete small-signal amplifiers) with Les Besser
	9:00 AM — 5:00 PM	Measuring the Wireless Transmission Spectrum with Morris Engelson
Wednesday, February 12th	9:00 AM — 5:00 PM	Wireless RF Circuit Design, Part 2 (Low-noise amplifiers) with Les Besser
	9:00 AM — 5:00 PM	Wireless Receiver Design with Larry Burns
Thursday, February 13th	9:00 AM — 5:00 PM	Wireless RF Circuit Design, Part 3 (High-efficiency amplifiers) with Steve Cripps
	9:00 AM — 12:00 PM	Wireless Local-Area Networks (WLANs) with Professor Sanjay Gupta

How Valuable	Circle
Highly	528
Moderately	529
Slightly	530

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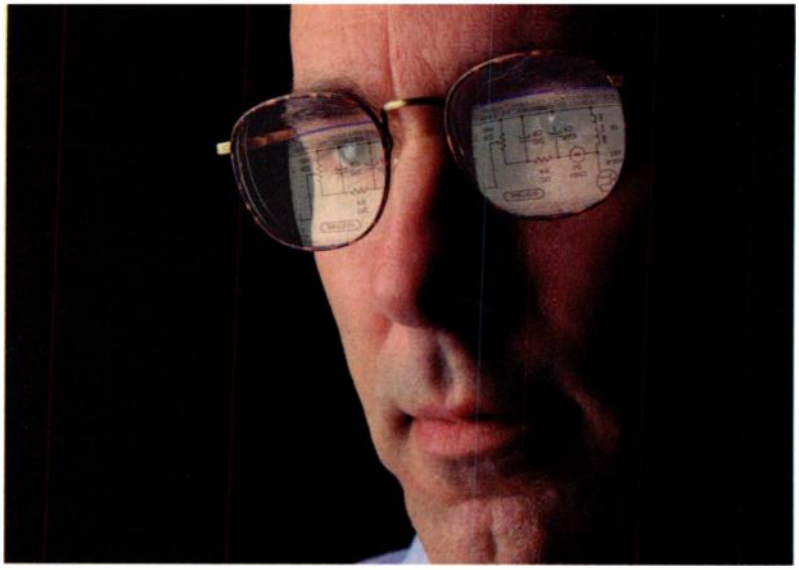

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Electronica '96 Takes The Wraps Off Advanced Communications Devices

The Latest ICs For Mobile And Cordless Telephones And ISDNs Are Showcased, With SLICs And Controllers Also Featured.

Alfred Vollmer

At Electronica '96 (Nov. 12-15, 1996), a host of new announcements were made for advanced telecommunication ICs. One of the hottest areas was devices for Global System for Mobile Telecommunications (GSM)—PCN and PCS digital mobile telephones. The semiconductor group of Siemens AG, Munich, Germany, for example,featured a new generation of chips, the HiGOLD series. These ICs represent a higher level of integration of the existing GOLDplus chip set, and integrate all digital baseband functions on one chip.

HiGOLD consists of a new HiGOLD baseband processor (the PMB2800), a GAIM (GSM Analog Interface Module) analog interface IC (the PMB2905), and a codec (the PMB2708, developed for the American market), as well as the required RF ICs. This chip set allows the construction of GSM-compatible PCN or PCS mobile telephones from baseband through to the antenna. The HiGOLD is fully software compatible with the GOLDplus generation.

Telefunken Microelectronic (Temic) GmbH, Heilbronn, Germany now has integrated all RF transmission functions of a mobile telephone onto one IC, the U2893B. The chip can be used without any modification in the mobile telephone standards of GSM, DCS1800, and PCS1900. Telephone manufacturers can exploit a single basic design for several different telephones.

Dual-band telephones that can operate in the GSM and DCS bands now can be produced with the same hardware. Because the U2893B's new architecture requires less filtering, the duplexer between the antenna and the power amplifier can be omitted, resulting in board-space and cost savings. An I/Q modulator, a mixer, programmable dividers, and a phase frequency detector (PFD) are integrated in the IC's SSO28 package. With an input of 40 mA, the modulator is able to process signals up to 500 MHz. The mixer can be operated up to 2.5 GHz, and is used as a down-converter for feedback.

The output signal of the mixer serves as a local-oscillator (LO) signal for the modulator and the I/Q signals from the baseband are modulated in the modulator. Then, the modulated signal is compared with a reference signal, which can be set with the integrated dividers in such a way that GSM, DCS, PCS, or dual-band (e. g. GSM/DCS) operation is possible. The PFD controls a charge pump which, in turn, activates the transmission voltage-controlled oscillator (VCO), whose output signal goes to the power amplifier and into the control loop. The phase frequency detector can process frequencies up to 200 MHz.

New SAWs

In the passive components market, Siemens Matsushita Components GmbH (S+M), Munich, Germany, now offers a new kind of surface acoustic wave (SAW) filter for analog (Advanced Mobile Phone Service) AMPS mobile telephones. The L437B integrates two filters in a single package no bigger than a conventional RF SAW filter. In the heterodyne receiver of an AMPS telephone, the received frequency is down-converted to a fixed intermediate frequency (IF). A mixer mathematically multiplies the received signal and the signal of the local oscillator (LO). Both the received and clean LO frequency need to be filtered out before they're applied to the mixer. The filtering step is required to get rid of frequency mixture products. Until now, different filter techniques were used for receive and LO filters. The receive or interstage filter was usually a SAW filter, while the LO filter was either composed of coils and capacitors, or consisted of multilayer ceramic. Siemens Matsushita Components

Fig. 1. Stripline coaxial technology is behind these microwave ceramic filters from Siemens Matsushita Components (S+M). They're aimed at GSM cellular and DECT cordless telephones.

So you say You need a

16-bit,

Upward mOving, mind-bending,
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real-time, riGht-NOW,
bust-riGht-Out-of-the-bOx

MCU

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COMMUNICATIONS TECHNOLOGY ELECTRONICA REVIEW

duplex modem communication and data-rate adaption according to V.110. It supports both voice and data applications using two B channels. A common ISDN application program interface known as a (CAPI) driver provides a hardware-independent interface to control the dialing and D-channel protocol. It supports North American, European and Japanese D-channel protocols. The CAPI driver is ready to use with an installation/uninstallation utility, and includes extensions to control special hardware features over this interface.

The package also includes application software to interface to the CAPI. The Siemens driver structure also supports Microsoft's NDISWAN and dial-up networks as well as AT-command-based applications.

Siemens also is offering a communication controller, the DSCC4 and a multichannel HDLC controller, the MUNICH32X (ELECTRONIC DESIGN, *Nov. 4, 1996, p. 53)*.

ISDN Interface Chips

Two new ISDN basic-rate devices have been introduced by the Components Division of Alcatel SA., Paris, France. The MTC-20278/79 combines four U interfaces on a single chip. Designed for use in public switching subscriber cards, it's available in pin-compatible line-code versions for 4B3T (MTC-20279) and for 2B1Q (MTC-20278). The second device, the MTC-20276/77, is nicknamed INT (Integrated Network Terminator), and is targeted for use in the network termination unit which provides the necessary interface between the telephone network and the standard S0 bus. This interface is now found in all terminals designed with an ISDN two-channel link. The MTC-20276/77 is a single chip which combines the U interface and the S0 interface functions *(Fig. 2)*. It reduces the size of a network terminator to a single chip, plus a few additional passive components. It's available in pin-compatible versions for both 4B3T and 2B1Q line codes.

Ericsson Components AB's Microelectronic Division, Kista, Sweden, is now offering a newly-designed family of SLICs *(Fig. 3)*. Designated the PBL 386XX series, "the devices offer improved performance and functionality, greater ruggedness, lower power consumption, and lower-solution costs than SLICs currently available," states Stefan Loef, product manager for line circuits at Ericsson Components.

"Helping system designers to reduce costs was a key consideration in the introduction of the PBL 386XX family," he adds. The devices can be used for applications like DLC (digital loop carrier), CO (central office), DAML (digital added main line), PBX (private branch exchange) and TAs (terminal adapters). Every device has the same pinout so the same pc board and footprint can be used for every application. Furthermore, the SLICs can be used in applications requiring constant current or resistive dc feeds by changing an external resistor. The on-hook power consumption of the new SLICs is 60 mW, which is, according to Loef, less than half the consumption of the previous SLICs. In addition, the devices can operate with single- or dual-battery supplies which are automatically selected by a proprietary integrated battery switch.

This feature of the PBL386XX removes the need for external logic and support from the microcontroller. For example, the PBL 38620 SLIC is a 90-V bipolar circuit optimized for use in PBXs, terminal adapters, and other telecom equipment. It emulates resistive loop feed, and is programmable between 2 x 50 Ω and 2 x 900 Ω, with short-loop current limiting adjustable between 18 and 30 mA. In the current-limited region, the loop feed is nearly a constant current with a slight slope corresponding to 2 x 30 kΩ. A second lower battery voltage may be connected to the device to reduce the short-loop power dissipation. The SLIC automatically switches between the two battery supply voltages without the need for external components or external control. It incorporates loop current, ground key, and ring trip detection functions, but also is compatible with loop start signaling.

Two-to-four-wire and four-to-two-wire voice frequency signal conversion is accomplished by the SLIC in conjunction with either a conventional or programmable codec/filter. The programmable codec/filter option provides the flexibility to use features such as transmit and receive gains, hybrid balance, and two-wire impedance (adjustable by the system controller). Furthermore, longitudinal voltages are suppressed by a feedback loop in the SLIC, and the longitudinal balance specifications meet Bellcore TR909 requirements.

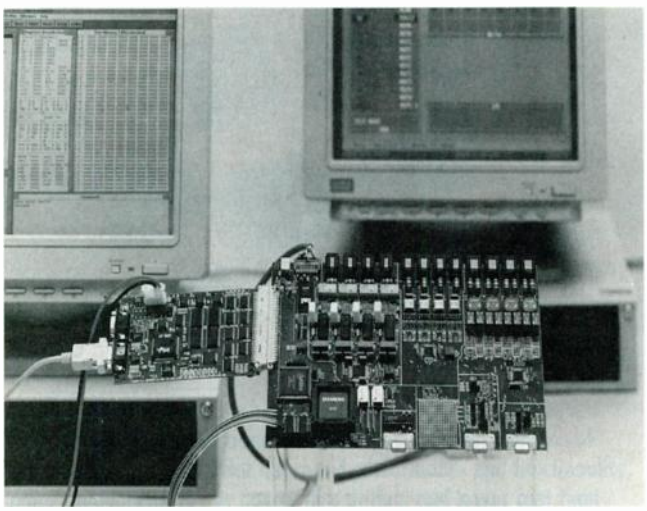

Fig. 4. All the features needed for building a PBX are incorporated in this DSP-oriented PBX controller from Siemens Semiconductors. The PEB20560 includes all the necessary functional blocks for digital switching and signaling, as well as DTMF tone handling and conferencing.

An All-In-One PBX

An IC incorporating "almost all features for building PBX systems" has been developed by Siemens Semiconductors. The PEB20560 DSP-oriented PBX controller (DOC) can be used as the central switching controller for small PBXs, or as a switching controller on PBX line cards *(Fig. 4)*. It comprises all necessary functional blocks for digital switching and signaling as well as dual-tone multiple frequency (DTMF)/tone handling and conferencing. Only the open systems interconnection (OSI) layer-one transceivers are not integrated. Two D-channel arbiters reduce the number of

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HDLC controllers needed from up to 64 down to 2. An on-chip, user-programmable16-bit DSP offers 40 MIPS of processing power for music-on-hold, conferencing, voice-mail, modem emulation, etc., as well as user-programmable functions. In the PBX mode, the DOC provides six fully-usable IOM-2 interfaces, an industry standard created by Siemens for interconnecting telecom ICs.

Furthermore, it is able to control up to 48 ISDN or 96 analog subscribers . For transferring information (voice and signaling from subscriber lines to time slots on pulse-lock modulation (PCM) communication highways) the DOC also provides four PCM highways with 128 time slots. In the line-card mode, the DOC provides two fully-usable IOM-2 interfaces with 16 IOM-2 subframes (2 by 8), two limited IOM-2 interfaces, and four PCM highways with 256 time slots. It is able to control up to 16 to 24 ISDN, or up to 32 to 48 analog subscribers.

Signaling is handled by eight assignable HDLC controllers, each with a 64-byte data FIFO memory for transmit and receive direction. Two of them, which are called SACCO-As (Special Application Communication Controller-As), are dedicated to communication between ISDN terminal equipment and the line card. These controllers are able to be multiplexed to different subscribers for signaling purposes (LAP-D protocol) by two different integrated D-channel arbiters. D-channel arbiters are used to facilitate the simultaneous serving of up to 64 D-channels with only two HDLC controllers.

Four slightly-modified HDLC controllers, dubbed SIDEC (SACCO-based ISDN D-channel exchange controllers), are assignable to any time slot in the data upstream or downstream direction on four IOM-2 interfaces. Communication between line cards and a group controller is handled by two dedicated SACCO-B controllers. These controllers also are assignable to any time slot in the data upstream or downstream direction on four IOM-2 interfaces, or to PCM highways.

Both controllers may be used as standalone HDLC controllers with a transfer rate up to 8192 Mbits/s. Furthermore, Direct Memory Access (DMA) is also supported. The on-chip, user-programmable 16-bit DSP was developed by Siemens in cooperation with the DSP Group (USA). With access to 64 time slots, this DSP is able to execute routines for various purposes. The DCU (DSP control unit) is responsible for such functions as controlling external memories, emulation support, interrupt handling, and bus arbitration.

The DSP communicates with an external microprocessor via a bidirectional mailbox. The multiplexed 8-bit microprocessor interface is compatiblewith bus schemes from manufacturers such as Siemens and Intel and with some Motorola bus schemes. An integrated watchdog timer supports the recovery from software or hardware failures while the integrated UART is compatible with the standard 16C550A type UART. The UART can be used for system tests and program downloads via a V.24 interface.

On the DOC chip there also is an interrupt controller, a multifunction I/O port, and a programmable clock generator with built-in logic for master and slave configurations. A serial test interface provides boundary scan test support for cost-effective circuit board testing according to IEEE standards.

The on-chip emulation allows the debugging of DSP programs in the field because it is accessible via a serial interface. To facilitate the board design of PBX systems and line cards with the DOC chip, Siemens provides specific software development tools. The development software contains a macro assembler, linker/locator, debugger, and simulator. The simulator allows the verification and monitoring of the DSP routines even without the DSP hardware. A development board with an ISA extender can be used for a quick start into new development projects. Siemens also intends to offer a PBX-oriented evaluation board with the DOC and basic software modules included as standard on the board.

How Valuable	Circle
Highly	487
Moderately	488
Slightly	489

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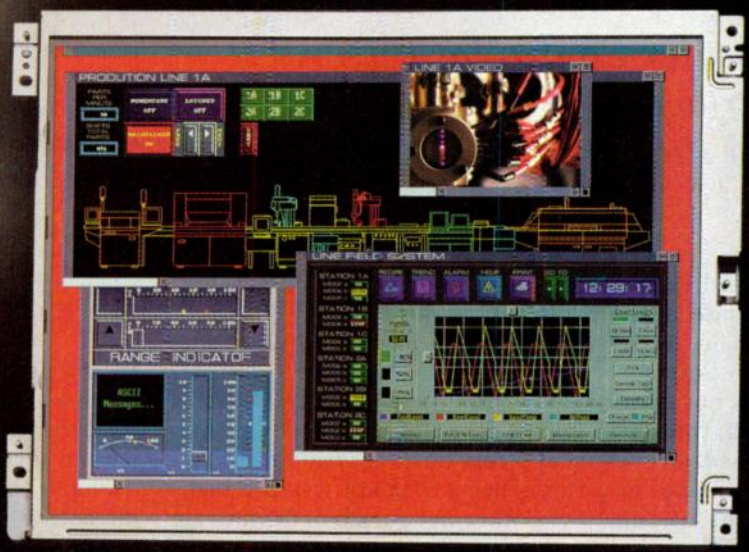

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12.1"	LM80C31	800 x 600	200
13.8"	LM14S70	800 x 600	150
13.8"	LM14X79**	1024 x 768	200
15.0"	LM15X77**	1024 x 768	150
17.7"	LM18X74	1024 x 768	150

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Four-Port Hub-On-A-Chip Slashes The Cost Of Fast Ethernet

A 100-Mbit Repeater Controller Integrates Four PHY Interfaces; A Quad Transceiver Makes Switched 10Base-T More Affordable.

Lee Goldberg

The maturation of the Fast Ethernet market is proceeding quickly as it finds its way to more desktops every day. With the cost of some 100-Mbit/s network cards hovering just above the $100 mark, there is great interest in simple, inexpensive hubs to meet the needs of smaller networks or workgroups at the edges of larger LANs. With a new chip from Advanced Micro Devices, designers may be better equipped to meet the rising demand for low-cost Fast Ethernet infrastructure. Another chip, a quad Ethernet switching transceiver aimed at traditional 10Base-T systems, is being introduced at the same time.

The Fast Ethernet chip, the IMR100 (also known by its AMD part number, the Am79C730) is a four-port, cascadable repeater hub that offers designers and manufacturers many competitive advantages over other network hub devices On one chip, it incorporates the entire Ethernet physical layer [including clock recovery and multi-level threshold 3-1 level (MLT-3) transmit/receive functions], the repeater controller, and collision detection logic. This design sends the parts count for a simple, unmanaged eight-port repeater hub plummeting from around nine chips to two, resulting in savings of PCB area, case material, and assembly costs. As a bonus, the chip's reduced power requirements (about 1.5 W—50% less than a less integrated solution) allow designers to use a smaller power supply and less cooling.

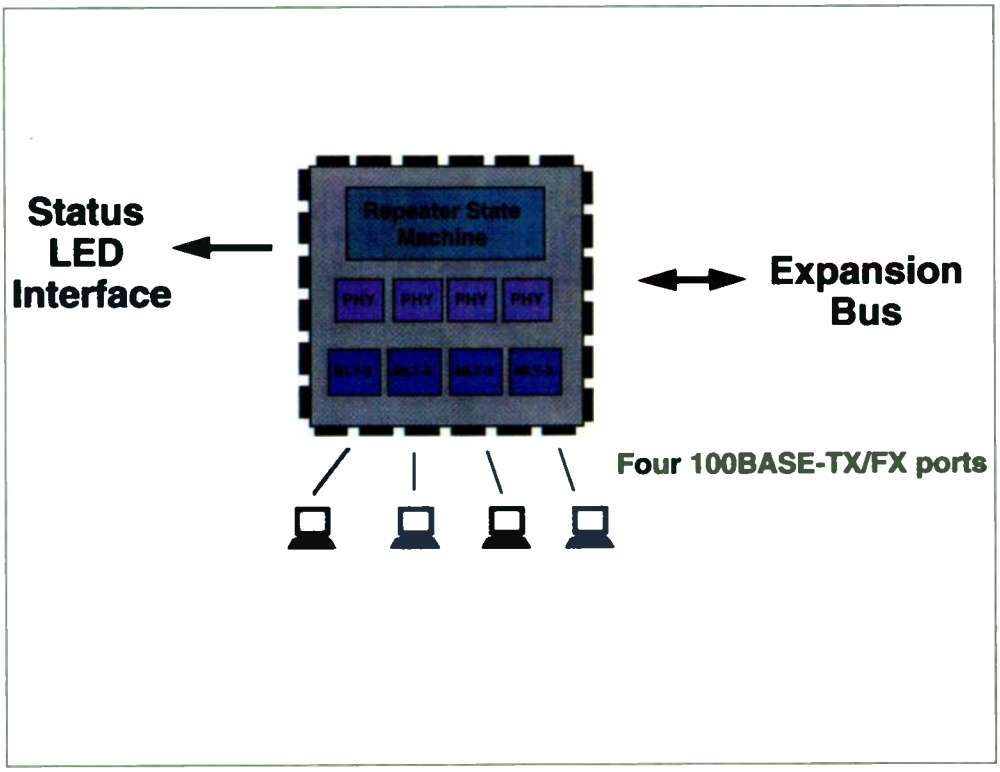
Low Cost, Tall Features

Despite its emphasis on reducing cost, the IMR100 also offers flexibility and several special features. For example, the chip is designed to handle both 100Base-TX (category five twisted-pair copper), and 100Base-FX (fiber-optic), and has a built-in asynchronous expansion bus. The bus makes it easy to cascade the devices within a single box, or across several stackable modules.

Another feature included in the chip are the logic and driver circuitry for a complete set of status LED indicators for link, partition, and carrier sense. Rate-based LED support also is available for global-receive activity and collision frequency.

While intended for use in "dumb," unmanaged hubs, the IMR100 is not completely helpless. Thanks to its user-enabled, far-end fault-indication (FEFI) capability, it can help users easily diagnose a partially severed wire or degraded connection.

Another state-of-the-art feature is the baseline-wander correction circuitry included in each of its four MLT-3 output drivers. Baseline wander is a dc offset of the signal which can be caused by certain fatal data patterns. These patterns can cause



The four-port IMR100 handles both 100Base-TX (twisted-pair) and 100Base-FX (fiber optic) media. Each of the four MLT-3 (multi-level threshold 3-1 level) output drivers includes baseline-wander correction.

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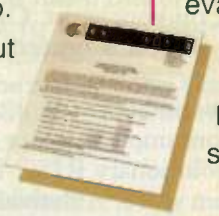

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Fast Ethernet Chip Family Builds Smart, Low-Cost, Networking Products

All-Digital Fast Ethernet Chips Cut Parts Count And Cost Of Managed And Unmanaged Hubs And Switches.

Lee Goldberg

The first offerings of a new family of Fast Ethernet ICs are aimed at giving designers a competitive edge in the increasingly price/performance-conscious network devices market. Having originally made its mark in the LAN world for delivering the first 100Base-T4 (4 pair UTP CAT-3) Ethernet transceiver, Broadcom Corp. has aimed its proprietary silicon compiler technology at the rapidly maturing 100Base-Tx (2 pair UTP CAT-5) market. The result is a family of all-digital integrated circuits that can be used to reduce the component count and cost of both managed and unmanaged repeater hubs, as well as other Fast Ethernet products.

Heading the family is the BCM5205, a fully integrated, five-port, 100Base-Tx repeater. It incorporates four 100Base-Tx physical-layer transceivers, an MII (media independent interface) port, a repeater controller, and repeater management logic. Large multiport hubs can be easily created by connecting the repeater chips via their integrated expansion bus circuits.

Each of the chip's transceivers requires only a simple set of magnetics to directly drive an IEEE 802.3u-compliant pair of Category-5 cables. If desired, any or all transceivers may be connected to a 100Base-FX fiber-optic driver and receiver instead. The transceivers also have carrier-integrity detection circuitry which can sense far-end line breaks and disable the transceiver before it can corrupt traffic from the other ports.

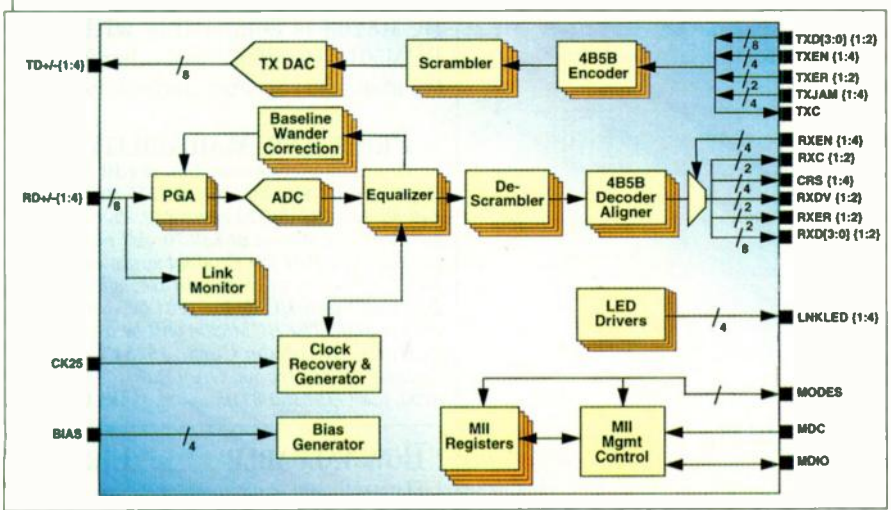
All-Digital Architecture

One of the unusual aspects of the transceivers, which are used in all of the new chips, is that their signal path is entirely digital. Using its proprietary silicon compiler, Broadcom's design team is able to quickly develop chips that include complex digital filtering, equalization, and other DSP functions. This was used to implement all the signal conditioning and processing functions used in the BCM5205 hub, the BCM5203 transceiver and the other chips of the BCM52XX Fast Ethernet family.

Once the LAN's signal enters one of the chip's receivers, it is immediately passed through an analog-to-digital converter (ADC) (sampling at 125 MHz) and does not become an analog signal again until it emerges from the transmitter's digital-to-analog converter (DAC) *(see the figure)*. Each channel undergoes digital adaptive filtering and decoding before being passed to the repeater port logic. This helps maintain signal integrity, even under poor and variable line conditions. On the output side, digital synthesis is used to perform baseline-wander correction as well as wave-shaping functions to eliminate the need for external filter components.

The BCM5205 hub's single MII port can be configured to connect to an 802.3 media access controller (MAC). Attaching the MAC allows designers to use the repeater to terminate four (or more) Fast Ethernet connections on a single switch port, an efficient way to expand a switching hub. The MII port also can be used as a fifth transceiver interface to bridge hub traffic to another PHY type. This only requires the addition of any 100Base-Tx or -FX MII-compliant transceiver. In addition, the 5205 has all the logic and driver circuitry required for the traffic and status indicator LEDs common to most repeater hubs.

If SNMP and RMON management is desired, the BCM5205 can be directly interfaced to the BCM5020, a repeater management device. Together, they collect traffic statistics which are used to evaluate network performance and identify problems. The management device observes traffic from the inter-repeater interface, analyzes data, and classifies the network events in terms of the IEEE



The BCM transceiver chip is a subset of the Broadcom BCM5205 repeater IC. It includes the data conversion, equalization, decoding circuitry, and other related features of the more complex chip.

802.3 or RMON statistics reporting formats. An automatic statistics management feature in the BCM5020 allows it to perform all statistics retrieval and management functions without the aid of an external controller. Capable of managing single- or dual-segment repeater sections, the device interfaces easily to most industry standard 8- and16-bit microcontrollers. Only one BCM5020 is required for an entire Fast Ethernet stack or chassis hub.

Special Solutions

While a one-chip hub solution is ideal for many applications, there are many products that could benefit from advanced transceiver technology but cannot use the BCM5205's 100Base-Tx repeater function. To fill this requirement, Broadcom created the BCM5203 and BCM5208, a pair of transceiver-only offerings that allow a designer to take advantage of many of the cost and space savings realized by the more complex repeater chip.

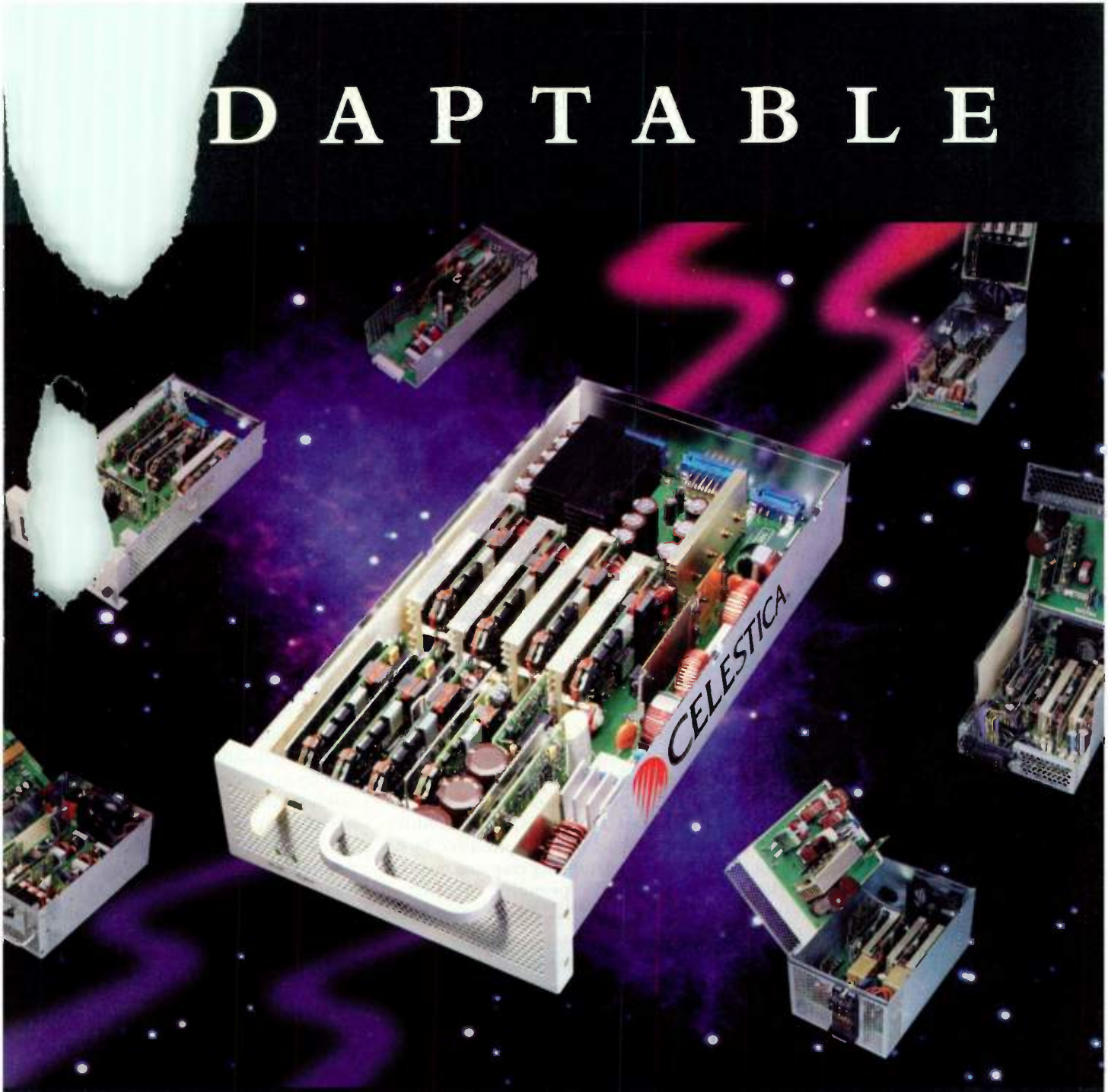
For those designers who are using proprietary silicon solutions for their repeater designs, the BCM5203 offers a technique for dramatically reduceing parts count and system cost by integrating four PHY-layer 100Base-Tx transceivers within a single chip. The device's all-digital transceivers and integrated status indicator LED driver circuitry are nearly identical to the components found in the BCM5205 repeater. An independent tri-state for each port allows several devices to connect to the repeater controller through a single MII bus. The BCM5203 is compatible with the BCM5010, BCM5012, and other industry standard repeater controllers.

Price And Availability

In 10,000-piece quantities, the BCM5203 is priced at $32.60, the BCM5205 costs $39.80, the BCM5020 costs $58.50, and the BCM5208 is offered at $38.70. All parts are packaged in PQFPs. Product samples of the BCM5203 are now available, while the BCM5205 and BCM5020 will be sampling next month. The BCM5208 will be available in April. Broadcom Corp., 16251 Laguna Canyon Road, Irvine, CA 92718; (714) 450-8700, fax (714) 450-8710. **CIRCLE 500**

How Valuable	Circle
Highly	531
Moderately	532
Slightly	533

DAPTABLE



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UPDATE ON CDMA TECHNOLOGY

Synchronous CDMA Technology Improves Cable-Modem Performance In Noisy HFC Environments

If hybrid fiber/coax (HFC) cable systems are to deliver on their promise of high-speed Internet and other interactive service access, they must be able to carry high-speed data reliably, both ways between subscribers and system headend. Delivery of downstream traffic (from the headend to subscriber) has been relatively easy, given a cable system's wide bandwidth and distribution system. Upstream communications (from the subscriber to the headend) have proven to be significantly more difficult, thanks to the noisy, unpredictable environment found on the reverse channel of most HFC networks.

Recently, however, Terayon Corp., Santa Clara, Calif., introduced a technology known as synchronous code-division multiple access (S-CDMA). Its developers view it as a powerful tool for achieving faster and more robust two-way communications over co-axial-based networks.

To understand the advantages of S-CDMA, it's important to look at the challenges faced by a signal on its trip from a subscriber's modem to the network headend. Many of the cable networks' difficulties with two-way data stems from the fact that they were not originally designed for upstream traffic, and suffer from several phenomena that create a very noisy environment. Typically, HFC networks place home-to-headend traffic in the 5- to 42-MHz region, known as the sub-split band, which resides below the video channels.

Unfortunately, the sub-split band finds itself in a part of the spectrum filled with both impulse and narrowband electrical interference, ranging from motor controllers and TV sets, to laptop computers and amateur radio operators. Known as ingress noise, it's commonly found in cable networks which have been installed without meticulous attention to how their lines' shields were terminated or grounded. Compounding the problem is noise funneling, which occurs as noise and signals from several branches are combined and amplified as they head upstream.

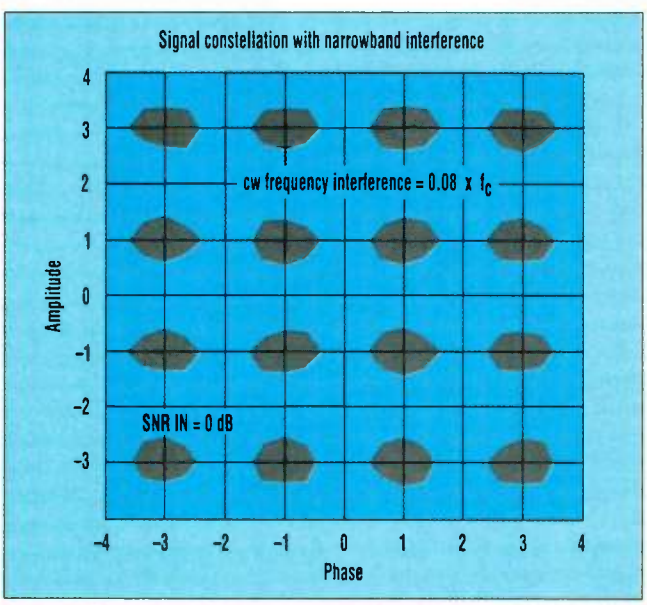
To cope with this environment, most HFC systems use simple, robust, phase-shift-keying-based modulation schemes which support low data rates (10 to 100 kbits/s, typically shared between 50 to 500 homes), but are fairly immune to the noise in the sub-split band. To improve a system's upstream capacity, more complex modulation—such as quadrature amplitude modulation (QAM), discrete multi-tone (DMT), or CDMA—must be used to squeeze more bits into the band's limited spectrum. Of these solutions, CDMA often works best in noisy environments by using wideband signals that are hard to intercept, demodulate, or impede.

Like CDMA, S-CDMA modulation's robust nature is achieved by using nonoverlapping chipping codes to perform the spreading function on each user's signal. As each one or zero of the data stream is tra[illegible]the transmitter creates a uniq[illegible]pectral pattern across the transmission band. That pattern is easily spotted by a receiver armed with the same code, even on an incredibly noise-ridden channel.

Conventional CDMA techniqu[illegible] have been used successfully to [illegible] mit high-speed data in a wirele[illegible] tem with noisy environments, [illegible] capacity tends to degrade a[illegible] users share the same piece [illegible] trum and signals begin to r[illegible] channel's noise floor even furt[illegible] chipping codes are only orthog[illegible] each other if they begin at the sa[illegible]e point in time. If operating in an asynchronous manner, portions of the codes from different sources can overlap, raising the overall energy (noise) level within the receiver's despreading section.

S-CDMA claims to avoid this problem by synchronizing all of the cable modem units to the headend. This arrangement permits each unit to spread its signal in a more orthogonal matter with respect to the other modems sharing the line. Thanks to synchronous transmission, S-CDMA greatly reduces the self-generated noise and permits much more efficient utilization of a given channel.

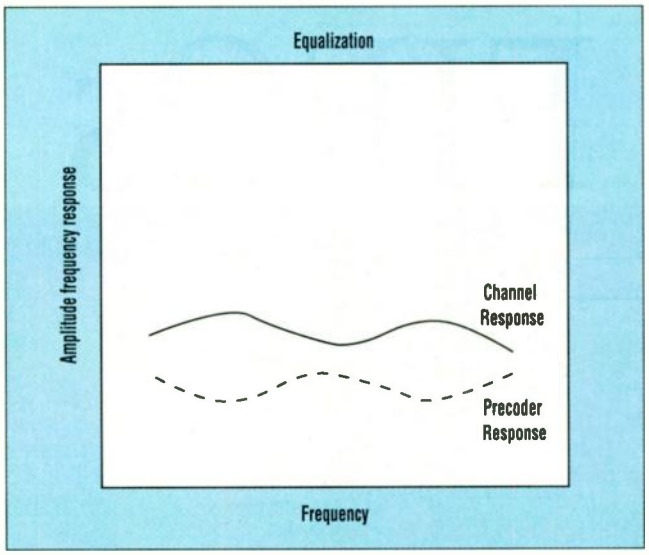
In practice, the Terayon system can support transmission rates of up to 10 Mbits/s in either direction using a single 6-MHz piece of spectrum (the bandwidth required for a single TV channel). The 10-Mbit/s main channel is actually composed of a series of 64-kbit/s streams, each individually trellis coded, and spread over the 6-MHz channel using its own unique spreading code. As in other systems, these data streams are further protected from loss through forward error correction (FEC). When combined with standard interleaving techniques, the data



1. The 16-QAM trellis-coding scheme employed by Terayon's S-CDMA technology encodes 4 bits of data into a single position within the phase/amplitude constellation. The S-CDMA process takes the QAM signal and spreads it across a 6-MHz portion of the sub-split band.

becomes much more resistant to impulse and Gaussian noise, as well as narrowband interference.

The Terayon system employs 16-QAM modulation, combined with spread-spectrum transmission for both its upstream and downstream channels. QAM's trellis coding adds 4.8-dB coding gain to the signal path, while the CDMA spreading function gives it an additional 22 dB of processing gain (Fig. 1). To combat data loss due to impulse noise, an interleaving process helps its data survive bursts of up to 100 µs. Together, these technologies yield a system-level interference rejection ratio of 27 dB.

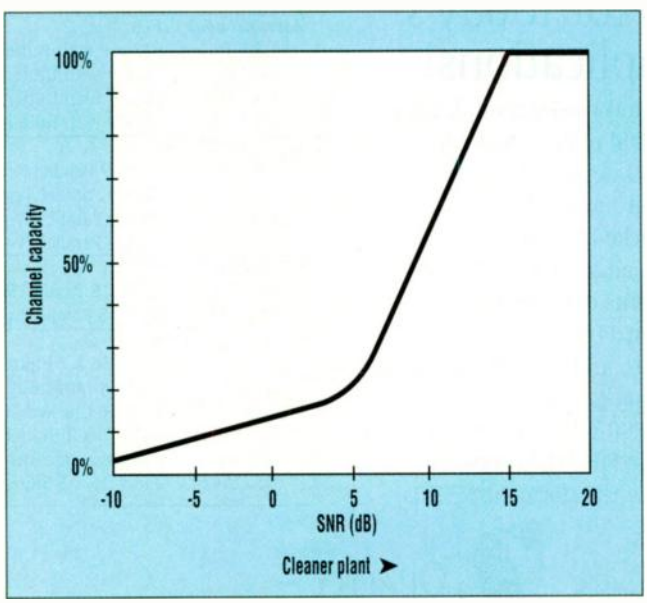


2. S-CDMA's precoder probes the frequency response characteristics of a particular cable segment, and adjusts its equalizer to cancel them.

The two primary techniques used to maintain code orthogonality between modems within the S-CDMA system are known as ranging and equalization. Ranging refers to the method used to determine the signal path length from a particular modem to the headend. Instead of transmitting all at the same time, modems that are closer to the headend start a short time later than the ones located farther away. This design assures that all the signals reach the upstream receiver at the same time. To compensate for changing line conditions (temperature-induced contraction/expansion and cable aging), ranging is accomplished on a continuous basis, transparent to the rest of the traffic.

Equalization is achieved by measuring the channel response from each user to the headend, and adjusting a precoder at the transmitter to invert the channel. The precoder's response corrects distortion induced by the channel response *(Fig. 2)*. S-CDMA's adherents claim that by maintaining orthogonality, it greatly minimizes mutual interference between users and provides increased capacity over asynchronous CDMA *(Fig. 3)*.

With the reliable, high-capacity upstream channel that S-CDMA claims to provide, HFC networks could be used for much more than the marginally interactive pizza-on-demand services currently anticipated by most cable operators. More sophisticated, bandwidth-intensive services such as teleconferencing, remote LAN access, distance learning, and telemedicine are only a few of the applications envisioned by Terayon. Terayon's S-CDMA scheme is flexible enough to allow it to be used for many types of IP-based or ATM traffic, including constant bit rate, variable bit rate, and available bit rate traffic. Bandwidth allocation per channel is negotiated with the headend, allowing support for applications with widely varied requirements on the same physical medium. For example, individual 64-kbit/s data streams may be allotted to telephony, while multiples of these may be aggregated and used for applications such as video conferencing and high-speed Internet access.



3. The system throughput of an S-CDMA-based return channel is shown under varying line conditions. Even under relatively harsh conditions, it can deliver 2 Mbits/s. It also can support data rates as high as 10 Mbits/s under line conditions typically found in today's cable plants.

While S-CDMA may have applications in wireless data transmission as well, Terayon is concentrating on putting it to work in cable/HFC systems. To this end, the company developed an ASIC-based S-CDMA transceiver that's produced by Lucent Technologies, Berkeley Heights, N.J. The chip is used in both the TeraPro cable modem and TeraLink 1000 headend master controller. Rather than take a proprietary approach, Terayon is open to discussion to eventually licensing S-CDMA technology and promoting it as a standard.

As most first-generation networks are already employing PSK-based technologies for their upstream channels, Terayon has set its sights on being written into the next generation of standards, and is currently working with several standards bodies (including MCNS, DAVIC, the ATM Forum, and theIEEE 802.14 Committee).

Shlomo Rakib, president of Terayon, is hopeful that the next generation of cable-modem standards will employ 64-QAM for its downstream data path, and a 16-QAM/10-Mbit/s S-CDMA upstream channel that would be shared by 100 to 2000 homes per fiber node.

For further information and literature, contact Terayon Corp., 2952 Bunker Hill Ln., Santa Clara, Calif., 95054, (408) 727-4400; fax (408) 727-6205; e-mail: *www.terayon.com*.

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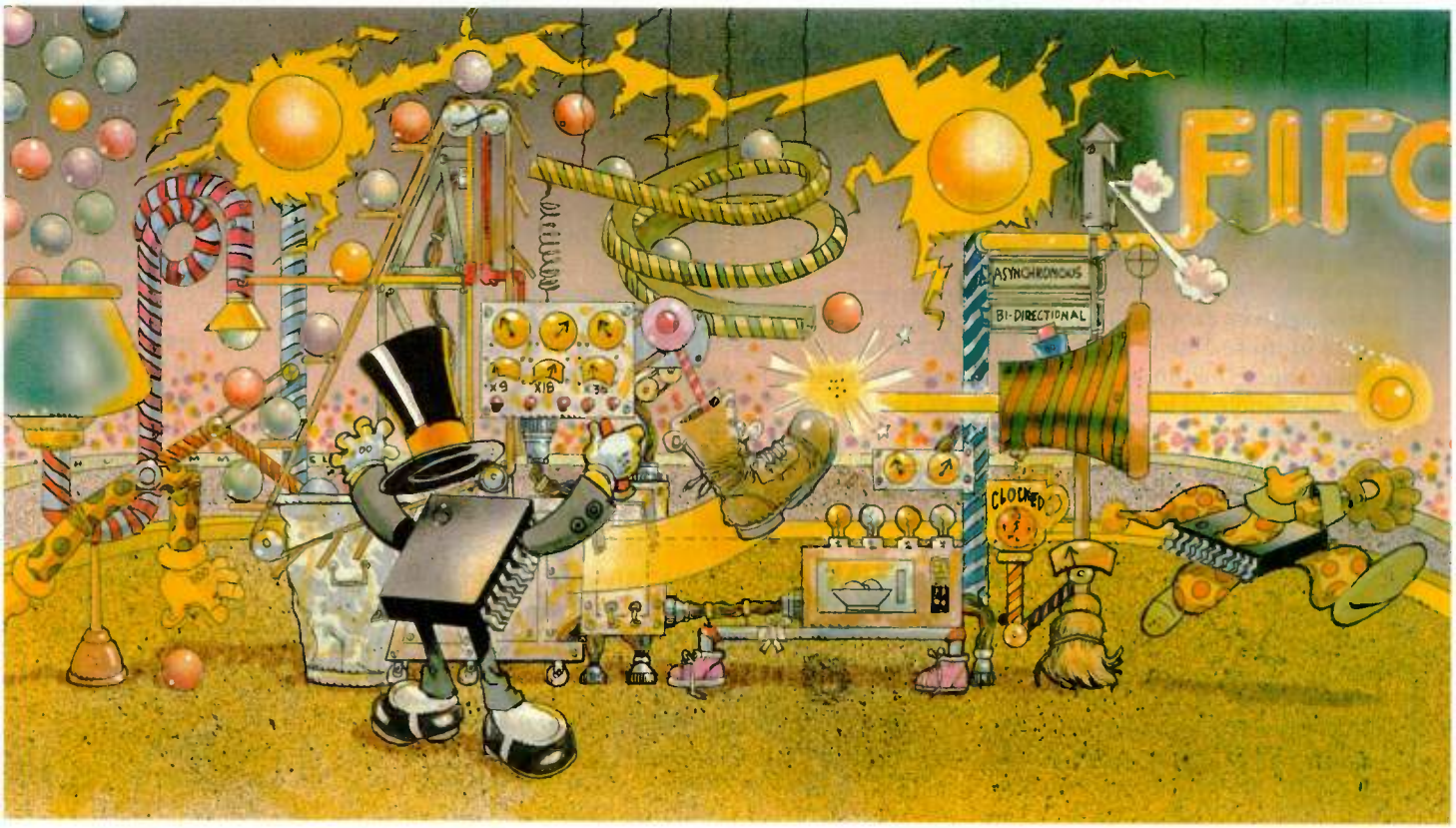

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QS7203	2K x 9 with Buffer Memory	32, 28
QS7204	4K x 9 with Buffer Memory	32, 28
Clocked x9 FIFOs		
QS72211	512 x 9 Parallel Synchronous	32
QS72221	1K x 9 Parallel Synchronous	32
QS72231	2K x 9 Parallel Synchronous	32
QS72241	4K x 9 Parallel Synchronous	32
Clocked x18 FIFOs		
QS72215	512 x 18 Parallel Synchronous	68
QS72225	1K x 18 Parallel Synchronous	64
Clocked x36 FIFOs		
QS723611	512 x 36 x 2 Bidirectional Clocked FIFO with Dynamic Bus Sizing	144
QS723620	1K x 36 Clocked FIFO with Dynamic Bus Sizing	132
QS723621	1K x 36 x 2 Bidirectional Clocked FIFO with Dynamic Bus Sizing	144
QS725420A	256 x 36 x 2 Bidirectional Clocked FIFO	132, 144

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PRODUCT FEATURE

Security Processors Are Capable Of Plugging Leaks In LANs, Cable, And CPUs

A family of embedded security processing chips brings affordable, hardware-based, data security to modems, web browsers, and set-top boxes, plus computers and their associated peripherals. The first two members are the VMS310 NetArmor general-purpose encryption processor and the VMS230 GhostRider PCI-bus encryption/decryption engine. Both employ on-chip key creation, storage, and encryption/decryption, making them much more secure than conventional software-based solutions.

The VMS310 NetArmor data-security processor is a flexible, single-chip device that can perform many functions, including DES encryption, access control, firewall building, digital signature processing, data authentication, certificate generation, and key management. Communications interfaces simplify integration into PCI-based systems, as well as PCMCIA and add-in cards.

Its architecture is based on an ARM RISC processor core, combined with data security, memory, and communication interface circuitry. On-chip security components, including a DES engine, multiplier/exponentiator, SHA hash engine, a secure ROM, and encrypted external memory and PCMCIA interfaces assure that only encrypted data is available outside the chip. On-chip memory stores the user ID, the chip's internal operating system, and encrypt/decrypt keys.

The VMS230 GhostRider is a security engine that includes a PCI bus interface, making it ideal for use in computers, modems, Web appliances and set-top boxes, and other PCI-based devices. To prevent unauthorized tampering, all off-chip data exchanges are secure, including data transfers across the PCI bus, to its associated peripherals and memory.

The VMS230 consists of four primary sections—the crypto section, the input data handler (IDH), the interface section, and the I/O section. Also incorporated are RSA key encryption and DES for unique key management functions and protocols with multiple data encryption capability via the master/slave PCI bus.

The VMS310 will sample in early 1997, with full production in the third quarter. Pricing is $50 in lots of 10,000. Contact Dave Auer at (602) 752-6308, or at dave.auer@tempe.vlsi.com.

The VMS23 is sampling now, with production early in 1997. Pricing is $25 in lots of 50,000. Contact Joe Wallace at (602) 752-6246, or via e-mail at joe.wallace@tempe.vlsi.com. *LG*

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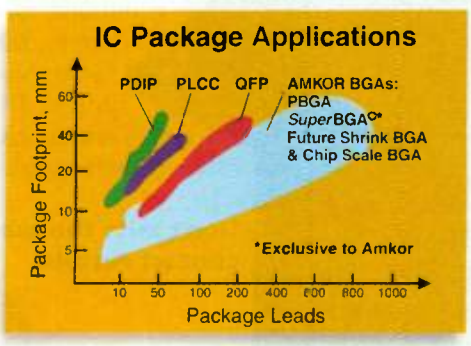

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PIPS

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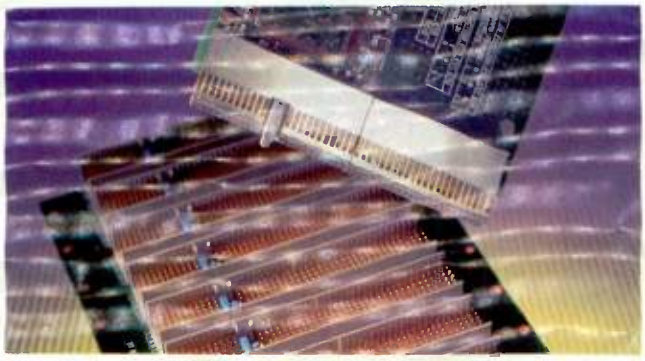
High-Performance Connectors—The Often-Underestimated Weak Link

In an era of increasing speed and complexity, designers must perform careful characterizations of available connector options.

Roland Mödinger
ERNI Elektroapparate GmbH, Seestrasse 9, D-73099 Adelberg, Germany 011-49-7166-50284

Michael Munroe
ERNI Components Inc., 12701 North Kingston Ave., Chester, VA 23831 (804) 530-5012



The engineer who understands how the connector will behave in the circuit will get products to market more quickly, and with fewer surprises.

To answer the call for faster systems with ever-increasing I/O rates, manufacturers are revamping older bus structures such as the VMEbus, while developing new bus structures such as the CompactPCI. As a result of these faster data rates, it is more important than ever to hone the interconnect path by focusing on possibly its weakest link—the connector. Because connectors affect both the performance and characteristics of the interconnect path, it is essential for engineers to make more precise measurements to confirm the simulation model used in circuit design. It is important to review the measurement fundamentals, and how basic characteristics are derived from the relevant formulas. Armed with this information, the necessary measurements can then be taken to provide the basis for the verification of a connector SPICE simulation. For this purpose, two popular connector systems will be examined: the older, high-density (HD) 160-pin DIN connector and the 2-mm hard-metric (HM) connector that is used to handle larger numbers of signals and higher frequencies.

Due to the stringent performance demands of higher signal frequencies and data rates, the short electrical length of connectors in the signal path can no longer be ignored. Good electromagnetic compatibility (EMC) and RF performance must be part of the design criteria of all components within the signal path. The key parameters affecting the RF performance of the connector system are: capacitance, inductance, characteristic impedance, signal propagation delay, differential time delay (skew), reflections, phase shift, crosstalk, and shielding efficiency.

Special test boards, made from standard FR-4, were built with pseudo-coaxial layouts *(Fig. 1)*. The signal traces were implemented using 50-Ω stripline construction. SMA connectors were installed for injecting signals and connecting test equipment. Various configurations of ground pins, unused pins, and driven pins were examined *(Fig. 2)*.

Two fundamentally different measurement methods—time domain and frequency domain—were used to measure the parameters. Variable analog frequencies were used for the measurements in the frequency domain. In addition, a network analyzer, a signal generator with a spectrum analyzer, and a Wheatstone bridge arrangement measured capacitance, inductance, reflections, and crosstalk.

In general, digital signals with very fast rise-times are used for time-domain measurements, with a time-domain reflectometer (TDR) as the measuring instrument. This method obtains the characteristic impedance curve and the signal propagation delay.

The digital signals change state very rapidly (in the region of picoseconds), and produce a frequency spectrum that extends up to 20 GHz (due to the edge-rate effect). As a result, the measuring setup must meet tight

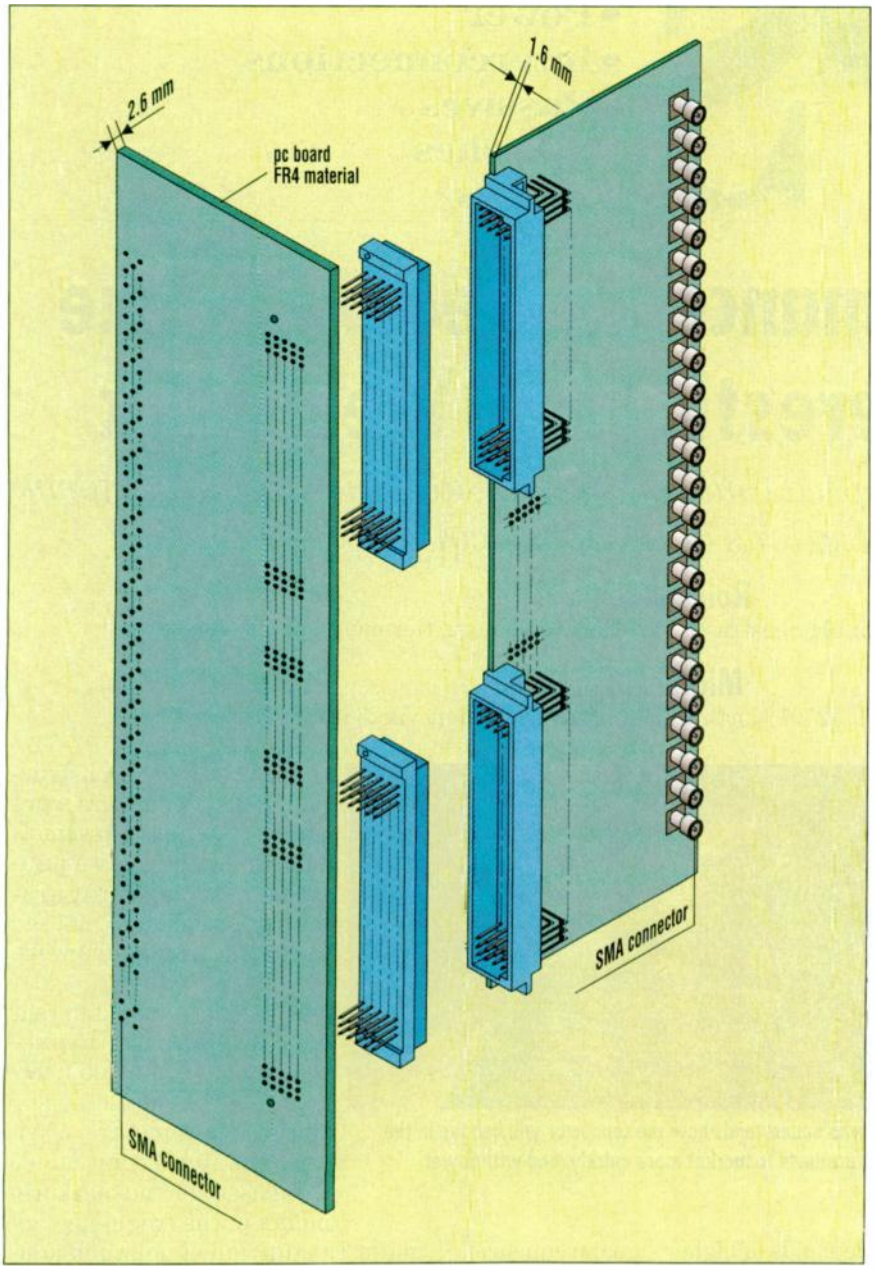


Fig. 1: RF measurements on connectors were made using a printed-circuit test board made from FR4 material. The signal traces were implemented using 50-Ω stripline construction and SMA connectors were installed for injecting signals and connecting test equipment.

specifications or spurious effects may substantially corrupt the results. In addition, the RF behavior of the connector also is a function of the signal's rise time. For sinusoidal signals, the frequency is easily determined. For digital signals, the equivalent analog frequency spectrum must be calculated. Fourier analysis can be used, and the following approximation is appropriate:

$$f_{An}(MHz) = 5 \times f_{Dig}(MBit/s)$$

or

$$f_{An}(MHz) = \frac{350}{T_r(ns)^*}$$

*Tr = rise time

Analyzing Parameters

Capacitance and inductance are the two key quantities which determine the characteristic impedance. The characteristic impedance is an important factor when considering the RF behavior of connectors.

The capacitance of a parallel-plate capacitor is given by the following formula:

$$C = \frac{A \times \varepsilon_r \times \varepsilon_0}{s}$$

Where A is the surface area, ε_r is the dielectric constant, 0 is the electric constant (permitivity of free space), and s is the distance between the plates. Therefore, the smaller the distance between the plates and the greater the area of the plates, the larger the capacitance. Additionally, the capacitance is directly proportional to the dielectric constant (air = 1). Crosstalk in connectors is caused by, and directly proportional to, the coupling capacitance.

The inductance (L) of a straight, round conductor is given by the following formula:

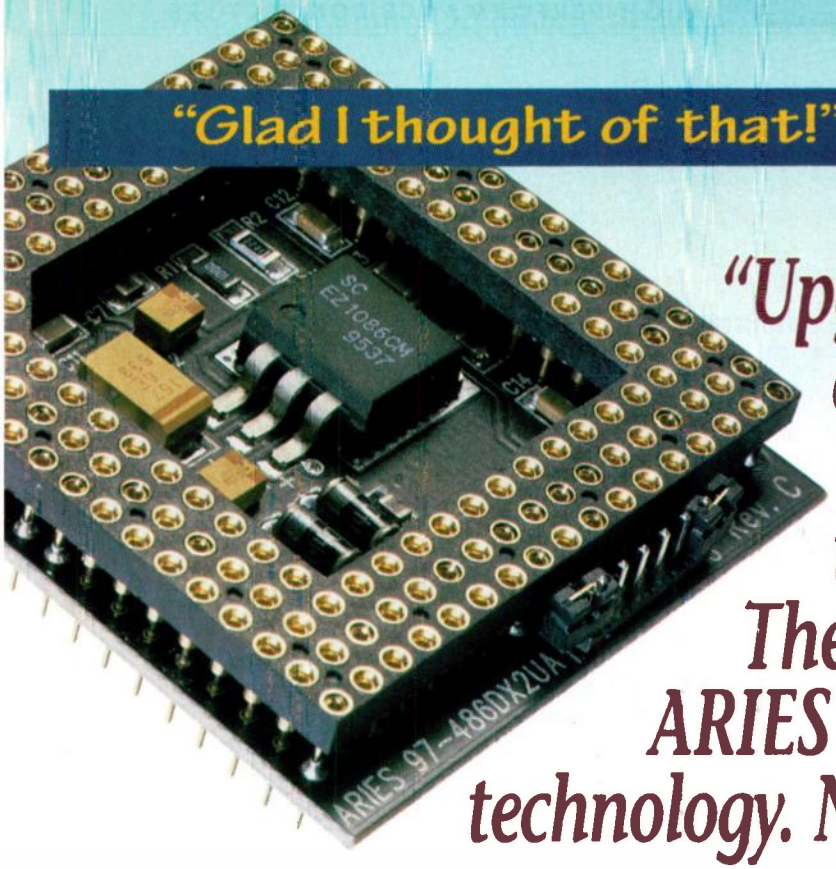
$$L = \frac{\mu}{2\pi} \times I \times \left(\ln \frac{2I}{r} - 3/4 \right)$$

One basic point is that the inductance increases as the length of the conductor increases, while it decreases with increasing conductor cross-section. An inductance of 8 to 10 nH/cm can be assumed to be as constant as possible over its entire length as it determines the characteristic impedance curve. Any abrupt impedance changes or discontinuities will cause reflections. Inductance in the ground path (ground bounce) plays an important role in signal transmission through connectors featuring a large number of contacts. The effect of this inductance can be reduced by increasing the number of signal lines that are used as a ground connections through on the connector. This lowers the total inductance in the connector's ground path, reducing interference at high data rates.

Characteristic Impedance

As mentioned previously, the characteristic impedance of a conductor is a function of its inductance and capacitance, and can be defined as the line impedance seen by a current that is varying with time (signal).

At high frequencies, this can be approximated as:



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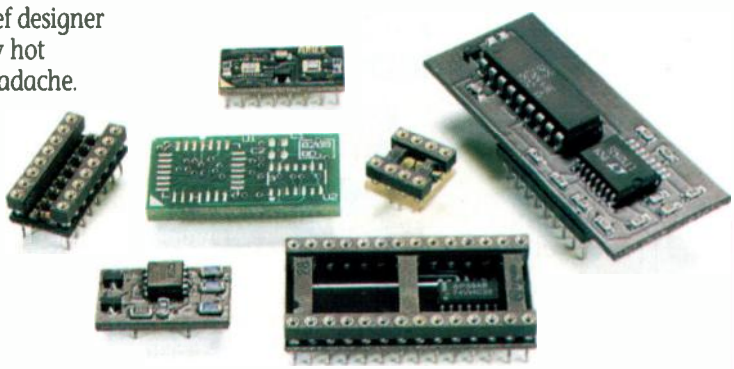

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In other words, the lower the capacitance C, and the higher the inductance L, the greater the characteristic impedance, and vice versa. If substitutions for capacitance and inductance are made in the impedance formula, an important expression for discussing pseudo-coaxial arrangements can be obtained. The smaller the separation between the signal and the ground contacts, or the larger the surface area between the signal and the ground contacts (for example, higher capacitance), the lower the characteristic impedance. Conversely, the characteristic impedance increases as the conductor cross-section decreases (due to higher inductance).

These interrelationships are important when interpreting the impedance characteristic of connector assemblies, and must be taken into consideration when designing connectors. As far as crosstalk is concerned, the lower the characteristic impedance of neighboring lines, the lower the crosstalk. However, in the case of bus systems, the lower limit is determined by the driver power of the bus driver ICs.

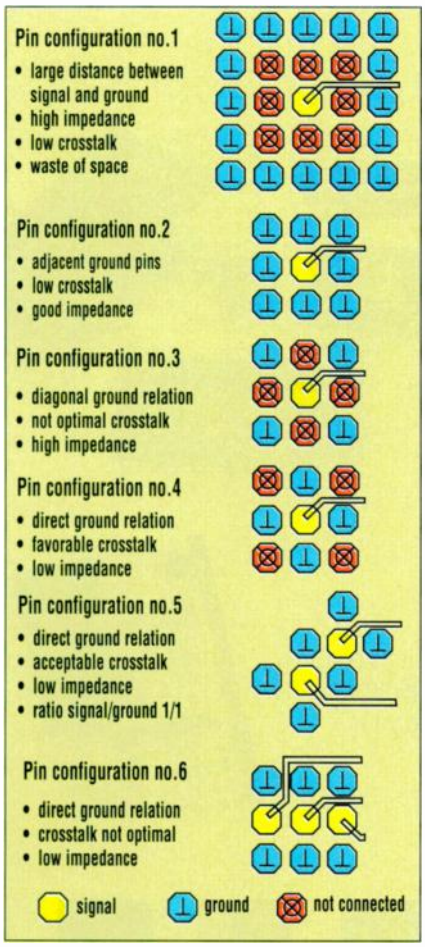

Fig. 2: Various configurations of ground pins, unused pins, and driven pins were examined to find the optimum layout.

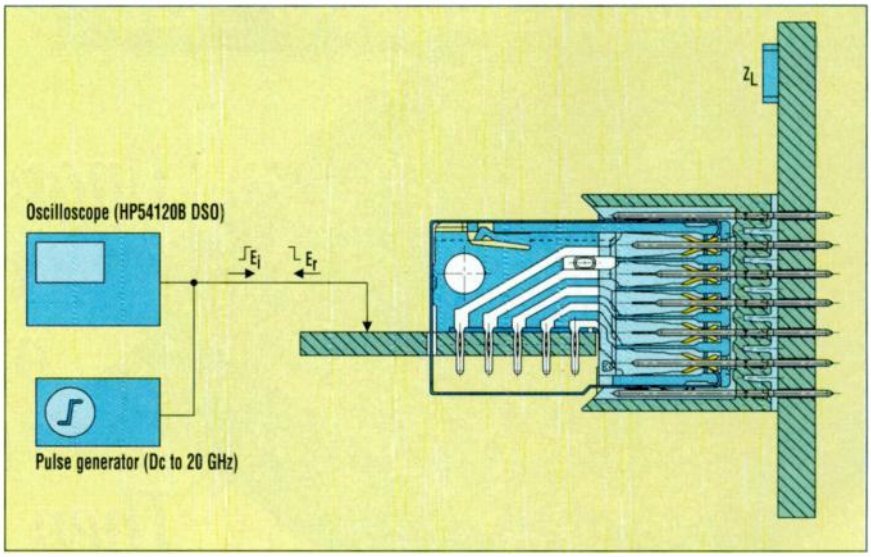

Fig. 3: The impedance characteristic, signal propagation delay, and skew were determined using TDR with an HP 54120B DSO, a four-channel step generator (dc to 20 GHz, HP 54121A), and terminating resistors, in addition to a special-purpose test adapter for connector assemblies.

Using a TDR to measure the characteristic impedance curve involves applying a very high-speed digital pulseto the device-under-test. Some of the leading edge of this pulse is reflected back to the measuring head whenever it encounters a discontinuity in the characteristic impedance, such as conductor bends or changes in diameter/ shape of the conductors within the connector. The characteristic impedance along the line is then calculated, with reference to an impedance (50 Ω), from the reflected magnitude of the injected signal. The measuring system's resolution is determined by the dielectric constant and, crucially, by the rise time of the pulse. The propagation speed of the measurement pulse is given by:

$$v_t = v_c / \sqrt{\varepsilon_r}$$

Consequently, the resolution, x, is given by:

$$X = v_t \times t_r / 2$$

or

$$X = (v_c \times t_r) / (2 \times \sqrt{\varepsilon_r})$$

A rise time of 35 ps was used for the above measurements, giving a resolution of approximately 3 mm.

The signal propagation delay and skew values for the various connector styles also were recorded with a TDR. The TDR plots indicate twice the propagation delay (including reflection) for any given signal path. Reflections can be described by various characteristic values: reflection coefficient, return loss, and the VSWR (voltage standing wave ratio). The reflection coefficient is the ratio of the reflected and incident energy at an unmatched transition point, and is equal to the ratio of the impedances (r = (Z-Z)/(Z+Z)). The return loss is the log of this ratio a= -20log r.

A standing wave is produced when the reflected and incident waves are superimposed, and the VSWR is the difference between the maximum and the minimum wave energy. The VSWR can be calculated from the reflection coefficient using the following formula:

$$VSWR = \frac{1+r}{1-r}$$

The reflection not only depends on changes in impedance, but also on the

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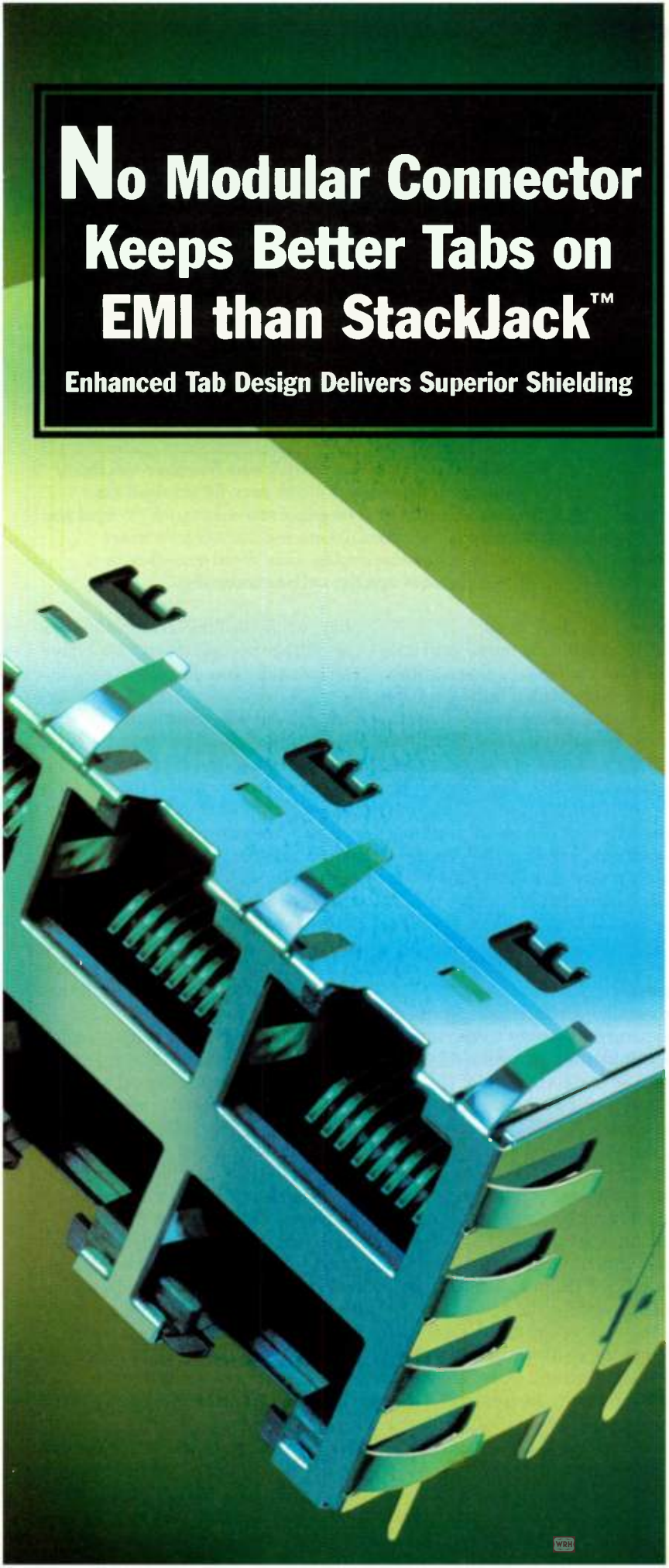

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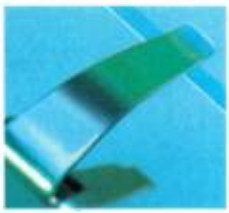

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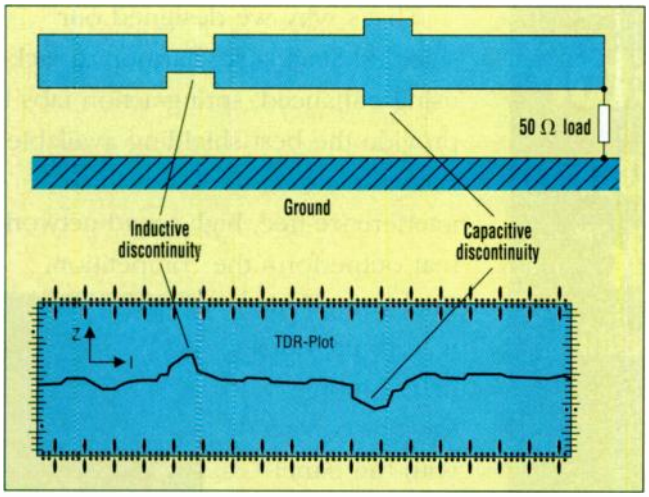


Fig. 4: A TDR profile of a microstrip line with abrupt changes in characteristic impedance clearly indicates the inductive and capacitive discontinuities and their effect on the TDR plot. The trace of the reflected voltage is shown on the DSO.

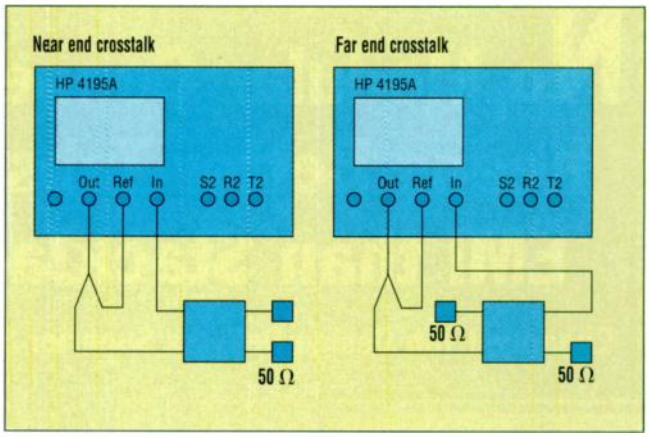


Fig. 5: Both near- and far-end crosstalk were determined with slightly differing measurement setups. In both cases, the test signal was applied to the pc board. In the case of near-end crosstalk the signal was measured on the pc board. The near-end crosstalk is the sum of capacitive and inductive coupling, while far-end crosstalk is the difference between capacitive and inductive coupling.

length of the discontinuity. A digital signal is not affected by a discontinuity if the edge's transit time is short (approximately <1/25) in relation to the signal's rise time.

The parameters of crosstalk and shielding are discussed in greater detail in the description that follows, however, inductance and capacitance also produce a phase shift between current and voltage. In addition, in the case of connectors, the capacitive effects are much greater than the inductive effects.

Measurement Setup

All measurements were conducted with the test pc boards described earlier for the various pseudo-coaxial configurations. For measuring capacitance and inductance, a network/impedance analyzer, an impedance adapter, and a special-purpose test adapter were used. Capacitance and inductance were measured from 50 to 500 MHz. The measured values for f = 100 MHz are compared in the following evaluations. The characteristic impedance was calculated from the formula Z = L/C. The impedance characteristic, signal propagation delay and skew were determined using the TDR. The TDR was used with an HP 54120B digital storage oscilloscope (DSO), a 4-channel step generator (dc to 20 GHz, HP 54121A) and terminating resistors, in addition to a special-purpose test adapter for connector assemblies *(Fig. 3)*.

A TDR profile of a microstrip line with abrupt changes in characteristic impedance clearly indicates the inductive and capacitive discontinuities and their effect on the TDR plot *(Fig. 4)*. The trace of the reflected voltage is shown on the DSO. The TDR profile makes it possible to determine not only the impedance characteristic, but also the propagation delay as well as the skew. The specified propagation delays relate to the signal's forward and return journey.

Crosstalk

Crosstalk is defined as the ratio of the measured voltage to the signal voltage, and can be expressed in percentage or in dB (the log of this ratio). To measure crosstalk, a pulse generator (HP 8657B), a spectrum analyzer (HP 8562A) or network/impedance analyzer (HP 4195), power divider, and terminating resistors (50 Ω), in addition to a special-purpose test adapter were used. Both near-end and far-end crosstalk were determined with slightly differing measurement setups *(Fig. 5)*.

In both cases, the test signal was applied to the pc board. In the case of near-end crosstalk, the signal was measured on the pc board. In the case of far-end crosstalk, the signal was measured on the backplane. The near-end crosstalk was the sum of the capacitive and inductive coupling, while the far-end crosstalk was the difference between capacitive and inductive coupling.

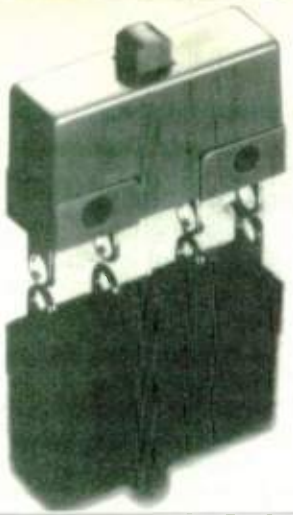
Results And Evaluation

The measurement results for a specific pseudo-coaxial pin configuration for the 2.54-mm HD 160-pin DIN connectors and the 2-mm HM connectors are shown in Figures 6(a) and (b), respectively. The signal pin is surrounded by ground pins in a pseudo-coaxial array. This design provides a direct ground reference.

The configuration is characterized by a signal-to-ground ratio of 1:1, a low characteristic impedance, and acceptable crosstalk values.

In comparing the measured values for the HD 160-pin DIN connectors and the 2-mm HM connectors, the differences are already very clear at a frequency of 100 MHz *(Fig. 7)*. The characteristic impedances show the various TDR plots for the same pin configuration for two different connectors. The impedance fluctuations in the area of connectors differ greatly. For example, while the impedance of the HD 160-pin DIN connector fluctuates between approximately 53 and 100 Ω, the 2-mm HM connector features a very smooth characteristic impedance curve.

The 2-mm HM connector also showed very good results for propagation delay and skew. The plots clearly indicate the influence of vias which cause abrupt impedance



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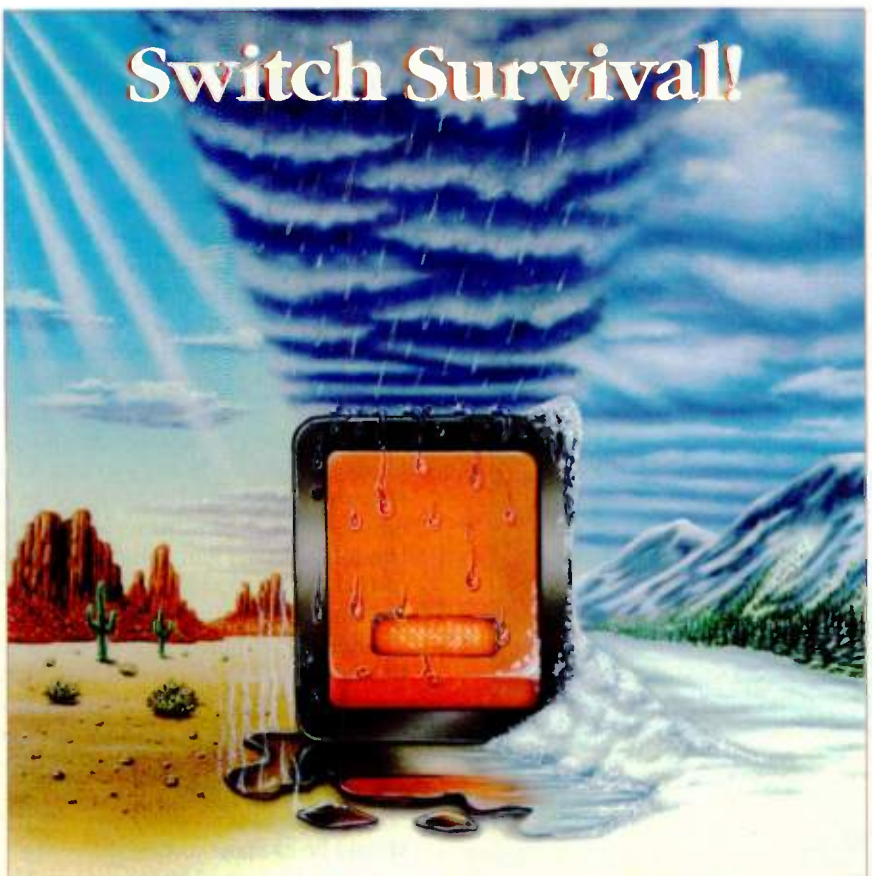

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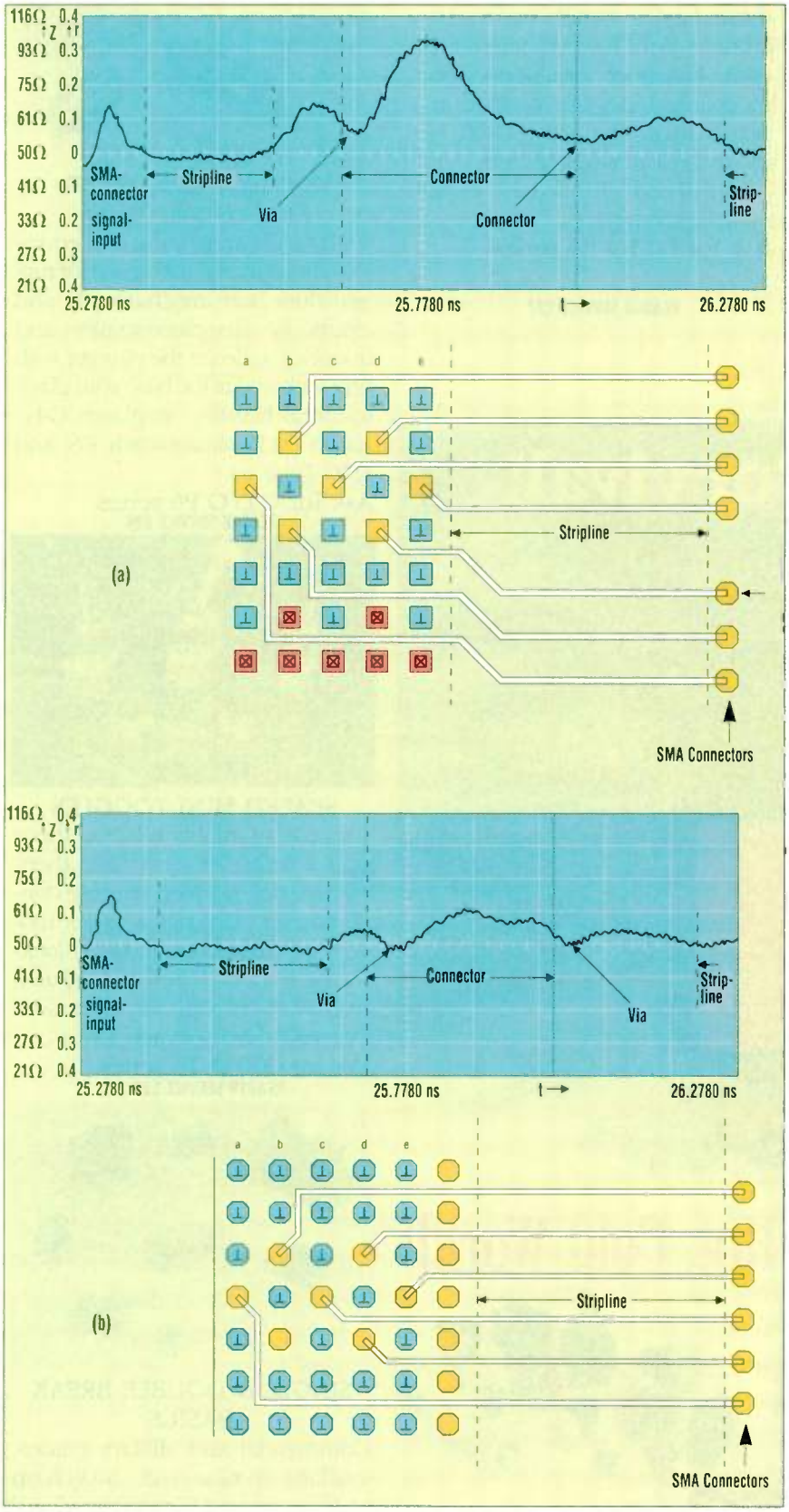

Fig. 6: The TDR plots for the same pin configuration (at 100MHz) for the the HD 160-pin DIN (a) and the 2-mm HM (b) connectors show that the impedance fluctuations in the area of connectors differ greatly. The plots also clearly indicate the influence of vias which cause abrupt impedance changes that are quite large.

changes that are quite large.

The measurements assessing the effect of shielding on crosstalk indicated that only a relatively slight influence was detected in the impedance-matched signal lines (pseudo-coaxial structure). The shielding acts specifically on the outer rows. With the various pseudo-coaxial structures, it was possible to decrease the crosstalk by 20 to 30% by using shielding. For signal contacts without impedance matching (i.e. no ground pins), the crosstalk was reduced by as much as 120%.

Conclusions

These results allow for some general requirements applicable to all connectors and pc boards for RF signal transmission:

- The connectors should have an impedance as close to 50 Ω as possible, and as low a capacitance as possible at the terminals. It can be seen that the impedance is up around 93 Ω, then down to 61 Ω *(Fig. 6, again)*.
- Importance must be attached to consistent mechanical geometries and consistent conductor cross-sections. Impedance is reached at a spike and the curve is smooth *(Fig. 6, again)*. These conditions are due to the uniform mechanical dimensions of the contact cross section within the connector path.
- All signal paths within the connector should have approximately the same length to avoid signal propagation skew, hence the serpentine contact path for the 2-mm HM connector *(Fig. 3)*.
- All blades, beams, and tails should be as short as possible.
- For right-angle connectors, the contacts should be embedded in plastic with no variation in the dielectric. Typically, HD 160-pin DIN connectors have contacts in open air, while the 2-mm HM connector has the right-angle leads within the plastic. This arrangement is responsible for the bottom end of the curve dropping down as it approaches the via *(Fig. 6)*.
- Any abrupt discontinuities in the signal path must be eliminated. The design and geometry of the contacts themselves can have a substantial influence on performance.

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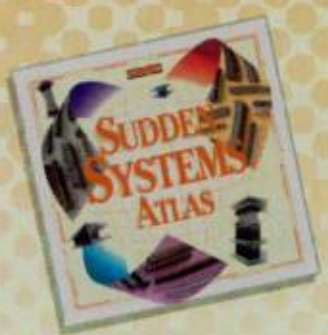

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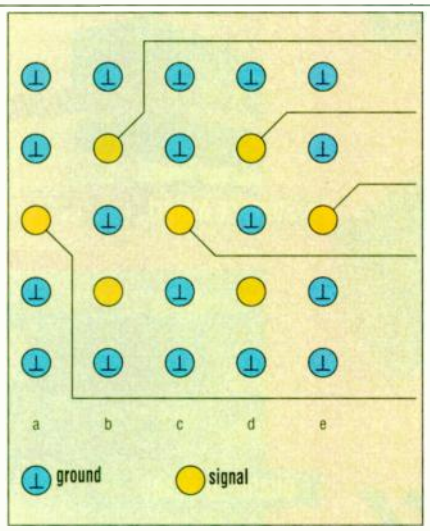
pc board itself affect the RF characteristics. These include, the trace geometry, the pc board's dielectric layer construction, capacitance of the via design, and power and ground plane spacings. Ground leads and grounding surfaces also should have a low impedance. Other requirements include proper termination design, trace isolation, and minimum stub lengths. Besides selecting a suitable pc-board laminate, it also is necessary to ensure compliance to the design tolerances during lamination, etching, and plating.

All of the above factors contribute to the electrical characteristics of the interconnect path, but it is important to realize that they all are within the control of the designer—with the exception of the signal path within the connector itself. This path has a fixed geometry, and its effect can either complement or degrade the interconnect system. For this reason, it is essential that the connector be fully characterized and chosen carefully for its intended application. The engineer who understands how the connector will behave in the circuit will get products to market more quickly, and with fewer surprises.

Proir to joining ERNI Elektroparate GmbH as an engineer in 1991, Roland Modinger was with ERNI's sister company, Regletron (Adelberg, Germany). At Regletron, Mr. Modinger was involved in software and hardware design. Before joining the ERNI Group, he was an engineer with Bosch Telecommunications in Germany.

Michael Munroe joined ERNI USA in 1995 as product manager for the ERmet 2-mm HM connector line. Currently, Mr. Munroe is responsible for evaluating new products for the VME and CompactPCI industry. Prior to joining ERNI, Mr. Munroe was Strategic Marketing Manager at Hybricon Corp.

How Valuable	Circle
Highly	549
Moderately	550
Slightly	551

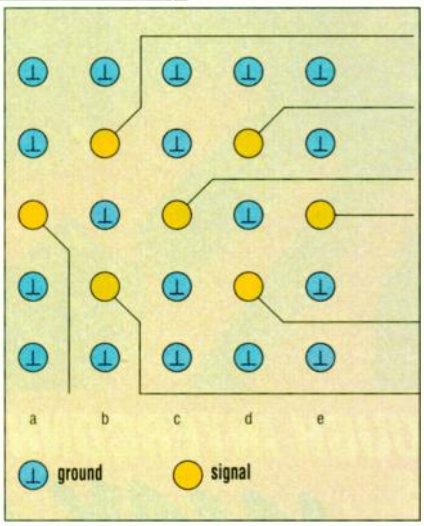


The measurement values in the table below are based on this pin configuration

Parameter	Connector pin row				
	a	b	c	d	e
Capacitance C (f =100 MHz)	2.5 pF	2.8 pF	2.9 pF	3.1 pF	3.2 pF
Inductance L (f = 100 MHz)	6.8 nH	7.6 nH	8.3 nH	8.7 nH	10.5 nH
Characteristic impedance	52 Ω	52 Ω	53 Ω	53 Ω	57 Ω
Propagation delay*	111 ps (86) ps	119 ps (94) ps	126 ps (101) ps	141 ps (116) ps	157 ps (132) ps
Signal skew	8 ps	9 ps	14 ps	15 ps	
	maximum 46 ps				
Crosstalk (f = 100 MHz)	← 57 dB →				
			← 53 dB →		
Reflection factor (50 Ω and f = 100 MHz)	0.02	0.02	0.03	0.03	0.065
VSWR (f = 100 MHz)	1.04	1.04	1.06	1.06	1.14
Reflection loss (f = 100 MHz)	34 dB	34 dB	30.5 dB	30.5 dB	24 dB

* The higher value of the propagation delay is measured from solder-side to solder-side. The value in parenthesis is calculated from component-side to component-side.

5 row 2mm HM connector



The measurement values in the table below are based on this pin configuration

Parameter	Connector pin row				
	a	b	c	d	e
Capacitance C (f = 100 MHz)	2.8 pF	3.05 pF	3.2 pF	3.3 pF	3.4 pF
Inductance L (f = 100 MHz)	8.8 nH	9.8 nH	12.7 nH	14.0 nH	17.0 nH
Characteristic impedance	56 Ω	57 Ω	63 Ω	65 Ω	70 Ω
Propagation delay*	126 ps (101) ps	145 ps (120) ps	161 ps (136) ps	176 ps (151) ps	193 ps (168) ps
Signal skew	19 ps	16 ps	15 ps	17 ps	
	maximum 67 ps (row a to row e)				
Crosstalk (f = 100 MHz)	← 48 dB →				
Reflection factor (50 Ω and f = 100 MHz)	0.056	0.065	0.115	0.13	0.166
VSWR (f = 100 MHz)	1.12	1.14	1.26	1.3	1.4
Reflection loss (f = 100 MHz)	25 dB	24 dB	19 dB	18 dB	15.5 dB

* The higher value of the propagation delay is measured from solder-side to solder-side. The value in parenthesis is calculated from component-side to component-side.

5 row DIN 41612 connector

Fig. 7: Measured values for a frequency of f = 100 MHz.

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Recent Advances In Rechargeable Batteries

Knowledge Of Battery Chemistries And Their Pros And Cons Goes A Long Way Toward Optimizing Designs For Portable Systems.

DR. PNINA DAN, Tadiran Electronic Industries Inc., 2 Seaview Blvd. Suite 102, Port Washington, NY 11050; (516) 621-4980.

The rapid growth of portable electronics, from notebook and palmtop computers to cellular telephones, has put the rechargeable batteries used to power these devices squarely in the spotlight. Although most designers consider batteries relatively "low tech," a number of breakthroughs have taken place that have considerably extended their operating life and power output. Ignoring these advances could seriously compromise a design's chances of success in a time where weight, capacity, volume, and cost must be fully optimized. This is especially true where portable computer and wireless communication devices are concerned.

Along with advances in the relatively old nickel-cadmium (NiCd) battery, a number of newer secondary battery contenders have appeared to pick up where NiCd runs out of steam. These include nickel-metal hydride (NiMH), lithium polymer (Li-Poly), lithium ion (Li-Ion), and lithium metal (Li-Metal). While no single rechargeable battery type can satisfy all requirements, making the proper tradeoffs during the battery selection process can go a long way towards optimizing system performance.

With respect to NiCd, the introduction of sponge-metal electrode technology a few years ago boosted NiCd cell volumetric efficiency to 150 Wh/liter, and energy density to 50 Wh/kg. NiCd battery technology has achieved approximately 30% of its theoretical maximum energy density. Self-discharge rate (the rate at which the battery loses charge while not in use) for this well-known and mature technology is moderate, compared to other types. The self-discharge rate can become an issue for end users who use a particular portable system infrequently, yet want to use it when necessary. Charging circuits for NiCd batteries are relatively simple and rapid, although care must be taken to avoid long periods at high temperatures during charging. Because NiCd batteries contain cadmium, an environmentally hazardous substance, their disposal is becoming controversial. This has spurred research into the other technology alternatives.

One of these alternatives is NiMH. These batteries offer increased volumetric efficiency—230 Wh/liter—over even the most advanced NiCd types and have replaced NiCd as the battery technology of choice for many applications. This technology has reached approximately 20% of its maximum theoretical energy density. Energy density is better than that of NiCd at 70Wh/kg. Open-circuit voltage for NiMH cells is 1.20 V, identical to that for NiCd cells. This latter factor has encouraged some designers to use NiMH batteries as "drop-in" replacements for NiCd packs. However, NiMH cells cost significantly more than NiCd cells (up to 50% more, depending on form factor) and require special charging circuits that are substantially different than the relatively simple ones used for NiCd (charging time, rate, and temperature must be accurately controlled).

NiMH batteries also have the highest self-discharge rate of any of the types discussed here. Self-discharge is caused by a combination of residual hydrogen reacting with the positive electrode and the reversible decomposition of the positive electrode. The self-discharge rate depends on the temperature at which the battery is stored or left unused (the higher the temperature, the greater the self-discharge rate). The loss of capacity due to self-discharging is reversible, and full capacity can be restored by cycling through several charge/discharge cycles.

NiMH cells do not contain any hazardous substances. Therefore, disposal is not an issue. Most cells are based on (in addition to nickel) alloys of titanium, zirconium, vanadium or chromium. There also has been some experimentation with the rare-earth element lanthanum. These cells do not exhibit the memory effect associated with NiCd types. However, a NiMH battery will exhibit a "voltage depression" phenomenon if it is repeatedly recharged after being only partially discharged. Several such cycles will result in a lower open-circuit voltage at full charge, caused by physical changes in the battery ma-

TABLE 1. A COMPARISON OF RECHARGEABLE BATTERY TECHNOLOGIES (AA-SIZE CELL)

Chemistry	Average operating voltage (V)	Energy density (Wh/kg.)	Volumetric efficiency (Wh/liter)	Cost ($Wh)	Memory effect	Self-discharge rate (%/month)	Environmental concerns	Operating-temperature range (°C)
NiCd	1.20	45	150	0.75 to 1.5	Yes	25	Yes	-10 to 50
NiMH	1.20	70	230	1.5 to 3.0	(see text)	20 to 25	No	-10 to 50
Li-Poly*	1.8 to 3.0	70 to 100	25 to 40	N/A	No	20	No	-20 to 50
Li-Ion	3.6	100	225	2.5 to 3.5	No	8	No	-20 to 50
Li-Metal	3.0	140	300	1.4 to 3.0	No	1 to 2	No	-30 to 55

**Li-Poly cells, to date, are not available in standard sizes.*

terials. Consequently, it appears that the cells "remember" the lower-voltage level. However, a few complete discharge/recharge cycles will restore normal operation.

Rechargeable Lithium

Newer lithium-based rechargeable battery systems have overcome the safety and environmental obstacles posed by early efforts and are, in general, the most efficient rechargeable types available. The two lithium-based rechargeable battery systems commercially available today are Li-Ion and Li-Metal. A new Li-Poly system is still under development and is briefly described below. While all three types exhibit the overall advantages of lithium-based systems, they differ in some important respects specifically related to portable applications.

Li-Poly

Li-Poly batteries are still in the early developmental stages, although there are at least two companies that are commercializing the technology. The system is based on organosulfide polymer electrode material developed by Lawrence Berkeley Laboratory (Berkeley, CA) and proprietary polymer materials developed by various commercial companies. The cells consist of layers of insulating material, a lithium foil anode, an electrolyte layer, a polymer cathode and a metal foil layer to collect current. The technology promises energy densities of 200 Wh/kg. from an essentially solid-state system. The cells can be manufactured with relative ease, as they consist mainly of sheet materials that are amenable to the high-capacity "roll-to-roll" processes of the plastic sheeting industry.

Li-Ion

Li-Ion rechargeable batteries were first introduced in small video camcorders and are now seeing use in other portable applications, especially laptop computers. The relatively high voltage (3.6 V) of the Li-Ion cell offers the advantage of fewer cells being required to achieve a given voltage. One major drawback to Li-Ion technology is its relatively high cost/performance ratio. The cost per watthour (Wh) of a Li-Ion cell is significantly higher than that of other types, but some performance figures are not in proportion *(Table 1)*. For example, the volumetric efficiency of a Li-Ion cell is significantly less than that of a Li-Metal cell and only slightly better than that of a Ni-Cd cell. Energy density is approximately 50% better than NiMH, but at a potentially greater cost penalty. Energy density also is 36% below that of Li-Metal. Present Li-Ion technology has achieved 18% of its theoretical maximum energy density.

TABLE 2. A COMPARISON OF TECHNOLOGIES THAT MAKE UP A 6-V CELL-TELEPHONE BATTERY PACK

Chemistry	Number of cells	Voltage (V)	Capacity (Ah)	Weight (g)	Volume (ml)
NiCd	5	6	1.0	104	40
NiMH	5	6	1.2	104	40
Li-Ion	4	7.2	0.8	72	32
Li-Metal	4	6	1.6	68	32
Li-Metal	2	6	0.8	34	16

Another shortcoming of the Li-Ion system is its primarily nonlinear discharge characteristic. Typically, an AA-sized Li-Ion battery, discharged at a rate of 250 mA, will drop in voltage from 4.1 V (fully charged) to approximately 3 V in about 90 minutes. The voltage will remain at 3 V for the next 90 minutes, and then drop off rapidly to the 2-V level, where the battery is considered discharged. Depending on the design, this characteristic can be troublesome in some portable applications that require a minimum voltage for operation—cellular telephones, for example.

To avoid overcharge or overdischarge a protective circuit is required inside each battery to limit charging voltage to a safe level (between 4.1 and 4.2 V, depending on the manufacturer), as higher voltages could damage the cells. The charging process for Li-Ion batteries comprises a constant-current limit and then a transition to a constant voltage limit that should be held within ±1%. A discharge "floor" of 2.7 to 3.0 V must be accounted for in any capacity-monitoring circuitry. Discharging any lower could damage the cells and reduce the number of useful charge/discharge cycles.

In general, Li-Ion batteries require very accurate capacity monitoring circuitry, usually involving a low-value (approximately 0.02 Ω) series "sense" resistor, analog-to-digital conversion, and a microcontroller. But even the most carefully designed battery monitors can be fooled if the Li-Ion battery being monitored has lost capacity due to self-discharge.

Li-Metal

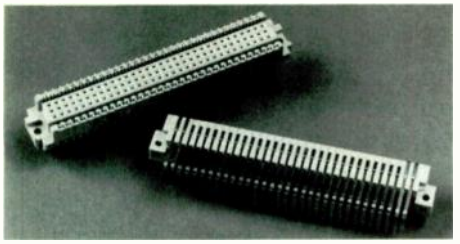
Recently developed rechargeable Li-Metal ($Li/LixMnO_2$) batteries offer energy density and volumetric efficiency unmatched by any other battery type. Energy density for the new batteries is 140 Wh/kg., and volumetric efficiency is 300 Wh/liter. Li-Metal batteries have the highest theoretical maximum energy density (nearly 900 Wh/kg.)—achieved only 13% thus far in commercially available cells.

Li-Metal cells are entirely safe and are immune to almost all types of physical or electrical abuse conditions, including internal or external short-circuit, overcharge, overdischarge, overheating, puncture, or crushing conditions. The increase in safety is due primarily to a fail-safe, self-quenching electrochemical system and a built-in safety vent.

Li-Metal batteries do not exhibit memory effect and have the lowest self-discharge rate of all rechargeable battery types. A typical Li-Metal battery stored at room temperature (70°F or 20°C) retains 85% of its capacity after one year. Operating temperature range (-30 to +55°C) also is greater than other battery types.

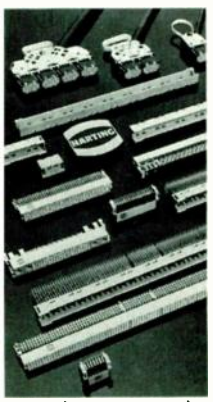
The discharge curve of these cells is practically flat. At a 250-mA discharge rate, after a brief (approximately 10-minute) drop from the fully charged voltage of 3.3 V, the voltage remains at 2.8 V for the remaining 80% of the discharge time, dropping off to 2 V (the "discharged" point) after that. This also means that when two cells are used in series (to create a battery with a nominal voltage of 6 V)

har-bus 64 New 160 Pin Connector For VME64



New connector series satisfies the new 64-bit computer architecture's requirement for higher speeds, more I/O and additional functionality. Qffering a five row connector solution that is 100% backward compatible with the popular 96-pin Eurocard connectors, the new ***har-bus 64*** has 160 pins with preleading contacts for live insertion. New contact rows can be used to improve signal speed of VME bus and as ground contacts. Current 96-pin Eurocard connectors mate to the 160 pin connectors, allowing all PCB's to be used in new or existing backplanes.

READER SERVICE 310



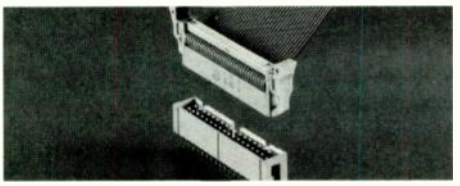
har-pak®2.5MM High Density Connector system

Developed for backplane and daughterboard applications in modern rack systems. The 5 row 2.5 mm connector design offers solderless PCB terminations, optimum utilization, of space three dimensional modularity, high contact density, EMI protection, and the ability to double-side surface mount components on daughter cards without loss of a 15mm card pitch. The *har-pak* connector system permits using a three dimensional 2.5mm grid. With the exceptional capabilities of the connector, only one connector style is required to solve your power, signal, ground, and high data rates, simplifying the design and manufacturing of future systems. The compliant pin technology utilizes the same 1mm plated through hole standard for many DIN 41612 compliant pin technologies.The consistency in design uses the many years of manufacturing and design experience already available. These attributes combined can lead to new advancements in board-level designs:15mm card pitch with double sided surface mounted daughter cards, butterfly or mid-plane techniques, modular design both horizontally and vertically, low number of system components combination with other standardized packaging systems, and lower applied costs.

READER SERVICE 311

New SEK "Press'n Snap" Press In Header

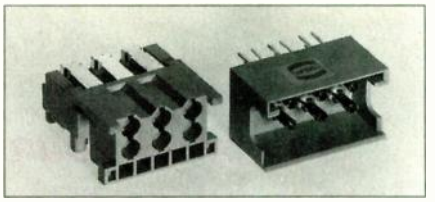
The new "press'n Snap" low profile press-in headers can be added to single or double-sided surface mount printed circuit boards any time after reflow. Press-in terminations of the two row .100" pitch headers permit easy installation into plated through holes without soldering. Removable temporary inserts allow any flat die to press the connectors. The straight header is shrouded by four plastic walls and available in versions from 6 to 64 contacts. The mating connectors are flat ribbon terminated socket connectors from HARTING's SEK range. These can be latched to the headers by using the locking levers installed onto the strain relief. The levers secure the socket connector to the end walls of the header. Placing the



locking levers on the socket instead of the PCB header saves valuable board real estate.

READER SERVICE 312

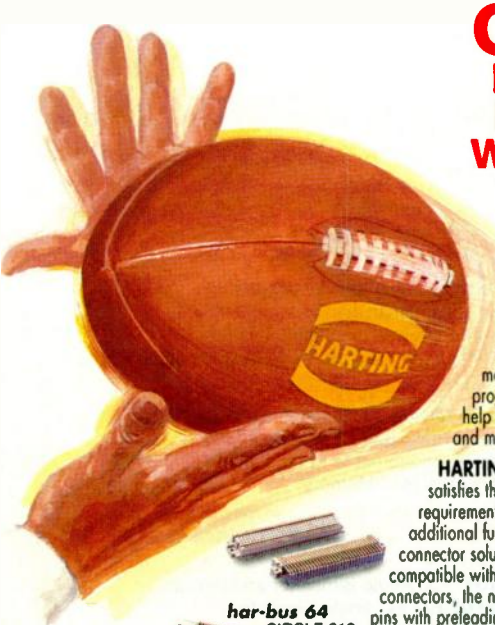
NEW HIGH DENSITY MICRO-COAXIAL CONTACTS



Designed for high speed data transfer rates. Can be used in the iec 1076-4-2 2.5mm High Density connector system, *har-pak®*. Provides more space efficiency, high frequency capability, easy handling, low applied cost and application with current equipment and emerging metric equipment practices. Designed for PCB termination on both daughter card to backplane connection; allowing users to bring signal directly into the backplane without a cable transition.

READER SERVICE 313

CONNECT FOR A WINNING PERFORMANCE WHEN IT COUNTS



Certified according to DIN ISO 9001

HARTING offers you winning solutions with a comprehensive line of high quality connectors that you can depend on for superior system performance.

HARTING's innovative designs, modern manufacturing facilities and progressive production techniques can help you stay ahead of the competition and maintain a decisive edge.

har-bus 64
CIRCLE 318

HARTING's *har-bus 64* connector series satisfies the new 64-bit computer architecture's requirement for higher speeds, more I/O and additional functionality. Offering a five row connector solution that is 100% backward compatible with the popular 96-pin Eurocard connectors, the new ***har-bus 64*** connector has 160 pins with preleading contacts for live insertions. New contact rows can be used to improve signal speed of VME bus and as ground contacts. Current 96-pin Eurocard connectors mate to the 160 pin connectors, allowing all PCB's to be used in new or existing backplanes.

har-mik har-press®
CIRCLE 317

The new ***har-mik har-press®*** SCSI 3 connector with compliant pins is flat rock, and can be inserted into a PCB with one stroke of a press. Eliminates soldering and saves time. The 68-pin, receptacle vertical mount connector is made of liquid crystal polymer, a high temperature resistant material which allows use of IR reflow for SMT components, with no danger of damaging the connector. Compliant pins fit into finished, plated through holes of 0.022" to 0.027".

har-pak®
CIRCLE 316

Need high pin count equal to the Future bus +4 row 2.0 mm connectors that can withstand robust handling and assembly? ***HARTING'S har-pak®*** 2.5 mm connector system with greater contact spacing provides superior high frequency performance.

Using the 0.040" plated through-holes typical of today's 0.100" connector, ***har-pak*** provides almost twice the density with no increase in manufacturing costs. All connectors are surface mount compatible, and ideal for high volume applications with solderless, compliant pin terminations.

Han-Modular
CIRCLE 315

HARTING's new ***Han-Modular*** System enables you to assemble a connector according to your specific requirements. Different modules permit transmitting electric signal, power, RF, coax, optical, pneumatic and liquid combinations in the same connector. High flexibility allows using combinations of different modules for different applications. System is ideal for use in assembly machines, factory automation, logistics, machine tools, railway and robotic applications.

Complete information available upon request

*You can rely on the same high quality, dependable performance and service that **HARTING** is known for Worldwide to make a winning connection for you.* ***Call, Fax or Write:***

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Hoffman Estates, Illinois 60195-5211
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READER SERVICE 314

the voltage remains above 4 V for the entire discharge cycle. The minimum operating voltage for many portable systems is 4 V, including many cellular-telephone models.

Li-Metal batteries are capable of delivering up to 2 A of current under continuous or pulse demand. The latter is especially important in cellular telephones, where in a typical 600-mW unit, current demands can jump from a standby current of 5 to 50 mA to a 0.6-ms "talk" pulse of 1.4 A with a 200-mA "floor" between pulses. Under these conditions, the mean "talking" current is 333 mA. A four-cell Li-Metal battery, with a capacity of 1600 mAh, can provide nearly four hours of talk time, combined with over 13 hours of standby time between recharges. This is accomplished in a four-cell battery pack that weighs only 68 g (2.4 oz.)—70% of the weight of an equivalent 6-V NiMH pack and approximately 60% of a Li-Ion pack. A comparison of rechargeable battery technologies in making up a 6-V battery pack for cell-telephone applications is shown *(Table 2)*.

Monitoring of the charge/discharge cycle of a Li-Metal battery is important, but is much simpler than the same task for a Li-Ion system. First, Li-Metal batteries need only be charged to a constant-current limit. A constant-voltage limit is not required. Second, in some applications (e.g., a two-cell series pack with a cut-off voltage of 5 V) cutoff voltage does not have to be monitored. The cost of Li-Metal batteries per watt-hour is nearly equal to that of NiMH batteries, making them the closest thing available today that meets the requirements of the lowest possible weight and highest possible capacity crammed into the smallest possible volume at the lowest possible cost.

Dr. Pnina Dan is director of research and development for rechargeable lithium batteries at Tadiran Battery Division, Rehovoth, Israel. She received her PhD in chemistry from the Weitzman Institute for Science, Rehovoth.

How Valuable	Circle
Highly	534
Moderately	535
Slightly	536

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MANUFACTURERS OF BOARD-LEVEL CONNECTORS

Manufacturer	Connector style	Contact/row spacing	Maximum pin density	Modular contacts	Number of contact rows	Functions other than signal lines	Max. insertion and min. withdrawal forces	Termination techniques used
Advanced Interconnections **West Warwick, R.I.** **Ann Cibelli, (401) 823-5200** **fax (401) 823-8723** **advintcorp@aol.com** **CIRCLE 660**	Pin and socket, SMT, BGA socket, QFP socket	0.100 in., 2 mm, and 0.50 in.	20/in.	Yes	32 by 32 (PGA, BGA)	End to end, side to side and vertical stacking, power connectors	Max. 500 g and min. 20 g	Press fit and solder
Andon Electronics Corp. **Lincoln, R.I.** **Ann Fortier, (401) 333-0388** **fax (401) 333-0287** **aecandon@aol.com** **CIRCLE 661**	Pin and socket headers	2.54 mm and 2 mm	2 to 40 position	No	Single or dual	N.S.	N.S.	N.S.
Beau Interconnect **Laconia, N.H.** **Sales Dept. (603) 524-5101** **CIRCLE 662**	Terminal, pluggable and fixed pc-board mount, rising clamp and screw terminal	3.5 mm to 12.7 mm	7.25/in.	Yes, on some styles	Two	Stacking, power, and polarizing	Approximately 200 g insertion, 150 g withdrawal	Solder
Circuit Assembly Corp. **Irvine, Calif.** **Monica Allphin, (714) 855-7887** **monica@ca-online.com** **http://www.ca-online.com** **CIRCLE 663**	IDC pc-board mount	0.075-in. center lines, 0.05-in. spacing	40/in., 80 contacts maximum	No	Four rows only	I/O and cable connections	N/A	IDC and solder combination
Comm Con Connectors Inc. **Duarte, Calif.** **Bob Farnum (818) 301-4200** **fax (818) 301-4212** **CIRCLE 664**	Pin and socket, board to board	0.100 in. to 1 mm	25	Yes	Up to four	Stacking, spacing	Average insertion, 213 g., average, withdrawal, 90g	Press fit and solder
Components Corp. **Denville, N.J.** **Christopher Minter** **(201) 627-0290** **compcorp@garden.net** **http://www.component-scorp.com** **CIRCLE 665**	Card edge	0.200 in.	20	Yes	Two	N.S.	260 g, 192 g	Solder
EBY Company **Philadelphia, Pa.** **Jack Hibberd, (800) EBY-3430** **fax (215) 537-4780** **http://www.cdcom.com/eby** **CIRCLE 666**	Tip and test jacks, card edge, sockets, custom, military, SMT, and custom filtered	From 0.156 by 0.200 to 0.100 by 0.150 in.	40	Yes, some	Up to four	Guidance/polarizing as well as custom features	10 oz. and 1 oz.	Press fit, solder, and/or compliant pin
EDAC Inc. **Scarborough, ON, Canada M1V 5B6** **Donna Van Ast, (416) 754-3322** **edac@edac.net** **http://www.edac.net** **CIRCLE 667**	Card edge, D subminiature, USB, rack and panel, audio/video connectors	From 0.100 to 0.250 in., and from 0.140 to 0.250 in., respectively	20	No	One to four	Rack and panel, coaxial, I/O, audio/video, and low power	Varies by connector style	Press fit and solder
ERNI Components Inc. **Chester, Va.** **Pamela McElrath** **(804) 530-4271** **fax (804) 530-5858** **CIRCLE 668**	Card edge, high density, pin and socket, SMT, solderless, and through hole	From 0.200 to 0.050 in. and 2 mm	125/in.	N.S.	Up to 10	Compliant, polarization/guidance, I/O, and matched impedance	N.S.	Press fit and solder
Fujipoly America Corp. **Kenilworth, N.J.** **Frank Hobler, (908) 298-3850 ext. 208** **fax (908) 298-1238** **fujipoly@aol.com** **CIRCLE 669**	Elastomeric	As low as 0.5 mm	N.S.	No	N/A	N/A	ZIF	Squeezed between the two planes
Kycon Inc. **San Jose, Calif.** **Wendy Wuerth, (408) 494-0330** **wendy@kycon.com** **http://www.kycon.com/kycon** **CIRCLE 670**	D-subs, modular jacks, card edge, PLCC and SOJ sockets, SMT, high temperature, and ferrite filtered	0.05 to 0.1 in.	0.05	Yes	One to two	Stacking, power, polarized, I/O, coax, and fiber optic	N.S.	Press fit and solder

If you're designing wireless communications devices, we're the antenna and battery pack specialist you need.

We designed these 2.4GHz antennas for wireless LAN applications.

We developed this connector for spread spectrum applications in compliance with FCC Part 15.

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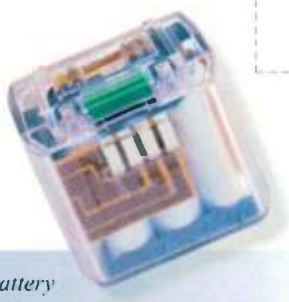

Every battery pack we design and manufacture meets or exceeds all electrical, mechanical and functional specifications.

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FAX: 800-848-3825/402-467-4528

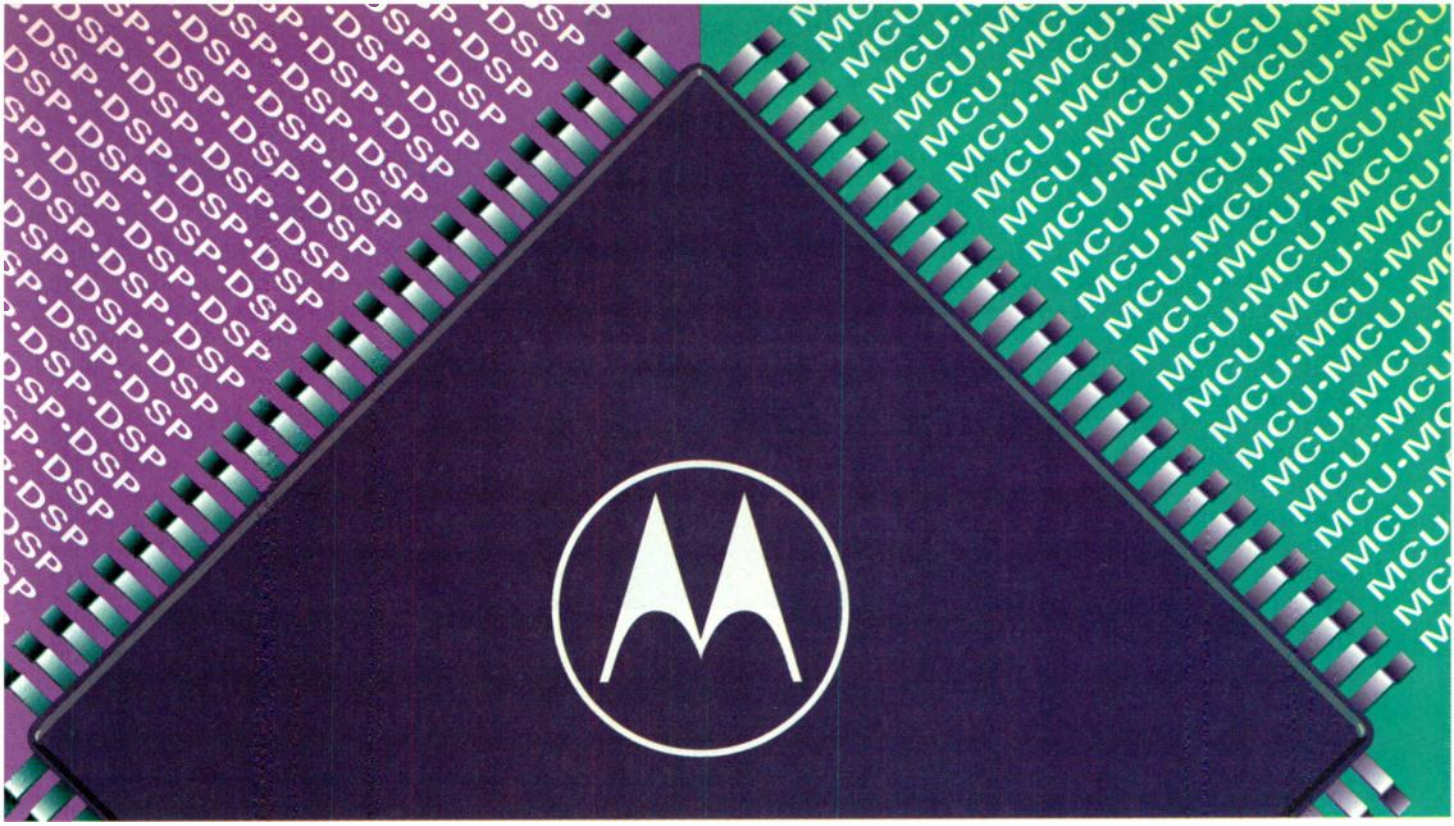
Lucent Digital Cellular Telephone 6720

Centurion International has developed antennas for many Lucent Technologies Inc. wireless terminals which meet Bell Labs specifications.

READER SERVICE 110

MANUFACTURERS OF BOARD-LEVEL CONNECTORS

Manufacturer	Connector style	Contact/row spacing	Maximum pin density	Modular contacts	Number of contact rows	Functions other than signal lines	Max. insertion and min. withdrawal forces	Termination techniques used
Lemo USA Inc. Santa Rosa, Calif. Cust. Service, (800) 444-5366 fax (707) 578-0869 lemousa@aol.com CIRCLE 671	Circular, quick connect/disconnect	N.S.	106 contacts	Yes	All circular	Coax, triax, fluidic, pneumatic, and fiber optic	Depends on contact size and number	Crimp, solder, and pc-board mount
Leoco (USA) Corp. Fremont, Calif. Frank Chou, (510) 651-4700 sales@leocousa.com CIRCLE 672	Pc-board, wire to wire, card edge, ZIF, FPC, D-sub, and PCMCIA	1 to 2.54 mm	0.05-in. centerline	No	Three	Stacking, polarizing, I/O, and coax	N.S.	N/A
LMI Connectors Inc. Boca Raton, Fla. Anne Gaborian, (561) 994-5896 fax (561) 994-5913 http://www.lmicorp.com CIRCLE 673	Pc-board mount, pc-board pluggable, pin pluggable, DIN, and panel mount	0.150 to 0.600 in.	0.150 in.	N.S.	Single or double level	High power (up to 45 A), panel mount, DIN 41612, and 19-in racks	N.S.	Solder
Lumberg Inc. Richmond, Va. Chris Shumaker, (804) 379-7247 fax (804) 379-3232 CIRCLE 674	SMT, IDC	1.27 mm, 0.05 in.	N.S.	Yes	36 poles	SMT header, and edge card connector	N.S.	Press fit or solder
Methode Electronics Chicago, Ill. Ken Marchmon, (708) 867-9600 http://www.methode.com CIRCLE 675	SMT, through-hole, straddle mount, and IDC	1 or 2 mm and 0.050, 0.100, 0.156, and 0.256 in.	1 mm	Yes	One or two	Locking, fiber-optic, I/O, and cable connections	N.S.	SMT, through-hole
Micro Plastics Inc. Chatsworth, Calif. Tom Miller, (818) 882-0244 fax (818) 882-0239 CIRCLE 676	Card edge	0.145 to 0.250 in.	0.100 to 0.156 center	No	Two	N.S.	10 to 12 oz and no less than 1 to 2 oz, respectively	Wire wrap
Mill-Max Mfg. Corp. Oyster Bay, N.Y. Tech. Services, (516) 922-6000 techserv@mill-max.com http://www.mill-max.com CIRCLE 677	Pin and socket	0.100 in., 2 mm, 0.70 in., and 0.50 in.	20	No	Two or over	None	Low, medium, and high options	Press fit and solder
ODU-USA Inc. Camarillo, Calif. Ralf Eberlein, (805) 484-0540 ralfeb@odu-usa.com http://www.odu-usa.com CIRCLE 678	IDC, D-subs, pin and socket, SMT, board to board, and board to cable	Down to 0.85 mm	Up to 30/in.	Yes	Two or more	I/O and cable, coax, power, andfiber optic	Approximately 18 g	Press fit and solder
Omnetics Connector Corp. Minneapolis, Minn. Greg Jones, (612) 572-0656 fax (612) 572-3925 CIRCLE 679	SMT, micro and nano miniature, through-hole, space and flight grade, and custom	0.0125 up to 0.050 in.	0.0125 in.	No	Up to two	Guide posts, keying, crimp, coax, and solder	6 oz and 1 oz, respectively, per contact	N/A
Power Dynamics Inc. West Orange, N.J. Frank Petrillo, (201) 736-5722 fax (201) 736-8930 CIRCLE 680	D sub, card edge, SIMM/DIMM, DIN, mini DIN, RCA, headers/receptacles	1.27, 2.0, 2.54, 3.96 mm	N.S.	Yes	Two	Polarizing, power, stacking, and latched	N.S.	Solder, press fit
RIA Electronic Inc. Eatontown, N.J. Ken Aurin, (908) 389-1300 ria@njsurfnet.net http://www.riaelectronic.com CIRCLE 681	Pc-board terminal blocks, single piece and pluggables	3.5 up to 10.16 mm	7.25/in.	Yes	Two	Wire protection and polarizing	N.S.	Solder
Samtec Inc. New Albany, Ind. Mary Kay Baumann (812) 944-6733 info@samtec.com http://www.samtec.com CIRCLE 682	Pin and socket andSMT	0.100 and 0.050 in., 2, 1, and 8 mm, and 0.50 by 0.100 in.	300 per square inch (series dependent)	Yes	Up to four	Multiboard stacking, alignment, I/O and cable, and blind mating	1.7 oz and 0.70 oz, respectively	Solder



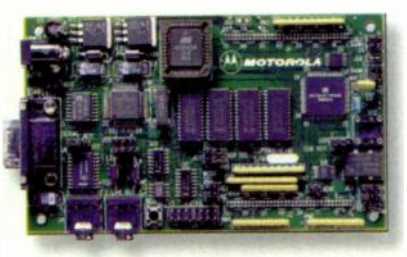
Our DSP56L811 has a split personality

(Good thing they're both so easy to get along with)

Is it a DSP? Is it a microcontroller? Well, it's both or it's either, the choice is yours. Microcontroller fans will see a general purpose, easy to program 16-bit controller, while DSP engineers can take advantage of a high-efficiency, low-power DSP architecture. The decision is easy.

Now you get a single part optimized for signal processing and microcontroller functions; plus it's easy to program, with compact assembly and C compiled code. This 3 V, 16-bit processor handles up to 20 MIPS @ 40MHz, and sells for less than $10 today. And whichever personality you like better, you won't need a lot of power, since the DSP56L811 typically consumes only 1.1 mA per MIPS.

Start your next design using the DSP56L811's robust array of development tools from both Motorola and independent developers. Our full featured DSP56L811 Evaluation Module not only includes software tools for application development, but it even comes with a codec and 128 Kbytes of SRAM already on board.



DSP56L811 Evaluation Module

So don't let the dual requirements of your next application drive you crazy. The DSP56L811 is the answer for cordless telephone, digital pager, digital tapeless answering machine, low speed modem and other consumer applications. Either way you look at it, increased functionality and performance at low cost is here to stay.

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SCSI Connector Is Lightweight And Low Cost

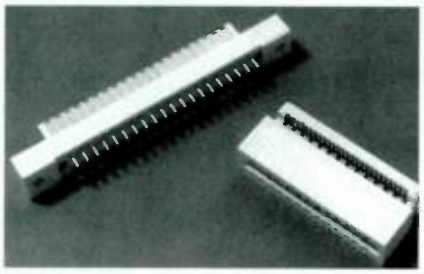
The FCN230 series of SCSI-2 and SCSI-3 pc-board connectors are offered as lightweight and economical alternatives to die-cast versions, while delivering the same level of performance. The SCSI-2 version is a right-angle, board-mount socket with 50 mating contacts. The SCSI-3 connector is available in both straight and right-angle board-mount socket configurations. Both feature a 0.050-in. contact pitch with through-hole terminals arranged in a staggered 0.050 by 0.075-in. configuration. Other features include a 240 V ac maximum allowable voltage, 1-A dc current handling capability, and an operating temperature range of -55° to 105°C. Pricing is: SCSI-2, $2.03; SCSI-3, $2.81 ea/10,000.

Fujitsu Takamisawa America Inc., *250 E. Caribbean Dr., Sunnyvale, CA 94089; (800) 380-0059; marcom@fta.fujitsu.com; http://www.fujitsufta.com*

CIRCLE 688

Card-Edge Connector Features 0.100-in. Spacing

The Pluggem is a male card-edge connector with 0.100-in. spacing that can be provided with cable-to-cable and



cable-to-pc board interface capabilities. The Pluggem is available with a pc-board, right-angle-mount, or vertical-mount male connector. Depending on the version, contacts range from 10 to 50. All have a 3-A rating and are UL approved.

WPI Viking, *9250 Independence Ave., Chatsworth, CA 91311-5713; Sales Dept. (818) 341-4330.*

CIRCLE 689

High-Density Connector Saves On Space

Part of the company's CWN-700 series, these connectors are made from polycarbonate material using an insert molding techniquefor an airtight seal and excellent pin retention. Spacing is

at 2-mm intervals and heat stake posts can be molded into the body. Custom attributes include number of contact pins, spacing between pins, pin plating materials, and insulator materials.

CW Industries, *130 James Way, Southampton, PA 18966; Mary Lovern (215) 355-7080; fax (215) 355-1088.*

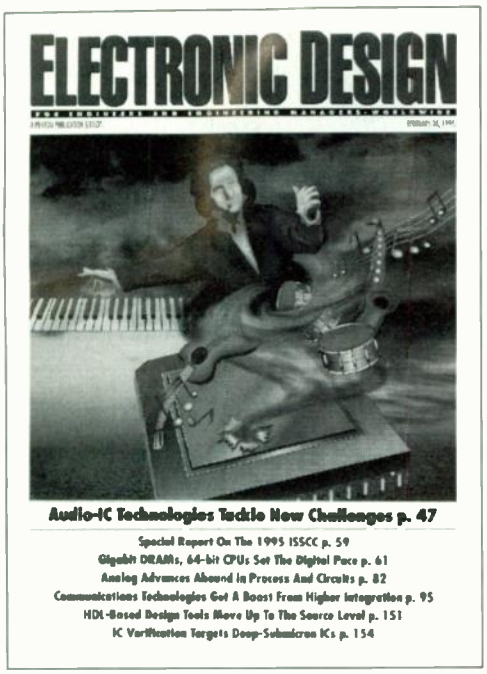
CIRCLE 690

MANUFACTURERS OF BOARD-LEVEL CONNECTORS

Manufacturer	Connector style	Contact/row spacing	Maximum pin density	Modular contacts	Number of contact rows	Functions other than signal lines	Max. insertion and min. withdrawal forces	Termination techniques used
Stewart Connector **Glen Rock, Pa.** **Tom Veres, (717) 235-7512** **tveres@stwconn.com** **http://www.stwconn.com** **CIRCLE 683**	IDC, modular SMT, modular filtering, CAT 5, and modular with LED	0.100 in.	25	N.S.	Four or less	None	Max 5 lb and 10 lb, respectively	Solder
Teka Interconnection Systems **Warwick, R.I.** **Patricia Powers, (401) 785-4110** **szgh88a@prodigy.com** **http://w3.bbsnet.com/teka** **CIRCLE 684**	Card edge, pin and socket, SMT, solder-bearing lead, and PCMCIA	1 mm to 0.156 in.	50/in.	Yes	Four	Stacking, I/O, pre-applied solder and flux	43 g and 15 g, respectively	Press fit, solder, and pre-applied flux
Teltec Inc. **Minneapolis, Minn.** **Gene Abel. (612) 854-9177** **fax (612) 854-8601** **CIRCLE 685**	High-density, two-piece for through-hole, SMT, and IDC cable interconnects	1.27, 1.0, and 0.5 mm	From 20 up to 160 positions	No	Four	IDC 0.025 ribbon cable, power, and polarizing	Insert and withdrawal, 2.9 to 1.2 kg, min	Solder
Teradyne Inc. **Connection Systems Div.** **Nashua, N.H.** **Christopher Van Veen** **(603) 791-3446** **vanveen.chris@tcs.teradyne.com** **http://www.teradyne.com** **CIRCLE 686**	Pin and socket, SMT, mini fork and blade, std. NAFI, power, coax, and fiber	0.5 mm, 2.0 mm, 0.100 by 0.100 in., 0.100 by 0.050 in.	101/in.	Yes	Up to eight	Stacking, power, guidance, I/O and cable, coax, and fiber optic	45 g typical, 15 g min., respectively, for 2-mm connnector	On daughterboard or press fit on backplane
TromPeter Electronics **Westlake Village, Calif.** **Mark Borton, (818) 865-6534** **fax (818) 706-1040** **trompeter@worldnet.att.net** **CIRCLE 687**	Pc-board mount, BNC connector	0.625 in.	N/A	No	N/A	Coax, insulated, and non-insulated bulkhead mount	N/A	N/A

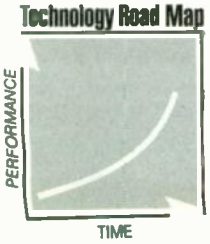
STRATEGIC PARTNERS WORKING TOGETHER

Information has always been a part of the developmental strategy needed for success in the OEM market. In today's fast-paced, competitive global market environment, technology information has become a priority. Systems designers not only want to know what their strategic supply partners are doing today, but where they're going. Designers and suppliers must now work in tandem to align enabling technology with the customer's system requirements. These strategies demand strong partnerships in the development of competitive products.



A third strategic partner completes this alliance. This partner's mission is to observe and report today's product availability by its editorial staff of respected experts, while constantly probing for the next generation of enabling technology. The constant flow of exclusive and vital information helps to bring systems designers and suppliers together as strategic partners. It also provides engineers and engineering managers with an enhanced ability to bring more competitive products to market, faster.

Electronic Design is that strategic information partner — a partner who provides the information that helps the systems designer make those critical decisions that stay the course of the technology road map.



Your Strategic Information Partner.

ELECTRONIC DESIGN

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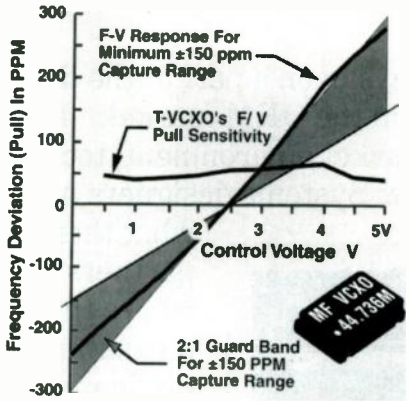
PRODUCT FEATURE

Miniature, Surface-Mount VCXO Guarantees Capture Span Over 0°to 70°C And -40° to 85°C

Claimed by MF Electronics to be the world's smallest surface-mount VCXO, the T-VCXO has a footprint of 5 by 7 mm and comes with capture spans of 50, 100, and 150 ppm over the temperature ranges of 0° to 70°C and -40° to 85°C. The center-frequency deviation is a guaranteed less than ± 25 ppm (max) over 0° to 70°C and less than ± 50 ppm over 40° to 85°C.

The device comes in a multilayer, ceramic leadless chip-carrier package that replaces "J" leads with large solder pads (0.045 by 0.048 in.) for enhanced soldering integrity, automated pc-board inspection, and two-sided pc-board design. The tiny footprint helps avoid damage from pc-board bending, warping, and vibration to meet military flexure specifications.

Key to the T-VCXO's high temperature tolerance are the 420°C bonding processes used during manufacture. They weed out early mortalities, provide accelerated aging, and shrink the oscillator's first-year drift to ± 3 ppm. The high production temperatures also ensure outgassing prior to hermetic sealing, thus helping to bring long-term drift down to ± 2 ppm.



In a further effort to improve performance while saving on space and overall cost, a 0.1-µF bypass capacitor has been integrated into the package to minimize triggering uncertainty, sharpen the output waveform, and reduce jitter to less than 35 ps peak to peak (typical). At higher frequencies of 5 MHz and above, including the capacitor in the package itself reduces wiring- and lead-induced impedances that diminish the capacitor's isolating capability.

The T-VCXO is targeted at portable data transmission and telephony applications, operates off 5 V ±5% dc and draws 25 mA. Pricing is less than $12 ea./qty. and delivery is stock to 6 weeks.

MF Electronics Corp.
10 Commerce Dr.
New Rochelle, NY 10801
Martin Finkelstein, (800) 331-1236; fax: (919) 576-6204.

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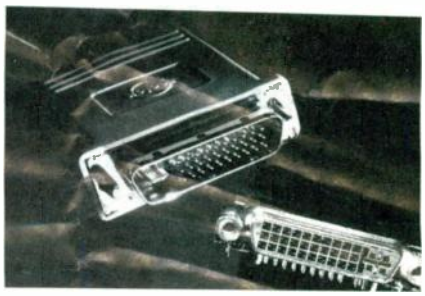
Connector Combines Multiple Functions

The MicroCross Enhanced Video Connector combines the separate connector functions required for keyboard, mouse, game port, monitor, parallel printer, and DDC, USB, and/or 1394 serial devices into one connector. The connector allows the monitor to be used as an I/O hub to eliminate the wiring maze now associated with multimedia computer applications. The connector helps to reduce EMI as well as installation costs as separate connectors and cables are no longer required. Other features include a patented crossing ground blade design that provides video bandwidth of over 2.5 GHz on RGB and clock lines. The company's patented LFH redundant contact

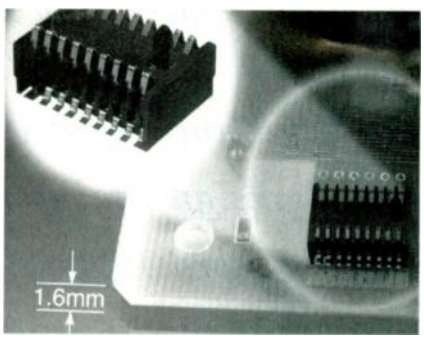


point terminal design provides mechanical integrity and electrical reliability. Pricing for a receptacle is $2.77 each in 100,000 units and delivery is four to six weeks.

Molex Inc., 2222 Wellington Court, Lisle, IL 60532; (800) 78-MOLEX; (630) 969-4550; fax (630) 969-1352. **CIRCLE 691**

One-Piece Parallel Stacking Connector Has Low Profile

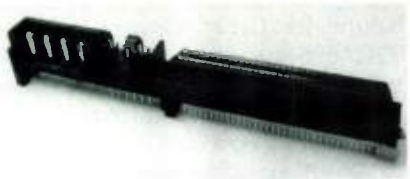
The 9158 Series is a one-piece, parallel board-to-board stacking connector with stacking heights as low as 1.6 mm up to 4.5 mm. Available in sizes ranging from four to 40 positions, the connector comes with a 1-mm-pitch dual row of contacts in a surface-mount configuration, and an optional locating boss for correct pc-board alignment. Contact material is beryllium copper with gold plating in the mating area and tin lead solder tails. The connectors are UL 94V-O rated to 125 V at 0.5 A, have an insulation resistance of 100 MΩ,and a contact resistance of 25 mΩ. Pricing is $0.04 per contact in quantities of 100,000 pieces. Delivery is four weeks for standard and 12 weeks for custom configurations.



ELCO Corp., 801 17th. Ave. South, Myrtle Beach, SC 29577; Sales & Mktg. (803) 946-0414; fax (803) 626-5186. **CIRCLE 692**

Ultra-SCSI Connector Combines Data, Power, And User Pins

The Ultra-SCSI is a high-density SCSI connector with 0.050-in. pin centers, 68 data pins, and 12 user pins. High-temperature resin ensures di-



mensional stability up to 260°C for 20 seconds and 220°C for a full minute. Normal rated operating temperature is -40° to 140°C. The insulation resistance is 5000 MΩ at room temperature. The contacts are rated at 1 A for signal lines and 3 A for power lines and are plated with a gold flash over palladium-nickel. Power-line contacts are located on standard 0.200-in. centers. Pricing is $1.60 and delivery is two to three weeks ARO.

***Ranoda Electronics Inc.**, 2315 NW 107th Ave., Miami, FL 33172; (305) 593-0129; fax (305) 594-3973.*
CIRCLE 693

Card-Edge Connector Aims At High-Frequency Applications

Featuring cantilever beam contacts with 30 to 150 dual positioned signal and ground pins in an alternating array, the F1D Series card-edge connector minimizes crosstalk and controls impedance for high-speed data transmission applications. The connector allows simultaneous switching of signals with 500-ps rise times. The connector comes with both through-hole and SMT contacts with standard tail lengths of 0.100, 0.125, 0.155, and 0.190 in. and is reflow-soldering-compatible. Pricing for a 73-dual-row version is $7.35 each in 1000-unit lots and delivery is stock to four weeks ARO.

***Thomas & Betts, Electronics OEM Div.**, 1555 Lynnfield Rd., Memphis, TN 38119; (800) 344-4744.*
CIRCLE 694

Modular Battery Contacts Target Portable Devices

Targeting portable electronics applications, these 70AD male and female Modular Battery Contacts come in two- to six-pin configurations with surface- or through-hole mounting options. The high-quality, captured-spring contacts have a precious-metal coating and are mounted in high-temperature molded plastic. Pricing in 1000-unit lots for the female is $0.57; for the male it's $0.68.

***Bourns Inc.**, 1200 Columbia Ave., Riverside, CA 92507; 800-403-7664; fax (909) 781-5140.* CIRCLE 695

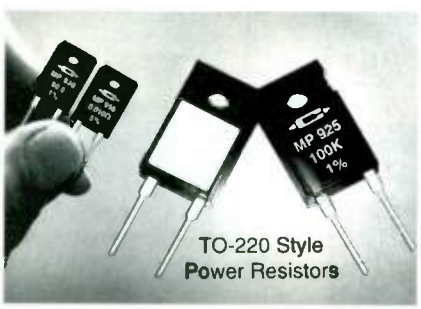
LEDs Replace Standard Bayonet-Based Bulbs

Designed to replace industry-standard T-3-1/4 bayonet-based light bulbs, the MB401-3CL1 LED cluster lamp incorporates a water-clear fresnel lens to maximize viewing angle and light dispersion (160°). The LED comes in red (654 nm), amber (594 nm), and green (565 nm), with outputs of 340, 200, and 45 mcd, respectively (measured without the lens). Comprising three LEDs in series, the lamp operates off voltages to 25 V dc or 120 V ac. Pricing per 1000 is $5.01 each for 5 to 28 V dc and up to $5.51 each for 48 to 120 V ac. Delivery is six to eight weeks.

***Data Display Products**, 445 South Douglas St.,El Segundo, CA 90245-4630; (800) 421-6815; fax (310) 640-7639.* **CIRCLE 696**

Low-Cost Resistor Heat-Sink Mountable

The MP925 is one of three TO-220-style, heat- sink-mountable resistors.



Rated at 25 W at 25°C, the 100-kΩ resistor has a tolerance of 1% and a voltage rating of up to 500 V. Two other versions are the 0.010-Ω MP916 and the 0.020-Ω to 4.99-kΩ MP930. These are rated at 16 W and 30 W, respectively.

***Caddock Electronics, Inc.**,1717 Chicago Ave.,Riverside, CA 92507-2364; (909) 788-1700; fax (909) 369-1151.* **CIRCLE 697**

SMD LEDs Have High Brightness

This line of 18 surface-mounted LEDs comprises the 1002 series of 11 flat-lens diodes and the 1005 series of seven domed-lens diodes. The devices have an output range of 2 up to 450 mcd, depending on wavelength, and measure 2.0 by 1.25 by 1.1 mm. Available wavelengths range from 555 nm (pure green) up to 700 nm (red). Pricing ranges from $0.15 to $0.50 each in 3000-unit lots.

***Toshiba America Electronics Components Inc.**, 9775 Toledo Way, Irvine, CA 92718; (800) 879-4963; http://www.toshiba.com/taec*
CIRCLE 698

TCVCXOs Provide High Stability

The K1700 Series of temperature-compensated, voltage-controlled crystal oscillators provide a temperature stability of ±10 ppm from 0° to 70°C, or ±20 ppm from -40° to 85°C. The frequency pull range (done by modulating the control voltage pin from 0.5 to 4.5 V) is ±100 ppm (min) to ±150 ppm (max). Linearity of pull versus control voltage is ±10 %. The device runs off 5 V±10 %, has a frequency range of 2.0 to 35.0 MHz, and ages ±3.0 ppm/year (maximum of ±5 ppm total aging). Packaging is standard 4-pin metal DIP with a maximum seat height of 0.327 in. Pricing is $22 each in quantities of 1000.

***Champion Technologies, Inc.**, 2553 N. Edgington St, Franklin Park, IL 60131; (708) 451-1000; fax (708) 451-7585; http://www.champtech.com*
CIRCLE 699

Dual Optocouplers Are PCMCIA-Compatible

Targeting telephone-line isolation and coupling and medical applications, the LOC210P and LOC211P are dual linear optocoupler devices in a 16-pin SOIC package which is PCMCIA compatible. Comprising an infrared LED and two phototransistors, the devices use the first transistor to generate the servo control signal compensating for nonlinear time and temperature characteristics associated with the LED. The second transistor provides an output signal that is linear with respect to the servo LED current. This allows the optocouplers to achieve better than 0.01% servo linearity and greater than 200-kHz bandwidth. Other features include a THD of better than -87 dB, an input-to-output isolation of 3750 V rms, and an operating temperature range of -40° to 85°C. Pricing is $2.74 for the LOC210P and $3.31 for the LOC211P, in 10,000-unit quantities.

***CP Clare Corp.**, 430 Bedford St., Lexington, MA 02173-1548; Robert Palladino, (617) 863-8704; fax (617) 863-8707.* **CIRCLE 700**

SMD TCXO Aims At Wireless Equipment

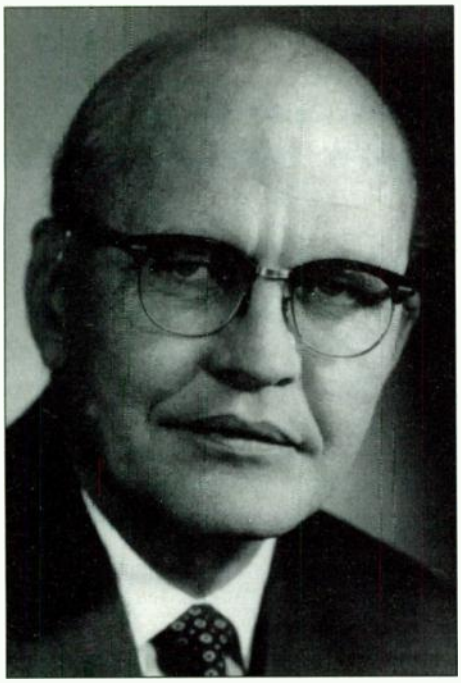
Intended for wireless telecommunication applications, the TXO-29SM is a surface-mountable TCXO that requires a low supply current and comes with frequency adjustment and low supply voltage. Frequency tolerances of ±2.5 ppm over a temperature range of -30 to 75°C are available. Measuring 11.4 by 9.6 by 3.9 mm, the device is available in standard frequencies of 10.00, 12.80, 13.00, 14.40, 15.36, 16.00, 18.54, 19.20, and 19.68 MHz. Pricing is $9.90 each in quantities of 10,000.

***ECS Inc.**,230 N. Monroe, P.O. Box 273, Olathe, KS 66061; (800) 237-1041; fax (913) 782-6991*
CIRCLE 701

Chip Trimmer Caps Have Low Profile

Designated the CTZ3 Series, this line of chip trimmer capacitors measures 4.5 by 3.2 mm with profiles of 1.8, 1.5, or 0.6 mm. Automatically adjustable and washable when mounted, the devices are available with capacitance values ranging from 3 pF to 50 pF with TCRs to ±500 ppm/°C. A high-stability version is also available with ±1% setting drift. Pricing ranges from $0.39 to $0.45 each in quantities of 1000. Delivery is eight to ten weeks with samples available now.

***AVX Corp.**, P.O. Box 867,Myrtle Beach, SC 29578; Mark Spera, (803) 946-0414; fax (803) 448-1943; http://www.avx-corp.com.* **CIRCLE 702**



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Revered by engineers worldwide as the inventor of the IC and a pioneer of solid state technology, Jack Kilby will once again make an appearance at the Portable By Design Conference & Exhibition. Two years ago, Mr. Kilby was the keynote speaker—this year, he will present the first annual "Electronic Design Award For Technical Innovation." The award will be presented the author of 1997's most innovative conference technical paper. The award represents the first of its kind given annually. The ceremony will take place at the Industry Reception, held on the show floor at the Santa Clara Convention Center in Santa Clara, Calif., on Tuesday, March 25, 1997 at 5:00 p.m.

Also at this year's gathering. . .

KEYNOTE SPEAKERS:

TOM BEAVER
Vice President
Worldwide Marketing
Motorola, Inc.

PHILIP WENNBLOM
Director, Strategic Planning
Mobile and Handheld Products Group
Intel Corporation

ROBIN SAXBY
President & CEO
Advanced RISC Machines
(ARM)

VAUGHN WATTS
Director of
Mobile Computing Architecture
Texas Instruments

and a presentation from **BOB PEASE**, author of "PEASE PORRIDGE"

Exhibitor Information: Contact **Lisa Zurick**, Director of Show Sales, at 847/263-6837; fax 847/263-6854
Conference Information: Contact **Rich Nass**, Program Chairman, at 201/393-6090; fax 201/393-6073; or call **Betsy Tapp**, Exhibition Manager, at 201/393-6075; fax 201/393-6073

POWER

Rechargeable Cell Has High Power Density

Based on the company's thin metal film technology, the 9/5 subC lead-acid cell measures 70.1 mm long, has a diameter of 22.9 mm, and is rated at 1.2 Ah. The TMF structure combines greater surface area with lower-impedance connectors. With an energy density of 78 Wh/l, the battery is claimed to have the highest power density of any such device. The cell targets portable equipment applications and has a nominal voltage of of 2.1 V, a cell impedance of less than 1.7 mW, and a weight of 82 g. The battery can be recharged at high and low rates, has no memory effect, is scalable in size, and has an inherently fast charge and discharge rate. Pricing is in line with competing lead acid and NiCd devices.

Bolder Technologies Corp., *5181 Ward Rd., Wheatridge, CO 80033-1925; Arnie Allen (303) 422-8200 ext.30; fax (303) 422-8180.*

CIRCLE 703

150-W DC-DC Converter Is Micro-Sized

This 150-W dc-dc converter module measures 2.28 by 1.45 by 0.5 in., accepts a nominal input voltage of 48 V dc, and provides a 12-V output with 86% efficiency. The device has an input range of 36 to 75 V, an output that's programmable from 1.25 to 13.2 V, and a power density of 90 W per cubic inch. Features include low input conducted noise and an output ripple of 210 mV, along with the company's proprietary zero-current switching and zero-voltage-switching architecture. The converter's baseplate temperature rating is 100°C at 150 W and the module is parallelable with N+M fault tolerance. The above-board height is 0.43 in. Pricing is $112.

Vicor Corp., *23 Frontage Rd., Andover, MA 01810; Kathryn Johnson (508) 470-2900; fax (508) 475-6715; e-mail: kjohnson@vicr.com; Internet: http://www.vicr.com*

CIRCLE 704

DC-DC Converter Has 300-W Power Output

The PH300S series of dc-dc converters output up to 300 W, yet measure only 3.38 by 3.27 by 0.5 in. to provide a power density of up to 54 W per cubic inch. Available in seven output voltages from 3 to 48 V, the devices have an efficiency of 86% at 5 V and provide up to 50 A with an input range of 200 to 400 V dc.

The devices use the company's unique patented topology and targe PBX, minicomputer, workstation, and other distributed power applications. The baseplate operating temperature rating is 100°C. All models come with integral overvoltage, overcurrent, and overtemperature protection, and are capable of parallel operation. Pricing is $0.42 per watt in OEM quantities.and delivery is from stock.

Lambda Electronics Inc., *515 Broad Hollow Rd., Melville, NY 11747; Lisa Waterman, (516) 694-4200.*

CIRCLE 705

DC-DC Converter Hits Radar Tasks

The ADDC02808PB high density dc-dc converter, in a package weighing 80 g, is specifically designed for pulse applications such as radar. The module operates from a 28 V input bus, providing up to 25 A pulse output current at 8 V (peak pulse output is 200 W). It delivers the pulse with minimum deviation in output voltage, and features an ultra fast return to the nominal output voltage. Output stability is ensured for a broad range of external load capacitances extending from 500 to 4000 µF. Transient response is 140 µs for a 24-A step load change. Other features include an integral EMI filter; current sharing for parallel operation; and low output noise. Internal feedback compensation can be modified at the factory for specific loads. Also included is output overvoltage protection, short-circuit protection, thermal monitor/shutdown, input overvoltage shutdown, and input transient protection. It meets MIL-STD-641D and NAVMAT requirements. Pricing is from $775 to $1185 each, in quantities of 100.

***Analog Devices**, One Technology Way, PO Box 9106, Norwood, MA 02062. (617) 329-4700; (617) 329-1241.* **CIRCLE 706**

Modular Switchers Provide 5-Slot Power

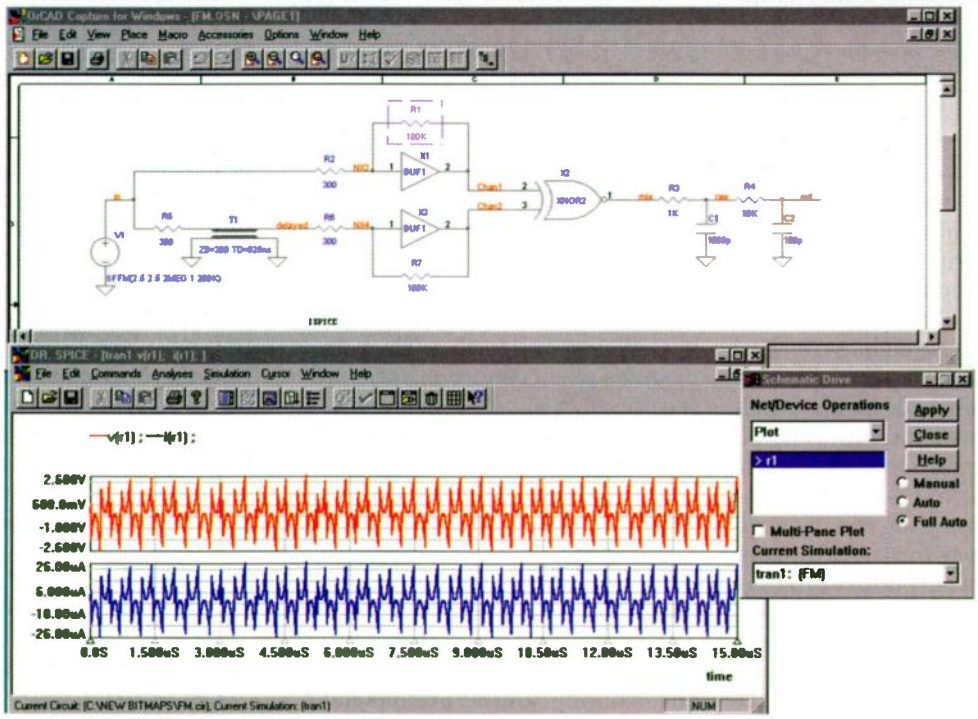
The KT and KNT switching power supplies, part of Unipower's K Series, provide five output slots and up to 1800-W of output in a case size measuring 5 (H) by 8 (W) by 11 (D) inches. There are 29 modules to choose from, each with a specific set of outputs configured at the factory. Output voltages are from 2 to 48 V dc at 80 to 1000 W. Both single- and dual-output modules are available. The KT models, with a universal input range of 85 to 264 V, come with high-frequency, zero-voltage switching and power factor correction to 0.99. The KNT models, without PFC, provide up to 1200 W output and incorporate input autoranging. Both versions have a standard FCC and EN level A input EMI filter with an optional EN level B filter.

The KT models also have an auxiliary 5-V, 50-mA output that's isolated from the other outputs and can be used to power external control circuits. Other features include remote sensing, output current limiting, short circuit protection, overvoltage and reverse voltage protection, and overtemperature shutdown. Control and monitoring functions include ac power fail, global and modular inhibit, remote margining, dc power good, thermal alarm, output current monitors, and alarms for current sharing and overvoltage. Single-output modules incorporate active current sharing circuitry. Pricing is $1690 for a typical five-output configuration with PFC, in 1-9 quantities; and $1530 for the same configuration without PFC. Delivery is two to eight weeks, depending on quantity.

***UNIPOWER Corp.**, 3900 Coral Ridge Dr., Coral Springs, FL 33065; (954) 346-2442; fax: (954) 340-7901.*

CIRCLE 707

Ten Important Reasons You Should Be Using Dr. Spice® 2000 A/D



1. Speed
Dr. Spice is fast - 2 times faster than other Spice simulators on average and up to 10 times faster on large or difficult circuits.

2. Ease of Use
Dr. Spice 2000 A/D is extremely easy to use for both beginners and experts. You can access all features by menus and dialog boxes. Every dialog box provides immediate access to extensive online help.

3. Superior convergence
In a test using the industry standard MCNC benchmark suite, Dr. Spice 2000 A/D ran over 93% of the circuits; the other leading brands ran just 87% and 62%, respectively.

4. Fast Built-in Mixed A/D
Dr. Spice 2000 A/D simulates even tightly-coupled mixed-signal designs. Its fast built-in mixed signal engine uses compiled C models for maximum performance. Primitives include gates, flip-flops, latches, state machines, comparators, decoders, multiplexers, adders, and RAM.

5. Schematic Driven Simulation
Dr. Spice links tightly with OrCAD, ProTel, and VIEWlogic. Select a net, component, or pin in your schematic and Dr. Spice plots its waveforms. By simply clicking on a component, you can also display its model parameters, operating point information, or run a parameter sweep. You can run simulations, set up stimulus, create plot windows or back annotate results onto your schematic, all from Capture menu items.

6. Non-Linear Magnetics for Power Supplies
Attention Power supply designers: Dr. Spice 2000 A/D provides the Chan non-linear magnetics model. This model is accurate, fast, and uses model parameters which come directly from the magnetics' data sheets. The Dr. Spice 2000 A/D model library includes over 2500 Chan magnetics models.

7. Library Support
Dr. Spice 2000 A/D has the largest library available, with over 20,000 parts, including virtually all manufacturers' libraries.

8. Automatically Generate Spice Models
Dr. Spice ModelMaker creates models of parts from data sheet parameters. Enter points graphically and ModelMaker automatically generates accurate SPICE models.

9. Automatically Calculate Power Dissipation
Dr. Spice automatically calculates the power dissipation of every device. You can also specify a maximum instantaneous power limit for any device in the circuit. If the device exceeds this power rating, an "alarm" occurs.

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Sweep (or step) analysis allows you to examine the effects of varying sources, device or model specifications, temperature, or user-defined parameters.

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PC GRAPHICS WATCH

Second-Generation UMA Systems

Tony Tong, S3 Inc.

As PCs evolve, performance and economic factors have made some form of shared system and graphics memory a logical choice for next-generation systems. Hence, performance and cost trade-offs can be made using a shared-memory architecture (SMA), or by employing the Advanced Graphics Port (AGP). The SMA partitions system memory to enable graphics accelerators to effectively use their allocated memory partition as local memory. Components other than graphics also may share system memory, such as wavetable audio processors.

The initial motivation behind the recent interest in shared memory is driven by cost. As the frame buffers' sizes and bus widths grow, lower system price points are enabled only by eliminating some or all of the discrete frame buffer. Another motivation for an architectural transformation is the greater bandwidth available for data transfers between system and graphics memory. The SMA allows transfers of this type to occur on the 64-bit, 66-MHz system memory bus instead of the lower bandwidth PCI expansion bus. This bottleneck is critical in total system performance and user satisfaction as high data-rate multimedia data types become integral to daily usage. The SMA also shows promise in 3D graphics, where the high data-rate requirements of texture and transparency mapping can overwhelm the PCI bus.

There are a number of shared memory implementations, either on the market or likely to appear in the next year. A dedicated frame buffer is the incumbent graphics architecture. Dedicated graphics memory guarantees the graphics memory bandwidth, and the ability to use advanced memory types, such as VRAM or SGRAM. However, PCI bandwidth limitations and graphics-memory granularity limit the usefulness of this approach. Flexibility also is impeded because the frame buffer size is limited by the amount of installed graphics memory.

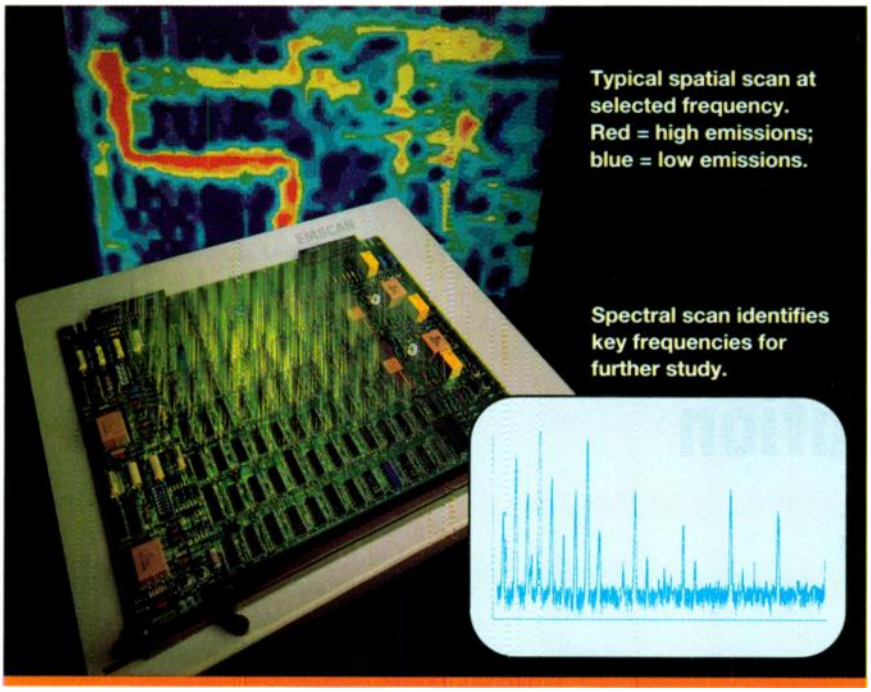
A unified-memory architecture (UMA) shares system memory between the discrete core logic and graphics memory controllers using dedicated arbitration signals. Two UMA-based standards have recently emerged—the Shared Memory Buffer Architecture (SMBA) championed by Intel, and the VESA UMA (VUMA) standard, led by the Video Electronics Standards Association (VESA). Both standards define a similar system partitioning and arbitration mechanism between the core logic and graphics components. The standards' defined system BIOS interfaces that allow the system to allocate and share the necessary memory space for the frame buffer are similar.

Two aspects of UMA arbitration are key to extracting the maximum total system performance from the architecture. First, the multiple arbitration priority levels enable the graphics controller to differentiate its memory requests between latency-sensitive operations such as screen refresh and less time-sensitive tasks like graphics engine operations. This allows the core-logic memory controller to maximize memory bandwidth whenever possible, while ensuring that screen updates are not compromised.

The UMA arbitration schemes minimize idle time on the system-memory bus by precharging the memory subsystem concurrent with the arbitration. Prior to control of the memory bus passing from the core logic to graphics, the system ensures that the proper RAS# and CAS# signals are driven high. These signals continue to precharge during the idle cycle where both components three-state the memory bus. When the graphics takes control, it then immediately begins a memory cycle by driving the proper RAS# signal low. The protocols call for a similar scheme during the reverse handoff from graphics to core logic.

The principal disadvantage of the UMA approach is its inability to further increase graphics performance. As user requirements rise and DRAM prices drop, most external frame buffer solutions allow the doubling of memory bus bandwidth (from 32 to 64 bits) by doubling the memory. This additional bandwidth significantly improves graphics performance.

Unlike the UMA, the SMA refers to a system where the graphics and core logic have been tightly integrated into a single chip. In addition, the SMA includes a greater cost savings compared to the UMA. While the same memory cost savings apply to each design, the SMA replaces multiple discrete components with a single chip and eliminates redundant subsystems and pins. Also important are performance gains realized by the integrated memory arbiter. While first-generation UMA designs successfully "hid" the DRAM precharge under the bus handoff arbitration, a page-miss penalty must be paid for each handoff between the system and graphics memories.



The single integrated memory arbiter in an SMA system significantly improves effective memory bandwidth. It reduces the number and frequency of handoffs between the system and graphics memory spaces over a UMA system.

Building a system using SMA with a separate frame buffer (SMA+FB) addresses the concerns of both discrete and shared memory graphics subsystems. In this approach, the discrete frame buffer is called upon only for primary display-pixel storage and is therefore a good candidate to use the specialized features of dedicated graphics memories.

Because the bandwidth and latency of the graphics-to-system-memory accesses in this SMA variant is similar to a dedicated frame buffer, all other graphics tasks, such as secondary stream support, Z-buffering, texture and alpha mapping, can be allocated from system memory as needed. Total system performance is enhanced because the system memory controller is no longer burdened with the bandwidth overhead of screen refresh.

The AGP is similar to the SMA+FB architecture. Both provide for external frame buffers of arbitrary bandwidth for high-resolution graphics modes, while allowing a peak system-to-graphics-memory bandwidth above 500 Mbytes/s. This relieves the system from the cost burden of extremely large frame buffers by allowing the prodigious requirements of texture data for 3D rendering to be accessed directly from host memory.

The principal weakness of the AGP lies in the relatively long latency for an AGP device to access system memory. The AGP split-transaction access queue exhibits a significantly longer access than a direct SMA access in an SMA or SMA+FB solution. This has two effects. First, it makes the AGP solution expensive to implement, with multiple large data and command pipeline queues needed to ensure adequate mean effective bandwidth. These buffers are needed on both the host and graphics devices. Second, the AGP imposes long latencies for initial memory accesses. This problem restricts the usefulness of system memory in an AGP system.

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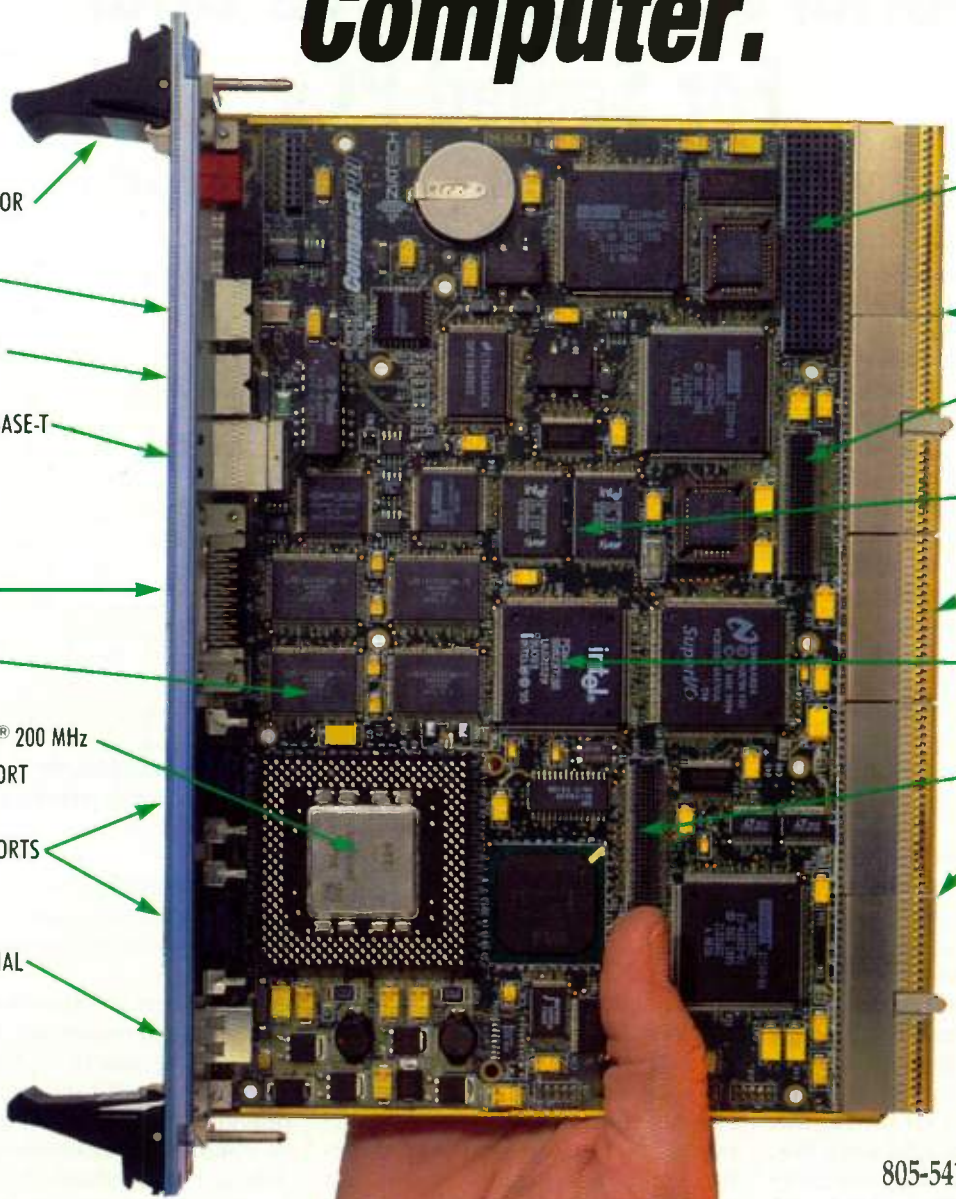

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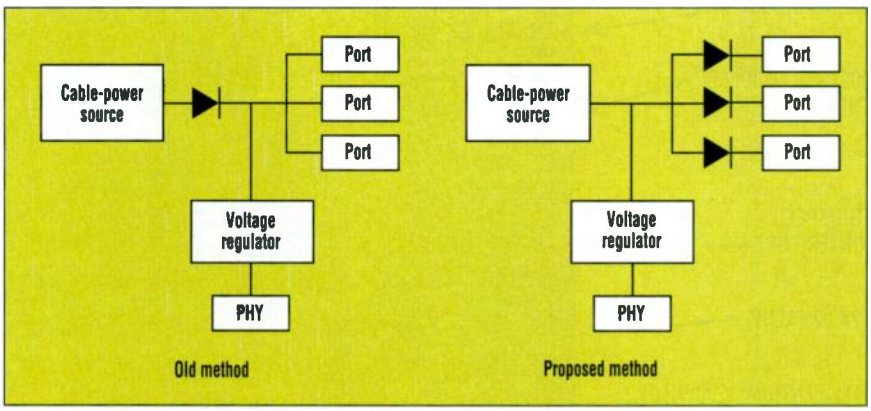
Serial Bus Opens The Door For Sealed PCs

IEEE 1394 Offers The Speed Required For Next-Generation PCs And Consumer Electronics.

GREGORY URBAN National Semiconductor Corp., 2900 Semiconductor Dr., MS D2-570, Santa Clara, CA 95052; (408) 721-5926

One of the biggest differences between today's PCs and the larger world of consumer electronics is the generally accepted notion that PC users must occasionally "open the case" and make changes to the PC's internal hardware. Even though the installation of new peripheral cards and resolution of IRQ conflicts have become less perilous with the advent of Plug and Play (PnP), they still remain daunting prospects to many mainstream users. Some industry analysts are even beginning to predict a plateau in the growth of the home-PC market unless tomorrow's PC designs can be made as simple to install as other consumer electronic devices. In addition, the rapid convergence of PCs with consumer video, audio, television, and other devices is driving the need for a high-speed processor that can provide interoperability through robust peer-to-peer connections.

One standards-based solution that's gaining support for solving this dilemma is the IEEE 1394 serial bus. The IEEE 1394 technology has many innovations over prior technologies used for peripheral I/O. The 1394 serial bus interface offers high-speed communications (currently specified for 400 Mbits/s, with an upgrade path to 1 Gbit/s) and fully supports isochronous real-time data services. It also supports PnP, allowing hot plugging of up to 63 external peripherals. The ultimate objective is to make attaching a 1394 device as easy as plugging a cord into an electrical outlet. Because it's a peer-to-peer memory bus, the 1394 is easy to program and allows devices to communicate without tying up computing resources. For instance, communication between a scanner and a printer can occur without consuming system memory and CPU resources; the 1394 bus allows isochronous connections for dedicated bandwidth.



1. Because there may be more than one power source on a 1394 serial bus, the sources must be diode isolated to the power pair on the cable so the current from a node providing a higher voltage doesn't flow into lower voltage sources.

For multimedia applications, the 1394 interface enables real-time digital data transfer for audio and video capture, editing, and playback. It also provides for distributed multimedia applications like desktop conferencing. For example, users can easily transfer images from a camcorder to a PC. These images can be edited and displayed on a PC or TV screen while users simultaneously print color pictures.

Despite the growing industry support, a number of technical implementation issues must be addressed to allow full implementation of IEEE 1394 bus as the solution to connect sealed PCs to consumer electronics. These issues include the creation of a standardized host-controller interface, mechanisms for bus security, power-distribution and device-isolation management, and cost optimization. Successful resolution of these challenges also requires the creation of standard component-level silicon to enable system designers to easily implement 1394 interfaces with seamless interoperability.

To become an effective standard for peripheral connection, IEEE 1394 bus must be able to replace existing mass-storage interfaces as well as provide a simple, universal interface to connect to consumer devices. Among the standards that will likely be supported are the Serial Bus Protocol (SBP), replacements for IDE and SCSI controllers, and the Open Host Controller Interface (OpenHCI).

One goal of the SBP is to define a device model that's acceptable to disk drive vendors looking for an evolution from SCSI and ATAPI. Another goal of SBP is to fully exploit the underlying capabilities inherent in 1394 busses, while balancing between implementation complexity and protocol comprehensiveness. Because the competition in the mass-storage market is so intense, cost of the interface has become a major factor.

Since the SBP was drafted, the

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complexity of its implementation has prevented widespread acceptance by the industry. However, momentum is now streamlining SBP to allow a lower cost implementation. Isochronous transactions have been made an optional part of SBP and Autosense requirements have been eliminated. In addition, SBP's interface model has been altered to use object-oriented Object Resource Broker (ORB) technology rather than emulating SCSI commands, data, and status protocols. Object-oriented communication allows SBP over 1394 busses to be more efficient while providing the flexibility to integrate future devices without rendering the underlying protocols obsolete.

The transfer rate of hard-disk drives is constantly increasing. Consequently, a higher speed version of the 1394 bus will be needed before the end of the century. The current goals of the IEEE 1394.2 working group include creation of a 1.2-Gbit/s serial bus with application layers which are the same as those for existing 1394 bus. The working group also will strive to make 1394.2 busses scalable to 4.8 Gbits/s, however the physical layer and the fundamental architecture also will be changed. IEEE 1394.2s will not be plug-compatible with IEEE 1394s, therefore legacy hardware will not be directly compatible.

Running At 1 Gbit/s

A second approach is to run 1394 buses at 1 Gbit/s. However, at higher data rates, the maximum achievable cable lengths will be much shorter. In addition, the encoding scheme will likely change above 400 Mbits/s, and may add cost to this higher speed solution to achieve lower-speed compatibility. Therefore, this approach can work for inside the box connections. When the 1394 goes outside the box, the transfer rates will have to be downgraded to 400Mb/s.

One of the reasons that the 1394 bus had not gained acceptance as a mass-storage interface previously, is the inherently high gate count required for a 1394 host controller. However, the prospect of large volumes of consumer electronics interfaces combined with improved silicon processes are leading to lower-cost 1394 implementations. As low-cost mass-storage options become available, a single bus can connect both the internal mass storage and external peripherals. Therefore, the mass-storage interconnect controller, such as IDE or SCSI, can be replaced by the 1394. Eliminating multiple interconnect methods helps reduce overall system costs.

Conversely, putting both internal mass storage and external peripherals on one bus can pose many problems. Although the 1394 bus supports up to 400 Mbits/s, one DVCR HDTV quality data stream will need 50 Mbits/s of bandwidth. If the DVCR device was implemented with 100-Mbit/s transfer capability, over 50% of the bandwidth will be consumed with overhead. Mass-market single-user PC hard drives can easily consume more than 160 Mbits/s. A DVCR with a 100-Mbit/s transfer capability can barely have both the video data stream running and the 160-Mbit/s disk drive working at the same time, even with a 400-Mbit/s host controller. Because there are few 100- and 200-Mbit/s implementations available today, peripheral vendors should be encouraged to migrate to 400-Mbit/s implementation as soon as possible.

The OpenHCI promotes the use of one software-hardware interface. This arrangement allows multiple host-controller vendors to design the controllers with a common hardware register set and software interface. The OpenHCI saves the vendors the cost and time of developing and testing software, as well as distributing software drivers. It also eases software support on the vendors themselves.

The design goal of the OpenHCI is to balance the complexity of the hardware and the cost savings of the software while maintaining the efficiency of the host controller's descriptor base control. The controller's efficiency is governed by the interaction of the software with hardware registers, and of the host controller with host memory. It should selectively enable and disable interrupts occurred from receiving packets to lower the interrupt count. Multiple isochronous input and output channels also are supported.

In a PC environment, many different classes of devices could be employed, such as mass storage, DVCRs, camcorders, and printers. A Device Classes specification describes the software interface to popular devices having common behaviors and functions. This specification lets operating-system vendors supply standard drivers for particular classes of devices. As a result, device vendors won't need to supply and support their own software drivers. However, device vendors still can provide and distribute their own drivers if the drivers offer significant differentiation for their products, or if their devices don't belong to one of the Device Classes.

An Open-Memory Bus

The IEEE 1394 is basically designed as an open-memory bus. Local memories on each node are directly accessible by all other nodes on the bus. Because there's no firewall protection against unauthorized access, disastrous consequences such as hard-drive corruption could occur if erroneous access was generated from a node's software glitch or from any hostile device. The goal of Bus Security is to protect the internal devices and host memory from corruption by external devices without raising the cost of the system.

One possible bus-security solution would employ Global Unique IDs (GUIDs) to all external 1394 devices. These IDs would establish a trust model for specific operations. During the negotiation phase of two nodes, the GUIDs are exchanged and the trust structure is established. In the case of boot devices, the device ID can be maintained at the CMOS level. For non-boot devices, the operating system can maintain the GUID codes. This GUID model may slightly raise the cost of the external device due to the fact that an additional ROM might be needed. The trade-off is that it allows greater use of the bus bandwidth by not requiring the operating system to intervene in every data packet.

The IEEE 1394 specifies that a node may be a power source, a power sink, or self-powered. Because there may be more than one source, they must be diode isolated to the power pair on the cable such that current from a node providing a higher voltage does not flow into sources of lower

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output voltage. The output voltage of 20 to 33 V dc is carried on the cable, up to 1.5 A per cable *(Fig. 1)*.

One problem with the current method is that the bus manager can't exactly determine how much power is really available from the bus. A power supply designed with minimum output current may dominate the bus' power because it has the highest voltage output. When one supply dominates the power, other sources can't add incrementally to the bus. If another power-consuming device (or in the worst case, a tree of power sinking devices) is added to the bus, it may crash due to power loss. The newly proposed method limits the fanout of the power source, and avoids multiple bus-powered devices sharing the same power source. The rules specify that:

- Bus powered devices must be endpoints. Bus powered devices should have only one 1394 bus connector, thereby eliminating the chance of having multiple bus-power devices chaining together into one source.
- Each port of the power source must be individually diode isolated, eliminating the distribution of power across segments.
- Self-powered devices must power their own physical layer (PHY) at all times. If the device is wall-plugged, it's responsible for the power of its own PHY. This specification ensures that the PHY performs the data repeater function at all times. If the device is powered off, some forms of trickle power must exist to maintain the PHY, otherwise any downstream nodes will be isolated.
- The distance from source to sink can't exceed three hops/cable. This design limits the distance required for passing power along the cable, thereby avoiding excessive power losses in the cable from the power pair's resistance.

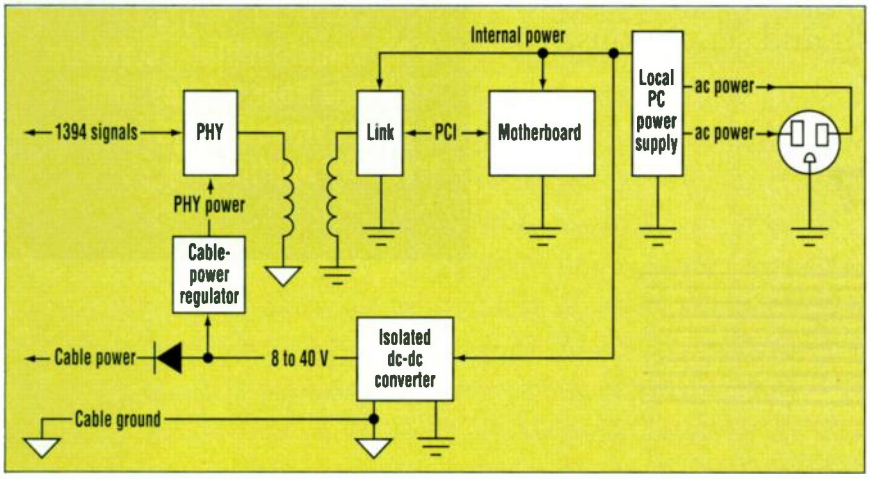
Electrical isolation protects devices from limiting current flow in the green-wire ground. By providing an interface between parts operating at the same or different voltages, it allows either side to be independently powered down. The internal enclosure's local supply provides external cable power, internal device (core logic) power, and link power. The signal isolation occurs between the PHY and link ICs. It doesn't matter how the link function is physically implemented as long as it's electrically isolated from the PHY. The PHY interface to the link chip should be designed with isolation in mind. Pin count should be kept to a minimum and data rates held constant. The cable power regulator must be isolated from the overall system power-distribution ground. It also must be diode-isolated from the cable power connection to avoid sinking power, if the external cable's voltage is higher than the cable power-supply voltage in this enclosure or if the internal power supply itself is turned off *(Fig. 2)*.

This design also illustrates another feature of the 1394's physical architecture—the use of external cable power for powering the PHYs. The power available from the cable can be very highly unregulated. It must be between 20 and 33 V, and therefore, is nearly always unsuitable for direct use as PHY power. A regulator will typically be used between the external cable power and the PHYs. In this case, the external cable ground is connected only to the regulator and the PHY—it can't be connected anywhere else inside the enclosure.

For floating devices, such as a portable PC, an integrated PHY-link IC could be used without PHY-link isolation. If the portable is powered or charged from an ac power line, the burden of electrical isolation is put on the power brick. Note that extra precautions must be put on external connectivity. Parallel and serial ports where portables are connected to ac- powered devices can be used to provide grounding. The rule of thumb is that any floating device equipped with external connections to ac-powered devices must be 1394-bus isolated.

For 1394-bus usage to become widespread, semiconductor vendors need to gear up to produce standardized 1394 PHYs and support components using advanced high-volume processes and increasing levels of functional integration. Initial implementations will likely consist of add-ons and modifications to existing PC designs, however the pressures of the consumer-electronics market will provide momentum to quickly move beyond the kludge stage and into robust, building-block implementations.

Gregory Urban, a marketing manager for National Semiconductor's Strategic Business Unit for the Personal Systems Group, holds a BSEE from the University of Illinois.



2. To provide electrical isolation, the cable power regulator must be isolated from the overall system power-distribution ground. In addition, the power regulator must be diode isolated from the cable power connection.

How Valuable	Circle
Highly	525
Moderately	526
Slightly	527

READER SERVICE 128

WHAT'S ON BOARD

Able to reduce the complexity of multimedia subsystems, the VxP195 multimedia controller developed by AuraVision Corp., Fremont, Calif., lets designers create full-function multimedia cards. These cards can handle video applications such as PC-based video editing, videoconferencing, and playback of MPEG-2 streams from DVD players and digital-video broadcasts. The chip simplifies the integration of data from multiple non-PCI audio-video sources (MPEG 1 and 2 decoders, audio codecs, Intercast decoders, etc.), requires only one PCI bus slot, and supports YUV and all popular RGB formats. On the chip are four major DMA pipelines—video in/out, audio in/out, coded MPEG or video-blinking interval, and bit-mask clipping—that act as data buffers between the multimedia devices and the PCI bus. The video channel supports simultaneous DMA transfers of capture and display data. As a result, the chip can execute up to five simultaneous DMA operations. With the multiple pipelines, the chip can enhance, scale down, and crop or filter the incoming video stream. Interpolation is performed for both horizontal and vertical scaling, and the Luma and chroma filters are two-dimensional. A dedicated 64-byte clipping FIFO buffer overlays a video window with a graphics window; it supports both pixel-by-pixel or rectangular overlays. The chip's video module interface (VMI) port allows video data to be sent directly into a VGA subsystem's video port, thus avoiding PCI bottlenecks in systems where available bandwidth is limited, such as CCIR656 and MPEG-2 applications. Samples are available, and in large quantities, the chip will sell for less than $20. Contact Jens Jensen, (510) 252-6800.

Users of workstations that employ SPARC-based CPU modules now have an upgrade option that delivers single or dual CPUs running at 180 MHz. Developed by Ross Technology Inc., Austin, Texas, the hyperSPARC MBus upgrade modules incorporate one or two hyperSPARC processors and tightly-coupled 512-kbyte secondary caches. The upgrade cards are the company's first based on the their enhanced version of the hyperSPARC CPU. Systems such as the SPARCstation 10, 20 and SPARCserver 630/670 and 690, or compatibles, can readily be upgraded with this "user" installable upgrade module. Based on a 0.35-micron triple-level metal CMOS process, the 180-MHz hyperSPARC CPU, cache and system controller chip, and cache memory—all mounted on one substrate—deliver system performance of 200 SPECint92 and 219 SPECfp92. The dual-CPU version delivers a SPECrate_int92 rating of 8893 and a SPECrate_fp92 rating of 9470. An even higher-performance version with 1 Mbyte of cache per CPU also is available. To get some of the improved performance, the CPUs incorporate an enhanced on-chip first-level cache that packs 16 kbytes of 4-way set associative storage, which reduces pipeline stalls. An improved floating-point processor can deliver results in two clock cycles rather than three. Contact Matt Gutierrez, (512) 436-2117 or see the company's web site at http://www.ross.com.

A block-lockable EEPROM designed to support microcontrollers such as Intel's MCS251, as well as 8051, 80196, and 88/188 class processors, provides 8 kbytes of segmented storage. The X88064 EEPROM, developed by Xicor Inc., Milpitas, Calif., is divided into eight 1-kbyte sections, with each section independently lockable, or multiple sections can be combined under a single lock. Incorporated on the chip is a mutiplexed address/data bus that allows seamless connection to buses on the 8051, 80196, and 88/188 processor families, eliminating the need for additional control-logic support circuitry. The chip supports toggle-bit polling, and page-mode writing. In the page mode, up to 32 bytes are written simultaneously. The fast address/data bus allows memory accesses in just 60 ns. In the active mode, the chip draws 30 mA from a 5-V supply; on standby the current drops to under 0.15 mA. Available in a 24-lead SOIC or plastic DIP, the chip costs $4.50 each in lots of 10,000. Contact Gary Craig at (408) 432-8888.

Employ Videoconferencing From The Road

Videoconferencing from the road is now possible using the Global Phone 1.5 software from VIC Hi-Tech Corp. The necessary hardware is a video camera, a video-capture PC Card, and a notebook computer with a telephone connection. The complete package permits two-way live videoconferencing with simultaneous voice, data, and video transmissions over standard telephone lines. A white-board feature allows application sharing and joint viewing of images or documents. Up to eight sites can be linked simultaneously over a LAN or WAN TCP/IP network. The company offers a Type I PC Card that's compatible with the Global Phone 1.5. The software supports compression and decompression of PAL, NTSC, S-Video, composite, or monochrome images within a Windows 95 environment. The Global Phone 1.5 software sells for $149. The enabling PC Card costs $415. Video cameras range from $299 to $2569.

VIC Hi-Tech Corp., *2221 Rosecrans Ave., Suite 237, El Segundo, CA 90245; (310) 643-5193; http://www.vic-corp.com*

CIRCLE 493

Chip Connects USB To PCI Local Bus

The USB0670 PCI-to-USB controller chip is suitable for desktop PCs, portable computers, docking stations, PDAs, and other platforms. The part, housed in a 100-pin package, lets system designers bring USB-enabled products to market quickly. Based on the OpenHCI specification, the part also complies with the PC97 Hardware Design Guide. It handles most of the USB protocol processing, eliminating any associated latencies, as well as the the extra overhead from the host microprocessor. Software support is available from the company. Operating-system support comes bundled with the latest version of Windows 95. The USB00607 USB-to-PCI controller is available immediately.

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CIRCLE 494

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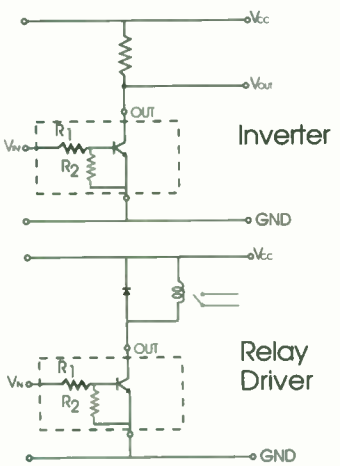
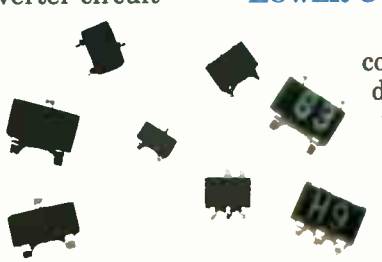
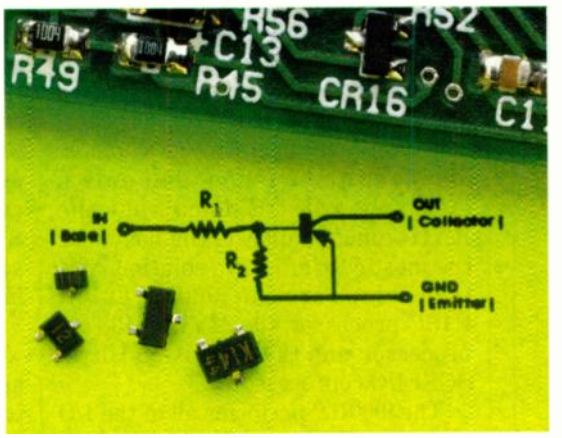


In inverter or relay drive circuits, for example, all the functions of a transistor switch are present in one part. One resistor controls the base current; the other works as a pull-down resistor to cut off transistor operation. The built-in bias resistor allows inverter circuit configuration without an external resistor for input.





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PRODUCT FEATURE

Add RAID On Motherboard Or As An Add-In Card Using Three-Chip Set

Mylex Corp.'s scalable RAID products are broken into three configurations of products: chip-level, board-level, and a half-and-half hybrid solution. Each takes advantage of a three-part chip set. The chip-level part, called Rome, is designed to be embedded onto a motherboard. OEMs can put the RAID functionality on the board for the most cost-effective solution. The three chips are the i960RP 32-bit RISC processor, the MYL-86138 coprocessor, and the BA-81C15 Ultra-SCSI I/O coprocessor.

The i960RP performs all of the I/O processing functions, freeing the host CPU for other tasks. The MYL-86138 functions as the XOR engine, generating parity information needed for RAID level 5 fault tolerance and write performance. It also functions as a cache controller to increase the speeds of reads and writes. The BA-81C15 minimizes the SCSI command overhead by reducing the number of interrupts generated to the host CPU.

The board-level product is called the DAC960PG. It's an add-in card that connects to the PCI bus, offering up to three SCSI channels. The board lets OEMs treat RAID as an upgrade that doesn't require any motherboard real estate. Lastly, the DAC960PC is a product that's part motherboard solution and part add-in card. In this configuration, the i960RP and MYL-86138 part would reside on the add-in card, while the BA-81C15 chip would be on the motherboard. The purpose of this setup is to give RAID functionality to systems that are already SCSI-enabled (but not RAID-enabled). The DAC960PC would plug into one of the existing PCI slots.

All of the products are compatible with the company's Global Array Manager, an integrated RAID software package that allows network administrators and end users to remotely monitor, configure, manage, and add storage to the RAID system. Support is available for most standard operating systems, including Windows NT, Netware, OS/2, Unix, and Solaris.

The DAC960PC will sell for about $950. The DAC960PG ranges from $1050 to $1350, depending on the number of channels. Rome prices vary depending on SCSI channel configurations and volume.

Mylex Corp.
34551 Ardenwood Blvd.
Fremont, CA 94555
(510) 796-6100.
CIRCLE 495
RICHARD NASS

Processors Accelerate 3D Graphics And Video

Aimed at high-end graphics subsystems, the Virge/DX and Virge/GX 3D multimedia accelerators provide 30-frame/s performance in DRAM, SDRAM, or SGRAM systems. Features of the chips include an integrated 170-MHz RAMDAC, as well as mip-mapping and trilinear filtering to remove visual artifacts. A transparency capability enables realistic rendering of objects like glass, water, and plastics. Atmospheric effects such as fog and depth cueing enable the rendering of real-world environments. Lastly, a buffer speeds the removal of hidden surfaces to improve overall quality and visual performance. In addition to accelerating 3D games, the Virge GX/DX chips are suited for next-generation business desktop applications, including data visualization, and accelerated VRML.

The difference between the two Virge chips is in the memory types that they support. The DX works with DRAM, while the GX operates with SDRAM or SGRAM. Both parts are available now. In lots of 10,000, the Virge/DX sells for $28 each, and the Virge/GX costs $29 each.

S3 Inc.
2770 San Tomas Expwy.
Santa Clara, CA 95051
(408) 980-5400
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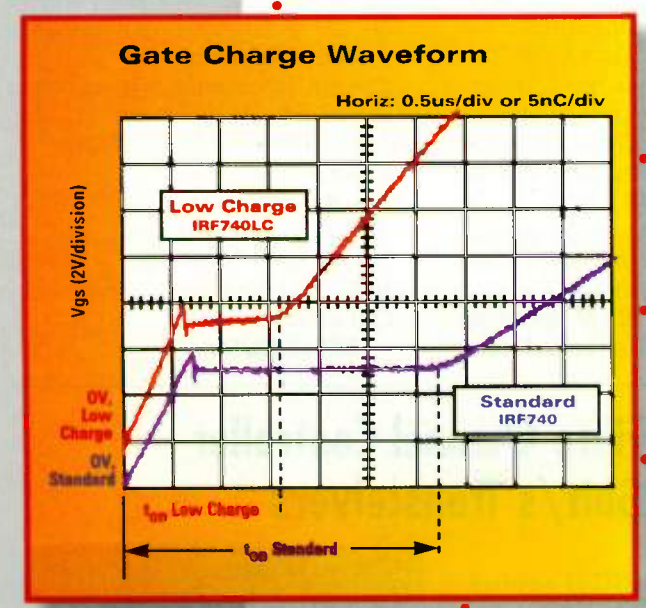

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READER SERVICE 130

PRODUCT FEATURE

Shared-Memory-Architecture Graphics Controller Eliminates North-Bridge Chip

The purpose of a unified-memory architecture is to save cost by reducing the memory requirement in a PC. By integrating a PC system controller and multimedia accelerator onto one chip, the 86C551 goes one step further. It eliminates the need for the North Bridge controller chip. S3 says the part supports a shared-memory architecture (SMA).

The graphics frame buffer can range in size from 512 kbytes to 4 Mbytes, depending on need. Graphics performance is improved because data is always transferred between the graphics controller, memory, and the CPU over a 64-bit bus.

The 86C551 supplies an integrated direct-mapped write-back secondary cache controller and supports various SRAM types. The DRAM controller supports fast-page, extended-data-output, and synchronous DRAMs with programmable timing. The graphics acceleration is produced by the S3 Trio64V+ accelerator, which also offers video acceleration. The streams processor allows mixing of three separate display streams. It also can do on-the-fly stretching and blending of a primary RGB stream with a secondary RGB or YUV video stream while the hardware cursor overlays the other two streams.

The 86C551 is housed in a 388-pin BGA package. Available now, the chip sells for $30 each in lots of 10,000.

S3 Inc.
P.O. Box 58058
2770 San Tomas Expwy.
Santa Clara, CA, 95052
(408) 980-5400.

CIRCLE 497

RICHARD NASS

Single-Chip Fibre Channel Controller Supports 1-Gbit/s Transceivers

High-bandwidth SCSI applications are the target for the ISP2100 PCI-to-Fibre Channel controller. The chip supports 1-Gbit/s transceivers, enabling direct connection to copper or fiber-optic cabling. The part is manufactured in a CMOS process, reducing the cost from previous products that were fabricated using gallium arsenide.

The ISP2100 single-chip controller supports a 264-Mbyte/s, 64-bit PCI host interface, a RISC processor that manages the data flow between the host system and the Fibre Channel interface, and a 1-Gbit/s Fibre Channel engine. The engine manages the Fibre Channel interface at the protocol level. By definition, Fibre Channel maps several common transport protocols, allowing it to merge high-speed I/O and networking functionality.

The ISP2100's three concurrently operating DMA channels support a 64-bit internal data path to help ensure maximum throughput. Specifically, the channels handle the command information, and the transmit and receive data.

The ISP2100 is housed in a 256-pin ball grid array. Samples of the chip are available now, with production commencing later in the first quarter. Prices start at $150.

QLogic Corp.
3545 Harbor Blvd.
P.O. Box 5001
Costa Mesa, CA 92628
(800) 662-4471 or
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CIRCLE 498

RICHARD NASS

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CIEE '97 is known for its consistently high-quality base of attendees. These attendees are influenced by the show's organizers, CEIEC and CCPIT. The CEIEC is the US$2.5 billion import-export arm of the Ministry of Electronics Industry and the seventh largest trading company in China. Prior to the show, Exhibitors will be able to utilize the CEIEC's extensive network of 41 branch offices and over 100 affiliate electronics companies in China to distribute information and literature to buyers and specifiers of overseas electronics products throughout the country. Exhibitors will also have the inside track on import/export information and be able to take advantage of meetings and trade negotiations during the show.

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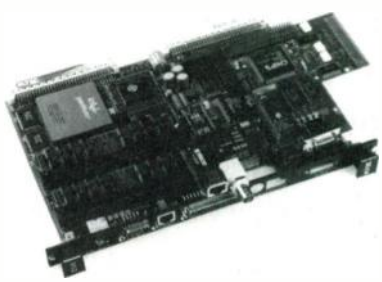
Sparc-Compatible Workstations Hold Dual CPUs

The Ultima 1 and 2 Sparc-compliant workstation and server platforms are built with a modular design, allowing users to upgrade from a single-processor system to dual CPUs. The difference between the two models is in the number of processors. Both units can hold UltraSparc processors, ranging in speed from 167 to 250 MHz. In addition, the Ultima 1 can hold 1 Gbyte of DRAM, while the Ultima 2 has room for 2 Gbytes. Support for 100-Mbit/s Fast Ethernet and 20-Mbyte/s fast and wide SCSI is integrated directly into the workstations' motherboard, leaving users with four available SBus slots for customization. The systems are built with a unique chassis design that employs sliding trays for easy upgrades and maintenance. Prices for the Ultima 1 workstation start at $9995, with a 167-MHz processor, 64 Mbytes of DRAM, and the Solaris operating system. In a similar configuration, the Ultima 2 sells for $14,995.

Axil Computer Inc.
3151 Coronado Dr.
Santa Clara, CA 95054
(800) 284-AXIL or
(408) 486-5700
http://www.axil.com
CIRCLE 630

Pentium-Based VME SBC Runs PC Software

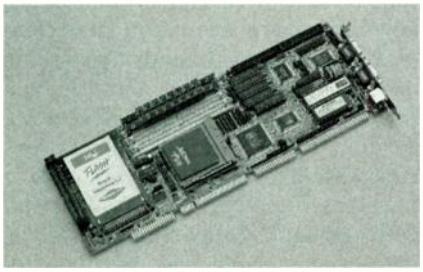
The E128 Pentium-based single-board computer combines the advantages and versatility of both the VMEbus and the personal computer. With a microprocessor ranging in speed from 75 to 166 MHz, the board is built with an internal PCI bus. The on-board PCI-based Super VGA controller supports standard monitors as well as flat-panel displays. The VME-PCI interface is implemented using the Universal chip from Tundra Semiconductor. Expansion is handled through a PC/104 interface. A network connection can be made over 10Base-5, 10Base-2, or 10Base-T. Main memory can be expanded to 128 Mbytes using standard SIMMs. The board can run all PC-compatible software, including Windows 95, Windows NT, and DOS. Prices for the E128 board start at $4920, with large quantity discounts available.



American Eltec Inc.
101 College Rd. East
Princeton, NJ 08540
(609) 452-1555
http://www.eltec.de
CIRCLE 631

Single-Board Computer Connects To ISA, VL, PCMCIA

The GMS486-VL is a passive-backplane single-board computer that's designed for industrial and embedded applications. One of its features is an integrated PCMCIA adapter. Any of the Intel 486 family of processors can

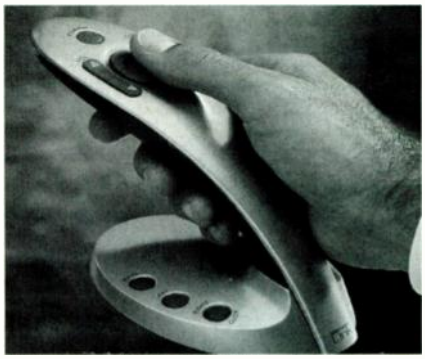


reside on the board, allowing users to match the processor with their application. It is built with a connection to the ISA bus as well as the VESA VL-Bus local bus. An additional connector brings many of the necessary connection points, including keyboard and status LEDs, to the passive backplane. The dual PCMCIA interface supplies one connector on the board and a second for external use. The GMS486-VL supplies support for two IDE drives and two floppy drives and a parallel and two serial ports. Standard configuration includes 128 kbytes of cache memory, upgradable to 1 Mbyte. The operating temperature ranges from 0 to 70°C, while the storage temperature runs from -20 to 100°C.

Granite Micosystems
10202 North Enterprise Dr.
Mequon, WI 53092
(414) 242-8816
CIRCLE 632

Remote Control Works With Internet Boxes

By employing the RemoteLink, users can get one-touch control over today's audio and video components as well as Internet appliances. The device combines an Internet-ready remote control with on-screen displays to deliver one-touch control of televisions, VCRs, CD players, and Internet-access and set-top boxes. While there are similar devices available that can access multiple appliances, the RemoteLink offers cursor navigation for the Internet box. System control is achieved using two

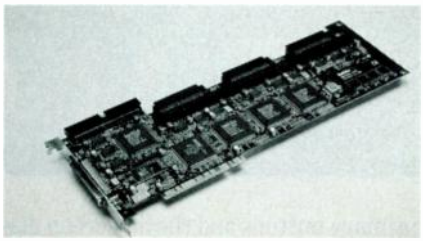


primary buttons and the on-screen display. Five other buttons are dedicated to specific functions.

Interlink Electronics Inc.
546 Flynn Rd.
Camarillo, CA 93012
(805) 484-8855
http://www.interlinkelec.com
CIRCLE 633

SCSI Host Adapter Connects Up To 60 Devices

By incorporating a quad-channel SCSI controller, the UltraConnect series of host adapters can connect up to 60 SCSI peripherals on one PCI-based add-in card. With the board, users can get four separate channels that offer compatibility with UltraSCSI (20 Mbytes/s), UltraWide SCSI (40

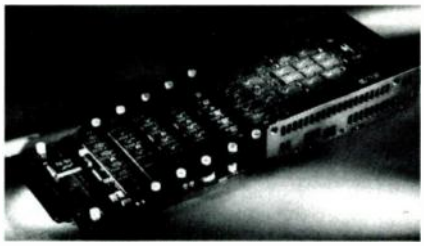


Mbytes/s), and legacy SCSI and SCSI II devices. With the maximum number of connected devices, potential storage capacity reaches 780 Gbytes in one PCI slot. Suitable applications include CD-ROM servers, video-on-demand systems, and imaging systems. Most standard operating systems are supported. A bundled user-friendly, BIOS-resident setup utility, called SmartSCSI, lets users boot from any channel and control individual device configuration and host-adapter termination.The UltraConnect family of SCSI host adapters costs $379.

Initio Corp.
2901 Tasman Dr.
Suite 201
Santa Clara, CA 95054
(408) 988-1919
http://www.initio.com
CIRCLE 634

Solid-State Disk Processes 2400 I/Os Per Second

Up to 804 Mbytes of data can be stored in the ESP3080R-V solid-state disk drive. Fitting in a 3.5-in. form factor, the drive connects to the host through a single-connector attachment (SCA-2). The drive is a volatile disk, meaning that it does not retain data when power is removed. Applications that suit such a device includes a RAID architecture, where the solid-state disk can augment an existing cache subsystem to improve overall system performance. The drive offers near-instantaneous data delivery and can process 2400 I/O re-



quests/s. Data throughput approaches the limits of its fast and wide SCSI bus (20 Mbytes/s).The drive is bundled with plug-and-play software, meaning that no special drivers are required.

Quantum Corp.
500 McCarthy Blvd.
Milpitas, CA 95035
(800) 624-5545 or
(408) 894-4000
http://www.quantum.com
CIRCLE 635

3.0-in. Disk Drive Holds 2 Gbytes

Designed for portable PCs, the N2160-3AR hard-disk drive stores up to 2 Gbytes of information in a 12.5-mm high, 3.0-in. form factor. Fitting into

the Nordic family, the drive lets system designers build portable computers with desktop functionality. The drive features SMART capability, integrated power-management modes, an average seek time less than 14 ms, a disk rotational speed of 4103 rpm, a 128-kbyte cache-memory buffer, a PRML read channel, and a Fast-ATA 3, PIO Mode 4 interface capable of transferring up to 16.6 Mbytes/s. A unique voice-coil-motor manufacturing technique improves the drives noise level, heat dissipation, and reliability. An embedded servo eliminates the need for thermal recalibration..

JTS Corp.
166 Baypointe Pkwy.
San Jose, CA 95134
(408) 468-1800
CIRCLE 636

Software Lets Users Treat Tape Like A Disk

Users of tape drives can view the peripheral as a logical hard-disk drive using the File Xpress. By simulating a random-access device, large files can be transferred and run directly from tape. As a result, multimedia users can take better advantage of their available hard-disk space to run more complex applications. In addition, on-line data can be temporarily stored on tape to avoid using critical disk space. According to the company, File Xpress runs 10% faster than any competitive product. The software supports all conventional file operations, such as delete, copy, move, rename, and execute. The software supports most popular peripheral interfaces, including ATAPI, SCSI, and parallel port. It runs under Windows 95 or Windows NT. File Xpress sells for $29. Evaluation copies can be downloaded from the Internet for a 30-day live trial.

Shuttle Technology
43116 Christy St.
Fremont, CA 94538
(510) 656-0180
http://www.shuttletech.com
CIRCLE 637

Software Helps NT Run On A Portable

A pair of software products have been developed to run the Windows NT operating system on a portable computer. CardWizard for Windows NT is a comprehensive plug-and-play product designed for portables that includes PC Card functionality. The product incorporates such features as hot-swapping and automatic resource configuration. The second offering, PowerProfiler for Windows NT, is a power-management solution that works closely with the Windows NT operating system. The software extends the platform's battery life by adding power-management capabilities to the operating system and also allows users to create personalized power-management settings.

SystemSoft Corp.
2 Vision Dr.
Natick, MA 01760
(508) 651-0088
http://www.systemsoft.com
CIRCLE 638

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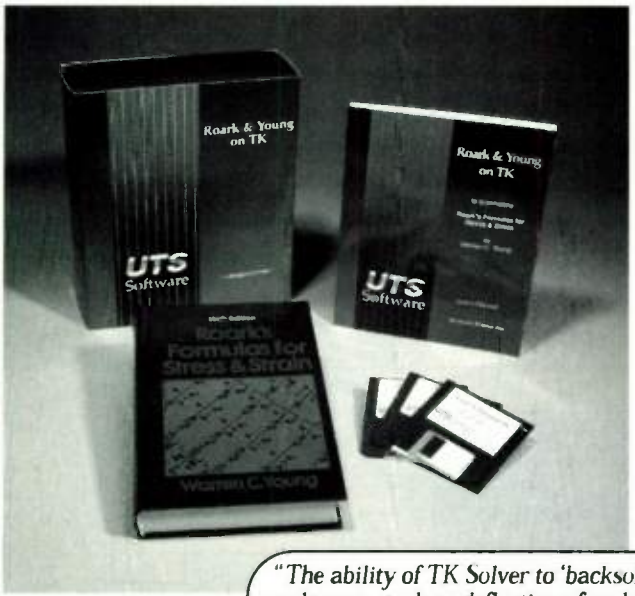

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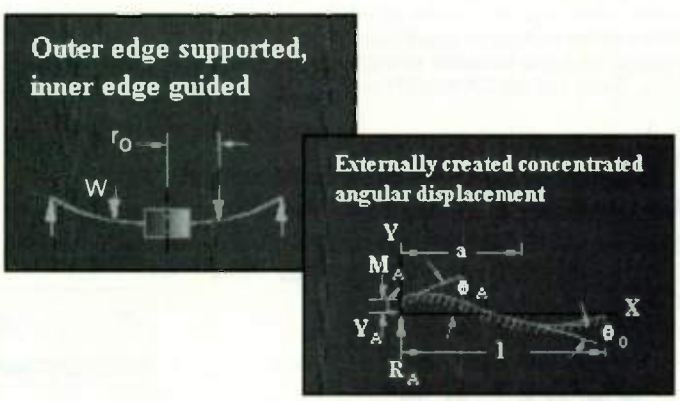

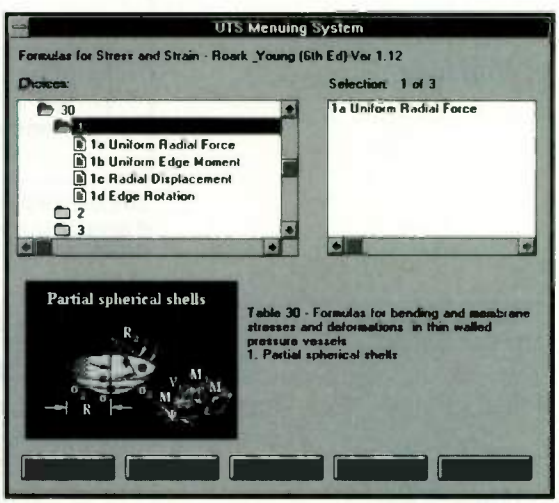

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Compact IC Performs 3 Power-Supply Jobs for Wireless Handsets

The MAX768 is a small, low-noise, dual-output charge pump with a power-ready indicator. This single IC does three important jobs: it biases a GaAsFET power amplifier, powers a voltage-controlled oscillator (VCO) or LCD, and protects the GaAsFET by controlling the drain switch until the negative bias is within regulation. It provides positive and negative outputs using only low-cost capacitors. Two internal linear regulators provide independently-adjustable low-noise regulated outputs. Use it in low-voltage systems where a simple charge-pump inverter is inadequate, or where the VCO needs more range to improve phase noise.

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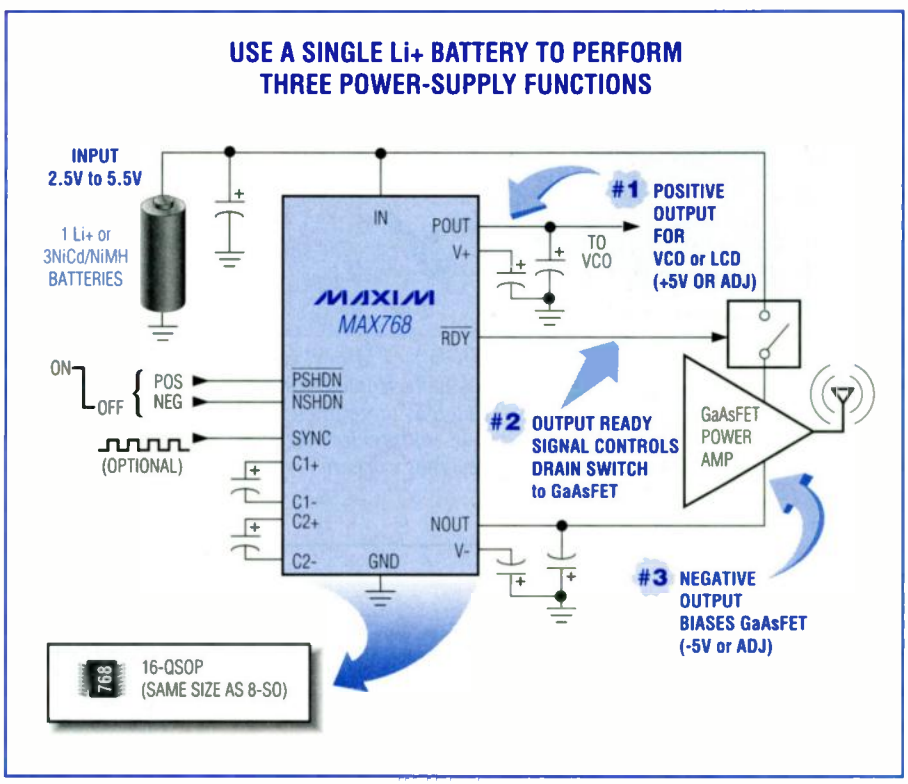

The MAX768 provides three important functions using only small, low-cost capacitors. It simplifies low-voltage designs powered directly from a single lithium-ion or three NiCd/NiMH batteries. Order the MAX768EVKIT evaluation board.

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Circle No. 135 - For U.S.Response
Circle No. 136 - For International

Circle 520

Battery-Switchover Circuit Accommodates 3-V Systems

RON YOUNG and LUONG HUYNH
Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086; (408) 737-7600.

Portable systems often include the flexibility to operate either from an internal battery or from an ac-dc wall adapter. Many such systems include circuitry that switches automatically between an internal battery and an external source as the user connects and disconnects the wall adapter.

The circuit shown implements this idea with a dual linear regulator, one side of which is preset for a regulated output of 2.84 V (other versions of the IC offer 2.80-V and 3.15-V outputs) *(see the figure)*. The other side of the regulator is configured to allow user-adjustable outputs, but in this case it monitors the wall-adapter voltage.

When that voltage is removed by unplugging the adapter, the regulator's pass transistor routes battery current into the IC for support of the 2.84-V output (current flow in this transistor is counter to that of most applications).The input bypass capacitor (C1) provides enough holdup time for seamless transitions between the battery and adapter voltages.

Resistors R1 and R2 sense the wall-adapter voltage and determine the switchover threshold V_{SW}:

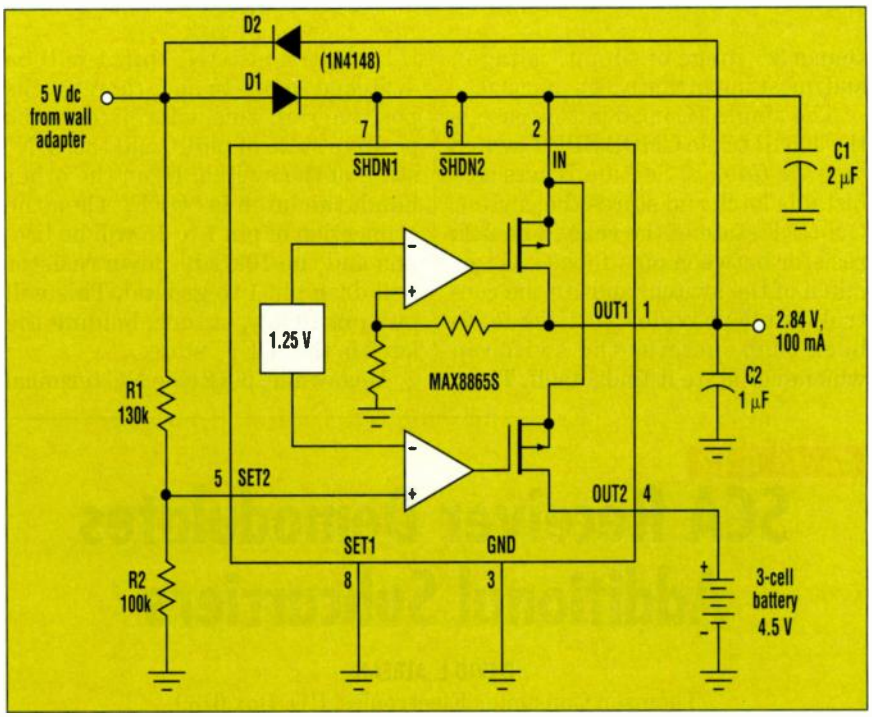
$$V_{SW} = V_{set}\left(\frac{R1+R2}{R2}\right)$$

$$= 1.25V\left(\frac{130k+100k}{100k}\right) = 2.875V$$

Diode D1 isolates the wall-adapter voltage so that the battery can't cause limit-cycling by retriggering the switchover. D2 holds the IC's "Dual Mode" input in the external-feedback mode by maintaining a minimum voltage at the SET2 input.

Battery operation interposes two pass transistors in series between the battery and the regulated output, which doubles the regulator's dropout voltage. These transistors have on-resistances of about 1.1 Ω each. To prevent battery current from bleeding through the OUT2 transistor's intrinsic body diode (when operating from the wall adapter), the wall-adapter voltage should be equal to or greater than the maximum battery voltage.

If the regulators are turned on and off with the shutdown inputs *SHDN1 and *SHDN2, then the MAX8865 should be used rather than the MAX8866, which has an auto-discharge feature that attempts to discharge the battery. As shown, the MAX8865S with a 5-V wall adapter and three-cell battery will provide up to 100 mA at 2.84 V.



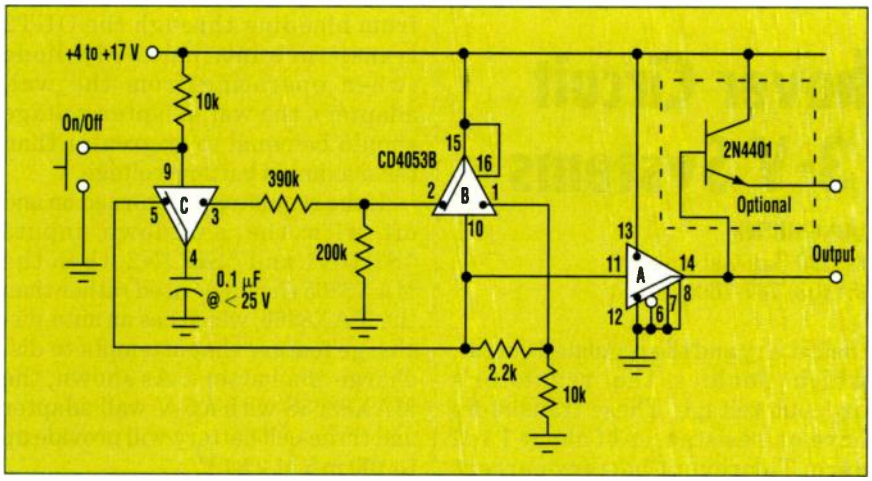
This linear voltage regulator with automatic switchover circuitry maintains a 2.84-V regulated output during connection or disconnection of the wall adapter.

Circle 521

Solid-State Circuit Replaces Latching Relay

W. STEPHEN WOODWARD
Venable Hall, CB3290, University of North Carolina, Chapel HIll, NC 27599-3290; Internet: woodward@net.chem.unc.edu

There are a multitude of simple circuits that perform switch debouncing, as there are many ways to implement a toggling latch. The circuit illustrated here merges these functions into one topology, is extremely tolerant of power-supply variation (it works fine over more



This unusual solid-state latching relay performs well over a wide supply voltage range.

than a 3:1 range of supply voltage), and, most importantly, it's unusual.

The single IC used in this case is the 4053B triple CMOS SPDT switch *(see the figure)*. Section B acts as a bistable latch and stores the current ON/OFF state of the relay. The 2.2k resistor between pins 1 (the NO terminal of the switch) and 10 (the control input) provides positive feedback that sustains the switch in whichever state it finds itself. Thus, if the latch is "ON," pin 1 will be switched to pin 15 and, thereby, the positive rail. This will reinforce the positive state of pin 10 and the "ON" state of the switch. If, on the other hand, the latch is "OFF," then the connection of pin 1 to 15 will be broken and the 10k pull-down resistor will drag pin 1 to ground. This will pull pin 10 low, in turn, holding the latch in the "OFF" state.

Meanwhile, pin 2 (the NC terminal of section B) will output the logic inverse of the signal appearing in pin 1. This signal communicates to pin 3 (NO of section C) and, if the control pushbutton is open, will connect to pin 4 and charge the capacitor to a state opposite that of the latch. Thus matters will rest until someone presses the button. This will connect the capacitor to pin 10 and toggle the latch state.

The approximately 40-ms time constant of the 0.1-µF capacitor and pin 2-3 resistance prevent even prolonged pushbutton contact bounce from disturbing the charge of the capacitor and messing up reliable toggling of the latch. When the button is later released, the connection of the capacitor to pin 3 is reestablished and the capacitor will recharge in preparation for the next toggle.

4053B section A serves as an output buffer and has an output impedance of about 200 Ω when run with a 5-V supply and 100 Ω with a 12-V supply. If this is insufficient for the application, a transistor emitter follower like that illustrated will boost output capability to beyond 0.1 A.

Circle 522

SCA Receiver Demodulates Additional Subcarriers

DAVID L. ALBEAN
Thomson Consumer Electronics, P.O. Box 6139,
Indianapolis, IN 46206; (317) 587-4950; fax (317) 587-6779.

The FCC has authorized some FM radio stations to broadcast uninterrupted background music for commercial use on one or more FM subcarriers. This service is known as subsidiary carrier authorization (SCA). This is done via a frequency-modulated subcarrier, typically at 67 kHz

However, in some cases, additional subcarrier(s) are present. Each of these subcarriers is FM-modulated with different program material. A common second subcarrier frequency is 91 kHz. These frequencies were chosen so as to minimize interference with the normal stereo programming. They're also present at a much lower level than the main channel information, usually at only about 5 to 10% FM deviation of the main carrier frequency. This SCA receiver can provide commercial-free music from one of two possible carriers. The SCA signal is monaural, and is relatively wideband (7 kHz). This bandwidth is adequate for reasonable quality music transmission.

A simple PLL-based FM demodulator can be made to demodulate these two subcarriers and provide a source of background music. A couple of references help to illustrate a simple SCA receiver design[1], and the basics of the PLL FM detector[2]. The receiver described here provides some enhancements to that basic design, such as better selectivity, the choice of two possible subcarriers, and an optional squelch circuit *(see the figure)*.

The input to this receiver is fed from the wideband audio output from an FM radio's first FM detector. This is the point that feeds the FM stereo demodulator in an FM receiver. Care should be taken so that the signal is tapped off at a point which hasn't yet been filtered (the subcarrier(s) are still present).

This FM input signal is then passed through a second-order high-pass filter and peaker stage (Q1), which serves to bandpass and provide additional gain within the input spectrum prior to the FM demodulator input. The FM detection is accomplished by a simple LM565 PLL IC (U1) operating as an FM demodulator.

The PLL's VCO is tuned to 91 kHz via R_T/C_T. The demodulated output signal is available at pin 7, which is followed by a second-order

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ERA-1SM	DC-8000	11.8	11.3	5.5	26.0	40	1.85
ERA-2	DC-6000	15.6	12.8	4.7	26.0	40	1.95
ERA-2SM	DC-6000	15.2	12.4	4.6	26.0	40	2.00
ERA-3	DC-3000	20.8	12.1	3.8	23.0	35	2.10
ERA-3SM	DC-3000	20.2	11.5	3.8	23.0	35	2.15
ERA-4	DC-4000	13.5	▲17.0	5.5	▲32.5	65	4.15
ERA-4SM	DC-4000	13.5	▲16.8	5.2	▲33.0	65	4.20
ERA-5	DC-4000	18.8	▲18.4	4.5	▲33.0	65	4.15
ERA-5SM	DC-4000	18.5	▲18.4	4.3	▲32.5	65	4.20
ERA-6	DC-4000	11.3	▲18.5	8.4	▲36.5	70	4.15
ERA-6SM	DC-4000	11.3	▲17.9	8.4	▲36.0	70	4.20

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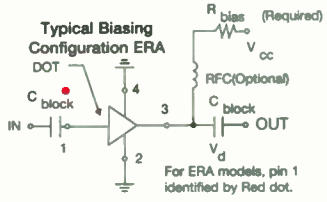
120x60	.002, .047, .068, .1 µf

ERA-1 ERA-1SM
ACTUAL SIZE



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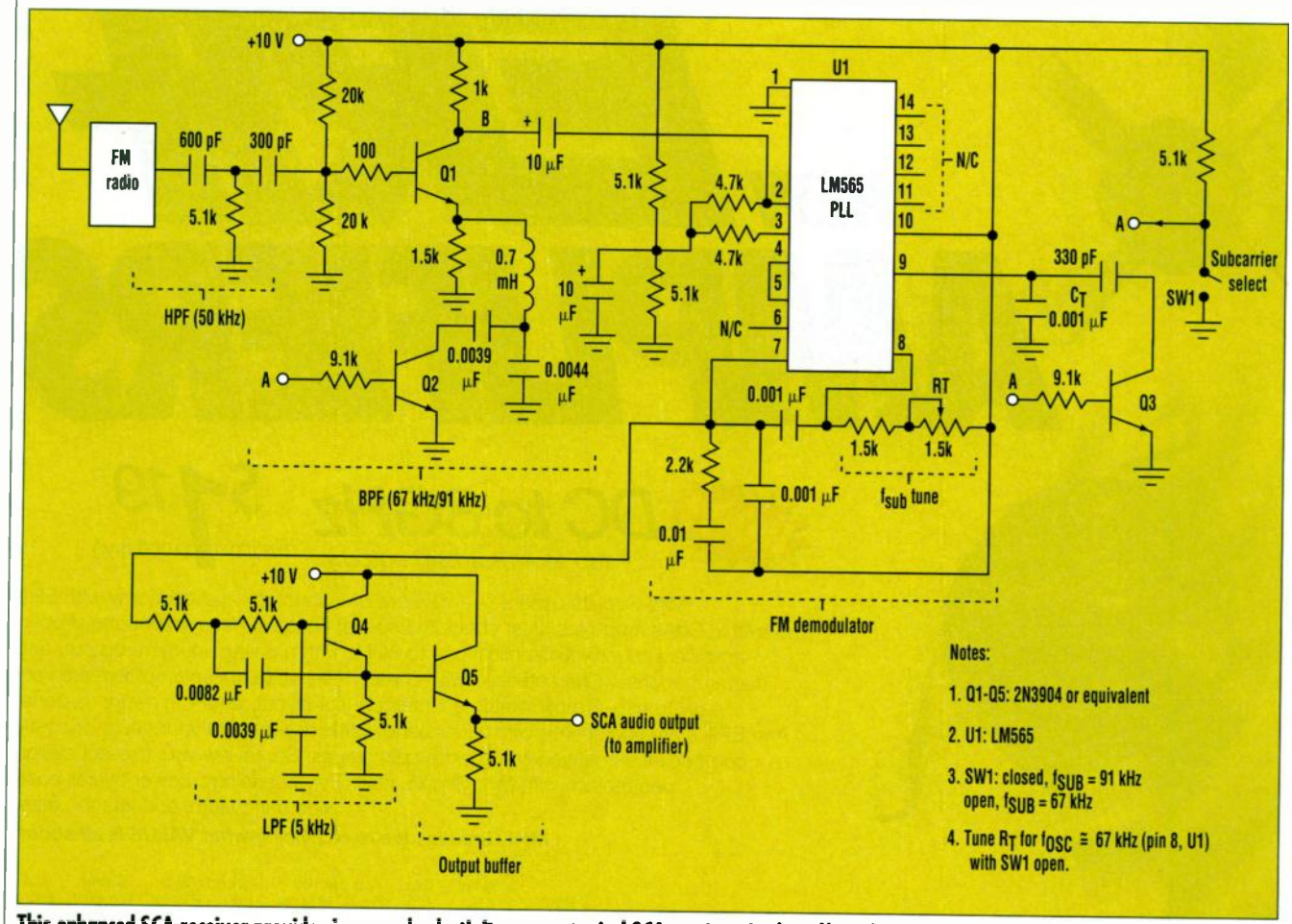

This enhanced SCA receiver provides improved selectivity over a typical SCA receiver. It also offers the listener a choice of two possible subcarriers to make use of all subcarriers currently in popular use.

LPF/buffer combination (Q4). The characteristics of this filter can be modified to suit the user.

The design shown has an audio corner frequency of about 5 kHz. The filtered output is the recovered audio output and is the input to an audio amplifier. To choose the second subcarrier (67 kHz), the peaker and VCO are gang-tuned by the Q2 and Q3 saturating switch transistors. These devices switch in appropriate-valued parallel capacitors to re-tune the peaker and VCO to the proper frequency for reception of the second subcarrier signal.

Circuit values shown are for an FM level of about 50 to 300 mV rms at the input to the peaker stage. In addition, the PLL dynamic characteristics can be altered as desired by modifying the loop filter[2]. The typical recovered audio level at pin 7 of U1 is 200 mV rms. Other enhancements could include a "squelch" circuit, which mutes the demodulator's output if the input carrier frequency is lost.

To receive SCA signals, the FM receiver can simply be tuned to normal FM stations and then the presence of either or both subcarriers can be checked. Checking can be done with a spectrum analyzer or by simply listening to the SCA receiver output on each of the two subcarriers. A list of FM radio stations in a particular region that carry SCA (and at what subcarrier frequencies) may be available.

One caveat: The SCA service is typically a pay-for-use service, thus the receiver should not be used for commercial applications.

References:

1. V. Lakshminarayanan, *Electronic Circuit Design Ideas*

2. *National Semiconductor Linear Applications Databook*, 1986 edition (AN46 and AN146).

IFD WINNERS

Alexander Eisen, State University of NY, Physics Dept., 239 Fronczak Hall, Buffalo, NY 14260. The idea: *"Data Acquisition Made Easy."* May 1, 1996 Issue.

Gerald L. Kmetz, Micrel Semiconductor, 1849 Fortune Dr., San Jose, CA 95131. The idea: *"Regulator Adjusts From 0V to 25V."* May 13, 1996 Issue

Yongping Xia, 23008 Arlington Ave., Torrance, CA 90501. The idea: *"Measure Temp Through Printer Port."* May 28, 1996 Issue

W. Stephen Woodward, University of North Carolina, Venable Hall, CB3290, Chapel Hill, NC 27599-3290. The idea: *"3-Wire RS-232 to RS-485 Converter."* June 10, 1996 Issue.

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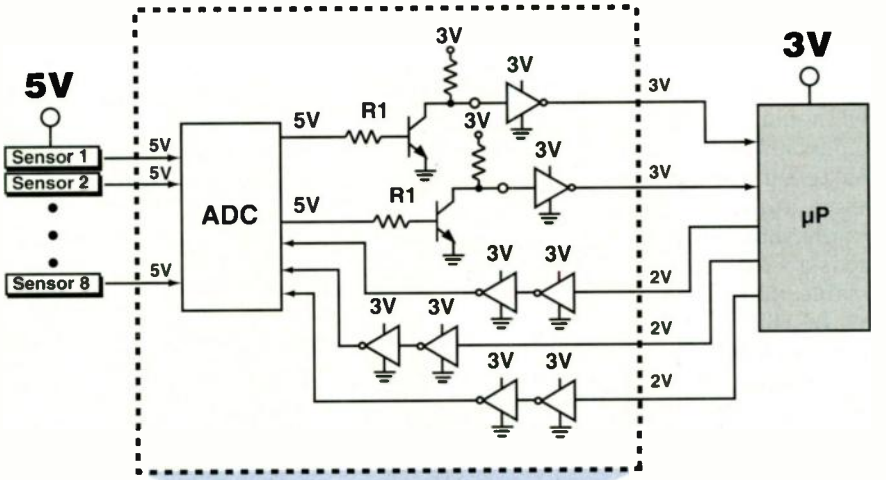

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Circle 523

Programmable Current Source for High-Efficiency Chargers

DAVID BELL
Linear Technology Corp.,
1630 McCarthy Blvd., Milpitas, CA 95035-7487.

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Constant-current sources are required in many applications, particularly when it comes to battery charging. In such applications, it's desirable that the output current is accurate, temperature-stable, and adjustable. The LT1620, a charge-current controller designed for high-efficiency switch-mode battery chargers, meets those goals *(see the figure)*.

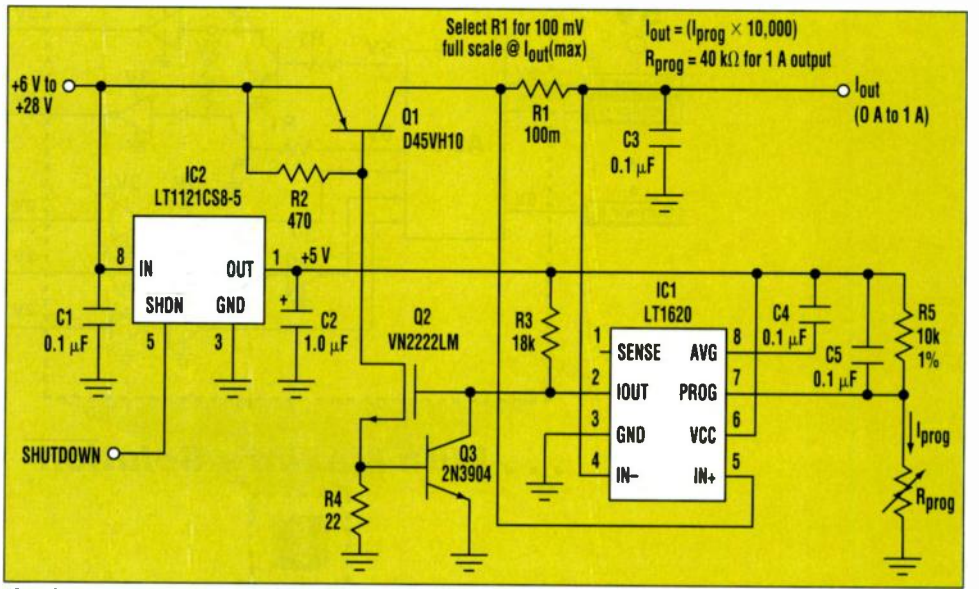
The controller also can be successfully employed as the control element in a low-cost linear current source. Output current is sensed by resistor R1, with the value selected so that 100 mV is full scale. The voltage across R1 is amplified by a factor of 10, and averaged across capacitor C4. An internal transconductance error amplifier compares the voltage on pin 8 against the programming voltage at pin 7. The error-amplifier output is present on pin 2 (I_{out}), and is level-shifted by Q2 to control the pnp pass transistor.

The LT1620's architecture allows current to be sensed in the collector of a low-cost pnp pass transistor, thereby eliminating base current errors that would otherwise affect accuracy. Output current remains controlled, even with the output shorted to ground, although current programming accuracy degrades slightly for output voltages below 4.3 V.

Output current is programmed by adjusting the voltage across R5 (1 V full scale). The LT1121 LDO regulator provides a 5-V, ±1.5% reference voltage, so current can be accurately programmed by simply connecting different values for R_{prog}. Alternatively, a PWM or voltage output DAC may be connected to pin 7 via a resistor to allow for microprocessor control.

Input voltage may range from +6 V to +28 V, with output current changing less than 0.3%. Because this is a linear current regulator, proper heat sinking must be provided for Q1, especially when operating with large input-to-output voltage differentials. Transistor Q3 and R4 limit the magnitude of Q1's base drive during dropout, preventing excessive dissipation in driver transistor Q2.

Using voltage regulator IC2, the constant-current source operates directly from the unregulated input voltage. Pulling IC2's shutdown pin low turns off V_{CC} to the entire circuit, and limits reverse current drawn from the output to less than 25 µA (important in battery-charger applications). IC2 can be eliminated entirely if another 5-V power source is available within the system.



This charge current controller, designed for high-efficiency switch-mode battery chargers, provides accurate, temperature-stable, adjustable output currents. It also can be used as a control element in a low-cost linear current source.

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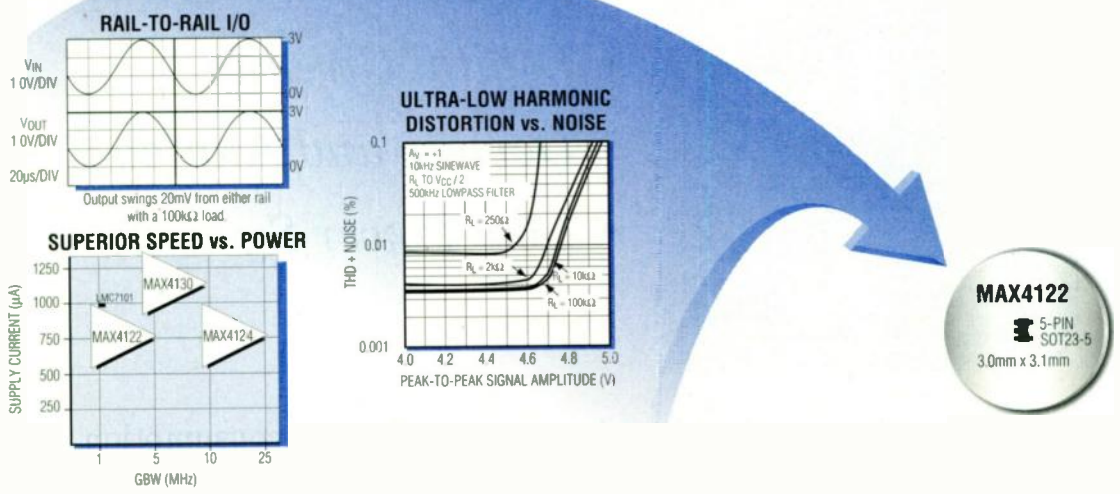

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MAX4128	Dual	No	+2.7 to +6.5	10	25	750	750	1.40
MAX4129	Quad	No	+2.7 to +6.5	1	5	750	1500	2.40
MAX4130/31	Single	Yes	+2.7 to +6.5	1	10	1050	600	0.85/0.98
MAX4132/33	Dual	Yes	+2.7 to +6.5	1	10	1050	750	1.40
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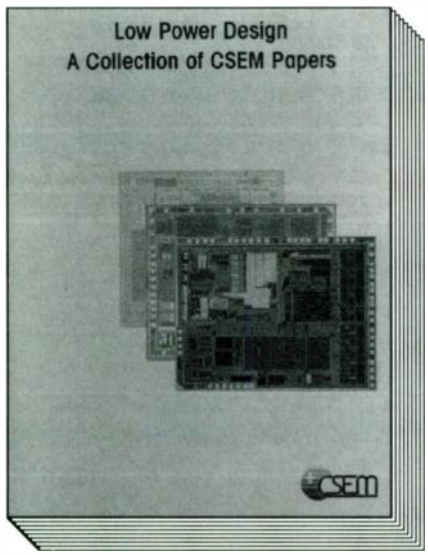

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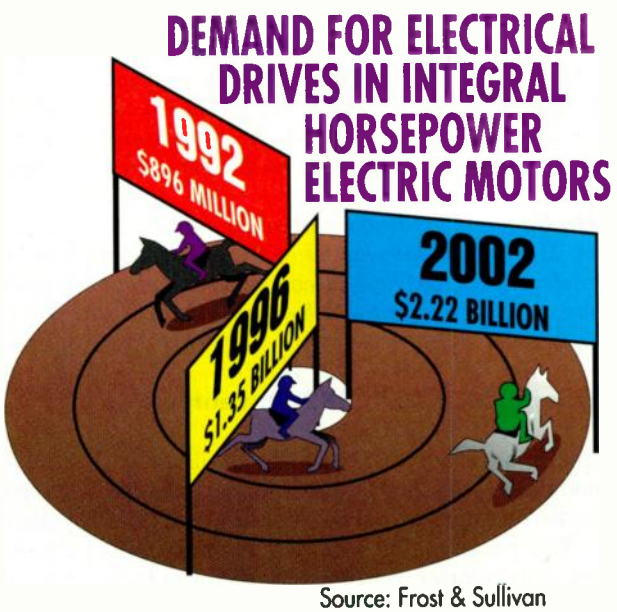
MARKET FACTS

A Horse Of A Different Power

If you wanted to horse around and look for all the different applications where integral horsepower electric motors are used, you'd be pretty tired at the end of the day. These motors show up in all kinds of places, from 10,000 horsepower (hp) bulldozers to hospital-serving, industrial-sized washing machines. According to a recent Frost & Sullivan study, "U.S. Integral Electrical Motor Markets," in 1995, the total market was estimated at $2.49 billion. That figure includes over $500 million in imports. Historically (over the last 75 years), fundamental motor technology has stayed pretty much the same, keeping competition in the field limited to customer service and minute product differences. The new report explains that since the introduction of semiconductors and electric drives, there has been a monumental change in the face of the market. Large stock manufacturers that used to lead the market are trailing behind aggressive small businesses with ground-breaking motor/drive systems. Some of the market trends Frost & Sullivan found include automation, energy efficiency, and rebuilding. Automation, a current trend throughout all industries, is driving the demand for robots with motors attached to semiconductor drives and controllers. For the last five years, demand for electrical drives has risen 10% per year from $896 million to approximately $1.35 billion in 1996. Projections in the report assert that this trend is expected to continue, reaching $2.22 billion by 2002. Energy efficiency will be greatly affected in the future with the activation of the 1992 Energy Policy Act in October 1997. The Act mandates a minimum energy efficiency rating for all squirrel-caged, T-frame polyphase induction motors with 1 to 200 hp. The new regulation will apply to 70% of the integral hp market, shaking out those firms with no (or little) commitment to research and development. Out of the 40 million estimated integral hp motors in the U.S. as of 1995, about 1.3 million will fail this year. Those motors will require either rewinding or replacement. Only half of the failed motors are replaced, feeding the rebuild market. This end of the market has changed, though, according to Frost & Sullivan, as new motor prices fall and labor costs rise. The trend will change again, in the fall, with the activation of the Act which exempts rebuilt motors. The evolution in electrical drives has brought ac motors to the forefront. Through the steady improvement in ac motor development, they are now surpassing dc motors in the high torque and variable speed categories. Throw in lower prices and trends such as ac motors replacing dc motors by 2010 start appearing. In technological trends, the drive technology for switched reluctance has improved enough to bring this nearly antiquated motor type into today's applications. The report predicts sales in switched reluctance drives to skyrocket through the millennium. Brushless permanent magnet servo-type motors for manufacturing and induction motors for mass transit applications have made a stable home in the market due to the heavy trends in automation, electric drives and very high-precision manufacturing. These industrial linear motors are used in the semiconductor and machine tool manufacturing industries to move objects up to five feet per second, while executing the utmost precision. For more information about "U.S. Integral Electrical Motor Markets," contact Frost & Sullivan, 2525 Charleston Rd., Mountain View, CA 94043; (415) 961-9000; fax (415) 961-5042; Internet: http://www.frost.com.-*DS*



Source: Frost & Sullivan

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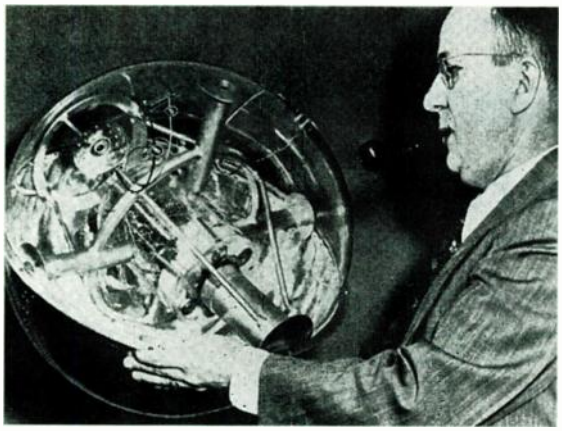
Satellite Computer Center

Project Vanguard recently announced that the Director of Cincinnati Observatory and Professor of Astronomy at the University of Cincinnati, Dr. Herget, has been appointed by the Navy Department to head the staff of the Vanguard Computer Center, Washington, D.C. The Vanguard IBM 704 computing facility will be directly connected by teletype and telephone with the Project Vanguard Communications Center. Following the launching of the satellite, the Computation Center will go into action on a "round-the-clock" basis. Data from a number of radio tracking stations in various parts of the world will be used to calculate the satellite's orbit. Each set of data will consist of two angles defining the direction of the satellite and the times of measurement determined by tracking station observers.



The Vanguard Communications Center also will process information received from unofficial tracking stations and optical observation points throughout the world and will turn data over to the Computation Center. (Project Vanguard Director Dr. John P. Hagen is shown holding a full-scale model of the Vanguard satellite.) *(Electronic Design, February 1, 1957, p. 6)*

Launched in March, 1958, the Vanguard satellite was the fourth in orbit, following Sputnik I, Sputnik II, and Explorer I, which was actually the fourth stage of the Jupiter-C launch rocket. When in orbit, the burned-out solid-fuel stage weighed 30.8 pounds, was 80 in. long, 6 in. in diameter, and carried instruments in its nose cone.

The picture caption says that Dr. Hagen is holding a full-scale model, but the Vanguard satellite launched on March 17, 1958 was much smaller—only 6.4 in. in diameter. It carried no instruments, but had silicon solar cells that powered a transmitter whose signals could be monitored by ground stations to determine the satellite's position in orbit.—SS

New Patents: Phase Meter, Patent No. 2,771, 582. (Inventors, C. N. Winningstad et al., AEC)

This patent relates to a phase meter that may be applicable to either amplitude modulated or frequency modulated phase measurements. Heretofore, the phase meters required the radio frequency source to be a continuous wave and with a stable frequency. This phase meter measures the phase difference of amplitude modulated radio frequencies, continuous wave or pulsed, when the frequency of the source is not stable. This is accomplished by having a frequency determining tank circuit and developing a voltage at a frequency equal to the difference between the input voltage and that of the tank circuit. *(Electronic Design, February 15, 1957, p. 129)*

Patent author C. Norman Winningstad joined Tektronix in 1958 as a sampling and digital oscilloscope designer, and rose from Project Leader to Division Manager. A frequent panelist at ISSCC sessions on high-speed transistors and circuitry, he left Tek in 1970 to get an MBA, and then helped found and took public three companies: Floating Point Systems Inc., Lattice Semiconductor Corp., and ThrustMaster Inc. Norm recalls the phase meter from his days at Lawrence Berkeley Labs as part of the Atomic Energy Commission's effort to use nuclear fusion as an energy source. The meter measured the phase of the control signal required to fire the reactor.—SS

Cable PCS Launched

Changing the face of both cable television and Personal Communication Services (PCS), Cox Communications and Sprint PCS have jointly launched the first cable-television-based PCS. The alliance pairs one of the largest cable television operators with the result of a joint venture between Sprint Corporation, Cox Communications, Comcast Corporation, and TeleCommunications Inc.

Distinguished as one of the three companies given the prestigious Pioneer's Preference licenses from the Federal Communications Commission in 1994, Cox was the only cable television operator to have been awarded the license, based on their work in developing cable-television based PCS service.

Cox's California PCS, responsible for the historic wireless telecommunications move, will be providing Sprint PCS's 100% digital, wireless service to Northwestern Arizona, Southern California, and Southwestern Nevada.

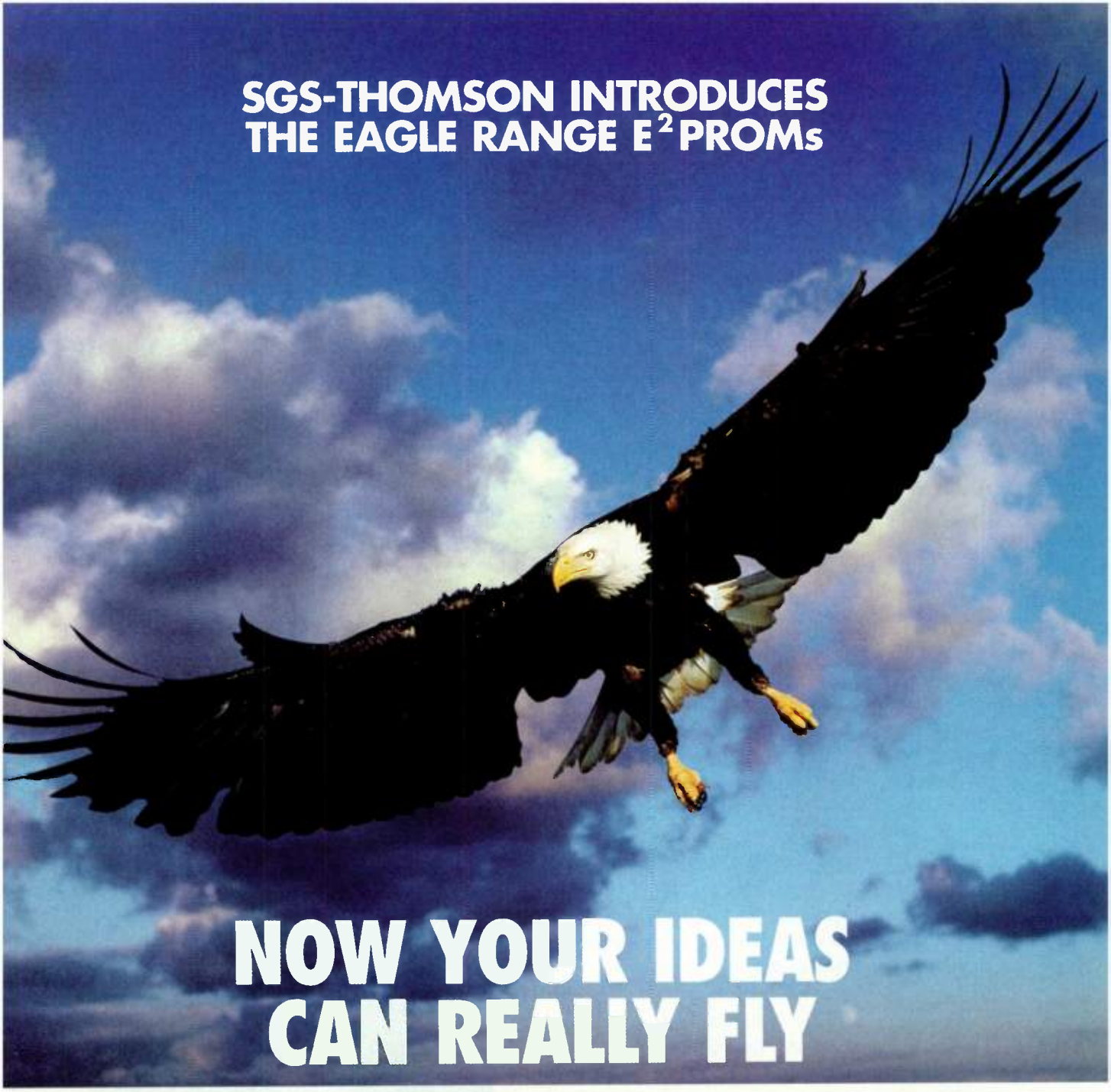
In late December 1996, Sprint PCS kicked off service in Fresno, Calif.; Portland, Ore.; Milwaukee, Wis.; and Spokane, Wash. The company plans to launch service in the following markets during the first six months of 1997: Boston, Dallas/Fort Worth, Denver, Kansas City, Miami, Minneapolis/St. Paul, New York, and Seattle.

Now in development, the Sprint PCS nationwide wireless network is expected to grow to 65 cities nationwide, and plans to expand the network to include 35 of the top 50 U.S. metropolitan areas. The Sprint PCS partnership is licensed to provide service in 33 Major Trading Areas. The projected audience for the service is estimated at 190 million, making Sprint PCS one of the largest wireless communications providers in the U.S.

Sprint PCS uses Code Division Multiple Access (CDMA) technology to deliver the digital service.

For more information, contact Cox Communications, 1400 Lake Hearn Dr., Atlanta, GA 30333; (404) 843-5000; fax (404) 843-5775; Internet: http://www.cox.com.

SGS-THOMSON INTRODUCES THE EAGLE RANGE E²PROMs



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As a world leader in non-volatile memories, SGS-THOMSON has always made it easy for you to take your designs to the top. With the introduction of our Eagle Range of EEPROMs, you have even more to fly with — including the industry's first 256K serial EEPROM. Now you can launch your product with a choice of high performance 256K, 128K, 64K, 32K and 16K devices in both serial and parallel.

And that's just for starters. We support you with a whole spectrum of EEPROMs from 256 bits up. Plus all the best serial bus types including the new SPI standard with clock frequencies to 2MHz.

Count on a million erase/write cycles over the entire operating temperature range — not just room temperature. Get more performance out of less space with ST's own advanced 0.6μ technology. And maximize your design opportunities with a range of operating voltages down to 1.8V.

In other words, don't just get your design off the ground when you can soar with number one. Fax 617-259-9442. Or write SGS-THOMSON, 55 Old Bedford Rd., Lincoln, MA 01773. And visit our web site at **http://www.st.com**

SGS-THOMSON MICROELECTRONICS

Service and Technology

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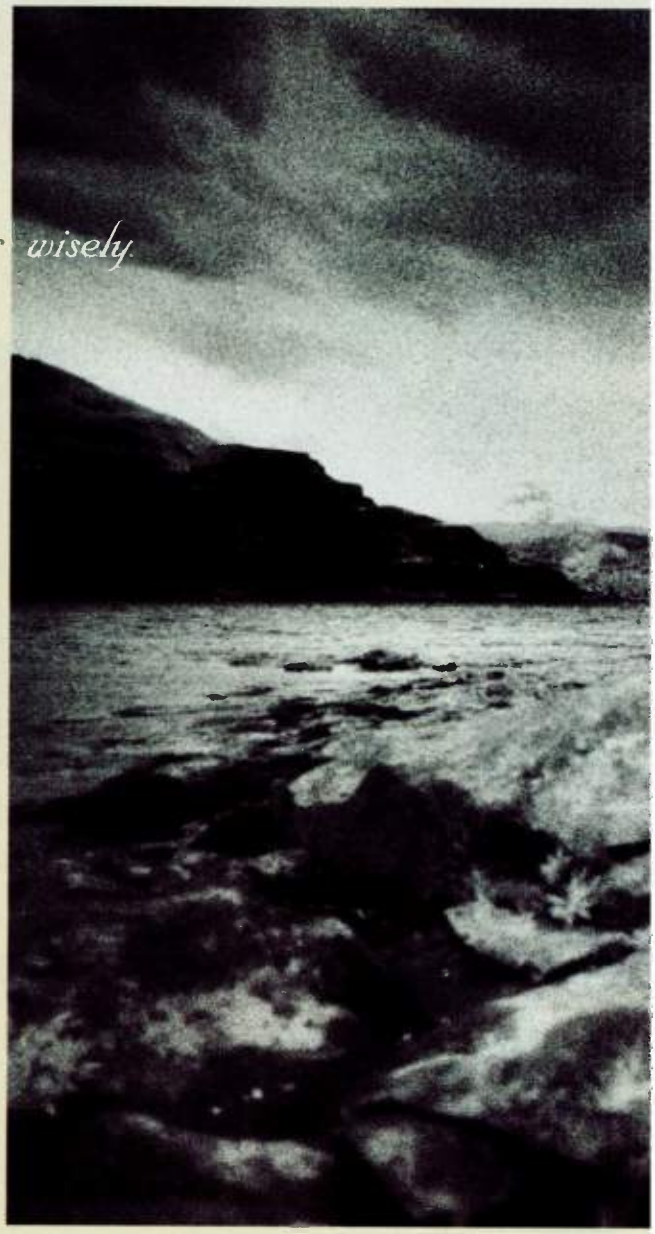
STARING INTO THE FACE

SHOULD MAKE YOU FEEL AS



For an engineer, each project should be a new beginning. A time when you can reach again for something that has never been done before.

Choose your embedded processor wisely.

It will, however, take a particular kind of embedded processor to break the dam—to let the best thinking move from your mind to the application. NEC's 64-bit V_R Series™ is that processor. The remarkable MIPS™ RISC architecture that can release you from what has been and move you to where things could be.

So what, exactly, makes NEC's MIPS RISC architecture the most sensible choice for office automation, consumer and internetworking designs? First and foremost, the price/performance issue. The fact is, no other processors provide better MIPS per dollar than our V_R4300,™ or V_R5000™ processors. And no other processor in its class offers more MIPS per watt than the V_R4100.™

NEC's MIPS RISC architecture also enables forward compatibility. It's extremely scalable and uses common code libraries. In other words, this is an architecture with a sharply defined migration path. Giving you a connection to future processors and backward compatibility to existing code.

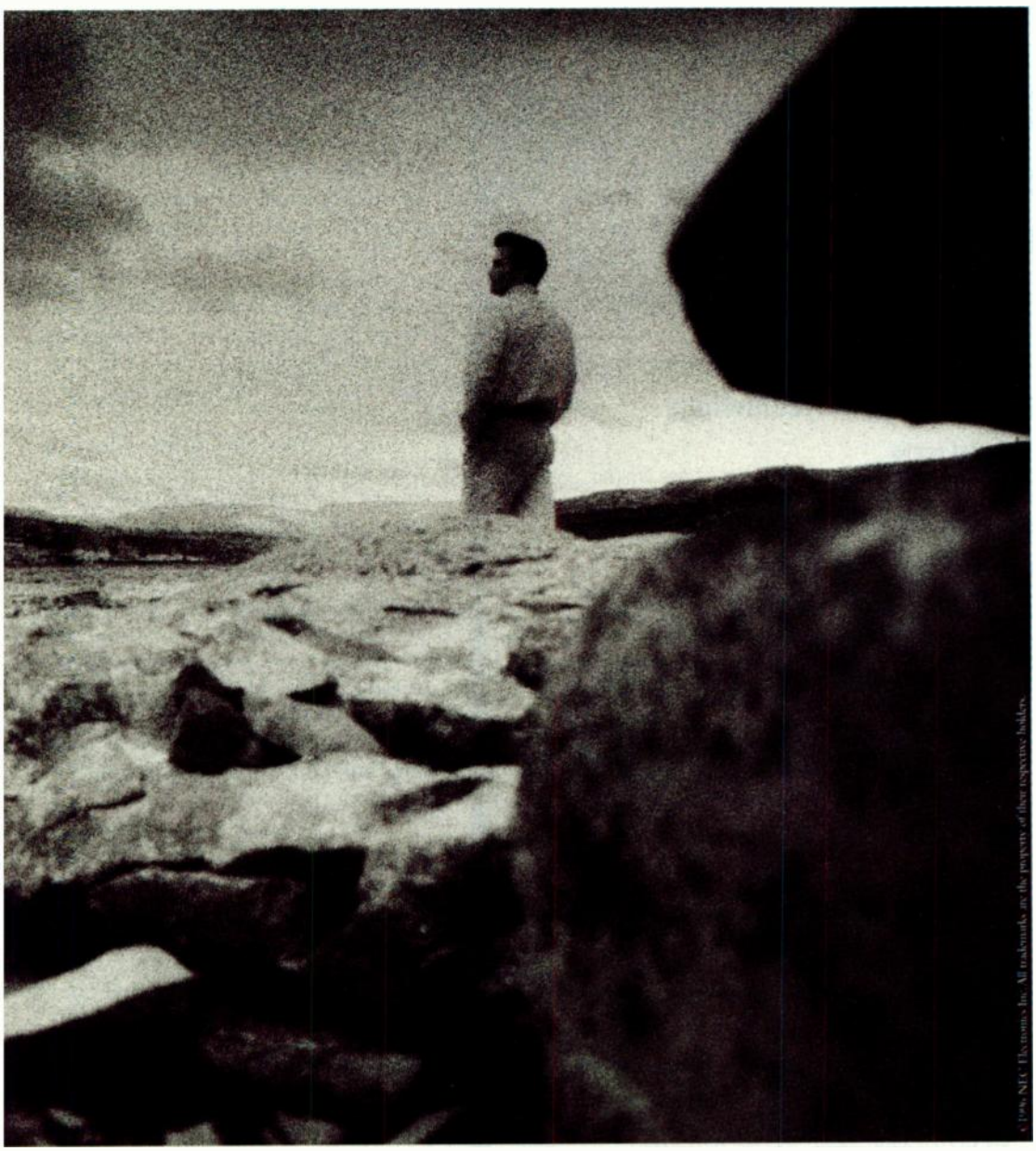
It is an amazing thing to create a successful design. The only problem is, you're being asked to do it faster than ever. Which is why NEC offers a comprehensive solution, including support for PCI Bus interface and laser printer control peripherals. We also provide companion chipsets and third-party tools.

When you think about it, finishing a project in record time is a pretty good thing. Because it means you get to move on to the next one.

Call us for more information about the V_R Series at *1–800–366–9782*. Ask for Info Pack 195.

OF YOUR NEXT *project*

IF ANYTHING IS POSSIBLE.



V_R5000. Paramount performance, incredibly affordable. This is the ultimate embedded processor for advanced applications like internetworking.

V_R4300. A high level of performance at an extremely low price. Ideal for office automation products, video games and X-terminals.

V_R4100. An uncompromising combination of performance and serious power management makes this a perfect choice for personal digital assistants and hand-held terminals.

	V_R4100	PPC403GA	V_R4300	PPC603	V_R5000	PPC604
Frequency	40MHz	25MHz	133MHz	80MHz	200MHz	100MHz
Bus Interface	32-bit	8/32/64-bit	32/64-bit	32/64-bit	64-bit	64-bit
I-Cache Size D-Cache Size	2KB 1KB	2KB 1KB	16KB 8KB	8KB 8KB	32KB 32KB	16KB 16KB
Pin Count/Package	100 PQFP	160 CQFP	120 PQFP	240 CQFP 256 BGA	272 BGA 223 CPGA	304 CQFP 256 BGA
SPECint92/SPECfp92	45 VAX MIPS	---	80/60	75/85	---	128/120
SPECint95/SPECfp95	---	---	---	---	5.5/5.5	---

NEC

READER SERVICE 166

Y2K UPDATE

Here's a quick synopsis of the Year 2000 date change problem (Y2K) for those individuals who've been stuck in an elevator for the last year. Underestimating the length of time that their systems would be in use, programmers used a two-digit year format to represent date fields in applications. These systems, now in legacy status, are predicted when the clock strikes 12 on December 31, 1999.

Computers will read the double zero in the year portion of the date field as 1900, not 2000, since 00 occurs before 99. The number of erroneous results will be astronomical. In fact, there are investment groups that are predicting that banks and other businesses will be experiencing difficulties throughout the next two years, 10 months, and 20 some odd days. People will be billed for overdue books, 100 years overdue. Social security recipients won't be receiving their checks because they won't be eligible for another 65 years. Credit cards will be expiring all over the place.

The bottom line, or rather, the headline is that if this coding issue is not addressed soon, the only businesses that will survive will be the ones that produce Y2K solutions.

Currently, there's quite a market out there for programmers who have a background in code writing and rewriting. The number of companies offering consulting services concerning the millennium mess grows on a monthly basis.

One of the companies offering Y2K solutions is Unicomp. Its subsidiary, Unibol provides GO2000 software, a solution featuring Impact Analysis. Impact Analysis gives the decision makers the facts about how badly the Y2K problem will hit the company. GO2000 looks at whether or not the company is actually affected by the problem, the size of the impact, where the business will be hit by the date change, when the systems will start to fail, and options for resolving the issues.

Unibol's GO2000 consulting services are offered to IBM System/36 installations, as well as IBM AS/400 installations. Big Blue estimates 103,500 System/36 and 350,000 AS/400 installations. Currently, Unibol provides the only product that features a rehosting path to Windows NT and Unix for RPG and COBOL applications for the two IBM systems. This situation has allowed for the implementation of GO2000 into a large customer base. In anticipation of increased demand, Unibol's parent is currently increasing its sales staff and field technicians.

For more information, contact Unibol Inc., 1800 Sandy Plains Pkwy., Suite 320, Marietta, GA 30066; (770) 218-7401; fax (770) 424-9123; Internet: http://www.unibol.com.—*DS*

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Most people know that a pacifier will stop noise, sometimes very quickly, other times it takes a little longer. The method, however, works. Add a little sweetness and it works even faster. And for certain applications the pacifiers come in different shapes and sizes.

Conec Filter Connectors stop noise as well. Noise created by EMI/RFI in today's high speed digital systems. And just like pacifiers, Conec Filter Connectors come in different configurations - industry standard d-sub, high density d-sub, filltered adapters, modular jacks and combo d-sub, with power filtering and signal filtering. We don't add any sweeteners. What we do add is our patented planar filters. The technology with a proven track record, combined with the industry's best connectors—ours. Both technologies fully integrated, for best results in filtering.

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OFF THE SHELF

"The Visual J++ Handbook" shows readers techniques on how to spice up web pages with animation, sound, and interactivity, and how to add Microsoft Java extensions to incorporate ActiveX controls and other COM objects into Java applets. The book explains the writing, compiling, and running of working Java applets with Visual J++, and also delves into web page design techniques, HTML coding, and running Java applets in web browsers. The 464-page book is priced at $29.99. For more information, contact Osborne/McGraw Hill, 2600 Tenth St., Berkeley, CA 94710; (510) 549-6600; fax (510) 549-6603; Internet: http://www.osborne.com.

"A Simplified Approach to Image Processing" covers topics such as color issues, warping, and Fourier transforms. If readers are familiar with C, the book will help to understand its real-world examples. Topics include fundamental techniques for scaling, rotation, and mirroring; digital morphing, and filtering algorithms. Contact Prentice Hall Inc., One Lake St., Upper Saddle River, NJ 07458.

KMET'S KORNER

...Perspective on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
P. O. Box 1070, 100 Prickly Pear Rd., Verdi, NV 89439; (702) 345-1455; fax (702) 345-0804

RON KMETOVICZ
CONTRIBUTING EDITOR

I teach a class each year at Santa Clara University—R&D Management 264 for those thinking of participating. The course attracts Silicon Valley engineers who aspire to be R&D managers, vice-presidents of engineering, directors of engineering, and others who run their own technology-based company. At present, class participants work in engineering, marketing, and manufacturing at Siemens, Hewlett-Packard, Cisco Systems, LSI Logic, Adaptec, Advanced Micro Devices, Sun, Intel, and other Valley companies.

To complete a particular class assignment, students returned to their respective companies to determine the cost of a new product development person-month. Some got the figure by doing a detailed bottoms-up analysis, while others simply determined the total monthly R&D budget and divided it by the number of engineers working in new product development. R&D costs include the summation of payroll and related expenses, operating expenses, and occupancy expenses. Payroll and related expenses segment into salaries, payroll taxes, insurance, education reimbursement, recruiting, and other miscellaneous charges. Operating expenses include travel, supplies, equipment, licenses, contracted services, equipment, prototype, and other costs. Occupancy contains charges associated with rent, utilities, and related items. To arrive at the cost of a person-month, students sum the above items and divide by the number of engineers represented within the figures. This year, the figure grew substantially over last year.

A simple ratio, monthly engineering expenses divided by engineering head count, produces the person-month figure. To create an increase, grow expenses, decrease head count, or both. So which of the three modes dominates?

The escalation appears to be driven by supply and demand—engineering talent is now in short supply. Expenses are rising at a greater rate than head-count growth. Boom times have returned, companies pay their engineers more as they try to elevate staff levels in a competitive environment. There is more work to be done then engineers to do it! Business growth dominates discussion, it's taking longer to get products to market because of staffing constraints. Activity to attract engineers shows itself in the paper, over electronic media, and in one-on-one interaction. The heat is on! My students report working from 10 to 12 hours a day on the job and then work at home at night and on weekends. Many perform from 60 to 70 hours a week and do so as part of a team working similar hours. Under such conditions, the fun of a great job tends to disappear—it becomes hard work. The employer becomes the true beneficiary, getting one to two engineers for free for each three working.

Employers have learned from the downsizing experience of past years, control of expense growth remains a serious issue. With pay levels rising, operating expenses and occupancy growth are held to a minimum.

From a time-to-market perspective, the actions being taken are shortsighted. Forced burn-out leads to business stagnation and failure.

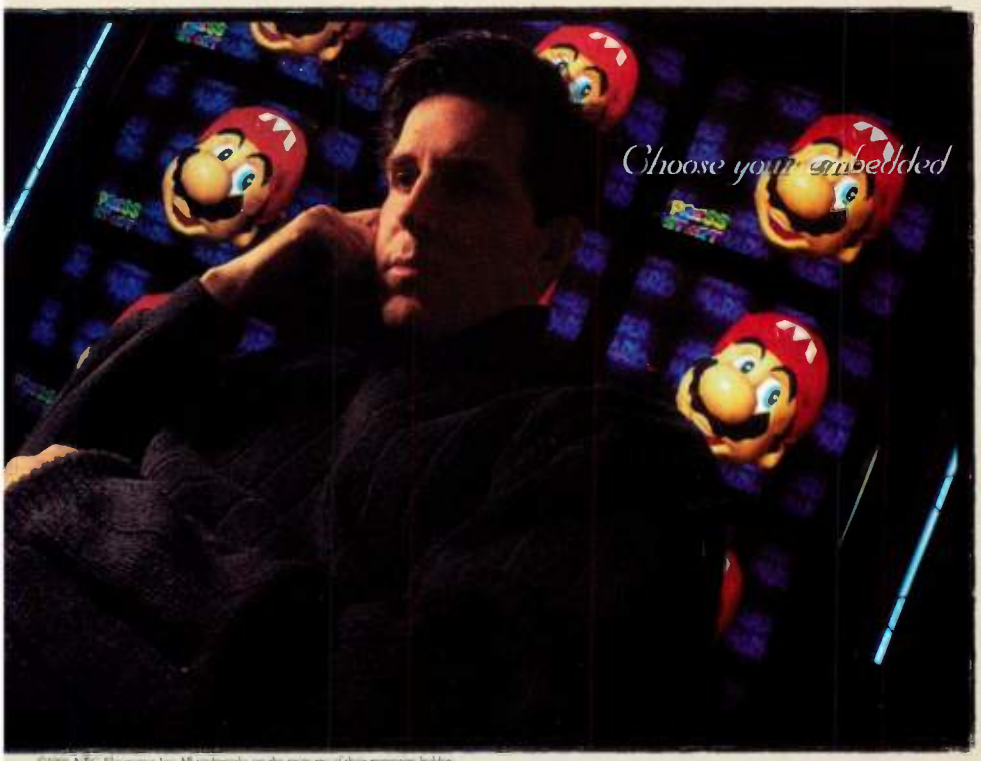
Responsible managers: Get feedback from engineers working 60- and 70-hour weeks and take action to stop it! You'll improve the work environment, enrich the lives of your engineers, add creativity and spark to new products, and make more money.

To obtain an e-mailed copy of "The Complete List of Reasons for Late Product Innovation," contact Mr. Kmetovicz at kmetovicz@aol.com.

"I'VE HEARD IT SAID THAT YOU CAN NEVER GIVE A GAME DEVELOPER ENOUGH RESOURCES.

WELL, THIS IS ONE OF THOSE TIMES WHEN WE EXCEEDED THEIR *wildest* EXPECTATIONS."

DARREN SMITH. *Project Manager,* NINTENDO 64



"Getting a machine like the Nintendo 64™ to market was an amazing experience. For three years, I coordinated efforts between Nintendo, MIPS™ and the folks at NEC.

During that time, we looked at several versions of MIPS RISC processors. However, NEC's V_R Series™ processor shot to the top. Without question, it provided the most power for the price.

One great thing about the V_R Series processor is what it enables. You see, game developers no longer have to hold back. It's now possible to create fantastic revolutionary games at an unbelievably low cost. With power to spare for things like on-the-fly image decompression, and even things they've only dreamed about doing.

For the first time, developers can truly simulate reality. If they want something to happen, it will happen. Take, for example, WaveRace64.™ The NEC V_R Series allows for such incredibly smooth and realistic dynamics when riding on water, that you'd be well advised not to play if you get seasick.

Frankly, it's exactly what you'd expect from a Nintendo/NEC partnership. I just can't stress enough what a phenomenal job NEC does of keeping an eye on your bottom line. NEC clearly understands that every penny counts. In fact, they were able to reduce the number of pins. And in case you didn't know, every pin is another million dollars in our business.

But it also means a lot to the kids. You see, the V_R Series processor is an evergreen design. So it won't be obsolete in two or three years. And that means Nintendo 64 devotees can put their allowances towards other things. Like buying books or planting trees. And hey, maybe they'll even buy a few more games."

For more information about NEC's V_R Series call *1-800-366-9782.* Ask for Info Pack #195.

"NEC's V_R Series processor has helped make the Nintendo 64 the most significant consumer electronics product since the VCR."

NEC

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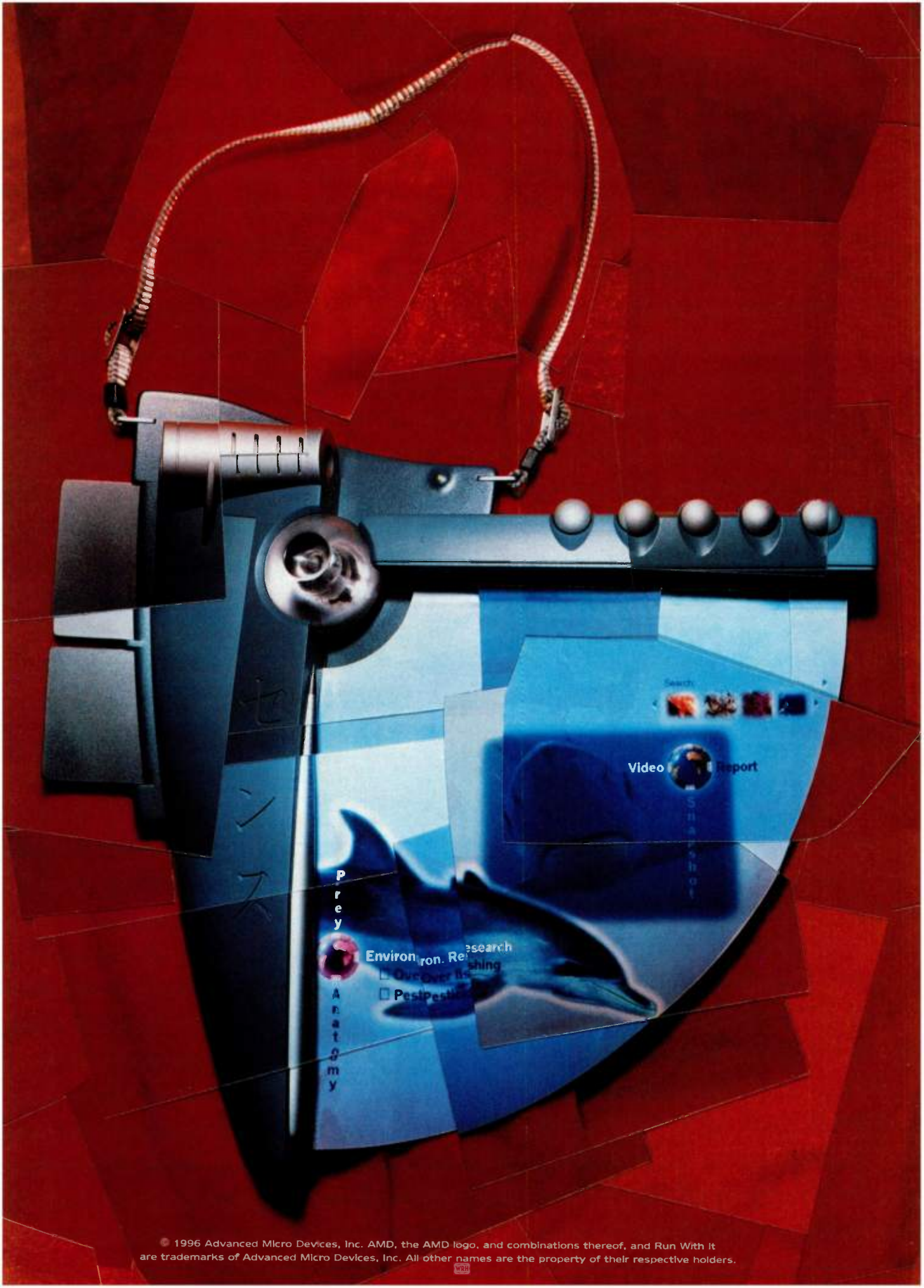

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The Sensu PDA from Design Edge features a collapsible thin-film color display, audio and video compression, a wireless modem, and CCD camera. It's not available today, but AMD's 2.7 volt-only Flash technology is.

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Segyehwa, the policy of total globalization declared by Korea's president Kim Young-Sam, consists of eliminating trade barriers, emphasizing cross-cultural understanding, and liberalizing markets. The new open economy that Korea is trying to achieve was born out of radical market reform and a sincere desire to integrate into the global marketplace.

Currently, the country is running at a trade deficit, exporting $125 billion worth of goods, but importing $135 billion in 1995.

According to the Korea International Trade Association, the country is the largest producer of DRAM computer chips in the world. Big name manufacturers out of Korea include Samsung, Hyundai, and LG Semicon. Exports of semiconductors produced in Korea totalled $22 billion in 1995. Samsung also is the world's largest producer of color-picture tubes. Korea produces the majority of the world's VCRs, and also exports the most microwave ovens.

The electrical parts and components manufacturers are represented by mostly small companies with 60 employees or less. Despite the fact that the large companies produce most of the parts and components, 93% of the market is comprised of companies with 300 or fewer employees.

Keeping pace with the rest of the global market, Korea's telecommunications industry is experiencing a period of exploding growth. When Korea Mobile Telecom became the first company in the world to introduce wireless communications networks with CDMA technology, in 1996, the government began speeding up its phasing out of restrictions on the market. The government has set aside $1 billion to design a new fully-digital intranet, connecting all government agencies, research centers, and universities by the year 2010.

For more information, contact the Korea International Trade Association at their New York office, 460 Park Ave., Room 600, New York, NY 10022; (212) 421-8804; fax (212) 223-3827; Internet: http://www.accesskorea.com.—*DS*

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ISC	Molded, shielded, wirewound technology, moisture resistant, excellent size-to-inductance-range ratio.	1210: .01µH-100µH 1812: .01µH-1000µH	Call 800-487-9437 Document #305
ILB	Multi-layer shield beads, ideal for EMI and RFI suppression. 1206 and 0805 sizes. (0805 Preliminary)	Impedance values range from 19Ω to 600Ω	Call 800-487-9437 Document #314
ILS	Multi-layer, shielded inductor. 1206 and 0805 sizes. (0805 Preliminary)	1206: .047µH-33µH 0805: .047µH-33µH	Contact Factory
TJ	High current, vertical mount reduces PC board size, toroid design decreases EMI, 7 sizes. Current ratings up to 20 Amps.	1.2µH-5600µH	Call 800-487-9437 Document #309
LPC	Low profile pot core, efficient voltage regulation in low current applications. High Q (up to 60). Low DCR.	47µH-6800µH	Call 800-487-9437 Document #304
TA	Audio, telephone coupling style designed to meet FCC Part 68. Frequency range: Data/voice = 300 to 3500Hz. Data = 800 to 3500Hz. 26 models.	———	Call 800-487-9437 Document #311
LPT	Low profile surface mount, toroidal core, 2 separate windings, 4 terminals, 4545: .450" diameter. 3535: .350" diameter.	10µH-1200µH	Call 800-487-9437 Document #301
IM	Standard and "R" level E-Rel models. Axial leads, flameproof molded epoxy coating.	Standard: .10µH-10,000µH ER: .10µH-33µH	Call 800-487-9437 Document #308
IMS	Standard and "R" level E-Rel models. Axial leads, shielded, molded epoxy encapsulation, flameproof, moisture proof.	Standard: .10µH-100,000µH ER: .1µH-12µH	Call 800-487-9437 Document #307
IHD	High current, axial leads, polyolefin sleeve. Current ratings up to 5 Amps.	IHD-1: 1.0µH-18,000µH IHD-3: 3.9µH-100,000µH	Call 800-487-9437 Document #312
IHA	High current, axial leads, polyolefin sleeve, flame-retardant. Current ratings up to 9 Amps.	50µH-1000µH	Call 800-487-9437 Document #313
LPE	High current, surface mount, gapped and ungapped, ferrite core, 5 package sizes, solvent resistant. Above board heights: .205" [5.20] to .335" [8.50]. Transformers and inductors.	10µH-330,000µH Custom transformers available	Call 800-487-9437 Document #302
IHSM	High current, surface mount, flame-retardant encapsulated body.	1µH-18,000µH	Call 800-487-9437 Document #303

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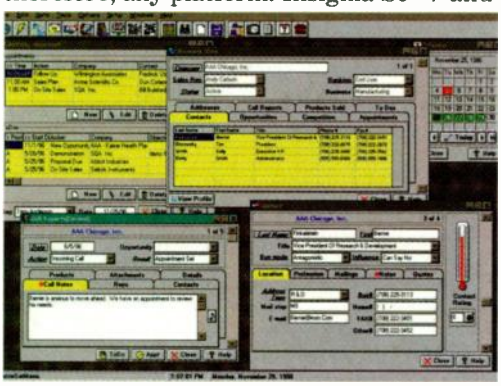
WRH

Power Sales

Allowing customers to use their Internet and intranet connections to the greatest extent, Insignia Solutions and Market Power have teamed to bring Market Power's Visual MATRIX to the World Wide Web (WWW) through Insignia's NTRIGUE solution. NTRIGUE is a Windows NT application server solution that will provide cross-platform access so that Visual MATRIX can run on WWW, and therefore, any platform. Insignia Solutions may be reached at their web site: http://www.insignia.com.



Another alliance recently built by Market Power is one made with Cognos. The company had been chosen as a Cognos Business Intelligence Partner, and is now a certified reseller of PowerPlay and Impromptu. The two software solutions are designed to satisfy enterprise-wide data access and reporting needs. PowerPlay and Impromptu support over 100 relational and OLAP data sources.

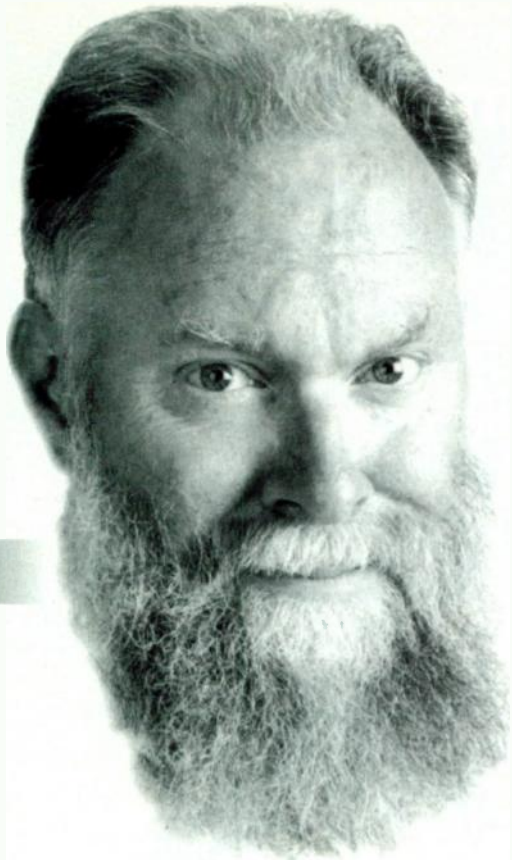
Targeted toward decision makers and sales representatives, Market Power's Visual MATRIX version 2.5 is designed to help businesses with unique sales force automation requirements. The new version of the comprehensive sales automation system offers new features such as Goal Management, Importer/Exporter Support for Mailhouses, and Multi-Centric Database Management.

The Goal Management system provides the user with an easy-to-use goal tracking system that allows sales reps to set up activity and monetary goals. Tracking different individual income sources and project earnings, dollar goals are displayed in the matrices. Activity goals organize and track such items as cold calls, relationship building calls, and written proposals.

The Importer/Exporter Support for Mailhouses lets users create mailing lists featuring their own criteria. The list can then be forwarded electronically to the company's direct mail house.

The Multi-Centric Database Management system provides a way for businesses to hierarchically organize their prospect information. This advantage allows companies to design the structure of their database according to their individual style of selling.

For more information, contact Market Power Inc., 101 Providence Mine Rd., #104, Nevada City, CA 95959; (916) 265-5000; fax (916) 265-5171; Internet: http://www.MPInet.com



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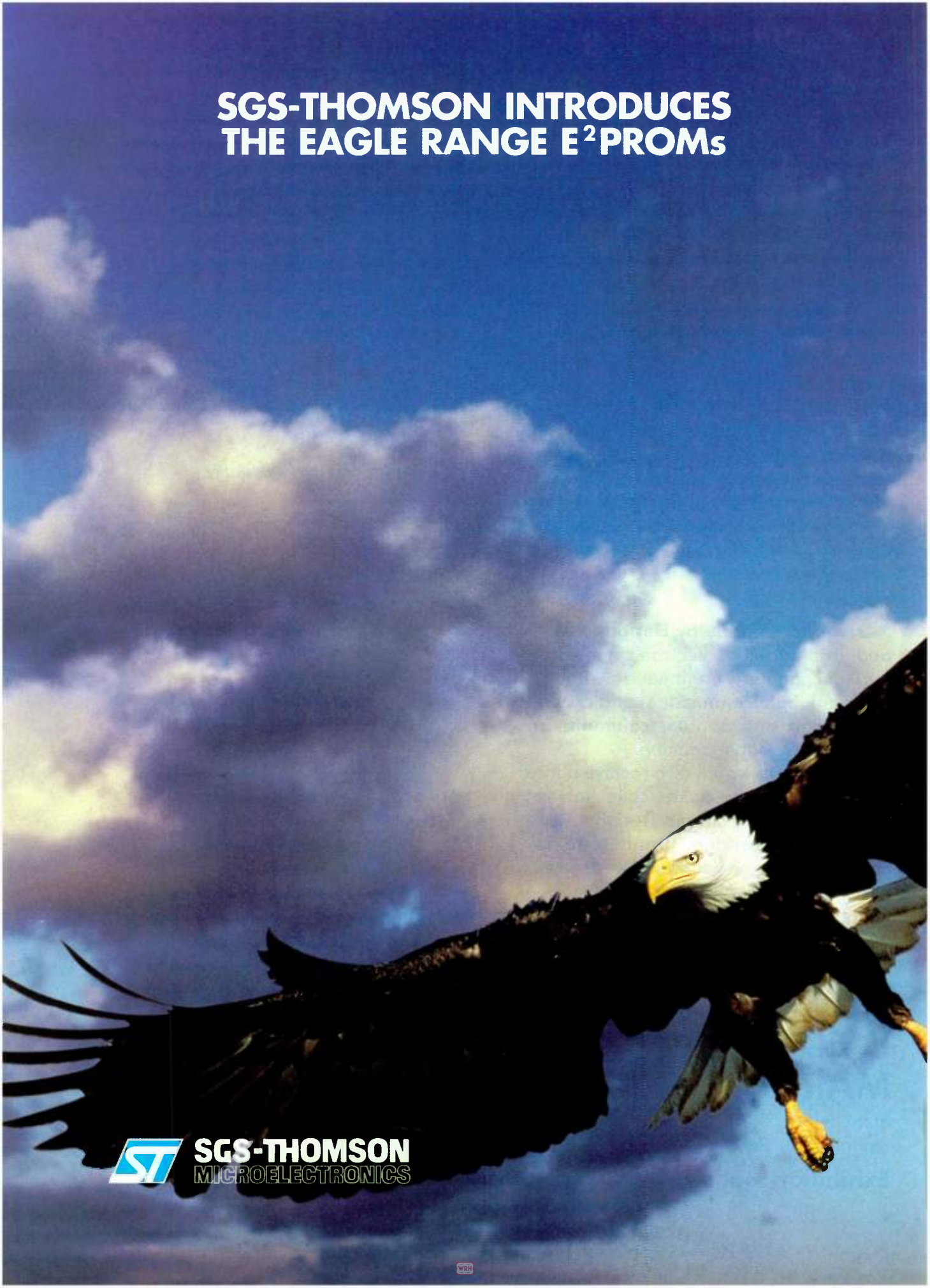
SGS-THOMSON INTRODUCES THE EAGLE RANGE E^2PROMs



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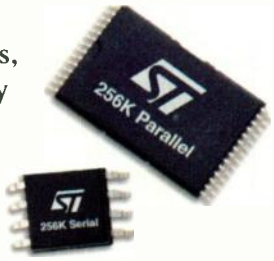
NOW YOUR IDEAS CAN REALLY FLY

As a world leader in non-volatile memories, SGS-THOMSON has always made it easy for you to take your designs to the top. With the introduction of our Eagle Range of EEPROMs, you have even more to fly with — including the industry's first 256K serial EEPROM. Now you can launch your product with a choice of high performance 256K, 128K, 64K, 32K and 16K devices in both serial and parallel.



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QUICKNEWS

TAKING A SWIPE AT THE COMPETITION—Mag-Tek, a long-time member of the magnetic-stripe technology community, now is offering its three-track RS-232 Card Reader. The new release is in response to the nationwide trend of states enhancing their driver's licenses with magnetic stripes. The stripes are imbued with information such as license number; the driver's address, age, and sex; and other data supplied by the Division of Motor Vehicles. The RS-232 is capable of reading all ISO-standard magnetic cards and the new licenses. The reader has a long-wearing head that can read up to one million cards. After checking the encoded stripe for errors using parity and LRC, the swipe reader sends serial data to the host using asynchronous stop/start ASCII format. The RS-232 is small enough to be attached to most keyboards. Switch block settings in the unit control baud rate, communication parameters, mode of operation (buffered or unbuffered), and user protocol.

For more information, contact Mag-Tek Inc., 20725 South Annalee Ave., Carson, CA 90746; (800) 788-6835; fax (310) 631-3956; Internet: http://www.magtek.com/.

INTRANETTING @HOME—The WebVisa Router from Accton Technology is a low-cost LAN/WAN routing solution designed to suit small businesses, branch offices, or home offices. The WebVisa supports Frame Relay, asynchronous and synchronous ports for dial-up links or leased lines, and standard IP-based internetworking. In accessing the Internet, the router has been designed to work with standard routers used by Internet Service Providers (ISPs). WebVisa also can maintain direct links with the ISPs. Supporting transmission speeds from T1 (1.544 Mbytes/s), E1 (2.048 Mbytes/s) or 64 Kbytes/s, the router uses RS232, V.35, and X.21 interfaces. Additionally, the WebVisa automatically adjusts itself to the maximum transmission rate available. The RS232 asynchronous port is programmable to up to 115.2 Kbytes/s. Dial-on-demand is available with WebVisa, allowing the user to store up to 32 dial-circuits in memory. As far as security is concerned, Password Authentication Protocol and Challenge Handshake Authentication Protocol are both supported by Accton's router. Designed to accommodate the busy home office, the WebVisa has been outfitted with a graphical setup utility. Users are prompted by requests for password assignments, Internet addresses, and subnet masks. The process is designed to connect the user in less than five minutes.

For more information, contact Accton Technology Corp., 1962 Zanker Rd., San Jose, CA 95112; (408) 452-8900; fax (408) 452-8988.

SEEQ AND YE SHALL FIND—New from SEEQ Technology is the 84C24 Quad 10Base-T Ethernet Media Interface Adapter for twisted pair networks. Designed to increase component density through integrating adaptive equalization and transmit filters, the single-chip unit is comprised of four complete 10Base-T physical layer interfaces that have been combined with IEEE full/half-duplex auto-negotiation onto one 68 lead PLCC surface mount package. SEEQ's adapter features easy-to-use installation. The 84C24 is capable of sensing wiring polarity and adjusting automatically to the correct orientation. The unit also can choose the highest-performance operating mode available by using the auto-negotiation algorithm. The unit is priced at $20 a piece in 10,000 unit quantities.

For more information, contact SEEQ Technology Inc., 47200 Bayside Pkwy., Fremont, CA 94538; (510) 226-7400; fax (510) 657-2837; Internet: http://www.seeq.com.

STEP TO THIS—Consummating the alliance between Ultratech Stepper and ASM Lithography, Ultratech is offering the 2244i stepper for the pair's mix-and-match microprocessor manufacturing solution. The joint venture includes engineering, executive management groups, marketing, and sales from both companies. Ultratech supplies photolithography systems used in the manufacturing processes of semiconductors and thin film heads for disk drives. As part of the agreement, ASM has given Ultratech extensive data concerning lens distortion matching, mutual optimization of stepper management, and overlay registration.

For more information, contact Ultratech Stepper Inc., 3050 Zanker Rd., San Jose, CA 95134; (408) 321-8835; fax (408) 577-3376.

UNIVERSE COMPATIBLE WITH WINDOWS NT AND UNIX—VMARK Software has developed an updated version of its UniVerse relational database management system (RDBMS) that is fully compatible with both Windows NT and UNIX systems. UniVerse 9 supports all existing versions of the operating systems, including all administrative tools, development interfaces, internetworking products, and ODBC connectivity. The RDBMS features stored procedures, allowing the engineer to write complex, server-side procedures in standard programming languages. UniVerse 9 also includes an intrinsic, programmable SQL gateway that supports any standard ODBC driver. The gateway allows data to be integrated with the RDBMS from anywhere in the system, whether from a mobile source or at the office in a mainframe. Administration of remote UniVerse servers can now be managed through the use of a Windows-based interface. Upgrading UniVerse to handle information that's been downloaded from the Internet, VMARK also has included the UV/Web toolkit. UV/Web allows the user to build web pages that contain UniVerse 9 relational databases. The stored procedures provide the necessary tools to create unique HTML documents. Another feature found in UniVerse 9 is the Bulk Data Loader. The Bulk Data Loader can combine multiple input files into a single table and multiple columns from different files into one solitary column.

For more information, contact VMARK Software Inc., 50 Washington St., Westboro, MA 01581; (508) 366-3888; fax (508) 366-3669; e-mail: psuita@vmark.com.

Lapping Up Remote Access

Keeping with the trend of installing off-line Internet software into new PC notebooks, Fujitsu PC Corp. recently announced that the company will be including LapLink for Windows 95 and WebEx from Traveling Software in its newest line of notebooks.

The profile of the typical notebook user is an individual who is highly mobile and uses the Internet to find the most up-to-date information. WebEx allows Windows 95 users to schedule the downloading of information to get the most out of their connection while they're on the road away from it.

Traveling Software also recently teamed with NETCOM On-Line Communication Service, an Internet service provider. The alliance brought a customized version of WebEx to NETCOMplete, an Internet service solution targeted at business professionals.

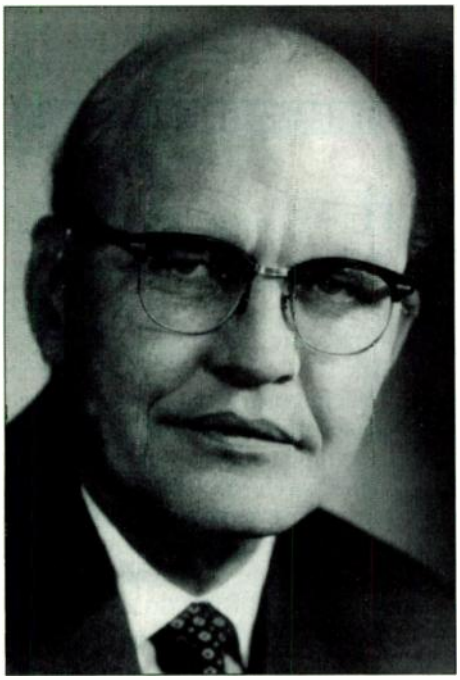
LapLink v. 7.5 now employs Xchange Agent technology to speed up file transfers and improve remote control. Putting more power into the hands (or mouse) of its users, Xchange Agent provides an easy-to-use wizard setup to synchronize folders automatically.

File transfer speeds also have been improved in the new 32-bit version by 30%. LapLink's adaptive compression technology automatically adjusts to the user's connection speed, maximizing compression. The data encryption feature ensures save data transfer during remote control. LapLink's patented SpeedSync technology is a file transfer recovery system that sends only the missing data of the file, not the full file, if a modem session accidentally cuts off during a download or upload. This addition can save 80% or more of long distance charges.

LapLink 7.5 also has an AutoConnect function that uses new shortcuts to connect users to other LapLink-equipped computers, matching screen resolutions and allowing chat sessions by clicking on an icon. Users can further speed up their transfer times by specifying the number of transmitted colors or cut the colors to black and white.

Priced at $149, the LapLink v. 7.5 for Windows 95 package includes the 32-bit software, documentation, LapLink for Windows 3.1, and a parallel cable. An English-language version is available free of charge at Traveling Software's home page (listed below). French, German-, Italian-, and Spanish-language versions also are available through the company's international distributors. Customers with LapLink's 7.0 version also can upgrade their software for $29.95 by calling Traveling Software directly.

For more information on LapLink, contact Traveling Software Inc., 18702 North Creek Pkwy., Bothell, WA 98011; (800) 343-8080; (206) 487-1284; Internet: http://www.travsoft.com.—*DS*



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Revered by engineers worldwide as the inventor of the IC and a pioneer of solid state technology, Jack Kilby will once again make an appearance at the Portable By Design Conference & Exhibition. Two years ago, Mr. Kilby was the keynote speaker—this year, he will present the first annual "Electronic Design Award For Technical Innovation." The award will be presented the author of 1997's most innovative conference technical paper. The award represents the first of its kind given annually. The ceremony will take place at the Industry Reception, held on the show floor at the Santa Clara Convention Center in Santa Clara, Calif., on Tuesday, March 25, 1997 at 5:00 p.m.

Also at this year's gathering. . .

KEYNOTE SPEAKERS:

TOM BEAVER
Vice President
Worldwide Marketing
Motorola, Inc.

PHILIP WENNBLOM
Director, Strategic Planning
Mobile and Handheld Products Group
Intel Corporation

ROBIN SAXBY
President & CEO
Advanced RISC Machines
(ARM)

VAUGHN WATTS
Director of
Mobile Computing Architecture
Texas Instruments

and a presentation from **BOB PEASE**, author of "PEASE PORRIDGE"

Exhibitor Information: Contact **Lisa Zurick**, Director of Show Sales, at 847/263-6837; fax 847/263-6854
Conference Information: Contact **Rich Nass**, Program Chairman, at 201/393-6090; fax 201/393-6073; or call **Betsy Tapp**, Exhibition Manager, at 201/393-6075; fax 201/393-6073

TRUDEL TO FORM

JOHN D. TRUDEL
CONTRIBUTING EDITOR

How can organizations effectively renew themselves to deliver better results? My last column discussed how Machine Age business was about repetition and refinement, but Information Age success demands more.

Revolutionary change is needed. Behavioral change, whether for an individual or a corporation, is usually difficult. Before people can change habits, they must sort through options and consequences. Unless convinced that their own well-being is at stake, they won't change.

Right or wrong, Wall Street measures corporate well-being by profits. Companies have several options for delivering profits. A decade ago, the preferred strategy was value creation.

Value creation is still the way for some, but most large firms have given up. For years, there has been little, if any, value growth for the Fortune 1000.

Counterexamples and exceptions are easily dismissed. Managers and business-school professors know that a few U.S. firms like Intel and Microsoft are doing well. They dismiss them as special, unique, abnormal cases. They know the Japanese do well at products and market share. They dismiss that too, because Japanese firms don't worry about, and don't deliver, high profits.

Limits are first set in our own minds. As managers realized that most large firms were unable to add value, they became fearful. They came to assume there must be some natural force at work. In the early days, words like "even IBM is having layoffs" helped make downsizing socially acceptable.

Managers think, "If even an IBM or an Apple can't add value to deliver profits, neither can I." Instead, they try other methods. Driven by performance pressures but lacking strategic vision, many companies in various industries have had no better idea for profit generation than to cut costs, fire workers, and buy up rivals.

Past columns have discussed the results. The statistics show a clear pattern. Cost cutting boosts profits only in a minority of cases, and not on a sustained basis. It creates lasting damage to innovation.

For the past year, I have been conducting surveys on business innovation. Few firms are consistently doing well at value creation. Michael Porter discusses why in the November-December 1996 *Harvard Business Review.*

The Japanese took the lead from America with better process: TQM, benchmarking, continual improvement, etc. Rivals were so poor at cost, quality, and cycle time that firms could seize markets just by building the same products better.

Cost cutting and copying have, therefore, become habits. Since most products are generic, even high tech firms are now selecting their CEOs from commodity industries.

As Porter notes, "A company can outperform rivals only if it can establish a difference that it can preserve." Improving cost and operational efficiency moves the bar up, but rarely leads to sustainable competitive advantage.

The problem is insidious—competitive convergence. "The more benchmarking companies do, the more they look alike. The more that rivals outsource activities to efficient third parties, often the same ones, the more generic these activities become."

Global competition quickly compresses margins on anything that is standard and routine. Today's competitors are quick, and information travels at electronic speed. Unless you use slave labor or enjoy a monopoly (which some do), it is difficult to sustain profits with generic, commodity products.

John Trudel, CMC, provides business development consulting and is the author of "High Tech with Low Risk." He is founder and director of The Trudel Group, 33470 Chinook Pl., Scappoose, OR 97056; (503) 640-5599; fax (503) 543-6361; e-mail: johntrudel@aol.com; Internet: http://members.aol.com/johntrudel.

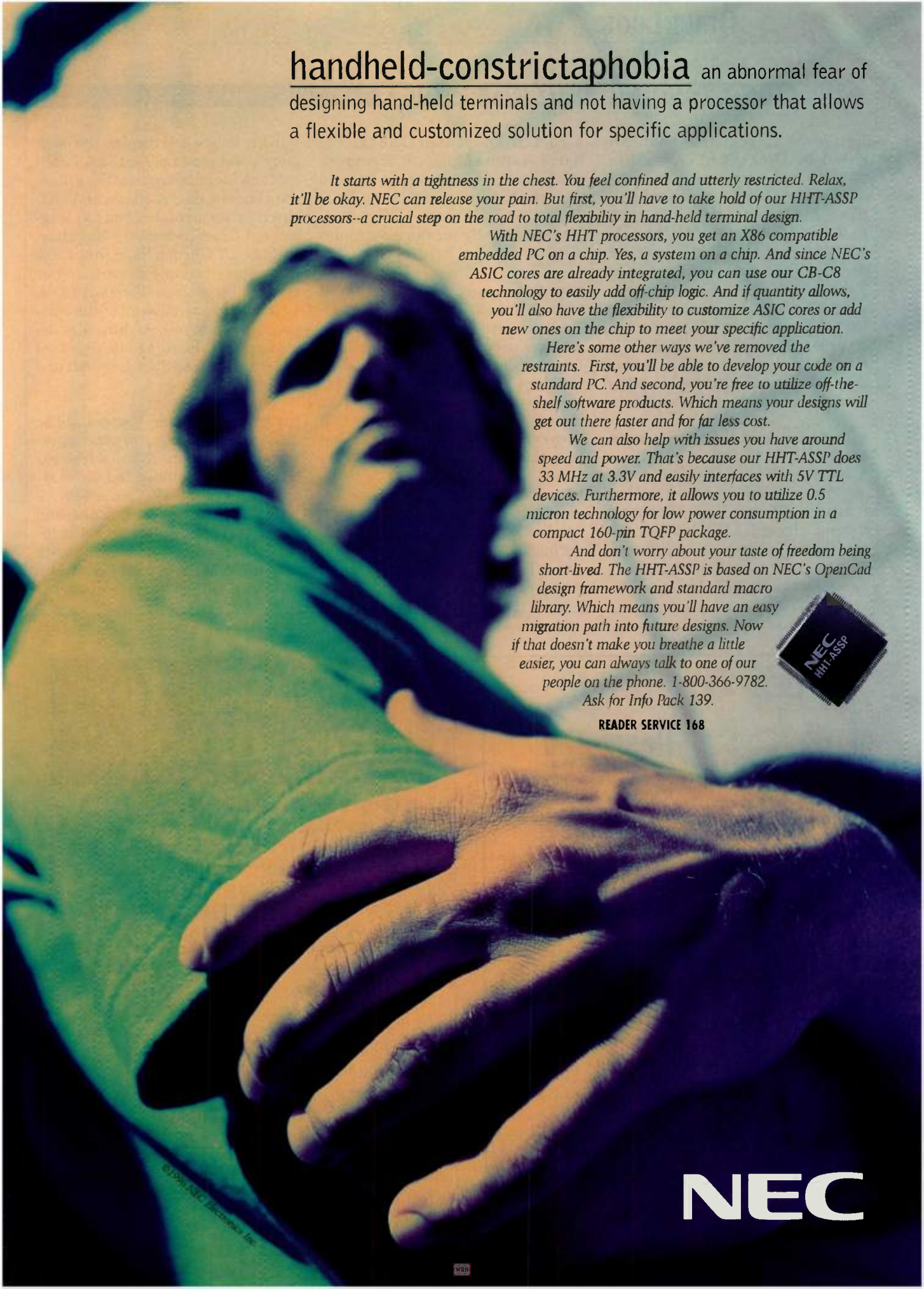
FREE STUFF

Hewlett-Packard's (HP) HP VXI Test Systems Components CD is available free of charge by ordering from the company's Test and Measurement Organization's web site at http://www.tmo.hp.com/tmo/catalogs. The CD provides fast solutions for configuring, selecting, and purchasing test-system and VXI-family components, systems, and services such as test software, controllers, and interfaces. System requirements are Windows 3.1, a 486 processor, 12 Mbytes of RAM, and a 2X CD-ROM drive. Contact Hewlett-Packard, Test and Measurement Organization, P.O. Box 50637, Palo Alto, CA, 94303-9512.

National Instruments' new version of its DAQ Designer software configuration utility for Windows is available free of charge. The interactive package asks system developers questions about application requirements such as the quantity and types of signals and sensors, and signal conditioning needs. It analyzes answers, produces a summary report, and recommends appropriate solutions. Contact National Instruments, 6504 Bridge Point Pkwy., Austin, TX 78730-5039; (512) 794-0100; fax (512) 794-8411; Internet: http://www.natinst.com.

FAN MAIL

One of our New Year's Resolutions is to print letters sent to this section. If there is a topic you'd like to see covered in QuickLook, a viewpoint on something you have seen here, or even some praise (our moms' would be proud) about a piece we've printed, please send it in. We welcome all correspondence. You can e-mail Mike Sciannamea at **mikemea@class.org** or Deb Schiff at **debras@csnet.net.** If you prefer to use regular mail, send your comments to The Copy Desk, *Electronic Design*, 611 Rte. 46 W., Hasbrouck Heights, NJ 07604. Our fax number is (201) 393-0204.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For more information, contact PTM, 119 Benton Oaks Dr., Sauk Rapids, MN 56379; (320) 253-0591; e-mail: cybercir@aol.com.

P KZIP 2.50 has recently been released from PKWARE. The storage standard now supports the 32-bit operating systems found in Windows 95 and NT. There also is an enhanced 16-bit version included for Windows 3.1x users. The compression utility can create self-extracting archives. This feature allows users to create program groups and register extensions in Windows 95. The program can now create spanned .zip archives, allowing users to use more than one diskette to store information. PKZIP 2.50 now supports filenames longer than eight characters. PKZIP 2.50 is priced at $49. Preregistered users of PKZIP for DOS and OS/2 may purchase the new Windows version for $29.

For more information, contact PKWARE Inc., 9025 North Deerwood Dr., Brown Deer, WI 53223; (414) 354-8699; Internet: http://www.pkware.com.

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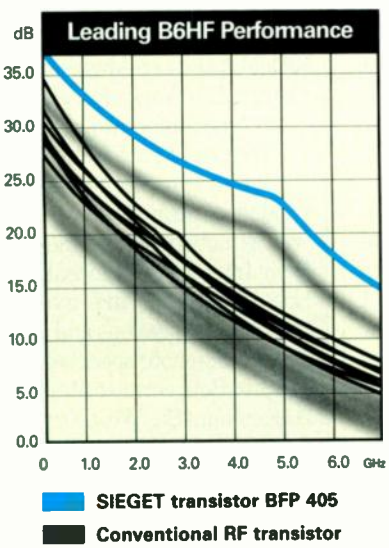

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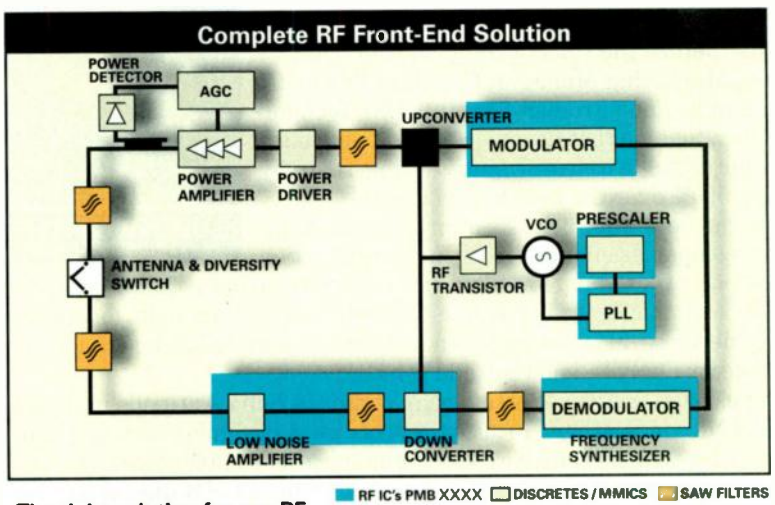

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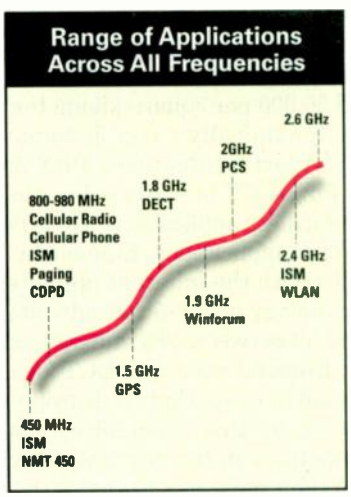

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LETTERS FROM LONDON

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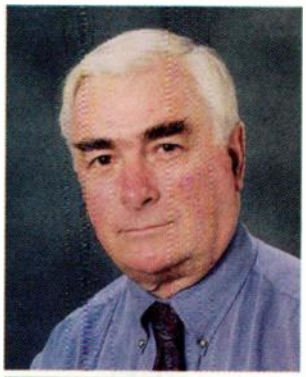

PETER FLETCHER
FIELD CORRESPONDENT

It seems that the British and Scandinavian predilection for mobile communications—I'm all but convinced that all Scandinavians have mobile phones super-glued to their faces as soon as they reach puberty—is spreading rapidly around the world to the delight of the semiconductor industry.

Just before the turn of the year, Patrick Edmond, Marketing Manager, Cordless Products, Communications Product Group, VLSI Technology Inc., told me that he expects worldwide markets for digital wireless systems will increase by nearly 500% over the next four years.

He can be so sure because at present the number of companies engaged in the mass production of the pocket-sized phones is strictly limited to no more than a dozen at most, and Patrick makes it his business to know them all. To make forecasts, all he really needs to do is "listen to what our customers tell us and make our forecasts accordingly"—and then add some.

A year ago, VLSI set up a design center in Sofia Antipolis in the foothills behind Nice in Southern France to specialize in designing complex integrated circuits for wireless and cordless communications applications. At that time, the company announced a reference design for a GSM digital handset that Edmond claims can be made for less than $150. Now, VLSI has launched a new range of chips designed for digital enhanced cordless telecommunications (DECT).

DECT was designed primarily for high-density digital cordless phone applications, especially for PABXs. It is capable of coping with user densities of around 50,000 per square kilometer. Further, it was designed to handle data with a dynamically variable bandwidth of between 32 kbits/s to a dull 1 Mbits/s. Apart from cordless PBX phones, Edmond sees a particularly bright future for DECT in wireless local loop (WLL) applications, as well as for domestic cordless applications. He is not so sure about cordless PBX systems.

In WLL applications, Edmond believes that the low cost of DECT devices, together with the inherent high-speed data capabilities of DECT, will give the technology a significant advantage over its rivals. He says, "Prices have reduced by between 20% and 30% each year for the past three years." In particular, Edmond expects DECT local loop systems to prove popular in developed countries especially in Europe.

He explains that when telecommunications is fully liberalized and opened for competition in January 1998, newly emerging network operators will need to build their networks as rapidly as possible in order to compete with incumbent national operators. At the same time, they will have to be able to offer advanced data services, he believes.

He cites Germany in particular. "Deutsche Telekom has been installing ISDN services for private subscribers as part of its competitive strategy leading up to 1998— so any competing PTO will have to offer similar services—DECT is basically the only wireless standard which is designed to be compatible with ISDN. That we see as a key emerging market for DECT."

The new chips announced by VLSI, known by the name "Vega," offer built-in capability for ISDN—both for a direct connection to a fixed line service when used as a base station, and for the provision of a 64 kbits/s digital air interface for handsets.

Peter Fletcher is Electronic Design's U.K. correspondent. His e-mail address is: panflet@cix.compulink.co.uk.

CONFERENCE CALL

Computer Telephony '97 Conference and Exhibition (CT Expo 97) will be held Mar. 4-6 at the Los Angeles Convention Center, Los Angeles, Calif. The conference features six seminar tracks by some of the leading computer telephony companies worldwide, along with numerous exhibitors and guest speakers. Among the topics to be discussed in the seminar sessions include "How to Build Voice-Enabled Internet Servers," "How to Order and Install T-1: Checklist for Success," and "PC-Based Switch Migration Strategies." For more information, contact CT Expo 97, 12 W. 21 St., New York, NY 10010; (800) 542-7279; fax (212) 691-1191; Internet: http://www.ctexpo.com.

Spring Internet World '97 will be held at the Los Angeles Convention Center, Los Angeles, Calif. from Mar. 10-14. The conference gives attendees the chance to gather information on the latest Internet technologies and products that will help companies, as well as individuals, get the most out of their Internet presence. Featured at the conference are over 600 exhibitors, 150 sessions and workshops, and five keynote speeches. For more information, contact Mecklermedia, 20 Ketchum St., Westport, CT 06880; (800) MECKLER, fax (203) 226-6976; Internet: http://events.iworld.com.

The National Ergonomics Exposition and Conference will be held April 1-3 at the Rosemont Convention Center, Rosemont (Chicago), Ill. Sessions will cover issues such as "Nerve Conduction Testing" and "The Ergonomics of Laptop Computing." Also scheduled are speeches by experts on how engineers and technologists can design and manufacture products that will reduce the risk of injuries such as Cumulative Trauma Disorder to office workers. For more information, contact Eberhard & Company, 645 Madison Ave., New York, NY 10022-1099; (212) 486-6186; fax (212) 486-6481.

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☐	ETC1.6-4-2-3	Wireless	500-2500	4:1	3 dB
☐	ETC4-1-2	Wireless	2-800	4:1	3 dB
☐	ETC9-1	Wireless	70-220	9:1	2.5 dB

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☐	ESDC-20-2-75	CATV	5-1000	20±1	1.1 dB

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☐	3	824-960	18	0.6	SOIC-8	DS53-0001
☐	4	824-960	23	1.0	SOW-16	DS54-0001
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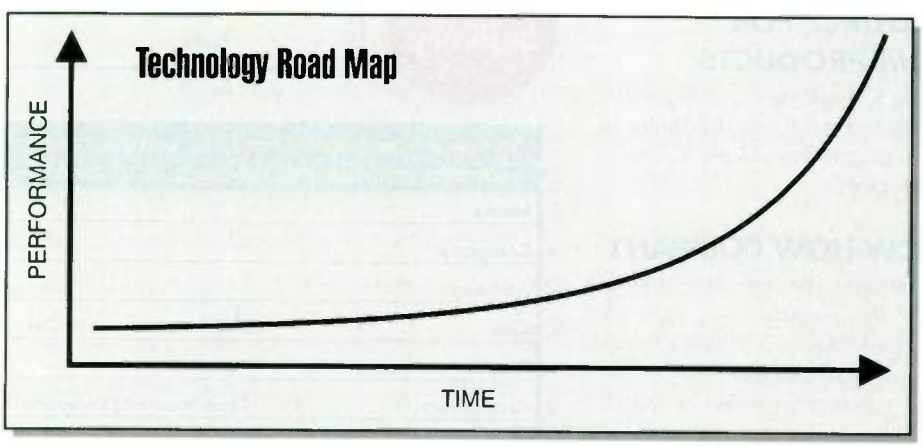

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INTERNET NEWS

Symbios Logic, in support of the IEEE-1394 standard, has made available sample quantities of its new IEEE-1394 to PCI link layer controller. The SYM13FW600 FireWire PCI controller is the result of a joint partnership with Apple Computer .

The new controller is based on Apple's Pele controller. Capable of both isochronous and asynchronous data transfers at speeds of 100, 200, and 400 Mbit/sec, the SYM13FW600 is designed for use with devices such as CD-ROM drives, hard disk drives, printers, scanners set-top boxes, televisions, and video cameras.

Features of the controller include cycle master and isochronous resource manager functions, serial bus manager support, six DBDMA channels, and two isochronous transmit and receive data streams.

The total IEEE-1394 solution, complete with host adapter boards and software, will support Windows 95, NT, and MAC-OS.

For more information, contact Symbios Logic Inc., 1731 Technology Dr., Suite 610, San Jose, CA 95110; (408) 441-1080; Internet: http://www.symbios.com.

Joining the growing numbers of companies developing "push" technologies for Internet and intranets, The Internet Company has introduced its Messenger client-server system. Messenger allows advertisers to send their information directly to users' desktops without using their e-mail or World Wide Web communications.

Content owners and publishers can use Messenger to exploit the direct marketing value of the Internet. Time-sensitive information, such as news items, product releases, or surveys can be delivered in real-time, complete with links to the corresponding web sites. Messenger also features a built-in counter for advertisements to monitor user response. There also is a "Priority Message" option that allows the provider to send urgent data, with links, to users' desktops.

The Messenger technology uses a proprietary wrapper, designed by The Internet Company to increase reliability, within an enhanced UDP transport protocol. Bandwidth-conscious providers will note that it requires slim bandwidth to deliver data. Designed for easy distribution and download, the client is small, and works well over 14.4 modems.

Pricing for Messenger is based on a per-system basis, but the base price for intranet applications is $35,000, not including consulting fees.

For more information, contact The Internet Company, 96 Sherman St., Cambridge, MA 02140; (617) 547-3600; fax (617) 546-3300; Internet: http://www.internet.com.

New FLUIDTOOLS with elbows and valves solves pipe and tube flow problems on your PC

Wouldn't it be nice if you could solve flow problems without having to look up all of your data? With FLUIDTOOLS, you can do just that? It's easy as A-B-C.

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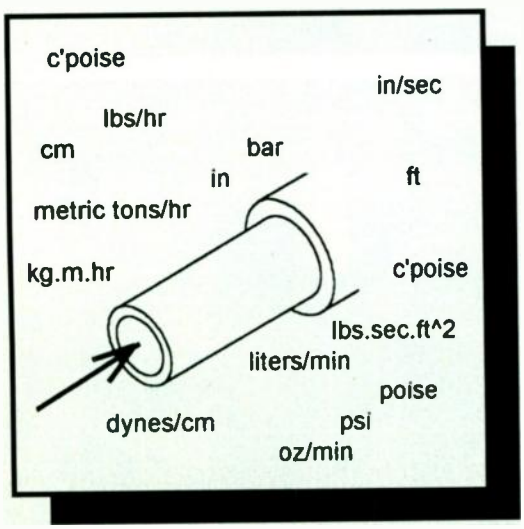
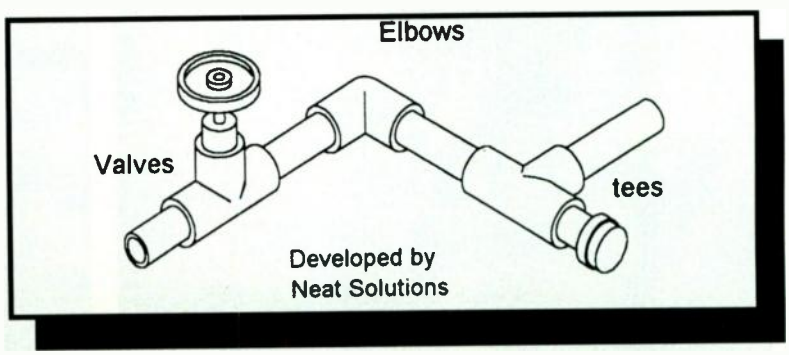
Program accepts mixed units





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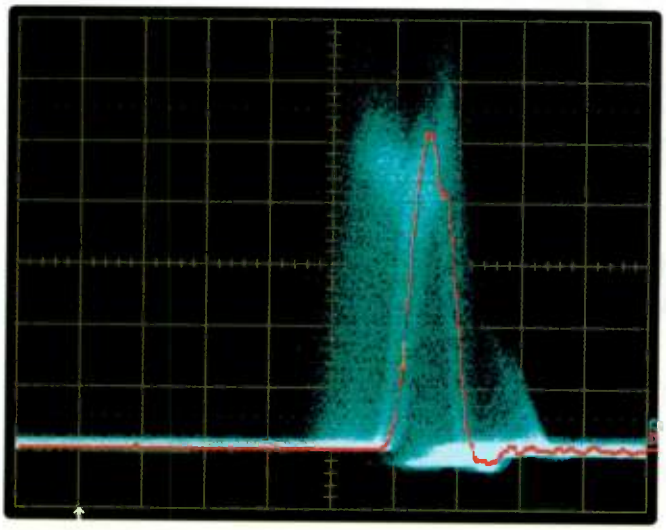

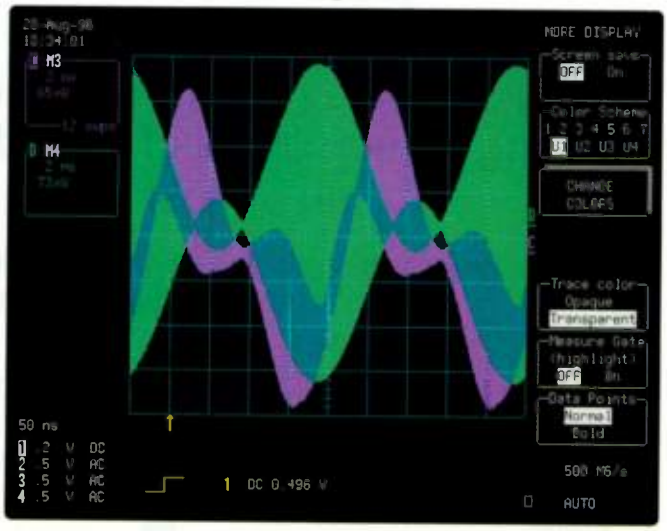

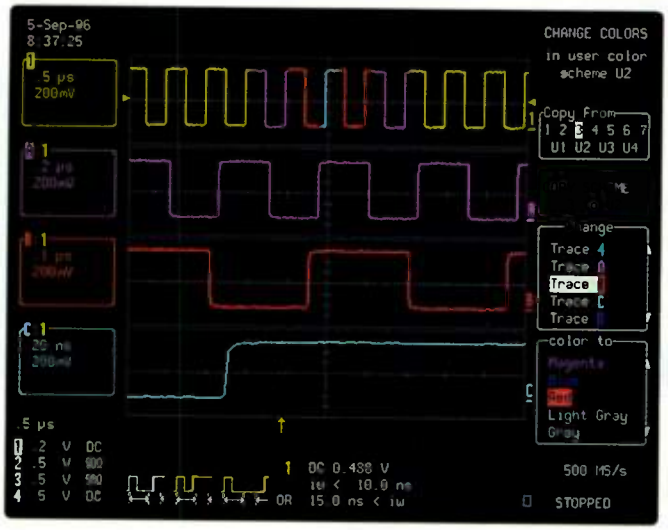

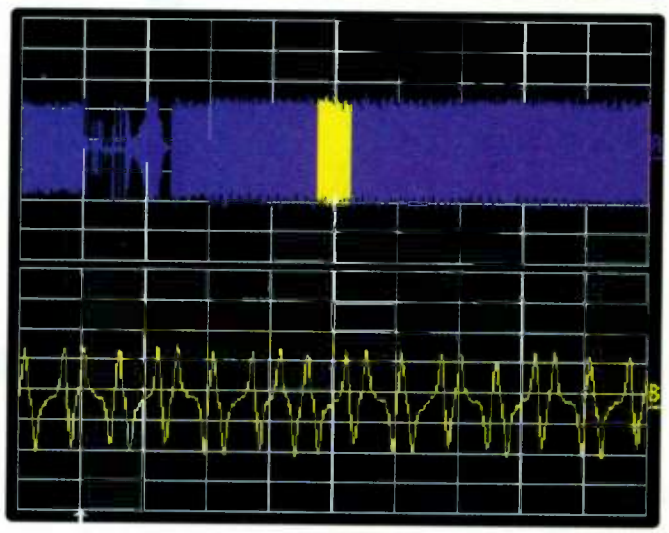

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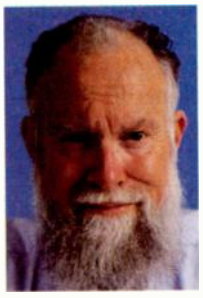
BOB PEASE

What's All This Lecturing Stuff, Anyhow?

Way back in 1968, when I was working as a Senior Engineer, back at Philbrick, I was going to take a Christmas vacation. But one engineer who was going to give some lectures suddenly decided to leave the company. So I was suddenly invited, with barely 2 weeks' warning, to go on a 3-week lecture tour, to 4 cities on the West Coast, and to Japan. I got my passport, and went on the road on December 27 and spent a week on the Coast, and 2 weeks in Japan, and it was great fun. I had a very good time, lecturing and talking about products and ideas.

I went to Japan again in 1971 and 1973. I went to Europe in 1972 and 1974. I remember being a little surprised at the end of my lecture when the German engineers went knock-knock-knock on their desks! (That's the German way to signify approval.) I remember the engineers in Kyoto who broke into APPLAUSE when my slide show demonstrated my Voltage-to-Frequency Converters covering a 1,000,000:1 dynamic range! (They liked it in Tokyo, but they didn't applaud....) I remember several years ago, when I was with a bunch of NSC FAEs (Field Applications Engineers) down in Santa Cruz, and Charlie Mitchell, the head of the FAEs, hollered across the room "Hey, Bob Pease." I walked over to talk to him, and he said "Hey, Bob, how would you like to go lecture in Europe?"



BOB PEASE OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

I told Charlie that sounded like a good idea, but I'd have to check it with my boss. Well, my boss liked the concept, but another senior engineer had more seniority, and he deserved to go. So I didn't go that year. But maybe it is now my turn. I have outlived all the other SOBs, as the old story goes.

I have usually enjoyed travel, domestic and foreign. And I have always enjoyed talking with customers, and friends of linear circuits. So I am ABSOLUTELY looking forward to going out to give some lectures.

I remember back in 1980, I went on the road for a week with the NSC Linear Road Show. We were winding up our week, lecturing in the Newark area. All the other guys had booked a flight back to San Jose that left at 5:30 PM. If they left before 4:40, they could easily make the flight—but that would leave me to close out the show all by myself. I said—No problem, let's do that, because my flight to SFO doesn't leave until 8. At about 4:30, I saw them all tippy-toeing out the back door. I waved discreetly. I finished off the lectures, and the quizzes and answers, and door prizes. And all the Questions and Answers. And I talked to all the guys who hung around after the main session to visit and talk. Then after everybody left, I started to roll up all our wires and gather up all our equipment. A phone call came in from the head of the Road Show.

"Bob, is there a little brown bag over in the corner?" I said, Yeah. "Well, take good care of it, because there are several hundred dollars of gate receipts in there." So I scooped it up and put it in my suitcase. That was no problemo.

It turns out, the laugh was on them, as my plane got me home before theirs did. That's because their plane had to make an extra stop to refuel in Salt Lake City, and was delayed considerably.

I have recently been invited by some colleagues, to "drop in," if I am in the area of New Jersey or Boston or Baltimore or Rochester, N.Y. to give a lecture. Well, I may just be doing that. BUT FIRST, I have to plan—what the heck should I talk about?

I will OBVIOUSLY be saying some good things about new linear circuits. Maybe even some good OLD ones. GOOD applications. NEAT tricks. I will surely say a few good things about *Electronic Design*. They are pretty good guys, and they have let me say good things about Analog Stuff. In fact, when we asked the guys at E.D. — would they like to co-sponsor my Lectures — they agreed! So that is nice, to let them in on the fun....

Of course, I will talk about analog circuits, and analog techniques. Maybe about Analog Multipliers. Or thermistors. We don't even make *them*. Things like PID. I might have a little DEMO on PID. My Ball-on-Beam Balancer is a fun circuit, but at 4 ft. x 1 ft. x 1 ft., it's NOT a good demonstrator to drag all over the countryside. Maybe I could design one 6-in. square x 3-in. high. That would be fun.

I will talk about various topics that have come up in my columns, and expand on them. I will *mention* my Troubleshooting book. I will *mention* my new book on "How To Drive Into ACCIDENTS—and How Not To." I do not plan to lug around a whole lot of books to sell, but I may bring along a few. I'll surely talk some about airborne computers—the natural result of the topic, "How to tell when your computer is lying".

I have given MANY kinds of lectures. I once even tried to give a lecture without slides or foils, to a bunch of 6th graders, and it nearly killed me, because without foils, I am not organized to do that.... I can use some slides, maybe a little video, mostly home-brew foils. Hand-made foils, and *audibles* made up at the line of scrimmage.

Anyhow, I will be going on the road to give a good round of lectures. They will be in a "Pease style". They will promote Analog and Linear Stuff, good thinking, and good ideas in general. I am sure it will fluctuate between *entertaining* and *educational*. After all, I have given a LOT of lectures in the last 5 years, to various IEEE and industry groups—such as a Keynote Lecture for an Embedded Systems conference, and an ASICS conference. Also, lectures to an IEEE Management Society, and an IEEE Measurement Society, and lectures on Fuzzy Logic to various IEEE groups. Lectures to several engineering school groups and industry retreats. Not to mention a wrestling match with Earl Cox. So you can see I am not exactly out of practice. I have lots of ideas that have never been in any column, that I can talk about in a Lecture. I think I can make the Lectures fun and educational.

NSC *used to* have seminars and Linear Applications lectures for an entrance fee—sometimes as much as $25. It does seem likely that we will have to charge for these lectures. I was hoping that we could charge just 2 cents. We could have run a little Ad: A picture of 2 pennies, with the text: "You can give Bob Pease your 2-cents worth." But the marketing guys said we had to charge $50. I guess that's the deal. We'll be kicking off the lecture series in the following locations:

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I hope all my fans, and all fans of Analog Stuff, will be able to attend: *"What's All This Analog Stuff, Anyhow?"*

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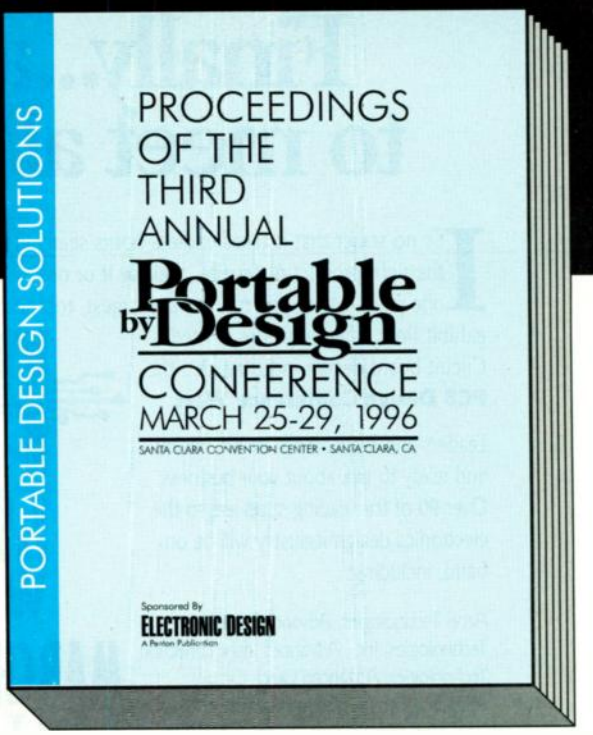

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   m. ❍ Approve purchases
   n. ❍ All of the above

4. Please specify all products and services which you specify, recommend, or buy:
   o. ❍ CAE software
   p. ❍ CAD software
   q. ❍ Interface software
   r. ❍ Autorouting software
   s. ❍ Hardware & upgrades
   t. ❍ Photoplotters/photo-plotting services
   u. ❍ Pen plotters
   v. ❍ Design services
   w. ❍ Drafting/artwork supplies

5. What is your job responsibility?
   x. ❍ Design engineer
   y. ❍ System engineer
   z. ❍ Circuit design, circuit system packaging design (including management)
   aa. ❍ Quality control/quality assurance
   bb. ❍ Research & development (including management)

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World Wide Web http://www.pcbdcon.com

An E-mail Starter Kit:

Internet E-mail With Minimum Hassle.

Communication with fellow human beings is a fundamental part of daily life. Aside from speaking face-face or by phone, permanent record communications include FAXes, conventional paper mail (US postal and/or overnight services), and the most ubiquitous of all Internet tools, *E-mail* (Electronic Mail). E-mail does require a PC, and can't accept paper input directly. Nevertheless, its virtues are many. It is faster than most other mail forms, it can easily transmit messages of long lengths, and it provides a permanent record. Printed e-mail allows the highest quality, essentially equal to the original input. Finally, it can also be used to *attach* various file types (i.e., transmit a file along with a message). These might be graphic images, program files, or, this column, which goes to Electronic Design as an e-mail attachment.

Many readers may already be plugged into some sort of e-mail system via work, in which case the program used may be outside your control. But, using e-mail from home via an Internet provider can be an extremely efficient communication tool, particularly when the latent powers of today's current programs are exploited. Having mastered ISP selection and getting Net' connected, in this column we look at an **E-mail Starter Kit** of basic concepts for Internet-style e-mail programs for Windows 3.1 and 95. Best of all e-mail virtues is the fact that, aside from your ISP service fee, e-mail traffic is basically *free*! Next best, it also goes virtually anywhere in the world—in a time frame of minutes, not days.

So, the focus of this column is on Internet compatible *off-line* e-mail programs. As this name implies, an off-line mail program operates most of the time in an off-line state, i.e., not connected to your phone line. You prepare messages at your leisure, and when ready to send they are queued for delivery, while the e-mail program calls up your WINSOCK program. It in turn dials your ISP, and net-connects, a WINSOCK feature called *demand dialing*. Once net connected, the mail program then logs into your ISP's outgoing SMTP (Simple Mail Transfer Protocol)[1,2] mail server, and sends your messages onward to their destinations. Then, it logs into your provider's POP3 (Post Office Protocol)[3] server, downloads any received messages to your local computer and disconnects, returning back to the off-line state. You can then read new messages, responding as you wish.

Note that you need not be present for this, as the mail program automatically fetches messages for you. Most e-mail programs automate the above process completely, storing your e-mail ID and password internally, making a mail send or pickup as close as a mouse click, or, alternately running as a background task, a once-per-hour (or other interval) mail checking process. As your messages arrive, you can be brought to attention with a "Mail's in!" sound[4] if you'd like.

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So, what's involved in getting a good e-mail package up and running, and what do they cost? The answers here are not much in real effort, and not much if any actual cost. This column is intentionally restricted to just some of the readily available Internet e-mail packages, with main focus on the most popular of those. If you'd like to explore these (or other) e-mail packages on the Net, just look at Forrest Stroud's useful Windows software site. To try out any of a number Windows 3.1 or 95 e-mail programs, see Stroud's "mail clients" listing under: *http://www.stroud.com/inx16.html*, or *http://www.stroud.com/inx32.html*, and download a trial program.

One might ask the obvious, since most browsers have built-in e-mail capabilities, won't that suffice? The answer is a "yes, but." Yes, you can certainly use Netscape e-mail as a starter. However, any integrated or "all-in-one" Internet application must necessarily sacrifice something, vis-à-vis an expressly tailored e-mail program (those listed below). My thinking is to use *E-mail* programs for e-mail, and browsers for browsing, i.e., the *right* tool for the right job.

E-mail program features can include a great number of things beyond just the bare ability to send/receive messages. The standard requirements list below will make a minimum set of feature requirements, while the extra (*) features will likely be found in the commercial packages.

First, any program should be easy to setup and configure. For this you'll need your e-mail ID and password, plus the applicable POP3 and SMTP server names (provided by your ISP). On-line help should be included in the package, and some minimum level of user support should also be available (FAQs, on-line newsgroup, etc.). Note that many freeware programs come with no documentation, other than built in help.

It should include a flexible, Windows-compatible text editor, or, the same, plus an integrated spell checker*.

It should include support for Internet compatible attachment encoding such as MIME[5] and UUENCODE/DECODE.

It should include an address book, for aliasing cryptic e-mail addresses into recognizable names. As extras, it can easily map received addresses into address book entries, and support multiple address books.*

It should include flexible support for hierarchical mail folders and mailboxes, so that you can organize your messages as you prefer. And as a plus, store messages in easily edited ASCII form.

Some extra features* which will most likely appear in the more complete commercial versions include: Vendor phone and/or e-mail support, mail *filtering* capability for mail organization, *support for multiple POP3 accounts*, message *encryption* capability, and support for program *plugins*.

Message filters are a great tool for organizing both incoming or outgoing mail, by virtue of the fact that they automatically place mail in an appropriate mailbox, just as you specify. Anyone handling more than a few messages per day can appreciate the utility of filters. Once set up, they re-

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ally do contribute to both ease-of-management and your overall mail organization. **TIP:** Once you see what filters can do, you'll say "This is the way E-mail is supposed to work!" More sophisticated filtering, along with spell checking are hallmarks of the more powerful e-mail programs.

Some popular off-line Windows e-mail programs are discussed below. They all have the virtue of being available for no (or low) cost, with fully supported versions available from $35 to $89. Freeware versions of these programs include the standard features above, and some, all, or more of the extra features can be found in their commercial counterparts.

While the list of E-mail programs available from the Stroud site (listed above) is a long one, just a few tend to be the more popular. Among these are **E-mail Connection**, a full featured Windows 3.1 program which also runs under 95, available from ConnectSoft, 11130 NE 33rd Place, Suite 250, Bellevue, WA, 98004; 206-827-6467, or 800-889-3499. Their URL is: *http://www.connectsoft.com/*. E-mail Connection has both freeware and commercial ($49.95) versions.

Another program is **Pegasus Mail**, suitable for both Windows 3.1 or 95. Written by David Harris, the program is available from the author: Pegasus Mail, c/o David Harris, P.O. Box 5451, Dunedin, New Zealand, plus various Net sites. Pegasus mail comes in but one basic (free) version, but there is a charge for the printed documentation ($35). Both of these programs are quite powerful, and incorporate many of the features listed above.

Eudora is a very popular e-mail program, with 18 million worldwide users claimed. It comes in both 3.1 and 95 Windows formats (the 95 version also runs under NT), plus versions for the Macintosh. For these platforms there are both freeware (Eudora Light) and commercial (Eudora Pro) versions. Eudora is available from the Eudora division of QUALCOMM Inc., 6455 Lusk Blvd, San Diego, CA, 92121-1779; (619) 658-1291 or 800 2EUDORA, or: *http://www.eudora.com*

Eudora began as a program designed expressly for the Internet, so many of its net-related features are innate. Easily the most popular e-mail program on the Net, some ISPs distribute Eudora Light, and two active USENET newsgroups plus a mail list are dedicated to it. The newsgroups are:

comp.mail.eudora.mac and:
comp.mail.eudora.ms-windows

The mailing list can be joined by sending a message of "subscribe eudora-win" to:
majordomo@wso.williams.edu

The dialogs on these forums abound in useful ideas and problem solving tips. There is also Pete Beim's uniquely useful website devoted to Eudora:
http://www.cs.nwu.edu/~beim/eudora/

This site includes many useful FAQs, freeware documentation, links to the various Eudora versions and other info sources.

Well, with all this interest, does the Eudora program deliver? You bet. Even the freeware versions have a good array of features, going beyond the basic list above. With the recently released v3.0.1 Light version there are such features as basic filters, drag and drop operation, "hot links" (auto-launch an application from a message URL), plus support for plugins and MAPI. For a more detailed freeware version comparison, check out:
http://www.cs.nwu.edu/~beim/eudora/eudora-ver-154-v-301.html

Going back about 18 months, I have used 5 different Eudora Light and Pro versions under Windows 3.1. Recently I upgraded to Eudora Pro v3.0, and tried it out on both 3.1 and 95 systems. The Windows 95 Eudora Pro version definitely has a lot of pluses vis-à-vis the 3.1 version; just two examples are extended text capabilities and a fancier graphics interface.

Some of the other Eudora Pro v3.0 extra features are powerful message filtering (you can even auto-forward incoming messages via a filter), multiple POP3 accounts, plug-in support, drag and drop operation, user customizable "stationery" templates, a customizable spell checker, a customizable toolbar (32 bit only), MAPI support, active hot links, and 90 days of toll-free phone support as well as e-mail support.

Two major features I like about Eudora are the virtually unlimited folders and mailboxes you can create, and the ability to customize filters to automatically direct in/out mail to the right mailbox. The mailbox flexibility allows you to file messages by topics you chose, such as "Analog," "Audio," etc. Obviously, this can get quite elaborate if you get carried away. Eudora support does warn against bloated mailbox systems, and the larger your mail database, the more memory resources you'll consume. However, I can't say that I've ever had a crash in Eudora due solely to an excess of mailboxes (although I've seen them for other reasons, such as a corrupt mailbox file).

Occasionally a mailbox can get messed up, and in such a case it is relatively easy to fix with an ASCII editor (Notepad). The reason this can be done is that Eudora's mailboxes are pure ASCII Internet style files, a case where the lineage definitely pays off.

TIP: Here's a "traveling e-mail" scenario. Does anyone think I'm overstating the issue of ASCII mailboxes as a significant plus? Just consider a case where you'd like to maintain a (master) desktop machine with an e-mail program and a main set of mailboxes, and sync it up with a (slave) laptop computer with similar e-mail. With Eudora, it is a simple matter of copying the mailbox files and complete directory structure from master to slave. Prior to a trip, you copy the mailboxes over to the slave, then you're on the way. You use the laptop-based Eudora for on-the-road e-mail, keeping up via your ISP's 800 #.

To work well, the slave machine needs to be set for a "leave messages on server" mail option. Upon return home, all the syncing that needs to be done is to copy all messages *sent* from the laptop over to a special mailbox on the desktop, let's call this mailbox "XFER.MBX." You can do this with a simple floppy transfer, but an even easier way would be to send yourself an extra message as you close down your laptop's use. Just attach the XFER.MBX file to it, and it will be downloaded to your desktop as you pull down those stored messages.

This single file, once copied to the Eudora desktop setup directory structure, will be recognized by Eudora, and then all the previously sent laptop messages can easily be integrated into their proper desktop system mailboxes (note that filters make this step a piece of cake). Unfortunately, I don't know of a simple way that such a "traveling e-mail" trick can be pulled

off if you are using the non-ASCII mail database files of other systems.

In summary, I have found that Eudora Pro v3.0 is one of those programs whose power seems easy to use. But, the freeware versions also offer great utility for little effort, particularly the recent v3.0.1 release. Both the commercial and freeware versions can be recommended on the basis of good to exceptional performance, and the available support (either direct or indirect). Never underestimate the importance of support! Without answers to your questions, no number of other features can compensate.

Eudora Pro v3.0 for Windows has a suggested list of $89, and Eudora Pro v2.x users can upgrade for $39. These figures are for a package including diskettes and a printed manual. Downloaded from the website, prices drop to $69 and $29 respectively (Note: street prices are as low as $49).

That's our E-mail Starter Kit, for those with questions on how to get e-mail going. Hopefully, one of the above programs will be useful to you. So, good luck with it, and send a note from your new e-mail setup!

References:

1. SMTP is described in RFC 821
2. Standard Internet messaging is described in RFC 822
3. POP3 is described in RFC 1225
4. Morticia Adams' mail arrival announcement, "The Adams Family" TV series.
5. MIME is described in RFC 1341
6. See *Eudora Pro 3.0 User Manual*, Appendices C and D for more information
7. The above RFC references and many other useful Internet information is available by FTP from: *ftp://nic.ddn.mil/rfc/*

Acknowledgement: Helpful comments on the manuscript were received from Eudora FAQs webpage author Pete Beim, and Qualcomm's Tracy Crowe.

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INSTRUMENTS

MPEG-2 Tool Captures, Replays Data Streams

The Data Stream Transport System (DSTS) captures and plays back MPEG-2 and other high-speed packetized data streams for use in testing, debugging, and prototyping systems that manipulate and transmit digital data. A proprietary disk interface, which eliminates the need for expensive DRAM storage, and an 8.2-Gbyte local disk allow up to 24 minutes of data to be stored and played back at clock rates up to 44.746 Mbits/s. The DSTS can use its own 34.368-MHz clock as the master output clock. Users can control packet length in input mode and packet timing in output mode. Currently supported data interfaces include serial differential ECL and PECL, and TTL NFS support allows data files to be downloaded from an NFS server. Call for pricing and availability. JN

Logic Innovations Inc., *6205 Lusk Blvd., San Diego, CA 92121-2731; (619) 455-7200; fax (619) 455-7273.*
CIRCLE 830

System Develops Tests At Engineer's Bench

Using the TDS-500 test development system, engineers can generate, debug, and verify test programs at their workstations and then transmit them directly to the production test floor. The system is designed to work with the company's ASL-1000 family of linear and mixed-signal testers. By creating tests on their workstations instead of production testers, users can avoid costly downtime on the test floor. The TDS-500 consists of a test head that incorporates the instrument card backplane of the ASL-1000. Its compact design allows operation on a desk or workbench without the need for a manipulator or other support. Both the instrument boards and test software are completely interchangeable between the TDS-500 and the ASL-1000. Call for information regarding price and availability. JN

TMT Inc., *880 East Arques Ave., Sunnyvale, CA 94086; (408) 730-5000.* **CIRCLE 831**

Data-Acquisition Module Runs On Laptops

The DACQ-25/12 data-acquisition module offers eight analog inputs with 12-bit resolution (0 to 4.1 V dc) and adjustable sampling rates from 12,500 samples/s to one sample every 30 seconds. Complementing the new module and the original 10-bit version (DACQ-25/10) is the DACQ-25/BB signal breakout box, which allows convenient sensor hookup through terminal strips. In addition, the Windows-based DATAQ software package that comes with the module was upgraded to include direct-to-disk data logging and a programmable controller. The modules are designed for use in portable applications, drawing only 2 mA, when active, from a laptop's parallel port. The DACQ-25 modules start at $99.95. Packages, including the breakout box, start at $139.95. JN

Base2 Computer Corp., *P.O. Box 950, Pasadena, CA 91102; (818) 583-5525; bradhite@smartlink.net*
CIRCLE 832

Reader Service No. 196 - Send Literature
Reader Service No. 201 - Please Call

INSTRUMENTS

3.3-V JTAG Controller Takes Up Less Space

The LVT8980 is a 3.3-V IEEE-1149.1 (JTAG) boundary-scan embedded test-bus controller (eTBC). The IC is 50% smaller than the previous test-bus controller, making it easier for designers to use boundary-scan test in space-sensitive applications. The controller also features an easy-to-program 8-bit interface to a microprocessor or digital signal processor. In an application, tests developed in a high-level programming language would be initiated by the system's processor and converted into boundary scan's serial bus protocol by the eTBC. The controller would then drive the test vectors over the boundary-scan test path that links ICs on the board. In 1000 units, the LVT8980 should cost under $10. JN

Texas Instruments Inc., *Semiconductor Group, SC-96050, Literature Response Center, P.O. Box 172228, Denver, CO 80217; (800) 477-8924, ext. 4500; http://www.ti.com*

CIRCLE 833

VXI Modulation Meter Measures AM, FM To 1%

The Model 8701 is a VXIbus-based modulation meter that measures AM and FM to 1% of reading; phase modulation to 3% over a carrier frequency range of 100 kHz to 2.5 GHz; and carrier levels to 0.01 dB. Carrier reference accuracy is ±3 digits on 10-Hz resolution for carriers under 1.0 GHz and 100-Hz resolution on carriers over 1.0 GHz. Operation can be completely automatic with internal frequency and level acquisition, or the carrier frequency and level can be entered over the terminal bus. Users can select from four low-pass filters, four high-pass filters, and four de-emphasis networks. True peak detectors make modulation measurements of plus, minus, or peak-to-peak divided by two, . The Model 8701, a one-slot, C-size module, costs $11,500. JN

Boonton Electronics Corp., *25 Eastmans Rd., Parsippany, NJ 07054-0465; (201) 386-9696; fax (201) 386-9191.*

CIRCLE 834

Wafer Probes Use New Communications Standard

The Generic Equipment Model (GEM) standard developed by Semiconductor Equipment and Materials International has been incorporated into the Horizon 4080X and 4090 wafer probers. GEM, an enhancement to the SEMI Equipment Communications Standard II, is the only equipment communications standard universally accepted by the semiconductor industry. By regulating and implementing communications interfaces between equipment and factory-management systems, GEM addresses the need for immediate, on-line access to equipment information. As a result, it's easier for users to condense volumes of data into one centralized information management system. The company will offer the GEM standard on all future advanced probers. JN

Electroglas Inc., *2901 Coronado Dr., Santa Clara, CA 95054; (408) 727-6500; fax (408) 982-8025.*

CIRCLE 835

BIST Line Adds ROM, Multiplier Capability

Two additions to a line of built-in self-test (BIST) products extend the testability technique to a larger portion of total IC functionality. The products are ROMBIST, which is for on-chip ROMs, and Multiplier BIST, which tests multiplier functions. Both fall under the umbrella of RSBIST, the company's regular-structure line. Related tools include RLBIST, for random logic, and BCAD, which automatically verifies compliance with IEEE-1149.1 boundary-scan standards and can be used with RSBIST and RLBIST via the RUNBIST instruction.

Another recent addition to the family is the Universal BIST Scheduler (UBS), which unifies the different parts of the BIST tool suite under one interface. RSBIST and UBS are design objects at the register transfer level, making them independent of computing platforms. Other tools are available for Hewlett-Packard and Sun hosts.

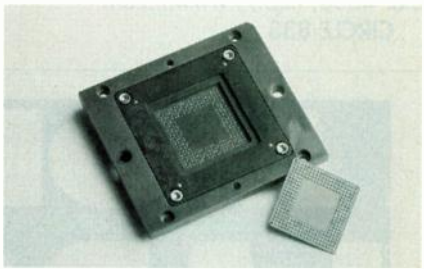
The starting price for the total IC BIST and boundary-scan product line is $95,000. Call the company for availability. JN

Lucent Technologies Inc., *Bell Labs Design Automation, Room PR5-2075, P.O. Box 900, Princeton, NJ 08540; (800) 458-8541 or (609) 639-2200; fax (609) 639-3197.*

CIRCLE 836

BGA Socket Minimizes Electrical Distances

The Micro BGA test socket uses miniature rigid contacts and a small geometry that minimizes the electrical distance between the balls of the device under test and the test load



board. The contact height for a 1.00-mm ball pitch measures 1.96 mm. The height is 1.30 mm for both 0.75- and 0.50-mm ball pitches. Contact compression forces are determined as well as controlled by the tensile properties of an elastomeric supporting element.

This element is designed to deliver predictable insertion force and contact motion for a controlled ball-to-contact wipe action. Such an action helps prevent solder build-up and facilitates the process of keeping solder debris from accumulating in the test socket.

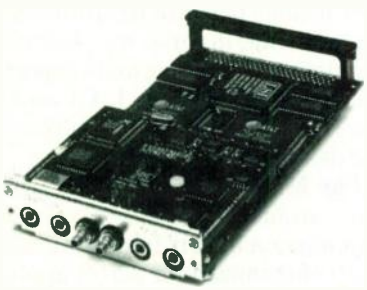
For further information, or for pricing and availability, contact the company. JN

Johnstech International Corp., *1210 New Brighton Blvd., Minneapolis, MN 55413-1641; (612) 378-2020; fax (612) 378-2030.*

CIRCLE 837

Telephony Board Has T1 Interface, Four Audio Channels

The SB32C is an S-Bus-based telephony board that can be configured for either a T1 or E1 interface. Equipped with two Lucent Technologies DSP32C digital signal processors, the board also provides four CD-quality audio input/output channels and up to 1



Mbyte of zero-wait-state SRAM. The SBC32C is suitable for various computer-telephony applications, including speech compression and recognition, text-to-speech, and secure speech. It interfaces directly with a T1 or E1 line and can transmit and receive in full-duplex mode.

Control for the frame chip is mapped into the DSP's memory space. T1 and E1 data are transmitted via the DSP's serial port over a maximum distance of 6000 ft. for T1 and 1500 m for E1 signals. The SB32C is available with either one or two DSPs; single-processor peak performance is 37 MFLOPS. The board's codec uses a delta-sigma analog-to-digital input that features 64X oversampling and linear phase digital antialiasing filters. The output sigma-delta modulator has 8X interpolation filters with 16-bit resolution.

Development support for the SB32C includes an AT&T compiler, DSP32C assembler, drivers for the Solaris and Sun operating systems, and a UNIX library of C-callable functions for host-to-DSP communications. Also included is a Windows-based source-level debugger.

Available immediately, an SB32C equipped with a single 50-MHz DSP and a T1 interface costs $2750. LG

Communication and Automation Control, *1642 Union Blvd., Suite 200, Allentown, PA 18103; (800) 367-6735 or (610) 776-6669; fax (610) 770-1232; Internet: http://www.cadsp.com.* **CIRCLE 838**

Quad 100Base-T Ethernet Transceiver Cuts Hub Power

The Am79C870 quad Fast Ethernet transceiver (QFEX) is a CMOS device that implements the MII, physical coding sublayer (PCS), and physical medium attachment (PMA) functions for four 100Base-TX/FX ports. Due to the QFEX's compact form factor, low cost-per-port, and reduced power consumption, designers will be able to realize highly competitive designs for both switched and repeater-type Ethernet hubs. Each of its four ports requires only a PMD interface device to directly drive either two multimode fibers or two pairs of Category-5 unshielded twisted-pair copper wires. Functions supported by the Am79C870 include encoding the MII 4-bit data (4B/5B); decoding the received code groups; generating carrier-sense and collision-detect indications; serializing/deserializing code groups for transmission and reception; mapping transmit, receive, carrier-sense, and the MII interfaces; and performing clock recovery. Moreover, it offers stream cipher scrambling/descrambling capability for 100Base-TX applications.

When transmitting, the QFEX chip receives 4-bit-wide data nibbles across the MII, encodes the data, serializes it, and transmits it in an NRZI data stream while the chip's four receivers reverse the process for incoming data. A programmable option permits the transmitted data to be scrambled and incoming data to be descrambled. The quad transceiver has an independent MII for each of its four ports. This allows all four ports to simultaneously transmit and receive data. The device also can be configured as a repeater hub interface, with its four ports mapped to share one or two MIIs. In addition, it features advanced features, such as an IEEE 1149.1 JTAG test port, a link monitor, and far-end fault-indication (FEFI) capability. The QFEX is available now in a 160-pin PQFP, priced at $25 for orders of 10,000 units. LG

Micro Devices Inc., *One AMD Place, P.O. Box 3453, Sunnyvale, CA 94088-3453; (800) 222-9323 or (408) 749-5703.* **CIRCLE 839**

Call Progress Receiver For Portable Applications

The M-9220-01P call-progress receiver operates at both 3 and 5 V with a lower crystal speed, thus minimizing power consumption for battery and line-powered applications. It offers a power-down mode to further conserve power when it's not being used.

The M-9220-01P is ideal for low- and line-power applications in equipment. Among these include personal/laptop computers, paging, repeaters, mobile radio, credit-card systems, and answering machines. Available now, the M-9220-01P is priced at $2.35 each in quantities of 10,000. LG

Teletone Corp., *22121 20th Ave. S.E., Bothell, WA 98021-4408; (206) 487-1515; fax (206) 487-2288.*

CIRCLE 840

IEEE 1394 Chips Let Your Products Play With FireWire

Embedding high-speed serial communications and control in your computer and multimedia equipment has been made even easier thanks to a pair of new chips that support the IEEE 1394 FireWire standard. The CDX1944 PHY-LSI is a physical-layer transceiver that can support isochronous serial FireWire communications at rates of up to 200 Mbits/s.

Its companion, the CDX1947Q LINK-LSI, is a host controller that can control several 1394 ports and interface them to a PCI host bus. Once enabled with FireWire, video cameras, computers, VCRs, and other equipment can be easily networked together using inexpensive cabling to assemble their own multimedia networks.

Both chips, which are sampling during the first quarter of 1997, are scheduled for volume production by mid-year. Pricing for the CDX1944R will be $20, while the CDX1947 will go for $50. Substantial discounts are available for production-level volumes. LG

Sony Semiconductor Co., *3300 Zanker Rd., San Jose, CA 95134; (800) 288-SONY; (408) 955-6572; fax (408) 955-5176; Internet: www.sel.sony.com/semi.*

CIRCLE 841

Digital-Access Modem Cuts Frame Relay Cost

The LTX441 is a highly integrated, single-chip digital-access modem that can reduce the cost and development time of adding Frame Relay connectivity and Internet remote access to networking products. It integrates virtually all of the analog and digital circuitry necessary to implement a Data Service Unit (DSU) on one device. The LXT441 enables full-duplex communication of end-user data at 56 or 64 kbits/s through a four-wire, twisted-pair leased line or private/public network facilities.

Operating at standard metallic loop speeds of 56 and 72 kbits/s, the device supports many service offerings, including switched 56, 56-kbit/s DDS, and 64-kbit/s clear-channel DDS. By incorporating a complete Data Communications Equipment (DCE) interface, the modem can connect directly to logic-level terminals or most popular serial controllers. The modem is able to support switched 56 call processing via its request-to-send (RTS) and data-terminal-ready (DTR) leads, or via an inexpensive microcontroller. Transmit timing can be recovered from the network or supplied from the host system. The device supports network control code detection and generation, as well as CSU and DSU loopbacks. Available now, the LXT441 comes packaged in a 44-pin PLCC and costs $25 each in quantities of 5000. LG

Level One Communications Inc., *9750 Goth Rd., Sacramento, CA 95827; Gary Sadamori, (916) 855-5000; fax (916) 854-1192; e-mail: gsadamori@level1.com.*

CIRCLE 842

ATM Cell Processor Handles Multi-Protocols At OC-3/12

Designed to operate transparently in the datapath of an asynchronous-transfer-mode (ATM) cell stream, the MXT3010 programmable cell processor can be used to perform SAR, multiplexer, or cell-in-frame (CIF) processing, as well as IP switching and other cell manipulation functions. Its speed and flexibility lend it to various applications including high-speed line termination and cell-tagging in switches and NICs, and ATM interfaces for routers. Its programmable architecture permits it to track evolving standards with simple firmware upgrades. Other less obvious applications include performing traffic shaping, policing, inverse multiplexing, signaling acceleration, and support of new protocols such as LAN emulation (LANE) and virtual source/virtual destination (VSVD).

The MXT3010's architecture is based around a specialized processor which has a 32-bit instruction set that's customized for 32-bit applications. Its pipelined, single-cycle operation architecture allows it to perform complex operations to a cell's header or contents on a per-cell basis. As an ATM layer segmentation and reassembly (SAR) device, the MXT3010 can support up to 16,000 ABR connections at line-rate bidirectional OC-3 (155 Mbits/s) speeds or unidirectional operation at OC-12 (622 Mbits/s).

The device's RAM-based buffer and programmable processing engine permit per-VC queuing using multiple queuing algorithms. In addition, it processes cells and communicates with other ATM devices that are in full compliance with the ATM Forum's traffic management 4.0 ABR specification.

A complete set of development tools and a Verilog-based simulator are available to support board-level hardware and firmware design and testing. A library of pre-developed, pre-certified cell processing and communication functions may also be licensed to facilitate any software development.

Available now, the MXT3010 is priced at $75 to $150, depending on the speed, quantity purchased, and software applications that are licensed. LG

Maker Communications Inc., *486 Totten Rd., Waltham MA. 02154; (617) 672-0622, fax (617) 672-0265. E-mail: info@maker.com or http://www.maker.com.*

CIRCLE 843

ATM Physical-Layer IC Has Built-In UTP Transceiver

The PM5350 S/UNI-Ultra is the first 155-Mbit/s ATM physical-layer device to be offered with an integrated on-chip transceiver circuit that can operate over Cat-5 unshielded twisted-pair wiring. Intended to reduce the cost and complexity of adapter cards, switches, and internetworking devices, the chip includes an analog receiver/driver, an equalizer, and baseline wander correction circuitry. Eliminating the external bipolar devices normally required to implement a line interface saves component costs, board space, and power. In addition, the high degree of integration helps minimize spurious RF emissions that can plague multichip designs. Clock jitter that typically occurs at the PHY/PMD layer is eliminated. A selectable PECL interface is provided to allow direct connection to optical data links for 51- or 155-kbit/s fiber-optic applications.The PM5350 S/UNI-Ultra is packaged in a 128-pin PQFP, and is priced at $45 each in volumes of 10,000. It's sampling now and should be shipping in production quantities during the first quarter of 1997. LG

PMC-Sierra Inc., *105-8555 Baxter Pl., Burnaby, BC Canada V5A 4V7; (604) 415-6000; fax (604) 415-6200; Web: http://www.pmc-sierra.com*

CIRCLE 844

Gigabit Ethernet Devices Handle 10- And 20-Bit Data

The S2046 and S2047 consist of a two-chip Gigabit Ethernet transmitter/receiver that can support both 10- and 20-bit data words. This dual-mode ability lets them send and receive 10-bit words at the 1062-kbit/s data rate, or 20-bit words at the 1250-Mbit/s speed approved for full-rate Gigabit Ethernet. Due to its flexibility, the chip set is targeted at applications, including high-speed ports on switches and hubs, especially in products that will bridge between older technologies and new standards. The 20-bit parallel TTL interface permits easier, less expensive interfaces to CMOS I/O structures that can handle its slower 62.5-MHz transfer rate. Employing proven interface technology from SONET products, the S2046/7 meets or exceeds the 802.3 specification's stringent limits on HSSG jitter. The S2046's on-chip PLL synthesizes the high-speed transmit clock from an inexpensive low-speed reference, while the S2047's PLL synchronizes the receiver directly to incoming digital signals. Each chip's low-jitter differential-PECL I/O for fiber-optic interfaces allows the pair to minimize crosstalk and ensure data integrity. Able to operate on supply voltages ranging from 3.3 to 5 V, the chip set typically consumes around 1 W of power. The chip set is priced at $33 per unit in OEM volumes of 50. lg

Applied Microcircuits Corp., *Marketing and Communications Dept., 6195 Lusk Blvd., San Diego, CA 92121-2793; (800) 755-AMCC or (619) 450-9333; fax (619) 450-9885; Internet: http://www.amcc.com.*

CIRCLE 845

10/100 Ethernet Transceiver Cuts Cost And Power

Requiring only a 25-MHz crystal, a simple isolation transformer and a MAC controller, the 78Q2120 is a complete single-chip 10/100Base-TX transceiver. The mixed-signal chip contains everything from the media-independent interface (MII) to a programmable line-driver circuit that can be used with a wide variety of magnetics. The transceiver, which is ideal for CardBus (PCMCIA) applications, runs off a 3.3-V supply and can run in a special bridge-driver mode that cuts transmit power consumption in half.

The receiver interfaces directly to a 1:1 isolation transformer and passes incoming signals to an on-chip adaptive equalization and dc offset adjustment, and automatic-gain block circuits. Besides cleaning up the signal, the receiver also corrects for any possible baseline dc wander that might occur. Other receiver features include a Manchester decoder with auto-polarity detection and auto-squelch control.

The chip's transmit section receives parallel digital data from the MAC chip via the MII, converts it to serial format, encodes it, and outputs it to either the 10- or 100-Mbit interface. The output circuit includes a clock generator, pulse shaper, and programmable line driver that can handle most common magnetics configurations. A separate high-impedance control port allows parallel connection to other transceivers for creating combo products. A host loopback mode also is provided for line testing and self-diagnostics. The 78Q2120 comes in an 80-lead TQFP and costs $25 each in lots of 500 pieces. LG

TDK Semiconductor Corp., *14351 Myford Rd., Tustin, CA 92780; (800) 624-8999 or (714) 573-6000; fax (714) 573-6917.*

CIRCLE 846

Cell/Packet Processor Bridges Ethernet And ATM

The SESAR (switched Ethernet SAR) is the industry's first single-chip bridge between Ethernet and ATM networks. Designed to make ATM LAN emulation (LANE) applications easy and inexpensive to implement, the SESAR processor can run transparent bridging, LLC SNAP, encapsulation, LANE, and MPOA over ATM-ready switches, routers, and enterprise hubs. Data transfer between Ethernet and ATM is performed via an internal SAR engine that intelligently translates data flows between Ethernet cells and ATM cells via AAL-5 and LANE protocols. In one possible configuration that uses only five chips, the SESAR can be interfaced to four quad-port 10-Mbit/s Ethernet controller devices (such as LSI Logic's L64381) to realize a complete 16-port switched Ethernet-to-ATM hub/concentrator. Once configured, a SESAR-based switch Ethernet packets locally or remotely (over ATM) without host intervention. The SESAR device is a purely output-buffered packet switch, capable of forwarding data at 200 kframes/s. Soon-to-be-released software device drivers will allow equipment designers to quickly integrate the SESAR into their system. Known as SESARSoft, the suite will include drivers, bridging software, LAN emulation, UNI signaling, VLAN support, and a network management agent with RMON support. Multiple SESARs may be aggregated to provide ATM connections with multi-gigabit bandwidths. Pricing for the SESAR device runs $60 in large quantities. LG

Integrated Telecom Technology Inc., *18310 Montgomery Village Ave., Suite 300, Gaithersburg, MD 20879; (301) 990-9890; fax (310) 990-9893; Web: http://www.igt.com.*

CIRCLE 847

Converter Combines Digitizer And Waveform Generator

Available in a single-slot, C-sized module, the recently developed VXIbus analog-to-digital and digital-to-analog converter offers system integrators the combination of a low-cost digitizer and waveform generator capability. Digitized signals can be captured for computer analysis and, at the same time, provide high-quality sine, triangle, and ramp waveforms for test simulation. This is made possible thanks to 16-bit vertical resolution and eight-channel mixed analog-to-digital and digital-to-analog input and outputs.

Dubbed the 6062, the device features 64-ksample memory per channel. The latest 6062 module allows a 400-ksample/s sampling rate for analog-to-digital conversion and a 2.5-Msample/s sampling rate for digital-to-analog conversion. The modules come with VXI-*plug&play* drivers and fully comply with the latest the VXIbus specification. *RE*

***Racal Instruments Ltd.**, 480 Bath Rd., Slough, Berkshire SL1 6BE, England; phone: (01734) 669969; fax: (01734) 262121.* **CIRCLE 510**

Video Capture IC First To Connect Directly To VGA Controller

The SAA7112 is the first single-chip video capture front-end to connect directly to a VGA graphics controller. Developed by Philips Semiconductors, the chip is the first in a generation of ICs for image port/memory-attached architectures designed for a new range of multimedia-enabled VGA cards and motherboard solutions.

Thanks to its high level of integration contained in one piece of silicon, glue logic can be eliminated when designing highly featured VGA video solutions. Consequently, time time-to-market for production of new VGA-based multimedia products is markedly slashed, and cost is reduced. On top of its direct interfacing to most VGA controllers, a bidirectional video expansion port with half-duplex functionality allows real-time decoded YUV data to be output from the decoder.

The SAA7112 decodes NTSC, PAL, and SECAM signals and their respective substandards to CCIR-601 color component values using Philips' line-locked clock decoding. Two analog preprocessing channels are able to accept a combination of six analog CVBS or S-Video (Y-C) inputs. In addition, its 3D scaler core can process up to 2047 active samples/line and lines/frame, and two independent programming sets can define two "ranges" per field. *RE*

***Philips Semiconductors**, P.O. Box 218, 5600 MD, Eindhoven, The Netherlands, phone: +31 40 272 20 91; fax: +31 40 272 48 25.* **CIRCLE 511**

Ruggedized Instrumentation Recorder Targets Military Apps

A recently developed digital tape recorder, called the DATaRec-D12, is suited for applications requiring extended high data rate and duration, as well as a resilience to harsh environments. Designed for the defense industry, where the COTS (commercial off the shelf) criterion is important, the recorder will find specific use in aerospace, marine, and ground vehicle operation, and for the development of lightweight, compact size, high performance, and extremely robust construction are key attributes.

The recorder's compact 3/4 ATR (air transport rack) chassis allows for mounting in various vehicles and platforms. Operating under a wide range of environmental conditions, the DATaRec-D12's heavy-duty DLT (digital linear tape) drive have integral anti-vibration mount, providing error-free operation in severe environments.

Data recording capacity is 3 hours and 40 minutes, and with the new DLT format, the recorder provides replay rates of up to 12 Mbits/s. It's compatible with a wide range of signal sources (without the need for external electronics), and supplies digital and analog input signals in numerous formats: serial, PCM, ARINC 429, 1553 bus, and analog. *RE*

***Racal-Heim GmbH**, Huttenstrasse 38, Bergisch Gladbach, D-51469, Germany.* **CIRCLE 512**

Display And Deflection Processors For TVs

The DDP 3310A is a single-chip digital display and deflection processor realized in 0.8-µm CMOS technology. It's intended for high-quality backend applications in 50-/60-Hz TV sets with 4:3 or 16:9 picture cathode ray tubes. It can be combined withDigit 3000 ICs family or with third-party products.

While the DDP 3310A is aimed at 50-/60-Hz applications, its sister product DDP 3310B is optimized for 100- Hz/32-kHz applications. One IC contains the entire fully digital video component and deflection processing, in essence forming the heart of a modem color television.

The ICs both operate with a single 5-V power supply, and they offer a black level expander, dynamic peaking, and a soft limiter for gamma correction. They both feature a programmable RGB matrix, a scan velocity modulation output, and a picture frame generator. There's also an analog RGB/fastblank input, and a separate ADC for tube measurements. *AV*

***ITT Semiconductors Group**, World Headquarters, Intermetall, Hans-Bunte-Strasse 19, 79108 Freiburg, Germany; phone: +49-761/517-0; fax:+49-761/517-2174.* **CIRCLE 513**

Sample Packs Come With Washer And Spacer Catalog

Over 12,000 non-standard size washers and spacers are included in the 78th anniversary catalog from Boker's Inc., Minneapolis, MN. This latest edition has expanded to 40 pages, adding nearly 1000 new sizes. Along with the catalog comes a Sample Pack of washers and spacers, including bright colors, unique shapes, and the latest in stampable materials, as well as a brochure explaining services offered by Boker's. Information on the company's stamping capabilities, secondary operations, minimum quantities, and delivery is spelled out. To obtain free copies of the catalog and the Sample Pack, call the company at 1 (800) 927-4377. *RE* **CIRCLE 570**

Catalog Replete With "Indestructible" Products

Everswitch USA's (Silver Spring, Md.) complete line of INDESTRUCTIBLE electronics products for harsh environments is detailed in its new free catalog. The entire line includes switches, keypads, keyboards, control panels, and custom designs. The products employ a patented piezoelectric design featuring totally sealed, one-piece, solid metal construction. The company claims the products pass every test, from extreme temperatures, to moisture, to vandalism, to even explosions. Because there are no moving parts, and no material or mechanical fatigue, life expectancy is virtually unlimited. To get the catalog, call 1 (800) 794-8243, or (301) 680-3100; fax (301) 680-9425. *RE* **CIRCLE 571**

Brochure Overviews Enduron Molding Compound Benefits

The design engineering and molding advantages of Enduron thermoset sheet molding compounds for electronic enclosures are discussed in a brochure available from Fiberite Inc., Winona, Minn. Charts and graphs help illustrate the various topics covered, such as processing guidelines, component design, material properties, impact resistance, flammability, and EMI shielding. Separate data sheets included in the brochure's folder give a specification rundown of the three Enduron products: carbon-reinforced Enduron 4685, aramid-reinforced Enduron 4690, and fiberglass-reinforced Enduron 4695. Call (507) 452-8044. *RE* **CIRCLE 572**

Liquid Crystal Polymers Are Subject Of Brochure

A new six-page brochure put out by Hoechst Celanese Corp.'s Technical Polymers Division, Summit, N.J., describes a new series of high-performance/lower-price Vectra liquid crystal polymers (LCPs). Detailed are the Vectra L Series resins' capabilities to create design freedom and how they help streamline manufacturing. According to engineering data (which is compiled in the brochure), the new Vectra grades have easier melt flow, greater latitude in processing conditions, and up to 25% faster cycle times than comparable types. For a copy of the brochure, call Hoechst Celanese's Polymer Div. at 1 (800) 526-4960. *RE* **CIRCLE 573**

Industrial Computer Source Book Adds New Products

The latest edition of the Industrial Computer Source-Book, *1997 Computer Systems Edition 1*, features approximately 25% new products. These include 275/300-MHz Alpha RISC single-board CPUs for Digital Unix and WinNT, Pentium ATX motherboards and chassis with up to nine PCI slots, and ISA-to-ISA bus expansion kits, among others. In addition, there's a technical reference section entitled "Selection of I/O: Plug-in vs. Remote," as well as a series of detailed product selection tables. Call Industrial Computer at 1 (800) 677-7329 for an index of available fax-on-demand data sheets. Also, the newest products and technical application notes can be found on the company's Internet address at http://www.industry.net/indcompsrc. *RE* **CIRCLE 574**

Power Semiconductor Databook, Brochure

Two releases from IXYS Corp. detail the latest information surrounding its power semiconductors for power-conversion and motion-control applications. In its 84-page databook, over 50 new part types are highlighted, including ultrafast switching IGBTs, 1600-V BIMOSFET power switches, and 1800-V fast switching diodes. The other release, a 14-page brochure, describes the company's high-power semiconductor capability. Featured is information on IXYS' facilities, current product range, and silicon and packaging strengths for meeting standard and customer-specific designs. Copies can be obtained free of charge through sales representatives or distributors. Or the company can be contacted directly at (408) 982-0700; fax (408) 496-0670; Internet: http://www.ixys.com. *RE* **CIRCLE 575**

Free JTAG-Compliant Components Selection Guide

Over 500 boundary-scan compatible components or component families are included in JTAG Technologies B.V.'s (Eindhoven, The Netherlands) updated Boundary-scan parts "Shopping List." Components and component families are listed by specific device type (ASICs, Bus Logic, digital signal processors, etc.). Another section lists all PLD-type devices that may be programmed "In-System" via their JTAG interface.The booklet is set up as a reference guide for digital designers and test engineers who are responsible for Design for Testability provisions in their particular company's designs. The first chapter presents a series of guidelines that pinpoint how to design-in boundary-scan as a part of a normal design process, simply by applying the designer's own rules. Categorized component listings are provided in the subsequent three chapters. For additional information, contact JTAG Technologies B.V. at ++31 40295 0870; or fax ++31 40246 8471. The company's e-mail address is: harry@jtag.nl. *RE* **CIRCLE 576**

LEGOS FOR GIRLS

had no idea that there would be such a high percentage throughout all the disciplines polled. Engineering showed 33% to be tomboys, 29% for math/science, 25% in social science, and 20% studied humanities. Standing out further, two-thirds of the women who described themselves as tomboys now see themselves as feminine. On the male side of the coin, the same trend did not hold true. When asked if they considered themselves to be "sissies" or "normal" kids, only 5% admitted to being sissies, as opposed to the 95% who had identified themselves as being normal. The study contained no definition for the terms "tomboy" or "sissy" (or "normal," for that matter), and relied on the participants' personal experience for definition.

The Climate In Joisey

In describing the campus climate, the study said it was either "warm" or "chilly" at the schools. Warm meant that there was less hate speech toward women and/or minorities, while chilly meant that there were various comments, sexist or racist jokes, or even stalking incidents at the schools. The overwhelming trend in this part of the study was that the urban campuses had warmer campus climates than the suburban schools. In addition, according to the study, the farther the school was from New York City (geographically), the more often hate speech was reported.

Two-thirds of the suburban college faculty told the study administrators that they heard sexist language on an occasional basis. Three-fifths of the faculty of the city schools said that they never heard their fellow staff members spewing racist or sexist speech.

There was a correlation between nationality and urbanity in the study. More students were inclined to make negative comments about an individual's nationality than faculty members in the suburban schools, but more faculty in the urban schools were found passing comments about nationality than students. The POWER study attributed this trend to the larger international population present at urban schools than at the suburban schools.

In the racist or sexist joke category, there was no difference in the amount of material from either the faculty or the students at the community colleges. At NJIT, however, faculty members report that their end of the academic population was more likely to use the sexist or racist language than the students. Remarkably, 45% of the NJIT faculty have overheard other faculty members tell sexist jokes, as compared to 37% of faculty members who have heard students telling sexist jokes.

All five of the New Jersey state colleges surveyed had the majority of the male faculty hearing racist jokes on their campus. The majority of the female faculty, on the other hand, did not have the same experience. The study hypothesized that perhaps the racist jokes were relegated to the men's room, keeping the female faculty in the dark about the racist joking on campus.

Ways Of Seeing

Interestingly enough, the study found that more often than not, men and women agreed on the issues raised in the questionnaires. Gender only entered into answers given for perception.

When female students and faculty were asked if the ratio of men to women in the class affected the class' dynamics, they overwhelmingly agreed. The majority of male students and faculty disagreed. Not only did they disagree, but in the engineering divisions where the male to female ratio is the highest, the disagreement also was at its highest. More than any other discipline, engineering faculty members (46%) disagreed that sex ratios affect classroom dynamic. On the other hand, 43% of the science/math, 52% of social science, and 55% of the humanities faculty agree that the ratio of men to women in the classroom affect the dynamic.

When the male professors were asked if their male students talked more in class than female students, the majority answered "no." However, the female professors who were asked the same question vehemently disagreed. According to Dr. Cavin, one possibility why this canyon of perception difference may exist is that having women teaching in engineering graduate school is a new phenomenon with no previous model to follow.

Notably, more than any other group, women in engineering faculty positions had fathers or uncles in their fields. In addition, women specializing in humanities, math, and science were more likely to have mothers in those fields.

As far as making appearances in textbooks was concerned, 55% of the engineering faculty answered that women rarely appeared in the text that they used. In the science/math department, 40% of faculty respondents replied that women appeared pretty regularly in text books; 42% of the social science faculty responded similarly, as did 60% of the humanities faculty.

The POWER Of Suggestion

The POWER program isn't just about getting more women enrolled in engineering programs, it's about raising awareness about issues that women encounter on campuses. Anyone can raise enrollment, but keeping those students and giving them incentives to stay on, eventually becoming faculty members is another story.

One of the ways that POWER is trying to achieve that goal is through gender sensitivity training sessions. Faculty members at all of the schools involved in the POWER program are offered these sessions. There are discussion groups, mock situations, as well as role reversals in the session. According to Dr. Cavin, the potential to change perception is great, as some faculty members see hundreds of students. In the NJIT training session, 30 out of 150 faculty members in the Engineering department came to the class.

POWER has been an integral part of mentoring programs at the participating schools. In its history, 40 female undergraduates and 15 graduates have participated in NJIT's mentoring program.

Deb Schiff is copy editor at Electronic Design. She attended a New Jersey state school, William Paterson College, and graduated with a B.A. in Communication. She played with her brother's Matchbox cars, and subsequently studied Audio Engineering. Ms. Schiff can be reached by e-mail at debras@csnet.net.

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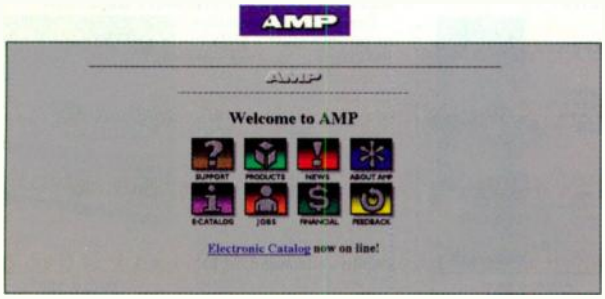

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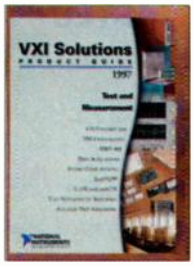
ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

FREE VXI Solutions Guide

The 1997 VXI Solutions Product Guide is a catalog and technical reference featuring product information on controllers, software, and our new VXI-DAQ instruments. VXI Solutions also includes a directory of over twenty VXI system experts from our Alliance program. Whether you develop systems internally or partner with a system integrator, VXI Solutions gives you the information that you need to build complete VXI systems.



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CIRCLE 252

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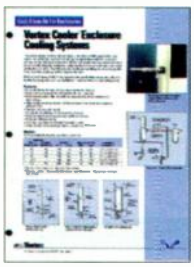

CIRCLE 257

ITW VORTEC

INTERNATIONAL SOURCE BOOK

The International Source Book offers detailed specifications on Ecliptek's through-hole and surface-mount crystals, oscillators, and inductors. Visit our internet site at http://www.ecliptek.com/ecliptek/.
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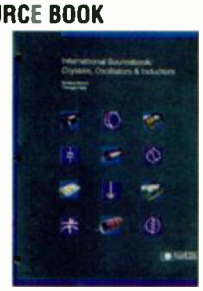

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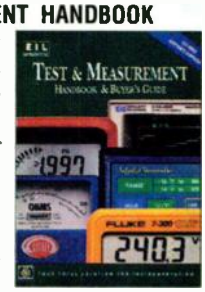
CIRCLE 259

IRONWOOD ELECTRONICS

TEST & MEASUREMENT HANDBOOK

This new catalog has been redesigned, bringing a whole new look, including full-color product shots, to its current and potential customers. E.I.L. continues to offer a wide variety of high quality products with over 450 pages of test and measurement instrumentation. Known for a wide variety of quality instruments, E.I.L. continues to offer electronic test equipment, and power measurement equipment,



CIRCLE 260

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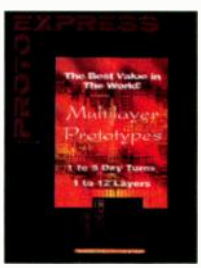

CIRCLE 261

PROTO EXPRESS

POWER INTEGRATED CIRCUITS

The 7th edition Apex Power Integrated Circuits data book contains complete product data sheets and applications notes for Apex Microtechnology's power Amplifier PWM Amplifier and DC/DC Converter product lines. Call: 1-800-862-1021; Fax: 1-520-888-3329; Email: Prolit@TeamApex.com

CIRCLE 262

APEX

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CIRCLE 263

ANSOFT

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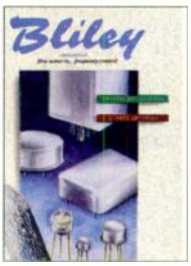
ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

NEW 1997 BLILEY CATALOG

Bliley crystal oscillators and quartz crystals are reviewed in a reader-friendly format. Spec tables, performance features cover OCXO, TCXO, VCXO, TCVCXO and clocks. Bliley quartz crystals and blanks also detailed. RFQ forms are included. The catalog is free on request. It can also be browsed on Bliley's Website at http://www.bliley.com.



CIRCLE 265

BLILEY ELECTRIC COMPANY

CRYSTAL OSCILLATOR CATALOG

A new product catalog and selection guide from Champion technologies features their full line of crystal oscillators. Technical information, specifications and mechanicals are featured in this catalog for over 60 of Champion's VXCOs, TCXOs, VCTCXOs, data clocks and related products. Frequency ranges up to 155.52 MHz for general purpose to high frequency or tight stability applications.Phone: 847/451/1000

CIRCLE 266

CHAMPION TECHNOLOGIES

NEW DC POWER SUPPLY CATALOG

The new catalog of DC power supplies, from an ISO9002 registered manufacturer, features rugged reliable bench units and programmable system supplies. Power outputs from 60 to 3000 watts are standard with features suitable for most applications. Five year warranty is standard. Send for your free catalog of call 1800-667-8422. Email: xantex@xantrex.com

CIRCLE 267

XANTREX

RF/IF DESIGNER'S GUIDE

180 page RF/IF Designer's Guide is looked with informative features such as practical articles, definitions of terms, environmental and reliability test procedures, answers to frequently asked surface mount technology questions, and more! It also contains the most complete and up-to-date specifications and price information about all Mini-Circuits signal processing components.

CIRCLE 268

MINI-CIRCUITS

NEW ROTATION PROCESSOR

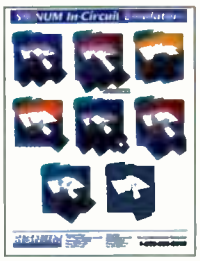
Sumitomo recently unveiled it's new IP90C16 rotation/ enlarging/ reducing processor. The chip offers bi-linear interpolation for high-resolution image system analysis even after rotation and is one of 15 specific function imaging components now available. Other chips include a color memory controller with 16-bit image throughput up to 27Mpixel/sec.

CIRCLE 269

ROSS ASSOCIATES

80186, 80196, 8051 EMULATION

Signum Systems has released its 1996 catalog of in-circuit emulators. This full line catalog includes Intel processors, Texas Instruments DSP's Zilog controllers, and National Semiconductor HPC family. Call (800) 838-8012 for information. Internet address: ww.signum.com



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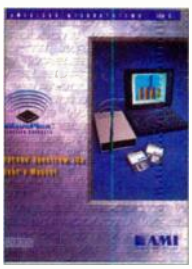

CIRCLE 272

AMERICAN MICROSYSTEMS INC.

DIFFERENTIAL MEASUREMENTS

A discussion of sing;e-ended and differential scope measurements on ground referenced and floating signals. differential amplifier characteristics such as common mode rejection ratio and commen mode range are covered.

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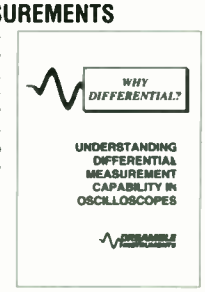

CIRCLE 273

PREAMBLE INSTRUMENTS

TELECOM SOLUTIONS DATABOOK

Teltone's 224-page Databook features a wide range of products for network interface applications, including: DTMF Receivers, DTMF Transceivers w/Call Progress Detection, Call Progress Tone Detectors, Line Sensing Relays, test tools including Telephone Line Simulators and ISDN Line Simulators, application notes, and more. For your copy call 1-800-426-3926 or 206-487-1515, E-mail at info@teltone.com.

CIRCLE 274

TELTONE

"X86 and 683xx/HC16 Design Tips"

Free application note shows how to use in-circuit emulation to isolate real-time events. Set clock-edge triggers, and then use trace to display system status and the source code leading up to the event. For immediate response: WEB page: www.microtekintl.com Voice: 800-886-7333

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MICROTEK INTERNATIONAL

1997 FLASH MEMORY DATA BOOK

The 1997 Flash Data Book from Micron Quantum Devices, Inc. is now available. This updated edition features sections on our industry-standard, IntelÒ - compatible 2,4 and 8 Meg SmartVoltage Boot Block Flash memories, and future products such as 8 and 16 Meg Sectored Erase Flash and the Flash ATA and CompactFlash™ Card families.

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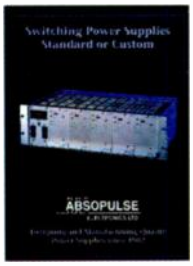

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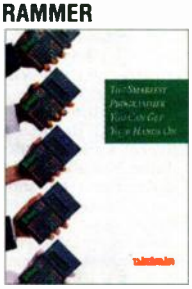

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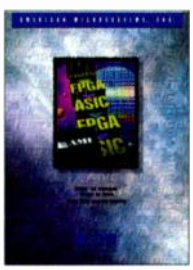

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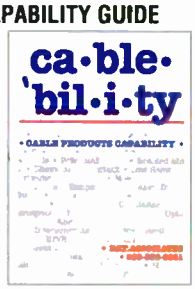
AMERICAN MICROSYSTEMS INC.

CABLE PRODUCTS CAPABILITY GUIDE

Designed to aid engineers in their cable, wire, assembly, and high-tech interconnect applications, this free Cable Products Capability Guide from Bay Associates, Menlo Park, CA, features the company's unique products, services, materials and processes.



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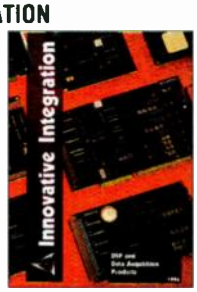

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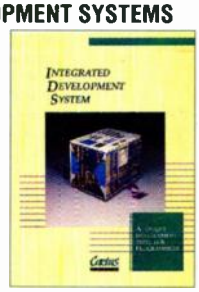
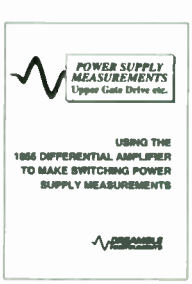


CIRCLE 293

CACTUS LOGIC

APPLICATION NOTE

Covers how to make safe and reliable measurements on switching power supplies operating on line. Includes such difficult measurements as upper gate drive and transistor saturation characteristics. Tells how to quantity measurement corruption caused by high dv/dt common mode. 1-800-376-7007



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INTERFACE TECHNOLOGIES

OMRON RELAYS, SWITCHES, MORE

Standard Product Catalog shows Omron's most popular relays, switches, and sensors. The 176 page catalog also includes card readers, time delay relays, totalizers, limit switches and temperature controllers. Literature sent only to addresses in the U.S.A. Omron Electronics, Inc. Call toll-free 1-800-55-OMRON or e-mail EDLit@oei.omron.com

CIRCLE 297

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CIRCLE 298

MODEL TECHNOLOGY

MECHANICAL ENCODER SOLUTIONS

New product Bulletin #698 lists the Series 25, single and multi-deck encoders. The Series 25 offers Binary, Binary Compliment and Gray code outputs in 1 deck through 4 decks. Choose from 4 to 36 switch positions for the selected code output. For an economical alternative, The Series 25L, single deck design, provides similar coding and position choices. The Series 25L is priced at $1.25 in production quantities.

CIRCLE 299

GRAYHILL

KEY SWITCHES SURVIVE

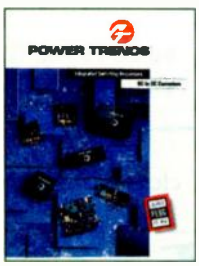
Low-profile tactile key switches with through-hole and surface - mount terminals are sealed to withstand wave-soldering and cleaning processes. Surface-mount models also tolerate reflow, vapor phase, hot-stamp, and laser soldering. The Rafi Racon 8 is approximately 5-mm high by 8-mm square; the Racon 12 is approximately 5-mm high by 12-mm square with an optional plunger to increase the height to 12.5mm .

CIRCLE 309

C&K COMPONENTS INC.

NEW SWITCHING REGULATORS

Power Trends Inc., has released a new 80 page full line catalog for its Integrated Switching Regulators (ISRs) and DC to DC Converters. The catalog introduces significant new products along with extensions to existing product lines. Complete specifications, photos and standard applications are provided for each product, along with mechanical configuration options and ordering information.



CIRCLE 302

POWER TRENDS INC.

ILLINOIS CAPACITOR'S CATALOG

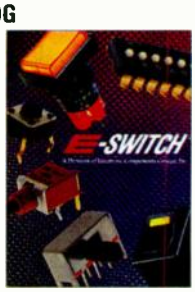
Illinois Capacitor's and Engineering Guide contains complete information on company's aluminum electrolytic, film, ceramic and power capacitors. It's all you need to make a knowledgeable capacitor selection. Available capacitance range, voltage ranges, operating temperature, case styles, IC authorized distributor listings, 208 pages.

CIRCLE 303

ILLINOIS CAPACITOR, INC.

NEW SWITCH CATALOG

The ALL-NEW, color E-Switch catalog contains 28 additional pages, including new lines of DIP, pushbutton, and gold tact switches. The catalog gives complete specifications for pushbutton, toggle, rocker, power, lever, slide, rotary, keylock, DIP, and tact switches. SMT and lighted versions available. 612-504-3525, http://www.e-switch.com.



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E-SWITCH

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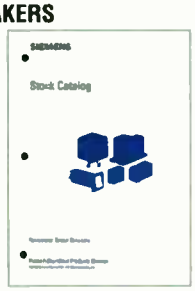

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SIEMENS ELECTROMECHANICAL

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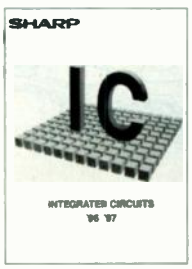

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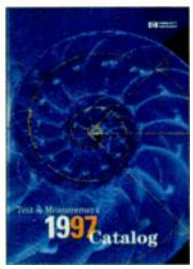

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Issue Date	Closing
February 17	1/7/97
March 3	1/22/97
March 17	2/5/97
April 1	2/20/97
April 14	3/5/97
May 1	3/21/97
May 12	4/2/97
May 27	4/17/97
June 9	4/30/97
June 23	5/14/97
July 7	5/29/97
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August 4	6/25/97
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September 15	8/6/97
October 1	8/22/97
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32 ☐ Video Controller

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02 ☐ Logic ICs
04 ☐ Storage Controller
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32 ☐ Memory Modules

A3 01 ☐ ICs, other

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32 ☐ Power Semiconductor Devices

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C ASICS
01 ☐ Gate Arrays
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08 ☐ Standard Cells
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32 ☐ Megacell Functions (CPU cores, etc.)

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E Interconnections & Packaging
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02 ☐ Wire & Cable
04 ☐ Fiber-optic Cable
08 ☐ Enclosures
16 ☐ Materials
32 ☐ Printed Circuits

E2 01 ☐ EMI/EMC Components & Materials

F Power
01 ☐ Power Supplies
02 ☐ Batteries

G Test & Measurement
01 ☐ Logic Analyzers
02 ☐ Development Systems
04 ☐ Oscilloscopes
08 ☐ Other Test Instruments
16 ☐ ATE
32 ☐ Field Test & Service Equipment

G2 01 ☐ Communications/Test Equipment
02 ☐ Data Acquisition Hardware/Software
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I Computer Boards
01 ☐ CPU Boards
02 ☐ Analog I/O & Converter Boards
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I2 01 ☐ DSP Boards
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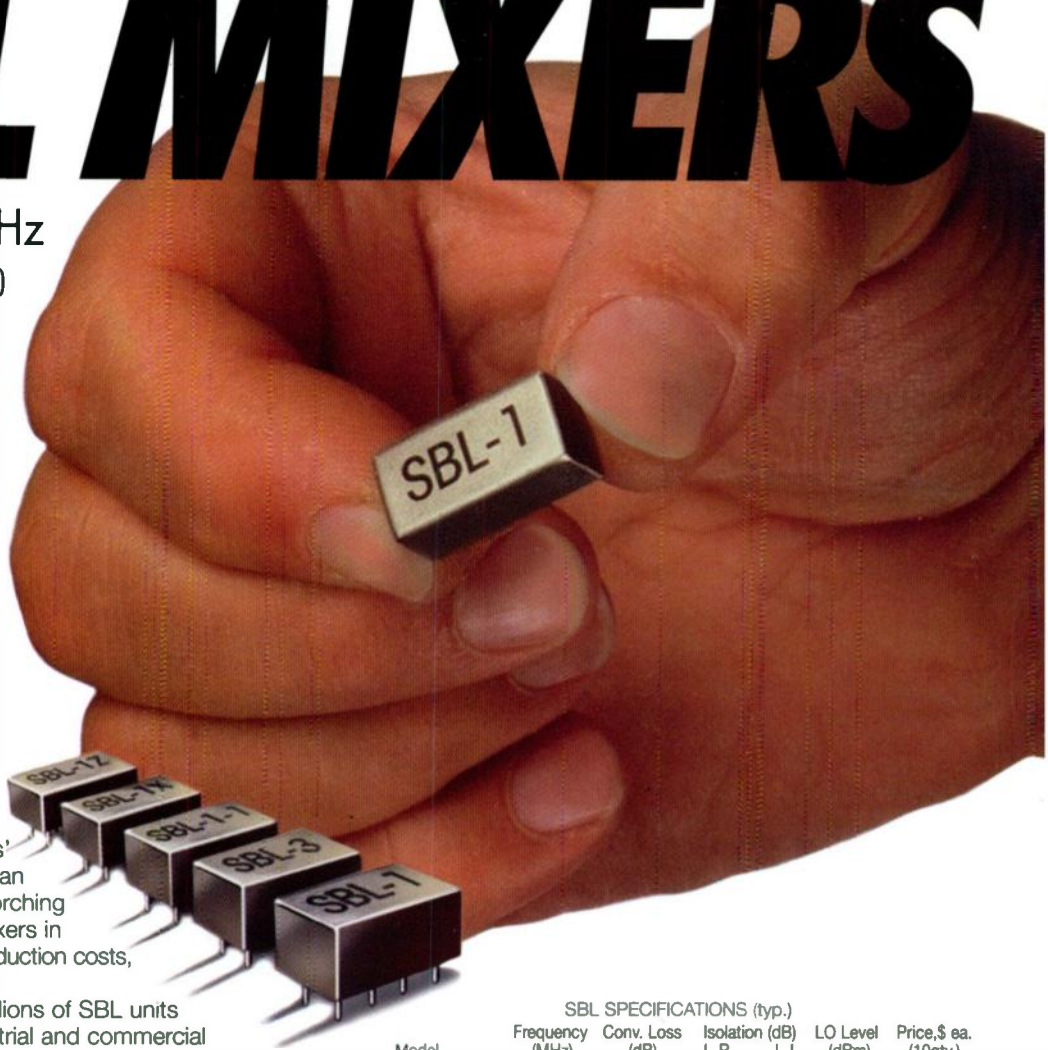

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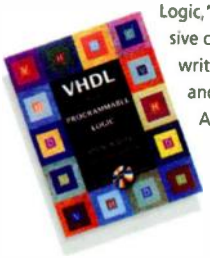

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