ELECTRONIC DESIGN

FOR ENGINEERS AND ENGINEERING MANAGERS - WORLDWIDE

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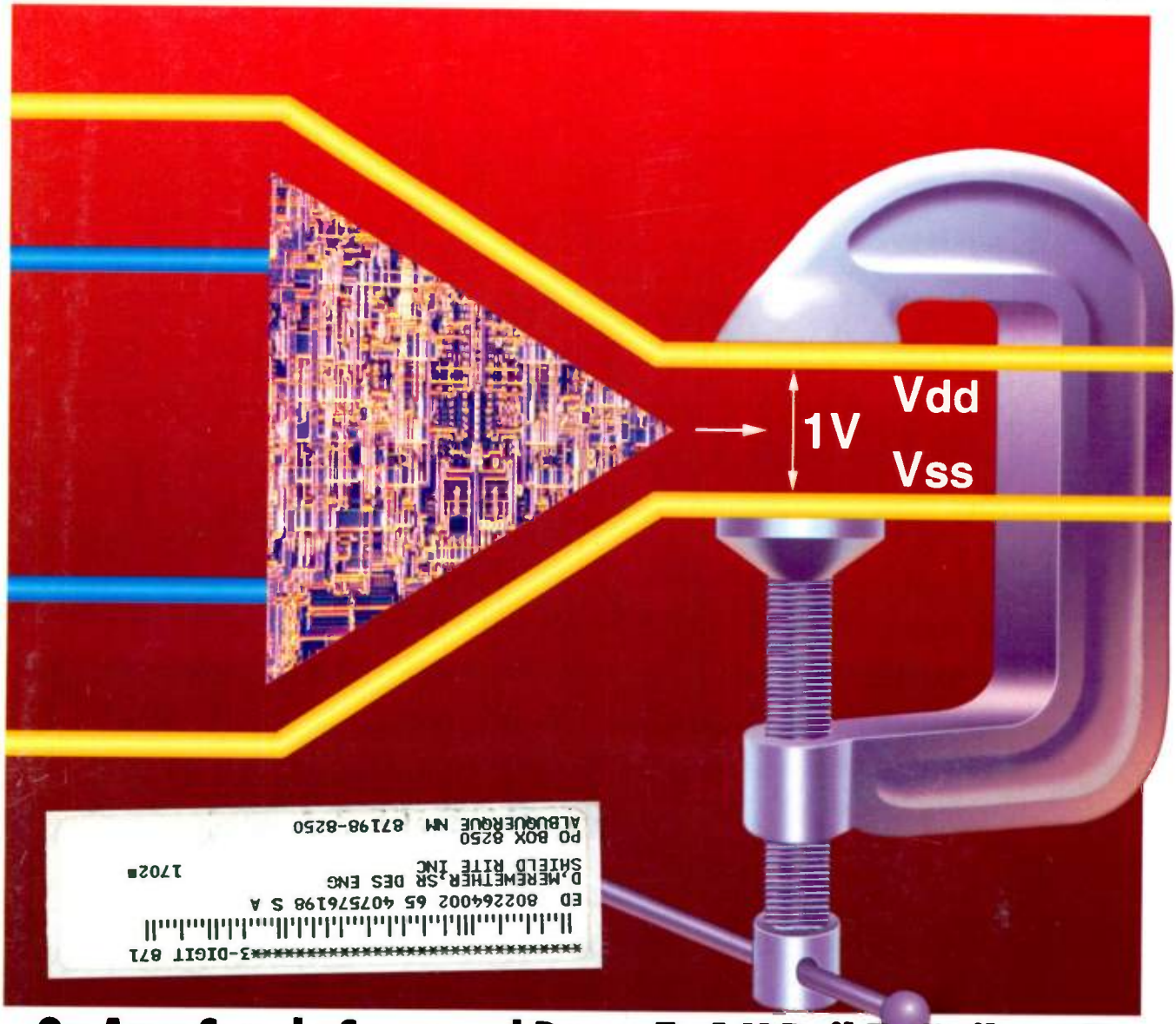
FEBRUARY 17, 1997



Op Amp Supply Squeezed Down To 1 V Rail-To-Rail p. 87

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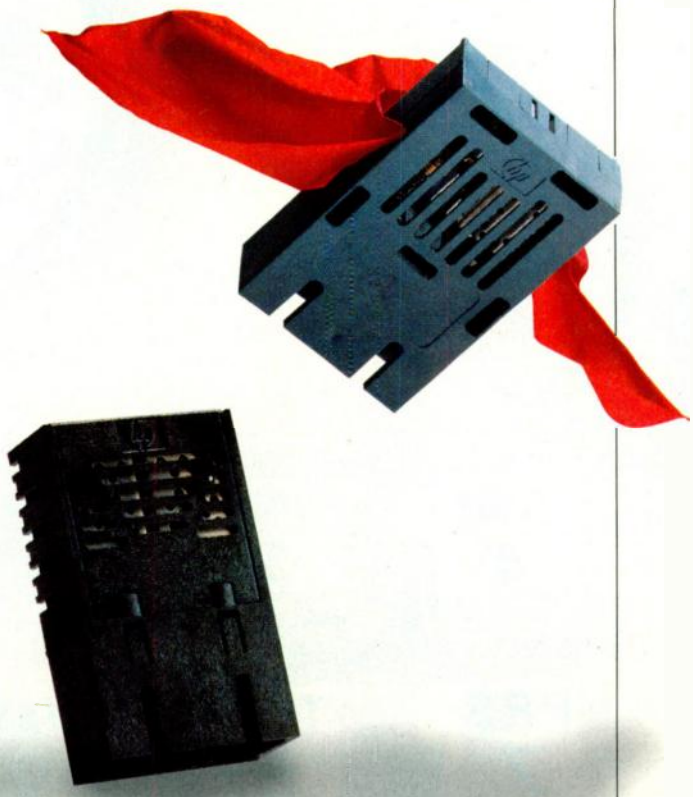

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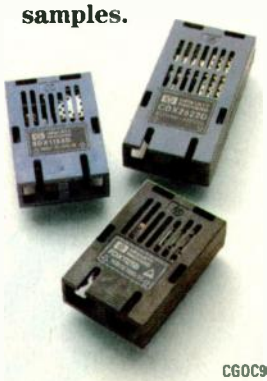

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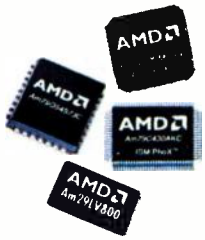

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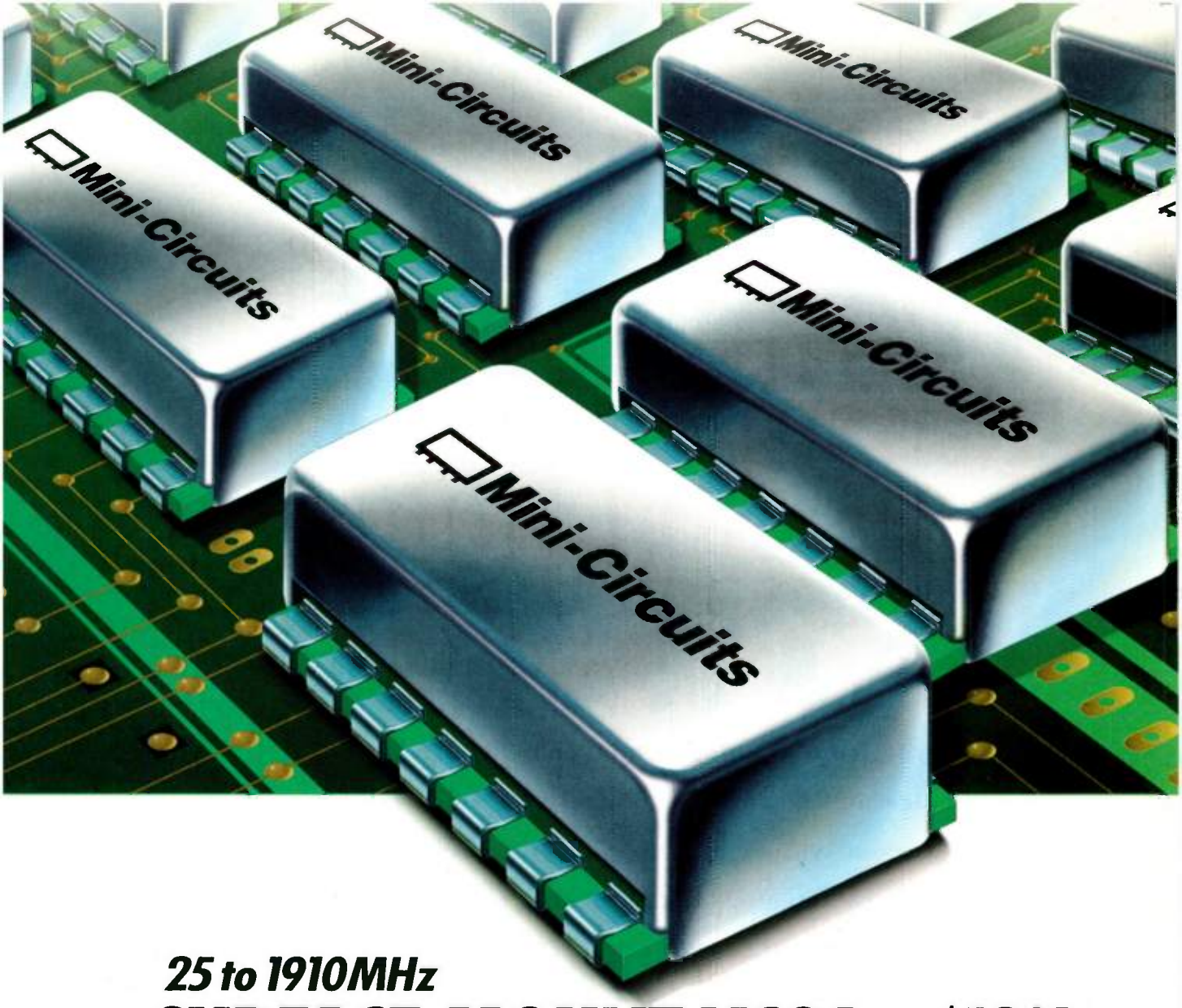

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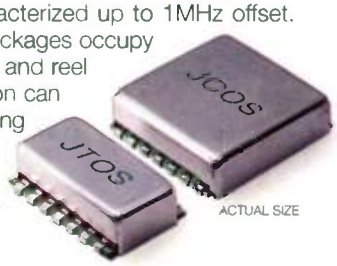

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JTOS-75	37.5-75	-110	-27	16V	20	13.95
JTOS-100	50-100	-108	-35	16V	18	13.95
JTOS-150	75-150	-106	-23	16V	20	13.95
JTOS-200	100-200	-105	-25	16V	20	13.95
JTOS-300	150-280	-102	-28	16V	20	15.95
JTOS-400	200-380	-102	-25	16V	20	15.95
JTOS-535	300-525	-97	-28		20	15.95
JTOS-765	485-765	-98	-30	16V	20	16.95
JTOS-1025	685-1025	-94	-28	16V	22	18.95
JTOS-1300	900-1300	-95	-28	20V	30	18.95
JTOS-1650	1200-1650	-95	-20	13V	30	19.95
JTOS-1910	1625-1910	-92	-13	12V	20	19.95
JCOS-820WLN	780-860	-112	-13	20V	25 (@9V)	49.95
JCOS-820BLN	807-832	-112	-24	14V	25 (@10V)	49.95
JCOS-1100LN	1079-1114	-110	-15	20V	25 (@8V)	49.95

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See "RF/IF Designer's Guide" or "VCO Designer's Handbook" for complete specifications.

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ELECTRONIC DESIGN

February 17, 1997 Volume 45, Number 4

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TECH INSIGHTS

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ELECTRONIC DESIGN

February 17, 1997 Volume 45, Number 4

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MULTIMEDIA

QUICK LOOK

DEPARTMENTS

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1968 First Place Award	1980 Certificate of Merit
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NORTH AMERICAN EDITION

Executive Editor: **ROGER ALLAN** (201) 393-6057 rallan@class.org
Managing Editor: **BOB MILNE** (201) 393-6058 bmilne@class.org

Technology Editors:

Analog: **PAUL McGOLDRICK** (San Jose) (408) 441-0550, ext. 113; 102447.346@compuserve.com
Analog & Power: **FRANK GOODENOUGH** (617) 227-4388 75410.2361@compuserve.com
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New Products: **ROGER ENGELKE JR.** (201) 393-6276 rogere@csnet.net
Contributing Products Editor: **MILT LEONARD**

Editorial Headquarters:

(201) 393-6060 Fax: (201) 393-0204 E-mail: edesign@class.org
P.O. Box 821, Hasbrouck Heights, N.J. 07604

Field Correspondents:

West Coast Executive Editor:
DAVE BURSKY (San Jose) (408) 441-0550, ext. 105; dbursky@class.org
Western Regional Editors:
CHERYL J. AJLUNI (San Jose) (408) 441-0550, ext. 102; cjajluni@class.org
PAUL MCGOLDRICK (San Jose) (408) 441-0550, ext. 113; 102447.346@compuserve.com
TOM WILLIAMS (Scotts Valley) (408) 335-1509 tomwillm@ix.netcom.com
2025 Gateway Place, Suite 354, San Jose, CA 95110
(408) 441-0550 Fax: (408) 441-6052

London: **PETER FLETCHER**
16 Maylons Road, Hextable, Kent, UK
44 1 322 664 355 Fax: 44 1 322 669 829 E-mail: panflet@cix.compulink.uk.co

Munich: **ALFRED B. VOLLMER**
Eichenstr. 6, 82024 Taufkirchen (near Munich) Germany
49 89 614-8377 Fax: 49 89 614-8278 E-mail: 75162.1246@compuserve.com

Chief Copy Editor: **MICHAEL SCIANNAMEA** (201) 393-6024 mikemea@class.org
Copy Editor: **DEBRA SCHIFF** (201) 393-6221 debras@csnet.net
Consulting Editor: **LISA MALINIAK**
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Editorial Director: **STEPHEN E. SCRUPSKI** (201) 393-6070
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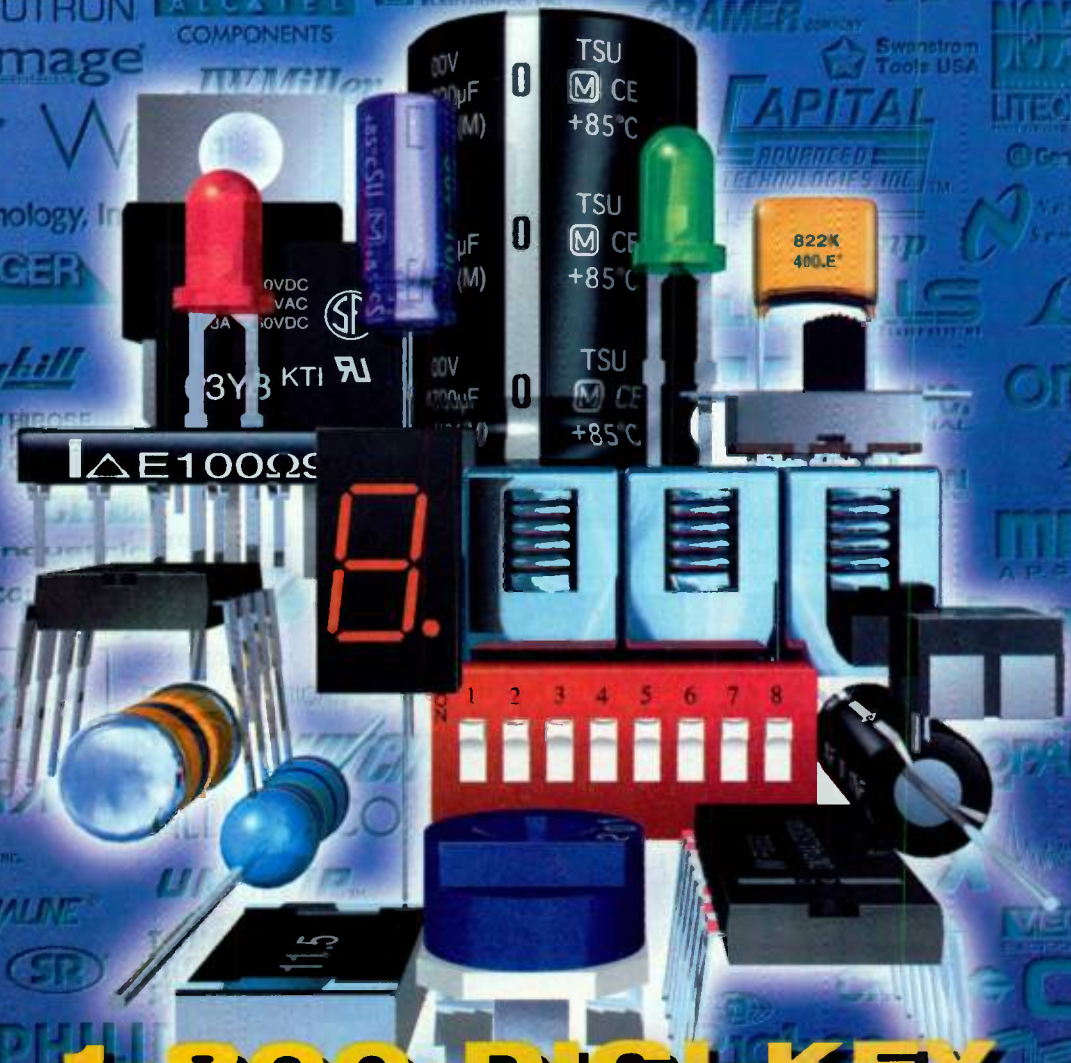

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MEETINGS

MARCH 1997

Computer Telephony Expo '97, Mar. 4-6. Los Angeles Convention Center, Los Angeles, California. Contact (212) 691-8215.

IPC Printed Circuits Expo 97 & 40th Annual Meeting, Mach 9-13. San Jose Convention Center, San Jose, Californria. Contact JoAnn Galluzzi (847) 509-9700; Internet: http://www.ipc.org.

Embedded Systems Conference East, Mar. 10-12. Hynes Convention Center, Boston, MA. Contact (617) 821-9222; e-mail: esce@exporeg.com.

PCB Design Conference West, Mar. 15-21. Santa Clara Convention Center, Santa Clara, California. Contact PCB Design Conference, P.O. Box 472, Canton, Massachusetts 02021; (617) 828-9185; fax (617) 828-8198.

European Design & Test Conference (ED&TC '97), Mar. 17-20. CNIT Conference & Exhibition Centre, Paris-La Defense, France. Contact ED&TC Conference Secretariat, CEP Consultants Ltd., 43 Manor Pl., Edinburgh, EH3 7EB, UK; (44) 131-300 3300; fax (44) 131-300 3400; e-mail: edtc@cep.u-net.com.

Antennas: Principles, Design, and Measurements (Short Course), March 18-21. Mission Bay, San Diego, California. Contact Kelly Brown, NCEE, 1101 Massachusetts Avenue, St. Cloud, Florida 34769; (407) 892-6146; fax (407) 892-0406.

Communication Design Engineering Conference, Mar. 24-26. Washington, DC. Convention Center, Washington, DC. Contact Denise Chan, Miller-Freeman Inc., (415) 278-5231.

Portable By Design Conference and Exhibition, March 24-27. Santa Clara Convention Center, Santa Clara, California. Contact Betsy Tapp, (201) 393-6075; fax (201) 393-6073; e-mail: portable@class.org.

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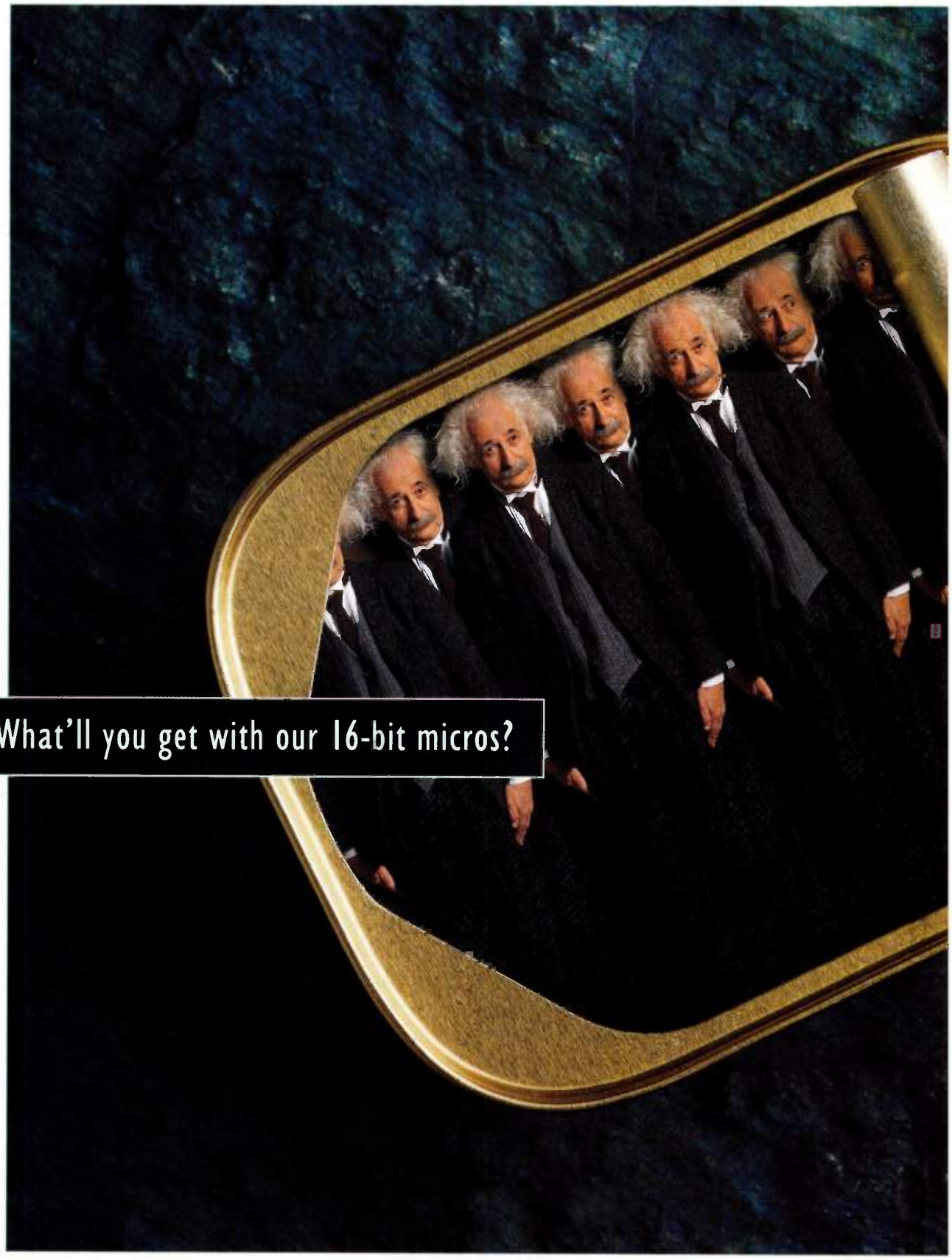
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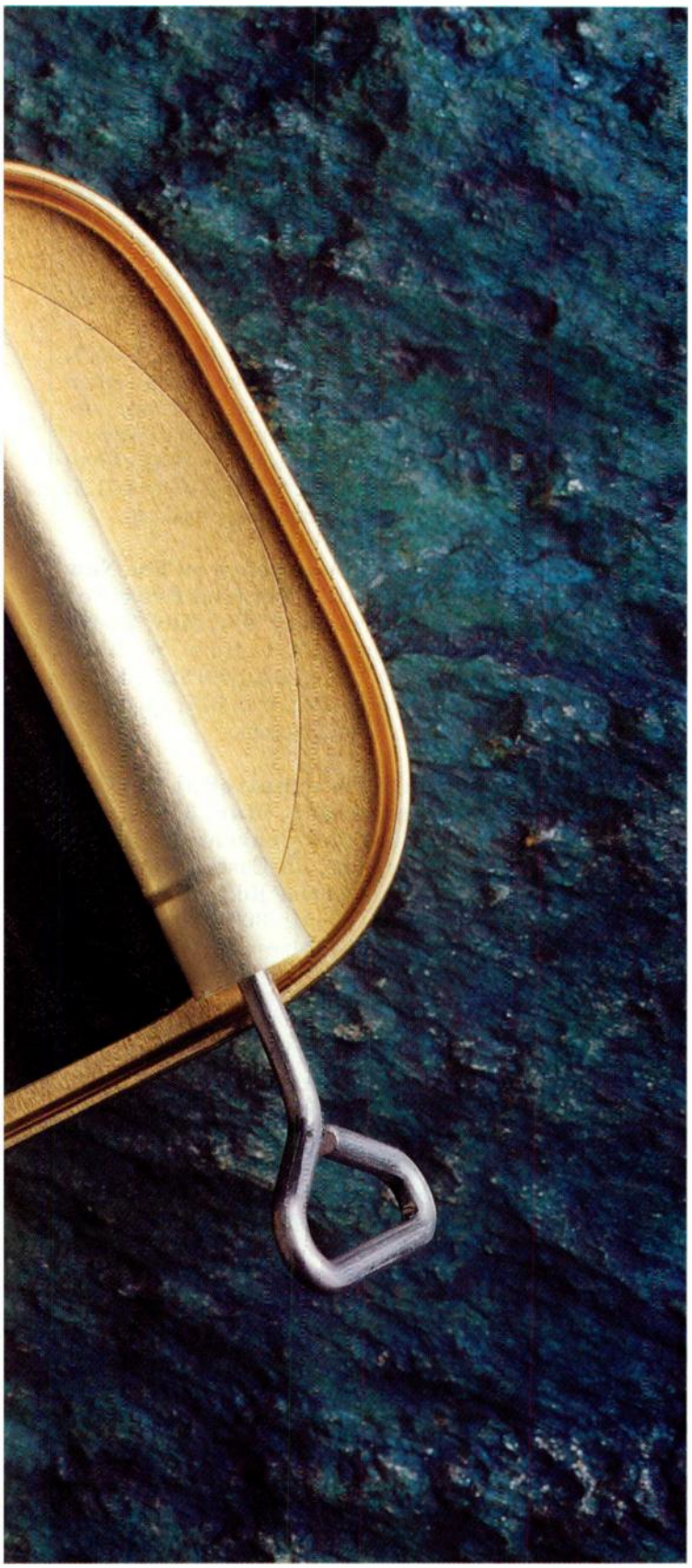

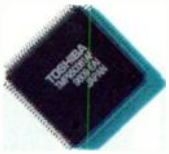

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DSP World Spring Design Conference, Mar. 25-27. Washington Convention Center, Washington, DC. Contact Denise Chan, Miller Freeman Inc., (415) 278-5231; e-mail: dsp@exoreg.com.

SOUTHCON '97, Mar. 25-27. Raleigh Civic and Convention Center, Raleigh, NC. Contact Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045; (800) 877-2668 ext. 243; fax (310) 641-5117; e-mail: southcon@ieee.word.org.

Second Conference on The New Integrated Service Provider (Supercarrier '97), Mar. 26-28. Washington Vista Hotel, Washington, DC. Contact (800) 822-6338 or (202) 842-3022 ext. 317; Internet: http://www.brp.com.

Sixth International Verilog Conference, Mar. 31-Apr. 2. Santa Clara Convention Center, Santa Clara, CA. Contact MP Associates, 5305 Spine Rd., Suite A, Boulder, CO 80301; (303) 530-4562; fax (303) 530-4334; e-mail: ivcinfo@ivc-conf.com.

APRIL

INTERMAG '97, Apr. 1-4. Hyatt Regency Hotel, New Orleans, LA. Contact John Nyenhuis, School of Electrical Engineering, Purdue University, West Lafayette, IN 47907-1285; (317) 494-3524; fax (317) 494-2706; e-mail: nyenhuis@ecn.purdue.edu.

Surface-Mount Technology Association, Apr. 2. Gwinnett County Civic Center, Atlanta GA. Contact (770) 569-1822; e-mail: smta-info@t-tech.com; Internet: http://www.smta.org.

IEEE International Reliability Physics Symposium, April 7-10. Adams Mark Hotel, Denver, CO. Contact IRPS Publishing Services, P.O. Box 308, Westmoreland, NY 13490; (315) 339-3971; fax (315) 336-9134; e-mail: 103227.2074@compuserve.com.

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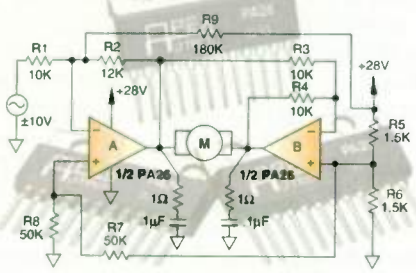

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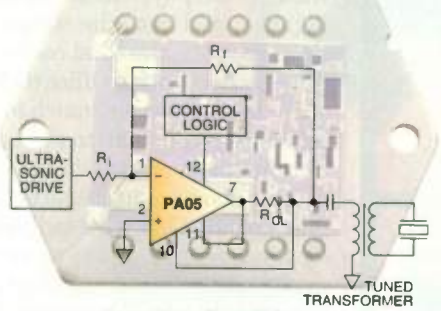

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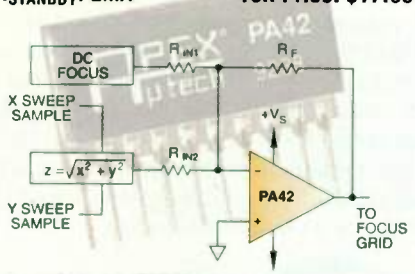

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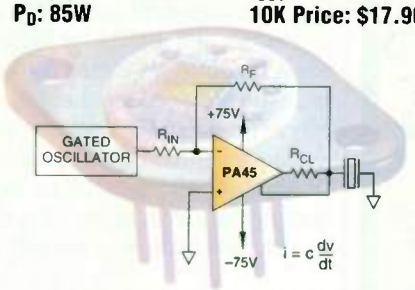

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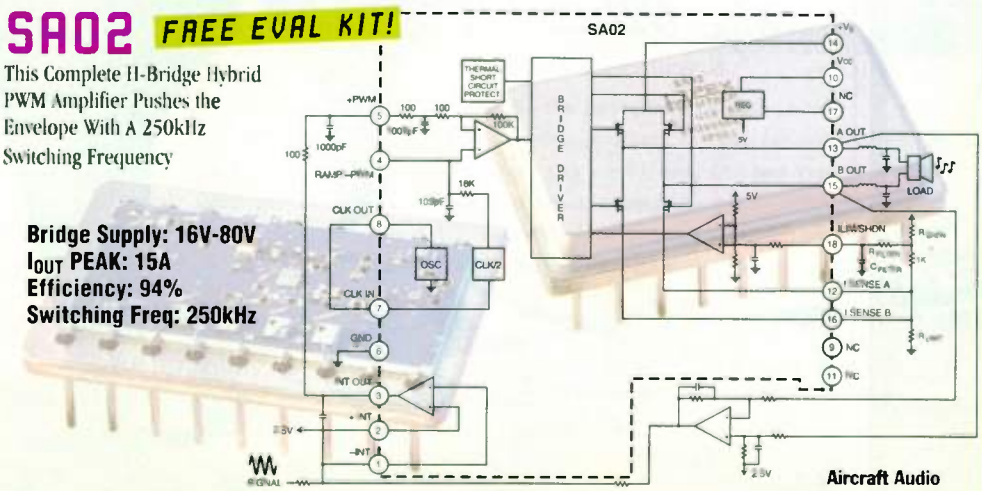

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[1] Free evaluation kits available with the single unit purchase of the following models: PA04, PA05, PA26, PA42, PA87, PB50/PB58, SA01, SA02, SA50, SA51. Limit 3 free kits per customer.

READER SERVICE 100

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Why Just A "V" Chip?

Ah, television, you can't live with it, and you can't kill the network executives. Although we don't watch much TV at home, the one or two hours that it's on at my daughter's day-care center ensures that she'll still get a snootful of what passes for American culture. Fortunately, Bob (our very own Mr. Mom) is very selective, alternately exposing the kids in his charge to Barney and ESPN. Since Bob is a rabid sports fan (as well as an excellent caregiver), I expect that Anwyn will soon be dispelling the ignorance of football and baseball that I've carefully cultivated over the years.

With the arrival of my new daughter, my concern over the *dreck* oozing into our homes has shifted from impersonal disgust to deeply personal outrage. While home sick one day, I surfed past Oprah and Geraldo to look at what was on the air for kids. Some of the stuff on Nickelodeon was excellent (actually better than most adult shows!), but for the most part, the spew from the screen was as bad or worse than the trash that permanently warped my own childhood. I was appalled at the celebration of violence, consumerism, and anti-social values, and that was only the commercials! It was so bad in fact, that it made me a V-Chip convert.

LEE GOLDBERG
COMMUNICATIONS

Free speech is a critical element of a free society, but so is the "off" switch on my radio, television, or computer. Heaven help us if the current onslaught of Big Brother-like laws and technology make it past the Supreme Court. We don't need some wacko congressman's idea of "communications decency" jammed down our collective throats. The V-Chip is little more than a sophisticated off switch to filter stuff we don't want in our homes without imposing our taste or morality on anyone else. My only disappointment is that big money managed to gut the rating system so that only part of the shows on the air will actually be rated, and even then, they will be tagged using calculatedly imprecise generalities.

We need an expanded ratings and screening system that will help keep the real offensive crud out of our homes while not dumbing down programming to the point where the only things allowed are "Gilligan's Island" reruns and Rush Limbaugh. I have some ideas for filtering criteria, and I'm sure you do as well.

•How about a "Z" chip? It would disable all home-shopping channels that refer to cubic zirconium, celebrity-endorsed hair appliances, and other useless products.

•While it may be nice, an "N" chip that filters out all negative and nonfactual political campaign material could erase up to 90% of the electoral activity in America.

•Russ Gerches, *Electronic Design's* sales manager, suggested we whip up a "DT" chip to shelter our kids from the "daytime television" shows, formerly known as soap operas. Great idea! I don't want Anwyn to assume that the morality portrayed in "General Hospital" or "Days Of Our Lives" bears any resemblance to acceptable behavior.

The same applies to the Internet. Rather than make a huge fuss about the content of cyberspace, we should be worrying about the incredible abridgments of our constitutional rights that are now taking place. One reason that we enjoy such a robust culture is that it is based on the free exchange of our ideas, even if it means putting up with bigots, hate-mongers, and other assorted cretins. One of the currently available plug-in "Web-Sitters" for your Internet browser could help shield your kids from the seamy side of the 'Net until they are old enough to decide for themselves. I hope that by the time Anwyn knows how to hack past the filtering software, she'll be able to talk with me about anything she encounters out there.

Meanwhile, I've decided to terminate our cable service. We'll just have to endure the hardships of books, music, crafts, and (occasionally) the fuzzy images that the antenna in our attic can snag out of the air. Who knows, we may have to talk to each other. What do you think? Write me at *leeg@class.org*.

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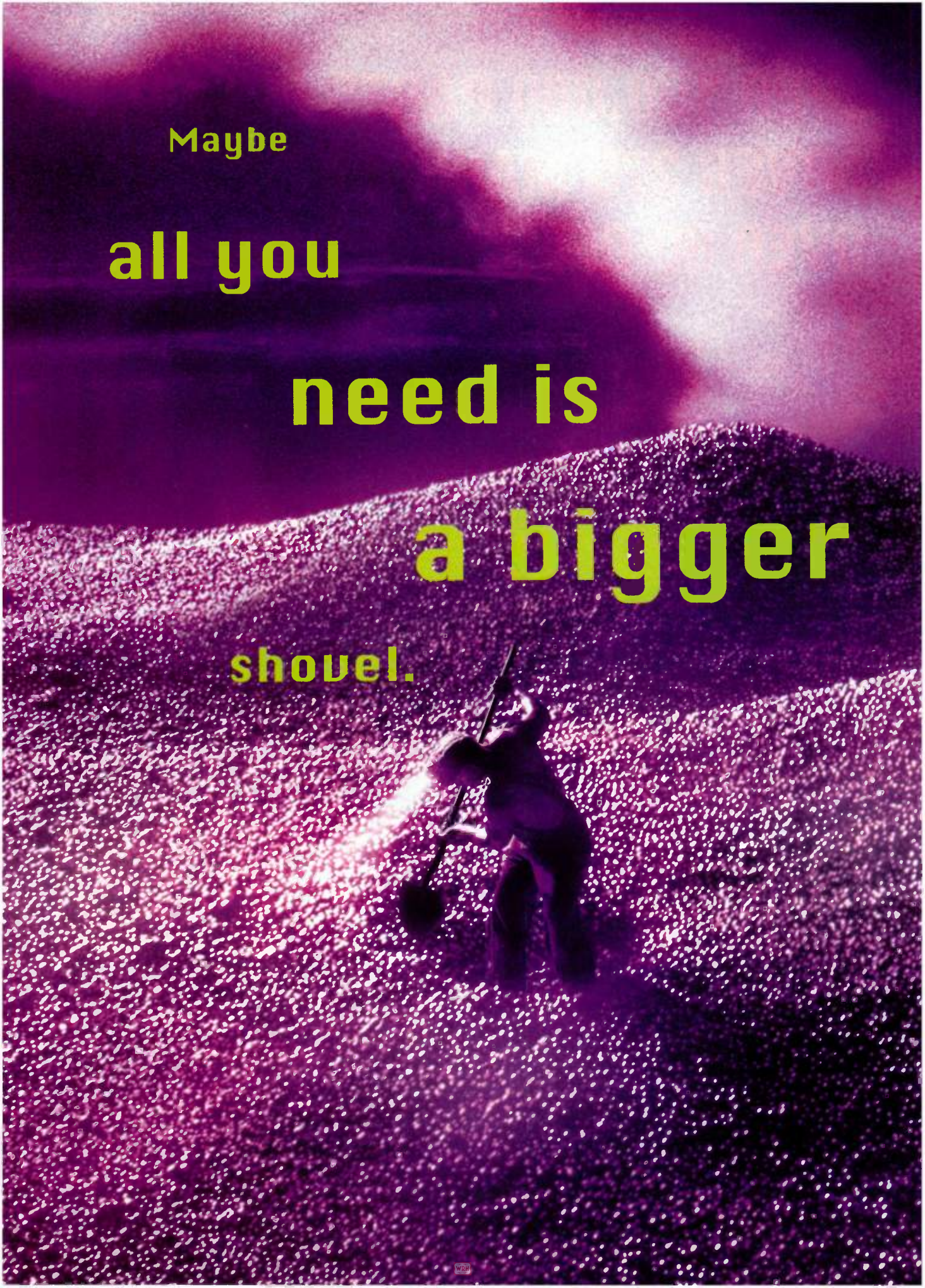
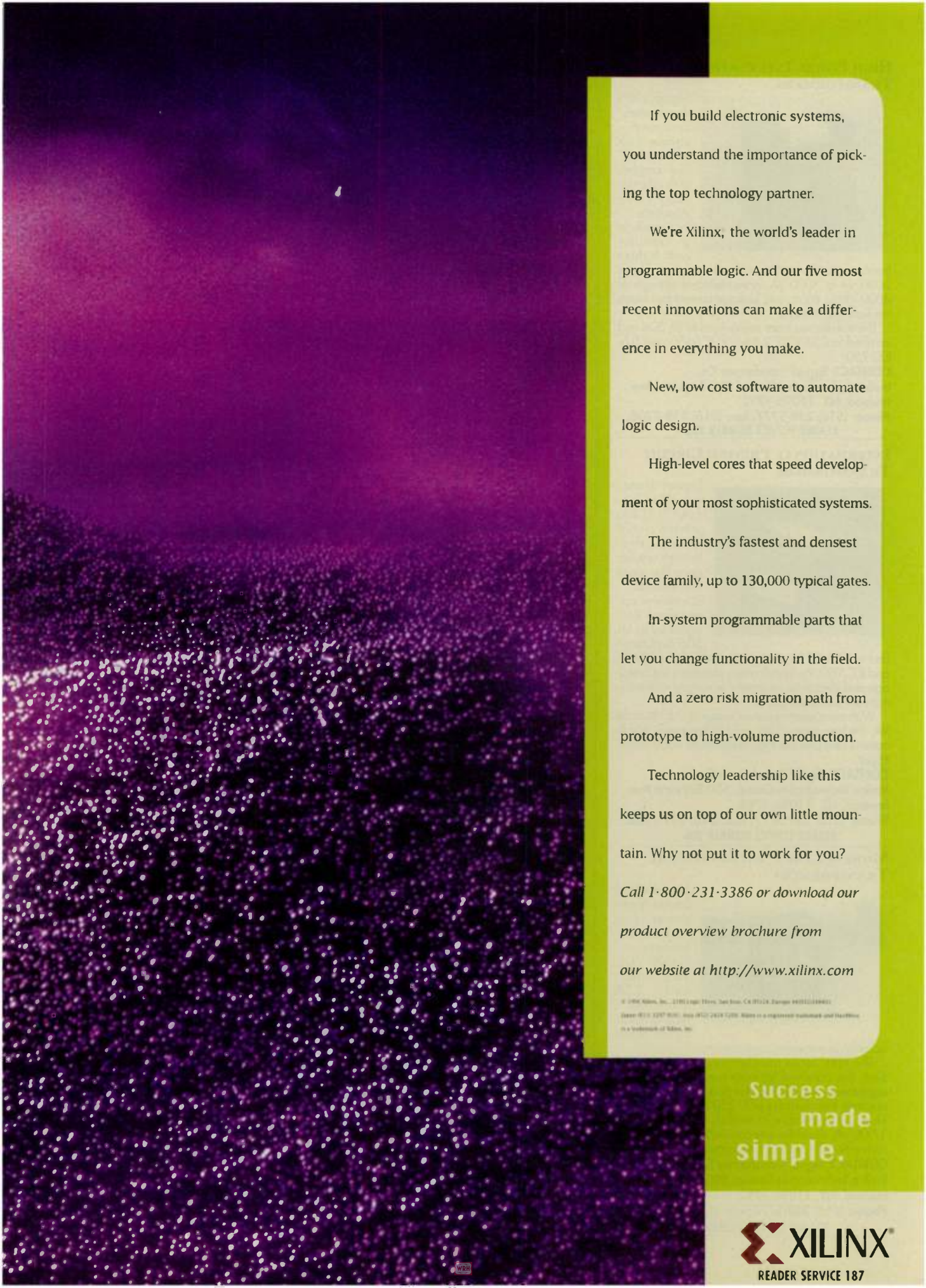

Maybe
all you
need is
a bigger
shovel.



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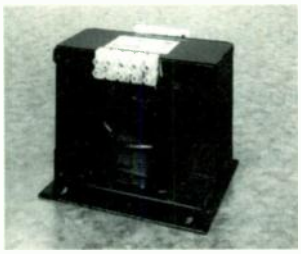
High Power International Transformers



Signal's HPI transformers incorporate unique coil construction that complies with international safety standards that results in a smaller and lighter transformer. The HPI transformers operate from 2000 VA to 3500 VA, have dielectric strength of 4000 VRMS Hipot, and leakage current that meets medical applications.

The transformers are recognized to UL 506 and certified to CSA C22.2 #66, VDE 0550 and TUV IEC 950.

CONTACT: Signal Transformer Co., Insilco Technologies Group, 500 Bayview Ave., Inwood, NY 11096-1792.
Phone: (516) 239-5777; fax: (516) 239-7208.
READER SERVICE NUMBER 205

International Printed Circuit Transformers

Signal Transformerís One-4-All™ (14A) printed circuit mount transformers are designed for use in international low power applications. Recognized to UL 506 and certified to CSA C22.2 #66, VDE 0805 / EN 60950, and IEC 950, the transformers also have the creepage and clearance necessary to comply with international safety standards.

With an operating power range of 2.5 VA to 56 VA, the transformers are used in low power applications and provide high isolation of 4000 VRMS Hipot.

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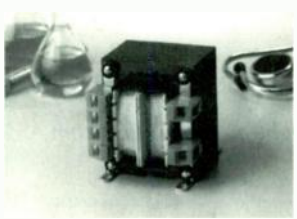

Signal's M4L Series high-power, isolation transformers satisfy UL, VDE, IEC, and CSA transformer requirements for low power isolation in numerous applications.

The M4L Series transformers comply with UL 544, the standard for both medical and dental equipment, and UL 506, the standard for specialty purpose transformers with 250 volt or less input. They are available in models from 300 VA to 1,000 VA, are extremely compact, and lighter than conventionally wound transformers.

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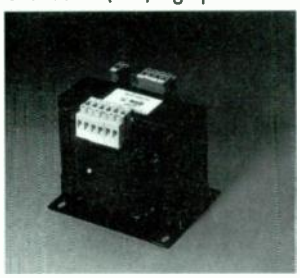
Multi-Purpose International Transformers

Signal Transformer's Multi-Purpose International Series (MPI) high-power transformers operate from 200 VA to 900 VA and feature higher volumetric efficiency than conventional 50/60 Hz transformers.



Featuring unique coil construction and winding methods, the MPI transformers have exceptionally good isolation of 4000 VRMS Hipot and low leakage current. They also have a 5 mil thick copper Faraday shield to reduce common mode noise. Faston/screw type shock-proof terminals are used on the series.

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READER SERVICE NUMBER 208

Standards Recommendations Proposed For System-Level HDL

In response to a System Level Design Workshop, sponsored by the Project Technical Advisory Board (PTAB) of the EDA Industry Council, a number of recommendations were set forth to help speed standards development for a new system-level design language. Today's hardware description languages (HDLs) are insufficient for the upcoming challenges presented by systems-on-silicon design flows.

For example, two of the more popular HDLs—VHDL and Verilog—were originally defined with discrete event simulation semantics. Since their inception, though, the need for a comprehensive description of design intent has changed substantially. Studies of current industry trends indicate that this problem will only get worse, creating a major bottleneck to future growth of the semiconductor and system electronics industries. The workshop grew out of the industry-wide need to identify key system-level design problems that face chip and electronic systems designers.

Among the specific recommendations made by the workshop attendees was the creation of a language that's coupled with extensions from today's current design languages, such as VHDL and Verilog, for continuity across the full design flow. They also recommended emphasizing formal semantics for standardized descriptions of system-level properties and constraints with the ability to support both operational and declarative methodologies. In addition, a high level of priority was given to the development of co-design support for embedded software mixed with hardware, stressing co-specification and partitioning for verification, and the need to follow up on the upcoming VHDL '98 revision to make sure it defines a clean interface to the new environment. For more information check out the group's web site at http://www.cfi.org/sld. *CA*

Light-Emitting Polymer To Be Made Available To Researchers

Researchers who want to explore the practicalities of light-emitting polymers can buy sample quantities of the Precursor PPV (polyphenylene vinylene) material developed by Cambridge Display Technology Ltd., Cambridge, England. The company holds a dozen or more basic patents on light-emitting plastics and its applications. (ELECTRONIC DESIGN, *January 8, 1996, p. 42).*

Marketing director Mark Gostick says he is now taking orders at $1000 for 200 ml of the material "This is sufficient to make quite a few displays for research purposes," he says. The material is supplied in solution ready for spin coating or screen printing onto substrates. Each sample comes with a data sheet that contains the details needed for purchasers to make working displays. Already a number of large corporations have taken up the offer. "We expect them to use the sample materials to gain confidence in the concept of plastic display technology," Gostick adds. "The translucent yellowish liquid is a good vehicle for polymer testing."

There are conditions attached to the sale. Gostick insists that purchasers sign a non-analysis agreement before the material is delivered, and that they not attempt commercial production without first negotiating a license. He stresses though that CDT doesn't plan to supply commercial quantities of the material, and is currently nearing completion of negotiations for the licensing of the manufacture of the LEP material by a "large chemicals corporation".

Lifetime has been increased dramatically. A year ago, this seemed to be a major problem with the technology with power on lifetimes of little more than 3000 being achieved. Now Gostick claims that lifetime has been tripled. Under accelerated testing conditions, driven at 3.3 V, and with a current density of 10mW/cm^2, unencapsulated devices have been in operation for more than 10,000 hours without showing signs of decay, he says.

Now Gostick says CDT is turning its attention to developing "high information content" displays including those able to emit a range of colors. For more information, go to the company's web site at http://www.cdtltd.co.uk, or call +44 (0)1223276351. E-mail is: mgostick@cdtltd.co.uk *PF*

Simulation Models Expected To Aid In B-2 Bomber Testing

As part of a $2 million, 14 month contract awarded by the U.S. Air Force Dept.'s Oklahoma City Air Logistics Center, Analogy Inc., Beaverton, Ore., will supply simulation models for use in the B-2 Stealth Bomber depot test and repair program. The company plans to employ its hardware description language, known as MAST, as the foundation for these models. The language is especially well suited to deal with complex, mixed-technology, mechanical and electrical circuitry, and can offer high model fidelity capabilities. Moreover, models written in MAST can be customized and reused.

Specific models being developed for the simulation and design of test programs for the B-2 Bomber's electronic systems include op amps, voltage regulators, ADCs, DACs, pulse-width modulators, analog switches and multiplexers. The simulation is intended to provide a better understanding of how the Bomber's electronic systems function and of their operational range. Faults are isolated without jeopardizing valuable Stealth Bomber components. For further information, contact the company at (503) 626-9700. *CA*

Trade Association Will Promote Mezzanine-Module Standards

With a charter to promote international open standards for mezzanine boards, the GRoupIPC-North America (GRoup-NA) was established as a branch from the parent organization, GroupIPC, which operates in Europe. The main goal of the initial organization was to provide a worldwide forum for the exchange of information on IndustryPack (IP) and PCI Mezzanine Card (PMC) technologies.

GRoupIPC-NA will promote market acceptance and the use of PMC and IP technologies; disseminate information about products, applications, and technical requirements that employ or affect IP or PMC technologies; and provide marketing and technical support to users, distributors, and manufacturers of related products. Promotion will occur through trade conferences, tutorials, and articles. Over 30 companies are already part of GRoupIPC-NA, including Digital Equipment Corp., Force Computers, GreenSpring Computers, Hewlett-Packard, IBM, Motorola, Spectrum Signal Processing, and Systran. For more information, contact the GRoupIPC-NA at (937) 427-9735, or on the Internet at http://www.GRoupIPC.com. *RN*

Individualized Laser Treatment Rids Port-Wine-Stain Birthmarks

Doctors faced with removing port-wine-stain birthmarks using a laser have had to estimate the laser energy and pulse length needed to successfully complete the task. However, results achieved from a four-year collaborative effort between researchers at the University of California at Irvine's Beckman Laser Institute and Medical Clinic and the U.S. Dept. of Energy's Lawrence Livermore Lab (Livermore, Calif.) eliminates the guesswork by individualizing treatments.

Port wine stains are birthmarks that occur when an excessive number of oversized blood vessels near the skin's surface. Approximately 12,000 Americans are born each year with these discolorations that range from light pink to deep purple.

Converting a computer code developed by Livermore electronics engineer Dennis Goodman, the researchers were able to improve astronomical imaging into a diagnostic tool. With that tool, doctors can pinpoint the precise laser parameters needed to remove port wine stains on an individual patient basis.

The diagnostic technique starts with a subtherapeutic laser pulse that is directed onto a patient's skin and blood vessels. An infrared camera system records images as the laser heats the skin's melanin (the material that gives skin its color) and the blood. As the laser heat flows back to the skin's surface, it helps identify the location, depth, and other data for the port-wine-stain blood vessels. This data, in turn, is converted into clinical images by Goodman's code. Only one sequence of measurements is needed for physicians to be able to obtain the data they need to treat individual port wine stains using Goodman's code. "This is particularly valuable because port wine stains vary not only from one person to the next, but from one location to another on the same patient," says Tom Milner, an assistant professor of surgery and optical physicist at Beckman. Goodman's code (program) generates images that permits the researchers to enter data about a stain and then determine how much laser energy is needed.

Another key element of the individualized treatments has been the development of a new laser to treat port-wine-stain patients. The laser delivers bursts of energy from a one-half thousandth of a second to 10 thousandths of a second.

Clinical trials using the complete three-dimensional diagnostic technique have started and will continue for about one year. For more information, contact Lawrence Livermore Labs at (510) 422-1100. *RE*

New Class Of Polymer To Boost Low-Cost MCM Manufacture

A new class of packaging materials derived from polymers of cyclic olefins is being developed by the MCM research area of the Georgia Tech PRC. According to Dr. Paul A. Kohl and Dr. Sue Ann Bidstrup, both of whom are faculty members at the School of Chemical Engineering, the unique properties of these polymers are characterized by a Tg (glass transition temperature) greater than 350°C, a dielectric constant of less than 2.4 to 2.6, a low moisture absorption of 0.1%, and good ductility.

The materials were modified to have excellent adhesion to commonly used materials such as silica and aluminum, while also fusing well with copper and noble metals like gold and silver. The polymers require no adhesion promoter or adhesion layer (e.g., titanium, tantalum, or chromium), and have been shown to remain as adherent films even after being placed in boiling water for two hours.

Sponsored by BF Goodrich and conducted by Bidstrup and a group of PRC graduate students, the results of the research are expected to "demonstrate utility in both semiconductors and packaging by offering superior performance over traditional materials, while reducing manufacturing cost," says Kohl.

For additional information, contact Georgia Tech's Dr. Paul A. Kohl at (404) 894-2893; or through the e-mail at paul.kohl@che.gatech.edu. Or contact Dr. Sue Ann Bidstrup at (404) 894-2872 ; e-mail: sue.allen@che.gatech.edu. *PM*

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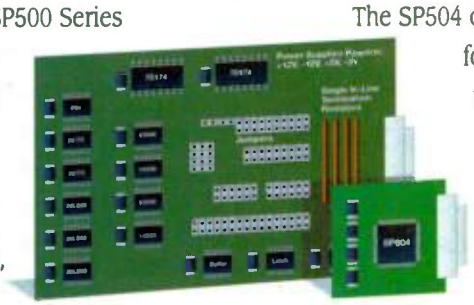
READER SERVICE 185

The Future of Network Communication in a Single Chip.

The SP504 is the newest release in the SP500 Series family of programmable serial interface transceivers from Sipex. Built on market experience, the SP504 includes such features as single resistor V.35 termination, programmable charge pump, and two new modes of operation, V.36 and EIA-530A.



The SP504 offers an efficient single chip solution for serial ports that require supporting multiple physical interface standards. Serial port designs for Frame Relay, X.25, and networking routers can be simplified by the SP504. The SP504 can be used in either DTE or DCE systems.

The SP504 supports the popular interface standards for Wide Area Network serial ports: RS-232 (V.28), RS-422 (V.11), V.35, V.36, EIA-530, or EIA-530A.

If Board Space, Power, or Performance are problems with your WAN port, the SP504 is the simple solution.

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READER SERVICE 174

Packaging Concept For Optoelectronic Components Eases Integration In Fiber Optic Systems

Assembling optoelectronic components to make high-speed fiber-optic transmission systems is complicated by the need to splice fiber "pigtails." A new packaging concept devised by a small British company seeks to ease the task with a push-fit coupling that more tightly integrates standard "butterfly" laser packages with its own unique modulator package.

The idea, developed by Integrated Optical Components (IOC) Ltd., Witham, Essex, initially provides more integration between the two critical components in a fiber system, the laser and the external light modulator. Adrian O'Donnell, IOC's chief scientist, explains that these components are currently interconnected with lengths of fiber known as "pigtails" for lightwave input and output *(Fig. 1)*. When they are assembled onto a printed-circuit board, the joining of the fibers is a highly skilled manual task that precludes the use of automatic component handling systems, slowing down the production process and adding cost.

O'Donnell says this problem is magnified with the introduction and wide-scale deployment of wave-division multiplex (WDM) transmission systems. In WDM systems, the capacity of an optical fiber is increased by using it to transport a number of independent lightwaves, each capable of transporting telecommunications traffic at rates of 2.54 to 10 Gbits/s. Each lightwave channel requires its own laser and modulator.

"WDM systems are currently being designed with as many as 16 channels per fiber," O'Donnell says. He points out that the International Telecommunication Union specifications allow for a maximum of 32 channels with wavelength separation of 8 nm. "In order that systems of that complexity can be manufactured in a practical and economic manner, there is a desperate need for a new way to assemble optical components to increase circuit-board packing density," he says.

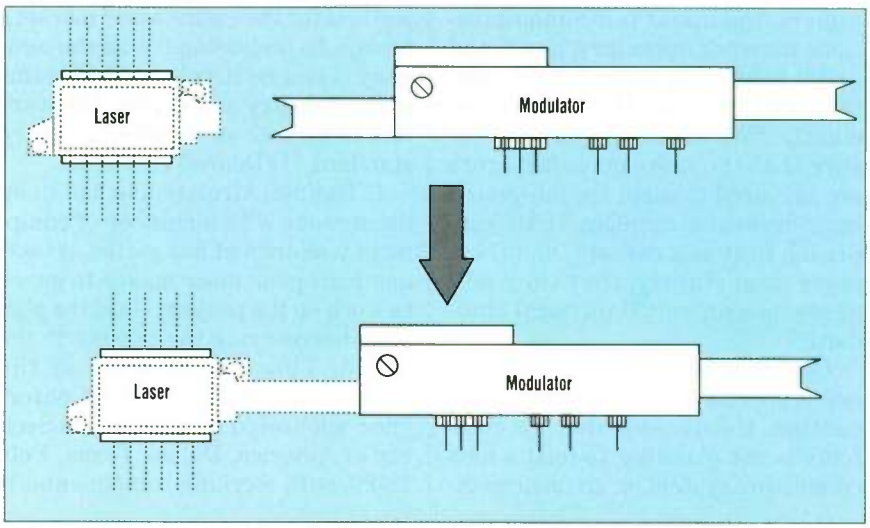
He explains that one suggested approach, including the laser and lithium-niobate modulator chips into the same physical package, is not a practical proposition at present. Lasers that can show equal efficiency at each of the wavelengths designated for high-density WDM systems are not available as of now. Therefore, they have to be carefully selected at the time of manufacture to cover a specific range of channels.

On the other hand, IOC's modulators are inherently wideband devices, so a single type of component can be used at any wavelength within the range covered by a WDM system. As a result, WDM system manufacturers need to be able to "mix and match" lasers and modulators to give optimum performance. That implies that the two components must be in separate physical packages.

The solution is to add a fixed optical connector ferrule to both laser and modulator packages *(Fig. 2)*. Although it may appear to be a relatively straightforward mechanical engineering problem, O'Donnell stresses that optical and commercial constraints combine to complicate the design.

The basic requirement is to ensure that the coupling can always be made accurately and repeatedly without signal loss. O'Donnell says he has identified two potential optical mechanisms for achieving this.

One approach is to use fibers carefully aligned within the ferrules so they physically butt together within the coupler. Another may be to use an intermediate micro-lens system at the physical interface within the coupling so that the two fibers don't physically touch each other. Each technique has its advantages and disadvantages, according to O'Donnell, who tends to favor the second solu-



2. Proposed mechanical configuration of an integrated laser modulator. The top shows the laser and modulator separated while the bottom shows both plugged into each other.

1. A conventional light modulator package with optical-fiber pigtails for interconnnection with a laser and to the transmission line.

tion at present.

But O'Donnell knows that any proposed solution can only be adopted if his customers, the WDM system manufacturers, and their customers, the major telecommunications network operators, like it and find it helps them make reliable systems and maintain them more efficiently. "We especially have to ensure that the laser manufacturers are prepared to adopt the integrated laser-modulator coupling (ILMC) approach first as a concept, and then, more importantly, that they will agree on a universal physical standard."

Conscious of the caveats, O'Donnell is approaching the industry with caution. He stresses that his company is not planning to foist a new connection system on an unsuspecting industry. While it claims to be one of the leading suppliers of lithium-niobate external light modulators (justified by a 1995-96 sales performance that equaled independent projections for the entire world market), he says he understands that the company is still relatively small in terms of the industry as a whole. "We want this to become an accepted industry standard," O'Donnell comments.

O'Donnell already has had deep discussions with a number of equipment makers and has gotten at least one European laser maker to agree to work on the project. Now, the plan is to demonstrate the concept to the world. This will be done at the OFC'97, the Optical Fiber Conference, sponsored by the Optical Society of America, Dallas, Texas, Feb. 18-20, with working components. If the idea is generally welcomed, then IOC could be manufacturing its modulators in coupled packages before the end of this year.

For the future, O'Donnell sees a great potential for a similar approach to the packaging of other components that are used to make multichannel 10-Gbit/s systems. In addition to the optical lightwave "carrier," the IOC's modulators also need to connect with "conventional" microwave devices that carry the signal that is to be impressed onto the lightwave.

For more information, contact Integrated Optical Components Ltd., 3 Waterside Business Park, Eastways, Witham, Essex CM8 3YQ; +44 (0)1376 502110; e-mail: adrian@intopt.com

Peter Fletcher

Low-Cost, Emissive Flat-Panel Display Challenges LCD And Plasma Schemes

Based on phosphors like those used in CRT displays, an emissive flat-panel technology developed by Telegen Corp., Redwood City, Calif., promises large-area displays (up to 40-in. diagonals) at manufacturing costs comparable to those of CRTs. And the glass vacuum container needed for the display is about half an inch thick, making the display a promising candidate for wall-hanging television sets or industrial/advertising displays.

The technology is based on a warm-cathode, high-vacuum approach that, unlike conventional CRT technology, does not rely on a multi-kilovolt anode potential or a shadow mask. Rather, the high-gain emissive display (HGED) employs an X-Y anode grid and a bias voltage of just 80 V. That bias voltage is applied to both grids to select the desired pixel location—the grid coordinate where the X and Y grids both have the 80-V potential. External high-voltage drivers provide the anode voltages.

Phosphors provide a light output of about 20 foot-Lamberts (ft-L) for the current prototype/proof-of-concept display. However, higher light outputs will be possible in future versions of the display. Contrast ratios for HGED panels can exceed 10,000:1—a much higher value than achievable with active matrix LCDs (40:1, typical) or field-emission displays or FEDs (100:1). Additionally, the display brightness will be controllable through a pulse-width modulation technique, which sets the amount of time that each pixel is turned on and off within each frame.

The pixels also respond quickly to address requests. Switching times are in the several-nanosecond range, allowing designers to drive the displays at high frame rates (180 Hz and higher). The high frame rate, in turn, would allow designers to employ a sequential scan system to produce fully-saturated color displays that have simpler control circuits.

In the frame-sequential approach, the three colors are interleaved on a frame-by-frame basis. With this approach and a 180-Hz frame rate, each color paints 60 full frames, yielding an effective frame rate of 60 Hz. This rate is more than sufficient to handle video and graphics.

With currently available lithography and manufacturing technologies, pixel sizes of 0.3 mm are easily produced, and sizes of 0.2 mm and smaller are possible. Subsequently, HGED resolution can pack as many as 14.7 million pixels on a 13-in. diagonal display. The high pixel resolution of the HGED also promises much sharper images, even when compared to CRT-based systems.

Currently, Telegen has created a proof-of-concept 6-in. diagonal monochrome/gray-scale display that operates at 180 frames/s. It has fabricated a larger-area color display. The 6-in. unit consumes about 4 W of power, while a 14-in. color display would consume about 25 W. These high power levels would, in many cases, rule out the display for use in portable systems. However, the panel technology would fit nicely into applications such as desktop computer systems as a CRT replacement.

Manufacturing overheads also are much lower than with other technologies. The cost to build a full-sized HGED manufacturing plant is less than $50 million, according to company officials. That figure is less than a tenth of the cost for a plant for FED or active-matrix LCD production. The company estimates it will take another 18 to 24 months to prepare production facilities to mass-produce the display.

For more information, contact Jessica Stevens,Telegen's president and chief executive officer at (415) 261-9400.

Dave Bursky

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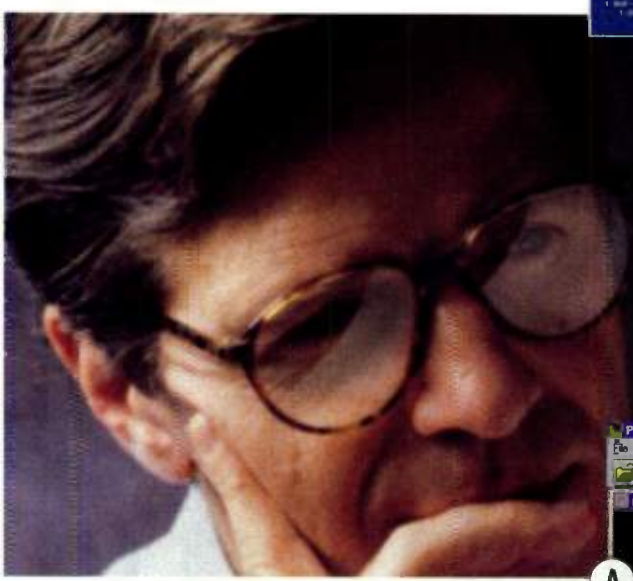

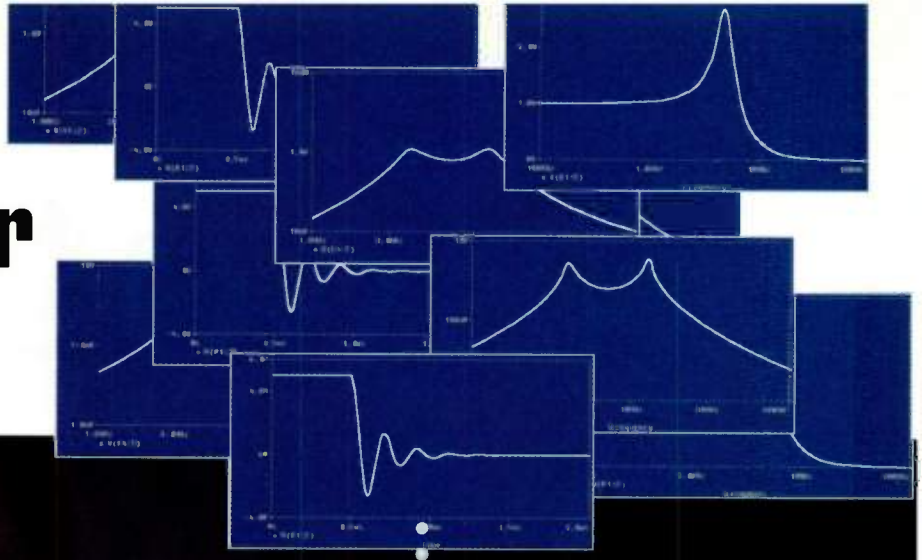

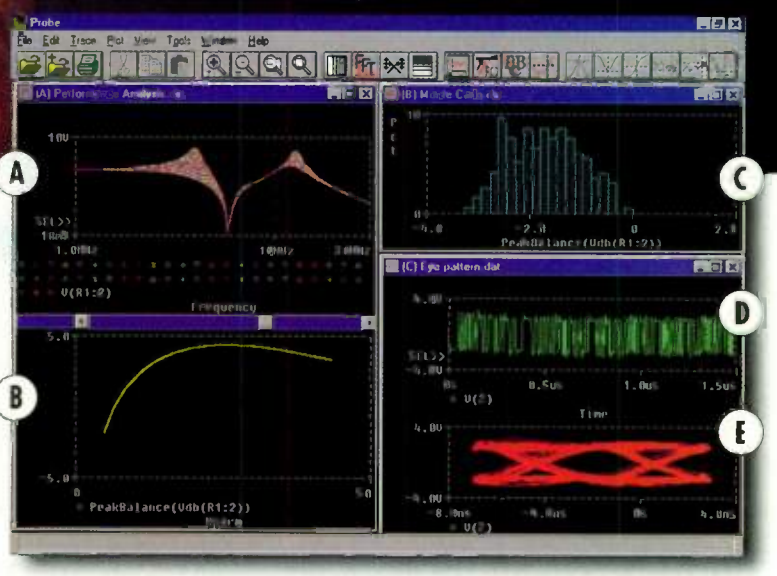

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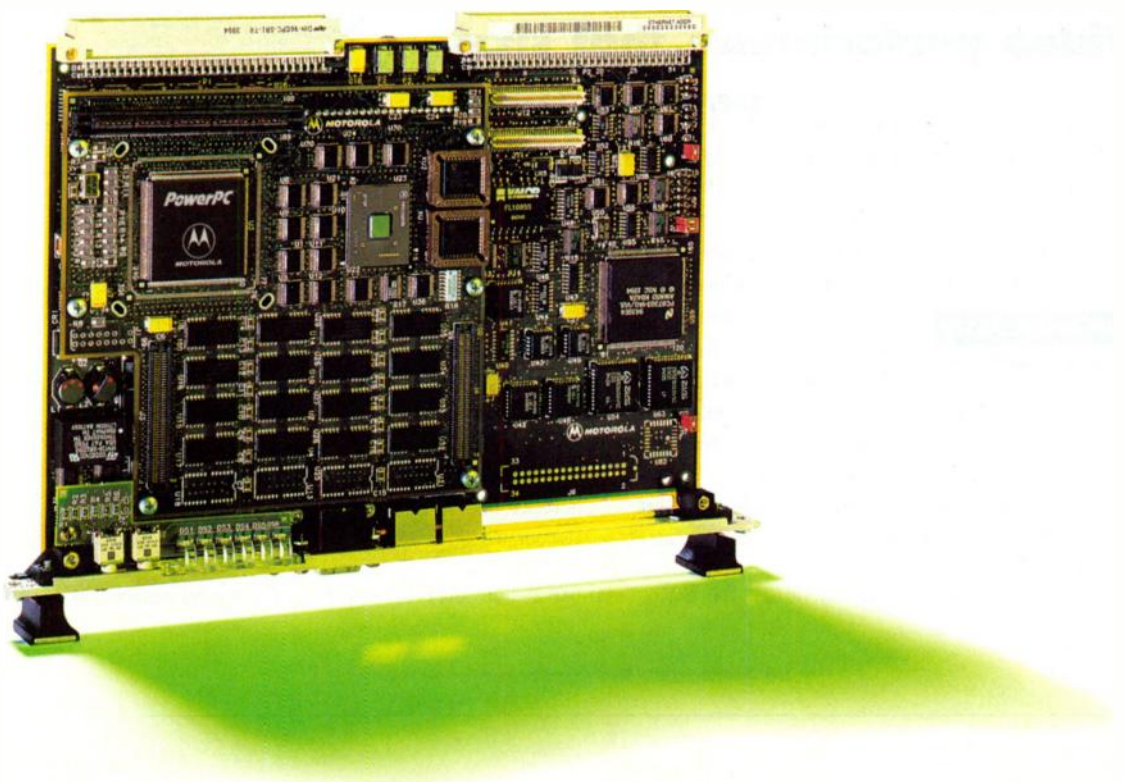

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TECH INSIGHTS

A review of developments at the 1997 ISSCC

ISSCC'97: A Hallmark Year Of Abundance And Breakthroughs

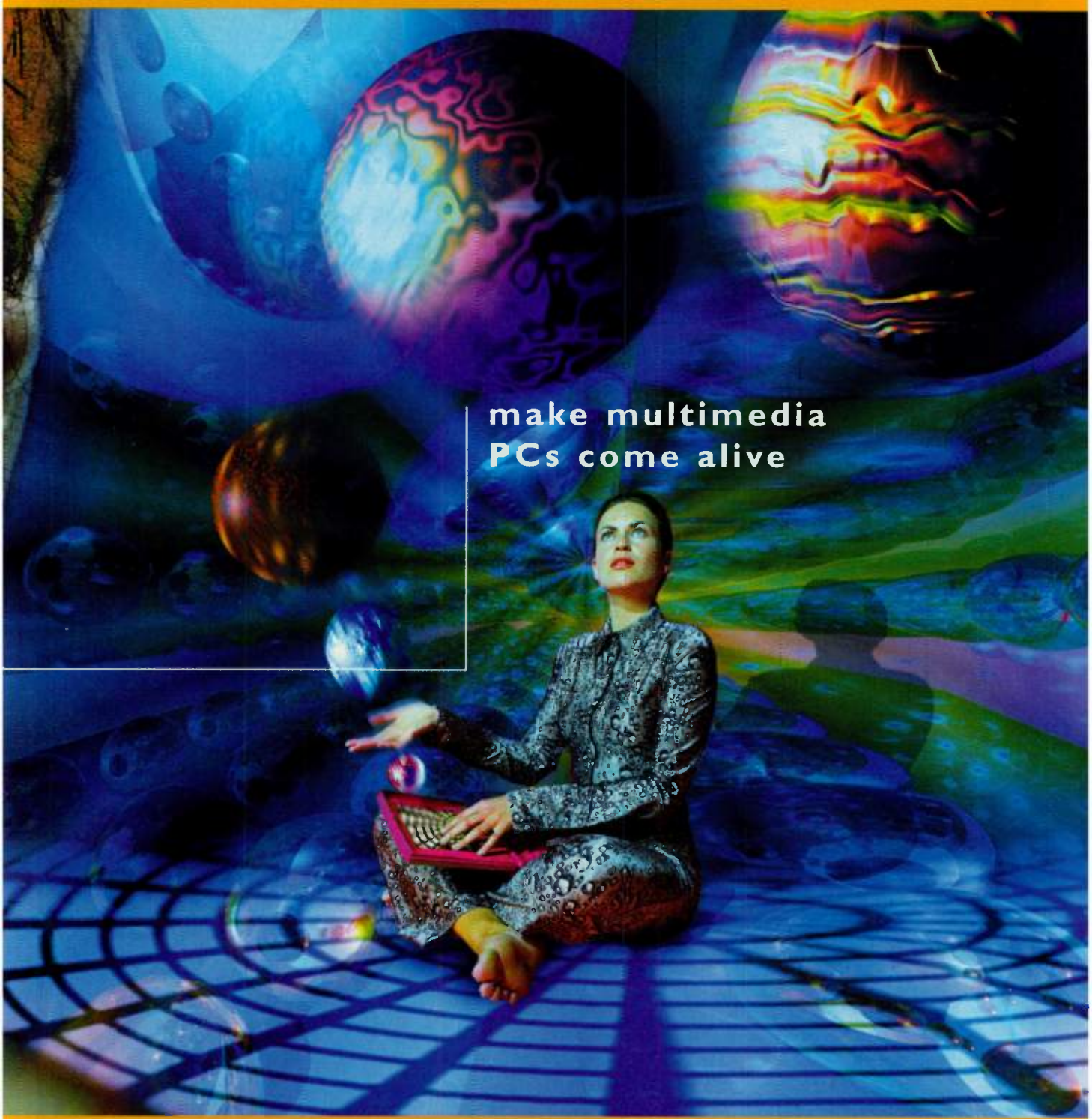
Dave Bursky

Every year, presentations at the IEEE International Solid-State Circuits Conference seem like they just can't get much better, and this year's set of papers is no exception. At the San Francisco Marriott Hotel earlier this month, the conference hosted its largest number of papers in a good many years—over 160 breakthrough presentations, not counting evening panel discussion sessions and tutorials and workshops.

Multimedia technology in its various forms was the main theme for the conference, and it was featured as part of most of the opening plenary presentations, as well as throughout the technical papers. Presentations took on many forms, from the communications technology needed to transfer MPEG data streams from satellites to TVs, to the digital processors and ADCs needed to transform the video and audio streams into digital data or back into analog form, to the memory subsystems needed to store the data. Roughly half the papers at this year's ISSCC can be thought of as multimedia-related. Of course, there are also many other topics incuded in the conference, sensor technology, new emerging quantum technologies, and elemental design techniques for low-power analog and digital circuits.

In the next 20 pages you will find excerpts and highlights of a majority of the papers presented at ISSCC. The discussions are roughly divided into five sections, collecting papers from various sessions and grouping them into themes—Analog Technology (analog circuits, filters, communications-related circuits), Real-World Interfaces (ADCs, sample-hold circuits, etc.), Communications Technology (satellite transceivers, wireless, optical, LANs, and ATM), Digital (microprocessors, memory, image processors, etc.), and Sensors (imaging and sensing circuits). Although the following reports barely delve into the details presented in the full papers, they capture many of the highlights of the papers and provide some perspective as to their relative significance.

If you would like a copy of the full proceedings and supplementary slide set (available in printed or CD-ROM formats), contact the IEEE on their ISSCC website at http://www.isscc.org, or John Kennedy at the IEEE office in Palo Alto, Calif., at (415) 494-7115; fax (415) 494-6509.



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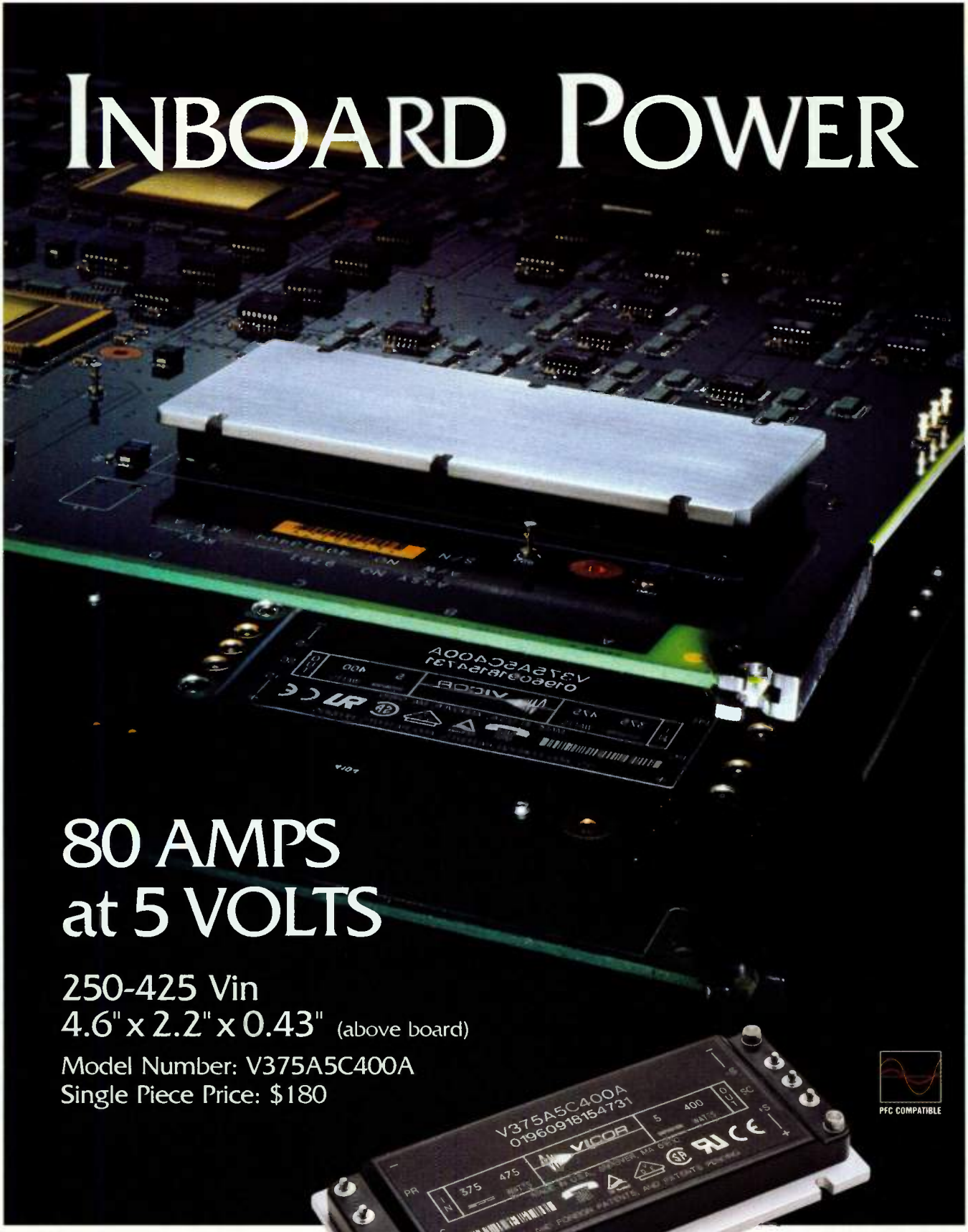

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Innovation Continues To Thrive As Circuits Get Denser And Faster

Digital Advances Lead To Single-Chip MPEG-2 Encoders, 600-MHz RISC CPUs, and 4-Gbit DRAMs.

Dave Bursky

SPECIAL REPORT

High-performance processors and large memory chips have typically been the highlight of the digital portion of every ISSCC program. This year's program was no exception, with a full session on multimedia signal processors, two sessions on advanced RISC processors, and a large session on dynamic RAM technology that included the largest DRAM to date—4 Gbits on one chip. Additional sessions investigated areas of specialized-processing sub-blocks and fundamental technologies for next-generation digital ICs.

It wasn't that long ago that the circuitry needed to encode a video signal into an MPEG-2 data stream required a rack-size cabinet. At this year's Session 16, three single-chip MPEG-2 encoders, capable of main-profile@main level or main profile@studio profile (MP@ML or MP@SP) encoding, were presented.

In paper 16.1, designers from the Philips Research Labs, Eindhoven, The Netherlands and Philips Semiconductor Systems Laboratory, Hamburg, Germany, collaborated to create a chip they dubbed I.McIC. The chip is an MPEG-2 video encoder that delivers MP@SP data. The chip employs about 4.5 million transistors to compress the video to a "good" quality signal data stream of about 5 Mbits/s and to an "excellent" quality data stream at 10 Mbits/s. Noise in such compressed data streams was an issue, so designers incorporated special noise-reduction circuitry on the chip to improve the image quality.

The chip architecture is divided into a front-end, back-end, memory interface, macroblock compressor, application-specific instruction-set processor, and control block. These sections communicate with each other through FIFO buffers in a dynamic data-flow fashion. The execution of a sub processor stops when it needs data from a FIFO buffer (data not available), or when it writes data to a FIFO that is full. Noise reduction is performed by a recursive, motion-compensated spatio-temporal noise filter. This noise filter is used to improve both the coding efficiency and the picture quality when less-than-perfect video material is processed.

Capable of full MP@ML encoding, a single chip, detailed by NEC Corp., Tokyo, Japan, in paper 16.2, concentrated on reducing chip power consumption so that all the functions could be integrated and housed in a low-cost package. The 3.1-million-transistor chip they developed consumes just 1.5 W thanks to the use of an adaptive, search-area motion estimator and demand clocking. The encoder contains the first and second search units and an embedded cache memory. The cache memory comprises two dual-port and two single-port memories that function as a pseudo 8-read/1-write memory. This design reduces, by 80%, the bandwidth needed by the motion estimator to transfer data to external synchronous DRAMs, keeping the operating frequency of the SDRAMs down to 81 MHz.

Plenty of on-chip parallelism is the key to a 2.2-Goperation/s video DSP chip described by Sony Corp., Tokyo, Japan, in paper 16.3. Although the chip performs MEPG-2 encoding with MP@ML, it does require separate support for the motion-estimation computations. On the chip is a dual-RISC controller, a vector processing unit, a variable-length coder/decoder, and various address generation and control blocks.

The high-definition television (HDTV) market is another challenge for video processors. The higher resolution and signal bandwidth will require even more horsepower to be incorporated on a chip. Matsushita Electric Industrial Co. Ltd., Osaka, Japan, in paper 16.8, detailed a 23-Goperation/s programmable systolic-array processor. Packing about 4-million transistors, the processor operates at an internal clock rate of 129.6 MHz and consumes about 7 W from a 3.3-V supply. Three such chips would be required to perform HDTV (MUSE) signal decoding in real time.

On each chip, 90 video-processing elements (VPEs) are configured into a systolic array so

that data can constantly be supplied to all VPEs, eliminating various data-transfer overheads. Each VPE has a simple structure that consists of a data processing block, a network control unit, instruction registers, and a decoder.

A simple approach to real-time compression of motion pictures employing vector quantization (VQ) was also proposed by Rohm Corp., Kyoto, Japan, in paper 16.9. The VQ approach uses an input vector containing 16 elements of 8-bit numbers, matched with 2048 template vectors within a 540 ns period. That would allow a full-color image of 640-by-480-pixels to be encoded in less than 30 ms.

The company also developed a new program for generating the code book needed for the templates. The software, universal self-organizing mapping (μSOM), was developed by modifying and optimizing the Kohonen's self-organizing map. A general-purpose code book of 2048 template vectors has been created, and can be applied to any kind of picture.

High-performance CPUs and building blocks were described in Sessions 10, 14, and 25. Running at the highest internal clock rate for a 64-bit CPU, a 600-MHz version of the Alpha processor, developed by Digital Equipment Corp., Hudson, Mass. (paper 10.7), incorporates dual 64-kbyte caches to deliver an estimated throughput of 40 SPECint95 and 60 SPECfp95. Designers at DEC employed a CMOS process with six levels of metallization and 0.35-μm minimum features, to pack the processor's 15.2 million transistors on a 17-by-18.9-mm chip. When powered by a 2-Vpower supply the CPU dissipates 72 W.

The high speed typically would cause a significant amount of switching noise but, designers dedicated 198 pins of the 587-pin package to V_{DD} and V_{SS} connections. Furthermore, designers mounted a 1-μF capacitor to the surface of the chip to augment the on-chip decoupling included beneath routing channels. The capacitor helps manage the power-supply noise components near the chip/package supply-loop resonant frequencies.

In addition to the high clock speed, the processor achieves its high throughput by performing out-of-order execution. Out-of-order execution is achieved by first reading four instructions, plus a next-address pointer from the instruction cache during each fetch cycle. The next-address pointer predicts the address of the subsequent four instructions and indexes the cache in the next cycle. In parallel, a branch predictor resolves the prediction.

Fetched instructions are dispatched to integer/memory and floating-point pipelines, issued and executed out of order, and retired in order. During dispatch, register specifiers are renamed to eliminate false dependencies by a pair of 12-port register mappers.

With a clock speed of 550 MHz, another version of the Alpha processor developed by Mitsubishi Electric Corp., Itami, Japan, in conjunction with DEC, includes on-chip support for MPEG-2 encoding and decoding through the addition of 13 instructions to the architecture (paper 10.6). The chip can deliver a 30-frame/s DVD playback stream with stereo-quality audio, in addition to performing normal data processing tasks. Instruction-set extensions include operations for motion-video estimation. They are fully pipelined and able to execute with a two-cycle latency. Caches on this chip are much smaller than on the other Alpha chip—a 16-kbyte direct-mapped instruction cache and an 8-kbyte dual-ported data cache.

A biCMOS process, developed for use on a PowerPC-compatible, superscalar processor allows the processor to operate at clock rates of 533 MHz and beyond. Detailed in paper 10.1, the biCMOS chip was developed by Exponential Technology Inc., San Jose, Calif. to deliver more than double the throughput of currently available CMOS PowerPC chips.

On the chip is a three-way-superscalar architecture that can issue one integer or floating-point, one load/store, and one branch instruction in parallel. A six-stage pipeline (fetch, decode, address calculation, cache access, miss detection, and write) executes the instructions. To support the high clock rates, designers kept the level-1 caches small, 2 kbytes each. The caches were direct-mapped to access their data quickly, 0.8 ns. Also, a 256-entry, branch-prediction table is coupled with the instruction cache.

Pushing the 64-bit, Version 9 SPARC architecture to new perfor-

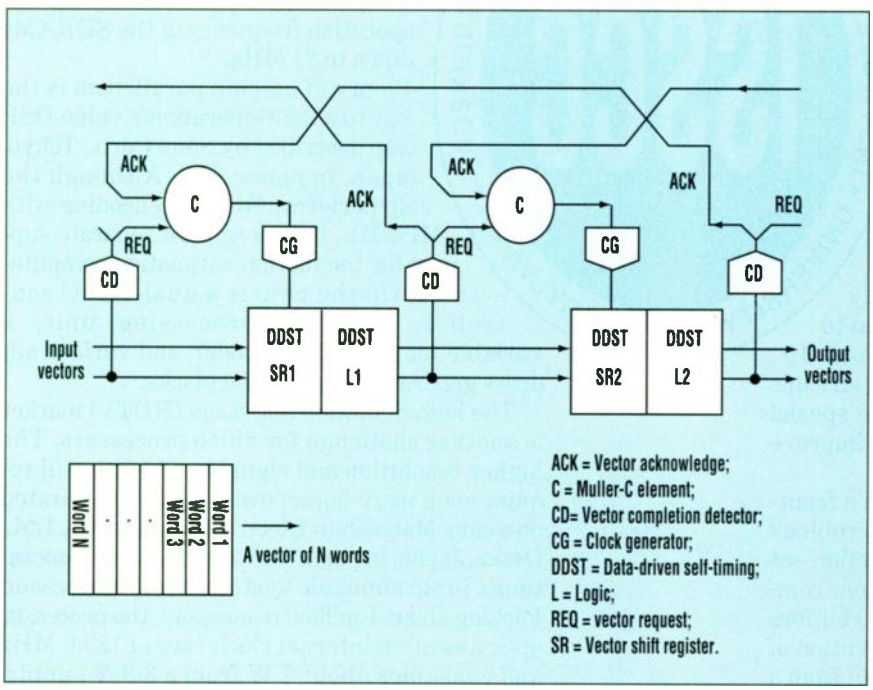

Fig. 1. Able to operate at a data rate of 20 Gbits/s, this self-timed vector processor, developed jointly by the University of California at Berkeley, Yokohama National University, and IBM, employs a data-driven, self-timing scheme--represented by the DDST blocks-- to implement a superconducting, single-flux quantum logic and memory circuit.

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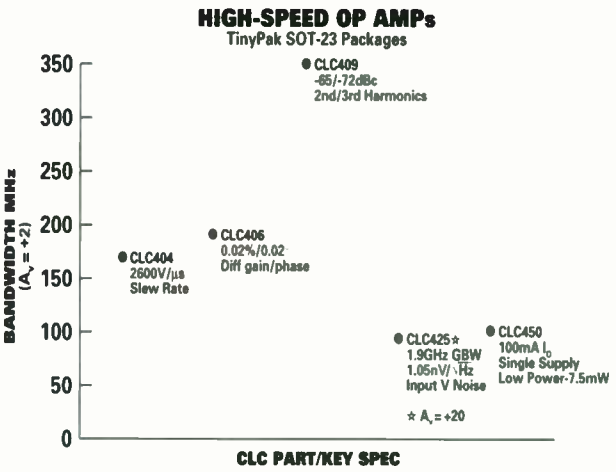

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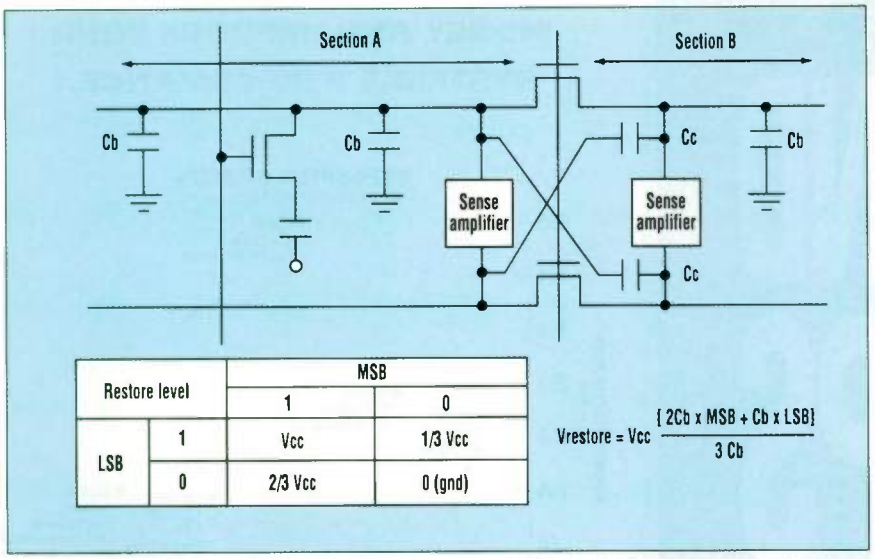

Restore level		MSB	
		1	0
LSB	1	Vcc	1/3 Vcc
	0	2/3 Vcc	0 (gnd)

$$Vrestore = Vcc \frac{[2Cb \times MSB + Cb \times LSB]}{3\,Cb}$$

Fig. 2. To perform the sense and restore operations required in its 4-Gbit DRAM memory cells, NEC designers created this simple, two-section sense and restore circuit. The two sections of the bit lines are connected by transfer switches that allow two bits to be stored in each memory cell by detecting the half-Vcc and either Vcc or Ground levels at different stages in the read cycle.

mance highs, designers at Sun Microsystems Inc., Mountain View, Calif., have upped the clock rate to 330 MHz and enhanced the memory subsystem of the 4-way superscalar architecture. Some of those improvements were made possible by moving the design to a 0.35-µm CMOS process with five levels of metal interconnections. That design allows the chip to shrink to just 12.5 mm on a side and consume less than 30 W when powered by a 2.5-V supply.

Papers 10.4 and 10.5, detailed the next-generation Pentium/Pentium-Pro processors that include the multimedia instruction extensions (MMX). From Intel Corp., Santa Clara, Calif., were details of a 300-MHz CPU that packs 7.5 million transistors on a 203 mm^2 chip. The chip has separate data and instruction caches of 16 kbytes each. The chip also features a dedicated L2 cache bus with source-synchronous clocking, supporting various external cache configurations.

A five-level-metal process was selected by designers at Advanced Micro Devices Inc., Milpitas, Calif., for their 8.8-million transistor, x86-compatible CPU with multimedia extensions. Dual 32-kbyte caches provide more on-chip memory than the Intel CPU offers, and account for most of the difference in transistor count.

Dual 64-kbyte, two-way, set-associative caches are a key feature of a 200-MHz PA-RISC processor described in Session 25. Developed by designers at Hewlett-Packard Co., Fort Collins, Col., the 32-bit processor employs a simple, two-way superscalar architecture. The combined resources allow the chip to deliver a throughput of 7.75 SPECint95 and 7.56 SPECfp95 when running in a 160 MHz system.

Moving to an eight-way, set-associative cache architecture, but halving the cache sizes to 32 kbytes each, a superscalar version of the PowerPC processor developed by IBM Corp. and Motorola Inc., both in Austin, Texas, runs at a clock speed of 250 MHz. The architecture, described in paper 25.2, includes an integrated L2 cache controller, six execution units, and dynamic power management circuits that can trim the operating power to about 5 W when the chip is powered by a 2.5-V supply.

Examining pieces of the CPU architecture, papers 25.3, 24.4, 25.4 and 25.5 detail two new cache designs; a compact 54-bit multiplier; and a 1-GHz, 64-bit datapath, respectively. The store-barrier cache described in paper 25.3 by IBM Corp., Microelectronics Div., Essex Junction, Vt., provides a 32-entry, two-port architecture that dynamically predicts and reduces load/store hazards. The technique is similar to Branch prediction, but when applied to load/store hazards, it can be used to delay a load operation that is later in the program order. Once the specified store is completed, the corresponding load can continue.

A dual-port cache macro that accesses in 2 ns was the result of developments at Hitachi Ltd., Tokyo, Japan. The macro, detailed in paper 24.4, is a dual-port, 16-kbyte memory organized as a 512-word-by-256-bit array. It can perform read and write operations simultaneously in the same cycle at 285 MHz. Two addresses are sent to the cache continuously in a single cycle. If the same addresses are accessed in a single cycle, the previous data of the cells are sent to the read bus and the write data are written to the cells. That technique allows the cache to respond to a store instruction in a pipeline in one stage, without using a hit signal.

High-speed in the data path was the goal of researchers from Toshiba Corp., Tokyo, Japan, when they developed an early-completion-detecting ALU that can operate in datapaths that clock at 1 GHz. Also implemented in a 0.25-µm CMOS technology, the data-path design exploits the fact that in asynchronous systems, the longest path for individual operations of a logic circuit is generally much shorter than a critical path of the circuit.

Experimenting with single-flux quantum technology, an advanced research project presented in Session 7, details a 20 Gbit/s, self-timed vector processor. Developed by researchers from the University of California at Berkeley, Yokohama National University, Japan, and IBM Corp., Austin, Texas, the work is based on superconducting single-flux quantum logic and memory. The ones and zeros are represented by the presence or absence, within a timing window, of a quantized-picosecond voltage pulse (one single-flux quantum, SFQ).

To implement a functional block, researchers created a self-timed vector processor that employs an asynchronous-timing scheme. Data-driven self-timing (DDST) registers remove global-clock-distribution problems and accommodate process variations. Data is processed by deep-pipelined, DDST logic circuits that treat the data

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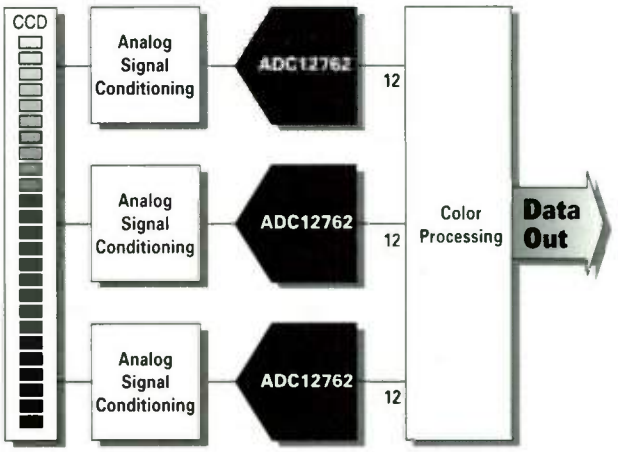

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as a vector that is composed of certain number of words *(Fig. 1)*. That vector is stored in a vector-shift register. Logical ordering is achieved through the use of block-level vector handshaking (vector-request and vector-acknowledge signals).

Performing the computation are Mueller-C elements. These elements are blocks that perform a logical AND of the input acknowledge and request signals, and generate an output SFQ pulse to initialize the clock generator. A 4-bit vector-completion detector is implemented by serially connecting two SFQ T-flip-flops, forming a 4-bit binary counter that provides a pulse for every four SFQ pulses.

Multivalued logic is just the basis on which designers at NEC Corp., Tokyo, Japan, have relied to craft the industry's largest DRAM (described in Session 4). The 4-Gbit memory chip, described in paper 4.6, actually contains 2 Gcells, but each cell can store two bits. Such a scheme has already been proposed for flash memories, but this is the first implementation in a dynamic memory structure. Fabricated in a 0.15-μm triple-well CMOS technology, the cell area comes to just 0.23-μm^2. This yields a rather large chip area, 986 mm^2.

To handle the four-level storage, the sense and restore scheme developed by NEC starts with two bit lines that are separated into two sections by transfer switches. This design sets up a capacitance ratio of 2 between section A and section B *(Fig. 2)*. Bit lines are precharged to the half-V_{cc} level, and transfer switches are ON during a standby cycle. In an active cycle, a word line is selected, and the charge stored in the cell is transferred to the bit line. Then the transfer switches turn off, and the bit lines are isolated. Subsequently, the sense amplifier in section A is activated, and the bit lines are driven to Vcc and ground, depending on the stored data.

The amplified data is the most-significant bit of the stored data, because the reference level is half V_{cc}. The MSB is transferred to the other bit lines through a crosscoupled capacitor, and changes the bit-line level for subsequent least-significant-bit sensing. Then the sense amplifier in section B is activated and the LSB is sensed. Finally, the transfer switches turn on, the charge on each bit line is shared, and the read-out data is restored to the memory cell.

High-performance synchronous DRAMs were the subject of paper 4.5. Designers at Fujitsu Ltd., Tokyo, Japan, detailed the use of an on-chip, register-controlled, delay-locked loop to trim clock access time to 1 ns in the memory timing. The RDLL structure keeps the DRAM stable versus temperature, voltage, and process variations.

The RDLL consists of a variable-delay generator with a logic-gate chain, a shift register for indicating the optimal tap point in the chain, a phase comparator for comparing the internal clock and the external clock phase, and a set of replica circuits for simulating a delay in the internal clock path *(Fig. 3)*. The replica circuits include an output buffer with a dummy capacitance and a loop circuit that automatically tracks the external clock. Thus, data outputs coincide with the rising edge of the external clock and are independent of the ambient temperature and process parameters. One drawback to the RDLL approach, it has a comparatively long lock-on time (100 cycles after the power-on sequence) needed to adjust the delay tap. However, it should not pose a serious problem in terms of system operation.

With large memory chips, one time-consuming operation is testing the memories. To circumvent that problem, designers at Oki Electric Co. Ltd., Hachioji, Japan, described in paper 4.4, an on-wafer, built-in, self-test scheme that can perform failed-bit searches for 1-Gbit DRAMs at rates of up to 200 Gbits/s.

The approach they developed includes a 4-kbit very-long-word bus and on-wafer test management units to probe the memory arrays. This approach shortens the wafer test time to less than 1/100 the time required for bit-by-bit testing. The test-management unit includes a failed-address aligner circuit that converts a transferred 4-kbit word into two streams of 10-bits-by-16-words of failed-address data.

Large blocks of DRAM are forming highly integrated systems on a chip that can take advantage of wide, on-chip buses, and the higher-memory density possible with DRAM over SRAM memorycells. In paper 4.1, designers at Texas Instruments Inc., Dallas, Texas, and Miho, Japan, described an innovative DRAM architecture that forms the heart of an embedded-DRAM module that can be integratred and merged into a logic process.

The DRAM employs a dual-sense-amplifier array that eliminates the penalty imposed with synchronous-DRAM architectures. Two sense-amplifier arrays, SA1 and SA2, are available for one memory array. A bank boundary, a data accessible/inaccessible border of the sense-amplifier array, does not exist in the new approach. Any loca-

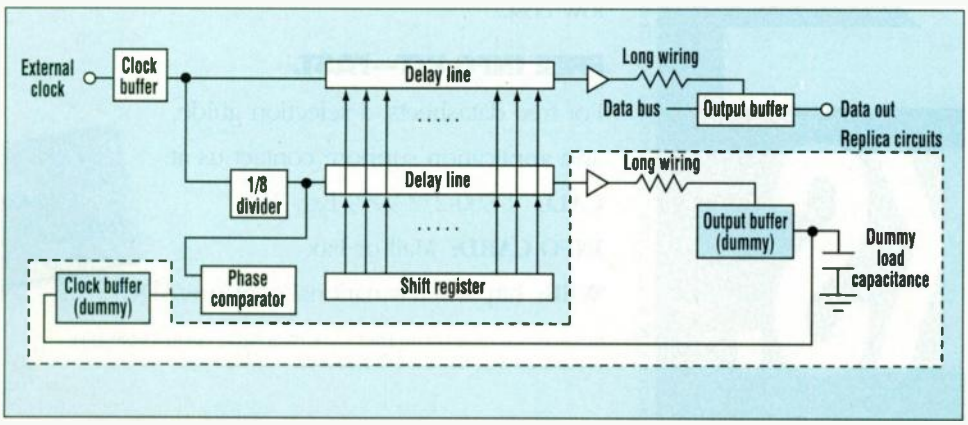

Fig. 3. A register-controlled, digital-delay locked loop or RDLL developed by Fujitsu to improve synchronous DRAM performance, employs a shift register and replica circuits to set the delay tap on the delay-locked loop. This design allows automatic optimization of the proper delay and independence from small changes in ambient temperature, supply voltage, and process parameters.

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tion of the memory array can be accessed by both SA1 and SA2. While one sense amplifier array is active the other is being precharged. Once data on the addressed page is transferred from the memory array to SA1 (or SA2), the memory array is disconnected from SA1. This arrangement allows precharging the memory array and preparing it for the next cycle.

In paper 14.1, researchers at the Electrical Engineering and Computer Science Department of the University of California, Berkeley examined various architectural approaches for CPU chips with wide memory buses and vector processing. The theoretical-vector processor, using a 0.18-µm DRAM process and occupying about 600 mm^2, could integrate 16-multiply-and-add units, running at 500 MHz. The processor also has 16, 1024-bit-wide memory ports running at 50 MHz, yielding a collective throughput of 100 Gbytes/s of memory bandwidth. Popular algorithms such as Linpack could execute at 8 GFLOPS, about five times faster than the Cray T-90 vector supercomputer.

One more practical example, presented in paper 14.3, details the forthcoming design of a parallel processor that combines 256 Mbits of DRAM and four 32-bit RISC processors. Developed by researchers at the Computer Science and Communications Engineering Department of Kyushu University, Fukuoka, Japan, the parallel-processing RAM also includes SRAM caches for each 32-bit processor (8 kbytes of instruction cache, 16 kbytes of data cache). The 256 Mbits of DRAM is divided into four blocks, one associated with each RISC processor.

When memory can't be integrated onto the same chip as the logic, high-speed or wide bus interfaces are needed to provide the high bandwidth needed to transfer data. Examining various interface options, designers at Rambus Inc., Mountain View, Calif., have developed some improved timing schemes. These schemes reduce clock skew and jitter so future DRAMs will be able to operate with data rates of 1.3 Gbits/pin/second (650-MHz clock rate), delivering a 5.2-Gbyte/s data rate over a 32-bit-wide interface.

A 300-MHz, dual-port graphics-RAM macro, detailed by Mitsubishi Electric Corp., Itami, Japan, in paper 24.3, employs a novel port-swap architecture. That port-swap architecture allowed designers to reduce cell area by 24% over the standard dual-port cell without impacting memory performance. The palette memory includes a read/write MPU port and a read-only pixel port. Internally, it shares the ports with a single bit line that is swapped via internal crossbar switches, reducing the cell area.

Both IBM Corp., Essex Junction, Vt., and NEC Corp., Tokyo, Japan, have developed high-speed, 4-Mbit, external-cache SRAM devices that operate at 350 MHz and 500 MHz, respectively. The IBM SRAM, presented in paper 24.5, achieves a 4.1-ns flow-through access time and employs self-timed, self-resetting, and low-signal-swing circuitry.

NEC, has developed a pipeline-burst cache SRAM that includes a point-to-point noise-reduction coding scheme in the I/O structures. Detailed in paper 24.6, the I/O circuits include push-pull output drivers that contain impedance control circuits. These drivers can achieve series-termination by matching the impedance of the output driver transistors to the transmission-line impedance. A customized ball-grid-array package also was developed to precisely match the impedance of the data lines in the package.

Making a NAND-based flash memory appear to the system as a non-volatile virtual DRAM, designers at Samsung Electronics Co. Ltd., Kiheung, Korea, have combined the best of both the DRAM and flash memory. In the so-called NVDRAM, fast, random-access time was achieved with a NAND flash memory by using a folded-bitline architecture. DRAM-comparable column-address-access time was achieved by sensing and latching 4k cells simultaneously. Dual on-chip 512-byte buffers hold data during read and write operations.

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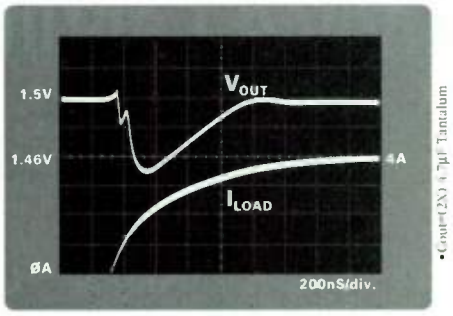

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Bandwidth Maintenance And Signal-To-Noise Ratios Are Key Points Of Discussion At The ISSCC.

Paul McGoldrick

SPECIAL REPORT

Analog circuits are facing many challenges as power supply voltages move toward 3.3 V and lower values. Some of the key issues include maintaining bandwidths and signal-to-noise ratios. Lowering the operating current or providing a standby mode are added goals in communications and consumer system design that have been placed on designers as well. Sessions at the ISSCC on filtering, low-power design, communication building blocks, and amplifier design provided many insights regarding design approaches for next-generation analog functions.

As the supply voltages on high-frequency circuits, particularly IF sections, continue to fall toward 3 V, the main design challenge is in creating operational amplifiers with high open-loop gain and large bandwidths to eliminate errors in the output. The output voltage swing also must be large enough to maximize the signal-to-noise ratio. These requirements are key aspects for functions such as sample-and-hold circuits, delta-sigma modulators, and switched-capacitor (SC) filters.

Communication Building Blocks

In highly-integrated transceivers used in wireless telephones, single-conversion superhetrodyne architectures have become popular as a means to reduce the number of passive filters required in the circuitry. Gain can be provided at either the IF frequency or at the baseband frequency, but as designers at ETH-Zentrum, Zurich, Switzerland, and Toshiba Corp., Tokyo, Japan, have found, the high-gain IF amplifier is preferable over a baseband amplifier since the IF amplifier prevents offset and flicker noise from significantly degrading the signal.

The companies have developed a programmable 71-MHz IF amplifier, fabricated in 0.4-mm CMOS, that is part of a 900-MHz transceiver. The amplifier, described in paper 5.1, delivers a maximum gain of 55 dB while drawing only 2 mA from a 3-V supply. However, to achieve the high gain at the IF, instability problems due to parasitic feedback through the substrate must be dealt with since CMOS does not have a buried layer to provide device isolation. To get around that problem, the IF amplifier is realized as a chain of three identically-configured amplifiers that each have their unity-gain bandwidth limited to 700 MHz.

The three-stage approach also lowers power consumption. Gain for the IF amplifier is programmable over a -20-dB to +60-dB range in 2-dB steps, but the first stage of the amplifier has a fixed 0- or +20-dB gain so that noise factor is minimized, while the second stage switches in three main steps, including attenuation, and the third stage in the needed 2-dB steps. Gain changes are realized with switched-sets of smaller differential pairs on both the inputs and loads.

An alternative to conventional I-Q modulation was proposed by the National Chiao-Tung University, Hsin-Chu, Taiwan, in the form of a phase-amplitude, vector modulation scheme that can generate higher frequency IFs (paper 5.2). It is felt that the modulation is particularly suitable for constant-envelope phase-modulation schemes, such as Gaussian-filtered minimum shift keying (GMSK), where no amplitude modulation is required.

In the circuit, a multiphase voltage-controlled oscillator (VCO) generates 64 different phases of the IF equally divided around the full 360° period (Fig. 1). The VCO output frequency is 4X the input reference and the phase-lock loop (PLL) contains a divide-by-four, a phase-frequency detector and a charge pump controlling the VCO. The 6-bit phase control selects a phase of the VCO output in the multiplexer, effectively converting digital-to-phase, with the amplitude changed by the (arbitrary) 3-bit control of the variable-gain output amplifier. Oversampling and an IF filter can push quantization noise outside the desired frequency band to filter it off.

The IC was fabricated on a standard 0.6-mm single-poly, double-metal CMOS semiconductor process and with a single 2-V power supply consumes 90 mW when operating at 100 MHz, with a PLL lock range from 82 to 106 MHz. Spurious

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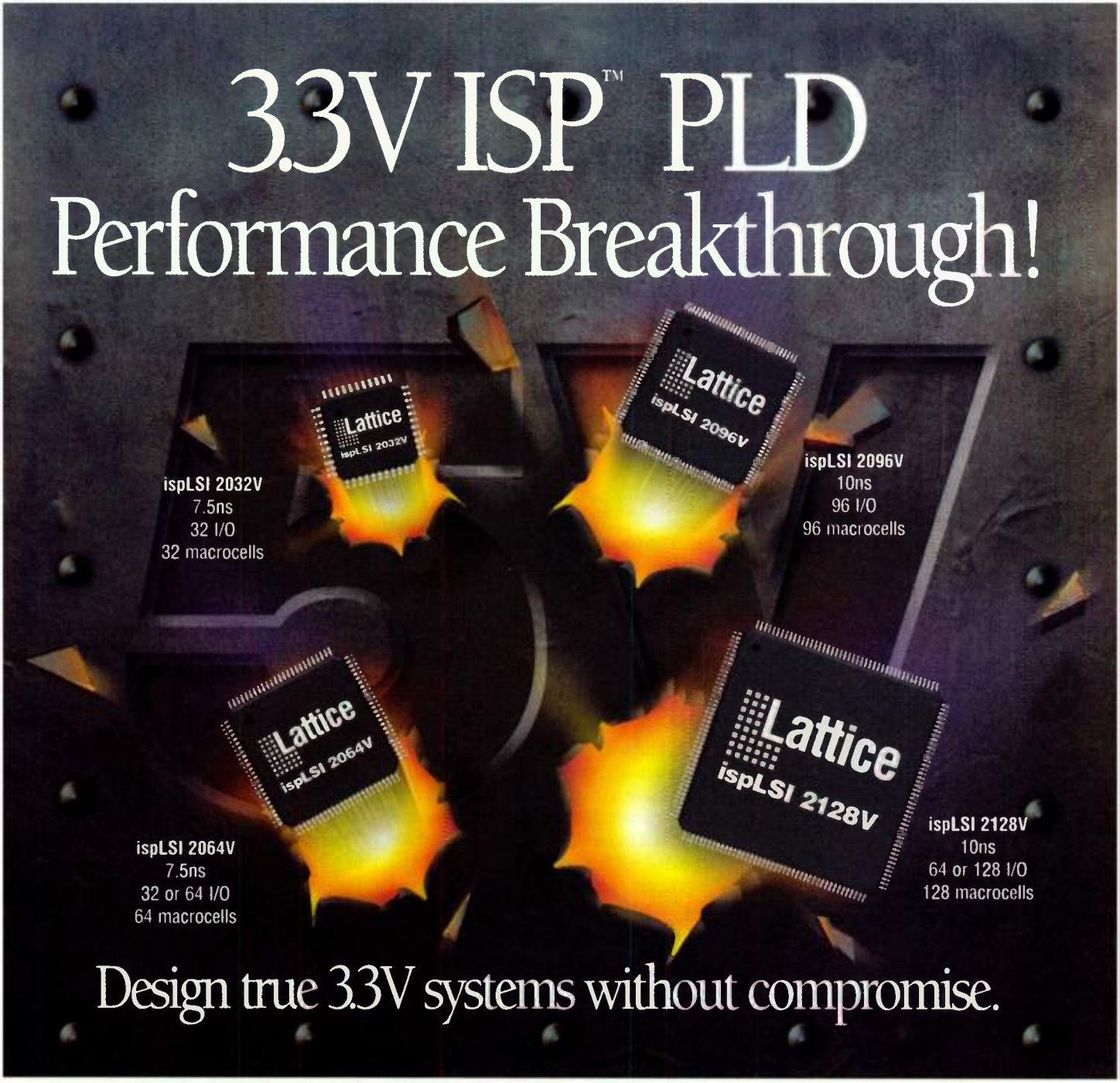

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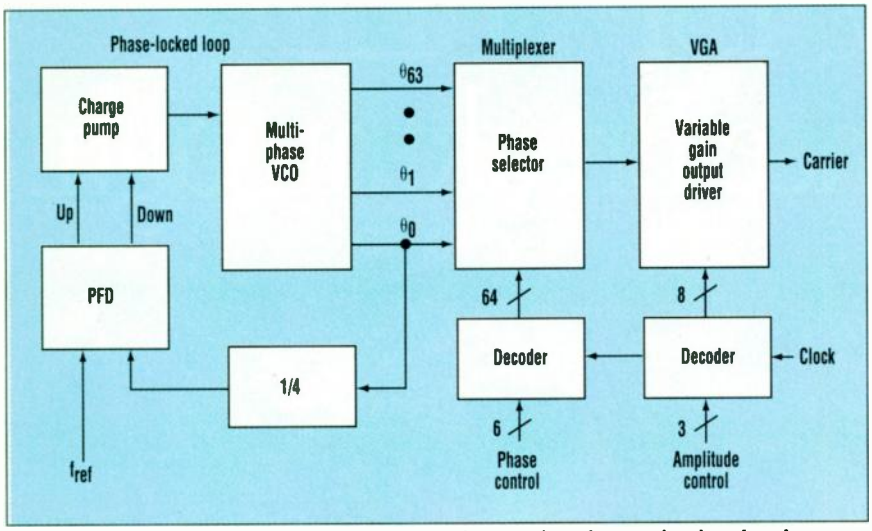

1. Able to generate high intermediate frequencies, this VCO-based circuit developed at the National Chiao-Tung University performs phase-amplitude vector modulation.

tones are all smaller than the main carrier by more than 41 dB, while time-domain phase jitter measured 29 ps rms and phase noise of the carrier was -91 dBc/Hz at 10 kHz offset.

IF amplifiers have a direct gain function and they also perform dynamic range compression by acting as an AGC or limiting amplifier without using any feedback loops. The simplification of receiver configurations makes them suitable for burst-mode operations such as time division multiple access (TDMA). Higher frequency IFs are in the offing when millimeter wireless systems offer services with bit rates of more than 10 Mbit/s and multi-GHz logarithmic/limiting amplifiers will be needed.

Low voltage operation, of course, is a continuing need for portable equipment, and resistive crosstalk in silicon substrates is a major problem in achieving high-gain, multi-GHz operation. NTT System Electronics Laboratories, Atsugi, Japan, described (paper 5.3) a 2-GHz monolithic silicon-bipolar logarithmic/limiting amplifier that solves many of the problems. It accomplishes this by introducing a waveform-dependent current phase shifter that compensates the intrinsic dependence of unit-amplifier phase shifts on input signals, and by silicon layout techniques that minimize crosstalk within and across the silicon substrate.

The IC dissipates 250 mW at 3.3 V and has a received signal strength indicator (RSSI) with a log-linear (semi-logarithmic) characteristic 60-dB dynamic range. The first implementation of the device used six cascaded unit amplifiers and seven full-wave rectifiers in the architecture, all in a fully differential configuration.

It has taken a while but the utility companies are becoming aware that they have a transmission capability on their power distribution network and that at a minimum it might be used for remote control and monitoring of the network; schemes also are proposed for reading utility meters in residences. Under a European Commission Esprit project, support has been given to Alcatel Mietec, Brussels, Belgium, and Landis & Gyr, Zug, Switzerland, to develop a power line carrier (PLC) modem using half-duplex, 300 to 1200 baud data streams modulated in a band of 9 to 95 kHz, via an FSK-like scheme (paper 5.4).

The analog front-end of the PLC modem chip under development requires a very high dynamic-range receiver (105 dB) and a direct-synthesis transmitter; the power network is not characterized for transmission quality, so impedance can range from 1 to 80 W , causing signal levels to range from about -63 dBm to +8 dBm. Noise levels also are highly unpredictable but are typically around 450 nV/ÖHz over the frequency band, while disturbances can be 30 dB above the useful level. Consequently, 8th order filters are needed prior to FSK demodulation while on the transmit side harmonics of the modulation must be kept 60 dB down because of the antenna-like behavior of the power lines.

Wireless Transceivers

Continuing their work on 900-MHz transceiver building blocks, the University of California at Los Angeles has taken them and developed a prototype, single-chip 900-MHz spread-spectrum transceiver fabricated in 1-mm CMOS (paper 7.2). The compelling attraction of large-scale integration to simplify systems raises questions as to how well digital CMOS can coexist with the radio front-end, provide isolation with large amounts of gain, or resist modulation of the VCOs by the power amplifier.

In their paper the authors presented design techniques for mitigating these possible problems and measurements from the transceiver to validate their approaches. On the ISM 902-928 MHz band with a 3- to 3.5-V supply, and a data rate of 160 kbit/s, receiver sensitivity was -105 dBm at 10 dB signal-to-noise ratio, the power amplifier output range was -17 to +14 dBm with a noise floor at -138 dBm/Hz and an active receive current of 120 mA and transmit current of 100 mA. The results basically validate the use of CMOS for an entire mixed-signal radio-on-a-chip.

The subcarrier capability of FM broadcast transmissions has been a relatively well-kept secret; these subcarriers, though, have been used for remote control of the transmitter equipment, commercial broadcasting of stock pricing, background music and numerous paging schemes. The European RDS (Radio Data System) uses a subcarrier at 57 kHz with 2.4 kHz reserved either side—and apart from its original use as a warning system to motorists, the subcarrier also is authorized for use as a pager channel. Work by Mixed Signal Structures, Roubaix, France; Info Technologies, Rungis, France; Info Réalité, Vendenheim, France; and the Polytechnical University of Bucharest, Romania, resulted in the development of a 2.2 to 3.5 V pager multi-chip module (MCM) in a standard TQFP package that follows a standard FM radio front-end (paper 18.1). Two ASICs are actually in the MCM, which together consume <300 mA in the active mode and <2 mA in the power-down mode.

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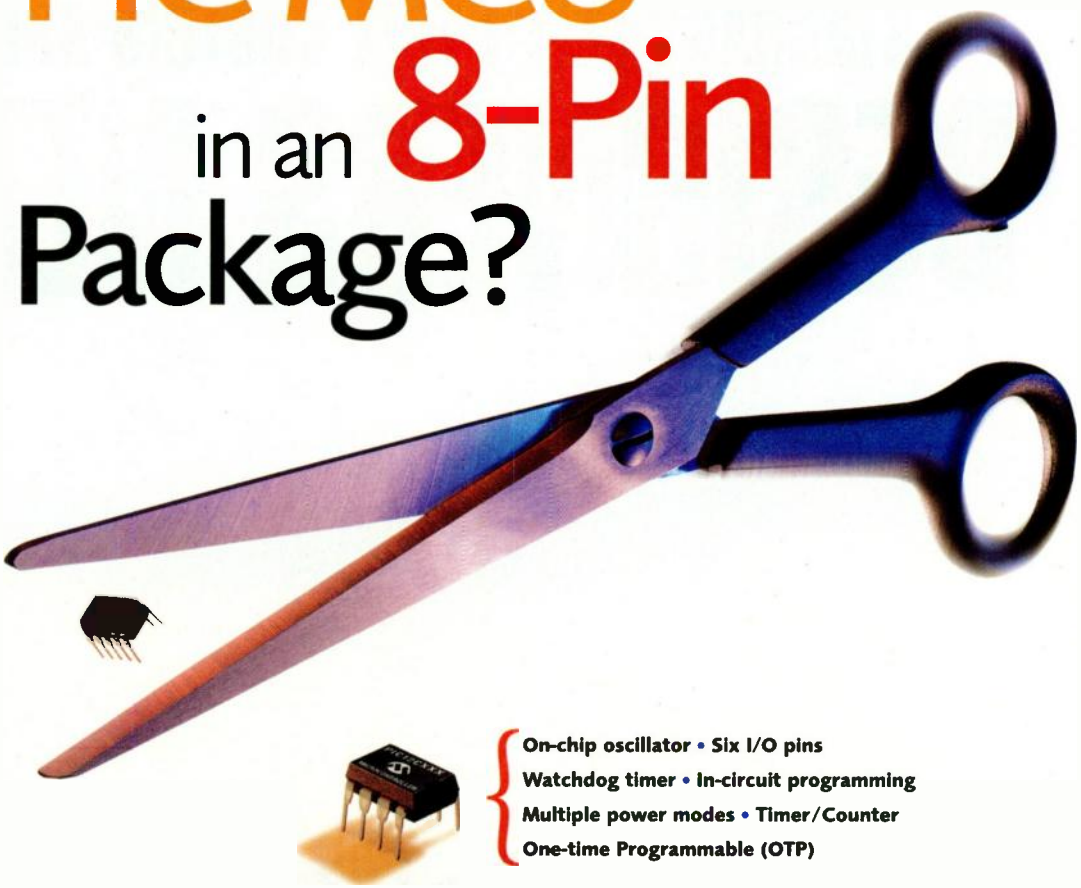

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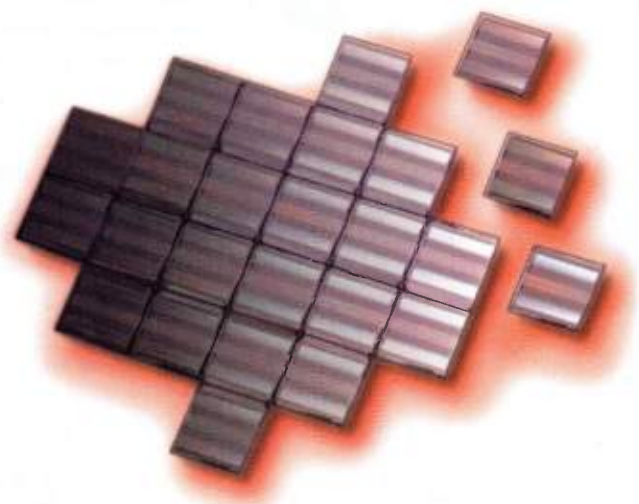

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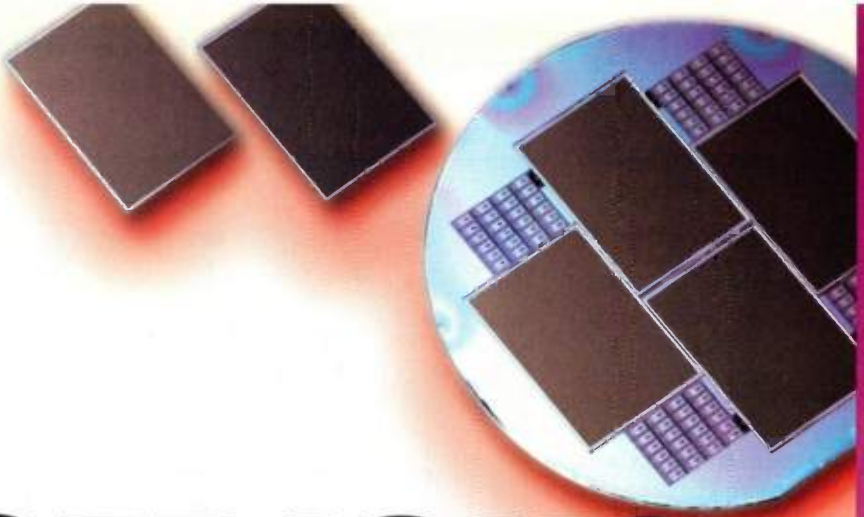

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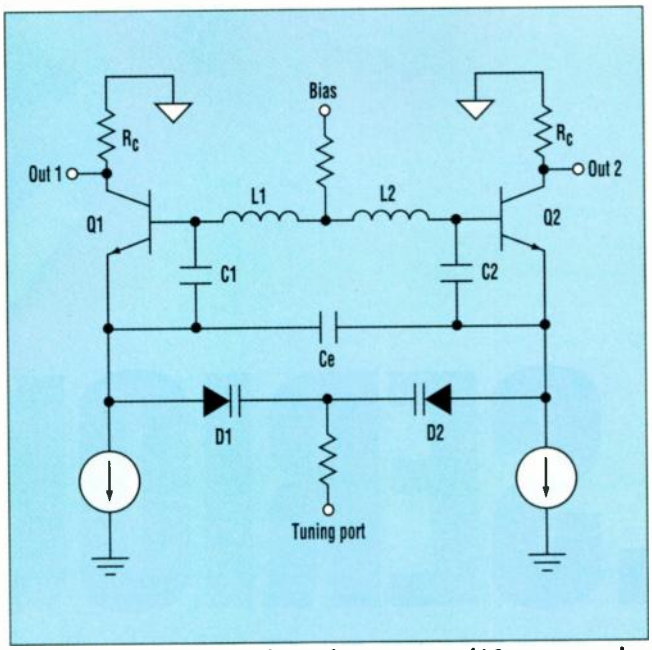
The design of a GSM transceiver using one main IC (plus power amplifier dual-synthesizer and peripherals such as SAW filters) was described by Hitachi Ltd., Yokohama, Japan, and The Technology Partnership, Cambridge, U.K., in paper 18.2. The main circuit employs quadrature-modulation PLL translator technology with an offset mix in the transmit path. The receive path is a double superhet that uses a low-noise amplifier (LNA) with active bias, two Gilbert-cell mixers, a programmable-gain linear amplifier and quadrature demodulator. The second oscillator VCO is on-chip, and separate power control functions are provided for receive and transmit. The IC is implemented in a 0.6-mm pure bipolar process with an f_T of 15 GHz in a 48-pin low-profile QFP package. Supply range is 2.7 to 3.6 V and the IC consumes about 32 mA in the transmit mode and 48 mA in receive.



2. A balanced 1.5 GHz VCO that packs an integrated LC resonant tank was jointly developed by Carleton University and Nortel.

Gilbert-cell mixers also are used in an integrated double-conversion receiver design from the University of California at Berkeley for the Digitally Enhanced Cordless Telephone (DECT) standard (paper 18.3). The conversion is wideband with channel selection made at baseband with low-pass signal processing; there is no band-pass filtering at the IFs. The entire RF, IF and baseband signal path is fully differential. The channel selection at baseband is, of course, like direct-conversion reception but there is no oscillator needed at the operating channel and the design of the local oscillators can be optimized. The reference sensitivity of the prototype was -90 dBm with a power dissipation of 198 mW from a 3.3-V supply.

A two IC chip set for DECT integrates virtually all but the receiver LNA, the transmitter power amplifier and filters in work reported by Siemens, Düsseldorf and Munich, Germany, (paper 18.4). The result is a receiver sensitivity of -95 dBm in the single conversion channel. To increase the isolation between oscillators and the PA, the transmitter buffer stage is included on the receiver IC. Two regulators also are on the transmitter IC, as are the PLL and control logic for both sides. The chips are fabricated in Siemens' 25 GHz B6HF bipolar semiconductor process.

A little less integration is involved in the work for DECT reported by Analog Devices Inc., Wilmington, Mass., where a baseband/IF IC as well as the LNA and PA are needed (paper 18.5). The design also was done in a 25-GHz bipolar process, and the chip includes a single-conversion receive chain, the upconverter transmit chain, as well as on-chip local oscillator distribution, a VCO, a low- dropout voltage regulator, and a node controller. A synthesis operating mode (where the VCO-only is active) is provided in addition to Receive, Transmit, and Standby. Minimum operating voltage is 2.7 V. The mixer on the transmit side is a degenerated Gilbert cell, while the receiver mixer is a class AB micromixer designed from an idea provided by Barrie Gilbert. The receive chain draws 37 mA at 3 V, while the transmit chain draws 32 mA.

More Building Blocks

A 1.8-GHz transmitter chip that avoids the use of mixers and DACs to generate I and Q waveforms by dithering the divider within a phase-locked loop was the focus of developments presented by the Massachusetts Institute of Technology, Cambridge, Mass., and Analog Devices Inc., in paper 22.2. The proof of the concept was implemented as a custom CMOS fractional-N synthesizer. Incorporated on the chip are a continuous-time filter requiring no external components or tuning, a digital pipelined, MASH-architecture D-S converter and a 64 modulus divider that supports any division value between 32 and 63.5 in half-cycle increments; dead-zone problems are avoided by the inclusion of a phase/frequency detector within the loop.

A CMOS front-end for a portable GPS receiver, including LNA and mixer, was described by Stanford University, Stanford, Calif., in paper 22.3. Implemented in a standard 0.35-mm digital process and consuming just 12 mW from a 1.5-V supply, the chip demonstrates the use of CMOS for wireless applications. The dynamic range of the receiver is determined by the care taken in the design of the linearity of the mixer and the noise figure of the LNA.

In anticipation of the complete integration of the GPS receiver (with a DSP core) these two blocks were designed with differential architectures, which results in a higher, but still acceptable, amplifier noise. A system of biasing the cascode amplifiers with a common-mode feedback scheme maximizes the use of the limited power supply headroom so that the amplifier will operate reliably on 1.5 V regardless of process, supply, and temperature variations.

The time division multiplex access (TDMA) use of the frequency bands for GSM and DECT requires that power amplifiers be ramped on and off rapidly for the transmit bursts. The recommendations dictate strict spectral templates to balance the rates of control with the spectral emissions. Just such a demand was met by Philips Semiconductors, Zurich, Switzerland, and Nürnberg, Germany, in their development of a Power RAMping (PRAM) controller (paper

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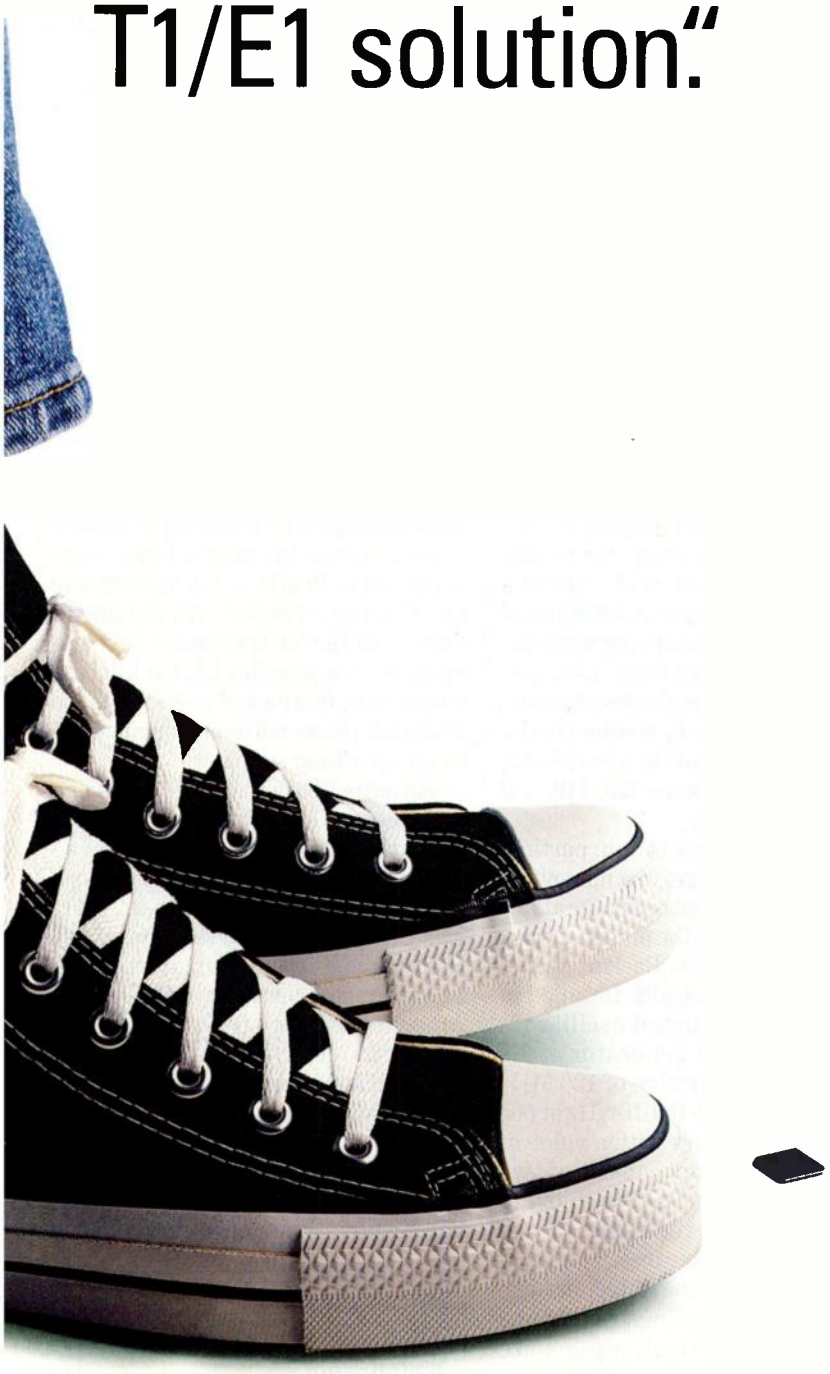

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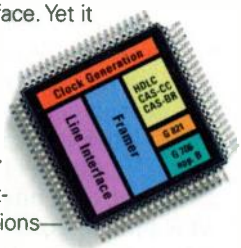

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22.4). The circuit offers all the controls for RF power amplifiers in bipolar or GaAs for the GSM, DCS1800 or PCN1900 standards.

The PRAM forms a control loop around the power amp with the ramping curves stored as target values; the actual output power is fed back for comparison and control. The start of a transmit burst, the minimum and maximum power, and the burst duration are set using a fast digital control bus and a real-time trigger signal. The device, which can be a library item with the power amp, can be programmed in real-time via the chip's digital control bus with a maximum operating speed of 10 MHz.

Analog Techniques

The Automatic Test Equipment (ATE) market is increasingly demanding higher speed, lower costs, higher pin-counts, and more accurate timing. Schlumberger Technologies, San Jose, Calif., and NTT System Electronics Laboratories, Kanagawa, Japan, worked in collaboration to develop a 600-MHz pin electronics IC (paper 23.3). The chip integrates the major ATE pin electronic components of a driver with termination function, a programmable load, a window comparator, and hard clamps.

By integrating the driver and termination switching, the pin-electronics chip allows for far faster testing. It has a timing error of less than 25 ps for pulse widths as short as 0.8 ns. It also reduces voltage glitches on the test pins, lessens the degradation of the minimum pulse width, and removes propagation delay mismatches. A silicon complementary bipolar process was used with an f_T of 9 GHz for npn and 5 GHz for pnp transistors. A GaAs MESFET device was not used because of the inherent problem known as "flow tails."

Controlled oscillators are a core component of communications systems . Important characteristics of the devices include frequency, tuning range, linearity of control voltage (or current) to frequency, phase noise, stability, and cost of fabrication. In the last few years, there have been some competing arguments about the design directions in which to go with technologies for the implementation, running from ring oscillators to relaxation circuits to monolithic inductance/capacitance elements.

In paper 23.5, the Korea Advanced Institute of Science and Technology and the Electronics and Telecommunications Research Institute, both in Taejon, Korea, presented their research in which they built and compared three types of CMOS current-controlled oscillators. A three-stage, single-feedback oscillator was compared with two other types:a three-stage, double-feedback and a four-stage, triple feedback circuit.

The simplification of receiver configurations makes IF amplifiers suitable for burst-mode operations such as TDMA

The oscillators were built fully differential and used steering-logic delay cells. The frequency range for oscillation was found to be wide, about a decade, with all three exhibiting good linearity; the maximum operating frequencies of the three were 1.39, 1.58 and 1.69 GHz for the single-, double-, and triple-feedback, respectively. Power dissipations of the core blocks, with a 5-V supply, were 123, 110, and 78 mW, respectively.

Examining the operation, particularly the tuning range, of a monolithic LC voltage-controlled oscillator at low supply voltages was the object of work performed at Hewlett-Packard Laboratories, Palo Alto, Calif. Detailed in paper 23.6, the coupled oscillators form a quadrature generator at 1.8 GHz with a tuning range of 120 MHz and a phase noise of -100 dBc/Hz at 500 kHz offset. Inductors with a value of 10 nH are used; they consist of two stacked-spiral structures, achieving roughly four times the inductance of one spiral of the same area. The parasitic capacitance of the inductors plus inter-oscillator couplings reduce the variable part of the tank capacitance from 780 fF down to about 270 fF.

Carleton University and Nortel, both in Ottawa, Ontario, Canada, presented their work on a balanced 1.5 GHz VCO also using an integrated LC oscillator in paper 23.7. This circuit is a further alternative to the controversial wire-bond inductor techniques, with coplanar inductors, polysilicon capacitors and on-chip varactors formed in a 0.8-mm biCMOS process with an 11 GHz fT (Fig. 2).

The circuit shows the output being taken from the collector instead of the normal emitter-output on a true common-collector Colpitts oscillator. This isolates the load from the tank circuit and increases the Q of the oscillator. Each side of the oscillator is a negative-resistance circuit, where the base input impedance is negative when the base resistance is low enough.

The authors believe the phase noise is the lowest reported in a fully-integrated LC oscillator at -105 dBc/Hz at a 100-kHz offset with a 3.6-V supply, meeting not only DECT but also CT-2 system specifications. The output level also is among the highest at -6.6 dBm into a 100-W differential load, thus avoidingthe use of buffers. The tuning range of the VCO is 150 MHz with less than 1 dB of output power variation over the range. Power consumption is 40 mW at 3.6 V, including the biasing circuitry. An enhanced version of the VCO is under development with a parallel LC tank in the collectors, instead of resistance, to maintain phase noise performance at lower operating supplies.

An output buffer is included on-chip in a design described by Hewlett-Packard Co., Newark, Calif., to get a -3 dBm output from a family of silicon bipolar VCOs over a 1.1-to-2.2-GHz range (paper 23.8). These circuits have the tank and tuning fully integrated, and a varactor characterized with a 3:1 capacitance range from 0-to-3-V reverse bias and a Q of 30-50 across the frequencies. Phase noise (at 100 kHz offset) ranges from -105 to -99 dBc/Hz from 1.1 to 2.2 GHz. The tuning ranges are from 150 to 250 MHz. All three take about 15 mA supply current and will operate over a range of 2.7 to 5.5 V.

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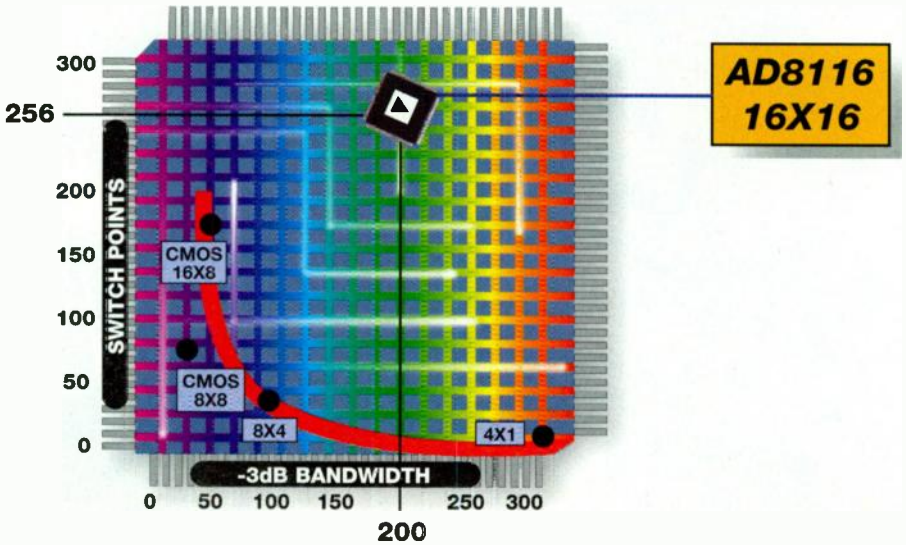

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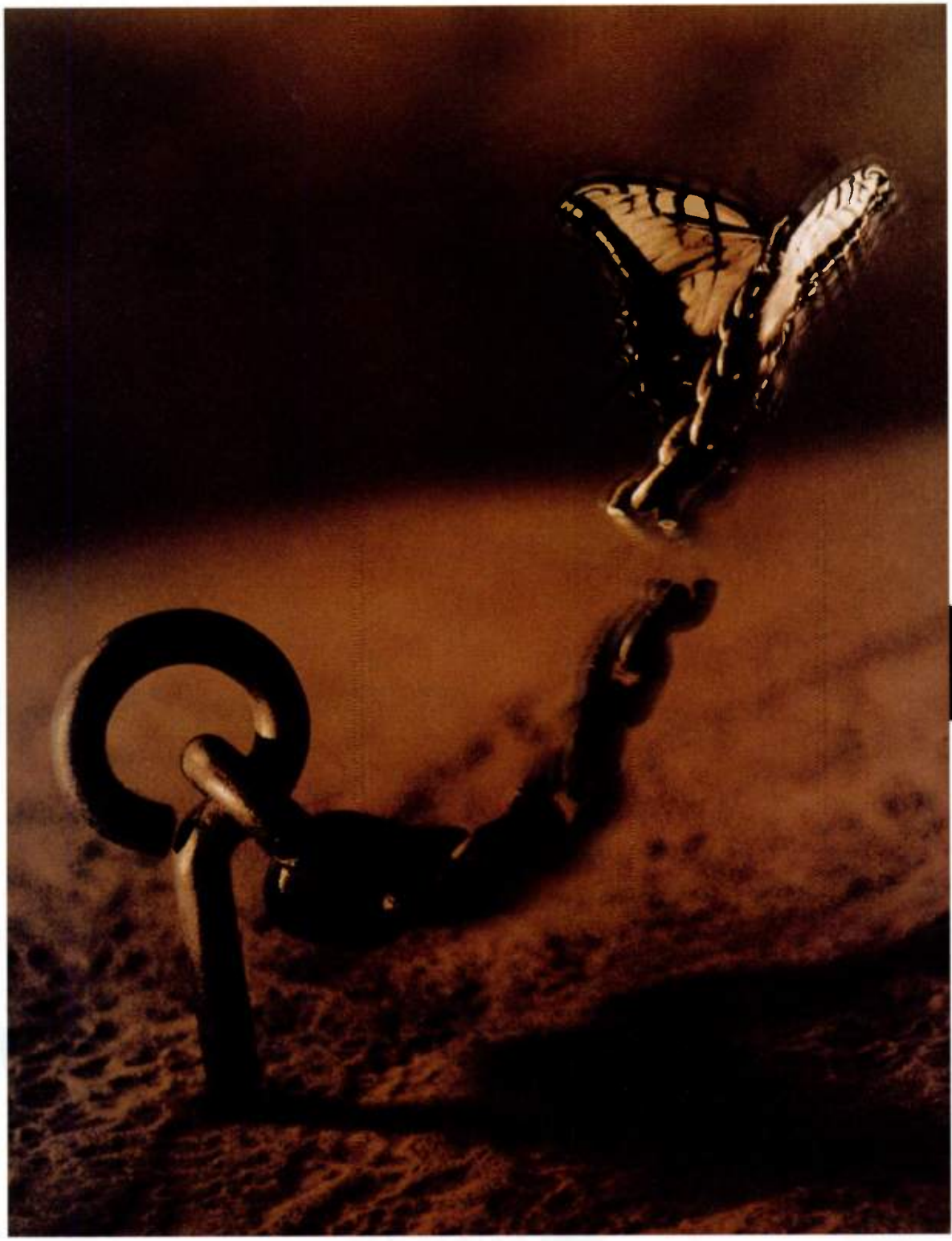

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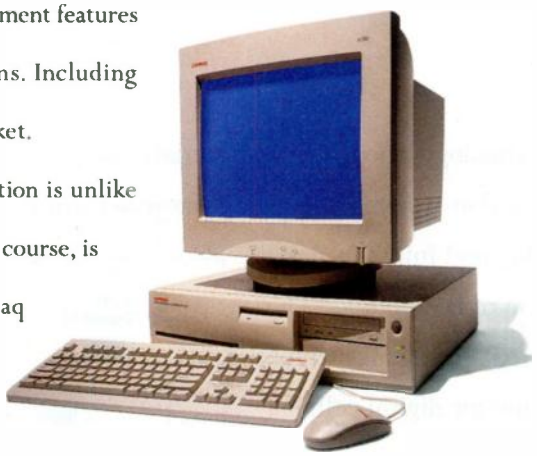

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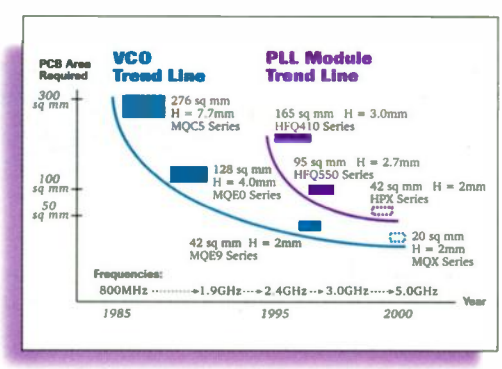

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Speed and Resolution Dominate A/D Converters at ISSCC

Track/Hold Amplifiers And Pure-Sampled Analog Signal Processing Reappear At ISSCC.

Frank Goodenough

SPECIAL REPORT

Those gurus who, a few years ago, wrote analog technology's obituary now are probably hiding their collective heads. The reason behind that shame is that at this year's ISSCC, 23.1% (the largest percentage) of the 164 accepted papers were analog. However, on closer inspection of the papers in the other classifications, a trend appears. Analog-IC technology dominates the conference. Papers discussing this technology include such topics as communications, sensors and imagers, disk-drive electronics, signal processing, and technology directions. In fact, even some of the digital papers describe phase-locked loops and clocks, which also have their roots in analog technology.

This year, ISSCC has seen a bumper crop of innovative new designs, with analog-to-digital converter (ADC) and sample-to-hold amplifier (SHA) presentations filling two sessions. Session 8 covers general-purpose converters that offer unique combinations of speed, power, and resolution, and Session 13 details high-resolution, oversampling ADCs. Additional ADC papers also are hidden in other sessions, embedded as part of more complex circuit discussions, or as part of the emerging technologies session.

In fact the fastest ADC, a 4-bit, 8-GHz device fabricated in SiGe, was presented as part of Session 7 (Technology Directions). Its silicon-germanium cohorts include several other pure-analog (not sampled analog) ICs, plus a 42-GHz SiGe frequency divider, quantum devices for memory and logic, and 20 Gb/s Josephson/Quantum technology.

The 4-bit flash ADC that samples inputs at 8 GHz, created by IBM, is fabricated with the company's heterojunction silicon-germanium bipolar process. The process yields npn transistors with an f_t of 45 GHz at 1 mA, a current gain of over 100, and an Early voltage of better than 60. In the past, similar devices have required power-hungry GaAs designs.

The ADC employs a pipelined encoder and sports an input bandwidth of 4 GHz. Able to run from a 3.6-V rail, the converter consumes just 500 mW. On the chip are 15 comparators that were built with the SiGe npns. These comparators all have differential preamplifiers (Q1, Q2, Q3) on their inputs *(Fig. 1)*. At high input frequencies the input signal feeds into the reference node via capacitor C_1. The decoding XOR gates are based on Gilbert multipliers. The open collector output stages (Q4/Q5) drive 50 Ω loads.

While their circuit simulation indicated the sampling rate could be upped to 10 GHz, testing the chip, even at the 8 GHz rate, could prove to be quite difficult. As the ICs get faster, they get harder to test due to a lack of high-frequency test equipment. To test the ADC, designers had to resort to beat-frequency testing to determine bandwidth. The use of FFTs to determine distortion was found to be impossible.

While ADCs abound, DACs are conspicuous by their absence. This year there was just a single paper on a CMOS chip developed by Yokogawa Electric Corp., Tokyo, Japan. Intended for providing programmable precision dc voltages for IC-tester pin drivers, the chip contains a 12.7-bit, 28-channel DAC.

The circuit does not have to be trimmed at any time during its manufacture or when in use. To eliminate calibration, designers combined a triple-rank architectural scheme with a binary-weighted transconductance technique. All 28 channels share the 52-resistor string in the coarse 6-bit DAC; they also share the 4-bit output of the g_m stages, and the 7-resistor string forming the fine 3-bit DAC. The voltage output of the three ranks are summed to form the output of the 28-channel DAC. Although the die is smaller than if it had to hold 28 complete DACs, it still is considerable for an analog circuit, more than 8-mm per side.

Since virtually all ADCs today are sampling devices, they contain their own on-chip SHA amplifier. In the recent past, few papers describing SHAs have been presented however, again proving that it's hard to predict future analog-IC trends, a trio of papers in Session 8 at this year's ISSCC detailed new SHAs.

All three of the SHAs provide 10-bit accuracy,

but while two of them sample at 250 MHz and 300 MHz (papers 8.7 and 8.5, respectively) the third samples at 1 GHz (paper 8.6). Developed by a three-man team from Ruhr-Universitat, Bochum, Germany, the 1-GHz device was built on a 25-GHz bipolar process that keeps the power down to less than 490 mW when the chip is powered by a -5.2-V supply. Measured total harmonic distortion over the full Nyquist band, while sampling at 1 GHz runs better than -62 dB.

Closed-loop SHAs usually offer better accuracy, but their bandwidth is limited. On the other hand, open-loop samplers, while speedy, offer limited accuracy, 10-bits. The 1-GHz SHA mixes open and closed-loop architectures to get the best of both approaches.

A Lively Quintet

The five ADC papers in Session 8 all describe outstanding chips. Each is very different from the other four in performance, architecture, and process. They range from a 10-bit 200 kHz successive-approximation (SAR) chip, using an R-2R network built of MOSFETs that boasts an untrimmed accuracy approaching 13 bits, to a 15-bit ADC that samples at 5 MHz. In between lie a trio of speed demons including 10- and 12-bit 50-MHz ADCs, and a 12-bit 128 MHz device.

The 15-bit, 5-MHz chip sports a differential nonlinearity of 0.75 LSB, while keeping harmonics below -93 dB. Both the 15-bit, 5-MHz chip and the 10-bit MOSFET SAR are built on CMOS processes, the former on a 1-µm process, the latter on a 1.4-µm technology. The speed demons and the 15-bit, 5-MHz chip all employ several unique conversion stages.

The 10-bit, 50 MHz ADC, built on a 0.5-µm CMOS process dissipates just 170 mW when powered by a 5-V supply. It was designed by a team from Broadcom Corp., Irvine, Calif., and the University of California, Los Angeles. It handles a full-scale input range of 2 V by cascading three stages of folding amplifiers ahead of a bank of comparators similar to those in a straight flash-type ADC. To improve the differential nonlinearity, the outputs of the folding amplifiers are averaged by connecting them with resistors.

The 12-bit, 50 MHz ADC, developed by a team from Philips Semiconductors, Caen, France, and Philips Research Laboratories, Eindhoven, The Netherlands, is based on an architecture that follows each of two 3-bit cascaded folding stages with interpolation. The interpolation stages are followed by a 6-bit fine-conversion stage and its encoders. The chip was fabricated on a 13-GHz, 1-µm BiCMOS process, and needs just 300 mW when operating from a 5-V rail. Its signal-to-noise ratio (SNR) while sampling a 4.43-MHz signal at 50 MHz, runs better than 64 dB. And, the total harmonic distortion (THD) under similar conditions, runs better than -75 dB.

To sample at 128 MHz and digitize to 12-bit accuracy, the team of designers from Hewlett-Packard Laboratories in Palo Alto, Calif., employed a basic two-step architecture. To get their final performance, they incorporated integrated dither, dynamic-element matching, and output-data scrambling. The results: an spurious-free dynamic range of 85 dB, and a differential nonlinearity of less than 0.05 LSB while sampling at 128 MHz.

The first flash ADC provides the five most-significant bits. These bits switch the 32 matched-current sources of the 12-bit accurate main DAC. The output of the DAC is summed with the output of the input SHA. The residue is then amplified and fed to the second flash ADC, an 8-bit circuit employing folding and interpolation. No analog pipelining is used (there is no SHA at the output of the residue amplifier) in order to allow very slow clock rates. However, it takes just 4.4 ns from the time the input SHA goes into hold until the 8-bit flash ADC latches its output. Dynamic-element matching linearizes the 5-bit main DAC. Fine-grain nonlinearities are removed by a dither circuit which, in the SHA, subtracts an 8-bit random value from the analog value and later adds it to the output in the digital error-correction adder. The dither spreads the dc input over 256 codes which averages or smooths the result. The chip contains over 14,000 npn transistors fabricated via a 25-GHz process and consumes 5.7 W from a 5-V supply.

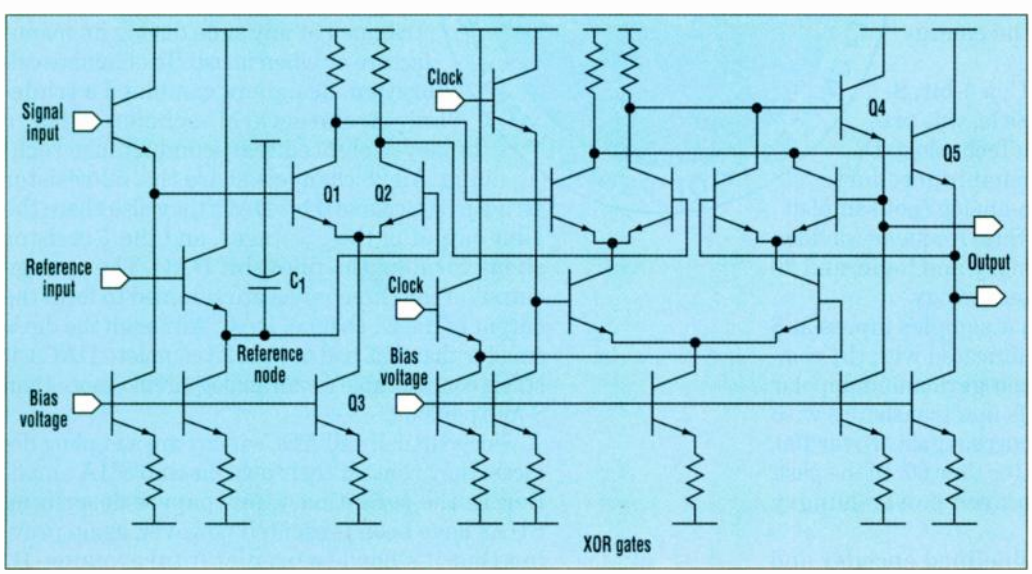

Fig. 1. Each of the 15 input circuits, such as this one, form the heart of a 4-bit silicon-germanium flash ADC, developed by IBM. The circuit samples its input at 8 GHz, then amplifies the input signal with a differential amplifier (Q1, Q2, Q3).

Fifteen Fast Bits

While it's fast for a 15-bit ADC, the 5-MHz CMOS converter lacks a SHA on the front end, so true ac performance is limited. The chip was designed to try out an innovative technique to auto-calibrate—continuously in the background—to 15-bit accuracy. Designed by a team

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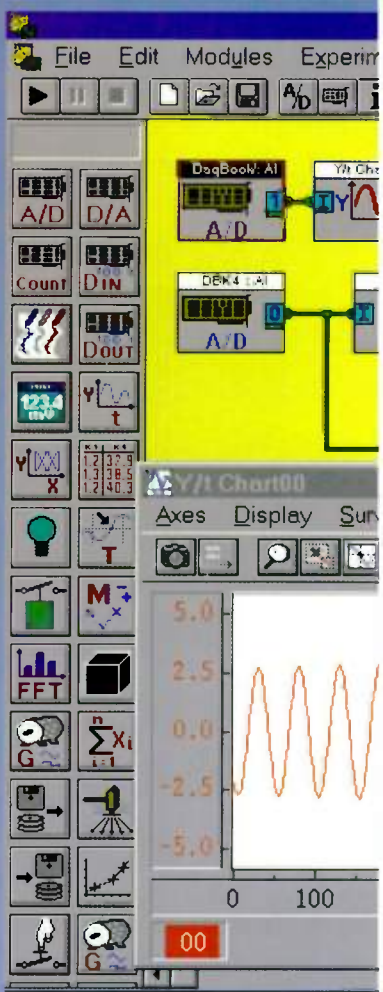

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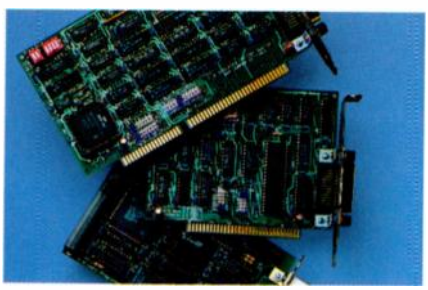

The Personal488™ series includes IEEE 488.2 interfaces for desktop PCs, notebook PCs, and PC/104 board-level computers. Software support includes DOS, Windows™, and Windows™ NT drivers for programming languages such as C, Pascal, Visual Basic™, and Quick Basic™. National Instruments-compatible DOS, Windows™, and LabVIEW® drivers available. From $395.

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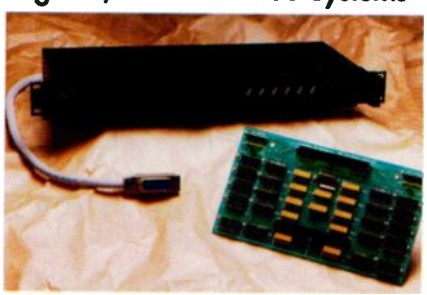

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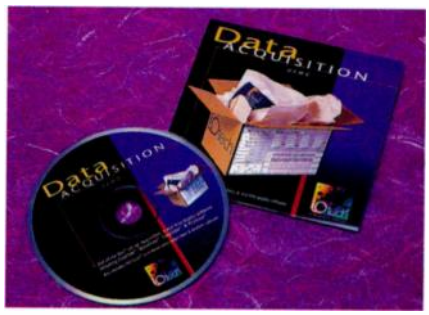
Data Acquisition Demo CD



IOtech's new Data Acquisition Demonstration CD features a variety of software products, including DaqView™ *Out-of-the-Box*™ set-up, data acquisition, and real-time display software for IOtech's parallel-port, ISA-bus, and PCMCIA data acquisition systems. The demo CD also offers evaluation versions of PostView™, a post-acquisition waveform display package, and DASYLab™ high-speed, icon-based acquisition, graphics, control, and analysis software. Free.

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from the University of Illinois, Urbana and Harris Semiconductor Corp., Melbourne, Fla., the converter employs four stages. A 6-bit flash follows three 5-bit flash stages, each with a 5-bit DAC, summer, and gain-of-16 residue amplifier.

The chip performs digital-code error calibration, in the background, via the first two 5-bit stages. As in any ADC using digital error correction, the number of bits resolved per stage is set higher than required by the basic converter resolution. During calibration, a known calibration voltage is injected in place of an input signal. The missing outputs are filled using nonlinear interpolation. In a switched-capacitor ADC such as this one, the technique eliminates two basic errors: those resulting from capacitor-ratio mismatch and those due its op amp's finite, open-loop dc gain.

The IC delta-sigma ($\Delta\Sigma$) ADC has been a basic building block in the electronics industry for over ten years. Additionally, it has revolutionized the high-resolution industrial ADC arena as well. The seven papers in Session 13 describe ADCs ranging from two high-frequency band-pass Δ-Σ modulators aimed at digitizing the output of radio frequency IF stages, to a complete converter designed to handle wideband (44 kHz) digital audio. The session also included papers describing such diverse devices as a delta sigma ADC on the front end of a pipelined ADC, and a high-performance audio Δ-Σ converter that dissipates just 2.3 mW.

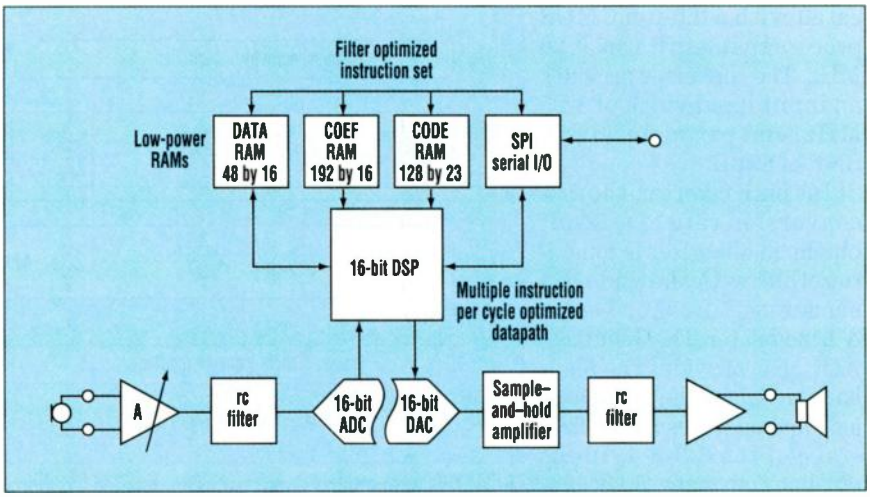

Fig. 3. This pseudo-analog signal processor on one chip, developed by Fujitsu, contains an ADC, a DSP, and a DAC. It converts the input signal to digital words, processes them, and converts the result back to analog form.

A team of designers from Hughes Research Laboratories, Malibu, Calif., and Hughes Radar and Communications Systems, El Segundo, Calif., described their bandpass Δ-Σ modulator that couples 92 dB (15 bits) of SNR with a continuously-programmable center frequency from 0 to 70 MHz. The 92 dB SNR is achieved during narrow-band (366 kHz) operation. It drops to 44 dB (7 bits) in broadband (62.6 MHz) operation. The modulator samples at 4 GHz. To achieve the high speeds, the chip was fabricated in a heterojunction AlInAs/InGaAs bipolar (npn only) technology whose transistors sport an f_t and an f_{max} of about 80 GHz. A fourth-order bandpass Δ-Σ modulator, fabricated with a 0.6-µm CMOS process was developed by designers at The Center for Integrated Systems at Stanford University, Stanford, Calif. It digitizes a 200-kHz signal centered at an IF frequency of 20 MHz, while offering a dynamic range of 75 dB.

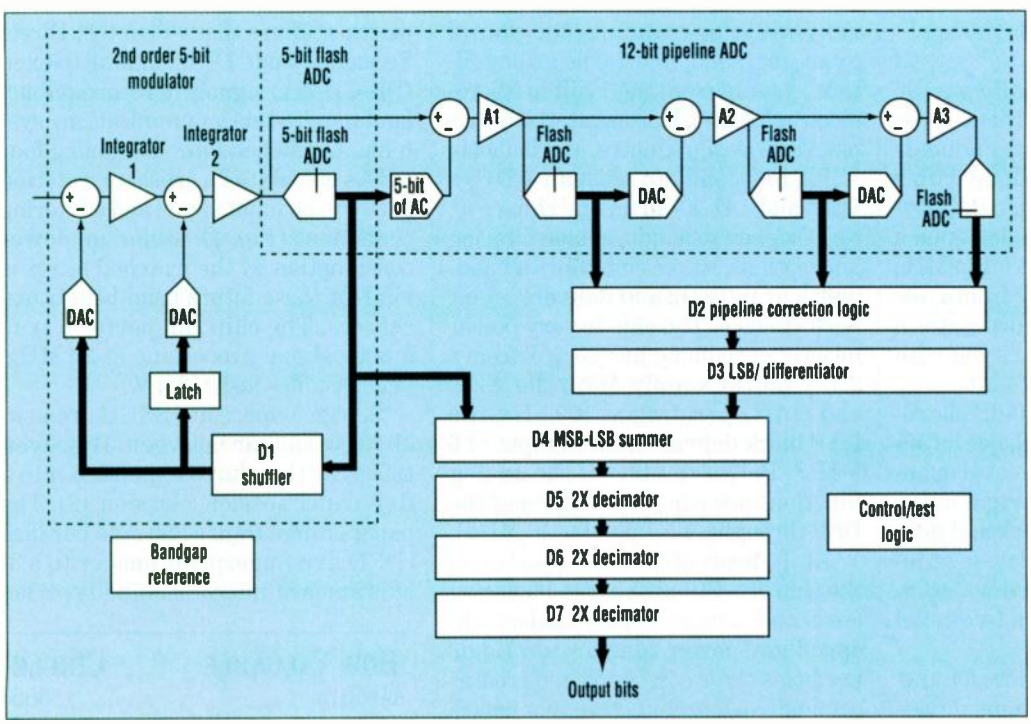

Fig. 2. This unique ADC combines high-precision, delta-sigma architecture with high-speed pipelined architecture. Developed by Analog Devices, the converter samples at 20 MHz and provides a 90-dB dynamic range.

The most interesting ADC of this genre has got to be the 16-bit pipelined ADC with a 5-bit, second-order, Δ-Σ modulator on the front end of the pipe *(Fig. 2)*. Developed by a team from Analog Devices, Wilmington, Mass., it provides a 2.5-MHz data rate. Aimed at multitone communication schemes that require ADCs with wide dynamic ranges and bandwidths above 1 MHz, the chip was fabri-

cated with a 0.6-μm CMOS process that lets it run at 20 MHz. The converter provides an input bandwidth of 1.25 MHz, and can maintain an SNR of 89 dB.

In this converter, the fast conversion rate of a 12-bit pipelined quantizer is joined-together with the wide dynamic range of a second-order Δ-Σ modulator. The 5-bit flash ADC, F1, provides the feedback signal for the modulator loop and operates as the first stage of the 5-3-3-4, 12-bit pipeline converter. A second-order modulator loop with a multiple feedback structure provides second-order differentiation of the flash quantization errors.

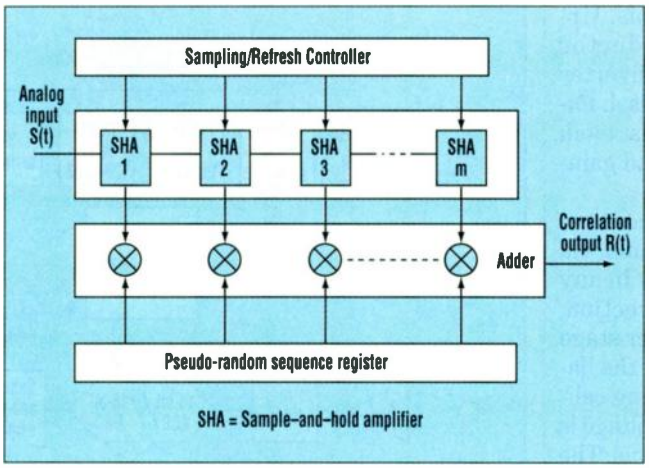

Fig. 4. This pure-analog signal processor, created by Sharp, performs cross correlation (a form of matched filtering) at 50 MHz with four sample-and-hold amplifiers.

The first-stage pipeline-residue amplifier, A1, provides an analog representation of these flash errors. The last three stages of the pipe digitize the output of A1. Differentiating the flash errors and subtracting them digitally from the 5-bit output of the modulator loop (with D3 and D4) cancels these errors.

Digital-signal processing can replace analog-signal processing in professional audio equipment only when ADC dynamic range approaches 120 dB. And, super-high-end audio applications extend the audio band beyond 30 kHz, and demand sampling at 96 kHz. To meet such applications, a design team at Crystal Semiconductor Corp., Austin, Texas, came up with a Δ-Σ ADC that offers 118 dB of dynamic range. Crystal also designed a modulator that samples at 6.144 MHz and consumes just 760 mW from a 5-V supply. The converter incorporates a single-loop, seventh-order circuit with a three-level quantizer.

The ADC achieves a 140-dB signal-to-quantization noise level, over a 48-kHz bandwidth. The three-level quantizer offers reduced thermal noise from the reference network and generator, no in-band tone for low-level inputs without dithering, and wider input dynamic range than a two-level modulator.

Two similar Δ-Σ modulators for low-power (battery) applications developed Philips Research Laboratories, Eindhoven, the Netherlands, allow a system designer to trade off performance for battery life. Both are fourth-order devices that have 20-Hz-to-20-kHz bandwidths and run from 5-V supplies. One of the circuits consumes just 2.3 mW, but can only provide a 96-dB dynamic range. The other implementation of the chip increases the power consumption to about 6.6 mW and improves the dynamic range under similar conditions to 101 dB.

DSP And Analog Signals

DSPs perform some analog tasks very well, for example, they build great, high-end, multi-pole analog filters. A team from the Fujitsu Microelectronics Ltd., European Mixed-Signal ASIC Design Centre, Maidenhead, U.K., has come up with an ADC, a DSP, and a DAC all on one chip *(Fig. 3)*. Designed to handle analog filtering applications, the circuit offers a bandwidth of 100 kHz and delivers 16-bit performance. The chip is very power miserly, consuming just 25 mW from a 2.7-V power supply. With the ADC and DAC operating at 100 kHz, the DSP block delivers a throughput of 6 MIPS. Power doubles if the analog functions are run at 333 kHz and the DSP throughput is upped to 16 MIPS.

At the heart of the analog portion of the chip lies a 16-bit, charge-balancing (switched-capacitor) DAC and a high-speed low-power comparator. Logic performs error correction and creates a unique SAR architecture that makes two comparisons per bit to remove the need for accurate settling. While demanding twice as many clock cycles, it still cuts total conversion and latency by more than a factor of four. This SAR only changes the DAC input code if the result is larger than half the weight. A conventional SAR compares the input to the DAC output and increases or decreases the DAC code by a full bit weight, which effectively halves each cycle. Thus, two clock cycles are needed to make comparisons with upper and lower thresholds.

The chip's 16-bit fixed-point DSP is optimized to implement cascaded, biquad, IIR filters. It needs half as many clock cycles per biquad as a general-purpose DSP. A multiple-bus triple-RAM architecture executes single-cycle compound instructions such as the following: multiply/accumulate, rounding/saturation/absolute value, memory read/write, auto address control, and fast sleep/wake up. This signal-processing IC interfaces with its system via a master/slave-mode 4-wire serial bus.

A team from the Sharp Corp., Tenri, Nara, Japan, has developed a chip that employs analog sampled-data techniques to build 50-MHz matched filters that will detect Direct Sequence Code Division Multiplexed (DS-CDMA) signals in future public-land mobile-telecommunications systems. A matched filter containing four SHAs calculates a cross-correlation between an input signal and a filtering coefficient *(Fig. 4)*. Minimum power consumption by the matched filters is vital for these future hand-held transceivers. The chip can perform true analog signal processing at 25 MHz, yet consumes just 110 mW.

Sensor papers at ISSCC are usually few and far between. However, this year they have expanded into a five-paper session (Session 12). The papers range from a 390 dots per inch (DPI) live fingerprint imager to a 3-axis surface-micromachined Δ-Σ ac-

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Many Approaches Expand The Communications Horizon

Wireless And Multimedia Take Center Stage As Technology Drivers, While Silicon Meets The Challenge Of GigaHertz Communications.

Lee Goldberg

SPECIAL REPORT

The communications explosion of the late 90's continues to challenge the semiconductor industry to push the frontiers of speed, size, and complexity. Nowhere is this trend more evident than at the International Solid State Circuits Conference (ISSCC). While papers throughout the conference covered a wide array of subjects, communications-related topics accounted for nearly 20% of the total, second only to analog design.

Some of the more notable topics within this vast offering include integrated satellite receivers, advances in wired and wireless LAN transceivers, digital baseband processing, and ever-more sophisticated ATM network components. Although many of the devices presented are labeled "experimental," it's a good bet that we'll be seeing many of their descendants entering the marketplace within a year.

Space Is The Place

The advent of the direct-broadcast satellites signaled the transition of satellite TV from an expensive toy to a consumer commodity and the rise of very small aperture satellite transceivers (VSATs) for industrial and commercial applications. This has created a strong demand for low-cost, high-performance receiver circuits. In Session 5, "Communications Building Blocks," two papers stand out as blueprints for the next generation of satellite RF components.

In "A 480 MHz Variable Rate QPSK Demodulator For Direct Broadcast Satellite" (paper 5.5), researchers from Analog Devices Inc., Wilmington, Mass., present a two-chip demodulator that performs all the necessary digital and analog functions to extract a 10- to 85-Mbit/s data stream from a 480-MHz QPSK signal. The chip's designers achieved their goals by carefully segmenting tasks onto separate analog and digital chips and setting up controlled feedback paths between them *(Fig. 1)*.

The analog front-end receives a single-ended IF signal. That signal is passed through a three-stage AGC circuit that provides high linearity over an input signal range of -50 to -10 dBm. Quadrature demodulation and on-chip PLL-based clock synthesis also is performed in the analog segment of the demodulator. Filtered I and Q signals are then passed to the digital chip for clock and symbol recovery.

As expected, the demodulator's digital segment performs the convolutional decoding and data synchronization functions, but it also is responsible for providing feedback for adaptive tuning of the PLL to compensate for phase drift due to time, temperature, or other factors.

A companion chip was presented by Philips Research Laboratories, Eindhoven, The Netherlands, in a paper entitled "A 0.9-to-2.2 GHz Monolithic Quadrature Mixer-Oscillator For Direct Conversion Satellite Receivers", (paper 5.6). The researchers contend that the low component count and simplicity of direct-conversion architectures offer many advantages for low-cost, highly-integrated systems. On the other hand, they suffer from some inherent problems. Besides addressing perennial problems of direct-conversion receivers (such as local-oscillator (LO) leakage and I/Q mismatching), the Philips authors chose to see if they could implement their design using a standard silicon process and a minimum number of external passive components.

Much of the quadrature-mixer/oscillator circuit is based on a stacked architecture that connects the mixers on top of the chip's quadrature current-controlled oscillator (QCCO), and stacks the QCCO on the band's switching circuit. The design is fully balanced and symmetrical, with both mixers switched in a balanced mode, resulting in good isolation between RF inputs and the LO. By reducing LO leakage to -70 dB, self-mixing is kept to a minimum, and problems with unwanted dc offset are virtually eliminated.

Getting Ready For FPLMTS

Not all the wireless high technology is going on in space. Even as the first generation of digital cellular and PCS systems are beginning to

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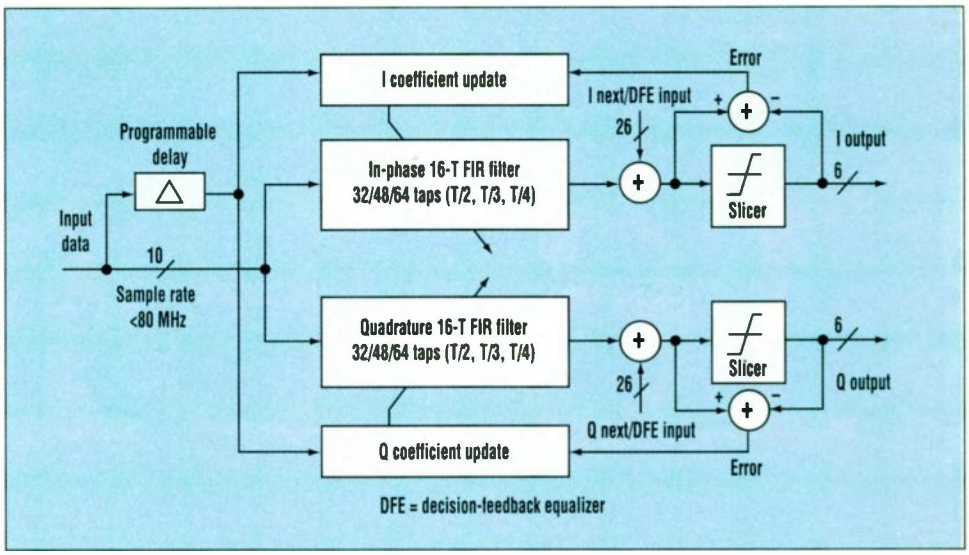
roll out, plans are being made for a more advanced universal wireless data/voice/multimedia system soon after the turn of the century. Known as FPLMTS (Future Public Land Mobile Telecommunication Systems), it is envisioned as a group of seamless services that will provide everything from paging and videophone services to high-speed Internet access.

One of the many challenges faced by FPLMTS will be to find a modulation scheme that is robust, able to support high data rates, and ready to handle subscriber densities approaching the wired-phone system. Direct-sequence, code-division multiple-access (DS-CDMA) is one of the most promising modulation schemes for FPLMTS because it enjoys exactly these attributes. In Session 6, "Low Power and Mixed Signal Processing," a team of researchers from Sharp Corp., Nara, Japan, detailed the design of a "Matched Filter for DS-CDMA of up to 50 Mchips/s" (paper 6.6). Based on sampled analog signal processing the circuit consists of a low-power matched-filter correlator that can acquire DS-CDMA signals. The filter calculates a cross-correlation between an input signal and a filtering coefficient that was originally used to modulate the signal.

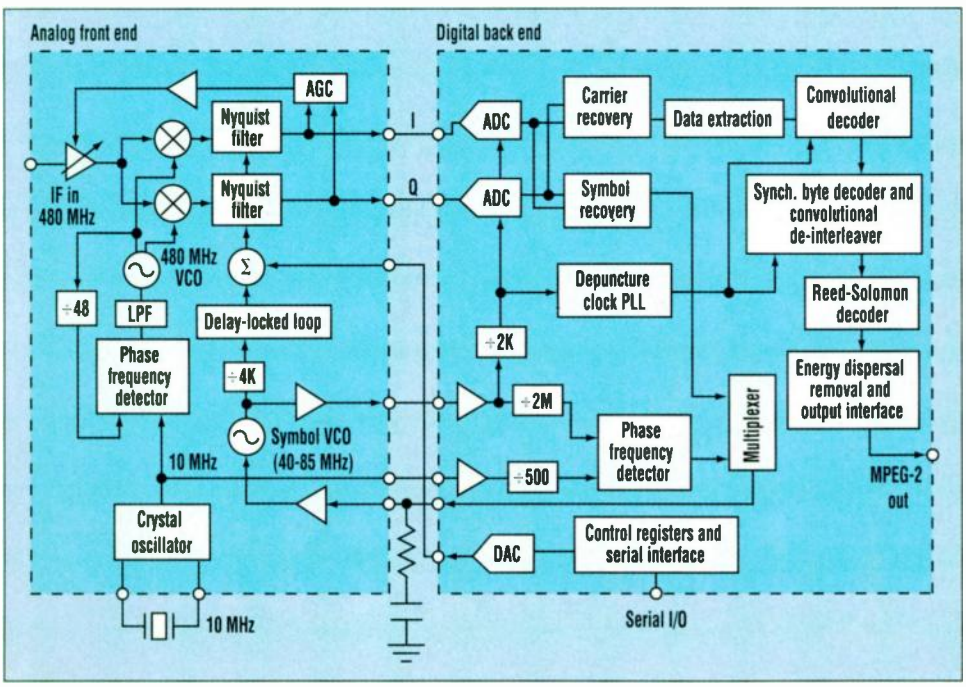
The filter has an array of sample-and-hold amplifiers that sample the incoming signal at regular intervals. The samples are then summed in an adder with parts of the pseudo-random spreading sequence to calculate a correlation value. Careful timing of the sample-and-hold amplifiers triggering and charge refresh rates were critical elements of the filter's design. Also, a compensating circuit was developed to eliminate the offset of the filter's inverting amplifier that normally occurs due to variations in the manufacturing process.



2. A low-power 128-TAP digital adaptive equalizer was developed by Lucent Technologies to combat the noise and multiple reflections encountered by high-speed data on unshielded twisted-pair (UTP) copper wiring. It has a programmable fractional frame capability, enabling it to receive both 51 and 155 Mbit/s signals over Category-3 UTP.

An increasing demand for bandwidth in LANs also has been a significant technology driver. While fiber optics is clearly the future, much effort is still being devoted to helping the bulk of today's networks make the best use of their existing copper infrastructure. At this year's ISSCC, important developments in both these areas were evident.

In the area of high-speed copper networks, a team from Lucent Technologies, Holmdel, N.J,. presented "A Low Power, 128-Tap Digital Adaptive Equalizer for Broadband Modems" (paper 6.3). It describes a fractionally-spaced feed-forward linear equalizer that compensates for the poor transmission characteristics of Category-3 twisted-pair wiring and performs the matched filtering required for symbol detection. The circuit



1. This 480-MHz QPSK demodulator designed by Analog Devices segments its digital and analog functions onto two separate chips for best performance and cost.

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provides programmable fractional frame spacings and slicers that allows it to receive both 51 Mbit/s and 155 Mbit/s ATM, as well as Fast Ethernet signals over inexpensive Category-3 wiring.

The filter's main section consists of a pair of parallel 64-tap adaptive finite-impulse response filters which serve to extract the signal's I and Q components *(Fig. 2)*. Filter coefficients are continuously updated via a decision feedback equalization loop while the filter's programmable delay and timing features permit it to work with a wide variety of data rates. On-chip slicers permit slicing of up to 8-by-8 constellations. A reduced constellation is used for blind training and then the circuit switches to the full constellation for full convergence.

In a related development, NEC Corp.'s Microelectronics ULSI Research Laboratory, Tokyo, Japan, will detail a paper "A 3.3-V 51.84 Mbit/s 16-CAP Transceiver LSI for ATM LANs" (paper 15.2). The authors present a low-voltage, low-power single-chip transceiver that employs carrierless amplitude phase (CAP) modulation to transmit high-speed data over voice-grade wiring.

AP has long been advocated for LANs, several problems have prevented its widespread acceptance. Among the more significant is the high power requirements of earlier 5-V CAP transceivers. Also, the large amount of analog circuitry required to implement CAP has been less amenable to high-level integration than other more digital-based technologies.

These problems were solved by developing high-speed biCMOS analog circuits that operated comfortably at a 3.3 supply. The building blocks included an analog-to-digital converter (ADC), a digital-to-analog converter (DAC), and a clock-recovery circuit. In designing the transceiver, MOS and CMOS circuit structures were used wherever possible to conserve power, while bipolar technology was employed for tasks requiring either very high speed or linearity.

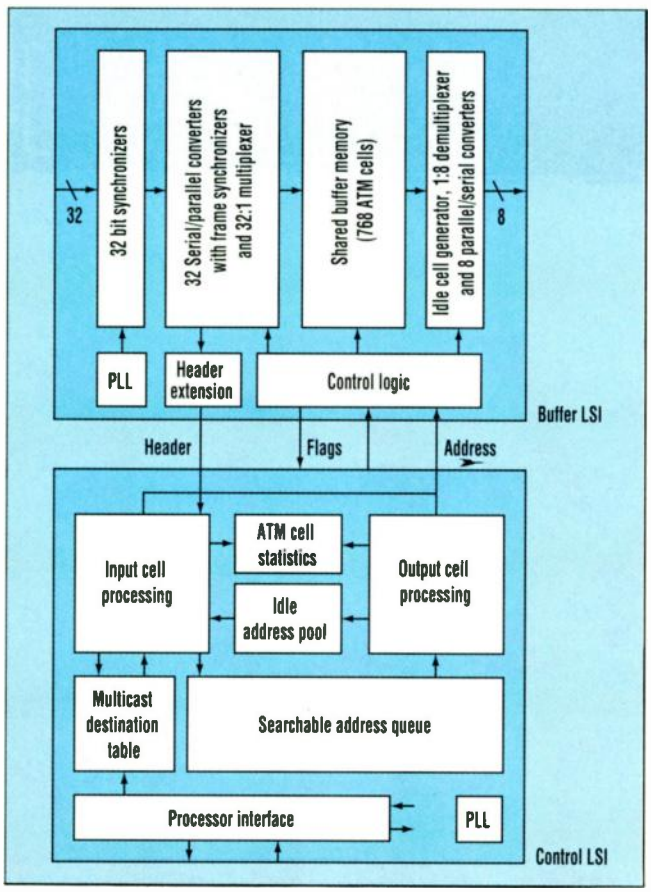
Among other notable features, the chip sports a biCMOS analog multiplier that serves as a variable-gain amplifier for the AGC circuit. Instead of the conventional Gilbert cell multiplier, the NEC design uses parallel-induced circuits based on MOS current mirrors, allowing a wider dynamic range—even at reduced operating voltages. Implemented in 0.35-µm biCMOS with triple metallization, the chip is anticipated to be relatively inexpensive to produce. This is in part because of the chip's small size of just 6.2-mm on a side, plus the biCMOS process does not employ a costly epitaxial layer growth step.

There was much activity in the area of optical networks too, as evidenced by papers like "A 3.3-V, 50-Mbit/s CMOS Transceiver For Optical Burst-Mode Communication," (paper 15.4) presented by members of Nippon Telephone and Telegraph's (NTT) System Electronics and Opto-Electronics Laboratories, Kanagawa, Japan. The two-chip set was designed for providing low-cost termination of an optical connection to a home or small office, and receiving and sending 1.3-µm ISDN data and voice traffic. To avoid stability problems common to high-gain, high-frequency applications, a two-chip architecture was employed,which segments the transceiver into a pre-amplifier with 30 dB of gain, and an AGC amp providing an additional 46 dB of gain.

To obtain the high frequency performance required from a CMOS process, the team employed an instantaneous-response amplifier designed with a feed-forward network. The chips were designed to be self-biasing and self-compensating for process-induced parameter variations to eliminate the need for in-circuit adjustments during manufacture.

Parallel optical networks were also a hot topic at this year's conference--Both IBM Corp.'s T.J. Watson Research Center, Yorktown Heights, N.Y.; Ericcson Microwave Systems, Mondal, Sweden, in conjunction with Linkoping University, Linkoping, Sweden; and NEC's Opto-Electronics Research Laboratories, Kawasaki, Japan, have written papers describing their work in this field in Sessions 15, 9, and 7, respectively. The NEC team's paper, "A 1 Gbyte/s 8-Channel Array OEIC with SiGe Photodetectors" (paper 7.3), describes an 8-channel detector array that was fabricated on a single silicon-germanium (SiGe) optoelectronic integrated circuit (OEIC)

One novel aspect of the detector array is the detectors themselves--they are vertical-cavity, P-i-N SiGe/Si devices built with a bonded silicon-on-insulator substrate



3. This 32-by-8 ATM switch, designed by Mitsubishi Electric, employs a shared buffer architecture plus a dynamic address and priority management system to achieve throughputs of up to 5 Gbits/s.

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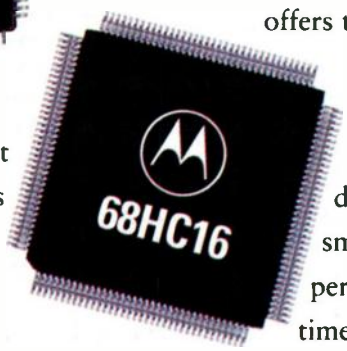

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using SiGe selective-epitaxial-growth technology. To eliminate external coupling capacitors, the preamplifier and limiter circuits are dc coupled using a special offset-voltage compensation circuit.

A special mirror/integrator circuit is employed in the offset circuit. That mirror circuit helps create the large integration time constant required with the relatively small capacitance values available from on-chip capacitors. Drawing 95 mW per channel, the detector was able to receive 0.98-(μm laser light, modulated at 1 Gbit/s per channel (1 Gbyte/s total) with an error rate of $1x^{10-9}$ at a signal strength of -10.4 dBm.

IBM's presentation, " A 500 Mbit/s/Channel, 20-Channel CMOS Laser Diode Array Driver For A Parallel Optical Bus" (paper 15.7) describes a single-chip, 20-channel device intended to drive a vertical-cavity surface-emitting laser diode array in a parallel optical bus transmitter. It has a 500 Mbit/s low-voltage differential signal (LVDS) input interface and a total throughput approaching 10 Gbits/s.

To save power, the driver can be clocked at 250 MHz as well as at its full 500-MHz speed. Other features include on-chip data scrambling and built-in link self-test. One of the interesting features of the driver chip is its LVDS receiver stage, which has both an NMOS and a PMOS block to allow it to detect the incoming signal with a wide input common-mode range. The current outputs of both blocks are summed into two self-cascode-biasing stages, converted to a differential voltage, and passed to a pair of inverters for final amplification. Using a standard 3.3-V supply, it draws only 1.6 W.

In their presentation, "A SONET/SDH Regenerator Framer In 0.6-μm CMOS" (paper 9.4), researchers from Ericcson Microwave and Linkoping University argue that using SONET/SDH becomes an attractive alternative to Fibre Channel or Gigabit Ethernet at extremely high data rates. The paper describes their regenerator framer circuit which takes 16 channels of 622 Mbit/s (OC-12) data and byte-interleaves them into a 16-bit parallel STM-64/OC-192 signal.

In addition to regeneration, retiming, and reshaping, the chip monitors the link's status for things like bit-error rate, and passes the information back to its host controller for analysis. What distinguishes this device is that it is fabricated in CMOS, rather than the bipolar processes previously used. Employing true single-phase clocked (TSPC) logic throughout, the regenerator enjoys a low error rate and consumes only 1.4 W.

ATM—Still A Hot Topic

Despite persistent rumors of its demise, ATM is far from dead, and if ISSCC is any indicator, it is still expected to be a major player in the field of high-speed LAN and WANs. To bring down the cost of ATM connections, engineers from Toshiba Corp.'s Microelectronics Engineering Labs, Kawasaki, Japan, developed a single-chip, 4-channel, 155 Mbit/s, SONET/SDH framing and clock/data recovery chip described in paper 9.6. Intended for terminating multiple STS-3c ATM connections in switches, routers, and other network equipment, each port also can be independently configured to support 51 Mbit/s and 25 Mbit/s connections. Clock recovery is handled by four independent on-chip PLLs.

ATM switching also appears to be a fruitful area of research this year, with many interesting papers presented in Session 9. Among the more intriguing topics is the discussion of the "Throttled-Buffer ATM Switch Output Control Circuitry With CAM-Based Multicast Support" (paper 9.2), presented jointly by The University of Toronto, Canada, and Nortel Semiconductors, Ottawa, Canada. To alleviate the congestion experienced by switch architectures employing linked-list or FIFO-based shared buffers, a CAM-based buffer was developed. This approach tags incoming cells with a unique combination of sequence number and multicast identifier (MCI). A fast tag-CAM is used to search for these identifiers, allowing a throughput of up to 47 Mcells/s to be achieved in a prototype test switch.

Also of note is "A 622 Mbit/s 32-by-8 Scalable ATM Switch Chip Set with On-Chip Searchable Address Queue" (paper 9.1), presented by a team of researchers from various portions of Mitsubishi Electric Corp., Itami, Japan. The chip set consists of buffer LSI and a control LSI, with a 768-cell on-chip buffer that is controlled by a searchable address queue *(Fig. 3)*.

Capable of supporting a 5 Gbit/s throughput rate,the switch has eight levels of cell delay priority and four levels of cell loss priority for multimedia applications. A funnel structure enables the switch architecture to be scaled upward. Massive parallelism and multiple data paths are employed within the architecture to keep signal speeds within the limits of its CMOS devices.

Gigabit Rumblings

Gigabit Ethernet and its parent Fibre Channel technology also attracted substantial attention at the conference. In "A 1.0625 Gbit/s Transceiver With 2x-Oversampling and Transmit Signal Pre-Emphasis" (paper 15.1), engineers from LSI Logic Corp., Milpitas, Calif., describe a Fibre Channel-compliant serial interface logic core that can be used as a standard cell in ASIC or semi-custom applications. It integrates all transceiver functions, including data serialization, clock/data recovery, and at-speed self-test functions. A 2x oversampling technique is used to ensure solid data recovery, even under non-ideal line conditions.

Direct support for Gigabit Ethernet is beginning to mushroom, even before the standard's fine print has dried. In "A 1.25 Gbit/s, 460 mW CMOS Transceiver For Serial Data Communication" (paper 15.3), a development team from Symbios Logic, Fort Collins, Colo., detailed a low-power standard-compliant transceiver capable supporting Gigabit Ethernet traffic at either 1.2 or 1.25 Gbits/s. Its small size and low power consumption opens up the possibility of integrating more than one transceiver on a single chip for use in multiport applications, such as switches and routers.

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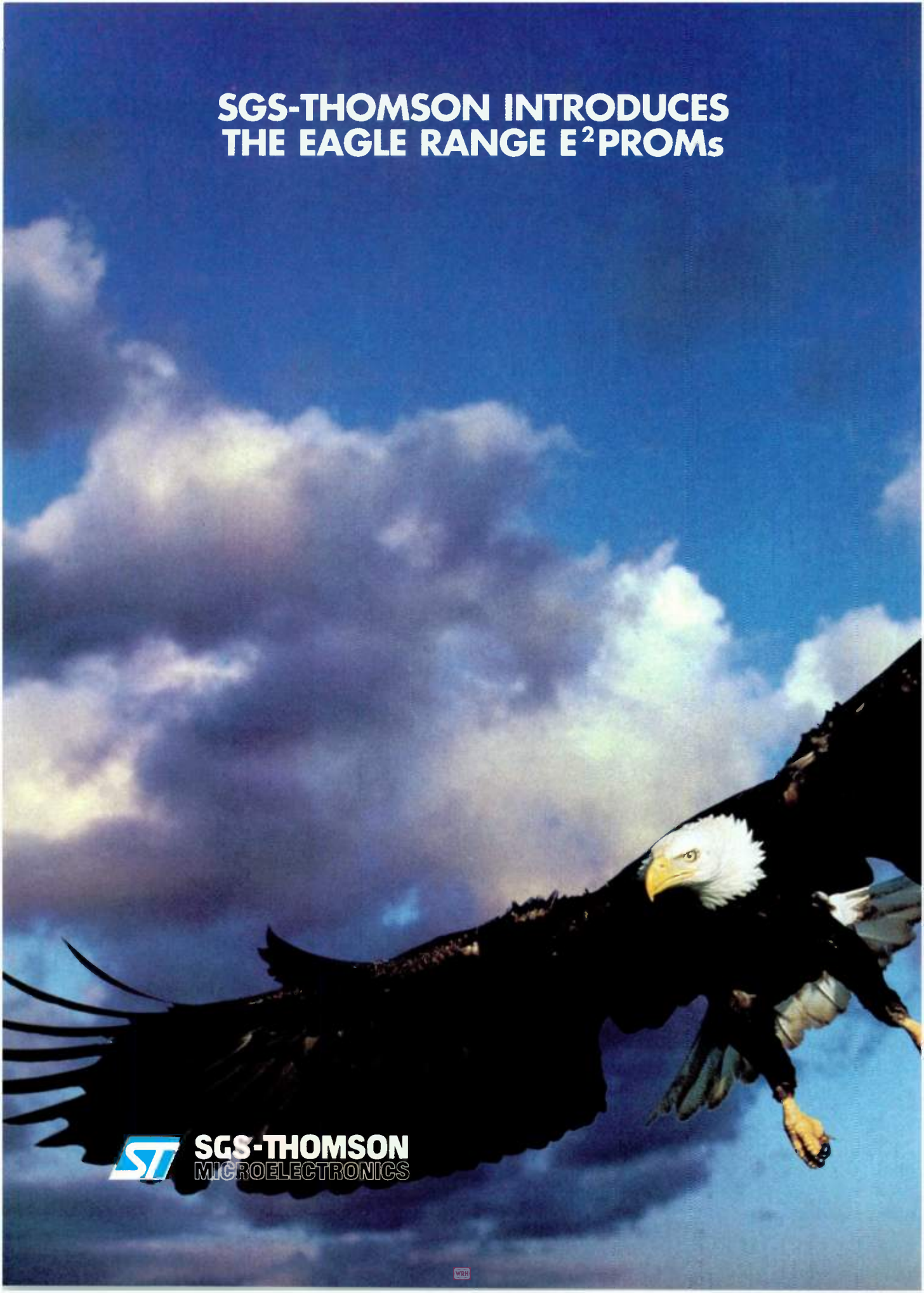

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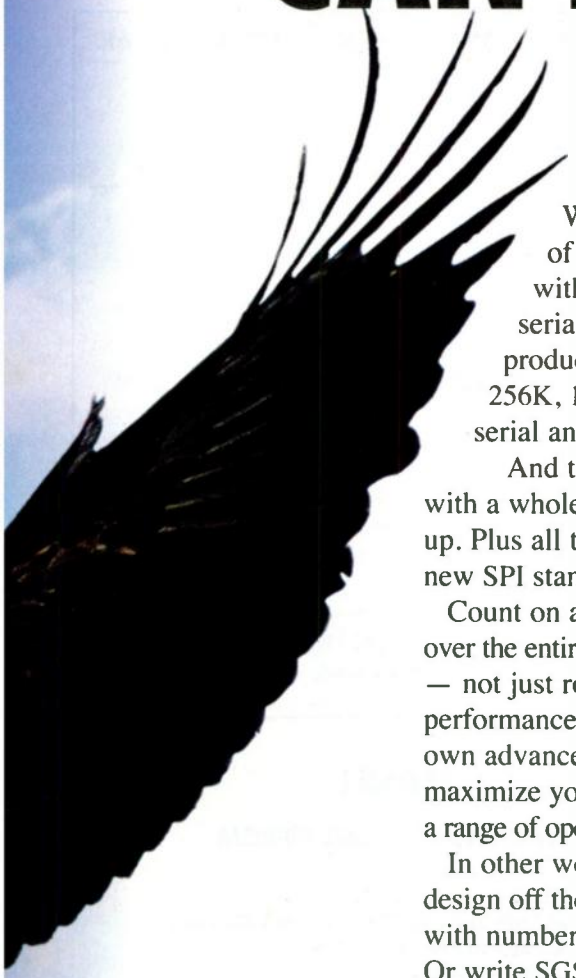

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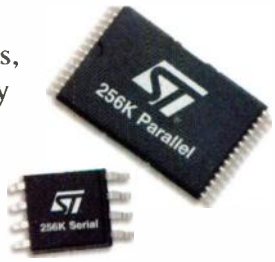

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Consumer Products Drive Sensor/Display Developments

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SPECIAL REPORT

Driven by the growing demand in machine vision, multimedia, portable consumer (digital still cameras), and other applications, research to produce better, lower cost image sensors, imagers, and displays has made significant progress. The papers presented at this year's ISSCC show some of the fruits of the research with devices that offer reduced power consumption, high resolution, high frame rates, and reduced system weight.

For example, research in the area of active pixel sensors (APS), has received much attention because the approach allows designers to integrate all the controlling, driving, and signal processing circuitry on the same chip as the sensing array. Although such a chip is attractive in many respects, one feature, the large pixel size in the sensor array, has hampered the chip's incorporation into consumer-based applications such as digital still photography.

Until now, the sensor's pixel size has been completely dependent on the size of the row select, charge reset, and amplification elements in a pixel. Thanks to a development from Toshiba Corp., Kawasaki, Japan, that the company described in Session 11, the pixel area now can be reduced. The improved sensor, as highlighted in the paper entitled "A 1/4-in. 330k Square Pixel Progressive Scan CMOS Active Pixel Image Sensor," is configured as a 1/4-in., 640-by-480-pixel, active-pixel array, and is based on a transistor address cell structure. Toshiba designers were able to reduce the individual pixel size to just 5.6 by 5.6 μm^2. Fabricated using a 0.6-µm, double-poly-silicon, triple-metal CMOS process technology, with both the color filter array and micro lens formed directly on the sensor, the imaging array is powered by a single 5-V supply and dissipates less than 30 mW.

The key factor in the pixel's decreased area is the unique structure of the pixel cell. The transistor-address-type structure, devised by Toshiba, consists of three devices: a select transistor (SL), a source follower transistor (SF), and a reset transistor (RS). The SL transistor activates the source follower, and addresses the selected line. A timing chart of the cell structure is made by switching on the SL to enable the RS transistor to discharge the photodiode.

In addition to the new cell structure, the sensor chip incorporates an innovative zigzag layout in which the even columns and the odd columns are all shifted by half a pitch, alternating in the vertical direction (*Fig. 1*). This format is needed to accommodate the use of square pixels; a must for multimedia applications.

Current-Mode APS Research

Also focusing their efforts on developments in theAPS arena, researchers from the Polaroid Corp., Cambridge, Mass., and Northeastern University, Boston, Mass., have developed a current-mode APS based on a current-reset approach. This scheme provides an alternate architecture to the more conventional type of voltage-mediated, source-follower APS devices. Detailed in the second paper of Session 11, "Current-Mediated, Current-Reset 768-by-512 Active-Pixel Sensor Array", the design not only significantly reduces fixed-pattern noise due to FET performance variations, but offers additional benefits as well. The array can be fabricated in a digital CMOS technology with far fewer FETs in the pixel and readout, fewer bus lines strapping the array, and less clocking required for operation, than was previously possible.

The APS CMOS image sensor contains an array of 768-by-512 15-μm^2 pixels. Typical device operation is 2 frames per second with integration times ranging from 1 to 500 ms (at a 5-V bias and clock, and a 120-µA reference current). The circuit contains an array of pixels with both reset and select signals connected along rows, and signal lines connected along columns. Each pixel sensor is composed of an NMOS dynamic-current mirror with a current-reset, photodiode-integration node located in each pixel. As explained by R. Daniel McGrath, one of the researchers of the develop-

ment, "a reset FET at each pixel diode-connects the active FET so that the gate charges to the voltage necessary to sink a reset current driven on the column bus. Turning off the reset FET forces the active gate capacitance to store this voltage, thus memorizing the reset current. Photogenerated charge collects on the integration node, decreasing the voltage and lowering, approximately quadratically, the output current when the pixel is read out. Turning on the select FET, with the reset FET off, allows the pixel current to be read out via the column bus." This current-reset process, effectively reduces the fixed-pattern noise by compensating for the threshold voltage variation that exists between pixels of the active FET.

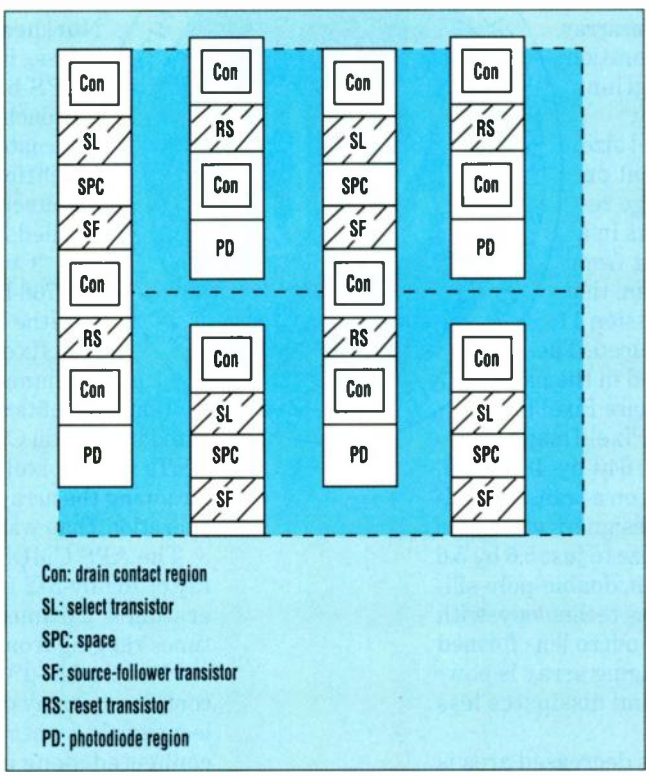
While the pixel structure enables the device to more robustly withstand manufacturing process-induced variations in a digital process, it does so with one catch—an increase in the power consumption during current reset. Ongoing work on the device is aimed at reducing power, further improving performance, and scaling the process technology.

Active pixel image sensors are not the only option for use in digital still cameras and digital video applications. A 4-Mpixel charge-modulation device (CMD) image sensor developed by the Corporate Research Division of Olympus Optical Company Ltd., Nagano, Japan, was presented in Session 11. The sensor has been specifically developed with skip-and-block access modes for utilization in real-time framing and focusing with digital still cameras. These modes are especially handy when the sensor is employed in systems that inspect products such as large-format LCDs. Such a task typically requires a wide field of view and the ability to make precise observations of specific areas. These requirements are now met by the CMD sensor.

The CMD sensor packs a large pixel count, roughly 2048 by 2048 elements, each measuring 7.5 by 7.5 μm; three scanning modes, a full-readout mode, a block-access mode, and a skip-access mode; and generates very low levels of dark current *(Fig. 2)*. The full-readout mode delivers high-resolution images from the device in a single readout cycle. The block-access mode, on the other hand, provides a readout of any arbitrary window of interest. The skip-access mode reads every fourth pixel in horizontal and vertical directions.

Both the block- and skip-access modes allow for real-time monitoring of a partial and a whole image. Electronic zooming and panning features, with moderate resolution, also are possible with this image sensor device, and do not require the use of any mechanical parts.

The sensor consists of an array of CMD transistors, horizontal and vertical scanners with on-chip drivers, and a clock controller. Dark current generation is reduced through the use of a voltage-difference switching circuit, while the use of a single-output-channel design greatly simplifies the signal processing circuitry. Realization of all three readout modes is possible with the implementation of a shift register in both the horizontal and vertical registers. The horizontal scanner operates from a 12-MHz clock that has a 3-V signal swing. Embedded clock buffers allow conventional CMOS logic circuits to drive the sensor.



1. The tight physical layout of the zigzag cell illustrates the simplistic approach developed by Toshiba. The shifting of the even and odd columns is required to accommodate the transistor address type cell structure within a square pixel.

Image Sensors In Multimedia

For multimedia applications, a joint effort on the part of ULSI Device Development Laboratories and the Microelectronics Research Laboratories of NEC Corp., Tokyo, Japan, has resulted in the development of a 30 frame per second (fps) 2/3-in., 1.3-Mpixel, progressive-scan, interline-transfer (IT) CCD image sensor. By comparison, most conventional 1.3-Mpixel progressive-scan CCD image sensors only offer frame rates of roughly 10 fps. Also presented in Session 11, this device makes use of a technique called an optimized well structure for the horizontal CCD (H-CCD), and a wide-bandwidth amplifier to achieve 49-MHz operation. A variety of other operations such as 1050-line progressive mode and 1049-line wide-dynamic-range interlaced mode are possible through the implementation of an 8-phase drive for the vertical CCDs (V-CCDs).

The sensor contains an array of 1308-by-1032 active pixels, each 6.7 μm^2, and is applicable to both 5:4 aspect 1280-by-1024 progressive scan, and 4:3 aspect ratio 1294-by-970 pixel interlaced-scan systems. Designers also incorporated a unique feature into the sensor's design, a method for removing residual charges stored in the V-CCDs of a digital still camera prior to exposure. To remove the charge, a newly-developed narrow-channel-barrier overflow drain (NCB-OFD) is simply attached under the H-CCD. During the sensor's operation the NCB-OFD automatically drains out extra charges. This particular drain structure was chosen because it does not require an overflow-control gate or any additional masks.

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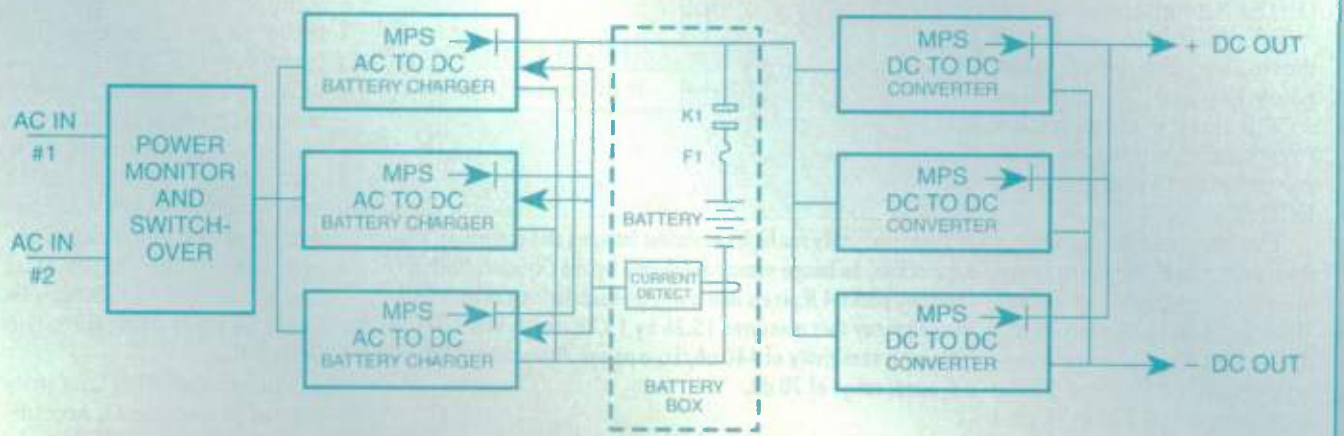

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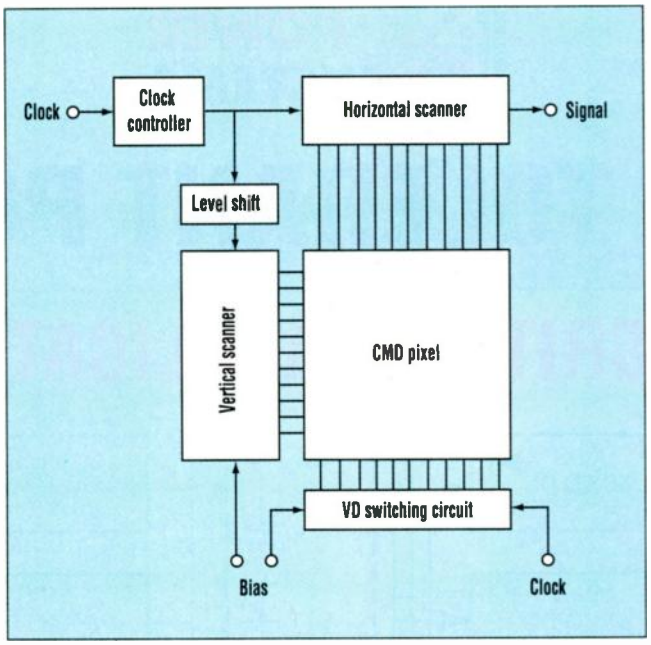
early vision-processing problems, an interesting development described in Session 2 comes from researchers at the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, Mass., in conjunction with Maxim Integrated Products Inc., Sunnyvale, Calif. The development, a custom analog VLSI chip, can compute the focus of expansion (FOE) (the image point toward which the camera is moving and from which other points expand). The chip uses a CCD imager along with a row-parallel, analog-processing scheme to estimate the FOE *(Fig. 3)*.

The sensor, which packs a 64-by-64 pixel imaging array, operates at a high frame rate, 1000 fps, providing rapid updates for the analog-processing section. At that speed, the chip consumes 170 mW, and has an accuracy of 3%. The chip is fabricated using a double-poly, buried-channel CCD biCMOS process and measures just 9200 by 7900 µm.

The FOE calculation provides useful information about the direction of the camera's motion—information that is vital for higher-level vision processing. The image processor's architecture, which enables this computation to take place, consists of an interline-CCD imager, an array of floating-gate amplifiers, a column of analog-signal processors, and a position encoder. Due to the computational complexity, a row-parallel processing scheme was chosen, as opposed to the more conventional pixel-parallel approach.

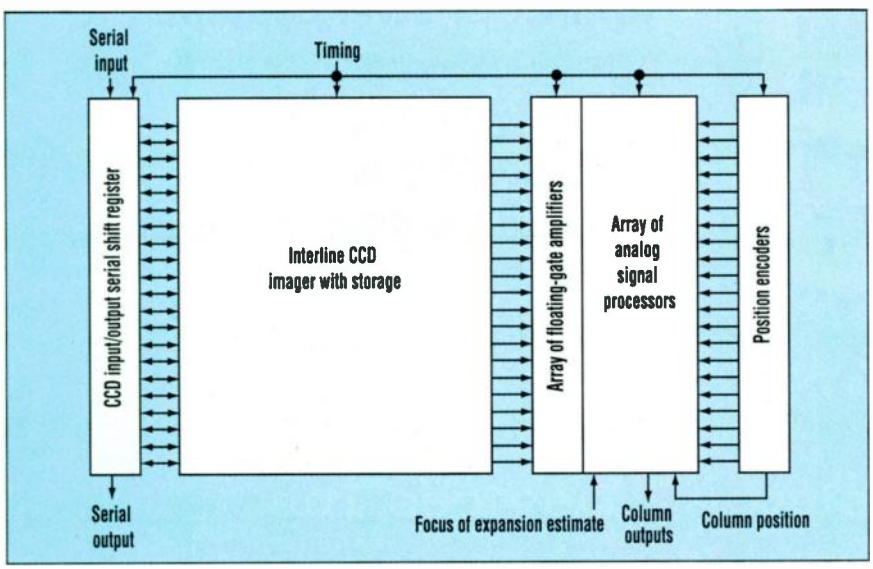


2. Built specifically for high-resolution imaging and machine-vision applications, an image sensor developed by the Olympus Optical Company packs 4 Mpixels into a charge-modulation-device-based imaging array that measures 15.36 by 15.36 mm. Additionally, the chip features a sensitivity of 440 nA/lx, a power dissipation of 90 mW, and a dynamic range of 70 dB.

Another interesting development, while not in the area of pixel sensors, comes from a joint effort on the part of the Toshiba R&D Center, and the Toshiba Semiconductor System Engineering Center. The development, called a dynamic-function shuffling technique for a new thin-film-transistor (TFT)-LCD panel driver IC is specifically aimed at cutting the typically high-power consumption of driver ICs. Most of the power in a display subsystem is consumed at the video signal input lines of the driver ICs, and at the TFT-LCD panel's vertical lines driven by the driver ICs.

The proposed IC, as presented in Session 11, accepts the three parallel analog RGB signals and feeds them to 38 groups, each consisting of a pre-shuffle stage, a post-shuffle stage, and nine function units. Each function unit comprises a sample-and-hold (SH) stage and a gain stage. A shift register generates the sampling signal for each SH stage. The pre-shuffle stage consists of 9-by-9 NMOS cross-bar switches, and the post-shuffle stage consists of 9-by-9 CMOS cross-bar switches.

A 0.6-µm dual-aluminum, single-poly-CMOS process is used to fabricate the chip, which measures 17.1 by 2.4 mm. Each of the 38 groups on the chip contains a 360-by-250-µm logic circuit, a 360-by-106-µm pre-shuffle stage, nine 40-by-500-µm SH stages, nine 40-by-530-µm gain stages, and a 360-by-123-µm post-shuffle stage. For the analog circuits the power supply can range from 3.3 to 5 V, while it is set at 3.3 V for the digital circuitry. The chip offers a total of 342 outputs to drive the vertical lines.



3. An analog image processor fabricated in biCMOS technology and designed to perform focus-of-expansion computations has been developed jointly by the Massachusetts Institute of Technology and Maxim Integrated Products. The chip architecture consists of an input-serial-shift register, an interline-CCD-imaging array, an array of floating-gate amplifiers, an array of analog signal processors, and a position encoder.

How Valuable	Circle
Highly	540
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Slightly	542

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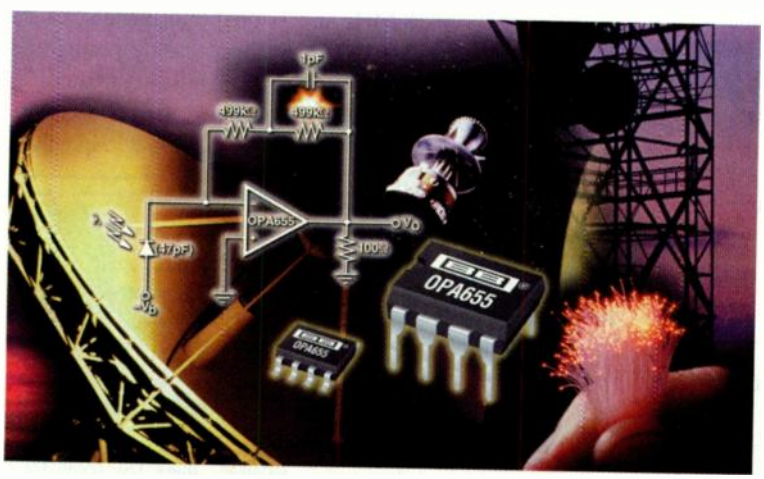

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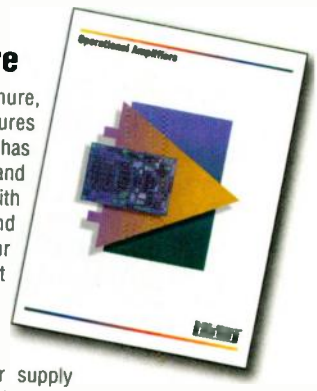

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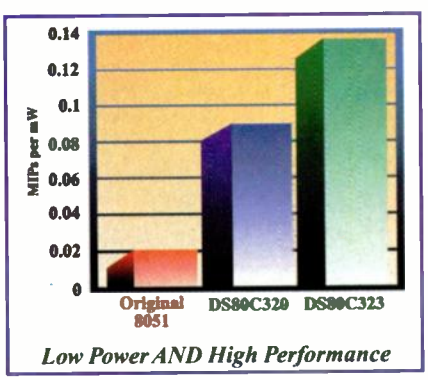

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1-V OP AMP

Op Amp Supply Squeezed Down To 1 V Rail-To-Rail

A Revolutionary Device With A Swing Within 30 mV Of The Supply Rails Opens The Door To A Massive Change For Analog Design.

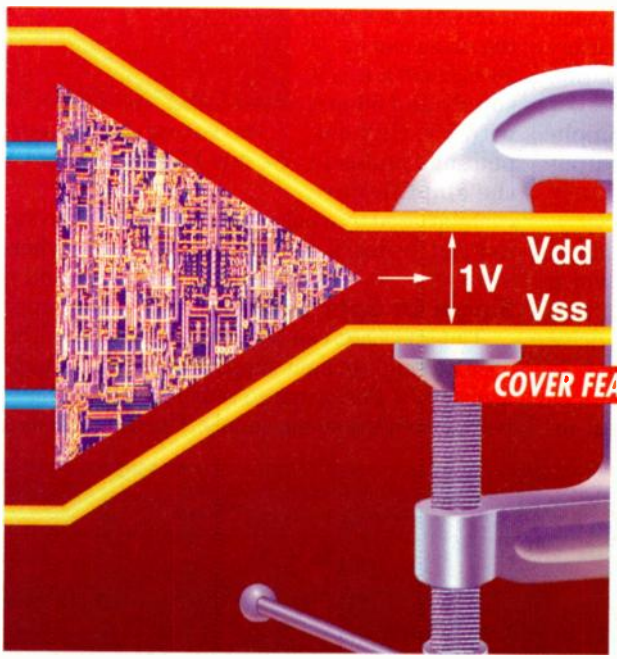
Paul McGoldrick

A new semiconductor product has been produced that, according to its designers, offers a simple and wide-ranging solution to what was once thought of as an impossible problem to solve. In fact, the development could be described as "revolutionary."

This is the scenario with the Motorola MC33502 dual operational amplifier, which can be described, succinctly, as providing rail-to-rail operation on both the input and output with supplies as low as 1 V.

Why such excitement over an op amp? Up until now, the lowest supply voltage for operational amplifier devices has been in the 1.8-V range. Because of the continuing demand for portable products, the pressure for lower-voltage operation has increased. While some products will take advantage of this technology's ability to operate from a single-cell, many more will continue to use multiple cells but with dramatically extended battery life. A standalone "ground-sensing" device like the MC33502, with both decent gain and speed, will open up a whole plethora of other products for which the op amp is a cornerstone.

Operation of the MC33502 at higher supply voltages is not sacrificed and can be as high as 7.5 V. The IC achieves a unity-gain bandwidth exceeding 4.8 MHz. The performance changes between 1-V and 5-V operation are quite minor.



COVER FEATURE

A New Architecture

Attempts have been made to operate op amps at lower supply voltages, with just about every terminal on a FET being controlled. The lowest operating voltage at the present time has been achieved with bipolar devices, with a 1.8-V on-voltage. The CMOS vo;ltage is intrinsically higher at 2.5 V or more.

Motorola's solution is to use depletion-mode devices, which are, of course, already on at 0 V and which will smoothly switch to enhancement-mode as the voltage increases. The technology uses n-channel MOSFETs employing Motorola's SMARTMOS fabrication process with vertical pnp and high-frequency npn devices.

The n-channel devices have a higher transconductance than p-channel devices and offer higher-speed operation for the same drain currents. In addition, with tighter process controls, thinner oxides, and buried channels, the noise corner frequency and flicker noise are now low enough for them to be used in most signal processing circuits. Most 1/f noise is produced at the Si-SiO interfaces, and with the changes overall noise is improved by a factor of three to give production-device noise levels of 40 nV/√Hz (at 1 kHz.)

The n-channel differential input pair of ion-implanted, negative-threshold, NMOS devices allows for the low-voltage operation because the normal common-mode range includes ground *(Fig. 1)*. The body effect shifts the threshold positively as the gates are moved positive from ground; the body-effect coefficient is high because of the highly-doped p-well (the coefficient is proportional to the root of the doping richness) and it ensures that the input stage remains saturated at the supply rail. (Correspondingly, the drain is lightly doped to give a reasonable breakdown voltage.)

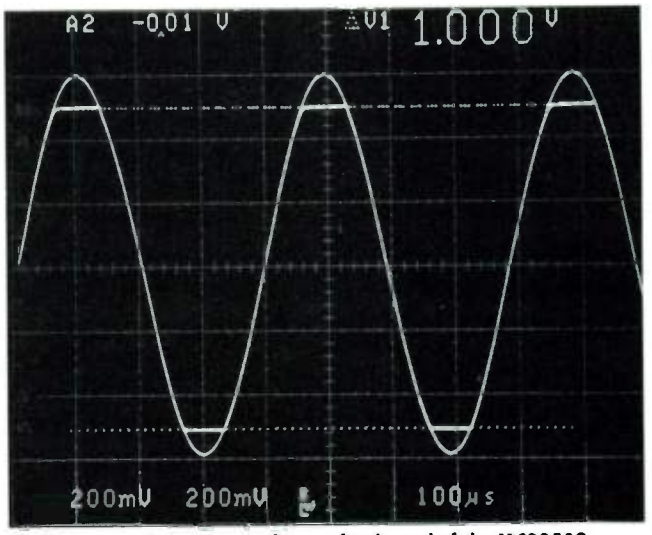
The input stage is a folded cascode, which uses high-impedance current mirrors to provide high gain. These current mirrors must cancel any unbalance, and therefore an increased input offset voltage, due to base current errors. A low-voltage—down to 900 mV—balanced mirror circuit was developed to provide high stage gain and cancellation as the more conventional current sources require two junction voltages, and could not therefore be used in this design. The small compensating voltage is applied to one of the input stage body terminals and reduces the input offset voltage to less than 500 µV.

The output from the input stage is taken off at high impedance, but the signal path must be kept at low imped-

ance in order to maximize the ac performance, maintain speed, and ensure the development of minimal voltage gain before the output stage. To isolate the input and output (to prevent the output from loading the input and changing the dc balance of the cascode stage), a depletion-mode source follower is used biased with an I_{DSS} current source. This scheme replaces the conventional Darlington-type emitter follower configurations to achieve a β^2 or β^3 reduction of the load-current reflections which become impractical with a 1-V supply voltage and which usually require an intermediate differential amplifier stage for the isolation to be complete

An on-demand base-boost amplifier provides base drive to the output npn device, while a complementary circuit drives the output pnp *(Fig. 1, again)*. A buffer amplifier provides a voltage-to-current conversion, which is in direct proportion to loading, with sense transistors monitoring the drive requirements and providing just enough bias for those needs.

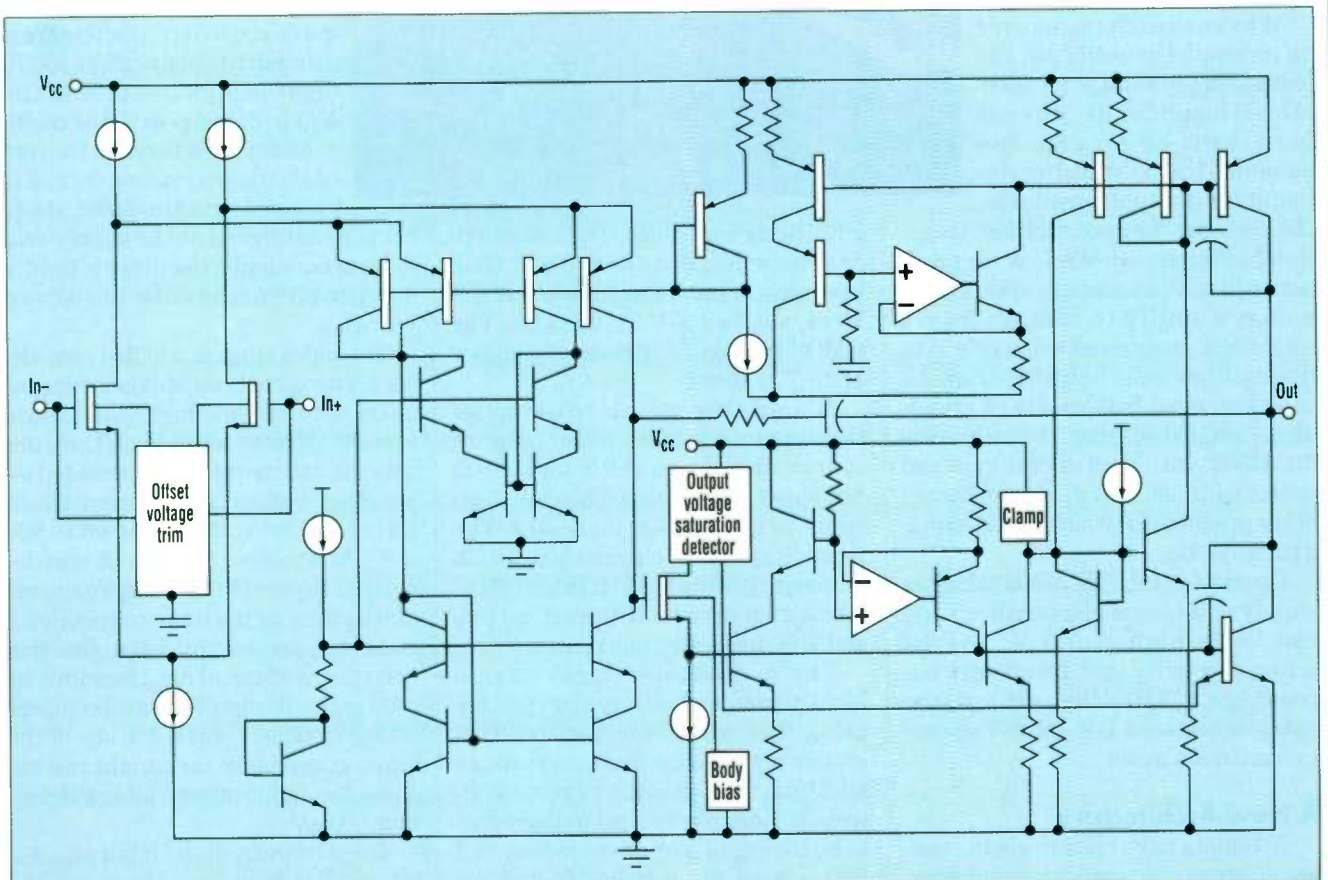
As the demand on the output increases, the emitter degeneration resistors limit the bias current in the amplifiers to that needed to provide the required drive capability. The biasing system is a low-voltage current source This system reduces the quiescent current to just a few microamps while the stage can drive 10 mA with a 1-V supply and 50 mA with 5 V. High-impedance nodes in the amplifier are compensated by a pole-splitting capacitor and feedback resistors.



2. The input and output waveforms of a channel of the MC33502 driven at 1.2 V showing the 1-V rail-to-rail output.

Single Or Split Supply

The MC33502 can be operated from either a single or split supply down to 1 V or ±0.5 V. Performance is marginally better from the single supply. The rail-to-rail performance is clearly shown, where the amplifier is driven by 1.2 V and the output is limited to the 1-V supply *(Fig. 2)*. The output can swing within 30 mV of each rail with a 10-kΩ load. Input current is typically less than 10 pA with a voltage gain in excess of 110 dB, and no phase reversal at



1. This simplified schematic of the Motorola MC33502 dual op amp shows a balanced circuit using biCMOS depletion-mode NMOS devices.

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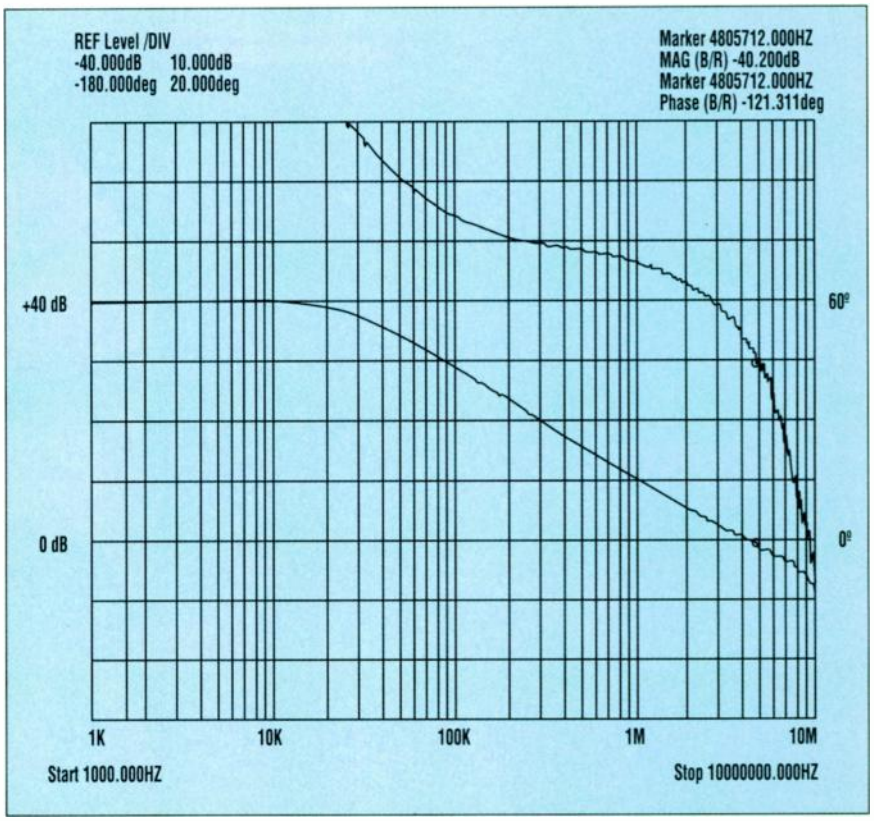

3. The frequency response of the MC33502 dual op amp is shown when operating with a 1-V supply rail and a closed loop gain of 100.

the output when the input is overdriven. Supply current is typically 1.2 mA and the slew rate typically 4 V/μs. With a 5-V supply, the voltage gain increases to 120 dB and the drain current to 1.4 mA. The noise performance at 1 kHz is identical at either voltage, although at 10 Hz the noise worsens marginally from 60 to 80 nV/√Hz when moving from 1- to 5- V.

The frequency response of the amplifier with a closed loop gain of 100 and a 1-V supply shows a unity-gain bandwidth of 4.8 MHz and a 60° phase margin *(Fig. 3)*. With a 5-V supply, the phase margin stays the same but the bandwidth increases to 5.5 MHz.

The thinking behind the design has, according to Motorola, placed the company ahead of the capabilities of other analog IC companies who very well could have come up with a similar solution. Robert Vyne, IC design section manager, and his team have done a considerable amount of analysis of the "what," the "how," and the "what else" that is essential for this kind of breakthrough in any analog design. In this respect, Motorola is in the lead with products already moving through.

The circuit is simple, clean, and utterly elegant in overcoming a major hurdle in the future development of portable products. In fact, in 10 years, the circuit could probably become known as the "Vyne Amplifier."

An operational amplifier is, of course, the fundamental building block of many other devices. This circuit, and varients, will start to appear in other products from the Motorola stable sooner rather than later.

Note: This operational amplifier technology was the subject of a ISSCC paper at the IEEE ISSCC held in San Francisco earlier this month.

Price And Availability

The MC33502 is available in either an 8-lead plastic DIP or SO-8, priced at $0.87 each in quantities of 10,000. Production quantities are available now.

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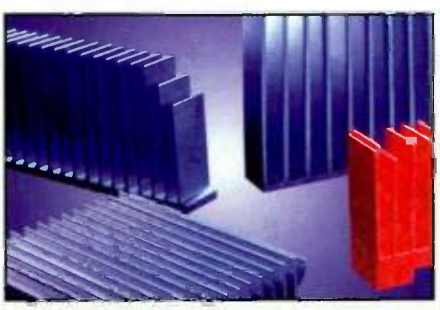

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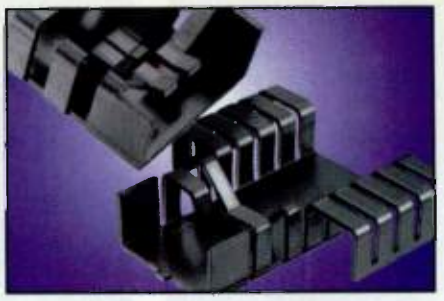

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DESIGN APPLICATION

Deliver Ultra-Low Spurious Levels To Base-Station ADCs

Extremely Low Harmonic Distortion Is The Cumulative Result Of Having Done A Lot Of Things Right.

MICHAEL STEFFES, Burr Brown Corp., Data Div., 6730 S. Tucson Blvd., MS #206, Tucson, AZ 85734; (520) 746-7979; e-mail: steffes_michael@burr-brown.com.

Using analog-to-digital converters (ADCs) with wide dynamic range has enabled significant advances in cellular base-station design. While the converters have improved to where they provide 80-dB spurious-free dynamic range (SFDR) at a 20-MHz Nyquist input, it remains a challenge to deliver an input signal that doesn't degrade this exceptional range. This article will describe a circuit that has been measured to hold lower than 90 dB spurious through 20 MHz for a 1-V p-p swing into a 200-W ADC input impedance.

Extremely low harmonic distortion is the cumulative result of having done a lot of things right. You must begin with a part that has a considerable ac performance margin beyond the intended range of application. For example, given a desired maximum voltage swing and frequency, you would like a part with at least 2X (and preferably 4X) the slew rate beyond what your signal will demand. Slew-rate-limited operation introduces course distortion mechanisms. The desired operating frequency and amplitude should be asking for much less than the op amp's rated slew rate to avoid suffering from these additional nonlinearities.

For an op amp operating in the linear mode (non-slew limited), harmonic distortion is generally determined by the open-loop signal path linearity. Harmonic distortion is then further improved by the loop gain at the fundamental frequency. Consequently, you'd like to have linear open-loop gain stages and as much loop gain as possible at high frequencies (dc open-loop gain doesn't matter as much for ac-coupled applications).

There are current- and voltage-feedback op amps that offer very low distortion. The voltage-feedback topology seems to offer the lowest distortion, while the current-feedback products have reasonable distortion levels that hold up well over a wide range of gains. Current-feedback topologies typically offer higher slew rates than voltage-feedback op amps. Comparable slew rates in voltage-feedback op amps are normally found only in non-unity-gain stable op amps. Some newer voltage-feedback designs overcome this limitation (offering high slew rate at low-gain stability), but only at the expense of much higher input-voltage noise.

For the very-lowest distortion, let's now focus on the voltage-feedback solution. Both the highest slew rates and open-loop gains (over frequency) are found in non-unity-gain stable op amps. As an added bonus, if the higher dominant pole of a non-unity-gain stable op amp was obtained by increasing the input stage g_m, this typically gives a lower input-voltage noise than a unity-gain stable equivalent. The difficulty comes in applying this type of part to an ADC input-buffer application. Low gains are normally required with exceptional frequency-response flatness. The challenge here is to take advantage of the high slew rate, open-loop gain, and low noise found in a low-distortion non-unity-gain stable voltage-feedback op amp—and apply it at low closed-loop gains while controlling the frequency-response flatness and phase linearity.

EQUATION LISTING

$$\frac{V_o}{I_n} = \frac{R_f \| \frac{1}{sC_f}}{1 + \frac{1}{LG}} \qquad (1)$$

where loop gain:

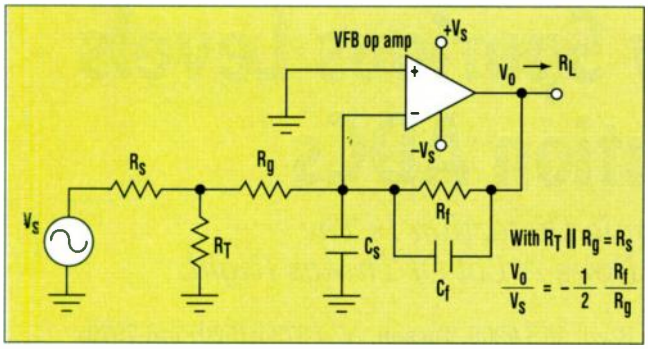
$$LG = \frac{A(s)}{1 + \frac{R_f \| \frac{1}{sC_f}}{R_n \| \frac{1}{sC_s}}} \quad \text{and} \quad A(s) \equiv \text{single-pole op-amp open-loop response}$$

$$A(s) = \frac{A_{OL}\omega_a}{s + \omega_a}, \quad \frac{A_{OL}\omega_a}{2\pi} = \text{Gain bandwidth product in Hz}$$

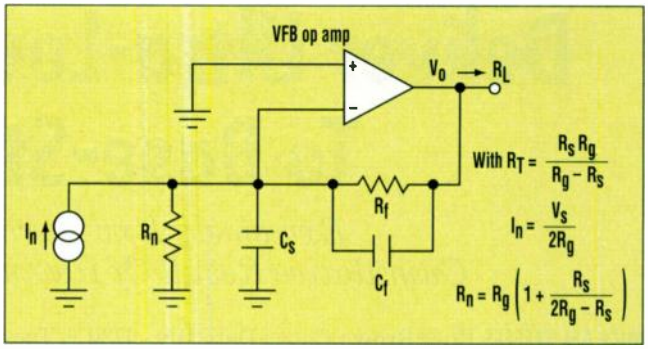
$$P1 = \frac{1}{R_f C_f} = 0.707 \sqrt{\frac{GBW}{(R_f \| R_n)(C_s)(1 + \frac{R_f}{R_n})2\pi}} \qquad (2)$$

$$= 0.707 \sqrt{\frac{GBW}{2\pi R_f C_s}} \quad \text{where } C_f << C_s \text{ is used to drop } C_f \text{ out of Z1}$$

and GBW is the op-amp gain bandwidth in Hz



1. This compensation-analysis circuit is the starting point for the ADC interface design.



2. Using resistor constraints and redrawing Fig. 1 to show a Norton equivalent for the source network gives an equivalent circuit for analysis.

New Compensation Technique

Let's begin with an ADC interface design *(Fig. 1)*. In order to control the signal gain and loop gain separately, the input signal is brought into the inverting input from a source impedance equal to R_s. The inverting configuration offers a number of benefits to this application. First, it's possible to shape the noise gain (by adding C_s) in a fashion that still allows tight control over the signal gain. Second, because there's no voltage swing on the noninverting input, no common mode nonlinearities are introduced that may degrade the distortion. Because the base-station application is a frequency-domain, FFT-based processing channel, the signal inversion (180° phase shift) through this inverting gain stage is incidental to the application.

R_t is included to allow impedance matching to R_s. This was done for the base-station application to provide a 50-Ω match for testing purposes (where R_s is the 50-Ω source impedance of the network analyzer or signal generator). If the previous stage in an application doesn't require the input-impedance match, R_t may be eliminated. Driving into the higher valued R_g as a load will improve the distortion of the prior stage. In this case, $R_t \,||\, R_g$ is set equal to R_s. Using that constraint on R_t and redrawing Figure 1 to show a Norton equivalent for the source network gives a new circuit configuration *(Fig. 2)*.

Figure 2 is starting to look very much like a transimpedance stage. By placing an external capacitor to ground at the inverting input (C_s), we get nearly the same analysis circuit as for a transimpedance amplifier. In a typical transimpedance application where the source is a detector diode and C_s is the parasitic capacitance of that diode, $R_n >> R_f$ and the solution for C_f proceeds assuming the diode's real impedance is infinite ($R_n \rightarrow \infty$).[1] Once C_s has been set (either by the diode or by the external value added for this application), it's then possible to determine the C_f value that will produce a desired second-order response for V_o/I_n. By inspection, the V_o/I_n transfer function of Figure 2 may be written as shown in Equation 1 *(see the equation listing)*.

Equation 1 shows a transfer function for the circuit of Figure 2 that has a gain of R_f at dc with a simple pole in the numerator (at $1/R_fC_f$) and a loop gain in the denominator. The denominator has the dominant open-loop pole of the op amp, along with a zero formed by C_s and a pole at $1/R_fC_f$. Using the analysis discussed in Reference 1, the $1/R_fC_f$ pole may be placed to achieve any desired Q for the closed-loop frequency response *(Fig. 3)*. The figure shows the Bode analysis of the loop gain for this circuit.

The differences between this and a transimpedance analysis is that the low-frequency noise gain is >1 and Z1 is now set by $R_f \,||\, R_n$ instead of just R_f (because R_n is less than infinity). Earlier analysis[1] showed that the ratio of P1 to the geometric mean of Z1 and GBW is about equal to the Q of the closed-loop second-order response. This includes the effect of the simple pole that shows up in the numerator of Equation 1 ($1/R_fC_f$). That result, while approximate, is very good when the dc noise gain = 1. It becomes less accurate as the dc noise gain is increased. The design done here based on this approximation will yield a response with a Q slighty less than targeted.

To use this simplified analysis, divide the op amp's GBW product by the dc noise gain (GBW′) to get an equivalent GBW′ product. And use the Z1 shown in Figure 3 for determining P1. To get a maximally-flat closed-loop response (Butterworth), set P1 to get Q = 0.707. Equation 2 puts all of this together to get a solution for P1 (using radians)

Placing P1 as described in Equation 2 will give us a maximally flat Butterworth closed-loop response for the circuit of Figure1. Even though this analysis is for a non-unity-gain stable op amp, the higher order poles of A(s) may be safely ignored (these are not shown in Figure 3).

Looking again at the Bode plot, even though $(1+R_f/R_n)$ may be at a gain that is unstable for the op amp's selected loop gain, crossover actually occurs at a much higher $(1+C_s/C_f)$ noise gain. This loop-gain shaping gives us higher loop gains (and hence improved distortion) at low frequencies, and takes us back to stable performance at

TABLE 1: HARMONIC DISTORTION FOR FIGURE 7

	Without dc trim		With V+ = 0.55 V	
Test frequency (MHz)	2nd harmonic (dBc)	3rd harmonic (dBc)	2nd harmonic (dBc)	3rd harmonic (dBc)
5	-103	< -110	-102	< -110
10	-87	< -110	-98	< -110
20	-74	-93	-92	-93

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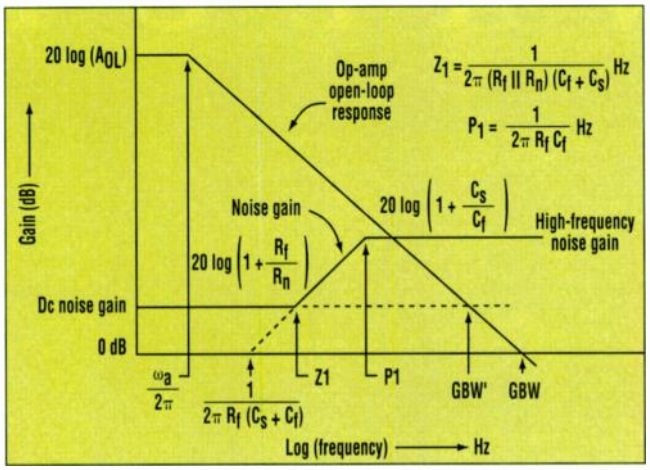
crossover. Because we're shaping the noise gain to higher values at high frequencies, we do get some peaking in the high-frequency gain for the op amp's noninverting input voltage noise.

This technique is intended to give exceptional performance for input frequencies below Z1. Because we're picking a C_s to add externally, Z1 will be set above the highest input frequency of interest if possible. Normally, a passive Nyquist filter is included after this stage prior to the converter. This also will filter out the increased output noise above the Z1 corner frequency in the noise gain *(Fig. 3, again)*.



3. This plots shows the Bode analysis of Equation 1 (loop gain).

Design Example

To achieve the best distortion performance when applying the circuit of Figure 1, an extremely-low-distortion, non-unity-gain stable op amp with relatively high slew rate was chosen. The key characteristics for Burr-Brown's OPA643 are: Gain Bandwidth Product = 900MHz (specified as a gain of +5 minimum stable gain); slew rate = 1000 V/µsec.; input noise voltage = 1.8 nV/$\sqrt{\text{Hz}}$; guaranteed output voltage swing = ±3 V; guaranteed output current = ±35mA; common mode and differential input capacitance = 1 pF each. The gain of +5 harmonic distortion at 5 MHz is specified as typically 90 dB for a 2 V p-p swing into a 100-Ω load.

The design proceeds as follows:

1. Pick R_f. Increasing values increase R_g for a given gain and reduce the output loading due to the feedback resistor. Increasing R_f to very high values will lead to an unrealizable compensation capacitor (C_f). Higher values also start to add a significant noise contribution. R_f values between 500 Ω and 1.5 kΩ are reasonable. 820 Ω was selected here.

2. Pick R_g to get the desired gain. Here, R_g = 402 Ω to get a gain of –2.04.

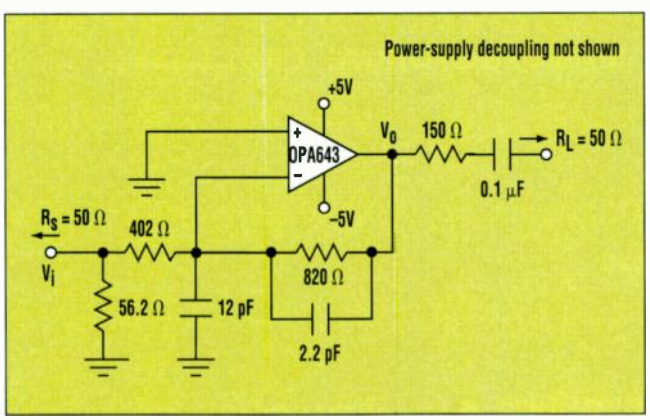
3. Set R_t to get the desired input impedance. Because R_s = 50 Ω was used for test, we'll select R_t = 56.2 Ω. These values set the R_n of Figure 2 to 429 Ω and the dc noise gain to (1 + 820/429) = 2.91. Again, R_t is optional. If the source doesn't need to be load matched, eliminating R_t will probably improve the distortion of the signal delivered into R_g

4. Pick a C_s to place Z1 in Figure 3. Z1 = 40 MHz was selected to keep high loop gain through the 20-MHz signal operation bandwidth. With Rf | | Rn = 282 Ω and 2-pF total parasitic capacitance at the input of the OPA643, the physical C_s is set at 12pF (e.g. Z1 = 1/(2π × 282 Ω × 14 pF) = 40 MHz).

5. Now use Equation 2 to set P1 and solve for the required C_f. P1 = 0.707 × (2π × 900 MHz/820 Ω × 14pF)$^{1/2}$ = 496 Mrad (= 79 MHz). This will set C_f = 1/(496 Mrad × 820 Ω) = 2.46 pF. Assuming a 0.26-pF parasitic in the R_f (chip) resistor then requires a 2.2-pF external capacitor.

The result of these five design procedures is a frequency response test circuit *(Fig. 4)*. The series output resistor was set to 150 Ω to get a total load of 200 Ω at the output. This will introduce a signal attenuation in the measurement, but emulates the input impedance of the converter. Next, we measure the broadband gain and phase for this circuit *(Fig. 5)*. A linear frequency sweep is used to allow a direct display of phase linearity. Expanding the low-frequency region (1 to 21 MHz) shows the exceptional gain flatness and phase linearity (constant group delay) that results from using this compensation technique *(Fig. 6)*. When operated at its minimum stable gain of +5, the OPA643 data sheet shows a typical peaking of 3 dB in its frequency response. Using the compensation described here, the circuit starts out at a dc noise gain of 2.91, but crosses over the open-loop gain at a noise gain = (1 + 14 pF/2.5 pF) = 6.6. This provides adequate phase margin to get the ±0.05-dB flatness *(Fig. 5, again)*.

The portion of Figure 5 that shows deviation from linear phase is obtained by subtracting a constant group delay from the measure phase response. Most of the low-frequency group delay shift was due the ac-coupling capacitor on the output. This places a pole at 42 kHz that still influences the phase at 1 MHz. The phase linearity could be further improved by increasing the value of the blocking capacitor to 1 µF.



4. In the frequency-response test circuit, the series output resistor was set to 150 Ω to get a total load of 200 Ω at the output.

Harmonic Distortion

Having achieved the extremely flat frequency response of Figure 5 using this compensation technique, you must now evaluate the distortion. First check the slew-rate margin. A 1-V p-p output at 20 MHz will require a 63 V/µsec. slew rate. The OPA643's 1000 V/µsec capability provides a 16X margin. Some CMOS converters can accept a 4-V p-p single-ended input through 20 MHz. This would push the operation up to 252 V/µsec., leaving a 4X operating margin.

In general, for distortion bet-

TABLE 2: HARMONIC DISTORTION FOR FIGURE 9

	2 V p-p output swing		4 V p-p output swing	
Test frequency (MHz)	2nd harmonic (dBc)	3rd harmonic (dBc)	2nd harmonic (dBc)	3rd harmonic (dBc)
5	-99	-105	-94	-93
10	-89	-95	-88	-84
20	-83	-81	-74	-67

ter than 60 dBc, the op amp must have a 2X slew-rate margin. And to reach better than 70 dBc, it must have a 4X margin. To reach into the 90-dBc region, a 16X margin on slew rate is by no means wasted performance margin. The 5-MHz distortion test setup includes a slight addition to the amplifier circuit *(Fig. 7)*. In this test circuit, a dc-bias voltage is added to the noninverting input.

The first prerequisite to a very low harmonic-distortion measurement is a spectrally pure input signal. Here, two cascaded eight-pole low-pass filters were used to get the input signal clean enough. Because the amplifier was achieving >100 dB SFDR at frequencies < 10 MHz, we needed the input signal spurious to be >110 dBc down. The input signal was controlled to produce a 1-V p-p swing at the op amp output pin. This was driving a 200-Ω load comprised of a series 150-Ω resistor into a 50-Ω, 6-dB attenuator. In all cases, a blocking capacitor was used at the output to allow different dc operating points at the op amp output without requiring dc load current.

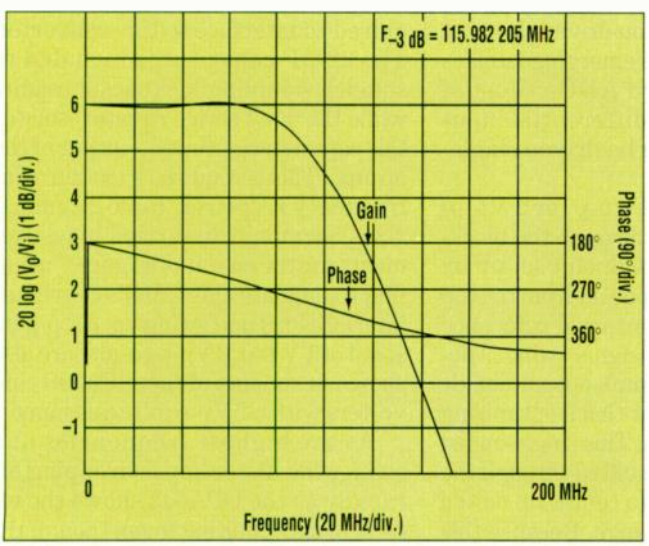
Following this attenuator, a 5-MHz notch filter was placed just before the spectrum analyzer. This notch filter is required to remove the fundamental (5 MHz) power at the input of the spectrum analyzer in order to limit the harmonic distortion created at the analyzer's mixer. The analyzer by itself does not have enough dynamic range to make this measurement.

Testing initially proceeded with the noninverting input grounded. Although excellent results were achieved, even better performance is possible by shifting the dc operating point of the signal at the op amp's output *(Table 1)*. The table summarizes the second- and third-harmonic distortion levels (in dBc below the fundamental power level) with and without the dc trim at the noninverting input.

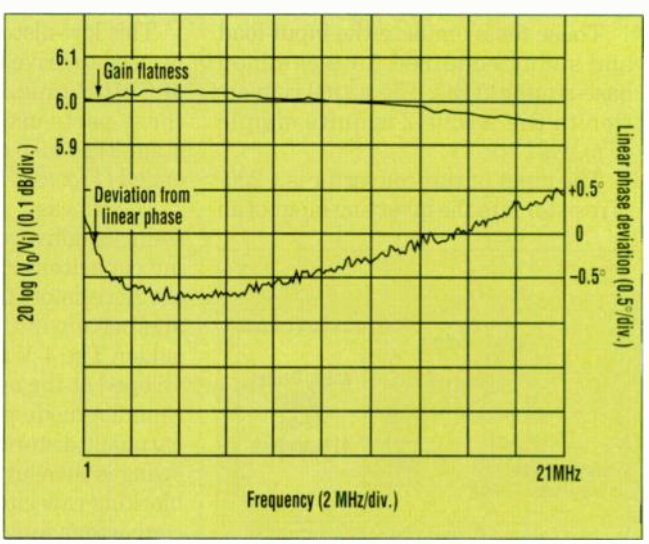
The third harmonic was still unmeasurable for ≤ 10 MHz fundamental frequencies. This also implies an exceptional two-tone, third-order intermodulation intercept for this circuit. Intermod testing showed a +46 dBm 3rd-order intercept at 20 MHz, referred to the output pin. For a 1 Vp-p full-scale 2-tone swing, this gives 2nd-order intermod spurs that are 92 dB below the test tones.

The dc operating point was set by minimizing the second harmonic at a 10-MHz input. Because the input was dc coupled, this 0.55 at the noninverting input was placing the output dc operating voltage at 0.55 × 2.91 = 1.6 V. With this offset, the output second harmonic was minimized when swinging 1.1 V to 2.1 V. One possibility is that this 18-dB improvement in the second harmonic at 20 MHz would be attributed to running the output Class A. Tests with the output-voltage swing centered, but with a bias resistor to the minus supply (Class A operation), did not, however, show any improvement in distortion.

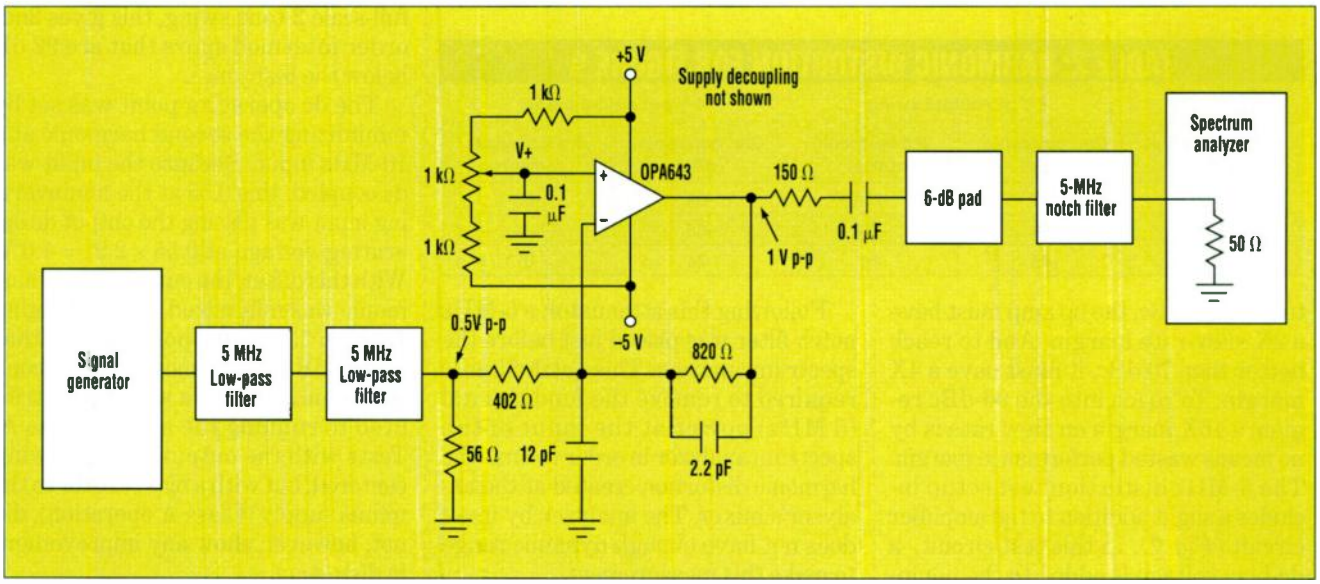
Open-loop second-order nonlinearities are principally due to signal-path imbalance over the two halves the sinusoidal swing. These arise from such issues as imbalanced ac impedance looking out the two supply pins and/or voltage-dependent capacitances in the signal path. Shifting the dc operating point seeks to balance those nonlinearities over the full voltage swing. The particular voltage required to null the second harmonic will depend on the amplifier selected and on the board layout. The OPA643 includes separate decoupling for the output stage critical to achieving the lowest distortion. The placement of those decoupling capacitors has a strong influence over the second harmonic. As a result, this nulli-



5. The broadband frequency response shows the measured broadband gain and phase for the circuit in Figure 4. A linear frequency sweep is used to directly display phase linearity.



6. Expanding the low-frequency region (1 to 21 MHz) of the plot in Figure 5 shows the exceptional gain flatness and phase linearity that results from using this compensation technique.



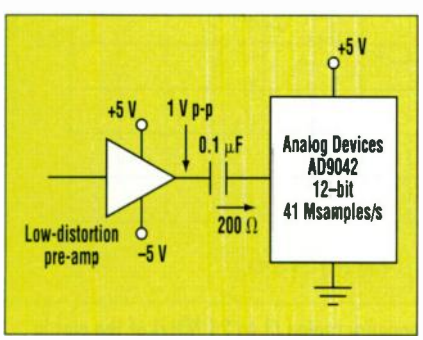
7. The 5-MHz harmonic distortion test setup adds a dc bias voltage to the noninverting input.

fying voltage is both part- and layout-specific.

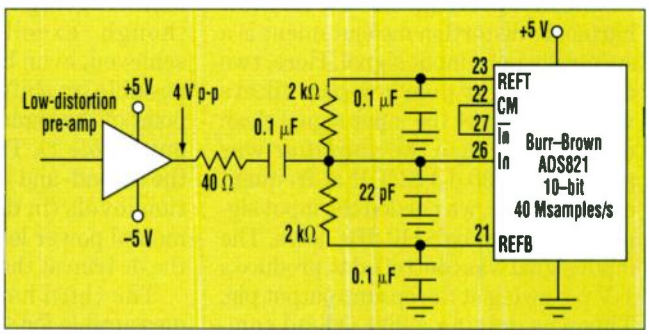
As a test of distortion repeatability with this input dc voltage,10 additional parts were placed into the circuit in Figure 7 (with no additional adjustments) and measured at 10 MHz. Less than 3-dB variability in this significantly improved distortion was observed. Testing over temperature also has shown little performance sensitivity. Once this nullifying voltage is determined for a particular part and board, it can be set with fixed resistors in production. Additional testing of the circuit at signal gains of –3 and –4 depicted a negligible increase in the harmonic distortion *(Fig. 7, again)*.

These tests emulate the input load and swing required for a common base-station ADC. The actual connection to the AD9042 is quite simple *(Fig. 8)*.

The input of this converter is a 200-Ω resistor into the inverting input of an op amp. The noninverting input sets up the required dc bias point so that no additional external components are required beyond the dc-blocking capacitor. This converter offers a 41-MSPS sample rate and 80-dB SFDR at Nyquist. The 90-dB distortion levels delivered by the circuit are required to limit degradation from this specification *(Fig. 4, again)*.



8. The connection to the AD9042 ADC is very simple.

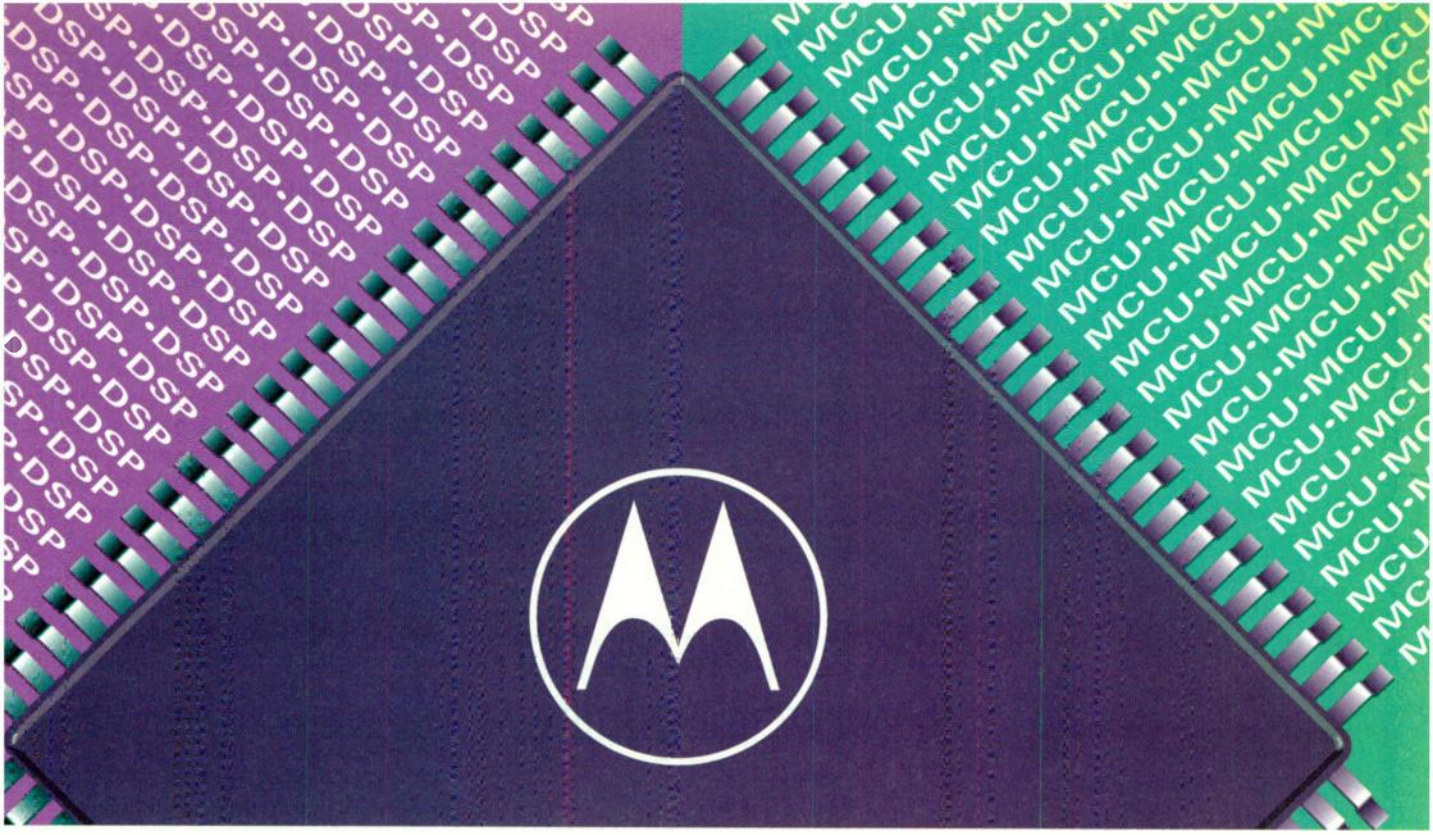


9. The interface to Burr-Brown's ADS821 ADC delivers a 4 V p-p swing through the blocking capacitor to a midpoint set up by two 2-kΩ resistors.

This low-distortion driver also may be used to drive the emerging families of CMOS pipelined ADCs. Most of these parts use a differential input stage that also can be driven single-ended *(Fig. 9)*.

In this case, a 4-V p-p (or 2 Vp-p) swing is delivered through the blocking capacitor to a midpoint set up by the 2k resistors tapped off from the top and bottom of the internal reference ladder. The 4-V p-p signal swing is developed at the op amp's output at a dc common-mode point that's optimizing harmonic distortion. This single-ended swing is then level shifted through the blocking capacitor to center up on the converter's input range. Because this is a single-ended drive into a differential converter, the internal ladder midpoint is tied to the other input. With the internal reference and buffered outputs for the top and bottom of the reference ladder, this is all that's required to interface to this converter. The 22-pF capacitor is included to squelch sampling kickback currents while the 40-Ω series resistor isolates this capacitance from the output of the op amp. This is required to retain a flat frequency response. Table 2 summarizes harmonic distortion measurements for the circuit of Figure 7 modified to emulate this CMOS converter interface load and swinging 4 V p-p instead of 1 V p-p. 2 Vp-p results are also shown in support of those CMOS converters with a 2 Vp-p full-scale input.

At the highest frequencies and swing, the distortion is dropping off rapidly as the OPA643 shows the effects of slew limiting (even though the signal is still asking for only 1/4 of the rated slew rate at 4 V p-p and 20 MHz). Because the distortion levels



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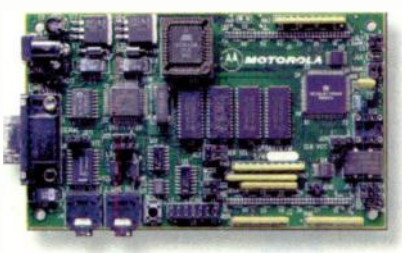

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shown in Table 2 are significantly better than present CMOS pipelined ADCs, this interface may be used without any degradation in rated performance of the ADC itself.

Conclusion

A high open-loop gain, non-unity-gain stable op amp can be successfully applied to a low-gain requirement using the novel compensation technique developed here. By intentionally introducing a zero into the noise gain of an inverting op amp configuration, a very well-controlled frequency response may be set with a feedback-compensation capacitor. Better than 0.05-dB flatness and 0.5° group delay variation was achieved from 1 to 20 MHz. Using the high loop gain and slew rate of the OPA643, and a second-harmonic nullifying technique, the resulting driver circuit can hold <–90 dBc distortion for a 1-V p-p swing into 200 Ω through 20 MHz. This same circuit can deliver a larger signal swing (4 V p-p) that can be coupled to the midpoint of a single-supply CMOS converter such as the ADS821. Harmonic distortion in that application is also considerably better than present CMOS pipelined converters.

Acknowledgements:

The author would like to thank Rosie Loaiza-Montiel for her invaluable assistance in making these demanding distortion measurements.

Michael Steffes is a strategic marketer for high-speed signal processing components at Burr-Brown. He has a BSEE from the University of Kansas, Lawrence, and an MBA from Colorado State University, Fort Collins. Michael has published over 25 articles and application notes on high-speed amplifiers.

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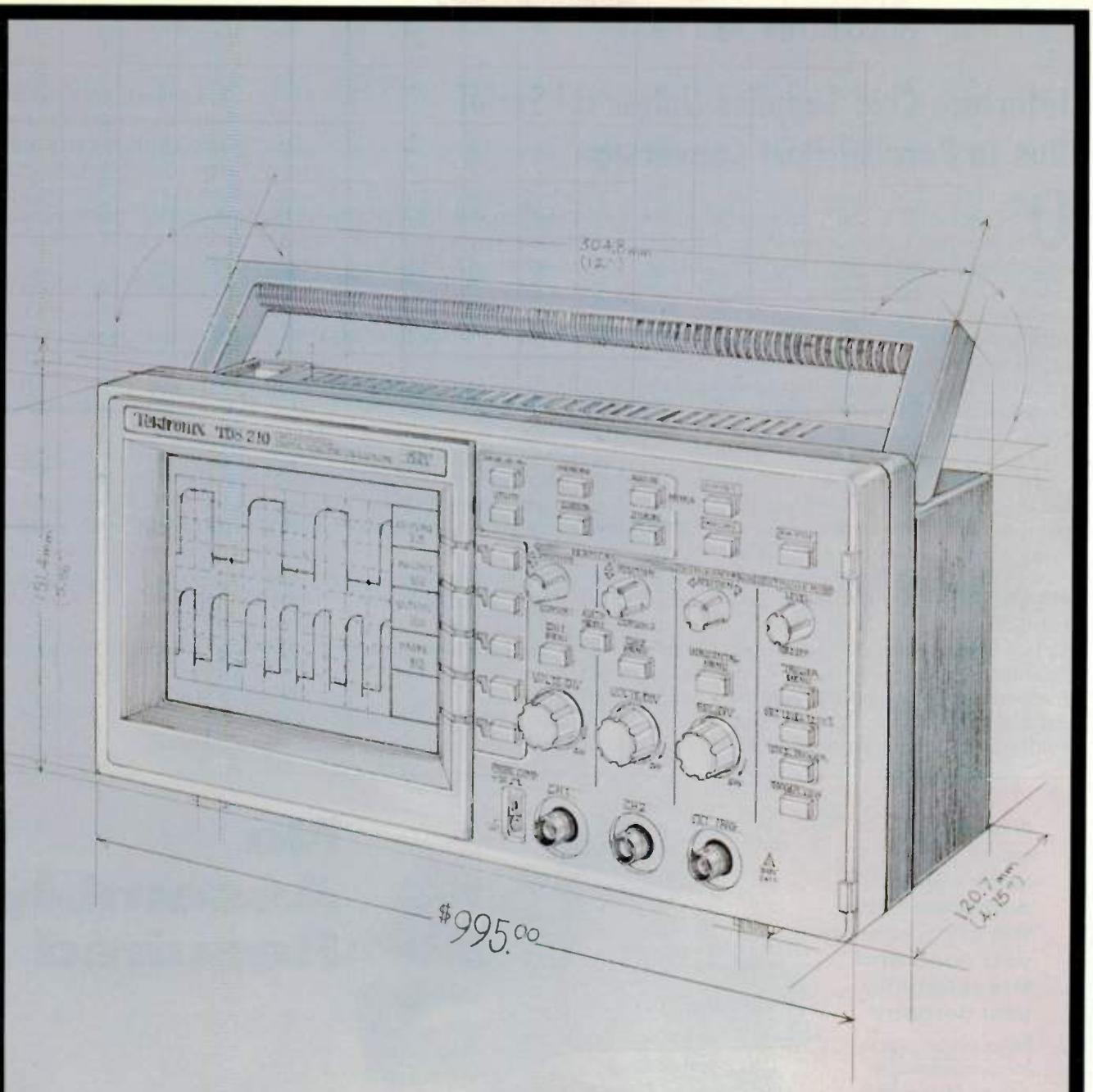
1. Steffes, Michael, "Control frequency response and noise in broadband, photodetector, transimpedance amplifiers," *EDN*, July 4, 1996, pp 113-125.

How Valuable	Circle
Highly	531
Moderately	532
Slightly	533



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PRODUCT FEATURE

Interface Chip Supplies Universal Serial Bus To Parallel-Port Conversion

One of the "hot" up-and-coming technologies is the Universal Serial Bus (USB), which offers end-users a serial connection for relatively slow peripherals, such as keyboards, mice, modems, etc. As a result, peripheral vendors are trying to reengineer their products to adapt to USB. One product that promises to simplify the task is the USS-720 Instant USB interface chip.

The USS-720 is a standard product that can be incorporated into PC peripherals containing a conventional parallel-port interface. The device provides a bridge between USB and the existing IEEE 1284 parallel port.

Two USB channels are supported to allow logically concurrent communications between the USB, the parallel port, and the chip's internal configuration. Application devices include printers, scanners, digital cameras, and backup storage systems. It can be incorporated into existing products or employed in an external adapter.

Functioning as an intelligent device controller, the USS-720 initiates and manages automatic negotiation for the fastest protocol available. Dual 192-byte on-chip USB packet buffering supplies a fast host-response time. On-board nonvolatile storage permits configuration-free power-up operation. Throughput greater than 900 kbytes/s can be achieved.

On the parallel side, the chip supports all modes, including nibble and enhanced parallel port (EPP). Hardware initiates and manages automatic negotiation for the fastest available protocol.

The chip ships with fully-compatible USB host software device drivers that enable designers to employ a modular approach to customized features. A third-party software suite from SystemSoft, Natick, Mass., enables the USS-720 to support the Instant USB features contained in the Microsoft Windows environment.

Lucent's Silicon Suite, which is also available, helps designers get their products to market more quickly. The suite includes USB device controllers and hubs that offer a direct connection to the Universal Serial Bus.

Operating at 3.3 V, the USS-720 USB-to-parallel-conversion IC is housed in a 48-pin TQFP. Samples of the chip are available now. Volume production is scheduled for the second quarter.

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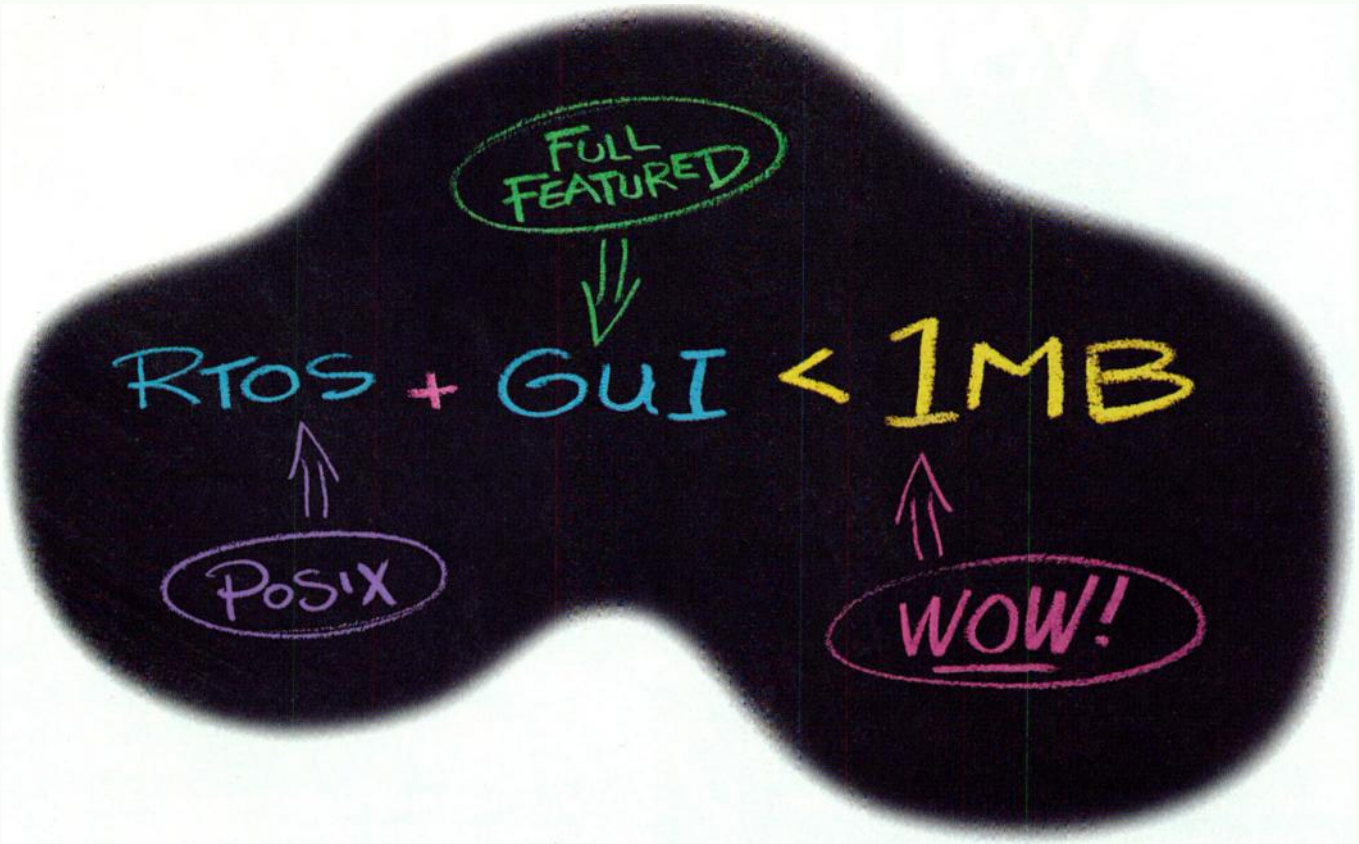

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At Last: DVD Is Available To The Consumer

After A Long Gestation Period, The First Distribution System For Digital Video Offers A Dramatic Improvement In Quality And Options That We May Never Have Thought Of.

Paul McGoldrick

SPECIAL REPORT

It's been a long time coming, but DVD (digital versatile disk) is finally with us—at least in a first-generation form. It's probably the most complicated technology ever to reach the consumer, and there is certainly a convergence track between DVD and satellite and cable technologies that use a lot of similar components. Furthermore, no one company can currently supply all the DVD technology.

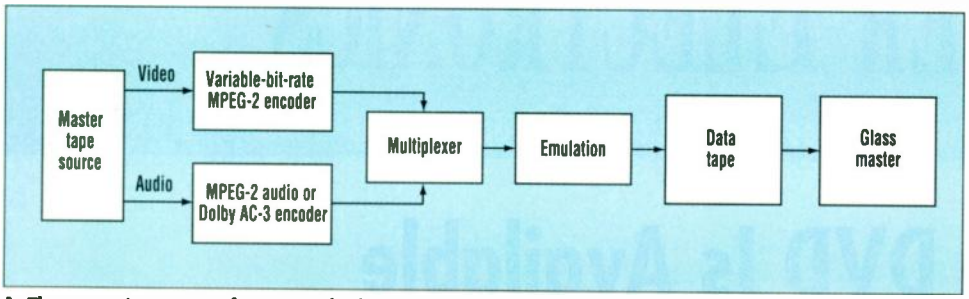
DVD should have been available to the consumer last fall. While the technology was ready, Hollywood was not. At the end of June 1996, 10 DVD-player manufacturers agreed to integrate standardized copy-protection circuits on their hardware to prevent the illegal duplication of software. Regional codes were even included so that software releases could be staggered, as the distributors in Hollywood wanted.

Art Courtesy of Zenith Corp.

The agreement was announced worldwide in a Toshiba press release, but then stalled until October. Small changes to the specifications and copy protection were added, requiring changes in the player software for all the already-manufactured players. Even with the revised specifications, the amount of software available is still quite limited. At the time this story went to press, there was some confusion about the audio specifications side of the DVD players but it was expected that this would be agreed upon by the end of January.

DVD was originally an abbreviation for digital video disk. But because of obvious applications for storing other types of signals, the term's meaning has been changed to digital versatile disk. The new technology poses a potential threat to the current proliferation of CD-ROMs, but whether the threat materializes will depend on the availability of software for the new system.

A major difference between the CD and the DVD is the wavelength of the lasers used. The CD uses an infrared laser that produces 680 Mbytes of storage *(see the table)*. The red lasers employed in the DVD, together with tolerance tightness learned from CD manufacture, offer 4.7 Gbytes of storage on the same single layer. With focusing techniques, a second layer can be pitted on the same side of the disk, allowing a total storage of 8.5 Gbytes. The fact that a single-layer capacity of 4.7 Gbytes does not double to 9.4 Gbytes for two layers is caused by a small change in the geometries of the second layer. The pitting sizes of the second layer are ac-



1. The mastering process for DVD is fairly straightforward, but it will require human intervention to view the master tape and enter standard timecode markers at required points.

tually increased so that when the sensors are refocussed at the slightly deeper point (an increase in distance for the optics), they do not see smaller objects.

Manufacturers also can apply a completely independent second side on the DVD, increasing the total capacity to 17 Gbytes. Since that represents about 9 hours of studio-quality video and audio, it's not surprising that the majority of disks issued will be single-sided, single-layered.

Mastering The DVD

The mastering and subsequent replication of a DVD for normal video and audio work is fairly straightforward. The source tape is either the original material or is a master made from a motion picture or a computer animation source *(Fig. 1)*. The mastering process must involve human intervention to view the tape and enter markers, using standard timecode, at intervention points. These points could include panning for wide-format inputs, color correction where required, parental control cues, closed-caption information, or even entry points for commercials. The typical mastering setup will use workstation facilities.

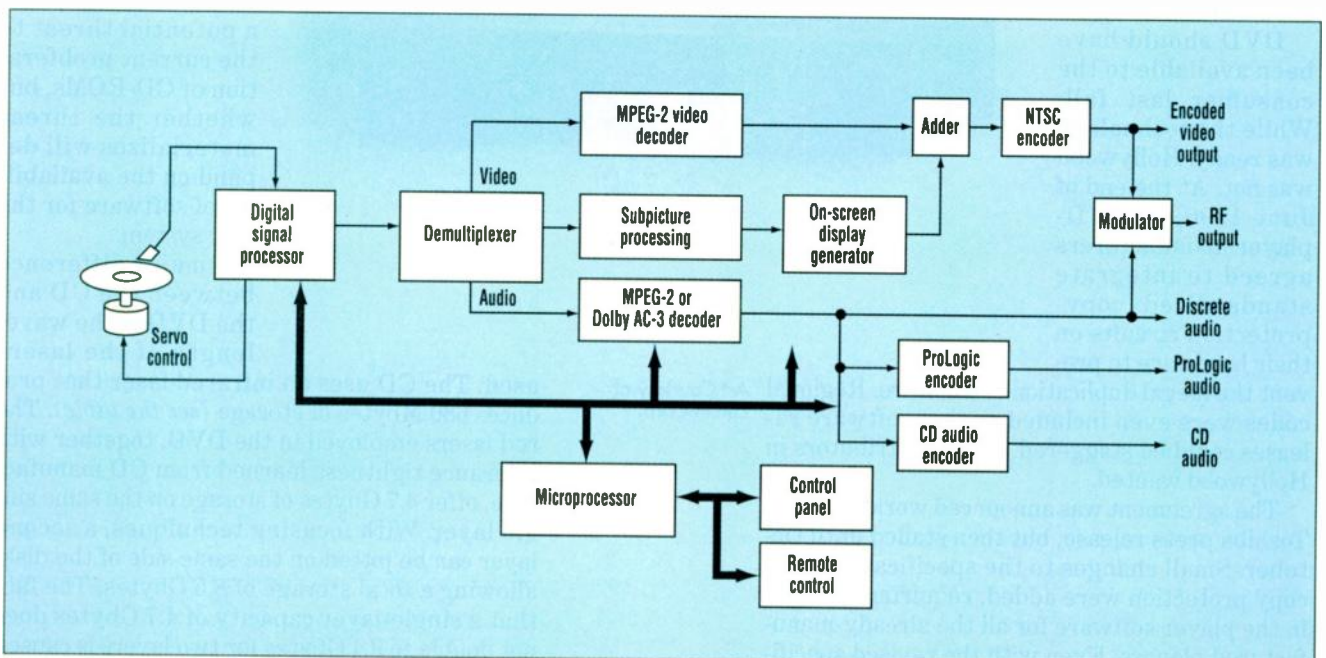
During mastering the video is bit-rate reduced (compressed) through an MPEG-2 encoder using MP@ML and the audio is compressed through a Dolby AC-3 encoder or an MPEG-2 audio encoder. Any additional data streams being used also will be coded through the audio side. The two encoded signals are multiplexed into a single data stream and then passed through an emulation stage, which simulates the playback peculiarities of the system. Any additional subpicture material would be multiplexed at the same point.

The required etch of the disk is then recorded on a data tape, which is used to produce a glass master. Consumer disks are replicated from this glass master. The cost of replicating a single-sided, single-layer DVD is currently being estimated at about 62 cents which is, quite comparable to an audio CD. The capital cost of mastering, however, is quite high; apart from the computer workstation, the MPEG-2 encoder does not come cheap.

Mastering material that is not a straight "dub" from a single source could be an extremely complicated process. Interactive material, for example, with multiple possible paths or stories are software challenges in and by themselves. Systems for such material are being developed by a number of companies, and they could be so specialized that a complete system may have to be developed for just one task.

The DVD Player

Standalone DVD players are available now. As was the case earlier with CD-ROMs, built-in DVD players will appear in PCs. The basic architecture of both is the same, with



2. The architecture of the DVD player is similar to that of the CD-ROM player, but with some different control features. A digital signal processor handles inputs from the disk reader and feedback signals to complete the speed-control loop

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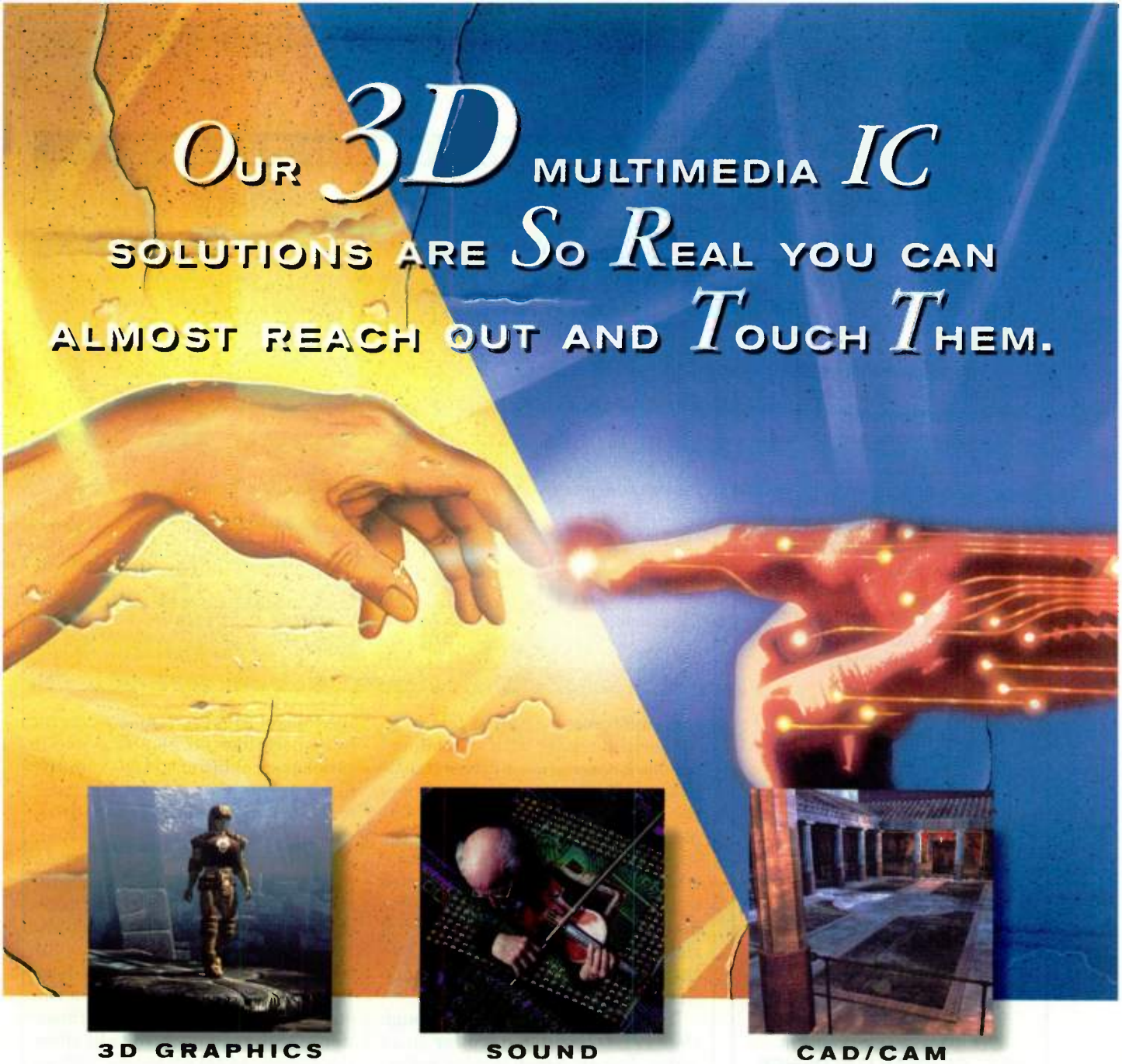

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READER SERVICE 184

COMPARISON OF CD AND CVD SPECIFICATIONS

Specification	CD	CVD
	General	
Disk diameter	120 mm	120 mm
Disk thickness	1.2 mm	1.2 mm
Disk structure	Single substrate	Two bonded 0.6-mm substrates
Laser wavelength	780 nm (infrared)	650 and 635 nm (red)
Numerical aperture	0.45	0.60
Track pitch	1.6 μm	0.74 μm
Shortest pit	0.83 μm	0.4 μm
Reference speed	1.2 m/s	4.0 m/s
Data layers	1	1 or 2
Data capacity	680 Mbytes	1 layer: 4.7 Gbytes 2 layers: 8.5 Gbytes
Reference user data rate	Mode 1: 153.6 kbytes/s Mode 2: 176.4 kbytes/s	1108 kbytes/s, nominal
	Video	
Video data rate	1.44 Mbits/s (video, audio)	1 to 10 Mbits/s, variable (video, audio, subtitles)
Video compression	MPEG-1	MPEG-2
Audio tracks	2-channel MPEG (mandatory U.S.); 2-channel linear PCM	2-channel MPEG; 5.1-channel Dolby AC-3; optional: up to 8 streams of independent data
Subtitles	Open caption only	Up to 32 languages

some differences in control features.

The disk reader with spinner and playback-sensing laser drives signals into a digital signal processor, where the speed-control loop is also completed with signals sent back to the spinner servo *(Fig. 2)*. The position of the reading point also is controlled by an onboard microprocessor. The data stream input from the digital signal procesor is demultiplexed into three parts: the video, audio, and subpicture sections.

The video stream passes through the MPEG-2 video decoder to an adder. Any on-screen display material is added at this point after being generated from the subpicture processing output. The video signal can be taken as an RGB(Red, Green, Blue) output or through an NTSC encoder as Y/C (luminance/chrominance) or fully composite. Some players also will have an RF modulator.

The audio stream passes through either an MPEG-2 or Dolby AC-3 decoder. The discrete audio signal can be taken as the output, and older standards are grandfathered with Dolby ProLogic, CD audio and Video CD 2.0. Additional data streams that have been encoded also will pass through the audio decoder.

The microprocessor's function is to translate all the instructions from the control panel and remote control into operations for playback, and it sets basic conditions read from the disc in terms of its content and track format. Parental lock-out features can also be preset into the player, which in some cases will allow the player to completely skip some material deemed inappropriate for underage viewers. To incorporate this feature, the player needs a buffer for both the video and audio signals so that the reader can jump from the out-transition to the new in-transition. This type of control will allow the system to take a movie with an R-rating and play it back as a PG-13. Street prices of a player are expected to be around $350 by the end of 1997 and down to $230 by 1999.

The PC version of the DVD player will, of course, allow the user to have front-panel access for the disk, and the DVD decoder will be located on a peripheral card. The control will be from the host CPU, while the video output from the decoder card will feed a graphics accelerator to drive the display.

How Valuable	Circle
Highly	558
Moderately	559
Slightly	560

PRODUCT FEATURE

Range Of High-Performance ADCs And DACs Target Consumers And Professionals

Four more products in the delta-sigma ADC/DAC arena are on the way from AKM Semiconductor. The AK4520A is a stereo CMOS ADC and DAC for middle-range DAT, surround-sound systems, and musical instruments. It uses 20 bits and with dynamic range and SNR at 100 dB with a supply rail of 5 V. All of the signal inputs and outputs are single-ended and the DAC outputs pass through analog lowpass filters to remove out-of-band noise. The ADC is 64x oversampled, and the DAC is 128x. The master clock frequency can be either 256 or 384 times the sampling frequency in use, which in itself can range from 16 to 50 kHz. The DAC has selectable digital deemphasis for 32-, 44.1- and 48-kHz sampling. The AK5351 is a 20-bit , 64x oversampled ADC using AKM's enhanced dual-bit architecture. The 5-V part was designed for digital surround and stereo audio applications such as car audio. The analog inputs are fully differential but can be configured single-ended. Both dynamic range and SNR are 100 dB. An on-chip linear-phase digital filter has a 22-kHz passband with a ripple of ±0.005 dB and a stop-band attenuation of 80 dB. The sampling frequency can be in the band of 16 to 54 kHz with the same master clock arrangement as the AK4520.

The AK5352 also is a 20-bit 64x oversampled ADC using the new enhanced dual bit architecture, but with a 96-kHz sampling rate giving dynamic range and SNR numbers of 103 dB. The 5-V part draws 145 mW. The part is designed for high-end digital, stereo, and audio systems.

The AK4324, another 96-kHz sampled part, is a 24-bit DAC designed for the 96-kHz sampling mode of DAT and DVD. Switched-capacitor filters are used in the analog outputs with a high immunity to clock jitter. Dynamic range is 106 dB and a low-distortion differential output is offered together with a switchable digital deemphasis, zero detect, and soft mute. Power dissipation is 200 mW with a 5-V supply.

The AK4520A is available now in a 28-pin VSOP package priced at $7.59 for 10,000-piece lots; and the currently available AK5351 packaged in a 24-pin VSOP is priced at $4.92 in 50,000-unit lots. The AK5352 also comes in a 24-pin VSOP and costs $17.39 for 1000 pieces, and is available now. Production quantities of the AK4324, also in a 24-pin VSOP, will be available in March 1997 (sampling now) at $13.50 in 1000-piece lots.

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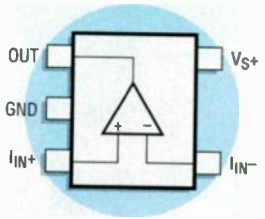

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PRODUCT FEATURE

Videophone Reference Design Has A Target Of Low-Cost POTS Usage

At last November's Comdex, Motion Media Technology Ltd. announced a reference design for small, standalone videophones for use on ISDN circuits. Next month, they will announce a similar design for POTS (plain old telephone service) use. With both, Motion Media will license the Xyclops reference design to manufacturers for the consumer market

Both designs use Lucent Technologies' AVP-III video/audio processor chip. Between the two designs, videophones will comply with the H.324 (POTS), H.320 (ISDN) and H.323 (LAN) international standards. Delay time using these processors is about 0.5 seconds, allowing for close-to-real-time videoconferencing.

The AVP-III also offers support for the G.723 audio compression/decompression standard and for MPEG-1 playback, maiking it a full-function platform for multimedia PCs and other consumer systems. Moreover, offers real-time two-way video conferencing over both analog and digital lines. Lucent supplies the communications software protocol to ensure interoperability with solutions from other vendors.

The basic arrangement of the POTS videophone design is centered around the Lucent AV4400. The AV4400 acts as the compression/decompression engine for the audio and video as well as supports the communications software protocol.

In the design, the telephone line couples into a modem subsystem that feeds the bus, which itself is under the control of the microcontroller with its associated function keypad. The main memory (ROM and RAM) couples directly to the bus while separate DRAM is controlled by the AV4400 for processing purposes. The video from the local composite camera is fed to the self-contained NTSC/PAL video decoder to drive the codec, while the output from the codec feeds an NTSC/PAL encoder to drive the local composite monitorwithe the images from the remote point .

Motion Media feels that the AVP-III chip design will bring strong quality improvements to the initial features of the videophone design. The bill of materials for the reference design (without the camera and monitor) goes for around $200.

Motion Media Technology Ltd.
Horton Hall
Bristol BS17 6QN
United Kingdom
+44 (0) (1454) 313444
Lucent Technologies, Microelectronics Group
555 Union Blvd.
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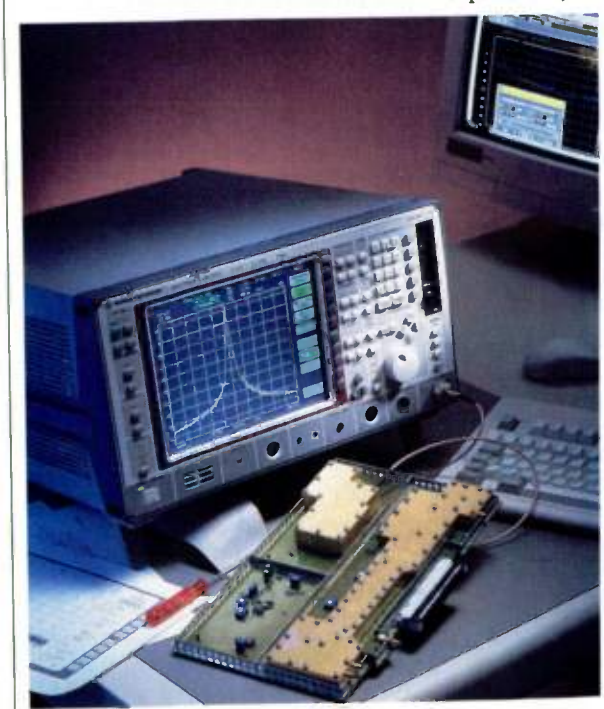
New Functions Enhance Spectrum Analyzer Flexibility

Complex modulation schemes in new communications systems are putting new requirements on an old standby.

John Novellino

Driven by the boom in wireless communication systems, spectrum analyzers are getting infusions of new functionality to keep up with new measurement demands. But the need for traditional spectrum analysis is also strong, at least in part because many designers are doing precompliance testing in order to ensure that their new products will meet electromagnetic compatibility (EMC) standards made mandatory by the European Union last year.

The increasing complexity of communications systems often requires more automated measurements, while the proliferation of standards demands flexible instruments if designers are to play in more than one market segment and do it economically. Rather than simplifying the problem, the use of digital modulation techniques is making the job more difficult.



While there's still a need for traditional spectrum analyzers, "We need to move more toward multifunctional pieces of test equipment, like merging spectrum analyzer measurement capability with other types of test equipment," according to Carla Slater, a product marketing engineer at Anritsu Wiltron Co., Richardson, Tex. She sees instrument OEMs coming at the problem from two different sides. For instance, Anritsu added spectrum analysis to a high-performance digital mobile radio test system. The company doesn't consider it a spectrum analyzer because the main focus of the unit is digital signal processing and digital demodulation for specific wireless communication formats.

But such narrowly-focused, high-end products are only a starting point, says Slater. There's also a need to take more economical conventional analyzers and add features that focus them towards more specific applications. "I think we'll be going towards doing more of that even within the realm of traditional spectrum analyzers, taking a spectrum analyzer and making it more multifunctional," she says. Adding digital demodulation to a conventional analyzer is one enhancement.

Other users might be looking for more accurate frequency measurements, says Slater. "So you provide a built-in counter with the spectrum analyzer," she says. "You might add a built-in power meter as well, to make more accurate power measurements."

Or, the user may want to work in a specific communication system format. The instrument vendor can then supply software that automatically sets up the analyzer and makes the measurements needed for the desired format. "That's providing not only greater functionality, it's making the user more efficient, and it's offering greater ease of use," says Slater.

One area in which software is available is EMC testing. Anritsu's PC-based software controls the spectrum analyzer and makes EMC measurements according to specified standards. Slater says the company is seeing a lot of interest from speciality firms that do contract EMC

testing for equipment manufacturers. A number of larger manufacturers also have set up their own EMC labs, she says.

In fact, EMC testing is becoming a major growth area for spectrum analysis, according to Bob Rennard, product marketing manager for spectrum analyzers and signal analyzers at Hewlett-Packard Co., Santa Rosa, Calif. Many manufacturers are doing their own precompliance testing, he says. "That's the engineer being able to do on a benchtop, or in a casual environment, testing to essentially sort out the dogs and cats before they go into a typetesting environment, which is much more rigorous and much more expensive," says Rennard.

He also sees some fundamental changes occurring in the use model for spectrum analysis. The traditional uses, looking at a broad frequency range for spurious signals and harmonics, continue. "But more recently, where a lot of the movement is going, is toward looking at a known signal in a communication system," says Rennard. "Literally, the analyzer is becoming a frequency-selective power meter. Actually, you can extrapolate that to a frequency-selective and time-selective, or code-selective power meter for a burst digital signal."

Providers of communication services—cellular and PCS companies, for instance—are licensed to a specific band and power level. So, designers of equipment for these services must optimize how they use that power within that band, to maximize the number of customers that they can accommodate, and to lengthen battery life on the user end.

"What you see is an extraordinary amount of work being done to send the maximum power level out for the licensed band without wasting power, because that may degrade battery life," says Rennard.

He explained that if the ramp up and ramp down during transmissions are too fast, spectral splatter can occur. And, distortions in the amplifiers can cause harmonics and distortion products in the transmitted spectrum that have to be filtered out later. "A whole bunch of work is being done on how to get to that maximum power level without unnecessarily throwing away excess power," says Rennard. "It's a matter of optimizing the circuit so that you're making efficient use of the battery power that's on your handheld. That's probably the dominant use in the communications world."

Rennard also sees a push in the industry toward what he calls a lower cost or personal spectrum analyzer. The idea is to enhance engineers' productivity by creating more personal toolsets.

"You've got a kind of bifurcated market," he says. "At the high end, you're looking for increased capabilities, going towards something like a vector analyzer. Then you've got the PC analogy, where you're trying to get more tools into more engineers' hands so there's less sharing. We see a lot of that. Precompliance testing is a good example of that."

"The hot applications that we are seeing are really coming out of the explosion of PCS and of cellular."

These basic instruments are "garden-variety, swept-tuned analyzers used like a frequency-domain scope," he says. But give them a software overlay, or "personality," and they can behave like an EMC tester or CDMA tester, and do some of the compliance testing required by different standards.

The boom in the communications industry is what's having the greatest effect on spectrum analyzers right now. "The hot applications that we're seeing are really coming out of the explosion of PCS and of cellular," according to Bob Buxton, product marketing manager for spectrum analyzers and digital mobile radio test sets at Tektronix Inc., Beaverton, Ore. "That whole tornado, of activity is driving a lot of demand for functionality in spectrum analyzers."

One important use of spectrum analyzers in communication systems is for adjacent-channel power measurements. There's no way to use a power meter to make the measurement, says Buxton, because it's just not selective enough to look at only a specific channel width at a 30-kHz offset from the carrier. But conventional analyzers were not accurate enough for today's measurements, and they were designed to measure an unmodulated CW signal.

"So that has driven spectrum analyzer manufacturers to include detection schemes that are essentially rms schemes rather than traditional peak detection. This was to make sure that the power is measured correctly even though it may be a signal modulated with pseudorandom sequences," says Buxton. He cites the FSE series from Rohde & Schwarz as an example.

Adjacent-channel measurements also bring up the issue of sufficient dynamic range. "It's now not just the noise floor that's important, it's also the phase noise of the local oscillator in the spectrum analyzer," says Buxton. "If you're trying to measure something at a 30-kHz offset from the carrier, in reality you're measuring not only the effect of the transmitter under test, but also the phase noise of the spectrum analyzer. So that has implications for the quality of the spectrum analyzer specifications."

The proliferation of standards has opened up a whole new area for spectrum analyzers. A manufacturer of communications components or equipment wants to sell those products into as many systems as possible, so they must be tested to multiple standards

"That's driving a demand for spectrum analyzers that not only can provide the traditional spectrum analysis functions of the frequency domain, but also modulation analysis," says Buxton. "And it must do so in a flexible way so that the instrument doesn't just make measurements on a CDMA, GSM, or IS-136 signal. It needs to be able to handle all of those standards and more."

How Valuable	Circle
Highly	552
Moderately	553
Slightly	554

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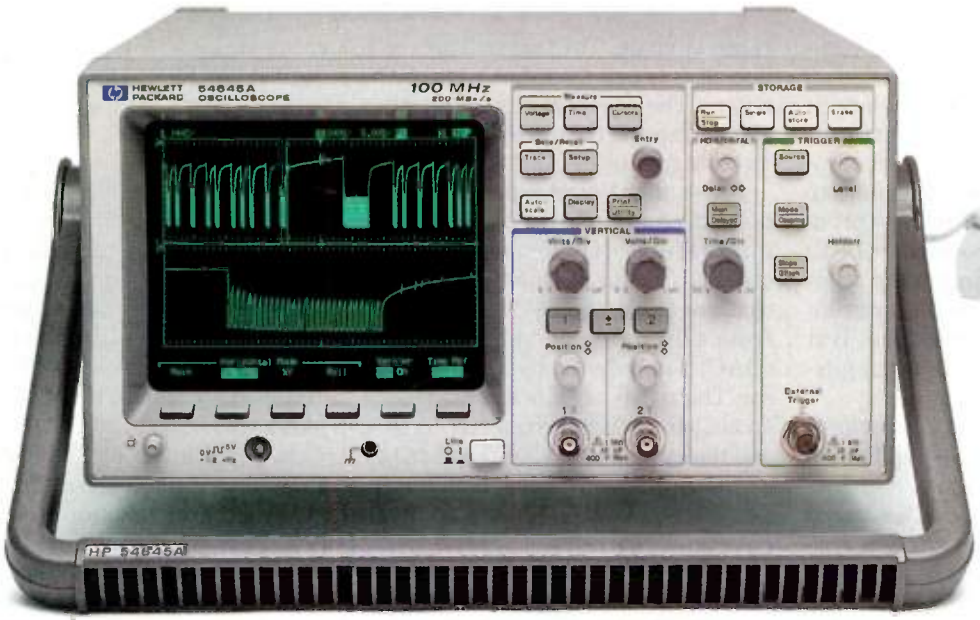

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READER SERVICE 27

Vector Signal Analysis Aids Test Of DSP-Based Wireless Designs

Digital Signal Processing Architectures Enhance Wireless Systems, But They Also Bring With Them Some Specialized Measurement Problems.

MATT BELLIS, Hewlett-Packard Co., Microwave Instrument Div., 1400 Fountain Grove Pkwy., Santa Rosa, CA 95403; (707) 577-3855.

The growth in the wireless communications market has fueled an unprecedented level of competition in this industry. Added features, reduced cost, and shorter development cycles have forced designers to seek better ways to create new products. Digital signal processing (DSP) is one solution, offering many engineers the ability to build better products faster than ever before. But DSP brings with it some testing issues that must be considered.

DSP has a number of advantages over analog signal processing. Design reuse is one. Generic receiver and transmitter designs may be leveraged across different products. This is possible even with products designed for different communication formats (e.g,. FLEX and POCSAG pagers). In addition, DSP techniques are readily simulated in software, allowing many of a design's performance characteristics to be determined before any prototypes are built.

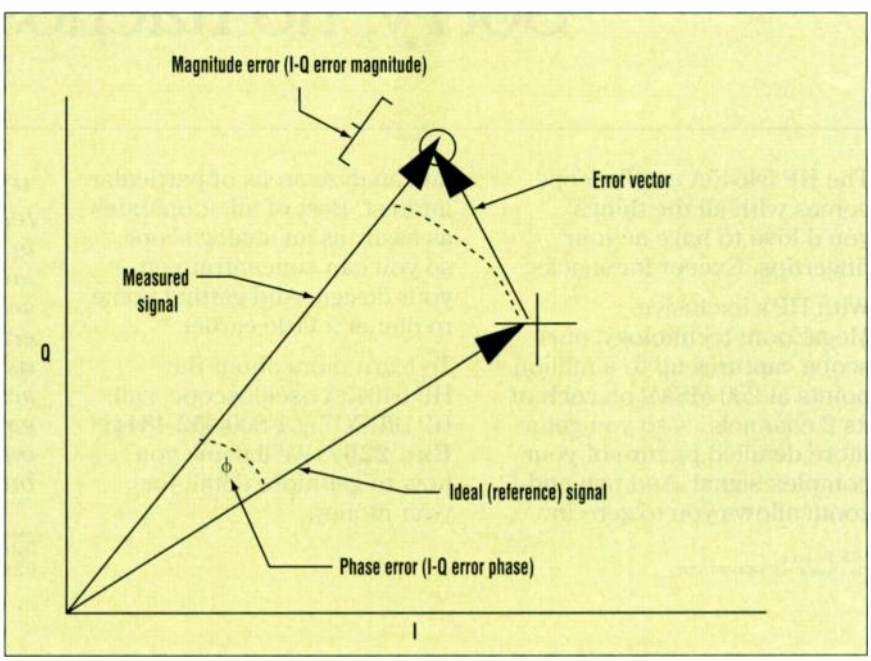
Manufacturing variability is reduced in DSP design. The components used for analog signal processing—for example, mixers and filters—have performance characteristics that vary from component to component. This variation increases the amount of tuning and testing required during the manufacturing process. Once a signal has been digitized, however, all subsequent blocks in the design are virtually immune to parametric variations. Thus, functional testing is the primary testing done in manufacturing.

A typical cellular phone architecture is a good example of how digital techniques are being used in formerly all-analog designs. The analog signal processing is restricted to the RF front end, which has a transmitter and receiver chain. The transmitter chain upconverts and amplifies a baseband signal. The receiver chain amplifies and downconverts the RF to an intermediate frequency (IF).

Most of the signal processing is done digitally. The in-phase (I) and quadrature (Q) baseband data streams (vector modulation products that are explained below) are output from a digital-to-analog converter (DAC) that is driven by a DSP processor. The receiver IF is sampled using an analog-to-digital converter (ADC), and the sampled data is interpreted by a DSP processor. The overall operation of the phone is controlled by an embedded processor.

Although DSP decreases the test requirements during production, the test complexity during design is increased. The boundary between the digital world and the analog world (generally where the DACs and the ADCs are) requires sophisticated analysis that was not required by all-analog designs. In addition, digitally modulated signals have a new set of parameters that identify the quality of the signal. Traditional signal analysis can uncover many design problems. However, vector signal analysis enables the designer to explore the properties of signals in ways that in the past have not been possible.

In a typical swept-tuned spectrum analyzer, the input signal first travels through the attenuator and input filter. The attenuator limits the amplitude of the signal, while the low-pass filter eliminates undesirable frequencies. After the filter, the input signal



1. By comparing the measured phasor against an ideal reference phasor, designers can determine the error vector being created by their system.

PRODUCT FEATURE

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Motion Media Technology Ltd.
Horton Hall
Bristol BS17 6QN
United Kingdom
+44 (0) (1454) 313444
Lucent Technologies, Microelectronics Group
555 Union Blvd.
Allentown, PA 18103-1229
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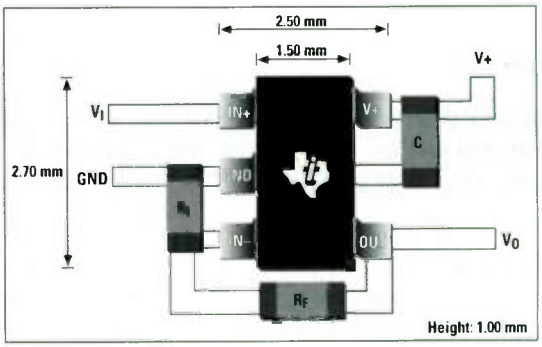

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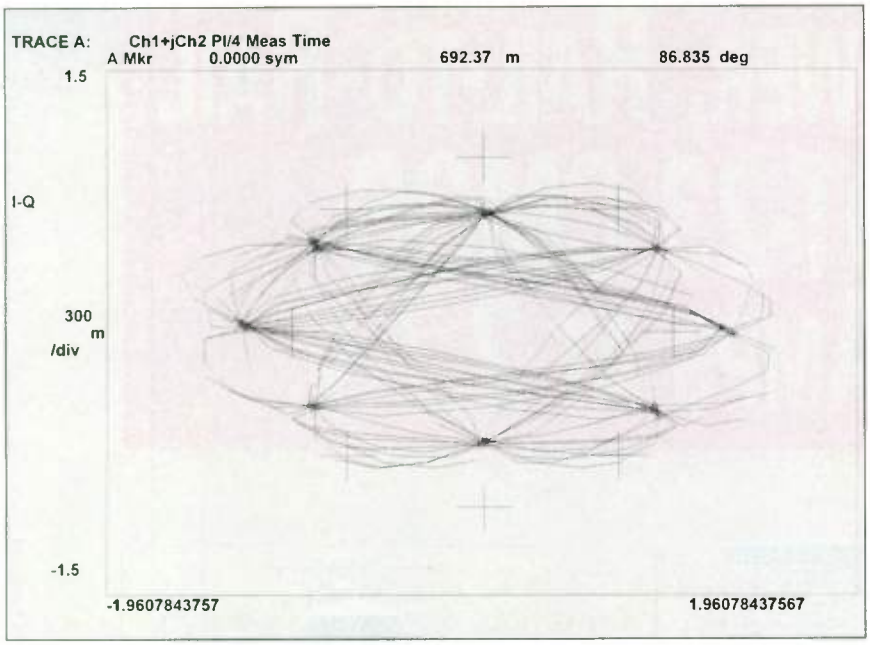


2. An ideal I-Q vector diagram should be symmetrical about the I and Q axes. This elliptical diagram indicates that the signal amplitude never reaches its ideal levels, so additional amplification is needed, and the gain through the DAC should be adjusted.

gets mixed with a signal generated by a voltage-controlled oscillator (VCO). The VCO's frequency is controlled by a repeating ramp generator, whose voltage also drives the display's horizontal axis.

As the frequency of the VCO changes, the mixed input signal sweeps through the resolution bandwidth filter (the IF filter), which is fixed in frequency. A detector then measures the power level of the signal passing through the IF filter, producing a dc voltage that drives the vertical portion of the display. As the VCO sweeps through its frequency range, a trace is drawn across the screen. This trace shows the spectral content of the input signal within a selected range of frequencies.

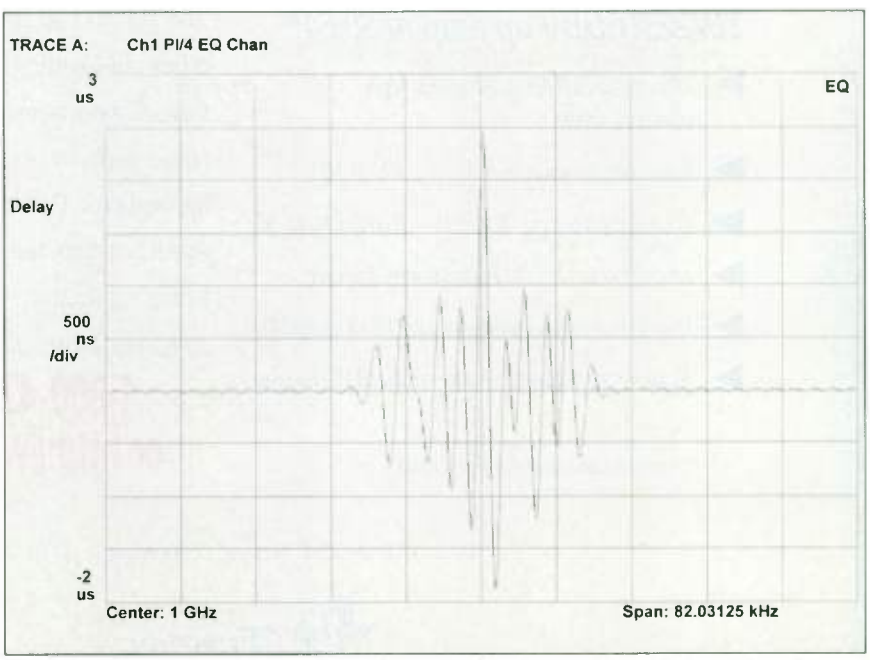
The architecture of a vector signal analyzer, however, resembles that of a wireless phone. The signal from the input port goes through an input antialiasing filter to eliminate signals that cannot be properly sampled by the ADC. After the signal is sampled, the digitized data is processed by the digital filter assembly. This is the main circuitry that produces band-limited, band-translated data to be processed by various DSP algorithms later. A memory block holds all data from different results and uses it on different occasions. The main engine is a DSP processor that processes the data to recover information about the signal.

Vector signal analysis has many applications in transmitter testing. Traditional parameters such as adjacent channel power, occupied bandwidth, and spurious emissions (spurs) may be measured. In addition, the transmitter turn-on and turn-off times are easily measured using vector analysis. The I-Q signal space may be measured to determine phase error, magnitude error, error-vector magnitude (EVM), and other parameters.

For modulated signals—in other words, signals that carry information—measuring the modulation quality of the signal is important. For digitally modulated signals, EVM is a quantitative measure of transmitter quality.

A review of the basics of vector modulation will help in understanding EVM. In vector modulation, digital bits are transferred onto an RF carrier by varying the carrier's magnitude and phase such that, at each data clock transition, the carrier occupies any one of several unique locations on the I versus Q plane. Each location encodes a specific data symbol, which consists of one or more data bits. A constellation diagram shows the valid locations (that is, the magnitude and phase relative to the carrier) for all permitted symbols, of which there must be 2n, where n is the number of bits transmitted per symbol. Thus, to demodulate the incoming data, the receiver must thus accurately determine the exact magnitude and phase of the received signal for each clock transition.

To determine the quality of the



3. This frequency-response measurement shows significant group delay, which may have been caused by nonlinearities in the reconstruction filters. Improper implementation of the digital filters can also affect the circuit's frequency response.

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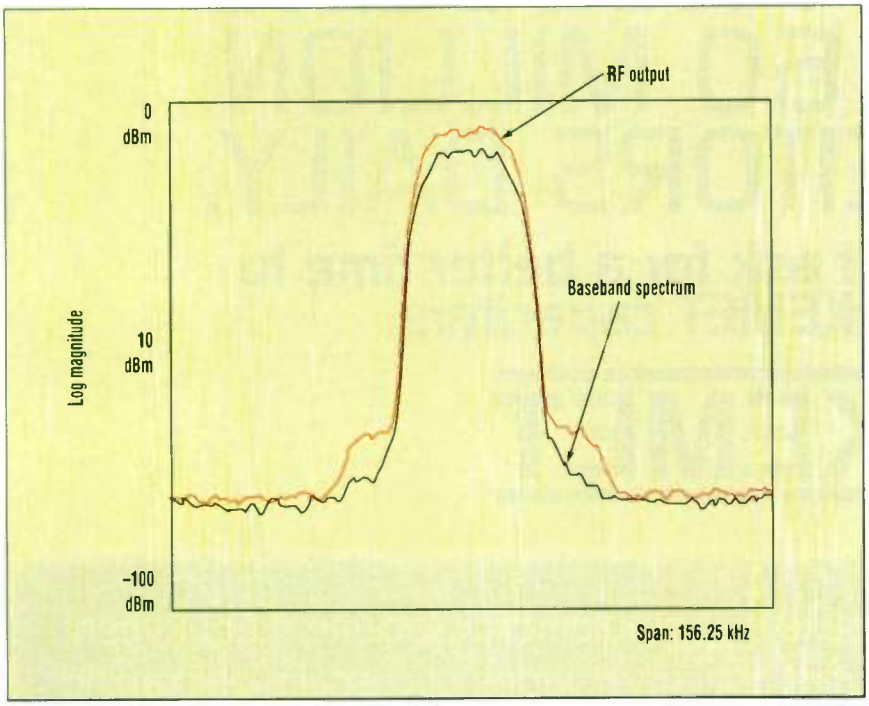


4. A comparison of the baseband spectrum and the RF spectrum can show if the transmitter's RF section is creating adjacent-channel interference, as is the case shown in this example.

transmitted signal, the engineer must measure the signal's magnitude and phase at a specific moment in time. These values, which define the actual or "measured" phasor, can be compared to a corresponding ideal or "reference" phasor calculated from knowledge of the transmitted data stream, the symbol clock timing, baseband filtering parameters, and other factors. The differences between the the measured and reference phasors provides both the signal EVM and the phase error. By convention, EVM is reported as a percentage of the peak signal level, usually defined by the constellation's corner states *(Fig. 1)*.

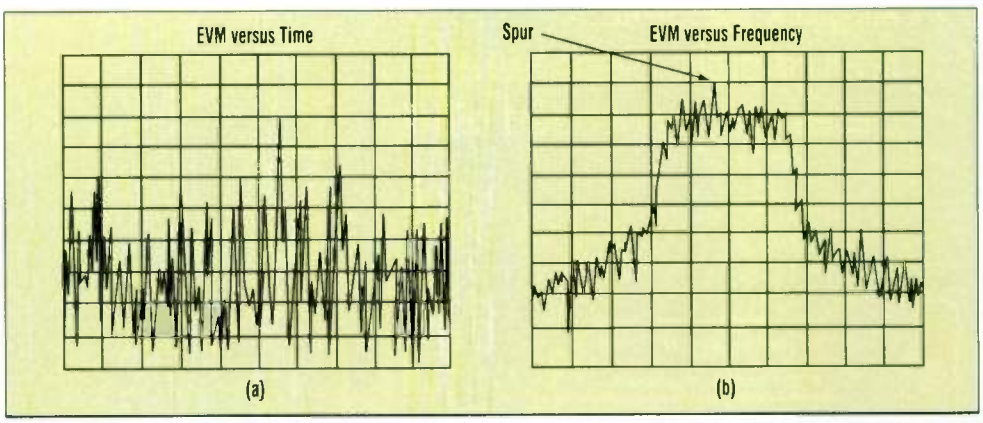
In addition to measuring the RF signal, designers can use vector signal analysis to measure the quality of the baseband I and Q signals. These signals are created by the transmitter's DSP section and are sent to digital-to-analog converters. The outputs from the converters pass through analog reconstruction filters before reaching the I-Q modulator. Using vector signal analysis, the designer can re-create the baseband spectrum from the I and Q channels. Errors in this reconstructed spectrum (as compared to the spectrum that would be created by an ideal I-Q modulator and RF upconversion chain) uniquely identify any problems associated with the analog reconstruction filters, the outputs of the DACs, or even the DSP algorithms that were used to create the signals.

For example, the analog reconstruction filters remove high-frequency components caused by the discrete nature of DACs. The analog output of a DAC is a series of discrete voltage levels that are a function of the DAC's bit resolution. Because of the sharp rises and falls between these levels, the DAC's output contain high-frequency components. If the system's reconstruction filters are inadequate, the reconstructed spectrum will reveal high-frequency spurs.

Other problems in the RF path can be diagnosed by looking at the demodulated I-Q signals. At the DAC inputs the I and Q streams go their separate ways. Ideally, the paths to the I-Q modulator should be identical. Frequently, however, the gain and group delay through each path is different. These differences can be measured and evaluated by looking at the demodulated spectrum.

The I-Q vector diagram indicates the measured signal trajectory in the I-Q plane. By comparing the measured trajectory with an ideal trajectory, the designer can calculate the signal's phase error, magnitude error, and EVM. Deviations from ideal indicate specific problems. For instance, the ideal trajectory is symmetrical about the I and Q axes. If the vector diagram appears to be elliptical along the Q axis, that means the signal amplitude never reaches the ideal levels *(Fig. 2)*. Therefore, the Q channel requires additional amplification, so the gain through the DAC in the Q channel must be adjusted.

Vector signal analysis also may be used to measure the baseband frequency response. Using the same setup as previously described, the frequency response is determined by equalizing the signal. The vector signal analyzer applies a filter to the signal to remove or compensate for the effects of linear distortion. The filter can be defined in the frequency domain by frequency response parame-



5. Error-vector measurements made as a function of time (a) can be transformed into the frequency domain by an FFT algorithm (b). In this form, they can be used to locate spurious signals.

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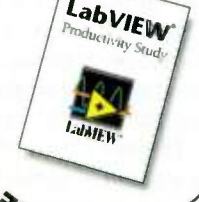

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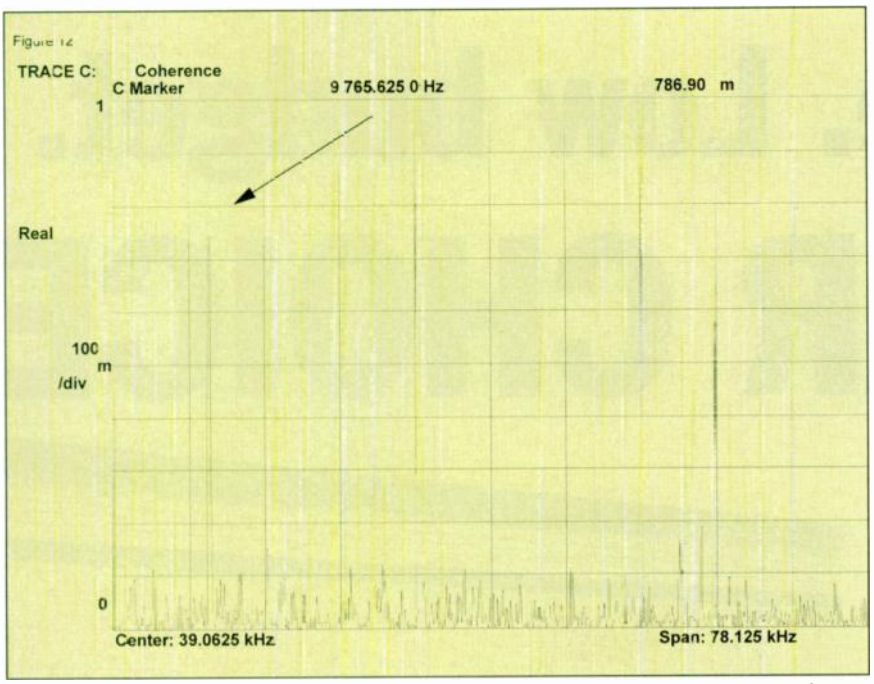

6. A high level of coherence (near one) between a baseband signal source and the RF signal indicates that the baseband source has been unintentionally modulated onto the output signal. This example shows such a source at about 9.8 kHz.

ters like gain and phase or group delay. Alternatively, the filter can be defined in the time domain by its impulse response.

If the frequency response measured at the outputs of the analog reconstruction filters identifies a significant amount of group delay, the problem may be caused by non-linearities in the reconstruction filters *(Fig. 3)*. Improper implementation of the digital filters also can affect the frequency response.

The impact of the RF section on signal quality may be determined by comparing the baseband and RF spectrums. An example of such a comparison shows degradation in the adjacent-channel performance of a PDC transmitter *(Fig. 4)*. Further examination indicates that non-linearities in the I-Q modulation and upconversion chain created some spectral regrowth in the adjacent channels.

Measured as a function of time, EVM can also be used to uncover low-level spurs created by the RF chain. The EVM time record can be transformed into the frequency domain by means of an FFT algorithm. The resulting EVM spectrum is a measure of the spectral content of the error. Within the modulation bandwidth of the signal, the spectrum should be nearly flat. The presence of discrete spectral lines indicates spurs *(Fig. 5)*. The EVM spectrum is an extremely accurate and sensitive tool for identifying spurs.

Another measurement, signal coherence, may be used to identify baseband signals that have been unintentionally modulated onto the RF signal. Signal coherence is defined as:

$$\text{Coherence} = Sxy(w) \times S^*xy(w) / Sxx(w) \times Syy(w)$$

where

Sxy(w) = cross power spectrum for two random processes, X(t) and Y(t),

S*xy(w) = complex conjugate of Sxy(w),

Sxx(w) = the power density spectrum of a random process, X(t), and

Syy(w) = the power density spectrum of a random process, Y(t).

Coherence values, which range between zero (no coherence) and one (complete coherence), may be used to compare potential signal sources in the block diagram of a transmitter to the RF output. A high-frequency probe is used to probe different locations within the block diagram. A high level of coherence between a baseband signal source and the RF signal indicates that this source has been unintentionally modulated onto the output signal and is degrading the performance of the transmitter *(Fig. 6)*.

Traditional signal analysis is still well suited to measuring many of the transmitter performance characteristics of the new wireless phones. But vector signal analysis, with its array of powerful measurement tools like EVM, EVM spectrum, and coherence, enables designers to effectively test all sections in today's typical block diagrams.

Matt Bellis is Business Development Engineer at Hewlett-Packard's Microwave Instrument Div., He is responsible for understanding the test needs of the wireless communications industry. Bellis received a BSEE and BA in physics from Northwestern University, Evanston, Ill. and an MSEE from the University of California at Santa Barbara.

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	R3261C(CN)/ $13,950	30 Hz-1 MHz	9 kHz-2.6 GHz	±25 Hz (@ 1 GHz)	–119 to +30 dBm	±0.5 dB	116 dB	Card reader; quasi-peak detector; am/fm demodulator; IEEE-488 std.; CN module has 75-Ω input.
	U4941(N)/ $14,500	1 kHz-3 MHz	9 kHz-2.2 GHz	±2 kHz (@ 1 GHz)	–117 to +30 dBm	±1.0 dB	107 dB	Preamplifier; am/fm demodulator; quasi-peak detector; IEEE-488 std.; N model has 75-Ω input.
	U3641/ $15,800	1 kHz-3 MHz	9 kHz-3 GHz	±2.16 kHz (@ 1 GHz)	–135 to +20 dBm	±2.0 dB	107 dB	Portable; color display; PCMCIA slot; IEEE-488 std.
	R3261D/ $19,865	30 Hz-1 MHz	9 kHz-3.6 GHz	±25 Hz (@ 1 GHz)	–119 to +30 dBm	±1.0 dB	116 dB	Card reader; quasi-peak detector; am/fm demodulator; IEEE-488 std.
	R3361C(CN)/ $19,980	30 Hz-1 MHz	9 kHz-2.6 GHz	±25 Hz (@ 1 GHz)	–119 to +30 dBm	+0.5 dB	116 dB	Same as R3261C(CN), plus tracking generator.
	R3263/ $21,000	300 Hz-5 MHz	9 kHz-3 GHz	±75 Hz (@ 1 GHz)	–115 to +30 dBm	±1.5 dB	110 dB	PCMCIA slot; am/fm demodulator; GSM, DCS1800, PCS 1900 analysis functions.
	R3361D/ $25,795	30 Hz-1 MHz)	9 kHz-3.6 GHz	±25 Hz (@ 1 GHz)	–119 to +30 dBm	±1.0 dB	116 dB	Same as R3261D, plus tracking generator.
	R3463/ $27,500	300 Hz-5 MHz	9 kHz-3 GHz	±75 Hz (@ 1 GHz)	–115 to +30 dBm	±1.5 dB	110 dB	PCMCIA slot; am/fm demodulator; demodulator for digital mobile radio.
	R3272/ $28,990	300 Hz-3 MHz	9 kHz-26.5 GHz	±200 Hz (@ 1 GHz)	–115 to +30 dBm	±4.0 dB	110 dB	PCMCIA slot; am/fm demodulator; IEEE-488 std.
	R3265A/ $32,250	10 Hz-3 MHz	100 Hz-8 GHz	±106 Hz (@ 5 GHz)	–135 to +30 dBm	±2.0 dB	130 dB	Card reader; quasi-peak detector; am/fm demodulator; IEEE-488 std.
	R3465/ $32,995	300 Hz-5 MHz	9 kHz-8 GHz	±75 Hz (@1 GHz)	–115 to +30 dBm	±1.5 dB	110 dB	Same as R3463.
	R3271A/ $36,364	10 Hz-3 MHz	100 Hz-26.5 GHz	±210 Hz (@ 10 GHz	–123 to +30 dBm	±4.0 dB	130 dB	Card reader; quasi-peak detector; am/fm demodulator; IEEE-488 std.
	R3365A/ $42,750	10 Hz-3 MHz	100 Hz-8 GHz	±106 Hz (@ 5 GHz)	–135 to +30 dBm	±2.0 dB	130 dB	Same as R3265A, plus tracking generator.
	R3371A/ $50,500	10 Hz-3 MHz	100 Hz-26.5 GHz	±210 Hz (@10 GHz)	–123 to +30 dBm	±4.0 dB	130 dB	Same as R3271A, plus tracking generator.

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The HP ESA-L1500A is a fully synthesized RF spectrum analyzer designed to test telecommunications equipment in rugged and diverse field environments. The portable, 27-lb. instrument is encased in rubber and has a rain-resistant front panel, shielded vents, and a side-mounted fan to ensure accurate operation in adverse weather. It requires only a five-minute warmup and features an automatic, internal background calibration function for accurate measurements over a wide temperature range. Ease of use features include one-button measurement of bandwidth, third-order intercept, and amplitude modulation, as well as a backlit high-resolution digital display with an 85-dB log display range. Frequency range is 9 kHz to 1.5 GHz with a ±2.0-kHz accuracy. Phase noise at a 10-kHz offset is –90 dBc or better, and residual FM is 100 Hz p-p or better. Sensitivity is –120 dBm or better. The HP ESA-L1500A costs $7300. An optional tracking generator costs $3000. Delivery is in four weeks.

Hewlett-Packard Co., *Test and Measurement Org., P.O. Box 50637, Palo Alto, CA 94303-9512; (800) 452-4844 ext. 5053.* **CIRCLE 628**

Lightweight Analyzers Cover 8.1-GHz Range

A pair of portable spectrum analyzers cover the 9-kHz-to-8.1-GHz range and weigh only 26 lb. The MS2653A has a dynamic range of 105 dB, an average noise level of less than or equal to –110 dBm, and noise sidebands of less than or equal to –90 dBc/Hz at a 10-kHz offset. The MS2663A has a dynamic range of –110 dB, an average noise level of less than or equal to –115 dBm, and noise sidebands of less than or equal to –100 dBc/Hz. Total level accuracy is ±1.3 dB from 100 kHz to 3.1 GHz and ±1.8 dB from 3.1 GHz to 8.1 GHz. Automatic measurements include burst power, adjacent-channel power, occupied bandwidth, and channel power. Options include a 1-Hz resolution frequency counter, high-speed time-domain sweep, internal and external trigger with gating function, AM/FM demodulator, and FM demodulation waveform display. The color CRT display allows display of two signals or measurements. The MS2653A's U.S. price is $17,500, and the MS2663A's U.S. price is $20,000.

Anritsu Wiltron Co., *485 Jarvis Dr., Morgan Hill, CA 95037; (408) 776-8300; fax (408) 776-1744.*

CIRCLE 629

SPECTRUM ANALYZERS

Manufacturer	Model/Price	Resolution bandwidth	Frequency Range	Frequency Accuracy	Amplitude Range	Amplitude Accuracy	Dynamic range	Remarks
Analogic Corp. 8 Centennial Dr. Peabody, MA 01960 (508) 977-3000	6500/$20,970	260 µHz-500 kHz	to 125 MHz	0.01%	±12.5 mV to ±10 V	1%	54 dB	Multifunction instrument with 660-1 spectrum analyzer plug-in module; on-board signal processing.
Anritsu Wiltron Co. 685 Jarvis Dr. Morgan Hill, CA 95037 (408) 776-8300	MS2651A/ $11,550	1 kHz-5 MHz*	9 kHz-3 GHz	2 ppm/year	-110 dBm to +30 dBm	æ1.1 dB	>105 dB	*30, 100, and 300 Hz available with narrow-resolution-bandwidth option.
	MS2661A/ $14,150	1 kHz-5 MHz*	9 kHz-3 GHz	2 ppm/year	–115 dBm to +30 dBm	±1.1 dB	>110 dB	*30, 100, and 300 Hz available with narrow-resolution-bandwidth option.
	MS2653A/ $17,500	1 kHz-5 MHz*	9 kHz-3 GHz	2 ppm/year	–110 dBm to +30 dBm	±1.3 dB <3 GHz; ±1.8 dB >3 GHz	>105 dB	*30, 100, and 300 Hz available with narrow-resolution-bandwidth option.
	MS2663A/ $20,000	1 kHz-5 MHz*	9 kHz-3 GHz	2 ppm/year	–115 dBm to +30 dBm	±1.3 dB <3 GHz; ±1.8 dB >3 GHz	>110 dB	*30, 100, and 300 Hz available with narrow-resolution-bandwidth option.
	MS2602A/ $26,765	10 Hz-3 MHz	100 Hz-8.5 GHz	$<1 \times 10^{-7}$/ year	–135 to +30 dB	±1.1 dB	>134 dB	
B&K-Precision Div. 6470 W. Cortland St. Chicago, IL 60635 (312) 889-1448	2615/$1795	12.5 kHz	150 kHz-500 MHz	100 kHz	–100 to +13 dBm	2 dB	80 dB	
	2620/$2195	12.5 kHz	150 kHz-500 MHz	100 kHz	–100 to +13 dBm	2 dB	80 dB	Built-in tracking generator.
	2625/$2695	12.5 kHz	150 kHz-1050 MHz	100 kHz	–100 to +13 dBm	2 dB	80 dB	Built-in am/fm demodulator.
	2630/$3395	12.5 kHz	150 kHz-1050 MHz	100 kHz	–100 to +13 dBm	2 dB	80 dB	Built-in tracking generator; am/fm demodulator.
Hameg Instruments Inc. 266 East Meadow Ave. East Meadow, NY 11554 (516) 794-4080	HM5005/ $1795	20/250 kHz	125 kHz-500 MHz	±100 kHz	–100 to +13 dBm	±2 dB	113 dB	Includes four-digit LED readout of center or marker frequency; am/fm demodulation.
	HM5006/ $2195	20/250 kHz	125 kHz-500 MHz	±100 kHz	–100 to +13 dBM	±2 dB	113 dB	Same as HM5005 plus tracking generator.
	HM5010/ $2595	20/400 kHz	125 kHz-1050 MHz	±100 kHz	–100 to +13 dBm	±2 dB	113 dB	Same as HM5005.
	HM5011/ $3395	20/400	125 kHz-1050 MHz	±100 kHz	-100 to +13 dBm	±2 dB	113 dB	Same as HM5006.
H.C Protek Inc. 154 Veterans Dr. Northvale, NJ 07647 (201) 767-7242	P-7802/$2995	1 MHz	1-1000 MHz	±1%	+15 to +129 dBµ	±2 dB	70 dBµ	

Advanced PCB^3

Printed Circuit Board Design Server for EDA/Client

Constraints and Rule Scripts bring rules-driven PCB layout to the desktop. Features real-time design rule checking, high-speed design capability, 8 Signal layers, 4 power planes and intelligent split planes. Component Wizard automates footprint creation. This top-to-bottom re-engineered PCB design tool is seamlessly integrated with other EDA/Client plug-ins.

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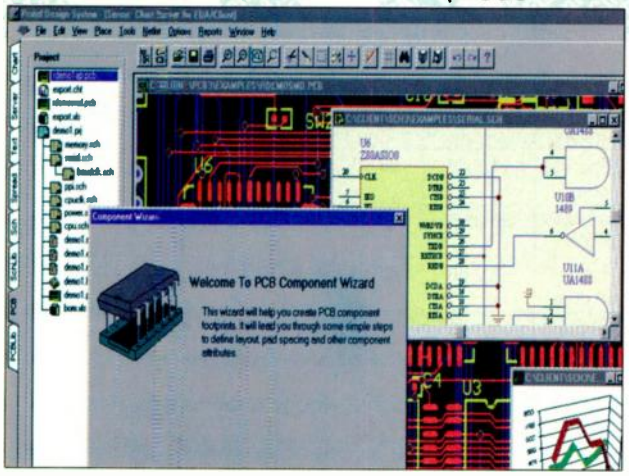

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Schematic Capture Server for EDA/Client

Advanced Schematic was the first Windows-based schematic capture system to provide engineers with a design tool that supported industry standard OrCAD® design files and libraries. Advanced Schematic 3 carries the designer beyond the boundary of today's EDA desktop. Engineered to "plug-in" to tomorrow's multi-user/multi-tool environment.

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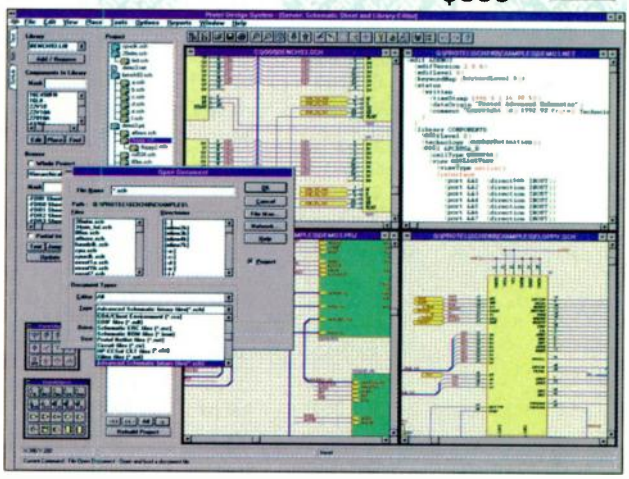

Advanced PLD^3

Programmable Logic Design Server for EDA/Client

Integrated, versatile and powerful development environment for Programmable Logic. Advanced PLD brings a new degree of integration to PLD design. Based on the industry-standard CUPL Hardware Description Language, Advanced PLD includes editing, compiling and simulation tools supported by a comprehensive and expandable collection of device libraries.

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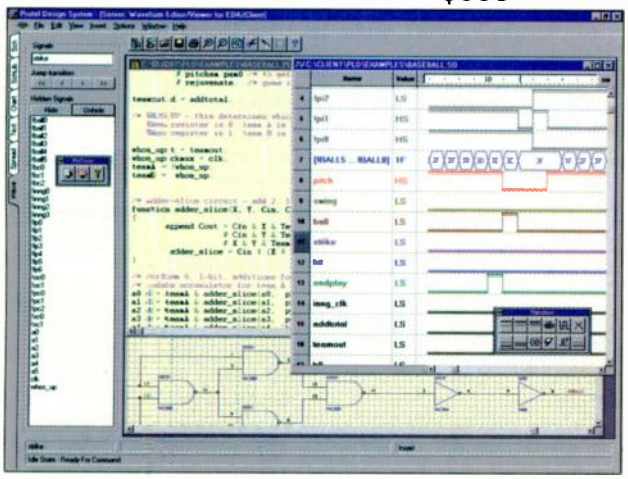

Advanced Route^3

Shape-Based Autorouter Server for EDA/Client

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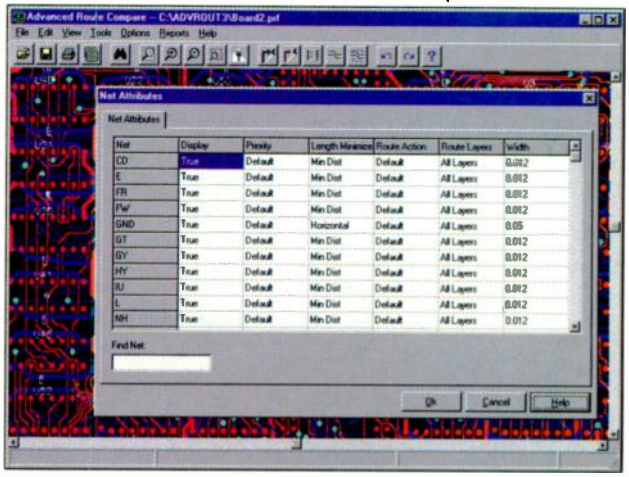

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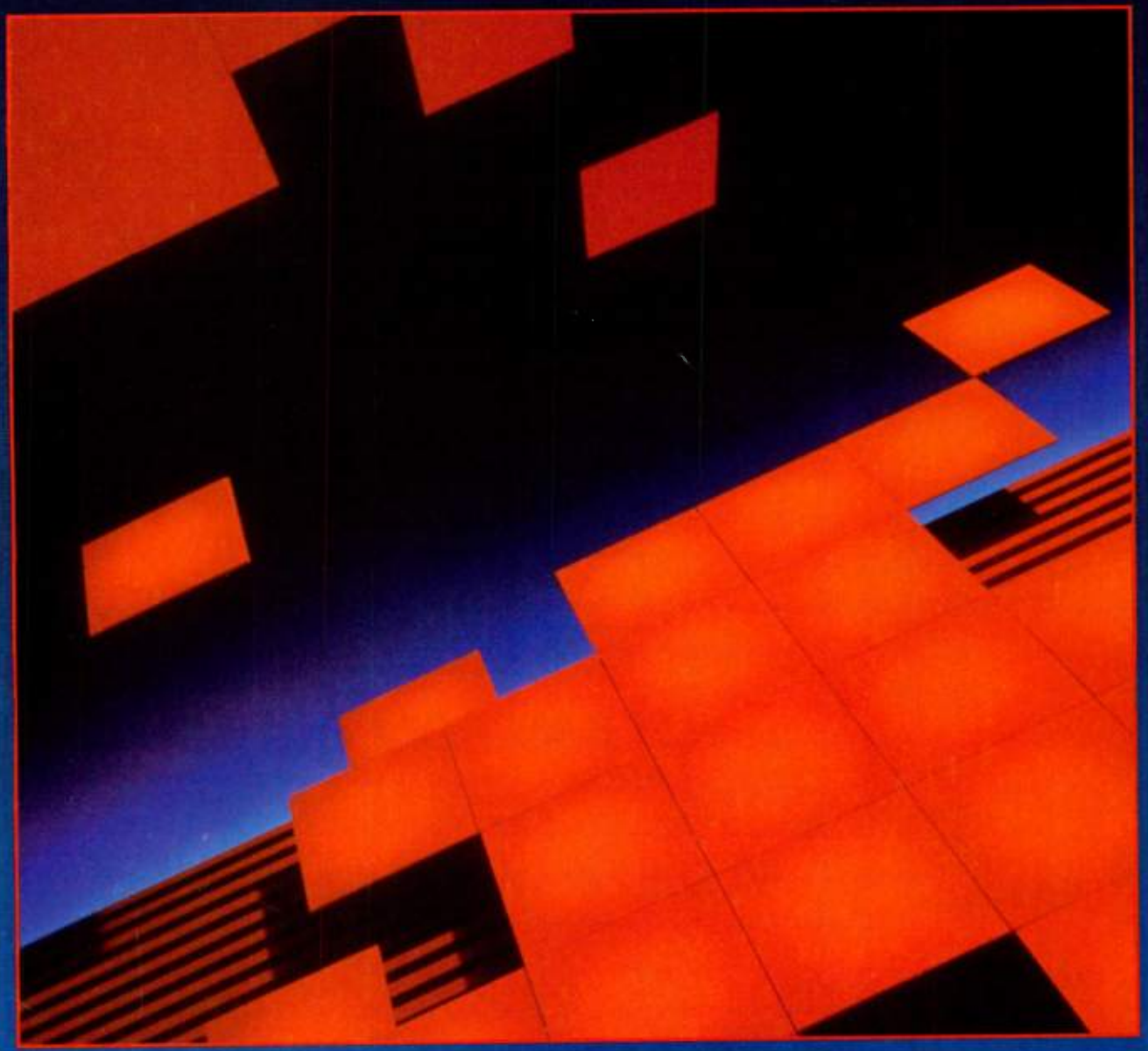
READER SERVICE 165

SPECTRUM ANALYZERS

Manufacturer	Model/Price	Resolution bandwidth	Frequency Range	Frequency Accuracy	Amplitude Range	Amplitude Accuracy	Dynamic range	Remarks
Hewlett-Packard Co. Direct Marketing Org. P.O. Box 58059 MS51L-SJ Santa Clara, CA 95051-8059 (800) 452-4844 ext. 5054	ESA-L1500A/ $7300	1 kHz-3 MHz	9 kHz-1.5 GHz	+2.0 kHz (@ 1 GHz)	–120 to +30 dBm	±1.5 dB	85 dB	Built-in tracking generator opt.
	HP 3560A/ $7960	625 µHz-1440 Hz	62.5 µHz-40 kHz	±8 Hz	5 mV to 5 V	±0.5 dB	60 dB	Portable, 7-lb, battery-powered unit.
	HP 8591E/ $11,750	30 Hz-3 MHz	9 kHz-1.8 GHz	±210 Hz (@ 1 GHz)	–130 to +30 dBm	±1.7 dB	90 dB	Built-in tracking generator opt.
	HP 35665A/ $13,500	322 µHz-920 Hz	122 µHz-102.4 Hz	±3 Hz	3.99 mV to 31.7 V	±0.5 dB	78 dB	Computed-order tracking, arbitrary source opt.
	HP 8594E/ $14,250	30 Hz-3 MHz	9 kHz-2.9 GHz	±210 Hz (@ 1 GHz)	–127 to +30 dBm	±1.7 dB	88 dB	Built-in tracking generator opt.
	HP 8591C/ $14,500	30 Hz-3 MHz	1 MHz-1.8 GHz	±210 Hz (@ 1 GHz)	–115 to +30 dBm	±1.7 dB	88 dB	Built-in tracking generator opt.
	HP 35670A/ $17,250	122 µHz-512 Hz	122 µHz-102.4 kHz	±0.003%	3.99 mV to 31.7 V	±0.2 dB	90 dB	Portable FFT and real-time analyzer.
	HP 8595E/ $20,400	30 Hz-3 MHz	9 kHz-6.5 GHz	±210 Hz (@ 1 GHz)	–125 to +30 dBm	±2.2 dB	86 dB	Built-in tracking generator opt.
	HP 8592L/ $20,500	1 kHz-3 MHz	9 kHz-22 GHz	±20 kHz (@ 10 GHz)	–102 to +30 dBm	±2.7 dB	71 dB	9 kHz to 26.5 GHz opt.
	HP 3562A/ $22,050	12 µHz-450 Hz	64 µHz-100 kHz	±4 Hz	3 mV to 22.4 V	±0.15 dB	85 dB	High-performance analog spectrum, network, and transient analysis.
	HP 3588A/ $24,000	0.004 Hz-17 kHz	10 Hz-150 MHz	±225 Hz	–150 to +26 dBm	±0.3 dB	80 dB	Built-in tracking generator; 3.5-in floppy drive.
	HP 8596E/ $24,600	30 Hz-3 MHz	9 kHz-12.8 GHz	±1.2 kHz (@ 10 GHz)	–127 to +30 dBm	±2.7 dB	102 dB	Built-in tracking generator opt.
	HP 3589A/ $24,750	0.004 Hz-17 kHz	10 Hz-150 MHz	±225 Hz	–150 to +26 dBm	±0.3 dB	80 dB	Same as HP 3588A, plus network analysis.
	HP 3567A/ $24,900	64 µHz-4096 Hz	64 mHz-102.4 kHz	±0.8 Hz	1.26 mV to 39.8 V	±0.15 dB	80 dB	2-to-48-channel modular, PC-based system.
	HP 8560E/ $26,500	1 Hz-2 MHz	50 Hz-2.9 GHz	±106 Hz (@ 1 GHz)	–145 to +30 dBm	±1.85 dB	103 dB	Built-in tracking generator opt.; meets MIL-SPEC.
	HP 8593E/ $26,800	30 Hz-3 MHz	9 kHz-22 GHz	±1.2 kHz (@ 10 GHz)	–117 to +30 dBm	±2.7 dB	103 dB	Built-in tracking generator opt.; 9 kHz to 26.5 GHz opt.
	HP 3563A/ $27,450	12 µHz-450 Hz	64 µHz-100 kHz	±4 Hz	3 mV to 22.4 V	±0.15 dB	85 dB	Same as HP 3562A, plus digital input and Z-domain analysis.
	HP 89410A/ $29,050	350 µHz-3 MHz	dc-10 MHz	±2 Hz (@ 10 MHz)	–170 to +24 dBm	±0.5 dB	80 dB	Includes time and modulation domain, analog or digital demodulation, I-Q inputs, network analysis.
	HP 4195A/ $29,500	3 Hz-300 kHz	10 Hz-500 MHz	±1 kHz	–140 to +20 dBm	±1 dB	89 dB	Includes vector network analyzer.
	HP 3566A/ $29,500	64 µHz-12.8 kHz	64 µHz-12.8 kHz	±0.1 Hz	5 mV to 10 V	±0.15 dB	72 dB	8- or 48-channel modular, PC-based system.
	HP 8561E/ $31,600	1 Hz-2 MHz	30 Hz-6.5 GHz	±106 Hz (@ 1 GHz)	–145 to +30 dBm	±1.85 dB	103 dB	Meets MIL-SPEC; tracking generator opt.
	HP 8567A/ $33,350	1 kHz-3 MHz	10 kHz-1.5 GHz	±5 kHz (@ 1 GHz)	–115 to +30 dBm	±2 dB	83 dB	Tracking generator opt.
	HP 8562E/ $33,500	1 Hz-3 MHz	30 Hz-13.2 GHz	±106 Hz (@ 1 GHz)	–151 to +30 dBm	±3 dB	108 dB	
	HP 4396A/ $34,600	1 Hz-3 MHz	2 Hz-1.8 GHz	±5.5 kHz*	–145 to +30 dBm	±1 dB	107 dB	Includes vector network analysis. *130-Hz accuracy opt.
	HP 8563E/ $36,700	1 Hz-2 MHz	30 Hz-26.5 GHz	±1 kHz (@ 10 GHz)	–148 to +30 dBm	±3 dB	109 dB	Meets MIL-SPEC; tracking generator optional.
	HP 8568B/ $43,350	10 Hz-3 MHz	100 Hz-1.5 GHz	±260 Hz (@ 1 GHz)	–135 to +30 dBm	±2 dB	97 dB	
	HP 8564E/ $49,500	1 Hz-2 MHz	30 Hz-40 GHz	±1 kHz (@ 10 GHz)	–147 to +30 dBm	±3 dB	108 dB	
	HP 71100C/ $52,350	10 Hz-3 MHz	100 Hz-2.9 GHz	±110 kHz (@ 1 GHz)	–134 to +30 dBm	±1.5 dB*	92 dB	Additional functional modules available. *0.9-dB accuracy opt.
	HP 89440A/ $52,500	1 mHz-3 MHz	dc-1.8 GHz	±180 (@ 1 GHz)	–170 to +25 dBm	±0.5 dB typ.	70 dB	Multiformat digital and analog demodulation; time and modulation domain; built-in RF source opt.
	HP 89441A/ $58,100	1 mHz-3 Mhz	dc-2.65 GHz	±180 Hz (@ 1 GHz)	–170 to +25 dBm	±1.1 dB typ.	75 dB	Same as HP 89440A.

CAREER OPPORTUNITIES
IN ELECTRONIC ENGINEERING

February 1997



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There's No Shortage Of Cubicle Space If You're A Good Engineer

Paul McGoldrick

The time was, not so long ago, that a person joined an employer's staff and stayed with that company for a long time; my father did that, a brother-in-law is still doing that (although in quiet contract times he has been "leased out"to other civil contractors.) But times have changed and most working people have, or will have, multiple employers on their resumes. It is said that the current average is about five employers and that within the next 20 years it will have increased to seven. The loyalty that the employee exhibited in both good times and bad has faded with the reality that the employer will not, in most cases, be burdened with extra costs during the bad times.

In a typical engineering career, an engineer will change companies more frequently and for more reasons than a non-engineer. If your technology is quite specialized, you may see movement as the only method of gaining a broad experience in the market; or you may be frustrated by the conservative, liberal, cash-cow, management-challenged (or whatever) nature of your present company, and see others as being more progressive. A lot of changes in Silicon Valley happen because someone has an idea and the only way to get it done is to get entrepreneurial. What we see little of in the Valley is movement to other companies strictly for the money–money changes.

We also are seeing in the engineering profession a much stronger movement toward the self-employed categories; five years ago, the title "consultant" was a euphemism for "unemployed" in all but a few cases. The label would not, for example, qualify you for a subscription to this magazine. Now that is not so and many engineers are earning more than just a decent living. And there are other ways of being employed without clocking in and out every day. In this article, let's look at some of these opportunities as well as the areas where engineering talents are most wanted and best rewarded.

We are all brought up with preconceptions. In many cases the more "civilized" our upbringing, the more preconceptions we have. For many of us, the notion of employment is paramount, and the idea of unemployment is a little frightening and socially embarrassing. That is not the most ideal of situations, of course, when a person needs the highest level of support and networking, but it is a basic fact of life for most of us. The notion of just having a "job," however, is something we have been able to overcome without any problem, and no young adult is released into the employment world without being absolutely aware that they can be and do anything they want. That would not have been the case in the time of the Great Depression. But, given that we now all expect a "career" instead of a "job," it should be easier to make changes, to think of changes, and to be always on the lookout for things that might be done differently.

Gaining Respect

Not actually being employed, by being on the books of a single employer, has taken a while to become "respectable" in electronics. It also is surprising how many independents are out there. It is still only a small percentage, but there is now a significant force working for themselves. It cannot be a situation for everybody, and it almost certainly isn't for the newly-qualified, but it can be profitable, and professionally rewarding. The actual role that these independents take is mixed but the common situations are as contractors and consultants. There are both semantic and practical differences in the titles and the actual work functions tend to be defined as "lump" or complete jobs, or tasks, and are performed by the contractor, while "on-going" advice or work is the task of the consultant.

There are problems with the way that some companies would like to define "contractor" and the way that the IRS defines the title. In short, if you are contracting work with only ONE company, you (and the company) will likely be targeted by the IRS as an employee hiding in a tax avoidance role. Working for more than one company in a tax year should avoid such accusations. Most independents seem to start by chance: The moonlighting work gets too much to moonlight; the frustration of the job drives an investigation of another company or networking contact; somebody gets laid off and then contracts work back with the same company. But such accidental entries are probably not the best long-term ideals. If you want to be a successful, independent engineer, here are some essential points to consider:

- Are you sure you know the field well enough without others to help?
- Can you work well without a team backing and supporting you?
- Is your specialization SO narrow that there will be little demand?
- Are you happy talking money and TELLING people what you need?
- Do you listen?
- Do you really understand deadlines?
- Do you understand that project failure means no future work?
- Do you have enough contacts at enough companies to get enough work?
- Are those contacts going to be around long enough?
- Do you understand that the hours you work are whatever it takes?
- Do you have your family's support?
- Are you able to obtain the medical insurance you want/need?

By far the most important thing to think about when venturing out as an independent is, curiously, your long-term goals. Is contracting something you always wanted to do, something you always COULD do? How does your knowledge base grow to keep up with changes? There is a grave danger that if you don't think long-term, you will become unemployable. You can make good money as an independent. Currently, in Silicon Valley, the returns for a contractor are between 30 and 60% more than a full-time employee doing the same tasks. But the downside is that you need to focus, focus, focus.

Another way of being quasi-independent is to work through temp agencies. The jobs often have the advantages of being flexible, well-paying, and give great all-round experience of different industries and other engineers, with the disadvantage that the end of

one job rarely perfectly coincides with the start of another. Some agencies offer benefits, some don't.

Industries

In terms of sheer numbers, there are two major growth areas, and both are surprising compared to a year ago–commercial airplanes and quasi-commercial satellites. Lockheed-Martin will add 3,000 new engineering positions in the Bay Area (Northern California) in the near future to fulfill the contracts already won in the satellite business; those positions are in addition to numerous current vacancies. In the Northwest, Boeing has so many vacancies in the engineering areas that they are now advertising in newspapers around the U.S. and in the professional journals in Europe.

Nearly anything to do with the Internet is, of course, hot. However, the staying power of a number of companies is questionable–the medical electronics fields are growing very fast; digital video and audio systems are really strong; personal communications systems are expected to be one of the hardiest sectors for a number of years; telecommunications in general and fiber, in particular, are expected to be major growth areas in both volume and also technology.

Private-sector jobs are still the largest group for engineers, with defense opportunities continuing to dwindle, and even evaporate. State jobs are increasing as are Federal areas involving large database activities, such as law enforcement.

Digital Hotspots

There aren't many really hot employment areas in the purely digital design arena. One reason is undoubtedly that the colleges in the U.S. are still producing too many digital engineers. For the semiconductor designer, a complete understanding of high-speed digital CMOS is essential and the non-CPU-type opportunities are in SRAM and VLSI. Test engineers are needed across the board, as are product managers and program managers. A good technical writer also is a highly-employable commodity across all industries. There are numerous opportunities for digital design engineers to work in the mixed-signal companies, but there are few who will hire an engineer who does not at least appreciate the needs of the analog side and absolutely show a desire and talent for learning them.

On the software side, various minor explosive areas exist at present and for what looks like the immediate future. Across the board the needs are for Windows NT and 95, UNIX, C, C++, TCP/IP, and there are increasing demands for Active X, ABAP/4, Perl, Java, Visual Basic, and CGI scripting:

- Applications software and database administration for client/servers
- Network software
- Oracle development and database management
- Web site development
- 64-bit SPARC software
- VLSI applications software
- Business modeling software
- Platform harmony, particularly applications development
- GUI developers
- Web servers development
- Games and interactive developments

One increasingly important area is software QA and test. Some jobs have already started to appear, and more will be seen as companies find different ways of defining the positions and the authority to be given the positions.

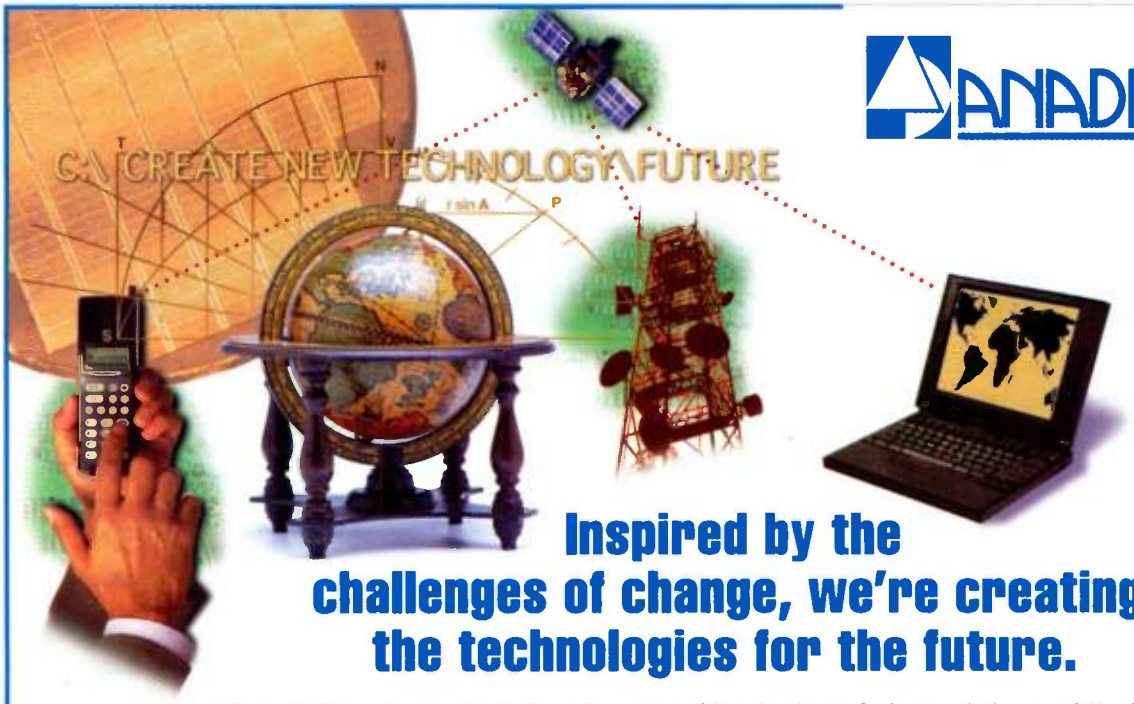
Mixed Signal And Analog

The employment opportunities for a good analog or mixed-signal engineer have never been better; if your analog experience is in RF, you are probably on the regular calling lists of a half-dozen recruiters. Semiconductor design engineers are needed across the whole range of industries, as are design managers, process engineers, and product personnel. Increasingly, manufacturers are thinking as systems companies and the best employees for them are those who have good communications skills with the customers and enough marketing savvy to cut through a lot of the hype that tends to always come back through the sales channels.

A major, largely undefined area, is in testing. The industry as a whole agrees that things need to change, and quickly, but the dedicated talent has not been drawn into the field, and most companies have not been able to get into the "chicken-and-egg" loop of who, how, when. They will do so within the next year.

Things are so open at the moment that if a small group of good analog design engineers were to get together and decide they wanted to live in Montana, they would probably find a "buyer" among the semiconductor manufacturers to set them up as a design center.

Paul McGoldrick is Analog Technology Editor at Electronic Design magazine. He can be contacted through Electronic Design's San Jose office at (408) 441-0550, ext. 113, or by e-mail: 102447.346@compuserve.com.



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SENIOR DESIGN ENGINEER

Independently designs and develops new RF IC products to volume production. Duties include electrical, mechanical layout, packaging and assembly design. Characterizes, models and analyzes devices such as FETs, diodes and passive components. Designs and purchases test fixtures and setups. Provides customer support on technical matters.

BSEE required, MSEE or higher a plus. Must have 5 years of directly related experience and broad background in characterization and applications of ICs for RF and Microwave. Will need to work independently with minimal supervision and train other engineers/technicians. ***JOB #96-280/CEE***

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Designs cellular radio controllers using available 8 bit microcomputers and is responsible for baseband signal processor applications using D.S.P. devices.

BSEE and at least 2 years of related experience that includes knowledge of microcontroller hardware and programming skills in C/Assembly required. Must be able to work independently. ***JOB #96-252/CEE***

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BSEE and 2-3 years of experience with RF IC design required. ***JOB #96-265/CEE***

DEVICE ENGINEER

Electrically characterizes new devices and circuits. Supervises layout, manufacturing and assembly of new device and develops test program for new devices. Evaluates new equipment for processing/device development and testing. Supports the improved M gauge resistivity program used in manufacturing. Conducts technology development for advanced passive components.

BS in Electrical Engineering, Physics or equivalent and at least 5 years of experience assembling and manufacturing power devices required. Must have design experience in power devices, specifically GaAs FETS. Background in device physics, processing, modeling and thermal design essential. ***JOB #95-72/CEE***

SENIOR ASSEMBLY/ PACKAGING ENGINEER

Responsible for new process development, continuing process improvement/cost reduction; troubleshooting, defining production control monitor systems; performing audit to process specification: writing process specifications; setting up new equipment and assisting in transfer of new products from Engineering to Production.

Must have electronic packaging experience; die attach, wire bonding, encapsulation, plastic molding, cleaning, epoxy adhesive and assembly, marking systems and molding compounds. ***JOB #96-17/CEE***

TEST ENGINEER

Designs, builds and maintains RF/Microwave Rack and Stack Test Systems; writes, compiles, debugs and documents production test and probe programs; generates schematics, drawings and equipment specifications as needed and provides guidance for test technician on system troubleshooting and repairs.

Must have RF/Microwave knowledge and 3+ years of experience. Exposure to PC/Automated testing required. Knowledge of Visual Basic/Basic Programming and RF/Microwave test equipment essential. ***JOB #96-146/CEE***

PACKAGING ENGINEER

Designs and develops surface mount packages.

BS/MS in Mechanical Engineering or Materials Science and at least 2 years of experience in electronic packaging or equivalent required. Will need background in thermal characterization, analytical skills and qualification of materials. ***JOB #96-144/CEE***

PRODUCT ENGINEERS

Monitors yield, analyses, summarizes and provides corrective action for electrical or visual failures. Designs experiments, Fab through life test, to improve processes for higher yield products; determines lot wafer/ dispositioning; verifies quality final test and calibration.

BSEE required. Must have at least 5 years of experience or similar technical background. Will also need basic knowledge of semiconductor fabrication, testing and packaging. ***JOB #96-198/CEE***

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time, Pacific Bell will look for engineers that can operate a system as well as develop new applications and services. "We are just seeing a tip of the glacier in applications," Lowry says. PCS technology, he adds, is going to have to grow vertically at a rapid pace.

Foreign Engineers

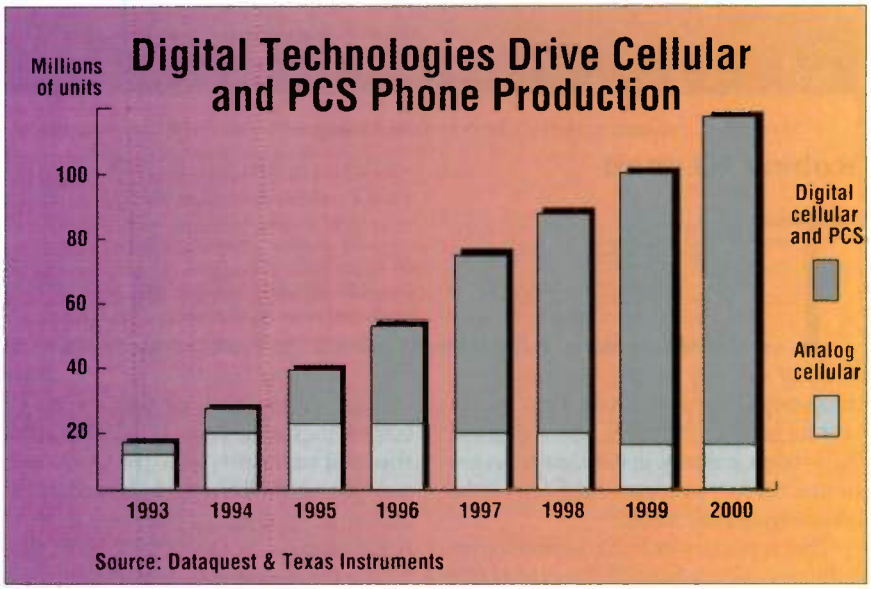
To increase the pool of candidates, some PCS companies are recruiting internationally--especially for operators of GSM–based systems.

Omnipoint is one company that has looked abroad to fill positions. The company, which is developing a composite time-division-multiple-access (TDMA)/code-division-multiple-access (CDMA) system, launched its initial network using a GSM platform. (GSM is a European-based technology.) As a result, Garelick says that there is a shortage of engineers in the U.S. with experience in this technology. To find the technical knowledge it needs, he says that Omnipoint has hired a number of engineers from Europe.

Pacific Bell has turned to the international arena for the same reason. According to Lowry, the company, which is developing a GSM-based system, has filled key engineering positions with engineers from Europe, Australia, and Asia.

Recruiting internationally does pose some challenges for companies. One of them is dealing with the strict U.S. immigration laws, which makes international recruiting a long and expensive process.

To deal with these laws, Pacific Bell has



Digital wireless technology started to take shape in 1996. With the roll-out of more PCS systems in 1997, digital technology is expected to dominate phone production.

employed a third-party company to contract foreign engineers on its behalf, as well as to deal with all immigration issues. Lowry says that by using this third-party contractor, Pacific Bell quickly staffed positions with foreign engineers. The company also learned the policies and procedures associated with hiring foreign engineers.

Now, Pacific Bell internally handles all international recruiting and deals with all immigration issues.

Omnipoint takes a different approach to dealing with immigration issues. According to Garelick, there are a number of U.S. citizens working in Europe on GSM systems. He says that by hiring these engineers, Omnipoint avoids the immigration process. "When we have U.S. citizens looking to get back, it is a plus for us," Garelick says.

College Grads

College campuses also have opened another recruiting door for PCS service providers. With more U.S. colleges and universities focusing on wireless technology, more college graduates are leaving school with a background in RF, network, digital-signal-processing (DSP), and software design. As a result, more service providers are turning to recent graduates to fill their engineering openings.

Omnipoint is one company turning to this arena. At the start, Omnipoint did not recruit college engineers. Garelick says that as a start-up company in the PCS business, Omnipoint needed engineers that could hit the ground running.

However, now that Omnipoint has started the initial launch of its system, more college graduates will be hired to fill engineering openings.

Recent graduates are also starting to play a bigger role in Pacific Bell's recruiting efforts. Lowry says that Pacific Bell has not fully developed its college recruiting program. But, to try and land these engineers, the company is encouraging current employees to promote Pacific Bell at the colleges and universities from which they attended.

AT&T Wireless, Kirkland, Wash., also actively recruits from colleges. Christine Bertany, director of staffing for AT&T Wireless, says that the pool of qualified candidates within the industry is getting smaller. As a result, she says that it is important for the company to hire and train less-experienced engineers–like college graduates. To train these engineers, AT&T has set up an engineering development program that provides in-class and hands-on experience for less-experienced engineers

The service providers are not alone in their quest for qualified engineers. Manufacturers of PCS products and components also have encountered similar recruiting problems.

"We have had some problems," says Dave McKay, vice-president and general manager for Ortel, Alhambra, Calif., a supplier of off-air repeaters, in-building distribution systems, and fiber-optic microcells. He says that with more companies entering the wireless business, hiring is getting tougher.

PCSI, San Diego, Calif., which supports and manufactures products for the personal-air-communications-technology (pACT) N-PCS protocol, is in a similar situation. Martha Dennis, vice-president of engineering, says that there are not enough good engineers to go around.

Dan Sullivan, senior vice president of human resources for QUALCOMM Inc., San Diego, Calif., also agrees that recruiting engineers with knowledge of PCS is difficult.

However, Sullivan says that QUALCOMM, developers of CDMA technology and manufacturers of PCS components and phones, has been fortunate in finding and hiring engineers. In fact, at one point, he says that QUALCOMM was hiring 30 to 40 engineers a month.

Sullivan says that there is no magic in QUALCOMM's recruiting scheme. "We stay at it every week and every month." To keep a steady pool of candidates, Sullivan says that QUALCOMM is continually running employment advertising to inform engineers that there are positions open within the company. Resumes received from these advertisements are loaded into a database. This database allows the company's human resource department to track and respond to potential candidates.

QUALCOMM's training program also aids the company in filling openings. Sullivan says that during the recruiting process, the company looks for the best people. Once these people are found, QUALCOMM will teach them what they need to know about wireless communications. "Some companies want engineers to hit the ground running," he says. "That is great when it happens. But how realistic is that? Personally, I don't think that it is. I think some training is expected."

Skills Sought

The trick is finding the best people. When looking for engineers, manufacturers want certain skill sets from a recruit.

According to McKay, Ortel needs both design and applications engineers. In a design engineer, the company wants a person that has RF system and propagation experience as well as the ability to deal with the customer. From an application engineer, Ortel looks for an engineer that understands RF circuitry and has application-specific-integrated-circuit (ASIC) design experince and board layout skills.

Lucent Technologies Microelectronics Group, Berkeley Heights, N.J., is seeking engineers with both a knowledge of GSM and CDMA technologies. Also, according to Aaron Fisher, general manager of wireless products, Lucent needs system engineers, circuit designers, and RF integrated-circuit (RFIC) designers.

QUALCOMM, according to Sullivan, is searching for people with backgrounds in software, digital design, RF design, and system experience. He says that the candidate must have a high intellectual capacity and high cognitive complexity. Good communications skills are another must. Sullivan says that the company works in a team environment and wants its engineer to work together.

PCSI also looks for good communicators. When recruiting an engineer, Dennis says that PCSI tries to sense if the engineer will work best in a team. ``Nothing done in wireless communications is done solo,'' she says, noting that many disciplines must work together to develop wireless products.

Another Hurdle

Finding an engineer is undoubtedly a challenge for both PCS providers and manufacturers. But, it is not the only challenge they share. Once the engineer is hired, the next hurdle for these companies is keeping the engineer.

Companies across the industry say that head-hunters are continually trying to lure their engineers away. To avoid losing an engineer, companies have had to reevaluate working environments, pay scales, and bonus plans.

In any industry, salary is important to employees. But for an engineer, Lowry says, salary is fifth or sixth on the list of reasons why an engineers stays at a company. The top requirement tool for an engineer, he says, is the working environment. According to Lowry, PCS companies have to provide their engineers with a technically challenging environment. For example, he says that while running a trial at the 1996 Republican National Convention in San Diego, Calif., Pacific Bell's engineering staff encountered problems they had never anticipated. In turn, the engineering staff then had to find ways to correct those problems. Lowry says situations like this keep an engineer with a company.

Bertany agrees that working environment is important to the engineer. She says that to keep an engineer, a company must provide an environment that is exciting, challenging, and not bureaucratic.

Stock options are another tool used by PCS companies to keep engineers. Sullivan says that stock options are an effective tool because they give engineers a vested interest in the company. Also, he says that stock options motivate the engineer to make the company successful, because this will in turn increase the engineer's equity.

Robert Keenan is an associate editor at Wireless Systems Design *magazine. He can be contacted at 611 Route 46 West, Hasbrouck Heights, NJ 07604; (201) 393-6250; fax (201) 393-6297, e-mail: robkwsd@aol.com.*

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Develop & Design software for RFTS and similar application in the windows NT/win 95 environment, duties include all aspects of product development including design, documentation, reviews, implementation, integration, test, and release. BSCS/CE, MS preferred. 3+ years c/c++ in windows environment DLL or OLE. Visual basic experience a must.
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CUSTOMER SERVICE ENGINEER
Responsible for software development and support for Wiltron's Manufacturing Divisions Customer Service department; develop calibration and verification of GPIB software for Wiltron microwave products, as well as provide worldwide support to our Field Sales Offices and customers as they develop GPIB software to control their Wiltron Microwave Instruments. Requires a BSEE or BS in Software Engineering or equivalent; the ability to program in Visual Basic; and familiarity with Microsoft Access. Familiarity with C, GPIB, DOS, Windows and UNIX is desired as is an understanding of Microwave test equipment and common Microwave Vector and Scalar measurements. **JOB CODE 490C**

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Develop state of the art Telecommunication Test Equipment. Job duty involves board level hardware design for digital analog, and digital signal processing based systems. Candidate should have strong analytical background, and knowledge in Digital filter design, D/A-A/D converters, DSP real time applications, and digital communication theory. Familiar with OrCAD, SPICE, MathCAD or similar analysis tools. BSEE/MS, 5+ years related experience.
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DIRECTOR OF MARKETING
Organize and supervise the marketing department responsible for definition, justification, development coordination and introduction of all telecom division products. Provide leadership of the division strategic planning process. Manage and recruit product managers who are responsible for market research, internal product proposals, competitive analysis, pricing recommendations and other activities needed to achieve marketing objectives. BSEE and MBA preferred. 15 years minimum experience, preferably in marketing of transmission of test products to telephone.
JOB CODE 800P

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Responsible for product marketing of the Anritsu - Wiltron remote fiber-optic test system (RFSTS). Includes new product definition and justification, market/ competitive analysis, pricing recommendations monitoring sales and profit trends, industry forum involvement (standards committees, etc.), support of product introductions, sales training//literature, travel required. BSEE or BSCS, MBA desirable. 10 years telecom industry experience at least 5 yrs marketing. Excellent written and oral communication and presentation skills.
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JOB CODE 650P

R&D SECTION MANAGER, WINDOWS
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JOB CODE 650P

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You will provide guidance to design effective use of manufacturing and supplier resources for our Manufacturing Division, and act as liaison with engineering to release new products, and define equipment needs for manufacturing. Requires an MSEE or equivalent, 10+ years' engineering experience including supervisory, exceptional project management skills, and knowledge of microwave measurements and instrumentation.
JOB CODE 400F

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Requirements;
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Five Ways Engineeers Can Improve Their Oral Communications Skills

Robert Keenan

In general, the role of the engineer is changing in today's business environment. With the move to flatter organizational structures, engineers find themselves working in cross-functional teams and dealing more openly with the customer on a day-to-day basis.

As a result, a company's view of an engineer is greatly changing. For example, in the past, Hewlett-Packard Co., Palo Alto, Calif., saw its engineers as background players who developed the new products and new technologies the company marketed and sold. Today, however, the company views these same engineers as valuable to expanding and improving business on a national and international basis.

The same holds true for many other companies in the engineering industry. To succeed in this environment, the engineer needs strong technical and communications skills. In particular, good oral communication skills are sought. Below are some tips that can help engineers improve these skills.

I. Know Your Audience

``Before you spend one minute researching your topic, before you write one word of your speech, analyze your audience first," says Joan Detz in her book *How to Write & Give a Speech* (St. Martin's Press, New York, 1992). "The speaker must first understand the audience's familiarity with the subject. How much does the audience already know about the subject? Where did they get their information? How much more do they need or want to know?"

Almost every book or article written on improving public speaking stresses this area. Through proper research, presenters can learn to tailor their speech to meet the needs of the audience, thus allowing them to make a more effective presentation.

In *The Communication Connection* written by James Watson, president of Watson Associates, Mansfield, Ohio, researching the audience is one of the main points."Each audience member is different in their need for information," Watson writes. "It is important to recognize different needs in both." *The Communication Connection* is one section taught under the WRITETALK Communication System which was developed in 1989 by IEEE president-elect Charles Alexander, Wayne Bennett, dean of engineering at Mississippi State University, Oxford, Miss., and Watson. The WRITETALK Communication System is set up to better improve communications skills for students studying engineering in college .

Researching the audience also has benefits outside the formal public speaking arena. In an August 1985 article in the *Public Relations Journal*, James Beckham, Jr. says that in order to better deal with customers or companies, a speaker must identify the topics that are important to that company. This is especially true when dealing with customers. By understanding a customer's product and needs, engineers can more effectively communicate solutions.

II. Use Anecdotes

Whether making a formal or informal presentation, using anecdotes can improve the quality of any speech. By incorporating anecdotes into the speech, the presenter can make points clear to the audience, and the audience can more easily relate to the speech.

"Think of the last time you were sitting with friends and wanted to express an idea, or to make a particular point. You probably told a story to bring that point home," Beckham says. He adds that a speech is a collection of thoughts that a speaker wants to make understandable. One way to accomplish this is through anecdotes.

Watson says that using real-life stories can enhance a speech. However, he says that when looking to use anecdotes in a presentation, the important thing to remember is that the story fits the needs of the audience.

III. Visual Aids

Visual aids can also improve the overall quality of a speech or presentation. When used effectively, displaying printed-circuit boards (PCBs), graphs, block diagrams, or slides can keep an audience interested in a speech. But, when not properly used or planned out, visuals can detract from any oral presentation.

"The use of properly selected and designed visual aids will multiply the effectiveness of the presentation," Watson says. For example, in small informal groups, he says that the use of blackboards, flip charts, and video tapes may be effective. For medium-sized groups (50 to 70 people), overhead transparencies and slides provide good solutions. For larger groups and more professional presentations, 35-mm slides provide excellent visual-aid tools.

The use of visual aids does have its drawbacks. Detz cautions all speakers who use visual aids. "Audiovisual aids are unnecessary if they contribute no information to your speech, fail to help the audience understand or appreciate your message, or actually detract from your role as the speaker." One of the main reasons that Detz says the visual aids are a problem is because speakers use them as a crutch.

As a result, Detz says that is you feel it is necessary to use a visual aid, use them wisely. "One effective technique is to use an audiovisual 'insert.' Prepare a short slide show or a videotape and insert this into your speech as a self-contained unit. The audience can concentrate on the audiovisual segment and then return concentration top the remainder of your speech."

IV. Humor

One of the myths of public speaking is that all speeches need to start with a joke. Although humor may seem one of the best approaches to improving a speech, it can be one of the biggest pitfalls. If delivered right, a joke can lift a speech. But, if delivered wrong, a joke can ruin a speech. "The fact is, humor is risky," writes Schenkein Associates in its "13 Rules For Writing Better Speeches."

"There is nothing worse then a joke that falls flat,"says Detz. The kind of humor that works best in a speech, she says, is the kind that is friendly, personal, and natural. "A few smiles and some chuckles are just fine for your purpose."

There are many books on the market that speakers can buy that will help them to add

humor to a speech. But, according to Detz, it is important for a speaker to learn to create his or her own light touches of humor. "Original material will work better then material that is lifted straight from books." To explain, Detz offers three reasons why:

One of the best ways to bring humor to a speech is through the speaker poking gentle fun at him or herself. But, this technique does have some drawbacks. Detz says that a speaker should never belittle his or her professional competence. This may cause an audience to question the reliability of the speaker and the speech.

V. Delivery

Once the sales presentation or speech is written, the next step is to effectively deliver the speech. Without proper delivery, even the best researched speeches or sales presentations may flop.

Rehearse—Practice is the first step to making a good delivery. "If a speech is a five minute retirement accolade, rehearsal should not take much time," Schenkein Associates says. For more formal presentations, more rehearsal is needed to maximize the forcefulness of the presentation.

"It is not enough to just know the content of your speech," Detz says. "You must also be comfortable with the gestures, pauses, and emphases that will help you get your message across to the audience." Some practice tips that she offers are rehearsing in front of a mirror, presenting the speech to a friend, and practicing in front of a small group.

Eye Contact—After the rehearsal is over, the next step is to make the presentation. In any public speaking or oral communication course, one of the first rules that a presenter learns is to make good eye contact with the audience during the presentation.

"When you look at people, they believe you care about them," Detz says. She adds that a speaker should avoid looking over the audiences' head or at a vague spot on the back of the wall. By looking audience members in the eye, the presenter creates sincerity.

Detz also says that another tip is to avoid focusing on one person. By making eye contact with as many people as possible, the speaker can get the audience more involved with the speech.

Voice—When making presentations, speakers should be concerned with rate, variety, emphasis, clarity, and rhythm. By evaluating each of these areas, a presenter can improve the overall delivery of a speech.

Detz offers some tips to improving the areas. When practicing a speech, she says that a person should time themselves. "Most people speak in public at about 150 words per minute." She also says that a speaker should vary pace and sentences to liven up the speech. Finally, by not slurring words, the presenter can more clearly relay the message to the audience.

Volume is another area the speaker must concentrate on. If the audience cannot hear a speech, the speech is useless to them. Watson says that a speaker must deliver a speech so the farthest person in the room can clearly hear the speech.

Robert Keenan is an associate editor at Wireless Systems Design *magazine. He can be contacted at 611 Route 46 West, Hasbrouck Heights, NJ 07604; (201) 393-6250; fax (201) 393-6297; e-mail: robkwsd@aol.com.*

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Design high-speed digital circuitry for telecommunications products. Three years' experience with PCB-level digital design required, including familiarity with RISC processors, DSP designs, and designing using FPGAs/PLDs. Hands-on lab prototyping and testing, and familiarity with schematic entry and PCB layout required. BSEE required, MSEE preferred.

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Lead the design and integration of leading edge technology. Conduct field tests, develop software analyses and system simulations, guide design engineers in developing hardware and software, and debug and characterize completed systems and sub-systems. Experience in system-level design, and implementation of wireless systems required. Background in programming, RF, or digital design preferred. Strong experimental skills, C/UNIX experience, and MSEE preferred.

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RF, VLSI, Software Engineers Head Companies' Wish Lists

Linda L. Hudson

Recent interviews with staffing managers at communications companies reveal pressing needs for engineers experienced in radio frequency (RF) and analog integrated circuit (IC) design. Managers at semiconductor companies, meanwhile, continue to seek a broad range of very large integrated (VLSI) circuit design skills. Computer science/software engineers remain vital to companies in almost every industry. And there's general agreement that a master's in business administration (MBA) or an advanced degree in a specialized area like embedded microprocessor design will help keep an engineer's career moving. Finally, companies are again recruiting in earnest on college campuses, looking for the "best and brightest."

"Top-Notch" Talent Wanted

Charlotte Wells, Intel's manager of Strategic Staffing, Folsom, Calif., says "top-notch" engineering talent–in every discipline–is always in demand. She says this is especially true at Intel, which works hard to keep its edge as the world's leading supplier of semiconductors, flash memory, and computer motherboards. Wells says top talent is particularly needed on the manufacturing floor.

"Companies don't go into semiconductor manufacturing with half a heart," Wells says, pointing out that new plants can cost about $2 billion to bring on line. "The entire industry needs engineers skilled in semiconductor manufacturing in order to continue to drive down production costs."

In its Internet employment postings, two of Intel's five categories–IC engineering and IC manufacturing–had manufactured-related listings.

Software engineers also are needed throughout the semiconductor industry, Wells says. Intel, for example, needs top software talent for every product line. In December 1996 alone, Intel listed 45 software "Hot Job" categories on its web site. Wells explains that as more applications are programmed into silicon, more engineers with software specialties are needed. Intel's new supercomputer, the world's fastest, also relies on software talent. And product managers at Intel are expected to have backgrounds in software as well as hardware.

Software engineers also are key personnel in manufacturing. Wells says a new inventory control system from Germany known as SAP that's very popular in the industry requires good software engineers along with analysts and programmers. "Engineers with experience in SAP are a very sought-after group," she adds.

In general, while Intel and the rest of the industry look for engineers with a broad range of VLSI design experience, microchip design in particular, specific needs vary by product lines. For instance, Wells points out, laptop computers require low-power, high-performance components that minimize battery drain, so the people who design such components must be knowledgeable in that area. Meanwhile, motherboards and flash memory require general expertise in integrated circuit design.

And wireless technology products need both digital and analog IC designers. "The whole wireless industry–computing and communications and sometimes entertainment–also are looking for graphics engineers," Wells says.

Broad Skills Pay Off

In general, any experience with board-level electronics should pay off for an aspiring engineer. Wells says, whether it's in consumer electronics, aerospace, or defense. "Where there's a pile of engineers, she notes, "there's opportunity." Of electrical engineers (EEs) and technicians coming out of the military, she says, "some of the best background experience is in nuclear submarines" because of the quantity and variety of electronic equipment in the subs.

Engineers with backgrounds in "various types of semiconductor IC design are becoming more important because more is being put on one chip," according to Dan Rogers, director of Public Affairs in Motorola's Semiconductor Product Sector, Austin, Texas. He also notes that one key area is in the design of embedded processors. Also needed are people with "advanced degrees in specialized areas such as microprocessor and memory design for both consumer and communications products."

"Really," he says, "the market for engineers hasn't changed recently." And at Motorola, he adds, "engineering needs have not changed in the past two years. We're looking for everything across the board."

Cellular, Wireless Experience A Plus

While the standard EE degree is useful, experience in cellular and wireless technology is particularly valuable at communications companies, says Michelle Fleck, vice-president of Staffing at Qualcomm, San Diego, Calif. She says Qualcomm designs and builds equipment for both the infrastructure and the subscriber hardware (i.e., telephones) that make up a wireless, personal communications system.

Among the company's "definite needs" Fleck lists RF engineers and IC designers. "Analog IC designers are harder to find because it's a newer technology. Our best success is with new grads–MSEE's–whom we then train."

She says that software engineers are another necessity in the wireless industry, especially those with backgrounds in real-time embedded systems. "And C++ is a definite requirement for software engineers," Fleck adds.

She notes that Qualcomm is in the middle of a "huge hiring trend,"looking to hire 528 engineers during the current fiscal year in several engineering disciplines–software, digital design, RF, systems, and VLSI–and at all experience levels.

Looking For RF Engineers

In wireless or cellular communications companies, RF engineers can write their own tickets, according to Chuck Gerberich, a Lucent Technologies recruiting strategist based in Allentown, Pa.

"We can't get RF and microwave engineers fast enough," Gerberich says. "That's the reality now. And an MBA doesn't hurt in

any new area." He says Lucent and other companies want product managers to have both a technical and a business background, so it helps to have a business degree on top of a "plain old electrical engineering" degree.

He adds that VLSI design experience is "part of what you need." Digital and analog circuit design also is important.

Ultimately, engineers must be able to keep pace as technology changes and companies diversify their product lines, says Greg Likins, a college recruiter with TRW's Data Technologies Division, Redondo Beach, Calif. That division, a part of the company's Space and Defense Group, has been at the forefront of diversification, seeking to apply its expertise in defense industry databases to the civilian sector.

"Data processing has allowed us to move sideways," and apply TRW's large software developments to federal, state, and local government agencies, Likins says. As a result, engineers with computer science experience in their backgrounds are extremely valuable.

Even though his division looks primarily for software engineers, Likins says he believes the future will require more "hybrid" engineers who can move easily between chip design and software development. In the meantime, he notes, database developers need people with some kind of computer science pedigree–even if computers are only used as a hobby or as part of other college classes. "Everything these days ends up on a computer,"he points out.

Besides capable people, the defense industry also needs individual with security clearances. As a result, says Likins, "We're all vying for the same very small group of people."

This continuing difficulty has led TRW to attempt to lure back women engineers with high clearances who've left the company to have children. Likins says many of these engineers do not want full-time jobs while the children are young, so TRW is offering them part-time positions and on-site daycare facilities.

Committed To College Hires

As the economy has improved and downsizing in industries like defense has come to an end, companies have begun recruiting again at colleges and universities.

Chuck Gerberich, for instance, says Lucent Technologies is emphasizing college hires more than they have in the recent past. "Now, for every experienced hire, we're bringing in a trainee. People throughout the industry are recognizing the need to do that."

"We definitely have a commitment to hire people of out college," says Wells, because recent grads help keep the company on top of new technological developments. She says about one-third of Intel's technicians and engineers are hired right out of college.

At TRW, defense downsizing had caused his division to stop recruiting, says Likins. "It was out of the question. The whole industry was that way."

Now, TRW is back on campus in a big way with a project called the College Recruiting Program. "We're going out looking for the best and brightest," says Likins.

Linda L. Hudson is a freelance writer and editor. She may be contacted at 733A Loma Verde Ave., Palo Alto, CA 94303; (415) 424-9828; fax (415) 424-1440.

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Founded in 1992, ArrayComm currently has 85 employees, including 50 engineers. Over the next 12 months, ArrayComm plans to hire approximately 50 more engineers. Positions will be open for hardware engineers, RF engineers, software engineers, product managers, and application engineers.

Company headquarters is located at:
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QUALCOMM, Inc.

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Philips Semiconductors headquarters is located at:
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Company Profiles

Wiltron Company

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Company headquarters is located at:
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Company Profiles

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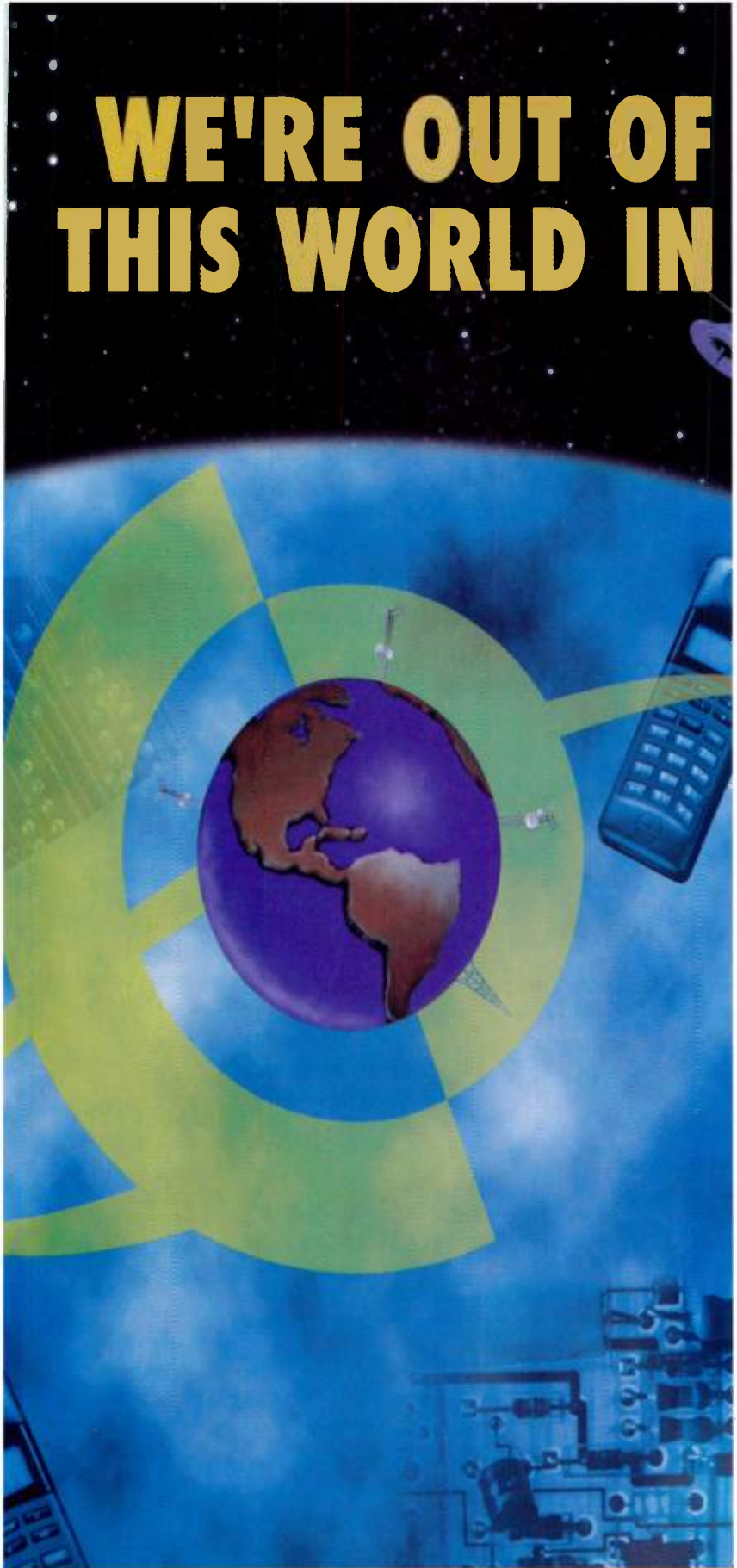

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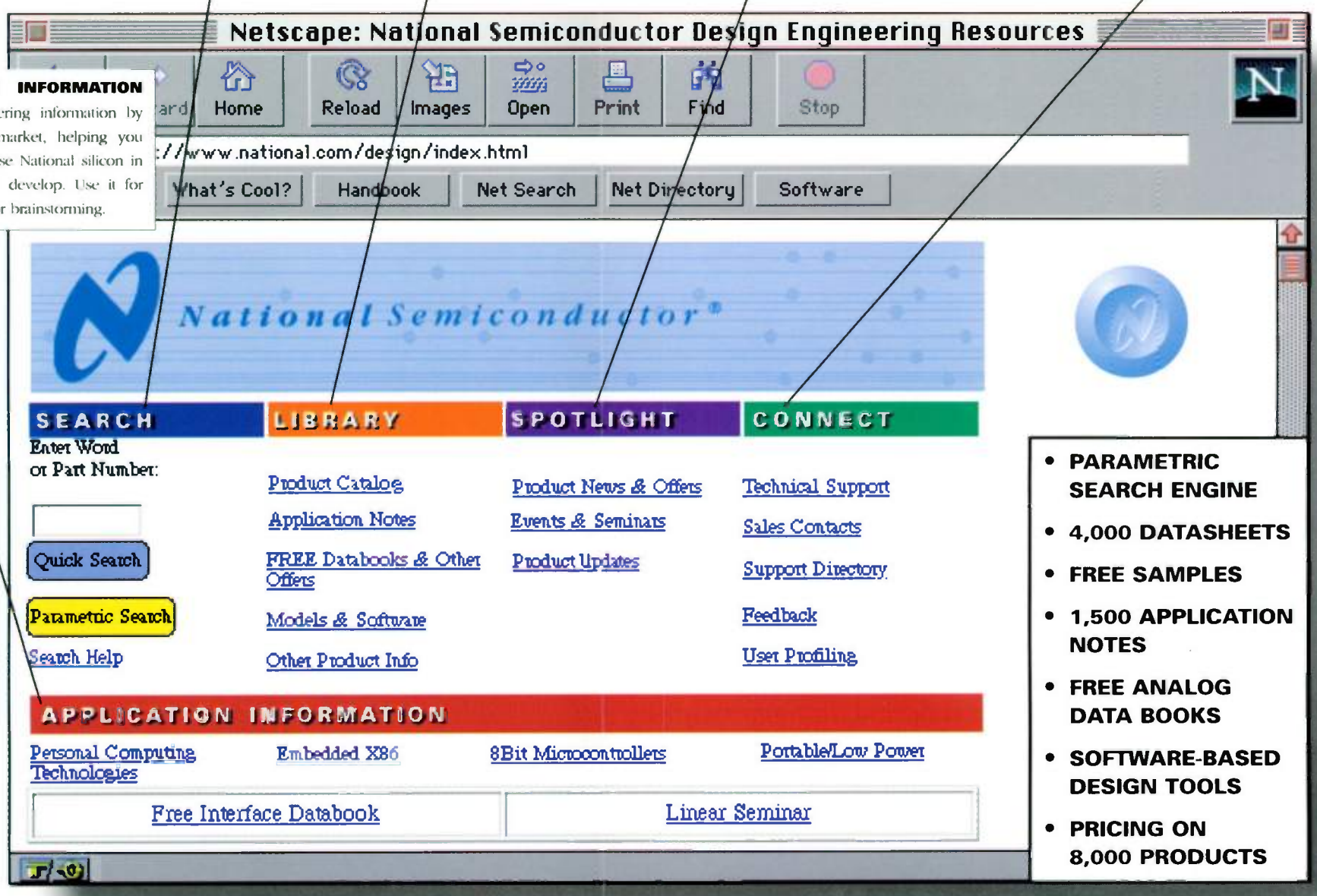

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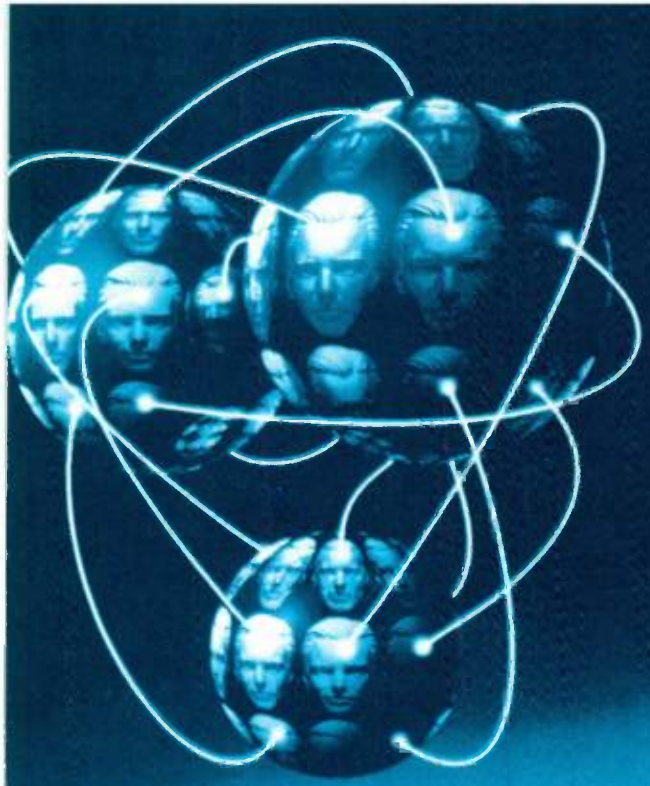

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CIRCLE 630

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The L Series power supplies are designed for benchtop and portable applications that don't require programmability. The family consists of a total of 14 models, with outputs available from 0 to 300 V at power levels from 90 to 375 W. They come in four configurations: the LS (small output), LM (medium output), LH (high output), and LT (triple output). The latter models have three independent and isolated outputs, two adjustable from 0 to 100% of voltage and current rating and one fixed at 5 V and 3 A. The supplies automatically cross over between voltage and current sourcing based only on load demand. Remote analog programming of voltage or current is available on the LS series. LED displays indicate the operating mode. Users can connect multiple supplies to increase output voltage, and the LS and LT models can be paralleled for increased current capacity. The ac input is externally selectable for 100, 120, 220, or 240 V at 50 or 60 Hz. Prices start at $335. Delivery is in six weeks.

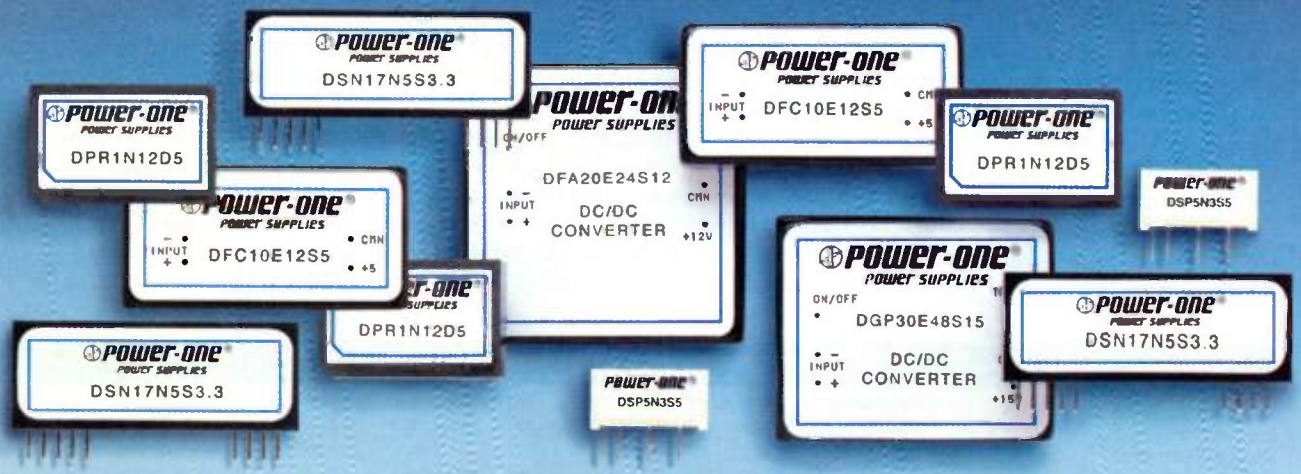
***Elgar Corp.**, Sorenson Div., 9250 Brown Deer Rd., San Diego, CA 92121; (800) 525-2024; (619) 450-0085; e-mail: sales@elgar.com*

CIRCLE 631

SPECTRUM ANALYZERS

Manufacturer	Model/Price	Resolution bandwidth	Frequency Range	Frequency Accuracy	Amplitude Range	Amplitude Accuracy	Dynamic range	Remarks
Hewlett-Packard Co. Direct Marketing Org. P.O. Box 58059 MS51L-SJ Santa Clara, CA 95051-8059 (800) 452-4844 ext. 5054	HP 71200C/ $60,150	10 Hz-3 MHz	50 kHz-22 GHz	±1 kHz (@ 10 GHz)	–109 to +30 dBm	±2 dB*	91 dB	Additional functional modules available. *0.9-dB accuracy opt.
	HP 8565E/ $64,750	1 Hz-2 MHz	30 Hz-50 GHz	±1 kHz (@ 10 GHz)	–147 to +30 dBm	±3 dB	108 dB	
	HP 71209A/ $73,950	10 Hz-3 MHz	100 Hz-26.5 GHz	±1 kHz (@ 10 GHz)	–137 to +30 dBm	±2 dB*	99 dB	Additional functional modules available; *0.9-dB accuracy, 40 GHz opt.
	HP 8566B/ $75,800	10 Hz-3 MHz	100 Hz-22 GHz	±2.5 kHz (@ 10 GHz)	–125 to +30 dBm	±2.7 dB	107 dB	Range extends to 325 GHz with external mixers
	HP 71210C/ $93,550	10 Hz-3 MHz	100 Hz-22 GHz	±1 kHz (@ 1 GHz)	–136 to +30 dBm	±2.5 dB*	98 dB	Additional functional modules available. *0.9 dB accuracy opt.
IFR Systems Inc. 10200 W. York St. Wichita, KS 67215-8935 (800) 835-2352	A-7550/$7495	300 Hz-3 MHz	10 kHz-1GHz	±25 ppm	–120 to +30 dBm	±2 dB	70 dB	Portable; built-in battery, tracking generator.
	AN920/ $15,695	300 Hz-3 MHz	9 kHz-2.9GHz	±0.2 ppm (±0.02 ppm opt.)	–135 to +30 dBm	±1 dB	80 dB*	Built-in tracking generator opt. *120 dB on-screen with two sweeps in enhanced sweep mode.
	AN930A/ $21,950	300 Hz-3 MHz	9 kHz-22 GHz	±0.2 ppm (±0.02 ppm opt.)	–135 to +30 dBm	±1 dB	80 dB	Same as AN920.
	AN940/ $27,500	300 Hz-3 MHz	9 kHz-26.5 GHz	±0.2 ppm (±0.02 ppm opt.)	–135 to +30 dBm	±1 dB	80 dB*	Same as AN920.
Marconi Instruments Inc. 2301 Horizon Dr. Fort Worth, TX 76177 (817) 224-9200	2945A/$13,500	300 Hz-3 MHz	100 kHz-1.05 GHz		–50 to +52 dBM		80 dB	Spectrum analysis function within a portable communications monitor.
	2392/$15,696	3 Hz-30 MHz	9 kHz-2.9 GHz	±5% of indicated span	–135 to +30 dBm	±0.25 dB	80 dB	DSO and FFT spectrum analyzer; am/fm demodulation; 1-Hz resolution frequency counter; extended range with external mixers. Optional applications software.
	2390/$21,950	3 Hz-30 MHz	9 kHz-22 GHz	±5% of indicated span	–135 to +30 dBm	±0.25 dB	80 dB	Same as 2392.
	2965A/$26,260	300 Hz-300 kHz	100 kHz-1.05 GHz		–100 to +70 dBm		80 dB	Spectrum analysis function within a high-performance communications monitor.
	2393/$27,500	3 Hz-30 MHz	9 kHz-26.5 GHz	±5% of indicated span	–135 to +30 dBm	±0.25 dB	80 dB	Same as 2392.

DC/DC Just Got Better.



Introducing DC/DC from the number one name in AC/DC...Power-One.

POWER-ONE DC/DC CONVERTER AVAILABLE OUTPUTS

Series	Max Watts	Vin Range	Vout 3.3V	Vout 5V	Vout 5.2V	Vout 7V	Vout 12V	Vout 14V	Vout 15V	Vout 17V
Single Output products										
DSP1	1	4.5-5.5		•		•	•	•	•	•
DFA6	6	9-27, 20-60		•	•		•		•	
DFC6	6	3.5-16		•	•		•		•	
DFC10	10	9-18, 18-36, 36-72	•	•			•		•	
DGP12	12	3.5-16		•			•		•	
DFC15	15	20-60		•			•		•	
DSN17	17	4.5-6, 6.5-15.5	•	•						
DFA20	21	9-18, 18-36, 36-72	•	•			•		•	
DGP30	30	36-72		•			•		•	
Dual Output products provide the indicated Vout as one positive and one negative output										
DSP1	1	4.5-5.5		+/-		+/-	+/-	+/-	+/-	+/-
DFC10	10	9-36, 18-72		+/-			+/-		+/-	
DGP12	12	3.5-16		+/-			+/-		+/-	
DFC15	15	20-72					+/-		+/-	
DFA20	20	9-18, 18-36, 36-72		+/-			+/-		+/-	
Triple Output products provide a main output (•) and two symetrical outputs (+/-)										
DGP20	20	9-18, 18-36, 36-72		•			+/-		+/-	

- 100% dynamic load burn-in.
- CE Marking pending.
- ISO 9000 approved quality.
- Stocked by your distributor.
- Industry standard footprints and pinouts.
- Over 100 models.

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READER SERVICE 194

ESCON Analyzer Stores 2 Gbytes Of Traces

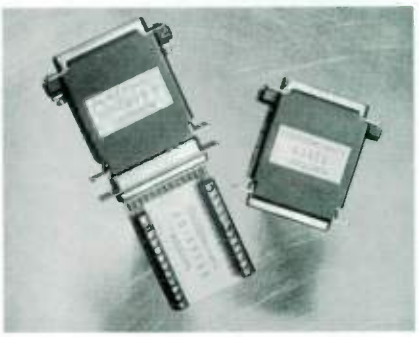
The GLA-3100, a gigabit link analyzer that unobtrusively monitors a full-duplex Enterprise System Connection (ESCON) data link, stores up to 2 Gbytes worth of traced frames for analysis. The deep memory allows the analyzer to monitor a link continuously before triggering on a predefined event and still capture the cause of the event, which may have occurred hours earlier. The system's software supplies extensive diagnostics, data capture with timestamping, and search, sort, filter, and trigger tools. Four analyzers can be controlled by one PC, which also displays the ESCON traffic patterns. Each analyzer has a removable interface board with two fiber-optic ports (in and out) to accommodate a full-duplex link. Users configure the GLA-3100 by plugging in the interface card for the desired protocol and loading the corresponding software. The ESCON interface is available now; Fibre Channel and SSA interfaces are planned. The GLA-3100 costs $36,560. The ESCON interface board costs $6800.

***Finisar Corp.**, 620B Clyde Ave., Mountain View, CA 94043-2214; (415) 691-4000; fax (415) 691-4010.*

CIRCLE 632

Data-Acquisition System Offers Range Of Inputs

The AD-612 data-acquisition system connects directly to a host computer's parallel port to offer easy interchangeability for a variety of analog and thermocouple low-speed inputs. Accessory modules include the AD-DIFF6, which provides conditioning for differential inputs from 0 to 100 mV. The AD-MSC01 is a signal-conditioning adapter that provides two thermocouple, one differential, two single-ended, and one frequency input. The AD-TSC5 converts the AD-612's six single-ended inputs to five J-, K-, or T-type thermocouples, with a CJC reference channel included. The AD-TDA3 is a hybrid of the AD-612 and AD-TSC5. It has two 0-to-4-V dc analog inputs; three J-, K-, or T-type thermocouple inputs; a CJC reference channel; and



three digital I/O channels. Included software allows operation without custom programming. The AD-612 costs $139. The AD-TDA3 goes for $199, and the other modules cost $110 each.

***Keithley MetraByte**, 440 Myles Standish Blvd., Taunton, MA 02780; (800) 348-0033; fax (508) 880-7635; e-mail: info@MetraByte.com.*

CIRCLE 633

SPECTRUM ANALYZERS

Manufacturer	Model/Price	Resolution bandwidth	Frequency Range	Frequency Accuracy	Amplitude Range	Amplitude Accuracy	Dynamic range	Remarks
Rohde & Schwarz GmbH & Co. Postfach 80 14 69 Mueldorfstrasse 15 D-81614 Munich 80 Germany (49) (89) 41290 In the U.S. and Canada: Tektronix Inc. P.O. Box 1520 Pittsfield, MA 01201 (800) 426-2200	FSEA20/ $29,995	10 Hz-10 MHz	9 kHz-3.5 GHz	1.01 kHz (@ 1 GHz)	–145 to +30 dBm	1 dB (to 1 GHz)	155 dB	Monochrome display; IEEE-488 std.; color display, high stability opt.
	FSEB20/ $34,995	10 Hz-10 MHz	9 kHz-7 GHz	1.01 kHz (@ 1 GHz)	–145 to +30 dBm	1.5 dB (1 to 7 GHz)	152 dB	Monochrome display; IEEE-488 std.; color display, high stability opt.
	FSEM20/ $41,400	10 Hz-10 MHz	9 kHz-26.5 GHz	1.01 kHz (@ 1 GHz)	–145 to +30 dBm	2 dB (1 to 18 GHz)	150 dB	Monochrome display; IEEE-488 std.; color display, high stability opt.
	FSEA30/ $45,575	1 Hz-10 MHz	20 Hz-3.5 GHz	11 Hz (@ 1 GHz)	–155 to +30 dBm	1 dB (to 1 GHz)	165 dB	Color display; IEEE-488 std.
	FSEB30/ $49,995	1 Hz-10 MHz	20 Hz-7 GHz	11 Hz (@ 1 GHz)	–155 to +30 dBm	1.5 dB (1 to 7 GHz)	162 dB	Color display; IEEE-488 std.
	FSEM30/ $55,00	1 Hz-10 MHz	20 Hz-26.5 GHz	11 Hz (@ 1 GHz)	–155 to +30 dBm	2 dB (1 to 18 GHz)	160 dB	Color display; IEEE-488 std.
Stanford Research Systems Inc. 1290-D Reamwood Ave. Sunnyvale, CA 94089 (408) 744-9040	SR760/$4750	476 µHz-100 kHz	476 µHz-100 kHz	0.0025%	–60 to +34 dBV	±0.2 dB	90 dB	Automated analysis functions; 3.5-in. floppy drive.
	SR770/$6500	476 µHz-100 kHz	476 µHz-100 kHz	0.0025%	–60 to +34 dBV	±0.2 dB	90 dB	Same as SR760, plus signal source.
	SR780/$9950	476 mHz-100 kHz	476 mHz-100 kHz	25 ppm	–50 to +34 dBV	±0.2 dB	90 dB	Two-channel network analyzer plus source.
Tektronix Inc. P.O. Box 1520 Pittsfield, MA 01201 (800) 426-2200	2711/$9350	3 kHz-5 MHz	9 kHz-1.8 GHz	±15 kHz (@ 1 GHz)	–129 to +30 dBm	±1.5 dB	80 dB	Built-in am/fm demodulator; pre-amplifier.
	2712/$12,750	300 Hz-5 MHz	9 kHz-1.8 GHz	±510 Hz (@ 1 GHz)	–139 to +30 dBm	±1.5 dB	80 dB	Built-in am/fm demodulator; pre-amplifier; IEEE-488 std.
	2714/$13,950	300 Hz-5 MHz	9 kHz-1.8 GHz	±510 Hz (@ 1 GHz)	–92 to +30 dBm	±1.5 dB	80 dB	Built-in am/fm demodulator; pre-amplifier.
	2715/$15,900	300 Hz-5 MHz	9 kHz-1.8 GHz	±510 Hz (@ 1 GHz)	–92 to +30 dBm	±1.5 dB	80 dB	Has advanced in-service testing features, digital RF measurements.
Wandel & Goltermann 1030 Swabia Ct. Research Triangle Park, NC 27709-3585 (919) 941-5730	SNA-23/ $43,870	1 Hz-10 MHz	100 Hz-26.5 GHz	$\pm 5 \times 10^{-10}$/ day	–125 to +30 dBm	±0.5 dB	155 dB	IEEE-488 std.
	SNA-33/ $50,825	1 Hz-10 MHz	20 Hz-26.5 GHz	$\pm 5 \times 10^{-10}$/ day	–125 to +30 dBm	±0.5 dB	153 dB	IEEE-488 std.

SAM-350 7-GFLOPS REAL-TIME DSP

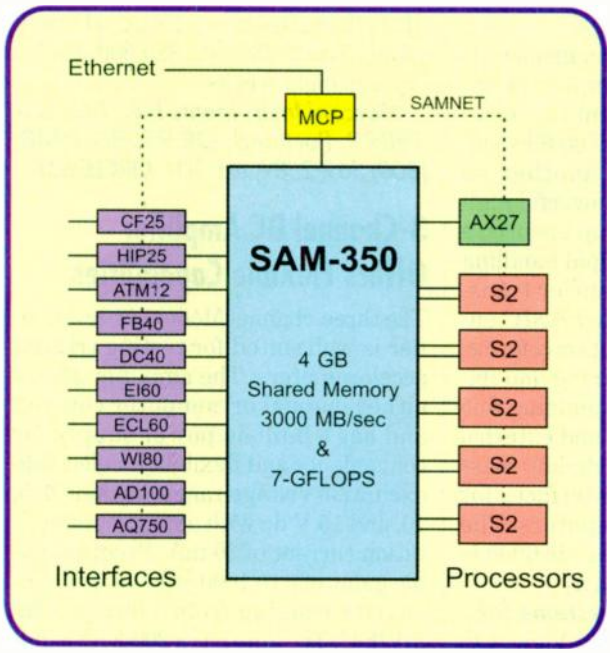
1K CFFT — 11 µsec 64K CFFT — 850 µsec 1M CFFT — 30 msec

High GFLOPS DSP

- 7-GFLOPS (5 Vector Processors)
- 550 MIPS Scalar Processor
- High Level Programming
- Scientific Math Library
- Real-Time Manager

High Bandwidth Memory

- 4-GB Shared Memory
- 3000 MB/sec Bandwidth
- 300 MB/sec per I/O Port
- 10 I/O Ports



High GFLOPS DSP --- The **SAM-350 (Shared Access Memory)** is the ideal real-time DSP system optimized for **FFT, convolution, correlation, and matrix multiplication applications**. It has multiple fast I/O ports, fast memory, fast processing, and a real-time executive. It is easy to program in a high level language **(C or FORTRAN)** and only needs a few vector processing nodes to run at 7 GFLOPS. Data sets are easy to manage in a large shared access memory instead of a distributed memory system. User applications execute as low-overhead single-thread programs on the **AX27 scalar processor (Alpha chip)**. Compute-intensive DSP functions are executed as subroutine calls to one or more **S2 vector processor** nodes. Our extensive S2 scientific math library includes over 100 DSP, vector and matrix arithmetic functions.

Real-Time Manager --- Coordinating all the I/O and DSP resources within the SAM-350 is the responsibility of the master control processor (MCP). The MCP is an embedded processor which runs a **multitasking real-time executive** under control of the application program. It schedules and synchronizes all tasks to ensure **responsive, event-driven, real-time programming**.

High Bandwidth Memory --- The shared memory of a SAM-350 system can be accessed simultaneously by as many as **10 fast I/O devices, five S2 vector processors, and an AX27 scalar processor**. Each of the ten I/O ports has dedicated FIFOs to keep data flowing seamlessly into or out of SAM memory at a sustained rate of 300 MB/sec. per port. The maximum aggregate I/O port bandwidth is 1500 MB/sec. Another 1500 MB/sec memory bus is available for the S2 vector processors. The total **3000 MB/sec bandwidth** to a single 4 Gigabyte shared memory allows fast input, fast DSP, and fast output for continuous, multi-channel processing with minimal latency.

Texas Memory Systems, Inc.
11200 Westheimer #1000
Houston, Texas 77042

(713) 266-3200
Fax: (713) 266-0332
www.texmemsys.com

GFLOPS for the Masses

READER SERVICE 183

Compact Supply Outputs 30 V DC At Up To 5 A

A compact, single-output dc power supply covers an output range from 0 to 30 V at currents up to 5 A. The Model 3005 features a special energy-saver circuit designed for cooler, more efficient operation. Two three-digit LED readouts allow users to simultaneously monitor voltage and current. The supply also has an overload indicator. The unit provides excellent line and load regulation, as well as noise and ripple specifications. It comes with three, five-way binding posts, coarse and fine voltage controls, and a set of cables. The Model 3005 costs $389.

HC Protek Inc., *154 Veterans Dr., Northvale, NJ 07647; (201) 767-7242; fax (201) 767-7343.*

CIRCLE 634

Distributed Emulation System Supports SH7040

Support for the Hitachi SH7040 series of microprocessors is now available as part of the HP E3472A distributed-emulation solution. Distributed emulation is a modular toolset that includes a processor probe, preprocessor, C debugger, and logic analyzer for a complete system debug environment. The processor probe controls the target by executing run control, providing memory substitution, setting breakpoints, and displaying memory contents. The preprocessor provides the interface between the target and the reset of the emulation system. The C debugger runs on Windows 95 PCs, HP 9000 series 700 workstations, and Sun SPARC workstations. The logic analyzer supplies real-time trace analysis and measurement of timing waveforms. The C debugger interface controls the analyzer, so the user needn't understand its complex trigger features. Users who don't need real-time trace can omit the logic analyzer. The HP E3472A SH7040 processor probe, preprocessor, and C debugger cost $10,800. Flexible 112- and 144-pin cables are $1400 each. Logic analyzers are priced separately.

Hewlett-Packard Co., *Test and Measurement Org., P.O. Box 50637, Palo Alto, CA 94303-9512; (800) 452-4844 ext. 2269.* **CIRCLE 635**

200-MHz DSO Features Variable-Intensity Display

The Classic 6000 is a four-channel, digital storage oscilloscope with a 200-MHz bandwidth and 100-Msample/s digitizing rate. The scope offers a color display, mass storage, and automatic sequencing and math functions. An architecture with PC-like expansion slots allows for easy upgrades with additional functions. A patented new feature called TruTrace generates a variable-intensity display similar to that produced by an analog real-time scope. With TruTrace, users can see fine details that usually would be lost with standard DSO display methods. The technique is particularly useful for viewing complex transients and signals in the presence of noise.

The Classic 6000 can display eight traces at once, so users can compare signals on each of the four channels with reference traces or zoomed versions. For easier viewing, channel annotations and ground markers are color-matched to the traces.

The standard waveform memory is 50 ksamples (200 ksamples is optional). Users can segment the memory, and the segments will be filled automatically one after another on successive triggers. A powerful digital-signal-processing chip ensures a quick update rate and rapid handling of functions like fast Fourier transforms. Also, a new display ASIC enhances the presentation of waveforms, providing better dot joining and improved resolution for examining fine details. Various internal and external options are available, including mass storage, plotters, and interfaces for links to printers or computers. The starting price of the Classic 6000 is $6195. Delivery is in 20 days.

Gould Instrument Systems Inc., *8333 Rickside Rd., Valley View, OH 44125-6100; (216) 328-7000; fax (216) 328-7400.* **CIRCLE 636**

Single Box Combines Three Independent 2.4-GHz Sources

The 2026 multi-source generator combines up to three independent RF sources in one instrument, with separate or combined outputs. The synthesized generator includes a series of predefined application-specific test setups. The frequency and level of internal RF sources can be coupled with a user-defined offset, enabling sources to track each other. A calibrated output guarantees excellent level accuracy, with exceptional intermodulation and isolation performance for all types of receiver, submodule, and component testing. Each source covers 10 kHz to 2.4 GHz, with sweep capability included. Modulation capabilities include am, fm, phase, pulse, and 2/4-level FSK. The unit has an internal modulation source, but an external input, either ac- or dc-coupled, can be used. Individual output levels are +24 dBm. The 2026 fits a 19-in., 4U rack space. The 2026 costs $20,000. Delivery is in eight weeks.

Marconi Instruments Inc., *P.O. Box 19899, Portland, OR 97280-9948; (800) 369-2589, ext. 101.* **CIRCLE 637**

3-Channel DC Amplifier Offers Flexible Capabilities

The three-channel Model 136 dc amplifier is well suited for testing triaxial accelerometers. The amplifier allows either manual or computer control, and has a built-in power supply for convenience and flexibility. Selectable excitation voltage ranges include 0, 5, 10, and 15 V dc with a maximum excitation current of 30 mA. Programmable gains of 0 to 1000 offer sensor sensitivity ranging from 0.001 to 9999 mV/EU. The amp has a 200-kHz bandwidth (–3-dB corner) and a built-in four-pole Butterworth low-pass filter. Computer control is through the standard RS-232 port and optional Windows-compatible applications software. Two versions are available. One runs on 90 to 264 V, 50 to 60 Hz ac, the other on 9 to 18 V dc. Call for prices.

Endevco Corp., *30700 Rancho Viejo Rd., San Juan Capistrano, CA 92675; (800) 982-6732; (714) 493-8181; fax (714) 661-7231.* **CIRCLE 638**

For today's problems that need to be solved yesterday.

The world's most powerful handheld scope.

When equipment goes down you need to fix it in a hurry, or get used to people looking over your shoulder. Fortunately, the 200 MHz THS730A handheld scope has the power to help you quickly solve the most complex design and troubleshooting problems. Its IsolatedChannel™ architecture lets you make floating measurements safely. It's the only handheld scope to offer 1 GS/s sampling rate on all channels. And it has advanced triggers for delay, pulse and video. For more information, call your Tektronix distributor today or call 1-800-479-4490, action code 727, or visit us at www.tek.com

Tektronix

Tool Allows Design Verification On Target Microprocessor

Using the VSP/TAP co-verification tool, developers can verify their designs using the actual target microprocessor, operating system, and firmware interacting with simulated hardware. As a result, hardware and software verification can be done early in the design cycle, when errors can be detected and fixed faster and less expensively than at the physical prototype stage. By using the actual processor instead of a model, VSP/TAP eliminates the need to modify code. Also, the technique processes 1000 to 5000 instructions per second, compared to a simulated processor's one or two instructions per second.

VSP/TAP introduces a unique hardware-software interface that allows any Applied Microsystems emulator (with the target processor) to connect to any hardware simulator through Eaglei. Eaglei is a virtual system integration platform from Eagle Design Automation Inc., Beaverton, Ore.

Eaglei links the hardware-simulation environment to the software development environment. It acts as the control panel for VSP/TAP and the hardware simulator. As the code executes in application memory, VSP/TAP puts the microprocessor on hold and sends the information to Eaglei, which interprets the information and sends it to the hardware simulator. The hardware simulator reacts to the access, sending results back to Eaglei. VSP/TAP presents the bus information to the application software and releases the microprocessor.

VSP/TAP prices start at $15,000. Delivery is in eight weeks. CodeTAP system prices start at $7900, and Eaglei prices start at $40,000.

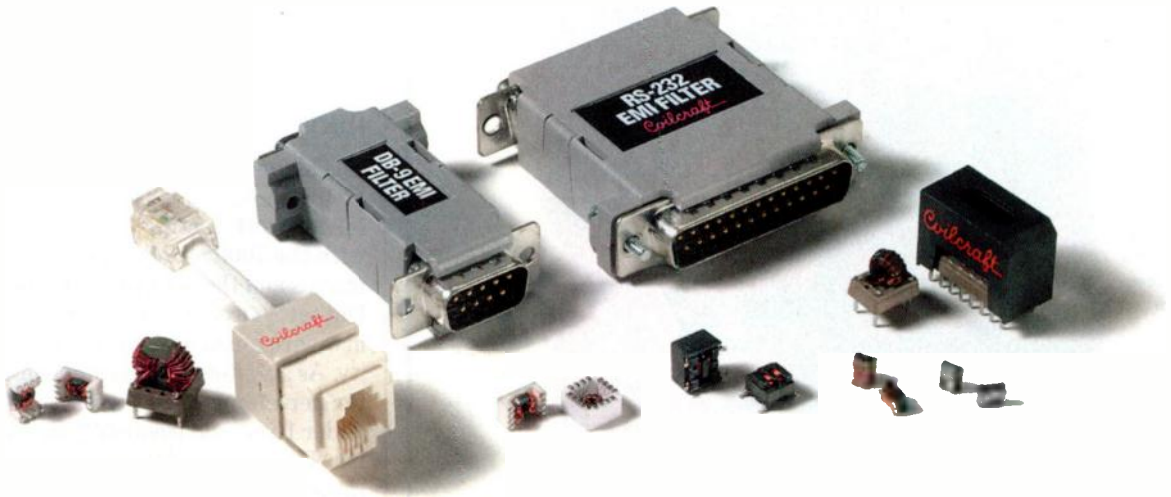
Applied Microsystems Corp., *P.O. Box 97002; Redmond, WA 97073-9702; (206) 882-2000; info@amc. com; http://www.amc.com.* **CIRCLE 639**

Frequency Counters Offer Fast Readings Down To 0.1 Hz

A pair of frequency counters extend high-resolution readings down to 0.1 Hz. The LF 826 covers 0.1 Hz to 550 MHz, and the LF 827 ranges from 0.1 Hz to 1.3 GHz. Time-base accuracy is ±3 ppm. The counters also feature RPM and totalizer functions, deviation readings from a preset reference, and Lo/Go/Hi indicators that work off preset references. Both units use reciprocal counting below 10 MHz to ensure fast, high-resolution readings. They employ direct counting from 10 to 100 MHz (input A) and the prescalar method above 80 MHz (input B). Sensitivity is 15 mV and 10 mV for inputs A and B, respectively. An auto-trigger mode optimizes the trigger level to minimize the effects of noise and hysteresis errors. A switchable low-pass filter removes RF to protect triggering on low-frequency signals. The LF 826 costs $495, and the LF 827 is $995. Delivery is from stock.

Leader Instruments Corp., *380 Oser Ave., Hauppauge, NY 11788; (800) 645-5104; (516) 231-6900; fax (516) 231-5295.* **CIRCLE 640**

Bye Bye EMI



Add one of these low cost, high performance filters and you can kiss your conducted EMI goodbye!

All Coilcraft filters use a single magnetic structure to filter multiple lines. Which makes them the fastest, most effective way to eliminate common mode noise in your circuits.

They deliver >20 dB noise reduction from 30 to 300 MHz. Or add a capacitor to increase attenuation to 40 dB or more. And unlike simple ferrite beads, you achieve this EMI attenuation without any affect on your signal.

Try them out by ordering our $60 Designer's Kit D103 with samples of many of the filters shown.

Or for complete specifications, visit our Web site at www.coilcraft.com, use our Data-by-Fax system, or call us at **800/322-2645** for a free brochure.

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READER SERVICE 106

Networked JTAG Controller Links PCs And Units Under Test

The Net-1149.1 boundary-scan controller provides an intelligent interface, using a memory-behind-the-pin architecture, between any IEEE-1149.1-compatible (JTAG) unit under test (UUT) and any PC or workstation that supports the TCP/IP protocol over Ethernet. The unit offers four independent test access ports with programmable clock rates to 35 MHz and includes 16 general-purpose I/O lines, which are individually controlled, for remote control and sense. The Net-1149.1 serializes to each of the port's boundary-scan instructions and test vectors after they've been loaded by the host computer over the network. Responses from the UUT are stored in 4 Mbytes (expandable to 16 Mbytes) of on-board RAM. Users can add a programmable delay between the active test clock edge and the sampling of the UUT's test-data-out line to compensate for propagation delay caused by long test cables between the Net-1149.1 and the UUT. The Net-1149.1 costs $5950 and is available from stock.

Corelis Inc., *12607 Hidden Creek Way, Suite H, Cerritos, CA 90703; (310) 926-6727; fax (310) 404-6196; e-mail: sales@corelis.com; www.corelis.com.*

CIRCLE 641

Matrix Switch Card Creates Automated Resistor Tester

The Model 7019-C 6-wire ohms-matrix card is designed for automated resistor-network testing. The card works with the 7000 Series switching mainframes and the company's Model 2400 Digital SourceMeter, which has built-in 6-wire ohms measurement capability. As a system, these components offer per-element test times typically under 10 ms and frequently as low as 5 ms. The card's unique switch configuration includes two independent 3-by-6 matrices. One is designed for switching the Model 2400's Force+, Force–, and Guard signals, while the other switches its Sense+, Sense–, and Guard Sense terminals. This capability eliminates the effects of shunt resistance when measuring dual-terminator resistor networks, attenuators, and hybrid circuits, thereby increasing measurement accuracy and throughput. This configuration also allows split Kelvin connections for the buried-node measurements often needed in R/2R ladder networks. The Model 7019-C costs $1195. Delivery is from stock.

Keithley Instruments Inc., *28775 Aurora Rd., Cleveland, OH 44139-1891; (800) 552-1115; (216) 248-0400; fax (216) 248-6168; e-mail: product_info@keithley.com; http://www.keithley.com.*

CIRCLE 642

FOR THE DISCRIMINATING PALATE

A Variety of New Solid State Relays

As the technology leader in solid state relays, Teledyne Relays continues to add new SSR varieties to serve its expanding customer base. We now offer one of the industry's broadest lines of solid state relays from SIPs and Mini-DIPs to Hockey Puck packages. You can look to us for all your commercial and industrial SSR applications involving AC, DC, or Bi-Directional switching, from milliamps to 1000 amps, and from millivolts to 1600 V.

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Software Tools Move Toward Automating Process Management

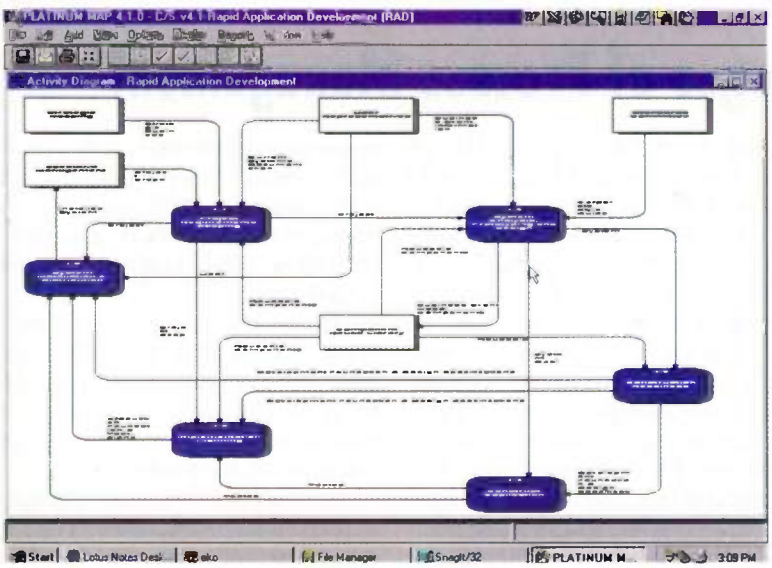
Version Control And Configuration Management Are Vital To Achieving An Orderly Software Development.

Tom Williams

SPECIAL REPORT

The days of the lone programmer are long gone. Software developers now work in teams, often in large, geographically-scattered organizations. The code they produce is ever larger and more complex than ever before—some of the latest models of cellular phones, for example, contain over one million lines of embedded C code. Moreover, today's products are often differentiated and upgraded not by changing hardware, but by changing software.

This rapid growth in the importance of software has created a demand for some form of automation to help keep track such issues as who is working on what, what each person's stage of progress is, which modules each person is responsible for, and what stage of testing each module has reached. And, since software can be deployed in different configurations, each type of product's configuration needs to be managed. Another important reason to have well-defined process automation is that people change jobs. When a new person takes over, it is much easier to have a defined process in place so he or she can pick up where the previous person left off.



Art Courtesy: Platinum Technology

CHANGE MANAGEMENT

A new breed of software-development-management tools is helping developers combine version control with change management, as well as more people-oriented issues, such as organizational structure and interpersonal communications. Taken together, these capabilities are aiding companies in true process-based development management—version control, configuration management, and change management, as well as definitions of human activity that can be analyzed, improved, and made repeatable.

Most organizations start with change management to track requests for changes and follow up on their implementation. They quickly move to version and configuration control to keep track of the changes they have made. From there, the companies try to put organizational models in place to help them understand and control the way work is done.

Change management has two elements: the information about the change (what to change), and the actions taken to make the change. Even this simple model implies some elements of process because once a change is requested and approved (a process involving management), responsibility for making the change is assigned to a programmer who is expected to carry it out.

A basic part of the process is the workflow involved in moving change requests through a series of steps to final approval and release. Com-

mercial software vendors have developed several aids for managing these steps. For example, in the workflow model used in Continuus/CM, a software package from Continuus Software *(see the accompanying listing for locations of all vendors mentioned in this report)*, people can take on various roles such as programmer and build manager. Then they are given access to files based on their roles. The system has an automatic e-mail capability that sends notification of completed actions to everyone affected by those actions. For example, when a programmer completes a change and checks the file back in, the system notifies the test manager who can promote the file to test stage. After successful testing, the system may notify the build manager that that module is ready for the next system build.

Use of these tools is not limited to the software developers within an organization. Most change-management tools interface with other parts of an organization, such as the help desk, marketing, or the internal development team itself. Requests for changes may come from almost anywhere within an organization. CCC/Harvest, from Platinum Software, uses a software trouble report (STR) to initiate and track changes *(see Fig. 1)*. The development team has a set of steps it takes to receive, review, and approve a change request, and then assign it to a programmer. CCC/Harvest, like other change-management systems, has a system for controlling who may or may not check out a file for revision.

Often, if one programmer is working on a file, others may read the file, but not work on it at the same time as someone else. The Continuus/CM system does let two programmers check out the same file and work on it simultaneously. Usually, they will be working on different parts of the code, but all their changes must be reconciled and merged into the final version of the file. In cases where there is no overlap, the system can do an automatic merge when the last person checks the file back in. In cases where both programmers have modified the same parts of the code, the system will notify that there is a conflict. That notification means that a manual reconciliation is necessary.

File-based change management is useful, but there can be a discontinuity between what is perceived as a portion of code that needs to be changed, and the files in which it resides. In other words, a functional change may involve more than one file. Continuus and Pure Atria Software are adapting the concept of change sets. Related modules of code involved in a change request may be spread over several files. Change sets group all files containing such related modules under one change set name. The programmer can then think in terms of the code and the task at hand, rather than the association of the files with the task.

Pure Atria implements change management in several parts. Its ClearCase product focuses on version control and simultaneous use of file objects. Up to 32 users can work on the same file, and ClearCase

The Five Stages of Process Management

The Software Engineering Institute (SEI) at Carnegie-Mellon University has developed a model to characterize the development stages that lead to a continually optimizing process. Called the capability maturity model (CMM), it has five stages: initial, repeatable, defined, managed, and optimizing.

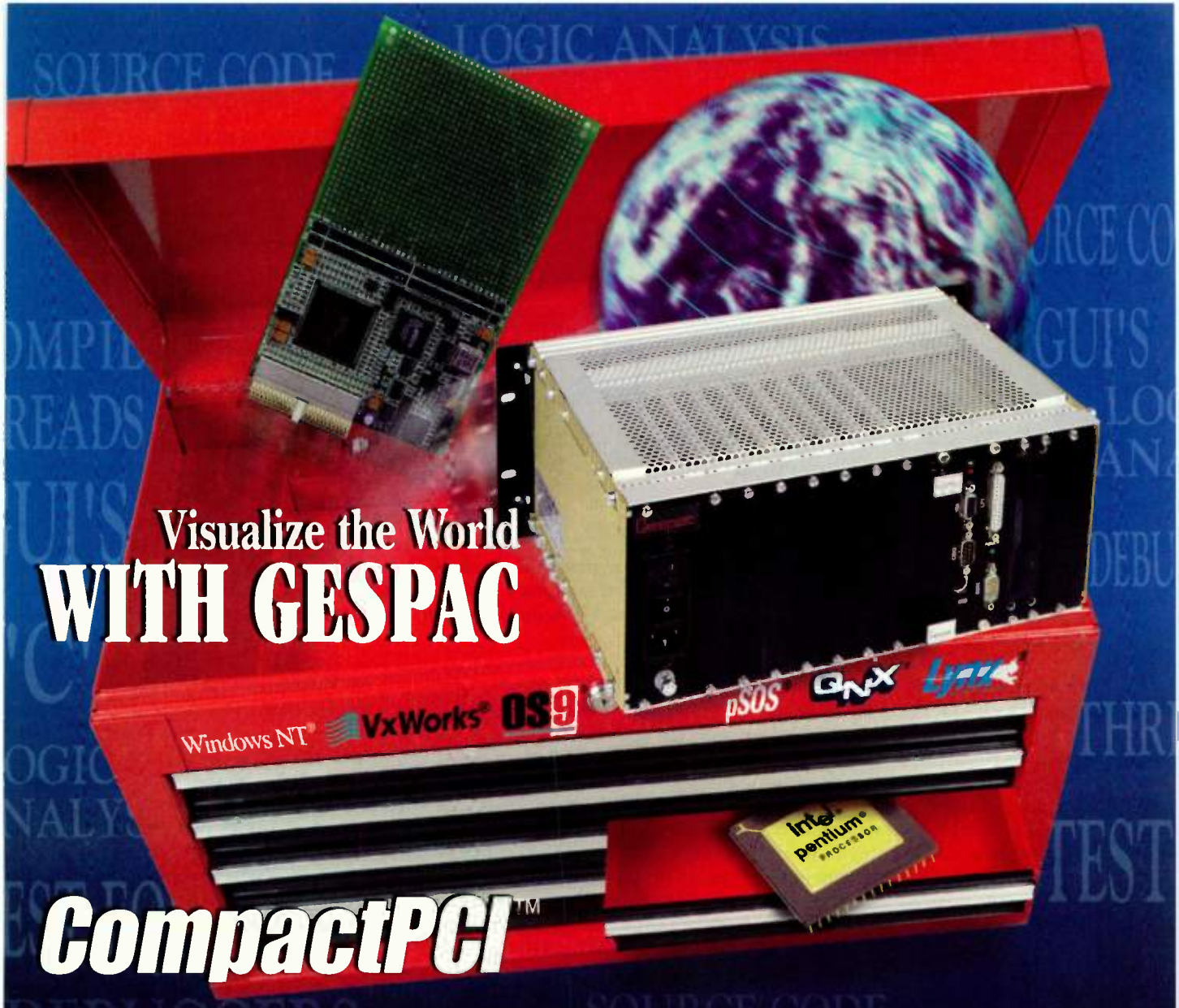
The initial stage is characterized as chaotic or ad hoc. There are no sound management practices in place, which makes it impossible for executives in the organization to predict cost, schedule, and quality. The organization's activity is primarily reactive— and may be crisis-driven, in many cases. This arrangement has programmers coding and testing, and trying to fit all the pieces together. The only hope here is a strong manager who can pull things together and communicate some sense of direction to members of the staff. However, without established procedures, any stability contributed by the manager evaporates when he or she leaves. According to data collected by SEI in mid-1996, some 68% of software development organizations were at the initial level.

The second level, the repeatable level, is characterized as disciplined. The organization is beginning to settle down andpeople are not constantly reacting to and dealing with crises. The organization has instituted basic project management, requirements management, configuration management, and software quality assurance. Managers are able to track cost and schedules, and can at least identify problems meeting commitments. There is some ability to plan new projects based on the experience and knowledge gained from executing previous projects.

At the defined level, the process is characterized as consistent. At this point, new technology such as management tools can be introduced to further improve the process. The implementation of management tools can only be effective once the organization is no longer in chaos or a crisis mode.

The fourth level is the managed level, which is characterized as predictable. The organization now has a quantitatively-measured process. A prerequisite to measuring this process is that it has to be defined.

The fifth level is the optimizing level, characterized as continuously improving. This point is the highest level of maturity that it is possible for the software development process to achieve. When the organization reaches level five, the process has become self-optimizing because it is now able to take the information from process measurements and feed it back into a well-understood and repeatable process. The prerequisite for reaching the level five stage is to have reliable process measurements in place.



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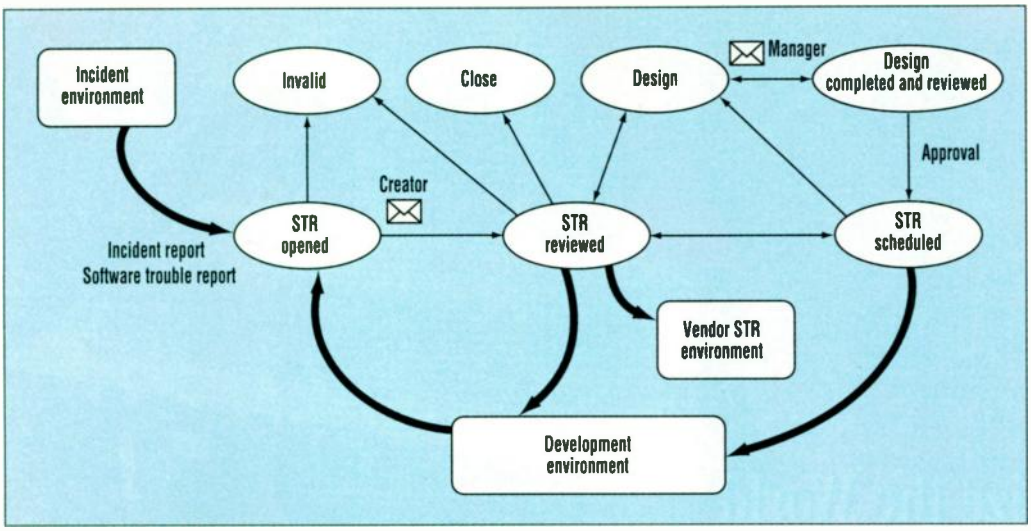


1. A SOFTWARE TROUBLE REPORT (STR) can originate as an incident from various sources such as a customer request for a change, or a bug discovered in the internal development environment. The Platinum Software CCC/Harvest environment shows an example of the procedure of such an incident from report through review,the action taken to implement the change, and approval.

keeps track of the different versions, automatically merging the objects. As with Continuus/CM, conflicts have to be resolved manually, using a set of editable windows where the user can compare multiple text files and make merge decisions that are synchronized and displayed in one window. File change management—done in some form by all CM tools—involves keeping track of multiple programmers working in parallel on multiple releases of the same project along with patches to existing releases *(see Fig. 2)*. Other products inthat fall in this category include MKS Source Integrity by Mortice Kern Systems and Visual SourceSafe from Microsoft.

Full change management comes with Pure Atria's ClearTrack, a change-request manager. When a request for a change is received, a programmer may check out an object and that check-out is monitored by ClearCase. ClearTrack assigns attributes that describe the status of the object in terms of rules that have been defined to govern the transition of that object from one status to another. Attributes may be, for example, "duplicate," "passed test," or "resolved." They reflect the status of the object in the development sequence. The rules that define the flow of objects through the development cycle represent a simple form of defining a process—the way work is done.

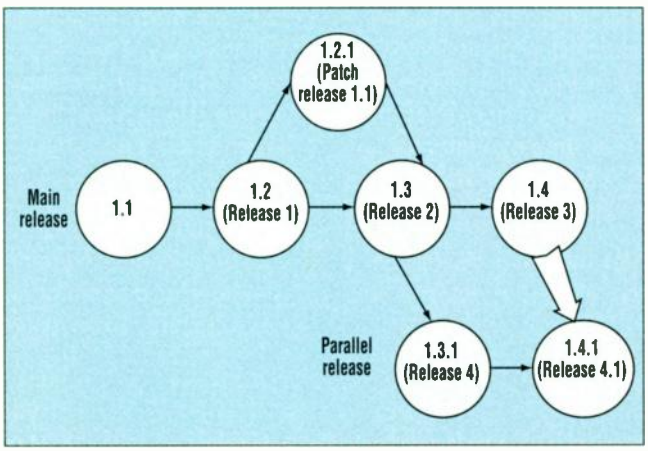
The PVCS suite of management tools from Intersolv consists of tools that can be used individually for tasks such as version control, configuration management, and problem and change request tracking.The tools also can be hooked together and interfaced with other applications to give management better control of the team effort. PVCS Version Manager provides check-out and check-in management of files with a drag-and-drop GUI.

The same GUI gives users an overview of the files that have been changed, are available to work with, and have been locked. PVCS Version Manager also lets developers visually access the archive for an overview of the entire development history of a software project. The version manager can work with PVCS Configuration Builder which manages, builds, and also maintains an audit trail of all configurations based on the different versions of a project's files.

The PVCS suite uses a mechanism of event triggers to manage the development process. For example, a manager can define a process that automatically creates a version label on a file when it is promoted to a certain level. Promotion to a certain level may launch test routines or, using the PVCS Notify tool, alert team members of who has checked out a file and for what task. On check-in, Notify can inform users on the system of the updated status of the file.

To coordinate the functions of the PVCS tools, PVCS Developer's Toolkit provides an API for integrating with existing applications, especially integrated development environments (IDEs) such as the C++ environments from Microsoft, Borland International, and Symantec. These IDEs include editors, class browsers, debuggers, and performance analysis tools. From the IDE's GUI, users can not only develop and debug their code, but also have access to the process management tools associated with the project at hand.

Adding process-based management tools to an organization that already recognizes the value of version control and change management can move that organization toward a continually optimizing and improving-



2. VERSION CONTROL KEEPS TRACK of files and the associated releases of a software. In this simple example, a patch release that was created to fix a bug can be archived, and the fix later incorporated into the next release that may have other changes. Parallel releases can be merged to create a later main release.

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process. The stages that lead to that goal have been characterized by the Software Engineering Institute at Carnegie-Mellon University in what it calls the capability maturity model (CMM). The CMM has five stages: initial or chaotic, repeatable, defined, managed, and optimizing or continuously improving *(See "The Five Stages of Process Management," p.142).*

However, no organization can reasonably take itself from chaotic to continuously improving by buying some software tools and forcing everyone to use them. For that reason, companies offering a path to full process management generally provide sets of tools that let developers get their operations under control in stages. SQL Software, for example, supplies a suite of tools called PCMS Dimensions. The tools can be accessed by managers by way of a process management user interface that gives an overview of the data produced by all the tools.

The PCMS Dimensions tools are respectively PCMS Version, Change, Personal Ada, Archive, Integration, Network, Helpbench, and HomeRun. PCMS HomeRun is the project planning and management tool that gives managers a dynamic view of the process. Each of the other tools has a built-in process engine that covers its particular set of functions, such as change management or version control.

PROCESS MODELS RULE

The process engines in each module are configured for a certain type of workflow within the overall organizational development process. For example, management can define roles and responsibilities of individual team members as well as the manner in which interteractions will take place. Rules can be set up to model and manage the states of software components and the translations between states and their status(e.g., checked out, tested, and approved for deployment). The process definitions within each tool are then coordinatedand deployed into an overall process model that can be reviewed and handled at the managerial level.

In addition to its CCC/Harvest tool, Platinum Software has a process management tool called Platinum Process Continuum. Process Continuum works with other Platinum tools including CCC/Harvest and an object-oriented analysis tool called Paradigm. These and other tools, such as an automated software distribution tool and a help desk tool, can be launched directly from Process Continuum. Process Continuum oversees an organization's entire operation in terms of users' activities and the manner in which the tools are used.

Process models are called routes. Routes describe the series of tasks required to produce software deliverables. They cover not only the coding, debugging, and testing activities, but also point to key management decision factors such as planning, cost estimation, allocation of personnel, and tracking the progress of a project. Routes also define the interdependencies between project phases, contain estimates of the experience of team members, and specify roles and responsibilities.

The tool comes with a portfolio of predefined project types. Routes are available for client/server development, mainframe-centric development, software reengineering, and change management. The tool can be used to customize existing route templates or to designproject routes from scratch. Once such routes are in place, team members can access them based on their particular roles and needs within the process.. Any team member can access them to reference project guidelines or view a summary of deliverables. Progress can be tracked using a variety of built-in data displays including calendars, Gantt charts, spreadsheets, and resource histograms.

As projects increase in size and complexity, developers will push the trend toward integrating point-management tools such as version and configuration management, with other parts of the development process including requirements analyses and CASE tools. The road to a fully operational and continually-improving software development process must be takencarefully and in stages, and involves a learning curve for an organization. But the long-term benefits of the ability reuse code, produce that code, and learn and improve in the process will be well worth the effort.

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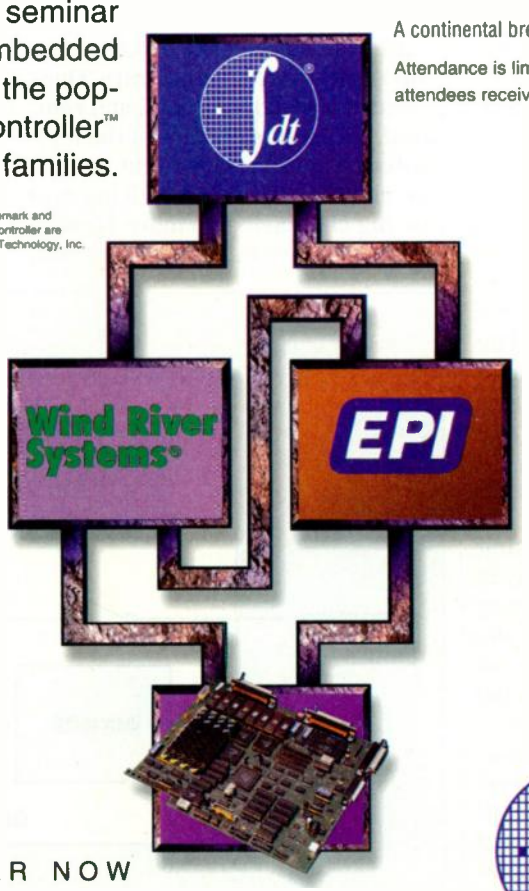

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Flash memories, with their nonvolatility, low power, and inherent solid-state ruggedness, are ideal for portable battery-powered embedded systems. In the past eight years, flash memory usage has grown from zero to a $2.5-billion market. However, the lack of standardization between silicon vendors on such aspects as architectural implementation, software algorithms, and product line upgrade paths has heightened the challenge of implementing flash software in embedded systems

The days of pure bulk-storage EPROM usage, where the CPU dumped the code into RAM and executed from there, are over. Today's designs demand fault-tolerant, on-line code updates, and that requires fault-tolerant data storage that can be updated over the air. Given these requirements, it often becomes the responsibility of the software team to make up for any last-minute changes on the project, and overcome any unexpected, undocumented hardware features (bugs) that crop up just before going into production.

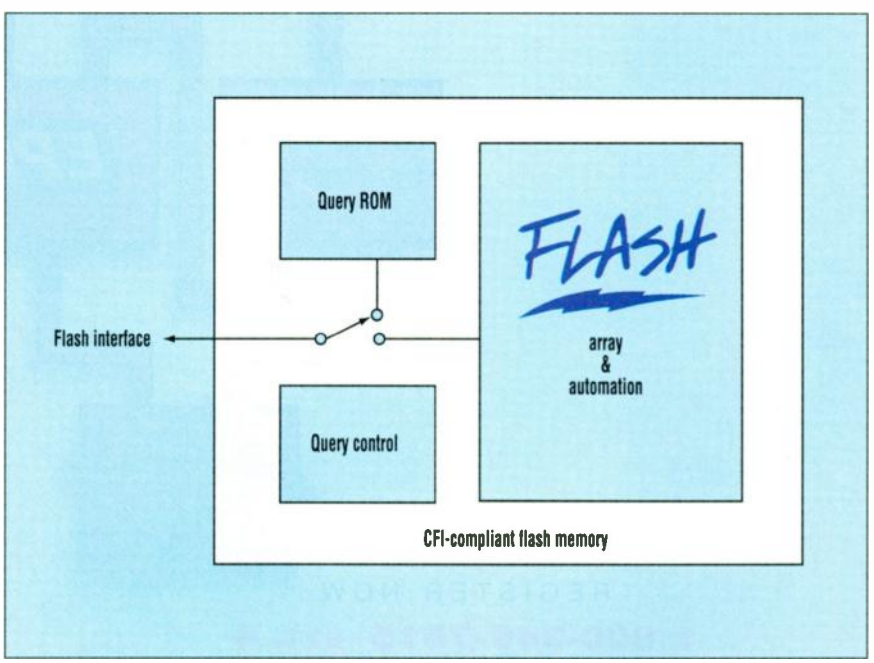
Fortunately, the ease of writing flash software has come a long way in the last year. Systems designers now have a standardized file system, the Flash Translation Layer (FTL), as well as a standardized interface, the Common Flash Interface (CFI), which allows software to sense and adjust to support the flash cards that are found on power-up or insertion. The standardization of both the file system and flash interface lets designers implement a host of new designs that need to take data from an embedded system and use it in the PC. This arrangement provides the opportunity for systems to accept and use the vast bulk of flash single in-line memory modules (SIMMs) and cards manufactured today and in the future, without revising the software.

A Unique Memory Media

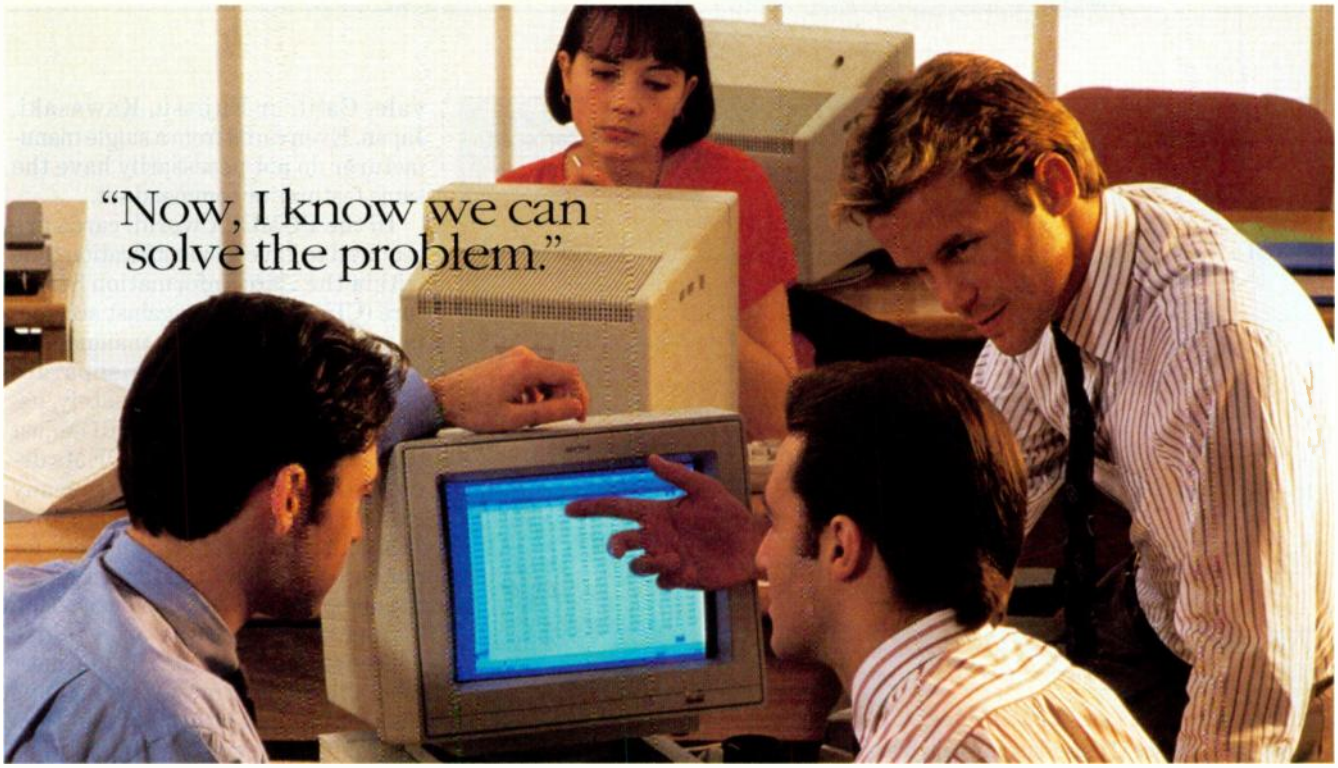
Like ROM or EPROM, flash memory is nonvolatile. Unlike ROM, it can be erased and written many times. With proper software usage, flash memory is rated at one million erase cycles. Today's flash memories use on-board state machines to execute commands such as write and erase. Once provided the address, data, and command, the chip takes care of the rest. On-board state machines cut out the laborious overhead of writing and erasing the flash—no more 15-step Quick Pulse programming algorithms, or the even older Intelligent algorithm with its overprogramming steps.

Flash memory was developed out of and uses EPROM logic. In an erased device, all bits start out as 1's. Programmed bits are 0's. Bits can be programmed singly from a 1 to a 0, just like RAM. Unlike RAM, bits cannot be individually changed back from 0 to 1—a key functional difference between flash and other memory devices.

To change a bit from a 0 to a 1, the device needs to be erased, bringing up architectural hurdle number one: blocking structure. Originally flash memory started with the same block structure as EPROM—one giant array. Over time, variations on blocking were developed. The two most prevalent are asymmetrically-blocked, com-



1. Writing a 98h to the CFI flash memory places it in the Query mode. Further read accesses provide information about such silicon requirements as programming voltage, page buffer depth, and write or erase timeouts.



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ROM Address	Length (bytes)	Description	Ex. Intel 28F008SC
1Bh	01h	V_{CC} Logic Supply Minimum Write/Erase voltage bits 7 - 4 BCD value in volts bits 3 - 0 BCD value in 100 millivolts	1Bh: 30h
1Ch	01h	V_{CC} Logic Supply Maximum Write/Erase voltage bits 7 - 4 BCD value in volts bits 3 - 0 BCD value in 100 millivolts	1Ch: 36h
1Dh	01h	V_{pp} (Programming) Supply Minimum Write/Erase voltage bits 7 - 4 HEX value in volts bits 3 - 0 BCD value in 100 millivolts Note: This value must be 0000h if no V_{pp} pin is present	1Dh: 30h
1Eh	01h	V_{pp} (Programming) Supply Maximum Write/Erase voltage bits 7 - 4 HEX value in volts bits 3 - 0 BCD value in 100 millivolts Note: This value must be 0000h if no V_{pp} pin is present	1Eh: 36h
1Fh	01h	Typical timeout per single byte/word write (buffer write count = 1), 2^N u-sec	1Fh: 03h
20h	01h	Typical timeout for maximum-size buffer write, 2^N u-sec (if supported; 00h = not supported)	20h: 00h
21h	01h	Typical timeout per individual block erase, 2^N m-sec	21h: 0Ah

2. This portion of the CFI specification details the type of information contained within the CFI ROM of the flash components. The example used is the latest Intel 8-Mbit flashfile component. The CFI information shows this device requires a write and erase voltage between 3.0 and 3.6 V on VPP.

monly called boot block due to its frequent use as a boot device in PCs, and symmetrically-blocked. In the asymmetrically-blocked case, block sizes range from 4 to 128 kbits on a single chip. In the symmetrically-blocked case, block sizes are of uniform size throughout the memory array, typically 64 kbits in size. In both cases, erasing a block at a time leaves the other blocks undisturbed.

A second key difference between flash and other memory devices is that the number of times a block is erased, or cycled, needs to be kept relatively constant throughout the device. Flash-silicon manufacturers usually specify the cycling differential allowed between blocks in the array. A differential of 10,000 is typical of an allowable worse case. This cycling-differential limit precludes using the same chip to store frequently cycled data, and infrequently cycled application code. It also prevents using a simple file-allocation table (FAT) filing in the first block of the flash device. Emulating a hard-disk drive by putting track 0 in the first flash block would quickly rack up a 10,000-cycle differential relative to the other blocks. Software, such as FTL, written specifically for flash avoids this problem by creating a FAT table that is periodically moved around in the flash memory. This movement minimizes excessive cycling differentials between the blocks.

From the beginning of flash memory, even prior to the formation of the Personal Computer Memory Card Industry Association (PCMCIA), portable-system manufacturers have been trying to use flash as the storage media in their systems. Its light weight, low power consumption, and robust nature make it the perfect match for battery-powered systems. With the advent of PCMCIA cards, and now Miniature Cards, removable flash exists in form factors for any design. The benefit of cards is the ability to add and remove flash at any time, without redesigning the hardware or software. Data communications companies like Cisco, San Jose, Calif., with their 7000 series router, designed their systems to use flash cards early on in order to give customers the option of plugging in newer and larger programs without having to power down their networks. In most cases, though, the real benefit of cards is their ability to take data back to the PC.

From a software standpoint, the problem of removability lies in not knowing what will be stuck back in the slot. A card from Intel does not behave the same as a card from AMD, Sunnyvale, Calif. or Fujitsu, Kawasaki, Japan. Even cards from a single manufacturer do not necessarily have the same features or command set.

In the PCMCIA world, cards are required to have an identification code within the Card Information Structure (CIS). To ensure against accidental erasure, many silicon manufacturers put their CIS in a separate dedicated device. Unfortunately, using a separate ROM or EEPROM just to hold the CIS adds cost. OEMs demand the lowest cost card, so many PCMCIA cards exist without a CIS. In addition, engineers writing code for motherboards have the same issue on the component level. The purchasing manager wants to be able to use whichever silicon is cheapest or most available at the time. Writing code that interrogates the chip and then self-configures gives the assembly line the ability to use the lowest cost device, and opens up the design to a wide array of second sources.

Common Flash Interface

This concept of keeping a unique ID on the chip is not new. JEDEC, and the JEDEC ID have been around for decades. Standalone programmer manufacturers like Data I/O, Redmond, Wash., have been electrically checking JEDEC IDs and comparing them against the manually selected algorithm since the inception of EPROMs in the early '70s. Software writes a 90h to the device, putting it in the JEDEC ID mode, and then compares the ID to a table of known IDs. The drawback with this method is that supporting new devices (and corresponding IDs) requires a software change. Even a straightforward cost reduction of existing silicon still requires a software revision.

The migration from simple EPROMs to flash memory with its many flavors and vendors, has increased the need for more information to be available for the software. Recognizing this, Intel, AMD, Sharp (Tenri, Japan), and Fujitsu, which represent over 80% of the industry's flash output, defined and published the CFI specification in July 1996.

The CFI specification extends the concept of the existing JEDEC ID residing in the silicon. Instead of just a two-byte identifier, the ID string has

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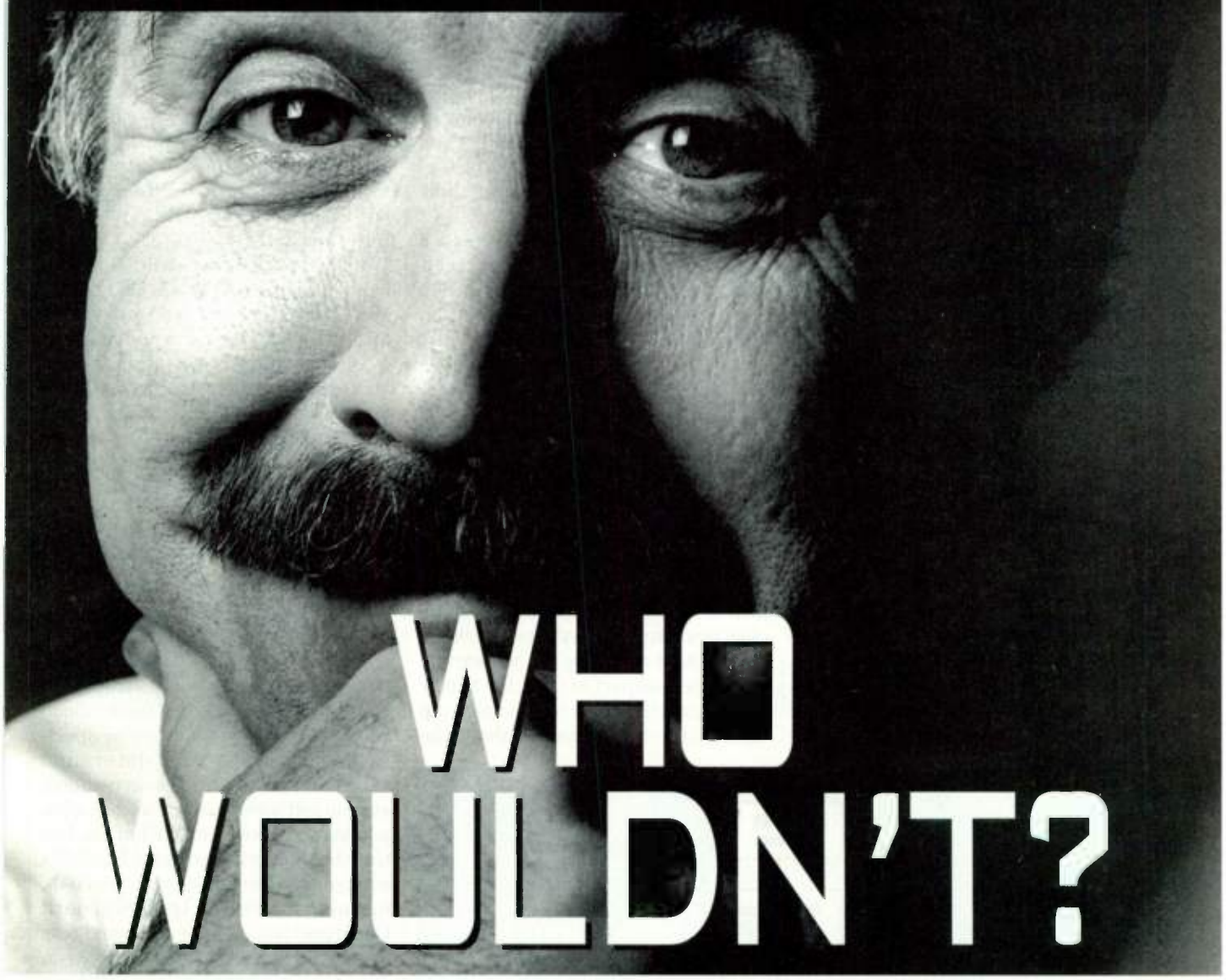

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been increased to 40 bytes and details all of the requirements and capabilities of the chip. Using CFI, software can dynamically configure itself to support cards and SIMMs from multiple vendors. Engineers are making use of the CFI specification to create code that will run on today's flash cards, and be ready to use in the next generations cost-reduced versions. This gives OEMs the ability to convert products to use lower-cost flash memory devices as they become available without rewriting code.

What Is CFI?

The Common Flash Interface has two parts. The first is the Command Set and Control ID code used to specify a vendor-specific control interface for a family of flash devices. The second is a Query ROM on the flash silicon itself, that acts as an on-board ROM look up table (*Fig. 1*).

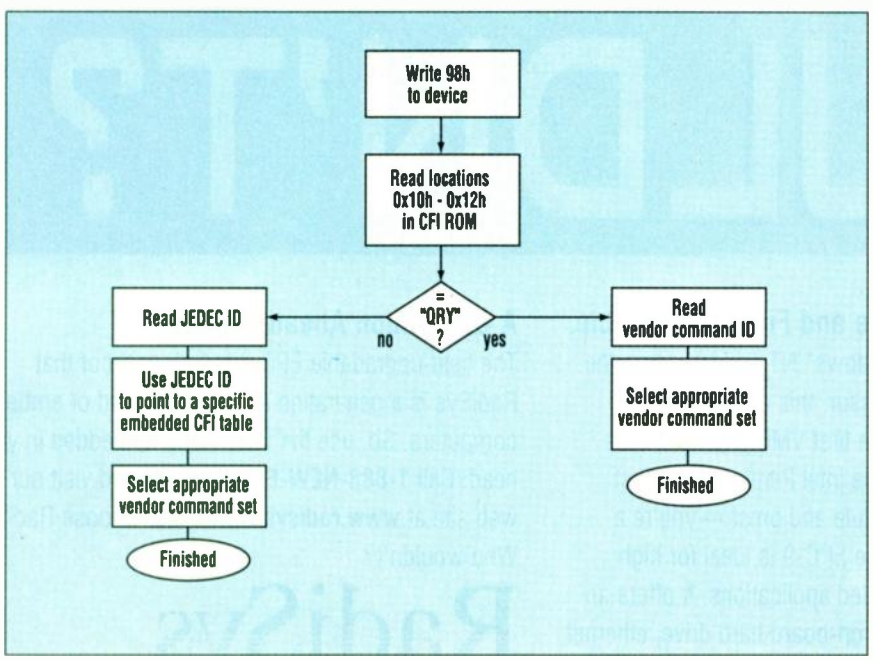
The Command Set and Control ID Code are comparable to a locomotive engine pulling a train of cars. Each vendor has a specific car number (Command Set ID) assigned. These cars, of which there are presently four, each contain the complete algorithm and knowledge to handle families of flash devices. For example, Intel's Standard Command Set, Vendor Command Set number 03h, supports Intel's FlashFile family of products, including the 8-Mbit SA and SC products and the 16-Mbit SA, SV, XS, and XD products. In addition, it supports the forthcoming 4-Mbit SC and 16-Mbit SC chips due later this year. The same algorithm supports other Intel and Sharp devices that use the FlashFile command set, even those that will not be available for a number of years. Flash vendors outside of the original four CFI promoters are petitioning to hook up their cars to the CFI train. The flash group of Mitsubishi Electronics has recently requested their own CFI Control ID Code.

By using CFI, an OEM can create a system that supports the device that it was designed to use, and allows the original design to make use of silicon shrinks and cost reductions that won't exist until well after the design goes into production. Thus, a system manufactured for a number of years of service, like a telephone switch, can take advantage of lower cost memory down the road without rewriting the software. In addition, if the software engineer included support for more than one Vendor Command Set, and the hardware design engineers used a flexible layout, the system could swap over to a competing vendor's flash device without rewriting the software.

The second part of CFI, the Query ROM, is a ROM array on the flash chip that contains information about the silicon's requirements and capabilities. It covers silicon requirements like operating voltages (VCC), and the programming voltages that are required (VPP). It also includes basic architectural information like device size and blocking structure, and capabilities like maximum number of bytes in a multibyte write.

To access the on-board ROM within the chip, system software writes a 98h to address 55h of the device. This puts a CFI-enabled device into Query mode. If the device is CFI-enabled, it will read back "Q", "R", "Y" in the three low bytes starting at offset 10h. Word and word devices will return 00h in all higher order bytes. CFI Query system interface information begins at offset 1Bh with the minimum required VCC logic supply voltage for both write and erase operations, and continues on minimally through offset 2Dh, with the erase block region size and quantity (*Fig. 2*). For asymmetrically-blocked devices, additional erase block region information is located at offset 31h and beyond. (Note: Fig. 2 is a table that represents the 28F008SECFI Query Structure.)

To make use of CFI, a software engineer needs to determine how thorough a job he or she wants to do in supporting the breadth of flash silicon. To support all CFI-enabled flash silicon requires a total of four vendor specified command sets. To determine which command set is the correct one, system software reads offset 13h after putting the device into CFI mode. For the above mentioned Intel Flashfile component, the device will read 03h, meaning it uses the Intel Standard Command Set. Vendor command sets are small, typically taking up between 500 bytes and 2 kbytes. Since CFI is a forward-looking specification, OEMs may want to add support for existing pre-CFI cards and components. In general, a silicon provider's pre-CFI material utilizes the same command set as the post-CFI material. It then becomes a straightforward matter of determining if the silicon is pre- or post-CFI by looking for the "QRY" string (*Fig. 3*). If the silicon is pre-CFI, the OEM adds a JEDEC ID look-up table that identifies the device. CFI Publication 100 lists example CFI parameters for some of the largest selling pre-CFI flash devices



3. The host software flow chart for supporting both CFI and pre-CFI flash devices shows the 98h written to the device and the two paths to select the appropriate vendor command set.

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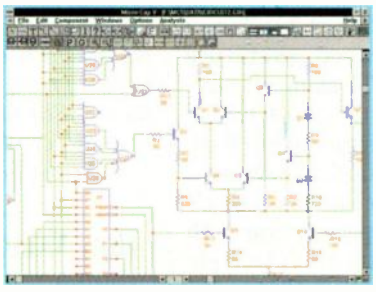

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from both Intel and AMD. If these pre-CFI devices had a Query Mode, this would be the data found in it.

The software engineer can support pre-CFI material by embedding the systems interface information in a lookup table within the code. After identifying the device, OEM system software can then point to the appropriate vendor command set.

Software vendors were among the first to request the CFI concept. Companies such as M-Systems, Santa Clara, Calif., with their FTL product, TrueFFS (TFFS), were among the first to implement CFI. Now that CFI is included in TFFS and found throughout the Microsoft Windows95 operating system, many systems are becoming preenabled for CFI. Consumer electronics manufacturers began taking advantage of the specification by adding CFI-enabled software to their systems in anticipation of the first CFI-based cards. To eliminate incorrectly implementing the CFI specification, these cutting-edge OEM's used CFI hardware emulators provided by the silicon vendors. This cooperation between suppliers and vendors provides these leading edge OEM's with a product feature jump on their competition.

CFI And Miniature Cards

By putting CFI-enabled software into their products, OEMs extend system life and improve the end-user experience at the same time. Digital cameras, audio recorders, and handheld devices like Philips' Velo1 platform are using flash memory in the Miniature Card package. A CFI-enabled camera can interrogate, and use any Miniature Card made. End users are not locked into using just one supplier's cards. Any card that fits into the system works in the system. In addition, cards that will not exist for years will still work in the same camera when they do. As a large camera OEM put it, a 35-mm camera sold five years ago can still use the film sold today. The same requirement applies to flash film. With CFI, a camera OEM can design today's flash in as the digital film, much like cameras from five years ago can use today's 35mm film. This is especially true with the coming of Multi-Level Cycle (MLC) flash.

Flash memory sold today stores one bit of information for every transistor in the array. It does this by comparing the threshold voltage to a known reference. Either the transistor turns on and conducts current or it does not. The concept has remained essentially unchanged since EPROMs were invented in 1972. In 25 years, the ability to measure the charge on the floating gate has grown more sensitive—the fundamental concept with MLC. Instead of a gross higher-than or lower-than analysis, MLC measures discrete states on the floating gate. Numerous flash silicon manufacturers have announced their intention to produce MLC flash product.

In 1997, MLC moves out of the lab and into production. The first generation of MLC flash stores two bits of information per cell. The concept is now being refined to store three and eventually four bits of data per cell. That increase of data storage will dramatically reduce the manufacturing cost per bit to the supplier and the price per bit to the OEM. CFI provides the ability to take advantage of this new technology when it comes off the production line.

Engineers looking for more information on CFI should visit the Miniature Card Web site at http://www.MCIF.org. Both the CFI specification and CFI Publication 100 can be downloaded free of charge. For more information on FTL, contact PCMCIA at http://www.pc-card.com, or a FTL supplier such as M-Systems at http://www.m-sys.com.

Gary Forni is software marketing manager for Intel's Memory Components Division (MCD). He oversees the development of reference software for OEMs designing with Intel flash memory devices, is responsible for standardizing file systems for flash memory cards, and ensures transportability of cards and data from embedded systems to the PC. He holds a BS in Electrical and Computer Engineering from the University of California, Santa Barbara, Calif. He received an MBA from National University, Sacramento, Calif.

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Highly	534
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Exhibit A

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UPDATE ON PORTABLE OPERATING SYSTEMS

Windows OS In Handheld PCs Opens Door To Embedded Systems

Microsoft has introduced Windows CE, a relatively compact operating system that can fit (along with a number of minature applications) into 4 Mbytes of ROM. Initially aimed at handheld PCs, Windows CE will eventually spread into smart telephones, set-top boxes, and specialized information appliances. The first products to incorporate the operating system are a class of companion devices for Windows-based PCs. These handheld PCs are not intended as replacements for desktop or notebook computers, but as "pocketable" information appliances for mobile professionals.

Microsoft also has produced an initial suite of applications along with a hardware reference design for a handheld PC. The reference design calls for a pocketable form factor that can comfortably fit into a jacket pocket or purse, and a QWERTY keyboard. The lack of a keyboard was, according to Microsoft, one of the barriers to wider acceptance of personal digital assistants (PDAs). Additionally, the baseline requires a minimum of 4 Mbytes of ROM and 2 Mbytes of RAM, each of which is expandable. In addition to a serial port and a PCMCIA type II slot, the design calls for an IrDA-standard IR interface. There is an optional docking cradle for use with a desktop PC.

Initially, Microsoft targeted Windows CE for the Hitachi SH3 and the MIPS R4000 processors rather than Intel CPUs. Recently, however, the list of supported devices has expanded to include a host of popular microprocessors such as Intel's X86 family; the Motorola PowerPC; the NEC VR4101; and the TwinChipPIP, PR31500, and UCB1100 units from Philips Semiconductor. In addition, Windows CE will support the Advanced RISC Machines (ARM) architecture on designs from various ARM partners including Digital Equipment and Cirrus Logic. Microsoft plans to offer cross-development support.

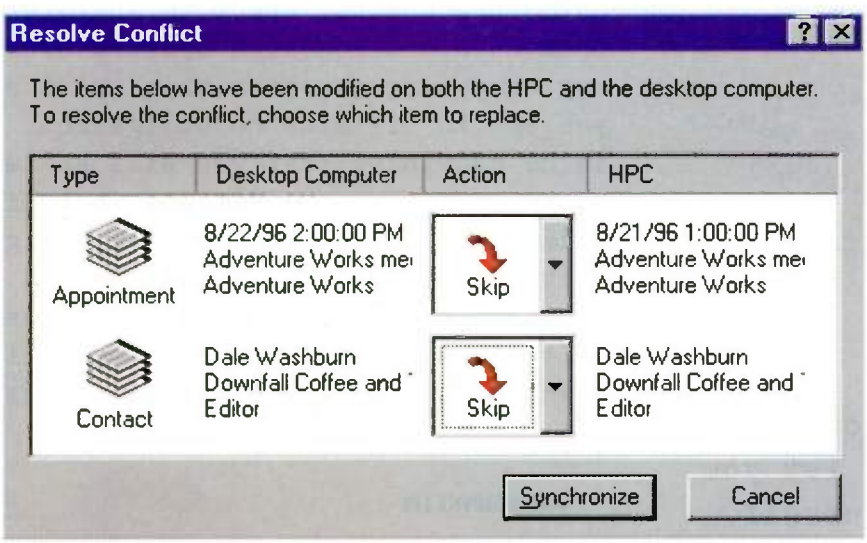
The basic design envisions no hard-disk drive. Applications are downloaded from a host PC, and data is kept separate in battery-backed RAM. This arrangement does not preclude manufacturers from including storage as a standard feature or an option. ACE Technologies, Sunnyvale, Calif.for example, says it will introduce a PCMCIA flash memory card, ShuttleFlash, in 0.5-, 1-, and 2-Mbyte versions.

Besides being able to exchange information with desktop and notebook PCs, handheld PCs are expected to communicate with each other—via the IR link—and to be able to access the Internet. Support for these modes of communication is built into the OS. The Win32 API subset used by Windows CE includes the TCP/IP stack; the PPP protocol; Winsock 2.0; and Microsoft's telephony API, TAPI. A miniature version of the World Wide Web browser, Internet Explorer, is included with the OS.

Microsoft envisions a series of companion applications emerging for the handheld PC to complement the full-featured applications on the desktop. Windows CE supports synchronization of data between applications such as personal information managers (PIMs), from handheld to desktop. The software prompts the user to resolve any conflicts between data sets *(see the figure)*.

Not surprisingly, Microsoft has already developed companion, or pocket, versions of its own applications. There is, for example, Pocket Word, Pocket Excel, and an information manager that corresponds to Schedule+ 7.0. Third party software developers also are developing synchronization software for other applications. DataViz, Trumbull, Conn., in particular, is working on a program called Desktop To Go that will include synchronizers for Lotus Organizer, Internet Sidekick, and ACT! 3.0. Additionally, it will have filters to trade information from Pocket Word and Excel, with WordPerfect, Lotus 1-2-3, and Quattro Pro.

Thanks to the broad CPU support of Windows CE, OEMs will have a wide range of options, not only for designing handheld PCs, but also for the variety of other devices that Windows CE is expected to spawn. Microsoft is counting on three factors that were not present in PDAs, with their proprietary OSs. The first is connectivity to larger Windows-based systems. PDAs that could not easily make the link to synchronize information, left their users with islands of data that were redundant and unsynchronized. Second is the familiarity of users with the Windows environment. Third is the existing base of developers that



Thanks to Windows CE, a portable operating system for handheld personal computers, synchronization of data in applications such as personal information managers (PIMs) are supported. The software prompts the user to resolve conflicts between data sets in handheld and desktop systems.

can leverage their Windows programming skills and experience to develop for a large and homogeneous market.

The development environment for Windows CE is, naturally, Windows 95 and WindowsNT using C, C++, and the Win32 APIs. The Windows CE API is a subset of the Win32 API taken from WindowsNT. Some of the features that were not implemented in the CE version are the security API, MAPI, ODBC, OLE, and DirectX. On the other hand, there are some functions unique to Windows CE. They include SMTP transport, an object store database API, and shell notification.

Since application development takes place on a host PC, it is, even when generating Intel code, a cross-development software process. Microsoft supplies a desktop emulation package called a software development kit (SDK) that provides a complete emulation environment. The SDK includes a number of utilities such as desktop libraries, header files, and Windows CE-specific examples. Using the SDK emulation, developers can expect to build and debug all but the most performance- and hardware-specific elements of an application. The executables are then downloaded to the handheld PC (or other device) via a serial cable connection.

Currently, Microsoft is not offering cross-debugging support which may become necessary if Windows CE moves to more specialized hardware platforms. However, Microsoft plans to offer cross-development tools as add-on packages for its Visual C++ development system in the near future. These tools will include cross-compilers, Win32 for Windows CE libraries, remote debuggers, and all the SDK emulation components. In other words, using the handheld PC and Windows CE as vehicles of the handheld PC and Windows CE, Microsoft finally appears poised to become a major player in the embedded systems industry.

For more information, including technical beta programs for developers, contact Jim Stuart at Microsoft, One Microsoft Way, Redmond, WA 90583; (206) 882-8080; or visit the Web site at http://www.microsoft.com/windows/windowsce.

TOM WILLIAMS

PRODUCT FEATURE

Modular Microkernel Links GUI And Browser For Embedded Web Devices

A modular microkernel teams with an embedded windowing system and a suite of Internet modules to speed the development of embedded web appliances. The new Neutrino microkernel developed by QNX Software provides a core of software services that can be configured by adding modular functionality up to and including a web browser, which is itself modular. QNX has recently entered an agreement with Spyglass , (located in Naperville, Ill.) for the browser technology.

The Neutrino microkernel weighs in at 32 kbytes in its most basic form. In that size, it supplies core real-time services, including thread services, mutexes, condition variables, semaphores, message passing, signals, and scheduling. The Neutrino microkernel is tracking the ANSI POSIX real-time standards, such as the specifications for threads and supports the POSIX 1003.1d draft proposal for interrupts.

In addition to the core services, modules can be added to support processes, POSIX message queues, files systems—including a flash file manager—and networking *(see the figure)*. The process manager makes it possible to build a single multithreaded system process in which all code shares a common address space. Then a number of system processes can be built up, each with multiple threads. This lends itself to a choice of memory protection schemes.

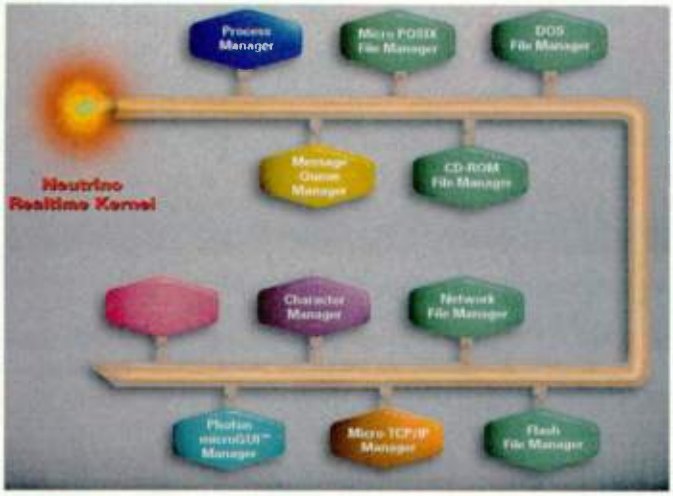
Memory protection is available in three different modes. First, of course, you can choose no protection. Alternatively, the system can be divided into a system's space in which Neutrino and its modules and processes run. A particular user space would contain a variety of user processes within a contiguous address space.

For a more robust system, there's segmented protected memory in which each process in user space has its own protected area of memory. One process can't write into another process's memory area even if it crashes. This also means that a system can be set up to continue running and restart a failed process without bringing down the entire system.

Adding the Photon microGUI manager lets Neutrino incorporate the Photon embedded GUI for systems that need a graphical user interface. The Photon GIU itself is built around a core microkernel that serves a set of optional cooperating processes. Modules include a windows manager, a desktop manager, a VGA graphics driver, and an input driver for mouse or keyboard.

Photon can be accessed over a network from either a QNX, Windows, or X-Windows-based workstation. The same Photon display will appear within a window of the host system regardless of the host's GUI environ-

PRODUCT FEATURE



ment. The device itself can be located on a network anywhere in the world without needing any of its own display hardware.

The network-transparent message passing built into QNX makes possible what QNX calls "JumpGate Connectivity." It lets an applications' entire user interface "jump" from one workstation to another. For example, you could pass over the interface to a networked device to someone else's machine to show them a problem or get advice.

Photon comes with a rapid application builder (RAD) tool called PhAB. PhAB supports point-and-click GUI development, and has a bit-map editor for customizing windows as well as a control panel for customizing widgets. Windows, once created, can be saved as objects. They can be recalled later and be modified for use in other applications. After its created, the user interface is able to automatically generate the underlying C code to link to the application. A multilingual resource editor supports several different language versions of the GUI.

The agreement with Spyglass gives Neutrino and Photon embedded browser capabilities for web-aware appliances, such as set-top boxes, web-aware telephones, handheld terminals, and PDAs. The Spyglass device browser technology will be modular and aimed at minimum memory usage. It will interface to Photon so that the browser running in a set-top box, for example, can display web pages within a Photon window.

Neutrino supports a number of x86 class embedded processors, such as the 486 and NS486SXF, the 386 and 386ER, the 386SE/DE, the AMD Elan and the Pentium and Pentium Pro. Bus Support includes VME, STD, STD32, ISA PCI, PC/104, PCMCIA, and Cardbus.

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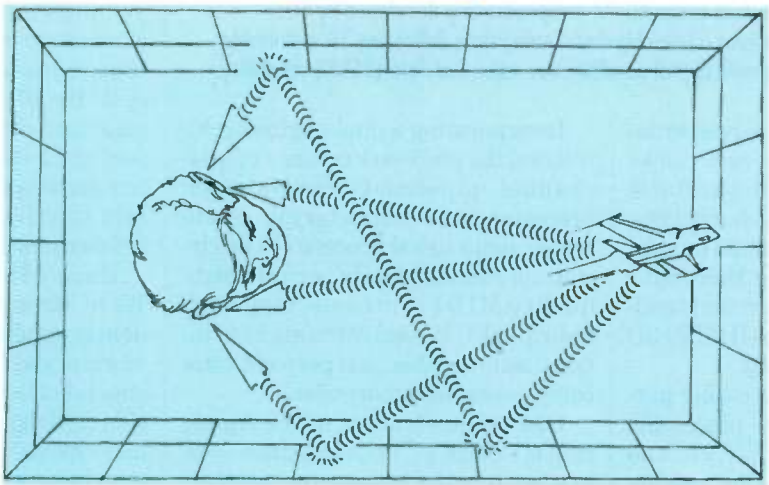
Advanced Multimedia Audio Chips Up Quality And Simplify Systems

Moving From The ISA To The PCI Bus Lets Audio ICs Reduce Complexity And Add Flexibility.

Dave Bursky

SPECIAL REPORT

Few areas of the support-chip arena for personal computers have evolved as rapidly as audio technology. From the basic 16-bit sound-blaster FM synthesis of just a few years ago, the technology has quickly moved to wavetable synthesis to achieve better sound quality. And, to provide better "realism," production schemes are changing from the basic 2D dual-speaker sound to techniques such as 3D enhancement and virtual 3D sound schemes, and in a few cases, full multispeaker Dolby ProLogic or AC-3 subsystems *(ELECTRONIC DESIGN, Nov. 4, 1996, p. 79)*. In just the three months since that article was published, more chips, along with several major licensing deals, have been announced.



Art Courtesy: Aureal Semiconductor Inc.

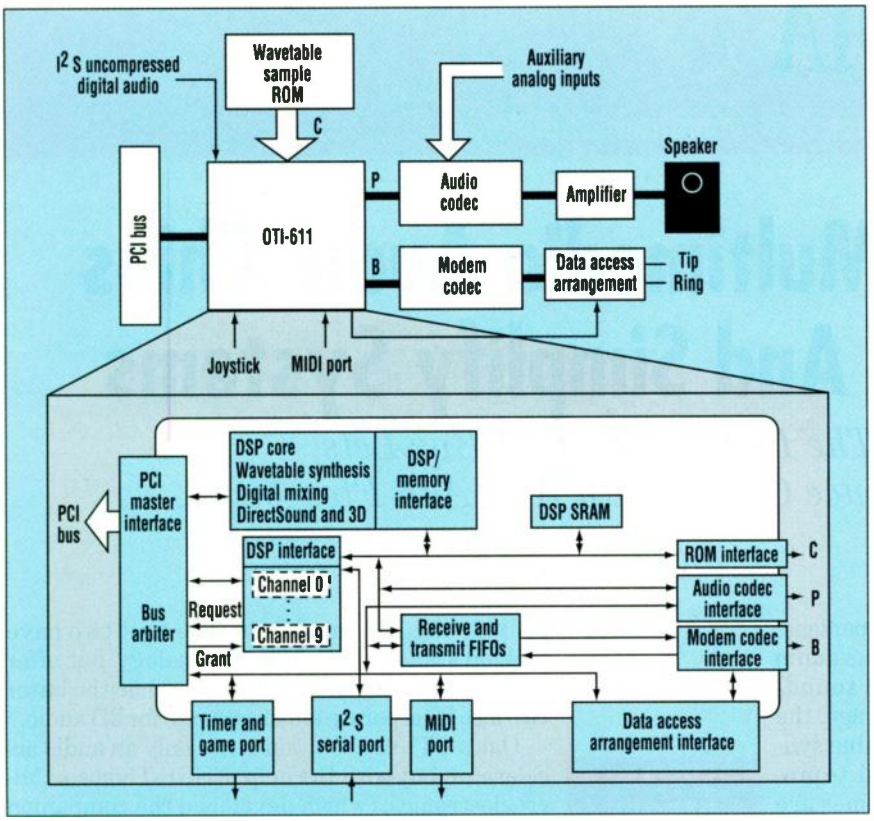
As PCI-based motherboards become the standard in most desktop systems and in some portable computer systems, and ISA bus slots start disappearing (Microsoft Corp. has stated a goal of designing ISA slots out of PCs by 1998/1999), SoundBlaster- or Ad Lib-compatible hardware (the most popular of today's standards for PC gaming), which depend on the ISA interrupt structure, will be rendered useless. Of course, many companies are working on silicon solutions—chips that tie into the PCI bus but internally emulate the ISA/DOS interrupt structure.

Five companies—Oak Technology, Platform Technologies, Rockwell Semiconductor Systems, S3, and VLSI Technology—have all developed single-chip audio solutions for the PCI bus that provide the ISA emulation. The first two have tackled standard 2D audio technology, but offer high-quality wavetable synthesis, while the latter two also incorporate enhancements for 3D audio.

Oak's OTI-611 solution is not only an audio accelerator, but with the help of SGS-Thomson Microelectronics, (which developed the companion codec chip, the STLC7549), the two-chip set provides both audio and modem functions *(see ELECTRONIC DESIGN, Oct. 1, 1996, p. 67, for more on the STLC7549)*. The TelAudia 3D chip set minimizes the board-level chip count and board space requirements, and allows an audio and data-communications subsystem to be implemented with a bill-of-materials cost of less than $50—a significant reduction in cost over a multiple-board alternative *(Fig. 1)*.

The SGS chip includes all analog functions for an advanced multimedia personal computer—CD audio, telephony, and V.34bis data/fax modems (up to 33.6 kbits/s) with digital simultaneous voice and data (DSVD) capability. Incorporating the AC-97 5-wire interface standard that was announced by Microsoft late last year, the chip's codec portion employs a 16-bit delta-sigma architecture and provides a dynamic range of better than 90 dB for the modem section, and 85 dB for the audio portion, when running at sample frequencies up to 48 kHz.

Complementing the analog chip is Oak Technology's OTI-611 digital audio accelerator. The chip contains a programmable digital-signal processor



1. The OTI-611 audio accelerator from Oak Technology offers both modem and audio capabilities. When used with a dual-codec AC-97-compatible chip developed by SGS-Thomson, the combination provides a low-chip-count subsystem delivering 3D wavetable sound and a data/fax modem with digital simultaneous voice and data (DSVD) capability.

and an integrated PCI bus-master interface. The audio processor packs support for general MIDI wavetable music synthesis and multichannel digital and MPEG decoded audio mixing, hardware acceleration for Microsoft's DirectSound (DS) software, and head-related transfer function (HRTF) 3D positional sound processing.

Host-based signal processing performs the modem protocol processing for V.34 data and V.29, V.17, and V.27ter fax applications, thus leaving the DSP block free to execute the HRTF algorithms. In addition to the AC-97 codec interface and the PCI bus interface, the OTI-611 packs game and MIDI ports, an interface to an off-chip wavetable sample ROM, and support for the telephone data-access-arrangement interface.

The Agogo-XP audio controller from Platform also incorporates the AC-97 codec interface. The chip also is compliant with the PC97 audio subsystem specification, the Windows 95 DS and Windows sound systems, and the PCI Bus version 2.1 specification.

Incorporating a dual-engine architecture, the processor consists of a 64-channel pipelined wave-stream processor, and a proprietary programmable audio signal processor. The circuit can simultaneously perform high-quality MIDI synthesis, play back multiple PCM data streams at arbitrary sample rates, and perform voice compression/decompression.

One unique feature of the Agogo chip is its dual PCI bus interface—one bus ties into the host-system motherboard bus, while the other supports up to three bus masters and serves as a multimedia data transfer bus between the audio processor and functions such as videoconferencing, MPEG/DVD engines, 2D/3D graphics controllers, a FireWire high-speed serial interface, or other functions *(Fig. 2)*. The high data transfer rate of the PCI bus versus the ISA bus (a 20-fold improvement) provides plenty of bandwidth to smoothly reproduce high-fidelity sounds from sources such as the Internet, MIDI files, WAV files, and conferencing audio.

The bus serves two purposes. First, it reduces the actual transfer time of audio data, and second, it enables the transfer of multiple independent data streams (time-multiplexed transfers over the PCI bus). These data-handling capabilities are needed to support the next generation of computer games, which will use multiple data streams interfacing to the sound hardware using the DS application program interface (API). The chip can thus provide direct acceleration of DS data by digitally mixing up to 32 PCM streams and sample-rate convert each stream from any frequency to 48 kHz.

Another benefit of the PCI interface is the memory savings and system simplification it permits. In most wavetable audio cards, a local ROM or on-card RAM was needed to hold the wavetable data since the ISA bus was too slow for the real-time transfer of wavetable audio files. With the PCI bus, the host system memory or the hard-disk drive can hold the data and in real time, and can stream the data into the Agogo-based system.

This Wave-Stream processing capability allows system designers to eliminate the separate ROM or RAM, thus reducing the system hardware cost. By allowing the host system's main memory to store the samples as part of the company's WaveCache system architecture, more samples can be kept in active memory, thus providing a richer mix of sounds.

Each of the 64 channels on the Wave Stream interface has independently programmable pan, tremolo, vibrato, and tone filtering. Additional special effects may include reverb, chorus, flange, echo, and 3D spatial enhancement. The chip also includes FM synthesis emulation to support all DOS-based games while providing software developers with an environment to create next-generation audio. And to support the Agogo chip, Platform developed its own AC-97-compatible codec, the PT-101, which adds some extra functionality (a mixer with dual stereo outputs and automatic gain control on the monaural microphone input) on top of the basic AC-97 requirements.

Focusing more directly on the 3D audio market with PCI-based solutions, the SongBird chip developed by Euphonics Inc., Boulder, Colo., and

VLSI Technology, and the SonicVibes chip developed by S3, pack some similarities and some differences with the Agogo processor. For instance, the SongBird chip (the VL82C829) provides full positional 3D audio acceleration along with ISA-bus-based SoundBlaster compatibility over the PCI interface. The chip also incorporates the company's ActiMedia technology, which, like the Agogo chip, allows the wavetable samples to be stored in the host-system's main memory and streamed over the PCI bus to the chip.

The SongBird processor can position multiple audio streams, while concurrently performing high-quality wavetable synthesis, in a full 3D space all around the listener with only two speakers or a set of headphones. That provides a significant differentiation factor between the SongBird and most of the other 3D audio products, which simply widen the sound field (spatialize), or spatialize and pan over a half circle, or localize static sound buffers in dedicated local memory. To perform the full 3D positioning, the chip employs the same psycho-acoustic cues used by the brain to locate sounds in the real world *(again, refer to the aforementioned ELECTRONIC DESIGN article in Nov. 4, 1996).*

Additional effects also can be added—for example, some local RAM to enable reverb and to provide concert-hall type audio effects. The circuit also supports a Dolby Digital or AC-3 MPEG audio decoder surround-sound encoding or a 5.1 channel surround-sound input for DVD audio playback, converting the multichannel inputs into a 3D positional output for two speakers or headphones.

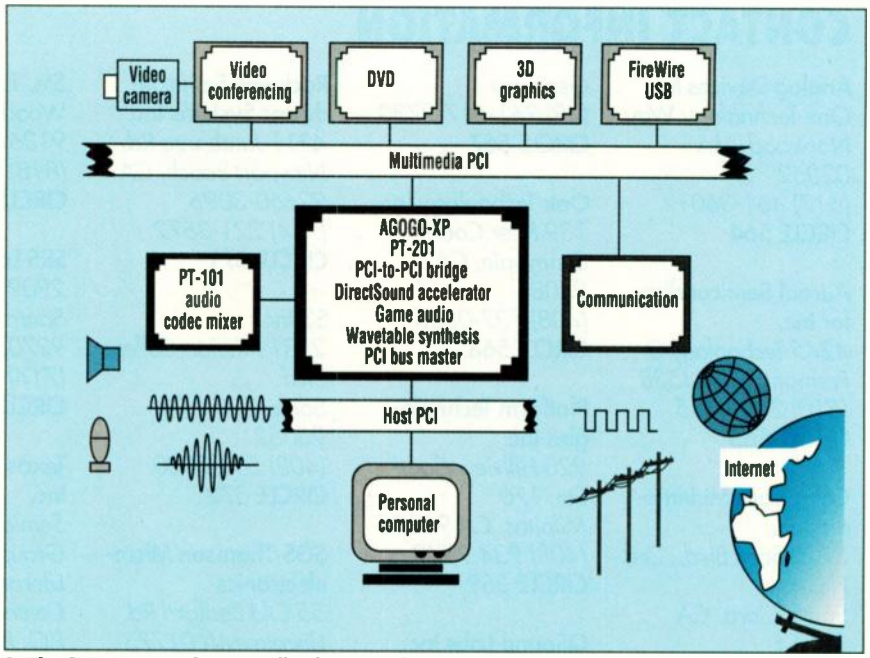
Performing the audio processing on the chip is the company's hybrid DSP engine. The engine handles any combination of up to 32 stereo synthesized voices and/or sound-effect tracks running under an on-chip multitasking kernel that manages the audio-optimized code. As with the Agogo processor, the Intelligent Wavetable caching in main memory and ROM-less wavetable approach opens the door for software that can be upgraded for sound libraries, while the processing bandwidth of the DSP core provides ample throughput to support advanced audio functions.

SongBird supports both the AC-97 interface standard and the DS API and provides full MIDI and Roland MPU401 standard compatibility. The SoundSuite firmware for the chip was developed by EuPhonics, a well-established company that provides high-quality audio products. Additional software partners include Echo Speech Corp., Carpenteria, Calif., which developed some of the hardware, firmware and software subblocks, and DiamondWare Ltd., Chandler, Ariz., who developed extensions to the DS API, known as DEV3D.

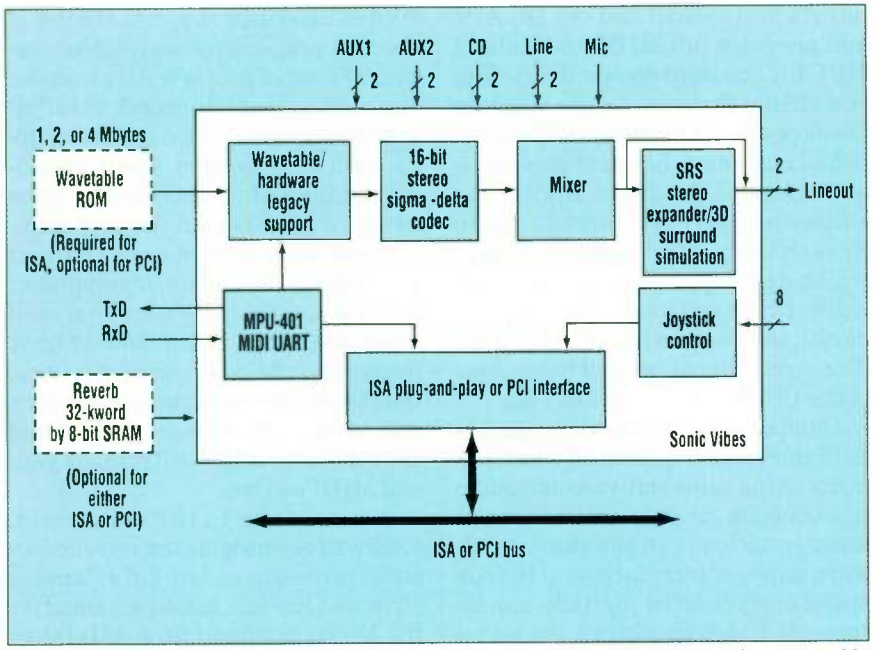
Competing with the SongBird is the SonicVibes chip from S3 which has many of the same software and audio reproduction capabilities. One area of differentiation is on the chip's hardware support interface—up to four speed-compensated joysticks can be supported, thus simplifying the set up for multiplayer gaming systems *(Fig. 3)*. To achieve the ISA/DOS compatibility, the chip's designers spent much time developing the distributed DMA scheme for the PCI bus master interface. Internally, the chip looks for ISA activity and responds to it by translating the operations into PCI activity.

Like the other chips, the SonicVibes processor supports the use of the host memory for wavetable storage. S3's name for their data transfer and management approach is Infini-Patch—so named since the use of updateable host memory allows an infinite number of wavetable files to be swapped in and out of the host memory and downloaded to the chip as needed. As part of its development program, S3's designers analyzed about 3600 songs and allocated higher memory to the most common sounds, thus providing an optimized memory map to minimize memory updates and give the user a 128-instrument general MIDI palette.

A newcomer to the audio field, Rockwell Semiconductor, unveiled an audio processor at last fall's Comdex show and has just added a license for the Aureal Semiconductor, A3D Interactive 3D audio algorithms. In return, Aureal gets rights to some of Rockwell's audio technology. Aureal, in conjunction with Crystal River Engineering, a company Aureal eventually purchased, developed the A3D Interactive positional 3D audio algorithms, and then introduced its own 3D audio processor and PCI bus chip set, the



2. The Agogo-XP audio controller from Platform incorporates the AC-97 codec interface standard, which is a five-wire interface that provides a standard interface to a codec. One of the most unique features of the Agogo chip is its dual PCI bus interface—one bus ties into the host-system motherboard bus, while the other supports up to three bus masters and serves as a multimedia data transfer bus between the audio processor and functions such as videoconferencing, MPEG/DVD engines, 2D/3D graphics controllers, and a FireWire high-speed serial interface.



3. S3's SonicVibes audio accelerator is almost a full audio card on a chip. It provides wavetable audio and legacy Sound-Blaster FM-synthesis plus DOS compatibility using distributed DMA and SerIRQ support over the PCI bus. For 3D sound enhancement, the chip also includes SRS stereo expansion.

ASP301/311 *(ELECTRONIC DESIGN, Nov. 4, 1996, p. 79).*

Aureal also offers another chip, the VSP901, that can play back Dolby ProLogic sound over a standard set of headphones. The chip converts the four-channel ProLogic signals into two channels through the use of the A3D algorithms. The A3D algorithms have become very popular since they provide positional 3D reproduction, and thus Aureal has inked a number of other licensing arrangements with other audio and DSP chip suppliers. One recent licensee, Oak Technology, has already incorporated it into the OTI-611 to achieve HRTF processing.

Dolby ProLogic surround sound is also delivered by the DPL3520A developed by ITT Semiconductors. The chip decodes stereo signals and allows the sound to,be played back through four or six speakers. The device supports all standard operating modes called out by the ProLogic specification. It includes such functions as Panorama sound and Pseudo surround sound to play back non-corrected sources over multiple speakers. All provides the processing circuits for baseband audio (volume, bass, treble, balance, and loudness) for six channels, minimizing the required off-chip circuits to complete the decoding system. Additional versions of the decoder chip, the DPL3518A and 3519A,

CONTACT INFORMATION

Analog Devices Inc.
One Technology Way
Norwood, MA 02062
(617) 461-3601
CIRCLE 564

Aureal Semiconductor Inc.
4245 Technology Dr.
Fremont, CA 94538
(510) 252-4245
CIRCLE 565

CompCore Multimedia Inc.
3120 Scott Blvd., 2nd Flr.
Santa Clara, CA 95054
(408) 567-0552
CIRCLE 566

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Hans-Bunte-Strasse 19
D-79108 Freiburg, Germany
(49) 761-517-2730
CIRCLE 567

Oak Technology Inc.
139 Kifer Court
Sunnyvale, CA 94086
(408) 737-0888
CIRCLE 568

Platform Technologies Inc.
920 Hillview Court, Ste. 170
Milpitas, CA 95035
(408) 934-9579
CIRCLE 569

QSound Labs Inc.
2748 37th Ave. N.E.
Calgary, Alberta, Canada T1Y 5L3
(403) 291-2492
CIRCLE 570

Rockwell Semiconductor Systems Inc.
4311 Jamboree Rd.
Newport Beach, CA 92660-3095
(714) 221-3672
CIRCLE 571

S3 Inc.
2831 Mission College Blvd.
Santa Clara, CA 95052
(408) 588-8000
CIRCLE 572

SGS-Thomson Microelectronics
55 Old Bedford Rd.
Lincoln, MA 01773
(617) 259-0300
CIRCLE 573

Spatializer Audio Laboratories Inc.
20700 Ventura Blvd., Ste. 134
Woodland Hills, CA 91364
(818) 227-3370
CIRCLE 574

SRS Labs Inc.
2909 Daimler St.
Santa Ana, CA 92705
(714) 442-1070
CIRCLE 575

Texas Instruments Inc.
Semiconductor Group, SC-96076
Literature Response Center
P.O. Box 172228
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CIRCLE 576

Toshiba America Electronic Components
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Irvine, CA 92718
(714) 455-2000
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Virtual Listening Systems Inc.
4637 Northwest 6th St.
Gainesville, FL 32609
(352) 379-0807
CIRCLE 578

VLSI Technology Inc.
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San Jose, CA 95131
(408) 434-3000
CIRCLE 579

Zoran Corp.
2041 Mission College Blvd.
Santa Clara, CA 95054
(408) 986-1314
CIRCLE 580

and 3419A are bused on the same DSP core used in the DPL3520A, and serve as coprocessors for digital, multistandard sound processor subsystems.

Another company that just signed a deal with Aureal is Zoran. Late last year, it released a more advanced version of its Dolby AC-3 decoder chips. The ZR38600 has a throughput of about 40 MIPS, performs full AC-3 and MPEG-2 decoding and has about 10 MIPS of headroom Those unused MIPS can be applied to execute the 3D sound algorithms.

Decoding for AC-3 applications is also available on another chip developed by SGS-Thomson—the STi4600. A fully-integrated Dolby AC-3 circuit, the STi4600 delivers the 5.1-channel output. Targeted for set-top boxes and DVD players, the chip includes support for Dolby ProLogic decoding.

A pair of solutions are available from Analog Devices. The first is based on a dedicated chip for the combined audio and data functions, and another based on the company's SHARC high-performance DSP chip. The AD1820 is a single-chip processor that combines a 20-voice music synthesizer with SoundBlaster compatibility, on-the-fly sample rate conversion and synchronization, and host-assisted modem and audio processing. The algorithms are part of the soundComm software that was jointly developed with Smart Link Ltd., Natania, Israel. Another member of the product family, the Phat stereo chip, provides 3D stereo sound.

The SHARC-based solution unveiled late last year, provides what Analog Devices calls a next-generation signal processor. Employing the Analog Devices ADSP-2106x series of DSP engines, the architecture handles real-time music synthesis. The software achieves that performance by using a comprehensive library of more than 300 optimized music functions (opcodes). Some of the opcodes include sampled-waveform playback oscillators, filters, mixers, and reverberators, as well as advanced functions like audio-input harmonization, FFT-based phase vocoder signal reconstruction, and a string "pluck" model.

Also looking at DSP-based audio solutions is the TLC320AD80 audio subsystem developed by Texas Instruments It combines a stereo audio DAC, volume and balance controls, an analog TV baseband audio decoder, a de-emphasis filter, and an analog wideband multiplexer in one chip.

Besides the general-purpose DSP chips, some of the new, programmable multimedia processors, such as the Mpact from Chromatic Research and sold by SGS-Thomson and Toshiba, have licensed algorithms to provide 3D or enhanced 2D sound. The TruSurround algorithms developed by SRS Labs will be incorporated into the next release of the Mpact Mediaware software, expected this quarter.

CompCore MultiMedia (now owned by Zoran) also has licensed the N-2-2 digital virtual surround sound technology from Spatializer Audio Labs and will incorporate that technology into its Dolby Digital (AC-3) software, which is the audio component of CompCore's SoftDVD. This technology incorporates many psychoacoustic techniques to allow playback of the 5.1-channel AC-3 data streams over a two-speaker system and still retain the positional information of the sounds. CompCore also has a development partnership with QSound Labs for its QSurround 3D audio for AC-3 subsystems as well. The N-2-2 algorithms also have been ported to Zoran's 38600AC-3 processors.

A headphone-based 3D surround sound processor, Auri Direct, is the commercial release of an inhouse technology developed by Virtual Learning Systems. It accurately reproduces 3D surround sound over standard headphones. Implemented on a 56000 family DSP chip from Motorola, the Auri sound algorithms make use of Dolby ProLogic and Teltec processing schemes. As part of the software, the user can select a "custom" head-related transfer function to best suit the ears and provide the most accurate sound locations for the processed audio. Three DSP modes are available: ProLogic, stereo, and mono, for choosing processing based on signal format. Three Venue modes are also available: theater, hall, and club, to select the simulated acoustic environment.

How Valuable	Circle
Highly	561
Moderately	562
Slightly	563

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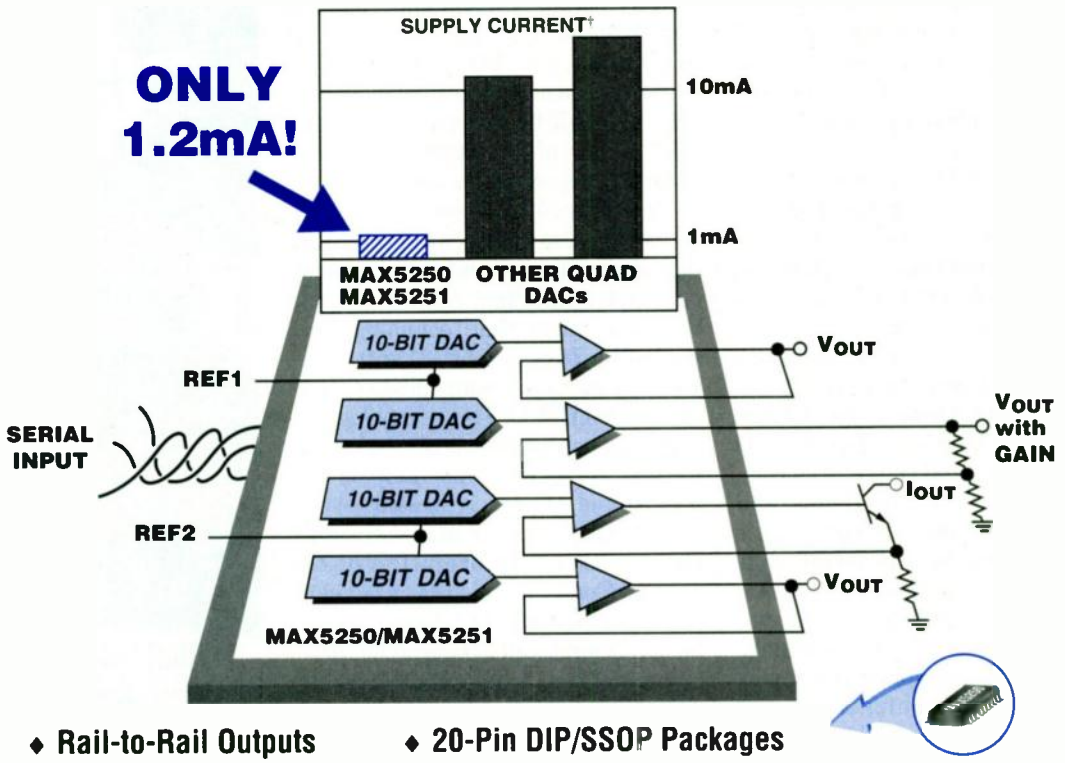

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Scope Calibrator Does Not Require Adjustment

CHESTER SIMPSON
National Semiconductor Corp., 2900 Semiconductor Dr., MS-D2740, Santa Clara, CA 95052-8090; (408) 721-7501.

Measurements made by an oscilloscope are only as accurate as its calibration. The circuit presented provides an inexpensive way to build a reference that can check both the vertical gain and horizontal sweep rate of an oscilloscope. This calibrator provides a precision 4-V square-wave output at frequencies of 100 Hz, 1 kHz, 10 kHz, 100 kHz, and 1 MHz.

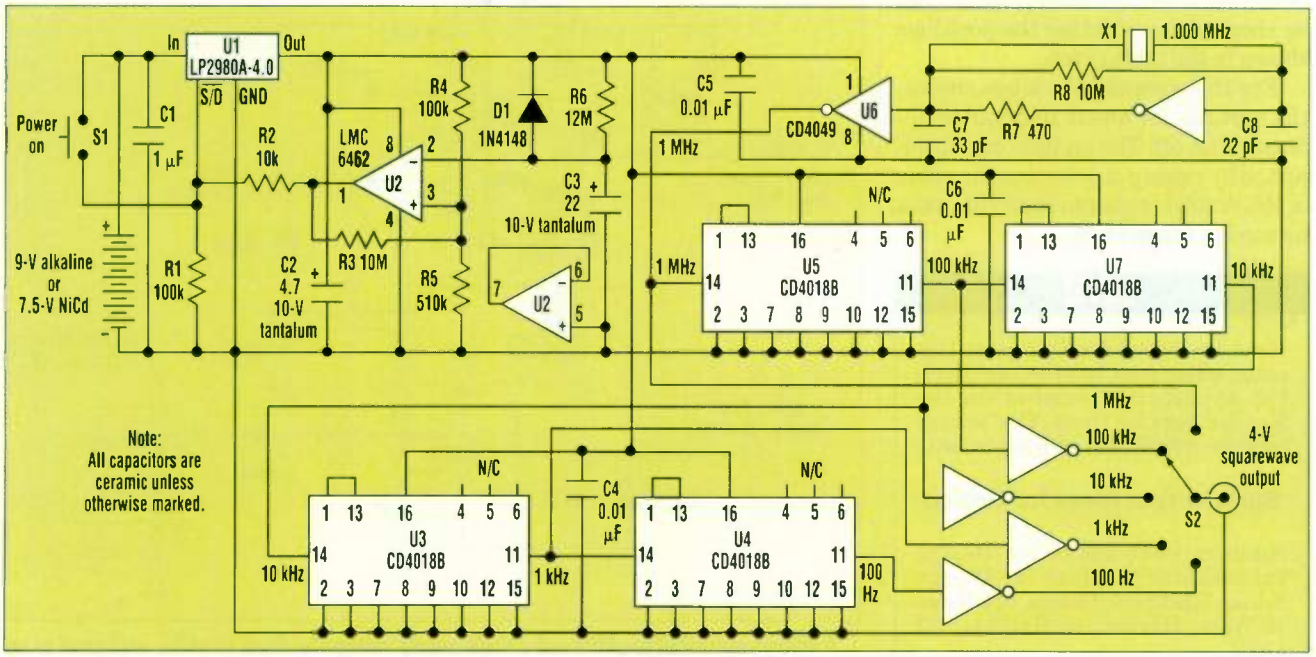
Key features of the design include: no calibration or adjustment is ever required, and no warm-up period is needed; the instrument can be made very small for portability; and it operates from any supply voltage between 4.5 V and 15 V, drawing less than 2 mA while operating (a typical 9-V alkaline battery would provide over 200 hours of on time). To guard against accidentally leaving it on, circuitry is provided that automatically turns the unit off after 10 minutes.

Looking at the circuit's operation, a 1-MHz clock is constructed using crystal (X1) and a CD4049 hex inverter (U6) *(see the figure)*. Because the frequency accuracy of all of the outputs depends on X1, a good quality crystal should be used (accuracy of 0.1% or better). The 1-MHz is divided down by four decade counters (U3, U4, U5, and U7) to provide outputs of 100 kHz, and 10 kHz, 1 kHz, and 100 Hz. All of the CD4018 outputs are connected through U6 inverters before switch S2 because the CD4049 outputs have faster rising/falling edges than the outputs of the CD4018.

U1 and U2 provide a regulated 4-V power supply. U1 is a fixed 4.0-V (±0.5%) precision voltage regulator. It's most important feature for this application is that it draws less than 1 µA of supply current when the shutdown pin is low. Because of this, it doesn't ever have to be discon-

SWEEP SPEED POSITIONS

Tester Frequency (Hz)	Horizontal (time/division)	# Cycles/10 Divisions
1M	0.1 µs	1
1M	0.2 µs	2
1M	0.5 µs	5
100k	1 µs	1
100k	2 µs	2
100k	5 µs	5
10k	10 µs	1
10k	20 µs	2
10k	50 µs	5
1k	0.1 ms	1
1k	0.2 ms	2
1k	0.5 ms	5
100	1 ms	1
100	2 ms	2
100	5 ms	5
100	10 ms	10



Both the vertical gain and horizontal sweep rate of an oscilloscope can be checked with this low-cost calibrator.

nected from the battery.

U2 and associated components control the shutdown pin of U1. When the "PWR ON" button (S1) is pressed, the shutdown pin is pulled high. This turns on U1, which supplies 4 V at its output. The 4 V applied to U2 causes it to pull its output (pin 1) high, which will hold the shutdown pin of U1 high until capacitor C3 charges up to about 3.35 V. At that point, the output of U2 will go low, U1 will turn off, and the whole unit deactivates until S1 is pressed again.

When testing for vertical gain, set the scope's vertical input attenuator to 1 V/div and connect the tester (note: the oscilloscope to be calibrated should be allowed to warm up for at least 30 minutes prior to adjustments). Set the tester's frequency to 100 Hz and the scope's horizontal sweep rate to 1 ms/div. Center the waveform vertically, and verify that the amplitude is exactly 4 divisions peak-to-peak.

For deflection accuracy, change the input attenuator to 0.5 V/div after the vertical gain is set (previous paragraph). Center the waveform, and verify that it's exactly 8 divisions peak-to-peak. Accuracy of the displayed waveform should be better than ±2% for a good oscilloscope.

To calibrate the time base, set the tester to 1 kHz and the scope sweep rate to 0.1 ms/div. Adjust the sweep speed so that exactly one square wave is displayed on the 10 division horizontal deflection. Other sweep speeds can be checked by selecting the positions shown in the table given.

For the component values shown, the unit ran for about 10 minutes before it shut off. The on time can be adjusted by raising or lowering the value of R6. A solid tantalum capacitor must be used at C2 and C3.

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Circle 521

Fast AGC Amplifier Has Logarithmic RSSI

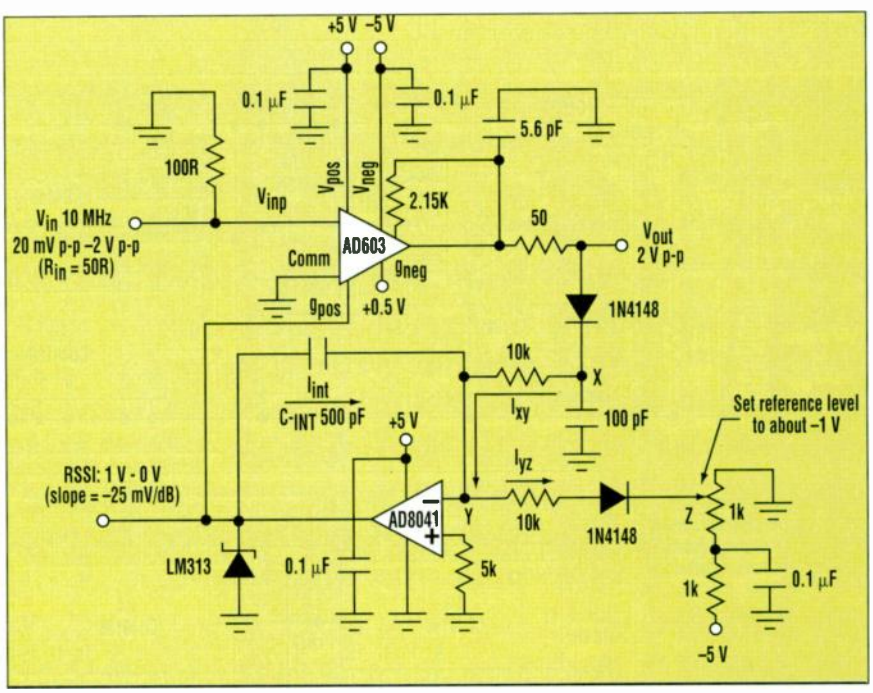
LEW COUNTS and EAMON NASH
Analog Devices, One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106; (617) 329-4700; fax (617) 326-8703.

A fast and accurate automatic-gain-control amplifier can be implemented using a voltage-controlled amplifier (VCA) and a single-supply voltage-feedback amplifier configured as an integrator *(Fig. 1)*. The AD603 VGA has a "linear in dB" transfer function. Varying the differential gain-control voltage ($G_{pos} - G_{neg}$) from –0.5 V to +0.5 V changes the amplifier gain from 0 dB to +40 dB (25 mV/dB).

The output signal from the AD603 is half-wave rectified and filtered using a switching diode and an RC combination (100 pF/10k). This RC combination yields minimum ripple at the popular 10.7-MHz intermediate frequency (IF). The dc representation of the VCA output signal generates a current I_{xy} that flows through a 10k resistor into the inverting node (Y) of the AD8041 op amp. A reference voltage of about –1 V causes a constant current to flow from this node through another 10k resistor (a diode is included in this reference circuit to compensate for the drift of the rectifier diode). The difference between these currents (I_{int}) flows through the integrator capacitor.

The integrator output voltage ramps up or down (varying gain) until I_{xy} (signal strength current) is equal to I_{yz} (reference current). When this equilibrium point is reached, the current I_{int} decreases to zero, causing the integrator (and hence the gain-control voltage) to settle. This occurs when the output voltage from the AD603 reaches approximately 2.4 V p-p. Because the inverting gain-control input G_{neg} has been offset to 0.5 V, the control voltage to the VGA swings from 0 V to 1 V, changing the gain from 0 dB to +40 dB.

The top trace of the oscilloscope



1. A voltage-controlled amplifier and a single-supply voltage-feedback amplifier configured as an integrator can create a fast and accurate automatic-gain-control amplifier.

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ERA-2SM	DC-6000	15.2	12.4	4.6	26.0	40	2.00
ERA-3	DC-3000	20.8	12.1	3.8	23.0	35	2.10
ERA-3SM	DC-3000	20.2	11.5	3.8	23.0	35	2.15
ERA-4	DC-4000	13.5	▲17.0	5.5	▲32.5	65	4.15
ERA-4SM	DC-4000	13.5	▲16.8	5.2	▲33.0	65	4.20
ERA-5	DC-4000	18.8	▲18.4	4.5	▲33.0	65	4.15
ERA-5SM	DC-4000	18.5	▲18.4	4.3	▲32.5	65	4.20
ERA-6	DC-4000	11.3	▲18.5	8.4	▲36.5	70	4.15
ERA-6SM	DC-4000	11.3	▲17.9	8.4	▲36.0	70	4.20

Note: Specs typical at 2GHz, 25°C. Exception: ▲ indicates typ. numbers tested at 1GHz.
* Low frequency cutoff determined by external coupling capacitors.
① Price (ea.) Qty.1000: ERA-1 $1.19, -2 $1.33, -3 $1.48, -4, -5 or -6 $2.95. SM option same price.

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Size (mils)	Value
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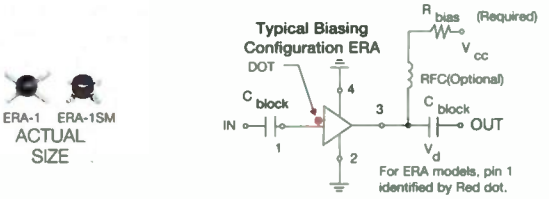
120x60	.002, .047, .068, .1 µf



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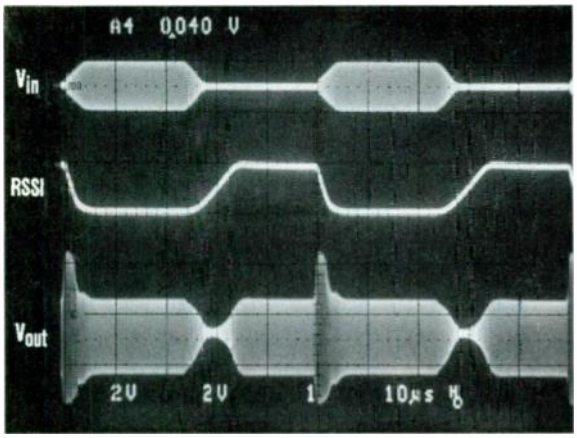

2. The top trace indicates the envelope of the input signal to the AGC amplifier. The middle trace shows the resulting gain-control voltage from the integrator, while the lower trace shows the voltage at the output of the AGC amplifier.

photo shows the envelope of the input signal to the AGC amplifier *(Fig. 2)*. This is a 10-MHz sinewave that has peak-to-peak amplitude switches between 20 mV to 2 V every 25 µs. The middle trace shows the resulting gain-control voltage from the integrator (swinging between 0 V and 1 V). The lower trace illustrates the voltage at the AGC amplifier's output.

From the middle and lower traces, it's evident that the AGC loop has a full-scale (0-40 dB) settling time of 10 µs when gain is increasing. When gain is decreasing, the settling time is 4 µs. The settling time can be decreased or increased by varying the value of C_{int}, which sets the integrator time constant. However, for lower integrator capacitor sizes, the gain-control response begins to ring when the gain is decreasing. This increases the settling time when gain is decreasing. As a result, an integrator capacitance of about 400 pF yields a full-scale settling time of 6 µs for both positive and negative gain ramping.

This gain-control voltage also can be used as an indicator of the input signal's received strength. This received signal strength indicator (RSSI) is inversely proportional to the log of the signal amplitude and has a slope of –25 mV/dB.

The integrator's output voltage is clamped on the high side to +1.2 V by a +1.2-V reference diode. On the low side, the single supply on the AD8041 prevent s the integrator voltage making excursions below ground.

Circle 522

Optically-Isolated Amplifier Has Super-Stable Zero

W. STEPHEN WOODWARD
Venable Hall, CB3290, University of North Carolina, Chapel Hill, NC 27599-3290; Internet: woodward@net.chem.unc.edu

Acquisition of low-level signals that require galvanic isolation, such as those from thermocouple temperature sensors in electrically noisy environments, is a messy but sometimes unavoidable design problem. Commercially available isolation amplifiers, although convenient and adequate for interfacing higher-level signals, suffer from large zero-offset errors and drift (multiple millivolts and tens of microvolts per °C, respectively). This makes them unsuitable for handling the microvolt outputs typical of some sensors.

By contrast, the amplifier described here achieves typical zero-offset error and drift of 3 µV and 0.01 µV/°C—three orders of magnitude better than conventional isolation amplifiers—by using the chopper-stabilized, micropower LTC1047 combined with optical coupling *(see the figure)*. Because galvanically isolated devices need a separate isolated power supply for each channel, this circuit maximizes ease of use with its unusual ability to handle bipolar signals while drawing no more than 300 µA from a single +5 V to +16 V unregulated supply rail. As a result, even an inexpensive 9-V alkaline "transistor" battery will support thousands of hours of continuous operation.

To understand the circuit's operation, consider first a positive input. This will pull A1's noninverting input high, forcing A1 to source current through LED E3 and through R2 to track it. The E3 current will produce a proportional photocurrent in Q3, which will tend to pull A3's inverting input low. To restore balance, A3 will respond by driving the E2/Q2 optical pair to pass an equal and opposite photocurrent.

Because of the symmetrical operating points of the E2/Q2 and E3/Q3 pairs, and their sharing of the same DIP package, their coupled gains will track well and provide good (< 1%) linearity and temperature stability in the E3/E2 current ratio. Overall amplifier gain for positive inputs is 33,333/R2 = 1000 (5 V out for 5 mV in), with R4 used to trim out minor mismatches in optocoupler gain.

For negative inputs, A2 takes over by sourcing current through E1 so that the current through R3 balances the input-proportional current through R1. R5 is used to accurately calibrate the negative-signal gain to the same 33,333/R2 value.

Power drawn from the isolated supply varies from 120 µA under zero-signal conditions, to 270 µA at full scale. A 500-mAhr alkaline 9-V battery can therefore be expected to provide 1800 to 4200 hours, or 2 to 6 months of continuous operation. Circuit bandwidth extends to several kilohertz for signals that don't frequently cross zero.

Response to positive-to-negative zero crossings is slow because it must include the 50- to 70-µs saturation recovery time of A2. This is a price easily paid in low-frequency applications like temperature sensing, in return for the superior zero-drift performance of the LTC1047. But for applications that require a snappier response around zero, ade-

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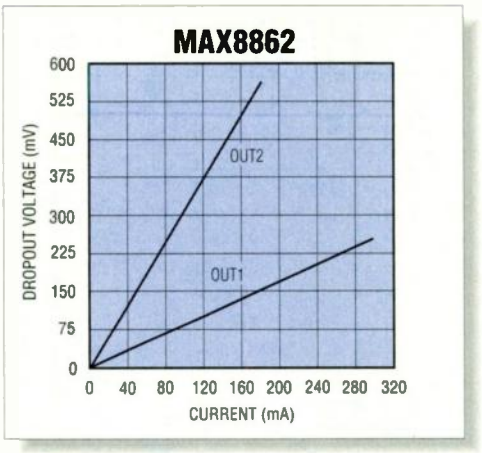

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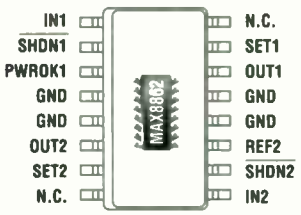

12V maximum input

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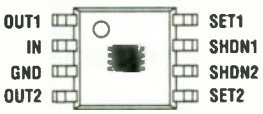

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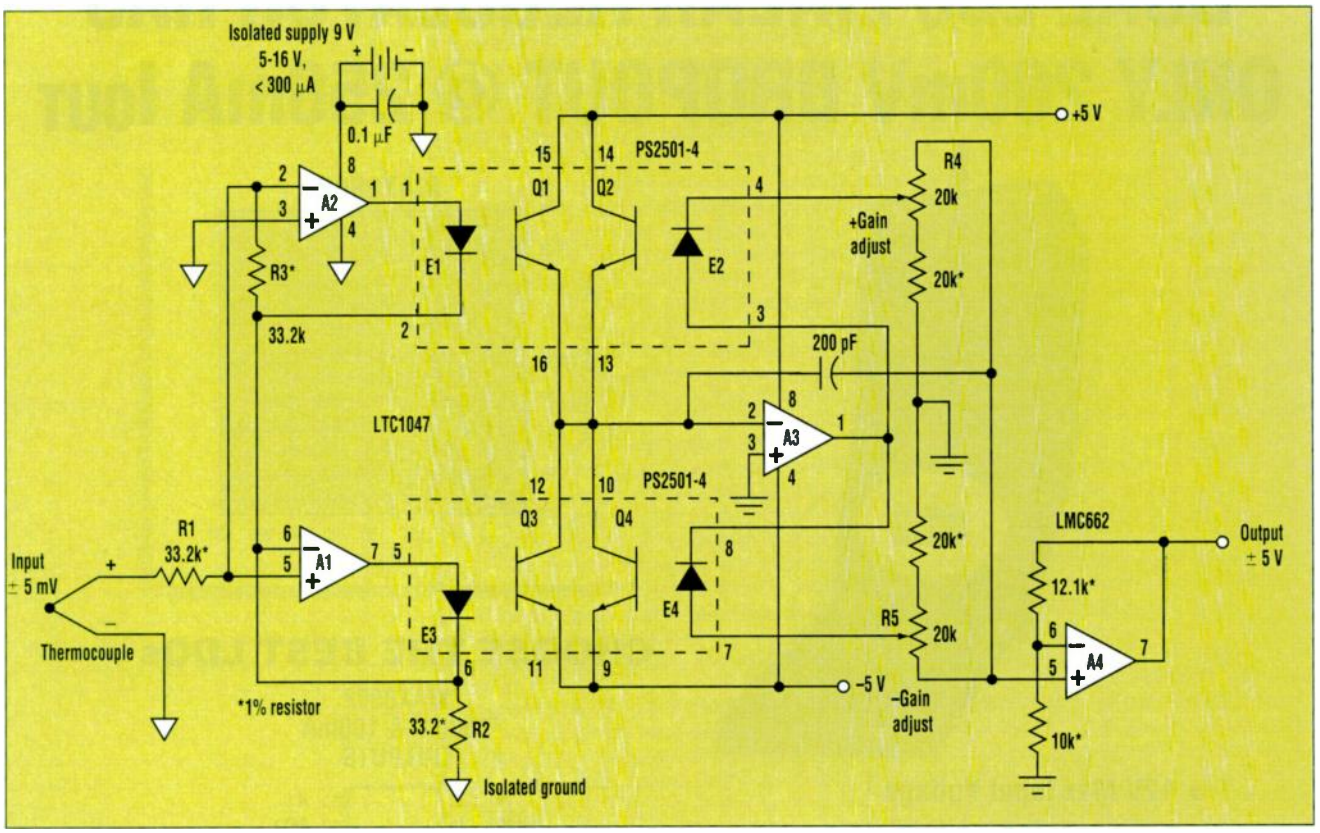


By using the micropower LTC1047 along with optical coupling, this amplifier achieves typical zero-offset error and drift of 3 µV and 0.01 µV/°C.

quate accuracy (< 1 µV/°C—still many times better than commercial isolators) can be provided by substituting any one of many bipolar micropower precision duals, such as the LT1178, for A1 and A2.

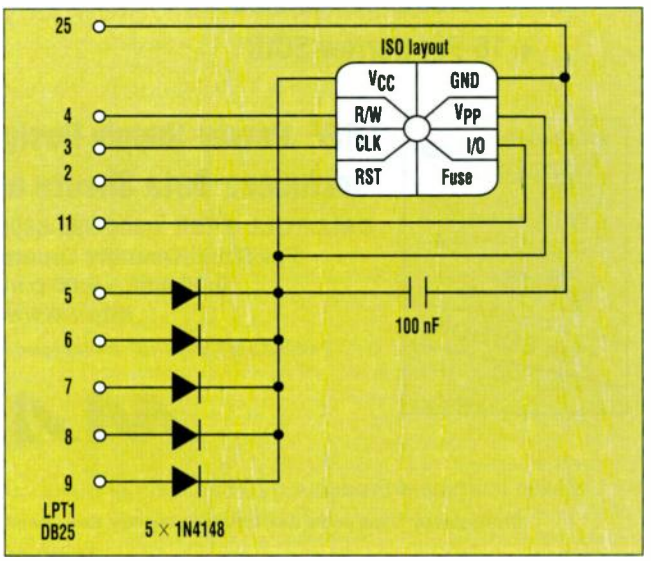
Circle 523

Simple PC Smart Card Reader Enhancement

JOSE CARLOS COSSIO
Acebedos, 11, 6-C, 39001 Santander, Spain; (+34) 42 370023.

The previously published Idea for Design titled "Simple PC Smart Card Reader" (ELECTRONIC DESIGN, *July 8, 1996, p. 113)* can be improved by taking into account the current output capabilities of the spare lines of the PC's parallel data port. These signal lines are capable of supplying enough current to power the smart card reader without need for an external power supply *(see the figure)*.

As an additional benefit, the software listing provided in the original article may be used without modification, due to the fact that the unused five data lines of the PC's parallel port are set high by default in the original program. These signal lines, when parallel-connected using the five general-purpose diodes, as shown, will allow the internal V_{cc} supply of the PC printer port logic to also power the smart card being read.



This simple PC Smart Card Reader, which contains a power supply that is completely derived from the PC parallel port's spare signal lines.

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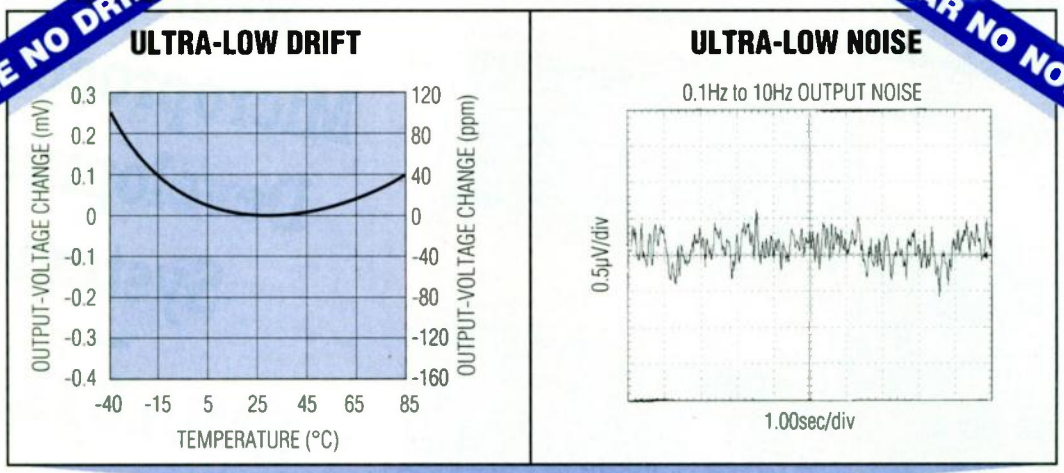

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MAX6241A	4.096	1.0/2.0	±0.025	4.0	Yes	4.65
MAX6250A	5.0	1.0/2.0	±0.02	5.0	Yes	4.65
MAX6225B	2.5	2.5/5.0	±0.1	2.8	Yes	2.25
MAX6241B	4.096	2.5/5.0	±0.1	4.0	Yes	2.25
MAX6250B	5.0	2.5/5.0	±0.1	5.0	Yes	2.25

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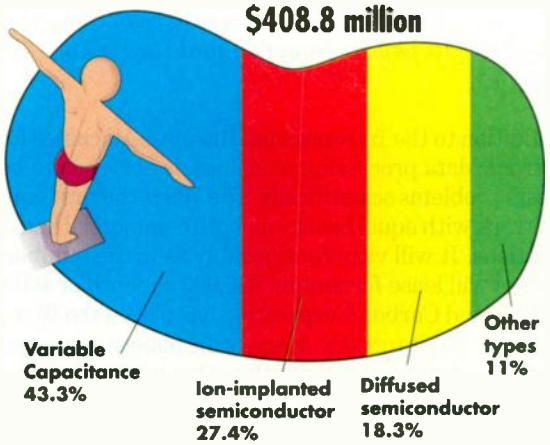
ELECTRONIC DESIGN
QUICK LOOK
Edited by Mike Sciannamea and Debra Schiff

MARKET FACTS

Under Pressure To Perform

Used in all kinds of applications from blood pressure monitoring systems to plastic extruders, process pressure transmitters were a $353 million market in 1995. According to "The U.S. Pressure Transducer, Transmitter, and Component-Level Sensor Industry: Seventh Edition," a recent study released from Venture Development Corporation, long-standing solid state pressure sensor suppliers and nonprocess pressure transducer manufacturers are now targeting segments of the process pressure transmitter market. There are three types of process pressure transmitters: low-cost/nonrepairable, smart, and traditional. The low-cost/nonrepairable units produce analog output signals and are known in the industry as "throwaways." Traditional process pressure transmitters also produce analog output signals, but unlike the throwaways, they can change pressure ranges, and are generally repairable. The smart units transmit digital signals, and are capable of remote ranging and calibration. According to the study, in 1995, traditional pressure transmitters typically ran about $835 a piece, while the low-cost unit was priced around $437 a piece. The market was divided in 1995, with 59.3% of the process pressure transmitters shipped in the U.S. being smart units. Traditional types made up 32.4% of the market, with low-cost transmitters trailing at 8.3%. The study found that process pressure transmitter suppliers who asked their customers which type of unit they preferred, were told that the low-cost units were not considered cost effective. The customers preferred the more flexible and repairable units. As is the case with most electronic devices these days, the size of the traditional process transmitter is shrinking. Historically, process pressure transmitters needed to be big enough to handle the amplification circuitry and signal conditioning required to send a high level analog or digital output signal over a long distance. Now, due to solid state piezoresistive pressure sensor design advances, inexpensive, small devices carry that circuitry and compensation on the same silicon chip as the sensor. As a result of these new designs, monolithic semiconductor pressure sensor manufacturers can market their low-cost packages as a cost-effective throwaway. The resulting trend is the rise of very inexpensive monolithic semiconductor units, replacing the traditional low-cost process transmitter. The 1995 tally for U.S. consumption of electronic pressure transmitters, transducers, and sensors was $1.08 billion. That figure was an increase of 42% over the last four years. The market includes component-level solid state pressure sensors, non-process pressure transducers, and process pressure transmitters. In the nonprocess pressure transducer market, the U.S. spent $690.5 million, in 1995. Driving the market, on-board automotive applications fueled 30% of that figure. Typical automotive applications include: manifold air pressure sensors (to control fuel-injected engines), air conditioning systems, advanced power steering systems, and oil pressure gauges. The rest of the market comprises commercial aviation, aerospace, and military applications clocking in at 21%, and the medical arts at 15%. In chip-level component sales, pressure sensors totalled $35.9 million, in the U.S., in 1995. Blood pressure monitoring systems were the largest application for these solid state piezoresistive units. Another big market for the chip-level sensors is the on-board automotive market.

Forecasted Share of U.S. Consumption of Process Pressure Transmitters



Source: Venture Development Corporation

For more information, contact Venture Development Corporation, One Apple Hill, Natick, MA 01760; (508) 653-9000; fax (508) 653-9836; e-mail: info@vdc-corp.com.—*DS*

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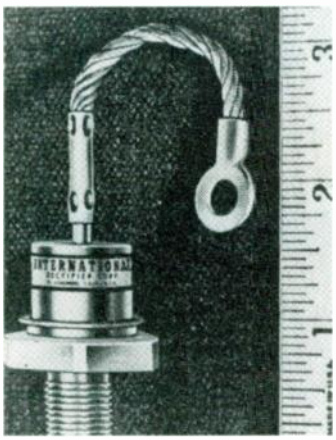

A series of silicon diodes in the 14 to 70 (half wave) amp rating have been made available for such industrial uses as motor loads, welders and battery chargers, and for dc power supplies in aircraft and missiles, and on ships. Six of these diodes assembled on heat sinks and connected in a three-phase bridge can supply 13 kw at 175 v dc with natural cooling or 33 kw at 175 v dc with forced draft cooling. The diodes are available for peak inverse voltages from 50 to 300 v. They are miniaturized, and hermetically sealed. International Rectifier Corp., Dept. ED, 1521 E. Grand Ave., El Segundo, Calif. *(Electronic Design, Feb. 1, 1957, p. 73)*

International Rectifier is now celebrating its 50th anniversary. Founder Eric Lidow is a classic American success story: He came to the U.S. from Germany in 1937 with only an EE degree from the University of Berlin and a camera—but almost immediately, he sold the camera to fund his first enterprise: Building and selling 42 radios made from spare parts. In 1940, he founded Selenium Corp. of America and developed special selenium rectifiers for military applications. He sold the company in 1945 to Sperry Corp. and then founded IR in 1947. IR was a pioneer in developing silicon rectifiers like the one shown here, but the company is perhaps better known for its power MOSFETs, which were developed by Eric's son, Alex, who has a PhD in solid-state physics from Stanford University.—SS

Now Up to 709

The IBM 709, the latest addition to the International Business Machines Corporation's 700 series of electronic data processing machines, is designed to help business management solve its problems scientifically. The 709 is the first equipment of its capacity that can work with equal facility on both commercial and scientific or engineering calculations. It will vary considerably as to the number of units used, but a typical system will lease for around $56,000 a month or sell for about $3,000,000. Union Carbide and Carbon Corporation has placed the first order for a 709 system. They plan to put it to work on scientific management problems such as sales forecasting and optimum distribution. One interesting application is to use the 709 to pinpoint the best possible location for a new plant. *(Electronic Design, Feb. 15, 1957, p. 6).*

The 709 was the last of IBM's vacuum-tube 700-series computers. A year later, the company introduced the first of its transistor-based mainframes, the giant 7090.—SS

Coasting-time Computer

A coasting-time computer will control the injection of the Vanguard satellite into its orbit around the Earth at precisely the right moment. Developed by Air Associates, Inc., Teterboro, N.J., the computer will gather flight data up through the second stage's thrust period and will compute the correct coasting time between the end of this thrust period and the jettisoning of the second stage and firing of the third stage. It also was announced that the first computer, after exhaustive tests have been performed, will be delivered to the Martin Company next month. *(Electronic Design, Feb. 15, 1957, p. 8).*

As mentioned in the last issue, the Vanguard satellite was launched into orbit on March 17, 1958, presumably with this computer on board. Air Associates began manufacturing aircraft hydraulic and pneumatic equipment at Teterboro Airport in the early 1940s. The company later became the largest manufacturer of aircraft seat belts but closed its doors in the 1970s. (Teterboro also is home to Allied Signal Aerospace, formerly Bendix.)—SS

Hello? It's The Internet Calling

Introduced at Fall Internet World this past December, CompuNet 2000 is a PC keyboard telephone with Internet capabilities. Used with Internet Phone, or any other Internet telephony software, CompuNet 2000 provides a different way of making long-distance calls that cost as much as a local call.

The device looks and functions like a PC keyboard, and features inputs for a headset and phone line. CompuNET 2000 eliminates the need for speakers and microphones in making calls through the Internet.

Users dial out with the numeric keypad or CompuNET Autodial software. Provided in both DOS and Windows versions, the autodialer dials any number listed in either card files or hot keys (in Windows), or off the screen from a virtual phone directory (in DOS). An on-line phone log lists incoming and outgoing calls.

When activating the phone feature of the keyboard, users need only press the Phone key. A coordinated LED lights up, turning the numeric keypad into a telephone keypad. To answer or hang up, the user presses the Line key, thus illuminating the Line LED.

Call Waiting is activated by pressing the Flash key. A Mute key allows for privacy in noisy environments.

Contact Integrated Technology USA Inc., 545 Cedar Ln., Teaneck, NJ 07666; (201) 907-0200; fax (201) 907-0344; Internet: http://www.ITI2000.com.—*DS*

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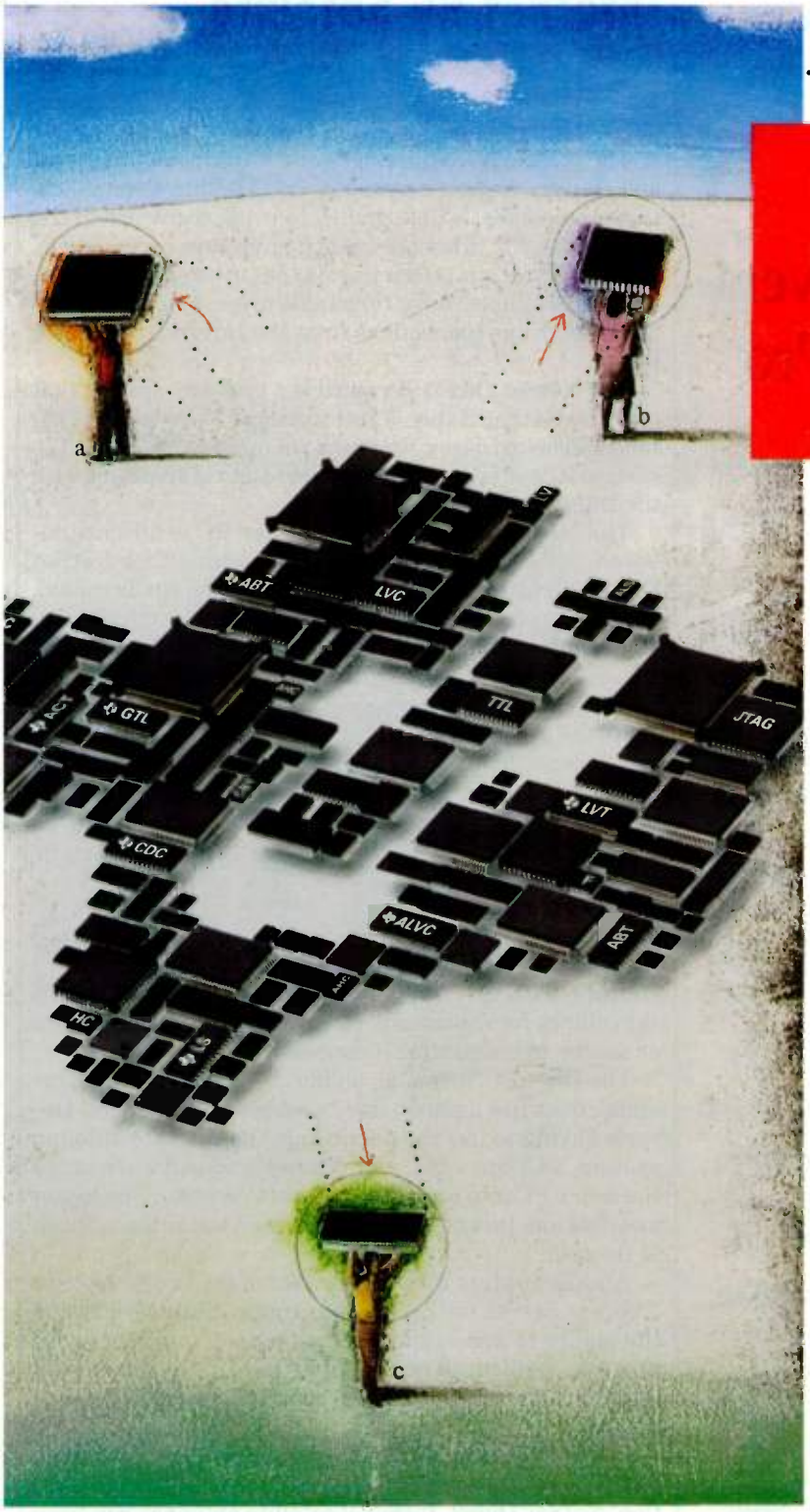

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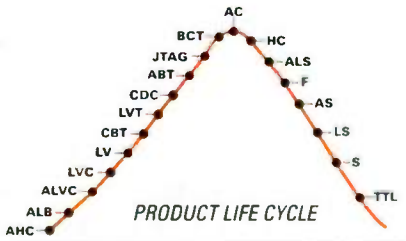

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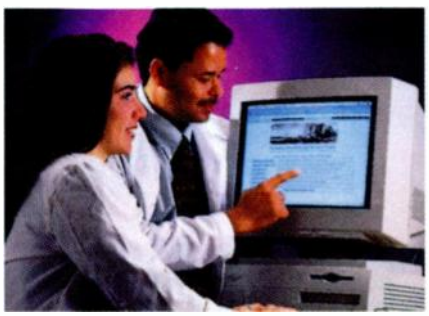
Internet By Satellite

If someone asked, "What words would you equate with speedy?" would "satellite" be one of them? NetSat Express is setting out to change that perception.

The strategic alliance between Worldcomm Systems and Hughes Network Systems, two satellite communications companies, is determined to bring the world of the Internet to any interested party, anywhere on the globe. NetSat Express is offering two types of satellite Internet access terminals. Both terminals are capable of giving users 400 Kbps connections from the Internet to a PC or LAN.

The NetSat Direct Terminal is a two-way system that uses the NetSat Express International Network to bring the Internet to users. The most unique feature about the system is that is doesn't need phone lines to connect with the Internet.

The NetSat Express Single User PC is a Pentium-based, preconfigured unit that runs with either NetSat Direct Terminal or DirecPC Satellite/Dial-up Terminal. NetSat Express also offers customized interactive multimedia solutions for a variety of different areas, such as computer-based training, distance learning, and telemedicine.



As far as security is concerned, NetSat Express bypasses the terrestrial-bound Internet service providers by using dedicated SCPC satellite circuits. This design allows for continuous two-way, high-speed Internet or secure, private intranet connections.

The DirecPC Terminal, unlike the NetSat Direct Terminal, does use a phone line to access the Internet. Despite having to use the phone link, the satellite antenna system, ISA bus card, and Windows 95 software make the user's PC into a satellite Internet receiver. The asymmetrical link brings the 400 Kbps from the Internet back to the user.

Another option for enterprises might be the NetSat Express Server for LAN workgroups. Many users have the ability to access the internet with one satellite connection. Dedicated connections provide symmetrical links to the Internet at rates from 64 Kbps to 2 Mbps, or higher.

DirecPC Terminal satellite antennas typically range from 66 centimeters to 1.8 meters, depending on the location. NetSat Direct Terminal satellite antennas run from 1.2 to 2.4 meters, also depending on location.

The DirecPC is priced at $1375, without the Universal Antenna Mount and Wingate software. NetSat Direct is priced at $8990. NetSat offers several service options, including a corporate package and a surfer's bundle.

For more information, contact NetSat Express Inc., 400 Oser Ave., Suite 300, Hauppauge, NY 11788; (516) 231-4422; fax (516) 231-9223; Internet: http://www.netsatx.com.—*DS*

Make A Decision

The newest version of Commander Decision, 1.2 now allows users to create dynamic decision support applications. The desktop-decision-support system also is now Web-enabled to provide users a new way of handling Internet information.

Commander Decision, along with the client software, Decision Desktop, was designed to inspire decision makers to think differently, to try alternative courses of action, and to monitor company progress. Specifically, Decision Desktop is targeted to developers designing highly-functional applications that don't need a great deal of maintenance.

Typical applications that can be produced using Decision Desktop are budgeting, executive information systems with key performance indicator monitoring, financial reporting and analysis, product and customer profitability analysis, sales and margin planning, and sales and marketing planning.

Maintaining an easy-to-use posture, the application building environment of Decision Desktop is mostly script-free. The system supports Arbor Software's Essbase databases and structures, eliminating scripting hassles for applications built around Essbase databases.

If a user does need to write some scripts, Decision Desktop features a Visual Basic for Applications language. The convenience of having Visual Basic for Applications within the system saves enterprises the time and money costs of sending individual developers to training for proprietary scripting tools.

On the end-user side, Decision Desktop provides graphic interfaces for business intelligence. There are charts, integrated mapping systems, color-coded exception reporting, and ad hoc queries and calculations.

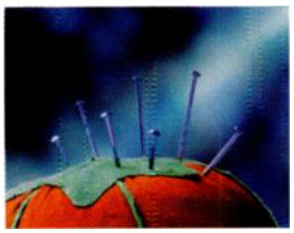
The Detect and Alert technology lets users identify data to be monitored, by entering their acceptable data ranges. The Private Monitor function of Detect and Alert then notifies users when values have appeared outside of the specified ranges. This feature provides quality control on the management side.

Another useful feature is the Intelligent Component Expansion (ICE). ICE shows users problems that have been hidden at lower levels of the hierarchy that they may not be viewing at that moment.

The Commander Decision client/server software has been written with Visual C++ and the Microsoft Foundation Class libraries. Decision Desktop is compatible with Windows 3.1, NT 3.51, and 95. The 32-bit software business tool uses OLE2 and OCXs to power the major visible objects.

The server, Decision Access Module is capable of multitasking, and is multithreaded.

For more information, contact Comshare Inc., 555 Briarwood Circle, Ann Arbor, MI 48108; (313) 994-4800; fax (313) 213-2161; Internet: http://www.comshare.com/home2.htm. —*DS*



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Such a micro size may seem impossible, but not to Toko engineers. The LL1005 (inductance range 1.0 to 27.0 nH) is merely the latest addition to Toko's micro-miniature line of ceramic multilayer chip inductors available from Penstock. With an 0402 footprint and an 0.05 profile, *the LL1005 is the world's smallest*–by far.

Toko's cutting edge design and leadership in ceramic multilayer technology helps in other ways, too. Toko chip inductors offer higher current handling capabilities (up to 1 amp) and tolerance as low as 3% on some values. Plus:

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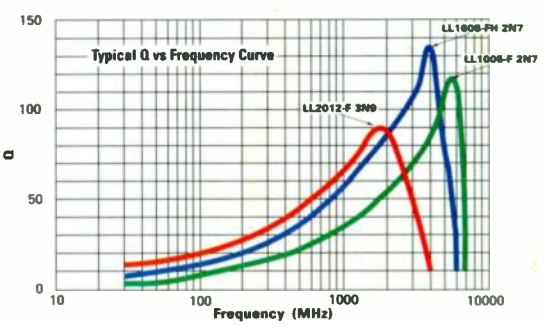
As the world's largest RF/microwave distributor, Penstock is the design engineer's link to Toko's advanced technology. We inventory more than 5 million Toko parts –*in stock*– and serve the engineering community from over 25 sales offices throughout North America and Europe. With **Toko** and **Penstock**, you always know, there's nothing more advanced–or more readily available– anywhere in the world.



Toko LL Prototyping Kits Available

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In Northern California call: 1-408-745-8190
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READER SERVICE 196

Blending Western Ideas Into Eastern Operations

Call it another version of "East meets West." Or, you may wish to refer to it as "East goes West to bring new ideas back East." No matter what name you desire to give it, a new master's degree in business administration (MBA) program has been recently developed to help Chinese scientists and engineers step into management positions with American technological companies in China.

A number of engineers, chemists, physicists, and other technologically-trained Chinese men and women are now enrolled in a program at Rensselear Polytechnic Institute's (RPI) Lally School of Management and Technology. It is the first American MBA program that has the official approval of the Chinese government. Students range in age from 25 to 55 years old.

It is hoped by the administrators that upon completion of the program, the students will then be vigorously recruited by Western companies that have divisions in China. The program aims to help Chinese students "understand American markets, the American consumer, the American culture, American technology, and the American language," says William Mow, founder and CEO of Bugle Boy Industries and an RPI graduate.

The MBA program is a joint effort between RPI and Zhejiang University in Hangzhou, China, and has been designed to address the growing needs of American companies with major operations in China. Program developers said that most companies they worked with in China reported significant voids management talent. Joseph Morone, dean of the Lally School, says that the program will attempt to help companies in China find educated and experienced managers to staff their operations. "It is prohibitively expensive for American companies to send their managers abroad to manage operations in China, and many managers are unwilling to leave family and friends to work there," says Morone.

Specifically, the 24 students that already have been enrolled in the program will spend roughly 12 months at RPI, three months as interns with American companies, and four months in additional graduate study at Zhejiang University. Those who successfully complete the program and receive the new MBA will graduate with full credentials from both universities.

In addition, a number of companies have agreed to sponsor three-month American internships for the Chinese students. Among them are Motorola, Mobil, Albany International, and Bugle Boy.

For more information on the MBA program, contact Shubo Xu, program director, RPI, Lally School of Management and Technology, 110 8th St., Troy, NY 12180; (518) 276-2388; Internet: http://www.rpi.edu.—*MS*

INTERNET NEWS

Serving up pizzas via the Internet, CyberSlice (http://www.cyberslice.com), has been using NeXT's WebObjects graphical interface to design their site. The on-line pizza delivery service uses MapQuest geographical information systems in conjunction with APEX telephony software to connect hungry site visitors to menus from restaurants in their localities.

Pizzerias that are registered with CyberSlice are contacted in real-time when an order is placed. The WebObjects software ensures that the restaurants are open and willing to deliver, or have patrons pick up their pies (or other meals, depending on the menu).

When an order has been placed at the slice site, WebObjects sends an interactive voice response to the pizzeria. Then, the order is accepted, sending message back to the customer that their meal is on the way.

As part of the service offered to the restaurants, CyberSlice offers free web pages and menu storage for participating pizza providers. The company will even help design pages.

Not all markets are supported by CyberSlice, but Boston, New York, San Francisco, and Seattle metropolitan areas are covered by over 1000 pizzerias on the service, with more markets to come.

For more information, contact NeXT Software Inc., 900 Chesapeake Dr., Redwood City, CA 94063; (415) 780-3731; Internet: http://www.next.com.

Eliminating the need for TCP/IP stacks, WebRamp's IPX Gateway combines the functions of ISDN T/A, IPX-to-IP gateway, and a LAN hub within a single unit.

WebRamp packages their Internet-access device with a Windows-based configuration utility, WebRampWiz. The point-and-click application accommodates novice and experienced users in installing, configuring, monitoring, and managing ISDN and ISP parameters.

Giving the client access to the Internet and NetWare simultaneously, the IPX Gateway translates IPX/SPX to IP transparently. The gateway provides high-speed (64 to 128 Kbps over ISDN) shared access to the Internet while cooperating with NetWare on LANs.

The WebRamp features eight 10Base-T Ethernet ports (including one MDI port) and one AUI Ethernet port for LAN interfacing. For WAN interfacing, WebRamp uses one ISDN BRI interface with built-in NT1 (U interface).

Marketed as a complete turnkey solution, WebRamp comprises all the hardware and software required to connect network PCs and Macintoshes to an ISDN line, and connect to an Internet service provider. The Client Software Bundle contains both Netscape Navigator and Microsoft Internet Explorer. WebRamp packages start at $849.

For more information, contact Trancell Systems Inc., 3180 De La Cruz Blvd., Suite 200, Santa Clara, CA 95054; (408) 988-5353, fax (408) 988-6363; Internet: http://www.trancell.com.

Recent testing in 87 area codes across the U.S. has shown that Internet information can be downloaded at nearly twice the speed of current connections.

U.S. Robotics placed approximately 20,000 V.34 calls with diagnostic software that found that the majority of the test calls have only one analog-to-digital (AD) conversion in the path. Having one AD conversion is necessary to connect at the higher speeds supported by U.S. Robotics new x2 technology. Calls made with more than one AD conversion sent the connect speeds spiraling down to 28.8K/33.6K.

Upgrades to the x2 technology are as simple as a software upgrade, in most cases. Converting a Total Control digital modem, NETServer I-modem, or MP I-modem requires a software download. The company is calling modems with digital connections to public switched telephone networks "x2 server modems." Courier V.Everything analog modems that are upgraded by a software download will now be called "x2 client modems." Some Sportster models need memory chip upgrades to become x2 compatible.

In a client/server application, an x2 server sends data over the telephone network, eight bits at a time, at the same rate as the network (8000 Hz). If all things were equal, and the x2 client modem could recover 8000 PCM codes per second, then the modem would be capable of downloading at 64 Kbps. Unfortunately, noise floors complicate transmissions, slowing down the process.

In the transmitting of digital information across telephone networks, the digits that are sent are reconstructed at the other end, mimicking the original analog waveform. Since the waveform has been quantized, and is not exactly the same as the analog waveform sent across the network, the result is quantization noise. This noise slows down the communication channel to approximately 35 Kbps.

The advantage of x2 is that it works on a digital-to-analog conversion, rather than the analog-to-digital conversion which is affected by the quantization noise.

Currently U.S. Robotics is meeting with Federal Communications Commission officials to certify the x2 lines and begin rapid transmission.

For more information, contact U.S. Robotics, P.O. Box 16020, 605 North 5600 W., Salt Lake City, UT 84116; (800) 527-8677; fax (801) 320-7000; Internet: http://www.usr.com.

Integrated Telephony Products Inc., recently announced new World Wide Web extensions for its flagship Enhanced Services Platform, the ESP product line.

The first product of the ESP line to be shipped is the Web Callback trigger mechanism. Web Callback allows anyone with World Wide Web access to easily activate a callback service with just a click of the mouse. Callers also can instantly see the rates they will be billed before a call is placed.

For more information, contact Integrated Telephony Products Inc., 1069 East Bethany Dr., #900, Aurora, CO 80014; (303) 338-1000; fax (303) 338-1345; Internet: http://www.Itp-Cti.com.

FLIPPING THROUGH THE INTERNET ROLODEX

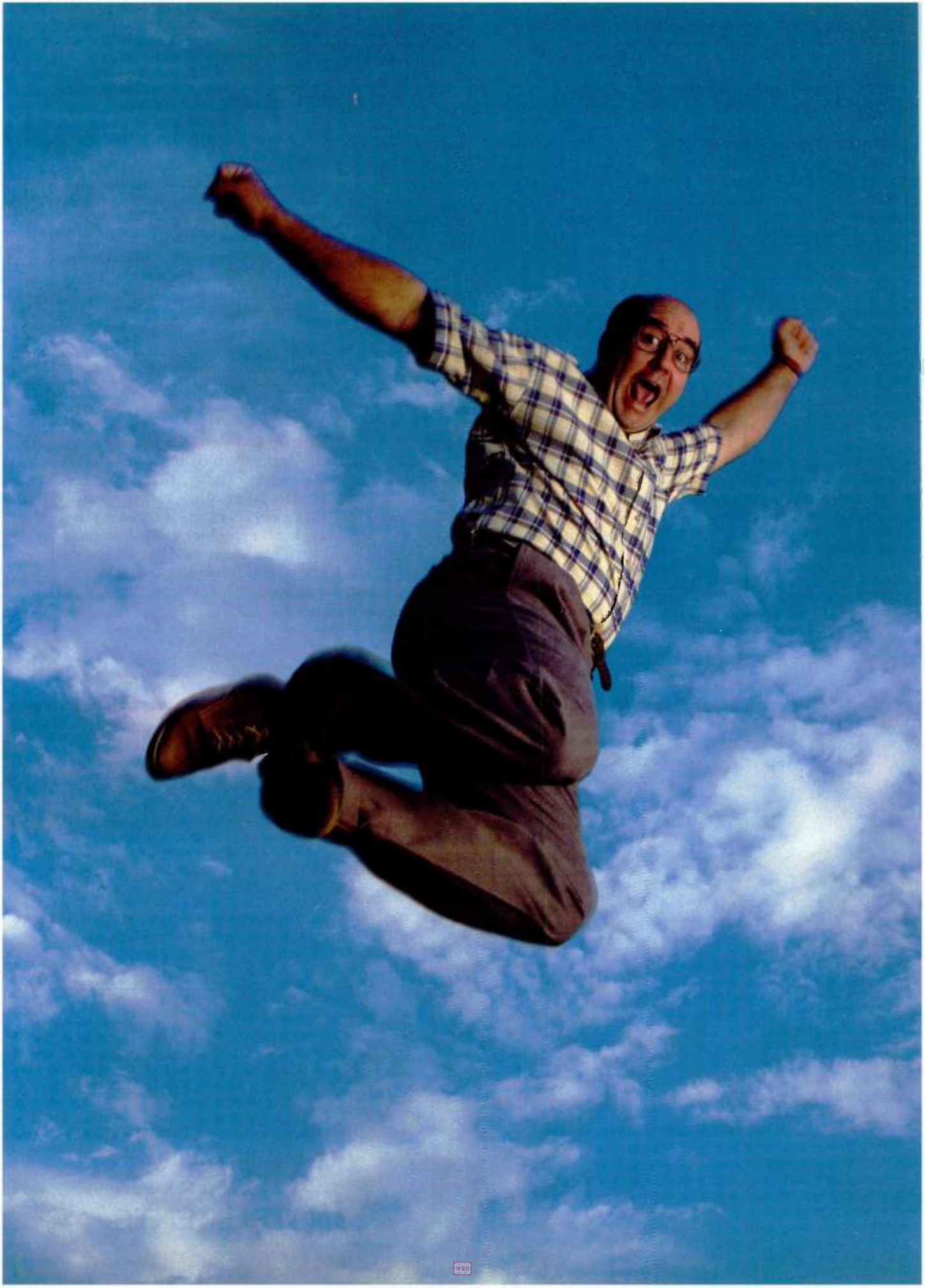
http://www.statpower.com: Visitors to this site will be able to view what Statpower Technologies has to offer from their line of battery inverters and chargers. Each product is presented complete with descriptions, specifications, and photographs. Also included on the site is an e-mail link to the company. Additionally, site visitors will find a section dedicated to the most-frequently asked questions about inverters and chargers.

http://www.stlabs.com: Stop into the Testers' Network at ST Laboratories' site. This URL features a monthly e-zine with white papers and articles contributed by testers. There also are plenty of links to valuable resources and related organizations. Equally interesting is a test documentation file archive, as well as product reviews, and an events calendar. Software testers and quality assurance/quality control professionals also will find a useful "ask a tester" resource here.

http://www.olflex.com: Enter this URL to find comprehensive information about flexible cables and accessories. Olflex supplies visitors with uses for their products in a variety of OEM and MRO automation/industrial manufacturing situations. There are web pages concerned with oil-resistant control cable, continuous-flex control cable, European-approved cable, conductors, conduit, and cable track. Potential customers interested in custom-designed cable will find Olflex's request form in the Feedback section of the site.

http://www.ICSPAT.com: In search of information relating to signal processing? Try dropping into the virtual conference modeled after the International Conference on Signal Processing Applications and Technology (ICSPAT). The site was designed to provide an interactive source for attendees who were too tied to the conference schedule to interact with authors. All of the white papers from the conference held October 7-10, 1996 are featured at the site. Audio files featuring speakers at the conference also are available. Additionally, industry news, guest columnists, interviews, a chat forum, future conference dates, and speaking opportunities can be found at the ICSPAT Online homepage.

http://www.balluff.com: Take the next exit to Balluff's site, to find the lastest catalog, distributor, and product information. Visitors can use the on-line literature request to solve application problems. The company also plans to have application sheets and technical data sheets in CAD format, ready for download.



RISC performance without scrapping code. And you thought engineers were a low-key bunch.

Engineers haven't been exactly giddy about moving from CISC to RISC. Rewriting code, blowing a ton on memory to support it, and delaying time to market. ColdFire™ technology from Motorola offers an exciting alternative. The cost-effective ColdFire architecture is derived from Motorola's 68K microprocessor family, and is supported by industry-leading development tools. So you can build on current product designs and programming experience to get to market faster, with a smaller investment. Plus, the ColdFire microprocessor's variable-length RISC instruction set maximizes code density, thereby reducing the amount of costly memory required to store it. All of which delivers a new level of price/performance for cost-sensitive applications. For more information on ColdFire microprocessors, call your Motorola representative at 1-800-521-6274 (ref. #HP002). Or visit www.mot.com/coldfire. You'll see a dramatic difference.

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READER SERVICE 151

YOU CAN MAKE AN *impact* ON A PRODUCT OR YOU CAN MAKE AN IMPACT ON THE WORLD.

There are those who are content designing products to move the world. And then, there are the others. The ones determined to rattle the orb, hellbent on writing a portion of their generation's history.

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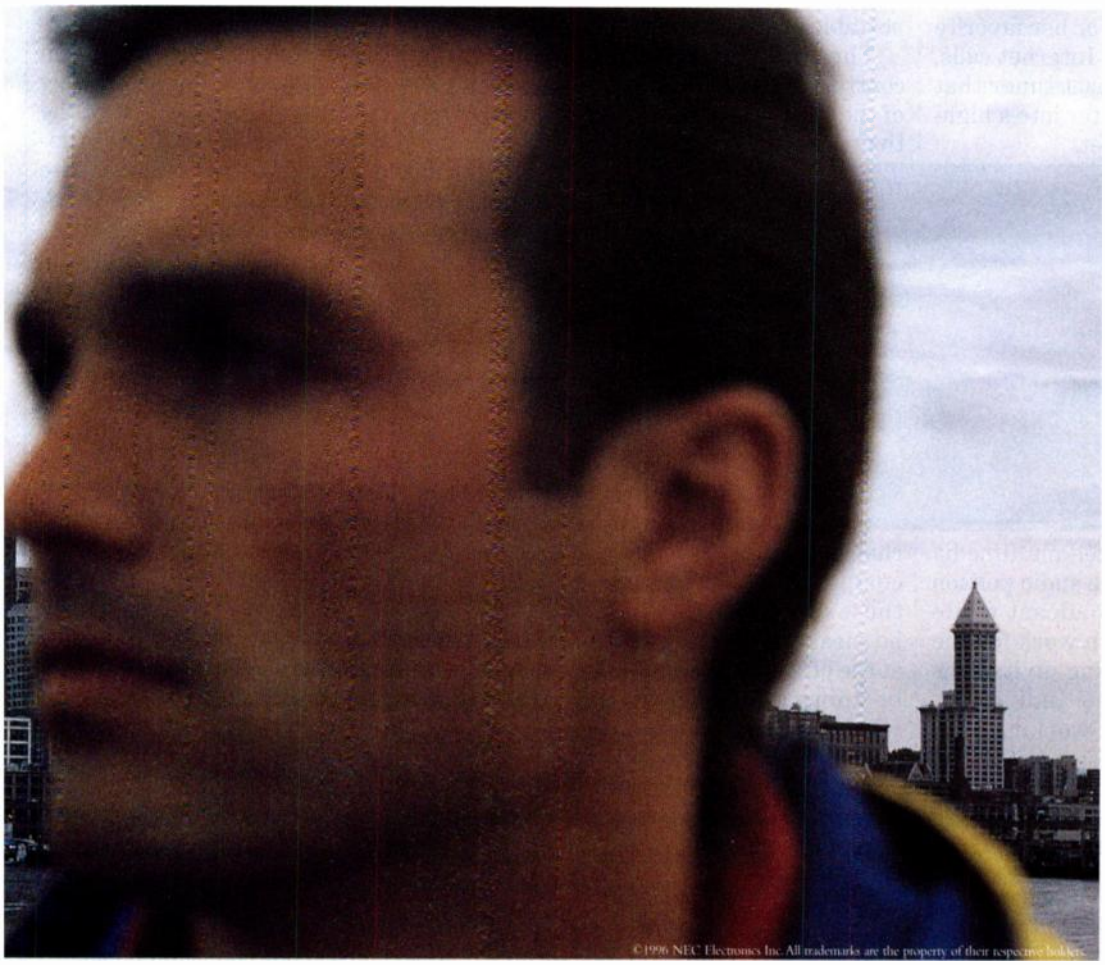
With NEC's MIPS architecture, the future is assured without having to discard the past. It enables forward compatibility. Plus, it's extremely scalable and uses common code libraries. In other words, our clearly defined migration path gives you a connection to next generation processors and backward compatibility.



V_R5000. *Paramount performance, incredibly affordable. This is the ultimate embedded processor for advanced applications like internetworking.*

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When you think about it, you are not just a product designer. Part visionary, part interpreter of dreams, your mission is to reinvent and redefine the way the world works. Well, we can help make that happen a little faster. NEC offers a comprehensive solution, including support for PCI Bus interface and laser printer control peripherals. We even provide companion chipsets as well as the third-party tools.

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	V_R4100	PPC403GA	V_R4300	PPC603	V_R5000	PPC604
Frequency	40MHz	25MHz	133MHz	80MHz	200MHz	100MHz
Bus Interface	32-bit	8/32/64-bit	32/64-bit	32/64-bit	64-bit	64-bit
I-Cache Size **D-Cache Size**	2KB 1KB	2KB 1KB	16KB 8KB	8KB 8KB	32KB 32KB	16KB 16KB
Pin Count/Package	100 PQFP	160 CQFP	120 PQFP	240 CQFP 256 BGA	272 BGA 223 CPGA	304 CQFP 256 BGA
SPECint92/SPECfp92	45 VAX MIPS	---	80/60	75/85	---	128/120
SPECint95/SPECfp95	---	---	---	---	5.5/5.5	---

NEC

READER SERVICE 155

With TV At Their Fingertips, Desktop Jockeys Will Never Leave Their Monitors

Further chaining professionals to their desks is the Proview TV Box from Proview Technology Inc. Catering to the 'net junkie who can't bear missing his or her favorite TV show because the Internet calls, the TV Box is a compact tuner that converts any PC monitor into a high-resolution television set.

Users with optimized multimedia setups can listen to the audio portion of the television broadcast while they're catching up on work for the office or even designing invitations to an upcoming soireé. Individuals with tools capable of working with audio or video feeds also may find the tuner useful.

A kajillion channels and nothing on—this situation now goes for the PC user. Functioning much like "regular" television, Proview TV Box allows the user to access 181 television channels. There's also a 23-key handheld remote control unit.

The dimensions of the tuner are 5.2-in. wide by 6.5-in. long by 1.0-in. high, nearly one-third the size of other currently-available TV tuner boxes.

Television functions such as Power, Channel Selection, and Volume can be controlled via the remote control, or by pushing the corresponding buttons located on the front panel of the Proview TV Box. The Proview TV Box does not require any software to run, and is compatible with any operating system designed for IBM PC or comparable computer.

Allowing for more multimedia options, the Proview tuner can be connected to a number of external pieces of equipment, such as camcorders, video cassette recorders, laser disk players, and video game systems. Additionally, the tuner may be plugged into a viewcam for a portable entertainment solution.

The Proview TV Box's remote control device can control the power of the PC, keeping the monitor on so that the user can continue his or her television viewing. It also allows users to choose between television, external video sources, and normal PC operation.

Although most multimedia mavens have their own set of high-performance speakers, the Proview TV Box comes with its own built-in mini-speaker. But, for selective audio listeners with a trained ear, the tuner company also included an outlet to connect to a more complex speaker system. And, for those professionals who just might be sneaking a peek at the game while at the office, or those kids who should be doing their homework, but are watching The Simpsons, there's also an outlet for headphones.

All of the control functions of the tuner can be displayed on screen, and adjusted using the function key on the remote.

Just for the channel surfers, Proview included full-channel autoscanning. This feature allows "clicker" hounds to automatically skip to available channels when surfing up or down the band.

The Proview TV Box also is closed -caption enabled to accomodate the hearing impaired.

Another option for the space-conscious individual is the Proview TV Card. The card fits into any IBM PC/compatible, 8-bit/16-bit ISA slot. A unique feature of the card is that it can be operated by a hand-held, wireless remote.

The Proview TV Box is priced at $119, and the Proview TV card is priced at $109.

For more information, contact Proview Technology Inc., 122272 Monarch St., Garden Grove, CA 92841; (714) 379-4455; fax (714) 379-3308; e-mail: pr@fbiz.com. —DS

OFF THE SHELF

The third edition of *"Microchip Fabrication—A Practical Guide to Semiconductor Processing"* is now available. The book familiarizes readers new to the semiconductor industry with the process for manufacturing integrated circuits. This new version provides information on new processes as well as the basics of the established processes. Topics discussed include an overview of the semiconductor industry, wafer fabrication, process yields, and packaging. The 623-page book is priced at $60. For more information, contact Semiconductor Services, 735 Hillcrest Way, Redwood City, CA 94062; (415) 369-7890; fax (415) 367-1062.

"3D Design Graphics: How to Create Real-Time 3D Models for Games and Virtual Reality" shows readers how to create sophisticated real-time 3D graphics for computer games and virtual reality. The book teaches readers how to design 3D artwork optimized for real-time, master industry-standard tools such as 3D Studio and Photoshop, and create graphics for different platforms. The book also features an accompanying CD-ROM containing a collection of 3D objects and textures that can be used immediately. The 383-page book is priced at $39.95. Contact John Wiley & Sons Inc., 605 Third Ave., New York, NY 10158-0012; (800) 225-5945; Internet: http://www.wiley.com/compbooks.

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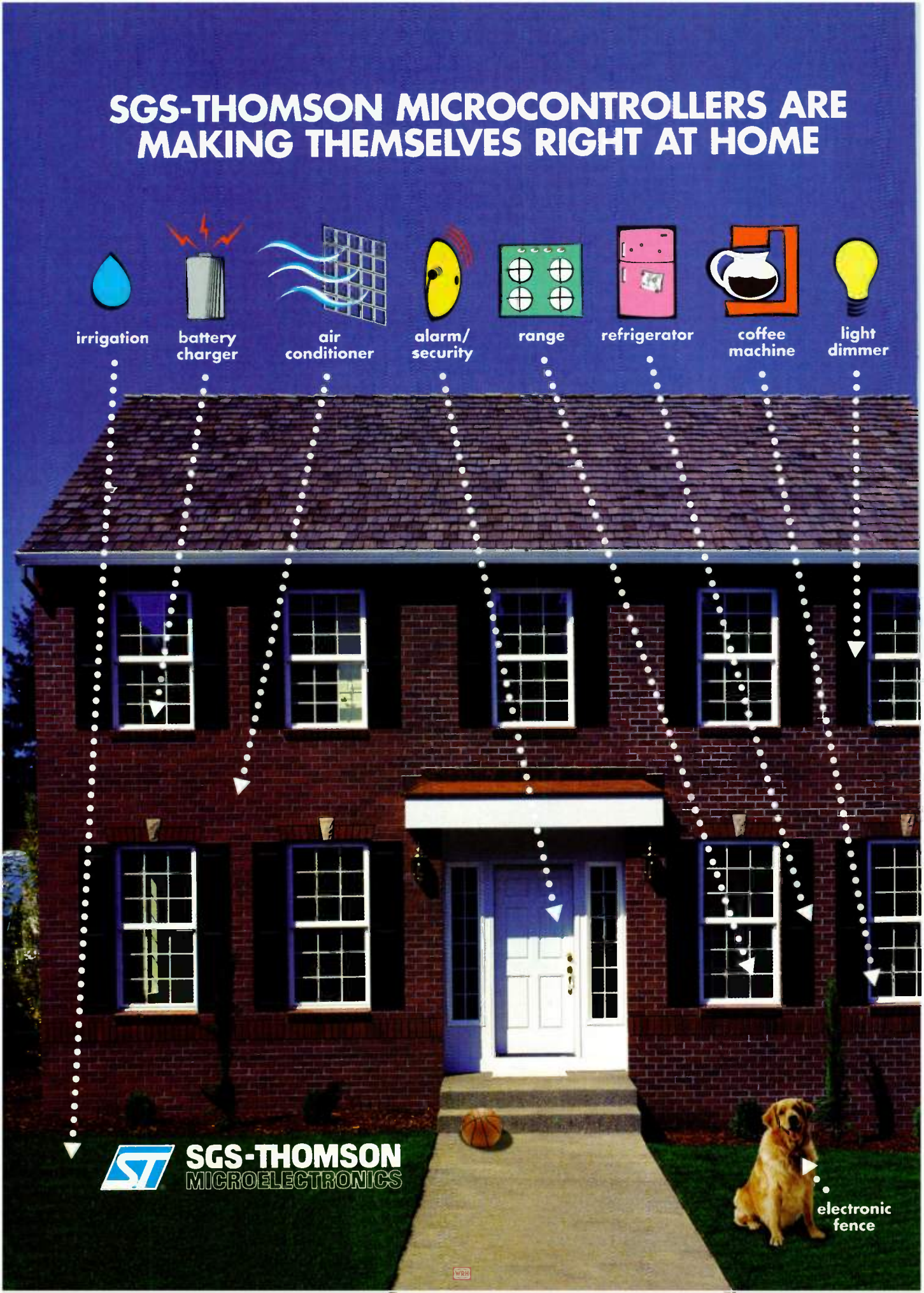


LET OUR MICROS MAKE YOUR PRODUCT A HOUSEHOLD WORD

The reason SGS-THOMSON's 8-bit ST62 family of MCUs is making itself at home in so many household appliances can be summed up in one word: *Value.* ST62 devices deliver more performance in less space for less money. Even the core is optimized for cost-effective operation. Add ESD protection and unmatched noise immunity and you begin to understand why the ST62 is opening doors to consumer applications that remain closed to ordinary MCUs.

Additional ST62 MCU Applications

- washing machine
- power tool
- heater
- UPS
- thermostat
- scale
- programmable timer
- vacuum cleaner
- home bus

All ST62s contain ROM, RAM, an 8-bit timer with 7-bit programmable prescaler and multifunctional individually programmable I/O ports. Also available: Devices with high-current buffers to directly drive LEDs or TRIACs, along with a wide range of peripherals such as PWM and LCD drivers. A wide operating voltage range and robust design allow ST62 microprocessors to be powered directly from a battery or the main with minimum external components.

In addition to the extensive ST62 family, SGS-THOMSON offers other 8-32 bit micro solutions such as ST7, ST9, ST10 and ST20 families. All of these products are fully supported with extensive development tools including C compilers for most families. So why not let our micros help make your product a household word. To find out more fax 617-259-9442, write SGS-THOMSON, 55 Old Bedford Road, Lincoln, MA 01773, or e-mail: info@stm.com. And visit our web site at **http://www.st.com**

ST6
The 8-bit MCUs of choice in automotive and industrial as well as consumer applications. Instruction set and addressing modes maximize code efficiency.

ST7
Powerful industry standard 8-bit core, surrounded by numerous advanced peripherals. 3K to 48K of ROM with different RAM sizes. Choose EPROM and OTP versions for proto-typing. On-chip EEPROM is also available for integrated data storage.

ST9
8/16-bit micro family fills requirements of most advanced computer, consumer, telecom, industrial and automotive applications.

Service and Technology

For More Info Turn Page

OUR 8-BIT MICROS ARE BECOMING HOUSEHOLD WORDS

	DEVICE	PROGRAM MEMORY	RAM	EEPROM	A/D INPUTS	TIMERS	SERIAL INTERFACE	I/O's	PACKAGE	OTHER FEATURES
*	ST6200	1K ROM	64		4x8-Bit	1x8-Bit		9	DIP/SO16	
*	ST6201	2K ROM	64		4x8-Bit	1x8-Bit		9	DIP/SO16	
*	ST6203	1K ROM	64			1x8-Bit		9	DIP/SO16	
*	ST6208	1K ROM	64			1x8-Bit		12	DIP20/SO20	
*	ST6209	1K ROM	64		4x8-Bit	1x8-Bit		12	DIP20/SO20	LED or TRIAC driver
*	ST6210	2K ROM	64		8x8-Bit	1x8-Bit		12	DIP20/SO20	
*	ST6215	2K ROM	64		16x8-Bit	1x8-Bit		20	DIP28/SO28	
*	ST6220	4K ROM	64		8x8-Bit	1x8-Bit		12	DIP20/SO20	
*	ST6225	4K ROM	64		16x8-Bit	1x8-Bit		20	DIP28/SO28	
	ST6240	8K ROM	216	128	12x8-Bit	2x8-Bit	SPI	16	QFP80	LCD driver (segment) + LED or TRIAC driver, 32KHz oscillator
	ST6242	8K ROM	152		6x8-Bit	1x8-Bit	SPI	10	QFP64	
	ST6245	4K ROM	140	64	7x8-Bit	2x8-Bit	SPI	11	QFP52	
*	ST6253	2K ROM	128		7x8-Bit	2x8-Bit		13	DIP20/SO20	
*	ST6260	4K ROM	128	128	7x8-Bit	2x8-Bit	SPI	13	DIP20/SO20	auto-reload timer + LED or TRIAC driver + PWM
*	ST6263	2K ROM	128	64	7x8-Bit	2x8-Bit		13	DIP20/SO20	
*	ST6265	4K ROM	128	128	13x8-Bit	2x8-Bit	SPI	21	DIP28/SO28	
	ST6280	8K ROM	320	128	12x8-Bit	2x8-Bit	SPI, UART	22	QFP100	LCD driver (dot matrix) + auto-reload timer + LED or TRIAC driver
	ST6285	8K ROM	288		8x8-Bit	1x8-Bit	SPI, UART	12	QFP80	
	ST7291	8/16/24K ROM	256/384			1x16-Bit		19	DIP28/SO28	wake-up function + power saving & standby modes + power supply monitor
	ST7294	6K ROM	224	256		1x16-Bit		22	DIP28/SO28	wake-up function + power saving & standby modes + WDG
	ST9036	16K ROM	224+256		8x8-Bit	2x16-Bit	SPI+SCI	56	LCC68	WDG + handshake + Direct Memory Access
	ST9040	16K ROM	224+256	512	8x8-Bit	2x16-Bit	SPI+SCI	56	LCC68	
	ST90R50		224		8x8-Bit	3x16-Bit	SPI+2xSCI	56	LCC84	WDG + 2 handshakes + Direct Memory Access + 16 M Bit address
	ST90R52		224		8x5-Bit	3x16-Bit	SPI+2xSCI	52	QFP80	

Abbreviations:

ADC = Analog to Digital Converter
SCI = Serial Communications Interface
WDG = Watchdog
SPI = Serial Peripheral Interface
USART = Universal Synchronous/ AsynchronousReceiver/Transmitter

Packages:

DIP = Dual In Line
QFP = Quad Flat Pack
S = Shrink
LCC = Leaded Chip Carrier
SO = Small Outline

Also check out our new ST62 REALIZER

The ST62 REALIZER is a user-friendly tool that assists designers in developing applications based on the ST62 family. A graphical schematic description of the application is used to automatically generate the executable code for the ST62 and to run simulations for verification of the program function. The complete tool set runs under Microsoft WINDOWS® environment.

*More Gold Standard devices available from ST (OTP versions only)

For more information fax 617-259-9442
Complete product information at http://www.st.com

SGS-THOMSON MICROELECTRONICS

READER SERVICE 142

HOT PC PRODUCTS

Eliminating the need to buy a new laptop, H&P Engineering is offering powerful upgrades such as the 586-150 MHz Compaq Elite upgrade. The processor upgrade allows users to have Pentium-class performance without having to spend the amount of money required for a new system. Previously, the soldered-to-the-board conditions of most portable systems prevented upgrades such as these, but now the greed for speed can be satisfied. Along with the Compaq Elite series, H&P also offers upgrades for Compaq Contura, IBM ThinkPad, and Toshiba laptop units. In addition to the new laptop upgrades, the company also offers complete hard-drive installation kits, with options for plug-and-play solutions. Recently, H&P introduced their PentiumUP! line, designed to outperform Intel's Pentium OverDrive CPUs. The upgrades do contain Intel Pentium CPUs, preventing compatibility problems. The company has clocked their Pentium-60 upgrades at 180 MHz, and Pentium-100 upgrades at 200 MHz.

For more information, contact H&P Engineering Inc., 425 Palm Ave., Ft. Lauderdale, FL 33312; (954) 463-6770; fax (954) 463-0620; Internet: http://www.upgrade.de.

It's tough to dislike a name like Smart and Friendly. The peripherals and multimedia manufacturer has recently expanded its CD-recordables line to include the CD-R 4006. The 4X6 CD recordable solution records at 4x speed and reads data at 6x speed. The recorder package comprises EasyCD-Pro CD mastering software that's Macintosh and Windows 3.1x, 95, and NT compatible; packet recording software; Macromedia's Backstage Designer Plus; MediaPath's MediaAgent for CDs; an Adaptec SCSI-2 host adapter for quick set up; applicator and software templates; cables, a sampler pack of CD-R labels; and one blank recordable CD. The recording and playback system allows users to record a complete 650 Mbyte disk in only 17 minutes. There are versions of the CD-R 4006 that come with Macromedia's Director 5 and Astartes Toast software. The internal version of the recorder is priced at $999, while the external version, equipped with Director 5 is priced at $1299. The external version that comes with Toast for the Macintosh is priced at $1099.

For more information, contact Smart and Friendly, 20520 Northoff St., Chatsworth, CA 91311; (800) 959-7001; fax (818) 772-2888; Internet: http://www.smartandfriendly.com.

PhotoSynthesis 1.0 is a new 3D solution for the PowerPC. The software from Silver Creek Software allows PowerMac users to produce high-resolution, photo-realistic, still-frame images. Designers will find that PhotoSynthesis models objects or scenes quickly, and can create to any resolution or size. Hundreds of preprogrammed shades provide unlimited options for the application of surface colors and textures. PhotoSynthesis also allows users to adjust shades to meet the needs of the designer. Simulating lighting found in a studio, the software is equipped with studio softbox lights. This lighting feature lets users create light reflections, eliminating the creation of environment maps. Silver Creek is offering two packages of PhotoSynthesis; one package includes Pixar's MacRenderMan (for rendering high quality image outputs), priced at $400, and PhotoSynthesis without the rendering software, priced at $350.

For more information, contact Silver Creek Software, 222 High St., #1, Silverton, OR 97381; (503) 873-2219.

Supporting the AES/EBU digital audio communication and SDI digital video (SMPTE 259M) protocols, the TARGA 2000 SDX by Truevision provides a real-time, desktop video editing system. Based on the TARGA 2000 RTX, the SDX features dual M-JPEG codecs to give users full resolution effects processing at up to 300 Kbytes per frame. Allowing video editing jockeys to link their systems with other SMPTE 259M compatible equipment, the SDX supports SDI. The TARGA 2000 SDX is priced at $11,995.

For more information, contact Truevision, 2500 Walsh Ave., Santa Clara, CA 95051; (800) 522-8783; fax (317) 577-8788; Internet: http://www.truevision.com.

Giving financial, business, and educational institutions a new way to present their video information, Connectware has introduced its RasterVideo-PC card. The RasterVideo-PC card is an ISA-based solution, designed to produce high-quality live video on any Windows 3.1-, 95-, or NT-equipped, ISA-compatible personal computer. RasterVideo-PC can display video coming from a variety of sources, such as antenna inputs, cable feeds, composite cameras, or SVideo sources. The video solution displays in 16.8-million (24-bit) colors, no matter what the graphics color depth might be. Featuring a fully-scalable video window up to full-screen 1600 by 1200 resolution, RasterVideo-PC also has audio-management capabilities. The new technology is capable of supporting independent audio supplies from two different video sources. Automatically selected, the RasterVideo PC audio feeds can be directed to either the line-in connector on the sound card, or the speakers. RasterVideo-PC comes in NTSC, PAL, composite-only, or custom versions.

For more information, contact Connectware, 1301 E. Arapaho Rd., Richardson, TX 75081; (214) 997-4143; fax (972) 997-4310; Internet: http://www.connectware.com.

Reinventing The Wheel

Targeting catalog developers, corporate knowledge bases, customer response services, directory publishers, and webmasters, Inmagic is currently offering DB/Text WebServer. WebServer as a 32-bit Windows NT-based Internet publishing solution designed to cut site maintenance time dramatically.

Providing a means for visitors to surf through sites without wading through endless hyperlinks, WebServer's robust data management features allow for quick and easy information searches.

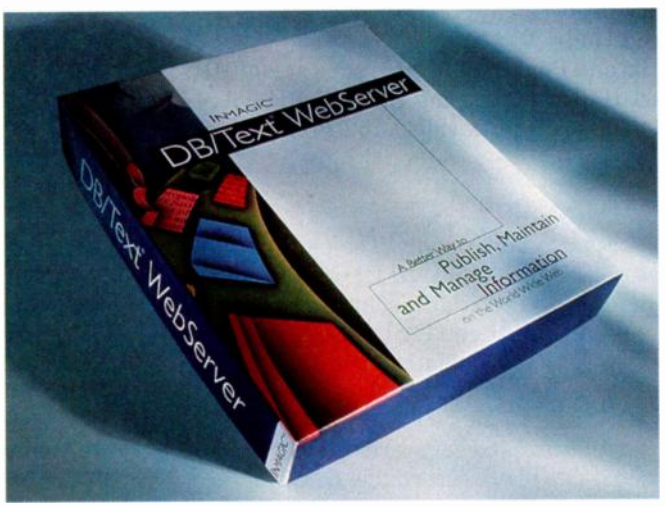
The WebServer publishing solution allows webmasters to create a variety of templates for information viewing. For example, if an individual has very little or no experience with the Internet or searching for information with a fielded search engine, the webmaster could provide a novice view or a summary view for that person. On the other hand, if the webmaster knows that the majority of people using the system are web savvy, detailed or expert views can be created. From queries entered at the views, WebServer dynamically generates HTML documents based on the search results.

Data management is improved by the use of batch modify, delete or import functions. These steps eliminate the confusing job of juggling hundreds, or even thousands of individual HTML documents. They also allow webmasters to maintain unlimited documents.

In the corporate intranet publishing environment, WebServer can be used to facilitate the dissemination of such information as competitive intelligence, employee handbooks, 401k policies, and market research databases. Customer requests for technical support or warranty information can be fulfilled over the Internet, rather than by phone, in the customer response service of WebServer.

Other features of DB/Text WebServer include:

- Dynamic display—Formatting on the fly; catering to specific audiences: Alphabetical, Brief/Detailed, Chronological, Novice/Expert.
- Instant text retrieval—All fields can be indexed, speeding up searches.
- Data management—Data can be edited across multiple documents; when documents are added or deleted no relinking in necessary.
- Variable-length fields—Data is not truncated by fixed-field limits, thereby keeping intact the structure and integrity of the text during queries.



- Three-dimensional fields—Data fields can have an unlimited number of entries.

In addition to Inmagic's WebServer publishing solution, the company recently introduced its Java applet add-on word wheel at the Fall Internet World Conference, New York, N.Y.

The word wheel allows users to preview the keyword indexes of all the words in a DB/Text WebServer database located on web sites or intranets. Designed to eliminate trial-and-error searching, the word wheel works by providing a list of words or terms found in a particular field, along with the number of records found containing each word or term. All the user has to do is to just enter one keystroke.

On the webmaster end, the applet eliminates the programming of pick lists. Programming pick lists for content-heavy sites can consume a great deal of time, to say the least. Not to mention the reprogramming that needs to be done when content changes are made. The reprogramming is unnecessary with the word wheel, because it automatically indexes new content and then adds it to the keyword lists.

Another new development at the Inmagic shop is its recent partnership with Lycos Inc. Lycos and Inmagic have arranged to produce a series of new corporate intranet spidering products.

The standard bearer of the product line will be the Lycos Intranet Spider. The Spider will provide basic navigation services by spidering HTML and non-HTML documents in a predefined browsing pattern. An Inmagic text database bundled with the product holds cataloged, searchable document data. For companies that require more powerful navigation, the Lycos/Internet team will offer the DB/Text NavigationServer. NavigationServer combines the Lycos Intranet Spider with the WebServer technology. Features include support for a wider variety of document formats, user-defined reporting, password access, and the ability to handle meta data.

Add-ons that will be forthcoming include the Lycos Sites by Subject Directory and the Lycos Catalog Link. The Sites by Subject Directory will allow users to access a list of the most popular web sites on the Internet from within the company firewall. There are rapid links to tens of thousands of sites.

In addition, users who add the Catalog Link can design their search criteria to query outside the firewall and receive information automatically imported into the database within the firewall.

If you'd like to see a live demonstration of the WebServer, visit the Inmagic site on the World Wide Web at http://www.inmagic.com.

For more information on the DB/Test WebServer, contact Inmagic Inc., 800 West Cummings Pk., Woburn, MA 01801; (617)938-4442; fax (617) 938-6393.

"I'VE HEARD IT SAID THAT YOU CAN NEVER GIVE A GAME DEVELOPER ENOUGH RESOURCES.

WELL, THIS IS ONE OF THOSE TIMES WHEN WE EXCEEDED THEIR *wildest* EXPECTATIONS."

DARREN SMITH, *Project Manager,* NINTENDO 64

"Getting a machine like the Nintendo 64™ to market was an amazing experience. For three years, I coordinated efforts between Nintendo, MIPS™ and the folks at NEC.

"During that time, we looked at several versions of MIPS RISC processors. However, NEC's V_R Series™ processor shot to the top. Without question, it provided the most power for the price.

"One great thing about the V_R Series processor is what it enables. You see, game developers no longer have to hold back. It's now possible to create fantastic revolutionary games at an unbelievably low cost. With power to spare for things like on-the-fly image decompression, and even things they've only dreamed about doing.

"For the first time, developers can truly simulate reality. If they want something to happen, it will happen. Take, for example, WaveRace64.™ The NEC V_R Series allows for such incredibly smooth and realistic dynamics when riding on water, that you'd be well advised not to play if you get seasick.

"Frankly, it's exactly what you'd expect from a Nintendo/NEC partnership. I just can't stress enough what a phenomenal job NEC does of keeping an eye on your bottom line. NEC clearly understands that every penny counts. In fact, they were able to reduce the number of pins. And in case you didn't know, every pin is another million dollars in our business.

"But it also means a lot to the kids. You see, the V_R Series processor is an evergreen design. So it won't be obsolete in two or three years. And that means Nintendo 64 devotees can put their allowances towards other things. Like buying books or planting trees. And hey, maybe they'll even buy a few more games."

For more information about NEC's V_R Series call *1-800-366-9782.* Ask for Info Pack #195.

"NEC's V_R Series processor has helped make the Nintendo 64 the most significant consumer electronics product since the VCR."

NEC

READER SERVICE 156

Here's another confirmation that the Year 2000 Date Change (Y2K) dilemma will be affecting an enormous sector of the population. According to the Christian & Timbers 1997 annual report on Hot and Not So Hot Jobs, the seventh hottest job is Vice President, Year 2000.

Defining a "hot" job, Christian & Timbers took a look at positions that are increasing in demand and increasing in compensation. "Not so hot" jobs are positions that are sinking in demand, and in some cases, compensation.

Christian & Timbers examined their files of interviews, client search requests, and surveys to compile a list of most and least requested positions to be filled in the executive ranks.

The results of the study are shown in terms of predicted percentage growth decline. Predicted percentage growth was defined by the largest increase in demand to fill positions. Predicted percentage decline was measured by the highest decrease in demand to fill positions.

To give the Veep of Y2K some perspective, here is the complete ranking of top hot jobs with their respective predicted growth percentages:

The Temporary Executive, 314%
Internet Software Architect, 198%
Chief Marketing Officer, 178%
Healthcare CIO, 121%
The Internet Executive, 99%
Chief Technology Officer, 96%
Vice President, Year 2000, 83%
Start-Up CEO, 81%
Executive Search Consultant, 76%
Security Analyst, 75%
Vice President, Staffing, 74%
Information Technology Consultant, 86%
Vice President, Call Centers, 51%

The job description for the Vice President, Year 2000 calls for a keen consultant. This person should be capable of quickly building a team to handle all of the problems concerned with converting computers to Y2K compliant status.

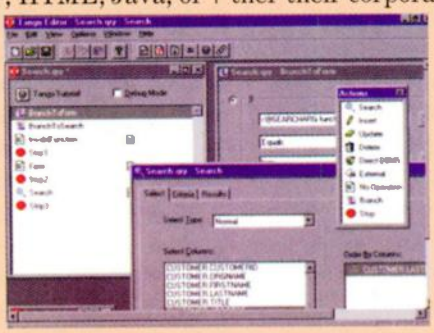
The most important feature of a consultant in this field is a patient nature. The customers will be in a very big hurry to find a quick fix to the problem. Government work or banking will be where this executive will be in the highest demand.

Contact Christian & Timbers, One Corporate Exchange, 25825 Science Park Dr., Suite 400, Cleveland, OH 44122; (216) 464-8710; fax (216) 464-6160; Internet: http://www.ctnet.com. —DS

Tango, More Than Just Cha-Cha-Cha

Dancing its way into WebFORCE, and other Silicon Graphics (http://www.sgi.com) toolkits, EveryWare Development's Tango technology is an Internet Rapid Application Development (IRAD) tool.

Requiring no knowledge of C/C++, HTML, Java, or SQL, Tango is compatible with Windows, Macintosh, and Unix. The toolkit employs Tango-based tools in the creation, deployment, and management of electronic storefronts. Users with the tools have the capability to create dynamic HTML pages from ODBC-, Oracle-, Informix-, or Sybase-compatible databases.



Tango Merchant supplies electronic storefronts with a relational SQL database, Tango Merchant Administrator, and the Storefront itself. Storing all pertinent product information, the database also holds all new orders that have been placed, automatically updating inventory. The administrator is of the point-and-click variety, keeping the management of the system to a minimum. The storefront application comprises a number of different kinds of templates that have been preconfigured with HTML.

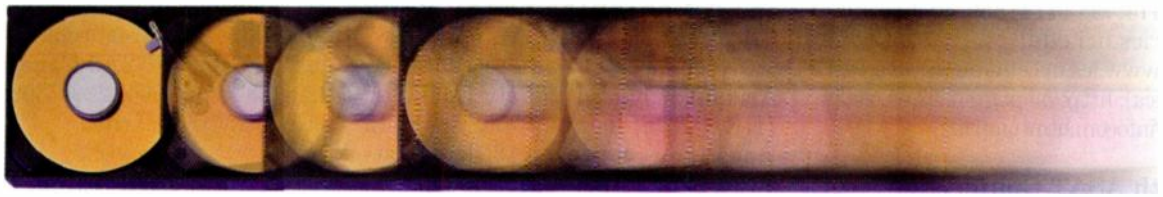
Tango Merchant allows electronic storekeepers to import existing product information, integrate their existing technology, ensure secure Internet transactions, authorize credit cards, support a variety of payment options, customize shipping charge calculations, send automatic order notifications, support repeat customers, provide order reference numbers, and purge processed orders (to cut down on administrative duties).

Tango Enterprise is a JavaScript-enabled tool designed to help companies provide dynamic sites for either their corporate intranets or Internet applications. The move to incorporating Netscape's (http://www.netscape.com) JavaScript within Enterprise was made to bring a number of new functions to the user. This functionality includes monitoring user-generated events, such as mouse clicks and key presses; calling and referencing Java classes; and validating form fields. Some of the features of Tango Enterprise include support for Oracle, FileMaker Pro, and ODBC data; the ability to access multiple related tables within the database simultaneously; and a debugging checkbox.

Tango Enterprise is priced between $995 and $2295. Tango Merchant starts at $4995.

For more information, contact EveryWare Development, 6733 Mississauga Rd., 7th. Floor, Mississauga, Ontario, Canada, L5N 6J5; (905) 819-1173; fax (905) 819-1172; Internet: http://www.everyware.com/.—DS

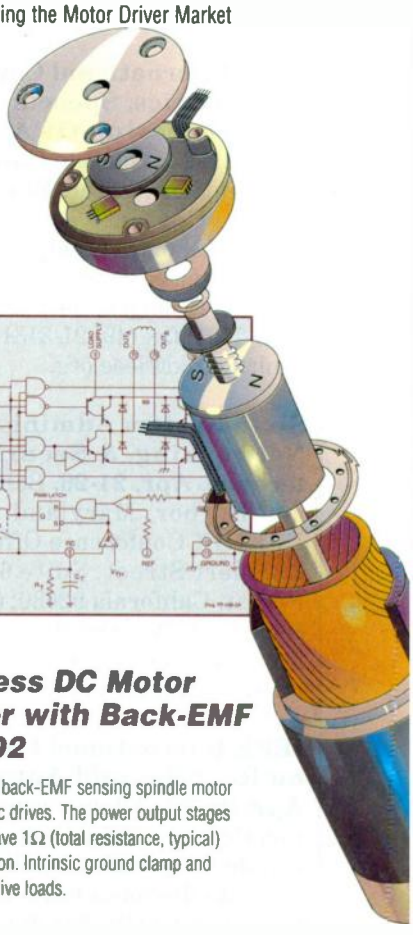
AT ALLEGRO, WE'RE SETTING A REVOLUTION IN MOTION



Whether it's bidirectional control of servo or stepper motors, PWM closed loop current control, back-EMF sensing, or 3 V operation, Allegro sets the standard for today's motion control needs.

Continuing our leading edge tradition, we've just introduced the new A3953 Full-Bridge Motor Driver, designed to provide the optimal bipolar drive solution. The A3953 is ideal for use in any industrial motor driver application which requires bidirectional pulse width modulated current control of up to 1.3 A. Supplied in two package options (16-Pin DIP or 16-Lead SOIC), the A3953 complements our existing line of single and dual full-bridge motor drivers.

At Allegro, we're dedicated to serving the Motor Driver Market by providing outstanding product performance and innovation that enhance your ability to design complete motion control solutions.



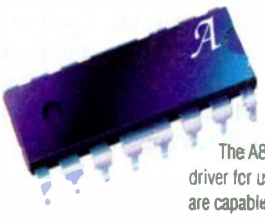
New From Allegro

Full-Bridge PWM Motor Driver — A3953

Designed for bidirectional pulse-width modulated (PWM) current control of inductive loads, the A3953S is capable of continuous output current to ±1.3 A and operating voltages to 50 V. Internal fixed off-time PWM current-control circuitry can be used to regulate the maximum load current to a desired value. The peak load current limit is set by the user's selection of an input reference voltage and external sensing resistor. The fixed off-time pulse duration is set by a user-selected external RC timing network. Internal circuit protection includes thermal shutdown with hysteresis, flyback diodes, and crossover current protection. Special power-up sequencing is not required.

- ±1.3 A Continuous Output Current
- 50 V Output Voltage Rating
- 3 V to 5.5 V Logic Supply Voltage
- Internal PWM Current Control
- Saturated Sink Drivers
- Fast and Slow Current-Decay Modes
- Automotive Capable
- Sleep (Low Current Consumption) Mode
- Internal Suppression Diodes
- Internal Thermal Shutdown Circuitry
- Crossover-Current and UVLO Protection

Dual Full-Bridge PWM Motor Driver — A2919



The A2919SB and A2919SLB motor drivers are designed to drive both windings of a bipolar stepper motor or bidirectionally control two DC motors. Both bridges are capable of sustaining 45 V and include internal pulse-width modulation (PWM) control of the output current to 750 mA. The outputs have been optimized for a low output saturation voltage drop

3-Phase Brushless DC Motor Controller/Driver with Back-EMF Sensing — A8902

The A8902CLBA is a three-phase DMOS back-EMF sensing spindle motor driver for use in 5 V and 12 V Winchester disc drives. The power output stages are capable of ±1.25 A output currents and have 1Ω (total resistance, typical) DMOS power outputs for low power dissipation. Intrinsic ground clamp and flyback diodes are provided for driving inductive loads.

Visit Our New Web Site

Complete information on many of the products offered by Allegro are now right on our web site. You'll find us on the World Wide Web at *http://www.allegromicro.com.*

The Clear Choice for Motion Control Design.

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READER SERVICE 95

APRIL

IEEE Conference on Computer Communications (INFOCOM 97), April 7-11. Kobe, Japan. Contact Tatsuya Suda, Department of Information & Computer Science, University of California, Irvine, California 92717-3425; (714) 856-5474; fax (714) 856-4056; e-mail: suda@ics.uci.edu; Internet: http://www.ics.uci.edu/infocom/ (North America); http://arpeggio.ics.es.osaka-u.ac.jp/infocom.html (Japan).

Fourth ASAT Conference , Apr. 14-16. San Francisco Airport Marriott, San Francisco, CA. Contact Suzanne Graf, Project Manager, (541) 984-5204; fax (541) 343-7024; e-mail: SGraf@Advanstar-Expos.com.

IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP 97), Apr. 21-24. Gasteig Cultural and Convention Center, Munich, Germany. Contact Bernd Girod, Lehrst.f.Nachrichtentechnik, Univ. of Erlangen Nuremberg, Cauerstr. 7, D-91058 Erlangen, Germany; (49) 91-3185-7101; fax (49) 91-3131-30840; e-mail: b.girod@ieee.org.

Sixth System Administration, Networking, & Security Conference, Apr. 21-26. Baltimore Inner Harbor, Maryland. Contact USENIX Conference Office, 22672 Lambert Street, Suite 613, Lake Forest, California 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

IEEE International Conference on Robotics and Automation, Apr. 21-27. Albuquerque Convention Center, Albuquerque, NM. Contact Jerry Stauffer, Intelligent Systems and Robotics Center, Program Office, MS0949, Sandia National Laboratories, Albuquerque, NM 87185-0949; (505) 845-8966; fax (505) 844-6161; e-mail: jdstauf@isrc.sandia.gov.

First Convergence Technology & IC Expo, Apr. 22-24. InfoMart, Dallas, TX. Contact Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045; (800) 877-2668, ext. 243; fax (310) 641-5117.

15th IEEE VLSI Test Symposium, April 27-30. Hyatt Regency Monterey, Monterey, California. Contact Y. Zorian; (408) 543-0146 ext. 227, e-mail: zorian@lvision.com.

MAY

IEEE Vehicular Technology Conference (VTC), May 5-7. Hyatt Regency at Civic Plaza, Phoenix, Arizona. Contact Wendy Rochelle, IEEE Conference Services, 445 Hoes Lane, P.O. Box 1331, Piscataway, New Jersey 08855-1331; (908) 562-3870; fax (908) 981-1769; e-mail: w.rochelle@ieee.org.

International Test Synthesis Workshop, May 5-7. Santa Barbara, CA. Contact K. Wagner; (415) 694-4386; e-mail: kwagner@symopsys.com.

IEEE Custom Integrated Circuits Conference (CICC '97), May 5-8. Santa Clara, CA. Contact Melissa Widerkehr, Widerkehr & Assoc., Suite 270, 101 Lakeforest Blvd, Gaithersburg, MD 20877; (301) 527-0902; fax (301) 527-0994.

Electronics Industries Forum of New England, May 5-9. World Trade Center, Boston, MA. Contact Summit Exhibition Management Inc., Norwalk CT; (800) 322-9332; (203) 855-3000; fax (203) 855-3003.

IEEE Power Industry Computer Applications Conference (PICA), May 11-16. Contact T.C. Wong, American Electric Power, 1 Riverside Plaza, Columbus, OH 43215; (614) 223-2235; fax (614) 223-2205; e-mail: t.wong@ieee.org.

IEEE/IAS Industrial & Commercial Power Systems Technical Conference (I&CPS), May 12-15. Wynham Hotel, Philadelphia, PA. Contact Barry Hornberger, Philadelphia Electric Co., 2301 Market St., Bldg N3-1, Philadelphia, PA 19101; (215) 841-4619.

Fifth IFIP/IEEE International Symposium on Integrated Network Management (ISINM '97), May 12-16. Hotel Del Coronado, San Diego, California. Contact Ann Marie Lambert, BBN Systems & Technologies, 10 Moulton St., Cambridge, Massachusetts 02138; (617) 873-3819; fax (617) 873-37776; e-mail: isinm97@bbn.com.

IEEE Particle Accelerator Conference, May 12-16. Vancouver, BC, Canada. Contact M.K. Craddock, TRIUMF, 4004 Wesbrook Mall, Vancouver, BC V6T 2A3 Canada; (604) 222-7341; fax (604) 222-7309; e-mail: craddock@triumf.ca.

Antennas: Principles, Design and Measurements (Shor Course), May 13-16. St. Cloud, FI Contact Kelly Brown, NCEE, 110. Massachusetts Ave., St. Cloud, FL 34669; fax (407) 892-0406.

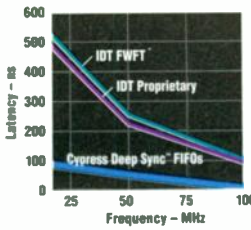
IEEE Radar Conference, May 13-15. Sheraton University Hotel & Conference Center, Syracuse, NY. Contact Michael Wicks, Rome Laboratory, 26 Electronics Pkwy., Rome, NY 13441; (315) 330-4437; fax (315) 330-2528; e-mail: wicksm@rl.af.mil.

Sensors Expo Boston, May 1 15. Hynes Convention Center, Bo ton, MA. Contact Expocon Manage ment Associates Inc. (203) 256-470 e-mail: sensors@expocon.com; Internet: http://www.expocon.com.

47th Electronic Components & Technology Conference, May 18-21. The Fairmont Hotel, San Jose, California. Contact Jim Bruorton, Electronic Industries Association, 2500 Wilson Blvd. Arlington, Virginia 22201-3834; 963-6621.

Finishing '97 Conference & E position, May 19-22. Rosemor Convention Center, Rosemont (Ch cago), Illinois. Contact Socie Manufacturing Engineers; (80 4763.

IEEE Instrumentation & Measurement Technology Conference (MTC '97), May 20-22. Chateau Laurier, Ottawa, Ontario, Canada. Contact Robert Myers, Conference Coordinator, 3685 M tor Avenue, Suite 240, Los A California 90034; (310) 287- (310) 287-1851; e-mail ers@ieee.org.

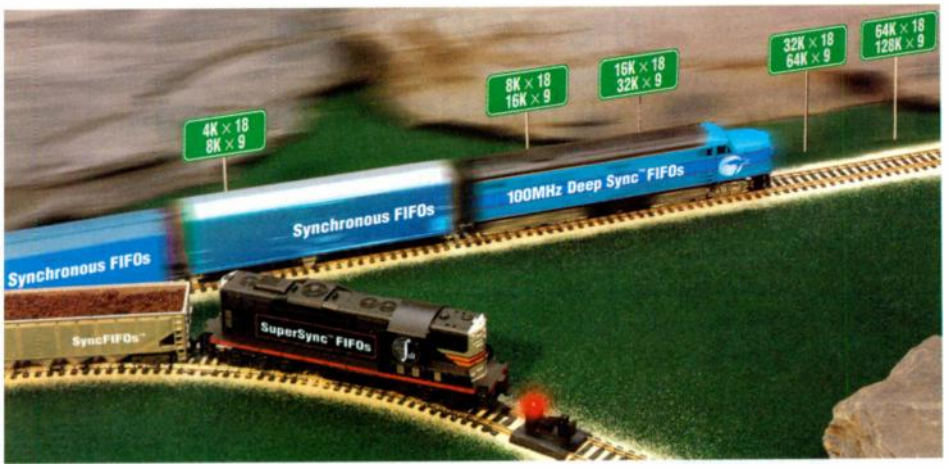


Deep Sync FIFOs offer true 100MHz performance, low first-word latency, and low power at <$1/KByte

Don't Let Them Get You Off the Track

"They" said it couldn't be done, but we did it anyway—broke through the density barrier with *standard-pinout* synchronous FIFOs. Cypress's CY7C4261/71 16K/32K × 9 and CY7C4255/65 8K/16K × 18 Deep Sync™ FIFOs offer the speeds and densities you need for high-bandwidth applications using the same industry standard synchronous (clocked) architecture used for lower-density sync FIFOs.

STAY ON TRACK WITH DEEP SYNC™ FIFOS



Upgrade Using Your Existing Sockets

No redesign. No timing issues. No pinout changes. No need to learn a new architecture. Just plug our Deep Sync FIFOs into your existing board to achieve the highest performance possible. No other FIFO supplier makes it this easy to upgrade your buffering solution!

The First-Word-Fallthrough Fallacy

Don't be fooled by FIFO features hype. Why should you wait 12.5 clock cycles for the first word of data when you can get it (and all the rest!) in less than 2 cycles? That's a savings of almost 500 ns!

Standard Sync FIFO Buffering Solutions for Today *and* Tomorrow

If you're looking for sync FIFOs offering the highest densities, fast cycle times, small packaging, low cost (less than $1/KByte), and the fastest time-to-market, look no further than Cypress. Our roadmap will keep you on track with devices that are deeper and wider, yet still socket-compatible with standard sync FIFOs.

Deep Sync FIFO Feature Comparison

IDT	CYPRESS	CYPRESS ADVANTAGE
Sync Architecture		
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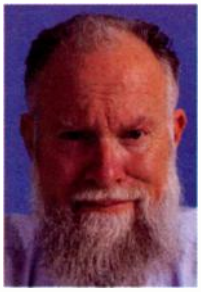
BOB PEASE

Bob's Mailbox



Dear Bob:

Re: "What's All This Stupid, Dangerous Stuff, Anyhow?" that appeared in the Oct. 24, 1995 issue. It's a little late, but I still wanted to tell you this one so that you might add to your collection of crassly stupid things we've done.

While at Mainz, West Germany with IBM from 1966 to 1974, our modest Analysis Laboratory—a production support facility—grew into a significant adjunct to IBM European research labs. I participated in research on thin-film disk drives and heads, "voice-coil" head positioners, and the original Winchester drive, to name a few.

This kept a young technician with only Air-Force electronics training and many hundreds of hours of self-directed practical training (lots of standby duty), really hopping (and studying).

Many incidents qualified for Hall of Duhh. For example an engineer applying 220 V/50 Hz directly to our brand new Tektronix 1S1 sampler input to "see if it worked." But one incident stands out:

Four or five scientists from Sindelfingen, FRG, and the Zurich, CH labs had come to observe our measurement techniques on an experimental disk of their making, using a variable-speed tester we had built. The design was based on the 2311 disk drive, a small free-standing unit.

Complete, the unit was about 36-in. tall, but it had been stripped down to the cast-aluminum base plate for access. The dc spindle drive motor was capable of 6000+ RPM with load, had great speed regulation and dynamic braking.

We mounted their 1/4-in. thick, 14-in. diameter glass disk on the standard spindle with hard paper shims. The test disk was a thing of beauty, with a sputtered iron-nickel film.

As our virgin disk first spun up toward 6 grand, I casually asked what kind of glass this was. Our visitors exchanged glances, shrugged and said it was standard plate glass from a Sindelfingen glazier. It took about two seconds to realize that this possibly stress-ridden monster was at a height located just below the belt with thin air as a shield. I immediately turned sideways and reached around to the vernier-dial speed setting. I cranked it down as smoothly as possible, rather than hitting the ac power switch which would have applied the dynamic brakes full-on before actual shutdown. My boss brusquely asked what I thought I was doing! I commented on my wish to retain my ability to father children and it finally dawned on them.

The next day, we were once again watching the spin-up, but protected by inch-thick aluminum sides and Plexiglass top cover. Thought this might bring a nervous grin to your grizzled visage. And thanks for the mixed Porridge, Pease.

STEVE ALLISON
TEKcellence
Ramon, Calif.

I'd have hollered "INCOMING" and dropped to the floor. And on the way down, I would have turned down the speed, smoothly, as you did. I guess the next day the disk did spin up to 6000 RPM, safely, or you would have said so.—RAP

Sir:

I've followed the Tandy 100 thread in your "Bob's Mailbox" column for Sept. 16 and Nov. 18th. The letter that follows was typed a half-hour ago, just before my fancy '486 locked up with a simple "No more handles allocatable. System Halted" on the screen. I think you'll catch the relevance!! You may wish to check an interesting web site: *http://lenin.cc.rochester.edu/orphan/orphan.html*. It has resources for owners of "orphaned computers." The Tandy 100 is one of the computers covered.

After owning a Tandy 100 and the Minisport, I think you may not wish to bypass looking at the Zenith Minisport. I purchased four of them back in 1991. Fifty bucks for working ones, and $25 for nonworking. I ended up selling two for a profit, and still use the other two now.

For two years, I published a newsletter about the Minisport. You can poke around a SimTel archive and find a compendium, or search for the phrase "mlhack" on the Lycos web search engine. Or, you can get link information from my home page: *http://www.pcisys.net/~mork/*.

The Minisport has all the Tandy 100 does, and more. It has a full 80-in. by 25-in., almost identical footprint. It has 1 or 2 Mbytes of memory, and any memory that's not used for system memory is available as a RAM disk. It's an 8088 with MSDOS in ROM. Using Stacker, I now have a 640 k MSDOS machine with a 3 Mbyte RAM disk, plus the on-board 2.5-in. floppy. Plus a modem port. Plus serial/parallel compatible with the PC world.

It comes with a FTP-ish program that will squirt itself through the serial line into another PC/MSDOS computer, and then allow free transfer of files back and forth. During three military deployments to Europe and Saudi Arabia back during Desert Storm, I was able to carry a Minisport around with me, and wherever I was, transfer programs and get laser printed hardcopies from whatever office I was currently in. Not to mention, backup on to hard drives.

Anyhow, I thought you'd be interested that there's more than a small group of people who've had enough of the $4000 multimedia laptop.

BRIAN J. MORK
USAFA, Colo.

Brian, thanks for the Minisport ideas. But, I just bought a Tandy 102. It's perfectly adequate for my ASCII typing. Still, I appreciate the clue on the website for orphan computers. Wonder if my ADAM is listed.—RAP

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

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National Semiconductor
P.O. Box 58090
Santa Clara, CA 95052-8090

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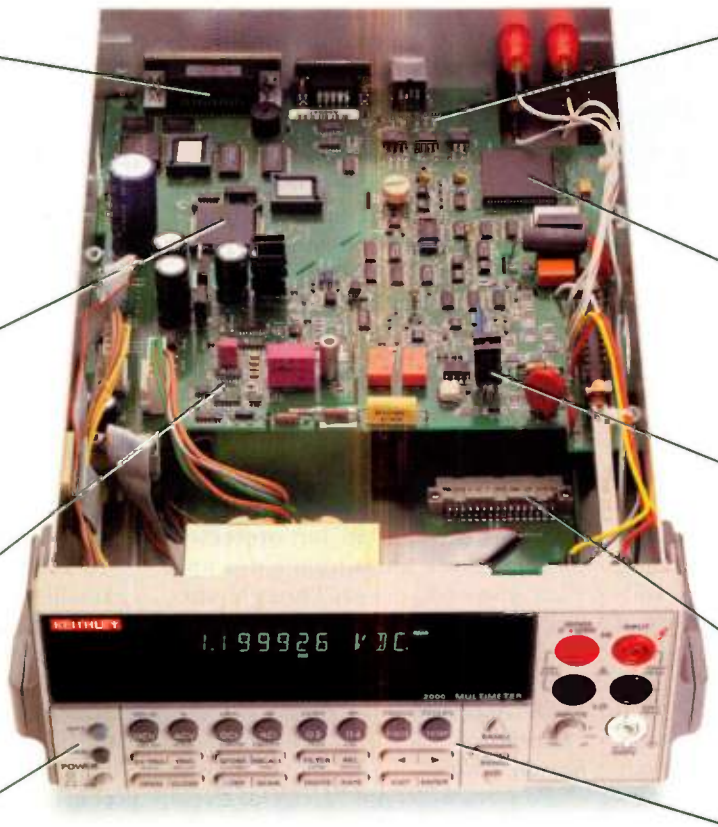

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Specifications

	Ranges	Resolution	Basic Accuracy 90-day (% of rdg. + % of range)	Basic Accuracy 1-year (% of rdg. + % of range)
• DC volts	100mV – 1000V	100nV – 1mV	0.002 + 0.0005	0.003 + 0.0005
• DC amps	10mA – 3A	10nA – 10µA	0.03 + 0.004	0.05 + 0.004
• AC volts	100mV – 750V	100nV – 1mV	0.05 + 0.03	0.06 + 0.03
• AC amps	1A – 3A	1µA – 10µA	0.10 + 0.04	0.10 + 0.04
• Ohms	100Ω – 100MΩ	100µΩ – 100Ω	0.008 + 0.001	0.01 + 0.001
• Frequency	3Hz – 500kHz	1µHz – 100mHz	0.01% of rdg.	0.01% of rdg.
• Period	2µs – 333ms	1ps – 100ns	0.01% of rdg.	0.01% of rdg.

HOWARD JOHNSON

Moats & Floats

Moats, islands, cuts in the ground, isolated power planes, floating ground regions and a host of other intricate layout techniques are routinely used by digital engineers to reduce crosstalk, bolster EMI performance, and otherwise improve overall system operation. Yet I rarely encounter an engineer who can show me a clear before-and-after comparison demonstrating precisely what was the effect of the "improved" layout.

Why not? The excuses most often given are: lack of time, money, and schedule for a separate test board. It's not that the testing process itself would be difficult. Given a test board, comparing the performance of two layouts is easy. The problem is that we don't usually have the test board.

We can improve this situation by taking advantage of the way PCB's are designed and manufactured. To see how this can be accomplished, let's first focus our attention on the interface between your layout shop (the people that route PCB traces) and the board fabrication shop (the people that make bare, printed circuit boards).

This is the point at which your board design crosses over into the realm of real-world manufacturing. It is also a point beyond which many of us digital engineers rarely dare to venture, and that is a real-world shame. If there is one thing I have learned over the years, it's that the more we know about manufacturing, the better our designs tend to be. I'd love to write a whole book on that subject. For now, let's turn our attention back towards the layout-to-board-fab interface. With a better understanding of how this interface works, you can learn to get eight different prototype boards fabricated for the price of one.

In most cases, information is transferred from layout to board fab in the form of Gerber files.[1] The standard Gerber file format is a rather primitive, but highly effective format for describing two-dimensional graphical information. It is well-suited for representing the two major components of a PCB image: lines and dots. To first order, you might think of each file in a Gerber file set as representing a picture of one layer in your printed circuit board stackup.

The layout house forwards to the fab house a set of Gerber files that completely represent every layer of your board. Now, here is where things get interesting.

HOWARD JOHNSON

The first thing the fab shop does with your Gerber file artwork is to panelize it; that is, to step and repeat the artwork several times in order to fill up a standard fabrication panel.

Fab shops like to work with big sheets, or panels, of printed circuit board material. Typical panel sizes might be 12 in. x 18 in., 18 in. x 24 in., or even bigger. The bigger the panel, the lower their manufacturing costs. On a big panel, a fab shop might be able to panelize six or eight of your circuit cards, resulting in less handling of each card, and lower costs than if the boards had been individually fabricated.

On a typical prototype run for an EISA card, the fab shop takes in one copy of the Gerber files and panelizes it to create a new Gerber file set that shows maybe eight boards on one panel. Next, they make a set of panelized artwork masks from the new Gerber files, and shoot a couple of panels worth of boards. Then they chop the boards apart. You end up with a set of perhaps sixteen cards for their minimum prototype processing fee. That's probably more than you wanted.

If you want to get more out of the prototype fab cycle, try this: ask your layout house to "prepanelize" the design. They will have to call the fab shop to get all the rules about panel sizes, minimum spacing between boards, placement of tooling holes, edge clearances, and the like, but it's well worth it.

The prepanelized design, like a regular design, results in a set of Gerber files. The difference is that the prepanelized design includes eight full copies of the same design, all laid out for fabrication on one big panel. Once you have the prepanelized Gerber files, this is where you get to have some fun. Have your layout person open up the Gerber file editor and just GO CRAZY.

Of the eight boards on your panel, try shorting out the moat on one, eliminate the guard traces on the next; just go ahead and do all those little modifications you always wanted to do but never seemed to have a chance to try.

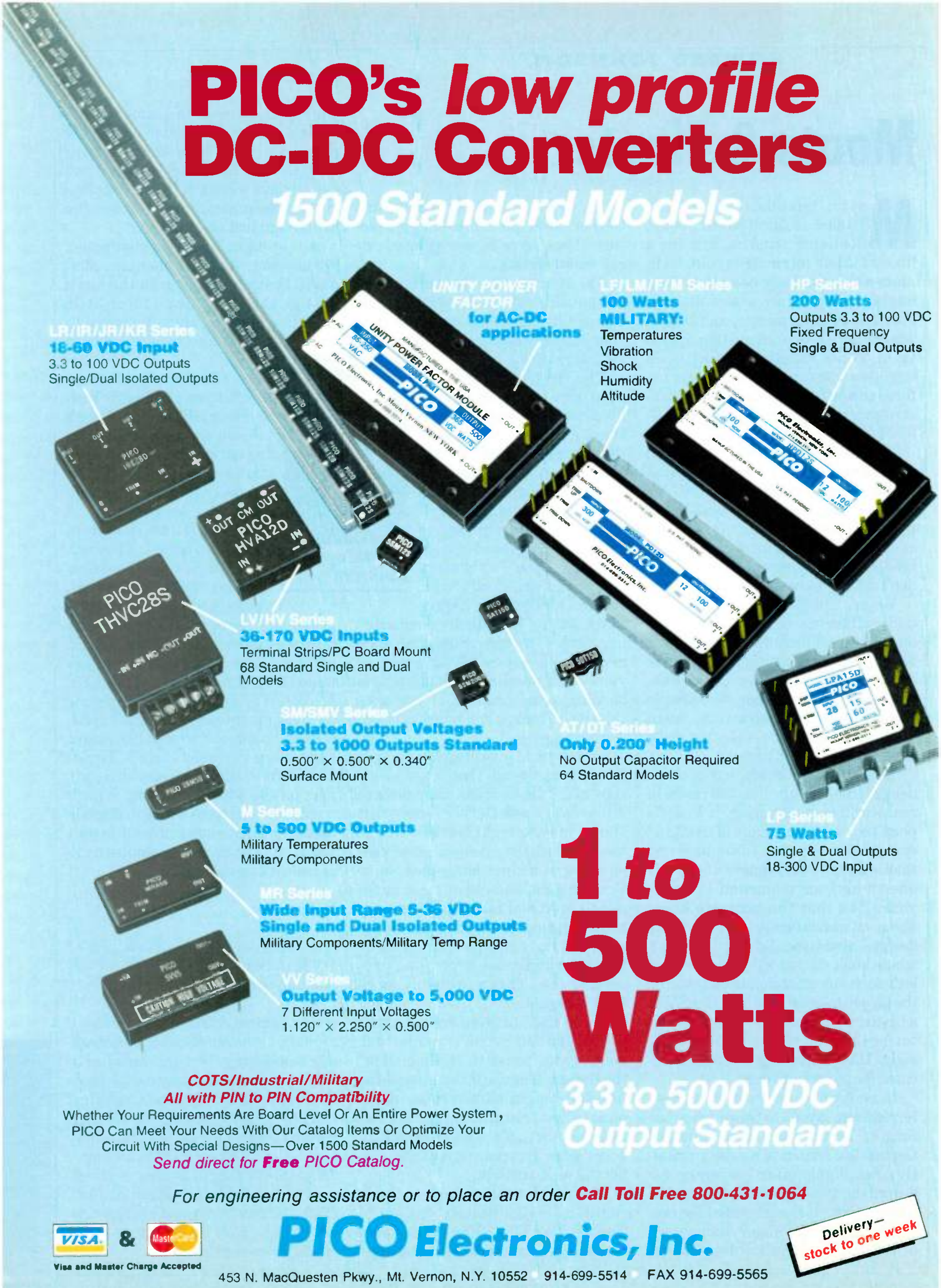
Sure, there are limitations on what you can modify with a Gerber editor. Your layout person can explain them. It's not perfect, but it gives you a wonderful opportunity to really learn something about your design.

Best of all, the fab shop probably won't notice. They will just take your panelized Gerber files, make the artwork masks, and shoot some panels in the regular way. When the boards come back ready for assembly, you'll get back all the real boards you need, PLUS ALL OF THE TEST LAYOUTS. By piggybacking your test designs onto an existing fab cycle, the test boards will appear, like magic, right when you need them. They're almost free, and have very little impact on the whole schedule. What's more, now you have a way to directly quantify the benefits of your layout tricks with an apples-to-apples comparison of like designs.

References:

1. Thanks to Dave Hawkins of DVK in San Jose, CA for first explaining to me how this works.

Dr. Howard Johnson is president of Signal Consulting Inc., a high-technology consulting firm specializing in solving high-speed digital design problem. He regularly presents technical workshops for digital engineers, including courses for Oxford University and UC-Berkeley. He is the author of "High-Speed Digital Design: A Handbook of Black Magic" (Prentice-Hall, 1993). He can be reached at (206) 556-0800; fax (206) 881-6149; e-mail: howiej@sigcon.com.



READER SERVICE 198

Spice Library Aid. SMPS Designers

Designers of switch-mode power supplies can get an assist from a new Spice library from Intusoft that contains a set of switching-level models for pulse-width-modulating ICs. Where previous modules were based on state-space-average models that don't show many critical nonlinear effects, this library includes a unified state-space PWM model which works for ac, dc, and transient analysis in continuous and discontinuous modes. Included are over 20 current- and voltage-mode PWM IC models for parts from Unitrode, Linear Technology, Siliconix, and Cherry Semiconductor. The models use analog behavioral elements, special Boolean logic elements, and new HD elements that reduce simulation run-time. The library also offers Spice models for nonlinear magnet cores, IGBTs, transformers, voltage regulators, motor controller ICs, and power-factor correcting ICs. Selling for $395, the library's models are compatible with Intusoft's native analog and mixed-mode Spice 3-based simulator, and existing ICAP/4 systems for DOS, NEC, Windows, Macintosh, and the Power Macintosh. IsSpice3 or IsSpice4 is required. ML

Intusoft, P.O. Box 710, San Pedro, CA 90733-0710; (310) 833-0710; fax (310) 833-9658; e-mail: 74774.2023@compuserve.com. **CIRCLE 655**

Extraction Tool Targets Deep Submicron Designs

As designs use increasing numbers of transistors, efficiently analyzing complex designs and reducing costly design iterations due to undetected timing problems is more critical than ever. Star-R version 2.0, a full-chip smart extraction package for deep submicron designs, now makes this possible. It allows for full-chip extraction of parasitic information and signal delays to within 5% of actual chip implementation.

Key to the tool's success is its automatic Smart Extraction, a simulation-based extraction technology developed in-house. With this technology, the designer, at various stages of a design process, simply specifies a desired delay accuracy and computer resource requirements are optimized automatically Simultaneously, the chosen accuracy level is guaranteed. As a result, computer run times and peak memory requirements are reduced by up to 10 times when compared with full-chip extraction without Smart Extraction.

Using simple push-button operations, all tool information is generated in industry standard formats, making it completely logic and timing simulator ready. With the tools graphical-analysis capabilities, complex clock distribution networks and critical signals can be easily extracted and analyzed. The Star-R version 2.0 software tool includes fast RC circuit reduction with accuracy control and asymptotic waveform evaluation (AWE)-based simulation for accurate interconnect delay calculations. It's also integrated with 3D field solver process simulation tools to automatically generate capacitance models. As a complement to the tool, silicon characterization and model calibration service (which matches the extraction models with actual silicon processes) are provided by Meta-Software's Meta-Labs. Available now, the Star-R version 2.0 tool, in U.S. dollars, starts at $125,000. CA

Avant! Corp., 1208 East Arques Ave., Sunnyvale, CA, 94086-5401; (408) 738-8881.
e-mail: info@avanticorp.com
Web: www.avanticorp.com
CIRCLE 656

Simulator Boasts 10-Fold Speed Improvement

A recently introduced linear-acceleration capability, the STAR-ADM(TM), boasts a 10X improvement over the STAR-ADM high-performance timing and power simulator. It's based on a PACT (pole analysis via congruence transformations) algorithm designed to reduce large multiport 3D mesh networks with strongly connected internal nodes. The STAR-ADM(TM) works by transforming admittance matrices representing a full network into smaller equivalent matrices. The smaller matrices then can be input directly into the STAR-ADM simulator. Large databases are able to be simulated while maintaining the integrity of crosstalk analysis and retaining critical cross-coupled capacitances. Consequently, this method can preserve network stability while reducing memory use for designs with large parasitic elements by up to 99%. The STAR-ADM(TM), when used with STAR-ADM, delivers accurate simulation of parasitic effects critical for signal crosstalk, power line, clock slew, power, and timing analysis. Offered as an option to the STAR-ADM product, the linear acceleration feature is now available and supports standard Spice net-list exchanges to all popular extraction tools and waveform viewers. Priced at $20,000 in the U.S., it runs on both Sun and HP Unix workstations. CA

Avant! Corp., 1208 East Arques Ave., Sunnyvale, CA, 94086-5401;(408) 738-8881.
e-mail: info@avanticorp.com
Web: www.avanticorp.com
CIRCLE 657

Pc-Board Tool Diagnoses Emissions Problems

The EmcScan emissions software simulation tool is specifically developed to help pc-board designers easily identify electromagnetic hot spots, as well as the segments of nets that cause these problems. The diagnostic and design tool is targeted for use by non-EMC (electromagnetic compatibility) specialists. It performs the EMC simulation during routing or at the post-layout stage, and interfaces directly with the CCT (Cooper & Chyan Technology) SPECCTRA autorouter and all major CAD layout tools. Focusing on pc-board design, it uses the same algorithms, design schematic, and layout databases as its counterpart—the Compliance electromagnetic compatibility simulator software tool aimed at systems of the pc board with cables and enclosures.

The EmcScan tool works by calculating the electric and magnetic fields over the pc board, as well as current spectra and track current densities. Current and voltage waveforms can be examined to look for signal ringing, which, along with improper routing, are major contributors to radiation. The EmcScan software tool,on a Unix platform, costs $15,000 in the U.S. CA

Quantic Laboratories Inc., 191 Lombard Ave., Winnipeg, Canada, R3B 0X1; (204) 942-4000 or 1 (800) 665-0235. **CIRCLE 658**

ANALOG

Temperature Controller Has Programmable Hysteresis

The TC07 temperature controller consists of an on-chip temperature sensor and user-programmable threshold detector. Running on power supply levels as low as 2.7 V, it operates over a maximum temperature range of -40°C to +125°C. Commercial and industrial versions also are available. The controller can operate in an open-loop mode as an overtemperature or undertemperature monitor, or as a closed-loop controller when its outputs are connected to a fan or heating system. Both high-true and low-true outputs are provided for system interfacing. Temperature and hysteresis trip points are each programmed with a single resistor for tailoring on/off characteristics to match system requirements.

Typical applications include thermal-overload sensing and fan control in power supplies and computing systems, environmental heating controls, LCD display heaters, and process control. The TC07 comes in an 8-pin MSOP, SOIC, and PDIP. In quantities of 10,000, pricing is $0.98 for the 8-pin MSOP version and $0.87 for the SOIC package. ML

***TeleCom Semiconductor Inc.**, 1300 Terra Bella Ave., Mountain View, CA 94039-7267; (415) 968-9241.*
CIRCLE 659

Fast 12-Bit ADC Comes In An SO-8

The LTC1400, with a 400-ksample/s sampling rate, is the industry's fastest 12-bit ADC in an SO-8 package. The LTC1400 converts 0- to 4.096-V unipolar inputs from a single 5-V supply and ±2.048-V bipolar inputs from ±5-V supplies. Integral linearity is ±1 LSB, differential linearity is ±1 LSB, and drift is 25 ppm/°C. Guaranteed ac performance includes a signal/(noise + distortion) ratio of 70 dB, and 76 dB total harmonic distortion at an input frequency of 100 kHz. A three-wire serial port allows compact and efficient data transfer to a wide range of microprocessors, microcontrollers, and digital signal processors. Power consumption is 75 mW from a 5-V source or from ±5-V supplies. ML

***Linear Technology Corp.**, 1630 McCarthy Blvd., Milpitas, CA 95035; (408) 432-1900.* **CIRCLE 660**

16-Bit ADCs Can Sample Up To 5 MHz

The ED2665 ADC provides 16-bit, analog-to-digital performance at sampling rates to 5 MHz. Its cousin, the ED2663, operates at sampling rates up to 3 MHz. They are guaranteed monotonic over their entire operating range. With signal/(noise + distortion) ratio of 85 dB, spurious-free dynamic range of 93 dB, and differential nonlinearity of ±0.5 LSB, they are ideal for CCD and photodiode applications. Six-sided shielding minimizes electromagnetic and electrostatic interference. ML

***Edge Technology Inc.**, 40 Salem St., Lynnfield, MA 01940; (617) 246-3800.* **CIRCLE 661**

Comparators Come In Singles And Duals

The LTC1440 and LTC1442 are single and dual comparators, respectively, with extremely low quiescent current draw (2.8 µA). Both have adjustable hysteresis up to 100 mV, and on-board reference of ±1.182 V, accurate to within 1%. The LTC1441 dual comparator is similar, with no voltage reference. The LTC1440 is guaranteed to draw less than 4.7 µA over the full industrial temperature range. Similarly, maximum current draw for the LTC1441 and LTC1442 is 5.7 µA. The voltage reference can provide more than 100 µA, and drive a bypass capacitor of up to 0.01 µF without oscillation. All three versions operate from a supply voltage of 2 to 11 V. The LTC1440 has a ground pin in addition to V–, enabling dual-supply operation from ±1 V to ±5.5 V Comparator input range extends down to the negative supply rail. The output stages are TTL-/CMOS-compatible, sourcing up to 40 mA and sinking up to 5 mA. The comparators are available in 8-pin PDIPs and plastic SO packages. ML

***Linear Technology Corp.**, 1630 McCarthy Blvd., Milpitas, CA 95035; (408) 432-1900.* **CIRCLE 662**

Chip Set Eliminates Jitter In CRT Monitors

Two ICs from National Semiconductor offer a complete deflection solution for continuous-sync CRT monitors. The LM1292 is a horizontal time-base solution for controlling the CRT horizontal scan rate of continuous-sync video monitors with stringent time-base requirements (763 ps at 125 kHz). The chip contains a frequency-to-voltage converter that controls the frequency tracking of an on-chip voltage-controlled oscillator to the incoming horizontal signal. The device automatically captures the incoming horizontal signal over the frequency range of 22 kHz to 125 kHz with a single set of external components.

By accepting all common computer sync signals without switching between sync sources, the LM1292 eliminates the need for external sync-stripping circuitry. Other features include video mute during resynchronization, undervoltage lockout, and an automatic shutdown latch mechanism that protects against CRT anode overvoltage. The companion part, the LM1295, is a dc-controlled geometry-correction system that synchronizes all output waveforms to the input voltage sync over the refresh-rate range of 50 to 125 kHz, with up to 125 kHz of bandwith for dynamic input signals. The chip provides sawtooth waveforms for East-West pincushion, E-W bow, and trapezoid and parallelogram correction in either positive or negative polarities. For quantities of 1000, unit pricing is $2.75 for the LM1292 and $2.54 for the LM1295. ML

National Semiconductor Corp., *2900 Semiconductor Dr., Santa Clara, CA 95052-8090; (800) 272-9959.* **CIRCLE 663**

High-Integration Phone Interface And Speakerphone

The MC33215 is a highly integrated IC for electronic telephones with speakerphone functionality. It completes ac and dc line terminations, bidirectional 2 - 4 wire conversion, line-length AGC, and DTMF transmission. Speakerphone functions include a half-duplex controller with signal and noise monitoring, and amplification for the base microphone and loudspeaker. The circuit will operate with line currents as low as 4 mA, enabling a phone using the circuit to be paralleled with a conventional phone. Microphone inputs to the circuit are differential while there's standard sidetone cancellation and muting for both microphone and earpiece. Hands-free operation switching depth can be adjusted, as can switch-over and idle-mode timing. The IC is available in either a 52-pin QFP or a 42-pin SDIP. It's priced at $2.55 in 10,000-unit quantities. PMcG

Motorola Inc., *Literature Distribution, P.O. Box 20912, Phoenix, AZ 85036; 1(800) 441-2447, or (602) 303-5454.*
Web: http://Design-NET.com
CIRCLE 664

Low-Power Rail-To-Rail Op Amps Are Versatile

The general-purpose LT1490 dual and LT1491 quad op amps draw only 50 µA per amplifier. The power requirements are unusually flexible, from 2.5 to 44 V for a single supply, or from +11.25 to ±22 V using split supplies. Each amplifier can source or sink 20 mA of current and is stable for all capacitive loads up to 5000 pF. The input common-mode range is from –0.4 V to 44 V. The amps are internally protected for 18 V of reverse supply. Their voltage and current characteristics make the amps suitable for applications in battery-operated handheld equipment, and especially in higher voltage industrial applications. The LT1490 comes in either an 8-lead plastic DIP or SO package. The quad LT1491 is available in 14-pin SO and PDIP packages. ML

Linear Technology Corp., *1630 McCarthy Blvd., Milpitas, CA 95035; (408) 432-1900.* **CIRCLE 665**

Sampling Analog-To-Digital Converter Runs On 1 mW

The SP8538 12-bit ADC consumes a maximum of 1.25 mW at 5 V, or 0.5 mW at 3.3 V. This makes it particularly suitable for battery-powered operation and in remote sensing environments. Its half duplex, digital serial interface accepts analog information with a range of 0 to V_{DD} for one-channel full-differential, or two-channel single-ended operation. Conversion time is 40 µs. Output data is in serial form, while linearity is ±1 LSB and ±3/4 LSB differential. ML

Sipex, *22 Linnell Circle, Billerica, MA 01821; (508) 667-8700.*
CIRCLE 666

Linear Isolation Amplifier Improves Stability

The LIA100 series of isolation amplifiers uses a servo-control loop to compensate for the nonlinear time and temperature characteristics of its LED. As a result, the amplifiers, which contain an optocoupler and two LF356 op amps, are ideal for medical electronics (EEG and ECG circuitry), isolated 4-20 mA converters, motor speed control, and audio signal coupling. The optocoupler features an infrared LED that drives two phototransistors, one in the feedback loop and one that provides an output signal that's linear with respect to the servo LED current. The optocoupler has better than 0.01% linearity and a bandwidth of greater than 40 kHz. Transfer gain stability is 0.005%/°C from –40°C to +85°C. The LIA100 series may be powered from ±5 to ±18 V supplies. Input to output isolation is 3750 V rms. The amplifier comes in a 16-pin SOIC package or DIP. ML

CP Clare Corp., *107 Audubon Rd., Wakefield, MA 01880; (617) 246-4000.* **CIRCLE 667**

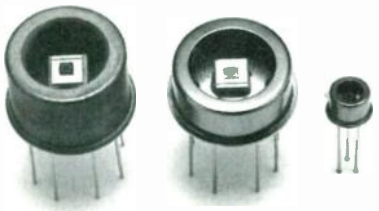
Analog-To-Digital Converter Delivers 15-Bit Accuracy

The HI7191, a 24-bit, sigma-delta ADC, provides measurements accurate to 15 bits over the industrial range of temperatures. Conversion rates from 1 Hz to 2 kHz are programmable. Its on-chip programmable amplifier allows for gains of 1, 2, and multiples to 128. Fully differential analog inputs can be programmed for unipolar or bipolar operation. Noise rejection at 50 to 60 Hz is better than –120 dB when the notch is programmed to a subharmonic of this frequency. Input/output is via a three-wire serial interface and is fully compatible with National, Intel, and Motorola microcontroller I/O standards. The HI7191 comes in 20-pin PDIP and SOIC packages. ML

Harris Corp., *P.O. Box 883, Melbourne, FL 32902.* **CIRCLE 668**

PIN Diodes Emit Near Infrared

The G5851 and G5852 InGaAs PIN diodes have extended cutoff wavelengths of 1900 nm and 2100 nm, respectively, for near-infrared spectrophotometry and measurement applications. The G5851 photodiode

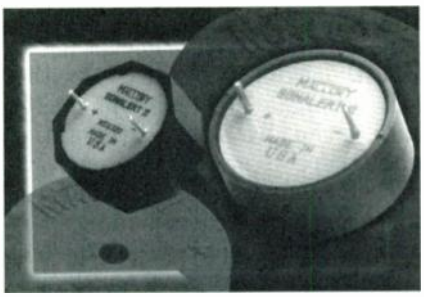


offers a typical photosensitivity of 1.1 A/W at a wavelength of 1750 nm. Dark current is 100 nA at a reverse voltage of 1 V, and cutoff frequency is 15 MHz. The G5852 reaches peak sensitivity at 1950 nm. Connecting a 500-kΩ shunt resistor across the 80-pF terminal capacitance of either device results in high sensitivity and low noise. The noise equivalent power is just 2×10^{-13} W/$\sqrt{\text{Hz}}$ at 1750 nm while the normalized detectivity is 5×10^{-11} cm$\sqrt{\text{Hz}}$/W at 1750 nm. The diodes come in a 3-pin TO-18 package with a borosilicate glass window. They can be used in temperatures from –40 to +85°C. Versions of the G5851 also are available with integral thermoelectric coolers. ML

***Hamamatsu Corp.**, 360 Foothill Rd., P.O. Box 6910, Bridgewater, NJ 08807; 1 (800) 524-0504.*
CIRCLE 669

Audio Signal Devices Have Boosted Decibel Levels

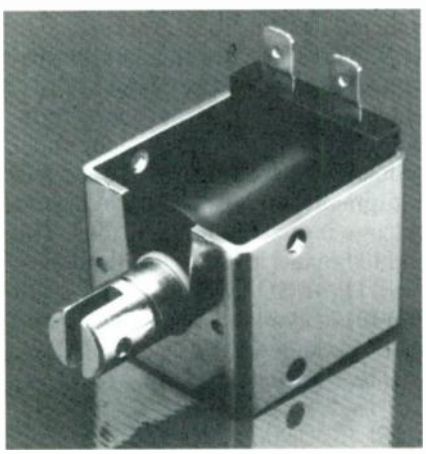
Three devices added to the Mallory Sonalert II line of piezoelectric signal generators from North American Capacitor Co. produce either continuous, fast-pulse, or slow-pulse extra loud sounds for applications such as fire and security alarms, call buzzers, clocks, cash registers and other POS equipment, and medical and electrical systems. Housed in a case measuring 10.5 mm high and 23 mm in diameter, the MSR516N, MSR516NP, and MSR516NJ supply a minimum sound-pressure level of 85 dBA at 12 V dc from a distance of 2 ft. Operating voltage range is 5 to 16 V dc at +65°C, and maximum current draw over the voltage range is 3 to 16 mA. All three versions have a built-in oscillator circuit and are suitable for wave soldering when ordered with the sound emission hole covered with a wash label. ML



***North American Capacitor Co.**, 7545 Rockville Rd., Indianapolis, IN 46214; (317) 273-0090.*
CIRCLE 670

Linear Solenoids Have One-Piece Box Frame

The BS series of linear solenoids from Dormeyer Industries are now available with a one-piece frame design that reduces cost while enhanc-



ing performance. The coil can be encapsulated in either thermoset or thermoplastic materials for a variety of applications. Standard terminals are 0.250-in. The BS series comes with both dc- and ac- input versions. The dc-input intermittent-duty model delivers 40 oz. of pull at 0.250 in., and the ac-input intermittent-duty version produces 32 oz. of pull at 1.00 in. Continuous-duty units also are available, as is a magnetic-latching option for energy-efficient applications. Data sheets and engineering samples are available. ML

***Dormeyer Industries**, 6585 N. Avondale Ave., Chicago, IL 60631-1521; (312) 775-3600.*
CIRCLE 671

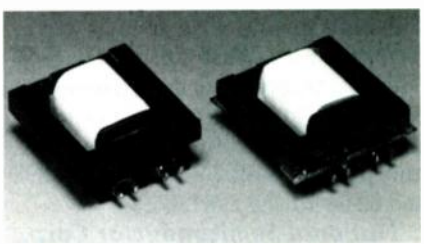
Brilliant Blue LEDs Added To Families

Dialight's blue LEDs, part of the company's 249 Series, are available in cylindrical or stovepipe cap versions with forward voltages of 3, 3.5, 10, 14, and 28 V at 10 mA. They're also available in the 507 Series, which are designed for use with holders and clips. Housings, cartridges, and holders for both series are made of black anodized aluminum. Lens caps consist of high-impact plastic. Pricing is $7.85 each per 1000 for the 249 Series, and $6 each per 1000 for the 507 Series. Delivery is 6 weeks. PM

***Dialight Corp.**, 1913 Atlantic Ave., Manasquan, NJ 08736. (908)223-9400; fax (908) 223-8788.* **CIRCLE 672**

Transformer for PCMCIA Keeps Low Profile

The SPT-032, designed specifically for use in V.34 modems (28.8 kbits/s), measures only 0.66 by 0.66 by 0.172 in. The maximum toe-to-toe dimen-

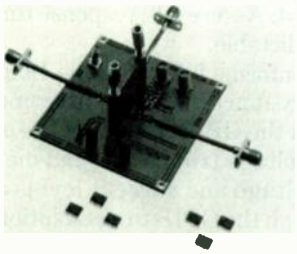


sion across the leadframe is 0.8 in. The leadframe is arranged so that the part can be placed in a square hole in a pc board. It also is available in a semi-gullwing configuration. This 1:1 transformer has an impedance of 600 W. The Hipot rating is 1500 V rms for a minimum time of 1 minute. Pricing for the transformer is approximately $4.50 each in production quantities. PM

***Prem Magnetics Inc.**, 3521 North Chapel Hill Rd., McHenry, IL60050; (815) 385-2700; fax (815) 385-8578; Internet: http://www.premmag.com*
CIRCLE 673

RF Front End Knocks Down Telephone Costs

The UAA line of RF front-end ICs allow telephone manufacturers to design better, smaller, lighter, and more power-efficient portable devices. The UAA2067G, -2077AM, and -2077BM devices reduce component, assembly, and alignment costs typically present when separate low-noise amplifiers



and mixers are used. Thanks to use of their dual-balanced, quadrature mixers in lieu of ceramic filters, the UAA line typically provides more than 30 dB of image rejection on-chip. Also integrated into the UAA2067G are RF and IF VCOs, a single-sideband upconversion mixer, and RF output drive stage for the telephone's transmitter section. The VCOs require only the addition of simple resonant circuits.

The UAA2077AM (for the DECT telephone) and the UAA2077BM (for the DCS1800 telephone) each have a down-conversion mixer for use in closed-loop transmitter architectures. The 2077s provide an overall noise figure of 4.3 dB. The chips operate at voltages down to 3.15 V. Typical standby current is 0.2 μA. All three ICs feature extensive on-chip buffering of local oscillator signals to ensure minimal pulling of the local oscillator frequency. Price for the UAA2067G, which is packaged in a 32-lead low profile quad flat pack, is approximately $5.15 in high volume. The 2077AM is $2.22, and 2077BM $3.50, in high volume.

Philips Semiconductor, *P.O. Box 218, 5600 MD, Eindoven, The Netherlands; phone (+31) 40 272 20 92; fax (+31) 40 272 48 25.* **CIRCLE 674**

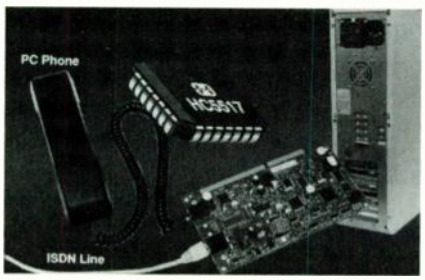
LAN Transceivers Whittle Down Time to Market

The FlexPHY family of high-speed local-area-network (LAN) transceivers offer OEMs a line of fully interchangeable physical-layer modules. Manufacturers may quickly select between 10Base, 100Base-TX, -VG, -T4 and -FX based technologies. A LAN system node can be initially configured as 10Base, yet be easily upgraded to any of the 100-Mbit/s technologies simply by switching modules. The seamless interconnect complies with IEEE 802.E and 802.12 standards, CISPR-22B EMI requirements, and the European CE Mark. The MD6126 transceiver (100Base-TX) sells for $82.50 in quantities of 1000. LG

Valor Electronics Inc., *9715 Business Park Ave., San Diego, CA 92131; (619) 537-2500; fax (619) 537-2525.*
CIRCLE 675

SLIC Solution Cuts Cost For ISDN Modems

The HC5517 subscriber-line interface circuit (SLIC) will reduce costs



in ISDN modems by approximately 30% in Internet-driven applications. It supplies the ringing and supervisory signals that allow standard voice phones to operate from either ISDN modems or wireless local-loop terminals. The device links to a conventional COMBO chip (such as the company's CD22354A) inside the modem, and the modem's communications controller. Voltage to the chip (-80 V) to derive the ring signal is supplied by the modem card. When the phone is off hook, the controller lowers battery voltage to conserve power. Externally, the HC5517 connects to one or more telephones via the standard POTS tip and ring, two-wire interface. It can handle up to a 3-REN (ringer equivalent number) bell load. The HC5517 comes in a 28-lead PLCC or SOIC package, and in 0°C to 75°C or -40°C to +85°C versions. It can be supplied in tape and reel. The PLCC 0°C to 75°C version goes for $5.29 each in quantities of 1000. LG

Harris Corp., *Semiconductor Sector, P.O. Box 883, Melbourne, FL 32902; (800) 4-HARRIS, ext. 7616.*
CIRCLE 676

Low-Noise Amplifier Boosts Wireless Receivers

The SM-515101 low-noise amplifier (LNA) provides the high-intercept figure required for wide-dynamic-range receiver applications. It features a noise figure of 1.4 dB (typical) and 23 dB of gain over a frequency range of 2.1 to 2.7 GHz. Its third-order intercept point is typically 19 dBm, and it provides 40 dB of reverse isolation. Typical supply voltage is 3.6 to 5 V. The amplifier is supplied in an 8-lead plastic SOIC package. The cost of the SM-515101 is $4.70 in quantities of 10,000. LG

Samsung Microwave Semiconductor, *1530 McCarthy Blvd., Milpitas, CA 95035; (408) 433-2222; fax (408) 432-3268.* **CIRCLE 677**

Monolithic Mixers Hike Dynamic Range

GaAs MMIC passive mixers developed by M/A COM feature a patented, floating-FET topology that provides high intermodulation performance without the need for dc biasing. Designed for 900-MHz to 1.9-GHz work, these mixers serve well in such transmitting and receiving applications as modulation and demodulation for base station and portable systems. They offer respectable conversion loss over a wide range of power levels, as well as stable performance over local oscillator load and temperature variations. The typical input third-order intercept point for the low-signal level MD54-0005 (900-MHz version) and MD54-0006 (1.9-GHz version) is 18 dBm, with +5-dB LO drive. The MD54-0003 (1.9 GHz) and MD54-0004 (900 MHz) high-level mixers provide an input third-order intercept of 24 dBm, with a +13-dBm LO drive. These SOT-25 mixers are priced at less than $1 in production quantities. LG

M/A COM, *1011 Pawtucket Blvd., Lowell, MA 01853. (508) 442-5000; fax (508) 442-5350.* **CIRCLE 678**

Ergonomic Connectors Are Built With Engineering-Quality Plastic

The series 405 connectors blend elegance, ergonomic styling, and high technical performance within lightweight engineering-quality plastic housings. These features,combined with the high chemical and temperature resistance and the reliable push-pull self-locking mechanism, make the connectors suitable for applications in avionics, test and measurement, medical electronics, and data acquisition in both the commercial and military range. Because they can withstand thousands of medical sterilization cycles, the plugs are particularly well suited for sensor/actor cables in medical systems that require sterile conditions.

The series 405 products use the same high-quality contacts and insulators as do other W.W. Fischer connectors. Therefore, the series 405 is interchangeable with the metal-body series 105, which also comes with up to 27 contacts. This includes mixed-contact arrangements for signal and high voltage, as well as coaxial and fiber-optic inserts. The series 405 connectors are available with or without integral EMI/RFI shielding. *LM*

W.W. Fischer SA, *Connecteurs Electriques, CH-1143 Apples, Switzerland, phone: +41 21-800 37 11; fax: +41 21-800 39 24.* **CIRCLE 500**

High-Speed Card Frees PC From Communications Processing

Pushing data through at 3.6 Mbits/s, the latest PC communications-processor card from HTEC is 12 times faster than its predecessor. The HTEC iPC486-X Intelligent Peripheral Controller, which was originally designed for the financial service sector, is now generally available. It enables systems integrators to free the host PC of complex communications-handling tasks.

The card is based on the 486SX/DX/DX2/DX4 processor. Two of four serial ports HTEC will customize the board's architecture and bus interface (16-bit ISA is standard) so that it can be used as a drop-in replacement for existing industry-standard offerings (such as RS-232, RS-423, RS-485, or X.21 interfaces, and as DTE or DCE). This gives users the benefit of higher speed with no need for software re-development. On-board memory is 0.5 Mbytes standard and 1 Mbyte optional, and is SRAM dual-ported to the local and host processors. The PC processor accesses memory through configurable window sizes of 16 kbits, 32 kbits, 64 kbits, 128 kbits, or 1 Mbit. The range of communications controllers for the PC spans from low-cost cards to multichannel high-speed controllers. *LM*

HTEC Ltd., *303-305 Portswood Rd., Southampton, Hampshire, SO17 2LD, U.K.; phone: +44 1703 581555; fax: +44 1703 671173.* **CIRCLE 501**

Programmable Power Supply Offers Fast Output Changes

A new GPIB-controlled programmable power supply from Thurlby Thandar Instruments offers fast response on its two 0-to-32-V outputs. Although the TSP3222H supply is based on a series-regulator design, it also incorporates active circuitry that sinks current when needed to ensure fast output changes, regardless of the load current. As a result, response times to bus commands are predictable.

The GPIB interface conforms fully with the IEEE-488.2 specification. Every function of the instrument can be controlled through the GPIB, including the output configuration, overvoltage trip points, and meter damping. The output voltage and current levels are able to be read back through the GPIB to a resolution of 12 bits.

Both of the two outputs on the TSP3222H provide 0 to 32 V at 0 to 2 A. They are fully independent and isolated to 300 V. Programmable internal switching can link the two outputs in series or parallel to provide voltages of up to 64 V or currents of up to 4 A. An LCD display shows the voltage and current set levels for both outputs simultaneously.

The compact case is half-rack width and 3U height. A National Instruments LabWindows device driver is available as an option. *LM*

Thurlby-Thandar Instruments Ltd., *2 Glebe Rd., Huntington, Cambs PE18 7DX, England; phone: (01480) 412451; fax: (01480) 450409.* **CIRCLE 502**

Genrad Test Fixtures Incorporate ESD Protection

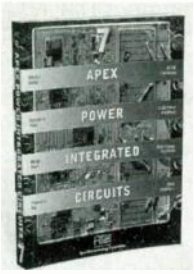
Test fixtures incorporating electrostatic-discharge (ESD) protection are now available from The Peak Group for use with the Genrad 2272 and 228x automatic test systems. The fixtures use Peak's recently introduced antistatic technology, in which the vacuum plate is made from an electrostatically dissipative material and can be grounded via a plug in the base of the fixture.

They're designed for vacuum operation with the test head hinged open, and give users easy access to the probe plate and interface wiring. Disassembly and reassembly can be varied out with no effect on the seal integrity. Four different fixture-kit sizes are available that cover various board sizes measuring up to 690 by 445 mm.

All kits include 1024 interface points. While units are normally available in kit form, they also can be custom built to users' requirements. *LM*

The Peak Group, *Peak Test Services Ltd., 152A Front St., Chester-le-Street, County Durham DH3 3AY; phone: (01462) 670877; fax: (01462) 480294.* **CIRCLE 503**

Revised Databook Includes New PWM Amplifiers



Apex Microtechnology has issued the 7th edition of its *Apex Power Integrated Circuits Data Book* highlighting the new hybrid PWM amplifier product line, updated data sheets on their hybrid 6 and 22 W dc-dc converters, and the entire library for their 75 high-power and high-voltage amplifiers. There's also a reorganized and expanded applications section. The accessories section of the databook includes new package outlines and a complete listing of accessory vendors. The databook can be requested, free-of-charge, by calling 1-800-546-APEX (2739) or through the e-mail to ProdLit@TeamApex.com. The company's web site is located at http://www.teamapex.com. PMcG

CIRCLE 505

Digital Oscilloscope Brochure Offers Time-Saving Tips

LeCroy's (Chestnut Ridge, N.Y.) new brochure suggests methods for design and test engineers to get their job done faster and more accurately using digital oscilloscopes. Highlighted in the discussion is a color CRT display with a 9-in. viewing area that's used in place of the typical low-power flat-panel displays. An "Analog Persistence" mode uses the brightness of each pixel to closely emulate the display of a waveform as it would be seen on an analog scope. The brochure also goes into the how the new scopes have improved complex-signal capturing, and their analysis and measurement.Call 1 (800) 453-2769 to obtain the brochure. RE

CIRCLE 506

Catalog Lists Appliance And HVAC Relays, Circuit Breakers

Components well-suited for use in high-volume appliance and HVAC (heating, ventilating, and air conditioning) applications are listed in Siemens Electromechanical Components' latest 40-page catalog. Included are thermal circuit breakers, and both pc-board-mount and panel-mount relays. Current ratings for the circuit breakers, which include rocker-actuated and push-to-reset, range from 0.5 to 20 A. Relays, both open-frame and enclosed, provide maximum contact ratings from 1 to 30 A. A selector guide section offers basic product information for quickly matching a product to a particular application. To get the free catalog, contact the Marketing Communications Dept., Siemens Electromechanical Components Inc., Potter & Brumfield Products Div., 200 S. Richland Creek Dr., Princeton, IN 47671-0001; fax (812) 386-2072; e-mail: info@ae.sec.siemens.com. RE

CIRCLE 507

Brochure Details Mod/Demod Products

Stanford Telecommunications Inc.'s latest brochure presents a quick overview of its modulator and demodulator ASICs and board-level assemblies for hybrid fiber/coax (HFC) upstream CATV systems. The four-page brochure explains the company's overall capabilities in the interactive cable transmission and reception arena. Discussed are the STEL-1108 BPSK/QPSK digital modulator ASIC, and several head-end demodulator boards, including the new STEL-9244 burst demodulator assembly. For a free copy, call (408) 745-2660; fax (408) 541-9030; e-mail: tpg.marketing@stelhq.com. RE

CIRCLE 508

Surge Suppressors Highlight Comprehensive Catalog

Surge suppressors, offered in ratings of 600, 1500, and 5000 W dominate a new catalog put out by Sussex Semiconductors Inc.,Farmingdale, N.J. Standoff voltages (V_{so}) range from 5 to 400 V. Custom products, such as assemblies rated from 300 to 60,000 W and 5 to 1500 V_{so}, as well as low-capacitance designs, also are available. Maximum ratings and electrical characteristics are detailed. To obtain a copy of the catalog, call (941) 768-6800; fax (941) 768-6868. RE

CIRCLE 509

Interface Technology Catalog Acts As A Reference Tool

A new catalog introduced by Lutze Inc., Charlotte, N.C., is designed to be a comprehensive source for interface components used between the control and sensor/actuator levels. The catalog strives to be a reference tool that assists engineers in selecting the optimal products for a given application. One section defines and explains commonly used interface-technology terminology. The product section features different interface modules, 24-V power supplies and surge suppression for contactors, solenoid valves, and three-phase motors. For further information, contact Lutze at (800) 447-2371 or (704) 357-8835; fax (704) 357-8836. RE

CIRCLE 510

IPC's Most Widely Read Document Now On CD-ROM

The Institute for Interconnecting and Packaging Electronic Circuits (IPC) announced that its most used document, "IPC-A-610B: Acceptability of Electronics Assembly," is now available on CD-ROM. In this format, the association (located in Northbrook, Ill.) for the first time can offer 100% full-color photographs and schematic illustrations with the touch of a keystroke. Enhanced features include "bookmark" icons and a search engine. For more information, or to order the CD-ROM, call IPC at (847) 509-9700; fax (847) 509-9798; e-mail: URL:http://www.ipc.org. RE

CIRCLE 511

LANscape Fiber-Cabling Solutions Highlight Brochure

Siecor Corp.'s new brochure, "LANscape Fiber Cabling Solution for Premises Networks," reviews the LANscape program, which involves tip-to-tip products and design-through-installation service and support for various situations. The program includes a comprehensive set of fiber-optic products and services to simplify installation. To obtain the brochure or for more information, contact Siecor at 1 (800) 743-2675, or at http://www. siecor.com. RE

CIRCLE 512

In the Dec. 16, 1996 issue, an editorial by Executive Editor Roger Allan on "Engineering And Social Responsibility" elicited a number of responses:

Your most recent editorial made some particularly good points. Not nearly enough is being said about an engineer's responsibility towards the "larger scenario." We are spending entirely too much time and effort on meeting deadlines without carefully analyzing the "bigger picture." The result is not just shoddy products and disillusioned customers, but we have a real opportunity to make a negative contribution to the well-being of our customers and their environment. I am not sure that we have the information available to make the best trade-offs to optimize the effects of our work on the "larger scenario."

My recent job assignment is an example of the frustration in visualizing the "bigger picture." I am to make one of our products compliant with IEC1000-3-2 which requires the addition of some extra circuitry to minimize the amplitude of higher harmonics of the main current waveform. This extra circuitry is not 100% efficient, so the result of making the waveform more friendly to the electric utility provider will of course increase the amount of electricity the product consumes. The IEC1000-3-2 specification does not concern itself with efficiency and there are no published guidelines on making trade-offs between main harmonic reduction and extra power losses. Did the IEC-3-2 authors not see this "bigger picture" when they created their spec? Did they envision that reducing main harmonics could easily increase power consumption by as much as 10%? If we engineers are to make responsible trade-offs in our designs, we need to be able to calculate the social impact of a given level of mains harmonic reduction versus a given level of extra power losses. At this point, I do not have the information available to perform this calculation.

James Knox
via e-mail

I found your editorial very interesting. I think you will find this message to Professor Whalen interesting.

Sandy Rotter
via e-mail

The following excerpted passages are from a message from Mr. Rotter to various people, including Professor Whalen at the State University at Buffalo (SUNY-Buffalo), regarding methodologies to predict the cost benefits of EMC protection from semiconductor chips.

I have attached a file of an INSPEC search on the subject of EMC and on-chip or IC. The results are not as good as I thought... Your interest in other areas of electrical engineering is clearly seen in the search. I understand that the lack of government and private funding is only part of the problem as there are also too few students interested in the subject.

....

I believe all products that contain ASICs have to clearly address the issue of EMC up front where the greatest scales of economy are. By the time one gets to the discrete area of a product, costs of EMC protection are outweighed by the value added.

....

It is ironic that after the demise of Citizens Band Radio and American companies like Motorola, E.F. Johnson, and Telex/Hygain losing millions of dollars, our lawmakers are blaming the CB phenomena on all consumers' EMC problems. Engineers will have to take the social responsibility for loss of civil liberties and anarchy if Senate Bill 2025 is enacted. I think S2025 loses sight of the presumption of innocence. Before individual rights are violated, it is the states' responsibility to take all precautions.

I would like to thank *Electronic Design* for writing about our microrelays *(July 8, 1996, p. 31)*. As a result, I have received well over 100 calls from interested commercial and academic parties. Many of these have turned out to be valuable contacts which will enhance our ability to commercialize these devices.

Prof. Paul M. Zavarcky
Northeastern University

You're welcome, and keep up the good work.

I have been a long time reader of *Electronic Design* and look forward to every issue. Your new look is just great. I make this statement with a bit of knowledge. You see, one side of my family has been in the magazine business for many years (Challenge Pubs, Canoga Park, Calif. and Jess Pubs, Newbury Park, Calif.) as well as being a SEE and a "frustrated amateur writer" actively working in the prepress industry for Autonomic, now called Autonomic Info. International.

I have one big complaint, however. I always looked forward to PAGE 8 in every issue, "40 Years Ago." This was one of my favorite columns and now it's gone! Do us a favor and put it back in, please!! I truly miss it.

August Hockey
Sr. Systems Eng.
Autonomic Info. Intl.

Don't fret! "40 Years Ago" has been relocated to our popular QuickLook section. In addition, you'll be able to see it on our web site in the near future. Stay tuned for more details.

Corrections

In the Nov. 4, 1996 issue, an error occurred when laying out captions with their respective art pieces for the article *"Surge Protection For Mobile Communications."* The caption for Fig. 1 should have gone with the opening photo, the caption for Fig. 2 should have gone with Fig. 1, the caption for Fig. 3 should have gone with Fig. 2, and the caption for Fig. 3 should have read: "To protect the CPU and I/O chips from transients entering the system from the power or data lines, the best strategy is to divert the transient current away from the sensitive semiconductor components. This can be done with separate protection for the signal interfaces and the power bus." We apologize for the confusion.

In the Dec. 2, 1996 issue, an incorrect phone number was given for Tra-Con, an adhesives manufacturer in Bedford, Mass., on page 148. The correct number is (617) 275-6363. We apologize for the error.

The phone number listed for Silicon Microstructures Inc., Fremont, Calif., in the Dec. 16, 1996 cover article, *"Low Pressure Sensor Opens Wide Applications Frontier,"* was in error. The correct number is (510) 668-7000.

Giving Workers A Better Understanding Of What They Need To Know

Michael Sciannamea

Most of us are familiar with the phrase "The Future is Now." These words definitely ring true today with the current globalization of markets, the continued expansion of information technology, and the formation of virtual organizations and businesses. However, most of us still have the attitude that we'll worry about the future when it directly affects us, especially at our jobs. In the meantime, we'll continue to work in the same way we've always done.

But that way of thinking may very well be obsolete, and sooner than we might think. According to one prominent educator, the continuous expansion of our technically-complex industrial society means that there will be a primary focus on the application of technology to develop and manufacture new products. To keep pace with this path of evolution, the effective use of technology to improve the design and manufacture of these new products is sorely needed. The question that has to be addressed is: Who will implement these new processes?

Dr. Jay D. Pinson, a former Dean of the College of Engineering at San Jose State University, San Jose, Calif., believes that in the future, the workplace will be one of constant change, changing as the business environment and the technology changes, and as new products are developed. As a result, workers, especially engineers and technicians, must be better educated and must have the ability to undertake numerous tasks. What this means for today's worker is that continuous education and training will be required in order to maintain employment in the future—and Dr. Pinson says, that the future is now.

To provide the education and training that will be needed to cope in the workplace of the future, Dr. Pinson has founded The Pinson Institute. Located in the heart of Silicon Valley, The Pinson Institute offers both industry and individuals what has been billed as "an accelerated education system" to help those who have the desire to expand their knowledge base to meet the demands of the high-tech world. The programs at the institute focus on what Dr. Pinson feels are the five most critical areas of technology that require education and training: Microelectronics, Semiconductors, Software, Telecommunications, and Networking. The changing dynamics of the global economy and the rapid introduction of new technological processes to produce innovative products demands that workers in the technological fields must keep up-to-date if they plan to succeed, much less stay afloat, in the workplace.

Constant Learning

For generations, the process of learning ended when students graduated from colleges or universities. Those graduates then applied their knowledge to their jobs, and most likely did the same thing after 20 years on the job as they did on their very first day. However, as Dr. Pinson can relate from his intimate knowledge and experience as an educator, that predictability no longer is the case.

Workers must keep up-to-date if they plan to succeed, much less stay afloat, in the workplace.

Shortly after leaving San Jose State in 1994, Dr. Pinson took the position of Director of Education and Technology for SEMI (Semiconductor Equipment and Material International). During his time at SEMI, he was responsible for developing and offering educational, technology, and training programs for member companies in such locales as Europe, Russia, the Far East, and the United States. Dr. Pinson says that he saw firsthand how other governments and companies in those countries worked together to provide the education and training needed to assure that skilled people are available at all levels of industry, especially in the expanding and changing microelectronics and semiconductor industries. In fact, he feels that he learned as much as he taught. "I should have paid SEMI a tuition," laughs Pinson.

Pinson developed and offered a Transitional Educational Program for unemployed engineers and scientists in the San Francisco Bay area to assist them in making the transition into the semiconductor industry. The program was conducted over a period of five evenings a week for six weeks. Taught at the graduate level, the Transitional Educational Program also gave homework and exams. The Pinson Institute expands on that idea by offering the same type of program to employed professionals in the semiconductor industry. "You are never too old, and it is never too late to learn," says Pinson.

Many engineers find it difficult to stay current in a specific field, especially with the state of constant change in technology. In most colleges of engineering and science, students expect the faculty members to have a basic knowledge and teaching ability in every area of the latest technology. And Dr. Pinson feels that process should continue. However, there is a great need to find other ways of providing the necessary education and training in the latest technologies for engineers to maintain the required

skills to keep up with these changing industries.

Specific courses of study at The Pinson Institute include a Software Technology Engineering Program, a Semiconductor Technology Engineering Program, and a host of short (one to five day) courses that cover a variety of semiconductor technologies. "There are two types of workers in the high-tech world—engineers/scientists and technicians. What I'm attempting to do is to accelerate the learning process," says Pinson. He adds that the courses were designed to assist people and corporations in learning the latest information in these technologies, and to rapidly apply that knowledge into the workplace. "Continuous learning has become a part of our daily life," says Pinson, "and that especially holds true when it comes to technology."

Dr. Pinson's solution was to develop a new educational system that provides the following:

New Technology Education and Training—As new technologies develop, so too must education and training be offered to the workforce of these new industries and jobs.

Continued Education and Training—The evolving complexity of the workplace demands an increase in skills. Learning new skills and technologies will be constantly required of the workforce.

Transitional Education and Training—With the effects of downsizing and workforce reductions, special educational programs are needed to assist people in making the transition to expanding industries.

For instance, the Semiconductor Technology Education Program, a six-week course, focuses on a fully-developed list of modules, which generally require 20 hours of classroom instruction: Process Technology, Device Physics, Electronic Materials, Metrology, Controls and Automation, and Embedded Systems. (The program has been approved for graduate credit for the Masters of Engineering by the College of Engineering at San Jose State University.) Pinson believes that semiconductor technology is an essential area of study. "The electronics industry, fed by the semiconductor industry, is growing at up to 15% a year, and will continue into the next century," he says. Pinson cites an example of a chip made in Asia that can be used as replacement for a chip made in the United States with similar performance. Pinson adds, "Common manufacturing tool sets are now used in producing semiconductors throughout the world."

Continuous learning is a part of our daily life, and is especially true when it comes to technology.

To emphasize that point, Dr. Pinson developed Technology Short Courses that focus mainly on semiconductors. Some of the areas covered include process technology, lithography, metrology, yield management, and embedded microprocessors. Pinson maintains that engineering and technical schools don't cover areas like process technology, and there is a great need for knowledge in this particular area.

However, semiconductor technology is not the only area where engineers and technicians require constant re-education. There are more companies today looking for people who have expertise in software engineering. Pinson says that skill in areas such as control interfaces, user interfaces, and Unix and C programming languages will give people a leg up on other potential job candidates in their employment marketability.

What it all boils down to is that those who have the desire to succeed in the workplace of the future must have the ability to learn new skills, and to apply them. Pinson says that he shares the same basic philosophy with U.S. President Bill Clinton's idea that education will help build the bridge to the 21st Century.

Narrowing The Focus

Pinson feels that constant re-education is crucial for engineers and technicians. "To perform a skill effectively, you must continue to learn," he says. Dr. Pinson emphasizes that no one, especially those in the high-tech industries, can learn the newest processes all at once. "My program is basically one of focusing on a few things, and learning to do them well," he notes.

As new technologies are created, developed, and applied, more education and training must be readily available to the workforce to meet the needs of those new industries and jobs. And it's exactly this kind of attitude, Dr. Pinson believes, that must be commonplace for both industry and individuals to keep up with the technological advances of the global marketplace.

But not all of this learning can take place in a classroom. "I have all the white shirts I need," Pinson says. One of his chief goals is to bring education to the workplace itself. The Pinson Institute now offers on-site classes for companies in Silicon Valley, however he aims to bring his programs into such technological hotbeds as Austin, Texas, and Boston, Mass., as well as the rest of the country. He also plans to put courses on videotape, CD-ROM, and desires to use the Internet in some capacity by developing a World Wide Web site. Pinson will be introducing his CD-ROM entitled "Process Technology and Device Design" at the Semicon West conference this July.

In addition to the education and training programs in technology, business, and management that The Pinson Institute offers at its own location as well as off-site classes, it also will offer consultant services in leading areas of technology. The initial programs and courses have already begun, and they focus on the areas of microelectronics, semiconductors, software, and telecommunications. Advanced technician and field engineering programs also are in the planning stages. "Anyplace there's a need, we'll try to address it," says Pinson.

For further information on The Pinson Institute and its programs, contact Dr. Jay D. Pinson at 3425 S. Bascom Ave., Suite B, Campbell, CA 95008-7006; (408) 559-3100; fax (408) 558-8092.

Michael Sciannamea is chief copy editor at Electronic Design. He may be contacted at 611 Route 46 W., Hasbrouck Heights, NJ 07604; (201) 393-6024; fax (201) 393-0204; e-mail: mikemea@class.org.

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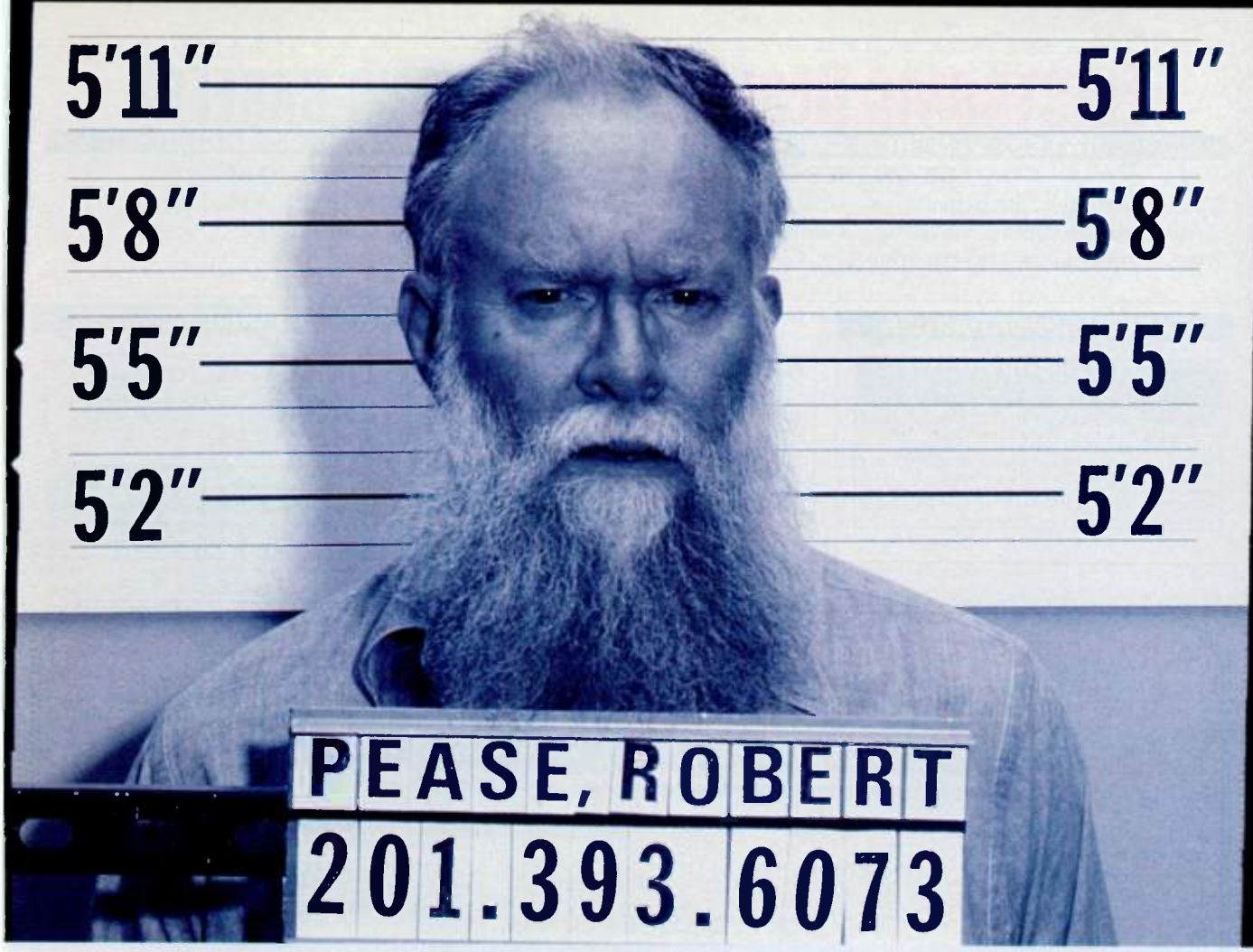

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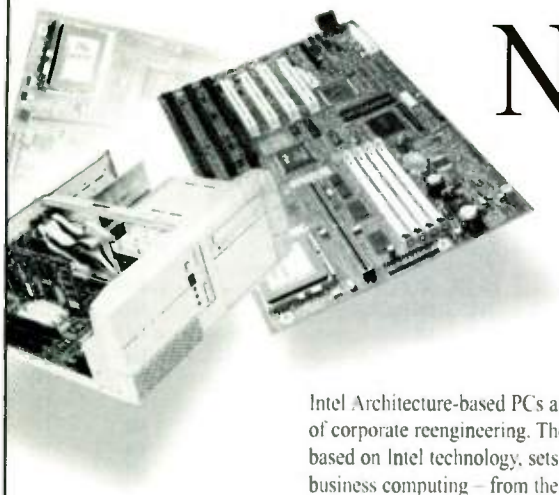

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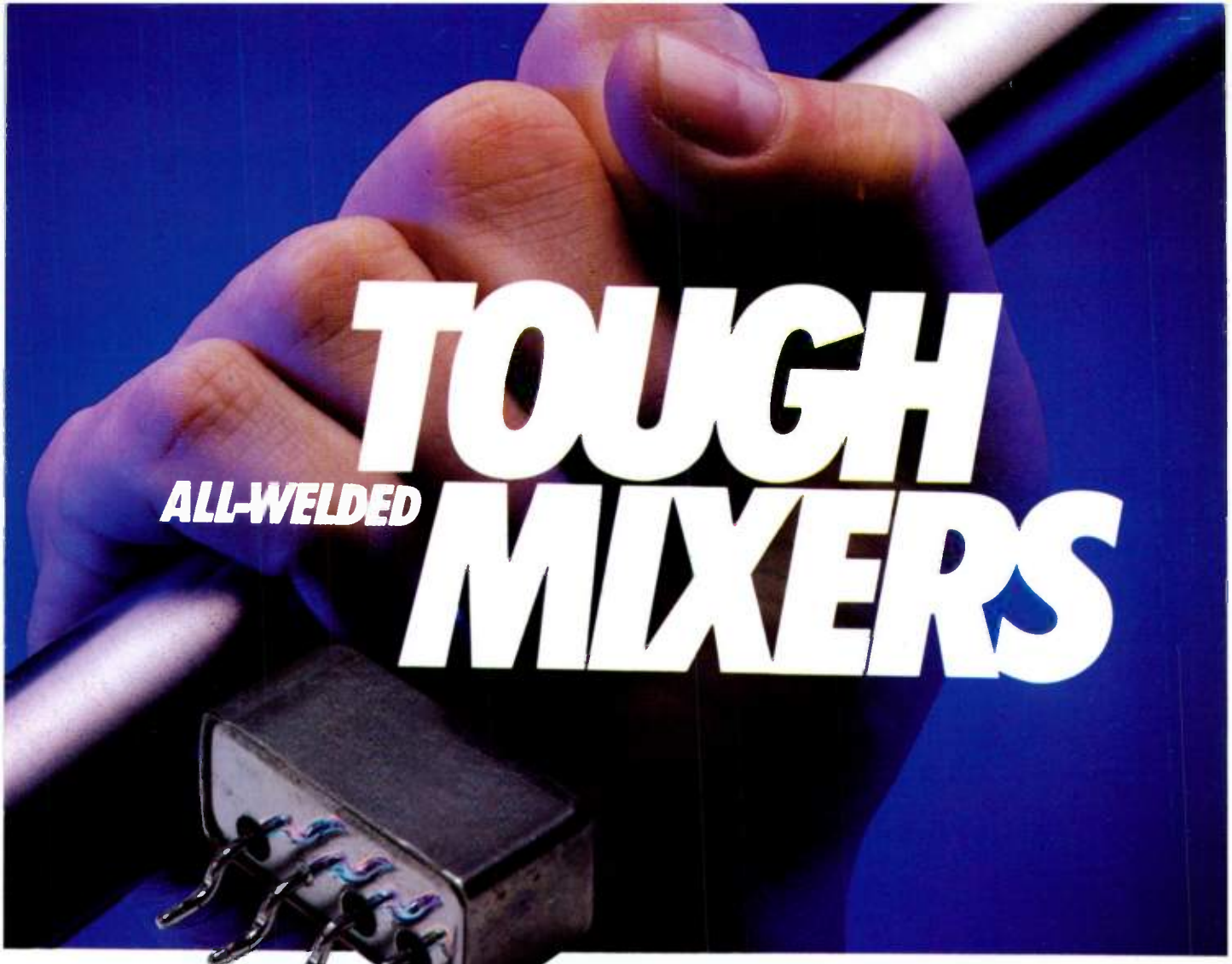

SURFACE-MOUNT or PLUG-IN FROM $3.95 (10 qty)

Expose Mini-Circuits' TUF-mixers to 250°C for five minutes, or to the extreme shock and vibration stresses of MIL-M-28837, or to 200 cycles of thermal shock from -55° to +100°C...they'll survive without any change in specs. They are mighty tough mixers!

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TUF-Ultra-Rel™ mixers are guaranteed for five years and boast unprecedented "skinny" sigma (δ) unit-to-unit repeatability as shown in the Table.

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5-YR. GUARANTEE

with extra long life due to unique HP monolithic diode construction, 300°C high temp. storage, 1000 cycles thermal shock, vibration, acceleration, and mechanical shock exceeding MIL requirements.

SPECIFICATIONS

Model	LO Power (dBm)	Freq. LO/RF (MHz)	■ Conv. Loss (dB) $\bar{X}$	δ	Isol. L-R (dB)	Price,$ Ea. 10 qty
TUF-3	7	0.15-400	4.98	0.34	46	5.95
TUF-3LH	10		4.8	0.37	51	7.95
TUF-3MH	13		5.0	0.33	46	8.95
TUF-3H	17		5.0	0.33	50	10.95
TUF-1	7	2-600	5.82	0.19	42	3.95
TUF-1LH	10		6.0	0.17	50	5.95
TUF-1MH	13		6.3	0.12	50	6.95
TUF-1H	17		5.9	0.18	50	8.95
TUF-2	7	50-1000	5.73	0.30	47	4.95
TUF-2LH	10		5.2	0.3	44	6.95
TUF-2MH	13		6.0	0.25	47	7.95
TUF-2H	17		6.2	0.22	47	9.95
TUF-5	7	20-1500	6.58	0.40	42	8.95
TUF-5LH	10		6.9	0.27	42	10.95
TUF-5MH	13		7.0	0.25	41	11.95
TUF-5H	17		7.5	0.17	50	13.95
TUF-860	7	860-1050	6.2	0.37	35	8.95
TUF-860LH	10		6.3	0.27	35	10.95
TUF-860MH	13		6.8	0.32	35	11.95
TUF-860H	17		6.8	0.31	38	13.95
TUF-11A	7	1400-1900	6.83	0.30	33	14.95
TUF-11ALH	10		7.0	0.20	36	16.95
TUF-11AMH	13		7.4	0.20	33	17.95
TUF-11AH	17		7.3	0.28	35	19.95

*To specify surface-mount models, add SM after P/N shown.

■ $\bar{X}$ = Average conversion loss at upper end of midband ($f_U/2$)
δ = Sigma or standard deviation

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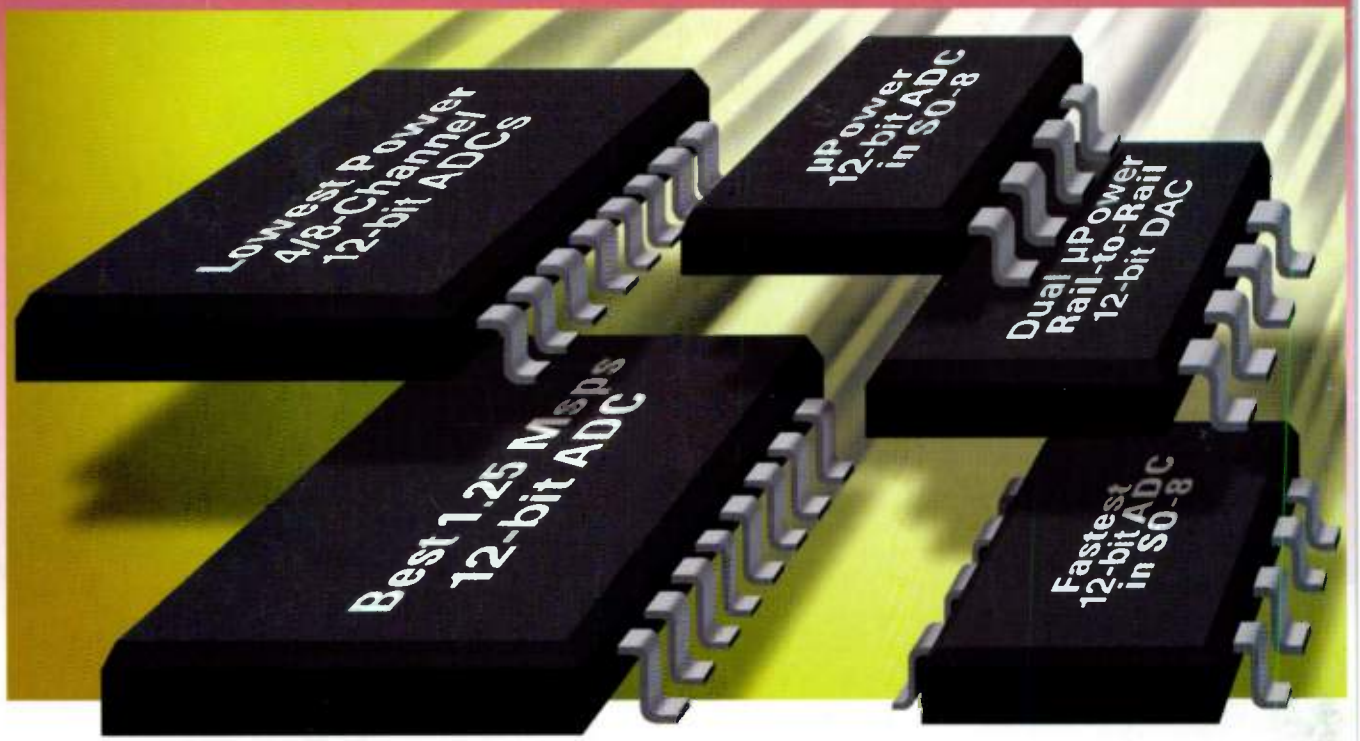

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