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FOR ENGINEERS AND ENGINEERING MANAGERS - WORLDWIDE

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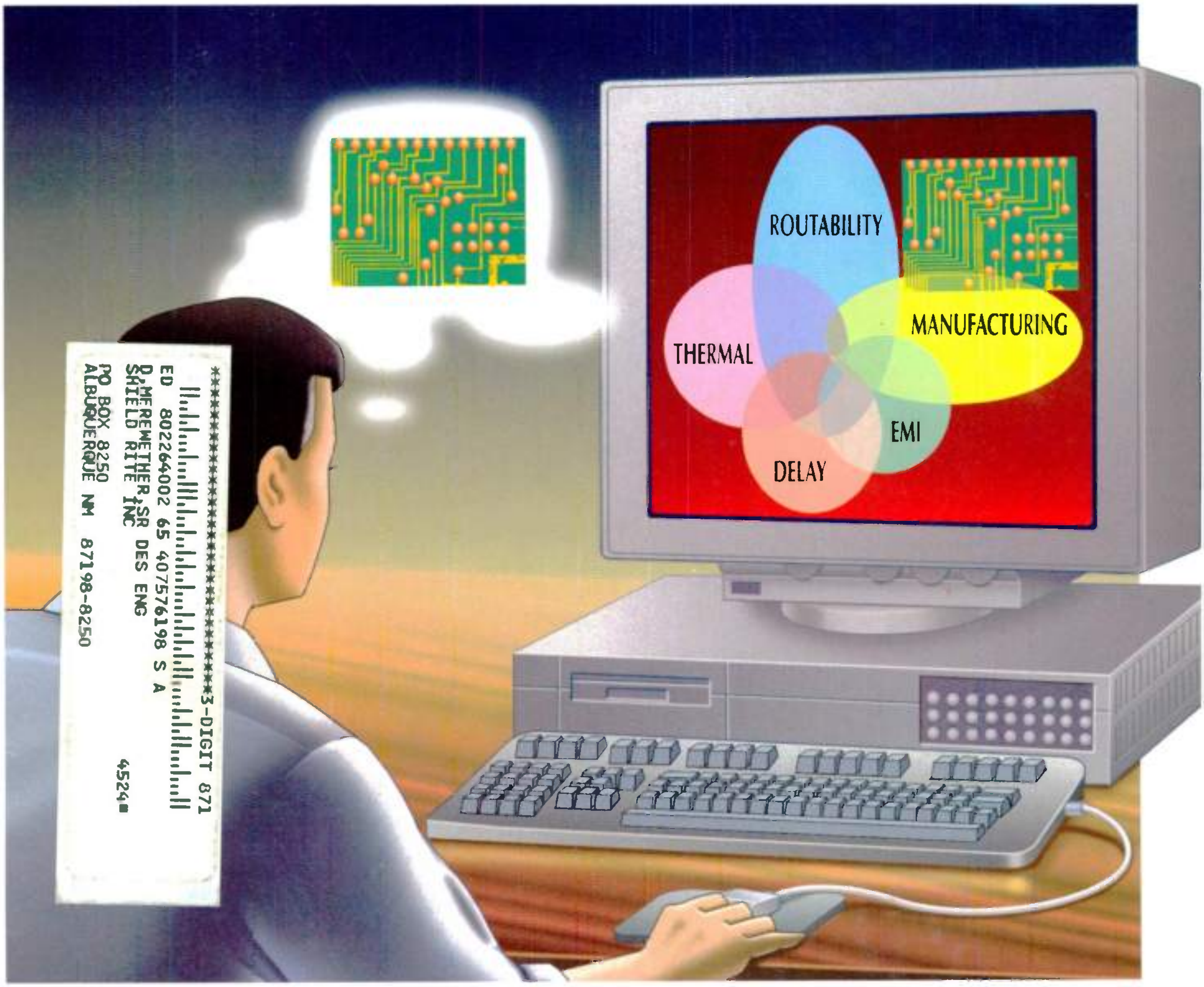
MARCH 3, 1997



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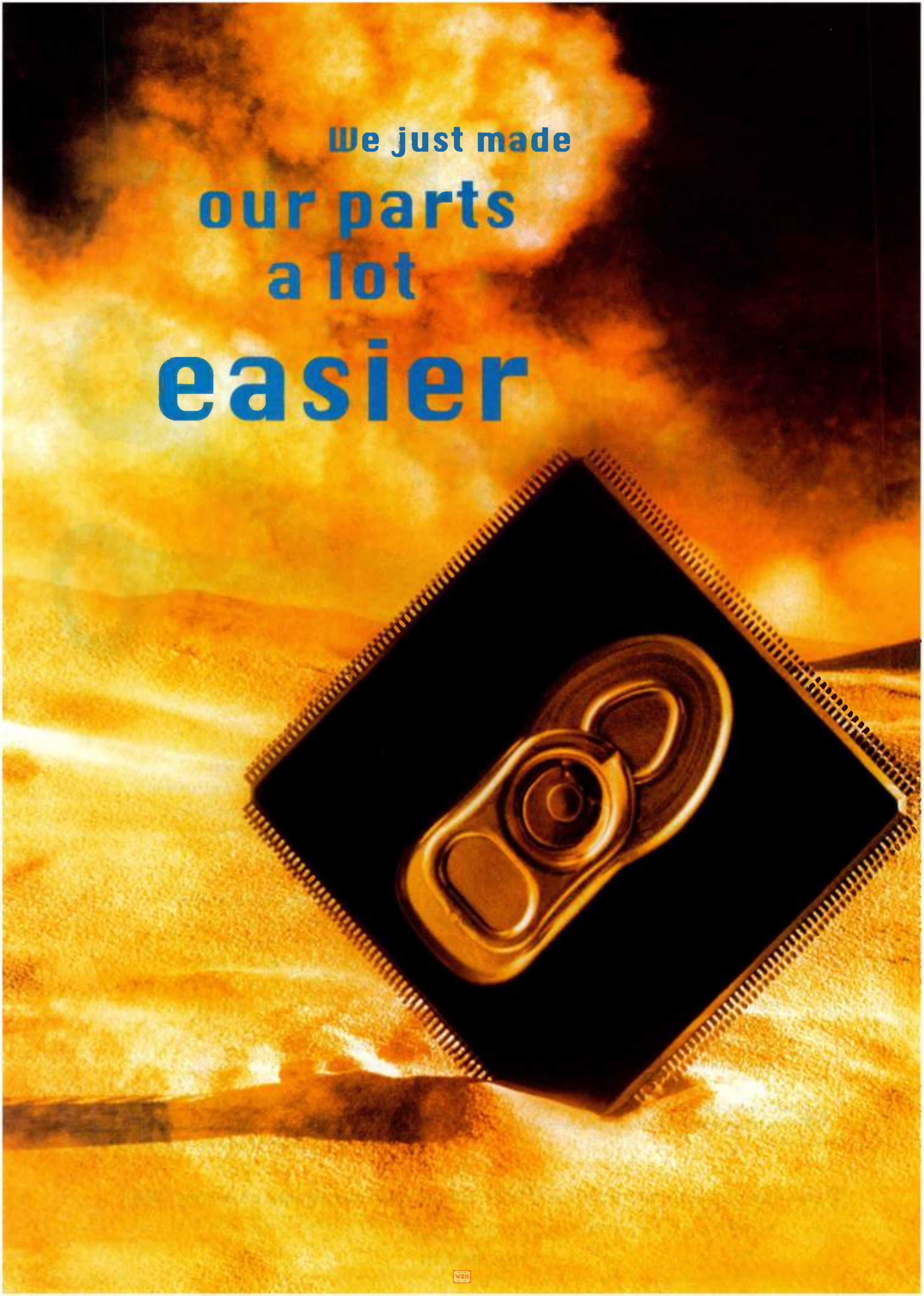
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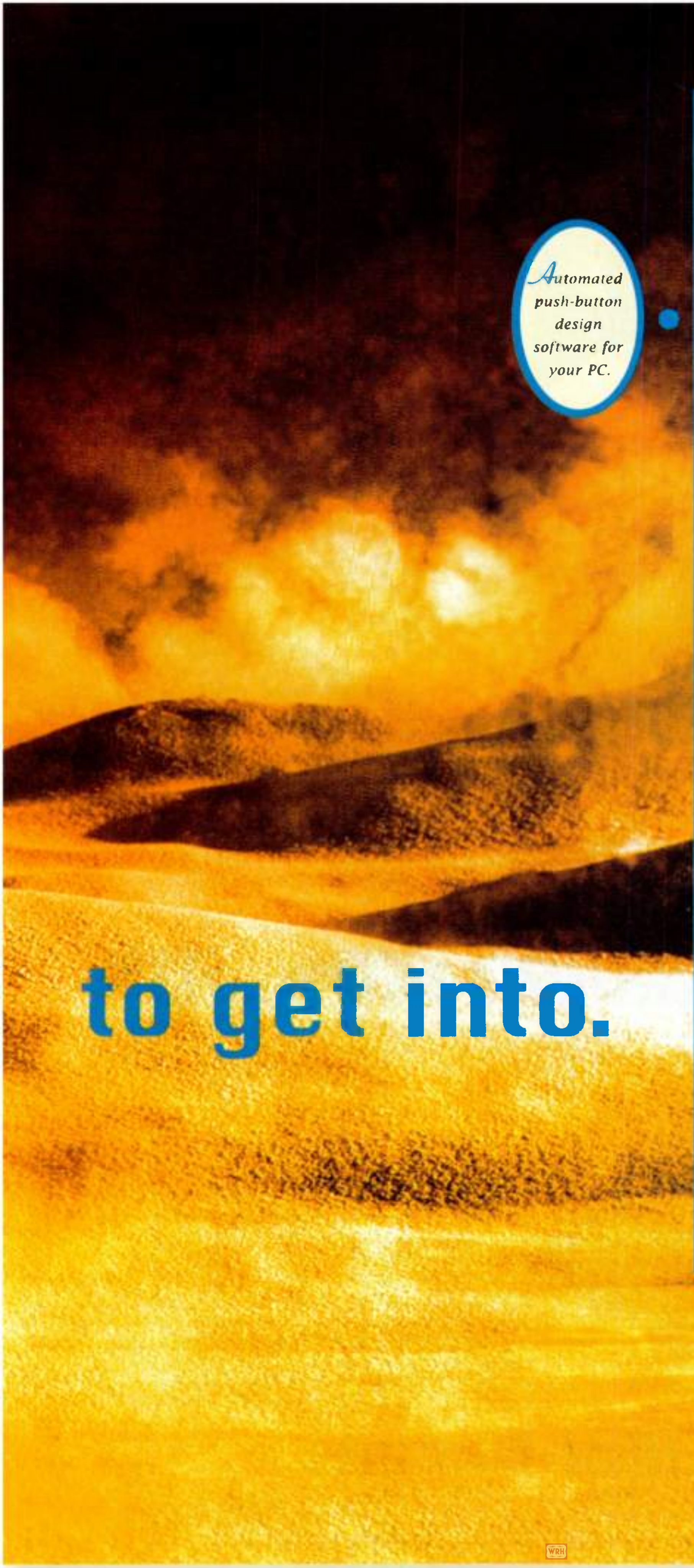
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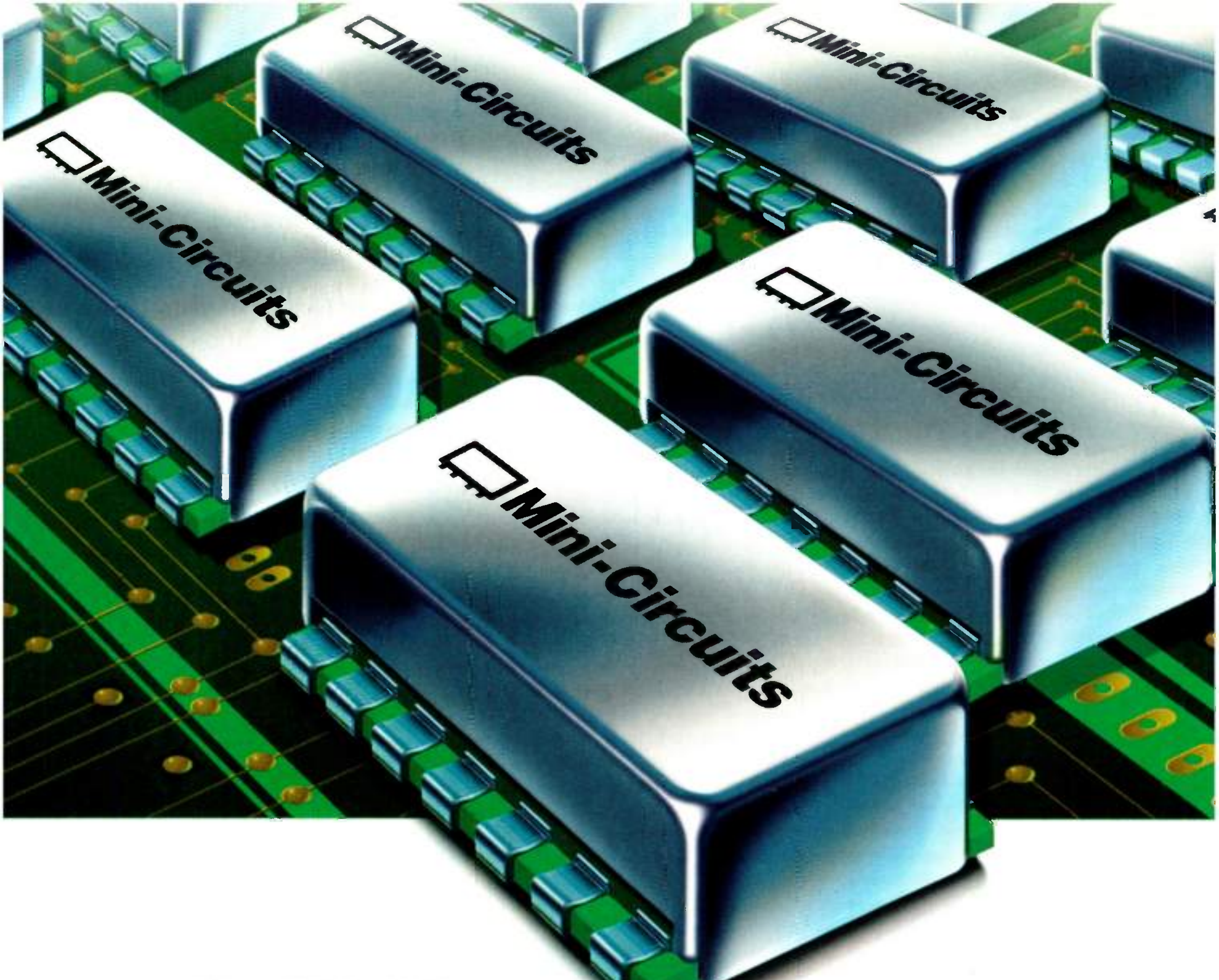

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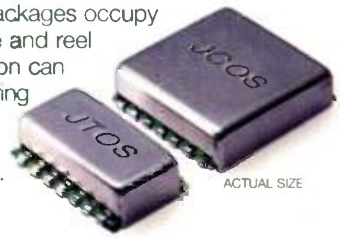

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JTOS-150	75-150	-106	-23	16V	20	13.95
JTOS-200	100-200	-105	-25	16V	20	13.95
JTOS-300	150-280	-102	-28	16V	20	15.95
JTOS-400	200-380	-102	-25	16V	20	15.95
JTOS-535	300-525	-97	-28		20	15.95
JTOS-765	485-765	-98	-30	16V	20	16.95
JTOS-1025	685-1025	-94	-28	16V	22	18.95
JTOS-1300	900-1300	-95	-28	20V	30	18.95
JTOS-1650	1200-1650	-95	-20	13V	30	19.95
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JCOS-820WLN	780-860	-112	-13	20V	25 (@9V)	49.95
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ELECTRONIC DESIGN

March 3, 1997 Volume 45, Number 5

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TECH INSIGHTS

EDA

COVER FEATURE

ANALOG OUTLOOK

PIPS

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ELECTRONIC DESIGN

March 3, 1997 Volume 45, Number 5

EDITORIAL OVERVIEW

PIPS

BOARDS & BUSES

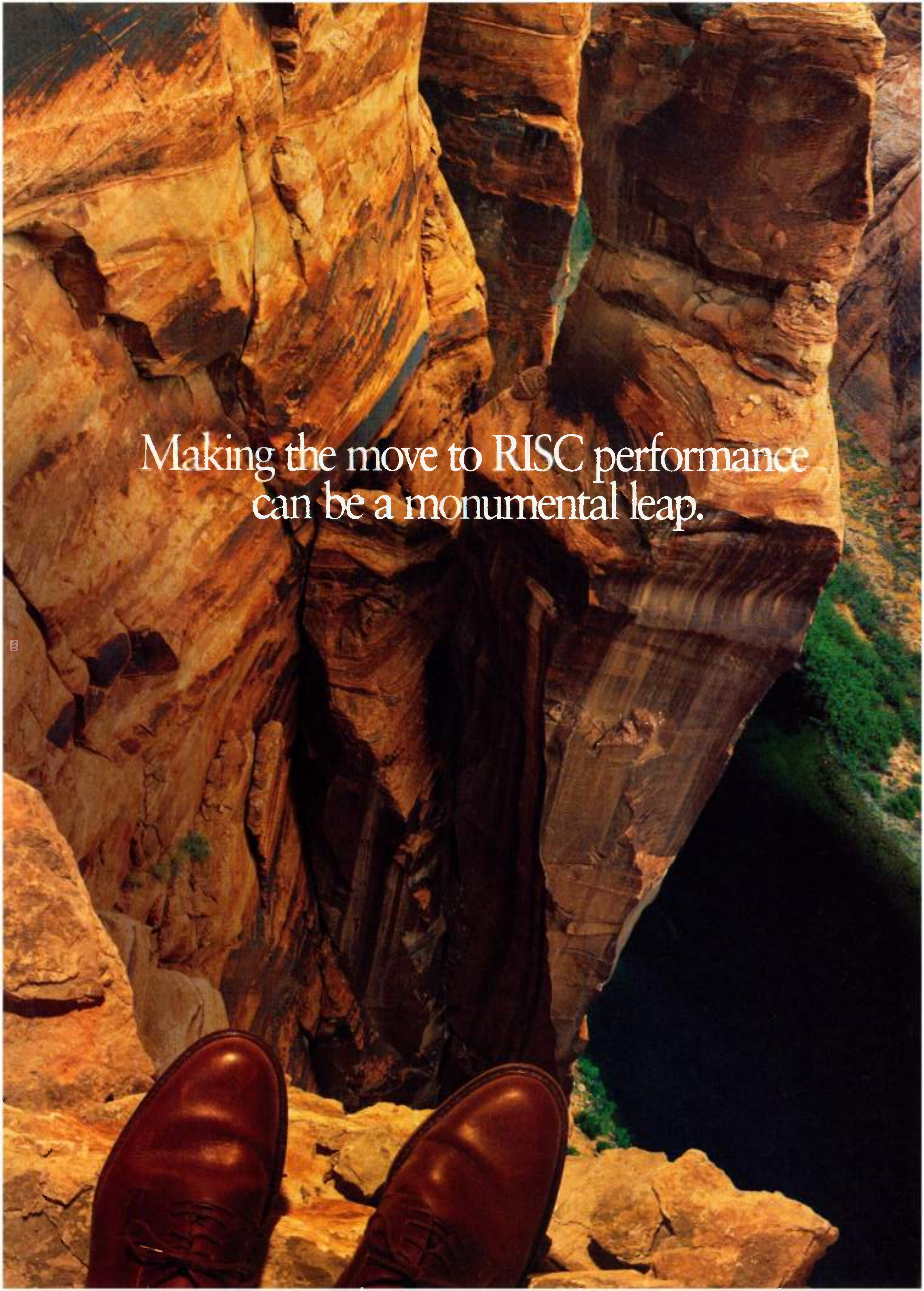
QUICK LOOK

DEPARTMENTS

COVER ILLUSTRATION BY: BRUCE JABLONSKI

Jesse H. Neal Editorial Achievement

1967 First Place Award	1978 Certificate of Merit
1968 First Place Award	1980 Certificate of Merit
1972 Certificate of Merit	1986 First Place Award
1975 Two Certificates of Merit	1989 Certificate of Merit
1976 Certificate of Merit	1992 Certificate of Merit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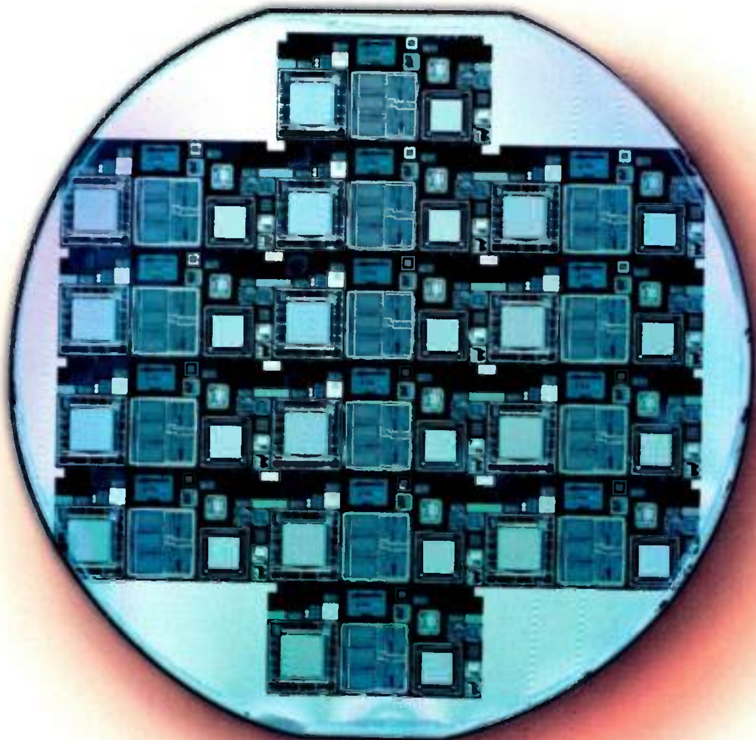

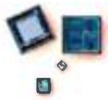

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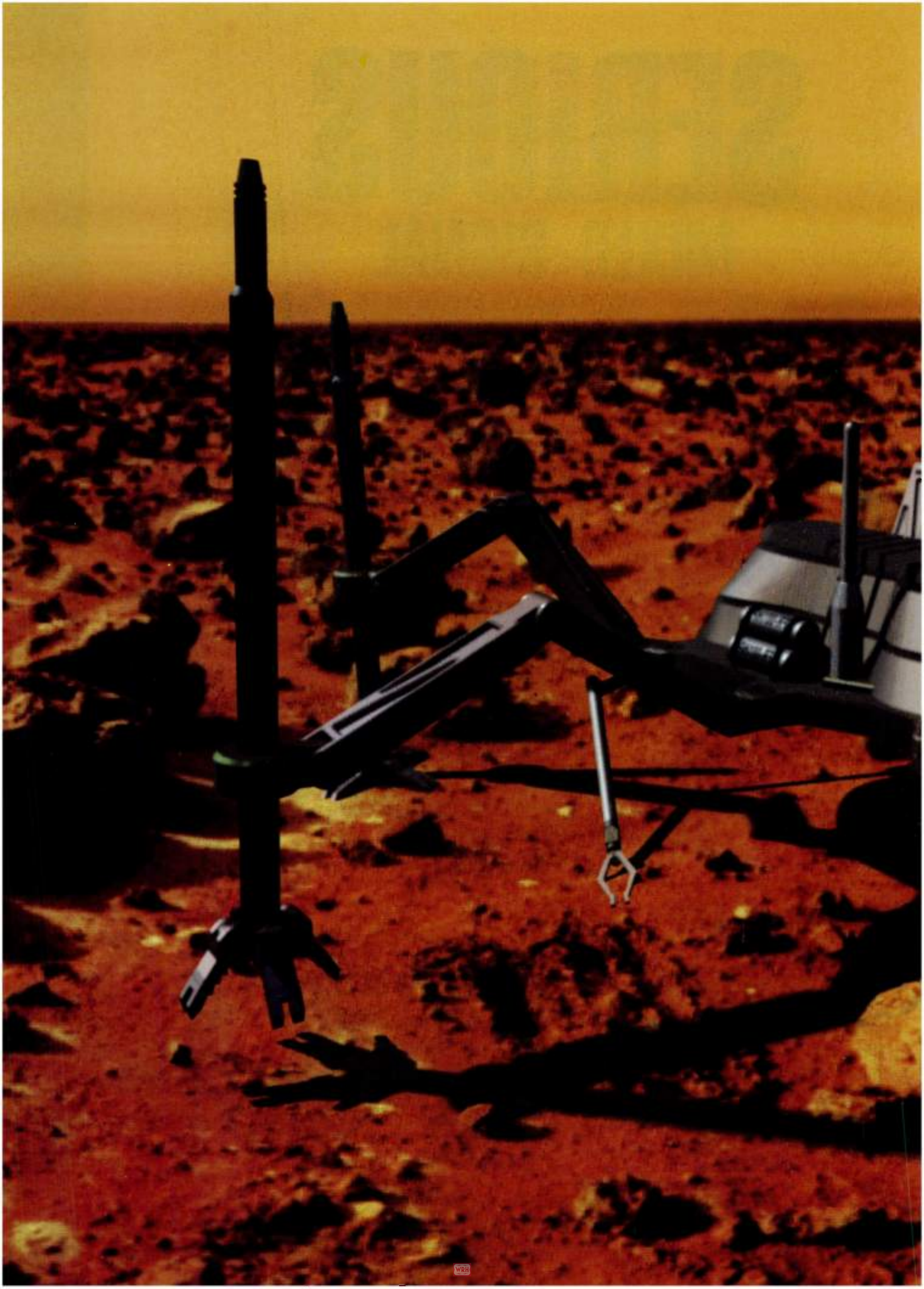
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MARCH 1997

Embedded Systems Conference East, Mar. 10-12. Hynes Convention Center, Boston, MA. Contact (617) 821-9222; e-mail: esce@exporeg.com.

PCB Design Conference West, Mar. 15-21. Santa Clara Convention Center, Santa Clara, California. Contact PCB Design Conference, P.O. Box 472, Canton, Massachusetts 02021; (617) 828-9185; fax (617) 828-8198.

European Design & Test Conference (ED&TC '97), Mar. 17-20. CNIT Conference & Exhibition Centre, Paris-La Defense, France. Contact ED&TC Conference Secretariat, CEP Consultants Ltd., 43 Manor Pl., Edinburgh, EH3 7EB, UK; (44) 131-300 3300; fax (44) 131-300 3400; e-mail: edtc@cep.u-net.com.

Antennas: Principles, Design, and Measurements (Short Course), March 18-21. Mission Bay, San Diego, California. Contact Kelly Brown, NCEE, 1101 Massachusetts Ave., St. Cloud, Florida 34769; (407) 892-6146; fax (407) 892-0406.

Communication Design Engineering Conference, Mar. 24-26. Washington, DC. Convention Center, Washington, DC. Contact Denise Chan, Miller-Freeman Inc., (415) 278-5231.

Portable By Design Conference and Exhibition, Mar. 24-27. Santa Clara Convention Center, Santa Clara, CA. Contact Betsy Tapp, (201) 393-6075; fax (201) 393-6073; e-mail: portable@class.org.

Communication Design Engineering Conference, Mar. 25-27. Washington Convention Center, Washington, DC. Contact (617) 821-9219; e-mail: cdec@exporeg.com.

DSP World Spring Design Conference, Mar. 25-27. Washington Convention Center, Washington, DC. Contact Denise Chan, Miller Freeman Inc., (415) 278-5231; e-mail: dsp@exoreg,com.

SOUTHCON '97, Mar. 25-27. Raleigh Civic and Convention Center, Raleigh, North Carolina. Contact Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, California 90045; (800) 877-2668 ext. 243; fax (310) 641-5117; e-mail: southcon@ieee.word.org.

Second Conference on The New Integrated Service Provider (Supercarrier '97), Mar. 26-28. Washington Vista Hotel, Washington, DC. Contact (800) 822-6338 or (202) 842-3022 ext. 317; Internet: http://www.brp.com.

Sixth International Verilog Conference, Mar. 31-Apr. 2. Santa Clara Convention Center, Santa Clara, CA. Contact MP Associates, 5305 Spine Rd., Suite A, Boulder, CO 80301; (303) 530-4562; fax (303) 530-4334; e-mail: ivcinfo@ivc-conf.com.

APRIL 1997

INTERMAG '97, Apr. 1-4. Hyatt Regency Hotel, New Orleans, LA. Contact John Nyenhuis, School of Electrical Engineering, Purdue University, West Lafayette, Indiana 47907-1285; (317) 494-3524; fax (317) 494-2706; e-mail: nyenhuis@ecn.purdue.edu.

Surface-Mount Technology Association, April 2. Gwinnett County Civic Center, Atlanta Georgia. Contact (770) 569-1822; e-mail: smta-info@t-tech.com; Internet: http://www.smta.org.

IEEE International Reliability Physics Symposium, April 7-10. Adams Mark Hotel, Denver, CO. Contact IRPS Publishing Services, P.O. Box 308, Westmoreland, NY 13490; (315) 339-3971; fax (315) 336-9134; e-mail: 103227.2074@compuserve.com.

IEEE Conference on Computer Communications (INFOCOM 97), April 7-11. Kobe, Japan. Contact Tatsuya Suda, Deptartment of Information & Computer Science, University of California, Irvine, California 92717-3425; (714) 856-5474; fax (714) 856-4056; e-mail: suda@ics.uci.edu; Internet: http://www.ics.uci.edu/infocom/ (North America); http://arpeggio.ics.es.osaka-u.ac.jp/infocom.html (Japan).

Fourth ASAT Conference , Apr 4-16. San Francisco Airport Marriott, San Francisco, California. Contact Suzanne Graf, Project Manager, (541) 984-5204; fax (541) 343-7024; e-mail: SGraf@Advanstar-Expos.com.

IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP 97), Apr. 21-24. Gasteig Cultural and Convention Center, Munich, Germany. Contact Bernd Girod, Lehrst.f.Nachrichtentechnik, Univ. of Erlangen Nuremberg, Cauerstr. 7, D-91058 Erlangen, Germany; (49) 91-3185-7101; fax (49) 91-3131-30840; e-mail: b.girod@ieee.org.

Sixth System Administration, Networking, & Security Conference, April 21-26. Baltimore Inner Harbor, Maryland. Contact USENIX Conference Office, 22672 Lambert Street, Suite 613, Lake Forest, California 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

IEEE International Conference on Robotics and Automation, April 21-27. Albuquerque Convention Center, Albuquerque, New Mexico. Contact Jerry Stauffer, Intelligent Systems and Robotics Center, Program Office, MS0949, Sandia National Laboratories, Albuquerque, New Mexico 87185-0949; (505) 845-8966; fax (505) 844-6161; e-mail: jdstauf@isrc.sandia.gov.

First Convergence Technology & IC Expo, Apr. 22-24. InfoMart, Dallas, Texas. Contact Electronic Conventions Management, 8110 Airport Boulevard, Los Angeles, California 90045; (800) 877-2668, ext. 243; fax (310) 641-5117.

15th IEEE VLSI Test Symposium, April 27-30. Hyatt Regency Monterey, Monterey, California. Contact Y. Zorian; (408) 543-0146 ext. 227, e-mail: zorian@lvision.com.

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inventor of the integrated circuit, March 25, 5-8 P.M.

BOB PEASE
author & columnist, March 26, 5-8 P.M.

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2. YOUR RESPONSIBILITY/INFLUENCE

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- ☐ c. Specify suppliers
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- ☐ e. 101 -250
- ☐ f. 251 - 500
- ☐ g. More Than 500

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- ☐ c. Computer peripherals, including PCMCIA modules
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- ☐ f. Communications services
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- ☐ h. Network equipment
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- ☐ j. Industrial controls
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- ☐ n. Automotive equipment
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- ☐ p. ICs and semiconductors
- ☐ q. Power sources/supplies
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EDITORIAL

Privacy, Surveillance, And "Big Brother"

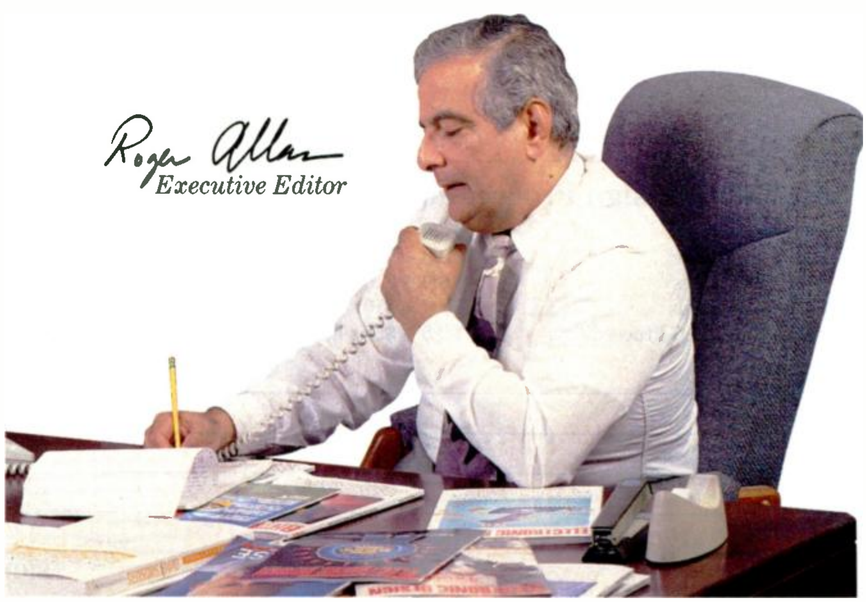
The dazzling array of electronic equipment that is now available—cellular and portable telephones, personal digital assistants (PDAs), pagers, baby monitors, interactive cable systems, and laptop computers—is redefining our view of "privacy." The proliferation of e-mail and the World Wide Web has brought the privacy problem to the fore "in spades." Just who's privacy is it anyway? Is it our right to have private conversations free from oversight and intrusion as the Constitution would have us believe, or is it "big brother's" equal, if not greater, right to listen in?

We all know that for every weapon a counterweapon will surely be developed. When the telegraph was invented back in the 1840s, snoopers started to climb the poles to tap the wires and listen in on transmissions. This was followed by the development of coded transmissions and the passing of anti-tapping laws. That may have provided a measure of privacy, but it didn't stop those intent on snooping; they simply developed more sophisticated countertechniques to listen in on the transmissions. The bottom line is that there simply is no "ultimate" privacy weapon. Sure, there are cryptographic and data-scrambling techniques that provide us with a high level of privacy, but no sooner are these developed than someone comes up with a countermethod to crack them.

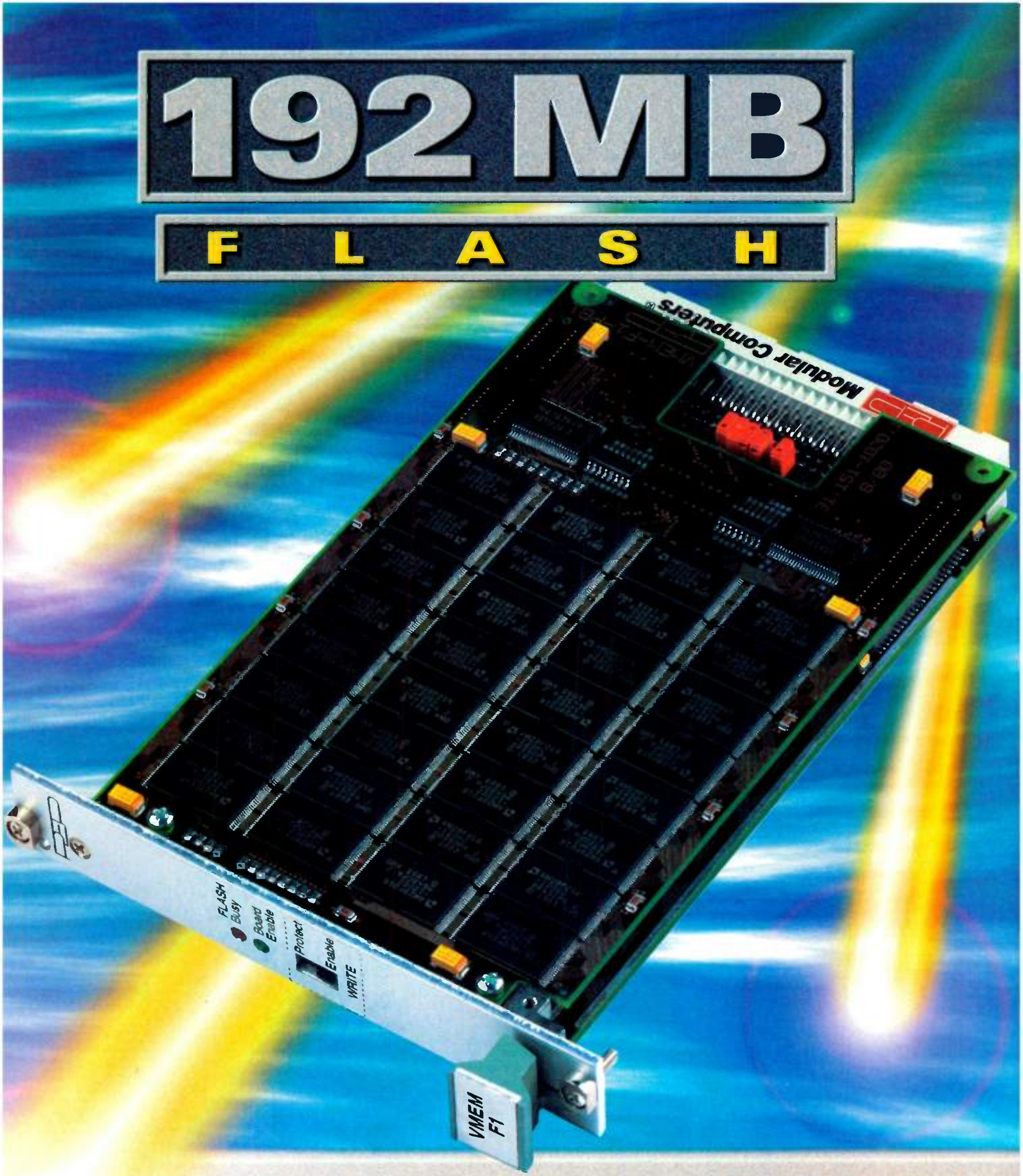
Nor would the government want there to be a perfectly secure communications system—at least not for those who argue that criminals, spies, and terrorists would have a free hand at making mischief. But that raises the question: "Who's privacy is it anyway?" The answer is not that simple. There are legal protections for the average citizen from unwarranted government intrusions, like court orders, before any "tapping" is undertaken. But recent events demonstrate that even without a court order, average citizens have been able to listen in on sensitive inter-computer and telephone conversation, with readily-available radio scanners and other listening devices.

Privacy is still not completely defined. And given the rapid advancements in communications and computer technologies, its definition will become even murkier. Technological ingenuities are invading our traditional understandings of privacy at record levels.

Citizens groups, industry, the legislature, and all interested parties must get together and come up with a common definition of how we should define privacy in terms of our present technological capabilities. Such a definition would be a moving target that will surely keep changing with technological advancements that are certain to continue. Are we ready for the Orwellian age? Give us your opinion. *rallan@class.org.*



Roger Allan
Executive Editor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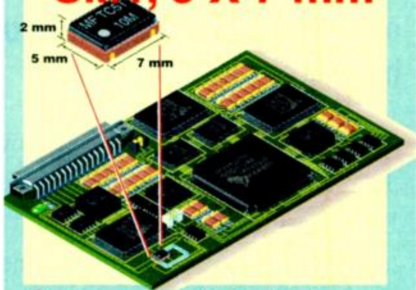

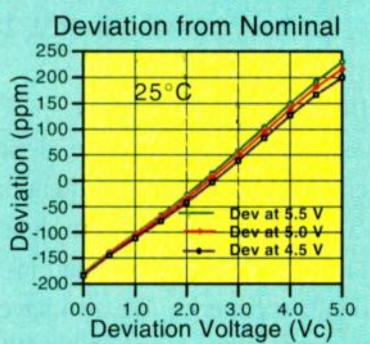

VXI And PCI Will Coexist Quite Nicely

A statement caught my eye as I was reading one of those white papers that companies mainly put out to catch an editor's eye. "The failure of the VXI bus has become a classic example of how multivendor standards can fail..." Competitive pressures had kept instrument manufacturers from cooperating, according to Muneeb Khalid, president of Gage Applied Sciences Inc., Montreal, Quebec, Canada.

I knew that the VXI hardware standard couldn't be the problem. That had been a success from the start. But the VXIbus Consortium's charter said nothing about software, and that had been a problem for VXI users.

In fact, the lack of a standard operating system was the main cause of VXI's failure, according to Khalid. In a phone conversation, he also defined failure: "This bus was supposed to take over all instrumentation. Back in 1989, that's what was said about VXI. And it didn't." So although VXI is a good bus and has a large following, it is a "relative failure" because it didn't meet expectations, he said.

The subject of the white paper actually wasn't VXI but "The Power of PCI Bus Instrumentation," which expresses Khalid's feelings on what he sees as the emerging standard for T&M, data acquisition, and instrumentation. The VXI bus was very fast when it was designed in the late 80s, but the PCI bus has passed it by, he said. Not only is PCI much faster, it also is much less expensive. The PCI platform and cards cost much less than VXI hardware, and because PCI is basically a PC-based system, it's much easier and less costly to program. "The expertise of programming for PCI is a lot more prevalent in the general population," said Khalid.

JOHN NOVELLINO
TEST AND MEASUREMENT

The only real advantage left to VXI is the standard's trigger bus, he said. And Gage, a supplier of PC-based data-acquisition products, has gotten around that by adding to its cards a mezzanine bus that connects multiple modules. That mezzanine bus is not part of the PCI standard, however.

James Kimery, VXI product manager at National Instruments Corp., Austin, Tex., disagrees with Khalid. VXI's original forecasts were very optimistic, he said. The bus was expected to replace IEEE-488 (GPIB), but it hasn't. Still, VXI is a $450 million industry and growing fast, said Kimery. NI is a major player in both VXI and PC-based instrumentation, including PCI bus.

Kimery said many people felt VXI was too difficult to use early on. "I don't think it was a question of operating system standardization, but a question of I/O software and a standard instrument driver model based on that standard I/O software," he said. The VXIplug&play Systems Alliance was established to address this problem. It's efforts have been an "unqualified success," he said, because all vendors stood to gain from it.

Speed isn't a factor either, said Kimery. He noted that the VME64 protocol doubles VXI bandwidth to 80 Mbytes/s and newer VME standards jump to 160 and 320 Mbytes/s. "Most users don't need these eye-popping numbers," he said. "But both buses will remain viable in the future as far as data transfer rates go."

Kimery agreed that VXI can be more expensive to buy and run, but he noted that most PCI computers have only three or four slots, due to load impedances and reflections. Going to a larger system can be much more costly. VXI has many other advantages, he said, including standards for shielding, electromagnetic radiation, and susceptibility; larger card sizes, and the VXI local bus.

The bottom line: With VXI, PC-based data acquisition, and that old standby, GPIB, designers have some pretty good choices available. VXI and PCI, in particular, will be around for some time, with the promise of continued improvements in the future. *jnovelli@class.org.*

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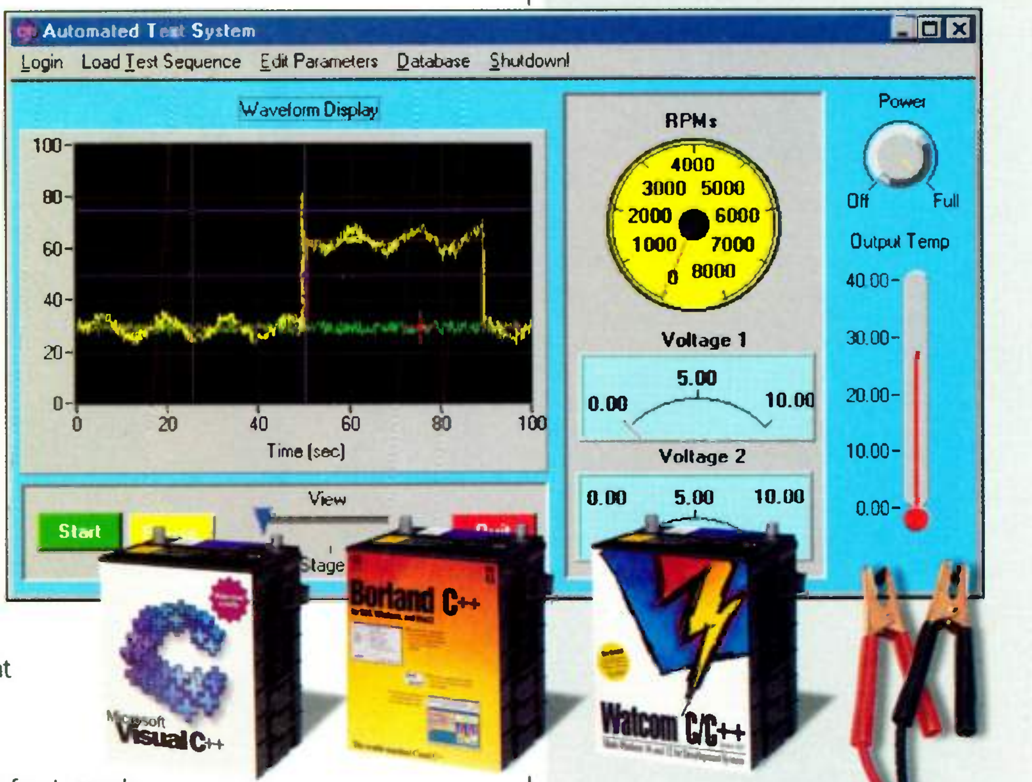

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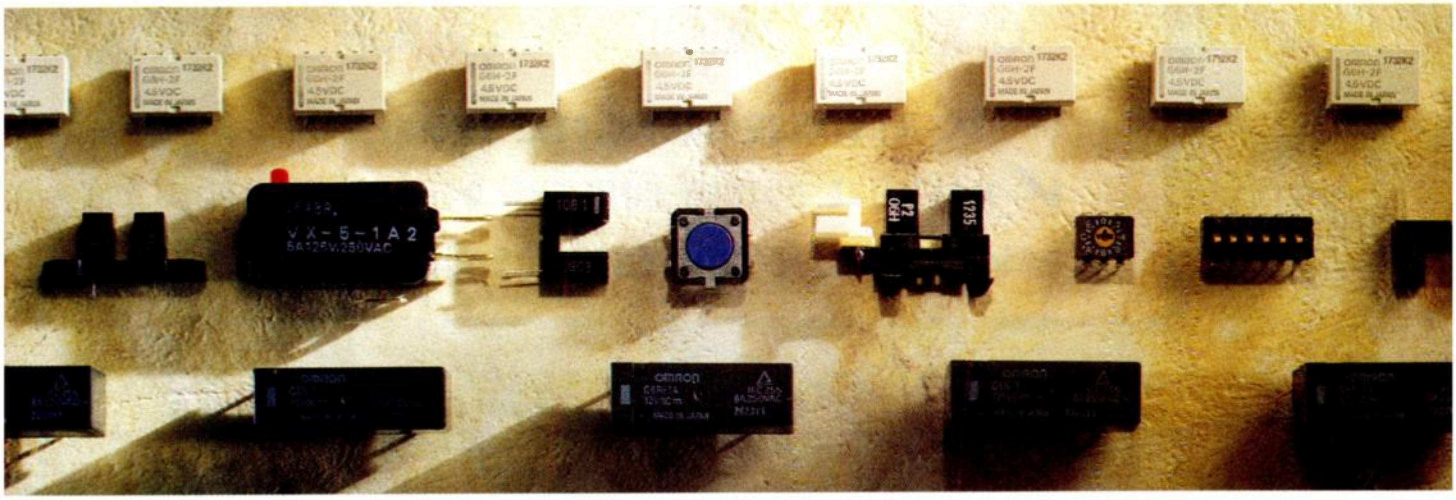

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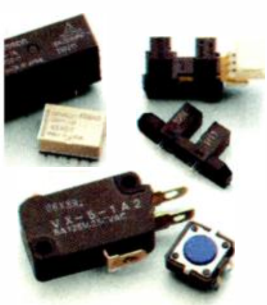

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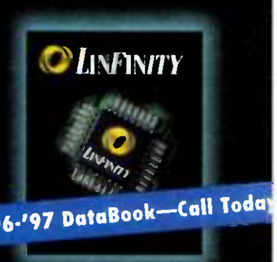

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READER SERVICE 113

New Laser Sings The Blues... And Red And Orange And Green

Full-color projection displays or high-density optical data-storage applications may benefit from an all-solid-state laser that produces four visible colors. The laser, developed by researchers at the Los Alamos National Laboratory, Los Alamos, N.M., can be tuned to produce red, orange, green, and blue light.

The new device's ability to generate blue light is particularly significant because blue has been difficult to produce reliably and efficiently from solid materials. The researchers employed a phenomenon called a photon avalanche. They placed two kinds of impurities in a zirconium-fluoride-based glass. The impurities, which are triple-charged ions, act as both energy donors and acceptors, while readily absorbing more energy from an infrared pump laser. As these excited ions release energy to yield less-excited ions, they produce light. The color of the light depends on the specific lower-energy state to which the laser is transitioning.

For more information, contact Kathy DeLukas, (505) 665-9201 or duke@lanl.gov. *JN*

Wireless ATM LAN Gives Mobile Callers Access To MPEG-2 Video

The most advanced prototype of a wireless asynchronous transfer mode (ATM) local-area network (LAN) was recently achieved. Developed by Lucent Technologies' Bell Labs, it features wireless laptop computers that run MPEG-2 video and Internet content in a building environment. The advance stems from the company's joint Mobile Information Infrastructure (MII) project with Sun Microsystems. The project addresses key technological challenges for wireless high-speed networking in order to provide digital video and multimedia services to wireless information appliances.

An architecture of wireless ATM LANs are interconnected through ATM switches in the prototype. Each wireless ATM LAN consists of portable base stations (PBSs), enabling wireless coverage for mobile laptops. High-speed wireless (radio or infrared) links are supplied between the laptops and the PBS, which is compact (coffee-can size) and can be deployed in a flexible and reconfigurable manner to provide end-to-end ATM connections to mobiles.

The prototype basically highlights key aspects of the MII, incorporating several advanced technologies. For instance, there's a 10-Mbit/s infrared wireless link between mobiles and PBSs that's capable of low-overhead, single ATM cell transmissions. An efficient demand-assignment-based MAC protocol, called DQRUMA, offers priority-based scheduling in the downlink and uplink directions.

A data-link-layer protocol founded on an adaptive scheme is used to implement ATM cell-based forward error correction using Reed-Solomon coding. Mobility management software performs fast location and connection management, and performs rerouting of connections during handoffs. Also included is real-time MPEG-2 video viewing and high-speed wireless Internet connectivity for mobile laptops. *RE*

Cordless Modem Technology Eases E-mail, Internet Access

Phooey with phone cords. A low-cost cordless modem technology developed by IBM Research Div., Yorktown Heights, N.Y., and Kyushu Matsushita Electric Co. Ltd (KME), Fukoka, Japan, should make Internet and e-mail access more convenient for home and small-office computer users. KME is a subsidiary of Matsushita Electric Industrial Co., best known for its Panasonic products.

Cordless modem technology is based on the same principle as cordless telephones, enabling users to go on-line without physically connecting to a phone jack. Data is transmitted directly between the PC and a small device connected to the phone jack. What this means is that home and small-office users can receive e-mail, surf the World Wide Web, or run videoconferencing or simultaneous voice and data applications without climbing under desks or rearranging furniture to reach the nearest phone outlet.

No software, driver, or operating-system changes to PCs are required, so the new technology is literally provides "plug-and-play" convenience. The cordless modem, based on IBM Research patent-pending technology, delivers V.34 connections at up to 28.8 kbits/s using a modified radio architecture similar to that used in today's 900-MHz cordless telephones. Because the technology is based on existing protocols, IBM and KME anticipate developing products that support high-speed analog modem data rates at affordable costs. For more information, call IBM at (914) 945-3738; or Panasonic at (201) 348-7184. *RE*

Joint Venture Dials In On Next Generation Of Wireless Paging

An agreement reached between Socket Communications Inc., Newark, Calif., and Cetronic AB, Sundsvall, Sweden, is expected to lead to a novel line of wireless data-paging products, eventually opening up new applications and markets for mobile computing. Socket Communications is the leading supplier of paging-based mobile computer products in the U.S., while Cetronic is the leading supplier of paging-based computer products in Europe. The products will take advantage of the newest paging protocols in each market and will incorporate technology from both companies.

Through the agreement, the new line of products will serve both the U.S. and international markets. For the U.S., the first product will be a new generation of Socket's PageCard based upon the new FLEX paging protocol. The PageCard, which currently uses the existing POCSAG paging protocol, is a data pager with a PC card interface that receives paged data or messages and downloads them into a handheld PC or notebook computer.

For the European market, Cetronic will market its products under its RadioCard name, creating a device similar to the PageCard that uses the ERMES protocol. The devices will remain fully operational with both Cetronic and Socket existing software interfaces. The FLEX and ERMES protocols were selected due to their superior reliability, faster transmission speed, and a much-enhanced efficiency in utilizing the paging infrastructure. Thanks to these advanced protocols, new applications are possible for delivering time-critical data to mobile workers, such as broadcasting or narrowcasting from the Internet or intranets.

For more information, log onto Socket's web site at http://www.socketcom.com. *RE*

Three Bulletins Published For Telecommunications Community

The Telecommunications Industry Association (TIA) recently released three Telecommunications Systems Bulletins: TIA/EIA-TSB76 "IS-41-C Enhancements for Personal Communications Systems (PCS) Multi-Band Support," TIA/EIA-TSB72 "Centralized Optical Fiber Cabling Guidelines," and TIA/EIA-TSB67 "Transmission Performance Specifications for Field Testing of Unshielded Twisted-Pair Cabling Systems."

The TSB76 document presents recommendations for supporting multiband handoffs, specifically intraband intersystem handoffs, interband intersystem handoffs, and handoffs for mobile stations (MSs) supporting various services. Among the services included are Advanced Mobile Phone Service (AMPS), Call Division Multiple Access (CDMA), Time Division Multiple Access (TDMA), and Narrowband Analog Mobile Phone Service (NAMPS). The recommendation support mobile-station identification based only on a mobile identification number (MIN).

The TSB72 specifies implementation guidelines and connecting hardware requirements when implementing centralized optical-fiber-cabling systems. The guidelines are intended for those single-tenant users who intend to deploy centralized electronics versus distributed electronics, and those who want an alternative to locating the cross-connection in the telecommunications closet.

The TSB67 details the electrical characteristics of field testers, as well as test methods and minimum transmission requirements, for unshielded-twisted-pair (UTP) cabling. The UTP cabling-link specifications are intended to be consistent with the three categories of UTP cable and connecting hardware specified in a previous document (TIA/EIA-568-A) entitled "Commercial Building Telecommunications Cabling Standard." Field-tester characteristics needed for swept/stepped frequency measurements reaching 100 MHz are described for consistency and accuracy reasons.

To obtain any or all of these documents, contact Global Engineering Documents at (800) 854-7179. *RE*

Space-Borne Radar Will Revolutionize Hazard Watching

Stanford University's Howard Zebker (geophysics and electrical engineer) is one of the inventors of a new technology that uses radar pictures taken from 500 miles or more up in space to track tiny movements in the surface of the Earth, like the flow of a glacier in Chile or the build-up of strain on a California earthquake fault. The technology, called synthetic aperture radar (SAR) interferometry, can show, for example, the pulsing over plus or minus a quarter-inch of the molten material in a volcano's magma dome.

Zebker received his doctorate from Stanford and returned after 11 years at the U.S. National Aeronautics and Space Administration's (NASA's) Jet Propulsion Lab (JPL). There a team of scientists were using SAR interferometry to map the surface of Venus. Then they turned the radar around toward Earth itself and used the data to make detailed, three-dimensional topographic maps. Zebker started to look at how the technology could show the topography on the move, even measuring the speed of ocean currents.

It is envisioned that a satellite with SAR capability would circle the earth, mapping volcanoes, earthquakes, and glaciers that are active, with each pass being compared to the previous ones. This could alert scientists to movements as small as a quarter-inch, and possibly provide a much earlier warning to a natural hazard that's on its way to becoming an event. No such civilian satellite exists, but two proposals have been made to NASA. Meanwhile, satellite capacity has been launched by Japan, Canada, and the European Space Agency. The data being collected is only available to American scientists on a limited basis, and Zebker has some limited access to the data coming from Canada's Radarsat and Europe's ERS-1.

A retrospective use of SAR data was made in the study of the magnitude 7.3 Landers earthquake in southern California in 1992. The study showed not only how the surface near the epicenter changed due to the quake, but also how strain relaxed along a number of connecting faults in the months after the quake.

For comment, contact Howard Zebker at Stanford at (415) 723-8067, or you can browse his home page at http://ee.stanford.edu/~zebker/. *PMcG*

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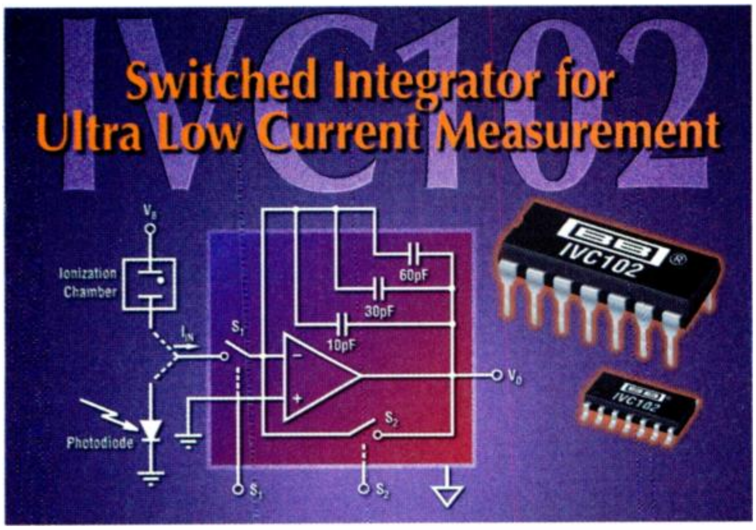
New Product Update



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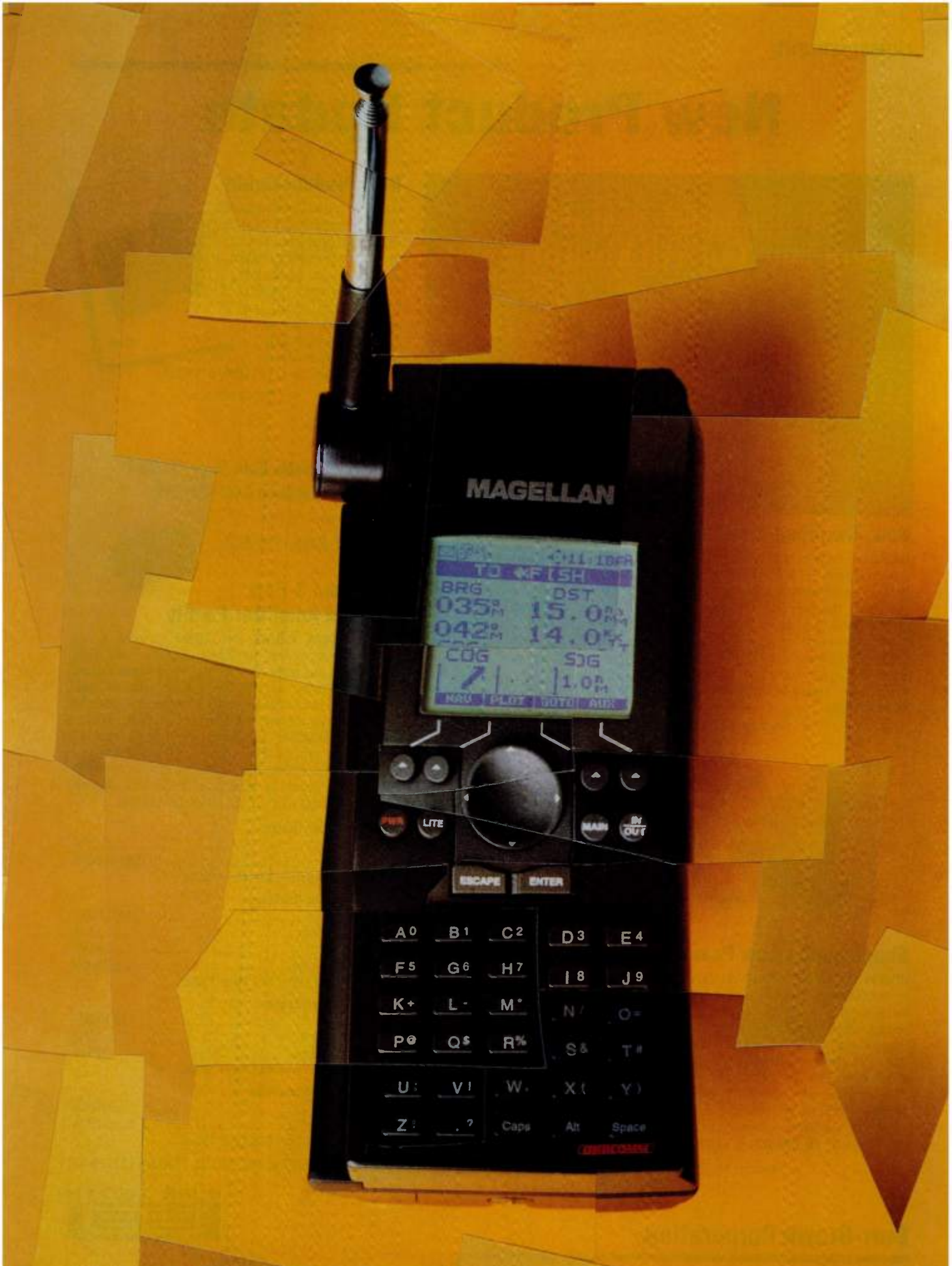
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Embedded Server Core Demonstrates The Feasibility Of High-Performance And Low-Cost Network Computing

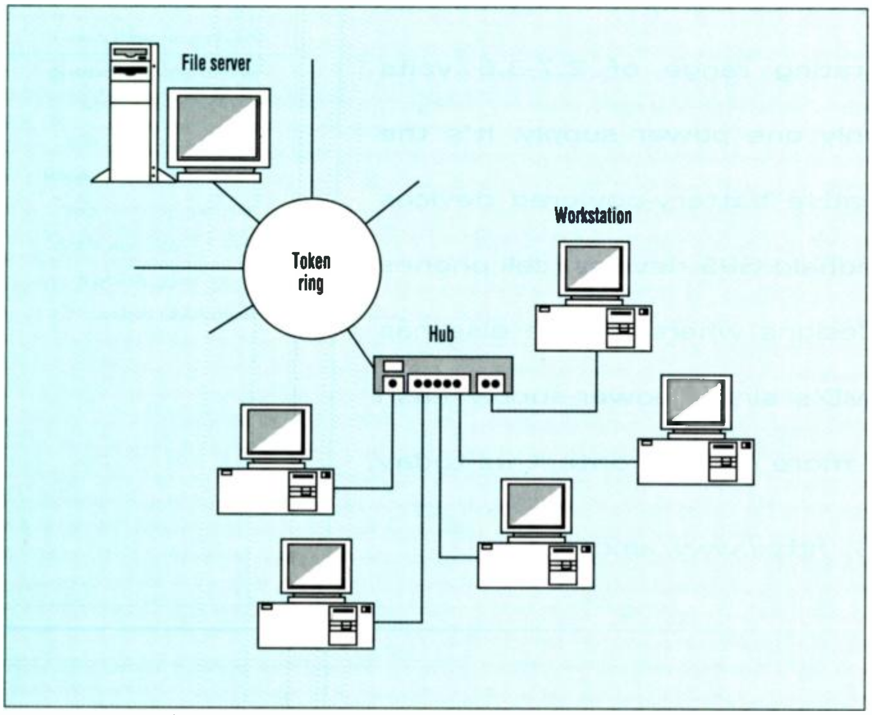
A core technology for the development of highly-optimized network servers has been demonstrated by the Network Power & Light (NP&L) Div. of Mylex Corp., Fremont, Calif. The company believes that the concept "has the potential to dramatically change the landscape of network computing."

The new concept integrates Mylex's advanced hardware and software technology with a high-performance microprocessor. The result is a low-chip-count embedded network server the company calls NetEngine. Incorporating industry-standard peripheral and network connections as well as a real-time operating system, NetEngine is said to form the basis of a complete network server in a very small and low-cost package. NP&L estimates that the technology will be available later this year for about $600 in small quantities.

A key aspect of NetEngine is that it's completely independent of both the operating system and the platform it's based on. The company foresees that the new concept will make obsolete the use of traditional high-end PCs—and their associated costs and complexities—in numerous network applications, including entry level servers, thin servers, and network-attached devices.

Presently, PC-based file servers, which represent over half of all server installations, are used for storing and retrieving data. The way NP&L sees it, this is a clear architectural mismatch because PCs were designed for running applications, not moving data. The new NetEngine technology will streamline file-server architectures for data movement, RISC CPU processing, and intelligent design, resulting in higher performance, lower cost, and an easier-to-use system.

As the responsibilities and complexities of conventional network servers have grown, so too has their cost, complexity, and manageability. What is happening is that these servers are starting to become more centralized, and are thus taking users away from the distributed networking approach file servers began with. The move to client-centric networking is thus ushering in a new server paradigm *(Fig. 1)*.



1. In a conventional centralized file server, a myriad of tasks are called upon to be performed leading toward a client-centric networking approach.

The NetEngine server is aimed at reversing this trend and bringing back the decentralized approach. According to its developers, this embedded server idea has a large number of advantages over conventional general-purpose file servers.

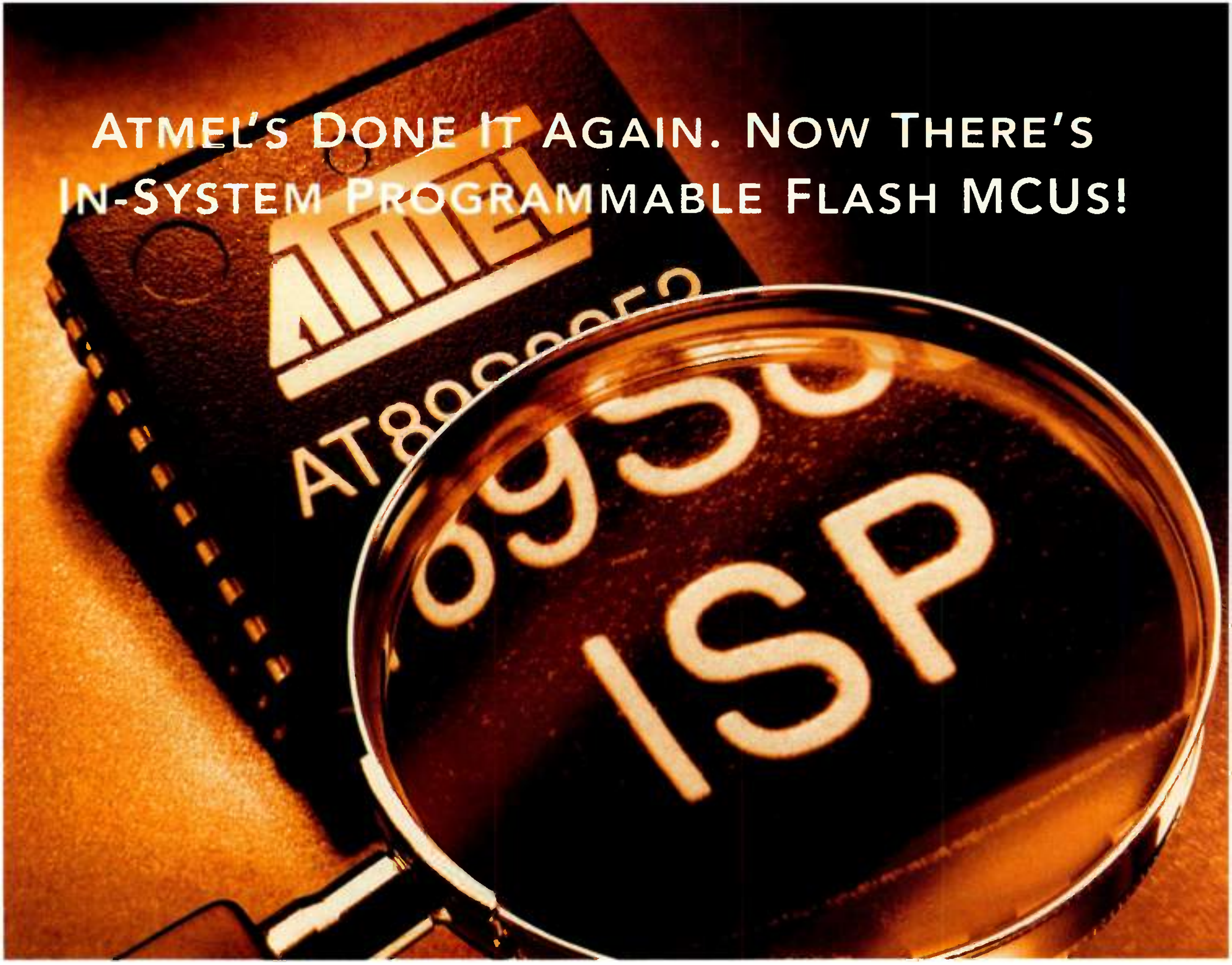
The NetEngine concept will initially be based on the Intel i960 microprocessor. Two potentially large applications, entry-level file servers and plug-and-play network attached storage servers, are thought to be major targets for the server

"Finally, servers will be easy to install and use as a television set," says Greg Brasier, NP&L's director of marketing. "Just plug them in and turn them on. No longer will users be required to spend hours in the arcane mysticism of typical server installations," he adds.

The NetEngine concept works by extracting solution sets from the general-purpose server of today and moving those solutions to a more optimized environment. This allows for the optimization of hardware and software to be used for the network services desired and then embedding all of the resultant parts into a chip or a chip set, or an extensible and small-footprint pc board *(Fig. 2)*. The level of integration then becomes simply a function of semiconductor processing technology, increasing with decreasing chip line widths.

The NetEngine concept eliminates the need for a number of components normally used in typical file servers. For example, keyboards, monitors, large enclosures, and expansion slots are all eliminated, with a resultant cost and space savings. Moreover, an embedded server doesn't require the user to purchase or learn how to operate a network operating system.

Servers based on NetEngine will allow network administrators to optimize subnetworks within an organization, and thereby enable work groups to share files without tieing up an entire local-area network (LAN). The off-loading of data-movement requests from high-end application



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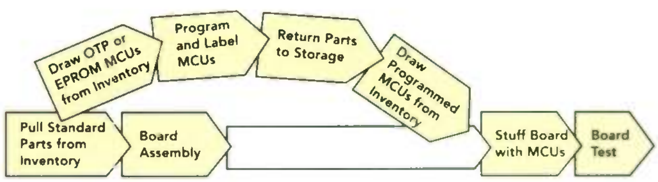

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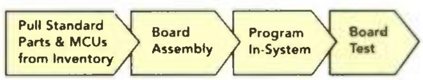

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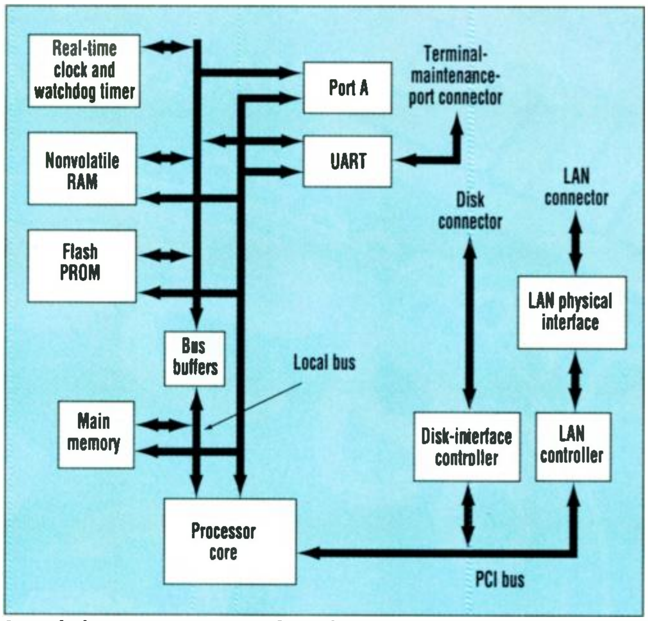
servers increases the performance of other application servers within a network.

According to NP&L, the embedded network server concept will be "of tremendous value" to the NetPC architecture that's being promoted by Microsoft and Intel, among others. For now, the concept is receiving a lot of early support from the industry.

The NetPC thin client reference platform calls for a Pentium microprocessor to be used. Actually, any microprocessor could be used.

The choice of an applications processor using the NetEngine concept depends on the application itself. For example, moving data, which is the principle function of a file server, optimally requires the use of an I/O processor that's tightly coupled with a real-time operating system, not an application processor with a scaled-down version of a general-purpose operating system.

States Jim Kearns, marketing manager for Intel's Enterprise Computing I/O Div., "We're very excited about this new division of Mylex and the technologies they are bringing to the market. Mylex has been closely involved with Intel for years, helping to steer the direction of the i960 processor family. This innovative use of key features of the i960RD I/O processor promises a greatly expanded market for network attached storage."



2. With the NetEngine concept from the NP&L Div. of Mylex Corp., optimized hardware and software can be selected for an application. These can then be embedded into a network-server chip, chip set, or a small-footprint pc board.

According to Michael Petersen, president of Strategic Research Corp., Santa Barbara, Calif., "The concept of shrinking the server into an embedded component will have an incredible impact on next-generation servers. This technology is a home run."

Thomas Lahive, senior analyst for storage systems at IDC, Framingham, Mass., also agrees. "This technology is revolutionary in addressing the needs of the entry segment of the LAN server environment. There are some outstanding market opportunities for the new architecture, including the development of 'storage toasters' that would greatly simplify the process of adding and managing data on a network."

For more information, contact Mylex Corp., 34551 Ardenwood Blvd., Fremont, CA 94555-3607; (510) 796-6100; Internet: http://www.mylex.com. **Richard Nass**

Interoperability Specs For Cable Modems Released Amid Industry Fanfare

The competition between the telcos and the cable industry for the privilege of wiring the American household has taken a significant turn with the introduction of a set of interoperability specifications for cable modems. The specifications define the radio-frequency interfaces between a network's headend and its modems, the network's security provisions, and its operations-support interface. A minimum downstream-data rate of 27 Mbits/s will be provided by equipment complying to this new specification.

This technology should permit manufacturers to design and produce interoperable equipment, capable of supporting transparent, two-way transfer of data, using Internet protocols between cable headends and cable customers. To ensure maximum flexibility, the specification contains provisions for upstream channels from users to be supported using either RF channels within the cable system, or a conventional telephone line as a return path.

The development effort was headed by the Data-Over-Cable System Interface Specification working group, comprising most major cable operators and the research and development consortium, Cable Television Laboratories Inc., (CableLabs). It was conceived as a way to arrive at an open, interoperable communication standard which would allow users and manufacturers to enjoy the benefits and economies of scale associated with high-volume semiconductors and other commodity items. Much like televisions, radios, and telephones, interoperable cable modems should be essentially Plug-and-Play devices, which can be purchased by consumers directly from retail outlets.

To meet the quickening pace of competition for delivery of high-speed, digital-access services, the specification had to take a low-risk approach, using as much existing technology as possible while leaving room for future advances. In order to accomplish this, the specification involved a set of trade-offs which the participants felt represented a prudent balance between performance, cost, and risk. In order of importance, the selection criteria that was used is listed below.

1. Equipment meeting the specification should meet basic performance, feature, and cost needs for the first three-to-five years of service. These requirements necessitate Internet-Protocol transparency and support for multiple grades of service. The target

cost of a first-generation modem was set at $400, descending to $250 for second-generation products.

2. The participants agreed that the specification would be offered without intellectual-property rights encumbrances. This royalty-free environment reduces development time and cost, and ensures the participation of multiple vendors.

3. The system should use technology that is already implemented and tested. This criterion was a must to guarantee the timely availability of both prototypes for testing and production-volume, field-deployable equipment. There should be some equipment on the market as early as the first quarter of this year, with several vendors bringing their products to market by the end of 1997.

4. The specification should be able to embrace advances in technology as they become available. The protocols within the specifications employ a layering strategy to decouple them from each other via clearly defined interfaces. This arrangement should give boxes of various generations the ability to support future changes and upgrades by negotiation of the physical- and higher-layer protocols when a session is established.

5. The specification should be open enough to support customization for vendor-specific features. This criterion permits manufacturers to add value and proprietary functionality without jeapardizing basic interoperability.

The network diagram used in the RF-interface specification illustrates a typical cable network with a two-way, cable-data system in place *(see the figure)*. It consists of a cable modem termination system (CMTS), the cable network, and a number of cable modems (CMs). The CMTS is located at the cable network's headend, with the CMs distributed across the network in the homes and businesses of subscribers. The specification defines the characteristics of the network's RF interface, as well as the message sets and signaling sequences used to pass data, and control between the CMTS and its associated CMs.

To enable transparent transfer of Internet-Protocol messages across a cable system, the Network Layer, Data Link Layer, and Physical Layer protocols, as well as sublayers, are defined. A concise description for the layers follows below:

The Network Layer employs the standard IP protocol.

The Data Link Layer comprises three sublayers:

A Logical Link Control Sublayer (LLC), which conforms to Ethernet standards.

A Security Sublayer that supports the basic needs of privacy authorization, and authentication.

A Media Access Control Sublayer (MAC), which handles cable system operations, and supports variable-length payload data units (PDUs).

The Physical Layer defines the RF transmission technology used, and is based on North American digital-video specifications (ITU-T recommendation J.83, Annex B).

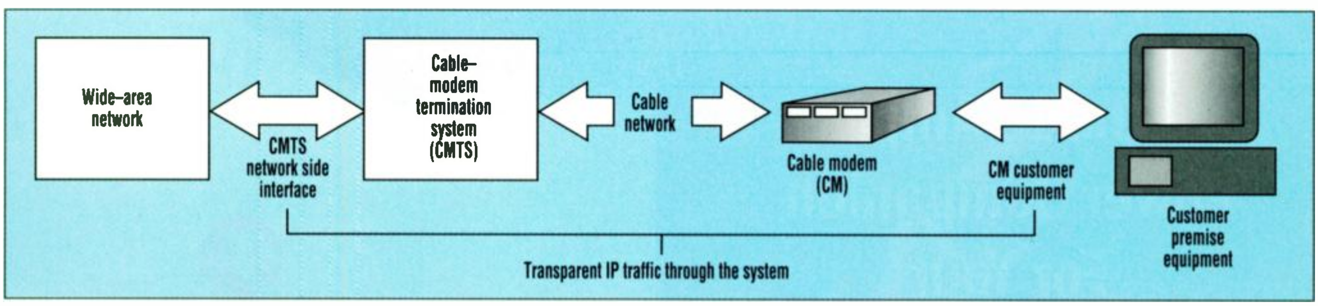
The MAC sublayer defines the rules of the road used by both the CMTs and its CMs to pass traffic between each other in a fair manner. It distributes network access evenly and arbitrates data collisions efficiently. The headend (CMTS) uses a controlled mix of contention and reservation opportunities to ensure that all parties have a shot at communicating. The upstream channel consists of a stream of minislots that are allocated to CMs by the CMTS. Variable -length packets are employed in both directions to ensure maximum utilization of bandwidth.

To accommodate a wide variety of service models, the MAC is designed to handle a wide range of data rates and grades of service. Within the MAC, extensions are provided which will eventually be able to support advanced protocols such as ATM.

At the Physical Layer, downstream transmission can employ either 64-QAM or 256-QAM modulation, with concatenated Reed-Solomon and Trellis forward-error-correction schemes. The standard's variable-depth-interleaving scheme can handle both latency-sensitive data (voice, video) and latency-insensitive data (block file transfers, e-mail, etc.). Contiguous serial bit-stream (for both input and output), with no implied framing, provides complete Physical Layer and MAC sublayer decoupling.

The cable modem's upstream transmission Physical Layer characteristics are governed by the network headend. Under its control, the unit can select either QPSK or 16-QAM modulation formats for upstream transmission. Other specifications, such as symbol rate, transmission frequency, TDMA slot control, and PDU and length are all dictated by the headend controller.

The specification also identifies means by which cable modems can self-discover the appropriate cable system frequencies for reception and transmis-



A high-level block diagram of the components required for a data-over-cable system. This setup allows two-way cable data communications in accordance with recommendations by the Data-Over-Cable System Interface Specification working group, comprising most major cable operators and the R&D consortium, Cable Television Laboratories (CableLabs).

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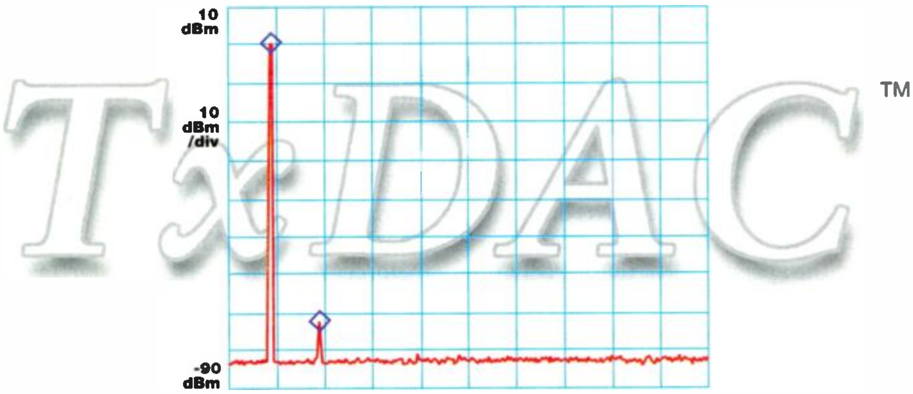

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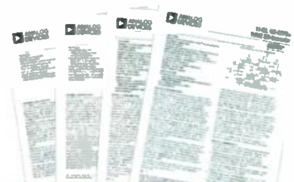

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sion, bit rates, modulation formats, error correction, and power levels.

To protect service and other users, and to ensure reliability, the specification allows cable modems to transmit only after downstream synchronization, and receipt of the appropriate transmission permission by the headend. Additional channels in both the upstream and downstream direction can be provisioned as necessary to optimize traffic loading. It's based on system topology, the number of people actually using a particular portion of the network, and the level of services provided by the operator.

Moderate future proofing is provided by the protocols in the specification. Standard headends will be able to activate new modems and program them with selected enhanced features at startup. The specification also contains provisions that allow the headend to remotely update the modem's software on an as-needed basis.

By rolling out a specification that can be rushed into service today and upgraded later, the cable industry hopes to get a jump start on the slower-moving telecom sector. The signatories to this endeavor include Comcast Cable Communications, Cox Communications, Telecommunications Inc. (TCI), Time Warner Cable, Continental Cablevision, Rogers Cablesystems Limited, and CableLabs. The manufacturers which have signed up to produce compliant equipment include Hewlett-Packard, Bay Networks' LanCity Cable Modem Division, and Com21.

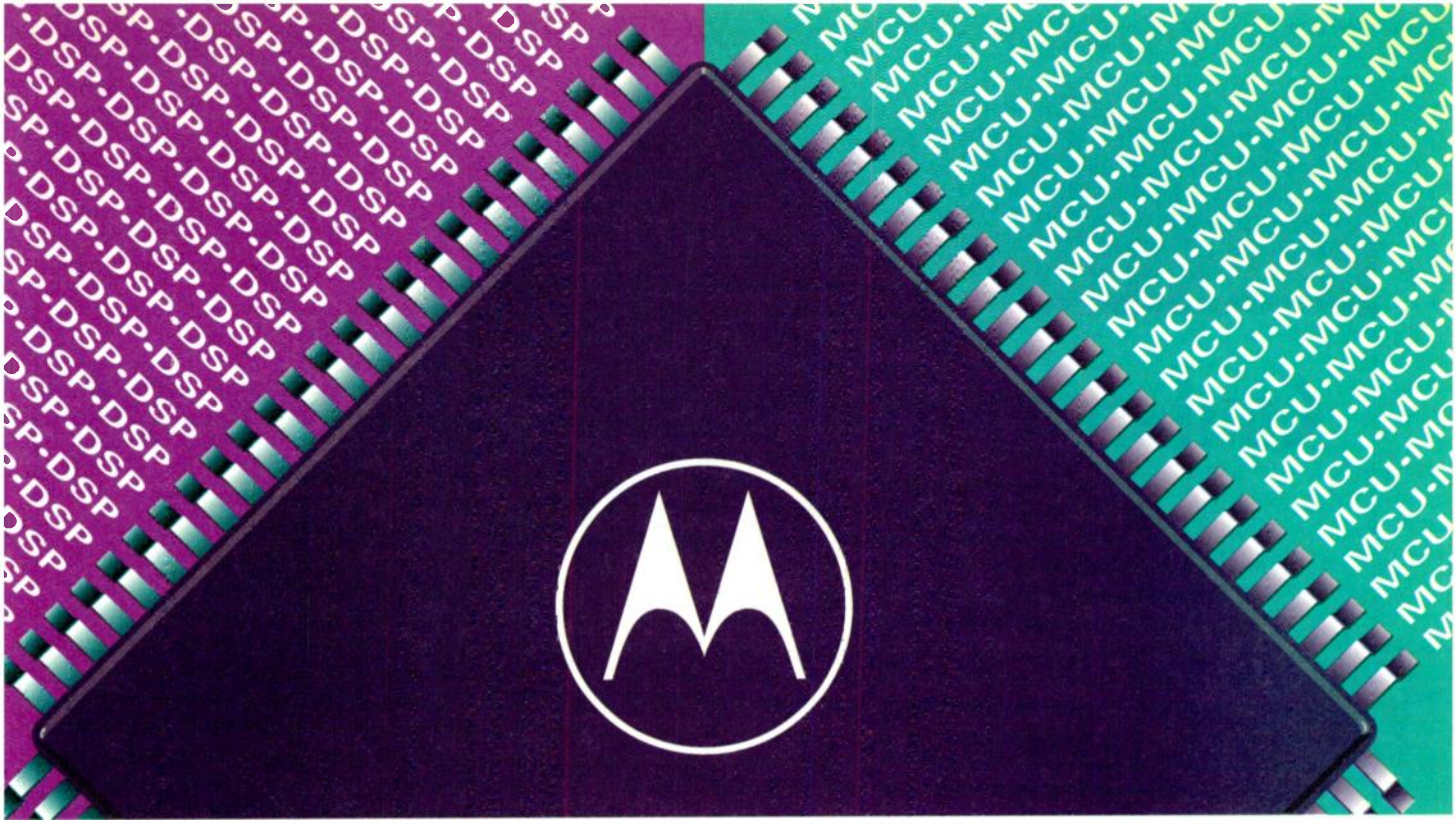
MCNS plans to grant nonexclusive licenses to vendors wishing to manufacture to these specifications. The MCNS license grant is conditioned on a manufacturer's agreement to contribute freely, or in a reciprocal no-cost basis, any crucial, intellectual property required to implement a compliant modem. This agreement should allow sufficient competition to ensure economic competition and the best-of-breed evolutionary process that accompanies open competition in a developing market.

While the first units will be costly ($400 and up) assemblages of off-the-shelf DSPs, controllers, and RF components, economic incentives will likely force highly-integrated, cable-modem chip sets appearing perhaps as early as the end of 1997. By creating an open standard with evolutionary hooks built in, chip makers will be able to reuse their investments in intellectual property and design expertise in several subsequent generations of products.

Vendors unwilling to contribute critical technical information to the royalty-free, intellectual-property pool, would be able to obtain any intellectual property they required through conventional licensing arrangements made directly with the property holders. Manufacturers with no critical intellectual property would be eligible for an MCN royalty-free license to obtain the technology required to produce compliant cable modems.

Further information can be obtained by contacting CableLabs, 400 Centennial Pkwy., Louisville, CO 80027; (303) 661-9100, fax (303) 661-9199; e-mail: *www.cablelabs.com*.

Lee Goldberg



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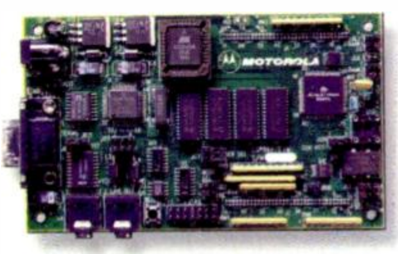

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Richard Nass

All aspects of a portable design. It sounds a lot of information to encompass in a few days, but that's what will be covered at the fourth annual Portable By Design Conference to be held March 24-27, at the Santa Clara Convention Center, Santa Clara, Calif. *(see Want To Go?)*. The four-day program consists of one day of workshops (March 24) and three days of technical sessions (March 25-27). The four full-day workshops include a battery tutorial, a course covering EMC problems and solutions, dc-to-dc converters, and working with the IrDA serial-infrared protocol.

The "Battery Basics" workshop focuses on the principles of battery operation. The performance and reliability of battery-powered equipment, as well as the size and weight of these products, are strongly influenced by the choice of a battery. The workshop will offer an understanding of battery characteristics used in selecting the most appropriate battery for a given application, and obtaining the best system performance. The specific topics to be covered will include basic concepts, electrochemical principles and reactions, factors affecting battery performance, battery design, and selection and application of batteries. The instructor also will discuss the specifics of primary, reserve, and secondary batteries, as well as advanced battery systems.

Workshop number two, titled "EMC Problems and Solutions for Portable Electronics," is presented by William D. Kimmel, of Kimmel Gerke Associates, West St. Paul, Minn. The class is directed at common EMC problems in portable electronic equipment and solutions for them. The session starts with the "Physics of EMI," emphasizing the FAT-ID (frequency-amplitude time impedance and dimensions) approach to grounding and shielding as related to portable design. It then continues with a number of case histories of EMC problems, along with how they were solved. This is a nuts and bolts approach to the design issues commonly encountered in electronics design.

Dozens of power-converter and switching-regulator ICs are currently

WORKSHOP & CONFERENCE SCHEDULE

Monday Workshops	8:30 A.M. — 5:00 P.M.	1. Battery Basics
	8:30 A.M. — 5:00 P.M.	2. EMC Problems and Solutions for Portable Electronics
	8:30 A.M. — 5:00 P.M.	3. Designing with DC-DC Converters
	8:30 A.M. — 5:00 P.M.	4. Working with the IrDA Serial Infrared Protocol
Tuesday Technical Sessions	8:30 A.M. — 11:30 A.M.	1. Defining and Overcoming End-User Battery Frustrations
	8:30 A.M. — 11:30 A.M.	2. MCUs and CPUs for Portable Devices
	12:00 P.M. — 1:30 P.M.	KEYNOTE LUNCHEON sponsored by Benchmarq Microelectronics
	1:30 P.M. — 4:30 P.M.	3. Designing with Current and Future Battery Technologies
	1:30 P.M. — 4:30 P.M.	4. CPU Power Supply Voltages: How Low Can They Go?
	2:00 P.M. — 8:00 P.M.	EXHIBITS OPEN
	5:00 P.M. — 8:00 P.M.	INDUSTRY RECEPTION, sponsored by Intel Corporation (Exhibit Floor)
Wednesday Technical Sessions	8:30 A.M. — 11:30 A.M.	5. Software: System Management and PC Card Issues
	8:30 A.M. — 11:30 A.M.	6. RF-Based Wireless LAN and WAN Technologies
	10:00 A.M. — 6:00 P.M.	EXHIBITS OPEN
	11:00 A.M. — 12:00 P.M.	BOB PEASE PRESENTATION
	12:00 P.M. — 1:30 P.M.	BOX LUNCH served on Exhibit Floor
	1:00 P.M. — 2:00 P.M.	PEASE AUTOGRAPH SESSION
	1:30 P.M. — 4:30 P.M.	7. Smart-Battery Management Architectures Addressing Multiple Battery Chemistries
	1:30 P.M. — 4:30 P.M.	8. IR-Based Wireless Communications
	6:00 P.M. — 9:00 P.M.	PORTABLE AFTER DARK I: Infrared Technology
	6:00 P.M. — 9:00 P.M.	PORTABLE AFTER DARK II: RF Technology
	6:00 P.M. — 9:00 P.M.	PORTABLE AFTER DARK III: Smart-Battery Technology
Thursday Technical Sessions	8:30 A.M. — 11:30 A.M.	9. Systems, Buses, and Architectural Issues
	8:30 A.M. — 11:30 A.M.	10. Thermal and Mechanical Considerations
	11:00 A.M. — 2:00 P.M.	EXHIBITS OPEN
	1:30 P.M. — 4:30 P.M.	11. Low-Power Analog Circuit Design
	1:30 P.M. — 4:30 P.M.	12. PC Cards and Other I/O

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	SFH617A	X	X	X	X
	SFH6156	X	X	X	X
6-Pin Single	CNY17	X	X	X	X
	CNY17F	X	X	X	X
	SFH600	X	X	X	
	SFH601	X	X	X	X
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available in the marketplace. The key for designers is choosing the one that's best suited for their particular application. But there are the inevitable questions. What about the magnetics? What kind of capacitors work best? What's the best method of laying out the circuit board so that the converter can be tested and also work properly without radiating noise and interference? The answers to these questions and other related issues will be found in the Designing With DC-DC Converters full-day workshop, presented by Eric Persson of Analog Circuit Design, Minnetonka, Minn.

Want To Go?

The Portable By Design Conference and Exhibition will be held at the Santa Clara Convention Center, Santa Clara, Calif. The technical sessions run March 25-27, while the workshops take place March 24. The exhibition area is open March 25-27. The keynote address and luncheon, featuring speakers from Advanced Risc Machines (ARM), Intel, Motorola, and Texas Instruments, will take place on March 25 at 12:00 noon. For more information, contact Betsy Tapp at (201) 393-6075 or send an e-mail to portable@class.org.

The IrDA Protocol

Presented by a team representing the Infrared Data Association (IrDA), the "Working With the IrDA Serial Infrared Protocol" workshop takes a close look at particular aspects of the IrDA standard. The specific topics include the Physical Layer, the Link Access Protocol (IrLAP), the Link Management Protocol (IrLMP), the Tiny Transport Protocol (TinyTP), and Serial and Parallel Port Emulation (IrCOMM). The instructors will start with an overview, then go into detail on each of the subjects. They will conclude with a series of implementation and testing strategies.

Each of the twelve three-hour technical sessions in the main program covers a different aspect of designing a portable product. In chronological order, the session titles are:

"Defining and Overcoming End-User Battery Frustrations,"

"MCUs and CPUs For Portable Devices,"

"Designing With Current and Future Battery Technologies,"

"CPU Power Supply Voltages: How Low Can They Go,"

"Software: System Management and PC Card Issues,"

"RF-Based Wireless LAN and WAN Technologies,"

"Smart-Battery Management Architectures Addressing Multiple Battery Chemistries,"

"IR-Based Wireless Communications,"

"Systems, Buses, and Architectural Issues,"

"Thermal and Mechanical Issues,"

"Low-Power Analog Circuit Design," and

"PC Cards and Other I/O" *(see Schedule At A Glance).*

As portable equipment proliferates, users of products ranging from laptops to cellular phones are experiencing problems with batteries. Not that battery technology hasn't improved over the years. In fact, batteries have come a long way in terms of power density, life, and weight. But users and their applications have become more demanding. Batteries must provide longer lifetimes while driving ever-more-powerful laptops, must shrink to fit into diminutive cellular phones, must indicate their available power and when they're close to running out, must charge quicker, and must not pollute the environment with dangerous chemicals when discarded. The session will isolate the major problems users are running into, and discuss how design engineers can best incorporate today's battery technologies to overcome end-user frustrations and concerns.

Future Battery Technologies

Until someone discovers how to accomplish nuclear fusion within the confines of a matchbox, power consumption will continue to be the Achilles' heel of portable-equipment designs. Take heart, however, as much progress has been made in the areas of operating life and power density for both standard and rechargeable battery cells. Session three will discuss the present state of affairs with respect to the various battery chemistries, along with predictions of where the technology is headed in the the not-too-distant future. The pros and cons of each technology, in addition to the best methods of incorporating these devices into upcoming designs, will be discussed.

The need for multichemistry and multivendor options is expanding as system designers strive to use the latest battery technology, while meeting user and market demands for price- and cost-performance and reliability. The session titled "Smart-Battery Management Architectures Addressing Multiple Battery Chemistries," reviews various smart-battery architectures and explains how they apply to today's portable systems. The presenters, representing various industry leaders, will show and review examples of real-world battery-management architectures and circuits.

Portable systems often require a mix of low-power processors—both a high-performance 32-bit or larger CPU that tackles the heavy-duty compute tasks and a lower-performance 4- to 16-bit microcontroller that can handle the I/O, and mostly non-compute-critical tasks. The MCUs and CPUs session will cover two areas: X86-based solutions for low-power systems and other processor architectures for low power.

The trend over the last few generations of microprocessors is to reduce the supply voltage. Session four looks at where the CPU voltage level is headed, and what it takes from a power supply perspective to support that voltage. In addition, speakers from companion-product companies will describe how the changing voltage level affects overall board and system designs. Speakers in the Low-Power Analog Circuit Design session will describe techniques and ICs for building low-power analog circuits and subsystems. They also will delve into power-management designs. Application examples will be provided.

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NDS355AN	NDS356AP	75	140	SuperSOT™-3
NDC651N	NDC652P	42	95	SuperSOT™-6
NDH853N	NDH854P	15	29	SuperSOT™-8
NDS8410A	NDS8435A	10	21	SO-8
NDT455N	NDT456P	13	26	Power SOT
NDM3000**		70	125	SO-16

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**SO-16 Contains 3 N-Channel and 3 P-Channel die in one package

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While portable- and embedded-system developers often come from hardware backgrounds, there are many software-based elements to contend with in these systems. Actual software development may not be required, but the portable designs do necessitate some understanding of how parts of the software operate and how they interrelate, such as the system-management (BIOS) functions, power management, and the PC Card issues. With all the standards now in existence, understanding the software is becoming a complex puzzle. The "Software: System Management and PC Card Issues" session will look at some of these software (and firmware) issues, giving hardware designers just the kind of information they need to understand the software.

Wireless Communications

Infrared (IR) data is rapidly becoming a must-have technology for the next generation of portable equipment. Thanks to its low cost and simplicity, it is becoming the favored data-transfer technology for everything from PDAs and PCs to meter readers and medical equipment. The IR-related session will provide an introduction to the technology and explore some of the technical challenges faced by designers when designing IR-based wireless data systems. Although the session will focus primarily on the short-range, point-to-point IrDA standard, other technologies concerned with IR design also will be discussed. The program will feature important topics such as sensor selection, processor-interface design, and software development.

On a larger scale, the RF-based session has been organized to help address some of the technical challenges involved in designing RF-based wireless data systems. A series of how-to papers will be presented, giving novices and experienced engineers practical insights into various aspects of designing and testing these systems. Both component-level and system-level topics for LAN and WAN technologies will be explored. Technologies presented at this session will include the IEEE 802.11 Wireless LAN standard, PCS short messaging technologies, and cellular packet data transmission.

Although the spotlight often is drawn to a portable system's trouble spots, such as the batteries and the CPU, bus issues are steadfast in all portable designs. Session nine will highlight some of the newer bus techniques and implementations, including the Zoom Video (ZV) port, CardBus, and docking considerations. Among the system-level topics to be discussed are speech recognition, alternative input devices, and handling multimedia on a portable PC.

A PC Card slot has become a must-have feature on a notebook computer, especially those that don't contain a floppy-disk drive. But the PC Card slot isn't just for notebooks anymore. Slots are now appearing on equipment such as palmtop PCs, vertical computing devices, and even industrial portable embedded systems. At the Portable By Design conference, these topics will be discussed in the "PC Cards and Other I/O" session. This session will look at the various I/O issues, including PC Cards, and how to implement those methods. Moreover, these issues will intertwine with a topic that's always a source of contention for portable-system designers that of , power-management. Other topics will include CardBus and multifunctionality.

Lastly, the presentations in the Thermal and Mechanical Issues session will concentrate on the pragmatic thermal and mechanical methods being implemented by OEMs to address the unique problems associated with notebook computers. The thermal portion of the session will provide insight as to how computational fluid dynamics can be used early in the design process. The session continues with specific discussions on the cooling of microprocessors. A special case on treating known good die in an MCM format also will be discussed. The session's mechanical portion looks at the shock mechanism of notebook computers, and how thermal solutions are ruggedized and integrated into the final product. MCM substrates also will be discussed.

How Valuable	Circle
Highly	540
Moderately	541
Slightly	542

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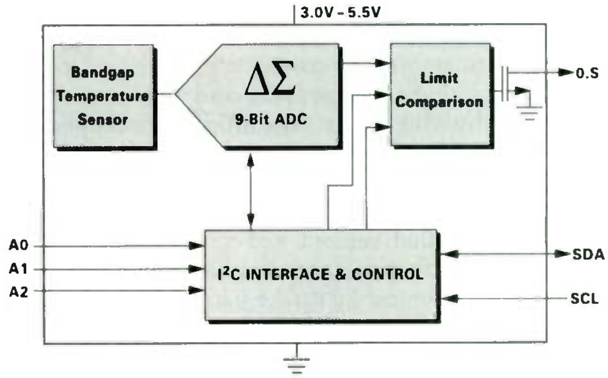

Yes, the **LM75** temperature sensor is cool. And it'll keep your system that way too.

The LM75 integrates an I²C interface and a 9-bit ΔΣ ADC on one chip. In addition to measuring temperature, it can also function as a digital thermostat, featuring programmable hysteresis. And its output can be set up to provide a conventional comparator response or a read-resettable interrupt flag.

With an accuracy of ±2°C from -25°C to +100°C, 3.3V or 5V operation, and 1mA quiescent current, the LM75 is ideal for a wide variety of thermal management and protection applications.

The LM75 temp sensor. The price is a cool *$1.40 (1000 units). And we've put together a free demo board and software so you can see for yourself how cool it will keep your system.

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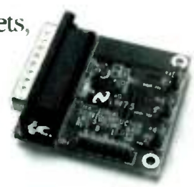

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Drag-And-Drop Tool Helps To Create And Modify Intelligent Drawings

An intelligent technical drawing tool lets users easily create, modify and share engineering and schematic drawings across the office or across the Internet. Visio Technical 4.5 provides sets of predesigned drag-and-drop drawing objects that can be combined, modified, resized, and configured and saved as new objects. While Visio Technical 4.5 can be used by those core CAD users who don't require direct output to production equipment such as EDA or pc-board design tools, it's also aimed at "adjacent" CAD users. Adjacent CAD users are people who generally work with, but don't create, CAD drawings.

Visio Technical can, for example, import .DWG drawing files created in AutoCAD. The Visio versions of the drawings would then become available to people involved in manufacturing and assemble, construction, product support, and maintenance. Beyond that, however, the shapes supplied with Visio, as well as the custom shapes created by the user, are intelligent objects with their own dynamic properties. This, along with the implementation of Microsoft's Visual Basic for Applications (VBA) and ActiveX capability inside Visio, makes it possible to create intelligent drawings for demonstrating concepts, maintaining inventory, and monitoring and controlling industrial processes.

In its simplest form, Visio provides a set of "stencils" that contain drawing objects *(see the figure)*. For example, a stencil contains a set of electronic symbols that can be dragged and dropped onto a page. Then you can connect the symbols, and resize and reorient them to create a schematic.

Beneath the symbols and the page, however, is a layer of software called the "shape sheet." It keeps track of the connections between objects, as well as other properties like color, size, associated text, etc. The status of one shape might depend on the status of another. For example, a lamp could be set to yellow when a given switch is set to closed.

The data in the shape sheets can be associated with ODBC database files using the database Wizard for such things as producing a parts list. Using the VBA and ActiveX capabilities, it would be possible to extract the connection data between shapes and produce a net list from a schematic or to import data logged to a spreadsheet to change the display state or color of shapes to monitor an industrial process. A program could animate a state transition diagram or flow chart to show logic flow in a software design.

In addition to importing drawings from AutoCAD, Visio Technical 4.5 has file converters for CorelDRAW, CorelFLOW, and Micrografx Designer. It also can save drawings as JPEG, GIF, and PNG formats for posting drawings to the World Wide Web. Enhanced web capabilities include the ability to generate a set of HTML pages from a set of drawings.

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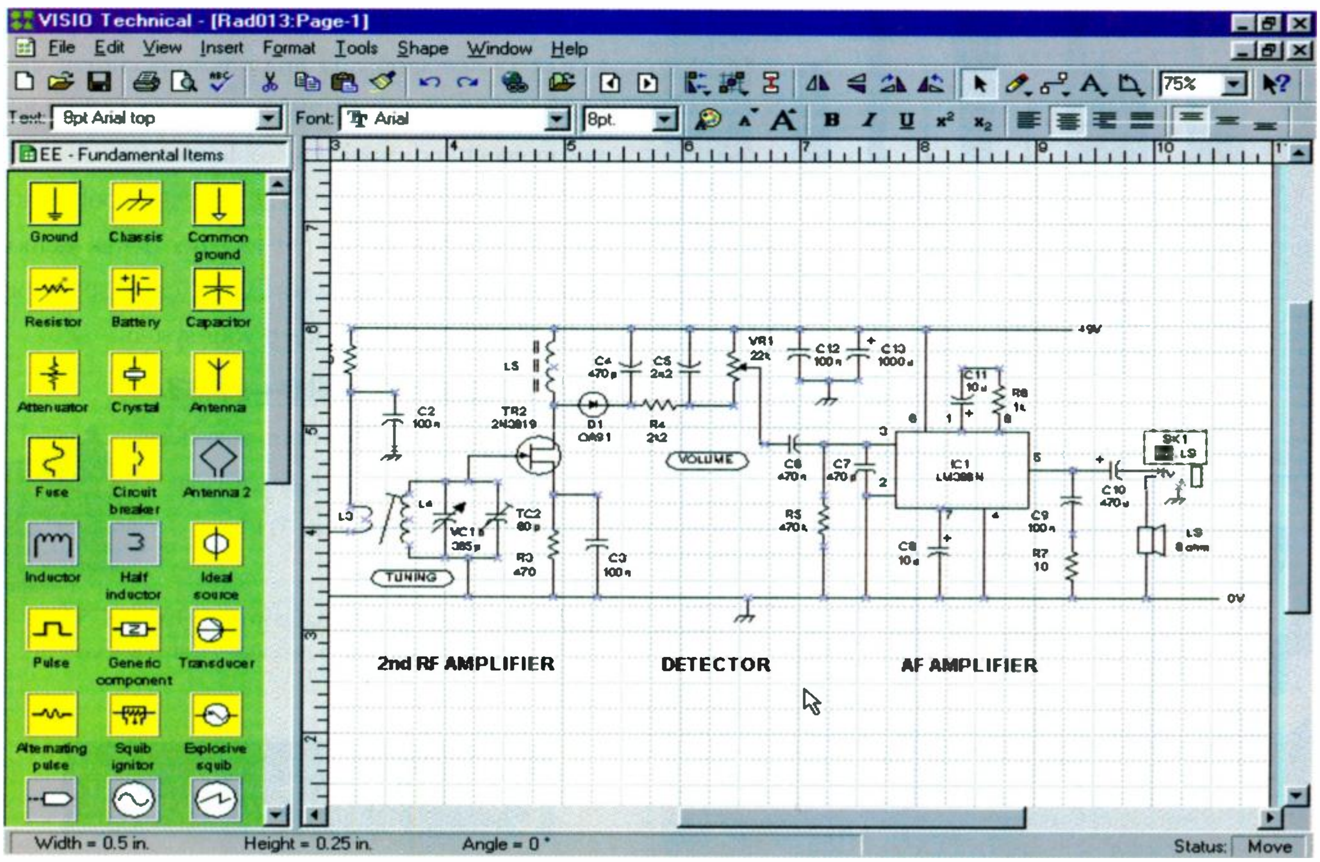
Seattle, WA 98101
(206) 521-4500
http://www.visio.com
CIRCLE 470
TOM WILLIAMS



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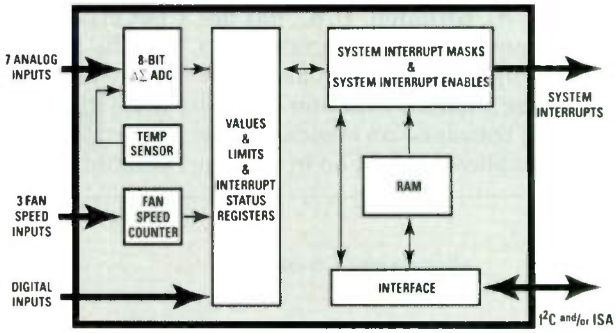

The **LM78.** Think of it as an early warning system for your system.

The LM78 monitors a wide variety of analog and digital functions. Including temperature, up to 7 analog voltage inputs (2 of which can be negative), fan speed and chassis security. It's user programmable. And it offers a choice of interfaces to your system, ISA bus and I²C.

The LM78 even helps you cut costs. First, you'd need several of anybody else's chips to monitor even half what it monitors. Second, it can cut your warranty costs (and/or your customer's cost of ownership) by catching small problems before they become big ones.

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PRODUCT FEATURE

GEC Plessey Unveils Details About Digital Satellite Tuner Chip Set

GEC Plessey Semiconductors (GPS), Swindon, U.K., has developed a highly integrated chip set for digital satellite tuners that complies with all common digital satellite transmission standards. Its major application will be in set-top boxes for the new TV service being put in place there.

The chip set includes an L-band mixer oscillator, a family of low phase noise PLL synthesizers, and a quadrature downconverter. According to a company spokesman, the new chip set "provides the highest level of tuner integration from any IC solution," because only a small number of active RF components, a reference crystal and surface acoustic wave (SAW) filter together with a small number of passive components are needed to build the complete tuner.

To evaluate the chip set, the company has created a demonstration board that contains support circuitry for standalone functional bench demonstrations of the chip set from L-band to I & Q analog buffered outputs. The board also is able to fully interface with an ADC and a QPSK/FEC block. This means that the board can demonstrate the functionality as a complete digital satellite front end from the L-band to the data stream.

Several front-end ICs are included: First of all, there's the satellite tuner IC SL2015, which is a full integrated mixer/oscillator with an RF input range from 0.75 to 2.15 GHz and dual-selectable AGC controlled IF outputs operating up to 550 MHz.

Two key ICs are the SL1711/14 and SL1713 I/Q IF downconverters. While the SL1711/14 downconverts QPSK/QAM signals from satellite digital video broadcasts, the SL1713 does the same in cable systems.

Another important front-end part is the SP5658/59 low-phase-noise frequency synthesizer that operates up to 2.7 GHz. The SP5658 is controlled via a three wire bus, but the SP5659 is an I^2C bus-controlled device. Together with the SL2005, the SL2001 is claimed to be the first bipolar broadband double-conversion chip set in the world. The SL2001 is a 1.2-GHz cable upconverter and SL2005 is a 1.3-GHz downconverter.

Furthermore, GPS offers ADCs for the set-top box in its chip set. They perform 90 Msamples/s for satellite applications (VP21X family) or 40 Msamples/s for cable applications (VP23X family). Finally, the VP305 is a DVB-compliant single-chip decoder for use in digital satellite TV receivers. It receives digitized I & Q signals and provides QPSK demodulation as well as all forward-error-correction functions.

In the fourth quarter of 1997, the VP320 is projected to arrive on the market—a device that will provide

(continued on page 50)

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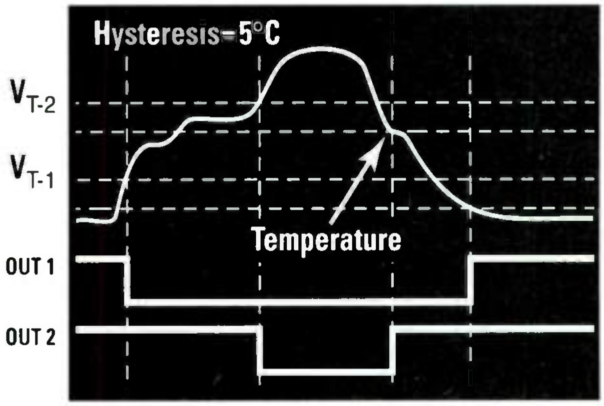

The **LM56** is one cool dual, in more ways than one. By detecting two separate temperature thresholds, it'll keep your system running cool. It's operating range is -40°C to +125°C. It's accurate to ±3°C. All you need to do is add 3 external resistors to set the trip points. And it includes hysteresis for each output set internally.

And the LM56 itself runs cool. It requires a mere 230μA of current. It's the first dual thermostat to operate on supplies as low as 2.7V. And it's available in compact SO-8 and, soon, SOT-8 packaging.

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(continued from page 48)
DVB-compliant channel decoding for digital cable receivers. This IC will comprise digital demodulation of up to 256-level QAM and the required error-correction functions.

For the decoder module, the company provides the VP400 MPEG-2 A/V chip, which is a single chip DVB-compatible MPEG-2 audio/video and transport demultiplexer chip capable of real-time decoding of ISO1318 (MPEG-2) and ISO11172 (MPEG-1) bit streams up to 72 Mbits/s. It includes a 2-bit/pixel or 4-bit/pixel OSD (on-screen display) function and requires 16 Mbits of SDRAM to decode both PAL/NTSC signals and OSD overlays. For enhanced OSD features, it also supports 32-Mbit SDRAMs.

The VP500 video encoder family consists of six digital-to-analog video encoders for converting REC656 data into PAL/NTSC composite and S-Video signals. Variants will provide true composite, inverted composite, RGB, and Teletext, as well as anti-copying circuitry.

The VP542 audio digital-to-analog converter is a complete 20-bit, delta-sigma DAC that uses a combination of switched capacitor and continuous time filtering. An internal clock generation unit allows the device to lock to several clocking frequencies, including the 27 MHz system clock. The generaton unit is also capable of supplying the common multiplies of the audio sampling frequencies used by most MPEG decoders. The device offers six audio sample rates (16 to 48 kHz) as well as direct connection to 54, 27, and 13.5 MHz.

Last but not least, GEC Plessey offers the SL5162 multistandard video modulator, which is able to handle PAL/SECAM/NTSC signals with stereo-sound capability. In addition to these ICs, the company has a license from ARM (Advanced RISC Machines)to use the company's 32 bit ARM RISC core.

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United Kingdom, SN2 2QW
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fax: +44(0)1793 518481
CIRCLE 471
ALFRED VOLLMER

Low-Cost Univeral Serial Bus Microcontroller Simplifies The Design of Peripherals

Since it conforms with version 1 of the USB 1.5-Mbit/s specification (low-speed option), a family of 8-bit RISC microcontrollers is able to drive down the cost of implementing the Universal Serial Bus on various peripherals.

Developed by Cypress Semiconductor in cooperation with Microsoft Corp., the microcontrollers are targeted at low-cost peripherals such as mice, joysticks, game pads, and keyboards. Growing markets that don't require blazing data-transfer rates (for example, home security, sprinkler control, and similar applications) also can take advantage of Universal Serial Bus as an interconnection technology.

To meet the cost target of less than $1 per chip to the OEMs, designers at Cypress kept the chip area to just 5900 mils^2 while including 2- or 4-kbytes of EPROM or ROM for program storage. That's about half the area of any commercial 8-bit general-purpose microcontroller.

Additional, more complex devices and some simpler devices will be available from Cypress by the end of this year. Some of the forthcoming devices will be targeted at Universal Serial Bus hub design and others targeted at the faster, 12-Mbit/s version of the USB standard.

The CY7C63000/1 and 63100/1 USB microcontrollers include a 34-instruction CPU, which has instructions optimized for use with USB. Also on-chip are 2 or 4 kbytes of EPROM/ROM, 128 bytes of RAM, and a watchdog timer.

There are 10 to 16 I/O lines that have programmable sink currents. The I/O lines don't require external sink resistors. When indicators are needed, designers can use "random," unmatched LEDs to further reduce system cost.

A clock-doubling circuit is used on the microcontrollers so that the chips can operate from a 6-MHz external crystal to ensure low EMI emissions. The chips also feature a zero-power "instant-on" capability to lower power consumption by 70% when idle, while being able to provide full asynchronous response.

Furthermore, the controllers perform direct-memory-access data transfers from the internal RAM rather than from dedicated FIFO buffers. This, in turn, saves a significant amount of chip area.

In addition to the microcontrollers, the company offers a USB developer's kit. The kit gives designers a full-speed hardware emulator module, development software, a power supply, and complete documentation, enabling immediate development of firmware and associated system drivers. Among the tools included in the developer's kit are an assembler, a debugger/monitor with full debug environment (break traps, single stepping, and register-, RAM- and I/O-display and modification), and an optional logic-analyzer interface.

With the emulator connected to the host computer's 9- or 5-pin serial port, designers can implement the firmware in either the on-chip EPROM or on the host system and downloaded to the program RAM. By using the RAM-based storage, firmware can be modified quickly by using the debug interface to alter bytes of code.

Program sizes of up to 8 kbytes are supported by the emulator. Cypress also has developed sample libraries of Universal Serial Bus application code to help accelerate development of peripherals.

The CY7C63000 MCU contains 2 kbytes of EPROM and sells for $1.80 in lots of 10,000 units (20-lead SOIC package). The 7C63001 device has 4 kbytes of EPROM and costs slightly more.

Available in 24-lead packages, the 7C63100 and 63101 offer more I/O lines and start at $1.98 apiece, also in 10,000-unit lots. In large volumes, these chips eventually will sell for less than $1 each. The developer's kit goes for $1500.

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PRODUCT FEATURE

VLIW Architecture Offers A Ten-Fold Improvement In Digital Signal Processing

Delivering a peak throughput of 1600 MIPS when clocked at 200 MHz, the TMS320C6201 fixed-point digital signal processor is the first in a new DSP family based on a very-long-instruction-word architecture called VelociTI. Developed by Texas Instruments, the new architecture delivers almost 10 times the performance of DSP chips currently available from any current vendor. Thus, for applications like wireless base stations, remote-access servers, pooled modems, cable modems, and digital-subscriber loop systems, the chip can implement the system at about half the cost per channel versus other DSP solutions.

The VLIW architecture of the CPU core consists of eight functional units—two multipliers and six arithmetic units—that together can execute eight instructions per cycle. The core is configured as two parallel data paths. Each data path contains one multiplier and three arithmetic units that can handle 40-bit arithmetic operations. Designed to operate from a 3.3-V supply, the DSP chip actually internally cuts that to 2.5 V to reduce power consumption, and at the same time keeps all of the I/O lines 3.3-V compatible.

The chip contains both program and data caches, each containing 512 kbits of SRAM storage. The data cache can hold 8-, 16-, or 32-bit data values, while the instruction cache is organized as 2048 words by 256 bits. Other resources on the chip include a dual-channel bootloading DMA controller, a 16-bit host-access port, two buffered serial ports, a pair of 32-bit timers, and a 32-bit interface to external memory.

The long instruction word allows simple instruction packing to reduce the code size, the number of program fetches needed, and the power consumption. Instructions are all conditional, which reduces costly (in terms of time) branching operations and enables increased parallelism for higher sustained performance. For example, a 1024-point complex FFT is executed in just 70 µs. Or, one 320C6201 can implement a bank of 10 to 15 V.34 modems at about $6 per modem.

However, programming VLIW processors has traditionally been a challenge to keep track of all operations and data movement. To alleviate that headache, TI's designers crafted an intelligent C-language compiler that averages about three times the efficiency of other DSP compilers. Those results are based on DSP algorithms written in C and compiled for several processors. Also available is an assembly optimizer and a Windows-based debugger interface.

Tools are available for both PCs and Sun (or compatible) workstations, and a hardware emulation board, compatible with TI's XDS50 JTAG emulator interface, is also available. The PC-hosted version of the tools sell for $2995, while the Sun version sells for $4995. Third-party tools also are available from many suppliers, such as Ariel Corp., D2 Technologies Inc., DSP Research Inc., GO DSP Corp., HotHaus Technologies Inc., Innovative Integration, Pentek Inc., White Mountain DSP, and others.

Housed in a 352-contact ball-grid-array package, the DSP chip will sell for $96 each in lots of 25,000 units. For designers that can't wait, the advance-release version of the chip, available now, will not have the timers and serial ports. The fully equipped version will be ready in the second quarter.

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Semiconductor Group, SC97001A
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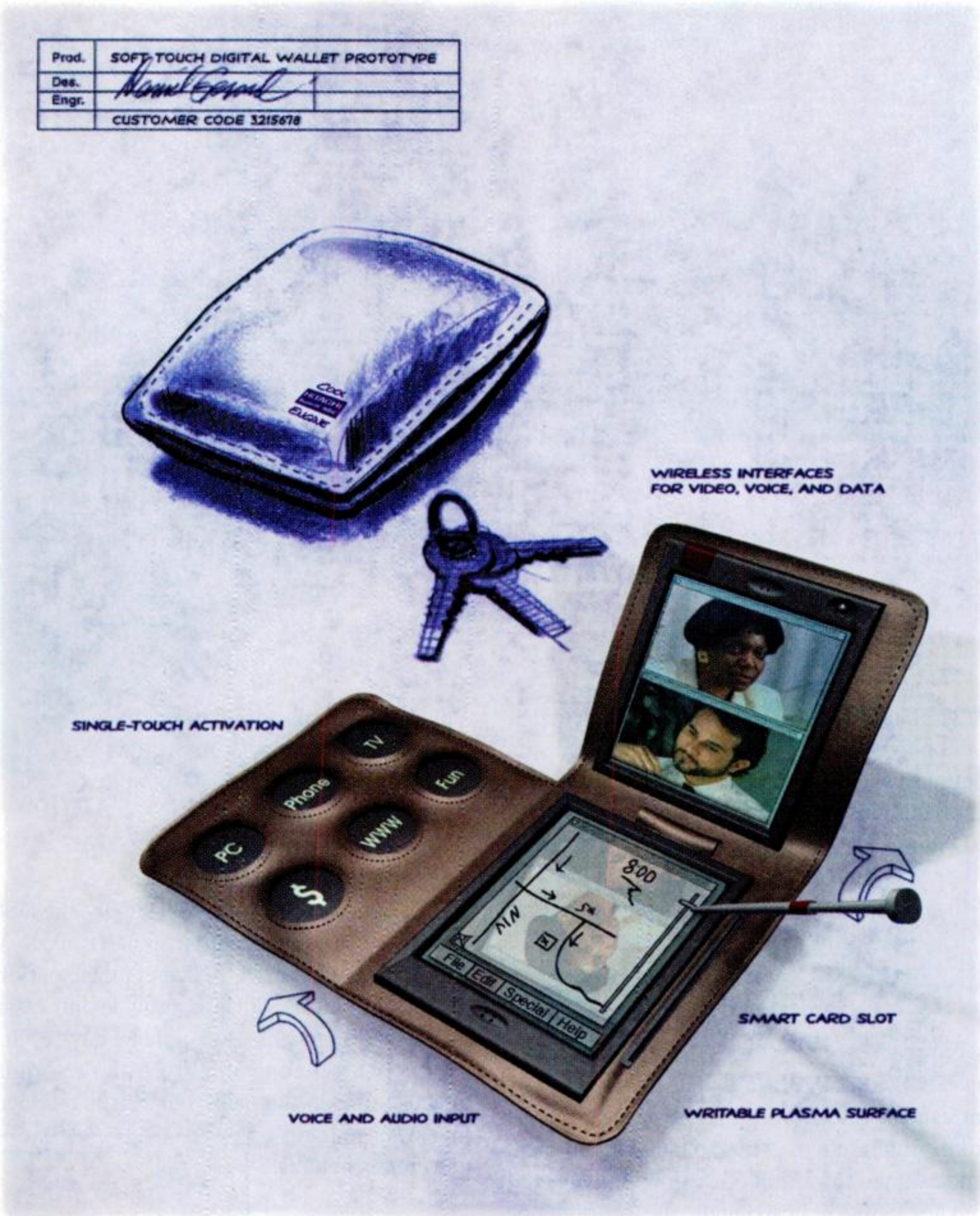

This Wallet May Not Exist Yet, But The Microprocessor For It Does.

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Because that's where the electronics revolution is headed. Off the desktop and out into the world at large.

It's a journey that requires an entirely new microprocessor technology. One that does far more with far less in terms of power consumption, space requirements and cost.

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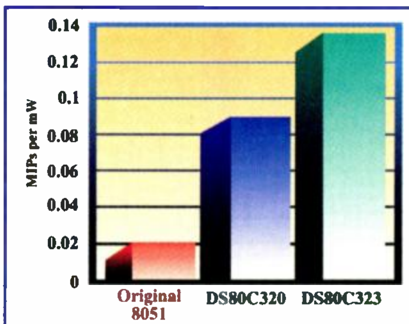

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Automated Virtual Prototyping Tool Delivers Optimized PCB Placement

PC-Board Design Tool Offers Low-Cost And Quick Placement In A Concurrent Environment.

Cheryl Ajluni

COVER FEATURE

Engineers with expertise in multiple disciplines are rare. Typically, individual experts in hardware, electromagnetic interference (EMI), thermal management, signal integrity, and manufacturing each worked autonomously on the placement of a design. For example, the EMI expert would do his work and then throw it over the wall to a thermal expert. Oftentimes, however, the thermal expert would find that changes made to EMI cause additional changes to the thermal results. After revising his work, the thermal expert would throw it back to the EMI expert, who would face the same problem. This resulted in a long, drawn-out series of sequential iterations between the experts until they eventually converged on an averaged solution. Adding an electrical, routability, and manufacturing experts to the mix only made things more complicated.

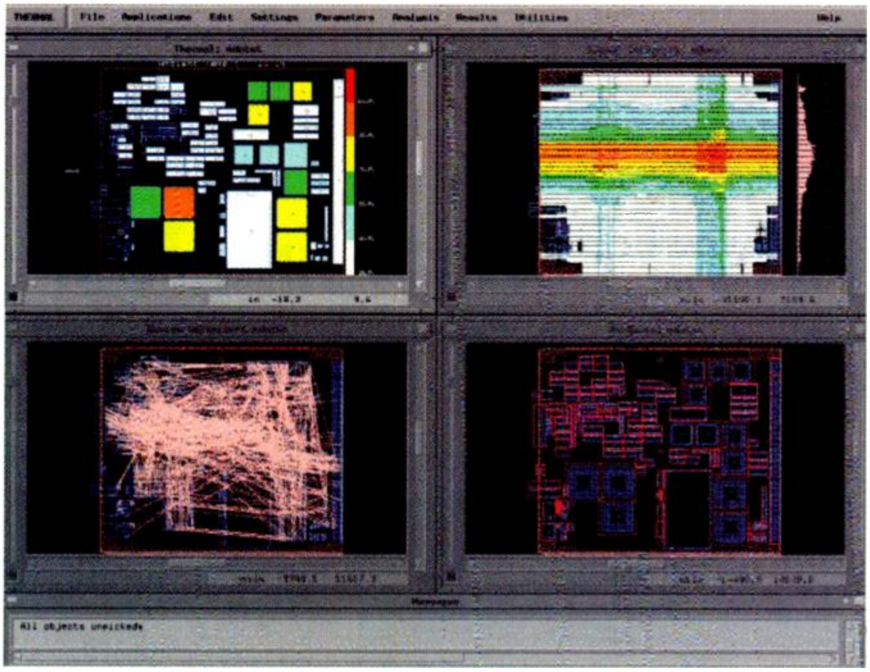
With the growing complexity of designs, pc-board (PCB) layout has become even more difficult, leaving designers with basically two choices. They either have to become experts in multiple disciplines, or they have to find tools that will do the job for them. With the sequential hardware design process no longer meeting the needs of today's designer, and the days of multi-disciplined engineers long gone, today's PCB designer is now forced to opt for the second choice, and seek out expert PCB placement tools.

Recognizing this need, UniCAD Inc., Ottawa, Canada, has come out with an expert tool intended to convert the more conventional sequential placement process into a concurrent one *(Fig. 1)*. Known as the Multi-Disciplinary Optimizer (MDO), this virtual prototyping tool enables automatic multi-disciplinary optimization of PCB placement. Based on a trade-off engine with discrete optimization algorithms, the PCB designer is able to rank the importance of each discipline for use in the optimization process, and more importantly, can regain control over the PCB design process.

Using an algorithm that acts like a neural net, effectively learning on the go, the tool quickly and automatically makes placement decisions based on user-defined constraints. This is significantly faster than the more conventional method and drastically cuts down on the number of iterations before layout. And, because it occurs in the physical synthesis part of a design, a PCB designer is free to explore design opportunities *prior* to making any commitments.

Over the past few years, UniCAD has developed a suite of virtual prototyping tools, which included the UniSolve tool for pc-board analysis, and SyntheSolve, an all encompassing tool that features automated synthesis capabilities with constraints generation. While a separate tool, SyntheSolve borrows heavily from the UniSolve tool suite. MDO further builds on this virtual prototyping environment by expanding on the SyntheSolve base. It does this by moving the synthesis further upstream in the design process so that the designer can have an earlier optimization of placement. In the past, the only early optimization available to designers was for interconnect. With MDO, the entire placement process can be optimized.

As one part of the virtual prototyping methodology, MDO takes advan-



1. MDO performs early optimization of critical design constraints—delay, emissions, thermal, routability, and manufacturability—in a concurrent tools environment. The delay, EMI, thermal and routability constraints are simultaneously and automatically adjusted by changes within each discipline.

tage of a number of benefits inherent to virtual prototyping which brings a design's back end further up front and automates the design process. It allows iterations to be done early on so that the results can be recorded for later design reuse. And, it means capturing the behavior of a design not yet implemented and using the representation for manipulation in exploration and analysis.

It truly is a different paradigm for hardware development. The MDO tool successfully leverages these features, making it possible to further inform the design process earlier on, and allows the designer to look at the design in a number of different ways *before* committing to one particular placement.

How It Works

MDO is launched as a separate application from within the UniSolve suite. A design file is read into UniSolve to provide the basic design data. Once the application is launched, additional information, such as defined goals or constraints, are entered by the designer to drive the optimization algorithm.

Of the five disciplines now supported by MDO, four are explicit and are user selectable—electrical, EMI, thermal, and routability. The manufacturing constraint that maintains inter-component clearance is built in to ensure that final placement is feasible from a manufacturing perspective.

The constraints make heavy use of signal and device attributes to define the rules required and to formulate the cost function. These attributes can be entered at the schematic-capture or layout phase to help guide the optimization algorithm. Besides the explicit constraints, physical rules such as locking or physical grouping of components also can be created and applied by the user on-the-fly or read in from the design file during design optimization. In addition, any restricted areas created during layout are supported by the placement algorithm.

The electrical discipline supported by MDO deals specifically with issues of radiated EMI and interconnect delay. For the EMI estimation analysis, algorithms are used to predict the radiated emissions from signal interconnections. To compute the interconnect delay, UniSolve's Signal Integrity analysis capabilities predict the interconnect flight time. The analysis capabilities are accessed once again to compute the package junction temperature for thermal analysis. Specifically, the rise in the junction temperature of the component is obtained by computing the temperature change at different levels of packaging and the board under natural or forced convection.

For routability analysis, a logic length computation of the design signals is required. This is accomplished by a fast algorithm using the minimum spacing tree method. A bounding box is created so that all pins on the signal are contained within the box. The half-perimeter of the bounding box is then determined. For manufacturing analysis, keepout areas for each component, defined as the minimum clearance for neighboring components, are calculated automatically within the MDO application. While keepout areas for adjacent components may overlap, the physical body of any component may not overlap within keepout areas. The user can make changes to these values if necessary.

Once all design requirements are entered, optimization begins using the initial placement as a benchmark *(Fig. 2)*. A cost function is evaluated for the benchmark and used to compare against all subsequent placements. Before each iteration of the design placement begins, the current placement is perturbed by randomly shuffling a random section of the board. With each new placement, the required analyses are performed and the cost function is evaluated. If it is accepted by the algorithm, the board's current state is stored. If not accepted, the placement is discarded and the process begins again until the optimization-controlling parameters determine that the total number of required iterations has been reached. When the optimization cycle is complete, the layout deemed by the optimizing algorithm to be optimal becomes the placement of the board.

A prime benefit of the MDO tool is its ability to do automated synthesis of device placement by optimizing for multiple conflicting sets of constraints. This optimization is quite simple to do with just a few signal nets. With thousands of nets, however, the problem becomes exacerbated. For example, a designer wishing to perform optimization based on thermal and EMI disciplines faces a dilemma. For thermal optimization, the components have to be as far apart as possible. Whereas for EMI optimization, the components have to be as close together as possible to mini-

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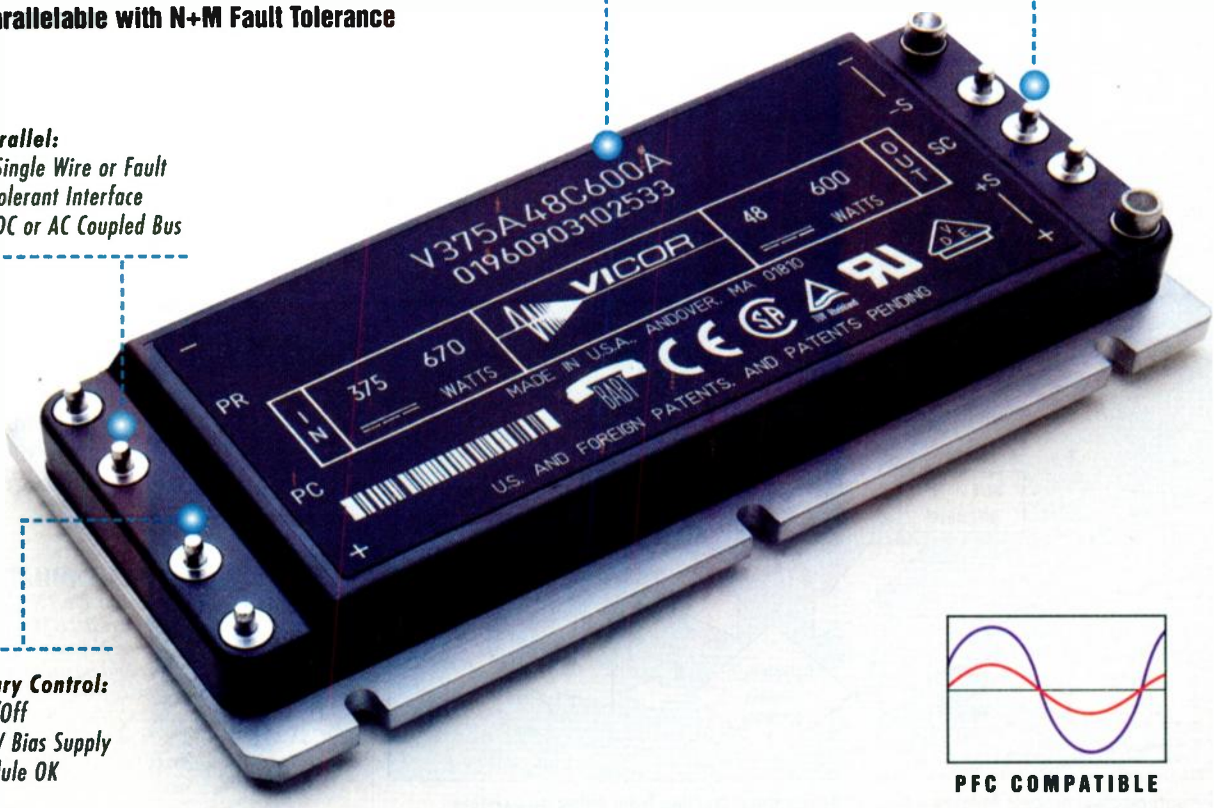

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mize interconnect length, in turn, decreasing radiation. With the MDO tool, the designer is able to place a level of importance on the different disciplines to signify which should be weighted more heavily during optimization of the automated device placement process.

Automation, as a key benefit of the MDO tool, offers an easy means of optimizing pc-board layout based on a number of different disciplines, and does it in a very short period of time. Though the layout could be done by hand by an experienced engineer, it would take an incredibly long time. MDO's automatic-layout capability on the other hand offers a significant time savings. And, it provides the designer with a high level of confidence that the design has been fully optimized and that nothing was inadvertently left unchecked.

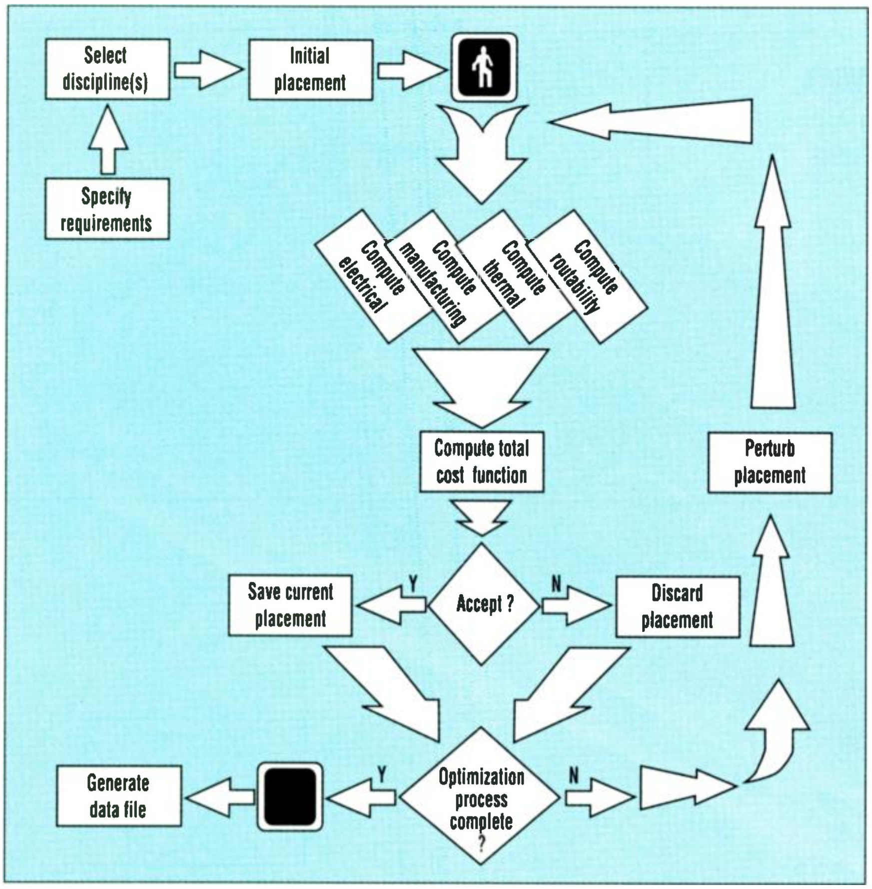
The optimization process can be done either automatically by the application or interactively so, for example, the engineer can set constraints on a certain level of EMI. The optimization would then take place based on this information. When the process is completed, the designer can make decisions based on whether or not the resulting values in the other four disciplines are acceptable for the design. If optimizing the one constraint causes a design problem, the designer can simply make changes to the specified design constraints and rerun the optimization until an acceptable layout is obtained. Consequently, control over the weighting of the different disciplines rests solely on the designer's shoulders.

A significant feature of the MDO tool is the effect it is has on the process of iterations. Historically, iterations have been looked down upon because they were typically done very late in the design cycle, when the risk and cost is substantially higher. But, it's not really the concept of iterations that is bad; it's where the iteration is placed within the design methodology. With MDO, designers can explore the design space early on in the design cycle before the design intent is captured. They can, for example, move components around on the board to see in concurrent time the affect the change will have on the different disciplines and on layout

MDO tool changes the implementation of iterations in today's design methodology. Currently, iterations are employed after the implementation process to settle on the most optimum layout. This approach typically requires many iterations and comes late in the design cycle when major changes can be costly. With MDO, iterations occur prior to implementation when the design is still a concept. This method, which really boils down to an automated floorplanning exercise, is significantly shorter in the long run because it drastically cuts down on the number of implementation iterations. And, because the number of hardware iterations through backend processes is significantly decreased, the cost is lower.

Another interesting feature of the MDO application is that it meets all the necessary placement requirements, and does so in an esthetically pleasing, and somewhat artistic, manner. Consequently, the design placement or layout is in a representation that is more like what designers are used to looking at, as opposed to just a variety of components thrown haphazardly on a board.

The future of the MDO tool lies in expansion of the selection of supported disciplines. Currently, the company is looking at the possibility of offering support for ground noise/ground bounce effects.



2. The optimization process follows a distinct design flow, starting from either an existing placement, or a random placement to create a unique placement. Once started, the optimization analysis runs thousands of times on thousands of placements. The tool saves the best placement and then proceeds by looking for incremental improvement in the next placement. Once completed, the results of the optimization are passed back to the host CAD system using the delt- file capability within UniSolve.

PRICE AND AVAILABILITY

The MDO tool runs on a UNIX platform on Sun OS/Solaris, HP and IBM workstations, and on a Windows NT environment. Available now, the tool, sold as an add-on application to UniSolve, sells for $21,000.

UniCAD, Inc., 2745 Iris St., Ottawa K2C3V5, Canada; Stephen Lum, Product Marketing Manager, (613) 596-9091.

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EDA WATCH

Growing A New Interface: Model Technology And The Grass Roots Movement To Tcl/Tk

Shepherded by its creator John Ousterhout and foster parents Sun Microsystems, Tcl has grown almost organically into its new role as one of the preferred development tools for Graphical User Interfaces (GUIs) as a universal scripting language. With functionality that matured through an Internet-wide group development effort, Tcl and Tk, its GUI development kit, meets many of the fundamental needs of CAD developers, third-party integrators, and end-users looking to customize their simulation environment.

Tcl is a powerful and highly adaptable glue that connects Tk library components, while also controlling their interactions with other applications. In its role as a universal scripting language, Tcl is an effective interface for joining a Tcl interpreter to an existing C program, giving the application access to Tcl's simple, flexible syntax. With Tcl's rich set of commands able to be embedded into a number of applications, developers may find it easier to build Tk-based interactive user interfaces.

That was an appealing characteristic to designers at Model Technology. They were faced with the need to create a variety of new user interfaces for their HDL simulators, and Tcl/Tk's accessibility of Tcl/Tk was a determining factor. They could now quickly create new user interfaces without having to write hundreds of thousands of lines of C code for each new application. This can be compared to how assembly languages gave way to a simpler and higher programming language such as C. Tcl/TK is a simpler and more abstract language than C for developing GUI's or integrating tools together. Tcl/Tk's portability also made it easier to create or modify custom interfaces for a variety of different platforms.

Tcl/Tk's position as a completely open standard, available without cost to anyone who wants to use it, made it even more attractive. Instead of paying licensing fees, Model's engineers just downloaded the source code from the nearest Web browser. They also were impressed with Tcl/Tk's broad acceptance by other developers. Already in use by tens of thousands of programmers, it has been subjected to enough use—and abuse—to prove its robustness. This will enable end-users who either use or develop a Tcl/Tk utility or application on one Tcl/Tk-supported application to reutilize it on all Tcl/Tk-supported applications. This level of openness should result in a mass proliferation of Tcl/Tk widgets and applications for users to download and customize.

Dave Griffin of Digital's Alta Vista Forum echoed many users when he said, "We selected Tcl as our scripting language because it was open, robust, highly extensible, and has a very nice book describing it."

Tcl/Tk's industry-wide popularity also presented other opportunities that revealed themselves as Model Technology moved further through its own development cycle. Because Model maintained an ongoing dialogue with its V-system VHDL simulator users, they already knew about their urge to "tinker with the tools." The people who work with Model's products show that they like to modify the tools they work with every day to meet their special needs. The company was happy to inform its users that the new Tcl/Tk-based interface was completely open, so they could tinker to their heart's content.

Tcl/Tk's higher level of programming abstraction now allows users to create "virtual prototypes" of designs they are simulating. One customer example that was turned into a workshop was the design of a traffic control system. Tcl/TK was used to create a "virtual prototype" of the traffic intersection. The simulation results were graphically animated and the behavior observed. Even the stimulus was controlled with a GUI. The frequency of cars arriving to the intersection were

What's On The Horizon

With a number of critical issues being raised by the migration to deep-submicron design geometries, the EDA and ASIC industries are struggling to bring some sense and understanding to the confusion. One of the more critical issues coming to light is whether or not the industry is outpacing today's design methodology as well as the tools that support it. This is especially prevalent in lieu of the current industry trend to move away from simulation accuracy and toward speed. Basically, simulator performance is impacted whenever accuracy is increased. In addressing the simulation speed issue, EDA tools have now been introduced into the marketplace that provide the added simulator performance at the expense of accuracy. With design complexity rapidly increasing thanks to shrinking geometries and the crunch toward faster time to market, designers need tools that can provide better cycle times. The end-user expects both the EDA and ASIC vendors to ensure that speed and accuracy are there. Deep submicron brings many new challenges in the modeling of device delays and interconnect, for example, that cannot be ignored.

The real dilemma lies in determining how much accuracy and speed is required during the various design processes and which verification methodologies are appropriate. And taking this a step further, what is the design flow that will accommodate these choices, and how should it be implemented? There are a number of tools currently on the market, along with different design techniques, that offer hope for a solution to the accuracy and verification time dilemma. While there are those who may choose to stand behind a single solution as the optimal approach to solve this problem, there are those who believe that ultimately, the future may lie in the combination of many solutions used in conjunction with a totally new design flow. These are some of the hard choices that will be facing vendors and designers alike.

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The extensions that have been created range from simple menu changes to sophisticated graphic representations of product behavior, and they're only just getting started. A lot of customer feedback new examples of user creativity almost every day. In each case, the Tk-GUI toolkit has allowed users to modify the interface and make the simulation process more graphical.

The growing acceptance of the Tcl/Tk standard presents other possibilities. It is expected that third-party software developers will take advantage of Model's open interface by developing add-on products. In addition, OEMs and VARs also will be free to adapt the look and feel of the simulator when they bundle it with their products. In any case, the openness of the standard and the open characteristics of the product's interface can be expected to provide a wide variety of growth opportunities.

A rapidly expanding number of other commercial uses for Tcl/Tk's capabilities also are appearing, including applications from Motorola, Wind River, Sybase, Oracle, and Digital's on-line AltaVista Forum. One of the newest advances in the Tcl/Tk development is showing up on the Internet, where a Tcl plug in allows standard HTML-based web browsers to view new content types such as Tcl "Tclets." Native Windows and Macintosh implementations are now in nearly-final beta versions and scheduled for release as Tcl 7.7 and Tk 4.3 later this year.

Why has Model Technology chosen to open up its product in this way, and why did Model decide to implement the new open system in Tcl/Tk? The answers are both practical and philosophical, reflecting a sensible need to make the product easier to manage, and a general conviction that only open systems can withstand the challenges of constant growth.

Contributed by Greg Seltzer, marketing manager, Model Technology, Beaverton, Oregon, (503) 641-1340, e-mail: greg_seltzer@model.com.

To obtain additional information on this topic, see Model Technology's web page at http://www.model.com., or read "Practical Programming in Tcl and Tk" by Brent B. Welch.

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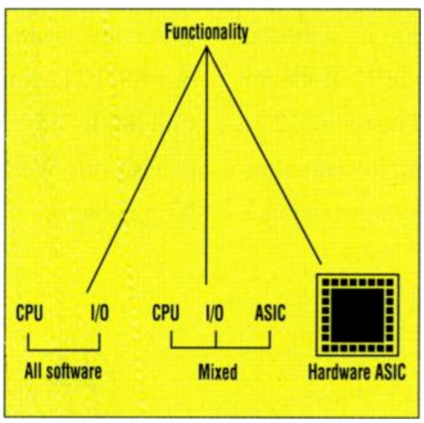
Because of the growing complexity of digital systems and the availability of a variety of implementation technologies, many of today's digital designs are mixed hardware-software systems. The hardware and software elements may be physically separate components, or they may be the same physical components viewed at different levels of abstraction. In either case, it's sometimes possible to integrate the hardware and software design into one design methodology.

Design automation for mixed hardware-software systems has evolved from the merging of IC design and programming *(Fig. 1)*. If we have some functionality to be implemented as a digital system, we could implement it as a program running on a processor (shown on the left-hand side of Figure 1), or as a hardware ASIC (shown on the right-hand side of Figure 1). Design aids, such as compilers and logic-synthesis tools, have been developed to support both of these options. More recently, however, design aids have been developed to support design in the middle ground of Figure 1, in which the final implementation includes both a software program and a specially-designed hardware element.

The design of mixed hardware-software systems presents several challenges to the designer. Not the least of these is the fact that while the hardware and software components are often interdependent, they are typically described and designed using different formalisms, languages, and tools. Hardware-software codesign is an attempt to integrate hardware and software design techniques with the goal of incorporating more of the system design process into a single design methodology.

Combining hardware and software design into a common methodology or automation tool has several advantages. One is that including more of the overall system design into one automated or structured design methodology may accelerate the design process. Another is that addressing hardware and software design simultaneously under a single methodology may enable hardware-software trade-offs to be made dynamically as the design progresses, thus giving the designer more flexibility in finding the optimal combination of hardware and software.

The potential benefits of integrating hardware and software into a single design methodology has driven quite a bit of research into hardware-software codesign over the past several years. However, due to the wide range of assumptions made in each case, it's often difficult to compare approaches to codesign. This article attempts to lend some structure to the field of hardware-software codesign by defining some terminology and suggesting some criteria that can be used to understand and compare new ideas. The suggested criteria is based primarily on the nature of the mixed hardware-software system and the design activities for which hardware and software are integrated.



1. Digital-system functionality can be implemented in a variety of ways. For example, it can be implemented as a program running on a processor or as a hardware ASIC.

Hardware-Software Systems

The primary consideration for many types of hardware-software codesign is the nature of the system being addressed. It's important to understand what constitutes hardware and software and the relationship between the two. The distinguishing factor is whether the boundary between hardware and software is a logical boundary (Type I) or a physical boundary (Type II).

In a Type I system, the hardware is thought to be executing the software, and so the relationship is one of abstraction level *(Fig. 2a)*. A Type I system may contain one or more physical components. An example of a Type I hardware-software system is one made up of a microprocessor and its associated glue logic. In this case, the hardware, which is probably specified as a microprocessor type and a net list of gates, is viewed at a much lower level of abstraction than the software, which is likely to be specified using a high-level programming language.

In a Type II hardware-software system, the hardware and software components are modeled at the same level of abstraction, but are physically separate components *(Fig. 2b)*. An example of a Type II hardware-

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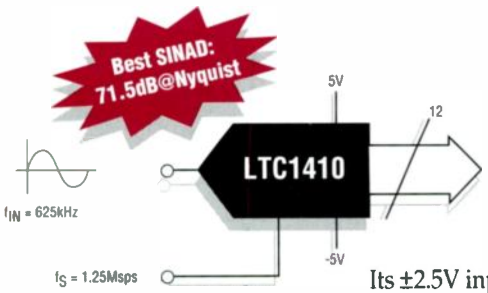

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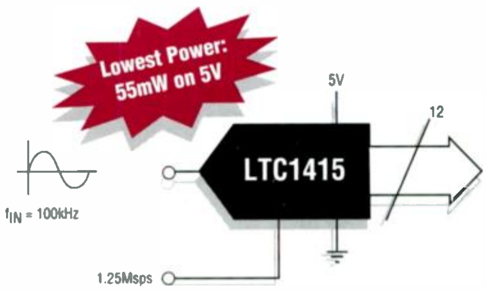

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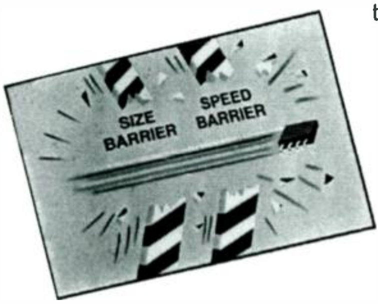
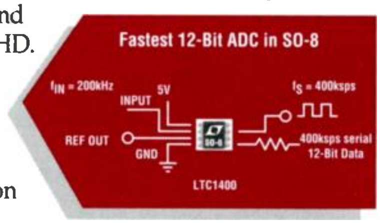


The LTC1400 has the smallest footprint available and true 12-bit performance at Nyquist. Maximum DC specs include 1LSB DNL and INL, and 25ppm/°C drift for the reference over temperature. The LTC1400 converts 0V to 4.096V unipolar signals from a single 5V supply or ±2.048V bipolar signals from ±5V supplies. Guaranteed AC performance includes 70dB SINAD and –76dB THD.

For high speed data acquisition systems, the LTC1400 offers two power savings modes. These allow the ADC to sample quickly but save power between samples. In NAP mode, it consumes only 6mW and can wake up and convert immediately. In SLEEP mode it uses just 30µW. At $9.95 in 1000-piece quantities, the LTC1400 is the only choice for 400ksps performance in an SO-8 package.



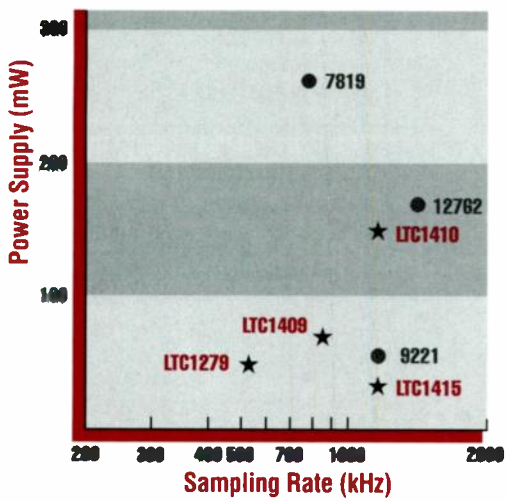
Circle No. 212

Now in SSOP: High Speed ADC Family

Faster, Better, Lower Power and Now Smaller Size

Linear Technology's high speed 12-bit ADC family has grown again and is now the smallest in the market—available in Shrink Small Outline Packages (SSOPs)!

Power Consumption of High Speed 12-Bit ADCs



Table—High Speed Parallel 12-Bit ADC Family

	LTC1279	LTC1409	LTC1410	LTC1415
Sampling Rate	600ksps	800ksps	1250ksps	1250ksps
Power Supply	5V or ±5V	±5V	±5V	5V
Power Consumption	60mW	80mW	150mW	55mW
SINAD at Nyquist	70dB	72dB	71dB	72dB*
Packages	SSOP-24 SO-24	SSOP-28 SO-28	SSOP-28 SO-28	SSOP-28 SO-28

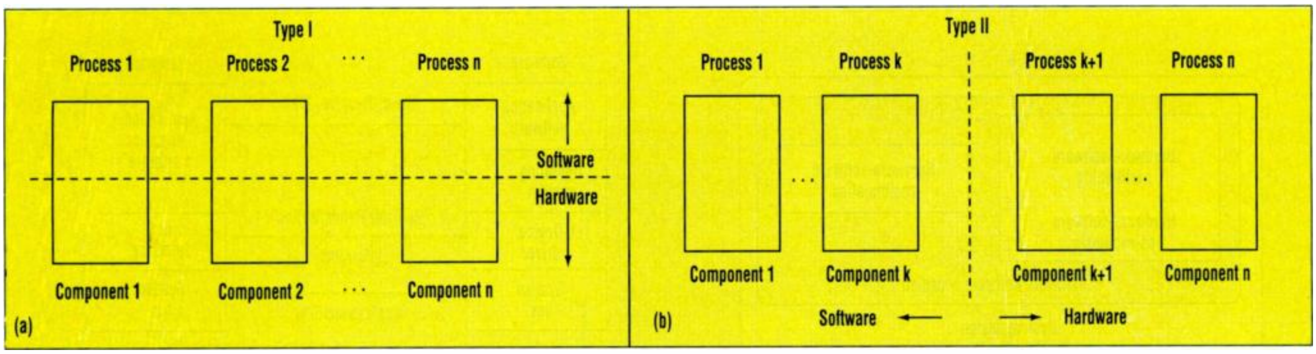
* At f_{IN} = 100kHz

These high speed ADCs span a range of sampling rates from 600ksps to 1.25Msps.

This family is ideally suited for communications applications including single-pair or dual-pair T1 and E1 applications. Excellent SINAD specifications and low power make them excellent choices for undersampling and high speed data acquisition applications as well. They offer both NAP and SLEEP modes for optimum power consumption in event-driven applications.

The industry's smallest footprint is the latest reason to look at our high speed 12-bit ADC family. See why we are *The New Choice in Data Conversion:* Linear Technology.

Circle No. 214



2. In hardware-software codesign, it's important to understand what constitutes the hardware and software and the relationship between the two. The distinguishing factor is whether the boundary between hardware and software is a logical boundary (a) or a physical boundary (b).

oftware system is one comprising oth a microprocessor and a special-urpose computing engine. If the pecial-purpose engine is designed ısing behavioral synthesis techniques, then the hardware, which is specified by a behavioral description, an be modeled at roughly the same vel of abstraction as the software.

Finally, it's conceivable that a hardware-software system could represent a mixture of Type I and Type II hardware-software boundaries. But to our knowledge, no published work has addressed this situation.

System Design Tasks

In addition to characterizing the type of the hardware-software system, it's also useful to characterize he design tasks included in the codegn methodology. The simplest disnction is the design activities for hich hardware and software are integrated *(Fig. 3a)*.

Simulation of hardware-software ystems, sometimes called hardare-software cosimulation, repreents the problem of modeling the ehavior of a system based on the beavior of components that have difering semantics and that may be deribed in different languages. The urpose of cosimulation may be to lesh out the functionality of hardware and software early in the design process or to integrate the two late in the design process. It may be aimed at verifying the functionality of the system[1,2] or at evaluating the performance.[3,4]

Hardware-software cosimulation requires a simulation environment that can understand the semantics of both the software and the hardware omponents and how actions in one domain affect the state of the other. The interaction of the hardware and software components may be modeled at a variety of abstraction levels *(Fig. 3b)*.

At the lowest level, the interface between the hardware and the software may be modeled by the activity on the pins of a CPU or the wires of a bus.[3] This approach is most accurate for evaluating performance, but is computationally expensive. If the hardware and software elements of the system communicate asynchronously, the interaction could be modeled at a high level by the process or device communication mechanism provided by an operating system.[1,2] This approach is much more efficient computationally, but isn't as useful for evaluating performance.

Codesign also may include integrated synthesis of hardware and software components, which we refer to as hardware-software co-synthesis.[5,6,7,8] Co-synthesis might involve designing the interface between the hardware and software components, configuring multiple heterogeneous processors and their interconnections through shared memories, or designing custom assist processors.

In addition, automated hardware-software co-synthesis may allow the designer to explore more of the design space by dynamically reconfiguring the hardware and software to find the best overall organization as the design evolves. This can lead to better results than could be achieved if the hardware-software architectures had to be specified up front during the early stages of the design. To do this, the design tools must understand the relationship between the hardware and software organizations and how design decisions in one domain affect the options available in the other. It also requires an understanding of how the overall system cost and performance are affected by the hardware and software organizations.

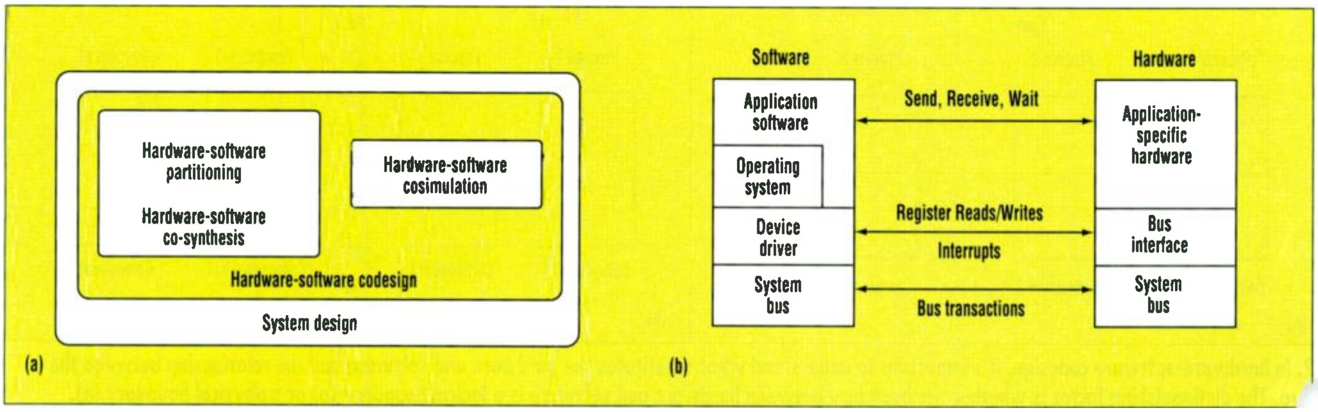
Unification

Another challenge for hardware-software co-synthesis is that hardware and software are often described using different languages and formalisms. If a design methodology considers moving functionality back and forth between hardware and software, a unified understanding of hardware and software functionality must be reached.

Codesign methodologies that include hardware-software co-synthesis may be further distinguished by whether hardware-software partitioning is performed and the factors that influence the partitioning. Hardware-software partitioning is possible whenever the design methodology allows for a choice between using hardware and software to implement some function.

For ASIC design, partitioning is well-understood: given a set of interconnected logic elements, split them into two or more non-overlapping subsets and minimize the interconnections that cross the boundary. However, in hardware-software codesign, we don't have logic elements at the start. Rather, we have behavioral (program-like) descriptions of the functionality to be implemented.

Behavioral partitioning was developed by McFarland,[9] and later Lagnese,[10] and Vahid.[11] The idea was to partition closely related features



3. It's useful to characterize the design tasks included in the codesign methodology (a). Simulation of hardware-software systems requires modeling th behavior of a system. The interaction of the hardware and software components may be modeled at a variety of abstraction levels (b).

of a behavioral description. These features included variables, operators, basic blocks, and procedures. Essentially, these partitioning schemes detect code locality, grouping entities that interact with each other. Hardware-software partitioning has grown out of behavioral partitioning, and includes the consideration of whether hardware or software is a better implementation choice for each entity.

Partitioning

Many factors may influence the hardware-software partitioning problem. These factors fall into three broad categories: Nature of the computation, implementation constraints, and managerial considerations.

Nature of Computation: The complexity of the computation influences partitioning. Some systems fall into the category of concurrent state-machine design. A dashboard controller for a car is a typical example where the functionality being implemented is control-dominated. That is, there's very little data processing, but there's a lot of condition checking and signal activation. In contrast, a video compression or handwriting analysis algorithm generally results in a far more complex system.

The functionality in question may also have an affinity for either hardware or software. Computations that benefit from a high degree of data parallelism, or require nontraditional logic operators, may be better suited for hardware. Signal processing is an example of the first category, and encryption is typical of the latter.

For Type II systems, hardware-software partitioning implies physical partitioning. In this case, the partitioning problem is complicated by the following issues:

1. Concurrency—Concurrency is the parallel execution of two separate, communicating processes. If the software and hardware components don't run in lock-step, the best system performance may be achieved by partitioning the functionality among concurrent hardware and software components.

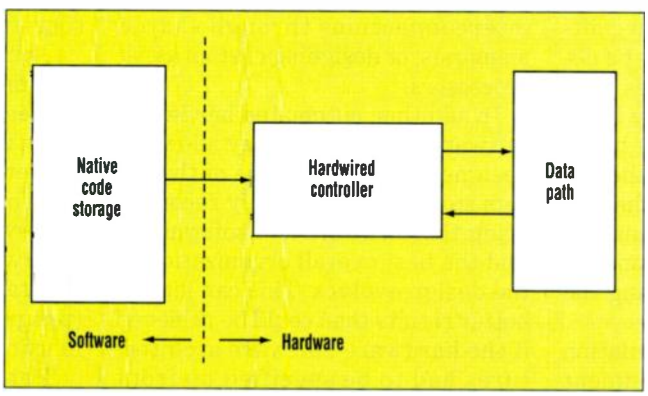
2. Communication—The overhead of synchronization and data transfer among concurrent hardware and software components is likely to have a significant impact on overall performance. This fact favors partitions that localize communication, even at the expense of other considerations.[10]

Implementation Constraints: Finding an effective hardware-soft ware partition may involve cons ing the cost of producing a hardw implementation of some of the func tionality. Functions that have a si nificant impact on the overall performance of the system may need to be implemented in hardware. This could be the case even if a hardware implementation of the function offers only a modest improvement in performance. If hardware resources can be shared among functions, it also may be necessary to consider how the partition impacts the sharing.

Managerial Considerations: Sometimes a software implementa tion is desired so that the function algorithm can be easily change Typically, this is a managerial/ma keting constraint that overrides tl above technical considerations.

Codesign Examples

Because a great many types digital systems include bot hardware and softwar there are numerous examples of hardware-softwar trade-offs. In this section, we will briefly cite two examples of systems that include hardware and software elements and afford ample opportunity for hardware-software codesign and trade-offs. Each example is characterized by what the designer considers the hardware and software components to be, and what sort of hardware/software part



4. For the example of an application-specific instruction set processor, the hardware-software boundary lies between the software running on the processor and the processor itself.

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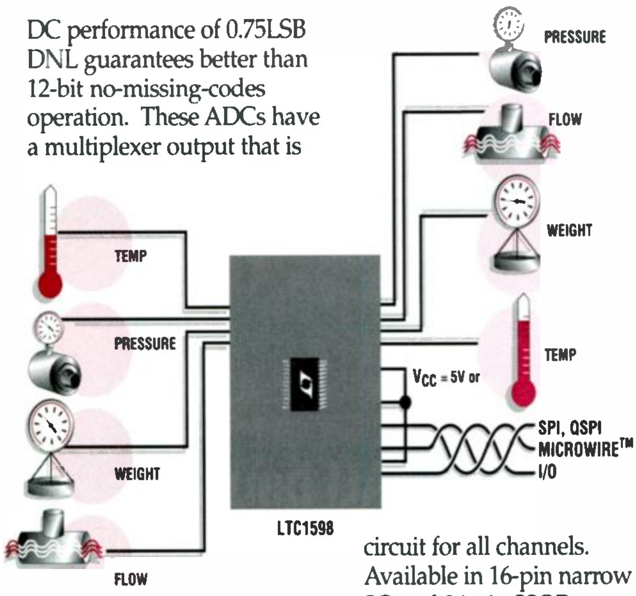
The LTC1594/1594L and LTC1598/1598L are 4- and 8-channel 12-bit micropower ADCs for single 5V and 3V applications. These small footprint ADCs are ideal for remote process control, portable data acquisition and other space conscious, power sensitive applications.

The 5V LTC1594 (4-channel ADC) and LTC1598 (8-channel ADC) typically draw just 320µA at 16.8ksps sampling rate while the 3V LTC1594L/1598L draw only 160µA at 10.5ksps. They all automatically power down to 1nA when not converting. These are the lowest power multiplexed 12-bit ADCs in the industry.

DC performance of 0.75LSB DNL guarantees better than 12-bit no-missing-codes operation. These ADCs have a multiplexer output that is separate from the sample-and-hold input which allows for one signal conditioning circuit for all channels. Available in 16-pin narrow SO and 24-pin SSOP packages, they start at $6.15 for 1000-piece quantities.



Circle No. 216

Micropower Operation Down to 480µW, These 12-Bit Multiplexed ADCs Offer 0.75LSB DNL

Micropower Dual and Quad DACs Fit in Tight Quarters

The LTC1446/1446L, LTC1454/1454L and LTC1458/1458L are a new family of 12-bit dual and quad DACs. A 3-wire serial interface allows several of these DACs to be daisy-chained to save board space. They are perfect as system calibration DACs in industrial control systems or in portable battery powered instruments.

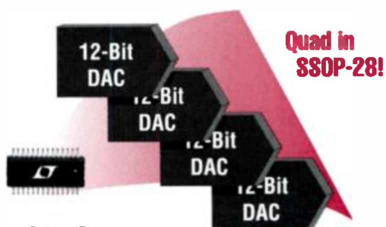
Key Features:

- Micropower
- Rail-to-Rail output amps
- Onboard reference
- 5V or 3V supplies

Table—Micropower V_{OUT} DAC Family

	LTC1446	LTC1446L	LTC1454	LTC1454L	LTC1458	LTC1458L
Type DAC	Dual	Dual	Dual	Dual	Quad	Quad
Supply Voltage	5V	3V	5V	3V	5V	3V
Supply Current	1.0mA	650µA	700µA	450µA	1.1mA	800µA
DNL (Max)	0.5LSB	0.5LSB	0.5LSB	0.5LSB	0.5LSB	0.5LSB
Packages	DIP-8	DIP-8	DIP-16	DIP-16	SO-28	SO-28
	SO-8	SO-8	SO-16	SO-16	SSOP-28	SSOP-28
Price-1K	$6.40	$6.50	$6.60	$6.70	$11.75	$12.50

LTC1446



LTC1458

Circle No. 218

Dual DAC in SO-8 Leads Family of Dual and Quad 12-Bit DACs with DNL of Only ±0.5LSB Max

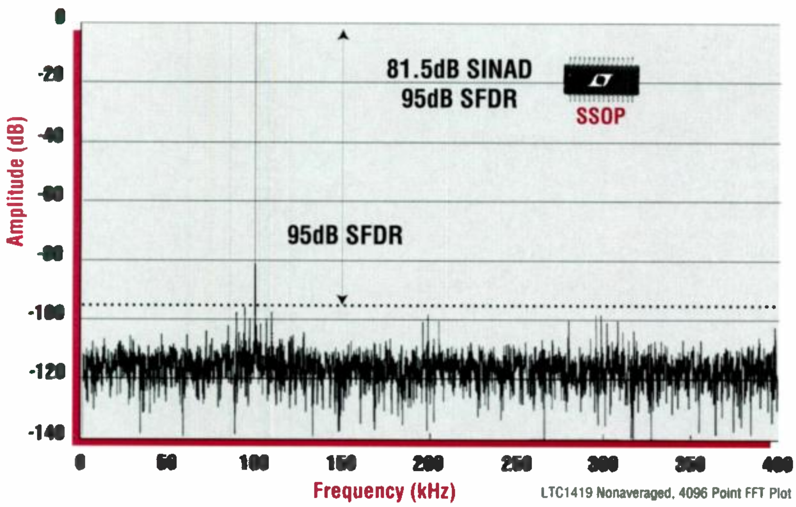
New!

LTC1419: Upgrade Your System with 81.5dB SINAD at an Affordable Price

The Cleanest 14-Bit, 800ksps ADC Offers DNL of ±1LSB Over Temperature, Consumes Only 150mW

Linear Technology now offers you an upgrade path for your existing high performance 12-bit system without resorting to expensive hybrid A/D converters. The LTC1419 is an 800ksps 14-bit ADC that has 81.5dB SINAD and 95dB SFDR, the cleanest in the industry. It's ideally suited for demanding telecom, IF down conversion, undersampling and multiplexed data acquisition applications.

With 20MHz full power bandwidth sampling, the LTC1419 gives you the cleanest 14-bit performance—setting your high speed communications system above the rest. A maximum DNL of ±1LSB over temperature ensures clean 14-bit DC performance as well. The 800ksps LTC1419 has no pipeline delay such as found with multistep architectures.



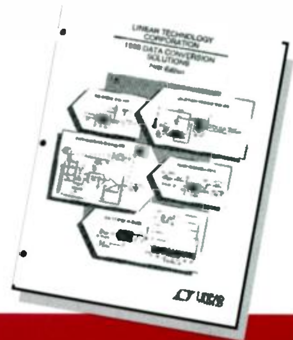
The LTC1419 consumes only 150mW of power from ±5V supplies and has NAP and SLEEP shutdown modes. It comes in 28-lead SO and SSOP packages and has similar pinouts to Linear Technology's high speed 12-bit parallel A/D converters, such as the LTC1415 and LTC1410, simplifying your upgrade path to 14-bit resolution. Pricing for the LTC1419 begins at $16.80 in 1000-piece quantities.

Circle No. 220

New Data Conversion Solutions Brochure

The *1996 Data Conversion Solutions* is a 52 page brochure that contains LTC's growing line of data conversion products, namely A/D converters, DACs, multiplexers/switches and references as well as practical tips on how to apply them. There are 60 products described and 24 application notes for your review.

Circle No. 222



For more details, contact Linear Technology Corporation, 1630 McCarthy Blvd., Milpitas, CA 95035-7417, Web Site: www.linear-tech.com. (408) 432-1900. Fax: (408) 434-0507. For literature only: 1-800-4-LINEAR.

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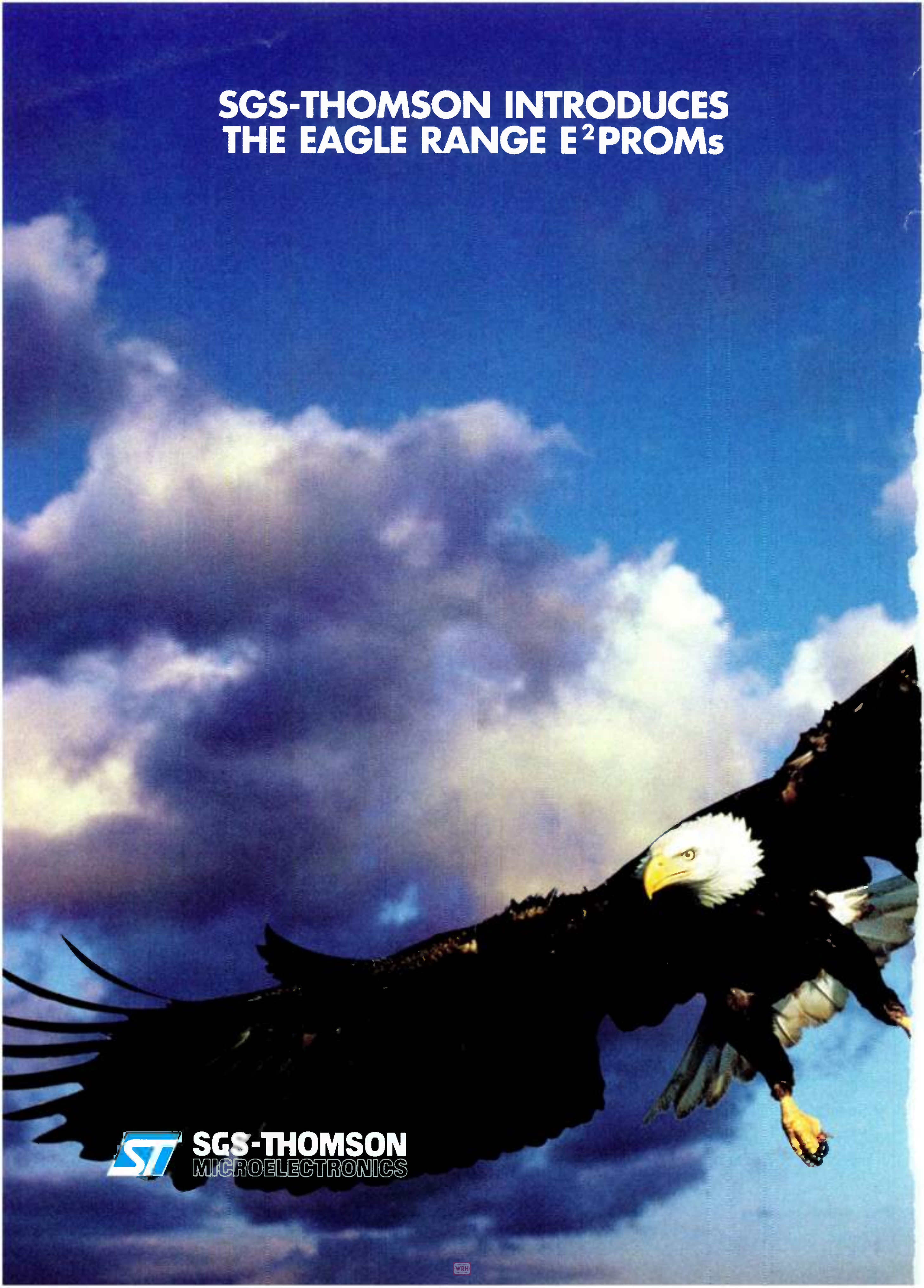
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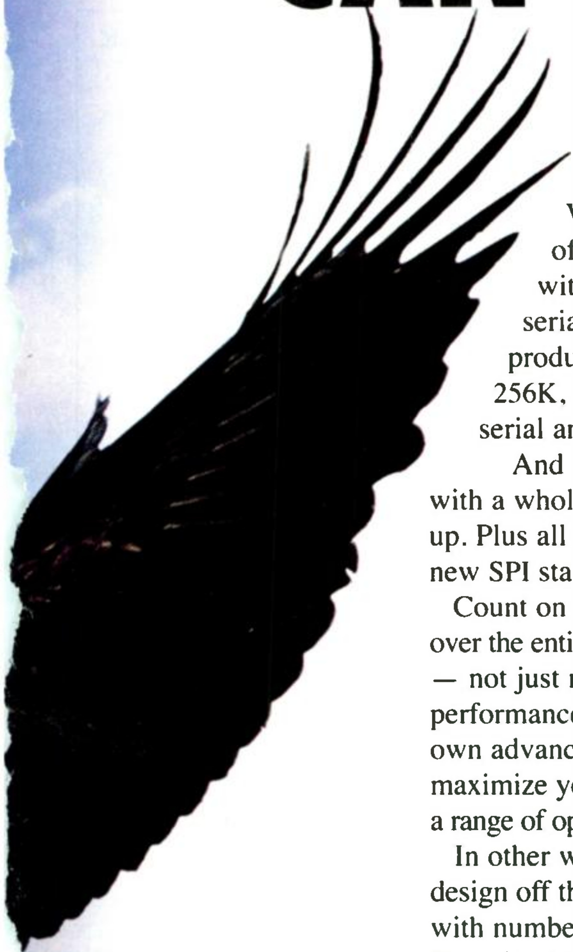

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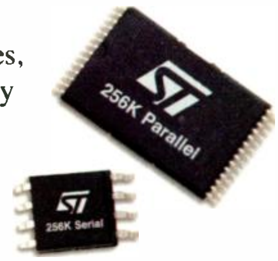

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I^2C		ST24C01 ST24W01 M2201* ST24LC21*	ST24C02 ST24W02 M34C02*	ST24C04 ST24W04	ST24C08 ST24W08	ST24C16 ST24W16 ST24164*				
EXTENDED I^2C						ST24E16	*NEW!* M24C32	*NEW!* M24C64	*Q496* M24128	*NEW!* M24256
SPI		ST95010 ST95011	ST95020 ST95021	ST95040 ST95041	ST95P08	*1H97* M95160 M95161	*1H97* M95320 M95321	*Q197* M95640 M95641	*1H97* M95280 M95281	*Q197* M95560 M95561
PARALLEL						M28C16 M28C17		M28C64C M28C64		*NEW!* M28256

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  - 100 μA STANDBY
- FAST 3 mS WRITE CYCLE TIME
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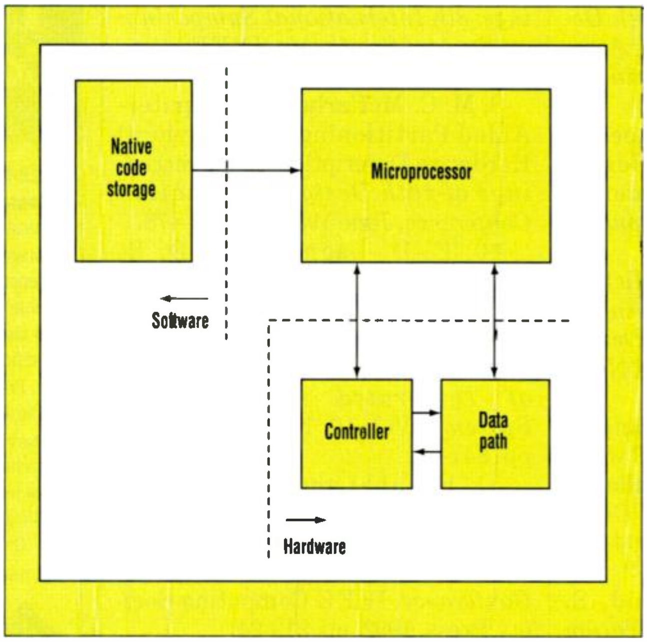
tioning might be possible.

Application-Specific Instruction Set Processors: One example of hardware-software codesign is the design of an application-specific instruction set processor *(Fig. 4)*. The hardware-software boundary in this case lies between the software running on the processor and the processor itself. Therefore, we think of this as a Type I system.

Hardware-software codesign for an application-specific instruction set processor attempts to find the best hardware implementation for a given software application or set of applications. This generally involves coming to an understanding of how the structure of the hardware implementation impacts the performance of the software.



5. This example shows a microprocessor with a custom coprocessor. The hardware-software trade-off in the design of custom coprocessors is between implementing some function using the instruction set processor or implementing it using the custom coprocessor.

In some cases, the design of an application-specific instruction set processor affords the opportunity to move the boundary between hardware and software by adding new instructions to the instruction set architecture. In these instances, hardware-software codesign for an instruction set processor may include hardware-software partitioning. Managerial considerations, such as modifiability, are likely to be important factors in determining the best hardware-software partition in such cases.

Note that the diagram shown in Figure 4 also would apply to the design of a general-purpose instruction set processor. But in that case, the application software is usually not part of the design methodology and is not known ahead of time. For this reason, we generally do not consider general-purpose processors to be examples of mixed hardware-software systems.

Application-Specific Coprocessors: In some cases, the performance of an instruction set processor can be enhanced by adding one or more custom coprocessors. The purpose of the custom coprocessor is to off-load some of the more computationally intensive tasks from the main instruction set processor, which may be either a general-purpose or special-purpose (e.g. DSP) processor.

The software component of such a system is the code that is to run on the instruction set processor, while the hardware component is the custom coprocessor *(Fig. 5)*. This is a Type II system because the hardware component includes its own data path and controller, and can be specified and modeled behaviorally at roughly the same level of abstraction as the software.

The hardware-software trade-off in the design of custom coprocessors is between implementing some function using the instruction set processor or implementing it using the custom coprocessor. Because the design methodology allows a choice between hardware and software, we consider this to be an example of both hardware-software co-synthesis and hardware-software partitioning. The nature of the computation is likely to be an important factor in determining the best hardware-software partition for a custom coprocessor system.

Because hardware-software codesign can mean many things, it's useful to have some criteria for characterizing codesign. We have suggested the following:

The type of hardware-software system being designed (Type I or II).
The system design tasks being addressed (simulation, synthesis).
If simulation is addressed, the level of abstraction at which the hardware-software interaction is modeled (pin activity, communicating processes).
If synthesis is addressed, whether hardware-software partitioning is performed.
If hardware-software partitioning is performed, the factors that influence the partitioning (nature of computation, implementation constraints, managerial considerations).

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Don Thomas is Professior of Electrical and Computer Engineering at Carnegie-Mellon University, Pittsburgh, Pa. He holds a PhD. in Electrical and Computer Engineering from Carnegie-Mellon.

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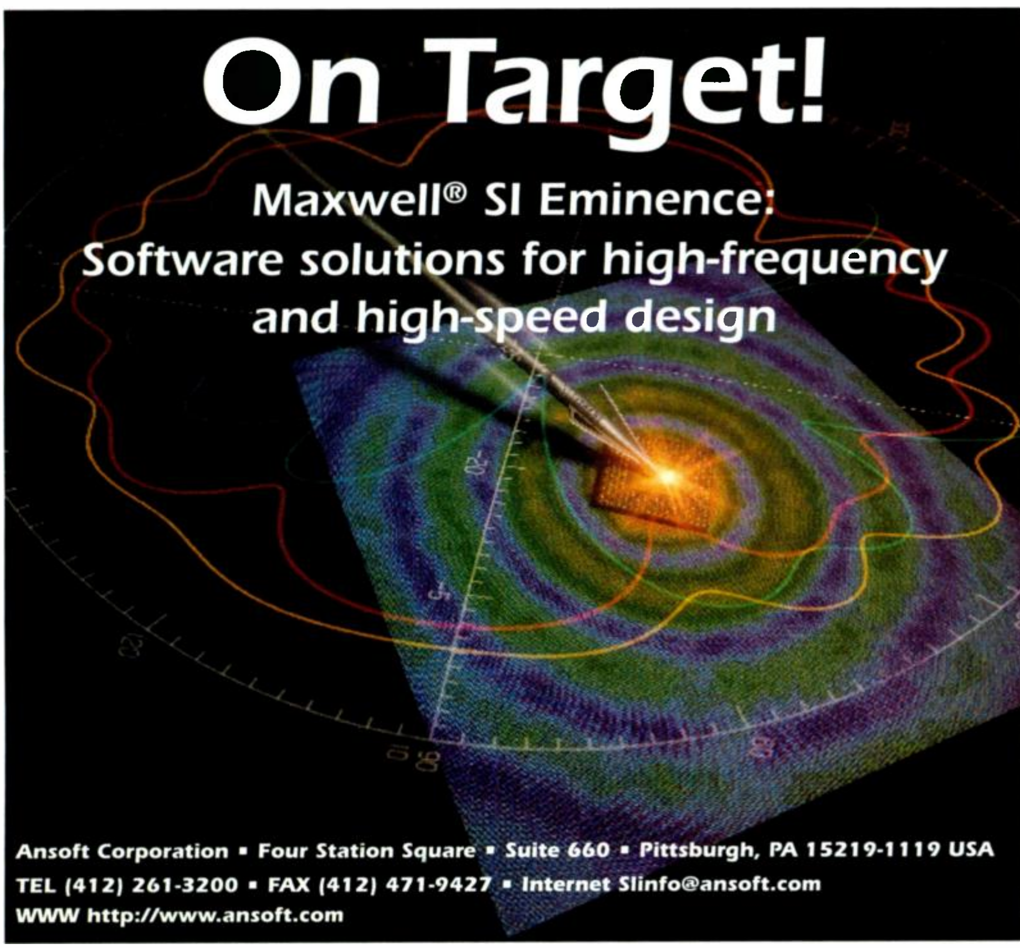
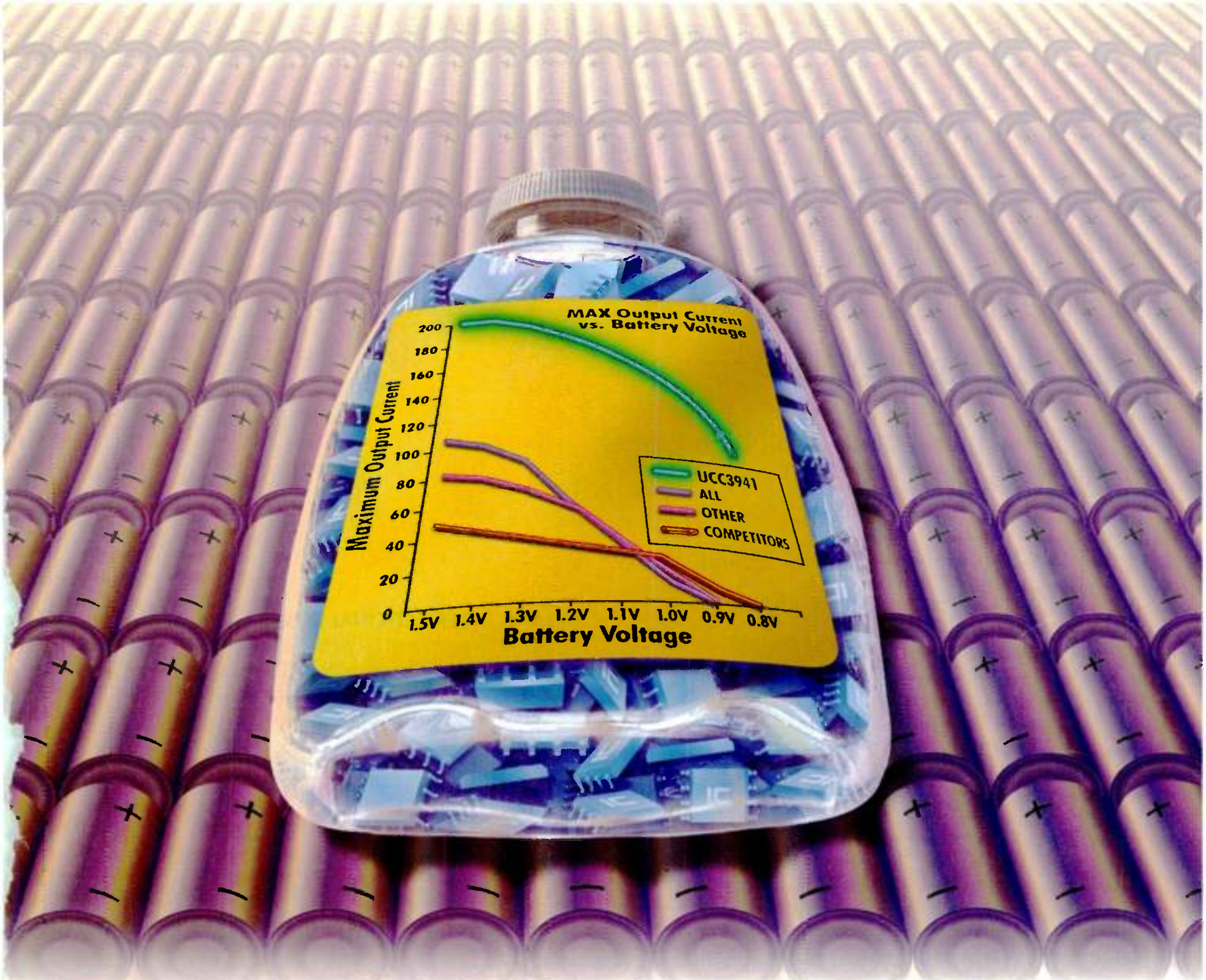
HOW VALUABLE	CIRCLE
HIGHLY	561
MODERATELY	562
SLIGHTLY	563




MAX Output Current vs. Battery Voltage
Maximum Output Current
200
180
160
140
120
100
80
60
40
20
0
1.5V 1.4V 1.3V 1.2V 1.1V 1.0V 0.9V 0.8V
Battery Voltage
UCC3941
ALL
OTHER
COMPETITORS

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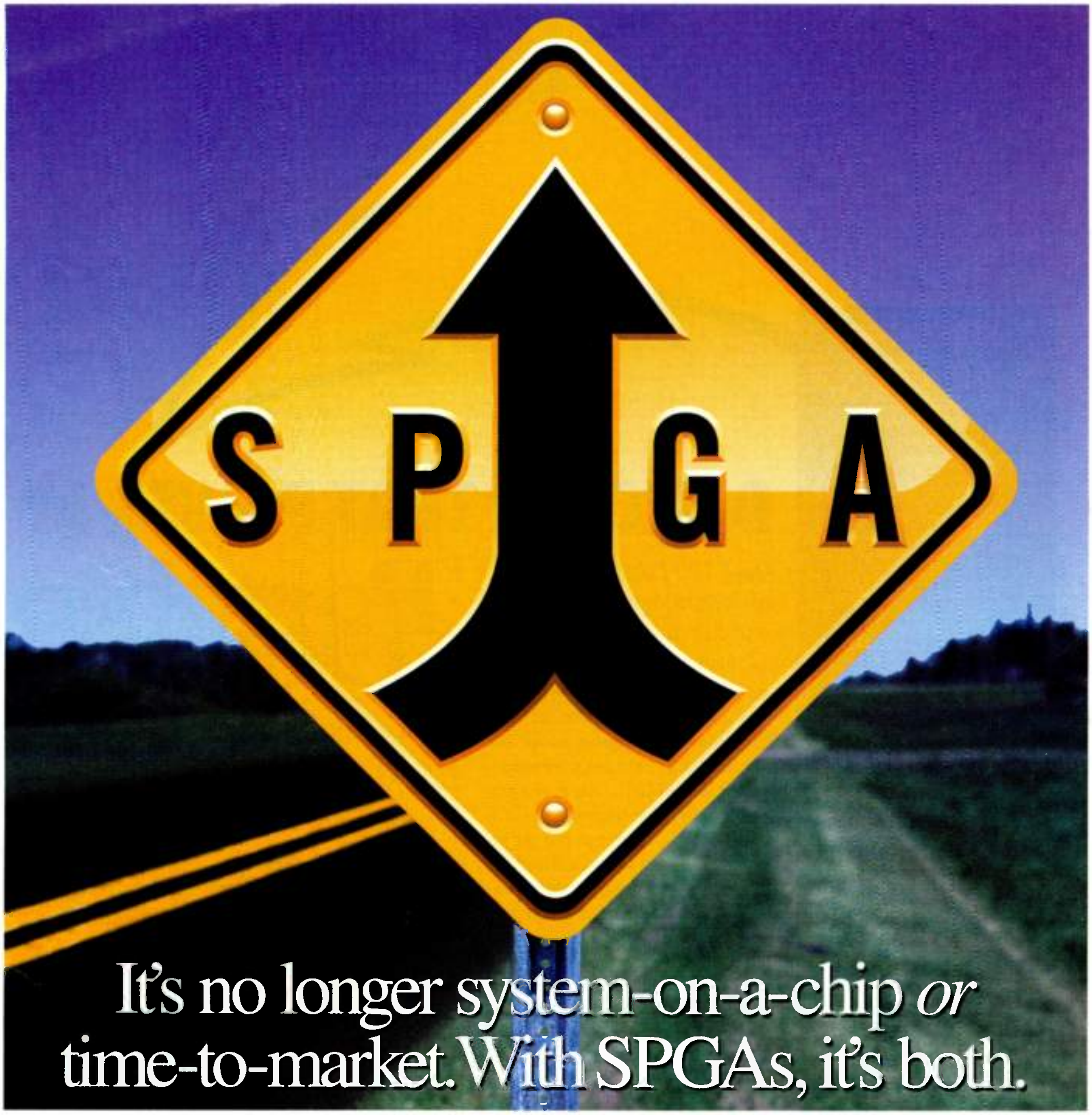

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Cell-Library Development Tool Eases Migration To Next-Generation ICs

Design-Rules Driven Methodology And Process-Technology Support Combine To Enable Rapid Library Migration.

Cheryl Ajluni

Today's cell-library developer faces many challenges, not the least of which is to provide accurate libraries to IC designers. One of the forces driving these challenges is that IC designers are being pushed to deliver products to market quicker which means that library developers have even less time than before to create new libraries. Increasing design complexity also poses a problem because it drives changes in the process technology required to handle higher level circuit functions, such as memories, datapaths, functional blocks, megacells, and cores. In turn, the changes in physical design tool technology and semiconductor process technology, including decreasing line widths, salicide processes, stacked vias, and area routers, drive the need for new libraries.

In the face of these intertwined trends, library developers are now competing for IC designers' business, based on how quickly and accurately they can provide libraries that reflect this dynamically changing environment. According to Don Carter, vice-president of Marketing for Cascade Design Automation, Bellevue, Wash., "Library developers compete based on breadth of library, available foundry process, time-to-delivery, accuracy and price. To satisfy the needs of IC designers today and deliver fair value, library developers must have the ability to resize, retarget and retune their libraries."

Recognizing these multiple need, Cascade Design Automation introduced a software tool known as MasterPort over a year ago. The tool was designed to close the gap between the introduction of new processes and library availability by allowing IC developers to automatically and accurately migrate existing cell libraries from one process technology to another.

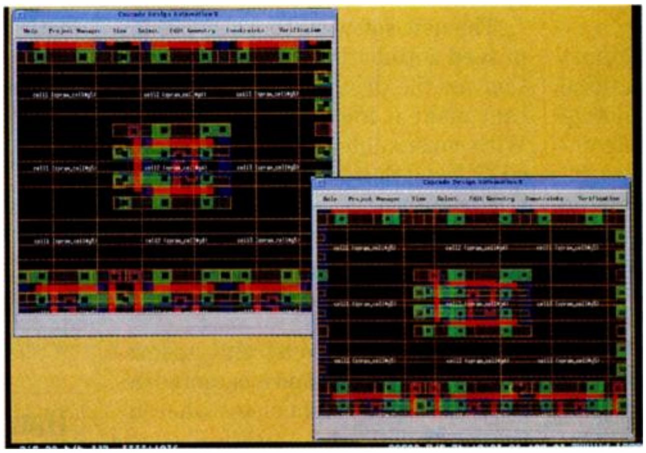
Now, with the introduction of a new version, MasterPort 2.0, library developers can produce libraries that not only take full advantage of each fabrication process with no inherent loss in density, but also apply to a wide variety of foundry processes *(Fig. 1)*.

Currently there are a number of techniques being used in library development tools, such as scaling, compaction, and linear shrink or least-common denominator to migrate libraries within a process generation. Unfortunately, these techniques are quite difficult to use when migrating libraries to a new process generation. In part, this is because they do not provide optimized layouts, while they require more iterations to reach a desired result and have limited device sizing. In addition, they give the user little or no control over the results, and, because they tend to treat layout as a piece of "artwork" rather than an IC, the layout often looks good but doesn't always perform correctly.

In contrast, MasterPort 2.0 is based on a module generator technology and is able to produce libraries that have been optimized for a specific process technology. It achieves this goal by storing existing GDSII data in soft process-portable format. Then, by simply entering the process parameters and design rules for the new process, the original design can be retargeted to the new process. Incremental process improvements can also be incorporated into the cell library with little effort.

MasterPort 2.0 is well-suited for use by semiconductor and ASIC vendors because it not only enables a company's cell-design expertise to be extended across several generations of libraries and process technologies, but also because it allows the library developer to take circuit technology and migrate it to a specific performance level. In addition, the software tool is equipped to tune libraries, by taking in very general information and tuning it for a specific application. This feature places MasterPort 2.0 in a strategic position to deal with the issues of Intellectual Property (IP) and design reuse being necessitated by the growing complexity of designs. As an added benefit, library developers are able to use the MasterPort 2.0 software tool to conduct explorations on standard cells. It does this by allowing process groups to make changes to see how they will affect the final outcome of the library.

The MasterPort 2.0 software

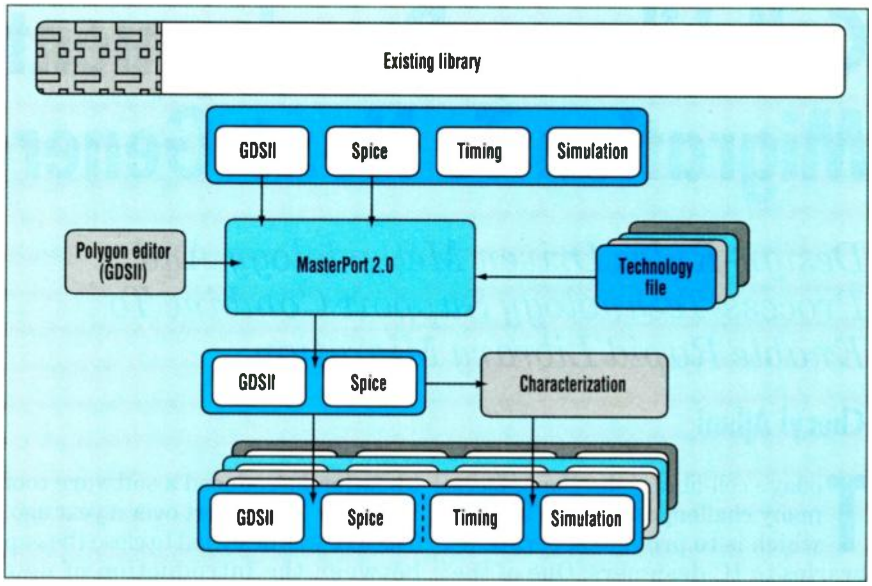


1. MasterPort 2.0, a cell library tool, allows retargeting and reuse of high-level functions through hierarchical pitch-matching, hierarchy preservation, and increased design size support capabilities.

tool works in existing library development flows *(Fig. 2)*. Users can input GDSII and Spice data for an existing leaf-cell library, and the tool then outputs GDSII and annotated Spice data for the cell library in a different process. By taking the leaf-cell description abstraction up a level and applying it to a second set of variables, it can be easily reconstructed to fit the new design rules. The new library can then be verified and characterized using an existing library.

A better hierarchy

One of the unusual new features provided by the MasterPort software tool is its hierarchy option, which enables process-accurate migration for the retargeting and reuse of higher-level functions from one process to another. Today, many complex functions are implemented in a hierarchical manner, whereby a grouping of cells is connected in a specific order.



2. The MasterPort 2.0 software tool fits into existing design flows and works by taking in a physical description of the leaf-cell data and technology files, provided by either the customer or the company, and then basically "filling in all of the blanks" required to migrate a library to new

With some of the other cell library technologies on the market, this hierarchy would tend to be pushed down and flattened. With Masterport 2.0 however,, the hierarchy is retargeted through an approach that migrates the individual parts but maintains an understanding of the "big picture;" in other words, the preservation of the hierarchy. Consequently, major hierarchical elements, such as memories, cores, and datapaths, as opposed to just standard cells, can be accommodated by the tool to produce process-optimized libraries. Additional features included in the hierarchy software tool option are hierarchical pitch-matching and support for increased design size.

Masterport 2.0 also can support new process technologies such as local metal and salicide processes. This capability is important because it significantly increases the tool's power to migrate library elements from drastically different processes. Support for a second routing grid has also been added to the MasterPort base tool, to help reduce manufacturing costs for masks.

With library developers having less time to develop new libraries, increased library development automation has been seen as a means of reducing development time and cost. Toward that end, MasterPort 2.0 now offers automatic jog insertion and automatic pitch-matching capabilities. Automatic jog insertion, based on the hierarchy in a design, enables the user to control the extent of the insertion usage with respect to critical paths, user-selected paths, and gates.

A jog is typically inserted into the metal to bring about a decrease in cell size density. The automatic pitch-matching, or cell-height calculation feature, determines and applies the minimum cell height for an entire cell library. With these new automation capabilities, library developers are able to achieve their results faster and consequently for a much lower development cost.

The new software tool also has improved automatic-constraint generation and file-driven global constraints that make it ideal for design reuse. With constraint-generation, existing GDSII and Spice descriptions of a cell are input into the MasterPort 2.0 tool. In turn, the software automatically generates constraints that define the spatial relationship between elements in the design.

The automatic constraint-generation process is based on a patented design-rule-driven technology, whereby the constraints are automatically evaluated based on the new design rules of a target ruleset. This results in a new layout that can be optimized for the new process based on application requirements. Initial porting of a basic standard cell takes less than 90 seconds, while subsequent cell porting takes less than 30 seconds.

MasterPort 2.0's configuration control capability helps to provide users with a more accurate design environment that further reduces IC library development costs. This is made possible because use of the tool reduces library maintenance,costs and also because it takes fewer people to maintain the libraries than in the past. Features included as part of the configuration control capability include version control, user control number of backups, and user control over automatic compression files.

Price And Availability

The MasterPort version 2.0 software tool is now available and runs on both the Hewlett-Packard and Sun Microsystems workstations. As a standalone product, the tool is priced at $180,000. With the optional hierarchy migration capability included, MasterPort 2.0 sells for $250,000.

Cascade Design Automation, 3650 131st Ave. SE, #650, Bellevue, WA 98006; (206) 643-0200; e-mail: info@ole.cdac.com; Internet: http://www.cdac.com. **CIRCLE 490**

How Valuable	Circle
Highly	528
Moderately	529
Slightly	530

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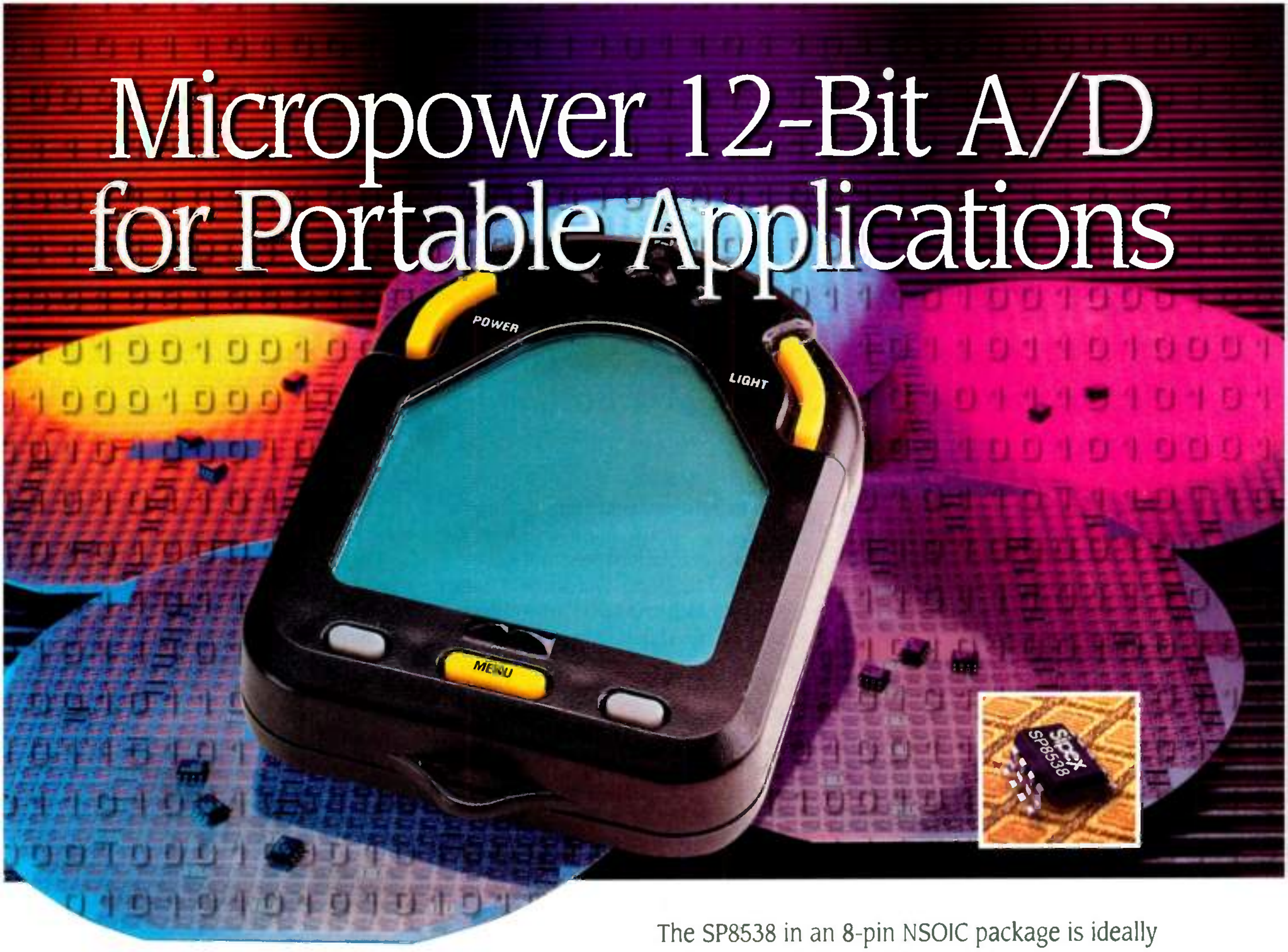

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Benefits	Sipex	Linear Tech	Condition
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73dB Signal to Noise Ratio at a mere 1.25mW. Plus, the simple 3-wire SPI serial interface works easily with a wide range of microprocessors and micro-controllers. Noisy environments? The SP8538 with its "True" differential inputs and a Common Mode Noise Rejection (CMR) of 110dB @ 60Hz is the solution to your problem.

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Advanced Emulation Tool Targets High-Speed Functional Verification

Advanced Processor And Innovative System Architecture Enable High-Capacity Verification.

Cheryl Ajluni

In the midst of enormous project risks and increasing time-to-market pressures, designers also are facing a major challenge in verifying more complex system designs. Today's deep-submicron processes are creating more gates on one chip than can be comprehensively verified with simulation alone. In fact, designers spend just about as much (and sometimes more) time verifying than they do actually design. Complicating functional verification is the growth of different types of designs such as asynchronous or synchronous, clock-less logic or single clock, for different applications—CPU design, graphics, communications—which call for different types of verification tools. While it will indeed be met by a combination of tools, it's clear to many in industry that the challenge of functional verification will best be served by emulation techniques.

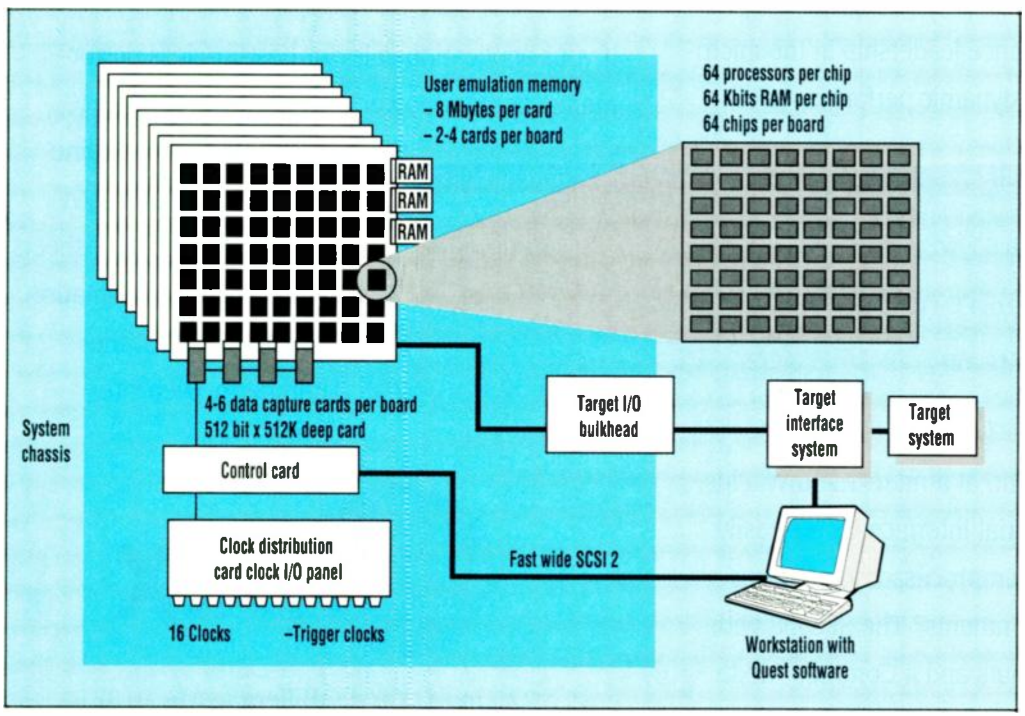
Toward that end, Quickturn Design Systems has introduced an emulation system, CoBALT (Concurrent Broadcast Array Logic Technology). CoBALT offers a combination of strong verification performance, with compilations of 1 million logic gates per hour on a single workstation, and large capacity, with up to 8 million logic gates. By comparison, other emulation systems available offer performance in the range of 50,000 to 100,000 gates per hour, and capacity up to 3 million gates.

The CoBALT emulation system, with 4096 processors per emulation board, is optimized for use with synchronous or mostly synchronous designs, including gated, multiple, and single clocks, that lend themselves to cycle-based verification. Based on an array of concurrent custom processors, it employs compiled-code, versus the more common method of using FPGAs to map wires to wires, effectively shortening the time-to-emulation.

The heart of the emulation system is a modular architecture, jointly developed with (and purchased under an OEM agreement from) IBM. The architecture is based on a custom 0.25-µm CMOS IC with an array of 64 interconnected processors and a 100-MHz internal-step clock *(see the figure)*. By comparison, most hardware accelerators have only one processor.

Each 60-layer emulation board contains 4096 processing units per card scalable from 500,000 logic gates to an 8 million logic-gate capacity, with up to 64 Mbytes of RAM and 128 Mbytes of vector memory. Also, the system has up to 32-million bits of register file, or wide memory, and 16 k by 512 k internal probes. The modular architecture improves runtime performance and design capacity. And, implementation of a partitioning capability enables the system to perform in-circuit emulation and accelerated co-simulation in dedicated or server modes. This allows users to rapidly prototype multimillion-gate ICs, or full systems comprised of multiple ICs.

The emulation tool evaluates one level of logic in each step of the engine's internal clock. The compiler transforms combinatorial logic between registers into Boolean logic. Users can trade off capacity with emulation speed. Emulation performance is set by internal clock speed and



The modular architecture utilized by Quickturn's CoBALT system emulator provides eight clock domains per board to allow users to emulate multiple designs independently and simultaneously.

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the number of system processors.

Buses, commonly used for interprocessor communicationof emulation tools, often cause a communications bottleneck. The CoBALT compiler, on the other hand, uses a broadcast-interconnect approach with significant advantages over other approaches such as time-multiplexed bus interconnections. This is done by improving bandwidth and by very fast emulation speed. All interprocessor communication is by direct connection. Subsequently, each processor is able to broadcast to all other processors.

CoBALT is a true multi-user system. As a simulation server, it emulates eight independent designs simultaneously. It acts as a shared network through which each of eight domains may be independently accessed by different designers. Individual macros or multiple chips can be verified simultaneously and interactively, using vector-based verification.

The family is supported by the company's Quest II emulation software, which provides the user with an easy to use graphical interface, QEL scripting language for automating emulation flows, and a comprehensive set of ASIC libraries. Additional features include timing-correct logic and memory compilation, automatic design mapping, fast incremental compilation of design changes, Verilog/VHDL RTL emulation, thousands of logic analyzer probes with complex triggering, and a functional accelerator mode with 100% visibility. CoBALT is supported by Quickturn's HDL-ICE software, and the new Q/Bridge co-simulation integration software. It offers support at the RTL and gate level for VHDL and Verilog high-level design languages.

PRICE AND AVAILABILITY

Now available, the CoBALT emulation family has a starting list price, for an entry-level 500,000 gate configuration, of $495,000.

Quickturn Design Systems, 440 Clyde Ave., Mountain View, CA 94043; (415) 967-3300, e-mail: info@quickturn.com, Internet: www.quickturn.com. **CIRCLE 491**

HOW VALUABLE	CIRCLE
HIGHLY	537
MODERATELY	538
SLIGHTLY	539

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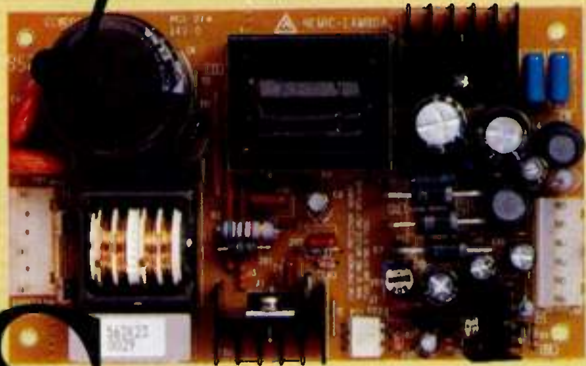

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READER SERVICE 177

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READER SERVICE 129

A Look At High-Speed DAC Performance For Communications

New Criteria Demand A Different Look For The Digital Radios That Are Becoming Real Every Day.

Paul McGoldrick

SPECIAL REPORT

The continued proliferation of wireless communications products has led to the development (and potential development) of numerous digital radio designs that look somewhat familiar to those who have worked in defense projects. An essential difference is that these new designs are now possible at low consumer costs. The designs demand digital-to-analog converters (DACs) that can be operated at high speed with high performance. Next-generation designs will be pushing the envelope even more with demands for yet lower power consumption with a single-supply voltage and, of course, lower cost.

Many of these DACs are to be used in analog reconstruction applications in the transmit paths of radios. They reconstruct complex analog waveforms from the digital modulation systems that are now driving the radios. Generally, the DACs will provide differential current outputs that are needed for the high bandwidths and refresh rates involved. The output frequency of the devices will generally be at the IF that is usually located between 50 and 100 MHz.

Art Courtesy: Signal Processing Technologies

As devices improve, there will be more cause for moving the IFs higher. The DAC is the critical component of the system with the next being the RF output device being used after up-conversion.

There is no one specification that is critical to implementation, but there are great differences in the areas where overall bandwidth is of concern *(see "Effective Use Of Specifications," p. 90)*. The analog reconstruction of a single channel is quite different from the effective conversion of a complete group of channels. The difference, for example, in a component's use in a single-channel radio and a multichannel cellular transmitter site, where dynamic-range characteristics might be more important in the former, and the production of unwanted spurious signals in the latter.

Generally regarded as an important measurement is the spurious-free dynamic range (SFDR). Understanding the generation of these spurious signals is straightforward. In their application note, number AN619, Harris Semiconductor gives an example of a pure 2.03-MHz tone as fundamental with a 10-MHz sampling rate creating alias terms at 7.97 MHz (10 – 2.03) and 12.03 MHz (10 + 2.03) *(see the figure)*. The aliases continue up through the spectrum around the harmonics of the sampling frequency. The highest-amplitude spur, either harmonically or non-harmonically, will define the dynamic range of the system and it is used to define the SFDR.

Harris offers the application note because it is increasingly true that the ability of the circuit designer to measure SFDR performance is severely limited by the quality of the laboratory setups that generally exist outside of the semiconductor manufacturers' premises. Some hard, practical advice is given in what to look for in adjusting and calibrating spectrum analyzers and the external conditions and considerations that must be taken into account to achieve accurate measurements. Harris also has pioneered, at the behest of Motorola, Power Amplifier Solutions

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[1] Free evaluation kits available with the single unit purchase of the following models: PA04, PA05, PA26, PA42, PA87, PB50/PB58, SA01, SA02, SA50, SA51. Limit 3 free kits per customer.

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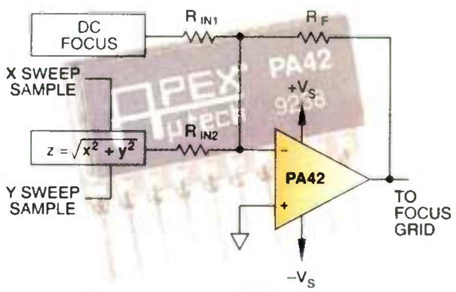
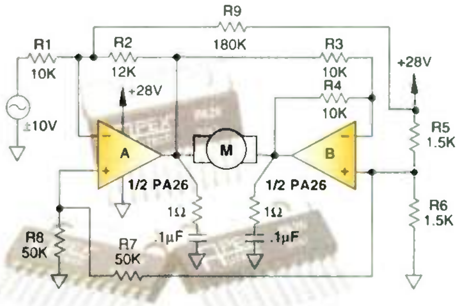
PA26 FREE EVAL KIT!

Two 2.5A Rated Amplifiers on One Die, in One Package, Priced $3.45*, Are the Many Reasons this Power Amplifier is a Popular Fit for Half, Full Bridge Motor Drivers

The PA26 saves valuable real estate by putting two 2.5A rated power amplifiers on a single die, in a single 12-pin SIP package. The PA26 provides the fit for bridge mode configurations or applications designed with multiple amplifiers per board The PA26 is also extremely affordable priced at *$3.45 in 10K pieces.



Dynamic Focus, CRT Display

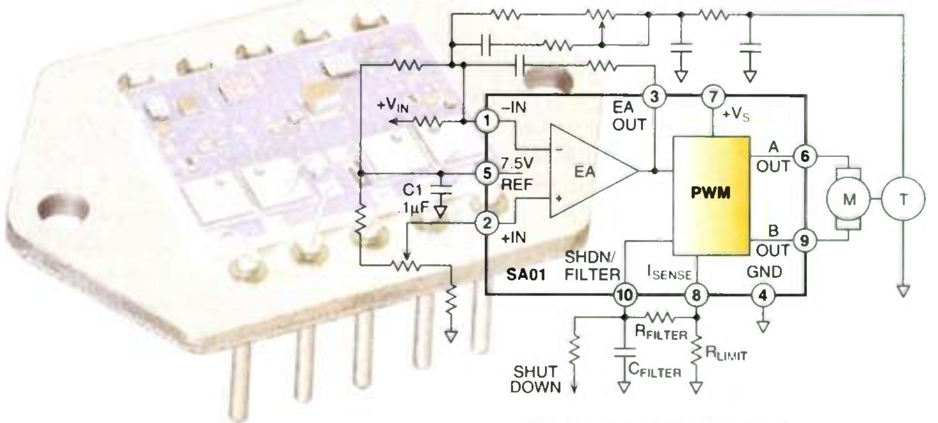


Bidirectional Small Motor Drive

SA01 FREE EVAL KIT!

This Industry First Hybrid PWM Amplifier Switches Its Way To 97% Efficiency And 2000W of Power in Brush Type Motor Control, Reactive Load Applications

Also known as a switching or Class D amplifier, the SA01 is an industry first hybrid PWM (Pulse Width Modulated) amplifier. High efficiency is the beauty of PWM technology, and with a 97% efficiency rating, operational on single supplies up to 100V and capable of 20A continuous, the SA01 can deliver up to 2000W to the load while reducing the need for bulky, space consuming heatsinks. The SA01 is also loaded with thermal protection features inside its hermetic power-dip package measuring just 2in².



Motor Drive With Tach Feedback

Effective Use Of Specifications

Technology has pushed the available performance of high-speed DACs into the Gsample/s range with output frequencies approaching 500 MHz. This has allowed the design of high-performance direct digital synthesis (DDS) systems to replace voltage-controlled oscillators (VCOs) and PLLs in such applications as fast-hop spread-spectrum communications, Doppler chirp radars, electronic counter measures, and for the direct generation of an assortment of digital modulation schemes such as FSK, CPFM, PSK, BPSK, QPSK, MPSK, and QAM.

In specifying high-speed DACs, the target application dictates which parameters are important. For instrumentation, high-resolution video, graphics displays, and arbitrary waveform generators, the sample rate, rise/fall time, settling time, linearity, glitch impulse, and clock/data feed-through are the important parameters. Measurement of these parameters is straightforward.

DDS systems rely on spurious-free dynamic range (SFDR) as the primary parameter. DDS performance has always been difficult to predict when using the specifications from data sheets since many DAC manufacturers supply data with output rates that are much lower than the maximum-rated Nyquist frequency. SFDR, when measured at 1- to 10-MHz sine-wave patterns, using clock rates up to 200 MHz, can achieve results as low as -72 dBc for a 12-bit DAC. When designers try to use sine patterns as high as $f_s/3$, they find that the performance degrades rapidly and is unusable for many applications. The ac test methodology used in generating the specifications can understate SFDR, or worse, may overstate the actual attainable performance.

Pattern-induced errors, such as insufficient pattern length, can result in the generation of spurs due to truncation errors, but are more likely to overstate a DAC's performance by exercising only a portion of the its circuitry. A 128K pattern generator filled with a repeating 512-word pattern will not exercise every bit, and may actually mask defects in the device under test and result in an overly optimistic SFDR. Careful selection of the clock-to-output frequency ratio should ensure a non-repeating pattern and use maximum pattern depth.

In DDS applications, $f_s/3+\Delta$ has been used as a standard measurement of DAC performance. The reason is that $f_s/3$ more closely approximates the maximum sine frequencies a device will be expected to deliver in actual use. Pushing the data to the Nyquist frequency provides a challenging problem when designing filters with good phase control and adequate margin. Adding a small amount of delta to $f_s/3$ pushes its second harmonic and clock frequency mixing products back into the Nyquist band with an offset from $f_s/3$ making it measurable.

Almost all DACs are trimmed at dc to less than 1/2 LSB DNL (dynamic nonlinearity) and INL (integral nonlinearity); when used in DDS applications, the ac INL is virtually impossible to measure. Factors that change INL at ac include: Glitch impulses at all transitions, clock feedthrough, data feedthrough, asymmetric rise and fall times, pattern dependencies, switch nonlinearities, and forward and reverse termination mismatches. By using the $f_s/3+\Delta$, the data precesses through all codes at the maximum clock rate, producing a worst-case SFDR. This is unlike an even multiple of the clock ($f_s/4$, for example) which produces one singular bit pattern whose SFDR can be very optimistic, depending on the phase of the data pattern.

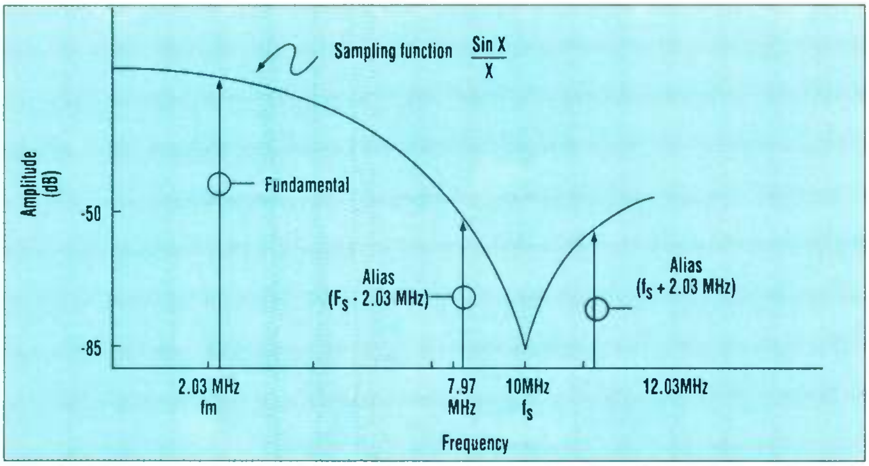
Another worst-case pattern used to specify ac performance is a $f_s/2+\Delta$ which exercises the analog and digital paths at maximum frequency. The fs/2 pattern causes the output to alternately switch between full scale and zero, bringing out ac errors such as those caused by slew-rate limiting. It also exercises the digital path with a worst-case one/zero pattern. (Skew variations in the digital path may be discovered with this pattern.) The Δ term is important here since it causes the pattern to search through all possible codes, thereby exercising all the data bits and current sources. In the frequency domain, the aliased harmonic spurs are separated from the aliased clock and data components that allow them to be independently measured.

A further measure of ac performance for DDS applications is to increase the clock rate while keeping the data rate the same. Differences in the slope of the SFDR and data and clock rates for various DACs can be very significant. When compared to a system using a 100-Msample/s 14-bit DAC operating at its maximum clock rate and generating a 33-MHz signal ($f_s/3$), spurious performance in a system can sometimes be improved 6 to 8 dB by instead using a 1-Gsample/s, 14-bit DAC clocked at a modest 500 to 600 Msamples/s using the same signal rate.

Aside from nonlinearities in the transfer function, which directly translate to an increase in the noise floor, the overall shape of the deviation from the linear case may produce harmonically-related spurs in the frequency domain. An S-shaped deviation may produce harmonics that are significantly different than those produced from a bow-shaped transfer curve. In addition, the inability of the DAC output to follow the digital inputs at GHz clock speeds may account for most of the full-speed performance degradation, along with those degradations produced by mixer products, clock/data feedthrough, and digital-timing skew variations.

When looking at data sheet specs, your end application will determine which specifications are most important to consider. Specifications which have been taken under best-case conditions may lead to selecting a DAC that does not meet performance in the end application. By considering data taken at worst-case conditions and seemingly overdesigning the system using higher clock rates, an overall improvement in analog performance can be achieved.

Contributed by Tyler Bowman, Design Engineer, SONET Development, and George Pell, Test Development Engineer, Fibre Channel Development, both of TriQuint Semiconductor Corp.



A 2.03-MHz tone sampled at 10 MHz produces alias terms at 7.97 and 12.03 MHz, and at 2.03 MHz on either side of all the harmonics of the sampling frequency.

the use of multitone power ratio (MTPR) testing.

The MTPR technique was introduced for ADSL (asymmetric digital subscriber line) testing where there are a number of "dead" zones where intermodulation products can be measured—and it is an extension of classic intermodulation distortion testing — but for converter testing, the missing tones are reduced to just one "dead" space in the middle of a band with possibly 20 test tones at equal frequency spacing. The worst-case spur in the missing band is created by a third-order harmonic product of the fundamentals (any 2fx–fy product) and the ratio of peak power to peak distortion

How Ideal Is An Ideal DAC?

At the heart of every digital communication system's transmitter exists a high-speed DAC whose task is to faithfully transform a sequence of digital words into its equivalent analog representation. The process establishes fundamental, yet predictable, limitations on how accurately even an ideal DAC can reconstruct an analog waveform. It is based on two fundamental concepts, sampling and quantization, that set the theoretical bandwidth and dynamic range of the DAC.

The Nyquist theorem states that an analog signal can be perfectly reconstructed, without any loss in information, if the sampling rate, f_s, is at least twice the bandwidth of the analog signal. The assumptions are that the original analog signal is band-limited and is sampled perfectly, not contributing any additive distortion and noise. Conversely, it is assumed that re-sampling is perfect in reconstructing the original sampled signal and is also band limited to $f_s/2$.

The time- and frequency-domain effects of a sampled signal can be modeled using a mixer as the "sampler" *(see the figure)*. In the case of a DAC model, a zero-order hold filter is inserted after the mixer to model its reconstructed output response. Although not shown, an analog reconstruction filter whose function is to smooth out the step response and return the sampled signal to its original form typically follows the zero-order hold filter. The time- and frequency-domain representations of the sampled and reconstructed signal are shown at different stages within the model. A band-limited signal, in this case a sine wave, is applied to one input of the mixer while the sampling clock, a zero-width impulse train, is applied to the mixer's local-oscillator input. In the time domain, the sampled output of the mixer appears as a series of zero-width impulses modulated by the original analog signal. Note that the sampled output signal is only represented at discrete instances in time and at all other times, assumes a value of zero.

In the frequency domain, the spectral output of the mixer will contain the original fundamental signal as well as introducing images of this signal around every multiple of the sampling clock frequency, f_s ,extending to infinity. These images are a form of distortion (although not harmonic) since they were not part of the original unsampled signal. The amplitude of these images is equal to that of the fundamental signal that appears in the baseband region between dc and $f_s/2$. During the reconstruction process, the sampled output signal is applied to the zero-order hold filter which serves to hold the sampled output signal between samples. In the time domain, the output appears as a series of modulated rectangular pulses whose width is equal to the reciprocal of the sample rate (i.e., update rate). However, the frequency spectrum of the previously described sampled output is now modified with the ubiquitous (sin x)/x roll-off response in which zeros or nulls appear at multiples of f_s.

In the case of a perfect DAC, this (sin x)/x response acts as a filter that slightly modifies the amplitude of the fundamental reconstructed signal. In some digital communication systems, this amplitude shaping must be compensated for with a [(sin x)/x] – 1 correction filter. Reconstruction of the sampled signal typically requires that the images be eliminated either to enhance the dynamic range of a reconstructed analog signal and/or limit the spectral bandwidth of a digitally generated communication signal. In the time domain, the analog reconstruction filter serves to smooth out the DAC step response. The first image is the most difficult to suppress in baseband applications since it always appears closest to the fundamental signal. In practice, due to the complexity of implementing an analog reconstruction filter, the frequency range is limited to typically 1/3 or less of a DAC's update rate. Note that it is possible to make use of another image (undersampling) and filter the remaining images and fundamental with a bandpass filter.

Quantization is the result of using a finite digital word length to represent an analog signal which, by definition,

(continued on page 94)

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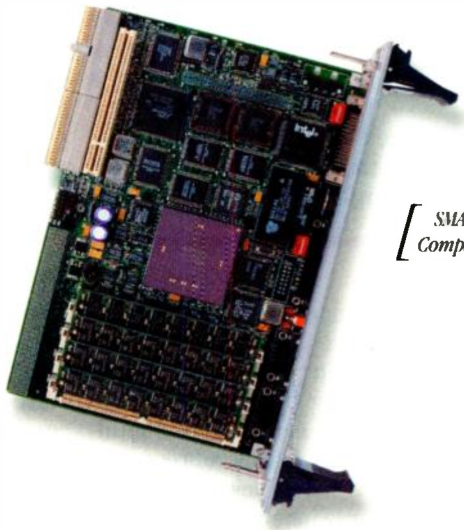

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is the MTPR.

Harris has found from customer feedback that the tested SFDR in practical circuits is closely matching the Nyquist numbers on most (but, annoyingly, still not all manufacturers') data sheets, while there is a magic number of 70 dBc being looked for in MTPR. This is attainable by Harris in their products for clock frequencies up to 30 MHz. The 70 dBc closely matches the limitations of the power devices available in the cellular base station applications a number of manufacturers are targeting.

The differences are reinforced by Maxim's David Bernel who notes that, "The requirements placed on high-

Companies mentioned in this report:

Analog Devices Inc., 804 Woburn St., Wilmington, MA 01887; (617) 937-1428, fax (617) 821-4273.

Harris Semiconductor, P.O. Box 883, Melbourne, FL 32901; 1-800-4-HARRIS; fax (407) 724-7240; Answerfax (407) 724-7800. Application note AN9619 ("Optimizing Setup Conditions for High Accuracy Measurements of the HI5741") is document 99619; AN9629 ("Multitone Performance of the HI5741") is document 99629.

Maxim Integrated Products Inc., 14320 SW Jenkins Rd., Beaverton, OR 97005; (503) 641-3737, fax (503) 644-9929; literature line (800) 998-8800.

Signal Processing Technologies Inc., 4755 Forge Rd., Colorado Springs, CO 80907; (719) 528-2300; fax (719) 528-2370.

TriQuint Semiconductor Corp., 3625A S.W. Murray Blvd., Beaverton, OR 97005; (503) 644-3535; fax (503) 644-3198.

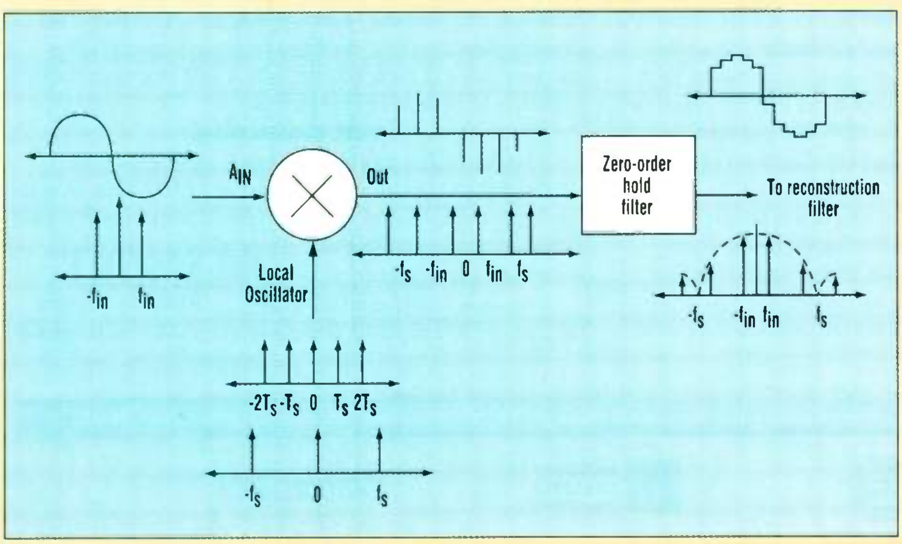
(continued from page 92)

can assume a continuous, infinite range of values. Since the effects of quantizing an analog signal are digital in nature, its effects in both the time and frequency domain are easily predicted. By representing an analog signal with a finite number of bits (N), an error exits between it and its digital representation. Each additional bit of digital representation (resolution) reduces this quantized error, or noise, by a factor of two. This quantization noise inherently limits the maximum theoretical carrier-to-noise (CNR) ratio of any digitized waveform. In the case of a digitized full scale sine wave, the maximum dynamic range attainable within a Nyquist band can be expressed as:

$$CNR = 6.02\,N + 1.76\ dB$$

Note that after the reconstruction of the digitized sine wave via an ideal DAC, this equation must be modified slightly to reflect the DAC's (sin x)/x frequency response which rolls off the quantization noise as well as the fundamental.

The assumption is often made that this quantization noise appears as white noise, spread evenly from dc to $f_s/2$. This assumption is not entirely valid since this noise is not actually random but correlated to the digital waveform. In some unique cases, this correlated quantization noise may be highly concentrated as harmonics, or spurs, related to the digital waveform. For example, if the frequency of a digitally-synthesized sine wave is set to certain exact multiples of the sampling rate, the quantization noise will be concentrated at multiples of the output frequency (harmonics.) If the output frequency is offset slightly from this exact multiple relationship, the quantization noise becomes less correlated, resulting in a lower spurious output. In most communications applications, the DAC is used to reconstruct some digitally-modulated sine wave(s) or other waveform that tends to reduce any correlation and subsequently suppress any spurs.As the number of modulated tones increases, additional testing and characterization is often required to qualify a DAC for a given multi-tone application. However, the majority of this testing and characterization tends to be highly application-specific with test conditions and multi-tone waveforms being determined by the system designer. Many systems designers prefer to perform their own bench characterization using vendor-supplied evaluation boards, but they should be aware that the test results are based on a single device and could possibly vary slightly among devices.



Contributed by Paul Hendriks, Application Engineer, High-Speed Converter Group, Analog Devices Inc.

As In:

Data speeds	>	1Gbps for channel links
Power consumption	<	10mA per channel (at 155Mbps)
Noise/EMI	<	TTL, RS-422, PECL, GTL, etc.
Cost	<	$3.50 per quad.

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Device	Bits	SFDR at Nyquist[1] (dBc)	SFDR at 2 MHz (dBc)	Window processing span (MHz) (f_s, f_{out})	Process	Glitch energy (pV-s)	Power dissipation (mW)	Supply voltage (V)	Price (in 1k quantities)
Analog Devices AD9760	10	59	84	100, 5	CMOS	5.0	190	+5	$12.54
AD9762	12	57	84	100, 5	CMOS	5.0	190	+5	$18.85
AD9764	14	NA	NA	NA	CMOS	5.0	190	+5	NA
Harris HI5721	10	51[2]	75	100, 2	biCMOS	1.5	700	±5	$25.00[5] (estimated)
HI5731	12	69[3]	79	100, 10	biCMOS	3.0	650	±5	$29.66
HI5741	14	71[4]	79	100, 10	biCMOS	1.0	650	±5	$49.90
Maxim MAX555	12	65	NA	NA	Bipolar	5.6	980	-5	$42.50
Signal Processing Tech. SPT9713	12	NA	68	50,10	Bipolar	15.0	640	±5	$29.00

Notes: NA = not available on data sheet or not relevant. 1 = for 100-msample/s clock (f_s) and 20-MHz f_{out} (single tone); 2 = f_{out} is 25 MHz; 3 = f_{out} is 2 MHz; 4 = f_{out} is 10 MHz; 5 = Harris quotes $38 each for 100-unit quantities.

speed, high-resolution DACs in RF applications are very different from the traditional time-domain applications. Specifications such as linearity, accuracy over temperature, and settling time are important in video or other instrumentation applications. But for RF signal synthesis, devices with excellent time-domain specifications cannot always deliver the dynamic range in terms of spurious performance (low SFDR) and the low total harmonic distortion (THD) necessary to achieve the high signal purity required, for example in multichannel, base-station architecture. To further complicate matters, some manufacturers specify these parameters differently, requiring designers to carefully scrutinize data sheets to compare converter performance."

Lee Walter of SPT (Signal Processing Technologies) expresses the feelings of some of his customers in choosing devices for the direct digital synthesis (DDS) market and for waveform synthesis generation: "The difficulty in looking at SFDR in DAC product data sheets is that SFDR varies greatly depending on a number of test conditions." Walter describes a DDS engineer's evaluation test setup. "He swept the frequency band of interest using the DAC being tested and accumulated a plot of all the 'spurs' in the band of interest. In this way he could see an aggregate picture of all the worst-case spurs for the various synthesizer frequency modes he intended to use the part in."

Walter goes on: "While SFDR is what most engineers want to look at, they ultimately have to try the device in their specific system or use one of the evaluation boards we provide for the part on identical conditions. From a DAC design point of view, SFDR can only be indirectly controlled, keeping non-linearity small, glitch energy low, and settling time fast."

This provides interesting observations on the high-speed arena and its specifications, and the ideals of a DAC *(see "How Ideal Is An Ideal DAC?" p. 92)*. It should be noted that the first offering from TriQuint Semiconductor, which is not in the comparison table, will be an 8-bit, 1-Gsample/s DAC, the TQ6122. Also, Analog Devices will always characterize several devices for a customer using the specific test conditions and waveforms in their applications *(see the table)*.

HOW VALUABLE	CIRCLE
HIGHLY	552
MODERATELY	553
SLIGHTLY	554

DESIGN APPLICATION

Putting Sensors To Work To Safeguard Computers

Various Digital And Linear Temperature And Motion Sensors Play Key Roles In Keeping PCs And Remote Internet Computers Out Of Harm's Way.

JERRY STEELE, National Semiconductor Corp., 6377 E. Tanque Verde Rd., Suite 101, Tucson, AZ 85715; (520) 751-2380

Sensor technology is increasingly important in personal computers in order to protect the equipment from high power levels that could lead to malfunctions and failure. Today's PCs are designed around a new generation of microprocessors that draw far more current than their predecessors, thereby dissipating greater power. This is driving up internal temperature levels to the point that sensing them is a critical element in PC reliability.

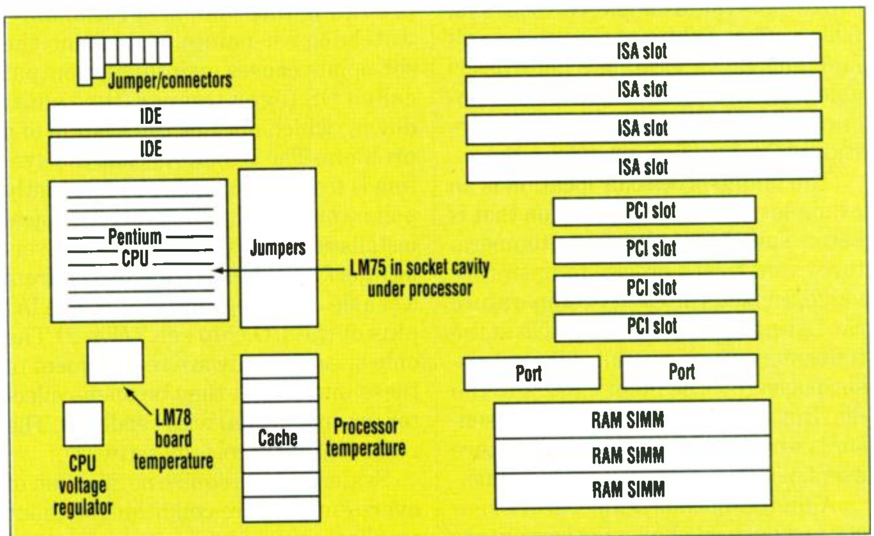
In addition, sensors may be even more important for hardware connected on networks like the Internet, since much of it is not in direct human view or control. Sensors, together with the proper hardware and software diagnostics, allow system administrators to monitor their system's health from a distance. This capability could spell the difference between a network that is shut down, and one where timely temperature information gives administrators a chance to reroute traffic to cooler running equipment.

Although power dissipation and overtemperature are the chief contributors to computer system failure, and thus must be sensed and controlled, sensor technology has a role to play in other areas of hardware protection. For example, sensor devices are being used to detect the opening of a computer case, to indicate levels of shock and vibration within the case or subsystem, and to monitor levels of humidity. Sensors can be used to detect an imminent fan failure by measuring fan rpms, allowing users to prevent a system malfunction from rising temperature within the case. And, while voltage sensing does not require a sensor in the strict sense of the word, it does require specialized mixed-signal ICs in systems that were previously predominantly digital. It makes sense to combine this capability with the other sensor requirements coming into the PC.

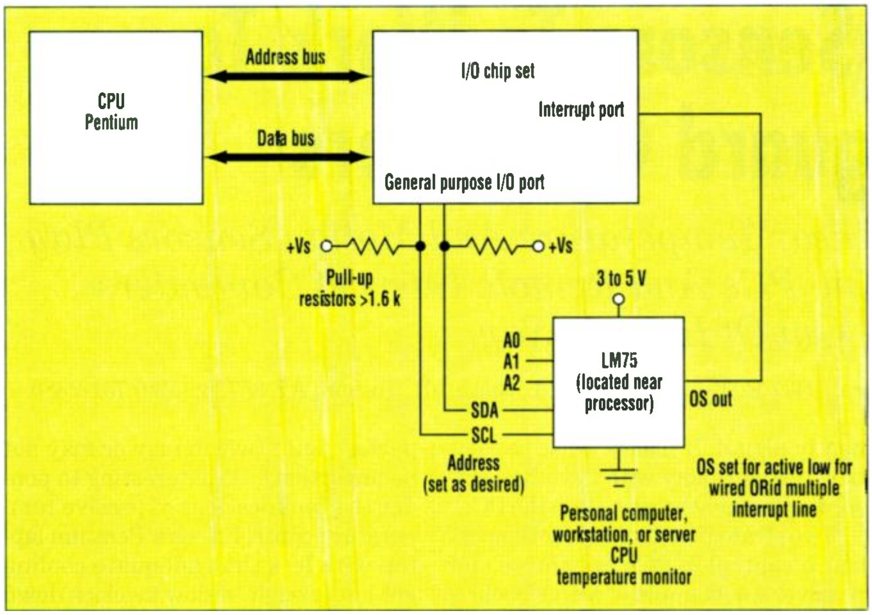
Two strategies common for temperature control in PCs are active and passive. An example of active cooling is the turning on of a cooling fan when the temperature rises to a predetermined set-point. An example of passive cooling (which includes simply using a heat sink) might be the slowing of the processor clock upon reaching a given internal temperature. An advantage of an active cooling system is better overall cooling at—generally—the expense of greater noise and the increased power consumption of fans. Temperature sensing minimizes both of these problems. Fans consume too much power for any laptop, and passive cooling can better control temperatures in laptops. The trade-off with passive cooling is reduced processor performance (which may or may not be important). It's interesting to ponder the ramifications of passive temperature control: does a Pentium laptop with less than adequate cooling get hot enough to slow its clock down enough that an older 486 keeps up?

Temperature sensing is more critical in today's computers than in electronic systems of the past because so much more circuitry and expensive components are packed into today's equipment. In addition, heat related malfunctions or failures can lead to costly system outages.

Temperature sensor placement for computers is much like any other application: The location of the sensor is vital and will influence the ultimate accuracy or usefulness of its output. "Usefulness" implies that it is often more important to sense a temperature event and its cause, than know an exact tem-



1. In this temperature sensor application, an LM78 system hardware monitor is installed on a computer motherboard in close proximity to both the processor and its regulator, the two components most likely to overheat. An LM75 temperature monitor is mounted in the cavity under the processor to respond only to its temperature events.



2. Temperature sensing in a PC is accomplished via a serial interface bus. The bus can be implemented with a pair of spare I/O lines from the I/O chip set (the SDA and SCL lines are usually the same ones of the system management bus or SMB).

perature value. For example, the size of the National Semiconductor LM78 system hardware monitor's 44-pin package dictates its installation in a location that responds to a composite of heat sources *(Fig. 1)*. These include the microprocessor, other components on the board, and the ambient temperature. A second, smaller package sensor such as an LM75 digital temperature sensod can be installed in the socket cavity under the processor where it can respond to processor-related temperature events (for example, the heat sink falling off, or failure of the processor's fan). This cavity location is quite desirable from the standpoint of mass production of printed circuit boards (ELECTRONIC DESIGN, *Aug. 18, 1996, p. 99)*.

The under-processor location is an example of a sensor application that is better suited for indicating a temperature event than a precise temperature value. In fact, the cavity temperature can be up to 10°C cooler than that at the top center reference point of the processor package—the point closest to the die. But the function of the cavity sensor is to indicate a rise-in-temperature event, not an exact temperature value.

A digital-output temperature sensor is a natural choice for computers (rather than an analog output sensor). This leads to products that can communicate via an I²C bus (Inter IC bus), which is used because it is related to the SMB (System Management Bus), a bus standard for communicating with support components within the PC. The mechanical and electrical requirements for a temperature sensor IC within a PC include the smallest possible size, a surface-mount package, and the ability to tolerate power-supply noise, preferably with no power-supply bypassing components.

The LM75 was designed to meet these requirements and simplify the task of temperature monitoring by providing internal, programmable, watchdog set-points. Exceeding the set-points causes an interrupt output called OS (over-temperature shutdown), which notifies the system of a problem. The benefit is that the system is freed from having to constantly poll internal temperatures. A typical installation in a PC shows that the serial interface bus can be generated from a couple of spare General Purpose I/O pins of the I/O chip set. *(Fig. 2)* The only specific hardware requirement of these pins is that they be open-collector (or open-drain) with readback. The rest of the protocol is all software.

Systems that require notification of over-temperature conditions without needing actual temperature data can use a device like an LM56 thermostat output temperature sensor with a user-programmable set point. When the programmed temperature is reached, its digital output level—connected to an interrupt port—is triggered.

Some computer systems still rely on analog temperature sensors such as the LM45 and LM50, the predecessors of digital sensors. Such sensors, however, require analog-to-digital converter (ADC) interfaces to change the data into digital form. Fortunately, the software overhead of analog sensors is minimized since their linear voltage output with temperature eliminates the need for linearization tables to be stored in memory.

The detection of a fan failure, or better yet, impending fan failure, provides an early warning of an overheating event even before a temperature sensor receives any change information. This gives users an opportunity to deal with the problem because the processor is usually still working properly. Fans with failure outputs have long been available. These are logic output lines that become active when the fan drops to typically 70% of its rated speed. This provides a simple, digital-only approach to fan sensing.

Even better system management can be performed if the actual fan speed is known and the hardware monitor IC accepts inputs from fans equipped with tachometer outputs. These also are logic outputs, and in most cases, two pulses per revolution are produced.

Fan failure is generally considered to have occurred when a fan has slowed to 70% of its normal speed, so in systems where fan speed is varied, a tachometer signal is required to determine if the 70% point is reached at any given speed. An early symptom of fan problems is the failure of the fan to start at power-up, even though it starts subsequently. A system check for fan status during or just after boot-up will help provide early warning of fan failure.

Fan sensing is increasingly being used since it provides advance information of an impending temperature event. While it may seem that temperature sensors are a closed-loop solution to temperature problems, an overtemperature condition on the CPU demands an immediate shut-down while early sensing of fan failure provides time in which the system can correct, compensate, or shut down with minimal problems. Multiple temperature sensors show how this can work. Assume an overtemperature condition is

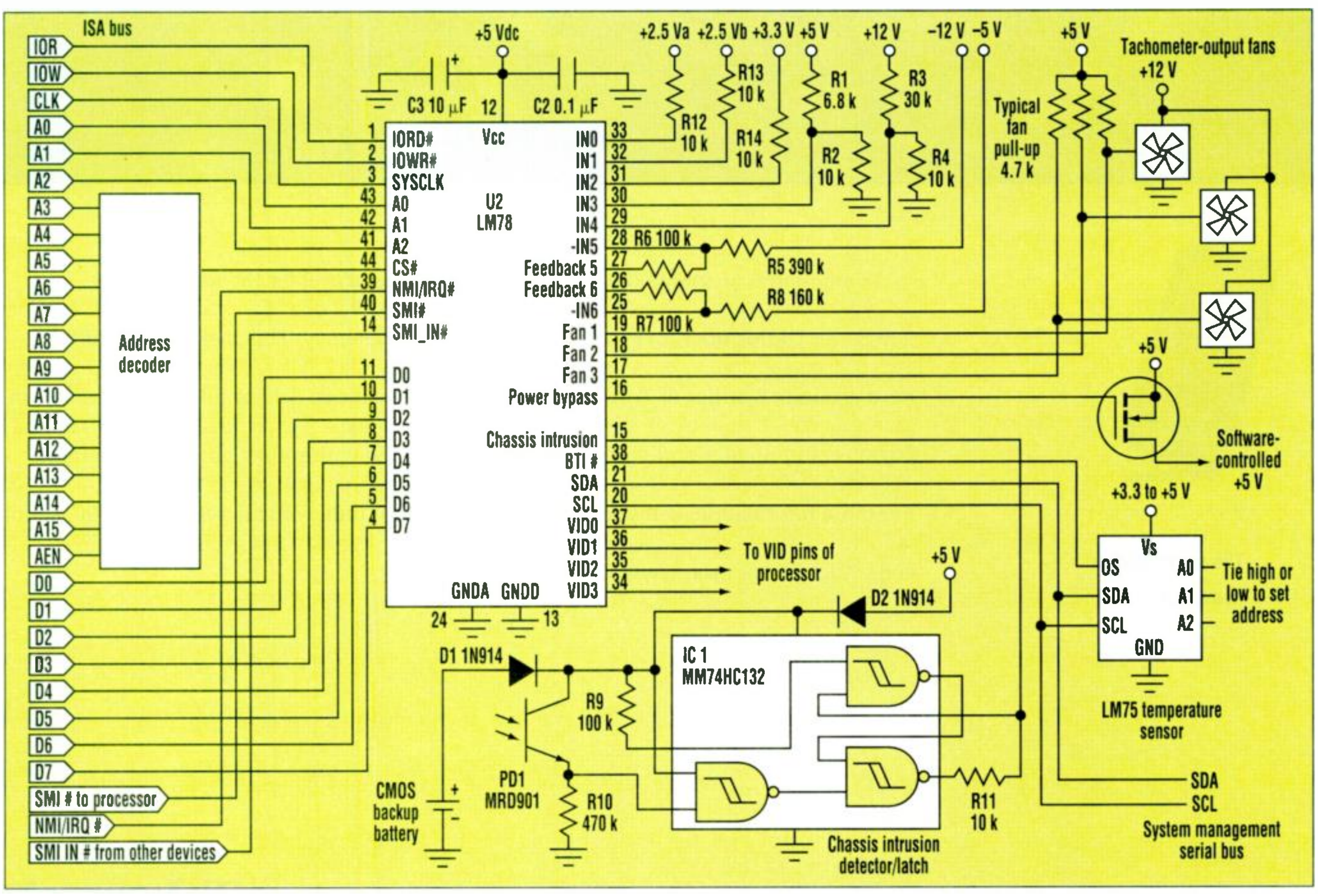
detected on a subsystem such as an audio board. If the processor temperature remains within limits, the system could notify the user, shut down the audio board, yet permit continued use of the computer for other functions.

Multiple temperature sensing can be provided by the LM78, a highly integrated PC hardware monitor chip. It combines temperature sensing, fan tachometer sensing along with 5 positive analog inputs (intended to monitor positive power supplies or signals), 2 inverting inputs (to monitor negative supplies or signals), and inputs from additional temperature sensors. A typical system installation of the LM78 hardware monitor shows the ISA bus interface, and the serial bus, or SMB interface *(Fig. 3)*. The LM78 decodes the three lowest address bus bits and provides a chip-select input for external decoding of the higher bits (the serial bus address is internally programmed). Device power comes from a 5-V rail in order to provide a 0 to 4.096-V analog input range, minimizing the component count. Inputs from 2.5-V or 3.3-V supplies need only an input protection resistor, while 5-V and 12-V supplies require dividers. The LM78 provides inverting op-amps for negative supply monitoring, and has several additional digital inputs and outputs for interrupt handling, power control, and reset functions.

Of particular note is that the LM78 must operate on a 5-V supply which causes conflicts when used on a serial bus that comes from a device operated on a 3-V power supply (the Intel PIIX chip for example). In this situation, a simple circuit permits the interfacing of these two normally incompatible logic levels *(Fig. 4)*. Of the three available fan inputs on the LM78, two can be programmed to work with fans from 1100 to 8800 rpm (the speed which provides 70% of the full-scale count in the monitor) while the third input is limited to 4400 rpm fans. All three provide an internal user-programmable watchdog that issues interrupts when any fans fall to that set-point.

Several alternative methods for interfacing fans may be required. A pull-up to 5 V is the simplest, and most fan tachometer outputs are open-collector *(Fig. 3, again)*. Other situations may require pull-up to 12 V, or have internal pull-up and pull-down to levels in excess of a 0- to 5-V range. An alternative fan sensing method might be necessary in the rare event that ac motor fans are used. In this case, an optical illuminator/detector combination can be used to detect passage of a reflective surface on the fan blades. In some cases, the blades themselves will be reflective enough; in other cases small pieces of reflective tape can be attached.

A simple technique for heading off heat-related problems is to place a temperature sensor adjacent to a small, low-mass heat source such as a low-wattage resistor that is set to dissipate enough power to reach a high temperature—such as 100°C—in the absence of sufficient airflow. If the fan fails, the temperature sensor will detect this rise well before any other



3. A motherboard temperature sensing and monitoring subsystem uses both an LM78 system hardware monitor and an LM75 temperature sensor chip. The LM78 includes an internal temperature sensor and accepts inputs from external temperature sensors (such as the LM75), fan tachometers, power supplies, and chassis intrusion detectors.

M I X E D - S I G N A L & A N A L O G

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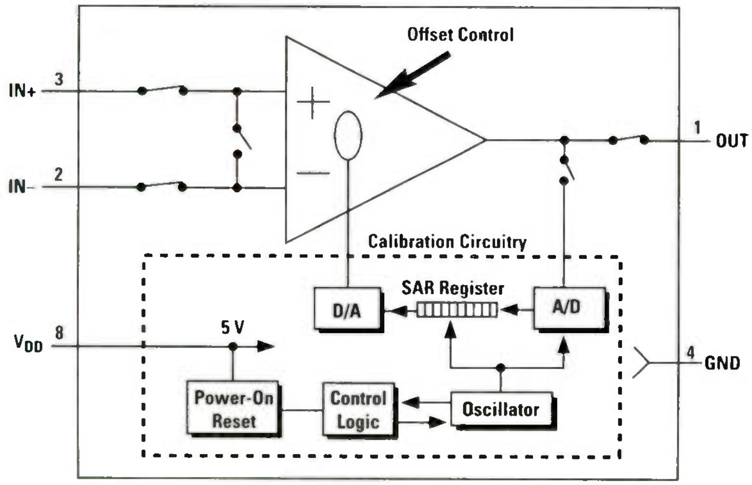

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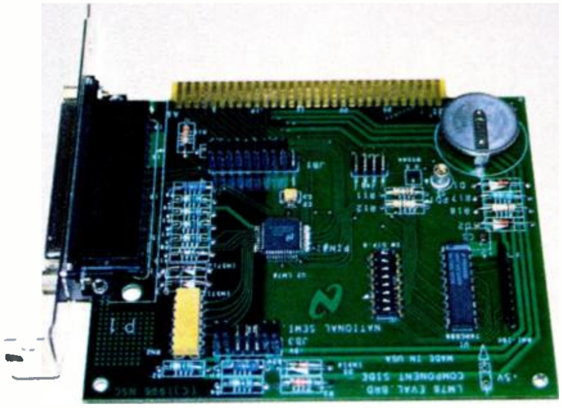
components in the computer have reached critical temperatures.

The LM78 hardware monitor IC, in its 44-pin PQFP package, is too large to permit installation in a location ideal for sensing processor overheating. The additional BTI# (board temperature interrupt) input of the LM78 provides for connection to the OS output of a few LM75 sensors *(Fig. 1, again)*. The LM75's smaller SO-8 package is easier to install close to the processor package, such as in the socket cavity. Other sensors can be installed near such locations as the processor regulator, and high power functions such as audio or modem.



5. This photo of the LM78 evaluation board illustrates the advantage of an optical intrusion detector. The detector is not visually obvious (the TO-46 package photo-detector, labeled PD1 on the board silk-screen, is the intrusion detector.) While this evaluation board is designed to fit a PC card slot, an OEM would put the intrusion detector on the main board where it would be even less visible.

In some situations even an SO-8 package can prove physically too large. In such cases a linear sensor such as a LM45 or LM50 (in tiny SOT-23 packages) can be connected to the analog inputs of the LM78 hardware monitor. This has the advantage that the LM78 in essence adds a watchdog and interrupt capability to these linear sensors (ELECTRONIC DESIGN Analog Supplement, *Nov. 18, 1996, p. 81)*.

Detection of the opening of the case of a computer is important because a system administrator needs to know if someone has tried to insert or remove cards, or tampered with settings or equipment. Case removal should be detected regardless of whether the computer has power applied, and the event should be latched even though the case is back on. An administrator should be able to reset the latch from a remote location. Mechanical switches are an obvious means of sensing case removal, but they present difficulties when trying to meet the requirement of latching the event, and remote electrical reset. In addition, a mechanical switch is, in comparison to other methods, easy to locate and bypass.

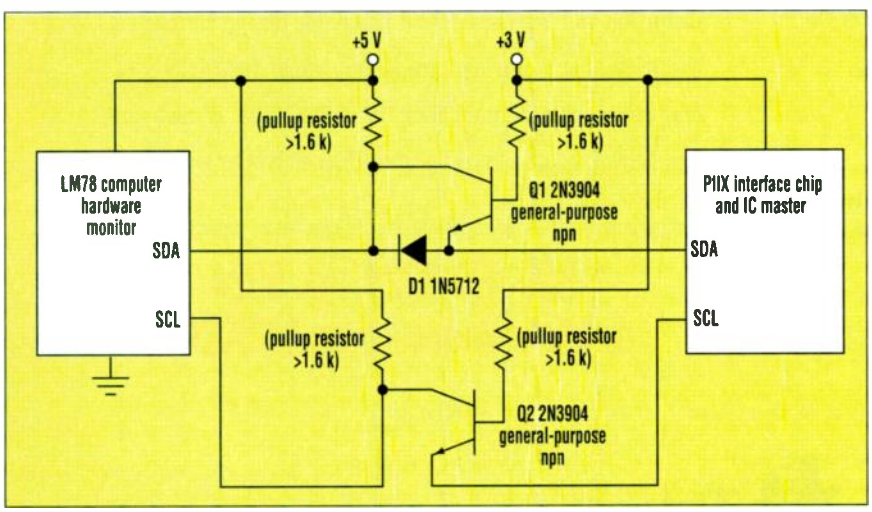
A Hall-effect sensor could be located near the case, requiring a magnet attached to the case. This could be made more difficult to detect and easier to meet the other requirements than a mechanical switch. A requirement of any chassis intrusion detector is that it consume miniscule power since it must be active even if the computer is turned off. This implies that a CMOS backup battery or similar source be used to power the circuit. At this time, Hall-effect sensors are not available with a low enough operating current to make this method practical.

Optical sensors prove to be the best method to meet all these requirements. An optical sensor can be installed inconspicuously almost anywhere on the motherboard. The optical sensor is then incorporated in a latching circuit powered by a backup battery (such as the CMOS backup battery) to operate at all times, and it only requires current when illuminated *(Fig. 5)*.

Other sensor applications in PCs include shock and vibration. Several manufacturers of disk drives for mobile applications include shock sensors for protection when powered. The shock sensors retract the heads when a shock occurs, protecting the drive.

Video recorders have used humidity sensors for years to prevent operation under conditions where dew might have formed on the working mechanism. Laptop PCs could conceivably be used in environments where similar moisture problems are encountered. The temperature sensing previously described could also incorporate low temperature limits to prevent the computer from booting (in most computers, boot-up is all accomplished within solid-state electronics not normally vulnerable to the cold, including the processor and BIOS ROM). These systems, can prevent actuation of mechanical devices such as drives until the temperature is warm enough, or humidity low enough.

Jerry Steele is an applications engineer for National Semiconductor's Data Acquisition Group. He has 25 years of experience in analog engineering.



4 To interface serial bidirectional devices,such as a hardware monitor and interface chip operating at different supply voltages (5 V and 3 V in this case), a simple circuit consisting of two transistors and a diode is used.

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HIGHLY	564
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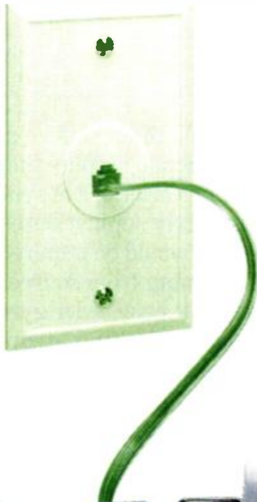

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Genlocking Sync Generator Provides Video Timing From Analog Input

Multi-Standard, Single-Chip Solution Handles Poor-Quality Analog Inputs To Give Clock Generation For Analog Or Digital Processing.

Paul McGoldrick

A major problem in processing analog or digital video signals is the generation of a new clock signal. This signal is based on timing information extracted from analog inputs that may contain noise or variations in sync edges. Normally, fairly sophisticated time-base correction would be required for video signals coming from sources with such problems as camcorder gyro errors, VCR head-switching, dropouts, freeze-frame artifacts, or playback at speed. However, a new IC, the BiCMOS ML6430, is designed to overcome those problems. Working from almost any analog video input it can perform the genlocking function, extracting timing information and creating stable clocks and timing signals. The chip can generate clock signals for both digital and analog video processing systems—MPEG encoders, high-performance displays, video editing devices, LCD and other projectors, and digitizers. It also can act as the master clock for serial digital interface (SDI) processing and transmission.

The ML6430 can cope with high and low luminance and chrominance levels, sync glitches of various kinds, and high noise. Multistandard and nonstandard operation can be provided from a single, external clock or a 3.58/4.433-MHz crystal. Operation in most standard video systems can be set up with pin-selectable preset modes; nonstandard applications can be set on a two-wire serial control bus, which can, in fact, control all of the ML6430's features.

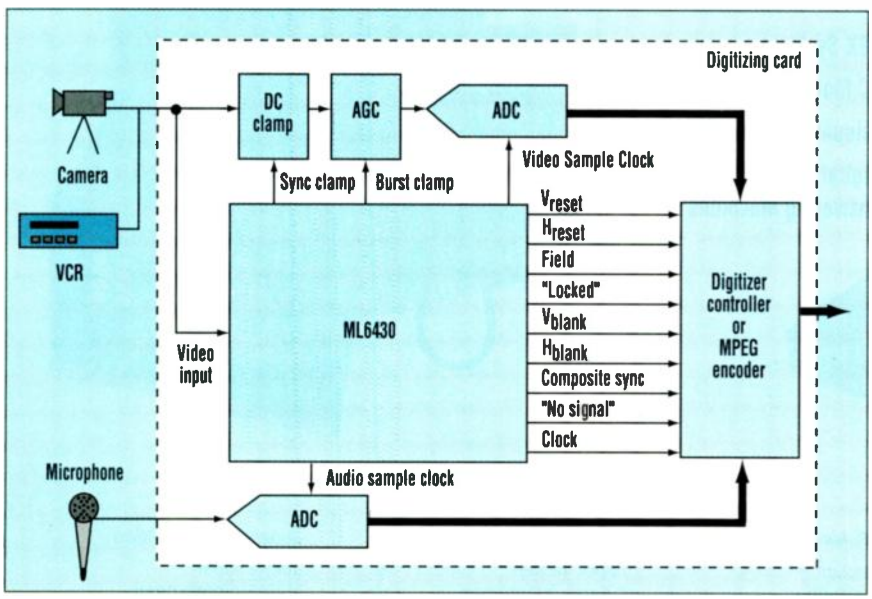
In a typical application, a video source (camera or VCR, for example) would feed a digitizing card with an input to the ML6430 *(Fig. 1)*. The video input can be either composite, the luminance channel of an S-Video system, or a sync-on-green signal from an RGB format. When the input video has no sync, such as a VGA signal, the input can be a TTL-level horizontal sync, with a TTL-level vertical sync applied to a separate input. The IC produces sync- and burst-clamping pulses for the video path processing, and generates the sampling clock for the ADC (the burst clamp may be a burst-gate-clamp pulse or a back-porch-clamp pulse.) It also handles the audio signal, digitizing the audio input using an audio-sampling clock generated by the IC.

With either the standard NTSC subcarrier frequency crystal at 3.58 MHz, or the PAL-B/G subcarrier frequency crystal at 4.433 MHz, all the standard signals can be produced. The oscillators also can be operated at four times the subcarrier frequencies. The preset conditions are enabled on a single three-state pin where the positions represent 3.58/14.43 MHz, 4.433/17.72 MHz, or serial-bus enabled. If one of the presets is enabled, a second pin selects either NTSC or PAL. The digital-audio-clock standards that are produced can be programmed to be 32, 44.1, or 48 kHz.

The outputs from the ML6430 to an encoder or processor, such as an MPEG encoder, consist of horizontal and vertical blanking, horizontal and vertical reset, field ID (odd/even), "no-signal" and "locked" indicators, mixed (composite) syncs, and a clock signal. The clock signal can be at either one or ten times the pixel-clock frequency of the digital PLL part of the IC (at 13.5 or 54 MHz), or at the CCIR 601 rate of 27 MHz.

The IC also can be free run, a useful feature in a decoder operation. The chip could be used as an sync pulse generator (SPG) for analog signal generation; with an external video signal, the IC could be genlocked to that source. However, there are no controls for horizontal and vertical timing with respect to the reference, or for generated burst phase with respect to line timing, so its genlock use would be restricted.

Analog sync separation is employed



1. Micro Linear's ML6430 uses a video source of composite, RGB, Y/C, or VGA to provide all the necessary drives and clocks for MPEG encoding and display, editing, and capture products.

2. The ML6430 is packaged in a 32-pin TQFP and will lock to 525- or 625-line signals in NTSC or PAL, as well as non-standard formats.

to minimize jitter, and peak-tracking analog amplifiers are used with precision sync slicers. The reference voltage for the slicers is set by an external capacitor charged by a charge pump following the sync-tip excursions. Two separate PLLs are used, one formed in analog and the other in digital. The analog circuit takes the external crystal or clock frequency and divides it to scale for the multiple standards possible. The number of pixels per line can be completely arbitrary, but the clock is always line-locked. The serial interface, or presets, set the dividers on the phase detector to match the clock division.

The locked reference oscillator on the analog PLL drives a digital phase modulator on the digital PLL, which sets the horizontal-pixel counter and the vertical-line counter from the separated syncs with suitable digital phase detection and filtering in the loop. The PLL derives all output signals. Timers are included in the PLL loop to discriminate true sync edges from noise glitches or chrominance overshoots. An intelligent state machine monitors loop errors and error history, and adjusts the gains of the loop accordingly.

The digital PLL has five operating states. With a stable video input, the controller stays in state one. With large, but consistent, errors, it will switch to state five. The intermediate steps are gradations from the stable input to the large errors. The state-one gain is low, giving a short-term jitter gain (the ratio of output jitter to input jitter) of about -30 dB. State two increases the gain by four with a corresponding reduction in settling time. State three increases the gain by eight, and state four by sixteen. State four also introduces frequency adjustments for fast settling during non-synchronous-video switches, or pathological gyro errors in hand-held equipment. State five has 16 times gain for phase, and zero gain for frequency changes. This gives quick settling times for head-switch phase disturbances of errors without affecting frequency.

The serial bus control in the ML6430 has two levels of addressing: by device or by register. In device addressing, there are six basic parts of the waveform covered in clock cycles zero through 19. In register addressing, the received data bytes are in two basic parts: four bits give the register number for an address nibble, and four bits give the address for a data nibble. The audio clock is protected from modulation by step changes in the video input (during video-source switches or large-head-switching errors, for example) by being isolated from any generated-phase-change requirements.

The IC, which draws about 35 mA from a single 5-V rail, will handle sync signals in a range from 80 mV to 2 V, and a maximum-composite-video amplitude of 3 V. The output jitter is less than 900 ps rms locked line-to-line, while the short-term output jitter rejection is -15 dB typical, with an input jitter of 50 ns rms. The chip comes in a 32-pin TQFP *(Fig. 2)*.

PRICE AND AVAILABILITY

The ML6430 is in a 32-pin TQFP, and is priced at $15 in 1000-piece quantities. The part is sampling now and will be in production volumes in April.

Micro Linear Corp., 2092 Concourse Dr., San Jose, CA 95131; (408) 433-5200, e-mail: info@ulinear.com; Internet: http://www.microlinear.com. **CIRCLE 493**

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350-MHz Op Amp Family Provides 100-mA Outputs

Excellent Distortion, Noise, And Power Specifications In SOT-23 Packages Remove Previous "Small" Limitations.

Paul McGoldrick

The demands of output current in op amps has required such devices to be fabricated with fairly large die sizes leading to large packages. Using a new output stage design, Comlinear's CLC45X series is a family of high-speed wideband 350-MHz, high-performance op amps and buffers in the small SOT-23 package. They are current-feedback amplifiers built in a complementary bipolar semiconductor process. The company believes that the op amps break the performance logjam that has existed in smaller-package products by delivering 100-mA output drive currents while consuming only a small quiescent current of 1.5 mA from a single +5-V supply rail. They maintain a consistent performance over a wide range of gains and signal levels with a linear phase response up to half of the 3-dB bandwidth frequency.

There are four devices that make up the family. The CLC450 and 452 are current feedback amplifiers, while the CLC451 and 453 are programmable buffers. The CLC452 and 453 are higher current, higher bandwidth products than the CLC450 and 451 and dissipate considerably more power. While all four versions are designed for single 5-V supply operation, they can be operated up to ±5-V dual rails, while the absolute maximum rating is 14 V.

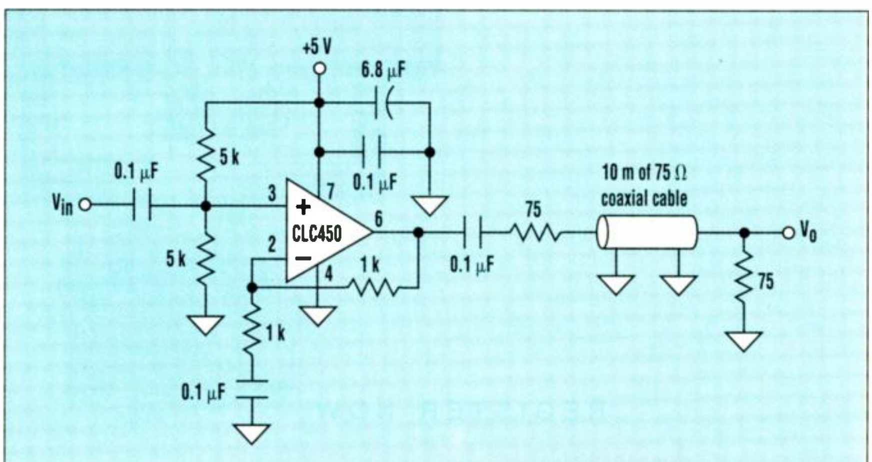
With the capability of driving low-impedance, high-capacitance loads, the products are ideal for driving single-ended cable applications, such as a coaxial cable *(see the figure)*. However, it is expected that applications will include driving twisted pairs, transformers, video line drivers and set-top boxes, high-speed modems, ADSL/HDSL residential systems, and digital video ADCs and DACs. In particular, the second and third harmonic distortion products are low enough so as to make the devices extremely effective for driving high-resolution ADCs.

The buffer versions in the family offer on-chip resistors to give gains of -1, +1, and +2 V/V. If other gains are required, then the amplifier versions of the ICs need to be used. By incorporating on -chip resistors, the buffers reduce the external component count in standardized designs. Some of the key features of current feedback technology are the independence of ac bandwidth and voltage gain, the inherent stability at unity gain, the adjustable frequency response with a single feedback resistor, a high slew rate and fast settling.

A proper printed-circuit layout is essential for achieving the high frequency performance that this family of devices can provide. Comlinear pro-

COMLINEAR'S CLC45X FAMILY OF AMPLIFIERS

Part	Supply (V)	Bandwidth (MHz @ Av=+2)	Dissipation (mW)	Output slew rate I (mA)	Output slew rate (V/µs)	Harmonic distortion 2nd. (dBc)	Harmonic distortion 3rd. (dBc)
CLC450	+5	100	7.5	100	280	–79	–75
	±5	135	16	130	370	–85	-74
CLC451	+5	85	7.5	100	260	-66	-75
	±5	100	16	130	350	–69	-73
CLC452	+5	130	15	100	400	-78	-85
	±5	160	32	130	540	–78	-90
CLC453	+5	110	15	100	370	-65	-84
	±5	130	32	130	460	–69	-90



Depicted is a typical application as a single-supply cable driver for the Comlinear CLC450 current feedback amplifier, and the response at the output of 10 m of 75-Ω coaxial cable to a 10 MHz square wave. Gain is set at +2 V/V to compensate for the termination at the end of the cable.

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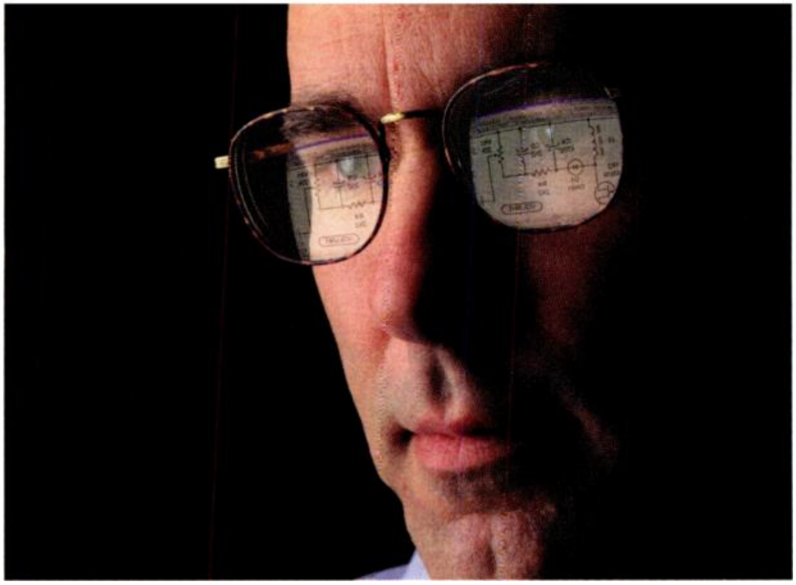

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work is complex

doesn't mean

it has to be difficult

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vides evaluation boards for the products and suggest their board layouts be a guide to the final design. Free SPICE models are also available for the monolithic amplifiers that support Berkeley SPICE 2G and its derivatives that reproduce typical dc, ac, transient, and noise performances.

A sampling of the performance characteristics of the family shows the differences when devices are operated with both a single 5-V rail and dual rails; there is between 20 and 30% improvement in bandwidth; however power dissipation is doubled, while there is a 30% increase in output current and slew rate *(see the table)*.

Input noise voltages are of the order of 3.0 nV/$\sqrt{\text{Hz}}$ while another typical number for the CLC450 powered from a single rail is that the 0.1-dB bandwidth is 30 MHz. The rise and fall times on a 2-V step are about 6.1 ns, with a 16% overshoot. The common-mode rejection ratio (CMRR) is 51 dB and the power-supply rejection ratio is 54 dB. The output voltage range is 1.0 to 4.0 V while the input voltage range (common-mode input range—CMIR) is 0.8 to 4.2 V.

The new family in the SOT-23 package is joined with the release of four other previously announced products in larger DIP/SOIC packages; the main performance parameters remain in the smaller versions. These are: The CLC404, a high-speed op amp with a 165 MHz bandwidth and a 2600V/µs slew rate; the CLC406, a 160-MHz video op amp with low differential gain of 0.02% and phase of 0.02°; the CLC409, a 350 MHz low-distortion op amp with 2nd harmonic distortion of -65 dBc and 3rd of -72 dBc; the CLC425, a low-noise op amp, with input voltage noise of 1.05 nV/$\sqrt{\text{Hz}}$ and a 1.9-GHz bandwidth.

PRICE AND AVAILABILITY

The CLC45X family and the re-released CLC404, 406, 409, and 425 in the SOT-23 TinyPak packages start at $1.39 in 1000-unit lots; all products are available now.

Comlinear Corporation, 4800 Wheaton Dr., Fort Collins, CO 80525; (800) 272-9959; fax (800) 737-7018; Internet: http://www.national.com. **CIRCLE 494**

HOW VALUABLE	CIRCLE
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MODERATELY	556
SLIGHTLY	557

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UPDATE ON AUTOMOTIVE SENSORS

Spread-Spectrum Sensing System Allows Remote Tire-Pressure And Temperature Monitoring On Trucks

The cost of truck tires—and the need to maximize their life—plus the enormous fleet costs of fuel, which increase when tires are run at less than optimum pressure or temperature, leads to a need for continuous monitoring of the running condition of the tires. Tire manufacturers also want to be able to properly analyze potential warranty claims with an idea of how the tires have been treated by the user.

To that end, Integrated Sensor Solutions (ISS) has now come up with a product concept using spread-spectrum technology to provide the solution to this need. The company has already developed an automotive micromachined pressure sensor built into a tire-valve cap. The unit is powered from the RF field of a reader unit, which would normally be a handheld "walk-about" carried by a truck supervisor as part of the daily lookover of a fleet—the more accurate equivalent of the "tire kicker."

The new concept involves using a pressure and temperature sensor built into the tire during production. Periodically taken measurements are transmitted to a centrally located receiver installed under the vehicle. The readings are then passed by cable to a readout or alarm system in the cab of the vehicle, and to any driver-performance chart system mandated by many governments for truck drivers.

To simplify the implementation of the system, it is highly desirable that the RF transmission from sensor to receiver be in a non-licensed area of the spectrum with an approved modulation scheme. In the U.S., this must be done in accordance with Code of Federal Regulations (CFR) Title 47, Parts 2 and 15, while the European Telecommunications Standards Institute (ETSI) has tried to standardize various national low-power schemes under the Industrial, Scientific, and Medical (ISM) umbrella with the ETS 300 220 and ETS 300 328 standards.

The lowest ISM frequency band that has achieved international commonality is at 2.4 GHz under FCC Part 15.247, ETS 300 328 and Japan's RCR-33; no licenses are required when the signal transmissions are within the regulation guidelines. In the U.S., the effective radiated power allowed at 2.4 GHz is severely restricted without spread-spectrum techniques, but such techniques are, anyway, advisable to minimize interference. One of the potential interference sources in the ISM frequency-band is the energy generated from microwave ovens.

The transmission arrangement from the tag in the tire to the reader is performed on an emergency or on-demand basis. For every 'm' minute (perhaps every one minute) the sensor circuits awaken. If a severe change of pressure or temperature occurs, the RF circuits wake up and the new readings are passed on as an emergency situation. If the changes are minimal, the tag shuts down until the next 'm' minute interval has passed; every 'n' minute (maybe every 30 minutes), an updated pressure and temperature reading is transmitted to the reader. Therefore, the tag has effectivelythree operational modes (sleep, measurement, and transmission modes) and the necessary wake-up circuits to switch between them.

Putting the intelligence of the system into the tag allows the tag to transmit real pressure and temperature values instead of just sensor values. The calibration values must be solved in the tag itself so the decision to transmit or not can be made there. In that way the reader can be, essentially, a dumb unit.

The measurement section and the processing circuits are integrated on one IC while the RF section is integrated on a second IC *(see the figure)*. The sensor devices are fully integrated and consist of an absolute capacitive pressure sensor in two parts, one part pressure-sensitive and the other acting as the reference and is non-pressure-sensitive. Both parts are read out and the values are divided to get a result that eliminates any temperature effects. The actual temperature is read from a fixed capacitor that's attached to the pressure sensor

The sensor is built in a multiple array to maximize sensitivity. The digital outputs drive the microcontroller while readings are stored in RAM during calculations with the results stored in EEPROM.

The RF section of the tag is unidirectional with an output power of about 10 mW giving it an operating range of about 100 m. The chip contains the required transmission functions including a direct-sequence spread-spectrum (DSSS) baseband processor, a quadrature IF modulator, the up-converter and RF amplifier. Frequency generation for the transmitter also supplies the clock for the microcontroller, both from an external crystal oscillator. The antenna also is external.

For more information, contact ISS, 625 River Oaks Pkwy., San Jose, CA 95134; (408) 324-1044, fax (408) 324-1054.

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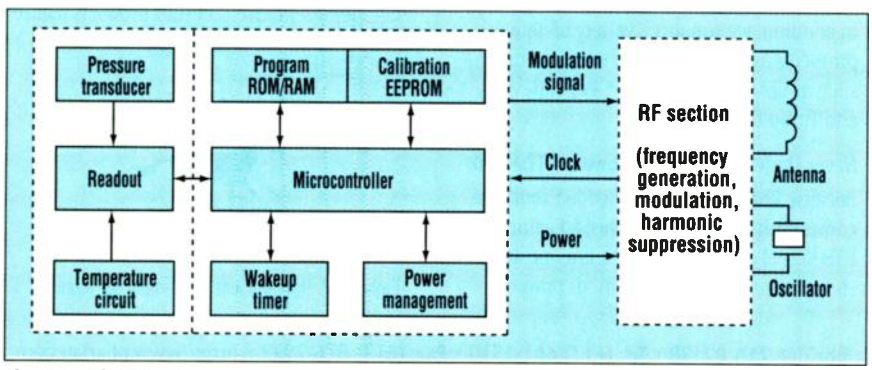

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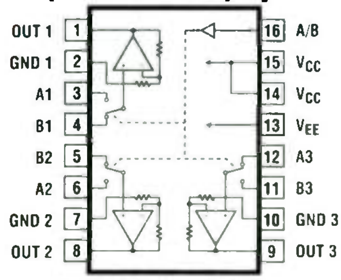

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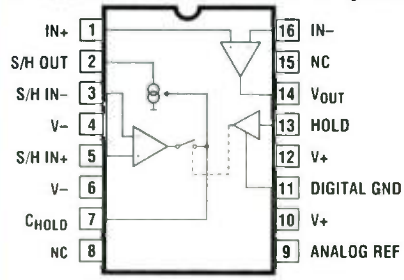

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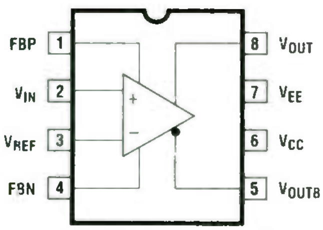

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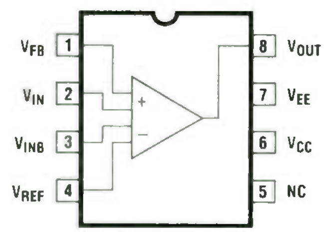

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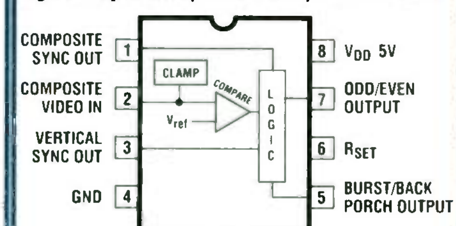

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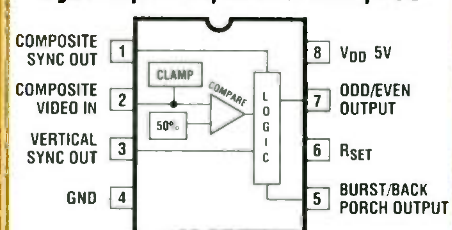

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Optical Detector Selection: A Delicate Balancing Act!

For Optimum System Performance, The Optical Detector Must Be Matched Carefully To Its Amplifier.

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Selecting the correct optical detector can be one of the most critical aspects of designing a viable instrument. While manufacturers' catalogs can give much useful data about the detectors themselves, they don't paint a complete picture. Designers must combine a knowledge of the performance features of the various solid-state detector devices available with an awareness of how amplifiers can affect those features. An incorrect match can seriously compromise overall system performance.

When considering a detector-amplifier combination, it is critical to define the application. Factors such as light power, bandwidth, wavelength, power consumption, and cost will often dictate the detector technology to be used. The most popular options are a photodiode, a p-i-n photodiode, or an avalanche photodiode (APD).

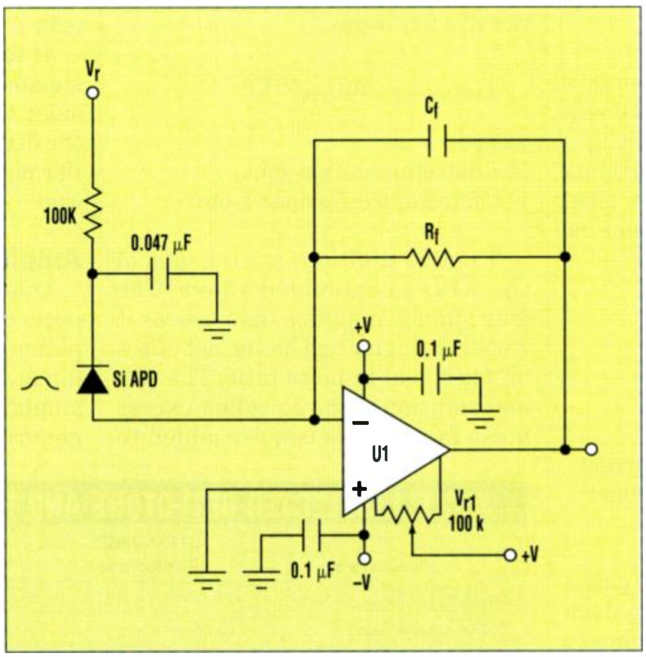
Silicon Photodiodes

A silicon photodiode is essentially a pn junction consisting of a positively-doped p region and a negatively-doped n region. Between these two regions lies a neutral region known as the depletion region. When light enters the device, electrons in the crystalline structure become excited. If the light energy is greater than the band gap energy (Eg) of the material, electrons will move into the conduction band. This creates holes in the valence band where the electrons were originally located. These electron hole pairs are created throughout the device. Electron hole pairs generated in the depletion region drift to their respective electrodes—n for electrons and p for holes. This results in a positive charge build up in the p layer and a negative charge build up in the n layer. The amount of charge is directly proportional to the amount of light falling on the detector. If an external circuit is connected to the p and n electrodes, current will flow in the circuit.

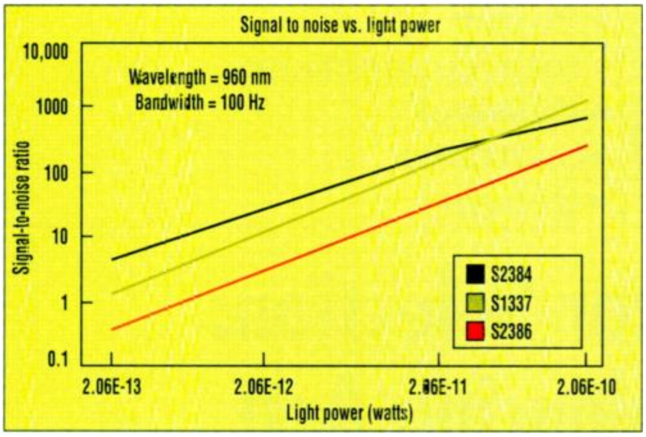
The above describes the photovoltaic mode of operation. It also is possible to apply a reverse bias to the photo detector. Known as the photoconductive mode, this method is generally used for p-i-n photodiodes and APDs, and has the effect of increasing the electrical field strength between the electrodes as well as the depth of the depletion region. The advantages of photoconductive operation are higher speed, lower capacitance, and better linearity. But since the dark current depends on the reverse bias voltage, the dark current becomes larger with increasing bias voltage.

APDs

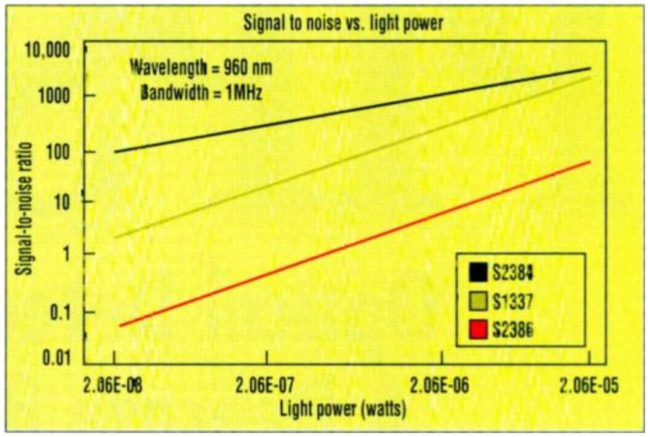
The APD is a specialized silicon p-i-n photodiode designed to operate with high reverse-bias voltages. Large



1. Knowledge of amplifier noise generation is essential if a proper match is to be made between the detector and the amplifier—a necessary feature of any viable system. The transimpedance amplifier shown is one of many possible amplifier configurations.



2. In narrow-bandwidth applications, the photodiode yields better performance than the APD when the amplifier's noise is no longer a factor.



3. Because the APD's gain boosts the signal above the amplifier's noise, it's a good choice for wide-bandwidth applications.

reverse voltages generate high electric fields at the pn junction. Some of the electron hole pairs passing through or generated in this field gain sufficient energy (greater than the bandgap energy) to create additional electron hole pairs in a process known as impact ionization. If the newly-created electron hole pairs acquire enough energy, they also create electron hole pairs. This process is known as avalanche multiplication and is the mechanism by which APDs produce internal gain. Internal gain is an important attribute when the detector is combined with an amplifier, as we shall see later.

Noise

The noise in a photodiode can take one of two forms. The first is the shot noise of the dark current, which results from the statistical uncertainty in the arrival rate of photons. Shot noise is present in all signals, and can be described as:

$$I_{dark} = \sqrt{2qi_{dark}B}$$

where
i_{dark} = rms noise current
q = electron charge
I_{dark} =photogenerated signal current
B = bandwidth of detector-amplifier combination

The second noise source for a photodiode is the thermal noise of the shunt resistance. Also known as Johnson noise, this noise takes the form of:

$$I_{jRsh} = \sqrt{\frac{4kTB}{R_{sh}}}$$

where
I_{jRsh} = rms noise current resulting from Johnson noise
k = Boltzman's constant
T = absolute temperature of the photodiode
R_{sh} = shunt resistance of the photodiode

The shot noise will dominate in photoconductive operation, while the Johnson noise will dominate in photovoltaic mode.

Since an APD is always operated in the photoconductive mode, its noise takes the same form as the photodiode dark current shot noise, with the addition of a few terms:

$$I_{APDdark} = \sqrt{2qi_{dark}M^2FB}$$

where
M = detector internal gain
F = detector excess noise factor

The two additions are the gain of the APD as explained above. The gain simply amplifies the noise as it would the signal and has no net effect on the signal-to-noise ratio. The second addition is the so-called excess noise factor. This is noise added to the output signal by the multiplication process of the APD. It has a strong dependence on wavelength as well as gain.

So far, only the noise equivalent power (NEP) has been a factor in detector selection. As the light level increases, however, the NEP no longer plays a role in the signal-to-noise ratio. The shot noise of the signal itself tends to dominate the signal-to-noise ratio, as shown by:

$$I_{signal} = \sqrt{2q(i_{signal}+i_{dark})M^2FB}$$

where
i_{signal} = photogenerated signal before gain

If the application has strong light signals, one would only need to consider the shot-noise performance of the detector, as dark noise and amplifier noise will be relatively insignificant

Amplifier Selection

One of the most overlooked aspects of detector selection is the amplifier. The amplifier usually sets the lower noise floor for the detector-amplifier combination. Therefore, a general understanding of amplifier

TABLE 1. SELECTED DETECTORS AND THEIR KEY PARAMETERS

Parameters	S1337-33BR Photodiode	S2386-33R Photodiode	S2384 APD
Sensitivity (S)	0.6 A/W	0.6 A/W	30 A/W
Dark Current (i_{dark})	10 pA	100 fA	1 nA
Shunt Resistance (R_{sh})	1 GΩ	50 GΩ	N/A
Terminal Capacitance (C_t)	65 pF	4300 pF	40 pF
Excess Noise Factor (F)	1	1	3.7
Gain (M)	1	1	60

TABLE 2. GENERATED NOISE IN SELECTED DEVICES

Parameters	S1337-33BR Photodiode	S2386-33R Photodiode	S2384 APD
I_{dark}	1.8e-14	1.7e-15	--
$I_{apddark}$	--	--	2.6e-12
I_{Rsh}	4e-14	5.7e-15	--
I_B	5.6e-15	5.6e-15	5.6e-15
I_f	4e-14	4e-14	4e-14
I_v	3.54-15	2.3e-13	3.6e-17
I_{tot}	6e-14	2.3e-13	2.6e-12
NEP Detector + Amp	1e-13 Wrms	3.8e-13 Wrms	8.6e-14 Wrms
NEP Detector	7e-14	9.9e-15	8.6e-14

Bandwidth = 100 Hz, feedback resistor = 1 GW, amplifier bias current = 1 pA, input noise voltage = 15 $nV/Hz^{1/2}$

noise is helpful in choosing a detector. The type of amplifier circuit that will be evaluated here is shown *(Fig. 1)*. The circuit is a transimpedence amplifier and the noise equations shown apply to that configuration. This discussion is by no means complete, however. The design of the photodiode amplifier is very complex and volumes have been written on the subject *(see References at end of article)*.

Amplifier noise can be broken down into three major components. The first two should seem familiar as they take the same form as the photodiode shot noise and Johnson noise. The first term is the shot noise of the amplifier input bias current (I_b). As a general rule, this current is much lower than the photodiode dark current, therefore it seldom presents a problem.

The second term is the Johnson noise of the amplifier feedback resistor, I_f, given by:

$$I_f = \sqrt{\frac{4kTB}{R_f}}$$

where
I_f = rms current due to Johnson noise of amplifier feedback resistance
R_f = feedback resistor

Since the value of the feedback resistor must be smaller than the shunt resistance of the photodiode, this term often dominates the amplifier noise.

The third term arises from the input voltage noise of the amplifier, and it takes the form:

$$I_v = \sqrt{V_a^2 \frac{4\pi^2}{3} c_t^2 B^3}$$

where
I_v = rms current noise due to voltage noise of amplifier
V_a = input voltage noise density ($nV/\sqrt{Hz}$)

The voltage noise current is interesting in that it is very dependent on the terminal capacitance of the detector. It also is very closely related to the bandwidth. The total detector-ampli-

Glossary

Spectral Response—The photocurrent produced by a given level of incident light varies with the wavelength. This relationship between the photoelectric sensitivity and wavelength is referred to as the spectral response characteristic and is expressed in terms of photo sensitivity, quantum efficiency, and so on.

Photo Sensitivity—This measure of sensitivity is the ratio of radiant energy expressed in watts (W) incident on the device, to the resulting photocurrent expressed in amperes (A). For example, 0.5 A/W

Quantum Efficiency (QE)—The quantum efficiency is the number of electrons or holes that can be detected as a photocurrent divided by the number of incident photons. This is commonly expressed in percent (%).

Dark Current (I_{dark})/*Shunt Resistance* (R_{sh})—The dark current is a small current that flows when a reverse voltage is applied to a photodiode, even in a dark state. This is a source of noise for applications in which a reverse voltage is applied to photodiodes (for example, as with p-i-n photodiodes). In contrast, for applications where no reverse voltage is applied, noise characteristics are figured out from the shunt resistance. This shunt resistance is the voltage to current ratio in the vicinity of 0 V.

Terminal Capacitance (Ct)—The terminal capacitance refers to the total capacitance of the detector pn-junction capacitance plus any stray capacitance introduced by the package and detector leads. The junction capacitance is the major factor in determining the response speed of the photodiode.

Rise Time (t_r)—This is the measure of the time response of a photodiode to a stepped light input, and is defined as the time required for the output to change from 10% to 90% of the steady output level. It depends upon the incident light wavelength and the load resistance.

Cut-Off Frequency (f_c)—This refers to the response of high speed avalanche and p-i-n photodiodes to a sinewave-modulated light input. It is defined as the frequency at which the photodiode output decreases by 3 dB.

Frequency Bandwidth (B)—Defined as the frequency range of the detector system, it is generally limited by the response speed of the detector amplifier. If the detector is limiting the response speed, the Frequency Bandwidth will equal the cut-off frequency.

Noise Equivalent Power (NEP)—The NEP is the amount of light equivalent to the noise level of a device. Stated differently, it is the light level required to obtain a signal to noise ratio of unity. NEP is measured at a bandwidth of 1 Hz and thus expressed in units of $W/\sqrt{Hz}$.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fier noise is described by:

$$I_{tot} = \sqrt{(I_{dark})^2+(I_{Rsh})^2+(I_b)^2+(I_f)^2+(I_v)^2}$$

It is now possible to calculate the NEP for a given detector, and, based on these calculations, select a detector that is best for a particular application. It is useful to make a table of the various devices under consideration and see what parameters affect performance the most *(Table 1)*. As can be seen from the table, the S1337 photodiode is designed for low capacitance, the S2387 for low dark current, and the APD to produce gain. The devices were selected with approximately the same active area size. The same amplifier will be used in the calculation of noise to get a feel for how the detector affects the total noise performance.

Some light is shed on detector selection, in the context of noise, in *(Table 2)*. From the above, it would seem to make the most sense to select the APD, but the APD requires a high-voltage power supply to bias it, is very temperature sensitive, and generally costs more than a photodiode.

Therefore, in the example shown, the S1337 would seem to be the best choice. Furthermore, when considering the detector's signal-to-noise performance at various light levels, it can be seen that the photodiode's performance will be better than the APD's when the amplifier noise is no longer a factor *(Fig. 2)*. This is because of the excess noise factor of the APD. Unless the application demands the lowest NEP possible, the photodiode would be the best choice under these conditions.

Based on the equations given, it is evident that amplifier noise is strongly dependent on the bandwidth. The results shown in Figure 2 were calculated at a bandwidth of 100 Hz. If the calculation was instead done at a 1-MHz bandwidth, the result would be much different *(Fig. 3)*. Because of the higher noise in wide-bandwidth applications, the APD is a good choice as it boosts the signal above the noise of the amplifier. Overall, choosing the correct detector is very application-specific. Here are some guidelines;

Try to use the smallest active area possible. If the light source for the application is diffuse, this might not be practical but from the standpoint of noise, small diodes have lower capacitance and dark current. They also are less expensive.

In most applications, small capacitance will be more important than small dark current. Furthermore, the NEP in the catalogs does not take capacitance into account, therefore care should be exercised when comparing detectors using NEP.

In low-bandwidth applications, photodiodes operating in a photovoltaic mode will generally outperform device-operated photoconductivity. To reduce noise, the detector shunt resistance should be much greater than the feedback resistance.

To reduce the Johnson noise, use as large a feedback resistor as possible in the first amplifier stage.

In wide-frequency-bandwidth applications, PIN photodiodes operating in the photoconductive mode are preferred because of lower terminal capacitance. APDs, with their internal gain, also perform well in wide-band applications. They should be considered when the light source is weak and the amplifier noise is large.

Earl Hergert earned a BA in Physics from Rutgers University and has been an Applications Engineer with Hamamatsu since 1989.

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Dymec, Inc. **Chelmsford, MA 01824** **Sales Dept. (919) 870-8564** **Fax (919) 870-0564** **CIRCLE 726**	Links/ repeaters, datalinks, optical stars	Both	850 nm (singlemode), 1300 nm (multimode)	20 dB optical budget	0 to 2 Mbits/s	-40° to 85°C	ST (optical), 25 pin (electrical)	LED	PIN photodiode
Ericsson Inc., Components **Richardson, TX 75081** **Jim Oursler (972) 583-7236** **Fax (972) 583-5005** **jim.oursler@ericsson.com** **http://www.ericsson.com** **CIRCLE 727**	Transmitters, receivers, transceivers, and sub-modules	Both	1310 and 1550 nm	-13 to 2 dBm	155.52 and 622.08 Mbits/s, and 2.488 Gbits/s	-40° to 85°C	Pigtail and integral	DFB, Fabry-Perot, and EA laser	PIN and avalanche photodiode
Force, Inc. **Christiansburg, VA 24073** **Chris Walters (540) 382-0462** **Fax (540) 381-0392** **force@forceinc.com** **http://www.forceinc.com** **CIRCLE 728**	Video, audio, data, fiber-optic transmission equipment	Both	850, 1300, and 1550 nm	-2.0 to 0 dBm	N/A	0° to 50°C	Integral	LED and laser	PIN photodiode
Fujikura America, Inc. **Santa Clara, CA 95051** **Chris Simoneaux** **(770) 956-7200** **Fax (770) 956-9854** **chris@fujikura.com** **CIRCLE 729**	Transceivers	Datacom	770 nm	-5 to -10 dBm	1.062 Gbits/s	0° to 50°C	Integral	Fabry-Perot laser	PIN photodiode
Gould Fiber Optics Div. **Millersville, MD 21108** **Moez Adatia (410) 987-5600** **Fax (410) 987-1201** **madatia@gouldfo.com** **http://fiberoptic.com/gould** **CIRCLE 730**	Amplitude modulator	Telecom	1550 nm	23 dBm	2.5 Gbits/s	0° to 70°C	Pigtail	Not given	Not given
H&L Instruments **North Hampton, NH 03862** **J.H. Landman (603) 964-1818** **Fax (603) 964-8881** **CIRCLE 731**	Transceivers, self-healing redundant-loop system	Datacom	850 nm, 1300 nm, single and multi mode	-24 to -8 dBm	19.2 kbits/s by four channels	-40° to 85°C	Integral	LED and laser	PIN photodiode
Hewlett-Packard Co., Components Group **San Jose, CA 95131** **Component Response Center** **(800) 235-0312** **Fax (408) 654-8575** **http://www.hp.com/go/ components** **CIRCLE 732**	Transceivers, transmitters, receivers, and ICs	Both	650, 820, 1300, and 1550 nm	Up to 1 mW uncooled, or 2.5 mW cooled	Up to 2.4 Gbits/s	From -40° to 85°C	Both	LED and laser	PIN photodiode

Mass-Produced MBE Laser Diodes Are Low Cost

The RLD Series of low-cost, mass-produced molecular-beam-epitaxy (MBE) laser diodes target short-distance communication links, including Fibre Channel and ATM. The devices provide high-frequency relaxation oscillation between 1.8 and 3.5 GHz to reduce modal noise and have an optical output power of 5 mW. The operating voltage and current requirements are 1.9 V (2.3 V max) and 45 A (65 mA max), respectively. Other features include an MTBF of over 100,000 hours at 60°C and 3-mW (CW) operation. The device outputs at 785 nm. Pricing is $9 each in quantities of 1000.

***Rohm Corp.**, 3034 Owen Dr., Antioch, TN 37013; Mark Inman (615) 641-2020, ext. 171; fax (615) 641-2022; http://www.rohmelectronics.com*
CIRCLE 741

MANUFACTURERS OF ACTIVE FIBER-OPTIC COMPONENTS

Manufacturer	Active component(s)	Datacom or telecom	Operating wavelengths	Output power range	Bit rate	Operating temperature range	Connector type	Transmitter element	Receiver element
Honeywell, MicroSwitch Div. Richardson, TX 75081 Customer Response Center (800) 367-6786 Fax (214) 470-4326 info@micro.honeywell.com http://www.sensing.honeywell/com CIRCLE 733	Transmitters, receivers, transceivers, connectorized components	Datacom mostly	850 nm	Up to 5 mW	0 to 1.25 Gbits/s	Up to 100°C	Standard interface (ST or SC)	LED and VCSEL	PIN photodiode
Laser Diode Inc. Edison, NJ 08820 Sales Dept. (908) 549-9001 (908) 906-1559 http://www.laserdiode.com CIRCLE 734	Transmitters, receivers, transceivers	Both	850, 1300, and 1550 nm	4 µW to 2 mW	1 Mbits/s to 1 Gbits/s	-40° to 85°C	Both	LED and laser	PIN photodiode
MRV Communications, Inc. Chatsworth, CA 91311 Ken Ahmad (818) 773-9044 Fax (818) 773-0261 CIRCLE 735	Transmitters, receivers, and transceivers	Both	1310 and 1550 nm	-15 dBm to 6 dBm	Up to 1 Gbits/s	-40° to 85°C	Pigtail and integral	LED and laser	PIN photodiode
Osicom Technologies, Inc. Broadband Comm. Div. San Diego, CA 92121 Sales Dept. (800) 854-2831 Fax (619) 558-3980 info@osicom.com CIRCLE 736	Transmitters, receivers, and transceivers	Both	850, 1310, and 1550 nm	Up to 8 mW	Not given	0° to 50°C	Both	LED and laser	PIN and avalanche photodiode
Rohm Electronics Nashville, TN 37013 Mark Inman (615) 641-2020 Fax (615) 641-2022 minman@rohmelectronics.com CIRCLE 737	Transmitters	Datacom	780 and 850 nm	0 to 5 mW	Up to 1 Gbits/s	-10° to 80°C	TO can laser diodes	Fabry-Perot laser	N/A
S.I. Tech Batavia, IL 60510 Chris Cirko (630) 232-8640 Fax (630) 232-8677 http://www.bitdriver-sitech.com CIRCLE 738	Transmitters, receivers, and transceivers	Datacom	850 or 1300 nm	10 to 100 µW	Up to 40 Mbits/s	0° to 50°C	Internal	LED	PIN photodiode
Siemens Components Inc. OED Fiber Optics Cupertino, CA 95014 Elizabeth Busetti (408) 725-3406 Fax (408) 725-3435 http://www.sci.siemens.com CIRCLE 739	Transceivers, receivers, bi-directional modules	Both	850, 1300, and 1550 nm	-20 dBm to 2 dBm	0 to 2.5 Gbits/s	-40° to 85°C	Integral and pigtail	LED and laser	PIN photodiode
Toshiba America Electronic Components, Inc. Irvine, CA 92618-1811 Margie Ferro (714) 455-2293 Fax (714) 859-3963 margie.ferro@taec.toshiba.com CIRCLE 740	Transceivers, receivers, transmitters	Both	Toslink = 650 to 850 nm, CLD = 1300 to 1500 nm	Toslink N/A, CLD = -15 to 3 dBm	From dc up to 10 Gbits/s	-40° to 85°C	Pigtail, and integral	LED and laser	PIN photodiode

Fiber-Optic Components Target Legacy LANs

Designed to be pin-for-pin-compatible with standard ST fiber DIP products, the HFD3300 SC Fiber DIP analog receivers and HFE4300 transmitters are aimed at legacy LANs such as

Ethernet and Token Ring. The receivers comprise a silicon PIN photodiode and a pre-amp IC and operate at data rates up to 125 Mbits/s . Also available as a low-cost alternative to 1300-nm components, the receivers output a linear voltage proportional to the optical input range of 1.0 to 175 μW peak. This gives a dynamic range of 23 dB. The transmitters couple power into different fiber sizes ranging from 50 to 125 μm to 200 to 240 μm. The operating temperature range is 40° to 85°C. Pricing is from $16.84 to $18.71 per component, and delivery is four to six weeks.

Honeywell, MicroSwitch Div., *11 W. Spring St., Freeport, IL 61032; 800-367-6786; opto@micro.honeywell.com; http://www.sensing.honeywell.com*
CIRCLE 742

DFB Laser Targets SONET OC-48 And SDH STM-16 Use

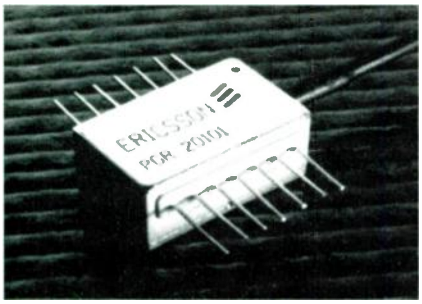
The Model 55TA is a ready-to-use distributed-feedback (DFB) laser trans-

mitter module for SONET OC-48 and SDH STM-16 applications. The device is optically isolated for dense wave-division multiplexing at 1550 nm and is wavelength-stabilized via a tightly controlled thermoelectric cooler circuit. Any one of 36 specific laser wavelengths can be ordered. The laser is capable of transmitting at distances over 75 km with standard single-mode fiber-optic cable and meets all published specifications over a 0° to 65°C temperature range. The device is certified as a Class 1 source and is specified for 2-dB maximum optical path penalty through 1200 ps/nm of dispersion. A 1310-nm DFB laser is also available.

Broadband Communications Products Inc., *305 East Dr., Melbourne, FL 32904; Richard Anders, (407) 984-3671; fax (407) 728-0487; fiberlink@bcpinc.com*
CIRCLE 743

APD Receiver Suits OC-48 Applications

Available in a 14-pin butterfly package, this family of avalanche photodiodes (APDs) suits OC-48 Long Reach applications at 2.5-Gbits/s. The PGR



20101 and PGR 20101 have typical sensitivities of -34 dBm and -33 dBm, respectively, and come with various options with respect to optical connectors, power supplies, and internal thermistors. The receivers maintain an overload of -8 dBm and -6 dBm, respectively, to maximize dynamic range.

***Ericsson Inc. Components**, 701 N. Glenville Dr., Richardson, TX 75081; Jim Oursler, (972) 583-7236; Jim Oursler@ericsson.com*
CIRCLE 744

Fiber-Optic Converter Has Bandwidth Down To DC

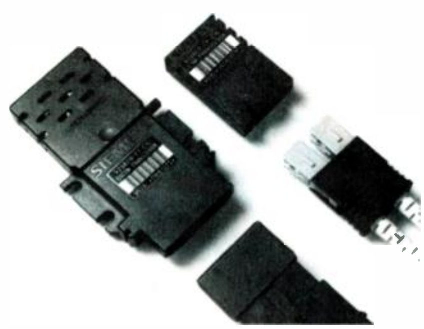
The Model 279 is a single-mode to multimode fiber-optic converter with a data throughput of up to 2.5 Mbits/s. Because the device operates to dc, a

line-loss switch is used to control the gain of the amplifiers to provide acceptable performance over single-mode fiber cables. The switch allows the converter to accommodate single-mode cable losses of 2, 5, 10, and 15 dB.Thes loss approximate cable lengths of 3, 7.5, 15, and 20 km, respectively. The selected line loss is displayed on one of the four LEDs.A phase-reversing switch also is included. A pair of Model 279s can be used to provide conversion for 850-nm multimode signals to 1300-nm single-mode signals. All fiber ports use ST connectors. The device measures 7 by 3 by 1 in. and operates off 110 or 220 V. Pricing is $775 with availability from stock.

***Telebyte Technology, Inc.**, 270 Pulaski Rd., Greenlawn, NY 11740; (800) TELEBYT; fax (516) 385-8184; sales@telebyteusa.com; http://telebyteusa.com*
CIRCLE 745

Transceiver Transmits At 320 Mbits/s Over 3 km

This line of 1300-nm, LED-based fiber-optic transceivers is designed for the reliable transmission of data over distances of 3 km at rates of up



to 320 Mbits/s. The devices operate from a single 3- to 5-V supply, a key feature for networks. Included in the line is a parallel transceiver for ESCON/SBCON and Fibre Channel applications that comes in a 35-by-40-mm surface-mount package. Multimode transceivers also are included for Fast Ethernet, ATM, FDDI, FC, B-ISDN, and SONET applications that meet the Common Mezzanine standard requirements of a profile lower than 10 mm.

***Siemens Electromechanical Components Inc., Fiber Optics Div.**, 4677 Old Ironsides Dr., Suite 210, Santa Clara, CA 95054; (408) 982-1980; fax (408) 980-8450; http://www.sci.siemens.com*
CIRCLE 746

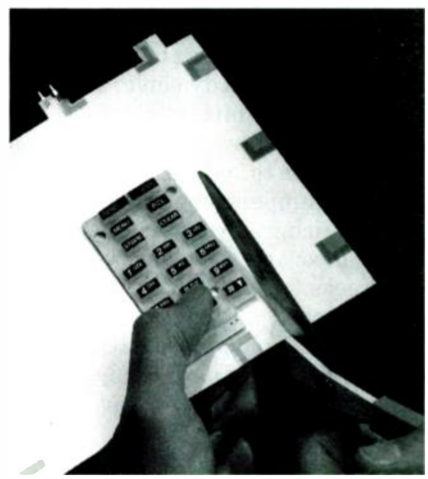
DC-AC Inverters Drive Dual Synchronized CCFTs

The K Series of dc-ac inverters come with dual output connectors to allow it to power two separate CCFT tubes in synchronization. The device has a profile of 8 mm, is available with multiple dimming options, and can be custom designed to ensure a proper match between the inverter and the display.

***Endicott Research Group Inc.**, 2601 Wayne St., Endicott, NY 13760; Scott Barney, (607) 754-9187; fax (607) 754-9255; ergsales@aol.com; http://www.ergpower.com*
CIRCLE 747

EL Lamps Can Be Cut And Shaped To Fit

The Proto-Kut cut-to-fit electroluminescent (EL) lamp panels can be cut to fit any shape using a pair of scissors, a blade, or a knife. The only re-



striction is that a pair of terminations remains connected to the portion of the lamp intended for use. Although not a substitute for custom-engineered lamps, the kit provides a convenient and inexpensive means of experimenting with EL lamps before committing to a design. The kit includes a low-voltage lamp (70 to 80 V rms) powered by an IC inverter with two AAA cells, plus one high-voltage lamp (up to 160 V rms) powered by either of two magnetic-resonating transformer-type inverters that operate off 9 V dc. Both measure 5 by 8 in. and have up to 14 pairs of terminals. Pricing is $100.

***BKL Inc.**, 421 Feheley Dr., King of Prussia, PA 19406-2658; Beth String, (610) 277-2910; fax (610) 277-2956.*
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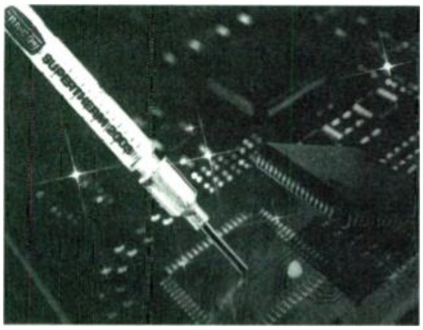
READER SERVICE 131

PACKAGING & MATERIALS

Epoxy Adhesives Are Thermally Conductive

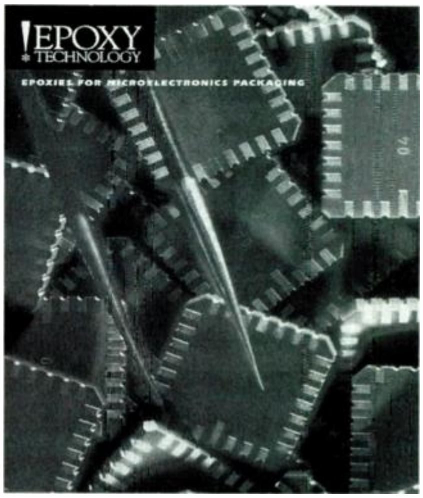
The Supertherm 2003 is part of the company's Supertherm line of thermally conductive epoxy adhesives that come in easy-to-use cartridges and syringes for manual or automatic dispensers. The adhesives are designed for microelectronic applications and come with a variety of fillers, including diamond, boron nitride, and aluminum nitride. The 2003 is a diamond-filled, electrically insulating thixotropic paste that meets MIL-STD-883C (Method 5011). The paste adheres to metal, glass, ceramics, and laminates, and has a shear strength of greater than 2000 psi. The operating temperature range is -60° to 160°C.



Tra-Con Inc., 45 Wiggins Ave., Bedford, MA 01730; (800) TRACON1; fax (617) 275-9249.
CIRCLE 749

Silver-Filled Epoxy Bumps Improve Performance

Designed specifically for the company's patented Polymer Flip Chip technology, the EPO-TEK H20E-PFC is a silver-filled conductive epoxy. The epoxy is offered as alternative to solder techniques to achieve lower cost, lower-temperature processing, and finer resolution using one-step screen-printing or stenciling techniques. The thixotropic paste allows for the deposition of bumps measuring 25 to 30 µm high with a 5-mil pitch. It will neither bleed out nor slump, and it has a snap-cure time of 45 seconds at 175°C to 90 min. at 80°C. Once cured, the epoxy has a volume resistivity of 0.00001 to 0.0004 Ω-cm and a V_{cesat} of 0.51 V at 4-A/400-mA base.



Epoxy Technology Inc., 14 Fortune Dr., Billerica, MA 01821-3972; (508) 667-3805, or within USA, (800) 227-2201; fax (508) 663-9782.
CIRCLE 750

Tube-Axial Fan Provides Quiet Operation

Available in ac and dc versions, the Maltese tube-axial fan has a capacity of 300 CFM and comes with a feathered-edge propeller for quiet operation.

The dc version operates off 12, 24, or 48 V dc, while the ac version operates off 115 V or 220/230 V ac, single phase, 50/60 Hz. Both come with various fan performance sensors, ball-bearing construction, and terminal, leadwire, and harness assemblies. The fans weigh 1.8 lb, are 2.165 in. deep, and have an operating temperature range of -10° to 70°C. Pricing is $40 for the ac version and $45 for the dc version. Delivery is eight weeks.

Comair Rotron, *2675 Customhouse Court, San Ysidro, CA 92173; Mike Turner, (619) 661-6688; fax (619) 661-1757; mturner@comairrotron.com*
CIRCLE 751

30-mm Fan Cools Notebook Computers

The 1204KL Boxer Series cooling fan measures 30 by 30 mm, has a height of 10 mm, and provides up to 4 CFM of free-air performance. Designed for spot cooling microprocessors and other pieces of equipment, the fan weighs 8.5 g, operates off a 6- to 18-V-dc supply, and uses a ball-bearing-based design. Pricing is $8 to $10.

NMB Technologies Inc., *9730 Independence Ave., Chatsworth, CA 91311; (800) 662-8321; fax (818) 341-8207*
CIRCLE 752

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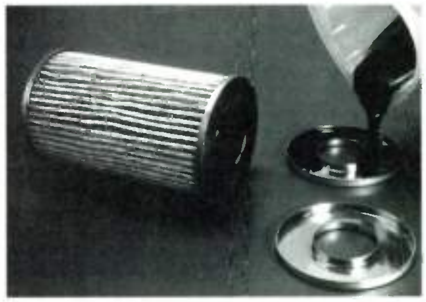

perature range of -65° to 230°C. The epoxy-based adhesive bonds to metals, plastics, ceramics, and glass, and has typical tensile lap shear values of greater than 2000 psi. Packaging is in one- or two-component systems.

Grace Specialty Polymers, *55 Hayden Ave., Lexington, MA 02173; Don Whitehouse, (800) 832-4929; fax (617) 861-9066.*
CIRCLE 753

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RADSTONE TECHNOLOGY

READER SERVICE 207

MEETING THE STANDARD

1997: The Year Of Technology On VME

Ray Alderman, VITA

In 1996, both the VITA and the VME communities concentrated on understanding the markets and marketing of VME-based products. We learned from reports developed in 1994 by Venture Development Corp. (VDC), city, state, that the military (29%), telecom (25%), and industrial-controls (20%) markets comprise the largest segments of VMEbus use. Other applications like transportation (traffic control, automated weigh-stations), medical equipment (CATscan, PETscan, and MRI machines), and scientific applications (particle physics research) round out the major markets for the venerable VME technology. Furthermore, we observed that the concentration of VME consumption was in the U.S. (60%), followed by Europe (30%), according to VDC.

The 1996 VME VDC market research shows exactly how these markets are changing. The total VME board market has grown from $937.9 million in 1994 to $1.262 billion worldwide in 1996 with about 48% coming from the US market and 35% from Europe.

Asia and South America now constitute a higher portion of the demand for VME boards. Board usage by industry segments shifted to 26% military, 27% telecommunications, and 26% in industrial applications. These three market segments totaled 72% of VMEbus application usage in 1994, and have increased to 79% in 1996.

Furthermore, OEM consumption of VME cards has increased from 67% in 1994 to today's 73%, while the percentage of system integrators remained nearly constant at 22%. OEM volume use of VME cards has been the primary source of the VMEbus' 17% per year growth rate in 1995 and 1996. End-user board consumption actually decreased from 11% in 1994 to about 5% in 1996.

This year promises to be the "Year of Technology" on the VMEbus. Many of the basic concepts of computer architecture will change dramatically in the next 12 months, and 1997 will be a challenging year for VMEbus designers. The sub-bus technologies on the P2 and P0 connectors (Raceway, Skychannel, Heterogenous InterConnect (HIC), Signal Computing System Architecture (SCSA), Myranet, and ATM Cellbus) will all continue to develop followings in military and telecom applications. The field buses (industrial I/O serial buses) will expand the use of VME in many industrial applications at the high end of the market. Upon completion of all the technical committee work, VME itself will show some dramatic advances in its bus speed in 1997.

Along with these additions to the bus, 1997 will be a year of technology transition in five basic areas in ALL computers: CPUs, memory architectures, chip sets, graphics, and I/O subsystems. CPUs are doubling in clock speed every 12 months. The chip sets and the memory architectures must catch up or system performance will plateau. At the same time, graphical presentation mechanisms are transitioning to advanced accelerator chips or are being integrated as part of the CPU instruction set. Finally, the microprocessor industry is learning what mainframe designers discovered in the mid-1970's—don't mix I/O and memory traffic in a high bus-utilization environment. As a result, we'll see implementations of USB, IEEE 1394 (Firewire), PCI, VMEbus, and possibly Fibre Channel to handle the I/O traffic, and advanced multiprocessor techniques to solve the bottlenecks.

The true measure of any technology is not its sales or market share, but its ability to adapt to technological change. While synchronous buses come and go based on the next higher clock frequency, the asynchronous VMEbus has adapted for the last 15 years to faster CPUs, local buses, and communications and I/O interfaces. Tremendous technological advances at the desktop and in the telecommunications industry have been adapted and implemented on VME by using creative thought and sound engineering practices.

Adapting the new technologies from the mainstream markets is VME's greatest asset, and it will continue in 1997. In the long run, VME has more technological innovation in front of it than behind.

There's an ancient Chinese proverb that says, "May you live in interesting times." This certainly holds true for both VME and its manufacturers. This year of transition contains the promise of innovation, progress, and prosperity for many years to come, not only for VME as a technology, but also for its users and manufacturers.

Embedded PCI Meets 68K: Some Bridging Issues

As PCI Proliferates, Embedded Systems Designers Need A Way To Bridge From The 68K-Based CPUs To The PCI Bus.

TOM WILSON AND RICHARD O'CONNOR, Tundra Semiconductor Corp., 603 March Rd, Kanata, Ontario, Canada, K2K 2M5; (613) 592-0714.

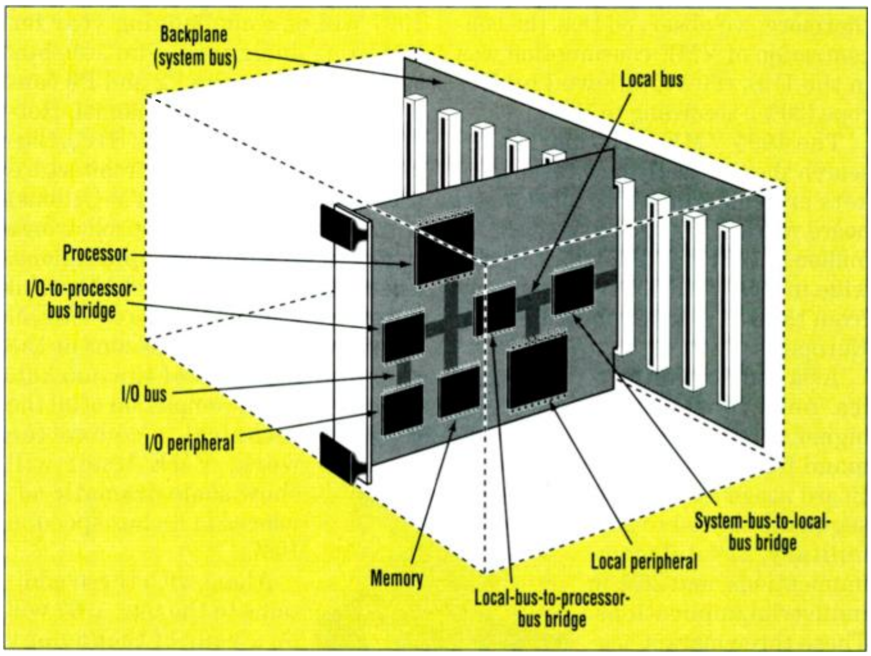
Whether you design routers, printers, photocopiers, or control cards for PABXs (private automated branch exchange) or switches, odds are that you are already designing with PCI or are thinking about it for your next product. Originally intended for the PC industry, PCI is winning broad market acceptance in various industrial and embedded-systems applications. One reason is that most new high-speed serial I/O controllers, like fast Ethernet, ATM, or ISDN, are PCI-based. In addition, because these components are targeted for the PC industry, designers of high-performance embedded systems can leverage component volumes from the PC industry and lower the cost of their products.

Beyond the economies of scale that accompany PCI, there are some valid architectural benefits. It's designed to support self-configuration (plug and play), which permits designers to mix and match PCI devices from various vendors (in theory). The bandwidth of PCI is attractive; at 32 bits and 33 MHz, the bus provides a theoretical maximum of 132 MBytes/s. You can expect to see 64-bit PCI buses appearing in embedded systems in the next year or two, effectively doubling the available bandwidth.

For both the cost and architectural advantages of PCI, designers of embedded systems are contemplating using PCI. To a large extent, these systems are still based on the Motorola 68000 microprocessor. For example, within the PABX market, the 680x0 architecture is the traditional favorite. This market is typified by long product life cycles, conservative design initiatives, and a high level of processor loyalty. Although new designs will attempt to use PCI-based I/O components, you can expect that the processor will be a 68030 or 68040. Alternatively, although the Internetworking market (hubs, routers, etc.) is faster paced, more nimble, and has less processor loyalty than the switching market, the 68K architecture is still commonly used. A particularly successful 68K component in this market is the 68360 (a 68030 core surrounded by an impressive array of communications peripherals). Designers in both of these markets face the same problem: How do I bridge PCI, an Intel-based protocol, to a Motorola-style 68K bus?

This article identifies a few of the issues that arise when you try to bridge these two bus types. At the level of protocol translation, these issues include cycle and endian mapping. At a system level, there are issues that arise from PCI's relative role in the system. Based on this system architecture, different approaches can be taken to locate the processor's boot code. Before tackling these issues, it would be beneficial to cover some bus basics in embedded systems.

Let's establish some terms for buses at different levels of the embedded system bus hierarchy. A typical embedded system contains an I/O bus specifically for access to I/O ports terminating on the card *(Fig. 1)*. There's the processor bus that is typically dedicated to processor-to-memory transfers, and the local bus that connects various peripheral devices or daughtercards. In addition, there could be a system bus (often passive backplane)



1. A typical embedded system contains many devices, and almost as many buses to connect to those devices. For communications, there must be a bridge between each of the buses.

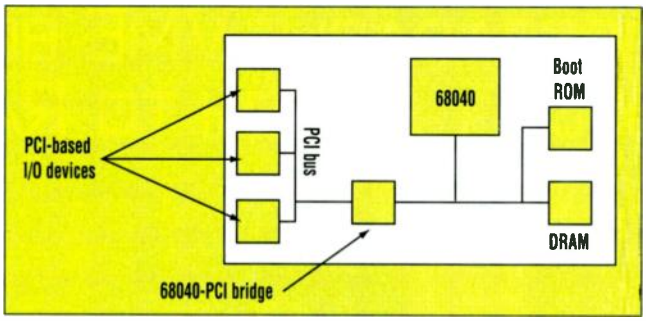
that connects multiple boards in a rugged card cage. Bus bridges are found at the junctures of the various buses—system-to-local, local-to-I/O, local-to-processor, and processor-to-I/O.

Lower-end embedded systems may incorporate just a processor bus and I/O bus for a simple single-board system. Middle-of-the-road systems often include only the buses discussed previously. For example, on a router motherboard there may be a processor bus with a separate local bus servicing network expansion cards. High-end embedded systems occupying a card cage will incorporate all of the buses discussed previously.

PCI is appearing in all of the system types described above, playing a role in each of the levels of the bus hierarchy. In simple single-board systems, PCI is the I/O bus that connects to communications chip sets. Such a system might be a laser-printer controller card where the PCI bus connects to Ethernet, SCSI, and other PCI-based I/O controllers. It's also used as a local bus for a system's motherboard with PCI-card expansion slots. Quite often, the processor in these embedded systems is 68K-based.

Because of its low cost and high performance, PCI is displacing existing I/O buses like SBus, with the most frequent casualty being the proprietary bus *(Fig. 2)*. In many designs, the PCI-based devices will have DMAs designed to burst into and out of system memory. This requires that the 68K/PCI bridge support these types of transfers through its PCI target interface. With a 68040 CPU, there's bursting on the processor bus to support the bandwidth requirements of the DMA engines on the PCI bus.

The other implementation of PCI in an embedded system is as the system bus *(Fig. 3)*. In these systems, PCI often displaces an existing proprietary bus, or perhaps the ISA bus in an embedded PC environment. The barrier to this type of re-architecting is often considerably higher than in the standard I/O bus role, and usually is coupled with a completely new product design. For example, introducing PCI as an I/O bus on an existing VMEbus board could be considered an incremental redesign of the VME board. However, completely converting a router's system bus to PCI probably represents a major new product family introduction.



2. The PCI bus can be employed as an I/O bus in a 68K-based system, connecting peripherals to the host processor (through a bridge).

There are some noteworthy aspects of the embedded system's PCI-based system bus. On the processor side, the application employs a 68040 as the host processor and a 68360 as a local peripheral. Despite the 68360's 68040-like companion-mode option, it's likely that the 68K-PCI bridge will be required to communicate to the two different processor buses. On the PCI side, the PCI peripherals will probably have DMA functionality and will expect to burst data through the bridge. Note also that there is a limit of about three cards on the PCI bus. A PCI-PCI bridge would be required to allow for more.

PCI-based addresses are mapped functionally into three different spaces: Memory, I/O, and configuration. However, on a 68K bus, address spaces are identified as Supervisor or User, combined with Program or Data. There are also other 68K address spaces that are specific to the 68K. To guarantee that a particular PCI address space can be accessed by the 68K processor, the type of PCI access must be encoded in the 68K transaction. The PCI-68K bridge can solve this problem by providing configurable PCI attributes that are used when the bridge decodes a 68K transaction destined for the PCI bus.

For example, if a PCI-PCI bridge was used in the system bus of the previous example to increase the number of PCI expansion cards, the 68040 would need to generate "type 0" configuration cycles on the primary PCI bus to configure the devices there. The processor would also need to generate "type 1" configuration cycles on the primary PCI bus. This cycle type is translated by the PCI-PCI bridge to type 0 configuration cycles on the secondary PCI bus, allowing those devices to be initialized. These potential PCI transaction types would need to be configurable options in the PCI-68K bridge.

In a similar way, the PCI-68K bus must allow for PCI transactions to be mapped to 68K address space. For example, when the PCI bus is employed as an I/O bus, the I/O devices will likely need to burst data directly into memory on the 68040 bus. The address type on the 68K bus is encoded using special-function code lines, which in this case would encode user-data access. The PCI-68K bridge would provide a programmable option where specific PCI accesses result in the generation of set function codes.

Beyond the problem of dissimilar address spaces, the PCI bus and 68K processors have an even more fundamental difference stemming from their separate evolutionary histories. PCI was born in the Intel world, making it little-endian, while the Motorola processors used big-endian.

In a big-endian system, the most significant byte is located at the lowest address in memory. When the data is moved to the data bus, the least significant byte is moved to the lowest byte lane, and the most significant byte is moved to the highest byte lane.

In a little-endian system, the most significant byte is located at the highest address location. When data is moved to the data bus, the least significant byte is moved to the lowest byte lane, and the most significant byte is moved to the highest byte lane. It's important in the PCI bridge to provide flexibility in how endian systems are mapped across the interface.

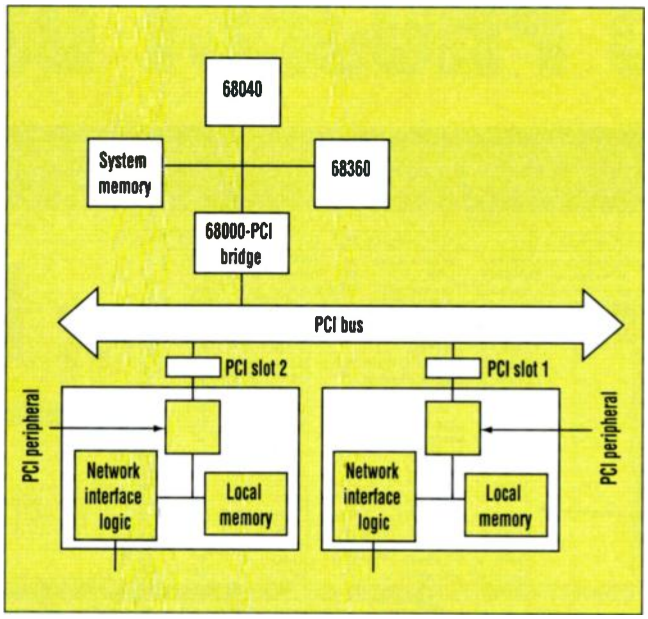
Many, if not all, host-bus adapters for the PCI environment will expect their descriptor blocks to be stored in main memory in little-endian format. This means that the PCI-68K bridge must supply a flexible endian mapping scheme to allow for PCI adapter-control information to be stored in 68K memory.

There are two approaches to endian

mapping—address invariance and data invariance. With address invariance, the addressing of the bytes in memory is preserved. By performing byte-lane swapping, the bytes appear in the same address but their relative significance is not preserved. This is fine for text information but scrambles operands.

Data invariance preserves the relative byte significance, but translates the byte addressing. With data invariance, byte 0 is still the most significant byte in the data structure but is now located at address 03 in memory rather than address 00.

By enforcing certain constraints on the system, it's possible to implement both options in the PCI-68K bridge. By assuming that all data structures are 32-bit integers, the bridge could be powered up in either of these mapping modes. In address-invariant mode, byte lanes would be swapped (independent of the data-path width) assuming that the bytes are part of a 32-bit word. In data-invariant mode, the byte lanes would be passed straight through, assuming that the bytes are again part of a 32-bit word.



3. When employed as a system bus, PCI can displace an existing proprietary bus or, in an embedded PC environment, the ISA bus.

Data transfer between the PCI and 68K buses can occur in two different ways. There's a buffered path, where burst transactions can be loaded into a FIFO and relayed to the destination bus. The PCI-68K bridge must allow for this by providing buffering in both directions. This type of posted or prefetched transfer is best for bulk data transfers, but has inherently higher latency and is problematic for transactions requiring low fault tolerance. For low-bandwidth, low-latency transactions that require sure data acknowledgment from the destination bus, a common approach is atomic or coupled transactions. In this scheme, the source bus is held with wait states while the transaction completes on the destination bus. However, there's a fundamental problem with this approach which results in livelock.

Livelock can occur in a system in which the PCI is the system bus and there are two PCI add-on bus bridges that perform coupled cycles. If the CPU on each of the two different add-on buses tries to access the other bridge in a coupled fashion at about the same time, the bridges accept the cycles and lock up their add-on bus by inserting wait states on the source bus until the transaction completes on the PCI bus. When each bridge attempts to access the other, they are retried on the PCI bus because their add-on bus is unavailable. The retries will continue indefinitely on the PCI bus in this scenario.

To prevent this occurrence, the PCI-68K bridge must perform PCI-like delayed transactions on the processor bus. For example, when the 68040 performs a delayed read or write to the PCI-68K bridge, the address and data information from the processor bus is latched by the bridge even though the transaction is actually retried. The PCI-68K bridge masters the PCI bus and completes the read or write transaction. When the 68040 returns after the retry and the PCI transaction is complete, the 68040 transaction is terminated normally. This meets the requirement of low latency as well as ensuring that the processor only receives data acknowledgment as a result of successful cycle completion on the destination bus.

As discussed earlier, lower end embedded systems may incorporate just processor and I/O buses for a simple-single board system. In such a system, PCI is employed as the I/O bus specifically selected to connect to serial-interface chip sets. In this case, the 68040 acts as the local host and configures the PCI devices at power up. This dictates that the PCI-68K bridge be configurable from the processor bus, allowing the 68040 to initialize the bridge before the PCI devices.

There also are different approaches for booting the processor itself, dictated by the system's architecture. One way is to locate all of the boot code right on the 68K bus in ROM. In this case, when the 68040 comes out of reset, it locates the boot vector and loads the initialization code. In contrast to the previous example, the PCI/68K bridge must remain in reset while the processor loads its boot code.

Alternatively, the 68K processor may receive its boot code from the PCI bus. In the case of the PC server adapter card, the card may come with a diskette containing the board's application software. The system host loads the boot code from the diskette to the embedded 68K processor through the PCI-68K bridge. Before this occurs , the application software for the expansion card will likely run drivers to configure the parameters of the bridge's PCI target images. These parameters include such settings as translation offsets, port width of the slaves on the 68K bus, and address type on the 68K bus. Once configured, the application software can download the 68040 or 68360 boot code.

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Richard O'Connor, Tundra's Director of Market and Business Development, holds an MBA from Ottawa University, Ottawa, Canada, and a BSEE from Algonquin College, Ottawa, Canada.

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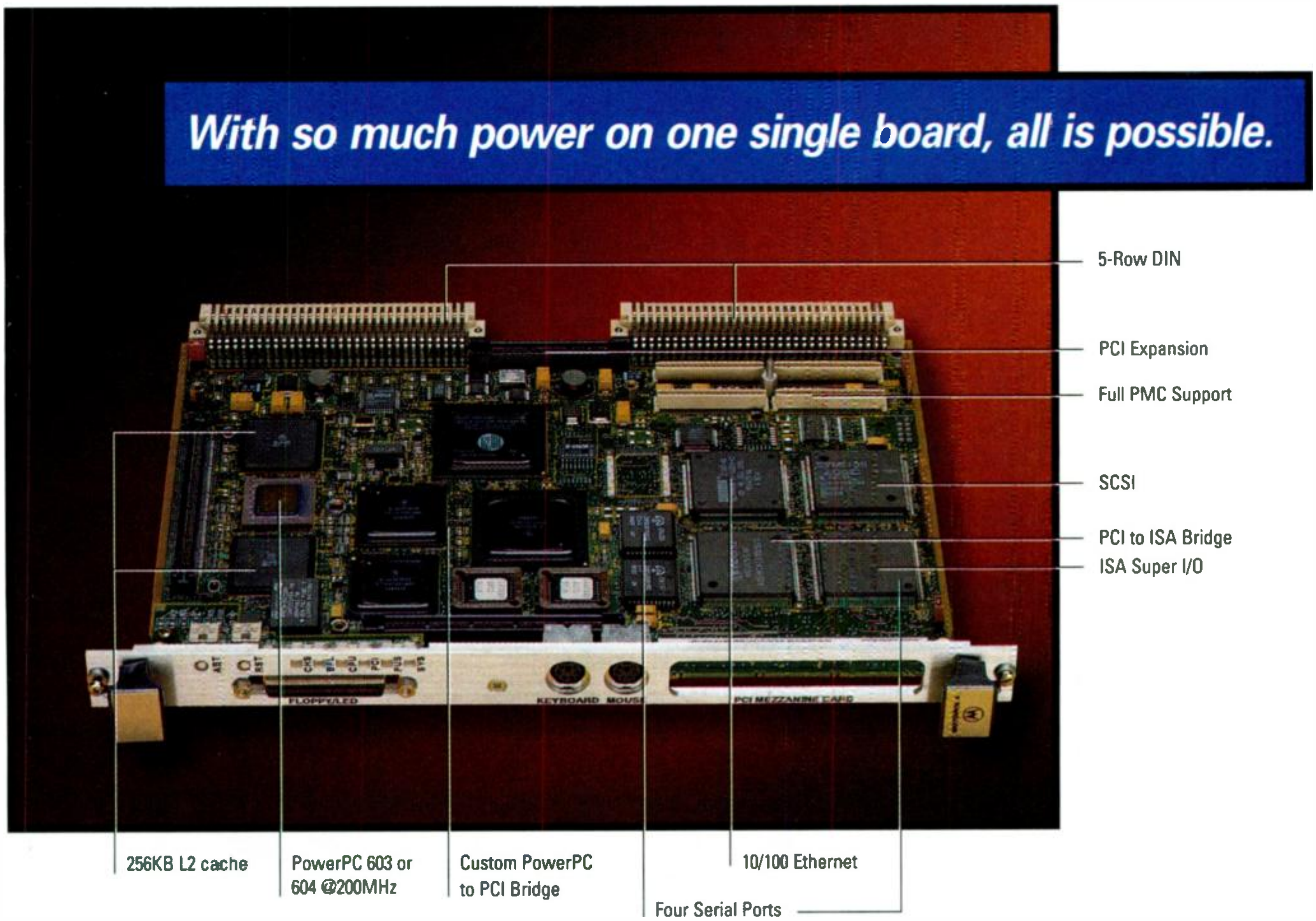

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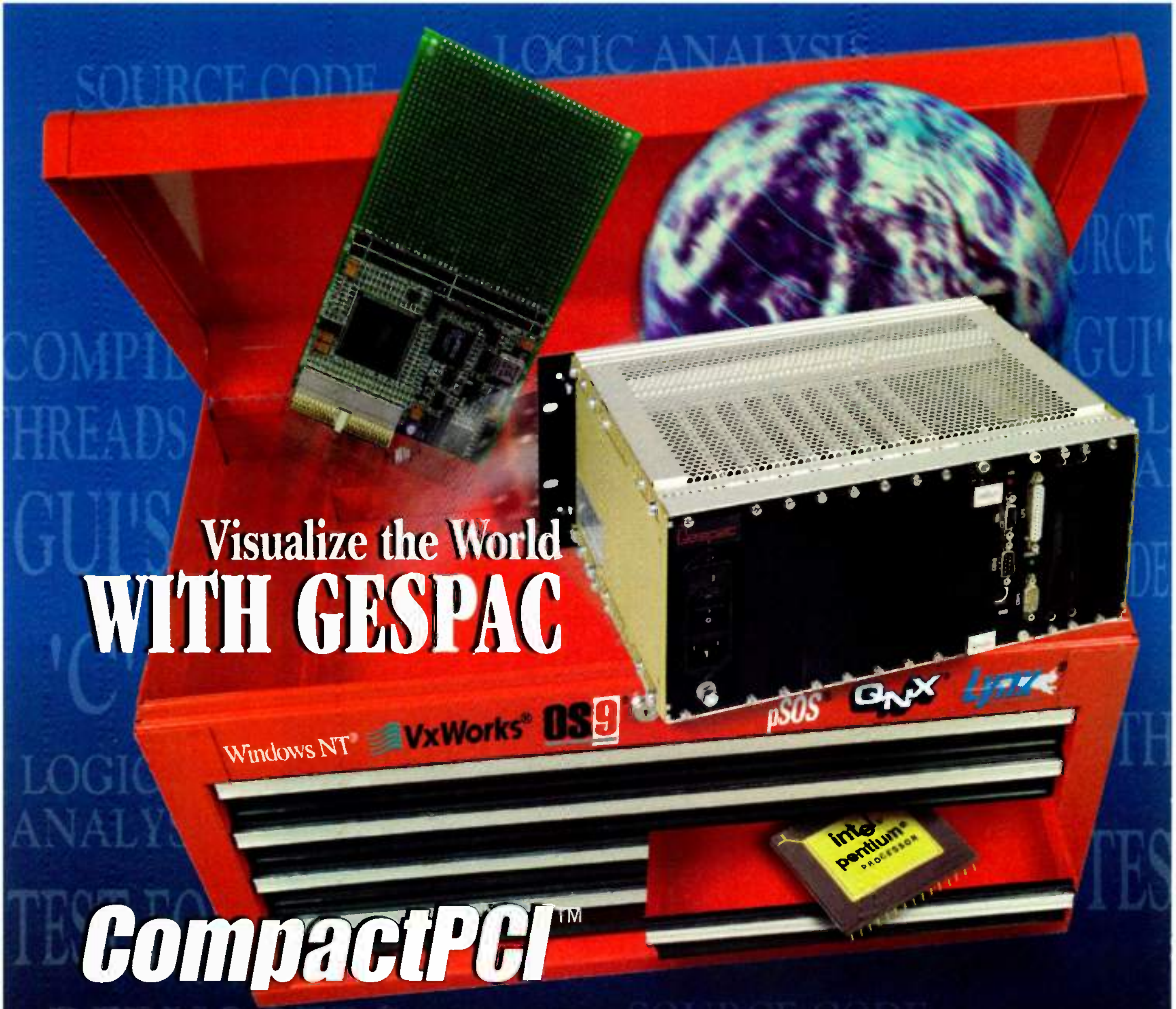

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Decoupling Opens Bottlenecks In VME64-Based DSP Systems

Host And Secondary Buses That Operate Independently Clear Roadblocks To Maximum Throughput.

GRANT BRYDON, Spectrum Signal Processing, 8525 Baxter Pl., Burnaby, BC, Canada V5A 4V7; (604) 421-5422.

High-speed data transfer is not just a desirable commodity for VME64-based digital signal processing systems— it's essential. Without the ability to communicate information freely from VME64 and dedicated secondary buses, these real-time systems can't accomplish their tasks. Among the methods used to reduce or eliminate data bottlenecks, decoupling the VME64 bus from secondary buses has the greatest potential for allowing throughput to reach its 80 Mbyte/s and future higher-speed transfers.

Data transfer bottlenecks are most commonly encountered (and most troublesome) in two types of signal-processing environments. In the first, data is transferred in large blocks, which consumes large amounts of bandwidth. If the I/O bandwidth approaches VME64 or local-bus bandwidth, processing slows or stops during I/O transfers.

In the second environment, device and circuit latencies (the time between initiating a request for data and the beginning of the actual data transfer) slow the data transfer across the VME64 bus to the point at which the data is useless by the time it arrives at its intended destination.

In non-real-time systems, overall system performance can still be maintained even though data doesn't arrive in the most timely manner. However, in real-time systems, bottlenecks can have catastrophic effects.

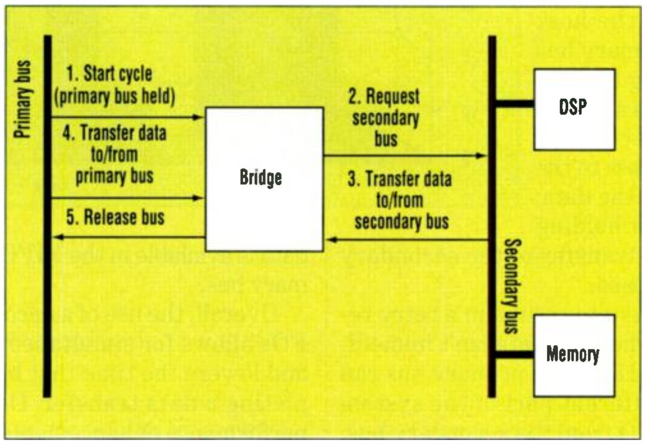
Designers have implemented several solutions to raise VME64 throughput nearer to its theoretical maximum by developing more sophisticated bus-interface logic. This method has the advantage of not requiring any modifications or additions to the existing bus standard.

Another way to circumvent data bottlenecks is to create an auxiliary bus to reduce the load on the primary bus *(Fig. 1)*. Using a standard bus protocol for this auxiliary bus has the greatest potential for interoperability among boards and subsystems. It's also comparatively easier to implement, places less demand on the system designer, and requires far less time than creating a proprietary bus. A general disadvantage of creating an auxiliary bus is that it can only interface with systems that have also implemented the auxiliary bus.

A third method is to develop a proprietary bus. If this route is chosen, the benefits must vastly outweigh the potential risk of making it difficult for users to combine boards from different vendors. It also may prove difficult to entice users and other companies to adopt an unproven bus standard designed by a single company. In addition, designing a new bus standard is a major undertaking, requiring a large investment in engineering time, resources and money.

Not surprisingly, the first approach of using more sophisticated bus interface logic is often chosen to provide seamless compatibility with existing products while increasing system performance. Bus decoupling is a primary method of increasing bus performance without drastically altering the bus or the protocol.

Decoupling the primary bus, such as VME64, from the secondary bus dedicated to serving high-speed DSP functions can reap large throughput gains. It's a good choice in DSP environments where large amounts of data must be transferred quickly and lengthy response times are not acceptable. The procedure in effect hides VME64 latencies and reduces or eliminates the need for the system to periodically stop processing and transferring data because its intended transmission path is not ready to receive it. These delays account for the majority of the data-transfer bottlenecks encountered in real-time signal-processing systems *(see "Demystifying Decoupling," p. 148)*.



1. In a coupled system, the data is transferred from the primary bus to the secondary bus, with the primary bus being held during this time.

The effectiveness of decoupling lies in the ability to free both primary and secondary buses to perform transactions simultaneously. In a coupled system, one bus would simply sit and wait for the other to become available. If the decoupled system is designed properly, data flow appears nearly continuous, without the stops and starts that characterize a coupled system.

Decoupling can be performed by a single chip, such as the SCV64 VME64-to-host interface or the Universe VME64-to-PCI bridge, both from Tundra Semiconductor Corp., Kanata, Ontario. The term "bridge" is used as these chips link two different interface buses in one IC. These bridges operate by monitoring primary buses (such as VME64) and secondary buses (such as host or PCI) and rapidly making transfer and arbitration decisions for the primary or secondary busses.

In the decoupling write scheme, the host processor sends data on the VME64 bus to the bridge that links the VME64 bus to the host or to the PCI or other secondary bus. The data is immediately placed in a FIFO buffer that queues up all the received data *(Fig. 2)*. The VME64 bus indicates that the last piece of data has been sent, and the FIFO tells the host processor on VME64 that it has been received, even though it still resides in the FIFO. The bridge then requests access to the secondary bus, and transfers the data to the DSP.

VME64 and host processor buses are then free to conduct transactions with other parts of the system. During a subsequent bus cycle, the FIFO transmits all the data to the recipient, which is either another bus or the DSPs. This procedure in effect hides the arbitration time for the secondary bus from the VME64 bus.

Several factors affect this scenario, the most obvious being FIFO depth (i.e., the amount of data that the FIFO can receive before it must dump its contents to the secondary bus). The greater the FIFO depth, the more data that can be transferred, the larger the data blocks, and the higher the throughput.

Peak throughput is achieved at a certain FIFO depth, beyond which performance increases trail off because the maximum throughput of the bus has been reached. If the FIFO is too shallow, the primary bus fills up the FIFO and is notified to stop sending or held off until the FIFO can dump data to the secondary bus. This in effect negates the major advantage of decoupling, because arbitration delays once again appear. However, if the FIFO is deep enough to accept all the transferred data at one time, or the FIFO begins emptying while it is also being filled, this blocking of the first bus can be limited.

Multiple data transfers can be made

Demystifying Decoupling

In a coupled system, the data is transferred across the primary bus to the secondary bus. The primary bus is held during this time. Once access to the secondary bus is granted, the data is transferred to the intended destination; then the secondary and VME buses are released. The entire process can take several hundred nanoseconds because of arbitration delays encountered in the waiting time, first for bus access, then for the secondary bus on the addressed target. In both reads and writes, the coupled operation locks both buses for the entire transfer.

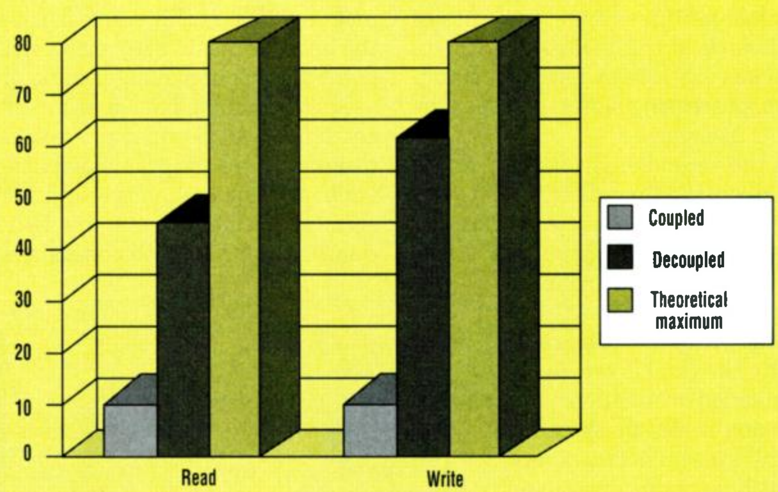
In a decoupled system, the host transfers data across the primary bus and into the FIFO, releasing the primary bus when it has received all of the data in the FIFO. The decoupled bridge chip then requests access to the secondary bus and transfers the data, completing the cycle. By not holding the primary bus during the transfer to the secondary bus, data throughput is increased.

A read in the decoupled system results in a retry response to the primary bus when the data isn't immediately available in a bridge FIFO. The primary bus can then perform a cycle to a different part of the system while the bridge fills its FIFO from the secondary bus. When the primary bus returns with the read cycle, the data is available in the FIFO and is transferred to the primary bus.

Overall, the use of a decoupling bridge containing FIFOs allows for simultaneous bus transactions to occur and lowers the time that both buses are locked in completing a data transfer. Decoupling offers significant performance enhancements in terms of much faster system throughputs *(see the figure)*.

Throughput comparison: Coupled vs. decoupled (32-bit VME to 32-bit PCI)

Theoretical maximum:	80 Mbytes/s
Coupled read:	10.3 Mbytes/s
Decoupled read:	45 Mbytes/s (64-byte block)
Coupled write:	10.3 Mbytes/s
Decoupled write:	61.5 Mbytes/s



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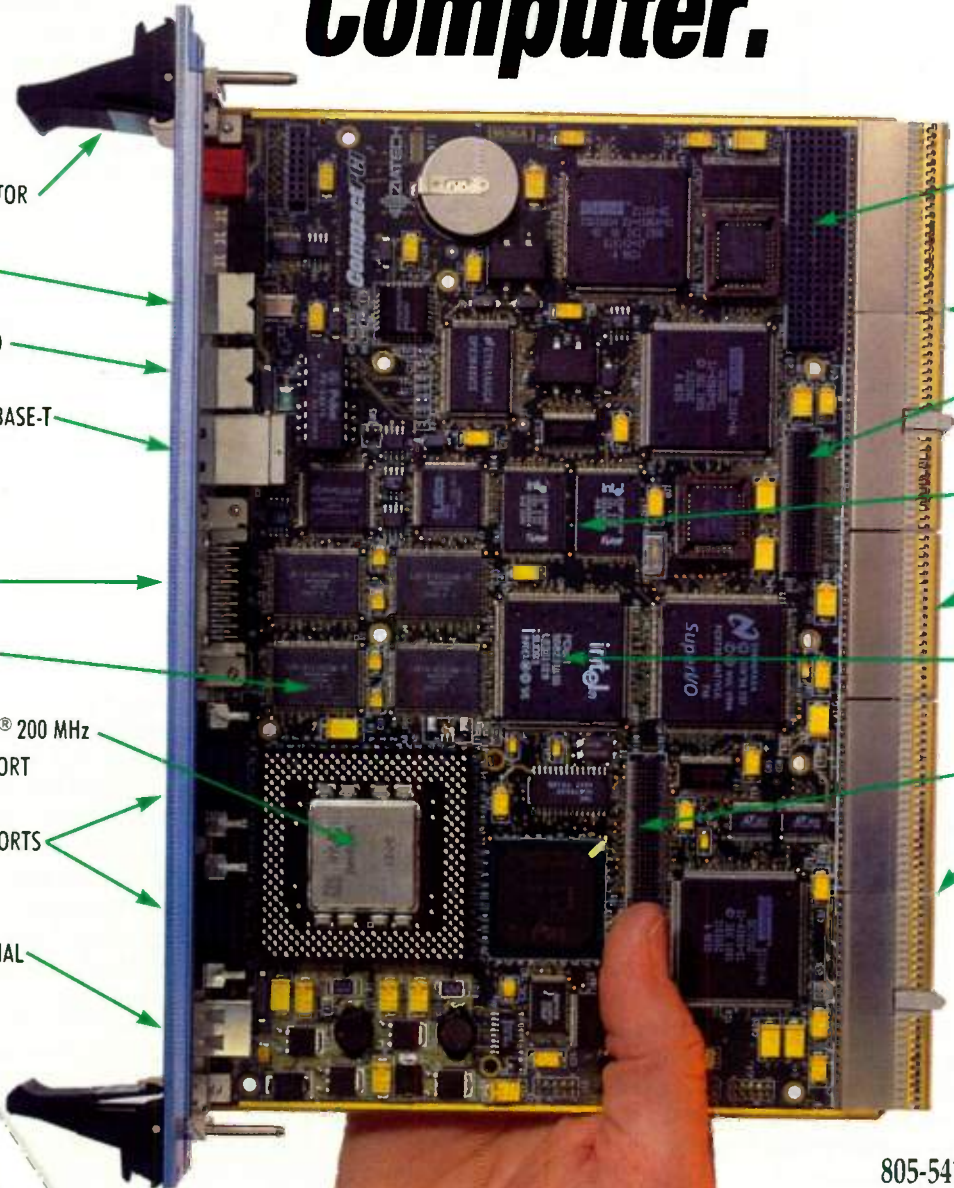

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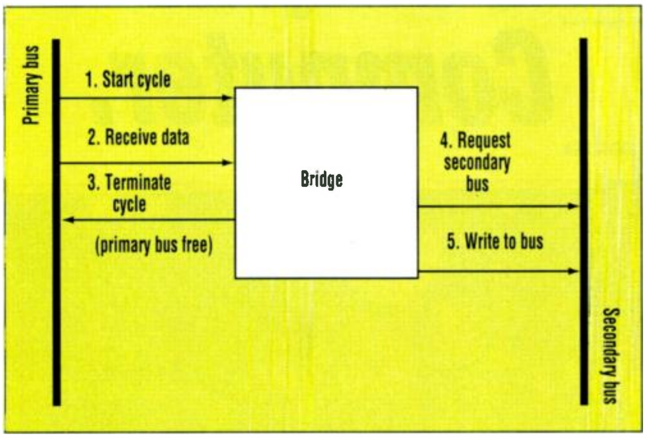
Pentium is a registered trademark of Intel Corporation. CompactPCI is a trademark of the PCI Industrial Computer Manufacturers Group into the FIFO, depending on the device chosen and how the circuit is designed. Multiple transfer capability allows for the VME64 bus to send, for example, five or six transfers over the VME64 bus to the FIFO even before the previous data leaves the FIFO for the secondary bus.

Read transactions are more complicated than write transactions because the data must pass back through the entire transmission path. One of the situations encountered in decoupled systems is that during a read, a FIFO will have no data to be read, and will thus inform the requesting device (most likely the host) that it is not ready and the requester should retry the request to allow the secondary bus to fetch the data. This retry function is a characteristic of the PCI bus. The VME64 bus generally doesn't use a retry function and thus loses some of the decoupling on the initial cycle. The FIFO filling allows the VME64 bus to operate in a decoupled mode on subsequent cycles.



2. In a decoupled system, the host transfers data across the primary bus and into the FIFO, releasing the primary bus when the FIFO contains all the necessary data. The bridge chip then requests access to the secondary bus and transfers the data, completing the cycle.

The bridge accepts the address, then requests the host to return later, while arbitrating and passing the address to the secondary bus. It will then fill up its FIFO with a transfer block. When the requester returns, it feeds the data onto the bus.

If the decoupling system has a high level of sophistication, it can monitor the FIFO, and when it begins to empty, periodically add another transfer block to the FIFO. Another approach is to let the FIFO empty, and request the host to retry a few clock cycles later to get the next block, and then refill the FIFO. By judicial choice of block sizes in maximizing the saturation of the FIFO, it's possible to make the transfer process appear to be a continuous data stream. Success in implementing this approach depends on the ratio of how long the host spends waiting for data to the time it spends transferring it from the FIFO.

One of the quirks encountered in a decoupled system during reads is some unnecessary data transfer into the FIFOs. Because the FIFO is being filled without knowledge of how much data is being transferred, data remains in the FIFO until the next read. When the system determines that the FIFO doesn't have the proper data, it purges its contents. To circumvent this, a DMA controller can be employed which is preprogrammed with the data stream 's length. This allows the optimized filling of the FIFO and delivery of the exact amount of data when requested.

Being in the same interface chip as both the primary and secondary bus interfaces, the DMA controller can monitor the status of both buses and the FIFO. This allows the DMA controller to optimally use the FIFOs and perform data transfers. In addition, the transfers can be set up so that rather than performing a more complicated (and often lower throughput) read transaction, a write transaction can be performed.

Decoupling FIFOs also allows for transfers to be performed simultaneously to both buses from the bus bridge. Once the FIFOs are filled, the read FIFO sends data across the bus, and any data still in the write FIFO can be sent over the secondary bus to the DSP. For example, as the outgoing decoupling FIFO writes to the VME64 bus, the incoming decoupling FIFO can be emptied to the secondary bus. Similarly, the DSP can fill the outgoing FIFO while the VME64 bus can fill an incoming FIFO. When the bridge sees a FIFO with a data transfer, it then requests one or both buses and begins the data transfers to the final destination.

Because all data is queued in the FIFOs, transfers smoothly follow each other. When accessing the secondary bus, the decoupling bridge immediately begins data transfers, without needing to tell the DSP that it is ready to conduct the transfer. Also, data in the FIFO is never more than a few clock cycles away from delivering data to the bus. All FIFOs are in a ready state while the buses are conducting other transactions.

Decoupling provides a way to remove the barriers that prevent real-time signal-processing systems from achieving their maximum throughput. To be most effective, it requires a careful choice of devices to optimally synchronize data-transfer operations on the bus.

However, bridge chips are available to make the transition between the VME64 host processor bus and secondary buses, such as PCI. Any of these decoupling chips, when properly designed into a system, can greatly improve the overall performance.

The V8 Octal Sharc Board from Spectrum Signal Processing contains eight Analog Devices Sharc DSPs and employs two decoupling bridges to provide high speed throughput between the DSPs and the VME64 bus. The first decoupling bridge is implemented with the Universe VME64-to-PCI bridge to interface between the VME bus and the on-board PCI bus. The PCI bus then connects to the DSPs through a second decoupling bridge. The dual bridges provide the high-speed decoupled transfers between the DSPs and the VME64 bus. High-speed decoupled transfers between a PMC site and the DSPs occur over the second bridge.

Grant Brydon is Technical Lead at Spectrum Signal Processing. He holds a Bachelor of Applied Science in Electrical Engineering from Simon Fraser University, Burnaby, B.C., Canada.

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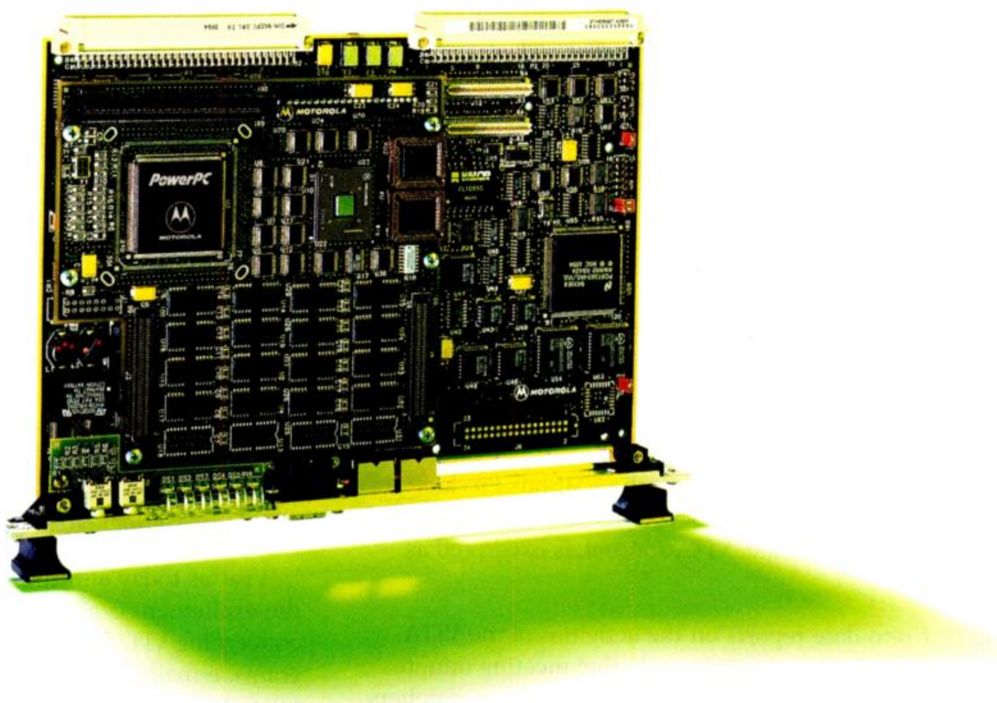

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Conference And Exhibition Showcases New Developments In Design Methods, Standards, And Technologies.

Tom Williams

As embedded systems grow beyond industrial applications, and increasingly affect the lives of consumers, designers more often are faced with the problem of making complex devices easier to use. Ironically, this challenge requires an ever-increasing amount of underlying complexity. Items such as intelligent phones, set-top boxes, and even the lowly remote control for TV and stereo need to provide more features and capabilities, but in ways that non-technical users can intuitively understand. Add to that, the need to make devices as inexpensive as possible, and you've given engineers an almost endless series of challenges.

There has been no slowdown in the high-end industrial use of embedded systems. Instrumentation and process control, and avionics and spacecraft control, are increasing in their complexity and the need for dataexchanges. Automobiles are a classic example of the surge in applications of embedded systems. An estimated 50% of the cost of a modern automobile is found in its electronic systems such as engine control, emission control, ABS brakes, air bags, climate control, and cruise control.

Embedded systems are facing the demands of connectivity and communication, not just over small, closed networks, such as those found in automobiles, but also over the Internet and World Wide Web. The concept of the Internet appliance requires that embedded-systems engineers face issues of user-interface design, communications protocols, and media that can connect and communicate at all levels. Industrial plants, with their networked control nodes and remote sensors and instruments, also are under growing pressure to be able to share their data with users worldwide.

All these subjects are ripe for discussion at the upcoming Embedded Systems Conference East, which will be held March 10-12 at Boston's Hynes Convention Center. The conference program comprises over 70 classes and tutorials to help engineers, designers, and managers keep abreast of developments in hardware and software for embedded applications. Not surprisingly, almost two-thirds of the sessions are devoted to software issues, such as languages like C, C++, and Java, and their application to embedded design. In addition, design and development tools, and debugging issues form a large part of the fare.

Tutorials abound

The conference starts off with six all-day tutorials, four of which deal directly with software topics. The "Real-Time Object-Oriented Modeling" tutorial will look at managing the rising complexity of real-time software, along with maintaining high performance. The tutorial will use the Real-Time Object-Oriented Modeling (ROOM) method to show how modeling techniques can be used to create more reliable real-time software. The techniques include capturing high-level architectures, implementing high-level state machine behavior, and creating reusable components.

The topics of Java, C, and C++ for embedded systems are ongoing themes throughout the conference, along with object-oriented technology in general. A tutorial, "Stepping up to C++" aims at helping C programmers move to the object-oriented language that evolved from C. It will explain what distinguishes C++ from C, and how programmers can take advantage of features such as classes, derived classes, constructors, destructors, and virtual functions.

Continuing the evolutionary spirit, the tutorial titled "Java for C++ Programmers" will start with the similarities between Java and C++, then move to the distinguishing features of Java. The course will cover Java inheritance, polymorphism, the I/O system, container classes, creating threads, applets, and windows and network programming.

"Software Estimation and Scheduling" looks at the areas where a great many development efforts fail: estimating the effort in people and money, and the scheduling of software projects. The session will look at the use of Gantt and PERT charts, adjusting resources, and a number of different methods for tracking team progress.

The challenge of hardware/software codesign and verification is tackled in "The 'Magic' of Building Hardware/Software Systems." The tutorial reviews the use of in-circuit emulators, hardware prototypes, microprocessor emulators, software simulators, instruction-set simulators, and system simulation, among other approaches. The tutorial will use real-life examples to analyze the alternatives available to hardware and software engineers and managers.

Rounding out the offering of tutorials will be "Usability Engineering for Embedded Systems." This session addresses the issue of usage-centered design, and is particularly relevant to the design of consumer products, as well as industrial applications. Jacobson's use-case model for object-oriented design is extended to cover user-interface design and usability engineering. The dynamics of user interaction with the system by employing a model-driven approach is examined, as well as the overall organization of the system.

The first day of the conference will be capped with a keynote address by Harel Kodesh, the general manager of Microsoft's consumer appliance group. Reflecting the growing importance of the consumer sector for embedded systems, Kodesh's talk will be titled, "WIN32: The New Paradigm for Embedded System Development." The address will point out that a number of WIN32-enabled operating systems exist which offer the benefits of proprietary RTOSs, but with the added compatibility of the WIN32 API. Kodesh predicts that designers will leverage this compatibility to use languages such as Visual Basic and Visual C++ to create reusable objects for embedded applications, as well as take advantage of existing modules.

The range of courses offered at this year's conference addresses programming language topics as they affect the design of embedded systems, software development methodologies, debugging tools, real-time operating systems, guidelines for selecting hardware, communications and networking issues, use of flash memory, bus standards, and new developments in embedded processors.

While the Java language is strongly supported by a number of classes, C and C++ also are well-represented. "Commercial Support for C++" examines a subset of the draft C++ standard that was developed by the Embedded C++ Technical Committee. The embedded-C++ subset is designed to better suit embedded applications. The session describes the compilers, libraries, and tools available, and looks at where the embedded-C++ effort is going. Another session, "How to Evaluate C++ as a Language for Embedded Programming" looks at real and imagined problems in using C++ for embedded applications. Issues of the language's complexity, potential for errors, and hidden costs are examined with the aim of giving the designer the background to decide if C++ is appropriate for his design.

Getting down to the nitty-gritty, "Manipulating Hardware in C and C++" looks at the specific mechanisms of C and C++ that support direct hardware manipulation, and their limitations. In addition to presenting the standard techniques, the class will explore techniques for packaging hardware interfaces as abstractions, and for placing data in ROM. In "Advanced Device Drivers" attendees will learn about working with device drivers for real-time operating systems and under complex I/O environments like Streams. The goal is to develop device drivers that are more transportable and robust.

Since embedded systems are quite cost sensitive, optimizing speed and memory requirements is a high priority. "Reducing Run-Time Overhead in C++ Programming" will look at the ways C++ can fine tune cost and performance without having to reject some of its more attractive features. Techniques include reducing the cost of member function calls, writing special purpose memory allocators, and avoiding compiler-generated temporary objects.

A cupful of Java

For the Java enthusiasts, there is "Embedded Processor Core for Executing Java Byte Codes," which will discuss the design and verification methods for developing an embedded core to run Java byte codes. Discussion will include the architecture of the core and the tools used in the design, as well as the coverage analysis technique used. "Java in Embedded Systems" will look at the enthusiasm generated for Java's potential in embedded systems, andit will point out some of the pitfalls, including some early experiences in trying to use Java in embedded applications. The class will focus on Java internals such as garbage collection versus Java's scheduling algorithm. In addition,the tutorial "Thread Support in the Java Language" will present the built-in multithreaded support of Java in comparison to its implementation in many RTOSs. The class will present the Java-thread object and move on to topics in synchronization and mutual exclusion mechanisms, as well as more complex structures.

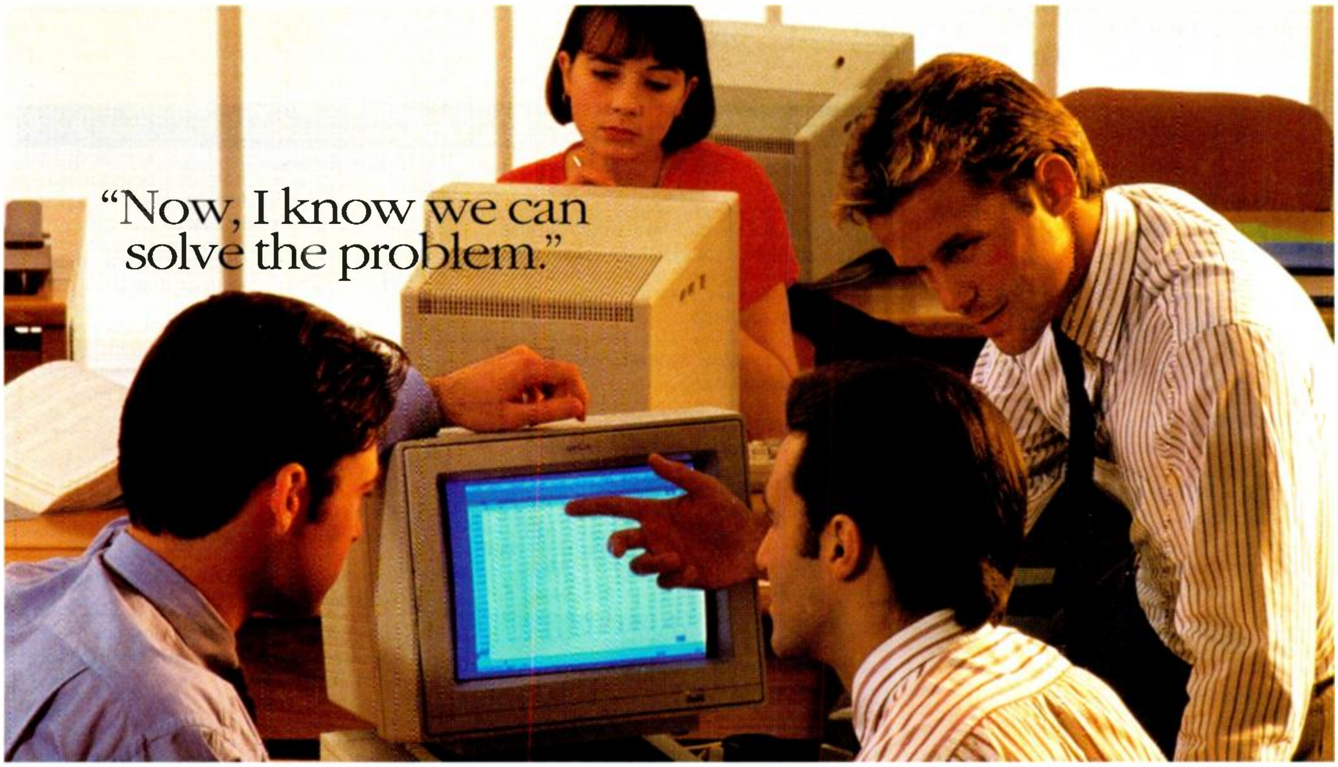
With systems becoming more cost sensitive, some functions done by specialized DSPs are migrating to 32-bit RISC CPUs for host signal processing (HSP). "Signal Processing with Embedded Coldfire Processors" will present fast algorithms for DSP on the Motorola Coldfire. Algorithms for discrete cosine transforms, fast Fourier transforms, and FIT filters will be presented along with a discussion of the new multiply accumulate (MAC) engine. "Image Processing in an Embedded PowerPC Environment" looks at trade-offs in processing power and memory cost needed to perform certain compute-intensive applications on a 32-bit host RISC processor. The class will discuss issues of such operations as convolutions, matrix manipulation, and FIR filtering.

Given the special needs of consumer products, "Microprocessors for Consumer Electronics, PDAs, and Communications" is aimed at helping the designer sort out the choices of really powerful CPUs used in toys, games, PDAs, and other devices that have extremely high computing requirements. An examination of successful chips in this area will point toward features to look for when designing new systems. Some lesser-known companies with unusual architectures will emerge as the biggest suppliers in this arena.

"Building Software for Appliances" will continue the consumer theme in describing how intelligent appliances such as set-top boxes, cellular phones, and car navigation systems differ from traditional embedded systems. In addition to the unique demands of the software, alternatives for appropriate platforms for intelligent appliances will be examined.

"Portable Systems and System Software Issues" will look at dealing with the underlying complexity of portable systems including graphical user interfaces, communications infrastructures, and battery power management. The class will examine how to use a real-time operating system to address these problems.

Not only is there a growing interest in object-oriented technology, but also in high-level object-oriented modeling and design methodologies. A two-part class, "Unified Object-Oriented Methodology," will present the Unified Method, the result of the convergence of several object-oriented methodologies: the Booch, the Rumbaugh or OMT method, and the Jacobson method. The class will present each of these methods, compare them, and show how the Unified Method utilizes the strengths of all three in a flex-



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EMBEDDED SYSTEMS CONFERENCE EAST

Monday, 3/10 Tutorials

8:30am-5:30pm

101	Bran Selic: Real-Time Object-Oriented Modeling
102	Bruce Eckel: Java for C++ Programmers
103	Dan Saks: Stepping Up to C++
104	Bruce Douglass: Software Estimation and Scheduling
105	Geoff Bunza: The "Magic" of Building Hardware/Software Systems: Process, Co-design, Co-verification, Integration, and Experience On The Bleeding Edge Of Technology
106	Larry Constantine: Usability Engineering for Embedded Systems

Tuesday, 3/11 Classes

8:30am-10:00am

211	William Hohl: Signal Processing With ColdFire Embedded Processors
212	P.J. Plauger: Commercial Support for Embedded C++
213	Alan Amis: Remote Debug and Dynamic Deplyment of an Embedded System
214	David Finkelman: Using Microsoft TEST for Embedded System Testing
215	Pat Megowan: IrDA Infrared Communications, Part I
216	Bruce Douglass: Unified Object-Oriented Methodology, Part I
217	Jim Sibigtroth: Next Generation Background Debug
218	Steven Sidman and Brad Stewart: Design and Use of Voice Recognition in Embedded Systems

10:30am-12:00pm

221	Rajeev Raman: Image Processing in an Embedded PowerPC Environment
222	P.J. Plauger: Translating Java to C
223	Dak Saks: How to Evaluate C++ as a Language for Embedded Programming
224	Joe Pavlat: New Developments in Compact PCI
225	Pat Megowan: IrDA Infrared Communications, Part II
226	Bruce Douglass: Unified Object-Oriented Methodology, Part II
227	Shrenik Mehta: Embedded Processor Core for Executing Java Byte Codes
228	Greg Viot: Third Generation Fuzzy Processing
229	Dan Hildebrand: Adapting PC Technology for Set-Top Boxes

2:00pm-3:30pm

231	David Howard: Thread Support in the Java Language
232	Jean Labrosse: Inside Real-Time Kernels
233	Dan Saks: Manipulating Hardware in C and C++
234	Chaitanya Vaidya: The microSPARC-IIep: High Performance for Embedded Applications
235	Jack Crenshaw: Math for Programmers Who Hate Math, Part I
236	Bruce Douglass: State Machines and Statecharts, Part I
237	Kees van der Bent: A New Approach to System Requirements Modeling, Part I
238	Greg Viot and Jean-Pierre Lavandier: Migrating to the 68HC12 in C
239	Emil Hahn: FMEbus: Open Standard Multimedia Engine

4:00pm-5:30pm

241	David Howard: An Embedded Web Server as the User Interface for an Embedded System
242	Jean Labrosse: Designing with Real-Time Kernels
243	Dan Saks: Reducing Run-time Overhead in C++ Programs
244	Phil Auzas: Programming On-Board Flash Memory Devices via the JTAG Port of a JTAG Compliant Microprocessor
245	Jack Crenshaw: Math for Programmers Who Hate Math, Part II
246	Bruce Douglass: State Machines and Statecharts, Part II
247	Kees van der Bent: A New Approach to System Requirements Modeling, Part II
248	Jim Sibigtroth: Building CPU12 Instruction Sets Upon M68HC11
249	Al Schneider: Writing Efficient Code for Small Microcontrollers

Wednesday, 3/12 Classes

8:30am-10:00am

311	Jack Crenshaw: The Alphabet from S to Z
312	Steven Stolper: Embedded Systems on Mars: The Next Generation, Part I
313	Richard Hecht: The Application of Internet Technologies in High Performance Embedded Systems
314	Alfredo Romagosa: Multiprocessing Architectures for Embedded Systems
315	Larry Mittag: Multitasking Design and Implementation Issues in Embedded Systems
316	Ed Klein: RTOS Design - How Your Application Is Affected, Part I
317	Charles Melear: Control of Electromagnetic Radiation in Microcontroller Circuits
318	Garth Gullekson: Managing Object-Oriented Development with ROOM
319	Bill Gatliff: The How-Tos of Using Flash: Implementing Downloadable Firmware

10:30am-12:00pm

321	David Walsh: The Anatomy of a State-of-the-Art DSP System
322	Steven Stolper: Embedded Systems on Mars: The Next Generation, Part II
323	Paul Ward: Mediators in Object-Oriented Development
324	Douglas Arndt: Implementation Details of Real-Time Analysis, Part I
325	Bruce Douglass: Custom Embedded Communication Protocols
326	Ed Klein: RTOS Design - How Your Application Is Affected, Part II
327	John Schill: An Overview of the Controller Area Network (CAN) Protocol
328	Bran Selic: Automatic Code Generation Methods for Embedded Applications - Theory and Practice
329	Peter Dibble: Java in Embedded Systems

2:00pm-3:30pm

331	Padmini Kumar: Other Language Programming Techniques
332	Jim Turley: Microprocessors for Consumer Electronics, PDAs, and Communications
333	Paul Ward: Is Information Modeling an Appropriate Technique for Embedded Systems Development, Part I
334	Douglas Arndt: Implementation Details of Real-Time Analysis, Part II
335	Larry Mittag: Advanced Device Drivers
336	Jack Ganssle: The Fine Art of Prototyping
337	Richard Daniel: Embedded Ethernet
338	Phil Dreike and James McCoy: Intro to Co-Simulation of Software and Hardware
339	Peter Dibble: Building Software for Appliances

4:00pm-5:30pm

341	Padmini Kumar: C or C++ Embedded Programming Techniques
342	Jim Turley: Choosing an Embedded RISC
343	Paul Ward: Is Information Modeling an Appropriate Technique for Embedded Systems Development, Part II
344	Doug Thomae: Early Processor Loading Analysis for Processor Selection in Real-Time Embedded Systems
345	John Canosa: Understanding Universal Serial Bus (USB)
346	Brent Thompson: Portable Systems and System Software Issues
347	Stephen Devries: Software Design Issues for Digital Set-Top Box Applications
348	Sigeru Sasaki: Proposal for On-Chip Debug Resources for High-Speed Microcontrollers
349	Stan D'Souza: Using 8-bit Microcontrollers for Low-Cost, High-Resolution A/D Techniques


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ible and extensible way.

A design method of particular interest to designers of real-time systems is the use of state machines. A two-part class, "State Machines and State Charts" will discuss Harel state charts, an improved method for representing state behavior in complex systems. The talk will show how state charts can be used with timing diagrams to model the real-time behavior of complex systems. While the emphasis will be on object-oriented models, the methods also can be applied to conventional structured techniques.

Another two-part class will look at "A New Approach to Systems Requirements Modeling." Getting the requirements straight is the first step in a successful design effort. The class will present modeling requirements using familiar notation for data flow and state transition diagrams, but focuses on the "controlled system" as a whole, rather than just on the "controller." The method creates a technology-independent model that can be transformed into an implementation model. Participants will be able to test their knowledge with exercises presented during the session.

One of the large emerging markets in the consumer area is the television set-top box (STB). Just how the STB will ultimately be used in the home is not yet settled. Once in place as a receiver for cable and satellite broadcasts, the STB lends itself to expansion for use as a cable modem for telephone and Internet access. It also could be used as a hub or server for the local network within the intelligent home. A class on "Adapting PC Technology for Set Top Boxes" will explore various PC-hardware architectures available, and present an example of a STB reference design that uses the QNX real-time OS and GUI. The class also will address issues of scalability, system configuration, and obsolescence management.

"Software Design Issues for Set Top Box Applications" will present some common set top box architectures and discuss their impact on the software system design. Topics include signal locking and monitoring, transport layer interaction, MPEG decoding, and user interface design. There also will be a two-part session on the subject of "IrDA Infrared Communications" which has applications that include consumer electronic as well as PDAs and wireless LANs, among a growing list of others. The session will explore the software issues concerned with integrating IrDA into systems including topics such as system analysis and usage scenarios, hardware and software requirements, and protocols, including the IrDA Lite and Ir Object Exchange.

The topic of real-time kernels can be called central to the design of real-time and embedded systems. A number of classes deal directly with the inner workings and the use of real-time kernels. For example, "Inside Real-Time Kernels" will examine matters such as tasks, task control blocks, scheduling, context switching, interrupt servicing and kernel services of real-time kernels. "Designing with Real-Time Kernels"is a class that will describe how to split an application into separate tasks, assign priorities, and use kernel services such as semaphores, messages queues. The class also will describe how interrupts interact with tasks.

Flash memory is gaining use in embedded systems and as a means of transporting data between embedded and desktop systems. "The How-To of Using Flash" will discuss implementing downloadable firmware to upgrade in the field. The class will survey different flash memories, applications for which they are appropriate, integrating flash memory into an embedded system, and issues of debugging. "Programming On-Board Flash Memory Devices With the JTAG Port" will demonstrate a cost-effective way to implement a flash programmer through the JTAG port of an Intel-architecture processor. It also will look at using JTAG to program and read any of the processor pins. Examples in C will demonstrate ways to control the flash device through the parallel port.

For further information, contact Embedded Systems Conference East c/o Expo Reg, 70 Shawmut Rd., Canton, MA 02021; (617) 821-9210; Internet: http://www.embedsyscon.com.

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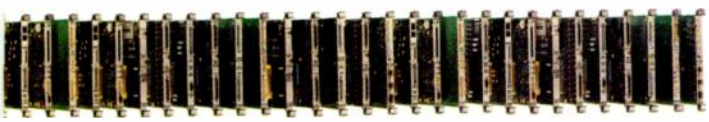

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WHAT'S ON BOARD

By taking advantage of the MMX instruction extensions available on the latest release of the Intel Pentium CPUs, the S-YXG50C wavetable audio device supplies software-based synthesis. The chip, from Yamaha Systems Technology Inc., San Jose, Calif., allows system suppliers to deliver high-quality audio without dedicated hardware. All that's needed is an audio codec. The company claims that the software consumes only a fraction of the CPU's processing power, and allows the CPU to perform additional tasks while delivering the wavetable audio. The product "bundle" offered by Yamaha includes the company's MIDI Studio application with several MIDI files, plus MIDPLUG, the company's plug-in for Netscape Navigator that provides music playback from web sites that have MIDI scores. In addition to providing a "soft" wavetable synthesizer with 16-bit audio and 32-note polyphony, the MMX technology permits features such as various digital filtering schemes, special effects, and playback of CD-quality 44.1-kHz digital audio streams. Contact Tim Lavelle at Yamaha, (408) 467-2300.

A standalone chip packs a full PC-to-television interface, allowing designers to build simple converters that permit PCs to use a television as a display monitor. The AIT2108 video-signal processor chip, from AITech International, Fremont, Calif., contains the company's patented VSPro and Flic-Free technologies that produces a clear, stable image on NTSC or PAL TV screens using the PC's RGB output signals as the input. The chip has a three-channel 8-bit input digitizer, a triple-channel 10-bit digital-to-analog converter, and extended memory to buffer the data. An optional off-chip field memory provides storage for freeze, zoom, pan features, and horizontal and vertical underscan. The circuit supports multiple video standards (NTSC, NTSC-EIAJ, and PAL-B/G/I) and sells for $30 apiece in sample quantities. Contact Richard Lee, (510) 226-8960.

Able to deliver system throughput equivalent to or better than a 166-MHz Intel Pentium, the AMD-K5-PR166 processor from Advanced Micro Devices Inc., Austin, Texas, provides designers with an alternate high-speed CPU. The processor can be dropped into "Socket 7" compatible systems, providing an upgrade path for many systems, and minimizes system redesign time and development cost. The processor is licensed by the Microsoft Windows Hardware Quality Labs to carry the Windows95 logo and has received compatibility certification from XXCAL Inc., an independent testing laboratory. Housed in a 296-pin staggered pin-grid-array package, the AMD-K5-PR166 sells for $167 apiece in 1000-unit lots. Motherboard chipset support is available from multiple suppliers, including Acer Labs, National Semiconductor, and VIA. BIOS support can be obtained from American Megatrends, Award Software, and Phoenix Technology.

A PCI-to-PCI bridge chip that supports 64-bit buses, the 21154 incorporates 64-bit primary and secondary PCI buses, allowing designers to extend the high bandwidth of the 64-bit PCI bus to additional slots on a system motherboard. Designed by Digital Equipment Corp., Maynard, Mass., the chip fully complies with the Rev. 2.1 of the PCI specification, including support for delayed transactions. The chip's enhanced architecture contains deep buffers to improve throughput across the bus. By providing dual 64-bit buses, the chip lets motherboard manufacturers implement systems that include more than the basic four slots permitted by a single PCI controller. The bridge chip allows adapter-card manufacturers to create new cards that overcome the single-load limitation by forming an independent PCI bus on the card, to which up to nine devices can be added. On-chip logic provides the 21154 with two-level arbitration and secondary clocks for up to nine PCI bus-master devices. A JTAG interface permits in-system testing, and four general-purpose I/O pins can be used for programmable control and status signals. Housed in a 304-contact ball-grid-array package, the chip sells for $43.10 apiece in 5000-unit lots. Samples are now available. Contact Matt Theall at Digital Semiconductor, (508) 568-4000.

VMEbus SBC Is Highly Customizable

The 744/132L single-board computer offers a SPECint95 performance rating of 5.9 and a SPECfp95 rating of 6.2. Built with a VMEbus interface, the board comes standard with integrated Ethernet, SCSI-2, dual RS-232 ports, parallel and audio ports, and two PS/2 connections. Two expansion slots are available to accommodate graphics, networking, or other I/O cards. As a result, users can tailor the board for their application needs. One graphics option is the Visualize-EG subsystem that suits such applications as air-traffic control and battlefield management. An ATM mezzanine card can be employed for reliable high-bandwidth isochronous transfers. The 744/132L SBC sells for $8600.

***Hewlett-Packard Co.,** Direct Marketing Organization, P.O. Box 58059, MS511L-8J, Santa Clara, CA 95051; (800) 637-7740.* **CIRCLE 626**

PowerPC Board Offers SMP Capabilities

Built-in symmetric multiprocessing (SMP) capabilities are one of the key features of the PowerEngine 4 series of Power-PC-based single-board computers. Built with a VME64 interface, the boards feature an ASIC that allows the processors to access memory at a rate of 400 Mbytes/s. A dual PCI-bus design supplies a fast interface between boards. One bus runs at 50 MHz at 64 bits, connecting all on-board resources, such as the processors and memory. The second is a 32-bit, 33-MHz bus that accesses the on-board I/O devices.

Standard features on the model VMPC4a include up to 256 Mbytes of DRAM, 1 Mbyte of flash boot memory, Ethernet and fast and wide SCSI interfaces, a PMC site, and a parallel and two serial ports. One or two processors can be employed at 200 or 266 MHz. A host of operating-system and tool support is supplied. With a 200-MHz processor and 32 MBytes of DRAM, prices start at $5900.

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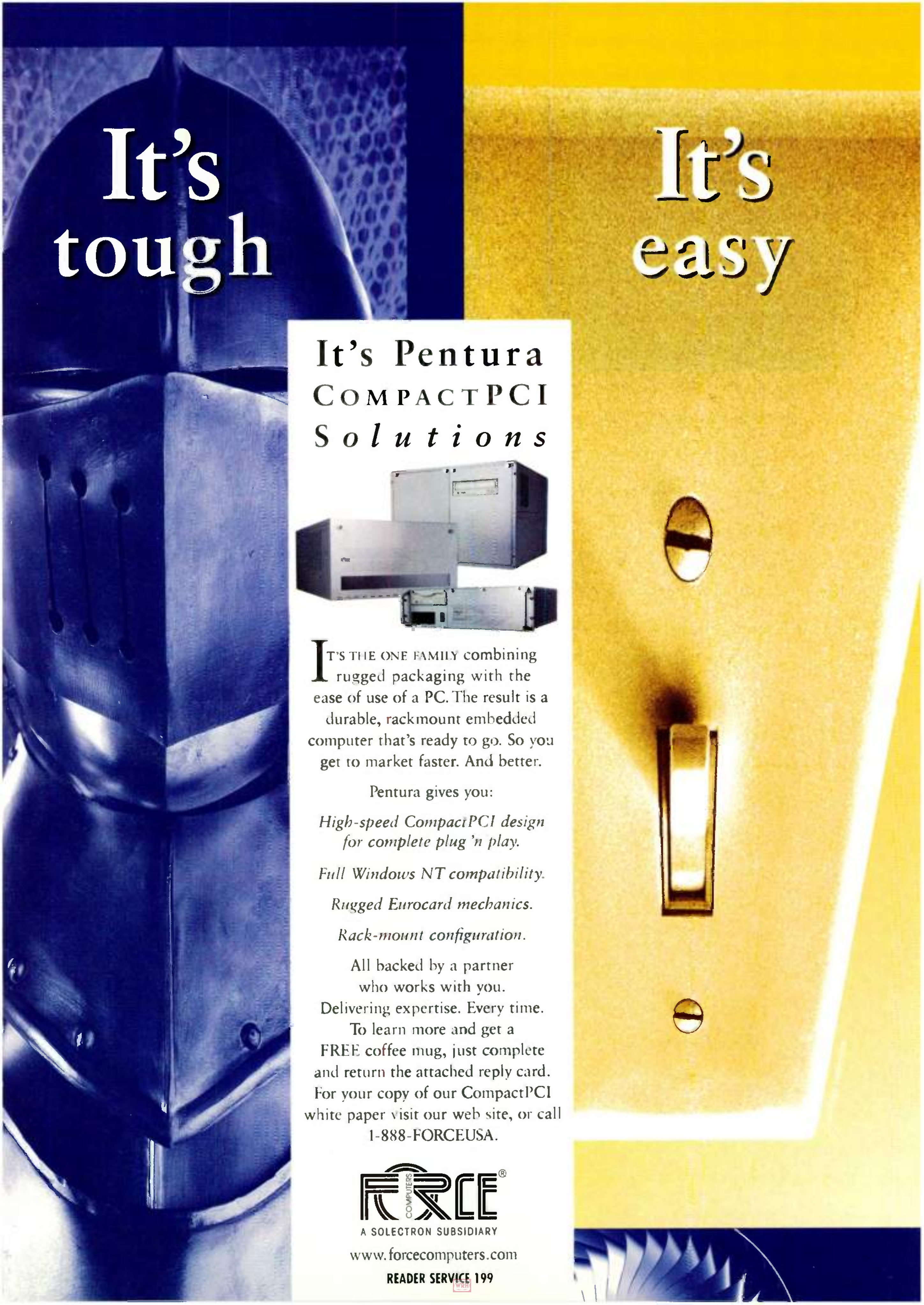
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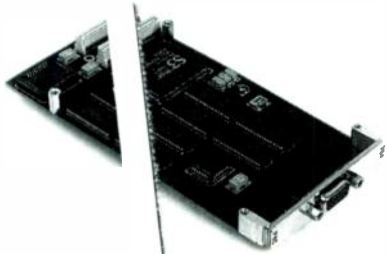

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Concurrent Te nologies Inc., 10921 Reed Hartman H ., # 204, Cincinnati, OH 45242; 513) 791-0073. **CIRCLE 800**

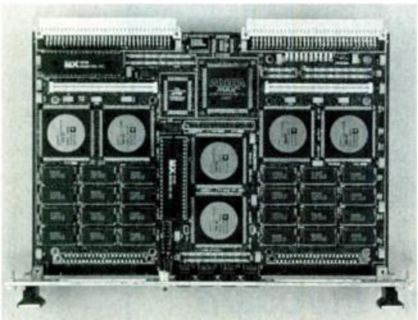
6U VMEbus B rd Is Built With Modula Architecture

The flexibility of the PowerCore Architecture lets OEMs build systems that fit particular needs. For example, one member of the PowerCore family of CPU boards is built with either a PowerPC 603e 120-MHz processor or a PowerPC 604e 200-MHz chip. The 6U VMEbus board contains two PMC slots whose user I/O signals are available on the VMEbus' P2 connector. As a result, easy connections can be made from the rear of the system. Up to 64 Mbytes of DRAM can be employed using user-installable memory modules. For ROM-based applications, up to 8 Mbytes of on-board flash memory is available. The board supports a host of operating systems, including Chorus/Classix, LynxOS, pSOS, VRTX, and VxWorks. Prices start at $2495.

Force Computers Inc., 2001 Logic Dr., San Jose, CA 95124; (888) FORCE-USA or (408) 369-6000; http://www.forcecomputers.com. **CIRCLE 801**

VME Board Features Six Sharc DSPs

Six 40-MHz Sharc DSP chips provide the processing power on the HammerHead V200 VMEbus board. Featuring a peak performance of 720 MFLOPS, the board offers 12 front-panel 40-Mbyte/s link I/O ports and two

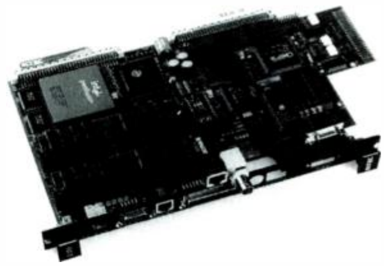


OpenIO baseboard access sites. These sites enable designers to employ off-the-shelf radar and sonar I/O modules, as well as custom modules. Up to 3 Mbytes of shared SRAM can be employed. The DSPs access this memory through a shared bus that's created by tying together the DSP's address and data buses.Up to 3 Mbytes of user-programmable flash memory is shared by all six processors. Operating as a VMEbus slave device, the board supports block-mode transfers. Development support includes a C compiler, assembler, simulator, and Windows-based EZ-ICE multiprocessor source-level emulator-debugger. Drivers for SunOS 4.1 and VxWorks are available. The HammerHead V200 DSP board sells for $7995.

***Ariel Corp.**, 2540 Route 130, Cranbury, NJ 08512; (609) 860-2900; http://www.ariel.com.* **CIRCLE 802**

VME SBC Runs PC-Based Software

Compatibility with the PC is one of the hallmarks of the E128 Pentium-based single-board computer. Built with a VMEbus interface, the board contains an internal 133-Mbyte/s PCI bus, an optional secondary cache, and a processor running at 75 to 166 MHz. The on-board Super VGA graphics controller supports standard monitors and flat-panel displays. The network connection can be 10Base-5, 10Base-2, or 10Base-T. System memory ranges from 8 to 128 Mbytes using standard SIMMs. A PC/104 interface lets users customize the board for specific applications. The reprogrammable BIOS is



stored in a boot-block flash EPROM. The board also can be configured to run without a standard hard-disk drive. All PC-compatible software can be run on the SBC. Prices for the E128 SBC start at $4920. Large-quantity discounts are available.

***American Eltec Inc.**, 101 College Rd. East, Princeton, NJ 08540; (609) 452-1555; http://www.eltec.de.* **CIRCLE 803**

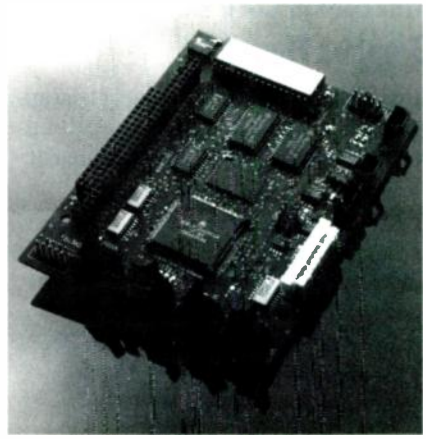
Compact Pentium Module Improves Time To Market

Designed as a tool for quick design of high-end board products, the Liberty module is a compact, Pentium-based CPU board running at speeds ranging from 100 to 200 MHz. The module's small form factor (4.2 by 5.3 in.), combined with its ISA, PCI, and USB connections, suits it for various applications that require a Windows 95 or NT operating system. The module is built with Intel's 430HX PCIset, a DRAM controller, a fast IDE interface, and an interrupt controller. Up to 64 Mbytes of DRAM can be employed using 72-pin SIMMs.

***RadiSys Corp.**, 15025 SW Koll Pkwy., Beaverton, OR 97006; (800) 950-0044; http://www.radisys.com.* **CIRCLE 804**

Low-Cost, Low-Power Board Suits Embedded Applications

Embedded systems are the target of the SBC2000-332 3.75- by 4.85-in. single-board computer. Operating with a 20-MHz Motorola 68332 processor, the board comes with two RS-232 serial ports, a real-time clock, a watchdog timer, and a keyboard port. Typical current draw for the board is 70 mA. Employing power-management



modes, the board can be put into a hibernation mode where almost no current is drawn. The integrated time-processing unit supports special time-related functions like PWM generation, quadrature decoding, asynchronous serial transfer, pulse generation, and period measurement. Basic and C development environments are supported. The SBC2000-332 operates in temperatures ranging from 0° to 70°C. Available immediately, the board sells for $188 each in lots of 100.

***Vesta Technology Inc.**, 11465 W. I-70 Frontage Rd. N., Wheat Ridge, CO 80033; (303) 422-8088.* **CIRCLE 805**

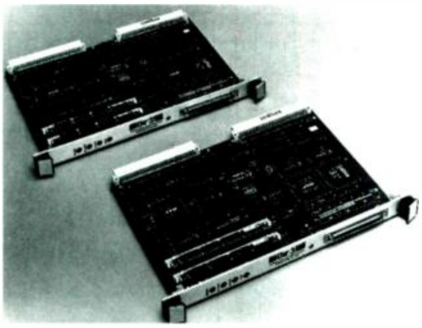
6U VME Board Supplies 960 MFLOPS

Up to 960 MFLOPS of processing power can be achieved from the single-slot IXZ8 Octal Sharc 6U VMEbus board. The board is built with eight 40-MHz processors and also features three banks of global memory, with up to 64 Mbytes of memory in each bank, and 16 off-board Sharc link ports, each operating at 40 MBytes/s. The IXZ8 can operate either as a standalone DSP subsystem or in arrays with other IXZ family boards. The IXZ8 is supported by a comprehensive set of software-development and debugging tools including host support for Solaris, VxWorks, and Lynx OS. In addition to their own tools, Ixthos resells Analog Devices development tools and will supply a full JTAG-based multiprocessor debugging environment and support for large-scale parallel systems that span multiple boards.

***Ixthos Inc.**, 741-G Miller Dr., SE, Leesburg, VA 20175; (703) 779-7800; http://www.ixthos.com.* **CIRCLE 806**

VME64 Adapter Sends 120 Mbytes/s Between Systems

Memory-to-memory transfers of 120 Mbytes/s can be achieved by the 2866 VME64-to-VME64 adapter. Bidirectional random-access reads and writes to the VMEbus are supported

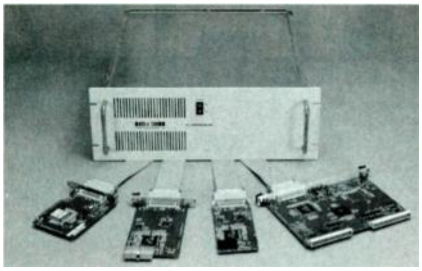


through memory mapping that makes the remote bus-address space appear as address space on the local VMEbus. In slave mode, a VME DMA device, such as a disk controller, can transfer data through the 2866 directly to other VMEbus devices at rates up to 40 Mbytes/s. The 2866 adapter also allows multiple concurrent operations and provides eight programmable interrupts to be exchanged between systems. Eight semophore bits are available for synchronization and serialization between VMEbus systems. One of the two adapter cards can function as the VMEbus system controller, eliminating the need for an additional VMEbus system controller. Optional dual-port RAM SIMMs (up to 2 Mbytes), which can be installed on either or both cards, supply a common memory. Available now, the 2866 two-card VME64-to-VME64 adapter sells for $5995.

***Bit 3 Computer Corp.**, 8120 Penn Ave. South, Minneapolis, MN 55431; (612) 881-6955; http://www.bit3.com.* **CIRCLE 807**

PCI Expansion Boxes Connect To PCI, PMC, Compact PCI, VME

A family of four host cards can connect to a seven-slot mini-tower or 19-in. rack-mount PCI expansion enclosure using a high-speed transmission-line-grade copper cable. The form factor of the four host cards is PCI, 3U Compact PCI, PMC, or 6U VME. In addition to a 212-W power supply and cooling fans, each expansion enclosure has a PCI backplane with slots for seven more PCI cards. The products support 32-bit memory addressing and I/O and



throughput up to 132 Mbytes/s. They can be connected to host computers with PCI buses running at 25 or 33 MHz and have BIOS or boot software supporting secondary PCI-to-PCI bridges to a depth of at least three levels. All combinations adhere to the PCI-to-PCI Bridge Architecture specification version 1.0 and the PCI 2.1 specification. The mini-tower expansion enclosure (model 220-2-1) sells for $648; the 19-in. rack (model 220-2-2) costs $950; the PCI host card (200-2) costs $269; the PMC host card (201-2) sells for $284; the Compact PCI host card (202-2) is set at $289; and the VMEbus host card (205-2) goes for $1015. All are available immediately.

***Bit 3 Computer Corp.**, 8120 Penn Ave. South, Minneapolis, MN 55431; (612) 881-6955; http://www.bit3.com.* **CIRCLE 808**

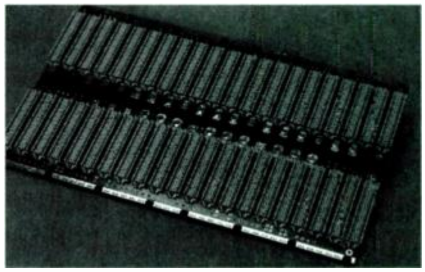
133-MHz PowerPC Guides VME SBC

A PowerPC 603e microprocessor running at 133 Mhz supplies the processing horse-power for the CVME single-board computer (SBC). Compliant with the PowerPC Reference Platform (PReP) standard, the board is designed around the VMEbus and PCI local bus architectures and supports up to four PCI Mezzanine Card (PMC) daughtercards. Designers can populate the PMC slots with functions like networking, SCSI, and graphics. Giving the designer the ability to customize the board makes it suitable for industrial, commercial, and military applications. A host of operating systems are supported, including AIX, Windows NT, LynxOS, and VxWorks. Prices for the CVME single-board computer start at under $5000.

***Cetia Inc.**, 58 Charles Street, Cambridge, MA 02141; (617) 494-0987; http://www.cetia.com.* **CIRCLE 809**

Backplanes Suited For VME64 Applications

The VME64 extensions specification are adhered to by a line of high-performance 64-bit extension backplanes. The 14-layer backplanes feature a five-



row, 160-pin VME extension connector and are fully backward-compatible with VME64- and VME32-equipped boards. The backplanes are suited for use with high-performance P2 mezzanine boards, such as Raceway or Quick-Ring, or systems that require fault-tolerant features. Slot counts of 4, 6, 8, 9, 12, 14, 16, 20, and 21 are available.

***Hybricon Corp.**, 12 Willow Rd., Ayer, MA 01432; (508) 772-5422; http://www.hybricon.com.* **CIRCLE 810**

Get 96 ADCs In Two VMEbus Slots

The VGD4 data-acquisition solutions packs 96 individual 12-bit analog-to-digital converters (ADCs) into two VMEbus slots. The result is high channel density with simultaneous sampling. This configuration is suited for applications such as control, test, simulation, and experimental research, where many analog signals must be digitized quickly and simultaneously. Accuracy can be maintained using a characterized calibration PROM. The digitized data can be transferred over the VME or VSB bus, or directly to a DSP module through TMS320C4X comm ports or Front Panel Data Ports. System integration is simplified by the inclusion of VxWorks software drivers and source library routines.

***Pentland Systems**, 1212 Baxter Drive, Plano, TX 75025; (800) 517 9343; http:\\www.pentlandsys.com.* **CIRCLE 811**

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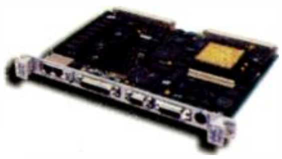

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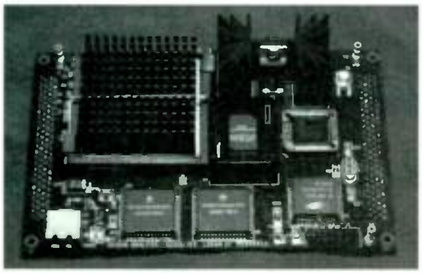
i960 Module Offers High Performance

The embedded i960ECM CPU module is designed for applications that require high performance, yet small size. The 3.4- by 5.3- by 1.4-in. module, which fits in a 168-pin socketed PGA package, is based on Intel's i960Hx architecture. Single-, double-, and triple-



core speed processors are available to supply performance of more than 150 MIPS. The module contains 256 kbytes of SRAM, 128 kbytes of flash memory, and a console serial port with an RS-232 interface. Two 100-pin connector offer external access to the microprocessor buses, interrupt lines, memory and I/O control, and spare signals that can be user-defined for custom applications. It comes bundled with a debug utility loaded into the flash memory. The module also can serve as a standalone evaluation platform for the i960Hx processor. An on-board electrically-erasable CPLD can be modified for prototype development. Power comes from a single +5-V supply. An on-board voltage regulator powers the processor with the required 3.3 V. Large-quantity pricing starts below $600.

Design Analysis Associates Inc., 75 West 100 South, Logan, UT 84321; (801) 753-2212. **CIRCLE 812**

SBCs Boast Extensive Embedded Software Suite

An extensive suite of embedded software adds to the value of the 6050 and 6040 single-board computers. The software suite includes diagnostics, networking, a DOS 6.22 operating system, and CAMBASIC, which is a multitasking control and data-acquisition language. Contained in flash memory, the software eliminates the need to write specific device drivers.

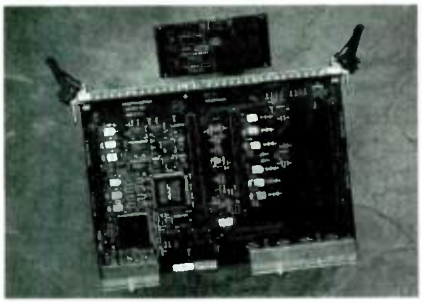
The boards' feature sets include dual 16C550-compatible serial port, an enhanced parallel port, two opto-isolated interrupts, 24 lines of bit-programmable digital I/O, a real-time clock, 1 Mbyte of flash memory, and 2 Mbytes of DRAM. The difference between the two boards is that the 6040 adds 10 lines of 12-bit analog I/O.

The boards, which measure 4.5 by 4.9 in., are built to work in rugged environments. For example, the operating temperature range runs from -40°C to +85°C. In addition, all the I/O lines of the board are protected, meaning that the serial ports can withstand an 8-kV discharge without failure, and the opto-isolation on the external interrupts protects the cards from high-voltage transients. Available now, the 6050 sells for $374, while the 6040 costs $562.

Octagon Systems, 6510 W 91st Ave., Westminster, CO 80030; (303) 430-1500. **CIRCLE 813**

IndustryPack Carrier Board Fits Compact PCI Systems

Intended for Compact PCI systems, the cPCI-200 is a carrier board that allows systems integrators to attach up to four IndustryPack (IP) modules.

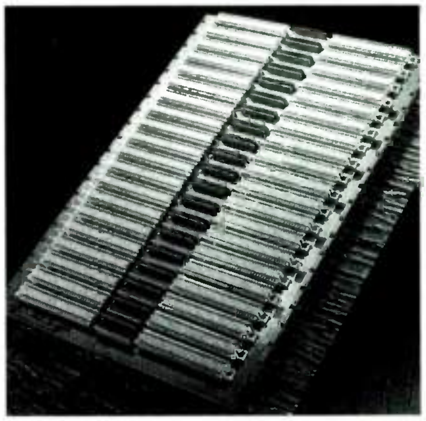


Typical applications for the modules include communications, motion control, temperature measurement, and graphics. The cPCI-200 employs a PLX9060 as the PCI bus interface chip to provide configurable PCI interrupts. It can be configured for either 8 MHz or 32 MHz operation. The full 8-Mbyte memory space, as well as two interrupts, are available for each IP site. Each IP site has a dedicated, shielded, latching front-panel connector. This feature allows complex systems to pass CE emission and immunity requirements. All I/O lines are routed through the backplane using J4 and J5 connectors. The cPCI-200 starts at $1095.

GreenSpring Computers, 181 Constitution Drive, Menlo Park, CA 94025; (415) 327-1200; http://www.greenspring.com. **CIRCLE 814**

VME Backplanes Offer New Features

A family of VMEbus backplanes offers a host of new features. For example, the backplanes includes a 160-pin DIN connector with "Z" and "D" pin rows in both the P1 and P2 areas. The new connectors are backward-compatible so that a 96-pin DIN connector can mate with the 160-pin VME64x connector. An optional P0 connector can be used between the P1 and P2 connectors to supply and extra 95 user-definable pins on a 2-mm hard metric connector. Other features include improved 3.3- and 48-V supply voltages, 35 additional ground returns, user-defined I/O pins on P2, and an optional test- and maintenance-bus interface. The VME64x backplanes come in 7-, 10-, 14-, 17-, and



20-slot sizes. The backplanes are available now.

VERO Electronics Inc., 1000 Sherman Ave., Hamden, CT 06514; (800) 642-VERO; http://www.vero-usa.com. **CIRCLE 815**

VMEbus Board Can Be Upgraded To Pentium Pro

While the EPC-9 VME CPU board comes standard with a Pentium microprocessor, it can be field-upgraded to a Pentium Pro chip. Other significant features of the board include integrated Ethernet and fast SCSI 2, two Universal Serial Bus (USB) ports, and connectors for two PMC daughterboards. The EPC-9 is PC/AT compatible and offers four 72-pin SODIMM sockets and 256 kbytes of secondary cache. An optional 1.44-Gbyte, 2.5-in. IDE hard-disk drive fits directly on the board without requiring an additional slot in the backplane. 100-, 133-, 166-, and 200-MHz Pentium processors are currently being offered. By mid-year, the Pentium Pro upgrade will be available. In lots of 100, the EPC-9 costs $3527 with a 133-MHz processor and 8 Mbytes of RAM. An SVGA PCM costs $206 in similar quantities.

RadiSys Corp., 5445 NE Dawson Creek Dr., Hillsboro, OR 97124; (503) 615-1100; http://www.radisys.com. **CIRCLE 816**

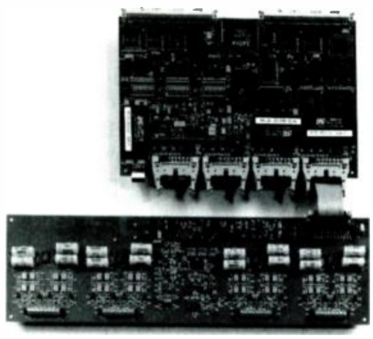
VMEbus Enclosure Contains Necessary Smarts

Designers can take advantage of the large area offered by the SmartChassis VMEbus enclosure. The intelligent chassis is built with voltage and thermal monitors to return control and system status to the user. The voltage monitor continuously measures voltages at the backplane to the VMEbus specification and supplies LED indicators for voltage status. The universal auto-ranging power supply automatically corrects the power factor to increase efficiency and present a resistive load to the power line. The thermal monitor continuously measures internal chassis temperatures and adjusts fan speed for minimal acoustical noise while providing maximum cooling. An audible alarm triggers when the SmartChassis reaches 45°C. The card-cage incorporates active automatic daisy chaining which eliminates improperly placed bus-grant jumpers. The SmartChassis consists of a 12-, 20, or 21-slot 6U by 160-mm or 9U by 400-mm card-cage frame. Three 90 CFM fans fit into the back of the enclosure.

Electronic Solutions, 6790 Flanders Dr., San Diego, CA 92121; (800) 854-7086 or (619) 452-9333. **CIRCLE 817**

Accurate Thermocouple Board Connects To VMEbus

Designed with a VMEbus connection, the VME 8436/50 thermocouple board is suited for process applications that demand high accuracy. The 6U board accommodates 64 channels in one



VMEbus slot. It features an analog-to-digital with true 16-bit accuracy. Typical CMRR exceeds 140 dB and the linearity error is better than 0.025%. The board connects to thermocouple devices through up to eight 8-channel remote multiplexer termination panels, which provide bare-wire connections through screw terminals to facilitate wiring. The multiplexer panels feature 1500-V isolation protection between grounds. A temperature sensor located on the multiplexer panel performs cold-junction termination measurement. An on-board 68020 microprocessor performs cold-junction compensation, thermocouple linearization, and EU conversion in software. Available now, the VME 8436/50 board is priced at $9430.

RTP Corp., 2705 Gateway Dr., Pompano Beach, FL 33069; (954) 974-5500. **CIRCLE 818**

High-End Board Serves Networking Applications

Embedded network bridge applications are the primary target for PowerBridge, a high-performance network-based compute engine. The platform will operate within the Advanced Intelligent Network and wide-area datacom markets. Employing various PCI Mezzanine Card (PMC) network interface modules that plug into two expansion slots, the PowerBridge lets users bridge to various networks including SS-7, T1/E1, X.25, HDLC, Frame Relay, ISDN, ATM, and Fast Ethernet. For protocol processing and other telecompute functions, the platform offers a choice of either a PowerPC 604e or 603e processor with up to 64 Mbytes of DRAM. To accommodate standard fast network connection for both development and end application use, the PowerBridge's Fast Ethernet (100-Mbit) port employs FIFO buffers and DMA, which off-loads the host processor of LAN transfers. The system supports Wind River's VxWorks real-time operating system.

Heurikon Corporation, 8310 Excelsior Dr., Madison, WI; (608) 831-5500 or (800) 356-9602, http://www.heurikon.com **CIRCLE 819**

Digital-Audio Boards Suit VMEbus Systems

High performance audio is needed for various VME-related applications, including simulators, multimedia workstations, industrial control systems, voice synthesis and recognition, and sound analysis. The Vigra family of digital-audio boards offers two or four channels of mono or stereo signals that allow users to record and playback sounds, generate tones, and digitally mix the sounds and tones. On-board DSPs supply various encoding and data compression methods ranging from 14- or 16-bit linear PCM to 4-bit Adaptive Differential PCM. Firmware provides easy-to-use, sophisticated digital recording and playback modes, offering a high-level interface to the flow and processing of audio data. Other features of the firmware and software include real-time vector-quantizing audio compression and decompression for very low bit-rate audio; real-time digital mixing; support for most popular audio data formats; and tight buffering for low latency. Available immediately, the Vigra VMEbus digital-audio boards start at $3900, with large-quantity discounts available.

VisiCom, 10052 Mesa Ridge Ct., San Diego, CA 92121; (619) 457-2111 **CIRCLE 820**

256-Mbyte Memory Module Supplies 320-Mbyte/s Access

The SKYbolt II multiprocessor VMEbus board can now be fitted with a high-capacity memeory module. Using the SKYram daughtercard, the memory module can be attached directly to the multiprocessor motherboard. This combination results in both faster access time and reduced costs.

The SKYchannel packet bus offers faster access by allowing the entire DRAM array to be accessed by any processor or other device in the SKYchannel system at the full 320-Mbyte/s bandwidth. In large system configurations, costs are reduced because fewer slots are needed for memory. Up to 256 Mbytes can be added to a SKYbolt II 6U, up to 512 Mbytes to a SKYbolt II 9U, and up to 768 Mbytes to the SKYpack. The SKYram fits on a 3- by 6-in. daughtercard that sits next to the compute daughtercards on each motherboard. Modules are available in increments of 64 Mbytes, up to 256 Mbytes per daughtercard. SKYram prices start at $3185.

***Sky Computers Inc.**, 27 Industrial Ave., Chelmsford, MA 01824; (508) 250-1920, http://www.sky.com.*
CIRCLE 821

VME High Performance Color Graphics Server

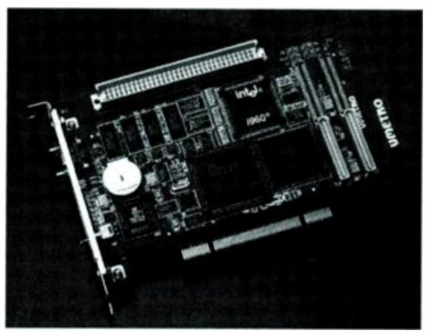
The VGS-882 graphics server, built with a single-board RISC-based processing engine, is intended for real-time VME-based graphics applications. The system executes X-Windows server software on its LSI Logic 33020 graphics processor. As a result, the burden of the X-Windows server processing is removed from the host CPU, freeing it for other tasks. This helps to increase the overall speed and performance of the system.

The LSI 33020 is a 33-MHz processor that's MIPS 3000-compatible. Its RAMDAC has a 256-entry color palette and drives most standard high-resolution monitors. It also supplies four overlay inputs and a hardware cursor. The VGS-882 supports programmable resolutions from 640-by-480 to 1280-by-1024 pixels. When using 640-by-480-pixel resolution, the display can appear simultaneously on an LCD panel and a VGA monitor. The system's VME slave interface gives VMEbus masters access to on-board memory. All standard 8-, 16-, and 32-bit VME access types are supported, including burst-mode, read-modify-write, and interrupt-acknowledge cycles. When a VME bus master accesses the board, the slave interface takes control of the 33020's system bus to transfer data.

***VisiCom**, 10052 Mesa Ridge Ct., San Diego, CA 92121; (619) 457-2111.*
CIRCLE 822

Development Tool Works With PCI- Or PMC-Based Platforms

Available either as a single standalone PCI board or as a PMC module, the Pdrive can operate as a bus master, target, or interrupt generator. The device is intended as a tool for testing PCI bus boards or systems. The board can generate and respond to nearly all PCI bus cycles types under full user control at the command level.



The Pdrive is implemented with an Intel I960 RISC processor talking to the PCI bus through a PLX 9060 PCI interface chip. This allows the Pdrive to act as a reference unit that generates cycles on the PCI bus with known characteristics. The device also can run memory tests with various data patterns, which is useful for testing new boards or in the debugging of faulty boards. Available now, the PMC version of the Pdrive development tool sells for $3995, while the PCI board model is priced at $4495.

***Vmetro Inc.**, 1880 Dairy Ashford, #535, Houston, TX 77077; (713) 584-0728.* **CIRCLE 823**

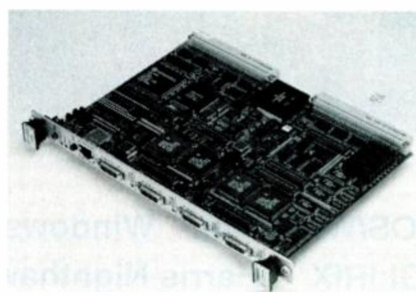
Digital Input Board Offers 32 Channels Of Variable Voltage

The NDI family of 6U digital-input cards for the VMEbus give the user 32 channels of variable voltage discrete inputs (5, 12, 24, and 48 V). Suited for harsh environments, the boards come in four classes—laboratory (0 to +55°C), rugged forced air (-40 to +75°C), rugged conduction (-40 to +75°C), and military (-55 to +85°C). Each of the four groups of eight inputs are jumper-selectable to monitor contact closure, voltage source, and current sinking. The selectable input-voltage threshold ranges from 1.25 to 66 V. The digital-input boards contain the circuitry needed for built-in test.

***Vista Controls Corp.**, 27825 Fremont Ct., Santa Clarita, CA 91355; (805) 257-4430; http://www.vistacc.com.*
CIRCLE 824

Communications Board Suits WAN Applications

Aimed at wide-area-network (WAN) applications, the PT-VME340 synchronous communications controller connects to the VMEbus. The board employs a four-channel serial I/O controller interface that's coupled to a 40-MHz, 32-bit 68EC030 microprocessor core supporting sustained data rates up to 10 Mbits/s. Flexibility is achieved using the plug-in line-adapter boards (LABs). The LABs lets users employ most industry-standard interfaces. The VME64 interface offers transfer rates up to 60 Mbytes/s over the backplane. Up to 4 Mbytes of shared memory can be employed.



***Performance Technologies Inc.**, 315 Science Pkwy., Rochester, NY 14620; (716) 256-0200; http://www.pt.com.*
CIRCLE 825

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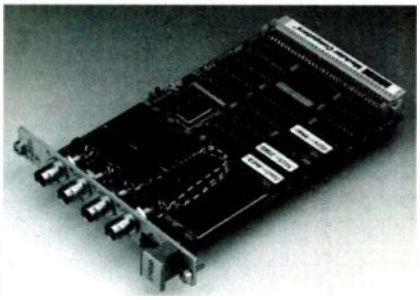
READER SERVICE 209

Serial I/O Card Conforms To MIL-STD-1553

Suited for harsh environments, the V1553B serial-bus module conforms to the Mil-STD-1553 standard. Built to a 3U VMEbus form factor, the card offers two dual-redundancy serial channels of electrically-isolated I/O at a transfer rate of up to 1 Mbits/s. The board is shock and vibration resistant at the extended temperature range of -40° to +85°C. Events can be tagged with a resolution of up to 2 µs. The card ships with a library for initialization of the three operation modes—bus controller, remote terminal, and bus monitor. In typical operation, the board consumes less than 3.5 W, thereby eliminating the need for special cooling procedures. Supporting real-time operating systems include OS-9 and VxWorks.



***PEP Modular Computers Inc.**, 750 Holiday Dr., Bldg 9, Pittsburgh, PA 15220; (800) 228-1737 or (412) 921-3322.* **CIRCLE 826**

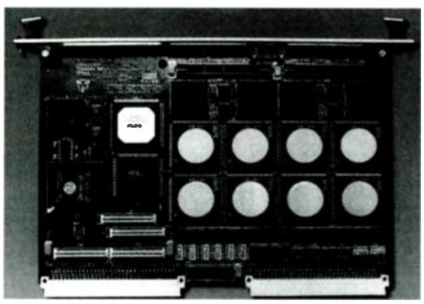
Software Lets Users Treat Tape Like A Disk

Users of tape drives can view the peripheral as a logical hard-disk drive using the File Xpress. By simulating a random-access device, large files can be transferred and run directly from tape. As a result, multimedia users can take better advantage of their available hard-disk space to run more complex applications. In addition, on-line data can be temporarily stored on tape to avoid using critical disk space. According to the company, File Xpress runs 10% faster than any competitive product. The software supports all conventional file operations, such as delete, copy, move, rename, and execute. The software supports most popular peripheral interfaces, including ATAPI, SCSI, and a parallel port. It operates under the Windows 95 or Windows NT operating system. File Xpress sells for $29. Evaluation copies can be downloaded from the Internet for a 30-day live trial.

***Shuttle Technology**, 43116 Christy St., Fremont, CA 94538; (510) 656-0180; http://www.shuttletech.com.* **CIRCLE 827**

DSP-Based VME64 Board Tops Out At 960 MFLOPS

A peak performance level of 960 MFLOPS and an 80-Mbyte/s transfer rate can be achieved from a single 6U VMEbus slot using the V8 Octal Sharc VME64 DSP board from Spectrum Signal Processing Inc. The board's integrated PCI bus connects an IEEE P1386 PMC site to the VME64 bus and the eight Sharc processors. The PCI bus allows transfers of 132 Mbytes/s from the processors to the VME64 bus and the PMCs. The PMC slot can be populated with any compatible I/O, networking, or memory module, allowing users to customize the board for a particular application. Typical applications include high-end signal and image processing, radar, sonar, and medical imaging.



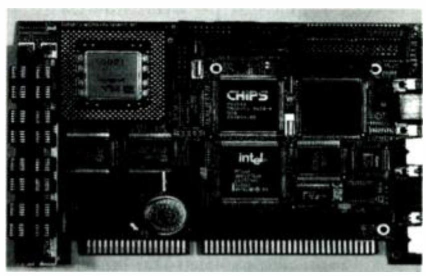
The V8 Octal design is based on eight 40-Mhz 120 MFLOPS ADPS2106x DSPs arranged in four clusters of two processors each. Each cluster has 512 kbytes of zero-wait-state SRAM. An additional 1 Mbyte of global SRAM is available to all clusters. Each processor also has 2 or 4 Mbits of on-chip dual-port SRAM that reduces the external bottlenecks by allowing the core processor functions to occur simultaneously with DMA data transfers to and from internal memory. VME64- or PMC-based I/O devices can write to either the cluster or common memory depending on the application. The board contains a flat coaxial cable connection from the front panel that allows a 40-Mbyte/s Sharc link-port transfer.

Software support comes from Spectrum as well as from third-party software suppliers, including operating systems, development tools, debuggers, and DSP and host-interface libraries. Available in the second quarter, the V8 Octal Sharc board starts at $24,000.

***Spectrum Signal Processing**, 8525 Baxter Pl., 100 Production Ct., Burnby, B.C., Canada V5A 4V7; (604) 421-5422; http://www.spectrumsignal.com.* **CIRCLE 828**

Pentium SBC Suits Embedded Applications

A Pentium microprocessor delivers the processing power on the 2109 single-board computer. The board is built with a Chips and Technologies 65548/65550 CRT and flat-panel controller with integrated BitBlt and GUI accelerator features. The graphics controller resides on a local bus and supplies a resolution up to 1280 by 1024 pixels using up to 1 Mbyte of video RAM. Also on the board is Intel's Triton II chip set, which offers support for the Universal Serial Bus (USB) and infrared (IR) connectivity. Up to 512 Mbytes of RAM can be employed. The 2109 incorporates basic embedded PC and system BIOS features, such as temperature sensing for processor clock-speed reduction. As a result, no fan is needed for processor clocks up to 133 Mhz. Prices for 100-MHz 2109 single-board computer fall in the $800 range for 100-piece quantities.



***Toronto MicroElectronics Inc.**, 5149 Bradco Blvd., Mississauga, Ontario, Canada L4W 2A6; (905) 625-3203; http://www.tme-inc.com.* **CIRCLE 829**

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READER SERVICE 198

Video Conference From A Notebook PC

By using the VideumConf Traveler and a notebook computer, users can employ videoconferencing from a remote location. The heart of the VideumConf Traveler is the Videum Traveler, which is an audio and video capture system built into a PC Card. It combines audio and video processing for H.324 and Internet videoconferencing and multimedia functionality. The VideumConf Traveler also includes the VideumCam color video camera with integrated microphone, a headset, and all the software needed for videoconferencing. Features of the package include full-duplex audio, remote camera control, and video capture at up to 30 frames/s with fully synchronized audio. All standard software protocols are supported. The VideumConf Traveler sells for $499. The Videum Traveler can be purchased separately for $299.

***Winnov**, 1150 Kifer Rd., Suite 201, Sunnyvale, CA 94086; (408) 733-7419; http://www.winnov.com.* **CIRCLE 830**

Subnotebook Computer Is Suited For All Climates

You've heard of an all-terrain vehicle. Now we're being introduced to the all-terrain subnotebook computer, dubbed the Scout. The compact (9.1 by 6.25 by 2.85 in.), light-weight (5.2 lbs.) computer runs the Windows 95 operating system. The platform integrates wireless communications technologies, including ARDIS, RAM Mobile Data, and cellular/CDPD. The Scout is built with a magnesium enclosure, a rubber bumper system, a floating hard-disk drive, and shock-mounted components. The waterproof connectors make the system water-tight to NEMA 4 and MIL-STD-810-E specifications. the standrd NiMH battery oofers a two-hour recharge time. The smart battery maintains an accurate measurement of battery capacity, as well as the history of charge cycles. A host of options are available, including a 28.8-kbaud data-fax modem. Prices for the Scout start at $2995.

***Melard Technologies Inc.**, 28 Kaysal Ct., Armonk, NY 10504; (914) 273-4488.* **CIRCLE 831**

Modules Add T1 Communications Capability

Big, expensive external connection boxes can be eliminated using the IM T1-CSU piggy-back module. Aimed at communications platforms, the module allows full-duplex operation for receiving and transmitting on one T1 channel. The module, which measures 13.2 by 4 cm, interfaces with DSX-1 trunks using an eight-position RJ-45 connector and supports D4 and Extended Super Frame (ESF) formats. Because of the small size, two channels can be installed on each communication card. It's also available for OEMs looking to build the functionality into existing cards. The IM T1-CSU sells for $495.

***Computer Modules Inc.**, 2350 Walsh Ave., Santa Clata, CA 95051; (408) 496-1881; http://www.compmod.com.* **CIRCLE 832**

CPU And Switch Boards Form Multicomputing Platform

The MAP-2610 6U VMEbus board delivers 400 MFLOPS of processing power in a single-slot form factor. Designed for use in a System Area Network (SAN), the board contains one Myrinet SAN front-panel connector. The board's processing power comes from its PowerPC 603 microprocessor running at 200 MHz. Other features include 5 Mbytes of flash memory, a high-performance memory controller, 64 Mbytes of DRAM, and a VME64 interface.

A 64-bit PCI bus is used for high-performance and flexible I/O. A companion PMC carrier board can be connected to the MAP-2610 to form a two-slot subsystem. The carrier board accommodates two modules. Another option, the MAP-SW-10, implements five SAN microstrip Amp aconnector on the front-panel and another on the VMEbus' P0 backplane connector. Each front-panel connector supports two Myrinet SAN links, and each link can operate at 320 Mbytes/s. A host of software utilities are available. The MAP-2610, with a run-time software license, sells for $18,500. The MAP-SW-10 costs $4800. Large-quantity discounts are avilable on both.

***CSPI**, 40 Linnell Circle, Billerica, MA 01821; (800) 325-3110 or (508) 663-7598.* **CIRCLE 833**

Half-Size CPU Board Suits Embedded Applications

Operating at speeds up to 133 MHz, the IHV-486/5x86 half-size ISA board offers Super VGA capability on-board, as well as an option to use the PROMDisk-Chip Disk Emulator in either a 2- or 4-Mbyte size. The board comes bundled with ROM-DOS 6.22. The passive-backplane CPU board comes in a 4.8- by 7-in. form factor, thereby suiting it for embedded applications.

The board's integrated PCI local bus Super VGA controller combines with 1 Mbyte of video RAM to result in a screen resolution of 1024 by 768 pixels with 256 colors or 1280 by 1024 pixels with 16 colors. The Super AT I/O controller that's employed includes dual NS16C550 UARTs, a dual PCI Enhanced IDE hard-disk port, and an enhanced parallel port. The board operates from a single +5-V power supply and has an external power connector that gives users a direct connection to an external power supply. The IHV-486/5x86 is priced at $625. Large-quantity discounts are available.

***Micro Computer Specialists Inc.**, 2598 Fortune Way, Vista, CA 92083; (619) 598-2177; http://www.industry.net/mcsi.* **CIRCLE 834**

Combine 140 PowerPCs For 38 GFLOPS

A series of multicomputer systems based on the PowerPC603e microprocessor deliver 4.4 GLOPS on a 9U form factor VMEbus motherboard or 1.1 GLOPS on a 6U board. Based on the Raceway architecture, the platforms can hold up to 140 200-MHz microprocessors, resulting in a top performance rating of 38 GFLOPS. The Raceway heterogeneous architecture, which employs a switched-fabric interconnect, addresses embedded multicomputing requirements with a building-block approach that's suited to power- and space-constrained applications. Systems are available now.

***Mercury Computer Systems Inc.**, 199 Riverneck Rd., Chelmsford, MA 01824; (508) 256-1300; http://www.mc.com.* **CIRCLE 835**

Talented Students Across the Nation are Recognized in 1996 Student VLSI Design Contest

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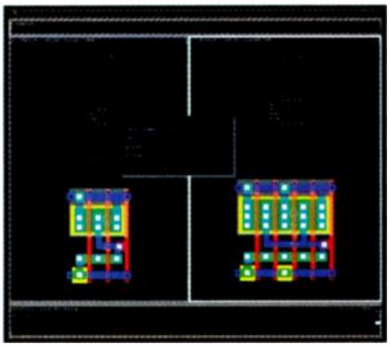


Novice Category – Rutgers University

Rutgers University students, Madhu K. Iyer and G. Parthasarathy, were awarded first place in the novice category for their entry titled, "Design of a Branch Prediction Controller Chip." This project dealt with the design and implementation of a hardware solution for branch prediction in deeply pipelined processors. They relied on Mentor Graphics' GDT Designer™ for the design of this chip.

Experienced Category – University of Michigan

The University of Michigan graduate students, Phiroze Parakh and Todd Basso, won first place in the experienced category for their design, "A High-Speed CGaAs Using Domino Logic." The primary focus of this work was to evaluate the capabilities of Domino Logic using Motorola's 0.5 μm CGaAs technology. This design was completed using Mentor Graphics' IC Station®

Winners: Novice Category

1. **Rutgers University** – Madhu K. Iyer, G. Parthasarathy
2. **Oregon State University** – Priya Parthasarathy, Douglas Beck, Ong Wee Shong, Ramsin Ziazadeh
3. **University of Minnesota** – Halim Theny, Aashish Rao
4. **University of Minnesota** – David Parker, Scott Hussong
5. **Harvard University** – Alexander Bugeja
6. **University of Michigan** – Maruis Evers, Michael Anderson, Michael McCurdy, Demetrious Papageorgieu, Edvard Veeser
7. **University of Nebraska-Lincoln** – Chuck Feilmeier, Joe Krause

Winners: Experienced Category

1. **University of Michigan** – Phiroze Parakh, Todd Basso
2. **University of Michigan** – Claude Gauthier
3. **University of Michigan** – Navid Yazdi, Andrew Mason
4. **University of Michigan** – Spencer Gold
5. **Colorado State University** – Fahad Alzahrani

Congratulations to these students on their winning designs!

A special thank you to Electronic Design Magazine for donating this space to recognize these talented students.

Mentor Graphics

THE POWER TO CREATE

Circle 520

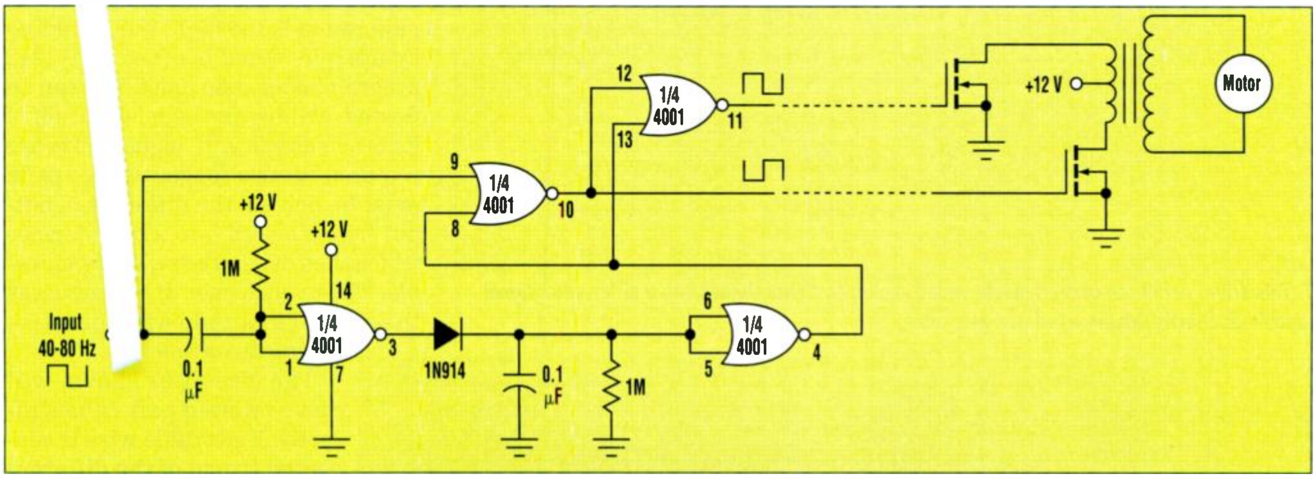
Missing Pulse Detector Protects Transformer

MICHAEL A. COVINGTON
285 Saint George Dr., Athens, GA 30606; (706) 549-4633.

Designed as part of the controller an astronomical telescope, this circuit delivers an ac drive waveform to the drive motor. The frequency of the ac output is set by an external oscillator that generates the desired drive rate.

But what happens if the oscillator fails or isn't hooked up? Most circuits of this type would leave one side of the transformer continuously energized, causing it to saturate and damage one of the FETs.

To keep this from happening, a missing-pulse detector was designed using two CMOS NOR gates *(see the figure)*. The input is capacitively coupled so that it will not be affected if the input gets stuck high or low. A 0.1-µF capacitor charges quickly through a diode and discharges slowly through a resistor. If the input signal is present, the charge on the capacitor is refreshed on every cycle. If not, the capacitor discharges, the output of the second gate goes high, and both FETs are held "off" until the input resumes.



This circuit generates complementary outputs for driving push-pull amplifiers, but both outputs are disabled if the oscillator fails.

VOTE!

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Address your Ideas for Design submissions to: Ideas for Design Editor, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604.

IFD WINNER

Scott C. Willis and Mark J. Jones, Loral Federal Systems, 9500 Goodwin Dr., MS 120/025, Manassas, VA 22110, (703) 367-4645. The idea: *"Fault-Tolerant Relay Driver Circuit."* June 24,1996 Issue.

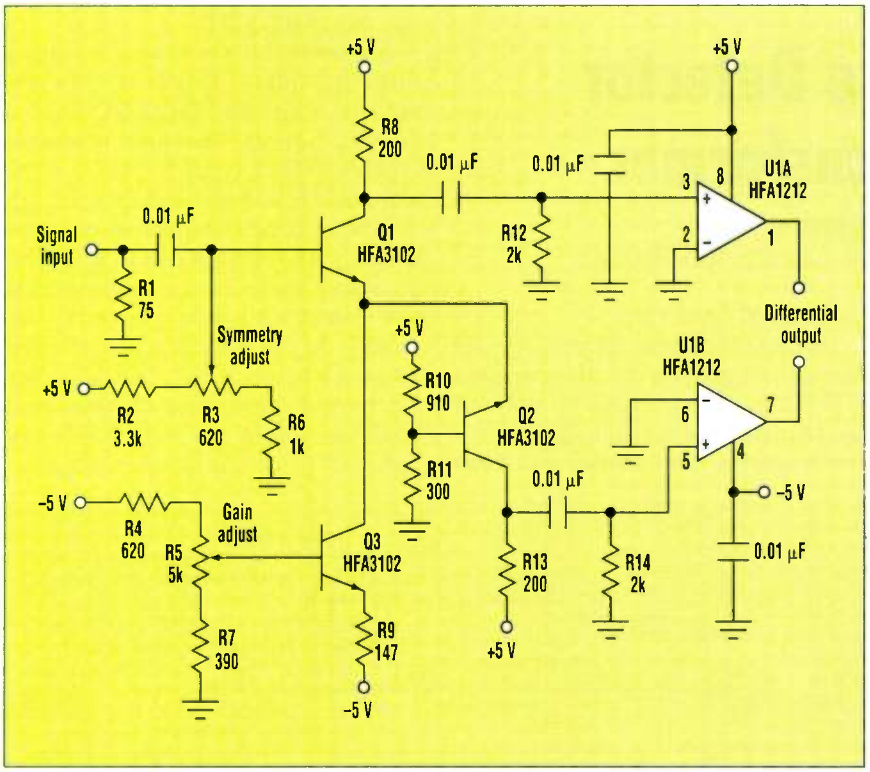
Circle 521

Single-Ended To Differential Twisted-Pair Driver

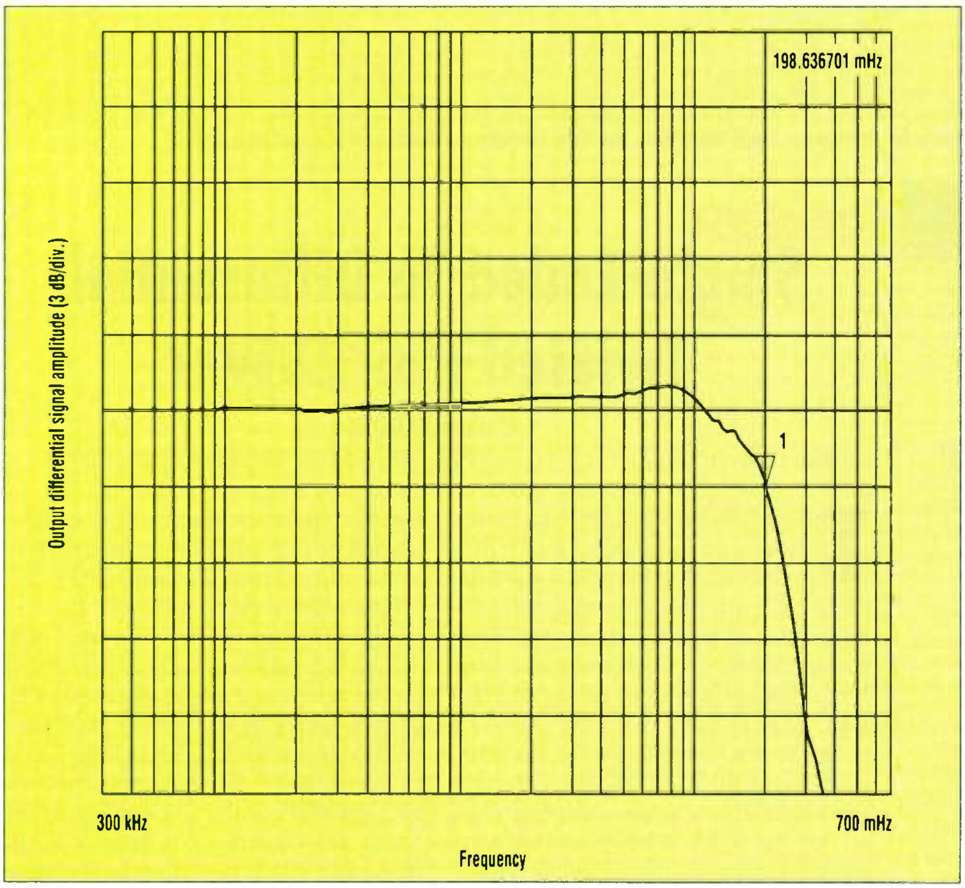
RONALD MANCINI
Harris Semiconductor, P.O. Box 883, M/S 58-095, Melbourne, FL 32902.

The proliferation of personal computers and particularly of video applications has created a need for sending high-speed analog signals over twisted pair for short distances (up to 200 feet). Twisted-pair data transmission is easy to set up and the wire cost is very low compared to coax, so it's becoming a popular replacement for coax. Most electronic signals exist in a single-ended format, so the signal must be converted to a double-ended or differential format to take advantage of twisted-pair data-transmission schemes. The circuit described here converts single-ended analog or digital signals into a differential signal capable of directly driving a twisted pair cable *(Fig. 1)*.

Q1, Q2, and Q3 are one half of a HFA3102 dual long-tailed-pair transistor array, and are configured in to function as a linear differential amplifier. Because the transistors are matched, they will yield nearly identical performance depending upon their bias circuits. The base of Q2 is biased at 1.24 V, and the base voltage of Q1 ranges from 1.0 to 1.6 V depending on the setting of R3. When



1. This driver circuit can convert single-ended analog or digital signals into a differential signal capable of directly driving a twisted-pair cable.



2. The frequency response for the single-ended to differential twisted-pair driver indicates a –3-dB bandwidth of 200 MHz.

R3 is set at 1.24 V, the signals are amplified equally by both transistors. Consequently, R3 functions as a symmetry adjustment that can be used to obtain equal amplitude but opposite phase outputs at the collectors of Q1 and Q2. This criteria satisfies the definition of a differential signal.

The differential gain is 5 to 7, as configured in Fig. 1. The gain is set in this range because a typical video signal is less than 2 V in amplitude, and these low gains won't cause distortion. R5 adjusts the current through both transistors and, since the gain is proportional to the emitter current, R5 functions as a gain control. If the gain range is too high, the inverting inputs (pins 3 and 6) of the HFA1212 programmable-gain amplifiers can be floated, making the gain fall to half of its previous value. If higher gains are required because longer twisted pairs must be driven, the differential output has to be fed into a transformer which then drives the twisted-pair cable. The transformer drive increases the signal amplitude without introducing distortion.

The circuit as shown will drive twisted pair cables directly. Each cable wire is connected to one of the differential outputs, and the cable is terminated at the receiving end in its characteristic impedance (about 100 Ω).

The frequency response for linear signals shows a -3-dB bandwidth of 200 MHz *(Fig. 2)*. The response of twisted-pair cables falls off at higher frequencies, so the amplifier response curve is purposely peaked at higher frequencies to compensate for this effect. This combination will yield a flatter overall frequency-response curve.

This driver, when coupled with a differential receiver, will reliably transmit data over 200 feet of twisted-pair cable in the presence of several hundred millivolts of single-ended noise. Digital signals should be handled the same as video signals, except that wide fluctuations in the digital data rate will cause skew due to the ac coupling.

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ERA-1	DC-8000	11.8	11.7	5.3	26.0	40	1.80
ERA-1SM	DC-8000	11.8	11.3	5.5	26.0	40	1.85
ERA-2	DC-6000	15.6	12.8	4.7	26.0	40	1.95
ERA-2SM	DC-6000	15.2	12.4	4.6	26.0	40	2.00
ERA-3	DC-3000	20.8	12.1	3.8	23.0	35	2.10
ERA-3SM	DC-3000	20.2	11.5	3.8	23.0	35	2.15
ERA-4	DC-4000	13.5	▲17.0	5.5	▲32.5	65	4.15
ERA-4SM	DC-4000	13.5	▲16.8	5.2	▲33.0	65	4.20
ERA-5	DC-4000	18.8	▲18.4	4.5	▲33.0	65	4.15
ERA-5SM	DC-4000	18.5	▲18.4	4.3	▲32.5	65	4.20
ERA-6	DC-4000	11.3	▲18.5	8.4	▲36.5	70	4.15
ERA-6SM	DC-4000	11.3	▲17.9	8.4	▲36.0	70	4.20

Note: Specs typical at 2GHz, 25°C. Exception: ▲ indicates typ. numbers tested at 1GHz.
* Low frequency cutoff determined by external coupling capacitors.
① Price (ea.) Cty.1000: ERA-1 $1.19, -2 $1.33, -3 $1.48, -4, -5 or -6 $2.95. SM option same price.

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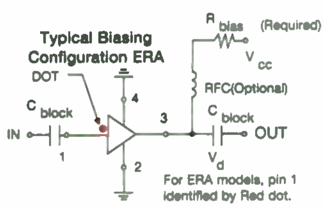
120x60	.002, .047, .068, .1 µf

ERA-1 ERA-1SM
ACTUAL SIZE

Typical Biasing Configuration ERA



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Circle 522

RS-232 Stepper Control Exhibits Versatility

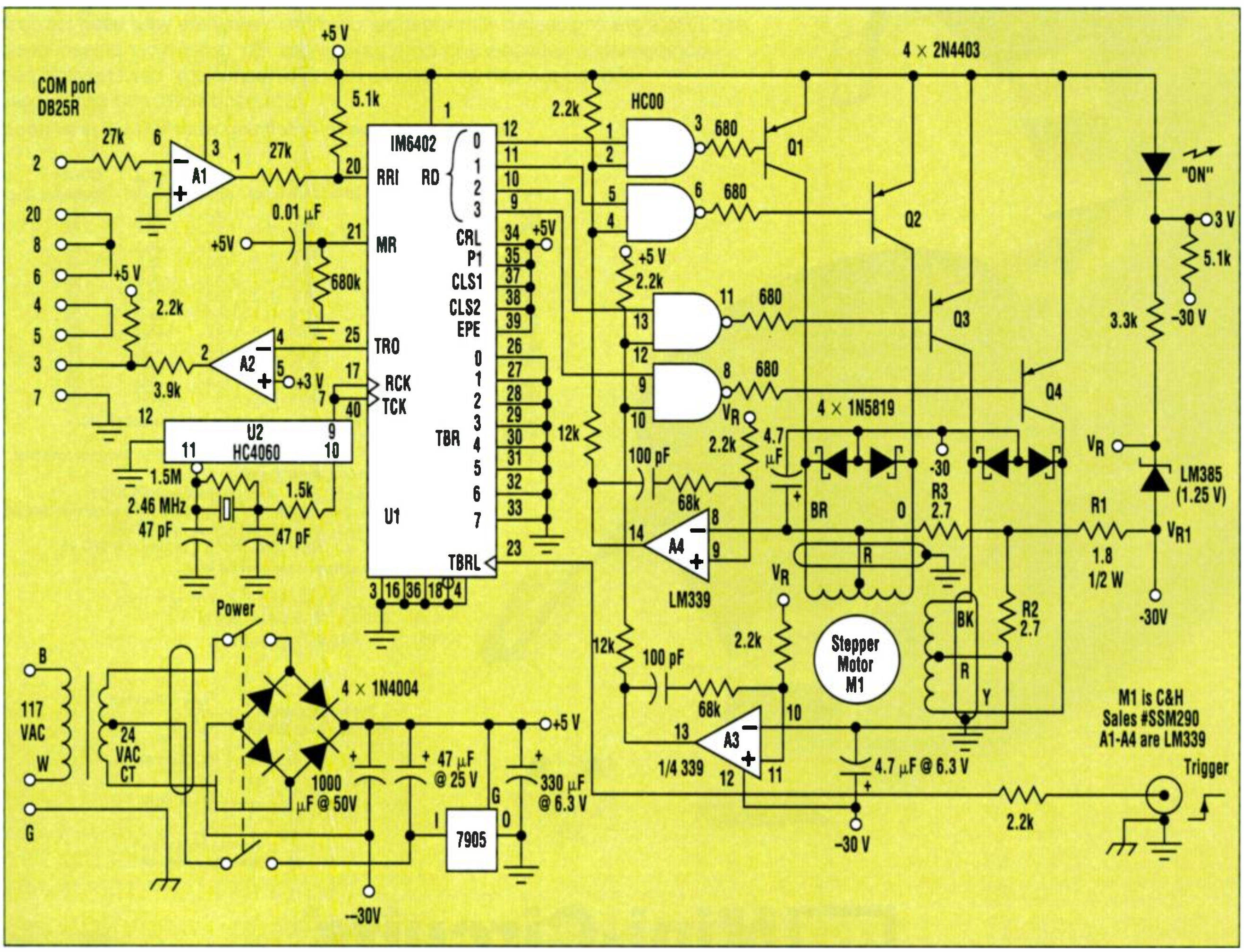
W. STEPHEN WOODWARD
Venable Hall, CB3290, University of North Carolina, Chapel Hill, NC 27599-3290; Internet: woodward@net.chem.unc.edu

A number of "smart" motion-control chips, commonly called "indexers," are available that will do a bang-up job of generating accurate ramps and slews in stepper-motor-driven actuators. But if the motion profile demanded by an application is really peculiar, such as a trigonometric cosine curve (like that in this application example), the convenience of use evaporates quickly.

The circuit shown uses an inexpensive universal asynchronous receiver/transmitter (IM6402 UART) and a few additional devices to allow precise timing of step-by-step motor control via PC generation of RS-232 character sequences *(see the figure)*. Timing of arbitrarily complex step sequences will be as accurate as the crystal-controlled COM port baud rate (<< 0.1%), even when controlled from a "sloppy" programming environment such as interpreted BASIC.

Control of individual stepper stator windings is achieved by connecting UART output bits directly to the motor drive circuits. Thus, by transmitting the appropriate ASCII character, motion-generation software can specify any combination of winding excitations. Carefully generated sequences of characters can therefore produce any desired sequence of steps. Clockwise full-speed rotation of the armature through a complete eight half-step cycle would be produced, for example, by transmitting the character sequence: "IAEDFBJH". Counterclockwise rotation results from simply reversing the character order: "HJBFDEAI".

The phase-drive circuits illustrated implement pulse-modulated constant-current via resistors R1, R2, and R3, and comparators A3 and A4. The specific circuit topology used



An inexpensive UART combined with a few other devices makes possible the precise timing of step-by-step motor control by implementing PC-based generation stepping waveforms directly from carefully selected RS-232 character sequences.

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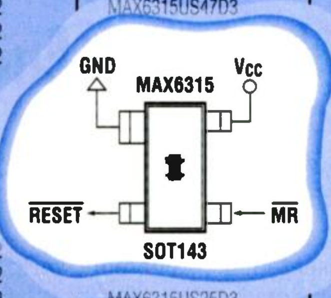
4.9	MAX6315US49D1	MAX6315US49D2	MAX6315US49D3	MAX6315US49D4
4.8	MAX6315US48D1	MAX6315US48D2	MAX6315US48D3	MAX6315US48D4
4.7	MAX6315US47D1	MAX6315US47D2	MAX6315US47D3	MAX6315US47D4
4.6	MAX6315US46D1	MAX6315US46D2		MAX6315US46D4
4.5	MAX6315US45D1	MAX6315US45D2		MAX6315US45D4
•	•	•		•
•	•	•		•
•	•	•		•
3.1	MAX6315US31D1	MAX6315US31D		MAX6315US31D4
3.0	MAX6315US30D1	MAX6315US30D		MAX6315US30D4
2.9	MAX6315US29D1	MAX6315US29D		MAX6315US29D4
2.8	MAX6315US28D1	MAX6315US28D		MAX6315US28D4
2.7	MAX6315US27D1	MAX6315US27D2		MAX6315US27D4
2.6	MAX6315US26D1	MAX6315US26D2		MAX6315US26D4
2.5	MAX6315US25D1	MAX6315US25D2	MAX6315US25D3	MAX6315US25D4



TO ORDER[1]: Fill in as part of the product name suffix:

A. 25 to 50 for the reset trip threshold needed (2.5V to 5.0V)
B. 1 to 4 for the reset timeout delay needed (1 for 1ms, 2 for 17ms, 3 for 140ms, 4 for 1120ms)

In the example, reset trip threshold is 4.6V and reset timeout delay is 140ms.
These products are trimmed at die sort to the different reset trip thresholds and timeout delays.

Example:
MAX6315US46D3
25 to 50
1, 2, 3, or 4

1) Contact factory for minimum order sizes.
Sample quantities are generally available on the following versions: MAX6315US44D1, MAX6315US26D1, MAX6315US44D2, MAX6315US26D2, MAX6315US46D3, MAX6315US44D3, MAX6315US31D3, MAX6315US29D3, MAX6315US26D3, MAX6315US44D4, MAX6315US26D4.

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MAXIM

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Circle No. 158- For U.S.Response
Circle No. 159- For International

```
' Linear Actuator Test Software
' W.S. Woodward

OPEN "COM1:9600,N,8,1,BIN" FOR RANDOM AS 1
1010 INPUT "Enter Length of Excursion in Millimeters...0-22 ", M
    INPUT "Enter Speed Coefficient...0-1 ", S
   GOSUB 10000 'Build motion-control sequence-string
   PRINT "READYSETGO"

1040 x$ = INPUT$(LOC(1), 1): ' Clear out buffer
    x$ = INPUT$(1, 1): PRINT #1, ext$;' Wait for trigger, then extend
    x$ = INPUT$(LOC(1), 1)
    x$ = INPUT$(1, 1): PRINT #1, ret$:' Wait for trigger, then retract
    IF INKEY$ = "" THEN 1040
GOTO 1010

10000 ' Half-Cosine Move-String Builder Subroutine
    ' Enter with M=Length of move in millimeters
'     ... S=Speed Coefficient: 0<S<=1
    ' Exit with EXT$=Extension String ... RET$=Retraction

ST$ = "IAEDFBJH": ' List of Extension-Motion Half STep States
ext$ = "": ret$ = "" HAM = 10.7 * M: Q = S / HAM

FOR I = O TO 3.14159 / Q
    Y = HAM * (1 - COS(I * Q))
    NXS$ = MID$(ST$, (Y AND 7) + 1, 1): ext$ = ext$ + NXS$
   ret$ = NXS$ + ret$
   NEXT

RETURN
```

here, in which a portion of the sense resistance (R2, R3) is independent for each winding pair, and a portion (R1) is common to both, maintains constant motor power dissipation over the half-step excitation sequence. This works by reducing the winding current by a factor of $(R1 + R2)/(2R1 + R2) = 4.5/6.3 = 0.71 = 2^{-1/2}$ for those steps where both windings are driven simultaneously.

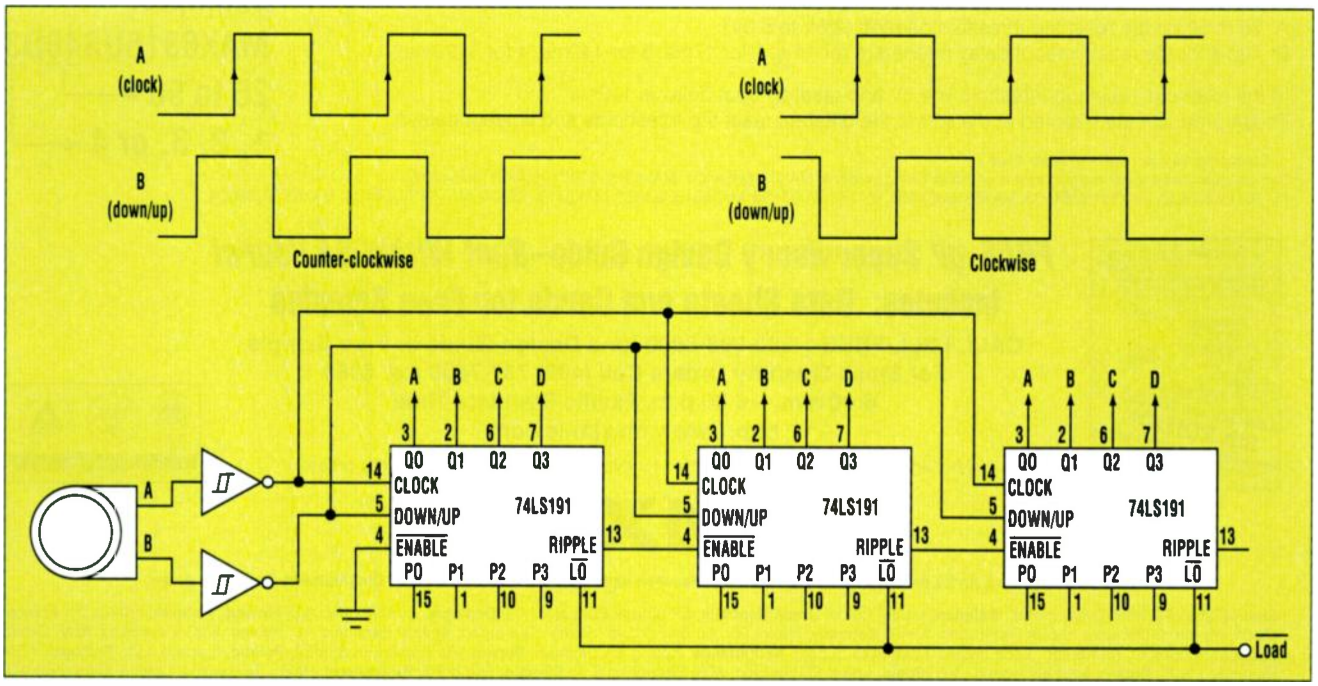
The Airpax Inc. linear actuator mentioned in the schematic (C&H Sales, stock number SSM9201) produces a movement of 0.001 inches per half-step at rates of up to 960 Hz, and was used with the circuit and example program *(see the listing)*.

Circle 523

Improved Rotary Encoder

MICHAEL ECK
Computer Designs, 71 Hillcrest Rd., Martinsville, NJ 08836;
(908) 356-5838; fax (908) 805-0731.

Although the design presented in "Rotary Encoder For Servo-Loop Apps," (ELECTRONIC DESIGN, *Sept. 16, 1996, p. 99)* will undoubtedly work, a more elegant solution for interfacing an encoder to a counter is to simplyuse the 74LS191 counter IC. This chip has a single positive-edge-triggered clock and a DOWN/UP mode control pin *(see the figure)*. When connected as shown, the rising edge of the clock always occurs while the mode control is high during counter-clockwise rotation, causing the counter to count down. Conversely, during clockwise rotation, the rising edge of the clock occurs when the mode control is low, causing the counter to count up. Using this IC completely eliminates the need for the 74LS73 in the original design.



An improvement on a previously published Idea For Design, this rotary encoder employs a single positive-edge-triggered clock and a DOWN/UP mode control pin. It eliminates the need for the 74LS73 in the original version.

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15.5mm² Area

8-SO
1.75mm Height
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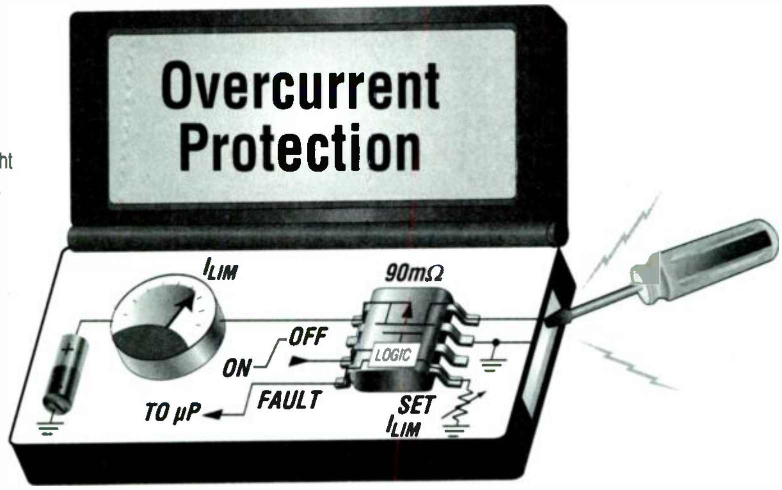

An external resistor sets the switch current limit to protect the battery against shorts or surges.

- 90mΩ On-Resistance (at 3V)
- User-Set Current Limit: 30mA to 1A
- Thermal Overload Protection
- Very Small Size
- 10μA Supply Current
- 0.1μA Shutdown Current
- 2.7V to 5.5V Input Range

PART	R_{ON} (Ω)	MAXIMUM CURRENT (A)	SINGLE/DUAL	PACKAGE
MAX890L	0.09	1	Single	8-pin SO
MAX891L*	0.15	0.5	Single	8-pin μMAX
MAX892L*	0.3	0.25	Single	8-pin μMAX
MAX894L	0.15	0.5	Dual	8-pin SO
MAX895L	0.3	0.25	Dual	8-pin SO

* Future product—contact factory for availability.

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Circle No. 160- For U.S.Response
Circle No. 161- For International

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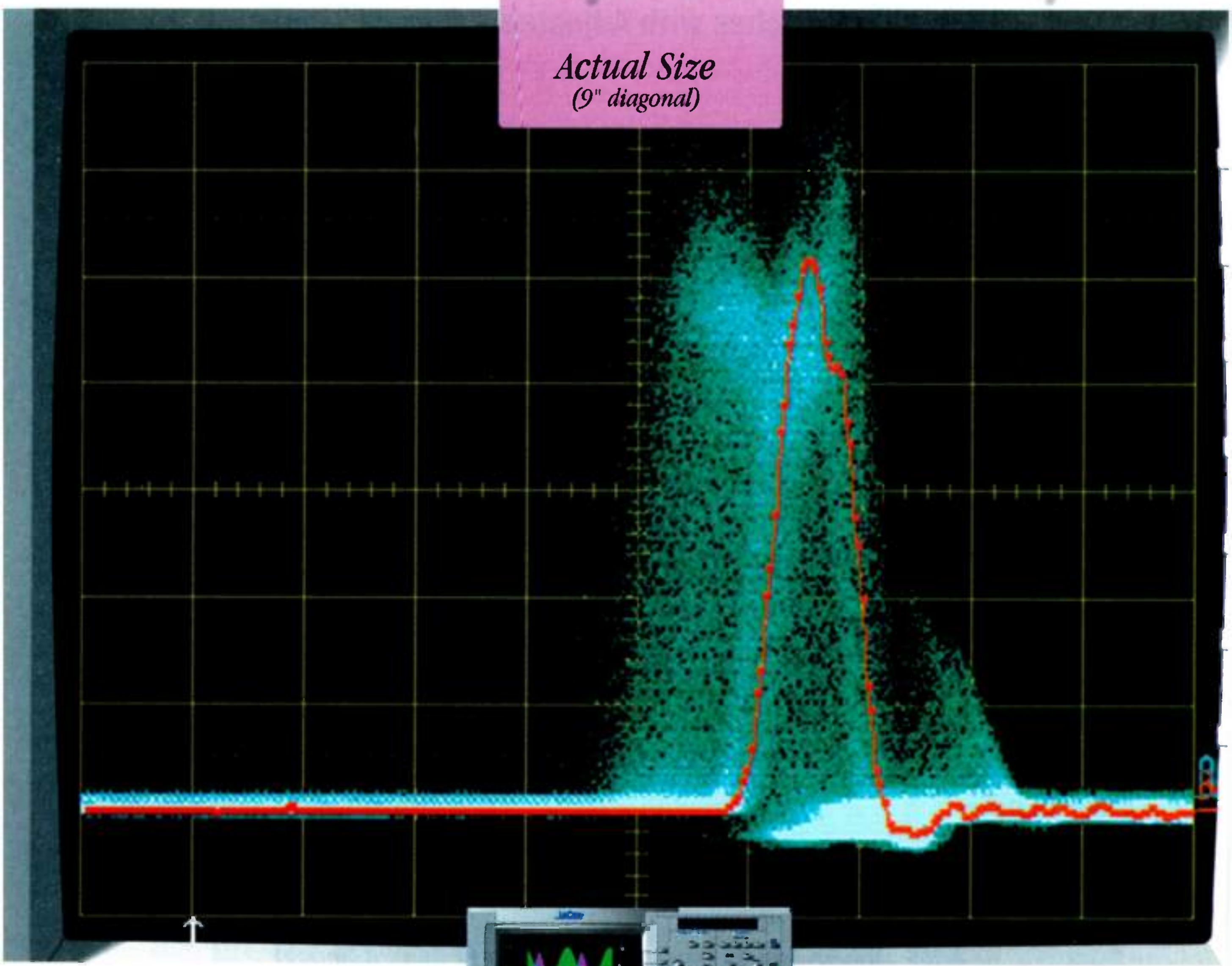

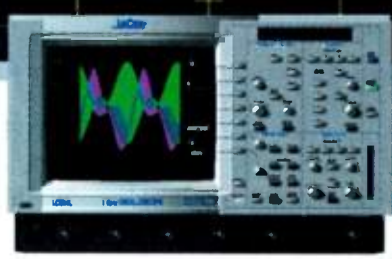

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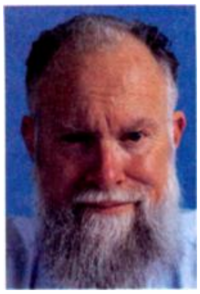
READER SERVICE 157

BOB PEASE

What's All This FLOOBYDUST Stuff, Anyhow? (Part 5)

A JACK-KNIFE is Handiest when at Hand: I have carried a pretty good jack-knife for about 50 years. But it wasn't the *same* jack-knife, it was about 40 different knives. Obviously, it's easy to lose a jack-knife, or leave it behind. I've done it dozens of times. It is not just annoying because it's expensive to buy the replacement knife; you may have to wander around without any knife for a while until you have a chance to buy one. (You can *partly* alleviate this by buying 2 or 3 knives when they are on sale....)

Recently, my friend Will Frangos said, "Take a look at my Swiss-Army knife. Have you ever seen one with a blade this narrow?" I agreed; it looked like he had been using it and sharpening it for many years. He explained that he, too, always used to lose his knife, every few months—but he decided to tie it to a cord, a tether tied to his belt, so it would not get lost. Consequently it was going strong after 10 years.



BOB PEASE
OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

I thought about that, but I didn't like the idea of a simple cord. If it was long enough to let me do useful work, the cord would be too floppy and bulky. I remembered the retractable cable for keys that key shops sell. I bought one. The legend stamped onto its back reads: " 'KEY-BAK', US Patent 2732148. Mfd. & Exported by West Coast Chain Mfg. Co., Box 9088, Ontario Canada. Distributed by CTL Co., Wausau WISC. Assy. in Mexico." This little reel, about 2-in. diameter by 1/2-in. thick, and weighing just 2 ounces, clips on to my belt.

When I need my knife, this cable reels out of the reel, as much as 4 feet. When my work is done, the cable reels back in. In addition, I put in a double strand of black shoelace to link from the knife to the cable. Then, when the cable is all the way up, the knife sits comfortably in the bottom of my pocket. I won't be buying very many knives for a while. If you like to carry a jack-knife, I can recommend this.

I got a copy of that old patent. The original design had a light chain. The newer version with the cable seems nicer. Some key stores sell that "Key-Bak" for about $14. Others sell it for $8. Whatever.

A while back, I had a dream where I was trying to protect a couple of old ladies from a vicious snarling, threatening monkey. I got out my jack- knife, and I confronted the monkey. Soon the monkey made a savvy move, and bit my hand—and grabbed the knife. But not for long, as he did not comprehend the return spring that brought the knife back to me before he could bite the shoelaces. Even in dreams, a jack-knife is a handy gadget....

MEASUREMENT ERROR? NO, a thinking error. A while back, in my Measurement Stuff Column, I said that my thumbnail was 12 milli-inches thick—and thus just 0.45 millimeters, not a whole millimeter as the Trivia Man said. One reader caught me up: "Bob, 12 milli-inches is NOT 0.45 mm, it is 0.3 mm." I went back and checked my math. Obviously, I had divided by 25.4, when I shoulda divided by 39.37. That's pretty dumb!

I *usually* am careful to start out: "1 meter is 39.37 inches, and 1 cm is 39.37 centi-inches, and 1 mm = 39.37 milli-inches. Then 0.3 x 1 mm would be about 12 milli-inches." IF you start from basic definitions, and use CORRECT dimensional analysis, you can avoid being fooled. I recommend good dimensional analysis. More later.

NOTE: While we all know 5280 feet is a mile, it is also useful (and convenient) to know that a kilometer is about 3280 feet, so when you are working with elevations, you can work with that. A mountain at 3,000 meters is 3 × 3280 feet high, or about 9840 feet. Much more precise and useful than "0.62 mile."

However, it is a surprise to find that 3280 feet and 10 inches is EXACTLY 1 kilometer. Not just approximately, or within a couple ppm, but EXACTLY. (Note, 2.54 cm is NOT exactly an inch. It's exactly 2 ppm shorter than an inch.)

When we did the Column on Measurements, a few months back, Roger Engelke, formerly the Chief Copy Editor at *Electronic Design* was horrified by my usage of "milli-inch," because he could not find it in any dictionary. But we got it published, anyhow. If he sees "centi-inch," he'll just DIE.

Maybe I should explain about the "ranchette." The "ranchette" is a unit of area defined as 1/2 pico-acre. The ranchette is exactly the size of a round emitter 1.0 milli-inches in radius (well, 0.9983 milli-inch), so it really is handy when dealing with large matched pairs of transistors. NO, I did not invent the "ranchette." I read about that, years ago. Yeah, let's include this and give Roger a hard time. Meanwhile, does anybody know to whom we should give "credit" for inventing the "ranchette?"

LAPTOPS— OKAY, you have seen me swap letters back-and-forth with several guys who talked about the advantages of the Tandy Model 100 or Model 102. And you know my opinion of hog-at-the-trough Pentium computers, fancy window-type formats, and power-hungry color LCD displays. (Heck, I cannot type at 166 MHz, 66 MHz, 66 kHz, or even 66 Hz. How about you?)

So you won't be surprised to hear that I got me a Model 102 from one of my readers who was going to give his to the Salvation Army. I figured that anybody who bought it at the Salvation Army would not know what it's good for. But I would. So I made it a home.

Good news—the keyboard is fullsized, and QUITE adequate and comfortable. NOT chiclets. Good news—the version with the full "32k" has an actual 29 kbytes of memory available, which is usually enough for an all-typing weekend or a 3-day business trip. Excellent news— the battery life (4 alkaline AA cells) is over 16 hours, and I can fill it up with 28k of typing in less than that.

The display is just 8 lines by 40 characters, but I can live with that. Moving around on the display is not very quick—but it's livable.

The little $10 cable and the $20 software that you need to transfer a file into a PC are a piece of cake. Its Word Processing system is quite adequate, and sufficiently user-friendly. Not a bad machine. The Model 102 weighs just 3 lb, slightly less than the older Model 100. It's like new. It will probably last forever.

If you are interested in a good old Model 100 (ballpark of $250) or a clean Model 102 (about $450), contact Richard Hanson. You can e-mail him at *richard.hanson@pcld.com*; or fax to (510) 937-5039; or phone to (510) 932-8956; or write to Club 100, P.O. Box 23438, Pleasant Hill, CA 94523-0438. These computers USED to be cheap, but now as they are getting better appreciated, the prices are going up. What that means is that Mr. Hanson will be able to make enough $ to keep them running for over 5 or 10 years more. I'll cheerfully pay to make sure that happens.

POSTAGE BY THE OUNCE—Recently, I got a letter from a guy asking for the answer to last year's April Fool's question on zenering the emitter of a transistor. He was nice enough to put in a SASE for my convenience. BUT he put two stamps on it. Well, perhaps he could not be POSITIVE my reply would not be over 1 ounce, so he put on two stamps.

Then I looked at his letter to ME. He put two 32-cent stamps on *that*, TOO—and he just had two pages in it. Hey, I like our postal service pretty well, but I hate to pay them *double*. I like to put just enough STUFF into my envelope to bring it up to 0.95 ounces, or 2.95 ounces, or whatever. I like to get my money's worth whenever I send a letter. That often requires me to leave out a couple clippings that will be sent later. When I am sending JUNK, I have to weigh it. But when I am just sending letters, I know that 4.8 pages of ordinary photocopy paper, when put in an NSC envelope, weighs just under 1 ounce. If I want to send 10 pages, that's still under 2 ounces, and costs 55 cents. NOTE: A lot of people know that the second ounce (and each succeeding ounce) does not cost 32 cents—it just costs 23 cents. So 7.9 ounces will cost 8 × 0.23 + 0.09, or $1.93. This is easily done with six 32-cent stamps *plus* a 1-cent stamp. It's a lot cheaper than just throwing on EIGHT 32-cent stamps.

(But when you get up to 13 ounces, which sounds like it should cost $3.08, STOP. From 13 ounces to 2 lb, it is a flat rate of $3.00, for First Class mail ("priority mail" = air mail.))

Postage for AIR Mail to overseas locations does cost 60 cents for the first half-ounce, BUT only 40 cents for the second half-ounce. So a full 1.9-ounce letter costs $1.80—NOT $2.40. The post office does not publicize this very much.

Mail to Canada is 46 cents for the first half-ounce, and 52 cents for the first ounce. From there on it is nonlinear: 72 cents for 1.99 ounces, and 95 cents for 2.99. Postage to Mexico is nonlinear, too.

A friend once sent me a letter with 78 cents worth of stamps—enough postage for 2.9 ounces. But the letter did not seem heavier than 2 ounces. I weighed it. It was about 1.95 ounces—and 55 cents shoulda been enough. I called him up and asked why he put on 78 cents. He said he checked it at his company mailroom, and it was just *over* 2 ounces. I suggested he should get those scales checked for calibration. He did, and they were right on. So was MY scale—right on.

We figured out later he was in a damp, humid climate. By the time his letter got to me, it had gotten enough drier to have fallen from 2.05 ounces to below 1.98 ounces. If you live in a damp place, and if you had a letter that was just 3.02 ounces, and if you only had 78 cents of stamps, you could put the envelope in your toaster-oven at 150 degrees for a couple of minutes. Then it would drop down below 3 ounces, and would go legally for 78 cents instead of $1.01. This is not always a great way to save money, but if you are about out of stamps (and if you have already snipped off the borders of the paper) this is a possible way to get the weight down just a little.

But, in general, as a rule of thumb, if your envelopes are not extremely heavy, you can mail AT LEAST 4 pages, and usually 4-1/2 pages, of ordinary paper, for 32 cents. If you have random stuff, you could check to see if it weighs less than 9 new zinc pennies (pennies made after 1985)—and THAT would be less than an ounce. Okay? If you are not sure, make up an envelope full of stuff that ought to weigh 1 ounce, and take it to the post office, and fiddle with the contents until it weighs just 1 ounce. You can keep that letter and use it for calibration. Calibrate your scales, and save money.

By the way, how often do you readers write a small P.S. on a small piece of paper, fold it over 3 or 4 folds, until it is like a popsicle stick, and *poke* it into an envelope, along the glued joints, after you sealed it? I do it often.

MOISTURE DETECTOR—Recently, I had a drain clog, and my dishwasher started to pump water all over my kitchen counter and onto the floor. After I cleaned up the puddles, I decided to make a moisture detector. I just happened to have around a couple of 12-V "buzzers." I tried four different buzzers from Radio Shack: Models 273-055A, 273-059, 273-029, and 273-060. These are all adequate as a beeper or noisemaker, and all are priced reasonably at $2 or $3.

I took an old 9-V battery and some old copper-clad, and a little 9-V connector (that I'd salvaged out of the top of a dead 9-V battery). I got an old piece of wire (that was the handle for a Chinese-food take-out basket). I decided that was JUST stiff enough and just springy enough. I soldered it to two separated areas on the copper-clad (where I had sawed with an old hacksaw to insulate them.) The two separate wires I adjusted so they would short out, with normal spring-loading. Then, I put an aspirin between the two wires. When the aspirin got wet, the wires would short out—and the buzzer would buzz.

My wife said, "The aspirin won't dissolve. It takes stomach acid to dissolve the aspirin." I told her I had always heard aspirin was good for this. So I put some water on the aspirin as a test. Sure enough—the beeper began to beep—in about 10 minutes. Not the response time I wanted!! But a half of a

sugar cube works better and faster. It collapses and fires in about 6 seconds. The only minor problem I foresee is if I put this in a cellar to detect for leaks, would dampness cause any false alarms? Or would the ants attack it? Still, it could help warn about problems with leaks or water-heater failures.

THERMOCOUPLES?? A friend asked me what kind of a thermocouple puts out 700 mV, like the one in his gas stove? Well, we know that does not run at 2000°C, so it must not be any ordinary 40 μV/°C thermocouple. It probably uses some kind of exotic metals or semiconductors. Can anybody tell me what is used in them? I'd like to know. It is obviously not a thermopile or *stack* of several thermocouples.

SMOG, REVISITED—I got a lot of information (and a lot of disinformation) about smog. To this day, the State of California (and almost all the "media") do not give a fair or correct definition of what a "gross polluter" is, nor do they talk about the best way to avoid having your car declared one—by getting it adjusted and repaired and tested before you take it in for the official tests. SIGH.

We DID learn that the State of California cannot confiscate your car just because it does not pass a smog test. HOWEVER, in some *cities*, such as San Jose or Santa Cruz, they have "abatement programs." The local "abatement officer" can "abate" your car right out of your driveway, if it is not registered, and can scrap it, and take the $3000 abatement charge, and sell it to some darned refinery or other polluter. Wonderful....

(Heyyyyy — a car that is not registered, and is not on the road, does not emit any smog *at all*. How come they think they are cutting smog by junking such a car????)

TIP: If you buy some shoes, and you like them, go back and buy another pair before you forget. If you wear the two pairs of shoes alternately, they will last longer. And, that way, you won't be cross to discover, when they are worn out, that you cannot buy them any more!

A friend brought in his new GPS receiver, and we went out in the parking lot to compare his data to mine. Sometimes *his* receiver made a 50-meter *lurch*—and mine didn't. Sometimes *my* receiver made a 40-meter *jump*—and *his* didn't! I surely was not expecting that. I had expected many of the lurches to be the same! Still, both gave acceptable accuracy. (Even if they did both list the elevation at –100 or –180 feet.) And they'll get better in a couple years when the Air Force turns off the noise. But, beware, as it is claimed that some older GPS receivers may experience "millennium" problems as early as August 1999.

BOOK REPORT—I got a good book in the mail yesterday, written by Jim Smith (of Cambridge Management Sciences, formerly The Phoenix Group) about Quality. He debunks a lot of myths about Quality. He explains why certain "Quality" procedures are good, and others are bogus. I am recommending to our librarian to get a copy or two. It is a big book, 520 pages: "Optimizing Quality in Electronics Assembly: A Heretical Approach," by James Smith and Frank Whitehall (McGraw Hill). Costs about $50.

I haven't found too many places that deal with the design of ICs, as it mostly deals with the assembly of ICs. So it should be of great value to our customers, and to us, when we are communicating with our customers.

Good writing. He points out the flaws in "the customer is always right, so give the customer the Quality he asks for." He DISMANTLES the Six-Sigma theories. He sorta likes a lot of the ideas of Juran, Deming, Crosby, and Feigenbaum—but not ALL of their ideas. I was pleased to see that he likes about ALL the ideas of Eliyahu Goldratt (*The Goal*). Conversely, he does mention Genichi Taguchi and his methods. He then prints some nice excerpts of how I was able to show that Taguchi's "optimal" regulator was not regulating at all (ELECTRONIC DESIGN, *June 10, 1993, p.85*). Anybody who is that realistic about Taguchi, and who is VERY SKEPTICAL of ISO 9000, I gotta like. A lotta good stuff in there. I have not finished reading all of it, but I've read half and skimmed the rest.

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

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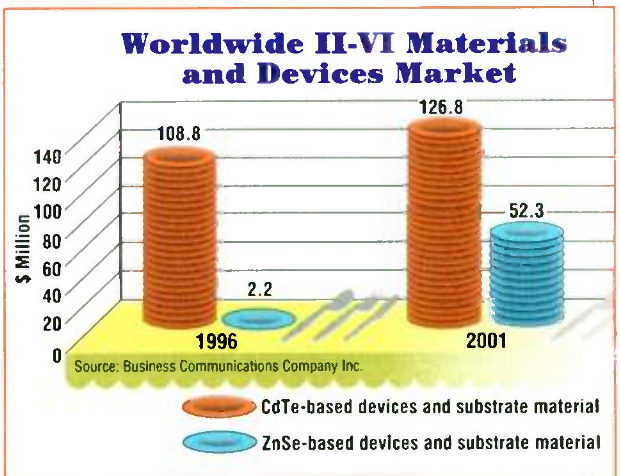
ELECTRONIC DESIGN QUICK LOOK

■ Edited by Mike Sciannamea and Debra Schiff

MARKET FACTS

Setting The Periodic Table

Contrary to the doommongers who said that silicon would have the shelf life of an apple pie, the material appears to have the lasting power of a twinkie. Despite the shrinking price tag of DRAMs, the semiconductor industry continues to soar, with silicon as the leading material in semiconductor devices. Because semiconductors have become far more functional, more companies are investigating alternative materials to compliment silicon. One of the biggest markets for these materials is wireless devices. With frequencies swinging out of the range of silicon functionality, wireless products are providing a breeding ground for silicon alternatives. In a new report from the Business Communications Company, "RGB-196A, Surging Markets for Silicone Alternative Materials: II-VI Materials and Devices," two standouts, cadmium telluride (CdTe) and zinc sellenide (ZnSe), are showing the power of niche material marketing. Predicting the growth of CdTe-based devices and substrate material, the report expects that market will expand from $108.8 million in 1996 to $126.8 million in 2001. The average annual growth rate for CdTe materials is estimated at 3.1% in the period between 1995 and 2001. CdTe has found its niche in the infrared radiation (IR) detection market. One drawback, though, is that in designing IR detection systems based on CdTe, engineers must take into account that these materials must be kept cool to operate effectively. Spurring competition, companies are researching new systems for room-temperature operation based on other alternative materials. CdTe materials manufacturers also are attempting to design room-temperature capable systems. The ZnSe materials market is estimated at $2.2 million in 1996 and projected to explode to $52.3 million in the first year of the next century. The average annual growth rate, according to Business Communications, is 85%. Classified as another niche market material, ZnSe is primarily used in blue-light emission. With the bulk materials now available and the blue diode laser problems fixed, ZnSe appears to be a player in the blue LED scene. Another alternative material compared to silicon in the report is gallium arsenide (GaAs). In pitting the alternative against silicon, the higher energy-band gap (1.4 eV) and electron mobility (6000+ cm^2/V-s) stood out for GaAs. Silicon's energy band gap measures 1.12 eV, while its electron mobility clocked in at 1300+ cm^2/V-s. Lowering GaAs' carrier concentration and raising resistivity, the higher energy-band gap allows fabs to produce a more isolated device. Continuing the debate from the silicon side, GaAs takes about three times as long to dissipate heat than silicon. But, the alternative material, with electrons moving five times faster than silicon's runs at lower power and produces less heat. When it comes to high temperatures, though, silicon wins. Even at 1000°C, single-crystal silicon wafers barely change. GaAs, on the other hand, starts to decompose at 600°C, dropping arsenic along the way. Just for a quick chemistry rehash, Group II elements are zinc, cadmium, and mercury. Group III elements are aluminum, gallium, and indium. Elements found in Group IV are carbon, silicon, and germanium. Group V elements are nitrogen, phosphorus, arsenic, and antimony. Finally, the two elements in group VI are selenium and tellurium. Elements in Group IV may be used in pairs or on their own, while elements in the III and V Groups and those in the II and VI Groups must be paired together. The RGB-196A "Surging Markets for Silicone Alternative Materials: II-VI Materials & Devices" report discusses the different combinations and the devices made from them. For more information, contact Business Communications Company Inc., 25 Van Zant St., Norwalk, CT 06855; (203) 853-4266; fax (203) 853-0348; Internet: http://www.buscom.com.—*DS*



40 YEARS AGO IN ELECTRONIC DESIGN

Solid-State Oscillator for Microwaves

Successful operation of a revolutionary solid-state device, which will oscillate at microwave frequencies, has been achieved at Bell Telephone Laboratories by Dr. Harold Seidel, Dr. Derrick Scovil, and Dr. George Feher (shown in the photo, left to right). The experiment produced oscillations at 9000 Mc with a power output of about 20 μW. Operation at much lower and higher frequencies is possible with proper choice of solid-state materials and operating conditions. Scientists believe it is only a question of time until microwave amplification can be obtained employing crystalline materials and operating under the same physical principles. One of the outstanding characteristics of the device is that it is expected to have very low noise compared with conventional microwave devices.

The development represents the first successful application to a solid-state device of the "maser" principle. "Maser" was first demonstrated for molecular beams in gases in 1954 by Professor C.H. Townes and his collaborators at Columbia University. They coined the word "maser" which stands for "microwave amplification by stimulated emission of radiation." Because it operates with electron spins in a paramagnetic crystal, theory predicts that it should have very low inherent noise compared to ordinary electronic oscillators or amplifiers which depend on the motion of charged particles at high temperatures. Therefore, it may be possible to amplify extremely weak radio signals—signals which may be several hundred times weaker than those usable at present. An as amplifier, it should be moderately broadband with a bandwidth of the order of 100 Mc, and easily tuned since its frequency is proportional to the applied magnetic field. Preliminary theoretical estimates indicate that a noise figure corresponding to thermal noise at perhaps 5 or 10 degrees Kelvin should be attainable. This is hundreds of times better than is now available with conventional microwave circuitry. *(Electronic Design, March 1, 1957, p. 6)*

Limited space prevents us from publishing the article in its entirety, but it does mention that the crystal is made of gadolinium ethyl sulphate immersed in liquid helium at reduced pressure, providing a temperature of 1.2 K.—SS

New Books: Electrons, Waves and Messages, John R. Pierce, Hanover House, Garden, City, N.Y., 318 pages, $5.00

Chances are that you will be fascinated and illuminated with these lucid, intellectual descriptions. Why do you sometimes get "snow" in your television picture? Will a machine ever be able to write detective stories? Can people in a rocket ship be kept from freezing, and will you be able to talk to them on a telephone? The answers to these questions and the why of the answers are presented in this book. Chapters on electric fields, waves, and Maxwell's equations will no doubt "refresh" the understanding of the brightest engineer. After providing this general background of basic electronic principles and how they are applied, the author discusses amplifiers, television, radiation, microwave systems and the most important problems in electronics. The book contains chapters on communication theory and noise, relativity and the future of electronics. In an entertaining style, Dr. Pierce has attempted to explain electronics to the general reader and to acquaint technically trained people with specialties other than their own. *(Electronic Design, March 1, 1957, p. 179)*

It's undoubtedly dated, but this sounds like a very interesting book, particularly since the author, John R. Pierce, was a science-fiction author (under a pseudonym) as well as a leading satellite communications scientist at Bell Labs. —SS

Y2K UPDATE

Call Peter de Jager*, there's an automated solution to the "millennium bug!"

Like a gigantic flyswatter, Data Integrity has introduced its Millennium Solution for Cobol. The patent-pending technology goes directly into the code, correcting the potential data miscalculations that will arise with the Year 2000 date change.

The Millennium Solution is designed to work only with the lines of code that are directly affected. It does not change program logic, data files, or archival data. According to the company, this technique dramatically reduces the software testing time and cost.

The solution works by using the affected programs' existing data definitions and database structures to find and fix the date code. The Millennium Solution does not require any expansion data or special encoding of fields.

In beta testing, enterprises have applied the solution to their systems, finding fewer than 1% of their lines of code requiring correction. This finding is in opposition to industry approximations of 6% to 12% of lines of code that will have to be changed before December 31, 1998. Companies will need one full year of testing their "fixed" applications, and working out the bugs.

Users of the solution have seen as much as a 35% reduction in total cost. The total time allocated to staff members who dedicated to fixing and testing the date-sensitive programs also was cut.

Also in the works are Data Integrity's Millennium Solutions for PL/1, RPG, and Assembler.

For more information, contact the company at 228 Highland Ave., West Newton, MA 02165; (617) 964-1977; fax (617) 244-2324.

**FYI—Peter de Jager has been a great source of Y2K information. Check out his web site: http://www.year2000.com/cgi-bin/y2k/year2000.cgi.—DS*

QUICKNEWS

NetFRAME has announced that it has joined Citrix System's Industry Solutions Alliance. The Alliance is made up of a coalition of industry vendors who have teamed to develop products specifically for the WinFrame software.

NetFRAME's part in the group will be to supply large-scale, enterprise-class server hardware to host WinFrame. The set up will be designed to deploy mission-critical Windows applications to remote users over the Internet or companies' intranets.

The Windows applications will be hosted on the NetFRAME NF9000 platform. Minimizing downtime, NetFRAME NF9000 will provide users with hardware fault tolerance; software error resilience; and on-line system management, repair, and expansion.

For more information, contact NetFRAME 1545 Barber Lane, Milipitas, CA 9035; (408) 474-1000; fax (408) 474-4100; Internet: http://www.netframe.com.

With a name that sounds like a mouth full of peanut butter, Intel's new MMX technology works off of the Pentium processor, speeding it up 10 to 20%.

Designed to optimize performance on media-rich applications, MMX is available for both desktop and mobile computers. The technology is offered at 166 and 200 MHz for desktop units and 150 and 166 MHz for notebooks.

MMX was developed by engineers at Intel who added 57 new instructions to the architecture. These new instructions are targeted at dealing with audio, graphical data, and video in a more efficient manner. Multimedia operations frequently run highly parallel, repetitive sequences that slow down applications. MMX's instruction set allows users to access multimedia information faster.

Another feature of the new technology it its use of the Single Instruction Multiple Data (SIMD) process. SIMD significantly trims the amount of time it takes to execute an application. In most communication and multimedia applications, engineers use repetitive loops to execute code. In SIMD, however, it only takes one instruction to affect multiple data. This technology is aimed at animation, audio, graphics, and video.

Additionally, Pentium processors that are fitted with MMX technology also have more cache. Doubling the on-chip cache to 32 k, Intel is allowing users to add more data and instructions to the chip. This advance cuts the amount of times the processor has to send for off-chip memory reinforcements.

For more information, contact Intel Corporation, 1900 Prairie City Rd., Folsom, CA 95630-9599; (916) 356-8080; fax (916) 956-5427; Internet: http://www.intel.com.

New from SMART Modular Technologies is a line of 2-Mbyte and 4-Mbyte Flash Miniature Cards. The cards are supported by the Miniature Card Implementers Forum.

The SMART cards are matchbook-sized Flash memory that are suited for advanced pagers, cellular phones, digital audio recorders, digital still cameras, hand-held computers, and PDAs. Applications include transferring still image information to computers for instantaneous printing and bringing audio from a remote source to a notebook for quick editing. The cards are priced at $49.50 for the 2-Mbyte version and $69.50 for the 4-Mbyte card, both in 100 piece counts.

For more information, contact SMART Modular Technologies Inc., 4305 Cushing Pkwy., Fremont, CA 94538; (510) 623-1231; fax (510) 252-7807.

Motorola recently announced the availability of the 68HC705MC4 one-time programmable microcontroller. The microcontroller has an 8-bit dual-channel, high-speed pulse width modulator (PWM) that operates at both 183 Hz to 23 KHz and 122 Hz to 15.6 KHz. In addition, the microcontroller features an 8-bit analog-to-digital converter.

For details on the microcontroller, contact Motorola, P.O. Box 52073, M/D 56-102, Phoenix, AZ 85072; (800) 765-7795; Internet: http://www.design-net.com/csic.

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☐	2	1510-1660	20	0.4	SOIC-8	DS52-0004
☐	3	824-960	18	0.6	SOIC-8	DS53-0001
☐	4	824-960	23	1.0	SOW-16	DS54-0001
☐	4	1200-1660	23	1.0	SOW-16	DS54-0003
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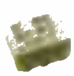

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READER SERVICE 133

OFF THE SHELF

"Win 32 Programming" features comprehensive information on Windows GUI programming, including Windows Controls, GDI, common dialogs, and background processing. Other topics discussed include creating Dynamic Link Libraries, storage management, windows subclassing, and threads. Packaged with the book is a CD-ROM with a C template readers can copy to create their own Windows applications and programs called Explorers written in C++/MF C. The 1582-page book is priced at $55. Contact Addison-Wesley Publishing Co., 1 Jacob Way, Reading, MA 01867; (617) 944-3700; Internet: http://www.aw.com.

"Fundamental Analog Electronics" covers the core material featured in an introductory-level university course in circuit theory and analog electronics for both engineers and scientists. Using a bottoms-up approach, the book begins with components and works its way up through more complex combinations to an understanding of systems. Also included is an introduction to PSpice, along with illustrated examples. Contact Prentice Hall Inc., College Publicity, One Lake St., Upper Saddle River, NJ 07458.

KMET'S KORNER

...Perspective on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
P. O. Box 1070, 100 Prickly Pear Rd., Verdi, NV 89439; (702) 345-1455; fax (702) 345-0804

RON KMETOVICZ
CONTRIBUTING EDITOR

My December 2nd column generated considerable feedback. The column offered two suggestions, which I repeat below, to consider instead of conducting an engineering layoff when a business declines. I recommended:

- •Reducing operating expenses to a minimum.
- •Placing the engineering team on a reduced-work schedule for reduced-pay program.

The measures function for a short period of time, up to six months, and should only be applied when an optimistic vision for recovery exits.

Readers jumped to attention on issues of fairness. What about the management team? Should they take a pay cut? Certainly, a case could be made that mismanagement may contribute to poor business performance. Or what about the marketing team that read indicators incorrectly? It is possible this cast of characters placed the company in dire straits. Maybe the folks in sales could get their act together and do what they were supposed to do? Possibly manufacturing could build it right and sales would go up?

Thinking this way places complex and interactive issues in view. Does the engineering team sacrifice alone while others go on working at full funding and full pay? Certainly not! The column, however, did not comment on those who work outside of new product development. Actions taking place prior to adopting the two recommendations may include:

Reducing the number of managers in proportion to business difficulty. This is done by looking at organization charts while counting the number of layers between the executive staff and the individual contributors. In the not too distant past, four or more layers were visible. Now, reengineering specialists recommend a two-layer structure. One layer consists of the executive staff and the second manages individual contributors. The action virtually eliminates the middle-management structure. Next, the remaining management layer consolidates by placing more decision making responsibility with direct contributors. In theory, the organization empowers those doing the work to guide their own actions.

Systemizing the work previously performed by managers. Concurrent with the management exodus, the remaining managers and contributors learn to apply new systems and tools to perform routine managerial duties. The systems and tools, most based on database structures, rely on the input of quality data. Data manipulation over company networks then makes it possible to serve the information needs of executive managers, managers, and individual contributors. Caution is advised here. The systems and tools must equal, or exceed the performance of the managers being replaced, at reduced cost. If not, remaining participants should expect continued business erosion.

Managers setting the example by taking a reduction in pay. Managers do what they ask of their employees. If working with less for less is the order of the day, they lead by example.

The company must have a vision on how to work its way back to prosperity. If the vision exists, and it includes new products, then the application of the two recommended actions places the business in an excellent position to recover. The business' likelihood of returning to prosperity lives with its product developers. The actions outlined preserve this fundamental corporate asset to set the stage for recovery. Hopefully, the distribution of the unavoidable pain and suffering retains some degree of fairness.

To obtain an e-mail copy of "The Complete List of Reasons for Late Product Information," contact Mr. Kmetovicz at kmetovicz@aol.com.

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"Frankly, it's exactly what you'd expect from a Nintendo/NEC partnership. I just can't stress enough what a phenomenal job NEC does of keeping an eye on your bottom line. NEC clearly understands that every penny counts. In fact, they were able to reduce the number of pins. And in case you didn't know, every pin is another million dollars in our business.

"But it also means a lot to the kids. You see, the V_R Series processor is an evergreen design. So it won't be obsolete in two or three years. And that means Nintendo 64 devotees can put their allowances towards other things. Like buying books or planting trees. And hey, maybe they'll even buy a few more games."

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FREE STUFF

The Institute of Electrical and Electronics Engineers (IEEE) has released the updated printed and electronic versions of its 1997 Standards Catalog. The catalog features a complete listing of standards publications and IEEE services. It's also a source for new, revised, reaffirmed, and withdrawn standards. To receive a free copy of the catalog, contact the IEEE, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331; (908) 562-3800; fax (908) 562-1571; e-mail: stds-maillst@ieee.org.

Pfeiffer Vacuum Technology Inc. has introduced an interactive vacuum catalog on CD-ROM, free of charge. The catalog section features over 3000 products, accessories, and components. The CD-ROM also contains a glossary of technical terms and data that can help users determine specific requirements for vacuum products and performance. Application areas, technical data, characteristic curve, scale drawing, accessories, and options can be called up and printed. Contact Pfeiffer Vacuum Technology at 8 Sagamore Park Rd., Hudson, NH 03051; (603) 595-3200; fax (603) 595-3250; Internet: http://www.pfeiffer-vacuum.com.

XLNT Designs Inc. has released a new white paper entitled "FDDI to Gigabit Ethernet." This free guide provides end-users and systems administrators with an overview of the technological framework that surrounds Gigabit Ethernet migration. It includes a look at the advancements associated with integrating Gigabit Ethernet into existing networks. The paper also discusses FDDI, and why Gigabit Ethernet is the high-speed networking technology that offers a viable upgrade path for FDDI. To receive a free copy of the white paper, contact XLNT Designs Inc., 1050 Avenue of Science, San Diego, CA 92128; (619) 487-9320; fax (619) 487-9768.

EAO Switch offers customers free samples of the world's smallest PCB slide switches. The switches can be used to replace unreliable wire jumpers, easy to lose shunts, or bulky selectors. The 1K2 slide-actuator switches provide easy circuit selection, even from the outside of an enclosure. With positive detent action, visual position indication, two different actuator heights, and 10,000 operations, these 1K2 "jumper" switches also can serve as a rugged general purpose subminiature slide switch. The 1-pole, 2-position switches feature regular gold contacts for reliable, low-level operation. For a free sample of the slide switch, or more information, contact EAO Switch Corp., 198 Pepe's Farm Rd., Milford, CT 06460; (203) 877-4557; fax (203) 877-3694; Internet: http://www.eaoswitch.com/.

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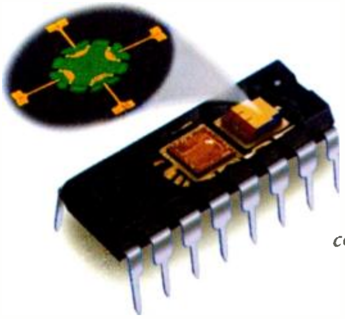
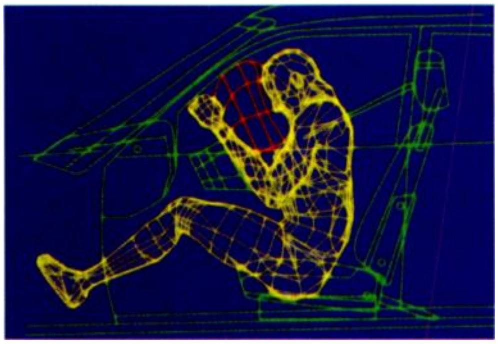
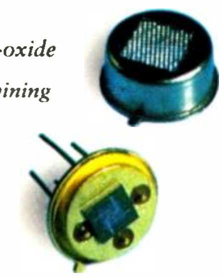


The Senseon™ accelerometer, with a patented, sealed G-Cell packaged in industry standard plastic packages is ideal for automotive systems, computer and industrial products.



Senseon gas sensors combine metal-oxide technology with silicon-micromachining techniques for new gas sensing solutions in homes, offices and industrial facilities.



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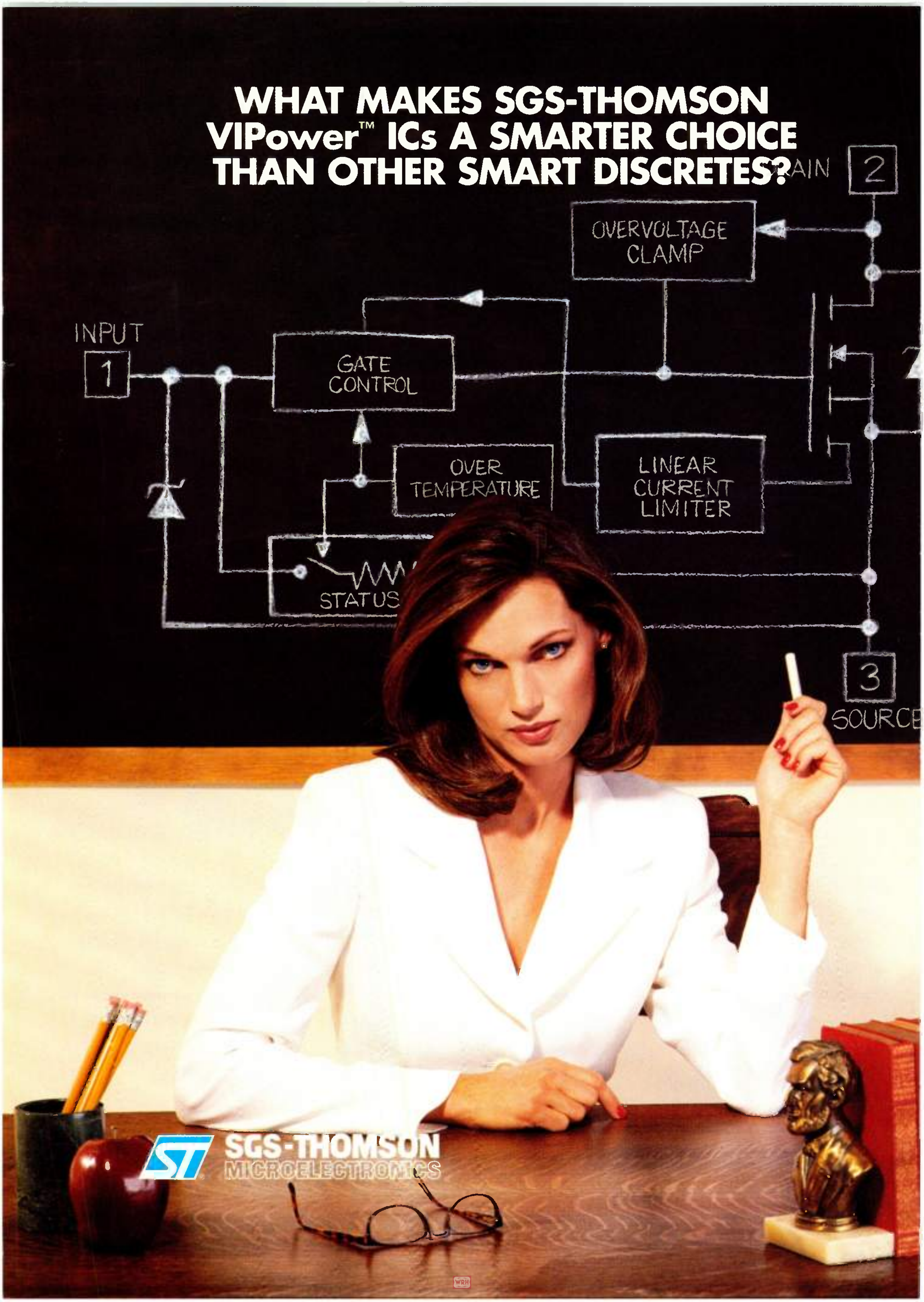

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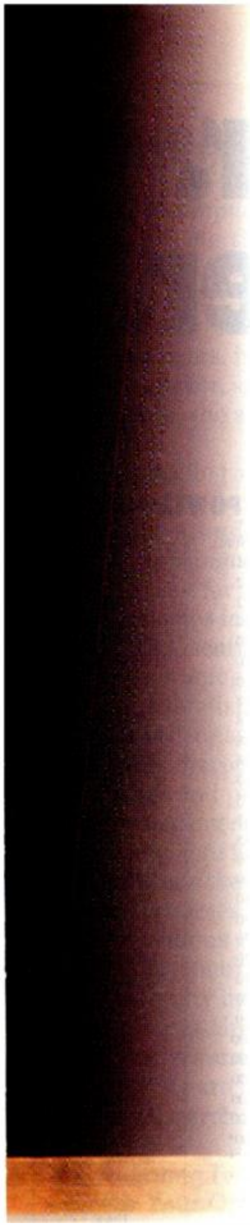

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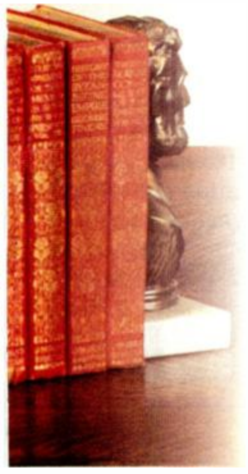
As logic level devices, OMNIFETs offer more features than their predecessors — TEMPFET® and SENSEFET™ — combined. With $R_{DS(on)}$ ranges from 12mΩ to 200mΩ and all industry standard through-hole and surface mount packages available, the OMNIFET product range can meet the most demanding power switching cost/performance parameters.

Do your homework and you'll get a real education on the unprecedented advantages of SGS-THOMSON VIPower devices. Be one of the first 500 respondents and receive a sample kit with complete data and actual devices. Fax 617-259-9442 or write SGS-THOMSON Microelectronics, 55 Old Bedford Rd., Lincoln, MA 01773. And visit our web site at **http://www.st.com**



ST®

Service and Technology

READER SERVICE 148

For More Info Turn Page

THE ENVELOPE, PLEASE

At the Brunswick Hilton, East Brunswick, N.J., on April 15, the Federal Laboratory Consortium will present a total of 30 awards for excellence in technology transfer. The presentation will take place during the consortium's National Technology Transfer meeting.

Out of the more than 650 federal government laboratories and research centers comprising the consortium, the Lawrence Livermore National Laboratory, University of California, Livermore was celebrated three times for work done in the Laser Program.

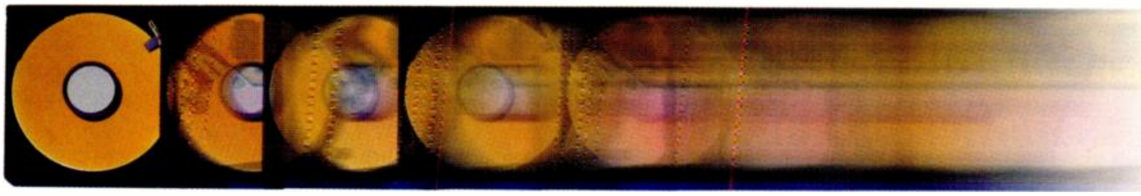
Recognized for their research with Intevac Inc., Rocklin, Calif., laser physicists Luis Zapata and Lloyd Hackel, in addition to former technology transfer official, Damon Matteo, produced a machine to manufacture flat panel displays. Intevac worked an arc lamp and reflector technology from the Lab (that was originally intended for defense applications) into a rapid thermal processor. The processor cut the time of producing flat panel displays from 30 hours to 5 minutes.

Also in the award-winning Lawrence Livermore Laser Program are electronics engineer Tom McEwan and technicians Pat Welsh and Greg Dallum. McEwan's short-pulse micropower impulse radar technology has been licensed to 18 companies over the past three years. The radar was used as an "electronic dipstick" for the measurement of such liquids as chemicals, food, gas, oil, paper, petrochemicals, pharmaceuticals, and pulp.

Last, but far from least, engineers Dino Ciarlo and Glenn Meyer with physicists Hao-Lin Chen and Booth Myers developed a new sealed tube electron beam technology, with the help of American International Technologies. The new tubes cost 10 times less than current systems, are smaller, and reduce X-ray and high electrical voltage exposure.

For more information, contact Lawrence Livermore National Library, University of California, P.O. Box 808, L-404, Livermore, CA (510) 423-3107; fax (510) 423-2943; Internet: http://www.llnl.gov.—*DS*

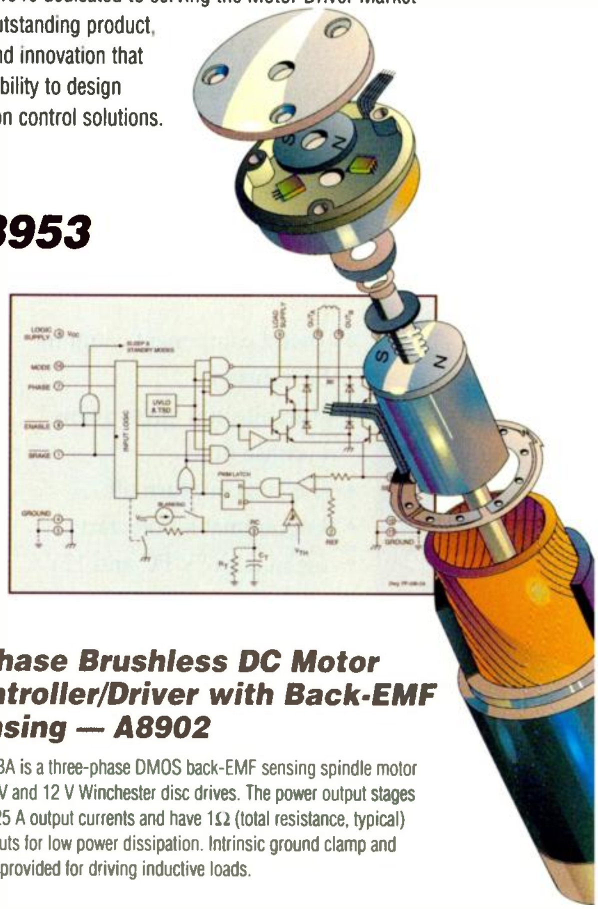
AT ALLEGRO, WE'RE SETTING A REVOLUTION IN MOTION



Whether it's bidirectional control of servo or stepper motors, PWM closed loop current control, back-EMF sensing, or 3 V operation, Allegro sets the standard for today's motion control needs.

Continuing our leading edge tradition, we've just introduced the new A3953 Full-Bridge Motor Driver, designed to provide the optimal bipolar drive solution. The A3953 is ideal for use in any industrial motor driver application which requires bidirectional pulse width modulated current control of up to 1.3 A. Supplied in two package options (16-Pin DIP or 16-Lead SOIC), the A3953 complements our existing line of single and dual full-bridge motor drivers.

At Allegro, we're dedicated to serving the Motor Driver Market by providing outstanding product, performance and innovation that enhance your ability to design complete motion control solutions.



New From Allegro

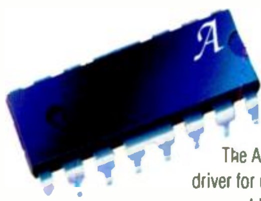
Full-Bridge PWM Motor Driver — A3953

Designed for bidirectional pulse-width modulated (PWM) current control of inductive loads, the A3953S is capable of continuous output current to ±1.3 A and operating voltages to 50 V. Internal fixed off-time PWM current-control circuitry can be used to regulate the maximum load current to a desired value. The peak load current limit is set by the user's selection of an input reference voltage and external sensing resistor. The fixed off-time pulse duration is set by a user-selected external RC timing network. Internal circuit protection includes thermal shutdown with hysteresis, flyback diodes, and crossover current protection. Special power-up sequencing is not required.

- ±1.3 A Continuous Output Current
- 50 V Output Voltage Rating
- 3 V to 5.5 V Logic Supply Voltage
- Internal PWM Current Control
- Saturated Sink Drivers
- Fast and Slow Current-Decay Modes
- Automotive Capable
- Sleep (Low Current Consumption) Mode
- Internal Suppression Diodes
- Internal Thermal Shutdown Circuitry
- Crossover-Current and UVLO Protection

Dual Full-Bridge PWM Motor Driver — A2919

The A2919SB and A2919SLB motor drivers are designed to drive both windings of a bipolar stepper motor or bidirectionally control two DC motors. Both bridges are capable of sustaining 45 V and include internal pulse-width modulation (PWM) control of the output current to 750 mA. The outputs have been optimized for a low output saturation voltage drop.



3-Phase Brushless DC Motor Controller/Driver with Back-EMF Sensing — A8902

The A8902CLBA is a three-phase DMOS back-EMF sensing spindle motor driver for use in 5 V and 12 V Winchester disc drives. The power output stages are capable of ±1.25 A output currents and have 1Ω (total resistance, typical) DMOS power outputs for low power dissipation. Intrinsic ground clamp and flyback diodes are provided for driving inductive loads.

Visit Our New Web Site

Complete information on many of the products offered by Allegro are now right on our web site. You'll find us on the World Wide Web at *http://www.allegromicro.com*.

The Clear Choice for Motion Control Design.

Allegro™ MicroSystems, Inc.

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FLIPPING THROUGH THE INTERNET

http://www.dmcwave.com: Stop off at Digital Microwave Corp.'s site to find the latest information on their line of high-performance digital microwave radios and associated systems and services. Visitors also will find links to other sites with facts on digital microwave technology, and the microwave information center.

http://www.littelfuse.com: Click on this URL to see Littelfuse Electronics' most recent product bulletins and news. The site also gives visitors a part number cross reference, and technical information. Designers looking for specifications on the company's 2029 series of surface-mount PTCs will find them here. Additionally, specifications for the NANO², 0603 SMF, and ALF II surface-mount fuses are here. The Littelfuse pages have current-curve and outline drawings, as well as product literature and technical articles. Circuit protection devices for the automotive, electrical, and electronic industries can be sampled via the sample request form.

http://www.commercialcontrols.eaton.com: Design engineers surfing the web might want to pause at Eaton's Commercial Controls Division site. The web page gives visitors a short look at the division, then proceeds into the newest product announcements, distributor listings, plant locations, and individual product lines. Visitors may request information on power tools, circuit breakers, and switches at the site.

http://www.encad.com: Specializing in wide-format printers, ENCAD has brought its product information to the World Wide Web at top speed. Visitors in need of the latest printer driver, can download it, register it, check out the technical specifications, and request product literature here. In addition to the most current information on the company's printers, ink and media products, and technical support, visitors can find financial reports, the annual report, and stock quotes. Products such as the NovaJet and CADJET plotters are highlighted at the site.

http://patent.womplex.ibm.com: Whether you're seriously searching for a patent or just noodling around the web, drop into IBM's Patent Server. Visitors can access over 26 years of U.S. Patent & Trademark Office patent descriptions. Additionally, Big Blue has scanned the last 10 years of images and made them available at the site. There's even a Gallery of Obscure Patents featuring items such as non-staling aerated bubble gum.

http://www.grit.com: It's not the same stuff we used to find on the back of old comic books. GRIT stands for Gould Resources & Internet Telecommunications. The site is a 24-hour broadcasting site for the worldwide cyber community. Audio shows at the site feature free-speech discussions, new software bugs, sports, and exercises for computer jockeys. GRIT broadcasts in RealAudio and StreamWorks formats. There also is a search engine, digital photograph gallery, and link to GRIT's CU-See Me reflector site.

HOT PC PRODUCTS

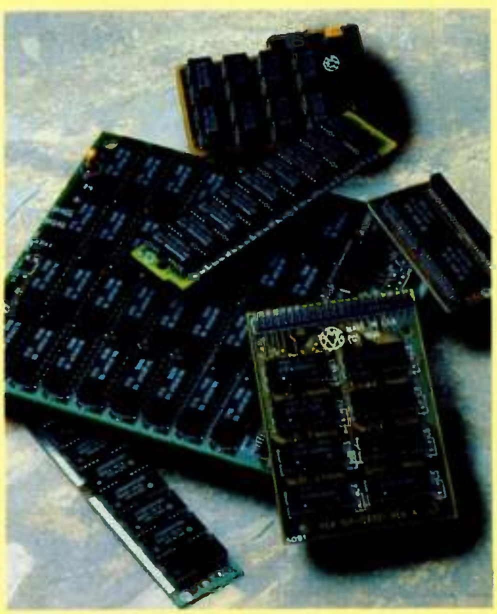
Cybex Computer Products now offers a new keyboard/video/mouse (KVM) switch. The Autoboot Commander II, capable of supporting eight computers, can be expanded to 64 servers. Users can page through a menuing system in the on-screen display to select computers. Supporting hot plugging, the switch enables users to connect and disconnect LAN servers without powering down or rebooting the servers that are already connected.

For more information, contact Cybex Computer Products Corp., 4912 Research Dr., Huntsville, AL 35805; (800) 793-3758; (205) 430-4030; Internet: http://www.cybex.com.

Just in time for the virus season, Allied Telesyn has begun packaging McAfee VirusScan for Windows 95 with its Ethernet network adapter card line. Included in this deal, McAfee will upgrade any VirusScan software that came with an Allied Telesyn adapter card. The upgrade is available at McAfee's Internet site: http://www.mcafee.com. Card models involved in this offer are the AT-2560TX 10/100 Mbps Fast Ethernet adapter card, the AT-2450 10 Mbps PCI adapter card, the AT-1700 Plus, and the AT-1500 plug-and-play 10 Mbps ISA adapter card.

For more information, contact Allied Telesyn International Corp., 950 Kifer Rd., Sunnyvale, CA 94086; (408) 730-8950; (408) 736-0100; Internet: http://www.alliedtelesyn.com.

Speaking of cards, MGV Memory has recently released a line of PC cards. The company has made available ATA Flash Cards in 4-Mbyte (Type I), 8-Mbyte (Type I), 12-Mbyte (Type I), 16-Mbyte (Type II), and 20-Mbyte (Type II) sizes. Offering other options, MGV also has a number of Linear Flash Cards in 5-V, as well as 12-V settings. The Linear cards come in 2-Mbyte, 4-Mbyte, 6-Mbyte, 8-Mbyte, 10-Mbyte, 12-Mbyte, 14-Mbyte, 16-Mbyte, 20-Mbyte, 24-Mbyte, and 28-Mbyte sizes. They are all categorized as Type I. Well-known for their ability to function as hard drives, without the space and power cost, flash cards are expected to be used in a variety of new applications throughout the next three years. In addition to all of the business professionals using the cards in their portable computers, there's a large group of digital camera owners using the versatile cards. The digital cameras use an electronic storage technology, rather than exposing light to treated films to produce, or rather, capture images. Chinon, Dycam, Kodak, Nikon, and Fujix cameras all support MGV Memory flash cards.



Contact MGV Memory, 29B Technology Dr., #100, Irvine, CA 92618; (714)453-1965; fax (714)453-1760; Internet: http://www.mgvgroup.com.

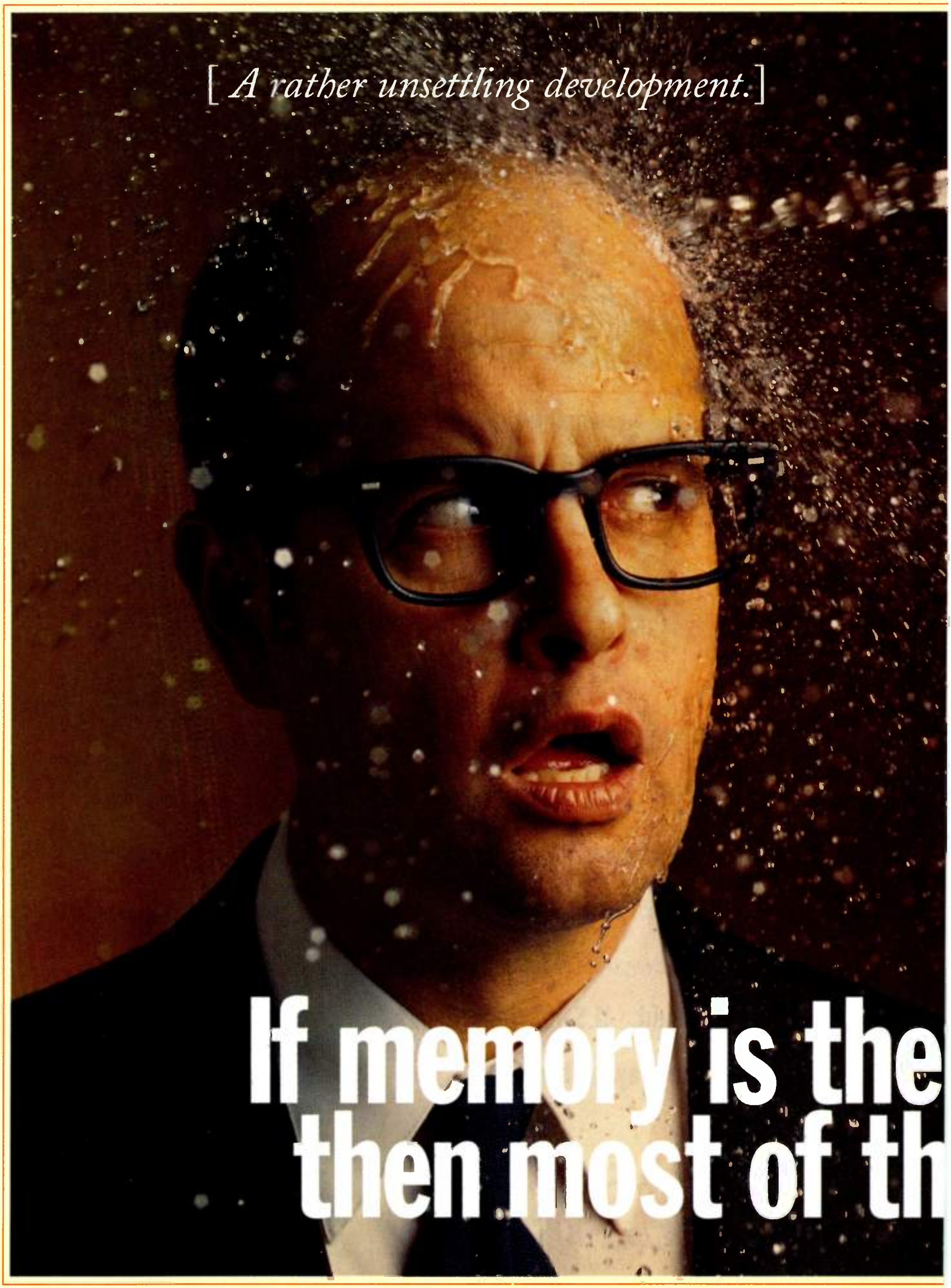
CONFERENCE CALL

The Communication Design Engineering Conference (CDEC) and the DSP Spring Design Conference (DSP) will be held Mar. 25-27 at the Washington Convention Center, Washington, D.C. Featured are two days of product exhibits on the latest technologies in communication and signal processing design. Over 60 training courses on communications equipment will be available at the chip, box, and board level, including Fibre Channel hub design. More than 50 training courses for signal processing will be featured, including designing with DSPs and partitioning and pipelining for multi-DSP platforms. For information on CDEC, telephone (617) 821-9219; e-mail: cdec@exporeg.com. For information on DSP, telephone (617) 821-9217; e-mail: dsp@exporeg.com.

The DCI Data Warehouse Conference will be held April 8-10 at the San Jose Convention Center, San Jose, Calif. Conference sessions will discuss topics such as data mining, database connectivity and replication, and file indexing optimizers. Also featured will be various product presentations and roundtable sessions. For more information, contact DCI, 204 Andover St., Andover, MA 01810; (508) 470-3880; fax (508) 470-0526; Internet: http://www.DCIexpo.com.

Contacting QuickLook

We'd love to start pinning your feedback up on our cubicle walls. So, if you have a topic you'd like to see covered in QuickLook, a viewpoint to express on something you may have seen in this section, or even some praise (maybe our publisher might give us a raise) about a piece we've printed here, please send it in. We welcome all correspondence. You can stuff our e-mailboxes—Mike Sciannamea at mikemea@class.org or Deb Schiff at debras@csnet.net. If you prefer our friends at the postal service, send your comments to The Copy Desk, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604. Our fax number is (201) 393-0204.


[A rather unsettling development.]
If memory is the
then most of th

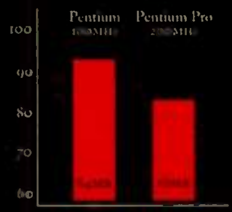
Allow us to stun you with some news. Memory is no longer overhead.

Instead, it's the single most cost-effective ingredient in PC performance.

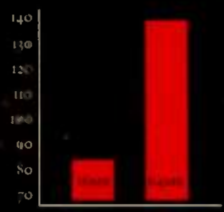
The reason: The price of memory is way down. And new studies provide insights that are, well, rather shocking.

For instance, a garden-variety 100 MHz Pentium-based system outperforms a state-of-the-art 200 MHz Pentium Pro-based system, when you add memory with a retail value of under $200.

Windows NT 4.0 Benchmark Performance



Amazingly enough, adding memory lets a 100 MHz Pentium-based system outperform a 200 MHz Pentium Pro-based system.



A 63% performance gain is what you get if you add 48 MB of memory to a 200 MHz Pentium Pro-based system.

The fact is, applications and graphics being what they are—not to mention the Internet—memory really is the food of computers. And most of them just plain aren't getting enough to eat.

For information on how to feed them, the leader in memory invites you to visit our home page today. http://www.more.memory.samsung.com. Or call 1-800-446-2760.

More Memory Changes Everything.

SAMSUNG

SEMICONDUCTOR

food of computers,
em are starving.

It's Ancient Greek (And Egyptian) To Me

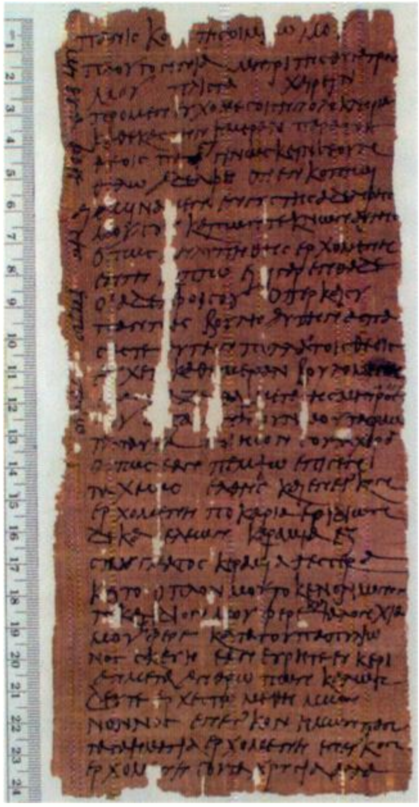
It's been said many times by many different people, but the saying still holds true—the more we learn from our past, the more we can predict our future. Meanwhile, in the present, six of America's finest learning institutions are bringing the past into the Internet age.

Columbia University, Duke University, Princeton University, the University of California at Berkeley, the University of Michigan, and Yale University are banding together to bring their collections of ancient manuscripts to the World Wide Web (WWW). The project is known as the Advanced Papyrological Information System (APIS). The first two-year development phase is being funded by a $300,000 grant from the National Endowment for the Humanities (NEH). The project leader, Roger Bagnall, chairman of the Department of Classics at Columbia, estimates the price tag for the entire system to be $3 million.

Columbia's participation in the project isn't the school's first venture into the digital domain. Two years ago, NEH granted Columbia's Media Center for Art History $575,000 to preserve humanities research and bring historical materials on line. Columbia has produced an on-line multimedia representation of Amiens Cathedral, begun a Digital Dante Project, and collaborated with Berkeley on a Digital Scriptorium. To support the digital libraries, Columbia has established a Center for Research in Information Access. The center provides information on research technology and intellectual property.

In restoring and studying papyri, historians have always had to struggle with the problems of locating missing pieces, managing the fragile materials, and keeping track of all of the papyri, which might be part of any number of collections around the globe.

The goal of APIS is to establish an electronic catalog of the schools' total 30,000-item strong collection of historical papyri. These papyrological archives represent about 10% of all the known materials of this nature worldwide. Most of the individual



collections at the universities were acquired through purchases of antiquities early in the century. The University of Michigan's collection was the result of excavations in Egypt in the 1920s and 1930s, in addition to purchases. The University of California at Berkeley's collection is made up entirely of items from excavations at the turn of the century. Yale's collection comes from a number of Syrian excavations from the 1920s and 1930s.

Papyrus, invented in Egypt around 3000 B.C. or earlier, was made from the fibers of reeds growing in Egypt's and Sudan's marshes. The word we use for describing the flat sheets put into our printers is derived from the Greek and Latin words for papyrus.

For the most part, these historical precursors to paper are documents used in daily life. Items such as legal files, literary works, and tax records make up the collections. Dating from the late fourth century B.C. to the middle of the eighth century A.D., some of the papyri have been in storage for over 30 years.

APIS, designed to be a comprehensive electronic information system, will include bibliographies, catalog records, images, and text linking all of the collections together. Hypertext markers will bring site visitors from one school's collection to another. Previously, examination of all these materials had to be done by traveling great distances and spending quite a bit of time visiting all the collections.

To present these materials to experts and nonspecialists alike, APIS uses high-quality digital images. For some materials that are extremely difficult to photograph or scan, multispectral imaging is used. This technique was developed at Caltech's Jet Propulsion Laboratory. Multispectral imaging uses infrared radiation to illuminate different layers of text.

According to Professor Bagnall, "The original tools were all from the 1970s, and nothing worked together. We wanted an integrated system so we could move around all the material, like a browser. We also needed common standards for how all these things were attached to each other."

Traianos Gagos, associate archivist in papyrology at the University of Michigan, used the Kontron camera, instead of a flatbed scanner to put the image shown on this page up on the school's site (http://www.lib.umich.edu/pap).

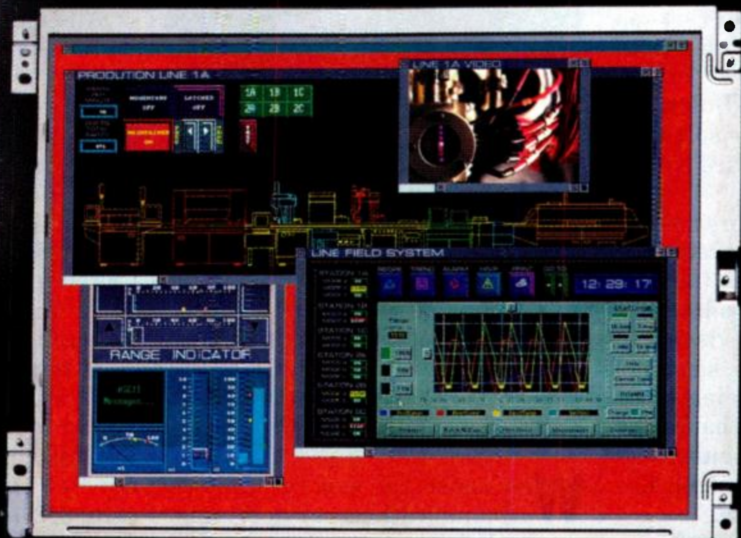
The image is a letter sent from a Greek gentleman to his wife. Here's an excerpt of the translation:

So when you have received this letter of mine, make your preparations in order that you may come at once if I send for you. And when you come, bring ten shearings of wool, six jars of olives, four jars of liquid honey, and my shield, the new one only, and my helmet. Bring also my lances. Bring also the fitting of the tent. If you find an opportunity, come here with good men. Let Nonnos come with you. Bring all our clothes when you come. When you come, bring your gold ornaments, but do not wear them on the boat.

For more information, contact the Office of Public Affairs, Columbia University, 304 Low Library, Mail Code 4321, 535 West 116th. St., New York, NY 10027; (212) 854-5573; e-mail: bagnall@columbia.edu.—*DS*

Wider viewing angles combined with higher brightness – up to 200 nits – make Sharp CSTNs easy to read, even in higher ambient light environments.

Talk about a sight for sore eyes! Superior color saturation is combined with the industry's highest contrast ratio CSTN LCDs.



Sharp's CSTN screen sizes include 10.4", 11.3", 12.1", 13.8", 15.0" and 17.7" – with even larger diagonal sizes coming soon!

Video response times and improved contrast ratios will soon allow for animation capabilities able to bring manufacturing process functions to life.

Sharp's CSTN displays are ideally suited to applications ranging from factory automation to medical diagnostics, point of sale and automatic banking to off-track gaming. You can bet on it!

Some view a CSTN LCD in terms of all the money it can save. We see a bigger picture.

Turning to large-screen CSTN* LCDs to meet your flat panel needs has always been a smart choice, budget-wise. But now it's an unbeatable solution, no matter how you look at it.

Because with Sharp's CSTN, there's no need to compromise your cost or performance expectations. Instead, you can get bright, bold, large-screen color performance that's increasingly indistinguishable from TFT – for about *half* the price you'd expect.

The fact is, in many applications Sharp's CSTN is definitely the wise choice. With screen sizes expanding ... color saturation rivaling that of TFTs ... vastly improved contrast, higher brightness and wider viewing angles ... it all adds up to the one display that combines compact size with great performance and yes, big savings in cold hard cash.

For the full story about Sharp's CSTN, call Sharp at 1-800-642-0261, Ext. 2024 or use our convenient FASTFAX number, 1-800-833-9437, and ask for Doc. #4000. Then, take a closer look at today's CSTN.

You're in for one big surprise.

CSTN Color Displays

Panel Size (Diagonal)	Part Number	Display Format	Brightness (cd/m²)
10.4"	LM64C350	640 x 480	70
11.3"	LM64C391	640 x 480	150
12.1"	LM80C31	800 x 600	200
13.8"	LM14S70	800 x 600	150
13.8"	LM14X79**	1024 x 768	200
15.0"	LM15X77**	1024 x 768	150
17.7"	LM18X74	1024 x 768	150

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* Color Super Twisted Nematic
** Integrated Inverter

INTERNET NEWS

Jumping into the set-top fray, Zenith Electronics has linked with Network Computer (an Oracle subsidiary) in releasing a family of Internet TV products.

Zenith's new line includes set-top boxes and integrated TV sets. Both will be based on Network Computer's N|C System Software (http://www.nc.com). The software will be included in the entire NetVision Internet TV line.

N|C's software lets users quickly connect to the Internet, run multimedia applications, and browse the web.

Essentially, NetVision allows TV viewers to use their televisions to surf the World Wide Web, send and receive e-mail, and use electronic commerce services. All of that can be accomplished through Zenith's Z-Trak track-ball remote control. The remote operates as a mouse.

Additionally, the company offers a wireless keyboard. Both the set-top boxes and Internet enhanced televisions will include a printer port and a smart card slot. The NetVision line features an internal 33.6 kbits/s phone modem and an Ethernet port for high-speed cable modems.

For more information contact Zenith Electronics Corporation, 1000 Milwaukee Ave., Glenview, IL 60025; (847) 391-8181; Internet: http://www.zenith.com.

WebAssist, the new interactive communications service, is the result of a joint venture between Sky Alland Marketing and US Interactive (http://www.usinteractive.com). The two-way service consists of a suite of Internet site enhancement tools to improve customer relations.

Allowing users to speak with an on-line service representative, talk through an Internet telephone, request product information, and schedule call backs, WebAssist is designed to provide a more responsive climate for customers.

The service also includes Web ScreenTalk (similar to chat), Web NetCall (Internet telephony for Netscape 3.0 or Microsoft Explorer 3.0), Web Callback (automated call back scheduler), and Web Lead Fulfillment (data capturing and forwarding).

For more information, contact Sky Alland Marketing, 6740 Alexander Bell Dr., Columbia, MD 21046; (410) 312-1515; (fax) (410) 312-4970; Internet: http://www.skyland.com.

Instant Access To Electronic Circuits

Adapted from the best-selling five-volume reference by Rudolf Graf and William Sheets, McGraw-Hill has just released the *"Encyclopedia Of Electronic Circuits On CD-ROM."* The disc includes 1000 circuit designs taken from companies such as Motorola, Texas Instruments, General Electric, RCA, and National Semiconductor. This new tool allows users to locate specific circuits, review them on a PC, and print them on a laser printer. The disc is described as a comprehensive resource for state-of-the art designs that can be used by engineers, electronic professionals, students, and hobbyists.

By using this compact disc, users can quickly find circuit designs by category or alphabetically. There are 142 circuit categories, which include audio circuits, display circuits, measurement circuits, power supplies, radio circuits, signal-generation circuits, as well as others. Once a topic is found, a text description of the circuit is provided, and the user can then view the complete circuit diagram using a built-in schematic viewer. Most of the schematics also feature mechanical details of parts,IC packages, and waveform diagrams. Users also have the option to print out the schematics.

A toll-free 800 phone number is available for users to access four locked CAD products that are available on the disc: SuperCAD, a full-featured schematic editor; SuperSIM, a digital simulator; SuperSPICE, an analog simulator; and SuperPCB, which creates printed-circuit boards. Free demo software is included for both SuperCAD and SuperPCB.

The CD-ROM, which also contains a user manual, is priced at $99 and is available now. Minimum system requirements are a 386 PC, 4 Mbytes of RAM, 10 Mbytes of hard-disk space, a VGA or better monitor, Windows 3.1 or higher, and a CD-ROM drive with Microsoft extensions.

To obtain a copy of the CD-ROM, or for more information, contact McGraw-Hill, 11 W. 19th St., New York, NY 10011; (212) 337-5951; fax (212) 337-4092.

BACK TO SCHOOL

Semiconductor Services' Semiconductor Processing Overview seminar will be presented four times during the course of the year—May 6, July 11, Sept. 16, and Dec. 2. The one-day course will take place at the Pacific Athletic Club, Redwood City, Calif. Topics covered during the seminar will include industry background, wafer manufacturing, IC fabrication, and test and assembly. For more information, contact Semiconductor Services, 735 Hillcrest Way, Redwood City, CA 94062; (415) 369-7890; fax (415) 367-1062.

"Creating and Compressing Digital Video" is a seminar that aims to provide a comprehensive understanding of high-quality and professional digital video. Topics to be covered include: The Science of Video Compression; Preprocessing Video; and Streaming Video on the Net. The 3-day seminar will be held in various locations around the U.S. Registration fee is $895. Contact Influent Technical Seminars, 498 Concord St., Framingham, MA 01702; (888) 333-9088; fax (508) 872-1153; Internet: http://www.influent.com.

Analog Book Reviews

New Op Amp Books For The Designer.

As far as standard ICs are concerned, op amps are probably the most universally used active part. Capable of far more than ever imagined back in the 60's when they first appeared, IC op amps are now used for a very wide array of tasks. Op amp books abound on my shelf, about 40 such titles in fact, and that's just for books dedicated *solely* to op amps. While the ones I use most often number ten or less, nevertheless good new analog books are always welcome. Which brings us to a case in point with this column's subject.

One of the more prolific writers of op amp books and applications that use them is Jerry Graeme. Graeme was an expert designer with Burr-Brown for many years, and is now a Principal Engineer with Gain Technology Corp. of Tucson, Ariz. Of course, he's no stranger to *Electronic Design* readers, having written numerous design articles in the past few years. Among the first op amp books I ever bought was *Operational Amplifiers: Design and Applications*, by Gene Tobey, Jerry Graeme, and Lawrence Huelsman, published by McGraw-Hill back in 1971. Since then, Graeme has published a number of other op amp books. The most recent include a book on photodiode applications using op amps, and a just-published one on optimizing op amp performance. This column focuses on these two books as analog design aids.

Photodiode Amplifiers: Op Amp Solutions, McGraw-Hill, 1996, ISBN 0-07-024247-X, is a 6-in. by 9-in. hardback book with a price of $49. Contact the publisher at (800) 2-MCGRAW or *http://www.mcgraw-hill.com*

Co-published with the author's company, Gain Technology Corp., the book features 272 pages and 105 illustrations within 10 chapters, plus a glossary and index.

This book should be a valuable aid to anyone using photodiode transducer circuitry for the wealth of information it contains. In the 10 chapters, Graeme starts from photodiode basics, and goes through amplifier-related considerations for noise, stability, bandwidth, gain, power supply effects, external noise effects, and such specialized applications as position-sensing photodiodes.

While the basic topology of a photodiode amplifier is one of an I/V converter with a photodiode as a current source transducer, extracting maximum performance from this setup is far from trivial. Various factors impact performance in terms of noise, bandwidth, and sensitivity, turning what appears from the surface as a somewhat straightforward circuit into a design challenge. Both the amplifier selection as well as the surrounding environment of the I/V stage often can have a major impact on performance— detrimentally!

WALT JUNG

Graeme explores thoroughly this amplifier topology from general standpoints, and shows various modifications to enhance certain performance aspects, such as high gain operation, revisiting topics he has covered in past *Electronic Design* pages. For example, by exploiting the "Tee" feedback network[1] to eliminate the usual $10^9\ \Omega$ feedback resistor needed for 1-V/nA sensitivity, high I/V stage gain now can be realized with more normal component values.

This step avoids susceptibility to contamination and leakage paths such as with the $10^9\ \Omega$ resistor. Among other such enhancements addressed are bootstrapping the photodiode for greater bandwidth, dark current compensation, and multiple amplifier configurations.

While the general treatment of this book toward the applications is excellent, it could use some detail in terms of typical op amp part numbers. It turns out that an optimum amplifier for wide dynamic range, high bandwidth photodiode I/V applications is a somewhat rare animal within the op amp universe. Generally speaking, it will be a low voltage noise, low input current, low input capacitance, wideband FET input op amp. This is not something you find just lying around in your junkbox, and you'll typically pay a premium for such performance.

All in all however, this is a book that can easily be recommended. It will serve the photodiode amplifier designer quite well, and also will serve as a single reference source for the occasional user of these configurations.

Optimizing Op Amp Performance McGraw-Hill, 1997, ISBN 0-07-024522-3, is a 6-in. by 9-in. hardback, priced at $55. Also co-published with Gain Technology Corporation, this brand new book includes 300 pages and 150 illustrations within six chapters, plus a glossary and index.

While photodiode applications tend to be a bit specialized, general op amp feedback considerations certainly aren't—in fact, they are universal to all feedback circuits. And that is one of the major strengths of this book, the new insights it opens into more sophisticated feedback setups and their analysis. The first two chapters deal with feedback and its analysis, with titles of: "Performance Analysis, Feedback, and Stability," and "Feedback Modeling and Analysis." The first of these is more of a refresher, but nevertheless, it makes some excellent points. These include such things as general stability requirements related to the Bode diagram open/closed loop rate-of-closure, and the surrounding circuit and op amp parasitic effects on stability.

The second chapter is one of the book's major highlights, as it develops new feedback analysis approaches to extend the classic non-inverting feedback model to more general uses including inverting and differential cases. For example, it is a very interesting treatment to see how Graeme develops $\beta+$ and $\beta-$ models into a net β, for use in the feedback calculations. The chapter includes examples of composite amplifiers and other complex feedback structures to illustrate the analysis points. To me, this chapter alone is worth the admission price. Readers should find it helpful when seeking maximum performance from op amps that use the classic voltage feedback architecture.

Chapter 3, "Power-Supply Bypass," details design methods for optimizing the power supply system of an op amp to minimize spurious resonances and noise components. This chapter draws upon the themes of a couple of recent Graeme-Baker articles from *Electronic Design*,[2,3] illustrating graphically how noise components in the supply system interact with the amplifier's response, how resonances can occur in bypasses, steps to take for damping, etc. While this coverage is generally excellent, it would be even better with the use of actual part number examples, for instance as were used in previous articles.[2,3]

Chapter 4, "Phase Compensation," shows how to counteract destabilizing loads as well as other parasitic effects around amplifier configurations. Chapter 5, "Reducing Radiated Interference," shows methods of reducing electrostatic coupling by means of impedance control and balance, and controlling magnetic interference by shielding, minimizing loop area, along with effective common mode rejection.

Chapter 6, "Distortion and Its Measurement," is one of the more interesting, yet puzzling, chapters of the book. Quantifying op-amp distortion is one of the more important measurement tasks facing a designer today, and toward this goal, sound measurement and analysis techniques are really invaluable. In this chapter, a number of useful op amp measurement hookups are suggested toward separating and scaling op amp input and output signals, thus leading to isolation of the op amp's distortion component(s), while minimizing sensitivity to the analyzer's limits.

Unfortunately, one of this section's weak points is that there are no complete in-context measurement examples to flesh out the concepts. So, one simply cannot judge whether a given approach will allow measurements of –80 dB or –100 dB. Or, better yet, how op amp topologies differ in their distortion.

Pre-process filter instrumentation such as described in another article[4] can enhance FFT dynamic range to well above 100 dB, allowing harmonics to be captured at –130 to –140 dB levels. Standard bench instrumentation such as the Audio Precision System 1 analyzer[5], allows both digital and analog domain signal tests. This instrument has a 20Hz-20kHz THD+N system spec limit of 0.0015% + $3\mu V$ for a 22Hz-80kHz measurement bandwidth (note: 0.0015% is equivalent to –96.5 dB). This can be extended with pre-processing, as noted above. Combining the power of this instrumentation and the Chapter 6 techniques can result in some powerful distortion analysis tools.

Despite some relatively minor caveats, I would recommend this book to anyone using op amps. The book's strengths are certainly the treatment of advanced feedback analysis, but there are plenty of other useful concepts for the designer within the covers.

TIP: Your analog design tool kit can be usefully enhanced by both of these books. Enjoy!

References:

1. Jerald Graeme, "The Tee-Feedback Factor in Photodiode Amplifiers," *Electronic Design Analog Special Issue*, June 26, 1995.
2. Jerald Graeme, Bonnie Baker, "Design Equations Help Optimize Supply Bypassing for Op Amps," *Electronic Design Analog Special Issue, June 24, 1996.*
3. Jerald Graeme, Bonnie Baker, "Fast Op Amps Demand More Than a Single-Capacitor Bypass," *Electronic Design Analog Special Issue, Nov. 18, 1996.*
4. Tom Mintner, "Pre-Process Audio With Notch Filter to Improve FFT Dynamic Range," *Electronic Design Analog Special Issue, Nov. 18, 1996.*
5. Audio Precision System One, Audio Precision, P.O. Box 2209, Beaverton, OR, 97075-3070; (800) 231-7350.
6. Distortion measurement techniques and results are discussed in Chapter 2 of Walter G. Jung, *Audio IC Op Amp Applications, 3d Ed.* Sams, 1987.

Walt Jung is a Corporate Staff Applications Engineer for Analog Devices, Norwood, Mass. A longtime contributor to Electronic Design, he can be reached via e-mail at Walter.Jung@Analog.Com.

First Low-Profile CD Laser Tweaks OC-12 Standards

This 1-by-9 optoelectronic transceiver in the MDX-19 Series, with the lowest profile of any product for mezzanine-card applications, fully complies to

ATM OC-12 standards. Suitable for bidirectional communication over multimode fiber, it operates at a data rate of 622 MBaud. The device can plug into any standard mezzanine card with its wave soldering attaching post, and link to a cable through its standard SC fiber connector. This Class 1 laser meets CDRH and IEC safety standards. It's also UL1950 approved. MDX-19 Series optical transceivers also contain modules compatible with OC-3, FDDI, and the Fibre Channel X3T11 physical standard PH-2 networking environments. LG

***Methode Electronics**, 7444 W. Wilson Ave., Chicago, IL 60656; (708) 867-9600; fax (708) 867-9130.* **CIRCLE 690**

QCELP Vocoder Developed For ANSI C Processor

DSP Software's Qualcomm Code Excited Linear Prediction (QCELP) Vocoder is a real time, bit-compliant implementation of the TIA IS-96A QCELP vocoder for the fixed point ANSI C digital signal processor. It provides coding for the multirate 8-kbit/s and 13-kbit/s coders supporting 1/2, 1/4, and 1/8 fractional coding (8, 4, 2, 1 kbits/s and 13, 6.5, 3.25, and 1.625 kbits/s). This re-entrant implementation can provide two full-duplex channels of encode/decode per DSP. LG

***DSP Software Engineering Inc.**, 175 Middlesex Turnpike, Bedford, MA 01730. (617) 275 3733; fax (617) 275-4323.* **CIRCLE 691**

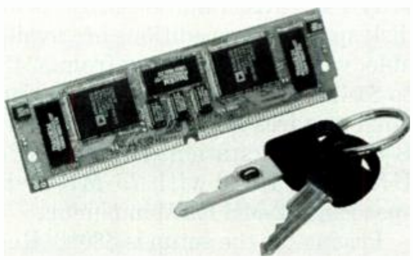
Integrated QAM Chip Runs At 40 Mbits/s

Lucent's AV6410 quadrature-amplitude-modulation (QAM) chip, a demodulator for cable TV modems, supports data-transmission rates to 40 Mbits/s, a thousand times faster than a conventional analog desktop modem. The most recent addition to the company's Cable Modem Silicon Suite, it combines an analog-to-digital converter, 256-QAM modulator, IF passband-to-baseband converter, and forward-error correction together for the first time. This chip also supports demodulation in 4, 8, 16, 32, 64, and 128 modes. Cost is less than $25 in quantities of 100,000 or more. LG

***Lucent Technologies**, 555 Union Blvd., Allentown, PA 18103; (800) 372-2447, Dept. R20. Canada: telephone (800) 553-2448, Dept. R20.* **CIRCLE 692**

V6 Data Engine Can Handle Six Modems

This RISC-based, single-board data pump houses six Analog Devices digital signal processors on a standard 72-pin SIMM measuring only 1.1 by 4.25 in. It interfaces directly with a T1 or



E1 line , providing designers of remote-access products with the ability to handle six V.34 modem calls or 24 ISDN calls per unit. The Patton V6 boasts 198 MIPS of sustained RISC processing and 864 kbytes of on-board memory. Four such V6 Data Engines handles an entire T1. The Data Engine interfaces with the T1/E1 carrier at the board level using only four TTL signals. Each DSP in the V6 is programmed to recognize which of the 24 TI channels (or 30 E1 channels) it is responsible for accessing. Power consumption is 4.2 W at 5 V dc. A low power version using only 2.5 W at 3.3 V dc also is available. The Patton V6 comes standard with V.34 modem software. The engine is priced at $540 each in quantities of 2500 pieces. LG

***Patton Electronics Co.**, 7622 Rickenbacker Dr., Gaithersburg, MD 20879. (301) 975-1000; fax (301) 869-9293.* **CIRCLE 693**

Frequency-Shift-Keying Receiver Tunes ISM Band

RF Micro Devices' RF9902 is a monolithic IC with CMOS-compatible outputs for use as a low-cost frequency-shift-keying (FSK) receiver at 400 to 930 MHz. It's designed to work independently or as part of an FSK transceiver when used with the company's FSK RF9901 transmitter. The RF9902 features an input amplifier, mixer, IF limiting amplifier, phase detector, and an output Schmitt trigger to generate the digital signal. The chip has two sections: one for performing down conversion, the second for demodulation. Typical applications include handheld POS terminals, meter reading, bar-code reading, and various digital systems applications. The RF9902 is offered in a standard 16-lead plastic SOIC package. LG

***RF Micro Devices**, 7625 Thorndike Rd., Greensboro, NC 27409; Internet: http://www.rfmd.com.* **CIRCLE 694**

Broadband VSAT Receiver Has Tunable Data Rate

The STEL-9258 board-level demodulator for very small aperture terminals (VSATs) offers user-selectable data rates to allow the system to operate at the lowest possible bandwidth. It's programmable from 19.2 to 1024 kbits/s BPSK, or 64 to 2048 kbits/s QPSK. In includes an integral L-band down-converter that can be tuned from 950 to 1450 MHz in 1-Hz steps. The assembly also can be supplied without the down-converter to accept a direct 70-MHz IF input. It can track input frequency drift of up to ±2 MHz without loss of signal lock. This permits the use of inexpensive "dielectric resonator oscillator" type LNBs, rather than much more expensive phase-locked LNBs. Price is $425 each in quantities of 1000. LG

***Stanford Telecom**, Telecom Component Products Group, P.O. Box 3733, Sunnyvale, CA 94086. (408) 250-2660.* **CIRCLE 695**

DataViews 9.7 Brings DDVT To Windows NT

Version 9.7 of the DataViews development tools for building graphics to monitor and control real-time processes is now available on the Windows NT platform. The dynamic data visualization development tool (DDVT) manages raw data and transforms it into intuitive graphical representations. Users can build fully animated interfaces for visualizing, analyzing, and regulating real-time industrial, telecommunication, and scientific processes.

DataViews 9.7 supports Microsoft Visual Basic, Visual C++, and Visual Basic-compatible OCXs, allowing programmers to create custom OCXs for data acquisition and other functions. Applications built with DataViews can be compiled with Visual C++. Over 10,000 dynamic graphical objects representing data points can be analyzed per second.

An open API environment provides developers with five different methods of integrating data, and the ability to interface to any third-party or proprietary data-acquisition device or data-distribution system. The DV-Draw drawing editor allows the addition or removal of dynamic properties through intuitive pop-up dialog boxes. DV-Draw also supports dynamic True Type text. DataViews also includes a true Multiple Document Interface for keeping multiple views of documents open simultaneously. Additional font support lets users work with any font available in their system, including scalable fonts and hardware and vector text.

Application examples include graphical analysis of data in R&D environments, satellite transmission and monitoring, supervisory control and data-acquisition applications for process control, and graphical information systems for air-traffic control and public transportation.

Pricing for DataViews 9.7 for Windows NT starts at $5000. Cross-platform versions are available for HP, Sun, SGI, IBM, and Digital platforms.

***DataViews Corp.**, 47 Pleasant St., Northampton, MA 01060; (413) 586-4144; e-mail: info@dvcorp.com.*
CIRCLE 696

Ada Rides Into Commercial Arena On Windows and Unix

Originally developed for mission-critical applications such as flight management and weapons control systems, the Ada programming language now qualifies as a development tool for a wider range of applications. These include the aerospace, energy, transportation, automotive, medical device, telecommunications, finance, and process-control industries.

Based on the object-oriented Ada 95 language, ObjectAda is the first object-oriented Ada environment for Microsoft Windows 95 and NT, and for Unix platforms from Hewlett-Packard and Sun Microsystems. Key features of ObjectAda for Windows include a full Ada 95 core language and key annexes, a familiar development paradigm and facilities for linking Ada code with C++ applications and vice versa, a Windows GUI builder, and Win32 bindings. Other attributes include Winsock TCP/IP bindings, an open library model, source browser, WinDbg/Codeview multilingual debug, and DLL import and export.

System requirements include an 80386-based or higher PC running Windows 95 or NT, with at least 12-Mbytes of RAM and 80-Mbytes of disk space. Three editions are available, with prices ranging from $245 to $1495 per copy. ObjectData for Unix requires HP 9000 series or HP B-Class workstations running HP-UX 10.01, 10.10 with 75-MB disk space and 32-MB RAM minimum.

Pricing for the setup is $8000. Requirements for Sun/Solaris are a Sun SPARCserver, SPARCclassic, SPARCstation and UltraSPARC computer families running Solaris 2.5 with 75-Mbyte disk space and 32-Mbyte RAM minimum. ML

***Thomson Software Products**, 101 Merritt 7, Norwalk, CT 06856; (203) 845-5000.*
Web: http://www.thomsoft.com.
CIRCLE 697

Free Video Demonstrates Machine Vision Development

VisionBlox is a set of Microsoft Visual Basic software tools that can be assembled in various ways to customize any machine-vision application. Standard features include popular image-processing and analysis routines. The 14-minute video shows how to program custom machine-vision applications using VisionBlox, including capturing a live image, using the search (feature find) tool, interfacing and controlling a multi-axis motion device, and interchanging frame grabbers from multiple vendors.

The video begins by illustrating the ease of capturing a live image from a CCD camera. The camera, frame grabber, and display icons are dropped into the Visual Basic Design form. To view an image, the camera is linked to the display window with just two lines of code. The entire procedure takes less than 5 minutes, compared to traditional programming methods that take two to three days.

Image analysis uses the search (feature find) function algorithm to drop the feature-find icon onto the design form and link it to the image display window using two or more lines of code. On-line help allows users to page to the example code, and cut-and-paste the code onto the design form. The tool subsequently finds the center of the trained model.

An alignment application is demonstrated with two image controls displaying alternating live images using a VisionBlox calibration control. The vision system uses the location of circuit board fiducials to determine the amount of motion necessary to bring the board into alignment by controlling an X,Y, theta stage.

VisionBlox capitalizes on the performance of a Pentium-class PC for image processing, instead of ISA Bus-based DSP boards. With a PCI frame grabber, similar speeds are attainable at a fraction of the cost. The simplicity of interchanging frame grabbers is displayed by sweeping out one piece of hardware for another, then modifying the frame-grabber reference in the original line of Visual Basic code.

The VideoBlox video is free and available by request, along with product brochures, help file disks, and information on training classes in the U.S, England, and Japan. ML

***Integral Vision**, P.O. Box 6295, Toledo, OH 43514-6295; (419) 536-1983.* **CIRCLE 698**

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READER SERVICE 179

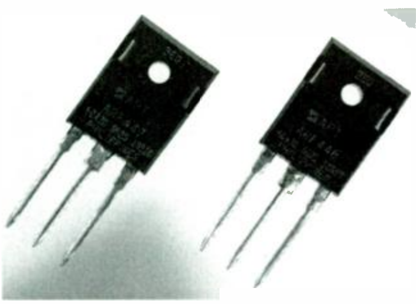
Red, Blue, Red/Green LEDs Brighten Panel Lighting

Polyus' LEDs come in red, blue, and red/green bicolor versions for panel lighting applications. Also available are 10- to 50-mW infrared types in the 730- to 930-nm region, which come in various T-1 and SM packages. These higher power units use an MDH heterostructure. Prices for the red and red/green types are $0.25 each in 10K quantities; blue, $2.50 (10K quantities), and the IR type is $0.50 each for 10K orders. PM

Polyus USA Inc., 8900 Fondren Rd., #296, Houston, TX 77074; (713) 961-1777; fax (713) 981-8449.
CIRCLE 699

Low-Cost HF MOSFETs Operate At 300 V

Combining low cost and plastic packaging, APT's ARF446 and ARF447 MOSFETs are optimized for 300-V opera-

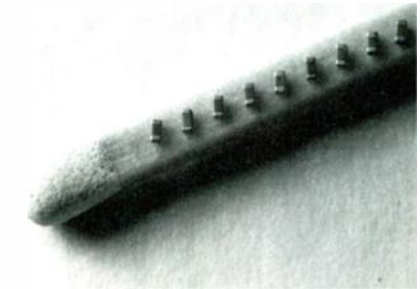


tion. They can provide up to 250 W at 14-dB gain and almost 70% efficiency at 27.12 MHz for industrial, scientific, and medical RF applications. Their high-voltage characteristic eliminates the need for a dc-dc converter, allowing the MOSFET to be driven directly by the output of the supply's power-correction-factor section. The ARF446 and 447 are priced at $51.35 each in 100-piece quantities. PM

Advanced Power Technology, 405 S. W. Columbia St., Bend, OR 97702. (800) 522-0809; fax (541) 388-0364.
CIRCLE 700

Ceramic Caps Can Handle Higher-Density Tasks

These ceramic multilayer capacitors, which come in a 0402 package, are ideal for use in cellular telephones, pagers, laptop computers, and porta-



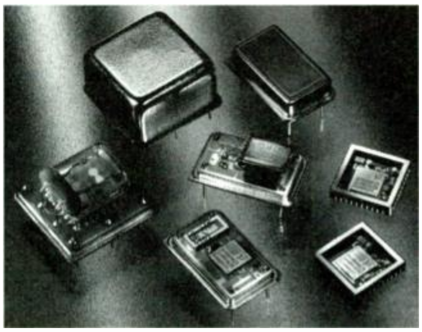
ble audio equipment—wherever high package density is required. These caps provide a reduction factor of between 1.5 to 2, compared with 0603 components. Standard thickness of the new models is 0.5 mm. Thinner versions (for mounting on tracks beneath ICs) are available on special order. Rated voltages are 16, 25, and 50. Class 1 caps (with NPO dielectric) offer 1, 2, 5, and 10 percent tolerance over the range of 0.47 pF to 100 pF.

Class 2 caps (with X7R dielectric) come in tolerances of 5, 10, and 20 % over 100 pF to 10,000 pF. They're designed for either reflow or wave soldering, and are supplied on tape/reel or in a new bulk case for automatic placement. Lead time is stock to 8 weeks. PM

Philips Components, 1440 W. Indiantown Rd., PO Box 689605, Jupiter, FL 33468. (407) 745-3300; fax (407) 745-3600. **CIRCLE 701**

ASIC TCXOs Meet Military Standards

The second generation of ASIC temperature-compensated crystal oscillators from C-Mac meet stringent telecommunications and military applications. Three standard packages



comprise the series: CMT4000, 5000, and 6000, all offering a range of standard frequencies. They provide a frequency stability of at least ±0.5 ppm over the temperature range of -40°C to +85°C. Phase noise is 100 dBc/Hz at 10-Hz offset, and the phase noise floor is 150 dBc/Hz. They've been specifically designed to support a 3-V power rail. The CMT4000 comes in a surface-mount package that's targeted for mobile communications systems, and operates over a frequency range of 1 kHz to 35 MHz. The CMT5000 comes in a 14-pin dual in-line package. It operates over a 1-kHz to 52-MHz range. The flat pack CMT6000, working over 1 kHz to 160 MHz, offers higher stability (±0.2 ppm over -20 to +70°C), and improved aging (±0.5 ppm in one year, ±2 ppm over 10 years) and phase noise characteristics. In addition, it has a tri-state output option. PM

C-MAC, 4709 Creekstone Dr., Suite 311, Morrisville, NC 27560; (919) 941-0430; fax (919) 941-0530.
CIRCLE 702

LED Family Glows In An Array Of Colors

A new line of LED lamps, which come in red, green, high-efficiency red and green, yellow,orange, and emerald green, are ideal for backlighting panels, illuminating switches, and for indoor and outdoor signs. Features include high on-axis intensity, consistent radiation pattern, and exceptional uniformity from lamp to lamp. These features allow designers to backlight a large panel containing a number of legends and indicators uniformly both in terms of color and brightness. The lamps provide uniform appearance from pixel to pixel, making images appear "smooth" for moving message signs.

Typical luminous intensity ranges from 27 millicandelas (at 20 ma) for emerald green (560 nm), to 2000 millicandelas for AlGaAs red (644 nm). Viewing angle is typically 15 to 25°. The lamps are supplied in a non-diffused, 5-mm package. It incorporates a 20-mil leadframe and tight meniscus controls, making it compatible with radial-lead, automated-insertion equipment. Yellow, orange, and green LEDs are lightly tinted so that they may be easily identified even when turned off. PM

Hewlett-Packard Co., Components Response Center, 3175 Bowers Ave., M/S 88U, Santa Clara, CA 95054. Melinda Herson (408) 435-4009.
CIRCLE 703

Display/Deflection Processors Target 50/60-Hz TV Sets

The DDP 3310A, a single-chip digital display and deflection processor realized in 0.8-µm CMOS technology, is intended for high-quality back-end applications in 50/60-Hz TV sets with 4:3 or 16:9 picture cathode-ray tubes. It can be combined with members of the Digit 3000 IC family or with third-party products. While the DDP 3310A is intended for 50/60-Hz applications, its sister product, the DDP 3310B, is optimized for 100-Hz/32-kHz applications.

One IC contains the entire fully digital video component and deflection processing and forms the heart of a modem color TV. The ICs both operate with a single 5-V power supply and offer a black level expander as well as dynamic peaking and a soft limiter for gamma correction. They both have a programmable RGB matrix, a scan velocity modulation output, a picture frame generator, and an additional analog RGB/fast-blank input. Also included is a separate ADC for tube measurements. *AV*

ITT Semiconductors Group, *World Headquarters, Intermetall, Hans-Bunte-Strasse 19, 79108 Freiburg, Germany; phone: +49-761/517-0; fax: +49-761/517-2174.* **CIRCLE 485**

Enhanced, Faster Model Created For Optical Module Testing

A newer version model of the LaserVision System for optically testing electronic modules, dubbed LV2, was developed by Rohde & Schwarz. The new system features additional test capabilities and a higher test speed. It's particularly suitable for testing SMDs, in which in-circuit testing is very limited because of the difficult adaption involved. The main fields of application include testing of mobile communication terminals as well as consumer and car electronics. LV2 offers an unusual combination of image processing and laser height measurement, providing a higher level of fault detection. The test rate is specified with more than ten components per second, enabling for use in assembly lines. *AV*

Rohde&Schwarz GmbH & Co KG, *Muehldorfstr. 15, Germany; phone: +49-89/4129-2232; fax: +48-89/4129-3208.* **CIRCLE 486**

Surface-Mount Varistors Protect Semiconductors From Overvoltage

To prevent damage of semiconductors caused by overvoltages, metal-oxide varistors are used to limit any overvoltage and reliably safeguard the semiconductors. The so-called SIOV multilayer varistors of the CN type series is available in sizes from 0603 through 2220. Their design is optimized for very low inductance, resulting in a response time of less than 0.5 ns. As a result, they're particularly suited for ESD protection, as well as in assuring CE conformity in cordless and cellular phones, interfaces like RS-232-C and Centronics, PCs (keyboard, mouse, printer interface, etc.), LANs, modems, sensors, and interface circuits. *AV*

Siemens Matsushita Components (S+M), *c/o Siemens Infoservice, P. O. Box 2348; 90713 Fuerth; Germany; fax +49-911/978-3321.* **CIRCLE 487**

Company Designs Surface-Mount LED Lamps For Mini Apps...

Intended for ultra-miniature applications is a new line of surface-mount-chip type of LED lamps created by Quality Technologies. Developed for standard footprints, their low profile, 140° viewing angle, and moisture-proof packaging suit them for panel illumination, push-button backlighting, and membrane switch applications. The new chip-type LEDs are available in red, AlGaAs red, green, and yellow, with either clear or diffused optics. Ideal for reflow-soldering or dip-soldering assembly lines, they're supplied on 8- mm tape and reel (2000 per reel). Another low profile surface-mount LED lamp arriving on the scene is the QTLP670C series. They conform to the EIA-535 BAAC standard specification for case 3528 tantalum capacitors. The lamps have non-diffused optics, suiting them for backlighting applications and coupling to a light pipe. They come in AlGaAs red, high-efficiency red, green, and yellow. *AV*

...And A 4-Pin Optocoupler That Cuts Device Size Nearly In Half

Another new product from the same manufacturer is a 4-pin dual in-line phototransistor optocoupler. It's claimed to require only about one half the size of a conventional 6-pin device without sacrificing any electrical performance. The optocoupler, dubbed H11A814, contains two gallium-arsenide, infrared-emitting diodes connected in inverse parallel that drive a single silicon phototransistor. Intended for applications such as ac-line monitoring, unknown polarity dc sensing, and telephone-line interfacing, the devices come in two current-transfer ratio ranges: 20% minimum to 300% maximum; and 50% minimum to 150% maximum. Also available is the H11A817 optocoupler, which consists of a single GaAs IR diode driving a single silicon phototransistor, again in the same 4-pin DIL package. It comes in five CTR ranges optimized for power line regulators, microprocessor and digital logic inputs, and in industrial controls. *AV*

Quality Technologies Ltd., *10, Prebendal Court, Oxford Rd., Aylesbury, Buckinghamshire HP19 3EY; Great Britain; phone +44-1296/39 44 99; fax +44-1296/39 24 32.* **CIRCLE 488**

Communications Connector Catalog Comes Calling

Cee whiz! Coaxial combination connectors with coaxial conductors, cable connectors, car-navigation connectors, coaxial multiple-contact connectors... they're all part of Hirose's *Connectors for Mobile Communications* catalog. Other products described run the gamut from battery terminals, spring terminal connectors, and base-station components for distribution, to a variety of internal wiring subminiature board-to-board connectors with 0.5-mm and 0.65-mm spacing. Connectors for car navigation include mini-twin crimp shielded types for antenna section connections and pin connectors for use with PC cards. To get the catalog from the Sherman Oaks-based company, call (805) 522-7958; fax (805) 522-3217 (for an instant catalog via fax, dial 1-800-879-8071, then ask for #0004). RE

CIRCLE 860

Designer's Guide On Fiber-Optic Transceivers

Amp Inc., Harrisburg, Pa., through its Optical Interconnection System division, has published a 76-page fiber-optic-transceiver designer's guide. The guide helps with the intracacies of incorporating transceivers in high-speed data-communication networks. Topics covered include transceiver components and functions, specifications and standards, safety, board layout, applications, and qualification and environmental testing. Though the book is geared toward AMP's products and technology, the principles involved are universal and can be applied to various standard applications like Fast Ethernet and Fibre Channel. Call (717) 986-5160 for further information. RE

CIRCLE 861

Catalog Revolves Around Global Solenoid Valves

Spanning 64 pages, Honeywell's new catalog concerning its global Valve Actuation Series of solenoid valves is aimed at specifiers and users of these devices in pneumatic actuator automation. Products covered include three- or four-way solenoid valves offered in various configurations, such as NAMUR interface, pipe mounted, sub-base mounted, intrinsically safe, etc. Specifications detail pipe size, flow factor, operating pressure differential, power consumption, voltages, and electrical connections. For more information and/or a copy of the catalog, call Honeywell's Skinner Valve division at (860) 827-2467; fax (860) 827-2384. RE

CIRCLE 862

LCD Product Guide Lights The Way For Designers

The Liquid Crystal Displays Product Guide is set up to help designers specify LCDs and display modules. Dot-matrix alphanumeric modules, complete display graphic modules, and segmented displays for use in a wide variety of applications are described. Descriptions are enhanced with detailed specifications and selection charts, as well as dimensional layouts for typical display modules. Technologies employed by Crystaloid, Hudson, Ohio, to create complete display solutions include twisted nematic, supertwist nematic, reverse constrast twisted nematic, touch screen, dichroic, dual-layer dichroic, and Heilmeier. For more information, call (216) 655-2429; fax (216) 655-2176. Or you can e-mail: crystaloid@aol.com. RE

CIRCLE 863

Audio/Multimedia Data Book Contains Layout Advice

The new *Audio & Multimedia Data Book* from AKM Semiconductors Inc., San Jose, Calif., is now available. At 451 pages, the book contains data sheets on AKM's ADCs, DACs, codecs, and its audio digital signal processor, together with the design of evaluation boards for most of the 19 products listed. There's also some extremely useful layout advice on product usage. Available free of charge, the book can be obtained by calling (408) 436-8580; fax (408) 436-7591; e-mail: ICinfo@AKM.com. PMcG

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Booklet Reviews Magnetic Theory And Core Applications

Selecting the proper core material for your specific core application is the basis of a new 20-page booklet made available from The Arnold Engineering Co., Marengo, Ill. Magnetic theory and core applications from dc to 100 kHz are discussed. Materials such as silicon steel, powdered iron, Sendust, Molypermalloy, Hi-Flux, Super-MSS, and ferrites all receive attention. Contact Arnold at (800) 545-4578; fax (815) 568-2228. RE

CIRCLE 865

Network, Computer-Telephony Product Guide Now Available

A new 64-page catalog from Industrial Computer Source, San Diego, Calif., features over 1000 model numbers of telecommunications product solutions. Included in the *Communication Source-Book 1997 Edition 1* are: a complete line of SBC/motherboard CPUs up to 300-MHz Alpha, 200-MHz Pentium; a complete line of plug-and-play wireless Ethernet products; 100Base-T network interface cards, switches, and hubs; and remote access routers. The reference sections contains tutorials on computer telephony, Fast Ethernet, and Ethernet. For further information, call (800) 523-2320; Web: http://www.industry.net/indcompsrc. RE

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OEM Instrument Components, Systems Outlined In Brochure

OEM instrument components and systems used by product designers and engineers are described in a brochure from the Nikon Instrument Group, Melville, N.Y. Among the products discussed are optics, focusing mounts, illumination systems, stereo microscopes, mechanical components, power supplies, and a host of others. Precision manufacturing, quality control, scientific research and diagnostic applications, are just some of the arenas that employ these components. To get a copy of the brochure, call (800) 52-NIKON, ext. P679; Web: http://www.nikonusa.com. RE

CIRCLE 867

If You Have A Brainstorm, Get A Patent Attorney

Eric L. Hausler

A light bulb just went off in your head—sorry, someone already got the patent on that one. Let's say that you have an idea for a new product. Once you get past the initial notion that you're fooling yourself, you start to seriously consider patenting and marketing your invention. Anyone who has sought a patent will tell you it's not an easy or cheap process. Deepak Malhotra, a patent attorney (Wells, St. John, Roberts, Gregory & Matkin, 601 W. First Ave. #1300, Spokane, WA 99204; (509) 624-4276; Internet: www.wsrgm.com), tells his clients, "Don't seek patents for the wrong reasons. If you think getting a patent will make you rich, you are probably mistaken. Many companies are not interested in buying technology unless the manufacturing engineering aspects are well developed, and a product is being made and sold."

What exactly is a patent and who issues them? The United States Patent and Trademark Office (PTO), located at Crystal Plaza 3, 2021 Jefferson Davis Highway, Arlington Va., defines a patent as "the right to exclude others from making, using, or selling" your invention for a period of 17 years. The right to exclude is key here. It doesn't give you the right to make, use, or sell your invention, only the right to keep others from doing it.

The PTO says that in order for an invention to be patentable, it must be new. Your invention is not new "if it has been described in a printed publication anywhere in the world, or it has been in public use or on sale in this country" before the date you apply for the patent. A patentable invention must be "sufficiently different from what has been used or described before." If you describe or use the invention publicly, or set it up for sale, you must apply for a patent before one year passes. Otherwise, you will lose the right to a patent. Be aware that filing deadlines in some foreign countries are much more strict than in the U.S..

The PTO reviews all patent applications. They also publish and issue patents, and maintain a search room for people to find currently-held patents. Examiners, who make up about one-half of the office's 4400 employees, have jurisdiction over assigned fields of technology. The examiners also initiate interferences, when two inventors claim the same invention. The PTO currently receives about 170,000 patent applications per year.

Patent Tips

Don Moyer, a patent agent (431 S. Dearborn 705, Chicago, Ill. 60605; (312) 939-3329; Internet: www.donmoyer.com) who runs patent-related workshops at Chicago's Harold Washington Library, cites three keys to a successful patent:

1. Patent something you can sell.
2. Get broad claims so that another product cannot get close to the functions and benefits of yours.
3. Do not give anyone an easy challenge both to your patent or to your business.

Moyer suggests that candidates formulate a plan for the invention that brings it from conception to payoff. Patenting an invention is not a cheap endeavor. The basic filing fee for the application is $770, not including the myriad of other related fees. Take a good financial inventory before starting the process to understand the costs involved.

Moyer also suggests making models of the invention. A good model "is the main distinction between dreaming and getting serious," he explains.

Is a patent attorney or patent agent necessary? "One key resource," says Moyer, "is a patent agent or patent attorney who will do the work to understand the invention, so that the inventor will get the broadest claims possible." Of course you can prepare and file your own applications, but Moyer points out that "you can also do your own brain surgery."

The PTO advises inventors not to file their own patent applications because "unless they are familiar with these matters, or study them in detail, they may get into considerable difficulty." Malhotra explains that "patent law is very complex and continues to evolve. Words that have one meaning in common parlance, may have been construed a completely different way by courts evaluating a patent case."

Only employ the services of an agent or an attorney registered with the PTO. Only registered attorneys and agents can represent clients for consideration before the PTO. Both Moyer and Malhotra warn inventors to be aware of invention marketing and development firms that take upfront fees. Many of these firms make their income from the inventors and not the inventions which they are developing. "Get a referral from your business attorney, or friends who are attorneys," says Malhotra. "Ask exactly what services will be performed, and what results should be expected."

The PTO publishes a directory of all registered patent attorneys and agents. The directory can be found at the PTO's website, www.uspto.gov. You also can purchase the directory from the U.S. Government Printing Office. Employ the services of a patent attorney or agent before making any marketing decisions, advises Malhotra.

Even if you plan to use a patent agent or patent attorney, you should still learn the rules and expectations for securing a patent. The PTO has strict rules, parameters, and fees. Learning what is expected will streamline the process and save money in preparation fees, filing fees, and downtime before the patent is secured. Here is a basic layout of the road from idea to patent:

1. Study and model the idea in relation to other similar inventions on the market, or in the works. Make sure it is not only a good idea, but also has marketing and manufacturing potential. A great idea is useless, if it can't be made or brought to the market.

2. File a disclosure statement with the PTO. This document provides evidence of the date of conception for the invention. It is not an application for the patent.

The disclosure statement should contain clear and concise information, including the process for making and using the invention; a drawing or sketch, if necessary; and the use of the invention. The disclosure statement must be accompanied by a signed cover letter requesting the material to be forwarded to the Disclosure Document Program. Later on, the disclosure statement may help determine who had the first idea, but this is no substitute for accurately detailed dates and records. The PTO will hold this statement for two years. After two years, the disclosure statement is destroyed, unless it is referred to in a separate patent application filed within those two years.

3. Make a preliminary search of existing patents to find ones that are closely related to, or the same as the invention. The PTO has search rooms in Washington, D.C., and in other libraries throughout the United States. These search rooms are designated Patent and Trademark Depository Libraries.

4. From the results of the search determine the differences that exist between the invention and the related patents. Evaluate the invention to make sure that it is new, and that it is useful enough to warrant filing an application.

5. If you determine that your invention will make a valuable contribution, and is "sufficiently different," then file a patent application. Malhotra stresses the importance of consistent terminology in writing a patent application. "For example," he says, "if you say that the invention involves inserting a sound card into your computer, you are implying that the term 'computer' is defined so as not to include computers with sound cards. You probably should have said that the computer includes a housing, and a sound card in the housing." Moyer warns that, "Most patents are duds because the person who wrote the patent did not understand the invention, and left ambiguities so that the patent is nearly worthless."

Four Basic Parts

There are four basic parts to the patent application:

(a) A written document with specifications, descriptions, and claims. PTO says this document must contain: "a written description of the invention and of the manner and process of making and using it." It must "be in such full, clear, concise, and exact terms as to enable any person skilled in the technological area to which the invention pertains, or with which it is most nearly connected, to make and use the same." Pay special attention to the claims. These are descriptions of the subject matter of the invention. Malhotra explains that claims "are used to define the scope of your invention, and provide a verbal description of the metes and bounds of your invention." A good attorney or agent will try to secure the broadest claims possible, but since there will be a monopoly on the invention for 17 years, the examiner will typically reject some or all of the claims in the initial application.

(b) A drawing. The PTO has strict rules for what the drawing must show and how it must appear. Know all these parameters.

(c) The filing fee.

(d) An oath or declaration. The oath is required by law. The applicant must take an oath that states he or she believes that they are the "original and first inventor" of the invention. The oath must be sworn in front of a notary or other authorized officer.

The application is not forwarded to an examiner until all the parts are received. The PTO defines the filing date of the application "as the date on which the names of the inventors, a specification (including claims), and any required drawings are received in the Patent and Trademark Office; or the date on which the last part completing the application is received."

6. When the completed application reaches an examiner, he or she will study the invention in relation to other patents. The examiner may cite objections, or reject the claims of the application. Applicants have to overcome the rejections raised by the examiner by demonstrating how the invention differs from those that have already secured patents. PTO says "it is not uncommon for some or all of the claims to be rejected on the first action by the examiner; relatively few applications are allowed as filed."

7. Respond, in writing, by distinctly and specifically (and tactfully) pointing out the errors in the examiner's action. Simply telling the examiner that he or she has erred will not work, you must prove your case.

8. After the response is reviewed, you will be notified if your claims have been rejected, or objections or requirements have been made. PTO says, "the second Office action usually will be made final."

9. Rejections may be appealed to the Board of Patent Appeals and Interferences.

10. If the application is approved, you will receive a notice of allowance. The fee for issuing the patent is due within three months of the date of notice. Once the fee is paid, the patent is issued as soon as possible.

11. Once the patent is issued, a maintenance fee is due 3.5, 7.5, and 11.5 years after the original patent has been granted.

The PTO averages 18 months from filing to issue on patent applications, and they grant patents about 66% of the time.

Deepak Malhotra recommends the

PENTON'S

Electronic Design

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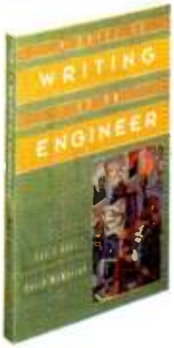
Books

A Guide to Writing as an Engineer

David Beer and David McMurrey



This essential guide focuses on what is important for engineering writing in particular, rather that just technical writing in general. Clearly explains all key writing concepts and covers content, organization, and format. Also provides complete coverage of computer communication, e-mail, and finding information on the Internet. Practical, relevant examples of solid engineering writing throughout help you apply the material covered right away.

book, $31.95, Item B2493PM

Web Page Design: A Different Multimedia

Mary E.S. Morris

Written for Web page authors, this hands on guide covers the key aspects of designing a successful web site including cognitive design, content design, audience consideration, interactive, organization, navigational pathways, and graphical elements. Includes designing for VRML and Java sites as well as designing with templates, style sheets and Netscape Frames.

book, $24.95, Item B2421PM

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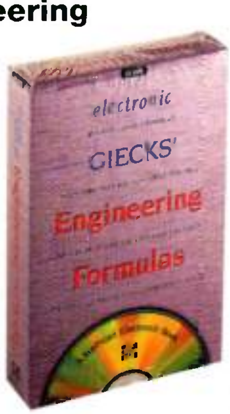

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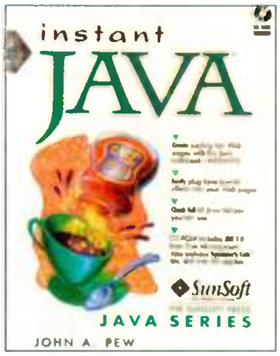

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book, "Marketing your Invention," available from the American Bar Association, Section of Patent and Trademark and Copyright Law, 750 North Lake Shore Dr., Chicago, Ill. 60611.

Securing a patent can be a profitable venture but remember, the best invention isn't going to walk out of your head and into the bank. "You must make the plan," says Moyer. "You must do the work. And you must get the best help. There are no shortcuts.

Other Resources

The majority of the PTO resources cited in this article were found at the U.S. Patent and Trademark Office homepage located at www.uspto.gov. It is an excellent and thorough resource for inventors. Be sure to visit Deepak Malhotra's homepage, another excellent resource for patent information. It has many links to related websites. It is located at www.ior.com/~malhotra/. Don Moyer's homepage is located at www.donmoyer.com. His site provides a wealth of information for inventors, including a schedule of his workshops.

The IEEE homepage also has resources devoted to patents. They are located at www.ieee.org. They also have a book available called "Successful Patents and Patenting for Engineers and Scientists." It is a beginner's manual that covers both U.S. and international concerns. It is available at the homepage. Ideas Digest Online news magazine, located at www.ideas.wis.net, has a section entitled Inventor's Corner, which is a forum for inventors. Finally, search engines such as Yahoo or Alta Vista will yield these sites and others, including sites for patent attorneys, patent agents and search firms.

Eric Hausler is a freelance writer specializing in writing on issues of concern to electrical and electronic engineers. He can be reached by phone, at (201) 635-0311 or by e-mail, at: erich@openix.com.

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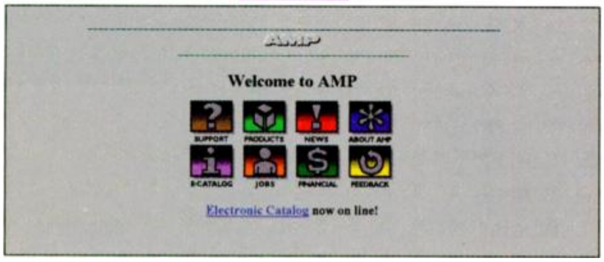

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ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

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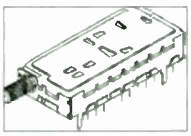

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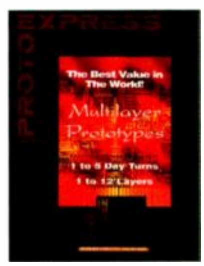

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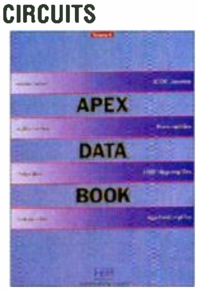

CIRCLE 262

APEX

MAXWELL ON TARGET

Electromagnetics based EDA solutions for high speed and high frequency design. 2D/3D RLGC extraction and SPICE model generation for high speed interconnects, IC packages. Signal integrity, ground bounce, and EMI enclosure design rules. S-parameters, antenna parameters including gain, directivity for RF and microwave design.

CIRCLE 263

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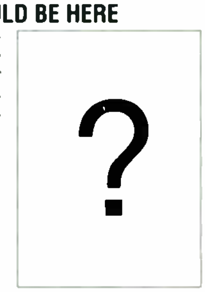

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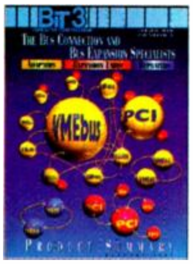

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MINI-CIRCUITS

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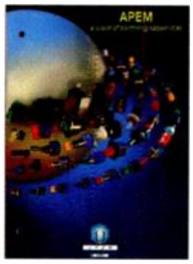

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APEM

80186, 80196, 8051 EMULATION

Signum Systems has released its 1996 catalog of in-circuit emulators. This full line catalog includes Intel processors, Texas Instruments DSP's Zilog controllers, and National Semiconductor HPC family. Call (800) 838-8012 for information. Internet address: ww.signum.com

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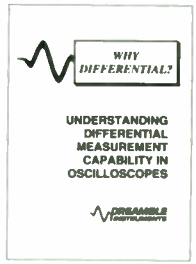

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PREAMBLE INSTRUMENTS

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Teltone's 224-page Databook features a wide range of products for network interface applications, including: DTMF Receivers, DTMF Transceivers w/Call Progress Detection, MF Trunk Signaling ICs, Call Progress Tone Detectors, Line Sensing Relays, test tools including Telephone Line Simulators and ISDN Line Simulators, application notes, and more. For your copy call 1-800-426-3926 or 206-487-1515, E-mail at info@teltone.com.

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TELTONE

"X86 and 683xx/HC16 Design Tips"

Free application note shows how to use in-circuit emulation to isolate real-time events. Set clock-edge triggers, and then use trace to display system status and the source code leading up to the event. For immediate response: WEB page: www.microtekintl.com
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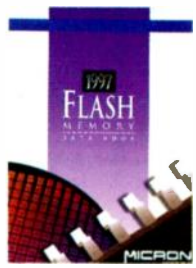
MICROTEK INTERNATIONAL

1997 FLASH MEMORY DATA BOOK

The 1997 Flash Data Book from Micron Quantum Devices, Inc. is now available. This updated edition features sections on our industry-standard, IntelÒ - compatible 2,4 and 8 Meg SmartVoltage Boot Block Flash memories, and future products such as 8 and 16 Meg Sectored Erase Flash and the Flash ATA and CompactFlashÒ Card families.



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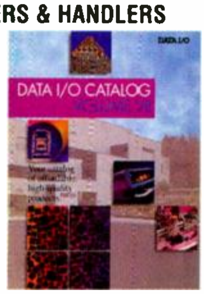

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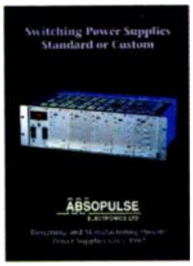

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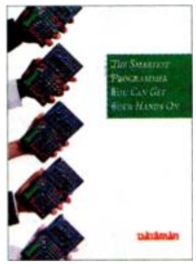

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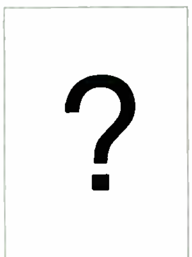

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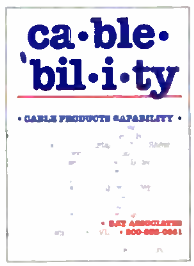
CABLE PRODUCTS CAPABILITY GUIDE

Designed to aid engineers in their cable, wire, assembly, and high-tech interconnect applications, this free Cable Products Capability Guide from Bay Associates, Menlo Park, CA, features the company's unique products, services, materials and processes.



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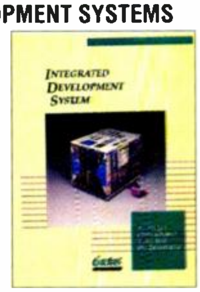

CACTUS LOGIC

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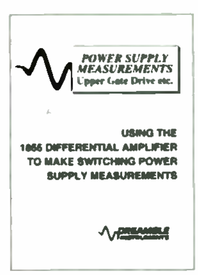
APPLICATION NOTE

Covers how to make safe and reliable measurements on switching power supplies operating on line. Includes such difficult measurements as upper gate drive and transistor saturation characteristics. Tells how to quantity measurement corruption caused by high dv/dt common mode. 1-800-376-7007



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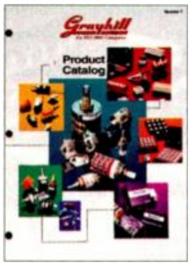

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GRAYHILL, INC.

OMRON RELAYS, SWITCHES, MORE

Standard Product Catalog shows Omron's most popular relays, switches, and sensors. The 176 page catalog also includes card readers, time delay relays, totalizers, limit switches and temperature controllers. Literature sent only to addresses in the U.S.A. Omron Electronics, Inc. Call toll-free 1-800-55-OMRON or e-mail EDLit@oei.omron.com

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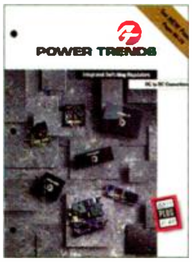
OMRON ELECTRONICS, INC.

NEW SWITCHING REGULATORS

Power Trends, Inc. has released a new 80 page full-line catalog for its complete line of Integrated Switching Regulators and DC to DC converters. the catalog introduces significant new products along with extensions to existing product lines. Complete specifications, photos and standard applications are provided for each product along with mechanical configuration options and ordering information.



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POWER TRENDS, INC.

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Western Design Center's product selection and developer guide describes our 65C02-BASED CMOS low power IC microprocessors. Included is information about our chips, boards and licensable cores.

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C&K COMPONENTS INC.

ENCLOSURES & ACCESSORIES AVAILABLE

Bud Industries' new Standard Products Catalog provides technical data and ordering information on over 3,000 products ranging from large relay racks and cabinets to desktop and portable instrument cases including a full line of NEMA and other plastic enclosures. Also included is information on computer workstations, custom fabrication and a wide range of enclosure accessories.

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BUD INDUSTRIES, INC.

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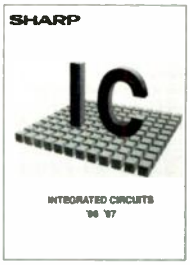
First-in, First-out memories are just the stuff the no-nonsense design environment of the '90s is meant to build on. Used as data buffers between systems operating at different speeds, FIFOs conserve valuable board space, streamline design tasks and reduce system cost.Sharp's new 1997 IC Short Form Catalog is packed with information about Sharp FIFOs.



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SHARP MICROELECTRONICS

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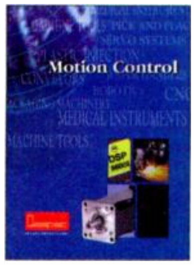

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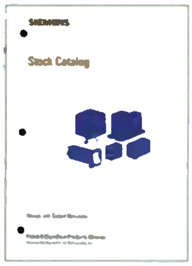
GESPAC

P&B RELAYS & BREAKERS

Catalog lists stock relays and circuit breakers from Potter & Brumfield products division. Describes electromechanical, solid state and time delays, as well as thermal and magnetic circuit breakers. Numerous options. Fax: (812) 386-2072, email: info@ae.sec.siemens.com



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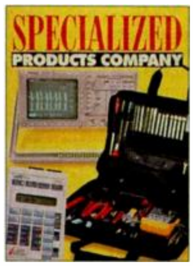

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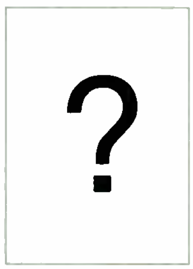

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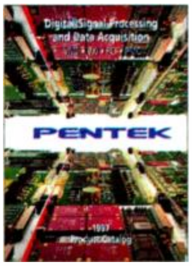
ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

1997 PRODUCT CATALOG



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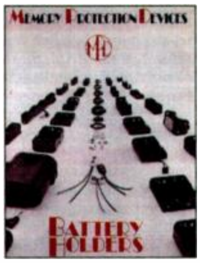

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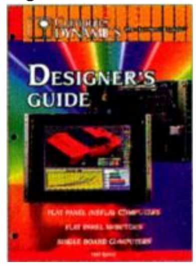
MEMORY PROTECTION

Flat Panel Systems Designer's Guide

Our new 1997 edition "Designer's Guide to Flat Panel Display systems and single Board Computers" offers an extensive range of OEM/end user flat panel display solutions: complete flat panel computers, plug-in flat panel monitors, the latest displays and several touchscreen technologies. Includes complete information on our PC-compatible single board computers.Visit our new website: www.cdynamics.com.



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COMPUTER DYNAMICS

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INTERCONNECT PROCESSING HANDBOOK

Samtec's Interconnect Processing Handbook addresses common problems encountered in surface mount and IR compatible board processing. The primary focus is on lowering the total applied cost of printed circuit boards through improved overall manufacturability. The major issues addressed are SMT interconnect placement and infra red soldering. Phone: 800- SAMTEC9. Fax: 812-948-5047.

CIRCLE 316

SAMTEC INTERCONNECT

Free CD-ROM Instrumentation Reference

The Windows- compatible Instrupedia - Your Interactive Encyclopedia for Instrumentation - features more than 60 tutorial and "how-to" application notes to help users learn how to combine hardware and software to built computer-based systems for instrument control and data acquisition, analysis, and presentation. Instupedia includes more than 20 User Solutions.

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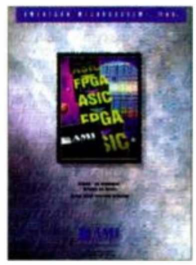

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AMERICAN MICROSYSTEMS INC.

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SCHURTER AG

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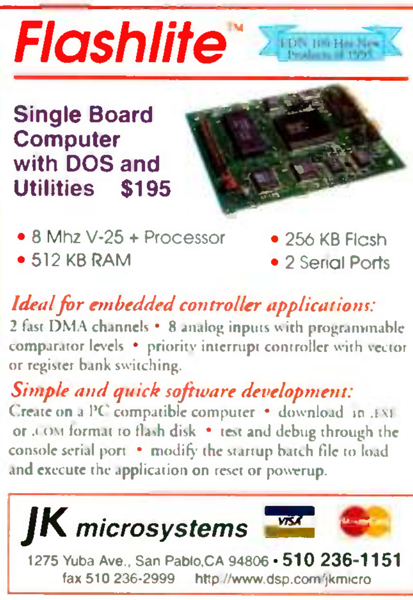

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109 to 144	$390	$460	$780	$910	$1700	$2650
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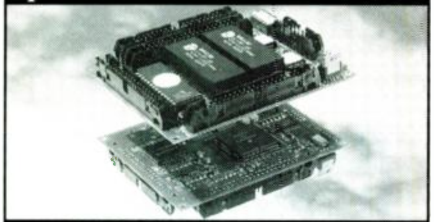

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L2
01 ☐ Emulators/Debuggers

M Computer Peripherals
01 ☐ Disk/Tape Drives
02 ☐ Computer Terminals
04 ☐ Monitors
08 ☐ Graphics Terminals
16 ☐ Printers/Plotters
32 ☐ I/O devices (Mice, keyboards, etc.)

M2
01 ☐ PCMCIA Cards
02 ☐ CD-ROM, including WORM & R/W
04 ☐ Multimedia Peripherals

☐ **NONE OF THE ABOVE**

11. Number of employees in your company? ____

12. Please check the publications that you receive personally addressed to you by mail: (check all that apply)

N
01 ☐ Computer Design
02 ☐ ECN
04 ☐ EDN
08 ☐ EE Times
16 ☐ Electronic Product News

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01 ☐ Electronic Products
02 ☐ PC Week

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SBL-1	1-500	5.5	45	40	+7	4.50
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SBL-1Z	10-1000	6.5	35	25	+7	7.25
SBL-1-1	0.1-400	5.5	45	40	+7	7.25
SBL-3	0.025-200	5.5	45	40	+7	7.25
• SBL-11	5-2000	7.0	35	30	+7	18.75
SBL-1LH	2-500	5.8	68	45	+10	5.65
SBL-1-1LH	0.2-400	5.2	64	52	+10	8.20
• SBL-1XLH	10-1000	6.0	40	55	+10	7.25
SBL-2LH	5-1000	5.9	61	54	+10	8.20
SBL-3LH	0.07-250	4.9	60	53	+10	8.20
• SBL-11LH	5-2000	7.0	45	30	+10	19.70
SBL-1MH	1-500	5.5	45	40	+13	9.80
SBL-1ZMH	2-1100	6.5	40	25	+13	11.70
• SBL-2500H	5-2500	6.0	44	44	+[illegible]	31.90
• SBL-173SH	5-1200	5.9	35	35	+17	20.65

• IF not DC coupled

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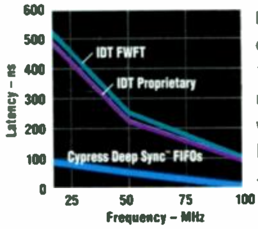

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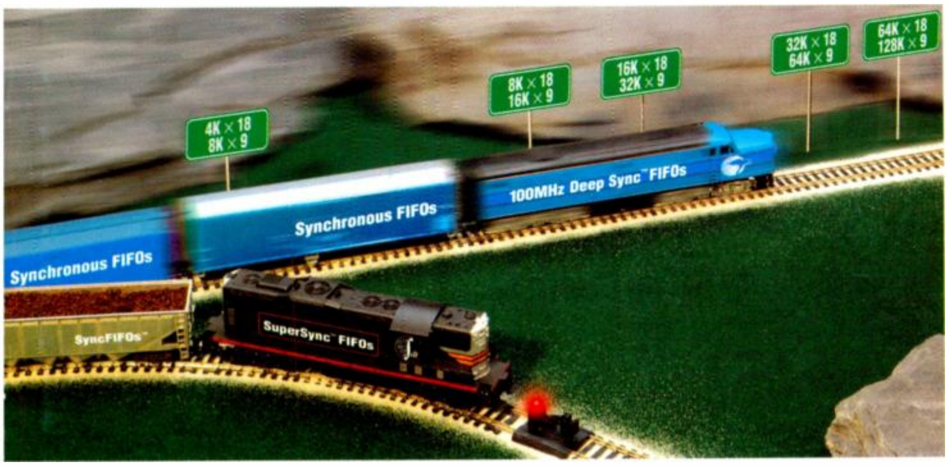

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Deep Sync FIFO Feature Comparison

	IDT	CYPRESS	CYPRESS ADVANTAGE
Sync Architecture			
	Proprietary FWFT	Industry Standard	All Cypress sync FIFOs are pin-compatible
Frequency Select Pin			
	FS Select pin	Clocks can be async	Does not limit range of operation
Depth Expansion			
	Serial cascade	Token passing	Low latency and low power
Power (f=20MHz)			
×18:	~180mA	~100mA	Lower power
×9:	~150mA	~50mA	Lower power
×9 Package			
	14 × 14 TQFP	7 × 7 TQFP	Smallest ×9 packaging for all sync FIFOs

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