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FOR ENGINEERS AND ENGINEERING MANAGERS - WORLDWIDE

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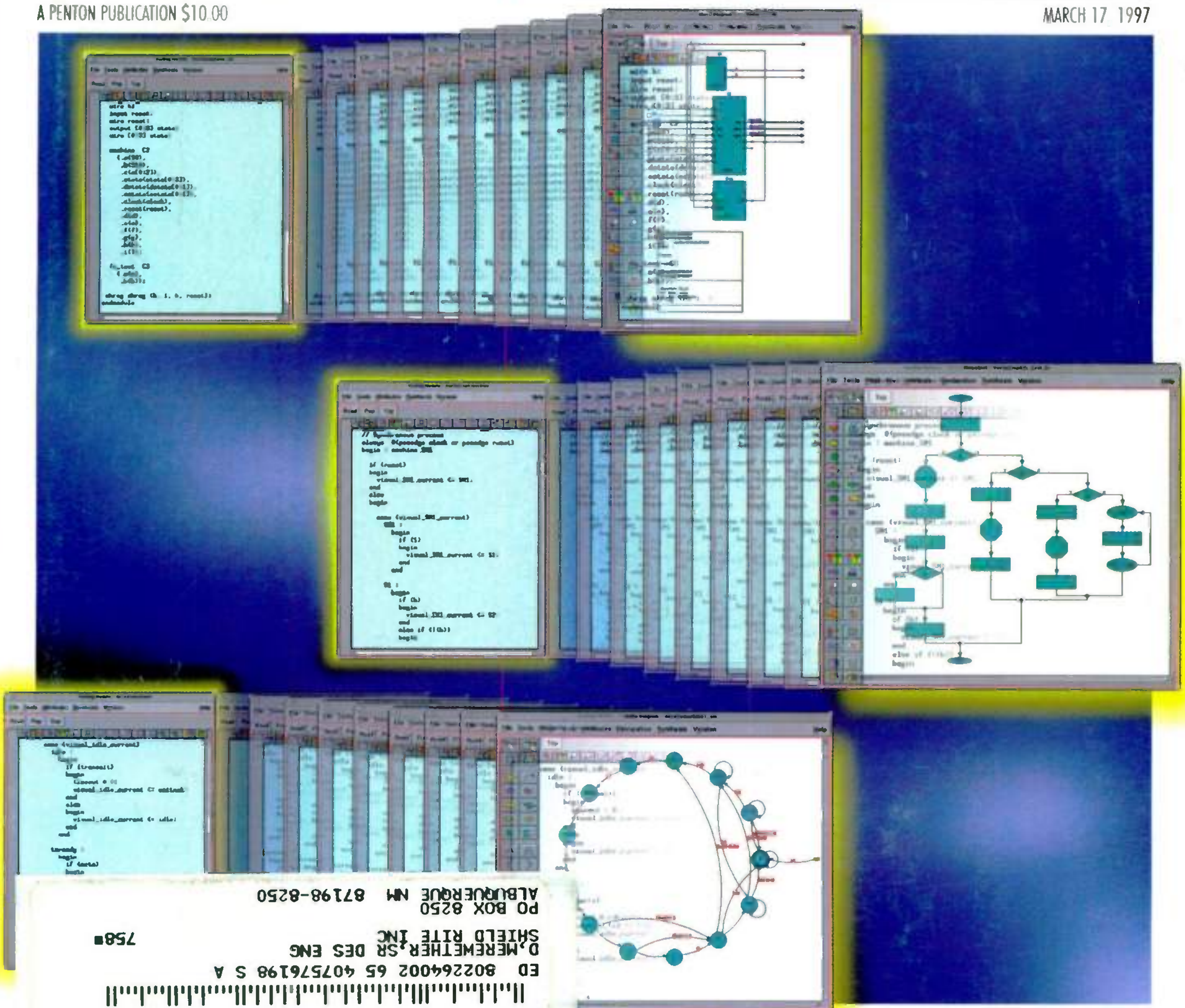

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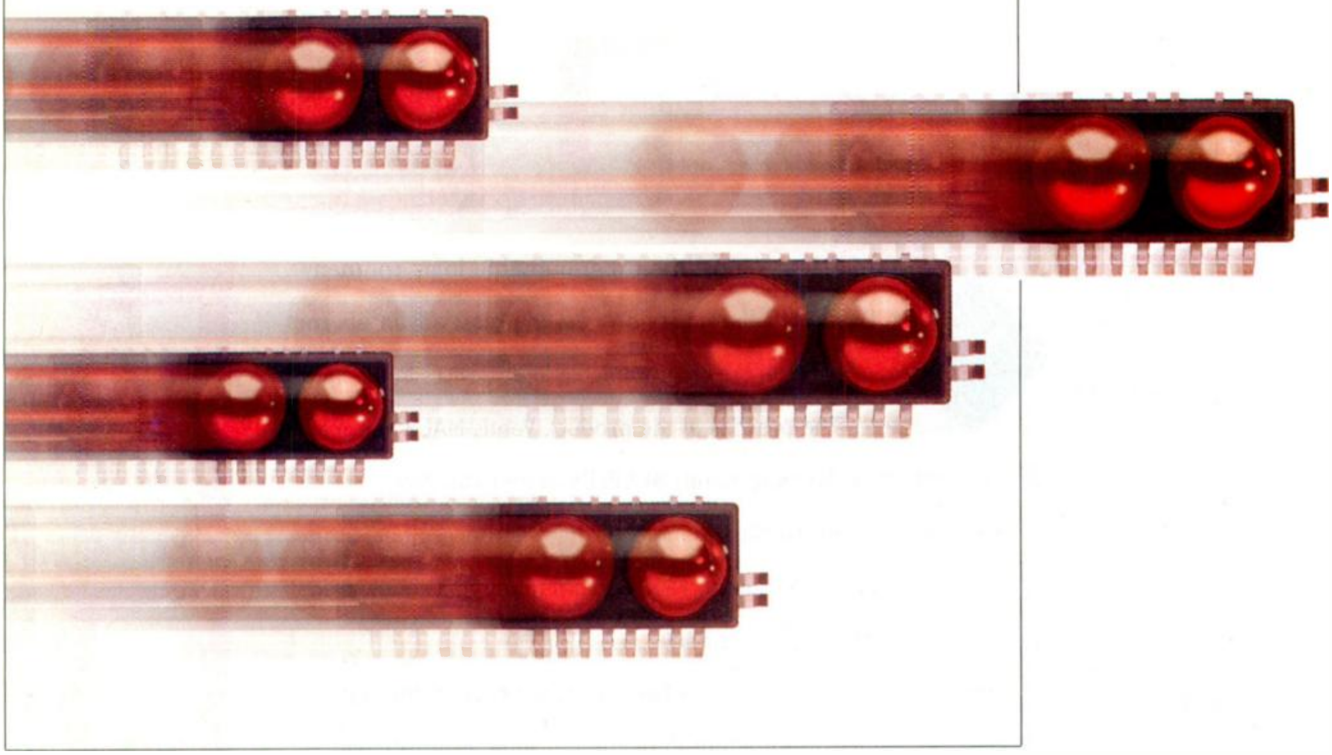

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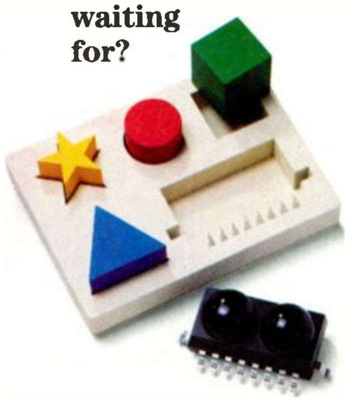

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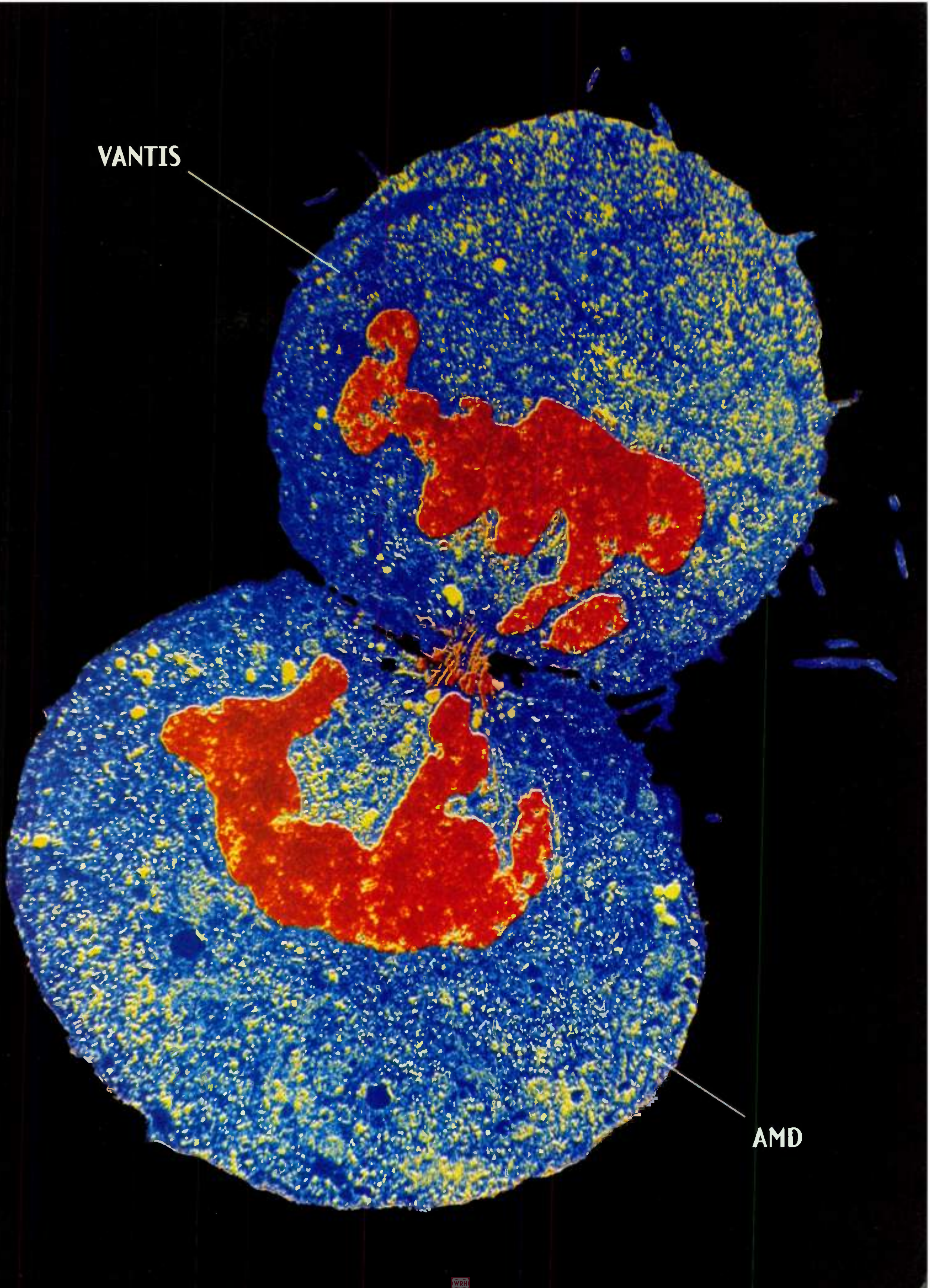
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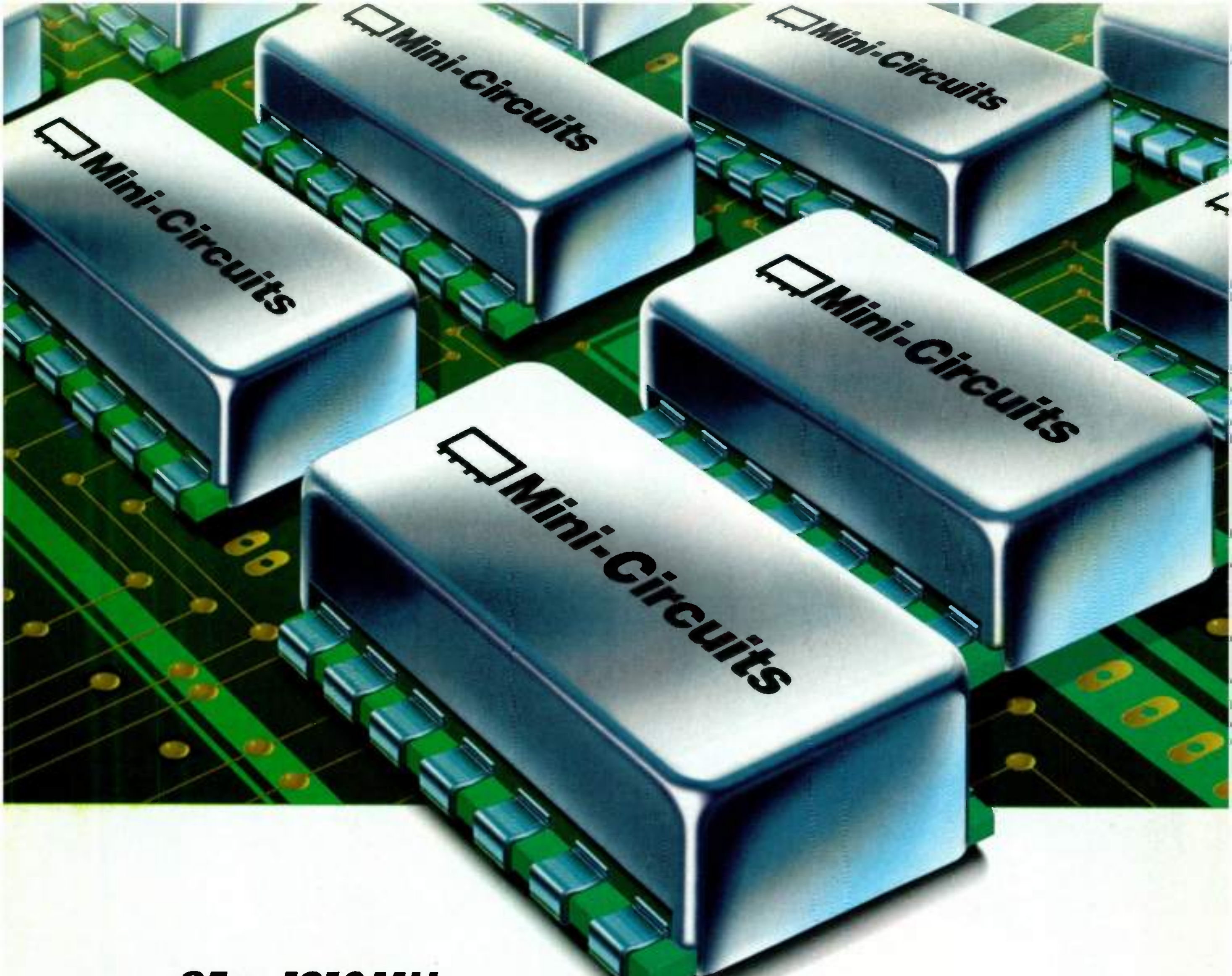

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JTOS-200	100-200	-105	-25	16V	20	13.95
JTOS-300	150-280	-102	-28	16V	20	15.95
JTOS-400	200-380	-102	-25	16V	20	15.95
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JTOS-1300	900-1300	-95	-28	20V	30	18.95
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ELECTRONIC DESIGN

March 17, 1997 Volume 45, Number 6

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March 17, 1997 Volume 45, Number 6

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TEST & MEASUREMENT

QUICK LOOK

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ELECTRONIC DESIGN

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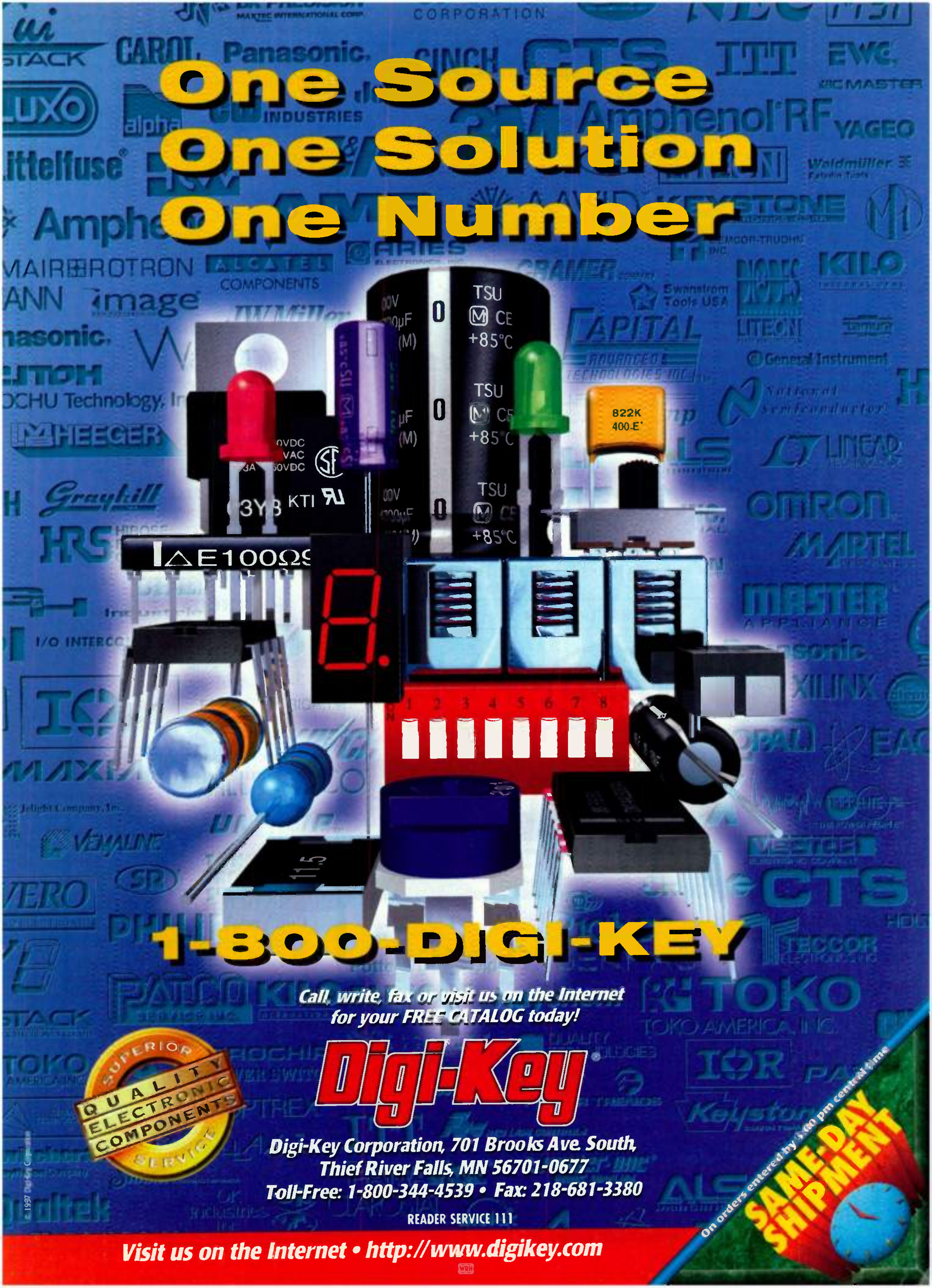
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MARCH 1997

Communication Design Engineering Conference, Mar. 24-26. Washington, DC. Convention Center, Washington, DC. Contact Denise Chan, Miller-Freeman Inc., (415) 278-5231.

Portable By Design Conference and Exhibition, Mar. 24-27. Santa Clara Convention Center, Santa Clara, CA. Contact Betsy Tapp, (201) 393-6075; fax (201) 393-6073; e-mail: portable@class.org.

Communication Design Engineering Conference, Mar. 25-27. Washington Convention Center, Washington, DC. Contact (617) 821-9219; e-mail: cdec@exporeg.com.

DSP World Spring Design Conference, Mar. 25-27. Washington Convention Center, Washington, DC. Contact Denise Chan, Miller Freeman Inc., (415) 278-5231; e-mail: dsp@exoreg,com.

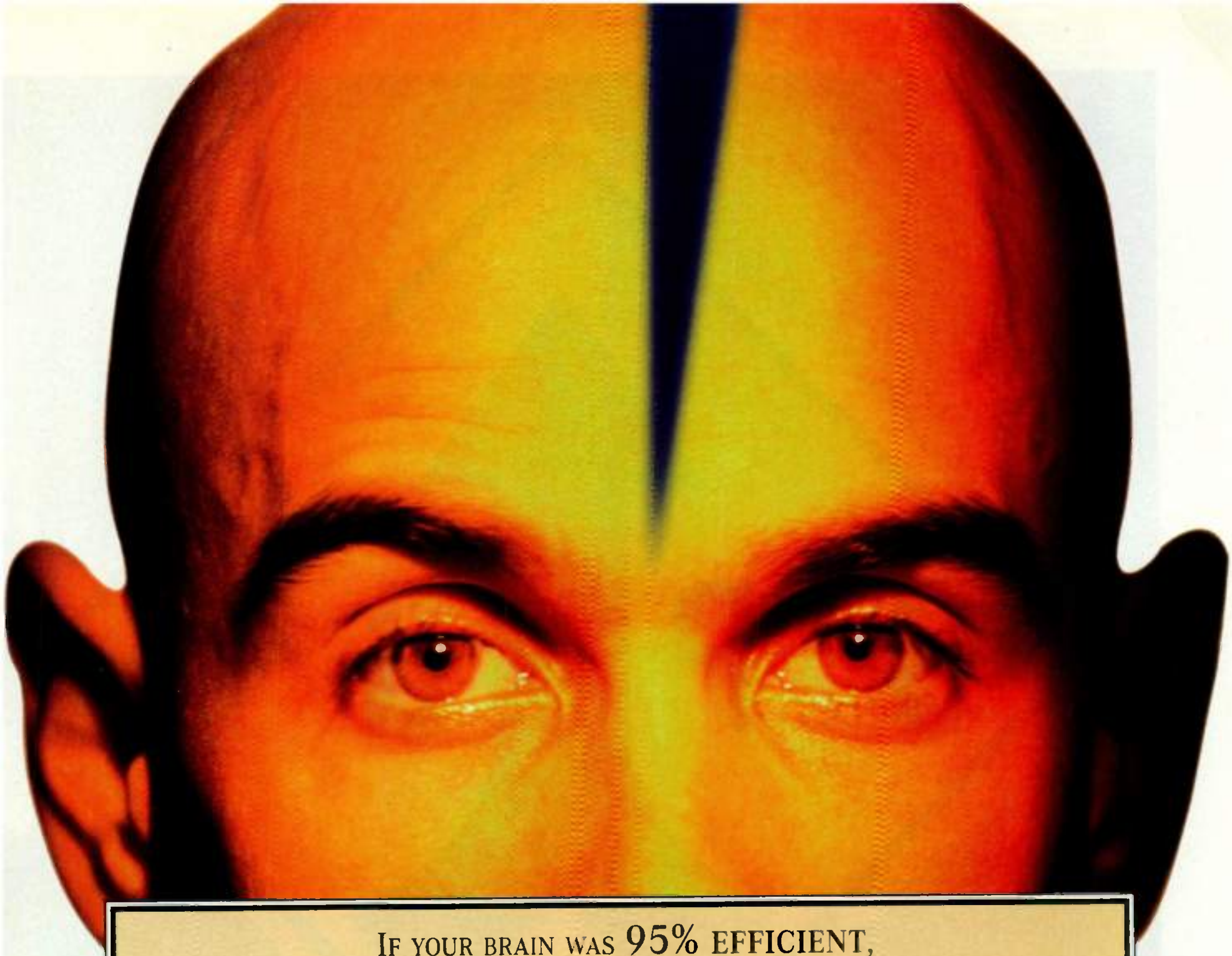
SOUTHCON '97, Mar. 25-27. Raleigh Civic and Convention Center, Raleigh, NC. Contact Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045; (800) 877-2668 ext. 243; fax (310) 641-5117; e-mail: southcon@ieee.word.org.

Second Conference on The New Integrated Service Provider (Supercarrier '97), Mar. 26-28. Washington Vista Hotel, Washington, DC. Contact (800) 822-6338 or (202) 842-3022 ext. 317; Internet: http://www.brp.com.

Sixth International Verilog Conference, Mar. 31-Apr. 2. Santa Clara Convention Center, Santa Clara, CA. Contact MP Associates, 5305 Spine Rd., Suite A, Boulder, CO 80301; (303) 530-4562; fax (303) 530-4334; e-mail: ivcinfo@ivcconf.com.

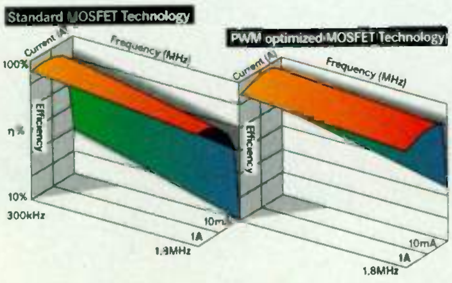
APRIL

INTERMAG '97, Apr. 1-4. Hyatt Regency Hotel, New Orleans, Louisiana. Contact John Nyenhuis, School of Electrical Engineering, Purdue University, West Lafayette, Indiana 47907-1285; (317) 494-3524; fax (317) 494-2706; e-mail: nyenhuis@ecn.purdue.edu.



IF YOUR BRAIN WAS 95% EFFICIENT, YOU COULD PROBABLY DERIVE π TO A BILLION PLACES, ORDER PIZZA TELEPATHICALLY, AND LEVITATE SMALL PETS. SO JUST IMAGINE WHAT YOU CAN DO WITH **MOSFET** TECHNOLOGY THAT ENABLES 95% EFFICIENCY.

Inside all of our craniums lies three pounds of sophisticated, highly-developed and utterly inefficient equipment. Luckily, however, a few of us at TEMIC harnessed some of the power in our gray matter and created something infinitely more efficient–PWM-optimized LITTLE FOOT™ MOSFET technology.



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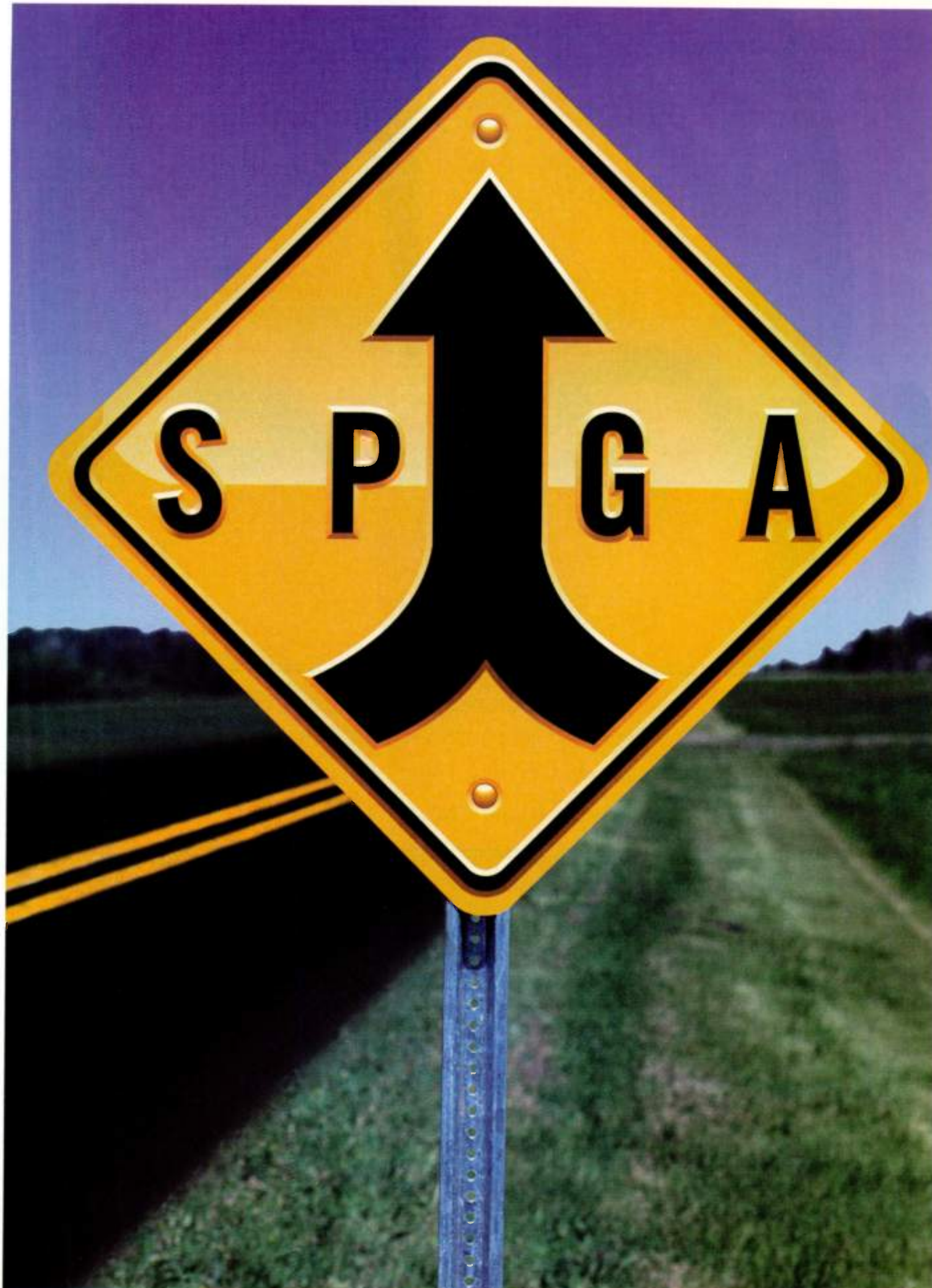
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Surface-Mount Technology Association, Apr. 2. Gwinnett County Civic Center, Atlanta GA. Contact (770) 569-1822; e-mail: smta-info@t-tech.com; Internet: http://www.smta.org.

IEEE International Reliability Physics Symposium, April 7-10. Adams Mark Hotel, Denver, CO. Contact IRPS Publishing Services, P.O. Box 308, Westmoreland, NY 13490; (315) 339-3971; fax (315) 336-9134; e-mail: 103227.2074@compuserve.com.

IEEE Conference on Computer Communications (INFOCOM 97), Apr. 7-11. Kobe, Japan. Contact Tatsuya Suda, Dept. of Information & Computer Science, University of California, Irvine, CA 92717-3425; (714) 824-5474; fax (714) 856-4056; e-mail: infocom@ics.uci.edu; Internet: http://www.ics.uci.edu/infocom/ (North America); http://arpeggio.ics.es.osaka-u.ac.jp/infocom.html (Japan).

Fourth ASAT Conference, Apr. 14-16. San Francisco Airport Marriott, San Francisco, CA. Contact Suzanne Graf, Project Manager, (541) 984-5204; fax (541) 343-7024; e-mail: SGraf@Advanstar-Expos.com.

IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP 97), Apr. 21-24. Gasteig Cultural and Convention Center, Munich, Germany. Contact Bernd Girod, Lehrst.f.Nachrichtentechnik, Univ. of Erlangen Nuremberg, Cauerstr. 7, D-91058 Erlangen, Germany; (49) 91-3185-7101; fax (49) 91-3131-30840; e-mail: b.girod@ieee.org.

Sixth System Administration, Networking, & Security Conference, Apr. 21-26. Baltimore Inner Harbor, MD. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

IEEE International Conference on Robotics and Automation, Apr. 21-27. Albuquerque Convention Center, Albuquerque, NM. Contact Jerry Stauffer, Intelligent Systems and Robotics Center, Program Office, MS0949, Sandia National Laboratories, Albuquerque, NM 87185-0949; (505) 845-8966; fax (505) 844-6161; e-mail: jdstauf@isrc.sandia.gov.

First Convergence Technology & IC Expo, Apr. 22-24. InfoMart, Dallas, TX. Contact Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045; (800) 877-2668, ext. 243; fax (310) 641-5117.

15th IEEE VLSI Test Symposium, Apr. 27-30. Hyatt Regency Monterey, Monterey, CA. Contact Y. Zorian; (408) 543-0146 ext. 227, e-mail: zorian@lvision.com.

MAY

IEEE Vehicular Technology Conference (VTC), May 5-7. Hyatt Regency at Civic Plaza, Phoenix, AZ. Contact Wendy Rochelle, IEEE Conference Services, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331; (908) 562-3870; fax (908) 981-1769; e-mail: w.rochelle@ieee.org.

International Test Synthesis Workshop, May 5-7. Santa Barbara, CA. Contact K. Wagner; (415) 694-4386; e-mail: kwagner@symopsys.com.

IEEE Custom Integrated Circuits Conference (CICC '97), May 5-8. Santa Clara Convention Center, Santa Clara, CA. Contact Melissa Widerkehr, Widerkehr & Assoc., Suite 270, 101 Lakeforest Blvd, Gaithersburg, MD 20877; (301) 527-0902; fax (301) 527-0994; e-mail: cicc96@aol.com.

Electronics Industries Forum of New England, May 6-8. World Trade Center, Boston, MA. Contact Summit Exhibition Management Inc., Norwalk CT; (800) 322-9332; (203) 855-3000; fax (203) 855-3003.

IEEE Power Industry Computer Applications Conference (PICA), May 11-16. Contact T.C. Wong, American Electric Power, 1 Riverside Plaza, Columbus, OH 43215; (614) 223-2235; fax (614) 223-2205; e-mail: t.wong@ieee.org.

IEEE/IAS Industrial & Commercial Power Systems Technical Conference (I&CPS), May 12-15. Wynham Hotel, Philadelphia, PA. Contact Barry Hornberger, Philadelphia Electric Co., 2301 Market St., Bldg N3-1, Philadelphia, PA 19101; (215) 841-4619.

Fifth IFIP/IEEE International Symposium on Integrated Network Management (ISINM '97), May 12-16. Hotel Del Coronado, San Diego, CA. Contact Ann Marie Lambert, BBN Systems & Technologies, 10 Moulton St., Cambridge, MA 02138; (617) 873-3819; fax (617) 873-37776; e-mail: isinm97@bbn.com.

IEEE Particle Accelerator Conference, May 12-16. Vancouver, BC, Canada. Contact M.K. Craddock, TRIUMF, 4004 Wesbrook Mall, Vancouver, BC V6T 2A3 Canada; (604) 222-7341; fax (604) 222-7309; e-mail: craddock@triumf.ca.

Antennas: Principles, Design, and Measurements (Short Course), May 13-16. St. Cloud, FL. Contact Kelly Brown, NCEE, 1101 Massachusetts Ave., St. Cloud, FL 34669; fax (407) 892-0406.

IEEE Radar Conference, May 13-15. Sheraton University Hotel & Conference Center, Syracuse, NY. Contact Michael Wicks, Rome Laboratory, 26 Electronics Pkwy., Rome, NY 13441; (315) 330-4437; fax (315) 330-2528; e-mail: wicksm@rl.af.mil.

Sensors Expo Boston, May 13-15. Hynes Convention Center, Boston, Massachusetts. Contact Expocon Management Associates Inc. (203) 256-4700; e-mail: sensors@expocon.com; Internet: http://www.expocon.com.

47th Electronic Components & Technology Conference, May 18-21. The Fairmont Hotel, San Jose, California. Contact Jim Bruorton, Electronic Industries Association, 2500 Wilson Boulevard., Arlington, Virginia 22201-3834; (864) 963-6621.

The Curse Of Normality

If you watch television or read some of the business magazines, you may have noticed a new advertising campaign for Hewlett-Packard printers in which the tag line is "Built by engineers. Used by normal people." At first, I was put off a little by the contrast implied between engineers and "normal people." How could this company, founded by two of the best engineers of modern times—Bill Hewlett and Dave Packard—which has been a bastion of engineering strength since its founding, issue an ad that could be interpreted as being demeaning to the very people who built, not just the printers, but the whole company? But then, after some thought, I came to another conclusion, and I'd like to be among the first to thank the folks at HP and their advertising agency for calling attention to the far-from-normal capabilities of engineers.

It's clear that they mean for us to interpret the word "normal people" as "average people," because, as I have often pointed out in the past, it's a well-known fact that engineers are well above the average person in terms of intelligence, taste, and in making sensible choices in lifestyle. With an intelligence level residing in the upper reaches of the intellectual spectrum (to complete the analogy, somewhere up around the ultraviolet would seem to be about right), from the time they were children, engineers demonstrated their talents: They always colored within the lines (except, of course, when it was necessary to improve upon the design of the picture), they always printed their names neatly (so that the sure-to-come award certificates would have no unfortunate misprints), and they accepted all the academic accolades with humility. Having survived a rigorous technical education, continually solving "given-nothing, calculate-everything" type problems by invoking the Law of Conservation of Energy, and attributing spurious effects to Coriolis forces, which are much too complex to explain here (actually, we leave those mundane explanations to the physicists), engineers have changed the world, and even created today's world (there's that humility again).

So once again, a tip of the engineering earflap cap to the people behind HP's advertising. Thanks again for reminding people of the absolute lack of normality among engineers at Hewlett-Packard and everywhere else. We worked hard to develop our reputation, so let the rest of the people out there look on in awe or amusement—it doesn't matter, because we enjoy being the way we are.

P.S. One other thing we did for everyone: Long before the buttoned-up MBAs ever thought about it, we were carrying the banner for wearing casual clothes at work— comfortable shirts with soft collars (neckties only when necessary), sensible shoes (when necessary), and well-creased trousers (lots of creases).

Stephen E. Scrupski
Editorial Director
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SERIOUS

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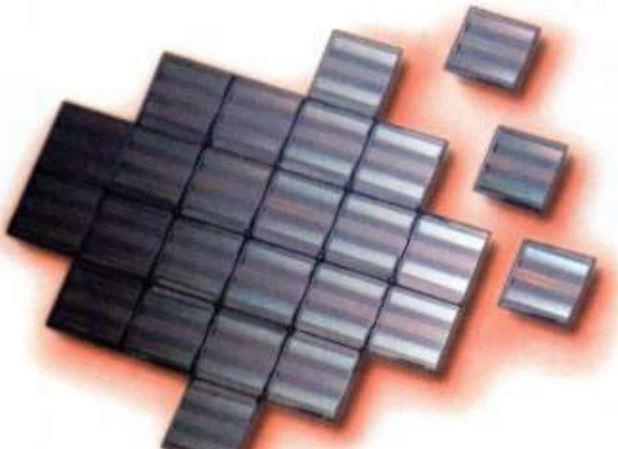

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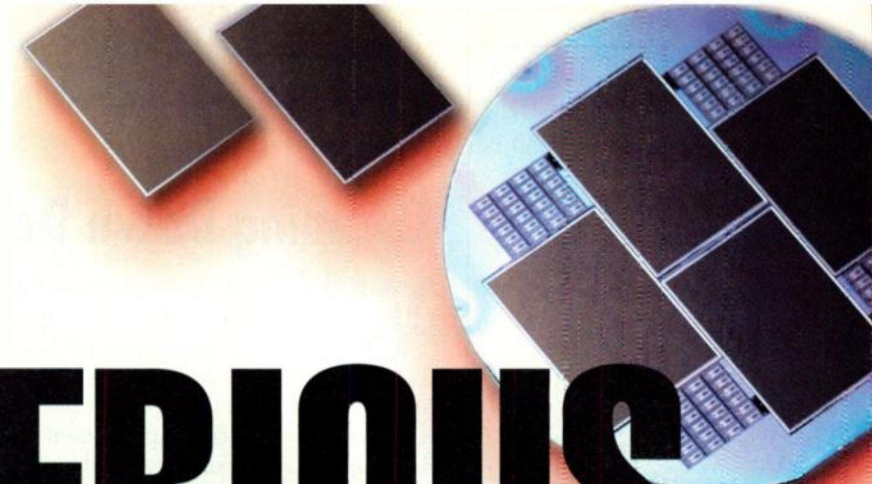

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Dumbing Down Designs

We frequently hear of the increases in speed, the reductions in size, and other benefits of the ever-improving digital IC, whether in a processor or some form of memory. It's easy to measure those changes in a nice ratio in that clean, digital world. These days, analog IC designers and process engineers don't get the opportunity to be patted on the back quite so easily: Calculations as to the improvement of performance are complicated, and are a long way past the simple gain-bandwidth product we used a few years ago.

Things are happening in most device areas—op amps, ADCs, DACs, communications circuits, and filters. Some improvements directly affect how other circuits are implemented. In the data-acquisition world, for example, sampling speeds and resolutions are improving with literally every new announcement from every manufacturer. The improvements are such that the thinking behind both receiver and transmitter implementation is moving solidly to direct conversion. And ADC implementation is limited because the serial interface cannot cope with the data speeds that ICs can now produce.

The continuing development of technology in op amps might seem a bit silly in light of the low dollar return from each product, but the total dollar return from the sheer volume is critically important, and the op amp is a cornerstone for an enormous range of products. Recent developments in op amps are quite staggering, and in just the last six months, we have seen enormous jumps in architectural style and performance with almost every possible parameter looking better. Improved mirror techniques, lower-voltage operation, enormous gains, staggering input impedances, higher drive abilities, lower power consumption, and smaller packages are things we are listening to and learning about every day.

PAUL McGOLDRICK
Westen Regional Editor

While obvious that a large amount of design engineering is concentrated on consumer applications with operation at lower voltages and powers, there is strong evidence that analog engineers will not give up 15-V rails when still practical to use them. With power IC products being manufactured to take telecommunications' 48-V lines directly down to 12 and 15 V, there is likely to be some expansion of such circuits in the future. Since most industrial applications require a 100% rating protection, there are still analog circuit techniques and devices needed with 40-V and higher designs.

But the most noticeable thing about many of today's devices is that they are not being used as designed. This is not the normal edge-of-tolerance stuff that allowed designers to create solutions that work, but which are not supported by specifications from the tested characteristics on the data sheets (a generally foolish activity), but a kind of dumbing-down of designs. A lot of applications engineers on the telephone service lines are seeing this as being the start of a new design era: The lazy design.

For example, we usually don't see the increased resolution of data-acquisition components being used in that way. Instead, the resolution is being used to increase the available dynamic range, helping designers avoid level shifting or gain modifications before driving a conversion circuit. A lot of the available resolution can be wasted, but the circuit design becomes much simpler. There also are an increasing number of op amps that can be described as design-easy, with little to do around the device itself. If the layout is done on a reasonable, clean basis, the circuit will achieve good results.

As a curmudgeon who has done it the hard way, there are feelings of regret about the dumbing down of analog designs. As a practical person, it is good that analog design is widened to allow design engineers to get impressive results quicker. *(Paul McGoldrick's e-mail address is 102447.346@compuserve.com.)*

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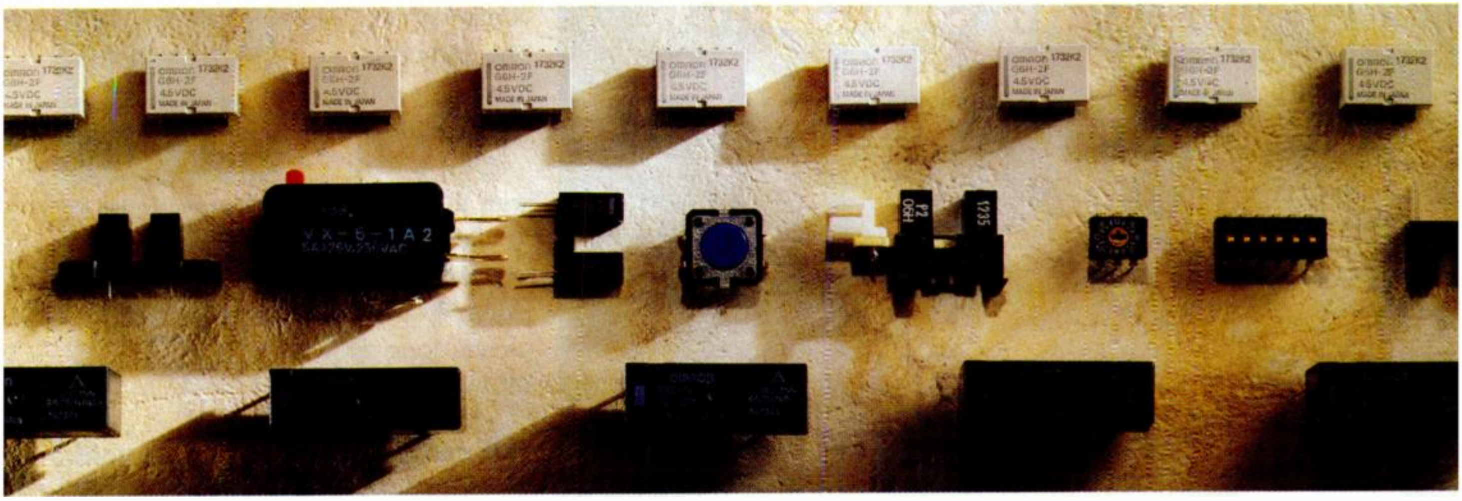

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Novel Image-Stability System Takes The Shakes Out Of Pictures

Image-stabilization techniques in cameras typically consist of gyro-systems to stabilize the whole camera and effectively isolate its positioning from the external vibration. In a completely different approach, an image-stability system developed by Canon neutralizes the shakes in optical instrumentation. Its first use was in a camcorder, and has now extended to binocular optics and other lenses.

The system consists of a standard lens with an additional optical plane in the form of a sealed variable-angle prism system. Two sides of the prism are connected by bellows that are motor-driven to open and close the spacing between the faces of the unit. The prism is filled with a high-refractive-index fluid. When the lens system is horizontal, the two sides of the prism are parallel and the light beam is unaffected. If the lens is tilted forward or backward, the prism's walls are moved, bending the rays of light back to the same, correct focal position. Sensing for movement is from horizontal and vertical sensors that feed a microprocessor, which in turn sends control signals to the motors. Any movement or vibration results in control and changes in the shape of the prism almost instantaneously.

An alternate technology from Canon has a specially-modified group of lens elements that are surrounded by a magnetic coil. Signals in the coil move the lens elements vertically and horizontally with drives through a microprocessor-control system that uses miniature gyros.

For more information, contact Canon USA Inc. at 1-800-OK-CANON; Web: at http://www.usa.canon.com. *PMcG*

Low-Voltage DSP Chips Trim Power To Milliwatts

By scaling the 0.6-mm design rules used to implement a 16-bit DSP chip down to 0.35 mm, operating voltage was able to be scaled to just 1 V, dramatically reducing operating power drain. The low-voltage DSP is a scaled functional duplicate of the TMS320LC545, a 3.3-V circuit previously created by Texas Instruments Inc., Dallas, and described at last month's IEEE International Solid-State Circuits Conference.

To shrink the circuit, design teams from several TI facilities collaborated to readjust the transistor thresholds, convert the analog phase-locked loop to a digital PLL, and scale the features to 0.35 mm and gate dimensions to 0.25 mm. At low supply levels, the digital PLL provides more reliable operation and is less sensitive to voltage variations. The resulting chip operates at 1 V and at speeds of up to 60 MHz while consuming just 17 mW. In comparison, the 3.3-V version of the DSP chip consumes 15 times as much power at the same clock speed.

The chip actually has a wide operating range—down to as little as 0.6 V, and at the high-end when biased at 1.35 V the chip can run at 100 MHz. Two threshold levels are employed for the transistors to optimize their performance—memory cells are implemented using a 300-mV threshold to minimize leakage, while more time-critical logic blocks were built using faster transistors that employ thresholds of 100 mV. Functionally identical to the original 320LC545, the 1.6-million transistor chip employs a modified Harvard architecture with a six-stage instruction pipeline. Although this version of the low-power chip is a test vehicle, a commercial version being developed. *PMcG/DB*

Advanced Silicon-Nitride Tool Runs At High Temps

Operating at high temperatures to perform silicon-nitride deposition, a tool developed by Applied Materials Inc., Santa Clara, Calif., deposits films with superior characteristics over that deposited by batch furnaces. Consequently, pre-metal-layer films such as used in 64-Mbit and 256-Mbit DRAMs, flash memories, and dual-gate CMOS circuits can be formed with high uniformity levels thanks to the precision control possible with the high-temperature processing system.

The high-temperature processing chamber in the HT Silicon Nitride Centura system has a 20°C/second ramp-up and cool-down rate to permit high wafer throughputs, which would make the tool cost-competitive with batch processing systems. The single-wafer, multichamber (up to three chambers) tool also can be clustered with other high-temperature chambers to create integrated processing systems that form oxide-nitride-oxide stacks, and poly-nitride and nitride-RTP films.

For example, when used to implement DRAM capacitors, the system can produce a low-leakage element. This is done by providing in-situ chamber cleaning and a hydrogen-bake process for native-oxide removal, and then depositing the films. During the procedure, the wafer is never exposed to oxygen or moisture. Film defects can be reduced by as much as 50% compared to batch furnaces, while still permitting a throughput of more than 40 wafers/hour in a two-chamber system. Within-wafer thickness variations of deposited films can be kept to less then 1% (1 Σ at a 50 Å thickness). Contact Dr. Stephen Schwartz at (408) 727-5555. *DB*

Step-And-Scan System Delivers 96 Wafers Per Hour

Promising greater lithography throughput, a Step & Scan system combines deep ultraviolet imaging with a high-speed, step-and-scan stage to deliver one of the highest imaging throughputs for 200-mm wafers—more than 96 wafers/hour. The PAS 5500/500 system designed by ASM Lithography, Velfhoven, The

Netherlands, accomplishes the task by projecting a 248-nm wavelength UV light through an illumination slit and onto a retical that scans at speeds of up to 1000 mm/s.

What results is an aerial image that's scanned onto a wafer, moving synchronously with the retical stage at up to 250 mm/s. That forms a 26-by-33-mm image (large enough to pattern two 1-Gbit DRAMs or advanced microprocessors in one exposure field) as "one" exposure site. Thus, field sizes can be extended without requiring larger-diameter, more-expensive lens systems.

Furthermore, the scanning approach reduces low residual lens aberrations by effectively averaging them along the path of the scan. The system also incorporates the company's fourth generation of laser-beam delivery systems and the Aerial illuminator. A continuously variable numerical aperture and 4X projection optics (developed by partner company Carl Zeiss) are extensions of the systems used in the PAS5500/300 deep UV stepper released last year.

The high throughput gives the system one of the lowest operating costs in the industry, and with a typical list price of $7.65 million per system, cost-efficiency is key. Contact Dr. Richard George, (602) 438-0559. *DB*

ACL Middleware To Allow DSP Tools To Produce Executable Code

One problem confronting users of DSP algorithm prototyping tools is that their generic C code output can't be compiled to run on a multiprocessor platform. Therefore, the code is unable to leverage the multitasking, interprocess communications, interrupt, and I/O facilities that are available in run-time environments such as SPOX.

To address this shortcoming, Spectron Microsystems, Santa Barbara, Calif., recently signed a $1.1 million dollar contract with DARPA to develop ACL (Application Configuration Language) middleware. The middleware will enable DSP software-development tools to produce executable code for multiprocessor DSP hardware platforms running the SPOX real-time operating system. The ACL middleware will act as a software layer to provide a hardware-independent interface between development tools and multiprocessor platforms equipped with real-time OSs.

In the first phase of the project, Spectron will work directly with Mercury Computer Systems, the original developer of ACL technology, to develop SPOX ACL middleware. In the final phase, the company will collaborate with Sanders, a Lockheed-Martin company, to produce a specific ACL/SPOX implementation for high-performance embedded computers.Known as HPSC (High-Performance Scalable Computers), it will be based on a distributed network cluster that uses processors. For further information, contact the company at (805) 968-5100, e-mail: info@spectron.com; or surf the web at: http://www.spectron.com. *CA*

Libraries Help To Eliminate Lengthy Download Times

As graphics, audio, and video get more play on the Internet, downloading and storing these files becomes an increasingly time-consuming task. The Redistributed Internet Objects (RIO) Platform offers a high-bandwidth solution that enables users to store graphics and audio data directly on a hard-disk drive. This technique, developed by S3 Inc., Santa Clara, Calif., eliminates the need for lengthy downloads over the Internet.

RIO consists of standardized libraries of graphics textures and audio samples that would be shipped as part of the graphics accelerator IC. Developers can use these standard libraries to create 3D-enabled Web sites. As users enter the site, textures and sounds can be downloaded directly from the hard drives, rather than from the Internet, thereby improving the users experience with that site.

RIO is VRML 2.0-compliant and will be initially supported by Internet 3D designers, Microsoft Internet Explorer 3.0, Netscape Navigator 3.0, and other browsers, authoring tools, and texture and model libraries. S3 will bundle RIO texture and audio databases with future 3D accelerators. Existing customers can download RIO from the company's Web site (http://www.s3.com). For more information, contact the company at (408) 588-8000. *RN*

Project Looks To Merge Antifuse Technology Into CMOS Process

QuickLogic Corp., Santa Clara, Calif., under partnership with the TSMC (Taiwan Semiconductor Manufacturing Company) semiconductor foundry, will work jointly to incorporate amorphous silicon antifuse technology into TSMC's 0.5-µm, three-layer metal CMOS process. The ViaLink metal-layer antifuse technology hosted on this 0.5- µm CMOS process will make it possible to manufacture very-high-density members of QuickLogic's pASIC 2 family with die sizes smaller than what is currently available. Subsequently, FPGA users can exploit significant increases in speed. As devices are migrated from a 0.65-µm to a 0.5-µm process, users can take advantage of die size being reduced by up to 44%.

In addition, designers will be able to cost-effectively obtain FPGAs over 10,000 usable gates without sacrificing performance or usability. On top of that, the two companies are working to shrink the ViaLink metal-layer antifuse technology onto geometries even smaller than 0.5 µm.

For more details, contact QuickLogic at (408) 987-2000; (800) 842-FPGA; e-mail: infor@quicklogic.com. Or you can check out the company's web site at http://www.quicklogic.com. *CA*


[Hey: this is big.]
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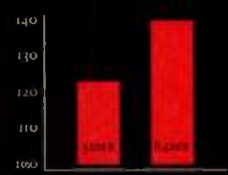

Check it out: going from 32MB to 64 MB of memory makes a 200 MHz Pentium Pro-based system 13% faster.

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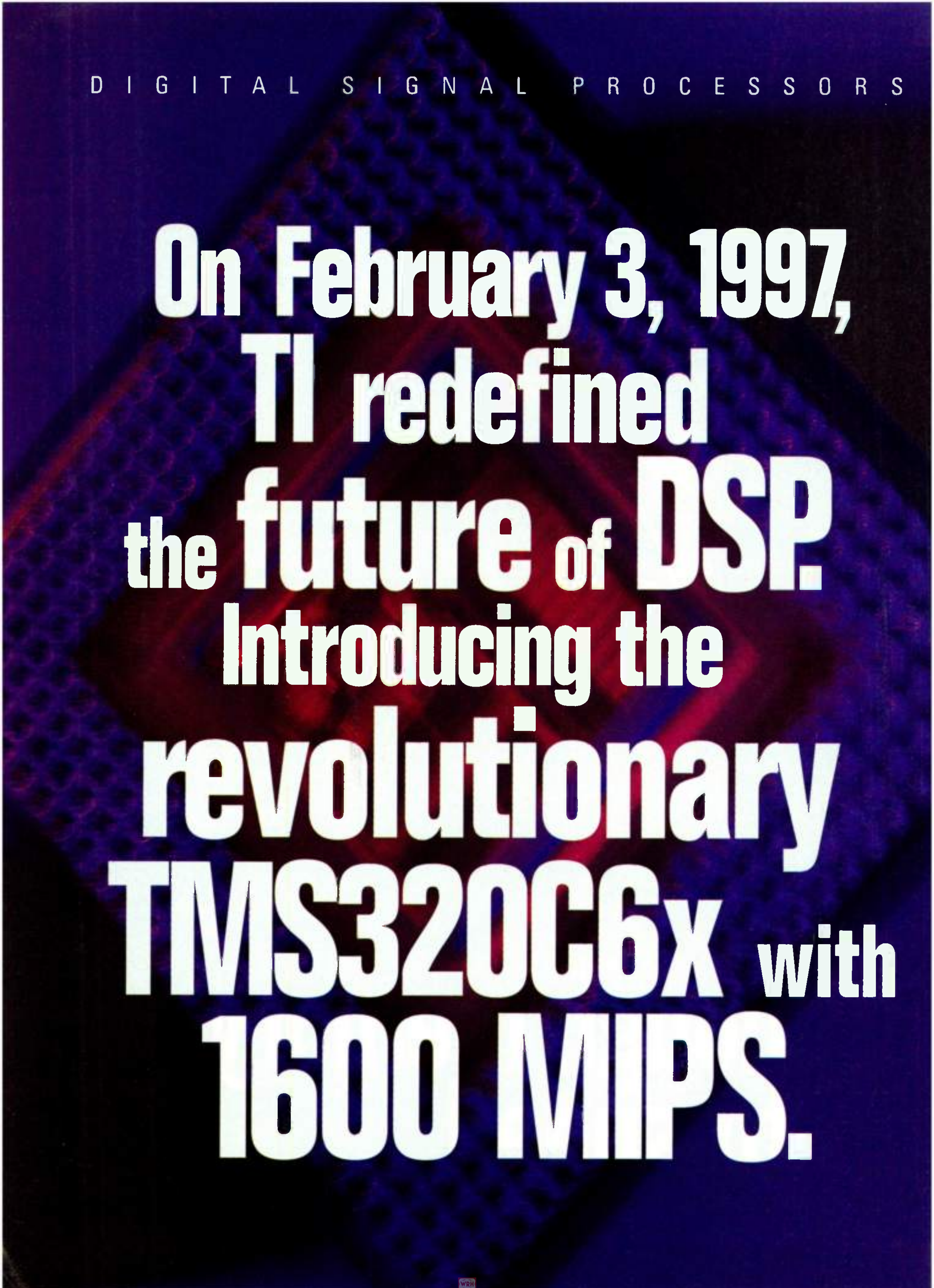
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Specialized Algorithms, Combined With Supercomputer Technology Promise Improved Cancer Radiation Therapies

Recent advances at Lawrence Livermore National Laboratory, Livermore, Calif., combining supercomputing power in PCs with specialized algorithms, are raising hopes for more accurate radiation treatments of cancer patients. The work is being performed in the Lab's Physics and Space Technologies Section. Scientists there have developed a new technology, named Peregrine (for St. Peregrine, to calculate the radiation dose in the body using microscopic particle-interaction data.

By comparison, present clinical calculations treat the patient as a mass of water, with only simple corrections for air cavities, lungs, organs, and bones. Using a patient's Cat scan, medical doctors can employ their own knowledge of radiation therapy to map out a plan of attack by determining where and how much radiation should be given. The radiation treatments are then delivered. Because this method is inaccurate, patients typically suffer a number of side effects from too much radiation, or worst of all, not enough, allowing cancers to spread.

Recent estimates suggest that of the more than 300,000 cancer patients in the U.S. who are treated today, over 100,000 die with active tumors at the primary site. Improved dose calculations through Peregrine could potentially save tens of thousands of these patients each year, according to the Livermore scientists.

Peregrine's advanced-modeling technology is made possible through the use of the Monte Carlo mathematical technique to track radiation. Monte Carlo code has been available for some time, and often is used by the Electronic Design Automation (EDA) industry for simulation purposes *(see "Monte Carlo Analysis In Operation," p. Below)*. While the basic code and implementation of the Monte Carlo analysis is the same, Livermore's researchers have developed specific models to make it radiation-treatment specific.

By sampling millions of the trillions of particles that enter the body, or, in effect, simulating the transportation of energy, Peregrine can develop an accurate representation of the dose in the body. In this way, the radiation dosage can be adjusted to attack the cancer cells while sparing healthy tissue.

Christine Hartmann Slantar, the principal researcher leading the Livermore team explains, "The process is like trying to predict the pattern of a spilled pail of sand. It is impossible to tell where each grain of sand is going to go, but you can still predict the shape of the pile." This process enables doctors, in a clinical setting, to one day predict damage to tumors with a greater chance of eradication.

Until July 1996, the process of performing a single Monte Carlo calculation on a Cray computer would have taken about a month to complete. Now, though, with supercomputer technology available on a PC, the en-

Monte Carlo Analysis In Operation

Today many engineers are using analog-simulation tools with statistical analysis capabilities, and only running basic dc-time or frequency-domain simulations for design verification. In such a scenario, the use of Monte Carlo statistical analysis, provides a large amount of crucial information on how a design will operate in the field.

Monte Carlo simulation works by performing multiple simulations. During each simulation run, a group of component parameters are varied within their statistical distributions. The results are a representation of the way the design will operate over a number of design builds. From these simulations, decisions can be made on how tight tolerances of components should be, or whether a device should be replaced in favor of a more accurate one.

In operation, the designer first must choose which parameters should be varied for the Monte Carlo runs. The chosen devices should be those that affect the design.

Once the parameters are identified, the designer must assign and/or verify the distributions for each parameter to be varied. These assignments usually can be done on the schematic or the models themselves. Verifying the distributions ensure that the designer is accurately reflecting real-world devices.

Next, a number of runs to simulate over are chosen, and simulation begins using known test vectors. Some simulation runs may have convergence problems in areas where others will not. Certain simulations may not run at all. While this situation is usually rare, on critical designs, the Monte Carlo simulation may have chosen device values that will cause a design problem or failure. When this occurs, it is typically a good indication that build problems may appear later in the design cycle.

Once the simulation runs are completed, the results files can be plotted against a known-good simulation run. From these graphs the designer can look for points where the outputs fall from the specification requirements, or regions where the outputs drop out altogether. The designer can choose one of these points and view the parameters that caused the problem. If the simulation tool has a sensitivity-analysis function, it can be used to find out which devices are going to affect a given output more than others.

At this point, the designer has identified which element needs to have its tolerance tightened, or whether a device needs to be replaced entirely. In rare cases the designer may need to redesign some circuitry. Consequently, using Monte Carlo analysis, the designer can obtain a valuable level of reassurance for predicting a design's operation in the customer's hands.

Contributed by Lee Hansen, analog product marketing engineer, VeriBest Inc., Boulder, Colo.

tire process is estimated to be anywhere from 20-to-50 times faster, using radiation specific Monte Carlo codes.

The Monte Carlo radiation-specific code of Peregrine is processed on an operating system that supports a symmetric-multiprocessing (SMP) architecture. In this manner, numerous computations can be performed in parallel. Since there is no particle interaction, each memory component can process a single particle. The results of each processed particle are then sent, in parallel, to a single collection point, where the data is brought together to form an accurate depiction of the required radiation dosage.

What began over three years ago as a laboratory-directed R&D program, now has become one of the facility's strategic initiatives. It is hoped that a proposal for commercial use of the technology will soon be presented to the U.S. Food And Drug Administration (FDA).

The Peregrine technology shows potential for implementation, not only because it promises greater dose calculation accuracy and is low in cost, but because it does not alter the established treatment-delivery mechanism. Rather, it significantly improves the ability to target tumors by tailoring precise radiation-dose calculations for each patient based on the patient's anatomy and disease, potentially leading to significantly higher cure rates. Basically, doctors will be able to treat patients with a higher dose of radiation, with the confidence that it will not affect the normal tissue structure, and that the patient will be able to tolerate the treatment.

While a clinical Peregrine technology-based product is still years away, Livermore hopes that it will one day become the standard for dose calculation in all clinical environments. One of the biggest misconceptions, though, in seeing this become a reality is that 10 million computers would be needed to make the technology work properly, and quickly enough for everyday use. To answer this concern, researchers are continuing to integrate faster and cheaper technology with advanced calculation tools. This endeavor will ensure that Peregrine technology finds its way into clinics at an affordable cost.

For additional information, contact the Public Affairs office of Lawrence Livermore Laboratory at (510) 422-1100.

Cheryl Ajluni

Vertically-Stacked Multichip Modules Promise Low-Cost Miniaturization Of Electronics In 3D

An innovative three-dimensional chip-stacking technique promises to allow the construction of low-cost high-density electronic assemblies to satisfy a variety of specialized electronic functions. Developed by Societe 3D+, Buc, France, the method employs MCM-V technology (the V stands for "vertical") to allow the integration of DRAM chips, portable telephones, and miniature cameras among other things.

After several years with the French electronics company Thomson CSF, 3D+'s founder Christian Val started 3D+ two years ago and began using the patented Thomson technology. MCM-V involves stacking layers of electronic circuitry to produce complete microsystems. The layers may contain identical or heterogeneous components such as sensors, micropumps, memory chips, and microprocessors.

Chips are mounted on flexible pc-board substrates, using a technique very similar to that used to produce "smart cards." Each device is fully tested before stacking.

Stacking of the chips is performed with an accuracy within 10 µm using a system of pre-drilled holes. The completed stack is then placed in an epoxy resin, hardening to form a block that is sightly larger than the size of the finished components. The faces of the block are then sawed at a distance of 0.2 to 0.4 mm from the edges of the largest chip, revealing the copper tracks on the printed-circuit substrates.

The blocks then undergo several metal deposition operations. First, nickel is deposited to improve surface adhesion. This is followed by a 5- to 7-µm deposition of copper, which in turn is protected by a layer of nickel, then a top layer of gold. Insulating corridors between the conductive strips are cut using a Yag laser. Any type of bare or encapsulated chip can be stacked.

The MCM-V method joins other popular multichip module (MCM) technologies like MCM-L (laminated devices), MCM-C (ceramic devices), and MCM-D (deposited devices) have been used for miniaturization. However, the latter three are 2D techniques.

A 32-Mbyte memory stack produced by the MCM-V method is smaller and lighter than an MCM-C component of the same capacity (a volume of 4075 versus 26,625 mm^3, a footprint of 214.5 versus 4053 mm^2, and a weight of 9.1 versus 64.5 g). While design and manufacturing costs are slightly higher than for surface-mount technology on a pc board, they're much lower than for a hybrid module.

3D+ has used the MCM-V technique to build a 256-Mbit memory consisting of a stack of sixteen IBM 16-Mbit DRAM chips in a volume of just 4.1 cm^3. The memory was built for the French telecommunications giant Alcatel Espace. For British Telecom, 3D+ built a microcamera with a total volume of just 1.5 cm^3 for video-capable portable telephones. The microcamera integrates a micro-sized lens, a 312-by-287-photodiode array, an image-processing module, and various data-storage chips. And 3D+ also is developing a computer module made up of a Texas Instruments C40 microprocessor and flash SRAM chips. New uses are being developed, including automated drug-delivery systems in medical applications.

This stacked-chip technology has attracted interest from two major worldwide research projects. One is the Barmint (basic research for microsystem integration) program under the European Esprit project. The other is the 10-year micromachine development project being funded by Japan's Ministry of International Trade and Industry (MITI).

For further information, contact Christian M. Val, Societe 3D+, 421 Rue Helene Boucher, 78532 Buc, France; telephone (33.1) 39 56 24 96; fax (33.1) 39 56 25 89.

Roger Allan

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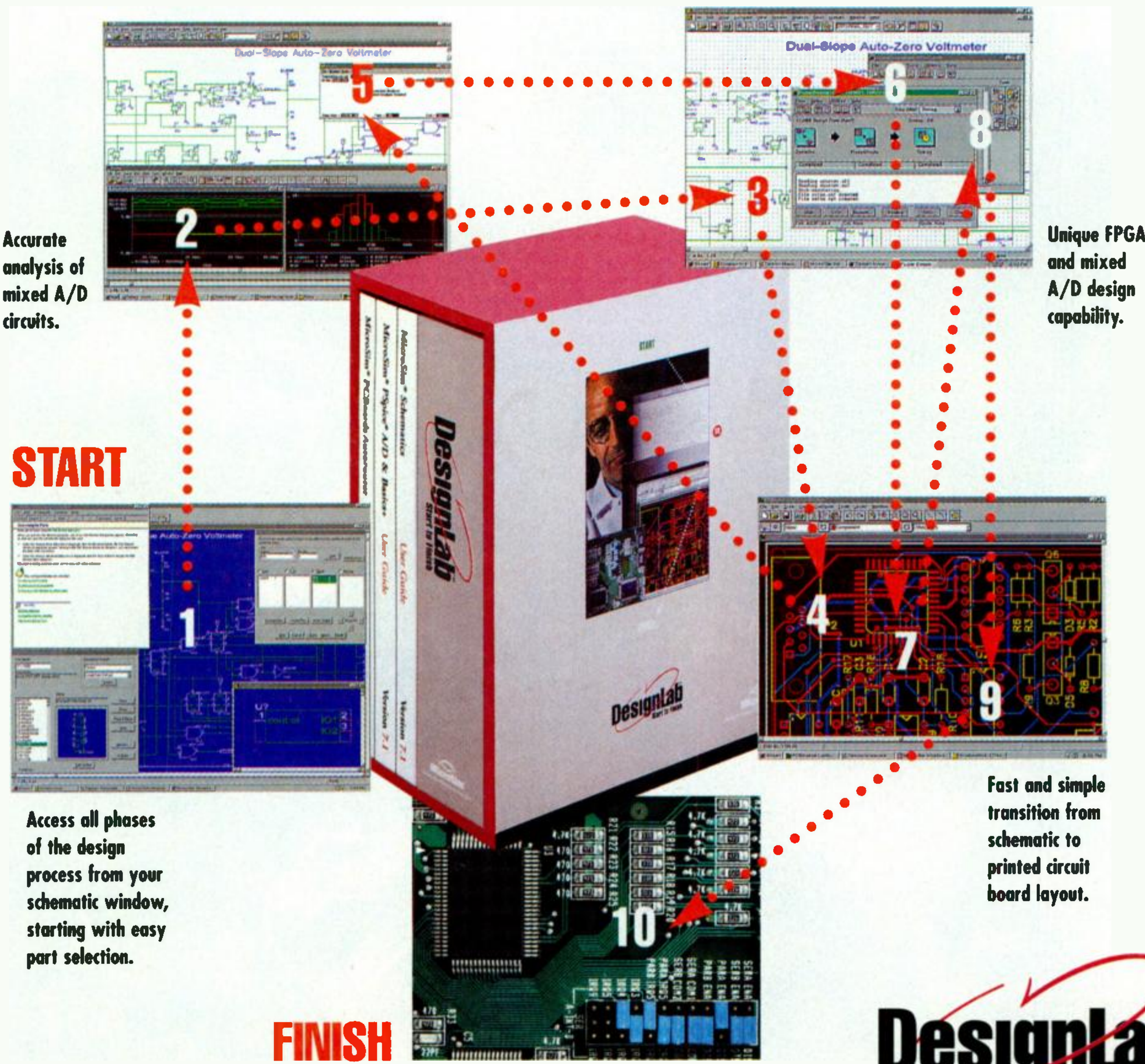

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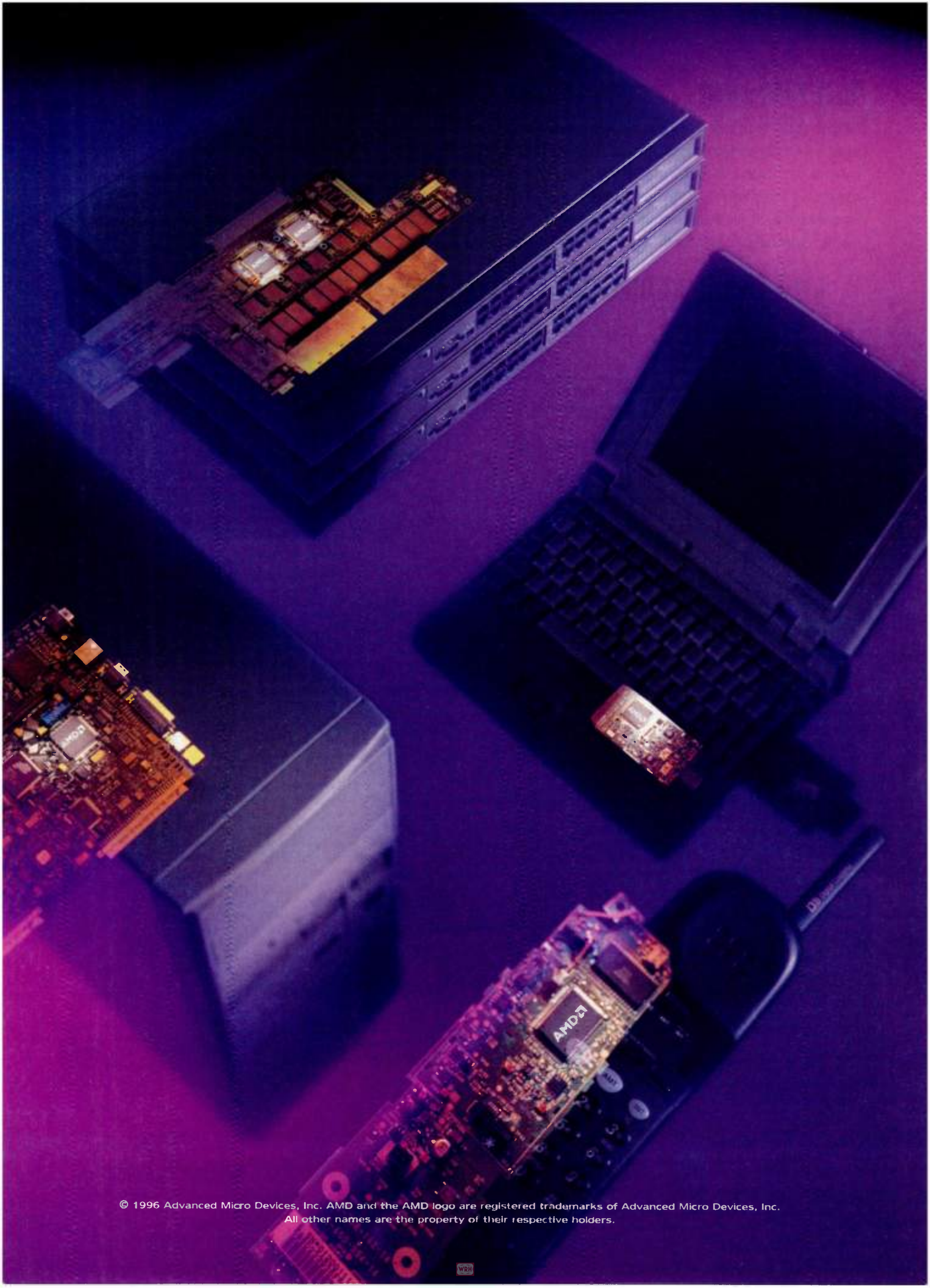
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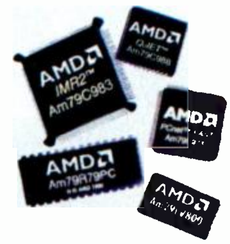
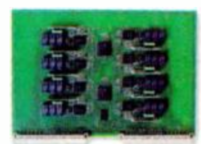


AMD communications silicon includes Ethernet controllers and repeaters, linecard ICs, programmable logic devices, flash and EPROM memory, and embedded processors.



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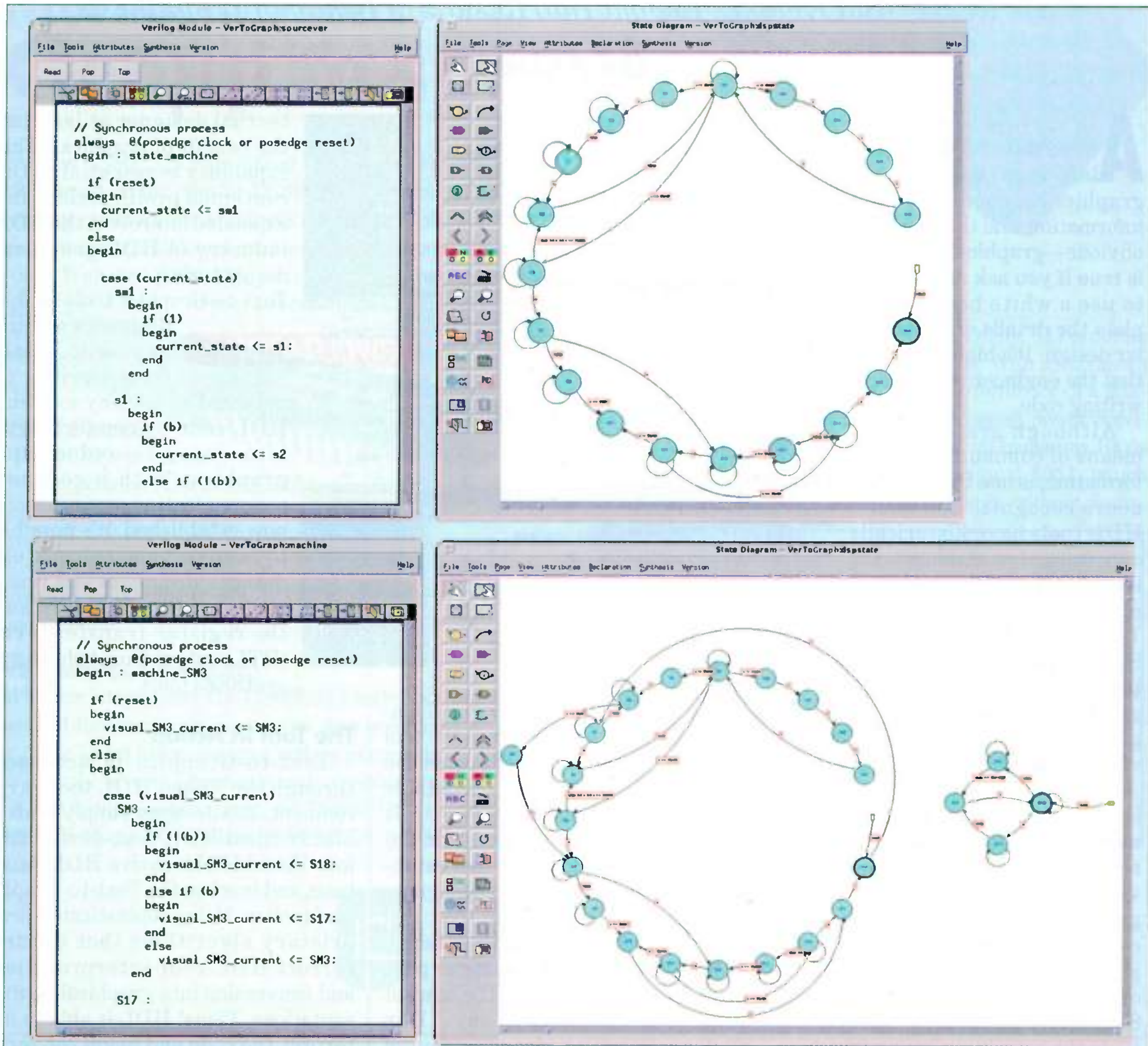
ing the input code to identify any structure. When the structure has been identified, Visual HDL then looks for any state machines, and subsequently, any algorithms that may be present in the code. Once these have all been found, they are broken down and recursively rebuilt using the design's hierarchy.

During the text-to-graphics conversion process, any code that cannot be translated is flagged for the user's attention. The rest of the code is converted as is to a graphical representation. The designer then has the option of leaving the unconverted code the way it is or rewriting it in a form that the tool can understand. The rewritten code can then be rerun and subsequently converted to graphics. While the tool currently supports HDL code from all the major synthesis vendors, additional support will be added.

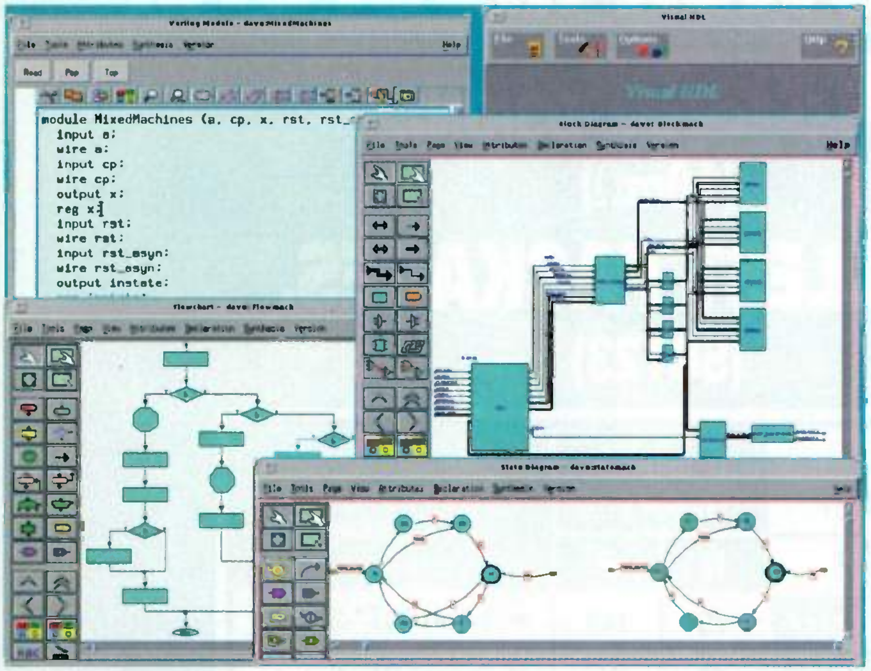
Once the text-to-graphics process is completed, the user can edit, modify, view, and print the converted text design just as if it were originally created using Visual HDL's graphical editors *(Fig. 2)*. The graphical specifications can even be used to regenerate optimized code. Additionally, during the text-to-graphics conversion process, Visual HDL retains all the documentation and comments included in the design source.

Tool Features

Of the many features offered by the Text-to-Graphics tool, the most important is its ability to allow preservation of legacy designs, and design reuse. With designs becoming ever more complex, it's almost impossible for the typical designer to start from scratch and reinvent the wheel. Rather, they are forced to reuse internal designs or buy pieces



1. Summit Design's Text-to-Graphics tool, accessed through the company's Visual HDL tool environment, generates IC or system graphics from existing Verilog or VHDL code. In doing so, it improves design-team communication, highlights design changes not apparent in the code, enables easy design reuse, and helps designers reclaim lost intellectual property.



2. The Text-to-Graphics tool, accessed through Visual HDL, allows designers to write in code and still leverage the benefits of graphics. Once the text has been to converted to graphics, it can be manipulated as if it were just created to provide, for example, a more effective design flow for behavioral synthesis or RTL optimization.

of intellectual property from other companies. While this sounds easy enough, the difficulty boils down to one thing—documentation. And many would agree that while it certainly is one of the more essential pieces of a good design, designers at every level avoid it like the plague.

There are a number of reasons why documentation has gotten such a bad rap in the past. Consider the fact that most designers today don't stay on the same project long enough to see it completed. So, for the average designer who is already under great pressure to crank out a quality design at lightning speed, there is no real motivation in taking the time to document a design. And, even if the design is documented, there are no guidelines in place to dictate how it should be done. This dilemma means that the quality of the documentation can, and does, differ according to the designer. In many cases, if the documentation is done after the design has been completed, it may not even match the code.

The result of this documentation quagmire is a loss of design legacy. In the end, many designers end up either rewriting a design from scratch, or investing huge amounts of time pouring over the existing code trying to understand the original designer's intent. This effort doesn't always work, though, because many designers don't have the time to choose either option.

The Text-to-Graphics tool eliminates all of these concerns by providing automated documentation, and reuse of manually-written code. By capturing the designer's intent by means of a universal graphical representation, the design can be reused by designers other than the original creator. And, because the graphical specification is closely linked to the HDL code, the designer can make changes to the code and use the tool to automatically update the corresponding graphics.

For large companies or design teams that want to leverage existing, poorly-documented HDL code, Text-to-Graphics gives designers a way to understand the design intent of existing text files so that they can be enhanced in future designs. For expert coders, it provides an automated process for graphically documenting their manually-written HDL text. And, for engineering management, work done by a designer on a project, such as any engineering changes, can be quickly deciphered, allowing the higher-ups to sign-off on the design with a complete understanding of what it's all about.

> **Most designers today don't stay on the same project long enough to see it completed.**

While graphical documentation improves the designer's ability to understand and reuse designs in subsequent projects, it also provides design security. It ensures that the design is preserved for later reuse in an easily recognizable format, even if the original designer is long gone from the company.

The Text-to-Graphics tool also allows for simple and fast debugging. By today's conventional means, debugging can often be quite difficult, requiring the designer to look at the source code or documentation, to find any changes made to the design. The problem is that once the designer invests the time examining the code and documentation, there's no guarantee the bug will ever be located. With a graphical representation of the design, on the other hand, most bugs, along with any design changes, can be spotted quickly. In addition, the tool also can be used to quickly implement engineering change orders (ECOs).

One of the unique features of Summit's Text-to-Graphics graphical debug capabilities is its close link between simulation of the HDL code and the associated graphics. Implied in this link is a cause and effect relationship between the HDL code and the graphics. Consequently, as opposed to having to simulate the HDL code within a design and then examine the source code line-by-line, debuging can be accomplished in a completely graphical environment. The designer simply views the HDL code in its graphical format for any bugs, and once these are located, all changes can be made graphically. The associated HDL code is auto-

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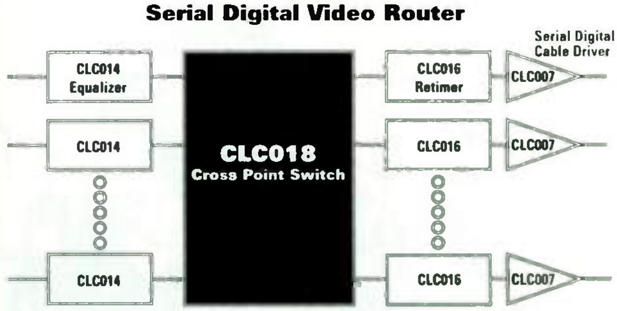

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matically updated.

The Text-to-Graphics tool also provides insight into the results of the post-synthesis analysis of behavioral synthesis. Today, behavioral synthesis is still an emerging technology. Its widespread use and acceptance has been hampered by the inability of designers to adequately figure out the output of a behavioral synthesizer, and how to interpret it. In effect, it's a black box, and the only way to really understand it is to simulate the code.

Text-to-Graphics aims to take some of the mystery out the technology by providing insight into the optimized RTL-code output from a behavioral-synthesis tool. It accomplishes this by converting the black box RTL code into graphical representations. Designers can then examine the synthesis tool's effect on control and data flow logic. And, by analyzing the behavioral-synthesis output data, designers can adjust their behavioral source code to improve synthesis results, or simply edit the design graphically in Visual HDL to make the necessary design improvements.

While today the Text-to-Graphics capability can work well with behavioral synthesizers, the real issue is integration. Behavioral synthesizers, therefore need to output RTL that can be read and converted by the Text-to-Graphics tool. And, in turn, the Text-to-Graphics tool must be capable of reading and converting the behavioral synthesizers' style of code. By doing so, Summit believes that Text-to-Graphics will have a major effect on the adoption rate of behavioral synthesis.

Price And Availability

The Text-to-Graphics add-on option to the Visual HDL tool is currently in beta test and will be available for both PCs and workstations. Pricing is set at $10,000. The Verilog Text-to-Graphics option will be available soon, while the VHDL version will be available later in the summer.

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Conference Shows The Lighter (And Low Power) Side Of Products

Portable By Design Conference And Exhibition Gives Designers A Path Toward Portable-Related Components.

Richard Nass

You've just been assigned the task of designing a portable system. That shouldn't be a problem—you've been designing desktop systems for years. Think again! There are many aspects of a portable design that differ from their stationary counterparts. To get your questions answered and to find some of the products that are built just for portable applications, check out the Portable By Design Conference and Exhibition, to be held at the Santa Clara Convention Center, Santa Clara, Calif., Mar. 25-27 *(see "Want To Go?" p.56)*.

In addition to being exposed to some of the latest portable-related products, there will be some special events taking place, such as presentations by Jack Kilby, inventor of the integrated circuit, and Bob Pease, renowned analog engineer and columnist for *Electronic Design*. The keynote luncheon also will feature four individuals who will offer their views on the future of the portable industry: Tom Beaver, Vice-President of Worldwide Marketing, Motorola Inc.; Philip Wennblom, Director of Strategic Planning, Mobile and Handheld Products Group, Intel Corp.; Robin Saxby, President and CEO, Advanced RISC Machines (ARM); and Vaughn Watts, Director of Mobile Computing Architecture, Texas Instruments *(see "Portable By Design: Special Events," p. 50)*.

Over 80 portable-product manufacturers will display their wares at Portable By Design. Products include microprocessors, chip sets, memory chips and cards, batteries, thermal-management devices, transceivers, voltage regulators, and input devices.

With the unveiling of the Windows CE operating system, which is geared toward low-power, portable systems, the VR4101 microprocessor becomes an attractive CPU choice. Developed by NEC Electronics Inc., Santa Clara, Calif., the 64-bit RISC processor features 33 VAX MIPS performance and 132 MIPS/W at 3.3 V, as well as DMA capability. A high-speed multiply-and-accumulate (MAC) feature enables the chip to run DSP-like instructions. As a result, the chip can replace external hardware by running some of the required functions in software.

The NEC device also integrates many of the functions required by a handheld platform. These include a modem and interfaces to an LCD, audio, a keyboard, and an infrared (IR) port. With a power consumption of 250 mW at 33 MHz, the VR4101 contains several power-savings modes. In standby, with the pipeline frozen, the part consumes 30 mW, while the suspend mode, which shuts down the pipeline and bus clocks, requires 10 mW. Hibernate mode freezes the internal phase-locked loop and requires just 240 W.

CSEM IC Design, Neuchâtel, Switzerland, will show its CoolRISC family of microcontrollers. The chips are designed from the get-go for low power dissipation. This comes from the use of gated-clock techniques and low-voltage cell libraries. The architecture allows for the execution of all instructions, including branch instructions, in just one clock cycle. The result is a performance level of 12 MIPS while consuming just 2.4 mW at 3.3 V. Other features include support for hierarchical memories, variable frequency modes, and multicontroller operation.

Connecting The Bridges

A series of chips that connect to the microprocessor help form a complete system, including the bus interfaces, real-time clock, I/O ports, and docking connections. The chip set, called the Mobile System Solution, hails from National Semiconductor Corp., Santa Clara, Calif. The chip set consists of the PC87550 PCI system controller (North Bridge), the PC87560 system I/O controller (South Bridge), and the PC87570 keyboard and power-management controller. The parts also can connect to the company's previously-announced PT80C525 PCI-to-PCI bridge chip.

The North Bridge part is designed to work with Pentium-class processors. It

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Fault	Conditions	Response Time
+5V over Voltage	$V_5 > 5.75$	490nS max
+5 under Voltage	$V_5 < 4.25$	
+3.3V over Voltage	$V_{3.3} > 4.1$	490nS max
+3.3V under Voltage	$V_{3.3} < 2.5$	
+3.3 > +5V Supply Reversal	$V_{3.3} > V_5 + 300mV$	90nS max
Reset Recovery	All Supplies in Tolerance	100mS typ

All Conditions Meet or Exceed Requirements of PCI Specifications Revision 2.1

Until now, there were two ways of dealing with power integrity on PCI-based systems. You monitored the power supply using a highly complex, board-gobbling set of components. Or, you simply crossed your fingers and hoped it wouldn't be a problem.

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Because the chip is self-contained, the LMC6953 saves you a bundle in both time and money when designing and building this critical PCI bus component. And with virtually no external connections required, you get the boardspace you need to keep your design clean and efficient.

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supplies a CPU-to-PCI-bus interface, secondary cache and DRAM control, and active and passive power-management modes. It also supports hot, warm, and cold docking. The South Bridge provides PCI bus mastering for the chip's two Enhanced IDE channels, a USB host controller, and a 4-Mbit/s infrared controller. Lastly, the PC87570 can replace up to five chips. Based on an embedded RISC processor core, the chip handles power management and keyboard and system control. It also supplies analog-to-digital and digital-to-analog conversion.

A pair of 3-V pen-input processors deliver the low current consumption required for battery-powered handwriting recognition and verification products. Designed by TriTech Microelectronics International Inc., San Jose, Calif., the TR88L803 and TR88L804 can detect when pen input has stopped, then automatically places the system into a sleep mode until pen input resumes. The difference between the two ICs lies in their interfacing options—the TR88L803 offers a serial interface, while the TR88L804 comes with an 8-bit parallel interface.

The two parts contain all the circuitry needed to interface with the low-cost resistive digitizers employed in PDAs, electronic organizers, and feature phones. Using a 10-bit analog-to-digital converter (ADC), the TR88L803/L804 can resolve up to 1024 voltage levels, resulting in better than 200 dots/in. resolution on a 3- by 5-in. touch pad. Two additional ADC input channels are available under a multiplex mode to allow portable products to include such features as a battery gauge and handwriting pressure sensing. Positional transfer rates of 200 coordinate pairs/s are typical using a 1.8432-MHz crystal. A higher-frequency crystal increases the transfer rates.

On a subsystem level, the Cardio-486D4, which is a credit-card-sized PC-AT, now supports Windows NT 4.0. Designers taking advantage of the Cardio-486D4, developed by S-MOS Systems Inc., San Jose, Calif., can realize a savings in resources, development costs, and time to market. The embedded version of Windows NT 4.0 is offered by VenturCom Inc., Cambridge, Mass. The memory requirement for the operating system is 8 Mbytes, while the Cardio-486D4 can hold up to 16 Mbytes.

The SMX/386, designed by ZF MicroSystems Inc., Palo Alto, Calif., is a 2.2- by 3-in. module that combines standard motherboard functions in a 240-pin package. The device contains a 33-MHz 386SX microprocessor, core logic, a DRAM controller, an 8- or 16-bit ISA bus, serial and parallel ports, floppy- and hard-disk controllers, and 256 kbytes of flash memory. It also holds an AT-compatible BIOS and an embedded version of DOS.

One of the ways designers are implementing an embedded operating system or BIOS is with flash memory. Nexcom Technology Inc., Sunnyvale, Calif., offers a pair of high-density serial flash memories. Employing the standard 4-pin serial peripheral interface (SPI), the NX25F040 and NX25F080 memories hold 4 and 8 Mbytes, respectively. Based on the company's NexFlash technology, the chips are suited for such applications as digital cameras, voice and data pagers, voice recorders, and handheld terminals and data loggers.

Operating at either 3.3 or 5 V, the NX25F040 and NX25F080 are built with 536-byte sectors that program quickly, thereby maximizing battery life. Data can be transferred to and from the devices at 20 MHz. Typical program times are 2.5 ms/sector, allowing for sustained programming rates of over 200 kbytes/s, including erase time. Other features include byte-level addressing, double-buffered sector writes, auto-erase before write, and an advanced write protection.

The Miniature Card Implementers Forum, Folsom, Calif., will be displaying a host of products from its member companies. These products include storage devices that fit various consumer electronics products such as a digital camera, an audio voice recorder, and a handheld computer. The Miniature Card is a PC-compatible digital media that stores data in nonvolatile removable memory. The cards measure 38 by 33 by 3.5 mm and can hold up to 64 Mbytes.

The Miniature Card specification calls for both 3.3- and 5-V voltage levels, with lower voltages expected in future revisions. The specification is a subset of the standard PC Card interface. As a result, transfers from a Miniature Card to a PC can be made with a low-cost Type II PC Card adapter. In addition, the Universal Serial Bus (USB) provides a means of transferring data to and from a card.

A similar form-factor product comes from Duel Systems, San Jose, Calif. The company offers a sonically-welded CompactFlash card package. Manufactured from insert-molded stainless steel and plastic, the rugged

Portable By Design: Special Events

For the first time, attendees will have an opportunity to mix and mingle with the manufacturers and suppliers of portable products on the exhibit floor during the Industry Reception, which takes place on Tuesday, Mar. 25, from 5:00 p.m. to 8:00 p.m. The casual atmosphere will provide a great forum for attendees to glean the information they need.

An added highlight to this year's Industry Reception: Jack Kilby, inventor of the integrated circuit, will present the First Annual *Electronic Design* Award For Technical Innovation. This award will be given to the author of Portable By Design's "Best Paper."

Simon Ellis of Intel Corp. also will make a presentation at the Industry Reception. He'll unveil his "Portable Videoconferencing Center" which will give attendees a peak at the future of one of the more anticipated technologies.

On Wednesday, Mar. 26, at 11:00 a.m., Bob Pease, renowned analog engineer and author of *Electronic Design's* "Pease Porridge" column, will enlighten attendees with a unique presentation that only he can give. He'll come back at 1:00 p.m. on the same day to talk to the attendees and autograph copies of his *Electronic Design* Compendium of Pease Porridge columns.

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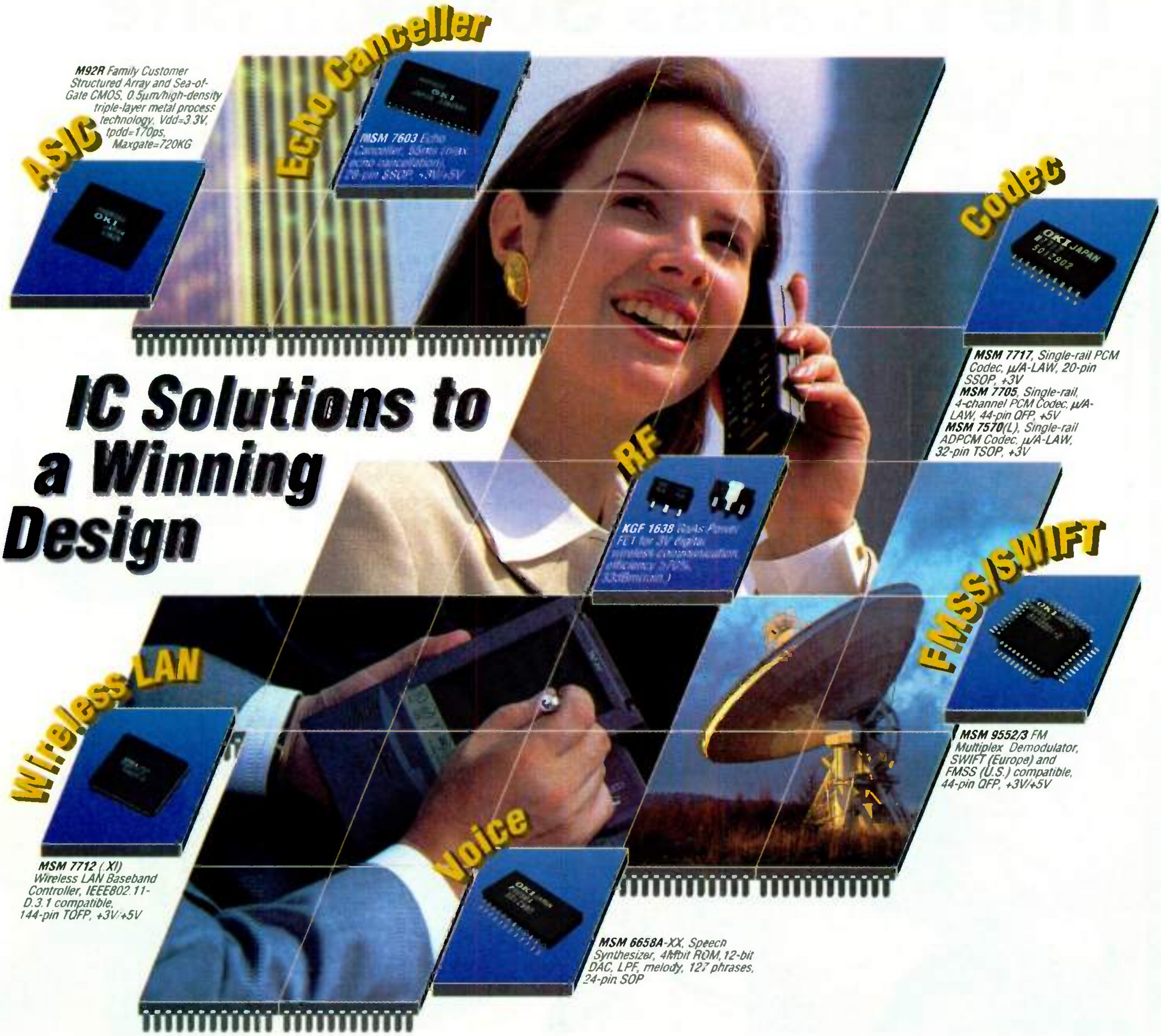
For the first time, attendees will have an opportunity to mix and mingle with the manufacturers and suppliers of portable products on the exhibit floor during the Industry Reception, which takes place on Tuesday, Mar. 25, from 5:00 p.m. to 8:00 p.m. The casual atmosphere will provide a great forum for attendees to glean the information they need.

An added highlight to this year's Industry Reception: Jack Kilby, inventor of the integrated circuit, will present the First Annual *Electronic Design* Award For Technical Innovation. This award will be given to the author of Portable By Design's "Best Paper."

Simon Ellis of Intel Corp. also will make a presentation at the Industry Reception. He'll unveil his "Portable Videoconferencing Center" which will give attendees a peak at the future of one of the more anticipated technologies.

On Wednesday, Mar. 26, at 11:00 a.m., Bob Pease, renowned analog engineer and author of *Electronic Design's* "Pease Porridge" column, will enlighten attendees with a unique presentation that only he can give. He'll come back at 1:00 p.m. on the same day to talk to the attendees and autograph copies of his *Electronic Design* Compendium of Pease Porridge columns.

MICROPROCESSORS/PERIPHERALS MICROCONTROLLERS TELECOM LSIs VOICE SYNTHESIS LSIs VF DRIVERS/CONTROLLERS LCD DRIVERS/CONTROLLERS ASICs MEMORIES



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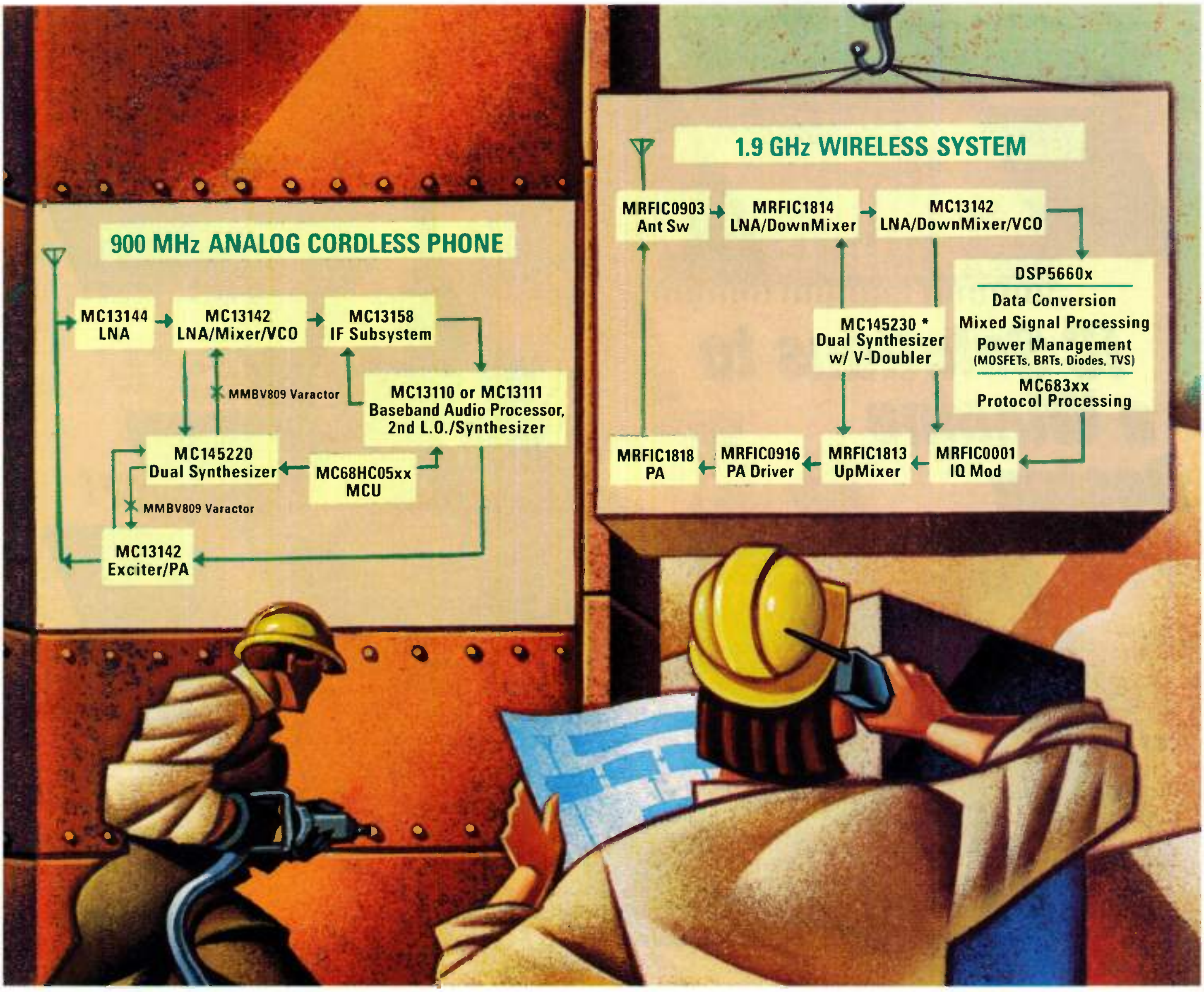
MEMORY MODULES MEMORY CARDS MODEM CARDS GaAs DEVICES OPTOELECTRONIC DEVICES OPTICAL MOS RELAYS FIBER OPTIC PRODUCTS LED PRINT HEADS REED RELAY/REED SWITCHES

The Wireless Solution Site



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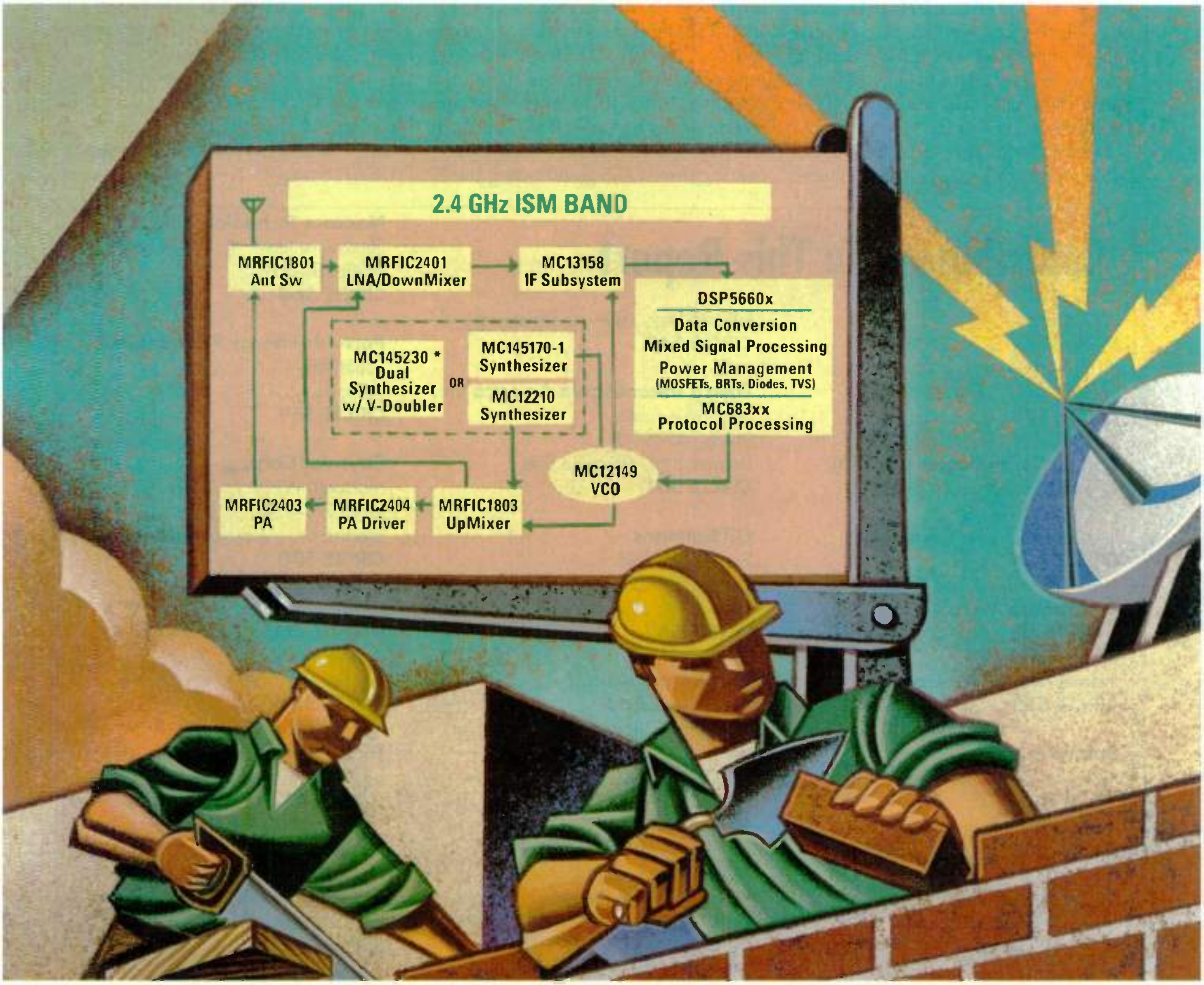
2.4 GHz ISM BAND
MRFIC1801 Ant Sw
MRFIC2401 LNA/DownMixer
MC13158 IF Subsystem
DSP5660x
Data Conversion
Mixed Signal Processing
Power Management
(MOSFETs, BRTs, Diodes, TVS)
MC683xx
Protocol Processing
MC145230 * Dual Synthesizer w/ V-Doubler
OR
MC145170-1 Synthesizer
MC12210 Synthesizer
MC12149 VCO
MRFIC2403 PA
MRFIC2404 PA Driver
MRFIC1803 UpMixer

packages give designers the maximum real estate, and clean and rapid assembly. Before being welded, the package can be snapped together for testing purposes. Duel Systems also offers a line of PC Card packages, with a Type III card coming shortly.

One of the limiting factors of a notebook computer's size is its keyboard. That limit will shrink thanks to the FKB7600 series of keyboards from Fujitsu Takamisawa America Inc., Sunnyvale, Calif. *(Fig. 1)*. Despite the keyboard's vertical height of 6.5 mm, it retains a 3-mm, full-travel keystroke by employing a gear-link mechanism in the keyswitch. Combined with an operating force of 55 g and a 20-g tactile force, the FKB7600 keyboard gives the user the needed key feedback. The 85-key model weighs 120 g and measures 287 by 109 mm.

Using a single IC, an operating system and BIOS can control any SMBus-compatible device that's connected to the IC's SMBus port. Developed by USAR Systems, New IC, an operating

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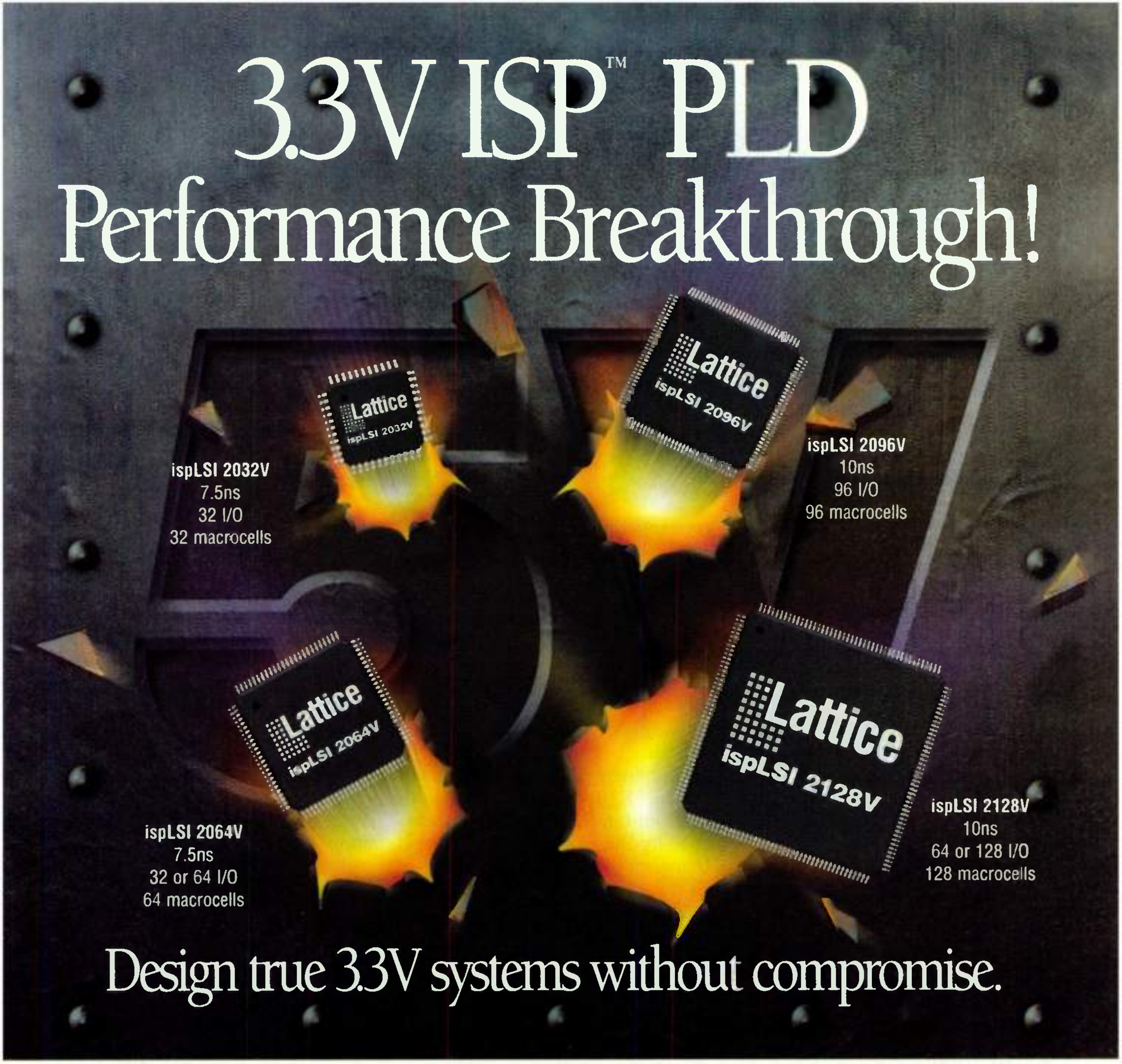

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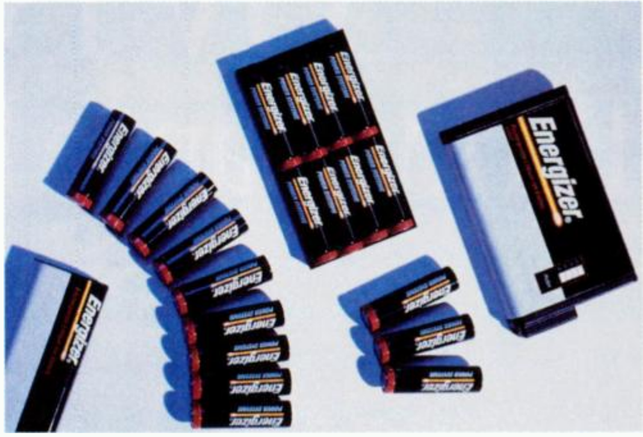
WRH

READER SERVICE 135

2. With a typical service life of 500 cycles, the GP10AAAM 1/3AAA NiMH battery offers a nominal capacity of 100 mAh.



3. The ELI-18650 rechargeable Lithium-Ion battery offers a high energy density—1350 mAh in an 18- by 65-mm cell.

system and BIOS can control any SMBus-compatible device that's connected to the IC's SMBus port. Developed by USAR Systems, New York, N.Y., the UR5HCSMB BatteryCoder achieves its SMBus implementation through a set of PS/2 protocol extensions. Through these extensions, commands can be sent from the host through the 8042 port to the BatteryCoder. The subsequently sends the commands to the appropriate SMBus device. These devices include smart batteries and chargers, digital potentiometers, EEPROMs, port expanders, temperature sensors, and power-plane controls.

Powering The System

One of the most essential components of a portable system is its batteries. As one would expect, there'll be no shortage of batteries at Portable By Design. For example, GP Batteries, San Diego, Calif., has developed a 1/3AAA NiMH battery with a nominal capacity of 100 mAh. The GP10AAAM has a diameter of 10.25 mm, a height of 13.7 mm, and a weight of 5 g *(Fig. 2)*. The recommended discharge current limits are from 10 to 300 mA with a typical service life of 500 cycles.

A second offering from GP Batteries is the GP80AAAH, which fits the 7/5 form factor. With a capacity of 800 mAh and a AAA diameter (10.5 mm), the NiMH battery is a candidate to replace prismatic batteries. In a cellular telephone, the expected talk time is 140 min., with a standby time of 22 hours.

Battery Technologies Inc. (BTI), Ontario, Canada, has developed a rechargeable alkaline manganese (RAM) battery available in AA, AAA, C, and D sizes. In addition to selling the batteries themselves, BTI will sell licenses and production equipment for third parties to build and sell the RAM batteries. According to the company, the batteries will hold a charge for up to five years and won't exhibit any memory effect, regardless of the usage pattern.

High energy density is the hallmark of the ELI-18650 rechargeable Lithium-Ion (Li-Ion) battery, developed by Energizer Power Systems, Gainesville, Fla. *(Fig. 3)*. The 18- by 65-mm cell produces 3.6 V and 1350 mAh. Suitable applications include portable computers, cellular telephones, camcorders, and other handheld electronic devices. The battery contains a graphitic carbon anode and lithium-cobalt-oxide cathode in an organic electrolyte. Intelligent charging and fuel-gauge options are available. Because Li-Ion batteries require a specific charging technique for proper charging, Energizer will offer comprehensive technical and design support.

Portable Energy Products Inc., Scotts Valley, Calif., has developed an auxiliary battery pack that can power a notebook computer or a camcorder for up to 10 hours or a cellular telephone for a week. The battery is rated at 12 V and 5 A (60 Wh).

The LifeX BR1632DK2 computer back-up battery for notebook computers is available from Rayovac Corp., Madison, Wis. The lithium coin cell offers a 130-mAh rating and can withstand rigorous thermal environments. Also from Rayovac is a charge-discharge controller, which lets designers test, measure, and evaluate the performance of the company's Renewal Rechargeable Alkaline batteries in their own devices. Co-developed with Benchmarq Microelectronics Inc., Dallas, Texas, the bq2902 and bq2903 work with up to two or four cells, respectively. The chips combine sensitive full-charge detection with a low-battery cutoff to provide overcharge protection. By maintaining proper charging characteristics, battery life can be pro-

Want To Go?

The Portable By Design Conference and Exhibition will be held at the Santa Clara Convention Center, Santa Clara, Calif. The technical sessions run Mar. 25-27, while the workshops take place Mar. 24. The exhibition area is open Mar. 25-27. The keynote address and luncheon, featuring speakers from Advanced RISC Machines (ARM), Intel, Motorola, and Texas Instruments, will take place on Mar. 25 at 12:00 noon. For more information, contact Betsy Tapp at (201) 393-6075, or send an e-mail to portable@class.org.

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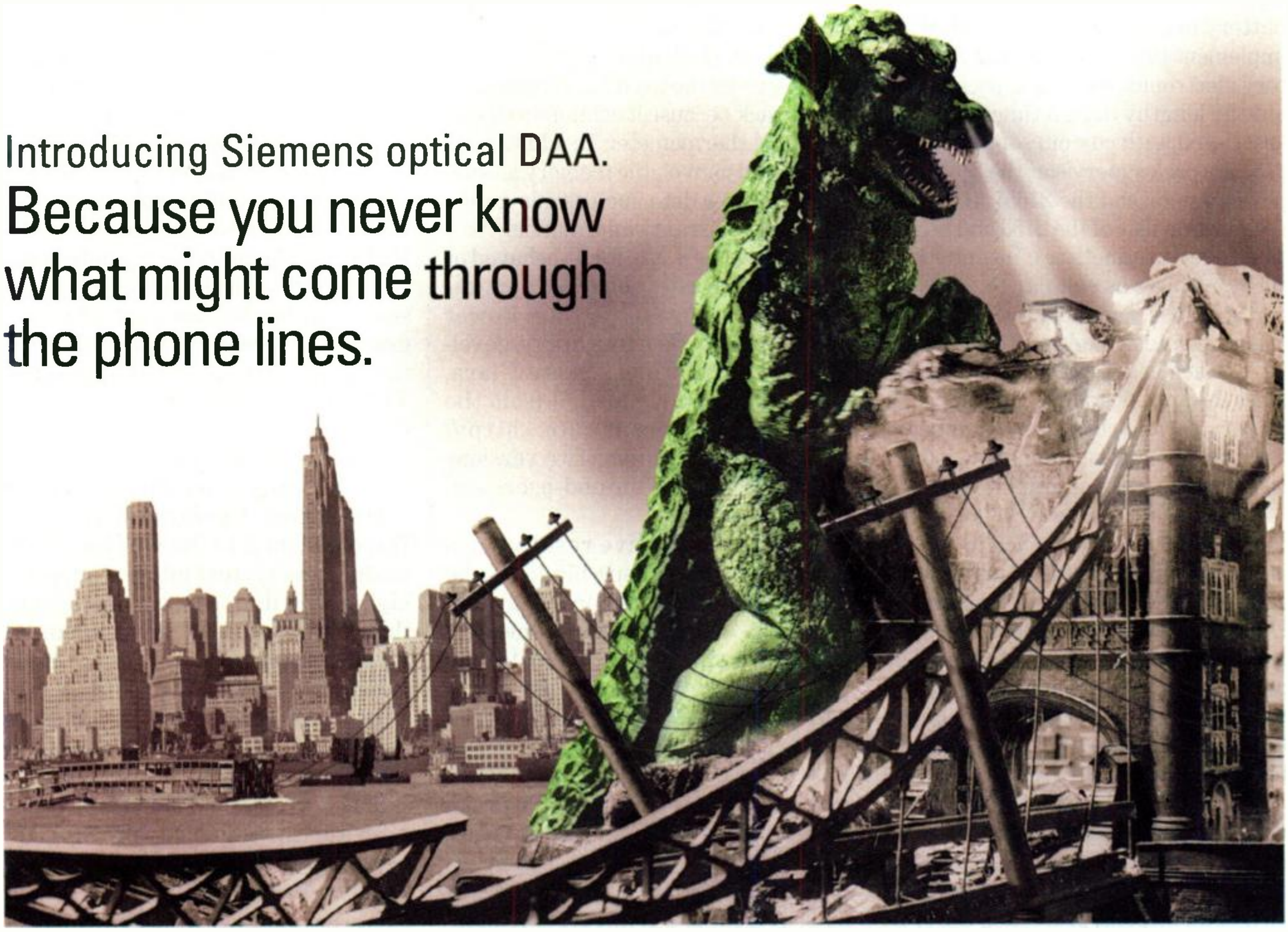

Features	DAA2000	DAA2100
10 Hz—4KHz Bandwidth	✓	✓
Transhybrid	✓	✓
Integrated Ring Detect	✓	✓
Hook Switch Control	✓	✓
Caller ID	✓	
Snoop Mode	✓	
Line Sense	✓	
Voltage/Frequency Converter	✓	✓
Power Mgmt.	✓	✓
Wake on Ring	✓	✓
Thermal Protection	✓	✓

The opto solution that shrinks interface/isolation problems.

Today's increasing modem speeds and decreasing device sizes can make the traditional transformer and circuitry solution seem like an unwieldy monster. Now the leader in optocoupler technology breaks through the transformer barrier with the new DAA2000 and DAA2100.

Smaller size. Giant capability.

The Siemens DAA2000 is ideal for applications in PC modem cards with multimedia capabilities and extremely tight real estate requirements. The DAA2100 is the lower-cost solution for internal and stand-alone modems where space is not an issue. The DAA2000 utilizes two 24-pin TSSOPs, while the 2100 uses two 24-pin SOICs. And both kits include two 8-pin Slimline IL388 linear optocouplers, with specifications to easily assemble the DAA function directly onto the mother board.

Special features tame distortion and power management.

The DAA2000 and DAA2100 are all-analog solutions, operating down to 2.7 V on the modem side, with distortion numbers flat across the whole band. And both include built-in ring detect and hook-switch control. In addition, the DAA2000 offers extra features such as snoop mode and built-in overcurrent/thermal limiting.

So whether you have a tight space or a tight budget, with Siemens DAA2000 and DAA2100 you'll find a perfect fit.

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longed.

Benchmarq also offers a series of products to monitor and supervise up to four Li-Ion cells. The bq2153, bq2150L, and bq2165L modules enable battery makers and system OEMs to implement protection circuits and battery electronics for Li-Ion packs without the lengthy design times typically associated with custom solutions. The 2153 is a pack supervisor; the 2150L is a power gauge; and the 2165L combines the functionality of the 2153 and 2150L. The three products are intended for such products as cellular telephones, portable PCs, handheld terminals, and other wireless communications devices. Each board can be configured to meet the specification of the particular battery pack, including the number of cells, the nominal pack capacity, and the battery type (coke or graphite anode).

The on-chip series FET built into the UCC3911 battery-pack protector helps to reduce manufacturing costs and increases reliability. Designed by Unitrode Corp., Merrimack, N.H., the chip works with Li-Ion batteries. The part safeguards applications against battery-output short circuits and protects both Li-Ion cells in two-cell packs from overcharge and over-discharge.

The UCC3911 employs a bandgap voltage reference that detects when either cell is in an overcharged or over-discharged state. The series FET switch then opens, protecting the cells. A negative feedback loop controls the FET switch when the battery pack is in either the overcharged or over-discharged state and allows for pack recovery. In the overcharged state, the feedback loop only allows discharge current to pass through the FET switch, while in the over-discharged state, only charging current is allowed to flow. In addition, the chip enters a sleep mode in the over-discharged state until it senses the pack is being discharged.

A series of battery-management products from Dallas Semiconductor Corp., Dallas, Texas, can be placed into two categories—battery chargers and battery instrumentation and identification. The DS1333 charger works with Li, NiCd, NiMH, and lead-acid batteries. The part is programmed to attain any current-vs.-voltage curve the designer requires and uses either Vmax or an on-chip timer to determine charge termination.

The DS2434, which falls into the Dallas Semiconductor's battery instrumentation and identification category, features an ID code that users can define so that the supporting electronics can identify the battery pack. The chip also removes the need for a thermistor in the pack because it contains a direct-to-digital thermometer. In addition, an integrated nonvolatile memory lets designers enter data such as gas-gauge levels and warranty information.

There's now a cure for ill-behaved or power-unfriendly software applications and drivers—the Intel Power Monitor (IPM). The free utility, developed by Intel Corp., Santa Clara, Calif., can be downloaded from the company's Internet site: http://www.intel.com/ial/ipm. Two versions are available, one for end-users and one for developers.

A second initiative resulted in a power-management specification—the Advanced Configuration and Power Interface (ACPI). When implemented, the ACPI allows a PC to instantly power up when accessed by the user or perform automated tasks when turned off. In other words, the ACPI enables PCs to enter a "sleep" state, rather than off. The specification, which can also be downloaded from the Internet at http://www.teleport.com/~acpi/., is fully compatible with existing power-management and configuration interfaces, while providing a processor- and operating-system-independent implementation.

In a typical portable design, board space is at a premium. The MultiGuard Series of four-element transient voltage suppressors (TVS), developed by AVX Corp., Myrtle Beach, S.C., can help save some of that valuable space. According to the company, the device consumes less than 10% of the board area required in an alternative solution. The part's multilayer construction provides protection from voltage transients caused by ESD, lightning, and inductive switching. The TVS arrays can be used on any electronic printed-circuit board that contains multiple chips of the same voltage (energy) rating. The most frequent use for such a device is the I/O data lines in a portable computer or the RF amplifier in a cellular telephone.

One of the keys to a portable computer is its ability to communicate with other platforms. To facilitate this process, Temic Semiconductors, Santa Clara, Calif., has developed an IrDA-compatible transceiver that offers a transmission rate up to 4 Mbits/s. Housed in a top-view, surface-mount epoxy resin package, TFDT6000 measures just 13 by 7.5 by 5.65 mm. Integrated components include the diodes, emitter, and analog circuitry needed for a complete IrDA implementation. The TFDT6000 is aimed at designers that can't accommodate a side-view transceiver because of board-layout issues or packaging limitations. By integrating the receiver's preamplifier and the transmitter's driver stage, the TFDT6000 combines the functions of two ICs.

A second wireless communications product comes from Lucent Technologies, Murray Hill, N.J. The WaveModem 2.4-GHz wireless LAN module lets system integrators offer high-speed data communications to their platforms. The device is suited for such applications as factory-floor monitoring, mobile point-of-sale terminals, scanning systems, bar-code readers, or notebook and handheld computers.

The WaveModem module incorporates Direct Sequence Spread Spectrum (DSSS) technology to provide reliable high-speed transmissions. The device incorporates a dual-antenna design to improve signal quality. Modem connections to the host platform are made using the WaveModem Modem Interface.

A standard solution for various telecommunications and portable electronics devices comes from the 70AD male and female modular battery contacts. The contacts, designed by Bourns Inc., Riverside, Calif., are available in two- to six-pin configurations, with surface-mount or through-hole mounting. High-temperature molded plastic maintains the 70AD's integrity for surface mounting, while captured contact springs prevent contact from being inadvertently damaged.

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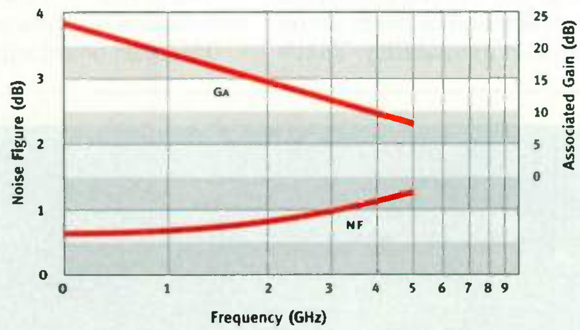

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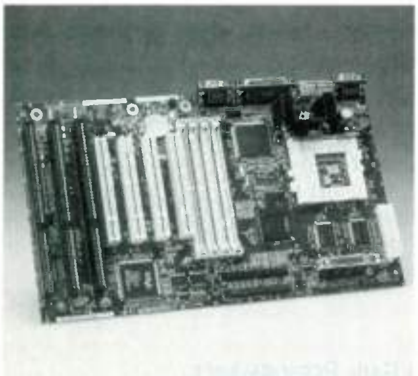
PRODUCT FEATURES

Pentium-Based Single-Board Computer Promises Long-Time Product Availability

One of the key attributes of the Marl baseboard is that it will be around for a long time. That sounds peculiar, but unlike the desktop-computer market, in which product life maybe only one or two years,



system integrators in the embedded market often demand as much as ten years of product availability. That's what RadiSys is pledging for its Marl board, which is a Pentium-based product that's built with a PCI local-bus interface. The baseboard is 100% mechanically, electrically, and BIOS compatible with Intel's Advanced/ML ATX board. As a result, designers can migrate to the Marl board and stay with the product for a long time.

In addition to the board's long-term hardware commitment, software maintenance also is reduced by the long life because the same code can be employed over a long period of time. Standard gold-plated connectors and headers are employed on the Marl board to help ensure long-term reliability. Targeted embedded applications include medical devices, telecommunications, and automation equipment.

The Marl board supports Pentium microprocessors running at speeds up to 200 MHz. It also can be purchased without a microprocessor. The board holds a 256-kbyte secondary cache memory and has four SIMM sockets to support various memory configurations. Connectors are available for parallel, serial, mouse, and keyboard ports, as well as power and hard- and floppy-disk drives. The board also contains three or four PCI slots and two or three ISA slots. Its AMI BIOS comes in a boot-block flash-memory chip that supports such features as IDE configuration, PCI autoconfiguration, ISA plug-and-play, multiple languages, and advanced power management. Without a microprocessor, the Marl board sells for $386 in quantities of 100.

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http://www.radisys.com

CIRCLE 490

RICHARD NASS

PRODUCT FEATURES

Libraries And IC Design Kits Support Migration To 0.35-µm Technology

Providing designers true foundry portability without compromising design goals, and enabling existing 0.6- and 0.5-µm customers easy migration to the next generation 0.35-µm technology, are the prime goals of the library set introduced by Compass Design Automation. The 0.35-µm Passport logical and physical libraries works hand in hand with a suite of front-end IC design kits. The company's Passport Foundry Program provides a crucial link between model performance and silicon.

To that end, the IC design kits are, for the first time, being offered to designers at no charge via the World Wide Web. This move will ensure designers the fastest possible access to library technology. Through the Passport Foundry Program, a large selection of physical libraries is coupled with multi-foundry cooperation to provide a support network for designers making silicon-optimization-related decisions. Those supporting the 0.35-µm libraries include Chartered Semiconductor, LG Semicon, Taiwan Semiconductor Manufacturing Co., and United Microelectronics Corp.

The 0.35-µm Passport logical and physical libraries include the company's Optimum Silicon (OS) standard cells, RAM and ROM compilers, high-density datapath compilers, and a complete package of I/Os with approximately 100 different interface functions. The Passport OS standard cells, targeted for deep submicron design, offer designers high silicon area efficiency while still meeting power and performance requirements. Based on Optimum Silicon Library technology, optimized for both synthesis and place-and-route tools, Passport OS offers over 300 standard cell functions.

As opposed to traditional libraries, the Passport libraries allow designers the flexibility to specify their foundry of choice much later in the design cycle than previously possible. This inherent flexibility is crucial in the link between model performance and silicon because it acts as a guide when making silicon optimization decisions. In other words, the libraries enable designers to optimize silicon by choosing the fab that will provide them with the best price/performance ratio, most advanced features, intellectual-property (IP) blocks, and the shortest time to market without sacrificing design integrity. The 0.35-µm IC design kits are available on the Web. The 0.35-µm Passport libraries will be made available during the fourth quarter of 1996. In the U.S., cost will start at $350,000.

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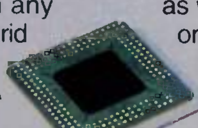

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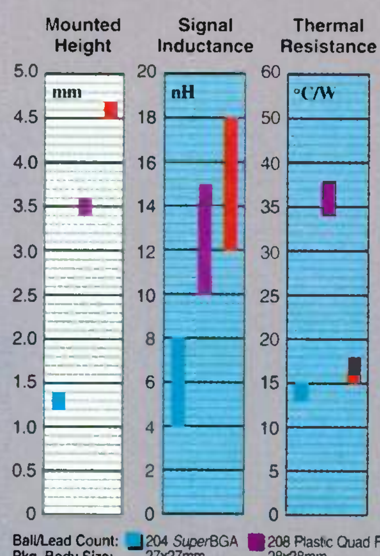

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READER SERVICE 97

ELECTRONIC DESIGN QUICK LOOK

Edited by Mike Sciannamea and Debra Schiff

MARKET FACTS

Those readers with kids, or perhaps a penchant for high-speed video games know what it's like to wait for the higher-powered system to be released. Behind all of it is the embedded controller. A new report from Frost & Sullivan, "The World Embedded Controller Market," discusses the growth of the market since 1992, and projects the future for the market through 2002. Information included in the new report is the result of interviews with semiconductor industry professionals, research from the World Semiconductor Trade Statistics organization, and other sources such as company financial reports and product literature. The report supplies details on revenues, unit shipments, and prices for five segments of the embedded controller market. There also is a geographic breakdown and end-user industry breakdown of revenues in the report. The world market, in this report, is broken up into four segments: North America, which includes Canada and the United States; Europe, comprising Western and Eastern Europe; Asia-Pacific, made up of Japan, South East Asia, Russia and the former Soviet Republics, India, Australia, and New Zealand; and Rest-of-World, which is made up of Central and South America, Africa, and the Middle East. The end-user industries are categorized as six different industries. They are: business computing, telecommunications, consumer electronics, transportation, industrial, and other. The highest embedded-controller-consuming industries in 1995 were the consumer electronics end-user industry with 32.6% of the total market revenues, and the telecommunications end-user industry with 26.2% of the total market revenues. Business strategies are outlined, and 30 companies in the market are profiled. In 1995, the value of the world embedded controller market was tagged at $11.34 billion. Frost & Sullivan's projection for 2002 has the embedded controller market pegged at $33.7 billion. Divided according to the width of the controller's data bus, the embedded controller market has five classes: 4-bit, 8-bit, 16-bit, 32-bit, and 64-bit embedded controllers. Further segmenting the market, embedded controllers are classified as either microcontrollers, as in the case of reprogrammable devices, and microprocessors, as in the case of devices that are not likely to need reprogramming. The report sees the fastest growing segments of the total embedded-controller market as the 16-bit at 23.2%, 32-bit at 25.6%, and 64-bit at 53%. Those percentages were measured as Compound Annual Growth Rates (CAGRs). Included in the report is a look at the migration to higher-performance embedded controllers. Two factors come into play when it comes to the migration to higher-performance devices. First, there's cost. As it stands today, the prices of low-end 8-bit controllers is in the same range as high-end 4-bit controllers. The same goes for low-end 16-bit controllers and high-end 8-bit controllers, and so on. Second, companies are looking at performance. They will choose to upgrade when the end-use product demands higher-performance, or when the price of that product is low enough to redesign for a wider bandwidth. But, as the report states, in the case of the toaster, it's unlikely that the company will upgrade to 32-bit processing no matter how low the price goes. The technological trends in the embedded-controller market point to the future development of smaller, faster, and more functional embedded controllers. On chip developments include faster clock speeds, integration of more peripheral functions, lower operating voltages, and new process technologies. Additionally, the report exposes the best business strategies for vendors in the embedded-controller marketplace, the most significant end-user industries, and the major competitive factor in the industry.

Worldwide Revenues of Embedded Controllers

Year	4-Bit (%)	8-Bit (%)	16-Bit (%)	32-Bit (%)	64-Bit (%)
1992	22.7	57.0	12.4	7.9	0.0
1993	19.5	55.5	15.4	9.5	0.1
1994	16.8	53.6	18.1	11.0	0.5
1995	14.3	51.7	20.4	12.5	1.1
1996	12.2	49.8	22.2	14.0	1.8
1997	10.5	47.9	23.6	15.3	2.7
1998	8.9	46.0	24.9	16.5	3.7
1999	7.5	44.0	26.2	17.6	4.7
2000	6.2	42.0	27.6	18.6	5.6
2001	5.1	40.0	28.9	19.6	6.4
2002	4.3	38.3	29.5	20.8	7.1

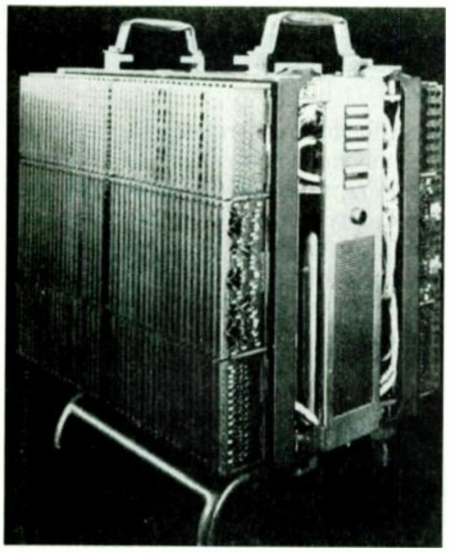
Source: Frost & Sullivan

For more information contact Frost & Sullivan, 2525 Charleston Rd., Mountain View, CA 94043; (415) 961-9000; fax (415) 961-5042; Internet: http://www.frost.com.—DS

40 YEARS AGO IN ELECTRONIC DESIGN

Midget Field Computer

RECOMP, a midget computer that can add, subtract, multiply and divide several times faster than the familiar desk type calculator, has been designed and developed by Autonetics, a division of North American Aviation Inc. To be used by the Air Force, RECOMP had to have the features of a true field instrument, for use where data transmitted over long distances to and from a central computing facility is too inaccurate or late. It weighs 200 lb, can be carried suitcase fashion by two men, or it can be transported, without bracing or padding, in a jeep or weapons carrier. Power dissipation has been held to 600 w, and the computer can be plugged in to any standard source of 115 v, 60 to 60 cps ac. RECOMP is a serial, single address, internally binary computer, having from 12 to 16 arithmetic instructions, 17 logical and transfer instructions and from 5 to 8 input-output instructions. It was designed to utilize a rotary magnetic disc memory with a main memory capacity of 2048 words and 4 arithmetic registers (a new model has a 40322-word capacity). Transistors are used exclusively and the circuits in the computer are so designed that component values are not critical. *(Electronic Design, March 1, 1957, p. 7)*



A first reaction might be to chuckle over that line about this "midget" computer being carried by two men, but don't forget that the invention of the IC was still more than a year away. This meant that not only were individual transistors used for the logic, but the DRAM IC was unknown, so it had to use a magnetic-drum memory, which probably accounted for much of the weight.—SS

Cryotron—Computer Revolution

The first useful application of superconductivity is embodied in the Cryotron, a new device that may upset transistor use in computers. The Cryotron operates only at the temperature of liquid helium within a cryostat. The advantages of the device are extremely small size—100 of the units will fit into a thimble—and small use of electric power. The complexity of computer circuits required for such applications as language translation are well suited to the size and simplicity of the Cryotron. Built-in multiplication tables in the memory unit would free the arithmetic section for higher mathematical or logical problems. Developed for practical application by the Arthur D. Little advanced science laboratory in Boston from research at M.I.T. by Dudley A. Buck, a Cryotron memory device could have all elements searched simultaneously, improving speed and efficiency of access.

The Cryotron comprises a single straight wire around which a wire coil is wrapped. The straight wire conducts current with no resistance. In the control winding a current produces a magnetic field which destroys superconductivity in the straight wire—and resistance is returned. Control winding current can also cut off current in the straight wire. One disadvantage is the slow speed in switching current among multiple paths, but the Cryotron itself can switch from one condition to another as rapidly as a transistor or vacuum tube. Present Cryotrons use tantalum and niobium wires. New metals and alloys may make possible a faster operation of the Cryotron. *(Electronic Design, March 15, 1957, p. 5)*

A lot of work has gone into attempting to exploit superconductivity in computers, but silicon has been hard to beat out.—SS

Just For The Kids

Stumped by questions like "Why is the sky blue?" or "How are bridges built with the water in the way?" If you find yourself promising answers, but not delivering, write down all the questions between now and April 23.

Sponsored by the National Science Foundation, the "Ask a Scientist or Engineer Hotline," (800) 682-2716, will be up and running from 9 a.m. until 9 p.m., Eastern Standard Time on April 23. This year will be the third successive year of the hotline in honor of National Science and Technology Week.

Aside from answering questions, the scientists and engineers (supplied by the federal government) will be explaining how the answers were found. They'll also give the adult callers some tips on how to better share science and engineering with their kids.

During the entire week of April 20-26, the scientists and engineers may be reached by via e-mail: asknstw@nsf.gov.

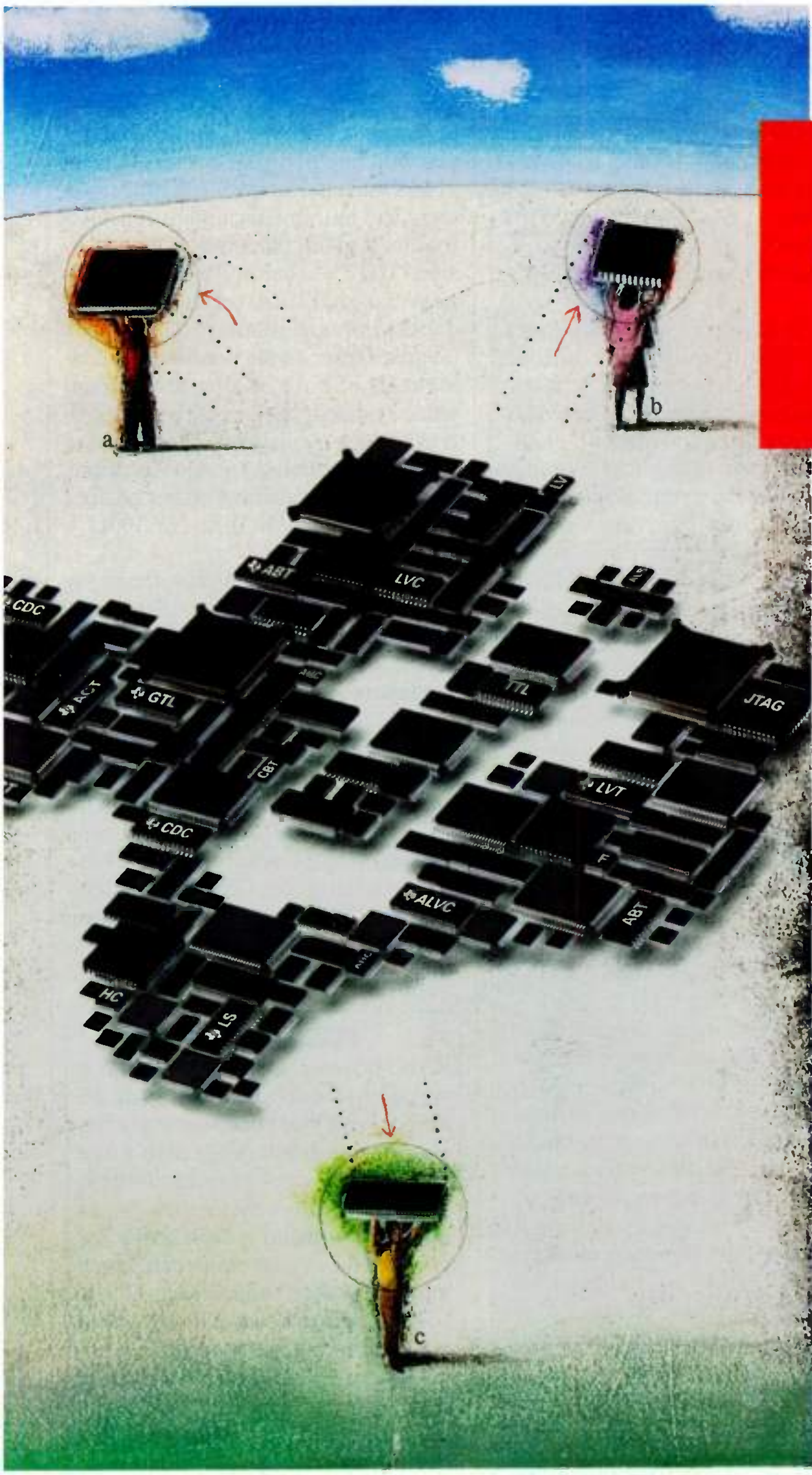
Little kids, ages three to eight might enjoy two new releases of Junior Arcade games from Humongous Entertainment.

Freddi Fish and Luther's Maze Madness and Freddi Fish and Luther's Water Worries are available on hybrid Windows and Macintosh CD-ROMs, and are priced at $14.95 each.

Both games have a Junior Helper feature which is activated when the cursor is at the bottom of the level-selection screen. In Maze Madness, it gives Freddi Fish the option of a bubble shooter, and in Water Worries, it gives Luther a Codfish Commando Action Urchin Suit. In both games, Junior Helper gives kids Unlimited Tries.

There also is a Custom Level Editor to build, save, and play mazes in the Maze Madness game.

For details, contact Humongous Entertainment, 16932 Woodinville-Redmond Rd. NE, Woodinville, WA 98072; (206) 486-9258; fax (206) 486-9494; Internet: http://www.humongous.com.—DS



How many suppliers does it take to meet your logic needs?

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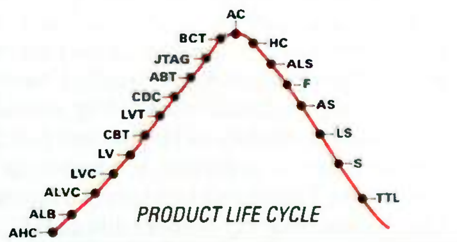
TI wrote the book on logic.



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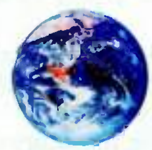

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TRUDEL TO FORM

JOHN D. TRUDEL
CONTRIBUTING EDITOR

Whenever I discuss good practices and name companies as examples, it usually leads to a ripple of comment. For the last year or so, I have noticed a new tone. A few readers asked if I owned stock in the companies I touted. One paranoid New Yorker demanded written, signed assurance that I did not.

Let's address that. As a Certified Management Consultant, I am sworn to a "squeaky clean" code of ethics. (The IMC code is on my web page, along with information about my practice and business philosophy. I have just added "selected readings," including the preface to my forthcoming book, *Engines of Prosperity*.) Among other things, I am required to avoid conflicts of interest and to always act in my clients' best interests.

I avoid impropriety or the appearance of impropriety. How can I consult for Company A if I hold a stock position in Company B, a competitor? Even owning stock in a client could pose similar problems. The leaders of winning companies—Andy Grove of Intel, Bill Gates of Microsoft—are conspicuous for making the right decisions, even if it causes a hit in their stock price. So, for reasons like that, I avoid direct stock ownership.

When you stand in your truth and do what you think is right, it often reflects back to your benefit. Since I have avoided direct stock trading and moved to mutual funds and trusts, I have prospered. I pick funds, and let the fund managers decide what to buy and sell.

I view my readers as clients, and feel that I owe them the same integrity. My columns are as correct and honest as I know how to make them. I spent time on the Patent Sell Out because the mainstream press is clueless, because this issue affects my readers and clients, and because I think the winners of the Patent Wars will own future prosperity. Was I paid for this? Well, one reader sent me a check for $25. I was so frustrated that I kept it and bought a nice dinner.

But, you were right to ask, dear readers. My resultant awakening is understanding that in the Information Age, honesty and knowledge are precious and scarce.

Alvin Toffler, the futurist, now says, "The sophistication of deception is increasing faster than the technology for verification. That means the end of truth." Political, executive, corporate, and governmental flacks and lawyers are exceptionally effective at misdirection and covering up unpleasant truths. It is hard to fix problems when much of what we believe to be so is not.

It is refreshing to live in a state like Oregon, for here the deceptions remain folksy. For example, a brain-dead political appointee squandered over $50 million on a database for drivers' licenses that never worked. Since very few people live in Oregon, a PC-server and some standard software would probably have done the job. We are talking basic incompetence here.

Laughably, Oregon hired a PR firm and mounted a campaign pointing out that several other states have wasted just as much money on defective drivers' license databases. I suppose that makes it OK?

Episodes like the Patent Sell Out, Donorgate, and the O.J. trial move deception onto a different plane, one where expert testimony and judicial process is almost worthless. The solution: Deep knowledge and knowing whom you can trust. Take the time to learn truth. Then take informed action.

John Trudel, CMC, provides business development consulting and is the author of "High Tech with Low Risk." He is founder and director of the Trudel Group, 33470 Chinook Pl., Scappoose, OR 97056; (503) 640-5599; fax (503) 543-6361; e-mail: johntrudel@aol.com; Internet: http://members.aol.com/johntrudel.

OFF THE SHELF

"Video Engineering, Second Edition" provides full coverage of the many growing nonbroadcast applications of video, such as computer display systems and multimedia applications. Attention is given to high-density television (HDTV) technology, as well as uses of digital video technology in the generation and display of computer images. Other sections address fundamentals of both analog and digital video systems, basic criteria for specifying image quality, and application of colorimetric theory to video systems. Contact McGraw-Hill Companies Inc., 11 W. 19th St., New York, NY 10011.

"Tolerance Design: A Handbook for Developing Optimal Specifications" addresses the upstream process of developing specific tolerance values, encompassing the analytical and experimental steps used in this process. The book emphasizes tolerance design using Taguchi's Quality Loss Function in harmony with Motorola's methods for Six Sigma quality. The 448-page book is priced at $58. Contact Addison-Wesley Publishing Co., Corporate & Professional Publishing Group, One Jacob Way, Reading, MA 01867; (617) 944-3700; Internet: http://www.aw.com/cp.

FEEDBACK TIPS

If you haven't used snail mail in a while, the new postage stamps no longer have that yucky-tasting adhesive on the back (they also have some really cool comics stamps, too). They're ready to stick on an envelope, making it even easier for you to send in your comments about material you've seen here in QuickLook. Of course, we'd love to send positive reinforcements back to the professors who doubted we'd make it through the semester, back in college, but we welcome all correspondence. Try stuffing our e-mailboxes: Mike Sciannamea's is **mikemea@class.org**, and Deb Schiff's is **debras@csnet.net**. Then again, there's always our friends in the mailroom: The Copy Desk/QuickLook, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604. Our fax number is (201) 393-0204.

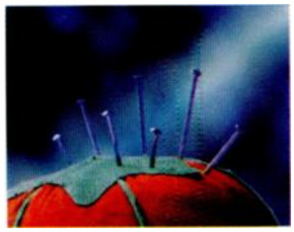
PPING THROUGH THE INTERNET ROLODEX

://www.digikey.com: Click is URL to find Digi-Key Corpo- n's new on-line order form. The ew form has links from the page to other information pages explaining the various entry spaces. Also at the site, visitors can use their Adobe Acrobat application to view Digi-Key's Electronic Catalog. For engineers in search of information from other companies, there is an extensive list of industry links.

http://www.xentek.com: Stop into the Xentek Power Systems home page for quick updates on their line of dc-power supplies, dc/ac inverters, extreme-isolation transformers, ac-power conditioners, and UPS systems. Visitors seeking notes on the company's newest line, the Mosaic Series, a group of modular, open-frame, switching power supplies, will find them here. In addition, the PowerGuard industrial-grade and LifeGuard medical-grade extreme isolation transformers, power-line conditioners, LCD backlight drivers, and custom power supplies can be found at the site. There are performance specification tables, application notes and case studies, graphical illustrations of products, diagrams and descriptions of product functions, and technical articles.

http://www.payneng.com: Visitors to Payne Engineering's home page will find information on the company's line of solid-state power and motor controls. For World Wide Web surfers who don't like waiting for all those graphics to load, Payne Engineering has designed their site to be light on the graphics and heavy on the text. At the site visitors will discover an application guide for motor controls. There also is a descriptive listing of 11 different solid-state power controls, complete with the product's dimensions, pricing, and ratings.

http://www.national.com: Pull into National Semiconductor's site for a complete and up-to-date library of the company's 27,000-plus product line. The product listing is set up as a series of application notes, design tools, electronic datasheets, and software behavior models. There's a Java-based parametric search engine for searching by keyword, part number, or product type. The Java technology also is used to produce product abstracts instead of forcing the surfer to wait for complete PDF file downloads. Also at the site, visitors will find the latest information on events and seminars. Links at the site lead to sales contacts and technical support. A unique feature at the site is the sample ordering capability. Here, visitors who order samples can have them within three days.



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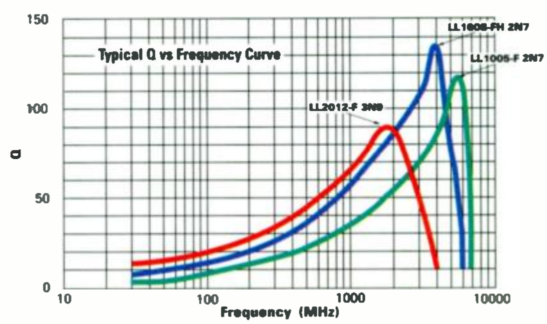

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Engineers Of Tomorrow Meeting In Canada Today

In late January, approximately 125 young women from Montreal high schools met at Concordia University, Montreal, Canada to discuss their possible futures as engineers. The fifth annual Engineers of Tomorrow Conference was organized by Concordia's Engineering and Computer Science Student Association.

Opening up the school's laboratories, Concordia exposed the teens to what was probably their first look at a Human Factors lab, a Biomedical lab, a Robotics lab, or a Light Twin-Engine Aircraft Flight Simulator lab. The Human Factors lab hosts experiments in ergonomics. The Biomedical lab, during the lab tours of the conference, was used in researching the applications of ultrasound in speech-language pathology. The Robotics lab is the scene of research on construction of light-weight robots, and the motion of robotics. Through the work of the Fluid Power, Control & Simulation Research Laboratory, the flight simulator training system is based on a pneumo-hydraulic, active, force-feel mechanism.

The visiting high schoolers also saw the concrete toboggan which student teams built out of concrete and other building materials. The toboggan competes annually in the Great Northern Concrete Toboggan Race which sees over 48 teams from around Europe and North America. The race this year was held in Ottawa, Ontario.

During the conference, the young women were involved with three hands-on workshops, "Eggstravagant Contraptions," "Unbreakable Bridges," and "Photoelectric Sensors." "Eggstravagant Contraptions" was an exercise in mechanical engineering which took the teens through designing a crack-proof shelter for an egg that would be dropped from a significant height. "Unbreakable Bridges" was a study in civil engineering, with a focus on designing the strongest possible bridge. The "Photoelectric Sensor" workshop gave the teens a basic look at electrical/computer engineering, with an emphasis on connecting photoresistors, diodes, and dc power.

Speakers included Corinne Mount Pleasant-Jetté, assistant professor in engineering and computer science at Concordia; Jane Norsworthy, project manager, Ericsson Research; Bernice Lamb-Sénéchal, manufacturing engineer, SPAR Aerospace; Ruxandra Botez, research engineer, Canadair; Zsuzsanna Bencsath-Makkai, biomedical engineer, McGill University; Jana Simandl, professor of chemical engineering, McGill University; Maria Elektorowicz, assistant professor of civil engineering, Concordia; Maria Corsi, technology transfer consultant, SIRICON; and Yimina Boumahdi, research engineer, Ericsson Research.

For more information, contact Concordia Univeristy, 1455 de Maisonneuve Blvd. West, Suite H880-10, Montreal, Quebec, Canada H3G1M8; (514) 848-7408; fax (514) 848-4535.—*DS*

Y2K UPDATE

In my searches around the web, I stumbled upon a call for members for the New Jersey Year 2000 User Group on the Year 2000 Information page, run by Peter de Jager (http://www.year2000.com/cgi-bin/y2k/year2000.cgi). I signed up, and within a month, or so, I received an invitation to the first annual meeting of the group, which was held at Matsushita Electric Corp. of America (Panasonic), in Secaucus, N.J.

Mike Cervine, manager of application administration at Panasonic, had sent me, along with approximately 40 others, the e-mail. Of that 40, 20 interested Y2K-compliance professionals showed up at the meeting, in addition to the presenters from PKS Information Systems, Omaha, Neb., (402) 496-8500; Hexaware, Princeton, N.J., (609) 951-9195; and Princeton Softech, Princeton, N.J., (609) 497-0205.

The vendors were given the morning session of the meeting to present their services and tools, and take questions from the group. They also stayed for lunch, participating in a much more informal question and answer setting.

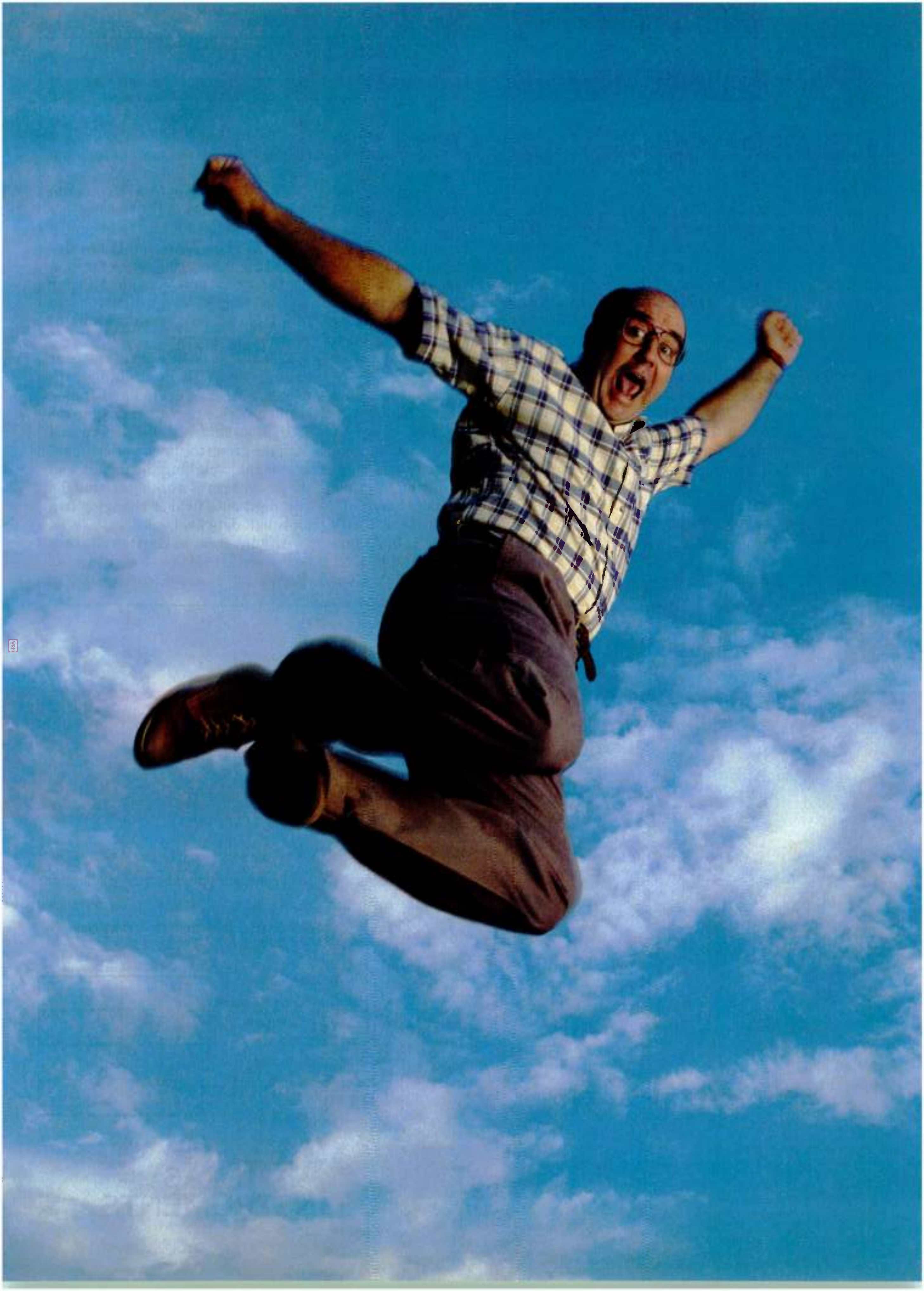
According to Brigante Hill, director of sales for PKS, the two most important facets of choosing a Y2K services vendor are "trust and talent." Basically, companies that plan to exist past 2000 are putting their businesses in the hands of a vendor they hardly know.

The answer to that issue is asking the vendor to perform a pilot study. Donna Agnew, sales manager at Hexaware, explained that some of their clients decided to try the pilot program of their solution because their service is primarily based offshore in India. One of Hexaware's clients, The Equitable Life Assurance Society, used the pilot project system, testing Platinum's SystemVision Year 2000 tool to project cost and resources, and determine impact analysis.

Version Merger from Princeton Softec was presented at the meeting as a reconciliation tool to organize Y2K changes. The tool is not designed for change control (or for PCs, for that matter). Version Merger works with MVS applications to identify all multiple versions of records and programs.

The afternoon session of the user group saw Y2K compliance approaches from Cervine and James Kinder, Y2K program manager for ADP, Roseland, N.J. Both discussed with the group the "two-versus-four" argument, weighing the merits and the drawbacks of working around the two-digit date field or changing to a four-digit date field.

Any interested Garden Staters can e-mail Mike Cervine at *cervinem@panasonic.com.—DS*



RISC performance without scrapping code. And you thought engineers were a low-key bunch.

Engineers haven't been exactly giddy about moving from CISC to RISC. Rewriting code, blowing a ton on memory to support it, and delaying time to market. ColdFire™ technology from Motorola offers an exciting alternative. The cost-effective ColdFire architecture is derived from Motorola's 68K microprocessor family, and is supported by industry-leading development tools. So you can build on current product designs and programming experience to get to market faster, with a smaller investment. Plus, the ColdFire microprocessor's variable-length RISC instruction set maximizes code density, thereby reducing the amount of costly memory required to store it. All of which delivers a new level of price/performance for cost-sensitive applications. For more information on ColdFire microprocessors, call your Motorola representative at 1-800-521-6274 (ref. #HP002). Or visit www.mot.com/coldfire. You'll see a dramatic difference.

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Security At The Touch Of A Finger

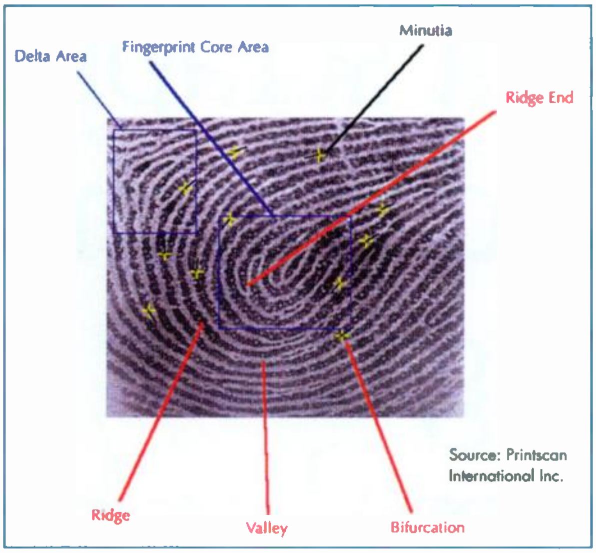
One of the hotter topics in technology today is security. More individuals and companies are taking steps to protect their most valuable information. For individuals, that may mean their credit cards, and for companies, that may mean access to their computer network and databases.

However, using a secret password or giving someone a key to the office simply is not enough. People can and will find ways to get that information. But there is a much more secure form of identifying someone, and it can be found at the tip of your finger.

A new fingerprint identification and verification system has been patented that uses an electronically-scanned fingerprint interpreted by a new software program.

PrintScan International Inc.'s PrintScan Core software is written in ANSI-C and is portable to any hardware and software program. It can be used for any number of applications that require identification and verification, including ATMs, smart cards, computer and home security, and financial services.

Utilizing PrintScan's patented Conicident Sequencing technology, the system accomplishes, in milliseconds, the same fingerprint identification and verification that normally takes hours of manual analysis by trained experts—with the same degree of accuracy. Minutiae from a scanned fingerprint are encoded and stored, then compared to the image of the actual fingerprint being presented. Coincident Sequencing refers to the information that is extracted and used to compare the fingerprints. This includes the type of minutiae (i.e., a ridge end or a bifurcation), the location of the minutiae, the direction in which the minutiae are pointing, and the intervening ridge counts *(see the figure)*.



Source: Printscan International Inc.

For law enforcement applications in the U.S. and most countries, a minimum of 8 minutiae in full coincident sequence is required. But for commercial applications, if a minimum of 8 minutiae are in full coincident sequence and the minutiae are not all in the core or delta areas of the fingerprint, then the two images are of the same fingerprint. This is the only internationally accepted method of comparing fingerprints when confirming identity.

PrintScan software stores only the algorithm; it does not store the entire fingerprint, and the entire fingerprint cannot be recreated. The PrintScan technology embodied in the core software is extremely accurate, with a 0% false accept rate, and a 1 out of 100,000 false reject rate.

For more information on the technology, contact PrintScan International Inc., 101 College Road East, Princeton, NJ 08540-6601; (609) 452-1716; fax (908) 302-9510; Internet: http://www.printscan.com.—*MS*

When There's A PC, There's An A

The days of kids only using computers to play games are effectively over. According to two new surveys, the computer is now an essential educational tool in both the classroom and the home, leading to more effective teaching methods, and most importantly, better student grades.

Both surveys, conducted by the Consumer Electronics Manufacturers Association (CEMA), indicate that students between ages of 12 and 18 and full-time teachers of grades K-12 agree that not only are computers becoming more important in education, but that both groups alike prefer to use computers, and feel they perform better with them. Dick James, chair of CEMA's multimedia division, says, "When deciding whether to purchase a PC for the family, parents should consider potential improvements in their children's education as yet another reason to make the investment."

Of the teachers surveyed, 56% said that computers were "very effective" as a teaching tool, while 40% responded "somewhat effective." Student responses reflected similar views. Of those who use a computer to do homework, 66% said they enjoyed computer assignments than those not done with a PC, with nearly 50% saying that they liked PCs "a lot better."

CEMA says that grades is one reason why the positive responses are so high. Forty-five percent of students said that their grades have improved since they started doing assignments on the computer, while 54% said that their grades stayed the same. Teachers saw similar improvement—68% said that grades on computer assignments are better than those assignments that do not require a computer's use.

The surveys also indicate that computers in the classroom are being used much more frequently. Over half of the teachers asked said that they and their students use computers in class at least 10 hours a week, with 33% responding that they used them at least four hours a week. The numbers directly reflect the greater accessibility of computers in school—50% of teachers said that there are over 50 computers in their particular school, and 82% of the students said that they use computers at school. In addition, over 60% of schools have Internet access, either through a direct connection or an on-line service (Compuserve, Prodigy, etc.).

For more information on the survey, contact CEMA, 2500 Wilson Blvd., Arlington, VA 22201-3834; (703) 907-7674; fax (703) 907-7690.—*MS*

And if you like our itsy-bitsy ball grid array chip-size Flash—as small as 8x8mm in its 8Mb 42-pin package—you should check out the whole huge colony of Flash products

INTERNET NEWS

Network, a free news network making its home on many corporate monitors these days, is now being packaged with Microsoft Internet Explorer 4.0 Active Desktop. In addition, the joint venture news product of the '90s, MSNBC will be joining the PointCast Network as a news and information provider.

Another part of the deal was PointCast's choosing the Microsoft Active Platform for its strategic development and delivery system in the new PointCast Network 97 release. With the new release, of course, the preferred browser will be listed as Internet Explorer.

Currently, the PointCast central broadcast facility boasts over 40 million hits a day. The company's servers run on Microsoft Windows NT.

Other wheelings and dealings at PointCast include a partnership with Compaq Computer Corp. to include a customized version of the broadcast software in Deskpro 2000 and Deskpro 4000 commercial PCs. Compaq also has its own channel, the Compaq Channel on PointCast, that distributes articles, software update news, and other information to users.

For example, a Compaq user will turn on his or her system in the morning to check their e-mail, and there might be an announcement about a driver update, product enhancement, new product, or support information.

Recently, PointCast opened up its doors to Macintosh users. By visiting the World Wide Web site, **http://www.pointcast.com**, Macintosh owners can download the software for free. When the Mac is idle, PointCast's SmartScreen technology automatically runs the network, turning the screen into a news and information center. Headlines, stock quotes, weather reports, etc., scroll across the screen, waiting for the user to click on a word for the full story.

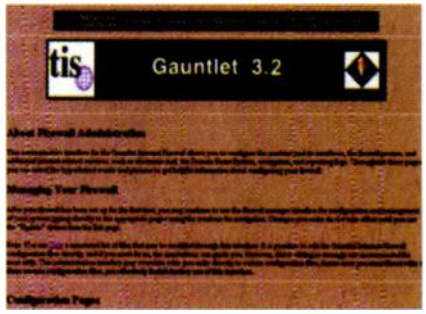
For more information, contact PointCast, 2475 Augustine Dr., Suite 101, Santa Clara, CA 95054; (408) 253-0894; fax (408) 235-8590.

In the dynamic world of encryption technology, a recent memorandum and executive order from President Clinton has sent companies to the Commerce Department for the details on export controls.

One company in particular, Trusted Information Systems (TIS), has garnered approval from the Commerce Department for the company's RecoverKey technology-laden products. The very-strong cryptography technology is found in the TIS Gauntlet Internet Firewall, with both the 56-bit Data Encryption Standard (DES) algorithm and Triple-DES; and the TIS Cryptographic Service Provider which supports the Microsoft Cryptographic Application Programming Interface using both DES and Triple-DES encryption.

Licensing arrangements have blossomed as a result of the Key Recovery Alliance formed by 40 information technology vendors and users, including TIS. TIS has licensed its RecoverKey technology to Hewlett-Packard for the company's International Cryptographic Framework.

The company's Internet firewall, Gauntlet Version 3.2, uses a "Crystal Box" technique, which distributes source code for assurance reviews. It's built on a hardened BSD/OS operating system, and runs on Intel's Pentium-based platform. TIS does offer the software in Hewlett-Packard, Windows NT, Solars, Sun MicroSystems, and Silicon Graphics capable platforms.



Other features include transparent access, firewall-to-firewall encryption, integrated management tools, built-in "smoke alarms" (designed to go off when connections to unsupported services are attempted), and an audit tool.

A Gauntlet spin-off from TIS is ForceField. It's a transparent web server security system that prevents the nasty graffiti that hackers can leave on web sites. ForceField comes ready to install on Apache, Netscape, or Open Market webservers.

Features of the security system include operating system hardening (prevents IP spoofing, OS attacks, Syn Flooding, etc.), access controls ("authorized only" users may change site contents or enter server administrative areas), Virtual Private Networks (secure, remote administration and content development), and smoke alarms.

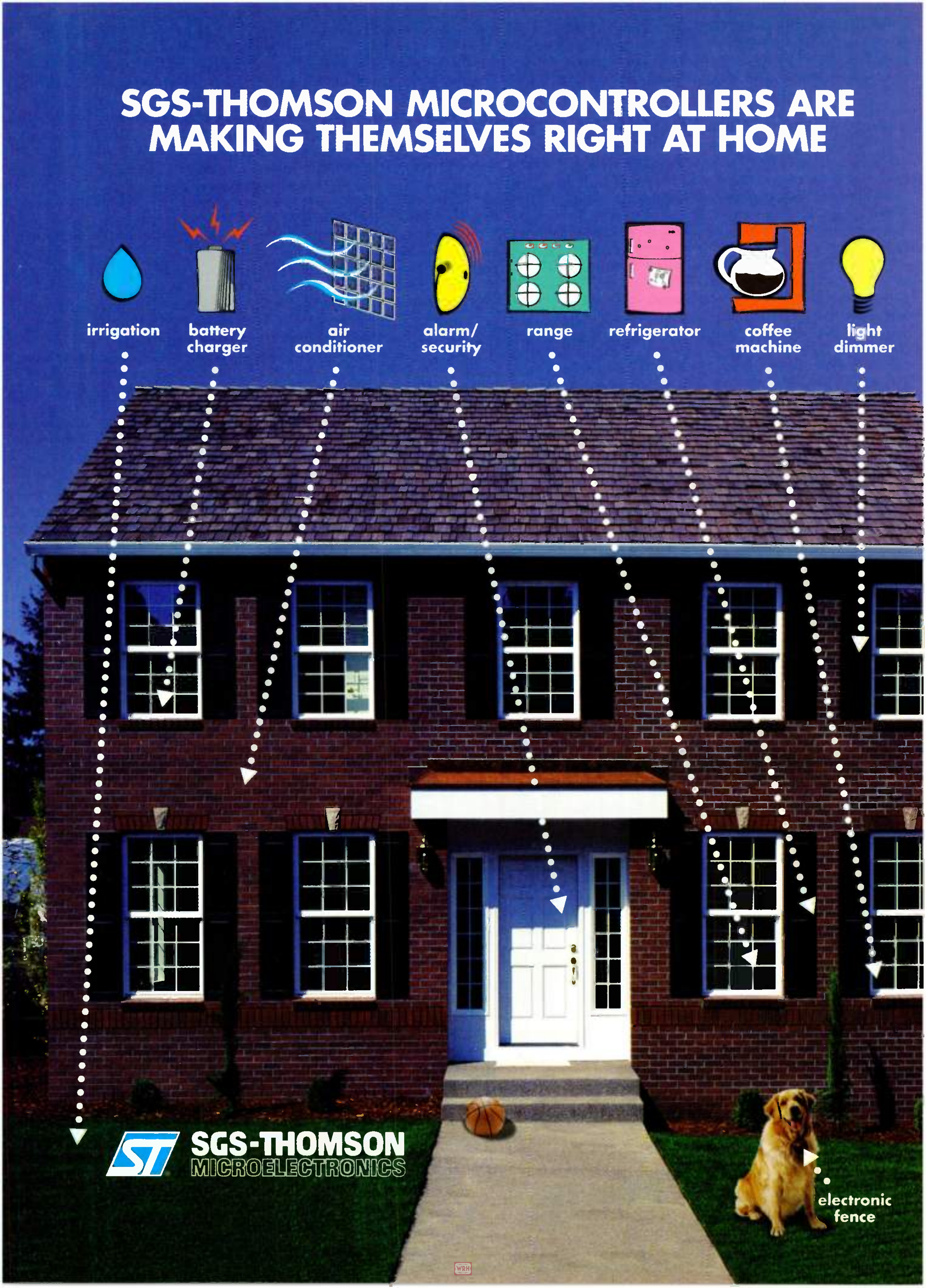
For more information, contact TIS Inc., 152 Omega Dr., Rockville MD 20850; (888) FIREWALL, fax (301) 527-0482; Internet: http://www.tis.com.

Also in the protection game is Querisoft Inc. The company has recently introduced its SecureFile personal information security tool. The software uses the beta release of Microsoft's CryptoAPI 2.0 to interface with cryptographic technology. SecureFile is seamlessly integrated into the Windows 95 and NT 4.0 Shell Interface, and provides a Wizard-based GUI for users creating secure documents.

The user has a wide variety of encrypting algorithms from which to choose, depending on their security needs. Compliant with security standard X.509 v3, SecureFile also supports PKCS#7 file formats. In addition, the tool allows multiple pluggable cryptographic engines and multiple algorithms. Secure operations may be performed using Java scripts or Visual Basic language.

The application has a SecureFolder feature that allows users to drag and drop single or multiple documents into the folder for convenient security. There are features for certificate storage, exporting, and importing.

For more information, contact Querisoft Inc., 3475 Oak Valley Rd., Suite 1210, Atlanta, GA 30326; (404) 812-6272; (404) 841-9377; Internet: http://www.querisoft.com.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alarm/ security
range
refrigerator
coffee machine
light dimmer
electronic fence
SGS-THOMSON
MICROELECTRONICS

LET OUR MICROS MAKE YOUR PRODUCT A HOUSEHOLD WORD

The reason SGS-THOMSON's 8-bit ST62 family of MCUs is making itself at home in so many household appliances can be summed up in one word: *Value*. ST62 devices deliver more performance in less space for less money. Even the core is optimized for cost-effective operation. Add ESD protection and unmatched noise immunity and you begin to understand why the ST62 is opening doors to consumer applications that remain closed to ordinary MCUs.

Additional ST62 MCU Applications

- washing machine
- power tool
- heater
- UPS
- thermostat
- scale
- programmable timer
- vacuum cleaner
- home bus

All ST62s contain ROM, RAM, an 8-bit timer with 7-bit programmable prescaler and multifunctional individually programmable I/O ports. Also available: Devices with high-current buffers to directly drive LEDs or TRIACs, along with a wide range of peripherals such as PWM and LCD drivers. A wide operating voltage range and robust design allow ST62 microprocessors to be powered directly from a battery or the main with minimum external components.

In addition to the extensive ST62 family, SGS-THOMSON offers other 8-32 bit micro solutions such as ST7, ST9, ST10 and ST20 families. All of these products are fully supported with extensive development tools including C compilers for most families. So why not let our micros help make your product a household word. To find out more fax 617-259-9442, write SGS-THOMSON, 55 Old Bedford Road, Lincoln, MA 01773, or e-mail: info@stm.com. And visit our web site at **http://www.st.com**

ST6
The 8-bit MCUs of choice in automotive and industrial as well as consumer applications. Instruction set and addressing modes maximize code efficiency.

ST7
Powerful industry standard 8-bit core, surrounded by numerous advanced peripherals. 3K to 48K of ROM with different RAM sizes. Choose EPROM and OTP versions for proto-typing. On-chip EEPROM is also available for integrated data storage.

ST9
8/16-bit micro family fills requirements of most advanced computer, consumer, telecom, industrial and automotive applications.

Service and Technology

For More Info Turn Page

READER SERVICE 142

OUR 8-BIT MICROS ARE BECOMING HOUSEHOLD WORDS

	DEVICE	PROGRAM MEMORY	RAM	EEPROM	A/D INPUTS	TIMERS	SERIAL INTERFACE	I/O's	PACKAGE	OTHER FEATURES
*	ST6200	1K ROM	64		4x8-Bit	1x8-Bit		9	DIP/SO16	
*	ST6201	2K ROM	64		4x8-Bit	1x8-Bit		9	DIP/SO16	
*	ST6203	1K ROM	64			1x8-Bit		9	DIP/SO16	
*	ST6208	1K ROM	64			1x8-Bit		12	DIP20/SO20	
*	ST6209	1K ROM	64		4x8-Bit	1x8-Bit		12	DIP20/SO20	LED or TRIAC driver
*	ST6210	2K ROM	64		8x8-Bit	1x8-Bit		12	DIP20/SO20	
*	ST6215	2K ROM	64		16x8-Bit	1x8-Bit		20	DIP28/SO28	
*	ST6220	4K ROM	64		8x8-Bit	1x8-Bit		12	DIP20/SO20	
*	ST6225	4K ROM	64		16x8-Bit	1x8-Bit		20	DIP28/SO28	
	ST6240	8K ROM	216	128	12x8-Bit	2x8-Bit	SPI	16	QFP80	
	ST6242	8K ROM	152		6x8-Bit	1x8-Bit	SPI	10	QFP64	LCD driver (segment) + LED or TRIAC driver, 32KHz oscillator
	ST6245	4K ROM	140	64	7x8-Bit	2x8-Bit	SPI	11	QFP52	
*	ST6253	2K ROM	128		7x8-Bit	2x8-Bit		13	DIP20/SO20	
*	ST6260	4K ROM	128	128	7x8-Bit	2x8-Bit	SPI	13	DIP20/SO20	auto-reload timer + LED or TRIAC driver + PWM
*	ST6263	2K ROM	128	64	7x8-Bit	2x8-Bit		13	DIP20/SO20	
*	ST6265	4K ROM	128	128	13x8-Bit	2x8-Bit	SPI	21	DIP28/SO28	
	ST6280	8K ROM	320	128	12x8-Bit	2x8-Bit	SPI, UART	22	QFP100	LCD driver (dot matrix) + auto-reload timer + LED or TRIAC driver
	ST6285	8K ROM	288		8x8-Bit	1x8-Bit	SPI, UART	12	QFP80	
	ST7291	8/16/24K ROM	256/384			1x16-Bit		19	DIP28/SO28	wake-up function + power saving & standby modes + power supply monitor
	ST7294	6K ROM	224	256		1x16-Bit		22	DIP28/SO28	wake-up function + power saving & standby modes + WDG
	ST9036	16K ROM	224+256		8x8-Bit	2x16-Bit	SPI+SCI	56	LCC68	WDG + handshake + Direct Memory Access
	ST9040	16K ROM	224+256	512	8x8-Bit	2x16-Bit	SPI+SCI	56	LCC68	
	ST90R50		224		8x8-Bit	3x16-Bit	SPI+2xSCI	56	LCC84	WDG + 2 handshakes + Direct Memory Access + 16 M Bit address
	ST90R52		224		8x5-Bit	3x16-Bit	SPI+2xSCI	52	QFP80	

Abbreviations:
ADC = Analog to Digital Converter
SCI = Serial Communications Interface
WDG = Watchdog
SPI = Serial Peripheral Interface
USART = Universal Synchronous/ AsynchronousReceiver/Transmitter

Packages:
DIP = Dual In Line
QFP = Quad Flat Pack
S = Shrink
LCC = Leaded Chip Carrier
SO = Small Outline

Also check out our new ST62 REALIZER

The ST62 REALIZER is a user-friendly tool that assists designers in developing applications based on the ST62 family. A graphical schematic description of the application is used to automatically generate the executable code for the ST62 and to run simulations for verification of the program function. The complete tool set runs under Microsoft WINDOWS® environment.

*More Gold Standard devices available from ST (OTP versions only)

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Complete product information at http://www.st.com

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QUICKNEWS

Source Code Solution Sold—Cygnus Solutions has announced the company's acquisition of multiX Software GmbH, Stuttgart, Germany, the developer of Source-Navigator cross-platform graphical source code browsing and editing software. Cygnus plans to integrate Source-Navigator into its existing GNUPro CDK product line.

The Source-Navigator tool is targeted at new engineers, designers working on cross-platform porting or re-engineering, and managers who need a logical look at the source code structure. The software is UNIX- and Windows NT-compatible.

According to Cygnus, Source-Navigator has been well-suited to applications where code line counts are above 100,000.

MultiX will still serve as the technology developers and sales staff, while Cygnus will distribute and support the tool.

For more information, contact Cygnus Solutions, 1325 Chesapeake Terr., Sunnyvale, CA 94089; (408) 542-9600; fax (408) 542-9699; Internet: http://www.cygnus.com.

Stream Of Consciousness—Supporting high-speed data from Direct Broadcast Satellite (DBS) providers, ComStream's satellite receiver transmission technology has been chosen by Microsoft as a component in the PC/TV product strategy.

ComStream's background includes delivering approximately two million digital satellite receiver subsystems to DSS TV set-top manufacturers. The technology uses industry-standard MPEG2 decompression and display interface. It's packaged in a standard PCI-bus architecture.

For more information, contact ComStream Inc., 10180 Barnes Canyon Rd., San Diego, CA 92121; (619) 657-5416; fax (619) 657-5404; Internet: http://www.comstream.com.

A Removable Feast—Mitsubishi Chemical America Corporation has made the move to use the AdvanSCSI ABP960 PCI host bus adapter from Advanced System Products in its MCA2600 5.25-in. removable media magneto-optical drive.

The large-capacity, high-performance drive boasts a 39 ms seek time, 3000 RPM rotational speed, and transfer rates of 3.3 Mbytes/sec.

The ABP960 bus adapter uses a jumper switch to alternate between PC or Power Mac settings. It also is soft-configurable.

The PCI-host bus adapter is based on a 50-MHz RISC processor, giving the CPU's I/O load a break. It sees transfer rates of 133 Mbytes/sec. Additionally, the adapter is Plug-and-Play capable, and meets SCAM and PCI local bus standards.

For more information, contact Advanced Systems Products Inc., 1150 Ringwood Ct., San Jose, CA 95131; (408) 383-5709; fax (408) 383-9612; Internet: http://www.advansys.com.

The Fax Of Life—Seeking to widen the reach of electronics companies, Xpedite Systems has recently introduced its International Fax Service.

The service is designed to deliver the most up-to-date information to customers and prospects worldwide. Manufacturers, brokers, and distributors can send product availability, product announcements, and sale information to their targeted audience in a timely and inexpensive manner.

The International Fax Service works through the Xpedite System. Companies dial their international numbers from their fax machine which routes the call through Xpedite's worldwide fax network. No dialing procedures change.

Additionally, Xpedite offers users the option of broadcasting documents to multiple fax and/or Internet addresses. The user just faxes the document to Xpedite and they distribute the information.

Another feature of the service is the 24-hour access to stored documents. It's a Fax-On-Demand service that requires a touch-tone phone, but leads the user through voice prompts and menu options. Usage reports track the requested information.

For further details, contact Xpedite Systems Inc., 446 Highway 35, Eatontown, NJ 07724; (908) 389-3900, fax (908)-544-0407; Internet: http://www.xpedite.com.

IEEE Endorses Bill

It's a bird, it's a plane, it's a Super IRA! Recently, legislation has been introduced in both the House and Senate concerning opening up Individual Retirement Accounts (IRAs) to more Americans. The Institute of Electrical and Electronics Engineers, United States Activities (IEEE-USA) has endorsed the proposed bill.

According to the IEEE-USA career policy chair, Paul J. Kostek, most Americans' retirement income security depends on savings from Social Security, employer-sponsored pensions and personal savings. Given the current vultures circling Social Security, and the downsizing of business and government, personal savings are becoming the safety valve for many people, especially IEEE members.

Between the years of 1982 and 1986, personal savings held in IRAs skyrocketed from $5 billion to over $38 billion. But, when government regulation tightened income-eligibility requirements in 1987, that figure dropped to $14 billion.

The Roth-Breaux Savings and Investment Incentive Act looks to restore universal eligibility, allowing IRA holders to make tax-deductible contributions over a four-year period. There also will be the option to choose between contributing to a deductible IRA or to a new non-deductible IRA Plus Account.

Additionally, the IEEE-USA feels that the bill's provisions to repeal current restrictions on contributions by spouses of active pension-plan participants, and index annual IRA contribution limits for inflation are also positive moves for the Legislative branch.

Overall, the IEEE's worldwide membership comprises 315,000 electrical, electronics, and computer engineers. Of those members, 220,000 happen to live in the U.S..

For further information, contact the IEEE, 1828 L Street Northwest, Suite 1202, Washington, DC 20036-5104, (202) 785-0017, fax (202) 785-0835, Internet: http://www.ieee.org.—*DS*

EYE ON ISO 9000

Vectron Technologies Inc. has received ISO 9001 certification. Part of the Vectron International Group, the company is a supplier of frequency generation and control products. Contact Vectron Technologies Inc., 267 Lowell Rd., Hudson, NH 03051; (603) 598-0070; fax (603) 598-0075; Internet: http://www.vectron-vti.com.
CIRCLE 489

Endicott Research Group (ERG) Inc. was awarded ISO 9001 certification. The company designs and manufactures inverters and converters for various display backlighting technologies, including CCFT-backlit LCDs, electroluminescent (EL), VF (vacuum fluorescent), and gas plasmas for use in consumer, industrial, instrumentation, automotive, and commercial applications. Contact ERG Inc., 2601 Wayne St., Endicott, NY 13760; (607) 754-9187; fax (607) 754-9255; Internet: http://www.ergpower.com.
CIRCLE 485

G&H Technology Inc. has achieved ISO 9001 certification. The company designs and manufactures ultra-high-reliability components and subsystems for military, aerospace, undersea, and other mission-critical and industrial/commercial applications. Contact G&H Technology Inc., 750 W. Ventura Blvd., Camarillo, CA 93010; (805) 484-0543; fax (805) 987-5062.
CIRCLE 487

GTE's Government Systems and Worldwide Telecommunications Services units have achieved ISO 9001 registration. Both deliver telecommunications services to government, military, and commercial markets. Contact GTE, 77A St., Needham Heights, MA 02194.
CIRCLE 486

HOT PC PRODUCTS

The MP200-GPS is a rugged, CDPD/cellular 3-W mobile modem with a Trimble Global Positioning Satellite (GPS) receiver module. Aimed at the vertical market, Sierra Wireless' newest modem provides a GPS-based solution for automatic vehicle location.

Normally, vehicle installations of GSP-devices require an in-vehicle PC to connect the wireless modem to the GPS receiver. A major problem that installers run into is that most portable PC don't feature two serial ports. The MP200-GPS has the GPS receiver module integrated within the mobile modem, eliminating the external unit problem and bringing the serial interface requirement down to one.

The MP200 end of the unit uses either 19.2 kbits/s CDPD or 14.4 kbits/s circuit-switched cellular data and fax with ETC. It operates in temperatures that range from -30°C to 60°C, and can be stored in temperatures that sit in the -40°C to 80°C range.

The modem is packaged with Windows and Macintosh Watcher software. Watcher is Sierra Wireless' graphical user interface application for modem mode switching, monitoring, and operation.

The host interface is DB-9 with RS-232 signal levels capable of reaching 57.6 kbits/s. The antenna interface is a 50-Ω RF connector.

Inside the MP200-GPS lives a microcontroller, allowing the modem to operate without a mobile data terminal or PC. It also gives the unit the ability to function as a standalone tracking monitor. In this capacity, a host computer wirelessly programs the modem to report its position on a preset timeout.

For more information, contact Sierra Wireless Inc., #260-13151 Vanier Pl., Richmond, British Columbia, Canada V6V 2J2; (604) 231-1100; (604) 231-1109; Internet: http://www.sierrawireless.com.

Moving ever-closer to bringing truly fast modem technology to reality, Boca Research has begun testing Rockwell Semiconductor's K56Plus technology.

Boca is testing the end-to-end loop of the 56.6 kbits/s modem response on both client and central cites.

Boca's 56.6 kbits/s upgrade policy allows end-users of any brand name 28.8 or 33.6 kbits/s modem to upgrade to a Boca Research "interim" 56.6 kbits/s modem at a reduced price. This part of the policy only applies to modem owners who choose to deal with retail locations. For those individuals with Boca Research 33.6 kbits/s modems, an option to send the modem directly to the company exists. Once the company has received the modem, Boca will send out an "interim" 56.6 kbits/s modem. Additionally, as soon as an industry standard of an 56.6 kbits/s Boca Research modem exists, owners of "interim" modems are eligible for the 56.6 kbits/s product.

Contact Boca Research Inc., 1377 Clint Moore Rd., Boca Raton, FL 33487; (561) 997-6227; fax (561) 997-7189; Internet: http://www.bocaresearch.com.

The four-channel CompuSwitch is a lower-priced keyboard-video-mouse (KVM) switch from Raritan Computer.

The unit is capable of controlling up to four PCs, any combination of PS/2 and AT systems, from one keyboard, monitor, and mouse. To accomplish this control, CompuSwitch uses Raritan's proprietary emulation technology. The emulation technology dedicates individual keyboard and mouse emulators to each PC, enabling smooth booting and operation.

CompuSwitch supports hot-key commands, and features a user-adjustable Scan function. Also included on the switch are a front-panel selector and control buttons.

The switch chassis measures 1.75 in. The company also offers an optional 1U rack mount kit. CompuSwitch is priced at $595. Connector cables run $40 for 6.5 ft. and $50 for 13 ft.

For more information on the CompuSwitch, contact Raritan Computer Inc., 10-1 Ilene Court, Belle Mead, NJ 08502; (908) 874-4072 ; fax (908) 874-5274; Internet: http://www.raritan.com.

Behold!
We've turned plain old telephone wire into something magical.

Motorola's CopperGold™ ADSL Transceiver delivers the information highway of tomorrow on today's copper networks.

Motorola Semiconductor's CopperGold ADSL Transceiver is a highly integrated single chip solution, designed for high speed broadband access. This flexible DMT-based transceiver is engineered to achieve low cost, while maintaining high performance.

Designed to be compliant with category two* of the ANSI standard, the CopperGold Transceiver utilizes echo cancellation and trellis coding for a high performance, future-proof product capable of 8 Mbps simplex and up to 1 Mbps bi-directional.

Motorola is dedicated to providing systems solutions to create a one-stop-shop for your ADSL semiconductor needs. In addition to the CopperGold Transceiver, we offer the CopperGold Line Driver, microprocessors, software, and unparalleled customer support for applications such as Ethernet, ATM, TCP/IP, and ISDN.

COPPER GOLD

For technical information on the CopperGold family call 1-800-201-0293 and refer to ad #BB001 or visit our website at www.mot.com/adsl.

MOTOROLA

Semiconductor Products Sector

What you never thought possible.™

*Without 26 dBm transmit power boost

THE ENVELOPE, PLEASE

Receiving an award is always an honor, but it's especially rewarding when the recipient is recognized for a lifetime of contributions to a single field. In this case, the Standards Engineering Society (SES) awarded Stephen P. A. Marriott with its Honorary Life Fellow.

According to SES, the Awards Committee gives the Honorary Life Fellow to non-SES members for their "unusual professional distinction and outstanding accomplishment or special contribution to recognized associations or committees in the field of standardization." One past honoree was former U.S. president Herbert Hoover.

Marriott, currently the Secretary General of the European Committee for Electrotechnical Standardization (CENELEC), earned the award for his more than 20 years of work fields of the standards and standardization. In 1976, Marriott began his career in standardization with the British Standards Institution. During his tenure there, the also held the post of technical advisor to the Saudi Arabian Standards Organization.

The Standards Engineering Society can be contacted at 1706 Darst Ave., Dayton, OH 45403-3104; (513) 258-1955; fax (513) 258-0018.

Normally, a Motion Picture Arts and Sciences Academy award wouldn't make it into *QuickLook*, but one of this year's Technical Achievement Awards merited this mention. Kenneth Perlin, the director of the Center for Advanced Technology (CAT), associate professor of computer science, and director of the Media Research Laboratory at the Courant Institute of Mathematical Sciences at New York University (NYU), received the award for the development of his "Perlin Noise."

Generated mathematically by computer, Perlin Noise statistically creates a random texture, producing naturally-appearing textures on computer-generated surfaces for visual effects. The tool gives computer-effects designers the means to produce a gritty, or grainy shot. Another of Perlin's technologies, Turbulence, can be used with Perlin Noise to create animated atmospheric effects, such as mist, fire, marbling, smoke or oil slick patterns. Perlin's texture algorithms have been used in "The Lion King," "Jurassic Park," and "Independence Day," among other feature films.

Perlin received his Ph.D. in computer science from the Courant Institute at NYU, and his B.A. in theoretical mathematics from Harvard University.

For more information, contact New York University, 25 West Fourth St., New York, NY 10012-11990; (212) 998-6838.—*DS*

So Loud... You Can Hear a Pin Drop

AKM's New Audio HiDS Captures the Loudest Louds and the Quietest Quiets

A jet engine roars. A pin drops. Both are sounds, both total opposites. Each demand uncompromising high-fidelity.

HiDS
HIGH DYNAMIC
SOUND

Now, AKM a worldwide leader in the design and manufacture of professional audio ICs, covers both ends of the audio spectrum in a new line of the world's best audio ADCs, DACs, and CODECs.

These wide dynamic range, low distortion, single supply, dual-bit audio ICs are known as HiDS converters. Wherever the HiDS logo is seen, be assured of the highest performance and quality.

Our HiDS product line includes: 24-bit ADC at 113dB DR (AK5391) and it's companion the 24-bit DAC (AK4324), 96kHz 20-bit 105dB DR ADC (AK5352), 20-bit 100dB DR CODEC (AK4520), and the highest performance multimedia CODEC (AK4531).

With AKM's aggressive new product release schedule, tremendous fab capacity, and numerous audio patents, we are the audio supplier to look for now and in the future.

And just to ensure that your experience is soothing, AKM stands behind its products with world-class service and support.

AKM HiDS Audio ICs		
ADC	AK5350	Enhanced dual bit $\Delta\Sigma$ 2 channel ADC HighPerformance 20 bit, 100 dB DR
	AK5351	100dB 20-bit 2 channel ADC, 48kHz
	AK5352	105dB 20-bit 2 channel ADC, 96kHz
	AK5391	113dB 24-bit $\Delta\Sigma$ 2 channel ADC
DAC	AK4320	High Performance 20-bit 2 channel DAC
	AK4321	High Speed (96kHz sampling), 20-bit 2 channel DAC
	AK4323	20-bit 2 channel DAC with analog PLL
	AK4324	106dB 24-bit 2 channel DAC, 96kHz
CODEC	AK4520	20-bit 2 channel ADC & DAC
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IEEE International Symposium on Information Theory, June 29-July 4. Ulm, Germany. Contact Han Vinck, Institue of Experimental Mathematics, University of Essen, Ellernstr. 29, 45326 Essen, Germany; (49) 201 3206458; fax (49) 201 3206425.

Sixth IEEE International Fuzzy Systems Conference, June 30-July 5. Barcelona, Spain. Contact Ramon Lopez de Mantaras, IIIA-CSIC Campus U.A.B. 08193 Cerdanyola del Valles, Spain; (34) 3 580 95 70.

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IEEE Signal Processing Workshop on Higher Order Statistics, July 21-23. Banff Centre for Conferences, Banff, Alberta, Canada. Contact Keh-Shin Lii, Department of Statistics, University of California, Riverside, 900 University Ave., Riverside, CA 92521; (909) 787-3836; fax (909) 787-3286; e-mail: ksl@ucrstat.ucr.edu.

IEEE Nuclear & Space Radiation Effects Conference (NSREC '97), July 21-25. Snowmass Conference Center, Snowmass, CO. Contact Dennis B. Brown, Naval Research Laboratory, Code 6612, Washington, DC. 20375; (202) 767-5453; fax (202) 404-8076; e-mail: dbbrown@ccfnrl.nvy.mil.

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Sixth IEEE International Conference on Universal Personal Communications, Oct. 12-16. Hotel del Coronado, San Diego, CA. Contact Gail Weisman, IEEE Communications Society, 345 E. 47th St., New York, NY 10017; (212) 705-7018; fax (212) 705-7865; e-mail: g.weisman@ieee.org.

Sixth IEEE International Conference on Universal Personal Communications (ICUPC '97), October 13-15. Contact Tony Acampora, MC 0409, Bldg EBU1, UCSD, 9500 Gilman Drive, La Jolla, California 92093-0409; (619) 534-5438; (fax) (619) 534-2486; e-mail: acampora@ece.ucsd.edu.

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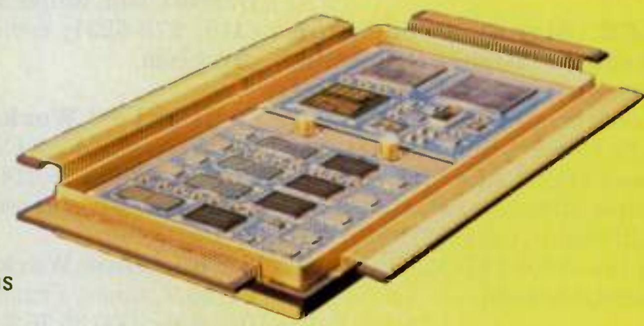

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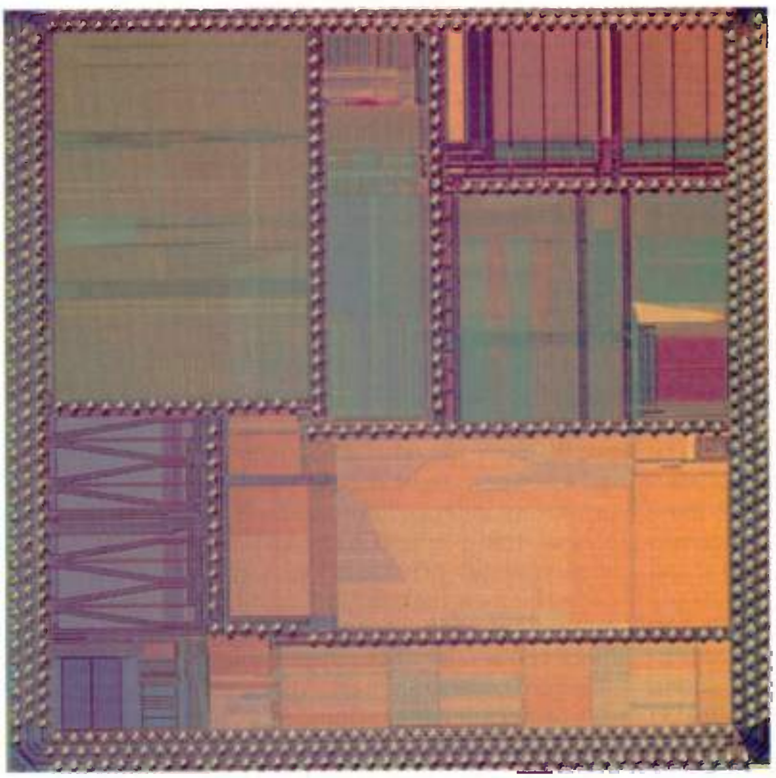
SPECIAL REPORT

In response to increasing multimedia performance demands, high-end CPUs are being enhanced with faster clock speeds, new instructions, and on-chip logic to accelerate the computations needed for multimedia algorithms. These enhanced CPUs will replace today's processors, which, with their clock speeds of up to 166 to 200 MHz, are just able to handle some low-to-moderate complexity multimedia tasks—softmodems, audio play-back, and even MPEG decompression.

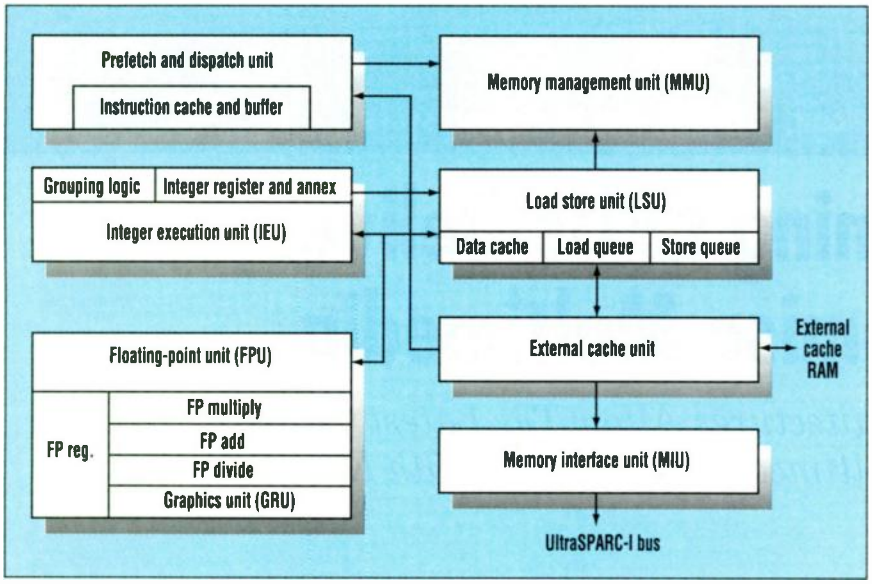


Art Courtesy: Sun Microsystems.

The need to enhance the multimedia processing capabilities of systems stems from the increasing use of multimedia in many applications. Thus, multimedia systems must now handle JPEG, MPEG, full video, videoconferencing, 3D graphics, data modem/ fax, and even speech-recognition functions. To address these needs in today's systems, additional coprocessor circuits or cards are often required to assist the host processor. That's because many multimedia functions require more compute cycles than the host CPU can deliver, especially when the host is expected to run all other applications at the same time. The additional logic results in a significant increase in system complexity and often ends up requiring multiple local memory spaces to hold intermediate data.

On the low-end of the CPU spectrum, chip architects have added DSP support blocks such as a hardware multiplier or multiplier-accumulators, speeding up single computations. CPUs that incorporate this simple enhancement include the Piccolo processor from Advanced RISC Machines, the StrongARM from Digital Equipment, the SH-DSP from Hitachi, and the M32R/D from Mitsubishi *(see "Multimedia without extensions," p. 70)*. Such CPUs are finding their way into web appliances such as dedicated browser hardware, set-top boxes, and portable computer systems.

But there is a second wave coming as the manufacturers of RISC and CISC processors used in desktop computers incorporate multimedia support hardware or software extensions. These capabilities will, in the long term, reduce the complexity of the system hardware and lower system cost. In the PC (x86) world, Intel has already released the enhanced Pentium processor that includes the 57 new MMX (multimedia extensions) instructions, and both Advanced Micro Devices and Cyrix are in the final stages of completing their enhanced CPUs that will offer code-compatible instructions.



1. Graphics support hardware and the visual instruction set are key additions to the 64-bit UltraSPARC I and II architecture from Sun Microelectronics. In the UltraSPARC I, the graphics support block was incorporated into the CPU's floating-point unit, while the VIS commands perform many of their operations in the 64-bit integer ALU.

Incorporating multimedia capabilities on the CPU is not a PC-original concept. It started with Hewlett-Packard (H-P), who embedded hardware enhancements in the ALU of one of its PA-RISC processors. Since that first effort, almost every other RISC manufacturer also has incorporated these enhancements—Digital Equipment, Silicon Graphics/MIPS Technologies, and Sun Microelectronics all have members in their processor families with multimedia support capabilities.

Aid For Multimedia

The extent of hardware and software support varies according to CPU type. For example, x86 CPUs include a minimal number of hardware changes, but 57 additional instructions. RISC CPUs include a few more hardware modifications to increase the computational acceleration and limit the number of new commands that must be added. In addition, the CPUs themselves have been enhanced, typically with a combination of clock-speed increases up to—and in some cases over—500 MHz. There also have been improvements in the microarchitecture—larger caches, better branch prediction, wider registers, and many other changes that all improve performance.

When H-P first modified its ALU, it did so to let the processor execute multiple byte-oriented operations in parallel. Such operations are a key part of the discrete cosine transform (DCT) algorithms used during MPEG image decoding.While a single CPU can perform one multiplication or addition per cycle, the HP-7100LC CPU can perform four operations per cycle. That increased throughput allows the processor to decode MPEG-1 data streams.

H-P has since evolved that scheme with its PA-RISC 8000 series CPUs and the multimedia acceleration extensions (MAX). The CPU's 64-bit ALU can be subdivided into as many as eight 8-bit sub-ALUs that can perform the byte additions and multiplications. Blocking the carries at the 8- or 16-bit boundaries in the ALU allows individual operations to be done in parallel, producing independent results. The only internal overhead in the ALU design is a slight increase in logic to decode the new instruction, and the equivalent of three AND gates to block the carries at the appropriate sub-word boundaries in the ALU.

For parallel operations, new instructions, Parallel Add and Parallel Multiply, were added to the CPU's instruction set. These operations have three variations, with each operation set to deal with overflows. The operations include modular arithmetic that discards the overflow, signed saturation (an overflow causes the result to be clipped to the largest or smallest signed integer in the result range), and unsigned saturation (an overflow causes the result to be clipped to the largest or smallest unsigned integer in the result range). And, to deal with multiplications by a constant, Parallel Shift Left and Add, and Parallel Shift Right and Add operations also were added to the instruction set. Just a minor change in the preshifter portion of the ALU was required to implement these operations.

One commonly performed operation, divide-by-two, also can be done very quickly by a new command—Parallel Average. This command adds two operands and then divides by two (right-shift by one bit). Also, when the ALU is subdivided, the same divide-by-two operation can be done in parallel on all subwords. The same, of course can done for multiplications—just shift in the other direction.

Additional changes to the CPU include a completely redesigned core with a 56-entry instruction reorder buffer, a capability to execute up to four instructions/cycle, dual load/store units, a 32-entry branch-target cache, branch-prediction hardware that includes a 356-entry branch history table, and static or dynamic prediction. On the core is a high-bandwidth system bus that can transfer up to 768 Mbytes/s and supports multiple outstanding memory requests. Overall, that gives the chip a throughput of 11.8 SPECint95 and 20.2 SPECfp95, when running at 180 MHz.

The latest version of the processor, the PA-8200, further improves performance—it can clock at 220 MHz and can deliver a throughput of 15.5 SPECint95 and 25 SPECfp95. That allows the chip to decode multiple MPEG-2 data streams simultaneously and perform other tasks. Planned for 1998 release is the PA-8500, which will operate at even higher clock speeds with more improvements to the microarchitecture.

Solar Power

Designers at Sun Microelectronics have gone a bit further than H-P. They've incorporated what they call the visual instruction set (VIS) into the basic architecture of Sun's UltraSPARC 64-bit superscalar processor unveiled in 1994. In the UltraSPARC I processor,

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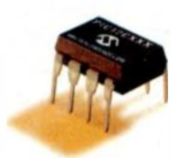

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the company added on-chip graphics and imaging support hardware and the VIS commands *(Fig. 1)*. The support allows the processor to decompress video streams and manipulate video information with broadcast resolution in real time. That allows system designers to eliminate a dedicated video processor that might otherwise be needed.

The 30 VIS commands drastically reduce the number of clock cycles required for complex graphics or imaging operations—in many cases, the instructions can execute in a single cycle what might take tens to hundreds of clock cycles to perform with standard instructions. The three-operand instructions break down into several groups—pixel format and conversion, image processing, real-time video compression, and data-transfer and animation speed-up. They execute in the chip's 32-register floating-point/graphics unit.

Pixel operations allow the processor to directly operate on pixel data, which can be stored as 8- or 16-bit integers. The Pixel Expand command, for instance, converts four 8-bit integers to four 16-bit integers and then stores the result as one 64-bit word—all with one instruction. Pixel Pack does the opposite—it converts four 16-bit or two 32-bit values to four 8-bit or two 16-bit values and also stores the result as one 64-bit word while using a single instruction. The efficiency of these commands reduces the number of instruction cycles by a factor of 34, greatly improving compute efficiency.

One of the more powerful operations, Pixel Distance, compares eight

Multimedia Without Extensions

Without software or hardware extensions to directly handle multimedia algorithms, microprocessors are often not able to execute the complex and the overwhelming number of computations (needed by algorithms for JPEG or MPEG decoding) and still have bandwidth available to handle the system control or data-processing tasks. The minimal functionality required on the CPU chip to help speed computations would be a block such as a single-cycle multiplier and an accumulator, so that efficient multiply-and-accumulate (MAC) operations can be done. Such functions are a key part of most multimedia algorithms for image and audio processing.

Lack of a dedicated MAC capability means that the CPU must perform equivalent operations using multicycle add, shift, and other instructions. Such operations can certainly be performed.But with CPUs that execute at clock speeds of less than 120 or even 166 MHz, there is no bandwidth left over to perform other tasks in parallel. Consequently, as a first step, several CPU suppliers, especially those companies that want to support multimedia-like functions for embedded applications—such as in personal digital assistants (PDAs), network appliances, and other performance- and cost-sensitive applications are moving to higher CPU clock speeds and packing multipliers, full MAC capabilities, or even dedicated DSP blocks onto the CPU chips. These are the first steps that can provide performance boosts at minimal cost.

For instance, both the StrongARM chip developed by Digital Equipment and the M32R/D combination RISC engine and 16-Mbit DRAM from Mitsubishi incorporate hardware multiplier support to handle the integer computations that might typically be needed for handwriting recognition, speech processing, and graphics operations. At the other end of the spectrum, processors such as the Piccolo developed by Advanced RISC Machines, and the SH-DSP created by Hitachi, incorporate full DSP engines on the chip in addition to the 32-bit RISC CPUs.

The StrongARM chip is a high-performance version of the ARM processor that is implemented by DEC with a 0.2-µm process. The tight process rules and good architectural implementation allow the StrongARM to operate at clock rates of 150 MHz—triple to quadruple that of the best performing ARM processors. The sheer speed of the StrongARM, coupled with the MAC capability, allows the chip to perform well in PDA applications such as the recently unveiled Newton MessagePad 2000 from Apple Computer.

Also finding a home in PDA-like applications is the M32R/D with its on-chip MAC. It can readily implement functions such as a softmodem, or perform tasks like handwriting recognition. One added bonus on this chip is that Mitsubishi offers substantial amounts of additional storage capability; it packs up to 16 Mbits of DRAM and several kbits of static-RAM-based cache on the same chip as the CPU, allowing the processor chip to hold large programs or arrays of data without requiring off-chip memory. A wide internal DRAM-to-cache/CPU interface allows the rapid movement of large blocks of data.

More complete DSP support, such as included on the SH-DSP or the Piccolo chips, provides designers with a 32-bit RISC engine and a 16-bit fixed-point DSP core, all on a single chip. The ARM7TDSP can deliver 40 MIPS of DSP computational throughput in addition to about 25 MIPS of standard ARM CPU throughput in the first chip implementation being done with 0.6-µm design rules. When shifted to a 0.35-µm process, the performance can be upped to 66 DSP MIPS and close to 50 MIPS for the ARM core.

The SH-DSP chip also provides high throughput, delivering 60 MIPS on the SH CPU core and 120 megaoperations/s on the DSP engine. Depending on the application, the chip can serve nicely as a standalone 32-bit SH-family CPU, or as a relatively powerful 16-bit integer DSP chip. A typical application for a chip like the SH-DSP is in a GSM telephone handset, where the processor can perform all the handset and call-management functions, while the DSP core would handle all the speech processing.

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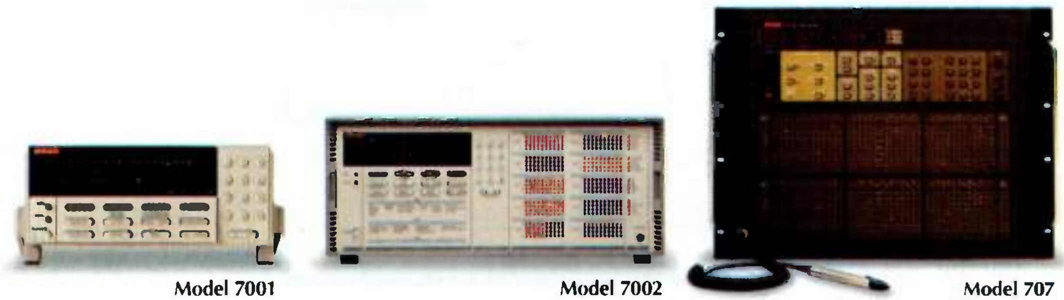

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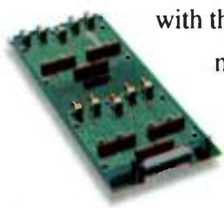

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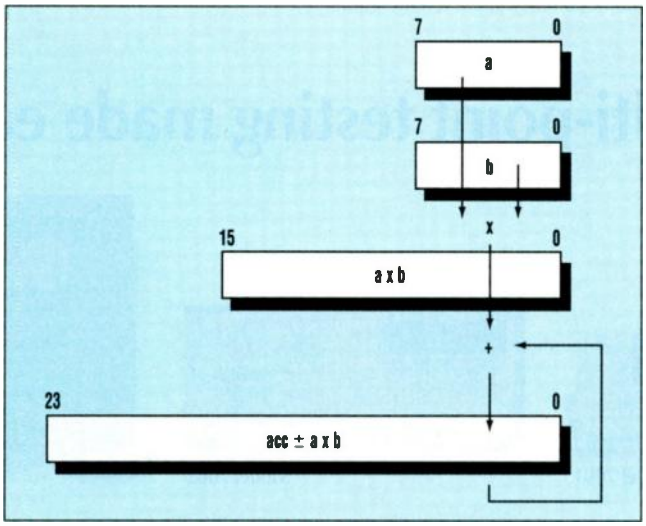
• Main display	VFD	VFD/LED	LED	LED
• Memory locations	100	500	100	100

pairs of 8-bit values simultaneously, using a sum of absolute values of differences. This operation provides a 20-to-50X performance improvement for the inner-loop computations in MPEG compression algorithms and is useful in motion-estimation, cross-correlation, character-recognition, and pattern-matching applications. Matrix computations, such as performed in volumetric calculations and 3D image manipulation, can be done quickly thanks to the Array instruction, which loads the cache with cubes of data, rather than lines of data. This capability greatly speeds up the ability of MRI scans to take arbitrary slices of a volume in real time.

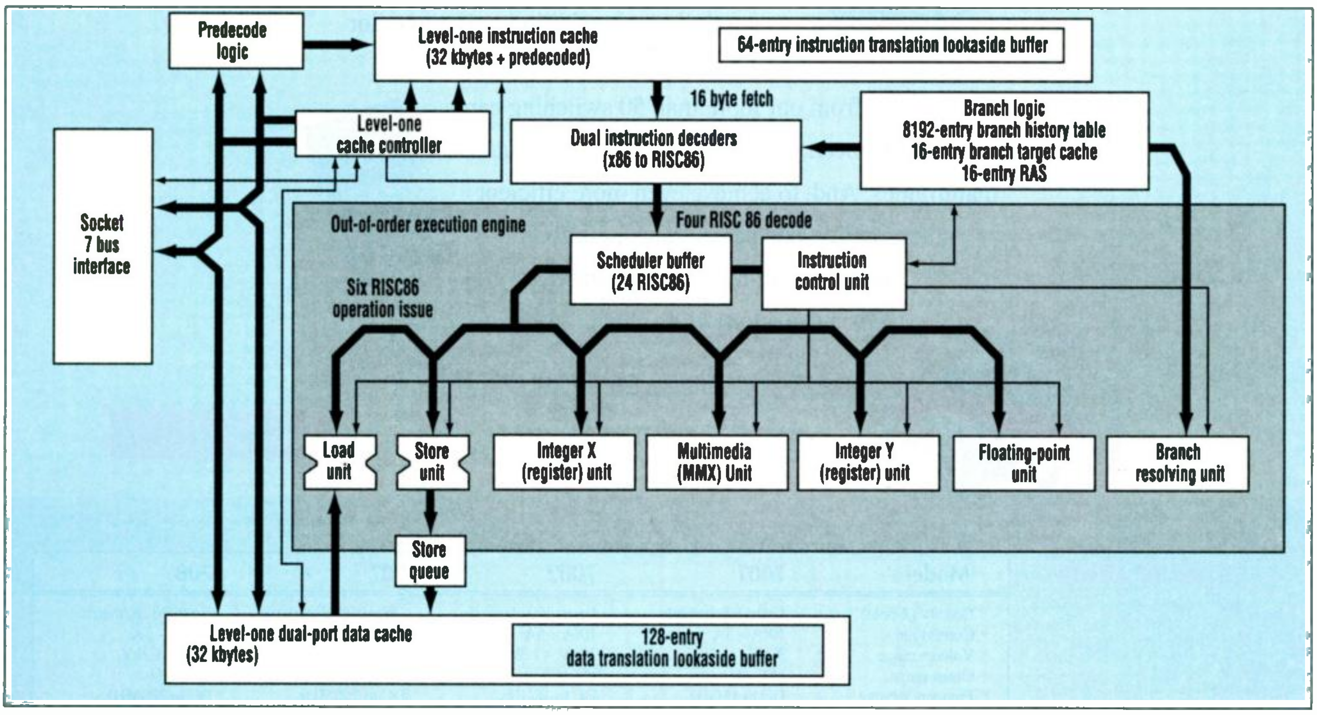


2. In one 8-bit slice of the MIPS V datapath from MIPS Technologies, two 8-bit integer values can be multiplied to form a 16-bit product that can then be accumulated in a 24-bit segment of the 192-bit accumulator. Thus, one slice can accumulate up to 256 8-by-8-bit or 65,536 16-by-16-bit multiplies.

Although the VIS commands were developed with multimedia applications in mind, the instructions are useful in many other applications, as Sun's designers found out when customers began putting the commands to work. In cryptography, the bit-matrix multiplication operations can be accelerated by 11 to 14 times; in genome sequencing, the sequence-comparison algorithm can execute twice as fast; network data transfers were accelerated thanks to the Block-Load-and-Store instructions that can transfer 64-byte blocks of data without displacing the data in the caches (cache bypass); and in printers, a six-fold speed-up can be achieved in look-up table accesses for color conversion.

As with any new instruction set, the hardest task is to develop the programs that take full advantage of the commands. To make that task easier, Sun engineers created mediaLib, a library of over 400 low-level C-language modules of commonly used functions employed in multimedia algorithms. The modules will be available in both C and VIS-accelerated C forms, providing full CPU independence. When the VIS commands are available, the programmer can exploit the accelerated performance by linking in the VIS-accelerated modules.

Some examples of what's available in mediaLib include imaging routines (data format conversion, spatial operations, image generation and copying, arithmetic and logical operations, color-space conversion, etc.), linear algebra, audio and video routines (digital filtering, signal generation, and the basic elements used in JPEG and MPEG processing), and graphics operations (2D and 3D primitives, rendering, and texturing). The modules



3. Maintaining the Socket 7 compatibility, the K6 processor from Advanced Micro Devices can execute all the MMX operation codes that Intel incorporated into its just-released P55C version of the Pentium. Dual 32-kbyte caches and RISC86 sub instructions allow the K6 to deliver throughputs better than the 200-MHz P55C without having to run at 200 MHz.

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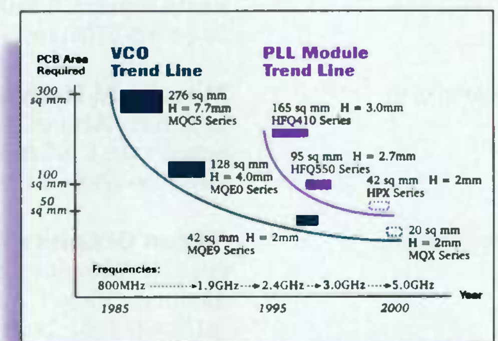

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work on a wide range of computing environments. Sun is currently working with industry partners, including Apple Computer, to ensure that optimally-tuned versions are available on other platforms.

In addition to the VIS commands, the UltraSPARC-I packs many features that give it its high throughput—a wide instruction fetch (128 bits per fetch), dynamic branch prediction, a nine-stage pipeline that issues up to four instructions per cycle, and a 12-entry prefetch buffer that decouples the instruction prefetching from instruction dispatch, thus preventing pipeline stalls.

Speedy Clocking

More recently, Sun's designers updated the processor with the release of the UltraSPARC II processor, detailed at last month's International Solid-State Circuits Conference (ISSCC). This latest version will clock at 330 MHz and has numerous enhancements to the microarchitecture that improve instruction efficiency and the execution time of multimedia algorithms.

Architectural enhancements are the key to performance improvements in the Alpha processor family from DEC as well. the latest version of the chip, unveiled at last year's Microprocessor Forum, the Alpha 21264, not only operates at a clock frequency of over 500 MHz, but incorporates what the company calls its Motion Video Instructions. These MV commands allow the Alpha processor to perform real-time MPEG-2 encoding of video data in addition to the expected decoding capabilities. This is the first general-purpose CPU that can perform real-time MPEG-2 encoding. Previously, such a capability required multiple, dedicated image processing chips that execute several gigaoperations per second.

The MV instructions on the Alpha were jointly defined by design teams at DEC and Mitsubishi Electric Corp., Itami, Japan. A low-cost version of the Alpha processor, detailed at the ISSCC by Mitsubishi, also incorporates the 13 MV instructions optimized for MPEG-2 encoding and decoding and can operate at clock speeds of up to 550 MHz. The 21164PC packs only 3.5 million transistors and delivers a throughput of 15 SPECint95 and 20 SPECfp95 while consuming about 35 W from a 2.5-V supply when clocked at 500 MHz. The MV commands combined with the overall high throughput of the CPU allows the chip to deliver 30-frame/s digital versatile disk (DVD) playback with stereo-quality audio without any other support circuits, or to perform 30 frame/s videoconferencing.

The instruction extensions include operations for motion-video estimation, which provide an order-of-magnitude improvement in computational throughput. There are three single-instruction/multiple-data instruction classes—Pixel Error, Max/Min, and Pack/Unpack—that allow the CPU to perform multiple sub-word operations

Manufacturers Listing

The following is a listing of manufacturers that appeared in the main text of this article. Note that this does not represent a complete list of all multimedia device manufacturers.

Advanced Micro Devices Inc.
One AMD Place, P.O. Box 3453
Sunnyvale, CA 94088-9968
(408) 749-5703; Internet: http://www.amd.com

Advanced RISC Machines Ltd.
985 University Ave., Ste. 5
Los Gatos, CA 95030
(408) 399-5195; Internet: http://www.arm.com

Cyrix Corp.
P.O. Box 853917
Richardson, TX 75085-3917
(214) 968-8388; Internet: http://www.cyrix.com

Digital Equipment Corp.
77 Reed Rd.
Hudson, MA 01749
(508) 628-4760;
Internet: http://www.digital.com/info/semiconductor

Hewlett Packard Co.
19410 Homestead Rd.
Cupertino, CA 95014-9810
(408) 447-4747; Internet: http://www.hp.com

Hitachi America, Semiconductor Div.
2000 Sierra Point Pkwy.
Brisbane, CA 94005-1835
(415) 589-8300; Internet: http://www.hitachisemi.com

Intel Corp.
2200 Mission College Blvd.
Santa Clara, CA 95052-8119
(408) 765-7766; Internet: http://www.intel.com

Mitsubishi Electronics America Inc.
1050 East Arques Ave.
Sunnyvale, CA 94086
(408) 730-5900; Internet: http://www.melco.com

Silicon Graphics Inc., MIPS Technology Div.
2011 N. Shoreline Blvd., P.O. Box 7311
Mountain View, CA 94039-1100
(415) 390-4134; Internet: http://www.mips.com

Sun Microelectronics Inc.
2550 Garcia Ave.
Mountain View, CA 94043-1100
(408) 774-8545; Internet: http://www.sun.com

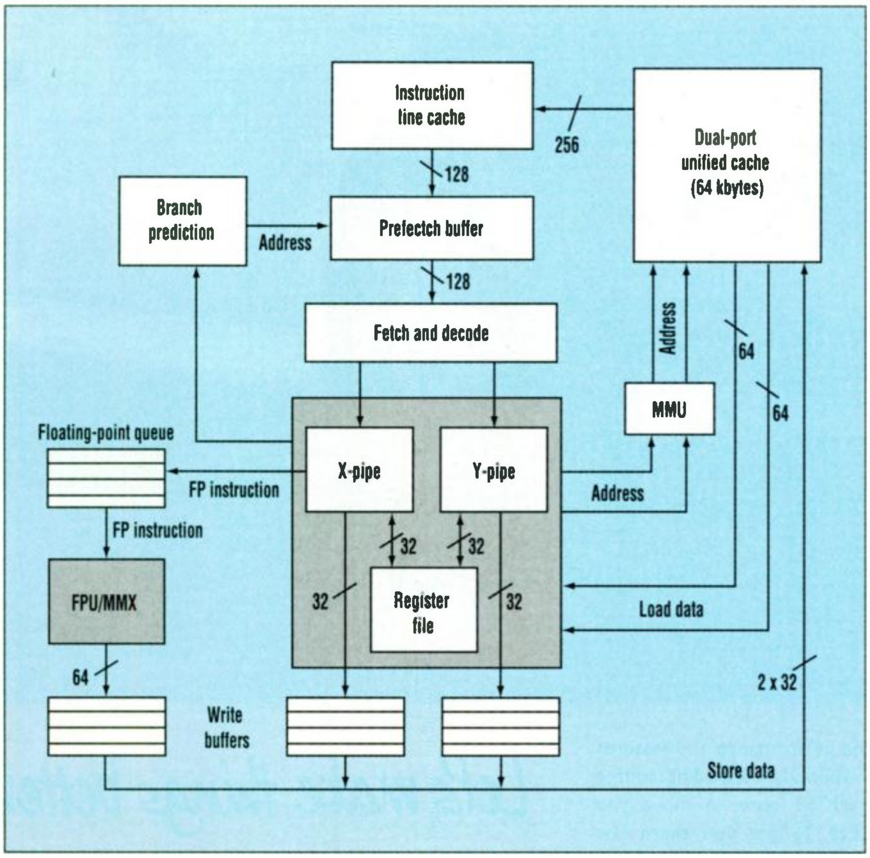
in parallel. The Pixel-Error operation, for example, computes the sum of the absolute differences of groups of eight bytes in just two CPU cycles. Vectorized Max/Min operations are used to clamp the values of groups of eight bytes or four 16-bit words with a single instruction. And the Pack/Unpack commands are used to expand or compact the data width on vectors of bytes or words.

MV instructions are fully pipelined and all execute with a two-cycle latency. Since the instructions are fully-integrated into the integer unit of the processor, operands are received directly from the other integer unit outputs or the integer register file, The integer unit can then bypass the results directly into other integer instructions.

The high-end 21264 version of the Alpha processor achieves its high level of performance thanks to the 15.2-million transistors packed onto the chip with six levels of metal interconnections. The resulting CPU performs four-way out-of-order instruction execution and can issue up to four integer instructions and two floating-point operations every cycle. Dual 64-kbyte on-chip caches hold the instructions data; and both caches are two-way set-associative.

The system interface to the chip can sustain a total data-transfer bandwidth of over 2 Gbytes/s with both the 64-bit system and 128-bit cache buses active. These features result in a chip that delivers an overall throughput estimated to be better than 30 SPECint95 and 50 SPECfp95. A further improvement on the process side described at the ISSCC allowed DEC to further up the clock frequency to 600 MHz. That translates to improved SPEC ratings of 40 SPECint95 and 60 SPECfp95—the highest numbers to date for a RISC processor.

The latest company to enhance its RISC architecture with multimedia support, Silicon Graphics, through its technology subsidiary, MIPS Technology, unveiled the MIPS V instruction set that includes the MIPS digital media extensions (MDMX). One key addition to the general instruction set is a Paired Single-Data Type, which doubles the performance of floating-point applications by processing two 32-bit operands in parallel in the CPU's 64-bit data path.



4. A unified dual-port 64-kbyte cache on Cyrix's M2 processor provides designers with a different architectural implementation that still lets Cyrix achieve P55C or better performance. Designers at the company incorporated the MMX capability into the floating-point block on their chip.

Prepped For 3D

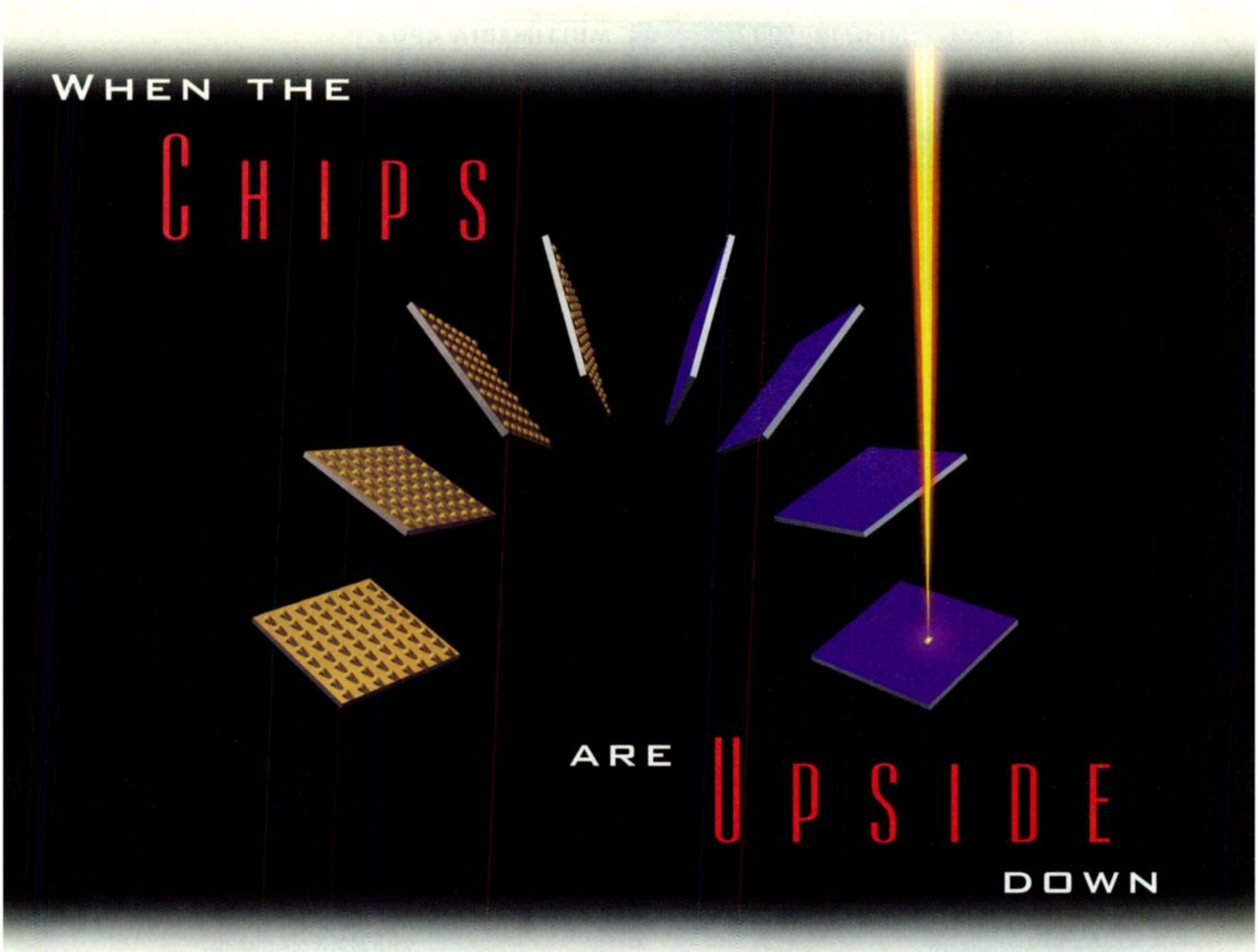
Although the company has not yet released actual details of the chip that's under design by its silicon partners, it estimates it will execute the multimedia signal processing algorithms at close to twice the speed of most of the other SIMD implementations. The MIPS V commands will deliver significant performance increases for 3D geometry processing, allowing the CPU to accelerate VRML applications, including those based on Cosmo Open GL and other visual environments.

The additional MDMX instructions take advantage of a dedicated, extra-wide 192-bit accumulator. This gives the processor true on-chip high-performance DSP capabilities, allowing it to execute algorithms for real-time video decompression, digital audio surround sound (Dolby AC-3 decoding), and fax/modem functions. For register space, the MDMX extensions share the 32 64-bit floating-point registers and eight single-bit condition codes.

The 64-bit registers can be subdivided into eight 8-bit integers or four 16-bit integers that can be processed in parallel with the SIMD MDMX commands. The wide accumulator can hold eight unsigned 24-bit results or four signed 48-bit integers, permitting multiply-and-accumulate computations to retain maximum precision until the very end *(Fig. 2)*. In a single slice of the ALU that performs an 8-bit operation, two 8-bit integer values are multiplied and the result accumulated in a 24-bit sub register. As a result, in a DCT or other algorithm, the registers can accumulate the results of 256 8-bit-by-8-bit multiplications, or 65,536 16-by-16-bit multiplies with only a single shift or round error at the end.

Mirror, Mirror

For the last 12 months, Intel has been professing the benefits of its MMX instruction set extensions—57 new commands and four new data types targeted at supporting multimedia applications. The first of the CPUs



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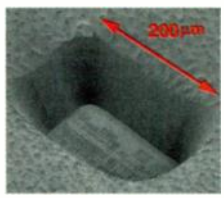

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KEY FEATURES OF MMX-CAPABLE CPUs

Feature/CPU Type	Intel Pentium	Intel Klamath	AMD K6	Cyrix M2
Interface	Pentium	P6+ L2 cache bus	Pentium	Pentium
MMX	Yes	Yes	Yes	Yes
L1 cache I/D	16k/16k	16k/16k	32k/32k	64k unified
L2 cache	Not on chip	256k/512k in module	Not on chip	Not on chip
L2 cache bus	None	1/2 CPU speed	None	None
Basic pipeline	6 stages	ND	6 stages	7 stages
Out of order	No	Yes	Yes	Limited
Peak decode rate	2 instructions	ND	2 instructions	2 instructions
BTB	256 entry	ND	8192 BHT	512 entry
TLB I/D	32/64 entry	ND	128/64 entry	16 entry L1 384 entry L2
Return stack	4 entry	ND	16 entry	8 entry
Write buffer	4 entry	ND	ND	8 entry
Core voltage	2.8 V (2.5 V mobile)	2.8 V	2.9 V	2.5 V
Typical power	5.5 to 7.3 W	ND	ND	ND
Maximum power	9.5 to 15.7 W	ND	ND	ND
IC process	0.28-µm CMOS 4-level metal	0.28-µm CMOS 4-level metal	0.35-µm CMOS 5-level metal	0.35-µm CMOS 5-level metal
Transistors	4.5 million	7.5 million	8.8 million	6 million
Die size	140 mm^2	203 mm^2	162 mm2	197 mm^2
Normalized performance (non-MMX Pentium=1)	1.1	1.35	1.45	1.3

BHT = branch history table; BTB = branch target buffer; TLB = translation lookaside buffer; I/D instruction/data; ND = not disclosed.

This is a simplified version of a table that appeared in the Dec. 30, 1996 issue of the Microprocessor Report, published by MicroDesign Resources.

to incorporate the MMX commands, known by its internal name the P55C, was released this past January, and provides system designers with the first new x86 instructions in almost a decade. But Intel won't be alone for long—both Advanced Micro Devices and Cyrix are close to delivering samples of their respective MMX-capable CPUs *(see the table)*.

In addition to including MMX in the P55C, Intel plans to incorporate the MMX commands in a Pentium Pro CPU code-named Klamath, scheduled for release later this year. Intel expects these chips to eventually replace all non-MMX CPU production within the next few years. Intel even expects to release a family of OverDrive processors that incorporate the MMX commands, allowing users with older systems to upgrade with minimal cost impact.

Although Intel expects the P55C to execute the multimedia algorithms 10 to 20% faster than a Pentium without the MMX commands, the MMX commands are not the only reason the 200-MHz P55C delivers outstanding performance. To boost basic CPU performance, the on-chip cache size also was doubled—the chip now packs 16 kbytes each of data and instruction cache. It also includes improved the branch prediction, an enhanced pipeline, and deeper write buffers.

To maintain 100% software compatibility with previous Pentium and older x86 processors, Intel's designers came up with a scheme that gives the MMX commands their own registers, and shadows those registers in the same address space as the floating-point unit's register file. As a result, programmers have an either-or situation: Either the FP unit goes inactive, or the MMX commands are not used when floating-point computations are needed. This situation does cause some system overheads, since when one operation is interrupted, there are a number of cycles of overhead operations to store the current state and then load in the new state, and finally restore the original state.

The 57 new MMX commands can be loosely grouped into six categories—Data Transfer, Pack and Unpack; Arithmetic; Shift; Logical; Compare; and miscellaneous—with many of the instructions capable of executing multiple operations on data (SIMD style). One integer and one MMX instruction can be issued simultaneously (with a few restrictions), and as long as MMX instructions do not use the same function units, two MMX commands could also be issued simultaneously. At its peak, the P55C could calculate up to 16 results (of one byte each) per cycle. Floating-point instructions cannot be paired with an MMX or integer instruction.

All MMX commands have a single-cycle latency except for the multiply and multiply-add commands, which have a three-cycle latency. The software model for MMX gives programmers eight new registers along with the new instructions. Those registers are actually mapped onto the floating-point registers, and that mapping locks out the possibility of doing any floating-point operations in parallel with MMX operations.

When a multitasking operating system or other application executes an FSAVE instruction, the contents of the MMX registers are saved in place of the floating-point registers if the MMX instructions are in use. On rare occasions, there might be a problem with the inability of the CPU to perform floating-point operations interspersed with MMX commands without any significant overhead. Fortunately, in most x86 application code, floating-point operations are rare. Therefore, Intel's designers felt that the occasional state-save overhead encountered when switching out of the MMX mode and switching back again would not greatly impact processor throughput.

Although demonstrations show that the impact is minimal on some applications, the overheads must be reduced to provide a better margin for the application software. Future versions of the processors will have more efficient state changes to reduce such overhead challenges.

Both Advanced Micro Devices and Cyrix have developed enhanced ver-

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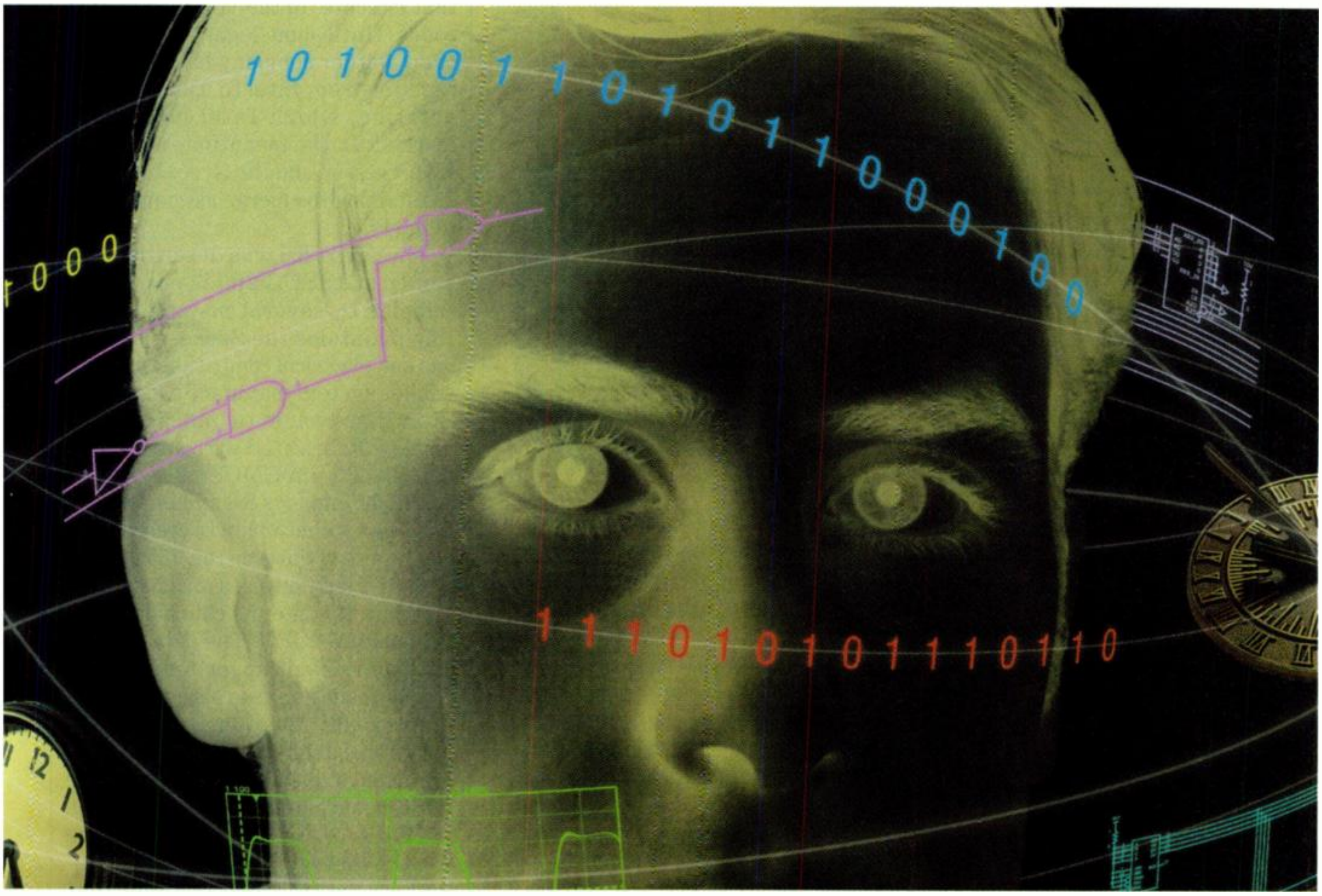

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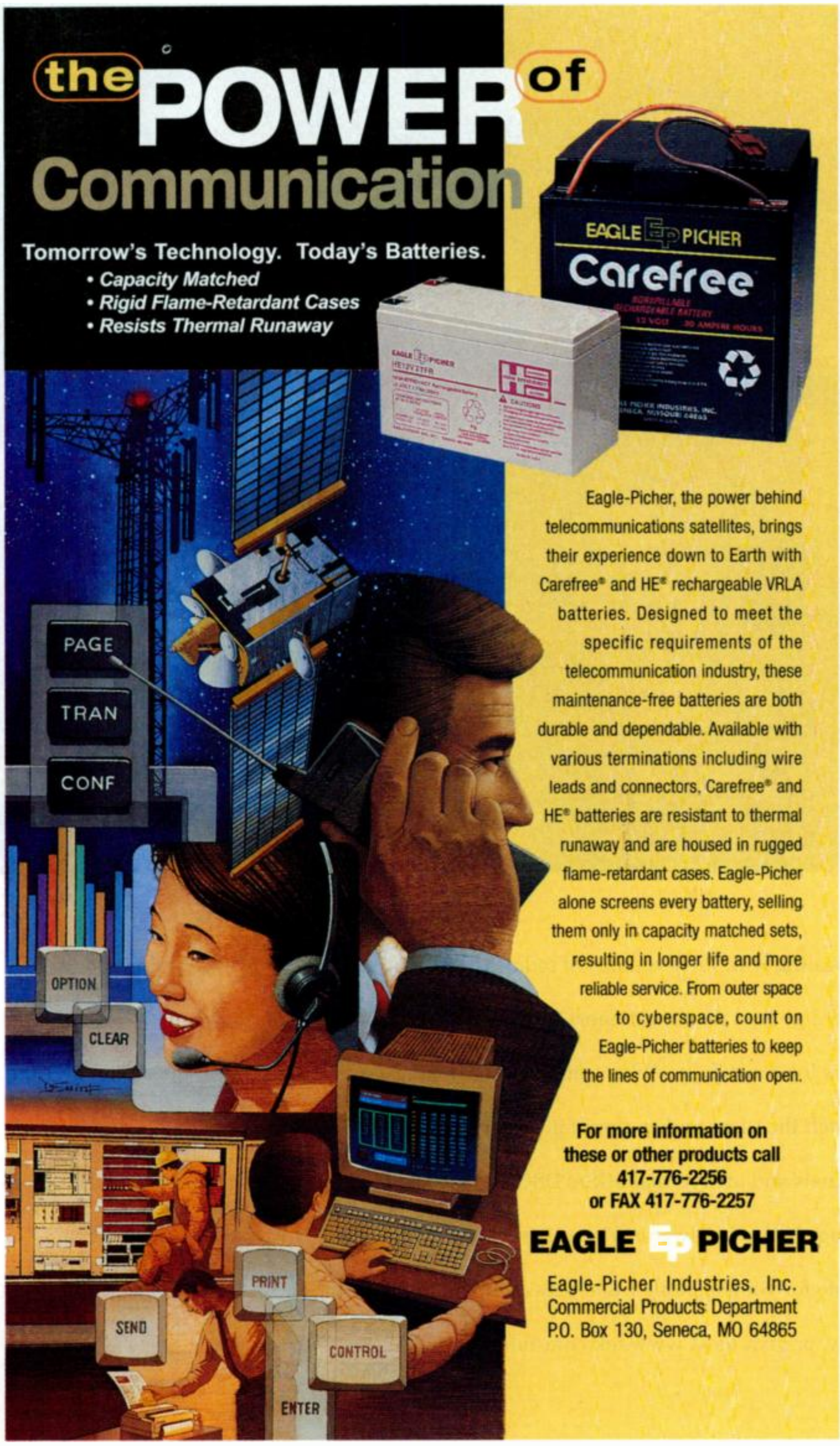

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sions of the their respective Pentium-compatible CPUs with commands that execute all the MMX operation codes. Until some legal wrangling is over, neither company has an official sanction from Intel to use the MMX notation, which Intel has trademarked. In the meantime, the AMD K6 processor, and the Cyrix M2 CPUs are starting to emerge as competitors to the P55C.

The AMD K6 was described last month at ISSCC and is now being sampled by several customers. The chip maintains the Socket 7 system bus and electrical compatibility, which will let system manufacturers bring their hardware to market very quickly. Fabricated with a five-level metal, 0.35-µm CMOS process, the processor employs 8.8 million transistors to pack dual 32-kbyte caches (double the size of those on the P55C), both with 32-byte line sizes and 2-way set associativity onto the chip along with the enhanced CPU. The data cache is dual ported and supports simultaneous loads and stores in a single cycle.

Internally, the K6 microarchitecture is an extension of the previous K5 architecture, which employs the RISC86 sub-instructions to execute x86 CISC operations *(Fig. 3)*. In the K6, the instruction control unit includes a centralized scheduler that buffers up to 24 of the RISC86 operations, performs full register renaming for the six-issue out-of-order execution engine, and issues up to six RISC86 instructions and performs in-order retirement.

Building on its 6x86 core, Cyrix has enhanced the core to create the M2, a chip that will execute the MMX instruction codes. Like the K6, the M2 will contain 64 kbytes of cache. However, unlike the AMD part, designers at Cyrix opted to use a unified dual-ported cache rather than separate instruction and data caches *(Fig. 4)*. Additional enhancements over the 6x86 CPU include an improved translation look-aside buffer that uses a two-level approach—a 16-entry first-level and a 384-entry second level.

HOW VALUABLE	CIRCLE
HIGHLY	544
MODERATELY	545
SLIGHTLY	546

CONFERENCE REVIEW

Hot Systems, Cool Software In Compcon '97 Spotlight

Speedy Microprocessors, Java Software, And Multimedia Took Center Stage At Compcon'97.

Dave Bursky

Touting a theme of Hot Systems/Cool Software, the 1997 edition of the IEEE Compcon conference delivered an array of technical sessions, plenary speakers and tutorials covering the latest high-performance microprocessors, advanced multimedia technology, new operating systems, and advanced networking topics such as electronic commerce, Java, and wireless technology. Held from Feb. 23 to 26 at the Hilton Hotel and Towers in San Jose, Calif, the conference provided some intereseting historical perspective on advances in digital computing as seen by one of the plenary speakers, Federico Faggin, CEO of Synaptics Inc., San Jose, Calif., and the founder of Zilog (and responsible for the development of the Z80 microprocessor).

Additional plenary presentations by Prof. Hector Garcia-Molina of Stanford University, Stanford, Calif. examined the concepts of meta-searches across the Internet. A trio of plenary speakers—David Gifford of the Massachusetts Institute of Technology, Cambridge, Mass., Ted Laliotis of Laliotis and Associates, Los Altos, Calif., and Dave Nagel of AT&T Labs, Basking Ridge, N.J.—each discussed different aspects of electronic commerce. And Professor Randy Katz, of the University of California at Berkeley, followed with an examination of the future of wireless technology.

In microprocessors, the sessions detailed a host of the latest high-performance processors from the leading manufacturers: The PA-8500 from Hewlett-Packard, Cupertino, Calif, the next-generation PowerPC microprocessors by Motorola and IBM, both in Austin, Texas, advanced Pentium processors with the MMX enhancements from Intel, Santa Clara, Calif, and the next-generation Alpha processors from Digital Equipment, Hudson, Mass., and Mitsubishi Electric Itami, Japan.

Multimedia-related sessions examined the developments in 3D graphics technology from 3Dlabs Inc., San Jose, Calif., and Intergraph Corp., Huntsville, Ala.; digital versatile disk (DVD) advances from Matsushita Electric Co. Ltd., Osaka, Japan, Pioneer Corp., and Toshiba Corp., Tokyo, Japan. Related to multimedia, a session on imaging over the Internet provided an overview of digital photography and digital cameras from Live Picture Inc., Soquel, Calif., and Hewlett-Packard Labs, Palo Alto, Calif. A session on image quality had papers by Hewlett-Packard and Stanford University on video/color image quality metrics.

The Java Brew

Java-related sessions also took center stage this year, with session topics including Optimization and Benchmarking for Java, Java Enabling Compilers and Translators, and a session on Internet Security that included several discussions of security architectures for Java. The optimization session presentations from Motorola, Sun Microelectronics, Mountain View, Calif., and Arizona State University, Phoenix, detailed Java optimizations for embedded environments, Java performance and benchmarking, and bytecode optimizations, respectively. The compiler session included presentations by IBM Corp., Cygnus, the University of Rochester, and SunSoft that examine NetRexx, an alternative to the Java language, a GCC-based Java implementation, Briki: A flexible Java compiler, and Java math libraries, respectively. And in the Internet Security session, both JavaSoft and the University of California at Berkeley covered security architectural directions aspects of Java, while a third presentation in the session from Microsoft Corp., Redmond, Wash., discussed the company's Internet Security Framework.

Database-related technology also received a great deal of attention at the conference. A full session was devoted to Object-Relational Database Systems and contained presentations on the evolution of DB2 as an Object-Oriented Database System by IBM Corp., San Jose, Calif.; the new Oracle universal server technology, Oracle Corp., Redwood Shores, Calif.; and DataBlade Snap-Ins for Informix-Universal Server, by Informix Software Inc., Oakland, Calif.

Tying many of the database, network, and CPU technologies together, a session on Network Computing examined a broad range of topics including Agent Technology from IBM; the use of Acorn Technology for Web Computing by Acorn Computers Ltd., Cambridge, England; The Information Appliance Revolution by Diba Inc., Menlo Park, Calif., A View of the Convergence of Services and Devices by the Philips Multimedia Center, Palo Alto, Calif., and a look at the P200 Telephone Client, also from Philips.

Copies of the conference proceedings for Compcon'97 can be ordered through the Compcon home page at http://www.compcon.org, or through the IEEE. For a copy of the final program listing all the papers, contact Dave Hunt at (510) 422-2199; fax (510) 422-2495: e-mail: compcon@lbl.gov.

How Valuable	Circle
Highly	528
Moderately	529
Slightly	530

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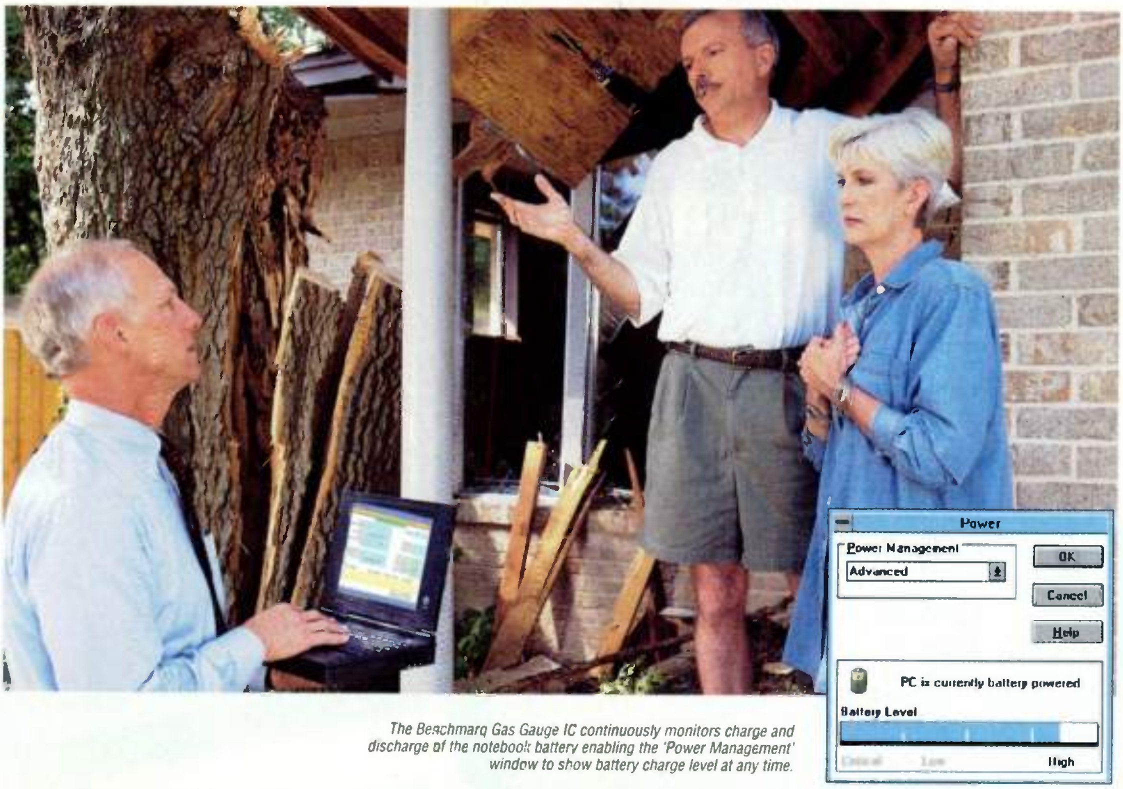

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bq2011/J	Gas Gauge IC for Power Tools	NiMH and NiCd	16/0.150" SOIC
bq2012	Gas Gauge IC	NiMH and NiCd	16/0.150" SOIC
bq2014	Gas Gauge IC with Ext. Charge Control	NiMH, NiCd and Li-Ion	16/0.150" SOIC
bq2050	Power Gauge™ IC	Li-Ion	16/0.150" SOIC
bq2091	SMBus v.95 Gas Gauge IC	NiMH, NiCd and Li-Ion	16/0.150" SOIC

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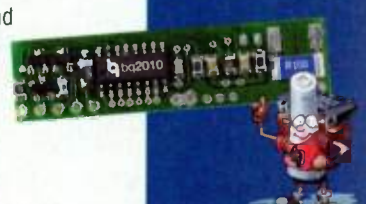

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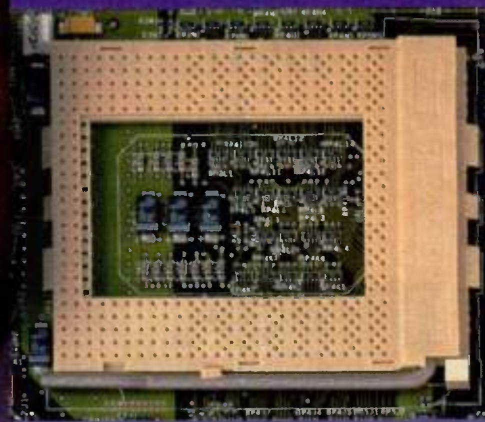

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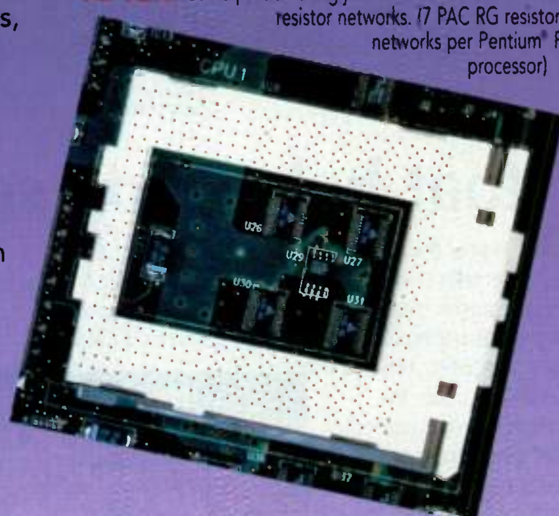

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[1]Covered by one or more of U.S. Pat. Nos. 5,355,014, 5,370,766, and 5,514,612 and other pending applications.

READER SERVICE 106

PRODUCT FEATURE

Single-Chip Multimedia Accelerator Shoehorns In 10 Mbits Of DRAM

Combining multimedia support functions such as MPEG-1 video and audio decoding, video-capture and business-audio applications, the Magic F/X 256/MSM7680 crams 10 Mbits of synchronous DRAM into a single-chip solution. Jointly developed by Silicon Magic and Oki Semiconductor, the accelerator chips provide a highly-integrated solution that makes multimedia subsystems easy to implement.

The 10 Mbits of DRAM, implemented with Silicon Magic's MaxEMem (modular and extensible embedded memory), ties into the multimedia logic via a 256-bit-wide bus. When clocked at 80 MHz, the 64-bit on-chip graphics engine achieves a memory transfer bandwidth of 2.5 Gbytes/s. That high transfer rate should eliminate many bandwidth concerns plaguing other graphics solutions attempting to offer high-quality scaling, multiple surface display, and video/MPEG playback.

The graphics engine includes a high-performance, 2.5D graphics accelerator and a 135-MHz RAMDAC, business audio support, and a DirectDraw accelerator. In addition, it can perform video overlays. An expansion bus on the chip allows an additional 1-Mbyte of memory to be attached, and a 32-bit PCI bus master interface ties the accelerator into the host system.

The Magic F/X 256 and MSM7680 are the same chip, but offered independently by Silicon Magic and Oki Semiconductor, respectively. They are both 100% VGA-compatible and include additional display modes that offer resolutions of up to 1280 by 1024 pixels by 8 bits/pixel with no additional memory, and 1024 by 768 pixels by 24 bits/pixel with 1 Mbyte of external memory.

Chip power is minimized because the device is housed in a 208-lead plastic QFP and operates from a 5-V supply for the PCI I/O lines and a 3.3-V supply for the logic and memory.

In lots of 10,000 units, the F/X 256 sells for $35 apiece. The MSM7680 also sells for $35 each in similar quantities. Both companies have available evaluation cards and a design-guide package that includes schematics, a bill of materials, and information about BIOS software and drivers/installation utilities.

Silicon Magic Inc.
4500 Great America Pkwy.
Santa Clara, CA 95054
Angelo Matthews, (408) 969-3200
http://www.simagic.com
CIRCLE 626

Oki Semiconductor
785 N. Mary Ave.
Sunnyvale, CA 94086
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READER SERVICE 186

PRODUCT FEATURE

First Of MCU Family Line Packs 8-Bit Features, 16-Bit Performance

Well known as a supplier of low-pin-count 8-bit microcontrollers, Microchip has now gone in the other direction by introducing its highest pin-count/performance MCU to date, the PIC17C756. The chip, which comes in a 64- or 68-lead package, is the first in the PIC17C75x family and will provide designers with a higher-performance microcontroller versus processors such as the MC68HC11 series from Motorola, and the H8 series from Hitachi. The PIC17C756 delivers a throughput of about 8.25 MIPS when running from an internal clock of 33 MHz.

On-chip resources include a 12-channel, 10-bit ADC with ±1 LSB accuracy, a single cycle (120 ns) 8-by-8-bit hardware multiplier, and dual high-speed serial channels, each capable of synchronous data-transfer rates of up to 8.25 Mbits/s (500 kbits/s asynchronous). The microcontroller includes a 16-kword-by-16-bit, one-time programmable, EPROM-based program memory and 902 bytes of user RAM. As a result, the chip is able to store and execute longer and more complex programs than previous PIC-family processors.

To round out the feature set, the chip also packs up to 50 I/O pins, all individually configurable as an input or output, four pins that can be configured as capture inputs (120-ns resolution), three pins that can be set to provide pulse-width-modulated outputs (1-10 bits resolution with 130 kHz at 8 bits, or 32 kHz at 10 bits), four timers (two 8-bit and two 16-bit), and local serial expansion interfaces (SPI and I2C). In addition to the active operating mode, the controller includes several reduced-power modes when idle or standing by.

The on-chip ADC's standby mode allows it to convert even when the circuit is in the sleep mode—that permits the processor to perform power-management functions with minimal power drain. On full standby, the chip's current drain drops to less than 1 µA from a 5-V supply, while at 4-MHz the active current is less than 5 mA.

Available in 64 or 68-lead packages, the OTP 64-lead plastic DIP version of PIC17C756 sells for $13.28 each in lots of 1000 units. A reduced-memory version, the 17C752, will be available later this year. The chips are supported by the company's PICMaster-17B universal development system that runs under Microsoft Windows. The software will be available this summer, selling for $2490 without the PRO MATE II device programmer, $3345 with the programming tool.

Microchip Technology Inc.
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Ron Cates, (602) 786-7609
CIRCLE 628

DAVE BURSKY

PRODUCT FEATURE

Embedded x86 CPUs Save Cost Yet Still Contain Most Key System Functions

A pair of x86-family processor developed by Advanced Micro Devices provide highly integrated CPU solutions for both 16- and 32-bit system needs. They offer high throughput and a very familiar programming interface.

Coming in at the high end is the Elan SC410, a cost-reduced version of the previously released SC400, which is based on the integer-only Am486 CPU core. For systems that don't need full DOS/Windows compatibility, the company also released the Am186ED, a new member to the Am186/188 embedded-controller family that includes a full DRAM controller to simplify the support of large but low-cost memory subsystems.

To lower the cost of the SC400, designers removed the SC400's LCD controller and the PCMCIA interface blocks to create the SC410. However, all other features of the SC400 remain intact on the SC410—full DOS/Windows compatibility, local bus and ISA bus interfaces, a bidirectional EPP parallel port, dual 16550-compatible serial ports, an IrDA-compatible infrared port, a keyboard controller, a DRAM controller, a glueless interface to burst-mode ROMs and flash memories, and comprehensive power management (a superset of the APM 1.2 feature set).

A fully-static design, the SC410 can operate at clock speeds of 33 or 66 MHz, and is powered by a 2.7- to 3.3-V supply, but offers 5-V tolerant I/O lines. The chip comes housed in an ultra-small 292 contact ball-grid array and sells for $33 apiece in lots of 10,000.

For high-end 8- and 16-bit applications, the Am186ED includes all of the functionality of the company's Am186EM and ES integrated microprocessors, plus a full DRAM controller. Previous 186/188 family members included refresh support for DRAMs, but didn't include full controllers. Thus, with the 186ED, a DRAM-based memory subsystem, using the low-cost, 16-bit-wide DRAMs can provide more memory at lower cost than memory subsystems built with static RAMs. The 186ED can deliver zero-wait-state performance at 40 MHz using 50-ns DRAMs, 70-ns SRAMs, or 70-ns flash memories for program/data storage.

In addition, since a '188 version of the chip won't be available, the AM186ED includes a programmable bus-sizing option that allows designers to mix 8- and 16-bit peripherals. In the boot mode, an inexpensive 8-bit-wide ROM can be used to boot the system and place speed-critical routines into the DRAM. Features carried over from the EM and ES versions include two 9-bit asynchronous serial ports, two DMA controllers, three 16-bit timers with pulse-width modula-

(continued on page 93)

(continued from page 91)
tion, 32 programmable I/O lines, 12 chip selects, 16 interrupts, and a watchdog timer.

The AM186ED is available in speed grades of 20, 25, 33, and 40 MHz, and housed in 100-lead PQFPs or TQFPs. Prices start at $9.70 each in lots of 10,000 units for the 20-MHz version in a PQFP. Samples are immediately available. A board demonstrating a full system will be available in the third quarter for $186.

Advanced Micro Devices Inc.
One AMD Place
P.O. Box 3453
Sunnyvale, CA 94088-3453
David Sandys for the Am186ED, (512) 602-4073. **CIRCLE 629**
John Hansen for the SC410, (512) 602-4155. **CIRCLE 630**
DAVE BURSKY

Digital-Signal-Processor Engine And 32-Bit RISC CPU Merged Onto One Chip

In its first implementation, the SH-DSP processor—the latest member of Hitachi's SH CPU family—combines a 60-MIPS, 32-bit RISC CPU and a 120 mega-operation/s DSP engine on one chip. The dual processor will initially be implemented in a 0.35-µm CMOS process and will be able to clock at speeds of up to 60 MHz. When executing DSP operations, the DSP engine can perform up to four independent operations during each clock cycle. As a CPU, the chip executes the single-cycle 16-bit instructions at the clock rate, thus delivering a 60-MIPS throughput.

Going for $25 each in lots of 10,000 units for a version with an on-chip 48-kbyte mask-ROM and 8-kbytes of SRAM, the SH-DSP is cost-effective against CPU-only chips on one hand, and against dedicated DSP chips on the other. The dual personality of the chip suits it well for applications in various types of portable communications devices. The DSP portion of the chip performs the speech coding and decoding, echo cancellation, and other signal processing, while the RISC engine performs the internal data management, keyboard control, and protocol handling.

Internally, the SH-DSP shares many on-chip resources to maximize the performance/watt rating. There's a single unified memory space to simplify addressing, and no duplicated circuits or functions, thus minimizing wasted chip area and power. The CPU core employs 16-bit instructions and executes on 32-bit data words. It's a superset of the SH-2 CPU and includes a 32-bit multiplier-accumulator as well as upward code compatibility with the SH-1 and SH-2 CPU families.

The DSP logic includes a single-cycle, 16-bit MAC as well as a barrel shifter and exponent detect logic. Unlike the CPU core, the DSP block employs 32- and 16-bit instructions to achieve the maximum amount of parallelism during each instruction cycle. The DSP block also performs zero-overhead looping, reducing system overheads during DSP operations. To move data quickly, a four-channel DMA controller minimizes the overhead operations to shift data between the external devices, memory, and on-chip peripheral functions.

The chip also contains two synchronous/asynchronous serial-communications channels for full-duplex communications, and three synchronous serial I/O ports that provide simple interfaces for off-chip peripheral functions such as codecs. A 32-bit I/O port provides a connection to a host system or to peripheral control lines. Also on-chip is a complement of various timers, an interrupt controller, and clock generation circuits.

Operating with 3.3-V power supplies, the chip typically dissipates about 200 mW. To conserve battery life in portable systems, the processor incorporates several power-down modes that drop the power drain to the microwatt level. Housed in a space-saving 176-lead low-profile QFP, the ROM-based version of the SH-DSP sells for $25 each in lots of 10,000 units. Volume production will begin in the third quarter. Available now is a RAM-based development version that replaces the on-chip ROM with SRAM.

(continued on page 94)

(continued from page 93)

Software support for the processor comes in the form of various tools and library routines to speed program development. In addition to its own development tools, Hitachi has arranged for software tools from Green Hills Software Inc., Santa Barbara, Calif.; CARDtools Systems Corp., San Jose, Calif.; and a DSP library from Ensigma Ltd., Chepstow, England.

Hitachi America Ltd.
Semiconductor and IC Div.
2000 Sierra Point Pkwy.
MS-080
Brisbane, CA 94005-1897
David Pelavin, (415) 589-8300.
CIRCLE 631

DAVE BURSKY

Four-Port Hub Control Chip Simplifies Systems

A hub controller for the universal serial bus, the AT43311, allows up to four individual computer peripherals to be connected to the computer's USB port. The hub can be implemented as a self-powered device with the controller powered from the power lines in the USB cable. Therefore, in the event of a power failure, the hub controller may still be able to communicate if any of the systems tied into the USB are supplying power to the USB.

Contained on the AT43311 are four downstream ports and one upstream port; the four downstream ports can transfer data at either the low- or high-speed USB data rates (1.5 or 12 Mbits/s). As a hub, the chip serves as a repeater between an upstream host computer and a downstream peripheral. It also can function as a hub controller, during which it records the status of the hub, performs bus enumeration, and transfers data over the downstream ports. Moreover, the chip can drive status LEDs to indicate when ports are in use.

Although the chip operates with an external clock frequency of 6 MHz to reduce EMI, internally that clock is multiplied up to 48 MHz to perform the four-port hub functions. In lots of 1000 units, the AT43311 sells for $6.50 each. DB

***Atmel Corp.**, 2325 Orchard Pkwy., San Jose, CA 95131; John Bryant, (408) 441-0311.* **CIRCLE 632**

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microPOWER, Low Cost IA in Tiny MSOP

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- 8-pin DIP, SO-8, MSOP-8 Surface-Mount
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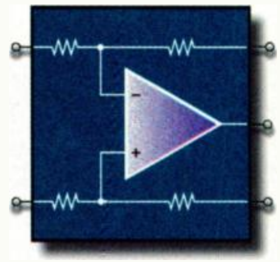
- Offset Voltage....................50µV max
- Low Drift....................0.5µV/°C max
- Input Bias Current....................5nA max
- High CMR....................120dB at G=100
- 8-Pin Plastic DIP and SO-8
- **INA128** and **INA129** are priced from **$3.37** in 1000s.

Reader No. 82 • *FAXLINE* 11296

"Instrumentation Amplifiers are more than just precise op amps. They are complete closed loop amplifiers with built-in precision feedback components."

microPOWER, Low Cost Difference Amplifier

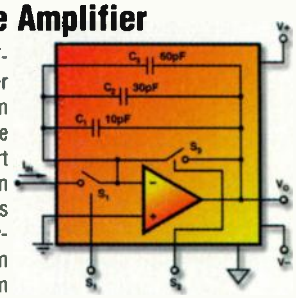


INA132 is a microPOWER, unity gain difference amplifier consisting of a precision op amp with a precision resistor network. On-chip resistors are trimmed for accurate gain and high common-mode rejection. The internal op amp's common-mode range extends to the negative supply—ideal for single-supply applications.

- Wide Supply Range ....Single Supply 2.7V to 36V *or* Dual Supplies ±1.35V to ±18V
- Quiescent Current....................160µA
- Gain Error....................±0.075%
- High CMR....................90dB
- 8-pin DIP and SO-8
- **INA132** is priced from **$1.40** in 1000s.

Reader No. 81 • *FAXLINE* 11353

Precision Switched Integrator Transimpedance Amplifier



IVC102 is a precision FET-input integrating amplifier with on-chip integration capacitors, and low leakage analog switches that convert low-level input current to an output voltage. IVC102 is ideal for amplifying low-level sensor current from photodiodes and ionization chambers. Transimpedance gain is determined by user-provided switch timing signals.

- Input Bias Current....................100fA
- Nonlinearity....................0.005%
- 14-Pin DIP and SO-14 Surface Mount
- **IVC102** is priced from **$4.25** in 1000s.

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READER SERVICE 160

Dynamic Software Reconfiguration Keeps Critical Systems Running

Many Systems Contain Large Amounts Of Code That Must Be Maintained And Updated Without Shutting Down. On-The-Fly Software Replacement Helps Maintain A Running System With Minimal Interruption Of Service.

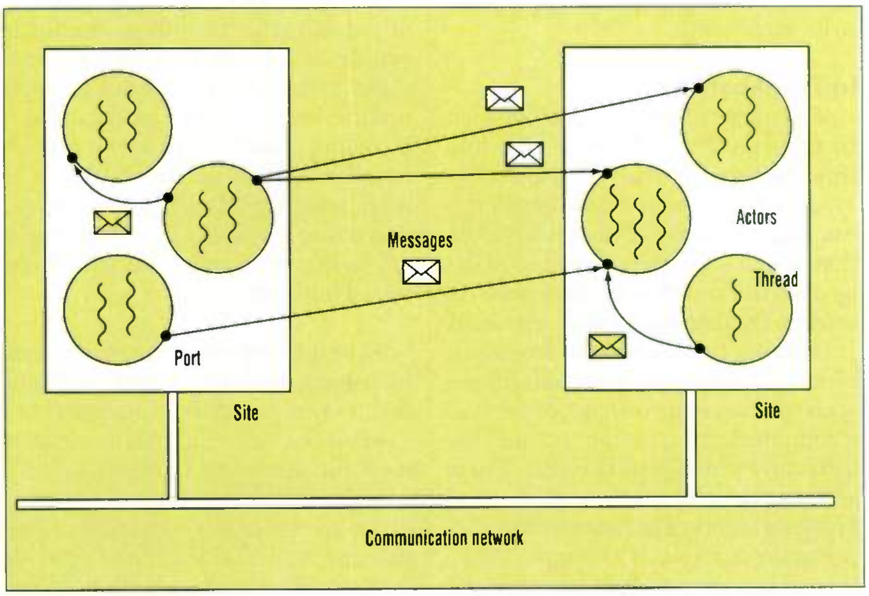
STEFFEN HAUPTMANN and **JOSEF WASEL**, Philips Research Laboratories, D-52066, Aachen, Germany; 49-241-6003-538 fax 49-241-6003-518.

Many large and complex systems such as PABXs (private automatic branch exchanges) are required to be constantly in service, yet contain enormous amounts of software that changes continuously. Despite adherence to stringent quality procedures during development, such system software inevitably harbors faults. In fact, the need for software repairs, upgrades,and extensions never stops.

On-the-fly software replacement allows for maintaining a running system with minimal interruption of service. For example, in a telephone switching system, the software must be upgraded during normal operation. Such replacement is done remotely over the telephone network from a centralized maintenance center and—in the case of fault repairs—simultaneously throughout the entire installed base. On-the-fly replacement also can be used in software for mass market electronics products such as televisions and set-top boxes.

The approach detailed in this article does not require any modification to compilers, linkers, or other software development tools. It does require a modification of the applications to make them replaceable. This entails a separate step in the software development process. There are rules, presented here, for doing this in a formalized way, so the process can be supported by tools.

Achieving on-the-fly software replacement depends largely on the underlying operating system and programming language abstractions. Since concrete concepts cannot be given in an operating-system and lan-

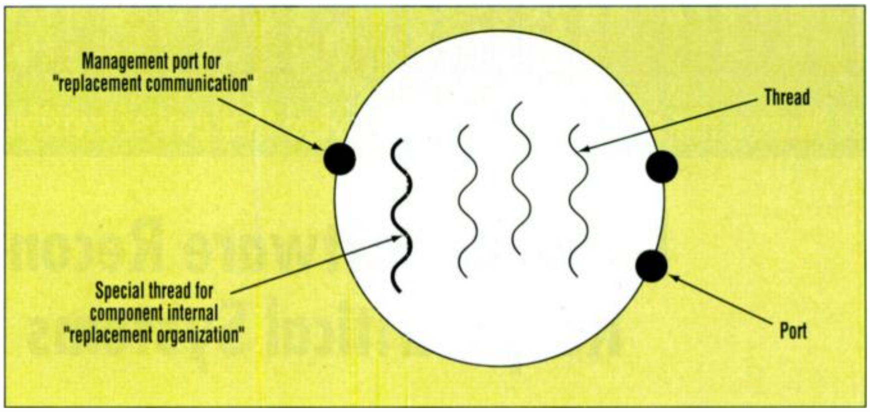


1. Two hardware nodes represent an extract of a distributed system. On each node, there is an arbitrary number of "actors," each of which can contain an arbitrary number of threads. Threads within an actor communicate using various mechanisms like semaphores and mailboxes. Actors communicate only through message queues called "ports."

guage-independent way, the Chorus operating system was chosen because it has characteristics that provide for dynamic software reconfiguration. This software reconfiguration approach could be used with another operating system provided it has the following characteristics: Message-passing based communications, transparent redirection of communication paths, the ability to interrupt or abort a blocked thread that is blocked behind a semaphore or a message-receive system call, and a facility for dynamically loading and starting new processes (called actors in Chorus) on a running node.

C++ was chosen for programming. It supports a combination of the following requirements: The availability of development tools for nearly all platforms, good suitability for real-time applications, and support for object-oriented software design.

The replacement methods do not introduce much run-time overhead in the application. They have a deterministic timing behavior that makes it possible to estimate an upper bound for the duration of the replacement process. The applications are designed to do all the communication between exchangeable units via message passing. There is no need to end any transaction, not even in the replaced module, because each module to be replaced transmits its complete state to its successor.



2. To be replaceable, an actor must have code to manage the replacement process. This involves designing applications so each actor has a dedicated thread, a dedicated port for replacement operations and a special management port.

In The Abstract

The major abstractions of interest in Chorus are actors, ports, and threads distributed across nodes *(Fig. 1)*. A node or site is a unit of tightly-coupled resources, such as a workstation, which is connected to other nodes by a network, such as an Ethernet. An actor is the unit of resource allocation. It is similar to a full-weight process. It contains a shared or protected address space, manages its own set of ports as a communication resource, and contains any number of threads. Ports serve as the points of communication between actors. Threads are the computation context. By comparison, a thread is a light-weight process that executes sequentially.

Since ports are globally-named message queues, they can provide for location-transparent communication and for building distributed systems. An actor can receive messages only via its own ports. Ports can migrate between actors and thus support programming for reconfiguration.. Threads in the same actor can communicate via different mechanisms such as ports, mutexes (mutual exclusions), semaphores, mailboxes, or even shared memory regions. Messages in Chorus are untyped byte streams of variable length and can carry any context.

In Chorus, an actor is the unit of configuration. It has a strong internal linkage and a clearly defined external interface. Therefore, it is well-suited to act as the smallest unit of software replacement.

To repair a software bug, it is usually sufficient to replace one, or in some cases, a very limited number of software units (actors). But to bring updates into a bigger program, it is often necessary to replace a certain number of related actors. This can be simplified by breaking the process down into a sequential replacement of single actors, which has the following advantages:

- The different components can be replaced independently in time, making it easier to meet real-time requirements.
- It is easier to control the replacement process (e.g., in case of a fault).
- The memory needs of the program are smaller because during replacement we only have to provide free memory for one additional actor at a time.

There is no problem to divide the replacement of a set of actors into a sequence of single replacements, if the interfaces between the replaced actors remain unchanged. However, bigger changes often make it necessary to alter interfaces and protocols within the set of replaced actors. The solution in this case is to guarantee the compatibility of the new interface(s). This means a new actor has to provide the interface of the older variant as a subset of its new interface. This requirement for downward compatibility is not difficult for the following reasons:

Oftentimes, the natural way to improve something is to extend it.

Even the complete change of an interface can be modeled with this approach by setting the new interface beneath the old one.

The new actor has to provide both interfaces as long as there is a client in the system that can make use of the old interface. If all such clients are eventually replaced, the old interface part could be invalidated by definition or by a second replacement procedure for the new component.

Replacing An Actor

As a rule, it is assumed that it is necessary to replace multi-threaded actors. The single-threaded case can be handled with simpler means. An actor replacement has to be totally transparent to the rest of the system. The replacement procedure consists of the following steps:

1. Load the new actor into the address space (but do not start it).

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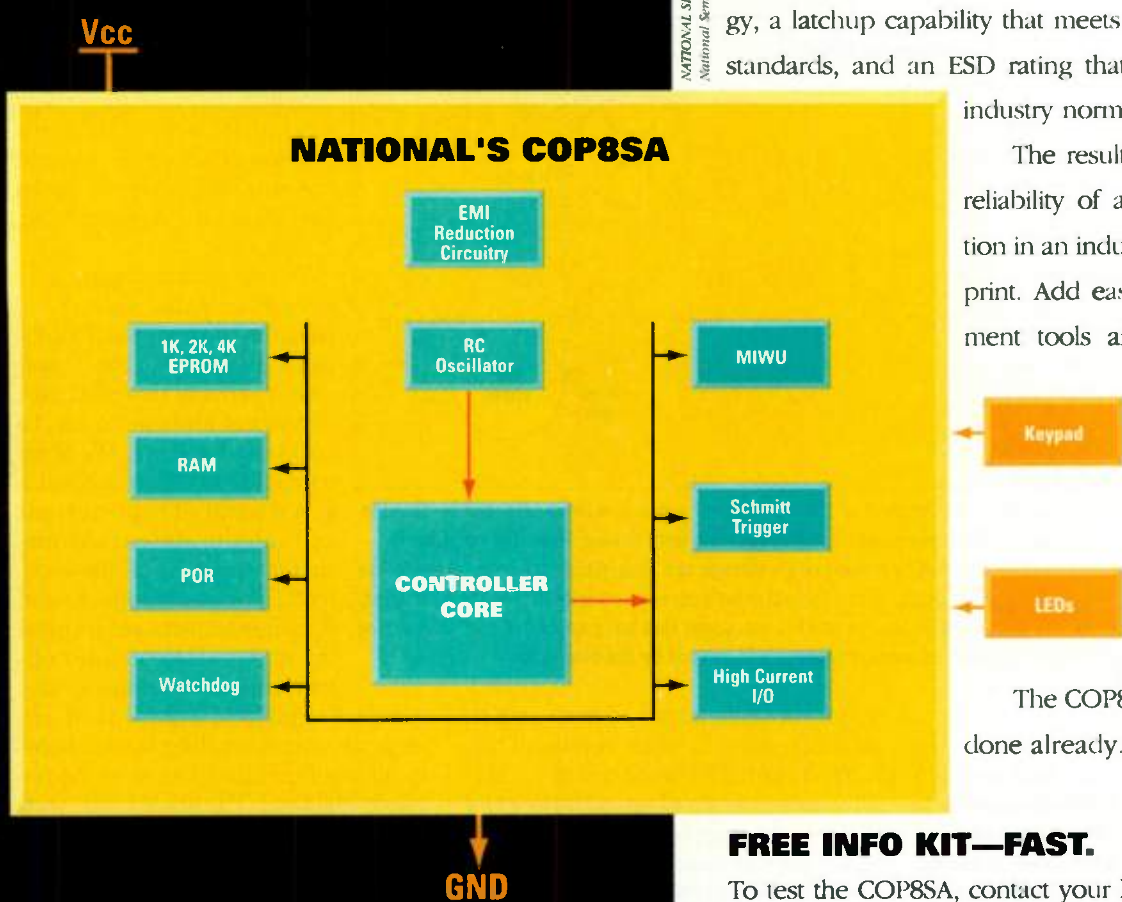

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2. Stop all application threads of the old actor.

3. Collect the state of all objects of the old actor.

4. Transmit these states to the new actor.

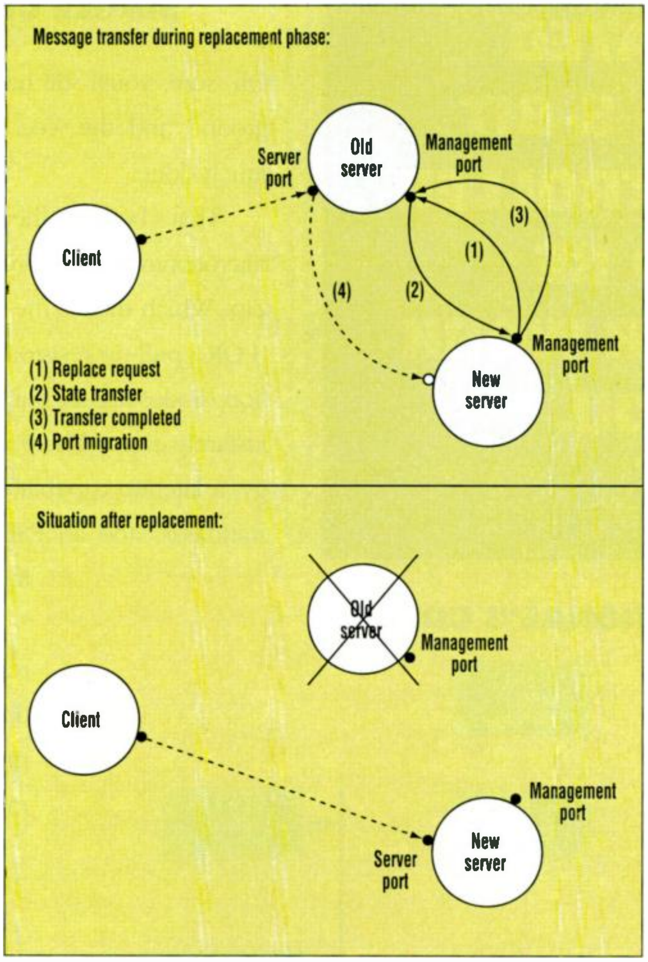
5. Migrate all ports (communication end points) of the old actor to the new one, including all pending request messages.

6. Map (possibly different) object structures between the old and the new actor.

7. Start the threads of the new actor at corresponding points.

8. Delete the old actor from memory.

A multi-threaded actor contains an arbitrary number of threads and ports. For the replacement process, "some additional processing" has to be done within such an actor. Any of the application threads could be chosen to organize the replacement, but the goal is to keep changes in the application as small as possible. Therefore, it was decided to extend the actor model. Each replaceable actor is given an additional thread which organizes the replacement procedure within the actor. It also is given an additional management port that is used for all replacement specific communication *(Fig. 2)*.



3. At the start of the replacement process, a client actor not involved in the replacement is communicating with the old actor. The old actor is stopped by halting all its threads and their states are transferred to the new actor. When the old actor's server port migrates to the new actor, it can be started and the messages that have queued at that port during the replacement process will be read by the new actor.

The exchange thread provides the application an interface that contains the whole functionality necessary to make an application replaceable. It helps to separate whatever is necessary for the replacement management from the application. The C++ implementation of the interface is a class definition. The application must set up exactly one instance of this class ExcThread. The ExcThread object has to be created within one application thread or outside a thread with a static object declaration. The class provides three methods: getExcInfo, setExcInfo and restartPointReached.

The method ExcThread::getExcInfo has to be called up once at the beginning of each thread. It delivers the information on whether the application component is started from scratch or if it replaces an older version of this component. In the latter case, ExcThread::getExcInfo delivers the state of the complementary thread of the older component and a parameter that describes the point at which the thread has to be restarted.

As soon as the thread has re-established all the objects making up its state from the received image, it must call the method ExcThread::restartPointReached.

This method is used to synchronize the start of all threads. It is imperative that no thread leave this method until all threads have entered it. This ensures that all objects are initialized properly before any thread uses them. It is especially important for any objects that are shared by several threads such as ports or semaphores. The method—ExcThread::setExcInfo—has to be called once by each thread after the thread has been stopped for the replacement. This method is used to deliver the current state of this thread to its counterpart in the new component.

The state transfer from the old to the new actor is called for because the new actor takes charge of the operation of the stopped one, the old actor. Therefore, the state transfer must take place between stopping the old actor and restarting the new one. The minimum message flow during the replacement process between the old and the new actor (server) and a possible client is shown *(Fig. 3, again)*.

To transmit the state of an actor means that we have to transmit the state of all its objects. To do this, each object has to provide two methods, one to get and one to set, to transmit its state. We need only know all the objects at a given point of replacement and call the state transmission methods for all these objects. For static objects and dynamic objects referenced through a static pointer object, this can be done by any thread. For all local (stack-based) objects the corresponding thread is responsible for calling the state transmission method. The predefined types of C and C++ are regarded as special objects. Since it is impossible to extend their set of methods, a corresponding set of simple functions is provided to transmit their states.

The new actor will often be different from the old one in code and object structures, but it has to provide corresponding restart points. At this point, the number and/or structure of objects need not be exactly the same as in the old actor. Some objects can disappear, some may be added and some can be changed. The same is true for the function call sequence that describes how a restart point is reached. This requires some kind of object state

transformation function.

The application programmer must define so-called state transformation functions for all changed and added objects that occur in an object set. These functions construct a new or changed object from zero, one, or more existing objects. In practice the number of changes in the object set is often very small. If the function call sequence at the exchange point changes, the application programmer has to provide information on what the corresponding call sequence looks like in the new object. However, this will only be necessary if functional structures are changed.

Exchange Points

The replacement process is started by stopping all threads at points where they can block. These points are called "exchange points." A thread is exchanged by aborting its normal operation after reaching an exchange point and then executing some replacement-related code. Bear in mind that the code of the new actor can be different from that of the old actor. Therefore you cannot choose an arbitrary point in the old actor as an exchange point. Each exchange point needs a (a-priori unknown) corresponding point in the new actor.

Choose as exchange points all the synchronization and communication points where a thread potentially can block. Therefore, the maximum execution time between two of these points determines how fast all threads of an actor can be aborted. This is a worst-case scenario. In a "normal" system, at any point in time, the overwhelming majority of all threads are blocked at synchronization points. They can be aborted immediately. If the execution time between two exchange points is too long we can insert artificial exchange points. The replacement process depends on the following system restrictions:

R1. The application is running on a single-processor platform. This is still the common case for most applications. An algorithm for the multiprocessor case is under investigation.

R2. The CPU load is not always 100%. This is not really a restriction because if the system load were always 100% the system would fail to do

ABORT MECHANISM CODES

Listing 1

```
buf.clear( );
errCode = ipcReceive (buf.msgDsc ( ) , servicePort,  TimeOut);
if (errCode == K_ETIMEOUT )   {
              error  (my Name ,  "Server is timed out ") ;   / / no return
}
```

Listing 2

```
ExcThread  ExcThread (...) ;
              / / create an exchange thread object
...
buf. clear ( );
errCode = ipcReceieve (buf. msgDsc ( ) ,   servicePort,  TimeOut);
if (errcode == K_EABORT    {/ / signals  replacement
             Bin state;   state << object1  << object 2  <<....
              ../ / clean up what is needed
              excThread. set ExchangeInfo (
                             ThreadName,  ReceiveExcPointId,  state);
              / / no return to this point
}
if (errCode  = = K_ETIMEOUT)  {
           error  (myName,  "Server is timed out");  / / no return
}
```

Listing 3

```
static int restart

void fctB ( )    {
         if (restart)  goto ExcPointX;   / / only this one is 'fctB'
         ...
         ExcPointX:
          if  (restart)    "reset state"
          .../ /  local exchange point in function 'fctB'
}
void fctA( )  {
         if   (restart)  goto ExcPointX;  / / only this one is  'fctA'
         ...
         ExcPointX:   fctB ( ) ;
          ...
}
void ThreadBody ( )    {
         restart = get ExcInfo (ThreadName,  excPointId, deliveredState);
         if (restart)
                  switch  excPointId)   {
                             ExcPointIdX:  goto ExcPointX;
                             ExcPointIdY;  goto ExcPointY;
                                                            ...
                  }
                  ...
                  ExcPointX:   fctA  ( );
                  ...
}
```

Listing 4

```
ReceiveExcPoint;
if  (restart)   {
          deliveredState  >>  object1  >>  object2 . .  ...;
           excThread. restartPointReached (deliveredState);
}
buf. clear ( );
errCode = ipcReceive (buf. msgDsc ( ),   servicePort,  TimeOut);
if  (errCode  == K_EABORT)   {/ / signals replacement
              / /  see Listing 2
}
```

Listing 5

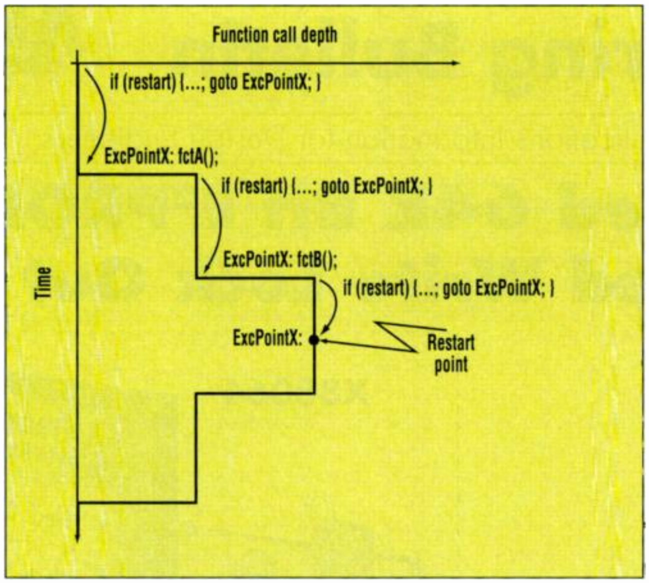
```
Bin state;
...
state  <<...<<  migrate(servicePort)  <<...;
...
excThread.setExcInfo(Threadname,  ExcPointId,  state);
```

all its work.

R3. The total system design guarantees that within a given time interval an actor requesting CPU time gets a guaranteed share of it. This is a normal restriction; otherwise the threads of the actor would not be executed.

R4. A thread must not be explicitly suspended asynchronously. An external suspension is a questionable programming style since we normally do not know at which point another thread really gets suspended. It is a better style to use a semaphore to block a thread at a well-defined point.

R5. All blocked system calls can be aborted in such a way that the thread immediately leaves the call and continues operation.



4. The goal in restarting new threads is to take up where the old actor left off without repeating a function the old actor has already executed. For nested functions, this is done by jumping to the point where a function is called and testing to see if it contains the restart point. This is repeated inside this function until the function is reached which contains the restart point. Then a goto command takes us to the restart point and execution can resume.

Now you can set up the following proposition: If R1 through R5 are valid, then all threads of an actor can be aborted within a deterministic time. This time starts at the point where an application is waiting for replies from an actor under replacement (replacement starting point) up to the point where the new actor has completely taken over the computation of all requests.

If we have one CPU (R1), and this CPU has a load of <100% (R2), then there exists a point in time when all threads of an actor are blocked. If we introduce an additional exchange thread with a priority lower than the priority of all other threads of this actor, then the exchange thread becomes active at this point, because the actor always gets a share of the available CPU time within a given interval (R3).

At this point, it is guaranteed that all "normal" threads of this actor have blocked themselves at blocking synchronization points, since an external suspension of a thread is not allowed (R4). The exchange thread now uses the guaranteed actor CPU time (R3) to carry out the replacement operation. It consists of the following phases: Unblock all threads (deterministic due to R5), collect state of all objects (deterministic due to finite number of objects), transfer state (deterministic due to the finite size of state), rebuild objects (a finite number), and restart new actor (almost instantly).

The upper limit of this time can be estimated by adding the processing time available for this actor, the time to collect, deliver and rebuild all objects plus some minor processing time intervals.

Examples of blocking points with respect to the underlying operating system are:

·ipcReceive: (asynchronous IPC)

·semP: (semaphore P-operation)

·mutexGet: (binary semaphore)

·threadDelay: (sleep a while)

Firing An Exchange Point

If each blocking point is declared to be an exchange point, then sometimes you get huge numbers of exchange points. Most of them will be simple mutex operations that prevent the parallel access to shared data. Some operating systems do not allow threads blocked in a mutex to be easily aborted because mutexes are based on very efficient and fast mechanisms. Therefore, we should avoid making a mutex a potential exchange point.

It has now become evident where to put exchange points in a thread. They can be implemented using the abort mechanism supported by the Chorus operating system. This abort system call unblocks a blocked thread and returns from the blocking system call with a special return code indicating the abortion situation. To avoid prohibiting the use of the thread abortion at the application level for replaceable actors, an additional flag variable to indicate an abortion is needed for a replacement. Assume for the following examples that the abortion return code can be directly interpreted as a signal for a replacement *(see "Abort Mechanism Codes," p. 102).*

Listing 1 shows an example with an ipcReceive statement. First, the buffer for the received data is cleared. Then the ipcReceive fills the buffer with new data available at the servicePort. The third parameter of the receive statement is a time-out value used to avoid an infinite waiting time e.g. caused by a client crash. After the ipcReceive statement, the error code is checked for a time-out condition. This should never occur and is seen as a fatal error.

To turn this blocking point into an exchange point, the extensions shown in Listing 2 (in boldface) are introduced.

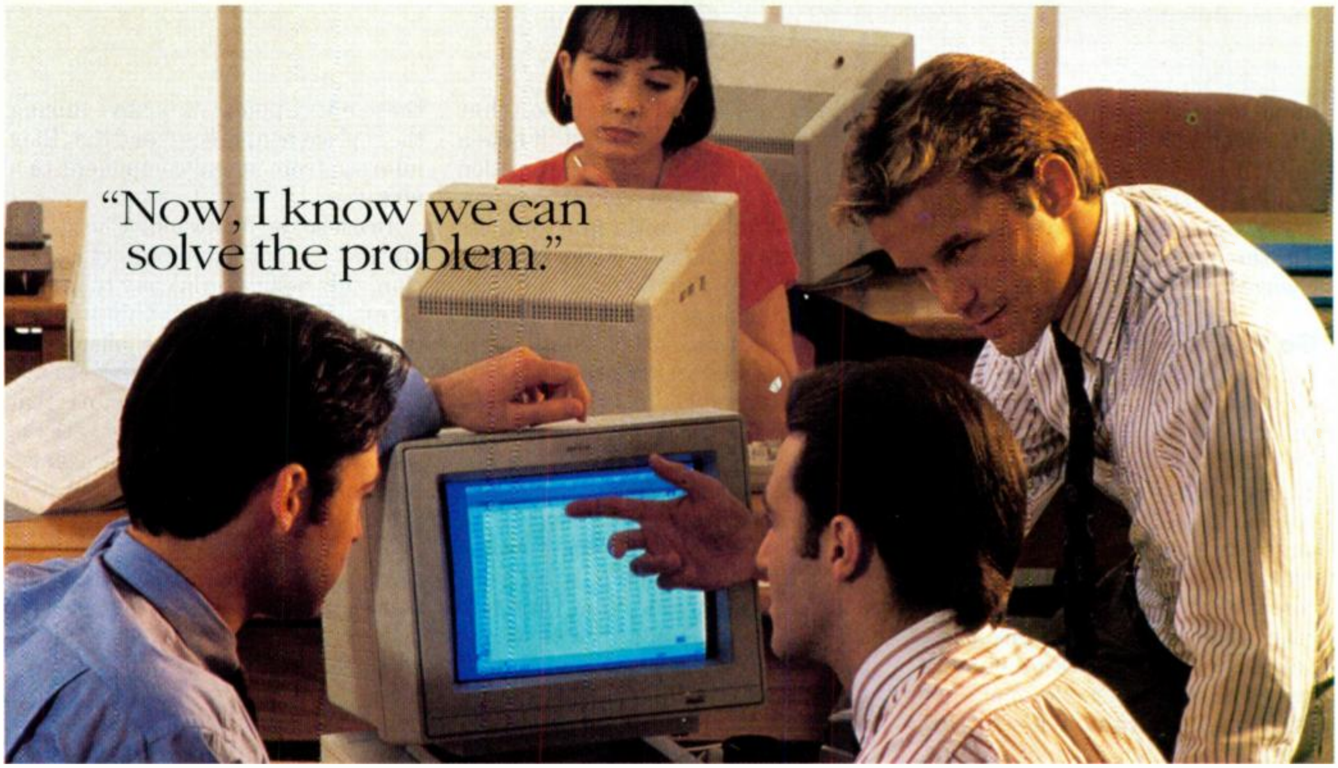
The error code K_EABORT has to be checked as it signals a replacement condition.

In the case of a replacement the state of the thread local objects must be collected first (object1, object2, object3, ...). The state is collected within a special object of type Bin that defines the operators << to append the state of an object and >> to restore it.

The thread then can delete dynamically-created objects or do other things to avoid resource wasting.

Finally the collected state is transferred via the call excThread.setExchangeInfo.

The first parameter of this call is a



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name identifying the calling thread, the second parameter is an integer identifying the current exchange point within this thread, and the third parameter is the state to be delivered. The thread never returns from setExchangeInfo.

Go To The Restart

Stopping the set of threads in the old actor is one thing. The other is to restart the set of threads in the new actor at a corresponding point. The main problem is that a restart point could lie in a function that does not lie on the top level of the function call chain. Therefore, it is necessary to reconstruct the function call chain to reach the restart point. This is not a trivial task with a stack-oriented language like C++ because there is no simple method available to start a program in the middle of a function.

The goal is to go to the restart point without having to execute a statement before this point because, logically, these statements were already executed in the old actor. The well-known "Goto" command can help here. The basic idea is to jump from the beginning of a function to the point where another function is called that contains, directly or indirectly, the restart point. The same is then done inside this function. This goes on until the function is reached that contains the restart point. Here, you jump to the restart point, reset state variables, and continue with the same statement that was aborted at the corresponding point in the old actor *(Fig. 4)*.

Listing 3 gives a general idea of how this works in practice:

Function threadBody calls fctA, and this calls fctB, which contains the restart point. The example code first checks to see if the restart condition is true (if (restart)). Then, the appropriate corresponding restart point is chosen (here reflected in the jump target ExcPointX). There the function fctA is called. Inside the function fctA, the same procedure is repeated. The final jump target ExcPointX is directly in front of the restart point within FctB.

The local variables of a function, which can be part of a calling chain at an exchange point, also have to be saved and restored. This is done by introducing a container object holding all these local variables. The container object also has a constructor that serves two purposes: First, it sets a pointer to itself whenever the function is entered. Second, it allows the reconstruction of the containing objects whenever a restart is made. Another method is provided to collect the state of the containing objects. During a replacement, this method is called via the pointer that was registered during object construction.

The only overhead during the normal operation are three if-statements: One at the beginning of each affected function, one in front of a restart point, one within the container object for the local variables. In addition, there is one pointer assignment! Now, return to the previous example of an exchange point. The code illustrated in Listing 4 gives the picture of the additional code prior to the ipcReceive statement:

We have the jump target for the restart entry and the statements necessary to rebuild all objects. This guarantees that they come up with the same state they had at that point when the old component was stopped. This is normally not the same state it is set to during the default initialization.

The rebuilding of the state in the replacement case has to end with a call of the method ExcThread::restartPointReached as shown in the previous example with excThread.restartPointReached. This ensures the simultaneous start of all application threads. The parameter of restartPointReached is used to check whether the state was read correctly by the application. If there are multiple restart points within one thread, then the set of relevant objects is made up for each restart point.

The restart code can be inserted semi-automatically. The application programmer has to declare the corresponding exchange points, and in case of data changes, one or more state transfer functions. Then all the replacement specific code can be inserted into the application by a preprocessing tool.

Actors communicate with one another via ports that they own. Although ports can be used for communication within one actor, most ports are also used to provide services to the outer world. These ports are the known entry points of external clients. Therefore, you must guarantee that these entry points stay alive during the replacement process and that they migrate from an old component to a new one.

Because the underlying Chorus operating system supports port migration, this behavior is easy to implement. The state of the port is transmitted in a manner similar to the way the states of other objects are transferred. The only difference is that the state of a port is delivered with the special method migrate() which starts port migration on the old actor as in the code example of listing 5.

The migrated port is then set up directly from the delivered state in the new actor. During the time needed for port migration, no external request is lost. All requests are still queuing behind the port and are delivered to the new actor together with the port. So after rebuilding the port the process can be continued at the same point that it was stopped.

In the last phase of the project, our application was ported to the STREAM v2.2 kernel. This kernel not only supports location-transparent communication via ports, but also via global mailboxes. Using these communication abstractions requires no redirection of communication paths, because these mailboxes are not attached to a special actor.

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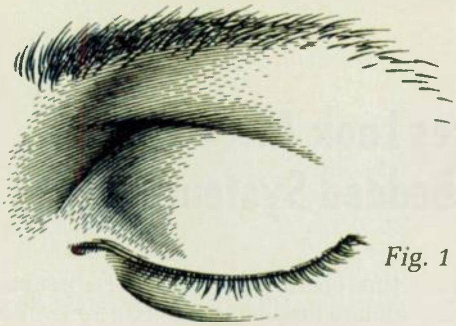

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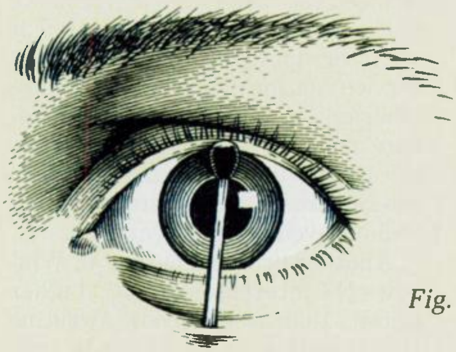

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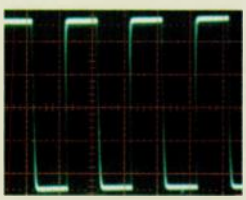

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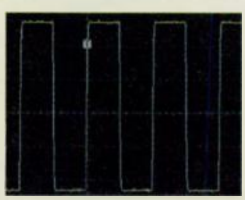

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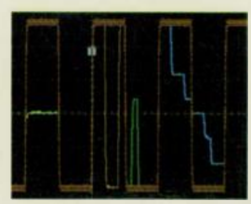

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UPDATE ON WINDOWS/RTOS

Windows API Features Look Attractive To Real-Time and Embedded Systems

The push is on to mate Windows with real-time and embedded systems. Even in the case of systems that will ultimately be deployed without a user interface, there are compelling reasons for having a connection with the Win32 API. The dominating motivation for a link with Windows is the wide availability of tools and compilers, at very low prices. Windows, then becomes attractive, if only as a cross-development environment. A further incentive is the ability to have a supervisory Windows-based user interface that can run on the same processor as the real-time system. Still another goal is to be able to run Windows applications along with the user-interfaced and real-time code. Getting all of these goodies in one package is difficult, inspiring several different approaches to connecting Windows with real-time systems.

Neither Windows 3.x, 95, nor NT, however, were designed to be real-time operating systems. The best candidate for adoption to real-time, Windows NT, has several mechanisms that must be overcome to achieve deterministic real-time performance. One of these is the deferred-procedure call (DPC). The DPC was designed to ensure responsiveness by ensuring that only critical code is executed at the interrupt level, and the rest of a service routine deferred if there are other critical interrupts. This procedure makes the actual timing of an interrupt-service routine unpredictable, and requires extreme care in writing well-behaved device drivers.

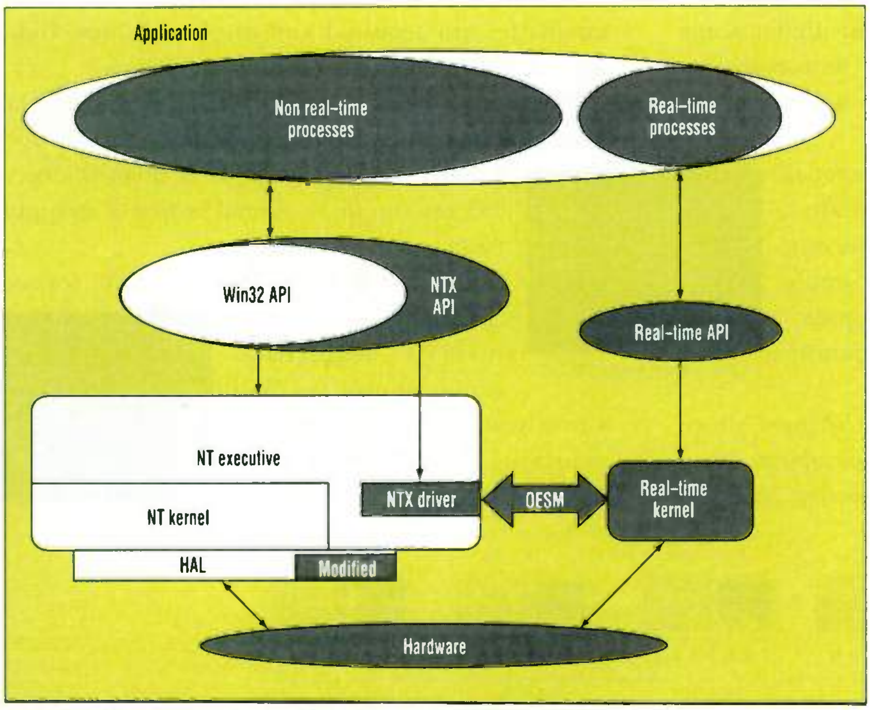
Another problem is that all Windows NT interrupts are at a higher priority than user threads. A routine that is critical to a user can be preempted by a mouse movement unless that routine is written at kernel level. Any code written at the kernel level has access to the entire Windows NT address space, and is not restricted by any protected memory. It is very easy to get into trouble by unintentionally writing over or operating system code, and very difficult to find what went wrong. There are other issues with the NT kernel, such as overcoming priority inversion and synchronization, that must be overcome to implement an actual real-time version of Windows NT

Microsoft will not license the kernel source code, so developers are left to find workarounds. One approach taken by RadiSys, Hillsboro, Ore., (503-646-1800) is to add a real-time kernel and corresponding API onto Windows NT 4.0. The RadiSys INtime product ensures that real-time tasks will always have priority over any NT task, because all of NT is made a single, low-priority INtime task. All tasks under Windows NT run as they normally would, however, when the real-time portion receives an interrupt, all of NT is suspended and the higher priority real-time task runs.

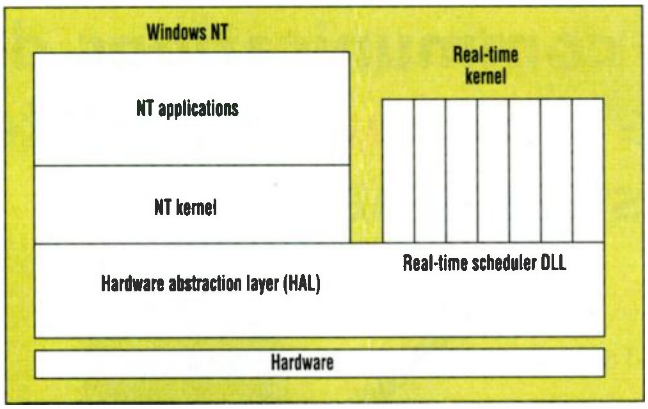
The real-time side of INtime has its own protected memory space, separate from that of Windows NT, thus real-time tasks and drivers cannot overwrite NT memory and vice versa. In addition, each real-time task is assigned its own protected-memory segment at the hardware level, using the descriptor-table registers in the processor. RadiSys did write one kernel-level driver as part of the INtime package. The NTX driver provides cross communication via the operating-system extension mechanism (OSEM). *(Fig. 1)*.

Given the separation and protection between Windows NT and the real-time side of INtime, it is possible for NT to crash completely without damaging an ongoing real-time process. While such a crash will eventually affect system operation, it provides an opportunity for graceful shutdown. Contingency routines on the real-time side can be invoked when there is a crash of NT, avoiding potentially dangerous situations. The current implementation of INtime is designed to run on a single CPU, but future releases will be designed to allow the real-time portion to run on a remote node and communicate with the NT side over a network.

Rather than building on an additional real-time kernel, VenturComm,



1. In The INtime Approach by RadiSys, the real-time kernel resides in its own protected-memory space and communicates with the Windows NT kernel via a special kernel-level driver and the operating-system extension mechanism (OSEM). A crash in Windows NT does not affect a real-time process running under the real-time kernel.



2. In the approach taken by VenturComm, the hardware-abstraction layer has been modified to trap selected interrupts before they go to the Windows NT kernel, and redirect them to the real-time scheduler DLL. This design works around Windows NT's priority spectrum and delayed-procedure calls. Real-time tasks run at the kernel level in Windows NT memory space.

Cambridge, Mass., (617-661-1230) has made modifications to the hardware-abstraction layer (HAL) of Windows NT. While Microsoft does not license the source code of the NT kernel, the HAL is a portion of code that was meant to be modified by OEMs to adapt NT to various hardware environments.

The HAL normally passes interrupts to the Windows NT scheduler to be handled in the standard way. The modifications let the HAL pass selected interrupts past the NT mechanism to VenturComm's scheduler DLL, which sends them to the kernel for execution *(Fig. 2)*. The highest priority is a real-time thread that runs ahead of all other NT interrupts. The real-time scheduler is part of the real-time API (RTAPI) that can be linked to Windows NT using VenturComm's Component Integrator tool. Nonreal-time interrupts will be scheduled according to NT's standard mechanism, but can be preempted by the hard real-time.

Modifications to the HAL allow for the selection of certain interrupts that may be critical-to-normal, off-the-shelf NT applications such as serial communications. It is possible to select such interrupts—like a serial interrupt for receiving data packets—for special treatment as high-priority real-time interrupts. This flexibility provides a finer degree of control than simply relegating all NT operations to the lowest rung on the real-time scale. On the other hand, all drivers are written in kernel mode which gives them access to all of NT's memory space. Essentially, extra care must be taken to see that drivers do not intrude on other drives or NT functions, because there is no segmented protection at that level.

While the RadiSys INtime approach requires a kernel-level device driver to communicate with the real-time side, Imagination Systems, Virginia Beach, Va., (804-497-8200) is currently shipping a real-time kernel called the Hyperkernel. The Hyperkernel talks directly to the hardware and works with an unmodified version of Windows NT 3.51 or 4.0. Like INtime, it loads first into its own segmented and protected memory space, then loads NT as a low-priority task. However, it does not communicate with NT at the kernel level, but at the user level through a real-time access subsystem.

The real-time access subsystem, called Hyperlink, forms a link between the Win32 API and the kernel's API. Imagination's parent company, Nematron, Ann Arbor, Mich., (313-994-0501) supplies a wide selection of Hyperkernel drivers for industrial devices and industrial communications such as Profibus and Interbus. The drivers let users build applications at the Win32 and the Hyperkernel API level.

Compatibility Versus Size

One of the attractions of the above implementations of real-time with Windows NT, is the binary compatibility of Windows applications that can run with and cooperate with real-time applications. While the real-time API's from all three companies are different, spreadsheets, user interfaces for process control, data acquisition applications, etc., can be purchased, and set up to communicate with real-time processes. The problem, however, is one of footprint. It is difficult to get a system under 10 megabytes, and that's before adding the application code.

Smaller real-time systems can still take advantage of the wide variety of tools and compilers for development, but they sacrifice binary compatibility with Windows applications. Phar Lap Software, Cambridge, Mass., (617-661-1510) wanted to address systems with a smaller memory footprint, yet take advantage of the familiarity and stability of the Win32 API, and the availability of development tools. Par Lap chose to write a real-time operating system from the beginning, based on Win32.

Phar Lap's Real-Time Embedded Tool Suite (ETS) was designed to be a smaller, single-task, multi-threaded operating system. A minimum configuration fits in about 28 kbytes of memory, while a fully-featured system with TCP/IP, C run-time library, and a mini-web server takes up roughly 300 kbytes. ETS uses a subset of the Win32 API, and has added 148 additional real-time API's..

Approaching the problem from the opposite direction, some established RTOS vendors are seeking to add Win32 functionality to their operating systems. Making use of a cross-platform porting tool provided by Willows Software, Saratoga, Calif. (408-777-1820), both Wind River Systems Alameda, Calif., (510-748-4100) and QNX Software, Kanata, Ontario (613-591-0931) have added Win32 APIs to their real-time operating systems, VxWorks and QNX, respectively.

Willows has introduced a new version of its tool called WillowsRT for real-time systems. WillowsRT consists of library that can be embedded in all the RTOSs, Unix, and Macintosh operating systems it supports. In addition there is a platform-abstraction layer with all the system-dependent code. Porting a Windows source-code application involves compiling the Windows-specific resource elements, using a language compiler to compile the application code, and linking to the Willows library.

This use of WillowsRT enables Windows source code to be compiled and run on the native RTOS and processor. It does not provide binary compatibility with Windows applications. It does, however, let developers use the familiar tools and port applications like databases, graphics, and office tools to work with their real-time applications.

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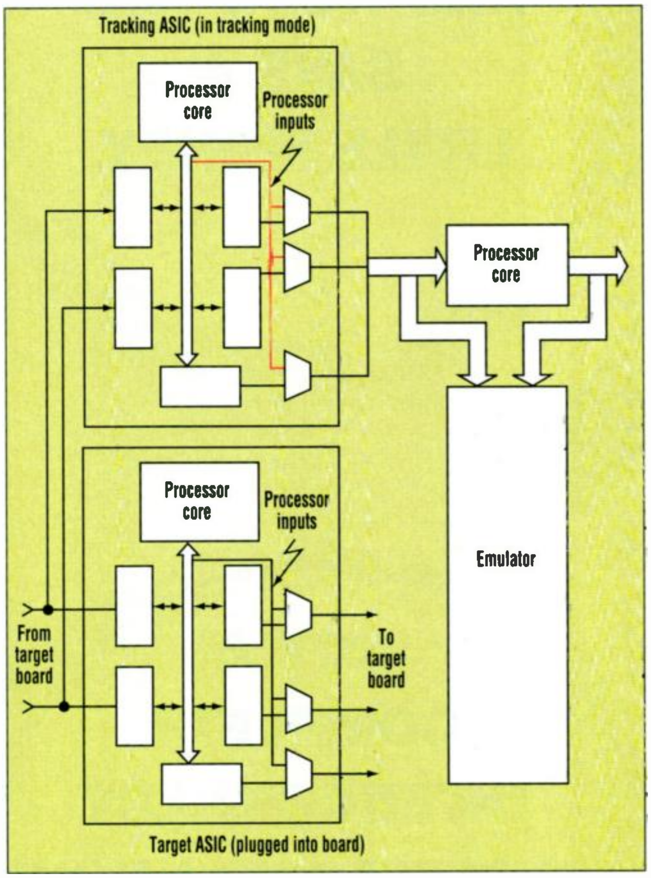
UPDATE ON ASIC TRACKING

Paths Opening To Real-Time Trace Capability On ASIC Cores



When set to tracking mode, the tracking ASIC connects the input signals to the processor to output pins on the ASIC (red line). The ASIC in the target board is identical to the tracking ASIC, but has not been set to tracking mode, so its output pins drive the system. Input signals routed to a bonded-out processor core in the emulator pod generate the same output as the core within the ASIC, making both input and output visible to the emulator.

Developers of ASICs must have the feeling of gradually losing their sight. As more functionality gets integrated onto the same die, the ability to see internal states in real time seems to vanish. This situation is especially true of ASICs based around 32-bit RISC cores, where not only cache, RAM, ROM, timers, and I/O ports are included, but where entire peripherals such as UARTs, modems, LCD display drivers, and all kinds of custom designs (along with their interconnect busses) are put on a single die. It's almost like taking an entire VME board and shrinking it down onto a slice of silicon.

The ability to debug by plugging an in-circuit emulator pod into the CPU socket has disappeared because the CPU core is buried on the die, surrounded by peripherals. Very few, if any, of the chip's external pins actually lead directly to the core. Until recently there have been two ways of getting an idea of what activity is going on inside a core-based ASIC while developing application code. One of these has been described by Norbert Laengrich, president of Embedded Performance (Milpitas, CA) as the "brute force" method.

"Brute force" entails using a packaged-CPU core on an evaluation board, turning off the cache, and implementing the other peripherals in gate arrays and EPROM. Evaluation boards have connections for attaching a logic analyzer that can work with a debugger, develop the code, and then go to an ASIC implementation. A second approach takes advantage of some of the debug support supplied with the processor cores.

In most cases this debug support is an extension of the JTAG boundary-scan technology, such as Motorola's background-debug mode (BDM), and the Embedded ICE supplied with the Advanced RISC Machines (ARM) core intellectual product. The debugger running on a workstation controls the processor core via its JTAG port. Embedded ICE, for example, consists of an ICE breaker module which allows users to set breakpoints, and three scan chains that allow users to clock data out of the chip and load data into it.While the JTAG technology was originally incorportaed into processor designs for testing purposes, it has been pressed into service as a debugging aid. The thing that all JTAG variants have in common is that execution of the CPU must be stopped to shift out the internal data from internal buses and registers.

JTAG support such as Embedded ICE and BDM can be a definite aid in the debugging process. A computer running a source-level debugger can work with a logic analyzer to control a processor core on an evaluation board. This design gives it control through the embedded-JTAG interface, and thus the ability to set hardware and software breakpoints and trigger a logic analyzer trace. The debugger can even show what is happening in the CPU registers.

However, this stop-and-probe approach using a mock-up of the ASIC design on an evaluation board falls short when there are critical timing issues.

The timing relationships between discrete parts on an evaluation board and the real peripheral modules on an ASIC are quite different. Getting a real-time trace out of a core-based ASIC requires cooperation between silicon manufacturer and instrument vendor. It means more than simply bringing enough pins out of the package, it means there must be more on-chip support for debugging.

Beyond JTAG

Motorola has gone beyond JTAG in putting debug support on its Coldfire family, which will soon include the Flexcore for custom designs. While Coldfire still supports BDM, several emulator vendors are taking advantage of the real-time-trace (RTT) capability built into its debug module. The debug module is actually its own little microcoded processor that, among other things, detects change of flow in execution. When it detects a branch, it outputs the destination address to the four DDATA lines that connect to an emulator.

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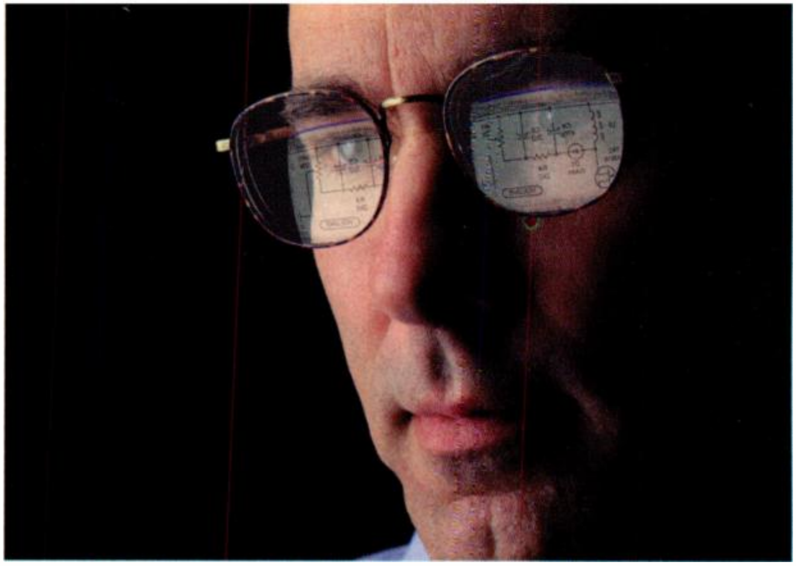

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work is complex

doesn't mean

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Unlike traditional trace, however, emulators, such as VisionICE from Embedded Support Tools (Canton, MA), ADViCE by Orion Instruments (Sunnyvale, CA), and emulator products for Coldfire that are still under development by Applied Microsystems (Redmond, WA), do not record data on every cycle. Rather, emulators record each branch address that is output from the debug module, and count the number of cycles between branches.

According to Applied Microsystems' product marketing manager Jeff Payne, there are four databases that need to be "stitched together" to reconstruct program execution. There is the program flow data from the debug module, the symbolic information generated by the compiler, the source code, and knowledge of target memory. This last piece of data tells which opcodes were located at the change of flow addresses. A register-tracking trace disassembler is then used to work backwards to reconstruct the program flow.

A source level debugger, running on a PC or workstation, can correlate the emulator's data with the compiler-generated symbol information to reconstruct the code with data that has been captured in real time. In the case of VisionICE, the emulator contains a copy of the program that is running on the target system. It can compare the branch addresses and cycle counts with the internal copy, and know exactly where it appears in the code.

Given the four DDATA lines on the debug module, it takes eight clocks to shift out each branch destination address. Since the same clock that is stepping the processor also is stepping the debug module, the two operate concurrently. According to Payne, "If a program jumps in less than eight cycles, it can affect performance." The contents of internal registers are not available during real-time trace, but according to Payne, AMI's emulators will be able, on a breakpoint, to stop the processor, clock out register contents via the BDM interface, then restart the processor. The debug module also can trigger the emulator on an internal core event.

Since the debug module is monitoring the Coldfire's internal bus, it sees what passes between external memory and the CPU, as well as between the CPU and the cache. There is no need to turn off the cache, because cache hits and misses can be followed as well as external memory accesses.

In order to have any kind of emulation, it is necessary to have the cooperation of the silicon vendor to build debug support for their cores. Motorola's step beyond JTAG, with its debug module, may be catching on among other core suppliers. Working with its Japanese partner, Yokagawa Digital Computer, Orion Instruments has developed a 5000-gate macrocell called the integrated debug block (IDB). The IDB works on the same principle as the Motorola debug module, and also offers the ability to break on internal events. The initial target for the Yokagawa/Orion IDB is the ARM architecture, but according to product manager Jack Neithardt, the technology can be adapted to other architectures.

The ability to debug by plugging an in-circuit emulator pod into the CPU socket has dissappeared....

Full Trace On An ASIC

For cores other than the Coldfire (including ARM's), the field is wide open for alternative solutions to emulation. Embedded Performance has been working with ARM to develop a way to capture all the reads and writes performed by the processor core in real time. The result is a technology called TrackerICE that uses a pod to plug into the ASIC socket on a board.

The TrackerICE technology uses a pod with two identical ASICs—one that is plugged into the target board and, a second that reads the input pins of the first. The emulator also uses a bonded-out version of the processor core used in the design of the two ASICs *(see the figure)*. The first ASIC, that is plugged into the target board, runs exactly as it would in the final application. Its input pins take in external signals, and its output pins drive the target board. This arrangement assumes that none of the bus signals of the processor core are visible on external pins.

The second ASIC, however, while identical to the first, is set to a different mode. TrackerICE requires that ASICs be designed with a set of gates that can be set via the JTAG port. These gates can connect the signals on the chip's internal input bus lines to output pins on the ASIC. Thus, the second ASIC is reading the internal inputs to the processor core (which may come from on-chip peripherals, cache, etc.), and making them visible on its output pins. The input bus signals are redirected to the output pins on the second ASIC. Since these pins are not used to drive the target board, there is no need for additional pads or pins in the ASIC design.

Instead, these internal bus signals are fed from the output pins of the second ASIC into the input of the processor core. The isolated-processor core on the emulator pod is, therefore, receiving exactly the same input signals as the core buried inside the ASIC. It then follows that the output signals of the isolated core will be exactly the same as those of the core on the ASIC. The emulator now has access to all the input and output signals of the ASIC core in real time.

According to EPI's Laengrich, there is obviously some propagation delay from chip to chip, but once the isolated core is running, all its timing relationships are identical to that of the core on the target ASIC. Since all the processor signals are seen, users can detect which addresses control on-chip peripherals, and have a clear picture of all reads and writes to cache and peripherals.

The use of a separately-packaged processor core as the basis of the TrackerICE technology adds a certain economy to debugging custom designs. Given the compatibility of packaging, any design built around a given core could be debugged using the same ICE pod. Just plug two target ASICs into their sockets on the pod.

TOM WILLIAMS

PRODUCT FEATURE

Visual Development Tool Accelerates Building Of Java Applets

A new rapid-application-development environment for Java supports visual programming methods with drag-and-drop component placement and property definition. Visual Café Pro, developed by Symantec, lets you place user-interface components such as buttons and dialog boxes onto a form to begin building a Java applet. For each component, there's an underlying source window with a pre-built code frame.

The source windows let you edit Java event handler code associated with each component. As you build the applet, Visual Café Pro dynamically builds a source file that can be later compiled to Java byte code. Any change to a component, either in the source code or by selecting a property in the property list, is automatically reflected in the form.

Visual Café Pro features extensive support for major database servers as well as compliance with the Java database client (JDBC) API. It includes the dbANYWHERE workgroup server that acts as a transparent middleware connection. With this server, Java-based clients can access a variety of different databases, such as Oracle, Sybase, or MS Access through a single server.

The dbNAVIGATOR tool provides a hierarchical view that lets developers see dbANYWHERE servers and available databases ,as well as the tables and columns in each database. Forms Wizards aid in constructing custom forms for accessing any of the supported databases from a single Java applet.

Visual Café Pro's class browser allows you to select a class and then view a list of the methods and data within that class. Clicking on a method will display the code implementing the method in an editing window. Symantec implemented a source parser technology that automatically creates a map of the objects in the source code. This map is used by the hierarchy editor to present a graphical display of the class relationships in an applet. With the hierarchy editor, you can change them or click to go to the section of the program that is desired at that time.

An integrated visual debugger provides windows to display calls, variables to watch and a list of calls by method and class. In addition, a remote debugger lets you debug an applet that's running on another machine across the network.

Visual Café Pro, available now, goes for $499.

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CIRCLE 633

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New Tools Design Object-Oriented Software

Graphical Designer version 2.0 introduces three new software design tools for both Unix platforms and Intel-based PCs running Windows 95 and NT. GDProPlus and GDPro allow developers to create object-oriented software designs using a range of design methodologies, such as Rumbaugh, Booch, Unified, and Use Cases. GDProPlus also features true meta-CASE capabilities for creating customized object-oriented design methods.

Both products generate source code for all supported design methodologies in one or more languages, including C++, C, and Java. They also can reverse-engineer source code to automatically produce detailed design diagrams and produce a variety of reports on design- quality and code metrics. Other features include collaborative multiuser development support, multiplatform support, and easy integration with other development tools such as debuggers, compilers, and configuration management tools.

The third family member, GDDraw, is a template-based engineering drawing tool. Organized in application-specific palettes, the templates provide symbols for many applications, including software design, computer network layout, and organizational charts. Graphical Designer 2.0 runs on Unix workstations from Sun, HP, Silicon Graphics, and IBM, as well as Intel-based PCs running Windows 95 and Windows NT.

GDProPlus pricing starts at $8995 for the Unix version and $3495 for either Windows version. GDPro pricing starts at $3495 for the Unix version and $995 for either Windows version. GDDraw pricing Starts at $995 for the Unix version and $495 for either Windows version. Prices include a hypertext-based on-line help system and tutorials. ML

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OCTOBER

Conference on Domain-Specific Languages (DSL), October 15-17. Red Lion Resort, Santa Barbara, California. Contact USENIX Conference Office, 22672 Lambert Street., Suite 613, Lake Forest, California 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

ICSPAT/DSP World 1997, Oct. 15-17. San Diego Convention Center, San Diego, CA. Contact Denise Chan, Miller Freeman Inc. (415) 278-5231; e-mail: dsp@exporeg.com.

IEEE Holm Conference on Electrical Contacts, Oct. 18-22. Wyndham Franklyn Plaza, Philadelphia, PA. Contact Wendy Rochelle, IEEE Conference Services, 445 Hoes Ln., P.O. Box 1331, Piscataway, NJ 08855-1331; (908) 562-3870; fax (908) 981-1769; e-mail: w.rochelle@ieee.org.

IEEE Telecommunications Energy Conference (INTELEC '97), Oct. 19-23. World Congress Centre, Melbourne, Australia. Contact Robert N.K. Thuan, Network Products-Telstra Corp. Level 14, 242 Exhibition St., Melbourne, Victoria 3000, Australia; (61) 3 634 6216; fax (61) 3 632 3607

Sensors Expo, Oct. 21-23. Cobo Convention Center; Detroit, MI. Contact Expocon Management Associates Inc., (203) 256-4700; e-mail: sensors@expocon.com; Internet: http://www.expocon.com.

Fourth IEEE International Conference on Image Processing (ICIP '97), Oct. 26-30. Fess Parker's Red Lion Resort, Santa Barbara, CA. Contact Sanjit K. Mitrea, Electrical & Computer Engineering, University of California, Santa Barbara, CA 93106-9560; (805) 893-3957; fax (805) 893-893-3262; e-mail: mitra@ece.ucsb.edu.

11th Systems Administration Conference (LISA '97), Oct. 26-31. Town & Country Hotel, San Diego, CA. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

19th Annual International Conference of the IEEE Engineering in Medicine & Biology Society, Oct. 29-Nov. 2. Sally Chapman, Secretariat, National Res. Council of Canada, Bldg. M-55 Rm. 393, Ottawa, KIA OR8, Canada; (613) 993-4005; fax (613) 954-2216.

19th International Conference of the IEEE Engineering in Medicine & Biology Society, Oct. 30-Nov. 2. Chicago Marriott Downtown, Chicago, IL. Contact Meeting Management, 2603 Main St., Suite 690, Irvine, CA 92714; (714) 752-8205; fax (714) 752-7444; e-mail: embs97@ieee.org; Internet: http://www.eecs.uic.edu/-embs97.

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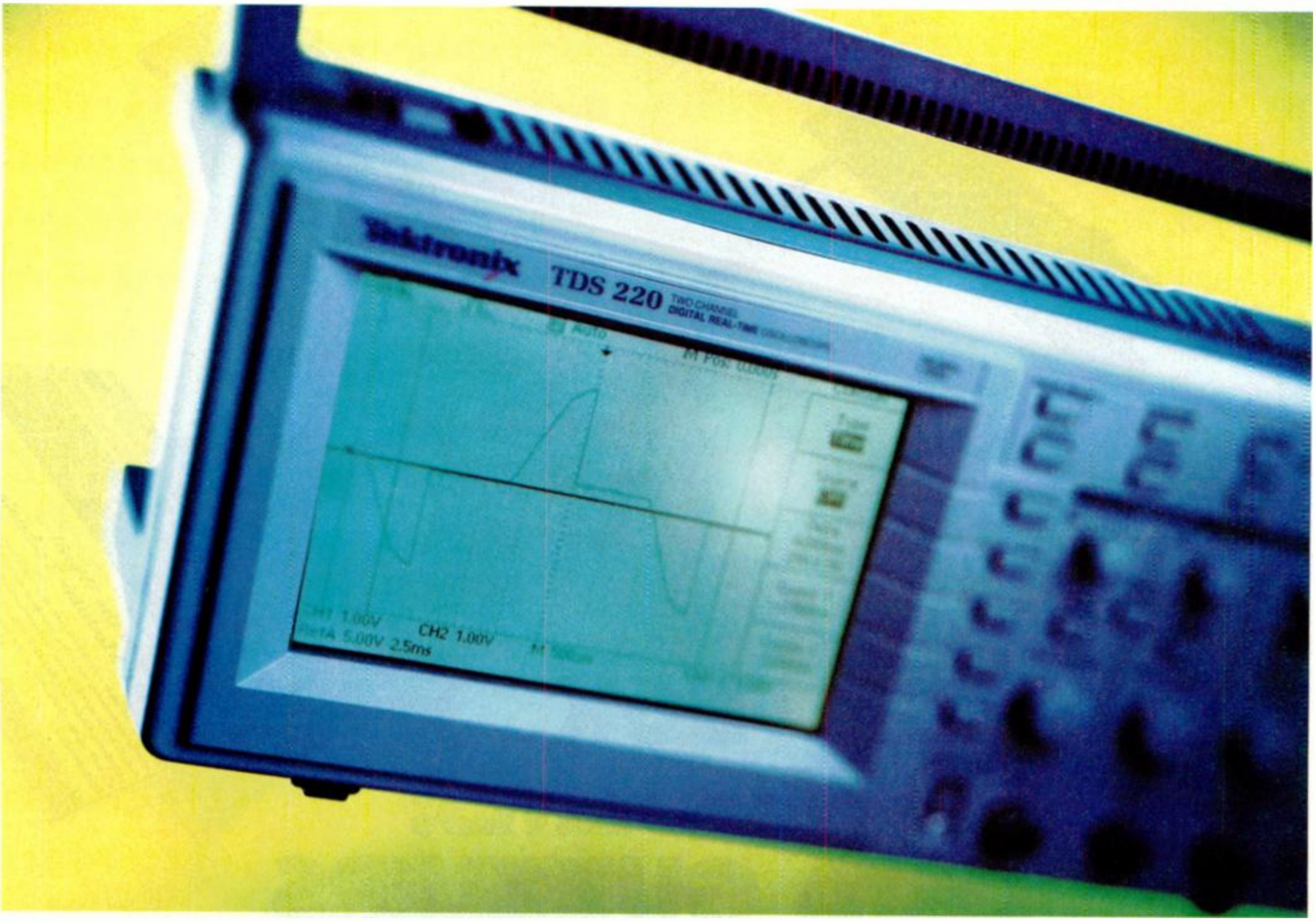

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56-kbit/s Modems: Hey! How'd They Do That?

PCM-Based Modems Are On The Scene, Promising To Operate At Near-ISDN Speeds Over POTS Lines.

Lee Goldberg

SPECIAL REPORT

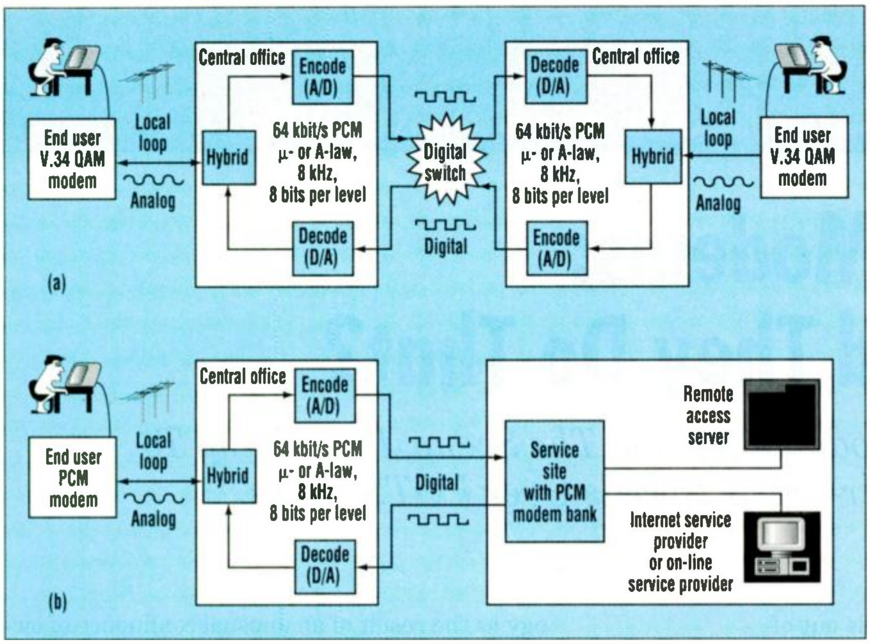
Technology has a way of making fools out of even the smartest people. For example, back in October (*"Advanced POTS Modems: Mr. Moore, Meet Mr. Shannon," ELECTRONIC DESIGN, Oct. 1, 1996, p. 77*), we cheerfully used Shannon's law to prognosticate that the 33-kbit/s modems were probably the last generation of POTS-based carrier technology to hit the market. During our research, we had queried many of the major players in the modem-chip world (Lucent Technologies, Rockwell Semiconductors, and Texas Instruments) if they had any near-term developments which might break through the Shannon limit. Of course, they all solemnly shook their head "no," and told us to wait for asymmetrical digital subscriber line (ADSL) if we wanted more speed over a copper pair.

Art Courtesy: Rockwell Semiconductor

Within two weeks of the article's publication, our magazine was deluged with letters from observant readers who called our attention to the newly-introduced 56-kbit/s technologies that were being introduced by those same major players (*see the box, "A Reader Gets Lucky," p. 124*). How could such breakthrough technology slide in under everybody's radar screens?

We can, at least partly, explain the unexpected and sudden appearance of 56-kbit modem technology as the result of an unusual confluence of circumstances and technology which would have taken even Nostradamus by surprise. It seems that several companies realized that pulse-code modulation (PCM) could be used to get faster downstream data rates. They all had been working quietly on similar solutions which they intended to announce some time in 1997. These plans were derailed when U.S. Robotics' unexpected announcement of its 56-kbit technology brought PCM modems into the spotlight one half-year or more ahead of schedule. This activity has grown from the unexpected and unrelenting demand for fast digital connections by many customers who, until recently, were content with a simple dial tone. Since most telecom providers have fumbled the rollout of ISDN digital lines so miserably, their subscribers have been left to make connections to the Internet over their plain-old telephone service (POTS) lines.

The increasing size of data transfers (and general disgust with long waiting times for downloads) provided ample incentive for development of several generations of increasingly sophisticated modems. These little speed demons used various flavors of quadrature-amplitude modulation (QAM) to squeeze as much digital data as possible, down lines which were heavily optimized for analog human speech. With QAM-based modems



Conventional V.34 modems use sophisticated analog modulation techniques to maximize the amount of information carried across the phone network (1a). The modem's signal is digitized at the sender's central office, transported across the network, and reconverted to an analog signal at its destination, adding at least 36 dB of quantization noise in the process (1b). PCM modems rely on the digitally-terminated lines used by ISPs to eliminate the downstream A/D conversion. The lower noise floor makes it practical to employ PCM encoding to handle higher data rates.

beginning to approach their theoretical limits at 33.6 kbits/s, technologists began to look at PCM-based schemes, which enjoyed significantly higher data rates under certain circumstances.

There's A Catch

Of course all this technology sounds great, but there's a catch. The reason PCM hadn't attracted attention until now is that it only works well when at least one end of the connection is digitally terminated (*see the box "PCM 101" p. 128*). PCM is not meant for ordinary analog phone connections. When you place an ordinary call, your voice travels over the phone lines as an analog signal, and gets as far as the local exchange (*Fig. 1a*). Once there, the analog signal is filtered, digitized by a codec, and folded into a trunk line for transport to the switch closest to its final destination. Then, the digital stream is pulled off the trunk line and passed to a codec, which turns it back into analog signal, sending it onto a set of twisted pair wires connected to your friend's phone or modem.

Now, the problem with PCM connections is that any time an analog signal is digitized with a standard µ-law codec, some of the finer details of the waveform fall between its digital cracks, adding about 36 dB of quantization noise to the signal. Unless elaborate processing is used, this noise can be significant enough to prevent reliable detection of sufficient discrete voltage levels to give it any real speed advantage over conventional QAM-based modems.

Luckily, most big-time Internet service providers now use digitally terminated lines to bring traffic off of the public-switched telephone network (PSTN) and onto the 'Net. This allows downstream digital traffic from a server or the Internet to be sent directly to the local exchange, where it undergoes a single D/A conversion to PCM levels (*Fig. 1b*). Since the D/A process introduces little or no noise into the signal, most of the codec's sampling points can be used. A better DAC will be required to synthesize the output cleanly enough. The prevailing wisdom is that a 16-bit converter will be sufficient, providing that its noise floor is 85 dB or more below full-signal level.

A PCM modem's receiver will use clock-recovery techniques to extract the 8-kHz master clock from the signal, and synchronize the incoming data to it. In theory, the first generation of commercial PCM modems will take advantage of the lower noise floor and synchronous data transfer to provide up to 70% more downstream throughput than today's best QAM-based modems. Of course, your mileage may vary depending on the modem you buy and local line conditions.

In other words, you won't be able to use your PCM modem to play networked Doom or exchange files with your friend's computer next door, but you will be able to download from your commercial Internet-access providers (IAPs) at near-ISDN speeds. Businesses using T1 lines or other digitally-terminated connections will also be able to take advantage of these faster modems to strengthen ties with home and mobile workers, as well as on-line customers.

Both Lucent Semiconductors, Berkeley Heights, N.J., and Rockwell Semiconductors, Newport Beach, Calif., seemed to be deeply shocked when U.S. Robotics, Skokie Ill., announced its X2 PCM-modem technology late in the fall of 1996, many months ahead of the two semiconductor houses' planned rollouts. In the ensuing panic, both Lucent and Rockwell nearly tripped over each other to see who announced their embryonic 56-kbit technology first.

After the smoke settled, both companies agreed to work together to make their products interoperable, although they would not work with products from U.S. Robotics and its allies. While this classic standoff will eventually resolve itself, it may take some time for market forces to erode the two parties' entrenched positions.

A Work In Progress

If the specifications and technical information presented about PCM modems seems a little vague, it's because they are works in progress. Under better circumstances, there would be time to attend to the details that surround a new communication technology hashed out behind closed doors. In this case, market pressures drove all parties to play their hands very early in the game, leaving lots of questions to be answered later.

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PCM modems have attracted more than one group that wants to exploit their potential. The original 3-way split has boiled down to two camps, with Lucent and Rockwell combining forces. Both camps are locked in a struggle to have their technology be declared a standard, since it would give the winner a time-to-market advantage of many months. Nevertheless, they are actively participating in both the Telecommunication Industry Organization's (TIA's) TR-30 fast-track committee, and the International Telecommunication Union's (ITU's) study group 14 to resolve their differences. Both sides are close to agreement on most of the key points necessary to implement a downstream PCM channel, but many other issues are far from resolved at the time of this writing.

The realities of the marketplace seem to be driving the standards process at a surprisingly brisk clip. The TR-30 group is now predicting a North American interoperability

A Reader "Gets Lucky"

Soon after I predicted an upper limit of 35-to-40 kbits/s for POTS modems in "Advanced POTS Modems: Mr. Moore, Meet Mr. Shannon" (ELECTRONIC DESIGN, Oct. 1, 1996, p. 77), the magazine received many questions from surprised readers, asking about the recent announcements of 56-kbit technology. I did some research and answered them as best I could, but one astute reader, Jack McDonald, went one better and contacted Bellcore's renowned communications researcher, Bob Lucky. Thanks to both Messrs. McDonald and Lucky for sharing their insights with us in the e-mail exchange below:

Date: Thu, 28 Nov 1996 13:43:38
From: Jackmcdon@aol.com
To: leeg@class.org
Subject: Fwd: Rockwell's Claims

Lee,

I have been thinking about our correspondence regarding Shannon and the PCM channel and contacted the world's best on the subject, Bob Lucky at Bellcore. I have attached our correspondence. Seems that Shannon does not apply to the PCM channel since the noise is not white Gaussian (which Shannon's theorem assumes) but is quantizing due to the PCM process.

Using this knowledge, Rockwell has predistorted its carrier, thereby minimizing the quantizing distortion, and gets direct access to the 64Kb/s channel (which becomes 56Kb/s because of bit robbing and digital-switch synchronization issues, unless, of course, clear-channel 64Kb/s line rates are used).

Best regards,

Jack McDonald
Past President
IEEE Communications Society

Forwarded message:
From: lucky@bellcore.com
To: Jackmcdon@aol.com
Date: 96-11-21 20:00:53 EST

Jackmcdon@aol.com wrote:
Bob,

I have been reading about 56 Kb/s speed claims for new modems from Rockwell and have a basic question. What does Shannon have to say about the maximum capacity of the public network, i.e. that of a single hop u-255 PCM channel? I recognize that this is not the subscriber-loop capacity which is set by paired cable, which people using ISDN and XDSL are exploiting at mega bits per second. But end to end, the PSTN has band-limiting devices like PCM codecs which modems must address.

I am just a switching guy and you are the expert, but according to my calculations, the maximum bit rate for such a channel is around 45 Kbps. This is from:

C= W log2(1+S/N)

and a single PCM channel with W= 3.4 Khz and S/N= 40 dB. I recognize that N is assumed to be Gaussian and the PCM channel noise is from quantizing distortion, but don't know the impact on the formula.

How does Rockwell get 56 Kb/s and are their claims valid?

Jack McDonald

****

Jack,

Funny you should ask. I really consider the 56kb modem my own invention. At a meeting about five years ago at Bell Labs, I observed that the Shannon capacity of a phone channel was not 30 kbps or so, as had been calculated for years, but was really closer to 64 kbps.

The reason is that the local loop is simply a copper wire with "infinite" bandwidth, which has a capacity of, say 1.5 mbps, for a distance of a couple of miles. After that, the channel is digitized, and sent as a 64-kbps stream on a digital carrier. Thus we cascade a channel with a capacity in excess of a megabit per sec with a channel of capacity 64 kbps.

What is the resulting capacity? Should be about 64 kbps. Because of various timing considerations, the capacity is really about 56 kbps. The way you get that capacity is to send a signal that is "pre-quantized," so that it flows through the quantizer without change. Bell Labs started working on this at that time five years ago, and finally the work is paying off.

Bob Lucky

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standard by June 1997, although the smart money is betting on seeing a solution in the late fall or early winter. The ITU will take a bit longer (perhaps one-to-two years) to produce a global standard.

Since these technical issues have become politicized as part of corporate marketing strategies, it may be much more difficult to converge on a single, working standard. Despite the confusion, it's not a bad idea to get some sense of the issues being kicked around in the TIA's and ITU's subcommittees. If nothing else, it may help in sorting through some of the conflicting claims that the competing interests are eagerly tossing out like trinkets at a Mardi Gras parade.

An Upstream Debate

While they differ on many smaller issues, their disagreement over how to implement this upstream channel (from the subscriber to the central office) is the most controversial part of the technical debate. PCM traffic in the upstream direction faces more difficulty, having to pass through the codec's A/D converter on the way to the trunk line. The μ-law encoder adds the aforementioned 36 dB to the noise floor, making it much more difficult to achieve high data rates.

While there are several other challenges limiting upstream-data speed, one of the most pernicious is the reflected energy known as far-end echo. It is introduced to the upstream signal by the central office's codec. This reflected energy is quite complex, and work is still in progress to develop the very sophisticated noise-cancellation techniques to reduce, if not eliminate this noise source. Synchronization of the upstream data to the 8-kHz network clock also is somewhat more problematic.

Because of the difficulty involved, U.S. Robotics chose to use simpler, proven V.34, 28.8-kbit/s QAM modulation and protocols for its upstream channel. This technology has allowed them to bypass a potential stumbling block and get their X2 technology to market first.

Lucent has more experience with the subtleties of digital phone lines, and has aggressively pursued a PCM-based upstream-channel technology. While their development is not quite complete, Lucent anticipates that a first-generation PCM modem using their V.flex2 technology will achieve around 40 kbits/s in the upstream channel. It is difficult to know whether the Lucent/Rockwell contingent is making valid claims that their 30% speed advantage is critical for advanced modem applications with symmetrical bandwidth requirements (POTS video-conferencing), or whether it is simply an attempt to gain marketing advantage with a proprietary technology.

There also are several issues surrounding the protocols that assure modems from different manufacturers can interoperate. Perhaps the most significant of these is the handshake protocol. The ITU's V.8 negotiation protocol is the worldwide standard which governs how modems recognize each other, and establish a connection. Among other things, V.8 provides guidelines on how to cooperate while probing line conditions, negotiating data rates, and selecting the error correction protocols to be used.

> **Even if they don't live up to all the claims, PCM Modems will play an important role in extending the life of the copper pair . . . infrastructure.**

To accommodate PCM modems, V.8 will have to be modified to include recognition and signaling for 56-kbit service, new line probing techniques, rules for backwards compatibility to QAM-based modems, and a robbed-bit signaling protocol. Since many countries use a codec-compression scheme called A-law, provisions also must be made for negotiating the use of the μ-law and A-law codec algorithms. It is likely that the ITU will allocate some of the unused bits in the current protocol exchange to control these features.

Even though the ITU is working hard to track the evolving technology, the global scope of the problem may delay final versions of the update to V.8 and the other appropriate modem standards until mid-to-late 1998. In the interim, PCM modems will be forced to rely on de facto industry standards to permit the new modems to talk with themselves as well as V.34, and other ITU-compliant, QAM-based devices. One ray of hope in this tangled mess is that it is almost certain that all parties will agree to have their modems fall back to V.34 (28.8 kbits/s) operation in the event that they cannot establish a PCM connection.

Hidden Gotchas

Beneath the hoopla surrounding 56-kbit modems lie a series of less-obvious technical problems which also must be addressed before the technology is rolled out for mass consumption. Efforts toward resolution of these issues are not limited to the three most prominent players. Cirrus Logic, Fremont, Calif., among others, has made substantial contributions to the standards effort, especially in the areas of symbol encoding and mapping. Cirrus also has worked extensively with techniques for DC suppression in PCM transmission.

Cirrus's vice president of DSP development, Dr. Carl Nordling explained that the PCM community must adopt a DC-suppression technique in order for their modems to work with the majority of line cards in today's networks. According to Nordling, a random PCM bit stream does not always average to 0 V within a short time. This condition results in the generation of a DC component which could create non-linear effects in the coupling transformers found in many line cards and modems. One way to alleviate the problem would be to break the transmission into 8- or 16-pulse frames and add a DC-correction pulse at the end, which brings the DC average of the frame to zero. While using a DC-suppression protocol would drop a modem's useful throughput around six percent, it may be necessary to ensure compatibility with the existing PSTN.

Another gotcha that Nordling pointed out was the fact that FCC part 68 regulations on EMI/RFI may not permit all PCM-voltage levels to

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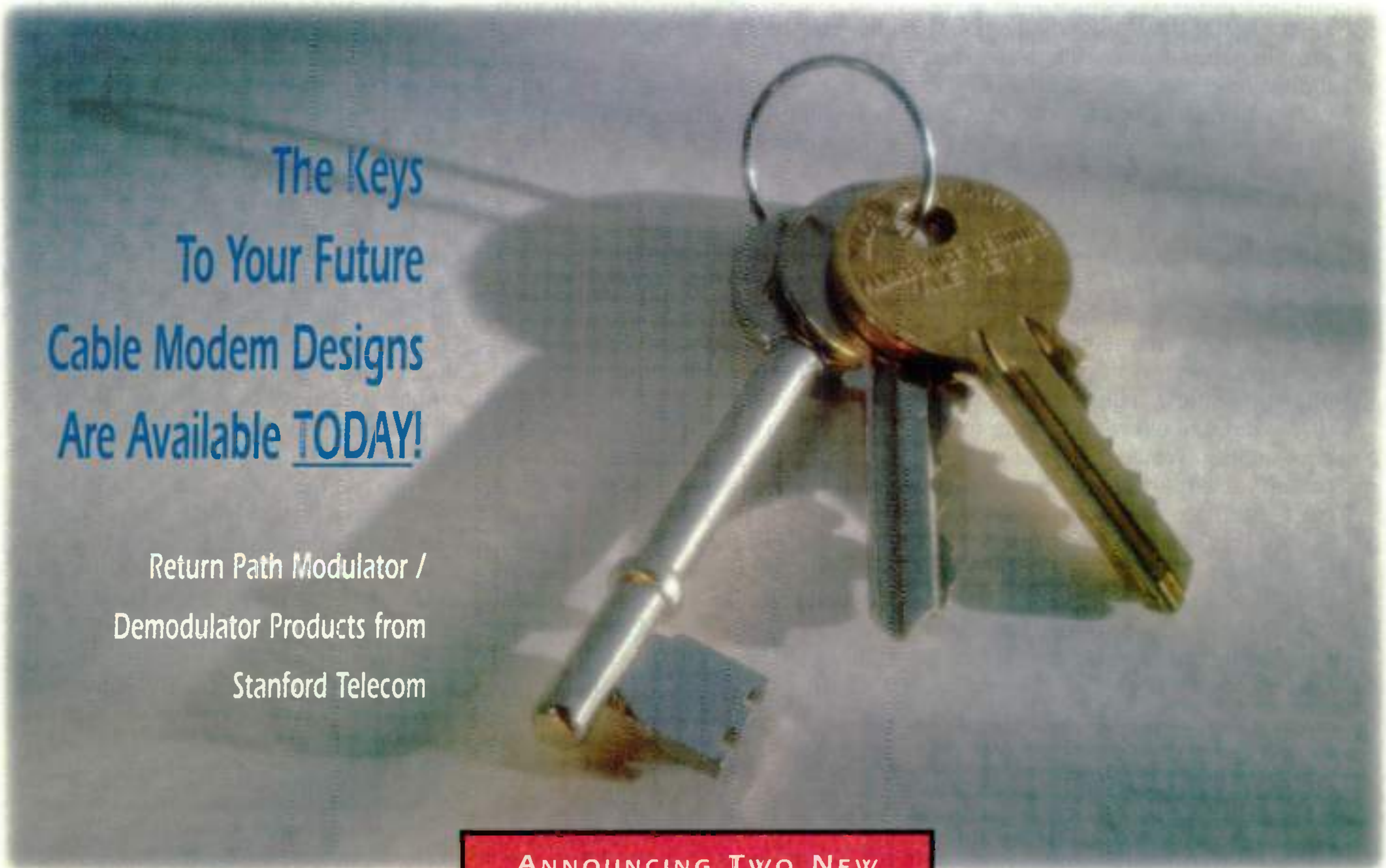

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be used to transmit data. The -9 dBm limit for signal strength at the modem, and -12 dBm at the central office could keep a few of the higher-voltage PCM sample points from being used. This limitation could result in an effective raw-data rate of as low as 53 kbits/s. Other potential solutions include a protocol to keep certain noisy bit patterns from being transmitted, or a relaxation of the FCC regulations.

Mike Henderson, director of marketing for Rockwell's network-access products division, points out that PCM technology will encounter similar problems to those faced by QAM-based products when dealing with lines that are extremely long or of poor quality. While PCM will be able to deliver superior performance in most situations, the actual speed they can support will be a direct function of the length of the line back to the central office.

Henderson also notes that both PCM and QAM modems will function poorly on lines that use extender coils. These are devices which are inserted into extra-long (usually over 18,000 feet) lines to keep their high-end frequency response at an acceptable level. Depending on which field study results you choose to believe, long-line effects will limit modem performance for 5-to-20 percent of U.S. subscribers.

Conclusions

Because PCM is a new technology, the subtleties of line characteristics that affect its performance are still something of a mystery. The solutions to these problems must be developed using theoretical techniques, then fine-tuned using experience gathered from real world situations. For example, during a series of wide-ranging field trials they conducted jointly with America On Line, U.S. Robotics discovered that line characteristics varied so widely that a single DC-suppression scheme would not work for all lines. To better assure compatibility with most users' telephone networks, they developed an adaptive DC-suppression algorithm.

Even if they don't live up to all the claims, PCM modems will play an important role in extending the life of the copper pair in the telephone system infrastructure found in nearly all of today's local loops. Fragmented standards will be a problem in the short run, but intelligently negotiated fall-back standards will ease early adopters' pain by assuring interoperability at V.34 rates. The same fragmented standards will drive most companies to develop software upgradable products, which either use on-board flash ROMs, or rely on RAM downloads from the host system on each startup.

The road to interoperability will be a rocky one, but it should smooth out relatively quickly, if Rockwell's plans are any indicator. Henderson indicated that Rockwell intends to put nonprogrammable, noninteroperable, modem chips, with their original K56Plus protocol, into developer's

PCM 101

PCM is a mature technology, used in ISDN local loops, switched-56 kbit data services, and countless digital-PBX systems worldwide. It uses analog signals to represent 8-bit digital words by dividing the line's rail-to-rail voltage swing into 256 discrete levels. Each data word is passed through an encoder (essentially a specialized D/A converter), and clocked out across the system using the tightly-synchronized 8-kHz master clock that forms the heartbeat of a traditional phone system. Within each 125-µsec window, the voltage on the line is sampled by a decoder and converted into a digital number, representing 7 or 8 bits of data.

Theoretically, one could expect that a PCM stream would transmit 64 kbits/s worth of data (8 bits of data × 8 ksamples/s = 64 kbits/s). Unfortunately, this isn't the case in the real world, partially because modems must be able to signal each other to control traffic flow, exchange error detection information, and renegotiate transmission rates as line condition changes. They accomplish this communication by using an in-band, or robbed-bit signaling scheme, which borrows some of the modem's data capacity and uses it to establish a dedicated control channel between the two modems. Most PCM protocols take 8 kbits off the top, because signaling leaves 56 kbits/s for the payload data stream.

Much like traditional modems, there's no guarantee that a PCM connection will be able to support its full 56 kbit/s rate. Part of the problem lies in varying line conditions, and part of the problem lies in the characteristics of the codecs used in PCM systems. PCM encoders and decoders employ a specialized compression algorithm called µ-law which was originally developed for digitally-encoding human speech.

If you've ever wondered why people sound as good as they do over phone lines with their relatively narrow bandwidth, it's due in good measure to µ-law codecs. These codecs take advantage of the fact that many of the nuances of human speech occur relatively close to the zero-voltage point. The µ-law algorithm is nonlinear, placing a greater percentage of its sample points closer together around the zero point, and fewer, more widely spaced sampling points at the extremes of its range.In PCM, it is the samples of the signal that are compressed and not the signal itself. This arrangement allows the most-often used portions or samples of the line's voltage range to enjoy a highly-effective resolution, while allowing higher amplitude portions of the signal take on a grainier character.

When a line's noise floor goes above a certain threshold, it becomes difficult to distinguish between different PCM levels, especially at the lower amplitudes where they are closest together. To combat this, the PCM codecs selectively remove some of the 256 available sample points when the bit-error rate goes above a preset threshold. While nobody knows precisely how they will actually work in real world conditions, some early studies performed by Texas Instruments indicate that we can expect the current generation of PCM modems to typically deliver 48 to 53 kbits/s.

hands as soon as possible. Next, they will offer a programmable chip set that will run the Rockwell/Lucent interoperability standard. The same chips could be upgraded, via software, to support the TR30 and ITU standards. Once the standards firm up, Rockwell intends to offer a less expensive, nonprogrammable chip set. This strategy should help get PCM modems out into the world as quickly as possible without burdening the standards process.

For the most cost-conscious applications, it will be possible to implement software-only PCM modems with host signal processing. It takes approximately the same (and in some cases fewer) MIPs to perform the PCM encoding and decoding. Products like PCTel's soft modem will find their way into laptops and other applications where power and space also are at a premium.

Charley Gonzales, marketing manager for telecommunication products at Texas Instruments, cautions, however, that a fully-host-based modem (PCM or V.34) can soak up 30% of the computing power of a 200-MHz Pentium processor, and up to 50% if it's only running at 133 MHz. This arrangement might not be suitable when you are performing computationally-intensive tasks while using your modem to communicate over the phone line (i.e. 2-way telegaming, telemedicine, or desktop publishing from a remote site).

Finally, it's hard to tell how much of the promised 56-kbit/s throughput rate the first generation of modems will actually deliver. It depends on many variables, including how the DC suppression problem is handled, what robbed-bit signaling protocol is chosen, and whether the FCC relaxes its EMI/RFI specifications for PCM in the local loop. One thing we can almost guarantee however, is that there will be at least incremental improvements in both upstream and downstream data rates as technologists gain real-world experience with this new application of PCM.

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TECHNOLOGY PERSPECTIVE

Software Modems: The Crossing Of A Communications Threshold

Large Market Shift Eases Modem Accessibility For End Users By Making Them Available As Software.

Larry Gerstner, Motorola, Information Systems Group, Software Products Div., 20 Cabot Blvd., Mansfield, MA 02048.

Successful products in the PC industry generally add new functionality to the platform at minimal or no cost, or provide existing technology at a lower cost. This usually is true with electronic products, but is especially apparent in the PC industry, a large, highly visible entry point for many new technologies. Because microprocessors double in performance every 18 months, opportunities to trade-off hardware for software, thereby reducing cost, are continually arising. However, a major threshold in this regard was passed recently when PSTN modem functionality, previously provided in largely dedicated hardware, made an initial move onto the PC's main microprocessor. This signaled a large shift in the market for modems and other communications products, which can now be delivered almost completely as software.

The last major shift in the modem market occurred in the 1980s, heralded by the advent of digital signal processors and the growth of the DSP industry. DSP technology delivered as chips became the building block that made high-speed (at that time 9600 bps) echo-canceling modems possible. There were many modem companies developing their own technology and adding value by tuning modulation algorithms and thereby differentiating products based on performance. This triggered the quick advancement of industry standards for high-speed modems starting with V.32 in the late 1980s, V.32bis in 1991, and then V.34 in 1994. In those early years, payback was fast regardless of the price and users were early adopters who derived much value from any increase in modem speed.

As sales volumes grew in the 1990s, another important milestone occurred as modem chip set vendors dramatically reduced the cost of modems by integrating the functionality of the entire modem into a handful of integrated circuits. Classic modem architecture included a DSP and associated SRAM for the data pump, a microcontroller and its associated SRAM for controller functions, and an analog front-end chip. Chip set vendors marketed these parts with their firmware and a reference design to show modem manufacturers how to put it all together. Until now, this was the prevalent architecture and business model.

The modem chip set era has been characterized by changing modem standards and the addition of related features. Voice and telephony features became modem functions, thus providing more potential for adding value. To deal with new standards and features, vendors have promoted various upgrade schemes. At worst, this meant physically changing a ROM chip on the modem. At best, they involved downloading new firmware to flash. Upgradeability in this situation is best suited for bug fixes and incremental feature improvements, because the horsepower on the modem's processors is fixed, upgradeability is limited.

Chip cost denies modem manufacturers the luxury of shipping DSPs with lots of processing power to spare for future functionality. This limitation practically disappears with purely software modems, which are as simple to upgrade as any other software. System limitations can still affect upgrades, but a relatively large pool of processing power and memory is available to perform many tasks of which communications is just one.

In addition to the classic modem architecture, some vendors tried other mixes of hardware and software as DSP-based modems evolved. A few put some or all of the control functions on the DSP with the data pump. Others moved all the controller functions to the PC's host CPU. This latter architecture, known as a controllerless modem, represents the last evolutionary step before software modems.

The software modem runs controller and data pump code on the host CPU *(see the figure)*. This is an architectural shift that represents a major new step function in the evolution of modem technology. Derived is a major reduction in system cost as well as a change in philosophy about communications functionality. While there is nothing new about the underlying modem technology, the move to the host processor of the PC is radically new and based upon the increasing power of the platform.

Powerful Processors Are Key

The Windows 95 Pentium platform is a powerful multipurpose machine optimized for data processing applications. Although the most common uses of the PC do not require real-time performance, users expect the PC to operate quickly and perform many tasks. The state-of-the-art PC has large processing resources on which to draw to satisfy users' requirements by and large. When the Pentium crossed the 100-MHz speed threshold, the possibility of using it to handle real-time applications such as modem operations without disrupting the end-user experience became a reality. To achieve this, developers had to work within the constraints of the PC architecture to meet user performance expectations.

Modem data streams require immediate attention from the processor when they arrive in the PC, making

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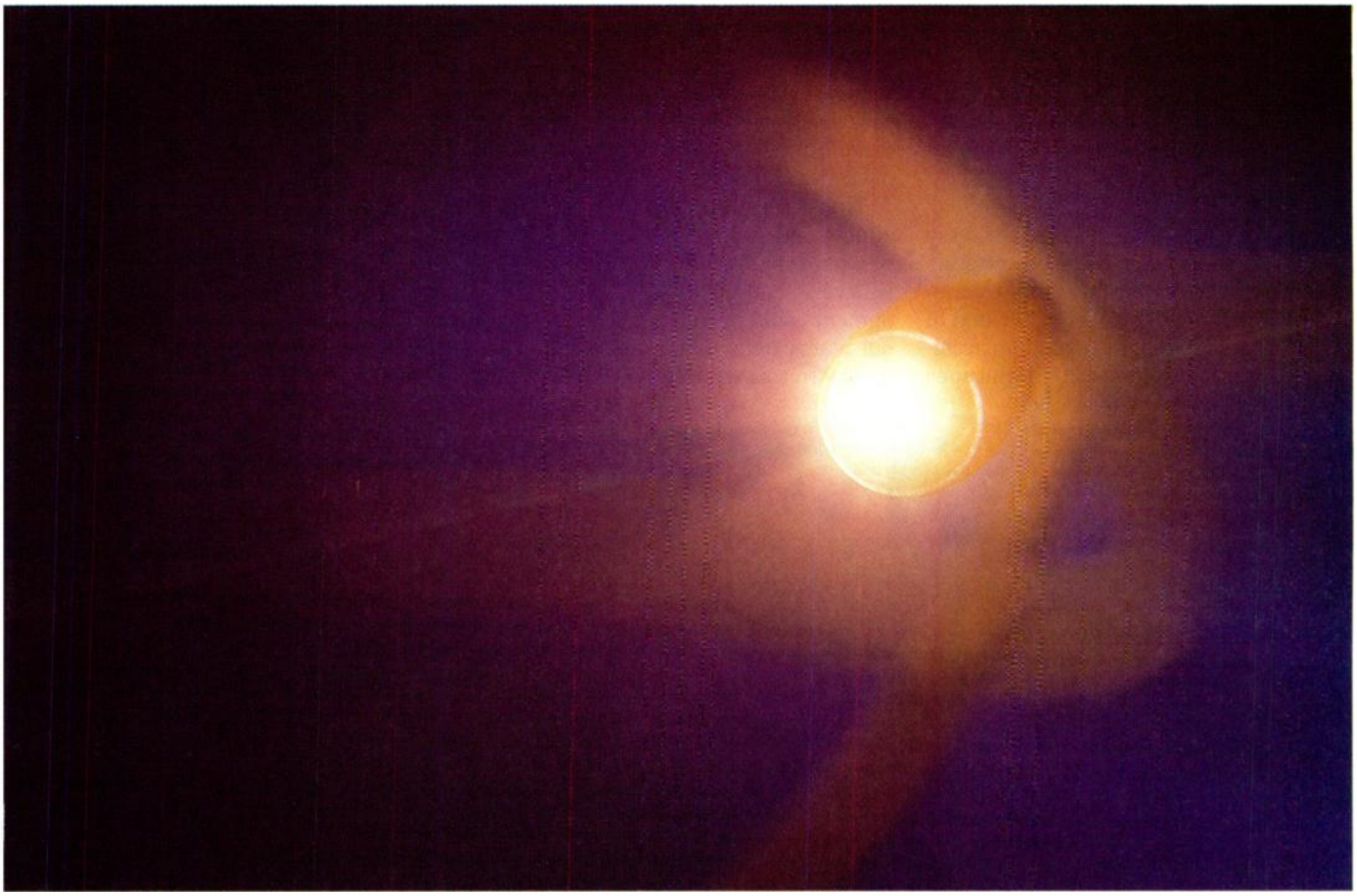

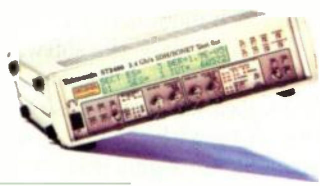

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them truly "real-time." Furthermore, the processor must perform all required operations on that data before the next series of data samples arrives. On a PC, user applications must execute in a timely fashion as well, or the user experience is unacceptable. Because the modem processing must be dealt with first, there must be sufficient processing overhead for the intended application.

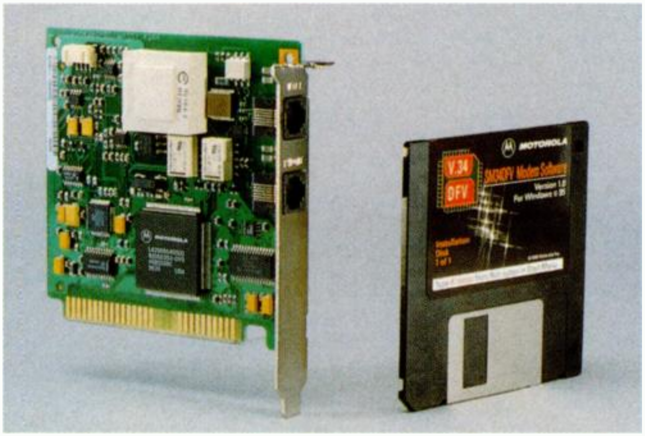
A road warrior using his notebook computer for e-mail needs relatively scant Pentium resources. Two interactive gamers communicating by modem are probably at the other end of the spectrum. Software modem architecture can accommodate both types of users and all those in between. This is accomplished by carefully crafting the V.34 modem to the Windows PC architecture. The design makes judicious use of the system's cache, floating point processing, and plans for long latencies that can be encountered. The software modem works well in what is now an inhospitable environment—and this environment will only get more friendly in time, with MMX, the windows driver model, and other enhancements.

What are the benefits of moving modem functionality to software? There are several, but again, one of the most important is ease of upgradeability for various reasons.

Communications speeds and standards have continued to change. Recently, 33.6 modems were touted as absolutely, positively, the fastest that analog modems could possibly get. Then came 56-kbits/s modems. At present, in the 56 kbits/s pre-standard period, no one is certain which implementation will be adopted or when. But software modems, with their small hardware interfaces, can be purely software upgradeable to any and all versions of 56 kbits/s modem up to and including the final ITU standard. With the software modem architecture, obsolescence is avoided, a welcome change in the PC and communications arena.

The changing landscape of simultaneous voice and data protocols makes another excellent case for software-based communications. For years, alternating voice and data, several proposals of digital simultaneous voice and data, and a couple proposals for analog simultaneous voice and data have slugged it out to be the chosen standard. The result has been marketplace confusion and little application development in an area where end users see compelling value.

Now if the hardware interface were simple and standard and all the various protocols could be provided as software, end-user application development could proceed unabated without worry about communication protocols. In this environment, when the application on each user's PC is ready to use a voice and data protocol, they query each other to decide the best one, load it in, and proceed.



This typical software modem from Motorola signifies a major step in the evolution of modem technology. It has the ability to run both controller and data pump code on the host CPU.

Pushing The Envelope Further

A key influence on the move of software modems into the market is multimedia. Multimedia PCs as a category have been around for several years, but early multimedia PCs had scant audio I/O and little else. Only recently, driven by games and the Internet, has the industry become serious about multimedia and real-time functionality. Soft modems will benefit from several structural changes being made to the PC platform to better support multimedia.

Key is a move made recently by Intel, which released its MMX extensions, adding 57 new instructions for signal-processing intensive applications. These instructions will greatly reduce the load of the software modem on the host processor. Similarly they reduce the load on the processor of other multimedia functions, leaving more room for all. MMX and analogous enhancements on other host microprocessors both acknowledge the importance of the DSP function for signal-processing functionality and signals its demise as a standalone component.

Another influence is AC97 (Audio Codec 97), developed by a consortium of PC audio technology providers and Intel. AC97 creates a standard architecture for controlling how audio comes in and out of the PC. The specification also defines an option for analog modem signals. This is appropriate since PC audio and analog modems require similar high-performance analog conversion. The resulting audio-modem codec will standardize the modem interface to the PC and drive down its cost. The modem codec practically rides along for free and makes soft modems even less hardware-dependent.

Microsoft also is taking steps to improve the PC's multimedia performance. Its Windows Driver Model for communications represents the most significant development for modem functionality. This model provides facilities for dealing with modem data streams in real-time. It defines the software modem interfaces at low levels as well as at the application level. These enhancements, along with the use of ActiveX components for signal processing, will make software modems even more welcome on the PC platform.

Other Opportunities

The PC is only the most prominent example of the opportunity for software modems. With the Internet as the key catalyst, demand for being connected is exploding. Network computers, TV-based web browsers, and handheld PCs challenge the PC's dominion over data communication to end users. This is especially true in the wireless communications arena where diverse protocols exist depending on service providers and national boundaries, software-based communications

has added importance.

Powerful, low-cost CPUs such as the MIPS, Hitachi SH and PowerPC families are more than capable of powering these new communications devices and running software modems. These devices, like all microprocessors, grow in power and shrink in cost with each succeeding generation. They, too, are extending their instructions sets to include DSP-type functionality and further ease soft communications integration.

Summary

The case for software communications is compelling. Software is easy, it's cheap, and it can be downloaded over the Internet. Software thereby addresses the end-user's fear of obsolescence by extending the life of their communications equipment. Processing power in host microprocessors has reached the point where soft analog modems are possible.

Processing power will continue to double every 18 months and communications modes and media will continue to proliferate. In the near future, one can envision desktop PCs with 500+ MHz microprocessors on them and all manner of specialized instruction sets.

It's easy to picture a cable modem or an xDSL modem provided largely as software. Users pick the best one based on service provision and their needs. Communications delivered as software will enhance the value and utility of the hardware on which it runs and help preserve people's initial system investment.

Larry Gerstner joined Motorola in 1996 as Marketing Manager for the Information Systems Group. He is responsible for planning, and marketing for new software-based communication products. Prior to joining Motorola, he was in charge of marketing at HTI Voice Solutions. He also worked at Analog Devices Inc. as a product manager for audio and communication solutions. Gerstner holds a BSEE from Brown University, Cranston, R.I., and an MBA from Columbia University, New York.

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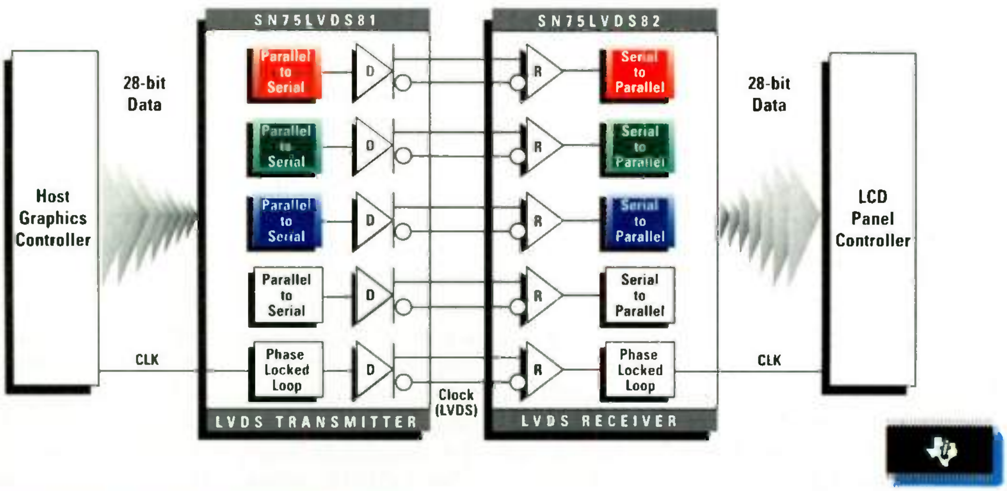

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TEXAS INSTRUMENTS

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1830-26

The DSLs: Sorting Out The Issues Behind The Technologies

An Insider's Guide To The Confusing Galaxy Of xDSL Technologies. Join Us As We Update Their Current Status And Compare Claims.

Rupert Baines, Analog Devices Inc., MS 116, Box 804A, Wilmington, MA 01887;. e-mail: rupert.baines@analog.com.

DSL—short for digital subscriber loop—is used to describe a variety of technologies that deliver digital data over twisted-pair lines at rates far higher than ever envisioned by the network's original architects. The original DSL was, of course, the Integrated Services Digital Network (ISDN), developed in the early 1980s. It squeezes 160 kbits/s into an 80-kHz bandwidth of local loop. ISDN uses a simple four-level phase/amplitude modulation (PAM) scheme with a "2B1Q" line code to reach a standard range of 18,000 feet, although more recent products use smarter signal processing to achieve longer range. ISDN has not been very successful in the U.S., but it has done very well in other countries, with Germany being a prime example.

ISDN was soon followed by HDSL (high-bit-rate DSL), which used the same 2B1Q modulation but on a larger bandwidth and with a lot more sophisticated DSP, to deliver much faster rates over a carrier-serving area (CSA) range of 12,000 feet of 24 AWG wires. HDSL most commonly operates with two pairs to deliver symmetric TI or E1 rates (1.544 or 2.048 Mbits/s), which it does by sending half the data on one pair and half on the other, both operating as full-duplex echo-cancelled links (with either 768 kbits/s for T1 and either 1168 or 1024 kbits/s for E1).

An Improved Pipeline

HDSL is a lot simpler and more robust than the old T1 service, which required repeaters every few hundred yards and was consequently difficult to install and maintain. As a result, it has essentially replaced T1, and the odds are good that if you have recently gotten a "T1 line," it was actually HDSL. (To be strictly accurate, you should refer to DS1—digital subscriber rates 1—for rates or services, while T1 refers to the older physical implementation using alternate mark inversion (AMI)—line code on two simplex connections). As well as high-speed data connections, HDSL is popular for connecting wireless base stations into the public switched telephone network or PSTN (multiple connections and a lot cheaper than fiber) and for "pairgain" applications, i.e., squeezing many voice channels onto one piece of copper.

In Europe, the standards body, ETSI, defined in their HDSL technical report what was essentially a family of HDSLs, all delivering E1 rates using the same 2B1Q line code, and operating on four, three (old but still used), two (nowadays the usual) or one pair of wires. (There also are definitions for 1- and 2-pair CAP systems). This has the advantage of being straightforward and simple, but each implementation would have a different reach, with a single pair falling perhaps 10 to 20% short of the CSA range. In Europe, where loops tend to be much shorter than in the U.S. (especially in Italy or Germany), this is acceptable.

ANSI is leading the discussions on next-generation HDSL—HDSL2 (although ETSI has opened discussion on an enhanced HDSL, which perhaps will support some rate-adaptive approach, they are most probably probably going to wait and look at ANSI's proposal before making too many decisions). This has the target of being a technology that will last, delivering T1 rates over a full CSA range with the reliability that has been proven with HDSL (it is possible that this should support rate-adaptive services too, allowing lower-speed access even on longer loops).

The difficulty is in meeting the range and strict latency requirements while still maintaining spectral compatibility and coping with real-world noise and interference. Latency of less than 500 m s is mandatory for many existing services—a tough requirement. A clearly defined CSA range is necessary for operational reasons, since the telco's customer databases often only classify distances as "within CSA? yes-no." If a customer requests a service, that is the only test if they can get it or not.

The expectation is that agreement will be reached over the next few meetings, with Pairgain, Level 1, Globespan and others close to a consensus. Due to latency, a multi-carrier system is unlikely, and the discussion on line code seems to have converged in favor of a single carrier technology (e.g., coded 64-point carrierless amplitude/phase modulation (64-CAP) or quadrature/amplitude modulation (QAM)). The uncertainty is more over error-correction and coding techniques, but all of the proposals exhibit impressive performance, with demonstrated achieved coding gains of some 5 to 6 dB (at least one vendor is using Turbo codes—probably the sexiest idea in information theory today).

A Galaxy Of DSLs

While the above are all standards (or quasi-standards), several companies have lower-speed/lower-price variants being proposed. Many simply consist of using half an HDSL chip set on a single line (e.g., to give 768 kbits/s, while others are new developments, targeting slower applications, such as 512 or 384 kbits/s). These are discussed for Internet ac-

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cess or low cost pairgain—especially in less-developed countries—and examples include MDSL (moderate-speed), PCM-n or Brooktree's DSL/384. Most importantly, all of these technologies are loop-powered (i.e., they receive their power from the central office), and all use the POTS band for data. While you can have voice, it needs to be incorporated digitally, and is not the transparent/backwards-compatible approach of ADSL.

Although some people use SDSL (symmetric DSL) to describe single-pair HDSL, it may preferable to use the somewhat-oxymoronic symmetric-ADSL by changing the up/down allocation of normal ADSL chips to give the same rate in each direction. Significantly, this interpretation means it operates over POTS and need not be loop-powered (both unlike HDSL).

Depending on crosstalk, this could deliver 1+ Mbits/s in each direction, and operate over the full CSA distance; however, it has not yet been standardized or widely available. As mentioned earlier, crosstalk is a VERY big "it depends" for the future of symmetric ADSL, since crosstalk more than any other factor limits how well a service will operate. There also are important issues surrounding general spectral compatibility that would need to be resolved. The standards bodies have not decided on this although at least one supplier is marketing such a product.

Standards Issues Abound

DMT-based ADSL has been standardized by both ANSI and ETSI—the T1.413 was published in late 1995 and is a very comprehensive specification, describing all manner of issues with ADSL from physical modulation, to coding, framing and management type operations. Discussions are now very well advanced on Issue 2 of this specification, and all the substantive items are likely to be frozen in the next few weeks, leaving editing and organizing before the new edition of the standard is published next year.

Most of the changes have been in updating the standard with the benefit of the last two years of practical experience, and updating it to reflect changes in the market. For example, incorporating more support for data-mode services and Internet, rather than the video-focus of the first version. Despite some comments, the standard is extremely well suited to data services without major change, but the document will be updated to include more details.

Another change is to describe rate-adaptive ADSL (in a marketing coup, one manufacturer appropriated the acronym "RADSL" for this; a bit of a surprise for the rest of the industry which had always had a rate-adaptive ADSL!). The omission is not in the technology, as T1.413 has a good description of how discrete multitone modulation (DMT) adjusts the rate in 32 kbit/s steps, but rather in standardizing the training and management protocols to ensure interoperablity between different rate-adaptive modems.

The other change in the standard will be to follow the lead of the ATM Forum and to separate the standard into parts dealing with PMD (physical media-dependent) and TC (transmission convergence) sub-layers. This may only be an editorial change in Issue 2, but it paves the way for more detailed specifications of ATM over ADSL or packet-mode operations in future texts.

The big debate within ANSI is over the introduction of a second line code: whether the standards body should stay with DMT only, or should support two flavors of ADSL and document a version of the CAP system *(see "Line code debates," p.142)*. The situation at the time of this writing is that the main group of T1E1.4 decided to stick with the status quo, but that a parallel ad hoc group has been established and is working on documenting the CAP system.

A Fat Upstream Pipe?

Some people have discussed "Reverse ADSL"—simply swapping two modems so that the high-capacity direction is from the home to the central office (CO). Unfortunately, this is not going to work in most cases. ADSL relies on all the "loud" signals being located together (e.g., downstream transmissions are all toward the CO), and all the weak received ones being located in a different frequency area, and physically separated. If you reverse this, then at the CO, the loud "send" of everyone else's downstream will be right where your reversed system is, trying to listen to a very weak signal with the attenuated noisy weak high-capacity "upstream" signal drowning it out. Conversely, your transmit signal will swamp everyone else.

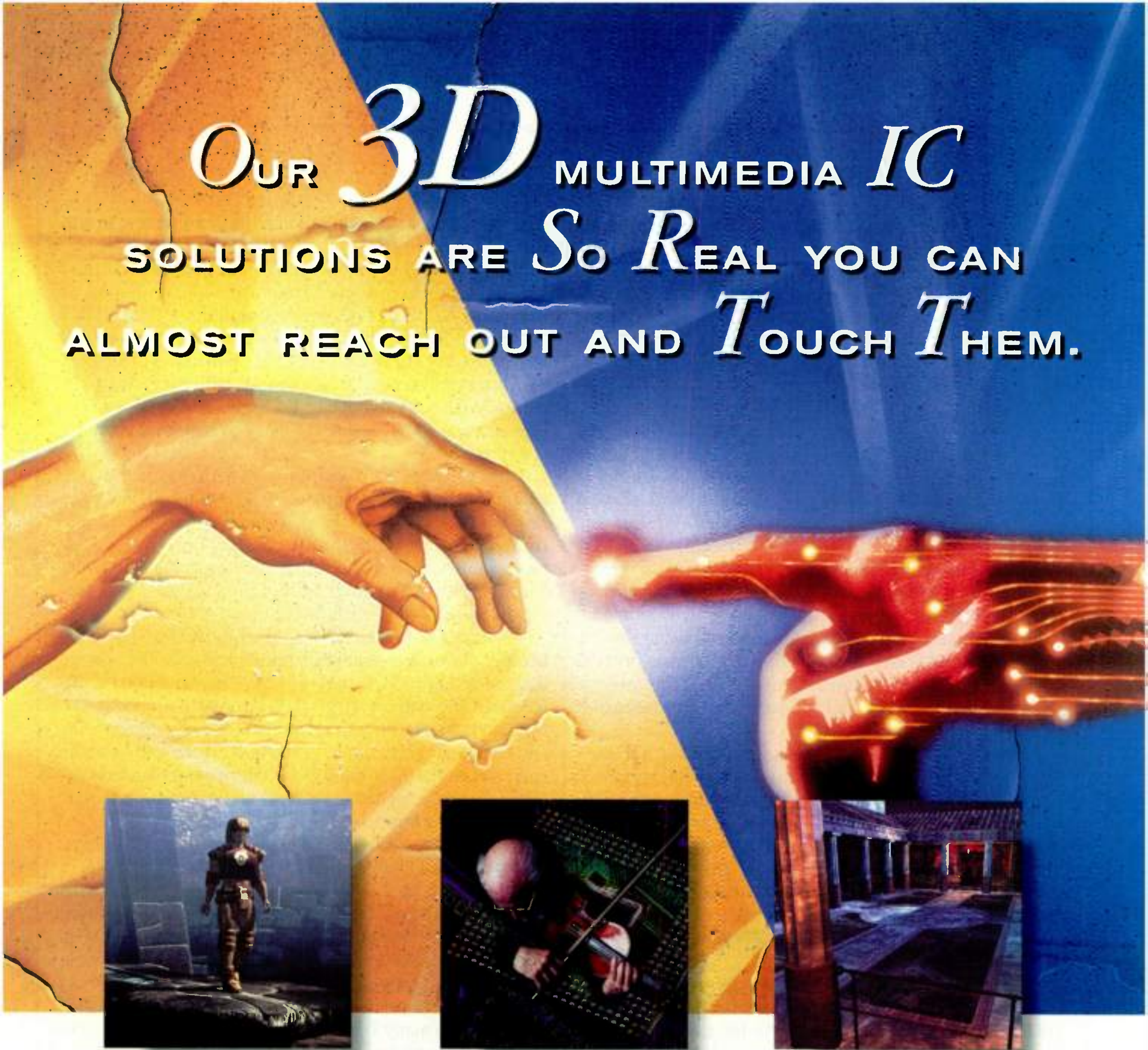
Given spectral compatibility constraints and considerations for "good citizenship," this will limit reverse ADSL to perhaps 1000 ft. Of course, up and down are arbitrary—what matters is everyone has to operate in the same direction. It is a little like driving; in the U.S. people drive on the right; in the U.K. they drive on the left—either is fine, so long as you are consistent!

Super-Fat Pipelines With VDSL

Finally, there is VDSL (very high-speed DSL). While there is still much debate over the specifics, the gist is clear enough. VDSL is intended as the last drop, operating over copper, in applications such as fibre-to-the-curb (FTTC) or fibre-to-the-building (FTTB), where the head-end will be located in an optical network unit (ONU) at the end of a length of fiber. It operates with very high data rates, but over short distances: 51 Mbits/s over 1000 ft. or 25 Mbits/s over 3000 ft. are typical. Intriguingly, even though the data rate is higher, it is likely that the shorter distance and more controlled environment may make this easier (and potentially cheaper) to implement than ADSL.

Various bodies are discussing how to actually implement VDSL, including ANSI, ETSI and DAVIC. This has resulted in virtually every combination of line code, specification and access method being suggested. For example, while most suggest that an asymmetric system with perhaps 10:1 ratio is adequate, some prefer a fully symmetric system, and others are flexible. Within ANSI, there are a few main proposals. Amati is championing "synchronous DMT"—a ping-pong modulation method that uses time-division duplexing, where the transmitter and receiver alternate roles.

The attractions are that various asymmetries can easily be supported,



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Line Code Debates

The line code (modulation method) for ADSL has been a topic of heated discussion among engineers, with people taking steadfastly rigid sides on the subject. In January 1993, Bellcore (with BT and NYNEX) organized the "ADSL Olympics" as a test, to compare the three main candidates: DMT (discrete multitone), CAP (carrierless amplitude/phase), and QAM (quadrature amplitude modulation).

While they were perhaps not completely authoritative (there are continued complaints it was not a fair test), the results of the trial indicated DMT had better performance, and the ANSI committee made its choice on that basis. Had the stakes not been as high as they are, that might have been the end of it, but that was not to be...

QAM is a very well understood and widely-used modulation technique. In essence, it is a single carrier signal, where the data rate is split in two and modulated onto two orthogonal carriers (I and Q) using sine/cosine mixers, before being combined and transmitted. CAP is very closely related to QAM—indeed, the two can be considered identical and compatible; the difference is primarily in the implementation.

Instead of the two signals being generated by a sine/cosine mixer, the modulation of the orthogonal signals is performed digitally using two digital transversal bandpass filters with the same amplitude characteristics and a p/2 difference in phase response (Hilbert pair), before being combined, fed to a digital-to-audio converter (DAC), and transmitted. The advantage over QAM is that the digital implementation can be realized very elegantly in silicon, and there is great scope for flexibility or efficiency in the implementation.

Being a multicarrier modulation system, DMT is a very different animal. DMT (essentially the same as OFDM—orthogonal frequency division multiplexing) divides the frequency range up onto a large number of discrete bands, or sub-channels. Each of these is independently modulated—with a carrier frequency corresponding to the center frequency of the bin—and the system uses them all in parallel, all at the same time.

The multi-carrier modulation technique requires orthogonality between all the subcarriers. A very elegant way to achieve this is by using fast Fourier transforms (FFTs). In ANSI standard DMT, there are 256 subcarriers, each with 4-kHz bandwidth, that can be independently modulated from zero to a maximum of 15 bits/Hz. This allows up to 60 kbits/s per tone. At low frequencies where the copper's attenuation is low and there is a good signal-to-noise ratio (SNR), it is easy to use a very dense constellation—10 bits/Hz is typical. Where the line is in worse condition, the modulation can be relaxed to allow for the lower SNR—perhaps to 4 bits/Hz or less, to give the necessary noise immunity. Furthermore, as the modem measures the line, it can avoid or compensate for crosstalk or interference. For example, an adaptive system can reduce the modulation in the band where an AM station is causing RFI.

The two techniques can be considered as duals: QAM/CAP techniques are frequency domain-based, as they have fast symbols, each lasting a short time, with a big bandwidth *(see the figure)*. For example, in a 6-Mbit/s DSL scheme, the symbol rate is 1088 baud— roughly about a symbol per microsecond—modulated to 256 points, with a bandwidth of 1.4 MHz. The short symbol time increases CAP's susceptibility to time-domain noise interference.

DMT is a time-domain approach, with symbols lasting a long time but only occupying a narrow frequency band *(see the figure, again)*. With a leisurely 250-ms symbol time, a 256-tone DMT system (4 kHz per tone, 1.1 MHz total bandwidth) needs only a 4-kbaud symbol rate to deliver 6 Mbits/s! This long symbol time makes it less susceptible to time-domain noise.

As duals, the two should, in principle, achieve the same throughput on a channel (Shannon's law does not specify line code). In practice, they will have implementation differences and will be affected differently by noise in the time domain or frequency domain—so real performance and complexity will differ. A single RF tone will be averaged across the wide band of a single carrier system—effectively rendering these systems highly resistant to narrow-band interference.

In contrast, a narrow-band signal will directly hit a subcarrier on a DMT system. This effect is clearly seen in VDSL, where the higher frequency range overlaps with the amateur radio ("Ham") operator's bands and a system must cope with strong pulses of narrow-band RFI. The reverse is true for a wideband noise signal—for example impulse noise burst from lightning, a hair-dryer or an electric light dimmer—which will be averaged across a short time on many DMT symbols, but will seriously clobber a single carrier symbol.

Both use error correction and interleaving to deal with these problems, and both are very effective. DMT claims an advantage in that time-domain noise is hard to predict, while RFI tends to be more stable and can be measured and adjusted for during training or operation.

There are many discussions on the relative advantages/disadvantages of CAP & DMT. A reasonably impartial summary of these is:

- DMT can direct information to subcarriers and modulate them independently, while CAP has a single carrier which has to be treated as a whole, even though the channel characteristics vary widely. As a result, DMT may deliver better performance or be more spectrally efficient. DMT has more complex initialization and needs more start-up time than CAP.
- DMT is inherently and straightforwardly rate-adaptive, delivering the maximum data for any given line. This

(continued on page 144)

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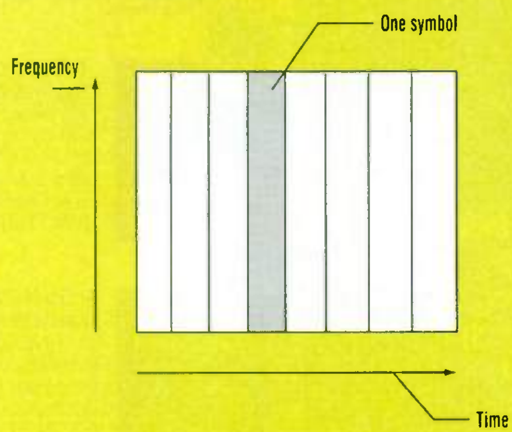
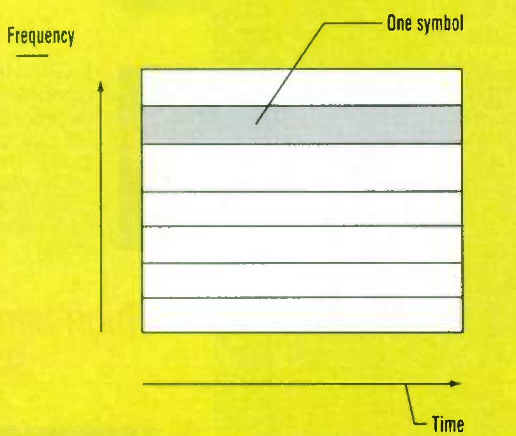
(continued from page 142)
method offers the flexibility to support higher rates over shorter loops (e.g., 8 Mbits/s), or sub-rate connections at very long reach.
•While CAP can support rate adaptation (by varying the constellation and the bandwidth), it is less obvious and requires more careful design of the analog circuitry. In addition, the rates have much lower granularity
•DMT steps in 32-kbit/s steps from 64 kbits/s to 8 Mbits/s, versus CAP's 320 kbit/s steps from 320 kbits/s to 7 Mbits/s. "DMT can be compared to a first-rate mountain bike—it has more gears to cope with the more different terrains it will encounter"
•DMT has much greater latency. This may actually be in violation of some specifications for particular services (e.g., ISDN).
•CAP is more resistant to RFI, although it is possible that DMT is more adept at coping with multiple or varying RFI sources. CAP has a lower peak-to-average ratio, simplifying the design of the analog stage and reducing its power needs.
•It is simple for DMT to meet an arbitrary or variable power mask spectrum for spectral compatibility.
•Echo cancellation in DMT is more difficult.
•DMT has greater immunity to impulse noise than CAP (as the symbols are longer).





•CAP can be simpler or optimized to a specific application. DMT is more complex, but this supports more versatility and flexibility (important in ADSL with many applications and a wide range of environments).
•DMT's analysis and measurement functions can be used as diagnostics and testing (e.g., to detect out-of-spec systems, or for preventive maintenance of the copper lines.)
•Engineers have more experience with CAP (QAM) and more specialized equipment exists—this may accelerate design and test of systems.
•Both are patented techniques, and intellectual property situation is comparable.

To give readers an idea of how these advantanages and disadvanteges translate into real-world implementations: CAP chip sets and DMT chip sets are approximately the same price, and will draw similar power. However, DMT is almost 50% more efficient than CAP, requiring 1.1 MHz for 6 Mbit/s throughputs, rather than 1.5 MHz. It is hard to compare performance as few results have been made public at the present time. . The only independent public tests I know of were conducted by GTE Labs and the magazine *tele.com* on an a number of ADSL systems. Interestingly, not a single CAP supplier was willing to submit modems for such impartial testing, but we can assume they'll be similar.

In summary, there is no single answer. This is an engineering decision, and the best technology depends on the needs of the application, and the tools to implement it. In general, while CAP can be simpler and is easy to optimize (in cost and power) for a particular situation DMT is more complex and more versatile. Given the wide variety of applications and environments ADSL faces, this can deliver several benefits in real implementations (obviously CAP can be designed to incorporate similar flexibility, but then it ends up with additional complexity!). However, for the more defined constraints of HDSL and VDSL, single-carrier approaches look more suitable.

To a large degree, it doesn't matter. Both technologies could work reasonably well, and will deliver roughly similar performance at roughly similar costs. It is fair to say that to date, most systems have been based on CAP, simply because as a single-source proprietary product, it had a significant time-to-market benefit (no need to wait for painfully slowly standards to thrash out a consensus) and hence was available sooner.

On the other hand, DMT is defined as ADSL—it is the only method that has been selected as the international standard (for good reasons), defined, and documented by non-proprietary groups ,supported by multiple manufacturers and interoperability. In an industry as international, as standards focused, and with the need for interoperability that characterizes the telecommunications industry, that may be all that is necessary to carry the day. In any case, the public will most likely be the biggest winner as DSL and CAP begin to give more and more citizens high-speed access to the information networks shaping our future.

by simply varying the duty cycle of send/receive. Secondly, the complexity is lower: little effort is needed to separate signals (i.e., no filters are required), and hardware can be shared at each end—swapped between transmitting and receiving as required.

On the other hand, DMT is perhaps more power-hungry than is desirable in the power-limited environment of an ONU. Secondly, the ping-pong system must be very tightly controlled between all systems (if there is any difference or jitter, a transmitter will swamp a receiver)—this might be difficult in a deregulated environment with competitive access. Finally, there is some concern that the proposed ping-pong frame rate (2 kHz) might be demodulated into an annoying audio-frequency signal (perhaps in an adjacent pair, which might not have a VDSL-splitter or filter). This has been claimed to occur with TDMA digital cellphones, where the burst frequency is detected in hearing aids.

A number of manufacturers are supporting a frequency division duplex system, with CAP for the downstream. This has the advantage that it is a low-power solution, and can be optimized to give a simple transmitter. Being a high-capacity broadband signal, it also is resistant to RFI and can be placed in a region where there is less concern with impulse noise.

Manufacturers including Analog Devices, Aware, Orckit, BBT, Globespan, Broadcomm and others all are developing a common draft standard based on this technology. (Importantly, the first three have all developed DMT solutions for ADSL, showing that line-code choices can be decided by technical criteria and are not unchanging). However, the consensus breaks down for the upstream. Some manufacturers are proposing single carrier techniques (CAP or QPSK) which have the attractions of low power and simplicity. On the other hand, in the home (where the upstream signal starts), low power is not as critical as it is in the ONU, so this is of less use.

Coping With Noise

Then there is the problem of noise, and how to deal with it. The low-frequency bands can be very noisy, with a lot of impulse noise and ingress from sources like electric light dimmers, vacuum cleaners, and the like. This can inflict a lot of grief on a system, in the form of noise that is very hard to filter out or work around. To get around this, some systems (for example, DAVIC 1.0's FTTC) place the up stream signal high in frequency—above the downstream. Here the system avoids the low-frequency wideband noise, and the filtering can be easier (reducing the waste from a large guard band).

Unfortunately, this region has lots of attenuation in the copper, reducing the useful capacity of the system; the DAVIC system only has 1.6 Mbits/s upstream and it is doubtful if the same arguments would work for higher rates of say 3 Mbits/s. In addition, the (narrow) high-frequency upstream link is now very vulnerable to notches in the channel caused by bridge taps.

Recognizing the very different characteristics of downstream (power constraints, high-speed/high-band-width) and upstream (lots of impulse noise, concern on frequency plan), Analog Devices, Aware, and BBT have proposed a hybrid solution, that uses very different techniques for each direction—hopefully getting the best of both worlds.

By adopting a CAP single carrier for the down-stream channel, the benefits listed above are achieved. The upstream is located at low frequencies, and uses a new multi-carrier technique—discrete wavelet multitone (DWMT). This copes extremely well with impulse noise, so the frequency plan can use the "good" low-frequency copper without worrying about noise. In addition, the technique easily lends itself to support multidrop in-home wiring (multi-point to point/passive network architectures).

Rupert Baines is the product manager for the ASDSL Products Division at Analog Devices Inc. He joined ADI in 1993, and holds a MSEE degree from Hull University, England, and an MBA from IESE.

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UPDATE ON COMPUTER-TELEPHONY INTEGRATION

New Architecture Promises "Object-Oriented" Hardware And Software For Computer-Telephony Integration

The introduction of a highly layered multiprocessor, multiresource architecture may bring some harmony to the tumultuous world of computer-telephone integration (CTI). Until now, applications such as voice response services, fax-back services, and automatic call processing have been pretty well tied to a specific processor, and often a specific hardware platform. Dubbed "DM3" (Dialogic Mediastream 3rd Generation) by its creator Dialogic Corp., Parsippany, N.J., the new architecture is a collection of specifications that can be used by independent technology and application developers to develop specialized media stream processing elements for use on the Dialogic platform.

Much like semi-custom cells used in ASIC chips, these specially-developed CTI functions can be combined with off-the-shelf software to create custom-featured applications with a minimum of development time and cost. Thanks to a nearly object-oriented interface between each layer, applications and resources can be easily combined and run on hardware platforms with a variety of processors and bus architectures.

DM3 was developed to simplify development for CTI systems based on the signal computing system architecture (SCSA) standard. SCSA treats CTI systems in a,layered manner, breaking them down into applications, CTI firmware resources, and hardware platforms. DM3 operates at the resource level, providing a uniform interface between the applications they serve and the hardware platforms they run on. It can be used to build embedded media stream processing resources, which reside below the application level, or service provider interface (SPI).

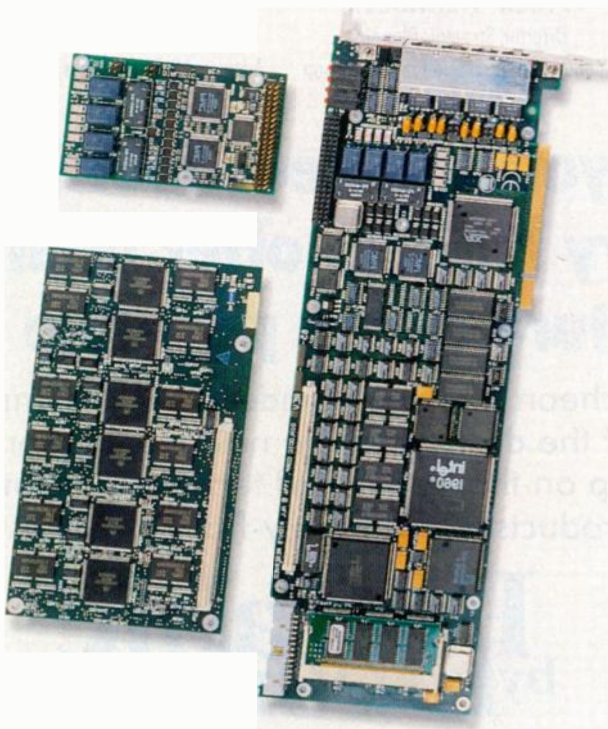
Some typical processing functions running on the DM3 architecture may include types such as speech recognition, call control, text-to-speech, audio player/recorder, fax, text-to-speech, or processing of SS-7 protocols. These CTI firmware resources can be accessed and shared among higher-level applications via a standard or custom "middleware" interface. By using a layered approach, the DM3 architecture concerns itself with the lower layers of the system and isolates the firmware resources from the vagaries of a specific platform.

On the hardware side, DM3 uses a pair of memory-mapped interfaces between the host system bus and the board's control processors, and a similar interface between the controller and whatever DSP resources are placed on the board. By establishing a uniform interface between them, any portion of the system can be replaced or upgraded at will.

The glue that ties the processors together is a collection of standard subroutine calls known as the "DM3 kernel." This standardized interface permits a controller to pass a media stream to a processor, along with a description of the operations it wants performed, without knowing its specific location or characteristics. Resources written to run on the DM3 kernel can be easily ported to more advanced processors as they become available.

Libraries of these resources can be obtained from Dialogic or other developers. From these resources, platform-independent applications can be developed on a variety of host systems. These may include telephone functions such as a voice-driven personal assistant, an automated call-processing center, or a voice-over-Internet system. These would be created on the host using high-level programming languages such as C or C++. The applications can be used "as is," or can be further customized by systems integrators using Visual Basic, C, Java, or commercially available custom toolkits.

The first DM3 board to be introduced during the first quarter of this year will support an array of up to 18 of Motorola's 56030x DSP units, or up to eight Motorola 603e PowerPC RISC chips. The processors are mounted on a detachable daughterboard and communicate via a mem-



Up to 18 Motorola 56030x DSP ICs, or up to eight Motorola 603e PowerPC RISC chips can be mounted on this detachable daughter board, allowing independent application developers to design specialized media stream processing elements. The DM3 interface board from Dialogic makes possible object-oriented hardware and software for the integration of computers and telephones.

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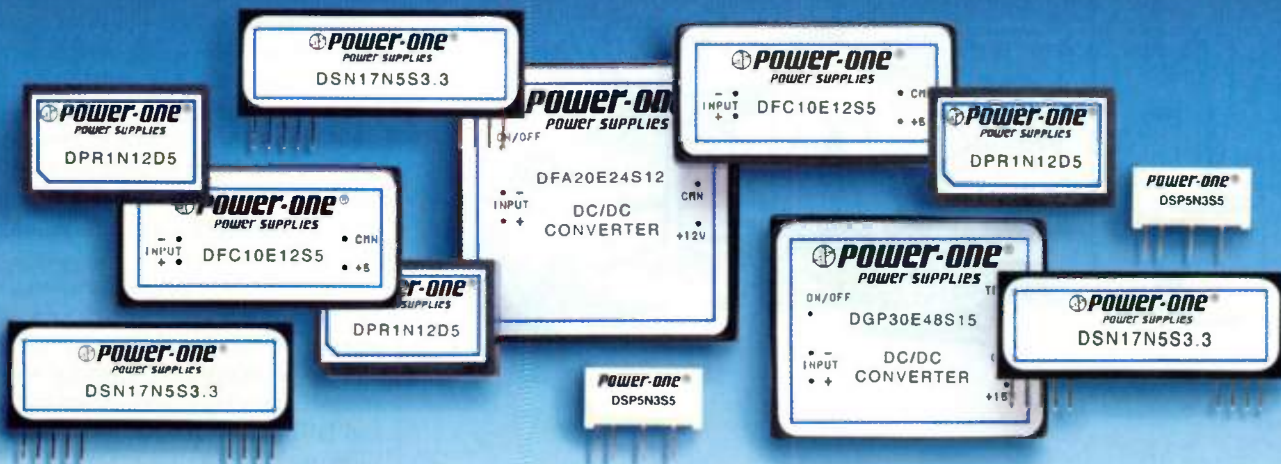

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ory mapped interface, permitting the easy addition of more processors or the integration of other processor types as the need arises *(see the figure)*.Depending on the particular model, the motherboard contains the bus interface for a PCI, compact PCI, or VME host system, as well as line interfaces for multiple T1, E1, and ISDN primary rate interface (PRI) lines. A standard SCbus interface permits the transport of up to 2048 call channels between boards. This scaling process arrangement permits a designer to process as few as four and as many as 120 voice channels using just a single card.

Opportunities exist for developers with unique telephony or signal processing expertise to create their own DM3-compliant modules. This one-time development effort creates a product which can be sold for use on a variety of processors and host platforms under both Unix and Windows NT environments.

Competitively-priced development kits provide the hardware and software that will enable resource technology developers to rapidly create and integrate high-performance RISC and DSP-based firmware resources. Bearing the moniker "DM-Fast," a complete set of integrated development tools is available for creating resources that run in standard real-time operating-system environments. Tools are included for writing DSP code under the SPOX operating system, and code for RISC machines under Wind River System's VX works.

OEM integrators will benefit from DM3's open computing environment. This allows them to directly interface their CTI application to Novell or Microsoft network resources and industry standard management tools. Besides eliminating the need to redevelop basic network resources, a CTI system that adopts this open-systems approach can be configured, managed, and upgraded like any other network resource. This greatly reduces time-to-market, development costs, and the cost of ownership for customers.

For further information, contact Dialogic Corp., 1515 Rte. 10, Parsippany, NJ 07054; (201) 993-3000; fax (201) 993-3093; Internet: http://www.dialogic.com.

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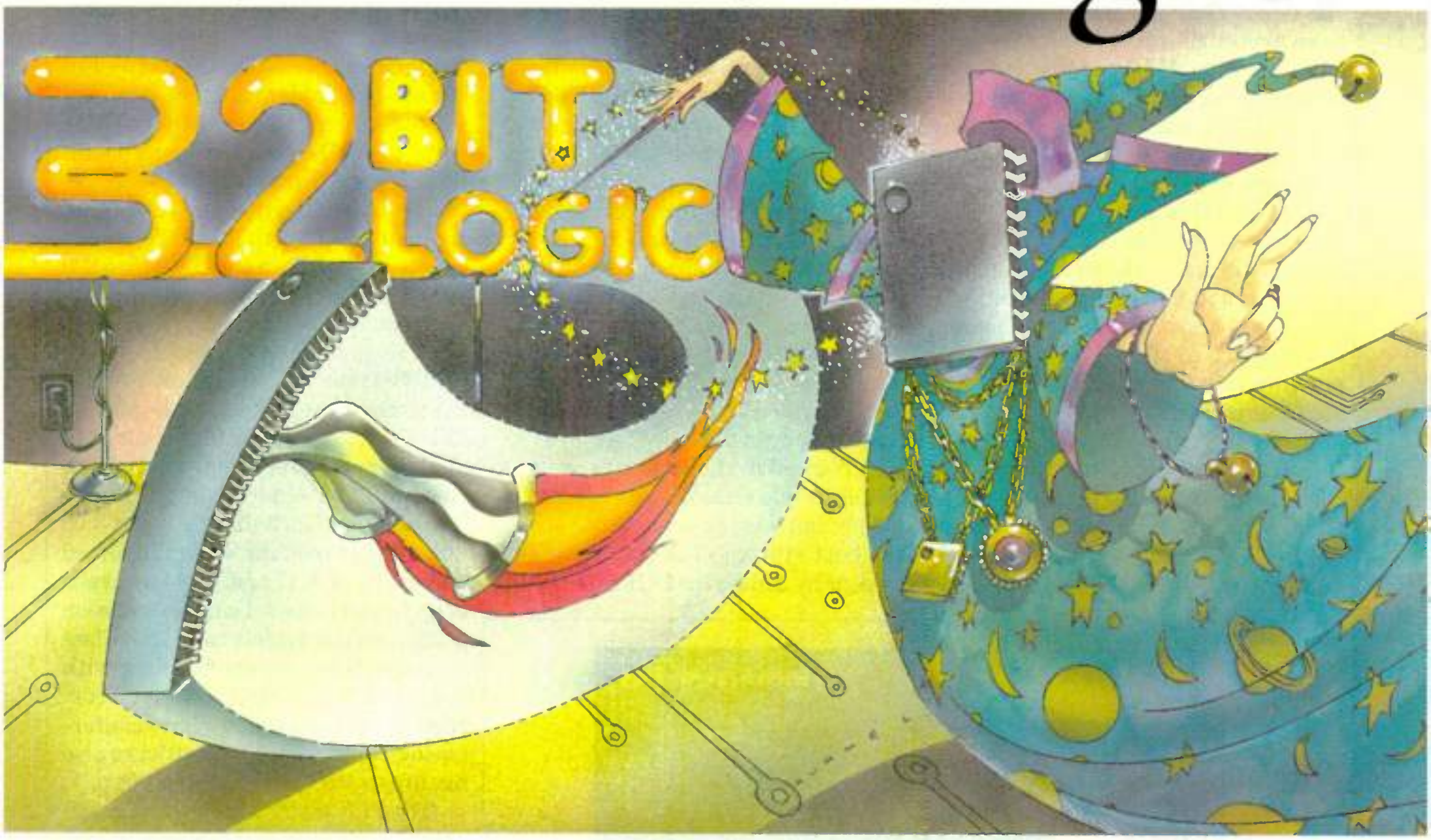

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PRODUCT FEATURE

Software PCM Modem Delivers Low-Cost 56-kbit Speeds, Speakerphone, and Simultaneous Voice/Data

The new breed of 56-kbit/s modems can now be implemented at a fraction of their previous cost, thanks to an almost all-software solution that uses surplus MIPs from its host processor for most critical functions. The PCT388P is a high-speed host-signal- processing (HSP) modem chip that supports both the established ITU-T V.34bis protocols and the newer 56 kbit/s technology.

The chip can perform all standard data, fax, and voice communications functions without the DSP data pump, controller, UART, and memory components found in most modems. Instead, it uses an inexpensive ASIC and specially optimized processing software that will run on any Pentium-class processor of 100 MHz or faster. On a typical 200-MHz Pentium machine, the modem requires around 25%, and less than 20% on an equivalent machine with MMX architecture.

Capable of operating under a wide range of operating systems, (Win 3.11, Win 95, NT 4.0, and OS/2), the first samples of the modem software will initially support a propriety "HSP 56," 56-kbit/s PCM modem protocol. Upgrades will support the TIA's "V.PCM" and the evolving ITU standards within two to three months of their release. Besides its modem and line interface circuitry, the PCT388P includes all of the logic required to attach it directly to the host system's ISA bus. The only other hardware required for a complete PCM modem are a set of off-the-shelf codec and line-interface chips, and a handful of passive components.

Advanced modem features, such as simultaneous voice/data and speakerphone, can be supported using either the host system's full-duplex sound card, or by adding the PCT144I DSVD vocoder/speakerphone adapter chip. The PCT388P features on-chip logic to support the plug-and-play (PnP) interface and its associated 16-bit PnP address, making it easy for the end user to install. The modem also can perform auto-selection of the computer's COM ports and IRQs necessary for its operation. The software is configured to respond to the full body of Ties AT modem commands. A virtual UART allows data-transfer rates as high as 115 to 200 kbits/s between host and modem.

In addition to supporting the newer PCM technology, a modem using the PCT388P and associated software remains backwards-compatible with all ITU and industry standards for data modem and fax equipment. This includes ITU-T V.34bis specifications for data rates including 28.8 and 33.6 kbits/s. Fax modulation is supported under ITU-T V.17 and V.29 for speeds of up to 14.4 kbits/s. Data compression using both the V.42bis and MNP Class 5 protocols is supported, along with V.42 LAPM and MNP 2-4 error-correction protocols. For video-conferencing applications, the software also features a V.80-compliant interface.

The PCT388P's low (75 mW at 5V) operating power and low component count make it ideal for applications such as laptop computers, where both space and power are at a premium. Automatic power-management functions make further energy conservation measures easy. Packaged in a 100-pin PQFP, the PCT388P is sampling now, with full production scheduled for June, 1997. Its companion, the PCT144I DSVD/speakerphone ASIC, is available now. The total cost of a basic 56-kbit modem should be under $35, including pc board, passive components, and assembly. Adding speakerphone/DSVD capability with the PCT144I will bring up the price to around $40.

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GOLFING NEWS

by Mike Hensen

Two New Driving Irons Challenge Woods on Distance. One Sets a World Record; the Other Is One Yard Short.

Patented Surfaces Automatically Correct Hooks and Slices

Trouble with Woods? *These Are for You*

YALESVILLE, CT– The same small Connecticut company that created a golf ball that *flies* too far has introduced two new driving irons that *hit* too far; way too far if you happen to sell woods. Mike Smith, a PGA Pro, recently set a World Record off the grass with the company's 17° driving iron, and stopped just one yard short of matching the record for a *driver* with its 12.5° counterpart. His shots were 335 and 358 yards respectively.

These are troublesome distances for wood manufacturers, but that may not be their biggest worry. *These clubs keep the ball on the fairway*, a characteristic drivers and fairway woods sorely lack. Official statistics show that even the top ten money-makers on the Tour miss the fairway with their driver 25% of the time. So don't feel alone if you have trouble with your woods, relief is on the way. A company spokesman told me this.

PATENTED "INVISIBLE" CURVE AUTOMATICALLY CORRECTS HOOKS AND SLICES

"We made these clubs for golfers who are fed up spraying shots left and right with their driver and 3-wood. And millions do. If the best ten golfers in the business have trouble with woods, imagine how tough they are for the rest of us. So we designed the Controllers (the clubs' name).

"Our initial test with the Controllers showed that a mid-80's golfer could get 30 to 50 more yards off the grass with our 17° Fairway Controller, and match or beat his driver with our 12.5° Tee Shot Controller. Mike's World Record and comments from other pros, including a former Master's champ, confirm that these are the clubs of the future.

"But power without accuracy doesn't cut strokes, and that's where we have wood manufacturers by the throat. Our Controllers have *patented accuracy*."

The Controllers' patented accuracy comes from a scientific head design that reduces hooks and slices. No other iron has it. Indeed, *can* have it.

It works like this. If you hit a ball off the toe of an ordinary iron, it will start off to the right, as the impact "opens" the clubface. But then a stronger force, called the gear effect, takes over and spins the ball violently to the left. The reverse happens with a heel shot. It "closes" the club face and starts off to the *left*, then the gear effect slices it wildly to the right.

The Controller driving irons have a patented "invisible" curve (you can feel it, but barely see it) across their hitting surface that *tames* the stronger gear effect and draws off-center shots back to the middle of the fairway. It's a major golfing breakthrough and, along with their massive power, probably makes the Controllers the longest and straightest clubs in golf today.

One golfer told me, it was "...the first time I've played 18 holes and never left the fairway." Another said he cut six strokes, and vowed he would never play with his driver or 3-wood again.

Top Ten Money-Makers on the Tour Miss the Fairway with Their Driver 25% of the Time

So let me ask you. Do you have trouble with woods? If you do, there's no risk testing one or both of these new, super irons. The company will refund their price, if their unique combination of World Record power and patented accuracy doesn't cut 5 to 10 strokes off your score, and you return them undamaged within 30 days.

To try one or both Controllers, call the company direct at **1-800-285-3900** anytime or day, or send your name, address and check (or cc number and exp. date) to NGC Golf (Dept. DS-568), 60 Church St., Yalesville, CT 06492. The steel shaft Controller Tee Shot (12.5°) and Fairway Controller (17°) cost $69.00 each. Both cost $119.00. The graphite shaft models cost $89.00 each. Both are only $159.00. Add $10.00 s/h/ins. CT and NY add sales tax. No P.O. boxes. All shipments UPS. Specify right or left handed, regular or stiff flex, men's or ladies'.

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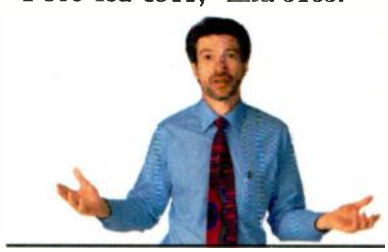

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Have you ever tried to debug a broken signal that only worked when your scope probe was touching it? Join the crowd. It's like a badge of honor. It means that you work on really fast systems. Then again, it may just mean you need a better probe. The one that you're using may not be up to par, or the way it is being used is inappropriate for the task at hand.

To help solve such problems, this article will explore how probes work, some ways to characterize their behavior, and the trade-offs inherent in various probe styles. It will even describe how to make a resistive-input probe that performs well into the gigahertz range.

Basically, all probes work the same way. When applied to a logic trace, a probe "siphons" off a portion of the signal energy and conveys it to the scope's vertical amplifier input. From there, the scope amplifies the signal and then displays it on the instrument's screen.

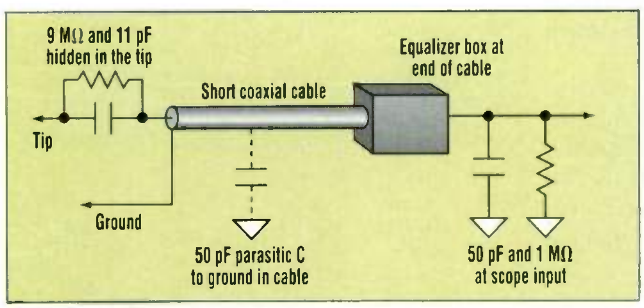
The siphoning process always distorts the signal being measured, because any probe loads down the circuit to which it is connected. Even with a 1-pF probe, the loading can be substantial. A 1-pF probe looks like a 160-Ω load at 1 GHz, which is the frequency associated with a 0.5-ns rise or fall time. (The effective upper band edge of a digital signal with a rise/fall time T is 0.5/T Hz. See *High-Speed Digital Design*, H. W. Johnson and M. Graham, Prentice-Hall, 1993.) Technically, the complex impedance is –j160 Ω, but that's splitting hairs because the phase doesn't matter as much as the fact that the 160-Ω magnitude is noticeable to a 50-Ω circuit.

Think about it. If you connect a 160-Ω load to your circuit, it would change the termination conditions. Wouldn't the levels shift? Wouldn't the signal's shape change slightly? Might it not ring, or overshoot differently, or cross the switching threshold at a different point in time? These same effects occur when probes are connected.

Room For Improvement

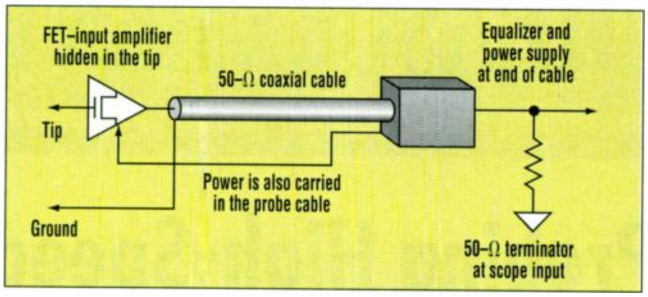
Some engineers assume that these effects are a manifestation of the Heisenberg Uncertainty Principle, but that is not the case. For ordinary digital problems, probe performance is nowhere near its fundamental physical limits. The problems are simply a manifestation of the rather crude state of the art of probe design. Better probes will do less damage to the signal under test. The industry can anticipate several more generations of improved probe designs before encountering limitations due to the immutable laws of physics.

You may be interested to know that electrical engineers in many other fields of



1. The capacitive-input probe, originally developed for use with vacuum-tube equipment, offers a high-input impedance at dc, but does not work well on very fast digital circuits.

study also are concerned with the general effect of probes on the device under measurement. (A good general reference on the subject is *Electrical Measurements* by Frank A. Laws, first published by McGraw-Hill in 1938.) We are not dealing here with any fundamentally new problems.



2. An FET-input probe employs an FET amplifier incorporated at the source end to improve performance, but this type of probe requires power, either from the scope or externally.

Besides the loading problem, a probe can introduce its own distortion, often in the form of additional ringing or overshoot. Even if it doesn't load down the circuit under test, a probe whose internal workings are ringy will fail to convey to the oscilloscope a faithful reproduction of the incoming signal. The actual waveforms in the circuit under test may be ideal, but what the scope sees may look completely different. I can't count the number of times I've seen engineers chase down presumed ringing problems in a circuit, trying every termination trick in the book, only to discover that the ringing was not present in the system, but was only a ghost image created by poor probing.

Three Basic Styles

There are three popular oscilloscope probe styles in use today:

- 10:1 capacitive-input probes,
- FET-input probes, and
- resistive-input probes (also called Z_0 probes).

The capacitive-input probe was originally developed for use on vacuum-tube equipment *(Fig. 1)*. This probe provides a very high input impedance (about 10 MΩ) at dc, which was a nice feature when engineers spent a lot of their time probing grid-bias circuits. Nowadays, digital applications don't require a 10-MΩ input impedance at dc. For digital applications, the probe's impedance at high frequencies is much more important.

Proper operation of the capacitive-input probe hinges on the assumption that the center conductor of the connecting cable has an aggregate capacitance to ground of 50 pF. At frequencies for which the cable begins to act like a transmission line (that is, frequencies in fast digital designs), the probe no longer performs correctly. A little box of compensating components at the end of the cable often includes a circuit to reduce this effect, but because of the fundamental limitations of the connecting cable few capacitive-input probes are rated for more than 500 MHz.

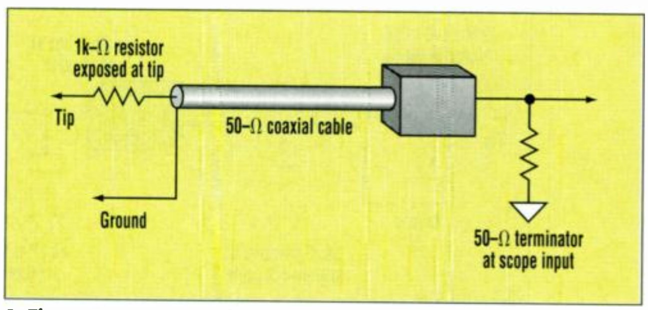
The FET-input probe has an active amplifier built into its tip *(Fig. 2)*. This circuit, which incorporates an FET-input buffer stage, amplifies the incoming signal and prepares it for its journey down the 50-Ω connecting cable to the scope. To use this probe, the scope must be equipped with a 50-Ω-terminated input circuit, and a power connection to feed bias power to the FET amplifier. The user must ensure that the power from the scope is compatible with the FET probe.

A probe can introduce its own distortion, often in the form of additional ringing or overshoot.

Some FET probes come with power adapters that permit their use on older scopes that have 50-Ω inputs but no power connections. But the engineer must make sure that the scope has a true internal 50-Ω input terminator. An external terminator connected with a "T" type BNC fitting substantially degrades signal quality in the 300-to-1000-MHz region.

The resistive-input, or Z_0, probe, combines characteristics of both of the other types *(Fig. 3)*. Like the 10:1 capacitive-input probe, the resistive-input probe is a passive device. That means that it will work with practically any scope. Like the FET-input probe, the resistive-input probe makes optimal use of its 50-Ω connecting cable. Once the input signal is coupled into the cable, it flows in a linear, time-invariant, almost lossless, and practically distortionless fashion all the way to the scope input termination, where reflections are damped. The scope must be set for a 50-Ω termination.

The resistive-input probe is inexpensive, has a terrific bandwidth, and is more tolerant of long ground wires than the other probes. These advantages come at the cost of a higher I_{OH} in the digital circuit in order to drive the 1-kΩ resistor. Fortunately, in modern high-speed systems, the extra drive current is almost always readily available.



3. The resistive-input probe provides excellent performance even at very high speeds. The trade-off is the need for a higher I_{OH}, but this is not normally a problem in high-speed digital systems.

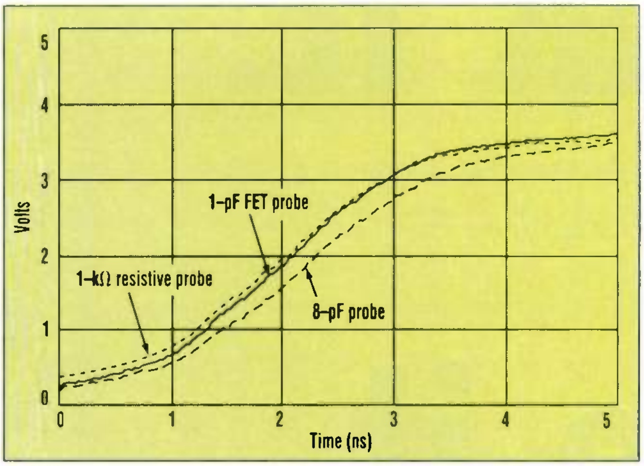
Characterizing Probes

Probes come in many different styles, shapes, and sizes to suit a wide variety of applications. Not all are appropriate for digital use. Engineers should consider several parameters when choosing probes for use on high-speed digital designs. The following is a discussion of those parameters.

Input loading—As noted, probes can load down a circuit, substantially distorting the signal under test. This happens when the probe's input impedance is comparable to (or less than) the driving impedance of the device under test.

To demonstrate the effects of probe loading, a high-qual-

ity reference probe was installed at the end of a long, source-terminated 50-Ω trace. The signal used in the demonstration had a rise time of about 2 ns. Three acquisitions were made, each with the addition of a scope probe: One acquisition with a 1-pF FET-input probe, another with an 8-pF capacitive-input style probe, and the third with a 1-kΩ resistive-input probe *(Fig. 4)*. A separate trigger circuit was used to maintain time-synchronism between the three measurements. These and all other measurements for this article were made on a Tektronix TDS 540B digital storage oscilloscope.



4. In measurements of a signal with a 2-ns rise time, an 8-pF probe caused a 200 ps delay. The 1-pF FET probe and 1-kΩ resistive probe did not significantly affect the transition time.

Even at the rather pedestrian rise time of 2 ns, the 8-pF probe clearly loaded down the circuit, delaying the rising edge by about 200 ps. In systems with little or no timing margin, this delay can easily be enough to cause a noticeable change in system behavior. At the frequency associated with this rising edge (250 MHz), the input impedance of the 8-pF probe is a mere 80 Ω, hardly good enough for working on fast digital circuits.

In contrast, the 1-pF FET probe and the 1-kΩ resistive-input probe did not materially affect the transition time, although the 1-kΩ probe did scale the signal amplitude to 95% of its nominal open-circuit value (1k/(1k+50) = 95%). The input impedance of both these probes at the frequency of interest (250 MHz) is much higher than 80 Ω.

At higher frequencies, eventually the 1-pF probe will run into difficulties. At signaling rates faster than about 300-ps rise-fall, only a resistive-input style probe can maintain a high enough input impedance to remain useful.

Bandwidth—Four classic criteria for evaluating an oscilloscope measuring system are sensitivity, linearity, gain flatness, and bandwidth. In modern high-performance oscilloscopes, problems with sensitivity, nonlinear distortion and ringing internal to the vertical amplifier and display circuits have largely been conquered. The primary limiting factor that remains, for digital applications, is bandwidth.

For very fast input signals, an inadequate bandwidth will, at the minimum, distort measured rise-fall times, skew timing measurements, and under-represent the extent of ringing problems. At worst, it may cause you to miss important features of the signals under test. Narrow pulses, glitches, and other effects can go unnoticed and untreated.

Given a scope's rated bandwidth, you can estimate its characteristic 10-90% rise-fall time *(see the table)*. If the scope's rise-fall time is at least three times faster than that of the logic being tested, you can expect to see little measurable distortion in any observed waveform. If the rise-fall times are comparable, expect to see a substantial deterioration of observed rise-fall times, but few other deleterious effects. Don't use a scope with a rise-fall time slower than that of the logic.

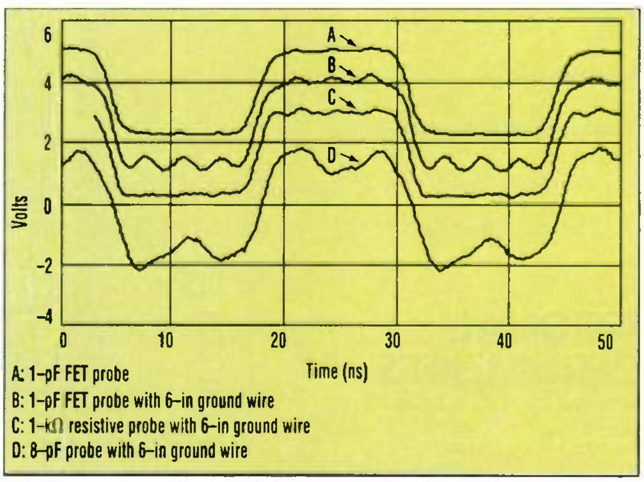
Most commercial probes also come with a bandwidth rating. The conversion from their bandwidth to 10-90% rise-fall time is, depending on the form of the bandwidth specification, the same as for an oscilloscope. For a high-end scope (one for which you purchase the scope and probes separately), you must then combine the scope rise-fall time and the probe rise-fall time to get an accurate picture of how the whole instrument will perform. The formula for this combination is:

$$t_{overall} = \sqrt{t^2_{scope} + t^2_{probe}}$$

Note that a 500-MHz scope and a 500-MHz probe does not a 500-MHz instrument make. When a 1-ns edge enters a 500-MHz probe, the edge speed is degraded to 1.208 ns, in accordance with

$$\sqrt{\left(\frac{0.339}{500\ \text{MHz}}\right)^2 + (1\ \text{ns})^2} = 1.208\ \text{ns}$$

Similarly, when the resulting 1.208-ns edge from the probe is processed by the scope, it deteriorates further to 1.38 ns. The net result is the same as if the signal had been processed by a circuit with an overall bandwidth of 353 MHz. For best results, plan for a combined overall rise-fall time that is three times faster than the signal to be measured.



5. Without a ground wire, all three types of probes performed similarly in measuring a 37-MHz clock. Trace A is representative. But with 6-in. ground wires attached, the resistive probe offered the least ripple.

Because of the transmission-line effects inherent in capacitive-input probes, they are generally not made with a bandwidth rating higher than about 500 MHz. The FET-input probes are limited today to around 1 GHz. Resisitve-input probes are available with bandwidths as high as 10 GHz.

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SANTA CLARA CONVENTION CENTER • SANTA CLARA, CA very low-level signals (fiber-optic receivers, for instance), the probe gain becomes important. All three probe styles introduce signal loss.

The capacitive-input probe, as depicted in Figure 1, has an attenuation ratio of 10:1 (–20 dB). If the scope has a minimum input sensitivity of 1 mV/div., then with this probe, the effective minimum input sensitivity will be 10 mV/div. Popular FET probes have an attenuation ratio of about 20:1 (–26 dB). Insisting on 1:1 performance at the probe level would require additional stages of amplification. Most manufacturers don't do this. They choose to build one tiny FET amplifier in the probe tip and then boost the signal back up to full strength at the scope. The 1-kΩ resistive-input probe also has an attenuation ratio of about 20:1 (depending on the exact resistor values used).

Ground wires—Capacitive-input probes, and to a lesser extent FET-input probes, sometimes perform poorly when connected to drivers with low source impedances. This effect is greatly exacerbated by the presence of any significant length of ground wire between the sensing end of the probe and the board under test. This effect can be analyzed by looking at the driver source impedance, the probe input capacitance, and the ground-wire inductance as an RCL series-resonant circuit. The following analysis of each probe type assumes a 6-in. ground wire (about 200 nH).

For a 10-pF capacitive-input probe, as the drive impedance drops below 100 Ω, the probe develops a nasty resonance at about 110 MHz. This resonance is right in the heart of digital territory, and is the primary reason why ground wires are not used with 10-pF probes when accurate measurements are needed.

The resonance in the 1-pF FET-input probe becomes evident at an even higher impedance level, 300 Ω, which is a worse problem for low-impedance digital circuits. Fortunately, the resonance is at a higher frequency, about 350 MHz, so you won't notice it unless your circuit rise-fall times are 3-ns or faster.

A resistive-input probe with a six-inch ground wire doesn't have a resonance. Its first-order circuit parameters form an RL network, which doesn't ring. To the first order, then, this circuit is always damped. That's one of the nice things about it: A resistive-input probe is less troubled by ground wire length than any other probe style.

An instructive demonstration of these effects in the time domain was made by measuring the same signal four different ways. The probes were applied one at a time, and the results stored, scaled, and time-shifted to fit the display. All four waveforms clearly show a 37-MHz clock *(Fig. 5)*. If that's all the detail you need, then the waveforms are essentially identical. If, on the other hand, you have been chasing glitchy bus ringing problems and need to quantify the undershoot, the differences are substantial.

In the absence of a ground wire (that is, with the shiny metal probe ground barrel directly connected to the PCB ground using a wire not longer than 0.100 in.), all three probes gave the same result. In that sense, they all performed reasonably well (except for the 200-ps timing shift noted above). Since all three results without ground wires were practically the same, only one, that using the FET probe, is shown (top trace).

The capacitive-input style probe, rated at 8 pF and 500 MHz and with a six-inch ground wire, had a resonance at 125 MHz, which showed up clearly as an 8-ns ripple (bottom trace). This configuration is not suitable for fast digital work. The FET probe with a 6-in. ground wire was better. The resonance was at about 350 MHz, which showed up as a noticeable, but smaller, 3-ns ripple (second trace from top). The best performer was the resistive-input probe with a 6-in. ground wire (third trace from top). This probe is clearly the least sensitive to ground wire distortion.

In summary, when probing low-impedance circuits, a capacitive-input probe is highly sensitive to ground-wire length, an FET probe less so, and a resistive-input probe performs best of all.

CALCULATING SCOPE RISE/FALL TIMES FROM BANDWIDTH

Type of bandwidth		
3-dB	6-dB	RMS
$\frac{0.339}{BW}$	$\frac{0.239}{BW}$	$\frac{0.361}{BW}$

A resistive-input probe is less troubled by ground wire length than any other probe style.

Making A 1-kΩ Probe

Fortunately, a 1-kΩ resistive-input probe is inexpensive and easily constructed. For reasonable performance up to 1 GHz, use a 1-m piece of RG-174 for the connecting cable. Terminate the scope end of the cable with a BNC connector, and solder a 1/8-W, 1-kΩ carbon-composition or carbon-film resistor to the center conductor of the sensing end. Dress the braid at the sensing end for soldering directly to the pc-board ground plane.

Some engineers like to solder a dozen or so resistive-input probes onto a board, and then connect them to the scope in various combinations as needed. They like this approach because the probes stay put and can be operated hands-free.

Alternatively, you can adapt this probe for free-roving operation by tacking a solid ground wire onto the end of the RG-174 ground braid. A number of ground-wire attachments made for other probes can be adapted for use with a resistive-input probe. On the end of the 1-kΩ resistor, try applying the crimp-on center-conductor contact from a male BNC connector. It makes an excellent permanent plated tip. In this form, the shop-built probe works well up to 1 GHz.

The resistive-input probe presents a flat 1-kΩ impedance all the way up to about 1 GHz. Above that, the input impedance begins to roll off, dominated by the unavoidable parasitic capacitance of about 0.17 pF that shunts end-to-end across the resistor. Using two 1/8-W, 470-Ω resistors in series instead of a single 1-kΩ component will reduce the parasitic capacitance, improving the roll-off characteristics by a factor of two.

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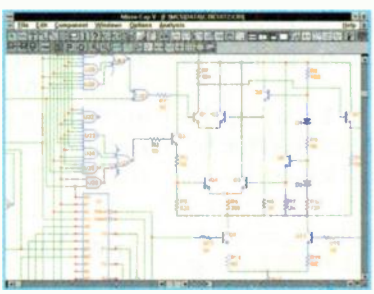

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the sense resistor. It should be kept up off the board under test, away from the ground plane. If it's pressed down near a solid ground plane, the resistor will pick up another 0.5 pF of parasitic capacitance to ground, substantially affecting the probe's performance. Kept at least 0.5 in. away from ground, this effect will be negligible.

As you move toward 10-GHz, the resistive-input probe is still an excellent choice, but it requires more care in its construction. For example, the 10-GHz probes offered by Tektronix use a well-crafted multibraided, low-loss coax; gold-plated SMA connectors; and very nice, long, skinny 950-Ω resistors, which have less end-to-end parasitic capacitance than short, squat resistors. These features extend the useful range of the probe easily into the 10-GHz region.

The resistive-input probe incorporates a fixed degree of signal attenuation. This is not usually a problem, assuming that the scope has adequate vertical sensitivity to make up the difference. The unit described above provides a 20:1 attenuation ratio.

If you need to make exact measurements, calibrate the resistive-input probes. Being made from carbon-composition or carbon-film resistors, they may not be too accurate. If you order up a batch of custom-select 950-Ω carbon-composition resistors, you can tune in a more precise 20:1 ratio. Beware of the temptation to use a 1% metal-film resistor at the tip unless you are certain of its construction. Many metal-film resistors incorporate an internal serpentine pattern in the metal film that will destroy the probe's high-frequency properties.

Practical Issues

Now we get down to some of the issues that can make or break your day. Things like flexibility of the connecting cable, size of the probe head, and cost. Here are some practical factors to think about:

- Will the probe fit between the cards in your chassis? It had better, because most truly fast bus systems won't function with extender cards, which add too much bus capacitance and screw up critical clock timing. Probes need to be squeezed between cards, with a right-angle bend at the tip. The shop-built resistive-input probe is a good candidate for this type of abuse.
- Will it stay on your bench, or get stolen? If you have invested in something nice, consider taking defensive actions to protect your property. I've seen more than one really good probe with a little tag on it saying: *Flaky connector—do not use.* In this respect, the shop-built 1-kΩ probe takes the cake; it's truly ugly.
- Will the probe help you meet higher-ups in the organization? Only the FET-input probe meets this requirement. Try ordering 50 of them, and you'll get to meet plenty of higher-level executives while they grill you about the cost.

For high-speed digital system designs, the ubiquitous 10-pF 10:1 capacitive-input probe is already inadequate. The two alternatives are the FET-input probe and the resistive-input probe. Of the two, the resistive-input probe is cheaper, has as good or better bandwidth, and is more tolerant of long ground wires. These advantages come at the cost of a higher I_{OH} required resistor. But in today's high-speed systems the extra drive current is almost always readily available, so the resistive-input probe makes a lot of sense.

As operating frequencies continue to rise, FET-input probes will run into increasing difficulties. For rise-fall times faster than about 300-ps, only a resistive-input probe can maintain a high enough input impedance to remain useful.

Howard Johnson is the president of Signal Consulting Inc., a high-technology consulting firm that specializes in solving high-speed digital design problems. He regularly presents technical workshops for digital engineers, including courses for Oxford University and the University of California at Berkeley. Johnson received his BSEE, MSEE, and PhD from Rice University, Houston, Texas. He is the author of "High-Speed Digital Design: A Handbook of Black Magic" (Prentice-Hall, 1993).

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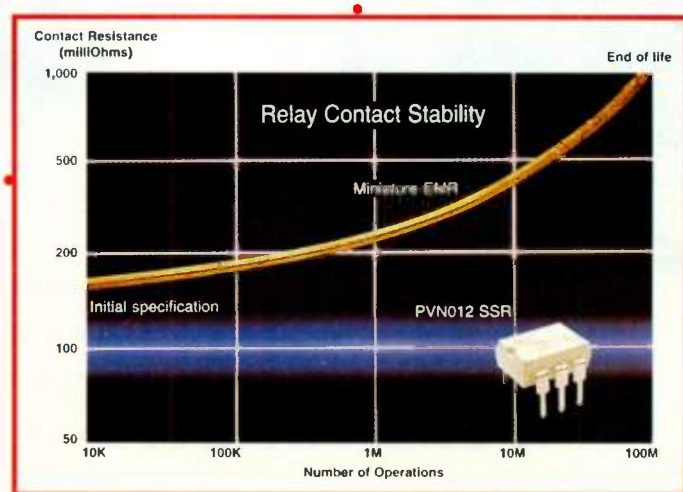

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European Design And Test Conference '97

Low-Overhead Design-For-Test Techniques, System-Level Design Issues, And Mixed-Signal Systems Take Center Stage At This Year's Conference.

John Novellino

Mixed analog-digital systems continue to hold the spotlight at the 1997 European Design and Test Conference (ED&TC). But new low-overhead design-for-test (DFT) techniques and innovative system-level design techniques also are areas of major interest. The number of papers on mixed analog-digital systems has again gone up, reflecting a particular strength of the European design community, according to conference organizers.

Those mixed-signal papers include new methods for on-chip testing of data converters. Other papers discuss synthesis techniques for delta-sigma converters and analog sensor interfaces, automated place and route for analog systems, and advances in symbolic analysis of large analog circuits.

Once again, the ED & TC will be held at the CNIT Conference and Exhibition Centre, Paris La Defense, France. The event will run from Mar. 17-20, starting with eight half-day tutorial sessions on Monday, Mar. 17 *(see the table)*. The accompanying exhibition will open with a preview session Monday evening (5:00 to 10:00 p.m.) and run Tuesday through Thursday. Besides the traditional scientific papers (93 this year) for oral presentation, the conference will include 23 poster presentations and 24 user forum papers, which will be published separately. The popular "Hot Topics" sessions, added last year, will continue.

Research into test technology will occupy 11 of the conference's technical sessions. Conference organizers note that the trend is to move testability concepts to the register-transfer and behavioral levels. Besides the low-overhead DFT techniques, papers will present new ways to estimate the testability of behavioral specifications. Several papers will discuss the design of self-checking data-path operators with less than 20% overhead. Other papers describe advances in built-in self-test that allow generation of tests for delay and CMOS stuck-open faults. Also covered is I_{DDQ} testing, including very sensitive on-chip current monitors and ways to use I_{DDQ} on deep submicron designs.

About a third of the conference's papers discuss system design techniques. Conference officials note that system-level CAD no longer focuses on simple applications, but rather now attacks state-of-the-art design problems. Authors use examples from video to multimedia and networking applications to show how executable specifications in C or C++ can be systematically refined into synthesizable VHDL modules. Academic research in this area is dominated by new techniques and computational models for software synthesis in embedded systems with real-time constraints, say organizers. Papers illustrate these methods using examples in MPEG, video, and digital communications. Also discussed are ways to synthesize and optimize memory architectures in data-intensive applications like video and multimedia.

The three Hot Topics sessions are designed to offer a combination of technical presentations and discussions on matters of current interest. They're more technical than panel sessions and offer more than just position statements. The discussions focus on the practical state of the art for each topic in an attempt to demystify it and present its practical implications, say conference organizers. Eric Van Utteren of Philips, Eindhoven, The Netherlands, coordinated the sessions.

One topic, "Networked CAD systems" (Session 5A), takes note of the increasing use of the Internet and of intranets to allow designers to work in geographically dispersed locations, without design tools and component libraries on site. The session, moderated by G. De Micheli of Stanford University, Stanford, Calif., looks at recent developments like simple and uniform protocols for design tasks, data visualization, and animation.

Another topic is "Deep submicron CAD" (Session 6A), moderated by Ralph Otten of the Delft University of Technology, Delft, The Netherlands. Speakers will discuss their first experiences with deep submicron design and their ideas on the new challenges for synthesis, simulation, and testing that this technology creates. Among the issues addressed are metrics, new paradigms, hueristics, and short cuts.

"Multichip packages for consumer applications" is the third Hot Topic (Session 7A). The session will center on consumer applications, in which multichip packages offer size, weight, and cost advantages. Subjects include known-good die issues, design, testing, substrates, ppm budgets, and marketing. Moderating the discussion will be M. Muris of Philips Research Labs, The Netherlands.

The Future Of Test

A panel session entitled "What will be the right test methodology for the year 2005?" (Session 4A) should be interesting. It's always difficult to make technology projections that far into the future, but work has to begin if test development isn't to consume the large majority of the design cycle as ICs get larger and larger. The panel, led by Keith Baker of Philips, will raise questions about the impact of high-level design and synthesis techniques and how the quality of the test process can be improved for devices of more than a hundred million transistors. The hope is to help academic and research institutions to identify future test needs.

A second panel is entitled, "How to introduce advanced design technology in qualified industrial design flows" (Session 2A). Its moderator, Patrick Dewilde of the Delft University of Technology, notes that a new methodology that lowers cost, leverages design flow, and uses leading edge technology would offer a competitive advantage. Such factors, however, are too hard to quantify, too vague to spend money on, and too simple to guide decisions, according to the session description. As a result, EDA users look more at whether a new product fits their current design approach rather than at the potential advantages of a new methodology.

The third panel, "Are there conflicts of interest in IP-based business?" (Session 9A) looks at the often incompatible goals of the participants in IP-based design. According to the session description, these groups include semiconductor houses that want to lock designers into proprietary processes, and fabless IP-vendors who prefer to license their technology to as many foundries as possible. System houses, on the other hand, want to be able to choose plug-and-play IP components from a variety of sources. Finally, EDA vendors try to make themselves attractive by offering access to as many IP components as possible. The panel will try to reconcile these conflicting points of view.

The user forum papers take a different tack than the scientific papers, offering descriptions of new CAD products and actual designs in a format that allows for intensive discussions with the authors. Among the topics covered are "FPGAs and dynamic reconfiguration" (Session 1D), "ASIC designs and design for testability" (Session 8D), and "CAD rules and

EUROPEAN DESIGN AND TEST CONFERENCE TECHNICAL PROGRAM

	Monday, March 17			
9:00 A.M. to 12:30 A.M.	Formal verification (Tutorial)	Systems-on-a-chip: From design validation to system test (Tutorial)	Rapid prototyping of digital signal processing systems (Tutorial)	Low-power circuit design for multimedia LSIs (Tutorial)
2:00 A.M. to 5:30 P.M.	Hardware/software codesign of embedded systems (Tutorial)	Built-in self-test for embedded cores (Tutorial)	Multimedia architectures (Tutorial)	CAD tools for analog and mixed-signal ASIC design (Tutorial)
	Tuesday, March 18			
8:45 A.M. to 10:30 A.M.	Opening and keynote addresses			
11:00 A.M. to 12:30 P.M.	**1A** System analysis techniques and applications	**1B** Sequential ATPG	**1C** Design and design methodology for analog circuits	**1D** FPGAs and dynamic reconfiguration (User Forum)
2:30 P.M. to 4:00 P.M.	**2A** How to introduce advanced design technology in qualified industrial design flows (Panel)	**2B** Advances in built-in self-test	**2C** Synthesis of controllers	**2D** Microsystems design I
4:30 P.M. to 6:00 P.M.	**3A** Software generation for embedded processors	**3B** Register and transfer-level test synthesis	**3C** BDDs and formal verification	**3D** Microsystems design II
	Wednesday, March 19			
9:00 A.M. to 10:30 A.M.	**4A** What will be the right test methodology for the year 2005?	**4B** High-performance architectures for multimedia & communication ASICs	**4C** Decision diagrams and diagnosis	**4D** Performance modeling
11:00 A.M. to 12:30 P.M.	**5A** Networked CAD systems (Hot Topic)	**5B** Progress in I_{DDQ} test technology	**5C** Architecture exploration	**5D** Layout design
2:30 P.M. to 4:00 P.M.	**6A** Deep submicron CAD (Hot Topic)	**6B** Testability solutions for regular structures	**6C** Data converter test issues	**6D** Test equipment and I_{DDQ} (User Forum)
4:30 P.M. to 6:00 P.M.	**7A** Multichip packages for consumer applications (Hot Topic)	**7B** Extensions and acceleration of discrete event simulation	**7C** Analog design and layout tools	**7D** Design flows and deep submicron circuits (User Forum)
	Thursday, March 20			
9:00 A.M. to 10:30 A.M.	**8A** Embedded tutorial: Hardware and software codesign in Europe and the U.S.A—A collaborative initiative	**8B** Power modeling and estimation	**8C** Formal methods in synthesis and verification	**8D** ASIC designs and design testability (User Forum)
11:00 A.M. to 12:30 P.M.	**9A** Are there conflicts of interest in IP-based business? (Panel)	**9B** Concurrent checking	**9C** New ideas in scheduling	**9D** CAD tools and design rules: From circuits to microsystems (User Forum)
2:30 P.M. to 4:00 P.M.	**10A** System-level design representation and transformation	**10B** Diagnosis and test generation	**10C** Logic synthesis for low power	**10D** Use of macroblocks in FPGA synthesis and design migration (User Forum)

design rules: From circuits to microsystems" (Session 9D).

A forum entitled "Test equipment and I_{DDQ}" (Session 6D) discusses new concepts in automated test equipment and off-chip and on-chip I_{DDQ} monitors. Session 7D, "Design flows and deep submicron circuits," presents design flows that focus on testability, mixed-signal applications, and deep submicron circuits. The final user forum, "Use of macroblocks in FPGA synthesis and design migration" (Session 10D), provides three examples of how to take advantage of existing macroblocks during circuit synthesis.

Once again, the conference's plenary opening session will feature three keynote addresses. According to Ludwig Eggermont, general chair, the speakers will build on last year's presentations, which discussed the consequences in design and test that could result from implementation of the National Roadmap for Semiconductor Technology from the U.S. Semiconductor Industry Association:

•Jim Meindel of the Georgia Institute of Technology takes a critical view of technology predictions and discusses system design issues from the point of view of physical limitations in semiconductor development. His talk is entitled, "Intrinsic (but not insurmountable) barriers to gigascale integration (GSI)."

•Aart DeGeus, president and CEO of Synopsys Inc., Mountain View, Calif., will present "System on a chip: The electronic industry at a crossroads." He will talk about the direction that the CAD industry must take, how the roadmap will affect it, what challenges it faces, and how these challenges might become affordable solutions for designers.

•Bjorn Pehrson of KTH, Stockholm, Sweden, will talk about the "Evolution of telecom and multimedia and their impact on system design requirements." He will show how these two major industries will profit from advances in process technology, how this will affect people's lives, and what design challenges the industries will face.

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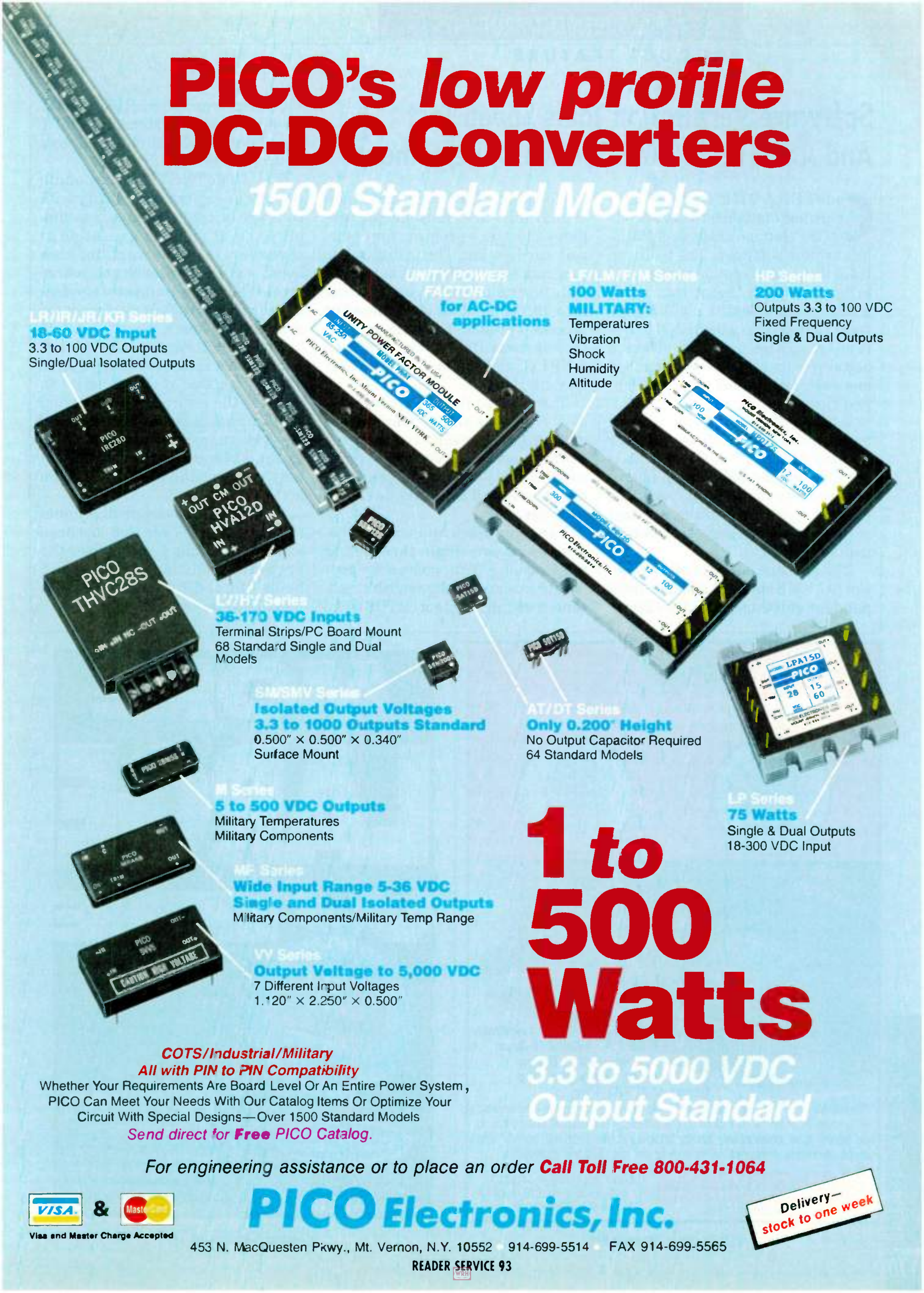

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READER SERVICE 93

PRODUCT FEATURE

Software Verification Tools Speed Test And Analysis In VME System Development

CodeTEST-VME is a software verification toolset that speeds up the test and analysis of VMEbus system software. The tools can trace the code execution of one CPU in detail or follow the intricate interactions of multiple CPUs with a high-level view of code using a VME system trace.The package offers a better picture of code execution than bus analyzers, which provide a limited view.

As an interactive, in-target set of tools, CodeTEST-VME can monitor as many as 32,000 C or C++ functions with the embedded-system microprocessors running at full speed. The package measures performance, test coverage, and memory allocation simultaneously.

The package consists of a single-slot 6U VMEbus card and four independent software modules (Trace, Performance, Coverage, and Memory). A software instrumenter prepares the user's program for in-circuit verification. The utility reads program source files and automatically inserts test point instructions into the code. The instrumenter processes programs written in C and C++ in compliance with K&R C, ANSI C, and the emerging ANSI C++ standards.

The card monitors the programs as it executes and communicates measurement results to the user's workstation or PC via an Ethernet connection. Run-time information may be viewed while the test is in progress.

The tools track application programs that are single-threaded or multitasking. The tools easily connect to a commercially available real-time operating system (RTOS), like VxWorks from Wind River, pSOS from Integrated Systems, or VRTX from Microtec Research Inc., or to a custom RTOS.

The CodeTEST Trace module combines deep trace capability with software-oriented features that simplify use. It displays execution at three levels of abstraction: high level, control-flow level, and source level. The trigger and storage features are specifically designed for software engineers.

CodeTEST Performance makes nonsampled measurements of up to 32,000 functions at a time, so it can monitor the entire application and pinpoint bottlenecks. The nonsampled measurements allow the module to display true worst-case and best-case times at the task or function level.

CodeTEST Coverage highlights the exact source code that has been executed, making it easy to see the program conditions that haven't been "forced" during the test *(continued on page 172)*

PENTON'S

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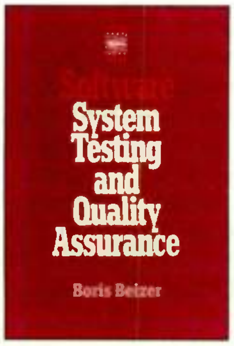
Books

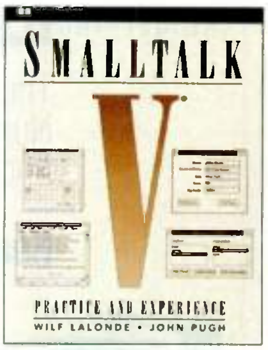
Software System Testing and Quality Assurance
Boris Beizer



This guide shows readers how to create and maintain reliable, robust, high-quality software. Using non-technical, easy-to-follow language, the author covers the gamut from unit testing to system testing and provides new and effective techniques for security testing, recovery testing, configuration testing, background testing, and performance testing. Integration testing strategies ensure that software components are compatible, while a wide range of techniques find and repair bugs at the unit and system levels.

358 pages, hardcover book, $55.95, Item B2454PM

Smalltalk/V: Practice and Experience
W. Lalonde & J. Pugh



Devoted to applications programming in Smalltalk. Each chapter is based on a column published in JOOP and Smalltalk topics are addressed within the context of practical and useful case studies, such as the design of classes with multiple representations, the importance of generalization, and the use of multi-level facilities and encapsulators. The accompanying disk provides full source code.

185 pages, softcover book, $39.00, Item DB2566PM

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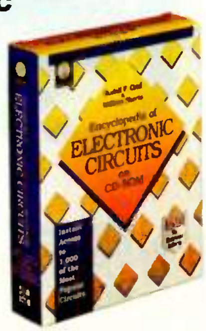

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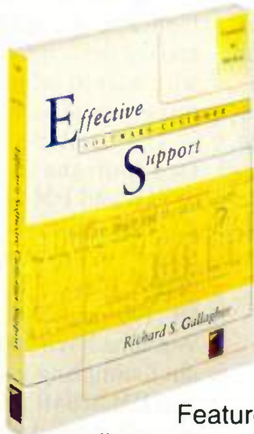

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PRODUCT FEATURE

(continued from page 170)
process. It uses interactive displays at the program summary, function, and source level while the program runs.

CodeTEST Memory tracks dynamic memory allocation in embedded programs so users can detect memory leaks in their code long before any symptoms appear in the system. It reports how many bytes have been allocated by each allocation statement and identifies more than 20 specific allocation errors.

The CodeTEST-VME measurement card costs $9800. Shareable, network floating software licenses are $5000 each for the Trace, Performance, Coverage, and Memory modules. Delivery is within two to four weeks.

Applied Microsystems Corp.
P.O. Box 97002
Redmond, WA 98073-9702
(206) 882-2000
e-mail: info@amc.com
Internet: http://www.amc.com
CIRCLE 496
JOHN NOVELLINO

Upgraded Analog-Digital Scopes Feature Increased Functionality, Performance

Five new CombiScope models feature increased functionality and performance. The instruments, which combine analog-oscilloscope and digital-storage-oscilloscope capabilities, have higher sampling rates on some models and deeper acquisition memories, along with built-in software for mathematical processing of waveforms.

The CombiScope B Series includes two four-channel models: the PM 3384B and PM 3394B; with 100- and 200-MHz bandwidths. It also contains three two-channel models: the PM 3370B, PM 3380B, and PM 3390B; with 60-, 100-, and 200-MHz bandwidths. All versions have 200-Msample/s single-shot sampling rates. The PM 3390B and PM 3394B also have a repetitive sampling modes. The four-channel models come with a 32K deep memory.

The scopes offer a multiple single-shot mode, which allows users to capture a series of single-shot waveforms and automatically store them for later analysis or comparison. This feature helps find all long-term malfunctions in a circuit under test without having to constantly watch the screen.

The scopes feature add, subtract, and multiply functions. The Math+ packages adds advanced functions, including FFTs, integration, differentiation, and histograms. Users can run two operations at a time on any waveform.

U.S. list prices for the CombiScope B Series are: PM 3370B, $2995; PM 3380B, $3575; PM 3384B, $5850; PM 3390B, $4790; and PM 3394B, $6925.

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P.O. Box 9090
Everett, WA 98206
(800) 443-5853
e-mail: fluke-info@tc.fluke.com
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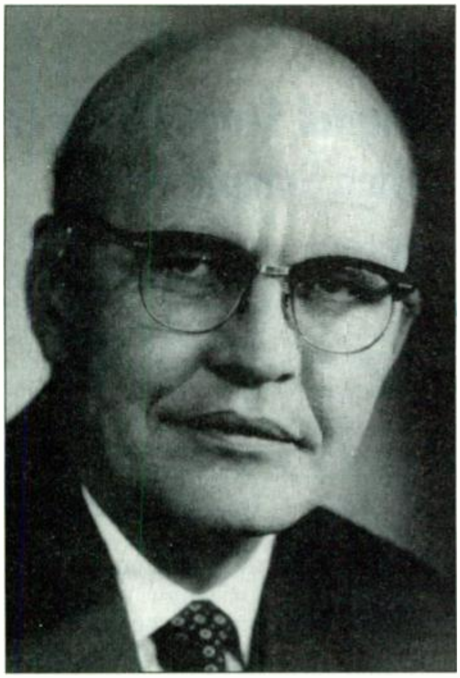
JOHN NOVELLINO



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Revered by engineers worldwide as the inventor of the IC and a pioneer of solid state technology, Jack Kilby will once again make an appearance at the Portable By Design Conference & Exhibition. Two years ago, Mr. Kilby was the keynote speaker—this year, he will present the first annual "Electronic Design Award For Technical Innovation." The award will be presented the author of 1997's most innovative conference technical paper. The award represents the first of its kind given annually. The ceremony will take place at the Industry Reception, held on the show floor at the Santa Clara Convention Center in Santa Clara, Calif., on Tuesday, March 25, 1997 at 5:00 p.m.

Also at this year's gathering...

KEYNOTE SPEAKERS:

TOM BEAVER
Vice President
Worldwide Marketing
Motorola, Inc.

PHILIP WENNBLOM
Director, Strategic Planning
Mobile and Handheld Products Group
Intel Corporation

ROBIN SAXBY
President & CEO
Advanced RISC Machines
(ARM)

VAUGHN WATTS
Director of
Mobile Computing Architecture
Texas Instruments

and a presentation from **BOB PEASE**, author of "PEASE PORRIDGE"

Exhibitor Information: Contact **Lisa Zurick**, Director of Show Sales, at 847/263-6837; fax 847/263-6854
Conference Information: Contact **Rich Nass**, Program Chairman, at 201/393-6090; fax 201/393-6073; or call **Betsy Tapp**, Exhibition Manager, at 201/393-6075; fax 201/393-6073

PRODUCT FEATURE

VLSI Testers Check Complex Chips At Up To 400 MHz On 1024 Pins

The J973 family of VLSI test systems uses a proprietary Pattern Integrator architecture. The result is fast, efficient testing of devices like microprocessors, audio and video controllers, and high-performance ASICs with complex, fast processor cores, embedded memory, specialty processes, and other megacells for custom functions.

The Pattern Integrator allows J973 systems to seamlessly interleave logic patterns with memory or scan patterns on any pin, at full speed. For devices with embedded analog macrocells, analog waveforms are synchronized with digital patterns. J973 systems are equipped with from 128 to 1024 pins, in 32-pin increments. Maximum data rate is 200 or 400 MHz. Minimum pulse width is 2.0 ns and edge placement accuracy is ±225 ps (1.0 ns and ±150 ps in Advanced Performance models). The testers have one timing generator per pin, with six edges pin to pin and 64 local edgesets.

A typical 200-MHz version with 384 pins costs $6000 per pin. Delivery is in 13 weeks.

Teradyne Inc.
VLSI Test Div
30801 Agoura Rd.
Agoura Hills, CA 91301
(818) 991-2900
CIRCLE 498
JOHN NOVELLINO

Upgraded Graphical Test Language Is Now Faster, Easier To Use

Version 4.0 of HP VEE, the graphical programming language for developing test and measurement applications, offers major enhancements over previous revisions. A new compiler executes typical computation-intensive routines 40 times faster than older versions and typical test applications between 150% and 400% faster than applications without a compiler.

A new professional development environment features a program explorer, a multiple document interface, and debugging tools. The graphical user interface offers navigation tools, including find, that facilitate the management of large programs.

VEE 4.0 also increases productivity by simplifying and automating routine tasks, such as instrument configuration and control, operator-interface development, test sequencing and debugging, and final test program distribution. The software's instrument manager searches for instruments connected to the computer and automatically handles addressing, whether the engineer is using drivers or controlling instruments directly. Furthermore, users now can employ HP VEE programs to create distributed applications without having to buy additional run-time versions of HP VEE.

Also new is the ability to integrate HP VEE objects into other commercial applications and proprietary systems written in standard text-based languages, like C. An ActiveX control encapsulates the HP VEE 4.0 user functions for integration into OLE-compliant applications like Excel and Visual Basic.

HP VEE 4.0 for Windows 95/NT (HP E2120E) costs $1295. The HP-UX version (HP 2111E) is $2495. A site license for 50 or more users costs $34,900. Evaluation copies, as well as application notes, user tips, and technical information, can be downloaded at http://www.hp.com/go/hpvee.com.

HP VEE 4.0 also is available from Computer Boards, CyberResearch, Data Translation, and Meilhaus as a companion product to those companies' plug-in boards.

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Test and Measurement Organization
P.O. Box 50637
Palo Alto, CA 94303-9512
(800) 452-4844 ext 5032
CIRCLE 499
JOHN NOVELLINO

Digital Scopes Deliver High Sample Rates

The three members of the LC574 family of digital oscilloscopes offer four channels with 1-GHz bandwidths, 1-Gsample/s digitizing rates, and acquisition memories ranging from 100 kbytes/channel to 2 Mbytes/channel. Resources can be combined to deliver up to 4-Gsample/s sampling and 8-Mbyte records on one channel.

To handle the long data arrays quickly and keep good front-panel responsiveness, the scopes employ a 96-MHz PowerPC microprocessor and up to 64 Mbytes of processing RAM. A memory-management system dynamically assigns maximum acquisition memory to each active trace to keep the sampling rate high. The system applies a patented min-max sorting algorithm to data records to quickly create a display that shows the signal's important features. It also assigns resources of computational or storage RAM to tasks requested by the user.

The scope's Analog Persistence mode allows users to display multiple signals with either opaque or transparent trace colors on the unit's 9-in. CRT display area. The full-screen mode displays a signal using the entire screen area.

Standard features include an advanced math package with integration, differentiation, square root, absolute value, exponential, and log functions, and six selectable digital filters. Multiple functions can be daisy-chained. Also standard is an FFT package that can resolve 4 million time-domain samples into the frequency domain, and histogramming capability. A floppy drive, IEEE-488 and RS-232 interfaces, and a high-speed graphics printer are all included.

The LC574A (400 kbytes total acquisition memory) costs $26,490; the LC574AM (2 Mbytes), $29,490; and the LC574AL (8 Mbytes), $37,490. The 64-Mbyte processing RAM costs $2000 on the LC574A and LC574AM. A 1-GHz active FET probe costs $990. Delivery is in four weeks.

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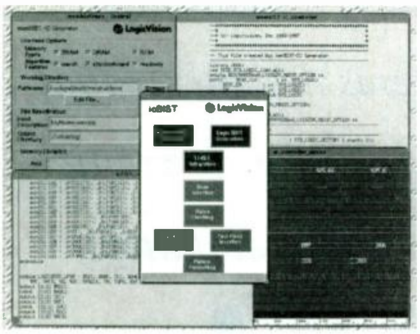
PRODUCT FEATURE

Automated BIST Solution Allows Testing Of IC Logic, Embedded Memories At-Speed

A comprehensive, automated BIST solution, icBIST, offers fault coverage up to 100% and true at-speed testing of IC designs, even at more than 100 MHz. As a next-generation product, icBIST features a new architecture to support high-speed designs, enhanced automation tools, and



a memory BIST technology for embedded DRAMs, SRAMs, and ROMs.

The package bundles proprietary BIST design objects (RTL hardware objects) for logic testing, memory testing, and IEEE-1149.1 boundary scan with automation software designed for use during the front-end of the IC design cycle. It automatically generates synthesizable RTL code for the BIST design objects and the IEEE-1149.1 boundary-scan chain and test- access port, making BIST insertion transparent to the user.

The logic-BIST controller employed has been designed to efficiently manage clock skew and multicycle paths, so that icBIST supports multifrequency, multipath designs. The controller architecture is scalable so that it can handle an unlimited number of scan chains for better control of test time, and it offers user-selectable pattern generation. Other features include back-end checking and analysis with streamlined, single-pass design rule checking, and fault simulation, signature generation, and BIST-control pattern sequencing and formatting.

New diagnostics include a standard pass/fail mode to determine whether a BIST test is successful. Also, a clock-freeze feature permits users to stop the clock during a BIST operation and determine the activity taking place in the internal scan chain for debugging purposes. Another feature allows scanning out of the system state during system mode operation for design debugging.

The new memory test technology, called memBIST-IC, replaces the company's ICRAMBIST product. A fully automated solution, memBIST-IC uses only one small (1000-gate) controller that can accommodate any type, configuration, mix, and number of embedded memories. Also included are significant enhancements to improve support and fault coverage for multiport memories.

The icBIST product is licensed on a per-design basis, starting at $46,500 per design for the first three designs. The memBIST software is available separately starting at $16,700 per design for the first three designs. Both products are available for Hewlett-Packard and Sun platforms.

LogicVision Inc.
101 Metro Dr.
Third Floor
San Jose, CA 95110
(408) 453-0146
e-mail: info@lvision.com
CIRCLE 501
JOHN NOVELLINO

Memory Test System Handles 64 Devices In Parallel At Speeds Up To 250 MHz

The J996 memory test system, the first model of the new Marlin platform testers, is a high-performance system for engineering characterization and volume test of packaged RAMs operating a up to 250 MHz, including standard or synchronous DRAMs and synchronous SRAMs. The system features overall timing accuracy of up to ±375 ps and edge placement accuracy of up to ±175 ps.

Using the company's System-per-Site architecture, the J996 offers a higher operating frequency and faster throughput than previous systems in a smaller footprint. For package test, the unit can handle up to 64 devices with 16 I/O pins each in parallel. The tester also provides high throughput for devices with wider I/O capability.

The J996 does this while using 20% less floor space than the previous-generation J994 system. The improvement is made possible by a new liquid cooling design that allows test systems to be placed closer together on the customer's test floor. The fully enclosed J996 does not interfere with the laminar flow in memory test facilities.

The Marlin systems use the IG900+ software system and are fully compatible with other J990 memory test systems. The IG900+ software offers a full suite of graphical engineering tools and templates optimized for production testing. Parallel testing is integrated in the IG900+ executive software, which allows rapid program development and efficient control of test flow and binning.

The system includes 512 I/O channels and 640 address/clock channels per test head. It features up to 32 independently programmable I/O functions and up to 40 independently programmable address/clock functions. It has one parametric unit per site. Two test heads can be employed with the system. Minimum pulse width is 2.0 ns at 2 V.

The J996 includes several features aimed at reducing the test cost per device. The high throughput reduces the number of systems needed, thus reducing capital costs. Also, the system can be purchased in several configurations and later upgraded as needed on the customer's test floor. Operating costs are reduced by the smaller footprint and by a new test head that does not have to be undocked from the handler when a circuit board is replaced. Finally, the system's overall accuracy and a high-fidelity handler interface increase the yield of tested devices.

Typical pricing for the J996 system is under $2 million for volume purchases.

Teradyne Inc.
30801 Agoura Rd.
Agoura Hills, CA 91301
(818) 991-2900
CIRCLE 502
JOHN NOVELLINO

Circle 520

Constant Power Load Needs Only A Few Parts

TIM R. BENGTSON
Rose Electronics, 1991 Concourse Dr.,
San Jose, CA 95131; (408) 943-0200; fax (408) 943-0360.

Switching dc-dc converters are often used in portable or battery-backed projects because of their broad input voltage range and high efficiency. These converters present a constant-power load to the battery—their input current increases as the battery voltage decreases.

By definition of current, charge is removed from the battery faster as the discharge progresses. Naturally, it's imperative to know how long the battery will keep the electronics alive, and the best way to find out is to test it on the actual product. If it's early in the product-development cycle, however, a prototype may not yet be available for testing, so a dummy load of some sort is required.

Using a constant-current or constant-resistance load risks overestimating the capacity of the battery, because the current never increases. The error can be significant, particularly when using batteries without a very flat discharge voltage profile, such as lead-acid or alkaline. This design uses only two inexpensive chips, a handful of passive components, and a power transistor to provide a true constant-power load *(see the figure)*. The key component is the LM3900 current-differencing (Norton) amplifier. It's similar to, but still distinctly different from, the familiar op amp.

An op amp connected in a negative feedback circuit follows the time-honored axiom that the amplifier's high open-loop gain causes the voltage difference between the inputs to be approximately zero. There's a similar rule with a Norton amp, except that it's the input *currents*, rather than the input voltages, that are made equal by the high gain of the amplifier. This mode of operation makes using the MC1494 analog multiplier easy, since the output is a current proportional to the product of its inputs.

The user applies an input current to the noninverting Norton amp input through R3. This causes the amplifier output to go high, which turns on Q1 and draws some current from the battery under test. By virtue of R7, the battery current causes a voltage to be seen at the multiplier V_X input; the V_Y input has been looking at the battery voltage all along. Consequently, the multiplier output current will increase until the Norton amp decides that the input current is equal to the multiplier output current, at which point the operation stabilizes.

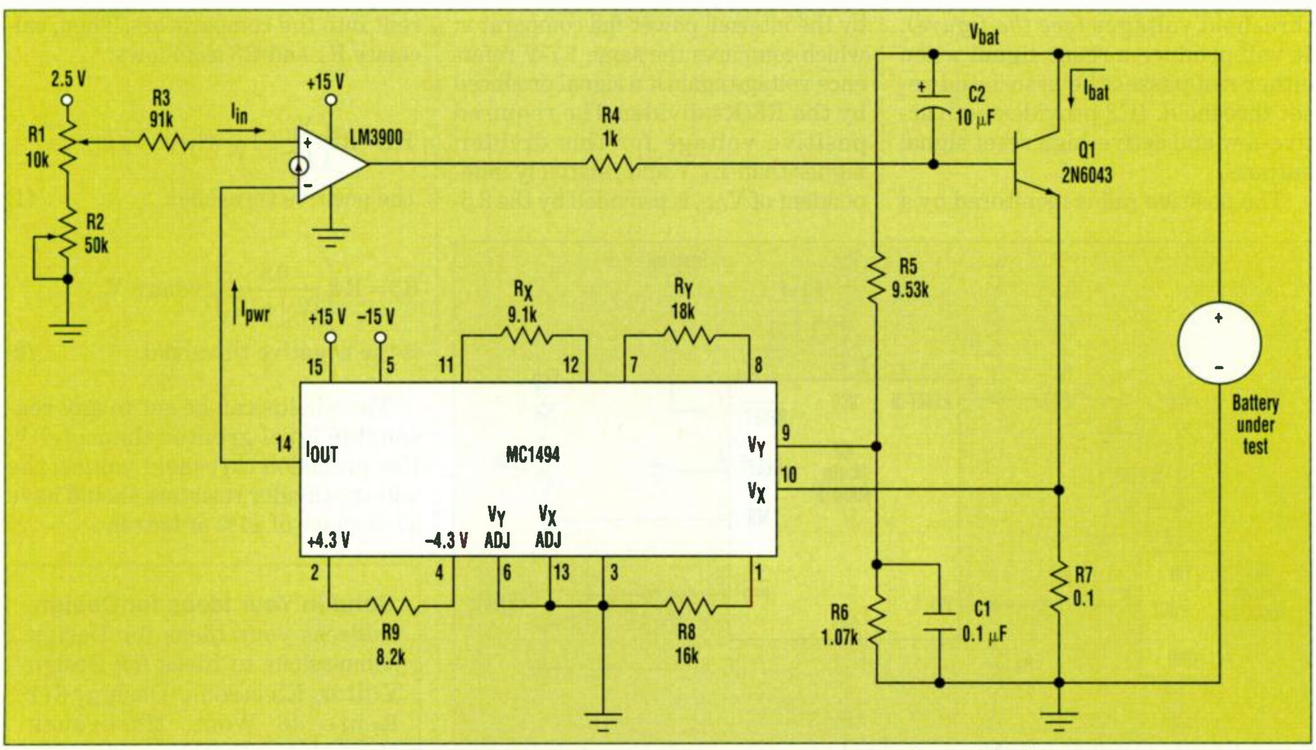
The MC1494 data sheet gives the multiplier output current as:

$$I_{pwr} = \frac{2}{R_X R_Y (500\ \mu A)}(V_X V_Y) = K1(V_X V_Y) \qquad (1)$$

$$V_X = R7(I_{bat}) \qquad (2)$$

and

$$V_Y = \frac{R6}{R5 + R6}(V_{bat}) = K2(V_{bat}) \qquad (3)$$



This low-cost design for a constant-power electronic load requires a minimal amount of parts, the most important being the LM3900 current-differencing Norton amplifier.

Due to the high Norton amp gain, $I_{pwr} = I_{in}$, which is constant. Substituting this and Equations 2 and 3 into Equation 1 gives:

$$I_{in} = (K1)(R7)(I_{bat})(K2)(V_{bat}) \quad (4)$$

The power delivered by the battery is $(I_{bat})(V_{bat})$:

$$(I_{bat})(V_{bat}) = \frac{I_{in}}{(K1)(R7)(K2)},$$

a constant. (5)

Capacitor C1 acts as a filter, and C2 kills the frequency response of Q1, assuring stable closed-loop operation. Note that while the noise in the voltage-sensing circuit can be filtered because it isn't under feedback control, attempting to filter the current-sensing circuit may slow down the feedback path enough to cause oscillation.

The component values shown give load maximums of about 30 Volts, 5 Amps, and 35 Watts. The scale factor of 1/10 for voltage and current sense is arbitrary, but modifying the scaling may require changes in R_X and R_Y (consult the MC1494 data sheet if modifications are necessary).

The MC1494 typically is used with potentiometers to zero out the input offsets, but as a practical matter, this circuit performs well without them. If extreme accuracy is required, and thus the potentiometers, then be aware that they must be temperature-stable. In fact, it's a good idea to ensure that all resistors associated with the multiplier have good temperature coefficients, particularly R_X, R_Y, and R8.

If R1 is a 10-turn potentiometer, then the load will be about 3.5 Watts/turn. A bias adjustment is necessary to account for a 10- to 15-µA output offset current from the multiplier. To adjust the bias, R1 should be set to the "zero input current" position, and R2 should be adjusted until current just starts to flow from the battery.

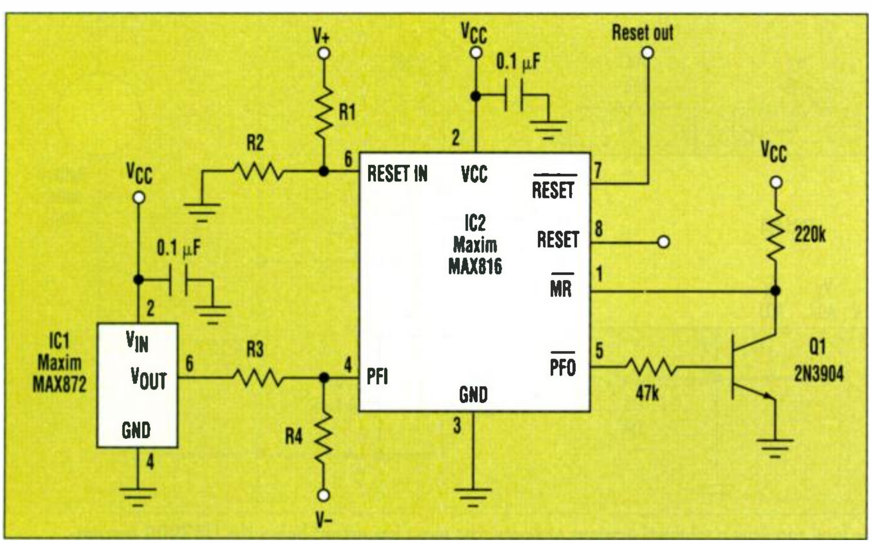
Circle 521

Single-Supply Microprocessor Supervisor Monitors Bipolar Rails

ROGER KENYON
Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086; (408) 737-7600.

The circuit shown monitors both rails of a bipolar power supply with respect to user-defined threshold voltages *(see the figure)*. It will produce a reset signal when either rail passes the associated reset threshold. IC2 provides both active-low and active-high reset signal outputs.

The positive rail is monitored by a comparator and 1.7-V reference voltage internal to IC2, plus the R1/R2 divider. The negative rail is monitored by the internal power-fail comparator, which compares the same 1.7-V reference voltage against a signal produced by the R3/R4 divider. The required positive voltage for this divider, higher than 1.7 V and relatively independent of V_{CC}, is provided by the 2.5-V reference IC1. V_{CC} can range between 3.0 V and 5.5 V.



This supply-voltage monitor asserts a reset in response to the loss of either rail.

These connections produce an action opposite to the usual one—PFO (pin 5) goes high instead of low when the negative rail fails. This transition is inverted by transistor Q1 to pull Manual Reset low, which in turn signals a power failure by triggering the reset outputs.

To set the threshold voltages, first select values for R2 and R4. Lower values waste power, and higher values produce error due to leakage current into the comparators. Then, calculate R1 and R3 as follows:

$$R1 = R2\left(\frac{V_P}{1.7} - 1\right), \text{ where } V_P \text{ is the positive threshold.} \quad (1)$$

$$R3 = R4\left(\frac{0.8}{|V_N| + 1.7}\right), \text{ where } V_N \text{ is the negative threshold.} \quad (2)$$

Thresholds can be set to any reasonable level greater than ±1.7 V. For precision threshold values, the voltage-divider resistors should have a tolerance of ±1% or better.

Send in Your Ideas for Design
Address your Ideas for Design submissions to Ideas for Design Editor, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604.

Circle 522

Precision DC Motor Speed Controller

W. STEPHEN WOODWARD
Venable Hall, CB3290, University of North Carolina,
Chapel Hill, NC 27599-3290; Internet: woodward@net.chem.unc.edu.

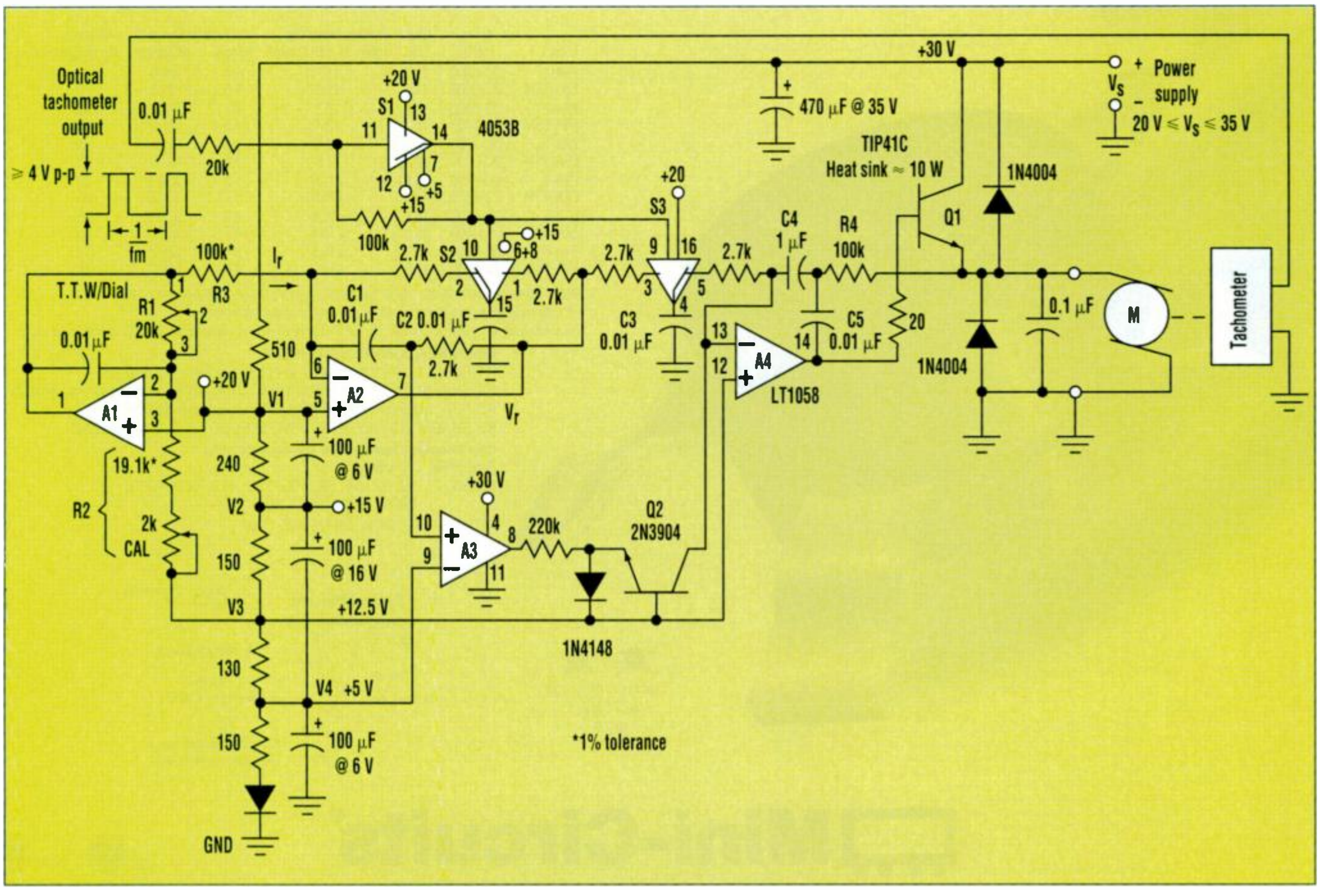
Optical tachometers that produce a frequency proportional to RPM are popular feedback sources for precision analog motor speed control. This usually involves a frequency-to-voltage converter (FVC) to convert the tachometer output to a voltage that's then input to a conventional servo. Though it typically works fine, it's unnecessarily complicated and requires a tachometer with a relatively high pulse/revolution characteristic to allow for both a reasonably fast loop response and adequate ripple filtering in the FVC.

The circuit shown circumvents those problems by replacing the usual FVC with period-to-voltage converter A2. The motor speed setpoint is adjusted with R1 as follows: The voltage on integrator A2 (V_r) is a negative-going sawtooth with slope given by $I_r/C1$. $I_r = (V3 - V1)R1/(R2R3)$, so if $1/F_m$ is the period of the tachometer pulses, the peak-to-peak swing of $V_r = (V3 - V1)R1/(F_mR2R3C1)$.

During the positive half-cycles of the tachometer square wave, S3 connects C3 to A2 so that the voltage on C3 tracks the sawtooth. On every negative square-wave transition, C3 is connected to the summing point of A4. This happens in such a way that if $V_r < (V3 - V1)$, then a positive increment of charge is deposited on the summing point. This tends to drive A4 negative and thus reduce the voltage applied to the motor, slowing it down.

By contrast, if $V_r > (V3 - V1)$, then a negative increment is dumped onto C4 and the motor voltage and speed are increased. The net result is for A4 to converge on the single motor voltage that makes $F_m = R1/(R2R3C1)$ because only then is $V_r = (V3 - V1)$. Consequently, the equilibrium tachometer frequency and therefore motor speed is directly proportional to R1 and independent of the absolute values of V1 and V3, removing any requirement for precision voltage references. Only the stability of the ratios of R1, R2, R3, and C1 contribute significantly to the error budget of the controller. Therefore, V_s supply voltages from 20 V to 35 V give the same accuracy.

Dc stability of the controller is assured by the relationships derived previously and by the error integration performed by A4. But, as in all servos, dynamic convergence is another matter. Damping of the system response and stable, over-shoot-free



A period-to-voltage converter is used in place of a frequency-to-voltage converter to reduce complexity in this optical tachometer.

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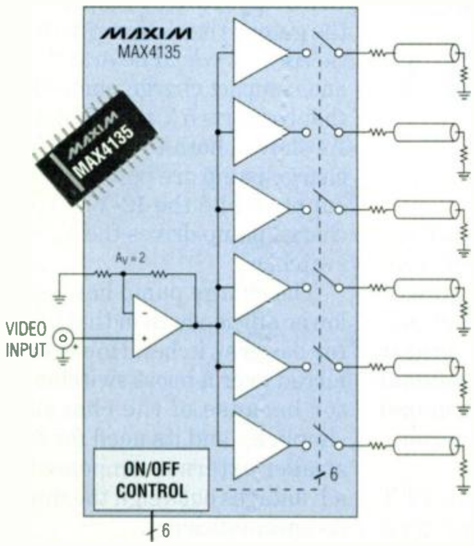

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response to perturbation are provided by the C4/C5 ratio and R4 x C5 time constant. The values for these parts, shown in the figure, worked well in the prototype. Different motors connected to different loads might require tweaking of these values. In general, the greater the C4/C5 ratio and R4 x C5 time constant, the greater net damping and tolerance of high load inertia.

One additional consideration is what happens if the motor stops and $F_m = 0$. Because the feedback path depends on charge transfers between C3 and C4, and since these transfers cease if $F_m = 0$, some means is needed to "jump-start" the servo. Comparator A3 does this by slewing A4 positive whenever V_r is allowed to ramp below V4. Accurate charge transfers in normal operation are promoted by the crisp square wave produced by Schmitt trigger S1.

Circle 523

Dual-Output Voltage Regulator Converts 5 V To 12 V And 3.3 V

PETER GUAN
Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95305-7487.

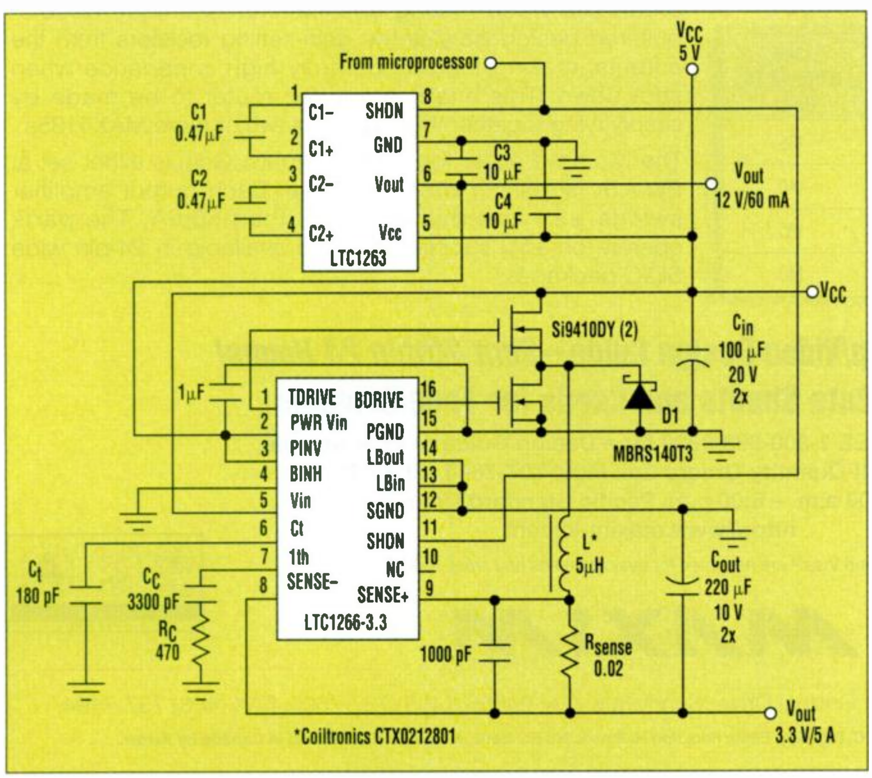
Today's microprocessors need a regulated 3.3-V supply that can provide several amperes of current. To obtain this, a synchronous switching regulator (LTC1266-3.3) using a 5-V supply is usually used with a p-channel top-side MOSFET and an n-channel bottom-side MOSFET. However, because a p-channel MOSFET has higher $R_{DS(on)}$ and higher gate capacitance than that of a comparable n-channel MOSFET, there would be a higher voltage drop across the MOSFET. This contributes to higher overall power loss. Such a drop in efficiency becomes even more obvious under high current situations. The ideal configuration would use n-channel MOSFETs for both top- and bottom-side switches.

To replace the p-channel MOSFET with an n-channel, a secondary input voltage capable of fully enhancing the n-channel MOSFET is needed. Because this secondary input only drives the gate of the charging MOSFET, little current would be drawn. A simple and compact charge pump (LTC1263) that converts 5 V to 12 V does the job. As shown, both the switcher and the charge pump are powered by the 5-V supply while the 12-V output of the charge pump drives the V_{in} pin of the switcher.

The charge pump has a somewhat lower efficiency than that of an inductor-based switcher. However, it's preferred over a boost switching regulator because of the charge pump's simplicity and its need for fewer and smaller external components. These advantages outweigh the drawback of its lower efficiency.

Since both the LTC1266-3.3 switcher and the LTC1263 charge pump have shutdown pins, both of them can be connected directly to an I/O line from a microprocessor. This way, the system can save much current and power during standby mode.

With these two new regulated supplies of 12 V/60 mA and 3.3 V/5 A generated from the original 5-V supply, many previously tough power-supply problems are eliminated.



A 5-V supply powers both the switcher and a compact charge pump. The charge pump's 12-V output drives the V_{in} pin of the switcher, allowing use of a dual n-channel MOSFET configuration.

IFD WINNERS

M. J. Salvati, Flushing Communications, 150-46 35th Ave., Flushing, NY 11354. The idea: *"High-Frequency Loop Antenna."* July 22,1996 Issue.

Jerry Steele, National Semiconductor Corp., Tucson Design Center, 940 Finance Center Dr., Suite 120, Tucson, AZ 85710, (602) 751-2380. The idea: *"Diff Amp Digitizes Small Signals"* Aug. 5,1996 Issue.

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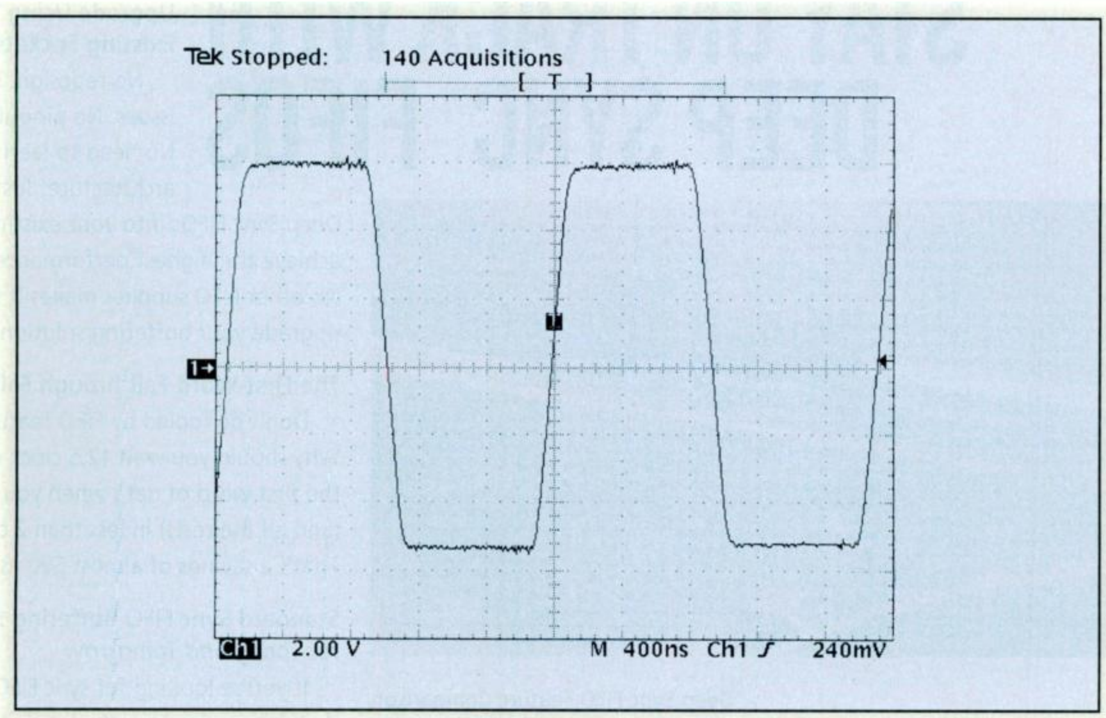

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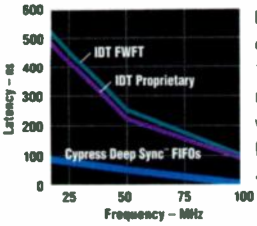

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	Proprietary FWFT	Industry Standard	All Cypress sync FIFOs are pin-compatible
Frequency Select Pin			
	FS Select pin	Clocks can be async	Does not limit range of operation
Depth Expansion			
	Serial cascade	Token passing	Low latency and low power
Power (f=20MHz)			
	×18: –180mA ×9: –150mA	–100mA –50mA	Lower power Lower power
×9 Package			
	10 × 10 TQFP	7 × 7 TQFP	Smallest ×9 packaging for all sync FIFOs

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BOB PEASE

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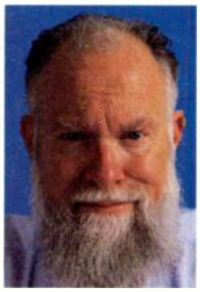

Hi, Bob:

So you don't like prepackaged team spirit. Your problem is, you prefer common sense to hard science. For example, the Fuller Brush Company has demonstrated over the last 55 years that every buck spent on team spirit has yielded $2.47 in additional profit, or an increase of 21.397%! How can you quibble with that?

Here's my own favorite teamwork tale from the waning years of the RCA Microwave group. I had been working on VERY advanced TWTs for many years, then shifted to GaAs amplifiers. One day, a former colleague who had switched to the greener pastures of management asked me whether I was participating in the "TWT Replacement" meeting. Nope. "But you're the only one in the building who has done BOTH," and Roy forced my presence down our Princeton team's gullet. (Boy, was he still green!)

With the assembled luminaries, I heard how our scientists were going to replace 8 to 18-GHz, 25-W tubes with solid-state amps. Then my turn came: I just drew power/gain/frequency curves on the whiteboard, first for my old tubes, and then for my new GaAs amp. (Singular—it was the only one EVER SOLD by the whole outfit.)

The sudden end of the "TWT Replacement Project" and its funding embarrassed even me. How can ONE real engineer defeat a whole gung-ho TEAM of EXPERTS in 5 min. flat! About a year later, RCA sold the TWT operation to Raytheon and closed up our shop.

Speaking of EXPERTS: I just came across a 1971 story in LIFE magazine about Tom McCuster's robot named Shakey. Seems its future had been questioned by Datamation, among others, but LIFE's Mate Scott was adamant about the "soundness" of the report. "Both Dr. Marvin Minsky and his colleague Dr. Seymour Papert estimated a 3- to 8-year timetable for the creation of a machine with the average intelligence of a human being." (Honestly! Copy enclosed!)

Here was the father of Artificial Intelligence himself, back in 1971, at MIT no less! Well, artificial intelligence simply never had a chance against natural stupidity. That goes for software as much as ANY kind of hardware. So don't you retire anytime soon!.

MAX J. SCHINDLER
Boonton Twp., N.J.

Yeah, one solid FACT is worth 10 buckets of wishful thinking. But are TWT's still any better than solid-state amplifiers, except for POWER output? As for Genuine Stupidity vs. Artificial Stupidity, that's a tough battle.—RAP

Hello, Bob:

I really enjoyed your Sept. 3, 1996 column. Measurements are my mania. Measurements are the essence of engineering and science; and I mean good, repeatable, precise, rational, and standards-traceable measurements. For the first two years of my engineering career, all I ever seemed to be assigned to do was repair equipment, track down ground loops, and measure, measure, measure.

Now, I'm very happy my mentors tormented me that way. I learned how to make measurements and operate test and measurement equipment. Often, I did not get to use the latest and fanciest gear, like the Fluke DVM. I had an old Simpson 303 VTVM and a 206 VOM, some old Tek 53X scopes, a GR R-L-C bridge, and some passive standards.

Even today, I still prefer the simplest approach when making measurements, like measuring cable phase delay with a vector voltmeter and sinewave RF generator, rather than a TDR. Moreover, I was taught to determine the overall accuracy of the measurements, and to compensate for the measurement system's accuracy. All measurements that went to customers or into my log were accompanied by a calculation for, and a statement of, the accuracy and traceability of the equipment. I never see that done today—by anybody.

I'm always suspicious of test equipment that purports to be self-compensating of its own measurement accuracy, as you so well pointed out. It's best to regard measurements with some skepticism and to validate against something of known value. It just might save you from disaster or disgrace!

via e-mail
JIM MEARS
Principal Engineer
Interface Products Group

Yes, there really is a difference between those who can measure, and the rest of the world.—RAP

Dear Bob:

Re: The letter from Herb Perten in the Nov. 18, 1996 *Bob's Mailbox*. Infinity Systems did have a speaker with a servo loop—their "Servo-Static 1," ca. 1972. The servo loop was on the combined channel subwoofer, which covered from 20 Hz to 110 Hz. The "Static" was in reference to the electrostatic panels for covering 110 Hz to 2 kHz, and 2 kHz to 20 kHz. I got a chance to hear one at the 1973 high-fidelity show in Burlingame.

The key parameter for the servo loop is the speaker cone *velocity*, not the position. The audio signal is proportional to sound pressure, and the pressure is generated when the cone moves. One exception would be in a small well-sealed car with large speaker cones, but I'm not really sure about subjecting my ears to that kind of abuse.

Even with a servo loop, there is another kind of distortion to look out for—Doppler shift from the moving cone. This is actually worse for the mid-range and above due to the smaller cones. This may account for my preference for electrostatic speakers. The velocity of the panels can be kept low due to their relatively-large area. I ended up buying a pair of Crown hybrids as a result of hearing them at the '73 show, and still have them.

ERIK MAGNUSON
Research Engineer
Quantum Magnetics
San Diego, Calif.

The theory on servo speakers leads you to expect some nice advantages.

BOB PEASE

Bob Carver just brought out a great new sub-woofer. Unfortunately, it requires 2700 watts for full output. But I'm told it sounds really nice. —RAP

Dear Bob:

Once again, you have hit the nail on the head with your column about smog check—"gross polluters." My wife's VW squareback, vintage 1971, did not quite pass the high-speed test (2500 RPM); it was way below the maxim allowable at idle. It was promptly dubbed a gross polluter requiring her to leave the car with an expert mechanic, who tried various rebuilt computers (new ones aren't available any longer), as well as new pressure sensors.

After screwing around with these devices for a whole week, he finally found a computer and pressure sensor combination that allowed the car to pass. However, we are now $850 out of pocket, and still have to take the car to a so-called "referee" station to have its good name cleared in Sacramento.

Why isn't similar criteria applied to trucks, busses (especially school busses), and motorcycles with and without mufflers? They stink up the environment at least as much as the cars. I believe that there is, indeed, a conspiracy to remove older cars from the road. Could it be so that the dealers can sell more new cars? Of course not, they would never pull such a dirty trick!

GERARD L. ZOMBER
Venice, Calif.

As I said, if it's really hard to get to your car to pass smog, then sell it out of state and buy something that's easy to keep tuned. Now, the Feds do want to crack down on particulates (diesel smoke, etc.). And a lot of people are bleating this will be very expensive, NOT cost-effective for improving health or air quality. Who's right? We shall see. —RAP

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

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READER SERVICE 161

HOWARD JOHNSON

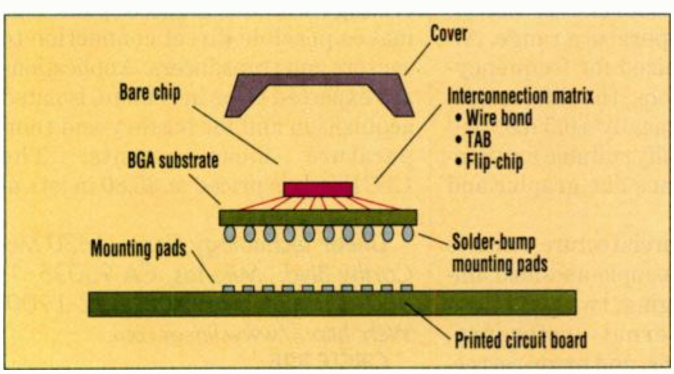
Ten Reasons Why I Love The BGA

Ball Grid Array (BGA) packages are taking the industry by storm, and I'm glad to see it. This new package style is suitable for any integrated circuit you might previously have put in a plastic QFP, PLCC, or SOIC type package (plus probably lots more stuff than that).

The BGA package is composed of three basic parts: The bare chip, a BGA substrate, and an interconnection matrix (*see the figure*). Depending on the package style, the bare chip may be affixed to the BGA substrate either face-up or face-down. The interconnection matrix then connects the bare chip to the BGA substrate using wire-bond, tape-automated-bonding (TAB), or direct attach flip-chip style connections. The BGA substrate, which is really a miniature multilayer PCB with teeny-weenie traces and microscopic through-hole vias, conveys the signals to the underlying printed circuit board through an array of solder-bump attachment pads on its bottom surface. A metal cover or plastic encapsulation is then used to seal the package.

Here are the 10 reasons why I love the BGA packaging concept:

1) BGA packages are inherently low-profile. There is nothing to it but the chip, some interconnections, a thin substrate, and a plastic encapsulant. There are no big pins, and no leadframe. The total installed height above your PCB can be as little as 1.2 mm (0.05 in.).



2) Their low profile and small size means that the total loop area, from a signal on the chip, through the interconnection matrix onto your PC, and back into the chip through the power/ground pins is very small, as little as one-half to one-third the size of the same loop on a QFP or SOIC package of equivalent pincount. This smaller loop area means less radiated noise, and less crosstalk between pins.


HOWARD JOHNSON

3) With all those bumps, you can devise very effective distributed arrays of power and ground bumps. Problems with ground bounce diminish in almost direct proportion to the number of power and ground bumps used.

4) Most BGA packages have big, fat, easy-to-work-with solder bumps, much bigger than the ones that are used for flip-chip connections. By way of contrast, flip chip techniques, which use solder-balls placed directly on the face of a silicon die, require solder bumps with much smaller dimensions, which can lead to troublesome and finicky manufacturing problems. Flip-chip has given the solder-ball technique a somewhat dark, mysterious, and wholly undeserved reputation—one which I hope will be redeemed by the rise in popularity of the BGA.

5) BGA packages are sturdy. Compare this with a 20-mil pitch QFP. On the BGA, there are no leads to bend or break. It's like a little brick.

6) With a BGA package, I can place a lot of the power and ground bumps in the interior bumps, leaving the I/O traces to the more routable positions around the edges. This is just one of the ways you can use the pre-routing inherent in the BGA substrate to straighten out an otherwise messy I/O routing situation.

7) Advanced BGA packages can cram all the solder-bumps right under the chip, with very little package overhang. That's as good as can possibly be done for miniaturization.

8) The bumps on the bottom look cool, and feel neat.

9) No fancy PCB technology is involved. It's not like C4 or direct attach flip-chip technology, where you have to carefully match the thermal coefficient of expansion between the PCB and the chip in order to prevent die cracking. With a BGA package, the interconnection matrix provides sufficient mechanical compliance to relieve thermal stress on the die. No expansion mismatches, and no hassles.

10) It is an inherently thin package, with reasonably good cooling properties. With the die mounted face-up, most of the heat flows down and out through the ball-grid array. In packages that mount the die face-down, the back side of the die is in intimate contact with the top of the package, making it an ideal arrangement for heat sinking.

I'm sure there are plenty of other really good reasons to love the BGA. I'd like to hear your reasons. In the meantime, if you want more information about BGA packaging, check out the book edited by John Lau entitled *Ball Grid Array Technology*, published by McGraw-Hill, 1995 (ISBN 0-07-036608-X). It's a keeper.

Dr. Howard Johnson is president of Signal Consulting Inc., a high-technology consulting firm specializing in solving high-speed digital design problem. He regularly presents technical workshops for digital engineers, including courses for Oxford University and UC-Berkeley. He is the author of "High-Speed Digital Design: A Handbook of Black Magic" (Prentice-Hall, 1993). He can be reached at (206) 556-0800; fax (206) 881-6149; e-mail: howiej@sigcon.com.

ADC Links Optically For Remote Tasks

A low-cost eight-channel ADC and controller, the Model RAD128 provides an optically isolated serial interface to any host computer with an RS-485 port. Typical applications include remote data acquisition, process monitoring and control, energy management, security systems, and other remote tasks. The unit, in a NEMA4 enclosure, may be used with up to eight of the company's 16-channel AIM-16P analog input multiplexer/conditioners, providing up to 128 single-ended or differential inputs. Each of the RAD128's eight digital I/O lines may be programmed as either an input or an output. All programming is accomplished in ASCII-based software, allowing the RAD128 to be used with virtually any host computer. On-board hardware support includes a crystal clock and three counter-timers for precision conversion, and a watchdog circuit for automatic reset on startup. ML

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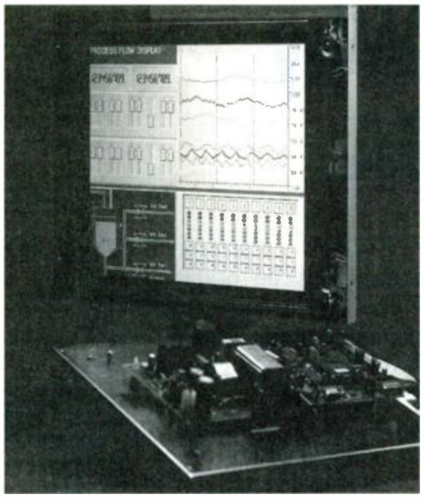
Open-Frame TFT Monitors Aim At Industrial Control

Four new open-frame TFT monitors are constructed in a flexible sandwich arrangement that provides enough space for an additional level of pc boards and fixed hard-disk drives. As a result, OEMs are able to construct integrated industrial computers or control systems for use in panels, production lines, and a number of other space critical areas.

The monitors are 10.4, 12.1, 13.3, and 13.8 in., and are compatible with VGA, SVGA and XGA (that is, 640 by 480 through 1024 by 768 pixels) and can be fitted with touch screens suitable for the final industrial environment. The manufacturer sees the OEM starting with the TFT monitor instead of just the panel as a way of demystifying the design and signal driving process, as well as saving on development time. The customer adds pc boards and a power supply into the OEM monitor kit. The product also can be supplied as a ready-monitor or a man-machine interface; the design



service can supply a finished, customized display with keypad or touch screen with 486 or Pentium processors inside. Even on small batch quantities the front panel color, finish, and legending can be customized. PMcG

***Kent Modular Electronics Ltd.**, 611 Maidstone Road, Rochester, Kent, ME1 3QL, United Kingdom; +44 (1634) 830123, fax +44 (1634) 830619.* **CIRCLE 826**

14-Bit, 3-MHz Sampling ADC Targets Digital Communications

The ADS-943 is a 14-bit, 3-MHz sampling ADC optimized to meet the dynamic-range and sampling-rate needs of digital-communications applications. Peak harmonic distortion reaches -83 dB and the signal-to-noise ratio is 79 dB. The device requires ±5-V supplies and dissipates 1.7 W in a 24-pin DDIP package. The power requirements and size, together with the ability to operate at the minimum 2.2 MHz sampling rate, suit the device particularly well to ATM, ADSL and HDSL applications.

The IC guarantees no missing codes to the 14-bit level over the entire military temperature range. Although it's optimized for frequency-domain applications, the differential nonlinearity (typically ±0.5 dB) and noise make it equally suitable for time-domain applications like graphic and medical imaging.

The ADS-943 architecture consists of a fast-settling sample-and-hold amplifier, a sub-ranging, two-pass flash ADC, an internal reference, timing/control logic, and error-correction circuits. Input and output levels are TTL while the circuit is edge-triggered, requiring a rising-edge of a start-convert pulse to initiate a conversion. The input range is ±2 V with versions in both the commercial and military temperature ranges using an autocalibrating, error-correcting circuit. The IC is pin-compatible with the 8-MHz ADS-946 and the 10-MHz ADS-947. Prices are $330 in 100-unit lots for the commercial ADS-943MC, and $412 for the military ADS-943MM. PMcG

***Datel Inc.**, 11 Cabot Blvd., Mansfield, MA 02048; (508) 339-3000; fax (508) 339-6356.* **CIRCLE 827**

Eight-Channel, 12-Bit ADC Has Max Diff Error Of ±0.75 LSB

The LTC1598L is a multiplexed 8-channel, 3-V micropower, 12-bit ADC. Supply current from the single 3-V rail is typically 160 µA while the part is converting and falls further to about 1 nA during conversions. The IC is a switched-capacitor, successive-approximation device that comes available in a 24-pin SSOP package. The maximum differential nonlinearity error of ±0.75 least significant bit (LSB) guarantees 12-bit resolution with no missing codes.

The 8-channel multiplexer output is brought to an outside pin on the IC so that a single processing circuit can be used externally. The input to the converter from such a circuit is located on the adjacent pin. The multiplexer and ADC can be controlled separately, allowing the continual conversion of a single channel. On-board serial I/O allows three- or four-wire transfers with the link compatible with Microwire and SPI. Maximum sampling frequency is at least 10.5 kHz, while the inputs can be in a range of 0 to 3 V operating with 1.5-V reduced spans. This makes possible direct connection to sensors and transducers. Applications are expected to be in remote, isolated acquisition and for battery and temperature measurements. The LTC1598L is priced at $5.80 in lots of 1000 pieces. PMcG

***Linear Technology Corp.**, 1630 McCarthy Blvd., Milpitas, CA 95035; 1-800-4-LINEAR, or (408) 432-1900; Web: http://www.linear.com.* **CIRCLE 828**

Speedy SRAMs Offer Shortest Access Times

Operating in systems with clock rates of up to 250 MHz and 225 MHz, respectively, a 1-Mbit and a 4-Mbit SRAM deliver the shortest access times for commercial CMOS memories. The 1-Mbit devices are available in either a 32-kword-by-36-bit or a 64-kword-by 18-bit configuration, while the 4-Mbit devices come in 128k-by-36 or 256k-by-18 organizations. Because they operate at a cycle time of 250 MHz, the 1-Mbit memories offer a pipelined access time of 2.25 ns. The 4-Mbit chips have a 225-MHz cycle time and a 2.5-ns pipeline access time.

All of the SRAMs can be had in processor-specific versions that incorporate register-to-register, register-to-latch, or flow-through modes, or offer a late-write cycle. The memories operate from 3.3-V supplies and can be had with either low-voltage TTL or HSTL interfaces. Active power for the 1-Mbit chip is 2.3 W at 250 MHz, while in the sleep mode the power drops to about 85 mW. The 4-Mbit chip has a slightly lower active power—2.25 W at 200 MHz, but a much higher sleep-mode power—520 mW.

Both SRAMs are housed in plastic ball-grid-array packages with a 7-row by 17-contact pad arrangement. The 1-Mbit SRAM (4-ns cycle time) sells for $95 each in lots of 1000 units, while the 4-Mbit device (4.5-ns cycle time) sells for $425 each in similar quantities. DB

***IBM Microelectronics Inc.,** 1000 River Street, Essex Junction, VT 05452-4299; Roger Verhelst, (802) 769-6780.*
CIRCLE 829

USB Core Family Eases Peripheral Design

A suite of synthesizable cores that implement various Universal Serial Bus (USB) interfaces provides designers with building blocks that can simplify the design of a custom interface circuit as well as speed time to market. Initially available will be the SL100, a USB core targeted at use in USB peripheral devices, and the SL75, a USB transceiver that can be targeted to a specific process technology. The SL100 core supports a wide variety of applications and handles all transfer types, including isochronous transfers. The interface to the peripheral is an 8-bit-wide bus that also supports data bursting. The licensing fee for the SL100 is $40,000. The SL75 transceiver has a license fee of $35,000, and that includes the targeting of the core to a specific process technology. In addition to the USB cores, the company is developing a family of products to support the IEEE-1394 (FireWire) standard. DB

***Innovative Semiconductors Inc.,** 444 Castro St., Ste. 405, Mountain View, CA 94041; Nabil Takla, (415) 968-3370.*
CIRCLE 830

Flat-Pack-Housed SRAM Quadruples Storage

With waning interest in the flat-pack option for high-density static memories, designers have lacked a 4-Mbit upgrade path to improve memory capacity. However, the WMS512K8-XFEX provides designers with a drop-in upgrade that fits the exact footprint of existing standard JEDEC 32-lead ceramic flat packs. The 4-Mbit monolithic SRAM (512 kwords by 8 bits) in the package offers access times as short as 17 ns, with other speed grades from 20 to 55 ns also available. The flat pack has corner power and ground leads and operates from a single 5-V supply. Inputs and outputs are TTL-compatible, and a low-power version with a low-voltage data-retention mode also is available. The SRAM comes screened for MIP-PRF-38534 and can be obtained in industrial- and commercial-grade versions. Moreover, the SRAM is available in 36-lead center power and ground flat packs (often referred to as the revolutionary pinout), both 32- and 36-lead ceramic SOJ packages, and a 32-lead DIP. In lots of 100 units the 4-Mbit SRAM sells for less than $200 apiece. DB

***White Microelectronics,** 4246 E. Wood St., Phoenix, AZ 85040; Philip Farahmand, (602) 437-1520.*
CIRCLE 831

Synchronous DRAM Modules Pack Up To 128 Mbytes

Available in either SIMM or DIMM configurations, a family of synchronous DRAM memory modules provides users with capacities of up to 128 Mbytes in a single module. The modules include 144-contact SO DIMM and 168-contact DIMMs, as well as 200-contact DIMMs for the high-end. Memory subsystem operating speeds range from 66 to 100 MHz.

The 144-contact, 64-bit-wide modules come in unbuffered, 3.3-V SO DIMM form with capacities of 6, 8, 32 and 64 Mbytes, and include serial presence detect. The 168- and 200-contact DIMMs also come in a 128-Mbyte capacity option and include either serial or parallel presence detect. Word widths are either 64, 72, or 80 bits, and the modules feature either registered or unbuffered I/O options. Prices for the modules start at $7.50/Mbyte in module quantities of 100 units. DB

***SMART Modular Technology Inc.,** 4305 Cushing Parkway, Fremont, CA 94538; Bill Johnston, (510) 623-1231.*
CIRCLE 832

Integrated 3D/2D Multimedia Accelerator Eases Design

The RealMagic3D multimedia accelerator, the SD6430, was designed from the ground up to meet the Microsoft Direct3D and DirectDraw application-program-interface specifications. The chip combines 2D and 3D 64-bit graphics acceleration and full-screen real-time video playback thanks to an on-chip, 200-MHz, true-color RAMDAC.

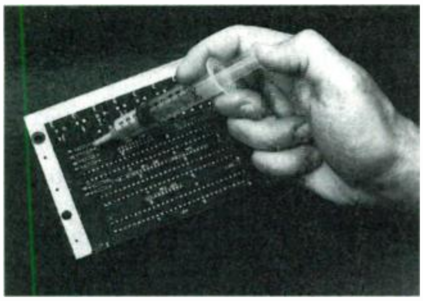
To minimize system redesign, the SD6430 was made pin-compatible with the popular Virge chip from S3. Consequently, the same board layout can be used; only new BIOS/driver software is needed. For 3D applications, there's support for Gouraud shading and flat shading, MIP-mapping and bilinear filtering, Z-buffering (16- or 24-bit), full perspective correction, Alpha blending and translucent effects, and Fog and Depth cueing.

An on-chip video processor supports multimedia video acceleration, which includes accelerated motion-video playback, horizontal and vertical scaling with linear X-Y interpolation, color-space conversion, and smooth scaling. These features all enable the playback of 3D interactive multimedia applications with MPEG video content on systems using a Pentium 120 or faster CPU. Housed in a 208-lead PQFP, the chip sells for $25 each in lots of 10,000 units. DB

***Sigma Designs Inc.,** 46501 Landing Parkway, Fremont, CA 94538; Prem Talreja, (50) 770-0100.* **CIRCLE 833**

Silver Adhesive Cures Rapidly At Room Temperature

The EP77M-F is a two-part, silver-filled, electrically conductive adhesive that will set up at room temperature within five to seven minutes, even when mixed in small amounts. The

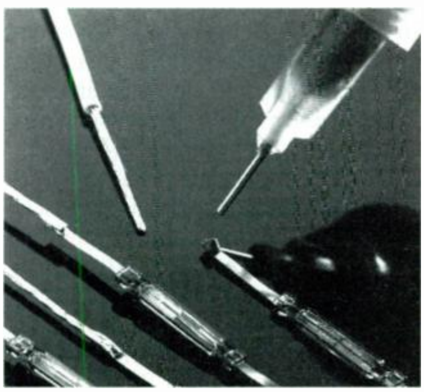


compound has a one-to-one mix ratio, by weight or volume, and develops a bond strength of 1500 psi tensile shear when fully cured. Electrical conductivity is noted within 30 to 40 minutes and volume resistivity is 0.010 Ω-cm. The epoxy adheres to metals, glass, ceramics, vulcanized rubbers, and many plastics, and is resistant to oil, water, and most organic solvents. PM

Master Bond Inc., *154 Hobart St., Hackensack, NJ 07601; (201) 343-8983; fax (201) 343-2132.*
CIRCLE 834

Paste-Like Solder Ensures Proper Fluxing

Packaged in a syringe-like container, SolderPlus paste solder can be applied either manually or with timed air pulse



dispensing to ensure proper amounts are deposited prior to heating. Solder melting can then be accomplished with one contact at a time; or batch melting using a hot air or furnace can be done. Because each metal particle of SolderPlus is coated with flux, instead of an internal core of flux, sticky adhesion holds the deposited solder in place and ensures proper fluxing to prevent cold solder joints. The packaging also prevents skin contact. PM

EFD Inc., *977 Waterman Ave., East Providence, RI 02914-1378; (800) 556-3484, or (401) 434-1680; fax (401) 431-0237.* **CIRCLE 835**

Water-Soluble Flux Is VOC-Free And Non-Corrosive

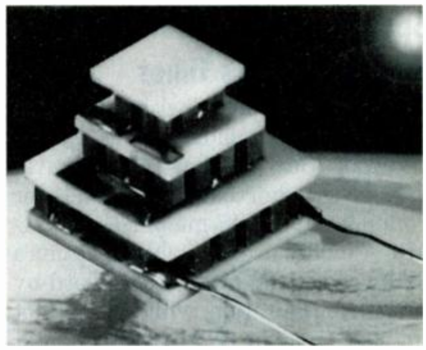
A water-soluble flux for electronics applications, no. 40MM4, is non-hazardous, VOC-free, and non-corrosive. The flux can be used for tinning pc boards and electronic-component

leads and for cleaning badly oxidized leads. Its moderately high chloride level doesn't attack ceramic packages or most sealing glasses. PM

Superior Flux, *95 Alpha Park, Cleveland, OH 44143; (216) 461-3315; fax (216) 461-6846.* **CIRCLE 836**

Coolers Are Targeted For Electro-optics

The OptoTEC series of thermoelectric products and services are designed specifically for electro-optic applications, such as laser diodes, IR detectors, or CCDs. The line comprises single-stage modules with a temperature difference of 60°C, or multistage modules with a temperature difference of up to 90°C. The devices are solid-state and use the Peltier effect to provide cooling. Features include precision temperature control, no acoustical or electric noise, and dc operation. PM



MELCOR, *1040 Spruce St., Trenton, NJ 08648; Kathy Salvatore, (609) 393-4178; fax (609) 393-9461.*
CIRCLE 837

Heat-Sink Family Cools Pentium Pro

The Allegro fan heat-sink family for the Pentium Pro comes with A-Pli thermal interface pads to deliver 0.9°C/W case-to-ambient heat dissipation. Combining a heat sink with a

ball-bearing fan rated at 50,000 hours at 25°C, the assembly is available with either dual internally captivated Pentium Pro clips or one of the company's EZ Sink-to-Socket clips. Pricing is $8.33 and delivery is four weeks or less, depending on stock. PM

Aavid Thermal Technologies Inc., *One Kool Path, P.O. Box 400, Laconia, NH 03247-0400; Patrick Riley (603) 528-3400; fax (603) 528-1478.*
e-mail: riley@aavid.com
Internet: http://www.aavid.com
CIRCLE 838

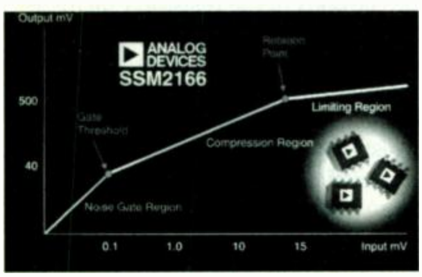
Voltage-Variable Attenuators Pad Mobile Wireless

Samsung's voltage variable attenuators (VVAs), the SM-515003 and SM-516003, are HF-VHF and UHF attenuator pads, respectively, for mobile wireless communications. They can be directly cascaded with additional 50-Ω VVAs. The SM-515003, which provides up to 70 dB of attenuation, is for use from 3 to 300 MHz. The SM-516003, for 300 MHz to 3 GHz, provides up to 40-dB attenuation. Both attenuators operate from 5 V dc and require two analog voltages per section with a range of -3 to +3 V at less than 15 µA. These devices maintain linearity and digital compression and act as an automatic gain control for typical radio signals. The SM-515003 is especially suited to communications and data-transfer applications in post down-converter IF processing. The SM-516003 is well suited to 0.9-, 1.8-, and 2.4-GHz ISM band applications. The SM-515003 is available for $2.10 each in quantities of 10,000; the SM-516003 is $2.40. Both come in a 16-pin SOIC, and are also available in tape and reel. LG

Samsung Microwave Semiconductor, 1530 McCarthy Blvd., Milpitas, CA 95035. (408) 433-2222; fax (408) 432-3268. **CIRCLE 839**

Preamp "System" Conditions Intelligent Speech

The new SSM2166 smart preamplifier system-on-a-chip, aimed at audio signals up to 20 kHz, features variable compression and automatic noise gat-



ing to yield microphone-level signals with a higher degree of intelligibility. With a single, user-selectable external resistor, users can set the SSM2166's compression ratio from 1:1 to 15:1 to produce an essentially undistorted audio output level, despite a varying signal input. In microphone applications, for example, the SSM2166 will attenuate very strong signals, and amplify weak ones. The SSM2166 also contains an automatic-noise-reduction circuit. It serves as an excellent input conditioner for the company's AD18xx series of codes. The SSM2166 costs $1.50 each, in 10,000-unit quantities. LG

Analog Devices, One Technology Way, P.O. Box 9106, Norwood, MA 02062; (617) 329-4700; fax (617) 329-1241. **CIRCLE 840**

LED Transceiver Drives ATM/FDDI Networks

The MDX-19 Series of optical LED transceivers for ATM (155 Mbits/s) and FDDI (125 Mbaud) data-communications networks is suitable for universal use with multimode fiber at 1300 nm.

Compatible with either 50 or 62.5-µm cable, these transceivers are utilized for most backbone applications. The MDX-19 uses a standard SC fiber connector and wave-solderable attaching post, and are pin-for-pin replacements for the standard 1-by-9 footprint. LG

Methode Electronics Inc., 7444 W. Wilson Ave., Chicago, IL 60656; (708) 867-9600; (708) 867-9130.
CIRCLE 841

IC Receiver Complies With Digital Video Broadcasting

The VES1520 is a single-chip receiver that's compliant with digital video broadcasting in cable systems. It combines continuous, variable-rate QAM demodulation (supporting symbol rates between 0.87 and 8.7 Mbaud), forward-error-correction functions, an adaptive equalizer for echo cancellation, digital antialiasing filters, and an on-chip digital clock. It's targeted for use in cable set-top receivers, digital cable modems, and terrestrial multipoint microwave distribution systems. The chip comes in a 100-pin MQFP. Sample quantities are available, with production quantities due in the second quarter. Cost is $20 each in quantities of 10,000. LG

VLSI Technology, 1109 McKay Dr., San Jose, CA 95131; (408) 434-3000; fax (408) 263-2511. **CIRCLE 842**

Voice Card Serves Computer Telephony

The Infostar/VXC Voice Exchange Card is a telephony-based communications server embedded in the company's Integrated Digital System (IDS) switch. It's designed to support computer-telephony applications in environments where a LAN may or may not be present. It brings the computer to the switch, reducing the need for a standalone PC to run standard voice mail/switch applications. The VXC Card plugs directly into one of the slots in the IDS cabinet to work as an applications server alongside the common control, station, and network cards. The first available application, voice mail, is currently shipping with the VXC card. VXC voice mail is available in 4-, 6-, and 8-port configurations with 45 hours of storage. Prices range from $4000 to $10,000, depending upon the application. LG

Executone Information Systems, Stamford, CT 06902; (800) 955-9866. Internet: http://www.executone.com
CIRCLE 843

Codec Targeted At Consumer-Telephony Applications

The KS8620 codec, a single-chip, PCM encoder/decoder and line filter, contains all of the functions required to interface a full-duplex voice telephone circuit to an analog phone line. The KS8620 uses µ-law coding with built-in bandpass antialiasing for 8-bit PCM processing, as well as provide signaling and supervisory information. Other features include an on-board precision reference. It consumes only 60 mW with dual 5-V supplies, and draws only 3 mW in the standby mode. Pricing is set at $1 in quantities of 100,000. It's supplied in either a 16-lead DIP or a 20-lead SOP. LG

Samsung Semiconductor Inc., 3655 North First St., San Jose, CA 95134; (408) 954-7000. **CIRCLE 844**

Fibre Channel Link Module Eliminates OFC

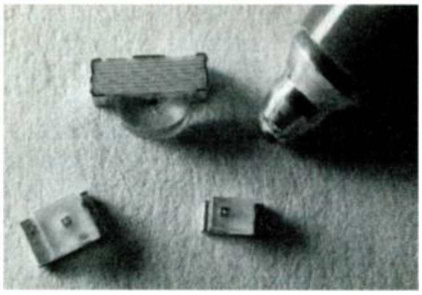
Methode's MGLM-1063 gigabit link module (GLM), designed for Fibre Channel arbitrated loop network applications, eliminates the need for an open-fiber-control (OFC) safety protocol. Utilizing the same footprint as standard

GLMs, the transmitter and receiver pair form a high-speed serial link with a date rate of 1.0625 GBaud. It provides a 20-bit-wide bus designed to transfer data encoded with the 8B/10B encoding scheme specified by the Fibre Channel ANTSI X3T11 standards. The parallel data bits to betransferred are serialized by the card and transmitted through fiber. At the receiver, a phase-locked loop recovers the data clock and processes the deserialized data. The output launch power is below the accessible emission limit as specified in the IEC-825-1 requirements. Typical transmission distance is up to 500 meters over 50/125-µm multimode fiber, and 10 km on singlemode fiber. The module operates from a single 5-V supply. PM

Methode Electronics Inc., *7444 W. Wilson Ave., Chicago, IL 60656; (708) 867-9600; fax (708) 867-9130.* **CIRCLE 845**

Three Different Lens Shapes For Three LEDs

Nova-Bright surface-mount LEDs, in orange, yellow, and red, come in three lens shapes: thin chip, ultra compact, and right angle. Using an advanced AlInGaP material, they achieve luminous intensities of 65 mcd (for 20-mA drive) for orange and yellow chips, and 50 mcd for reds. Applications include cellular cordless phones and pagers, handheld personal computers, and



portable industrial/medical testing and measuring equipment. In addition, they can replace incandescent lights in applications where compact design, longer life, and high reliability are important. PM

I.I. Stanley Co. Inc., *2660 Barranca Pkwy., Irvine, CA 92606; (800) LED-LCD1; fax (714) 222 0555.* **CIRCLE 846**

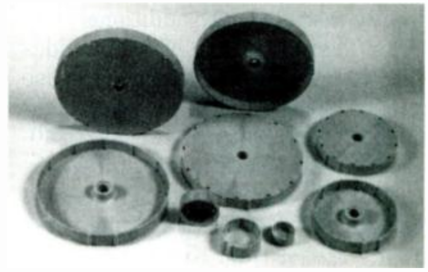
Surface-Mount EMI Suppressor Terminates in 600 W

The LCB-0603 suppressor, which comes in a 0603 surface-mount package, provides an impedance of 600 Ω for applications in ISDN modems, multimedia, and other high-noise environments. Maximum rated current for the device is 100 mA. The direct current resistance (DCR) is 0.90 Ω. Operating and storage temperature is -55°C to 125°C. The device may be either flow or reflow soldered. It's packaged in a standard 178-mm paper reel, with 8-mm tape width and 4-mm component pitch. There are 4000 devices on each reel. The LCB-0603 is priced at $0.11 each for orders of 100,000 pieces. Delivery is stock to six weeks. PM

Associated Components Technology, *11576 Trask Ave., Garden Grove, CA 92843; (800) 234-2645; (714) 636-8276; Internet: http://www.act1.com* **CIRCLE 847**

HTSM Line Enables Horizontal Mounting of Toroids

Mounting toroids to printed-circuit boards is easier with the HTSM line, which features two vertical locating ribs for ease of positioning either with manual or pick-and-place equipment. Cored slots permit standardization of pc-board surface-mount leads. Four standoff feet allow for solder fillet formation and flush cleaning of solder flux residues from underneath the assembly after installation to the pc board. The 16 largest sizes feature a recessed hex counterbored hole to accept a brass hex insert for securing the assembly from beneath by a screw. Four midrange sizes accommodate a brass knurled insert that will accept the screw from beneath the pc board



to secure the final assembly. Available in 28 incremental sizes to accommodate most common toroid sizes, the HTSM line is available from stock to four weeks following receipt of order. Prices for the mounts range from $0.13 to $0.70, each depending on size, in quantities of 1000. PM

Robison Electronics Inc., *P.O. Box 8121, San Luis Obispo, CA 93403. (805) 544-8000; fax (805) 544-80911.* **CIRCLE 848**

Wirewounds Eliminate EMF Problems

The RBR Series of wirewound resistors developed by Ultronix are constructed to eliminate EMF. This is achieved by forming the interface between wire and device termination so that there's a minimal difference in temperature between them. In addition, these junctions are buried deep inside the body of the resistor. Full materials compatibility is ensured by using bobbins fabricated in-house, and using the same material for the resistor body. Uniform resistance windings provide consistency between products. Electrical specifications include a resistance range from 0.1 Ω (±1%) and 10 Ω (±0.1%) to 1.37 MΩ; temperature coefficient range of ±10 to ±90 ppm/°C, power rating of 0.125 to 0.75 W, and a short time overload that's equal to twice the rated power. Price for a 5K to 10K resistor with a tolerance of 0.1% is $3.91 each in quantities of 1000. Availability is stock to 6 weeks. PM

Ultronix Inc., *461 North 22nd St., Grand Junction, CO 81502; (610) 644-1300.* **CIRCLE 849**

RF Power Modules Help Shrink Cellular-Phone Design Time

Designers of AMPS/ETACS cellular phones now can take advantage of silicon RF power that are basically ready-made power amplifiers. By using the BGY122A and BGY122B modules, which require no external components, time-to-market can be shortened because they significantly reduce the amount of design-in effort. Not only are they easy to design in, but the modules are currently the smallest 1.2-W modules on the market. Packaged in SOT388As, they have a pc-board footprint of 17 by 12 mm and a mounting height of 2mm.

The BGY122A covers the 824-to-849 MHz (AMPS) band, while the BGY122B covers the 872-to-905-MHz (E)TACS band. Both modules provide a minimum power gain of 27.8 dB, which means that only 2 mW of RF drive is required to deliver an output power of 1.2 W into a 50-Ω antenna load. This eliminates the need for a separate driver stage. In addition, both operate from a single 4.8-V supply and require no external bias circuitry or power-control switches.

Operating efficiency is typically 55%, minimizing power dissipation and improving device reliability. Standby current consumption is usually less than 1 µA. The modules are constructed with high-performance npn silicon planar transistor chips mounted on a metallized ceramic substrate, providing good thermal conductivity to the mounting base. *RE*

Philips Semiconductors, *P.O. Box 218, 5600 MD, Eindhoven, The Netherlands, phone: +31 40 272 20 91; fax: +31 40 272 48 25.* **CIRCLE 492**

Low-Cost Function Generator Has Arbitrary-Waveform Ability

By employing direct digital synthesis (DDS), the TG1010 10-MHz function generator can generate both standard and arbitrary waveforms. The arbitrary-waveform-generation function uses a 28-MHz clock, which allows harmonic information into the megahertz region to be generated. Waveforms of 1024 samples can be loaded via the digital interfaces and then replayed at any desired frequency and amplitude. Or, waveforms can be entered manually into the generator.

As a function generator, the TG1010 offers sine, triangle, square, pulse, multilevel, square-wave, and positive/negative ramp waveforms, as well as a set of quasi-arbitrary waveforms like sin x/x. Output level is settable between 6 mV and 20 V p-p, and output impedance is selectable between 50 and 600 Ω. Resolution is 0.0001 Hz, with an absolute accuracy of better than 10 parts in 10^6. Call the company for pricing and availability. *RE*

Thurlby Thandar Instruments Ltd., *Glebe Rd., Huntingdon, Cambs, PE18 7DX, England; phone: (01480) 412451; fax (01480) 450409.* **CIRCLE 493**

Photosensor Ignores Ambient-Light Background Disturbance

Targeted for safety- and performance-critical products (e.g., medical applications), the iC-WQ photosensor is designed specifically to ignore the background disturbance associated with ambient light. Its monolithic design and construction with an integrated photodiode ensures high noise immunity and technical reliability.

Sensitive signal photocurrent changes are amplified at the first stage, whereas dc photocurrents caused by background light are electronically suppressed. The integrated amplifier forms a bandpass characteristic without using any external components. A highpass filter suppresses constant light and low-frequency alternating light, while a lowpass filter reduces high-frequency noise.

The iC-WQ operates with visible or near infrared signals, with maximum sensitivity at approximately 100 kHz. The output signal coming from the iC-WQ is typically amplified in the current stage by 50 dB. Designed for low-power consumption, the photosensor will operate from a 5-to-12-V dc supply. The iC-WQ comes in a four-pole TO-18 metal package with a glass window, or in a surface-mountable SO-8 package. *RE*

LasIRvis Technology (Europe) Ltd., *26 Gosforth Close, Middlefield Industrial Estate, Sandy, Bedfordshire, SG19 1RB, England; phone: +44(0) 1767 692727; fax +44 (0) 1767 692626; e-mail: lasirvis@kbnet.co.uk.* **CIRCLE 494**

Display Case Has Easy-To-Remove Battery Compartment

A series of cases, dubbed "DATEC-CONTROL," offers lots of space for large, graphic displays and a battery compartment that can hold up to five round cell 1.5-V (AA) or rechargeable batteries. The part containing the batteries can be removed without needing any tools, allaying the typically annoying procedure of removing "battery packs."

For the first time, these cases can act as holders for PCMCIA cards without carrying out subsequent, elaborate milling work. The PCMCIA slot is soldered onto the circuit board; the card, which is removed below the battery compartment, is protected against dust, dirt, and water by an end cover with a snap-in mechanism. Unintentional release is impossible, therefore loss of data or failure of the program can be avoided.

With the PCMCIA capability, the case is suited for data transfer via modem, ISDN, or infrared; or for flash memory. Call for pricing information. *RE*

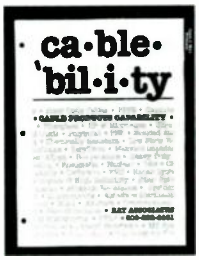
Odenwalder Kunststoffwerke GmbH & Co., *Gehausesysteme KG, Postfach 13 41, 74712 Buchen/Odw.; phone: (06821) 404-00; fax (06821) 404-123; e-mail: (06821) 4 04 00-00 01@t-online.de; Web: http://www.okw.com.* **CIRCLE 495**

Label Selector Guide Provides Extensive Materials Listings

The *Label Material Selection Guide* from Imtec Inc., Bellows Falls, Vt., is designed to aid in choosing appropriate labeling through a series of label-material listings. Nine labeling-application categories are represented, such as shipping, abrasion resistant, security laminations, and high-temperature resistance. Detailed specifications cover everything from thickness and adhesive type to color and compatible surfaces. To obtain the free guide, call (802) 463-9502; fax (802) 463-4334; e-mail: imtec@sover.net. RE

CIRCLE 670

Wire And Cable Guide Helps With App Designs



The *Cable Products Capability Guide* should help engineers in their cable, wire, assembly, and high-tech interconnect applications. Available from Bay Associates, Menlo Park, Calif., the guide details the variations of coaxial, multiconductor, flat ribbon, and high-voltage cables available. Options such as braids and tubing are identified to give designers somewhat of a "roadmap" when specifying cable constructions for specific applications. To get a free copy of the guide, call 1 (800) 552-0661. RE

CIRCLE 671

Two Epoxy Brochures Stick To The Basics

Epoxy Technology, Billerica, Mass., has issued two separate brochures detailing their epoxy products. The first brochure, "Epoxies for Semiconductor Applications," covers the complete capabilities for formulating and manufacturing sophisticated adhesives and coatings for semiconductor packaging. To help determine the optimal material for both manufacturing efficiency and product performance, technical expertise and details on the selection process are provided. The other brochure "Advanced Epoxies and Polymers for Demanding Applications," delves into how the company's materials are optimized for bonding, coating, encapsulating, and interconnecting in semiconductor packaging, hybrid microelectronics, fiber-optic cable assembly, and so on. To obtain either or both brochures, call (800) 227-2201 or (508) 667-3805; fax (508) 663-9782. When calling, specify the brochure. RE

CIRCLE 672

Electronic Catalog "Pumps" Out The Answers

Quick and easy identification of pumps most suitable for a designer's specific application is the goal of Haskel International Inc.'s (Burbank, Calif.) electronic catalog. Available on a computer disk formatted for MS-Windows, the catalog features interactive displays that graphically illustrate how the pumps operate. When a customer specifies performance parameters, such as flow rate, pressure, etc., the pump best meeting those specifications is indicated. Full technical details on dimensions, materials, and connections, as well as performance graphs, are displayed.The disk will be exhibited at the Offshore Technical Conference, Houston, Texas, in May. For more information, call (818) 843-4000; fax: (818) 841-4291. RE

CIRCLE 673

Company Claims Largest Surface-Mount LED Selection

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Catalog Focuses In On Magnifiers And Microscopes

Magnifiers, measuring magnifiers, microscopes, and other optical inspection devices get an up-close look in GEI International Inc.'s (Syracuse, N.Y.) new full-color catalog. The range of products include magnifiers and microscopes to measure dimensions of less than one-thousandth of an inch, zoom magnifiers, binocular and telescope magnifiers, three-dimensional sighters, and others. Six different reticle scales are available, all of which are illustrated. Call (315) 463-9261 for a free copy, or fax (315) 463-9034. RE

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Test And Measurement Guide Scopes Out Product Range

Covering 300 plus pages, Keithley Instrument's (Cleveland, Ohio) new 1997 edition of its Test & Measurement Catalog and Reference Guide highlights many new products and goes into depth on its mainstay items. Among those being profiled is the Model 2400 Digital SourceMeter, a high-speed test solution for large-volume component manufacturers. Another is the SmartLink family of miniaturized devices that make possible laboratory-grade measurements virtually anywhere.

The Guide is divided into nine sections: General measurements, Sensitive measurements, Sources, AC measurements, Scanners and switches, Semiconductor measurements, accessories, Keithley's Radiation Measurements Div., and Ordering information. Call (800) 552-1115 or (216) 248-0400; fax: (216) 248-6168; e-mail: product_info@keithley.com; Web: http://www.keithley.com. RE

CIRCLE 676

Fresh Opportunities Beckon At The Reinvented AT&T Labs

Gene Heftman

Even though it split itself into three parts a year and a half ago, The American Telephone and Telegraph Company, better known as AT&T, remains the world's largest and most formidable telecommunications organization. And even though it cast off a big chunk of its R&D unit in restructuring itself, AT&T still retains a distinguished laboratory that has laid the foundation of the world's communications systems and is home to a cadre of the leading experts in fields such as network design, digital signal processing, speech processing, software engineering, and computer security. The company may be "new" in terms of its business objectives but its appetite for fresh blood to keep the ideas and innovations flowing at AT&T Labs is as strong as ever.

As a company, AT&T is no longer the ubiquitous giant that once controlled every aspect of communications from basic telephone equipment to local telephone service to long-distance dialing. The new AT&T's focus is on communications and information systems services and is reflected in the structure of its R&D organization.

In the restructuring, the company spun off its systems and technology units into a new and independent entity called Lucent Technologies whose mission is to manufacture and sell network systems and telephone products—the hardware of communications. This meant giving up three-quarters of Bell Laboratories, its renowned scientific and technical research facility. Those that remained with the new AT&T Labs are concentrated largely in the field of information sciences. Among the key areas studied there are applications in network technologies, service platforms, interpersonal communications, electronic commerce, information for decision making, and on-line and transaction services.

AT&T Labs comprises three distinct units, each with its own role in the new corporate structure. AT&T Research, also known as "Core Research," takes the long view with some of its projects extending out years into the future. AT&T Applied Technologies works the other side of the research continuum, developing technologies and services for projects that are closer to realization. The third group, AT&T Internet Services, is concerned with developing new applications and services for the Internet.

Core Research consists of seven laboratories that investigate a wide range of communications areas to enhance the future performance of the network and seek out new technologies that can be applied to make it better, faster and less expensive for users.

The research effort covers fields such as the evolving wireless and lightwave technologies, speech synthesis and recognition, network architecture to handle current and future traffic on the AT&T Network, online interactive services and numerous others. Advanced mathematical techniques are used in statistical modeling, data analysis, probability and information theory to find new ways to improve communications.

Applied Technologies has four laboratories that study and support current communications operations through software development, performance analysis and operations research. It is also concerned with all kinds of communications services including cellular, private mobile radio, personal communications services and satellite systems

To staff these divisions, AT&T is on the lookout for individuals who possess certain so-called critical skills and talents. Among them are network management and infrastructure, Internet experience, digital signal processing, audio, video, and multimedia. Because of the swift pace of technology, the network will look very different than it is today and the company is counting on the Labs to design it.

Who Qualifies?

The work at AT&T Research requires a very high level of scientific, mathematical, and computing skills, so it's no surprise that most of the people recruited and hired for this group are PhDs. Not only that, but the demand for electrical engineers (EEs) is not as great as in the past because of the changed nature of the company's business which is now more software- and systems-oriented and less hardware.

As Joan Ardizzone, director of Human Resources at AT&T Labs, Murray Hill, N.J., puts it, "Since the spin-off of Lucent, EE demands are not as high as previously. It's now about a 60-40 split of computer scientists to EEs. And we look for highly academic types, especially mathematicians." Even when the Labs has a need for so-called critical market hires, individuals with special expertise and experience in a particular discipline like communications or mathematics, they usually come with a PhD according to Ardizzone, but not always.

While core research people almost always have a PhD, that requirement is not as critical in the other two divisions. Since the projects at AT&T Applied Technology and Internet Services are more business-oriented and directed at immediate customer solutions, masters- and bachelor-level engineers will find a less rigorous demand for higher educational attainment.

The centerpiece of recruitment efforts at AT&T Labs, and particularly at core research, is on college campuses. In this respect, it bears a striking resemblance to Bell Labs, its former sister group (ELECTRONIC DESIGN, *Jan.*

20, 1997, p. 169). The concentration on the top scientific and engineering college campuses is well developed and active, and because of the technical demands of interviewing prospective new hires, all recruiters are from research groups within the Labs and not from Human Resources. Ardizzone says, "HR people can't do this kind of recruitment; they don't speak the language and they don't know enough."

Up to 70 recruiters from the Labs, all PhDs who volunteer for recruiting assignments, and all with other jobs in various research departments, are the front-line warriors who fan out to various campuses to win newcomers to the Labs. Many of them are under the direction of Amy Muller, co-chair of the PhD Advisory Committee who describes it as, "A grass roots effort to organize PhD recruiting and to make sure that we're covering the right campuses." Although their primary mission is to recruit at the doctoral level, they also have an eye out for promising undergraduates who are in their graduating class. And while computer scientists and EEs comprise the bulk of the recruits, Muller says they also are looking for psychologists and behavioral scientists and people who understand human-computer interactions.

The role of the PhD Advisory Committee is to seek out candidates for all of AT&T Labs, not just core research. Over 50% of the openings are there, but recruiters also try to fill spots in Applied Research and also are trying to get people in the business unit of AT&T interested in some of the candidates.

Recruiting at the Labs is not simply a one-way street where PhDs go to the universities to seek out the best candidates. A significant dialog and partnership has developed between the Labs and its top universities by which faculty members come to work at the Labs for parts of the year and then go back to teaching. Some of these professors act as talent scouts, identifying promising students to the recruiting staff for consideration as employees. In many respects, it works like a farm system in professional sports. Joan Ardizzone says that "Some kids are followed by the Labs from their freshman year in college and when they complete their PhDs, the lab tries to recruit them."

To allow budding researchers to get their feet wet, AT&T runs a big summer intern program for students. Over 100 young people spend the summer working on different projects at laboratories in either Murray Hill, N.J., or Holmdel, N.J. They are provided with housing, are paid for their work, and then return to school in the fall. To get acquainted with the research environment, the summer interns are assigned a mentor, usually a senior scientist or engineer whose role is to show the young student the ropes and teach him or her what goes on at the Labs.

> **"Today's languages and applications aren't going to be the same five years from now."**

Who Gets In?

To get a job with AT&T Labs, a person not only needs an outstanding academic record along with faculty recommendations and a flair for independent research; he or she also needs a set of core skills applicable to the requirements of the type of research being conducted and to the areas of work they are interested in. Some candidates have already demonstrated research capabilities by publishing papers for technical journals and conferences.

Computer science and mathematics applicants should have a good general background in their fields in addition to training in some of the more specific fields of programming languages, distributed computing, optimization techniques, and just about any type of system integration and networking skills. According to Amy Muller, "We don't expect people to come in and redo their thesis. They must be able to move on and learn new stuff since today's languages and applications aren't going to be the same five years from now."

The mentoring approach used with summer interns also is the method for bringing new hires on board when they arrive at the Labs. A mentor takes the new person under his wing, serving as an advisor in all aspects of adjusting to the world of research. And the Labs are replete with numerous experts in every field of communications and computers who can serve as mentors. For example, the Labs are home to 26 AT&T Fellows, senior researchers who have performed outstanding work in their fields. One of them, Lawrence Rabiner, present director of the Labs, is one of the leading experts on the applications of digital signal processing to speech communications and speech recognition. Other AT&T Fellows have made significant contributions in fields such as computer and communications security, ISDN communications, lightwave technology and systems, network architecture, computer languages, and database management systems.

In addition to the mentoring program, the Labs provide incoming employees with an orientation program that includes formal session and meetings to get acquainted with how things are done and to understand the overall mission of the organization. Increasingly, there is a move to put much of the pertinent information on the World Wide Web. For those interested in learning more about AT&T and the work at the Labs, their Internet address is *http://www. att.com*. The company also uses magazines, newspapers, and agencies in its recruitment program.

Because the competition is steep for the caliber of people the Labs seek, compensation packages are generous and the work atmosphere is not highly regimented. As befits a university-oriented institution with an open campus, people are not forced into rigid work rules. Flex time is the norm and staffers are generally free to come and leave any time they want. The buildings are open 24 hours a day, seven days a week, and all services are available.

The company offers a tuition-assistance program and some individuals are allowed to attend universities to obtain an advanced degree while remaining on the payroll.

Gene Heftman is a free-lance technical writer specializing in advanced electronic technology including ICs, computer systems and software.

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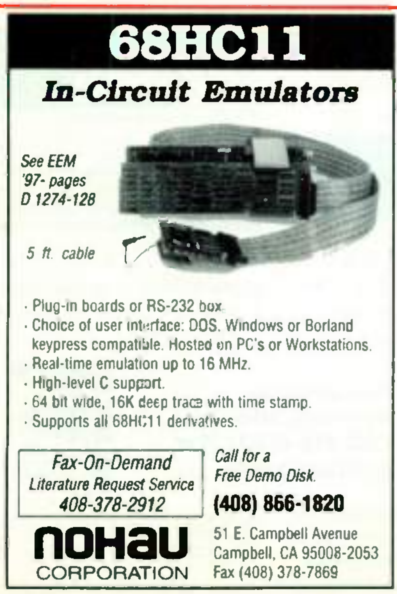

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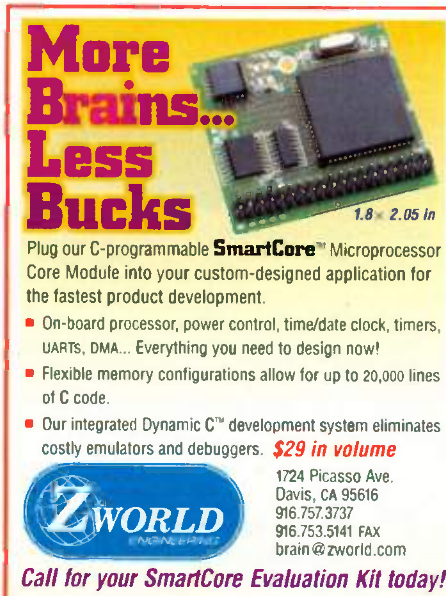

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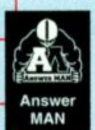

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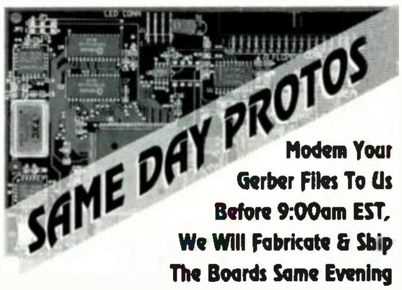

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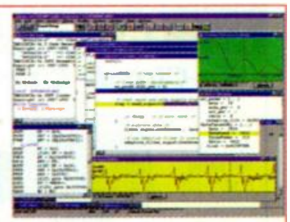

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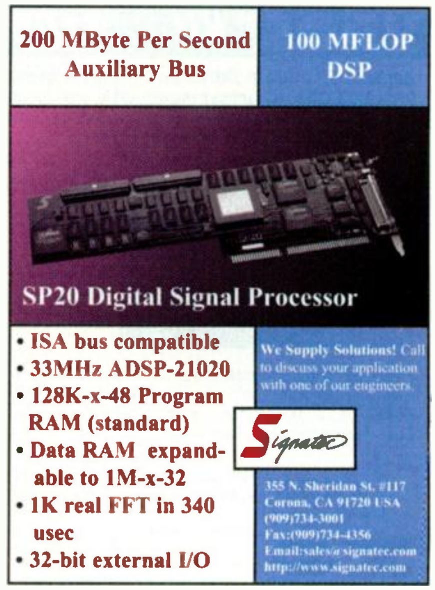

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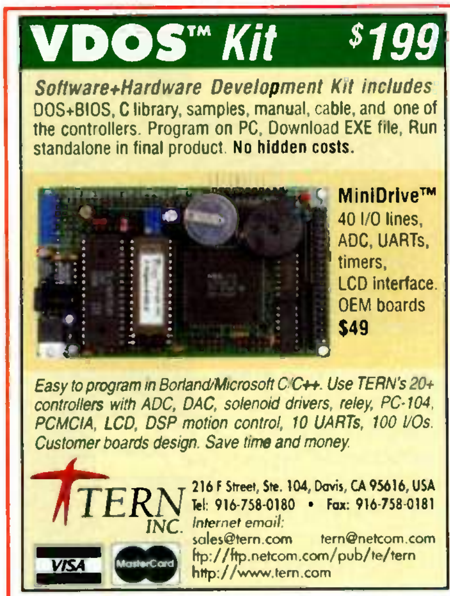

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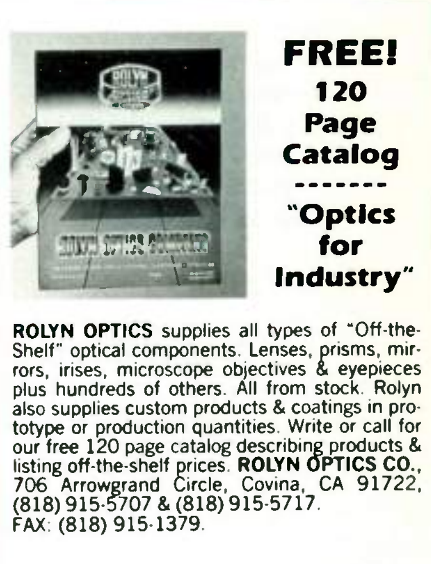

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   1. ☐ Design & Development Engineering Management
   2. ☐ Design & Development Engineering
   3. ☐ General Corporate Management
   ☐ Other (please describe) ______

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   - 07. Design & Development Engineering Management (including R&D - circuits)
   - 12. Design & Development Engineering (including R&D - circuits)
   - 11. Executive & Operating Management (engineering/technical)
   - 01. Corporate & Operating Management (non-engineering)
   - 03. Manufacturing & Production Management (non-engineering)
   - 13. Engineering Services Engineering (evaluation, quality control, reliability, standards, test)
   - 08. Engineering Services Management (evaluation, quality control, reliability, standards, test)
   - 14. Manufacturing & Production Engineering
   - 09. Manufacturing & Production Engineering Management
   - 23. Other (please be specific) ______

4. ☐ What is the PRIMARY end product or service performed at this location? (Insert or circle one code only)
   - 21. Mainframe, Mini/Super Computers
   - 22. PCs, Workstations, Servers
   - 23. Laptops, Notebooks, Hand-helds, and other mobile computers
   - 24. Other Computer/Computer Systems
   - 02. Computer peripherals: disk drives, terminals, printers, plotter
   - 03. CAE/CAD/CAM systems
   - 04. Software manufacturer/developer
   - 05. Computer systems integrator
   - 06. Office & business machines
   - 07. Communications systems & equipment
   - 30. Networks/Software - LAN, WLAN, WAN, etc.,
   - 31. Cellular, Consumer Phones, RF & Microwave Systems
   - 08. Industrial controls, systems, equipment & robotics
   - 09. Electronic instruments, ATE systems, design/test equipment
   - 10. Medical electronic equipment
   - 11. Avionics, marine, space & military electronics
   - 12. Government & military
   - 13. Automotive and other ground vehicles
   - 14. Consumer electronics & appliances
   - 15. ICs & Semiconductors
   - 16. Other components, materials, hardware & supplies
   - 17. Electronic sub-assemblies (boards, modules, hybrids and power supplies)
   - 28. Other (please be specific) ______

5. Do you buy through distributors? ☐ Yes ☐ No
6. Do you design wireless systems or systems that include wireless subsystems or components? ☐ Yes ☐ No
7. Do you design hand held, portable, mobile, nomadic transportable or other products with low power requirements? ☐ Yes ☐ No
8. Do you have or have access to a CD ROM? ☐ Yes ☐ No
9. Do you subscribe or have access to the Internet? ☐ Yes ☐ No
10. Products you specify or authorize purchase of: (Check all codes that apply)

A Digital ICs
01 ☐ Microprocessor Chips & Support ICs
02 ☐ 4/8/16 bit uPs/uCs
04 ☐ 32-bit and larger CISC uPs/uCs
08 ☐ RISC uPs/uCs
16 ☐ Digital Signal Processors
32 ☐ Video Controller

A2
01 ☐ Video Compression/Decompression
02 ☐ Logic ICs
04 ☐ Storage Controller
08 ☐ Memory - DRAM, SRAM
16 ☐ Memory - ROM, PROM, EPROM, EEPROM, Flash
32 ☐ Memory Modules

A3
01 ☐ ICs, other

B Analog/Mixed-Signal Circuits
01 ☐ Mixed Signal Devices
02 ☐ Converter ICs & Modules
04 ☐ Linear ICs & Modules
08 ☐ Communications ICs
16 ☐ Audio Processing
32 ☐ Power Semiconductor Devices

B2
01 ☐ RF Devices
02 ☐ Hybrid Devices
04 ☐ OP Amps

C ASICS
01 ☐ Gate Arrays
02 ☐ FPGA
04 ☐ Programmable Logic Devices (PLD)
08 ☐ Standard Cells
16 ☐ Custom LSI/VLSI
32 ☐ Megacell Functions (CPU cores, etc.)

C2
01 ☐ Analog Cells

D Components
01 ☐ Capacitors, Resistors, Potentiometers
02 ☐ Display Devices
04 ☐ Relays, Switches, Keypads
08 ☐ Fans
16 ☐ Sensors & Transducers
32 ☐ Microwave Components–Hardware & Crystals

D2
01 ☐ Fiber-optic/Optoelectronics
02 ☐ Transformers & Inducters
04 ☐ Fuses
08 ☐ Blowers & Fans
16 ☐ Circuit Breakers

E Interconnections & Packaging
01 ☐ Connectors & Sockets
02 ☐ Wire & Cable
04 ☐ Fiber-optic Cable
08 ☐ Enclosures
16 ☐ Materials
32 ☐ Printed Circuits

E2
01 ☐ EMI/EMC Components & Materials

F Power
01 ☐ Power Supplies
02 ☐ Batteries

G Test & Measurement
01 ☐ Logic Analyzers
02 ☐ Development Systems
04 ☐ Oscilloscopes
08 ☐ Other Test Instruments
16 ☐ ATE
32 ☐ Field Test & Service Equipment

G2
01 ☐ Communications/Test Equipment
02 ☐ Data Acquisition Hardware/Software
04 ☐ EMI/EMC Test Equipment

H Computers & Workstations
01 ☐ Minicomputers
02 ☐ Workstations
04 ☐ Personal Computers

I Computer Boards
01 ☐ CPU Boards
02 ☐ Analog I/O & Converter Boards
04 ☐ Memory
08 ☐ Disk/Tape Controllers
16 ☐ Communication/Interface
32 ☐ Graphics & Imaging Boards

I2
01 ☐ DSP Boards
02 ☐ Other Special Purpose Boards

J Communications
01 ☐ Modems
02 ☐ LAN/WAN Hardware & Software
04 ☐ ISDN Hardware

K Design Automation/CAE/CAD
01 ☐ Digital/Analog Simulators
02 ☐ PCB Layout Tools
04 ☐ IC Design Tools
08 ☐ Design Entry Tools
16 ☐ Synthesis Tools
32 ☐ CASE Tools

K2
01 ☐ HDL Based Tools
02 ☐ Workstation Based Tools
04 ☐ PC Based Tools
08 ☐ CAE/CAD Software

L Software
01 ☐ Software Tools, Dev. Systems and/or High-Level Language
02 ☐ Utility Software Packages & Serv.
04 ☐ Operating Systems
08 ☐ Real-time Operating Systems
16 ☐ Productivity Tools
32 ☐ Compilers/Interpreters

L2
01 ☐ Emulators/Debuggers

M Computer Peripherals
01 ☐ Disk/Tape Drives
02 ☐ Computer Terminals
04 ☐ Monitors
08 ☐ Graphics Terminals
16 ☐ Printers/Plotters
32 ☐ I/O devices (Mice, keyboards, etc.)

M2
01 ☐ PCMCIA Cards
02 ☐ CD-ROM, including WORM & R/W
04 ☐ Multimedia Peripherals

☐ **NONE OF THE ABOVE**

11. Number of employees in your company? ______

12. Please check the publications that you receive personally addressed to you by mail: (check all that apply)

N
01 ☐ Computer Design
02 ☐ ECN
04 ☐ EDN
08 ☐ EE Times
16 ☐ Electronic Product News

O
01 ☐ Electronic Products
02 ☐ PC Week

☐ **NONE OF THE ABOVE**

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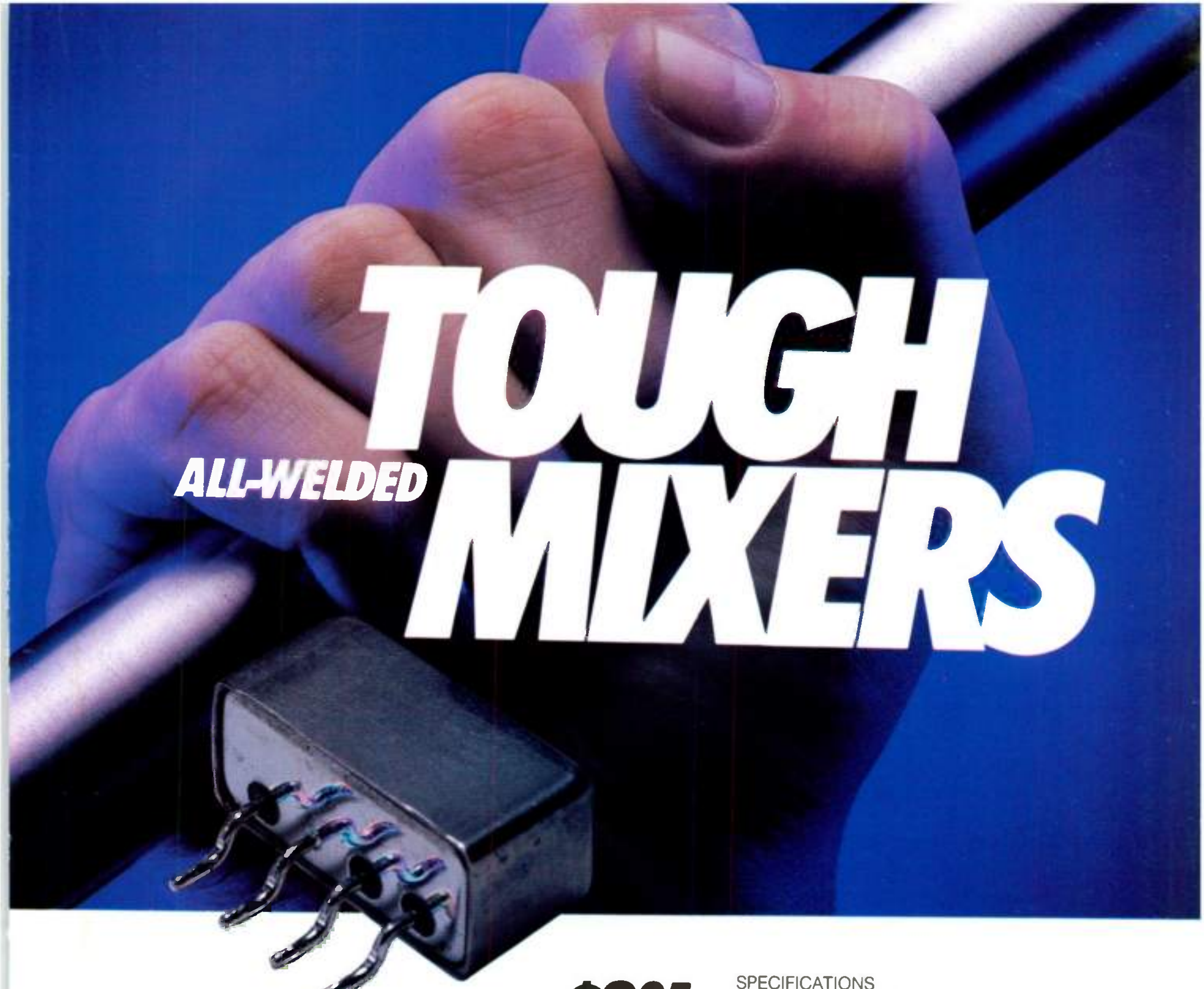

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SPECIFICATIONS

Model	LO Power (dBm)	Freq. LO/RF (MHz)	■ Conv. Loss (dB) $\bar{X}$	δ	Isol. L-R (dB)	Price,$ Ea. 10 qty
TUF-3	7	0.15-400	4.98	0.34	46	5.95
TUF-3LH	10		4.8	0.37	51	7.95
TUF-3MH	13		5.0	0.33	46	8.95
TUF-3H	17		5.0	0.33	50	10.95
TUF-1	7	2-600	5.82	0.19	42	3.95
TUF-1LH	10		6.0	0.17	50	5.95
TUF-1MH	13		6.3	0.12	50	6.95
TUF-1H	17		5.9	0.18	50	8.95
TUF-2	7	50-1000	5.73	0.30	47	4.95
TUF-2LH	10		5.2	0.3	44	6.95
TUF-2MH	13		6.0	0.25	47	7.95
TUF-2H	17		6.2	0.22	47	9.95
TUF-5	7	20-1500	6.58	0.40	42	8.95
TUF-5LH	10		6.9	0.27	42	10.95
TUF-5MH	13		7.0	0.25	41	11.95
TUF-5H	17		7.5	0.17	50	13.95
TUF-860	7	860-1050	6.2	0.37	35	8.95
TUF-860LH	10		6.3	0.27	35	10.95
TUF-860MH	13		6.8	0.32	35	11.95
TUF-860H	17		6.8	0.31	38	13.95
TUF-11A	7	1400-1900	6.83	0.30	33	14.95
TUF-11ALH	10		7.0	0.20	36	16.95
TUF-11AMH	13		7.4	0.20	33	17.95
TUF-11AH	17		7.3	0.28	35	19.95

*To specify surface-mount models, add SM after P/N shown.
■ $\bar{X}$ = Average conversion loss at upper end of midband ($f_u/2$)
δ = Sigma or standard deviation

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