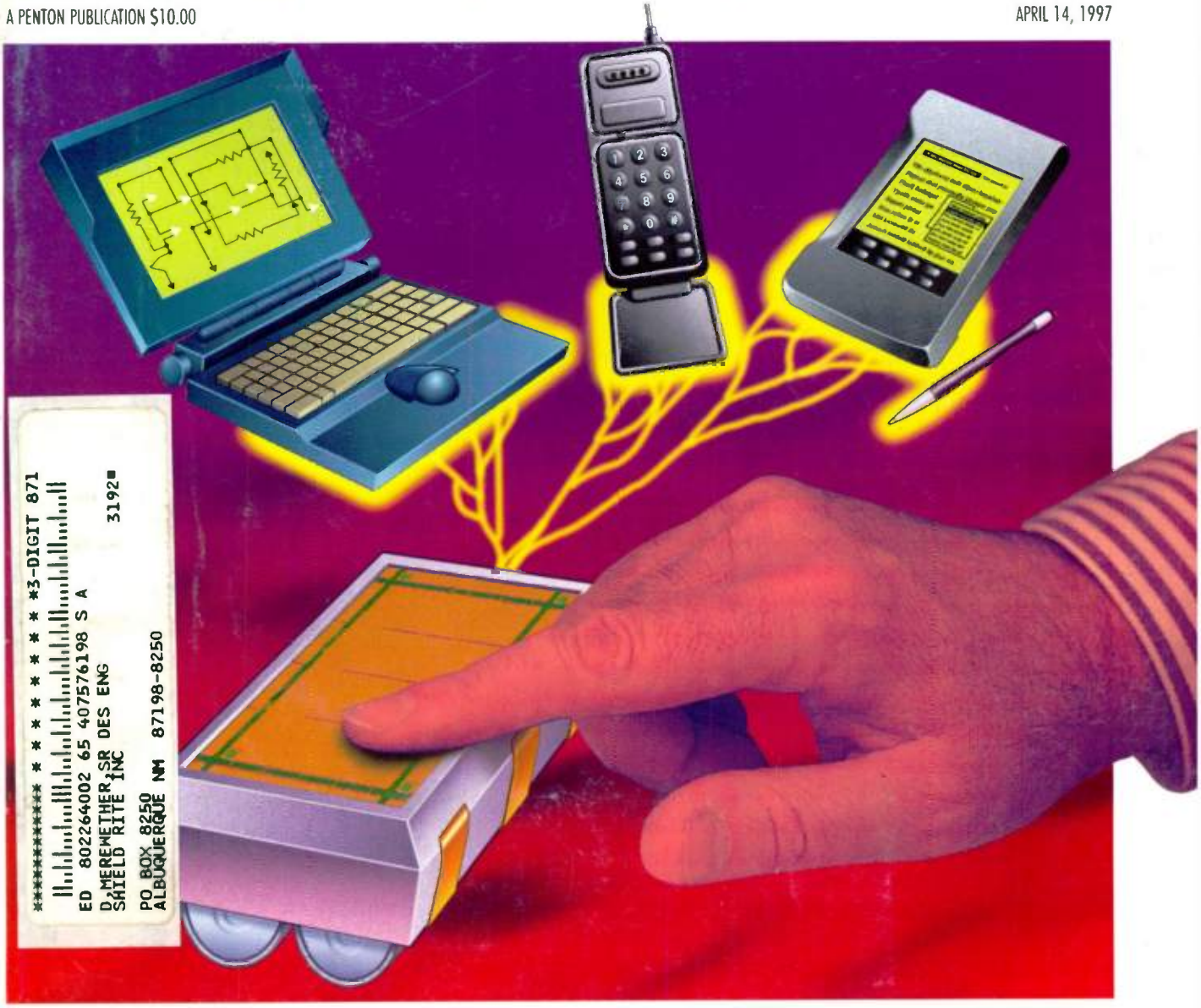
ELECTRONIC DESIGN

FOR ENGINEERS AND ENGINEERING MANAGERS - WORLDWIDE

A PENTON PUBLICATION $10.00

APRIL 14, 1997



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FEATURE	[illegible] 10	[illegible] 20	EPF10K30	EPF10K40	EPF10K50(V)	EPF10K70	EPF10K100
TYPICAL GATES	10,000	20,000	30,000	40,000	50,000	70,000	100,000
MEMORY (bits)	6,144	12,288	12,288	16,384	20,480	18,432	24,576

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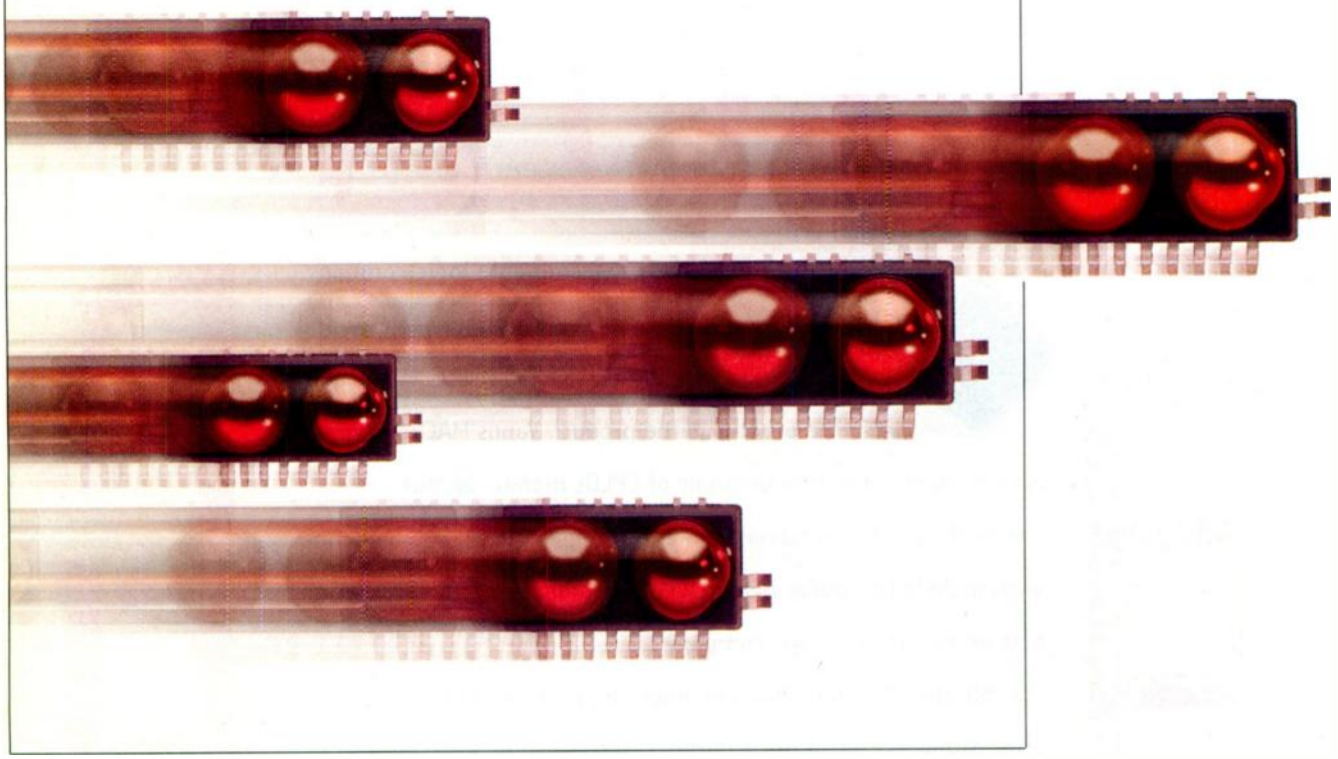

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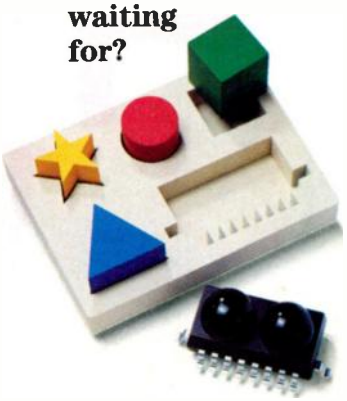

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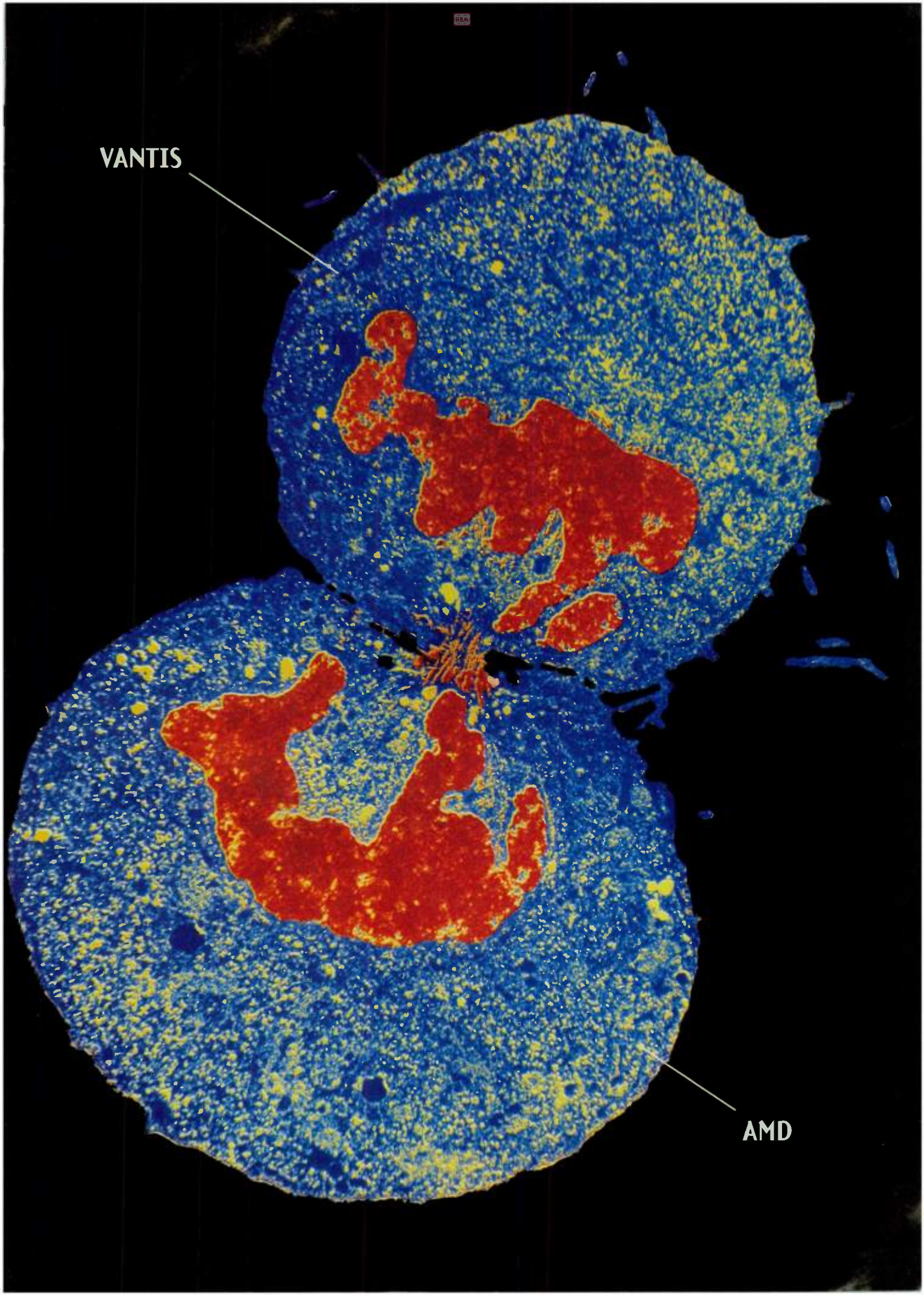
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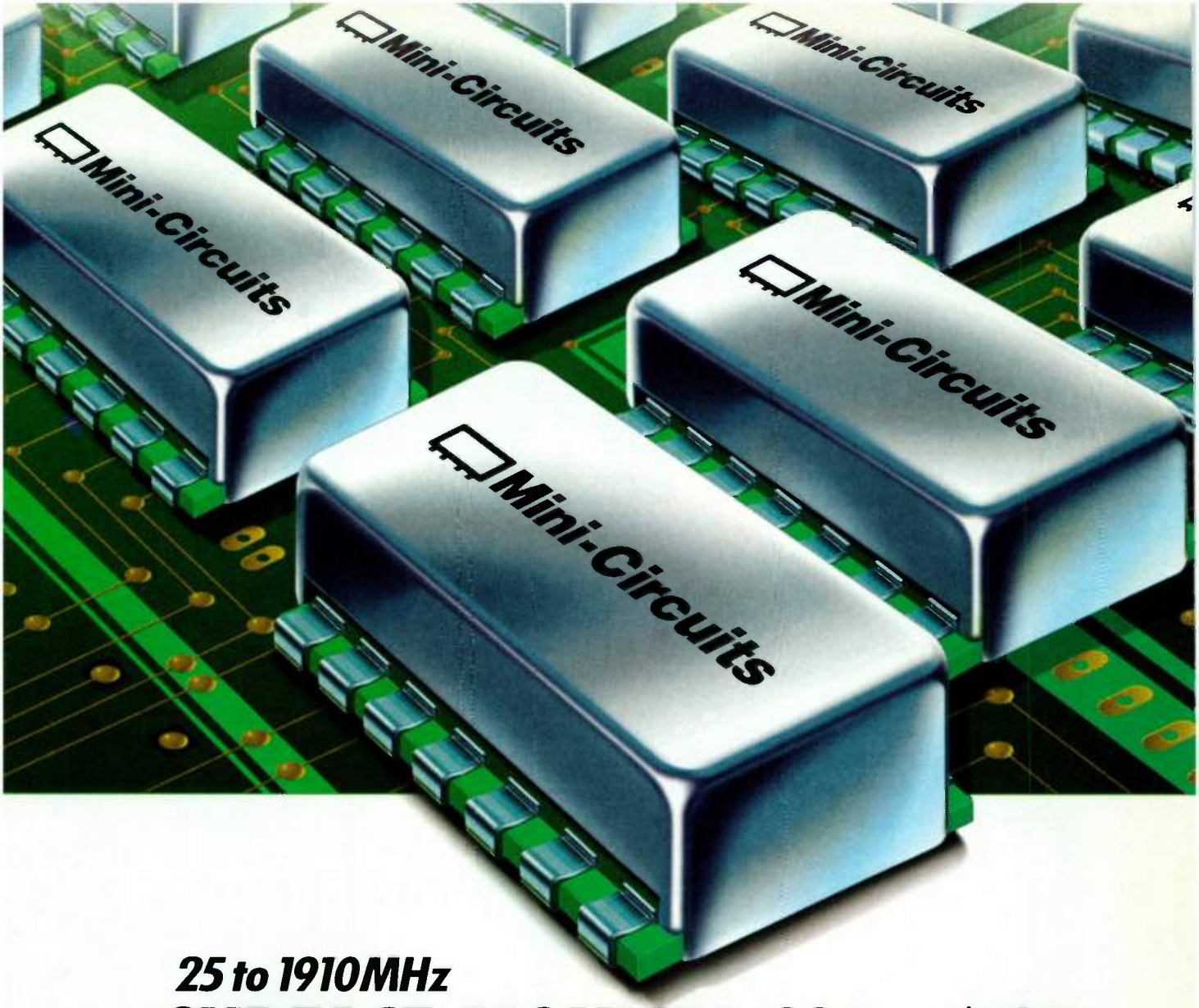

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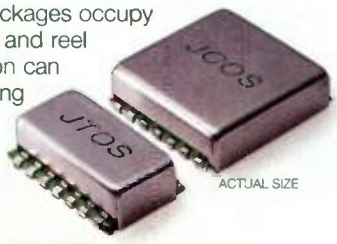

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JTOS-150	75-150	-106	-23	16V	20	13.95
JTOS-200	100-200	-105	-25	16V	20	13.95
JTOS-300	150-280	-102	-28	16V	20	15.95
JTOS-400	200-380	-102	-25	16V	20	15.95
JTOS-535	300-525	-97	-28		20	15.95
JTOS-765	485-765	-98	-30	16V	20	16.95
JTOS-1025	685-1025	-94	-28	16V	22	18.95
JTOS-1300	900-1300	-95	-28	20V	30	18.95
JTOS-1650	1200-1650	-95	-20	13V	30	19.95
JTOS-1910	1625-1910	-92	-13	12V	20	19.95
JCOS-820WLN	780-860	-112	-13	20V	25 (@9V)	49.95
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JCOS-1100LN	1079-1114	-110	-15	20V	25 (@8V)	49.95

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ELECTRONIC DESIGN

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DEPARTMENTS

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ELECTRONIC DESIGN

April 14, 1997 Volume 45, Number 8

EDITORIAL OVERVIEW

EMBEDDED SYSTEMS

DIGITAL DESIGN

MULTIMEDIA

MULTIMEDIA

QUICKLOOK

COVER ILLUSTRATION BY: BRUCE JABLONSKI

Jesse H. Neal Editorial Achievement

1967 First Place Award
1968 First Place Award
1972 Certificate of Merit
1975 Two Certificates of Merit
1976 Certificate of Merit
1978 Certificate of Merit
1980 Certificate of Merit
1986 First Place Award
1989 Certificate of Merit
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IEEE Vehicular Technology Conference (VTC), May 5-7. Hyatt Regency at Civic Plaza, Phoenix, AZ. Contact Wendy Rochelle, IEEE Conference Services, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331; (908) 562-3870; fax (908) 981-1769; e-mail: w.rochelle@ieee.org.

International Test Synthesis Workshop, May 5-7. Santa Barbara, CA. Contact K. Wagner; (415) 694-4386; e-mail: kwagner@symopsys.com.

IEEE Custom Integrated Circuits Conference (CICC '97), May 5-8. Santa Clara Convention Center, Santa Clara, CA. Contact Melissa Widerkehr, Widerkehr & Associates, Suite 270, 101 Lakeforest Blvd, Gaithersburg, MD 20877; (301) 527-0902; fax (301) 527-0994; e-mail: cicc96@aol.com.

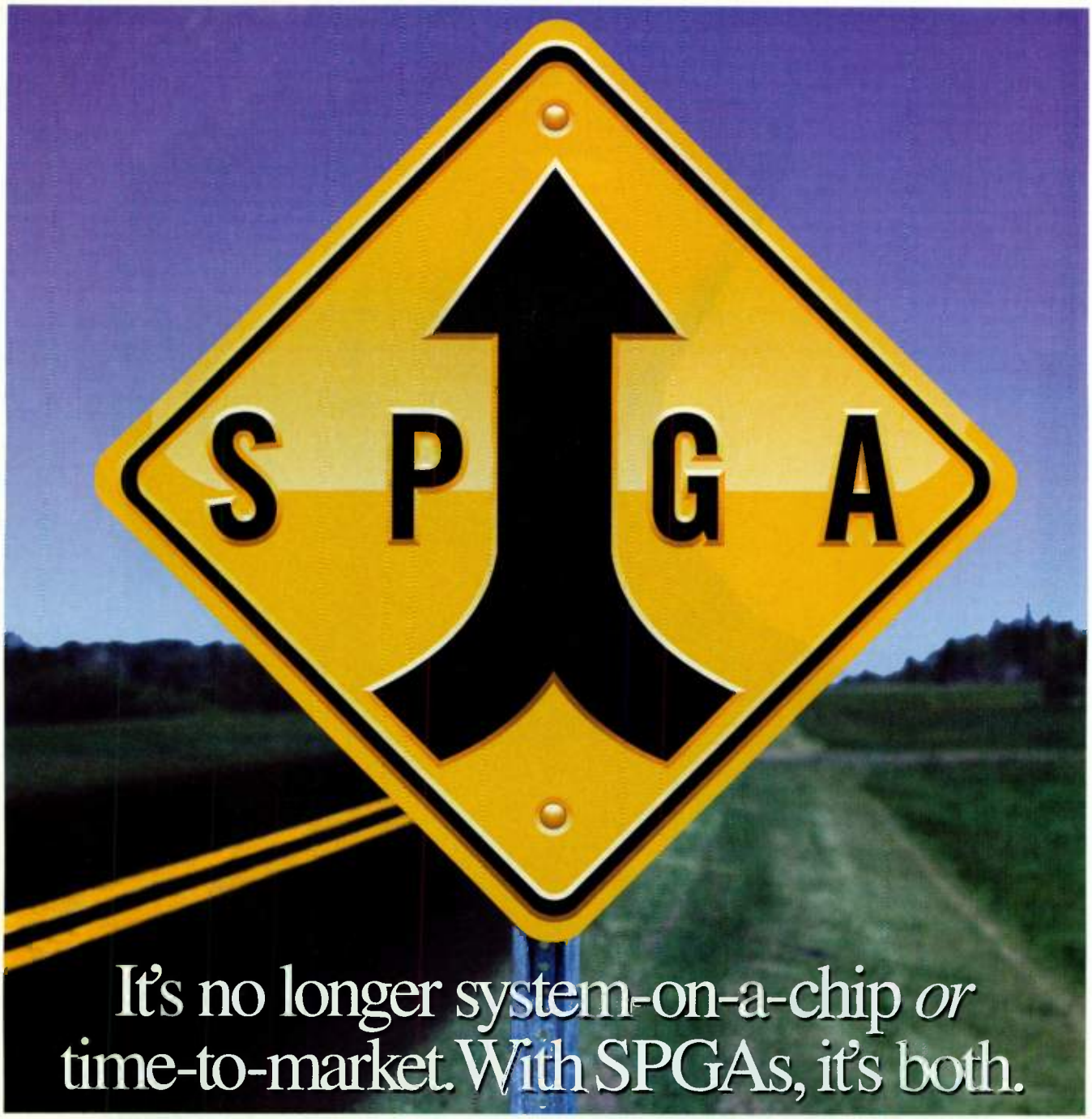
Electronics Industries Forum of New England, May 6-8. World Trade Center, Boston, MA. Contact Summit Exhibition Management Inc., Norwalk CT; (800) 322-9332; (203) 855-3000; fax (203) 855-3003.

Ideas in Science & Electronics (ISE), May 6-8. Albuquerque Convention Center. Contact www.isetradeshow.com/ exhibit or call (505) 872-8020.

Nepcon Shanghai '97/Microelectronics Shanghai '97, May 6-9. Shanghai International Exhibition Centre, Shanghai, China. Contact Sarala Govindan, Export Div., Reed Exhibition Companies, 383 Main Ave., Norwalk, CT 06851; (203) 840-5355; fax (203) 840-9355.

IEEE Power Industry Computer Applications Conference (PICA), May 11-16. Contact T.C. Wong, American Electric Power, 1 Riverside Plaza, Columbus, OH 43215; (614) 223-2235; fax (614) 223-2205; e-mail: t.wong@ieee.org.

Third International Conference on Optical Fiber Submarine Telecommunication Systems (SubOptic'97), May 11-16. Contact Ida M. Espinoza, 340 Mt. Kemble Ave., S120, Morristown, New Jersey 07960; (201) 326-2119; fax (201) 326-2609; e-mail: iespinoza@attmail.com.



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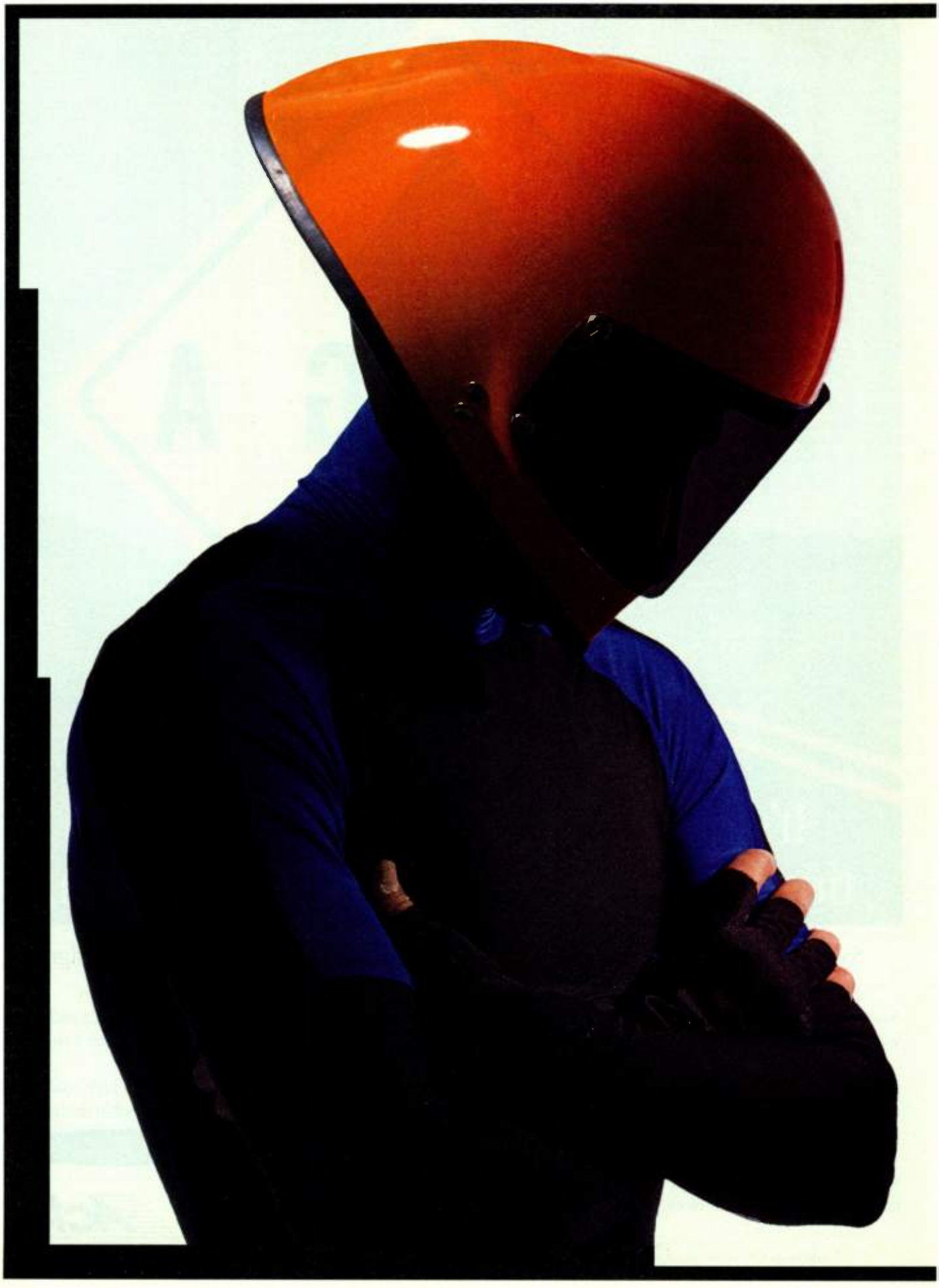

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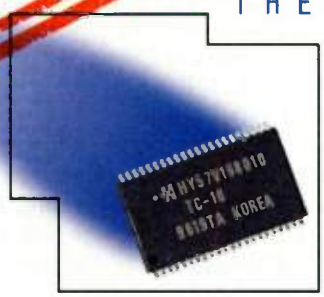

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IEEE/IAS Industrial & Commercial Power Systems Technical Conference (I&CPS), May 12-15. Wynham Hotel, Philadelphia, PA. Contact Barry Hornberger, Philadelphia Electric Co., 2301 Market St., Bldg N3-1, Philadelphia, PA 19101; (215) 841-4619.

Fifth IFIP/IEEE International Symposium on Integrated Network Management (ISINM '97), May 12-16. Hotel Del Coronado, San Diego, CA. Contact Ann Marie Lambert, BBN Systems & Technologies, 10 Moulton St., Cambridge, MA 02138; (617) 873-3819; fax (617) 873-37776; e-mail: isinm97@bbn.com.

IEEE Particle Accelerator Conference, May 12-16. Vancouver, BC, Canada. Contact M.K. Craddock, TRIUMF, 4004 Wesbrook Mall, Vancouver, BC V6T 2A3 Canada; (604) 222-7341; fax (604) 222-7309; e-mail: craddock@triumf.ca.

Antennas: Principles, Design, and Measurements (Short Course), May 13-16. St. Cloud, FL. Contact Kelly Brown, NCEE, 1101 Massachusetts Ave., St. Cloud, FL 34669; fax (407) 892-0406.

IEEE Radar Conference, May 13-15. Sheraton University Hotel & Conference Center, Syracuse, NY. Contact Michael Wicks, Rome Laboratory, 26 Electronics Pkwy., Rome, NY 13441; (315) 330-4437; fax (315) 330-2528; e-mail: wicksm@rl.af.mil.

Sensors Expo Boston, May 13-15. Hynes Convention Center, Boston, MA. Contact Expocon Management Associates Inc. (203) 256-4700; e-mail: sensors@expocon.com; Internet: http://www.expocon.com.

47th Electronic Components & Technology Conference, May 18-21. The Fairmont Hotel, San Jose, CA. Contact Jim Bruorton, Electronic Industries Association, 2500 Wilson Blvd., Arlington, VA 22201-3834; (864) 963-6621.

Finishing '97 Conference & Exposition, May 19-22. Rosemont Convention Center, Rosemont (Chicago), IL. Contact Society of Manufacturing Engineers; (800) 733-4763.

19th IEEE International Conference on Software Engineering, May 19-23. Boston, Massachusetts. Contact W. Richard Adrion, Deptartment of Computer Science, University of Masachusetts/Amherst, 307 LGRC, Post Office Box 34610; Amherst, Massachusetts 01003-4610; (413) 545-2742; e-mail: adrion@cs.umass.edu.

IEEE Instrumentation & Measurement Technology Conference (MTC '97), May 20-22. Chateau Laurier, Ottawa, Ontario, Canada. Contact Robert Myers, Conference Coordinator, 3685 Motor Ave., Suite 240, Los Angeles, California 90034; (310) 287-1463; fax (310) 287-1851; e-mail: bob.myers@ieee.org.

OEMed Midwest, May 21-22. Rosemont Convention Center, Rosemont, IL. Contact Exposition Excellence Corp., 112 Main St., Norwalk, CT 06851; (203) 847-9599; fax (203) 854-9438.

OEM Electronics Midwest, May 21-22. Rosemont Convention Center, Rosemont, IL. Contact Exposition Excellence Corp., 112 Main St., Norwalk, CT 06851; (203) 847-9599; fax (203) 854-9438.

Canadian Conference on Electrical & Computer Engineering, May 25-28. Delta Hotel, Newfoundland, Canada. Contact David Collett, Newfound land & Labrador Hydro, P.O. Box 12400, St. Johns, NF, A1A 4K7, Canada; (709) 737-1372; fax (709) 737-1782; e-mail: t.d.collett@ieee.org.

Fifth IEEE International Conference on Properties & Applications of Dielectric Materials (ICPADM), May 25-30. Sheraton Walker Hill, Convention Center, Seoul, Korea. Contact Joon-Ung Lee, Department of Electrical Engineering, Kwangwoon University, 447-1 Wolgye-Dong, Nowon-Ku, Seoul, 139-701, Korea; (82)-2-910-5144; fax (82)-2-942-0107.

Next Generation Telephony West: Voice Over the Internet, May 28-30. Hotel Monaco, San Francisco, California. Contact (800) 822-6338 or (202) 842-3022 ext.317; Internet: http://www.brp.com.

JUNE

IEEE International Conference on Neural Networks, June 1-5. Houston, TX. Contact Nicolaos B. Karayiannis, Dept. of Electrical & Computer Engineering, University of Houston, Houston, TX; 77204-4793 (713) 743-4436; fax (713) 743-4444.

International Symposium on VSLI Technology, Systems, and Applications, June 3-5. Grand Hyatt Hotel, Taiwan, China. Contact T. P. Ma, Dept. of Electrical Engineering, Yale University, 15 Prospect St., New Haven, CT 06520-8284; (203) 432-4211; fax (203) 432-7769.

Mixed Signal Test Workshop; June 3-6. Seattle, WA. Contact M. Soma; (206) 685-3810; e-mail: soma@ee.washington.edu.

American Control Conference (ACC '97), June 4-6. Albuquerque Convention Center, Albuquerque, New Mexico. Contact Steven Yurkovich, Department of Elec. and Engrg., The Ohio State Univ., 2015 Neil Avenue, Columbus, Ohio 43210; (614) 292-2586; fax (614) 292-7596; e-mail: s.yurkovich@i.ee.org.

IEEE International Conference on Communications (ICC 97), June 8-12. Montreal, Canada. Contact Celia Desmond, Stentor, Fl. 6b, 33 City Center Dr., Mississauga, Ontario L5B 2N5, Canada; (905) 615-6507; fax (905) 615-8421; e-mail: celia.desmond@tc.resonet.com.

IEEE/MTT-S International Microwave Symposium (MTT 97), June 8-13. Convention Center, Denver, CO. Contact John Dunn, Dept. of Electrical & Computer Engineering, University of Colorado, Campus Box 425, Boulder, CO 80309; (303) 492-5920; fax (303) 492-5323; e-mail: dunn@boulder.colorado.edu.

IEEE International Symposium on Circuits & Systems (ISCAS 97), June 9-12. Hong Kong Convention & Exhibition Centre, Hong Kong. Contact ISCAS '97 Secretariat, Department of Electrical & Electronic Engineering, University of Hong Kong, Pokfalam Rd., Hong Kong; (852) 28592710; fax (852) 25598738; e-mail: iscas97@hkueee.hku.hk.

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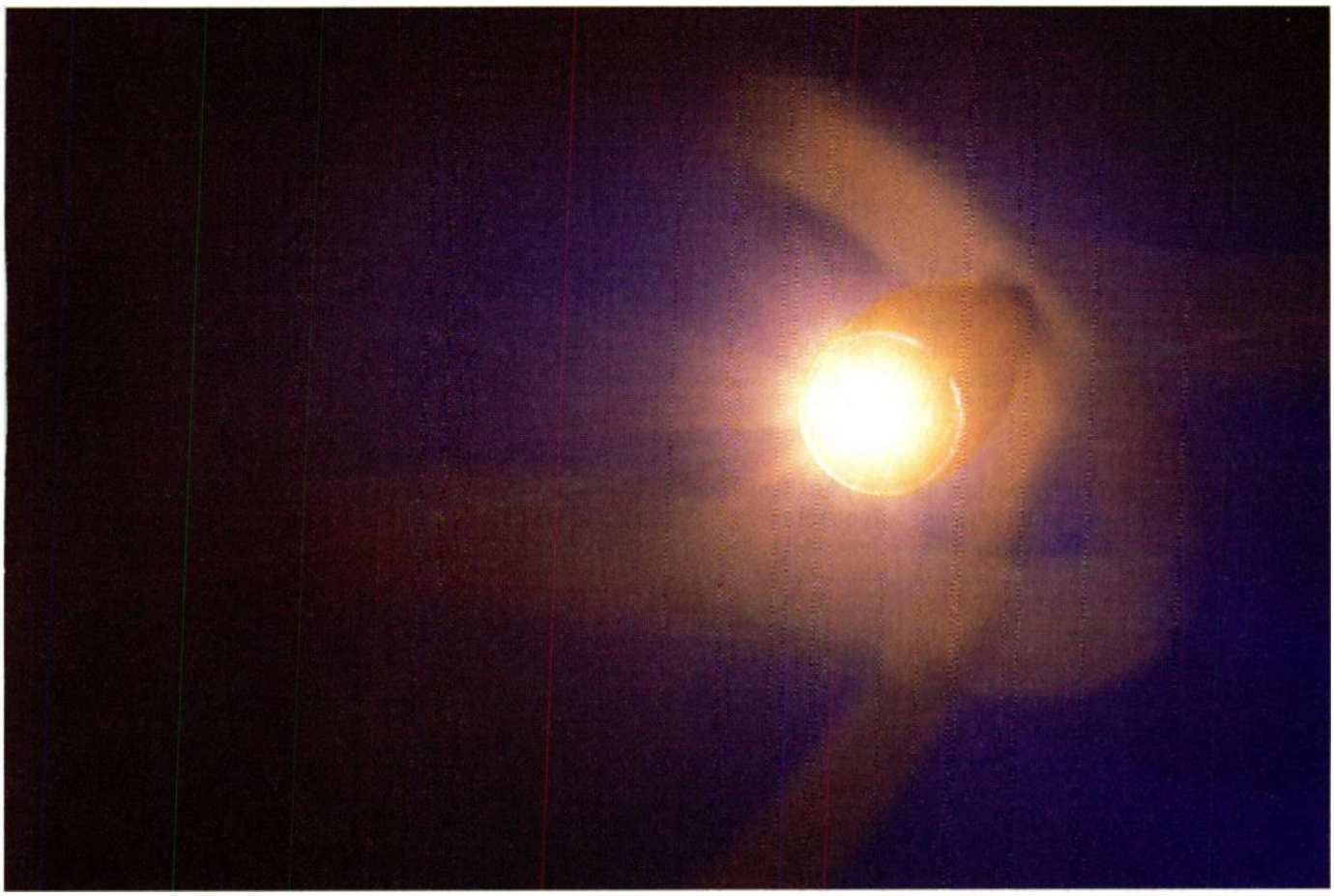

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JUNE

34th Design Automation Conference (DAC '97), June 9-13. Anaheim Convention Center, Anaheim, California Contact MP Associates Inc., 5305 Spine Rd., Suite A, Boulder, CO 80301; (303) 530-4333; fax (303) 530-4334.

ASIA TELECOM '97 (TIA), June 9-14. Singapore, Asia. Contact (703) 907-7736.

IEEE International Conference on Consumer Electronics (ICCE), June 11-13. The Westin Hotel O'Hare, Rosemont, IL. Contact Diane D. Williams, 67 Raspberry Patch Dr., Rochester, NY 14612-2868; (716) 392-3862; fax (716) 392-4397.

Virginia Tech/MPRG Symposium on Wireless Personal Communications, June 11-13. Campus of Virginia Tech, Blacksburg, VA. Contact MPRG Conference Coordinator Jenny Frank (757) 686-3765, or Jack Lilly, (540) 231-4849.

International Solid-State Sensors and Actuators Conference (Transducers 97), June 15-19. Hyatt Regency Hotel, Chicago, Illinois. Contact Kensal D. Wise, 1246 EECS Building, University of Michigan, 1301 Beal Avenue, Ann Arbor, Michigan 48109-2122; (313) 764-3346; fax (313) 747-1781.

IEEE Digital Cross Connect Systems Workshop VII (DCS 97), June 16-19. Banff Park Lodge, Banff, Alberta, Canada. Contact James H. Simester, Lucent Technologies, Post Office Box 3030, Room 4J-526, 101 Crawfords Corner Rd., Holmdel, New Jersey 07733-3030; (908) 949-7336; fax (908) 949-2724; e-mail: sims@bostare.ho.att.com.

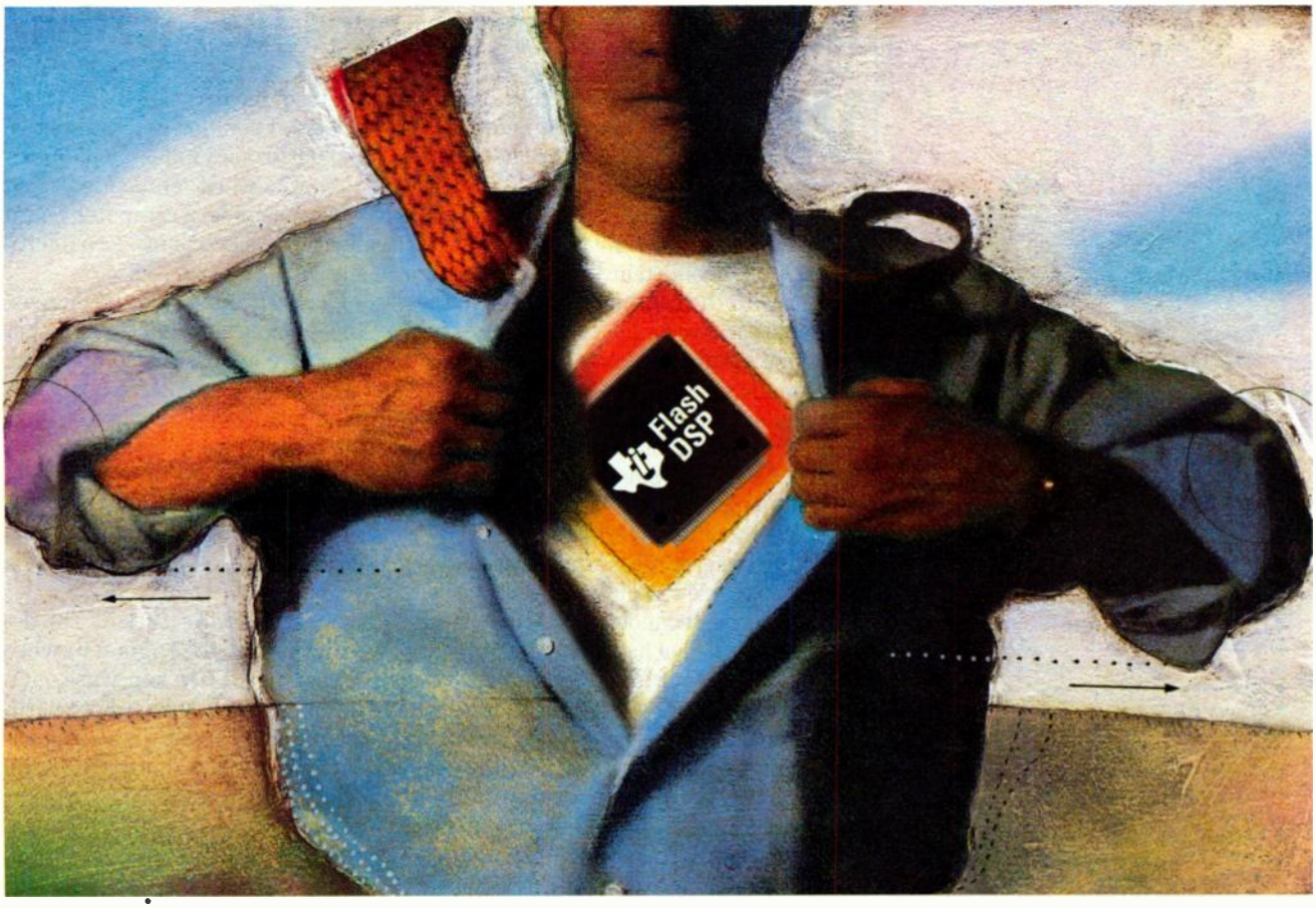
Third Conference on Object-Oriented Technologies & Systems (Coots 97), June 16-19. Marriott Hotel, Portland, OR. Contact USENIX Conference Office, 22672 Lambert Street, Suite 613, Lake Forest, California 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

IEEE International Conference on Systems, Man, and Cybernetics, June 16-20. Hyatt Orlando, Orlando, FL. Contact James M. Tien, Chair, DSES Department, Rensselaer Polytechnic Institute, Troy, New York 12180-3590; (518) 276-6486; fax (518) 276-8227; e-mail: tienj@rpi.edu.

IEEE/ASME International Conference on Advanced Intelligence Mechatronics, June 16-20. Contact Hideki Hashimoto, Institute of Industrial Science, University of Tokyo, 7-22-1, Roppongi, Minato-ku, Tokyo 100, Japan; (81) 3 3402 6231 ext. 2359; fax (81) 3 3423 1484.

IEEE Sixth International Fuzzy Systems Conference, June 20-25. Barcelona, Spain. Contact Ramon Lopez De Mantaras, IIIA-CSIC Campus U.A.B., 08193 Cerdanyola del Valles, Spain; (34) 3-580-95-70.

D I G I T A L S I G N A L P R O C E S S O R S



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EDITORIAL

Embedded Systems Change The Equation

While walking around the exhibitor booths at last month's Embedded Systems Conference East show in Boston, Mass., I couldn't help but notice the profound difference between how the electronics industry did business a couple of decades ago and today. Back then, the word "embedded" conjured up images of largely military applications; for example, a computer board embedded within a fighter aircraft's countermeasures electronics, or a microprocessor embedded in a tank's fire-control system.

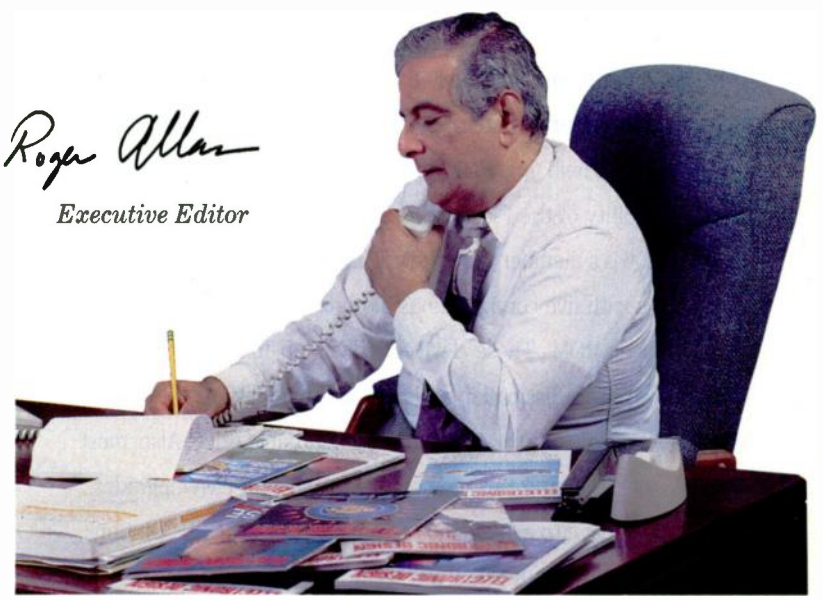
But with the continuous decline in the cost of hardware ICs and the increasing sophistication in the performance levels of these chips, new market opportunities have rapidly opened up in consumer, automotive, industrial, commercial, and communications sectors. This means that OEM designers must not only satisfy challenging technical performance requirements, they also must know their end-user applications that can be as varied as an office or home fax machine, a bank ATM, or a sophisticated factory floor controller. The home is seen as a potentially huge future market for embedded microcontrollers. For example, it is estimated that the average middle-class consumer household now has about 30 embedded microprocessors in various devices and appliances, a number that is projected to grow rapidly.

Electronics technology has thus become very pervasive. As a result, the design equation also has changed. It used to be that hardware engineers were mostly responsible for circuit designs. In some cases, one or two hardware engineers were all that were needed for a design. The challenge now is for both hardware and software designers to work closely together to come up with innovative solutions. No longer is electronic design a one-person show. It's truly a team effort, and a multidisciplinary one at that. Packaging, test, mechanical, and industrial designers are frequently involved.

Advanced 32- and 64-bit CISC and RISC processors, flash memory, and various forms of logic are readily available to suit many applications. But these advanced hardware devices can only work within the right software design environment. They're only as good as the software languages and programming techniques, the simulation and emulation tools, the operating system, and the development environment that make possible getting the most performance out of hardware components. On the other hand, software designers might just as well "sit on their hands" if they didn't have the latest hardware elements with which they can ply their magic. What all this means is that the average engineer today must have a wider view of issues that often go far beyond his or her primary areas of expertise. *rallan@class.org*

Roger Allan

Executive Editor



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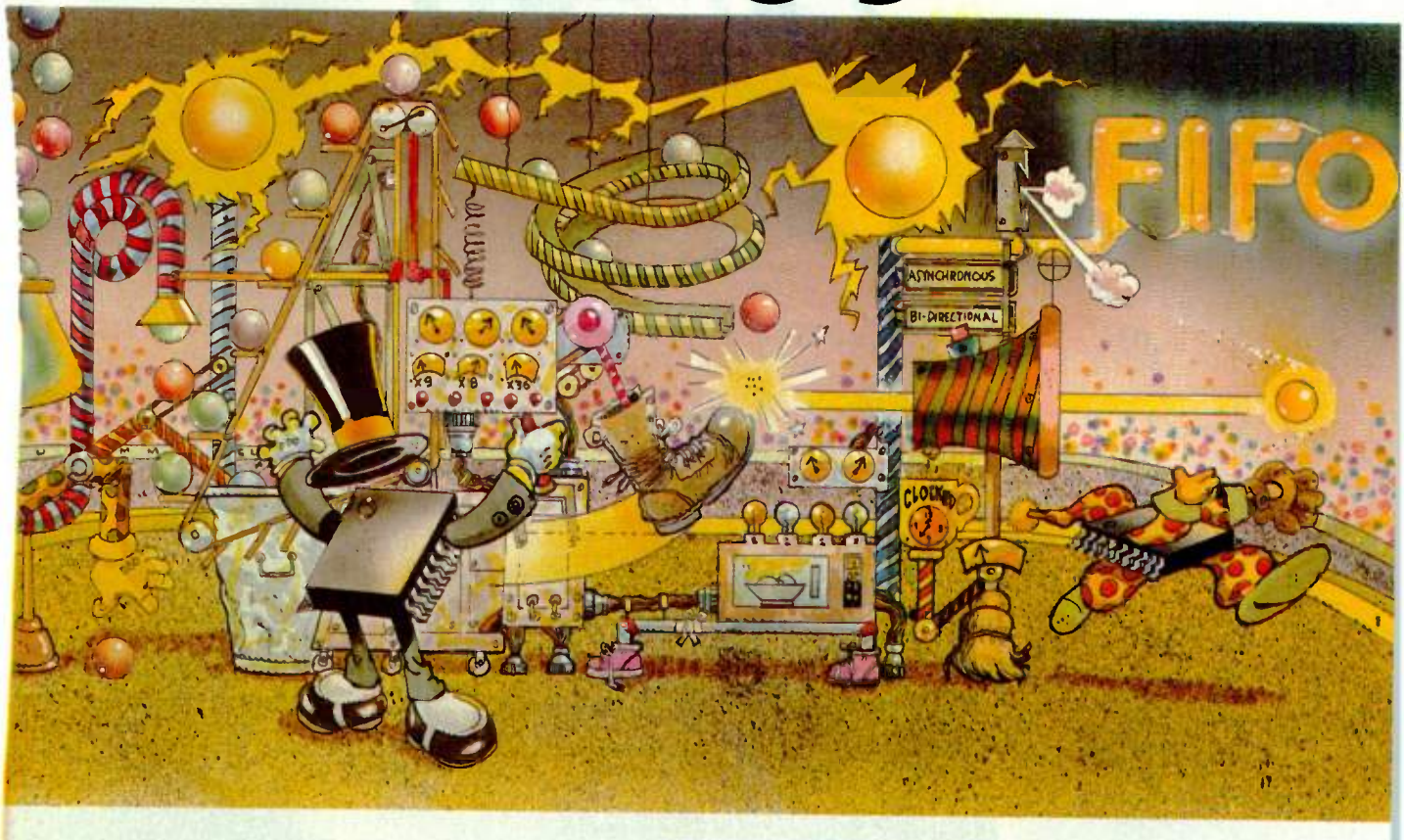

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QS72211	512 x 9 Parallel Synchronous	32
QS72221	1K x 9 Parallel Synchronous	32
QS72231	2K x 9 Parallel Synchronous	32
QS72241	4K x 9 Parallel Synchronous	32
Clocked x18 FIFOs		
QS72215	512 x 18 Parallel Synchronous	68
QS72225	1K x 18 Parallel Synchronous	64
Clocked x36 FIFOs		
QS723611	512 x 36 x 2 Bidirectional Clocked FIFO with Dynamic Bus Sizing	144
QS723620	1K x 36 Clocked FIFO with Dynamic Bus Sizing	132
QS723621	1K x 36 x 2 Bidirectional Clocked FIFO with Dynamic Bus Sizing	144
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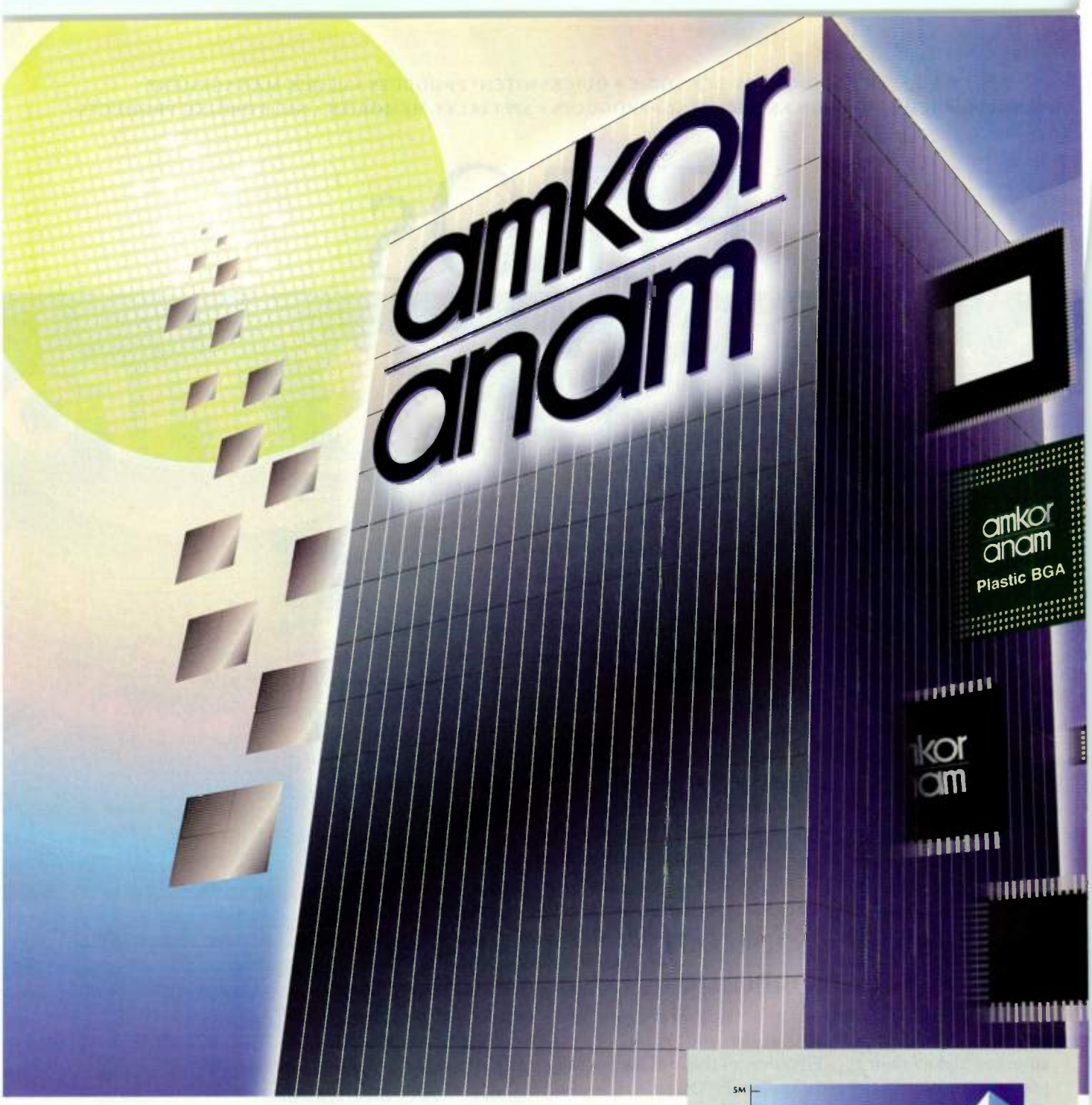

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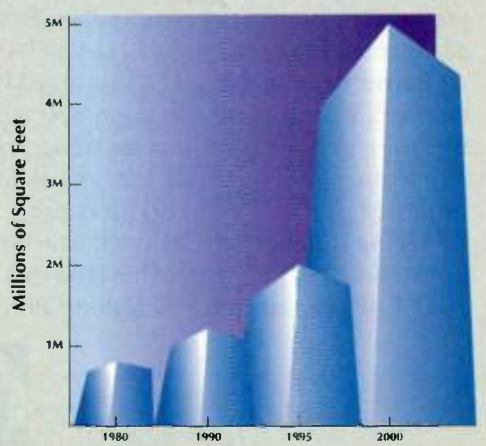

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READER SERVICE 98

The New EDA Intellectual Property

Everywhere I go, the topic of human resources, and its current role in business, comes up. At first, it seemed like an odd topic for the electronic design automation (EDA) industry, but at a recent press conference, Gerry Hsu, president and CEO of Avant!, said, "Technology is changing so quickly today there is not enough time or energy to spend on dealing with tough problems like employees that aren't performing. A number one company needs number one people. A high-tech company today must hire and retain the most talented people to keep turning out products that consumers will buy."

What he said represents a subtle shift in the high-tech arena, although the trend toward employees as a valued commodity is increasingly obvious. Qualified employees are now seen as a company's own "intellectual property," as opposed to worker bees. The workforce is now a vital link in the successful development and commercialization of technology. Who'd have thought 10 years ago that a point of differentiation between companies would be whose employees stay later at night to get more work done? Qualified employees are now bargaining chips, drawing large salaries, high sign-on and yearly bonuses, and other perks.

But if qualified employees are such a hot commodity, then why is it that the EDA industry doesn't better meet the needs of its people? Ask any designer to list their biggest complaints, and guaranteed on the list will be that vendors do not provide them with tools that are flexible and simple to use, or even with tools that match current technology capabilities. While most vendors acknowledge this gap, I wonder if anyone is really listening.

CHERYL AJLUNI
DESIGN AUTOMATION

While researching the analog/mixed-signal (A/MS) special report on the emergence of A/MS HDL standards in this issue's EDA section, I was confronted with a similar view of the industry. Many realize the benefits of standardizing A/MS HDL's, and are working to ensure that they will be available for use as current design solutions grow old. But, as Mentor Graphics, San Jose, Calif., pointed out, when analog/mixed-signal HDL language standards do come out, designers will still use what they already have because it gets the job done, albeit the hard way. It seems that many people still miss the point.

The standards will bring benefits not previously possible with the free-style design approach used by many A/MS designers. But what seems to have been forgotten is how the designers will move from their current solutions to standards-based solutions. And what migration path has been set to ensure that this transition will be as painless as possible?

Mentor has the right approach to the issue. When asked what would happen to its HDL-A language once the standards become available, they said that HDL-A is just a temporary solution until the standards take effect. Mentor now has a clear migration path that will transition its current tool users to the standards when available. In effect, the company's HDL-A v3 will be the same as the VHDL A/MS standard. They understand its role to support the development of emerging standards, and to provide a migration path to its users.

The EDA industry can't just focus on the development of technology. Rather, it must seek ways to implement and transition designers to that new technology. Organizing study groups to evaluate the future needs of designers in the analog/mixed-signal area is only half the answer. Vendors need to plot out a migration path for designers that will enable a quick and easy transition from what they use today into what they will use tomorrow.

If someone tells you their company is number one because you'll see cars in its parking lot after 5 p.m., ask them to clarify. Are they working late because they're being productive, or because they can't figure out how to use their design tools to meet their tight product-cycle deadlines? *cjajluni@class.org*

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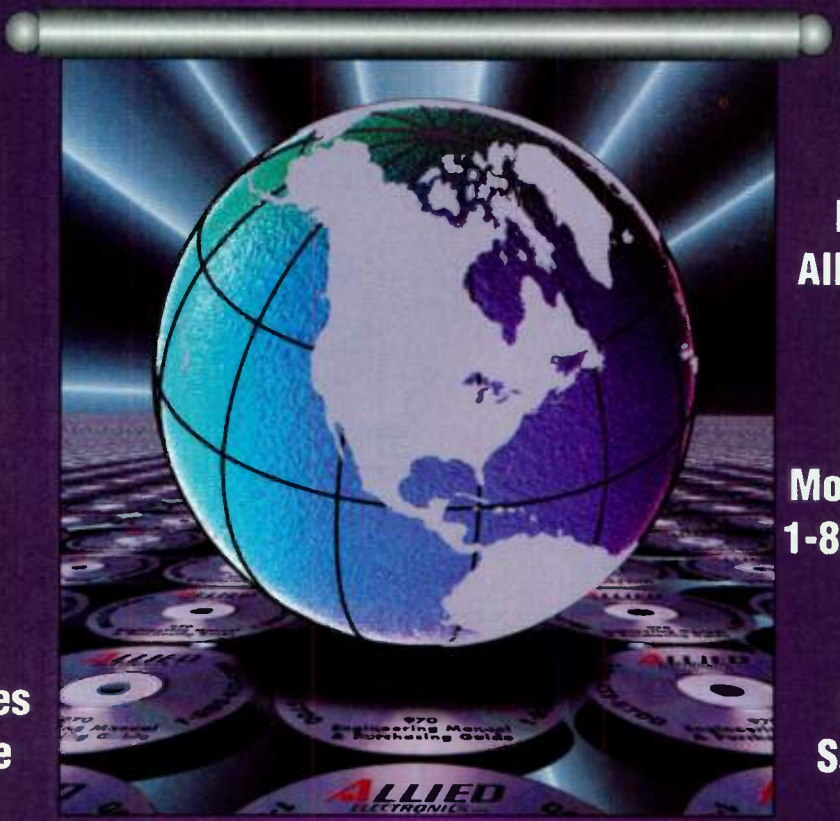

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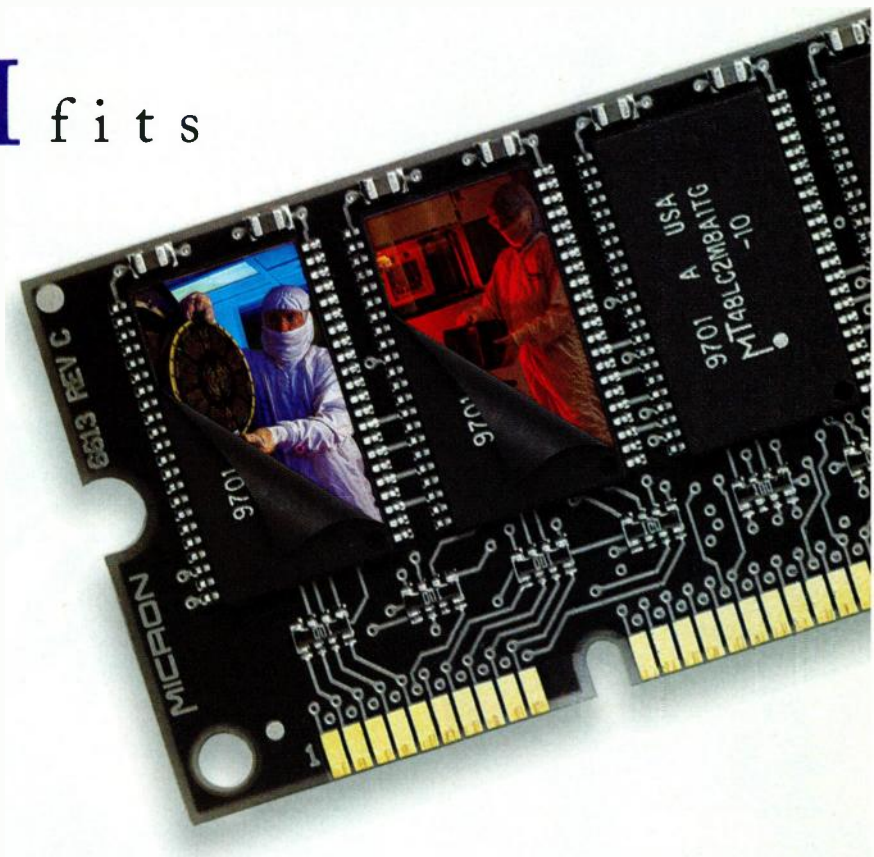

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2 Meg x 64/72	168-pin DIMM	256K x 32 SGRAM component)
4 Meg x 64/72	168-pin DIMM	

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JUNE

IEEE Power Electronics Specialist Conference (PESC 97), June 22-27. Regal Riverfront Hotel, St. Louis, Missouri Contact Philip T. Krein, University of Illinois, 1406 West Green Street, Urbana, Illinois 61801; (217) 333-4732; e-mail: krein@uipesl.ece.uiuc.edu.

IEEE International Symposium on Information Theory, June 29-July 4. Ulm, Germany. Contact Han Vinck, Institue of Experimental Mathematics, University of Essen, Ellernstr. 29, 45326 Essen, Germany; (49) 201 3206458; fax (49) 201 3206425.

Sixth IEEE International Fuzzy Systems Conference, June 30-July 5. Barcelona, Spain. Contact Ramon Lopez de Mantaras, IIIA-CSIC Campus U.A.B. 08193 Cerdanyola del Valles, Spain; (34) 3 580 95 70.

JULY

Fifth TCL/TK Workshop, July 14-17. Tremont House Hotel, Boston Massachusetts. Contact USENIX Conference Office, 22672 Lambert Street, Suite 613, Lake Forest, California 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

IEEE Power Engineering Society Summer Meeting, July 20-25. Intercontinental Hotel, Berlin, Germany. Contact Executive Office, IEEE Power Engineering Society, Post Office Box 1331, Piscataway, New Jersey 08855-1331; (908) 562-3864; fax (908) 981-1769.

IEEE Signal Processing Workshop on Higher Order Statistics, July 21-23. Banff Centre for Conferences, Banff, Alberta, Canada. Contact Keh-Shin Lii, Department of Statistics, University of California, Riverside, 900 University Ave., Riverside, California 92521; (909) 787-3836; fax (909) 787-3286; e-mail: ksl@ucrstat.ucr.edu.

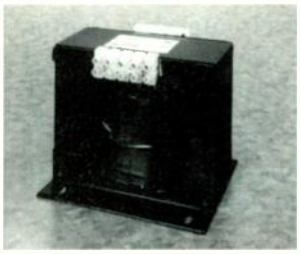
IEEE Nuclear & Space Radiation Effects Conference (NSREC '97), July 21-25. Snowmass Conference Center, Snowmass, Colorado. Contact Dennis B. Brown, Naval Research Laboratory, Code 6612, Washington, DC. 20375; (202) 767-5453; fax (202) 404-8076; e-mail: dbbrown@ccfnrl.nvy.mil.

AUGUST

40th Midwest Symposium on Circuits and Systems, Aug. 2-6. Hyatt Regency Hotel, Sacramento, California. Contact Sharon Baumgartner, Department of E&CE, University of California, Davis, California 95616; (916) 754-6216; fax (916) 752-8428; e-mail:mwscas97@ece.ucdavis.edu.

IEEE International Geoscience & Remote Sensing Symposium (IGARSS '97), Aug. 4-8. Singapore International Convention Exhibition Centre, Suntec City, Singapore. Contact Kwoh Leong Keong, CRISP, National University of Singapore, Faculty of Science, Lower Kent Ridge Rd., S 119260 Singapore; (65) 7727838.

High Power International Transformers



Signal's HPI transformers incorporate unique coil construction that complies with international safety standards that results in a smaller and lighter transformer. The HPI transformers operate from 2000 VA to 3500 VA, have dielectric strength of 4000 VRMS Hipot, and leakage current that meets medical applications.

The transformers are recognized to UL 506 and certified to CSA C22.2 #66, VDE 0550 and TUV IEC 950.

CONTACT: Signal Transformer Co., Insilco Technologies Group, 500 Bayview Ave., Inwood, NY 11096-1792. Phone: (516) 239-5777; fax: (516) 239-7208.

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International Printed Circuit Transformers

Signal Transformeris One-4-All™ (14A) printed circuit mount transformers are designed for use in international low power applications. Recognized to UL 506 and certified to CSA C22.2 #66, VDE 0805 / EN 60950, and IEC 950, the transformers also have the creepage and clearance necessary to comply with international safety standards.

With an operating power range of 2.5 VA to 56 VA, the transformers are used in low power applications and provide high isolation of 4000 VRMS Hipot.

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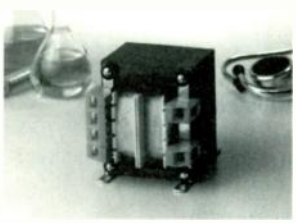
More-4-Less™ International Transformers



Signal's M4L Series high-power, isolation transformers satisfy UL, VDE, IEC, and CSA transformer requirements for low power isolation in numerous applications.

The M4L Series transformers comply with UL 544, the standard for both medical and dental equipment, and UL 506, the standard for specialty purpose transformers with 250 volt or less input. They are available in models from 300 VA to 1,000 VA, are extremely compact, and lighter than conventionally wound transformers.

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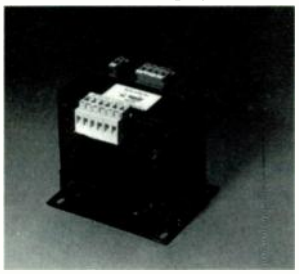
Multi-Purpose International Transformers

Signal Transformer's Multi-Purpose International Series (MPI) high-power transformers operate from 200 VA to 900 VA and feature higher volumetric efficiency than conventional 50/60 Hz transformers.



Featuring unique coil construction and winding methods, the MPI transformers have exceptionally good isolation of 4000 VRMS Hipot and low leakage current. They also have a 5 mil thick copper Faraday shield to reduce common mode noise. Faston/screw type shock-proof terminals are used on the series.

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READER SERVICE 230

Laser Blasts—The Next Step For Smaller, More-Powerful Chips

The discovery of a new technique for processing ultra-high-density semiconductors could lead to a new generation of smaller, more-powerful and energy-efficient microprocessors. The new method, which uses powerful laser blasts instead of a conventional heating process, is being developed at the Naval Research Lab, Washington D.C., in conjunction with physicists from Sam Houston State University, Huntsville, Texas.

Currently, microprocessors are produced from a single crystal of silicon that's manipulated by adding dopants, which transform the silicon's electrical properties, thus creating miniature transistors. These dopants are introduced to the silicon by a high-speed beam that penetrates the surface. What happens, though, is that during this process, the silicon crystal becomes damaged. To repair the damage and electrically activate the dopants, the crystal must undergo annealing, whereby atoms are, so to speak, forcibly repositioned. Annealing involves heating the dopant-implanted ("doped") silicon in high-temperature ovens. But, if the chips are small, they will diffuse during the procedure. This limits the size and density of transistors implanted on the silicon crystal, and, ultimately, the size of the computer chip. The annealing process also limits the number of chips that can be produced from a single silicon wafer.

The new laser-beam process repairs and activates the doped silicon crystal. According to Sam Houston physicist Billy Donnelly, "It's just like hitting it with a hammer." The atoms are literally rattled into proper alignment, correcting the defects and activating the chip's electrical properties. Such a process will allow much smaller, more densely packed transistors to be fabricated, leading to smaller chips requiring less power to operate. Less power means less heat generated, which means more transistors can be crammed into a smaller chip. Non-thermal annealing also could eradicate problems with heating larger silicon wafers, which could result in more chips being fabricated in considerably less time: The thermal process requires the silicon to bake about an hour in a high-temperature oven, while the non-thermal method involves only a 5-ns blast from a pulse laser.

For additional information, call (409) 294-1836; fax (409) 294-1834. RE

ATP Announces Eight New Projects In Key Technology Areas

The U.S. National Institute of Standards and Technology revealed that eight research projects, cost-shared with U.S. industry under the Advanced Technology Program (ATP), will be undertaken to resolve issues revolving around economically important new capabilities in electronics, biotechnology, energy, and polymer recycling. The projects were chosen from the ATP 1996 General Competition, in which open proposals from any area of technology are put under peer review. The review considers each submission's technical and scientific merit, plus its potential benefits to the U.S. economy, and awards are made on those deemed most qualified.

The eight projects are:

- Direct oxidation of natural gas to methanol and transportation fuels
- Enabling large-scale recovery of plastics from durable goods.
- Programmable nanoscale engines for molecular separation.
- A portable genetic analysis system.
- Cost-effective planar solid oxide fuel cells for distributed power generation.
- High-performance sensor arrays for digital x-ray and visible light imaging.
- Color sequential imaging.
- Development of novel DNA binding proteins as antiviral therapeutics.

If carried through to completion, the eight projects will be valued at $36.9 million, with approximately $17.6 million in funding from private industry and $19.3 million in ATP funding. To see more about these projects, check the ATP's web site at http://www.atp.nist.gov. RE

Dual-Speaker 3D Sound Algorithm Provides 360°Field

Another 3D sound algorithm, called the RSX 3D, has arrived that goes beyond most other positional sound 3D approaches by offering 360° lateral sound positioning as well as vertical positioning. Most other 3D schemes only offer a 180° sound plane plus vertical positioning. Employing just two speakers, the RSX (realistic sound experience) 3D software developed by Intel Corp., Hillsboro, Ore., incorporates 3D interactive positional sound that allows listeners to distinguish sounds as sources from above, behind, to the left, to the right, etc.

The algorithms employ transaural cross-cancellation technology, a scheme that allows the realistic sound to be produced by speakers as well as with headphones. Audio objects in RSX 3D can accept and process real-time data, and the software also can handle multichannel streams with multiple sample rates. In addition, the software has an interface that models room acoustics and simulates sound effects occurring in a confined space. Effects such as reverberation and doppler can readily be produced—the algorithms will automatically calculate the change in frequency of a soundwave resulting from the relative motion of the sound source and the listener.

When used with Internet applications, the RSX 3D

software is VRML 2.0-compliant. It supports Internet-based streaming, including multichannel streams with multiple sample rates. Java applets running under Microsoft's Internet Explorer or Netscape's Navigator 2.0 and higher also can benefit from RSX 3D. Moreover, the software can accept MIDI-based applications.

For a free copy of RSX 3D or the software development kit, surf into http://www.developer.intel.com/ial.rsx. Or call (503) 264-1946. DB

First Copper-Equivalent Wireless Local-Loop System On Trial

Century Telephone Enterprises Inc., Monroe, La., is conducting a trial in Marion, La., of the first copper-equivalent, wireless local-loop system available in the U.S. Through the trial, the company hopes to determine feature and service transparency of switch-based services. It also will help Century evaluate the operational requirements associated with the deployment of wireless telephony on a larger scale, as well as identify potential bandwidth and service limitations.

The system delivers all of the basic and enhanced voice and data services of today's wired telephone service network with none of the costs for maintenance of copper or fiber connections. Installation of the entire system into a neighborhood can be accomplished in a few days.

Says Nick Bowman, Century's vice president of operations and network design for its telephone group, "The system will provide state-of-the-art wireline-quality telephony services on a real-time basis without immediate, large capital expenditures in copper and fiber facilities."

For more information, visit the company's website at: http://www.centurytel.com. RE

Laser Emergency Kit Can Strap On Just Like A Backpack

The U.S. Air Force's Phillips Laboratory, located in New Mexico, has developed a laser medical pack that has the power to cut like a scalpel, coagulate bleeding, and close wounds. The pack is self-contained and fits into a space that's about the same as a backpack. The working tip of the instrument has the laser power delivered through a fiber-optic cable. The laser operates at 808 m with an output power of 8.5 W.

The fiber-optic system is pigtailed into the laser array. The complete system consists of a resonator exciting a small-diameter section of about 10 cm and a set of hot and cold exchangers to drive the magnet and piston at the tip. The intensity at the tip of the fiber can be as high as 1 kW/cm^2. A rechargeable lead battery powers the system with a duration for the 12-V, 4.5-A/hr system of about 20 minutes between recharges. The laser is fully protected from overheating by thermal sensors and cut-offs. Also, the battery recharger includes a key lock to prevent access in a safety mode.

More information can be obtained through the Office of Public Affairs, Phillips Laboratory, Kirtland Air Force Base, NM 87117; (505) 846-1911. PMcG

Chemistry Lab On A Chip Is The Goal of DARPA-Funded Project

A chemistry laboratory small enough to fit on a microchip—that's the project the U.S. Defense Advanced Research Projects Agency (DARPA) has commissioned to the University of Cincinnati, Ohio. The focus of the $2.8 million project is to develop handheld micro-electromechanical systems (MEMS) that can detect tiny quantities of a protein representative of a typical biological compound sampled or monitored by analytical chemists in medical, environmental, or industrial settings. It's expected that the design would be adaptable to a wide variety of chemical or biological applications.

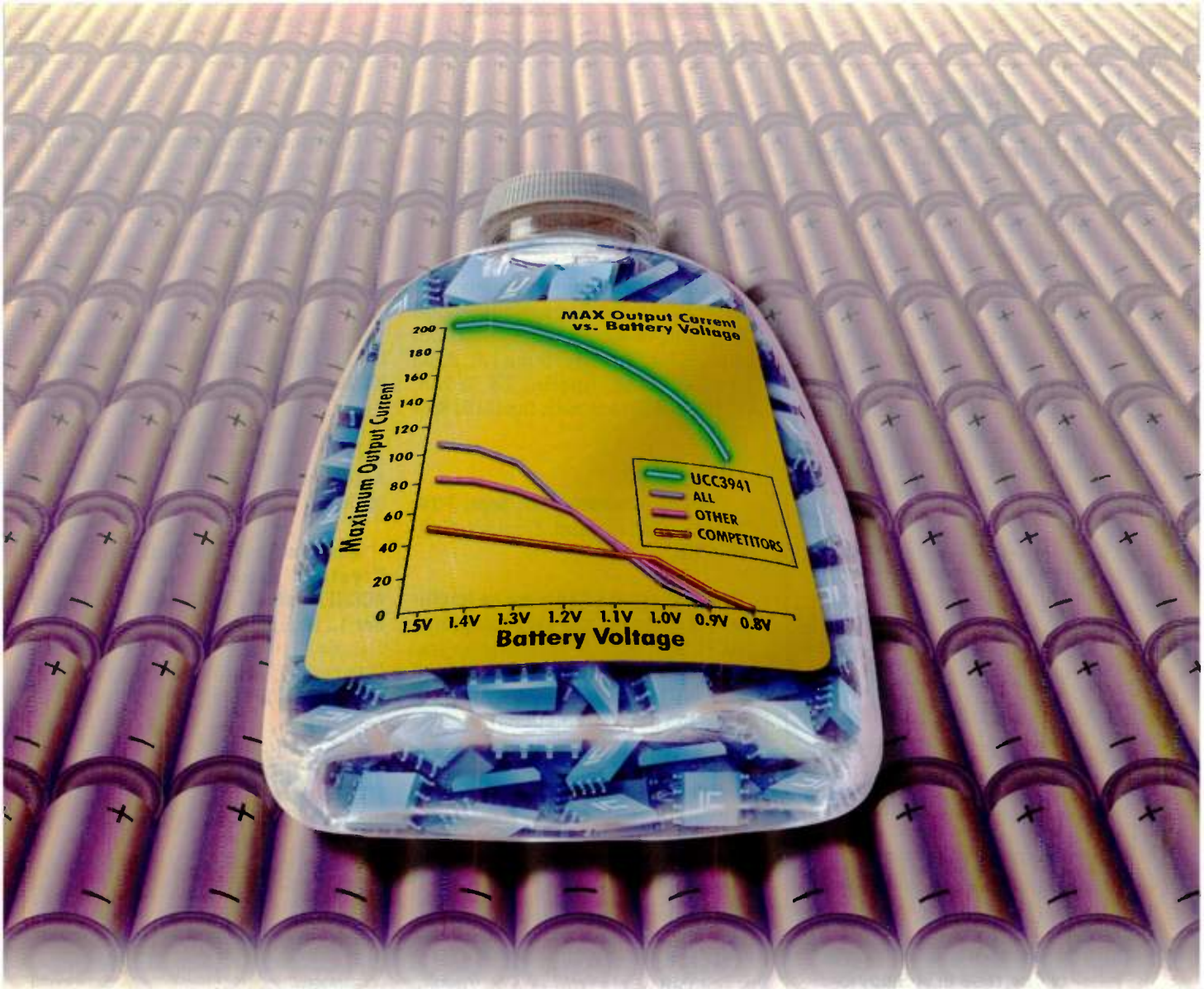
The collaboration takes on significance simply because it, in essence, takes the expertise of research chemists and puts it in a form that can be used by almost anyone. Other advantages of "chemists-on-a-chip" is the fact that less material means lower cost. It's possible that the cost of some highly technical analyses could be reduced from $10,000 to less than $50 because large, expensive laboratory equipment would become obsolete. Smaller systems also can run much faster. Professor Thurman Henderson, one head of the university's research team, estimates that a reaction which typically takes 30 minutes in a lab might take only a few seconds on the chemistry chip.

Analysis will be very similar to what happens in a full-scale chemical laboratory—only that it happens on a microscopic scale. According to Chong Ahn, the other head of the research team, "We're going to have microvalves, micropumps, reservoirs, and controllers. We already have so many MEMS components on campus. We're simply putting them together in a new way for different applications."

Apparently, DARPA's original interest in microanalysis was to develop a battlefield sensor that soldiers could wear to warn them in case of an attack with chemical or biological weapons. But many other applications are possible: they could detect environmental pollutants; monitor the health of a premature baby; help control the delivery of drugs; and increase the safety of chemotherapy. And, by using smart technology, it's believed that implanted micro-machines could be adapted to send signals remotely to physicians, alerting them to problems.

For further details, contact the University of Cincinnati at (513) 556-3001; fax (513) 556-2340. RE

Edited By Roger Engelke



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AUGUST

Memory Technology, Design, & Test Workshop, Aug. 11-12. San Jose, CA. Contact F. Lombardi; (409) 845-5464; e-mail: lombardi@cs.tamu.edu.

IEEE International Symposium on Electromagnetic Compatibility (EMC '97), Aug. 18-22. Contact John Osburn, EMC Test Systems LP., 2205 Kramer Lane, Austin, TX 78758; (512) 835-4684 ext. 669; fax (512) 835-4729.

SEPTEMBER

Telecom Interactive '97, Sept. 8-14. Geneva, Switzerland. Contact (703) 907-7736.

Fifth European Congress on Intelligent Techniques and Soft Computing (EUFIT '97), Sept. 8-12. Aachen, Germany. Contact Promenade 9, 52076 Aachen, Germany; (49) 2408 6969; fax (49) 2408 94582; e-mail: eufit@mit-gmbh.de; Internet: http://www.mit-gmbh.de/elite/elite/eufit.html.

ICSPAT/DSP WORLD 1997, Sept. 14-17. San Diego Convention Center, San Diego, CA. Contact Denise Chan, Miller Freeman Inc. (415) 278-5231; e-mail: dsp@exporeg.com.

MCM Test Workshop, Sept. 14-17. Napa Valley, CA. Contact Y. Zorian, (408) 453-0146 ext. 227; e-mail: zorian@lvision.com.

International Conference on Solid State Devices and Materials (SSDM), Sept. 16-19. Act City Hamamatsu, Hamamatsu, Japan. Contact Secretariat of SSDM '97, % Business Center for Academic Societies Japan, 5-16-9 Honkomagome, Bunkyo,Tokyo 113, Japan; (81) 3 5814 5800; fax (81) 3 5814 5823; e-mail: confg3@bcasj.or.jp.

Thermionic Workshop, Sept. 21-23. Cannes, France. Contact B. Courtois; (33) 35 76 7 46 15; e-mail: bernard.courtois@imag.fr.

AUTOTESTCON '97, Sept. 22-25. Disneyland Hotel, Anaheim, CA. Contact Robert C. Rassa, Hughes Aircraft, P.O. Box 92426, MS R07/P553, Los Angeles, CA 90009-2426; (310) 334-4922; fax (310) 334-2578; e-mail: rcrassa@ccgate.hac.com.

Electrical Overstress/Electrostatic Discharge Symposium, Sept. 23-25. Santa Clara Convention Center, Santa Clara, California. Contact ESD Association, 7902 Turin Road, Suite 4, Rome, New York 13440-2069; (315) 339-6937; fax (315) 339-6793.

Fifth China International Electronics Exhibition (CIEE '97), September 24-28. China International Exhibition Centre, Beijing. Contact Gu Jinjing, CEIEC, Post Office Box 140, Beijing, 100036 China; (011) 8610 6822 3909; fax (011) 8610 6821 3348

Eastern Regional Conference on Crystal Growth & Epitaxy, ACCGE/east-97, September 28-October 1. Bally's Park Place Hotel & Casino, Atlantic City, New Jersey. Contact Louis G. Casagrande, (516) 346-6379; fax (516) 346-3670; e-mail: Lou_Casagrande @atdc.grumman.com, or Ed Porbansky, Conference Secretariat, 163 Carson Drive, Colonia, New Jersey 07067; (908) 382-1806.

Embedded Systems Conference, September 29-October 3. San Jose Convention Center, San Jose, California. Contact Miller Freeman Inc. (415) 278-5231; e-mail: esc@exporeg.com.

OCTOBER

OEMed Northeast, October 1-2. Bayside Expo Center, Boston, Massachusetts. Contact Exposition Excellence Corp., 112 Main Street, Norwalk, Connecticut 06851; (203) 847-9599; fax (203) 854-9438.

OEM Electronics Northeast, October 1-2. Bayside Expo Center, Boston, Massachusetts.Contact Exposition Excellence Corp., 112 Main Street, Norwalk, Connecticut 06851; (203) 847-9599; fax (203) 854-9438.

IEEE Ultrasonics Symposium, Oct. 7-10. Marriott Hotel, Toronto, Canada. Contact Stuart Foster, Dept. of Medical Biophysics, Room S-658, Sunnybrook Health Science Ctr., 2075 Bayview Ave., Toronto, Ontario, M4N 3M5, Canada; e-mail: stuart@owl.sunnybrook.utoronto.ca

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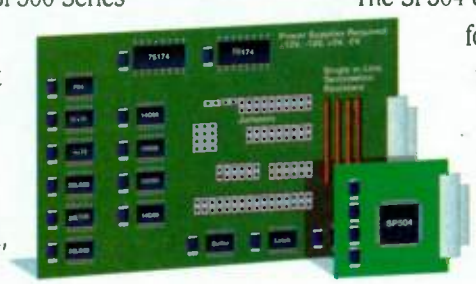
READER SERVICE 198

The Future of Network Communication in a Single Chip.

The SP504 is the newest release in the SP500 Series family of programmable serial interface transceivers from Sipex. Built on market experience, the SP504 includes such features as single resistor V.35 termination, programmable charge pump, and two new modes of operation, V.36 and EIA-530A.



The SP504 offers an efficient single chip solution for serial ports that require supporting multiple physical interface standards. Serial port designs for Frame Relay, X.25, and networking routers can be simplified by the SP504. The SP504 can be used in either DTE or DCE systems.

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READER SERVICE 174

Development Of Digital MEMS-Based Display Technology Promises Improved Resolution, Contrast, And Speed

With LCDs trying to overtake CRTs in the desktop market, it's easy to forget that there are other display technology options. In fact, a great deal of research continues to focus on the development of new display technologies. The bottom line is that no single technology is a perfect fit for all applications, especially in light of the increased demand for sophisticated and complex display content. The incremental progress made in the traditional CRT and LCD markets has failed to keep pace with industry's needs.

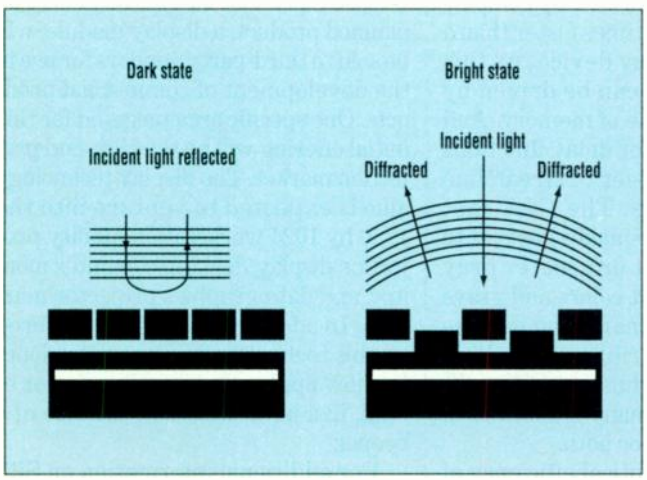
Recently, a company that had long researched and developed a new display technology came to light. Having closely guarded its technology until it was ready for scrutiny from the global display community, Silicon Light Machines (formerly known as Echelle), Sunnyvale, Calif., unveiled the magic behind the mirrors. Until now, all that had been known about its core display technology, Grating Light Valve (GLV), was that it promised to deliver brighter, higher-resolution, higher-contrast images for applications ranging from convention-hall projection systems to handheld information tools.

Focusing on the development of a cost-effective, silicon-based reflective-light technology, the company was able to deliver on these promises, and much more. It came up with a digital technology that can be used to fabricate displays with microelectromechanical techniques (MEMs) and simple optical principles. Because it can be manufactured using existing semiconductor production facilities and standard VLSI production equipment, GLV can be made for a very low cost. The technology features high brightness and resolution (1.3 Mpixel in a 1.3-in. diagonal), a high contrast ratio of greater than 200:1, and a switching speed of 20 ns, roughly six orders of magnitude faster than an LCD. A wide dynamic range ensures that both the computer and video images are of very high quality. And since it's based on the reflected-light principle, the images stand out under normal room lighting. The technology delivers high color accuracy with a digital gray scale, consumes very little power, and has a zero-power pixel-state retention.

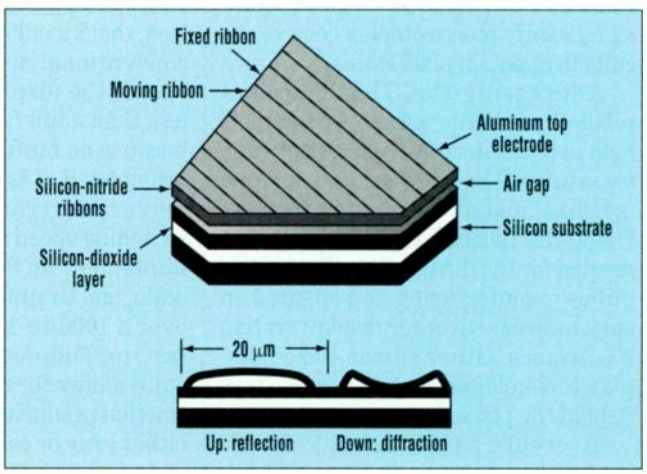
The GLV can be scaled either up or down and features a very reliable architecture. In fact, recent tests on the GLV display-device ribbons show that they can run without fatigue for 210 billion switching cycles. That's the equivalent of a television set running nonstop for 15 years without a single failure. And, because the ribbons are constructed of silicon nitride, a ceramic material, they are extremely rugged compared to other analog parts.

A GLV device is a micromechanical phase grating in which the controlled diffraction of incident light enables the production of either bright or dark pixels in a display system *(Fig. 1)*. Key to the GLV technology, developed by professor David Bloom and his students from Stanford University, Menlo Park, Calif., are parallel rows of reflective ribbon structures formed on the surface of a silicon wafer. According to Rob Corrigan, vice president of marketing at Silicon Light Machines, "Silicon was chosen for the convenience of fabrication, but, in fact, you don't even need to use transistor-grade silicon, it just needs to be flat. This means that the device can be very cheap."

In the pixels' dark state, all the ribbons are in the same plane, so as incident light hits their surfaces it is simply reflected off. By blocking the light that returns along the same path as the incident light, a dark spot in the viewing system is produced. But, in the bright state, the situation is a bit different. Rows of the moveable ribbon are alternately pulled down



1. The Grating Light Valve has two states: dark and bright. In the dark state, the ribbons are coplanar, and incident light is reflected off the device. In the bright state, every other pixel is addressed, effectively creating a diffraction system in which light goes in and out of each pixel separated by exactly one phase. In this instance, all normally reflected light is diffracted. The first order light gets back roughly 81% of light.



2. The ribbons-up position is maintained by the tensile stress of the silicon-nitride material. The ribbons will then naturally snap back into an upward position if no other force is applied. In order to have control over this behavior, electrodes are integrated below the ribbons. As different voltages are applied to the ribbons and the bottom electrodes, an electrostatic attraction pulls the movable ribbons downward.

roughly one-quarter wavelength. In this manner the device functions as a capacitor or spring. Consequently, when incident light hits the surface, it is diffracted away from the surface of the ribbons. Because the angle of the diffracted light is different then that of the incident light, a bright spot in the viewing system occurs. Accordingly, the device is either on or off.

Controlling the movement of the ribbons is a straightforward process. The ribbons naturally assume the up, or the dark, state, so the only real issue is how to get them to pull down. Placing electrodes beneath them and applying a voltage difference to each pixel (made up of six ribbons) independently accomplishes the task*(Fig. 2)*. This electrical signal provides the electrostatic force needed to pull the ribbons down. In reality, the ribbons are not actually "pulled" down, but "snapped" between off and on states in response to an electrical signal.

Even as the voltage differential is reduced, the ribbons maintain their down state. Therefore, a high voltage does not have to be consistently applied to keep the ribbons in the down state during a display devices operation. This ribbon hysteresis allows the bright state pixel states, e.g. the ribbons down, to be maintained with a bias voltage, without drawing current. In other words, a static pixel configuration can be maintained with practically zero power consumption. By comparison, other display technologies require significantly more complex control circuits to maintain pixel states.

Addressing the GLV is accomplished while the array of ribbons is held in place at a bias voltage between two states. The addressing technique is a pixel matrix addressing scheme. Using this method, transistors are not needed for the device. This design simplifies manufacturing and ensures an easy interface to other display system electronics. Other silicon-based display technologies require transistors to hold the pixels in a certain state.

To create a GLV display device package, a clear piece of glass is adhered to the chip, just above the layer of ribbons. Then the entire package is hermetically sealed in a one-atmosphere dry-nitrogen environment for pressure equalization and oxidation prevention. With this packaging technique, the chip can be sawed normally. Any additional components such as an electronic driver or control logic can be built into a complete, lightvalve, multichip module.

The entire process to build a GLV array requires a mere seven mask steps. The more masks required, the higher the initial cost and the greater the negative impact on manufacturing yields. Two of the steps are specifically used to define the basic GLV pixel. The most critical mask step involves setting the gap between the fixed ribbon and the moving ribbon. This step is very critical since the smaller the gap, the higher the light efficiency.

To produce an image using a GLV, a standard light source is used to reflect light off tiny mirrors embedded in the surface of the chip onto the screen. This technique produces an image of monochrome bright or dark pixels. The back of each mirrored surface is treated with a diffraction grating for color displays. Distinct contrast is the result of each mirror (or micromachine) being physically raised or lowered to be turned on or off sharply. A greater resolution may be achieved by simply manufacturing a larger chip. There are several techniques used to produce color images, including color filters with multiple light valves, field-sequential color, and subpixel color using tuned diffraction gratings.

One of the unique features of the GLV technology is its ability to switch very quickly, in just 20 ns. By comparison, that's a million times faster than a conventional display device. At this speed, the display can be driven by less than a full frame of memory. And because no buffers or delay functions are needed, it is easier to streamline driver electronics. The GLV fast switching speed also makes it easier to implement an 8-bit or greater gray scale, and to support colors and grays over a 1000-to-1 dynamic range. The fast, up-and-down ribbon-switching state allows for modulation of the diffraction producing many gradations of either gray or color or both.

In general, the optical efficiency of reflective devices is much higher than that of transmissive devices. Since GLV is a reflective technology, it has a higher overall efficiency for projection (2 lm/W minimum, 10 lm/W maximum) than the more conventional LCD. This high efficiency contributes to the ability of GLV systems to deliver higher levels of brightness per watt of power consumed.

Compared to other display technologies such as CRTs and LCDs, and GLV-based display devices offer a number of advantages. CRTs, for example, are analog devices and tend to be big and heavy. The LCD also is an analog device, dependent on the temperature of its environment. By comparison, GLV is digital in nature, and has the same performance regardless of temperature. In addition, neither CRT nor LCDs are particularly well suited for resolving very fine, detailed images—a challenge easily met by any GLV-based display.

Other technologies currently in development, such as plasma and field-emission displays (FEDs), are hampered by their need for manufacturing infrastructure and tooling for fabrication. Since GLV-based devices use existing tooling and manufacturing infrastructures, this issue is not a concern.

GLV technology represents a shift in the trend toward larger displays in that it enables a single, very small, very high-density display to be adapted easily for very large projection images, as well as very small direct-view images. This versatility is possible because GLV technology breaks with the traditional dependence of image size on display size.

Presently, the company has plans to release a product late in the year. The planned product, a display module, will be sold to third-party vendors for use in the development of commercial products. One specific area targeted for this initial offering will be the high-end projection market. The display technology also is expected to venture into the 1280 by 1024 workstation quality projection display, desktop computer monitor, and data/graphics projector markets. In addition, the benefits offered by this technology will open the doors for new applications such as fax or e-mail, in a hand-held box the size of a beeper.

For additional information on Silicon Light Machines and its GLV technology contact them at 385 Moffett Park Dr., Suite 115, Sunnyvale, CA 94089; (408) 541-1990; or by Internet: http://www.siliconlight.com.

Cheryl Ajluni

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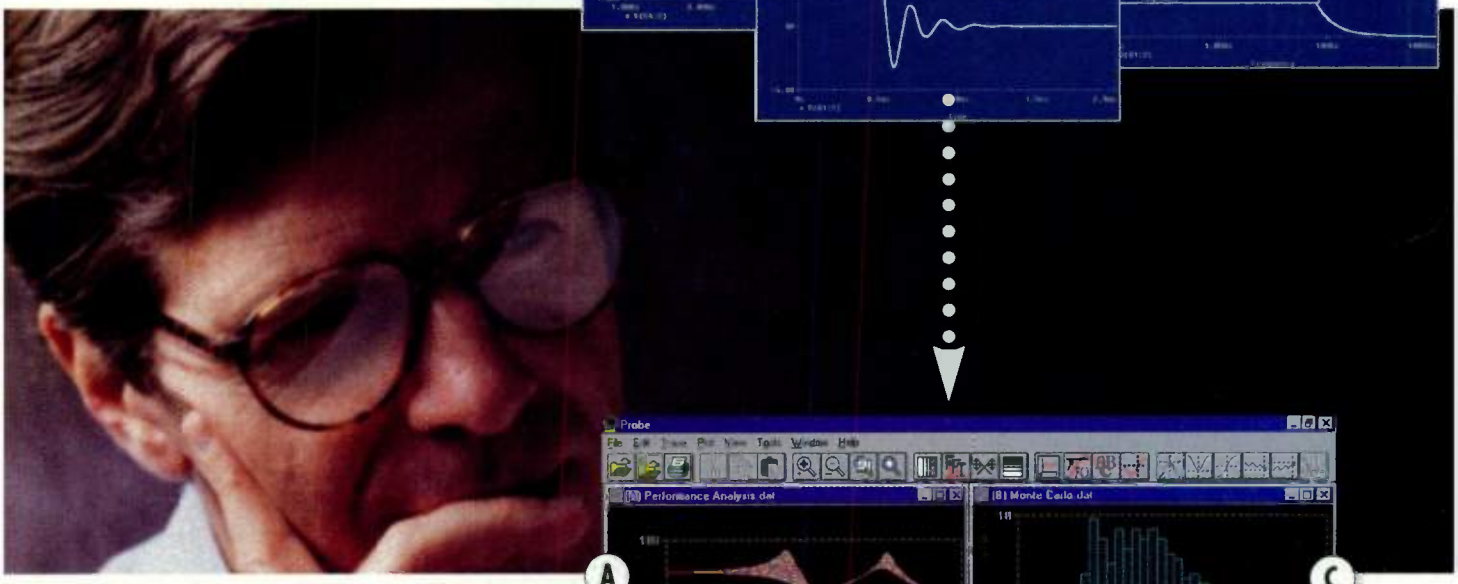

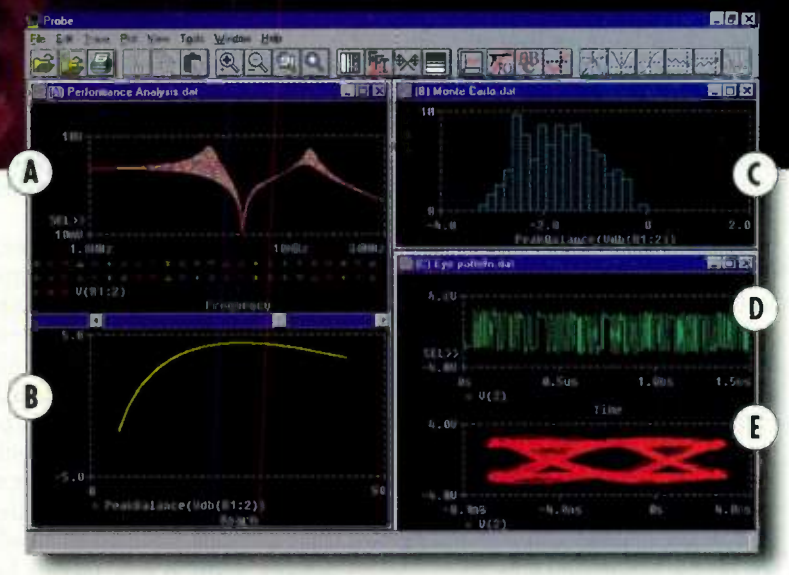

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READER SERVICE 300

Self-Focusing Infrared Telescopic Glasses May Restore Sight To Millions

Her new glasses are no miracle, but don't try telling that to Jenna Meck, a visually-impaired junior at Merideth College in Raleigh, N.C. She says that her battery-powered, computer-controlled, self-focusing telescopic glasses are the next best thing. "These are tremendously helpful," Jenna said. "I am excited because they are changing my life already, and I just got them."

For the first time, she can see well enough to read a blackboard at school. In the past, that was frustrating because her poor eyesight forced her to hold a bulky telescope to her face and put it down each time she took notes. For the first time, she can see her mother and father from farther away than a few inches. With the new glasses, she's also able to recognize teachers and friends.

Weighing less than three ounces, the VES-EF auto-focus telescope attaches to an ordinary pair of glasses (with modified lenses) to provide enhanced eyesight for many visually-impaired people. The compact system contains a set of high-performance optics, an infrared ranging system, and a stepper motor-driven, auto-focus mechanism.

Born with a detached retina in her left eye and a coloboma—the visual equivalent of a cleft palate—in her right, the young woman has always been nearly blind. Using magnifying glasses and a telescope, she could see well enough with her right eye to keep up with school, but not well enough to see people's faces and objects.

Now, thanks to the efforts of a team of doctors and technologists from North Carolina, soon it may be possible for millions of visually-impaired people like Jenna to enjoy dramatically higher levels of productivity and independence. Originally developed by Dr. J. "Russ" Pekar of Chapel Hill, they were refined and engineered for mass production in collaboration with Dr. Henry Greene, clinical associate professor of opthamology at the University of North Carolina at Chapel Hill School of Medicine. Also working closely on the nearly seven-year project was engineer Robert Beadles of Durham. Together, they have produced what is thought to be the first self-focusing telescopic glasses.

The glasses resemble a small camera perched atop a pair of ordinary spectacles *(see the picture)*. The Ocutech VES auto-focus telescope weighs in at only 2.5 oz., despite the fact that it is tightly packed with electronics, optics, and mechanical components. Its auto-focus system employs two microcontrollers and takes its cues from an infrared range-finder using a low-power beam to gauge the distance from the wearer to an object.

Until now, the many visually-impaired people who could benefit from magnified images used handheld telescopes or head-mounted units, both of which required manual focusing. Television-based magnification systems also are available, although the head-worn units are still fairly bulky, power-hungry, and expensive.

Of the present options, the head-mounted magnifying telescopes seem to be the most convenient for the majority of users. Weighing 2 to 4 oz., these compact optical systems give magnifications of 3 to 6 power, enough to boost a legally-blind person's visual acuity (20-200) to the equivalent of 20-50. Nevertheless, the telescopes are far from ideal because they still require manual re-focusing each time they are used at a different distance. An automatic-focusing system is a big advantage because it allows a user to let his or her gaze shift naturally from object to object, without the hassle of refocusing.

While prototypes have existed in various forms for several years, Green and his team faced several challenges in making the device practical for general use. The telescope had to be fully automatic, require little or no operator training, and run for extended periods (up to 12 hours) on a small battery. The complex electronics and mechanics had to be miniaturized sufficiently to permit a unit to be worn comfortably on a pair of conventional frames. Perhaps the biggest challenge was to design the telescope so that it could be manufactured at a cost that was affordable by the average person.

To avoid reinventing the wheel, the project was based around an existing head-mounted telescope, known as the VES, or vision-enhancing system. It is manufactured by Ocutech, Inc., Chapel Hill, N.C. The VES is available in 3X, 4X, and 6X versions, and has been used successfully used by thousands of people worldwide. Its compact, horizontal optical path gives it a low profile, making it an ideal candidate for an automated-focus system. In order to reduce the power and time required to focus, Dr. Pekar, president of Ocutech (and inventor of the original VES), developed a low-friction lens-focusing actuator that formed the basis of the automatic system. Elan ETS, another North Carolina-based research company was recruited to develop the electro-optics associated with range-finding. The electro-mechanical aspects of the design were shared between the two organizations.

While it borrows some of the basic technology and concepts from infrared auto-focus systems used in point-and-shoot film cameras, many of the VES's

system parameters differ sharply from photographic applications. For instance, a camera must get a focus lock only once per frame, while a vision-enhancement system must continuously, quickly refocus itself to provide smooth, seamless operation. Preliminary studies indicated that for the telescope to be transparent to the user, it would have to measure range twice a second and perform a full-range refocus in 200 ms or less. This rapid, continuous operation put power at a premium, driving the project's engineers to employ aggressive power conservation techniques.

Other significant differences are found in the focus range and granularity requirements. Cameras typically use between 3 and 16 preset focus zones to cover a distance range between 3 ft. and infinity. Research revealed that the glasses require a focus range covering 1 ft. to infinity in a minimum of about 30 steps.

Balancing these stringent performance requirements against tight cost and power constraints resulted in a "bicameral" architecture, where tasks within the unit are divided between a pair of microcontrollers. A Microchip PIC 16C71 is responsible for running the focusing mechanism and performing housekeeping tasks. It also contains the operational software and special functions used during calibration and burn-in. The PIC drives the telescope's focusing assembly using the world's smallest, commercially available, stepper motor, weighing just 0.17 oz.

To prevent the focus mechanism's stepper motor from losing a step due to under voltage, the supply voltage is measured after it performs each refocus. If it falls below a preset safety level, the controller will go into sleep mode and will not attempt to drive the motor. This design prevents the mechanism from losing its factory calibration settings, which rely on keeping precise track of the stepper motor's position.

Focus determination is handled by a Hamamatsu H2476, an ultra-low-power, 3-V controller that was originally used in auto-focus film cameras. To circumvent errors caused by the noisy infrared environment, the controller takes 16 distance measurements and averages them. Twice a second, it produces an averaged distance measurement which is compared to the current focus setting to determine if a refocus is needed.

The H2476 was originally designed to provide only 16 focus zones, but the engineering team was able to coax 29 steps of resolution out of it by developing an individualized calibration process which is performed on each unit before it is shipped. The telescope is placed on a 12-ft. calibration table and connected to a PC that controls it during the test. The PC's calibration software steps the telescope through a battery of tests against known distances and determines the focus values that are unique to that particular unit. These values are then programmed into the controller's on-chip PROM.

By using highly-efficient drive circuitry and turning off portions of the unit during periods of inactivity, the telescope can squeeze up to 12 hours of operation out of its 4-oz. external NiCd rechargeable battery pack. Another trick the designers employed was to minimize the power losses inherent in voltage regulators. Nearly all the unit's circuitry runs directly off the unregulated voltage directly available from the NiCd battery pack. Only the range-measuring IC and a voltage reference source require regulated power. The unit's low power consumption also allows the use of a smaller, head-mounted, 1-oz. battery pack to be used when a one-piece configuration is desired.

All the hard work at miniaturization and optimization of the design to lower production costs seems to have paid off. While not all visual impairments can be improved with simple magnification, there are several million people in the U.S. alone that could benefit from the glasses. Now in pilot production, a monocular version of the telescope system is available for $3000. An improved binocular version also is under development.

Among the first recipients of the new glasses is Tom Vernasco, of Cary, N.C. Born severely near-sighted, he works as a reservations agent for Holiday Inn and relied on a special terminal and large-print software to perform his work until now. After purchasing the telescope just before late December, 1996, he discovered that they changed his life. "I no longer have to use the special large-print programs at work," Vernasco said. "At home, I can go shopping by myself now if I want to. And I can almost see well enough to drive."

For further information about the electronic technology behind the glasses, contact Elan Enabling Technology Systems, P.O. Box 14228, Research Triangle Park, NC 22709; (919) 383-8794; fax (919) 383-4818; Internet: *http:// www.eurekalert.org*. Information about the optical system or about purchasing the Ocutech VES can be obtained from the manufacturer, Ocutech Inc., P.O. Box 625, Chapel Hill, NC 27515; (919) 967-6460; fax (919) 968-4601.

Lee Goldberg

Advanced GaAs Process Integrates RF Front-End Functions

Pushing process technology even further, designers at TriQuint Semiconductor, Hillsboro, Ore., have devised the latest generation GaAs process for highly integrated RF front ends. As the name suggests, the TQTRx process offers a solution to both the transmit and receive side of the RF front end. The requirements for such an integrated device include the ability to produce power with high linearity and good efficiency, as well as small-signal capability and sensitivity and low noise. The process also needs to have the maximum values of on-chip capacitors and inductors possible with, of course, high-transition frequencies.

The advanced 0.6-µm process allows the production of enhancement-, depletion-, and power-depletion-mode MESFETs. It features three global metal-interconnect areas. The layers are incorporated in a high-performance interlayer dielectric that provides a high degree of wiring flexibility. This flexibility, in turn, permits the

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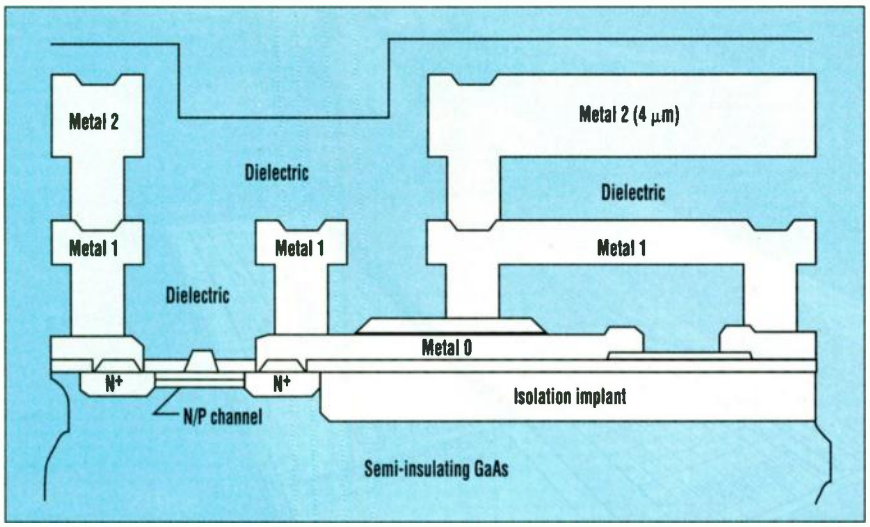


TriQuint Semiconductor's TQTRx process in GaAs offers performance specifications that make it suitable for fabricating both transmit and receive RF functions. Power depletion- and enhancement-mode MESFETs, as well as passive components, can be fabricated on the process.

wire layout to be optimized for the simplest plastic packaging, nichrome (NiCr) resistors, metal-insulator-metal (MIM) capacitors, and high-Q spiral inductors.

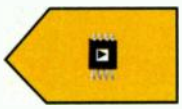
Although TriQuint Semiconductor will be designing standard parts with the process, the first uses will be for foundry applications. Characterization of the process is showing an f_T of 20 GHz, while f_{max} is greater than 70 GHz, allowing for designs up to the Ku band (12.5-18 GHz). The noise figure is under 1 dB, while the avalanche breakdown is greater than 15 V. Inductor Q factors are more than 17 at 1.9 GHz, while the capacitors that can be fabricated will be about 1200 pF/mm^2. The output-power capability will be more than 300 mW/mm^2. Typically, the number of mask layers needed for the fabrication of ICs will be only 16.

TriQuint Semiconductor's vision of the integrated RF world is for a product such as a cellular telephone to be fabricated in three blocks. The digital processing and control would be made in CMOS technology, the analog baseband and IF would be made in bipolar technology, and the RF front end would be done on the TQTRx GaAs process.

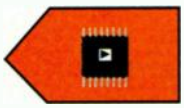
For more information, contact Rob Christ, foundry marketing manager, TriQuint Semiconductor, 2300 NE Brookwood Pkwy., Hillsboro, OR 97124; (503) 615-9000, fax (503) 615-8900; or at their World Wide Web site: http://www.triquint.com.

Paul McGoldrick

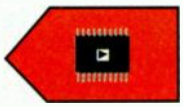
Introducing A New Family Of 8-Bit And 10-Bit ADCs: Micro Packages At Micro Prices.



AD7810
8-Pin Micro SOIC



AD7811
16-Pin TSSOP



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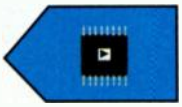
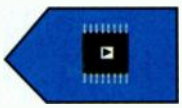


AD7813
16-Pin TSSOP



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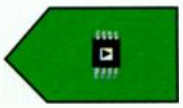
16-Pin TSSOP



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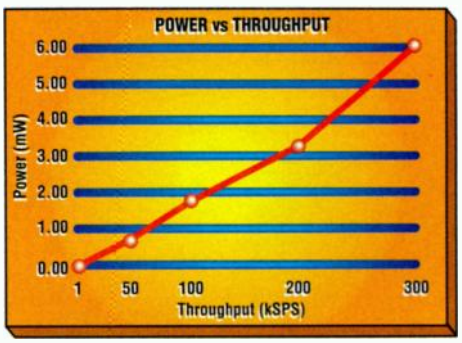
	AD7810	AD7811	AD7812	AD7813	AD7819	AD7823
Resolution	10	10	10	10	8	8
# Of Channels	1	4	8	1	1	1
Interface	Serial	Serial	Serial	Parallel	Parallel	Serial
Throughput (kSPS)	350	350	350	350	135	135
Temp. Range (°C)	-40/105	-40/105	-40/105	-40/105	-40/125	-40/125
Price*	$2.45	$2.90	$3.30	$2.55	$1.95	$1.95
Faxcode	2061	2062	2062	2063	2064	2065

Power Consumption

Each part in the family operates from 2.7 to 5.5 V, consumes only 1.5 mW @ 100 kSPS over a wide temperature range of -40°C to 125°C and comes with optional automatic power-down. The ability to read the conversion result during power-down also minimizes the time the part is operating at full power. These features make this family of parts ideal for battery-operated devices. The analog input range extends from 0 V to the reference voltage, which has a range of 0 V to V_{DD}.



The AD7810 at 3 V.

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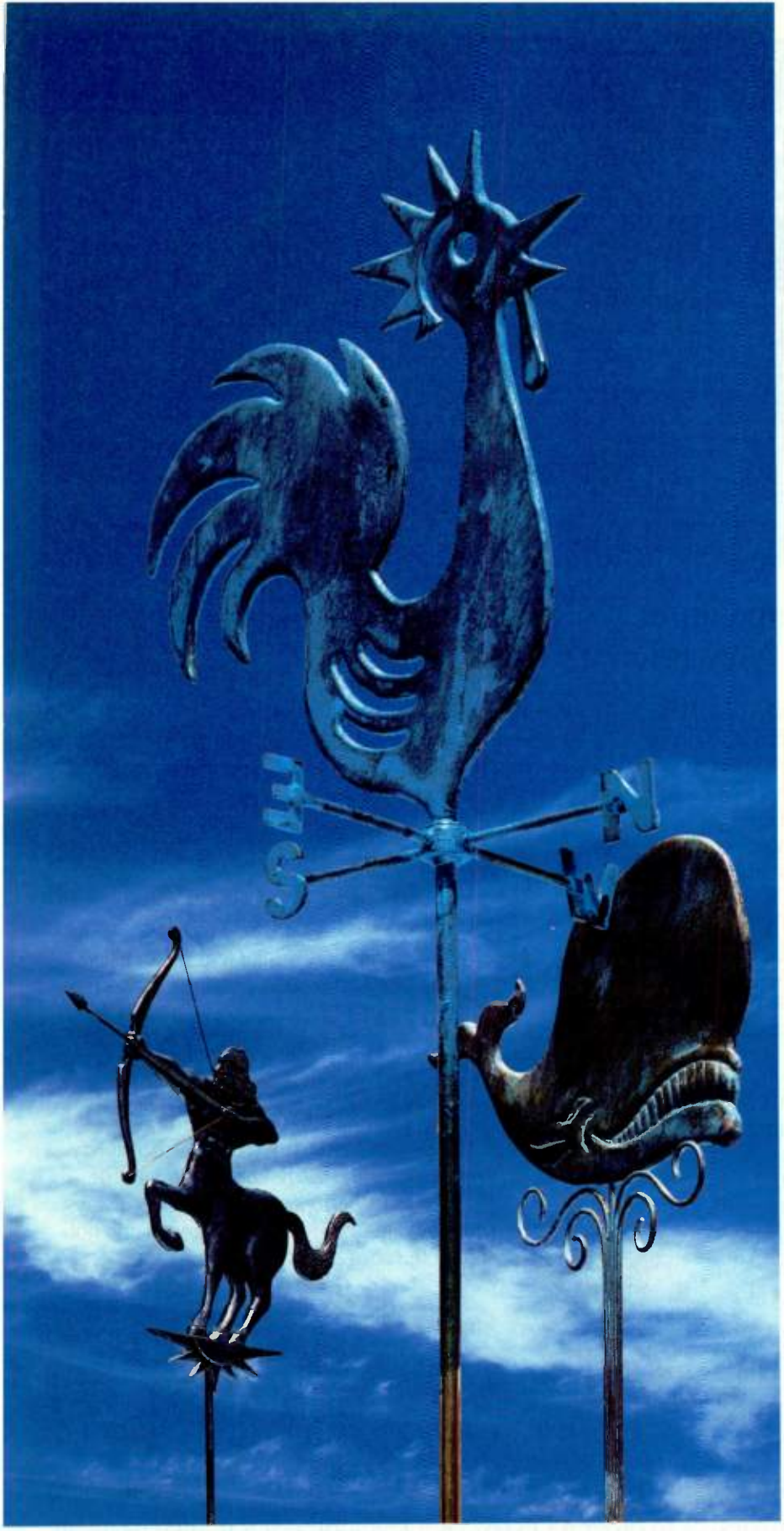

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Dense MOSFET Enables Portable Power Control

With A 32 Million Cells/In.^{2} Density And New, Space Saving Packaging, A Power MOSFET Family Finds Numerous Switching And Control Applications In Portable Equipment.

Frank Goodenough

COVER FEATURE

Power-supply voltages for all kinds of equipment are heading lower, but at the same time, marketers and customers are demanding that designers pack more computing capability into their systems. However, they're also demanding that system size and power usage either remain the same or drop significantly.

With those requirements in mind, Temic Semiconductors (formerly Siliconix) increased the cell density of their low-voltage power MOSFETs to 32,000,000 cells/in^2 *(Fig. 1)*. That's up fourfold from 8,000,000 cells/in^2, the company's advanced processing technology of less than three years ago (ELECTRONIC DESIGN, *May 2, 1994, p.89)*

The increased cell density brought about by this advance in so-called TrenchFET power MOSFET semiconductor technology has made possible the development of two families of low-voltage power MOSFETs with unique performance features that will be useful in today's applications.

For starters, one family represents the first announcement of so called "Low-Threshold" powerFETs. These powerFETs have been optimized and are specified for operation with a mere 2.5 V between gate and source. That is, they turn on "hard" with a gate-to-source voltage (V_{GS}) about half that of a family of so-called "logic-level" MOSFETs that are specified to turn on at a V_{GS} of 4.5 V. And,the Low-Threshold devices turn on at a much lower V_{GS} compared with typical standard powerFETs that need at least 10 V between the gate and source to turn on *(see the table)*.

Truly low-voltage devices, their maximum drain-to-source voltage (V_{DS}) is rated at just 20 V, while maximum V_{GS} is specified as 12 V (Temic calls this Low-Threshold technology "Generation V TrenchFET"). On-resistance for the Low-Threshold FETs is not even specified at a V_{GS} of 10 V because it is too close to the 12-V maximum. Instead, it will be specified at a much lower 8 V *(see the table, again)*. Temic's second family of 1997 MOSFETs reduced the on-resistance of earlier, 1993/94, n-channel and p-channel FETs by about 35%, compared with similarly rated devices (maximum V_{DS} = 30, maximum V_{GS} = 20).

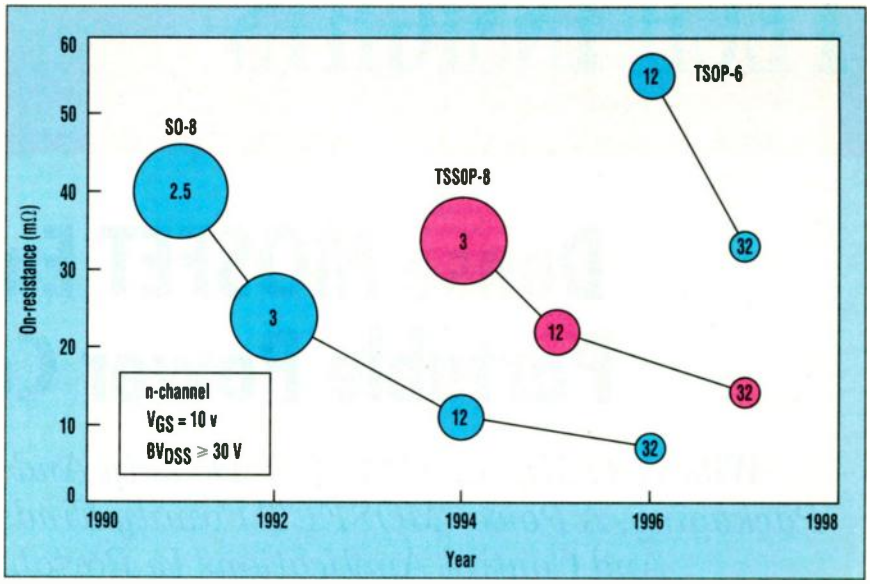
In addition, working closely with Motorola, Temic designers have optomized the thermal properties of the TSOP-6, a tiny surface-mount power package, for these new TrenchFETs.

To put this performance upgrade in perspective (Temic calls it "Generation IV TrenchFET technology"), compare the on-resistance of typical n- and p-channel SO-8 packaged die in 1997 TrenchFET technology with similar devices from TrenchFET technology of four years ago. Maximum on-resistances of the earlier FETs such as the n-channel Si4410 and the p-channel Si4425 are shown in the first line of data of the table. Their typical on-resistances with V_{GS} = 4.5 run at 20 mΩ and 35 mΩ, respectively. The typical on-resistance of similarly driven equivalent FETs in the en-

hanced 1997 technology comes in at just 13 mΩ and 23 mΩ, respectively.

A rule that's been adhered to by most application engineers is not to design to a manufacturer's typical specifications. But according to Richard Williams, director of Device Concept and Development at Temic, if a statistical analysis of their TrenchFET's typical specifications shifts, the process is adjusted to bring the specifications back to where they belong. Designing a battery-powered system's dc-dc converters to these new MOSFET typicals can significantly increase battery life. So it may be time to look a little closer at some typical specifications. At a minimum, it may be wise to consult an application engineer at your semiconductor supplier for more information.

These two families of low-voltage power MOSFETs, both based on Temic's 32,000,000 cells/in.^{2} TrenchFET technology, offer a significant drop in specific on-resistance. Specific on-resistance is a long-used figure-of-merit (FOM) for power semiconductor devices—it equals device-on-resistance times device-die-area.

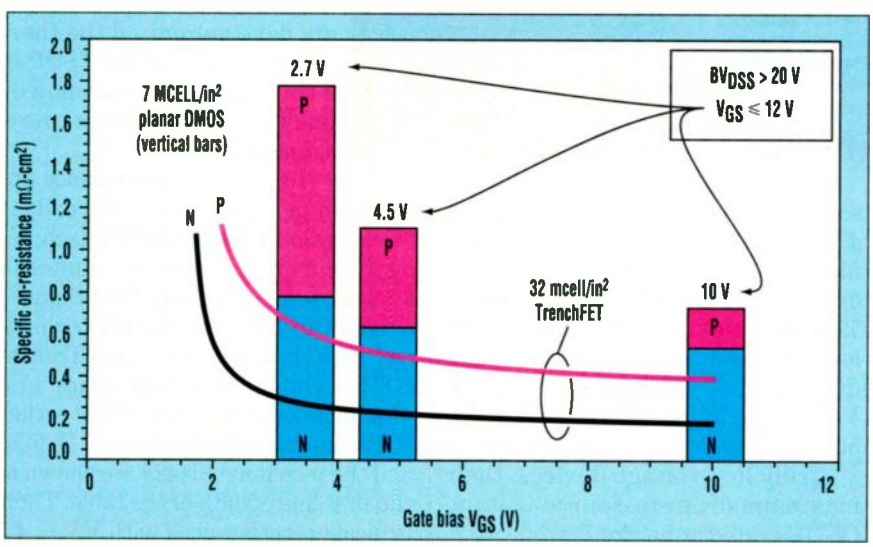


2. Since 1990, the on-resistance of low-voltage power MOSFETSs has dropped while die area of, the devices has also dropped (relative area of circles), permitting the use of smaller packages. Increasing cell density (number in circles in millions of cells/square inch) and moving to TrenchFET technology has made it possible.

Packaging With A Twist

As power MOSFET die size drops and the systems in which they are used shrink, the need for a smaller surface-mount power package became clear to device designers and marketers. The trick was to reduce the package size below that of the TSSOP-8, yet still find a way to dissipate the heat. That's when Temic and Motorola jointly came up with the innovative TSOP-6 to fit the smaller power supplies of today's equipment.

In addition, all the 1997 TrenchFETs will be available in the traditional SO-8 and the TSSOP-8 package *(Fig. 2)*. The number in the circle beneath each package type is the cell density in millions of cells per square inch of the die while the area of the circles is a function of the technology's cell area.



1. By increasing TrenchFET cell density to 32 million per square inch (N and P curves), both n- and p-channel power MOSFETs can be fully-enhanced (turned on hard) with a relatively low voltage--less than 2.7 V between gate and source.

With the TSOP-6, Temic designers optimized the thermal properties of the tiny surface-mount power package for these new TrenchFETs *(Fig. 3)*. As they had done earlier with the SO-8 and TSSOP-8, designers optimized the thermal conduction of the leadframes to maximize the power dissipation and get the heat out. The heat flows from the die, through the die attach, into the copper leadframe and out the four drain leads. The small cross-section of the leads account for most of the package's thermal impedance. However, because the package is small, the leads are short. By using all four leads and keeping them short, the package's thermal impedance is low.

The TSOP-6 footprint is significantly smaller than that of both the TSSOP-8 and SO-8, and its height less than that of the SO-8. Each TSOP-6 packaged FET is available with a copper leadframe (V series) or with a leadframe of Alloy 42 (X series). The former dissipates 2 W and can handle up to 4 A. The latter dissipates 0.5 W and current handling is 1 A. While both series have identical electrical resistances, the thermal resistance of the X series is higher. Therefore, X-series FETs can't handle as much current and are thus lower in cost than the V series.

One of the significant achievements of of the technology from a packaging

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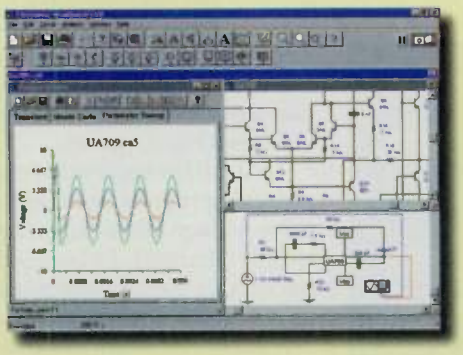

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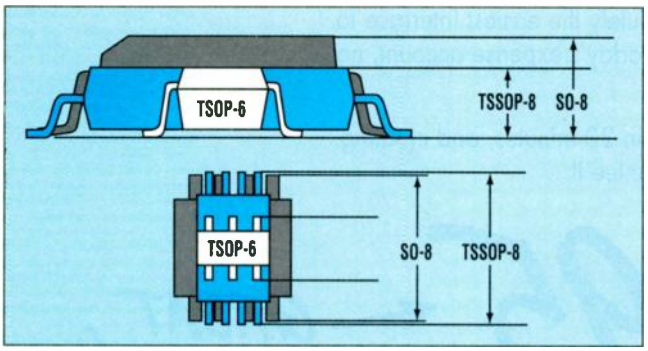
standpoint is that today's lowest available on-resistance in the TSOP-6 rivals that of the first powerFETs in an SO-8 despite a 200% cut in footprint-area *(Fig. 2, again)*.



3. The 32 million cells per square inch powerFETs come in both of Temic's tiny surface-mount power packages the SO-8 and the TSSOP-8 and in the new even smaller-footprint TSOP-6.

A FET For All Seasons

While capable of handling virtually any low-voltage power MOSFET application the new powerFETs are aimed at performing all three basic tasks of a power transistor *(Fig. 4)*:

- High and low-side load switching.
- Buck and Boost switching regulators including synchronous switchers.
- BDS (battery disconnect switches) safety switches for Li-Ion batteries. These devices remove the load if the battery voltage exceeds a high (charging) or low (discharging) limit. The BDS function also is required when a system provides more than one battery.

New designs with higher performance (higher efficiency switching regulators or series switches with lower voltage drops) are possible by simply replacing current generation FETs with the new devices using the the same-sized die and package. For example, one of the new FETs in an SO-8 can provide the currents demanded by a Pentium Pro microprocessor. It is no longer necessary to use two FETs in parallel.

In addition to lower on-resistances and lower-voltage gate-drive requirements (a function of the trench technology's higher transconductance), the parasitic capacitances of the new MOSFETs are less which, in turn, reduces switching losses at all switching frequencies in a dc-dc converter. This leads to higher efficiency and makes possible faster switching rates. Higher switching rates cut the size of a switcher's inductors and capacitors and ups their response time to plus and minus full-load transients (one of the problems of advanced microprocessors such as the Pentium).

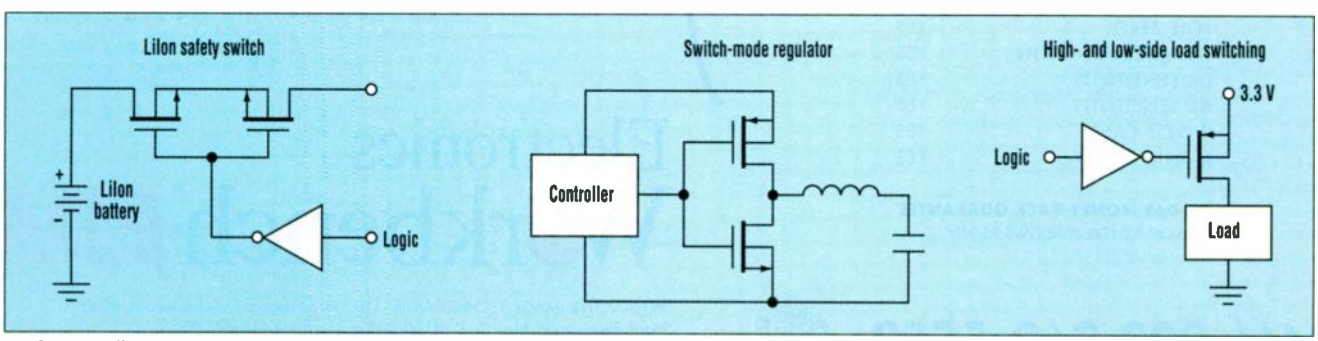
By shrinking the size of individual FET cells, more cells can be paralleled in a given area, and theoretically the array's overall on-resistance reduced.

The low-threshold FETs are particularly useful in applications involving 1 and 2-cell Li-Ion battery packs and systems using regulated buses of 5 V or less. While the low-threshold FETs have somewhat lower maximum V_{DS} and V_{GS} ratings than older devices, their applications will not demand higher ratings. Therefore, as supply rail and logic voltages continue their decline, the low-threshold FETs will find even more applications.

Within a single charge/discharge cycle, a Li-Ion battery puts out from as much as 4.2 V down to a low of 2.5 V. As a result, power switches run directly from the battery. For example, a switching regulator must operate with gate-drive voltages as low as 2.5. The MOSFETs used within every Li-Ion battery pack for the BDS function also must operate at minimum battery voltages (*Fig. 3, again*).

In the BDS application and in some switching regulators, maximum gate drive voltage occurs when the battery is fully-charged. In two-cell battery packs, this voltage can range as high as 8.4 V. As noted earlier, the low-threshold FETs are designed to handle both one- and two-cell batteries. Both combine a maximum gate-to-source rating of 12 V with an on-resistance specified at 2.5 V. Designing the FET to handle voltages up to 12 V demanded minimal thinning of the gate oxide; the input capacitance and gate charge are not altered much by the low-threshold voltage enhancement.

The higher-threshold voltage FETs will improve the performance of systems using battery stacks to 26 V and handle load switching or switching regulators supplies running off regulated 12-V rails. In this situation, p-channel FETs provide an on-resistance virtually as low as that of available n-channel FETs. Therefore, in most applications, a designer can substitute a p-channel FET

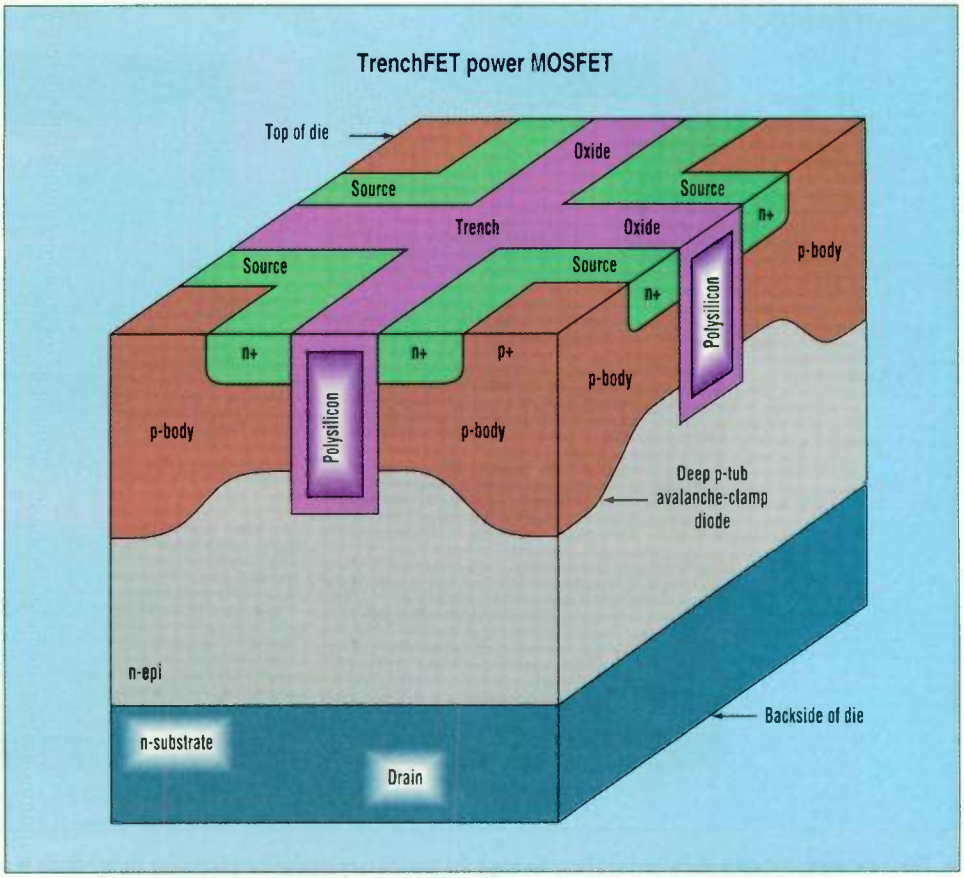


4. The 32 million cells per square inch powerFETs are aimed at three basic applications, Li-Ion battery safety switches, switching regulators, and switching low- and high-side loads.

for an n-channel FET and simplify the drive circuitry.

In applications that demand two MOSFETs (for example, such as a synchronous switcher, or a BDS), a dual FET in a single package may be able to take the place of two individual FETs because the duals and the complementary FETs use separate die that are physically isolated from each other. On the other hand, a complementary device with one p-channel and one n-channel FET die in the same package can often do the job. Unitrode, Merrimack, N.H. is one manufacturer that offers a synchronous buck controller IC designed to drive complementary power FETs (ELECTRONIC DESIGN, *April 1, p. 64).*

The tiny high-performance FET die from the 1997 technology makes it possible to manufacture multichip power ICs with additional features. These can include self and load protection, level-shift, and gate-drive circuits. For example, an additional die as simple as a Schottky diode or as complex as a controller for a switching regulator or an LDO could be incorporated in a package with one or more power FETs. An array of isolated power FETs for power management could find many homes.



5. The TrenchFETS gate permits increasing low-voltage power MOSFET cell density, and lowering device on resistance, without suffering from increased resistance from the parasitic JFET in each cell.

Cell Counts Go Sky High

You might ask: "How did Williams and his cohorts at Temic, FET designer Wayne Grabowski and Director of Process Engineering Dr. Michael Chang, do it?" They are glad you asked. Now for a little technology review provided by Williams.

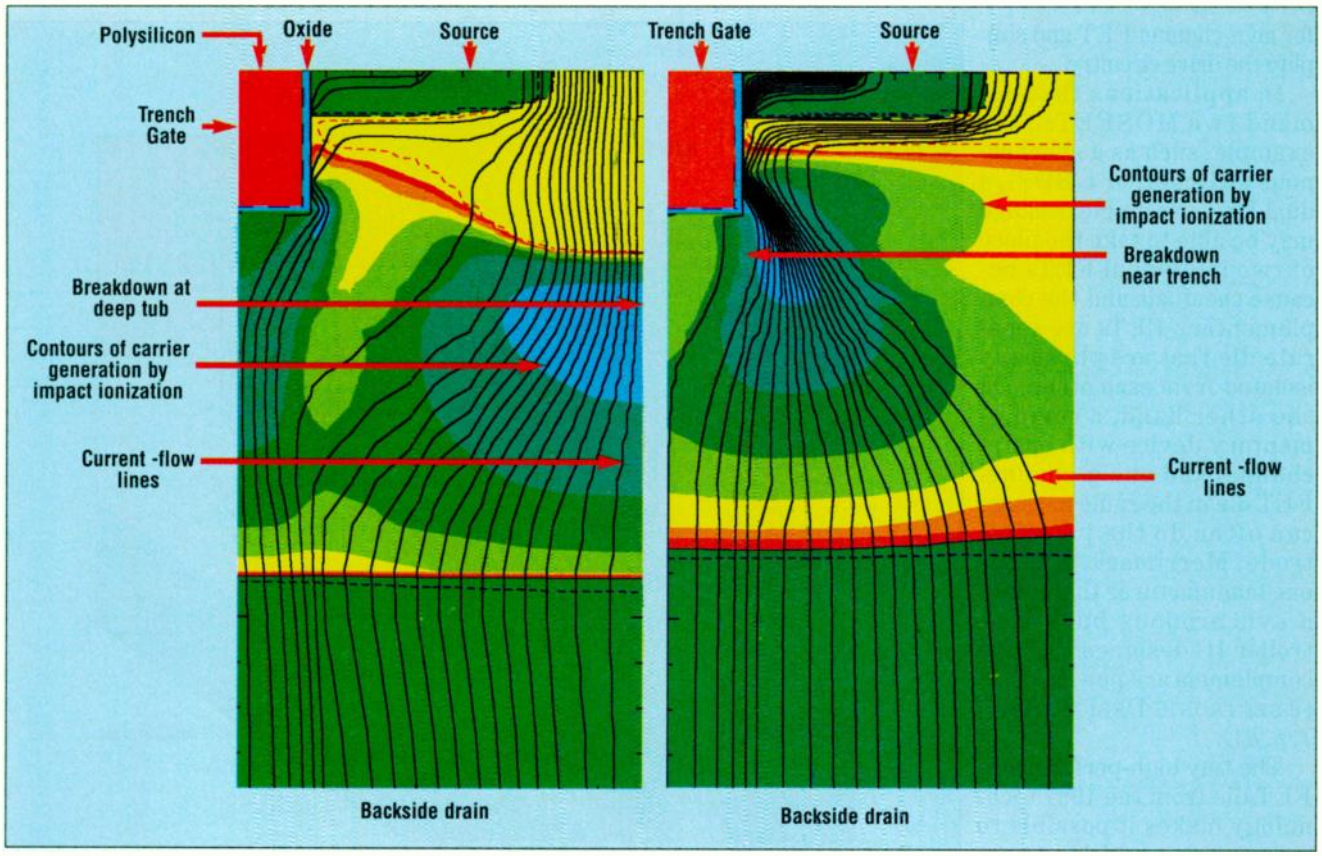
Most vertical power MOSFETs are semiconductor switches consisting of an array of millions of tiny individual vertical DMOSFETs, or cells, all connected in parallel, drain-to-drain, gate-to-gate, source-to-source. This vertical DMOSFET array operating as a single device achieves minimum on-resistance, and with it low on-state voltage drops and high conduction currents while dissipating little power. By shrinking the size of individual FET cells, a process also known as "scaling," more cells can be paralleled in a given area, and theoretically the array's overall on-resistance reduced.

Since their introduction nearly two decades ago as a new technology to compete with power bipolar transistors, cell density, die size, and other technological innovations have continuously cut power MOSFET cost (area of silicon required for a given voltage and current rating) while improving performance (cutting on- resistance, or example). This scaling is somewhat analogous to the ongoing feature size reduction in the processes that fabricate microprocessors and DRAMs; albeit the MOSFETs must handle currents many orders-of-magnitude greater.

However, cell construction often imposes process and design limitations to feature scaling. In conventional vertical planar double-diffused MOSFETs (or VDMOSFETs), current first flows laterally from the source through a surface channel (often of submicron length), the conduc-

GENERATION IV AND V TrenchFET GUARANTEED SINGLE-DIE PERFORMANCE IN AN SO-8 PACKAGE

TrenchFET technology	Maximum rating		Die configuration	R_{DS} (on) typical (mΩ)		
	V_{DS}	V_{GS}		V_{GS} = 10V	V_{GS} = 4.5V	V_{GS} = 2.5V
Early devices (1993-1994)	30 V	20 V	single N-ch	13.5	20	
			single P-ch	20	35	
Low on-resistance (1997)	30 V	20 V	single N-ch	9	13	
			single P-ch	14	23	
Low-threshold (1997)	20 V	12 V	single N-ch		10	14
			single P-ch		16	25



6. These simulation results show current flow through the proprietary avalanche-protection clamp-diode in every cell in early TrenchFETs. Simulation results show potentially damaging current flow close to the gate in a TrenchFET cell without a protecting diode.

tion of which is controlled by the gate-to-source voltage. After passing through the channel, the current turns 90°and flows vertically toward the drain. But the current must first squeeze through the resistance of a parasitic JFET (its pinch-off region), before flowing out a drain contact on the backside of the die.

Reducing the cell size and adding more cells in parallel in the same area basically cuts the resistance of the channel when it is fully enhanced by the gate-to-source voltage. However, at a density of about 7,000,000 cells/in.^{2}, the FET designer hits a point of diminishing returns because reducing cell size any further increases the resistance of this JFET region and cancels out most or all of the reduction in on-resistance. In its proprietary TrenchFET process, Temic brings the trenched gate into the p-body and n-epi material that reduces the effect of the parasitic JFET when cell density is increased *(Fig. 5)*. The trench is etched and coated with oxide. It is then filled with the polysilicon gate material.

Scaling TrenchFETs also has its challenges. In the earlier TrenchFETs, Siliconix designers used a patented structure, which is known as the deep (it goes deeper into the epi material than the gate) p-tub avalanche (zener) clamp diode. A clamp diode in each cell controls the location of breakdown in every cell *(Fig. 5, again)*. As shown in simulation results, the deep p-tub avalanche-clamp-diode forces avalanche breakdown and its "hot" carriers into the bulk silicon and away from the trench gate *(Fig. 6)*.

According to Williams and illustrated by simulation results, anyone (competitors) attempting to produce trench gated MOSFETs using a truly flat p-body/n-epi junction without Temic's patented clamp risks high avalanche currents wherever the gate protrudes through the body-to-drain junction *(Fig. 6 again)*. Driving inductive loads can easily force a power MOSFET into avalanche, so Williams and Grabowski like to control where that occurs in the FET. Despite its benefit, use of the protective diode is problematic since it limits the maximum cell density because it takes up cell area, that is, it makes the cells bigger cutting density.

Williams and his partners solved this problem by distributing a voltage clamp around the die without substantially sacrificing the TrenchFETS avalanche current capability. Their so-called "1-of-n" design locates a diode clamp at regular intervals around the die rather than putting one in every cell. In this design, handling avalanche energy becomes a design parameter rather than just process-related.

PRICE AND AVAILABILITY

Pricing for these MOSFETs in the TSOP-6 start at $0.45 in quantities of 100,000. In similar quantities, prices for FETs in the TSSOP-8 and the SO-8 RUN $1.20 each and $1.41 each, respectively.

Temic Semiconductors , 2201 Laurelwood Rd., Santa Clara, CA 94056-0951. Joyce De Sorbo, (408) 567-8220. **CIRCLE 547**

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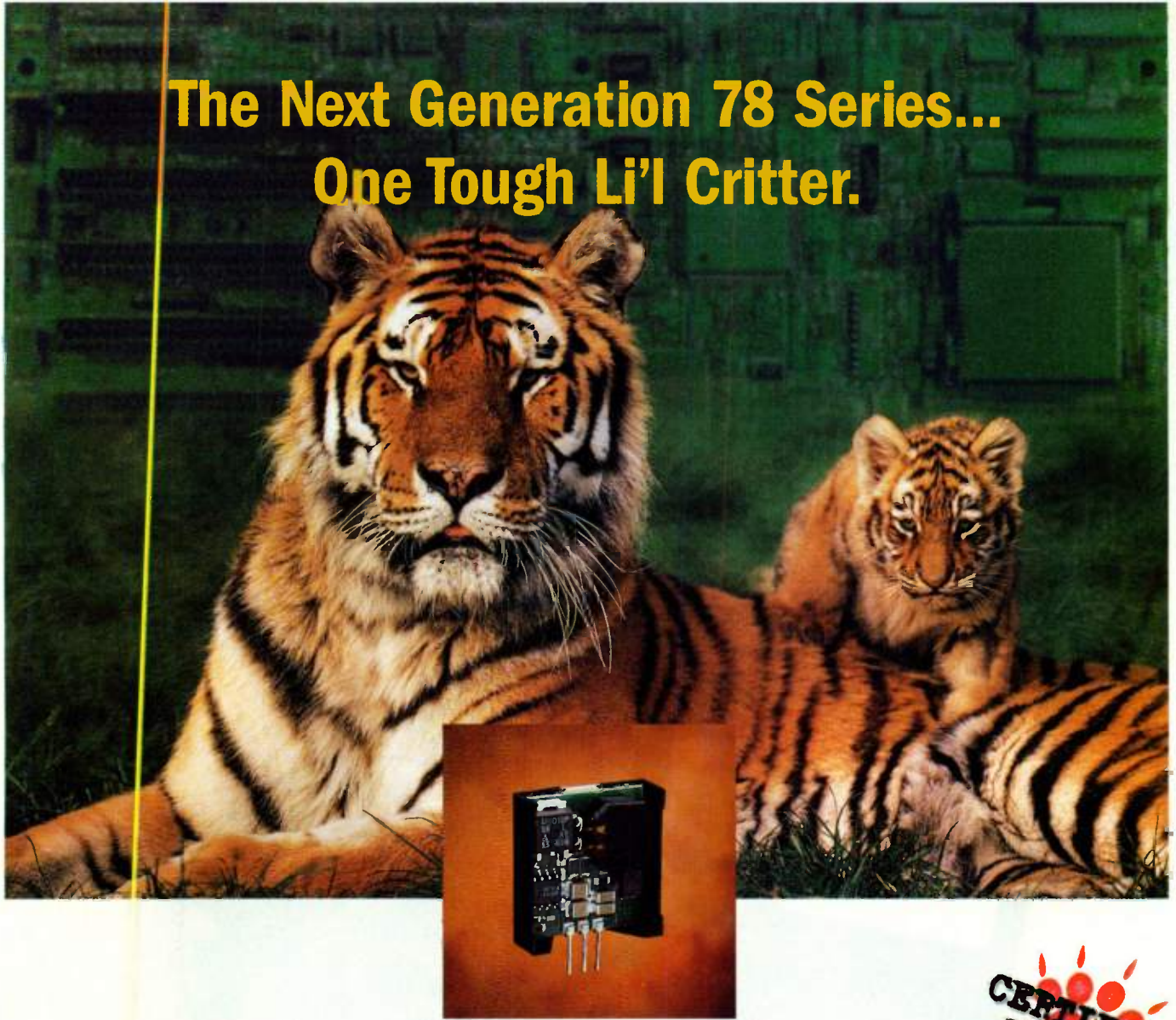

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Test	Method	Conditions
Mechanical Shock	MIL-STD-883D, Method 2002.3	Condition A, 500G peak, 1 mSec, half sine, 5 shocks, 2 directions, 3 axes, (30 shocks total)
Mechanical Vibration	MIL-STD-883D, Method 2007.2	4 four-minute sweeps, 4x each axis, total time 48 minutes, 20 to 2000 Hz logarithmically

ENVIRONMENTAL ENDURANCE TESTING

Test	Method	Conditions
Thermal Shock	MIL-STD-202F, Method 107	200 cycles, -40°C to +125°C, 15 minute dwell time
Humidity	MIL-STD-202F, Method 103	85% relative humidity (non-condensing), 85°C ambient, 240 hours, Vin=Vmax, Iout=10% Imax
Accelerated Life	MIL-STD-202F, Method 108	1000 Hours, 60°C ambient, Vin=Vmax, Iout=Imax

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Test	Method	Conditions
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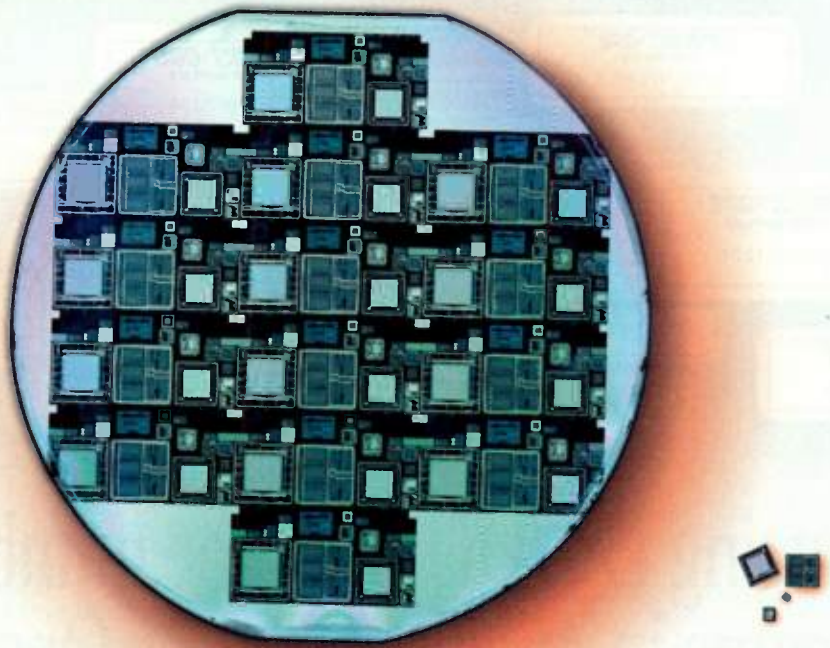

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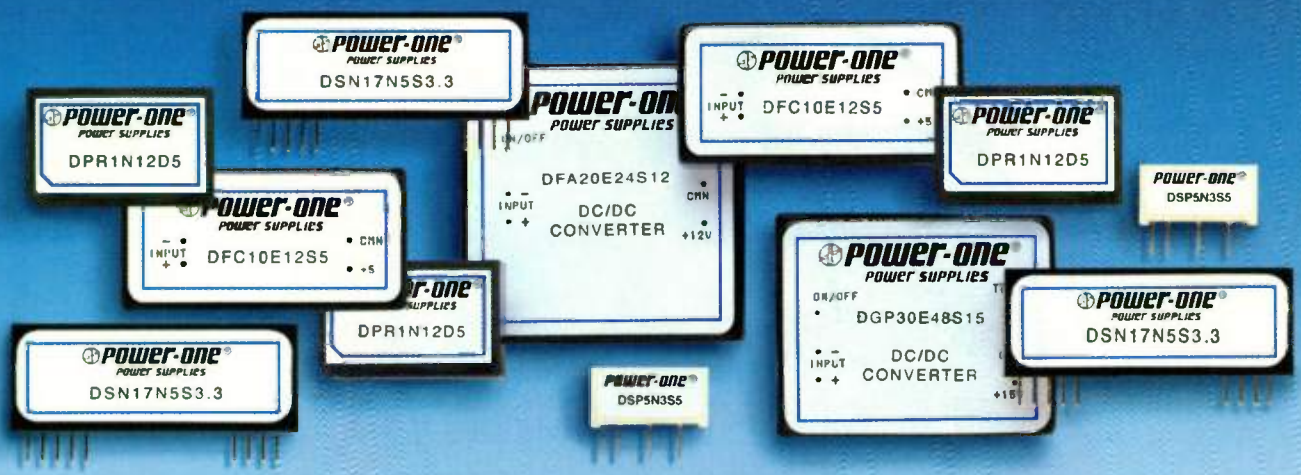

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DFA6	6	9-27, 20-60		•	•		•		•	
DFC6	6	3.5-16		•	•		•		•	
DFC10	10	9-18, 18-36, 36-72	•	•			•		•	
DGP12	12	3.5-16		•			•		•	
DFC15	15	20-60		•			•		•	
DSN17	17	4.5-6, 6.5-15.5	•	•						
DFA20	21	9-18, 18-36, 36-72	•	•			•		•	
DGP30	30	36-72		•			•		•	
Dual Output products provide the indicated Vout as one positive and one negative output										
DSP1	1	4.5-5.5		+/-		+/-	+/-	+/-	+/-	+/-
DFC10	10	9-36, 18-72		+/-			+/-		+/-	
DGP12	12	3.5-16		+/-			+/-		+/-	
DFC15	15	20-72					+/-		+/-	
DFA20	20	9-18, 18-36, 36-72		+/-			+/-		+/-	
Triple Output products provide a main output (•) and two symetrical outputs (+/-)										
DGP20	20	9-18, 18-36, 36-72		•			+/-		+/-	

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CONFERENCE REVIEW

Display Works Conference Spotlights U.S. Manufacturing Advances

Advanced R & D Funding In Materials And Tools Allows Domestic Display Makers To Catch Up With The Competition.

Cheryl Ajluni

The Display Works Conference 1997, held January 29-31 in San Jose, Calif., was a demonstration of the continuing interest and feverish activity occurring in the display industry. The Conference's real impact is not in the exhibits, technical sessions on flat-panel and manufacturing technology, or the introduction of a revolutionary development, but in the ongoing progress made toward a more stable and long-lasting multitechnology display infrastructure.

Two organizations, the U.S. government's Defense Advanced Research Projects Agency (DARPA) and the United States Display Consortium (USDC), have doled out large amounts of money for a variety of display-related research and development projects. For example, the USDC, an industry-led public/private partnership chartered by the U.S. government to enhance the competitiveness of flat-panel display (FPD) manufacturers, at the end of last year announced a $1.2 million multiprogram contract with Supertex Inc., San Jose, Calif., to develop a display driver chip design and associated packaging. The goal of the project is threefold: to establish a fast turnaround operation for the design, prototyping, and fabrication of specialty driver chips; to reduce the cost and size of these chips by fabrication on silicon-on-insulator (SOI) substrates; and to advance packaging capability from current plastic-leaded chip carriers (PLCC) to tape-automated bonding (TAB) for size reduction.

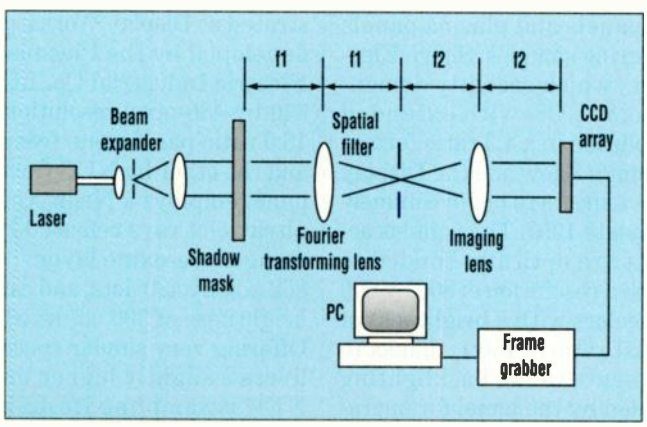
While the Supertex project is in the beginning stages, the fruits of labor on other projects are becoming apparent. As detailed in paper 1.3, researchers from Science Applications International Corporation (SAIC), San Diego, Calif., under the auspices of the USDC Backlight Program, have developed a backlight assembly based on a fluorescent-cavity design. The design can be tailored for various LCD sizes, and display specific mechanical and electrical interface requirements. It also adapts to different environments.

The backlight comprises an ultraviolet exciter mounted within a cavity formed by a phosphor-coated housing. Its four components include a cover glass, quartz lamp, housing, and driver electronics. The backlight design is available in a range of sizes from 4 in. by 4 in. to 10 in. by 12.5 in. The backlight design has a history of proven performance for use with LCDs in military equipment. And, while it is not expected to compete with the simple, edge-lit backlight used in commercial laptop computers, it is primed for use in demanding military applications. A lower cost, lower performance version also will be available for industrial applications where sunlight readability and rugged features are required.

This development, part of a $4.3 million shared effort between the USDC and SAIC, is one of many designed to foster the growth of the LCD industry. The completion of the project promises to enable a 12,000-backlight-assemblies per year manufacturing capability. Production is expected to begin in the first half of 1997.

DARPA's contribution to the establishment of a competitive display-manufacturing infrastructure lies in its sponsorship of the Consortium For Intelligent Large-Area Processing (CILAP). This program was established with three prime objectives: to develop low-cost, high-volume, thin-film manufacturing processes; to demonstrate the integrated capability; and to transfer the manufacturing technology to the U.S. electronics industry. With the help of The Dow Chemical Company, Midland, Mich., and Radiant Technology Corporation, Anaheim, Calif., the first of these objectives has now been met.

The development, as detailed in paper 2.2, is a prototype oven designed for rapidly curing BCB, also known as PFCB (perflourocyclobutene) thin-film organic insulator coatings with tight uniformity (±2.5°C). The oven can handle panels up to 400 mm by 400 mm. It is based on models of the thermal BCB cure process using existing lamp infrared-radia-



1. The rapid-pattern inspection system developed by the Korea Advanced Institute of Science and Technology in conjunction with the LG Electronics Production Research Center can be used for quality assurance in the manufacture of shadow masks. It comprises a number of optical components, and relies on the use of a Fourier-transformed image of the shadow mask to expose any defects.

tion (IR) furnaces and finite-element modeling of an advanced oven using arrays of tungsten-halogen bulbs.

Initial testing of the equipment has shown that it is compliant with specifications for low particulate levels within the process area, and can provide an inert atmosphere to adequately prevent coating oxidation. Ongoing work on this project will focus on further refinement of the oven control algorithm to ensure ±2.5% or °C across-panel temperature uniformity. Demonstration of the equipment is currently underway.

It is apparent from projects such as those funded by DARPA and the USDC that wanting to be a strong force in the display arena and actually becoming one are two different stories. The U.S., in particular, strives to be a formidable player in this area, supporting research into developing new display technologies and making improvements to exiting technology. But the bottom line is that without the means to mass produce these technologies for commercial use, being a dominant player in the display arena is nothing more than a pipe dream. Until now, the manufacturing infrastructure to achieve such a goal has been a major limitation in the U.S. attempts to move forward. The DARPA and USDC efforts, as well as research and development efforts by individual companies (some of which were highlighted at Display Works), have contributed to progress in this area.

The backlight design has a history of proven performance for use with LCDs in military equipment.

Paper 3.1, for example, from the researchers at the Korea Advanced Institute of Science and Technology, Taejon, and LG Electronics Production Research Center, Pyeongtaek, Korea, highlighted a new technique for rapidly inspecting for pattern defects residing on shadow masks. Based on the use of machine vision and Fourier optics, irregular defects are captured in real time by blocking the periodically repetitive pattern of normal mask holes. The pattern is blocked via a coherently-illuminated pinhole-type spatial filter. Background and noises are suppressed through software image processing that uses a special image processing algorithm. Shadow masks for the cathode ray tube (CRT) are typically comprised of a thin, Inbar metal plate on which a two-dimensional array of fine holes, either rectangular or circular in shape, is fabricated. Traditionally, inspection of these shadow masks for abnormal holes was done visually. The problems associated with this technique are obvious—the accuracy of defect detection and repeatability of inspection results is dependent on the person conducting the test.

With the use of machine-vision techniques and Fourier optics, the process accuracy depends solely on the test equipment *(Fig. 1)*. This method enables only defect holes to be extracted from the shadow mask because the normal holes are periodic and have a constant pitch. The defect holes, on the other hand, violate this periodicity and can be singled out because they block the normal pattern. With spatial filtering using a pinhole filter, the regular normal hole pattern is suppressed, allowing only the defect holes to pass.

Paper 6.2, from researchers at Tamarack Scientific Co. Inc., Anaheim, Calif., details a two-dimensional scanning-projection lithography tool, developed under a USDC contract, that can provide exposure for an area of substrate of up to 840 mm by 1025

Large-Area LCD And Plasma Panels Begin Sampling

A number of companies targeting the manufacture of large-area color LCD panels and plasma panels are now offering engineering samples. Sharp Electronics Corp., Camas, Wash., which recently demonstrated a 40-in. diagonal color LCD with extended graphics adaptor (XGA) resolution in a 4:3 ratio format at both the Consumer Electronics Show and the Display Works conference in January, expects to begin commercial sampling of the display in late 1997. The panel is actually two 20-in. panels that are optically bonded to form a single display area with a resolution of 800 by 600 pixels. It can display 16.7 M colors with a brightness of about 200 cd/m^2 and a contrast ratio of 150:1, thanks to some proprietary improvements to the backlighting scheme. About 130 W is needed by the panel for operation, with most of that power consumed by the backlighting. And, to ensure a stable, high-quality picture, the panel employs low-voltage differential signaling between it and the host system, minimizing potential electromagnetic interference.

A trio of plasma display panels also were demonstrated at Display Works: a 42-in. diagonal 4:3 ratio unit developed by the Plasmaco subsidiary of Matsushita Electric Industrial Co. Ltd., Highland, N.Y., provides 640-by-480-pixel resolution; and a pair of 42-in. diagonal 16:9 ratio panels, one from Fujitsu Ltd., Tokyo, Japan, and the other by NEC Corp., also in Tokyo. The Fujitsu panel employs a Neon/Xenon gas mixture, excited by ultraviolet rays released by the surface discharge of a manganese-oxide layer. The panel has a resolution of 852 (x3) by 480 dots, and can display 16.7 M colors with a brightness of 300 cd/m^2 while consuming about 300 W. Offering very similar specifications, the NEC panel delivers a slightly higher brightness level of 350 cd/m^2. NEC is sampling its 42-in. panel, with single-units priced at roughly $12,000. Volume pricing will drop the cost by 50% when the displays ship in lots of 1000 units/month. Fujitsu's panels are currently sampling, and in similar volumes will sell for about $5000/unit.

Dave Bursky

Fig. 1

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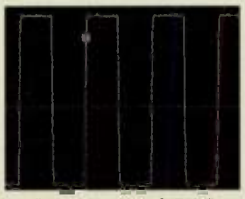

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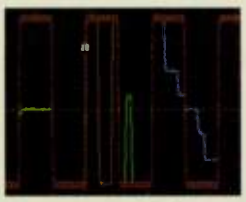

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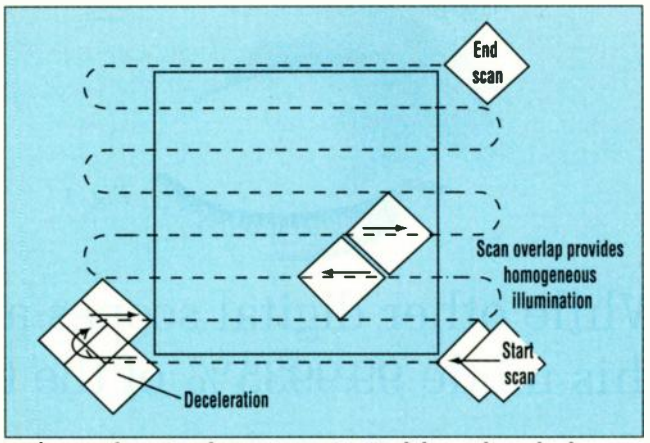
Max. Record Length	250K	500K	250K	500K	500K
Max. Wfm. Acquisition Rate	100,000 Wfm/s	100,000 Wfm/s	180,000 Wfm/s	400,000 Wfm/s	400,000 Wfm/s
Display	Monochrome	Monochrome	Color	Color	Color

Tektronix

mm *(Fig. 2)*. The tool uses a scanning-projection concept that patterns large substrates for flat-panel displays and (multichip modules) MCMs . With this approach, researchers have been able to demonstrate the alignment and resolution of large-meter size substrates down to 3 µ.

The intermediate-resolution lithographic tool is available now, and able to work with substrates in manufacturing a variety of display types including electroluminescence (EL), active-matrix liquid crystal display (AMLCD), field emission display (FED) and plasma display. Because the tool can be used in a mix and match mode, it is expected to significantly reduce the cost of manufacturing flat panel displays.



2. The two-dimensional, scanning-projection-lithography technology developed by Tamarack Scientific works by continually scanning a mask of the same size as the panel, through the image plane of a noninverting, 1:1 projection system. During this process, the projection system is constantly projecting a small fraction of the mask image onto an equally-sized fraction of the substrate. Since the substrate and mask are mounted on the same stage, the mask image always falls onto the correct substrate location. Subsequently, the scanning operation can expose the entire substrate, and is adjustable to any substrate size.

While display manufacturing is certainly a hot area of research, there is some focus on refining existing display technologies and implementing them in commercially available products *(see "Large-Area LCD And Plasma Panels Begin Sampling," p.56)*. Paper 1.1, from Samsung Electronics Co. Ltd., AMLCD Division, Kiheung, Korea, reported the results of research in the area of low-dielectric constant organic interlayer materials. These materials, which can be used for back-channel passivation of etch-type thin-film transistors (TFTs), as well as for inter-layer insulators, are effective in minimizing capacitive coupling and significantly increasing aperture ratio. The research, which focused primarily on three organic materials: polyimide, acryl, and dry-etchable PFCB, examined the extent to which the use of such materials could improve aperture ratio and decrease capacitance coupling. High aperture ratio, in particular, has been a key obstacle in enabling low power consumption of TFT LCD panels. This task is made even more formidable by the capacitive coupling that occurs between the pixel interface transfer object (ITO) and data line, inducing the light leakage due to the lateral electric field. The typical method of dealing with this problem has been covering the capacitive-coupling-induced declination line with a black matrix (BM) on the color-filter side. Unfortunately, this technique limits the enhancement of the aperture ratio. The only way to optimize the aperture ratio is to minimize the lateral field induced by the capacitive coupling.

Researchers found that by using the organic materials as an interlayer insulator between the data line and the pixel ITO—effectively putting the pixel-ITO layer on top of the low-dielectric interlayer insulator— the lateral field could be minimized by controlling the film thickness. The width of the data line determines the aperture ratio of the pixel. Also, because organic films feature excellent planarization, the TFT surface also is planarized, helping to guarantee the uniformity of liquid crystals' alignment, as well as the cell gap. No degradation of TFT performance was noted as a result of using the organic materials. These materials are targeted to variety of FPD-based applications.

In a related development, the researchers at the Durability and Functional Performance Polaroid Corporation, Polarizer Division, Norwood, Mass., and Nippon Polaroid, Tokyo, Japan, have developed and begun commercialization of an improved K-type polarizer. Referred to as KE, the polarizer laminate offers significantly improved polarization efficiency and color rendition, enabling its use in environmentally-demanding LCD applications. Made from the linear orientation of polyvinylalcohol (PVA) sheets or film, the KE polarizer derives its light-absorption properties from an acid-catalyzed thermal-dehydration reaction resulting from significant unsaturation within the polymer backbone.

The improved efficiency demonstrated by the KE polarizer is derived from a newly-developed stretching scheme for PVA films or sheets that results in a high degree of molecular orientation for the polymer chains. An advance in the maintenance of the dehydration kinetics to control the distribution of conjugation lengths in the polyvinylene also is significant since it determines the spectral region in which the chromophore absorbs light. In addition, treating the web with a finishing chemical bath in which the pH as well as the anionic/cationic balance of various ionic species are rigorously maintained, works to improve the overall efficiency of the KE polarizer. In fact, the researchers report that for KE, efficiencies in excess of 99.9% at a Kv (the average visual transmittance to unpolarized light) of 42% can be obtained.

Another important feature of the KE polarizer is its environmental stability, which is a result of its chemical nature. Due to its high performance, it is believed that the KE polarizer will lead to a redesign of the basic LCD structure, and possibly the manufacturing process. This, in turn, could spawn an economic benefit with correspondingly lower cost products. In addition it can be used in existing LCD applications where durability is a key attribute. Its availability may even open up applications previously inaccessible due to the limited durability of the polarizer. Such applications include automotive and telecommunications.

How Valuable	Circle
Highly	533
Moderately	534
Slightly	535

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READER SERVICE 167

PRODUCT FEATURE

Data sheets on products like these can be found at www.penton.com/ed/

RISC-Based Platform Speeds Networking Applications Development

Thanks to its embedded development software and flexible architecture, the ACE860 RISC-powered development platform can help accelerate the design cycle of virtually any internetworking product. Based on the MPC860 PowerQUICC chip, the ACE860 features an open motherboard standard for internetworking products. Its on-board real-time kernel and development tools can dramatically cut the time and effort required to produce high-performance routers, Frame Relay devices, xDSL access multiplexers, remote access servers, and primary-rate ISDN systems.

The board's four interface slots accept any one of a series of network interface modules (NIMs), which can in turn provide a mix-and-match combination of Ethernet, T1/E1, CSU/DSU, and ISDN interfaces. A programmable serial interface NIM allows it to support a variety of sync/async interfaces, including RS-530A, RS-530/RS422/V.11, and RS-232/V.28. Applications can be developed using the board's RTXC real-time operating kernel and ROM-resident diagnostics. If desired, optional bridging/routing software also can be supplied.

While it comes equipped with 4 Mbytes of 32-bit DRAM, the system can accommodate up to 32 Mbytes if needed. Its 1.5-Mbyte flash ROM provides more than adequate storage for the real-time kernel and applications software. A 96-pin bus expansion interface connector and a Motorola-standard, 10-pin, on-chip emulation header provides further development support. A console interface is provided in the form of a set of RS-232 transceivers, terminated in a single RJ-11 jack.

All of the ACE860's communications functions are run under the control of the MC68360, a PowerPC core that sports internal data and instruction caches as well as an on-chip communications processor module (CPM). The CPM has four high-speed serial controllers, each with two DMA channels that can implement most popular layer-communications protocols (Ethernet, HDLC, SDLC, UART, and asynchronous HDLC) in hardware. Depending on the chip, it can deliver as many as 52 MIPS while running at 40 MHz.

The ACE860 is available from stock for $999 in small quantities, falling to less than $399 for 1000-piece orders of selected models. The network interface modules (NIMs) range in price from $99 to $199 in small quantities.

Atlas Computer Equipment Inc.
3700 State St.
Suite 200
Santa Barbara, CA 93105
(805) 898-2450 or (800) 224-1223
fax (805) 898-2452
e-mail info@ace360.com
Web: http://www.ace360.com
CIRCLE 536
LEE GOLDBERG

PRODUCT FEATURE

Data sheets on products like these can be found at www.penton.com/ed/

Test-Pattern Generator Speeds Creation of Mixed-Signal Tests

Specifically designed for mixed-signal circuits, TestDirect is a virtual test productivity tool that automatically generates test patterns for automated test equipment (ATE). TestDirect creates the pattern from the designer's original testbench simulation environment, which simplifies the process, saves time, and improves quality. Also, designers needn't change their existing design methodology.

TestDirect first documents the device's behavior by using timing-diagram waveforms. The engineer graphically creates or imports the waveforms and the software automatically converts them into HDL "watcher" code. This runs with the simulation of the design, monitoring the design activity and creating cyclized patterns directly. The tool then combines these patterns with waveform timing and formatting information from the targeted tester to create tester-specific test patterns.

This proprietary approach eliminates the processing of large dump files and the multiple, incremental refinement of databases. A feature called Intelligent Data Filtering reduces the amount of extracted data by selecting only the desired simulation events, substantially reducing development time.

Another feature, Dynamic Pattern Cyclization, ensures correctly cyclized test patterns by monitoring the design testbench. Matching desired trigger events and timing data produces fully cyclized test pattern data from the simulation environment. Dynamic Pattern Cyclization also manages ambiguous edge placements, variable timing, multiple timesets, and multiple case matching.

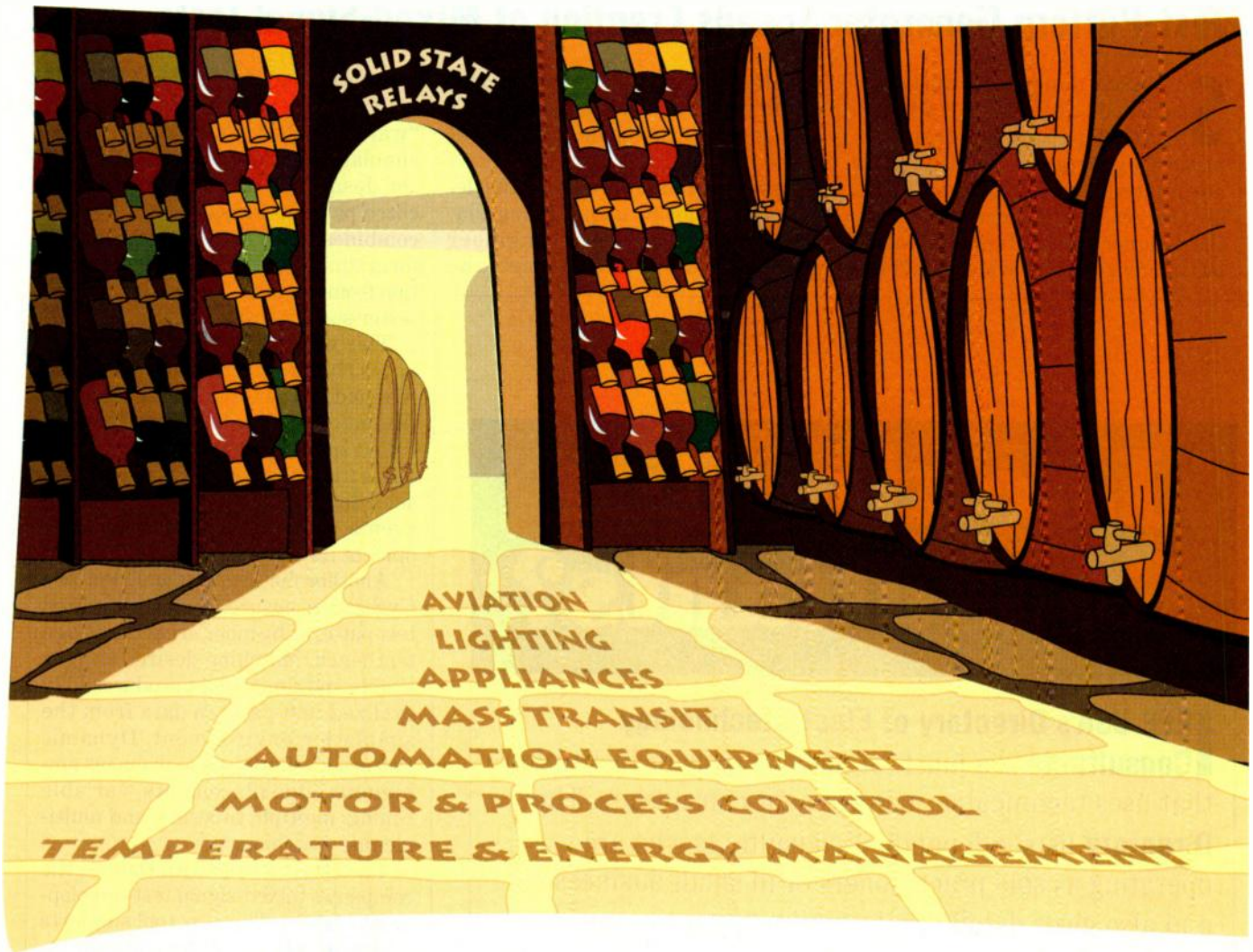
TestDirect works with Dantes, the company's mixed-signal test-development system. The new tool supports mixed-signal test by automatically inserting tester subroutine calls into the test program at the appropriate locations to correctly drive the ATE for mixed-signal testing. The tool provides for direct mapping of signal names to ATE channels, device-under-test pins, multiplex conditions, and pattern mapping.

Because TestDirect runs with any standard VHDL or Verilog simulator, it doesn't require a programming language interface. Initial tester support will include the Hewlett-Packard 9490 through 9495, the IMS MTS FT, and the Teradyne A570 and A580. Prices start at $35,000.

Integrated Measurement Systems Inc.
9525 S.W. Gemini Dr.
Beaverton, OR 97008
(800) 879-7117 or (503) 626-7117
Internet: http://www.ims.com.

CIRCLE 537
JOHN NOVELLINO

FOR THE DISCRIMINATING PALATE



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READER SERVICE 180

ELECTRONIC DESIGN QUICK LOOK

Edited by Mike Sciannamea and Debra Schiff

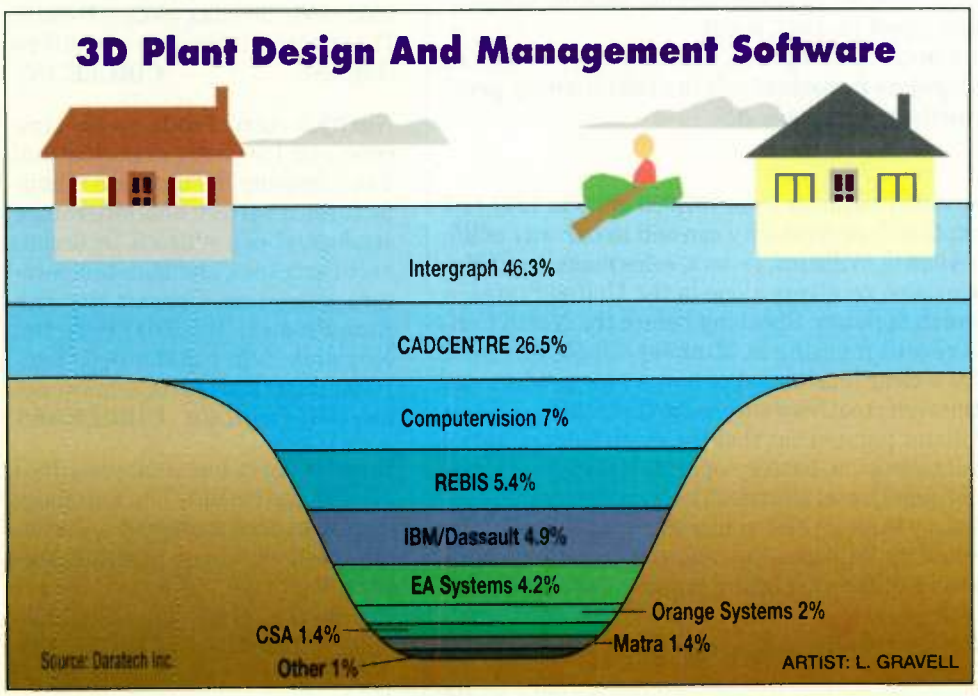
MARKET FACTS

Flooding The Market

The rivers of 3D plant design and plant management software have overflowed their banks, causing the market to rise 28%, cresting at $97 million in 1996. According to Daratech's "CAD/CAM, CAE: Survey, Review, and Buyer's Guide," the swelling tide of growth in this market is due to the increased acceptance of the cost-effectiveness of 3D technology to design and maintain power and process plants. The rise in demand for 3D technology also is attributable to ever-higher pressure on plant owners and operators, as well as construction and engineering businesses to minimize costs, tighten schedules, improve quality, and utilize automated tools to more effectively manage their plants. Swimming well ahead in the race to capture the 3D plant design and plant management market is Intergraph Corporation, taking 46.3% of the market share. That portion of the 3D plant design and plant management software market is a 44% improvement from 1995 for Intergraph. Looking at the company's revenues of $44.9 million in 1996, Intergraph experienced a 34.8% growth. The successful market share percentage is the result of Intergraph's widely used PDS 3D plant design system, as well as the system's related applications. Closing up the gap on Intergraph is CADCENTRE Group plc, with 26.5% of the 3D plant design and plant management software market. Between Intergraph and CADCENTRE, the two enterprises seal up almost three-quarters of the total 3D plant design and plant management software market revenue. Making a big splash in the market, CADCENTRE's revenues in 1996 were estimated at $25.7 million. CADCENTRE's market acumen is tied to the company's PDMS family of 3D plant design and management products. The PDMS software line raised the 3D segment of CADCENTRE's business approximately 33.2% in the last year. That improvement marks a one-point rise in market share over the company's 1995 position. The PDMS tools are based on an associative, database-centric approach. The remaining quarter of the 3D plant design and plant management software market belongs to Computervision (7%), REBIS (5.4%), IBM/Dassault (4.9), EA Systems (4.2%), Orange Systems (2%), CSA (1.4%), Matra (1.4%), and other companies (1%). In addition to the figures comparing market share, Daratech's new survey relates emerging trends, technology news, and vendor strategies in the CAD/CAM and CAE markets. The survey, review and buyer's guide is updated on a monthly basis, and is available at a price of $972 per year from Daratech.

For more information, contact Daratech Inc., 255 Bent St., Cambridge, MA 02141; (617) 354-2339; fax (617) 354-7822; Internet: http://www.daratech.com.

—*DS*



40 YEARS AGO IN ELECTRONIC DESIGN

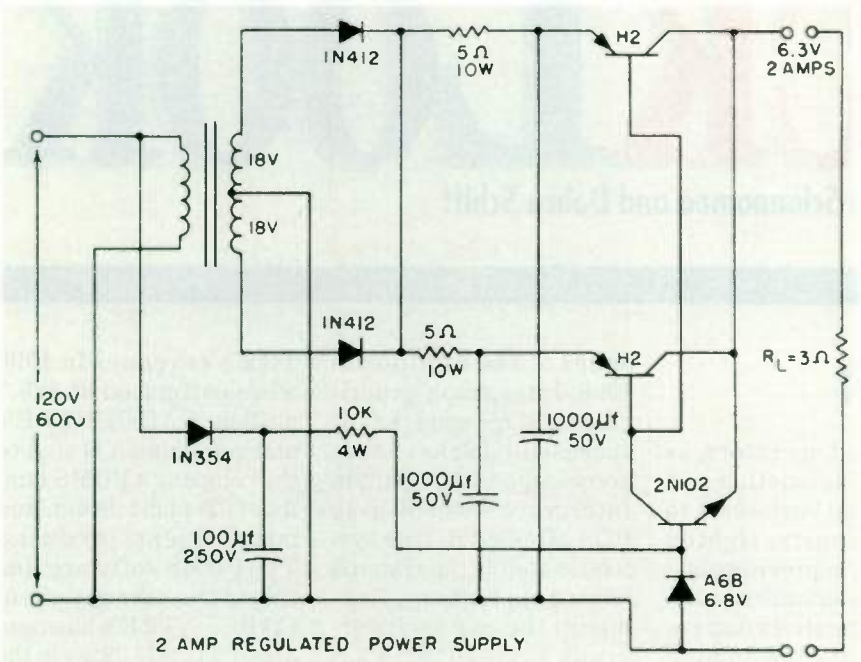


Fig. 2: 2 amp regulated supply.

Design Procedures For Semiconductor Regulated Power Supplies

...The design is now complete, and the regulation factors may be calculated to determine whether the specification requirements are met. A power supply designed according to this procedure, and rated at E_o = 6.3v and I_L = 2 amp is shown in Fig. 2. ...A noteworthy feature of this supply is the regulator efficiency of greater than 50% which is unusually high for a supply at this voltage and current level, and makes regulated d-c filament supplies feasible in equipment design. *(Electronic Design, April 15, 1957, p. 22)*

This is a brief extract from a larger, step-by-step, how-to-design article. In the 1950s, Electronic Design played an important role in disseminating practical design information on transistor circuits. —SS

TV Industry

The meteoric rise of the television business from 137,000 units in 1947 to 7 million units in 1956 is an example of how creativity can add to our way of life and our economy, according to Allan G. Williams, general sales manager of Motorola Inc. The operation of television receivers alone in the United States in 1955 consumed $481,000,000 worth of power. Speaking before the North Central Electrical League at its recent meeting in Minneapolis, Minnesota, Williams pointed out that TV is a clear illustration of how a new product can enter the business scene and through creativity succeed and prosper.

Looking into the future, Williams pointed out that the electronics industry is just in its infancy. Mural wall television, battery operated portable television, wireless paging devices for family use, electrically controlled traffic systems, and improved highway safety through electronics were only some of the "down-the-road" possibilities cited by Williams. Push-button drive-in grocery stores and waterless washers were other such future possibilities mentioned. *(Electronic Design, April 1, 1957, p. 17)*

This appears to be one of the few future-looking articles that got at least some things right.—SS

EYE ON ISO 9000

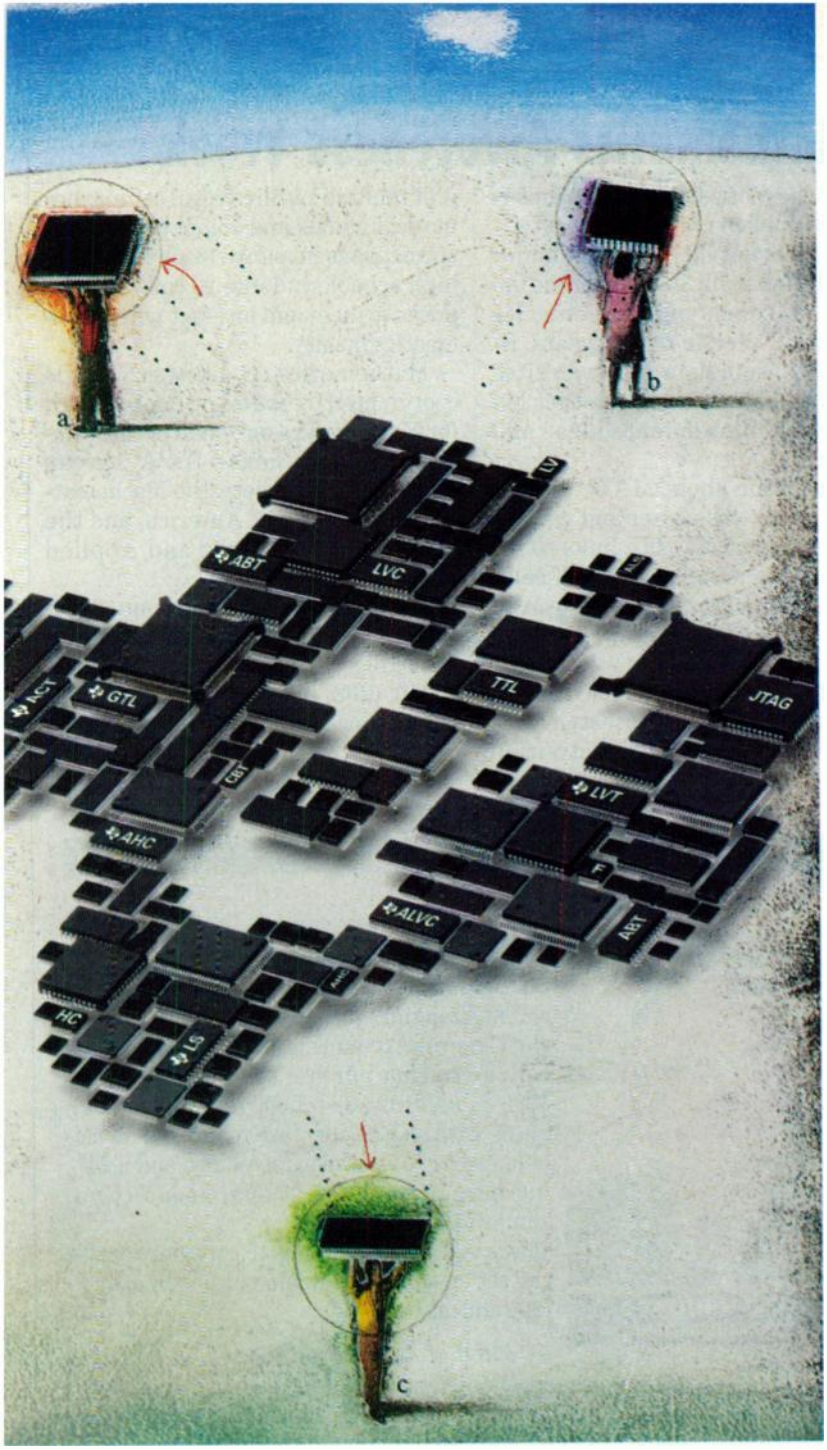
Bicron Electronics Co. has received ISO 9001 certification. The company manufactures general purpose dc and specialty solenoids for battery operation and fluid control applications. Contact Bicron Electronics Co., 50 Barlow St., Canaan, CT 06018; (860) 824-5125; fax (860) 824-1137; Internet: http://www.bern.com. **CIRCLE 485**

Merix Corp. has achieved ISO 9001 registration. The company manufactures interconnect solutions, including advanced pc boards and laminate-based IC packages, for use in various electronic equipment. Contact Merix Corp. 1521 Poplar Lane, P.O. Box 3000, Forest Grove, OR 97116-0300; (503) 359-9300; fax (800) 525-5769; Internet: http://www.merix.com. **CIRCLE 486**

Microchip Technology Inc. has received ISO 9001 certification. The company supplies field-programmable 8-bit microcontrollers, serial EEPROMs and related specialty memory products, code hopping devices, and a family of masked ASICs, for FPGA/ CPLD conversions. Contact Microchip Technology Inc., 2355 W. Chandler Blvd., Chandler, AZ 85224-6199; (602) 786-7200; fax (602) 899-9210; Internet: http: //www.microchip.com. **CIRCLE 487**

Norwich Aero Products Inc. has received ISO 9001 certification. The company designs and manufactures a variety of temperature sensors, speed sensors, interconnect harnesses, and high-temperature connectors. Contact Norwich Aero Products Inc., 50 O'Hara Dr., Norwich, NY 13815; (607) 336-7636; (607) 336-2610; e-mail: noraero@norwich.net. **CIRCLE 488**

Hamlin Inc. has achieved ISO 9001 registration. The company manufactures standard and custom reed switches, position sensors, and reed relays. Contact Hamlin Inc., 612 E. Lake St., Lake Mills, WI 53551. **CIRCLE 489**



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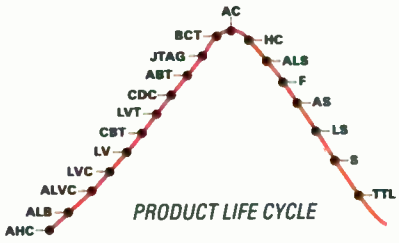

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TEXAS INSTRUMENTS

The Internet Adds To Mathematics Awareness Week

The theme for Mathematics Awareness Week (MAW) 1997, which will be observed nationwide from April 20-26, is "Mathematics and the Internet." Developments in mathematical fields such as number theory and queuing theory have enabled key Internet technologies including data encryption for secure financial transactions, data compression for messages with audio and/or video components, and routing and network configuration.

The Internet has given rise to worldwide collaborations among mathematics teachers and researchers. These collaborations are advancing both education from kindergarten through university, as well as increasing understanding of some of the most difficult problems in pure and applied mathematics.

The Internet has played a major role in dramatically increasing the impact and reach of Mathematics Awareness Week in recent years. E-mail, discussion lists, and web sites are now commonly used to gather, exchange, and disseminate ideas and materials.

Information about MAW '97—including the theme poster and visuals, an annotated essay with links to related sides, and news of MAW celebrations—is on the World Wide Web at: *http://forum.swarthmore.edu/maw/*.

Celebrations will take place at colleges, universities, and research laboratories across the U.S. Activities will include public lectures, mathematical games and competitions, and special days in many states that bring high school students to college campuses to meet and interact with mathematics faculty.

Mathematics Awareness Week is coordinated by the Joint Policy Board for Mathematics on behalf of three national organizations—the American Mathematical Society, the Mathematical Association of America, and the Society for Industrial and Applied Mathematics.

For more information, contact the Joint Policy Board for Mathematics, 1529 18th St. NW, Washington, DC 20036; (202) 234-9570; fax (202) 462-7877; e-mail: jpbm@math.umd.edu.—*MS*

TIPS ON INVESTING

Everyone, including engineers, managers, consultants, and technicians, needs a financial plan at every stage of life. A basic rule of thumb to use when creating your financial plan is to balance current lifestyle against future needs. At each stage of your life, you should reevaluate your current portfolio and investment strategy. Here are some basic guidelines for "what to do when."

HENRY WIESEL
CONTRIBUTING EDITOR

The Next Generation

Suppose you've started a new job and moved into your own place. While saving money during this time could be difficult, there are a few simple steps you can take to help improve your future financial outlook.

A common mistake is living from paycheck to paycheck. There are few things more frustrating than paying off last month's credit card bills with this month's paycheck. Pay off your credit cards every month. Better yet, use a debit card instead of a credit card; the charges will automatically be deducted from your account and you will avoid interest rates adding to your credit card balance.

Put away as much as you can for retirement. You may think, "I'm just beginning my career. Why should I be thinking about retiring?" Starting early pays off. If you are age 25, and want to accumulate $1 million in retirement savings in such accounts as IRAs and 401(k)s by the time you turn 65, you should immediately begin saving $3900 annually. Assuming an 8% rate of return, you should reach your goal.

The Family Years

During the years after you've settled down with your spouse, you'll be faced with the greatest financial challenge of all—raising a family. Saving for your children's education may be the most significant expense. According to the General Accounting Office, the average college tuition jumped 234% between the 1980-81 and 1994-95 school years. That compares with an 82% increase in median household income over the same period and a 74% increase in the Labor Department's Consumer Price Index.

There are several options to consider to ease the severe financial strain of affording a college education:

- *Custodial Account for Your Child:* This will allow you, and other friends and relatives, to make gifts of cash or securities to your child. These assets belong to your child and you can only spend them for your child's benefit.
- *Trusts:* You also may choose to set up a trust for the benefit of your child. With a trust, you can prescribe exactly how and when the money will be used.
- *Financial Aid:* If you intend to qualify for financial aid, you should save in your name, and earmark specific funds for your child's education.

The next column will discuss financial planning for the "50 Plus Years" and "Gearing Up for Retirement."

Henry Wiesel is a Vice-President/Financial Consultant and Qualified Pension Coordinator. He may be contacted at Smith Barney Inc., 1040 Broad St., 2nd Floor, Shrewsbury, NJ 07702; (800) 631-2221, ext. 8653.

Ladies And Gentleman, *Charge* Your Engines

Every year in the month of May, the eyes of the auto racing world focus in on arguably the most famous race in the world, the Indianapolis 500, better known as the Indy 500. Held during the Memorial Day weekend, millions of people gather around their televisions to marvel at the magnificent vehicles reaching speeds up to 250 miles per hour over a 500-mile race, complete with frequent pit stops for refueling and repair.

Another event taking place around the same time of the Indy 500 may not draw as much attention, but may have a significant impact on the type of vehicles we non-race drivers will operate in the future. The 9th Annual Northeast Sustainable Energy Association (NESEA) American Tour de Sol will take place May 17-23. But it's not just another race around the track. It's a 350-mile road rally that begins in Waterbury, Conn. and ends in Portland, Me. The field consists of 50 top electric, hybrid, and solar-powered vehicles, and all are required to maintain normal highway speeds and earn points based on range (distance traveled without recharging), efficiency (miles per equivalent gallon of gasoline), and dependability.

Entries from major automakers such as Toyota and Ford will compete alongside vehicles from speciality manufacturers such as Solectria to demonstrate the capabilities of these vehicles to potential consumers. In addition, the road rally will feature sedans, pickup trucks, and other purpose-built vehicles designed by high school and university students from around the country. The Goodyear Tire and Rubber Company is the major corporate sponsor of the Tour de Sol, with the U.S. Dept. of Energy and the Waterbury Convention and Visitors Bureau joining them as major sponsors.

The tour begins with two days of qualifying tests in Waterbury on May 17-18. The road rally itself begins on May 19, and ends on May 23 in Portland, Me. Additional activities are scheduled along the route with stops in Northampton and Greenfield, Mass.; Bellows Falls and White River Junction, Vt.; and Lincoln and North Conway, N.H.

During the course of the event, the NESEA tour office will release daily updates that can be accessed by students, teachers, and the public via their World Wide Web site at *http://solstice.crest.org/nesea*. The NESEA also will be offering education packets and a speakers bureau for elementary and secondary teachers to help them design projects and lessons around the event. They also are encouraging schools to plan a field trip to the event and will be offering guided tours.

For more information on the NESEA American Tour de Sol, contact the NESEA at 50 Miles St., Greenfield, MA 01301; (413) 774-6051; fax (413) 774-6053.—*MS*

THE ENVELOPE, PLEASE

At a gala event sponsored by Ernst & Young and *Automotive News* magazine, five companies were honored with the Premier Automotive suppliers Contributions to Excellence award (PACE). Recognizing the importance of the awards ceremony, Michigan's Governor John Engler declared February 23 "Automotive Suppliers Day." The PACE program's mission is to recognize accomplishments occurring within the automotive supply chain.

The winner in the Small Supplier category is the Automotive Products Group of Gentex Corp., Zeeland, Mich. Gentex garnered the award by producing the Gentex Metal Reflector coating, which is used on the larger exterior mirrors of light trucks and sport utility vehicles. The Gentex Metal Reflector coating allows the vehicles to use electrochromic technology, increasing their safety value. The auto-dimming technology is still able to withstand the tough environmental stresses imposed on exterior mirrors.

In the Medium Supplier category, the two winners are the Spicer Transmission Div. of Dana Corp., Toledo, Ohio; and Bosch Automotive Systems Corp., Farmington Hills, Mich. Dana won for its development of an electronically-controlled truck transmission. The Auto Mate 2 works with Class 8 over-the-highway trucks to automatically shift the top two gears from the engine's management control system. Bosch won for using 25% post-consumer recycled material in the design of a dual fan-shroud assembly. In working with Wellman, Bosch developed their post-consumer nylon component from discarded carpeting from the equivalent of 1300 homes. Each part weighs just 4 lb.

The winner of the Large Supplier category is Prince Automotive Systems Div. of Johnson Controls, Plymouth, Mich. Prince's HomeLink radio transceiver received the award for providing a seamless transition between the user's car and home. The HomeLink transceiver is designed to protect car owners from remote control theft, and attack during the activation and deactivation of home security systems.

Finally, the Service Company category winner of the PACE awards is Rapid Design Services, Dayton, Ohio. Rapid Design Services won for its three information systems: The global CAD network, the financial network, and the human resource system. Their innovation in instituting volume discounts in engineering services was a new strategy, recognized by the PACE judges.

For more information, contact Ernst & Young, 500 Woodward Ave., Suite 1700, Detroit, MI 48226; (313) 596-7100; fax (313) 596-7101.—*DS*

INTERNET NEWS

Networks has joined with the na Internet Corporation) to design and implement na Wide Web (CWW). The primary target is businesses ing trade ties with other es in China and beyond.

The rst phase consists of servers in fi ties. CIC intends on adding five e cities to the network per quar with a target of 20 cities by 1998 e Phase One sites are: Beijing, ngzhou, Hong Kong, Shanghai, a henyang.

W he Hong Kong changeover and t igh-speed reform policy, Chin ready for its information netw The CWW features a bilingual interface, further opening access to an international, as well as national, audience.

The architecture of the system is based on Bay Networks' System 5000 Hubs, switching modules, routers, remote access servers, and the Optivity suite of network management solutions. The system is designed to be robust, scalable, and flexible in nature. Each of the Phase One sites will have high-speed switching modules that will allow the servers at each branch to trade site maintenance, backup, and management information. They will be interconnected via the company's high fault tolerance Backbone Concentrator Node routers.

Once the other sites link up to CWW, they will be joined via Bay Networks' Access Stack Node routers. These routers are lower in cost than the Backbone Concentrator Node models, but they still provide high fault tolerance and redundancy.

Contact Bay Networks Hong Kong Ltd., Suite 1510-1513, 15th Floor, City Plaza 4, 12 Taikoo Wan Rd., Hong Kong; (852) 2539-1288; fax (852) 2523-4028; Internet: http://www.baynetworks.com.

If you've been looking for an in depth study of the publishing that's been happening on the World Wide Web, check out the "Interactive Publications Review 1997" from Cowles/Simba Information.

This year's edition of the review analyzes 50 on-line publications including newspapers, magazines, and on-line-only publications.

The 50 publication profiles look at site traffic, advertising rates, editorial performance, site navigation, reader-staff interactivity, site format and content, economic models, subscriber base, and staff size. The review also rates the sites according to advertising, contact names, design, ease of use, interactivity, and their performance.

Contact Cowles/Simba Information, 11 Riverbend Dr. South, P.O. Box 4949, Stanford, CT 06907-0949; (203) 358-4384; fax (203) 358-5811; Internet: http://www.simbanet.com.

QUICK NEWS

In a move that further addresses the problem of controlling and monitoring the communication of the U.S. inmate population, Science Dynamics will be incorporating the Natural MicroSystems' Alliance Generation family of voice, call, and fax processing products into the Commander Plus inmate telephone system.

The Alliance Generation line is an assortment of full-function digital signal processing resource cards. The cards come with an integrated software environment suitable for developers to design systems with voice and call processing, speech recognition, faxing, switching, and integrating telephone systems and computer or database systems.

The cards can connect to daughterboards to expand the number of ports or add Natural Media extensions. Two of the available extensions are NaturalFax and NaturalRecognition.

Using digital signal processing, the Alliance Generation family integrates fax algorithms seamlessly with standard voice and call processing algorithms.

Commander Plus, the digital inmate telephone control and administration platform, was introduced last year. The system is designed to cut inmate fraud and annoyance calls by putting the call control in the hands of the correctional officers.

The current version of Commander Plus features a three-way call detection and termination software module, and an automated operator services software module. Future packages will have commissary/debit accounting, line concentration, concentrated recording and monitoring, and call-in-progress monitoring.

For more information on Commander Plus, contact Science Dynamics at **http://www.scidyn.com.**

Interested readers may contact Natural MicroSystems at 8 Erie Drive, Natick, MA 01760; (508) 650-1300; fax (508) 650-1352; Internet: http://www.nmss.com.

There's no dribbling going on at GLOBEtrotter Software, especially now that the U.S. Department of Commerce, Bureau of Export Administration has approved the company's FLEXcrypt data encryption technology for international use.

By using FLEXcrypt, software vendors can control their global distribution of products and avoid the costly and time-eating process of applying for individual export licenses. One licensee of the encryption tool is Sun Microsystems, using it to distribute its Solstice Management line.

FLEXcrypt's technique is based upon encrypting a set of files as a "secured package." After the set is encrypted, the vendor then ships a standard software distribution kit, complete with the files and a decryption program. The vendor has the option of sending the same decryption key to each end-user or an individual key to unlock the files.

Contact GLOBEtrotter Software, 300 Orchard City Dr., Suite 131, Campbell, CA 95008; (408) 370-2800; fax (408) 370-2884; e-mail: rich@globes.com.

Opening up new possibilities for price-conscious Ethernet LAN users, New Media Corp. has begun shipping their new value-priced, high performance LiveWire+ Ethernet LAN Adapter. The PC card proves throughput of up to 20 Mbyte/s in switched Ethernet networks.

Priced at $109.99 for 10BaseT and $129.99 for the 10BaseT/2 combination, the LiveWire+ gives mobile computer users who have the desire for speed a more viable option for their network connectivity.

One feature, Integrated Messaging, automatically alerts users, with helpful on-screen messages, the moment a problem has been detected. For example, Integrated Messaging informs users in the boot step, if their card is plugged in or if their network cable has become disconnected.

Using full-duplex architecture, the LiveWire+ enables notebook users to send and receive information simultaneously. Further boosting the speed, LiveWire+ incorporates Adaptive Self-Tuning technology. Self-tuning optimizes performance by examining the network's data patterns and automatically initiating the tuning process. It shifts buffer memory to transmit or receive network packets, depending upon the direction of network data.

Designed with New Media's Zero Consumption Advanced Power Management (APM) technology, LiveWire+ can be left in the slot without killing the battery. Typical PC cards can drain up to 25% of a laptop's power when not in use. The LiveWire+ automatically powers down the card, using zero battery power when not active.

The LiveWire+ is packaged with NewMedia's tool suite which includes Knowledge Bank, a database of technical information; CardSleuth, a general diagnostic utility program; and the aforementioned Integrated Messaging.

For further information, contact New Media Corp., 1 Technology, Building A, Irvine, CA 92618; (714) 453-0100; fax (714) 453-0114; Internet: http://www.newmediacorp.com.

Expanding its 900-MHz digital cordless phone family, Zilog has added a low-power 3.3-V chip set that offers cordless phone users the option of multiple handsets, with the possibility of a 14-handset capable base station. Wireless phones using the chip set with three standard battery cells provides over four hours of talk time and seven days of standby time.

Zilog uses spread-spectrum technology to increase phone range from several hundred feet to over a mile. This allows users to move about without losing the connection to the party they're calling.

For developers, Zilog provides the Z87L00 ZPhone development kit, which includes the chip set, an RF module, handset, and base-station boards. The reference design is of the turnkey variety, and is software-based, allowing simple customization. Both the Z87L00 controller and the Z87L10 audio encoder/decoder use a fast-adaption algorithm to avoid noisy channels and raise voice quality.

For more information, contact Zilog, 210 E. Hacienda Ave., Campbell, CA 95008; (408) 370-8000; fax (408) 370-8056; Internet: http://www.zilog.com.

A "Virtual" Face-To-Face Meeting

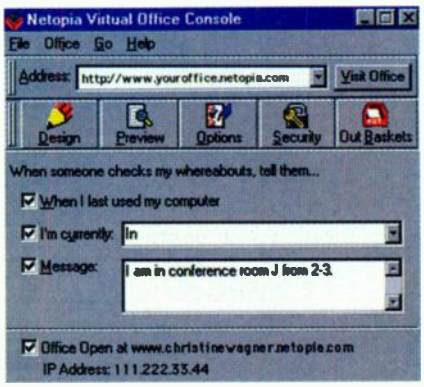
Is "phone tag" not on your list of favorite party games? Don't you hate walking to the other end of the office to consult with a co-worker and find that he or she is out, not leaving any word as to their whereabouts? A new software package has been introduced that will inform people of your schedule and whereabouts, and will eliminate that annoying phone tag game.

Netopia Virtual Office allows you to communicate and collaborate with anyone who has a Web browser. It transforms a PC into a collaborative Web office where you can work with others in real time and exchange information. Your own personal Web address gives visitors a way to meet you over the Internet or your corporate Intranet.

Virtual Office can be set up instantly. Anyone can visit your office from a browser using free plug-ins and ActiveX controls for collaboration. Don't worry—your resources are safe from unauthorized access.

Here's how it works: For someone to visit your Virtual Office, they first type in your Web address into their browser. They can view messages you've left regarding your schedule. At your office door, they can "knock" to see if you're there or ask to be notified upon your return.

The Virtual Office conference room allows true real-time collaboration over the Internet or Intranet. Visitors can be given permission to see what you're working on and share your mouse and keyboard to collaborate on projects or even run applications on your machine. And while you and your visitor are working, you can seamlessly communicate with both an intercom and keyboard. Virtual Office also integrates Microsoft NetMeeting for conducting multiuser conferences.

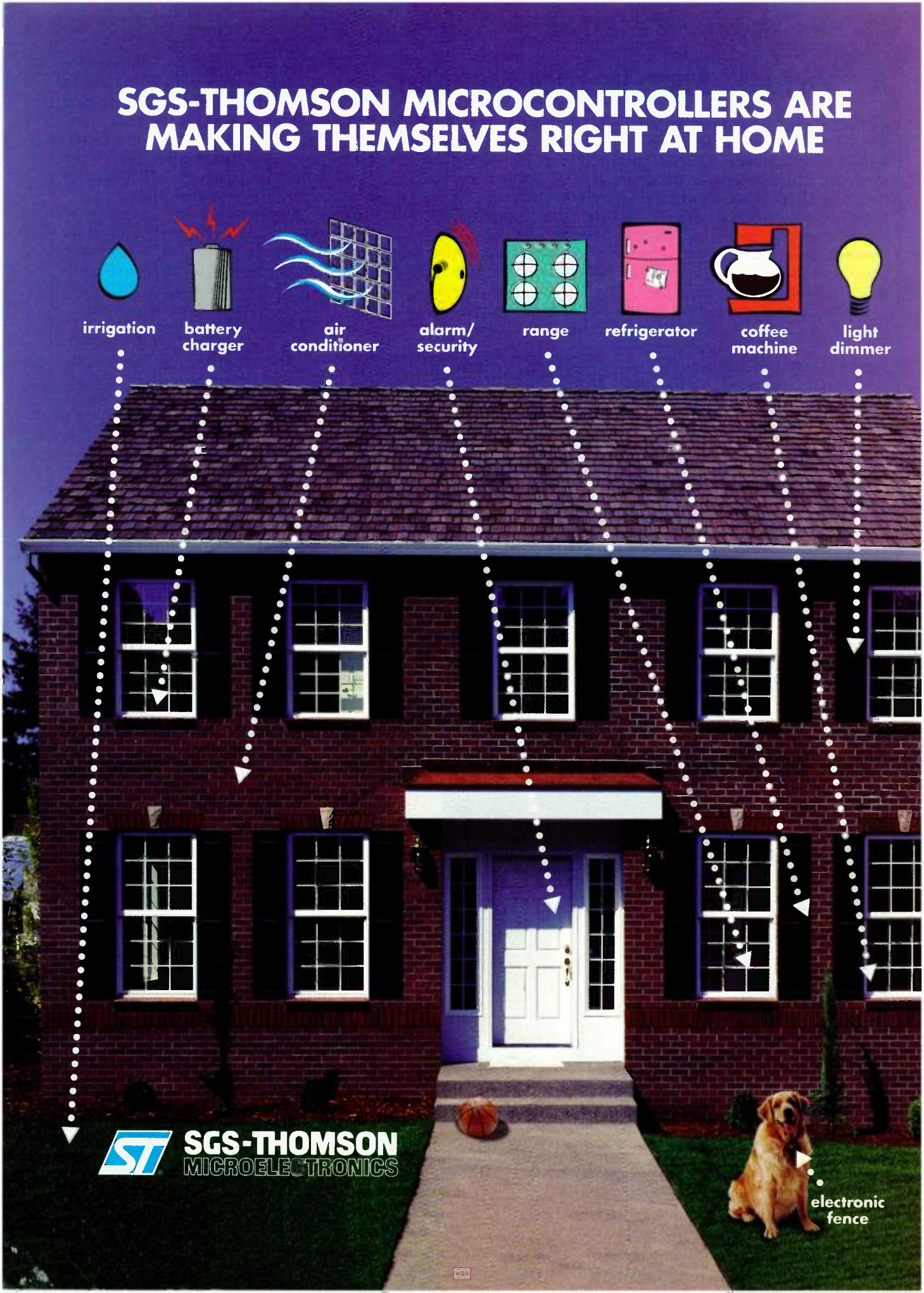


Public and private "Out Baskets" let you leave files and messages for others. An "In Basket" lets visitors drop-off files and documents, eliminating the hassles usually found with e-mail attachments over the Internet.

Virtual Office comes with a CD-ROM, Netopia Virtual Office Software, Microsoft Internet Explorer, Microsoft NetMeeting, and user's guide. System requirements are a 486 DX 66MHz processor, 8 Mbytes of RAM, a sound card,and Windows 95, 3.1, or Windows for Workgroups. Pricing is $49.95 electronically and $69.95 in a boxed version.

Contact Farallon Communications Inc., 2470 Mariner Square Loop, Alameda, CA 94501-1010; (510) 814-5000; fax (814) 814-5023; Internet: http://www.farallon.com.—*MS*

SGS-THOMSON MICROCONTROLLERS ARE MAKING THEMSELVES RIGHT AT HOME



LET OUR MICROS MAKE YOUR PRODUCT A HOUSEHOLD WORD

The reason SGS-THOMSON's 8-bit ST62 family of MCUs is making itself at home in so many household appliances can be summed up in one word: *Value.* ST62 devices deliver more performance in less space for less money. Even the core is optimized for cost-effective operation. Add ESD protection and unmatched noise immunity and you begin to understand why the ST62 is opening doors to consumer applications that remain closed to ordinary MCUs.

Additional ST62 MCU Applications

- washing machine
- power tool
- heater
- UPS
- thermostat
- scale
- programmable timer
- vacuum cleaner
- home bus

All ST62s contain ROM, RAM, an 8-bit timer with 7-bit programmable prescaler and multifunctional individually programmable I/O ports. Also available: Devices with high-current buffers to directly drive LEDs or TRIACs, along with a wide range of peripherals such as PWM and LCD drivers. A wide operating voltage range and robust design allow ST62 microprocessors to be powered directly from a battery or the main with minimum external components.

In addition to the extensive ST62 family, SGS-THOMSON offers other 8-32 bit micro solutions such as ST7, ST9, ST10 and ST20 families. All of these products are fully supported with extensive development tools including C compilers for most families. So why not let our micros help make your product a household word. To find out more fax 617-259-9442, write SGS-THOMSON, 55 Old Bedford Road, Lincoln, MA 01773, or e-mail: info@stm.com. And visit our web site at **http://www.st.com**

ST6
The 8-bit MCUs of choice in automotive and industrial as well as consumer applications. Instruction set and addressing modes maximize code efficiency.

ST7
Powerful industry standard 8-bit core, surrounded by numerous advanced peripherals. 3K to 48K of ROM with different RAM sizes. Choose EPROM and OTP versions for proto-typing. On-chip EEPROM is also available for integrated data storage.

ST9
8/16-bit micro family fills requirements of most advanced computer, consumer, telecom, industrial and automotive applications.

Service and Technology

For More Info Turn Page

READER SERVICE 171

OUR 8-BIT MICROS ARE BECOMING HOUSEHOLD WORDS

	DEVICE	PROGRAM MEMORY	RAM	EEPROM	A/D INPUTS	TIMERS	SERIAL INTERFACE	I/O's	PACKAGE	OTHER FEATURES
*	ST6200	1K ROM	64		4x8-Bit	1x8-Bit		9	DIP/SO16	LED or TRIAC driver
*	ST6201	2K ROM	64		4x8-Bit	1x8-Bit		9	DIP/SO16	
*	ST6203	1K ROM	64			1x8-Bit		9	DIP/SO16	
*	ST6208	1K ROM	64			1x8-Bit		12	DIP20/SO20	
*	ST6209	1K ROM	64		4x8-Bit	1x8-Bit		12	DIP20/SO20	
*	ST6210	2K ROM	64		8x8-Bit	1x8-Bit		12	DIP20/SO20	
*	ST6215	2K ROM	64		16x8-Bit	1x8-Bit		20	DIP28/SO28	
*	ST6220	4K ROM	64		8x8-Bit	1x8-Bit		12	DIP20/SO20	
*	ST6225	4K ROM	64		16x8-Bit	1x8-Bit		20	DIP28/SO28	
	ST6240	8K ROM	216	128	12x8-Bit	2x8-Bit	SPI	16	QFP80	LCD driver (segment) + LED or TRIAC driver, 32KHz oscillator
	ST6242	8K ROM	152		6x8-Bit	1x8-Bit	SPI	10	QFP64	
	ST6245	4K ROM	140	64	7x8-Bit	2x8-Bit	SPI	11	QFP52	
*	ST6253	2K ROM	128		7x8-Bit	2x8-Bit		13	DIP20/SO20	auto-reload timer + LED or TRIAC driver + PWM
*	ST6260	4K ROM	128	128	7x8-Bit	2x8-Bit	SPI	13	DIP20/SO20	
*	ST6263	2K ROM	128	64	7x8-Bit	2x8-Bit		13	DIP20/SO20	
*	ST6265	4K ROM	128	128	13x8-Bit	2x8-Bit	SPI	21	DIP28/SO28	
	ST6280	8K ROM	320	128	12x8-Bit	2x8-Bit	SPI, UART	22	QFP100	LCD driver (dot matrix) + auto-reload timer + LED or TRIAC driver
	ST6285	8K ROM	288		8x8-Bit	1x8-Bit	SPI, UART	12	QFP80	
	ST7291	8/16/24K ROM	256/384			1x16-Bit		19	DIP28/SO28	wake-up function + power saving & standby modes + power supply monitor
	ST7294	6K ROM	224	256		1x16-Bit		22	DIP28/SO28	wake-up function + power saving & standby modes + WDG
	ST9036	16K ROM	224+256		8x8-Bit	2x16-Bit	SPI+SCI	56	LCC68	WDG + handshake + Direct Memory Access
	ST9040	16K ROM	224+256	512	8x8-Bit	2x16-Bit	SPI+SCI	56	LCC68	
	ST90R50		224		8x8-Bit	3x16-Bit	SPI+2xSCI	56	LCC84	WDG + 2 handshakes + Direct Memory Access + 16 M Bit address
	ST90R52		224		8x5-Bit	3x16-Bit	SPI+2xSCI	52	QFP80	

Abbreviations:

ADC = Analog to Digital Converter
SCI = Serial Communications Interface
WDG = Watchdog
SPI = Serial Peripheral Interface
USART = Universal Synchronous/ AsynchronousReceiver/Transmitter

Packages:

DIP = Dual In Line
QFP = Quad Flat Pack
S = Shrink
LCC = Leaded Chip Carrier
SO = Small Outline

Also check out our new ST62 REALIZER

The ST62 REALIZER is a user-friendly tool that assists designers in developing applications based on the ST62 family. A graphical schematic description of the application is used to automatically generate the executable code for the ST62 and to run simulations for verification of the program function. The complete tool set runs under Microsoft WINDOWS® environment.

*More Gold Standard devices available from ST (OTP versions only)

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Complete product information at http://www.st.com

SGS-THOMSON MICROELECTRONICS

READER SERVICE 171

TRUDEL TO FORM

JOHN D. TRUDEL
CONTRIBUTING EDITOR

In addition to this column, I publish a free, but sporadically published, newsletter. For over a year, I have been using it to collect information about exactly what companies have been doing for New Product Innovation.

Unfortunately, the process was non-convergent. I am still working on it and will eventually put summary results up on my web page as well as into a future newsletter, but this year my new book *"Engines of Prosperity"* takes precedence.

Nevertheless, I can share the most amazing result, that, so far, there seems to be no pattern. The methods and structures that firms are using for new product innovation are random.

Some have no formal processes whatsoever, others have rigid processes, and some mix the two methods "somewhat" (whatever that means). Often, there is a certain tension reflected in the answers. For example, comments like "about 5% of our new products meet expectations" were not uncommon. Some sent in responses with the numbers blank, saying that my questions were "too direct in nature."

Some inputs seemed to come from a different universe. When a firm cites a new product success rate of over 95%, I wonder what exactly they are counting. It sounds more like engineering mods, repackaging, or cost reduction.

I expected diversity. I am a national examiner for Product Development Management Associations' national "Outstanding Corporate Innovator" (OCI) award. We select from the best of the best, and all the candidates have to exhibit robust processes that are linked to metrics and to results. Past OCI winners are diverse and their methods are dissimilar. Hewlett-Packard, is not like Eastman Kodak,or Marriott, or NordicTrack, or Fluke, or Nabisco, or Bausch and Lomb, or Pepsi-Cola, and so on.

But all the OCI winners were consistent in one area—they were all delivering excellent business results. All but one (Apple) were growing and prospering. My larger, random, self-selected, survey also was consistent, but in the opposite direction. With very few exceptions, the respondents cited flat sales or single digit growth rates. Such low growth in today's markets means share loss and relative decline.

My tentative conclusion has been that most firms are not very good at new product innovation. Further, it seems that the respondents and their CEOs don't much care, as they are focused on other things.

A recent visit to the booming Silicon Valley reinforced this. As never before, large companies are paying extreme prices to purchase small firms. Several friends have gotten very rich from this trend. One former client was bought for 40 times its sales. I am told that the average selling price for companies with any type of successful product, profitable or not, is now 12.3 times the firm's annual sales. That is astonishing.

Guess what? I think that an undiscussed result of dumb-sizing is to outsource New Product Development, even at almost any price. That is amusing to me, and I love it! Living well is the best revenge. Some of the engineers, managers, and professionals who were laid-off to save money are now getting wealthy.

Many companies seem to have lost the ability to fund, plan, and implement innovation. These firms have been hollowed out to the point where only a brand name and distribution channel is left, so they now desperately acquire products and hope for the best. Think of what a competitive advantage that offers to those who can innovate.

John D. Trudel, CMC, provides business development consulting and is author of "Engines of Prosperity." He is founder and director of The Trudel Group, 33470 Chinook Pl., Scappoose, OR 97056; (503) 640-5599; fax (503) 543-6361; e-mail: johntrudel@aol.com; Internet: http://members.aol.com/johntrudel.

OFF THE SHELF

"Digital Design and Modeling with VHDL and Synthesis" covers all the possible VHDL constructs and features, including design techniques and considerations. The book contains 115 complete working examples with 6200 lines of VHDL code; every line of VHDL code is analyzed and has an associated line number for easy reference. All code examples illustrate various constructs, features, practical design considerations, and techniques. The 368-page book is priced at $55. Contact the IEEE Computer Society Publications Office, Los Alamitos, CA 90720-1314.

"Pentium Pro Processor System Architecture" describes the hardware and software characteristics of the Pentium Pro Processor, the bus protocol it uses to communicate with the system, and the overall machine architecture. The book details the internal architecture of the processor, and provides insight into how it translates legacy x86 code into RISC instructions, executes them out-of-order, and then reassembles the result to match the original program flow. Other topics include the relationship of the Pentium Pro to other processors, PCI bridges, and memory; descriptions of the data, code, and L2 caches; transaction deferral, and performance monitoring and time stamping. The 556-page book is priced at $34.95. Contact Addison Wesley Longman, One Jacob Way, Reading, MA 01867; (617) 944-3700; Internet: http://www.aw.com.

"Client/Server Developer's Guide with Delphi" shows readers how to design efficient client/sever applications. The book demonstrates how to integrate Delphi with major databases like Interbase and Oracle, and includes sample programs, components, and advice on building client/server database applications. The 1000-page book is priced at $60. Contact Macmillan Computer Publishing USA, 201 W. 103rd St., Indianapolis, IN 46290; (317) 581-3500; fax (317) 581-3550.

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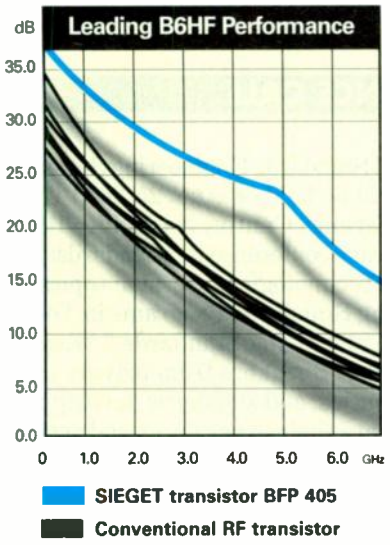
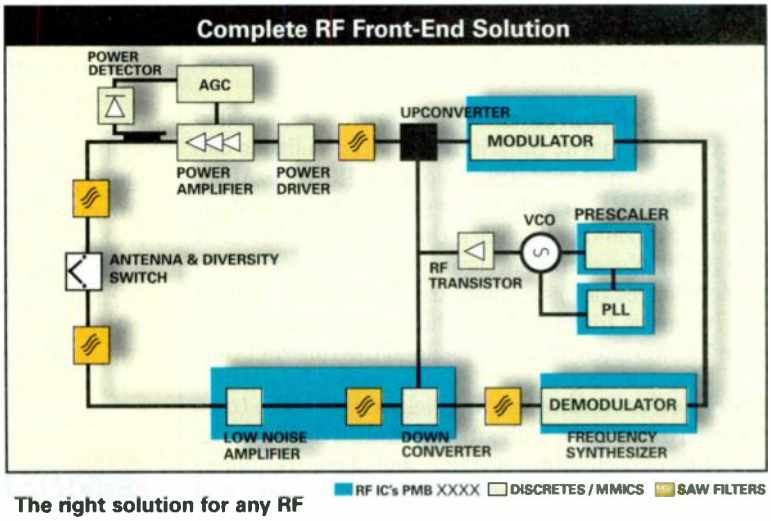


Astounding performance for a range of frequencies.

Our advanced SIEGET® (SIEmens Grounded Emitter Transistor) RF transistors combine bipolar technology and SMD packaging for performance levels with up to 25GHz transition frequency. This technology, combined with our CMOS, gives Siemens ICs the high level of integration, and our discretes the high gain, low noise and low power use you want for your ever-shrinking designs.



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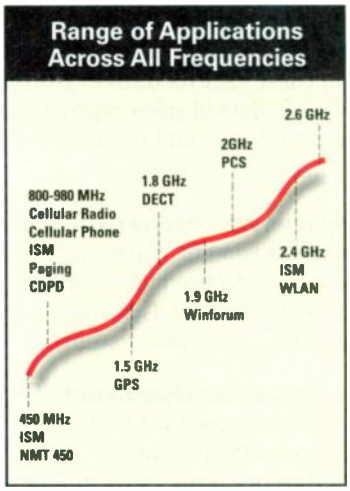
Your global partner raises local support to a new level.

Siemens supplies a world-wide array of customers, including some of the largest telecom companies in the U.S., Europe and Asia. Our international resources make it possible for us to meet your needs through a leading U.S. value-added distributor of wireless technology. And that translates directly into superior service and support for you — no matter where you are, or what your application.

As you begin your next generation of wireless products, talk to Siemens, the world leader in communications components.



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INTERNET ROLODEX

http://www.ashling.com: Wax your electronic surfboard at Ashling Microsystems' homepage. The site focuses on delivering specific information on embedded-microprocessor development and software quality assurance tools. Clicking on links will lead visitors to in-circuit emulators, source-level debuggers, software quality assurance systems, compilers and assemblers, integrated-development environments, development support for microprocessor manufacturers, and Smart Card development tools. Product data sheets also are available. Included are links to other microcontroller information sources, as well as reference information.

http://www.softsource.com: Web surfers have a distinct advantage here at SoftSource's site. Visitors can download Vdraft Internet Tools Version 1.3. The AutoCAD, DXF, and SVF drawing viewer and publisher runs under Windows 95 and NT, using either Microsoft Internet Explorer 3.0 or Netscape Navigator 2.0 or newer. Additionally, SoftSource offers a commercial version of Vdraft (comes with more features), available for licensing. To date, over 100,000 sites have downloaded the Internet tool.

http://www.foxonline.com: Click on this URL to go to Fox Electronics' new web site. Technical data for the company's line of oscillators, crystals, and other frequency control products can be found here. Designers will find that the homepage is sectioned off into 12 different compartments. They include real-time clock modules, monolithic crystal filters, and TCXOs/VCXOs. For novice visitors, Fox also has included a glossary of technical terms. Details on the FastFox delivery program can be found here, as well as lists of sales representatives and distributors, company facts, and quote requests and e-mail response forms.

http://www.warnernet.com: Visit the Linear and Electronics Division of Warner Electric for the latest on their motion control products. The new site features products such as SLO-SYN DC Step and synchronous motors, motion controls, and servo systems.

http://www.embedded.com: Keeping an ear to the pavement about embedded systems? Check out the "Embedded Systems Programming" magazine web site. Engineers will find breaking news and new product information, complete with editorial analysis; a code download area; Miller Freeman Directories; conference listings, buyer's guides, and a job center. The Miller Freeman Directories comprise 17 on-line directories with extensive product information on microcontroller architectures and the hardware and software tools that support them.

http://www.accumet.com: Drop into Accumet Engineering Corp.'s site for tough-to-find technical information on precision substrates fabricated to fine tolerances. Listed are specifications such as standard surface finish, camber, and CTE of 96% Alumina, 99.5% Beryllium Oxide, and Fused Silica. Ceramic fabrication questions can be posed and answered at the site.

FREE STUFF

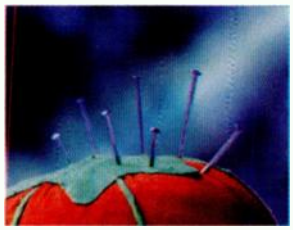
TRA-CON Inc., an international supplier of epoxy adhesives for fiber-optic, laser, electronics, aerospace, medical instrumentation, and industrial applications, provides free product samples on request. Adhesives can be provided in either 1-g MINIPAX, 2-g or larger BIPAX, or pre-mixed and frozen in syringes. Larger packages can be arranged for higher volume testing. For more information, contact TRA-CON Inc., 45 Wiggins Ave., Bedford, MA 01730; (800) TRA-CON1; fax (617) 275-9249.

Interconnect Devices Inc. (IDI) has released the fourth edition of its "Catalog and Source Book" which provides all the information necessary to find all probes and receptacles to fit any specific applications. The catalog offers an assortment of options in sizes, tip styles, spring forces, and platings. The source book contains technical references for issues related to probing, such as applications, fixturing, cleaning, and electrical performance. To obtain a free copy of the catalog and source book, contact IDI, 5101 Richland Ave., Kansas City, KS 66106; (913) 342-7043; fax (913) 342-5544.

CONFERENCE CALL

The 46th annual Standards Engineering Society (SES) conference will be held on Aug. 25-26 at Opryland Hotel and Conference Center, Nashville, Tenn. The theme for this year's conference is "Standards: New Directions—New Technologies." Session topics will include "Promoting Standards Programs in Your Company," "Finding and Using Standards," "Regulatory Use of Standards." Speakers from private industry, government agencies, and standards developing organizations will share their experiences and activities in these areas. For more information, contact Donald Kear, Executive Director, SES, 1706 Darst Ave., Dayton, OH 45403-3104; (937) 258-1955; fax (937) 258-0018; e-mail: dlkgen@aol.com.

The Magnetic Materials Producers Association (MMPA) Conference will be held Sept. 22-23 at the Hyatt Regency O'Hare Hotel, Rosemont, Ill. The conference is being held in conjunction with the EIC/EMCW Expo '97 (Coil Winding Show) which is being featured at the Rosemont Convention Center. The focus of the MMPA Conference is the Permanent Magnet Seminar, which will cover the basics of permanent magnets, materials, design examples, and environmental considerations; and the Soft Ferrite Seminar, which will provide interactive sessions on current and future ferrite core materials. The fee for the conference, including one continental breakfast, two lunches, and a buffet dinner is $495. For more information, contact MMPA, 8 S. Michigan Ave., Suite 1000, Chicago, IL 60603; (312) 456-5590; fax (312) 580-0165.



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ON THE HEAD OF A PIN?

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RF/MICROWAVE DISTRIBUTION
AN AVNET COMPANY

YOUR RF DESIGN TEAM

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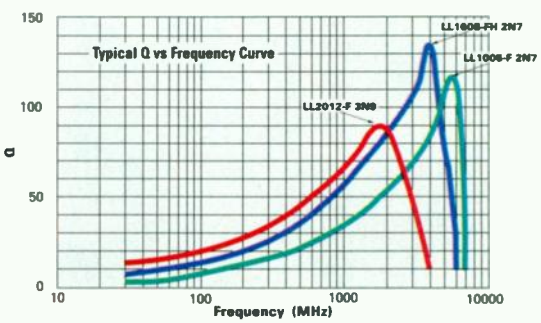

Toko LL Prototyping Kits Available

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LL1608-F, LL1608-FH
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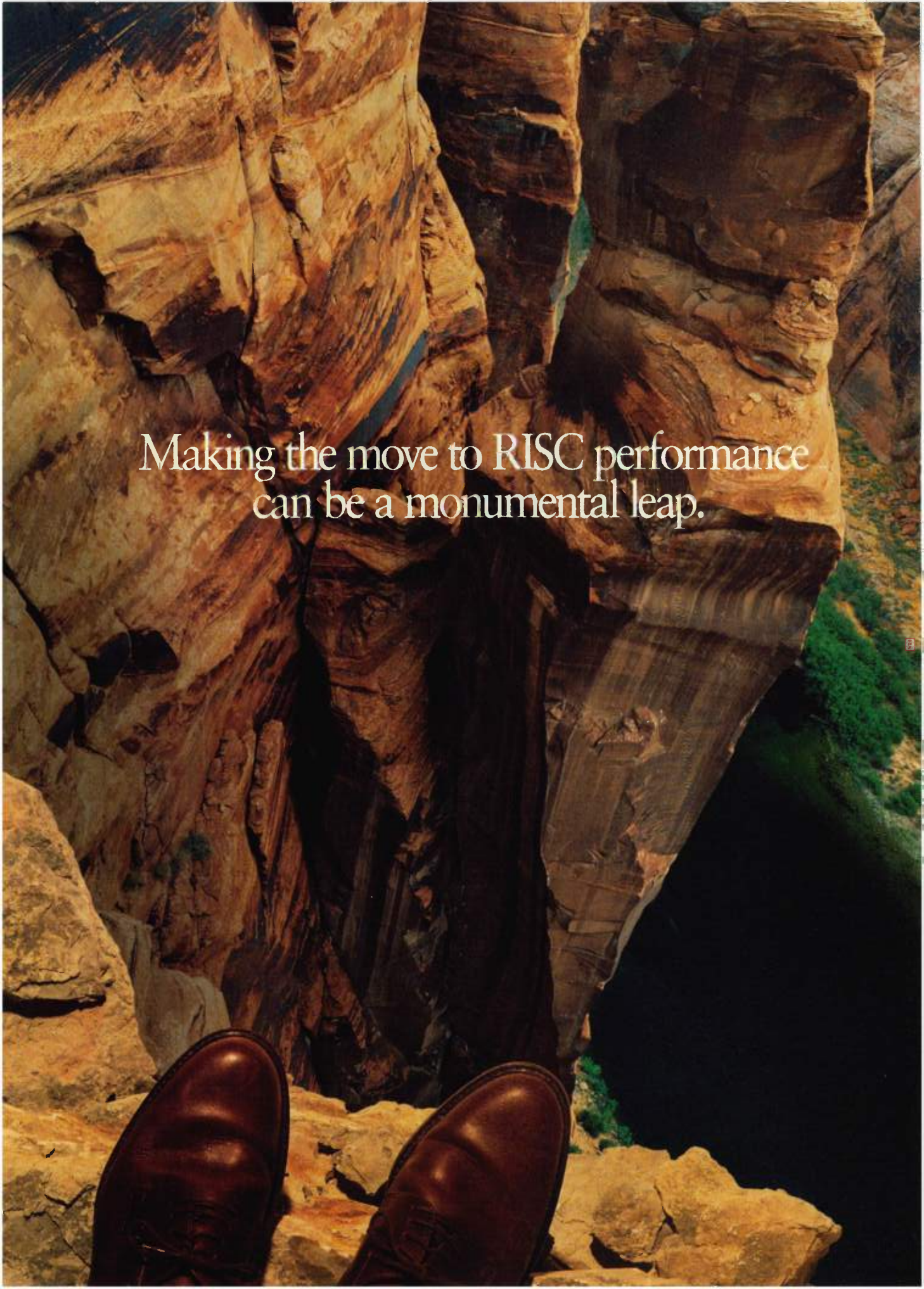
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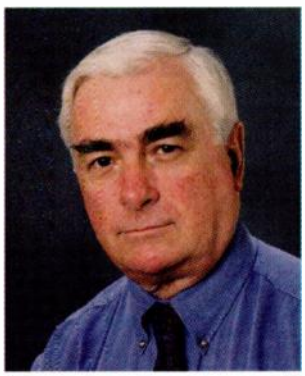
LETTERS FROM LONDON

Antique Radio Roadshow

During the 34 years I've been writing about the electronics industry, I've collected—accumulated might be a better word—quite an assortment of electronic bits and pieces.

One of these oddities is a section of circular waveguide. In the early 1970s this waveguide was going to form the high-capacity trunk telecommunications backbone of the United Kingdom, but was superceded by optical fiber before it was laid down. Additionally, I have in my possession early digital watches, calculators, a Transputer chip, and a handful of components that had been considered the most advanced technology of their time.



PETER FLETCHER
FIELD CORRESPONDENT

Around 20 years ago, I dubbed this collection "The Society for the Preservation of Electro-Technical Antiquities." It soon became an in-joke among many of my colleagues in the electronics press.

But now, the radio and electronics industry has passed its centenary year, and it really is old enough to have generated genuine antiques of sufficient value to take their place in the fine art auction rooms of London.

On April 24 and 25, Christie's of South Kensington will auction off the archives of the Marconi Company. The archives are described by the auctioneers as a "unique collection that charts the history of radio from the arrival of Guglielmo Marconi in England, in 1896, through to the end of World War II." This time period spans the first 50 years of electronics as we know it.

The two-day sale at the legendary auction house is expected to fetch more than $1.6 million. Goods to be sold feature antique electronic artifacts valued at prices ranging from $160 to more than $15,000.

Highlights of the sale include what Christie's describes as "some of the earliest recorded wireless messages" transmitted in 1897 and 1898. These messages include what Marconi claimed to be the first ever "wireless telegraph" messages communicated from poet Lord Tennyson and researcher Lord Kelvin, and a famous message from Queen Victoria inviting her son, the Prince of Wales, to tea on her yacht.

Marconi's personal diary from 1901 is expected to garner approximately $2000, while the headphones on which he heard his first transatlantic transmission, could grab up to $10,000. A letter from Dr Ambrose Fleming to Marconi, in which he describes his invention of the thermionic tube—including what may be the electronics industry's greatest understatement—"I have not mentioned this to anyone as it may become very useful"—also will be on the auction block. Additionally, a collection of some of Fleming's early tubes (we call them "valves" in the U.K.) will accompany the letter. Be prepared to write out a hefty check for these items.

Other memorabilia and hardware coming under the hammer include the microphone used by opera star Dame Nellie Melba to make one of the first public entertainment broadcasts in November 1920 from Marconi's first private radio station in Chelmsford, Essex. Attendees of the auction will be able to view and bid on the designers model of the antenna used for regular high-definition television broadcasts by the British Broadcasting Corporation in 1936.

Viewing for the sale will take place from Saturday, April 19 through to Wednesday, April 23. But before then, some of the items will be sent on a tour of the United States and Italy. More information can be obtained by visiting Christie's World Wide Web site at http://www.christies.com/marconi.

Peter Fletcher is Electronic Design's U.K. correspondent. He can be contacted via his e-mail address at panflet@cix.compulink.co.uk.

BACK TO SCHOOL

"Information Technology and Telecommunications: Designing for Compliance to UL 1950" is a seminar that will be held May 13-14 in Chicago, Ill., July 16-17 in Camas, Wash., and Oct. 14-15 in Orlando, Fla. Sponsored by Underwriters Laboratories Inc. (UL), the seminar explains key requirements for the new U.S. and Canadian binational Standard for ITE and Telecommunications equipment and how to evaluate products to comply to the new standard. Participants will review new requirements that apply to information technology equipment; generate diagrams to determine and measure compliance with insulation requirements; and identify the hazards that affect enclosure design. Contact UL, 333 Pfingsten Rd., Northbrook, IL 60062-2906; (847) 272-8800.

"Supporting and Troubleshooting Windows 95" is a two-day demonstration/hands-on seminar that examines each layer of Windows 95. It looks at the new memory model, multitasking abilities, and network support capabilities. Attendees will learn to diagnose and repair all types of Windows 95 problems. Techniques for managing the new desktop and registry will be discussed, along with network security maintenance through authentication and proactive troubleshooting. Contact Data-Tech Institute, P.O. Box 2429, Clifton, NJ 07015; (201) 478-5400; fax (201) 478-4418; Internet: http://www.datatech.com.

P.S. Write Back Soon!

How often do you find yourself wishing you had commented about something you had seen in *Electronic Design*? Often? Sometimes? Not at all? What's *Electronic Design*? We don't want our readers to feel that they can't come to us and share their feelings. So, get honest and tell us what you really think, and e-mail us: Mike Sciannamea at **mikemea@class.org,** or Deb Schiff at **debras@csnet.net.** Snail mail commentary should be sent to: QuickLook, *Electronic Design*, 611 Route 46 West, Hasbrouck Heights, NJ 07604. Our fax number is (201) 393-0204.

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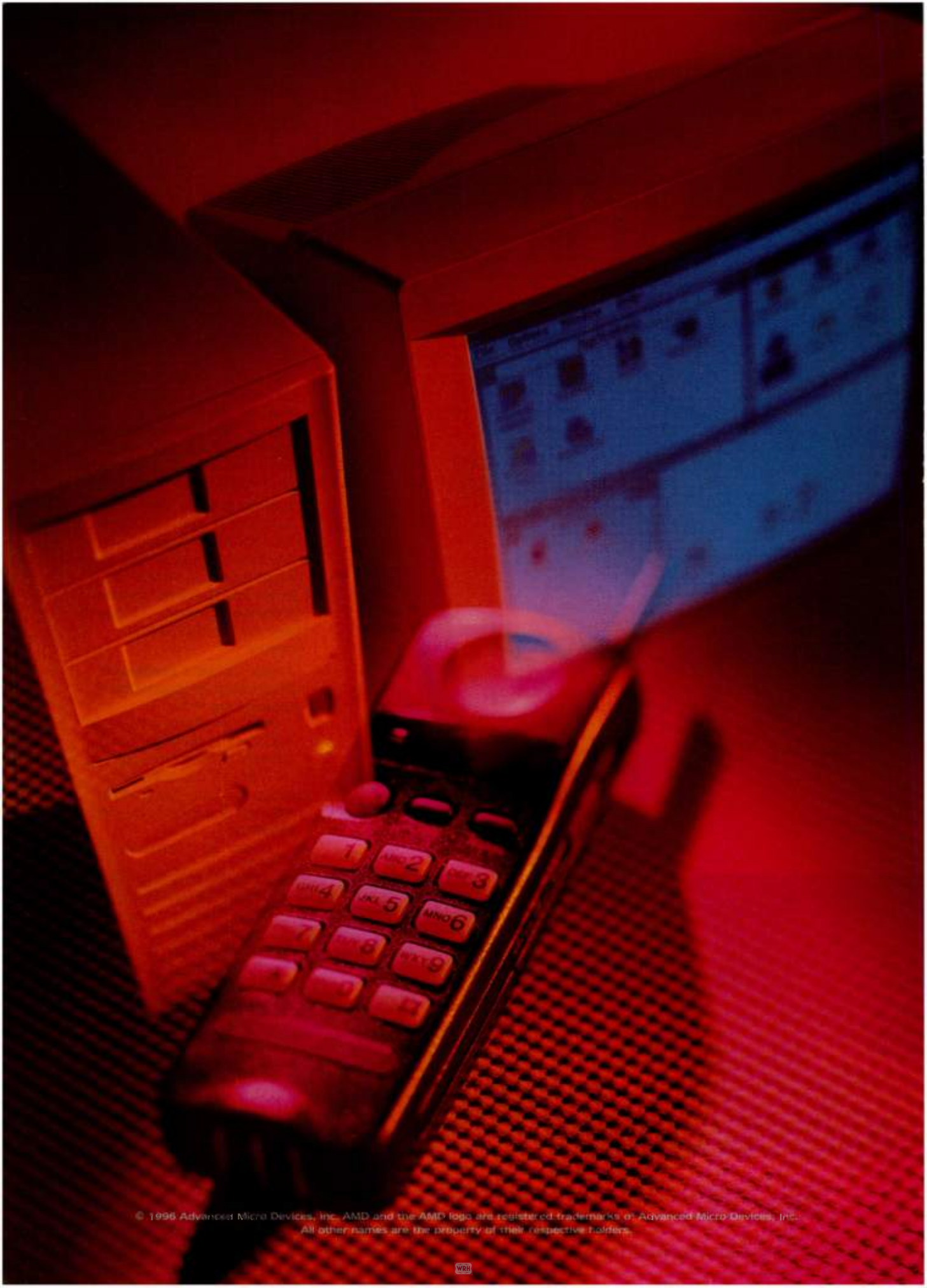

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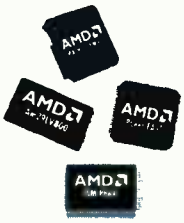

Half of the silicon we make this year will include linecard ICs, Ethernet controllers and repeaters, programmable logic devices, flash and EPROM memory, and embedded processors.

Magic Packet® technology gives the new HP Vectra XM the power to lower network administration and maintenance costs. Now a network manager can remotely wake-up a PC in sleep mode and remotely power-up a PC that has been powered down.

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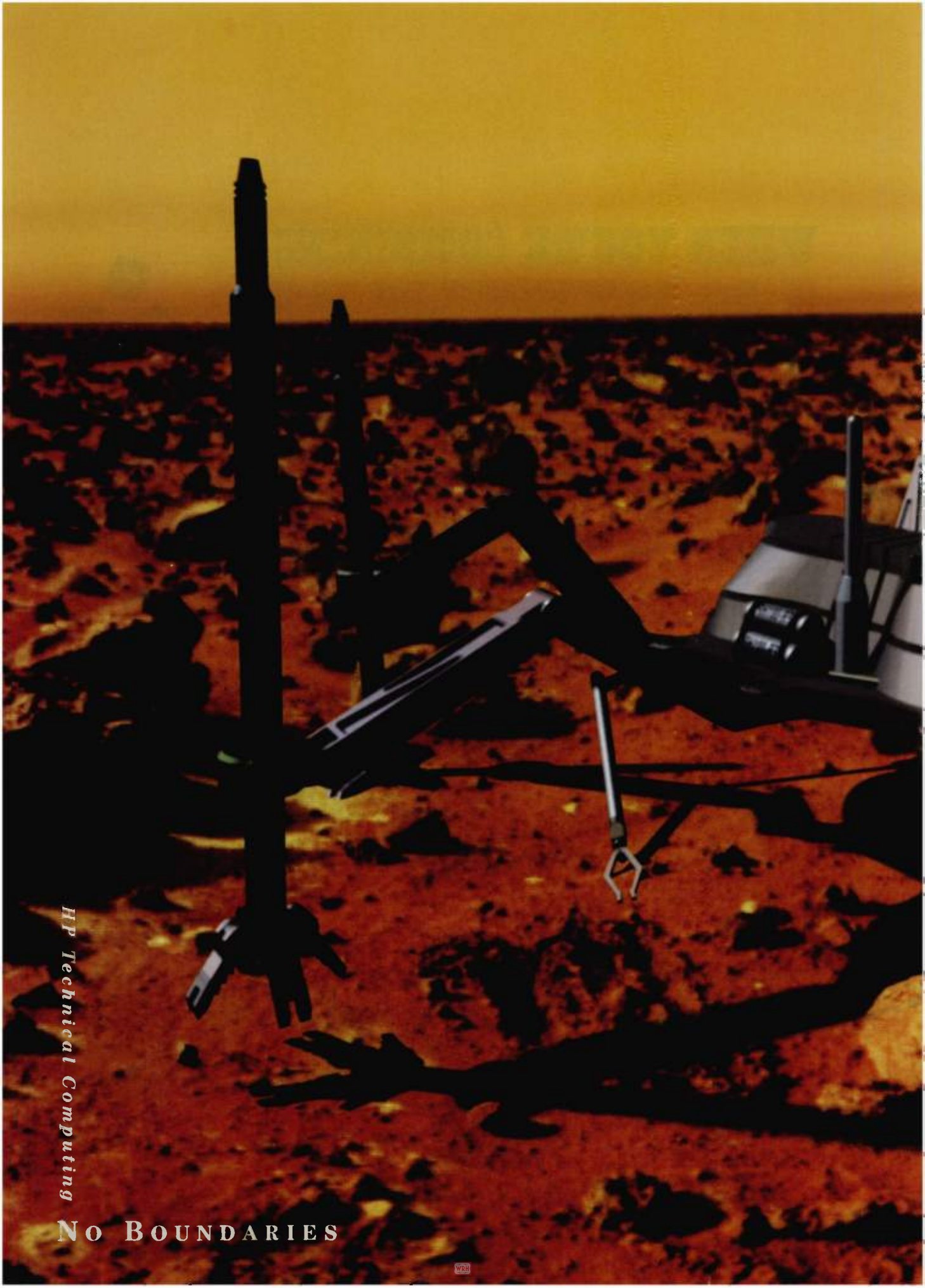
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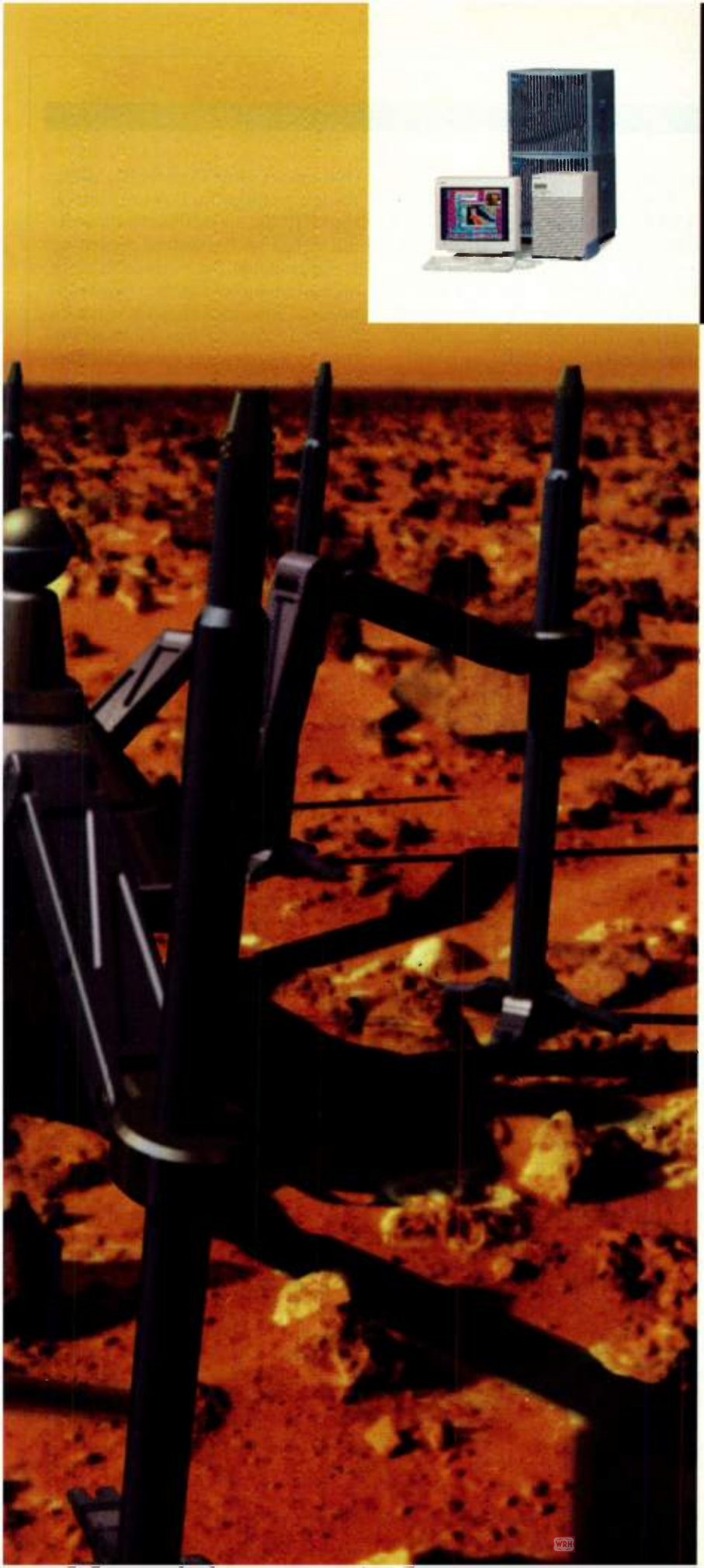

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HOT PC PRODUCTS

The Yamaha CDR400c is a CD recorder that supports the company's RapidLinked high-performance variable and fixed packet writing software. It is capable at writing at four times the typical speed of CD recorders, and reads at six times the typical speed.

Jumping on the bandwagon to eliminate buffer underrun, the CDR400 holds 2 Mbytes in its data buffer.

Because fixed packet writing, with its premastering process, is still required to write music or multimedia files to CD, Yamaha's RapidLinked packet writing software features both fixed and variable styles. Variable packet writing, the new kid on the block in CD-recording technology, gives the user true floppy disk ease of use, especially in backup applications. The future for variable packet writing lies in streaming Internet data directly to CD, long-term storage, and large file storage.

Yamaha also built in SCSI and ATAPI interface options in the CDR400c. These two widely accepted interfaces make it possible for trading information via CD.

Targeted toward OEMs and software and hardware integrators alike for its flash ROM capability, the new CD recorder allows simple downloading of firmware upgrades to further the development process.

To deal with difficulties caused by noise, shudder, and stability, Yamaha has installed tray, as well as caddy loading, for the recorder.

The CDR400 features five different session modes: session-at-once, packet writing, disc-at-once, track-at-once, and multisession.

The new recorder supports seven standard formats: CD-digital audio, CD-Extra, CD-I, CD-ROM, CD-ROMXA (in both photo CD and video CD), and Video CD.

Another feature is the Running Optimum Power Control. By using Running Optimum Power Control, the CDR400 maintains media writing integrity. Error-free recording is controlled in the recorder's write operation automatically. This technology allows more brands of media to be supported, thus allowing the user to choose their own cost-effective solution.

All major platforms including UNIX, Windows, and Amiga are supported. Earlier editions of Yamaha's CD recorders have been supported by 25 software developers with 50 different applications.

Pricing for the Yamaha CDR400c, 4x/6x internal caddy or tray units start at $749. The CDR400tx, 4x/6x external tray unit starts at $849.

Contact Yamaha Systems Technology Inc., 100 Century Center Ct., San Jose, CA 95112; (408) 467-2300; fax (408) 437-8791; Internet: http://www.yamaha.com.

In a deal struck with Apple Computer, Asanté Technologies has designed and developed the Mini PCI Network/Modem for the Apple PowerBook 3400. The new modem card will be built into most PowerBook 3400 configurations, and comes with Asanté's network acceleration software.

NetDoubler accelerates both Ethernet and Fast Ethernet networks. The software boosts the speed of copies, as well as the opening and saving of large files across networks. According to the company, NetDoubler speeds network file functions by a factor of nine. Winning the Macworld World Class Award for best networking product, NetDoubler is known as an industry standard in Macintosh environments.

Currently, the Mini PCI card is the smallest plug-in Ethernet/modem card in the Macintosh notebook market. The card uses a 33.6 kbits/s modem for data and voice communication, and combines this capability with 10BASE-T Ethernet. Users can dial out with the modem, using the Ethernet connection at the same time, without experiencing a drop in performance.

In a power-saving vein, by using the PCI technology built into the PowerBook, the Mini PCI Network/Modem prevents drain on the CPU.

The card is available at a price of $495 list, $399 street. Apple service providers will install the the Mini PCI card in PowerBooks without built-in Ethernet/modem capabilities.

Contact Asanté, 821 Fox Lane, San Jose, CA 95131; (408) 435-8388; fax (408) 432-7511, Internet: http://www.asante.com.

It may look like an Orwellian refrigerator, but the Proline modular PC enclosure is designed to protect commercial-grade PCs from harsh industrial manufacturing environments.

The result of a partnership between Hoffman Engineering and Schroff GmbH, the Proline modular enclosure allows PCs to be used in areas that would normally call for very expensive industrially-hardened computers. The modular enclosure uses UL/NEMA Type 12 protection to ensure that the PC will be protected in harsh environments. Proline features a pull-out keyboard tray that allows workers to use the PC without exposing the monitor or CPU to contamination.

Built with 12 ga. steel roll-formed members with six bends for superior stability, Proline modular enclosures can accommodate very large monitors or additional components. The frame members are welded to a solid steel corner block, further reinforcing protection of the computer. Featuring tempered safety glass, the large window door on top resists scratches for clear viewing and easy cleaning.

For more information, contact Hoffman Engineering, 900 Ehlen Dr., Anoka, MN 55303-7504; (612) 421-2240; fax (612) 422-2178.

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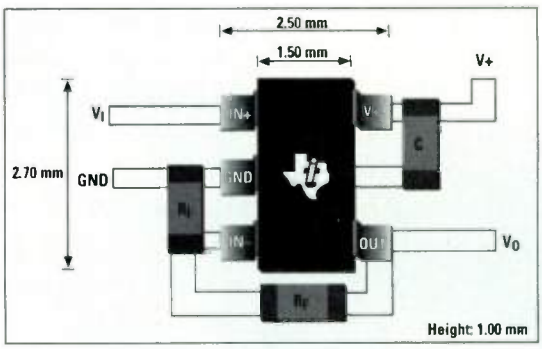
	typ	max	typ	typ	typ	max	max
TLV2211	11	25	56	.025	22	3	.015–2.94
TLV2221	100	150	480	.18	20	3	.015–2.97
TLV2231	750	1000	1900	1.25	16	3	.010–2.87

	V_{DD} = 5 V						
	I_{DD} (μA)		BW (kHz)	SR (V/μs)	V_N (nV/√Hz)	V_{IO} (mV)	V_O (V)
	typ	max	typ	typ	typ	max	max
TLV2211	13	25	65	.025	18	3	.012–4.95
TLV2221	110	150	510	.18	19	3	.012–4.88
TLV2231	850	1200	2000	1.6	15	3	.080–4.90



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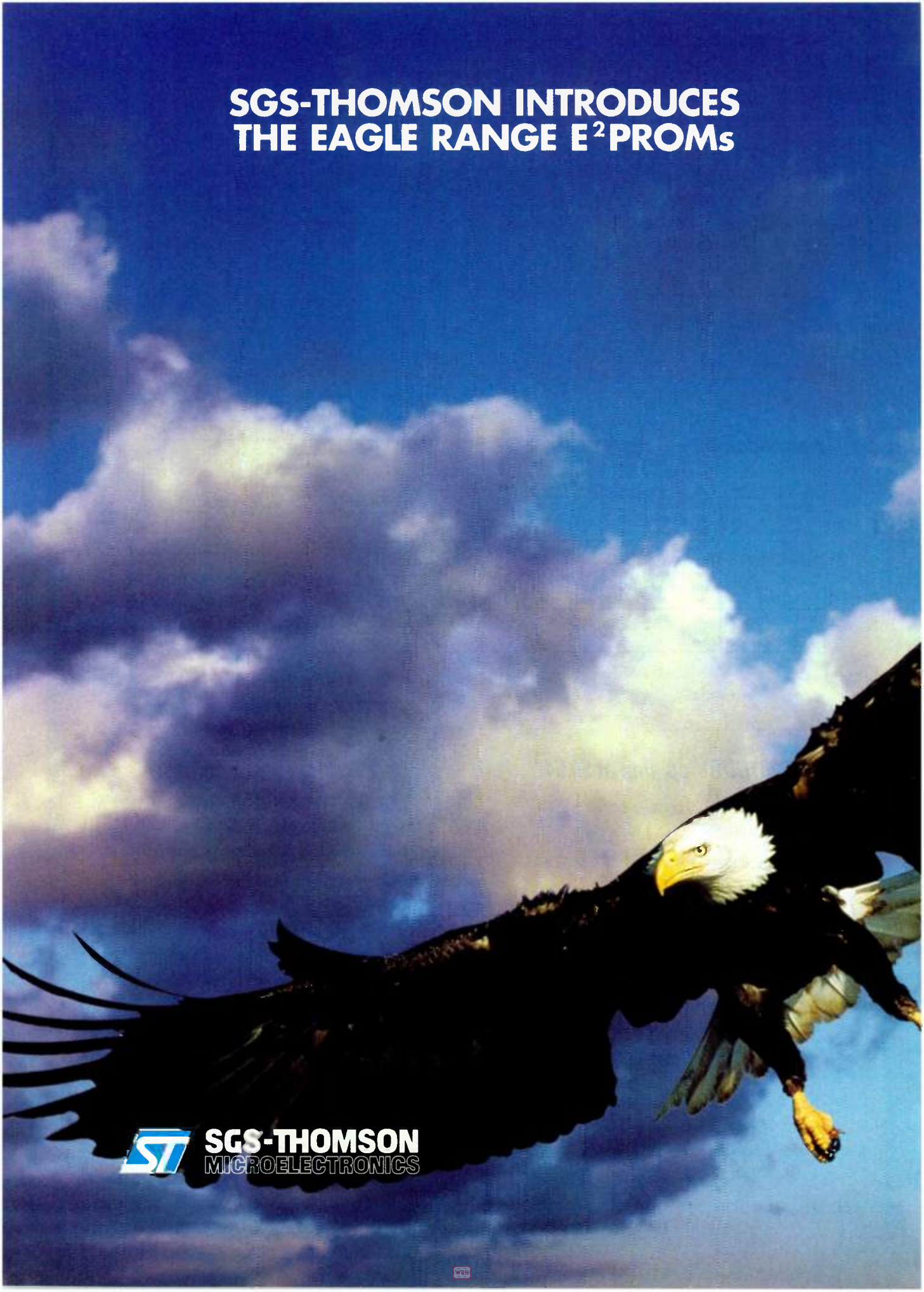

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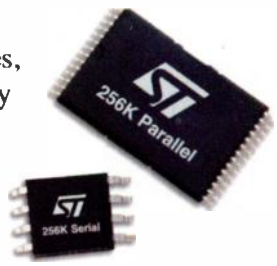

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I²C		ST24C01 ST24W01 M2201* ST24LC21*	ST24C02 ST24W02 M34C02*	ST24C04 ST24W04	ST24C08 ST24W08	ST24C16 ST24W16 ST24164*				
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SPI		ST95010 ST95011	ST95020 ST95021	ST95040 ST95041	ST95P08	*1H97* M95160 M95161	*1H97* M95320 M95321	*Q197* M95640 M95641	*1H97* M95280 M95281	*Q197* M95560 M95561
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- SOFTWARE DATA PROTECTION

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OCTOBER

Sixth IEEE International Conference on Universal Personal Communications, October 12-16. Hotel del Coronado, San Diego, California. Contact Gail Weisman, IEEE Communications Society, 345 East 47th Street, New York, New York 10017; (212) 705-7018; fax (212) 705-7865; e-mail: g.weisman@ieee.org.

Sixth IEEE International Conference on Universal Personal Communications (ICUPC '97), Oct. 13-15. Contact Tony Acampora, MC 0409, Bldg EBU1, UCSD, 9500 Gilman Dr., La Jolla, CA 92093-0409; (619) 534-5438; (fax) (619) 534-2486; e-mail: acampora@ece.ucsd.edu.

Conference on Domain-Specific Languages (DSL), October 15-17. Red Lion Resort, Santa Barbara, California. Contact USENIX Conference Office, 22672 Lambert Street, Suite 613, Lake Forest, California 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

ICSPAT/DSP World 1997, Oct. 15-17. San Diego Convention Center, San Diego, CA. Contact Denise Chan, Miller Freeman Inc. (415) 278-5231; e-mail: dsp@exporeg.com.

IEEE Holm Conference on Electrical Contacts, October 18-22. Wyndham Franklyn Plaza, Philadelphia, Pennsylvania. Contact Wendy Rochelle, IEEE Conference Services, 445 Hoes Ln., P.O. Box 1331, Piscataway, New Jersey 08855-1331; (908) 562-3870; fax (908) 981-1769; e-mail: w.rochelle@ieee.org.

IEEE Telecommunications Energy Conference (INTELEC '97), Oct. 19-23. World Congress Centre, Melbourne, Australia. Contact Robert N.K. Thuan, Network Products-Telstra Corp. Level 14, 242 Exhibition St., Melbourne, Victoria 3000, Australia; (61) 3 634 6216; fax (61) 3 632 3607

Sensors Expo, Oct. 21-23. Cobo Convention Center; Detroit, MI. Contact Expocon Management Associates Inc., (203) 256-4700; e-mail: sensors@expocon.com; Internet: http://www.expocon.com.

Fourth IEEE International Conference on Image Processing (ICIP '97), Oct. 26-30. Fess Parker's Red Lion Resort, Santa Barbara, CA. Contact Sanjit K. Mitrea, Electrical & Computer Engineering, University of California, Santa Barbara, CA 93106-9560; (805) 893-3957; fax (805) 893-893-3262; e-mail: mitra@ece.ucsb.edu.

11th Systems Administration Conference (LISA '97), Oct. 26-31. Town & Country Hotel, San Diego, CA. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

19th Annual International Conference of the IEEE Engineering in Medicine & Biology Society, Oct. 29-Nov. 2. Sally Chapman, Secretariat, National Res. Council of Canada, Bldg. M-55 Rm. 393, Ottawa, KIA OR8, Canada; (613) 993-4005; fax (613) 954-2216.

19th International Conference of the IEEE Engineering in Medicine & Biology Society, Oct. 30-Nov. 2. Chicago Marriott Downtown, Chicago, IL. Contact Meeting Management, 2603 Main St., Suite 690, Irvine, CA 92714; (714) 752-8205; fax (714) 752-7444; e-mail: embs97@ieee.org; Internet: http://www.eecs.uic.edu/-embs97.

NOVEMBER

IEEE International Test Conference (ITC), Nov. 1-5. Sheraton Washington Hotel, Washington, DC. Contact ITC, 655 15th St., N.W., Suite 300, Washington, DC. 20005; (202) 639-4164; fax (202) 347-6109.

IEEE Global Telecommunications Conference (GLOBECOM '97), Nov. 3-7. Phoenix, AZ. Contact Nigel Reynolds, 15436 N. First Ave., Phoenix, AZ 85023; (602) 942-5583; fax (602) 942-4542; e-mail: nigelaz@aol.com.

WESCON '97, Nov. 4-6. San Jose Convention Center and Santa Clara Convention Center, San Jose and Santa Clara, CA. Contact Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045-3194; (800) 877-2668; fax (310) 641-5117; e-mail: wescon@ieee.org.

IEEE Intelligent Transportation Systems Conference (ITS '97), Nov. 9-12. Boston Park Plaza Hotel, Boston, MA. Contact Richard Sparks, 8 Richard Rd., Bedford, MA 01730; (617) 862-3000; fax (617) 863-0586; e-mail: r.sparks@ieee.org.

23rd Annual Conference of IEEE Industrial Electronics (IECON '97), Nov. 9-14. Hyatt Regency Hotel, New Orleans, LA. Contact Michael Greene, 200 Broun Hall, Electrical Engineering, Auburn University, Auburn, AL 36849-5201; (334) 844-1828; e-mail: greene@eng.auburn.edu.

Asian Test Symposium, Nov. 17-19. Akita, Japan. Contact Y. Takamatsu, (81) 89 927-9955; e-mail: takamatsu@cs.ehime-u.ac.jp.

DECEMBER

36th IEEE Conference on Decision & Control, Dec. 8-12. Hyatt Regency, San Diego, CA. Contact Ted E. Djaferis, Department of Electrical & Computer Engineering, University of Massachusetts, Amherst, MA 01003; (413) 545-3561; fax (413) 545-1993; e-mail: djaferis@ecs.umass.edu.

Workshop on Internet Technology & Systems (WITS), Dec. 9-12. Marriott Hotel, Monterey, CA. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

JANUARY 1998

Annual Reliability & Maintainability Symposium/Product Quality & Integrity (RAMS), Jan. 20-22. Anaheim Marriott, Anaheim, CA. Contact V.R. Monshaw, Consulting Services, 1768 Lark Lane, Cherry Hill, NJ 08003; (609) 428-2342.

Seventh Security Symposium, January 26-29. Marriott Hotel, San Antonio, Texas. Contact USENIX Conference Office, 22672 Lambert Street, Suite 613, Lake Forest, California 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

SIEMENS

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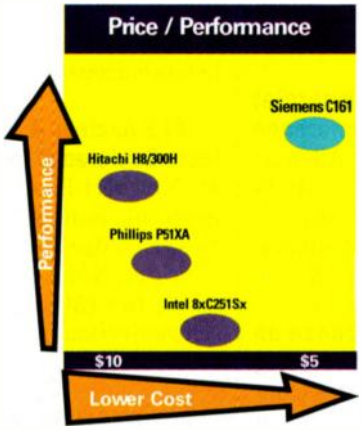

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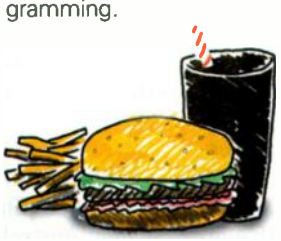
If you find upgraded 8-bit products pretty hard to swallow, Siemens has a treat for you — the new C161 microcontrollers in stock today. All are based on the C166 core with RISC-like architecture, with an instruction set and optimizing compilers designed for easy C programming.



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Marshall

IT'S ABOUT TIME

JANUARY 1998

IEEE Power Engineering Society Winter Meeting, Jan. 31-Feb. 5. Tampa, FL. Contact Jim Howard, Tampa Electric Co., P.O. Box 111, Tampa, FL 33601; (813) 228-4653; fax (813) 228-1333; e-mail: j.howard@ieee.org.

FEBRUARY

IEEE International Solid-State Circuits Conference (ISSCC '98), Feb. 5-7. San Francisco Marriott, San Francisco, CA. Contact Diane Suiters, Courtesy Associates, 655 15th St. N.W., Washington, DC 20005; (202) 639-4255; fax (202) 347-6109; e-mail: isscc@courtesyassoc.com.

APRIL

IEEE Applied Power Electronics Conference and Exposition (APEC '98), Feb. 15-19. The Disneyland Hotel, Anaheim, CA. Contact Pamela Wagner, Courtesy Associates, 655 15th St., N.W., Suite 300, Washington, DC 20005; (202) 639-4990; fax (202) 347-6109; e-mail: pwagner@courtesyassoc.com.

Southeastcon '98, Apr. 10-15. Hyatt Regency, Orlando International Airport, Orlando, FL. Contact Parveen Ward, ECE Dept., University of Central Florida, Orlando, FL 32816; (407) 823-2610; fax (407) 823-5835; e-mail: pfw@ece.engr.ucf.edu.

MAY

IEEE International Conference on Evolutionary Computation, May 3-9. Ankorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@akaska.net.

IEEE International Conference on Neural Networks (ICNN '98), May 3-9. Anchorage, Alaska. Contact Patrick K. Simpson, Scientific Fisher Systems Inc., Post Office Box 242065, Anchorage, Alaska 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@akaska.net.

IEEE World Congress on Computational Intelligence, May 3-9. William A. Egan Civic and Convention Center, Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc. P.O. Box 242064, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

MAY

Seventh IEEE International Fuzzy Systems Conference, May 3-9. Anchorage, Alaska. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, Alaska 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

IEEE/IAS Industrial & Commercial Power Systems Technical Conference (I&CPS), May 4-7. Edmonton, Alberta, Canada. Contact Marty Bince, Modicon Canada Ltd., 5803 86th St., Edmonton, Alberta T6E 2X4, Canada; (403) 468-6673; fax (403) 468-2925.

IEEE International Conference on Acoustics, Speech & Signal Processing (ICASSP '98), May 12-15. Seattle Convention Center, Seattle, WA. Contact Les E. Atlas, Dept. EE(FT 10), University of Washington, Seattle, WA 98195; (206) 685-1315; fax (206) 543-3842; e-mail: atlas@ee.washington.edu.

JUNE

IEEE/MTT-S International Microwave Symposium (MTT 98), June 7-12. Baltimore Convention Center, Baltimore, MD. Contact Steven Stitzer, Westinghouse Electric Corp., P.O. Box 1521, MS 3T15, Baltimore, MD 21203; (410) 765-7348; fax (410) 993-7747.

USENIX 1998 Technical Conference, June 13-17. Marriott Hotel, New Orleans, LA. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

JULY

IEEE International Geoscience & Remote Sensing Symposium (IGARSS '98), July 6-10. Sheraton Seattle, Washington. Contact Tammy I. Stein, IGARSS Business Office, 2610 Lakeway Drive, Seabrook, Texas 77586-1587, (281) 291-9222; fax (281) 291-9224; e-mail: tstein@phoenix.net.

IEEE Power Engineering Society Summer Meeting, July 11-17. Sheraton Hotel, San Diego, CA. Contact Terry Snow, San Diego Gas & Electric, P.O. Box 1831, San Diego, CA 92112; (619) 696-2780; fax (619) 699-5096.

IEEE Power Engineering Society Summer Meeting, July 12-16. Sheraton San Diego Hotel & Marina, San Diego, CA. Contact Terry Snow, San Diego Gas & Electric, P.O. Box 1831, San Diego, CA 92112; (619) 696-2780; fax (619) 699-5096; e-mail: t.snow@ieee.org.

IEEE Nuclear & Space Radiation Effects Conference (NSREC '98), July 20-24. Newport Beach, CA. Contact Jim Schwank, Sandia National Laboratories, P.O. Box 5800, MS-1083, Albuquerque, NM 87185-1083; (505) 844-8376; fax (505) 844-2991; e-mail: schwanjr@sandia.gov.

AUGUST

AUTOTESTCON '98, Aug. 24-27. Salt Palace Convention Center, Salt Lake City, UT. Contact Robert Myers, Myers/Smith Inc., 3685 Motor Ave., Suite 240, Los Angeles, CA 90034; (310) 287-1463; fax (310) 287-1851; e-mail:bob.myers@ieee.org.

OCTOBER

IEEE International Conference on Systems, Man, & Cybernetics, Oct. 12-14. Hyatt Regency La Jolla, La Jolla, CA. Contact M.A. Jafari, Dept. of Industrial Engineering, Rutgers University, P.O. Box 909, Piscataway, NJ 08855; (908) 445-3627; (908) 445-5467; e-mail: jafari@gandalf.rutgers.edu.

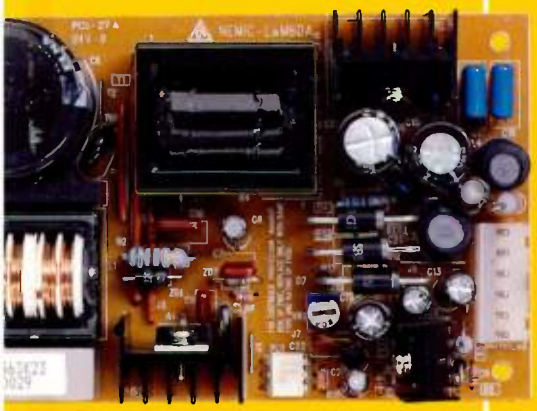
NOVEMBER

IEEE Global Telecommunications Conference (Globecom '98), Nov. 9-13. Sydney, Australia. Contact Sam Reisenfeld, School of Electrical Engineering, University of Technology, Sydney, P.O. Box 123; Broadway, NSW 2007, Australia; (61) 2-330-2435; e-mail: samr@trnasmit.ee.uts.edu.au.

DECEMBER

12th Systems Administration Conference (LISA '98), Dec. 6-11. Marriott Hotel, Boston, Massachusetts. Contact USENIX Conference Office, 22672 Lambert Street, Suite 613, Lake Forest, California 92630; (714) 588-8649; (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

"I'm going with these power supplies not because of Lambda's reputation for reliability, their worldwide distribution and support, or all of the features they have to offer.



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Single and multiple outputs,
from 5W to 150W.

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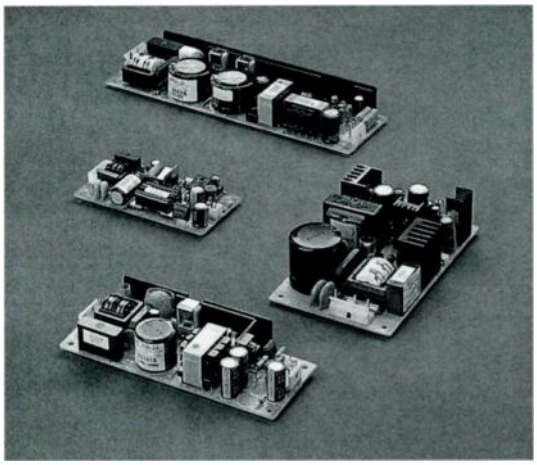
Lambda's SWT, ZWS, VSB Series



Low cost single and triple outputs for high volume worldwide applications

Now, Lambda reliability and support is available in low cost, industry standard power supplies in a variety of package sizes – including 3"x5". Lambda's new SWT, ZWS and VSB Series are ideally suited for use in computers, peripherals, factory, office automation and other high volume applications.

Available from 5W-150W, many models are designed with a universal AC input, as well as power factor correction for worldwide operation. OEM-type input and output connectors are provided for ease of wiring and installation in high volume applications. And all models meet radiated and conducted EMI to Curve B for unparalleled global performance in a cost effective package.

By providing optimal specifications for input voltage, safety agency approvals, size and reliability, Lambda has set the new standard for cost and performance in open frame power supplies.

Broad Product Line	Lambda stocks over 100 single and triple output low cost models, so you can choose the ideal product to meet your specific requirements.
Popular Package Sizes	Lambda's SWT Series is available in the popular 3"x5" footprint. In addition, the ZWS and VSB Series are designed in a variety of low profile, narrow packages – fitting easily into desktop or 1U heights.
Universal Input	85-265VAC input on the SWT and ZWS Series provides the ideal turn-key solutions for worldwide use. 110VAC VSB Series models are also available for cost sensitive North American applications.
Device Protection	In order to protect the power supply, as well as the load from adverse conditions, the following standard features are designed in: • Overvoltage protection • Overcurrent protection • Short circuit protection
Power Factor Correction	Power factor and harmonic correction available on ZWS models greater than 50W. This ensures compliance to IEC1000-3-2 and improves input power quality, line regulation, AC noise immunity and reliability worldwide.
Meets Worldwide EMI Requirements	Radiated and conducted EMI to EN55022 and FCC Class B simplifies system filtering requirements and eases system compliance in global markets – without external components.
Low Cost, High Value	The proprietary designs minimize the component counts and optimize reliability and cost.
Ease of Manufacturing and Service	All models are designed with Molex type interface connectors ensuring easy assembly and service.
Worldwide Safety Agency Approvals	Safety agency approvals pending for UL 1950, CSA 950, EN60950, and the CE mark (Low Voltage Directive) to ensure compliance throughout the world.
One Year Guarantee	Lambda's one year guarantee includes labor as well as parts.
One Day Delivery	Lambda's SWT, VSB and ZWS Series power supplies are in stock for one day delivery.

OUTPUT VOLTAGE	MAX CURRENT (AMPS)	UNIT PRICE PER DELIVERED QUANTITY 1	10	100	500	1000	MODEL
3.3V±5% FIXED	1.0	$ 35	$ 32	$ 20	$ 17	$ 16	**ZWS5-3**
3.3V±5% FIXED	2.0	38	35	21	18	17	**ZWS10-3**
3.3V±5% FIXED	3.0	50	45	28	24	21	**ZWS15-3**
3.3V±5% FIXED	6.0	55	50	30	25	23	**ZWS30-3**
3.3V±5% FIXED	10.0	68	62	40	33	30	**ZWS50-3**
3.3V±10% ADJ.	15.0	105	95	58	48	45	**ZWS75PF-3**
3.3V±10% ADJ.	20.0	130	117	73	60	55	**ZWS100PF-3**
3.3V±10% ADJ.	30.0	170	153	94	77	71	**ZWS150PF-3**
5V±5% FIXED	1.0	35	32	20	17	16	**ZWS5-5**
5V±5% FIXED	2.0	38	35	21	18	17	**ZWS10-5**
5V±5% FIXED	3.0	50	45	28	24	21	**ZWS15-5**
5V±5% FIXED	6.0	55	50	30	25	23	**ZWS30-5**
5V±5% FIXED	10.0	68	62	40	33	30	**ZWS50-5**
5V±10% ADJ.	15.0	105	95	58	48	45	**ZWS75PF-5**
5V±10% ADJ.	20.0	130	117	73	60	55	**ZWS100PF-5**
5V±10% ADJ.	30.0	170	153	94	77	71	**ZWS150PF-5**
12V±5% FIXED	0.4	35	32	20	17	16	**ZWS5-12**
12V±5% FIXED	0.9	38	35	21	18	17	**ZWS10-12**
12V±5% FIXED	1.3	50	45	28	24	21	**ZWS15-12**
12V±5% FIXED	2.5	55	50	30	25	23	**ZWS30-12**
12V±5% FIXED	4.3	68	62	40	33	30	**ZWS50-12**
12V±5% FIXED	6.3	105	95	58	48	45	**ZWS75PF-12**
12V±5% FIXED	8.5	130	117	73	60	55	**ZWS100PF-12**
12V±5% FIXED	12.5	170	153	94	77	71	**ZWS150PF-12**
15V±5% FIXED	0.3	35	32	20	17	16	**ZWS5-15**
15V±5% FIXED	0.7	38	35	21	18	17	**ZWS10-15**
15V±5% FIXED	1.0	50	45	28	24	21	**ZWS15-15**
15V±5% FIXED	2.0	55	50	30	25	23	**ZWS30-15**
15V±5% FIXED	3.5	68	62	40	33	30	**ZWS50-15**
15V±5% FIXED	5.0	105	95	58	48	45	**ZWS75PF-15**
15V±5% FIXED	6.7	130	117	73	60	55	**ZWS100PF-15**
15V±5% FIXED	10.0	170	153	94	77	71	**ZWS150PF-15**
24V±5% FIXED	0.2	35	32	20	17	16	**ZWS5-24**
24V±5% FIXED	0.5	38	35	21	18	17	**ZWS10-24**
24V±5% FIXED	0.7	50	45	28	24	21	**ZWS15-24**
24V±5% FIXED	1.3	55	50	30	25	23	**ZWS30-24**
24V±5% FIXED	2.1	68	62	40	33	30	**ZWS50-24**
24V±5% FIXED	3.2	105	95	58	48	45	**ZWS75PF-24**
24V±5% FIXED	4.3	130	117	73	60	55	**ZWS100PF-24**
24V±5% FIXED	5.0	144	130	84	69	63	**ZWS120PF-24**
24V±5% FIXED	6.3	170	153	94	77	71	**ZWS150PF-24**
36V±5% FIXED	0.9	55	50	30	25	23	**ZWS30-36**
36V±5% FIXED	1.4	68	62	40	33	30	**ZWS50-36**
36V±5% FIXED	2.1	105	95	58	48	45	**ZWS75PF-36**
36V±5% FIXED	2.8	130	117	73	60	55	**ZWS100PF-36**
36V±5% FIXED	3.4	144	130	84	69	63	**ZWS120PF-36**
36V±5% FIXED	4.2	170	153	94	77	71	**ZWS150PF-36**
48V±5% FIXED	0.7	55	50	30	25	23	**ZWS30-48**
48V±5% FIXED	1.1	68	62	40	33	30	**ZWS50-48**
48V±5% FIXED	1.6	105	95	58	48	45	**ZWS75PF-48**
48V±5% FIXED	2.1	130	117	73	60	55	**ZWS100PF-48**
48V±5% FIXED	3.2	170	153	94	77	71	**ZWS150PF-48**

VSB Series Single Output, 100VAC Input

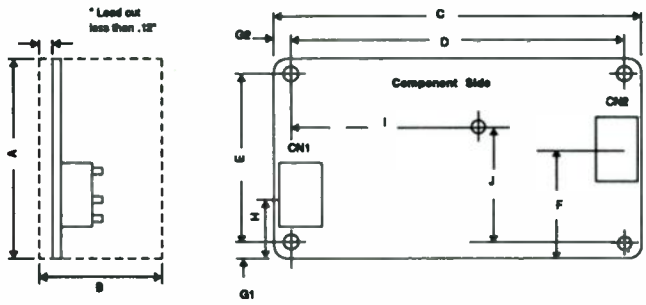
OUTPUT VOLTAGE	MAX CURRENT (AMPS)	UNIT PRICE PER DELIVERED QUANTITY 1	10	100	500	1000	MODEL
3.3V±15% ADJ.	1.0	$ 34	$ 31	$ 19	$ 16	$ 15	**VS10B-3/TRM**
3.3V±15% ADJ.	3.0	44	40	25	22	19	**VS15B-3/TRM**
3.3V±15% ADJ.	6.0	49	44	27	22	21	**VS30B-3/TRM**
3.3V±15% ADJ.	10.0	60	55	36	30	27	**VS50B-3/TRM**
3.3V±15% ADJ.	15.0	93	84	52	43	40	**VS75B-3/TRM**
3.3V±15% ADJ.	20.0	115	103	65	53	49	**VS100B-3/TRM**
3.3V±15% ADJ.	30.0	150	135	83	68	63	**VS150B-3/TRM**
5V±10% ADJ.	2.0	34	31	19	16	15	**VS10B-5/TRM**
5V±10% ADJ.	3.0	44	40	25	22	19	**VS15B-5/TRM**
5V±10% ADJ.	6.0	49	44	27	22	21	**VS30B-5/TRM**
5V±10% ADJ.	10.0	60	55	36	30	27	**VS50B-5/TRM**
5V±10% ADJ.	15.0	93	84	52	43	40	**VS75B-5/TRM**
5V±10% ADJ.	20.0	115	103	65	53	49	**VS100B-5/TRM**
5V±10% ADJ.	30.0	150	135	83	68	63	**VS150B-5/TRM**
12V±10% ADJ.	0.9	34	31	19	16	15	**VS10B-12/TRM**
12V±10% ADJ.	1.3	44	40	25	22	19	**VS15B-12/TRM**
12V±10% ADJ.	2.5	49	44	27	22	21	**VS30B-12/TRM**
12V±10% ADJ.	4.3	60	55	36	30	27	**VS50B-12/TRM**
12V±10% ADJ.	6.3	93	84	52	43	40	**VS75B-12/TRM**
12V±10% ADJ.	8.5	115	103	65	53	49	**VS100B-12/TRM**
12V±10% ADJ.	12.5	150	135	83	68	63	**VS150B-12/TRM**
15V±10% ADJ.	0.7	34	31	19	16	15	**VS10B-15/TRM**
15V±10% ADJ.	1.0	44	40	25	22	19	**VS15B-15/TRM**
15V±10% ADJ.	2.0	49	44	27	22	21	**VS30B-15/TRM**
15V±10% ADJ.	3.5	60	55	36	30	27	**VS50B-15/TRM**
15V±10% ADJ.	5.0	93	84	52	43	40	**VS75B-15/TRM**
15V±10% ADJ.	6.7	115	103	65	53	49	**VS100B-15/TRM**
15V±10% ADJ.	10.0	150	135	83	68	63	**VS150B-15/TRM**
24V±10% ADJ.	0.5	34	31	19	16	15	**VS10B-24/TRM**
24V±10% ADJ.	0.7	44	40	25	22	19	**VS15B-24/TRM**
24V±10% ADJ.	1.3	49	44	27	22	21	**VS30B-24/TRM**
24V±10% ADJ.	2.1	60	55	36	30	27	**VS50B-24/TRM**
24V±10% ADJ.	3.2	93	84	52	43	40	**VS75B-24/TRM**
24V±10% ADJ.	4.3	115	103	65	53	49	**VS100B-24/TRM**
24V±10% ADJ.	6.3	150	135	83	68	63	**VS150B-24/TRM**
36V±10% ADJ.	3.2	93	84	52	43	40	**VS75B-36/TRM**
36V±10% ADJ.	4.3	115	103	65	53	49	**VS100B-36/TRM**
36V±10% ADJ.	6.3	150	135	83	68	63	**VS150B-36/TRM**
48V±10% ADJ.	1.6	93	84	52	43	40	**VS75B-48/TRM**
48V±10% ADJ.	2.1	115	103	65	53	49	**VS100B-48/TRM**
48V±10% ADJ.	3.2	150	135	83	68	63	**VS150B-48/TRM**

SWT Series Triple Output

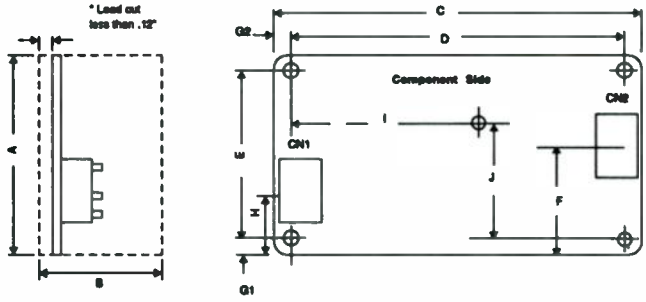
MAX POWER	OUTPUT 1	OUTPUT 2	OUTPUT 3	UNIT PRICE PER DELIVERED QUANTITY 1	10	25	50	MODEL
30W	+5V@2A	+12V@1.5A	-5V@0.3A	$67	$64	$60	$45	**SWT30-525**
30W	+5V@2A	+12V@1.5A	-12V@0.3A	67	64	60	45	**SWT30-522**
30W	+5V@2A	+15V@1A	-15V@0.3A	67	64	60	45	**SWT30-5FF**
40W	+5V@3A	+12V@2A	-5V@0.3A	78	74	70	53	**SWT40-525**
40W	+5V@3A	+12V@2A	-12V@0.3A	78	74	70	53	**SWT40-522**
40W	+5V@3A	+15V@2A	-15V@0.3A	78	74	70	53	**SWT40-5FF**
65W	+5V@6A	+12V@2.5A	-5V@0.5A	95	90	86	64	**SWT65-525**
65W	+5V@6A	+12V@2.5A	-12V@0.5A	95	90	86	64	**SWT65-522**
65W	+5V@6A	+15V@1.8A	-15V@0.5A	95	90	86	64	**SWT65-5FF**
100W	+5V@8A	+12V@4A	-5V@0.8A	135	128	122	91	**SWT100-525**
100W	+5V@8A	+12V@4A	-12V@0.8A	135	128	122	91	**SWT100-522**
100W	+5V@8A	+15V@3.2A	-15V@0.8A	135	128	122	91	**SWT100-5FF**
140W	+5V@20A	+12V@2A	-12V@1A	188	179	168	139	**SWT140-522***

NOTE: *Contact the factory for status and specifications.

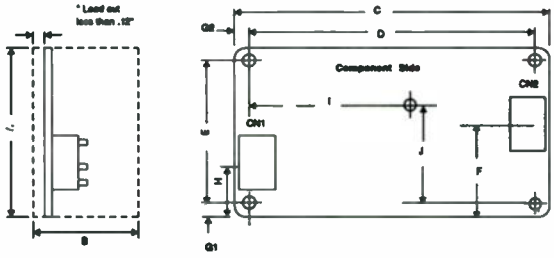
SWT Outline Drawing



ZWS Outline Drawing



VSB Outline Drawing



DIMENSIONS

MODEL	A	B	C	D	E	F	G1/G2*	H	I	J
SWT30	3.00	1.20	5.00	4.55	2.55	0.93	0.224	1.04	-	-
SWT40	3.00	1.40	5.00	4.55	2.55	1.61	0.224	1.03		
SWT65	3.50	1.77	6.00	4.80	3.15	1.19	0.18/0.60*	N/A	-	-
SWT100	4.25	1.77	7.75	7.25	3.75	2.05	0.25	1.0	5.05	1.85
ZWS5	1.77	0.83	3.86	3.58	1.50	0.54	0.14	1.05	-	-
ZWS10	1.97	0.83	4.14	3.86	1.69	0.67	0.14	0.99	-	-
ZWS15	1.97	0.83	4.93	4.65	1.69	0.57	0.14	1.04	-	-
ZWS30	2.17	1.02	5.24	4.85	1.77	1.16	0.20	0.20	-	-
ZWS50	2.17	1.02	7.68	7.29	1.77	0.72	0.20	1.32	-	-
ZWS75PF	2.17	1.38	8.74	8.35	1.77	0.88	0.20	1.04	3.33	0.0
ZWS100PF	2.44	1.38	8.74	8.35	2.05	1.02	0.20	1.00	3.23	0.28
ZWS150PF	2.95	1.58	8.74	8.35	2.56	1.90/0.80**	0.20	2.01	2.93	0.55
VS10B	1.93	0.67	3.70	3.43	1.65	0.85	0.14	1.02	-	-
VS15B	1.97	0.67	4..53	4.26	1.69	1.39	0.14	1.22	-	-
VS30B	1.97	0.985	5.22	4.83	1.58	1.18	0.197	1.02	-	-
VS50B	1.97	0.985	7.68	7.23	1.58	0.67	0.197	1.10	4.85	1.10
VS75B	1.97	1.26	8.74	8.35	1.57	1.06	0.20	0.85	5.33	1.28
VS100B	2.44	1.26	8.74	8.35	2.05	1.22	0.20	0.98	4.70	1.67
VS150B	2.95	1.42	8.74	8.35	2.56	0.91/0.85**	0.20	1.81	4.96	2.17

Note: All Dimensions are in Inches
See Installation Data Sheet For Tolerances And Mounting Holes
*G1 - G2 Unless Noted
**Two Connectors

AC Input
85-265VAC, 50-60Hz on SWT30, 40,100.
85-265VAC, 40-440Hz on ZWS5 through ZWS50.
85-132VAC/170-265VAC, 47-63 Hz on ZWS75 through ZWS150 and on SWT65, 140.
85-132VAC, 47-440Hz on VSB Series.

EMI
Radiated and conducted EMI conforms to FCC Class B, VCC1-2 and EN55022 on all models.

Power Factor and Harmonic Correction
Available on all ZWS models greater than 50W.

DC Output
Voltage ranges are shown in tables.

DC Output Range
5.0-5.25V adj. on the main output of SWT Series. Auxiliary outputs are fixed.

Efficiency

	Typical Efficiences (%)							
	All	3V	5V	12V	15V	24V	36V	48V
SWT30,40	70	-	-	-	-	-	-	-
SWT65,100,140	72	-	-	-	-	-	-	-
ZWS5	-	62	67	68	68	70	-	-
ZWS10,VS10B	-	62	70	70	71	71	-	-
ZWS15,VS15B	-	63	71	71	71	71	-	-
ZWS30,VS30	-	70	75	77	77	78	78	78
ZWS50,VS50	-	73	77	80	81	82	82	82
ZWS75PF,VS75B	-	70	75	77	78	80	80	80
ZWS100PF,VS100B	-	72	78	80	80	82	82	82
ZWS150PF,VS150B	-	72	78	80	80	82	82	82

Regulated Voltage

line regulation.....SWT Series: 1% on the main output, 5% on auxiliary outputs. ZWS, VSB Series: 20mV on 3V and 5V models. 48mV on 12V models. 60mV on 15V models. 96mV on 24V models. 144mV on 36V models. 192mV on 48V models.

load regulation .....SWT Series: 2% on Outputs 1 and 3. 4% on Output 2. ZWT, VSB Series: 40mV on 3V, 5V models. 96mV on 12V models. 120mV on 15V models. 240mV on 36V models. 300mV on 48V models.

ripple and noise.....120mV pk-pk for the main output of SWT Series; 3V, 5V outputs of ZWS, VSB Series. 150mV pk-pk for auxiliary outputs of SWT Series; 12V, 15V outputs of ZWS, VSB Series. 200mV pk-pk for 24V output of ZWS, VSB Series. 300mV pk-pk for 36V output of ZWS, VSB Series. 400mV pk-pk for 48V output of ZWS, VSB Series.

temp. coeff. .....0.04%/°C on SWT Series

In-Rush Current Limiting
30A on ZWS75PF, 100PF, 150PF, VS75B, 100B, 150B; and on 200VAC models of ZWS5, 10, 15, 30, 50 and VS10B, 15B, 30B, 50B. 15A on all other models.

DC Input
110-330VDC on ZWS5, 10, 15, 30, 50. 110-175VDC on VS Series.

Preload and Overcurrent Protection
SW Series only.

Model	Output 1	Output 2	Output 3	Overcurrent Protection (min.)
SWT30	0.2A	0.4A	0	170%
SWT40	0.2A	0.3A	0	140%
SWT65	0.3A	0	0	105%
SWT100	0.5A	0	0	105%
SWT140	2.0A	0	0	105%

Overvoltage Protection
Overvoltage protection is provided on the main 5V output of the SWT Series. AC input must be recycled to restore operation. 140% on ZWS5, 10, 15, 30 and VS10B, 15B, 30B. 125% on ZWS50, VS50B. 115-135% on ZWS75PF and VS75B.

Overload Protection
Avoid short circuit or overload condition for more than 30 seconds.

Surge Current Capability
Surge current capability on the SWT30 and SWT40 only. 10 second surge of 1.5 times the output current rating with a 30% duty cycle. Total power must not be exceeded.

Cooling
All models are convection cooled (100% load).

Operating Temperature Range
0°C to +50°C continuous operation on SWT Series. Derate output power linearly to 70% up to +60°C operation. -10°C to 60°C on ZWS, VSB Series. Derate as follows: ZWS5-100PF, VS10B-100B: –10°C to +50°C:(100%) +60°C (70%) VS150B -10°C to +30°C (100%) +40°C (80%) +60°C:(50%).

Storage Temperature Range
–40°C to +85°C on SW Series. –30°C to 85°C on ZWS and VSB Series.

Isolation Rating
3000VAC Input to Output for 1 minute. 2500VAC Input to Chassis for 1 minute on SW Series; 2000VAC on all other models. 500VAC Output to Chassis for 1 minute.

Mounting
One mounting surface on all models. Ratings are for horizontal mounting, component side up. Consult factory for ratings for other mounting configurations.

Construction
PC Board construction.

Physical Data

Package Model	Lbs. Net.	Lbs. Ship.	Dimensions (Inches) (L x H x W)
ZWS5	0.26	0.60	1.77 x 0.83 x 3.86
VS10B	0.26	0.60	1.93 x 0.67 x 3.70
ZWS10	0.26	0.60	1.97 x 0.83 x 4.13
VS15B	0.26	0.60	1.97 x 0.67 x 4.53
ZWS15	0.26	0.60	1.97 x 0.83 x 4.92
VS30B	0.26	0.60	1.97 x 0.98 x 5.22
ZWS30	0.59	0.90	2.17 x 1.02 x 5.24
VS50B	0.26	0.60	1.97 x 0.98 x 7.68
ZWS50	0.59	0.90	2.17 x 1.02 x 7.68
VS75B	0.59	0.90	1.97 x 1.26 x 8.76
SWT30	0.51	0.75	3.0 x 1.2 x 5.0
SWT40	0.62	0.87	3.0 x 1.4 x 5.0
SWT65	0.77	1.00	3.5 x 1.77 x 6.0
SWT100	1.32	1.50	4.25 x 1.77 x 7.75
ZWS75PF	1.34	1.60	2.17 x 1.38 x 8.74
VS100B	1.34	1.60	2.44 x 1.26 x 8.76
SWT140'	1.35	1.55	4.25 x 2 x 7.75
ZWS100PF	1.61	1.90	2.44 x 1.38 x 8.74
VS150B	1.61	1.90	2.95 x 1.42 x 8.76
ZWS150PF	2.14	2.50	2.95 x 1.58 x 8.74

Mating Connectors
Available separately as evaluation kits or direct from Molex.

	Input CN1 Molex		Output CN2 Molex		Pins		Lambda Evaluation
Model	Qty	Order #	Qty	Order #	Qty	Spool/ Loose	Kits ($9)
SWT30	1	09-52-4064	1	09-52-4064	13	516PGT/08-70-0013	KT-SWT30
SWT40	1	09-52-4064	1	09-52-4064	13	516PGT/08-70-0013	KT-SWT40
SWT65	1	09-52-4064	1	09-52-4074	13	516PGT/08-70-0013	KT-SWT65
SWT100	1	09-52-4064	1	09-52-4104	13	516PGT/08-70-0013	KT-SWT100
SWT140	-	-	-	-	-	-	KT-SWT140

Contact the factory for part numbers on other models

Safety Agency Approvals
All models are presently under evaluation for UL 1950, CSA 234 M90, IEC 950, EN 60950 and the CE Mark (Low Voltage Directive).

Guarantee
One year guarantee includes parts as well as labor. Guarantee applies to operation within the published specifications and recommended application data at the end of one year.

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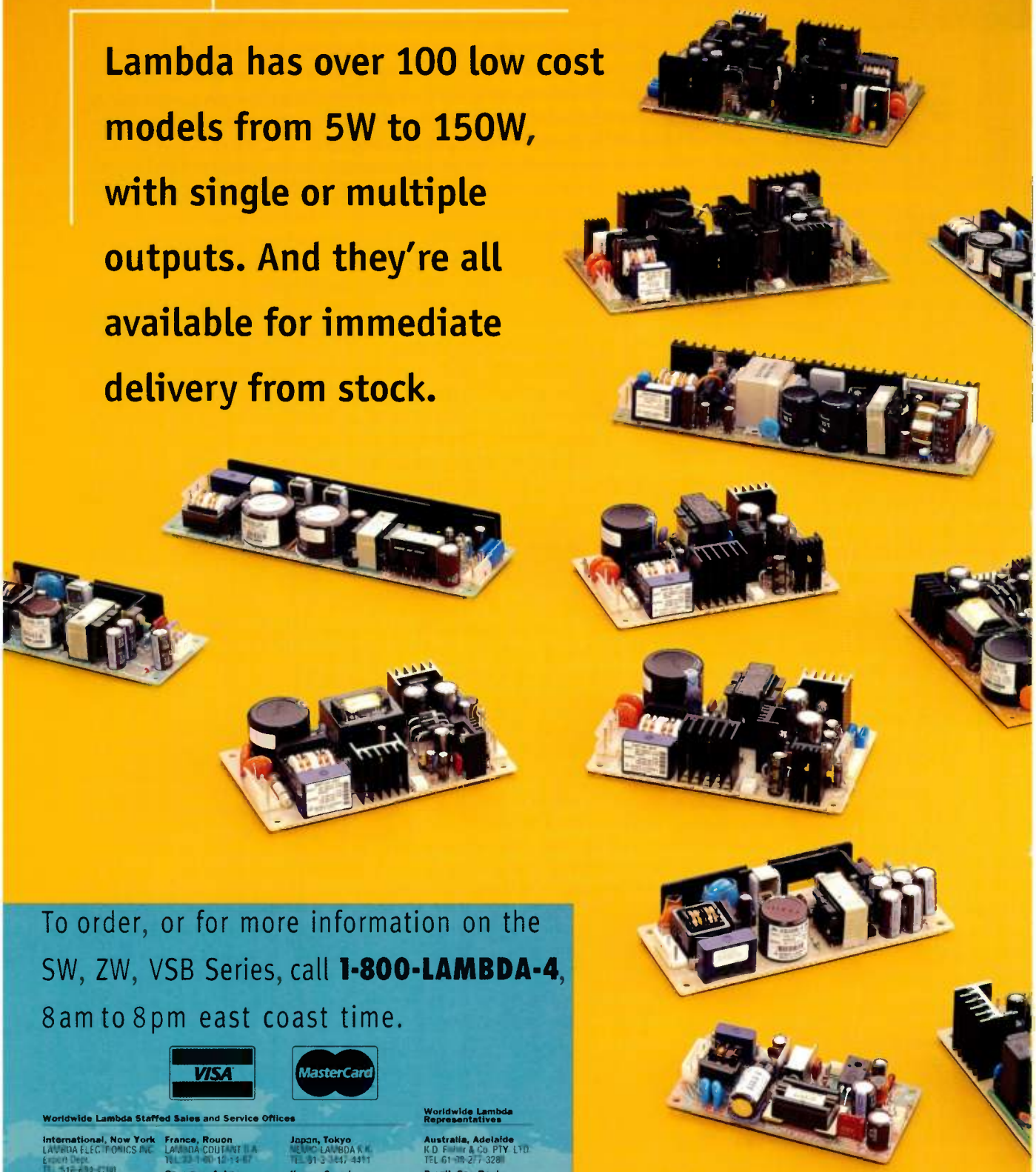

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Analog/Mixed-Signal Standards Needed For Next Generation Design Tools

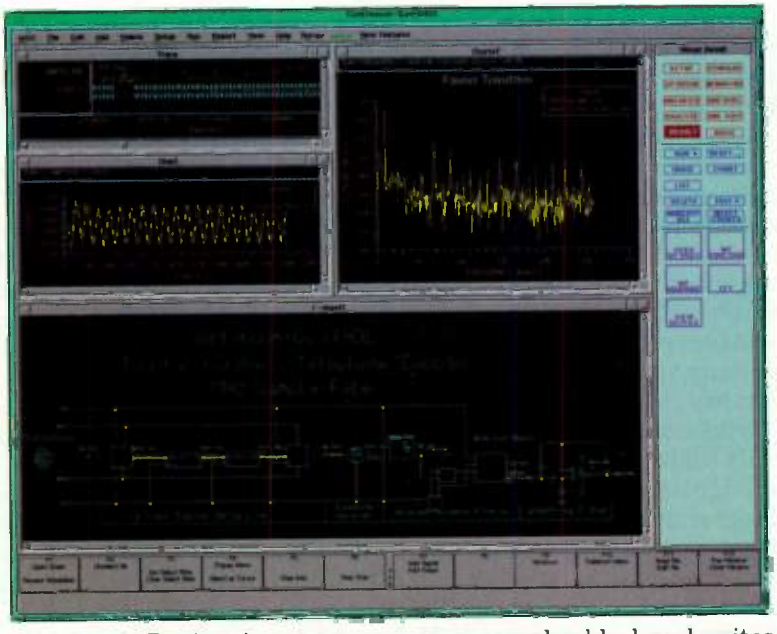
Larger, More Complex Analog Systems, Coupled With The Need For A Common Analog/Digital Design Method, Drives The Development Of A Standardized Mixed-Signal Language.

Cheryl Ajluni

SPECIAL REPORT

Like it or not, analog/mixed-signal design is here to stay. In fact, much to the chagrin of almost every digital designer, it's becoming more prevalent, spurred by a number of factors including increased chip complexity and shortened product life-cycles. What makes many digital designers downright uncomfortable is that not only are they faced with mixed-signal designs that contain significantly increased analog content, but they are being forced to deal with real-world analog effects earlier in the design cycle.

Back when the analog content of mixed-signal designs was minute, the designer simply partitioned the design into analog and digital blocks at the beginning of the development cycle. Separate simulations were run on each block and the blocks were then merged together at the end of the design cycle. Unfortunately, it's not that simple anymore.



Art Courtesy: Mentor Graphics

The landscape of the Electronic Design Automation (EDA) industry is changing drastically. At the same time, there has been rapid growth in the analog/mixed-signal area. This growth, coupled with the convergence of multimedia, telecommunications, and computing, or as Laurie Stanley, Senior Public Relations Manager at Cadence Design Systems, Inc., San Jose, Calif., puts it, "the consumerization of electronics," results in increased challenges facing analog/mixed-signal design. Compounding the issue is that today's designer is driven by the need to put more functionality on smaller dies with increased performance and faster time-to-market. Add to the mix the migration toward systems on a chip and an increased number of applications that require high complexity monolithic solutions sporting lower power and portability requirements. The result is a segment of the industry crying out for direction and the development of simulation engines based on a set of standardized languages that will allow the designer to describe digital and analog functions with the same tool *(see "Developing A Mixed-Signal Standard," p. 68).*

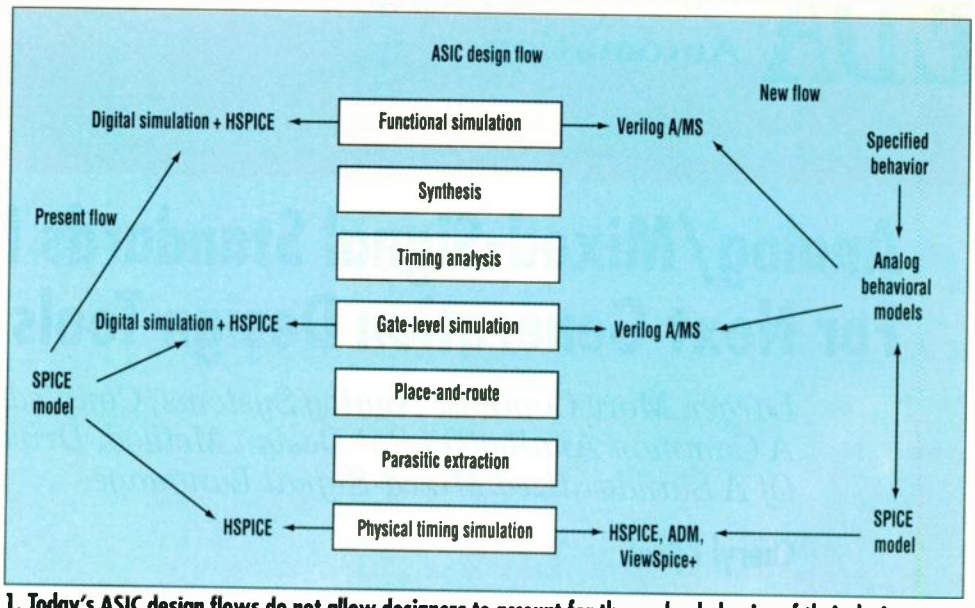
Today's Landscape

Currently, the designer using both analog and digital blocks has limited options to accomplish the design goal. One option available is to use the Verilog bits2real method. With this technique, the designer takes an analog block and writes a Verilog module for it. This is followed by a co-simulation using the bits2real blocks. Although this technique does permit dealing with analog components, it tends to be a very slow and clunky process.

Another method of analog/mixed-signal design is to use blocks of analog behavior models developed by expert analog designers. Some designers simply create an analog specification and merge it with the digital part of the design later on at the physical simulation level (*Fig. 1*). Once the analog

and digital design aspects have been integrated, the devices performance is verified through a chip-level simulation.

Designers also can use HSpice, Spice, or Matlab to model analog effects. These models can then be used at the gate-level simulation stage to provide relatively accurate results. The difficulty with this approach is that these solutions are locked into primitives or elements, such as transistors, capacitors, and resistors, that must be used to describe the analog effect. This means that the analog behavior can't be modeled directly. Although it produces accurate results, it is very difficult, time-consuming, and limits the designer's flexibility. And, putting the models together from each of the different tools once they are complete is prone to errors, not to mention the fact that if one language has a revision, it affects the other language components, which makes revisions a nightmare.



1. Today's ASIC design flows do not allow designers to account for the analog behavior of their designs early on in the design cycle. Consequently, designers are unable to leverage the benefits that are attributable to a top-down design methodology. Instead, they typically are forced to wait until physical timing simulation to incorporate the analog effects into a mixed-signal design. The same situation also holds true for today's System and PCB design flows.

To further complicate matters, many of these approaches reinforce the traditionally separate roles of the digital and analog designer. Although the analog/mixed-signal design task has become more complicated, design team communication is kept to a minimum. When digital engineers are forced to deal with analog effects, their first response usually is to change the analog input into a digital input and then proceed with the design. This "bury your head in the sand" approach rarely gives designers a high level of confidence in design validation, typically leads to more surprises and more design iterations, and prevents the designer from exploring architectural options, optimizing a design, or even exploring design weaknesses.

Another alternative is to use proprietary language-based tools available from various companies. These tools tend to be difficult to support and costly to own. But, in the absence of any standardized HDL languages, they have enabled design solutions that would not have been possible otherwise.

Analogy, Beaverton, Ore., for example, is one company that offers an HDL-based analog simulator for mixed-signal design, known as Saber. Based on its own proprietary language (MAST), Saber can be utilized for both IC- and system-level design and enables analog, mixed-signal, and mixed-technology modeling. Unlike the standards now available in the analog/mixed-signal design area, MAST provides unique built-in features for statistical analysis. According to David Smith, marketing manager at Analogy, "MAST has been around a long time and has an extremely large installed base of models. While it will take a while before models and simulators can be developed for the standard languages in development, MAST provides a complete solution for the designer now, libraries and all." When a mixed-signal standard does become available, Analogy promises to ensure interoperability between its tools based on the MAST language and the standard language.

Spectre HDL from Cadence, San Jose, Calif., is an analog design tool that utilizes a Verilog-A simulator, and is currently available to designers. Based on an open architecture concept, the tool seeks to provide a front- to-back, fully-integrated solution. The company has been actively participating in standards organizations to ensure that its tool will be compliant with any initial standards offerings. In fact, the company intends to have an analog/mixed-signal standards-compliant product available in the near future.

Viewlogic, Fremont, Calif., also supports the industry standards and promises tool compliance once they are passed. Its current product in the analog/mixed-signal area, Fusion-HDL, a logic simulator product for ASIC and IC designers, effectively allows designers to mix digital and analog designs. It can perform mixed-digital/analog simulation and has links to HSpice, PSpice, ViewSpiceTM, and Analogy's Saber Designer.

When the researchers at Mentor Graphics, Wilsonville, Ore., looked into design solutions for the analog/mixed-signal arena, they realized that some sort of language solution was needed, but there were no standards yet available. As it stood, designers were experiencing run times of weeks, high overhead, and the inability to perform full chip analog/mixed-signal simulation. Recognizing this need, the company developed HDL-A, a VHDL-based analog modeling language dedicated to the behavioral description of analog and mixed-signal components. Designed to be upwards-compatible with the IEEE VHDL standard 1076.1, HDL-A, combined with the company's Eldo simulator, forms the basis of a modeling simulation environment that

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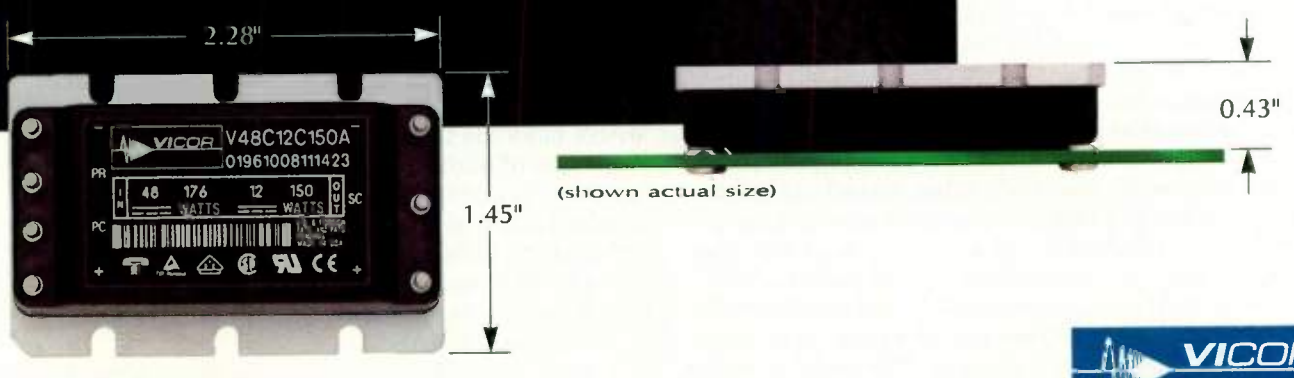

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includes analog and mixed-signal simulation. As a follow-on, the company's Mixed-signal Pro combines Eldo and HLD-A in support of analog and digital models described in VHDL or Verilog, hierarchical analog behavioral models, and Spice-level descriptions in a high-performance simulation environment. Unique to the Mixed-Signal Pro tool is its architecture in which analog and digital processes are scheduled by a specially-adapted algorithm.

The tools offered by Mentor, based on the HLD-A language, enable top-down design over multiple domains, which means virtual prototyping is possible, as well as full chip simulation. The HDL-A language has more than 6200 models from diodes and transistors to specialized parts such as op amps, pulse-width modulators, and other complex devices. According to the company, the HDL-A language is a temporary one that will progressively disappear as the analog/mixed-signal version of the VHDL language becomes a reality. Consequently, by the time Mentor's customers migrate to version 3 of the HDL-A , they will actually be using VHDL A/MS, because they will be one and the same. This approach, phasing out of one's own language tool, is unique. But as Mentor explains, it is not looking to protect its own intellectual property, but rather the intellectual property for its entire customer base.

While several methodologies now exist that allow an analog and digital simulator to interact and perform mixed-signal simulation, what's needed is a next-generation simulation capability that will allow mixed-signal behavior to be described using one common language. In effect, a way to define analog behavior at the functional simulation stage, not just at the gate-level simulation stage.

One reason why the issue of standards development is such a hot topic in the analog/mixed-signal environment is because designers can no longer con-

Developing A Mixed-Signal HDL Standard

Many of the pressures that drove the creation and adoption of VHDL are now present in the mixed-signal domain. No longer an arcane offshoot, analog systems are now becoming more prevalent, larger and of greater complexity, requiring the coordinated design efforts of many people.

More designs fall into the mixed analog/digital domain, further complicating matters. It is no longer feasible for mixed-signal simulation to consist of taking digital simulation results and analog simulation results, and "guestimating" about the interaction between the two. The interaction of thermal, mechanical, and hydraulic systems with electrical systems on a single integrated circuit, now being investigated by the Micro Electro-Mechanical Systems (MEMS) initiative from DARPA, adds even more complexity.

The same top-down design techniques that have been used in the digital domain are being employed successfully by leading edge systems designers who use mixed-technology HDLs such as MAST, in combination with VHDL and Verilog. But as the above challenges progress from the cutting edge to mainstream design, the demand for standardization has correspondingly increased. In response to this demand, the IEEE is developing 1076.1, which is an analog and mixed-technology extension to the 1076 digital VHDL language. Open Verilog International (OVI) is developing an extension to Verilog, called Verilog A/MS. It is hoped that both standards will be finalized this year.

There are valuable benefits from using a standard HDL that addresses the analog, mixed-signal, and mixed-technology domains. Foremost among these benefits is that the models and designs created with standard language are independent of tool vendors. With a standard HDL, designers are not bound to a single vendor's language, so they are free to switch tools when a better solution becomes available. The investment that they make in creating their models is protected.

Vendor independence associated with the adoption of a standard is positive because it leads to increased competition among tool vendors. A standard language has a stable, public specification. This lowers the entry barrier to small, innovative entrepreneurs who no longer have to reverse-engineer the semantics of a proprietary language and risk litigation. To effectively compete, EDA vendors must differentiate in areas other than language, such as speed, ease of use, platform, or complementary tools. More competition means lower prices, better service, and higher quality to customers.

Vendor independence and the stability of a standard language will eventually lead to the availability of more models to users. It also leads to easier communication of design data between different groups and even different companies, facilitating teamwork. By sharing their internally-written models, they expand the pool of available models. Libraries of models can be accumulated without fear of obsolescence.

Does the demand for standardization mean the end of languages like Analogy's MAST? Definitely not. A standardized language will be the least common denominator of the set of features required to model mixed-signal and mixed-technology behavior. Designs that push the technology envelope will always need advanced features and flexibility that go beyond the scope of a standard language. In this case, the stability of a standard language actually works against it. Languages such as MAST have the flexibility to respond quickly to the challenges of leading edge design, and fill the gap during the extended period of time it takes to update a standard language. And with the advances in simulator architecture, including single-kernal solutions in which multiple languages are usable, users can reap both the benefits of standards and the leading-edge technology of a language like MAST.

Contributed by Kurt Schwartz, Technical Marketing Engineer, Analogy Inc., Beaverton, Ore.

Model 2010

7½ digits

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• DC volts	10nV – 1000V	1nV – 1100V	10nV – 1100V	100nV – 1000V
• AC volts	100nV – 750V	100nV – 1100V pk	100nV – 1100V pk	100nV – 750V
• Ohms	1μΩ – 100MΩ	100nΩ – 1GΩ	1μΩ – 1GΩ	100μΩ – 120MΩ
• DC amps	10nA – 3A	10pA – 2.1A	10pA – 2.1A	10nA – 3A
• AC amps	1μA – 3A	100pA – 2.1A	100pA – 2.1A	1μA – 3A

tinue designing as before. New tools are needed to better equip designers to work in an increasingly complex, increasingly analog world. To accomplish this with widespread acceptance, standards cannot be avoided.

Wanted: Design Standards

A number of organizations are sponsoring efforts toward the development of standards as extensions of Verilog and VHDL for the analog/mixed-signal design environment. While each takes different approaches to the problem, they all have the same goal—to make it possible for the digital and analog side of a design to speak the same language, and for designers to be able to work in a mixed-signal environment, with the same language. Organizations such as OVI (Open Verilog International), Los Gatos, Calif., IEEE (Institute for Electrical and Electronics Engineers), and the Virtual Socket Interface Alliance (VSIA), both in San Jose, Calif., with its active mixed-signal working group, among others, are not adversarial or aggressively in opposition in their standardization attempts. Rather, as Graham Bell, Analog Products Marketing Manager at Viewlogic, Fremont, Calif., explains, "They are complementary, and in the end, Verilog A/MS and the analog/mixed-signal version of 1076.1 VHDL will both have a place."

However, building an analog language standard is difficult because it faces the same problems as on the digital side, and also the associated analog problems due to the nature of the circuits. There are only a small number of analog/mixed-signal tool vendors in the EDA industry, and many of the technologies available on the digital design side do not yet have analog counterparts. Added to this is the fact that the EDA industry is known for having tools that notoriously lag behind the available technology, and it's easy to see that the road ahead, although paved with good intentions, is bound to be rocky.

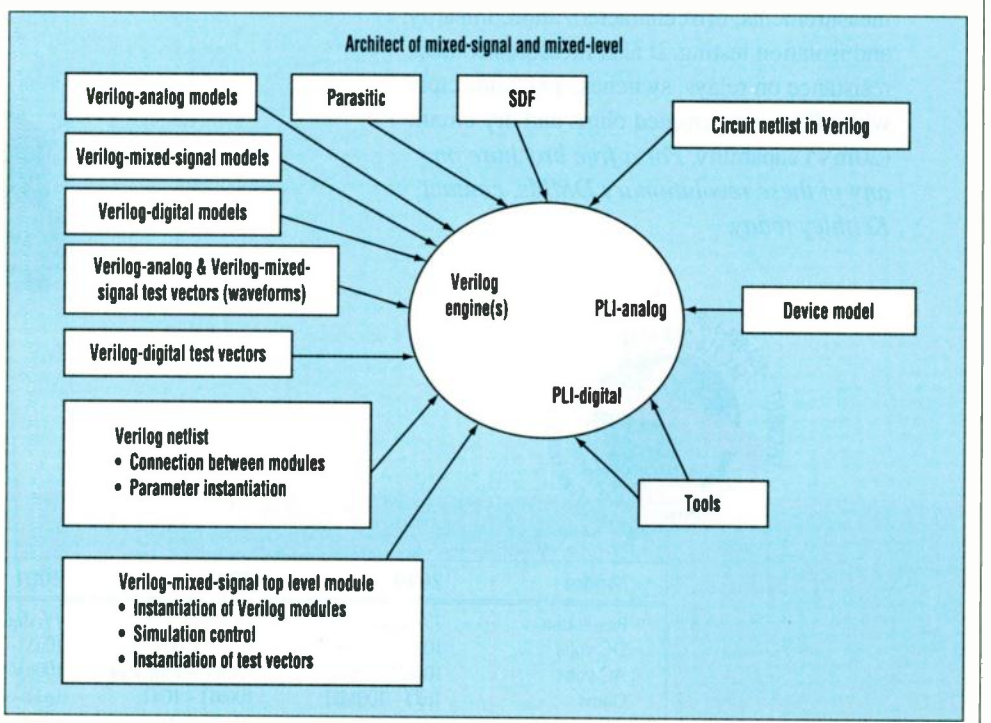
On the Verilog side, great progress has been made—spearheaded by OVI—toward the development of an analog/mixed-signal language standard. Verilog-A, the analog extension of Verilog, was published at the Design Automation Conference (DAC) this past June. As an extension to the IEEE 1364 Verilog HDL specification and Spice, it is the first step toward the development of a full mixed-signal Verilog standard. It emphasizes mathematical descriptions to describe electrical or nonelectrical behavior in terms of input and output ports for components and system modules. These modules can be hierarchically interconnected into full system descriptions.

Verilog-A, while already building up a client list, is expected to take off in the next year as designers begin understanding that it can do things that they cannot presently do with the Verilog language-based design tools. For example, if you can describe something with a differential equation, then it can be dealt with by Verilog-A. This includes such things as a nonelectrical motor, a car's wheel movement, or thermal effects.

The VHDL effort, VHDL-A 1076.1, while not progressing quite as fast as Verilog-A, will begin standard balloting this month. A draft should be ready in June, and the actual standard is expected to be available next year.

Toward the development on an analog/mixed-signal standard language, OVI is now working on Verilog A/MS, scheduled for release later this year. As an extension to Verilog to describe mixed-signal behavior, it will define the interface between analog (continuous-time) and digital (event-driven) modules *(Fig. 2)*. This language interface will help deal with moving signals across the digital-to-analog interface. In effect, this means that the designer will only see one netlist, as opposed to the two that come from using two different languages and two different language formats.

The IEEE also is working on a Verilog A/MS standard. It is the same as the one being worked on by OVI to the extent that OVI's finished standard will be used as a starting point from which the more general IEEE standard will be based *(Fig. 3)*. As an aside, the standard developers predict that for the IEEE Verilog A/MS standard to remain compatible with Verilog 1364-1995, some changes must be instituted into the Verilog 1364 standard. To remedy this, a new Verilog standard will be out in 1998 that will encompass any needed changes to make the two compliant. This standard Verilog 1364-1998 will be both recertified and restandardized. To date, there is no VHDL analog/mixed-signal standard.



2. OVI's view of the analog/mixed-signal design solution involves more than just a mixed-signal extension to the Verilog language standard. One benefit is the single resulting netlist.

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The analog/mixed-signal design environment has traditionally occupied a small niche within the EDA industry. In recent years, it has emerged as one of concern for many designers who are worried about designing the digital part of their designs and its real-world analog effects. This breakdown in the traditional analog/mixed-signal design method has become more difficult to deal with as the market grows, because designers don't have the luxury of tool interoperability. Therefore, they can't leverage the power of a single language across multiple tool platforms.

Standards are being looked at as the answer to many of these concerns. And, just as designers now embrace either VHDL or Verilog, they are anxiously awaiting the realization of analog/mixed-signal extensions of that language. In part, this is because they have already invested time becoming experts in one of these languages and have no real incentive to adopt the analog/mixed-signal extension of the one they don't already use.

While the division of designers currently using VHDL and Verilog tends to vary a little each year, VHDL has been consistently used more by system houses, was designed with a wider range of abstractions, and seems to have a much larger following in Europe. Verilog, on the other hand, tends to find more use on the IC side, bears closer allegiance to physical datatypes and hardware, and has a heavier following in the U.S. Ultimately, the analog/mixed-signal extensions of each will have to coexist. Toward that end, one of the goals of the organizations developing these standards is to ensure their interoperability through the creation of one advanced library format for use with both the analog/mixed-signal extensions of VHDL and Verilog. This effort is currently being undertaken by the OVI and VI (VHDL International), San Jose, Calif., working groups.

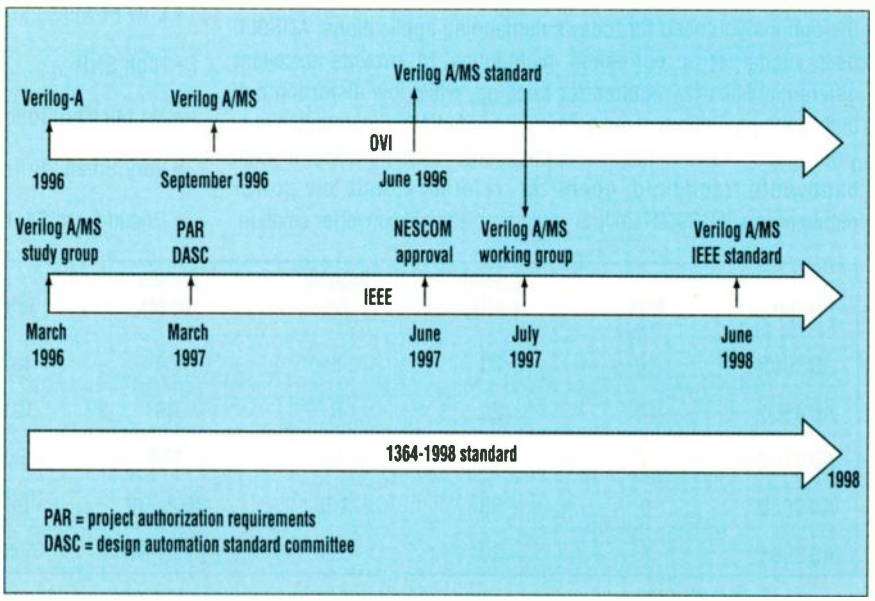
One of the questions that the standardization of analog HDL languages brings up is what will happen to the traditional roles of the analog and digital designers. The obvious question is whether standards existence will mean the obsolescence of the analog designer. The answer, of course, is "no." What it will mean is that design teams will be able to build better designs because the two sides, digital and analog, will be able to speak the same language. This does not mean, of course, that the digital designer will do analog design, or vice versa. Rather, the design paradigm will change such that they will be able to work more effectively together using better tool interfaces.

As Joel Alanis-Rodriguez, general manager, Analog/Mixed-Signal SSD-Simulation Business Unit, Mentor Graphics, explains, "Today's digital designer is not yet a mixed-signal designer. When intellectual property becomes available, this transition will occur, but very slowly. Rather, today's mixed-signal designer is an analog designer designing from the bottom-up using a schematic-based methodology. This approach, though, is not capable of responding to many problems early on in the design cycle. With standardized languages comes a shift from a schematic-based to a language-based methodology. This shift will allow the mixed-signal designer to do top-down design, as opposed to the bottom-up design currently practiced by many analog designers. With this approach, the designers will be able to anticipate problems early on, and effectively gives the designer the opportunity to do explorations right from the start."

Another issue yet to be resolved is that of intellectual property (IP). Standards will actually help enable the development of analog/mixed-signal IP. In a deep submicron world with increasingly complex designs, designers are forced to deliver products to market faster. IP and design reuse in such a scenario is crucial. Without the standards, it would be painstakingly difficult, if not impossible, to construct a design with multiple IP blocks from different vendors. If each block is based on a proprietary language, then bringing the blocks together to work as one device would be a huge problem. Either the designer can't do the design or the proprietary languages on which the IP blocks are based must each have front-end interfaces to one another. On the other hand, if the IP blocks are all based on a standardized language, then this would be a moot point, since component intercommunication would be assured.

Standards Benefits

It is obvious that behavioral languages will play a role in the proliferation of "mix and match" IP, as well as allowing the designer to perform system level architectural explorations. Organizations such as OVI and the IEEE, as proponents of the standards, are critical because they will provide the framework from which the analog/mixed-signal marketplace can be created, as well as from which all components at chip assembly can speak.



3. Both the OVI and IEEE Verilog A/MS efforts are considered complementary. With OVI's standard being used as the basis from which the IEEE working group can begin to put together its standard version, the EDA industry is assured that its requirements for such a standard will be seen in the final IEEE Verilog A/MS standard.

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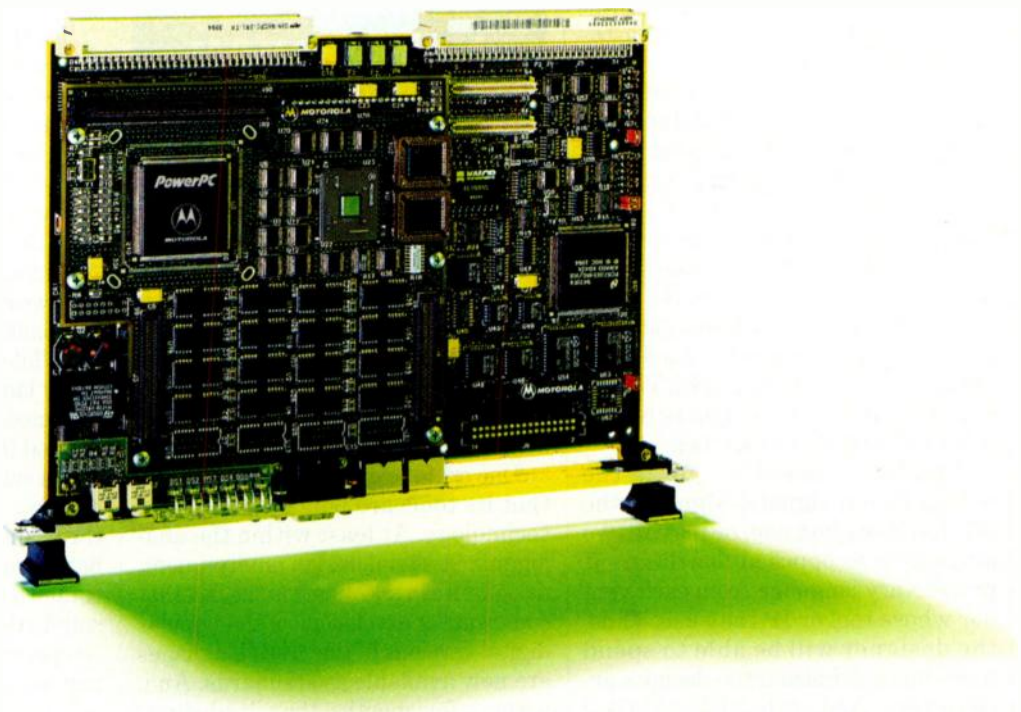

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The benefits of standardized languages have significant implications for the designer who uses them. Primarily, they offer portability, easy design and model interfaces, and interchangability. The designer's job will be easier because libraries can be moved from group to group, allowing reusability of platform products and cycle time reduction. Also, once a mature higher level language is adopted, the designer will be able to simulate full chips and design at a higher level of abstraction. This means that potential hook-up problems and architectural difficulties can be corrected early on in the design cycle when there is still time to make changes without significantly impacting design cost or time-to-market schedules.

Verilog and VHDL are two mature languages. As such, simulators currently exist for both. Consequently, any extensions to these languages would be based on a product that already exists. This means that the analog design environment could use the existing digital simulator for analog design. So, while today's designers must simulate the digital and analog blocks of a design separately, in the future, with Verilog A/MS, for example, designers will be able to simulate them together.

Another benefit for the analog/mixed-signal designer is the need to learn just one, or maybe two languages, as opposed to a different proprietary language from each vendor whose tool or IP they use. Thus, the designer will be able to spend more time optimizing the design's architecture. And, if the either Verilog or VHDL Is already being ued, learning the syntax of its analog/mixed-signal counterpart is considerably simpler then having to learn a proprietary language from the ground up.

While the benefits of standardized languages are significant, they should not be overestimated. The bottom line is that they will never be the answer to all of the issues being faced by the evolving analog/mixed-signal design area. In fact, they are a starting point from which a solid foundation of interoperable tools and solution can develop. But there are many areas that still need work. A higher degree of automation and library models development are just a few. Presently, there are little or no library models available for the analog extensions to the Verilog language. Mixed-signal extensions of Verilog and VHDL languages are just around the corner and will be faced with a similar problem.

Traditionally, specialists have been required to design the models for use by designers. The situation is a little different today with the Verilog and VHDL language extensions. No longer does the designer have to depend on the expert modeler for models. By using Verilog-A and VHDL-A, designers can now make their own models. Even then, most designers don't have the time to build the models and verify them well enough to use in their design work.

The landscape of the Electronic Design Automation (EDA) industry is changing drastically.

The Future

One critique of the EDA industry is that its tools are lagging behind its technology. At least within the analog/mixed-signal design environment, designers can take heart in the fact that some analog extensions of the popular digital versions of the HDL languages are now available as standards. And, within a few months, the mixed-signal extension of Verilog will be on the streets. While some would argue that it could be at least two to three years before the industry fully understands the behavior of the languages and eliminates all the bugs, it is a step in the right direction. Once in place, the standards are bound to spur a flurry of activity in the development of interoperable tools for the analog/mixed-signal design environment, as well as libraries and any other peripheral software that will be needed to optimally help designers ride the wave of IP, design reuse, and Hardware /Software (HW/SW) co-design and co-verification.

With the emergence of the standards in full swing, the question is what happens to the companies that are now offering proprietary language solutions. According to Maqsoodul Mannan, chairman of OVI, the bottom line is that "customers will have to make the choice between using a proprietary language that locks them into a particular language and models library, versus an open one." Viewlgoic's Graham Bell says, "Before the issue of proprietary versus nonproprietary languages ever gets resolved, the Verilog-A/MS and VHDL-A/MS languages will have to be able to solve some of the real problems facing designers. In the mean time, designers will continue to use the proprietary tools available to them now, in spite of any weaknesses."

DSM design and IP are two factors that will help to turn the popular opinion toward standards. But, as Graham points out, "only if they can begin to shed light on questions like will the designer have access to useable models, and will they allow synergy with IP such that the designer will have a clear understanding of how to incorporate and work with IP cores from other companies in a design."

While it may be difficult for proprietary languages to have engines general enough for widespread use, it is not beyond the realm of possibility to hope that a solution as simple as offering an interface from proprietary languages to the standards could allow a place for both. Proprietary languages could continue to fulfill a niche market, while standards could allow industry wide interoperability. In any case, it is important to know that the analog/mixed-signal design subset of the EDA industry is still early in the game. Many end-users don't even know what they want in terms of tools or languages. And, typical in the industry, all change is-driven by the end-user. Consequently, as they better understand what they want, user needs will drive the emergence of perhaps one or two languages, standardized or not, above the rest. Until then, with something as new as standards, it is unlikely that designers will settle on just one language.

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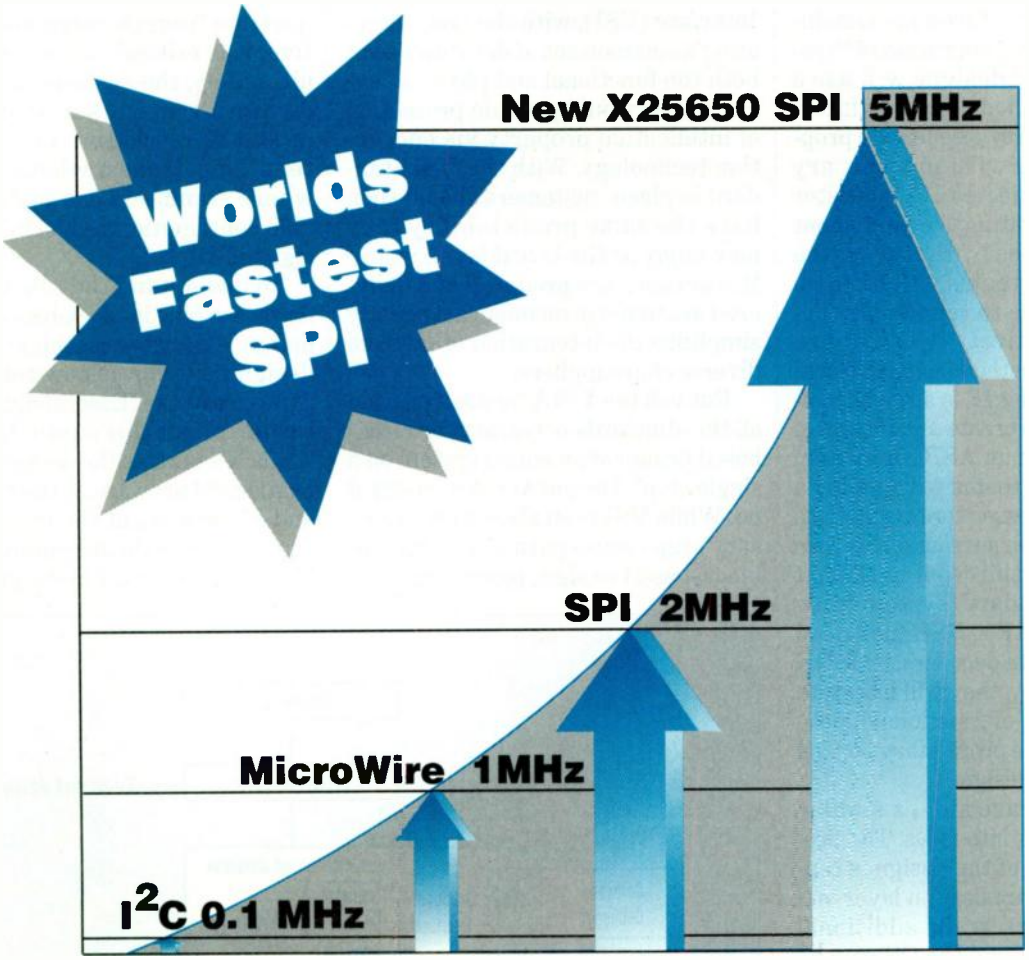

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EDA WATCH

Block-Based IP Standards For Chip Design Are Merely The Tip Of The Iceberg

It's now almost a foregone conclusion that a new generation of "system on a chip" designs will use a block-based methodology that incorporates third-party intellectual property (IP) along with proprietary blocks. With projected IC transistor capacities generating the equivalent of 40 million gates by the end of the decade, design teams will have no choice if they are to remain productive and competitive.

The general methodology for block-based design using IP is already coming into focus. To create and install an entire system on an ASIC or custom IC, most design teams will employ a third-party processor core to serve as the CPU and then surround this core with additional third-party IP that represents standard system functions, such as UART, USB (universal serial bus), Viterbi decoders, or ISDN interfaces. Finally, they will integrate an additional set of functional blocks that represent the proprietary portion of the hardware design.

On the software side, a similar process is coming into focus. The proprietary portion of the design is represented by the application layer and firmware drivers, while additional firmware drivers and the OS may be provided as IP by third parties. On the hardware side of block-based design, it is apparent that implementation is the true challenge.

Unless third-party IP blocks are accompanied by a well-defined and well understood set of deliverables, the challenges of system hardware integration become formidable. This is true both at the functional level, with issues such as interface protocols; and at the physical level, with issues such as clocking, testability, and power structures.

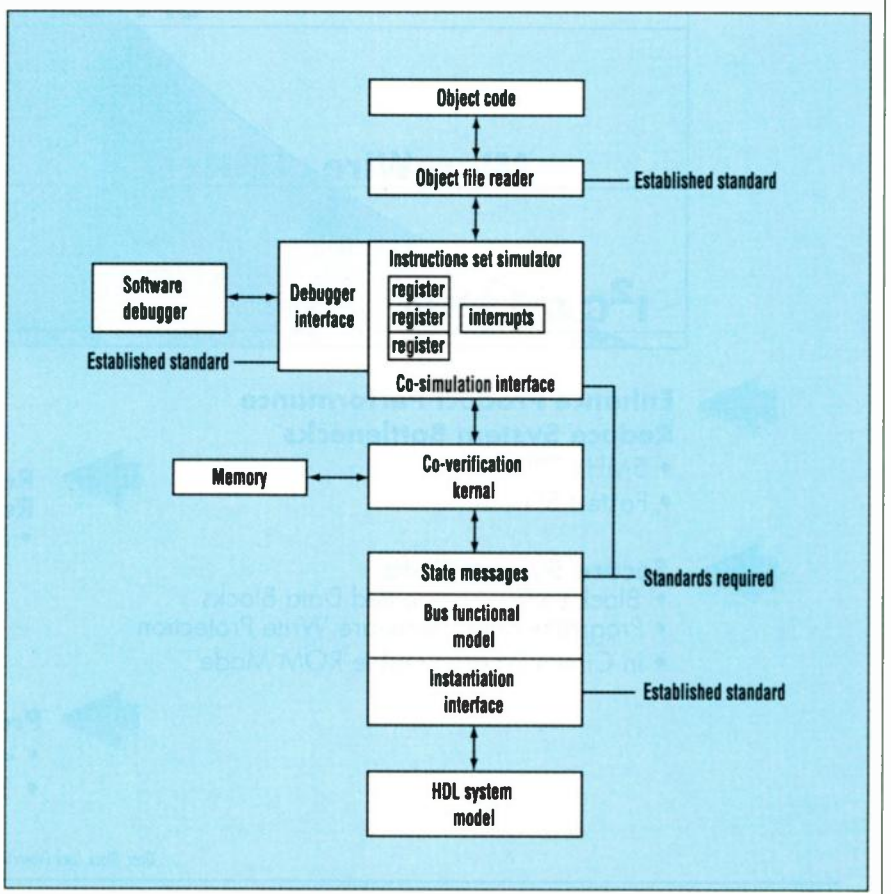
Toward IP Standards

To meet these challenges, the EDA, IP, Systems, and IC industries have formed a group called the the Virtual Socket Interface Alliance (VSIA), which is in the process of constructing a standard called the Virtual Socket Interface (VSI), with the goal of creating a common set of deliverables at both the functional and physical levels. It also would provide protection of intellectual property via encryption technology. With the VSI standard in place, customers should soon have the same predictability they now enjoy at the board level, where IC packages are produced and delivered in a uniform manner that greatly simplifies the integration of IP from diverse chip suppliers.

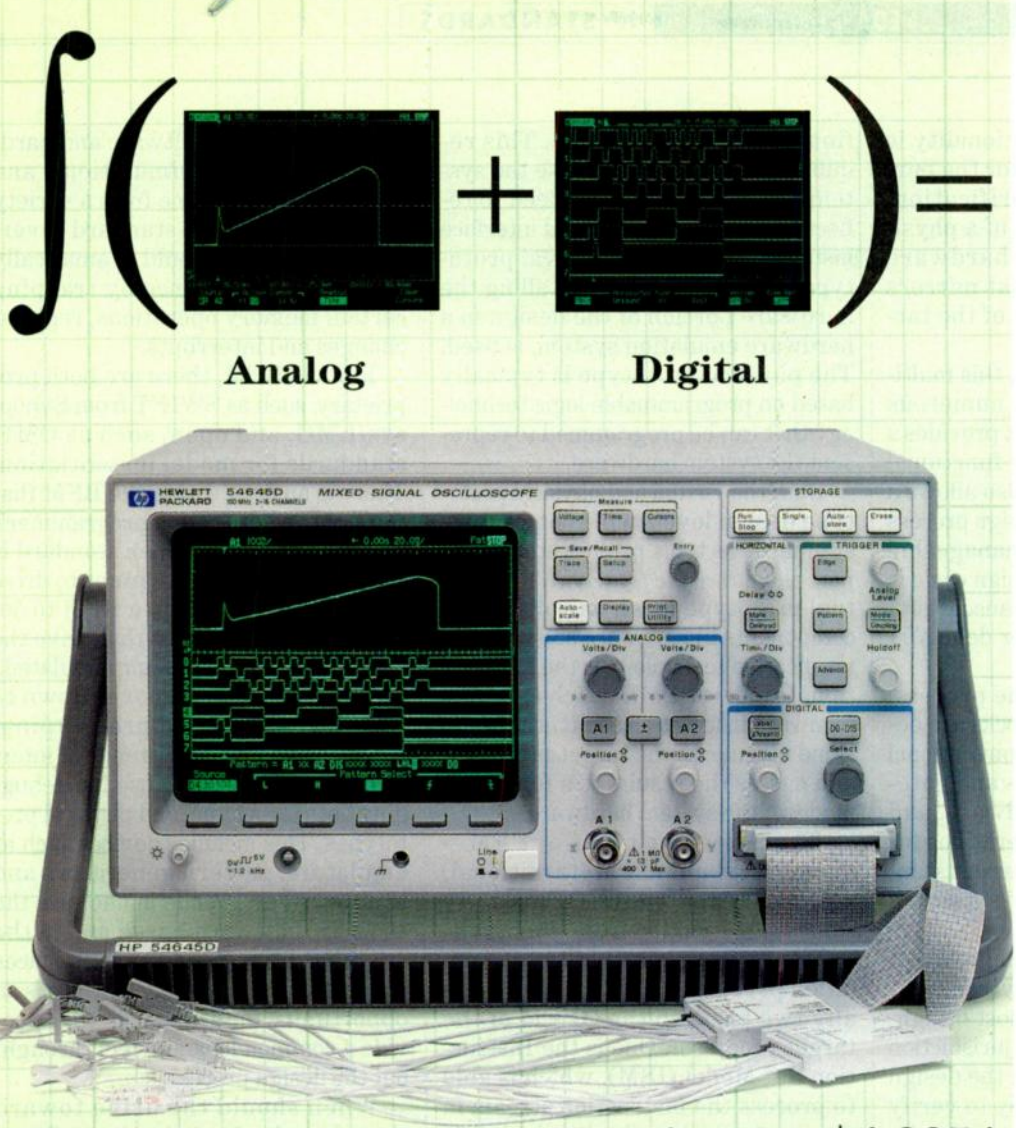
But will the VSIA by itself provide all the standards necessary for block-based design of an entire system on a single chip? The answer is a qualified no. While VSI is an absolutely necessary step on the path to productive block-based design, participation is predominantly from IP providers, EDA and semiconductor companies, where it addresses the obligation of IP suppliers/integrators to present a uniform solution to designers.

If one looks at the IP standards question from the systems perspective, it is critical to remember that ultimately, the systems architect is designing not a set of interconnected IC blocks, but an entire system. This opens a whole new area where standards can make a valuable contribution to block-based design via IP.

To understand the role that standards can play in block-based systems design, it is best to consider the overall design flow that is now coming into widespread use. Essentially, this flow can be broken down into three basic levels. The first is the design and verification of hardware at the block level and of software at the module level. The second is the assembly of these blocks into a virtual prototype, where



While some standards are currently available to address specific segments of the virtual prototyping environment for Intellectual Property, the development of a number of other standards, such as for the Bus Functional Model and the object code file, are crucial to a successful Intellectual Property-based design process.



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the entire system's functionality is represented in software for the purpose of analysis and verification. The third is the creation of a physical prototype through hardware emulation techniques that mirrors the on-chip functionality of the target system.

When properly applied, this multilevel approach produces numerous benefits. Most important, it provides a high probability of a fully functional chip on the first pass. It also allows a very large and complex design process to be broken down into manageable tasks. Also, the overall design cycle is reduced to a minimum because it provides an optimized path for debug/fix iterations.

At the first level of the process, hardware and software blocks are designed and verified using conventional techniques such as HDL- and gate-level simulation for hardware, and host-based debugging operations for software. At this level, current standards are adequate and are supported by a wide variety of tools.

At the next level, virtual prototyping, we encounter an environment that is relatively new to most designers and mostly beyond the jurisdiction of any standards. Early in the design cycle, there must be a way to verify that the embedded software under design will interact in a predictable manner with the system hardware—even though the chip-level hardware does not yet exist. Therefore, the entire system must be modeled and put through a process known as hardware/software co-verification. This level, a hybrid of emulation and simulation, is critical in several respects. It allows driver software to be verified in terms of its interaction with the hardware—before the application layer adds another level of complexity. It allows the design's various blocks of hardware IP to be exercised using stimulus that represents real system operation. And, it accelerates the design cycle because debugging cycles can progress without waiting for a physical prototype.

Real-World Prototyping

While virtual prototyping provides invaluable insight into low-level hardware/software interaction, it does not provide a complete picture of how the final system will operate. This requires the ability to exercise the system at speed or reduced speed to reflect real-world stimulus and interface issues. To do this, a physical prototype, accomplished by installing the hardware portion of the design in a hardware emulation system, is used. The physical prototype is typically based on programmable logic technology that can be programmed to represent the system hardware.

Both the virtual and physical prototype design levels will soon require standards as tools proliferate to support them *(see the figure)*. At the virtual prototype level, one of the key components in hardware/software co-verification technology is the full functional model (FFM), which executes firmware instruction sequences in the same manner as the target processor, and passes the results to a functional model of the system hardware.

There are two types of FFM—monolithic behavioral (traditional) and optimized FFM (OFFM). By separating function from timing, the OFFM dramatically increases simulation performance. There are actually two parts to the OFFM of the target processor. One is the Instruction Set Model (ISM), which is able to process the instruction stream in a manner consistent with the internal registers and logic units of the target processor. The second is the Bus Functional Model (BFM), which is able to convert internal processor states into the appropriate signals on the processor's external pins. In both cases, there is an opportunity to optimize HW/SW co-verification through standards.

In the case of the ISM, there are three potential areas for standards *(see the figure, again)*. One concerns the reading of the object code file representing the target processor instructions and data. Currently there are several separate standards for object file readers, such as COFF and IEEE 695. A second concerns the debugger interface, which handles command and control of ISM during debugging operations. There are at least two proprietary standards here, and an open standard would be desirable. A third covers the interface between the co-simulation kernal, which manages the interface between the software and hardware sides of the simulations, and ISM, which may come from a variety of sources. An API standard covering this interface could dramatically improve performance by trapping certain memory operations, register changes and interrupts.

For the BFM, there are both proprietary, such as SWIFT from Synopsys/LMG, and open, such as OMF, standards for model instantiation. There is an area within the BFM that requires an application programmer's interface (API). An open standard is required to allow C programs to drive stimulus messages into a BFM to define the state messages that drive the pins of the processor being simulated.

When the design moves down to the level of physical prototyping, there should be a consistency of interface between the tools used in debugging both the virtual and physical prototypes. This includes devices such as emulators, pattern generators and logic analyzers. While in one case the tools are software-based and in the other hardware-based, the interfaces are both software-based, so there is an opportunity for standards that provide a common look and feel throughout the design process.

When should the drive toward these standards begin place? Given the inevitably slow pace of standards development in the past, with all its trade-offs and compromises, the best time is probably yesterday. System-on-a-chip designs are already moving out of the early-adopter phase of development and into the mainstream, so the impact of standards in this area will soon be substantial. New prototyping methodologies are too important for improving productivity to delay the standards process. Unless standards for prototyping are quickly enacted, the system design process will be severely hobbled by a lack of coherent methodologies. Commitment and participation by systems designers is absolutely critical in an effort to drive IP standards within VSIA.

Contributed by Brian Barrera, Director of Marketing, Inventra IP Business Unit, Mentor Graphics Corporation. For further information on this topic, contact the author at brian_@mentorg.com.

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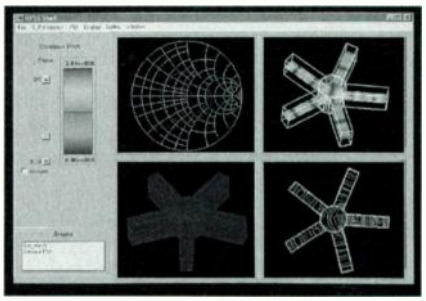
PRODUCT FEATURE

Structure Simulator Boasts Improved Speed And Advanced Drawing Environment

The latest version of HP EESOF's High-Frequency Structure Simulator, HP HFSS5.0, helps designers of high-frequency circuits and machined components achieve faster, more accurate simulation results. Able to model arbitrarily shaped, passive 3D structures, the tool is well suited for electromagnetic (EM) modeling applications such as antenna, circuit, and high-speed digital circuit designs. Most notable of the tool's features is tat it delivers, on average, 10X more speed (it has the potential to perform even faster), and requires 50% less memory than its predecessor.

These capabilities are, in part, due to improvements in the engine technology. The tool's 2D and 3D simulation and mesh engines are based on a completely new design that utilizes the finite element method (FEM). This method allows large, arbitrarily shaped 3D structures to be subdivided into smaller, more easily manageable, finite-sized elements. Using Maxwell's equations, the electromagnetic interactions



between each of the elements are calculated. The result is a complete representation of the structure's electromagnetic field, along with its S-parameters.

An improvement made to the simulation engine's meshing algorithm also contributed to the tool's improved accuracy, speed, and memory requirement. As opposed to previous versions of the tool, HP HFSS5.0 uses fewer tetrahedrons, and thus fewer subdivisions, in its FEM. Consequently, the resulting mesh is of much higher quality.

Another feature of the HP HFSS5.0 tool is a completely new drawing environment based on the industry standard AutoCAD software package. This HP-customized environment offers richer drawing capabilities, enabling designers to draw structures not previously feasible. Individual solids can be created from the Solid Model Parts Library, and a single solid can be created from multiple solids. Once the structures are created, designers can actually see through the structure and move it around without having to recalculate the field. The user can even reposition the structure without losing filed plots or animation. Other features include user-settable port excitation magnitudes and phases, as well as broader file compatibility and transla-

(continued on page 81)

PRODUCT FEATURE

(continued from page 80)
tion with other 3D drawing tools.

Other improvements to the tool, such as a tighter integration between its software modules, offers an efficiency improvement. An increase in the tool's accuracy comes from improvements to the fast-frequency sweep capability and the addition of a library of standard parametrized building blocks and complex shapes.

HP HFSS5.0 is compatible with HP, Sun, and IBM platforms, as well as with the PC on both Microsoft Windows 95 and Microsoft Windows NT operating systems. The tool offers easy translation between Unix and the PC. Cost is $43,000.

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Modeling Tool Offers Complex Test Bench Modeling, Advanced Protocol Capabilities

Designers today face ever-tougher system-design and verification challenges. In steps the Quickbench 2.0, which is a visual testbench modeling tool for Verilog and VHDL users that creates dynamic, self-checking bus-functional verification models (BFM) from timing-diagram specifications. The models, which can be generated in either Verilog or VHDL code, are derived from a specification. As a result, prior to the start of the design, they provide an accurate representation that's guaranteed to match the design requirements. These models then can be used to verify HDL designs during simulation.

With version 2.0 of the Quickbench tool comes a number of features that provide users with greater flexibility in designing complex test-bench models. Support of modeling protocols that contain repeating elements, for example, reduces the complexity of a diagram with multiple repeating sequences.

The repeating elements are created by adding specifying loop objects to timing diagrams. The user is free to specify a variety of parameters associated with the repeating elements, such as the number of times a loop is repeated, repeating a loop while a Boolean condition holds true, repeating a loop until a specified input event occurs, or repeating a loop forever. Nested loops, wait and loop combinations, using loops as conditional branches, control over whether an event occurs inside or outside of a loop, and measuring timing constraints between loop iterations also are possible.

With Quickbench 2.0's runtime timing control feature, users can model various timing conditions during the same simulation run or model asyn-

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PRODUCT FEATURE

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chronous protocols, which require detailed timing control. Designers treating timing and logic simulation separately can use default timing values during the simulation, while at the same time retain full timing details during timing analysis.

Quickbench 2.0 offers a number of additional test bench tools than its predecessor. A Design Component function, for example, allows designers to use components that don't have associated Quickbench models. A Copy/Import Component dialog function enables component port definitions with a Quickbench-defined file format to be imported into the Quickbench environment. Both tools can be used to automatically create test-bench component port lists given the Verilog or VHDL code for a design. In addition, the development of top-level test-bench files and the importing of port definitions from a design have been fully automated.

Another new feature of the Quickbench 2.0 offering are changes to the code so that it contains fewer processes and no delay triggers. To further break down the complexity of the code and allow designers to better understand the diagrams created, comment lines are included along with the generated HDL code.

Because Quickbench 2.0 is a specification-driven verification tool, it gives designers the capability to incorporate Intellectual Property (IP) blocks into their designs. The tool also allows for design exploration, since the simulation can be stopped when an error in the design occurs.

Quickbench 2.0 is available on HP and Sun workstations, as well as PCs equipped with Windows 3.1, Windows NT, or Windows 95 operating systems. Now shipping, the tool costs $10,000 for a single computer version, and $15,000 for a floating version. It comes free of charge to existing Quickbench owners who are part of the company's annual support option.

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PRODUCT FEATURE

HDL Graphical Entry Tool Enables Easier Generation Of Synthesizable HDL Code

At the top of most designers' wish lists would be an easy-to-use powerful EDA tool that's interoperable with other tools. Attempting to fulfill those needs, Mentor Graphics, developed an automated hardware-description-language (HDL) graphical design entry tool that offers ease of use with many special features to ensure tool flexibility. Moreover, with the push of a button, it can connect to all leading synthesis, simulation, and hardware/software coverification tools on the market.

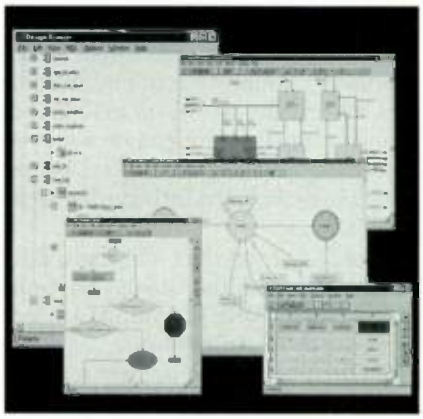
The tool, called Renoir, completely replaces the company's existing System Architect tool for use in the capture of high-level design and functional behavior of ICs. It operates by taking in higher levels of abstraction than were previously possible. In turn, it's able to provide automatic rapid HDL generation that's VHDL/Verilog-ready for simulation and synthesis.

Designers will reap a number of benefits by working at higher levels of abstraction. These benefits include the ability to investigate architectural options or conduct explorations, as well as improved design-team communication.

Whether operating on a Unix or PC, Renoir offers a true windows look and feel. This ensures that designers can share files between the platforms with complete compatibility. And, because Windows is a familiar environment to most designers, the tool's functions are easy to understand, with little or no learning curve. Intuitive, context-sensitive, on-line help documentation, and tutorials add to the tool's ease of use.

With Renoir's diagramming and editing tools, HDL code can be generated quickly. Higher-level functions such as creation and modification, and processing of ECOs and HDL debug functions, can be processed faster than with conventional text editors.

The tools flow-chart editor enables



designers to set the start and end, action, decision, wait, and loops. Truth tables can be used to compare any number of conditions to determine how modifications to the code will af-

(continued on page 84)

PRODUCT FEATURE

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fect the output editor. And, a library and hierarchy browser help to provide a quick graphical overview of the design's hierarchy.

Renoir also offers integrated online checking of HDL fragments for syntax in any HDL. When a syntax error is discovered, an error report is immediately generated, telling designers where the problem is located. Consequently, they can be assured that their HDL code is correct before they move forward into synthesis or simulation.

The Renoir product offering is fully compatible with the Quality Systems & Software (QSS) Dynamic Object Oriented Requirements System (DOORS)—a multi-platform requirements management and traceability system supporting real-time communication between PC and Unix development environments. With this compatibility, designers can capture and trace requirements throughout the entire design process.

Renoir's what-if and impact analyses enables users to evaluate the design modifications in real time. This assures that the original design intent and specifications are maintained at all times.

In addition, it supports any of today's text editors and comes in several flexible, modular configurations, depending on the users specific needs.The complete Renoir solution includes both the Renoir State and Renoir Block editors, a flow chart, truth table, symbol editors and the design and hierarchy browser.

Renoir State and Renoir Block are both standalone editors. Renoir State is a state-machine editor used to represent the control requirements of either part or all of a system. It offers support for both concurrent and hierarchical state machines, along with Mealy, Moore, and mixed machines. Renoir Block is a block editor that provides a logical schematic that includes components, blocks, buses, signals, and connectors. By using HDL text objects, any valid HDL can be added to a block diagram, or can be used for signal-type conversion.

The tool comes bundled with QuickHDL-VHDL, known as Renoir Palette for VHDL, and QuickHDL-VLOG, known as Renoir Palette for Verilog. Additionally, there's QuickHDL-VHDL and QuickHDL-VLOG, which are also referred to as Renoir Palette.

Renoir comes on either a Unix or Windows NT/95 platform, and supports both Verilog and VHDL for one price of $20,000. The Renoir State and Renoir Block standalone tools can be purchased for $5000 each. Renoir Palette for Verilog and Renoir Palette for VHDL cost $36,500 apiece. Renoir Palette sells for $54,000. A free, fully functional, evaluation version of the Renoir tool can be downloaded at http://www.renoir.com.

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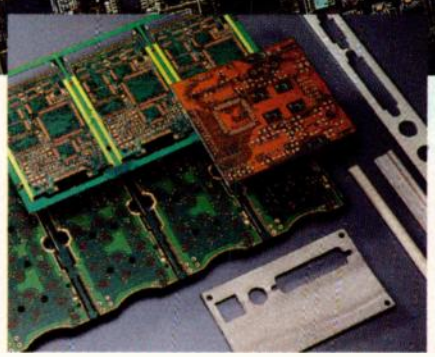

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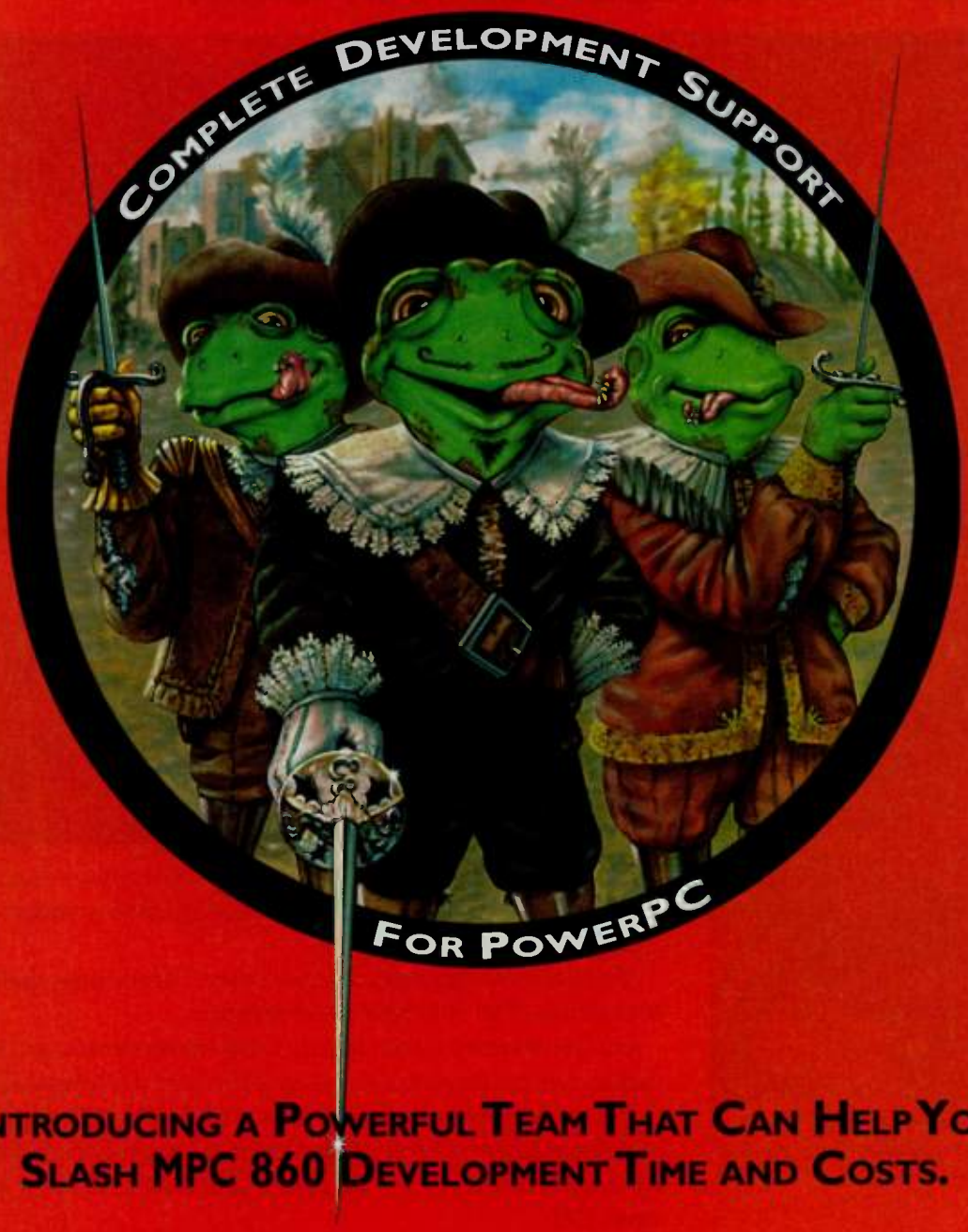

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Internet Protocols Migrate To Silicon For Networking Devices

Moving Internet Standards Onto ASICs Will Bring The "Internet Toaster" To A Variety Of Consumer Applications.

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Internet technology is poised to become a household phenomenon in more ways than one in the near future. That means much more than just e-mail in every home. The alphabet soup that has become the glue that holds the Internet together—Transmission Control Protocol/Internet Protocol (TCP/IP), Simple Network Management Protocol (SNMP), Remote Monitoring (RMON), and hypertext transfer protocol (HTTP)—is rapidly being harnessed as part of the silicon that drives everyday household appliances. These networking protocols are no longer just for networking applications, but rather for networked devices. To express it more accurately, the engineering world is redefining the concept of "the network."

Once upon a time, the term "computer network" meant a local area network or enterprise network consisting of several standalone computing boxes, each interconnected by cable, and each performing a specific function (e.g., server, client, router, hub, bridge, etc.). These same computer networks also ran on their own proprietary operating systems, whether it was a flavor of UNIX, Novell NetWare, or some other system. Even then, the Internet standards defined by the Internet Engineering Task Force (IETF) were the only open protocols available to interconnect these proprietary network systems.

Today, Internet standards are being harnessed in place of proprietary network operating systems to create corporate Intranets, little mini-Internets whose universe only extends to the corporate firewall. TCP/IP which was once used as a translation protocol, is now used in place of proprietary network operating systems as a universally compatible networking protocol. The fact that Microsoft's Windows 95 includes TCP/IP as part of the operating system demonstrates how TCP/IP has become a desktop standard. Internet standards and protocols are slowly displacing proprietary computer technology, tearing down the electronic tower of Babel that used to characterize computer networking, improving commerce and global communications.

And as these standards have stabilized and become the network fabric, they have driven new layers of network applications and protocols. TCP/IP, SNMP, HTTP, and RMON are all being embedded in computer silicon, forming a new breed of "nano-networks; deeply embedded protocols that operate within the network silicon to preprocess and offload the host MPU. The trend is to siliconize the more traditional bus-oriented network devices, for example between the CPU and the peripheral chips and are physically nothing more than traces on the circuit board.

The first phase of this migration is to embed networking standards like TCP/IP and portions of SNMP into the silicon ASIC itself. Once this is done, some of the common protocols used in World Wide Web communications will be implemented in silicon. This design will simplify the integration of hardware and software, reduce time to market, and reduce the cost of web-enabled devices. Finally, real-time Java applets will be created to dynamically customize the personality, or functionality of silicon. The end result will be a new era of consumer applications that rely extensively on Internet technology that is embedded in silicon.

Silicon-based computer networks are already emerging, although most consumers don't realize it. Many automobiles have four or five computer networks under the hood. Mechanics are using computer monitors to read data from embedded SNMP agents in the ignition system. BMW aficionados are hiring programmers to reverse-engineer the networks in their cars to tweak the performance. SNMP is used to track pay-per-view movies on Digital Satellite Systems. To paraphrase Sun Microsystems, the network has not only become the computer, the network is the chip. The age of the "Toaster Control Protocol" has arrived!

Embedding SNMP Technology

The first evolutionary milestone in embedding the Internet has been to create a new generation of networking chips that include TCP/IP, RMON, and SNMP as part of the silicon. Embedded TCP/IP and SNMP agents have been around for some time in the form of software. Most

real-time, embedded-operating-system suppliers, such as Integrated Systems, Inc., (Sunnyvale, Calif.) and Wind River Systems (Alameda, Calif.), have an embedded TCP/IP protocol stack as part of the real-time OS. Using the embedded TCP/IP, real-time applications embedded in the silicon can interface with other network devices and graphical user interfaces.

When migrating TCP/IP or any Internet protocol to silicon, the implementation has to have a small enough memory footprint to make it ROMable. It also has to be fully compliant with the standard in order to be useful. Again, most real-time OS suppliers have a standalone embedded protocol stack, and in some cases, offer a complete, embeddable IP implementation which includes subnet masks and routing, TCP, UDP, and other Internet protocols for more extensive networking support.

Once the TCP/IP stack is included as part of the chip set to handle communications, an embedded SNMP agent can be used to view and control network devices. SNMP typically operates in an agent/manager architecture, where the agent resides at the local device and reports to an SNMP Network Management Station (NMS), such as Hewlett-Packard's HP OpenView or Sun Microsystems' SunNet Manager *(Fig. 1)*. SNMP agents are responsible for gathering statistics and other data concerningthe local network device, then transmitting that information back to the NMS for final processing.

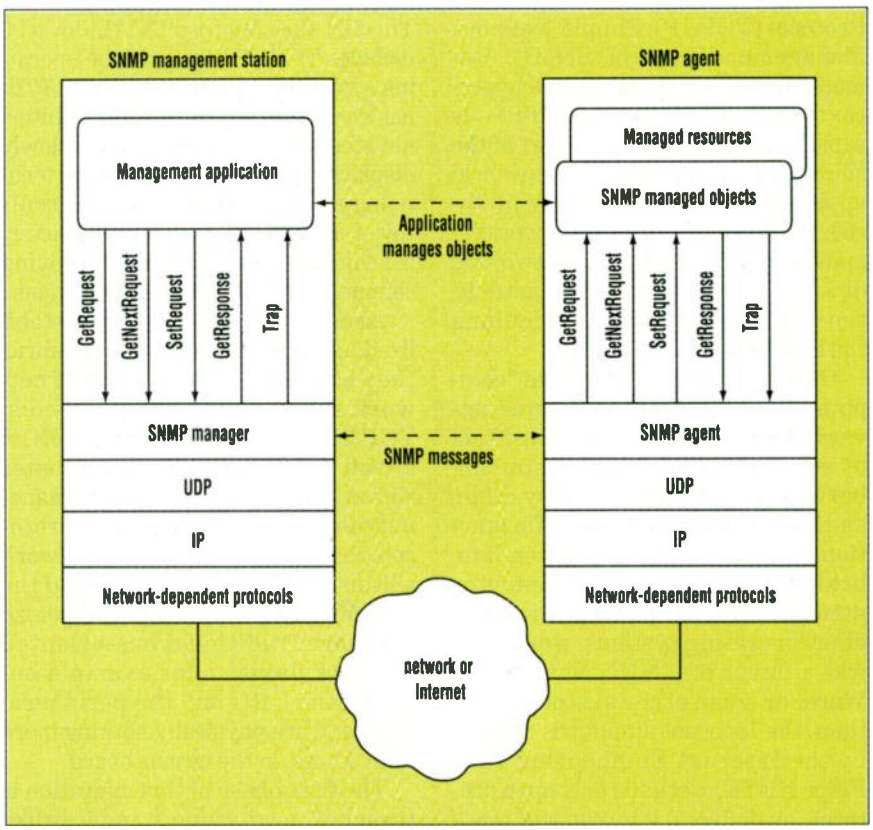
Traditionally, SNMP agents are delivered as software that is loaded into a network device, residing in either RAM or in some cases in flash or EEPROM memory. The advantage of using modifiable memory, such as flash or EEPROM, is that if the implementation changes, it's a simple matter to upgrade the network device. However, the SNMP standard is both compact and stable, so it is practical to implement data gathering right in the network silicon. The challenge is to make the agent small enough to keep the silicon footprint small. A typical real-time SNMP agent can be implemented in less than 46 kbytes if it is SNMPv1 (the original version of SNMP), or in 95 kbytes if it is bilingual and supports both original SNMPv1 and the current SNMPv2c standards.

Silicon-based computer networks are already emerging, although consumers don't know it.

To optimize the embedded SNMP agent structure, it's best to implement a hierarchical master/agent management architecture. If comprehensive SNMP support is needed, a Monolithic Agent may be implemented. Subagents, which are smaller SNMP data gathering engines that are supported by master agents, also can be implemented. Master Agents are responsible for one or more subagents, gathering SNMP data from multiple sources and reporting back to the NMS. Proxy Agents perform tasks requested by other agents.

By using a hierarchical master/agent architecture, some of the data preprocessing can be off-loaded onto the chips in hubs, routers, and other devices. The results are presented to a master SNMP agent that can then complete the processing. Each subagent is given control of a specific network-management task and, processes SNMP requests locally, then reports to the master agent which in turn reports to a NMS. The master agent automatically receives updated information about any device as its characteristics change.

With an SNMP agent embedded in silicon, SNMP transactions can be used for a variety of innovative applications. In the case of networking hardware, an embedded SNMP can be used to handle remote diagnostics in a wide area network, system configuration, and other applications. For example, if a network manager has to support a remote office network, he or she can use data provided from an embedded SNMP agent at the router that connects the remote office to an ISDN dial-up line, for troubleshooting or configuration. SNMP has been used as self-contained system-management



1. SNMP (Simple Network Management Protocol) uses an agent/manager structure where the agent is responsible for gathering statistics and information about a local object. It then forwards that information to the SNMP Management Station.

software for high-performance photocopy machines. The well-defined messaging and robust reporting allows a number of the different copier components to offload error and status conditions to a single management card that processes the information and makes appropriate decisions. The advantage of using an embedded SNMP agent is that it requires no configuration or maintenance; the hardware is typically plug and play.

RMON Comes Of Age

Remote Monitoring (RMON) provides a standard management information base (MIB) methodology to collect, sort, and provide meaningful information regarding the status of any device on a network segment. RMON has proven most useful for creating historical information about network performance. For example, patterns of operation can be used to predict network behavior and facilitate preventive maintenance of network devices. Embedding RMON support in network silicon is a much more complex problem, because the data gathering defined by the RMON standard is far more extensive.

RMON was designed to deliver an effective, efficient means of monitoring the behavior of subnetworks without imposing an undue burden on network agents or network management stations. RMON is basically structured as a MIB extension to SNMP, giving network managers information about activity from RMON probes situated throughout the network. However, the RMON standard defines nine separate groups of information that can be accessed, potentially making RMON data gathering very bandwidth-intensive on any network. To minimize network overhead and make it practical to siliconize RMON data gathering, developers have to decide which data groups should be embedded in silicon.

First, let's review the nine RMON data groups:

1. Statistics—Collects general, low-level traffic information, such as number of packets, bytes, errors, etc.

2. History—Records periodic statistical samples for a LAN segment over a user-defined time interval using information from the Statistics group.

3. Alarm—Defines either absolute or delta value thresholds on existing MIB objects and monitors those objects. If the thresholds are exceeded, an alarm is generated.

4. Host—Gathers basic information about the media access control (MAC) addresses on a network and various types of network traffic by reading traffic flowing to and from the host.

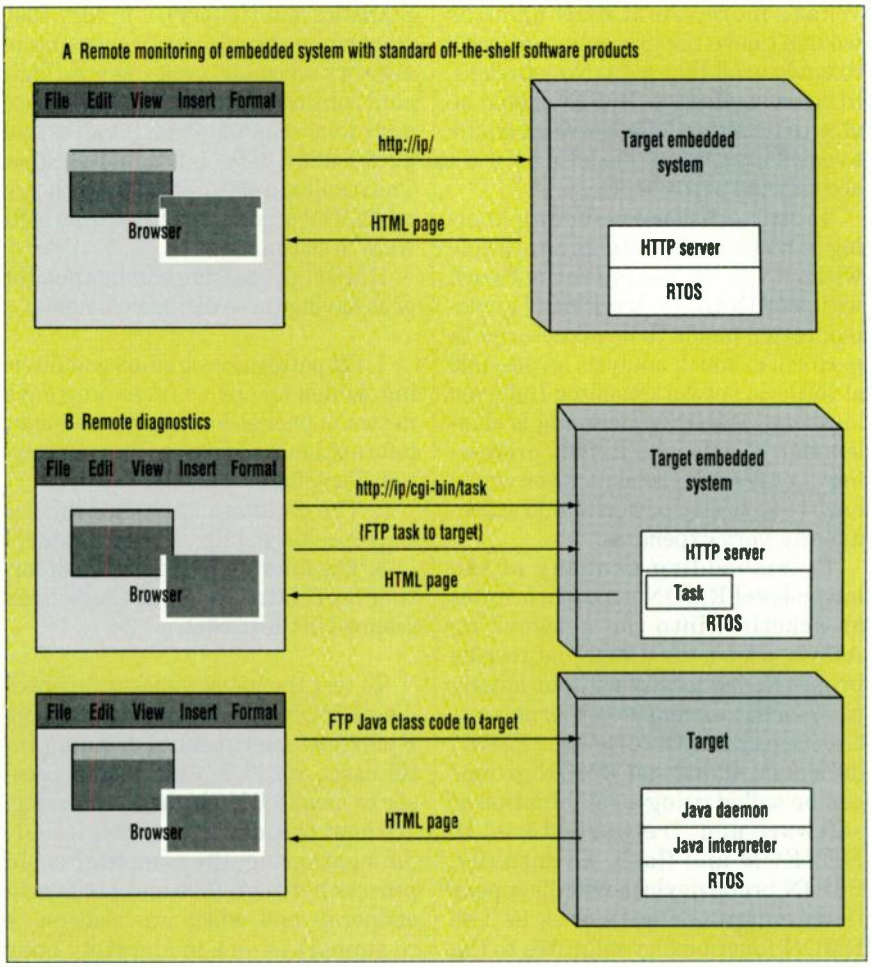
5. Host Top N—Prepares a report of the top N hosts, as ordered by one of the host group statistics.

6. Matrix—Collects basic statistics about transactions among MAC addresses of individual devices so the manager can retrieve information from any pair of addresses and show them in matrix form.

7. Filter—Creates channels based on arbitrary filters. The RMON monitor can capture all packets that meet the filter, or record statistics about those packets.

8. Packet Capture—Captures all or part of a packet contained on a channel and forwards it to a management console.

9. Event—Controls the generation and notification of events from the agent. Events can be ignored, logged, and/or used to generate a trap.



2. Embedding SNMP and HTTP in silicon (a) allows users to perform remote monitoring using any off-the-shelf HTTP browser (b). Once SNMP and HTTP are embeddable in ASIC silicon, automated systems can be created that not only diagnose a problem, but implement a follow-up process through a Java script to address the problem, all through a conventional Web browser.

It would be impractical to create an embedded RMON application that supports all nine groups. The memory requirements would make a comprehensive nine-group RMON implementation in silicon impossible. More importantly, RMON is a very powerful extension to SNMP and very data intensive. If the faucet on an RMON probe gathering all the statistics for all nine groups were opened, the flood of data traffic would fill the network pipeline and effectively stop the flow of any useful packet information.

What's more, the RMON monitor wouldn't have the processing capacity to analyze all that data. Nonetheless, to be truly effective, RMON should be able to monitor all the network traffic to develop a realistic model of network activity and performance.

To strike a balance between gathering as much statistical data as possible without overwhelming the network with RMON traffic, the RMON implementation needs to be structured to perform as much analysis as possible at the local network monitor. But even localizing RMON processing is challenging, because the RMON processing engine at the local monitor would have to be pretty powerful, and subsequently, very expensive.

By embedding as many of the lower-level RMON group processes as practical into the networking ASICs, a lot of the RMON data can be preprocessed locally without having to resort to expensive external processing engines. Once the core RMON data is in, additional RMON groups can be called using a combination of software and firmware stored in EEPROM and flash. Eventually, RMON probe devices will disappear from computer networks as the RMON functionality migrates to the network silicon in hubs, switches, and other networking devices. In other words, the hub or switch will become the RMON probe.

A study of the processing loops within RMON reveals that in the traditional RMON groups (principally Statistics and History), it is very easy to perform simple preprocessing in network silicon by creating gate logic additions to the network chip. These additions scan network packets and perform low-level bit manipulations. The result is a 40% offloading of the total RMON processing cycles from software to silicon.

RMON processing can be thought of as having three distinct elements:

1. Bit pattern recognition and filtering, which comprises scanning each network packet looking for relevant information, and passing that information along for processing.
2. The database function, which is the repository of the gathered data.
3. The filtering function, which further correlates the data that's been scanned in the packet.

To test the effectiveness of embedding RMON preprocessing in silicon, Epilogue experimented using an Intel-based 80286, 8-MHz microprocessor to handle RMON data processing. Without the silicon-assisted RMON data gathering, the computer could process between 1000 and 1100 packets per second, which was inadequate to support even a moderately busy network. With data preprocessing embedded in silicon, RMON processing speeds jumped to 14,880 packets per second, the effective speed of Ethernet. In addition to the 40% performance improvement, embedding RMON preprocessing saves money, since less expensive CPUs can be used for RMON support.

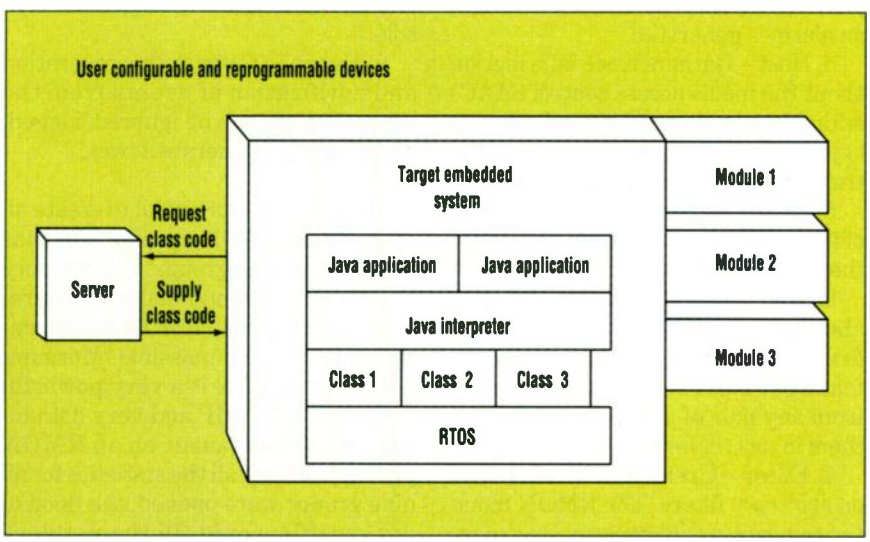
To bring RMON to the new breed of fast networking technologies such as ATM and 100BASE-T, it is crucial to embed RMON data gathering. The added boost in speed that siliconizing the History and Statistics groups brings is the only way that the probe can process enough RMON data to keep up with the higher packet rates. Higher data rates mean faster propagation of errors, so more data has to be processed to isolate errors. In fact, the amount of data required for effective RMON monitoring of fast-packet networks grows exponentially, and the cost of the hardware to process the data grows as well. Siliconizing RMON data gathering is the only cost-effective way to bring RMON to fast-packet networking.

Embedded Devices On The Web

HTTP and hypertext markup language (HTML) are the lingua franca of the World Wide Web. HTTP-based network management has been gaining rapid acceptance for applications that have traditionally been reserved for SNMP. Network hardware manufacturers like Cisco Systems, Hewlett-Packard, and Tivoli Systems have already started adding HTML-based interfaces to their hubs, routers, and switches. These vendors have found it much easier and less expensive to create their own HTML device-management interfaces that plug right into a web browser, than to write proprietary interface software.

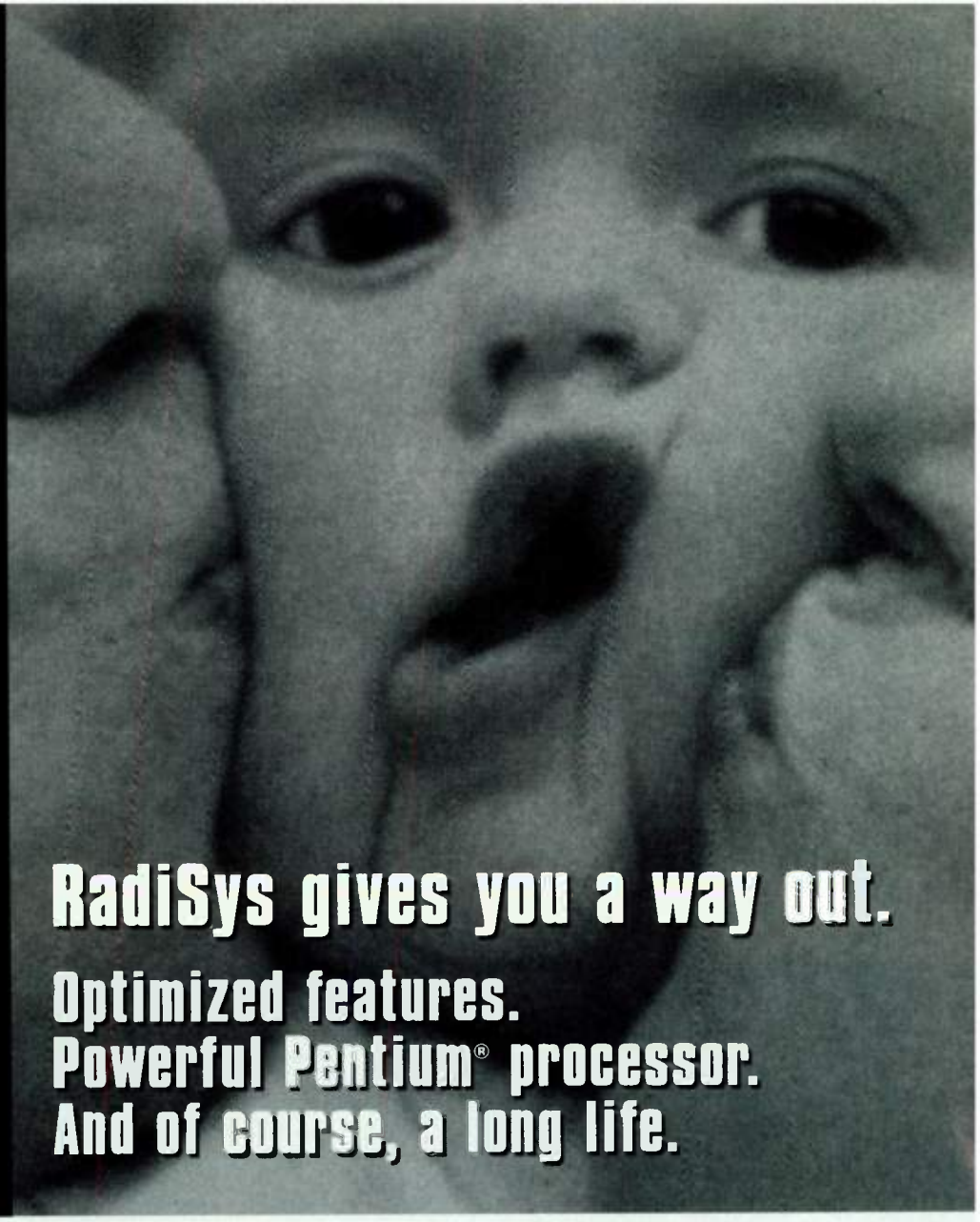
Likewise, device configuration is moving to HTTP. In the past, network devices were configured using sets of dip switches to configure such metrics as address, port specifications, and other tunable parameters. These switches were replaced by custom-written software embedded into the device and accessible from an RS-232 port, resulting in the same functionality with a better interface. Now, thanks to web technology, manufacturers are embedding small, dedicated HTTP servers, providing a truly user-friendly configuration interface accessible from any Web browser.

The next logical step is to extend the network-management capabilities of SNMP and RMON by adding an HTML interface. The ideal marriage



3. Embedding SNMP, HTTP, and Java allows designers to dynamically change the behavior of the embedded device, making it user-configurable and reprogrammable.

IN A TIGHT SPOT?



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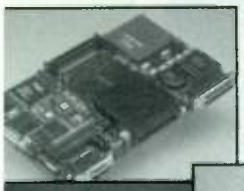

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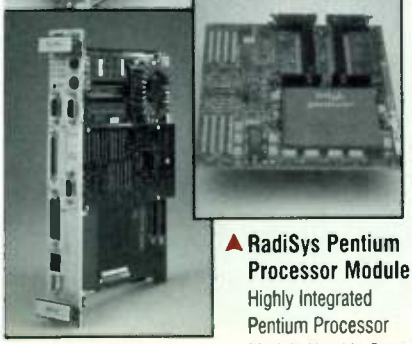
Pentium Processor Based Multimedia Computer



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intel inside
pentium PROCESSOR

of the web and network management will use SNMP agents in local network devices for data collection, web browsers for data display, Java scripting for intelligence, and HTML or some other protocol as a standardized format to port SNMP data between platforms. RMON will be used for application-specific monitoring.

The reason HTTP-based network administration looks so attractive is the flexibility and the potential savings it offers. Traditionally, SNMP network management station (NMS) solutions like OpenView and SunNet Manager are expensive software solutions that require sophisticated (ergo expensive) computing hardware. By integrating SNMP and HTML technologies, network managers can now perform routine administration tasks using any off-the-shelf browser running on any PC *(Fig. 2)*.

Some predict that by supplementing traditional NMS solutions with HTTP-based network management solutions, customers can save 50% or more on network management. Not only are the cost savings substantial, but customers gain additional benefits such as dial-up management access through the Internet for remote monitoring of network devices.

However, this solution does not mean that web-based network management will supplant SNMP and RMON solutions. Java applets and proprietary web-based management interfaces have their place, but the SNMP environment is too robust, too well-defined, and too well-established to be eclipsed by emerging web management technology. What will emerge is a new set of mid-level, web-based applications that bring SNMP and HTML technology together to provide more limited network management capabilities.

And just as SNMP and RMON are migrating to silicon, so is HTTP. Embeddable HTTP servers make it possible for network devices to act as fully functioning HTTP severs that are accessible using any web browser. So, combining an embedded SNMP interpreter solution with an embedded HTTP server, allows the use of Netscape Navigator, Microsoft Explorer, Mosaic, or any other standards-based web browser for network management and device configuration.

When embedding both SNMP and HTML in silicon, there are some issues to keep in mind. A native HTTP server will make it possible to run specific SNMP routines—Gets, Sets, GetBulk, Traps, etc.—for a specified URL. That way devices can be accessed using requests from any web browser, just as though it were a conventional web site. A certain amount of system security is built in to the HTTP standard, so all transactions can be password protected.

It is important to ensure that the embedded-HTTP server can act as an SNMP-to-HTML translator, supporting legacy SNMP technology. By generating SNMP requests as HTML and converting HTML responses back to SNMP requests, embedded network management solutions are universally compatible.

HTTP Joins Real-Time Java

The next stage of evolution in this embedded network-management scenario is creating Java applets to control the devices which now have embedded SNMP and HTTP. In fact, Java was originally created by Sun Microsystems to facilitate the development of embedded-systems software, although it was immediately adapted for web programming because it is flexible, portable, and supportive of distributed applications with a high-level GUI.

Java is particularly well-suited for embedded applications for a variety of reasons *(Fig. 3)*. Java has a compact run-time system with a basic interpreter that is about 40 kbytes, and basic libraries and thread support adding about 175 kbytes. Java applications are more portable since Java specifies a machine-independent, intermediate byte-code that can be transferred between network nodes, and is compiled on-demand by a local Java run-time environment. It is adaptable to changing environments, since code modules are downloaded dynamically. It is secure, with built-in protection against viruses and tampering. Additionally, it incorporates support for just-in-time translation of portable byte codes to the native machine language of the local Java host. The second time such a routine runs, it runs as native code. What all this means is that Java offers developers a robust and versatile platform for embedded applications. Its compact executables will make it possible to embed Java applets almost anywhere.

Since Java applets first translate Java programs into a portable, standard byte-code representation, that byte code can be processed by any virtual machine. As far as Java is concerned, a virtual machine can be any software system capable of understanding and executing the Java byte-code representation. Currently, Java uses an interpreter to execute the byte codes.

The Java virtual-machine code will become part of the computer silicon, as will many of the class libraries that support Java applications. As virtual-machine functionality moves into silicon, it will be easier to perform prefetches, caching, and other class functions, increasing performance. As Java evolves, high-performance Java systems will be developed that are capable of translating byte code to native machine code on the fly, using just-in-time translation. In theory, this will give Java programs the same speed as C++ applications.

The "Internet Toaster" Age

With the advent of embedded Java applets, we have entered the age of the proverbial "Internet Toaster," small, networked consumer appliances. Embedded Java is ideal for a wide range of applications, including pen computers, automotive diagnostics, telephone switches, video games, global-positioning-satellite navigation systems, interactive TV, robotics — the list is almost endless. Even the simplest device can include embedded networking technology.

Many see set-top boxes as the first foothold for embedding Internet technology in consumer applications. When

users punch in their remote control to buy a pay-per-view movie, the transaction that registers the purchase could easily be SNMP. The SNMP data is stored in firmware in the set-top device, and at off-peak hours once a day (or once a week), a modem in the device connected to a telephone jack in the user's home dials the cable head end to register the transaction via a telephone line. If it's a hard-wired connection such as cable TV, then the same transaction could even be sent over the coax.

RMON brings even more to this scenario. As viewers surf through the hundreds of channels available, an embedded RMON agent records a history of those viewing habits. This RMON MIB then reports back to the NMS at the cable head end to provide an ongoing portrait of those television preferences. This information could then be translated into a user profile that could form the basis of customized programming, targeted advertising, etc. Using data gathered with RMON, cable companies could create a customized service that matches viewers' individual tastes. The integration advances and cost savings that result from such a consumer market also will inevitably have an effect on industrial instrumentation and control systems.

If RMON can collect viewer habits, it also can monitor process traffic. As Internet standards continue to stabilize and more networking technology becomes part of the computer chip, the shape of computer networking will change forever. The network will become the computer, or rather, the network will become the computer chip.

David Preston is vice president, business development for Integrated Systems Incorporated (ISI),Sunnyvale, Calif. Previously, he was president and COO of Epilogue Technology Corporation,which became a wholly owned subsidiary of ISI in July ,1996. Mr. Preston has been in the computer networking industry since 1975 and holds a BSEE from Rutgers University and is a graduate of the Rutgers Advanced Management Program.

How Valuable	Circle
Highly	541
Moderately	542
Slightly	543

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UPDATE ON COVERIFICATION

Coverification Tools Ease Debugging Of Internal Core-Based ASIC Code

Developing code for core-based ASICs can be a lot like a game of "Blind Man's Bluff." In order to properly debug the code, you have to see what the processor is doing. But in a core-based ASIC, that processor is like a fair princess in a castle, guarded by an array of peripherals behind a wall of pungee stakes that are the external pins of the device. For developing application code that runs partly within the ASIC and partly from external memory, developers have come up with a number of tricks such as enhanced JTAG access, intelligent on-chip debug modules and are even making strides toward real-time emulation (ELECTRONIC DESIGN, *March 17, p. 108*).

However, ASICs with an embedded processor core have more software issues than just application code. Designers have to verify that the hardware/software interfaces between core and peripherals are correct. For example, if the software expects to select a certain mode by setting a bit in a peripheral register to "1," there must be an agreement between hardware and software on what that bit means. In addition, for each on-chip peripheral there needs to be driver code that often runs from on-chip ROM. In some cases, especially where security is a primary concern, parts of an application or even the entire application could be crammed into on-chip memory.

If on-chip software that is to be contained in masked on-chip ROM is not correct before the design goes to the fab, two very bad things will happen. First, it will be an enormous problem to figure out what is wrong. Second, when the error is finally found, it will take another $30,000 to $50,000 spin of the ASIC to get back on track—to say nothing of the time-to-market loss.

One approach to this dilemma that is drawing increased attention is to use hardware/software coverification technology to ensure the correctness of design before committing it to a wafer fab. The two major players in this arena are Mentor Graphics, Wilsonville, Ore., with its Seamless coverification environment, and Eagle Design Automation, Beaverton, Ore., with its Eaglei verification tool. The two systems have quite a bit in common. Basically, both provide a means of executing software on a model of a processor and linking that execution to a hardware simulation model in a hardware description language like VHDL or Verilog. In addition, there is a user interface for control and for gathering metrics.

The processor is modeled at a higher level than a VHDL or Verilog logic model because otherwise, they would execute too slowly to be useful. In the case of Mentor's Seamless, the processors are modeled as instruction set simulators (ISSs) that recreate all the processor operations such as register and stack operations and allow developers insight into the details of those functions. Eagle offers what it calls virtual software processors (VSPs) that offer a functional design description of a microprocessor. They work at a higher level of abstraction and as a result run faster but offer less insight into their internal workings than an ISS. For certain cores, such as MIPS and ARM, Eagle also offers instruction set simulators.

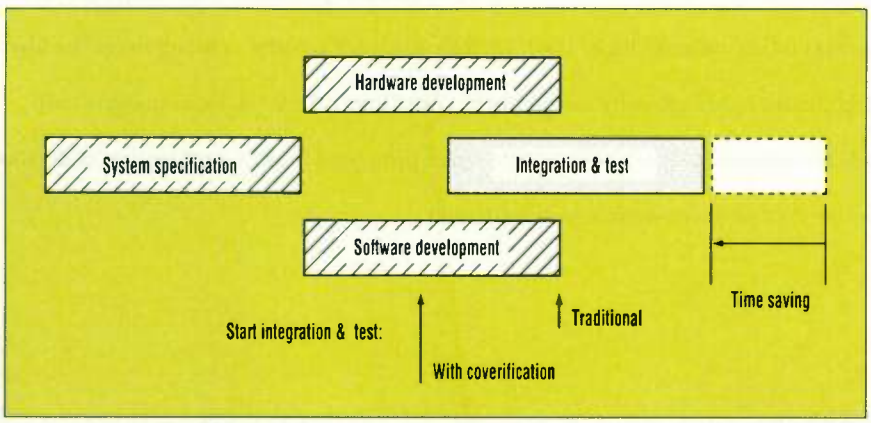
Neither the ISS nor the VSPs are gate-level VHDL models, and so they must be provided with a VHDL or Verilog "wrapper" to simulate the hardware pins in order to be able to talk to the bus model and to the hardware models running in the simulator *(Fig. 1)*. While Mentor supplies a hardware simulator called QuickHDL, Seamless also works with simulators from all other major vendors of logic simulation tools. Eagle does not supply its own simulator, but Eaglei also does work with simulators from all major vendors.

Breaking The Bottleneck

Since the speed bottleneck in a coverification environment is the hardware model, it is important to maximize the speed at which the processor model executes code and to limit its interaction with the hardware model without affecting functionality. Therefore, the processor model needs to fetch instructions from real memory on the workstation rather than from hardware model of memory.

Eagle calls the memory where code for the simulation is stored the instruction model subsystem (IMS) and maps it to the hardware model's memory space. Mentor's technology also supplies the ability to run native compiled software (NCS) that executes on the workstation's processor and stimulates the hardware. While NCS is not the object code for the end system, it communicates with an API on the bus interface model to the simulation and thus appears to the hardware model as if it were coming from the target processor.

While hardware/software coverification can be used effectively to shorten the design cycle for board-based designs, it really shines in the design of core-based ASICs. The basic



1. **Coverification provides the ability to develop and run software on hardware that is still under development. This not only shortens design time by moving the start of integration back; it also helps identify and fix problems before committing an ASIC design to fab.**

ERA AMPLIFIERS

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- *Driver amplifier for a fiber-optic transmitter*
- *LO driver amplifier for a mixer in a high dynamic range wideband frequency converter*
- *RF amplifier for a wideband frequency converter*
- *IF amplifier in a broadband RF system*
- *Driver stage for a broadband distribution amplifier*
- *Buffer amplifier for a VCO*
- *Driver amplifier for a broadband frequency doubler*
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SPECIFICATIONS:

at 25°C


ERA


ERA-SM

MODEL NO.	FREQ. GHz f_l - f_u	GAIN, dB Typical over frequency, GHz 0.1	1	2	3	4	6	8	Min.@ 2 GHz	Flatness DC-2 GHz	MAXIMUM POWER, dBm at 2 GHz* Output (1 dB Comp.) Typ.	Min.	Input (no dmg.)	DYNAMIC RANGE at 2 GHz* NF dB Typ.	IP3 dBm Typ.	VSWR Typ. (:1) In DC-3 GHz	In 3-f_u** GHz	Out DC-3 GHz	Out 3-f_u** GHz	MAXI-MUM RATING[3] I mA	P mW	DC POWER at Pin 3 Cur-rent (mA)	Volt Typ.	THER-MAL RESIS-TANCE θjc, typ. °C/W	Case Style Note A	CONNECTION	Price $ Qty. (30)
ERA-1	DC-8	12.2	12.1	11.8	11.5	11.3	11.0	10.2	9	±0.3	11.7	9.7	15	5.3	26	1.6	1.8	1.5	1.9	75	330	40	3.6	455	VV105	cb	1.37
ERA-2	DC-6	16.2	16.0	15.6	15.1	14.6	14.0	—	12	±0.3	12.8	11	15	4.7	26	1.4	1.4	1.4	1.6	75	330	40	3.6	455	VV105	cb	1.52
ERA-3	DC-3	22.9	22.2	20.8	19.2	—	—	—	17	±1.1	12.1	9	13	3.8	23	1.7	—	1.7	—	75	330	35	3.5	432	VV105	cb	1.67
ERA-4	DC-4	13.8	13.7	13.5	13.3	13.0	—	—	11	±0.2	17.0	15	20	5.5	32.5	1.6	1.6	1.4	1.6	120	650	65	5.0	278	VV105	cb	3.85
ERA-5	DC-4	20.2	19.8	18.8	17.7	16.4	—	—	16	±0.75	18.4	16.5	13	4.5	33	1.2	1.2	1.3	1.5	120	650	65	4.9	278	VV105	cb	3.85
ERA-6	DC-4	11.1	11.1	11.3	11.5	11.3	—	—	10	±0.2	18.5	16.5	20	8.4	36.5	1.3	1.3	1.6	1.6	120	850	70	5.5	220	VV105	cb	3.85
ERA-1SM	DC-8	12.3	12.1	11.8	11.2	10.8	10.4	9.2	9	±0.3	11.3	9.3	15	5.5	26	1.6	1.9	1.5	1.9	75	330	40	3.6	460	WW107	cb	1.42
ERA-2SM	DC-6	16.2	15.8	15.2	14.4	13.6	13.0	—	12	±0.5	12.4	10.5	15	4.6	26	1.5	1.6	1.5	1.7	75	330	40	3.6	460	WW107	cb	1.57
ERA-3SM	DC-3	22.8	21.8	20.2	18.4	—	—	—	16	±1.3	11.5	9	13	3.8	23	1.5	—	1.5	—	75	330	35	3.5	437	WW107	cb	1.72
ERA-4SM	DC-4	14.0	13.8	13.5	13.2	12.7	—	—	11	±0.3	16.8	15	20	5.2	33	1.6	1.6	1.3	1.5	120	650	65	5.0	283	WW107	cb	3.90
ERA-5SM	DC-4	20.2	19.5	18.5	17.3	16.2	—	—	16	±1.0	18.4	16.5	13	4.3	32.5	1.3	1.3	1.2	1.3	120	650	65	4.9	283	WW107	cb	3.90
ERA-6SM	DC-4	11.2	11.2	11.3	11.4	11.2	—	—	10	±0.2	17.9	16	20	8.4	36	1.3	1.3	1.6	1.5	120	850	70	5.5	225	WW107	cb	3.90

NOTES:

- * at 1 GHz for ERA 4, 5, 6, 4SM, 5SM, 6SM.
- ** f_u is the upper frequency limit for each model as shown in the table.
- o Low frequency cutoff determined by external coupling capacitors.

A. Units are non-hermetic unless otherwise noted. For details on case dimensions & finishes see "Case Styles & Outline Dimensions".
B. Prices and Specifications subject to change without notice.
1. Model number designated by alphanumeric code marking.
2. ERA-SM models available on tape and reel.

absolute maximum ratings

operating temperature: -45°C to 85°C
storage temperature: -65° to 150°C
device voltage:
3.0V min., 4.1V max. for ERA 1,2,3
4.2V min., 5.5V max. for ERA 4,5
5.0V min., 6.0V max. for ERA-6

DESIGNERS KITS AVAILABLE

KIT NO.	Model Type	No. of Units in Kit	Description	Price $ per kit
K1-ERA	ERA	30	10 of each 1,2,3	49.95
K2-ERA	ERA	20	10 of each 4,5	69.95
K1-ERASM	ERA-SM	30	10 of each 1SM, 2SM,3SM	49.95
K2-ERASM	ERA-SM	20	10 of each 4SM, 5SM	69.95
K3-ERASM	ERA-SM	30	10 of each 4SM, 5SM, 6SM	99.95

CASE STYLES/ outline dimensions (inch / mm)

case no.	A	B	C	D	E	F	G	H	wt. grams.	NOTES*
VV105	.085 2.16	.060 1.52	.008 .20	.020 .51	.256 6.50	.012 .30	.025 .64		.015	A13, C4, E2
WW107	.020 .51	.10 2.54	.020 .51	.092 2.34	.085 2.16	.060 1.52	.008 .20	.026 .66	.015	A13, C4, E2, F4

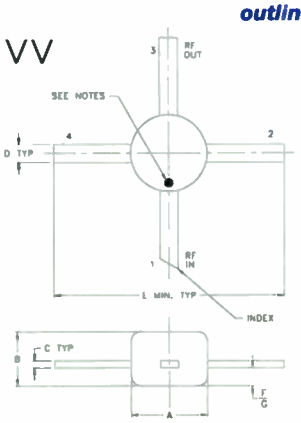
tolerance .x±.1 .xx±.03 .xxx±.015 inch **oz. = grams x.0353**

NOTES*:

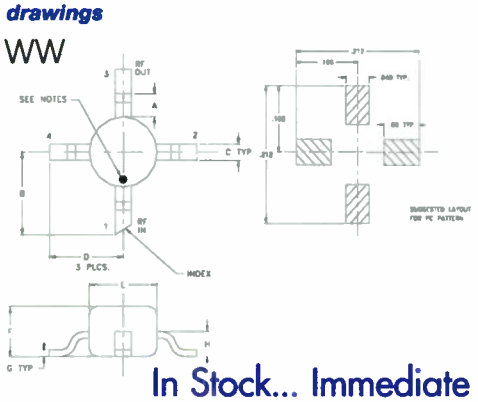
A13. Case material: plastic. Lead finish: Tin or tin-lead plate.
C4. RF input lead (1) identified by diagonally cut lead; the cut may be 45°(ref) in either direction. It may also have an additional orientation mark. Model dash number identified by color dot or alphanumeric code on case.
E2. Lead width ±.010; lead thickness ±.005 inch.
F4. Tape and reel packaging available. See Tape and Reel Packaging Information for details. To order Tape & Reel version add -TR suffix to model.

outline drawings

VV



WW



marking identification

Model	Alphanumeric Code
ERA-1, ERA-1SM	E1
ERA-2, ERA-2SM	E2
ERA-3, ERA-3SM	E3
ERA-4, ERA-4SM	E4
ERA-5, ERA-5SM	E5
ERA-6, ERA-6SM	E6

Available Tape & Reel

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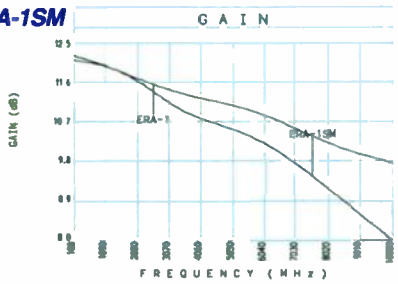
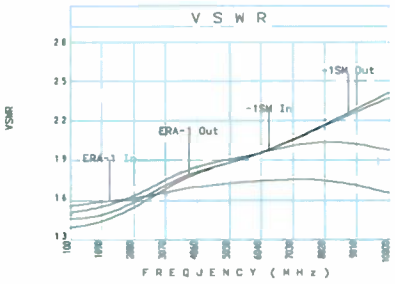
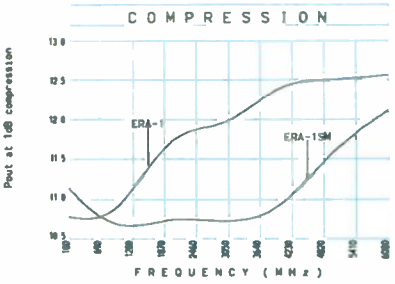
S-PARAMETERS GAIN, GAIN COMPRESSION, RETURN LOSS, ISOLATION

ERA-1SM

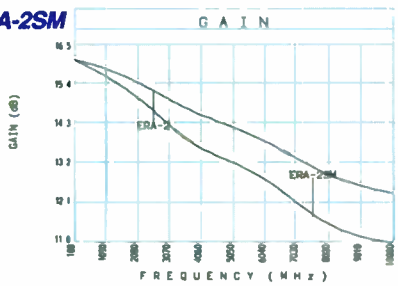


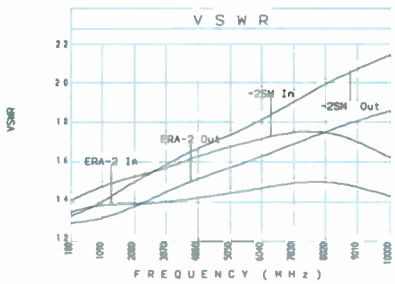


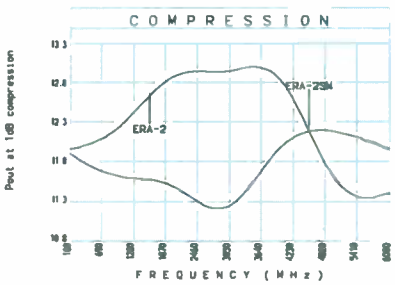


Freq. MHz	S_{11} (Input Return Loss) dB	Mag	Angle	S_{21} (Power Gain) dB	Mag	Angle	S_{12} (Isolation Out-In) dB	Mag	Angle	S_{22} (Output Return Loss) dB	Mag	Angle	K
100	-13.97	0.20	177.96	12.31	4.13	170.76	-16.97	0.14	-2.91	-15.84	0.16	172.55	1.06
550	-13.43	0.21	159.71	12.12	4.04	137.76	-16.60	0.15	-30.72	-15.42	0.17	158.11	1.04
1000	-12.92	0.23	144.17	11.97	3.97	104.55	-16.66	0.15	-55.46	-14.62	0.19	142.15	1.04
2000	-11.63	0.26	115.37	11.50	3.76	31.11	-16.70	0.15	-111.57	-12.59	0.23	118.14	1.01
3000	-10.30	0.31	94.66	10.94	3.52	-42.64	-16.75	0.15	-168.73	-10.90	0.29	102.41	0.98
4000	-9.47	0.34	82.30	10.33	3.28	-114.36	-16.87	0.14	134.07	-9.44	0.34	87.77	0.96
5000	-9.17	0.35	74.43	9.53	3.00	175.55	-17.16	0.14	75.93	-8.35	0.38	69.43	0.98
6000	-9.34	0.34	69.53	8.94	2.80	107.96	-17.39	0.14	17.51	-7.42	0.43	54.63	1.00
7220	-10.05	0.31	63.58	9.04	2.83	26.04	-18.12	0.12	-55.87	-6.81	0.46	33.66	1.05
8000	-9.80	0.32	60.25	9.10	2.85	-25.22	-18.78	0.12	-101.98	-6.39	0.48	23.31	1.06

ERA-2SM

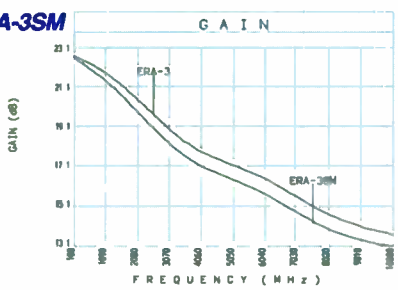


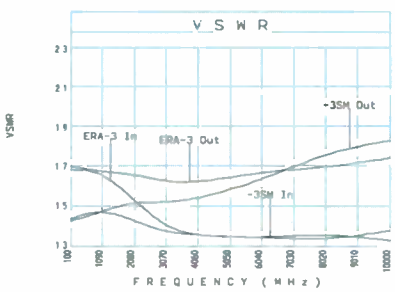


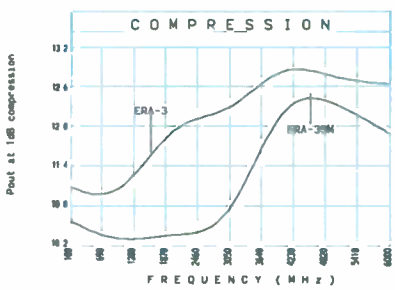


Freq. MHz	S_{11} (Input Return Loss) dB	Mag	Angle	S_{21} (Power Gain) dB	Mag	Angle	S_{12} (Isolation Out-In) dB	Mag	Angle	S_{22} (Output Return Loss) dB	Mag	Angle	K
100	-17.46	0.13	176.77	16.14	6.41	170.10	-19.36	0.11	-2.02	-19.03	0.11	174.06	1.03
550	-16.15	0.16	152.26	15.95	6.27	135.76	-19.03	0.11	-28.55	-18.19	0.12	154.95	1.02
1000	-15.45	0.17	132.82	15.69	6.09	100.80	-19.05	0.11	-52.12	-17.07	0.14	138.34	1.02
2000	-13.66	0.21	99.88	14.90	5.56	23.41	-18.33	0.12	-105.24	-14.85	0.18	115.14	0.99
3000	-12.34	0.24	79.89	13.99	5.01	-50.95	-18.64	0.12	-160.52	-13.10	0.22	102.29	1.00
4000	-11.85	0.26	71.57	13.03	4.48	-123.74	-18.52	0.12	144.60	-11.53	0.27	89.80	1.02
5000	-11.74	0.26	69.51	11.86	3.92	166.38	-18.68	0.12	87.38	-10.34	0.30	71.96	1.08
6000	-12.16	0.25	69.51	11.11	3.59	98.14	-18.67	0.12	29.47	-9.27	0.34	58.13	1.11
7220	-13.03	0.22	76.69	11.07	3.58	15.13	-19.28	0.11	-41.09	-8.96	0.36	36.99	1.18
8000	-11.73	0.26	79.33	10.97	3.54	-36.97	-19.93	0.10	-85.53	-8.48	0.38	27.38	1.20

ERA-3SM







Freq. MHz	S_{11} (Input Return Loss) dB	Mag	Angle	S_{21} (Power Gain) dB	Mag	Angle	S_{12} (Isolation Out-In) dB	Mag	Angle	S_{22} (Output Return Loss) dB	Mag	Angle	K
100	-13.57	0.21	174.98	22.57	13.44	168.49	-24.83	0.06	-6.88	-13.54	0.21	172.92	0.93
550	-13.16	0.22	143.84	22.13	12.78	128.25	-24.15	0.06	-20.53	-13.45	0.21	148.84	0.92
1000	-13.21	0.22	119.72	21.46	11.83	88.76	-23.91	0.06	-39.52	-13.20	0.22	127.78	0.93
2000	-13.91	0.20	80.56	19.44	9.38	5.82	-22.50	0.07	-88.03	-12.83	0.23	99.76	0.95
3000	-14.90	0.18	63.12	17.48	7.48	-70.08	-21.40	0.09	-140.31	-12.59	0.23	86.91	0.99
4000	-15.99	0.16	66.26	15.69	6.09	-142.98	-20.38	0.10	164.98	-11.83	0.26	78.08	1.03
5000	-15.68	0.16	78.95	14.00	5.01	147.59	-20.07	0.10	108.25	-11.05	0.28	62.38	1.10
6000	-15.06	0.18	89.08	12.77	4.35	81.29	-19.70	0.10	50.92	-9.95	0.32	52.96	1.14
7220	-12.95	0.23	106.02	12.45	4.19	-2.14	-19.68	0.10	-17.83	-10.09	0.31	36.16	1.13
8000	-10.12	0.31	97.46	12.06	4.01	-54.58	-19.83	0.10	-60.30	-9.58	0.33	29.45	1.08

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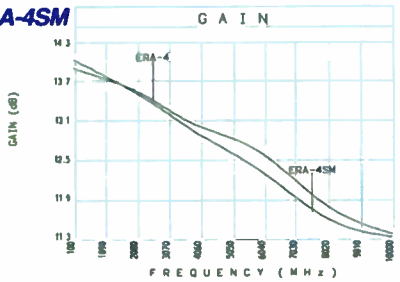
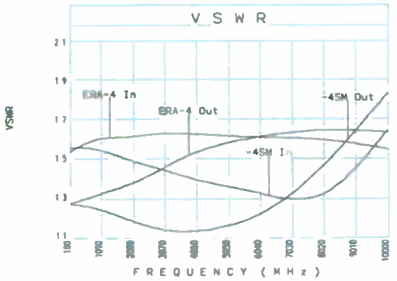
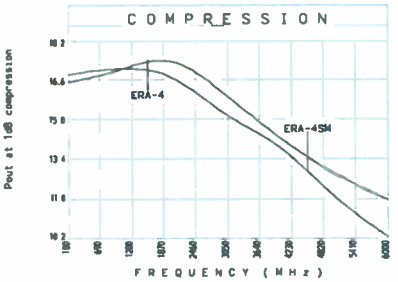
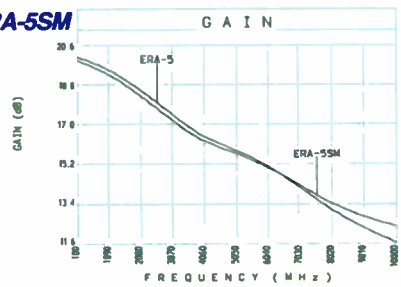


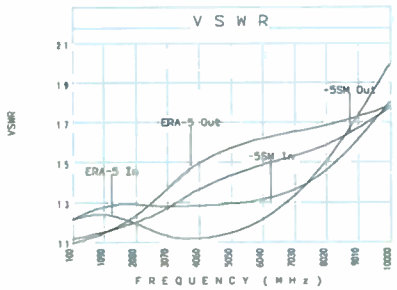


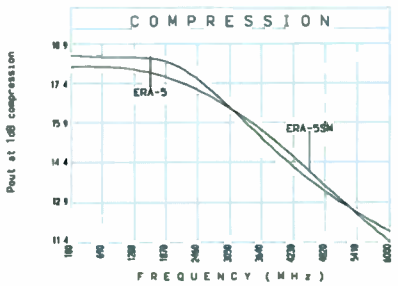


Freq. MHz	S_{11} (Input Return Loss) dB	Mag	Angle	S_{21} (Power Gain) dB	Mag	Angle	S_{12} (Isolation Out-In) dB	Mag	Angle	S_{22} (Output Return Loss) dB	Mag	Angle	K
100	-12.64	0.23	177.59	13.67	4.83	170.61	-18.09	0.12	-5.31	-17.67	0.13	178.50	1.04
550	-12.36	0.24	158.88	13.56	4.76	136.16	-18.17	0.12	-29.89	-16.88	0.14	162.80	1.04
1000	-12.10	0.25	143.21	13.47	4.72	101.77	-18.16	0.12	-54.80	-16.29	0.15	149.98	1.04
2000	-11.54	0.26	111.96	13.16	4.55	23.71	-18.21	0.12	-109.29	-14.66	0.18	129.88	1.03
3000	-11.21	0.28	88.25	12.85	4.39	-53.45	-18.30	0.12	-165.76	-13.27	0.22	116.80	1.03
4000	-11.88	0.25	76.83	12.41	4.17	-130.95	-18.66	0.12	138.93	-12.24	0.24	103.89	1.08
5000	-13.04	0.22	79.31	11.63	3.82	152.70	-19.18	0.11	81.11	-12.25	0.24	86.11	1.22
6000	-13.34	0.22	93.52	11.03	3.56	77.52	-19.69	0.10	26.67	-12.46	0.24	76.84	1.35
7220	-10.27	0.31	108.89	10.63	3.40	-17.86	-20.58	0.09	-35.88	-13.29	0.22	80.82	1.45
8000	-7.77	0.41	98.82	9.81	3.09	-76.73	-20.76	0.09	-75.38	-11.39	0.27	82.14	1.39

ERA-5SM

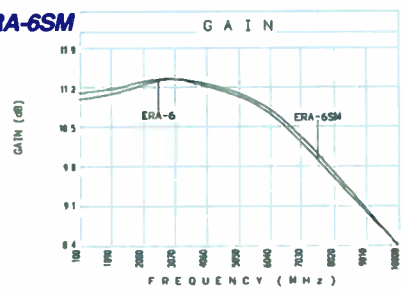


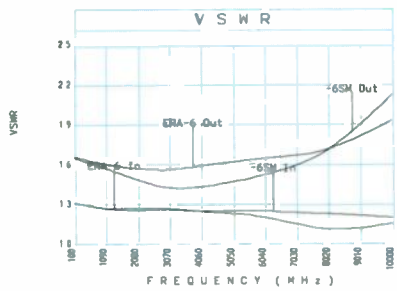


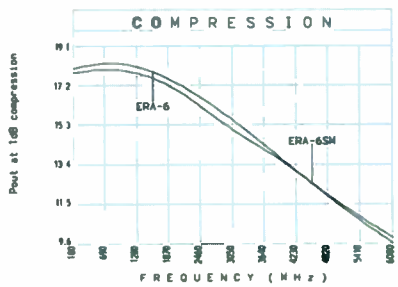


Freq. MHz	S_{11} (Input Return Loss) dB	Mag	Angle	S_{21} (Power Gain) dB	Mag	Angle	S_{12} (Isolation Out-In) dB	Mag	Angle	S_{22} (Output Return Loss) dB	Mag	Angle	K
100	-14.91	0.18	172.80	20.08	10.09	169.05	-23.72	0.07	1.81	-17.76	0.13	173.95	1.03
550	-14.61	0.19	149.79	19.80	9.77	130.66	-22.47	0.08	-25.08	-17.80	0.13	158.90	0.99
1000	-14.54	0.19	127.39	19.43	9.36	92.07	-22.47	0.08	-46.48	-17.18	0.14	144.80	1.00
2000	-15.20	0.17	88.80	18.21	8.14	7.80	-21.96	0.08	-96.71	-15.98	0.16	126.69	1.02
3000	-16.90	0.14	72.32	16.81	6.93	-72.65	-21.39	0.09	-148.00	-14.68	0.18	119.64	1.07
4000	-18.41	0.12	90.96	15.31	5.83	-150.97	-20.92	0.09	160.47	-13.07	0.22	111.07	1.13
5000	-15.79	0.16	113.66	13.69	4.84	134.42	-20.88	0.09	106.02	-12.89	0.23	96.01	1.24
6000	-11.86	0.26	120.29	12.47	4.20	61.41	-20.42	0.10	52.41	-11.48	0.27	89.96	1.22
7220	-7.68	0.41	114.34	11.43	3.73	-31.64	-19.67	0.10	-10.06	-10.13	0.31	87.00	1.03
8000	-5.99	0.50	98.67	10.30	3.27	-87.65	-19.50	0.11	-53.25	-8.56	0.37	79.20	0.91

ERA-6SM







Freq. MHz	S_{11} (Input Return Loss) dB	Mag	Angle	S_{21} (Power Gain) dB	Mag	Angle	S_{12} (Isolation Out-In) dB	Mag	Angle	S_{22} (Output Return Loss) dB	Mag	Angle	K
100	-16.75	0.15	-2.94	11.09	3.59	170.58	-17.19	0.14	-4.79	-11.83	0.26	-1.41	1.13
550	-16.91	0.14	-0.03	11.01	3.55	135.73	-16.54	0.15	-32.00	-12.06	0.25	-14.25	1.10
1000	-17.32	0.14	2.75	11.04	3.56	100.28	-16.63	0.15	-57.70	-12.78	0.23	-25.84	1.12
2000	-18.03	0.13	12.27	11.04	3.56	19.44	-16.80	0.14	-116.46	-15.24	0.17	-62.30	1.16
3000	-17.99	0.13	26.56	10.92	3.52	-62.65	-17.17	0.14	-175.73	-16.71	0.15	-125.67	1.21
4000	-18.20	0.12	43.82	10.39	3.31	-145.69	-17.69	0.13	126.08	-14.15	0.20	173.19	1.29
5000	-17.56	0.13	64.89	9.28	2.91	132.93	-18.59	0.12	66.95	-12.24	0.24	137.21	1.49
6000	-16.31	0.15	80.31	8.14	2.55	53.42	-19.44	0.11	9.86	-9.70	0.33	111.65	1.69
7220	-13.36	0.21	94.70	6.60	2.14	-44.65	-20.58	0.09	-56.02	-7.21	0.44	90.13	1.94
8000	-10.91	0.28	86.50	5.10	1.80	-102.76	-21.17	0.09	-99.65	-5.94	0.50	75.87	2.11

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How To Use ERA Amplifiers

MICROSTRIP STRUCTURE

Board Layout Suggestions For ERA Amplifiers: In a typical microstrip structure (**Figure 1**), line impedances are determined by strip width (w), board dielectric constant (ϵ_r), and dielectric thickness (h). Since the impedances of the ERA units are prematched to operate in a 50 ohm system, microstrip lines should be as close to 50 ohms as possible to realize full specified performance. For various board materials, line width dimensions for a 50 ohm line are given in **Table 1.** Operation in systems with characteristic impedances other than 50 ohms is possible with somewhat reduced performance. ERA amplifiers offer very good return loss in a 50 ohm system. The board material for a microstrip structure should be selected to suit the intended frequency of operation. PTFE woven glass performs well to frequencies in excess of 2GHz, is a fairly rugged material that can tolerate substantial rework, and is not particularly sensitive to heat or humidity. Duroid is the favored material of microwave designers because of its high dielectric consistency and low dialectric dissipation. RT/duroid is a somewhat fragile material which crushes fairly easily; glues do not adhere well to its substrate so thin metalization patterns are subject to lifting if abused with repeated rework. Some versions can also be quite hydroscopic, and can show substantial dilectric shifts with variations in humidity. Because of these factors, care should be taken when working with the material. Other materials are Taconic, OAK 602, etc.

Table 1 Line Widths for 50 ohm line for various board materials

Board Material	ϵ	Thick	w for 50Ω
RT/Duriod 5870[1]	2.3	.015"	.044"
PTFE-Woven Glass Fiber (Typ.)	2.55	.010" .031" .062"	.025" .079" .158"
Epoxy-Glass (G10)	4.8	.062"	.108"
Alumina/E10[2]	10.0	.025" .050"	.025" .048"

[1] *Trademark of Rogers Corp. for its PTFE nonwoven glass PC material. (RT is reinforced teflon and PTFE is polytetraflourethylene)*

[2] *E-10 and Epsilam-10 are trademarks of 3M for its ceramic filled PTFE substrate.*

GROUNDING ERA's AND AVOIDING PARASITICS

During board layout, care should be taken to minimize all parasitics. Remember that extra lead length equals extra inductance added to the design. This is particularly important if the circuit is to be operated above 1GHz. Transmission lines should, whenever possible, run flush to the package. This requires that a hole be made in the board so the ERA amplifier leads are in the same plane as the transmission line. ERA amplifiers should be mounted on the etched side of the board to minimize the inductance of feedthrough connections. Abrupt changes in transmission line width also create parasitic effects called step discontinuities. Tapering the transmission lines from 50 ohms down to the amplifier lead width helps minimize this effect. Bends in transmission lines can create parasitic effects and should be avoided when possible. When they must be used however, the corners should be chamfered to prevent the bends from acting as extra shunt capacitance. Ground planes should be kept as large and as solid as possible. Return paths for high frequency circulating currents must be kept as short as possible, especially at the emitter leads (ERA ground lead connections). If plated through holes are used as ground returns, they should be placed directly under the ground leads of the ERA and be located as near as possible to the body of the package. Any additional path length acts as series inductance, which translates into unwanted emitter resistance at operating frequencies. Gain, output power, compression, and high frequency rolloff will all be degraded if proper grounding techniques are not used. A gain decrease of more than 1dB can be expected at 1GHz for approximately 2nH of lead inductance. An excellent way to design a PCB footprint for ERA's is to use coplanar waveguide with ground plane. **Figure 2** shows the suggested layout.

Figure 1 Solid Metalization Microstrip Structure

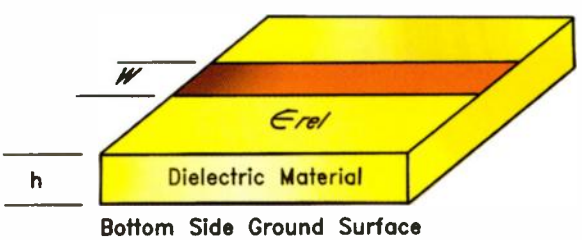

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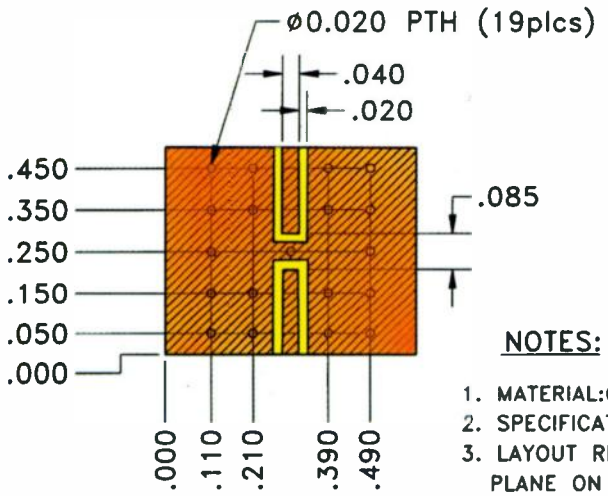
Figure 2 Suggested PCB Layout For ERA Amplifiers



NOTES:

1. MATERIAL:OAK-602, DIELECTRIC THICKNESS: .015±.001
2. SPECIFICATIONS/REQUIREMENTS PER GS-162.
3. LAYOUT REPRESENTS COPLANAR LINE WITH GROUND PLANE ON THE BOTTOM SURFACE OF PCB.

ERA BIASING TECHNIQUES

For any of the ERA MMIC amplifiers, the biasing scheme is fairly simple. It requires DC blocking capacitors at the input and output ports, with a common output port and bias terminal. Hence, an RF choke in series with a biasing resistor is required at the output port. Biasing resistor values can be calculated from:

$$R_{bias} = [1000(V_{cc} - V_d)] / I_{bias}$$

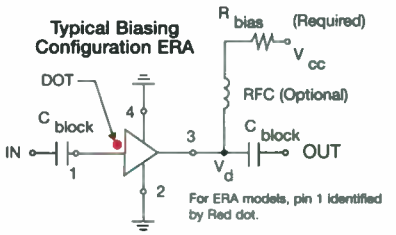
where:

V_{cc} = the supply voltage
V_d = the device voltage
I_{bias} = the bias current (in mA).

For a 50 ohm system, the bias resistor appears in parallel with the output load impedance. For example, for ERA-1 with a +5.6V DC supply, the bias resistor is 50 ohms and appears in parallel with a 50 ohm output load, resulting in a 3dB loss of power across the output load with an alteration in the output VSWR. To avoid this "power divider" effect, an RF choke should be added in series with the bias resistor. The RF choke should offer an impedance of at least 500 ohms (about 10 times the load impedance) at the lowest operating frequency, and be free of resonances to the highest operating frequency. The typical biasing arrangement can be seen in **Figure 3.** **Table 2** illustrated at right shows the different resistor values that are needed for various bias voltages for all ERA amplifiers. If different bias currents are used other than the ones recommended in our specification chart, then bias resistor values have to be recalculated using the previously stated equation substituting the different value for bias current (I_{bias}) and the device voltage (V_d) at that current.

Figure 3

TYPICAL BIASING CONFIGURATION



In this typical biasing configuration, DC blocking capacitors are added to the input port (pin number 1 on the packaged amplifier) and the output port.

Table 2 ERA Resistor Values (in ohms) at Various Bias Voltages

Model	Bias Current mA	Supply Voltage				
		5V DC	9V DC	12V DC	15V DC	20V DC
ERA-1	40	35	135	210	285	410
ERA-2	40	35	135	210	285	410
ERA-3	35	43	157	243	328	471
ERA-4	65	*	61.5	108	154	230
ERA-5	65	*	63	109	155	232
ERA-6	70	*	50	93	136	207

* Not Recommended

MEDIAN TIME TO FAILURE (MTTF) AND QUALIFICATION TESTS

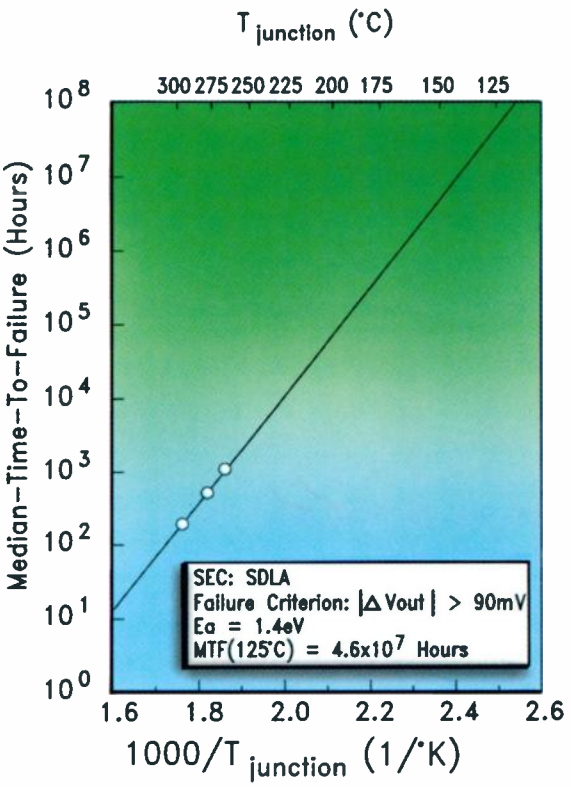
GENERIC HIGH TEMPERATURE LIFE TESTS

MTTF (Median Time To Failure) of a device is a function of the junction temperature, and is governed by the Arrhenius equation:

$$t = Ce^{-E_A/kT}$$

where t is time to fail, C is a constant, E_A is the activation energy (eV), k is Boltzmann's constant = 8.617×10^{-5} (eV/K), and T is absolute temperature in degrees Kelvin. By taking the log of both sides, it is easy to see that log t vs. 1/T is a straight line. Thus, by performing life test at two or more temperatures which are high enough to induce failures at a reasonably short time, the above equation is defined and can be used for predicting MTTF at lower temperatures. Three temperature life tests were done on the generic HBT amplifiers: at 200, 215, and 230°C ambient temperatures. From this data, MTTF is read for each temperature. This is plotted on the Arrhenius graph as shown in **Figure 4**, where MTTF is in log scale and 1000/T is on linear scale where T_j is the junction temperature. This is the basis for the MTTF curve illustrated in **Figure 5** (page 10).

Figure 4 Arrhenius Graph MTTF vs. $1000/T_{junction}$



HIGH TEMPERATURE LIFE TESTS

High temperature life tests on the actual devices substantiate the MTTF curve and qualify the devices. This consists of DC burn-in of ERA-1SM at +125°C, and RF burn-in of ERA-3SM, -4SM, and -5SM at +85°C.

ACCELERATED LIFE TEST (DC BURN-IN)

ERA-1SM: 10 units are being subjected to DC Burn-in at 125°C and 50mA constant bias current. Periodic measurements are made for gain and device voltage at room temperature and compared to initial values. Failure criteria is gain change of 1dB or more, device voltage change of 10% or more.

84 days (2016 hours) completed at 125°C.
All units within spec. 1 unit out of 10 showed gain degradation of 1.2dB from initial value.

The chip size of ERA-1SM is the same as ERA-2SM and ERA-3SM, therefore the results of the above burn-in can be valid for all three models. Since this test was run at 50mA device current, at 125°C, and we are specifying ERA-1SM and ERA-2SM at 40mA and 85°C ambient, we have tested under much more stringent conditions. The junction temperature at 40mA will be 35°C lower than at 50mA and the MTTF will be improved by 15 to 20 fold. If we add to that the difference between 125°C and 85°C, which is the upper limit in our ambient temperature spec, this brings the total to 75°C resulting in a MTTF ratio of almost 500 to 1. Therefore, 2000 hr burn-in at 50mA and 125°C is the equivalent of approximately 115 years at 85°C and 40mA. This is in agreement with our predicted results and the MTTF curve in **Figure 5** (page 10). This DC Burn-in test will continue until 50% failures are seen. This is predicted to be at around 0.6 years, which translates to 300 years at +85°C and 40mA.

RF BURN-IN

ERA-3SM, -4SM, and -5SM: 16 units of each are being tested for RF burn-in at 2GHz, 1dB compression point at 85°C. Periodic measurements are made for output power and compared to initial values. Failure criteria: Output power change of more than 1dB. So far, the following data has been obtained:

ERA-3SM 251 days (6024 hours).....*No Failures*
ERA-4SM, -5SM 190 days (4560 days)..... *No Failures*

This corresponds to 11 device years without failure and 16.7 years for ERA-4SM and -5SM combined, which translates to 125 device years without failure at rated current. This test is planned to continue until 50% of the units have failed.

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OTHER QUALIFICATION TESTS

The following qualification tests have been performed on ERA-3SM per MIL-STD-883. By design similarity, this data can also be applied to ERA-1SM and -2SM.

ERA-1SM, -2SM, -3SM

Qualification	MIL-STD-883 Method	Remarks
*Resistance to solvents	2015	6 units tested, *0 failures*
*Solderability	2003	8 units tested, *0 failures*
*Lead Integrity	2004	12 units tested, *0 failures*
Temp. Cycle 1000 cycle -65°C to +150°C	1010C	15 units tested, *0 failures*
Steady State Life Test@ 125°C	1005B	1000 hrs completed, 50 units *0 failures*
Autoclave	N/A	168 hrs, 121°C, RH=100%, 15psig 15 units tested, *0 failures*
85% humidity @ 85°C T_a		1000 hrs completion due 3/14/97

**Applicable to all ERA models.*

The following qualification tests have been performed on ERA-5SM per MIL-STD-883. By design similarity, this data can also be applied to ERA-4SM and -6SM.

ERA-4SM, -5SM, -6SM

Qualification	MIL-STD-883 Method	Remarks
Steady State Life Test@ 85°C	1005B	1000 hrs completed, 50 units, *0 failures*
Steady State Life Test@ 125°C	1005B	500 hrs completed, 50 units, *0 failures*
85% humidity @ 85°C T_a		1000 hrs completed, *0 failures*

STABILIZATION BAKE

All ERA amplifiers are stabilization baked at 240°C for 48 hrs at chip level prior to packaging.

MECHANICAL TESTS

ERA units are mechanically similar to MAR series amplifiers, which have been successfully marketed for several years. ERA amplifiers should therefore meet all mechanical specifications applicable for MAR units. In addition, the following mechanical tests (per MIL-STD-883) are being scheduled for ERA-3SM and -5SM:

Mechanical Shock	condition 2002
Constant acceleration	condition 2001
Vibration	condition 2007

RELIABILITY ANALYSIS

Reliability analysis of the ERA amplifiers involves calculation of junction temperature under various operating conditions, and using this junction temperature in the MTTF curve to read the median time to failure of the device. The junction temperature T_j is a function of the ambient temperature T_a, the thermal resistance junction to case θ_{jc}, and the dissipated power P_{diss}.

It can be shown in the following equation:

$$T_j = T_a + \Delta T_{ac} + \theta_{jc} \cdot P_{diss}$$
$$= T_a + \Delta T_{ac} + \theta_{jc}\, V_d\, I_d$$

The thermal resistance θ_{jc} is mainly a function of the physical size of the device and its components. It is expressed in °C/Watt. The dissipated power (P_{diss}) is a product of the device voltage (V_d) and the device current (I_d), which are both given on the specification page. This method is very conservative and will give the worst case, since it does not subtract the output RF power from the DC input power to reduce the power dissipation. The maximum ambient temperature T_a is given on the spec page for all ERA units as 85°C. ΔT_{ac} is the temperature difference between ambient and case lead, and its value is dependent on how well the port is heat sunk. In our tests, ΔT_{ac} was measured to be around 6°C when units were soldered to a PC board. This is a good approximation that can be used in all calculations. At various device currents from 35 mA for ERA-1 and ERA-2, we can obtain different junction temperatures and Median Time To Failure (MTTF) data. Since ERA's are made of two transistors in Darlington pair, power dissipation in each transistor is not linearly proportional to the device current. Hence, the thermal resistance is not constant with device current/power dissipation. The change in device current changes the dissipated power and also the thermal resistance. The device voltage is also slightly reduced with reduced device current. **Table 3** shows thermal resistance, junction temperature, and MTTF at various device currents for all ERA amplifiers. **Figure 5** (page 10) shows MTTF as a function of junction temperature for all ERA amplifiers.

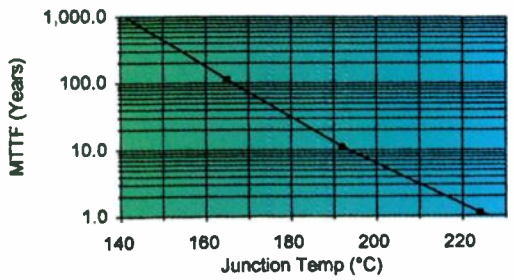
Table 3 Junction Temperature and MTTF vs. Device Current

Model No.	Device Current mA	Device Voltage volts	Power Dissipated Watts	Thermal Resist. θjc °C/W	Junction Temp. @85°C ambient °C	Computed MTTF Years
ERA-1,-2	35	3.5	.1225	432	143	1000
	40	**3.6**	**.144**	**455**	**156**	**250**
	45	3.7	.166	496	173	40
	50	3.8	.190	531	191	11
ERA-3	30	3.5	1.05	420	135	2000
	35	**3.5**	**.1225**	**432**	**143**	**1000**
	40	3.6	1.44	455	156	250
ERA-4	55	4.9	.269	270	164	150
	65	**5.0**	**.325**	**278**	**181**	**28**
	70	5.0	.350	282	190	13
	80	5.1	.408	290	209	3.3
ERA-5	55	4.8	.264	270	162	160
	65	**4.9**	**.319**	**278**	**180**	**30**
	70	4.9	.343	282	188	15
	80	5.0	.400	290	207	4
ERA-6	55	5.2	.286	225	156	280
	70	**5.5**	**.385**	**225**	**178**	**40**
	75	5.6	.420	225	186	20
	80	5.7	.456	225	194	9

We can see from this data and calculations that amplifier reliability and MTTF are greatly dependent on device current, which the user can select. A drop of 10mA (from 50 to 40mA) for ERA-1 and -2 reduces the junction temperature by 35°C and improves the MTTF almost 22 times. The surface mount units have the same device current and voltage. The thermal resistance is higher by 5°C/W due to the bent leads. This will result in a slightly higher junction temperature and slightly lower MTTF. For ERA-1 and -2 at 40mA, the thermal resistance is 460°C/W (instead of 455), which results in only half of a degree higher junction temperature. Rounded off to the nearest °C, both the junction temperature and the MTTF of the surface mount units are approximately the same as the corresponding drop-in units. Other factors possibly effected by changes in device current are gain, output power, IP3, return loss, and noise figure.

Figure 5

MTTF vs JUNCTION TEMP(ERA)



PERFORMANCE PARAMETERS VS. DEVICE CURRENT

We evaluated all performance parameters at various device currents and compared them with each other to see the effect of device current on performance. For power gain, a drop of 10mA in device current for ERA-1 and -2 does not make a significant change. The drop in gain is less than 1/4dB at most frequencies. We are able to maintain all our minimum gain values (as stated in the specification page) at 40mA as we did at 50mA. Similar results are seen for other ERA's to show that gain is not varying significantly with device current. The input and output return loss are also not significantly affected due to change in device current. Lowering device current can slightly improve input and output return loss, especially at the lower frequencies. At the higher frequencies, there is no difference and the results are the same. The output power at 1dB compression point does show a drop with dropping device current. We measured this parameter at various device currents, and the results are shown in **Table 4** and **Figure 6**. Generally, there was a drop of 2 to 3dB in output power at 2GHz for dropping device current from 50 to 40mA for ERA-1 and -2. This drop was much less at higher frequencies. For ERA-4 and -5, the change to 65mA from 80mA caused a drop of 1 to 2dB in output power at 1GHz, and around 1dB drop in output power for ERA-6. IP3 measurements also showed some drop as a result of reduced current. This was around 4dB for the ERA-2, 3.5dB for ERA-1 and -4, and 3dB for ERA-5 and -6. The noise figure is reduced at lower device currents, about 1 to 2dB for most models except ERA-5, where the noise figure increased by

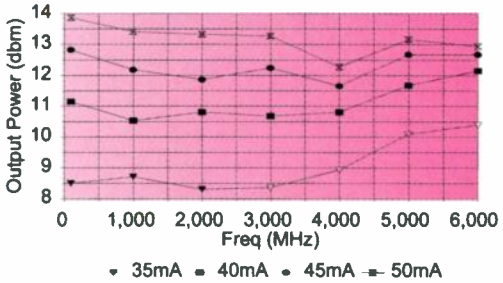
Table 4 ERA Performance At Various Device Currents

Model No.	Device Current mA	Type Gain @1GHz dB	Flatness to2GHz ±dB	VSWR IN @1GHz Typ.	VSWR OUT @1GHz Typ.	IP3 @1GHz dBm Typ.	Noise Figure @1GHz Typ.	Pout @1dB Comp. Typ. (dBm)
ERA-1	**40**	**12.2**	**.27**	**1.48**	**1.38**	**25.5**	**5.3**	**10.8**
	45	12.35	.27	1.51	1.39	27	---	12.1
	50	12.4	.28	1.52	1.40	29	7	13.2
ERA-2	**40**	**16.0**	**.27**	**1.39**	**1.30**	**26**	**4.6**	**11.6**
	45	16.1	.28	1.51	1.43	28	---	13.2
	50	16.1	.30	1.44	1.27	30	6	14.2
ERA-3	30	21.3	0.9	1.19	1.18	20.5	---	8.3
	35	**21.9**	**1.0**	**1.36**	**1.35**	**23**	**3.8**	**10.4**
	40	22.3	1.1	1.50	1.48	24	---	12.0
ERA-4	**65**	**13.6**	**.23**	**1.57**	**1.26**	**32.5**	**5.5**	**17.0**
	70	13.7	.21	1.62	1.34	33.5	---	18.1
	80	13.7	.20	1.60	1.33	36	5.2	19.1
ERA-5	**65**	**19.4**	**.75**	**1.27**	**1.08**	**33**	**4.5**	**18.4**
	70	19.3	0.9	1.25	1.13	34	---	18.9
	80	19.5	1.35	1.22	1.20	36	4.0	19.6
ERA-6	**70**	**11.2**	**.13**	**1.35**	**1.69**	**36**	**8.4**	**18.3**
	75	11.2	.12	1.31	1.68	37.5	---	18.8
	80	11.13	.12	1.29	1.80	39	8.7	19.3

OUTPUT POWER (1dB COMPRESSION)

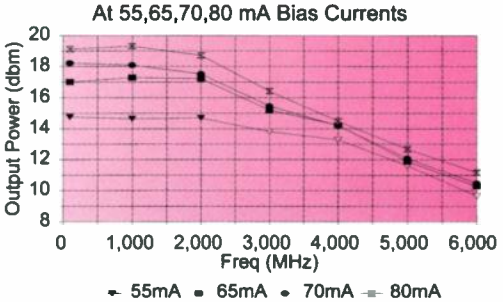
ERA-1SM 1dB Compression

At 35,40,45,50 mA Bias Currents



ERA-4SM 1dB Compression

At 55,65,70,80 mA Bias Currents



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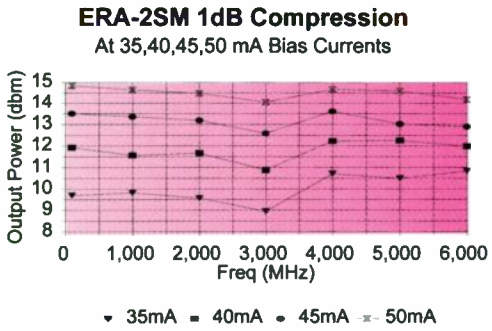
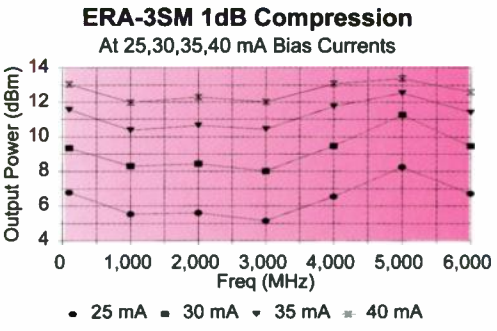
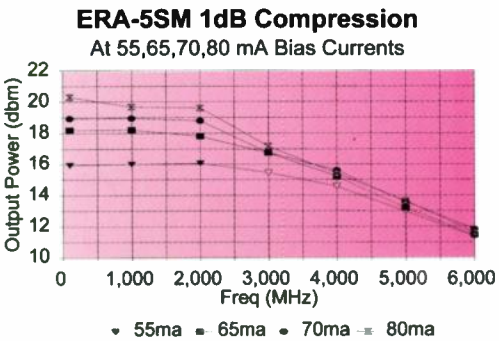
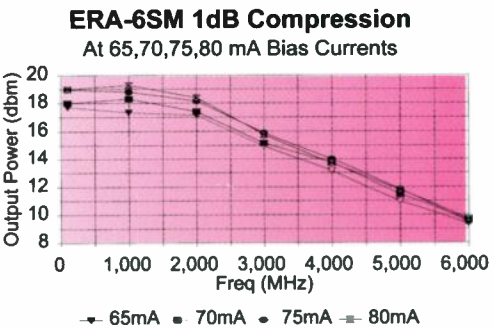
VS. CURRENT Figure 6









about half a dB. **Table 4** shows all the performance parameters with three different device currents. It can be seen in the above analysis and calculations that lowering the device current of the amplifiers will lower junction temperature, increase MTTF, and improve the life expectancy. The trade off will be a reduced output power and IP3. At this point, the user has to be aware of the main goal. If high output power is the main concern, or if ambient temperature is lower than the +85°C maximum specified, then the device current can be increased. If reliability and long life are the major concern, then lower device current is recommended. In any case, by the method shown above, the user can calculate the junction temperature and the MTTF. A decision can then be made about selecting a current level to best suit the need.

HBT TECHNOLOGY CONTRIBUTES TO ERA's SUPERIOR RELIABILITY

Heterojunction Bipolar Transistor (HBT) technology is the most advanced bipolar transistor technology providing very high frequency operation, and is used in all ERA's. The superior performance capability is due to the high electron mobility of Gallium Arsenide (GaAs), as compared to Silicon and the Heterojunction in the device. The material used for the base is different from the emitter, which is why the name Hererojunction is given. In an HBT, emitter and base are formed of semiconductors having different bandgaps. For the ERA's, the transistor is n-p-n, the emitter is made of $A1_{0.3}G_{a0.7}As$, and base of GaAs. The emitter has a wider bandgap 1.87eV than the base 1.43eV. The bandgap difference (Heterojunction) blocks the transportation of holes from the base into the emitter. Electrons have a higher mobility than holes. Preventing hole movement helps improve high frequency performance. This allows for a transistor design which has a higher base doping concentration than the emitter. Advantages include:

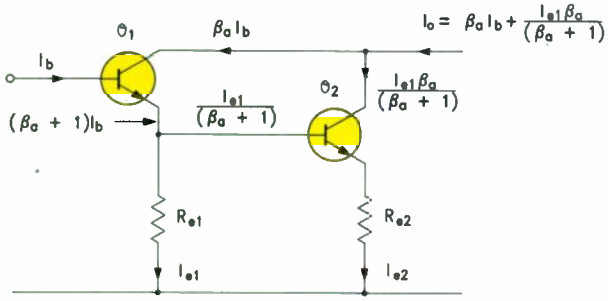
1) Lower base resistance - for higher RF power gain
2) Lower emitter-base capacitance
3) Higher emitter-base breakdown voltage
4) Higher early voltage

The very low base resistance allows the base to be made very thin, which increases f_t and current gain β. Beryllium doping is used as the p-type doping because of its excellent properties for HBT device fabrication using molecular beam epitaxial growth technology, including reproducible process control of a highly doped thin layer, excellent incorporation, and stability. Another dopant that is commonly considered for HBT fabrication is carbon. In a side by side test of equivalent devices fabricated with the same doping concentration, material thickness and process, experiments show greater than 100 times longer lifetime using beryllium doped HBT's produced by MBE versus carbon doped HBT's produced using MOCVD at the rated junction temperature.

DARLINGTON CIRCUIT CONFIGURATION

As previously described, HBT provides capabilities for high frequency amplifier design. Further enhancement of frequency of operation is provided by Darlington circuit topology. **Figure 10** shows the schematic of a Darlington amplifier.

Figure 10 Schematic of a Darlington Amplifier



Increased frequency of operation is explained as follows: Referring to **Figure 10**, let R_{e1} and R_{e2} be adjusted so the current is the same in R_{e1} and R_{e2}. The RF current gain β_a is greater than one, then $\beta_{comp} \simeq 2\beta_a$. Then, the composite current gain β_{comp} is approximately twice that of a single transistor. This effectively doubles the unity current gain frequency of the transistor. Hence, ERA amplifiers use Darlington topology to increase the operating bandwidth. **Figure 11** shows the schematic of ERA-1 to -3, and **Figure 12** of ERA-4 to -6. Note that multiple transistors are used at the output in **Figure 12** to increase the output power.

Figure 11 Schematic of a Darlington Pair (ERA-1 to -3)

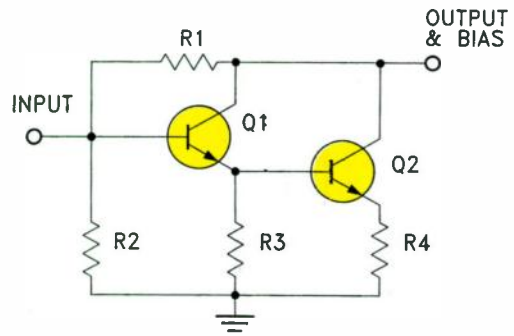
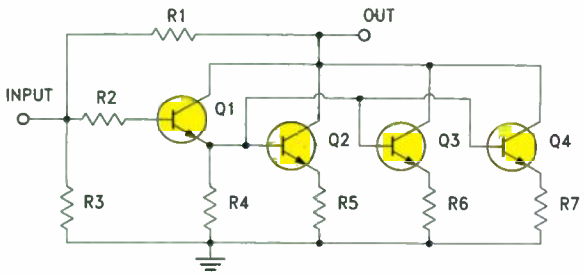


Figure 12 ERA-4 to -6 Schematic



ERA AMPLIFIERS GAIN, DEVICE VOLTAGE, OUTPUT POWER, AND IP3 CHANGE WITH TEMPERATURE AT CONSTANT CURRENT

ERA amplifiers were tested for device voltage and gain fluctuations over the entire temperature range in the specification of -45°C to +85°C. Units were mounted on a PC board, connectorized with SMA female at input and output. Biasing at constant current was done through the network analyzer HP8720C. Data was taken on 5 units individually at -45°C, -25°C, +25°C, and +85°C. **Table 5** below shows the device voltage change with temperature. The device voltage decreases with increasing temperature. The average device voltage temperature coefficient can be calculated to be -2 to -4mV/°C.

Table 5 Device Voltage vs. Temperature

Model	Device Current mA	Device Voltage (Volts)@ Temperature			
		-45°C	-25°C	+25°C	+85°C
ERA-1&SM	40	3.77	3.75	3.60	3.47
ERA-2&SM	40	3.75	3.72	3.60	3.49
ERA-3&SM	35	3.64	3.54	3.49	3.37
ERA-4&SM	65	5.31	5.20	5.05	4.85
ERA-5&SM	65	5.15	5.05	4.92	4.71
ERA-6&SM	70	5.76	5.74	5.60	5.42

Data was also taken on power gain at frequencies up to 10GHz at 4 temperatures using constant current. **Figure 7** shows fluctuation with temperature at various frequencies on ERA units. As you can see, gain decreases slightly with increasing temperature. Gain temperature slope can be calculated to be around -.003dB/°C for ERA-1, -2, and -6, and -.006dB/°C for ERA-3, -4, and -5. At the higher frequencies above 3GHz, the temperature gain slope gets steeper, especially for ERA-4, -5, and -6, as seen in the figures. Output power at 1dB compression on all ERA units showed about 1/2 to 1dB increase when temperature was increased from +25°C to +85°C. At low temperatures below +25°C, the output power also increased slightly then leveled off. **Figure 8** (page 14) shows 1dB output power vs. temperature for all ERA amplifiers. IP3 analysis over temperature was also done for all ERA units. For ERA-1, -2, and -3, IP3 rises with increasing temperature then, above room temperature, levels off. For ERA-4, -5, and -6, IP3 decreases with increasing temperature, then levels off above room temperature. The total variation of IP3 in the entire temperature range is about 2dB. **Figure 9** (page 15) shows the IP3 variation over temperature. Data was taken at 2GHz for ERA-1, -2, -3, and 1GHz for ERA-4, -5, and -6. These are the same parameters specified in the specification table.

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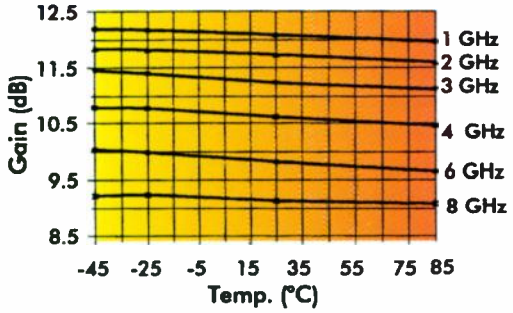
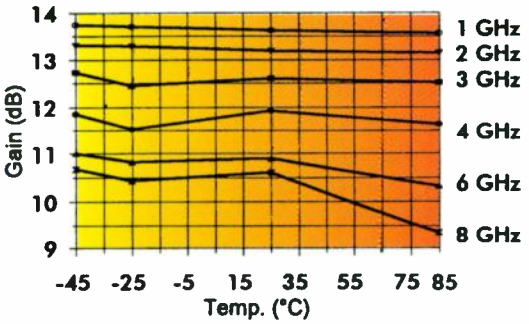
TEMPERATURE

GAIN VS. TEMPERATURE Figure 7

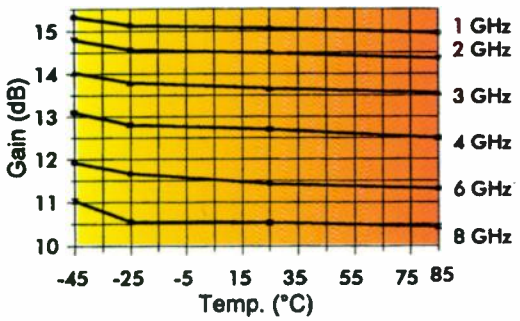
ERA-1SM Gain vs. Temperature @ 40 mA



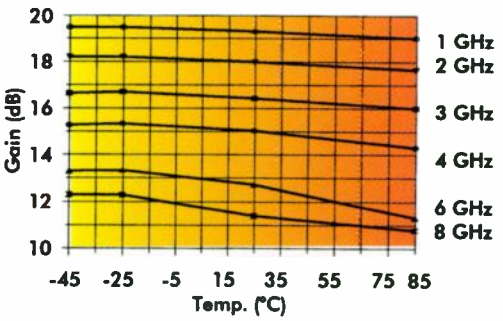
ERA-4SM Gain vs. Temperature @ 65 mA



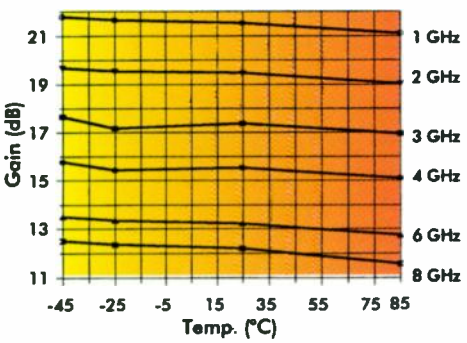
ERA-2SM Gain vs. Temperature @ 40 mA



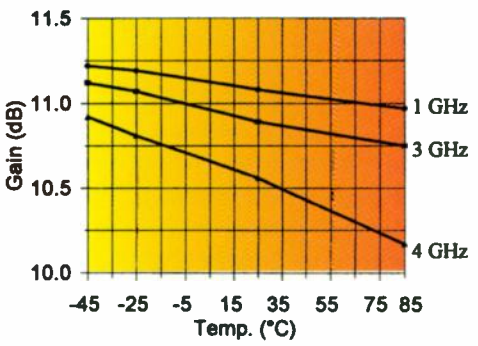
ERA-5SM Gain vs. Temperature @ 65 mA



ERA-3SM Gain vs. Temperature @ 35 mA



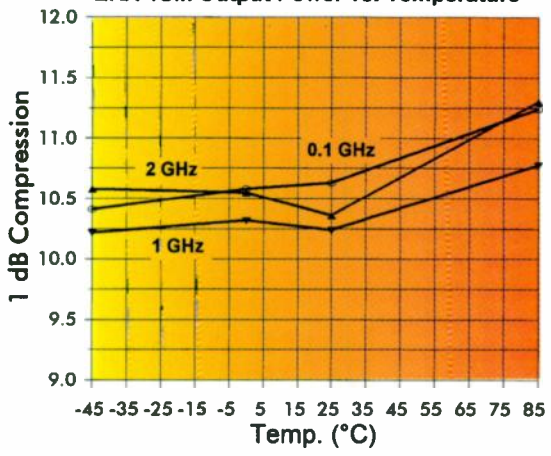
ERA-6SM Gain vs. Temperature @ 70 mA



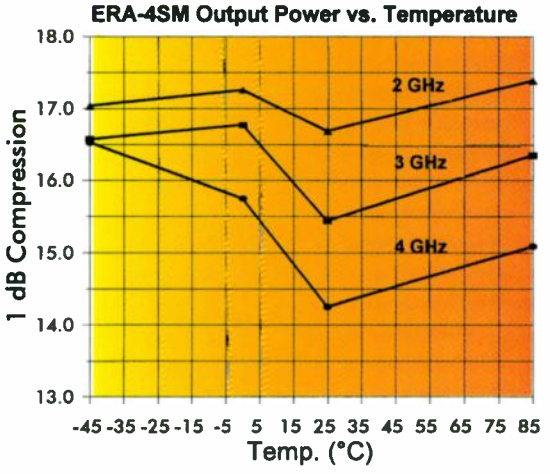
PERFORMANCE VS. TEMPERATURE

OUTPUT POWER VS. TEMPERATURE *Figure 8*

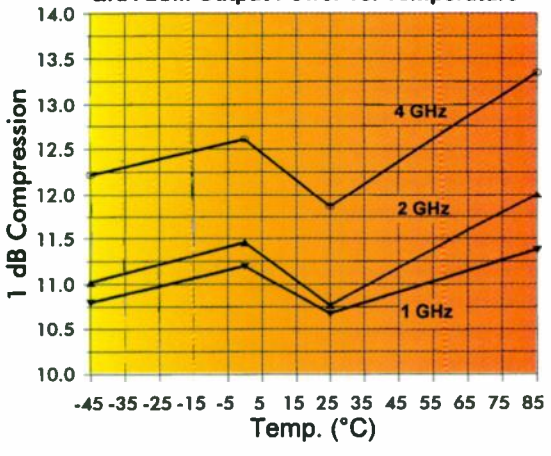
ERA-1SM Output Power vs. Temperature



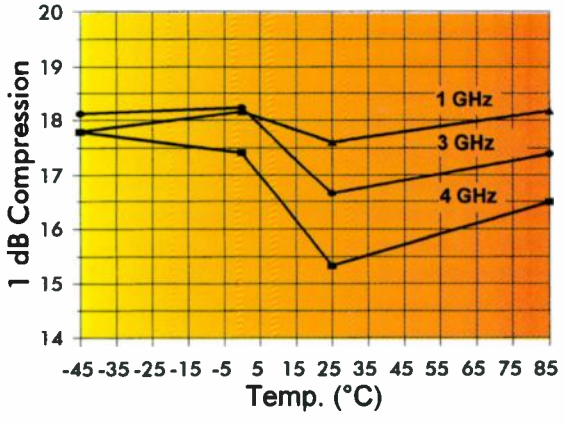
ERA-4SM Output Power vs. Temperature



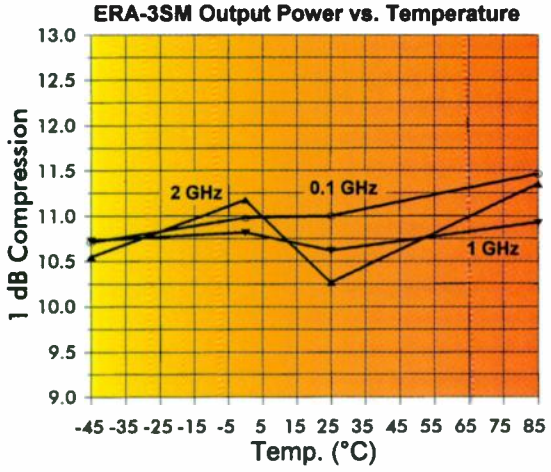
ERA-2SM Output Power vs. Temperature



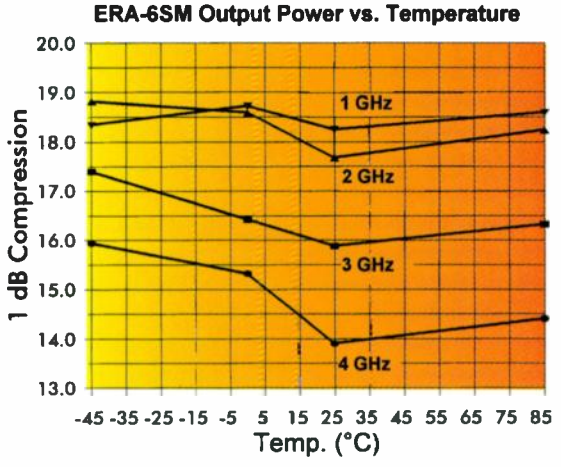
ERA-5SM Output Power vs. Temperature



ERA-3SM Output Power vs. Temperature



ERA-6SM Output Power vs. Temperature



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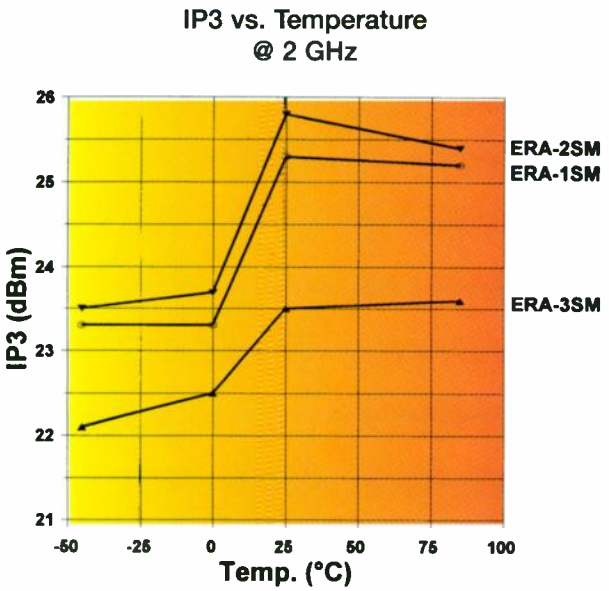
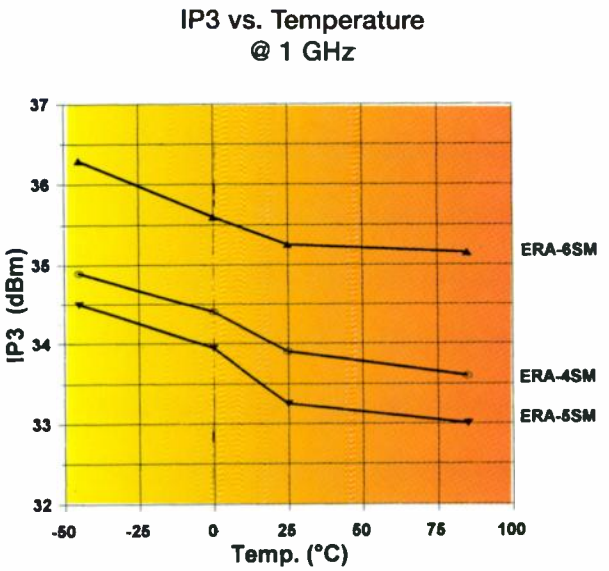
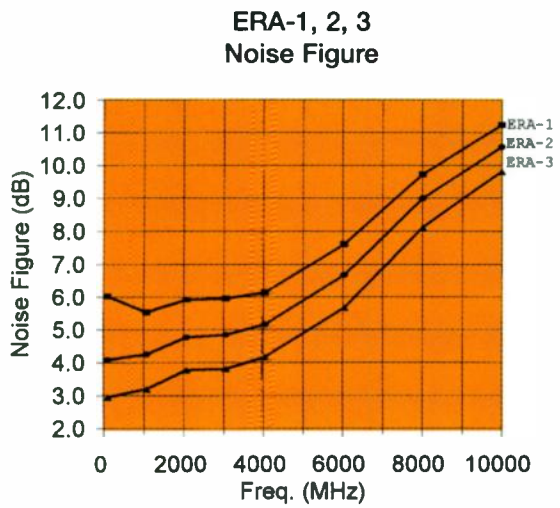
IP3 VS. TEMPERATURE Figure 9

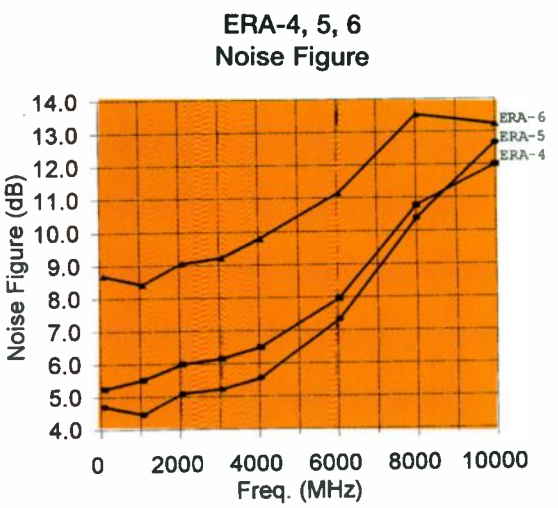




NOISE FIGURE (AT 25°C) Figure 10

Noise figure measurements were performed on all ERA amplifiers in frequencies from 100MHz to 10GHz. ERA-3 has the lowest noise figure among the 6 models, which is around 3dB at 100MHz, followed by ERA-2 and ERA-5. ERA-6 has the highest noise figure which is around 8dB at 1GHz. Noise figure increases with increasing frequency in all ERA models. **Figure 10** illustrates the graphs for noise figure of all ERA amplifiers for frequencies up to 10GHz.





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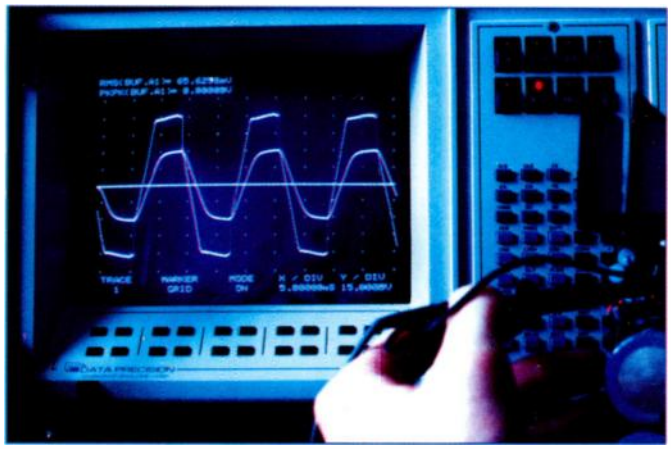

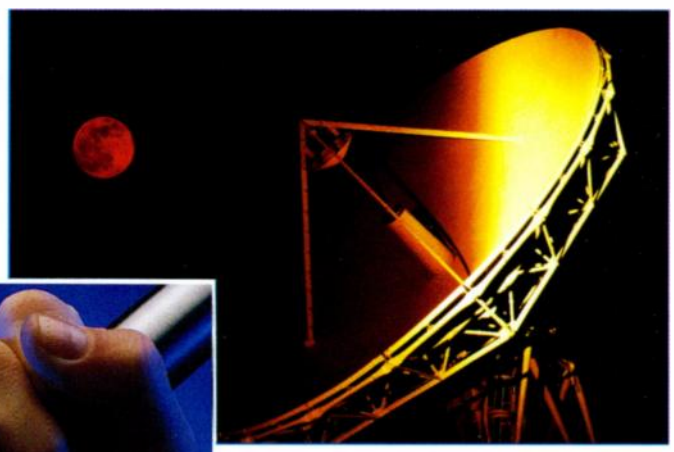

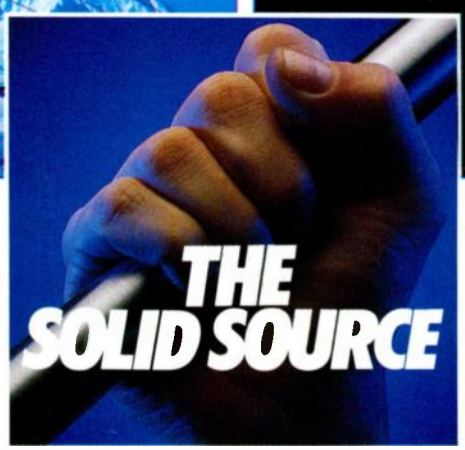

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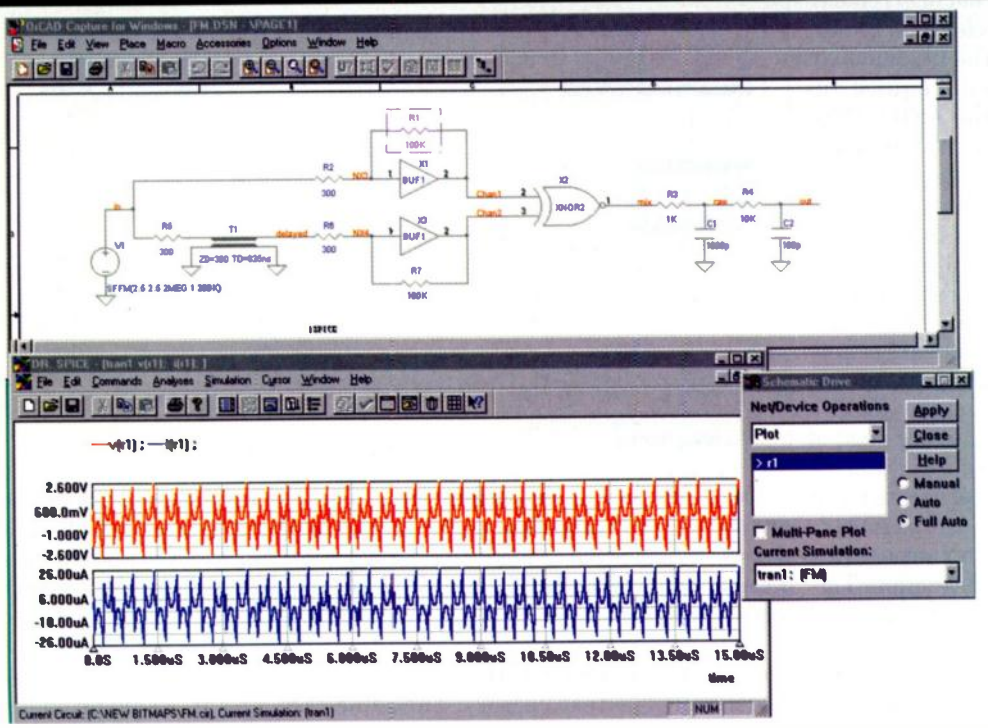

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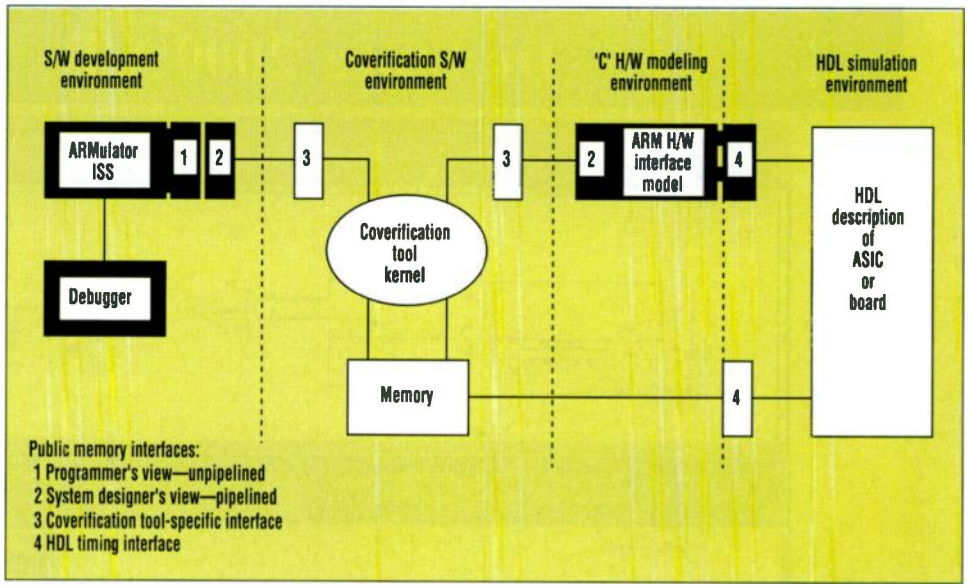
goal is to perform hardware and software integration and to verify it before committing to silicon. This not only reduces the design cycle *(Fig. 2)*, but also reduces the likelihood of errors that will require another spin of the ASIC. "The only way to verify the hardware/software interface," says Mentor's marketing director Jim Kenney, "is to run some code on that embedded core and have it interact with the rest of the ASIC logic."

Logic simulators are simply too slow to run any reasonable amount of software to exercise the ASIC logic. Since most of the code in a real system affects only the processor and memory status, it is possible to simulate those operations at a high level of abstraction. This leaves the relatively small amount of code that affects hardware external to the processor. This code can be sent to the bus model in Verilog or VHDL form, greatly speeding up the simulation. In fact, this arrangement generally makes the external logic the bottleneck to simulation speed rather than the processor. The processor models make it possible to take software from a number of sources and run it against the ASIC gates to verify the correctness of both the hardware/software interface and the working of the custom logic.



2. A hardware/software coverification setup—in this case, an ARM design running in the Mentor Seamless environment—lets you simultaneously observe the behavior of hardware and software. The instruction set simulator talks to an HDL interface model via the coverification tool. A normal software source-level debugger can be used on the ISS side while the hardware debugger in the HDL simulator can display the behavior of the ASIC.

Benefits of Coverification

The ability to test the logic with real software provides another advantage. Normally, when designing test benches for logic designs, these test benches are written in VHDL or Verilog. They often get huge, sometimes bigger than the design itself. The problem is that once you've got silicon, the test benches can no longer be used to test the prototype.

With a coverification system, you can begin writing prototype code in C that will functionally exercise the hardware. With Eaglei, you can generate test vectors in C that derive not from a hardware designer's idea of how the hardware should work, but from a software engineer's idea of how the system should work. Basically, the person who is developing the device drivers becomes the person generating the test vectors. The same test vectors used to test the VHDL or Verilog model can later be used to almost automatically generate a prototype diagnostic suite to test the real silicon. The code can even be refined and developed as the hardware design progresses, further collapsing the design and integration time.

Since most, if not all, of the driver software for the on-chip peripherals will run from on-chip ROM, getting the driver code right is essential, whether the peripherals are full-custom designs or intellectual property (IP) purchased from an ASIC vendor. When commercially sold macrocells are used, they sometimes come with some driver code. However, that code is usually in the form of a template or example code and needs to be further refined to be of practical use in a particular ASIC design.

In some cases, such as a security system using smart cards, an entire application will be expected to run from on-chip masked ROM. In such systems it is necessary to thoroughly test a large amount of software against on-chip hardware before risking a prototype. Mentor offers the XRAY development tools including the XRAYsim instruction set simulators and the XRAY debugger from its subsidiary, Microtec, Santa Clara, Calif. Eagle provides an open interface to third-party software development tools and debuggers. Both parties support all major hardware simulators. Since logic simulators include a hardware debugger, developers can control and observe hardware and software execution simultaneously. You can choose to set breakpoints in either hardware or software.

Speeding Board Design

For core-based ASICs, full modeling of hardware and software and the use of an instruction set simulator is the most popular approach. The ISS masks out much of the internal processor logic but retains a model of the internal register activity. While the ISS processor model runs somewhat slower than the more abstract processor models such as Mentor's NCS or Eagle's high level language VSP, it's level of detail is usually needed for verifying the internal interfaces. For board-level designs where a model of an off-the-shelf CPU will do, the NCS or VSPs of a higher level of abstraction run faster, since you can assume that the processor works correctly.

Both Mentor's Seamless and Eagle's Eaglei can be applied to board-level designs as well as to ASIC designs. In board-level designs, when

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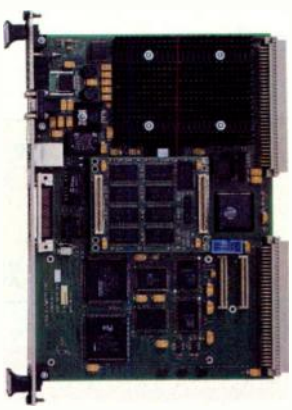

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using a commercially-available microprocessor, you're more likely to use the more abstract (and faster) processor model because the focus of the design is on the board, not the processor, which is assumed to work correctly. Often, you may be working with a mix of off-the-shelf hardware and some custom ASIC designs.

Eagle is working with Applied Microsystems, Redmond, Wash., to include real hardware in the virtual environment along with simulated hardware. This can speed simulation by only requiring simulation of custom designs and letting proven silicon peripherals run on their own. The virtual software processor-target access probe (VSP/TAP) lets you use the actual target microprocessor, operating system, and firmware to run simulated hardware.

The VSP/TAP uses an 'interposer" board to implement a testing interface between the target processor and software. The board is connected to the Eaglei simulation environment by means of an Applied Microsystems emulator. The emulator detects requests for virtual target access, puts the processor on hold and sends the information to Eaglei. When the hardware responds, results are sent back to the Eaglei environment and on to the VSP/TAP, which presents the bus information to the software and releases the processor.

As systems become more complex and hardware revisions more expensive, detailed coverification of the interaction between hardware and software will become more attractive. Not only can coverification avoid costly re-spins of custom hardware, it also can shorten the overall process of hardware/software integration and provide economic benefits to ASIC developers by shortening vital time to market.

For further information contact Mentor Graphics, 8005 SW Boeckman Rd., Wilsonville, OR 97070; Internet: http://www.mentorg.com; and Eagle Design Automation. 13515 SW Millikan Way, Beaverton, OR 97005; (503) 646-3884; Internet: http://www.eagledes.com; Applied Microsystems, 5020 148th Avenue NE, P.O. Box 9702, Redmond, WA; (206) 882-2000; Internet: http://www.amc.com.

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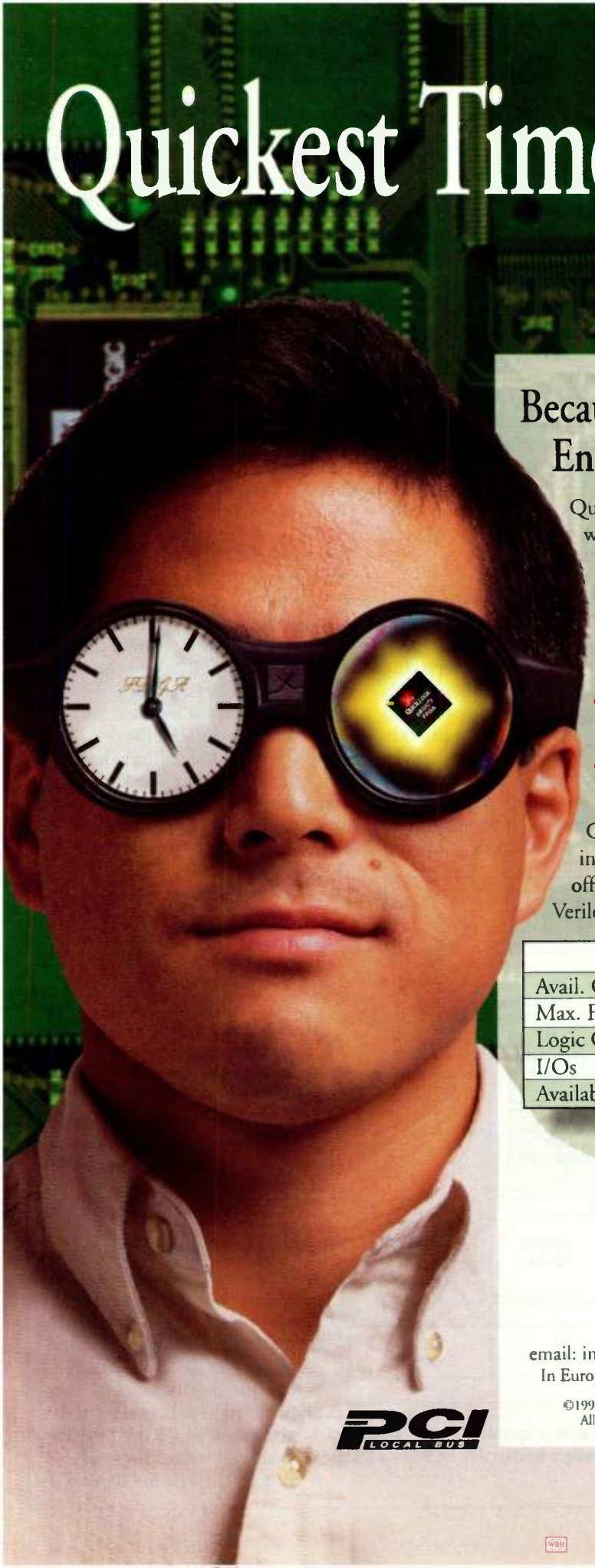

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UPDATE ON MODULAR SOFTWARE

Modular Software Speeds Development Of Web Appliances For Consumer Use

A new generation of embedded systems is about to appear—the information appliance. Information appliances will be consumer products with the underlying computer technology so deeply embedded that users should be essentially unaware that they are dealing with a computer. As with common household appliances like toasters, blenders, and washing machines, information appliances will be dedicated to a single purpose. For the most part, they will connect to the Internet and may involve subscription to some kind of information service, such as on-line yellow pages, travel information, food and recipe data, financial information, or e-mail.

Diba Inc., Menlo Park, Calif., is gearing up to support the design and development of information appliances with a suite of modular software that will let developers customize and differentiate their products and allow for modular enhancements. According to Joe Gillach, Diba's vice-president of marketing, a vast, untapped market of consumers still do not relate to computers. They have no idea how to search for information and have no interest in "surfing the Web" to find information. These consumers could be convinced to buy information appliances if they addressed a direct informational need without being aware of the computing involved. The concept is similar to how users of satellite TV systems and cellular phones meet their information needs without being aware that they are interacting with vast networks of computers.

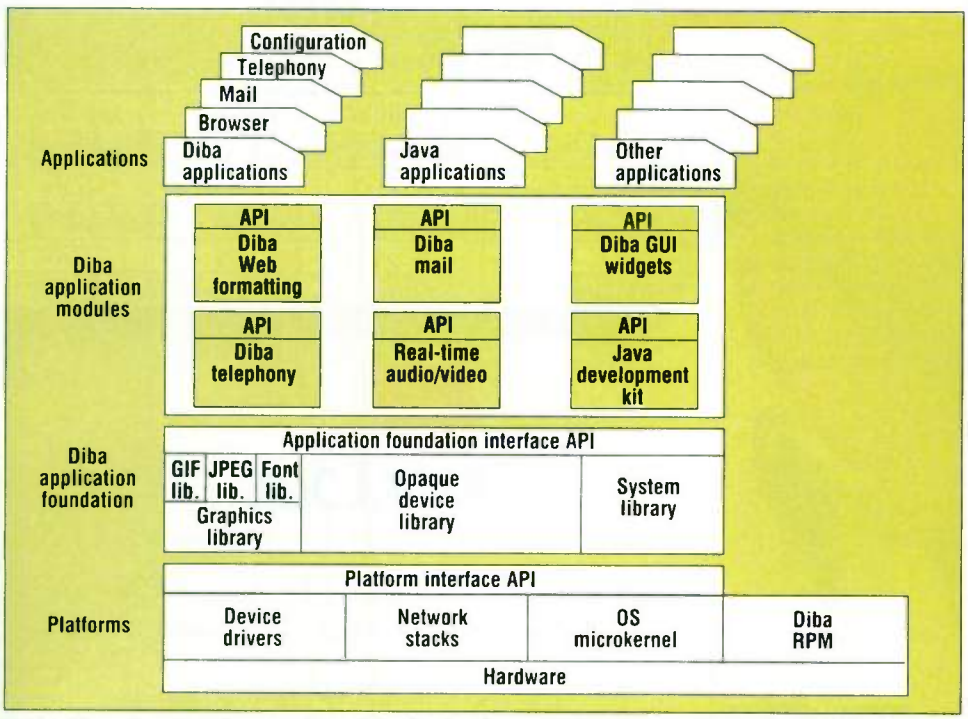
Setting The Foundation

The appearance of information appliances will depend on a chicken-and-egg scenario. Low-cost, user-friendly devices that meet consumers' needs must be available, and there must be an infrastructure in place to provide the needed information services. In other words, both client and server technologies are required. Diba is addressing the first requirement, but its customers, besides building the devices, must also see to it that the second requirement is in place to make those devices useful.

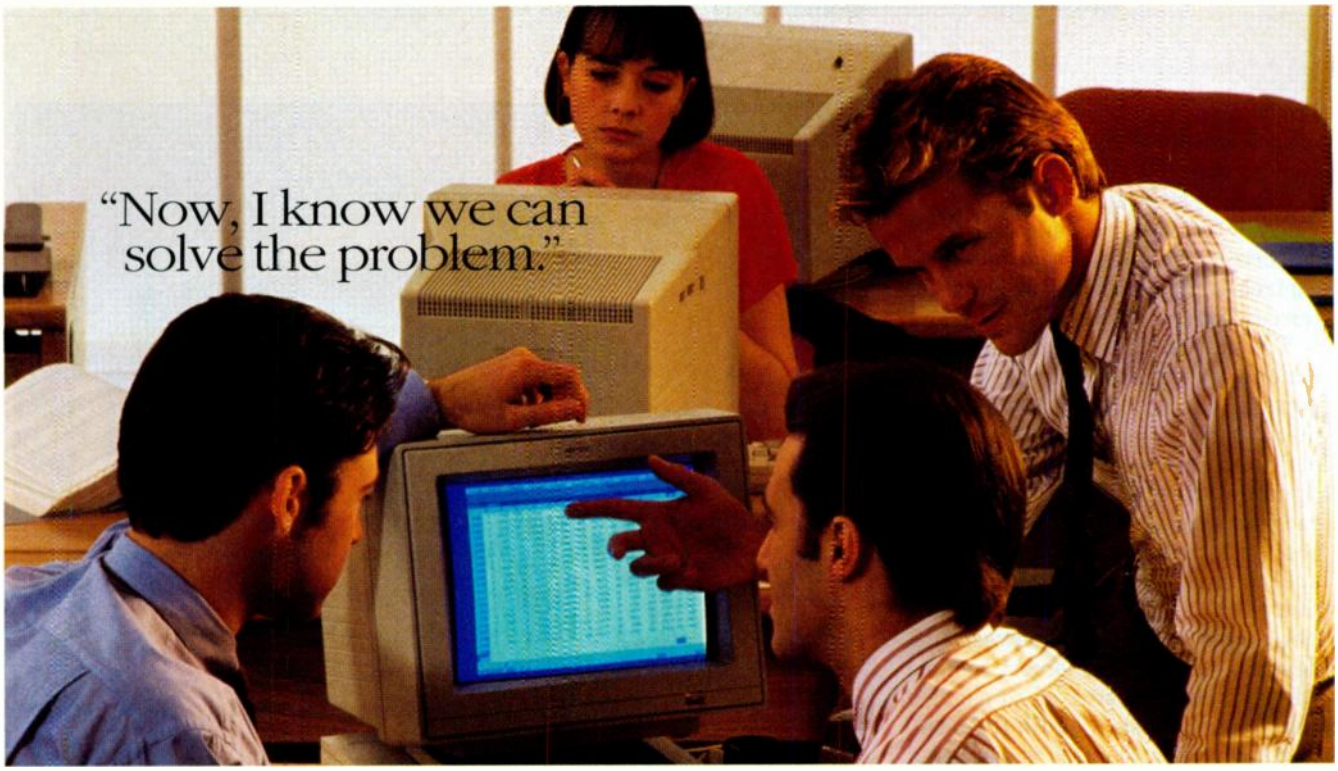
The Diba software is organized in four layers, each with its own open API *(Fig. 1)*. This architecture gives the OEM a range of options for differentiating a product and for making time-to-market trade-offs. The lowest layer is the platform layer, which is built around a microprocessor and a microkernel. The microkernel can be almost any modern microkernel that supports multitasking and multithreading. Currently, Diba supports ITRON from several Japanese vendors for the Mitsubishi M32R/D, and pSOS from Integrated Systems, Sunnyvale, Calif., for the PowerPC and Motorola 68000. The company plans to add support for Linux and Windows NT for the Intel architecture. Diba also supplies its own lightweight (120 k) microkernel for the M32R/D, the 68000 and PowerPC, and the NEC V830. In addition, Diba can work with customers to port other microkernels, like OS/9 from Microware, Des Moines, Iowa, to the platform layer.

In addition to the microkernel/microprocessor combination, the platform layer includes a portable TCP/IP stack, which can support either TCP/IP or UDP/IP, and a set of device drivers. The drivers are modular and support network connections, I/O devices, modems, graphics chips, touch screens, and so on. Developers can license the drivers they need, or can write their own. Another part of the platform layer is the remote provisioning and maintenance (RPM) module, which is a software upgrade and maintenance system. The RPM performs power-up verification and provides for downloading and installing software upgrades.

On top of the platform layer is the application foundation, which supplies generic services that interact with the platform layer to access hardware-specific functions. The opaque device library supports general classes of devices such as I/O devices. The same call to the display function in the opaque device li-



1. The Diba software architecture is structured in four layers, each with an open API. This lets developers and OEMs make trade-offs between quick time-to-market versus unique functionality. OEMs need license only those parts of each layer they need.



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brary can access drivers for a variety of specific devices such as TV, LCDs of varying sizes and resolution, and VGA displays. The graphics library provides 2D drawing, imaging, and screen rasterizing routines; screen and color controls; and font control, including international characters.

The system library provides applications with five infrastructure components. The first is memory management with a special emphasis on defragmentation. The memory management component also handles caching of web content to provide the best performance from the user's perspective, given the limited memory that will be available in many information appliances. Like a browser on a desktop system, the memory module will instantly display cached pages if they are requested again from the web connection. Content is discarded on a least-recently used basis.

Other system services include a real-time clock interface, along with time stamps for e-mail messages, an error handling mechanism that can either invoke appropriate responses to errors or route them to a general error handler, and a messaging queue paradigm for communication between threads and program units. A thread and state management module supports a threading architecture based on the POSIX model, which gives developers a familiar interface. It also allows the creation of complex multithreaded applications or the construction of a suite of related applications for a given appliance.

Many OEMs may be content to start developing at the application foundation layer. Indeed, some who don't need a user interface may even start at the platform layer. For those developers with tighter time-to-market constraints, another layer of application modules provides general services that can be expected in a wide variety of specific applications. Developers can start with the modules, then modify and build on them to focus on the unique aspects of their specific applications.

One such device is the web formatting module. Web pages exist on web servers in a given format and must be displayed on a variety of devices ranging from TVs to LCDs in different formats. The formatting module formats the page content appropriately to the target display device, and sends the content to the display service in the opaque device library, which then calls the driver for the physical device.

2. One concept-design prototype for an information appliance is an e-mail device integrated with standard telephone and fax capabilities.

Other application modules include a mail module that supports SMTP, POP3, and IMAP4 protocols, and implements MIME encoding and decoding. A GUI widget module provides the foundation for user interface elements and includes a text editor. Widgets include the familiar dialog boxes, buttons, check boxes, and radio buttons and pop-up menus. A telephony module supplies a suite of voice and fax functions as well as dialing, conference calling, call waiting, hold, and mute. Diba also is working on advanced functions such as caller ID and support for the telephony API (TAPI) of Windows 95 and Windows NT. A real-time audio module supports .WAV and .AU formats and can be extended to other audio formats. The company also is looking for partners to implement real-time video.

The appearance of information appliances will depend on a chicken-and-egg scenario.

Finally, for developers who need to get to market immediately, there are some ready-made applications—including a browser, a mail and telephony application, and configuration code—to get a complete turnkey system put into a plastic enclosure and onto the market in the shortest possible time. Even these applications could be differentiated by the choice of display, user interface (touch screen vs. buttons), and processor/microkernel choices.

Examples And Infrastructure

While Diba is not in the business of designing and selling consumer electronics, it has proposed several sample products, and has built some prototypes to demonstrate potential applications, including a mail appliance with a telephone *(Fig. 2)*. This device can be used as a normal telephone and

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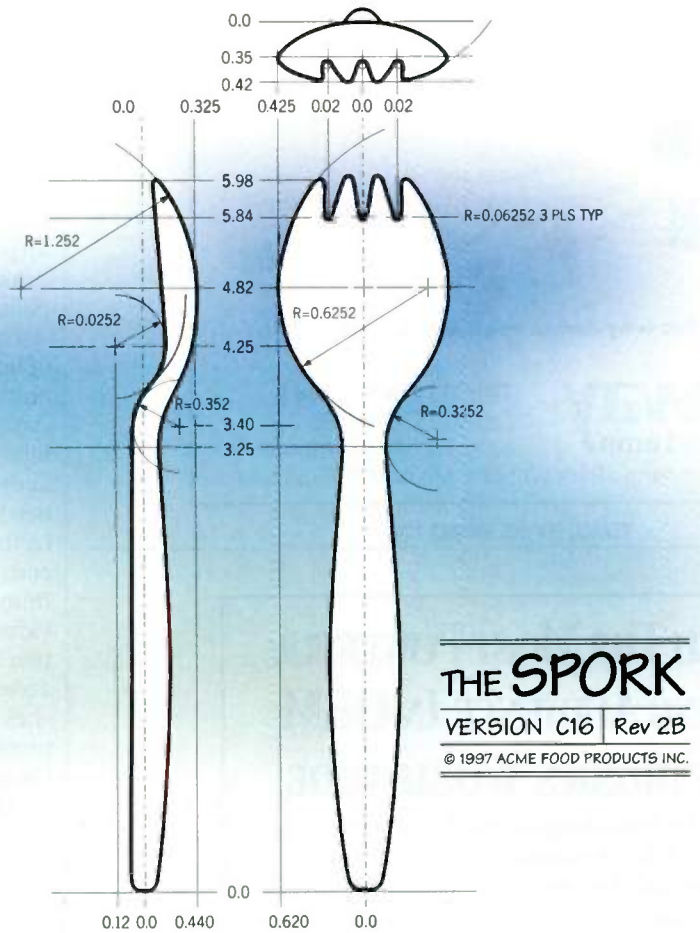

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fax with autodialing from a database displayed on its LCD screen. It also can be used as an e-mail appliance using the internal software and a fold-down keyboard. A kitchen appliance that mounts under a cabinet can be used to retrieve and display recipes from a CD-ROM or from web sites maintained and coordinated by an information provider.

Other examples include a "Yellow Pages" appliance that looks up entries based on a keyword search or by use of a slider for browsing within a limited area, and also prints out addresses and phone numbers. A financial assistant, a travel guide that can download tourist information from local kiosks in airports, and a Web-TV device give some idea of the range of possible appliance designs.

Of course, much of the functionality of information appliances will depend on the underlying information infrastructure. The average consumer is not interested in surfing the Web, but has specific and immediate information needs. This suggests that many manufacturers of information appliances will earn the majority of their revenue not from the sale of the devices, but by providing focused and up-to-date information. They can lock-in their products to access a single or limited number of sites and sell subscriptions, or they can provide custom servers that work with the appliances.

At the moment, Diba is concentrating on the client side, but the company has plans to add server technology. That way, a manufacturer could coordinate the design of the appliance with the design of the supporting information service. In addition to serving manufacturers who want to bundle information services with their appliance products, the server technology also is intended to address the needs of ISPs who want to deliver value-added services to the general Web audience. Among some of the planned features of these types of services are remote upgrade and maintenance services, registration services, parental blocking, and real-time audio and video streaming.

For further information contact Diba Inc., 3355 Edison Way, Menlo Park, CA 94025; (415) 482-3400; http://www.diba.com.

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UPDATE ON CODE OPTIMIZATION

Profiling Compiler Automates Code Optimization Process

A new compiler technology automates optimization decisions based on the actual, run-time behavior of an application. The first introduction of the profiling compiler technology is by Intel Corp. in its CTOOOLS development suite for the i960 RISC processor family. However, the technology's principles can be applied more broadly.

While designers have been able to base optimization decisions on runtime performance profiles in the past, doing so required a separate, time-consuming process. Intel has integrated its profile-driven compiler optimization process into the make environment so it is transparent to the user, eliminates the need to hand-tune the code, and improves performance by 20 to 30%.

Profile-driven optimization involves instrumenting the code and then running the application to gather performance information based on what the code really does. You can choose to instrument-selected portions of the program or the entire application. The instrumented code added to the executable code captures a number of critical parameters, like the number of times each function is called from different sites, the number of times a global variable is referenced, the number of times each statement in the program is executed, and the average number of times various subroutine loops are executed. The instrumented code can be run as many times as desired using different possible real-world conditions.

The information gathered during profiling is kept in a database and used by the optimization utility supplied with the compiler *(see the figure)*. For example, the database can provide information on what functions are suitable for inlining to reduce call-return overhead. The optimization utility can use the data to help optimize instruction-cache utilization by identifying frequently taken paths of execution. By identifying these paths, he utility can arrange basic blocks so they execute sequentially in time into the same sequence in the object code, resulting in a greater cache hit rate. It also can identify available resources, such as registers, that may be allocated to frequently executed parts of the program.

Another profile-driven optimization is the formation of superblocks. This involves selective code replication to form larger and larger blocks that can be very effectively optimized. For example, if an if-then-else statement contains a sequence of blocks that are executed the majority of the time, they can be merged into a larger block and the branch that is much less often taken can be separate from this new block. This allows other optimizations on the superblock without having to deal with the less-often taken branch. The result is faster execution but larger code size.

Automating the profiling and optimization process eliminates the need to bring in a processor expert and compiler expert as a separate step in the development process. However, it does require automated aids for the user to manage the database and the different versions of profiles and object modules that will be created for a given application.

Profile-driven optimization requires two compilation steps: instrumentation recompilation. Users must ensure that their sources do not change between these steps. There are two sets of object files to manage, instrumented objects and recompiled objects. A change to one object may require changes in other object modules that are dependent on it.

Because profiles are based on a given version of source code, any significant changes to the source will render a profile useless. In addition, it may be necessary to generate new profiles if an application's operating conditions change. Intel has introduced the concept of "stretched" profiles where a program profile can be extrapolated to fit a slightly modified source program; however, any major changes will require new profiles.

The program database is implemented as a Unix or Windows directory and is accessed via a user interface. It stores multiple versions of object modules. Some may be instrumented for use in creating profile data. Others may contain debug code and yet others may have been optimized using an existing profile. Each of these may come from the same source module. The compiler and linker switches used in a particular build determine which object module from a given source module is linked into the final image. The system also performs dependency analysis to determine which modules must be recompiled and which versions of a source module can be reused.

For further information, contact Intel Corp., 2200 Mission College Blvd., P.O. Box 58119, Santa Clara, CA 95052; (800) 628-8686; http://developer.intel.com.

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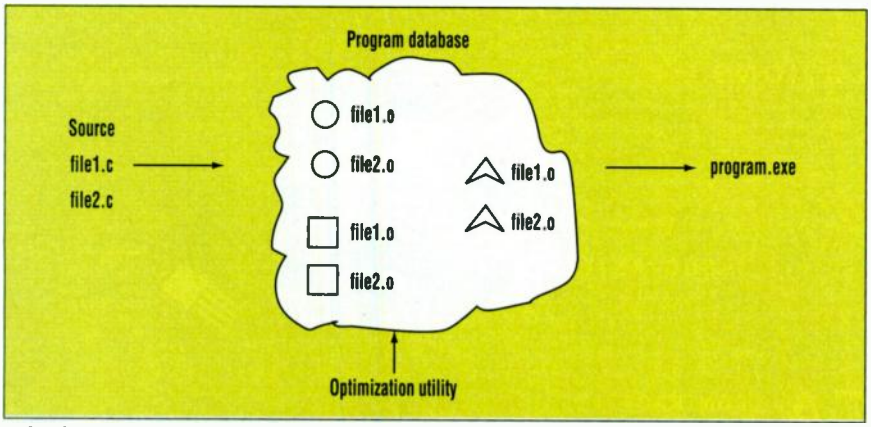

A database stores information gathered during profiling. The optimization utility and the management of the program database are controlled from a graphical user interface, so the details of the implementation are hidden from the user.

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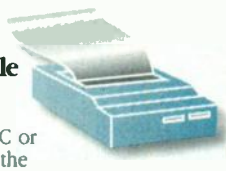

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FPGAs Take On The PCI Performance Challenge

The Latest Generation FPGAs Now Have The Density And Performance To Handle The Speed And Complexity Of PCI.

Dave Bursky

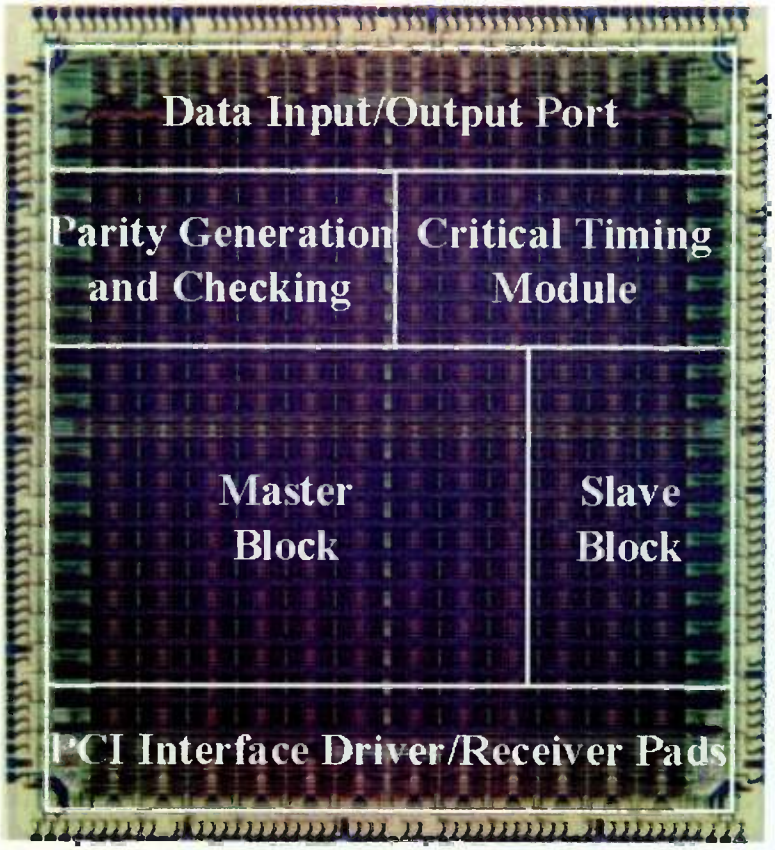
SPECIAL REPORT

Although developed as a bus to interconnect high-speed peripheral circuits to the host CPU, the PCI bus has not only become a standard expansion bus in the PC, but it also serves a variety of other applications from industrial control systems to network bridges and routers. The broad range of applications that PCI or PCI-like interfaces serve allows designers to create custom versions of the PCI interfaces. By customizing the interface, designers can better optimize performance and cost by removing unused features and functions, and adding custom logic to better match their system needs.

For prototyping and low-volume production needs, programmable logic chips provide designers with the ideal building blocks to build PCI interfaces. However, only in the last few years has the density (gate count) and performance of field-programmable gate arrays (FPGAs) reached sufficient levels for them to handle the PCI-interface function in a single chip.

There are currently seven FPGA suppliers that have devices with enough gates on the them to hold the PCI target or PCI master/target controller. Those suppliers include Actel, Altera, Atmel, GateField, Lucent, QuickLogic, and Xilinx. To support the PCI interface, these companies have, in most cases, developed their own megacell circuit functions that are a combination of handcrafted logic and high-level design software.

To provide additional support capability, the silicon suppliers have struck licensing or partnership deals with several independent intellectual property (IP) suppliers such as CAE Technology (now part of the Inventia Div. of Mentor Graphics), Virtual Chips (now part of Phoenix Technologies), Sand Microelectronics, Eureka Technology, and Toucan Technology, that provide HDL-based PCI designs for use on ASICs and FPGAs. These blocks of IP can be licensed, modified, and then synthesized using the ASIC's or FPGA's design library to create a custom version of the PCI controller.



Art Courtesy: QuickLogic

However, PCI is not a simple interface to implement. In fact, even FPGA suppliers admit that designers who want to do a good PCI block should have already studied PCI inside and out, to ensure the proper selection of features and the timing parameters. Additionally, for FPGA suppliers, they must be able to meet tight timing requirements and have the logic density

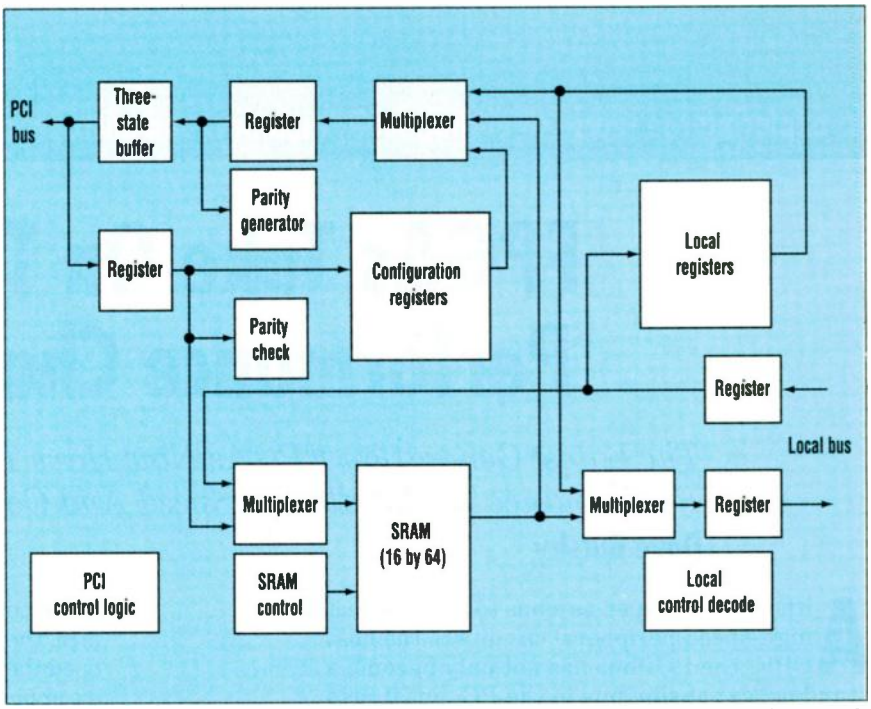
and routability to handle functions such as 36-bit parity generation and checking, configuration registers, 36-bit input and output pipelines, and bus control logic.

For the PC market, PCI cards typically are implemented in one of the two main variations—target only or master/target. The target interface responds to a master-controller request and cannot initiate data-transfer operations. It is the simpler of the two main PCI options, requiring between 2000 and 3000 gates to implement the interface. Target-only interfaces must use FPGAs that contain 4000 or more usable gates.

The more complex master/target interface can initiate operations, perform DMA transfers, and other more-complex data-management functions. It requires about triple the logic (6000 to 8000 gates), and must use FPGAs that contain at least 8000 usable gates to ensure the block can be placed on the array. In either instance, a larger FPGA might typically be used to accommodate the system-specific logic the designer wants to incorporate along with the PCI interface.

Although FPGAs provide designers with the ability to reuse the logic and try various options without the high expense and long delay of mask iterations, other fast turn-around options—such as laser-programmed gate arrays (LPGAs)—can provide some of the same flexibility with full gate-array architecture and performance. However, it will take one to seven days to get a prototype, and the initial cost will be higher.

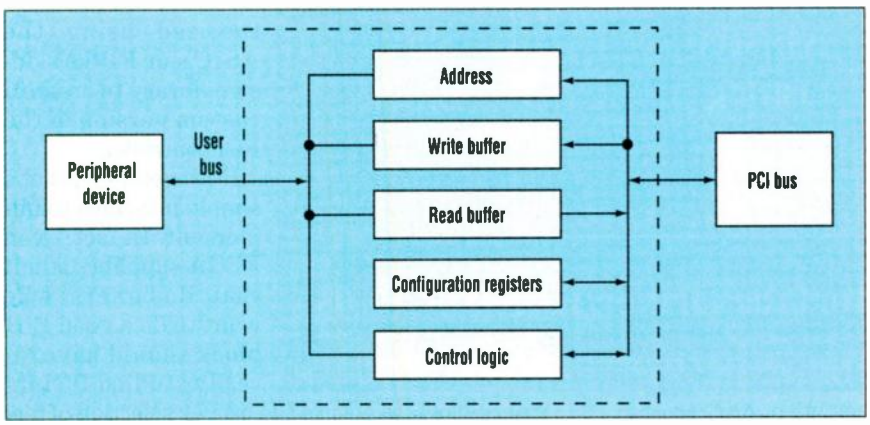
The higher cost, though, of the LPGAs is counterbalanced by the much shorter development cycles. Since LPGAs have a true gate-array architecture, they can deliver the full 33-MHz performance required by PCI with minimal effort. On the other hand, FPGA solutions require handcrafted logic to extract the best performance. It will be the rare case in which synthesis and automatic place-and-route tools can be used to implement a full-performance PCI interface on an FPGA. Furthermore, handcrafting may require several iterations to achieve the desired performance.



2. A master/target PCI interface offered by Lucent Technologies on its 2CxxA and 3C families of OrCA field-programmable logic arrays has many features. They include parity generation and checking, configuration registers, a 128-byte SRAM for data buffering, and bus-control logic. The cell requires between 6000 and 8000 equivalent logic gates.

To clarify the definitions of what is and what isn't PCI, let's set a few discussion ground rules. For full PCI specification compliance the interface must operate at 33 MHz with no wait states. Additionally, the signal interface must meet the 11-ns clock-to-output time, the 7-ns clock-to-input (setup) time, and the 0-ns hold-to-system-clock time required by the PCI specification (*see Checking Out The Design," p. 118)*. The signal interface also must provide the current drive and low-leakage current required to meet the load requirements (10 pF loading with less than 70 nA of leakage current). If it can't meet the timing or drive specifications, the interface becomes PCI-like, but not PCI compliant. Granted, not all systems require the full-PCI timing compliance, thus having a PCI-like interface is still an acceptable solution.

The PCI target interface is the more widely available block for FPGA implementation. It requires the creation of read and write buffers, configuration registers, address control, and general control logic for the PCI-bus signals *(Fig. 1)*. Such a megafunction is available from nearly every FPGA



1. The PCI target interface as offered by Altera is a relatively simple logic block of between 2000 and 3000 gates. It provides read and write buffers, configuration registers, some control logic, and address logic.

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DG409	4 Ch. Diff.	DG509A, HI-0509

Analog Switches

Part #	Function	Replaces
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DG403	Dual SPDT	DG191, HI-5043, IH5043, IH5143
DG405	Dual DPST	DG184, HI-5045, IH5145
DG411	Quad SPST	DG211 Upgrade
DG412	Quad SPST	DG212 Upgrade
DG413	Quad SPST	DG211/DG212
DG441	Quad SPST	D201A, HI-0201
DG442	Quad SPST	DG202
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supplier, however some implementations don't offer 100% compliance with the PCI specification. Since the mega-

DMA engine, and select other features to enable or disable.

One target megafunction devel-

•A synchronous user bus which is normally used in 486-based PC systems. All transfers are fully synchronized

DIGITAL DESIGN PCI ON FPGAs

a user bus. As data is written into the buffer, a data transfer on the bus can take place simultaneously, allowing the bus to perform other write operations. The peripheral device may take as many clock cycles as needed to complete its write operation without affecting bus performance. Additionally, the PCI bus specification requires all target devices to support several configuration registers. Those registers are used by the system software for automatic system configuration.

For master/target applications, Altera also has a PCI master/target megacore of its own design that can overlay onto the FLEX 10K FPGA family. It consumes about 850 of the Lcells in a FLEX 10K30RC240-3 array. That's less than half of the array, and would leave plenty of room for custom logic to complete the system. The initial version of the core will be compliant with the PCI specification, rev. 2.1, delivering 33-MHz operation.

The master implementation offers many more options than the target version. To start with, the master interface includes features such as memory read/write, bus parking, a fully-integrated DMA engine, a configurable interrupt source, a 64-byte FIFO buffer, zero-wait-state PCI read (107 Mbytes/s) and zero-wait-state PCI write (102 Mbytes/s), a full set of configuration registers, parity generation and checking, and a PCI target interface. Through options in the design-tool software, blocks and registers can be deleted to simplify the interface and reduce the number of logic cells the interface requires.

The integrated DMA engine in the core handles a maximum burst access of 16 data cycles and includes an address register, transfer word counter, and control and status registers. The configurable interrupt source provides signals for DMA terminal count, master abort, target abort, and back-end interrupt. Support also is included in the core for a Type Zero configuration header of 256 bytes.

A second PCI bus master megacell, the EC210, is available through the AMPP program from Eureka Technology. It will support the PCI specification, rev. 2.1, and has an X86-style back-end bus interface. Accesses through the bus master can be initiated by the back-bus device to reach the PCI memory or I/O spaces. For instance, a video coprocessor or DMA controller could reside on the back bus and initiate a data transfer to the PCI bus. In the other direction, a transfer over the PCI bus can perform a read or write on the back bus to program the control registers of the back-bus DMA block or read the status from the video coprocessor.

The recently released OrCA 2CxxA series of RAM-based FGPAs from Lucent also is supported by several PCI megafunctions in VHDL

For prototyping and low-volume production needs, programmable logic chips provide designers with the ideal building blocks to build PCI interfaces.

form licensed from Logic Innovations—designers can select from a target only or a master/target block. In terms of gate count, the target consumes about 6000 equivalent gates, while the master/target block consumes about 12,000 gates.

Although the target megablock can fit into the OR2Cxx, 2TxxA, or 2CxxA families, the more complex master/target block can only overlay on the high-density OR2CxxA family or the just-released OR3C family of FPGAs. The 2CxxA family includes chips that pack from 3500 to about 40,000 usable gates and from 160 to 480 I/O pads. The new 3Cxxx/3Txxx family packs from 19-k to 320 kgates and from 224 to 608 user I/O pads *(ELECTRONIC DESIGN, Feb. 3, p. 48)*.

The target block is basically a pass-through design, with buffering external to the block, keeping the logic simple and easy to implement. The master/target, though, includes a 16-word-deep bidirectional buffer in the interface and employs dual-port synchronous memory to achieve the 33-MHz data-transfer rate over the PCI interface *(Fig. 2)*. The buffer depth may be the most common feature that designers modify. Once a master starts transferring data, it must have data to send or the system must add wait states for the data to catch up. Increasing the buffer depth could avoid the system slow downs.

The megafunction design kits provide the functional description in either VHDL or Verlog HDL form, making the functionality easy to modify. But once the cells are modified, the system performance may change, versus the guaranteed performance of the unmodified cell. The software used by Lucent in the OrCA foundry for circuit design and simulation of functions in the FPGAs is timing-driven, so that information on timing needs is carried along to the automatic placement-and-routing tools. Therefore, if the circuit design passes the foundry software, it should meet all timing specifications.

To achieve even better timing margins, FPGA architects at Lucent are seriously considering the inclusion of a hardware-PCI megafunction preembedded in the FPGA, just like the way blocks of RAM are now prediffused into some of the latest FPGAs. Plans at Lucent call for the megafunction to appear in the company's 3C family of system arrays by the end of this year. Such FPGAs from other vendors will probably start to surface toward the end of this year as well. The challenge faced by the FPGA suppliers, though, is to determine the base level of functionality to embed in the chip.

A hard macro in the silicon will give designers a higher-performance implementation that might be able to meet the timing needs of the next-generation PCI interface, which designers expect will run at 66 MHz. Such a high bus speed is not possible with today's crop of FPGAs, if the megafunction is configured as part of the programmable logic. The internal propagation delays would not let such a block meet the PCI specification timing requirements.

PCI building blocks also are available on the Xilinx RAM-based FPGA family. The blocks can overlay onto FPGAs such as the XC4000, 5000, and 6000. The first offering will be a master/target megafunction in the LogiCore family that provides a 100% com-

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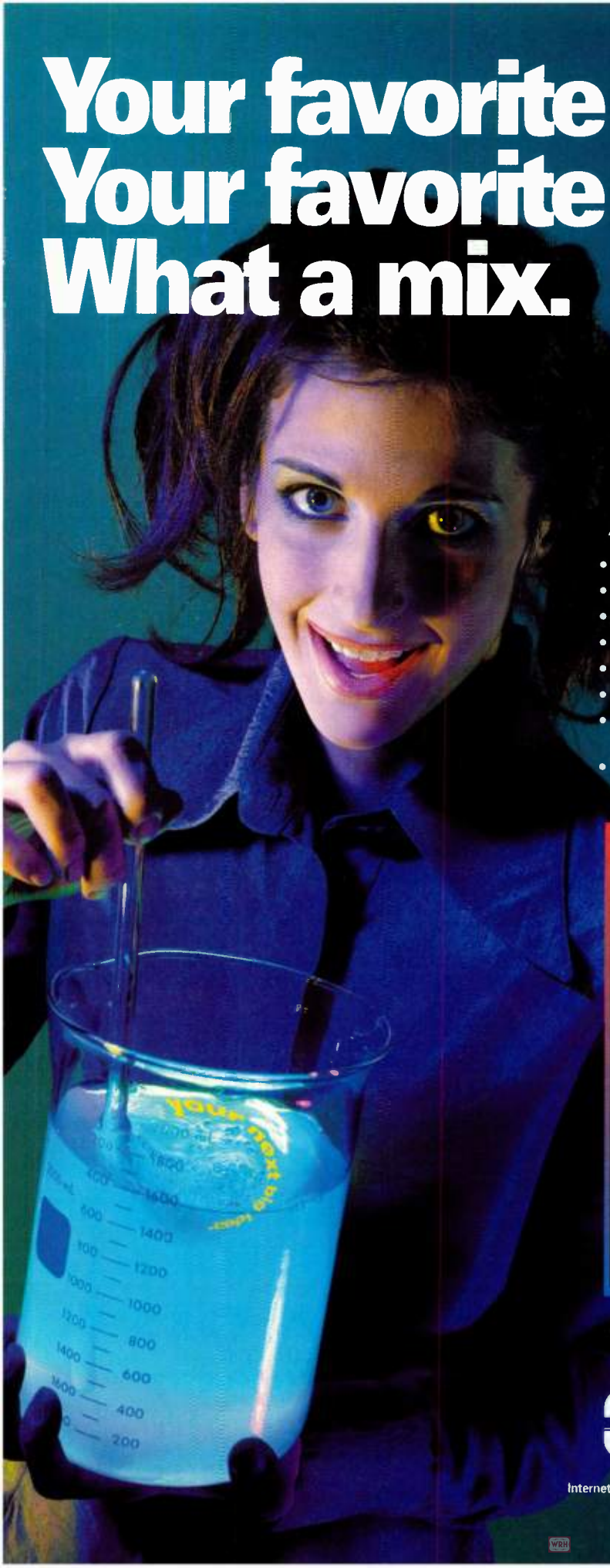

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DG412	Quad SPST	DG212 Upgrade
DG413	Quad SPST	DG211/DG212
DG441	Quad SPST	D201A, HI-0201
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supplier, however some implementations don't offer 100% compliance with the PCI specification. Since the megafunction provides a fairly minimal version of the PCI interface, there are few functions that designers delete or modify to optimize performance.

In contrast, the master/target interface is much more complex with many aspects that can be modified to suit cost and performance requirements. For example, the Master/Target megafunction typically incorporates FIFO buffers, a DMA engine, and a full set of configuration registers. Designers can reduce the number of configuration registers, increase or decrease the depth of the FIFO buffers, drop the use of the DMA engine, and select other features to enable or disable.

One target megafunction developed by Eureka Technology is available through the Altera Megafunction Partner Program (AMPP) alliance set up by Altera for its FLEX 8000 FPGA family. The block is fully compliant with the PCI specification (rev. 2.1) and requires about 366 logic cells on a FLEX 8000 chip. The block has three user-bus options to support peripheral devices with different data-transfer characteristics. And for each option, the block provides the byte assembly and disassembly functions to match the peripheral-bus data width with the user-bus data width. The three options include:

- A synchronous user bus which is normally used in 486-based PC systems. All transfers are fully synchronized with the system clock, and wait states can be inserted by a peripheral device any time during data transfer.
- A user bus which interfaces directly with the internal FIFO buffers. Data transfers typically require zero-wait-state operation, unless a FIFO full or empty signal is detected.
- A user bus with ISA-like functionality. In this mode, data transfers are not required to be synchronized to the system clock, and buses narrower than 32 bits are allowed.

Included in the megafunction block is a 32-bit write buffer that helps improve the speed of write operations on

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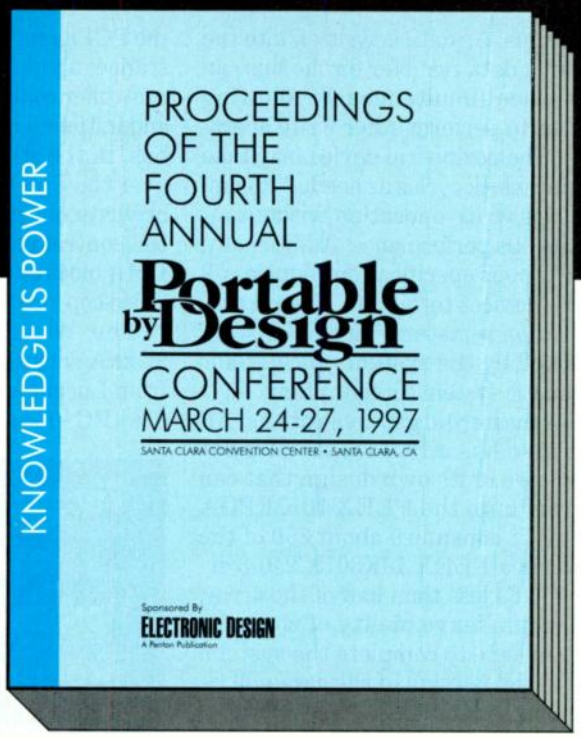

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a user bus. As data is written into the buffer, a data transfer on the bus can take place simultaneously, allowing the bus to perform other write operations. The peripheral device may take as many clock cycles as needed to complete its write operation without affecting bus performance. Additionally, the PCI bus specification requires all target devices to support several configuration registers. Those registers are used by the system software for automatic system configuration.

For master/target applications, Altera also has a PCI master/target megacore of its own design that can overlay onto the FLEX 10K FPGA family. It consumes about 850 of the Lcells in a FLEX 10K30RC240-3 array. That's less than half of the array, and would leave plenty of room for custom logic to complete the system. The initial version of the core will be compliant with the PCI specification, rev. 2.1, delivering 33-MHz operation.

The master implementation offers many more options than the target version. To start with, the master interface includes features such as memory read/write, bus parking, a fully-integrated DMA engine, a configurable interrupt source, a 64-byte FIFO buffer, zero-wait-state PCI read (107 Mbytes/s) and zero-wait-state PCI write (102 Mbytes/s), a full set of configuration registers, parity generation and checking, and a PCI target interface. Through options in the design-tool software, blocks and registers can be deleted to simplify the interface and reduce the number of logic cells the interface requires.

The integrated DMA engine in the core handles a maximum burst access of 16 data cycles and includes an address register, transfer word counter, and control and status registers. The configurable interrupt source provides signals for DMA terminal count, master abort, target abort, and back-end interrupt. Support also is included in the core for a Type Zero configuration header of 256 bytes.

A second PCI bus master megacell, the EC210, is available through the AMPP program from Eureka Technology. It will support the PCI specification, rev. 2.1, and has an X86-style back-end bus interface. Accesses through the bus master can be initiated by the back-bus device to reach the PCI memory or I/O spaces. For instance, a video coprocessor or DMA controller could reside on the back bus and initiate a data transfer to the PCI bus. In the other direction, a transfer over the PCI bus can perform a read or write on the back bus to program the control registers of the back-bus DMA block or read the status from the video coprocessor.

The recently released OrCA 2CxxA series of RAM-based FGPAs from Lucent also is supported by several PCI megafunctions in VHDL form licensed from Logic Innovations—designers can select from a target only or a master/target block. In terms of gate count, the target consumes about 6000 equivalent gates, while the master/target block consumes about 12,000 gates.

For prototyping and low-volume production needs, programmable logic chips provide designers with the ideal building blocks to build PCI interfaces.

Although the target megablock can fit into the OR2Cxx, 2TxxA, or 2CxxA families, the more complex master/target block can only overlay on the high-density OR2CxxA family or the just-released OR3C family of FPGAs. The 2CxxA family includes chips that pack from 3500 to about 40,000 usable gates and from 160 to 480 I/O pads. The new 3Cxxx/3Txxx family packs from 19-k to 320 kgates and from 224 to 608 user I/O pads *(ELECTRONIC DESIGN, Feb. 3, p. 48)*.

The target block is basically a pass-through design, with buffering external to the block, keeping the logic simple and easy to implement. The master/target, though, includes a 16-word-deep bidirectional buffer in the interface and employs dual-port synchronous memory to achieve the 33-MHz data-transfer rate over the PCI interface *(Fig. 2)*. The buffer depth may be the most common feature that designers modify. Once a master starts transferring data, it must have data to send or the system must add wait states for the data to catch up. Increasing the buffer depth could avoid the system slow downs.

The megafunction design kits provide the functional description in either VHDL or Verlog HDL form, making the functionality easy to modify. But once the cells are modified, the system performance may change, versus the guaranteed performance of the unmodified cell. The software used by Lucent in the OrCA foundry for circuit design and simulation of functions in the FPGAs is timing-driven, so that information on timing needs is carried along to the automatic placement-and-routing tools. Therefore, if the circuit design passes the foundry software, it should meet all timing specifications.

To achieve even better timing margins, FPGA architects at Lucent are seriously considering the inclusion of a hardware-PCI megafunction preembedded in the FPGA, just like the way blocks of RAM are now prediffused into some of the latest FPGAs. Plans at Lucent call for the megafunction to appear in the company's 3C family of system arrays by the end of this year. Such FPGAs from other vendors will probably start to surface toward the end of this year as well. The challenge faced by the FPGA suppliers, though, is to determine the base level of functionality to embed in the chip.

A hard macro in the silicon will give designers a higher-performance implementation that might be able to meet the timing needs of the next-generation PCI interface, which designers expect will run at 66 MHz. Such a high bus speed is not possible with today's crop of FPGAs, if the megafunction is configured as part of the programmable logic. The internal propagation delays would not let such a block meet the PCI specification timing requirements.

PCI building blocks also are available on the Xilinx RAM-based FPGA family. The blocks can overlay onto FPGAs such as the XC4000, 5000, and 6000. The first offering will be a master/target megafunction in the LogiCore family that provides a 100% com-

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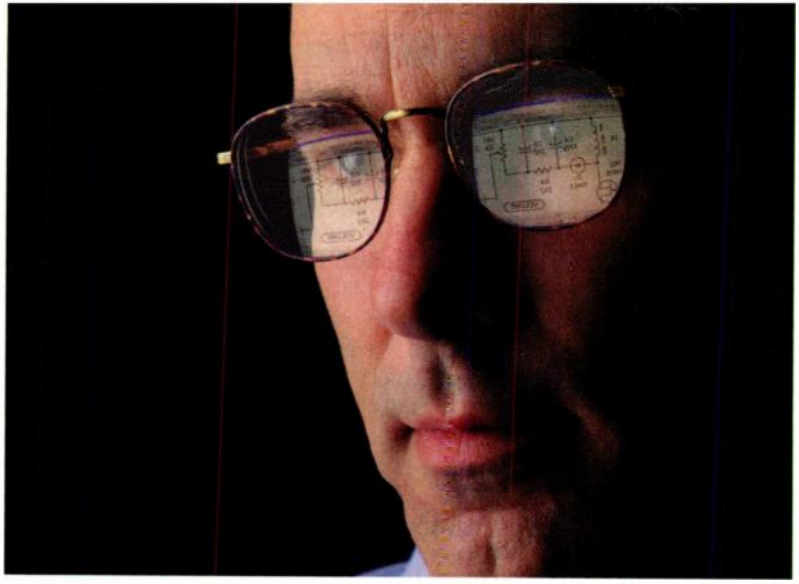

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pliant PCI interface block. It will be able to operate at 33 MHz and perform high-speed burst transfers thanks to the use of synchronous FIFO buffers.

Although the flash-memory-based FPGAs offered by the GateField division of Zycad have the capacity to hold PCI megafunctions, the performance of the older GF100K and GF200F families was such that the arrays could not deliver adequate performance to provide PCI-compliant interfaces. The latest family, the GF250F series, pack arrays with up to 150 kgates, with twice the performance of the GF200F series. That higher performance will still not let the arrays deliver full-PCI compliance, but the arrays can be used for functional prototyping or applications that don't need the maximum speed or full compliance.

In the antifuse-based FPGA arena, both Actel and QuickLogic offer PCI options for their respective FPGA families. To support PCI, Actel designers have prequalified their ACT 3 FPGA family to ensure that the on-chip performance and I/O buffers can handle the speed and drive requirements of the PCI megablocks. The A1460B and 14100BP FPGAs provide about 6000 and 10,000 usable gates, respectively, and up to 1153 flip-flops for internal logic. Plans call for Actel to eventually support PCI interfaces on the 3200SX family as well. Some of the same CorePCI functions also can be implemented on the older ACT 2 family of FPGAs, however those implementations won't be fully PCI compliant. In the new ES FPGA system array family, the company is considering a prediffused PCI implementation in the base array so that they will eventually be able to support the forthcoming 66-MHz version of PCI.

The CorePCI megafunctions, available in VHDL or Verilog HDL formats provide a suite of compliant modules that can be customized and integrated with the rest of the system logic. Claiming one of the broadest varieties of PCI blocks, Actel offers three target variations (one with memory and I/O, one with memory only, and one with a DMA master), two master versions (master only and master with target), and a PCI-to-PCI bridge. Gate counts for the CorePCI megablocks range from about 400 logic modules (occupying about 47% of an A1460BP FPGA), to 1250 logic modules for a master with two targets (occupying about 91% of an A141000BP FPGA). The master-plus-target combination core does not deliver zero-wait-state performance. Additional IP providers that offer PCI functions include both Technical Data Freeway and Toucan Technology.

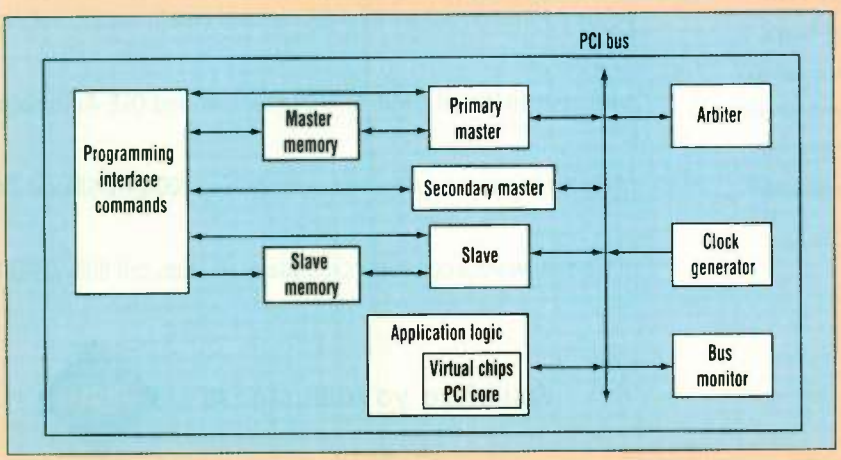
The models can be synthesized into logic-using tools from Synopsys Inc. (Mountainview, Calif.), Synplicity Inc. (Mountainview, Calif.), and Exemplar Logic (Alameda, Calif.), and support the timing-driven layout through Actel's DirectTime design tool. Separate models are available for targets, masters, and bus-to-bus bridges. However, unlike most of the cores available for other FPGA suppliers, the

Checking Out The Design In A Test Environment

Once the PCI interface has been defined, the next challenge is to ensure that it meets all the functional and timing requirements. To that end, Virtual Chips, a division of Phoenix Technologies, offers a PCI-bus test environment in either Verilog or VHDL. The verification environment comes configured as a dual-master, single-slave system. It includes test functions such as simulation models for master and slave (target) devices on the PCI bus, a bus arbiter to control bus access, and a bus monitor to detect and report PCI protocol violations. The test environment also has a full suite of compliance scenarios, as defined by the PCI rev. 2.1 specification *(see the figure)*.

The master and slave models each include a PCI bus interface and a command/data memory, and are controlled by high-level programming interface commands. The memory allows for multiple PCI transactions, including large burst transfers to be loaded and compared with results. All transactions are logged in the status register for easy access. Furthermore, the user can specify the severity level and simulation action for each type of protocol violation.

During PCI operation, the bus monitor checks for over 35 different protocol violations. Also, the design under test can be linked to the test environment by instantiating the design description (behavioral or gate-level) at the top level. The compliance software suite can then be run, and/or custom tests can be created using the programming interface commands. More than 100 commands are available in the programming interface. They allow the designer to initiate many different types of PCI cycles—burst, read-compare, read-modify-write, etc. Commands can initiate normal bus activity, or can be used to introduce errors such as parity or protocol violations to test the system response.



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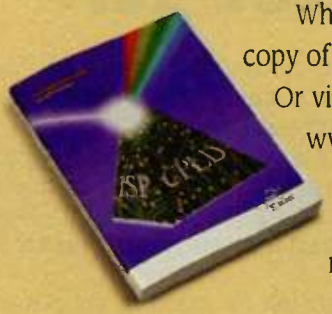

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CorePCI megafunctions do not include internal FIFOs as part of the core. They must be implemented directly in the register spaces. The cores also support PCI handshake signals, and one- or zero-wait-state operating modes.

Delayed transactions are not supported in the current cores and a special decode operation would be needed to provide that support. Caches are not supported, and the blocks do not support interrupts. Code modifications can be done, to support one or four interrupts. Included as part of the CorePCI design kit are the HDL models, a test bench to verify system performance, and the Designer Series FPGA development system.

Offering a target and a master/target implemention in their macro library, QuickLogic has been able to tune the design to achieve full-speed operation and full-compliance with the PCI specification. As with some of the other PCI implementations, designers at the company estimate that the master/target interface requires between 6000 and 7000 gates, while the target-only interface needs about 2000 gates. The designs are available as part of the company's PCI design kit, version 2.0. A PCI application kit produced on a CD-ROM provides application notes, VHDL/Verilog HDL source code, and an HDL simulation suite.

Designs can easily be modified to accommodate system requirements, since the HDL source code is available for the cores. Features such as the FIFO space, the number of configuration registers, the DMA control, and the burst-mode transfer capability, can all be modified, deleted, or massaged to the designer's needs. From what designers at QuickLogic have found, the burst-mode transfers are the hardest operation to meet all PCI timing constraints due to the setup time for the internal state machine. In that area for the current family of FPGAs, they do recommend adding one wait state per transfer.

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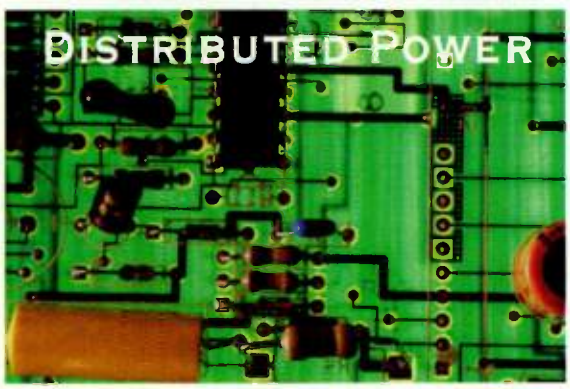

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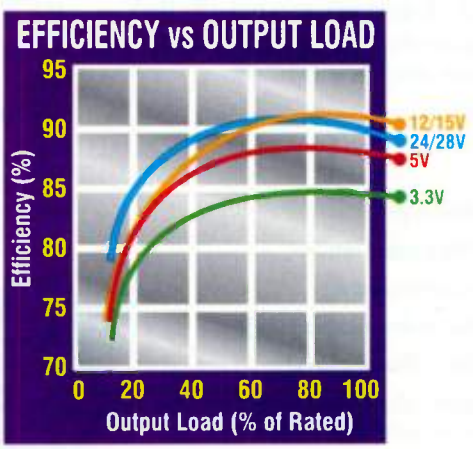

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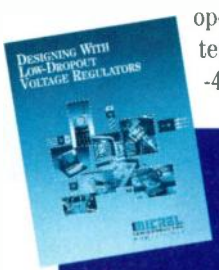

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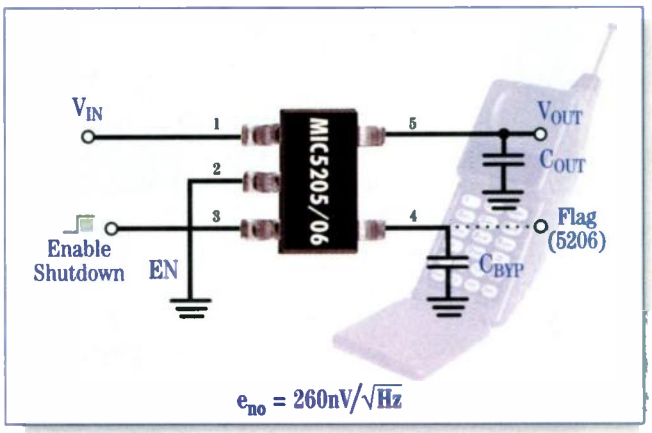
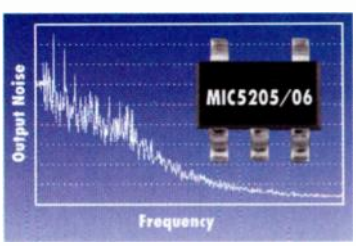


(C_{BYP}) is inserted into the voltage divider that sets the loop gain necessary to achieve a specific output voltage. Although gain is a necessary part of the feedback that makes a regulator work, it also "amplifies" noise. The capacitor reduces the loop gain at high frequencies to reduce high-frequency noise.



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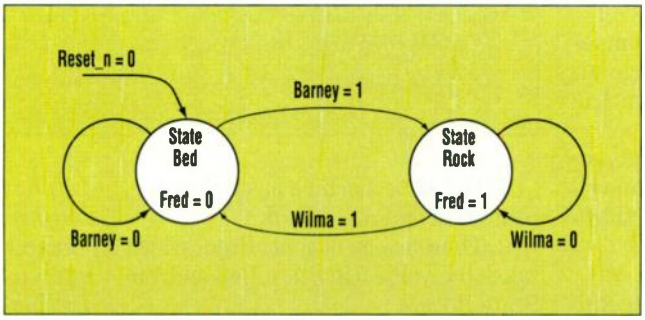
The Ten Commandments Of Excellent Design: VHDL Code Examples

Learn The Ins And Outs Of Writing VHDL Code For Synchronous Digital Designs.

PETER CHAMBERS, VLSI Technology Inc., 8375 South River Pkwy., Tempe, AZ 85284; (602) 752-6395; e-mail: peter.chambers@vlsi.com.

This article is the second of a two-part series that will give you some pointers for designing synchronous circuits that work the first time. Take note of the ten commandments that should *always* be followed! Part one of the series discussed the commandments in detail (ELECTRONIC DESIGN, *April 1, p. 33*). This article will help you learn about writing VHDL through the use of simple code examples.



This illustration shows the state diagram for the Flintstones state machine.

Those Ten Commandments:

Just in case you forgot, here are the Ten Commandments of Excellent Design:

1. All state machine outputs shall *always* be registered.
2. Thou shalt use registers, never latches.
3. Thy state machine inputs, including resets, shall be synchronous.
4. Beware fast paths lest they bite thine ankles.
5. Minimize skew of thine clocks.
6. Cross clock domains with the greatest of caution. Synchronize thy signals!
7. Have no dead states in thy state machines.
8. Have no logic with unbroken asynchronous feedback, lest the fleas of myriad Test Engineers infest thee.
9. All decode logic must be crafted carefully—eschew asynchronicity.
10. Trust not thy simulator—it may beguile thee when thy design is junk.

How to Write Ten-Commandment Code: Conforming to the Ten Commandments isn't difficult. In this section, you'll see how to write VHDL (yours truly doesn't do Verilog, but the translation is easy) that complies with the rules. Robust design and first-silicon success are the goals!

The philosophy behind Ten-Commandment code is that synthesizers aren't to be trusted. Most of the code you will see in this article is close to the structural level; some more overtly than others.

Most of the code is self-explanatory. It's assumed that the reader is familiar with VHDL. Signal names also are obvious to anyone "skilled in the art."

How to Create a Flip-Flop: One of the basic primitives that we need at our disposal when creating robust synchronous designs is the D-type flip-flop *(see Listing 1)*. The flip-flop in Listing 1 has the following properties:

- An asynchronous active-low clear input sets the Q output to zero.
- It is triggered on the rising edge of the clock.

How to Create a Latch: While the Ten Commandments specifically forbid the use of latches, there are those heretics who still insist on using them *(see Listing 2)*.

The code to instantiate a transparent latch is shown in Listing 2. This

LISTING 1

```
--VHDL Code for a D-Type Flip-Flop with an Asynchronous Clear

D_Type_F_Flop: process(Reset_n, Clock_In)
begin
   if (Reset_n = '0') then
      Q_Output <= '0' after 1 ns;
   elsif (Clock_In'event and Clock_In = '1') then
      Q_Output <= D_Input after 1 ns;
   end if;
end process D_Type_Flip_Flop;
```

LISTING 2

```
-- VHDL Code for a Transparent Latch

Latch_Data: process(Latch_Open, D_Input)
begin
   if (Latch_Open = '1') then
      Latched_Data <= D_Input;
--If Latch_Open = 0, then Latched_Data keeps its old value,
-- i.e. the latch is closed.
   end if;
end process Latch_Data;
```

latch has the following properties:

•A latch control that opens the latch when high (the latch is transparent).

How to Create a Metastable-Hardened Flip-Flop: The use of a metastable-hardened flip flop is nothing more than the direct instantiation of a suitable library element. In this case, the element is a "dfntns" flip-flop *(see Listing 3)*. The component declaration in Listing 3 is pure structural VHDL. Your library name is likely to be different from VLSI's "dfntns," but the declaration will be similar.

After creating the flip-flop component, you can then use it in your circuit *(see Listing 4)*. This flip-flop has the following properties:

•A maximum clock-to-out time under worst-case setup-and-hold time violations. This time is available in the library element specifications.

The Care and Feeding of Toggle Signals.—Receiving a Toggle Signal: Part one of the Ten Commandments article suggested that a method for exchanging single-point information across clock domains is by the use of toggle signals. Here, it's assumed that the toggle event should generate an active-high pulse to pass to a state machine. Every toggle—rising edge and falling edge—must create the pulse. In addition, the pulse must be synchronized correctly to the receiver's clock *(see Listing 5)*.

When synthesizing the code in Listing 5, remember to use the "fix hold" option so a fast path doesn't occur between the two flip-flops in this circuit.

Generating a Toggle Signal: Recall that a toggle signal is generated by simply inverting a level to pass the information. The code required to do this is trivial *(see Listing 6)*. The suffix "_T" is used to denote a toggle signal.

The Beginner's Guide to State Machines: The creation of state machines is a mixture of art and science. A well-crafted state machine will possess a sense of elegance, and it will be appealing, both functionally and visually.

This article presents a very simple example as an illustration of state machine design *(see the figure)*.

The Flintstones state machine operates as follows:

LISTING 3

```
--VHDL Code for a Nice Metastable-Hardened Flip-Flop

component dfntns
  Port (
    CP  : In  std_logic;
    D   : In  std_logic;
    Q   : Out std_logic
  );
end component;
```

LISTING 4

```
-- VHDL Code to Instantiate the Metastable-Hardened Flip-Flop

Metastable_Hardened_Flip_Flop_Please: dfntns port map (
  D  =>  D_Input,
  CP =>  Clock_In,
  Q  =>  Q_Output
);
```

1. The state machine has two states, State Bed and State Rock.

2. There is one output, Fred, which takes the value 0 in State Bed and 1 in State Rock.

3. A reset, caused by a low level on Reset_n, puts the state machine into State Bed.

4. The state machine waits in State Bed while Barney is low, and enters State Rock when Barney goes high.

5. The state machine then waits in State Rock while Wilma is low, and returns to State Bed when Wilma goes high.

Implementing the Flintstones State Machine: An example implementation of the Flintstones State Machine is shown written in VHDL code *(see Listing 7)*.

Notes on the State Machine Implementation: For the most part, the Flintstones state machine's operation should be clear. A few points are worth noting, however:

1. The reset signal (Sync_Reset_n) is synchronized with Clock_In before being sent to the state machine.

2. Barney and Wilma also must be

LISTING 5

```
--VHDL Code to Create a Pulse from an Asynchronous Toggle Signal

--First, use a metastable-hardened flip-flop to synchronize the toggle input

Metastable_Hardened_Flip_Flop_Please: dfntns port map (
  D  =>  Handshake_T,
  CP =>  Clock_In,
  Q  =>  Sync_Handshake_T
);

--Now pass the synchronized toggle through another flip-flop

Toggle_Reg_Proc: process(Clock_In)
begin
  if (Clock_In'event and Clock_In = '1') then
    Reg_Handshake_T <= Sync_Handshake_T after 1 ns;
  end if;
end process Toggle_Reg_Proc;

--Finally XOR the two synchronized signals to create a pulse

Toggle_Pulse <= Reg_Handshake_T xor Sync_Handshake_T;
```

LISTING 6

```
--VHDL Code to Create a Toggle Signal (embedded in a clocked process)

Handshake_T <= not (Handshake_T) after 1 ns;
```

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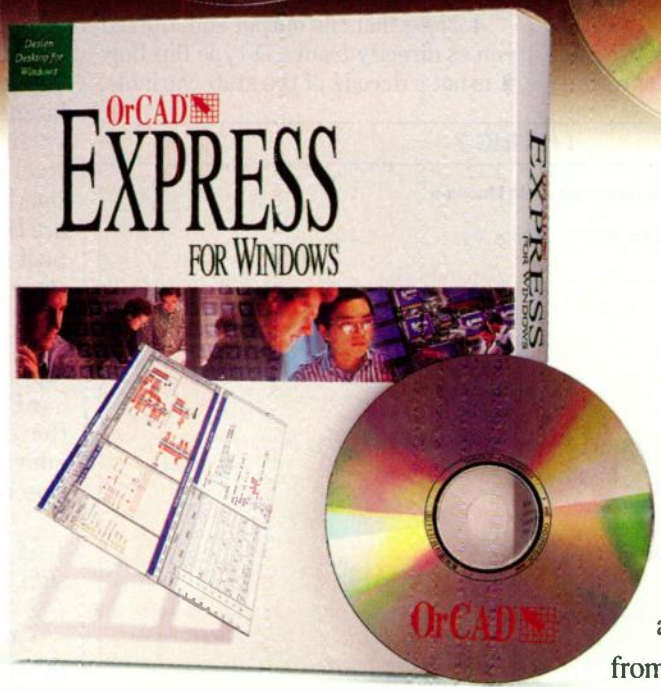

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synchronous to Clock_In. At the very least, there must be an assurance that the state machine's state and output registers' setup and hold times are not violated.

3. This design assigns a default value to each output and to the state variable before entering the case statement. This ensures that only those signals that are not taking default (usually inactive) values need be listed in the case statement. This is optional; it's entirely reasonable to list every signal under each transition term, including inactive signals.

4. Note that the output signal Fred comes directly from a D-type flip-flop: it is not a decode of the state variable. This ensures Fred's cleanliness (so to speak).

5. The "when others" in the case statement handles the possibility that the state machine might end up in a dead state.

Latches, Schmatches: In the first article, the second commandment, Thou shalt use registers, never latches, has been somewhat controversial (to say the least). Dyed-in-the-wool latch users have been squealing that latches are wondrous things, and are the solution to good designs, compact chips, and peace on earth. Two clear advantages of latches are:

- Considerably smaller than D-type flip-flops.
- Provide anticipation of the data (for example, the decode of a latched address can begin before the latch is closed).

If you do insist on a latch-based design, watch out for the following:

- A glitch-free enable—remember that glitches on the enable can corrupt the latch's data. If you are synthesizing the code to create the enable, consider seriously the direct instantiation of the gate that drives the enable to the latch. Don't trust optimized equations!
- Data input hold time—ensure that the data is held for long enough as you close the latch. If your latch enable is derived from a clock, the latch will lag the clock, requiring the latch's D inputs to be held valid after the clock edge.

Conclusions: The code examples in this document should only be considered as examples. There are many ways to write excellent VHDL code; this code is a place to start. If you have a neat snippet of VHDL to add to the list, please contact the author!

Peter Chambers is an engineering fellow at VLSI Technology's Computer Products Div. He holds a BSc degree from the University of Exeter, England, and an MS from Arizona State University, Tempe.

LISTING 7

```
--VHDL Code to Implement the Flintstones State Machine

Flintstones_SM_Proc: process(Sync_Reset_n, Clock_In)

-- Enumerate state types:

type Flintstones_Statetype is (
      Bed, Rock
   );

--define the state variable:

variable   Flint_State:   Flintstones_Statetype;

-- Here's the state machine:

begin
-- Define the asynchronously set reset states...
   if (Sync_Reset_n = '0') then
      Fred          <= '0' after 1 ns;
      Flint_State    := Bed

--Default conditions for each output, in this case identical to the reset state:

   elsif (Clock_In'event and Clock_In = '1') then
      Fred          <= '0' after 1 ns;
      Flint_State    := Bed

--Here are the state transitions:

      case Flint_State is
        when Bed =>

--Transition from Bed to Rock:

            if (Barney = '1') then
              Fred          <= '1' after 1 ns;
              Flint_State    := Rock;

--Holding term in Bed:

            else
              Flint_State    := Bed;
            end if;

        when Rock =>
--Transition from Rock to Bed:

            if (Wilma = '1') then
              Fred          <= '0' after 1 ns;
              Flint_State    := Bed;

--Holding term in Rock:

            else
              Fred          <= '1' after 1 ns;
              Flint_State    := Rock;
            end if;

--Default term for dead states:

        when others =>
          Flint_State    := Bed;
      end case;
   end if;
end process Flintstones_SM_Proc;
```

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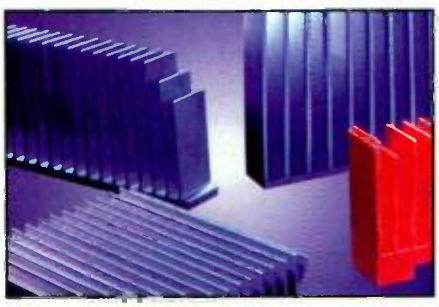

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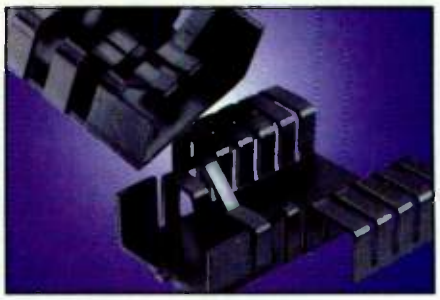

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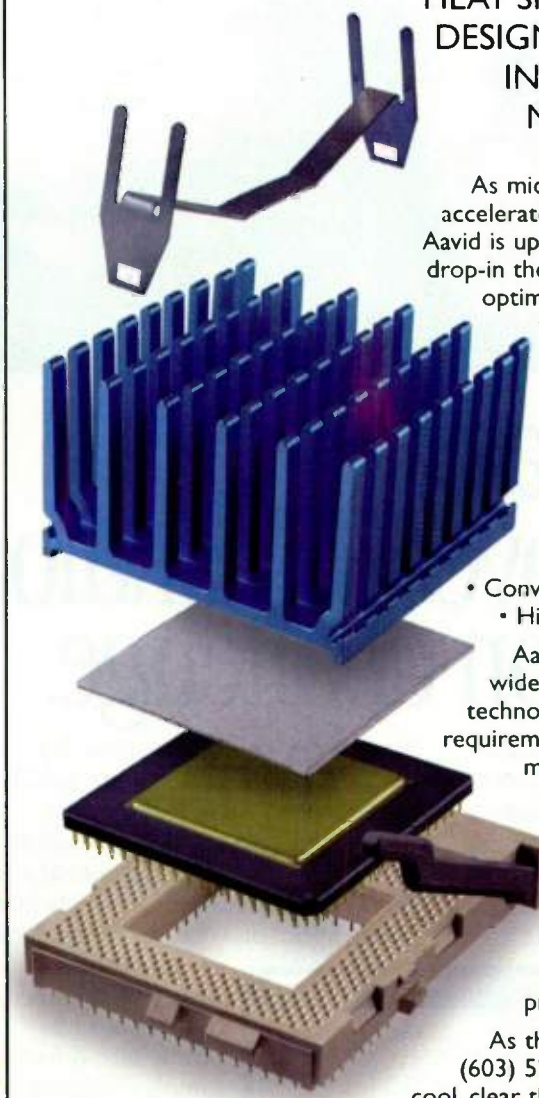

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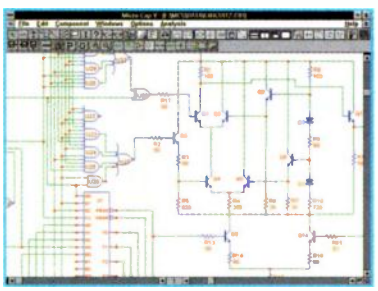

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Programmable Chips Provide Flexible Signal Routing, Predictable Timing

By Combining Programmable Interconnections And Flexible I/O Cells, Signal Routing With Short Delays Has Never Been Easier.

Dave Bursky

The well-defined architecture of complex-programmable logic devices often limits their flexibility when it comes to rearranging signal paths through the chip or altering the system logic. However, a new family of in-system programmable (isp) devices developed by Lattice Semiconductor exploits digital crosspoint technology to deliver high I/O line density, short pin-to-pin delays, and a highly-programmable system solution. The ispGDX (generic digital crosspoint) family of programmable logic components provides designers with a flexible solution for board-level signal routing, data path implementation and switch-replacement applications.

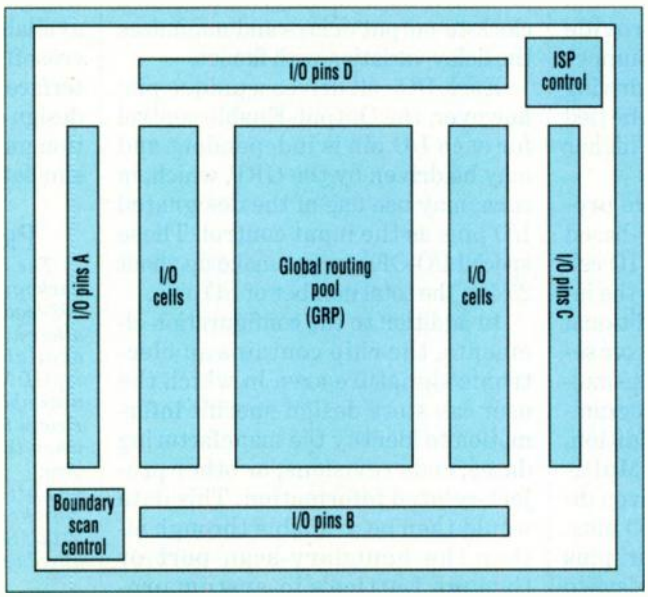
Furthermore, the in-system programmability of the ispGDX architecture allows system logic to be reconfigured on-the-fly, thereby permitting one set of logic components to do the work of many. The ability to reuse the hardware can considerably lower system component count, lower system cost, and even improve system performance by allowing the system logic to be optimized for each application.

The logic architecture of the ispGDX chips is optimized for fast pin-to-pin signal propagation—just 5 ns pin-in to pin-out and 4.5 ns clock-to-output delays including all programmable interconnect delays. Such short delays will allow the logic circuits to tackle applications typically handled by C-grade FCT logic circuits. The chip also can handle the critical timing requirements and bus drive needs of PCI-bus systems, driving 24-mA loads with low ground bounce and minimal signal skew. The outputs also have programmable switching speed to better match edge rates to the system.

The EEPROM Connection

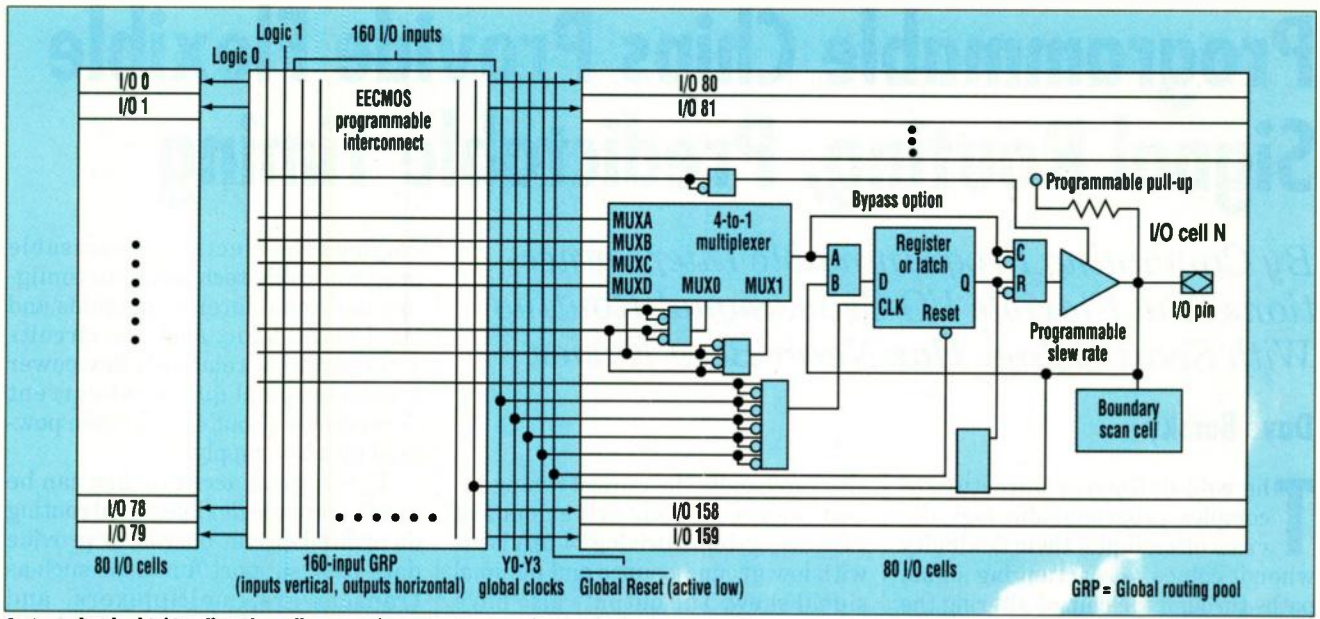
Initially, there will be four members in the ispGDX family—the ispGDX64, 80, 120, and 160—that all have the same basic architecture, but have 64, 80, 120 and 160 I/O pins, respectively. A second series currently in development will extend the I/O pin counts to 192 to 256 lines. The new architecture of the ispGDX includes no programmable logic arrays, but rather employs the electrically-erasable programmable technology to configure the signal interconnections and the I/O cell logic. And, the circuits will operate at relatively low power levels—typical quiescent current drain is only about 40 mA when powered by a 5-V supply.

This type of architecture can be used to provide flexible signal routing on printed-circuit boards, or provide data-path support functions such as transceivers, multiplexers, and latches—functions that provide direct support for today's high-performance 32- and 64-bit microprocessors. The ispGDX chips, with their high I/O-pin counts, can often eliminate many lower-density interface circuits, thus freeing up valuable board real-estate and simplifying the system. Yet another application, programmable switch replacement, is a common application for small EEPROMs, but with the ispGDX chips, the new chips can provide more flexible switch options.



1. Programmable I/O cells surround a Global Routing Pool (GRP) that is formed by a digital crosspoint switch in the ispGDX family of programmable logic devices from Lattice Semiconductor. The GRP allows interconnections to be made between any of the I/O pins and any one or multiple I/O cells.

Internally, the circuits consist of a series of programmable I/O cells that surround and are interconnected by a global routing pool (GRP). The I/O pins are grouped into four banks—A, B, C, and D—each of which is positioned on one edge of the chip *(Fig. 1)*. Two banks of programmable I/O cells are positioned on two opposite edges of the GRP, between the I/O pin buffers and the GRP. Each of the I/O cells consists of a 4:1 dynamic multiplexer, a D-type flip-flop that can serve as a register or latch, and a buffer with programmable slew rate and programmable pull-ups *(Fig. 2)*. Also included is a boundary-scan cell to support the chip's IEEE 1149.1-compliant (JTAG) boundary-scan test capability.



2. An individual I/O cell in the cell array of Fig. 1 consists of a 4:1 multiplexer, a D-type register or latch, a buffer with both programmable slew rate and programmable pull-ups, and IEEE JTAG-compliant self-test features.

Through in-system programming, connections between I/O pins and the devices's architectural features (latched or registered inputs or outputs, output-enable control, etc.) can be defined. Furthermore, there are no pin-to-pin routing constraints for 1-to-1 or 1-to-many signal routing—any I/O pin configured as an input can drive one or more I/O pins configured as outputs. All inputs include Schmitt-trigger buffers for noise immunity. Outputs also can be set to provide fixed high or low logic levels (jumper or DIP switch mode), or when driving high-current loads, outputs can be tied together in parallel to achieve higher drive capabilities.

The circuit connections are programmed using the EECMOS-based configuration elements. Each IO cell has four inputs that connect to the internal 4:1 multiplexer and additional lines that perform the multiplexer selection functions. Polarity for the multiplexer signal inputs also is programmable for each I/O cell. In addition, Output Enable, Clock, and Multiplexer-Select inputs can be driven directly from selected sets of I/O pins. Optional dedicated clock-input pins also keep the clock-to-output delays to a minimum.

The four data inputs to the multiplexer in the cell can access one quarter of the total I/Os; for example, in the ispGDX160, each data input can connect to any one of 40 I/O pins. Also in the I/O cell is a programmable flow-through latch or register that can be placed in the input or output path, or bypassed when combinatorial outputs are needed. The programmable-polarity clock available to the latch or register can be connected to any I/O in the I/O clock set (one-quarter of the total number of I/O cells), or to one of the dedicated clock input pins. Use of the dedicated clock inputs gives minimum clock-to-output delays and minimizes the delay variation with fanout.

Each I/O cell drives a unique pin; however, the Output-Enable control for each I/O pin is independent and may be driven by the GRP, which, in turn, may use one of the designated I/O pins as the input control. These special I/O-OE pin sets make up about 25% of the total number of I/O pins.

In addition to the configuration elements, the chip contains an electronic signature area in which the user can store design-specific information to identify the manufacturing dates, code revisions, or other project-related information. This data would then be available through either the boundary-scan port or through Lattice's in-system programming port. A security bit is also included in the ispGDX devices, which when set, will prevent any configuration information from being read out; the signature information, though, can be read out.

Designed for operation from a 5-V supply, the ispGDX circuits have a 3.3- or 5-V I/O operation thanks to separate power supply pins for the I/O lines and the internal logic. Therefore, the chip can operate in mixed-supply systems. And, like previous members of Lattice's isp families, the circuits can be fully programmed and reconfigured using the serial isp port. Design tools to support the family are available for free and run under Microsoft's Windows graphical user interface. The tools provide HDL-based design entry and compilation. Simulation models are available for popular simulators.

Price And Availability

The ispGDX chips will be available in packages ranging from 84-lead PLCCs to 208-lead PQFPs. Space-saving TQFP and other high-density packages also will be available. In 1000-unit quantities, the ispGDX sells for $18 apiece and will be available in sample quantities this month. Prices for the other chips will be released when the chips start sampling later this year.

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UPDATE ON ACTIVE TERMINATION LOGIC

Logic Protocol Takes Advantage Of Active Memory Bus Terminator To Speed Data Transfers

Series Stub Terminated Logic (SSTL), defined by JEDEC, is a direct descendent of TTL and Low Voltage-TTL (LV-TTL). SSTL is popular with designers because it allows memory buses to run at clock rates above 100 MHz. To operate at the higher speed, SSTL employs a narrow separation between the voltage levels that distinguish a logic high (above 1.5 V) from a logic low (below 1.1 V). This 500-mV separation lets the bus run faster because its signals don't swing as far as an LV-TTL circuit, for example, which has a 1.2-V separation (from 0.8 to 2.0 V). Although the narrower voltage separation provides a greater speed, it is much more susceptible to noisefrom voltage reflections and echoes.

The noise problem can be handled using active termination, which is supplied by a chip such as the ML6550 from Micro Linear Corp., San Jose, Calif. While the chip boasts a 10% increase in the memory bus' speed over passively terminated buses, a greater benefit comes from the part's reduced power consumption (a reduction of up to 100 times). The ML6550 IC chip can terminate up to 40 bus lines, while eliminating the need for the 40 resistors that connect the bus lines to ground in a passively terminated bus (*see the figure*).

The ML6550 acts as a "super charger" to boost speed and lower power consumption. With the speed improvements, users will see faster video with better resolution and greater overall performance. The chip reduces the power consumption by delivering current on an "as needed" basis. For example, a typical 40-line bus using the chip only consumes 25 mW (0.625 mW per line), while a passively terminated bus would consume 2.5 W (62.5 mW per line).

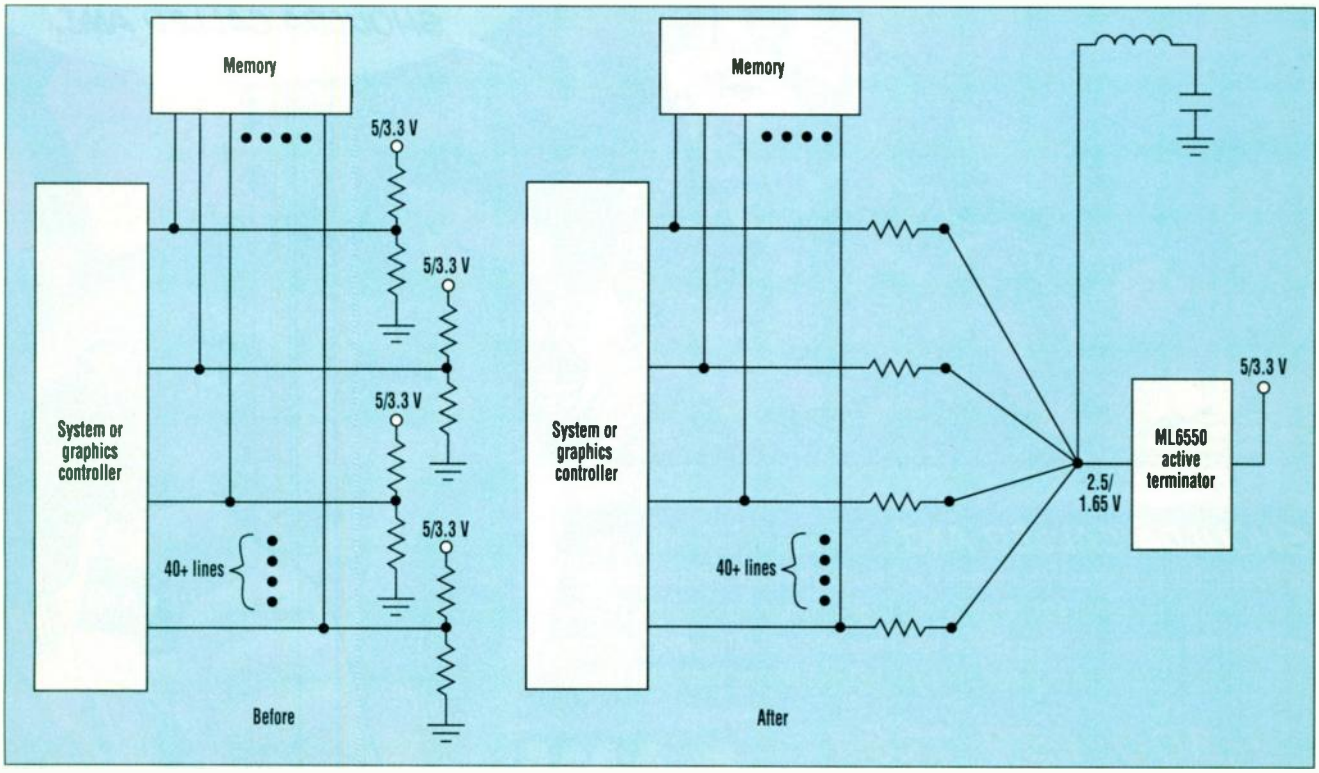
The ML6550 terminates buses connecting microprocessors to their memory and terminates buses connecting graphics controllers to their video memory. The active device speeds these connections by pumping out the precise amount of current needed to quiet noise on the bus lines. In contrast, passive termination employs a "brute force" method that pumps a steady stream of current from a fixed resistor pair regardless of need, thereby dissipating excessive power.

Passive termination gained popularity in the design of high-speed buses clocking data at rates above 60 MHz. At these speeds, passive components squelch the noise of reflecting bus signals or signals going from one end of the bus to the other. If this noise was not suppressed, the echoes might register as false data or commands. With bus clocks exceeding 100 MHz, active termination should become the preferred choice.

The chip produces a 2.5-V output for a 5-V bus, or a 1.65-V or a 3.3-V bus. It can sink or source currents up to 600 mA. The ML6550 can actively terminate a bus using any memory interface including TTL, LV-TTL, and SSTL.

For further information, contact Micro Linear at (408) 433-5200, or on the Internet at: http://www.microlinear.com.

RICHARD NASS



Passive termination using "power-hungry" resistors (left) can now be eliminated using active-termination techniques (right) made possible by the ML6550 active terminator IC from Micro Linear. A single chip can terminate up to 40 bus lines.

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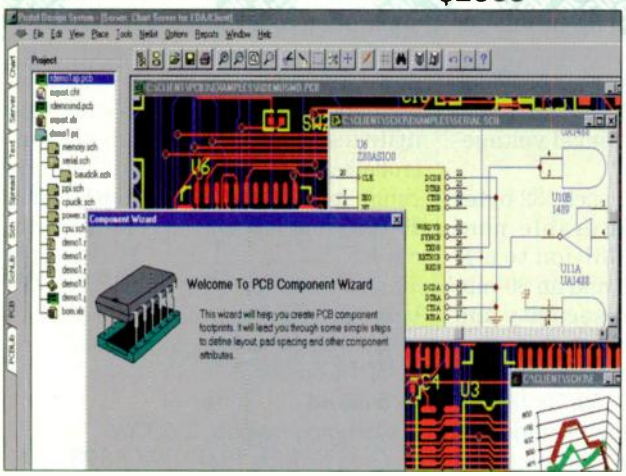

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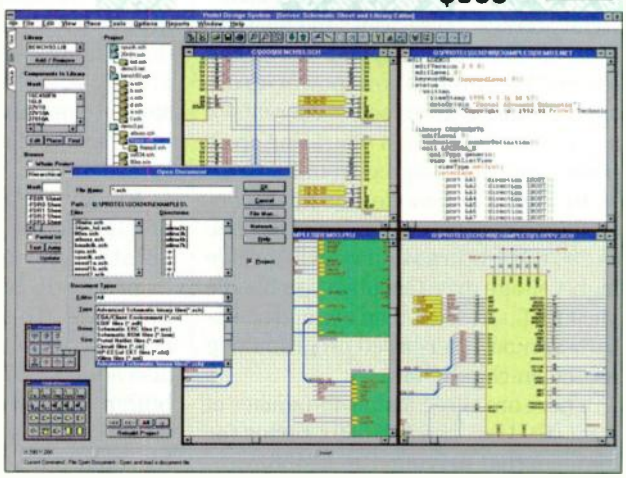

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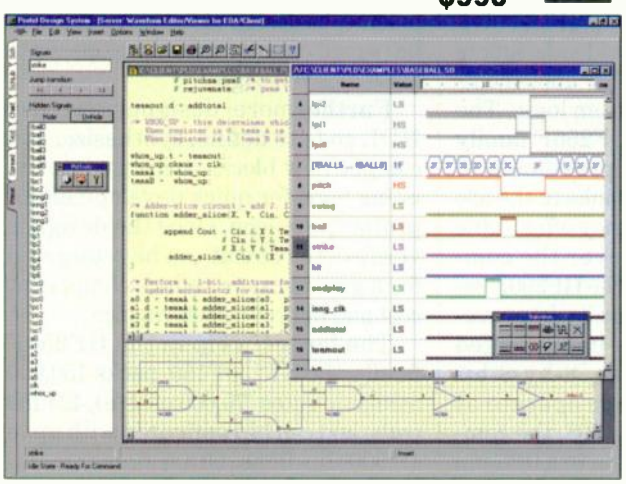

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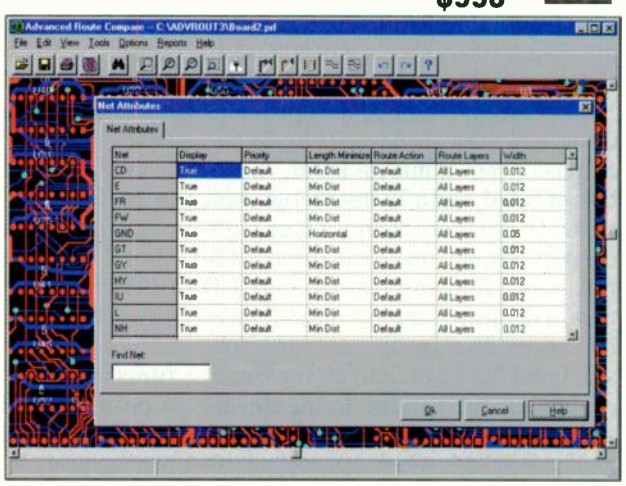

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READER SERVICE 165

PRODUCT FEATURE

Speedy Low-Power 4-Bit MCUs Contain An LCD Drive And EEPROM

Based on a RISC architecture that executes one instruction every two clock cycles, the EM 66XX family of 4-bit microcontrollers includes members that pack LCD controllers, EEPROM storage, pulse-width modulators, high-current drivers, and more. The MCUs, targeted at low-power-drain applications, feature active currents of as little as 5 µA when operating from power supplies ranging from 1.2 to 3.6 V. In their sleep mode, the microcontrollers have current drains of as little as 200 nA. Future versions will include high-voltage drive capability to handle vacuum fluorescent displays and short-turn-around, laser-based programming for the on-chip ROMs.

There are three main sub-families of 4-bit MCUs—the EM660x series for high-current driving; the EM662x series for LCD driving; and the EM664x series with EEPROM and a large serial write buffer for remote control and security applications. The EM660x devices operate over a 1.2-to-1.7-V range and consume just 3 µA in their active mode and 300 nA on standby. The EM662x MCUs can operate from 1.2-to-3.6-V supplies and consume about 5-µA in their active mode and 500 nA during standby. Lastly, the 664x series runs from 1.8-to-3.6-V supplies, drawing 45-µA when active and 500 nA in the sleep mode.

Specifically, the EM6604 provides designers with 1536 words by 16 bits of mask-programmable ROM, 72 nibbles of RAM, and a 72-instruction 4-bit CPU. I/O support includes four high-current outputs (each can drive a 4.5-mA load), four input pins, four I/O pins, a dedicated buzzer output, an 8-bit timer with prescaler, a supply-voltage level detector, and an interrupt controller that handles four external and two internal sources.

The EM6620, which can control a 3-digit-by-8-segment or 4-by-8 LCD display, incorporates a 1024-word-by-16-bit ROM, 64 nibbles of RAM, a metal-mask programmable segment allocation architecture, a 4-bit input port, a 4-bit bidirectional port, 10-bit counter with pulse-width modulator, a millisecond counter with three-digit BCD outputs, and an interrupt controller with five external and seven internal request sources. The EM6622 offers a similar feature set, but can drive a 3- or 4-character 32-segment display and a 4-kword-by-16-bit ROM or OTP EPROM. In addition to the 64-nibble RAM, a second 64-nibble indexed addressable RAM supports the display. A melody generator provides seven tones, an 8-bit three-wire serial interface, and an eight-level voltage-level detector.

Finally, the EM6640 packs 32 bytes of EEPROM user-alterable nonvolatile storage in addition to a 1-kword-by-16-bit ROM, and an 80-nibble RAM. To support security and remote control applications, designers also added a 256-bit-long serial-write buffer that can clock at 150, 75, 18.8, or 9.4 kHz. Other functions include a 4-bit input port, two 4-bit bidirectional ports (one of which includes a pulse-width modulator), a 10-bit universal counter with 19-stage prescaler, an interrupt controller with four external and five internal sources, and a supply-voltage level detector (two levels, software selectable).

Software tools for developing the application code include a full environment running under Microsoft Windows. Included is a software simulator, debugger, compiler, and additional utilities. Samples of the microcontrollers are available immediately and range in price from less than $0.90 in 100,000-unit lots for the versions without EEPROM, and about $1.10 each in similar quantities for the EEPROM-based MCUs.

EM Microelectronic-Marin SA
601 Campus Dr.
Suite B4
Arlington Heights, IL 60004
Greg Krasick, (847) 394-8893
e-mail: emgreg1@aol.com
CIRCLE 463

DAVE BURSKY

Flash-Based FPGA Family Shoehorns In Up To 150,000 Gates

An enhanced family of field-programmable gate arrays (FPGAs), developed by the GateField division of Zycad Corp., provides designers with up to 150,000 gates for implementing large blocks of system logic. The flash-memory-based GF250F family provides a density improvement of more than 50%. And, thanks to the use of 0.6-µm design rules, they offer a 20% speed improvement over the company's previous family, the GF200F series. The speed and density improvements allow internally implemented functions, such as an 8-by-8-bit pipelined multiplier, to operate at speeds of 125 MHz. In 1998, the company expects to transition to a 0.35-µm process that will create densities of up to 400,000 gates, and double the operating frequency of the GF250F series.

The entire ProASIC product family makes it possible for designers to reuse blocks of intellectual property. That's because the higher gate count no longer requires logic be reduced to a bare minimum, or be reconfigured specifically for the FPGAs before compiling the design. The small granularity of the cells in the GF250F allows macrocells designed for gate arrays to be ported directly onto the chips without major redesign.

Furthermore, designers can use HDL code to define, synthesize, and compile new blocks to merge into existing logic for quick development of prototype silicon. Once the design is verified, the circuit can be retargeted for a gate array to reduce component cost and improve performance.

The largest chip in the GF250F family, the GF250F150, packs 150,000 available gates (70,000 usable), 424 I/O pads, and can be configured with up to 18,000 flip-flops. Other family members include the GF250F025, 250F050, and 250F100, which pack 25k, 50k, and 100k total gates, respectively. Those gate counts translate into usable counts of 12k, 22k, and 46k gates. The three chips also have respective I/O pad counts of 176, 248, and 360, and can implement 3k, 6k, and 12k flip-flops.

The large number of flip-flops can

(continued on page 136)

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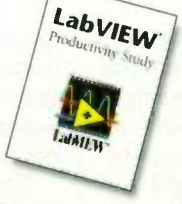

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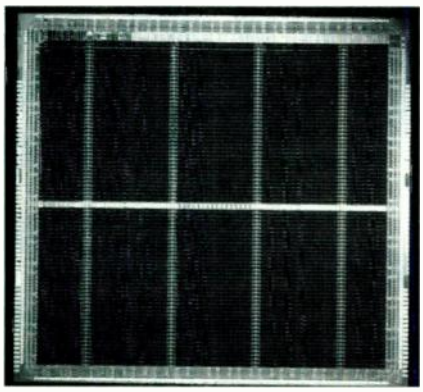
READER SERVICE 152

(continued from page 134)
be implemented in registers, register files, small blocks of RAM, etc.—all of which can form complex blocks such as digital signal processors or functions with distributed memory. Power consumption, of course, depends on the



logic functions implemented, but the base logic consumes about 8 μW/gate/MHz. Based on EEPROM configuration elements, the nonvolatile but reprogrammable chips fit smoothly into the ASIC design flow since the same basic design approaches can be used right up until the time the design must be compiled.

In the design library, the GateField FPGAs include simple gates, complex gates, and storage elements—functions ranging from simple NAND gates to Exclusive NORs, to registers and latches. The I/O cells include input, output ,and bidirectional options, while input buffers handle TTL or CMOS input signal levels. Output buffers have programmable pull-up resistors and programmable slew-rate control, and can drive loads of 6 or 12 mA. Buffer timing specifications can meet PCIbus system needs by allowing designers to create PCI-compliant circuits.

As part of the design tool suite, the company includes a memory compiler that allows users to quickly define register files and FIFO buffer building blocks. Dual-port (1 read, 1 write) asynchronous operation is possible for either memory option. The compiler delivers a Verilog net list and an ASICmaster constraint file used by the GateField design tools.

Tool support includes synthesis software, VHDL simulation, schematic capture, gate simulation, and timing analysis programs from many well-established tool vendors. These tools couple into ASICmaster, GateField's ASIC design-flow manager. The tool provides predictable silicon utilization, power, and timing while providing pin-constrained place and route.

Able to run on both Sun and HP platforms, the tool interfaces to suites from Mentor, Cadence, ViewLogic, and Synopsys. For device programming, the company sells the ASICmaker programming attachment that connects directly to the workstation.

Samples of both the GF250F050 and 250F100 are available immediately, with production quantities coming in June. The largest chip, the GF250F150 will be sampled in the third quarter. Pricing for the 50-kgate GF250F050 housed in a 208-lead MQUAD package is $222 apiece in lots of 100 units. In 1998, the same device will sell for less than $84 each in volumes of 5000 units. The ASICmaker with related software sells for $2000.

GateField Div. of Zycad Corp.
47100 Bayside Pkwy.
Fremont, CA 94538
Todd Scott, (510) 623-4400
Web: http://www.zycad.com
CIRCLE 464
DAVE BURSKY

Synchronous Dual-Port SRAMs Push Throughput Of Network Subsystems

Adding a second access port, address generators, and output registers to a family of synchronous static RAMs helps to achieve higher throughputs when transferring blocks of data in pipelined systems. These dual-port synchronous SRAMs, developed by Integrated Device Technology, promise to improve the performance of network subsystems such as hubs, routers, and switches, as well as other high-speed digital-signal-processing, data-buffering, and data-processing applications.

The dual-port pipelined architecture provides each memory with two address input ports, and two data ports (two 8-bit or two 16-bit ports), each with their own output registers. Each port can be controlled independently, and each contains its own burst address generator. This double address structure eliminates the need to externally generate new addresses for each clock cycle. A starting address is loaded into a port; then the internal counter automatically increments on each rising clock edge at the same time the data requested in the previous cycle is delivered to the output port (for writes, the operation is similar, except that data is presented to the input port at each clock cycle).

The IDT709xxx family consists of four 512-kbit and two 256-kbit memories that are available in dual 8-bit- or dual 16-bit-wide I/O configurations, each packing two independent address-input ports. Both memory den-

sities can deliver data at speeds as short as 12 ns (clock to data), with high-speed accesses simultaneously possible on both ports. Initial cycle times are 25 ns (40-MHz system clocks), but the company expects to offer faster versions later this year. DSP applications, data-buffering subsystems, and various multiprocessor system architectures can take advantage of the new memory chips' dual data-stream capability.

In addition to the pipelined operation on both ports, one of the ports can also be configured (via a control pin) as a flow-through port, bypassing the internal output register. This increases the clock-to-data time to 25 ns and the cycle time to 30 ns for the flow-through port. Dedicated chips that offer only flow-through operation on both ports also are available. These versions provide better performance in systems that need fast random-access to individual memory locations and quick transitions from write-to-read operations. The 512-kbit chips are available in 32-kword-by-16-bit (IDT709279 and 70927) and 64-kword-by-8-bit organizations (IDT709089

(continued on page 138)

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READER SERVICE 110

(continued from page 136)
and 70908); item numbers in parentheses indicate pipelined or flow-through versions, respectively. The 256-kbit chips are restricted to pipelined versions, but they do come in either a 16-kword by 16-bit or a 32-kword by 8-bit organization (IDT709269 and 709079, respectively). All chips will be available in 100-lead thin QFP packages, and will operate from a 5-V supply that consumes 190 mA when active and about 1 mA on standby.

Prices in 100-unit sample quantities start at $29.95 each for the 256-kbit IDT709079, and go up to $31.35 for the IDT709269; $38.35 for the 70908; 47.95 for the 709089; $39.95 for the 70927; and $49.75 for the 512-kbit 709279. Samples of the 32k-by-16 memory are immediately available; the remaining chips will be sampled next month.

Integrated Device Technology Inc.
2975 Stender Way
Santa Clara, CA 95054
Carl May, (408) 754-4623
CIRCLE 465
DAVE BURSKY

56-kbit/s Modem Chip Set Doubles Download Speed

A three-chip set, based on Texas Instrument's TMS320x2 digital signal processor, lets designers create 56-kbit/s modems that are compatible with the US Robotics (now part of 3Com Corp.) x2 high-speed modem implementation. Except for local memory and the telephone-line interface, the trio of chips provides all of the functions required to implement the modem—the signal processing, the codec, and the host-bus interface and modem control functions. Using standard phone lines to deliver 56-kbit/s data downloads and 40-kbit/s data downloads, modems based on the chip set can basically double the speed of data downloads versus standard 28.8-kbit/s modems. It sells for $75 per set in 10,000-unit quantities. DB

***Texas Instruments Inc.**, Semiconductor Group, SC-96062, Literature Response Center, P.O. Box 172228, Denver, CO 80217; (800) 477-8924; Web: http://www.ti.com.* **CIRCLE 466**

Low-Voltage MCUs Trim Power, Not Performance

The 68331 and 68332 microcontrollers, operating from a 3.3-V supply, trim their power consumptions by almost 50% versus their 5-V counterparts. The processors can run at 16.78 MHz and include all of the features of the 5-V versions, such as a 32-bit 68020 processor and 2 kbytes of RAM.

Available as well is a 2.7-V, 16-bit MCU, dubbed the 68HC16Z1. The chip can operate over a 2.7-to-3.6-V range and runs at a clock speed of 16.78 MHz. It contains 2 kbytes of SRAM, as well as the queued serial and system-integration modules. The 3-V 68331 and 332 come in 144-lead TQFPs and sell for $11.45 and $13.20 apiece, respectively, in 10,000-unit quantities. The 2.7-V 68HC16Z1 also comes in a 144-lead TQFP and sells for $10.20 each in 10,000-unit quantities. DB

***Motorola Inc.**, Advanced Microcontroller Div., P.O. Box 13026, Austin, TX 78711; Bill Pfaff, (512) 328-2268.*
CIRCLE 467

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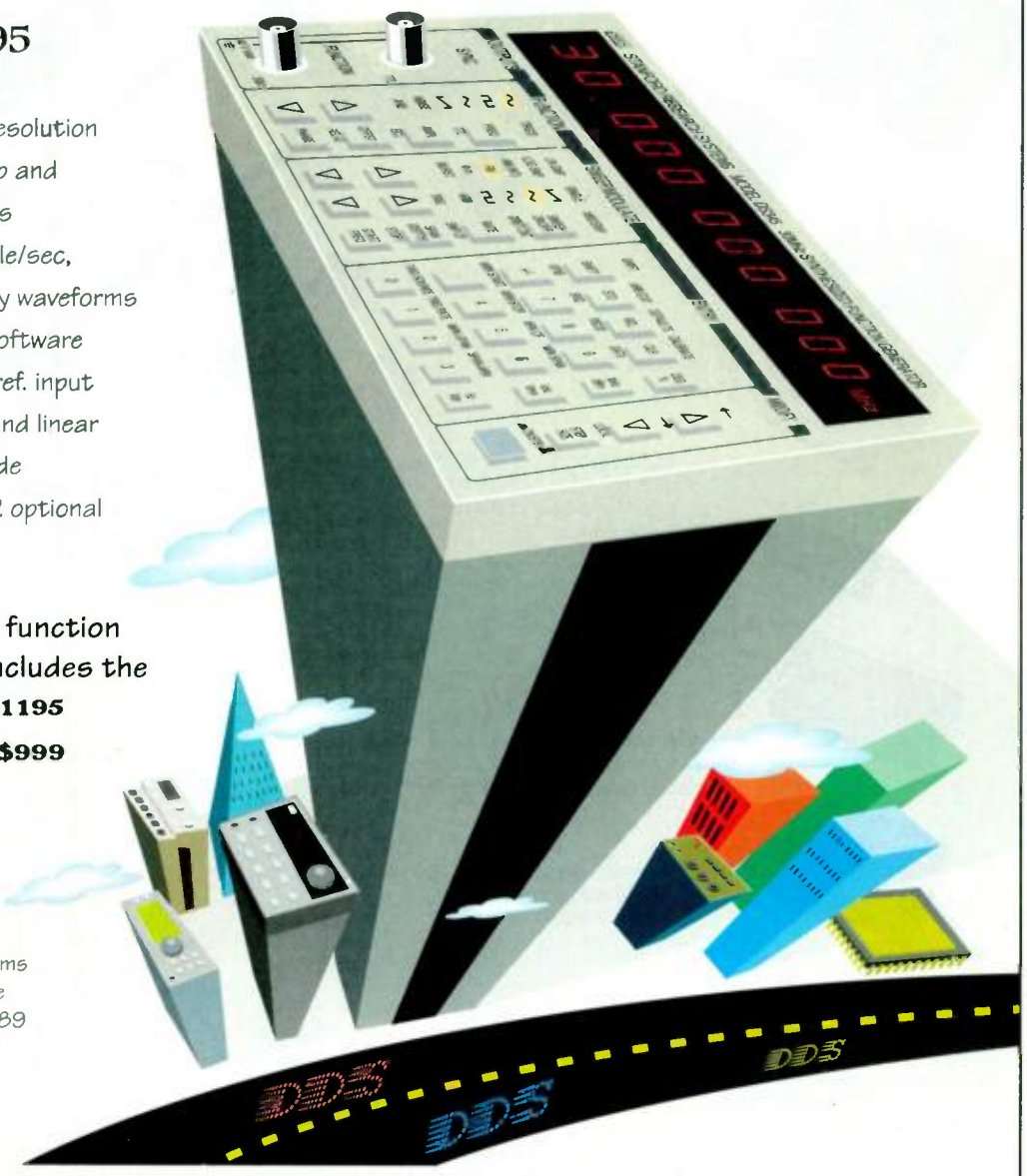

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READER SERVICE 176

Merging Television With PCs—Which Display Is In The Picture?

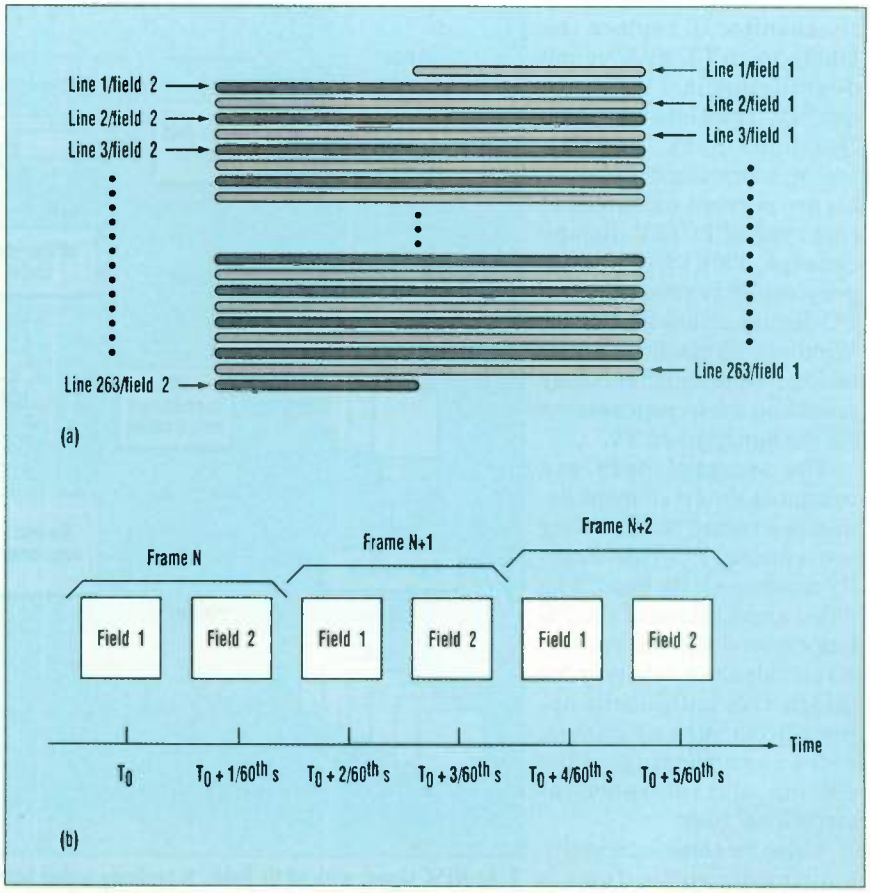
The Battle For The Home-viewing Audience Continues As PC Monitors Compete With The Sharpness And Quality Of TV Screens.

ERIC RAYEL, Brooktree Division, Rockwell Semiconductor Systems, 9868 Scranton Rd., San Diego, CA. 92121; (512) 349-3538, e-mail: erayel@brooktree.com

As consumer and computer product technologies converge, many theories have been discussed about how PCs and TVs should mesh, but the optimal blend has yet to be found. The emerging market for interactive, digital home-entertainment devices spawned a number of early products and product concepts, ranging from web-browsing set-top boxes to PC-based, high-end home theater systems. But these efforts have been met by the consumer with limited enthusiasm. Among the unknowns: What does the customer want? What products can deliver on those expectations? How should those products be packaged? The challenge for PC/TV equipment manufacturers seems to be finding the right level of PC-style interactivity without compromising the look and feel of the family room TV.

Attempts to design a merged PC/TV are complicated by differences in the design of displays used by PCs and TVs. Computer monitors have been optimized for reading 10-point type and static images from a distance of 2 ft. Accordingly, the physical display size is small and uses a low-brightness, non-interlaced scan, with fast screen refresh to produce a crisp, high-definition image which is easy on the eyes at short viewing distances.

TV imagery, on the other hand, has been optimized within the constraints of the relatively archaic National TV Systems Committee (NTSC) system. Designed to generate a low-resolution, high-brightness image, TVs use an interlaced scan with low screen refresh, suitable for viewing moving images on a large display area at distances of 6 ft. or more. Ultimately, consumer PC/TV appliance manufacturers will choose between PC- or TV-style displays to best suit their particular product feature set. Each display type presents its own unique problem



1. Interlacing in the NTSC format is created by the first (odd) field starting with a half line (a) and the second (even) field ending with a half line. Because the two fields are laid down sequentially, there is a temporal offset (b) between them.

to the merged PC/TV device—a TV is a very poor substitute for a PC monitor as a computer-graphics display device; likewise, standard PC-display technology cannot measure up to the TV as a display device for family room video entertainment.

The TV attachment to the PC is not new, and various techniques for adapting computer graphics image content to the TV screen are well understood and have been used for some time. Still, the TV's text display capabilities are severely limited at best, even if supported with good-quality digital video flicker-filtering and careful attention to font selection. While TV output is valuable in PC-video entertainment and game applications, it will not allow the PC to be used as a personal productivity tool.

Given TV's inherent limitations as a character display, adapting TV picture content to the constraints of the PC monitor has gained the attention of home computer makers. Of particular interest are PC-graphics display technologies which allow the monitor to replace the family-room TV without any degradation in TV picture quality. The Gateway 2000 Destination PC and Microsoft's Broadcast PC models are current examples of this type of PC/TV display concept. This PC/TV category seeks to preserve the PC display utility for today's Windows 95 platform applications while simultaneously providing a true replacement for the family-room TV.

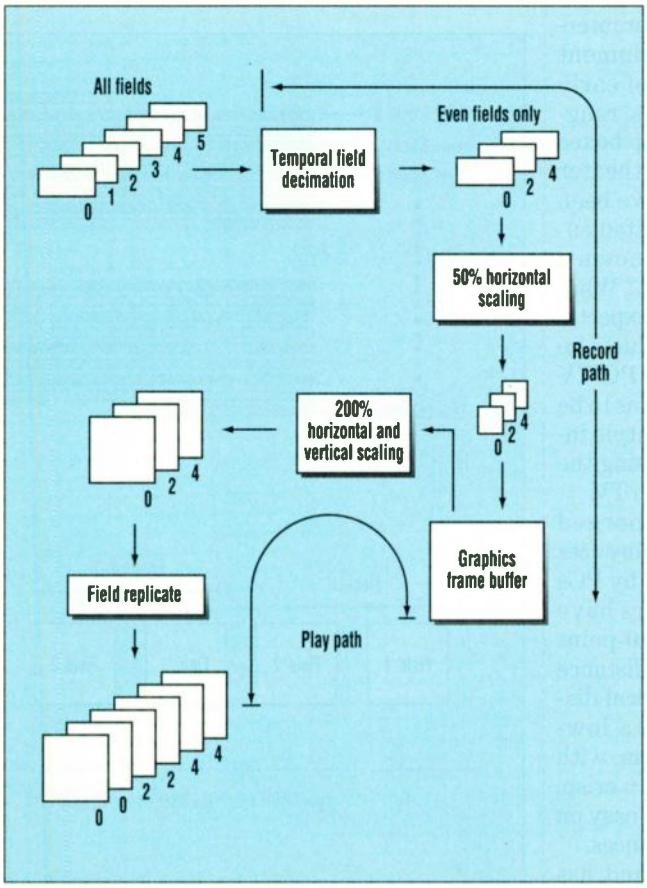
The concept of the PC as a consumer entertainment device is a recent one, turning conventional PC-Video quality wisdom on its head. The video architecture of the PC has evolved with an emphasis on video as a data type for interactive multimedia applications such as games, video conferencing, video editing, and reference/instructional tools.

Video for these interactive multimedia applications is characterized by non-interlaced sequences of very limited duration. These sequences have low native resolution and low frame rates. Compressed-video data formats such as MPEG-1, H.261, Indeo, and Cinepak are typical of this genre of video in which 15 field/s of 384 by 288 resolution (VHS quality) is about as good as one can expect. The graphics system architecture that evolved to support these limited video requirements focuses on the integration of color conversion, image resizing hardware, and off-screen video buffers to enable a low-quality on-screen video picture that doesn't require changes to display behavior. Again, the role of video has been limited to enhancing the PC visual interface for interactive leisure and productivity applications, a role in which graphics continues to be the predominant data type.

Raising The Bar

The emergence of the family room PC-product category dramatically raises the performance bar for PC-Video systems. The family room PC must manage consumer-entertainment video formats and display TV-style images gracefully to meet the consumer's high expectations for new, digital home-entertainment appliances. The nature of linear, consumer-entertainment video is fundamentally different from that of interactive multimedia: linear, digital-video content for consumer entertainment is created for display on a TV.

To produce high-fidelity pictures rivaling those of high-end TVs, PCs must incorporate digital-video processing technology which adapts the video stream to the characteristics of the PC monitor. This process must preserve the inherent fidelity of the video source while simulating the TV's scan techniques on a PC display. This process requires a combination of techniques to preserve the native resolution of a digital-video stream, while simultaneously handling the special deinterlacing and frame-rate conversion tasks necessary to produce high-fidelity, consumer-entertainment-grade digital-video images.



2. An NTSC signal, with all its fields, is typically scaled both vertically and horizontally prior to storage in a PC graphics-frame buffer. The information that is thrown away cannot be restored in playback, and further degradation is added.

The nature of NTSC TV display format creates enormous challenges. Video made for TV is comprised of a continuous sequence of pictures, or fields, at a constant rate of 59.94 Hz. With an image size of 640 by 240 pixels, each field contains only half of the full 480-line picture's vertical resolution. Each field scans only alternate lines of the TV display, with adjacent fields scanning 240 lines—each offset from the other on the screen by one half-line position. The first, or odd, field which scans the display starts with a half-line scan while the second, or even, field ends with a half-line *(Fig. 1a)*.

A full-frame of NTSC video actually contains 525 lines. Approximately 480 of those lines are used for the video picture (the active lines), while the remainder makes up the vertical-blanking interval. Accordingly, there are 262.5 lines in each field. This sequence of field pairs—scanning every other

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display line with a half-line off-set between fields—creates an interlaced display scan. Each field pair combines to form a full 640 by 480 TV picture frame. Complicating matters, each of the fields within a frame are separated temporally, representing two discrete instances in time 1/60th of a second apart *(Fig. 1b)*. So, to present a true TV-like picture, the PC must attempt to copy this display scanning technique as faithfully as possible.

One of the first examples of a video-display solution that addresses this challenge is TrueView technology from the Brooktree Division of Rockwell Semiconductor Systems. In developing TrueView technology for its video/graphics controller family, Brooktree saw three separate issues related to displaying TV-quality video on the PC.

First, the native resolution of the digital-video stream must be preserved from its origin—typically an MPEG-2, or composite video, decoder—through to the DACs of the graphics device. Second, that native video source must be converted from an interlaced format to a display format that is suitable for the PC's progressive-scan display mechanism, without introducing any visible image glitches. Finally, the PC screen display refresh rate must be locked to the field rate of the original video source to avoid display-rate conversion artifacts. Each of these areas presents its own particular challenges.

Preserving Native Resolution

Until now, the video display technology implemented in today's typical PC-Video graphics controller solutions has severely degraded the fidelity of broadcast quality video for TV *(Fig. 2)*. A CCIR601-resolution video source such as MPEG-2, or broadcast TV, is generally both horizontally and vertically downscaled by a factor of two before it can be stored in the graphics frame buffer (vertical downscaling is usually achieved by dropping alternate video fields). The displayed image resolution is subsequently restored to its original size through back-end upscaling. The result is an enormous degradation in image quality caused by the two stage scaling process used to manage the video image in local storage.

Once downscaling is applied to the video picture, visual image information is lost forever; it cannot be recovered. But, even worse, the back-end upscaling process will magnify existing image artifacts in the downscaled image, and also introduces some artifacts of its own. Half of the temporal information in the original video is discarded. The native video source has been converted from a 60 field/s (i.e. 30 frame/s) interlaced picture sequence to a 30 field and frame/s noninterlaced picture sequence. Removal of half the temporal information content creates an unnatural, stilted motion.

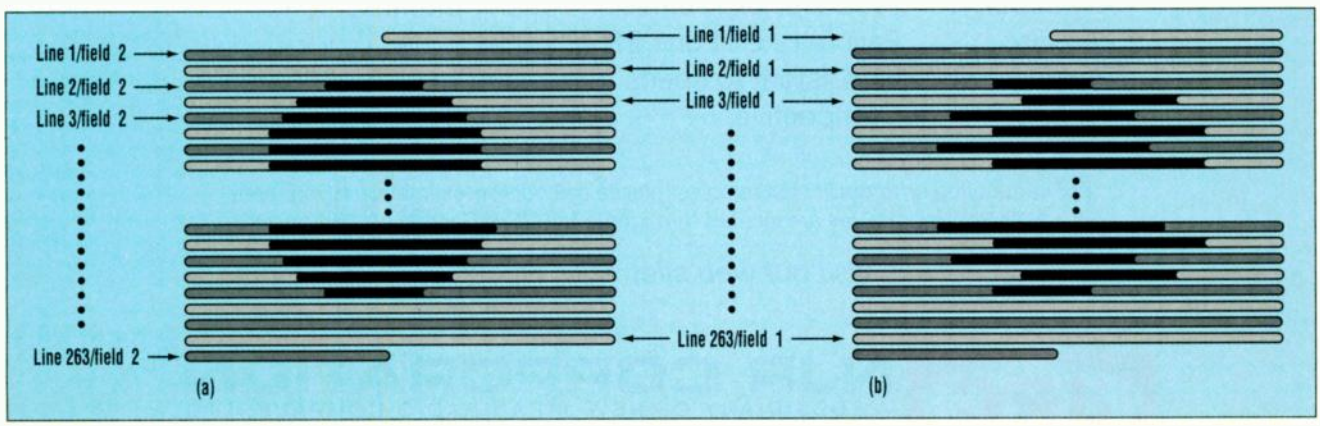
The visible problems with 30 frame/s noninterlaced video become particularly acute for film video sources which have been formatted for TV. A technique known as 3:2 pull-down is used as a rate converter in flying-spot telecines, to reformat movies recorded at 24 frame/s for NTSC TV transmission at 30 frame/s (60 field/s). Alternate individual film frames are transmitted for two and three NTSC fields, respectively, to fit within the standard 30 frame/s required by the NTSC standard. When the displayed picture rate is decimated down to 30 field/s from 60 field/s after 3:2 pull-down, the result is a sequence in which every fourth field is displayed twice in succession. These repeated fields generate even further problems in motion on the video.

To avoid these shortcomings and preserve digital-video fidelity all the way to the PC screen, video should be captured into the frame buffer at 60 field/s, with up to 720 YCrCb 4:2:2 formatted video pixels per line into the frame buffer, all without any intermediate decimation or scaling. This technique is critical for family room entertainment systems which include MPEG-2 decoder hardware for delivering pristine digital TV broadcast and DVD source pictures conforming to the CCIR601 video format standard.

Mimicking The TV Approach

Although capturing both fields of the video frame, at full horizontal resolution, into the graphics frame buffer can eliminate the image degradation caused by the dual scaling process, systems capturing 60 fields/s contend with the problem of deinterlacing the video without throwing away picture information.

The conventional, simplistic approach to the interlaced-to-noninterlaced conversion challenge is to capture both fields of a video frame in local memory and read out both fields simultaneously to the PC display. This deinterlacing technique ignores the



3. In a typical PC deinterlacing system, the two fields are stored in memory and then read out simultaneously to the display. With a static image (a) there is no problem, but because the second field was originally temporally offset, a moving image appears jagged (b) or "feathered."

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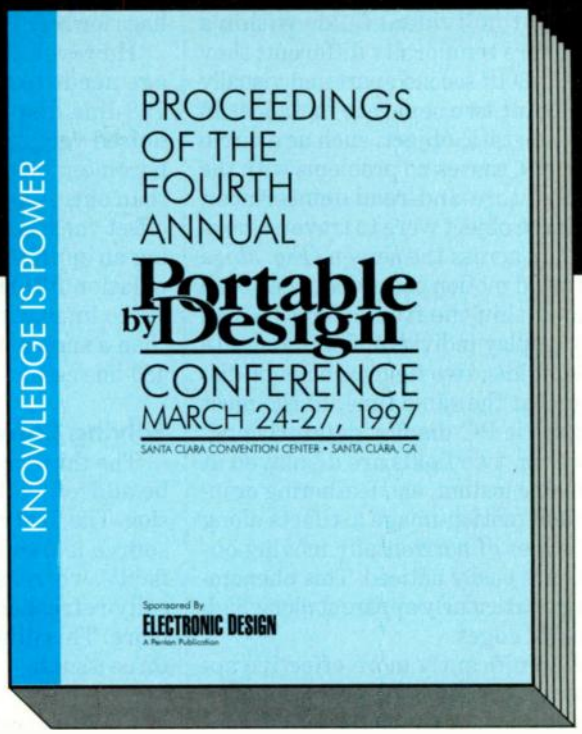

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fact that individual fields within a frame are temporally different; they occur 1/60th second apart and visually represent two separate instances in time. A static object, such as a circle *(Fig. 3a)*, causes no problems with the simple store-and-read deinterlacer, but if the object were to traverse horizontally across the screen *(Fig. 3b)*, a distorted motion occurs between each field within the frame. The TV can only display individual fields at a rate of 60 field/s; two fields are never displayed at the same time. In the most simplistic PC-display deinterlacing, however, two fields are displayed at the same instant, and feathering or interfield motion-image artifacts along the edges of horizontally moving objects are easily noticed. This phenomena is particularly apparent along high contrast edges.

A significantly more effective approach is to mimic the interlacing display action of a TV on the PC display. This technique is possible by displaying each field of a 60 field/s stream as a discrete image on the display, rather than combining every pair of fields to compose a video frame image as described previously. Each field is displayed on the screen on alternating scan lines, as on a TV. The empty, or blank, lines are generated by interpolating new video pixels from the adjacent, captured video lines immediately above and below the empty line. A full 480 lines of NTSC video are produced for each field update to the screen. By using a three-tap, eight-phase interpolation filter on the video/graphics controller, the system can then accurately create all of the empty video lines on the display.

The second element that the deinterlacing technology must address is a display position adjustment for even and odd fields relative to each other during successive PC-display updates. The screen display position of the even- and odd-field video lines must be vertically offset from each other to faithfully replicate the interlaced display action of a TV picture. This technique allows the video/graphics controller to compensate for the half-line offset between even and odd fields in CCIR601 interlaced video. A single PC display line is offset when the video is to be displayed at its native vertical resolution; e.g., 480-active lines for NTSC.

However, if the 480-line video image needs to be fitted into a 600- or 768-line display area, then the required vertical offset between fields becomes a noninteger value, greater than one. A noninteger, vertical line-offset value is achieved by implementing an appropriately weighted interpolation filtering between adjacent video lines within each field, rather than a simple averaging used for the 480-line case.

Solving Conversion Problems

The third major problem that must be addressed is frame-rate conversion. The field rate of the native video source is fixed at approximately 60 field/s, whereas PC displays are typically refreshed at a rate of 70 Hz or more. This difference in rates raises three issues:

1. When a single video buffer is used for both the capture and display of the video image, image tearing or shearing can occur. The damage is the result of the buffer being updated at a slower rate than the display refresh rate. An object in motion will often become sheared in the video sequence because the displayed image contains portions of two different frames separated in time by 1/30th second. Double buffering of the video can easily be implemented to overcome this problem, but there will still be some occasional stilted motion, caused by a periodic replication of a video frame or field. This occasional replication is necessary to convert from 60 to 70 image updates per second.

2. Ideally, the PC-screen refresh rate should match that of the original video source to truly replicate TV display behavior. Special digital display frame-locking techniques must be used to ensure that the screen-refresh rate precisely tracks the actual field rate of the original digital-video source. This technique guarantees that the display-update rate will never drift from the native video source rate. Even small mismatches in the input- and output-image update rates will cause regular, noticeable hiccups in the video picture motion. It is not an acceptable compromise for consumer-video entertainment devices.

3. The most effective frame-locking technique is adaptive, digital frame-locking, rather than an analog PLL-locking technique. The display-refresh rate must be controlled very tightly around the nominal 59.94 Hz rate for NTSC. Typical graphics-IC PLLs have an unacceptably large granularity in their timing increments, exacerbated further by the tolerance of the low-cost 14.318 MHz crystal used with these PLLs. Rather than constrain the entire graphics solution with tighter PLL and crystal tolerances, a digital-locking technique should be used to provide a more cost-effective and flexible solution.

Home-PC manufacturers face significant challenges as they prepare to do battle with consumer electronics manufacturers for a piece of the living room entertainment-equipment market. Chief among these challenges is turning the PC screen into a real TV display. Preserving the TV look and feel is critical for consumer acceptance of PC-based entertainment equipment. But now, in the age of mainstream direct-to-home digital video delivery, consumer expectations of video picture fidelity are sky high.

The PC enjoys a big advantage over digital-TV systems as the nature of family room entertainment becomes more of an interactive medium.. But until now, the PC has not been able to match the TV for the display of robust, crisp video pictures. That situation could change with the emergence of new and advanced PC-display techniques that more closely mimic the display techniques of the family-room TV. As these techniques are implemented in future machines, , the PC will be poised to mount a serious challenge for a share of the mainstream consumer entertainment electronics market.

Eric Rayel is a Sr. Product Marketing Manager in the Brooktree graphics chip business unit. He holds an MSEE from the University of California, Santa Barbara and an MBA from the University of San Diego.

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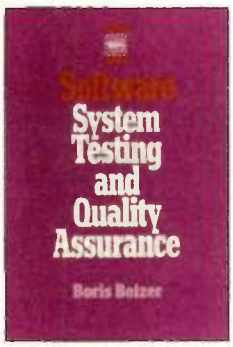

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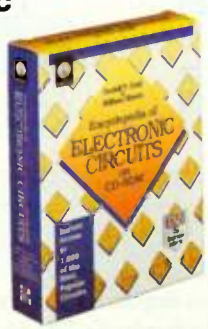

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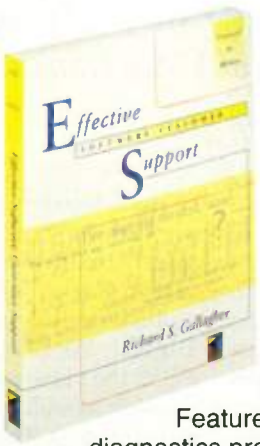

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A Pair of DVD Decoder ICs Use Microcoded Architecture To Give Users A Faster Way to Design, Differentiate, And Upgrade Digital Video Consumer Products.

Paul McGoldrick

The ZiVA-DS and the ZiVA-D6 are single-chip, highly-integrated, second generation DVD (digital versatile disk) decoders intended to replace the multiple chips used in the first DVD players. The decoders use microcoded architecture to shorten OEM design cycles—with subsequent faster time-to-market—and to allow for future upgrades with minimal design effort. The decoders offer full DVD specification compliance, high video quality, and tolerance from media errors. The ZiVA-D6 gives an integrated 5.1 channel Dolby Digital (formerly known as AC-3) audio output; the ZiVA-DS downmixes the Dolby Digital signals to two channels.

Multimedia cards featuring ZiVA support a high level of functionality, including full 30 field/s playback and wide compatibility with a broad range of graphics controllers. Design support is available in the form of a reference design for DVD multimedia products such as DVD PCI-compatible plug-in cards, or designs on a PC's motherboard with the decoders and Windows-compliant AVI drivers *(Fig. 1)*. The reference design includes the DVD decoder chip plus external dynamic random-access memory (DRAM) necessary for "holding" material during playback processes which are noncontiguous, plus the DACs for the audio.

A Macrovision 7 encoder is included in the video output path (C-Cube is licensed to sell DVD copy protection) and the interfaces to the PCI bus and VGA displays. For standalone consumer players, designers also can obtain the ZiVA manufacturer's kit featuring the ZiVA decoders and advanced navigation software.

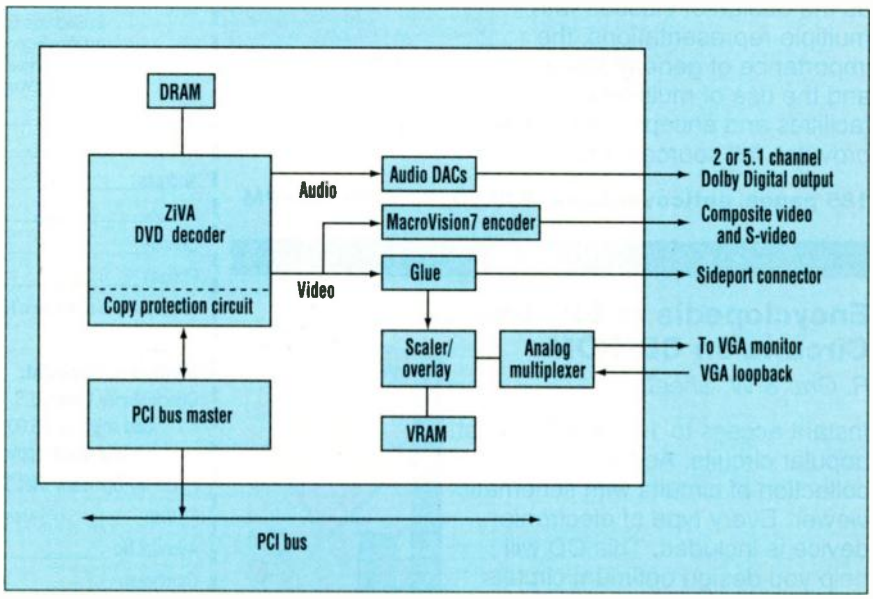
Both decoders contain the demultiplexers to separate the audio and video data streams as well as the on-screen display with three options for audio decoding in the form of Dolby Digital, MPEG decoding or linear PCM; the video path has the MPEG-2 decoder, as well as the sub-picture decoder *(Fig. 2)*. The complete specifications for the two ICs allows for both MPEG-1 and MPEG-2 video decoding with compressed resolutions of 720 x 480 at 30 Hz (for NTSC), 720 x 576 at 25 Hz (for PAL), and half-resolutions with 352 x 240 at 30 Hz and 352 x 288 at 25 Hz. DVD standards are decoded as well as legacy-compatible for Video CD 1.1, 2.0 and CD-DA. On the audio side, in addition to the Dolby Digital decoding, the MPEG decoding is for both MPEG-1 and MPEG-2, Layers I and II. The sample rates supported are 44.1, 48, and 96 kHz.

The compressed data that is input to the ICs can be in the form of a parallel DVD/CD interface or as an 8-bit host interface. The compressed data rate can be a sustained 16 Mbit/s, or can be a burst of 80 Mbit/s for the host interface or 160 Mbit/s for the parallel interface. The memory attached to the chips must be 16 Mbit of 70-ns EDO DRAM.

Microcode Architecture

C-Cube's microcoded architecture gives considerable freedom to OEMs in their designs and the feature set offered to the market in the form of different models; decoder functions can be packaged into user-oriented commands such as Play, Pause, and Slow-Motion, simplifying system software design. Microcode upgrades can be added later to expand the features, extending the design life for the future.

Like all consumer technologies, the success is usually in the content offered rather than the technology. With Hollywood finally behind the standard, the qualities of more storage, faster access, and higher quality video and audio are



1. Shown in the system block diagram is the reference design for the complete digital versatile disk (DVD) using the C-Cube decoder ICs ZiVA-DS or ZiVA-D6.

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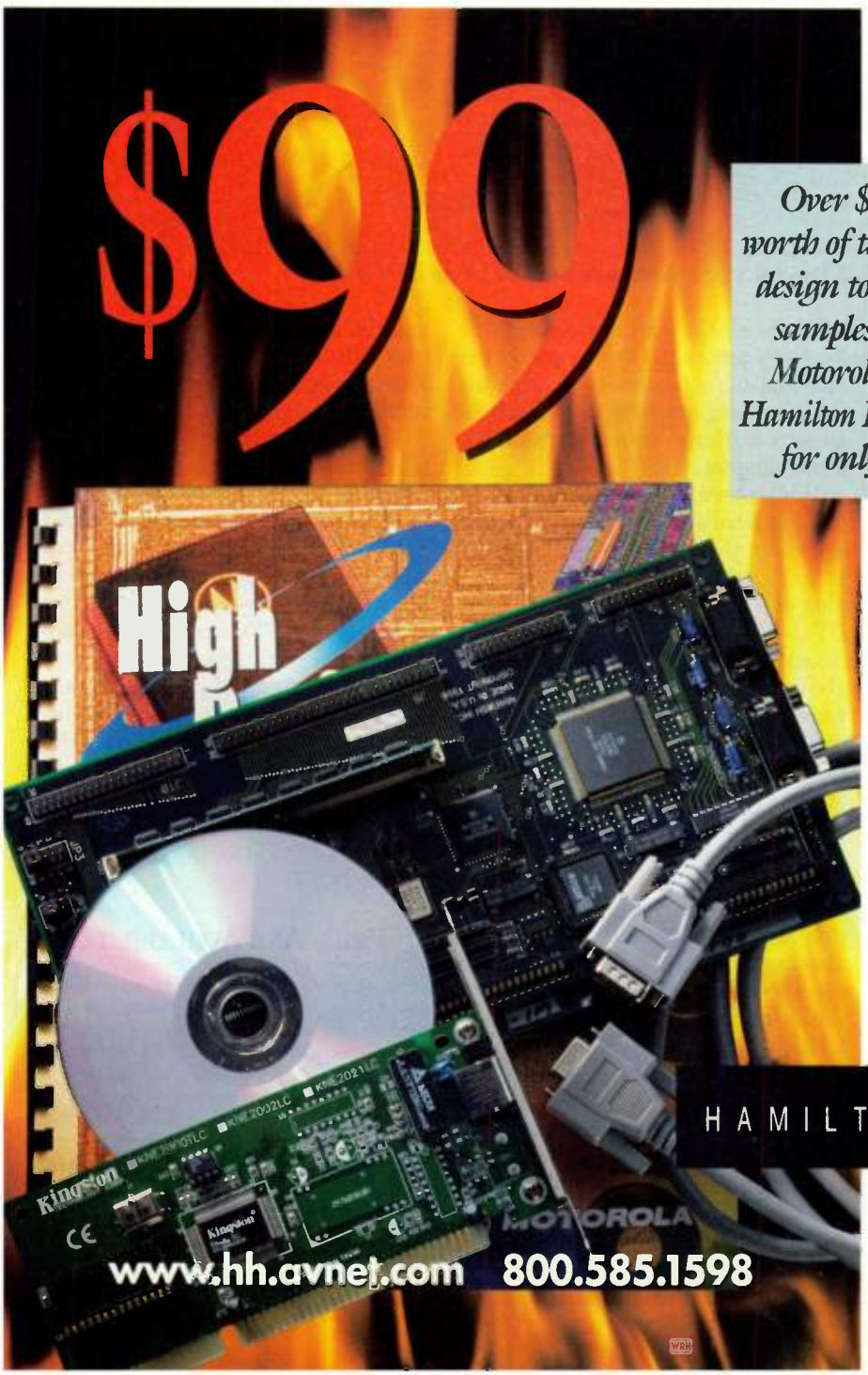

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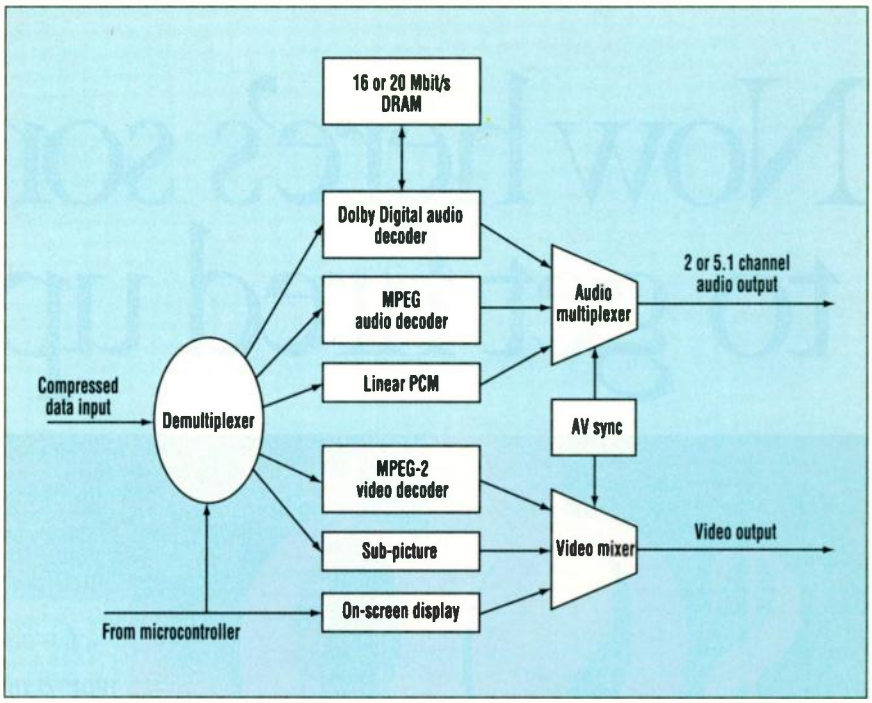

2. Depicted is the basic arrangement of the C-Cube ZiVA-DS and -D6.

likely to help the standard's acceptability. Copy protection for the content is essential and copy protection chips are now becoming available, but C-Cube is already working on an integrated descrambling solution.

While there is no current discussion of a nonhardware solution for DVD decoding, C-Cube believes that after 12 to 18 months of one-for-one shipping of a hardware decoder for each DVD-ROM drive, that situation will change. Designs will be announced in about 12 months for hybrid hardware/software solutions. At the same time, there will be a coming peak in demand for hardware solutions for notebooks. The total window for hardware decoders for DVD is seen by C-Cube to be about two years.

Apart from quality issues, where DVD has the highest video resolution and highest audio quality (but also has compression), the comparison of DVD with the other consumer video/audio playback systems—VHS and laser disc—indicates there is one current disadvantage of DVD when compared to VHS—lack of recording capability. However, the recording features are expected to be available in 1999. Moreover, DVD has significant advantages over both the others in terms of interactive functions such as multiangle, multiending, multiaspect ratios, sub-picture, parental control, playback at a lower censored category and, of course, use within a PC.

Margins in VHS are low, with the bill of materials (BOM) pricing ranging from $120 to $600 for consumer prices of $150 to $1000. The laser disc player has BOMs from $250 to $500, with consumer prices ranging from $400 to $1200. DVD players have a current BOM of about $700 and expected consumer prices ranging from $550 to $1200. By the end of 1997, BOMs are expected to range from $225 to $400 using the C-Cube chips. The ICs are designed for operation with a supply rail of 3.3 V ±5%, but they will tolerate 5 V. The packaging for the ZiVA-DS is a 160-pin PQFP and for the ZiVA-D6 is a 208-pin PQFP.

Price And Availability

The price of the ZiVA-DS will be about $45 each in volume, and will be between $50 and $55 each in volume for the ZiVA-D6. Samples are available now.

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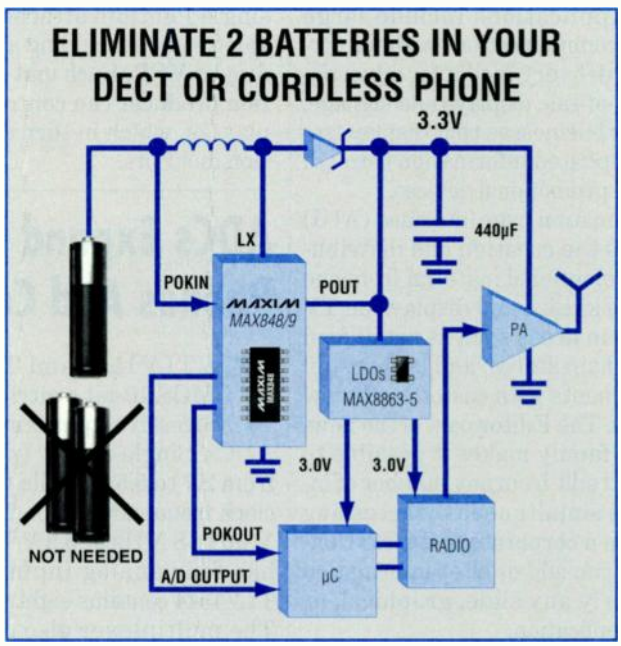

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New desktop video software, dubbed "newstation 6," enables chain stores and retail establishments to create, schedule, and distribute multimedia promotions and dynamic video signage with considerable flexibility and cost-effectiveness. The product addresses the needs of professionals who strive to communicate electronically to an entire employee population. Applications include large audience communications within a corporation, delivery media for advertising, point-of-sale displays and signage, and other businesses that display frequently-updated information through PC-based promotional devices.

An animation user interface (AUI) simplifies the creation and distribution of promotional material from one system to kiosks, and displays on TV monitors in areas such as retail food outlets, chain stores, and large retail establishments with customized show schedules. The Editor part of the newstation 6 family makes it possible to create and edit from any number of individuals simultaneously accessing one file on a corporate network. Contributors can add or alter information from nearly any slide, graphical, or textual application.

Emergency transmissions are provided for in newstation 6 with an emergency broadcast feature. It enables the creation of special shows which inform, explain, or direct employees faced with an emergency ; the emergency show list provides priorities from greatest to least risk. Emergency shows can't be deleted and they override any current corporate shows in locations identified by the emergency.

An optional accelerator combines MPEG hardware decoding to provide high quality full-motion images with a set of analog features to enhance the look and feel of corporate shows such as overlays and text crawls superimposed over video. The board also has an RF tuner that can inject current TV or cable programming into presentations. Both analog and digital video can be scaled on a continual basis from thumbnail to full screen. An on-board still-image capture makes it possible to inject stills into a presentation.

The desktop broadcasting network of VideoFax consists of three sections: the hub, the distribution system, and the display devices. The newstation producer, or the hub, is where presentations are assembled for broadcast and where master schedules are set. Complete authoring, playback, and communications software can run on a single Pentium attached to any live video source including a camera, laser disc, or VCR. Each unit of the newstation producer can control newstation players, which in turn control television monitors.

The display devices of newstation 6 take the form of televisions, video monitors, or LAN-based PCs. Viewer software is sold in bundles and lists for $199 per user for a 50-site network, and $125 per user for a 500-site network. The Editor software is currently available and lists for $795. There also will be an upcoming release of a video mail product that will provide Internet transfer of video messages created with newstation 6 software.

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60 Madison Ave.
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New York, NY 10010
(212) 689-3440
fax (212) 689-3616
e-mail: info@videofax.com
CIRCLE 468
PAUL McGOLDRICK

ADCs Expand DSP Portfolio For Cellular Phones And Consumer Electronics

The TLV1544 and TLV1548 are CMOS 10-bit switched-capacitor, successive-approximation (SAR) ADCs. Single-supply voltages can be from 2.7 to 5.5 V, while the maximum clock frequency can be 2.2 MHz at 2.7 V up to 8 MHz at 5.5 V. The TLV1544 has four analog inputs, while the TLV1544 contains eight analog inputs. The multiplexer also can switch to three internal self-test voltages.

Each device has a chip select, input-output clock, data input, and serial data output that provide a direct, four-wire, synchronous serial-peripheral interface port of a host microprocessor. When interfacing with a TMS320 DSP, an additional frame sync indicates the start of a serial data frame. The devices allow high-speed transfers from the host while an inverted clock input provides further timing flexibility for the serial interface.

The CMOS threshold detector in the SAR system determines the value of each bit by examining the charge on a series of binary-weighted capacitors. In the first phase of the conversion process, the analog input is sampled by closing one capacitor switch to the reference voltage and all of the series threshold switches simultaneously.

Two reference inputs are used—these voltage values establish the upper and lower limits of the analog inputs to produce a full-scale and zero-scale reading. The values of the upper and lower limits, and the analog input, shouldn't exceed the supply voltage or be less than ground. The digital output is at full-scale when the input signal is equal to or higher than the upper limit, and is at zero when the input signal is equal to or lower than the lower limit.

Maximum current consumption for the devices is 1.5 mA for supply voltages between 3.3 and 5.5 V. The power-saving feature is further enhanced with a software-programmed power-down mode and conversion rate—currents in power-down can vary from 1 to 25 mA. Leakage current from a selected channel is less than 1 mA. Typical input capacitance on both the analog and control inputs is 20 pF. The TLV1544 comes in a 16-pin SOIC package while the TLV1548 comes in a 20-lead SSOP. The 1000-piece price of the TLV1544 is $3.25; the TLV1548 goes for $3.64 in the same quantities.

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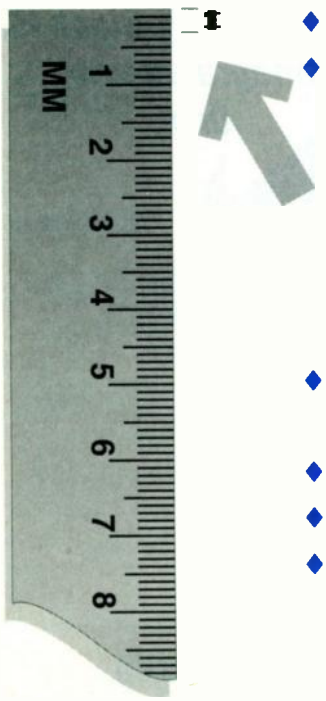

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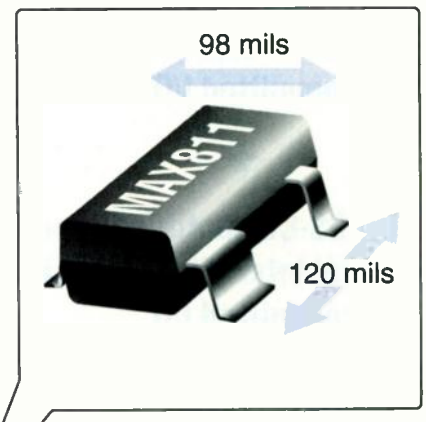
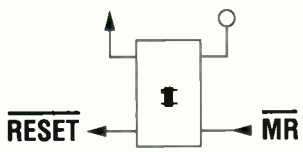


The SOT-143 package has four pins, allowing a manual reset input within a footprint no greater than 98 mils by 120 mils.



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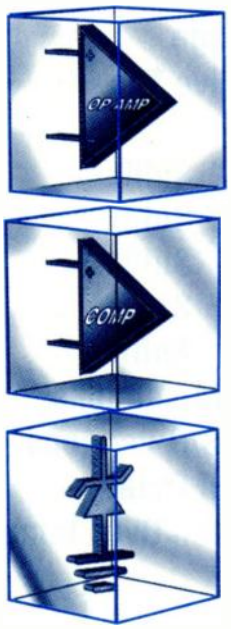

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Zero-Voltage Switching Converter

ERNEST WITTENBREDER
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Glendale, AZ 85308; (602) 439-1833; fax (602) 439-8203.

The "TWitt" converter shown features a forward converter transfer function and can operate effectively at high switching frequencies because it achieves zero voltage switching (ZVS) of all of its switches for all transitions *(Fig. 1)*. Because of its high switching frequency capability, high efficiency, and simple architecture, it can provide very high power density. Another benefit is that it eliminates diode reverse-recovery effects, which are a problem in other ZVS converters, such as the popular ZVS phase-shift-modulated full-bridge converter. Due to the converter's ability to eliminate reverse recovery, it can be operated without a snubber. (For more information on this circuit, check out the reference at the end of the article).

One of the shortcomings of the circuit is that it has both pulsating input and output currents similar to a continuous-mode flyback converter, but without the flyback's right half plane zero. By adding a second coupled inductor or flyback transformer, the output current can be made nearly constant throughout the switching cycle, except during the brief switching transitions. With proper design of the added transformer, the output current ramp slope becomes approximately zero. For input voltages that differ from nominal input voltage, the current ramp is small but non-zero.

Figure 2 illustrates the new, two-transformer TWitt converter. The size of the second transformer (T2) is typically 30 to 60% of the size of the main transformer (T1), depending on duty cycle. The size of the series choke (L_R) is 0.5 to 5% of T1, depending on circuit parasitics. The T1 transformer in Figure 2 is likely to be smaller than that in Figure 1 because the two transformers in Figure 2 share the load.

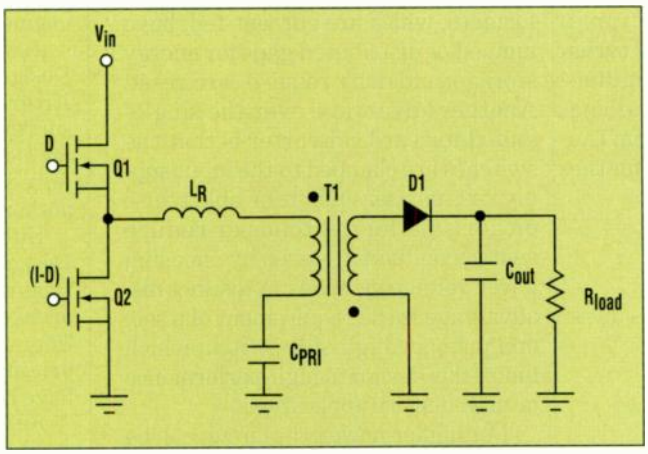
L_R provides the key to zero-voltage switching. The energy stored in this small choke plus the energy stored in the leakage inductances of the two transformers provides sufficient energy to drive both transitions of all switches, including rectifiers, and energy to charge and discharge all of the circuit's parasitic capacitances during the resonant transition. Part of the energy for each switching transition is supplied by the stored energy in one of the transformer's primary windings, which reduces the amount of stored energy required by the series choke (L_R) and the leakage inductances. However, the energy stored in the transformers is insufficient to complete the transition without some additional series inductance, due to the clamping of the primary circuit by the reflected output voltage. The converter operates using simple PWM control, with a short dead time between the on times of the two switches. When the upper switch (Q1) is turned on, T2 behaves like an ideal transformer.

The primary current in T2 has two components: the magnetizing current and the reflected secondary current. The current ramp in T2 is controlled by the open circuit inductance of the T1 primary winding (L1). The T1 transformer looks like a choke during this phase of operation because its secondary rectifier is reverse-biased while T2's secondary rectifier is forward-biased. Note the transformers' winding polarities in the figure. If the primary current I_2 were to be held fixed, then the portion of the primary current that's magnetizing current would increase and the portion that's reflected secondary current would decrease.

By increasing the total T2 primary current at the same rate as the rate of increase in T2 magnetizing current, the reflected secondary current remains constant. When the secondary current remains constant, there's no output inductor current ramp and, except for some minor sagging during the switching transitions, the secondary current remains at the same value throughout the cycle. As a result, the output filter capacitor value can be reduced when compared to a standard forward converter's output filter capacitor, and output ripple and EMI are reduced when compared to the standard forward converter. With the circuit element values shown in Figure 2, the rms output voltage ripple is less than 0.1% of the output voltage.

The magnetizing current ramp slope in T2 is $V_{out}/(N_2L_2)$, while Q1 is on. In this case, V_{out} is the sum of the output load voltage plus the rectifier forward voltage drop. The primary current ramp is $(V_{in} - V_{CPRI} - V_{out}/N_2)/(L1 + L_R)$. For the output current to be zero, these quantities must be equal: $V_{out}/(N_2L2) = (V_{in} - V_{CPRI} - V_{out}/N_2)/(L1 + L_R)$.

When Q1 is switched off, the energy stored in L_R drives a zero voltage transition and briefly reduces the output current. For the Q1 turn-off transition to be zero voltage, it must be turned off very quickly, which implies an appropriate gate-drive circuit. After the body diode of Q2 is turned on by L_R, the channel of Q2 is turned on at zero voltage and with zero switching power loss. During the



1. This buck-derived PWM converter, dubbed the "TWitt converter," operates effectively at high switching frequencies since all of its switches achieve zero voltage switching for all transitions. It provides high power density and eliminates diode reverse-recovery effects.

switching transition, the load current is shared by the two transformers as one transformer's current ramps down while the other transformer's current ramps up. The resonant switching transition current slopes in the transformers are controlled by the voltage applied to L_R and the value of L_R.

During the state in which Q2 is on, the primary current in T1 is controlled by the open circuit inductance of the primary winding of T2, which is L2. In this half cycle, the rate of increase in magnetizing current in T1 is equal to the increase in total primary current in T1, so once again the output current ramp slope is zero.

The magnetizing current ramp slope in T1 is $V_{out}/(N_1L1)$ while Q2 is on. The primary current ramp is $(V_{CPRI} - V_{out}/N_1)/(L2 + L_R)$. For the output current ramp to be zero, these quantities must be equal: $V_{out}/(N_1L1) = V_{CPRI} - V_{out}/N_1)(L1 + L_R)$. The requirement of volt second product balance in each magnetic circuit element forms three additional defining equations for steady-state circuit operation.

When Q2 switches off, the stored energy in L_R and leakage inductances drive another resonant transition, turning on the body diode of Q1. Q1 is turned on at zero voltage very soon after its body diode begins to conduct, completing the switching cycle.

Obtaining near-zero current ramp slopes can be done by adjusting turns ratios and primary-winding inductances of the two transformers. The operating equations derived from the five equations described earlier for the Figure 2 converter are:

$$V_{CPRI} = D\,V_{in}$$

$$V_{out} = V_{in}\,D(1 - D)/[D/N_2 + (1 + L_R/L1)(1 - D)/N_1]$$

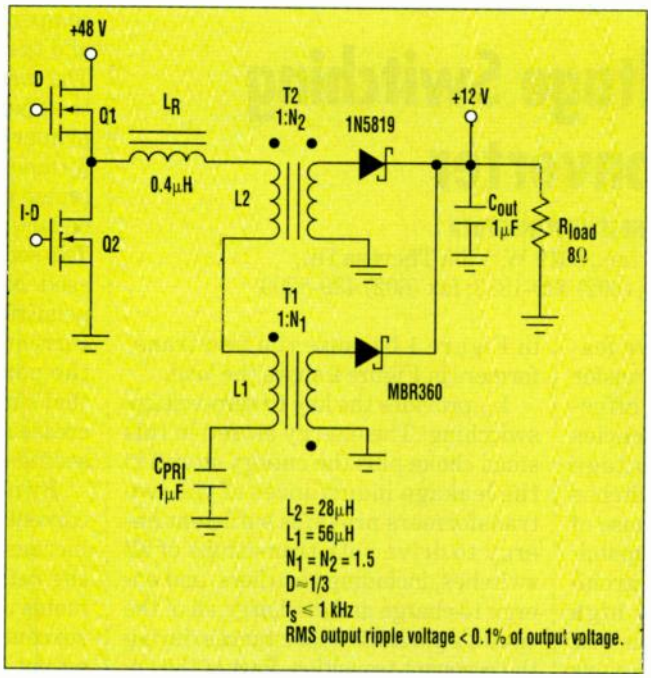
and

$$L2 = L1(N_1/N_2)D/(1 - D)$$

where V_{CPRI} is the primary capacitor voltage, V_{in} is the input voltage, D is the duty cycle, V_{out} is the output voltage, N_2 is the secondary to primary turns ratio of T2, N_1 is the secondary to primary turns ratio of T1, L1 is the primary open circuit inductance of T1, and L2 is the primary open circuit inductance of T2. The input-to-output transfer function is similar to the asymmetrical half-bridge designs and must be operated below 50% duty cycle. That's because the control-to-output transfer function goes to zero and changes sign at a duty cycle of 50%.

A reliability advantage of these converters is that there are no staircase saturation effects in the transformers, which are current-fed, have lumped or distributed gaps for energy storage, and don't require core reset. Another advantage over the single-ended forward converter is that the switches are clamped to the input supply rails so users might be able to use either smaller switches or reduce switch conduction losses by choosing lower voltage switches. A distinct disadvantage is the requirement of a second primary high-side switch, which limits this design to high-performance or high-density applications.

For higher power, the circuit can be bridged simply by adding two more switches and increasing the voltage rating of the primary capacitor. For bridging purposes, the primary capacitor isn't returned to ground but connected to a second pair of switches, which effectively doubles the input voltage applied to the converter. Because of the soft switching, low ripple, and the elimination of diode reverse-recovery effects, the converter is a good candidate for regulated high-voltage power supplies.



2. The addition of a second coupled-inductor or flyback transformer to the original TWitt convertertopology creates a nearly constant output current throughout the switching cycle.

Author's note: The Figure 1 circuit is patented and shown as an example of prior art. The new circuit represented and advocated by this Idea For Design is shown in Figure 2 and represents a circuit that overcomes shortcomings of the prior art as indicated in the article. The author will make no patent claim on the Figure 2 circuit. To the author's knowledge, no patent has been granted or is pending on the Figure 2 circuit, although it's quite likely patentable.

Reference:
Wittenbreder, E.H., "Zero Voltage Switching Pulse Width Modulated Power Converters," U.S. Patent 5,402,329, Dec. 9, 1992.

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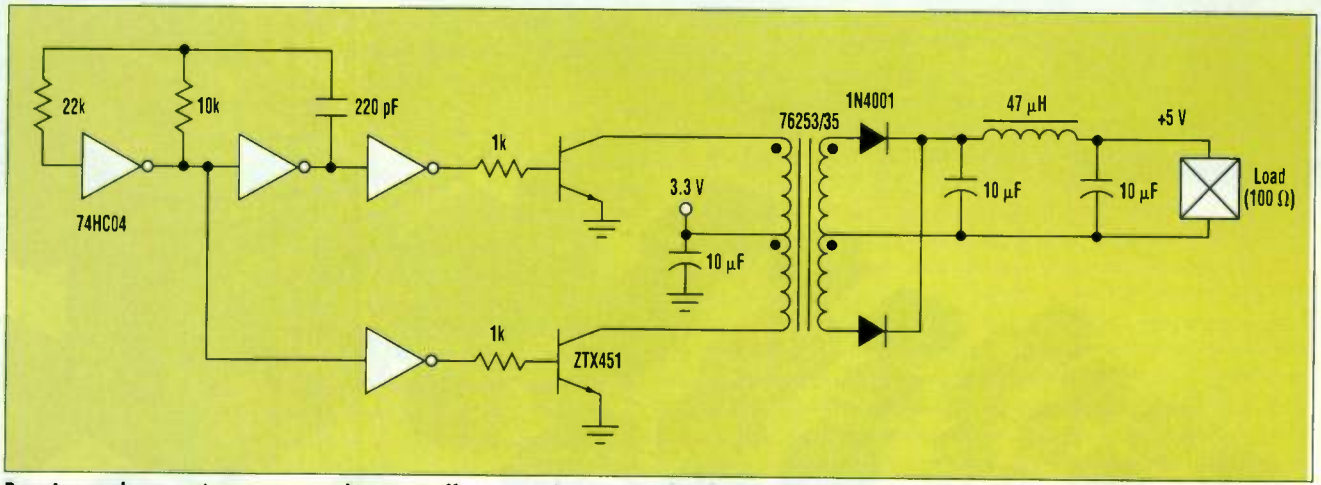
Occasionally, a 3.3-V logic system will need an isolated supply for a peripheral function. There are some dc-dc converters available. However, if spare inverters are present in the circuit, a low-cost solution can be produced using only four inverters and a few discrete components.

The design presented here employs four inverters to produce a square-wave RC oscillator with complimentary outputs *(see the figure)*. The output inverters drive switching transistors (ZTX451), which in turn drive an off-the-shelf, low-power transformer. The transformer (76253/35) is designed for use in 3-V to 5-V supply systems with the MAX253 IC. In the circuit shown here, the discrete implementation of inverters and transistors imitates the basic operation of the IC and produces an oscillator frequency of 200 kHz.

The transformer's output is unregulated and supplies approximately 250 mW of useful power at 4.80-V output from the circuit. This is often sufficient for peripheral functions such as slow ADCs and as a reference for 3-V to 5-V logic translators. If the circuit is planned for logic-translator applications, then the isolation may not be required and input and output ground can be connected together.

The circuit can be improved for higher current loads by reducing the 1k base resistors to the ZTX451 driver transistors. The overall circuit efficiency is 50%. Improvements can be made by using better Schottky diode rectifiers and lower V_{cesat} transistors (e.g., ZTX489).



By using stock magnetic components, this circuit offers a very low-cost method for adding a low-power 5-V supply to a 3-V logic system.

Circle 522

Simple Digital AC Wattmeter

W. STEPHEN WOODWARD
University of North Carolina, Venable Hall, CB3290,
Chapel Hill, NC 27599-3290.

To make useful measurements of "real" power consumption, wattmeters must be accurate despite large reactive and dc components in the current drawn by the monitored load. Moreover, power consumption from multiple ac phases (two in the case of a typical 220-V residential power panel, three in the case of 208-V industrial ac) must sometimes be simultaneously monitored and summed.

This simple, optically isolated wattmeter satisfies these criteria. It converts power readings from one or more phases to (given the circuit values illustrated) a 1-pulse/joule (1 Hz/W) frequency output. Optionally, it can be configured to run from an interface to the COM port of a standard PC. PC COM port hardware then interprets each 1-joule pulse as the "start bit" of a valid (although meaningless) ASCII character. Simple BASIC software *(see the listing)* running on the PC can monitor and average the frequency of character reception as an accurate measure of power consumption. Somewhat more sophisticated software could capture and store detailed logs of power consumption over arbitrarily long time periods.

The core of the wattmeter circuit is a quad-channel optoisolator consisting of LEDs E1-E4 and phototransistors Q1-Q4 connected in a double-bridge arrangement *(see the figure)*. This arrangement acts as a variant (admittedly peculiar) of the well-known

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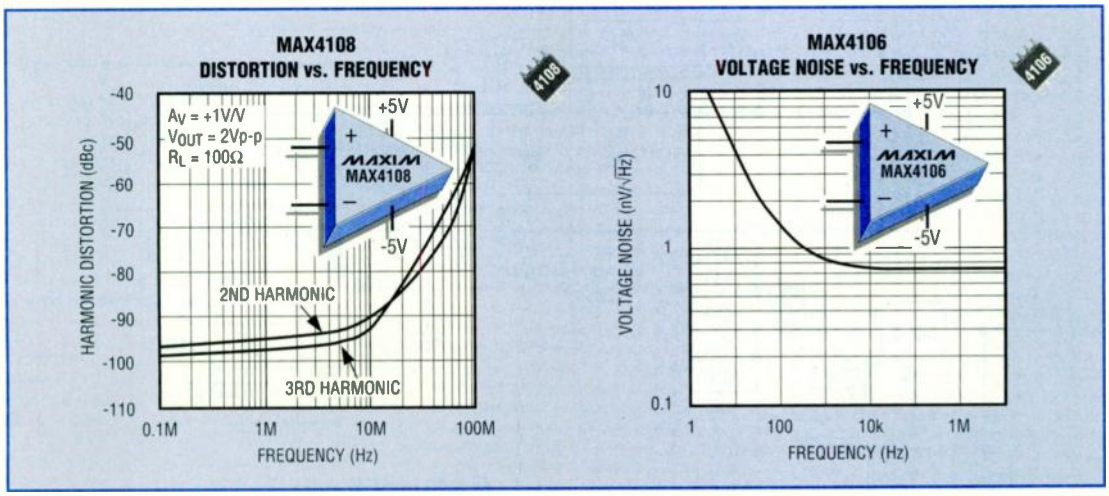

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Lowest Noise	MAX4106	5	350	275	18	-63 @ 5MHz	0.75	0.02	0.04
Lowest Noise	MAX4107	10	300	500	18	-60 @ 5MHz	0.75	0.03	0.03
Lowest Distortion	MAX4108	1	400	1200	12	-81 @ 20MHz	8.0	0.002	0.002
Lowest Distortion	MAX4109	2	225	1200	12	-80 @ 20MHz	6.0	0.002	0.003

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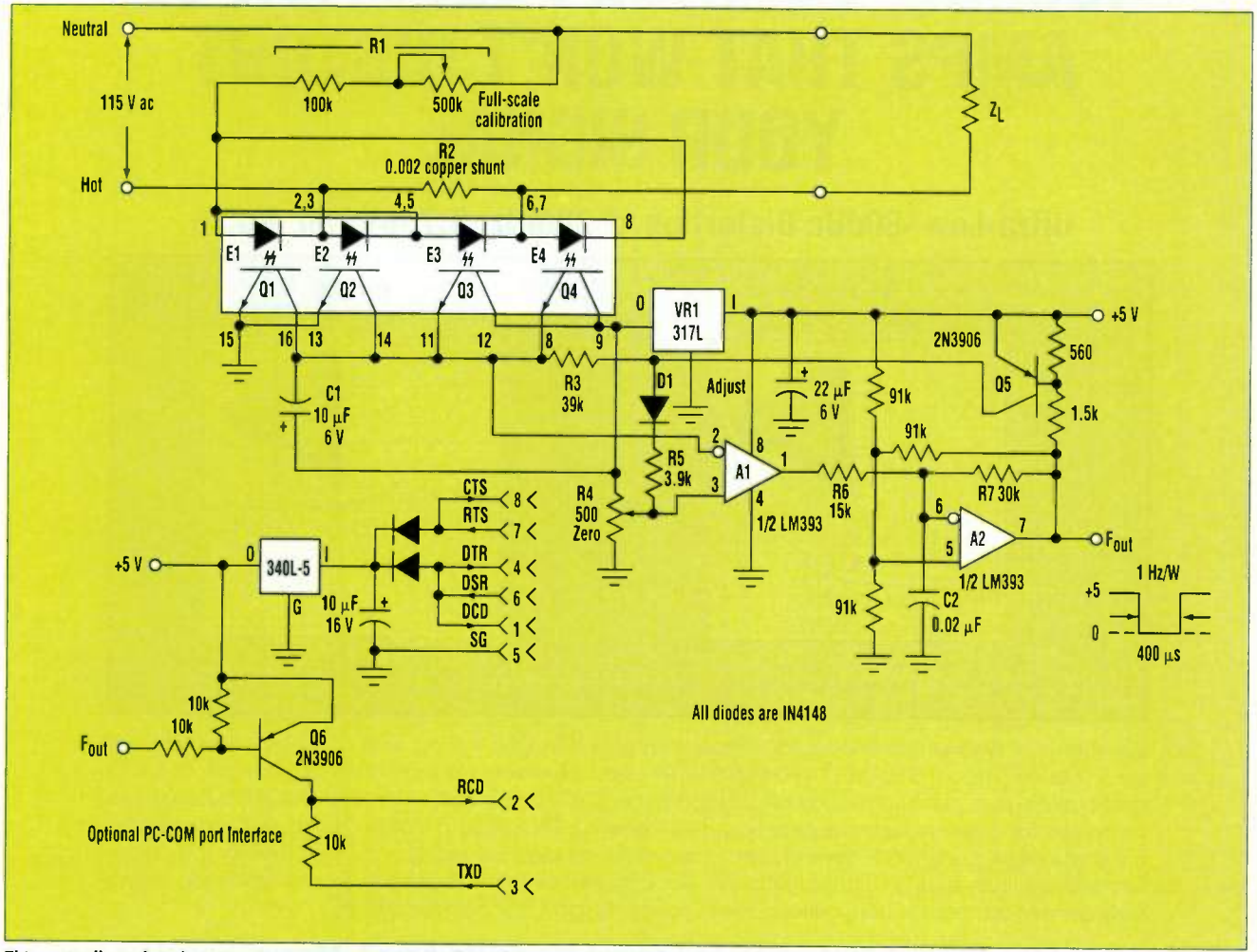

This optically isolated wattmeter converts power readings from one or more phases to a 1-pulse/joule (1 Hz/W) frequency output. The PC's COM port hardware interprets each pulse as the "start bit" of a valid but meaningless ASCII character, which are counted by the PC to obtain a reading.

"Gilbert cell" analog multiplier to compute the four-quadrant product of ac line voltage and Z1 load current.

The principle of operation of the optobridge multiplier is explained in an earlier Idea for Design (*"Optical Isolator Computes Watts,"* ELECTRONIC DESIGN, *Oct. 14, 1994, p. 102*). The multiplier's output is a current drawn from C1 that's proportional to the true instantaneous power delivered to the load. Accuracy is maintained even if the line voltage wanders and the load is reactive and nonlinear. If multiple ac power phases are to be monitored, only resistors R1 and R2 and the optoisolator need be duplicated for each additional phase. The phototransistors of the additional isolator(s) should be paralleled with Q1-Q4.

The current-to-frequency converter formed by reference VR1, comparators A1 and A2, and associated discretes, converts the passively summed power-proportional currents to a 0-1200 Hz output appearing at A2 (pin 7). If the wattmeter is to be used with a PC COM port, optional regulator VR2 can be added to develop a sufficient +5-V supply for wattmeter operation from the port "handshake" signals. No other dc power source is necessary. Meanwhile, Q6 will convert A2's output pulses to RS-232 levels.

In the prototype, the 0.002-W shunt (R2) consisted of 5.8 inches of 16 gauge copper wire. Copper's 3900 ppm/°C coefficient of resistance serves to temperature compensate most of the scale-factor variation due to LED and phototransistor temperature coefficients. Zero stability (voltage feedthrough) of the wattmeter is very sensitive to temperature gradients in the optoisolators. They should be shielded carefully from drafts.

```
' Wattmeter Power Display Demo ... W.S. Woodward
'     18.2065 ... # of MSDOS-compatible Time-of-Day "ticks"/second
      DEF SEG = 0: ' T.O.D. clock lives at memory addresses (&H46C,D)
' Setup COMport to accept Watt Meter character stream
      OPEN "COM1:9600,N,7,1,BIN,RB5000 FOR RANDOM AS #3
      ON ERROR GOTO ohoh: ' Discard spurious character formatting errors
wattmeter:
      tclk = 18: ' Setup to sum Wattmeter pulses for ~1 second
      SUM = 0: WHILE tclk > 0
          Y% = PEEK(&H46C): WHILE PEEK(&H46C) = Y%: WEND: ' Await a T.O.D. tick
          x% = LOC(3): SUM = SUM + x%
          A$ = INPUT$(x%, 3)
          tclk = tclk - 1:WEND
      PRINT USING "#####"; SUM
      GOTO wattmeter
ohoh: RESUME wattmeter
```

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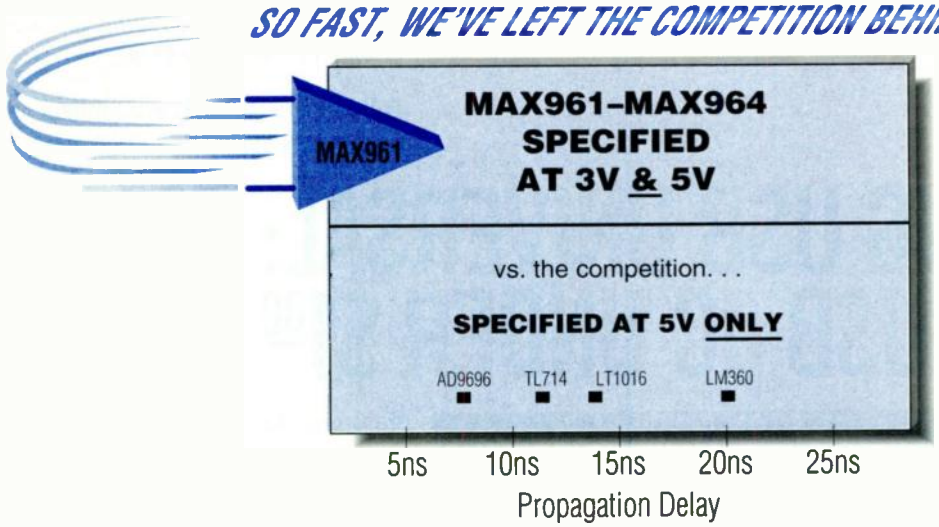

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MAX962	2	0.5	CMOS	No	+2.7 to +8	8	7
MAX963*	2	0.5	CMOS	Yes	+2.7 to +8	11	7
MAX964*	4	0.5	CMOS	No	+2.7 to +8	8	7

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CY7C632xx	128 Bytes	4 KB	10	18-pin DIP
CY7C634xx	256 Bytes	8 KB	31	40-pin DIP 48-pin SSOP
CY7C635xx	256 Bytes	8 KB	39	48-pin SSOP

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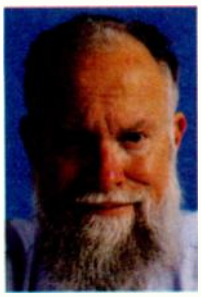
BOB PEASE

What's All This Solution Stuff, Anyhow?

Here are the solutions to last issue's puzzles: Of course, to post these *solutions* just two weeks after the questions, we had to print them before we saw any readers' answers. Thus any superior or amazing solutions sent in by readers will be mentioned in a couple months....

1. Little Egbert can arrange all 7 cylinders to touch each other—3 on a bottom deck, and 3 above them on a higher, parallel plane, and one down the middle *(Fig. 1)*. I can't prove that you can't do more than 7, but it looks convincing that you could never add one more to this arrangement and have it touch all the others. Conversely, I cannot think of any solutions for 5 or 6 cylinders that are not trivial variations on this. If you can get past 4, 7 is easy.

2. The minimum length is a bit less than 6.1 × D. The numerical answer is approximately 6.062178109 × D, give or take a few ppb. The first approximate answer is that the angle x is: $x = 49.1066° = \tan^{-1} 2/\sqrt{3}$. We can then solve for the length L by the law of sines: $L / \sin 60° = 3\sqrt{3} / \sin(120° - 2x)$. But by using the formula for the sin (a–b): $\sin(a-2x) = \sin a \cos 2x - \cos a \sin 2x$, and also the identity that $\sin 2x = 2 \sin x \cos x$, and starting from: $\sin x = (2/\sqrt{7})$ you come up with the precise answer that $L/D = 3.5\sqrt{3}$, which comes out to the numerical answer listed above.



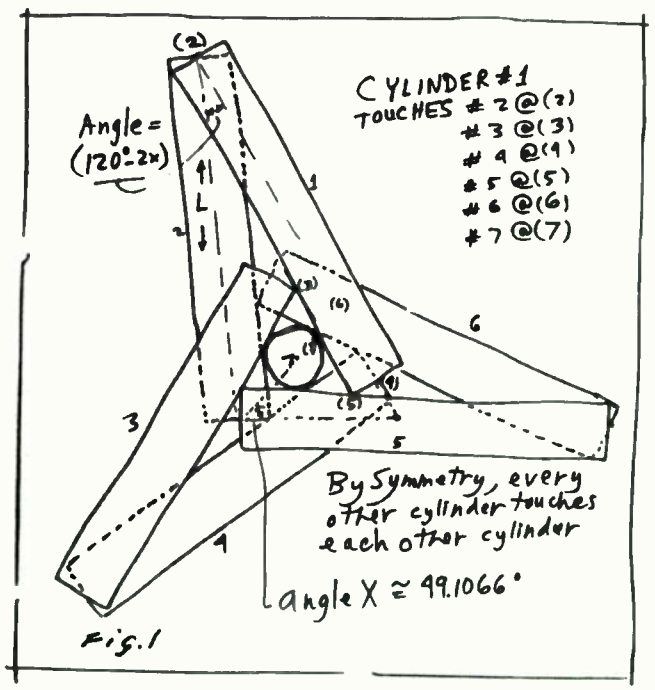
BOB PEASE OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

3. What is it, that is greater than God, worse than the Devil, and if you eat it you will die? NOTHING. One guy told me, "I ate nothing for breakfast. Am I going to die?" I replied, well, yes, sooner or later....

4. You can cut a doughnut into 13 pieces with three cuts. The first two cuts are fairly obvious, each slicing along the axis through the North Pole and the South Pole *(Fig. 2)*. A 90-degree angle looks nice, but any angle will do. Now, with the third cut, can you cut each of the 6 pieces into 2 pieces? Yes, and you can even cut one piece into 3 pieces, as shown. Cut through the axis at point X, and you'll get 7 more pieces. Admittedly, a couple of the pieces are pretty *small*.

5. By cutting at MMMM, and then at NNNNNNNN, you get 6 pieces. Now arrange the pieces as if on one flat plane, and cut carefully as shown (P-P), and you get 18 pieces *(Fig. 3)*. I had a solution with 14 pieces, but Jim Ball over in our Input Signal Group came up with this excellent and cagey solution. Some of these pieces are pretty *small*, too. Note, I drew this with a skinny toroid. It would work with *any* toroid, but the *drawings* would get too bulky if I did these cuts on the fat toroid shown in item 4.

6. The guy who sent us this riddle back in 1991, Steve Aisthorpe, just happened to depart from our trek around Mont Blanc, before we remembered to ask him to tell us the answer. So I kept racking my brain. *Sins*?? *Chest hairs*?? I was sitting on a stone wall in Dharapaani, Nepal, last March, 40 miles from the nearest road and 20 miles south of Dhaulagiri. I was resting and dangling my feet, when along came Steve! He was doing missionary work in that area. He finally told us the answer: PEERS. Good answer! It sure was good to see Steve after five years. Actually, he told us the riddle in part 3, above, too.



7. The cowboy's horse was named Friday. (Shamelessly lifted from *CarTalk*.)

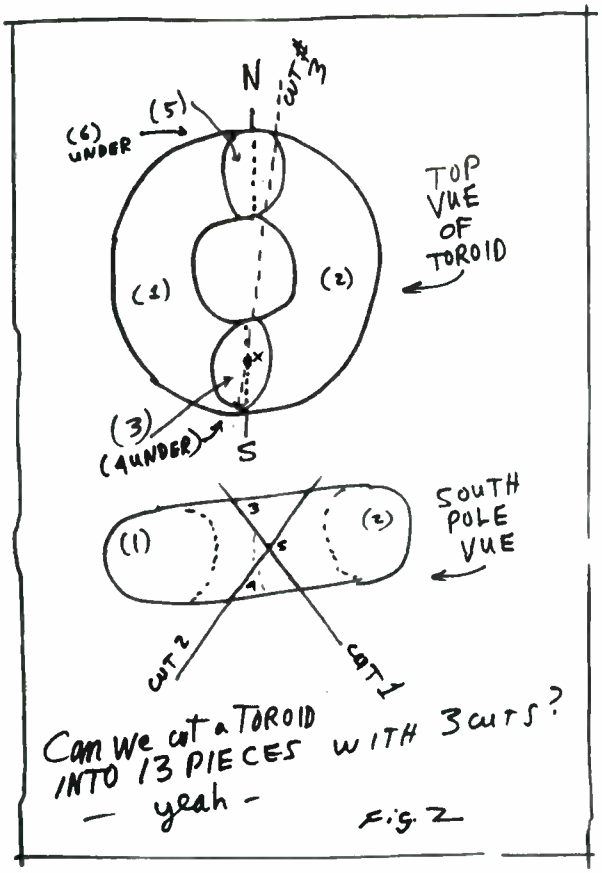
8. On October 4, 1582, THURSDAY, that was the last day of the old Julian Calendar. That was the day the cowboy rode into town. The very next day was Friday, October 15, 1582, which was the first day of the Gregorian calendar, which we still use. Six days later, it was Thursday, October 21, and the cowboy rode out of town. (NOT stolen from *CarTalk*.)

9. If you add a K to the letters in ISUZU, you can spell SUZUKI. If you add a V to the letters in DATSUN, and rearrange thoughtfully, you can spell SATURN.

10. Think about the status of the piece of paper that has been folded 9 times, just before the 10th fold. You have something as thick as a big tele-

BOB PEASE

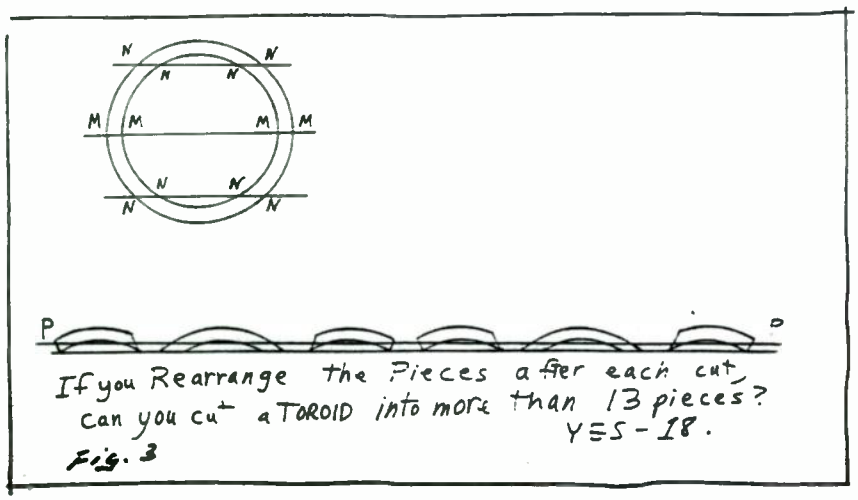
phone book, over an inch thick (even if you used very thin paper). It's kinda hard to fold it again—you certainly can't do that with a $10 bill. So, you lose. I, however, started with a piece of paper 100-feet long by 8.5- inches wide, from an old copy machine that used roll paper. I folded it 3 times to be 1-inch wide. Then I folded it 7 more times. It came out 5- in. thick—and barely 4-in. long—with a huge folded area. But if I had a big paper punch, I could have punched 1024 little paper circles... in concept.



11. *Extra Credit:* If the answer was "aggry and puggry"—What was the question? This: "There are 3 common, everyday words that end in 'gry.' One is *angry* and the other is *hungry*. What is the third word? We use it every day, though we do not think about it." As you may have noticed, the aggry (Ghanian burial bead) and puggry (alternate spelling of puggaree or puggharee, a scarf for the back of your neck in India) are NOT EXACTLY "common, everyday words." So let's lay that one to rest. When this question was passed around by word-of-mouth by teachers and students in school, and on the Internet, we trusted that it was a valid riddle, with a real answer. People who lay out trivial riddles that have no real answer, are NOT nice people. Not helpful. They make me *angry*. Life is full enough of tough questions that have tough answers, not to try to fool us with impossible questions.... Heck, this is just another way to use the Internet to waste time. The story I heard about the origin of this riddle was that a kid supposedly wanted us to think about *gravity*, but misstated the question. Yeah, sure.

Lastly—This is not a *riddle*, but a challenge appropriate for this time of year: can you bend some solder so it looks just like a paper clip? I'm pretty good with pliers, and I am pretty good at manipulating wire, but this is harder than it looks. Yet if you get some good results, you can puzzle the heck out of some secretaries. If you succeed, don't mail it to me, as it will croak in the mail. But if you photocopy four paper clips and four fakes, can I tell which is which? I made a few paper clips out of solder, indentations and all. Not worth the effort. Besides, they do not sit up in a magnetic paper-clip holder.

P.S. Take a peek at my new website: *http://www.national.com/design*, and hit "Good Stuff"—RAP



BOB'S MAILBOX

Dear Mr. Pease:

You write like some of my best teachers taught. Theory is fine, but experience passed on is crucial. I repair a lot of pc boards, most of which come from computers/electronic systems in machine shops. Some of this technology literally goes back to to the late 1960's and earlier. Some parts are difficult to find, so we sometimes substitute a newer, more-reliable component. We look for old data books and hang on to them to identify said old chips so we can test them. Imagine my surprise, therefore when I looked in the *National Semiconductor 1982 Linear Databook*. It officially describes your LH0033 and LH0063 as *Fast and Damn Fast Buffer Amplifiers*. 'Fess up, Bob. You wrote these, didn't you?

MATT J. McCULLAR
Arlington, Texas.

No, I didn't write those; they were done before I came to NSC in '76. About 1985, some born-again Christian wrote to Charlie Sporck and asked him why he couldn't delete the naughty word. He couldn't think of a good reason to argue.—RAP

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

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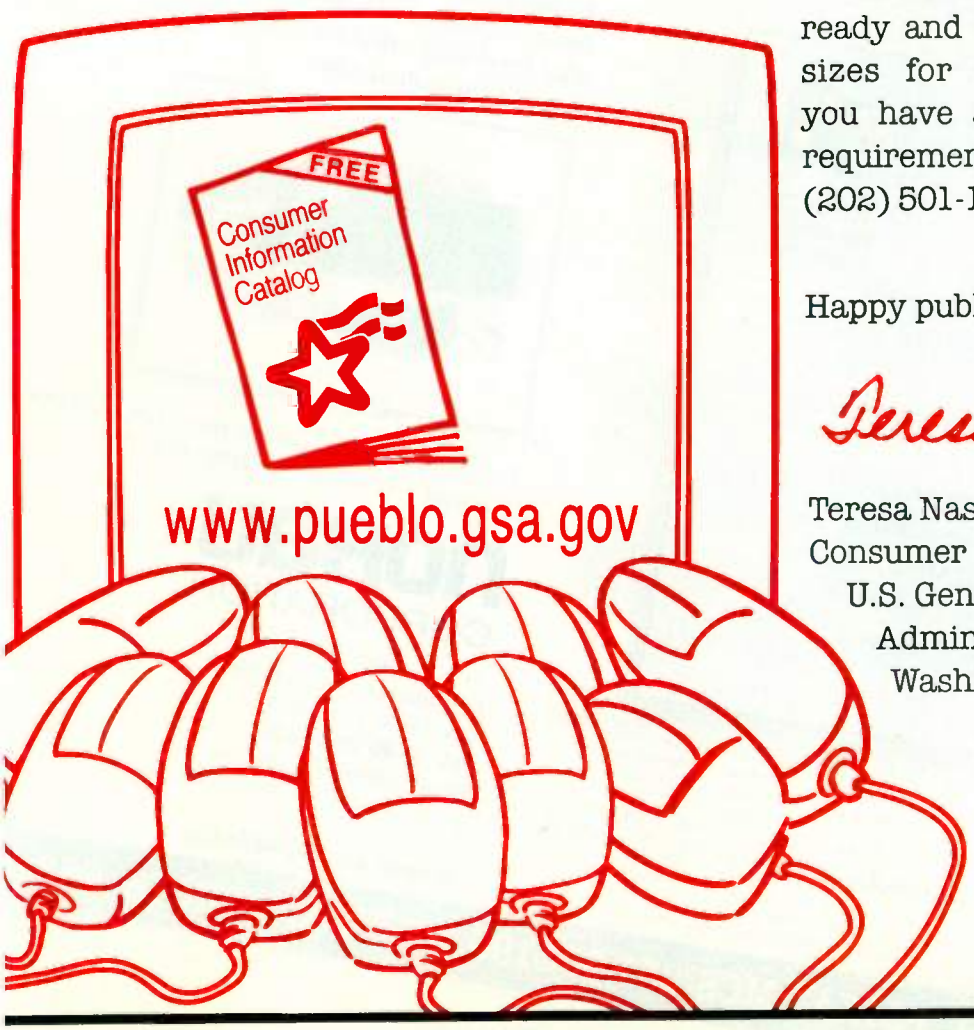

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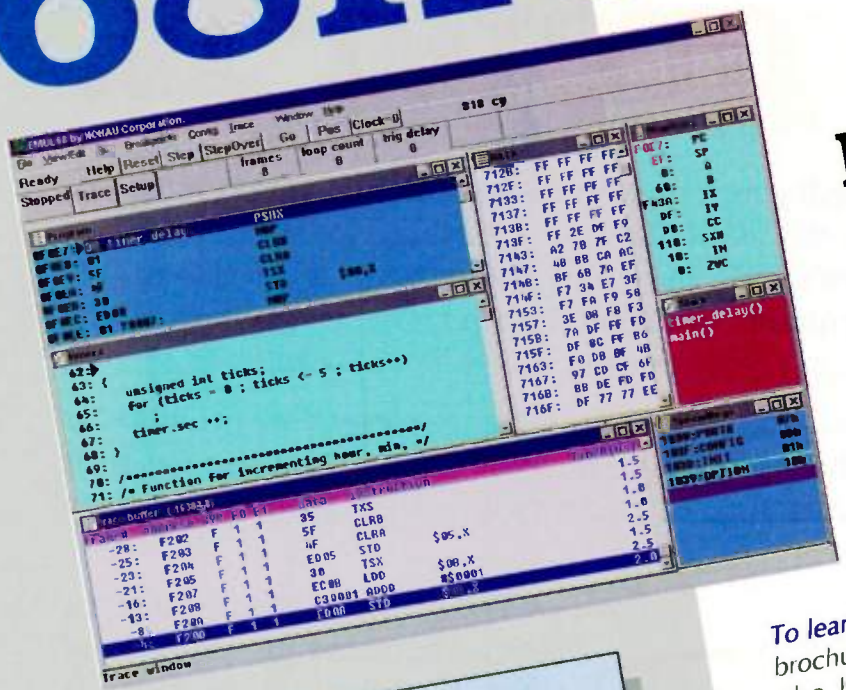

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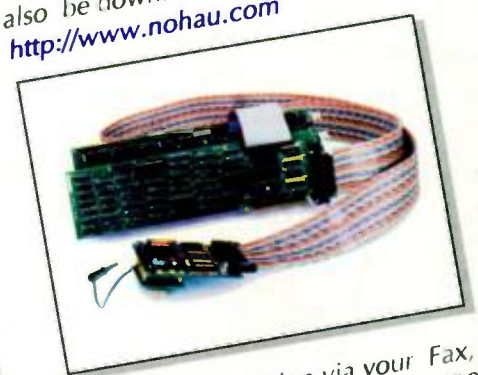

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HOWARD JOHNSON

Operating Above Resonance

Bypass capacitors, for us digital designers, are a fact of life. They may not be our favorite components, but we can't live without them. As we push designs to higher and higher speeds, it is becoming vitally important to understand how bypass capacitors will perform in the 100 MHz to 1 GHz region.

Those skilled in the art of analog design may point out that this frequency range is well above the series-resonant frequency of a typical bypass component. They may say such a component will become useless, or will fail to act as a capacitor, in our target frequency range. Don't be swayed by these arguments. You can still use bypass capacitors effectively in this range. Here's why.

The purpose of a good power bypass system is to provide a very low impedance connection between V_{CC} and GND at all speeds. A low impedance path from V_{CC} to GND permits chips to draw huge surges of current from the power rails without perturbing the power voltage. The lower the impedance between V_{CC} and GND, the less power supply noise a system will have.

Most designers know that the V_{CC}-to-GND impedance has to be low, but what about the phase? Is the phase of the V_{CC}-to-GND connection important? For example, the impedance phase angle normally associated with a bypass capacitor is 90° (voltage lags current). What if it were 0°? Would it still work?

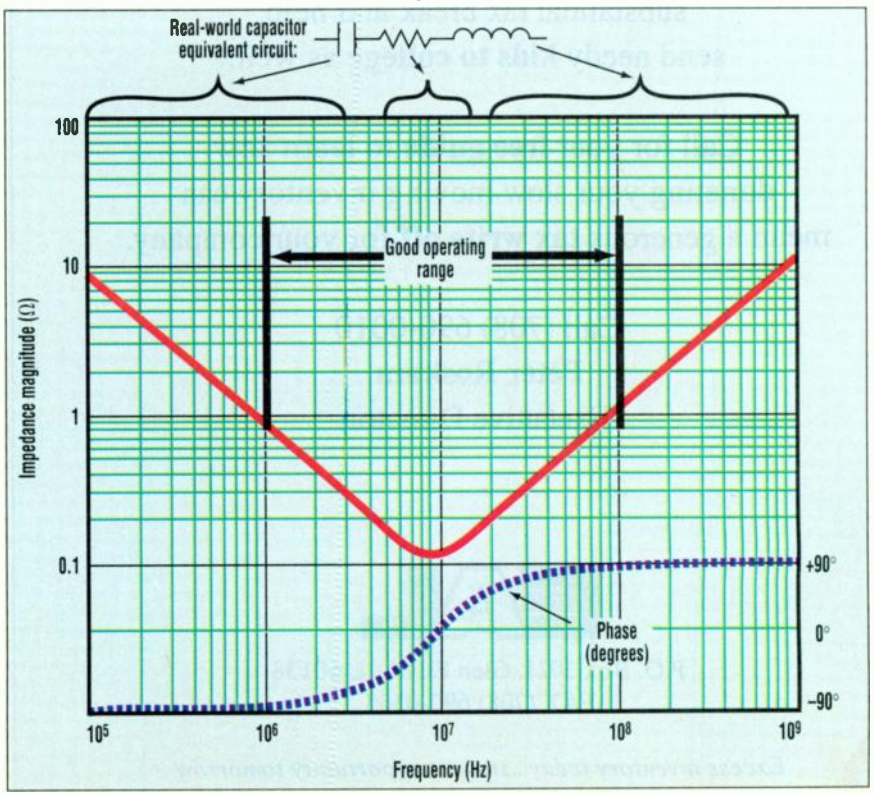
To investigate that question, let's set up a mental experiment. Imagine an ordinary digital product laid out on an FR-4 substrate and having mounting pads for 100 surface-mounted bypass capacitors. Next, mentally replace all the bypass capacitors with 1-Ω resistors (sounds crazy, but go ahead and do it). That would make the V_{CC}-GND impedance equal to 0.01 Ω, a nice, low impedance for this application. Everything looks fine except for one detail: We've shorted out the power supply with 0.01 Ω. No problem, since this is a mental experiment, we can hook up a 500-A current source to the power terminals and...*Voila*! We've made a very stiff 5-V power source with a 0.01-Ω output impedance. From the logic gates' perspective, it is near-perfect. The gates can draw huge surges of power without creating V_{CC} noise. Gates don't care about the impedance phase. They just care about the impedance magnitude between V_{CC} and GND.

HOWARD JOHNSON

But from the global warming perspective, maybe it's not such a good idea. With each resistor dissipating 25 W, the board is going to light up like the Fourth of July. Hint: This is a great experiment to try on Spice, but I wouldn't want to build it.

Fortunately, the premise of this column does not hinge on whether we can actually build a power system out of 1-Ω resistors. I'm merely pointing out that digital logic will work with any reasonably low impedance path between V_{CC} and GND without regard to the phase angle associated with that impedance, whether it is –90°, 0°, or even +90°.

The reason for this discussion is simple. It's because the phase angle of a real-world capacitor changes as a function of frequency *(see the figure)*. At low frequencies, a bypass component is essentially a perfect capacitor, and its impedance plot displays a phase angle of –90°. In the capacitive region, the impedance is decreasing at a rate of –20 dB per decade. At some intermediate frequency (10 MHz for the capacitor plotted in the figure), the component's series lead frame inductance becomes significant compared to the magnitude of its capacitance, and we enter the self-resonance zone. At the precise point of self resonance, the interaction of capacitive and inductive effects exactly cancel each other out; all we see is the equivalent series resistance (ESR) of the component. As we progress above resonance, the lead-frame inductance begins to dominate



the behavior of the whole component, the phase angle approaches +90°, and the magnitude plot starts heading up at a +20 db per decade rate.

As we go from low to mid-range to high frequencies, the impedance behavior changes from capacitive to resistive to inductive. Although the impedance magnitude wanders all over the map, and the phase flips polarity from −90° to +90°, it's still a useful bypass component. As plotted in the figure, over the range of 1 to 100 MHz, this capacitor maintains an impedance of 1 Ω or less. That's good enough for most digital work. From 1 to 100 MHz, 100 of these babies would give us our 0.01 Ω. Note that at 100 MHz, we'd be using this bypass component more than an order of magnitude above its series resonance frequency. That's OK. That's the nature of the bypass capacitor application.

Analog applications are different. In the analog design world, particularly in linear time-invariant filter designs, phase is everything. For example, in a five-pole Butterworth filter, a phase error of a couple of degrees can degrade performance noticeably. An analog designer in such an application would be very cautious about using a capacitor anywhere near resonance. Analog filtering applications often demand precise phase response. For that reason, many analog designers think of a capacitor's series resonance point as representing something akin to total circuit dysfunction. They just don't use them above resonance.

Happily for us digital folks, we can live with the resonance, and way beyond, too. Resonance in bypass capacitors is a property to be managed and used, not avoided.

Dr. Howard Johnson (howiej@sigcon.com) is the president of Signal Consulting, Inc., a high-technology consulting firm specializing in solving high-speed digital design problems. He is the author of "High-Speed Digital Design: A Handbook of Black Magic" (Prentice-Hall, 1993), and a frequent guest lecturer at both the University of Oxford and UC-Berkeley. For information about his ongoing series of on-site workshops for digital engineers, visit Signal Consulting's website at http://www.sigcon.com.

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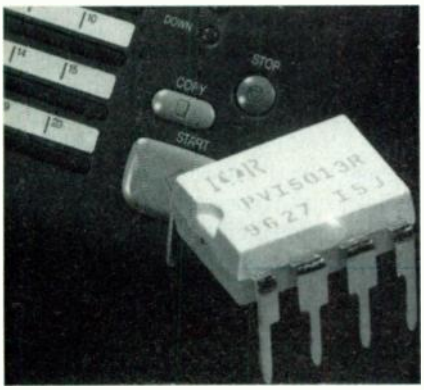

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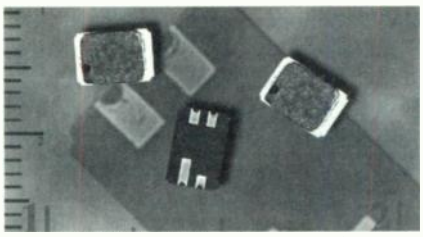
The MPH series of matched-pair resistor networks are hermetically sealed, have an absolute tolerance of 0.1 to 1%, and provide a shelf stability of less than 100 ppm per year absolute. The ratio tolerance is 0.05 to 0.1%. Absolute TCR is +-25 ppm/°C standard, with TCR tracking to ±2 ppm/°C. Temperature range is -55 to +125°C. These elements are rated at 100 mW (typical) at 70°C. Prices range from $3 to $5, depending

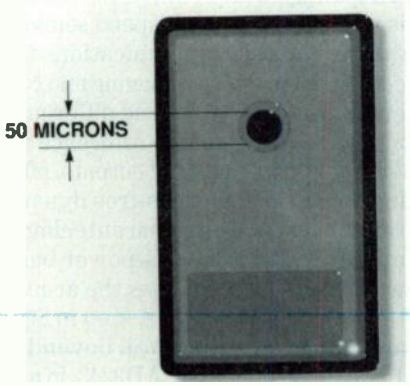


on performance requirements. Availability is 6 to 8 weeks. PM

Vishay Thin Film, 2160 Liberty Dr., Niagara Falls, NY 14304; (716) 283-4025; fax (716) 283-5932. **CIRCLE 709**

Infrared LED Provides A Point Source

The OED 884 is a point-source infrared LED (880 nm) with an emitting surface measuring 50 µm in diameter. The device has a typical output of 2 mW at 50 mA and has a spectral-line half-width of 45 nm. The rise and fall times are 20 ns each. The device comes in chip form



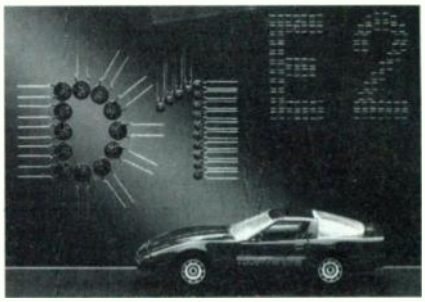
or mounted in a TO-18 hermetically sealed glass-and-metal package. Optionally, the device can be mounted hybrid fashion on a variety of substrates, including pc boards and ceramic hybrid assemblies, or in arrays. PM

Centronic Inc., E-O Div., 2088 Anchor Court, Anchor Business Park, Newbury Park, CA 91320-1601; Yuval Tamari, (805) 499-5902; fax (805) 499-7770. **CIRCLE 710**

Rugged Varistor Families Handle Vast Temp Range

The D1 varistors SIOV-S...AUTOD1, radially leaded disk varistors aimed at applications with a maximum operating temperature of +125°C, have full dc and load-dump capability. They can survive a thousand temperature shocks between -40 and +125°C, as well as accelerated humidity tests at 85°C/85% RH with maximum operating dc voltage.

Typical applications of these overvoltage-protection devices include motor controllers and high-voltage gas-discharge lamps (HIDs). Diameters range from 5 through 14 mm, the latter being able to absorb up to 50 J of



load-dump energy.

Another new varistor series is the E2 series (CN2220S14BAUTOE2G2), with a load-dump energy absorption capability of 25 J. They're able to withstand a maximum current surge of 1200 A. Other features include a protection level of 40 V at 10 A plus a temperature range through +125°C. They present a surface-mount alternative to earlier 10-mm disk varistors. AV

Siemens Matsushita Components, Infoservice, P.O. Box 2348, 90713 Fuerth, Germany; fax +49-911/978-3321. **CIRCLE 711**

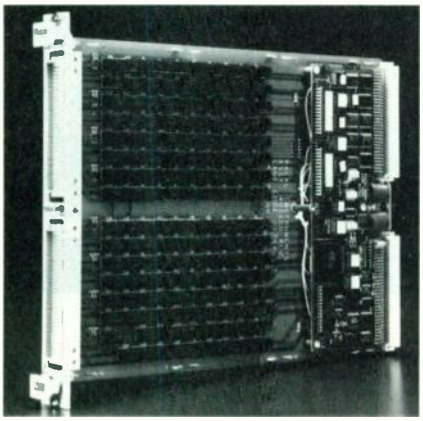
Miniature Inductors Are Surface-Mountable

Targeting telecom, test-equipment, and medical applications, the EC3225 and EC4532 surface-mountable inductors measure 3.2 by 2.5 by 2.2 mm and 4.5 by 3.2 by 3.2 mm, respectively. The EC3225 has an inductance range of 0.12 to 220 µH while the EC4532 has an inductance range of 0.1 to 1000 µH. The devices come with tolerances of ±20%, ±10%, or ±5%, and have an operating temperature range of -25° to 85°C. Tape-and-reel packaging is standard. Delivery is from stock to eight weeks. PM

Ecliptek Corp., 3545 Cadillac Ave., Costa Mesa, CA 92626-1401; (800) ECLIPTEK; fax (714) 433-1234.
e-mail: ecsales@ecliptek.com
Internet: http://www.ecliptek.com
CIRCLE 712

Low-Cost Digitizer/Waveform Generator For VXIbus Systems

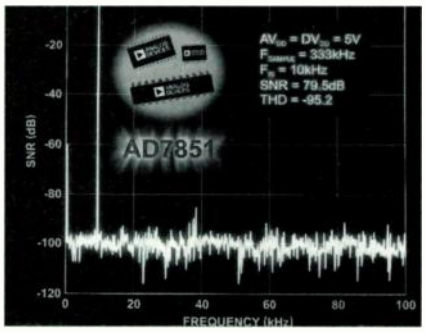
The 6062 is a VXIbus ADC and DAC that offers systems integrators a low-cost digitizer and waveform generator in a single-slot, C-size module. With 16-bit resolution and 8-channel mixed ADC and DAC inputs and outputs, the unit allows digitized signals to be captured for analysis in the computer. It also provides high-quality, sine, triangle and ramp waveforms for test simulation. Each channel has 64 ksample of memory, and up to three channels can be combined up to 567 ksamples. This allows for configurability and precision with independent channel-timing and flexible triggering. ADC sample rates can be up to 400 ksamples/s; for the DACs, sampling can be up to 2.5 Msamples/s. The modules fully comply with the latest revision of the VXIbus specifications (Racal being a founding member of the VXIbus consortium), and VXI*plug&play* drivers are included. PMcG



***Racal Instruments Ltd.**, 480 Bath Rd., Slough, Berkshire, SL1 6BE, UK; +44 (0) 1628 604455 (John Brampton); U.S. sales: (714) 859-8999 (Todd Nash).*
CIRCLE 713

Monolithic 14-Bit ADCs For General And High-Speed Apps

Two new monolithic ADCs are believed to be the fastest 14-bit devices in the market. The AD7851 has been developed for general purpose and the AD9243 for high-speed solutions. The AD7851 runs off a single 5-V supply and dissipates about 60 mW with a throughput of 333 ksamples/s; the power-down mode dissipates about 5 µW. Two input ranges are offered with reference voltages from 4 V to V_{DD} and with self-calibration and system-calibration options, and autocalibration at power-up. The input signal range allows for conversion of full-power signals up to 20 MHz.



The AD7851 comes packaged in 24-pin DIPs, SOICs, and SSOPs. The AD9243 breaks the 1-MHz sampling rate barrier, operating at 3 Msamples/s. Operating from a single 5-V rail and dissipating about 110 mW, the AD9243 is well suited for high-speed semiconductor and telecommunications test equipment, as well as imaging and communications system. True differential inputs have an on-chip reference and 3/5-V compatible digital outputs, offering an SFDR (spurious-free dynamic range) of 91 dB and guaranteeing no missing codes. The full-power bandwidth of 40 MHz enables the acquisition of a full-scale input step in 80 ns and under-sampling well beyond its 1.5-MHz Nyquist. The AD9243, in a 44-pin MQFP package, is priced at $49.00 in 1000-piece lots. The AD7851 is priced at $12.50 in 1000s. PMcG

***Analog Devices Inc.**, 804 Woburn St., Wilmington, MA 01887; (617) 937-1428, fax (617) 821-4273; Web: http://www.analog.com.* **CIRCLE 714**

Clock Generator Simplifies Satellite, Terrestrial TV System

The FS6011 digital video/audio clock generator, an IC that produces the 27-MHz reference clock for MPEG-2 video decoders, simultaneously produces audio-oversampling, utility/modem, and system-processor clock outputs. The IC can run stand-alone or it can be precision-locked to an external source. The integrated VCXO permits precise locking of all programmable frequencies without frame-dropping or frame-repeating. This is accomplished by using a combination of both analog and digital tuning techniques to ensure maximum stability and tuning resolution, particularly in the standalone mode.

The audio clock frequencies support 32-, 44.1- and 48-kHz 256X oversampled DACs as well as 384X at 44.1 and 48 kHz. The frequencies can be "tweaked" plus or minus just less than 0.1% to provide a seamless resynchronization of audio and video—these are fixed ratiometric changes and not variables. A total of three on-board PLLs are used for the processor, utility, and audio clocks. Expected applications for the IC include digital satellite video/audio decoders, multimedia PCs, and the upcoming digital terrestrial broadcast decoding. The FS6011 requires about 30 mA from a 5-V supply and is sampling now in a 16-pin SOIC package, priced at $2.95 in quantities of 10,000 pieces. An I^2C version of the device is expected to sample next quarter. PMcG

***Focus Semiconductor Inc.**, 768 North Bethlehem Pike, Suite 301, Lower Gwynedd, PA 19002; (215) 654-9700; fax (215) 654-9791.*
focus@focussemi.com
http://www.voicenet.com/~focus.
CIRCLE 715

SPST Switches Are Pin-Compatible With 74H4316

The MAX4536/37/38 series of quad, SPST (single-pole, single-throw) analog switches, which incorporate a common enable pin, are each pin-compatible with the 74H4316. Contacts for the 4536 are normally open; those of the 4537 are normally closed; and those of the 4538 have two normally open and two normally closed contacts. The switches can be operated from either single supplies of 2 to 12 V, or from dual supplies of ±2 V to ±6 V and will switch rail-to-rail. The on-resistance of a maximum of 200 Ω with a single 5-V rail halves with ±5-V supplies. Resistances match within 4 Ω. Power consumption is less than 1 µW. The switches come in 16-pin DIP, narrow SO, and QSOP packages with prices at $0.98 for 1000-unit lots. PMcG

***Maxim Integrated Products**, 120 San Gabriel Dr., Sunnyvale, CA 94086; (800) 998-8800, or (408) 737-7600, ext. 6087; http://www.maxim-ic.com*
CIRCLE 716

Noise Generator Targets CATV System Testing

The UFX-BER-CATV is an additive white Gaussian noise generator that covers the 5-to-850-MHz band. The unit is designed to test CATV systems and cable modems by injecting noise in the upstream and downstream paths.

The instrument automatically sets accurate C/N (Eb/No) ratios, which greatly reduces bit-error-rate test times. Direct setting of Eb/No, C/N, C/No, and C/I is available, or users can employ the IEEE-488.2 bus for remote control. LabVIEW drivers are available for the creation of fully integrated automatic test systems. Call for price and availability information. JN

Noise Com Inc., *E. Midland Ave., Paramus, NJ 07652; (201) 261-8797; fax (201) 261-8339; e-mail: info@noisecom.com; http://www.noisecom.com.*

CIRCLE 717

Pulse and Digital-Delay Generators Offer Versatility

A line of multichannel pulse and digital-delay generators provide features that enhance their versatility. The Model 400 and 500 series instruments, which come in two-, four-, and eight-channel modes, have optoisolated in-

puts and outputs for noisy environments. The units supply a wide range of operating modes, including delay and width control on all channels, internal and external trigger, duty cycle, burst, and gate. RS-232 remote control is standard on all models, and IEEE-488 is optional on four-channel versions. Prices start at $940 for two-channel models. JN

Berkeley Nucleonics Corp., *3060 Kerner Blvd., No. 2, San Rafael, CA (415) 453-9955; (415) 453-9956; www.BerkeleyNucleonics.com.*

CIRCLE 718

VXI Module Merges DMM, Counter Functionality

The VX4101 DMM/Counter combines a full-function 5-1/2-digit digital multimeter and a two-channel 250-MHz universal counter in a one-slot, C-size VXI module. Meter functions include ac and dc volts, 2- and 4-wire ohms, and dc current. It can take 50 5-1/2-digit readings per second and 1000 4-1/2-digit readings per second. The counter performs frequency, period, time interval, pulse width, and other measurements. Resolution is 250 ps single-shot and 1 ps averaged. Optional 500-MHz coverage is available for the two channels, as is a 3-GHz prescaler third channel. Also included is an integrated switching and scanning control that DMMs and other VXI instruments often need. The VX4101 is priced at $5395. The 500-MHz option is $495; the 3-GHz third channel is $1095. JN

Tektronix Measurement Group, *P.O. Box 1520, Pittsfield, MA 01202; (800) 426-2200 code 575; http://www.tek.com/Measurement.* **CIRCLE 719**

In-Circuit Programmer Handles 32 Cards At Once

The T-4000 in-circuit programming system can program or (after erasing) reprogram up to 32 circuit cards simultaneously. The system supports all types of programmable devices, including microcontrollers, flash, EPROM, EEPROM, FPGA, EPLD, PAL, GAL, and others. A custom adapter configured with sockets and cables to convert the printed-circuit boards to the T-4000 connects the boards to the programmer. Using in-circuit programming eliminates the need for sockets on the boards themselves. Base price of the T-4000 is $13,950, including training and lifetime technical support. JN

Sunrise Electronics Inc., *675 Brea Canyon Rd., No. 6, Walnut, CA 91789; (909) 595-7774; fax (909) 594-7009; e-mail: sunrise@sowest.net.*

CIRCLE 720

100-MHz Analog Scope Offers 3 Channels, 8 Traces

The three-channel Model SS-7811 analog oscilloscope features a dc-to-100-MHz bandwidth, 2-mV/div. sensitivity, and the ability to save up to 32 front-panel settings. The eight-trace scope includes fast automatic setup, full TV triggering with field and line selection, a fast sweep to 2 ns/div., and a five-digit frequency counter with ±0.01% accuracy. The channel 3 input can be switched between 50-, 100-, and 500-mV/div. inputs, making it ideal for ECL, TTL, and 24-V applications. Overall accuracy is ±2%. Cursor indications can be instantly canceled or restored, and a responsive multifunction control handles hold-off, delay, trace separation, TV line, and cursor settings. Delivery for the SS-7811, which costs $1795, is approximately two to three weeks. JN

Iwatsu America Inc., *Test and Measurement Equipment Div., 430 Commerce Blvd., Carlstadt, NJ; (201) 935-8486; fax (201) 935-8533; Web: http://www.iwatsu.com.*

CIRCLE 721

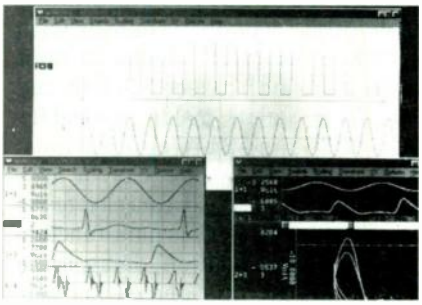
100-W Solid-State Amplifier Covers 1-to-1000-MHz Range

An all-solid-state amplifier, the Model 100W1000 delivers a minimum of 100 W of CW power from 1 MHz to 1000 MHz. The minimum linear output power measured at the 1-dB gain compression point is 60 W over the same bandwidth. The minimum gain at the maximum setting is 50 dB. The amplifier is well-suited for applications such as RF susceptibility testing, antenna and component testing, and watt-meter calibration. It also can be used as a driver for frequency multipliers and higher-power amplifiers. An analog front-panel meter displays forward and reflected power up to 150 W. The amplifier will operate into any magnitude and phase of source and load impedance, including shorts and opens, without damage or oscillation. It will provide full rated power without foldback into loads with VSWRs of up to 6.0:1.The Model 100W1000 costs $28,000. JN

Amplifier Research, *160 School House Rd. Souderton, PA 18964-9990; (800) 933-8181; fax (215) 723-5688; http://www.ar-amps.com.* **CIRCLE 722**

Data-Acquisition Tool Has New Features

WinDaq/200 multitasking data-acquisition software developed by Dataq Instruments has a feature set that allows users to acquire, review, store, and analyze waveforms without leaving the Microsoft Windows programming environment With this multi-



tasking capability, users can acquire and record waveform data to disk without interruption in the background, while operating any combination of other Windows applications in the foreground.

Waveform data can be reviewed and analyzed while the information is acquired and streamed to disk. Acquired waveform data also can be transferred to unrelated Windows applications, such as word processors and spreadsheet packages, without interrupting data acquisition and storage. WinDaq/200 is fully compatible with Windows 3.xx and 95 environments, and follows all Windows standards, such as pull-down menus, dialog boxes, context-sensitive help, scroll bars, and error reporting and handling. The WinDaq XY Reviewer simultaneously creates an XY plot of two channels of waveform data being stored to disk with the same engineering units and calibration information. For capturing only transient waveform events, a triggered acquisition mode allows users to specify the number of pre- and post-trigger data points to be stored each time a trigger condition is met.

WinDaq/200 provides four data-acquisition methods per channel. The average method displays and stores a specified group of data points as a single point. The last-point method reports the last input data point of a group of points. The remaining methods report either the highest value data point or the lowest value data point of a group. With multiplexer support, WinDaq/200 can record up to 240 channels simultaneously and display any 32 channels at the same time. The software is compatible with Dataq's DI-500 industrial data-acquisition systems, which provide up to 240 channels at speeds up to 250,000 samples/s. ML

Dataq Instruments, *150 Springside Dr., Suite B220, Akron, OH 44333; (330) 668-1444; fax (330) 666-5434.*
CIRCLE 723

Software Develops Internet/Intranet Applications

Passport IntRprise allows developers to build applications that use Java front ends for Internet/intranet deployment, while supporting a transaction, a multi-tier architecture, and fault tolerance for interprise computing. If a system fails, IntRprise delivers HATP (high-availability transaction processing), which immediately returns the application to pre-failure status. IntRprise provides all of the server-side manageability of a thin-client architecture without the overhead of large script traffic for every change. In two weeks, a programmer with no prior experience in object-oriented, multi-tier Internet applications can be building them successfully. Passport IntRprise supports Windows 3.1, NT and 95, all Unix versions, network computers, and Java. A single developer's license is $8995. ML

Passport Corp., *Mack Centre III, 140 East Ridgewood Ave., Paramus, NJ 07652; (201) 634-1100; fax: (201) 634-0406 or 1-800-926-OPEN; web site: http://www.passport4gl.com.*
CIRCLE 724

Data-Management Software Tests Cable TV Systems

The HP CaLan 85921B data-management software is designed to help cable TV operators identify system performance trends. Running on IBM-compatible PCs, the software provides general reporting and graphical analysis of measurement data acquired within the cable TV system. Measurement results can be stored from HP's CaLan 8591C, 2010B and the entire 3010 family of test instruments.

Manual data entry can be used to combine test results from other brands of test equipment, allowing complete analysis and comparison of data from all test instruments used in the cable system. Test plans can be set up once on a PC and downloaded to multiple test instruments. The cable TV technician can choose which data to analyze: data from one location over time, from all locations on a certain date, or from one instrument.

An optional compliance-reporting feature simplifies semi-annual proof-of-performance reporting. This option allows operators to compare measurement results with compliance specifications and display pass/fail messages for each test. It also provides full reports for the measurement portion of FCC requirements in the U.S.

The HP CaLan 85921B software sells for $650 and has a three-week delivery time. The compliance-reporting option is an additional $300. ML

Hewlett-Packard Co., *Test and Measurement Organization, P.O. Box 50637, Palo Alto, CA 95303-9512; 1-800-452-4844, ext. 2292; Web site: http://www.hp.com.* **CIRCLE 725**

Development Environment Targets Motion Controllers

Motion Workbench software from Warner Electric simplifies the setup and programming of Superior Electric MX2000 motion controllers. The application-specific software allows users to customize the operation of MX2000 motion controllers to meet precise performance requirements. The Windows-based programming tool features icons that are appropriate to programmable motion control, and that represent the controller's most commonly used commands and capabilities. Using the icons, the user draws a flowchart-style representation of the application, instead of writing lines of code in a programming language. Workbench also includes an in-line code icon that provides access to commands too complex to be represented as icons. A free demonstration version with limited functionality is available for download from the Warner BBS at 815-389-6440.

Warner Electric, *Advertising Dept., 449 Gardner St., South Beloit, IL 61080; (815) 389-3771; fax: (815) 389-2582.*
CIRCLE 726

Audio Chip Provides 3D Sound And AC-97 Support

A PCI-based audio processor called the OTI-610 combines support for Microsoft's DirectSound application program interface for 2D and 3D sound. It also supports the Auriel head-related-transfer-function (A3D) 3D positional sound algorithms and the AC-97 audio codec interface. At the heart of the

chip lies a RAM-based digital signal processor, which allows OEMs to easily modify the algorithms and thus support new audio standards as the market evolves. The OTI-610 supports multiple multimedia sound standards, including general MIDI-compliant wavetable synthesis, multichannel digital audio mixing (via Microsoft's DirectSound Direct Input), SoundBlaster Pro emulation (through the Microsoft DirectX environment), the Windows sound system, and the MPU-401 MIDI interface.

Because the chip can co-reside with ISA-bus SoundBlaster hardware, it provides maximum multimedia compatibility. By using the PCI bus as the host interface, data-transfer rates from main memory have enough are fast enough so that designers no longer need a local audio memory, thus simplifying the audio subsystem. With the OTI-610, the audio files can be kept in main memory and pulled in as needed over the PCI bus master interface. The positional 3D sound support allows subsystems to deliver performance over two speakers that emulates the surround-sound over 5+ speakers, like that used in the emerging DVD playback systems. In lots of 25,000 units, the chip, which comes in a 160-lead PQFP, sells for $15 each. Samples are available immediately. DB

***Oak Technology Inc.**, 139 Kifer Ct., Sunnyvale, CA 94086; (408) 737-0888 http://www.oaktech.com.* **CIRCLE 727**

Synchronous SRAMs Let Systems Run At 125 MHz

With a data-transfer rate of up to 125 MHz and a 7-ns initial access time, a pair of high-speed synchronous SRAMs provides designers with 4 Mbits per chip. The memory chips are available in 128-kword-by-36-bit (HM67S26130) and 256-kword-by-8-bit (HM67S18258) organizations and have register-to-latch output modes. Both memories operate from a 3.3-V supply and have low-power LVCMOS-compatible inputs and outputs.

When active, the SRAMs consume 2.7 W, while on standby the power drops to about 333 mW. Byte-write control allows the CPU to write several lines of data at a time, and a self-timed late-write signal simplifies system design by eliminating the need to generate a write-control pulse. Housed in 119-bump BGA packages that occupy an area of just 127 mm^2, the SRAMs were designed with the future in mind—the low package parasitics will allow frequency upgrades to 200 MHz and beyond. Both the HM67S36130 and 67S18258 sell for $200 apiece in 1000-unit quantities, with samples available from stock. DB

***Hitachi America Ltd.**, Semiconductor and IC Div., 2000 Sierra Point Pkwy., MS-080, Brisbane, CA 94005-1819; Brett Etter, (800) 285-1601; Web: http://www.hitachi.com.* **CIRCLE 728**

Monitor Controller Chip Allows Host To Adjust Screen

Digital control of PC CRT color monitors makes it possible for the monitors to be remotely adjusted and would provide simple manual controls. The TDA4885 video-controller chip includes an IIC serial bus that supplies a simple communications path between the host system and the monitor, providing a remote means to adjust the monitor. Internal monitor adjustment signals enable users to control the brightness, contrast, white point, black level, and on-screen display contrast. Automatic gray-scale tracking maintains the correct color balance when the brightness or contrast settings are changed.

The chip supports a pixel rate of 150 MHz and has an output rise time of 2.7 ns. Thus, the signal maintains the sharp picture quality needed for high-resolution displays. The TDA4885 has RGB inputs that accept 0.7-V video signals, and includes all of the necessary blanking, clamping, and clipping circuitry. Chip outputs provide feedback paths for both dc-coupled and ac-coupled CRT cathodes. Housed in a 32-lead skinny DIP, the TDA4885 sells for $1.60 apiece in large quantities. DB

***Philips Semiconductors**, P.O. Box 216, 5600 MD Eindhoven, The Netherlands, (31) 40 272-2091.* **CIRCLE 729**

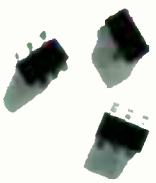
Military-Grade CPUs Now Have New Source

Available in various speeds and ceramic packages, versions of Motorola's 68020, 68040, 68332, and 68360 microprocessors Motorola were recently put through rigorous screening by White Microelectronics to provide military-grade versions. The WC32P020 is their military-grade version of the 68020, and it comes with maximum clock speeds of 16, 20, or 25 MHz and in either a 114-lead ceramic PGA or 132-lead ceramic quad-flat-package. The WC32P040 is the 68040 CPU, which features either 25- or 33-MHz speed grades, comes in either a 179-lead CPGA or a 196-lead CQFP. Operating at 16 MHz, the WC16P332 (the 68332) microcontroller is housesd in a 132-lead CQFP. This chip combines a 32-bit CPU with a system integration module, a time-processing unit, a queued serial module, and 2 kbytes of on-chip SRAM. Targeting data communications, the WC32P360 (the 68360) contains four serial communication controllers that provide a total of seven serial channels. The chip operates at 25 MHz and comes in either a 241-pin CPGA or a 240-lead CQFP. Prices for the chips depend on the level of testing and package. DB

***White Microelectronics**, 4246 E. Wood St., Phoenix, AZ 85040; Philip Farahmand, (602) 437-1520; Web: http://www.whitemicro.com.*

CIRCLE 730

...MORE NEW 3 VOLT RF ICs FOR YOUR HANDHELD WIRELESS PRODUCTS



NEC's 3 Volt ICs not only reduce power consumption in your wireless designs, they help reduce your parts count, improve the reliability, and simplify assembly.

We're committed to 3 Volt Silicon technology. These parts are just a sampling of the wide variety of the semiconductors we stock.

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For product literature, call your nearest CEL Sales Office. Or better yet, call anytime, 24 hours a day:

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7 dB CG @ 1.9 GHz
2.7 to 5.5 V Supply Voltage

UPC2758T
Downconverter
100 MHz – 2.4 GHz
17 dB CG @ 2.0 GHz
+6 dBm IP3

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100 MHz – 1.9 GHz
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Flat Response to 1 GHz RF
DC–100 MHz I/Q Output

UPC2721GR
High Compression Point
Downconverter
900 MHz – 2.0 GHz
21 dB Conversion Gain

UPB1505GR new
Prescaler
÷64/128/256
3 GHz Guaranteed RF Input
High Input Sensitivity

...plus dozens of discrete transistors including three new small signal bipolar series:

new	PART*	NF (dB)	G_A (dB)	V/IC	f_{TEST}(GHz)
	NE68619	1.7	10.0	2V/3mA	2.0
	NE68719	1.5	8.0	1V/3mA	2.0
	NE68819**	1.6	8.0	3V/7mA	2.0

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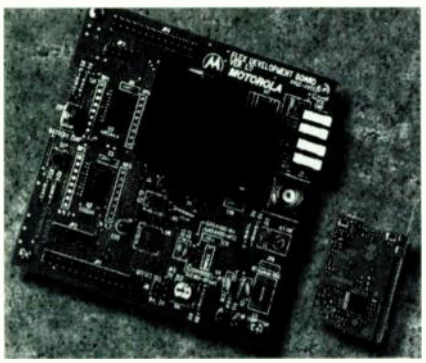
Middleton, MA (508) 762-7400 Hackensack, NJ (201) 487-1155 Snellville, GA (770) 978-4443 Altamonte Springs, FL (407) 774-7682

FLEX-Based Pager Controller Has Powerful Development Set

The 68HC11P8 microcontroller is the first member in a large family of circuits that has been optimized for wireless messaging products using the FLEX protocol. The controller performs most of the logic functions in an alphanumeric pager, including controlling the receiver message formatting and storage, controlling the display, generating the tone or chime, and keeping track of the time.



It's built around a high-performance, low-power, 8-bit 68HC11 CPU core and a host of on-chip features that reduce the parts count and cost of implementing sophisticated alphanumeric paging functions. The processor itself has 48K ROM, 768 bytes of EEPROM, and 2 kbytes of RAM. Its I/O capabilities include two SPI subsystems for communication with the FLEX chip and its displays, as well as two eight- or nine-bit SCI subsystems, one with MI BUS capability. Other I/O features include an on-chip LCD controller; an eight-channel, eight-bit ADC; an interrupt line; and 54 general-purpose I/O and eight input-only lines. Three eight-bit timers, a 16-bit timer, and a four-channel pulse-width module timer also are included.

Rapid development of FLEX-based products using the 68HC11P8 is facilitated by the M68HC11EVS evaluation kit. It's a two-board tool for designing, debugging, and evaluating products using controllers with the 68HC11 architecture. It also can function with the MMDS11, a powerful software development system with in0circuit emulation capabilities.

The 68HC11P8 is available now in 84-pin PCC, 112-pin TQFPs, and 100-pin TQFPs. In 10,000 -piece lots, it costs 10.07, $9.21, and $11.66, respectively. The 69175FDB will become available in the second quarter of this year, and will cost $175. LG

Motorola Microcontroller Information, *P.O. Box 13026, Austin, TX 78711; (800) 765-7795, ext. 986, or (512) 328-2268, ext. 986.* **CIRCLE 731**

ReFLEX Messaging Chip Set Speeds Wireless Designs

The Series 6000 wireless messaging chip set is designed to bring inexpensive two-way messaging capabilities to everything from pagers, laptop, and palmtop computers, to vending machines, traffic lights, and vehicle dispatching systems. Operating in the 900-MHz band, the three-chip set uses the ReFLEX two-way alphanumeric paging protocol and a library of software APIs to create an antenna-to-user interface solution that greatly reduces the amount of RF engineering required to implement a design.

The WR6010 is a bipolar IC that converts 900-MHz signals to an intermediate frequency in the receiver, and creates high-power RF signals for the transmitter. The WM6040 takes the IF signal, demodulates it, and creates individual subchannel data streams to accommodate the ReFLEX protocol. In the transmit mode, the WM6040 provides modulation data to the synthesizer for transmission.

The WB6050 decodes the demodulated digital data stream in the receiver and implements the elements of the ReFLEX protocol. In transmit mode, the WB6050 creates data frames for transmission, and performs power-management functions for the entire chip set. Sampling now and in full production during the third quarter of this year, the Series 6000 chip set will cost $75 each, when purchased in lots of 1000. LG

Wireless Access Inc., *2010 Tasmin Dr. Santa Clara, CA 95054; (408) 653-1555; fax (408) 653-1543.* **CIRCLE 732**

Dual-Mode Wireless Modem Has A Six-Mile Range

Operating in the 900-MHz ISM band, the Hopper FD wireless modem can use either frequency-hopping or direct-sequence modulation to carry wireless data over clear line-of-sight distances spanning six miles. It's a plug-and-play device that operates much like a conventional modem, supporting full-duplex data rates of up to 19.2 kbits/s and 38.4 kbits/s in half-duplex mode. The modem offers a built-in menu system for configuration functions, and an "AT-like" command set .

Users can reprogram the Hopper FD from direct-sequence to frequency-hopping operation in less than a minute using any common terminal emulation program. Available now, the Hopper FD costs $1495 each in single units, with substantial discounts for volume purchases. LG

Wi-LAN Inc., *300-801 Manning Rd. NE, Calgary, Alberta, Canada T2E 8J5; (403) 273-9133; fax (403) 273-5100; e-mail: wi-lan@wi-lan.com; Internet: www.wilan.com.* **CIRCLE 733**

FH Wireless Modem Supports 255 Nodes For Embedded Apps

Operating in the 2.4-GHz ISM band, the WIT2400M frequency-hopping wireless modem provides low-cost, full-duplex, medium-speed, wireless data connections for applications using up to 255 nodes in a particular location. Designed for monitoring and control applications as well as wireless terminals, it can support data rates of up to 115 kbits/ s in either direction. Its 100 mW output gives it a typical range of of 500 to1000 feet indoors, and over a half-mile in line-of-sight outdoors. For limited-range applications, 10-mW output power can be selected. The 82-frequency-hopping sequence employed by the modem makes it resistant to channel fading and multipath effects.

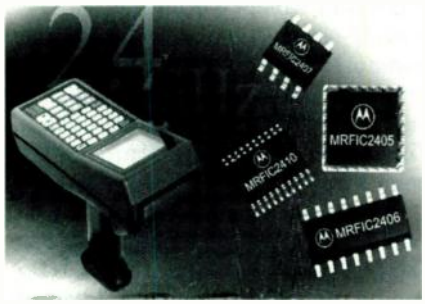
In a network of two or more units, one is configured as a base station/network controller that can perform point-to-point or multipoint communications with the other nodes. Its simple automatic repeat request (ARQ) protocol ensures error-free data transmission. The compact 2.4-by-2.9-by-0.6 module accepts either synchronous or asynchronous data interfaces.

Priced at $360 each in 1000-piece lots, the WIT24000 is available now. A ready-to-run evaluation kit/base station also is available for $850. LG

Digital Wireless Corp., *One Mecca Way, Norcross, GA 30093; (770) 564-5540, fax (770) 564-5541; e-mail: mktg@digwrls.com.* **CIRCLE 734**

2.4-GHz RF Chip Set For FH And DS Wireless Data Apps

A new four-chip, 2.4-GHz RF front end is able to lower the cost, size, and power consumption of ISM-based wireless data systems. Consisting of the MRIFC2405 transconverter, the MRIFC2406 active up-mixer, the



MRIFC2407 exciter amplifier, and the MRIFC2410 two-stage power amplifier, the chip set can be used for both direct-sequence and frequency-hopping spread-spectrum transmission systems. All parts are fabricated using a self-aligned MESFET GaAs process.

The MRIFC2405 transconverter integrates a two-stage power amplifier, LNA, downmixer, antenna diversity switch, and transmit/receive switch. While designed for 3-V operation, the PA can be run at 5 V for higher-power (23 dBm) operation. The MRIFC2406 active upmixer is designed to provide IF upconversion for RF signals in the 2-3-GHz range, and add 6 dB of gain. It has internal active Baluns, eliminating the requirement for off-chip matching components.

The MRIFC2407 is a two-stage, class-A amplifier, with a typical gain of 17 dB. It's designed to drive the power amplifier in the MRIFC2405 and has a 1-dB compression point of 5 dBm. Finally, the MRIFC2410 is a 2.4-GHz MESFET power amplifier that's capable of 30 dBm (1 W) output power at saturation.

All of these components except the MRFIC2410 are optimized for 2.4-GHz wireless LANs, but can be used across the 2-3 GHz band for MMDS wireless cable and other ISM band applications. All parts are housed in inexpensive plastic packages. In10,000-piece quantities, the MRFC2405 costs $7.40 each, the NMRFC2406 is priced at $3.35; the MRFC 2407 goes for $2.10; and the MRFC2410 is priced at $6.50. LG

Motorola Semiconductor, Products Sector, EL 710, 2100 E. Elliott Rd., Tempe, AZ 85008; attn: Mikle Civello, (602) 413-3593; fax (602) 244-4597; RVCB60@email.sps.mot.com.
CIRCLE 735

Integrated IR Transceivers Handle Up To 4 Mbits/s

Incorporating infrared data transmission into your next design may get easier thanks to the TFDT4000 and TFDT6000 IrDA-compatible data transceivers. Both units come in an extremely compact, surface-mounted, "top view" package, measuring only 13 mm wide by 7.5 mm wide. They also both contain the detector, emitter, and all of the analog circuitry necessary for an optimized infrared data association (IrDA) standard-based implementation. This includes an amplifier, comparator, received data line driver, AGC logic, and an open collector transmitter driver. Side-view versions of both devices also are available.

The TFDT6000 is a multimode integrated transceiver that can perform bidirectional data transmission at speeds of up to 4 Mbits/s. While intended to support IrDA-compatible systems, it also works with the HP-SIR and Sharp ASK standards. Intended for lowest-cost applications where speed is less critical, the TFDT4000 supports only the IrDA standard with a transmission rate of up to 115 kbits/s. If higher power is desired for transmission beyond the three-meter range specified by IrDA, the TFDT4000 transceiver allows its internal IRED driver to be connected to an independent unregulated power supply.

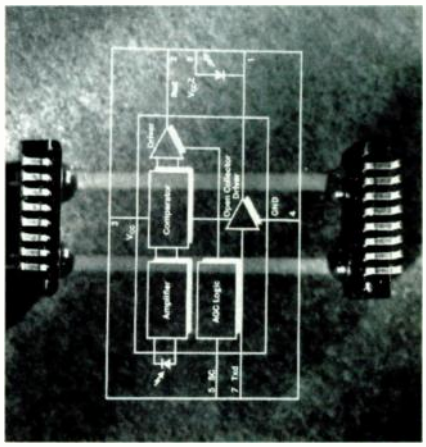
Available now, high-volume orders (100,000 pieces or more) of the TFDT4000 will cost $2.75, and $4.50 for the TFDT6000. LG

Temic Semiconductors Inc., 2201 Laurelwood Rd., Santa Clara, CA 95054-1595; (800) 554-5565, ext. 31; (408) 567-8220, ext. 31; fax (408) 567-8995. **CIRCLE 736**

FLEX Chip Set Simplifies Embedded Paging, Messaging

The TMS320FLEX1, targeted at alphanumeric pagers and other embedded wireless messaging applications, is a DSP-based chip set. It implements the FLEX paging protocol and interfaces easily with most major microcontrollers.

The simple controller interface makes it easy for designers involved in developing new products or upgrading older ones to the advanced FLEX protocol. Only a receiver and microcontroller are required to complete a low-power, compact messaging system that can be embedded in notebook and desktop PCs, PDAs, smart home electronics, and automobiles. The chip set supports FLEX's alphanumeric messaging at 1.6, 3.2,



and 6.4 kbit/s transmission rates, as well as group paging.

The chip set consists of the TLV5591B FLEX protocol decoder, a signal processor that decodes the incoming transmission, and the TLV5590 ADC, which converts the receiver's analog signal to a digital format for decoding by the TLV5591B.

The final part of the solution is the FLEXstack software, which was designed by Motorola to facilitate rapid product development. Running on the system processor, it is an operating kernel that handles inter-chip communications and interprets host commands for the TLV5591B. FLEXstack is available via Motorola's Web site at: www.mot.com/FLEXstack. The TLV5590 and TLV5591B are offered as a set, costing $8.30 in quantities of 100,000. LG

Texas Instruments Inc., Semiconductor Group, SC-96070A, Literature Response Center, P.O. Box 172228, Denver, CO 80217; (800) 477-8924, ext. 4500. **CIRCLE 737**

Chip Set Handles All Analog And Digital Functions For DAB

A German semiconductor manufacturer has come up with a complete chip set that takes care of all analog and digital functions involved with digital audio broadcast (DAB). A DAB receiver consists of the analog functional blocks of an L-band downconverter and an RF front end, as well as the digital functional blocks of the channel decoder and the source decoder. The single-chip L-band downconverter U2730B integrates the amplifier, mixer, VCO and phase-locked loop.

The RF front end consists of three ICs: the U2750B integrates a front-end mixer, an oscillator, and an automatic gain control (AGC). The U2759B device is responsible for the IF processing, while the U2733B is a PLL circuit with an integrated frequency doubler and two DACs for the automatic adjustment. The channel decoder consists of two devices: the U2757M and the U2758M. The U2757 is responsible for the FFT, including digital AFC (automatic frequency control) and AGC functions and rough-time synchronization. The U2758 contains the de-interleaver, Viterbi decoding functions, and data processing.

DAB offers high-quality audio as well as the possibility to transmit additional visual information with a data rate high enough to send an entire daily newspaper within a few seconds. AV

Temic Telefunken Microelectronic GmbH, *P. O. Box 35 35, 74025, Heilbronn, Germany; phone +49-71 31/67-29 45, fax +49-71 31/99 33 42.* **CIRCLE 610**

First Two Chips Of Family Debut, Target Low-Cost Ethernet Apps

The first two devices of a new family of products optimized for so-called "low-cost" fast Ethernet NICs, hubs, repeaters and switch applications have been launched with the NWK914 and NWK935 Ethernet PHY products. The NWK914 integrates the 100Base-Tx transceiver, clock, data-recovery, and NRZI conversion functions. It's capable of operating up to 150 meters of STP (shielded twisted pair) and Category 5 UTP (unshielded twisted pair) cable. According to the chip manufacturer the NWK914 achieves a power savings "of up to 50 % compared with existing production solutions." The NWK914 provides a 5-bit symbol interface to media access controllers (MACs) incorporating the PCS layer, such as the 21143 and the MX98713.

The other new device, the NWK935, integrates the 100Base-Tx Physical Coded Sublayer (PCS) functions. It supports both full- and half-duplex operations, and fully satisfies the IEEE 802.3 specification. When combined, this chip-set solution performs all functions ranging from magnetics to MII for use in hubs and repeaters. When used with a MAC controller like the 21140A or the 82557, it's also usable for NICs. Reference designs are available. The NWK914 comes in a 52-pin PLCC package, and the NWK935 is housed in a PLCC with 64 pins. AV

GEC Plessey Semiconductors, *Cheney Manor, Swindon, Wiltshire, SN2 2QW, Great Britain; phone: +44 1793 518 128; fax: +44 1793 518 481.* **CIRCLE 611**

Surface-Mount SAW Resonators For Radio Remote Controls

Surface-acoustic-wave (SAW) resonators are key components in radio remote controls because they help stabilize frequency in the transmitter and receiver. Typical applications include all telecontrols, from the classic remote control to data-transmission systems in the UHF band. Further application possibilities are cordless headphones, remote controls for TV/SAT and video recorders, security systems, garage door openers, and data transmission within automobiles. SAW resonators also can be found in new tuner designs for digital television in satellite receivers. Now these SAW resonators (single-port and two port) and resonator filters are available in SMD packages for all internationally allocated frequencies in these kinds of systems. For receiver designs with conventional IC sets, there are resonators with 10.7-MHz and 500-kHz offset from the transmission frequencies. Call for more information. AV

Siemens Matsushita Components, *P. O. Box 2348, 90713 Fuerth, Germany; fax: +49 911 978-3321.* **CIRCLE 612**

Hall-Effect Sensors Feature Direction-Detection Function

A new family of direction-detection Hall-effect sensor ICs was designed for the contactless sensing of direction and speed. The A3420/ 3421/ 3422 devices each are based on two Hall latches, with the Hall elements spaced 1.5 mm apart. Each latch is independently actuated by the ambient magnetic field to produce high or low digital outputs. These are fed to a logic circuit to obtain the directional output signal. An internal voltage regulator power both the analog and digital circuitry. The regulator senses the load current and controls a variable current source, which helps to maintain a constant current The A3420 is a high-hysteresis device that allows for current signaling of its information. The A3421 and A3422 are standard open-collector devices that communicate through voltage levels. All of the devices come in the standard five-lead KA package. RE

Allegro Microsystems Inc., *Balfour House, Churchfield Rd., Walton-on-Thomas, Surrey, KT12 2TD, England; phone: (44-1932) 253-355; fax: (44-1932) 246-622.*

CIRCLE 613

Edited By Roger Engelke

SP70XX Dc-Dc Converters Hit The Right App Note

A new application note titled "SP70XX Series DC/DC Converters Power High Performance A/D Converters from a Single +5V Supply" outlines design solutions for many high-performance data-conversion applications. Discussions include ADC power requirements, PSRR versus noise requirements, +5-V requirements, isolation needs, bypassing, chopper synchronization, and temperature limitations. The SP70XX family powers 14- and 16-bit ADCs from a single +5-V supply while providing low noise-plus-ripple performance of 5 mV p-p. For a free copy of the application note, contact Analogic Corp., Peabody, Mass., at (800) 446-8936; fax (617) 245-1274. Or you can e-mail to: dcpinfo@analogic.com. *RE*

CIRCLE 600

Repair Capabilities Manual Gets A Fix On Products

Over 34,000 different products from more than 2000 manufacturers of circuit boards and electronic controls that can be repaired or retrofitted by Galco Industrial Electronics' repair division are listed in the company's new *Repair Capabilities Manual*. Rundowns of instrument calibration capabilities that are traceable to NIST standards, as well as available remanufactured controls to assist customers in "down" situations, are provided. Repair capabilities include ac and dc variable-speed drives, counters and timers, CNC controls, encoder devices, pc boards, temperature controllers, and an assortment of other products. Call (800) 521-1615 for a copy. *RE*

CIRCLE 601

The Latest "Wrap" On Zip-On Jacketing/Shielding

Zippertubing, a product that protects wire, cable, tubing, and other lines, is covered in a new 32-page catalog produced by Zippertubing Co., Los Angeles, Calif. The material essentially is a wraparound, repairable, re-enterable, flexible jacket that features a zipper closure, which avoids having to pull through tubing or disconnect cables. If offers EMI shielding and abrasion resistance, and resists chemicals. Specs, photos, descriptions, etc. are included for the line of jackets, shields, closures, and so on. Call (800) 321-3178; fax (310) 767-1714. *RE*

CIRCLE 602

Industry's First "Magalog" Talks DSP Tools

DSP Connection apparently is the electronics industry's first ever combination magazine and catalog, or "magalog." Available from White Mountain DSP, Nashua, N.H., the bi-annual publication offers detailed descriptions of the company's products as well as app notes, contributed articles from the digital-signal-processing community, and other features. DSP third parties such as Ariel, GO DSP, Ixthos, and Pentek, as well as DSP silicon provides like Analog Devices and Texas Instruments, contributed to the publication. Future plans include more expansion for the company's numerous partners, and an international edition. For a copy, e-mail your mailing address to: connection@wmdsp.com. *RE*

CIRCLE 603

Get Your Handle On The New Citizens-Band Catalog

Complete product lines for both mobile and base-station antennas, including a recently consolidated monitor line, are showcased in the 14-page catalog *CB & Scanner Antennas*. The mobile antenna line offers various mounting options, such as "On Glass," magnet, trunk, lid, roof, side body or gutter. Two notable base-station antennas are the AV-140 Moonraker 4 dual-element and the AV-122 PDL II patented dual-polarity beam. Both have very broad bandwidth for low 1.3:1 VSWR across all 40 channels. For a free copy of the catalog, call (216) 349-8687; fax (800) 321-9978. Reference catalog CB-1004 when ordering. *RE*

CIRCLE 604

Catalog Steers In Direction Of Automotive Relays

Automotive relays are the basis of a free 40-page catalog from Siemens Electromechanical Components Inc., Princeton, Ind. Specifications are detailed for relays and modules designed specifically for automotive applications. The catalog include listings for plug-in, bracket-mount, and pc-board-mount relays. Maximum contact ratings range from 10 to 70 A. Both open-frame and enclosed models are described. Basic product information in the selector guide section helps readers determine which product series is best suited for a particular application. There's also a group of pages that list the detailed technical specifications for those series. For a copy of the catalog, contact the company through fax (821) 386-2072, or e-mail at info@ae.sec.siemens.com. *RE*

CIRCLE 605

Tact-Switch Selection Guide Makes Contact With Readers

A new four-page tact-switch selection guide helps users find the tactile or key switch that best suits their requirements. Put out by EAO Switch Corp., Milford, Conn., the guide includes a wide range of tact switches designed for communications equipment, consumer electronics, computer applications, and industrial control. Through-hole, right-angle, surface-mount, and washable models are discussed. There's a photograph of each switch plus features and specs. Soldering, sealing, and accessory actuator caps are detailed. To obtain the free guide, contact EAO Switch at (203) 877-4577; fax (203) 877-3694; e-mail: info@eaoswitch.com. *RE*

CIRCLE 606

Application Notes Published For Board-Level Switcher

Originally designed for handheld pagers, Augat Inc.'s (Attleboro Fall, Mass.) SPS121151RG is meant for board-level switching in tight spaces. Now there are application notes available to illustrate various approaches to particular board-level interconnection needs. The right angle, telecom-grade slide switch allows two-position side-to-side actuation, as well as a third position, when the actuator is depressed. Call Augat Customer Service at (508) 699-7646 for samples and data sheets (reference application note #103). *RE*

CIRCLE 607

■ To strengthen its partnerships with signal-conditioning and data-acquisition, **Analog Devices,** Norwood, Mass., has changed its sales strategy for these products to no longer include industrial distributors in North America. This includes signal-conditioning modules like the 5B series, data-acquisition boards like the RTI-800 series, and associated software like the SW-800. All orders for such products will now be handled by the current U.S. network of manufacturers representatives, as well as Analog Devices' own sales and customer service representatives. Distributors will still be used outside North America. The decision comes on the heels of the recent merging of the former Iomation Product Group into Analog Devices' Transportation and Industrial Products Div.

■ New England regional distributor **Coghlin Electric/Electronics,** Westboro, Mass., has been awarded franchises to sell products for Eaton Commercial Controls Div. and Fujitsu Takamisawa America (FTA). The franchises include Eaton Commercial Controls' entire switch line and FTA's relays, connectors, keyboard/input devices, and thermal printers. Coghlin is an ISO 9002-registered single-source supplier of electrical and electronic components servicing the New England region. It's also a founding member of the iPower Distribution Group, an integrated supply consortium of 15 distributors, each with different distributor strengths.

■ E-T-A, Altdorf, Germany, has chosen **Sager Electronics,** Hingham, Mass., to nationally distribute its line of circuit breakers for electrical and electronic equipment. E-T-A's products serve the transportation, telecommunications, and medical industries. Sager will maintain an in-depth inventory of E-T-A's circuit breakers in its advanced distribution center, enabling quick response times and just-in-time delivery.

■ A form for on-line ordering of parts from **Digi-Key Corp.,** Thief River Falls, Minn., can now be used by purchasers via the company's web site at *http:/www.digikey.com.* The form enables those purchasing parts from the nationwide distributor to instantly build and submit an order, on-line, or over a period of hours, days, weeks, or even months. Customers can now perform a part-number or key-word search, access current pricing and availability information, obtain technical information by downloading Digi-Key's catalog pages or by linking directly with the parts manufacturers, and place an order, all on-line.

■ **Insight Electronics,** San Diego, Calif., North America's fifth largest semiconductor distributor, and Synplicity Inc., Mountain View, Calif., have announced a joint distribution agreement to promote a Xilinx-specific version of Synplicity's FGPGA design software—Synplify. Insight is the first U.S. distributor to offer third-party tools , complete with software, hardware, and technical support, separate from those provided by the FPGA suppliers it represents. Specifically, Insight will offer Xilinx's FPGA technology, Xilinx-specific VHDL or Verilog Synthesis languages from Synplicity, and sales and technical support through its staff of technical sales engineers. Insight will conduct intense VHDL training for its technical sales engineers and will hold external VHDL classes for its customers.

■ **Wes-Garde Components Group Inc.,** Hartford, Conn., a leading distributor of electro-mechanical products and services, has signed a franchise agreement with Weidmuller Inc., Richmond, Va. In place from the beginning of this year, the agreement calls for Wes-Garde to distribute Weidmuller's complete product line of connectors, terminal blocks, and interface modules at all of Wes-Garde's distribution facilities in the U.S. Weidmuller's products and services serve the automotive, marine, medical, telecommunications, food equipment, and industrial equipment industries.

■ **MFS (U.K.) Ltd,** headquartered in Shelton, near Coventry, Warwickshire, England, has been given exclusive distribution rights in the United Kingdom and Ireland to distribute products from Dexter Electronic Materials, Londonderry, N.H. The agreement allows MFS to distribute Dexter's full range of high-performance fluxes and oils for leveling and fusing, screen cleaners, waste treatment, solder strippers, etchants, plating resists, etch resists, and one- and two-component inks for substrates. In addition, MFS will become an agent of Dexter with responsibility for commercial sales of Advanced Chemill Systems' (ACS') wet process equipment to circuit board manufacturers in the U.K. and Ireland.

■ Programmable logic devices made by Advanced Micro Devices (AMD) are being programmed for customers by **Hamilton Hallmark,** Culver City, Calif. AMD also is changing the name of its PLD division to Vantis but users will get the same products with the same part numbers manufactured at the same AMD facility, so there will be no need to requalify parts. The distributor maintains advanced automation equipment to program the PLDs with a 3-day turnaround time and a capacity of over 4 million devices per month. Users also can get technical support and programming services from the distributor.

■ A new, full-color newsletter called "The Source" will be published 6 times a year by **GC Electronics,** Rockford, Ill. In addition to information on the distributor's electronic products and accessories, the publication will feature stories about customer successes. The aim of the newsletter is to provide distributors of electrical and electronic parts with ideas of how to broaden their product lines and increase profits. The company hopes to open a dialogue with its customers through the newsletter to understand and adapt to the changing components market.

■ Comprehensive information on all chargeable and non-rechargeable battery chemistries is available in a new 72-page catalog from the **House of Batteries,** Huntington Beach, Calif. The publication contains technical and applications data as well as extensive cross-reference information for all major battery aftermarkets. The catalog is intended for engineering and purchasing personnel who need unique types of information to effectively specify and order batteries. The distributor carries an inventory of over 50,000 batteries and is a value-added reseller (VAR) for major battery manufacturers such as Duracell, Sanyo, Yuasa/Exide, Saft, Varta, Bolder Technologies, GP, Powersonic, and Maxell.

Securing Your Financial Future Means More Than Just Earning A High Salary

Tom Ajluni

It used to be that engineers were a dime a dozen. Nowadays, finding skilled engineers in the high-tech arena is a difficult task. Getting them to stay at a company for any extended period of time is next to impossible. Today, the average engineer jumps from one company to the next roughly every two years, enticed by significant salary increases and annual performance bonuses. Even large sign-on bonuses are becoming the norm as opposed to the exception. But, if engineers don't participate in the 401 (k) programs offered by each of their employers, they could be sabotaging their financial future and, ultimately, their retirement security.

Most people fundamentally understand the need to save for the future. After all is there anyone who doesn't question, just the slightest bit, whether the Social Security tax you pay now will be available as a resource by the time you are actually old enough to collect it? But understanding the need to save and actually doing it are two totally different things.

What many fail to understand is that every dollar invested today bears a direct correlation to the quality of life after retirement. For the average engineer, who having understood the rewards of hard work and a little early educational planning is now basking financially in the fruits of these labors, this concept should not be a stretch. Committing oneself to this goal of long-term planning now and sticking to it over the years is the key to ensuring financial security after retirement.

There are a number of ways to prepare for retirement. One method, the 401 (k) program, offers advantages that, compared to traditional pension plans, can result in a bigger nest egg at retirement.

The 401 (k) program was originally established as a long-term retirement plan by the government to help people save for retirement. It allows participants to set aside money from their paychecks for deposit into a special account set up by the employer. Special tax advantages make the plan especially appealing since all contributions are made on a pre-tax basis. The net effect is that the participant's taxable income is reduced.

How It Works

Employer's are not required by law to offer a 401(k) program. But when they do, it's an offer that shouldn't be refused. Here's how it works:

A participant first decides the amount of money to be contributed to the plan during each pay period, up to a predetermined maximum. Next, the participant chooses, from among the company's investment fund options, where the money is to be invested. The options typically include a number of mutual funds managed by professional money managers as well as company stock. An employee can obtain details regarding the fund options' past performance, and information about the company's own stock by contacting its Human Resources department. This is recommended prior to deciding how to invest the money.

Once plan contributions begin, periodic statements are sent to the participant throughout the year to help track investment progress. To get the most out of the plan, participants should contribute the maximum amount and leave it in as long as possible so that its earnings can grow tax-deferred. All contributions and growth earnings remain tax-free until the money is withdrawn, either during retirement or in case of an emergency.

Many engineers, as well as the general public at large, fail to take advantage of 401 (k) programs because either they don't think they need to or don't think they can afford to. The standard rule of thumb is that each individual needs at least 70% of their pre-retirement income to maintain their current standard of living in retirement. That means that for the typical engineer bringing home a salary of $80,000 a year, a retirement income of at least $56,000 is needed just to live comfortably. And even this may not be enough in these inflationary times. 401 (k) investments can provide one of the easiest solutions to this retirement "cash crunch."

Those concerned that 401 (k) participation will put too large of a dent in their pocketbooks are often surprised to discover that deductions will not affect their take-home pay as much as they previously thought *(see "How*

COMPARING TAX-DEFERRED AND TAXED ACCOUNTS

Contribution	Tax-deferred account	Taxed account
Gross amount contributed by plan participant	$50.00	$50.00
Federal income taxes paid on gross contribution (28% tax rate)	$0	$14.00
Actual monthly contribution	$50.00	$36.00
Account balance after 10 years	$9,208.00	$5,870.00
Account balance after 30 years	$75,015.00	$35,096.00

This table is for the purposes of illustration only. It assumes an 8% return, compounded monthly. With a tax-deferred account, contributions and earnings are taxed upon withdrawal of funds from the plan. With a taxed account, on the other hand, contributions are taxed monthly and earnings are reduced annually.

Deductions Affect Take-Home Pay"). The advantages of pre-tax deductions outweigh what's lost in income each pay period. By starting off with a small contribution, the participant can slowly increase contributions over time until their comfort level grows that they won't find themselves strapped for cash.

Participation Advantages

The rewards of 401 (k) participation, whether short- or long-term, are substantial. Automatic contribution makes investing easy and means that the money is deducted before the participant has a chance to spend or even miss it. And, with most employers offering to match employee contributions, the participant gets paid just for putting money into the plan. On average, most employers match contributions $0.50 on the dollar.

Because plan contributions are made on a pre-tax basis, the participant's taxable income is reduced, which in turn results in lower federal taxes, and in some cases, state income taxes. Tax-deferred income taxes are not paid on the contributions, or growth earnings, until the money is withdrawn from the plan

. With the money in the plan growing tax-deferred, assuming it remains invested for a significant amount of time and that it earns a decent rate of return, it is possible for the participant to witness impressive account growth *(see Table 2)*. In fact, the participant is able to accumulate more money than if the same amount of money was stashed away in a taxable account.

The 401 (k) program is very flexible, offering a number of investment options to choose from. Depending on the participant's future goals and objectives, the contributed plan money can either be placed in a conservative and relatively low-risk investment fund, or in an aggressive one that takes more risks, yet has the potential for higher gains. Once participants decide how much and where the money is to be invested, they are not locked into these choices, and are free to make changes to the investment mix as their needs and retirement goals change.

One factor that causes people to shy away from a 401(k) plan participation is the feeling that once they contribute, they will never see their money again until retirement. This could not be more further from the truth. While not necessarily recommended, the money is accessible to the participant, and can be withdrawn in case of a financial hardship or through loan provisions. Situations that would qualify as a hardship withdrawal include a medical emergency, college tuition, or a down payment on a primary residence. There may be federal and state tax penalties on hardship withdrawals for early distribution (withdrawals) of plan contributions.

Employer's are not required by law to offer a 401(k) program. But when they do, it's an offer that shouldn't be refused.

In today's dynamic workplace environment, as engineers move from one company to the next in pursuit of better employment and financial opportunities, some may wonder whether or not it's even worth investing in their employer's 401(k) program. The answer is an emphatic "yes."

An employee contributing to a company's 401 (k) plan who terminates employment has three options: The investments can be left where they are to continue growing; they can be distributed to the employee in one lump sum (in which case there will be a 20% federal tax withholding under the Internal Revenue Service (IRS) rules and an optional state withholding at a rate of 10%); or, if the new employer allows, the account can be rolled over. As long as the money is rolled over into another qualified plan or individual retirement account (IRA), it will remain in a tax-deferred status. Regardless of which option is chosen, the contributed money and any associated earnings still belong to the employee.

401 (k) Means Security

For many people, a salary increase automatically means a standard of living increase. With the amount of hours and hard work engineers and other professional now invest in their ca-

How Deductions Affect Take-home Pay

Here's an example of how various payroll deductions from an employee's theoretical salary can affect take-home pay:

- Salary: $35,000 per year.
- Annual tax (assuming a 28% tax bracket): $9800
- Plan investment: $3500 or 10%.
- Taxable income: $35,000.
- Reduced taxable income due to plan investment: $31,500 ($35,000-$3500).
- Annual tax (assuming plan investment of 10%): $8820 ($31,500 × 28% tax rate).
- Tax-bill savings: $980 ($9800-$8820).
- Consequences of employee investment: While the initial investment costs the employee a total of $3500, when the savings from the tax bill is factored in, the net cost to invest for the employee is only $2520. Assuming the employee's monthly take-home pay was originally $2100, a 10% plan investment would only mean a reduction in take-home pay of $210. The employee's new take-home pay would be $1890. Each month, though, the employee waves a

reers, it's easy to understand why "living the good life" beyond the workplace is such a high priority. The problem is that the old saying "work hard, play hard" doesn't always hold true. While engineers are a hot commodity today, demanding and receiving higher pay, this trend is no more stable than the fluctuating interest rate. Job security and job loyalty are certainly not what they were 20 years ago. And, in fact, in today's economic climate, most people don't expect to work for just one company for the rest of their lives.

With no guaranteed security on the job front, it is even more crucial that today's engineer start to secure a financial future. This is the only way to ensure that come retirement time, the enjoyment does not stop. And, although some would argue that they can't afford to invest in their future, what they really ought to be thinking about is how they can afford not to invest.

The bottom line is that while 401 (k) participation does not guarantee membership to the exclusive millionaires' club, the accumulation of funds that it allows for can provide a substantial nest egg not possible by simply making more money and plunking it into a savings account. Financial security during retirement means preparation and a little hard work today. Engineers must make a conscious decision to not only enjoy life now, but also have a plan so they can continue that enjoyment well into retirement. This means setting a financial goal and working toward it, and making smart choices about what to do with the money they make. Participation in an employer's 401 (k) program is definitely a smart move.

Tom Ajluni is a Senior Human Resources Professional for Samsung Electronics. He has a degree from San Jose State University in Labor Economics with a minor in Human Resource Management, and specializes in the management and implementation of 401 (k) programs.

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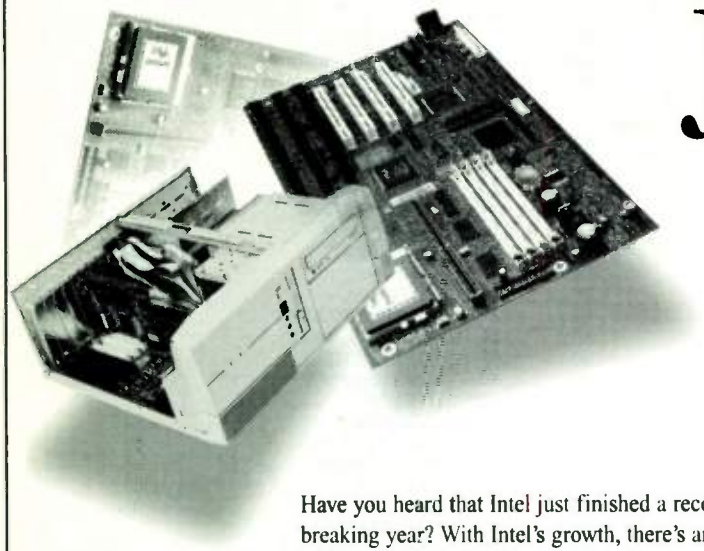

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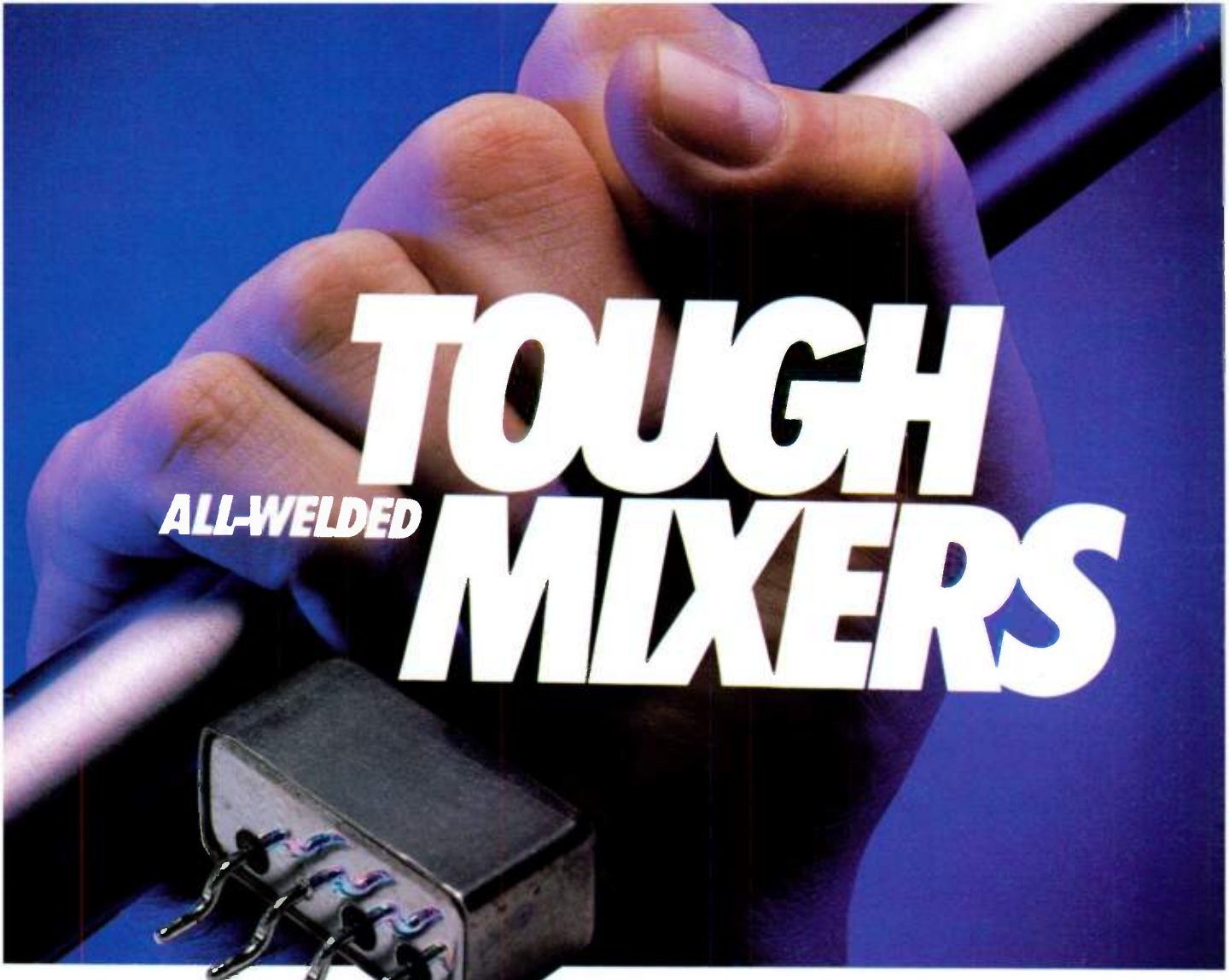

SURFACE-MOUNT or PLUG-IN

FROM **$3.95** (10 qty)

Expose Mini-Circuits' TUF-mixers to 250°C for five minutes, or to the extreme shock and vibration stresses of MIL-M-28837, or to 200 cycles of thermal shock from -55° to +100°C...they'll survive without any change in specs. They are mighty tough mixers!

Available with LO drive levels from +7 to +17dBm, performance features include very low conversion loss flat over the entire band, high isolation (L-R, L-I), and well-matched VSWR at all ports.

All-welded internal and external construction is used to assemble and package the TUF-unit in its tiny 0.5 by 0.2 by 0.25 in. metal case, for plug-in or surface-mount* assembly.

TUF-Ultra-Rel™ mixers are guaranteed for five years and boast unprecedented "skinny" sigma (δ) unit-to-unit repeatability as shown in the Table.

Tough, tiny, and with tight repeatability...Mini-Circuits' Ultra-Rel™ TUF-mixers with a five-year guarantee, priced from $3.95...available only from Mini-Circuits.

actual size

ULTRA-REL™ MIXERS

5-YR. GUARANTEE

with extra long life due to unique HP monolithic diode construction, 300°C high temp. storage, 1000 cycles thermal shock, vibration, acceleration, and mechanical shock exceeding MIL requirements.

SPECIFICATIONS

Model	LO Power (dBm)	Freq. LO/RF (MHz)	■ Conv. Loss (dB) $\bar{X}$	■ Conv. Loss (dB) δ	Isol. L-R (dB)	Price,$ Ea. 10 qty
TUF-3	7	0.15-400	4.98	0.34	46	5.95
TUF-3LH	10		4.8	0.37	51	7.95
TUF-3MH	13		5.0	0.33	46	8.95
TUF-3H	17		5.0	0.33	50	10.95
TUF-1	7	2-600	5.82	0.19	42	3.95
TUF-1LH	10		6.0	0.17	50	5.95
TUF-1MH	13		6.3	0.12	50	6.95
TUF-1H	17		5.9	0.18	50	8.95
TUF-2	7	50-1000	5.73	0.30	47	4.95
TUF-2LH	10		5.2	0.3	44	6.95
TUF-2MH	13		6.0	0.25	47	7.95
TUF-2H	17		6.2	0.22	47	9.95
TUF-5	7	20-1500	6.58	0.40	42	8.95
TUF-5LH	10		6.9	0.27	42	10.95
TUF-5MH	13		7.0	0.25	41	11.95
TUF-5H	17		7.5	0.17	50	13.95
TUF-860	7	860-1050	6.2	0.37	35	8.95
TUF-860LH	10		6.3	0.27	35	10.95
TUF-860MH	13		6.8	0.32	35	11.95
TUF-860H	17		6.8	0.31	38	13.95
TUF-11A	7	1400-1900	6.83	0.30	33	14.95
TUF-11ALH	10		7.0	0.20	36	16.95
TUF-11AMH	13		7.4	0.20	33	17.95
TUF-11AH	17		7.3	0.28	35	19.95

*To specify surface-mount models, add SM after P/N shown.

■ $\bar{X}$ = Average conversion loss at upper end of midband ($f_U/2$)
δ = Sigma or standard deviation

Mini-Circuits®

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CIRCLE READER SERVICE CARD

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For detailed specs on all Mini-Circuits products refer to • 740- pg. HANDBOOK • INTERNET • THOMAS REGISTER • MICROWAVE PRODUCT DATA DIRECTORY • EEM

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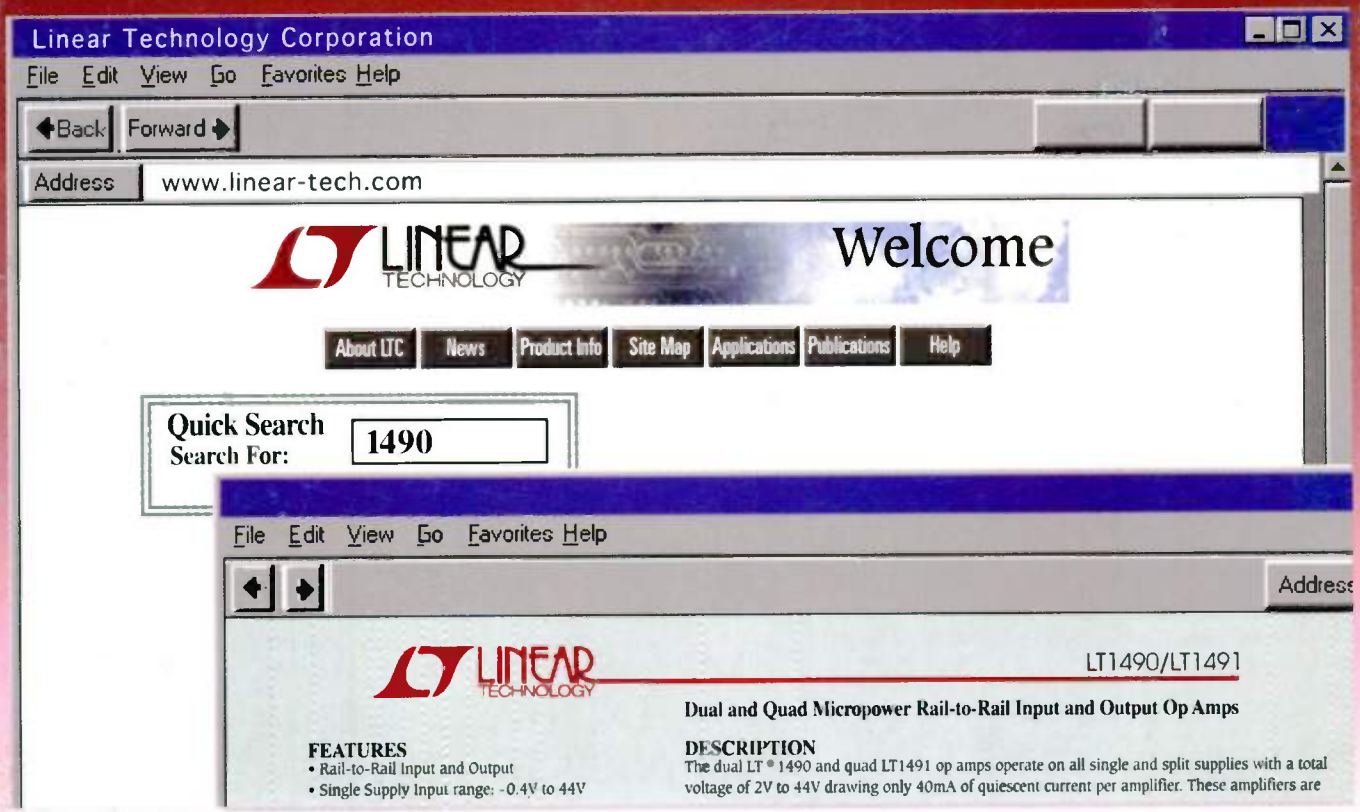

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