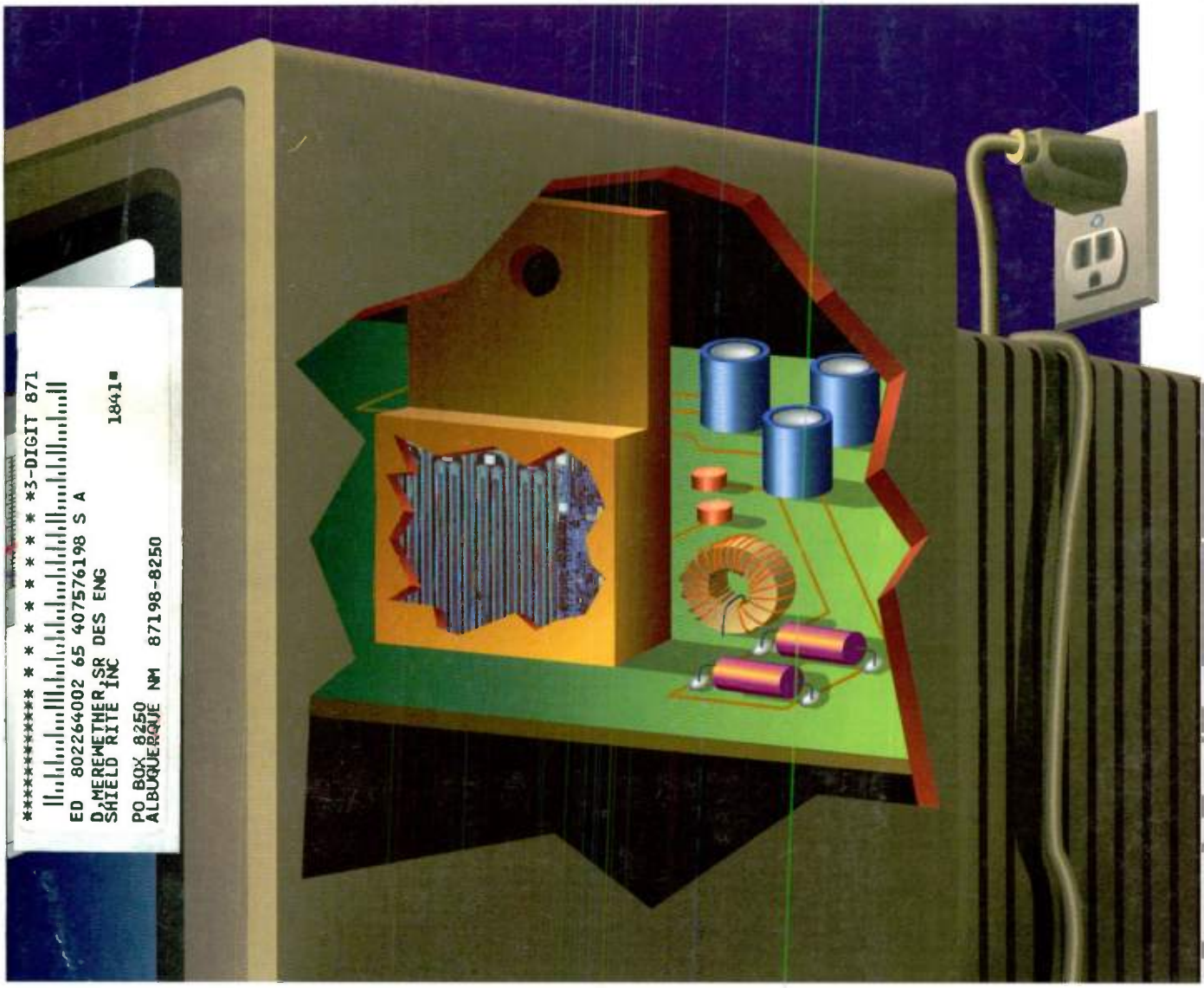
ELECTRONIC DESIGN

FOR ENGINEERS AND ENGINEERING MANAGERS-WORLDWIDE

A PENTON PUBLICATION $10.00

APRIL 1, 1997



Switch-Mode ICs Minimize Off-Line Power-Supply Size p. 53

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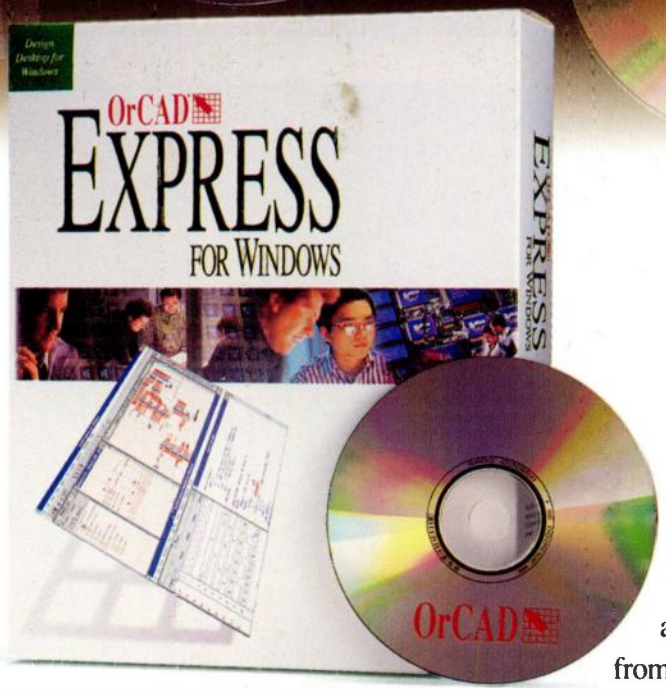

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Columbia, MD	June 3
Dallas, TX	June 10
Dayton, OH	April 29
Denver, CO	May 20
Detroit, MI	June 19
Fairfield, NJ	May 15
Houston, TX	June 12
Indianapolis, IN	May 1
Irvine, CA	May 28
Kansas City, MO	May 15
Long Island, NY	May 13
Milwaukee, WI	June 3
Minneapolis, MN	May 1
Montreal, QUE	May 29
Orlando, FL	June 26
Ottawa, Ontario	June 24
Philadelphia, PA	June 5
Phoenix, AZ	June 19
Pittsburgh, PA	June 5
Portland, OR	June 10
Rochester, NY	June 12
Salt Lake City, UT	May 22
San Diego, CA	June 17
San Jose, CA	May 6
Seattle, WA	June 12
St. Louis, MO	May 13
Toronto, Ontario	May 28
Vancouver, BC	May 8
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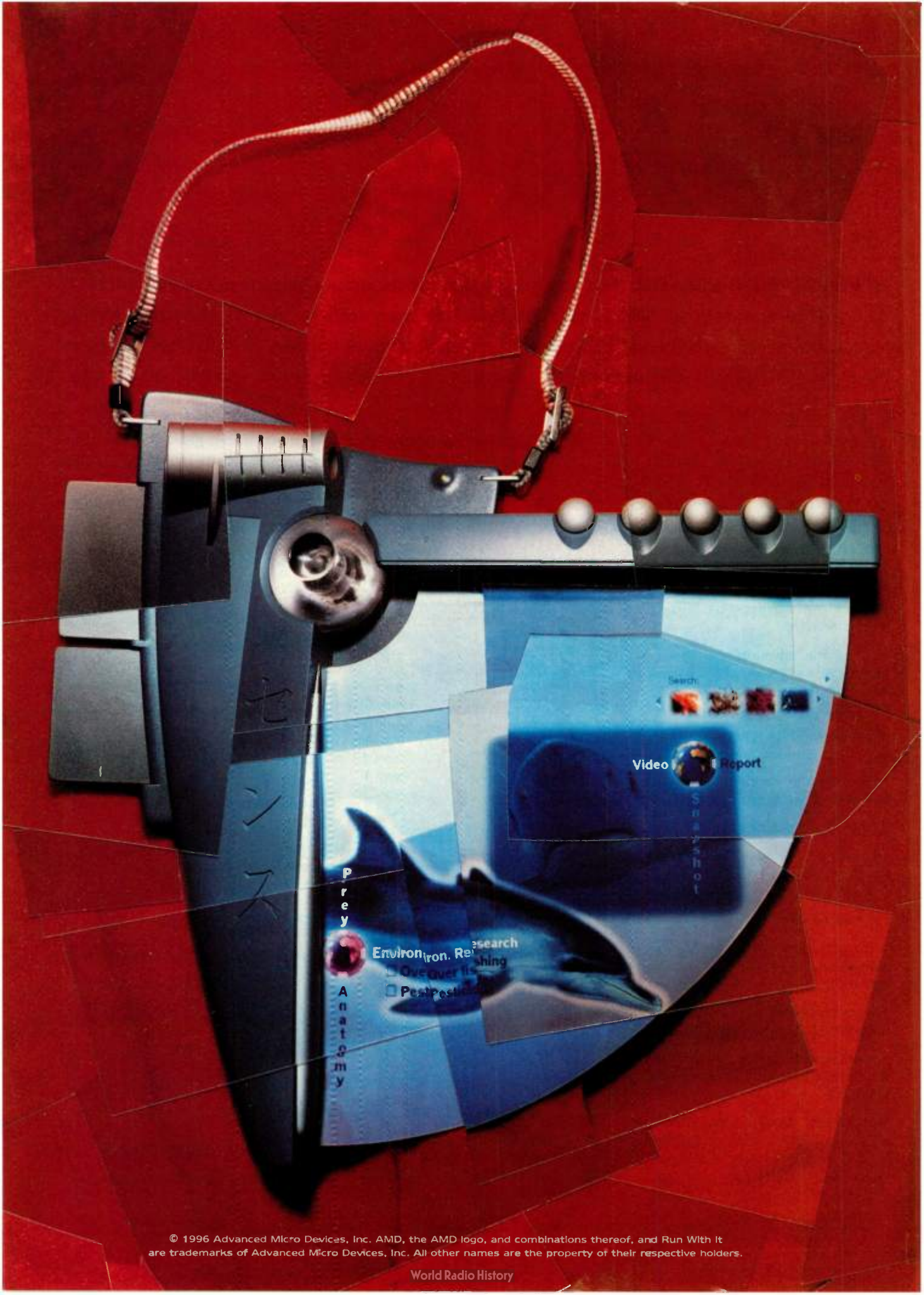

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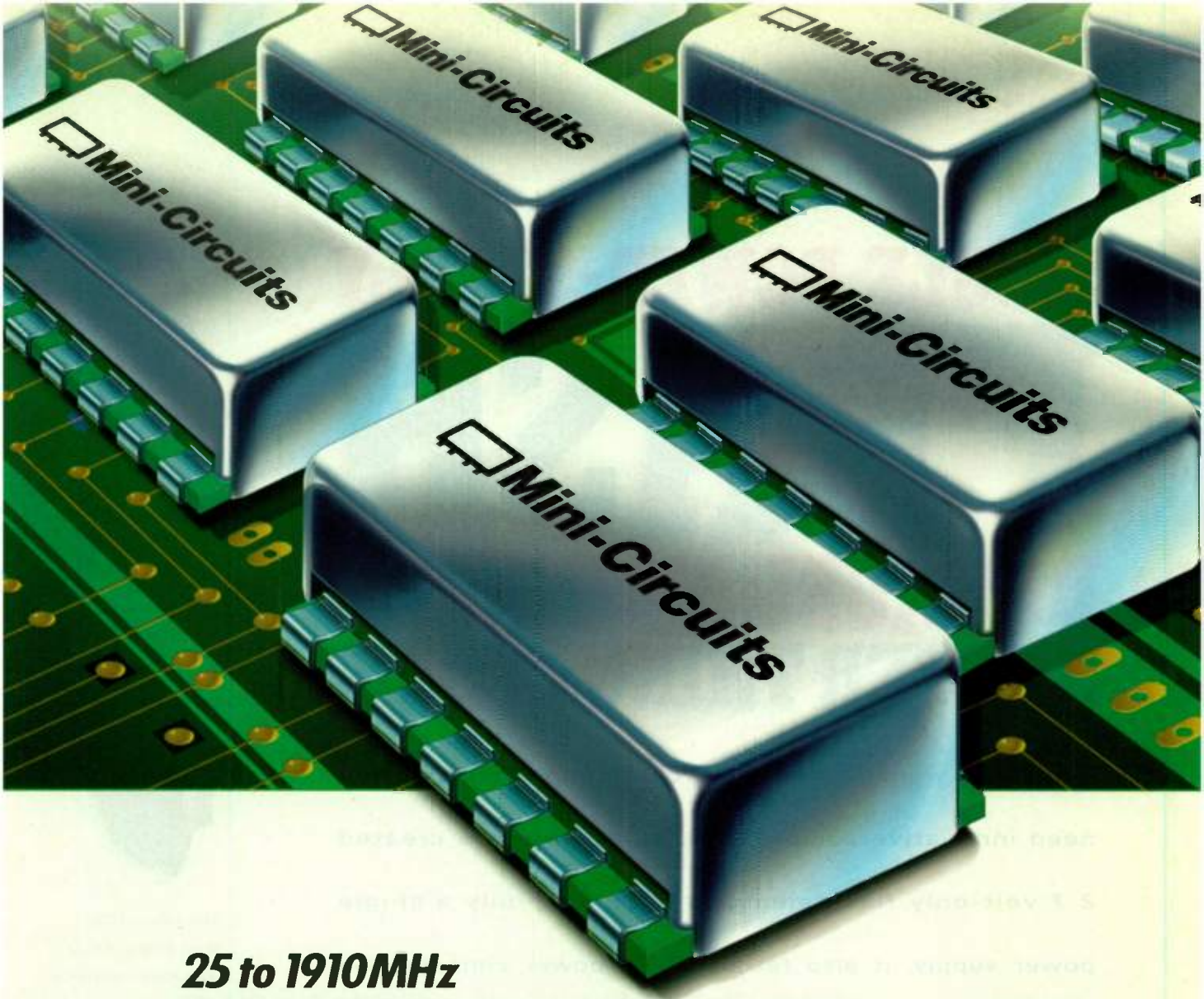

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Model	Freq. Range (MHz)	Phase Noise (dBc/Hz) SSB@ 10kHz Typ.	Harmonics (dBc) Typ.	V_{tune}** 1V to:	Current (mA) @+12V DC Max.	Price $ea. (5-49)*
JTOS-50	25-47	-108	-19	15V	20	13.95
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JTOS-100	50-100	-108	-35	16V	18	13.95
JTOS-150	75-150	-106	-23	16V	20	13.95
JTOS-200	100-200	-105	-25	16V	20	13.95
JTOS-300	150-280	-102	-28	16V	20	15.95
JTOS-400	200-380	-102	-25	16V	20	15.95
JTOS-535	300-525	-97	-28		20	15.95
JTOS-765	485-765	-98	-30	16V	20	15.95
JTOS-1025	685-1025	-94	-28	16V	22	18.95
JTOS-1300	900-1300	-95	-28	20V	30	18.95
JTOS-1650	1200-1650	-95	-20	13V	30	19.95
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JCOS-820WLN	780-860	-112	-13	20V	25 (@9V)	49.95
JCOS-820BLN	807-832	-112	-24	14V	25 (@10V)	49.95
JCOS-1100LN	1079-1114	-110	-15	20V	25 (@8V)	49.95

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ELECTRONIC DESIGN

April 1, 1997 Volume 45, Number 7

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ANALOG OUTLOOK

COMMUNICATIONS TECHNOLOGY

COMMUNICATIONS TECHNOLOGY

BOARDS & BUSES

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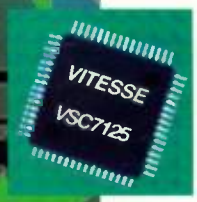

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The industry's first integrated Fibre Channel transceiver offers low power (650 mW) and low cost. [VSC7125]

1.25 Gb/s 10-Bit Transceiver
The first Gigabit Ethernet transceiver provides the highest performance and lowest power (700 mW) solution. [VSC7135]

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This low cost, fully integrated hub circuit retimes 1 Gb/s Fibre Channel data and bypasses faulty ports. [VSC7120]

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April 1, 1997 Volume 45, Number 7

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DEPARTMENTS

COVER ILLUSTRATION BY: MARGARET ENDRES-BANGS

Jesse H. Neal Editorial Achievement

1967 First Place Award	1978 Certificate of Merit
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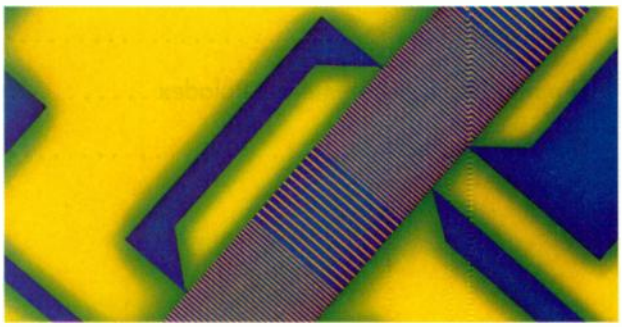

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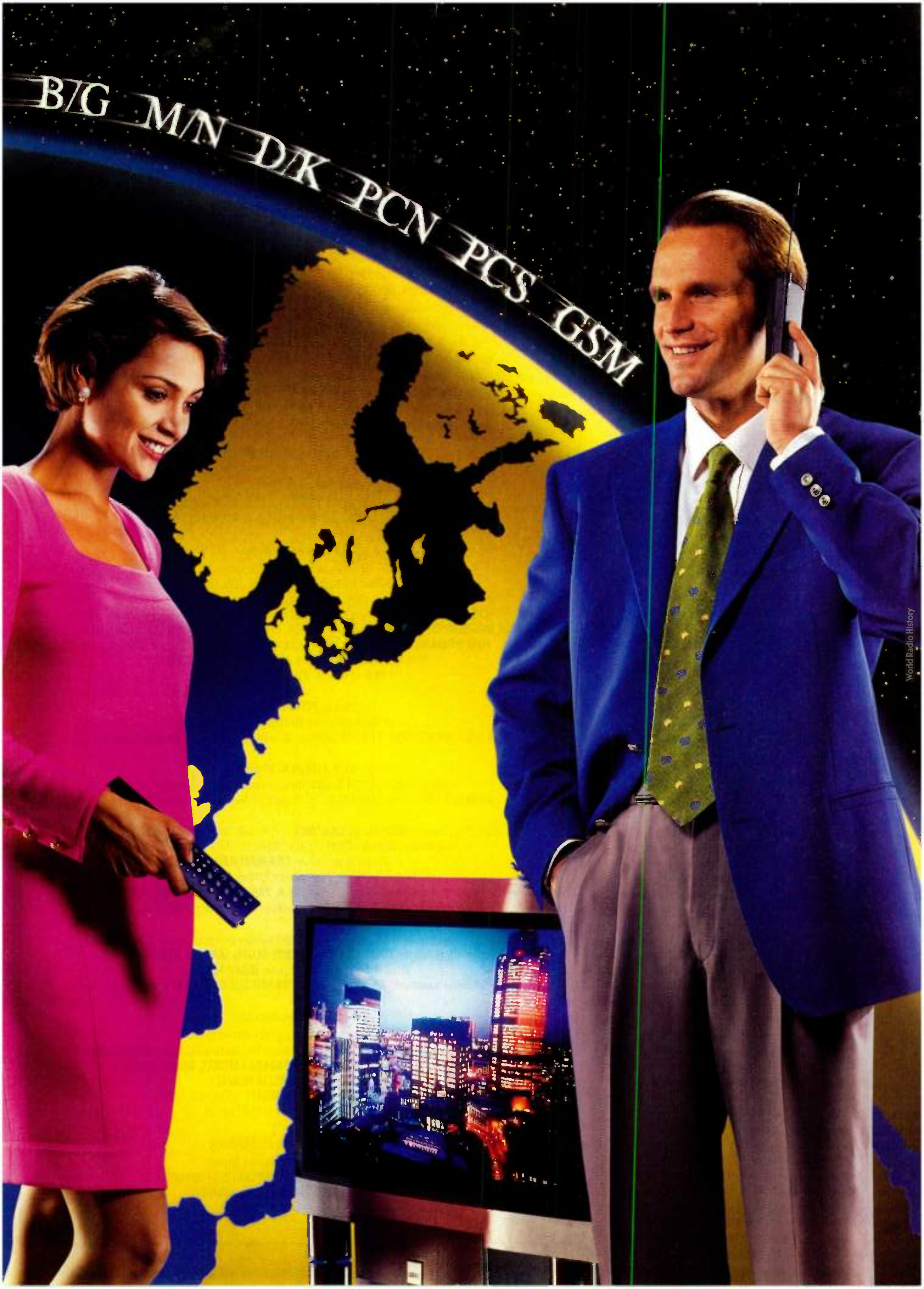

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APRIL 1997

Fourth ASAT Conference, Apr. 14-16. San Francisco Airport Marriott, San Francisco, CA. Contact Suzanne Graf, Project Manager, (541) 984-5204; fax (541) 343-7024; e-mail: SGraf@Advanstar-Expos.com.

Third Annual PCI Plus Conference, Apr. 14-18. Santa Clara Convention Center, Santa Clara, CA. Contact Annabooks, (800) 690-3858 or (619) 673-0870; fax (619) 673-1591; e-mail:pci@annabooks.com.

IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP 97), Apr. 21-24. Gasteig Cultural and Convention Center, Munich, Germany. Contact Bernd Girod, Lehrst.f.Nachrichtentechnik, Univ. of Erlangen Nuremberg, Cauerstr. 7, D-91058 Erlangen, Germany; (49) 91-3185-7101; fax (49) 91-3131-30840; e-mail: b.girod@ieee.org.

International Conference on High Performance Computing, Apr. 21-25. Hotel Lotte World, Seoul, Korea. Contact Ki Soo Sung, Tongmyung University of Information Technology 535; Yongdang-dong, Nam-gu, Pusan, Korea; (82) 52 629 1021; fax (82) 51-627-8362; e-mail: kssung@tmic.tit.ac.kr.

Sixth System Administration, Networking, & Security Conference, Apr. 21-26. Baltimore Inner Harbor, MD. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

IEEE International Conference on Robotics and Automation, Apr. 21-27. Albuquerque Convention Center, Albuquerque, New Mexico. Contact Jerry Stauffer, Intelligent Systems and Robotics Center, Program Office, MS0949, Sandia National Laboratories, Albuquerque, NewMexico 87185-0949; (505) 845-8966; fax (505) 844-6161; e-mail: jdstauf@isrc.sandia.gov.

First Convergence Technology & IC Expo, Apr. 22-24. InfoMart, Dallas, TX. Contact Electronic Conventions Management, 8110 Airport Boulevard, Los Angeles, California 90045; (800) 877-2668, ext. 243; fax (310) 641-5117.

15th IEEE VLSI Test Symposium, Apr. 27-30. Hyatt Regency Monterey, Monterey, CA. Contact Y. Zorian; (408) 543-0146 ext. 227, e-mail: zorian@lvision.com.

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IEEE Vehicular Technology Conference (VTC), May 5-7. Hyatt Regency at Civic Plaza, Phoenix, AZ. Contact Wendy Rochelle, IEEE Conference Services, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331; (908) 562-3870; fax (908) 981-1769; e-mail: w.rochelle@ieee.org.

International Test Synthesis Workshop, May 5-7. Santa Barbara, CA. Contact K. Wagner; (415) 694-4386; e-mail: kwagner@symopsys.com.

IEEE Custom Integrated Circuits Conference (CICC '97), May 5-8. Santa Clara Convention Center, Santa Clara, CA. Contact Melissa Widerkehr, Widerkehr & Associates, Suite 270, 101 Lakeforest Blvd, Gaithersburg, MD 20877; (301) 527-0902; fax (301) 527-0994; e-mail: cicc96@aol.com.

Electronics Industries Forum of New England, May 6-8. World Trade Center, Boston, MA. Contact Summit Exhibition Management Inc., Norwalk CT; (800) 322-9332; (203) 855-3000; fax (203) 855-3003.

IEEE Power Industry Computer Applications Conference (PICA), May 11-16. Contact T.C. Wong, American Electric Power, 1 Riverside Plaza, Columbus, OH 43215; (614) 223-2235; fax (614) 223-2205; e-mail: t.wong@ieee.org.

Third International Conference on Optical Fiber Submarine Telecommunication Systems (SubOptic'97), May 11-16. Contact Ida M. Espinoza, 340 Mt. Kemble Ave., S120, Morristown, NJ 07960; (201) 326-2119; fax (201) 326-2609; e-mail: iespinoza@attmail.com.

IEEE/IAS Industrial & Commercial Power Systems Technical Conference (I&CPS), May 12-15. Wynham Hotel, Philadelphia, PA. Contact Barry Hornberger, Philadelphia Electric Co., 2301 Market St., Bldg N3-1, Philadelphia, PA 19101; (215) 841-4619.

Fifth IFIP/IEEE International Symposium on Integrated Network Management (ISINM '97), May 12-16. Hotel Del Coronado, San Diego, California. Contact Ann Marie Lambert, BBN Systems & Technologies, 10 Moulton St., Cambridge, Massachusetts 02138; (617) 873-3819; fax (617) 873-37776; e-mail: isinm97@bbn.com.

IEEE Particle Accelerator Conference, May 12-16. Vancouver, BC, Canada. Contact M.K. Craddock, TRIUMF, 4004 Wesbrook Mall, Vancouver, BC V6T 2A3 Canada; (604) 222-7341; fax (604) 222-7309; e-mail: craddock@triumf.ca.

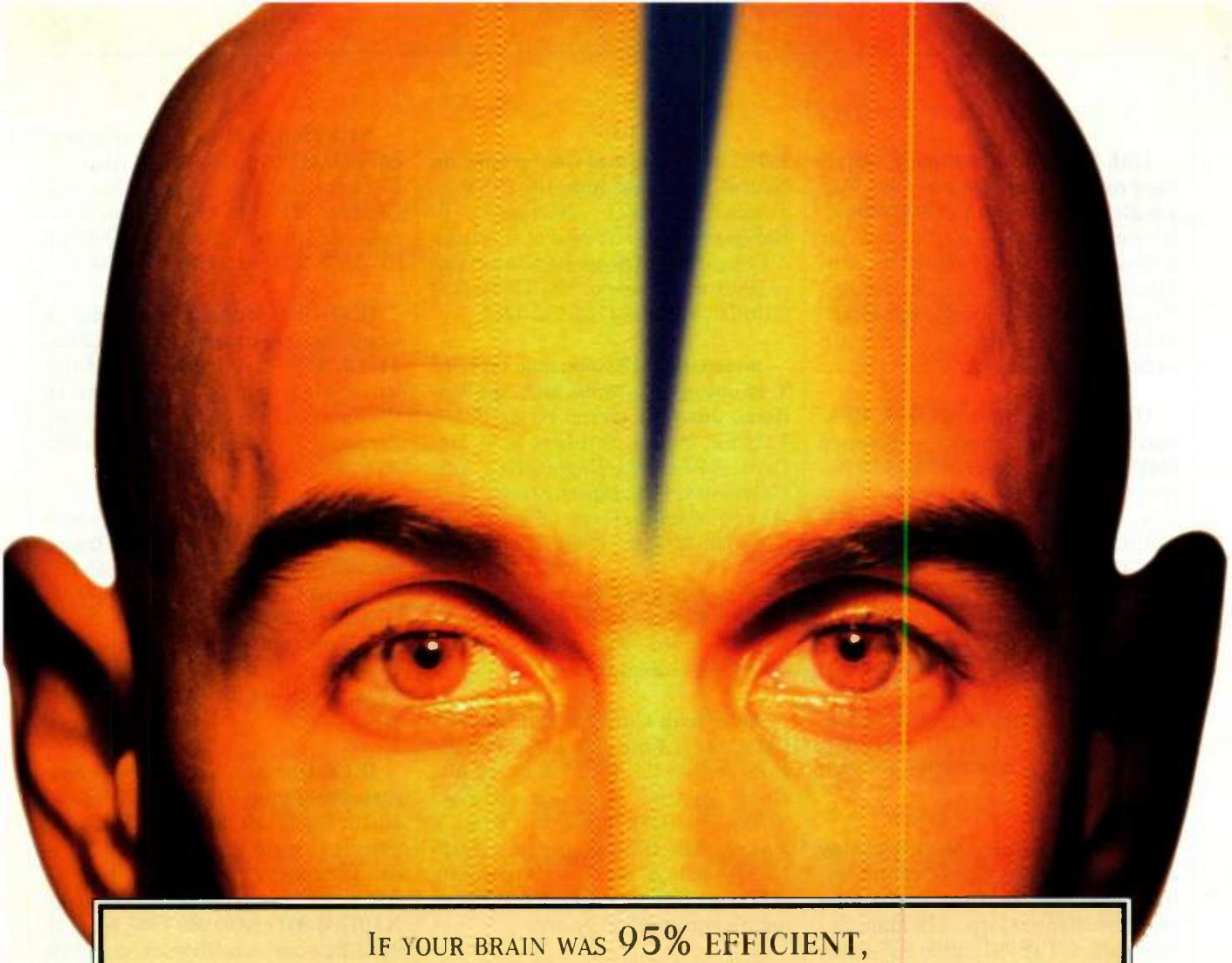
Antennas: Principles, Design, and Measurements (Short Course), May 13-16. St. Cloud, FL. Contact Kelly Brown, NCEE, 1101 Massachusetts Ave., St. Cloud, FL 34669; fax (407) 892-0406.

IEEE Radar Conference, May 13-15. Sheraton University Hotel & Conference Center, Syracuse, New York. Contact Michael Wicks, Rome Laboratory, 26 Electronics Pkwy., Rome, New York 13441; (315) 330-4437; fax (315) 330-2528; e-mail: wicksm@rl.af.mil.

Sensors Expo Boston, May 13-15. Hynes Convention Center, Boston, MA. Contact Expocon Management Associates Inc. (203) 256-4700; e-mail: sensors@expocon.com; Internet: http://www.expocon.com.

47th Electronic Components & Technology Conference, May 18-21. The Fairmont Hotel, San Jose, CA. Contact Jim Bruorton, Electronic Industries Association, 2500 Wilson Blvd., Arlington, VA 22201-3834; (864) 963-6621.

Finishing '97 Conference & Exposition, May 19-22. Rosemont Convention Center, Rosemont (Chicago), IL. Contact Society of Manufacturing Engineers; (800) 733-4763.



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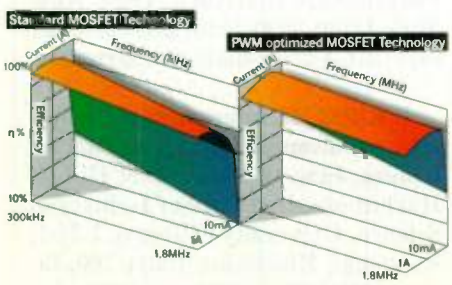

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MAY

19th IEEE International Conference on Software Engineering, May 19-23. Boston, MA. Contact W. Richard Adrion, Dept. of Computer Science, University of Masachusetts/Amherst, 307 LGRC, P.O. Box 34610; Amherst, MA 01003-4610; (413) 545-2742; e-mail: adrion@cs.umass.edu.

IEEE Instrumentation & Measurement Technology Conference (MTC '97), May 20-22. Chateau Laurier, Ottawa, Ontario, Canada. Contact Robert Myers, Conference Coordinator, 3685 Motor Ave., Suite 240, Los Angeles, CA 90034; (310) 287-1463; fax (310) 287-1851; e-mail: bob.myers@ieee.org.

OEMed Midwest, May 21-22. Rosemont Convention Center, Rosemont, IL. Contact Exposition Excellence Corp., 112 Main St., Norwalk, CT 06851; (203) 847-9599; fax (203) 854-9438.

OEM Electronics Midwest, May 21-22. Rosemont Convention Center, Rosemont, IL. Contact Exposition Excellence Corp., 112 Main St., Norwalk, CT 06851; (203) 847-9599; fax (203) 854-9438.

Canadian Conference on Electrical & Computer Engineering, May 25-28. Delta Hotel, Newfoundland, Canada. Contact David Collett, Newfoundland & Labrador Hydro, P.O. Box 12400, St. Johns, NF, A1A 4K7, Canada; (709) 737-1372; fax (709) 737-1782; e-mail: t.d.collett@ieee.org.

Fifth IEEE International Conference on Properties & Applications of Dielectric Materials (ICPADM), May 25-30. Sheraton Walker Hill, Convention Center, Seoul, Korea. Contact Joon-Ung Lee, Department of Electrical Engineering, Kwangwoon University, 447-1 Wolgye-Dong, Nowon-Ku, Seoul, 139-701, Korea; (82)-2-910-5144; fax (82)-2-942-0107.

Next Generation Telephony West: Voice Over the Internet, May 28-30. Hotel Monaco, San Francisco, California. Contact (800) 822-6338 or (202) 842-3022 ext.317; Internet: http://www.brp.com.

JUNE

IEEE International Conference on Neural Networks, June 1-5. Houston, Texas. Contact Nicolaos B. Karayiannis, Department of Electrical & Computer Engineering, University of Houston, Houston, TX; 77204-4793 (713) 743-4436; fax (713) 743-4444.

International Symposium on VSLI Technology, Systems, and Applications, June 3-5. Grand Hyatt Hotel, Taiwan, China. Contact T. P. Ma, Dept. of Electrical Engineering, Yale University, 15 Prospect Street, New Haven, Connecticut 06520-8284; (203) 432-4211; fax (203) 432-7769.

Mixed Signal Test Workshop; June 3-6. Seattle, WA. Contact M. Soma; (206) 685-3810; e-mail: soma@ee.washington.edu.

American Control Conference (ACC '97), June 4-6. Albuquerque Convention Center, Albuquerque, New Mexico. Contact Steven Yurkovich, Department of Elec. & Engrg., The Ohio State Univ., 2015 Neil Avenue, Columbus, Ohio 43210; (614) 292-2586; fax (614) 292-7596; e-mail: s.yurkovich@i.ee.org.

IEEE International Conference on Communications (ICC 97), June 8-12. Montreal, Canada. Contact Celia Desmond, Stentor, Fl. 6b, 33 City Center Dr., Mississauga, Ontario L5B 2N5, Canada; (905) 615-6507; fax (905) 615-8421; e-mail: celia.desmond@tc.resonet.com.

IEEE/MTT-S International Microwave Symposium (MTT 97), June 8-13. Convention Center, Denver, CO. Contact John Dunn, Dept. of Electrical & Computer Engineering, University of Colorado, Campus Box 425, Boulder, CO 80309; (303) 492-5920; fax (303) 492-5323; e-mail: dunn@boulder.colorado.edu.

IEEE International Symposium on Circuits & Systems (ISCAS 97), June 9-12. Hong Kong Convention & Exhibition Centre, Hong Kong. Contact ISCAS '97 Secretariat, Department of Electrical & Electronic Engineering, University of Hong Kong, Pokfalam Rd., Hong Kong; (852) 28592710; fax (852) 25598738; e-mail: iscas97@hkueee.hku.hk.

34th Design Automation Conference (DAC '97), June 9-13. Anaheim Convention Center, Anaheim, CA; Contact MP Associates Inc., 5305 Spine Rd., Suite A, Boulder, CO 80301; (303) 530-4333; fax (303) 530-4334.

IEEE International Conference on Consumer Electronics (ICCE), June 11-13. The Westin Hotel O'Hare, Rosemont, IL. Contact Diane D. Williams, 67 Raspberry Patch Dr., Rochester, NY 14612-2868; (716) 392-3862; fax (716) 392-4397.

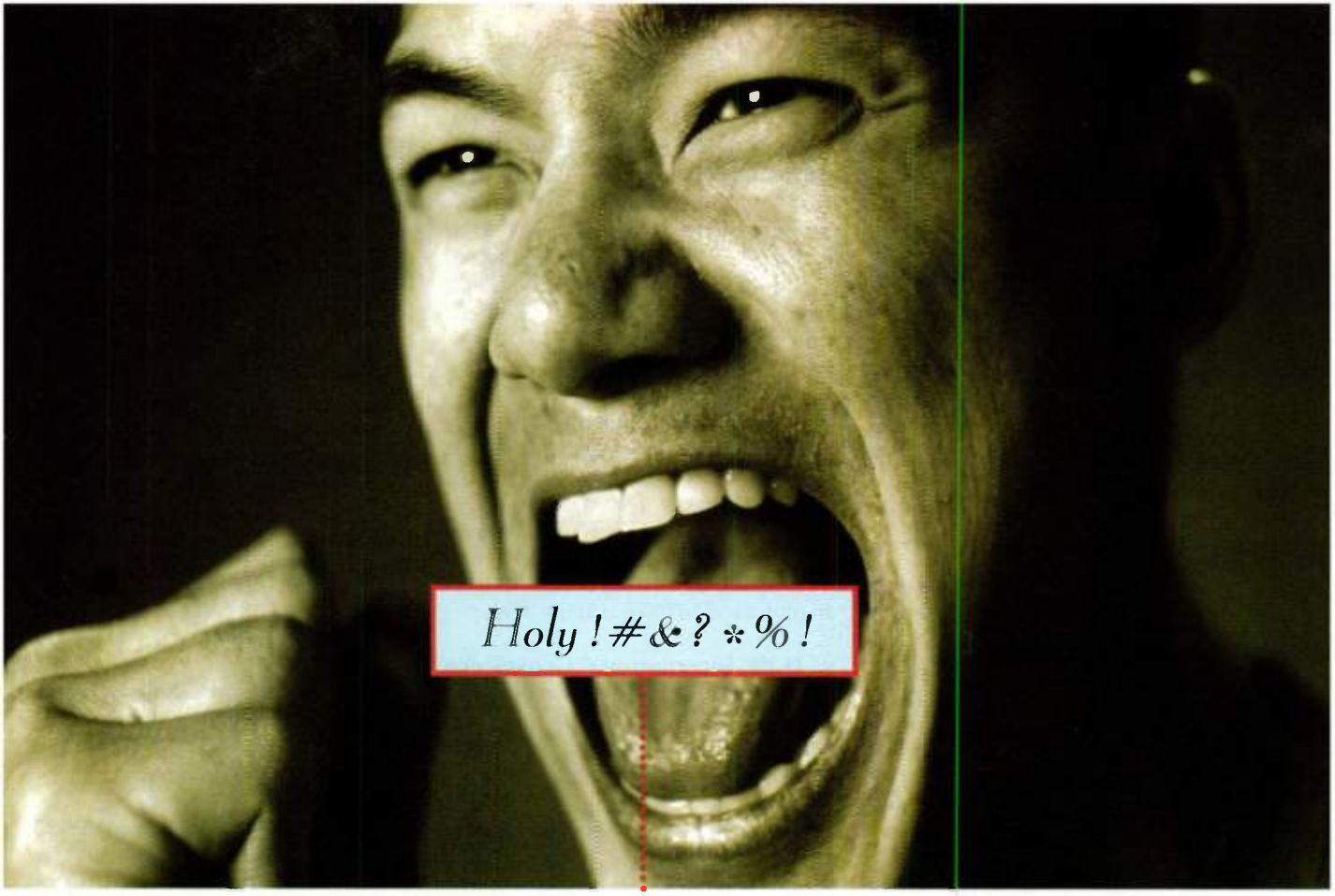
International Solid-State Sensors and Actuators Conference (Transducers 97), June 15-19. Hyatt Regency Hotel, Chicago, IL. Contact Kensal D. Wise, 1246 EECS Building, University of Michigan, 1301 Beal Ave., Ann Arbor, MI 48109-2122; (313) 764-3346; fax (313) 747-1781.

IEEE Digital Cross Connect Systems Workshop VII (DCS 97), June 16-19. Banff Park Lodge, Banff, Alberta, Canada. Contact James H. Simester, Lucent Technologies, P.O. Box 3030, Room 4J-526, 101 Crawfords Corner Rd., Holmdel, NJ 07733-3030; (908) 949-7336; fax (908) 949-2724; e-mail: sims@bostare.ho.att.com.

Third Conference on Object-Oriented Technologies & Systems (Coots 97), June 16-19. Marriott Hotel, Portland, Oregon. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, California 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

IEEE International Conference on Systems, Man, and Cybernetics, June 16-20. Hyatt Orlando, Orlando, Florida. Contact James M. Tien, Chair, DSES Department, Rensselaer Polytechnic Institute, Troy, New York 12180-3590; (518) 276-6486; fax (518) 276-8227; e-mail: tienj@rpi.edu.

IEEE/ASME International Conference on Advanced Intelligence Mechatronics, June 16-20. Contact Hideki Hashimoto, Institute of Industrial Science, University of Tokyo, 7-22-1, Roppongi, Minato-ku, Tokyo 100, Japan; (81) 3 3402 6231 ext. 2359; fax (81) 3 3423 1484.



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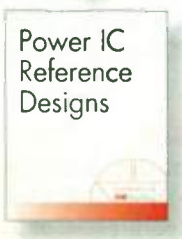

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JUNE

IEEE Sixth International Fuzzy Systems Conference, June 20-25. Barcelona, Spain. Contact Ramon Lopez De Mantaras, IIIA-CSIC Campus U.A.B., 08193 Cerdanyola del Valles, Spain; (34) 3-580-95-70.

IEEE Power Electronics Specialist Conference (PESC 97), June 22-27. Regal Riverfront Hotel, St. Louis, MO Contact Philip T. Krein, University of Illinois, 1406 W. Green St., Urbana, IL 61801; (217) 333-4732; e-mail: krein@uipesl.ece.uiuc.edu.

IEEE International Symposium on Information Theory, June 29-July 4. Ulm, Germany. Contact Han Vinck, Institue of Experimental Mathematics, University of Essen, Ellernstr. 29, 45326 Essen, Germany; (49) 201 3206458; fax (49) 201 3206425.

Sixth IEEE International Fuzzy Systems Conference, June 30-July 5. Barcelona, Spain. Contact Ramon Lopez de Mantaras, IIIA-CSIC Campus U.A.B. 08193 Cerdanyola del Valles, Spain; (34) 3 580 95 70.

JULY

Fifth TCL/TK Workshop, July 14-17. Tremont House Hotel, Boston MA. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

IEEE Power Engineering Society Summer Meeting, July 20-25. Intercontinental Hotel, Berlin, Germany. Contact Executive Office, IEEE Power Engineering Society, P.O. Box 1331, Piscataway, NJ 08855-1331; (908) 562-3864; fax (908) 981-1769.

IEEE Signal Processing Workshop on Higher Order Statistics, July 21-23. Banff Centre for Conferences, Banff, Alberta, Canada. Contact Keh-Shin Lii, Department of Statistics, University of California, Riverside, 900 University Ave., Riverside, CA 92521; (909) 787-3836; fax (909) 787-3286; e-mail: ksl@ucrstat.ucr.edu.

IEEE Nuclear & Space Radiation Effects Conference (NSREC '97), July 21-25. Snowmass Conference Center, Snowmass, CO. Contact Dennis B. Brown, Naval Research Laboratory, Code 6612, Washington, DC. 20375; (202) 767-5453; fax (202) 404-8076; e-mail: dbbrown@ccfnrl.nvy.mil.

AUGUST

40th Midwest Symposium on Circuits and Systems, Aug. 2-6. Hyatt Regency Hotel, Sacramento, CA. Contact Sharon Baumgartner, Department of E&CE, University of California, Davis, CA 95616; (916) 754-6216; fax (916) 752-8428; e-mail:mwscas97@ece.ucdavis.edu.

IEEE International Geoscience & Remote Sensing Symposium (IGARSS '97), Aug. 4-8. Singapore International Convention Exhibition Centre, Suntec City, Singapore. Contact Kwoh Leong Keong, CRISP, National University of Singapore, Faculty of Science, Lower Kent Ridge Rd., S 119260 Singapore; (65) 7727838.

Memory Technology, Design, & Test Workshop, Aug. 11-12. San Jose, CA. Contact F. Lombardi; (409) 845-5464; e-mail: lombardi@cs.tamu.edu.

IEEE International Symposium on Electromagnetic Compatibility (EMC '97), Aug. 18-22. Contact John Osburn, EMC Test Systems LP., 2205 Kramer Lane, Austin, TX 78758; (512) 835-4684 ext. 669; fax (512) 835-4729.

SEPTEMBER

Telecom Interactive '97, Sept. 8-14. Geneva, Switzerland. Contact (703) 907-7736.

Fifth European Congress on Intelligent Techniques and Soft Computing (EUFIT '97), Sept. 8-12. Aachen, Germany. Contact Promenade 9, 52076 Aachen, Germany; (49) 2408 6969; fax (49) 2408 94582; e-mail: eufit@mitgmbh.de; Internet: http://www.mitgmbh.de/elite/elite/eufit.html.

ICSPAT/DSP WORLD 1997, Sept. 14-17. San Diego Convention Center, San Diego, CA. Contact Denise Chan, Miller Freeman Inc. (415) 278-5231; e-mail: dsp@exporeg.com.

MCM Test Workshop, Sept. 14-17. Napa Valley, CA. Contact Y. Zorian, (408) 453-0146 ext. 227; e-mail: zorian@lvision.com.

International Conference on Solid State Devices and Materials (SSDM), Sept. 16-19. Act City Hamamatsu, Hamamatsu, Japan. Contact Secretariat of SSDM '97, % Business Center for Academic Societies Japan, 5-16-9 Honkomagome, Bunkyo,Tokyo 113, Japan; (81) 3 5814 5800; fax (81) 3 5814 5823; e-mail: confg3@bcasj.or.jp.

Thermionic Workshop, Sept. 21-23. Cannes, France. Contact B. Courtois; (33) 35 76 7 46 15; e-mail: bernard.courtois@imag.fr.

AUTOTESTCON '97, Sept. 22-25. Disneyland Hotel, Anaheim, CA. Contact Robert C. Rassa, Hughes Aircraft, P.O. Box 92426, MS R07/P553, Los Angeles, CA 90009-2426; (310) 334-4922; fax (310) 334-2578; e-mail: rcrassa@ccgate.hac.com.

Electrical Overstress/Electrostatic Discharge Symposium, Sept. 23-25. Santa Clara Convention Center, Santa Clara, CA. Contact ESD Association, 7902 Turin Rd., Suite 4, Rome, NY 13440-2069; (315) 339-6937; fax (315) 339-6793.

Fifth China International Electronics Exhibition (CIEE '97), Sept. 24-28. China International Exhibition Centre, Beijing. Contact Gu Jinjing, CEIEC, P.O. Box 140, Beijing, 100036 China; (011) 8610 6822 3909; fax (011) 8610 6821 3348

Embedded Systems Conference, Sept. 29-Oct. 3. San Jose Convention Center, San Jose, CA. Contact Miller Freeman Inc. (415) 278-5231; e-mail: esc@exporeg.com.

OCTOBER

OEMed Northeast, Oct. 1-2. Bayside Expo Center, Boston, MA. Contact Exposition Excellence Corp., 112 Main St., Norwalk, CT 06851; (203) 847-9599; fax (203) 854-9438.

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EDITORIAL

Engineers And Public Perception

In the last issue of *Electronic Design*, my colleague Steve Scrupski commented in his editorial, "The Curse Of Normality," that "it's a well-known fact that engineers are well above the average in intelligence, taste, and in making sensible choices in lifestyle." His comments were related to an advertising campaign for Hewlett-Packard (H-P) printers in which the tag line is "Built by engineers. Used by normal people." The ad, and Steve, were referring to those individuals who "create" things, including electronic, mechanical, and packaging engineers, to name a few. Which brings up another point: Just what is the general public perception of electrical/electronic engineers? Judging from my many experiences and I'm sure those of many electrical/electronic engineers, the answer can be considered a mixed bag at best, and not very encouraging at worst.

It's another well-known fact that if you asked, for instance, 10 average persons of what they think an engineer does, chances are that quite a few (some would say a majority) would think that such a person is either a train operator or a person who maintains "boilers." We even have garbage collectors being called "sanitation engineers." Many people think that electrical engineers are electricians. This is not to demean these latter professions, but there can be no comparison between the formal and rigorous education, training, and intellect that electrical/electronic, chemical, and mechanical engineers must endure and those borne by train operators, boiler-maintenance persons, and sanitation collectors. Electrical engineers design the electric-utility systems that give rise to a huge infrastructure in which electricians can ply their trade in wiring up homes and buildings. This is certainly not the public's fault. It's more the fault of the engineering professions and the organizations that represent them for not "educating" the general public about what engineers really do and stand for. Unions representing boiler makers and train operators carry the banner quite loudly for their members. Contrast this with another well-known fact that engineers in general tend to be "humble" individuals who don't always "toot their horns" about their accomplishments, and you can see why there is this false perception of who an engineer is and what he or she does.

The IEEE is probably in the best position to act as a spokesman for electrical/electronic engineers. I'm also sure there may be just as many engineers who could care less about public perception as there are those who do care. I tend to care. Perhaps if the IEEE promoted the professional aspects of electrical/electronic engineering to the general public, in sort of the same fashion as H-P's ad campaign, all of us might be winners—engineers as well as the general public. *rallan@class.org.*

Roger Allan
Executive Editor

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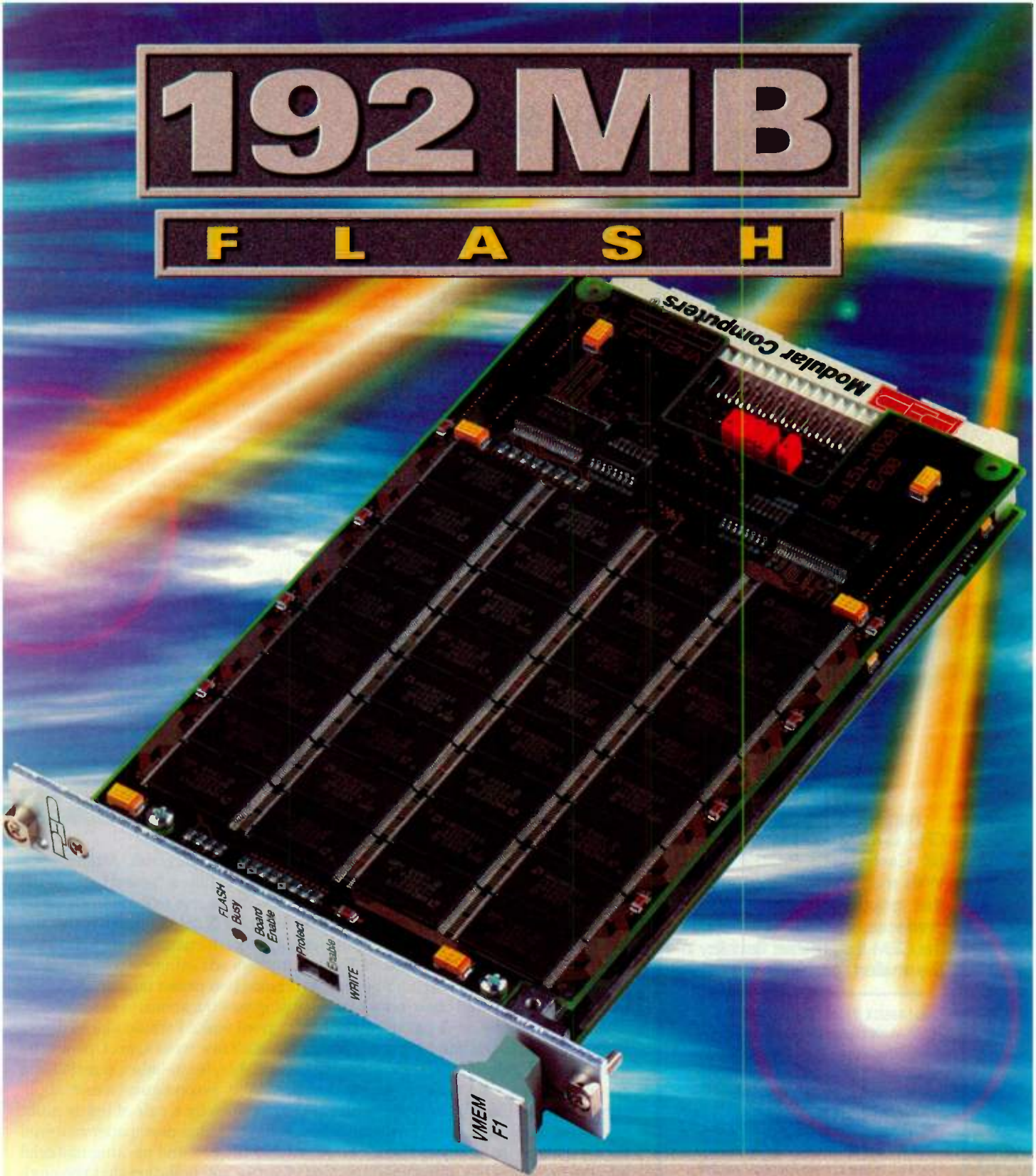

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Field Of Geeks

Poor Catherine. Even after nine years together, she's never been quite able to deal with the fact that I cry at movies. When she feels a telltale shudder next to her in the theater, she sort of hunches down in the seat and pretends to be sitting with somebody else. I guess it wouldn't be so tough on her if it didn't happen at during Disney cartoons and Kevin Costner flicks. Nevertheless, she's the one who bought me a videotape of "Apollo 13" for my birthday, plopped down on the couch with a box of tissues, and held my hand as we relived the acts of ingenuity, teamwork, and determination that brought the astronauts home safely after any reasonable person would have given them up for lost.

One of my favorite parts of the movie is when the managers at Mission Control dump out a boxfull of parts onto a table in front of a bunch of bowtied-and-bespectacled engineers and tell them to devise an emergency air purifier that the astronauts can build themselves from the junk they have in their capsule. It's so much like what many of us face every day at work that it brings tears to my eyes (sorry about that, Catherine). That movie did so much for the self-esteem of engineers everywhere that I'll even forgive Tom Hanks for playing "Forrest Gump."

Thanks to movies like this, and society's fascination with anything digital, engineers are enjoying a level of respectability we haven't known since the fifties. Look 1996's hottest movie: "Independence Day." Who gets to save the world? A nerdy engineer! Finally, it's chic to be geek! Too bad the trend happened so late. When I was single, I had to tell women I was a truck driver to get a date.

LEE GOLDBERG
Communications

While its great that we're finally being recognized, we shouldn't forget that engineers have been quietly "saving the world" in big and small ways since the dawn of history. Most of the time, we toil as wage slaves, doing the bidding of the corporation or kingdom that we find ourselves attached to, but more than occasionally one of our rank manages to get beyond the agenda of the moment and apply their skills to "the bigger picture."

One of the best examples I can think of is the Voyager spacecraft. Although scientists had hoped to use a rare planetary alignment to take a "grand tour" of the Solar system, politicians mandated a smaller, less expensive mission to swing by Jupiter and Saturn. While they followed the "letter" of NASA's directive, the project's engineers managed to quietly design lots of performance margin into the spacecraft's systems. This allowed Voyager to take advantage of a "fortunate" launch window that carried it far beyond its original two-planet mission, giving us a wealth of unexpected discoveries and surprising new questions.

Since most of us don't get to work at this grand scale, I would like to direct your attention to the humble toaster oven I bought a few weeks ago. Opening its box, I braced myself for the shower of nonrecyclable, toxin-laden, plastic foam "peanuts," bags, and packing inserts that inevitably accompanies a new appliance. Instead, I found the oven securely held in place by a pair of lightweight conformal shells that were made out of the same recycled newspaper material that is used to make egg cartons! While putting the box and packing material into the recycling bin, I imagined the tons of waste and pollution that the engineers at Black and Decker had prevented. It made me wonder what each one of us can do within the context of our own jobs and lives.

Thanks to your response to an earlier column, I'm starting to cover some of the ways we are "making a difference" in the world. I'm asking you to send me stories, potential contacts, or personal accounts of "geek heroes" and their exploits. Wherever possible, I'll publish them here, or in a book on "green engineering" that I've been asked to write. Who knows, if the trend continues, we may see Kevin Costner starring in movies like "Dances With Workstations" or "Field of DRAMs." *leeg@class.org*

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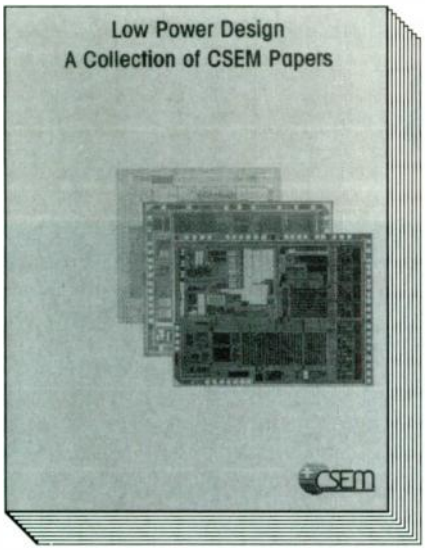

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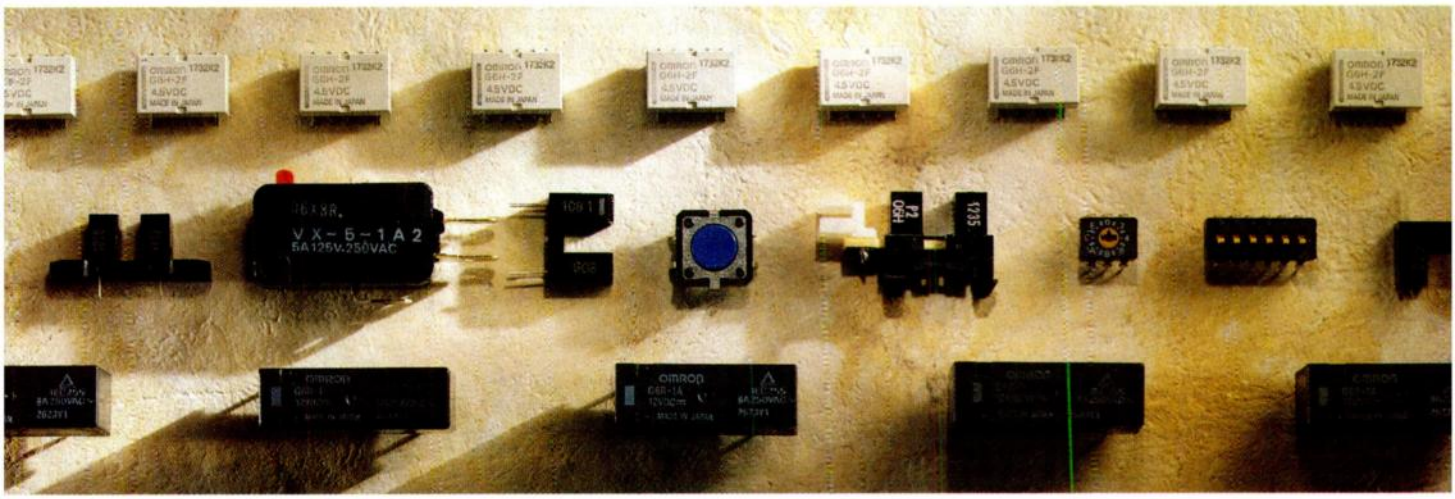

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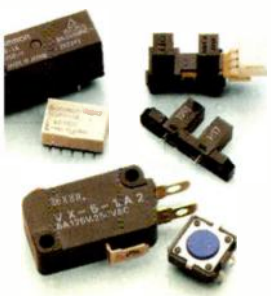

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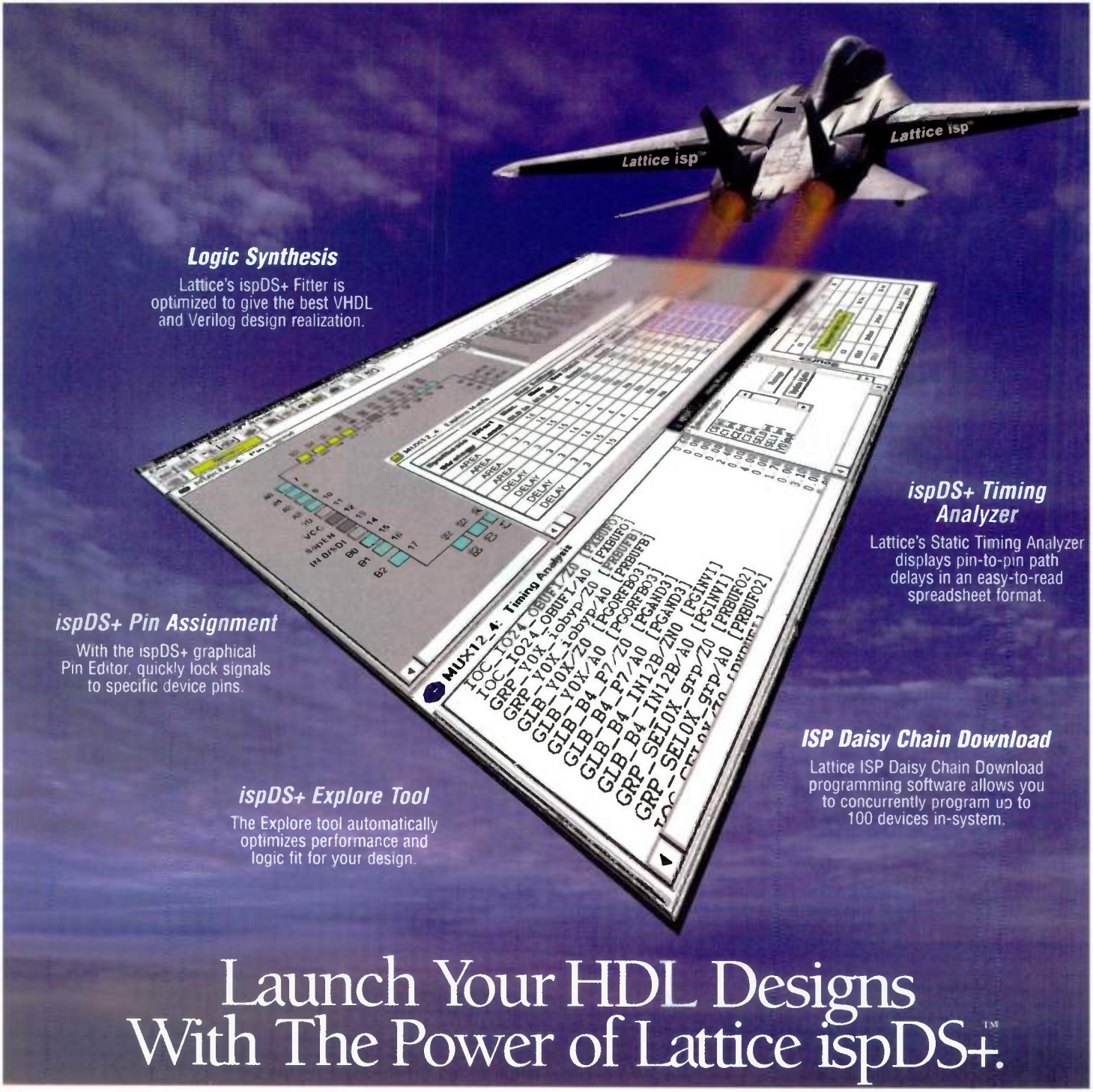

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Laser Transmits Data Over 206-Wavelength Information Rainbow

Using a single laser to generate light pulses each lasting just 100 millionths of a billionth of a second, reseachers at Lucent Technologies' Bell Labs (Holmdel, N.J.) were able to transmit data, in ones and zeros, over 206 wavelengths, or colors, of light. This represents the largest number of communications channels ever generated.

To accomplish this feat, the researchers used wavelength-division multiplexing (WDM), which is the transmission of data over multiple wavelengths. WDM is generally acknowledged as the transmission technology of next-generation communications systems. Each wavelength adds a transmission lane to the information superhighway. The more lanes there are, the more traffic (e.g., voice, data, video) can be carried on a single fiber.

Lucent's team strayed from convention to launch multiwavelength lightwave signals for WDM transmission by using a femtosecond laser transmitter and a novel data-encoding scheme. Such a laser was chosen because the technique requires an extremely broad color spectrum and a short optical pulse width.

The femtosecond light source is a modelocked, or pulsed, laser made of a length of optical fiber containing erbium. Each color, or channel, in the experimental system carries 36.7 million bits of information per second. For further information, surf into Lucent Technologies' web site at: http://www.lucent.com. *RE*

Digital Watermarking Prevents Illegal Audio Duplication

An information embedding technology that allows special digital signals to be hidden in audio information-- much like watermarking on paper--is aimed at protecting the information against unauthorized duplication. Based on work done by Solana Technology Development Corp., Solana Beach, Calif., and Spatializer Audio Laboratories Woodland Hills, Calif., two similar technologies have been developed. Electronic DNA (E-DNA) can embed indelible, inaudible information into a digital or analog audio source. An advanced version called E-DNAc allows information to be embedded directly into compressed digital audio signals and to be recovered after decompression.

The need for information embedding continues to grow due to the interest in direct delivery of copyrighted audio material over the Internet and other online services. The potential for unauthorized duplication is huge since each copy of audio material could become a digital master for illegal duplication. E-DNA addresses the problem by giving content providers a means for tracing each copy of copyrighted material back to its source or original recipient.

Information embedded by E-DNA can't be removed or altered without significantly degrading the audio content. The embedded data becomes a part of the audio signal and doesn't require a separate signal or additional bandwidth. Typical user information includes copyright notices, time stamps, purchasing data, and serial numbers. For further information, call (619) 259-2783, ext. 1104. *RE*

International Telephone Numbers Now Can Handle 15 Digits

The International Telecommunications Union (ITU) has advised all telecommunications administrations that their telephone networks and switches should now be able to handle up to 15-digit international telephone numbers. Up to this point. most switches were limited to 12 digits or less. Now some carriers, including Finland, Germany, and Iridium (a new global mobile satellite system provider) are already introducing 15-digit numbers.

Such switch changes are necessary to ensure the continued flow of traffic between countries. Implementation date for the first changes was December 31, 1996. The complete timetable for network changes is in ITU-T Recommendations E.165 and E.162.

Without the network changes, a situation would exist in which countries calling carriers needing 15 digits would not be connected, and routings from such 15-digit carriers would have to be handled by an operator. It's understood by the ITU's Telecommunication Standardization Bureau that the first changeover, which carried a 10-year notice, went smoothly in most countries. ITU-T Recommendations can be found on the Web at http://www.itu.ch. *PMcG*

ADC Built With CMOS FETs Lowers Cost, Not Performance

A new concept in analog-to-digital-converter design uses n- and p-channel CMOS field-effect transistors (FETs) to replace the conventional resistive R-2R ladders in such devices. Its designers at the Swiss Federal Institute of Technology, Zurich, Switzerland traded off a number of variables to construct the converter, which offers a fast sampling rate of 200 MHz and 12-bit integral nonlinearity.

While not the fastest or most precise device of its type, it can be fabricated at low cost because of its unique design, small chip area (1490 x 1946 mm2), and low power consumption. Intended for audio and telecom applications, the converter is built on a 1-µm CMOS process and draws just 2.4 mA at a 5-V supply voltage. Another advantage of the device is that it needs no trimming or calibration of any kind. *FG*

Video Camera Brings A 360° Undistorted, Linear View To TV

The literal impossibility of seeing "like you've got eyes in the back of your head" now could, from a technical purview, become more of a reality. A video camera developed by Shree K. Nayar at Columbia University's School of Engineering and Applied Science, New York, N.Y., can see in all directions at once. Such a camera, if placed atop a concert stage or at midfield of a sports event, could provide a 360° view—an entire sphere—to television viewers. A set-top box and joystick could bring any frame of that view to their screens. Instead of getting a hemispheric perspective, they would see normal, undistorted, linear perspective. In fact, on-screen windows could be created to see several views simultaneously.

Dubbed "Omnicam" by Nayar, the video camera uses a small parabolic mirror to obtain hemispheric views. A miniature video camera mounted in a frame is aimed at the apex of the parabolic mirror—a small inverted cup of polished metal enclosed within a transparent hemisphere. Software created by Venkat Peri, a graduate student, allows multiple Omnicam images to be displayed on a computer screen in linear perspective at any magnification.

So far the laboratory has come up with four prototypes, with different configurations for surveillance, teleconferencing, entertainment, and robotic vision. Two Omnicams mounted back-to-back can produce views of 360°, a complete sphere, for surveillance or security operations. For teleconferences, every participant seated around a table can be shown in a hemispheric or linear perspective. In addition, it allows a mobile robot to determine its location and direction of travel from local features. Because the camera views itself at the parabola's apex, there's one small blind spot in each hemisphere. For further information, or to see an on-line demo, call up the laboratory web site at http://www.cs.columbia.edu/CAVE. *RE*

Joint Effort Produces Satellite-Based Mobile Data Network

Racotek Inc., Minneapolis, Minn., and Caterpillar Inc., Peoria, Ill., combined to develop a prototype of a satellite-based mobile data-communications network. What's so unique is that it's designed to monitor and relay location and diagnostic information from Caterpillar equipment (Caterpillar manufactures construction and mining equipment) in use anywhere in the world to its corporate information systems and dealers.

Caterpillar selected Racotek to provide the system-design architecture and operating-system software, including elements of Racotek's KeyWare software. This provides two-way information flow between systems on Caterpillar equipment in the field, through the ORBCOMM satellite network, to Caterpillar's extended information systems. The companies developed this open software architecture to allow for the consistent use of the software application should system components or services require modification.

For more information, contact Racotek at (612) 832-9800, or Caterpillar at (309) 675-9984. *RE*

CTIA Seeks FCC Opinion On Local, State Authority Over Sites, Fees

Alleged abusive activities engaged by state and local governments when wielding their regulatory authority over matters of wireless system sites and fees has been brought to the attention of the Federal Communications Commission (FCC). The Cellular Telecommunications Industry Association (CTIA) has asked the FCC for a series of declaratory rulings on these abuses that are thwarting the build-out of a national wireless telecommunications infrastructure.

Says Thomas E. Wheeler, president of CTIA, "After receiving billion in wireless auction revenues, it is incumbent upon the Federal government to exercise its preemptive authority to assure that the provision of wireless service to consumers is not hamstrung by local politics." Abuses cited by the CTIA include:

RF emissions: One New England state requires the State Public Health Service commissioner to issue a report and recommend regulations for RF emissions, a matter clearly preempted in Federal law.

RF environmental impact: One Pacific Northwest county's denial of an antenna siting was based upon a hearing record that dealt mostly with the environmental effects of RF, which is also preempted by Federal law.

Unreasonable taxation: A Florida city is proposing to impose annual $40,000 payments for each permit for each monopole, even if the pole is part of an existing utility pole program (such as for power distribution), a matter that the Federal government has had preemptive authority since 1934.

Lengthy moratoria: A West Coast city adopted a year-ling moratorium (enforced by jail terms) on the acceptance and processing (not just the granting) of applications for antenna while the planning commission conducted a study. The inability to even request approval prohibits the entrance of new wireless competitors in clear contravention of Federal policy establishing competitive wireless service.

Extortion: One East Coast city demanded, as a condition to receiving a license to operate in the city, a wish list of goods and services, such as the provision of service at 20% below the lowest price charged to any customer.

For further details, contact the CTIA at (202) 785-0081 or (202) 736-3207; fax (202) 467-6990. *RE*

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- 8-pin DIP, SO-8, MSOP-8 Surface-Mount
- **INA126** is priced from **$1.60** in 1000s.

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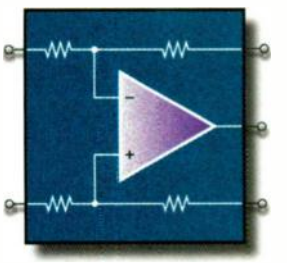

INA132 is a microPOWER, unity gain difference amplifier consisting of a precision op amp with a precision resistor network. On-chip resistors are trimmed for accurate gain and high common-mode rejection. The internal op amp's common-mode range extends to the negative supply—ideal for single-supply applications.

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- Gain Error ..... ±0.075%
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- High CMR ..... 120dB at G=100
- 8-Pin Plastic DIP and SO-8
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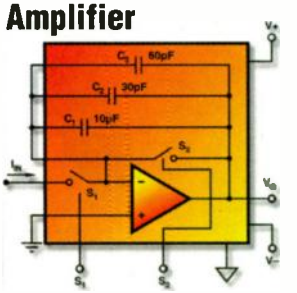

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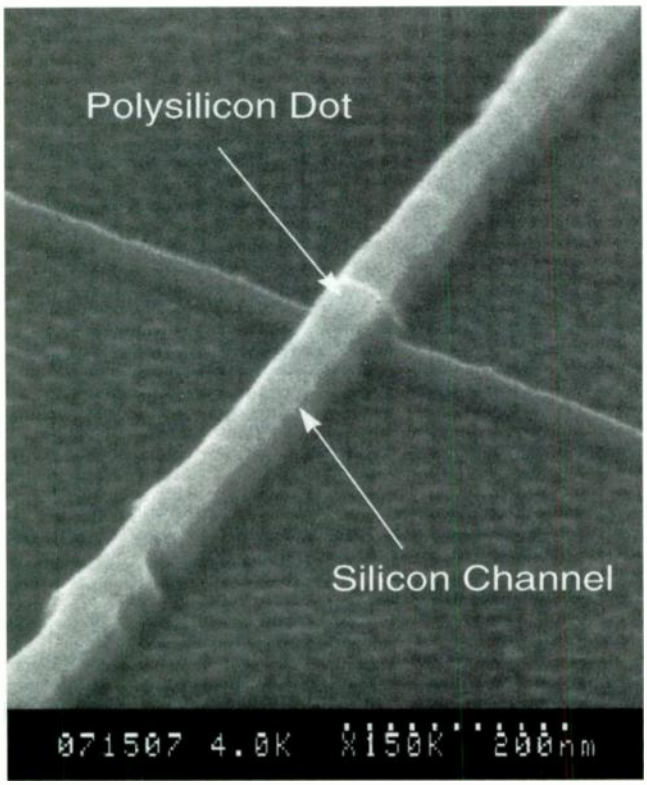
Single-Electron MOS Transistor Holds Promise For A Tiny Memory Cell

A single-electron MOS memory in which a bit of information is stored at room temperature has been developed by researchers at the University of Minnesota, Minneapolis. The nanoscale device with a floating gate and a narrow channel holds promise of increasing the storage potential of a memory chip by two to three orders of magnitude for the same silicon area, power consumption, or fabrication cost.

"The only way to make an IC powerful is to put more transistors in it and make each transistor operate faster," explains electrical engineering professor Stephen Chou, the principle investigator in the MOS memory development. "So the size of each transistor must be reduced. A smaller memory cell also leads to a faster speed and a lower power consumption," he adds. Working with Chou on this project are Lingjie Guo and Effendi Leobandung of the Nanostructure Laboratory at the University's Dept. of Electrical Engineering.



1. A single-electron MOS memory with a narrow silicon channel and a nanoscale polysilicon dot as the floating gate (a). The control oxide layer between the dot and the control gate is not shown. A cross section of the floating gate and the channel region (b).

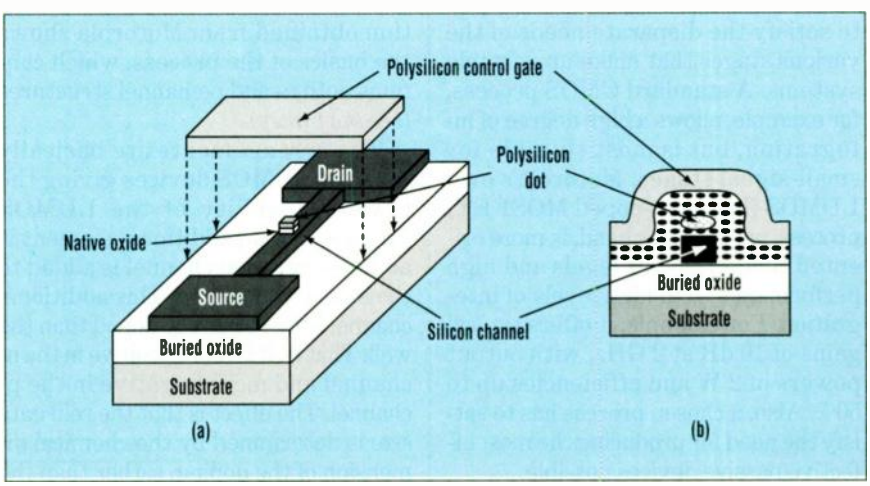
Previous single-electron MOS memories had to have nonconventional structures (e.g., a polysilicon channel or a floating gate consisting of many isolated silicon nanocrystals) with resultant large fluctuations in device dimensions and performance. The new device, on the other hand, is said to be the first single-electron MOS memory with a very narrow crystalline silicon channel and a nanoscale polysilicon floating gate with well-controlled dimensions *(Fig. 1)*.

To make the device, 35-nm-thick silicon channels, with widths varying from 25 to 120 nm, are fabricated on a silicon-on-insulator (SOI) substrate using electron-beam lithography and reactive-ion etching. Next, square-shaped polysilicon floating gates, called dots, are deposited and patterned using second-level electron-beam lithography as well as reactive-ion etching *(Fig. 2)*.

The size of the gate is nearly the same as the channel width whose initial thickness is 11 nm. An 18-nm-thick oxide layer is then thermally grown on the structure, consuming silicon and reducing the thickness of the polysilicon dot by about 9 nm, as well as the lateral size of the dot and the silicon channel with by about 18 nm. This is followed by depositing a 22-nm-thick oxide, using plasma-enhanced chemical-vapor-deposition (PECVD) techniques, giving the total control oxide of 40 nm. A 3-μm-wide polysilicon gate that covers the small floating gate and part of the narrow channel is deposited and patterned.

After final contacts were made, the devices were sintered to reduce interface states. No tunnel oxide was intentionally made between the channel and the floating polysilicon gate. However, the potential barrier still exists due to the grain boundary and a thin native oxide.

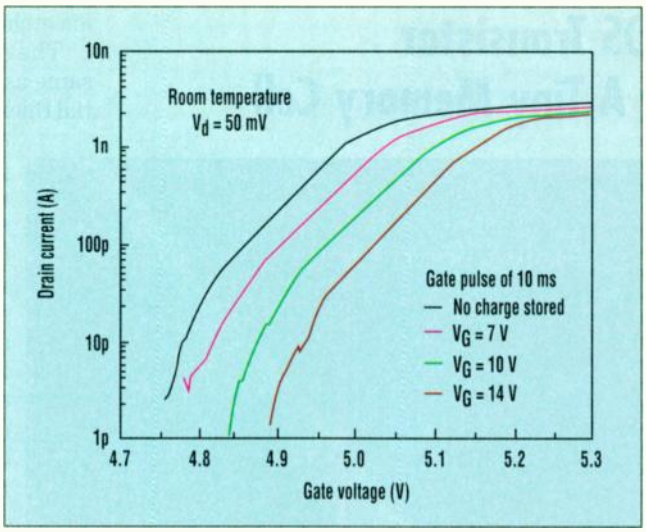
Characterization was performed at room temperature in a two-step process. First, a voltage pulse relative to the grounded source was applied to the control gate (at a drain-source voltage, V_{DS}, of 50 mV), forcing the electrons to tunnel from the channel to the floating gate. Next, the single-



2. A scanning-electron micrograph of a 50-nm-wide silicon channel and 50-nm polysilicon dot on top, before size reduction by thermal oxidation. Line in the buried oxide are due to second-level electron-beam lithography and have no effect on device behavior.

electron memory's drain current was measured as a function of the gate voltage (the same V_{DS} of 50 mV), resulting in the threshold-voltage (V_{th}) shift. A simple switching circuit was used to ensure that the second step occurred within one second of the first step.

The I-V characteristics of a single-electron memory (with a channel width of about 7 nm, and a 2-nm-thick 7-by-7-nm square floating gate) showed that despite the fact that the charging voltage is continuous from 2 to 14 V, V_{th} always takes a discrete shift in 55-mV increments *(Fig. 3)*. (The dimensions of the channel and the floating gate are estimated from scanning-electron-microscope measurements and by the oxidation rate, but indeed may be larger due to self-limiting oxidation.)



3. Transfer characteristics of a single-electron memory before and after charges are stored onto the floating dot. Threshold voltage shift is quantized in 55-mV increments.

A staircase relationship exists between the charging voltage and V_{th}, with each threshold shift corresponding to a charging-voltage range of about 4 V. Moreover, for a given charging voltage, the threshold shift is self-limiting—V_{th} is independent of the charging time.

According to its developers, the behavior of the novel device can be explained by the single-electron charging effect in three ways. First, since there is little oxidation between the channel and the floating gate, the charging voltage primarily drops between the control gate and the floating gate. The capacitance of the 7-by-7-nm floating gate and a 40-nm control oxide is 4×10^{-20} F, which gives a single-electron charging voltage of 4 V.

Second, the shift in the memory's threshold voltage due to a single electron stored in the floating gate, estimated from a single-electron Debye screen length, is 51 mV. Third, the self-limiting charging process is a result of raising the potential in the floating gate due to single-electron charging, a large Coulomb energy level spacing, and a thin barrier layer. All these estimations were found to be consistent with experimental results.

For more information, contact professor Stephen Chou via e-mail at: chou.ee.umn.edu.

Roger Allan

Advanced MOSFET Process To Blend High Levels Of Integration With High Speeds

Motorola Semiconductor, Phoenix, Ariz., looked at the problems associated with integrating the RF stages of portable devices and concluded that a new approach is needed to satisfy the disparate needs of the various stages that make up portable systems. A standard CMOS process, for example, allows a high degree of integration, but is most suitable for small-signal stages. Motorola's own LDMOS (laterally-doped MOSFET) process, on the other hand, is more oriented to high-power levels and high performance than high levels of integration. For example, it offers typical gains of 10 dB at 2 GHz, with output powers of 2 W and efficiencies up to 50%. Also, a chosen process has to satisfy the need for producing the most effective passive devices possible.

A solution is now under development which will lead to devices later this year. Details of the new process being called GCMOS (graded-complementary MOSFET) will be presented in a paper at the IEEE's MMTS Conference in Denver, Colo., June 8 through June 13. Advance information obtained from Motorola shows the basics of the process, which contains both n- and p-channel structures *(see the figure)*.

The arrangements are basically those of LDMOS devices giving the power capability of the LDMOS process. But an additional element is added—a graded channel is added to the side of the source. This additional channel is more heavily doped than the well. That is, it is more positive in the n-channel and more negative in the p-channel. The effect is that the real gate size is determined by the chemical dimension of the doping, rather than the mechanical dimension of the process. This design allows for more different electrical characteristics than the traditional LDMOS structure. The graded channel operates in the enhancement mode at the source side, and the remainder at the drain side operates in the depletion mode.

Compared to the same structure with a uniformly-doped channel and the same gate length, the GCMOS process has a higher drain current (I_d) and lower capacitance, giving, of course, a higher speed. In a low-noise-amplifier configuration with the process, Motorola is achieving gains of about 21 dB with 3.0 mA of I_d, and a drain-source voltage (V_{ds}) of 2.7 V. Noise figures are below 1.5 dB at most currents.

In a 900-MHz down-converter with a cascode low-noise amplifier and a cascode mixer, overall gain is 26 dB with a noise figure of 1.8 dB. A 900-MHz, 2-W integrated power amplifier has the characteristics of a LDMOS circuit with gains up to 30 dB and efficiencies up to 55%.

The narrower gate reduces the breakdown voltage of the devices, which are really intended only for use in lower than 3-V circuits. In addition

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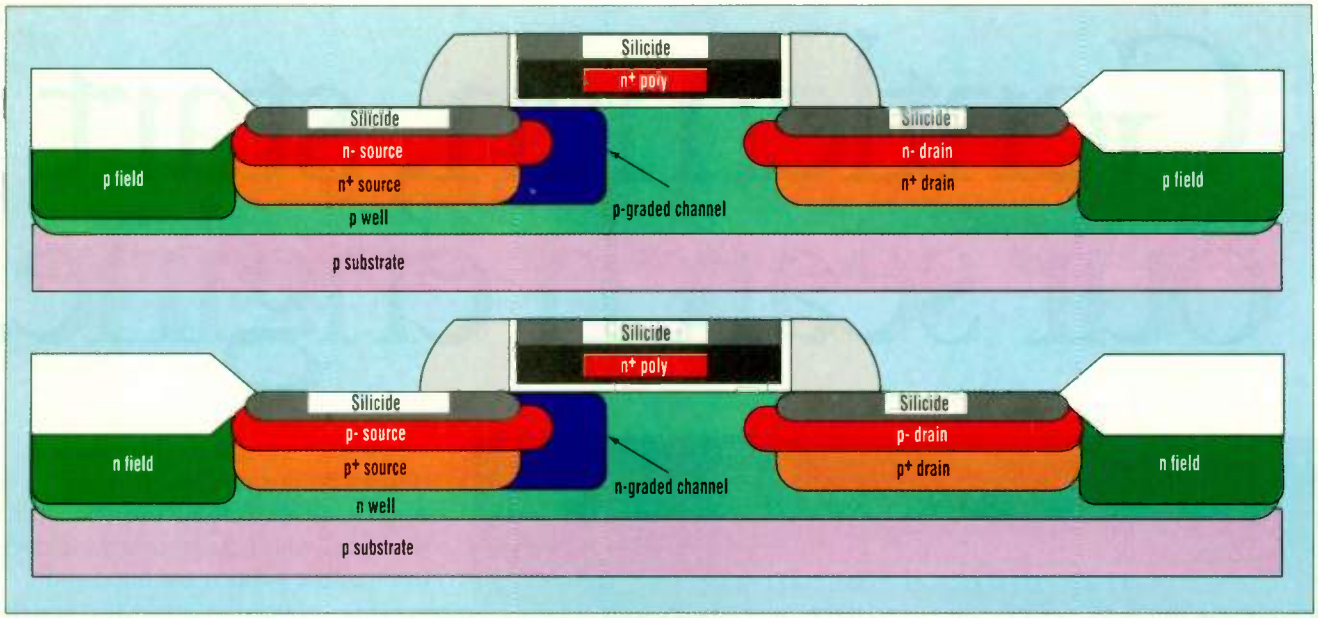

N-channel-unilateral (top) and p-channel-unilateral (bottom) cross-sections in the Motorola GCMOS process. They allow mixing the small-signal benefits of CMOS with the power capabilities of LDMOS processes.

to the complementary MOSFETs, capacitors, both shunt and series, can be formed with Q factors of about 55 at 900 MHz and values of more than 1 fF/μm≈. Resistors can be from 260 Ω to 1.5 kΩ/square, and inductors can be fabricated from 2 to 15 nH, with Qs up to 7 at 900 MHz.

For more information, contact Motorola Semiconductor at (800) 441-2447.

Paul McGoldrick

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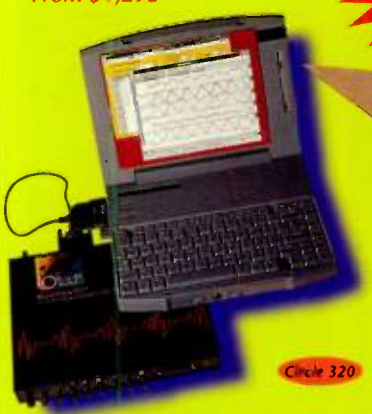

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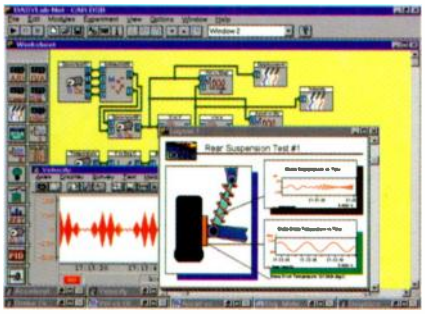

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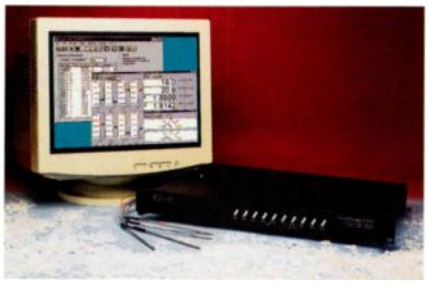

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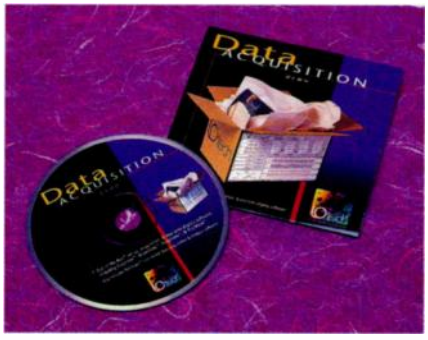

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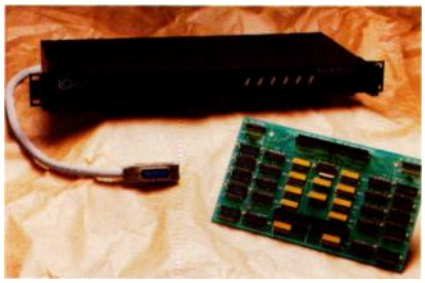

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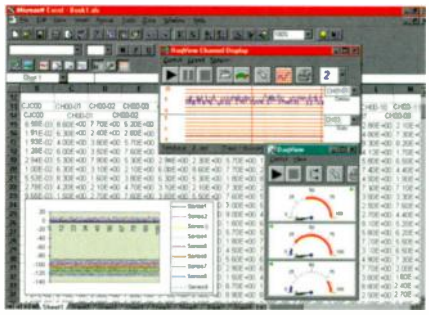

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The Ten Commandments Of Excellent Design

Instability And Unreliability In Synchronous Systems Can Be Avoided By Rigorously Following These Design Rules.

PETER CHAMBERS VLSI Technology Inc., 8375 South River Pkwy., Tempe, AZ 85284; (602) 752-6395; e-mail: peter.chambers@vlsi.com.

This article is the first of a two-part series written to offer some pointers for designing synchronous circuits that work the first time. Take note of the ten commandments that always should be followed! Part two of the series will appear in an upcoming issue,and will provide VHDL-code examples to support ideas discussed here.

Synchronous digital systems are pervasive in today's designs. Engineers create clocked circuits for every conceivable application, with frequencies ranging from dc to GHz. Every synchronous system has certain common characteristics, and is prone to a group of common faults that can cause instability and unreliability, and may not be uncovered in the typical design process. The net result is a poor product that fails to meet the design criteria.

Poor design results require the engineer to endure costly and time-consuming design modifications and revisions. However, by applying a few simple rules, designers can avoid synchronous faults in designs and achieve consistent first-pass success.

Digital Systems 101

We'll begin by describing a typical synchronous circuit *(Fig. 1)*. Many variations are possible, but a simple, one-clocked element example, showing the circuit and timing, will adequately illustrate the sources of error.

With such problems, why use synchronous logic? Wouldn't asynchronous logic be faster? The answers could fill a book, but here are some reasons to use synchronous design:

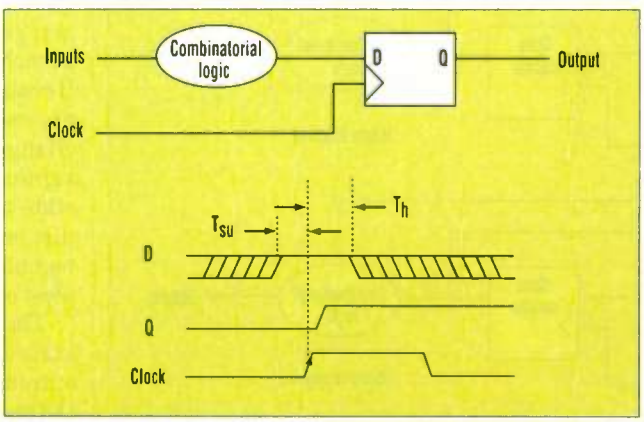
- Synchronous designs eliminate problems associated with speed variations through different paths of logic. By sampling signals at well-defined time intervals, fast paths and slow paths can be handled simply.
- Synchronous designs work well under variations of temperature, voltage, and process. This stability is key for high-volume manufacturing.
- Many designs must be portable. In other words, they must be easily migratable to a new and improved technology (for example, moving from 0.6 µm to 0.35 µm). The deterministic behavior of synchronous designs makes the process of moving to a new technology very straightforward.
- Interfacing between two blocks of logic is simplified by defining standardized synchronous behavior. Asynchronous interfaces demand elaborate handshaking (or token passing) to ensure integrity of information. However, synchronous designs with known timing characteristics can guarantee correct reception of data.

Synchronous circuits are made with a mixture of combinatorial logic and clocked elements, such as flip-flops or registers. The clocked elements share a common clock, and all transition from one state to another on the rising edge of the clock. When the rising edge occurs, the registers propagate logic levels at their D inputs to the Q outputs.

Figure 1, defines two important timing parameters:

- Setup Time (T_{su}): Setup time is the time that a register's D input must be valid before the clock transitions.
- Hold Time (T_h): Hold time is the period that a register's D input must be valid after the clock has transitioned.

If the setup- or hold-time parameters are violated, terrible things happen. We'll discuss this later in the section on synchronization.



1. This simple circuit introduces the notation and timing parameters for a D-type flip-flop, which is the basic element of synchronous circuits.

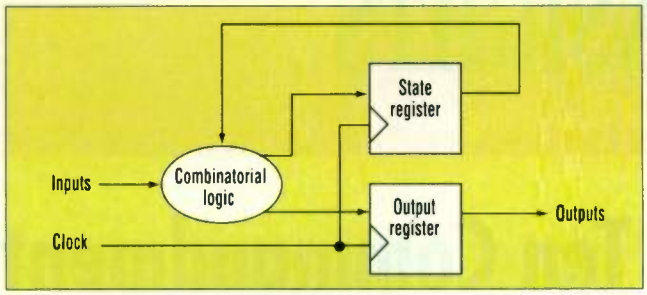
Clock Distribution

The distribution of clocks throughout a design has received considerable attention with the increase in logic speed. Common personal computers have bus speeds of 66 MHz, and processor clocks

run at 150 MHz or greater. In this article, we're concerned more with the possible pitfalls in the synchronous logic itself, not with the production of decent clocks. However, here are the important parameters needed for a good clock distribution system design:

•Skew Minimization: Clock skew is the variation in time of the clock's active transition being detected by different devices within a system. Skew must be kept to a minimum to ensure that setup and hold times are not violated at any one device. Methods for managing skew include equal-length traces, zero-delay PLL-based buffers, and additional logic for extending hold times.

•Clock Fidelity: The clock's waveform must be as clean and deterministic as possible. Techniques used to guarantee consistent clock behavior include transmission-line termination, ground-bounce minimization, and the use of identical clock drivers.



3. A better state machine registers the outputs as well as the current state. That way, it's possible to produce glitch-free outputs for latch control, register loads, and tristate enables.

Good State Machine Design

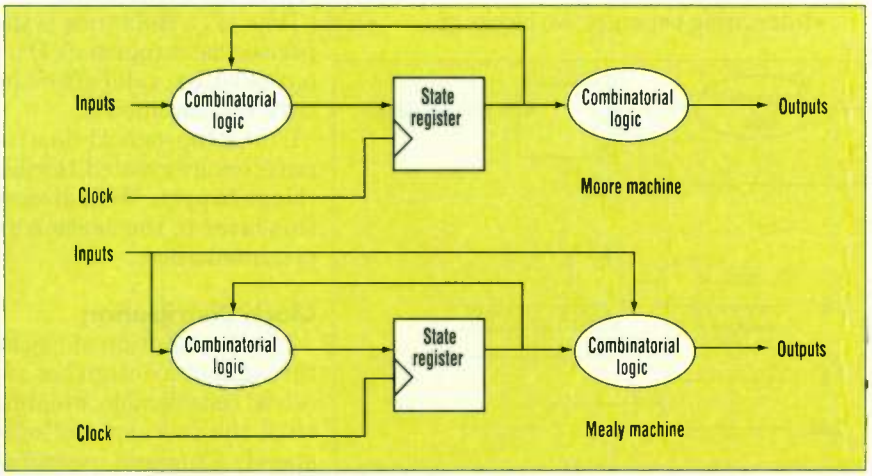
One of the designer's most powerful constructs for synchronous design is the state machine. By combining combinatorial logic and a number of registers, the state machine makes decisions based on its inputs and its current state. The behavior of the state machine is entirely synchronous, with all decisions made at the time of the clock transition. There are two conventional forms of state machines: Mealy and Moore *(Fig. 2)*.

Moore machines are the simpler of the two standard types. Their output is a function only of the current state of the machine. The outputs of Mealy machines are a function of the current state of the machine plus the inputs. This additional path provides more flexibility, but may complicate the understanding of the machine.

Books on high-level design languages (HDLs) expound at great length on the construction of state machines. But the results are frequently disappointing. Defining a state machine in an HDL and running the design through a synthesizer could produce spaghetti logic that no self-respecting designer would ever put together.

Mealy/Moore Drawbacks

Moore state-machine outputs are combinatorial decodes of the current state, and Mealy state-machine outputs are combinatorial decodes of the current state and the inputs *(Fig. 2, again)*. While this arrangement is fine in principle, there are pitfalls here waiting to trap the unwary.



2. The characteristics of our old friends, the Mealy and Moore state machines, are shown in this diagram. Their behavior is entirely synchronous.

The outputs of the state machine may include the following types of functions:

•Latch enables (low- or high-going pulses to open or close latches)

•Tristate enables (signals turning drivers on and off to on-chip or off-chip buses)

•Register enables (enables for synchronously-clocked registers)

•General control signals, such as counter enables, flags, and others.

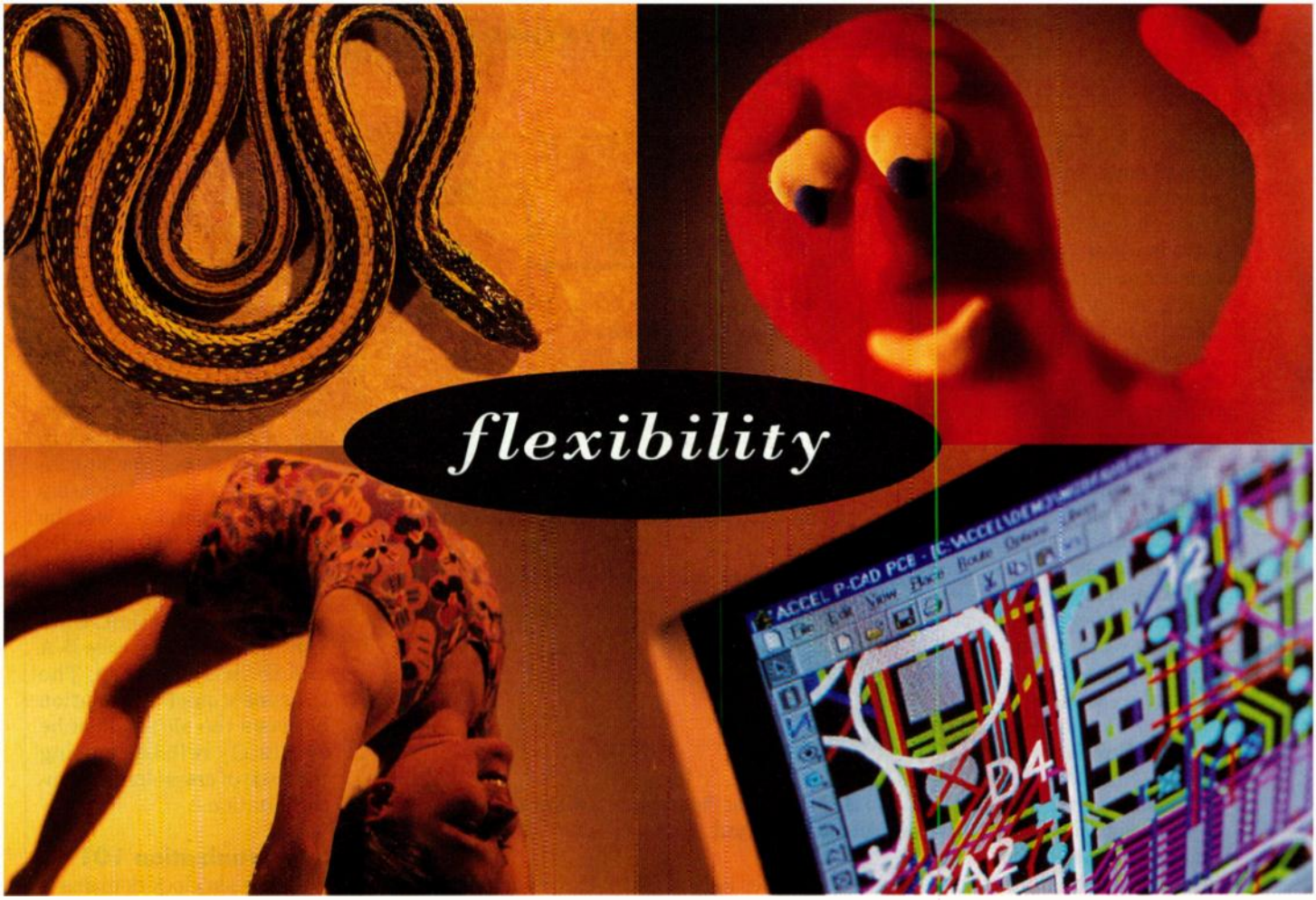
Most of these signals have one characteristic in common—glitches are absolutely unacceptable at any time. As the state registers and inputs of the Mealy or Moore state machines transition and settle, the combinatorial gates are capable of generating glitches as a consequence of the varying gate propagation delays. These transitory glitches may well contain enough energy to open latches, clock registers, and cause other highly-undesirable effects.

What About Gray Code?

We all learn early on that gray code counters are wonderful because only one bit changes at a time. When fed to an asynchronous decoder, theory suggests that the outputs should settle to their new state without noise. I'm suspicious of this when the implementation is created by synthesized logic; unclocked feed-forward paths might well negate the advantage of gray code.

There is, however, a greater challenge to the use of gray code. The sequence of transitions taken by a state machine as it operates is likely to be quite elaborate. Many state machines are very complex, with numerous branches between the possible states. Because gray-code-driven decodes are only glitch-free when a single bit changes at each clock edge, the designer must ensure that all possible state transitions result in a change in just one bit of the state variable. This technique is practical in only the simplest of state machines.

There is a much better design for a state machine *(Fig. 3)* By adding an output register (with cleanly-clocked D-type flip-flops) that's reloaded at each clock edge, the outputs of the state machine are guaranteed to be



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glitch-free. It's suggested that all state machines be implemented in this form, because the quality of the outputs is independent of the number of states or outputs.

Reset signals are traditionally asynchronous, and are routed directly to the clear inputs of state-machine register elements. When the reset is asserted, all registers (state and output bits) are cleared immediately. All well and good, but what happens when the reset is deasserted?

Consider a state machine that transitions from the reset state to another state directly after the reset is deasserted. If reset deasserts close to a clock edge, some of the state bits will assume their new states while others might not. The state machine ends up in an undefined error state.

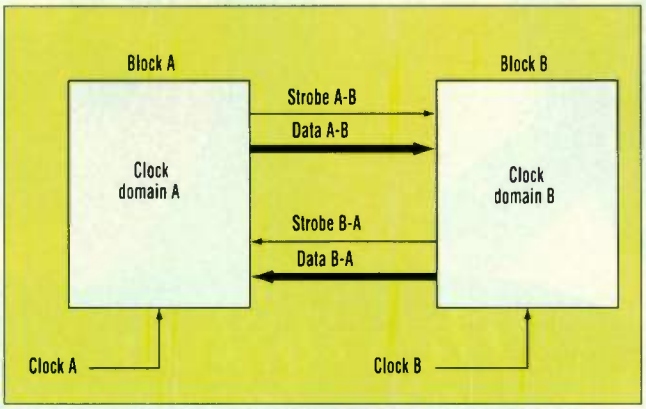
The solution? Synchronize that darned reset! That way, the reset will be removed well before the clock edge, and all register elements will correctly transition to their new states.

In fact, every input to the state machine must be synchronous. At the very least, be absolutely certain that no input will violate the setup and hold times of the state machine's state and output registers.

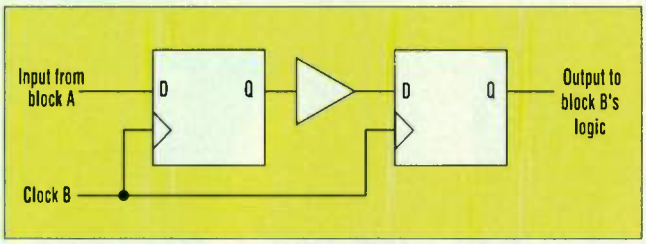
State machines with encoded state bits don't always use all possible states. For example, for a 20-state state machine, use a five-bit state register. This design leaves 12 unused state values. Because states are usually counted incrementally from zero, the example would use states 0-19 for normal operation, while states 20-31 wouldn't be used at all, hence the name dead states.

If the state machine ever enters states 20-31, errors are likely. Even worse, the machine may totally lock up, with the state machine forever in one of these illegal states. It may require a hard reset to recover from this condition.

Clearly, it's best to ensure your state machine never reaches a dead state. However, a robust design will at a minimum guarantee that if the state machine does enter a dead state, it will exit the dead state immediately, and then, perhaps enter a quiescent state.



4. In this environment, signals and data venture from one clock domain into another.



5. Two flip-flops provide the easiest way to synchronize an asynchronous input signal.

Crossing Clock Domains

Moving information from one clock domain to another is much like descending into Dante's inferno. All sorts of evils lie in wait to beset the naïve. Set-up and hold violations, metastability conditions, unreliable data, and other perils are manifest when moving from one clock domain to another. In fact, the whole issue of synchronization merits its own article. But these tips might help to resolve the block-to-block synchronization issues.

First, let's define the problem *(Fig. 4)*. Logic Block A operates with Clock A, while logic Block B operates with Clock B. No assumptions have been made about the frequencies of Clock A and Clock B, nor is it assumed that any integer or multiple relationship exists between the two; the two are totally independent.

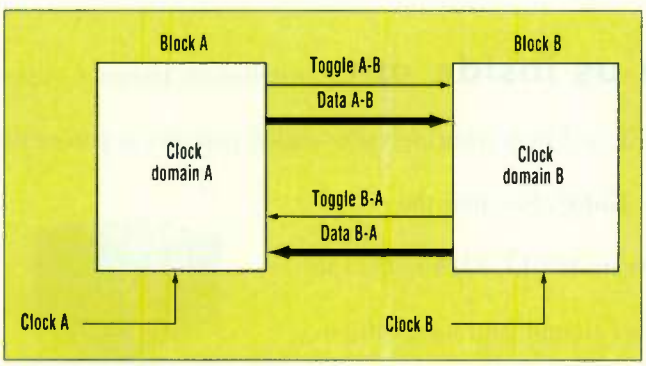
A strobe is sent from Block A to Block B (Strobe A-B), and some data is sent, Data A-B. In response, Strobe B-A and Data B-A return. The transmission of information between the blocks must be absolutely reliable, raising the issue of cross-domain synchronization.

Synchronization 101

Crossing between clock domains is an issue that's similar to managing asynchronous inputs. Because no relationship between the multiple clock domains can be assumed, the inputs from Block A to Block B must be assumed to be asynchronous inputs.

The traditional way of synchronizing an asynchronous input signal is as follows: two D-type flip-flops are used because two synchronization stages are usually sufficient *(Fig. 5)*. Only the rarest applications demand three stages of synchronization. If your silicon library supports metastable-hardened flip-flops, then the first stage should use such a device. Typically, metastable-hardened flip-flops guarantee that their Q outputs will settle after a given maximum time, no matter how close the data transition is to the flip-flop's clock edge.

This method of information interchange has one drawback. If the strobe has the form of a pulse, it may not be seen by the destination block if the pulse width is less than the destination block's clock (sampling) frequency. This design is not a problem if the two blocks exchange levels



6. Toggle signals provide an efficient, unambiguous way to carry information between clock domains. This figure shows how toggle signals qualify the data path between domains.

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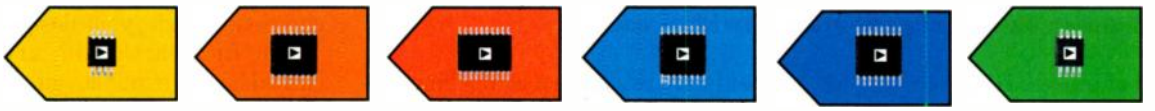

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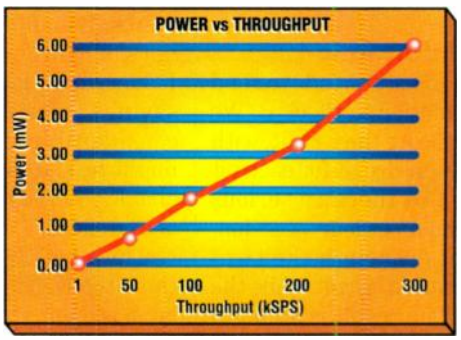

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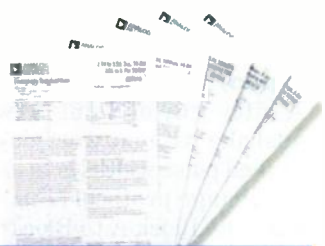

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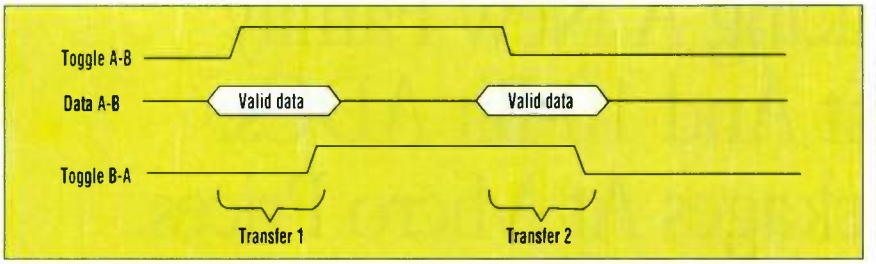

7. A toggle-signal timing diagram shows that pulses are not used to initiate data transfer. Instead, transitions (rising or falling edges) carry all the information.

instead of pulses. However, it's slow, typically as four level exchanges must occur for a two-way handshake. The toggle method described later is an excellent solution to this problem.

Single-Point Information

Imagine that Block A needs to send two bits of information to Block B. We could simply duplicate the circuit, with one synchronization circuit for each bit *(Fig. 5, again)*. But there's a serious problem that should be clear: occasionally, one bit gets through the two-stage synchronization circuit while the other does not. The result is ambiguous information and errors.

The solution is shown back in Figure 4—use a single strobe from Block A to Block B, and send the rest of the information separately. The single-point strobe from A to B informs the destination block that the Data A-B is valid, and the originating block ensures that there is adequate setup time.

Toggleo, Toggleas, Toggleat

A nifty way of doing a two-way handshake without worrying about levels and pulse widths is to use a toggle-exchange protocol *(Fig. 6)*. The signal from Block A to Block B, indicating the data (Data A-B) is valid, is a transition of the signal Toggle A-B. This transition may be low-to-high or high-to-low. Both transitions have the same meaning: the Data A-B bus is valid *(Fig. 7)*.

Each transfer is complete with only two events: a toggle of the two Toggle strobes. While each toggle must be synchronized carefully at the receiving end, this method guarantees successful transmission and reception of wide data busses across clock domains of arbitrary frequency. From GHz to KHz, the toggle method is predictable and reliable.

When creating a set of clocked elements, there's often a compelling reason to use latch-based designs. A single-bit register implemented with a latch may use just 60% of the gates that a conventional D-type flip-flop requires. If your design uses great numbers of configuration registers, FIFOs, or has elaborate data paths, the savings from using latches might be considerable. And the latch control might be the same signal as the clock enable to a D-type flip-flop, so why not use latches?

The latch's Q output is stable while the latch is closed *(Fig. 8)*. When the latch is open, the input is continuously copied to the output. Two potential pitfalls exist with latches:

- Noisy Inputs—Any glitches on the latch's D input are propagated directly through to the output. This design is, of course, manageable by ensuring that there aren't any glitches on the input. However, in a synchronous system, busses tend to switch states at clock edges, and the latch enable typically straddles a clock edge, requiring that the D input be perfectly clean right through the same clock edge. This is the worst time for switching noise, particularly on wide busses.

What's more, the latch needs the D input to be stable for two clock periods (so it's clean through the clock edge). Changing the D input with the same edge that closes the latch, produces a race that you're bound to lose (Murphy and his law).

- Noisy Latch Enable—Perhaps worse than noise on latch inputs is noise on the enable line. If a latch enable glitches as a result of an asynchronous decode, your design is toast.

The first part of this article discussed how to eliminate glitches on decoded signals. However, if you get it wrong, a register-based design is still likely to be robust because glitches on clock enables don't matter except when the clock transitions. But glitches on latch enables always mean instant death when they occur.

Registers Rule!

Register-based designs suffer from none of the disadvantages listed above. Race conditions are rare to nonexistent, glitches on the control or D signals are unlikely to cause harm, and signals can be reliably latched in one clock period. A register-based design may be larger than its latch-based equivalent, but it will be more robust and will contribute toward first-silicon success. Bottom line: If you absolutely have to use latches, beware!

The classic example of a race condition shows that the transition as the output of the first flip-flop changes might well violate the hold time on the D input of the second flip-flop *(Fig. 9)*. This situation can worsen if there is skew between the clocks to each of the two flip-flops. If flip-flop B's clock lags A's, then B's output might actually replicate the output of A, rather than

The Ten Commandments Of Excellent Design

1. All state-machine outputs shall always be registered.
2. Thou shalt use registers, never latches.
3. Thy state-machine inputs, including resets, shall be synchronous.
4. Beware fast paths, lest they bite thine ankles.
5. Minimize skew of thine clocks.
6. Cross clock domains with the greatest of caution. Synchronize thy signals!
7. Have no dead states in thy state machines.
8. Have no logic with unbroken-asynchronous feedback, lest the fleas of myriad test engineers infest thee.
9. All decode logic must be crafted carefully—eschew asynchronicity.
10. Trust not thy simulator—it may beguile thee when thy design is junk.

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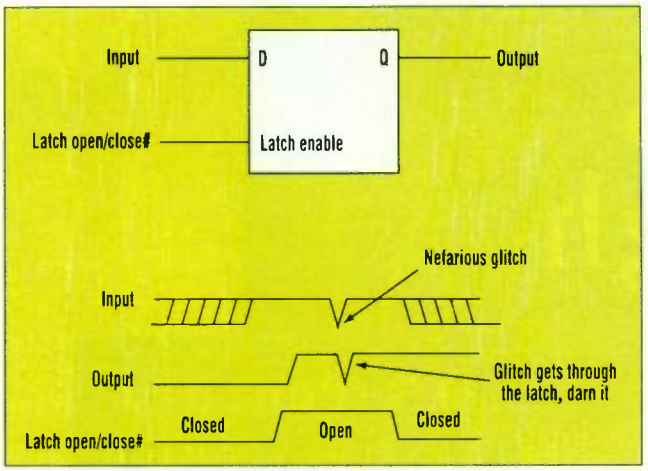
add the extra clock delay that is required.

A simple delay solves the fast-path problem *(Fig. 10)*. The delay element ensures that there is sufficient time for flip-flop B to complete its transition before the result of A's transition reaches B.

Some synthesizer tools have a fix hold option that claims to take care of this situation. But if your design fails, who gets the blame, the designer or some well-hidden option in a synthesizer? Check carefully for fast paths.

If all goes well, the chip will enter mass production and the world (or at least the shareholders) will rejoice. To get to mass production, the design must be testable. Because testability is a much-neglected aspect of many designs, these tips might help test engineers sleep better at night:



8. This diagram illustrates the workings of a basic, transparent latch. Propagation of glitches is a less-desirable feature of latch circuits.

Sympathy For The Test Engineer

•Break long counters into bite-size chunks. Counters require lots of test vectors to ensure that all bits toggle correctly, and that carry bits are generated as they should be. To keep the number of test vectors to a reasonable number, provide the ability to partition a counter into multiple, smaller (for example, four bits each) counters.

Provide visibility of the most significant bit of each stage. That way, the test sequence can verify that every counter stage works by observing the most significant bit's low-to-high and high-to-low transitions, and can reasonably conclude that the counter will work as a unit. You can use the partition-and-provide-visibility method to increase testability of any long, sequential piece of logic. Counters are discussed here because they're the most common example of this type of design.

•Asynchronous feedback paths are a federal offense. Even without considering the effect they have on a test engineer's disposition, logic that uses asynchronous feedback is generally bad for a number of reasons. It's hard to simulate; it may be dependent on voltage, temperature, and process. It also may be very susceptible to transients. Just as bad, it may be impossible to test on a fixed-frequency tester.

If there are unclocked feedback paths in your design, make sure that they can be broken and analyzed from the tester. Better still, get rid of them altogether.

It's tempting to say, "I'll just design it quickly, then find the bugs in simulation." But it's a bad idea that's doomed from the start. Simulators are notorious for hiding the quirky details of a design. Examples include:

•Clock Synchronization—Synchronizing flip-flops constantly battle metastability and glitching inputs. Their behavior is not even closely approximated by an average simulator. All you see is a clean transition at the clock edge. Crossing clock domains must always be correct-by-design from the earliest stages.

•Asynchronous Logic—Similarly, asynchronous logic is often simulated poorly. Certainly, fast paths and race conditions may be hidden. Some situations will determine (and optionally correct) hold-time violations, but this is not a universal panacea for correct asynchronous logic.

Correct-By-Design

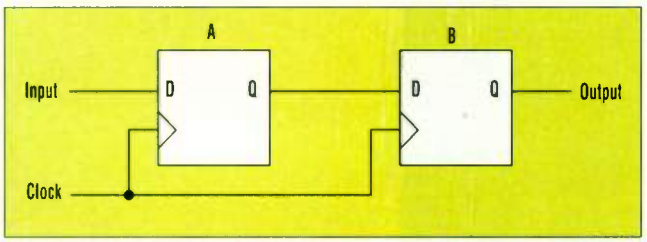
When designing logic that is outside the protected realm of clock-to-clock register-to-register implementations, the only solution for robust design is to do it right from the start. Logic must be:

•Correct by Design—Each gate, each line of VHDL, or each line of Verilog must be understood completely. Don't hope that simulation will find the bugs because you may neglect to test a part of the design. If it was designed sloppily, it will fail.

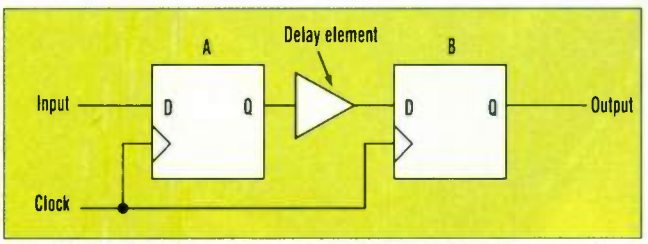
•Correct by Inspection—Disciplined layout also will make your design more robust, comprehensible, and maintainable. It should not be necessary to sort through a mass of ugly code or spaghetti gates to understand the operation of the function. Organized gates, commented code, and thorough accompanying documentation will provide a basis for a reliable design.

Peter Chambers is an Engineering Fellow in the Computer Products Division at VLSI Technology, Tempe, Ariz. He holds a BSc degree from the University of Exeter, England, and an MS from Arizona State University.

How Valuable	Circle
Highly	540
Moderately	541
Slightly	542



9. A simple circuit with two flip-flops shows the classic race condition in which the switching of flip-flop A violates the hold time of flip-flop B . If B's clock lags A's clock, then B's output may be incorrect.



10. The fast-path problem is easily solved with a delay element. Many synthesizers will insert the delays automatically, but they'll only work if the constraints are set up correctly.

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Networking Equipment And Downtime: Caught In The Middle

Understanding The Disparities Between NEC And IEEE Specifications Can Help Minimize Costly Power-Related Downtimes.

TONY DeSPIRITO, American Power Conversion, 132 Fairgrounds Rd., West Kingston, RI 02892; (800) 877-4080; fax (401) 788-2739.

In 1994, studies conducted by Contingency Planning Research and Stratus Computer revealed some alarming statistics. The results indicated that the total cost of computer downtime to U.S. businesses had climbed to an all-time high of over $3 billion. This staggering figure was further broken down into specific causes, from most prevalent to rare in occurrence. "Power-related problems" was the number one cause of computer downtime, amounting to over 45% of occurrences and resulting in losses of $1.5 billion.

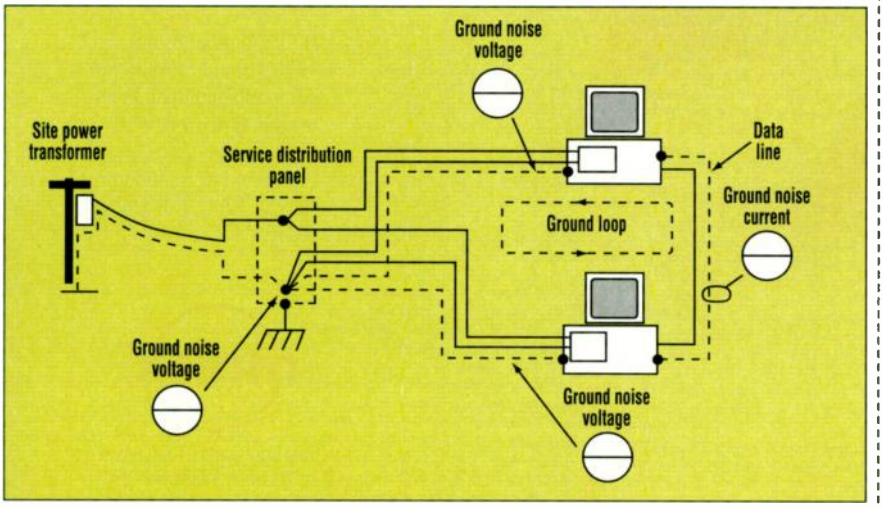
Many of the power-related problems can be traced to the most basic element of the computer network: The wiring and grounding of the host building. Several guiding principles are called into play when attempting to electrically support a computer network. The National Electrical Code (National Fire Protection Publication 70: NEC) is the exclusive reference source for the electricians performing the electrical work. Another standard, IEEE Standard 1100-1992, "Powering and Grounding Sensitive Electronic Equipment," better known as "The Emerald Book," is often more restrictive than NEC. And, in several cases, it is in direct contradiction to the NEC code!

Common Problems

Ever since the idea of attaching two computers together to communicate with each other arose, power events have manifested themselves in communication problems. When two or more computers are attached to each other, the primary means of attachment is via a copper wire. The Fiber Data Distributed Interface (FDDI) is becoming more popular, but the majority of today's networks are still attached via a copper-based medium. Due to basic electricity and magnetism principles, this copper wire can be the path for disruptive and potentially dangerous current and corresponding voltage events.

The gambit of electrical events manifesting themselves in downtime of a computer network range from nuisances such as intermittent reboots or lockups to dangerous, spark-producing power supply damage. Power supplies are not the only element of a server or workstation that are susceptible to these damaging events. Network interface cards (NICs), serial ports, parallel ports, and even modems are all prime targets for these destructive power events.

How do these power events happen? We have all seen the damage that a lightning strike can cause to an electrical distribution system. We also have seen the damage that occurs when a vehicle crashes into a utility pole. But what about "mixed loads" in an electrical panel? How about differences in ground-voltage reference potential? How about a haphazard grounding system in the building itself, where everything from building steel to a separate ground rod have been used as the "building ground?" Surely in this age of growing networking standards, there must be room for a "single reference manual" *(Fig. 1)*.



1. An ideal interconnected system has power lines for computer equipment.

Governing Standards

Two primary standards must be taken into consideration when planning or installing the electrical distribution infrastructure of the building. These two standards also will play a critical role in determining the performance of the installed computer equipment. The NEC, or simply "the Code," is the primary reference source used by electricians across the U.S.

Article 90-1 (b) on the opening page of the Code states that the "purpose of the Code is the practical safeguarding of persons and property from the hazards arising from the use of electricity." It further states that the "Code contains provision considered neces-

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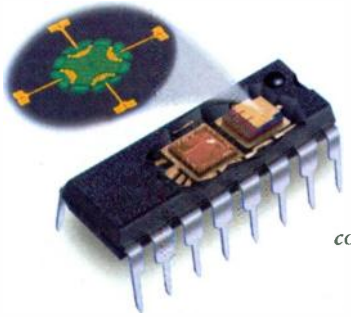

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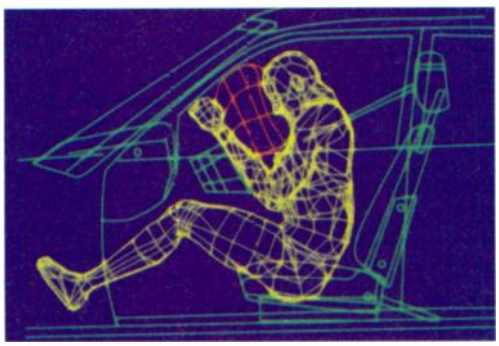

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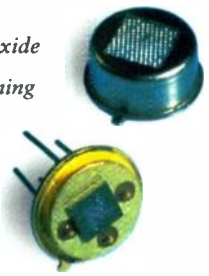

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MGSF1N03L	30	N	0.090	0.135	750	NOW	NOW
MGSF1P02L	-20	P	0.350	0.500	750	NOW	NOW
MGSF1P02EL	-20	P	0.160	0.200	750	Q1 97	Q2 97

			$r_{DS(on)}$ MAX at VGS = (W)				Samples		Production	
Device	VDS(V)	Type	+10V	+4.5V	+2.5V	ID(A) @ 4.5V	V	X	V	X
MGSF3454V/X	30	N	0.065	0.095	-	3.4	Q2 97	NOW	Q2 97	Q1 97
MGSF3455V/X	-30	P	0.100	0.190	-	2.5	Q2 97	Q1 97	Q2 97	Q2 97
MGSF3442V/X	20	N	-	0.070	0.095	4.0	Q2 97	Q1 97	Q2 97	Q2 97
MGSF3441V/X	-12	P	-	0.100	0.135	3.3	Q2 97	Q1 97	Q2 97	Q2 97

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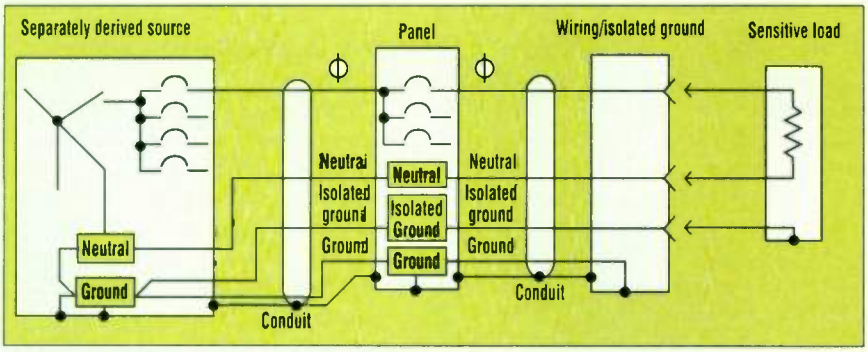

2. Proper grounding should consider insulated grounds and conduit connections.

sary for safety. Compliance [with] will result in an installation free from hazards but not necessarily efficient, convenient or adequate for good service."

The Institute of Electrical and Electronics Engineers (IEEE) has published IEEE Standard 1100-1992: IEEE Recommended Practice for Powering and Grounding Sensitive Electronic Equipment. The main purpose of this standard is to present "recommended engineering principles and practices for powering and grounding sensitive electronic equipment." The standard attempts to provide a consensus about what specific installation practices, relative to the electrical distribution system, should be used to afford the electronic equipment maximum availability.

With both of these standards to refer to, one would think that installations with computer networks would not have problems with the electrical distribution system. Several pieces of evidence point quite to the contrary. First, as mentioned earlier, in a study done by Status Computer in 1994, the total cost of "Downtime to U.S. Businesses" was approximately $3.4 billion dollars. Again, as previously mentioned, concurrent with the Stratus Computer study, Contingency Planning Research "drilled-down" on the causes of this downtime and found that in over 45% of the downtime occurrences, the cause was a power problems.

Another thing that may dispel the myth of adequate and sustained power in computer installations is that U.S. electricians are required to know and wire to the standards put forth in the Code. They are not required to know or even acknowledge the existence of the IEEE standards. This fact would be acceptable if inconsistencies between the Code and the IEEE standards did not exist.

Discontinuity

When examining the IEEE and NEC specifications on powering a network, we find several different types of discontinuities. In all areas, the IEEE specifications are more stringent than those contained in the NEC. On a few occasions, the IEEE specification is either omitted or ignored by the NEC. For purposes of discussion, the four main areas of discontinuity will be briefly explored:

The Shared Neutral

The proliferation of computers and the persistence of their nonlinear loads has made our first discontinuity an expensive and often dangerous one. Nonlinear loads do not draw current in phase with the voltage waveform. As a result of this current draw, resultant current sent back to the source on the neutral wire is additive. (A linear-load's resultant current will cancel on the neutral wire.)

The NEC allows multiple circuits to share a common neutral wire. The result can be current flowing on the neutral wire at a multiple of twice the phase current. This current can quickly overload the ampacity (current capacity) of the neutral wire, causing the wire to overheat and resulting in a very dangerous situation.

According to NEC 210-4, a "shared" or common neutral is allowed to exist in multiwire circuits. IEEE Std. 1100, 6.4.1.1 takes the code a step further by specifying the need for dedicated circuits for computer equipment and neutral conducting impedance and sizing requirements. In this case, the IEEE standards complement the NEC requirements, and in effect make the NEC requirements more restrictive.

The Use Of The Conduit As Ground

According to NEC 250-91(b), the conduit or piping that electrical wires are run in is allowable as "ground." Since this conduit is used all over a facility, its integrity as a grounding source is questionable. IEEE Std 1100 6.4.1.1.7 recommends that "electronic loads . . . be grounded with a separate equipment grounding conductor" and that this equipment grounding conductor be "insulated from the conduit ground." The IEEE further recommends maximum resistance measurements for all conductors, including the grounding conductor. This, again, is a case where the IEEE standards are more restrictive than the NEC requirements.

"Isolated Ground" Wiring Practices

The last two areas of contention between the NEC code and the IEEE are the proper installation of isolated ground circuits and the use of metal conduit or a raceway when housing critical electronic circuits.

Isolated ground circuits were supposed to be a panacea to the grounding issues faced by today's computer equipment. In reality, the installation of these circuits is seldom done correctly. In fact, on-site experience points to the fact that every site examined under American Power Conversion's PowerAudit program over the past two years has had isolated ground circuits installed incorrectly *(Figs. 2 and 3)*.

The procedures for when an isolated ground is required and how to install the actual circuit are very limited in the NEC code. NEC 250 mentions the grounding requirements for electronic circuits, but the procedure is not mandatory and is found in a Fine Print Note (FPN). NEC 517 discusses grounding requirements for hospital locations and does not specify isolated ground requirements for other types of installations. In the IEEE Emerald Book Section 9.10.12.6, specific procedures for installation and maintenance of isolated ground circuits are defined. Very specific details are contained in this section, right down to termination points and conductor size. As is the case in the previous examples of discontinuity between the IEEE standard and the NEC code, the IEEE takes the NEC re-

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quirements and "raises the bar."

Networking equipment is caught firmly in the middle of these two standards. Ultimately, it is the computer user and more generally, the business itself, that is suffering the discontinuity between the IEEE and NEC guidelines. The only true way to ensure that your specific site has an acceptable electrical distribution infrastructure is to have the site thoroughly examined by engineers trained in both the NEC and IEEE standards.

Many different "power quality surveys" are available in the market today. Utility companies, smaller engineering firms, and some independent contractors offer some type of analysis. However, when it comes to "bridging the gap" between IEEE and NEC specifications, there are few programs available on the market today.

The Power Audit

A power quality survey should be a very custom-centered and focused consulting process. From the initial meeting to the final deliverable product or service, the methodology should be focused on providing the customer (business) with the benefit of maximum reliability of their information processing investment. For example, a typical power audit can range from one day of on-site work to many days for very large enterprises. The technical analysis and interpretation do not, however, change from site to site. The basic NEC requirements and IEEE standards are used as the foundation for the analysis.

Before the engineer can perform any of the on-site work, customer interaction beforehand is required. An engineer will work with a facilities person from the customer's site to build an electrical "picture" of what the site will require in terms of analysis. Based upon this information, the analysis can be focused and streamlined to ensure maximum efficiency of the engineer.

The on-site work required usually starts at the computer equipment under question and works backwards through the electrical distribution infrastructure. Branch circuits are examined for total harmonic distortion (THD), conductor resistance, rms voltage, and grounding methodology. Handheld instruments are ideal for this type of measurement. Working through the electrical infrastructure, circuit-breaker panels feeding power to the previously examined branch circuits are analyzed.

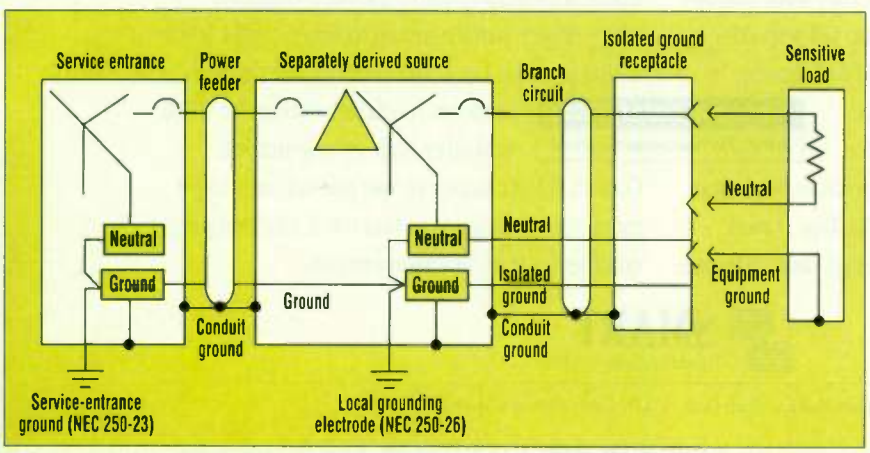
Handheld equipment such as the Fluke model 41 harmonics analyzer and the Fluke model 87 true-rms voltmeter are perfect instruments for recording true-rms voltage and current readings at the circuit-breaker panel. Grounding methodology in the panel is of critical importance here. The type of grounding and bonding at the panel is examined and a predictive analysis can be made as to the performance of computer equipment.

Tracing the electrical distribution system back to its origin, readings are made at the transformers feeding the circuit-breaker panels. Basic measurements are made here—voltage, current, and grounding methodology. Finally, the service entrance switch gear is analyzed. Due to the higher voltage involved, alternate equipment may have to be used. Continuous line monitors made by Dranetz and BMI often are applicable at the service entrance to provide a longer-term power monitoring option.

Deliverable Construction

After all the on-site work is accomplished, the task of translating the basic measurements and inspection into an easily understood and comprehensive document begins. The deliverable report is a culmination of the entire site visit and the conformance to (or nonconformance) to NEC and IEEE standards. During the initial customer interaction, the "level" at which the report is to be written is determined. Often these reports are read by the chief information officer (CIO) or the director of MIS, but the action required is on the part of the facilities engineers or outside contractors. It is critical that the audience for the report be known before the actual writing begins.

Depending on the size of the site, the report may be varied in length, complete with digital pictures and waveshape pictures. The traditional report contains an executive summary, allowing the overall analysis to be distilled into several paragraphs. The body of the report contains the recommendations for change, if required, complete with an action item list with NEC and IEEE references. This action item list can be given to the facilities engineers or contracted electrician to perform any upgrade work required. Finally, the report contains several appendices, each relating to a different part of the electrical distribution system. The report itself is then delivered to the customer within 14 working days of the on-site visit.



3. A proper isolated-grounding wiring methodology with a separately derived source.

Tony DeSpirito is Director of Professional Services at American Power Conversion. He holds a B.S. in Applied Mathematics/Computer Science from Worcester Polytechnic Institute, Worcester, Mass., and an MBA from the University of Rhode Island, Cranston. With over 10 years of military service, his technical experience includes principles of radar operation and electronic countermeasures.

How Valuable	Circle
Highly	534
Moderately	535
Slightly	536

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LX8582A	8.5	1.3
LX8383/A/B	7.5	1.5/1.3/1.3
LX8580	7	0.55
LX8584/A/B	7	1.4/1.2/1.4
LX8581	6	0.5
LX8586/A	6	1.3/1.1
LX8554	5	1.0
LX8384/A/B	5	1.5/1.3/1.3
LX8585/A	4.6	1.4/1.2
LX8587/A	3	1.3/1.2
LX8385/B	3	1.5/1.3
LX8386/A/B	1.5	1.5/1.2/1.3
LX8117	0.8	1.2

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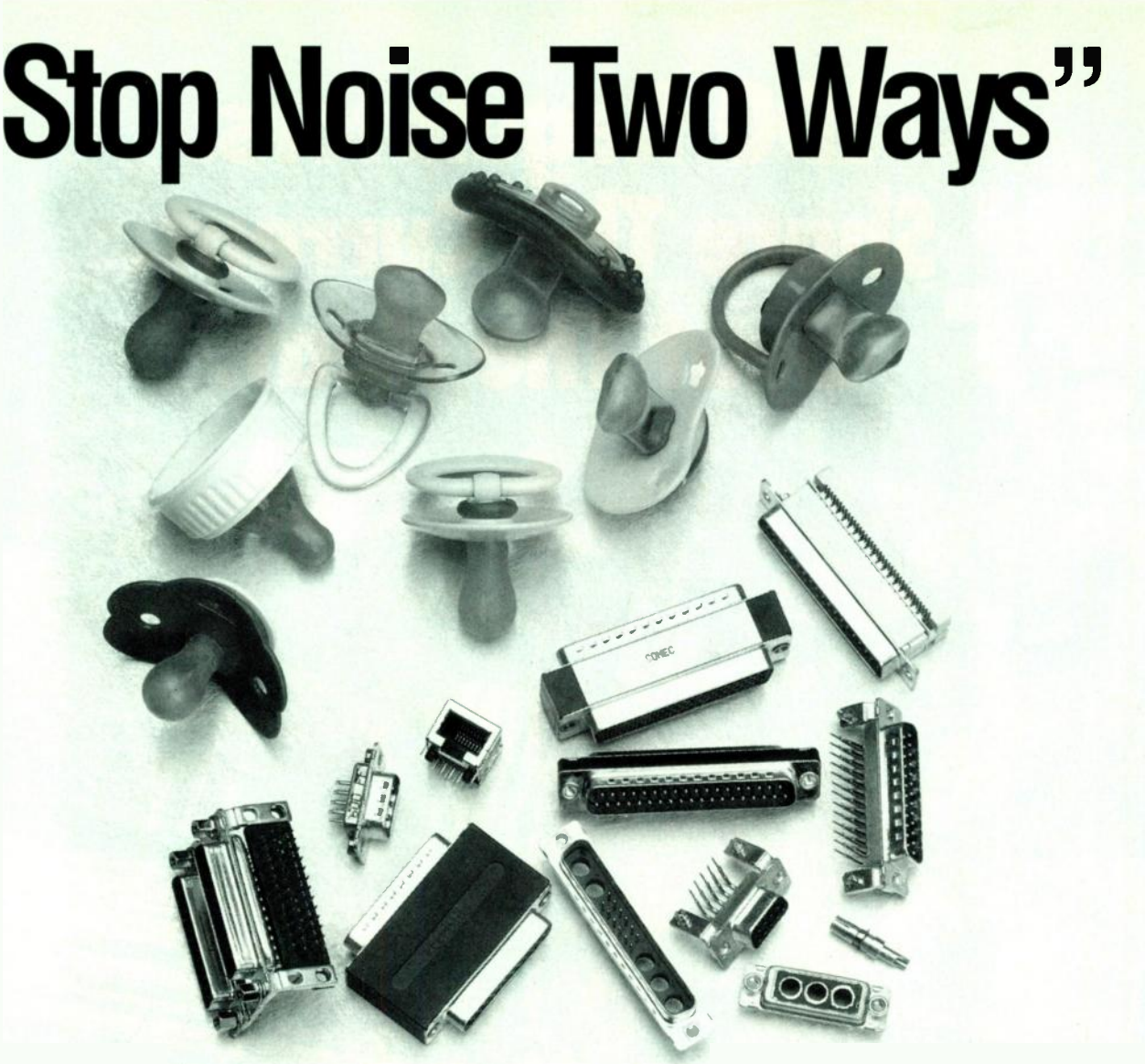
"Stop Noise Two Ways"



Most people know that a pacifier will stop noise, sometimes very quickly, other times it takes a little longer. The method, however, works. Add a little sweetness and it works even faster. And for certain applications the pacifiers come in different shapes and sizes.

Conec Filter Connectors stop noise as well. Noise created by EMI/RFI in today's high speed digital systems. And just like pacifiers, Conec Filter Connectors come in different configurations - industry standard d-sub, high density d-sub, filltered adapters, modular jacks and combo d-sub, with power filtering and signal filtering. We don't add any sweeteners. What we do add is our patented planar filters. The technology with a proven track record, combined with the industry's best connectors—ours. Both technologies fully integrated, for best results in filtering.

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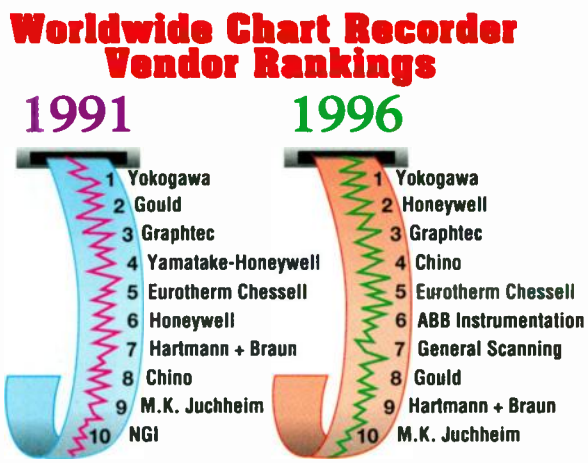
ELECTRONIC DESIGN QUICK LOOK

Edited by Mike Sciannamea and Debra Schiff

MARKET FACTS

A Recorded Decline

As the progression toward a paperless society continues to affect the entire data recording market, a definite trend has emerged. During the last seven years, according to a new report from Venture Development Corporation, "The World Chart Recorder Industry," the world's chart recorder market has seen a $135 million decline. The majority of the sinking demand is seen in the paper chart recorder sector. In 1991, strip chart recorders were enjoying shipments of $535.1 million. But five years later, in 1996, strip chart recorders were counting only $404.8 million in total shipments. This downslide is thus reflected in the predicted -5.6% compounded annual growth rate (CAGR) derived from the span between 1995 and 2000. Further slowing in the circular chart recorder market led Venture Development Corp. to predict a -1.3% CAGR during the same time period. In 1991, the circular chart recorder shipments hovered around $73.3 million, while in 1996, shipments were stagnant, only collecting $84.1 million. The oscillographic sector is expected to maintain a CAGR of 2.8% through 2000. The 1996 worldwide chart recorder market ticks in at $111.7 million in shipments. On the up side, videographic chart recorders are basking in the glow of a 37.8% projected increase in shipments in the second half of this decade. Worldwide shipments increased from $3.2 million in 1991 to $37.3 million in 1996. According to the report, applications for the chart recorders in the next five years reside mainly in the process sector. Due to the increase in concern regarding regulatory compliance, the need to monitor process control and flow, as well as quality control, will continue to feed the recorder market. The application sector is still shy of inviting videographic recorders into its midst, but Venture Development sees the market growing over the next five years. The targets for the videographic recording industry will be electric, gas, waste, and water utilities. In addition, the fastest growing application will be environmental monitoring. OEMs in the natural gas and petrochemical fields also are expected to add videographic technology to their tool chests. The medical field, especially applications that have medical professionals monitoring heart rate or brain activity, is a prime source of revenue for the oscillographic chart recorder market. In studying the chart recorder vendor market since 1991, Venture Development found that the top 10 leaders in the field have changed over the course of the years. Honeywell Corporation, in its bid to sit on the worldwide chart recorder throne, has risen from the sixth spot, in 1991, to second place in 1996. The number one position in the worldwide chart recorder vendor ranking has not changed, with Yokogawa hanging on tightly to the crown. The fourth edition of the industry report attributes Honeywell's success to its acquisition and aggressive marketing strategies, and strong distribution network. By acquiring Leeds & Northrup, Honeywell improved its position in the environmental chamber and furnace industries. Joining Honeywell on its rise to the top is Chino Corporation. In widening its distribution channels to include areas outside of Japan, Chino has risen in the rankings from eighth place to fourth. The report notes that one of the biggest surprises came from Gould. The company slipped from the number two position to eighth in five years. The slide is the result of the market evolving from paper to paperless technologies. Gould produces paper oscillographic recorders. General Scanning is known for its supply of oscillographic chart recorders to the medical industry. General Scanning and ABB Instrumentation are two newcomers to the top ten list. Of interest to market watchers, some of the companies in the list had been acquired by larger concerns, for example, NGI by LEM Holdings. "The World Chart Recorder Industry" also provides end-user analysis, distribution-channel analysis, product forecasts, and strategic trends. For more information, contact Venture Development Corporation, One Apple Hill, Natick, MA 01760; (508) 653-9000; fax (508) 653-9836; e-mail: vdc4u@aol.com.—*DS*



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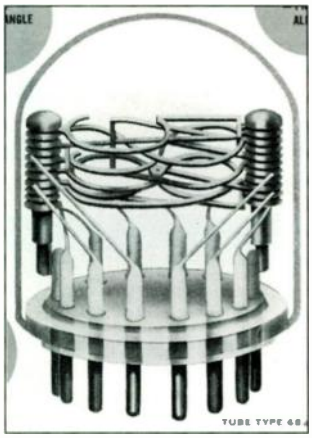

The first mass-produced, all-electronic read-out tube ... NIXIE, IS NOW IN VOLUME PRODUCTION at the Burroughs Corp. Electronic Tube Div. ....

NIXIE is a gas-filled, cold cathode tube which contains all the numerical digits 0 to 9. Any individual number can be simply selected and displayed in a common viewing area, the ideal method for converting electro-mechanical or electronic signals directly to readable characters.

NIXIE Design Advantages include: unlimited rate of change; lowest cost in-line indicator; lowest power in-line indicator; operation unaffected by temperature changes; multiple remote indications from one driving circuit; production uniformity from tube to tube and number to number; and human engineered for performance, appearance, and reliability.

Electronic Tube Division, Burroughs Corp., Plainfield, N.J. *(Electronic Design, April 15, 1997, p. 52)*

The Nixie tube was the first easy-to-use numerical display module. Shown is a closeup of the tube, with its ten elements shaped as numerical characters. Only the selected character will glow (bright red-orange) with its surrounding gas discharge. Nixie tubes were widely used in the new digital instrumentation coming onto the market—electronic frequency counters, voltmeters, etc.—SS.

Basement Death Rays Needed

Freelance inventors who have lately been dulled and depressed by the usual challenges to their imagination might find inspiration in the following list of nine problems proposed by the National Inventors Council, U.S. Department of Commerce. The Council calls these "blue sky" problems; that is, they demand a sky-is-the-limit type of thinking. If you have an idle basement laboratory, you might well put it to the use of the armed services and solve the following:

Death Ray or Wave. Equipment of usable size, capable of producing death rays effective at 500 yards—without excessive power input. Investigations so far indicate that a completely new approach is needed.

Snow Track Eraser. A practical means of destroying the tell-tale tracks of men or vehicles across snow fields. Object is to restore original contour of snow field to avoid air detection.

Non-magnetic Compass. A device small enough to be carried by a man on foot, which can determine true north, independently of the earth's magnetic field. Better still, it should enable a man to determine his position accurately.

Explosive Mine Detector. A method for locating explosives buried at shallow depths below the earth's surface. Present detectors locate the explosive's container, or signal the presence of a hole in the ground.

Method for Converting Light into Electrical Energy. An invention that will convert a small amount of light into enough electricity to operate electrical equipment. Far greater power output is needed than has been supplied by solar batteries.

Mail your solutions to the National Inventors Council, the official clearing house for inventions of potential value to the Government. A complete list of hundreds of technical problems affecting national defense can be obtained by writing NIC, U.S. Dept. of Commerce, Washington, D.C. *(Electronic Design, April 1, 1957, p. 10)*

Not much comment necessary—most of the items are still just someone's pipedream—except for one that's deadly serious: The problem of buried land mines, which has escalated to horrendous proportions. Many scientific groups have joined forces to find a solution to the problem of locating and destroying abandoned land mines. See our report in the Dec. 2, 1996 issue.—SS

A Pair Of Scissors And A Dream

Engineers looking for a convenient and cost-effective way to experiment with electroluminescent lamps can turn their eyes to BKL for the solution. The company's Proto-Kut lamp panels are designed to be cut and shaped to fit, using scissors, razor blades, or hobby knives.

With the condition that at least one pair of terminations remains connected to the portion of the lamp intended for use, the lamps can be cut to fit any shape.

BKL does issue a caveat: The Proto-Kut lamps do not substitute for custom-engineered lamps, and do not hold up under the same environmental conditions. Despite the drawbacks, though, the panels allow design engineers to try out electroluminescent backlighting techniques such as cool operation, consistently even lighting, high brightness, long life, low power consumption, and no glare.

BKL's Proto-Kut kit also includes one low-voltage lamp and one high-voltage lamp. The low-voltage lamp is powered by an IC inverter with two AAA cells, while the high-voltage lamp is powered by either of two magnetic resonating transformer-type inverters. Optimized to power different size lit areas, the transformer-type inverters are of the 9-V dc variety.

The kits are priced at $100 each. The fee includes shipping and handling charges.

For more information on the Proto-Kut kit, contact BKL Inc., 421 Feheley Dr., King of Prussia, PA 19406-2658; (610) 277-2910; fax (610) 277-2956.

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Y2K UPDATE

As we edge closer to the turning of the millennium, the more options become available for Year 2000 Date Change (Y2K) compliance. All of the helpful advice garnered from Y2K professionals points to being choosy about your service vendor—especially if your business hangs in the balance while in the doorway of the 21st. century. Managers must decide if they want to take on the challenge themselves (and many may argue that if they're at that decision now, they're running very late in the game), or drop Y2K compliance either partially or wholly into the hands of a consultant. Either way, the informed decision is, of course, the better decision.

One information management company, Unisys Corp., is now acting as a reseller for Micro Focus' Revolve/2000 product as a component of its TEAM2000 solutions suite. Although Revolve/2000 will be applied in analyzing and assessing Unisys' 2200 series COBOL code, the tool also can be used across multiple languages within a variety of application environments.

One of the issues facing companies in the process of becoming Y2K-compliant is the inability to examine and assess the potential damage throughout their entire program structure, covering millions of lines of code. The TEAM2000 addresses this problem with the Revolve/2000 tool. Businesses in transition can extend their current applications to handle the date change. Developers can deploy production systems in client/server applications, as well as move application development and maintenance off the mainframe.

Details concerning Revolve/2000 can be obtained from Micro Focus' web site: **http://www.microfocus.com.** Unisys Corp. can be reached at Township Line and Union Meeting Roads, Bluebell, PA 19424; (215) 986-2243; fax (215) 986-2037; e-mail: chucktuori@unn.unisys.com.

For those companies that have already begun to bring their systems into compliance, MDY Inc. offers their Year 2000 Project Review service. Enterprises that are looking for third-party confirmation that their progression is on target can use MDY's "Year 2000 Project Review Document." The document is targeted toward firms who would rather conduct their own periodic reviews. The review document is available separately, and allows businesses to monitor their progress within their own time frame.

The company focuses on 10 critical compliance areas including communications, methodology, scope, testing, and tools. MDY can conduct audits ranging from two to five days, but it does not provide software tools or perform long-term conversions. The fact that MDY is offering the audit end of the compliance issue is important to remember, as the buzzword in Y2K conversation is usually "tool."

On the very important "awareness" side of the Y2K process, MDY also offers Executive Year 2000 Education consulting services.

For more information, contact MDY Inc., P.O. Box 862074, Marietta, GA 30062; (770) 642-8467; e-mail: mdyinc@aol.com.—*DS*

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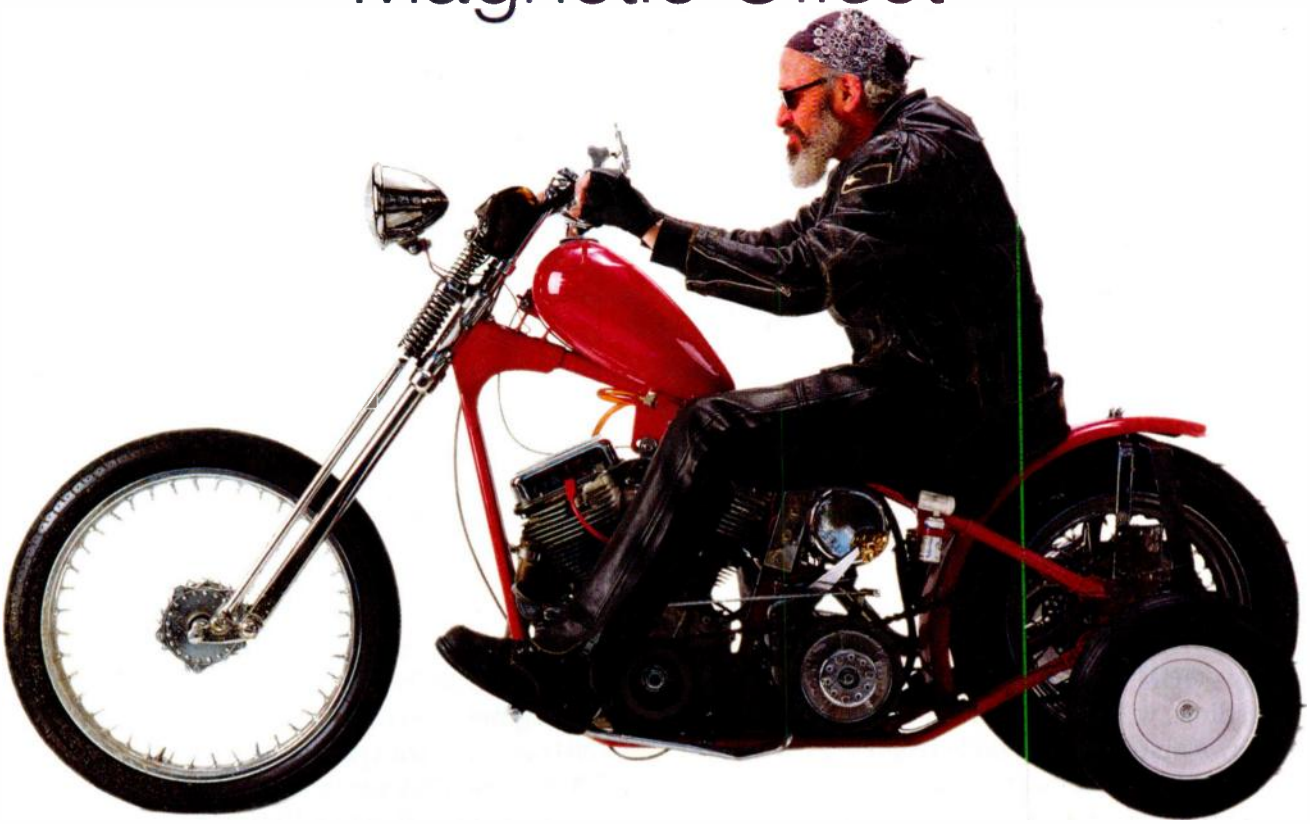
The Answer For Reducing Magnetic Offset



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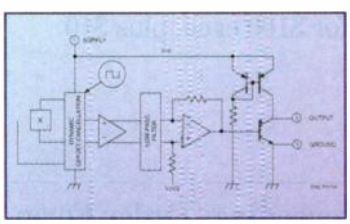

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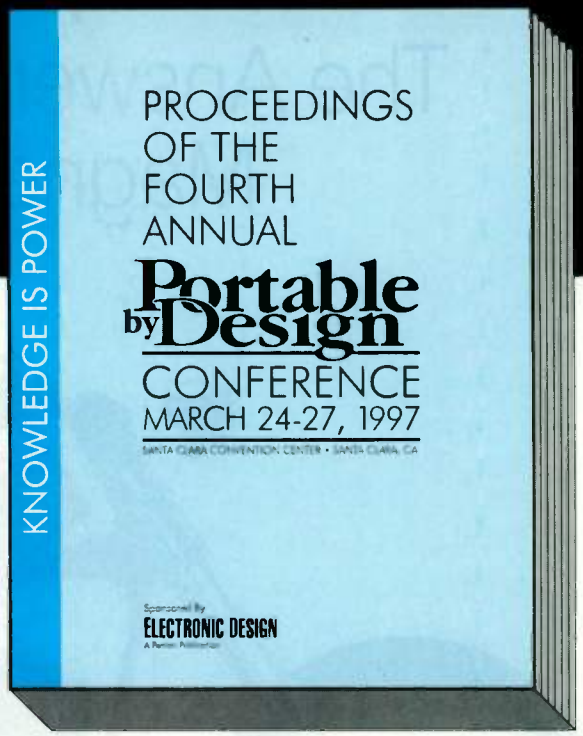

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KMET'S KORNER

RON KMETOVICZ
CONTRIBUTING EDITOR

My December 2 column stated: "Put the engineering team on a reduced schedule for reduced pay program." I offered the recommendation as an alternative to laying off new product development engineers when business falls.

Reader response included:

"Your second point, the reduced schedule, is to me a very dangerous and highly undesirable technique. The company has presumably already eliminated the ineffective engineers. The reduced plan will then work on the best ones."

"If you give engineers a 5% or 10% pay cut (which is what the "reduced schedule" really is), and they are good at what they do, they'll be out the door so fast they'll leave skid marks—and suddenly unsupported projects."

"Everyone gets angry. The volume of work falls to less than the level of the cut. Innovation ceases. The talented engineers leave the company. The product introduction is not only late, but of a much lower quality. The competition now has the advantage of inside knowledge that departed with the good engineers."

These views offer little hope over being de-cruited, downsized, laid off, or fired. They suggest harsh corporate cutting actions in response to market downturns rather than offering the best available option to return a business to prosperity. The quotations imply that the "best" engineers on new product teams want members of their peer group to suffer from the corporate hammer and boot; and if it does not happen, the "talented" prefer to turn tail and run. Sadly, some engineers, engineering managers, and executive managers tend to believe it!

Bear in mind, a company must be undergoing significant hardship to even consider a reduction program. And it will not be implemented if a vision for full recovery does not exit. Furthermore, this vision must contain believable measures that return the business to prosperity, including the elimination of the reduction initiative, in a relatively short period of time. So what really happens?

Having personally experienced this type of program I know they offer many positive options to the individual and the company. Upon hearing about the situation for the first time, a fear of the future materializes. I thought about making ends meet with a smaller paycheck. A wife, two children, big mortgage on a Silicon Valley house, and general living expenses came to mind—I knew a financial adjustment was in order. But compared to the option of being unemployed and pounding the streets for a new job, the pay reduction looked manageable. I moved on to thinking about dusting off the resume while looking at my company's vision for recovery. If I believed in and supported the vision, I could bet on the future without a job change; if not, I had time to look around.

As I became more content with the modified environment, the inevitable happened—people began to talk. Engineer to engineer, engineer to engineering manager, engineer to executive manager interactions built the foundation for working business recovery issues. Team involvement to produce a workable solution to the business problem consumed the organization. As a participant in the process, I had the option to contribute or desert, as did everyone else. In a few weeks, we reached a point of equilibrium. Never did I send out a resume, nor did I witness the departure of a key contributor. In every case, the reduction option led to an improved presence in the market place for the company with increased professional and financial reward for myself. Is this approach to business in the sole possession of Hewlett-Packard?

I encourage businesses to give this program full consideration. The idea that engineers head for the door when such a program is implemented is wrong. Most appreciate the commitment the company makes to the turnaround and the key role they perform. Once successful, the ties that bind become significant.

To obtain an e-mail copy of "The Complete List of Reasons for Late Product Information," contact Mr. Kmetovicz at kmetovicz@aol.com.

OFF THE SHELF

"Satellite Communications System Design" contains reviews of various signal types, causes of signal impairment, source signal processing, various telecommunication services, and quality of service for different types of signals. The book also includes an outline of satellite communications systems, an assessment of the link budget problem, discussions of satellite and earth station characteristics, and various aspects of technical systems design, including operational orbits, RF design issues, and system economics. The 837-page book is priced at $110. Contact the Penton Institute, 1100 Superior Ave., Cleveland, OH 44114; (800) 223-9150; fax (216) 696-6023; Internet: http://www.penton.com.

"SMPS Simulation With Spice3" is a reference guide for power supply and power circuit designers. It contains information on how to simulate, model, and design switched-mode power supplies using the SPICE3 circuit simulator. Topics discussed include overcoming emergence problems; converting ac waveforms into dc voltage levels; and using optimizer routines to assure the best possible designs. Priced at $55, the book includes a disk with SPICE3 models, schematics, and SPICE netists. Contact Intusoft, P.O. Box 710, San Pedro, CA 90733-0710; (310) 833-0710; fax (310) 833-9658; Internet: http://www.intusoft.com.

Sending Letters To QuickLook

We're pretty accessible people here at *Electronic Design*. We like our readers to know where to find us (while we're at work, of course). So, if there's some urgent fact that you feel we should know, you can e-mail either Mike Sciannamea at **mikemea@class.org** or Deb Schiff at **debras@csnet.net.** That goes for fan mail, too, but if you plan to extol the virtues of QuickLook, do us a favor and print that out on company letterhead—looks nicer when laminated. Hard copies should be addressed to: QuickLook, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604. Our fax number is (201) 393-0204.

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To access Vishay on the Internet: http://www.vishay.com

For Literature, Call Vishay's FlashFax™ Service at 1-800-487-9437.
(For specific document numbers, refer to the articles below.)

COMMITTED TO PASSIVES

Sprague® Provides Low ESR Capacitors for Pentium™ Applications

Solid Tantalum Chip Capacitors Solve Filtering Problems

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The newest Pentium microprocessors are pushing power supply designers to use low equivalent series resistance (ESR) capacitors to control ripple current and ripple voltages. Other factors including power dissipation capabilities, lower voltages, miniaturization, surface mount assembly and operating frequencies also affect the designer's selection of filter capacitors.

For frequency filtering below 500kHz, Sprague's 594D tantalum chip capacitor offers the best combination of low ESR, good power dissipation, and small SMD construction compared to other technologies.

Like all solid tantalum chip capacitors, the 594D is extremely stable under temperature changes and time. In addition, they have no end-of-life constraints or known wearout mechanisms for excellent reliability and stability.

The 594D features values ranging from 4.7µF to 470µF and

voltages from 4V to 50V. For space critical applications, the conformally coated 594D offers up to 35% better volumetric efficiency than a molded chip at the same rating.

For a data sheet, call Vishay's FlashFax℠ Service at 800-487-9437. Document #518.

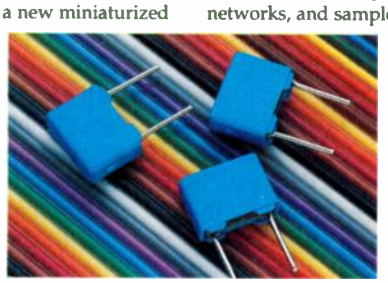
Pentium™ is a trademark of the Intel Corporation.

Roederstein Introduces a New Miniature Film Capacitor

The Highest C-values Available with 5mm Lead Spacing

VISHAY Roederstein

Roederstein Electronics, Inc. has expanded its MKP 1840 series of metallized polypropylene film capacitors to include a new miniaturized version with the highest C-values available with 5mm lead spacing. Fully auto-insertable, these capacitors allow the design engineer to take advantage of a much reduced printed circuit board footprint while maintaining the superior characteristics of the polypropylene dielectric.



Polypropylene's excellent stability, very low dielectric absorption, high insulation resistance and low dissipation factor make these capacitors ideally suited for use in designs where precision is required, such as audio and instrumentation applications. Most commonly these capacitors are used in oscillators, timing and LC/RC filter circuits, high frequency coupling/decoupling, cross-over networks, and sample and hold circuits.

Roederstein's MKP 1840 capacitors are also self-healing and do not exhibit a piezioelectric effect. The new 5mm lead-space capacitors are available in C-values up to .10µF and in a 100-volt rating. Larger sized capacitors are available in higher voltages and capacitance values up to 10µF. All are encapsulated in flame-retardant cases.

For a data sheet, call Vishay's FlashFax℠ Service at 800-487-9437. Document #707.

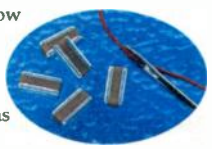
Low Inductance Capacitor from Vitramon® Improves Circuit Performance

0612 Cuts Inductance in Half

VISHAY Vitramon

Selecting capacitors with low inherent inductance is always an important design consideration—particularly in high speed microprocessor and multi-chip module circuitry. Normally in the 0.8nH to 1.0nH range, this inductance can now be cut by more than half with a new monolithic ceramic chip capacitor developed by Vitramon®.

The new Vitramon chip (VJ0612) provides standard inductance levels as low as 0.3nH in easily-packaged dimensions (.062"L x .126"W x .038"H). Standard capacitance range is from 8200pF to 0.22µF with tolerances of ± 5%, ± 10%, ± 20% and voltage ratings of 25V and 50V.



This combination—available in a robust, easily mounted package—makes the VJ0612 ideal for use in new designs where low inductance is important as well as for improving the performance of existing circuitry.

For a data sheet, call Vishay's FlashFax℠ Service at 800-487-9437. Document #410.

VISHAY DALE · VISHAY Roederstein · VISHAY SPRAGUE · VISHAY RESISTIVE SYSTEMS · VISHAY Vitramon

VISHAY ELECTRONIC COMPONENTS, NORTH AMERICA/ASIA: DALE®, ROEDERSTEIN, SPRAGUE®, VISHAY RESISTIVE SYSTEMS, VITRAMON®

QUICK NEWS

Persoft has recently expanded its antenna lines to link companies' LANs up to 10 miles apart, at 2.4 GHz. The Intersect Remote Bridge is a wireless connection system designed to provide a secure alternative to T1 lines for Ethernet or Token Ring LANs.

Using spread spectrum radio frequencies, the bridge connects remote wired Ethernet or Token Ring LANs at 2 Mbits/s. The new antennas can be installed quickly, and are resistant to interference. Persoft offers a variety of antennas, such as directional and omnidirectional for a flexible decision-making process.

Several factors are involved in choosing the appropriate antenna to connect sites—the distance between sites, possible signal-blocking obstructions, and the number of sites.

The antennas are sold separately from the Intersect Remote Bridge, and start at $400. The Ethernet version of the bridge is priced at $9500 per pair; the Token Ring version runs $11,995 per pair.

Contact Persoft Inc., 465 Science Dr., P.O. Box 44953, Madison, WI 53744-4953; (608) 273-6000; fax (608) 273-8227; Internet: http://www.persoft.com.

Catching the digital video wave, NuWave Technologies has moved its video processor, the NVP, from alpha to beta testing. The chip brings back color and light to video monitor images, without changing the original signal.

NuWave plans to produce approximately 100 printed-circuit boards for manufacturers of cable and satellite set-top boxes, computer monitors, camcorders and VCRs, and television sets. The goal of the beta testing is to incorporate the changes and recommendations into the final specifications for an application-specific integrated circuit (ASIC).

The NVP is designed to improve video images by selective mapping of the analog video wave, but the technology is not dependent on either analog or digital standards to produce an improved image.

Beta PC boards will be demonstrated at the National Association of Broadcasters trade show April 7-10, Las Vegas, Nev.

Further facts can be provided by NuWave Technologies Inc., 1 Passaic Ave., Fairfield, NJ 07004; (201) 882-8810; fax (201) 882-8812.

SEEQ Technology has released its 84301 and 8431 Hurricane Fast Ethernet switches. The 8431 is pin-compatible with SEEQ's 84C30A four-port controller, and the 84301 is pin-compatible with the company's 84C300A unit.

Both "switch-MACs" come with 15 network-management counters per port. As is the case with the entire Hurricane family, these new networking products support an open-system architecture. The 84301 controller features a 100 Mbps Fast Ethernet capability.

The open-system interface consists of a synchronous 32-bit data bus, Little Endian and Big Endian data formats, an 8-bit command/status bus, and independent 128-byte transmit/receive FIFOs for each channel.

In 1000-piece quantities, the 84301 is priced at $53 and the 8431 is priced at $37.

More details can be obtained from SEEQ Technology Inc., 47200 Bayside Pkwy., Fremont, CA 94538; (510) 226-7400; fax 9510) 657-2837; Internet: http://www.seeq.com.

Expanding its low-power, multipoint transceiver family, National Semiconductor has added four new RS-485 devices to its lineup: The DS485, DS481, DS1487, and DS36C280.

Targeted toward industrial and telecommunication applications, the RS-485-compliant devices are 5 V, 1 x 1 transceivers, built with a CMOS process. These transceivers are found mostly in physical cable interfaces that require reliable data transmission over long distances.

They are designed to provide stable transmissions over noisy environments. Typical applications for the RS-485 devices are alarms, cellular base stations, networking switches, remote I/Os, sensors, and traffic signals.

Power savings as compared to bipolar or BiCMOS devices come from the transceivers' operating Icc reaching as low as 500 A. And, each device in the line allows designers to choose the precise transceiver for the application. Features include a one-quarter unit load, programmable slew-rate control, industrial or commercial temperature ranges, Sleep Mode, and DIP/SOIC packages.

The baseline transceiver of the family, DS485, has a maximum I_{cc} of 800 µA, a one unit load input impedance to the bus, and a data rate of up to 2.5 Mbits/s over the entire industrial temperature range.

For commercial temperature ranges, the DS1487 is more applicable than the DS485. The DS1487 sees a maximum I_{cc} of 500 µA, a one-quarter unit load input impedance to the bus, and a data rate of up to 2 Mbits/s. This transceiver can be used in applications such as security alarms or remote sensing/response systems.

In addition to the features of the DS1487, the DS481 has a Sleep Mode setting, where the I_{cc} is down to 0.2 µA. This device has a one-half unit load input impedance to the bus. Remote site applications, such as mobile diagnostic equipment or cableless data collection systems, are suitable for the DS481 because of the Sleep Mode setting. These systems typically are powered by batteries that are disabled for extended periods.

Having the same features as the DS1487, but functioning in the industrial temperature range, the DS36C280 has an added Slew Rate control feature, which allows the designer to set and change the rise and fall times of the on-chip driver. This adjustment is done through an external resistor.

The DS485, DS1487, and DS481 are priced at $1.25 per unit in 1000-unit quantities. The DS36C280 runs $1.32 each for all packages.

Contact National Semiconductor, 2900 Semiconductor Dr., P.O. Box 58090, Santa Clara, CA 95052-8090; (408) 721-3825; Internet: http://www.national.com.

INTERNET NEWS

It's tough to talk software these days without hearing the word "licensing" at least once. Offering a solution to the challenge of software distribution is Élan Computer Group, with their License Express.

License Express is actually a suite of tools designed to automate the entire sales process for demonstration, evaluation, and purchase of software over the Internet. Developers can use the suite to distribute software, issue demos, and automatically generate software licenses from their World Wide Web site.

Through License Express, customers can purchase portions of applications, then upgrade or add other components later, automatically by going to the web site. Keys are automatically distributed with the software for demonstration, during the download, and new keys are issued when payment by credit card has been received.

Queries may be directed to Élan Computer Group Inc., 888 Villa St., 3rd Floor, Mountain View, CA 94041; (415) 964-2200; fax (415) 964-8588; Internet: http://www.elan.com.

Another useful tool for web site administrators is site analysis software. NetIntellect 2.1, from WebManage Technologies, allows users to obtain geographical, marketing, and statistical data about visitors to the site, as well as their host site.

NetIntellect finds postal and e-mail addresses, as well as contact names via an updated database of over 500,000 Internet organizations. The tool can produce easy-to-read, preformatted summary reports and custom reports from a Microsoft Access database.

Log file data can be accessed for new reports without having to reprocess the log file, through a "Use Existing" feature. Additionally, the scheduling capability allows users to automatically schedule multiple reports to be generated at any time, or multiple times. This facility is accomplished through the FTP within the scheduler which remotely retrieves files from the server.

NetIntellect is priced at $149 for a single-user version, but those interested can download a 15-day trial version at WebManage's site: http://www.webmanage.com.

Security on the Internet is based upon the level of encryption protecting the user's information. In the encryption world, there are two kinds of stories: New technology and licensed technology. In this case, Atalla has licensed Certicom's Elliptic Curve (EC) toolkit to develop cryptographic firmware for the Net Armor Internet Security Processor (ISP).

Elliptic Curve Cryptosystem (ECC) is a public-key technology which Certicom has implemented in its EC toolkit. ECC currently holds the highest strength-per-bit of all known public key systems. The toolkit uses ECC to provide high-speed data encryption, digital signature generation, and verification.

Atalla's Net Armor chip, jointly developed with VLSI Technologies, is a fully-integrated single-chip design targeted toward PCMCIA cards, PCI add-in cards, set-top motherboards, and computer motherboards.

Information regarding the EC toolkit can be obtained from the Certicom Corp., 200 Matheson Blvd. West, Mississauga, Ontario, Canada L5R 3L7; (905) 507-4220; fax (905) 507-4230; Internet: http://www.certicom.com.

As is the case with many cities in the world, the only way to build is up, and the web is no exception. According to the "Final Report of the International Ad Hoc Committee: Recommendations for Administration and Management of gTLDs" from the Internet Society, the newest additions to cyberworld are projected to be the seven new generic Top Level Domain (gTLD) name types for Internet locations. At press time, this document is purely a proposal, inviting public comment.

The proposed new gTLDs are:

.firm—for businesses or firms.

.store—for businesses offering goods for sale.

.web—locations with activities specific to the web.

.arts—locations featuring cultural and entertainment information.

.rec—locations that specialize in recreational or entertainment information.

.info—sites providing information services.

.nom—intended for individuals, and not for commercial concerns or organizations.

Continuing in the multiples of seven vein, 28 new registrars also may be established to grant registrations for the second-level domain names under the new gTLDs. There would be a lottery deciding who among the applicants will be selected for the new responsibility. The new registrars would be able to register the domain names under all of the new gTLDs. In addition, the three existing gTLDs, known as .com, .net, and .org, would be shared as well, under the plan. Currently, Network Solutions Inc., at the hands of the United States National Science Foundation, acts as the registrar for those three gTLDs.

For future registrar activities, a new group, the Council of Registrars (CORE), would be established under Swiss law to create and enforce registration requirements. The target date CORE's Memorandum of Understanding MoU, if signed by all the registrars, is May 15, 1997. The MoU would be the mechanism for establishing CORE. A MoU also would be the deciding factor for the future policies regarding the gTLDs. Both the private and public sectors would be invited to sign the nonregulatory policy framework, known as the gTLD MoU.

Questions or comments regarding the new recommendations should be directed to the Internet Society, 12020 Sunrise Valley Dr., Reston, VA 20191-3429; (703) 648-9888; fax (703) 648-9887; Internet: http://www.isoc.org.

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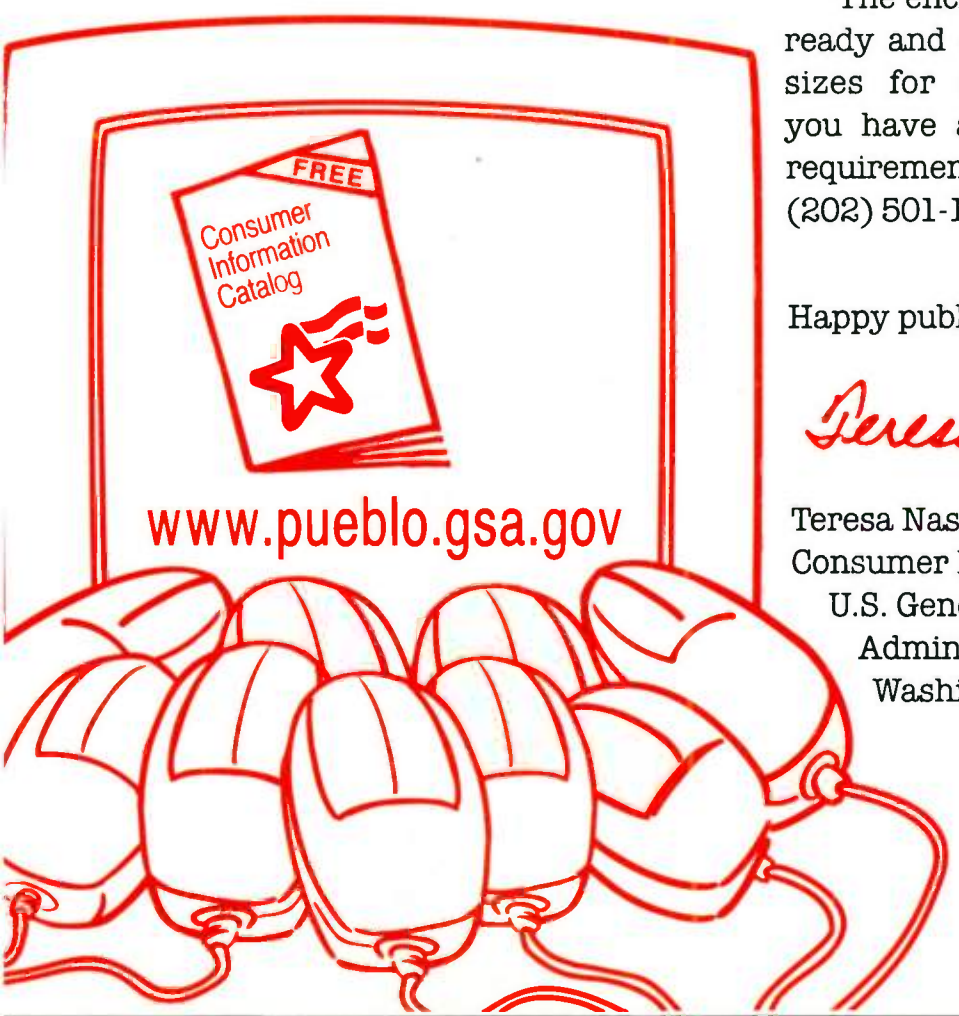


The enclosed ads are camera ready and come in a variety of sizes for easy placement. If you have any special printing requirements, please call me at (202) 501-1794.

Happy publishing!

Teresa Nasif

Teresa Nasif, Director
Consumer Information Center
U.S. General Services Administration
Washington, DC 20405

HOT PC PRODUCTS

The LM1050 Hub Controller is a Universal Serial Bus (USB) device designed to control PC monitors. The controller solution, from National Semiconductor, uses the USB technology to allow nontechnical PC users to add new external components to their systems quickly and easily.

Using a single thin cable and small connectors, peripherals such as mice, keyboards, printers, and scanners can be added to USB-based PCs.

The host controller also integrates clock generation features for system-level timing, eliminating the need for a separate microprocessor clock. Allowing monitor manufacturers to use one design on multiple models, the LM1050 features a dual-action microcontroller interface. According to National, the interface reduces design complexity and time-to-market.

Used with a microcontroller and firmware, the hub controller has five ports. The upstream port connects to a host controller in the PC. The remaining four are hardware downstream ports for additional USB peripherals. All of the ports have on-chip transceivers.

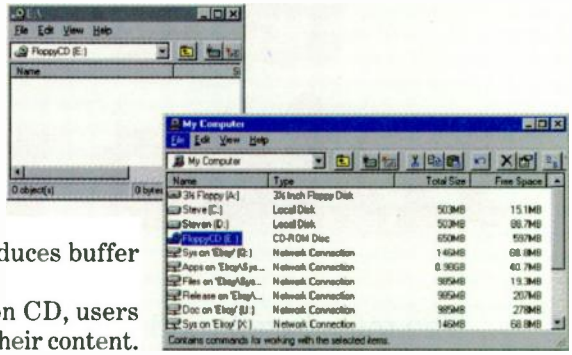
The microcontroller is connected to a hardware-selectable I2C-compatible or UART interface. When the microcontroller is configured for I2C, the interface operates at up to 400 kHz. If configured as a UART, the microcontroller can operate at up to 750 kbaud.

When the LM1050 is acting as a downstream port to control the monitor, the PC user can adjust the geometry, change the colors, and generally customize the monitor. These settings are controlled via a windowing application on the PC.

Other features on the LM1050 are an on-chip 3.3 V voltage regulator, oscillator, and clock generator. Eliminating the need for other oscillators and clock circuits, these features allow a single crystal to control all system timing functions.

For more information, contact National Semiconductor Corp., 2900 Semiconductor Dr., P.O. Box 58090, Santa Clara, CA 95052-8090; (408) 721-5000; Internet: http://www.national.com

FloppyCD is Smart Storage's variable-packet writing software, designed to bring CD-recording (CD-R) to the easy-to-use level. The tool eliminates the need to remaster, significantly reduces overhead, and reduces buffer underruns.



When recording data on CD, users usually had to premaster their content. This technique dropped another step into the process, having users stage their data on a hard disk and transfer it to the CD in a single session. Unfortunately, during the mastering process, it didn't leave much room for error.

The FloppyCD software uses the drag-and-drop model to allow users to save files directly to the FloppyCD drive via Explorer, the File Save function or File Manager in Windows, or COPY and XCOPY commands in DOS.

In traditional premastering software, writing sessions typically pick up from 10 to 15 Mbytes of overhead. If more data is written to the same CD, the same amount of overhead is created for that session. If a user wanted to record 25 sessions worth of material, using the premastering software, the CD would be wearing anywhere from 250 to 375 Mbytes of overhead. All that overhead leaves only about half of the Mbytes available on a 650-Mbyte CD.

In tests conducted by Doculabs, Chicago, Ill. (312-433-7793), the FloppyCD software created less than 1 Mbyte of overhead in writing 35 Mbytes of data, during three separate sessions.

Buffer underruns are created when streams of data, on their way to the CD, are interrupted or the data transfer rate changes. Usually, this situation occurs when the hard disk can't keep up with the transfer rate, or when multitasking slows down the hard drive.

The FloppyCD software has a cache-defining feature that allows the user to circumvent the buffer underrun. By setting the buffer size to 1 Mbyte, the cache prevents the writing from being interrupted.

For more information, contact Smart Storage Inc., 100 Burtt Rd., Andover, MA 01810; (508) 623-3300; fax (508) 623-3310; Internet: http://www.smart-storage.com.

Solid-state disks from Quantum will now be offered with ECCS's Synchronix Storage Management system. Part of the Rushmore ESP 3000 family, the ESP3013 and ESP3026 disks hold 134 Mbytes and 268 Mbytes of data, respectively.

The disks are meant for midrange to high-end computer systems, including minicomputers, servers, RAID subsystems, and workstations. The solid-state disks exceed 5000 I/O requests per second, delivering a sustained data transfer rate of over 13 Mbytes/s. The nonvolatile storage units use DRAMs as the storage media.

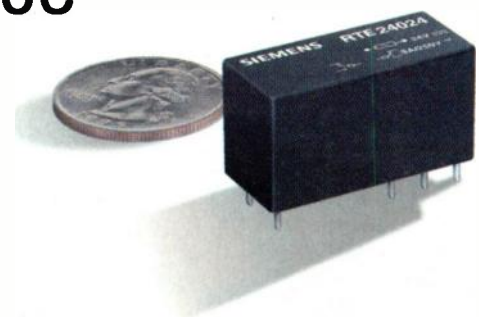
The Synchronix Storage Management system from ECCS, Tinton Falls, N.J. (908-747-6995), uses a fault-tolerant architecture in its operation within open systems environments. In the Synchronix system, hot (most frequently used) data would be stored in the Quantum solid-state disks. The other files in the system are stored in either an array of fault-tolerant hard-disk drives or tape autoloaders and libraries.

In addition to the new 3.5-inch solid-state disks, Quantum has a line of 5.25-inch disks, the ESP5000 series.

For more information, contact Quantum Corporation, 500 McCarthy Blvd., Milpitas, CA 95035; (408) 894-5090; fax (800) 4DISK-FAX; Internet: http://www.quantum.com.

SIEMENS

RT series relays are small in size, but deliver big performance



RT series relays rise only 0.62" (15.7mm) above the PC board, but they switch up to 16A at 240VAC. And they provide 8mm spacing between contacts and coil for more than 5kV isolation. That's a level of performance you might not expect from a relay this small.

The RT doesn't sacrifice life expectancy, either. Life at various loads is appropriate for appliances, HVAC systems, industrial controls, and computer peripherals.

Check out these features:

- Silver-nickel 90/10 contacts
- SPST-NO through DPDT contacts
- 8, 12, and 16 amp models
- Choice of immersion cleanable or flux-tight enclosure
- Withstands 10kV surge
- Sensitive, 400mW coil
- UL Class F insulation system
- UL recognized, CSA certified, VDE approved

How do we top all that? Easy. We produce the RT on fully automated lines for consistent quality, then use environmentally-friendly, returnable plastic shipping containers. And we provide the level of service you've come to expect from Potter & Brumfield Products Division, an ISO9001/QS9000 company that's been delivering dependable, innovative switching solutions for more than 60 years.

Find out more. From the U.S. or Canada, use a touch-tone phone and our automated fax-response system. Simply dial 812.386.2561 and request document #7800. Or, follow the prompts to speak with your sales representative.

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Potter & Brumfield Products Division
200 South Richland Creek Drive
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Fax 812.386.2072
e-mail: info@ae.sec.siemens.com

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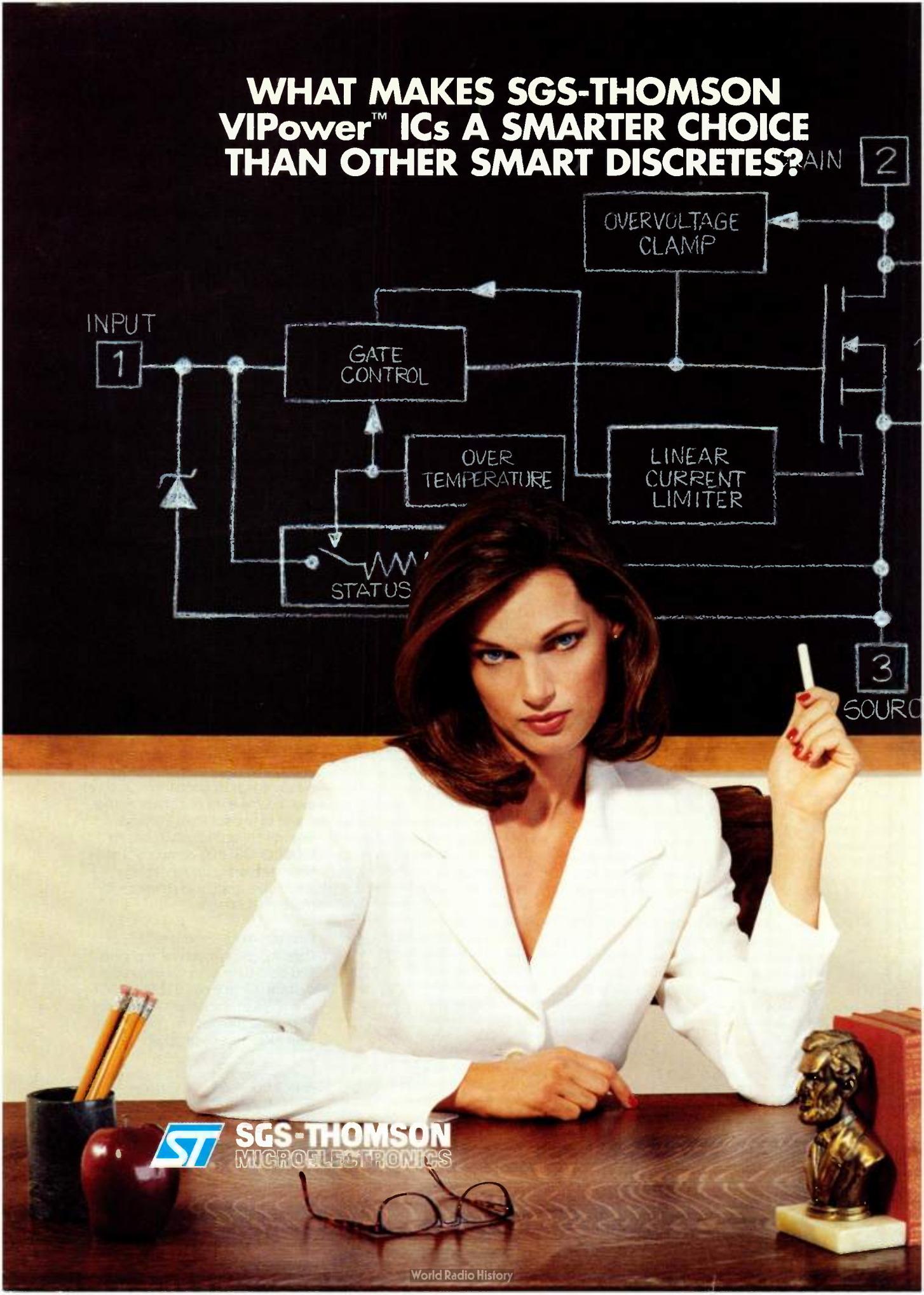
WHAT MAKES SGS-THOMSON VIPower™ ICs A SMARTER CHOICE THAN OTHER SMART DISCRETES?



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SGS-THOMSON took VIPower™, the industry's most flexible, most functional truly vertical-flow smart power technology, expanded the range and made it better.

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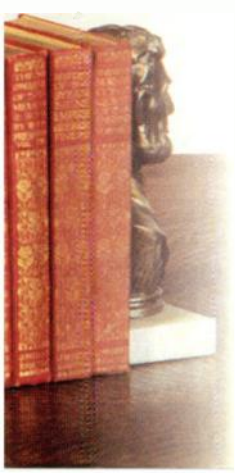

Service and Technology

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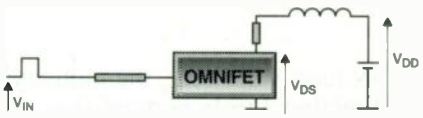
OMNIFET-VIPower. The Smarter Power.



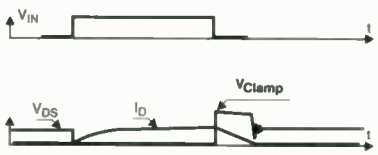
OVERVOLTAGE CLAMP

FEATURES

>Unrivaled energy handling
>Clamp internally set from 42V to 70V

BENEFITS

>No damage due to overvoltage spikes



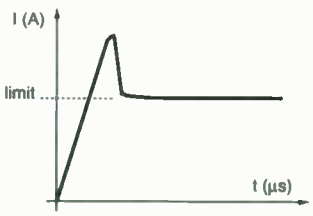
LINEAR CURRENT LIMITER

FEATURES

>Linear current limitation
>Fast step response

BENEFITS

>Load protection
>Adjustable current limit by changing the metal mask



GATE CONTROL

FEATURES

>Analog driving due to direct access to the gate of the Power MOSFET
>Logic-Level operation from a TTL/CMOS driver circuit

BENEFITS

>Pin to pin compatibility with standard MOSFET

OVER TEMPERATURE

FEATURES

>Short circuit protection
>Overtemperature protection
>Automatically restarts at 135°C

BENEFITS

>High safety in all environmental conditions

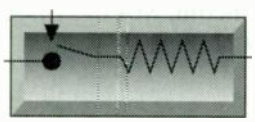
STATUS

FEATURES

>Overtemperature feed back through input pin

BENEFITS

>Real time monitoring



OMNIFETs - AUTOPROTECTED POWER MOSFETs

Type	V_{Clamp} (V)	$R_{DS(on)}$ (mΩ)	Package
VNW100N04	42	12	TO-247
VNW50N04	42	12	TO-247
VNP49N04	42	20	TO-220
VNP49N04FI	42	20	ISOWATT220
VNV49N04	42	20	PowerSO-10
VNB49N04	42	20	D2PAK
VNP35N07	70	28	TO-220
VNP35N07FI	70	28	ISOWATT220
VNV35N07	70	28	PowerSO-10
VNB35N07	70	28	D2PAK
VNP28N04	42	35	TO-220
VNP28N04FI	42	35	ISOWATT220
VNV28N04	42	35	PowerSO-10
VNB28N04	42	35	D2PAK
VNP20N07	70	50	TO-220
VNP20N07FI	70	50	ISOWATT220
VNV20N07	70	50	PowerSO-10
VNB20N07	70	50	D2PAK
VNP14N04	42	70	TO-220
VNP14N04FI	42	70	ISOWATT220
VNV14N04	42	70	PowerSO-10
VNB14N04	42	70	D2PAK
VNK14N04FM	42	70	SOT-82FM
VNP10N07	70	100	TO-220
VNP10N07FI	70	100	ISOWATT220
VNV10N07	70	100	PowerSO-10
VNB10N07	70	100	D2PAK
VNK10N07FM	70	100	SOT-82FM
VNP10N06	60	300*	TO-220
VNP10N06FI	60	300*	ISOWATT220
VNK10N06FM	60	300*	SOT-82FM
VND10N06	60	300*	DPAK
VND10N06-1	60	300*	IPAK
VNP7N04	42	140	TO-220
VNP7N04FI	42	140	ISOWATT220
VND7N04	42	140	DPAK
VND7N04-1	42	140	IPAK
VNK7N04FM	42	140	SOT-82FM
VNP5N07	70	200	TO-220
VNP5N07FI	70	200	ISOWATT220
VND5N07	70	200	DPAK
VND5N07-1	70	200	IPAK
VNK5N07FM	70	200	SOT-82FM

*V_{IN}=7V

For more information fax 617-259-9442
Complete product information at http://www.st.com

SGS-THOMSON MICROELECTRONICS

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QUICKSPEAK

Olfactory Synthesis Adds Realism

If Dr. A. H. L'fuhl has his way, in the near future telling your friend that his or her computer "really stinks" will be a great compliment. Sarcastically dubbed "smellevision" by industry naysayers, the micromachined "odor organ" that lies at the heart of olfactory synthesis technology (OST) could revolutionize a variety of computer applications from gaming and videoconferencing systems to virtual reality devices that bring the smells of a battlefield, pine forest, or expensive restaurant, to life.

Developed by NoseCom Systems Ltd., Palo Alto, Calif., the OST system combines a sophisticated artificial nose and an odor organ to support two-way olfactory communications. While this device has been predicted for some time, previous technologies have been expensive, cumbersome, and limited in scope. The breakthrough came when L'fuhl and his colleagues were working on a battlefield simulator as part of a DARPA research grant at the Stanford Research Institute, Stanford, Calif.

The team discovered the key to OST while attempting to reduce the number and complexity of different odorants that were required to give a realistic olfactory experience in a given situation. Under laboratory conditions, they identified a group of primary odorants (POs) that, when combined in the proper proportions, could be used to simulate virtually any other scent.

NoseCom's prototype odor organ (the stinkjet) contains a few dozen small vials of microencapsulated odorants, each with its own micromachined heater/valve assembly. Upon application of an electrical charge, the contents of the vial are heated, causing them to vaporize and burst from their encapsulants. By carefully modulating the power to each capsule's heater and venting valve, the odorants can be released in precise proportion and mixed via a turbulence generator mounted in the organ's forced-air collection/dispersal plenum.

If an OST-PO dispersal system can be manufactured for under $100 in OEM quantities, it should find its way into everything from video games to VCRs. Several game manufacturers have expressed enthusiasm for adding the dimension of smell to their high-end products. Plans are now in progress for adding a group of copyrighted "Smells of Victory" to new versions of popular action/combat games by Christmas 1997.

One-way olfactory broadcast is only one aspect of the OST system. Also in development is an artificial nose, known as an olfactory analyzer (OA). It can analyze an air stream and produce a digital output that represents its major PO components in a 2-to-4 kbit/s serial data stream. The nose employs an array of micromachined sensors, each of which detects the concentrations of molecules with a specific weight. Problems still exist with aliasing phenomena, where molecules with approximately the same weight can trigger false responses, but a DSP-based anti-aliasing filter is under development.

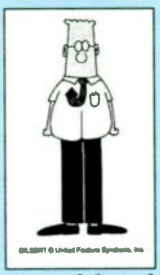
Researchers expect to demonstrate a full two-way teleconferencing system with simultaneous voice/data/video/odor (SVDVO) by 1999. In anticipation of its widespread acceptance, both TIA's T1 committee and the ITU have formed working groups to develop standards for SVDVO transmission for telephony, LAN, and Internet environments. A modified version of the V.8 modem negotiation protocol that supports one- and two-way olfactory interfaces is already under review at the ITU.

Several major modem chip manufacturers also have joined the drive for aromatic data standards and formed the SVDVO Alliance. Their goal is to develop a working de facto industry standard ahead of the slower-moving organizational committees. Meanwhile, Microsoft is rumored to be preparing WinSmell APIs, which will be folded into the next release of both Windows and Windows NT.

Contact Dr. Apri L'fuhl, NoseCom Systems Ltd., 1313 Mockingbird Lane, Suite 16, Palo Alto, CA, 90248; (408) 555-2324; fax (408) 555-2325; Internet: http://www.jokesonu.nosecom.com.

LEE GOLDBERG

Mom, Don't Throw These Cards Out!



Remember those baseball cards you used to keep in shoeboxes in your bedroom closet? Remember when you and your family moved into your new home, unpacked your belongings, and found out that Mom, in her desire to throw out "useless junk," threw out your most prized possessions?

To add to the agony, you now know how valuable that "useless junk" is, and the fact that you could fund a nice early retirement by selling that "junk" to a collector gnaws at the pit of your stomach.

Well, now's your chance to acquire a new set of prized possessions that may turn out to be valuable in the near future. Omega Engineering Inc. has announced the release of the premier Dilbert Collection Series deck card package. The package features the popular comic strip Dilbert, created by Scott Adams.

The Series #1 release, the first in a series of Dilbert and Omega product card packs, includes over 40 Dilbert comic strips printed in full color. As an added bonus, the cards will feature glimpses of Omega's newest and most popular process and measurement control products.

The Dilbert product series card packs will be available free of charge, and according to Omega, are destined to become collectors' items. Omega will publish collections of Dilbert cards quarterly throughout 1997, with a total of approximately 200 Dilbert strips for the entire year.

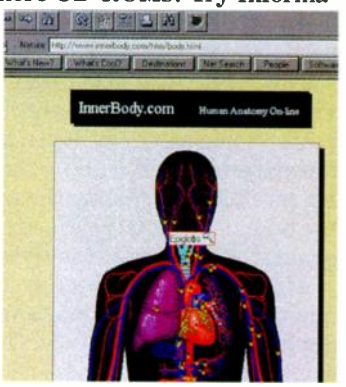
To receive the free premier Collection Series #1, and to reserve upcoming Dilbert deck card packs, call the Omega Engineering Dilbert Hotline at (203) 329-1266; fax (203) 359-7700; Internet: http://www.omega.com. (And tell Mom to keep her hands off those shoeboxes!)—MS

INTERNET ROLODEX

http://www.teleprocessing.com: Stopping off at TeleProcessing Products' site will give visitors a good look at the company's network access product line. In addition, there's a free offer for "A Guide to Integrated-WAN Access," available for visitors who fill out an on-line survey.

http://www.newport.co.uk: Newport Components has updated its site to bring two-minute data downloads to its visitors. Because the company is offering free data books on all its dc-dc converters, engineers visiting the site had been asking for quicker downloads. All of the data sheets are in Adobe PDF format. Also featured at the site is information about transformers and inductors. A new dc-dc selector program at the site allows visitors to choose the appropriate converter by keying in voltage and current requirements, as well as specifying single or dual outputs.

http://www.innerbody.com: Looking for a quick way to check aspects of human anatomy without having to download software or buy even more CD-ROMs? Try Informative Graphics' free site for an extensive guide to the human body. Included are animated body functions such as breathing lungs and beating hearts. And, teaching kids about what goes on inside Mommy during those crucial nine months of pregnancy is even easier with this free service. Tutorial sections also are in the works for this unique site.



http://www.ergpower.com: Click on this URL to arrive at power source supplier ERG's site. The World Wide Web homepage is an interactive clearinghouse for backlit information display power supplies. At the site engineers will find application information, new product information, as well as downloadable data sheets. The data sheets cover a large line of dc-ac inverters and dc-dc/ac converters for a number of different manufacturers' displays. Source information for CCFT-backlit LCDs, EL lamps and displays, vacuum-fluorescent displays, and gas-plasma displays also can be found at the site.

http://www.ashling.com: Take the opportunity to wax your electronic surfboard at Ashling Microsystems' homepage. The site focuses on delivering specific information on embedded-microprocessor development and software quality assurance tools. Clicking on the featured links will lead visitors to in-circuit emulators, source-level debuggers, software quality assurance systems, compilers and assemblers, integrated-development environments, development support for microprocessor manufacturers, and Smart Card development tools. Product data sheets also are available. In addition, links to other microcontroller information sources can be found here, as well as reference information.

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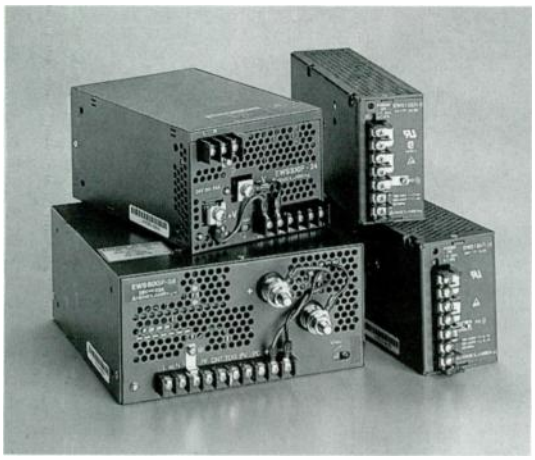
EWSP Series



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EWSP Series

OUTPUT VOLTAGE	MAX CURRENT AMPS AT AMBIENT TEMPERATURE OF 40°C	50°C	60°C	UNIT PRICE PER DELIVERED QUANTITY 1	10	25	MODEL
2V-10%~+20%	60.0	60.0	42.0	$545	$495	$452	**EWS300P-2**
2V-10%~+20%	120.0	120.0	84.0	768	692	658	**EWS600P-2**
3.3V+10%	20.0	20.0	14.0	217	196	187	**EWS100P-3.3**
3.3V+10%	30.0	30.0	21.0	294	265	252	**EWS150P-3.3**
3.3V-10%~+20%	60.0	60.0	42.0	545	495	452	**EWS300P-3.3**
3.3V-10%~+20%	120.0	120.0	84.0	768	692	658	**EWS600P-3.3**
5V±10%	20.0	20.0	14.0	217	196	187	**EWS100P-5**
5V±10%	30.0	30.0	21.0	294	265	252	**EWS150P-5**
5V±20%	60.0	60.0	42.0	545	495	452	**EWS300P-5**
5V±20%	120.0	120.0	84.0	768	692	658	**EWS600P-5**
12V±10%	8.4	8.4	5.9	217	196	187	**EWS100P-12**
12V±10%	12.5	12.5	8.8	294	265	252	**EWS150P-12**
12V±20%	27.0	27.0	18.9	545	495	452	**EWS300P-12**
12V±20%	53.0	53.0	37.1	768	692	658	**EWS600P-12**
15V±10%	6.7	6.7	4.7	217	196	187	**EWS100P-15**
15V±10%	10.0	10.0	7.0	294	265	252	**EWS150P-15**
15V±20%	22.0	22.0	15.4	545	495	452	**EWS300P-15**
15V±20%	43.0	43.0	30.1	768	692	658	**EWS600P-15**
24V±10%	4.2	4.2	2.9	217	196	187	**EWS100P-24**
24V±10%	6.3	6.3	4.4	294	265	252	**EWS150P-24**
24V±20%	14.0	14.0	9.8	545	495	452	**EWS300P-24**
24V±20%	27.0	27.0	18.9	768	692	658	**EWS600P-24**
28V±10%	3.6	3.6	2.5	217	196	187	**EWS100P-28**
28V±10%	5.4	5.4	3.8	294	265	252	**EWS150P-28**
28V±20%	12.0	12.0	8.4	545	495	452	**EWS300P-28**
28V±20%	23.0	23.0	16.1	768	692	658	**EWS600P-28**
48V±10%	2.1	2.1	1.5	217	196	187	**EWS100P-48**
48V±10%	3.2	3.2	2.2	294	265	252	**EWS150P-48**
48V±20%	7.0	7.0	4.9	545	495	452	**EWS300P-48**
48V±20%	13.0	13.0	9.1	768	692	658	**EWS600P-48**

Power Factor Correction	Active power factor and harmonic correction circuitry ensures compliance to IEC1000-3-2, while improving input power quality, line regulation, AC noise immunity and holdup time. These key features ensure greater system performance and reliability worldwide.
Universal AC Input	Lambda's EWSP Series provides 85VAC to 265VAC input, without the need for external strapping. Full operation from the low line 85VAC of Asia, to the highest lines of 265VAC in many European countries, allows your system to operate effectively in any part of the world.
Input Transient Protection	Integral input transient protection allows the EWSP to ride through input abnormalities typical of industrial factory floor environments. It also ensures system compliance per: IEC1000-4-2 ESD, Level 3 -3 Susceptibility 3V/m -4 Conducted Susceptibility -5 Lightning Strike, Level 3
Meets International Safety Agency Approvals	Safety Agency Approvals to UL1950, CSA950, EN60950 and the CE Mark (Low Voltage Directive) ensure compliance throughout the world.
Wide Range Output Adjustment	Output adjustment of up to 20% can help solve requirements where long leads, diode drops, and unusual voltages exist.
Meets Radiated and Conducted EMI Curve B Requirements	Integral radiated and conducted EMI filtering helps ease system compliance in global markets—without the use of external components.
Current Share	Active current sharing on 300W and 600W models simplifies and increases system reliability for redundant operation.
Delivery From Stock	Available for one day delivery to help quick time to market cycles, unforecasted demand, and inventory reduction programs.

EWSP Series Specifications

AC Input
line.....85-265VAC, 47-63Hz on the EWS300P, 600P.
85-132/170-265VAC auto-selectable,
47-63 Hz on the EWS100P, EWS150P.

Efficiency

	2V	3.3V	5V	12V	15V	24V	28V	48V
EWS100P	-	65%	74%	77%	78%	81%	82%	82%
EWS150P	-	65%	75%	77%	78%	81%	82%	82%
EWS300P	58%	66%	71%	77%	77%	78%	78%	79%
EWS600P	58%	68%	74%	81%	79%	81%	81%	81%

Efficiency is measured at 100VAC.

EMI
Conducted EMI conforms to EN55022-B and FCC Class B. Radiated EMI conforms to EN55022-A and FCC Class A.

Power Factor Correction
0.95 min. at 100/220 VAC max power, compliant to IEC1000-3-2.

Input Surge and Susceptibility
All models meet IEC1000-4-2,4,5 Level 3 and IEC1000-4-3 3V/M.

DC Input
100-330VDC on the EWS300P, 600P. 230-330VDC on the EWS100P, EWS150P.

DC Output
Voltage ranges are shown in tables. All outputs are adjustable over the ranges shown.

Regulated Voltage (mV)

	2V	3.3V	5V	12V	15V	24V	28V	48V
EWS100P, 150P								
ripple and noise	-	120	150	200	200	250	250	250
line regulation	-	20	20	48	60	96	112	192
load regulation	-	40	40	100	120	150	180	384
EWS300P, 600P (mV)								
ripple and noise	100	100	100	200	200	200	200	400
line regulation	10	10	10	24	30	48	56	96
load regulation	20	20	20	48	60	96	112	192

Line regulation is measured from 85-132VAC or 170-265VAC, constant load. Load regulation is measured from no load to full load with a constant input voltage.

Temperature coefficient . . . Less than 1% at −10 to +60°C.

Overload Protection
Automatic electronic current limiting circuit limits the output current from 105-130% of nominal current rating with automatic recovery. The power supply will shut down if an overload condition is maintained for more than 20 seconds.

Overvoltage Protection
Factory set overvoltage protection from 125-160% via internal shutdown method is standard on all models. Refer to the instruction manual for specific settings. Reset by recycling input power.

Holdup Time
Output voltage will remain within regulation limits for 20msec upon loss of AC input, measured at 100/200 VAC, when operating at nominal output voltage and full load conditions.

Remote Sensing
Internal circuitry compensates for total cable drops of up to 0.5VDC.

Inrush Current
14-20A maximum @ 100VAC.
40A maximum @ 200VAC.

Remote On/Off
A TTL compatible signal enables the power supply. An open circuit or a voltage of 2V to 5V applied to the remote on/off terminals will initiate turn-off. A short circuit or 0 to 0.8V signal will cause turn-on for the EWS300P, 600P.

Remote Monitoring Signals
A DC power fail (open collector output) signal is provided on the EWS300P, 600P.

DC Output Controls
Simple, screwdriver adjustment over the entire voltage range.

Input, Output and Signal Connections
All connections are made via terminal blocks. DC output connections are via studs on the EWS600P.

Isolation Rating
3750V RMS input to output (8mm spacing). 2500V RMS input to ground. 500V RMS output to ground.

Cooling
The EWS100P, 150P are convection cooled. The EWS300P, 600P are forced-air cooled via an internal fan.

Operating Temperature Range
Operation from 0 to +50°C.

Mounting
One mounting surface and one mounting position on the EWS100P, 150P. Two mounting surfaces and two mounting positions on the EWS300P, 600P.

Finish
Gray, FED.STD.595 No. 26081.

Physical Data

Package Model	Weight Lbs. Net	Weight Lbs. Ship	Dimensions (inches)
EWS100P	1.9	2.5	2.13 x 3.82 x 7.87
EWS150P	2.2	3.0	2.56 x 3.82 x 7.87
EWS300P	6.2	7.2	4.72 x 3.62 x 7.48
EWS600P	10.0	11.0	7.48 x 3.62 x 7.87

Safety Agency Approvals
All models are under evaluation for EN60950, UL1950, CSA950 and the CE Mark (Low Voltage Directive).

Guaranteed For 3 Years
Three year guarantee includes labor as well as parts. Guarantee applies to operation at full published specifications at the end of three years.

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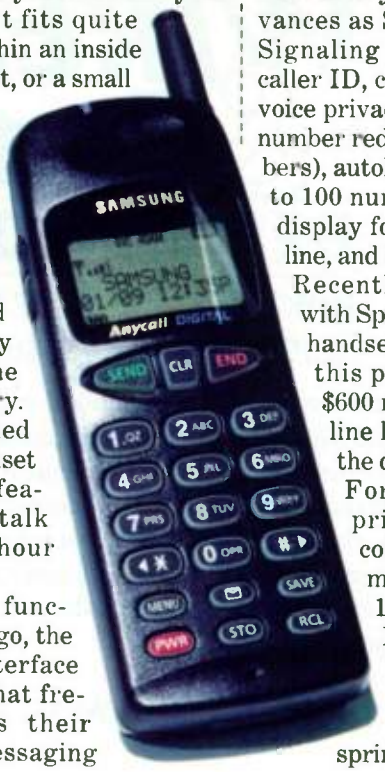
REV. A

Tiny, But Powerful

Wireless phones can sometimes be inconvenient to hold, too big to fit in a shirt pocket comfortably, or just plain bulky. The object of the whole cellular movement was to allow the user to communicate from any location, with the utmost ease. So, while the evolution continues, one cellular handset stands out as being worthy of investigation, the SCH-1101 from Samsung Telecommunications America.

The new handset is of the Code Division Multiple Access (CDMA) Personal Communications Service (PCS) variety. CDMA focuses in on the human voice, delivering crisper-sounding calls. The technology prevents the static and cross-talk frequently found on cellular phones. Digital PCS transmission is designed to be much more secure than traditional cellular phone systems, addressing electronic identification number theft (known as cloning) and the truly obnoxious eavesdropping.

It's a pretty small unit—it measures 5.7 in. long by 2.1 in. wide by 0.9 in. deep—and it fits quite comfortably within an inside suit jacket pocket, or a small pocketbook.



Weighing in at 6.7 oz. with the standard battery, the SCH-1101 has a two-hour talk-time capacity and a 20-hour standby capacity with the standard battery. With the extended battery, the handset weighs 8.9 oz., features a 5-hour talk time, and a 60-hour standby time.

As far as the functions of the unit go, the menu-driven interface targets users that frequently access their memory and messaging applications. The tiny handset is feature heavy, and includes such advances as Short Message Service Signaling Message Encryption, caller ID, call timer, call restriction, voice privacy, power save mode, last number redial (up to the last 10 numbers), autolock, memory storage (up to 100 numbers), large three-line display for twelve characters per line, and icons.

Recently, Samsung partnered with Sprint PCS to distribute the handsets to customers who use this particular carrier. Over $600 million worth of the slimline handsets are involved in the deal.

For more information and pricing on the SCH-1101 contact Samsung Telecommunications America Inc. 1130 E. Arapaho Rd. Richardson, TX 75081; (972) 761-7000; fax (972) 761-7001; e-mail: pr_vantage@mindspring.com.—*DS*

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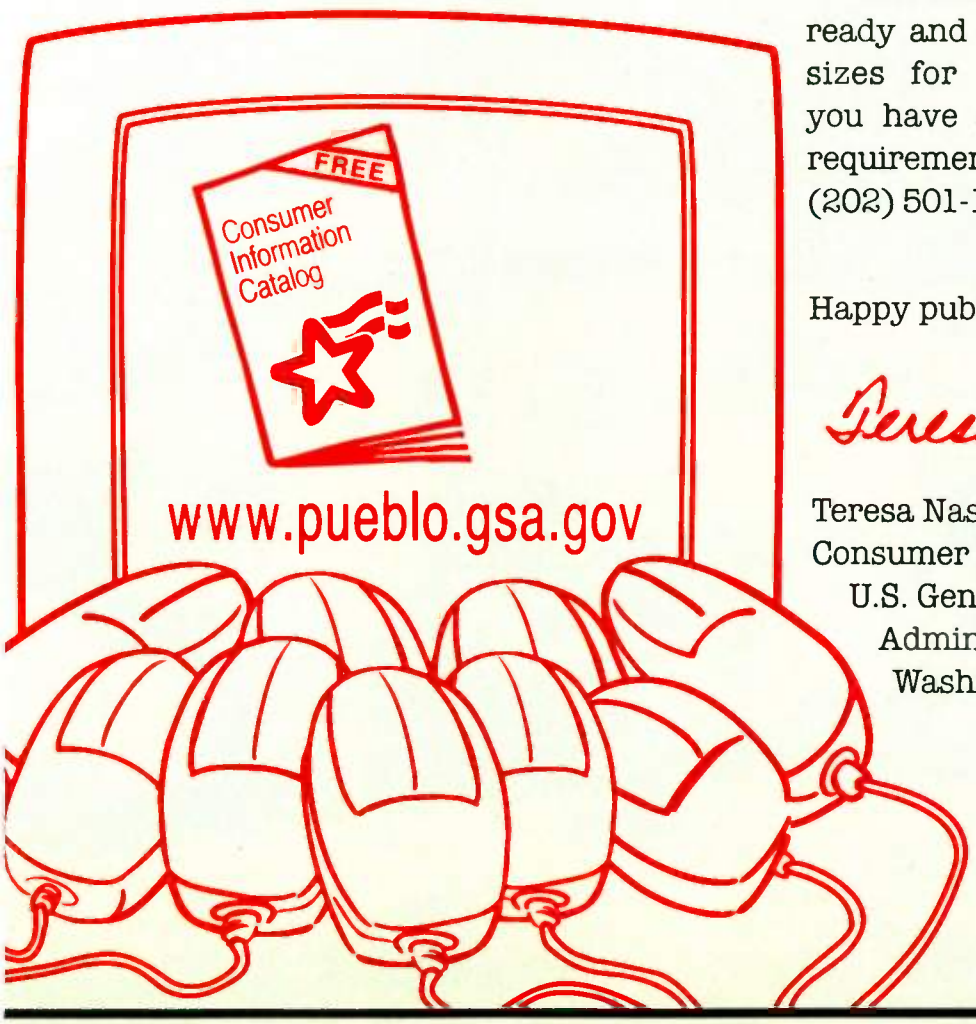

The enclosed ads are camera ready and come in a variety of sizes for easy placement. If you have any special printing requirements, please call me at (202) 501-1794.

Happy publishing!

Teresa Nasif

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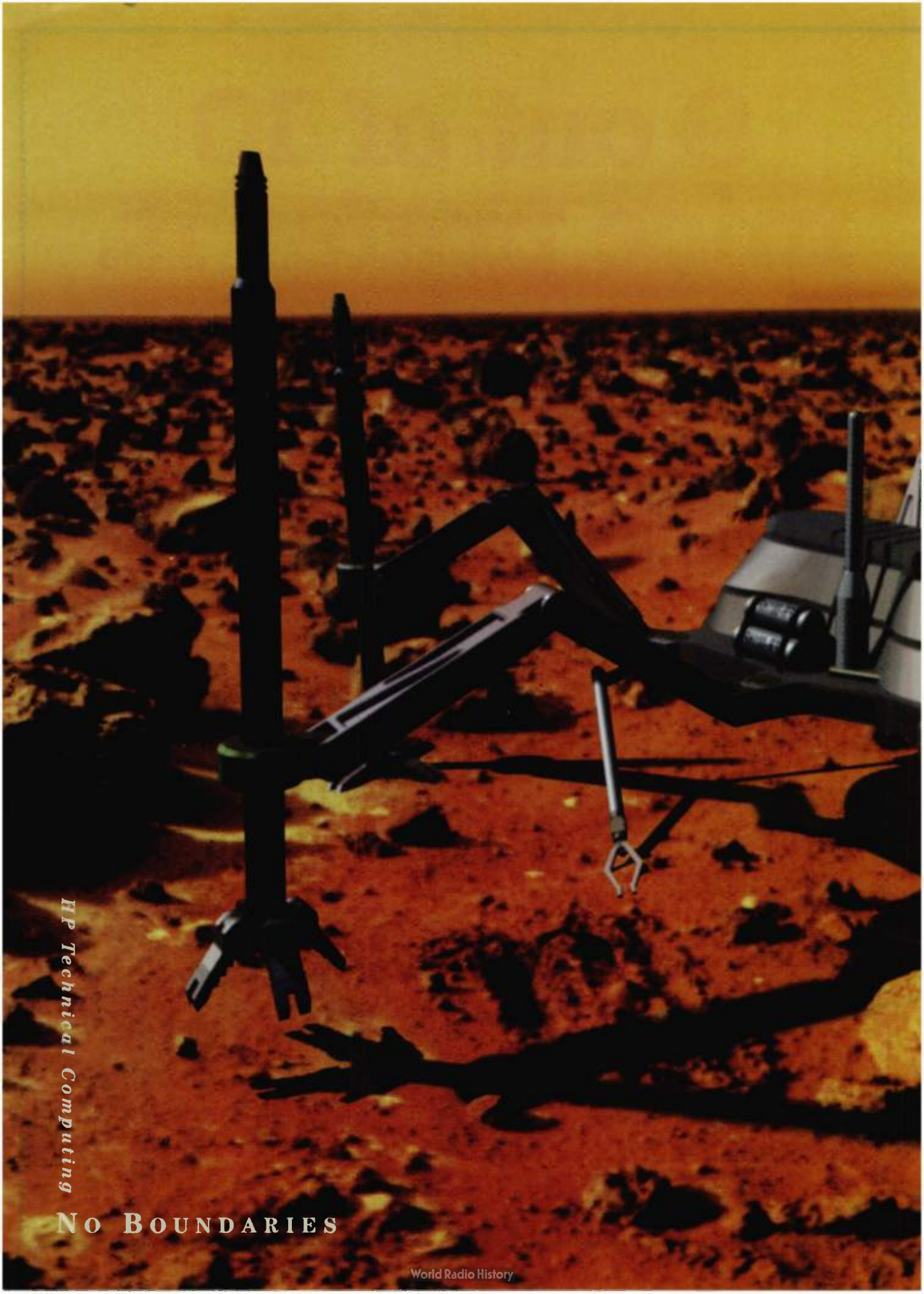

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READER SERVICE 158

Switch-Mode ICs Minimize Off-Line Power Supply Size

With Power Supply Space At A Premium, Two Power IC Makers Are Finding Ways To Put More Circuitry And Components Into Their Switching Regulator ICs.

Frank Goodenough

COVER FEATURE

From computers to test equipment to portable instruments and entertainment products, the complexity is growing while the cases are shrinking. This is making life a challenge for component manufacturers who have to squeeze ever-more sophisticated devices into smaller housings. Off-line power supply makers are not only facing size and mounting constraints, but also must find ways to keep naturally hot-running components cool.

For the most part, the challenges have been met. Those bulky, costly off-line power supplies with their heavy, iron-core 60-Hz power transformers, rectifier bridges, and beer-can sized filter capacitors are relics of the past. Replacing them are supplies designed with switch-mode regulator ICs that run at frequencies of 100 kHz and higher, allowing today's transformers, inductors, and capacitors to be much more compact than their predecessors. Nevertheless, the heat is still on for power semiconductor makers to come up with devices that pack more components into one IC to meet the needs of tomorrow's smaller equipment.

Two companies that have stepped up with innovative semiconductor devices to meet the needs of modern power supply design are Power Integration, Sunnyvale, Calif., and SGS-Thomson, Lincoln, Mass. Power Integration has come up with the TOPSwitch II family of switching regulators, while SGS-Thomson's entrant in this power IC derby is called the VIPer 100. These switchers offer power outputs in the 100- to 150-W range. A typical desktop computer requires a 150-W supply, while a computer monitor draws about 100 W by itself *(Figs. 1 and 2)*.

One way to shrink an off-line power supply is to move the power MOSFET switch from its discrete package and heat sink onto the same silicon die as its controller—the result is a power IC. This approach has taken a long time to become economically feasible. Over the years, the argument has always been that high-voltage discrete power switches (in the past usually bipolar devices, today power MOSFETs) are cheap and so are low-voltage PWM controllers. On the other hand, the power ICs needed for an off-line supply are built on expensive, high-voltage processes. That is, it has always been cheaper to use a discrete power switch and a controller IC—oftentimes, even the controller is built of discrete devices.

The 700-V power ICs of the TOPSswitch II range from 100 to 150 W when driven from either the 100/115-V ac line or a 230-V ac line. On the other hand, the output drops down to between 80 and 90 W when running from a "universal" (rectified) 85-V ac to 265-V ac line.

High-Voltage MOS

All TOPSwitches are built on a patented high-voltage CMOS process that is compatible with virtually any low-voltage CMOS fab (such as a now

antique 5-V/3-μ process). The power device is a large, lateral n-channel MOSFET. It is not (as might be expected) either a lateral, or a vertical, DMOSFET. The process requires just one implant more than is needed in a standard CMOS process. The on-resistance, Rds(ON), of the high-power, 150-W TOP227 runs at a maximum of 3 Ω at 25° C while passing 300 mA.

The 600-V, VIPer100 from SGS-Thomson puts out 100 W operating from a rectified 85/115-V ac line or from the rectified 270-V ac line. It is capable of delivering 50 W when driven from a "universal" supply that can range from rectified 85-V ac lines to rectified 270-V ac lines. The VIPer100 is built on a well-characterized proprietary high-voltage MOS process called VIPower—MO. The process is used for enhancement- and depletion-mode lateral NMOS FETS in a p-well and vertical DMOS power MOSFETs *(Fig. 3)*.

VIPower stands for Vertical Integrated Power. The control and drive circuits are built from the NMOS FETs, while the single power switch is a vertical DMOSFET. Unlike the lateral power switch in the TOPSwitch, it is fabricatedin the traditional manner of most discrete power devices. That is, the current enters through the top of the IC—the FET's source—and exits through the metallized bottom, the FET's drain. While most power ICs employ vertical power devices, their on-resistance is usually pretty high because the vertical current is returned to the top of the die via a horizontal buried layer and a vertical plug. Although both buried layer and plug are low resistance, they can add significant Rds(ON). The on resistance of the VIPers' FET switch runs 2.8 Ω and it is rated at 3.5 A.

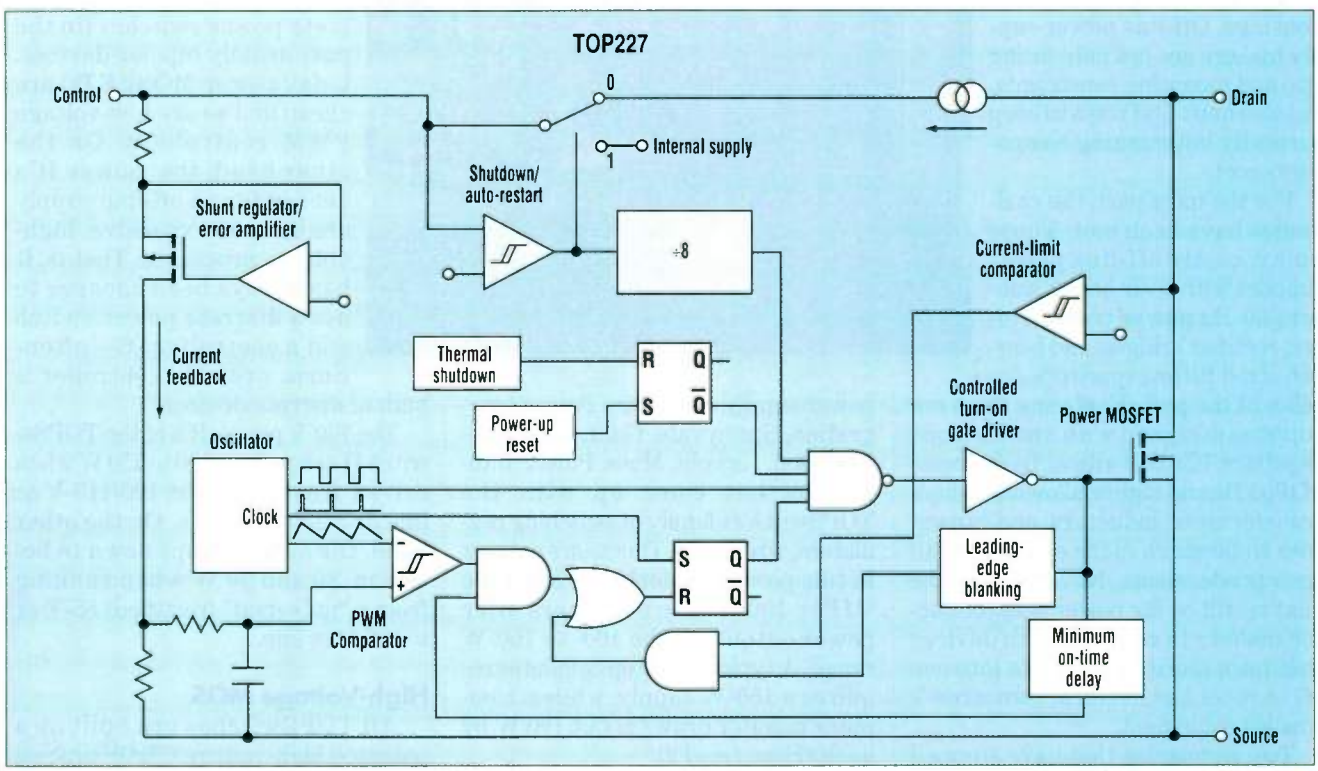
OUTPUT POWER TABLE

TO-220 Package			8L PDIP Package		
Part order number	Single-voltage input (100/115/230 V ac ±15%)	Wide-range input (85-265 V ac)	Part order number	Single-voltage input (100/115/230 V ac ±15%)	Wide-range input (85-265 V ac)
	P_{MAX}	P_{MAX}		P_{MAX}	P_{MAX}
TOP221Y	12 W	7 W	TOP221P	9 W	6 W
TOP222Y	25 W	15 W	TOP222P	15 W	10 W
TOP223Y	50 W	30 W	TOP223P	24 W	15 W
TOP224Y	75 W	45 W	TOP224P	31 W	19 W
TOP225Y	100 W	60 W			
TOP226Y	125 W	75 W			
TOP227Y	150 W	90 W			

The VIPer 100 comes in both a 5-pin "pentawatt" TO-220 package and the SO-10 surface-mount power package whose footprint runs less than 0.24 in^2. It is aimed at applications such as set-top boxes, video recorders, laptop computers, monitors, camcorders, and TV sets. Its use improves the reliability of a system by typically reducing the number of components by 50%.

Just 3 Pins

Power Integration's TOPSwitch family of switching regulators offers a number of unique features .It provides



1. Unique circuits in this off-line IC switching regulator from Power Integrations (the TOP227) requires connections to only three pins, the power FETs drain and source, and a control pin that handles functions such as shutdown and restart.

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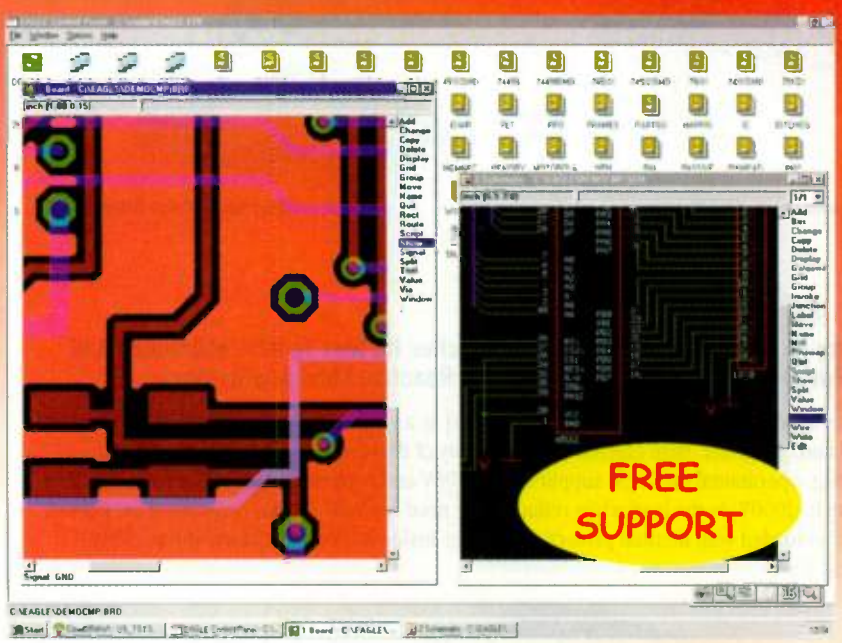

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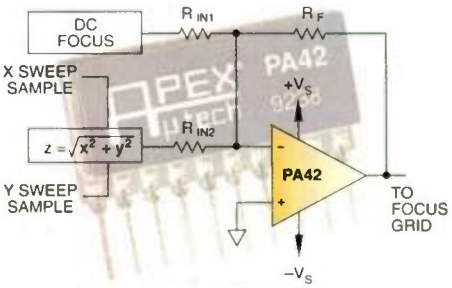
PA42 FREE EVAL KIT!

A Low Cost, High Voltage Combination has this Power Amplifier Stacking up on Piezo and ATE Driver Boards Thanks to a Space-Saving Single-in-Line Package

When you combine the PA42's $17.90 price tag in 10K pieces with its footprint measuring less than one fourth that of a TO-3 package, the PA42 is the choice for high density applications. Its 2mA maximum standby current is also consistent with high density, and remember, this monolithic is rated up to 350V total supply and 120mA output.

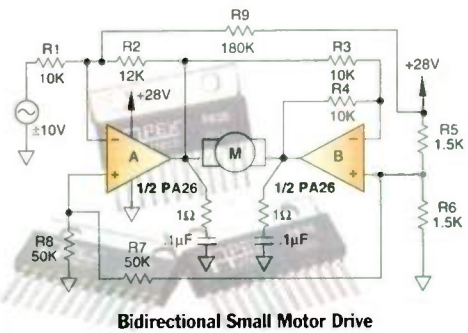


Dynamic Focus, CRT Display

PA26 FREE EVAL KIT!

Two 2.5A Rated Amplifiers on One Die, in One Package, Priced $3.45*, Are the Many Reasons this Power Amplifier is a Popular Fit for Half, Full Bridge Motor Drivers

The PA26 saves valuable real estate by putting two 2.5A rated power amplifiers on a single die, in a single 12-pin SIP package. The PA26 provides the fit for bridge mode configurations or applications designed with multiple amplifiers per board. The PA26 is also extremely affordable priced at *$3.45 in 10K pieces.

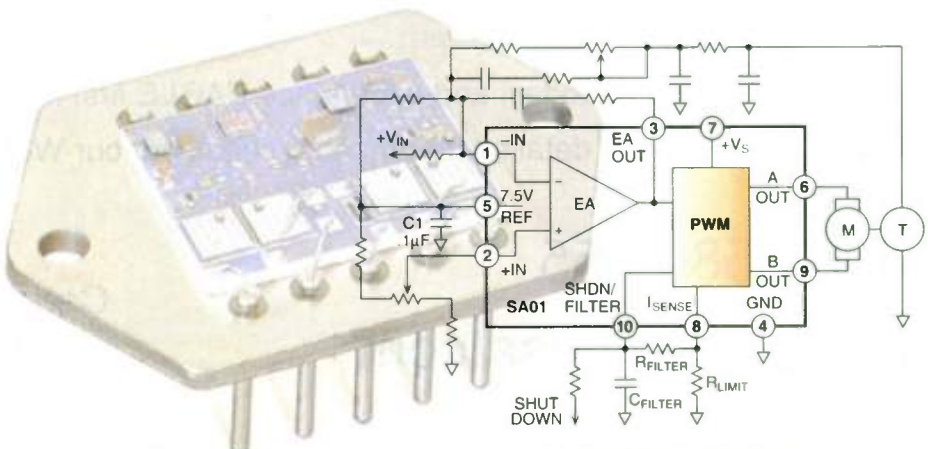


Bidirectional Small Motor Drive

SA01 FREE EVAL KIT!

This Industry First Hybrid PWM Amplifier Switches Its Way To 97% Efficiency And 2000W of Power in Brush Type Motor Control, Reactive Load Applications

Also known as a switching or Class D amplifier, the SA01 is an industry first hybrid PWM (Pulse Width Modulated) amplifier. High efficiency is the beauty of PWM technology, and with a 97% efficiency rating, operational on single supplies up to 100V and capable of 20A continuous, the SA01 can deliver up to 2000W to the load while reducing the need for bulky, space consuming heatsinks. The SA01 is also loaded with thermal protection features inside its hermetic power-dip package measuring just $2in^2$.



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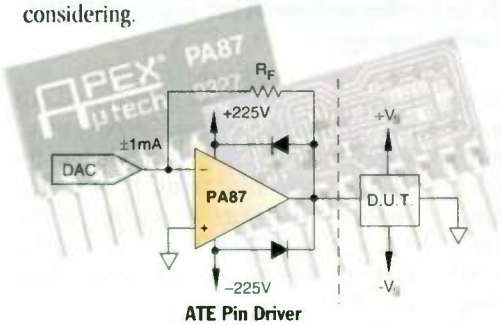
PA87 FREE EVAL KIT!

This Hybrid Keeps its Cool While Running on High Voltage Supplies and Delivering 200mA Continuous Current in Programmable Power Supplies and HV Instrumentation Applications

The PA87 combines a 450V total supply with 200mA of continuous output current while running cool with only 3.8mA max standby current. This makes the PA87 an attractive solution for driving large capacitive loads and powering piezoelectric applications. Its 10-pin hermetic SIP package makes the PA87 a solution that's easy to apply and certainly worth considering.

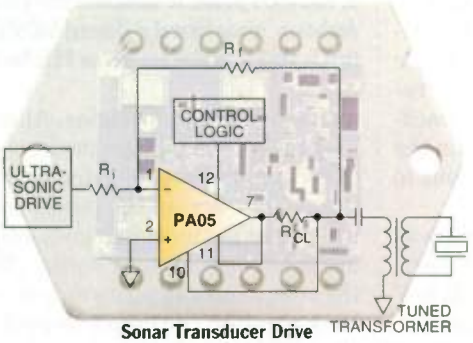


ATE Pin Driver

PA05 FREE EVAL KIT!

More Power, More Speed, More Internal Dissipation Make the PA05 a Power Amplifier Player in Linear, Rotary Motor Drives, and Sonar Transducer Drivers

If it's speed with power you need, then the PA05 provides 30A of output current at a 100V/µs. The PA05 achieves this exceptional speed on a 100V total supply while it internally dissipates up to 250W. A very flexible power op amp, the PA05 features external shutdown control, optional boost voltage inputs and thermally limited output stages.

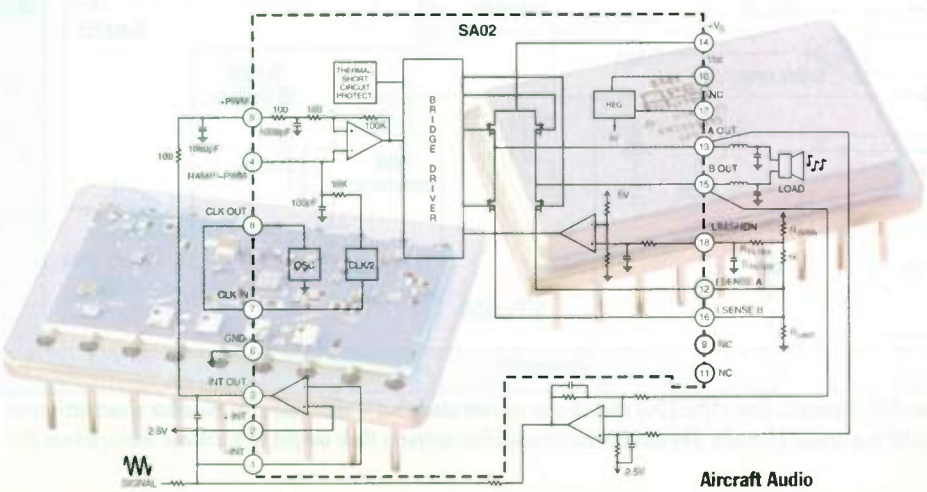


Sonar Transducer Drive

SA02 FREE EVAL KIT!

This complete H-Bridge Hybrid PWM Amplifier Pushes The Envelope With A 250kHz Switching Frequency

The SA02 breaks new ground with a 250kHz switching frequency which translates to a useable power bandwidth out to 25kHz. Designed as a full-bridge amplifier, the SA02 operates on a 16V to 80V supply with a 10A continuous output, which translates to a power delivery of up to 800W to the load. Rated 94% efficient, the SA02 offers a synchronizable clock and three levels of protection, including on-chip thermal sensing and shutdown control. The SA02 also includes a digital input pin.



Aircraft Audio

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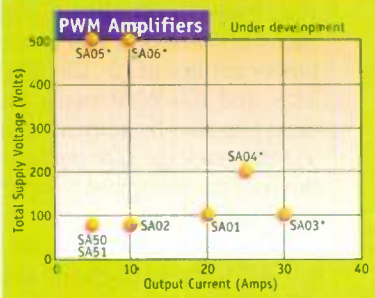
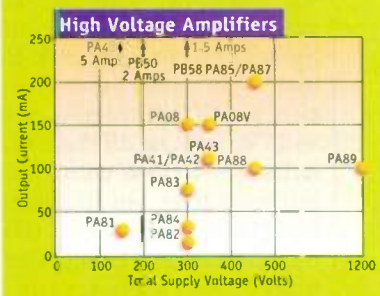
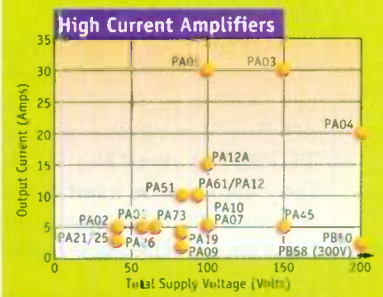
Power Amplifier Solutions







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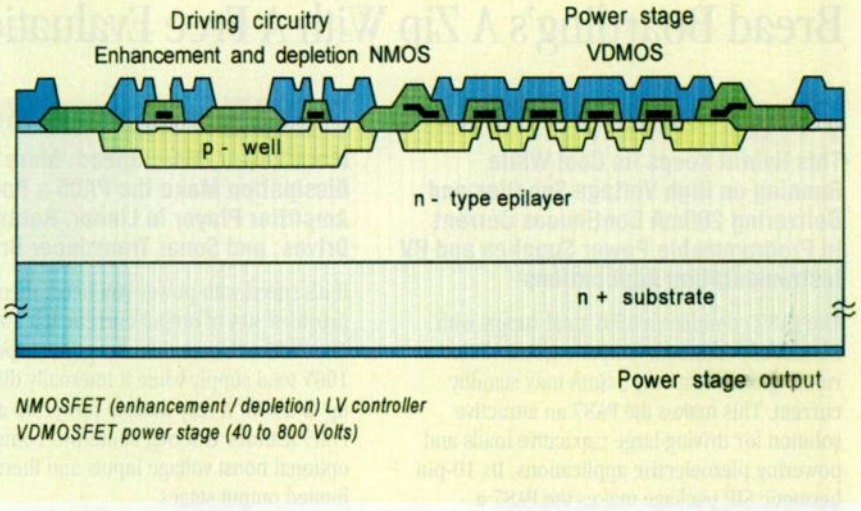
all the functions required by an off-line supply, while connecting up requires just three input/output pins *(Fig. 1 again)*. Therefore, TOPSwitches with power ratings of 12-, 25-, 50-, 75-, 100-, 125-, and 150-W fit easily into a standard low-cost (readily available) 3-pin TO-220 package *(see the table)*. These devices are designed to operate from 100/115/230 V ac.

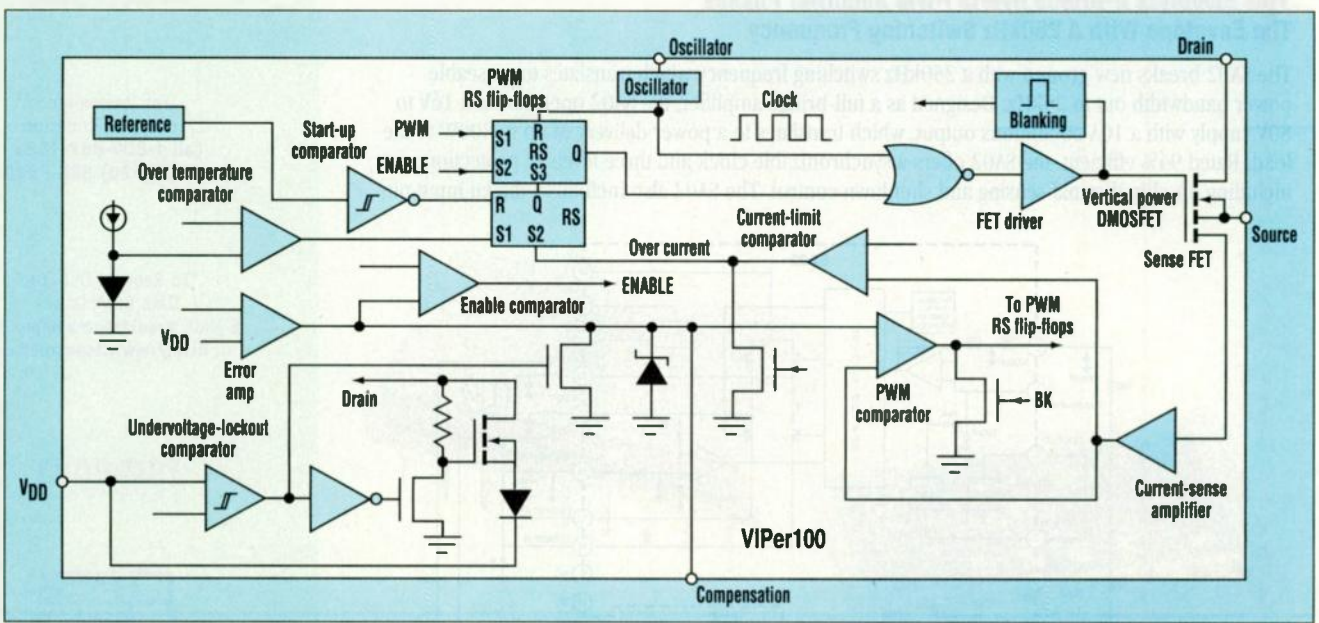
The same TOPSwitches for "universal" wide-input-range applications (85 to 265 V ac) come in a broad array of power ratings: 7-, 15-, 30-, 45-, 60-, 75-, and 90-W . Switching regulators rated at 100 W or more employ TOPSwitch II technology as do the 60-, 75- and 90- W universal devices. In addition, four TOPSwitches rated from 9 to 35 W, running off the 100/115/230 V ac line or 6 to 19 W with a universal input have been put into compact, pc-board mountable 8-pin DIPs. Since only 3 electrical connections are required, the 5 spare pins on the package are used to get the heat from the lead frame inside the package out to the pc board.

TOPSwitches typically operate as voltage-mode PWM flyback converters as illustrated by the 150-W, 5-V off-line converter based on the TOP227 shown *(Fig. 4)*. However, they also can be used to implement the most popular power supply circuits such as the buck-, boost-, or forward-converter topologies. Although they operate in voltage mode, the on-chip current-limit comparator senses the voltage across the power switch which falls as the switch goes into saturation *(Figs. 1 and 4, again)*. When the comparator flips, its output is fed back through the chip's control loop where it combimes with timing and control signals to turn off the power FET. This mechanism provides the cycle-by-cycle current limiting that is typically found in conventional current-mode converters. These switchers run at 100 kHz, a rather low frequency compared to many of today's switcher designs which run at frequencires of 200 kHz and higher, but EMI problems are virtually eliminated.

During startup, the regulator's run off a current source from the drain (input voltage) pin to an on-chip shunt regulator. Zener diodes drop



3. This MOS power IC semiconductor process developed by SGS-Thomson uses enhancement- and depletion- mode lateral n-channel MOSFETs for handling small-signals and a vertical DMOSFET that is similar to discrete power FETs for handling large signals.



2. This off-line IC switching regulator from SGS-Thomson (the VIPer100) operates at current mode but it eliminates the need for a current-sense resistor since cells in the power FET are used in a senseFET mode. The current-sense amplifier converts their output to a voltage which drives the PWM comparator. (See figure 4).

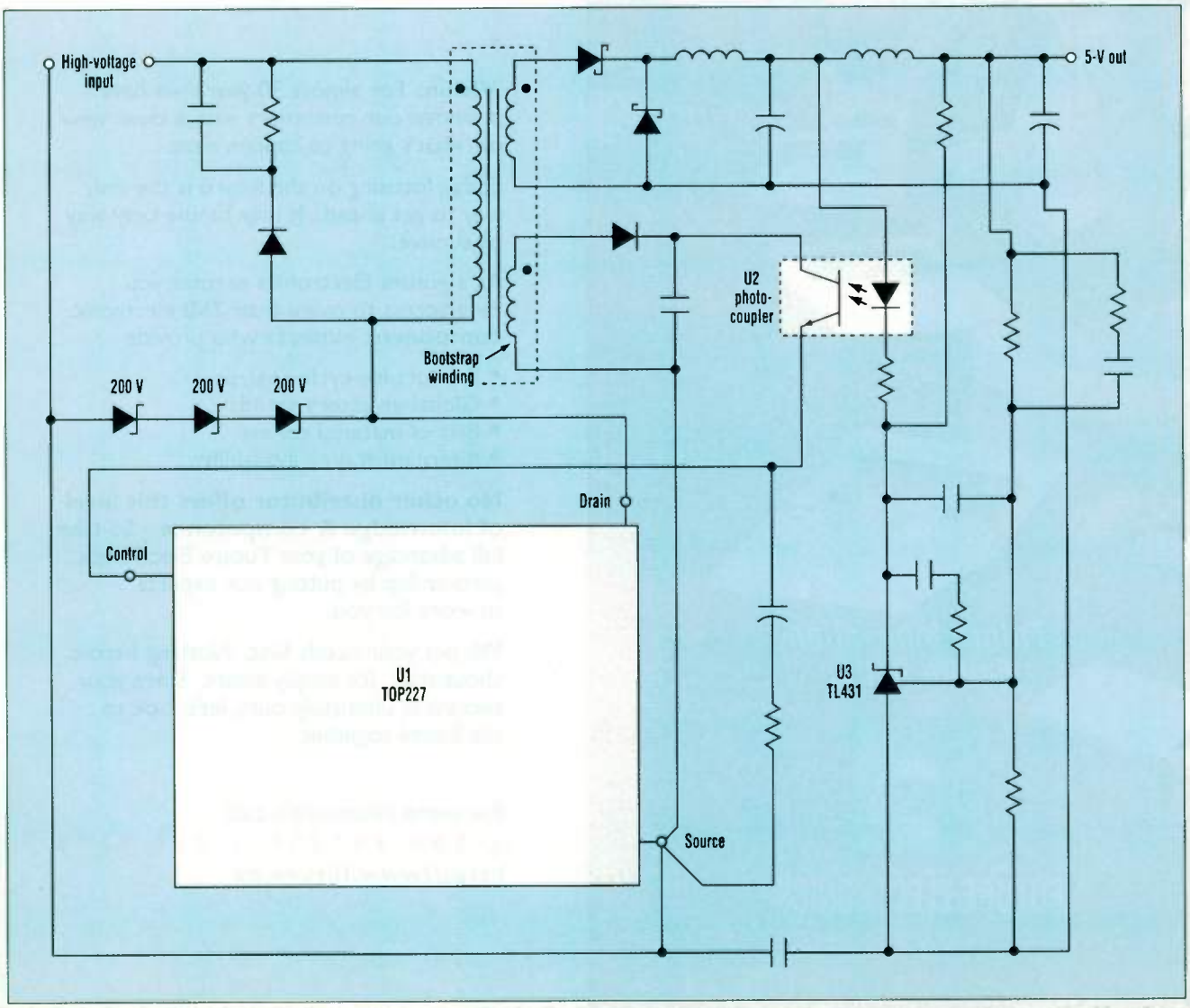
the voltage from the dc input to the drain pin for start up. Once running, the current source is disconnected and the chip is powered—like most flyback regulators—from the rectified output of the bootstrap winding (also called the bias winding) on the transformer *(Figs. 1 and 4, again)*. The chips also can get their voltage feedback from this primary-side source or they can operate with an optocoupler (U2) and reference (U3) on the secondary side *(Fig. 4, again)*. The collector of the optocoupler's output transistor connects to the output of the bootstrap winding and its emitter provides the feedback to the control pin of the TOPSwitch.

Power Integrations announced a TOPSwitch I, 100 W off-line regulator, about two years ago (ELECTRONIC DESIGN, *June 27, 1994, p. 55*). However, the 150-W TOPSwitch II die (an area of 21,000 mils^2) is about 2% smaller than than the earlier TOPSwitch-I . As might be expected, it took a combination of design tweaks and careful layout to reduce the die size. First, the designers modified the circuit's controller so that the power switch operates close to 50% duty cycle most of the time. Then they increased the accuracy of the current-limit circuit so that the initial current is close to 70% of the final operating current. The initial current through the TOPSwitch I die ran about 20% of final current— about what could be expected from a discrete design. Essentially, the earlier TOPSwitch die was overdesigned in order to handle overcurrents for short periods of time. The new die is layout critical.

Under low-load conditions, the chip goes into a low-power standby mode.

Sense FETs Make Sense

The complete VIPer100 PWM power IC operates at up to 200 kHz as a current- mode flyback-topology switching regulator. Unlike most



4. The TOP227 150-W off-line switching regulator IC can be the controller in a power supply capable of running a typical desktop PC. Although it runs at voltage mode, it provides cycle-by-cycle current limiting by sensing when its power switch goes into saturation.

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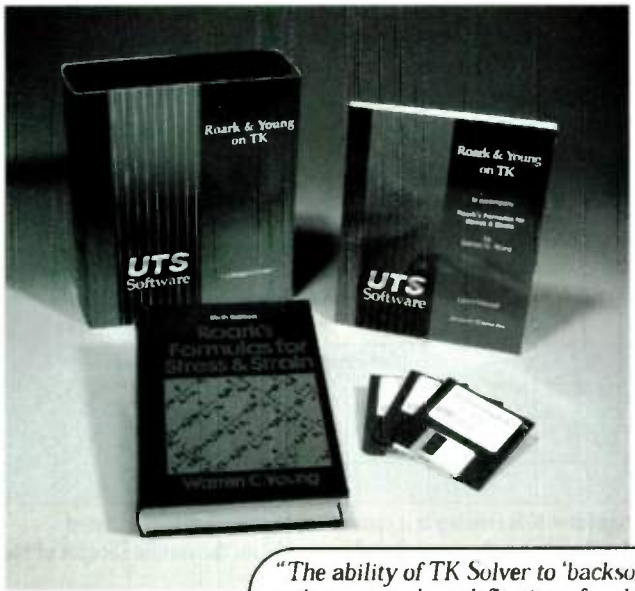

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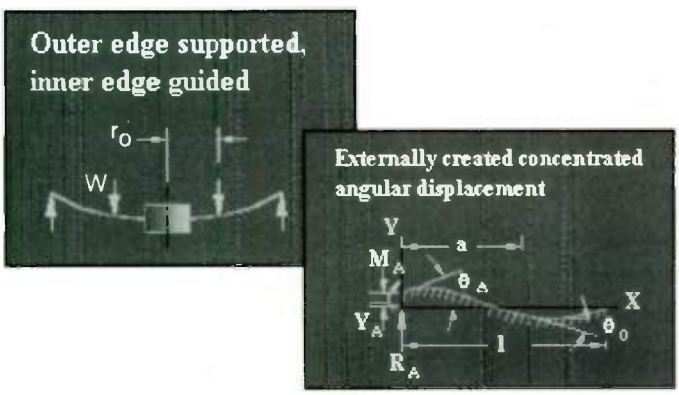

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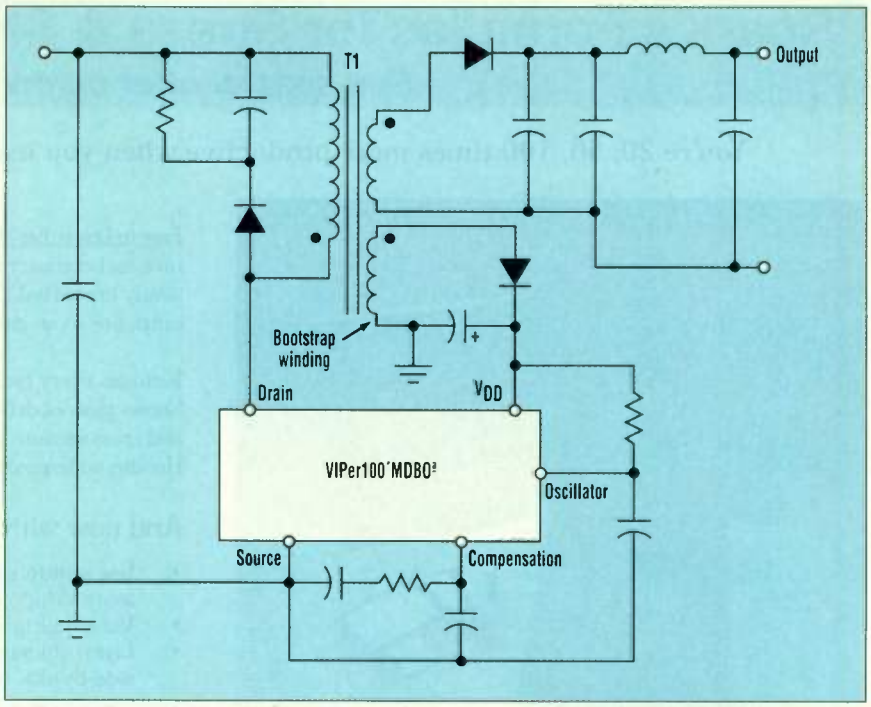

5. This off-line switching regulator IC is running in a current-mode, pulse-width modulated flyback topology. Voltage feedback is coming from the primary side via the rectified output of the bootstrap winding of transformer T1.

current-mode regulators, it needs no expensive, bulky, power-grabbing current-sense resistor. Instead, a group of the on-chip vertical power MOSFET cells are used as "sense FETs." Their current is proportional to the current through the FET switch *(Fig. 2, again)*. Current-mode operation provides inherent feed-forward operation and line regulation superior to that of typical voltage-mode operation controllers. It also removes a pole from the control loop that simplifies the compensation. The circuit also provides current-limit protection.

Like most of today's flyback switchers built with controller ICs and a discrete power switch, the regulator operates successfully with primary-side voltage feedback from the bootstrap winding supplying power for the chip at the V_{DD} pin *(Fig. 5)*. Alternatively, it operates with secondary-side voltage feedback via an opto-coupler.

A current source from the Drain pin (rectified line-voltage input via the flyback transformer) powers the chip at start up. After it is running, and getting power from the bootstrap winding, the current source is switched off. Under low-load conditions the chip goes into a low-power standby mode. In addition to its current limit feature, the chip incorporates a complete suite of load and self-protection features including over voltage and over temperature protection, undervoltage lockout, soft-start, and an external shutdown input. Such features are increasingly important to ensure reliable system operation.

Price And Availability

It should be noted that over 50 million of Power Integrations' TOPSwitch I ICs have been produced and delivered. Pricing for TOPSwitch II family members in quantities of 10,000 starts at $0.98 each for the 9-W/6-W (U.S. or European ac lines/"Universal" supplies) TOP221P in the 8-pin DIP. The 150 W TOP227Y goes for $2.24 each in similar quantities. Samples are available now, with reference design boards available within 60 to 90 days.

Power Integrations Inc., 477 N. Mathilda Ave, Sunnyvale CA; (408) 523-9200.

The VIPer100, which comes in a die size of 24 mm2, is priced at $1.80 each in 10,000-unit lots.

SGS-Thomson Microelectronics, 55 Old Bedford Rd., Lincoln, MA 01773; (617) 259-0300. **CIRCLE 550**

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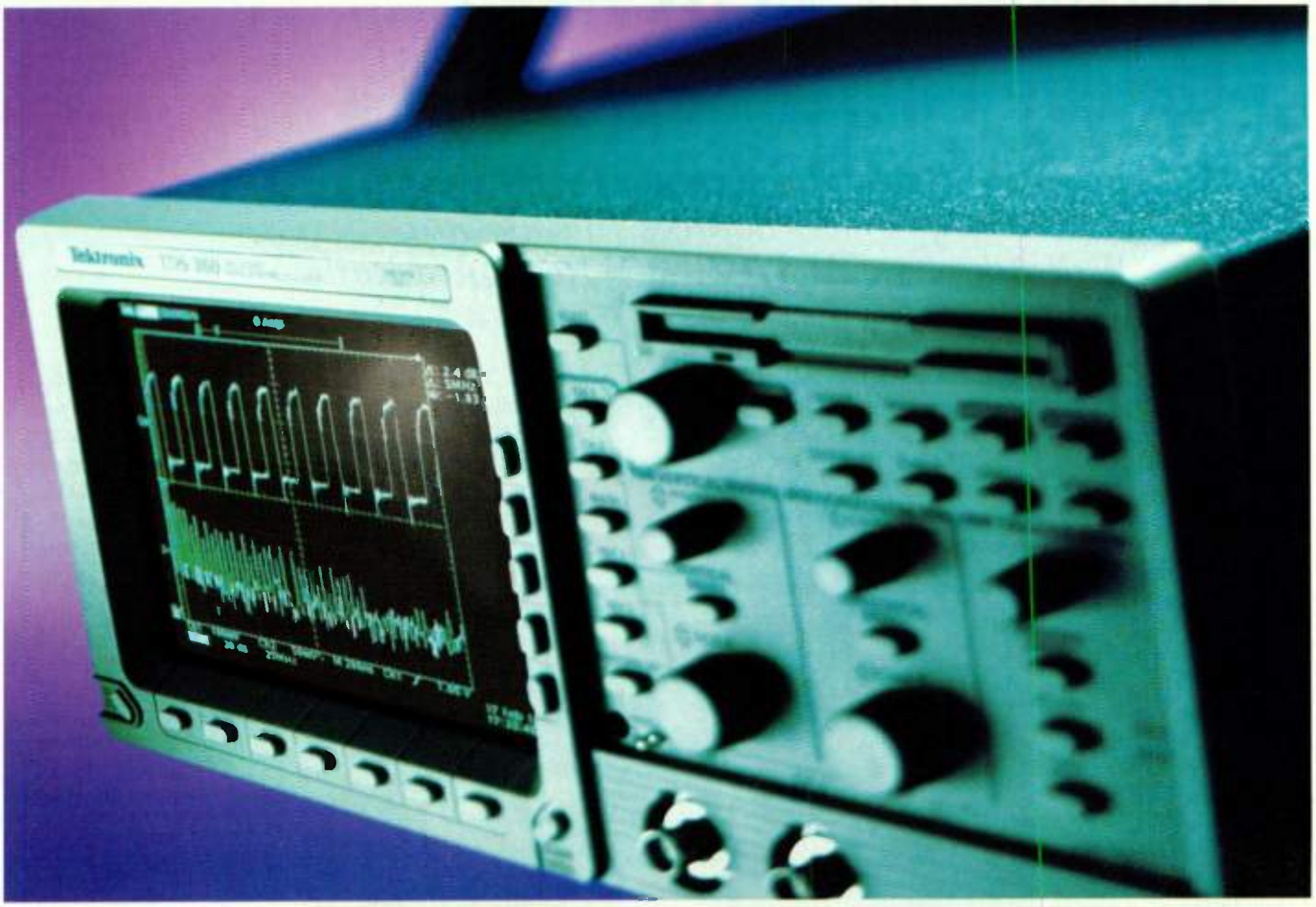

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Simply buy the TDS360 by July 31, 1997, and Tektronix will give you a P5100 passive 100x probe free. Call your local distributor for details. *Suggested retail price, USD.

Tektronix

Portable PC CPUs Need Unique Power Supplies

Portable Personal Computer CPUs Need Efficient, Low-Voltage Power Sources To Run Off Batteries, Wall Adapters, And 5- Or 3-V Regulated Rails.

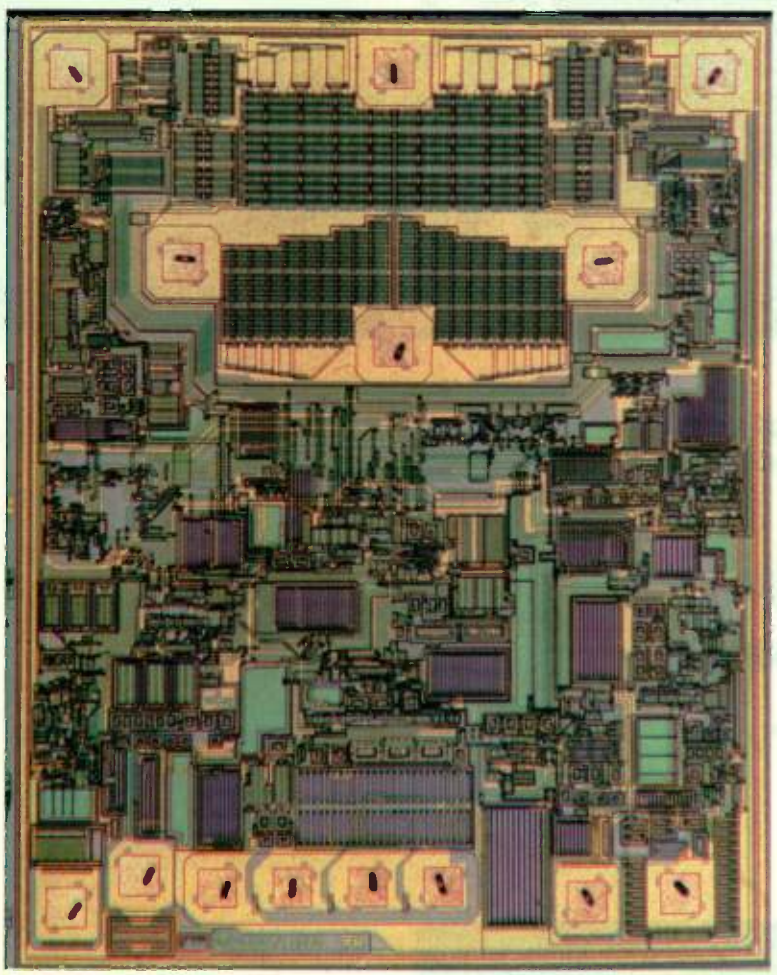
Frank Goodenough

SPECIAL REPORT

Portable PC power supplies that convert battery stack voltages into the levels required by CPUs must be optimized for efficiency to minimize battery drain. For the most part, notebooks and laptops should be able to run for at least six hours while executing the advanced desktop-like programs appearing in the newest machines. While it might seem obvious that efficiency is optimized using a single PWM buck-regulator switcher (dc-dc converter) as the power source, current practice is to employ two switchers, and in some computers, three or more.

The use of multiple converters offers system designers a way to put the power where it is needed most. That is, converters can be distributed geographically throughout the PC to handle some of the problems brought on by feature upgrades. For example, to suppress software-induced transients, the CPU supply must be located as close as possible to the chip itself—ideally at the CPU supply pins. The ability to distribute power converters translates into other benefits as well: The units can be placed where the most space is available, or where their heat dissipation will not degrade performance or reliability, or where it is simplest to get the heat out of the case.

The high-speed CPU ICs in today's battery-powered machines run off a range of sub-5-V supply voltages similar to those required by their desktop siblings (*For information on power sources for CPUs in desktop PCs and servers, see* ELECTRONIC DESIGN, *Jan. 20, p. 31 and p. 44*). Supply voltages range from 2.2 to 2.9 V. Current draw is in the range of 2.5 to 3 A. Many of today's handheld consumer, laboratory, and medical devices and systems are based on the same microprocessors.



Art Courtesy: Unitrode

Two major differences distinguish the power-source requirements of portable PC processors from those in desktop PCs. For starters, maximum power is limited to 10 W (to keep the tightly packed PC's plastic case from melting). Not only that but the CPU chip does not get to pick its supply voltage with a 4- or 5-bit code. That is, the designer and manufacturer of the PC know beforehand the voltage that must be supplied to the CPU. Secondly, converters must be ultra-efficient at both high and low load currents. Efficiency is vital when load current is low because the CPU in most portable systems puts itself into an idle or sleep mode when it is not actively processing data. In addition, it often cuts the load to near-zero under software control, for example, between keystrokes. In many typical applications, the load current is minimum but not negligible.

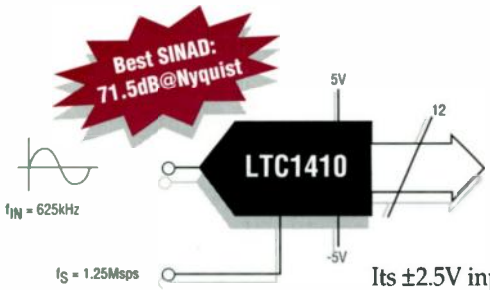
According to many sources, the next 18 months should see CPU IC power demands rise to over 10

LINEAR TECHNOLOGY

LinearSolutions
Data Conversion

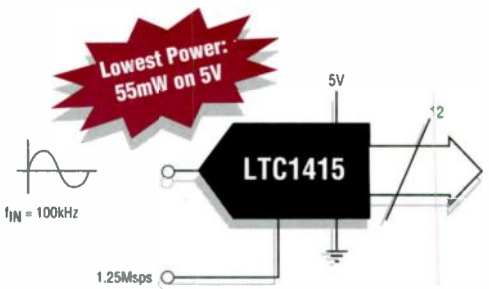
March 1997

The Best Choices for 12-Bit 1.25Msps ADCs!



Searching for the best 12-bit ADC performance at 1.25Msps for your high speed communications design? Wish you had more choices? Look to *The New Choice in Data Conversion:* Linear Technology.

For wideband applications, the LTC1410 has the best INL, the best SINAD and NAP/ SLEEP modes for the lowest power consumption. Its 71.5dB SINAD at Nyquist is unmatched for high speed communications and telecom applications. Its ±2.5V input range is ideal for use with high performance op amps.



Want more choices? For single 5V applications, the LTC1415 has the industry's lowest power, 55mW. It delivers 72dB SINAD and 1LSB DNL and INL, making it perfectly optimized for imaging, communications, multiplexed and high speed data acquisition.

New!

The LTC1410 and LTC1415 are free of pipeline delay so they can take single shot measurements or run continuously. (Competitive devices have up to three cycles of latency and cannot support discontinuous applications.) This and their flexible DSP interfaces make them top performers in either event driven or continuous sampling systems. And our space saving SSOP packages give the smallest footprints available.

When the highest performance ADCs also have the smallest size and the best price, there is clearly only one choice: Linear Technology.

Table—5V 1.25Msps ADC Comparison

	LTC1415	9221
Power at 5V	55mW	60mW
INL (Max)	±1LSB	±1.2LSB
NAP/SLEEP	Yes	No
Data Latency	No delay	3 cycles
Package	SSOP-28	SO-28
Price*	$10.90	$11.90

*1000-piece quantities

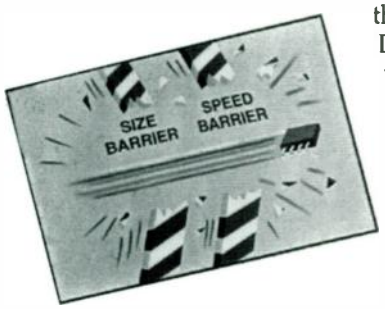
Circle No. 210

In This Issue...

Fast! The Fastest 12-Bit ADC in SO-8!

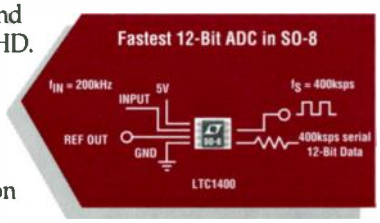
Get 70dB SINAD at Nyquist and Save Space

The LTC1400 is the industry's first 400ksps 12-bit serial A/D Converter in an SO-8 package. This tiny device packs in a 200ns sample-and-hold, a precision reference and a 3-wire serial interface to create the perfect device for DSP applications where high speed and small size are critical.



The LTC1400 has the smallest footprint available and true 12-bit performance at Nyquist. Maximum DC specs include 1LSB DNL and INL, and 25ppm/°C drift for the reference over temperature. The LTC1400 converts 0V to 4.096V unipolar signals from a single 5V supply or ±2.048V bipolar signals from ±5V supplies. Guaranteed AC performance includes 70dB SINAD and –76dB THD.

For high speed data acquisition systems, the LTC1400 offers two power savings modes. These allow the ADC to sample quickly but save power between samples. In NAP mode, it consumes only 6mW and can wake up and convert immediately. In SLEEP mode it uses just 30µW. At $9.95 in 1000-piece quantities, the LTC1400 is the only choice for 400ksps performance in an SO-8 package.



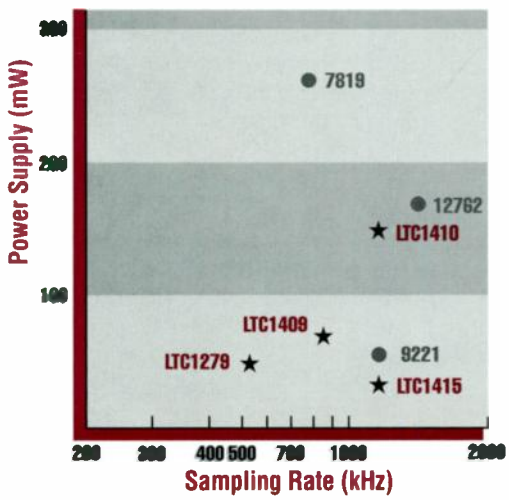
Circle No. 212

Now in SSOP: High Speed ADC Family

Faster, Better, Lower Power and Now Smaller Size

Linear Technology's high speed 12-bit ADC family has grown again and is now the smallest in the market—available in Shrink Small Outline Packages (SSOPs)!

Power Consumption of High Speed 12-Bit ADCs



Table—High Speed Parallel 12-Bit ADC Family

	LTC1279	LTC1409	LTC1410	LTC1415
Sampling Rate	600ksps	800ksps	1250ksps	1250ksps
Power Supply	5V or ±5V	±5V	±5V	5V
Power Consumption	60mW	80mW	150mW	55mW
SINAD at Nyquist	70dB	72dB	71dB	72dB*
Packages	SSOP-24 SO-24	SSOP-28 SO-28	SSOP-28 SO-28	SSOP-28 SO-28

* At f_{IN} = 100kHz

These high speed ADCs span a range of sampling rates from 600ksps to 1.25Msps.

This family is ideally suited for communications applications including single-pair or dual-pair T1 and E1 applications. Excellent SINAD specifications and low power make them excellent choices for undersampling and high speed data acquisition applications as well. They offer both NAP and SLEEP modes for optimum power consumption in event-driven applications.

The industry's smallest footprint is the latest reason to look at our high speed 12-bit ADC family. See why we are *The New Choice in Data Conversion:* Linear Technology.

Circle No. 214

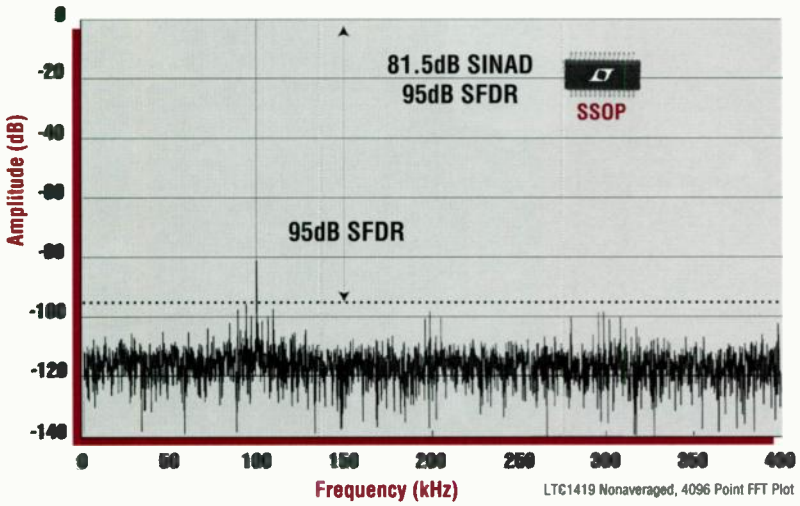
New!

LTC1419: Upgrade Your System with 81.5dB SINAD at an Affordable Price

The Cleanest 14-Bit, 800ksps ADC Offers DNL of ±1LSB Over Temperature, Consumes Only 150mW

Linear Technology now offers you an upgrade path for your existing high performance 12-bit system without resorting to expensive hybrid A/D converters. The LTC1419 is an 800ksps 14-bit ADC that has 81.5dB SINAD and 95dB SFDR, the cleanest in the industry. It's ideally suited for demanding telecom, IF down conversion, undersampling and multiplexed data acquisition applications.

With 20MHz full power bandwidth sampling, the LTC1419 gives you the cleanest 14-bit performance—setting your high speed communications system above the rest. A maximum DNL of ±1LSB over temperature ensures clean 14-bit DC performance as well. The 800ksps LTC1419 has no pipeline delay such as found with multistep architectures.



LTC1419 Nonaveraged, 4096 Point FFT Plot

The LTC1419 consumes only 150mW of power from ±5V supplies and has NAP and SLEEP shutdown modes. It comes in 28-lead SO and SSOP packages and has similar pinouts to Linear Technology's high speed 12-bit parallel A/D converters, such as the LTC1415 and LTC1410, simplifying your upgrade path to 14-bit resolution. Pricing for the LTC1419 begins at $16.80 in 1000-piece quantities.

Circle No. 220

New Data Conversion Solutions Brochure

The *1996 Data Conversion Solutions* is a 52 page brochure that contains LTC's growing line of data conversion products, namely A/D converters, DACs, multiplexers/ switches and references as well as practical tips on how to apply them. There are 60 products described and 24 application notes for your review.

Circle No. 222

For more details, contact Linear Technology Corporation, 1630 McCarthy Blvd., Milpitas, CA 95035-7417, Web Site: www.linear-tech.com. (408) 432-1900. Fax: (408) 434-0507. For literature only: 1-800-4-LINEAR.

LINEAR TECHNOLOGY

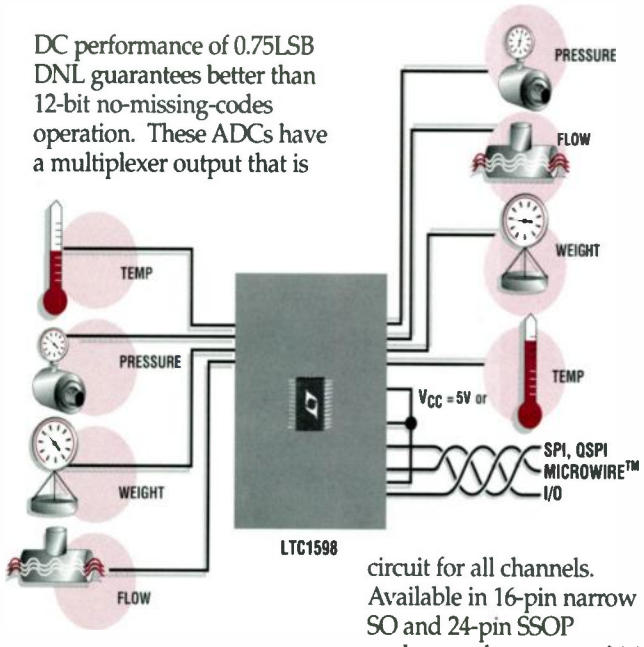
FROM YOUR MIND TO YOUR MARKET AND EVERYTHING IN BETWEEN

Lowest Power 4- and 8-Channel ADCs

The LTC1594/1594L and LTC1598/1598L are 4- and 8-channel 12-bit micropower ADCs for single 5V and 3V applications. These small footprint ADCs are ideal for remote process control, portable data acquisition and other space conscious, power sensitive applications.

The 5V LTC1594 (4-channel ADC) and LTC1598 (8-channel ADC) typically draw just 320µA at 16.8ksps sampling rate while the 3V LTC1594L/1598L draw only 160µA at 10.5ksps. They all automatically power down to 1nA when not converting. These are the lowest power multiplexed 12-bit ADCs in the industry.

DC performance of 0.75LSB DNL guarantees better than 12-bit no-missing-codes operation. These ADCs have a multiplexer output that is separate from the sample-and-hold input which allows for one signal conditioning circuit for all channels. Available in 16-pin narrow SO and 24-pin SSOP packages, they start at $6.15 for 1000-piece quantities.



Circle No. 216

Micropower Operation Down to 480µW, These 12-Bit Multiplexed ADCs Offer 0.75LSB DNL

Micropower Dual and Quad DACs Fit in Tight Quarters

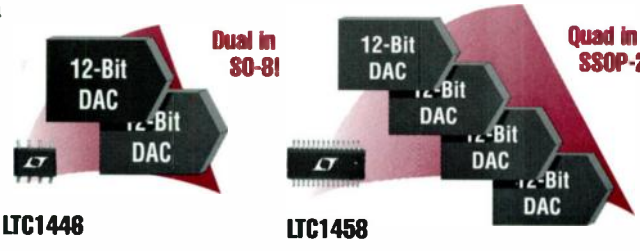
The LTC1446/1446L, LTC1454/1454L and LTC1458/1458L are a new family of 12-bit dual and quad DACs. A 3-wire serial interface allows several of these DACs to be daisy-chained to save board space. They are perfect as system calibration DACs in industrial control systems or in portable battery powered instruments.

Key Features:

- Micropower
- Rail-to-Rail output amps
- Onboard reference
- 5V or 3V supplies

Table—Micropower V_{OUT} DAC Family

	LTC1446	LTC1446L	LTC1454	LTC1454L	LTC1458	LTC1458L
Type DAC	Dual	Dual	Dual	Dual	Quad	Quad
Supply Voltage	5V	3V	5V	3V	5V	3V
Supply Current	1.0mA	650µA	700µA	450µA	1.1mA	800µA
DNL (Max)	0.5LSB	0.5LSB	0.5LSB	0.5LSB	0.5LSB	0.5LSB
Packages	DIP-8	DIP-8	DIP-16	DIP-16	SO-28	SO-28
	SO-8	SO-8	SO-16	SO-16	SSOP-28	SSOP-28
Price-1K	$6.40	$6.50	$6.60	$6.70	$11.75	$12.50



Circle No. 218

Dual DAC in SO-8 Leads Family of Dual and Quad 12-Bit DACs with DNL of Only ±0.5LSB Max

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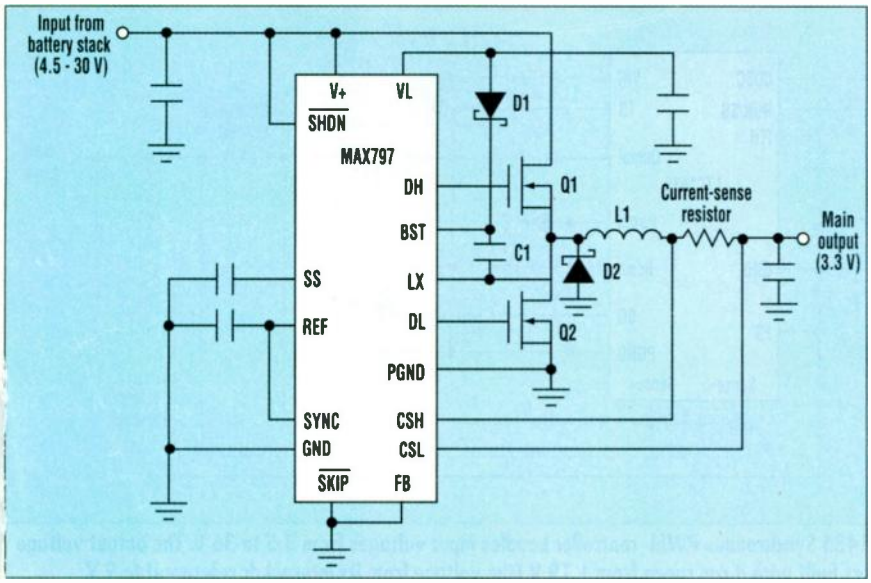


1. A typical battery stack's output voltage is converted to a 3.3-V rail by a synchronous PWM controller such as the MAX797, which drives a MOSFET switch (Q1) and a synchronous rectifier MOSFET (Q2) which replaces the usual Schottky diode.

W while operating voltages drop below 2 W. That implies currents jumping to 5 A or more. Like their desktop counterparts, many of the processors and/or their systems also require at least two different supply voltages. These so-called split-plane processor chips use a low voltage (2.9 or less) for their core and 3.3 V for logic and I/O. In most cases, the rest of the system's ICs use 3.3 or 5 V. Many systems also have a 12-V rail for peripherals.

Many semiconductor suppliers recommend using two separate switchers, one to take the voltage from the battery pack down to 5 V or 3.3 V, and a second to take it below 5 V or below 3.3 V, even though it means taking efficiency hits from two converters. Moreover, there are practical reasons for using two converters or three converters if split-plane processors are being powered (its not just a way to sell more silicon).

Here's the problem. At very high input to output voltage ratios—for example, when converting from 30-V or higher battery stacks to power rails below 3.3 V at typical switching frequencies between 100 kHz and 1000 kHz—in a typical fixed-frequency PWM converter, the duty cycle drops as the load drops, and the minimum on time drops with it. However, switching losses climb (at high voltages, they can approach conduction losses) and the efficiency drops. In addition, the very short on-times of the switch make it difficult for the supply to respond to fast load-dropping transients. They call for even shorter on-times instantly, an impossible task in many converters.

Sharing The Load

System designers and power supply vendors have been talking about distributed power for a long time and it is widely used in mainframes as well as telecom, HVAC, industrial, and military systems. But it has been slow in making headway into the instrument, small-system, and PC arenas.

Most systems using distributed power eliminate the system's "monster" power supply, with its multiple, well-regulated, low-voltage/high-current outputs. These supplies are usually stuck in some remote corner of the system where space was made available at the last minute. (Thus, one power-supply vendor's custom supply was nicknamed "The Oklahoma" because of its shape—the available space). In such a system (which may fill many equipment racks), the power-wiring harness and the IR drops in the individual supply lines soon become nightmares. And the resulting poor regulation at the ends of these lines has helped create large families of linear regulator ICs.

Systems using distributed power replace the "monster" supply with a simple power supply that produces a high-voltage dc distribution bus. Bus voltages range from 48 V (a telecom industry standard because it is said to be the highest, non-lethal dc voltage) to over 300 V (found in some main frames). The higher the voltage, the lower the voltage and power losses. Wherever power is needed, a dc-dc converter/regulator module produces it from the bus

Consequently, as illogical as it may seem, the PC industry is turning the principles of distributed power on its head by distributing low voltages (5 and 3.3 V), at high currents. It should be noted that when 12 V is available it is often employed for power distribution, but in battery-powered PCs, the high-voltage battery output is rarely distributed to multiple converters.

PORTABLE POWER IC SUPPLIERS

Harris Semiconductor	1-800-4HARRIS
Linear Technology Corp.	(408) 432-1900
Linfinity	(714) 898-8121
Maxim	(408) 737-7600
Micro Linear	(408) 433-5200
National	(800) 272-9959
Power Integrations	(408) 523-9300
Raytheon	(415) 966-7734
Semtech	(805) 498-2111
Siliconix/Temic	(408) 567-8220
Unitrode	(603) 424-2410

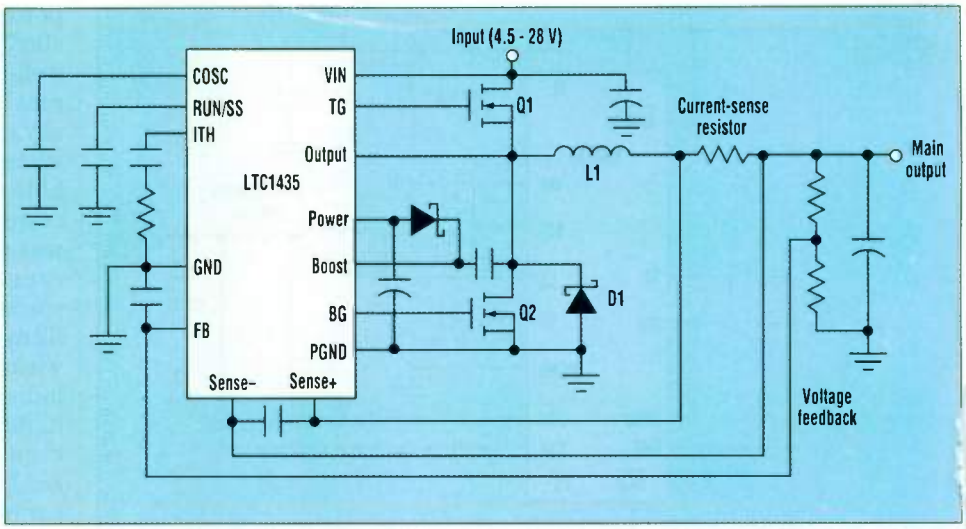
The above is a sampling of companies that manufacture portable power ICs. However, it is not a complete listing.

Moreover, no other voltage has been chosen as a standard. However, 24 and 48 V are being talked about for systems in which tens of amperes must be pumped around.

A typical solution to getting sufficient current from a battery stack usually consists of two or more fixed-frequency, synchronous, PWM-controller-based converters. Synchronous converters are usually more efficient than those using Schottky diode rectifiers.

In synchronous converters, a MOSFET switch (Q2), operating as a synchronous rectifier, replaces the Schottky "catch" diode commonly connected between the output and ground *(Figs. 1 and 2)*. Circuitry inside the controller turns Q2 on when it turns off the controller's MOSFET switch (Q1). Many synchronous converters employ both FET and Schottky to gain a few additional percent efficiency at low currents.

Some silicon vendors offer controllers that can handle input voltages below 5 V as well as the 30 V at the battery stack. Output voltages run greater than 5 V and below 2.9 V. Designers using these devices can employ several controllers of the same type to create both the 5 V/3.3-V system rail and the low-voltage rail for the processor or its core.



3. The LTC1435 Synchronous PWM controller handles input voltages from 3.5 to 36 V. The output voltage of converters built with it can range from 1.19 V (the voltage from its internal dc reference) to 9 V.

Have It Your Way

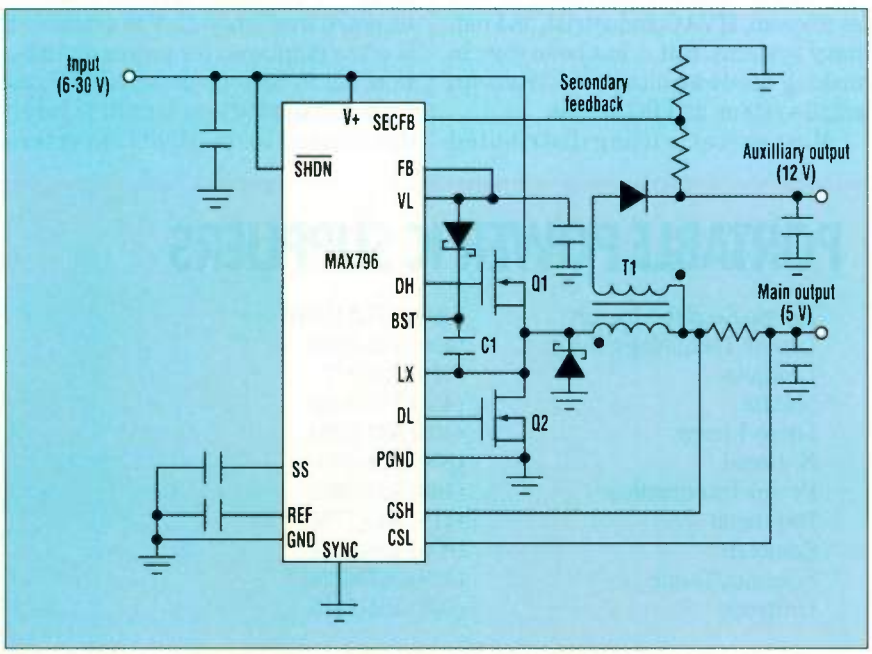
Alternatively, the supply designer can employ one of these controllers to build a single converter that takes the battery stack directly to the low-voltage processor's supply rail. Examples of such IC controllers are Maxim's MAX796/MAX797/MAX798/ MAX799 *(Figs. 1 and 2, again)*.

Regardless of the application, while running its typical, synchronous, current-mode-controller based converter, the MAX797, drives a pair of low cost n-channel power MOSFETs, the PWM switch Q1 and the synchronous rectifier Q2.

Feedback from the output via the CSL (current-sense low) pin connects to an internal resistor network that sets the output of the regulator at 3.3 or 5 V by connecting the FB (feedback) pin to VL or ground respectively. Alternatively, an external resistor-divider network (between the output and ground) with its output to the FB pin sets the output voltage between 2.5 and 6 V (since it is a buck regulator, the input voltage must be at least 6 V).

To maximize efficiency at low currents, the MAX797, as well as the other controllers in this family, automatically switch into a pulse-skipping mode when the current drops below a preset value. A linear regulator between the V+ pin and the VL pin creates the regulated 5 V that runs the chip at start up and can provide the system with 5 V at up to 5 mA from the VL pin. However, when the converter is running, it is powered from the output via the CSL pin.

To minimize conduction losses in the high-side n-channel MOSFET Q1, its gate must be driven at least 5-V positive with respect to its drain. Schottky diode D1 and capacitor C1 form a flying-capacitor boost circuit that creates VL, the supply rail for Q1's on-chip driver circuit, thus providing the required high-side MOS-

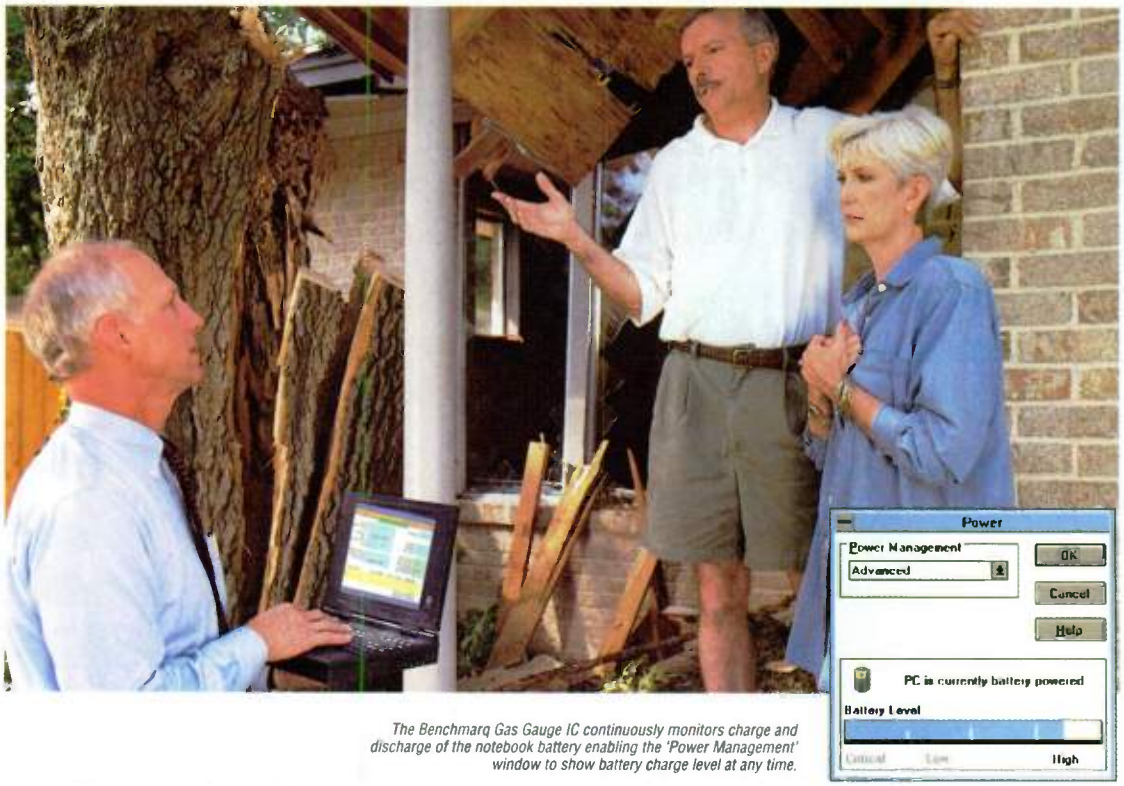


2. In addition to its main 5-V output, the MAX796 Synchronous PWM controller contains a secondary feedback loop that creates and regulates an auxiliary output with the help of

Benchmarq supplies the chip that monitors the battery

that runs the notebook

that calculates the damage...



The Benchmarq Gas Gauge IC continuously monitors charge and discharge of the notebook battery enabling the 'Power Management' window to show battery charge level at any time.

that helps Don settle claims fast.

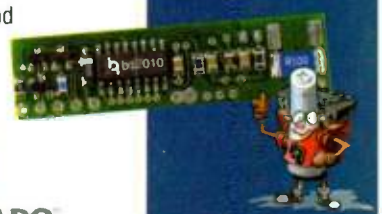
One look at the battery display on Don's notebook computer tells Don he's got the power to prepare all his customers' claims this busy afternoon. Convenient, efficient operation is the reason why Don uses a notebook computer. And that's possible because the makers of Don's computer used Benchmarq gas gauge battery management technology.

Benchmarq gas gauge ICs accurately monitor the battery charge in computers, power tools, cellular phones, and other electronic devices. They require very little board space. And a variety of gas gauge ICs are available to meet your specific needs.

Talk to a Benchmarq product support specialist and find out how you can differentiate your product, improve its performance, and shorten your time to market with Benchmarq battery management solutions. Call 1-800-966-0011 today. And claim more of your market tomorrow.

Gas Gauge IC Selection Guide

Part No.	Description	Battery Technology	Pins/ Package
bq2010	Gas Gauge IC	NiMH and NiCd	16/0.150" SOIC
bq2011/J	Gas Gauge IC for Power Tools	NiMH and NiCd	16/0.150" SOIC
bq2012	Gas Gauge IC	NiMH and NiCd	16/0.150" SOIC
bq2014	Gas Gauge IC with Ext. Charge Control	NiMH, NiCd and Li-Ion	16/0.150" SOIC
bq2050	Power Gauge™ IC	Li-Ion	16/0.150" SOIC
bq2091	SMBus v.95 Gas Gauge IC	NiMH, NiCd and Li-Ion	16/0.150" SOIC



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- Expensive design time
- Reticle/mask costs
- Wafer prototype lot

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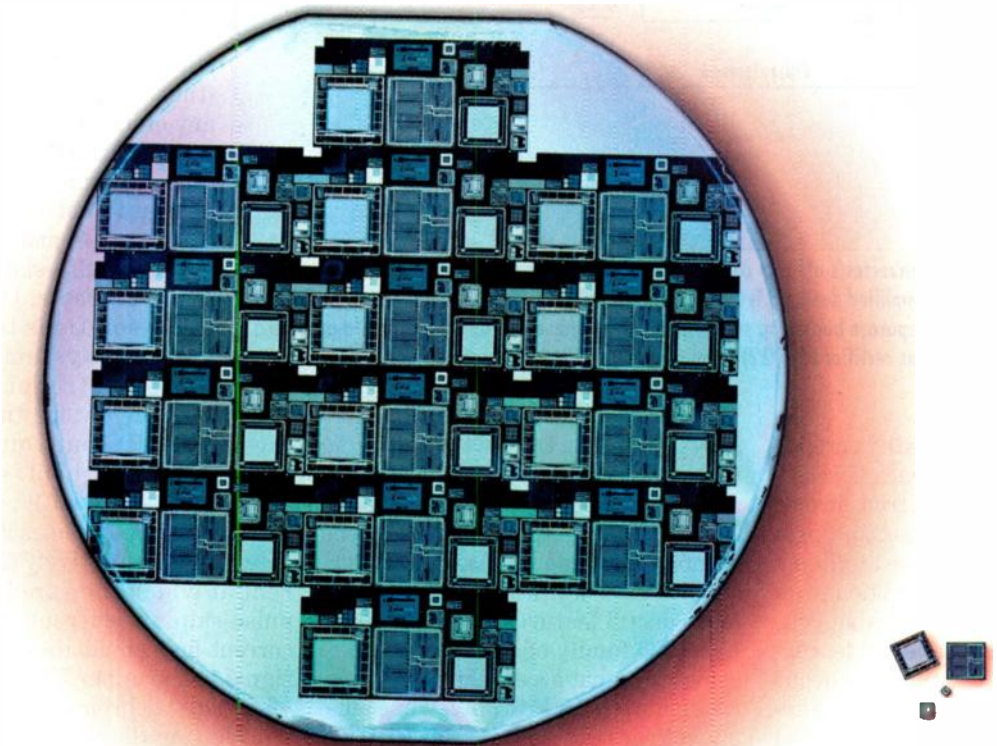

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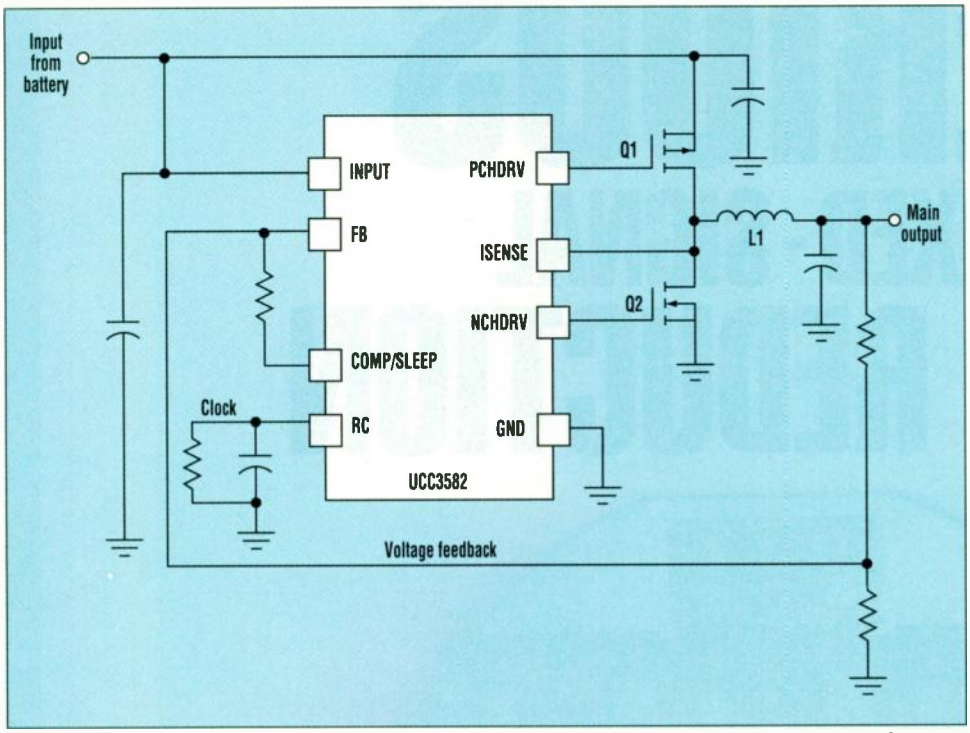
Foresight – MULTI-PROJECT

READER SERVICE 186



4. To minimize the cost of its converter's off-chip components and the pc board space they require, the UCC3582 controller offers a simplified design driving a p-channel MOSFET (Q1) for its switch. The p-channel FET eliminates the need for a separate bootstrap supply (and its off-chip diode and capacitor) to provide a high-side drive. The synchronous rectifier FET (Q2) remains a lower cost n-channel device.

FET drive at the DH pin.

The MAX796 incorporates a proprietary "Secondary Feedback Circuit" that lets it operate with a transformer (T1) instead of an inductor, and provides a regulated positive auxiliary voltage such as +12 V in addition to its main output. The auxiliary output voltage is set with the resistive divider connected between the auxiliary output and ground. The MAX799 sports a similar circuit that provides a regulated negative voltage such as -5 V.

A newer family member, the MAX798, which sports converter operation and specifications like its siblings, including an efficiency of 95% at high loads, is aimed particularly at handling the jump from 30 V to low-voltage CPU power. It differs from the MAX797 primarily in that it provides greater accuracy. That is, line and load regulation are rated at 0.06%/V and 0.4% respectively. It corrects for high-speed transients within 5 cycles of its 300 kHz clock.

Linear Technology Corporation's LTC1435/36/37/38 controller family perform similar functions including dropping into a proprietary pulse-skipping operation (called "Burst Mode") at low currents *(Fig. 3)*. During burst mode, the switch is driven with a short burst of high-frequency pulses. Similar to the previous family of controllers, all members sport a number of unique proprietary analog circuits, each of which provides one or more useful features. Moreover, the LTC1435 family of controllers build converters that accept input voltages ranging from 3.5 V to 36 V, while output voltages can run as low as 1.19 and can range up to 9 V.

Multi Bucks

To handle portable systems that require two or more supplies Maxim has added the MAX1630/MAX1635 family of controllers to their arsenal. Similar to their earlier devices, these are duals that offer similar specifications. However, each can build two buck regulators. Each can have resistor-network-set variable outputs or fixed outputs of 5 or 3.3 V. Several have secondary feedback circuits similar to those of the MAX796 or the MAX799. Most family members also contain a 12-V linear regulator rated at 120 mA. Efficiency typically runs better than 80% over a load current range of 1000-to-1.

LTC's LTC1538/LTC1539 family of dual controllers handle similar applications. However, like their kin, they offer a wide input (3- to 36-V) and output (1.19- to 9-V) voltage range.

Since some notebooks need at least 3 power supplies—for example, 5 V, 3.3 V, and 2.xx V, where xx represents a number of different operating voltages between 2.1 and 2.9 V. To that end, Raytheon has come up with the RC5023. It contains a trio of current-mode synchronous buck-regulator controllers. It is designed to drive logic-level n-channel FETs that need only 4 V of drive (thus, no bootstrap-circuit, or any of its external capacitors, are required). Each pair of FETs operates in a high-efficiency PWM-mode at high currents (4A) and drop into an efficient pulse-skipping mode at low currents. Unlike most other solutions to battery-powered system supplies, these controllers provide "fold-back" current limiting. That is, the supply's output voltage drops when the current-limit is exceeded. Current is sensed with a resistor. A trio of comparators in each controller determines respectively the load current at which the supply starts to pulse-skip, the current at which the current-limit circuit disables the drive signal to the upper FET switch, and when the synchronous (lower) FET is enabled or disabled. However, a Schottky diode is required in parallel with each synchronous FET.

Most of these controllers can build a "second-step" converter that takes the voltage from a 5-V rail to a lower voltage for the CPU core. However, some suppliers make special controllers for this purpose to minimize cost and/or board space, which is also costly. In addition, they are usually built on a lower-voltage, finer-geometry process to cut die size; thus the input voltage range is limited. The drop in die size cuts silicon cost and permits a smaller package. For example, whereas the LTC, Raytheon, and Maxim controllers reside in IC packages ranging from 16-pin SOICs to 36-pin SSOP's (in order to handle all their

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MCU

Solution.

features), Unitrode has squeezed a basic, efficient, synchronous controller into an 8-pin SO package *(Fig. 4)*.

Called the UCC3582, it handles input voltages from 4.5 to 7 V and puts out voltages as low as 1.25 V. Moreover ,it needs few external components which further cuts cost as well as pc-board space. To handle low currents, the controller must be "forced" into its Sleep Mode by bringing the Comp/Sleep pin below 0.5 V. The controller employs a p-channel MOSFET (Q1) for its high side switch, and thus needs no charge-pump, boost, or other special circuits, on or off the chip, to create a high-side drive voltage. The synchronous rectifier MOSFET (Q2) remains as an n-channel device. In addition, the UCC3852 operates in voltage mode rather than in current mode so no lossy, expensive, bulky, current-sense resistor is needed. To implement "lossless" current, limiting the voltage drop across the p-channel switch is sensed during conduction.

While voltage-mode operation usually requires a lead-lag network around the voltage amplifier to compensate for its two-pole LC-filter characteristic, Unitrode has found some converter designers who employ the simple proportional-feedback scheme *(Fig. 4, again)*. However, the UCC3582 controller still allows users to provide their own compensation scheme since the output of the error amplifier is available at pin 6.

The controller runs the converter at 100% duty cycle during a low-battery condition, essentially connecting the battery directly to the output through the p-channel MOSFET. Efficiency typically runs better than 90%. Operating frequency runs to 500 kHz. To convert battery voltage to a 5 or 3.3 V rail, Unitrode recommends a converter based on their UC3870 controller driving a pair of MOSFETs.

All On One Chip

The Unitrode controller cuts space and cost by minimizing the external parts required for the converter and squeezing itself into a tiny package. Power IC designers at Harris Semiconductor took another tack to cut the space required by the converter and the cost of additional components. They eliminated the external MOSFETs in their HIP5020 synchronous buck-regulator IC *(Fig. 5)*. That is, they put a complete switcher, consisting of a current-mode PWM controller plus a pair of n-channel power MOSFETs, on one chip.

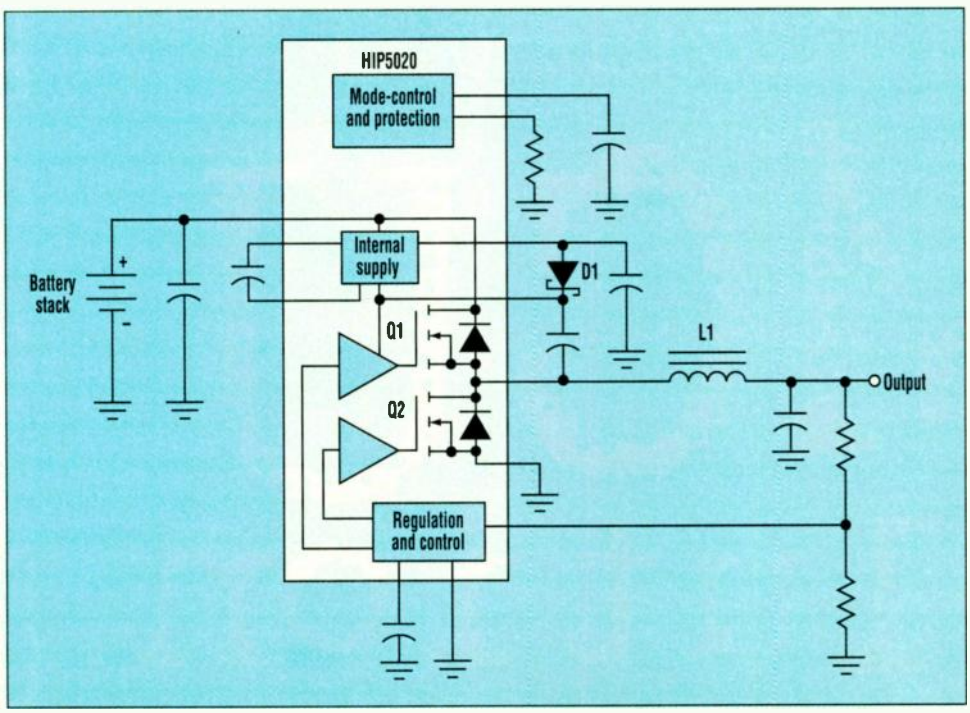
The HIP5020 handles input voltages from 4.5 to 18 V and can deliver 3.5 A at output voltages ranging from 1.26 V to approximately 17 V at a typical light-load efficiency of better than 80%. As a result, it handles battery stacks consisting of from 5 to 12 NiCd or 2 to 3 Li-Ion cells. Alternatively, this complete converter can create a 5-V (or lower) voltage rail from a 12-V rail or similarly step down a 5-V rail. However, it can't step down a 3.3-V rail.

It cuts external parts not only by eliminating the MOSFETs but the chip incorporates a few other neat tricks. For example, it offers the advantages of current mode operation but substitutes an on-chip current-mirror circuit for the external current-sense resistor. The current mirror employs some of the cells in the high-side MOSFET switch (Q1) as sense-FETs. Current-mode operation offers inherent line regulation and fast response to the large load transients expected from the CPU. In addition, when using current-mode control, feedback-loop compensation is easy (single pole) and often not required.

When load currents drop below a user-determined preset value, the converter automatically switches to hysteretic-mode control in which the PWM circuits drive the output with fixed bursts of current at high-frequency. Letting the power system designer determine the current level at which the converter switches between control modes permits trade-offs between efficiency and ripple on the output voltage. To further boost low current efficiency, the user can locate a Schottky diode across the synchronous-rectifier FET (Q2).

The HIP5020 runs at switching rates up to 1 MHz, typically offering peak efficiencies approaching 90% while running at 625 kHz. Since the controller and switches lie on the same silicon die, there is little EMI at high switching frequencies compared with that of converters based on controllers driving MOSFET pairs. That is, antennas formed by component connections are virtually nonexistent.

Harris designers were not alone in realizing that combining a controller and synchro-



5. To minimize the cost of off-chip components, the designers of the HIP5020 put a complete PWM synchronous converter, including a pair of n-channel power FETs (Q1 and Q2), on the same chip.

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nous power-MOSFET switcher on one chip was the way to go for a converter for the CPUs in portable systems. National Semiconductor came up with a fixed PWM switcher power IC the LM2650. It is similar to, yet different from, the Harris part. Rated at 3 A it offers efficiencies of 90% over a load range from 200 mA to 2 A. Input voltages can range from 4.5 to 18 V and output voltage from 1.5 V to 16 V.

Like the Harris converter it employs an automatic hysteretic mode of operation at low currents. National calls it a "sleep" mode. The user determines the "sleep in" and "sleep out" thresholds with resistor networks. In addition, a logic input allows the user to override the automatic "sleep" feature and keep the LM2650 in a PWM mode regardless of the load current.

The National chip differs from the Harris device by operating in voltage rather than in current mode. As a result, it requires relatively complex feedback-loop compensation but no current-sense resistor is required. On-chip lossless current sensing is employed for current limiting. It is slightly smaller than the previous complete converter; a 24-pin SOIC vs a 28-pin SOIC.

Like the Harris chip, the LM2650 can't handle inputs from a 3.3-V rail. However, since a number of processors run off 2.9 V, a switcher is not necessarily the best way to create a 2.9-V CPU rail from a 3.3-V rail. The losses in a linear regulator, such as LTC's LT1575 LDO (low drop out) controller that drives a single power MOSFET, are in a class with those of a switcher in that application.

Another interesting controller IC in an 8-pin package (SOIC), the Raytheon RC5011, contains a 5-V/40 mA linear regulator and a boost rather than a buck PWM controller. Operating with input voltages between 6 and 30 V, it can be used as a standalone switcher and low-current linear regulator, or if used with a separate low-voltage power controller (such as their RC5023), it can provide 12 V for Flash BIOS or PCMCIA cards.

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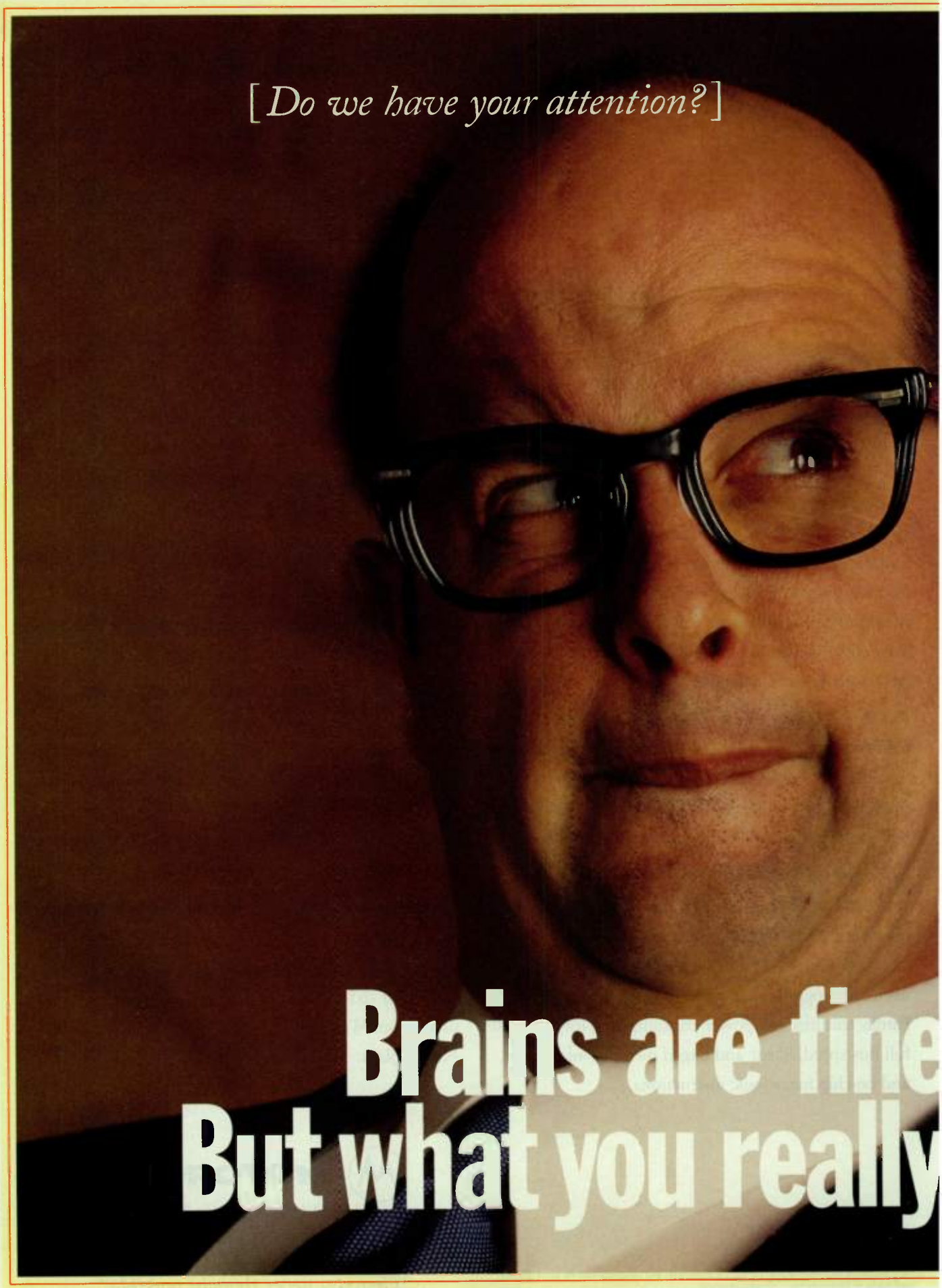
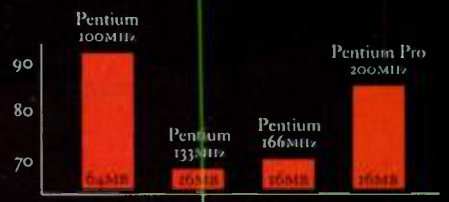


Sometimes you just have to grab people and shake them. For their own good.

And that's exactly what new research findings about PC performance are doing. The thinking used to be like this: Processor = PC. And if you wanted to upgrade performance, the way to do it was to upgrade the processor—at considerable expense.

What you need to know today is that as important as that brain (the processor) is, the memory (DRAM) is every bit as important.

Windows NT 4.0 Benchmark Performance



What about it? The performance gained with a memory upgrade is often greater than what you gain with a CPU upgrade.

For instance, a garden-variety 100 MHz Pentium-based system will actually outperform a 200 MHz Pentium Pro-based system—when you upgrade the 100 MHz system to 64MB memory. And the performance gains of adding memory are just as dramatic in most other cases.

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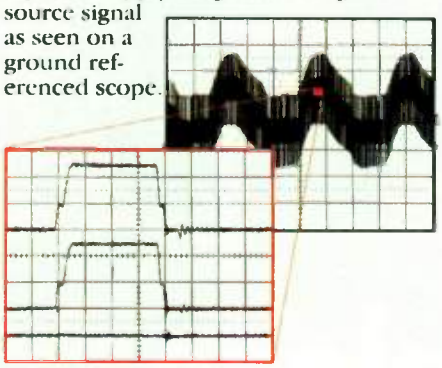

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The 1855 rejects the line voltage and high dv/dt signal, cleanly displaying the upper and lower gate drive signals.

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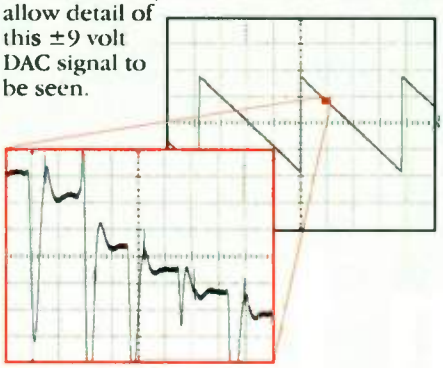
CONVENTIONAL
A scope lacks sufficient position range and lacks the ability to recover from overdrive to allow detail of this ±9 volt DAC signal to be seen.



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PRODUCT FEATURE

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PC Audio Codec With 16-Bit Stereo Full-Duplex Operation Meets AC97 Specifications

The HMP9701 fully meets the audio codec specifications of Intel's, Creative Labs', and others' AC97 specifications, providing the analog codec and digital interface with DACs, ADCs, a mixer, and I/O. By adhering to the specs, the IC supports all available AC97 controllers either on a separate IC or as an embedded function. Rate conversions are to and from 48-ksample/s Sound Blaster compatibility, Dolby AC-3 decoding, and FM or wavetable synthesis.

The part includes 16-bit stereo full-duplex operation with the fixed sample rate; four analog, line-level mono inputs connect from LINE IN, CD, VIDEO and AUX sources. Individual variable-gain amplifiers are provided with 22.5-dB gain range in 1.5-dB steps. Two additional line-level inputs provide sourcing for a speakerphone and a PC "beep." A dedicated pass-through ADC channel for a microphone can have the input switched between two input points with either 0- or 20-dB gain. This allows the subsystem to record the microphone channel and for input filtering either in the AC97 controller or by the host CPU.

The selected input is a pseudo-differential stereo format fed through two 48-ksample/s ADC paths with a stereo line-level output (at a signal-to-noise ratio of better than 90 dB) and a mono output for speakerphone. All three channels have antialiasing filters that need only a single 1-μF capacitor. The mixer in the IC supports playback and record of the range of possible analog and digital audio input sources from standard sources, as well as digital PCM (business, games and multimedia), Analog CD and DVD, and Video (tuner or capture card.)

The HMP9701 is connected to the AC97 audio controller with a bidirectional, five-wire, serial, time-domain-multiplex format interface that handles multiple input and output streams, and control register accesses. Each audio frame is divided into 12 outgoing and twelve incoming data streams. Support is provided for two input slots for PCM record, two output slots for PCM playback, two input slots for status, and two output slots for control.

One of the advantages of the AC97 protocol is the possibility of getting the analog processing as close as possible to the audio input points. The HMP9701 comes in a 9-by-9-mm TQFP with 48 pins and consumes less than 500 mW from a 5-V rail. The part is priced at $6.50 in lots of 10,000, and is available now.

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High-End Electronic Imaging Targeted By Correlated Double Sampler For CCDs

The classical offset error in a CCD's output has been approached a number of different ways, some depending greatly on the desired performance level. Such solutions vary from the homemade circuit to the dedicated IC. One of the popular correction systems has been correlated doubling sampling (CDS), in which a pixel's offset is sampled with no image present and then immediately resampled with the video signal present. The difference represents the valid video signal.

Because the offset continually changes, the closer the timing is between samples, the more accurate the video output is. The result is that CDS eliminates the consequences of residual charge, charge injection, and low-frequency noise, providing a significantly more accurate video output.

The secondary, and as important,

effect of CDS is that the noise floor of the image system is lowered, increasing the dynamic range and allowing for the capture of lower-level intensities of light. CDS circuits are notoriously expensive to implement and present challenges when making the dynamic trade-offs in slew rate, bandwidth, settling time, and noise/distortion. As a result, the method has been used only on the highest quality, most demanding systems.

The CDS-1402 is a complete and flexible CDS function in a single IC, which Datel believes to be a first. While maximizing dynamic range and signal-to-noise ratio from CCDs using CDS with two sample-and-hold amplifiers in a sample-subtract-sample approach, the part demonstrated high accuracy, a wide 24-MHz bandwidth, and up to 5-Mpixel/s throughput for 14 bits. The acquisition time is 50 ns to ±0.5 mV, while noise is at 200 μV rms and power consumption is about 350 mW with ±5 V supplies. The part is packaged in a 24-pin DDIP with gold-plated Kovar alloy leads; an SMT version also is available. For commercial temperature devices, pricing is $98 in 100-unit lots. Samples are from stock, production orders require six weeks.

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27C2048	5V	2Mb	128K x 16	70 ns	PLCC/PDIP/TSOP
27C4096	5V	4Mb	256K x 16	85 ns	PLCC/PDIP/TSOP
27BV4096	2.7V	4Mb	256K x 16	150 ns	PLCC/TSOP

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IEEE Ultrasonics Symposium, Oct. 7-10. Marriott Hotel, Toronto, Canada. Contact Stuart Foster, Dept. of Medical Biophysics, Room S-658, Sunnybrook Health Science Ctr., 2075 Bayview Ave., Toronto, Ontario, M4N 3M5, Canada; e-mail: stuart@owl.sunnybrook.utoronto.ca.

Sixth IEEE International Conference on Universal Personal Communications, Oct. 12-16. Hotel del Coronado, San Diego, CA. Contact Gail Weisman, IEEE Communications Society, 345 E. 47th St., New York, NY 10017; (212) 705-7018; fax (212) 705-7865; e-mail: g.weisman@ieee.org.

Sixth IEEE International Conference on Universal Personal Communications (ICUPC '97), Oct. 13-15. Contact Tony Acampora, MC 0409, Bldg EBU1, UCSD, 9500 Gilman Dr., La Jolla, CA 92093-0409; (619) 534-5438; (fax) (619) 534-2486; e-mail: acampora@ece.ucsd.edu.

Conference on Domain-Specific Languages (DSL), Oct. 15-17. Red Lion Resort, Santa Barbara, California. Contact USENIX Conference Office, 22672 Lambert Street, Suite 613, Lake Forest, California 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

ICSPAT/DSP World 1997, Oct. 15-17. San Diego Convention Center, San Diego, California. Contact Denise Chan, Miller Freeman Inc. (415) 278-5231; e-mail: dsp@exporeg.com.

IEEE Holm Conference on Electrical Contacts, Oct. 18-22. Wyndham Franklyn Plaza, Philadelphia, Pennsylvania. Contact Wendy Rochelle, IEEE Conference Services, 445 Hoes Ln., Post Office Box 1331, Piscataway, New Jersey 08855-1331; (908) 562-3870; fax (908) 981-1769; e-mail: w.rochelle@ieee.org.

IEEE Telecommunications Energy Conference (INTELEC '97), Oct. 19-23. World Congress Centre, Melbourne, Australia. Contact Robert N.K. Thuan, Network Products-Telstra Corp. Level 14, 242 Exhibition St., Melbourne, Victoria 3000, Australia; (61) 3 634 6216; fax (61) 3 632 3607

Sensors Expo, Oct. 21-23. Cobo Convention Center; Detroit, MI. Contact Expocon Management Associates Inc., (203) 256-4700; e-mail: sensors@expocon.com; Internet: http://www.expocon.com.

Fourth IEEE International Conference on Image Processing (ICIP '97), Oct. 26-30. Fess Parker's Red Lion Resort, Santa Barbara, CA. Contact Sanjit K. Mitrea, Electrical & Computer Engineering, University of California, Santa Barbara, CA 93106-9560; (805) 893-3957; fax (805) 893-893-3262; e-mail: mitra@ece.ucsb.edu.

11th Systems Administration Conference (LISA '97), Oct. 26-31. Town & Country Hotel, San Diego, CA. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

19th Annual International Conference of the IEEE Engineering in Medicine & Biology Society, Oct. 29-Nov. 2. Sally Chapman, Secretariat, National Res. Council of Canada, Bldg. M-55 Rm. 393, Ottawa, KIA OR8, Canada; (613) 993-4005; fax (613) 954-2216.

19th International Conference of the IEEE Engineering in Medicine & Biology Society, October 30-November 2. Chicago Marriott Downtown, Chicago, Illinois. Contact Meeting Management, 2603 Main Street, Suite 690, Irvine, California 92714; (714) 752-8205; fax (714) 752-7444; e-mail: embs97@ieee.org; Internet: http://www.eecs.uic.edu/-embs97.

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IEEE International Test Conference (ITC), Nov. 1-5. Sheraton Washington Hotel, Washington, DC. Contact ITC, 655 15th St., N.W., Suite 300, Washington, DC. 20005; (202) 639-4164; fax (202) 347-6109.

IEEE Global Telecommunications Conference (GLOBECOM '97), November 4-8. Phoenix Civic Center, Phoenix, AZ. Contact Paul Narula, AG Communication Systems, Information Line, (602) 581-4297; (602) 582-7697.

IEEE Global Telecommunications Conference (GLOBECOM '97), Nov. 3-7. Phoenix, AZ. Contact Nigel Reynolds, 15436 N. First Ave., Phoenix, AZ 85023; (602) 942-5583; fax (602) 942-4542; e-mail: nigelaz@aol.com.

WESCON '97, Nov. 4-6. San Jose Convention Center and Santa Clara Convention Center, San Jose and Santa Clara, CA. Contact Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045-3194; (800) 877-2668; fax (310) 641-5117; e-mail: wescon@ieee.org.

IEEE Intelligent Transportation Systems Conference (ITS '97), Nov. 9-12. Boston Park Plaza Hotel, Boston, MA. Contact Richard Sparks, 8 Richard Rd., Bedford, MA 01730; (617) 862-3000; fax (617) 863-0586; e-mail: r.sparks@ieee.org.

23rd Annual Conference of IEEE Industrial Electronics (IECON '97), Nov. 9-14. Hyatt Regency Hotel, New Orleans, LA. Contact Michael Greene, 200 Broun Hall, Electrical Engineering, Auburn University, Auburn, AL 36849-5201; (334) 844-1828; e-mail: greene@eng.auburn.edu.

Asian Test Symposium, Nov. 17-19. Akita, Japan. Contact Y. Takamatsu, (81) 89 927-9955; e-mail: takamatsu@cs.ehime-u.ac.jp.

DECEMBER

36th IEEE Conference on Decision & Control, December 8-12. Hyatt Regency, San Diego, California. Contact Ted E. Djaferis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, Massachusetts 01003; (413) 545-3561; fax (413) 545-1993; e-mail: djaferis@ecs.umass.edu.

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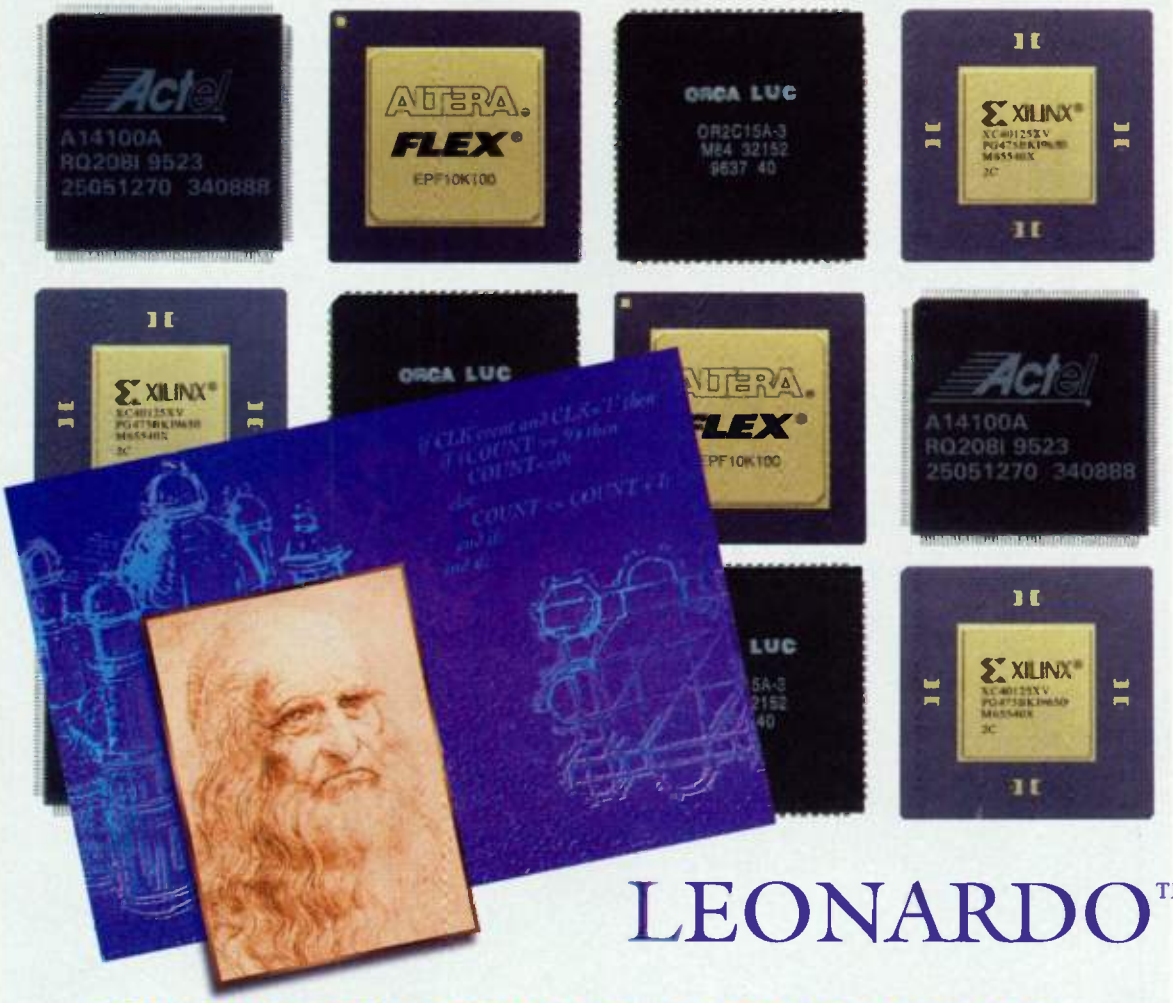

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Gigabit Ethernet: Technology, Systems, And Network Applications

Is Gigabit Ethernet Ready For Prime Time? Is It The Great "ATM Killer"? Is It Really Ethernet? For The Answers To These And Other Questions, Tune Into This Month's Exciting Installment Of "LAN Wars..."

PATRICK VAN EIJK, Vitesse Semiconductor Corp., 741 CallePlano, Camarillo, CA 93012; (408) 969-0432.

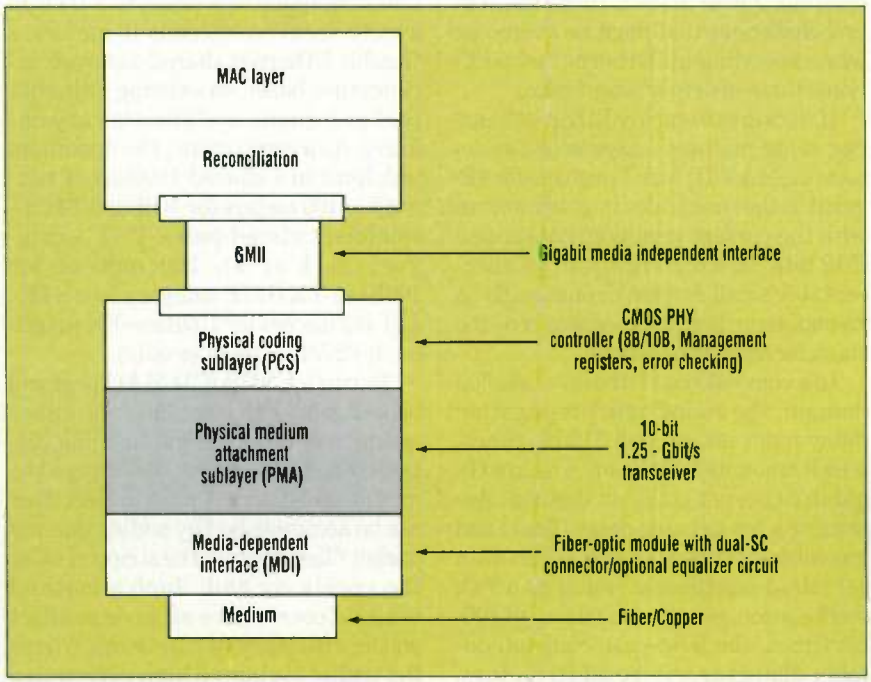
With today's ever increasing LAN network laboring under loads load from faster CPUs, laser printers, scanners, video servers, high-speed graphical displays, and other high-resolution image based applications, it is not surprising that the IEEE 802.3 High-Speed Study Group is looking for a standard beyond Fast Ethernet (100 Mbits/s). In July 1996, the 802.3z Gigabit Ethernet Task Force was created, in charge of completing the 802.3z Gigabit Ethernet standard by the end of 1997.

To minimize risk and improve time-to-market, the standards committee is building upon proven Fibre Channel (FC) physical (PHY) layer technology, running at 1.25 Gbits/s (this rate includes a 20% data coding overhead). By adapting Ethernet's existing media-access-control (MAC) protocol, management information base (MIB), frame format and link-level-control (LLC) interface, maximum compatibility with the installed base of over 60 million LAN nodes is maintained.

While it took three years to get approval on the Fast Ethernet standard, it looks like the Gigabit Ethernet standard will progress much faster taking about half that time to be completed. With standard approval expected before the end of this year, all the networking giants and a dozen networking startups are working frantically on several types of Gigabit Ethernet systems for a 1997 introduction.

Fibre Channel, the point-to-point, serial protocol specified by the ANSI X3T11 Committee, is a layered protocol, loosely based on the OSI network system reference model. The lowest or so-called PHY layer, dictates several different serial transmission rates of which the most popular is the 1.0625-Gbit/s or "full-speed" rate. The Fibre Channel industry specifies a 10- or 20-bit TTL parallel interface which is serialized to a 1.0625-Gbit/s data stream. At the receiving end, serial 1.0625-Gbit/s data is deserialized back to 10 or 20 bits (*see "A closer look at the hardware," p.88)*. The highest-integration PHY layer device is a 10-bit 1.0625-Gbit/s transceiver device developed for dual-channel disk drives.

Disk drives are acting as the gating items in the developing Fibre Channel market, providing the volume re-

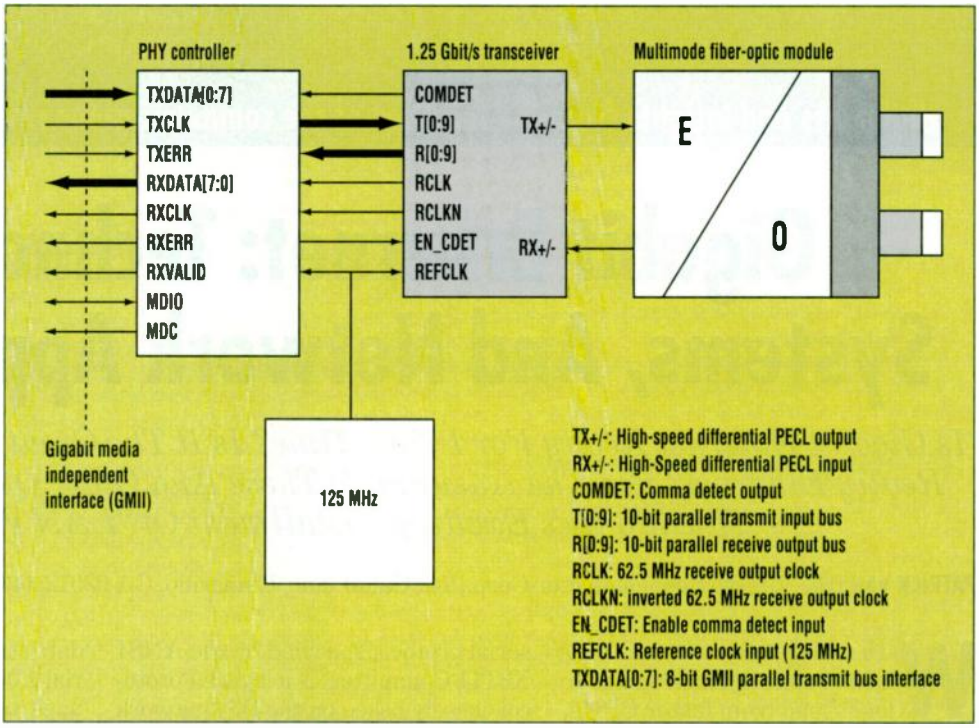


1. In this full-duplex Gigabit Ethernet link implementation, the GMII interface provides the connection between the MAC layer and the physical coding sub-layer (PCS), which provides 8B/10B coding, management registers and error checking. The 10-bit 1.25-Gbit/s transceiver is located below the PCS layer in the PMA sub-layer.

quired to make this high-performance technology affordable for other applications. The ramp-up observed in transceiver volumes during the fourth quarter of 1996 should push prices well below $10 per channel.

Reliability and high-performance already have been demonstrated successfully. The transceiver's functionality, performance and cost are what attracted the Standards Committee to consider Fibre Channel as their method of implementing their physical layer. Multiple vendors have committed to providing functionally equivalent transceivers at 1.25 Gbits/s for Gigabit Ethernet.

As we will see later on in this article, the prevalent links between future switched-architecture networks will be gigabit links in full-duplex operation. With data flowing simultaneously in both directions across the link, a 100% improvement in throughput (over a simplex link) can be realized (assuming the traffic is evenly balanced between send and receive). Nevertheless, there are several challenges that must be overcome when speeding up Ethernet an additional three orders of magnitude.



2. In this example of a full-duplex fiber-optic Gigabit Ethernet adapter card, the GMII interface provides the connection between the MAC layer and the PCS. The transceiver interfaces to a fiber-optic module, which converts the high-speed electrical signal into an optical signal, and vice versa.

If we were to employ Ethernet's carrier-sense multiple-access/collision-detect (CSMA/CD) MAC protocol for Gigabit Ethernet links in conjunction with the current minimum packet size (512 bits), it would result in an unacceptably small domain diameter. Even its maximum link distance would be too short for most applications.

In a conventional Ethernet collision domain, the round-trip propagation delay must not exceed 512 bit times, which amounts to only 409.6 ns in a Gigabit Ethernet collision domain. Assuming a 5.0-ns cable delay (fiber) and a combined repeater and DTE (data terminal equipment: such as a PC, workstation, server, etc.) delay of 100-bit times, the best-case collision domain diameter will be 32.96 meters. This means that two DTEs talking to each other over a shared Gigabit link through a repeater can only have a combined cable length of 32.96 meters, or an individual cable length of just over 16 meters.

Since the average length of most horizontal wiring (from a repeater in a telecommunications closet to a DTE in a work area) far exceeds 16 meters, a Gigabit Ethernet shared-network architecture based on existing Ethernet packet formats and sizes is very unlikely. As a comparison, the maximum link limit in a shared 100Base-T network is 100 meters for 100Base-T4 (unshielded twisted-pair—UTP—category 3, 4 or 5), 100 meters for 100Base-TX (UTP category 5 or STP), and 412 meters for 100Base-FX (multimode 62.5/125-µm fiber only).

To run a CSMA/CD MAC protocol on a Gigabit Ethernet link, one either needs to keep the individual link distance below 16 meters, or change the minimum Ethernet packet size. This can be accomplished by adding dummy packet fillers that will be stripped off at the receiving end. Such a method would of course have an adverse effect on the efficiency of a network where the traffic contains a high percentage of minimum-size packets. The IEEE 802.3z is currently evaluating several proposals on how to increase the minimum link distance.

On a Gigabit Ethernet link serial data will be transmitted at 1.25 Gbits/s that can no longer propagate over UTP wiring. Instead, 150-Ω coax or fiber needs to be used. The latter is more attractive from an EMI and cable-length point of view. Since most Gigabit Ethernet links will initially be installed from switch-to-switch or from switch-to-server, it seems necessary to retain the 100-meter link distance requirement.

Transmission media

The standards committee has already agreed upon and demonstrated a 500-meter maximum link distance at 1.25 Gbits/s over a 50-mm core multimode fiber, and a 200-meter maximum link distance for a multi-mode fiber with a 62.5-mm core. On copper, the existing Fibre Channel PHY transceivers can only drive 30 meters (150-Ω coax) which does not satisfy the existing link distance requirement for Fast Ethernet. However, with 2X PECL output drivers and the use of an equalizer, distances of 100 meters or greater are easily achievable.

At this point, it remains unclear if the 8B/10B encoding/decoding scheme will be used for both a fiber and a cop-

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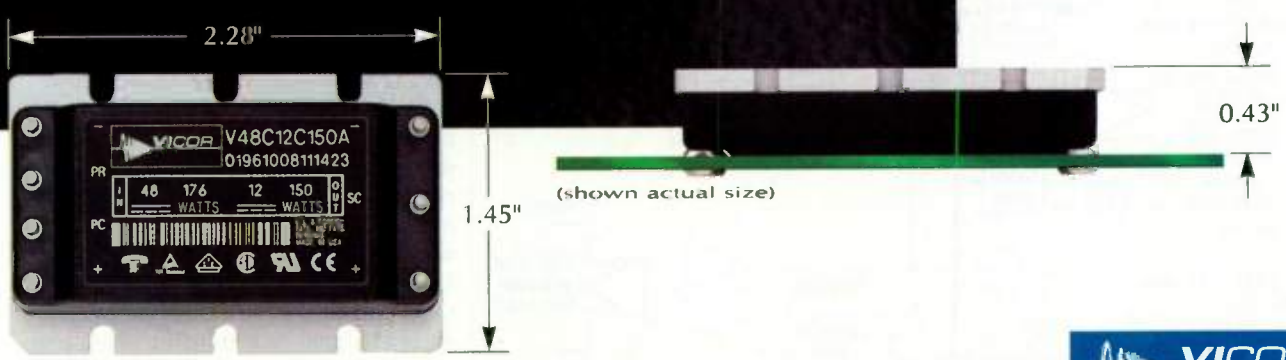

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per medium (8B/10B encoding/decoding is necessary to provide a high enough transition density to allow for the correct operation of the clock recovery circuit at the receiving end). It is possible that in order to reduce the maximum frequency on a copper link, a different encoding scheme plus nonbinary signal levels could be used. This would result in the requirement for a separate transceiver that would significantly delay the development of copper Gigabit Ethernet links.

Gigabit Adapter Cards

It is important to note that the only difference between the Fibre Channel PHY transceiver, operating at 1.0625 Gbits/s, and a potential Gigabit Ethernet transceiver will be in their speed. Assuming the Standards Committee decides to implement the Gigabit Ethernet physical layer for using a Fibre Channel PHY, a CMOS PHY controller is required to implement the functions needed to support a Gigabit media-independent interface (GMII). Such a controller would include 8B/10B data encoding and decoding (or a different encoding/decoding scheme), a set of management registers, and error checking logic *(Fig. 1)*.

The main difference between a Fast Ethernet and a Gigabit Ethernet MII will be the number of parallel bits, which will be eight in the case of 1000Base-T. Since 10-bit, 1.25-Gbit/s transceivers are currently available from Vitesse Semiconductor (VSC7135) and soon from other vendors as well, one can implement full-duplex Gigabit Ethernet adapter cards today *(Fig. 2)*.

Gigabit Ethernet Systems

In 1997, three different types of Gigabit Ethernet systems will be introduced: A Fast Ethernet switch with one or two Gigabit Ethernet uplinks, a Gigabit Ethernet buffered distributor (hub), and a full-blown Gigabit Ethernet switch. The Fast Ethernet switch will have one or two Gigabit Ethernet ports that can be used for a backbone switch or a high-speed server connection. The buffered distributor will consist of an 8-to-12-port system, each port being a full-duplex Gigabit Ethernet connection.

If the traffic load is divided equally across all N ports, the available bandwidth would be 1.0 Gbits/s divided by the number of ports. The main difference with a Fast Ethernet repeater is that each port is full-duplex; therefore, there are no collisions on the actual cable. Essentially, the CSMA/CD has been moved "inside the box." High-speed buffers and a simple port arbitration algorithm assure a fair distribution of available bandwidth. This system would be ideal as a backbone for a Fast Ethernet network. Finally, the Gigabit Ethernet switch will be a 8-to-32 full-duplex port systems for maximum bandwidth needs in backbone network connections.

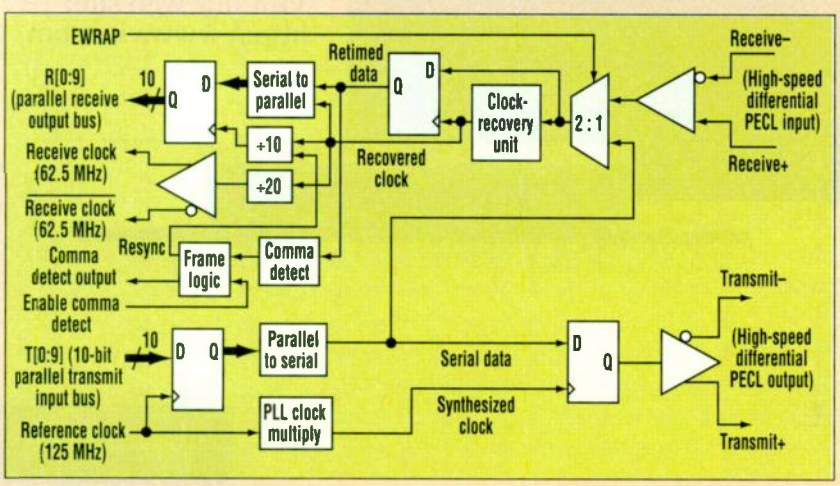
Network Applications

As the current 10Base-T shared hub-and-spoke networks migrate to switched 10 and 100Base-T networks, to avoid the performance degradation experienced by users of shared media LANs, it becomes evident that gigabit links from switch-to-switch and server-to-switch will be able to solve tomorrow's bottlenecks in networks.

Many networks have already migrated to a collapsed backbone architecture, where the 100-Mbit/s shared FDDI backbone has been replaced by a switch with both 10-Mbit/s and 100-Mbit/s ports to allow for a seamless upward migration *(Fig. 3)*. Since switching will be deployed from the top down, starting at server and router connections, it will push its way

A Closer Look At The Hardware

The figure illustrates a typical gigabit transceiver architecture. On the transmit side, it accepts 10-bit 8B/10B encoded data at 125 Mbits/s, latches it in on the rising edge of the reference clock and serializes it onto the transmit+ and transmit- PECL differential outputs at a baud rate 10 times the reference-clock frequency. The 8B/10B encoding is necessary to guarantee a minimum transition density in the serial signal in order to perform a correct clock and data recovery at the transceiver differential input. The transceiver samples serial receive data on the receive+ and receive- PECL differential inputs, recovers clock and data, deserializes it onto the 10-bit receive data bus, outputs two recovered clocks at 1/20th the incoming baud rate and detects Fibre Channel "comma" characters (0011111XXX), used for word alignment. This "comma" character is a unique character not part of the 8B/10B code set. Upon detection of three sequential "comma" characters, word alignment will occur if comma detection is enabled (held High). The chip contains on-chip PLL circuitry for synthesis of the baud-rate transmit clock, and extraction of the clock from the received serial stream.



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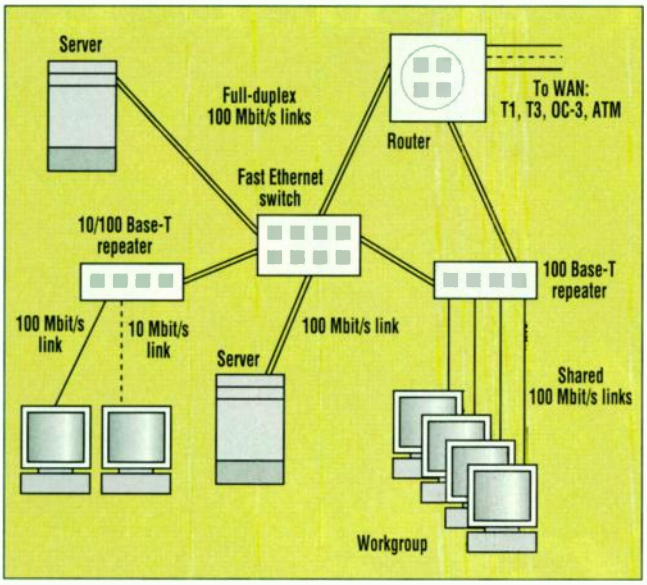
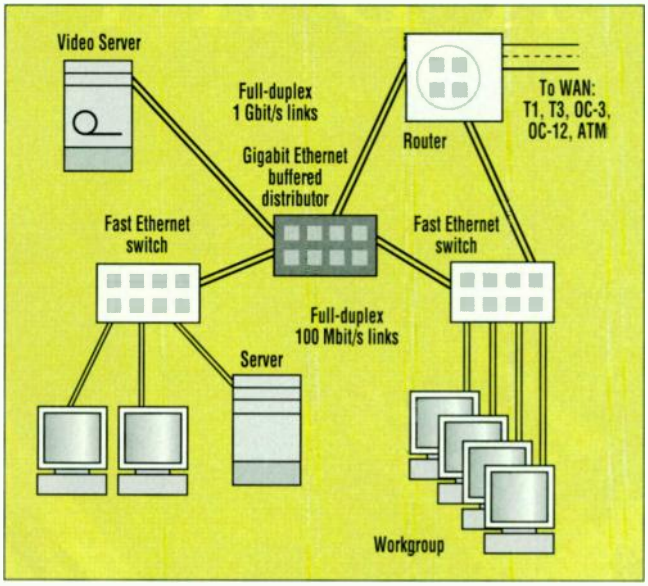


3. A collapsed backbone network with 100-Mbit/s backbone links employs a Fast Ethernet backbone switch to connect between repeaters (hubs), servers, and a WAN interface (router). As most users outgrow their shared links and demand more bandwidth, the repeaters will have to be replaced with Fast Ethernet 10- Mbit/s switches. This will require the backbone connections to be upgraded to 1 Gbits/s, see Figure 4.



4. This switched Fast Ethernet network uses Gigabit Ethernet backbone full-duplex links to bridge the 100-Mbit/s Fast Ethernet switches with one or two gigabit uplinks. A Gigabit Ethernet buffered distributor provides a shared 1.0-Gbit/s connection between Fast Ethernet switches, high-speed servers, and routers. High-speed imaging applications can be accommodated with this network.

down toward the end user's desktop.

As the price of switched networks comes down, more and more 10 and 100Base-T repeaters will be replaced with Fast Ethernet switches interconnected by gigabit links *(Fig. 4)*. The full-duplex Gigabit Ethernet buffered distributor will form the gigabit backbone for a switched Fast Ethernet LAN. This fully-employed switched network architecture, with a multi-gigabit aggregate bandwidth, will be able to support the most-demanding full-motion multimedia, videoconferencing, medical imaging, simulation and modeling, and other high-speed image applications. The full-blown Gigabit Ethernet switches will be deployed to connect these switched fast Ethernet LANs on the enterprise or campus-wide level.

ATM Comparison

Fast Ethernet (100 Mbits/s) has narrowed the gap between the future promises of ATM and today's available performance. Because of this, widespread deployment of 155- or 622-Mbit/s ATM to the desktop has been pushed out to the year 2000 or beyond.

ATM at the LAN level is an attractive feature because of its perceived capability to provide wide-area ATM connectivity once fully ATM-based WANs become deployed. For now, user have to chose between ATM, with its perceived future WAN capability, and switched architecture Fast Ethernet networks with Fast Ethernet and Gigabit Ethernet switch-to-switch and switch-to-server links. The latter come with greater availability, a range of options and configurations, and software support.

There is no doubt in anyone's mind that ATM will be the connectivity solution of choice for WANs. Eventually, it will deliver the lowest-cost long-distance transmission service. Just like Ethernet, ATM supports UTP category 3, 4, and 5, 150-Ω shielded twisted-pair (STP) wiring, and single and multi-mode fiber. A switched architecture combined with high-speed links will provide almost unlimited scalability and flexibility.

Although ATM's small cell size provides very low delay, which is advantageous for WANs as well as LANs, ATM standards are still not yet complete. Especially lacking are mechanisms for monitoring and policing traffic to prevent internal switch-buffer overflow in public networks.

Much like ATM, Ethernet also offers switching. A Fast Ethernet switched architecture network with Gbit/s switch-to-switch and switch-to-server links will offer a solid foundation for the transport of multimedia. Such a network, combined with protocols such as real-time transfer protocol (RTP), real-time transfer control protocol (RTCP), or resource reservation protocol (RSVP) to guarantee on-time delivery of multimedia traffic and to smoothen the inherently jerky Ethernet traffic patterns, will be a serious ATM competitor in the LAN arena.

Patrick Van Eijk is a senior field applications engineer at Vitesse Semiconductor, Camarillo, Calif. As one of the principal architects of several SONET and other networking ICs, he focuses on telecom and networking systems applications. . Mr. Van Eijk holds a combined BS/MSEE degree from the University of Twente in The Netherlands, where he specialized in integrated optics and semiconductor lasers. He also holds a MSEE degree in semiconductor device physics from the University of California at Los Angeles (UCLA).

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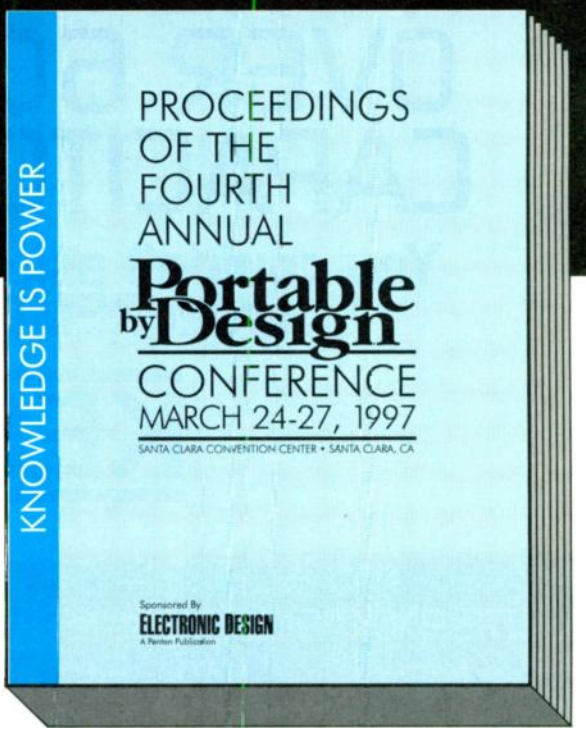

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Wireless ATM Promises To Deliver Internet Access And Live Video

Researchers Are Developing Prototype Wireless ATM Networks That Are Blazing A Path For Commercial Technologies To Follow.

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Look into your crystal ball and envision mobile-knowledge workers, or even the average consumer, carrying handheld wireless devices that consistently connect with the Internet. The devices don't subject the users to busy signals, and they can even handle multimedia data streams, including live video.

Wireless-ATM technology could enable that vision in just a few years. In fact, wireless ATM promises to deliver voice, data, and video over a single wireless channel, first within LANs, later across business or school campuses, and ultimately, coast-to-coast via cellular-like networks. Obstacles to the vision range from the development of reliable broadband radios to appropriate protocols, but already, laboratory models and test beds indicate that they can be overcome.

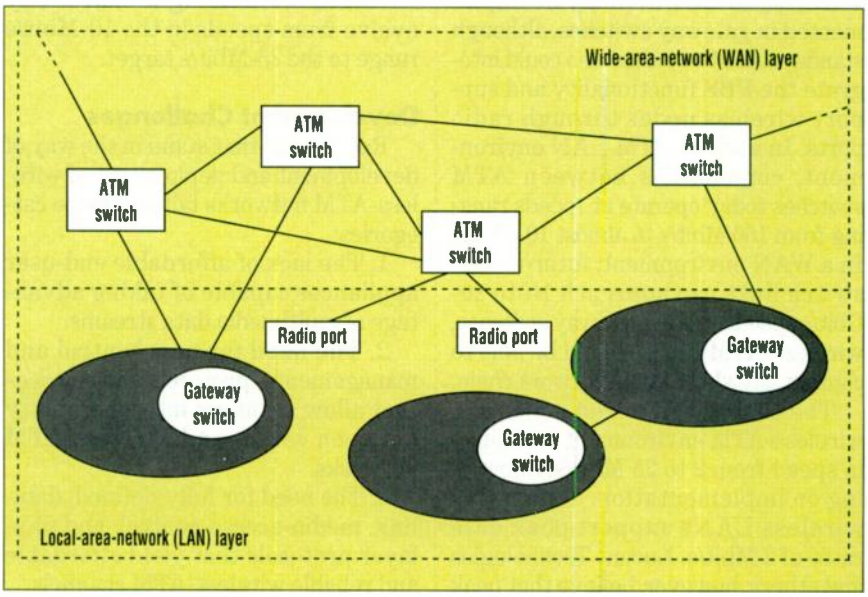
A number of government organizations and leading communications and computing companies are working through the early stages of wireless-ATM development. The efforts seek to prove the feasibility of the technology and to develop protocols and technologies. In November 1995, for example, Lucent Technologies and Sun Microsystems began collaboration on a three-year effort—the Mobile-Information-Infrastructure (MII) project *(Fig. 1)* The MII is partially funded by the U.S. government's Advanced Technology Program, and is administered by the National Institute of Standards and Technology (NIST). Early work in the project was based on a network model called the broadband-adaptive-homing-ATM architecture (BAHAMA).

Logically, wireless ATM is exactly analogous to wired ATM. Today, more companies are using ATM as a key part of enterprise networks. The technology can serve as high-performance links to desktops in advanced LANs, as high-speed backbones in LANs, and even as WAN interconnects. Moreover, public utility companies, such as telephone companies, are integrating ATM into their networks, and will ultimately transition to all-ATM networks that carry voice, video, and data. Down the road, wireless ATM will fit in these same applications both in place of, and as an extension to wired-ATM networks.

ATM's connection-oriented, switched architecture gives it attributes that enable the technology to serve in wide-ranging roles. For example, ATM employs fixed-length data cells that simplify bandwidth allocation. This cell-switching technology, combined with a layer of quality of service (QoS) cell-routing priorities can support data streams ranging from MPEG video that requires isochronous delivery, to e-mail that can be routed on a bandwidth-available basis.

Other Wireless Technologies

Wireless ATM will differ from other wireless data-communications technologies such as IEEE 802.11 wireless LANs. The wireless LANs use Ethernet-like protocols, and currently can't allocate bandwidth using QoS priorities. Still, wireless ATM and LAN technologies can be used together. The MII program, for example, defined a network model with support for wireless access points called BAHAMA portable base stations (PBSs) that support end-to-end ATM links to each

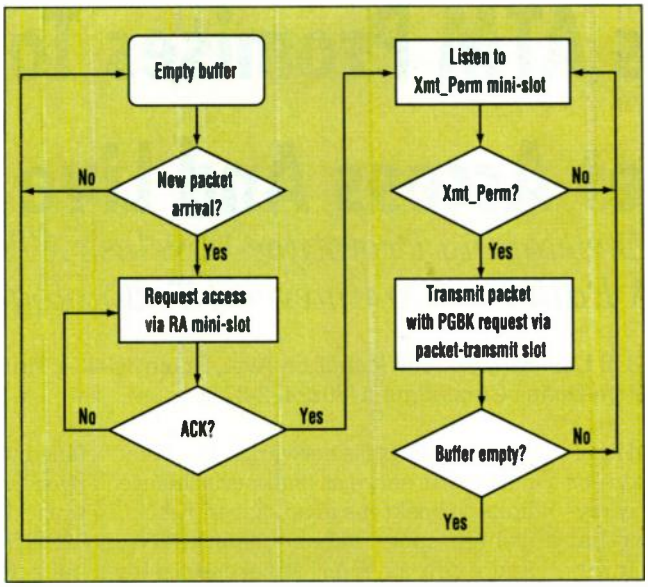


1. The mobile-information infrastructure (MII) employs radio ports to bridge communication between the fixed infrastructure and its wireless terminal. Traffic is directed through an ATM switch, to its destination via a gateway switch. Protocol adaptation allows both ATM and TCP/IP traffic to use the network in a transparent manner.

wireless node.

The model also supports a second class of PBSs that use IEEE 802.11 wireless links to connect with standard wireless-LAN nodes. The so-called Wireless Virtual LAN (WVLAN) PBSs must provide proxy-agent facilities for each non-ATM node. End systems that support native ATM are called Type-1 hosts and end systems that use 802.11 wireless channels are called Type-2 hosts.

Remember that ATM also can carry standard Ethernet traffic such as TCP/IP packets. The ATM Forum developed the ATM-adaptation layer (AAL) as a means of encapsulating TCP/IP traffic across an ATM backbone. Wireless ATM will inherently include AAL support. In the case of Type-2 hosts, the WVLAN PBS will translate AAL traffic back to TCP/IP traffic while Type-1 hosts will directly integrate the AAL facilities.



2. The DQRUMA protocol provides a wireless media-access-control (MAC) method that doles out bandwidth in a fair and efficient manner. In this flow chart, a DQRUMA-equipped transceiver might transmit the contents of its buffer by first issuing a permission (Xmit_Perm) request in a specially designated time-slot, and wait for explicit permission from the network. Once a node begins transmitting, it can piggyback additional bandwidth requests in the data slots, further optimizing delay-throughput performance.

The MII model

An ideal wireless-ATM network will be capable of using off-the-shelf ATM switches from a number of vendors in arbitrary topologies *(Fig. 1, again)*. Wireless PBSs will likely be implemented in gateway switches, although standard ATM switches also could integrate the PBS functionality and support wireless nodes through radio ports. In a wired-ATM LAN environment, connections between ATM switches today operate at speeds ranging from 150 Mbit/s to almost 10 Gbit/s. In a WAN environment, future inter-switch links can approach 10-to 20-Gbit/s speeds. Using gateway switches, wireless-ATM PBSs should be able to connect anywhere in the network chain.

The connection to end nodes in a wireless-ATM environment will range in speed from 2 to 25 Mbit/s, depending on implementation. Today, RF-wireless LANs support peak data rates of 2 Mbit/s. Lucent Technologies and others, however, believe that peak rates can move into the 10-Mbit/s range in the near future.

In the long term, Type-1 hosts will dominate wireless-ATM networks so that applications such as MPEG-video delivery get QoS priorities from end to end. Ultimately, the BAHAMA model targets 25-Mbit/s speeds for RF links between the PBS and Type-1 hosts. MPEG video can be successfully transmitted at much lower rates, and wireless-ATM designs will likely evolve from speeds in the 10-Mbit/s range to the 25-Mbit/s target.

Development Challenges

Roadblocks that stand in the way of development and deployment of wireless-ATM networks fall into three categories:

1. The lack of affordable end-user appliances capable of taking advantage of multimedia data streams.

2. The need for new control and management—protocols and services that allow seamless interoperability between wired- and wireless-ATM networks.

3. The need for fully-defined, data-link, media-access-control, and phy-layer protocols that yield affordable and reliable wireless-ATM channels.

Arguably, the first challenge will be solved over time as portable-device vendors try to package more PDAs and handheld computers. Today, such devices can only handle relatively low-speed data for applications such as e-mail and paging. Limitations include cost, CPU horsepower, display quality, and power consumption, as well as the wireless communication link. To ensure that portable devices will be able to leverage wireless-ATM capabilities, Sun Microsystems is developing a next-generation, multimedia handheld device for the MII project.

The control and management tasks that the MII must perform include connection control, mobility management, call control, service control, and aspects of network management. ATM is inherently connection oriented, so connection-control algorithms must be developed to set up and release connections.

Mobility-management functions must be available to permit users to roam between mobile-access points, while maintaining the same logical connection to the network. The network must first keep track of mobile nodes so that packets can be delivered, then employ hand-off procedures to reroute ATM connections as users move between PBSs.

Call and service control functions include implicitly checking for service triggers before setting up a connection, and automatically invoking services such as calling-card validations and billing. Network-management functions comprise performance monitoring, configuration management, fault management, accounting, and security management. Ultimately, a model for control and management service must consider the different needs of LAN and WAN environments, and the different needs of Type-1 and Type-2 hosts.

The OSI Layers

Solving the wireless-communications problems in the lower three layers of the OSI reference model provides perhaps the biggest challenge to deployment of wireless-ATM technology. At the physical (PHY) layer, wireless ATM will require burst ra-

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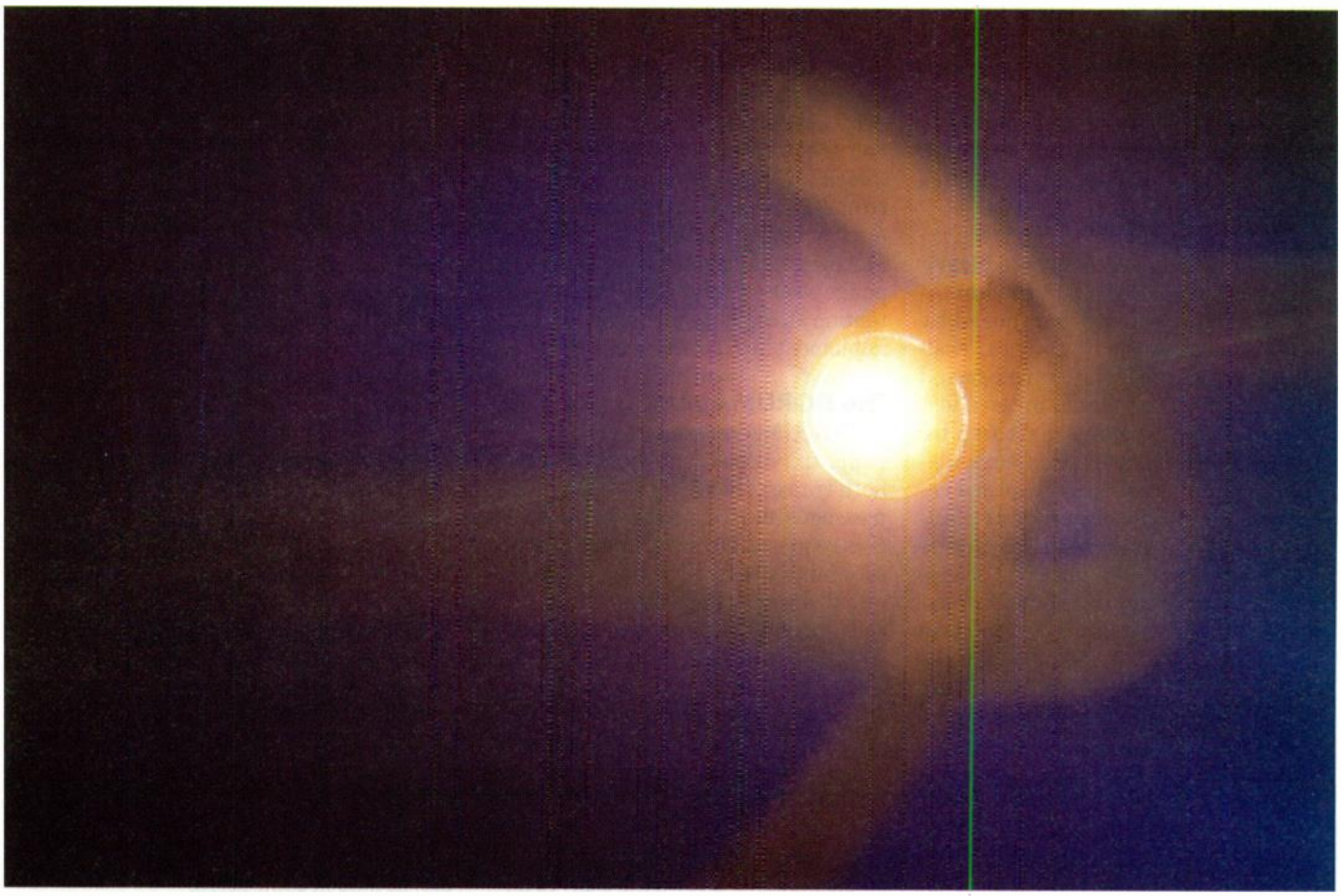

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dios capable of operating at more than 20 Mbit/s, and no such products are commercially available today. At the media-access-control (MAC) layer, wireless ATM requires a new protocol that includes QoS facilities and offers better bandwidth efficiency than Ethernet protocols. At the data-link layer, multiple protocols will be required to guarantee cell delivery. Streams such as MPEG video will require real-time, forward error correction (FEC).

To develop a suitable PHY layer, researchers must overcome both technical design challenges and the limitations on RF bandwidth imposed by agencies such as the FCC. These challenges make optical infrared-based systems simpler to build in the short term. Infrared systems don't require complex frequency or phase-modulation schemes. Instead, an optical receiver simply detects pulses of infrared energy. Infrared PHY layers have been proven very effective within the confines of a room. For example, the MII test bed is currently using 10-Mbit/s infrared optical links which can can successfully stream video between a PBS and Type-1 host.

RF PHY layers will be required to support larger coverage areas. Researchers are making progress in the RF area—for example, the FCC has opened 300-MHz of spectrum in the 5-GHz band for unlicensed-national-information-infrastructure (U-NII) usage. With more spectrum, researchers must develop a way to overcome multipath reception which results in a space- and time-varying wireless channel. Equalization schemes can eliminate multipath reflections, but they add overhead, and must be performed over and over again in a time-varying channel.

RF PHY-layer research will likely lead to the choice of a constant-amplitude-modulation scheme, such as frequency-shift keying (FSK), or one of its many derivatives. The possibility also exists for implementation of a multi-rate system that leverages high bit rates when a wireless channel's signal-to-noise ratio (SNR) is high, and has low bit rates when it degrades. The researchers believe that ultimately a radio with a single nondirectional antenna can approach a bandwidth efficiency of 1 to 2 bit/s/Hz., or 20 to 40 Mbit/s in a 20-MHz channel.

At the MAC layer, meanwhile, researchers have already developed alternatives to the carrier-sense multiple-access with collision-detect (CSMA/CD), and carrier-sense multiple-access with collision-avoidance (CSMA/CA) schemes used in Ethernet and wireless LANs today. One new protocol called distributed-queueing request update multiple access (DQRUMA, pronounced "dee-que ruma"), employs a demand-assignment scheme to minimize cell latency. Moreover, the protocol separates the packet-scheduling and channel-contention algorithms, making it simple to implement QoS guarantees.

The DQRUMA MAC Layer

DQRUMA maximizes efficiency by using fixed-size time slots to handle both transmission-request/permission messages and data cells. All media-access requests, however, are partitioned into mini-slots within designated request-access (RA) slots, while data cells traverse the link using full slots.

A mobile node that has data to send issues an RA command via a mini-slot *(Fig. 2)*. It then listens for permission via Xmt_Perm mini-slots. Once a node begins transmitting, it can piggyback additional bandwidth requests in the data slots to further optimize delay-throughput performance. The slot-by-slot scheduling allows the PBS to allocate bandwidth on a QoS basis, unlike Ethernet environments in which the first node that grabs the channel immediately begins transmission.

On top of the MAC layer, the data-link layer must provide a means by which end-to-end data transfers can be guaranteed. With no QoS in the Ethernet world, the data-link layer can use a static protocol without regard to packet latencies. In the wireless-ATM environment, however, QoS assignments will dictate a dynamic choice of protocols. The protocols must provide zero probability of loss at one extreme, thus ensuring 100% accurate delivery of critical data files. At the other extreme, the protocol must minimize delay.

For example, streams such as MPEG video will be transmitted using a minimum-delay QoS protocol. The minimum-delay protocol will use FEC to correct most errors. Small errors have little impact on the appearance of decoded MPEG video, or the sound of decoded audio. Meanwhile, a protocol such as automatic repeat request (ARQ) will likely be used to simplify the implementation, yet guarantee accurate delivery of data cells.

The State Of Wireless ATM

After considering the depth and breadth of the challenges to wireless ATM, its easy to doubt the viability of the technology. Already, however, researchers have demonstrated many of the key elements of the network in laboratories. For example, the MII project has met major milestones by demonstrating the following technologies in an end-to-end wireless-ATM system:

- A 10-Mbit/s infrared wireless link, capable of low-overhead, single ATM-cell transmissions.
- The DQRUMA protocol, including the use of priority-based scheduling in both the downlink and uplink directions.
- An adaptive data-link protocol that implements ATM cell-based FEC, using Reed-Solomon coding.
- Mobility management software that performs fast location and connection management, and performs rerouting of connections during PBS hand-offs.
- Real-time MPEG-2 video viewing and high-speed Internet links for mobile notebook computers.

These demonstrated capabilities represent the first step toward broadband wireless networks that could ultimately provide worldwide access to the Internet or other services.

Kai Eng is the head of the Broadband Systems Research department at Bell Laboratories. He received his Doctorate of Engineering Science in electrical engineering from Columbia in 1979. Since 1979, he has been with Bell Laboratories, Holmdel, N.J., where his work has spanned research on TV transmission, video information systems, LAN, MAN, optical networking, switching theory, and ATM switching, as well as wired and wireless ATM networks. He is a fellow of the IEEE.

How Valuable	Circle
Highly	537
Moderately	538
Slightly	539

Variable-Bit-Rate Receiver Targets Upstream CATV Headends

Burst-Receiver-Demodulator Addresses The Hybrid-Fiber/Coax (HFC) Environment.

Paul McGoldrick

One of the hottest issues in the world of CATV is the use of the cable infrastructure for two-way interactivity. Interactive TV, per se, has been a highly-touted offering for the consumer, but one that the consumer has not embraced with real enthusiasm. Now, other functions appear viable for the two-way cable system. Some, such as video-on-demand (VOD) or "nearly-on-demand," require little bandwidth on the return (upstream) path to the headend (from the subscriber to the headend)—just enough for simple instructions on program requirements and billing. Internet access or computer networking, on the other hand, could be as bandwidth-hungry as the space available.

There are various estimates about the percentage of cable plants that are technically ready for two-way service. They range from 20 to 40%. But the cable systems that are profitable are, in general, upgrading to hybrid-fiber/coaxial (HFC) systems to allow for that capability.

The most difficult part of the subscriber-CATV-subscriber loop is the design of the headend receiver. Now, Stanford Telecom has made that job much easier with its STEL-9257 variable-bit-rate headend receiver. Stanford believes that this part is one of the first OEM upstream receivers to address the HFC environments.

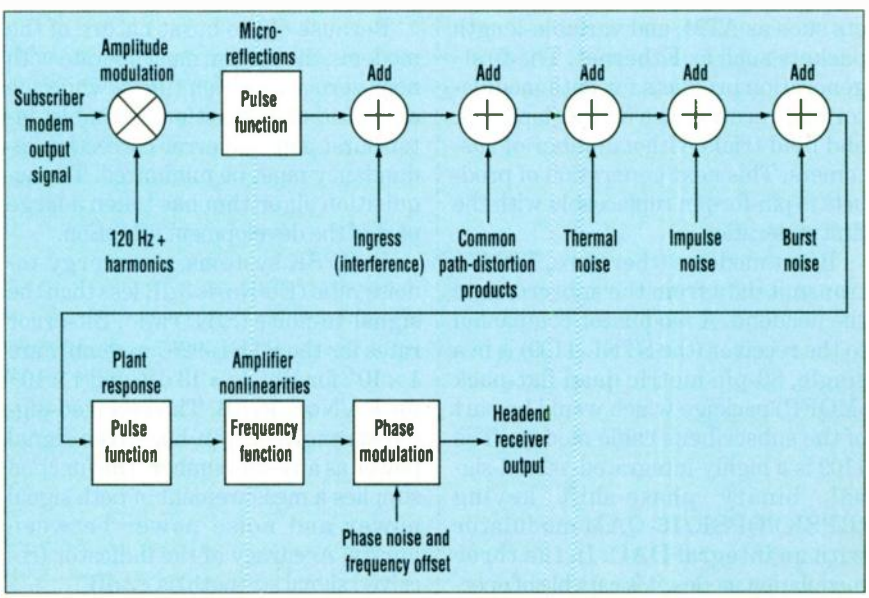
Downstream cable channels are carried from 54 MHz up to between 650 and 1000 MHz, depending on the system and its age. For now, the downstream modulation used on the system is conventional vestigial-sideband video and FM audio, but that will change with the conversion to digital and compressed signals with multiple video offerings, or other services, in a single channel. Nevertheless, the distribution is conventional, with the signals split from trunk feeds with levels continuously set by the line amplifiers for the optimal performance of that system.

The upstream path is very different in the two-way system. In the band from 5 to 42 MHz, signals from hundreds and thousands of subscribers are mixing and additively feeding into common nodes, and then back to a single point at the headend. But it is not just the data signals that add, it's all that noise! And even when the subscribers are not generating signals from their modems, many of the sources of noise are still active and still passing back.

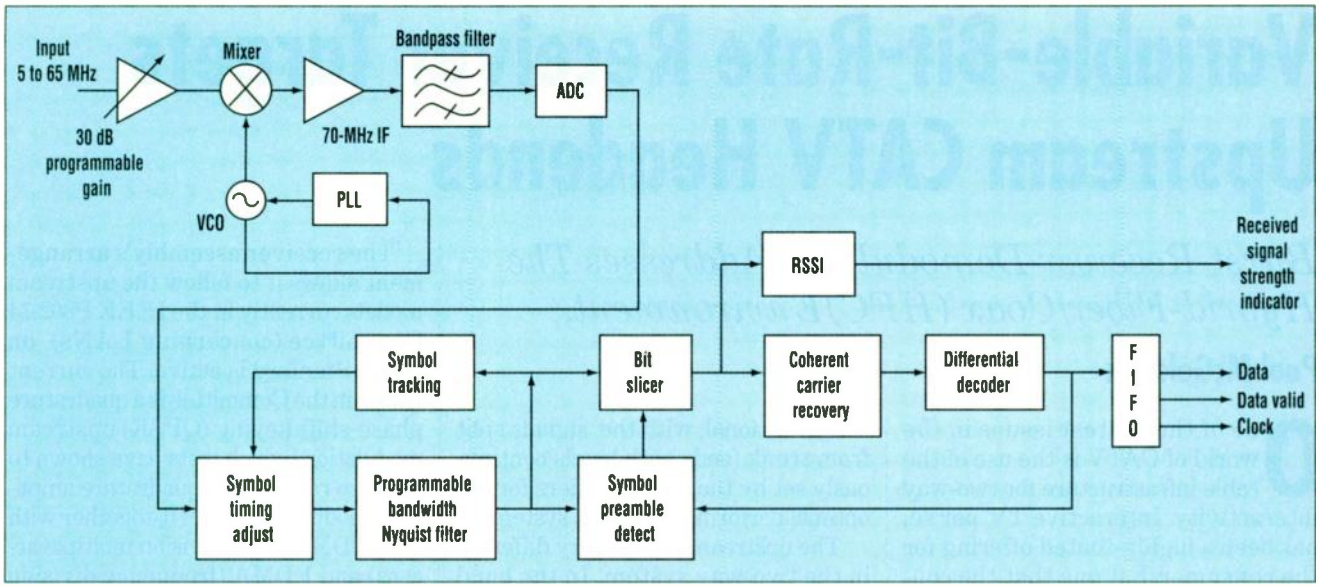
The challenges for the upstream path are such that the number of players in the market—compared to those in the downstream cable modem market—is really small. As a result, Stanford Telecom has established itself as an important force in the area with the STEL-9257.

The receiver assembly's arrangement allows it to follow the upstream models currently in the IEEE P802.14 Committee (concerning LANs), on which Stanford is active. The current leader in the Committee is a quadrature phase-shift keying (QPSK) upstream modulation [which tests have shown to be more robust than quadrature amplitude modulation (QAM)], together with both TDMA (time division multiple access) and FDMA (frequency division multiple access). The Digital Audio-Visual Council (DAVIC) has already accepted QPSK as their standard.

The IEEE model for the channel looks at the subscriber signal as it moves from home to headend *(Fig. 1)*. Various channel effects are shown in an arbitrary order. Signals such as multiples of the line frequency (120 Hz and harmonics) amplitude-modulate the signal, while most others are additive problems. The principal sources of the problems are created by poor connectors and drops, terminators, corrosion, location to other electro-magnetic signals, and the normal antenna pickup of terrestrial broadcasting. Nonlinear effects are dominant in the amplifiers in



1. The IEEE 802.14 Standards Committee upstream-channel modem with various sources of additive- and mixed-interference problems.



2. Block diagram of the Stanford Telecom STEL-9257 variable-bit-rate headend receiver for the CATV upstream return path.

the system, and are compounded in HFC systems because the laser characteristics are so different from electrical signal amplifier devices. Additionally, dynamic range limitations increase nonlinear effects in HFC systems. The diplexer filters that separate and recombine downstream and upstream signals also cause linearity problems, particularly at the higher end of the upstream band. Impulse and burst noise are felt by many to be the worst problems on the return path.

The STEL-9257 is Stanford's second-generation product. It offers variable-bit-rate capability, as well as the ability to track both fixed-length packets such as ATM, and variable-length packets such as Ethernet. The first-generation products for both modulator and receiver are in development, and field trials with a number of customers. This next generation of products is pin-for-pin replaceable with the first generation.

Burst modems (therefore, TDMA) transmit data from the subscriber to the headend. A modulator companion to the receiver (the STEL-1109) is in a single, 80-pin metric quad flat-pack (MQFP) package which would be part of the subscriber's cable modem. The 1109 is a highly-integrated, mixed-signal, binary phase-shift keying (BPSK)/QPSK/16-QAM modulator with an integral DAC. In the three modulation modes, it is capable of operating at 10.3 Mbits/s, 20.6 Mbits/s and 41.2 Mbits/s, respectively, and can generate carrier frequencies up to 66 MHz.

The STEL-9257 receiver has a mixture of technologies *(Fig. 2)*. The 75-W front end has a 30-dB variable-gain amplifier, programmable in 1-dB steps. This design allows it to handle input signal levels from -15 to +15 dBmV, with an input-return loss of better than 18 dB. A digitally-controlled, phase-locked loop (PLL)/voltage-controlled oscillator (VCO) loop can be set in 100-Hz steps from center frequencies of 5 to 65 MHz, to convert the incoming signals to an intermediate frequency of 70 MHz. The baseband signals are then produced from an analog-to-digital converter acting as a digital down-converter.

Because of the burst nature of the modems, the system must operate with near-zero acquisition times, while the overhead of acquisition preamble, inter-burst gap, and error-correction redundancy must be minimized. The acquisition algorithm has taken a large part of the development attention.

In QPSK systems, the energy-to-noise ratio (Eb/No) is 3 dB less than the signal-to-noise (S/N) ratio. Bit-error rates for the STEL-9257 assembly are 1×10^{-6} for Eb/No = 13 dB, and 1×10^{-9} for Eb/No = 15 dB. The received-signal-strength output bus gives signal power as an 8-bit number. The function supplies a measurement of both signal power and noise power between bursts. Accuracy of the indicator (received signal strength) is ±2 dB.

The data rates that the receiver can handle vary between 0.256 Mbits/s and 5.12 Mbits/s. The effective bit rates for an equivalent QPSK modulation are 0.128 Mbits/s to 2.56 Mbits/s burst symbol rates, which will require 160 kHz to 3.2 MHz of allocated bandwidth. Data rates between the extremes can be varied with 1-kbit/s resolution.

The Nyquist filter in the QPSK demodulator is programmed to the data rate. A symbol feedback loop minimizes edge-timing errors especially for long-packet lengths. The decoded data also are fed back to detect the symbol preamble, which can be 14 symbols (28 bits), 16 symbols (32 bits) or 16-symbol DAVIC.

Burst lengths can be programmed from 32 to 8192 symbols (fixed), or can be fully variable in length. The guard time between bursts can be as low as 3 symbols, but is 11 symbols for variable-packet lengths. Complete control of the assembly is on a serial bus at TTL levels at a rate of 19.2 kbaud.

Price And Availability

The STEL-*9257 is priced at $625 in 1000 quantities. The assembly is sized at 3.5 by 5.5 by 0.5 in. The companion modulator, the* STEL-*1109 is available at $15 in 10,000 piece lots.*

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UPDATE ON SATELLITE COMMUNICATIONS

Inexpensive Standardized Satellites Deploy Payloads Faster, Better, And Cheaper

Space, the final frontier—sole province of governments and multibillion-dollar communications giants. Until now, that is. Thanks to the rapidly-shifting economics of the aerospace business, it soon will be possible for smaller corporations, scientific organizations, and even universities to purchase a small, sophisticated low-Earth satellite, which can be delivered on-orbit for a fraction of the price of a conventional Comsat. Space Systems/Loral, Palo Alto, Calif., has recently announced that it will be making available copies of the spacecraft busses that were developed for the Globalstar low-Earth orbit (LEO) communication satellite constellation.

Marketing mavens at Loral are betting that the low cost of these compact, but powerful spacecraft will find a wide variety of applications. Such targets include specialized communications, commercial remote-sensing ventures, and budget science projects for universities and research institutions. NASA and Jet Propulsion Laboratories have expressed strong interest in using these generic spacecraft to carry a wide variety of Earth observation experiments for the new breed of "faster, better, cheaper" science missions, envisioned by NASA Director Dan Goldin. By making use of innovative mass-production techniques and leveraging its existing launch, telemetry, and control infrastructure, Loral is challenging the conventional wisdom that has dominated the aerospace community since its inception.

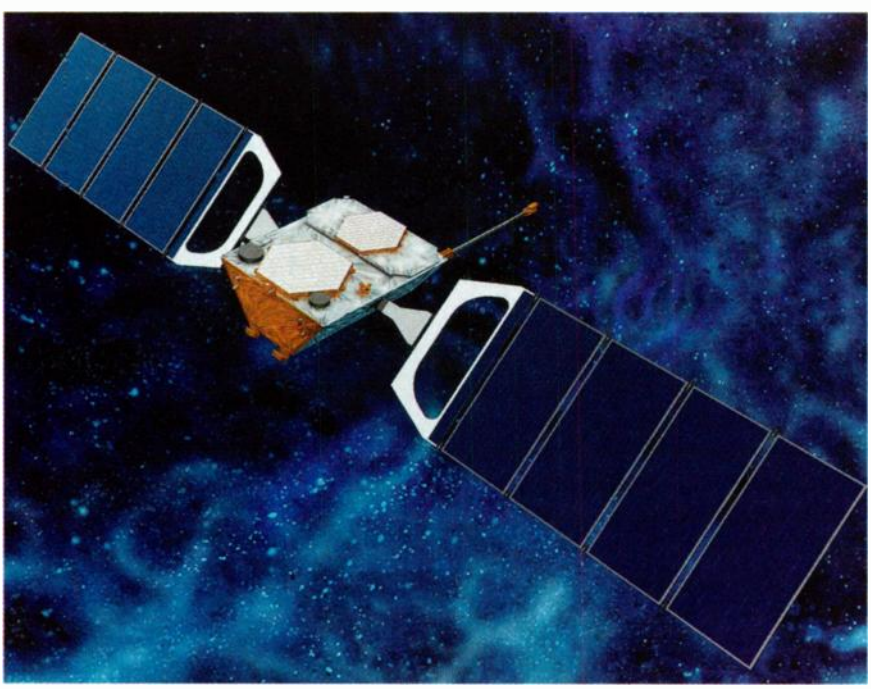
There has always been a peculiar chicken-and-egg syndrome surrounding the prices of satellites. Because a launch vehicle can easily cost $50-$100 million, there has been little or no incentive to aggressively reduce the cost of the satellites themselves. Instead, manufacturers have concentrated their efforts on making their spacecraft last as long as possible on orbit. The traditional approach to high reliability has been to use expensive, labor-intensive assembly and quality control techniques borrowed from the manned space flight program of the sixties. This manufacturing style led to a culture where spacecraft were designed and built as custom, one-of-a-kind products, and a production run of three or four units was considered large.

The recent flurry of interest in LEO-based communications systems, which employ large constellations of small-to-medium-sized satellites, has finally upset the equilibrium, giving rise to a new breed of lower-cost, mass-produced spacecraft. Several companies are rushing to fill the sky with networks of dozens of satellites that are small enough to allow a few to a ride on a single booster, but sophisticated enough to form the backbone of an orbital telephone network.

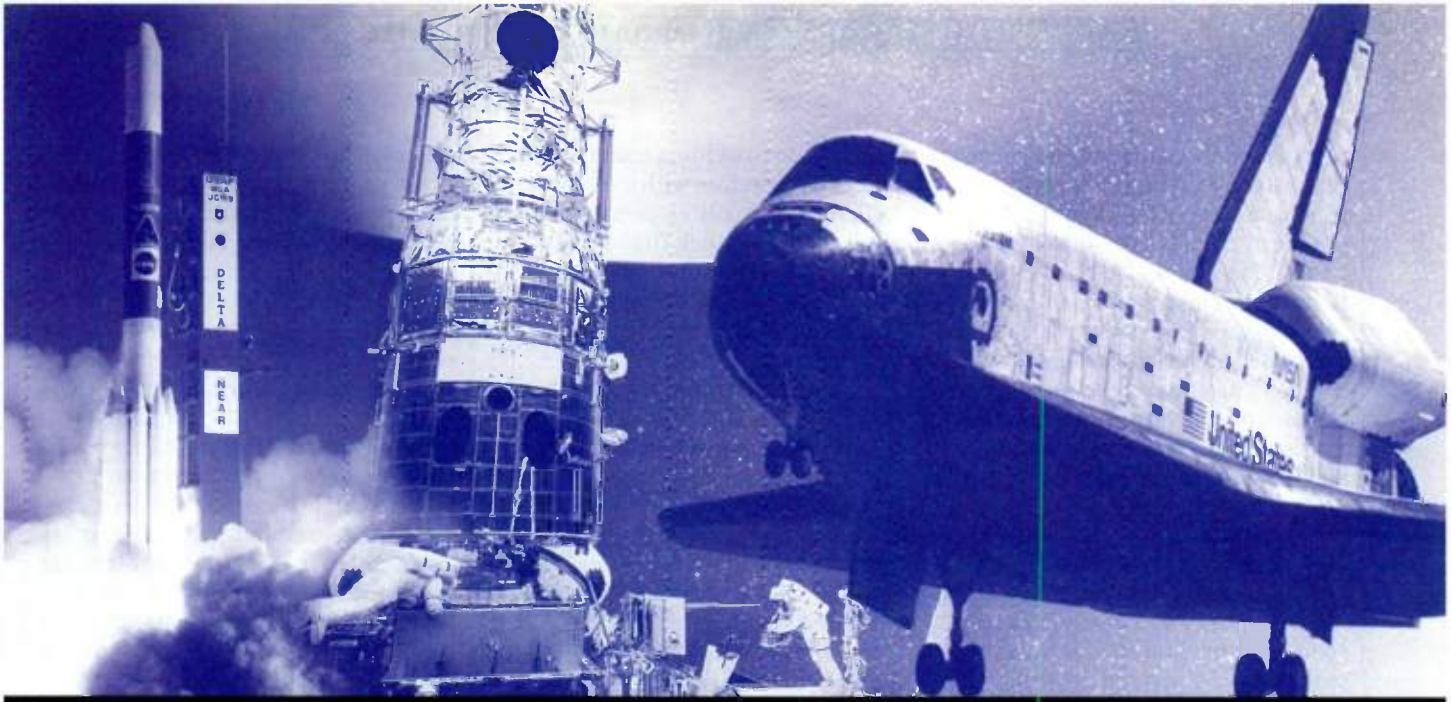
Loral's Globalstar program is one of the more promising ventures, consisting of 48 satellites that will form a global web, providing voice, data, messaging, and location services. The Globalstar satellite itself is a box, a little over 6 ft. high, and about 3 ft. deep. Its Earth-facing surface is just under 6 ft. wide, while its narrower anti-Earth panel taper the width to 4 ft. in the rear. This trapezoidal profile *(see the figure)* makes it easy for several spacecraft to be clustered together within the cramped confines of a launch vehicle's nose cone. Its two deployable solar arrays can supply up to 1600 W, with as much as 1400 W available for payload operations. The standard craft itself weighs a shade under 1000 pounds, including its 330-lb. payload of Globalstar communications.

For custom applications, the same vehicle can accommodate payloads of up to 36 cubic ft., weighing as much as 484 lb. The satellite's three-axis stabilization system enjoys a high degree of redundancy, including a backup attitude-determination system. The system employs a differential-global-positioning system (GPS) to control pointing within 0.6 degrees, in case the traditional gyro platform and Earth-sensors fail.

Rather than take the conventional approach to designing Globalstar, Loral chose to control cost and quality through the use of modern, process-oriented design and manufacturing practices. The result is a modular spacecraft, delivered in fully-tested, interchangeable subsections that requires a minimum of testing and assembly at the final integration stage. In the event of a problem with the electrical power, propulsion, control, or pay-



Shaped like a trapezoid, the compact, lightweight Globalstar satellite is a heavyweight when it comes to lifting payloads into orbit. Totalling just 1000 pounds itself, Globalstar can handle payloads of 484 lb. and 36 cubic ft. in volume.



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load/telemetry subsystems, a spare unit can be substituted from stock, or from a unit slated for a later launch.

One of the keys to Globalstar's low cost and flexibility is the use of a distributed telemetry and command processing system. In conventional spacecraft, each power line, telemetry point, and control signal is carried back to a central command/telemetry processor via a separate set of wires. Rather than add the weight, complexity, and cost of several thousand wires running through the entire spacecraft, Loral's engineers designed an LSI-based multi-chip module, called a branch module. The branch module executes commands from, and passes telemetry to the central flight computer via an industry-standard IEEE-1553 serial bus.

Each 2-in. square module can be configured to perform a group of tasks, such as activating power relays, providing logic pulses to command subsystem functions, or relaying several analog and digital telemetry signals back to the central processor. One or more of these branch modules can be easily adapted to provide a command and telemetry interface with a custom payload, requiring only elementary modifications to the stock flight software. This flexibility allows payloads to be controlled from the ground via the existing Globalstar tracking, telemetry, and command infrastructure.

Depending upon the application, a spacecraft can either be launched into its own orbit using a (relatively) small Pegasus- or Taurus-class rocket, or it can "rideshare" a launch with the Globalstar fleet. If an application uses one of Globalstar's 52-degree-inclined orbits, significant savings can be realized by riding up as one of four satellites aboard an American Delta rocket. Loral also will be using the Russian Soyuz booster to loft four craft at a time into orbit. There's also the larger Zenit model that carries as many as 12 Globalstars at a time.

Globalstar officials are reluctant to discuss the exact price of an on-orbit satellite, but the bus itself should run in the $10-to-$15 million range. That does not include a similar charge for sharing part of a launch. While this is not pocket change, it is so much less than a conventional solution that an entire range of new space-borne applications could become commercially viable. "Of course, your mileage may vary," says Fred Green, director of Advanced Studies for the Globalstar program. He explains that the actual cost of a Globalstar depends on many factors, including a customer's orbital requirements, desired launch schedule, and willingness to use the Globalstar Bus on an as-is basis. While it can be modified to accommodate unusual requirements (at extra cost), Green is confident that his spacecraft's generous mass, volume, power, and control provisions will allow most passengers to enjoy the ride with a minimum of customization.

For further information on the Globalstar communication system or the Globalstar spacecraft, contact Lisa Koppel, at Loral Space & Communications, 1755 Jefferson Davis Highway, Suite 1007, Arlington, VA 22202; (703) 414-1049, fax (703) 414-1075, e-mail: 102715.3610@compuserve.com.

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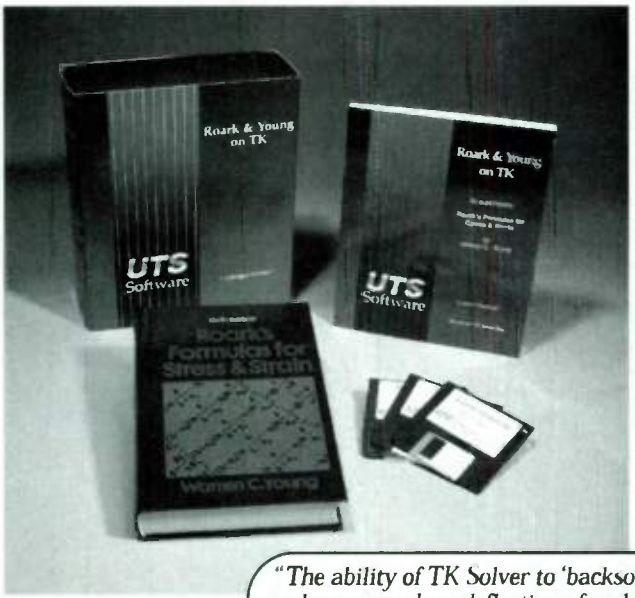

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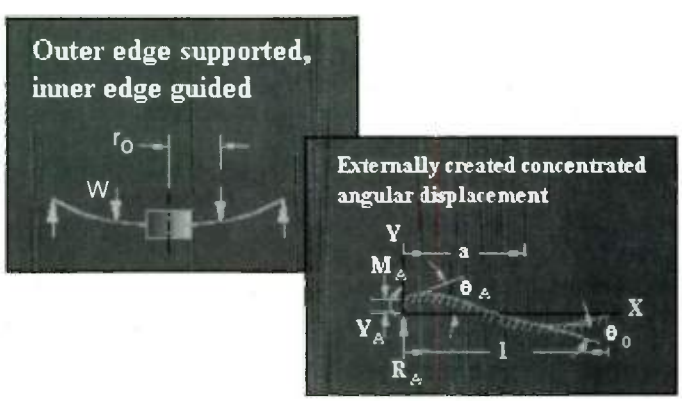

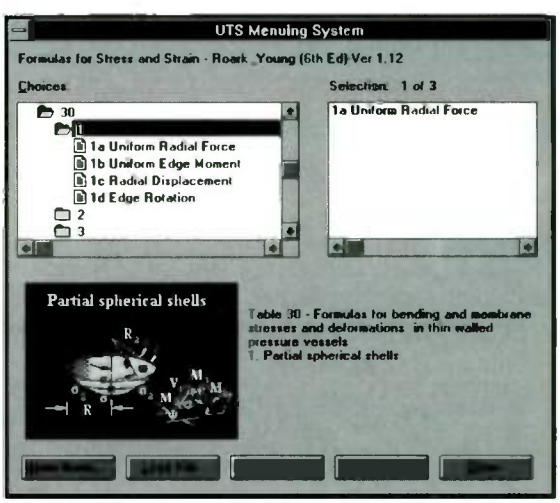

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Integrated Switch/Controller Cuts Cost Of Managed Ethernet Switching To $100/Port

A new integrated Ethernet switch and controller chip will allow network equipment designers to add management capability to their switched Ethernet products. And such management can be incorporated while still meeting the critical $100 per-port price threshold. The PM3350 switch/controller combines eight, 10-Mbit/s switched Ethernet channels, a shared-memory switching controller, and a 50-MHz RISC processor optimized for switch and management functions.

An on-chip PCI bus interface can be used to as a host interface or as an expansion bus for high-density and stacked switch products. It accommodates traffic from up to 64 Ethernet ports, allowing eight PM3350s to share the same PCI bus without loss of any throughput. Furthermore, the PCI bus can be utilized to add a high-speed backbone interface to the switch by incorporating a 100-Mbit/s port chip.

The PM3350 filters and switches at wire rates (up to 14,480 packets per port). It also performs all address learning, table management, and aging functions for up to 32,768 MAC addresses, with a learning rate reaching 10,000 addresses per second. On-chip, user-enabled, back-pressure flow control is available as well, with configurable per-port buffer thresholds and limits.

Constructing an eight-port switch with the PM3350 requires only a pair of quad Ethernet PHY interface chips and their associated magnetics, an SRAM chip for the switch buffer, and some nonvolatile program memory for the RISC controller. The reduced parts count turns into additional savings in board and case size, assembly and test labor, as well as component cost.

The on-chip controller's embedded software makes it possible to implement the simple network management protocol (SNMP) management information bases (MIBs), thus providing control, diagnostic, and statistics collections functions. Both in- and out-of-band signalling are supported via a TCP/UDP/IP protocol stack. RMON statistics also are maintained on a per-port basis.

A hardware and software reference design is available, as well as a 16-port evaluation board, to help speed the development process. Available immediately, the PM3350 comes housed in a 240-pin PQFP. Overall cost is $69 each in quantities of 10,000 pieces.

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PRODUCT FEATURE

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Single-Chip Transceiver Supports Both Gigabit Ethernet And Fibre Channel

Designers will now have one more tool to reduce the cost of Gigabit-speed networks: a single-chip transceiver that is able to work with both Fibre Channel and Gigabit Ethernet applications. The S2052 is intended for use in cost- and power-sensitive applications in all kinds of high-speed network equipment.

In Fibre Channel networks, it is well suited for adapter cards, file servers, and RAID storage systems. In Gigabit Ethernet networks, the transceiver is expeted to find a home in places like adapter cards and line interface ports on network switches, routers, and hubs.

The device is capable of operating at either the 1.062-Gbit/s Fibre Channel frequency, or the faster 1.25 Gbits/s that is specified for Gigabit Ethernet applications, giving it unparalleled flexibility. Its industry-standard media-independent interface (MII) permits it to work seamlessly with nearly every one of the PHY-layer transceivers conforming to the requirements of the proposed 802.3 HSSG specification. This specification includes fiber-optic or coaxial cables, or twinax cables

Using a state-of-the-art, low-power bipolar process, the transceiver's receiver section incorporates an on-chip PLL to synthesize its high-speed clock from an inexpensive low-speed reference crystal.

Its receiver employs a second PLL to synchronize the incoming data stream and recover both clock and data signals. A bidirectional, PECL-compatible I/O interface is designed to minimize line jitter, a critical factor in both long-and short haul fiber-optic applications.

To facilitate manageability, the S2052 incorporates a local loopback feature, which gives products using the transceiver the capability of self-diagnosis. An integrated filter greatly reduces the number of external passive components required to implement a fully operational Fibre Channel or Gigabit Ethernet interface. This is a double advantage, saving both parts and assembly costs.

Housed in a standard 64-pin PQFP, the transceiver dissipates only 0.8 W of 3.3-V power when fully operational.

Priced at $18.95 each when purchased in lots of 10,000, the S2052 is available in sample quantities immediately, with full production slated for later this month.

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CIRCLE 562

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Quad And Octal ADPCM Processors Expand Analog Phone-Line Capacity

A pair of adaptive differential pulse-code-modulation (ADPCM) transcoders can help build equipment that increases the amount of voice traffic on a single subscriber loop by a factor of four or eight. Using the ITU G.726 and ANSI T1.301 standards, the TP11362A and TP11368 convert standard 64-kbit/s A-Law or μ-Law PCM voice channels into the more compressed ADPCM format, and multiplex them together for transmission across a standard 8-kHz frame. When used with the TP3410 or other ISDN basic rate adapter, one 8-kHz PCM stream can support four or eight ADPCM voice channels.

Besides greatly expanding the capacity of wired infrastructures, the transcoders have applications within DECT cordless phone systems, larger-scale wireless PBXs, wireless key telephone systems, and satellite communications.

The TP11362A is a quad ADPCM transcoder that supports encoding and decoding of ITU-compliant 40-, 32-, 24-, and 16-kbit/s digital voice streams, as well as ANSI-compliant 32-kbit/s traffic. It can operate on up to eight independent channels in each 8-kHz frame, giving designers the option of implementing four, full-duplex or eight, half-duplex channels, or any combination thereof. Its companion, the TP11368, can support 16 half-duplex or eight full-duplex channels.

In a typical application, the transcoders take two or more standard 64-kbit/s PCM digital voice channels and multiplex them within the same bandwidth normally used for a single channel. They do this by applying compression algorithms that reduce each 8-bit PCM code to a 2-to-5-bit ADPCM code, depending on the selected bit rate. The ADPCM encoder converts the 64-kbit/s PCM input into a uniform PCM signal, which is subtracted from an "estimated" signal obtained from an on-chip adaptive predictor.

The ADPCM decoder reconstructs the original PCM signal by adding the received quantized signal to the signal estimation calculated by the predictor. A synchronous coding adjustment unit prevents cumulative distortion that can occur on synchronous tandem coding under certain conditions.

Both transcoders meet ITU G.726 and ANSI T1.301 specifications. Power consumption is 8 mW/channel at 5 V. They are both available now in surface-mount or DIP packages. Pricing in 1000-piece quantities are $16 for the TP11362, and $32 for the TP11368.

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Growing Networks As network capacities expand, address filtering gets too complex for conventional scheme searches. MUSIC's new 32 Bit Wideport LANCAMs are much more efficient. Searches are done in parallel; output is data ready for use. CAM (Content Addressable Memory) produces matches within large lists in a short, constant time period - *critical to high end networks such as ATM or Gigabit Ethernet.*

Greater 64-128 Word Width With 32 bit I/O, MUSIC Wideport LANCAMs support extra bandwidth. The 2485A/L has a 2k x 64 bit density, suitable for applications designed for high speed MAC address processing. The wider 1k x 128 CAM array of the 1965A/L handles long address matches necessary for LAN-to-ATM, IPV4/IPV6 routers, and VLAN switches. *Wideport LANCAMs don't let network address length slow down a network.*

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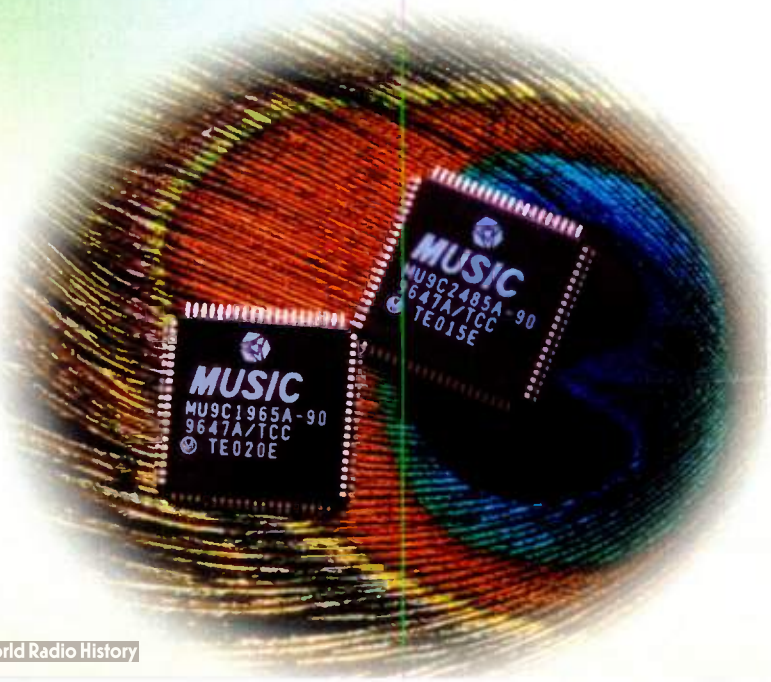

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STANDARDS WATCH

Defining The Home Network

Joel DiGirolamo, Lexmark International Inc.

For the last two years, members of the Video Electronics Standards Association (VESA) have been hard at work on a standard for home networks. The VESA Home Network Committee will be writing a standard that permits interoperability of different devices and networks in the home. Such a standard will allow consumers to purchase consumer electronics devices in the retail market, plug them into their network, and have them accessible and usable without any configuration hassles.

The VESA Home Network Committee is represented by manufacturers from a number of industries, including consumer electronics, semiconductors, computer hardware, computer software, connectors, media, home automation, and telephone companies. Hoping to get the necessary cross-industry input, the committee also is connected to groups working with related technologies, such as set-top boxes, in-home gateways, and cable television provider networks. In addition, the home network must be flexible enough to support new technologies as they become available, and open enough so that manufacturers and developers can easily design and build equipment for it.

The standard will be an interoperability specification that allows the transfer of information from one device to any other device in the home. There are and will continue to be networks in the home with widely differing requirements. A home network must allow subnetworks to exist so that all devices won't need a constant connection to a high bandwidth, relatively complex network. For example, devices such as telephones and intercoms do not require access to the same network as an HDTV. As a result, the home network that has been defined is intended to unify all the subnets so that they can all communicate.

An analog network exists in most homes today, typically in the form of coaxial cable running from room to room. This network will continue to exist until analog TVs are no longer used or inexpensive digital-to-analog converters are available.

External network service providers, such as telephone and cable-TV companies, will provide data into and out of the home. They'll need to connect to the home network for distribution to the various devices in the home. The VESA Home Network Committee is planning to define an interface for the service providers to connect to.

Because many different devices will be plugged into the home network, a directory of devices also must be made available. This directory would receive a device's information when the device is plugged into the network or one of the subnetworks. Device management would let users interact with them through one common user interface, such as a dedicated Web server.

Users may have a CEBus or X-10 set of devices in their homes to handle "home automation." For example, when a CEBus network port is bridged between the home network and the CEBus network or powerline, the CEBus devices are presented to the home network and then inserted into the directory system. Address translation also will take place at this network port.

A modified version of the IEEE 1394 (FireWire) bus has recently been chosen as the backbone for the VESA home network, pending completion of hardware construction. This backbone is intended to be capable of at least 50 Mbits/s with minimum cable lengths of 50 m.

As of this writing, the VESA Home Network Committee is working on the internetworking issues so that data can be routed to the proper devices for proper addressing. In addition, user names must be assignable in order to make the entire system user-friendly.

A flexible, open home network standard will help to provide additional momentum toward the adoption of products. By utilizing this process, manufacturers, installers, and users will have the opportunity to give their input on and help shape the home network. This will go on to assist manufacturers to ensure that their devices are being built to the standard and will eventually be recognized when plugged into the home network. The network is being designed in such a manner that the user will be given the option to connect just two nodes or to completely wire the whole house.

The VESA Home Network Committee will be demonstrating the home network technology during the course of this year at various industry events to showcase its ability to deliver multiple simultaneous video streams and multiple types of data over long distances, as well as connecting to multiple network types. For more information on these developments, contact VESA at (408) 435-0333 or on the Internet at http://www.vesa.org.

Tips On Designing A High-End CompactPCI Board

CompactPCI Is The New Kid On The Block, But Could Soon Turn Into A Formidable Competitor

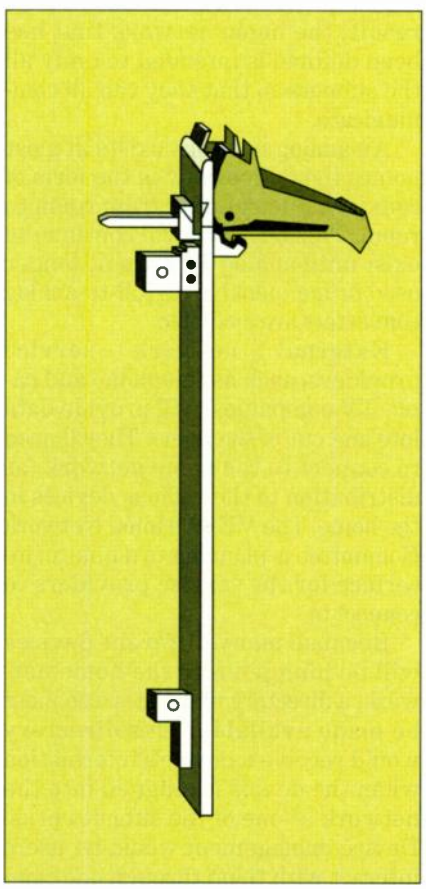
JIM MEDEIROS, Ziatech Corp., 1050 Southwood Dr., San Luis Obispo, CA 93401; (805) 541-0488.

The CompactPCI bus specification, introduced in 1995, combines the electrical specification of the traditional desktop PCI bus with a mechanical "Eurocard" form factor made popular by older architectures such as VMEbus and Multibus II. Combining computing bandwidth with a rugged form factor, a 32- or 64-bit CompactPCI platform is suited for various industrial control applications. In addition to discussing the general steps necessary to design a CompactPCI board, this article will detail three distinct scenarios: sporting a PCI board designed for a desktop PC to CompactPCI; designing a CompactPCI board using a specification chip set; and designing a CompactPCI board from scratch.

Before describing the particulars of the CompactPCI recipe, it's important to understand the general ingredients. At the heart of CompactPCI is the PCI specification originally created by Intel as a means to define a single local bus for chip-set ICs within the staid PC. Through the adoption of rugged packaging, a more sophisticated connector, and a unique signal-termination technique developed through bus simulation, this architecture was transformed into CompactPCI, a modular architecture suitable for professional applications.

The Eurocard form factor was chosen for CompactPCI because a wide variety of manufacturers already provide off-the-shelf card cages and mechanical fixtures for this specification, which is the same packaging used for the VMEbus. The Eurocard specification defines 3U (100 by 160 mm) and 6U (233.35 by 160 mm) form factors. Most CompactPCI designs will use the 3U and 6U sizes.

The mechanical components of CompactPCI comply to the IEEE P1101.10 and IEEE P1101.11 specifications, which provide additional mechanical specifications to the IEEE 1101.1 specification on which most VMEbus systems are based. The newer specifications are supported by both CompactPCI and VME64 extensions, further assuring a reliable supply of enclosures, board ejectors, board guide rails, and other mechanical components covered by the CompactPCI specification.

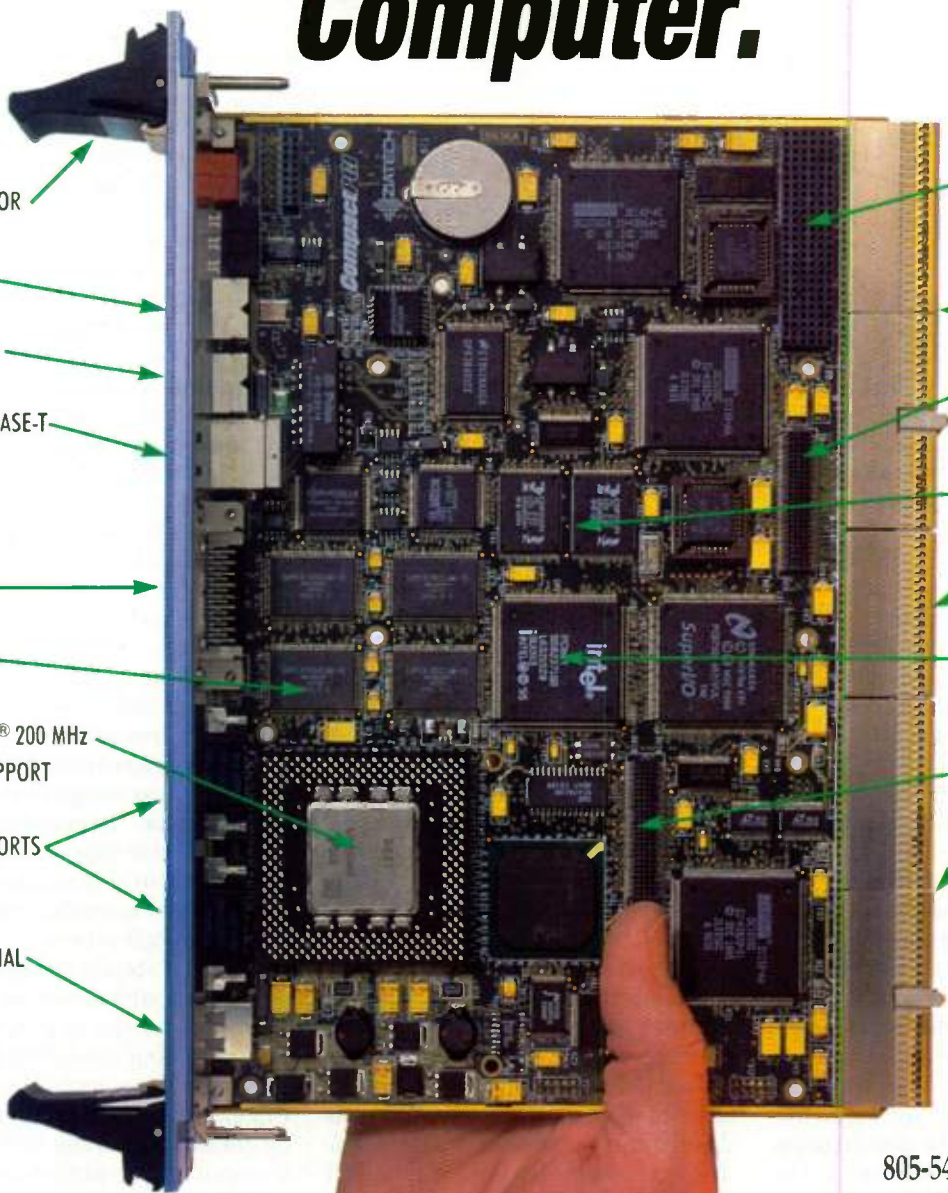


1. Extractor handles are required for single-height 3U and double-height 6U form factors, and filler panels. The handle is connected to a prealigned pin and key that secures the board in the enclosure when the handle is pushed in, and releases the connection when it's pulled out.

CompactPCI boards provide a front-plate interface that is consistent with Eurocard packaging. Extractor handles defined and illustrated by IEEE P1101.10 are required for single-height 3U and double-height 6U form factors, and filler panels *(Fig. 1)*. The handle on the outside of the front panel is connected to a prealigned pin and key that secures the board in the enclosure when the handle is pushed in, and releases the connection when it's pulled out. The IEEE P1101.10 ejector also supplies enough "ejection throw" to fully unseat the board's connector from the backplane. Suppliers of this injector-extractor include Rittal and Schroff. The ejector also locks the board into place when its lever is fully closed.This keeps a board from becoming unseated when not intended. Screws located on the top and bottom of the frontplate also may be used to firmly secure boards into the subrack. The front panel thickness is 2.5 mm.

CompactPCI features a pin-and-socket connector style that's popular in the telecommunications industry because of its modularity and reliability. This 2-mm hard-metric connector features a five-plus-two row design: five signal rows, with 47 pins per row for the PCI bus itself, and up to two outer shield rows for low-impedance connections to ground *(Fig. 2)*. The outer shield, coupled with an optimum placement of power and ground pins within the connector, improve signal propagation, reduce noise, and allow the bus to be extended to eight slots, significantly more than desktop PCI. The connector is currently manufactured by AMP, ERNI, and Framatome, and complies with the interna-

THE CompactPCI™ Computer.



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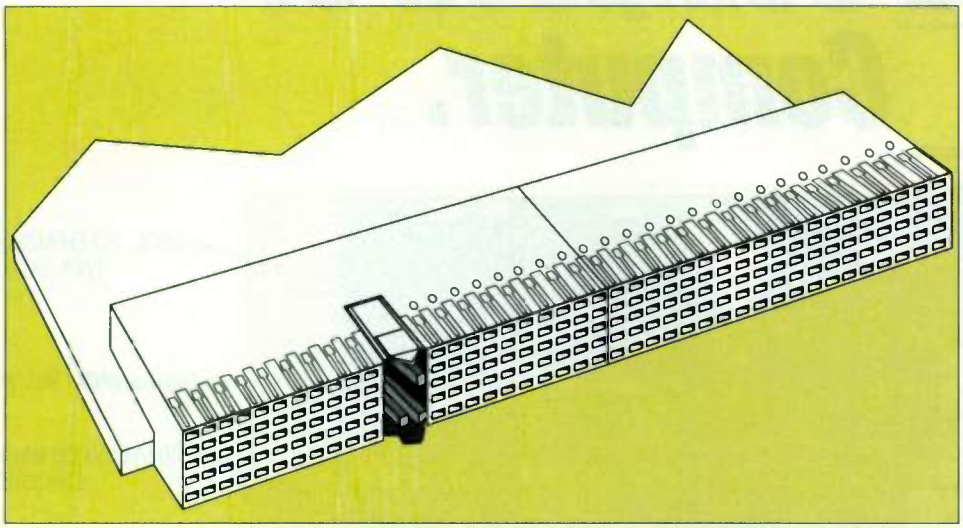

2. CompactPCI's 2-mm pin-and-socket connector employs a five-plus-two row design: Five signal rows, with 47 pins per row, and up to two outer shield rows.

tional specification IEC 1076-4-101. It also is used by VMEbus manufacturers for the P0/J0 connector.

The 32-bit PCI signals on the connector are defined by positions 1 to 25 which are, referred to as the J1 connector. The additional signals for 64-bit PCI are represented by 22 positions on the J2 connector. Several signals in both J1 and J2 are reserved for future expansion.

CompactPCI implements a keying mechanism to differentiate between 3.3- and 5-V signaling capability. The mechanism prevents a board built with one technology from being inserted into a system designed for the opposite technology. Positions 12 to 15 of J1 are used for the keying mechanism. This location also provides a mechanical guidance to the connector array to avoid pin stubbing on the connector upon board insertion. Peripheral boards that can be operated at either 3.3 or 5 V are not keyed and can be inserted into either system. These boards are referred to as Universal Boards in the PCI specification.

A CompactPCI passive backplane consists of eight board locations (connector slots) with 0.8-in. board center-to-center spacing. The backplane contains one system slot and seven peripheral slots. The system slot provides arbitration, clock-distribution, and reset functions for all boards on the bus. This slot performs the slot-specific configuration initialization by managing each local board's so-called ID Select (IDSEL) signal. IDSEL is driven uniquely to each peripheral slot during configuration cycles by the system-slot board, allowing that board to be configured in true Plug and Play fashion.

The system slot drives five buffered clocks using signals CLK0 through CLK4. Board slots receive their specific clock using the CLK pin. To minimize the effect of clock sharing, the clock connection for peripheral slots 2-3 and 4-5 must be physically connected *(Fig. 3, a)*. Adapter board slots 6-8 have a direct connection from the system slot *(Fig. 3, b)*.

The peripheral slots may contain simple or intelligent interfaces. Simple interfaces are for boards that don't master the bus, such as a VGA interface. Intelligent interfaces are boards that feature a processor or DMA logic that can master (drive cycles) the PCI bus. CompactPCI supports both types of interfaces.

PCI expansion boards designed for desktop PCs vary in height and length, as the PCI specification defines three physical board sizes and manufacturers have added even more sizes. Generally, a chip set designed for a desktop "long board" which measures 4.2 by 12.3 in is a good candidate for a 6U CompactPCI design, while a fixed-height "short board" (4.2 by 6.9 in.) is the appropriate size for a 3U CompactPCI board.

Taking into account a "Component Keep Out" area along the sides of the board and the space taken up by the connector, a 3U CompactPCI board has about 21 in.^{2} for implementing a board design. With the density of today's PCI chip sets, this usually provides enough room. Larger designs can move up to the larger 6U board size. The board thickness is 1.6 mm for boards plugged into the backplane.

The desktop PCI card connector is derived from the Micro Channel connector, a hemispherical card-edge contact as opposed to the CompactPCI pin-and-socket style. Like CompactPCI, the desktop connector supports both 32- and 64-bit signals and uses a keying mechanism to differentiate between 3.3- and 5-V environments. But the density of the CompactPCI connector allows it to support the PCI signaling environment in a smaller footprint than desktop boards, and it's superior reliability improves the reliability of CompactPCI. Additional reference signals (V_{cc}, 3.3 V, and Ground) were added to provide a lower noise environment for the PCI signals as compared to the desktop connector. The standard CompactPCI connector supports up to 250 insertion-removal operations, which is important for telecommunications and industrial applications.

The first step in designing a CompactPCI board involves creating a connector for the schematic-capture package being used. Detailed pin assignments are available from the CompactPCI Specification, which can be obtained from the PCI Industrial Computers Manufacturers Group (617-224-1100). Using a schematic capture program, replace the desktop connector with the CompactPCI connector. The remaining step involves adding some termination resistors to the bused PCI signals.

After the connector has been added to the schematic, termination resistors must be incorporated into the design. Adding a stub terminator to all bused PCI signals on the board is one of the features that allows CompactPCI to accommodate eight slots in a backplane. A 10-W resistor needs to be placed in series with the signal immediately adjacent to the connector to isolate the trace stub from the PCI bus. In this fashion, a distributed ter-

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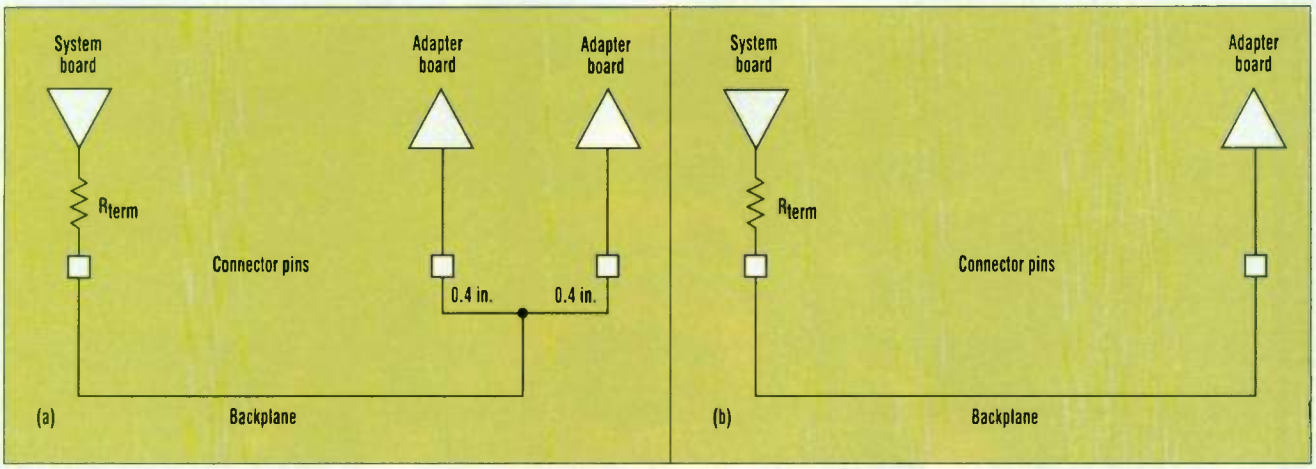

3. The system slot on a CompactPCI backplane drives five buffered clocks. To minimize the effect of clock sharing, the clock connection for peripheral slots 2-3 and 4-5 must be physically connected (a). Slots 6-8 have a direct connection from the system slot (b).

mination is applied to the PCI signaling environment that helps reduce signal ringing noise while not adversely affecting signal timing. For best results,the resistor should be placed within 0.5 in. of the connector.

Designing a CompactPCI board using a specification chip set also is a relatively straightforward process. Most chip-set manufacturers provide a sample schematic, typically in ORCAD format. This schematic will likely include an interface between the back-end design and a desktop PCI connector. Again, the key process involves replacing the desktop connector with the CompactPCI connector, and placing the termination resistors on the necessary bused signals as traces are routed to the connector.

Designing a board from scratch involves more choices and considerations than the two methods described above. The first decision involves choosing between programmable logic devices (PLDs), field-programmable gate arrays (FPGAs), ASICs, or off-the-shelf generic chips. In all cases, it is important to use devices whose I/O buffers are PCI-compliant and meet the PCI timing requirements.

Designing with PLDs is the most expensive, yet most flexible method for creating a CompactPCI board. A typical PLD can replace anywhere from a few to a few dozen fixed-function devices, depending on the application, and though expensive, requires much less of an up-front cost than an ASIC design. Because PCI interfaces are limited to one load on each PCI signal per board, all of the logic for implementing the PCI interface must be contained in one IC. You must take a hard look at how much logic will be needed to implement the PCI interface and how much is left over for the back-end interface.

The Programmable Logic Array (PLA) architecture that is at the heart of a typical PLD design has a limited flexibility and expandability. PLDs have limited flip-flop availability, which constrains the implementation of required PCI registers for Plug and Play operations. In addition, implementing required features of PCI, such as parity calculation, results in the use of large portions of a typical PLD's resources, leaving less for the real application. Designers looking for an alternative to a PLD that provides more functionality in one programmable device often turn to FPGAs. These are distinguished from PLDs by their use of a finer-grain architecture (lower level logic blocks), and by their requirement for completely different implementation strategies (one-hot state encoding, for example). Specifically, FPGA's are composed of uncommitted device resources that must be selected, configured, and interconnected. PLDs don't require the interconnections process, which allows potentially faster operation at the expense of flexibility.

One other important design rule to mention is the proper routing of signals on the board.

An ASIC offers the most rigid design choice, but the least expensive in terms of component cost, especially if the ASIC is produced in high volumes. It's the most rigid approach because making changes to the design involves a long lead time to fabricate a new device. During the development phase, comprehensive simulation of the logic is necessary to ensure proper operation before committing the design to silicon. The design techniques used to develop an ASIC are different than PLD or FPGA implementations, although they are converging.

An ASIC's lengthy development process and its high, nonrecrurring engineering (NRE) costs often preclude its use. ASIC vendors are in tune with the PCI market, however, and often provide soft cores (existing implementations) that can be used as a stepping off point to a new design.

The use of generic PCI bridge chips represents a middle-ground design choice. These devices are more flexible and more expensive than an ASIC, but less flexible and less expensive than a PLD or FPGA. These bridge chips make it easier to interface a design to the PCI bus, but still involve a certain level of back-end (application-logic) design. Generic PCI interfaces are available from such vendors as AMCC, PLX and V3. Most interfaces are oriented to a particular back-end architecture, such as Intel's i960 bus.

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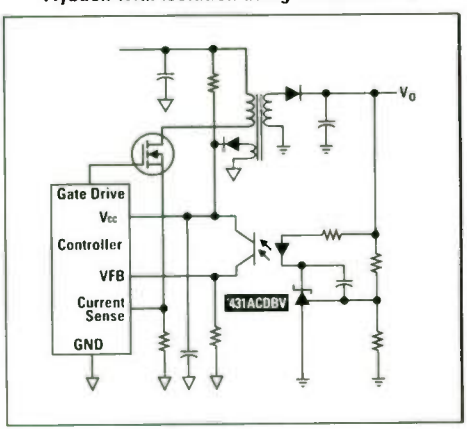

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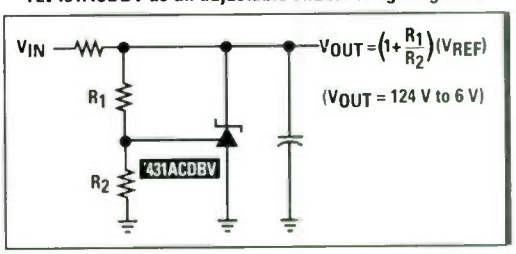

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When designing a CompactPCI board from scratch, care should be taken to use components with buffers that comply with the PCI Specification Revision 2.1. Because of the PCI bus' reflective wave technology, failing to use PCI-compliant buffers could cause the board to operate improperly at the maximum bus speed (33 MHz). Most programmable-device vendors offer parts with integrated PCI-compliant buffers.

It's important for designers to utilize the Delayed Transaction Termination Protocol as defined in Revision 2.1 of the specification. This is used by devices that can't complete the initial data phase of a read cycle within a reasonable number of clock cycles. Delayed transactions allow a target device to latch the read request from the bus and terminate the cycle, allowing bus bandwidth to be used by other PCI agents. The target device then obtains the data from its back-end function so that when the master that originally requested the data comes back to complete the request, the data is ready. Also be sure that the chosen programmable device supports delayed transactions.

Once the device logic is implemented, the rest of the design is similar to implementing a reference design as described above. If field-programmable logic is used, then it's desirable to choose an architecture that's in-circuit programmable to allow easy changes during the debugging phase.

One other important design rule to mention is the proper routing of signals on the board. The clock signal must be routed exactly 2.5 in. ± 0.1 in. between the connector and the PCI device and 32-bit signals must be routed no longer than 1.5 in., with 64-bit signal additions being no longer than 2.5 in. All signals should be routed with an impedance of 65 W.

Jim Medeiros is CompactPCI Section Manager at Ziatech Corp. He holds a BS degree from California Polytechnic State University, San Luis Obispo, Calif.

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UPDATE ON BUSES

Think The VMEbus Is Too Slow? Think Again. Try 320 Mbytes/s On For Size.

Do thoughts of the VMEbus conjure up images of a slow, but steady bus, plodding along at 80 Mbytes/s? The VMEbus has been a fairly stable bus for many years, unlike most buses in the computer industry. Well, if all goes according to plan, the tortoise soon will be transformed into the hare, right in front of your very eyes. Called VME320, the new backplane technology offers a 4X speed improvement over today's VMEbus, from 80 to 320 Mbytes/s. A 160-Mbyte/s version, appropriately called VME160, should appear as well.

VME320 will initially be an enabling technology for the telecommunications and military markets. The first interface ICs are scheduled to arrive in the early part of next year, thereby enabling board manufacturers to roll-out their compatible products.

The technology was invented by the designers at Arizona Digital, Scottsdale, Ariz. It's since been licensed to Bustronic Corp., Fremont, Calif., which is developing the initial backplanes. Bustronic, in turn, will sublicense the design to interested backplane manufacturers. Board manufacturers are free to develop VME320-compliant boards without having to pay any licensing fees or royalties.

Fred Hirsch, General Manager of Bustronic Corp., says, "The VME320 design is no more expensive to manufacture than conventional VMEbus backplanes. So why would anyone want to employ the old design?"

With a formidable competitor like Compact PCI staring right in the face of the VMEbus manufacturers, a potential upgrade like VME320 is welcome in the VMEbus community. Compact PCI runs at 132 Mbytes/s at 32 bits and 264 Mbyte/s at 64 bits.

According to Ray Alderman, Executive Director of VITA, the VMEbus' governing body, "The VMEbus will get a 4X speed improvement, akin to the silver bullet. We are showing it at 320 Mbytes/s, but we know that it can go a lot faster than that."

One of the beauties of the VME320 technique is that it is backward-compatible with existing VMEbus technologies. This means that both conventional VMEbus and VME320 boards can simultaneously reside in the same backplane. It employs a synchronous protocol that takes advantage of the VME320's high-performance backplane technology. Alternatively, conventional VME employs a fully interlocked protocol for all transfers across the bus. Although this is a reliable technique, it introduces some long delays. One data transfer requires four times the propagation time of the bus, plus four times the logic delays, in addition to the setup and hold times.

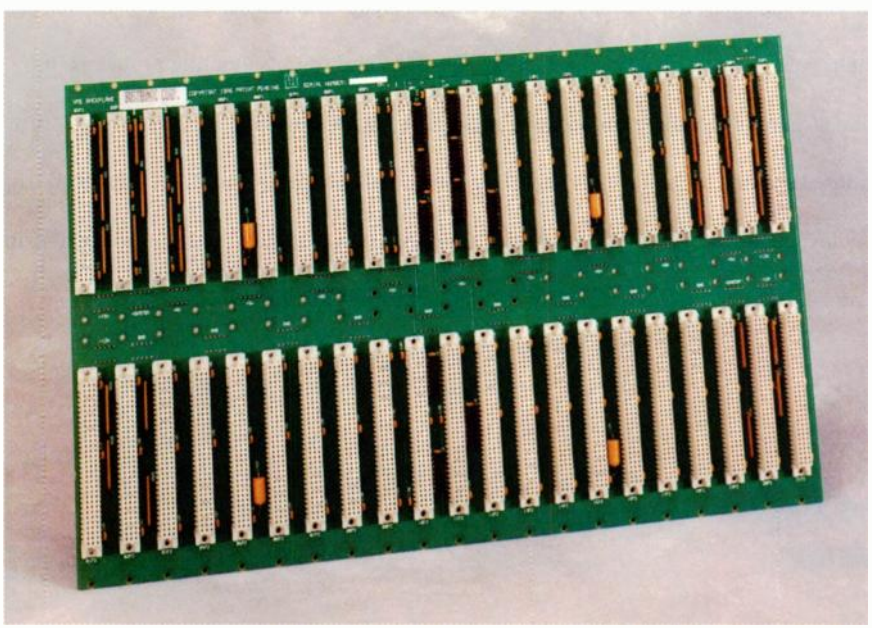
It's in the backplane where most of the VME320 innovation has occurred *(see the figure)*. The VME320 protocol employs the efficient initial steps of the conventional VMEbus protocol, except that it sends the data without waiting for an acknowledgment. This technique is known as Source Synchronous Transfer (SST), and it can also be employed on the VME320 backplane because the clean waveforms allow first incident wave switching.

Using only the negative-going edges, the new protocol applies two data strobes (DS0 and DS1) to drive data along the bus. Each data strobe is driven every other cycle when the data is quiet. Once the strobes are received by their designations, they combine into one strobe on the receiving board. The net result is that the bandwidth required by the signal lines carrying the data strobes is the same as the lines carrying the data. The data strobes use only the negative edges of the signals, which have been proven over time to be well controlled.

Another feature of VME320 is that it defines the DTACK* line as coded so as to prevent overrunning the receiver. A second benefit of this technique is that it ensures that the data is not going to a nonexistent destination. By holding the DTACK* line low, the sending board can stream data out as fast as it wants. When the sending board sees the DTACK* line pulled high, it reads this signal as the FIFOs on the receiving board are getting full, and adjusts accordingly.

For more information about the forthcoming VME320 technology, contact Bustronic Corp. at (510) 490-7388, or visit the company's web site on the Internet at http://www.bustronic.com.

RICHARD NASS



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WHAT'S ON BOARD

Supporting both the Ultra ATA and ATAPI-4 (IDE) standard interfaces, the ATEC378 storage controller chip developed by QLogic Corp., Costa Mesa, Calif., is targeted for fixed and removable hard-disk-drive manufacturers. The chip incorporates the company's headerless controller technology and the ability to tie into systems that employ magneto-resistive (MR) heads. Format-compatible with the company's previously-released ATEC336 triple-embedded IDE controller, the ATEC378 is largely firmware-compatible with the company's TEC376 and 386 SCSI controllers, and provides exact disk format and ECC compatibility. This allows system manufacturers to offer both SCSI and IDE versions of their products while minimizing code-development time. Internally, the ATEC378 combines a disk-format controller, a buffer controller, and a host ATA bus processor/controller. The chip exceeds all ATA and ATA-2 bus specifications for advanced PIO timing modes 3 and 4, and meets the specifications for multiword DMA timing modes 1, 2, and 3. ATA bus transfer rates range from 16.6 Mbytes/s in the PIO mode to 33 Mbytes/s in the DMA mode. ATAPI support is included to handle packet commands that support removable media applications. The disk formatter provides an 8-bit parallel NRZ disk interface that handles data rates of up to 20 Mbytes/s, while ECC includes programmable Reed-Solomon coding with selectable 144- or 192-bit ECC data field protection. The ATEC378 comes in a 128-lead PQFP and sells for under $9 apiece in large OEM quantities. Contact Dave Tovey at (714) 438-2200.

The Windows CE operating system from Microsoft Corp., Redmond, Wash., now supports the CompactFlash (CF) small-format storage card for use as a removable flash data storage media. Support for the CF format gives system users access to ATA-compatible memory cards with 20-Mybte capacities. The CF format allows system manufacturers to minimize the initial system cost by supplying the system with a minimal amount of memory, and allowing the user to upgrade as needed. Because the CF cards have ATA compatibility, they can be used in many digital cameras to readily transfer captured images between the camera and the CE platforms. Contact Nelson Chan at (408) 542-0456.

A two-chip solution for Windows CE platforms and other portable information appliances, the PR31500 CPU and UCB1100 analog chip from Philips Semiconductors, Sunnyvale, Calif., incorporates a software fax/modem capability thanks to the MIPS R3000-based CPU, which incorporates a multiplier-accumulator. The CPU chip includes an IrDA interface, a high-speed serial port, and support for two PC Card slots and for color and monochrome touchscreen LCD panels. The chip set, available in production quantities, reduces system size and power consumption, while trimming system cost and complexity. The soft-modem algorithms are executed on the CPU thanks to an on-chip multiplier-accumulator that supports the DSP computations needed for the modem function. Incorporating all the digital-to-analog and analog-to-digital converters needed for the touch-screen interface and audio/modem functions, the UCB1100 can be directly connected to a microphone and speaker. The chip set sells for $39/set in 100,000-unit quantities. Contact Philips at (408) 991-2000.

Geared toward motor-, industrial-, and instrumentation-control applications, the TMP95C063F, a 16-bit microcontroller from Toshiba America Electronic Components Inc., Irvine, Calif., packs an array of timers and a full DRAM controller to handle a large address space. The DRAM controller simplifies system design and eliminates separate controller chips and costly SRAM. Eleven timers are included—one watchdog timer, two 16-bit timers and eight 8-bit timers—to support applications that require multiple simultaneous events to be independently monitored. Other features include a 10-bit analog-to-digital converter, an 8-bit digital-to-analog converter, dual serial ports, 91 I/O pins, and two pattern-generator channels. The ROMless and RAMless controller comes in a 144-lead PQFP and consumes about 50 mA when running from a 5-V supply and clocked at 25 MHz. In100,000-unit lots, the TMP95C063F sells for $9.50 apiece. Contact Bob Salem at (714) 455-2000.

Pentium Pro Board Ups Performance With i960 RD

An Intel i960 RD I/O processor, combined with a pair of Pentium Pro microprocessors, is designed to improve throughput on the M6DPd system board. The I2O-ready board is built with the 440FX PCIset and supports a 64-bit graphics accelerator in addition to Adaptec's Ultra Wide SCSI and RAIDport architectures. Pentium speeds can run anywhere from 166 to 200 MHz. The i960 RD allows for multiple functions to be handled in the I/O subsystem, freeing the host COUs for applications processing. Designed to adhere to the standard AT form factor, the M6DPd supports both Fast Page Mode (FPM), and Extended Data Output (EDO) DRAM types, and also includes error checking and correcting with parity memory.

Micronics Computers Inc., 45365 Northport Loop West, Fremont, CA 94538; (510) 651-2300; http://www.micronics.com.

CIRCLE 568

RS-485/422 Card Offers True Isolation

The Ultra-SIO is a two-channel serial I/O adapter for PCs that supplies two RS-485/422 DOS-, Windows-, or OS/2-compatible serial ports. Each of the two ports can be connected to as many as 32 RS-485 devices. The ports offer true optical isolation, eliminating the effects of ground loop current and other transient spikes. Ground loop current could eventually result in data errors or possibly device corruption. The ports are viewed by the host system as a standard COM port. An auto-initialization feature thus enables the board's line driver during character transmission and then disables the driver. This feature allows for the RS-485 line to be managed transparently without any user or software intervention, and also eliminates the effects of RS-485 network contention. Currently available, the Ultra-SIO sells for $289. Also available is a nonisolated version that is offered at a price of $239.

Sealevel Systems Inc., P.O. Box 830, 155 Technology Place, Liberty, SC 29657; (864) 843-4343; http://www.sealevel.com.

CIRCLE 569

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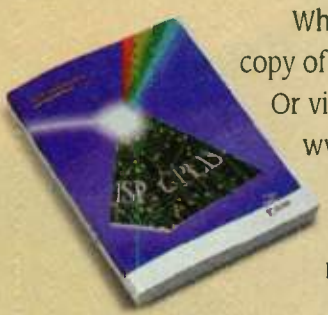

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PRODUCT FEATURE

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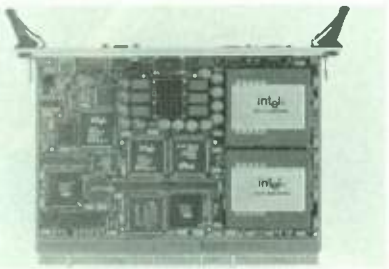
CompactPCI Board Holds Two Pentium Pro CPUs And Still Maintains 6U Form Factor

In the bus-board industry, one of the buzzwords that's in vogue is "CompactPCI." This fairly new specification is starting to gain momentum in terms of product releases. CompactPCI is an extension of the PCI local-bus standard that's been enhanced to support more slots in a more rugged environment. One example of this is the ZT 5520, a dual Pentium Pro board that holds a pair of microprocessors while maintaining a single-board 6U form factor. Each processor is cooled by an integrated heat sink and fan.



When two processors are employed, the board operates in a symmetric-multiprocessing mode, and complies with Intel's multiprocessor specification.

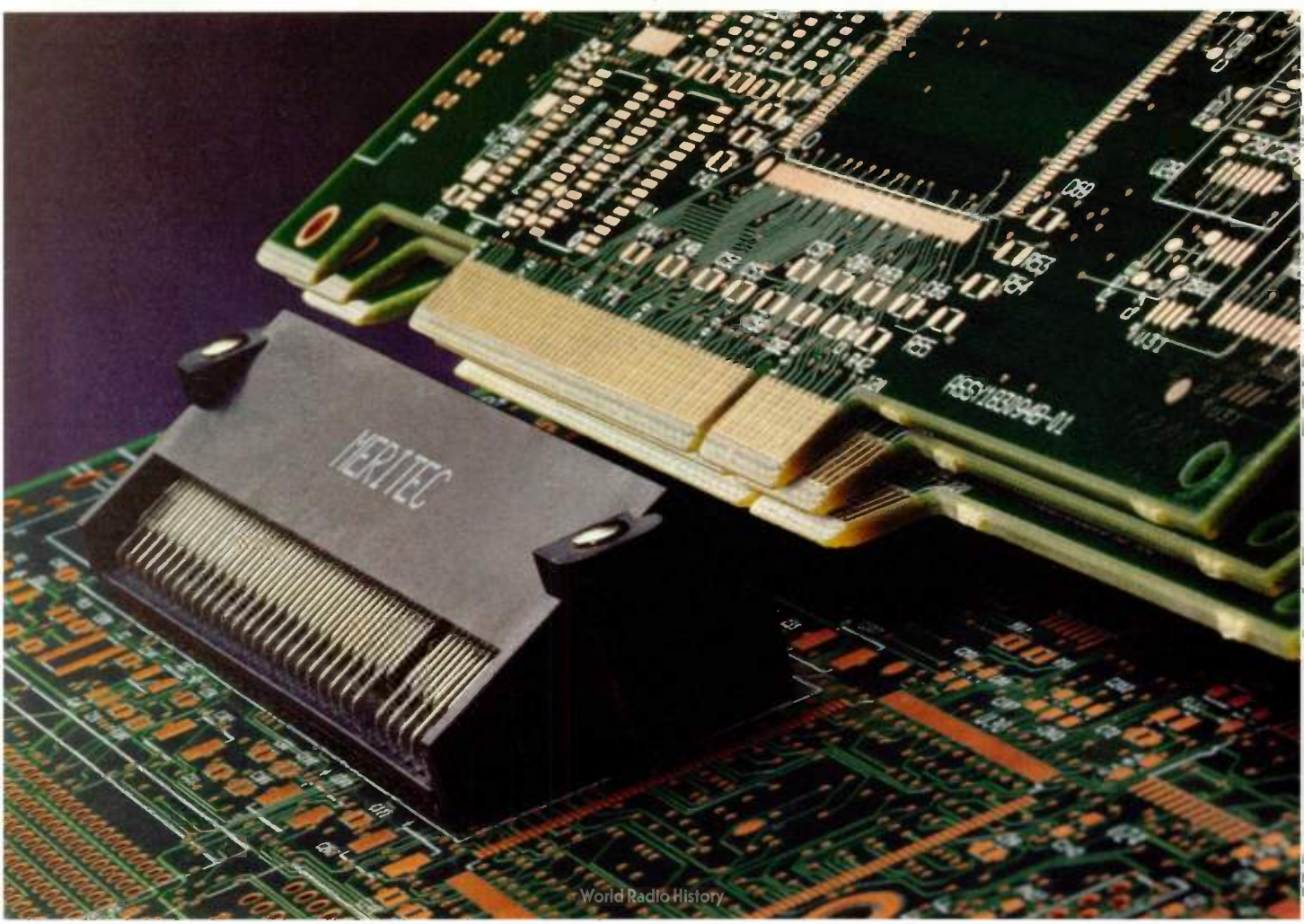
The ZT 5520 is built with Intel's 440FX chip set, which provides a direct connection to the PCI bus, as well as high-performance memory and I/O interfaces. Two complete 33-MHz CompactPCI buses are supported on both the bottom (J1 and J2) and top (J4 and J5) connectors. As a result, the board can drive up to 14 CompactPCI peripherals without an external bridge board. A third connector (J3) supplies rear-panel connection for I/O.

On-board features of the ZT 5520 include Enhanced IDE, a floppy-disk controller, Universal Serial Bus (USB), a parallel and two serial ports, up to 128 Mbytes of DRAM, and 8 Mbytes of flash memory (enough to hold MS-DOS, making the board compatible with PC-based software). Up to 32 Mbytes of flash can be connected through an expansion board.

The ZT5520 comes standard with the company's BIOS and MS-DOS boot files loaded in flash memory. The BIOS is user configurable to boot an operating system residing in local memory, from a fixed or floppy drive, or over a network. Support is included for Windows 95, Windows NT, QNX, and VxWorks.

Available later in the quarter, the ZT 5520 Pentium Pro CompactPCI board sells for $3850 with one Pentium Pro microprocessor and 16 Mbytes of DRAM.

Ziatech Corp.
1050 Southwood Dr.
San Luis Obispo, CA 93401
(805) 541-0488
http://www.ziatech.com
CIRCLE 564
RICHARD NASS



PRODUCT FEATURE

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PC Card Reads Smart Cards To Enable Digital Video Broadcasts

With the expected boom in digital video broadcasting (DVB), time-to-market and system integration will be critical in determining success or failure for manufacturers of DVB set-top boxes and TV sets. To that end, SCM Microsystems developed the DVB Conditional Access module (DVB-CAM), which controls the access the the set-top box that's needed to access the digital-video broadcast.

The DVB-CAM is an all-in-one PC Card that reads a smart card. It then determines, based on the information on that smart card, whether the viewer should have access to a given content provider's service. If the viewer is authorized for access, the module descambles the signal for viewing.

The DVB-CAM complies with the DVB Common Interface (DVB CI) standard, which is widely accepted in Europe. The DVB CI is actually a PC Card interface that bridges a DVB decoder with a CAM to provide descrambling and conditional-access functions.

The DVB-CAM provides a secure device that can be customized for use either as part of a set-top box or a PC. It also can be integrated directly into the television. This would lower the cost by removing some of the packaging limitations required by an external end-user device.

In practice, the DVB-CAM is basically a smart-card reader. Users would receive cards from the content providers, which would then "unlock" their systems to receive a particular broadcast. The device enables such functions as video-on-demand, pay-per-view, interactive video, home shopping and banking, and interactive gaming. Industry projections estimate that 30 million units will be sold in Europe over the next ten years, either as set-top boxes or as an integrated package within the television.

To further help OEMs integrate the DVB technology, SCM Microsystems is offering its CI Test Tool, which supplies a verification system to determine whether a device conforms to the DVB CI hardware and software specifications. The Test Tool include such functions as simulation for an external conditional access module with transport, session, and application-layer protocols as defined in the DVB standard. There's also a DVB interface CI command bus spy between a terminal and a module.

SCM Microsystems Inc.
131 Albright Way, Suite B
Los Gatos, CA 95030
(408) 370-4888
http://www.scmmicro.com
CIRCLE 565
RICHARD NASS

PRODUCT FEATURE

Data sheets on products like these can be found at www.penton.com/ed/

3D Audio Accelerator Connects To PCI Local Bus

Today's PCs ship with a PCI local bus as a standard feature, not as an option. So when designing some functionality into the PC, it makes sense to take advantage of the bandwidth offered by PCI. Such is the case with audio technology. The CS4610 DSP Audio Accelerator, designed by Crystal Semiconductor Corp., supplies digital audio processing for wavetable synthesis, three-dimensional audio, and sample-rate conversion. On top of that, it connects to the motherboard through the PCI bus.

The CS4610, built with a specialized DSP core, is designed to handle streaming data, such as wavetable data. In addition to operating as a wavetable engine, it functions as a 3D audio processor and a hardware audio-sample mixer. It offers a 300-MIPS architecture and a sophisticated DMA engine. The part also integrates Dolby AC-3 hardware acceleration.

The chip's multichannel DMA capability makes it possible to process 64 independent data streams, ensuring that no data is lost. Although audio accelerators typically process less data than their video counterparts, it's a fairly acceptable practice to drop video frames. That's not the case with audio.

The CS4610 offers the ability to handle spatializing, or enhancement. This pushes the stereo effect further apart than the speakers are physically located, trying to wrap it around 180°. The stereo audio stream has a certain amount of width in terms of the listener's perception. This effect is being embraced by PC game developers, who are trying to give a more realistic effect to their games.

Another feature of the CS4610 is its digital serial audio output ports, which support surround sound. If the PC's motherboard holds a stereo codec, its designers can connect four digital-to-analog converters to the CS4610 and output surround-sound audio.

The part's PCI bus interface contains a pass-through mode to handle such applications as telegramming. In this configuration, the pass-though mode would be used to connect a modem to the audio accelerator. As a result, the modem enjoys a direct connection to the PCI bus, rather than the slower ISA bus.

The CS4610 DSP Audio Accelerator IC is housed in a 100-pin MQFP. In lots of 10,000, it sells for around $22. Production should begin in the third quarter.

Crystal Semiconductor Corp.
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CIRCLE 566
RICHARD NASS

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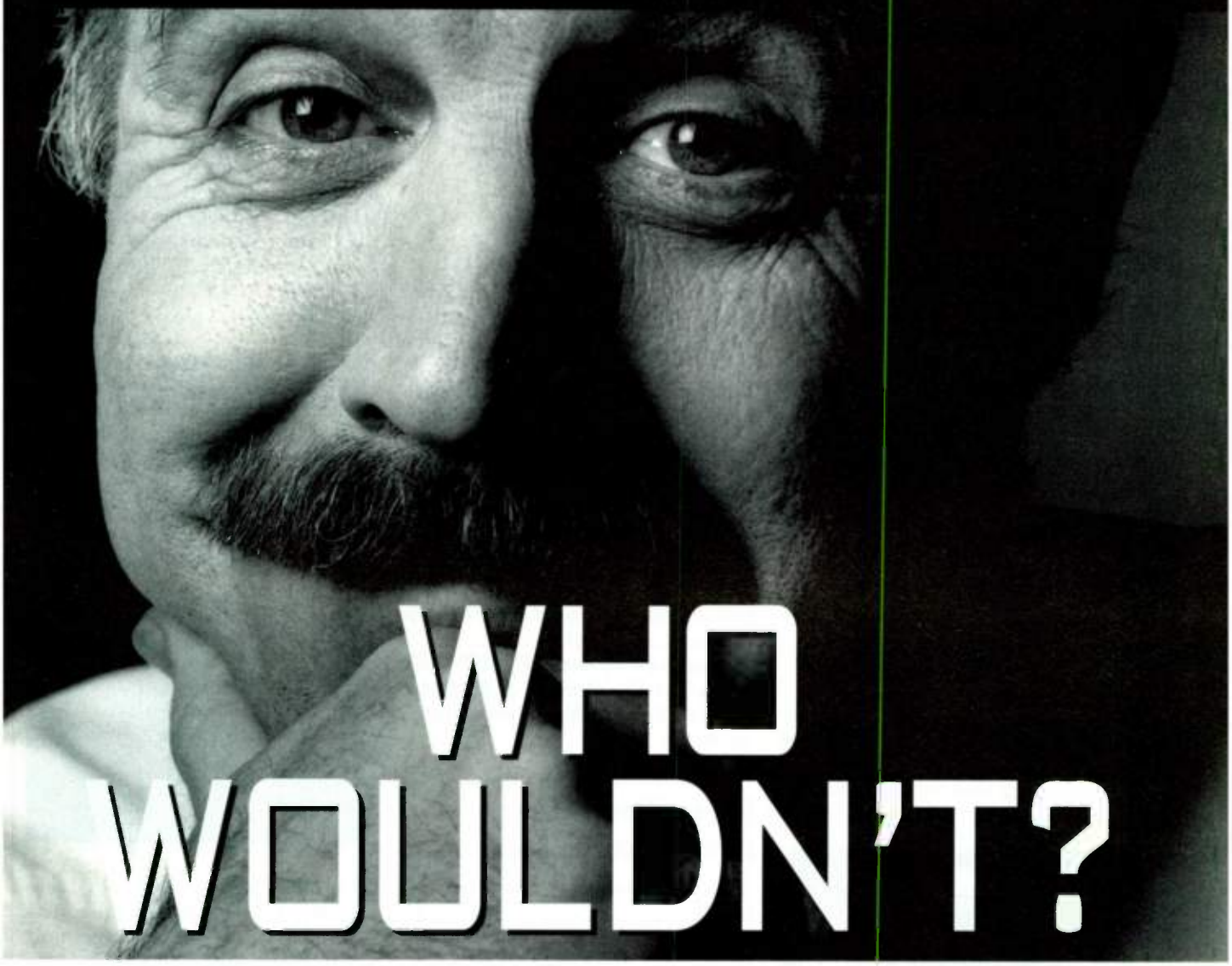

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WAN Controllers Offer Cost-Effective ISDN PRI

Built for the VMEbus architecture, the T1/E1 PRI ISDN Communications Controller is an intelligent, two-port T1/E1 serial interface for ISDN PRI that requires no external CSU/DSU. Offering cost-effective ISDN PRI and serial line communications, the board contains a 16-port high-density controller. Dubbed the PT-PCI370PQ, the board is based on Motorola's PowerPC MPU. According to the company, in real-world tests, the board maintains a sustained throughput of 2.048 Mbits/s full-duplex on each of its two channels. In addition, by relegating most of the ISDN communications processing to the controller, the host workstation or server operates more efficiently. While able to executing protocols directly, the board also can handle most of the low-level communications activities that typically would burden the host.

Performance Technologies Inc., *315 Science Parkway, Rochester, NY 14620; (716) 256-0200; http://www.pt.com.*

CIRCLE 570

Low-Cost Monitor Offers High-End Features

Designed for the growing population of business and home-office (SOHO) users, the V773 monitor employs a Super Contrast screen for sharp text and bright colors. The 17-in. monitor offers

a 15.8-in. viewable area. For both PC and Macintosh environments, the V773 is built with a flat-square screen that minimizes distortion. The 0.26-mm dot pitch results in crisp images, even at resolutions up to 1024 by 768 pixels at 86 Hz. An anti-glare, anti-static screen treatment makes viewing easier without compromising image quality. An on-screen menu is employed to control contrast, brightness, and color tuning. The V773 monitor, which exceeds MPR-II and EPA Energy Star requirements, will sell for $599.

ViewSonic Corp., *20480 Business Pkwy., Walnut, CA 91789; (909) 869-7976; http://www.viewsonic.com.*

CIRCLE 571

10.4-in. Touch Display Measures Just 1.36 in. Deep

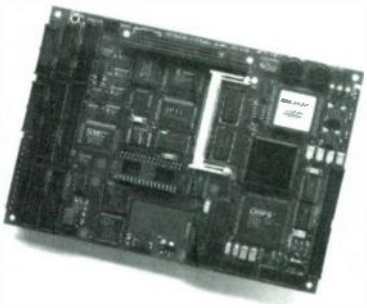
Measuring only 1.36 in. deep, the TruePoint SpaceSaver is a 10.4-in. active-matrix LCD capacitive touch monitor aimed at POS, industrial, and financial markets. Three mounting options are available—desktop, wall, and swivel. It's also designed with a special cable that combines the serial communications, video signals, and power. With a resolution of 640 by 480 pixels, the display can show up to 262,000 colors. Available immediately, the TruePoint SpaceSaver LCD flat-panel capacitive touch monitors is priced at $1945, with volume discounts offered.

MicroTouch Systems Inc., *300 Griffin Brook Park Dr., Mrthuen, MA 01844; (508) 659-9000; http://www.microtouch.com.*

CIRCLE 572

SBC Combines Higher Performance, Small Size

High performance in a small form factor is what's touted by the PC-510 single-board computer. In a 5.75-by 8-in. package, the board offers a 133-MHz 586 processor, six serial ports, a GPS interface, a graphics accelerator (that supports video), and 48 lines of digital I/O. Aimed at rugged mobile communications, data acquisition, and industrial-control applications, the board is available as a standard or semicustom embeddable card. Other features include up to 33 Mbytes of EDO DRAM, 2 Mbytes of video RAM, a PC/104 interface, a multifunction parallel port, floppy- and hard-disk interfaces, a 2-Mbyte flash-memory disk, and a real-time clock. In addition to the card's -40°C to



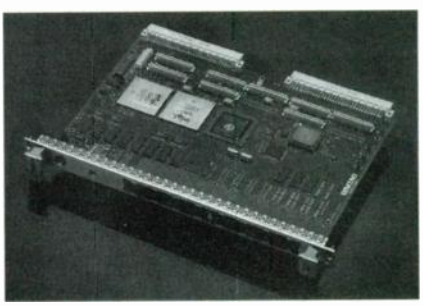
+70°C temperature range, the PC-510 can withstand 10 Gs of shock and 3 Gs of vibration. Available immediately, the board sells for $995.

Octagon Systems, *6510 W. 91st Ave., Westminster, CO 80030; (303) 430-1500.*

CIRCLE 573

PMC I/O Subsystem Supports VME, Raceway

Designed as building blocks for embedded systems, the Midas family combines PMC, RaceWay, and VME64 technology with dual processors and a swinging-buffer memory architecture. The basic configuration

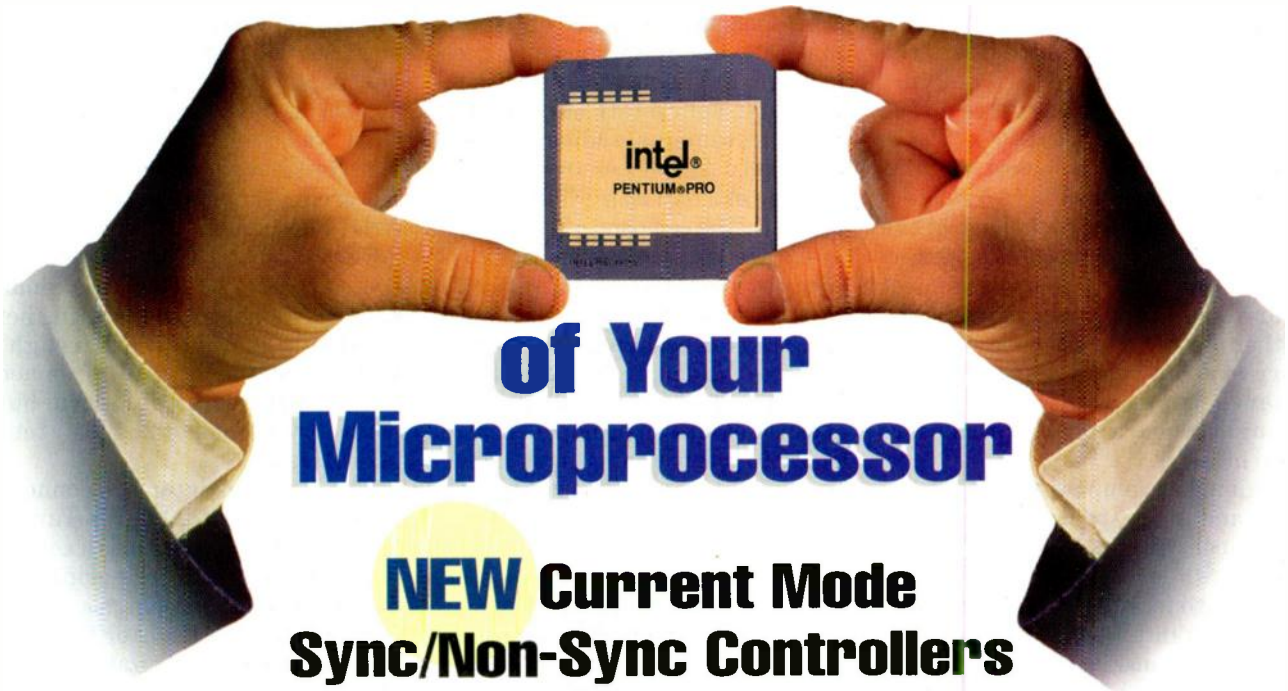


of the Midas board contains a PCI subsystem and two PMC modules. The symmetrical PMC arrangement places one module on either side of the board's i960RP processor. A single-chip PCI-to-RaceWay interface permits a continuous data rate of 120 Mbytes/s into the standard RaceWay crossbar interface. Suitable applications include medical diagnostics, seismic exploration, communications, and the military. With the board's VxWorks operating-system support, drivers from various vendors can be employed.

Vmetro Inc., *1880 Dairy Ashford, #535, Houston, TX 77077; (281) 584-0728; http://www.vmetro.com.*

CIRCLE 574

Take Control



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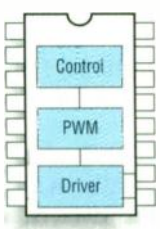

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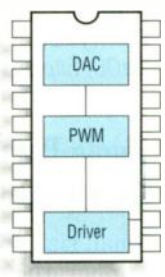
- Available in 16-lead SO package



Next Generation Processor EL7571C

- Direct drive up to 20A FETs
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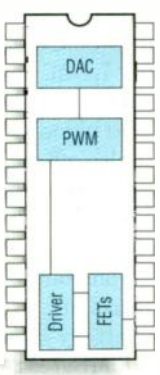

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SYSTEM DESIGN

Data sheets on products like these can be found at www.penton.com/ed/

Daughtercard Delivers 1.44 GFLOPS Of Performance

Designed for the SkyChannel-based multiprocessor architecture, the SharcPool daughtercard delivers 1.44 GFLOPS of performance. Based on the Analog Devices 2106x (Sharc) microprocessor, the board contains 12 CPUs configured in two clusters of six. The link ports in each of the clusters are configured as a bidirectional ring, plus two links connect corresponding processors in the other cluster. The three-level memory system offers a high-performance connection between the daughterboard's microprocessors and memory.

Aimed at compute-intensive signal- and image-processing applications, one card fits onto a 6U motherboard, while a 9U motherboard can hold up to four modules. The daughtercard's interface to the motherboard has a maximum throughput of 320 Mbytes/s. A host of development tools are available. The SharcPool high-performance daughterboard is priced at $23,250.

Sky Computers Inc., *27 Industrial Ave., Chelmsford, MA 01824; (508) 250-1920; http://www.sky.com.*

CIRCLE 575

Backplanes Comply With CompactPCI Specification

Offered in 3U and 6U form factors, a series of backplanes comply with the CompactPCI specification. CompactPCI is an adaptation of the PCI specification that's geared toward industrial applications. The specification is electrically identical to desktop PCI, but offers a more robust mechanical form factor.

The backplanes feature ten-layer stripline construction and support for 32- or 64-bit PCI transfers. They can handle boards operating at either 3.3 or 5 V and are available with or without on-board modular power-supply connectors. Initially, eight-slot versions of the CompactPCI backplanes are available. Prices start at $395.

Vero Electronics Inc., *5 Sterling Dr., Wallingford, CT 06492; (800) 642-VERO; http://www.vero-usa.com.*

CIRCLE 576

Flash Cards Support Miniature Card Standard

Don't look now, but some of the consumer devices you've become accostomed to are being stocked with removeable solid-state storahe. For example, cameras, audio recorders, and cellular telephones are taking advantage of a Miniature Card offered by AMD. The company offers 2.7- and 5.0-V card based on flash memory. The low-power cards are useful in such devices because of their rugged capabilities. They can be dropped and mishandled to some degree and still operate without a flaw. The Miniature Card doesn't require any complex control logic for implementation, and the connector is designed to be user-friendly and low cost. The Miniature Card is compatible with the standard set forth by the Minature card Implementers Forum. The card measures 33 by 38 by 3.5 mm, about one-fourth the size of a PC Card. Many capacities are offered. In lots of 10,000, the 2-Mbyte version sells for $30.

AMD, *One AMD Pl., P.O. Box 3453, Sunnyvale, CA 94088; (408) 732-2400; http://www.amd.com.*

CIRCLE 577

Single-Board Computer Suits Embedded Networks

Small size, low cost, wide operating temperature, AT compatibility, and connectivity are the basic element required for an embedded network platform. That's also a list of the features that are offered by the SAT-SXPlus expandable single-board computer (SBC). The 4.5- by 7.1-in. board combines a 40-MHz 386SX CPU with a solid-state disk, and video and Ethernet controllers. It also offers 24 digital I/O lines. Further expansion is handled through a PC/104 interface. Other features include seven DMA channels, three 16-bit counter-timers, two interrupt controllers, a keyboard controller, and a battery-backed real-time clock. Up to 8 Mbytes of DRAM are supported. With 2 Mbytes of DRAM, the SAT-SXPlus sells for $695.

WinSystems Inc., *715 Stadium Dr., Arlington, TX 76011; (817) 274-7553; http://www.winsystems.com.*

CIRCLE 578

CPU Boards Harness PowerPC Processors

One way of getting more processing power out of a CPU board is to double the number of processors that appear on the board. That's exactly what was done on the MVME4600 VMEbus board, developed by the Motorola Computer Group, Tempe, Ariz. The board contains a pair of PowerPC 604 microprocessors, connected to a 60-MHz bus. the combination is capable of transferring better than 400 Mbytes/s. Through a PCI bridge, the processors connect to a 33-MHz, 64-bit PCI local bus, where transfers of 264 Mbytes/s take place.

The VMEbus interface connects to the PCI bus through a Tundra Universe chip. There's also a connection to the ISA bus for peripherals that don't require the high speed offered by the VMEbus or PCI bus. Further board customization is handled though a series of PMC expansion slots. The base MVME4600 contains one slot, and one or two optional carrier board can be employed up add up to four additional PMC sites. Available now, the MVME4600 starts at $6900.

Also from Motorola is a small form factor board that features a PC/104+ expansion slot. PC/104+ is the version of PC/104 that supports the PCI local bus. As a result, it can handle transactions at a rate of 132 Mbytes/s. In addition, the board contains a PC Card connection. This lets end users handle the board's customization if they so choose. Powered by a PowerPC 860 microprocessor, the MBX860 board is aimed at real-time applications. For this reason, the board runs real-time operating systems from Wind River Systems, Microware, Integrated Systems, and Lynx Real-Time Systems.

The MBX860 PC/104+ card measures 8 by 5.75 in. The entry-level configuration is stocked with 4 Mbytes of DRAM, 2 Mbytes of flash memory, and 32 kbytes of nonvolatile RAM.

Motorola Computer Group, *2900 S. Diablo Way, Tempe, AZ 85282; (602) 437-6867.*

CIRCLE 579

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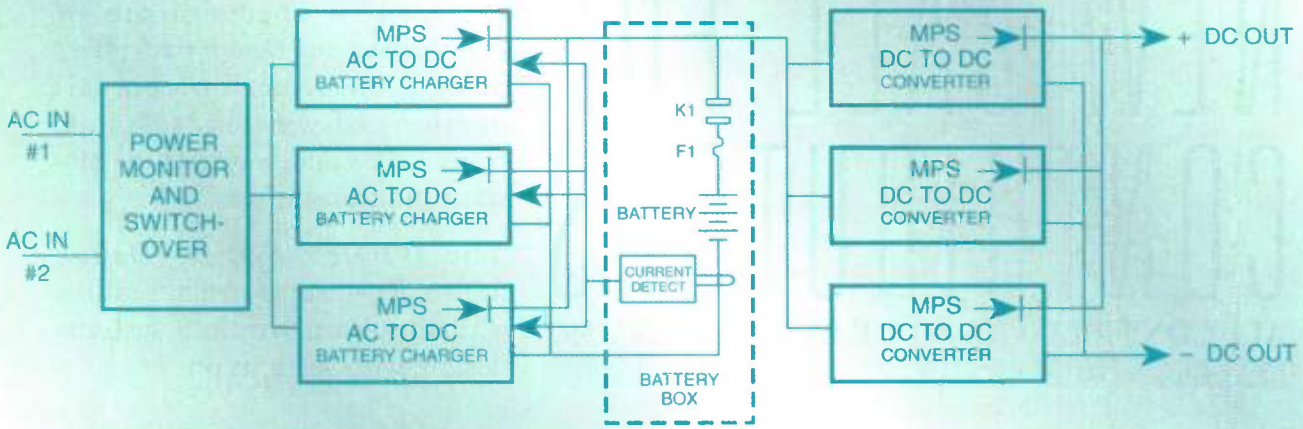

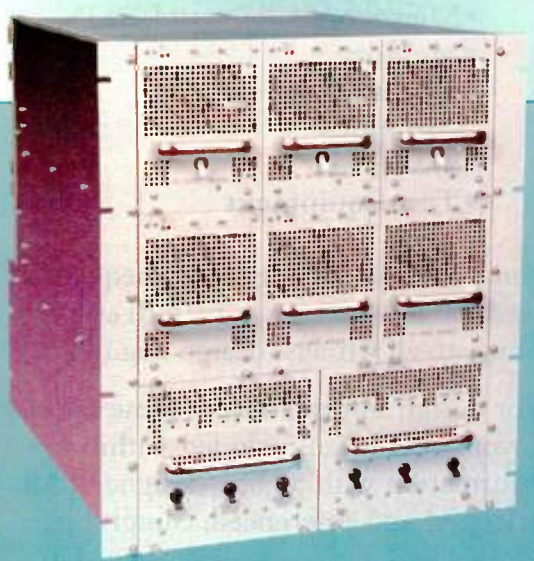

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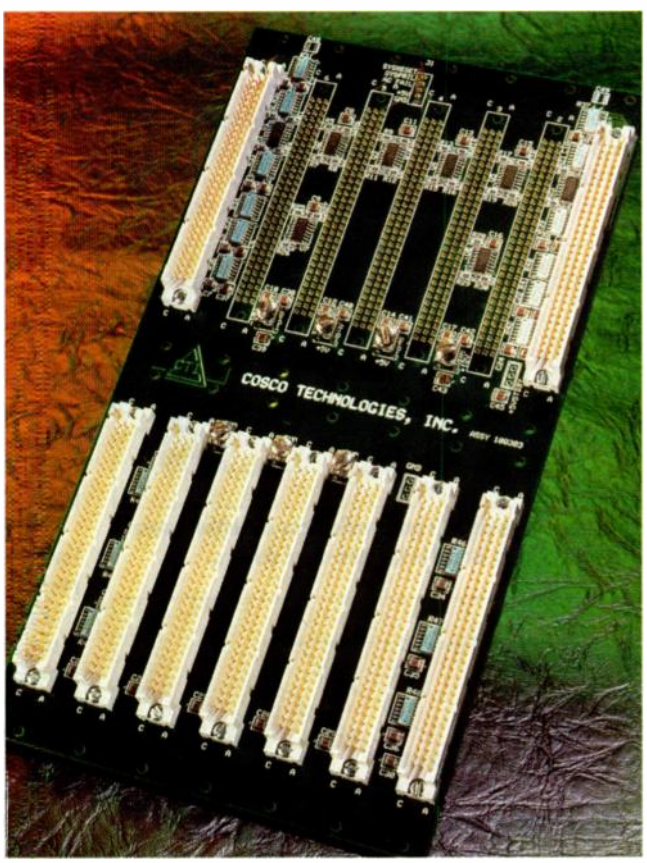
Design Considerations For High-Performance Backplanes

Although I/O Rates Keep Pushing The Envelope, Backplane Technology Is Staying Ahead Of The Game With Advances In Components, Fine-Line Traces, And Multilayer Construction.

Ray Cosimano
Cosco Technologies Inc., 140 Washington Ave., Endicott, NY 13761-7399; (607) 757-0633; fax (607) 757-0771.

No matter how advanced the computer system, optimum performance still depends heavily on the ability of the backplane to accurately and reliably move large amounts of data from one system board to another as quickly as possible. Specifically, the backplane is a critical component in the performance equation since advances in active silicon devices are not directly transferable to the backplane. Fortunately, advances in pc-board fabrication such as fine-line traces and multilayer construction, combined with the advent of inexpensive surface-mount devices, have vastly improved backplane performance and reliability, while keeping costs down.

Despite the technological improvements, backplanes remain as somewhat of a bottleneck in high-end applications as I/O rates spiral upward. For example, typical Category 5 twisted-pair runs at 100 Mbits/s; wide and fast SCSI maintains 40 Mbits/s data streams; and home PCs costing less than $2000 are running at 166 MHz and using PCI interfaces capable of 256 Mbits/s data transfers. This kind of performance is driven by the market place. The entertainment market needs high-resolution, full-motion video. The information systems market for large enterprises demands reliable high-speed information retrieval and storage, while the communications market requires high-bandwidth switches and routers. When choosing a backplane to meet the requirements of these applications, three primary factors must be considered—signal integrity, power distribution, and reliability.



1. Responsible for maintaining signal integrity as information is passed from board to board, the backplane is facing increasing performance pressures as data rates target 80 Mbytes/s and beyond.

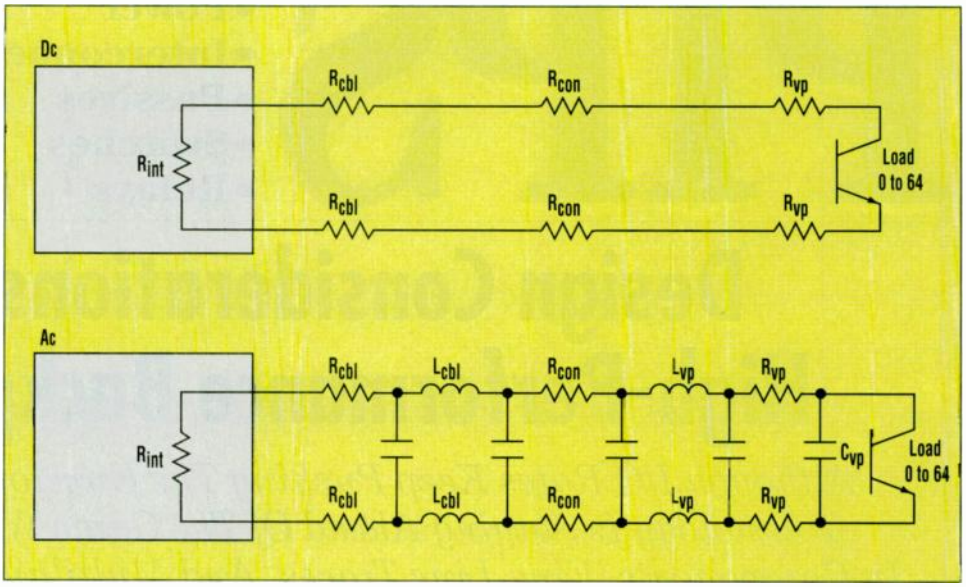
The backplane is responsible for maintaining signal integrity while accurately and quickly moving information, both digital and analog, from one system board to another (*Fig 1*). It also is responsible for maintaining accurate timing relationships between clock and data information as the signals propagate. Loss of signal integrity comes from three main sources—reflections, crosstalk, and propagation delays.

Reflections occur in backplanes when there is a change of impedance anywhere along the conductive path of the signal (*Fig. 2*). These changes in impedance can be caused by something as simple as a change in the thickness of a trace. The resulting reflections can either cause spurious negative effects such as

false "1s" or "0s," or aid in the turn-on of drivers, as in the case of reflective-wave switching used in VMEbus or PCI systems. In any case, strict adherence to the specification attached to the architecture in question is essential if unwanted reflections are to be avoided.

Crosstalk in backplanes can lead to false switching and intermittent operation and is mostly a capacitance coupling phenomenon (*Fig. 3*). As such, the crosstalk between signal lines can be approximated as being inversely proportional to the distance between the signal lines, and directly proportional to the distance between the signal lines and the ground plane.

One technique for reducing crosstalk is to use fine-line technology that increases the distance between signal lines while decreasing the distance between the signal line and reference plane. It has been shown that going from 12-mil lines to 5-mil lines can reduce crosstalk by up to 25%. Though once prohibitive, the cost of fine-line technology has decreased steadily over the last five years due to advances in etching technology combined with improved standards of cleanliness in the photo-etching and pc-board manufacturing process.



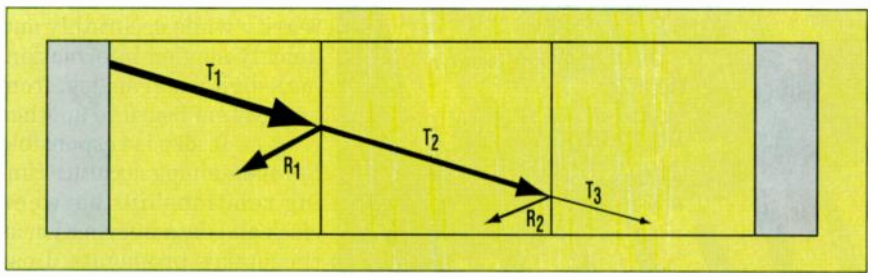
4. The equivalent circuit for the dc and ac modes of power distribution introduces the equivalent capacitance C_{VP} that is created by using plane pairs in the pc-board layout.

Propagation delays are not a problem if the timing relationships between clocks and signals are maintained. To maintain the timing, special attention must be paid to trace lengths and the difference in propagation due to signal lines running on the surface and those surrounded by epoxy glass structure. Uncertainty in the propagation time of data with respect to the clock could cause a "1" to be interpreted as a "0" or vice versa.

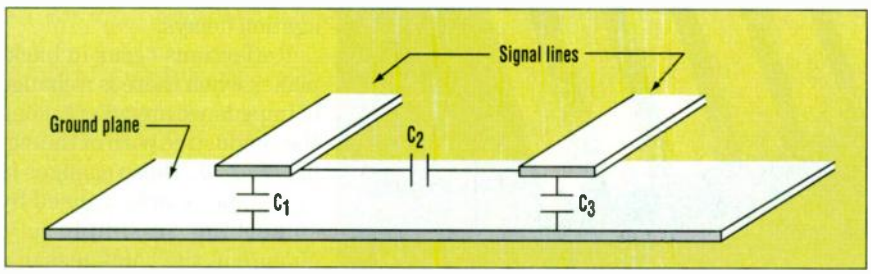
In most backplane systems, the power is supplied to the boards via the backplane. It is important that a low-resistance path is provided by the backplane to ensure that all boards in the system share the same reference with respect to the supply and ground. This reference also must be maintained under dynamic conditions. The equivalent circuits for the dc and ac modes of power distribution; depicted is a model of distributed capacitance (C_{vp}) that is created by using plane pairs in the pc-board lay-up (*Fig. 4*). This is a very effective stabilizing capacitance because of the low-inductance path to the load. The ground and power pairs are used to create a distributed capacitance to control the change in current created by simultaneous switching of lines on a 64- and 128-bit buses (*Fig. 5*). Surface-mount decoupling capacitors and terminators should be used because of their low-inductance leads.

High reliability with respect to the backplane is critical as any failure that requires the backplane to be replaced normally means the whole system must be dismantled. The probability of a backplane failure could be viewed as the sum of the probability of the pc-board failure, plus the probability of connector-system failure, and the probability of process-induced failures.

Pc-board failures can be minimized by maximizing the distance between conductors, minimizing the number of plated-through holes, minimizing the length of lines, avoiding sharp turns

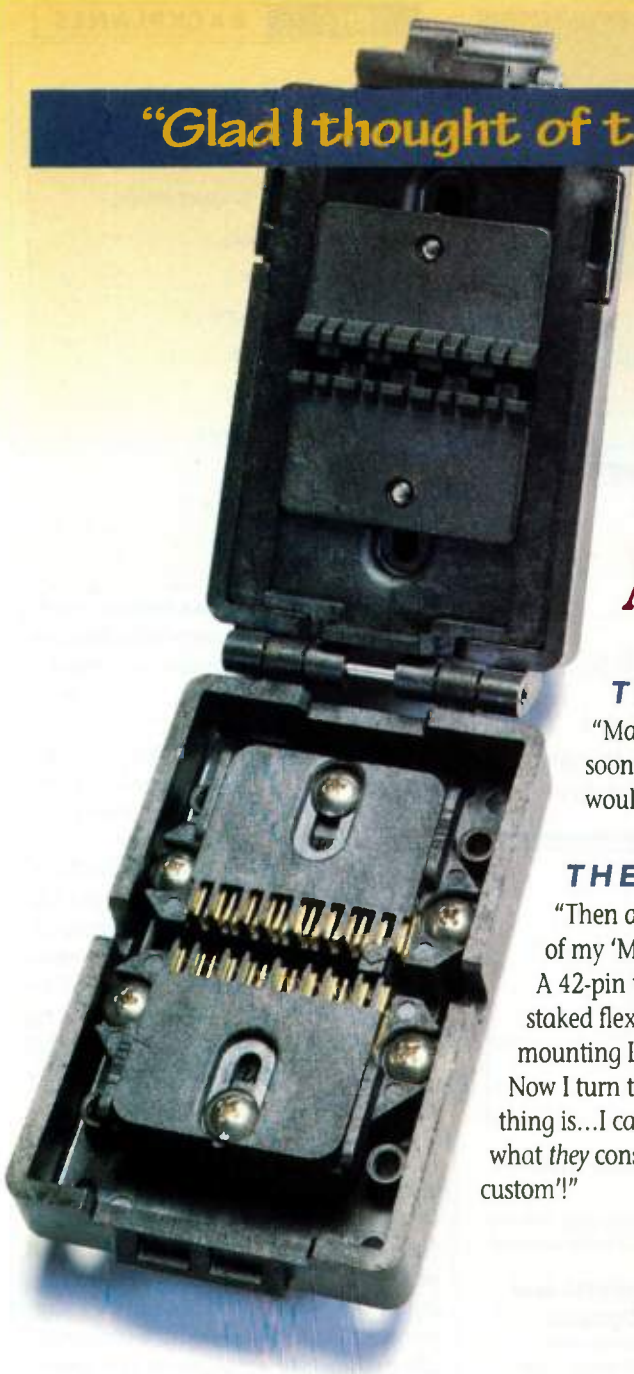


2. Caused by changes in impedance anywhere along a signal's path, reflections can either cause negative spurious effects such as false highs and lows, or aid in the turn-on of drivers.



3. Crosstalk between signal lines is mostly a capacitance coupling problem and can be approximated as being inversely proportional to the distance between the signal lines, and directly proportional to the distance between the signal lines and ground.

"Glad I thought of that!"



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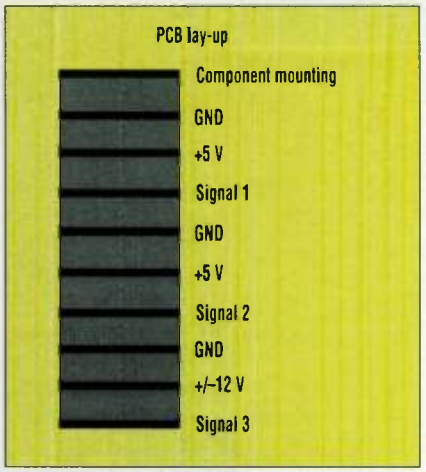

5. The distributed capacitance created by using ground and power pairs controls the change in current caused by simultaneous switching of of lines on 64- or 128-bit buses.

and square corners, and making sure that the line width specified in the design is matched with the process capability of the pc-board fabricator.

Connector reliability is a function of lubrication, wipe, normal force, plating integrity, and the number of contacts. Choosing a backplane system based on a two-piece connector system like VME or CompactPCI will go a long way toward optimizing wipe, normal force, and plating, because the epoxy glass is eliminated as a substrate for carrying one of the mating surfaces.

Processes used to assemble the backplane affect system reliability. Repeated exposure to large temperature changes can cause cracking of plated-through holes and overstressing of the assembly. This can be exaggerated if the temperature is applied after connector attachment because of the different thermal expansion characteristics between the connector material and the epoxy glass used in pc boards. Other common process-induced failures include contamination from fluxes and solders, as well as cold solder joints

Raymond J. Cosimano is president and founder of Cosco Technologies Inc. in Endicott, N.Y. He holds an AAS in Electrical Technology from Erie Community College in Buffalo, N.Y.

How Valuable	Circle
Highly	554
Moderately	555
Slightly	556

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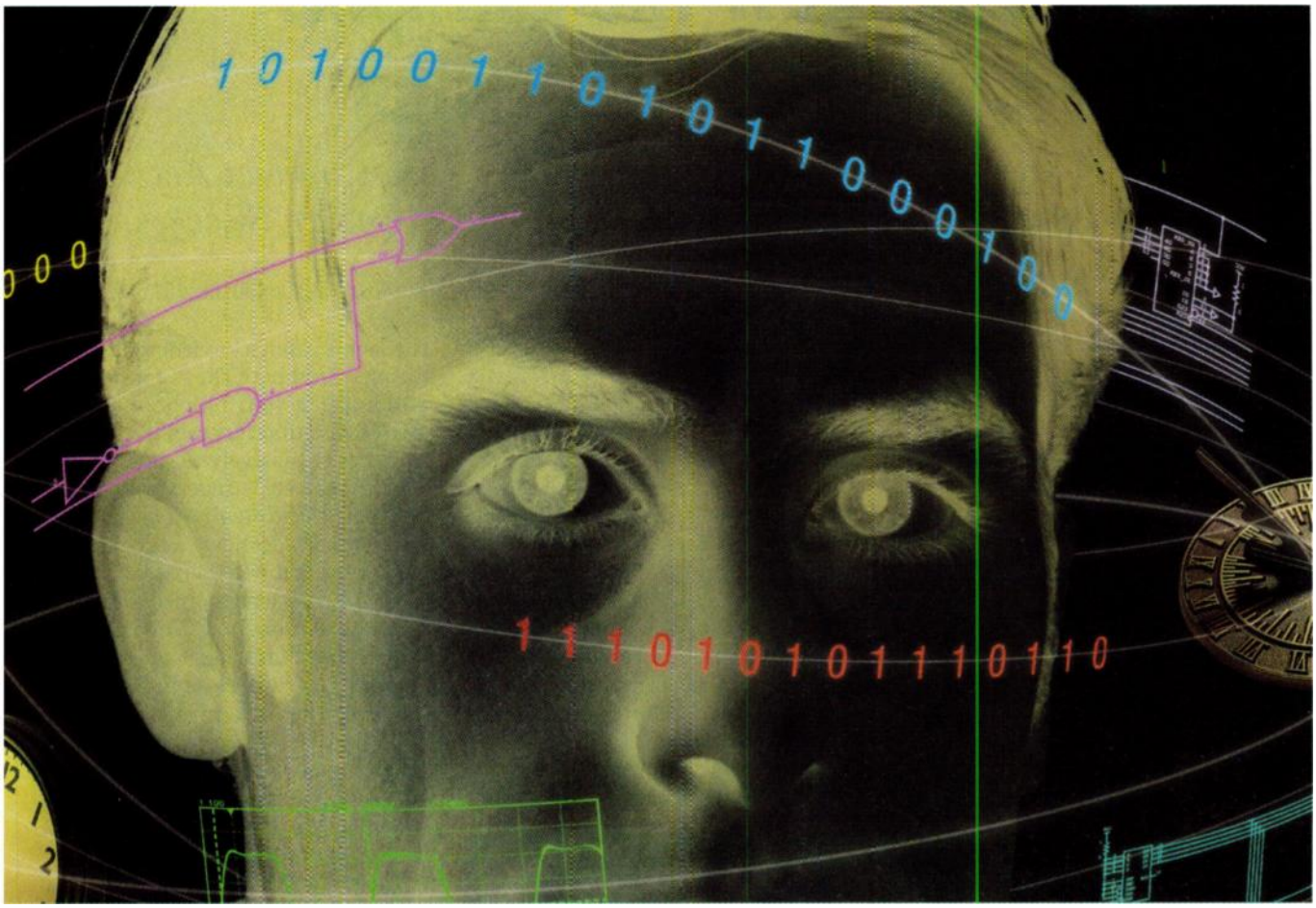

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Tektronix

Switches: The Linchpins Of A Good Design

Given Proper Foresight, The Lowly Switch Can Connect Actual With Perceived Quality—A Key Factor For Design Success.

PETER BROUILLETTE, C&K Components Inc., 57 Stanley Ave., Watertown, MA 02172-4802; (617) 926-6400; fax (617) 926-6846.

As design cycles shrink, many engineers are waiting until the last minute to select a switch suitable for their application. While this approach may work in some cases, it often leads to delays, cost overruns, and even design modifications. In addition, giving such short shrift to what is often the key interface between the user and the piece of equipment can not only compromise the actual quality of the item, but the perceived quality as well.

Seven key points to keep in mind to avoid program delays, and to improve customer satisfaction are:

Ergonomics should not be taken for granted. The look and feel of the switch reflects on the product in which it is being used. Actuation force, travel, and switch tactility are all factors that affect this. Visual feedback is also important. Toggle and rocker switches display actuator status well, while rotary and push-button switches require marking or illumination.

Environmental compatibility is essential. All too often, unsealed switches are specified for applications that require a sealed solution. One of the most common sources of failure in switch products is foreign substances in the contact area.

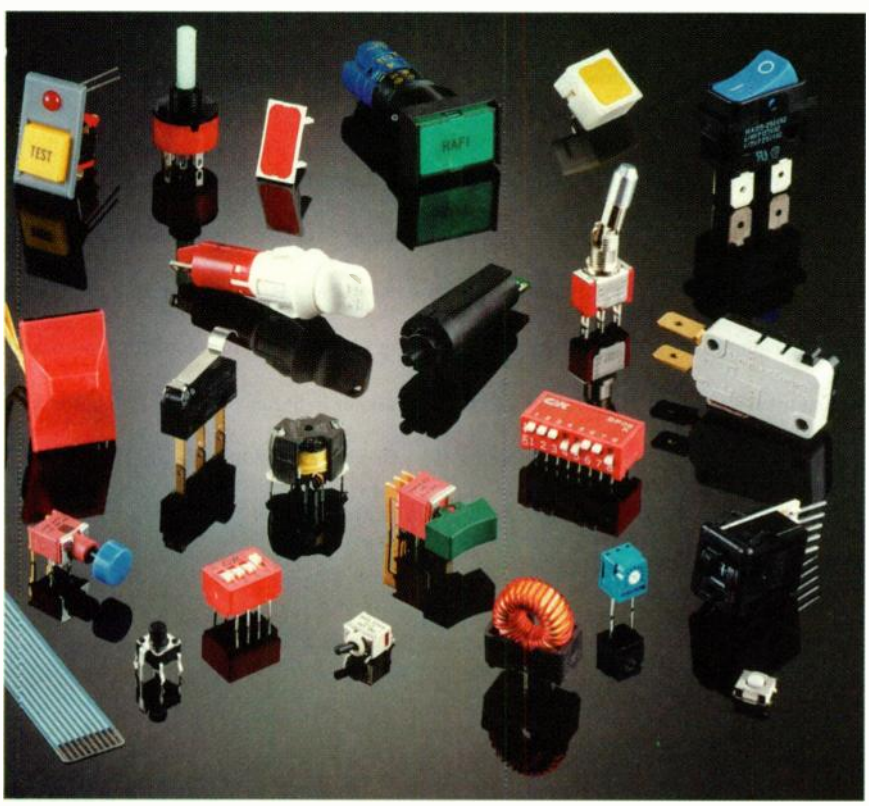
In addition, the designer should ensure that the manufacturer has tested the switch under environmental conditions similar to those found in the end application. The best-in-class switch manufacturers will test their switches extensively to simulate real-world, long-term usage of the product.

All pc-board-mounted switches are not equal. By acknowledging this fact, designers can avoid critical damage during the soldering process. Surface-mount switches must be manufactured from materials that can withstand temperatures as high as 260°C (high-temperature nylons and liquid-crystal polymers are recommended). Through-hole switches on a hybrid board also must be capable of withstanding the high temperatures. Testing for this tolerance is essential.

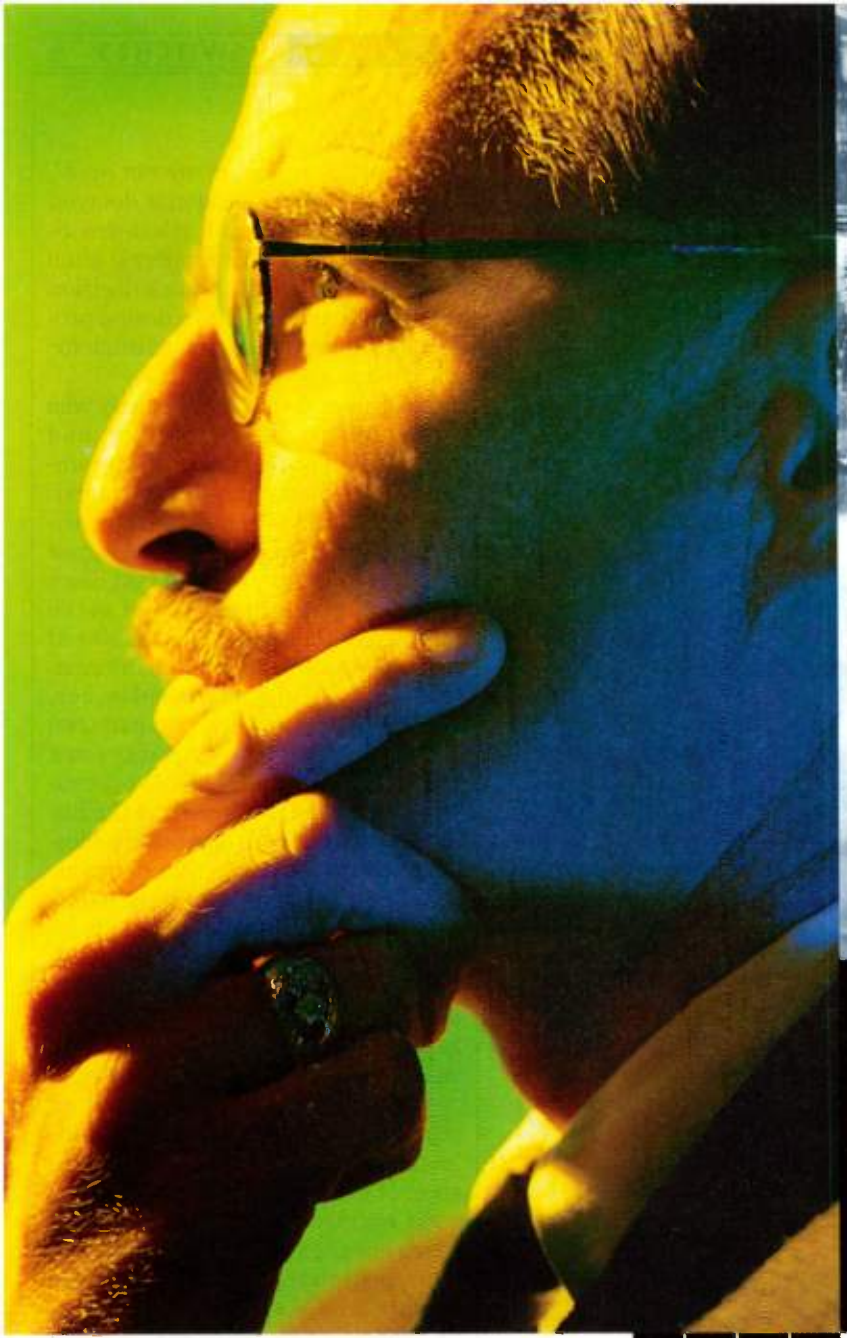
Electrical loads are critical considerations, if a switch is to perform to specification. Too often, in-rush currents are ignored with switches used to activate power supplies. Likewise, switches used for power applications are frequently misused in dry-circuit applications.

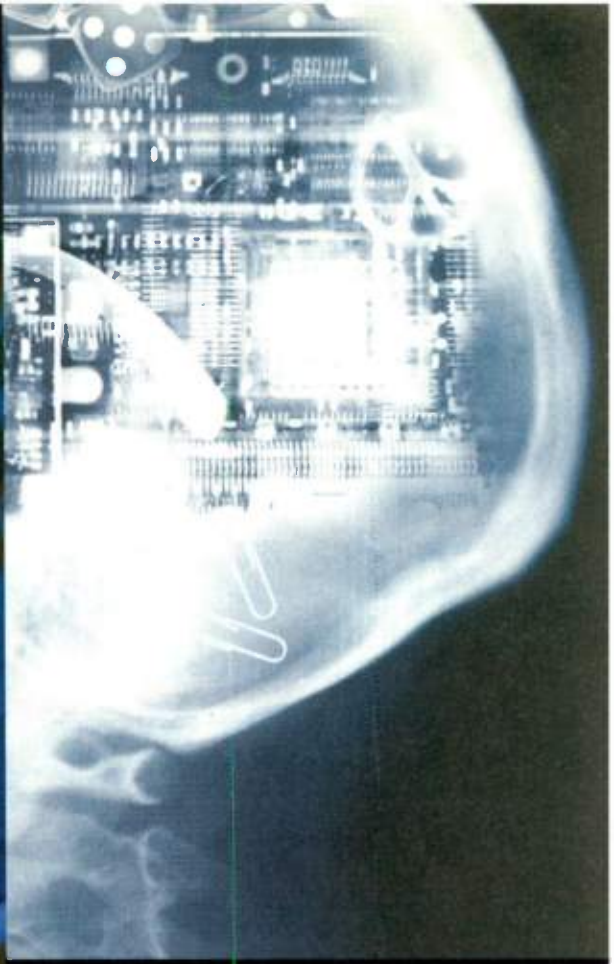
Factoring in the switch interface up front helps ensure effective operation. Addressing this problem when the design is complete leads to switch actuation difficulties. The alignment of the switch in relation to the product's actuator must be studied. The actuator style must be compatible with the type of switch being used. Elastomer actuators on electrical equipment are growing in popularity due to their low cost and sealing performance, yet they may dampen the critical feel of the switch.

Modifications to standard products can extend lead times. Most switch manufacturers offer a catalog illustrating a wide range of standard products (*see the figure*). The variety helps the designer avoid time-consuming custom modifications.



The wide range of products most good manufacturers offer helps to avoid the lengthy lead times required for semi- to full-custom product runs.





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READER SERVICE 192

All switch suppliers are not equal. When the switch decision is delayed until the end of a product's development cycle, the switch supplier is often selected in haste. This quick decision can be as detrimental to a design project as selecting the wrong switch for the application.

Designers should know exactly who is manufacturing the switch, and where it is produced. Does the company build its own product or second-source it? If an off-shore switch manufacturer has been chosen, the designer must factor in the extended lead times that could be involved, as well as the difficulties that may be encountered when requesting application information and resolving technical issues. When selecting a switch manufacturer, a frame of reference for quality must be established. An ISO9001 registration is essential, while a Total Quality Management (TQM) operating philosophy should be a strong consideration.

While much of the talk in the industry dwells on the pressure designers are under to keep costs down, don't forget that switch suppliers are under the same pressures. Even the most reputable suppliers cannot waste valuable resources ensuring that each product they sell meets all application requirements. They must make compromises to keep their product affordable. It is up to the designer to see what compromises were made, and which ones, if any can be tolerated. A key question the designer engineer should ask is, "Am I absolutely certain that there is a standard switch available from a reliable supplier, in the volumes I require, at the price I need, and that meets all of my requirements?" If not, then the switch application must be addressed at the start of the product design cycle.

Peter Brouillette graduated from The University of Lowell, Mass., in 1983. He joined Augat, Inc.-Alcoswitch in 1987 as a Senior Design Engineer. He became New Product Design Manager at C&K Components, Inc. in 1994, and is currently Director of Engineering.

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DIP SWITCHES

MANUFACTURERS OF DIP SWITCHES

Manufacturer	Power range	Lifespan	Positions available	Actuator styles	Ganging option	Mounting configurations	Packaging options	High-temp. plastics	Full -seal and/or gas-tight options
APEM Components, Inc. Wakefield, MA 01880-4444 Barry Mitchell (617) 246-1007 Fax (617) 245-4531 bmitchel@apem.com http://www.apem.com CIRCLE 485	Dry circuit to 100 mA @50 V dc	2000 cycles (min)@ full rated electrical load	One to 12	Piano, flush, extended, slide	Yes	Through-hole, SMD, vertical, right angle, piano, half pitch, tri state	Tape & reel, anti static, tubes, bulk, trays	Yes — reflow compatible, UL94V-O rated	Yes
Bourns, Inc. Riverside, CA 92507 Customer Service (909) 781-5079 Fax (909) 781-5378 http://www.bourns.com CIRCLE 486	100 mA, 50 V dc	2000 cycles	One to 12	Piano, raised, recessed	No	SMD, through hole, insertable	Tubes, tape & reel	Yes	No
C&K Components, Inc. Watertown, MA 02172-4802 Joan Donahue-Servey (617) 926-6400 Fax (617) 926-6846 jdonahue@ckcorp http://www.ckcorp.com CIRCLE 487	0.1 mA @ 5 V dc to 25 mA @25 V dc	2000 to 20,000 actuations	Two to 12 on DIPs, eight, 10, and 16 on DIP coded rotary	Flush, extended, piano	No	SMD with 1/2-pitch spacing; SMD with 0.1 spacing; through hole, right angle	Tube, tape & reel	Yes	Yes
CTS Corp., Electrocomponents Elkhart, IN 46514 Ron Sumrak (219) 296-0415 Fax (219) 293-1240 ctselect@mail.michiana.net http://www.ctscorp.com CIRCLE 488	100 mA or 50 V dc, non switching	1000 to 10,000 actuations	One to 12	Low profile, extended	No	SMD and through hole	Tube for all, tape & reel for SMD	Yes, for SMDs	Full seal with bottom epoxy and removable tape
EAO Switch Corp., Secme Div. Milford, CT 06460 G. Bracci (203) 877-4577 Fax (203) 877-3694 info@eaoswitch.com http://www.eaoswitch.com CIRCLE 489	50 mA @ 24 V dc	1000 to 2000 actuations	Two to 12	Standard, low profile, piano	No	Through hole and SMD	Tube, tape & reel	Yes, to 85°C operating, to 260°C for 1 min infrared soldering	Sealed for soldering
EECO Switch Santa Ana, CA 92705 Sales Dept. (714) 835-6000 Fax (714) 953-3747 sales@eecoswitch.com http://www.eecoswitch.com CIRCLE 490	100 mA @ 5 V dc	20,000 actuations	Eight, 10, 16	Flush, extended	Yes	SMD and through hole	Tape & reel, tubes	Yes	Yes
E-Switch Brooklyn, MN 55428 Kris Akse (612) 504-3525 Fax (612) 531-8235 info@e-switch.com http://www.e-switch.com CIRCLE 491	Switching, 25 mA @ 24 V dc; carrying, 100 mA @ 50 V dc	2000 cycles	One to 12	Recessed, extended	No	SMD, through hole, IC machine insertable	ICtubes, tape & reel	Yes, UL94V-O high-temp plastic	Process-sealed and tape-sealed versions
Globtek Inc. Northvale, NJ 07647 Sales Dept. (201) 784-1000 Fax (201) 784-0111 globtekl@chelsea.ios.com http://gramercy.ios.com/~globtek CIRCLE 492	100 mA @5 V dc, 25 mA @25 V dc	2000 cycles	Two to 12	Top, side, right angle, J-lead, rotary	No	SMD, through hole	Tape & reel, bulk	No	Yes
Grayhill, Inc. LaGrange, IL 60525 Dan Neumann (708) 354-1040 Fax (708) 354-2820 dan_neumann@grayhill.com http://www.grayhill.com CIRCLE 493	1 mA @ 5 V dc up to 150 mA @ 30 V dc	5000 to 20,000	Two to 12	Slide, rocker (raised and recessed both), toggle	Yes	SMD, through hole, right angle, piano DIP	Tube, tape & reel	Yes	Yes
NKK Switches Scottsdale, AZ 85260 Bob Wanless (602) 991-0942 Fax (602) 998-1435 CIRCLE 494	100 mA @ 5 V dc	20,000 (min)	10 and 16	Screw-driver, shaft, dial, knob	Yes	SMD, through hole	Tape &reel	Yes	No
Shogyo International Corp. Plainview, NY 11803 Mark Rubin (516) 349-5200 Fax (516) 349-7744 CIRCLE 495	25 mA @24 V dc	2000 cycles	Up to 12	Normally recessed	No	Through hole	Tubed or tape & reel	PPS	No

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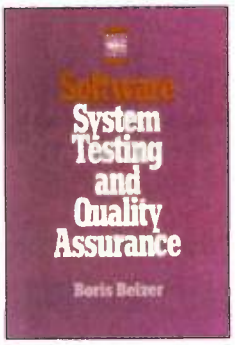

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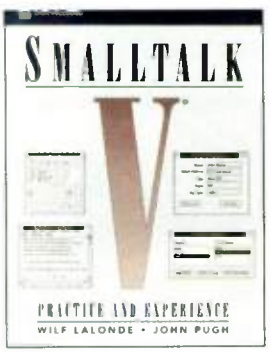
W. Lalonde & J. Pugh



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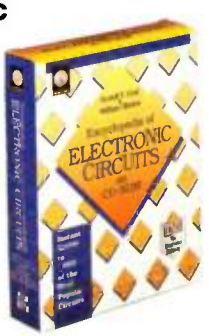

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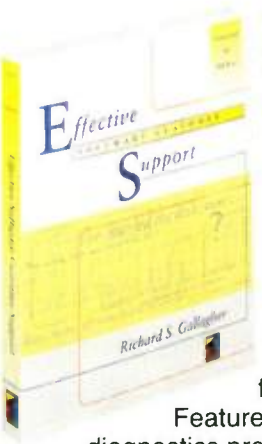

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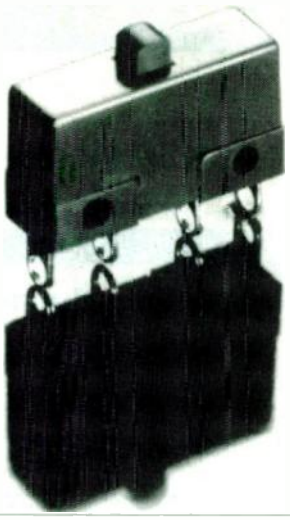

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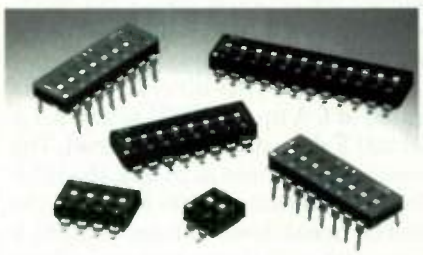
SWITCHES & RELAYS

DIP Switches Have Low Profile

The SD series of low-profile DIP switches come with bifurcated, wiping, gold-plated contacts, and flush or extended actuators. The SPST switches have surface-mount or through-hole



terminals with an off-the-board height of 0.155 in. and 0.168 in., respectively. Available with two to 12 positions, the switches are rated at 100 mA (max) at 20 V dc or 0.1 mA (max) at 5 V dc.

C&K Components Inc., *57 Stanley Ave., Watertown, MA 02172-4802; (800) 635-5936; fax (617) 926-6846.*
CIRCLE 660

Keypad Switches Have Custom Legends

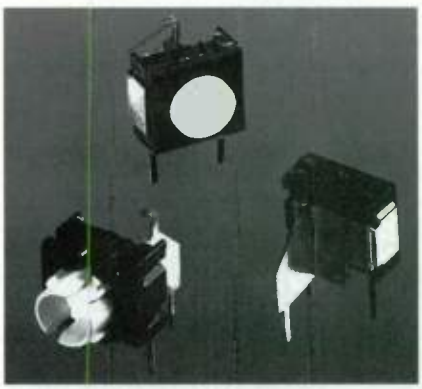
The JF line of SPST keypad switches are rated at 50 mA at 24 V dc, and are available in LED-illuminated or nonil-

luminated models. The switches have a profile of 5.72 mm and are rated for 500,000 actuations. Available options include round, square, or rectangular actuator caps in red, green, blue-gray, or orange. Sculptured actuators are also available. A totally-sealed construction facilitates automated wave soldering and washing. Pricing is $1.58 each in units of 500.

NKK Switches, *7850 E. Gelding Dr., Suite 100, Scottsdale, AZ 85260; (602) 991-0942; fax (602) 998-1435.*
CIRCLE 661

Switches Mount At Right Angles

The Multimec range of switches target applications where stacking of pc boards prohibits access to a normally mounted switch. The switch has an actuator travel of 1 mm, an actuation

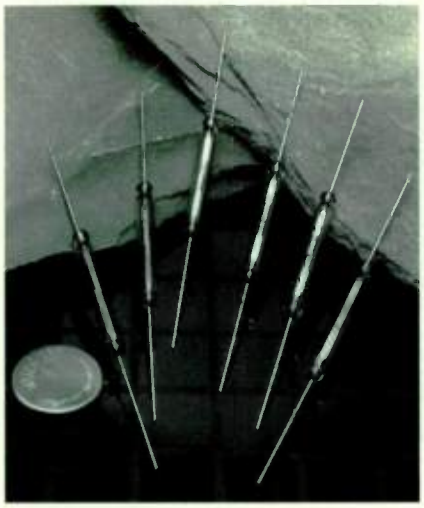


force of 2.5 N, a lifespan of 10 million cycles, and is sealed to IP-67M.

MEC A/S, *P.O. Box 26, DK-2750 Ballerup, Denmark; +45-97 33 66; fax +45-44 68 15 14.* **CIRCLE 662**

Reed Switches Have Stable And Low Contact Resistance

The Series GR10 miniature Form A pressurized magnetic reed switches have a maximum switching voltage of



500 V dc, a maximum switching current of 1.0 A, a dc contact rating of 15 W, and a maximum initial contact resistance of 0.10 Ω. The contacts are made of ruthenium. The switches are 20 mm long, have a diameter of 2.54 mm, and can be supplied potted for pc-board mount and position sensing applications. Options include lead length and shape.

Power Components, *P.O. Box 1348, 56641 Twin Branch Dr., Mishawaka, IN 46545; (800) 221-9257; fax (219) 256-6643.*
CIRCLE 663

Rockers Give Indication Without Draining Power

The CRL Series rocker switch uses a highly-visible flag seen through a circular actuator window to give lighted switch perception without excess power loss. The switch is rated at 16 A, 125 V ac or 8 A, 250 V ac and has a lifespan of 10,000 cycles (min). A wide range of indicator colors also are available.

DNA Group Inc., *P.O. Box 31727, Raleigh, NC 27622; (919) 881-0889; fax (919) 881-0144.* **CIRCLE 664**

Miniature Limit Switches Are UL/CSA/DIN Approved

Conforming to UL/CSA and DIN 50047 standards, the NAiS AZD miniature, vertical-type limit switches are applicable to U.S. and CENELEC conduit sizes. A modular construction allows the actuator unit, head block, and main block to be combined in a variety of configurations.

The AZD two-circuit series is rated at 6 A up to 3500 V ac and 0.3 A at 220 V dc, with a resistive load. The contact resistance is 25 mΩ, the insulation resistance is 100 MΩ, and the initial breakdown voltage is 2500 V rms. Other features include a functional shock resistance of 30 g (max), a vibration resistance of 10 to 55 Hz, and a forced-contact-opening mechanism for safety. Pricing is $17 each in quantity.

Aromat Corp., *629 Central Ave., New Providence, NJ 07974; Walter Roginski, (800) 228-2350; fax (908) 771-5658; http://www.aromat.com*
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SWITCHES & RELAYS

Side-Actuated DIP Switch Is Surface Mountable

The PIANO-DIP switch is a surface-mountable, side-actuated DIP switch that is available with two to 10 positions. Able to withstand temperatures to 260°C, the switch comes in tape-and-reel or tube format. Pricing is $1.30 each in 1000-unit lots.

Grayhill Inc., 561 Hillgrove Ave., La Grange, IL 60525; (708) 482-2131; fax (708) 354-2820. **CIRCLE 666**

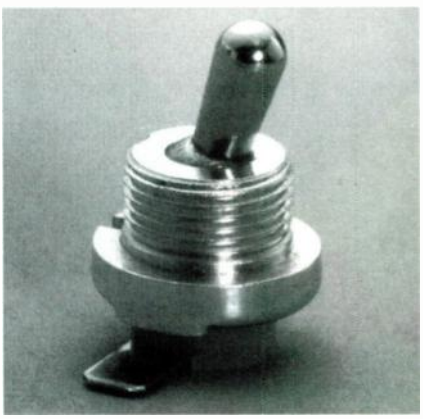
Side-Actuated DIP Switch Has Up To Eight Positions

The Series 193 is a side-actuated, surface-mount DIP switch with two to eight positions. The switch handles temperatures up to 260°C for a period of 60 seconds and comes with self-cleaning, enclosed actuators with gold-plated contacts and an over-center design. Pricing is $0.72 for an eight-position switch and delivery is eight weeks ARO.

CTS Electrocomponents, 1601 Mishawaka St., Elkhart, IN 46514; (219) 296-6700; fax (219) 293-1240.
CIRCLE 667

Toggle Switches Ground Outdoor Equipment

The 4000 series of grounding/shorting toggle switches are designed for outdoor-lawn applications. The SPST devices perform as an ignition grounding



switch to turn off high-voltage ac or dc circuits. The switches are available with quick-connect tab or solder terminals and fit into a 0.154-in. diameter hole.

Tower Manufacturing Corp., 25 Reservoir Ave., Providence, RI 02907; Mike Pitkin, (401) 467-7550; fax (401) 461-2710. **CIRCLE 668**

Snap Domes Target Large-Key Applications

Designed for applications requiring large actuator keys, the FD20625 20-mm, SPST, tactile dome switch has an actuation force of 625 g. Made of stainless steel with optional nickel, silver, or gold plating, the domes have a contact life of over 5 million cycles and can switch from 0.1- to 50-V dc at 0.005 to 100 mA. Custom actuation forces are available. Pricing is $0.25 each in quantity.

Snaptron Inc., 2468 E. 9th. St., Loveland, CO 80537; (970) 663-2820; fax (970) 667-6261.
CIRCLE 669

The top ten reasons we sold so many power inductors last year.

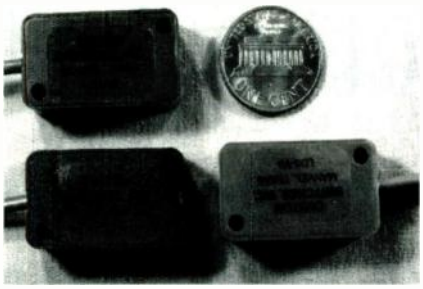
10. Marketing cut a bundling deal with the Girl Scouts. **9.** Our parts seat and solder better than parts from many other manufacturers. **8.** President Clinton thought he could use DC/DC conversion on Washington Republicans. **7.** Pulse's award-winning engineering and its one-of-a-kind prototyping. **6.** We put one in every box of Cracker Jacks. **5.** With nearly half a million square feet of manufacturing, we can ramp up to high volume very quickly. **4.** They had the same part number as Tickle Me Elmo. **3.** No one has a wider variety of low-profile magnetic components for switchmode applications. **2.** We were the Official Choke of National Heimlich Day. **1.** Compaq, 3Com, IBM, Intel, HP and Lucent Technologies bought millions of them.

Pulse
A TECHNITROL COMPANY

For a copy of our Power Inductor catalog (PC503), contact 619-674-8100 (USA), 441-483-428-877 (Europe), 886-7-821-3141 (Asia) or http://www.pulseeng.com

SPDT Proximity Switch Replaces Snap-Action Switch

The magnetically-operated LDS-V3 SPDT proximity switch provides a direct replacement for inductive proximity switches or mechanical switches. The device comprises



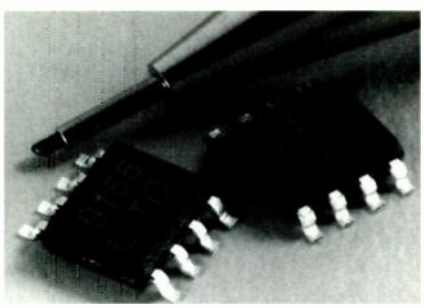
rhodium contacts hermetically sealed within a glass capsule in a dry nitrogen environment. This gives the switch a lifespan rated at over 10 million operations. The assembly is housed in a rugged ABS housing. Included is a 3/16-in.-diameter, 1/16-in. thick disk magnet that will operate the switch approximately 1/8 in. from the target.

***Custom Switches Inc.**, P.O. Box 11, Manvel, TX 77578; (713) 489-7844; fax (713) 489-7521.*

CIRCLE 670

SPDT RF Switch Operates From DC To 2.5 GHz

The TQ9155 is an SPDT, reflective-RF switch IC for operation over the range of dc to 2.5 GHz. Available in an



SOIC-8 package, the switch comprises four depletion-mode transistors in a series/shunt arrangement and uses dual negative voltages to control the switching action. The device has an insertion loss of 1.0 dB (max), an isolation figure of 22 dB (min), and a return loss of 14 dB (min). The parts are 100% RF-tested and have an operating temperature range of -40° to 85°C. Pricing is $1.25 each in 100,000-unit lots and delivery is from stock.

***TriQuint Semiconductor, Inc.**, 3625A SW Murray Blvd., Beaverton, OR 97005; (503) 644-3535; fax (503) 644-3198; http://www.tqs.com*

CIRCLE 671

Rotary Switches Are BS415 Certified

This line of 1- and 4-A, 250-V on/off ECO rotary switches has been tested and certified to BS415 by the BSI. Designed to mount directly onto 16- and 20-mm potentiometers, the switches are available in single- and two-pole configurations. Termination options are either wiring tags or pc-board mounting pins. Made from high-temperature plastic, the switches have a 3-mm contact gap and a lifespan of 30,000 cycles. The over-center switch mechanism uses carbon-steel springs.

***OMEG Limited**, Imberhorne Industrial Estate, East Grinstead, West Sussex, RH19 1RJ, United Kingdom; M. Grantham, 01342 410420; fax 01342 316253; omeg.sales@omeg.co.uk*

CIRCLE 672

Overcurrent Relays Fit A-B 1771 PLC Chassis

The SEL-1551 relay is offered as the first overcurrent/reclosing relay designed to be compatible with the Allen-Bradley 1771 PLC chassis. Able to perform all its power-system protection functions independently from the PLC, the relay comes with all settings and reports accessible through the EIA-232 port on the front panel. Relay element status, metering information, and simplified event reports are available through the PLC backplane

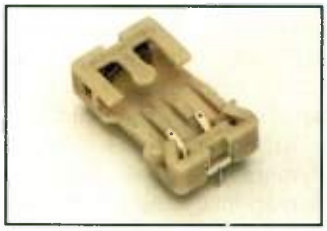
Key features include numerous phase, ground, and negative-sequence overcurrent elements, multiple-shot reclosing with sequence coordination, and enhanced SELogic control equations to create traditional or advanced schemes.

***Schweitzer Engineering Laboratories, Inc.**, 2350 NE Hopkins Court, Pullman, WA 99163-5603; (509) 332-1890; fax (509) 332-7990.*

CIRCLE 673

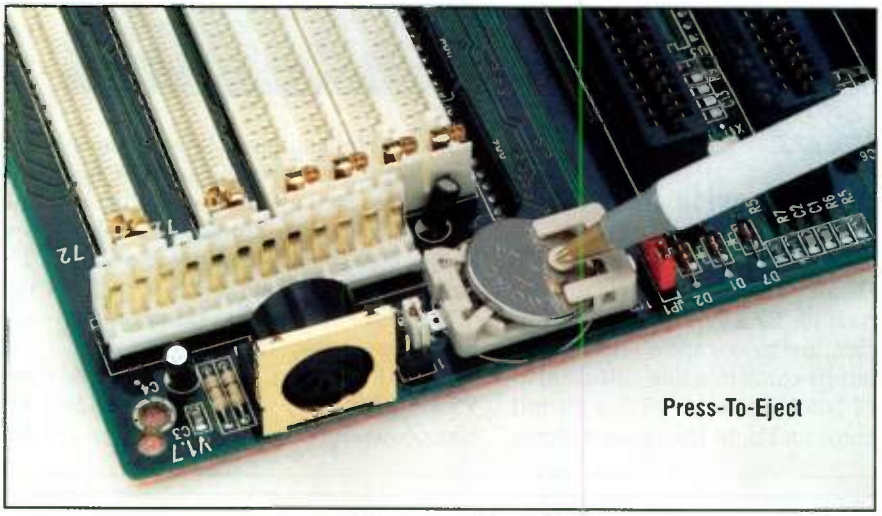
Introducing a breakthrough in coin cell holder technology.

Innovative design enables battery to "Snap" in place, "Lock" tight, and press and "Pop" for easy removal.



BA2032 Plug-In Model

BA2032 with coin cell inserted



BA2032SM Surface Mount Model

MPD Series BA2032* provides greater reliability than any other holder made for CR2032 lithium batteries, yet costs less.

SNAP, LOCK & POP

Once you snap the cell in, the holder provides a snug, locking-fit, so you can forget about the coin cell dislodging, or contact problems. And, when you want to remove the cell, a little pressure from your finger, or a pen point, can pop the coin cell instantly thanks to a *Press-To-Eject* feature.

OTHER KEY FEATURES

Available in plug-in or surface mount configurations, specifically for motherboards, Series BA2032 is shock and vibration resistant, and meets UL2069 specifications. Construction is durable 30% glass-filled NYLON 66. Costs are lower because we are able to manufacture these units in large quantities using our patented, fully automated process that employs several optical inspections.

Add to all that our dedication to on-time delivery and you'll know why choosing MPD Series BA2032 coin cell holders is a snap. Call, write or fax today for complete specifications and pricing.

Memory Protection Devices, Inc.

320 Broad Hollow Road, Farmingdale, New York 11735

Tel.(516) 293-5891 • Fax (516) 752-1971

*U.S. & Int'l Pat. Pending

READER SERVICE 184

GaAlAs LEDs Provide Stable Output

The Model ODT-880W GaAlAs LEDs come with a monolithic detector that includes the LED chip. The monolithic design gives better tracking of power output over the operating temperature range of -55° to 100°C. The LED outputs 20 mW (typical) at 100 mA, while the detector current is 50 µA (typical) at an LED drive current of 100 mA. Pricing is $5 each in 100-unit lots and delivery is three to five weeks ARO.

Opto Diode Corp., *850 Mitchell Rd., Newbury Park, CA 91320; Russ Dahl, (805) 499-0335; fax (805) 499-8105.*

CIRCLE 673

LED Lamps Provide Performance At Low Cost

The HLMP-C series of LED lamps are designed for backlighting, switch illumination, and indoor and outdoor signs. The lamps come in a non-diffused, 5-mm (T1-3/4) package with a 20-mil leadframe and tight meniscus controls for compatibility with radial-lead automated-insertion equipment. The devices come in 644-nm red, 637-nm red, 626-nm red, 585-nm yellow, 602-nm orange, 570-nm green, and 560-nm green

versions. Light output at 20 mA ranges from 27 mcd at a viewing angle of 25°, up to 2000 mcd at 15°, depending on color. Pricing ranges from $0.19 to $0.24 each in 50,000-unit quantities and samples are available from stock.

Hewlett-Packard Co., Components Response Center, *3175 Bowers Ave., M/S 88U, Santa Clara, CA 95054-9929; (800) 537-7715, ext. 1185; http://www.hp.com.* ***CIRCLE 674***

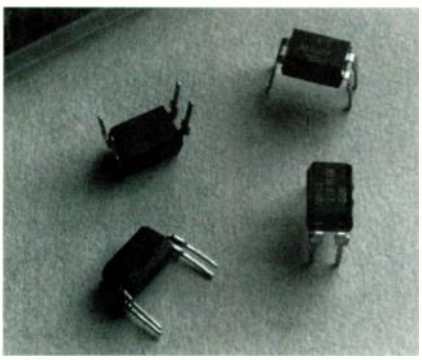
UV Detectors Operate From 5 To 80 mm

Designed to help eliminate the need for visible markers on products, this line of ultraviolet light detectors operates over distances of 5 to 80 mm and can spot objects with diameters ranging from 3 to 25 mm. The devices emit ultraviolet light (350-nm wavelength) that's converted to visible light upon striking a luminescent object or mark. The reflection is then detected by the receiver through a filter that only registers in the 450- to 700-nm wavelength range. A red light-emitting diode indicates signal output. Additional features include DIP switches to select between normal, memory, or one-shot output mode, a response time of 1 ms, and a switching frequency of up to 500 Hz. The devices operates off a 10- to 30-V dc supply and are rated for a life span of up to 8000 hours.

Balluff Inc., *8125 Holton Dr., Florence, KY 41042; Dave Bird, (800) 543-8390; fax (606) 727-7752; http://www.balluff.com.* ***CIRCLE 675***

Four-Pin Optocouplers Come With Multiple CTR Ranges

This line of four-pin DIL phototransistor optocouplers comes in two versions. The H11AA814 Series consists of two GaAs infrared (IR) diodes, connected in inverse parallel, driving a single silicon



phototransistor. The device is available in two current-transfer-ratio (CTR) ranges of 20% minimum to 300% maximum, and 50% minimum to 150% maximum. The H11A817 Series optocoupler consists of a single GaAs IR diode driving a single silicon phototransistor and is available in five CTR ranges from 50% minimum to 600% maximum up to 300% minimum and 600% maximum. The devices dissipate 200 mW, have an operating temperature range of -55° to 100°C, and have a rise and fall time of 2.4 µs each. Pricing for the H11AA814 is $0.47 and for the H11A817 is $0.25, both in 1000-unit lots.

QT Optoelectronics, *610 North Mary Ave., Sunnyvale, CA 94086; (800) LED-OPTO.* **CIRCLE 676**

High-Output LEDs Target Outdoor Applications

The SLE-560, -570, and -580 series of yellow, red, and orange LEDs, respectively, provide a luminous intensity of up to 300 mcd at 20 mA over a 40° viewing angle. In addition, at 20 mA the SLA-570 provides an output of 1000 mcd at 24°, while the SLA-580 provides an output of 4000 mcd at 8°. Designed for outdoor applications, the GaAsP devices come in a T1-3/4 package with an untinted, non-diffused, dome-type lens and emit in the 590- to 620-nm range. Pricing starts at $0.22 each in 100,000-unit lots and delivery is 12 weeks ARO.

Rohm Corp., *3034 Owen Dr., Antioch, TN 37013; (615) 641-2020 ext.154; fax (615) 641-2022; http://www.rohmelectronics.com*

CIRCLE 677

1/4-VGA LCD Designed For Rugged Applications

This line of 1/4-VGA LCDs comes with the company's proprietary Color SuperHomeotropic technology for rugged applications. The passive, multicolor display has a 6.3- by-4.7-in. frame and a 4.5- by-3.4-in. screen. Features include a viewing angle of 120° in horizontal and vertical directions, a response time of 50 ms, and a duty ratio of 1/64 to 1/240. The operating temperature range is -20° to 70°C.

II Stanley Co. Inc., *2660 Barranca Pkwy., Irvine, CA 92606; 800-LED-LCD1; fax (714) 222-0555.*

CIRCLE 678

Panel-Mount Blue LEDs Use High-Impact Lenses

These blue LEDs have been added to the company's 249 and 507 Series of indicators for panel-mount applications that come with high-impact lenses.

Designed for 3/8-in. holes, the 249 Series is available in cylindrical- or stovepipe-cap versions with forward voltages of 3 V, 5 V, 10 V, 14 V, or 28 V at 10 mA. The 507 Series of cartridges are designed for holders and clips. Housings, cartridges, and holders for both series are made of black anodized aluminum. Pricing for the 249 Series is $7.85 each and for the 507 Series is $6 each in 1000-unit lots. Samples are available now, with production quantities in six weeks ARO.

Dialight Corp., Electronic Products Group, *1913 Atlantic Ave., Manasquan, NJ 08736; Elsie Ford, (908) 223-9400; fax (908) 223-8788.*
CIRCLE 679

Assemblies Simplify Panel Mounting Of LEDs

The PM series of low-cost LED panel-mount assemblies cater to T-1 and T-1-3/4 LEDs, and feature a narrow-

flange bezel and minimum housing depth. Ideal for handheld and portable devices, the assemblies are made from 66 UL and 94V-O black nylon material with an oxygen index rating over 28%. Various installation, lead, and lens options are available. Pricing is from $0.63 each in quantities of 500 and delivery is from stock.

Bivar Inc., *4 Thomas, Irvine, CA 92718; Anthony Vilgiate, (714) 951-8808; fax (714) 951-3974.*
e-mail: bivar@interserv.com
Internet: http://www.bivar.com
CIRCLE 680

Fuse Uses Color To Ensure Easy Identification

The 0481 Alarm Indicating Fuse reduces downtime by pinpointing the open circuit using an easily visible color-coded spring arm that extends when the fuse opens. The alarm also offers a visual LED indicator and/or an audible alarm. Color coding is in line with telecom standards for identifying amperage ratings. The fuse is available with current ratings from 0.180 to 15 A at 125 V ac or 60 V dc.

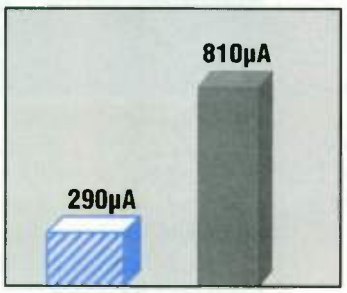
Littelfuse Inc., *800 E. Northwest Hwy., Des Plaines, IL 60016; (847) 824-1188; fax (847) 391-0894.* **CIRCLE 681**

WORLD'S LOWEST POWER 3MHz OP AMPS

290µA Maximum Supply Current in a SOT23-5 Package

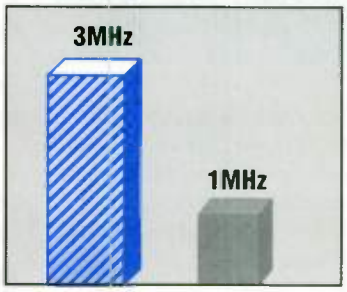
GET RAIL-TO-RAIL® I/O WITHOUT COMPROMISES

CUT SUPPLY CURRENT BY MORE THAN 2x



SOT23
(ACTUAL SIZE)
3.0mm x 3.1mm

INCREASE SPEED BY 3x



Choose Maxim for the Fastest, Lowest Supply Current Op Amps Available!

PART	No. OF AMPS	GBW (MHz)	SUPPLY CURRENT PER AMP (µA, max)	SUPPLY VOLTAGE RANGE (V)	INPUT OFFSET VOLTAGE (mV, max)	LOW-POWER SHUTDOWN MODE	PACKAGES
MAX4330	1	3	290	2.3 to 6.5	±1.5	No	5-pin SOT23
MAX4331	1	3	290	2.3 to 6.5	±0.6	Yes	8-pin µMAX/SO
MAX4332*	2	3	290	2.3 to 6.5	±0.6	No	8-pin µMAX/SO
MAX4333*	2	3	290	2.3 to 6.5	±0.6	Yes	10-pin µMAX, 14-pin SO
MAX4334*	4	3	290	2.3 to 6.5	±0.6	No	14-pin SO

† Rail-to-Rail is a registered trademark of Nippon Motorola Ltd.
* Available after April 1997.

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Circle No. 201 - For U.S. Response
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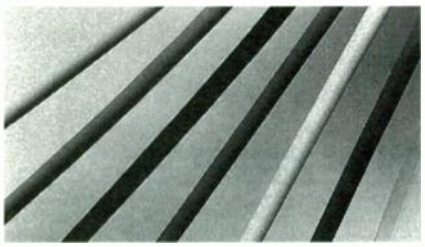
Heat-Shrink Tubing Contains Adhesive Liner

The Poly 421 DW heat-shrinkable polyolefin tubing comes with an adhesive lining and a shrink ratio of either 4:1 or 3:1. Available in diameters



ranging from 1/8 to 2 in., the tubing conforms to MIL-1-23053/4 Class 3 specifications and is packed in standard 4-ft. lengths or spools. Black is standard; other colors are optional. Delivery is from stock from three to four weeks.

Jamco International Inc., *Pennington Business Park, 55 Rte. 31 South, Pennington, NJ 08534; (800) 895-0331; fax (609) 737-8937.* **CIRCLE 682**

Conductive Silicone Sheets Bond Heat Sinks To PWBs

The Thermabond conductive elastomeric sheet adhesives bond printed wiring boards onto heat sinks to help conduct thermal energy away from devices mounted on the boards. The sheets have a bond rating of up to 350 psi, a thermal conductivity of 2.5 BTU-in./ft^2-hr-°F (typical), and an elastic shear modulus of 60 psi. High elasticity permits the PWB and heat sink to expand and contract independently. The adhesive comes in two standard thicknesses of 8 or 15 mils and in sheet sizes or slit rolls up to 36 in. wide by 100 yards long.

Arlon, Silicone Technologies Div., *1100 Governor Lea Rd., Bear, DE 19701; Chuck Roye, (800) 635-9333; fax (302) 834-4021.* **CIRCLE 683**

Miniature Card Package Provides Portable Storage

The Miniature Card package, which complies with specifications laid down by the Miniature Card Implementer's Forum, is a match-book-size, two-piece, sonically welded steel and plastic unit. The package allows for the storage and transportation of digital information, measures 38 by 33 by 3.5

mm, and comes in voltage combinations of 3.3, 5, and 3.3/5 V. The top and bottom cases have a metal connect for built-in ESD protection.

Duel Systems, a Division of Methode Electronics Inc., *1750 Junction Ave., San Jose, CA 95112; (408) 436-4931; fax (408) 436-6063.*

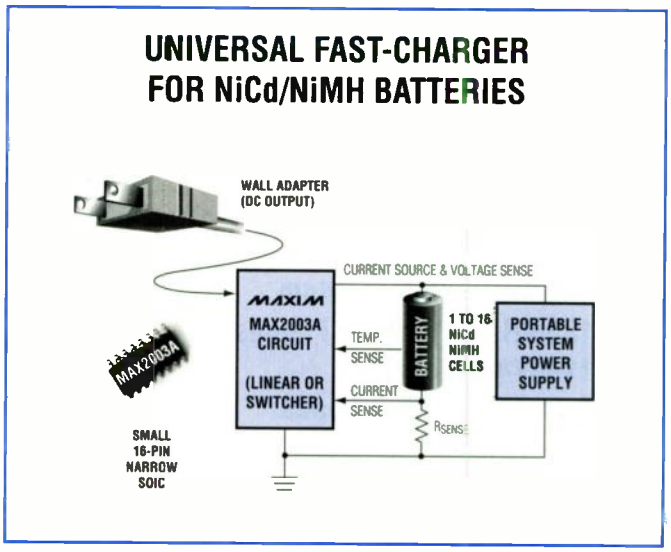
Web: http://www.duel-systems.com
CIRCLE 684

FAST-CHARGE BOTH NiCd & NiMH BATTERIES USING ONE SMALL CIRCUIT!

No Microcontroller Required—Charging Algorithms Are Built In

Use the MAX2003A to build a safe and reliable universal fast-charger and conditioner for both NiCd and NiMH batteries. This stand-alone charger IC features five built-in termination methods, including temperature-slope sensing, and up to three charging stages: fast, top-off, and trickle. It also lets you completely discharge the battery prior to charging. Configure it as an efficient switch-mode current source or as an economical linear current source with fewer components.

- **Charges Both NiCd & NiMH (1 to 16 Cells)**
- **Narrow SOIC**
- **Switch-Mode or Linear**
- **Discharge-Before-Charge:**
  - **Reconditions NiMHs**
  - **Prevents NiCd Damage**
  - **Permits Gauge Recalibration**
- **Temperature-Slope Sensing Termination**
- **Evaluation Kit Speeds Designs (Order MAX2003AEVKIT-SO)**



A MAX2003A-based charging system, powered from a DC wall adapter, simultaneously powers the load and charges the battery. By monitoring the rate of battery temperature rise, it eliminates false charge termination due to battery voltage fluctuations. Besides temperature-slope, other termination methods include negative ΔV, maximum temperature, maximum voltage, and timeout.

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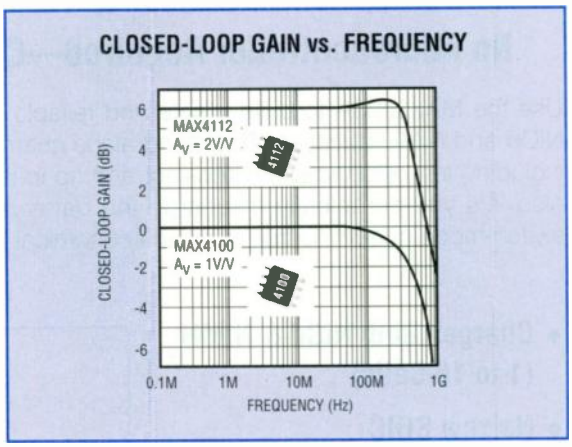
500MHz VIDEO AMPLIFIERS CONSUME ONLY 5mA AND DELIVER 80mA OUT!

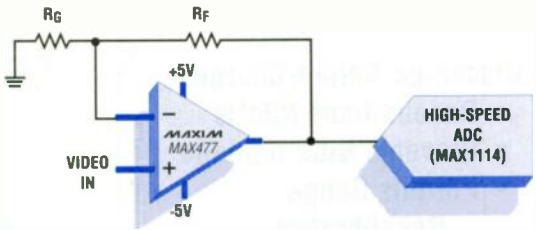
◆ Current-Mode Feedback:
(MAX4112/MAX4113 Family)
- Single/Dual/Quad*
- Bandwidth Independent of Gain
- 15ns Settling Time (0.1%)
- 1200V/µs Slew Rate
- 300MHz FPBW ($V_O = 2V_{p-p}$)

◆ Voltage Feedback:
(MAX4100/MAX4101)
- Unity-Gain Stable
- 8nV/√Hz, 0.8pA/√Hz Noise
- 65MHz 0.1dB Gain Flatness

◆ Voltage-Feedback:
(MAX477)
- Unity-Gain Stable
- 300MHz -3dB Bandwidth
- 130MHz 0.1dB Gain Flatness
- 1100V/µs Slew Rate
- Drives Capacitive Loads

*Contact factory for Quad op amp availability.





The MAX477s high-speed, fast settling, high output current, and C_{LOAD} drive make it ideal for driving high-speed ADCs.

Choose the Ideal High-Speed, Low-Power Amplifier for Your Application

Part	Op Amps per Package	-3dB Bandwidth (MHz)	Min. Stable Gain (V/V)	0.1dB Bandwidth (MHz)	Slew Rate (V/µs)	Supply Current (mA)	V_{OUT} Swing† (±V)	Distortion (SFDR†, dBc)	Diff. Phase (Degrees)	Diff. Gain (%)	Price†† ($)
MAX4100	Single	500	1	65	250	5	3.5	-70	0.04	0.06	1.95
MAX4101	Single	200	2	50	250	5	3.5	-65	0.04	0.07	1.95
MAX4112 Family	S/D/Q	500	2	30	1200	5	3.5	-68	0.03	0.02	1.95
MAX4113 Family	S/D/Q	275	8	90	1800	5	3.5	-62	0.04	0.02	1.95
MAX477	Single	300	1	130	1100	8	3.5	-74	0.01	0.01	2.40

† Notes. V_S = ±5V, R_L = 100Ω, f_C = 5MHz. ††1000-up suggested resale single channel op amps, FOB USA

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Circle No. 208 - For U.S. Response
Circle No. 209 - For International

Circle 520

Tiny Smart Card OS For PIC16C84

PATRICK GUEULLE
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tel. and fax: +33 02 35 43 53 53.

ISO7816-compliant "asynchronous" smart cards consist primarily of nonvolatile memory (ROM, EPROM, and/or EEPROM), managed by an embedded 8-bit microcontroller. Usually, this microcontroller derives from a very popular processor family such as the 68HC705, TMS370, or 8051.

The behavior of the card (including most of its security features) is programmed into an "operating system" (OS) that's mask-programmed into the ROM section of the chip. It can't be altered by the end user.

It is, however, possible to write a smart card OS for virtually any known processor, in order to make it emulate a card with more exotic features. Most microcontrollers with a sufficiently small die could be embedded into a true smart card, but even DIP versions can easily be mounted on a 0.8- mm-thick ISO7816-sized pc board with contacts etched in the ISO position.

The Microchip PIC16C84 RISC microcontroller lends itself well to such applications, obviously extending to various types of secured "portable memory devices" using the same communication protocol as smart cards. Therefore, it's able to utilize off-the-shelf reading and writing equipment and software.

Besides optional features such as cryptographic routines, the very core of a smart card OS is quite a simple matter: The OS merely generates an ISO-compliant ATR (Answer To Reset) when required, then it receives and sends bytes through a specific serial protocol (9600 bits/s for a clock frequency of 3.58 MHz). Special functions such as PIN (personal identification number) checking are simply a combination of these basic routines.

A minimal OS for the PIC16C84 can fit in just 81 words of its 1024 x 14 bits of program EEPROM. It assumes that the chip is connected to the ISO contacts of the card *(Fig. 1)*. No other component of any kind is required, since V_{DD}, RESET, and CLOCK signals all come from the card reader.

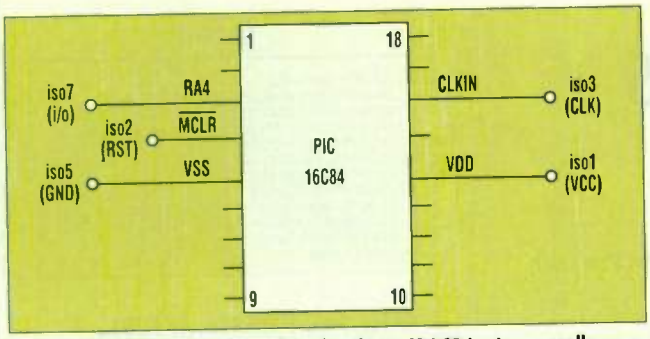
Figure 2 suggests a layout for a 8/10 mm epoxy smart card, designed to ac-

LISTING 1

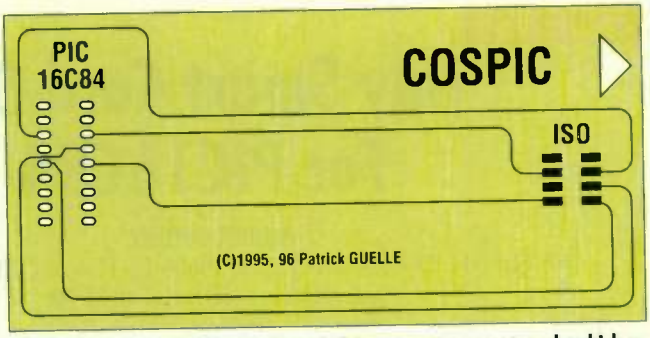
```
:020000000042802
:10000000083160814881483120F20123090004B2076
:10001000900B0B28512A8316051283120800831 6AB
:100020000051683120800800D09083088000051210
:1000300048200310800D0318051603100512492 0CB
:100040000800B1D280800910105 1A46284420083037
:10005000900000310910D051A11144820900B2D2888
:100060000442091090804B20172005164B2005163F
:10007000048200800172005124B20051 44B20080038
:10008000223040C280E304C202728183 04C281C309E
:0A0098008F008F0B4D280800502840
:00000001FF
```

LISTING 2

```
;-----------------------------------------------------------------------
; PIC16C84 configuration fuses:      watchdog (WDT):        OFF
; (to be set manually on the        power on timer (PuT):  OFF
;  PICSTART programmer)             oscillator:         XT mode
;-----------------------------------------------------------------------
;
listen  equ     13H
talk    equ     0FH
bit     equ     4BH
even    equ     38H
odd     equ     3EH
recv    equ     27H
lock    equ     50H
org 51
;
; ----------------------------------------------------------------------
; ATR (answer to reset) generation: 3F 65 25 08 31 04 6C 90 00
; ----------------------------------------------------------------------
reset   movlw 3F           ;first byte
          call even
        movlw 65           ;second byte
          call even        ;send an even parity byte
        movlw 25
          call odd         ;send an odd parity byte
        movlw 08
          call odd
        movlw 31
          call odd
        movlw 04
          call odd
        movlw 6C
          call even
        movlw 90
          call even
        movlw 00
          call even
; ----------------------------------------------------------------------
; wait for a PIN presentation (5678h) at a specified address (1234h)
; ----------------------------------------------------------------------
        call listen        ;set pin 3 (RA4) to input mode
        call recv          ;wait for a byte on I/O
        movlw 0BCh         ;received byte = BCh ? (BULL CP8 ISO class)
        xorwf 11,1         ;compare
        btfss 3,2          ;test the result
        goto lock          ;if false then lock  the card
        call recv          ;wait for a byte on I/O
        movlw 20           ;received byte = 20h ? (PIN presentation opcode)
        xorwf 11,1
        btfss 3,2
        goto lock          ;if false then lock  the card
        call recv          ;wait for first byte of PIN address
        movlw 12h          ;12h ?
        xorwf 11,1
        btfss 3,2
        goto lock
        call recv          ;second byte of PIN address
        movlw 34h          ;34h ?
        xorwf 11,1
        btfss 3,2          ;if false then lock  the card
        goto lock
        call recv          ;wait for a byte on I/O (PIN length information)
        movlw 02           ;PIN length = 2 bytes ?
        xorwf 11,1
        btfss 3,2
        goto lock          ;if not then lock  the card
        call talk
        call bit
        call bit
        movlw 20           ;send procedure byte "no Vpp needed"
        call odd
        call listen
        call recv
        movlw 56h          ;first byte of received PIN = 56h ?
        xorwf 11,1
        btfss 3,2
        goto lock          ;if false then lock  the card
        call recv
        movlw 78h          ;second byte of received PIN = 78h ?
```



1. This simple smart card interface for the PIC16C84 microcontoller can be implemented using merely 81 words of its 1024 word EEPROM.



2. Here's a suggested layout for a 8-10 mm epoxy smart card, which can accommodate the 18-pin DIP version of the PIC.

commodate the 18-pin DIP version of the PIC. The OS itself is supplied here as an Intel HEX dump COSPIC.HEX *(Listing 1)*. It should be merged with a specific application software before being programmed into the PIC.

A simple example of such an application program *(Listing 2)* performs the following tasks:

- send a valid "answer to reset" response each time the ISO2 contact is activated;
- wait for the presentation of a PIN (5678h) at the address 1234h;
- answer 8765h (only once!) when exactly 2 bytes are read from address 4321h;
- lock the card until the next reset.

Any PIN or address error, or other illegal operation, will lock the card until its next reset: this is a very basic smart card security feature.

LISTING 2 (continued)

```
        xorwf 11,1
        btfss 3,2
        goto lock       ;if false then lock the card
        call talk
        call bit
        call bit
        movlw 90        ;send status bytes 9000h (everything OK)
        call even
        movlw 00
        call even
        call listen     ;set pin 3 (RA4) in input mode
;-------------------------------------------------------------------------
; answer to a "read 2 bytes" instruction at address 4321h
;-------------------------------------------------------------------------
seek    call recv
        movlw 0BCh      ;received byte = BCh ? (ISO class)
        xorwf 11,1
        btfss 3,2
        goto lock
        call recv
        movlw 0B0h      ;received byte = B0h ? (read opcode)
        xorwf 11,1
        btfss 3,2
        goto lock
        call recv       ;first byte of the address
        movlw 43        ;(43h)
        xorwf 11,1
        btfss 3,2
        goto lock       ;if false then lock the card
        call recv       ;second byte of the address
        movlw 21        ;(21h)
        xorwf 11,1
        btfss 3,2
        goto lock       ;if false then lock the card
        call recv       ;data length information
        movlw 02        ;2 bytes ?
        xorwf 11,1
        btfss 3,2
        goto lock       ;if not then lock the card
        call bit
        call bit
        call talk       ;set pin 3 in output mode
        movlw 0B0h      ;first byte of card's answer (B0h)
        call odd
        movlw 87h       ;first byte of the data (87h)
        call even       ;(even parity)
        movlw 65h       ;second byte of the data (65h)
        call even       ;(even parity)
        movlw 90        ;status bytes "everything OK"
        call even       ;(even parity)
        movlw 00
        call even
;-------------------------------------------------------------------------
        goto lock       ;lock the card until next reset
;-------------------------------------------------------------------------
end
```

Of course, much more complex applications can be programmed into the PIC, and it would be worth considering some kind of byte exchange with its 64 x 8 data EEPROM (for example, a nonvolatile "error counter" that could invalidate the card forever after, say, three successive presentations of a false PIN).

Basically, seven entry points will be used to activate the OS:

LISTEN (13h): sets I/O line (ISO 7) to input mode

TALK (0Fh): sets I/O line (ISO 7) to output mode

BIT (4Bh): waits for the duration of 1 bit on the I/O line (104 µs at 3.58 MHz clock frequency), used as a general purpose timer

EVEN (38h): transmission of a byte with an even parity

ODD (3Eh): transmission of a byte with an odd parity

RECV (27h): waits for a byte on the I/O line (ISO 7)

LOCK (50h): locks the card in a "silent" mode until next reset.

Of course, the ISO 7816-3 standard will be essential reading before any attempt to develop even the simplest

IFD Winners

Patrick Guelle, B.P. 279, 76055 Le Havre, Cedex, France. The idea: *"Simple PC Smart Card Reader"* July 8,1996 Issue.

Kerry Lacanette, National Semiconductor Corp., 6377 E. Tanque Verde Rd., Suite 101, Tucson, AZ 85175. The idea: *"Temp-Controlled Fan Reduces Noise"* August 19,1996 Issue.

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ERA-2SM	DC-6000	15.2	12.4	4.6	26.0	40	2.00
ERA-3	DC-3000	20.8	12.1	3.8	23.0	35	2.10
ERA-3SM	DC-3000	20.2	11.5	3.8	23.0	35	2.15
ERA-4	DC-4000	13.5	▲17.0	5.5	▲32.5	65	4.15
ERA-4SM	DC-4000	13.5	▲16.8	5.2	▲33.0	65	4.20
ERA-5	DC-4000	18.8	▲18.4	4.5	▲33.0	65	4.15
ERA-5SM	DC-4000	18.5	▲18.4	4.3	▲32.5	65	4.20
ERA-6	DC-4000	11.3	▲18.5	8.4	▲36.5	70	4.15
ERA-6SM	DC-4000	11.3	▲17.9	8.4	▲36.0	70	4.20

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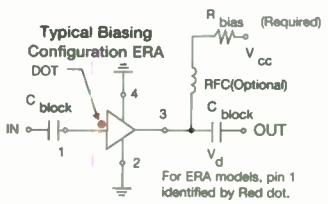
120x60	.002, .047, .068, .1 µf

ERA-1 ERA-1SM
ACTUAL SIZE



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MITCHELL LEE
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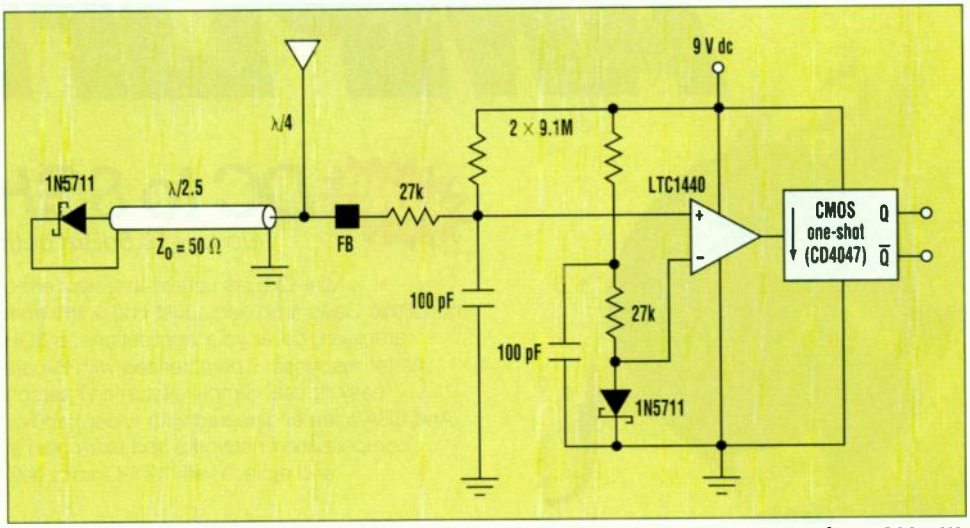
RF ID tags, circuits that detect a "wake-up" call and return a burst of data, must operate on a very low quiescent current for weeks or months, yet have enough battery power in reserve to answer an incoming call. If the system operates in the ultra-high frequency range, designing a receiver for micropower current consumption can be problematic. Familiar receiver techniques such as direct conversion, super-regenerative, or superheterodyne consume far too much supply current. A better method involves a technique borrowed from the simple field strength meter—a tuned circuit and a diode detector.



This UHF micropower field detector, shown here configured for operation at 470 MHz, can detect 200 mW from a reference dipole at 100 feet. It can detect a signal of only a few milliwatts at up to 10 feet.

The circuit, which was tested at 470 MHz, contains a couple of improvements over the standard L/C-with-whip field strength meter *(see the figure)*. Tuned circuits aren't easily constructed or controlled at UHF, so a transmission line is used to match the detector diode (1N5711) to the approximately 6-in.-long whip antenna.

The 0.4-wavelength section presents an efficient, low-impedance match to the base of the quarter-wave whip, but transforms the received energy to a relatively high voltage at the diode end of the transmission line for good sensitivity. Sensitivity is improved 10 dB by biasing the detector diode. The forward threshold is reduced essentially to zero, so a very small voltage can generate a meaningful output change.

When a signal at the resonant frequency of the antenna is received, the left-most Schottky diode rectifies the incoming carrier and creates a negative-going dc bias shift at the noninverting input of the comparator. Note that the bias shift is sensed at the base of the antenna where the impedance is low, rather than at the Schottky diode where the impedance is high. This introduces less disturbance into the tuned antenna and transmission-line system. Total current consumption is approximately 5 μA, including the CMOS one-shot. The one-shot output is used to temporarily enable other circuitry, which in turn answers the interrogation.

Sensitivity of the detector is excellent. The finished circuit can detect 200 mW from a reference dipole at 100 ft. Of course, range depends on operating frequency, antenna orientation, and surrounding obstacles. But, in the clear, a more reasonable distance (e.g., 10 ft.) can be achieved at 470 MHz with only milliwatts of output power.

All selectivity is provided by the antenna. A quarter-wave stub (shorted with a capacitor) can be added to the base of the antenna for better selectivity and improved rejection of low-frequency signals.

Circle 522

Customize And Improve An Oscilloscope Differential Probe

XAVIER ALBERTO and RAMON PALLAS-ARENY
Universitat Politecnica de Catalunya, Departament d'Enginyeria Electronica, c./ Gran Capita, s/n. Edifici C4, 08034 Barcelona, Spain; phone: +34-3-4016766; fax: +34-3-4016756; e-mail: elerpa@eel.upc.es.

Differential active probes for oscilloscopes allow measurement of small differential voltages while rejecting common-mode signals. Commercially available differential active probes can be dc- or ac-coupled. When ac-coupled, however, these probes have a very limited common-mode rejection ratio (CMRR) for low-frequency signals. This is because they use independent filters for each signal line *(Fig. 1a)*.

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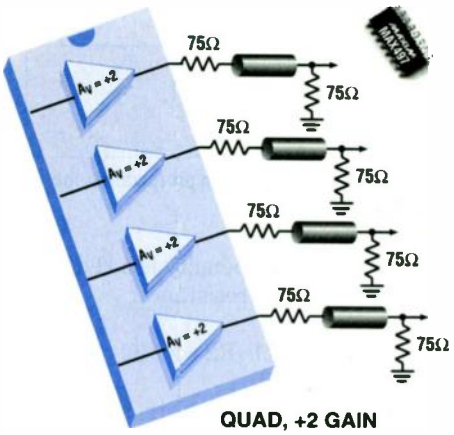
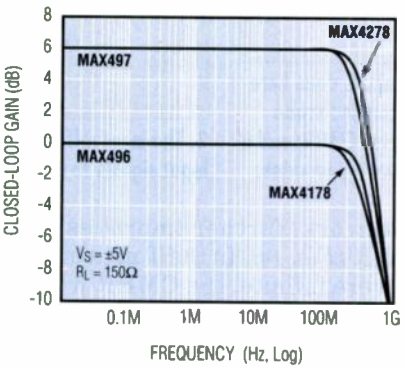
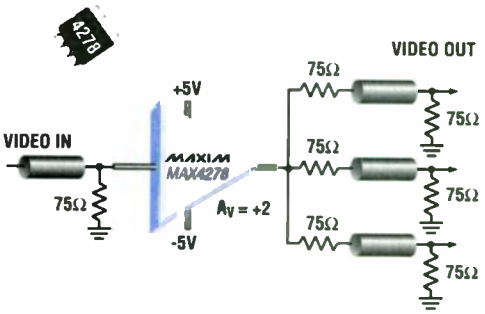


QUAD, +2 GAIN





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MAX4178	Single	+1	330	150	1300	0.01	0.04	-78	8
MAX4278	Single	+2	310	150	1600	0.01	0.04	-72	8
MAX496	Quad	+1	375	80	1600	0.01	0.01	-64	8
MAX497	Quad	+2	275	120	1500	0.01	0.01	-58	8

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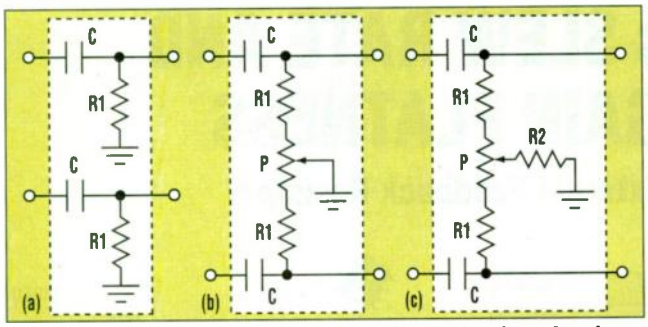
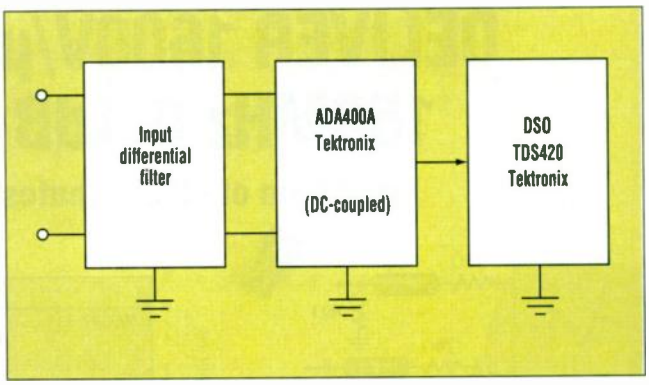


1. Creating a more effective oscilloscope differential probe is done here in several stages: first, the basic input filter for an ac-coupled probe (a); an improvement on the input filter that yields a better CMRR; and a further enhanced input filter for improved CMRR at lower frequencies.



2. The input differential filter is shown configured to precondition the input signals to a standard differential probe.

In a worst-case situation, component tolerances limit the CMRR in the bandpass to:

$$CMRR\ (f >> f_c) \approx 20 \log f/f_c - 20\log(t_R + t_C) + 34\ dB$$

where f_c is the corner frequency for the filters, and t_R and t_C are the respective percent tolerances for resistors and capacitors. If $t_R = t_C = 1\%$, for example, at $f = 10f_c$, the CMRR can be as low as 54 dB. Furthermore, f_c can't be selected, but it is fixed. The ADA 400A probe from Tektronix, for instance, has $f_c \leq 2$ Hz (typical). For a gain of 10, at 1 Hz we measured a CMRR of 28 dB when ac-coupled, and 109 dB when dc-coupled.

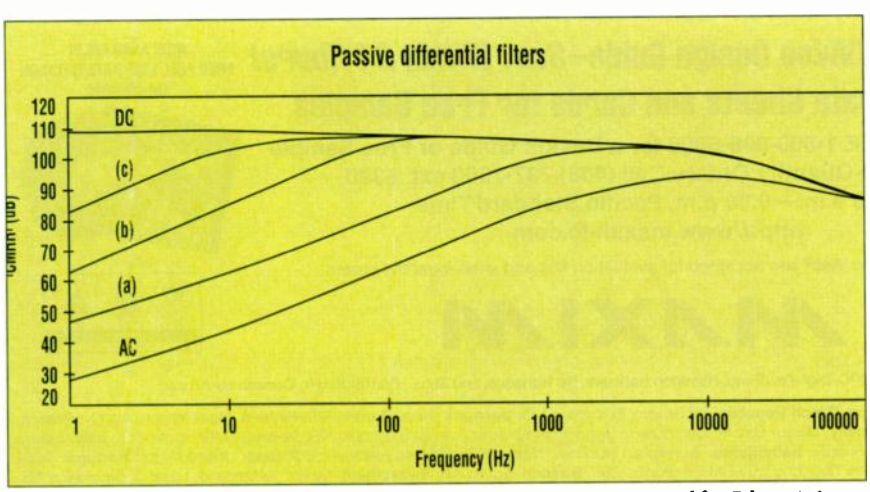
The differential filter *(Fig. 1b)* yields a custom corner frequency and a better CMRR. Instead of relying on matched components, the circuit uses a potentiometer to balance the time constant for each filter.

Another circuit, based on a resistor T network, further improves the CMRR *(Fig. 1c)*. In the T network, if R2 were infinite, the CMRR would only be limited by the amplifier, not by the filter. This is because there would not be any way for an input common-mode voltage to result in a differential-mode voltage at the filter output. Nevertheless, R2 must be included in order to provide a bias path for the amplifier inputs. In the ADA 400A probe, it's possible to disconnect resistor R1 (1 MΩ) in Figure 1a, but a path to ground for a bias current of 25 pA must always be provided.

The three circuits in Figure 1 were designed using C = 100 nF (t_C = 20%), R1 = 2.2 MΩ, R2 = 10 MΩ (t_R = 5%) and P = 500 kΩ. Figure 2 shows the connection of the filters to the differential probe. Figure 3 displays the respective CMRR, together with the CMRR for the probe alone, both dc- and ac-coupled, when the probe gain was 10. The third circuit provides the larger CMRR improvement at low frequencies. The penalty is a reduced differential input resistance:

$$R_d = 2R1 + R1^2/R2 \approx 5\ M\Omega$$

In addition to their superior CMRR, the circuits in Figures 1b and 1c enable f_c to be chosen at will ($f_c = 1/2\pi R1C$). For example, it's possible to design an f_c larger than power-line frequencies in order to better reject interference.



3. Graphical data is given for the CMRR for each of the circuits in Figure 1 and for Tektronix's ADA 400A probe when dc-coupled and ac-coupled. Differential gain was 10.

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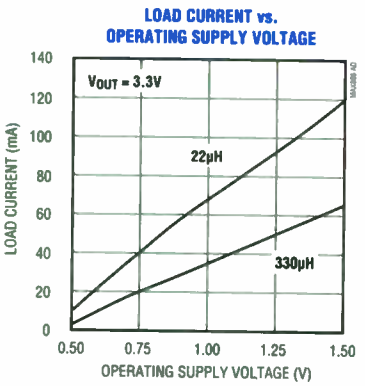

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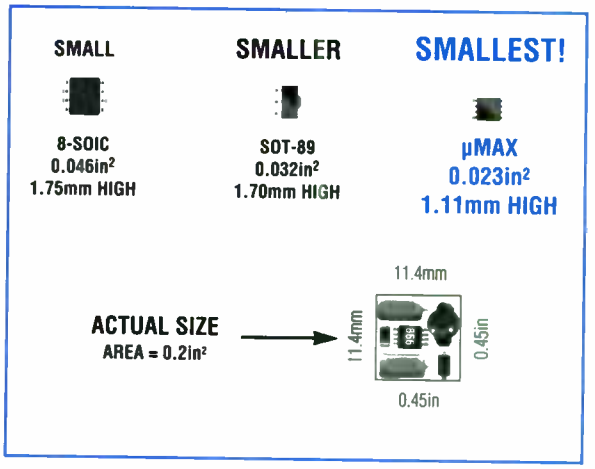

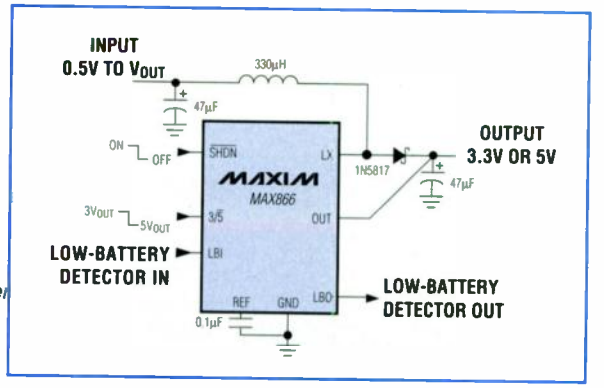

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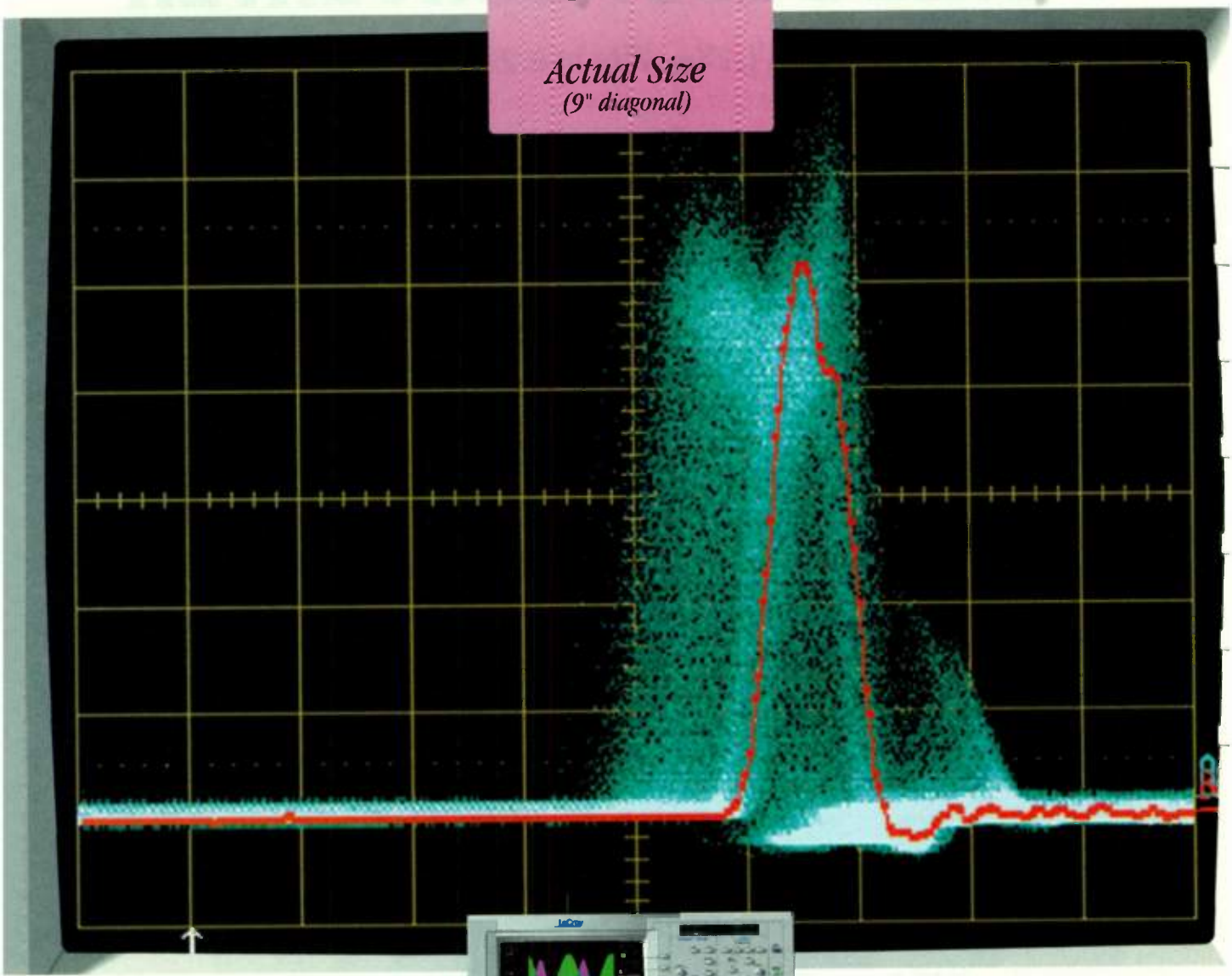

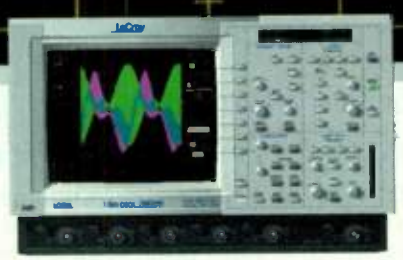

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READER SERVICE 196

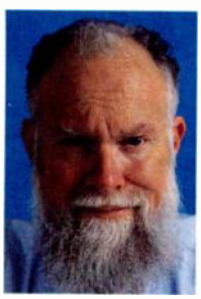
BOB PEASE

What's All This Puzzle Stuff, Anyhow?

Well, April has rolled around again—and that means one thing: 'Tis the season to raise questions. Answers will come in the next issue.

1. Little Egbert has some long, rigid cylinders—a whole lot of them. He observes that he can arrange 2 of them to touch, and, of course, he can arrange 3 to touch each other. If he stands one on end, he can make 4 cylinders each touch each other one. How long can he go on with this? Can he get 5, 6, 7, 8, or 9 cylinders to each touch each other? Of course, bending, warping, or deforming the cylinders is not permitted.

2. In the above problem, it is safe to assume there is a solution. In that solution, how long do the cylinders have to be—what is the minimum ratio of L/D? (For n = 4, L/D = 0, but that's trivial...)



BOB PEASE OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

3. What is it, that is Greater than God, and Worse than the Devil, and if you eat it you will die? (Hint: This riddle is probably at least several hundred years old.)

4. Take a doughnut. Or a bagel. Or any toroid. Cut it with a straight (planar) cut. Do not rearrange the pieces. Cut again. Then cut a third planar cut. How many pieces can you cut the toroid into? Note, a doughnut really is DIFFERENT from a biscuit (8 pieces max)! However, in this case, it makes no difference if you use a SOLID toroid, or just a SHELL. The answer is the same.

5. The same problem as above, but, you are permitted to rearrange the pieces before you re-cut. How many pieces can you get with 3 cuts?

6. What is it that God has none of, the Queen of England has very few of, and I have *lots* of? Note: This riddle is probably not half as old as number 3.

7. A cowboy rode into town on Friday. Four days later, he rode out on Friday. How did he do that?

8. A cowboy rode into town on Thursday October 4. In less than a year, he rode out of town on Thursday October 21. How did he do that?

9. What two MAKES of automobiles can have their names turned into another MAKE of automobile by adding one letter and rearranging the letters?

10. Can you take a piece of paper and fold it over (fold it in half) 10 times? Here's a $10 bill. If you can fold it in half 10 times in a row (and not unfold it each time), you get the $10. If you can't, you owe me $10. Now, are you having trouble folding it in half 10 times? I can fold a piece of paper in half (repeatedly) up to 10 times. How come??

11. Extra credit: Here is the answer to a question—*aggry* (a Ghanian burial bead) and *puggry* (a scarf worn under a hat, to protect the back of the neck, in India). NOW—what is the QUESTION? This is a trick question; don't feel bad if you can't guess.

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

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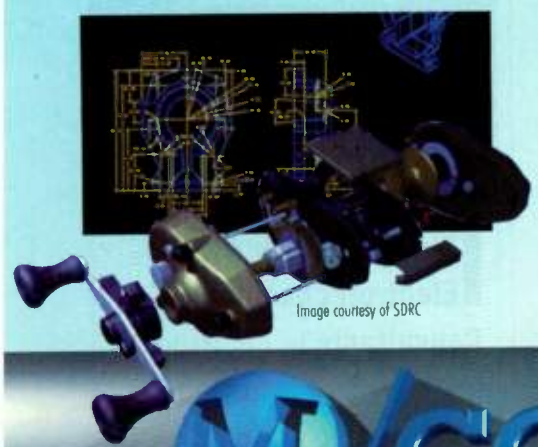

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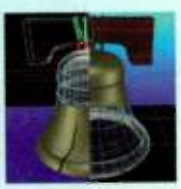

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Analog's Shrinking World

The Pros And Cons Of Surface Mount.

An obvious fact of life about the hectic world of electronic engineering that we live in is that it constantly becomes more so. At one time or another, everyone has wished for "the good old days" when life was simpler and our electronic hassles were less frequent. Of course, those good old days won't be coming back, no matter how hard we wish. We are just left to our own devices as how to best deal with this modern world of ours. Thus enters the topic(s) of this column.

Analog electronics has never been a piece of cake under any circumstances, and typically, it presents us with all sorts of steady challenges. There are the circuit design challenges, which deal with the initial concepts of a design to a certain specification, including hand calculations and/or simulations. Then, there is a breadboard phase, where the design is built up and tested in a lab environment, but usually within loose guidelines regarding a final form factor. The following prototype phase is intended to be very close to final form in size, shape and other physical/electrical factors, and may involve final environmental testing.

While various tools and other design aids have arisen to help expedite the various phases of the design process, these aren't the main focus of this column. Instead, as a broad general example of how the analog designer's life has become more complex, I'd like to talk a bit about some current trends in packaging. The revolution in printed-circuit board (pc board) packaging and design is driving our electronic systems, and quite hard. And, it seems to me that this drive is not always for the good; at least it is generally not always positive from an analog designer's perspective.

Take the surface mount (SM) craze for example, and the general rush to miniaturize and integrate everything. Many electronic components aren't necessarily improved by being shrunk to minimum size. For example, in SM vs. traditional leaded passive components, performance can be sacrificed in several ways. Power dissipation is an obvious one; it is unquestionably a challenge to get the heat out of a part when the only appreciable heat sinking is through two surface-mount leads. Although individual SM chip thin-film resistors are available, their stability/accuracy, while good, isn't up to that of the best leaded components. But thin-film arrays in SM can be quite good, as they take advantage of the natural ratio matching/tracking properties typically critical for analog gain stages.[1]

For capacitors, high-Q, low-dissipation-factor units are available in NP0 ceramic chips, but only in small sizes (≈0.01μF or less). So, if you need a high quality 0.1μF film capacitor for a filter or sample-and-hold circuit, you'll need to look very hard to find one in surface mount (and then it won't be as good as a leaded type). Surface-mount inductors are a real form and function mismatch, but nevertheless they, like many other parts, are fast being force-fitted into this component style.

WALT JUNG

Active parts have seen a radical revision of packaging standards, with many standard ICs like op amps now going into SM compatible SOIC and even more tiny packages, such as the SOT-23. By contrast, familiar 8-pin DIPs may seem almost an anachronism! But, in these cases as well, smaller isn't always better, as a designer using these tiny packages definitely gives up power dissipation. Take an 8-pin package, for example. A DIP version has a thermal resistance of about 90 to 100°C/W, while an SOIC raises this by about a factor of 1.5, and a TSSOP by an additional 1.5X factor. If you go to the extremely small package size of the SOT-23-5, you are talking about a thermal resistance in a range of 300 to 400°C/W, which places rather severe constraints on the part's allowable dissipation.

Performance also can be affected directly and indirectly, as obviously die sizes are small simply to allow such packages, which means more simple, single-function circuits. But some aspects of a smaller chip size are good, i.e., the package's parasitics are lower, meaning better high speed amplifier performance, for one thing. The bottom line here is that more or less chip performance can be available to the end user in SM, dependent upon whether high speed or high dc precision is the primary design goal.

All-in-all, today's typical pc-board designs using SM parts have cramped the design freedoms of an analog designer in many ways. With pc boards typically being multilayer to accommodate largely the digital aspects, the analog subsystem gets to share this, with a big price paid in terms of difficulty in prototyping and troubleshooting. There is no clear-cut answer to address this serious issue, although careful DIP breadboarding, simulations, and lots of prior experience can be helpful.

It's also true that the constraints of SM parts bear little burden for a digital designer, where subtleties of passive component performance are rarely so critical. And, unfortunately, since digital designs outnumber analog by at least an order of magnitude, their requirements call the shots driving most new component developments. And, the analog design challenges get much greater as parts shrink and board densities/complexities increase. And so, the discussions above are best taken as an introductory "fact-of-life."

In truth, the analog designer needs all the help that can be mustered just to stay ahead of the game these days. While dealing with SM and pc-board design issues can certainly be challenging enough, this is but one of a number of vexing issues facing the analog technical types.

References:

1. See SM type "ORN" thin film series, Vishay Thin Film, 2160 Liberty Drive, Niagra Falls, NY, 14304; (716) 283-4025.

Walt Jung is a Corporate Staff Applications Engineer for Analog Devices, Norwood, Mass. A longtime contributor to Electronic Design, he can be reached via e-mail at Walter.Jung@Analog.Com.

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READER SERVICE 189

Pipelined-Burst SRAM Doubles Cache Density

Providing 2 Mbits of cache storage, the M5M5V2132 synchronous pipelined burst static RAM can operate on cache buses that run at up to 133 MHz. The chip is organized as 64 kwords by 32 bits and includes a 2-bit burst counter as well as input and output registers. Thanks to its 2-Mbit density, the burst SRAM can double the level-2 cache-memory size without increasing motherboard real-estate. To get the high density and speed, the chip is manufactured in the company's SuperCMOS process, which combines the best characteristics of bipolar and CMOS technology with minimum feature sizes of 0.4 µm. Also included is a snooze-mode, which turns off the memory when it's not being accessed. The burst mode also can be switched between the interleaved mode needed for Pentium CPUs or the linear mode used by PowerPC CPUs. I/O pins on the chip are low-voltage TTL-compatible and the chip operates from a 3.3-V power supply, consuming 790 mW when clocked at 100 MHz and 870 mW at 133 MHz. In the snooze/standby mode, the power drops to 3.3 mW. Housed in a 100-lead TQFP, the chip fits in a 14-by-20-mm board footprint with a lead pitch of 0.65 mm. Samples of the chip are available immediately; in sample quantities the 133-MHz version sells for $19 each. DB

Mitsubishi Electronics America Inc., *1050 East Arques Ave., Sunnyvale, CA 94086; Narayan Purohit, (408) 730-5900.* **CIRCLE 690**

LCD Controller Delivers Desktop Performance

The CL-GD7556, a 64-bit graphics controller designed to drive LCD panels in portable computers, operates from a 3.3-V supply. The chip offers desktop performance in a low-power device that reduces graphics-subsystem power consumption by about 40% versus previous 5-V circuit choices. The chip also provides multimedia and TV-out capabilities for system designers to implement next-generation portable systems.

Incorporated on the chip is a true 64-bit graphics architecture with a 64-bit bitBLT engine, memory interface, and data paths. The circuit eliminates most of the setup latency during bitBLTs by double-buffering the bitBLT setup registers. Also on the chip is the company's motion-video acceleration technology that includes a color-space converter, andd continuous hardware scaling (thanks to an interpolated scaling engine with edge-sharpening technology). Support is included for mixed color depths through a multi-format frame buffer (RGB, YUV, and AccuPak), which enables up to 16.8-Mcolor video to be displayed simultaneously on top of 256-color surrounding graphics. The CL-GD7556 also features V-Port support for MPEG video playback, teleconferencing, TV tuner, and other applications. Housed in a 256-contact ball-grid-array package or 256-lead PQFP, the chip sells for $22 or $21 apiece, respectively, in lots of 10,000 units. DB

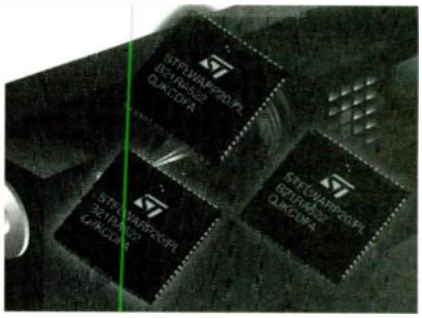
Cirrus Logic Inc., *3100 West Warren Ave., Fremont, CA 94538-6423; George Brecht, (510) 249-4207.*
CIRCLE 691

8-Bit Dedicated Fuzzy Controller Claimed As World's First

An 8-bit fuzzy-logic coprocessor called W.A.R.P. 2.0 (Weight Associative Rule Processor) allows designers to exploit the benefits of the fuzzy-logic approach to implement high-level control without requiring a higher-performance MCU or DSP. Claimed to be the world's first 8-bit dedicated fuzzy controller, W.A.R.P. 2.0 includes input fuzzification and output defuzzification stages, an inferencing unit, memory banks for storing rules, antecedents and consequents, and control logic to handle the downloading of rules and variables. The chip can work either as a coprocessor interfacing directly to all popular microprocessors or as a standalone unit.

With a 40-MHz clock and the ability to handle up to 8 inputs, 4 outputs, and 256 rules, W.A.R.P. 2.0 is suited for such applications as motor control, thermal control, signal and image processing, industrial automation, and consumer products.

An important benefit of the W.A.R.P. architecture involves its technique of storing the membership functions in dedicated on-chip memories. With this ability, the IC can compute a complete fuzzy process comprising eight inputs, four outputs, and 256 rules within 200 µs. Another key feature of the new architecture is that different data structures are used at different stages. Therefore, the data representation is always optimized for the current computation. This overcomes the traditional hurdle of data structures most suitable for fuzzification not being well-suited to defuzzification and vice versa. AV



SGS-Thomson Microelectronics, *1310 Electronic Dr., Carrollton, TX 75006; (214) 466-6000.* **CIRCLE 692**

Convert CPLD and FGPA Designs To Gate Arrays

The QuickASIC conversion program allows CLPD- and FPGA-based designs to be converted quickly and inexpensively to gate arrays once the programming patterns are locked in. Seven gate-array capacities ranging from 6000 to 72,000 gates and from 80 to 300 pads are available in the QuickASIC family. These arrays provide drop-in functional pin-for-pin replacements for most FPGAs and CPLDs, since the pinouts can be completely user-defined. Gate delays (from an input, through a flip-flop, and to an output) are less than 7 ns, and the arrays can operate from supplies ranging from 2.7 to 5.5 V. To keep user costs low, there's a Zero-NRE program that eliminates the non-recurring engineering costs often associated with gate-array designs. All popular package types—SOIC, PLCC, PQFP, TQFP, and VQFP—are available. In 5000-piece quantities, the QuickASIC prices range from $4-$6 per chip for the 6000-gate devices to $20-$28/chip for the 72,000 gate devices. DB

Microchip Technology Inc., *2355 West Chandler Blvd., Chandler, AZ 85224-6199; Bryan Liddiard, (602) 786-7910.* **CIRCLE 693**

COMPUTER-AIDED ENGINEERING

Tool Has Hierarchical Physical-Verification Capabilities

The deep submicron design of integrated circuits presents a number of onerous challenges. To counter those challenges, the Hercules 2.0 hierarchical physical-verification system has been specifically optimized to deliver up to 50% faster CPU run time and use 20% less memory than its predecessor, Avanti's VeriCheck 2.5. As opposed to more traditional physical- verification tools that flatten a design, Hercules 2.0 is able to manage the design complexity of IC designs with tens of millions of transistors on one chip in a completely hierarchical fashion.

The tool uses a set of proprietary third-generation verification algorithms, and provides a single environment for cell-level, block-level, and full-chip verification. Compared to other tools that would require a complex set of operations to analyze complex design rules, Hercules 2.0 can perform design-rules analysis with a single operation.

Another key feature is a "checkpoint and restart" capability, which allows related verification processes to share the same operations that, in turn, increases productivity and reduces time to market. There's also a new programming environment for the industry-standard Scheme language. Consequently, device and parameter extraction and comparison can be flexibly controlled to accommodate complex design rules. Moreover, by using Scheme, designers can even define and compare user properties for devices.

Hierarchical DRC, LVS, and Hercules Explorer, which is an advanced graphical debugging environment used to debug DRC and LVS errors, also are included in the software package. Hercules 2.0 runs on a Unix workstation, and is available now. Call for pricing information. CA

Avant! Corp., *1208 East Arques Ave., Sunnyvale, CA, 94086-5401;(408) 738-8881.*
e-mail: info@avanticorp.com
Web: www.avanticorp.com.
CIRCLE 694

Pc-Board Tool Offers Schematic Viewing Capability

Exchanging pc-board design-related files between design teams located at different sites, even across the Internet, has become vital with the growing complexity of designs. With WinDraft Schematic Capture version 1.26, designers can freely distribute schematics in a standardized format to anyone, anywhere. Furthermore, the tool, regardless of pin size, can act as a schematic viewer. It's able to view any size sheet or document without having to purchase a full version of the software. Added printing functionality allows for x- and y-offsets in the print dialogue box. The WinDraft Schematic Capture version 1.26 tool is free to any current WinDraft user simply by downloading it from the company's World Wide Web site at http://www.ivex.com. CA

IVEX Design International, *15232 N.W. Greenbrier Pkwy., Beaverton, Ore., 97006; (503) 531-3555, e-mail: info@ivex.com.* ***CIRCLE 695***

Graphical Tool Eases Test Generation

DFT Explorer is a graphical access and exploration tool for users of the Sunrise TestGen software suite. The new package allows users to point and click through their testability, fault coverage, and simulation information, rather than having to examine all test-related information serially without the aid of graphics. Two major environments are included: simulation and test. The simulation environment includes three windows that let users graphically examine the data returned by the Sunrise logic and fault simulator. The testability environment has two windows with which users can browse testability and fault data. By allowing users to view fault coverage information simultaneously with simulation and testability results, DFT Explorer makes it easier to determine why a fault wasn't detected. DFT Explorer prices start at $20,000. JN

Viewlogic Systems Inc., *293 Boston Post Rd. West, Marlboro, MA 01752-4615; (508) 480-0881; Internet: http://www.viewlogic.com.*

CIRCLE 703

Digital-To-Analog Boards Include Digital Patterns

The PC-423 analog output boards are four-channel, fully buffered units for ISA computers. Each channel has its own 12-bit digital-to-analog converter and 16-bit digital output ports. The PC-423B offers an 8-ksample FIFO buffer for each channel, and the PC-423A version has 1-ksample buffers. Small-signal update rates peak at 1 MHz, with sample rates to 330 kHz available for full-scale outputs. These are individually selectable for ±5 or ±10 V at up to 5 mA using a rear-panel 25-pin D connector. The boards come with a low-level driver diskette.

Available software includes the PC-423WIN, which runs under Borland Delphi and provides three options: a large host buffer, a host-ring buffer, or streaming from disk. The ring buffer mode continuously loops through a large signal or pattern array in host mode.

The PC-423A costs $1250, and the PC-423B is $1495. OEM discounts are available. Delivery is from stock to three weeks. The PC-423WIN software costs $95. A full source-code version (PC-423WINS) goes for $395. JN

Datel Inc., *11 Cabot Blvd., Mansfield, MA 02048; (508) 339-3000; fax (508) 339-6356.* **CIRCLE 704**

Test Design Software Receives Upgrades

Version 2.0 of the Dantes test design and verification environment features interactive simulation support, improved forms technology, and the ability to start with a complete test schematic. Dantes supports graphical test capture, modeling, rule-checking, simulation, ATE-specific code generation, fixture design, verification, and documentation of mixed-signal tests. Engineers can design and verify tests on a workstation before silicon is available. Interactive simulation allows users to stop the simulation, change instrument setups, and restart the test at any point in the test cycle. The new forms technology offers more flexible and easier-to-use property forms.

Also, users formerly had to enter a Test Module Schematic for each test before generating the Final Test Schematic (FTS). Now the user can begin by entering the entire FTS. Dantes 2.0 costs between $80,000 and $100,000, depending on the licensing arrangement. JN

Integrated Measurement Systems Inc., *9525 S.W. Gemini Dr., Beaverton, OR 97008; (800) 879-7177 or (503) 626-7117; http://www.ims.com.*

CIRCLE 705

VXI-Based Switching Modules Handle 10 A

A pair of high-current VXIbus switching modules extend the power handling capacity of the SurePath routing and switching technology from 2 A to 10 A. Both modules use interchangeable externally socketed relays that can be quickly replaced if damaged during high-current tests. The VX4351 is a 40-channel, 10-A single-pole, single-throw module. The VX4381 is a 4-by-4, 10-A, dual one-wire switch matrix. The VX4351 is U.S. priced at $1950; the VX4381 costs $2200. Delivery is in four weeks. JN

Tektronix Measurement Group, *P.O. Box 1520, Pittsfield, MA 01202; (800) 426-2200, code 1008; fax (413) 448-8033; http://www.tek.com/Measurement/vxi.* **CIRCLE 706**

EMI Testers Evaluate Designs Between 1 And 40 GHz

A family of measurement systems is designed to test new designs for electromagnetic interference in the 1-to-40-GHz range, in accordance with FCC standards in the U.S. and proposed European standards. The systems will

measure electromagnetic radiation from intentional or unintentional radiators. Each package includes either an HP 8593EM electromagnetic compatibility analyzer or an HP 8564E spectrum analyzer with appropriate preamps, power supplies, antennas, and cables for the desired frequency range. The equipment comes mounted on a rolling cart, except for the antenna, which can be tripod-mounted or handheld. Calibration data is stored in the test receiver for automatic data correction. Measurement software provides an easy-to-use interface, allowing for quick recall of measurement settings. The systems display the field strength of the emission in dBμV/m. The three systems include the HP 84125A (1 to 18 GHz) for $57,150; the HP 84125B (1 to 26.5 GHz) for $59,150, and the HP 84125C (1 to 40 GHz) for $85,200. JN

Hewlett-Packard Co., *Test and Measurement Org., P.O. Box 50637, Palo Alto, CA 94303-9512; (800) 452-4844, ext 5012; http://www.hp.com.*

CIRCLE 707

10-Bit, 40-Msample/s ADC Latest To Enter Video Arena

The TMC1185 is a 10-bit, 40-Msample/s ADC with internal track-and-hold, reference,and power-down mode. The inputs can be either single-ended or differential while the IC works from a single +5-V supply, dissipating 380 mW. The part is fabricated in a 0.6-µm CMOS process and comes packaged in a 28-pin SOIC. Excellent Nyquist differential linearity performance is claimed, as is low distortion and a high signal-to-noise ratio. Applications are expected to be in the video and telecommunications areas. The TMC1185 is available in production quantities now and is priced at $14.75 in 1000s. PMcG

Raytheon Electronics, *Semiconductor Div., 5580 Morehouse Dr., San Diego, CA 92121; (619) 457-1000; fax (619) 455-6314; fax-back service on (415) 988-2123 (document #1177).*

CIRCLE 696

14-Bit, 3-MHz Sampling ADC Targets Digital Communications

The ADS-943 is a 14-bit, 3-MHz sampling ADC optimized to meet the dynamic-range and sampling-rate needs of digital-communications applications.

Peak harmonic distortion reaches -83 dB and the signal-to-noise ratio is 79 dB. The device requires ±5-V supplies and dissipates 1.7 W in a 24-pin DDIP package. The power requirements and size, together with the ability to operate at the minimum 2.2 MHz sampling rate, suit the device well to ATM, ADSL and HDSL applications.

The IC guarantees no missing codes to the 14-bit level over the entire military temperature range. Although it's optimized for frequency-domain applications, the differential nonlinearity (typically ±0.5 dB) and noise make it equally suitable for time-domain applications like graphic and medical imaging.

The ADS-943 architecture consists of a fast-settling sample-and-hold amplifier, a sub-ranging, two-pass flash ADC, an internal reference, timing/control logic, and error-correction circuits. Input and output levels are TTL while the circuit is edge-triggered, requiring a rising-edge of a start-convert pulse to initiate a conversion. The input range is ±2 V with versions in both the commercial and military temperature ranges using an autocalibrating, error-correcting circuit. The IC is pin-compatible with the 8-MHz ADS-946 and the 10-MHz ADS-947. Prices are $330 in 100-unit lots for the commercial ADS-943MC, and $412 for the military ADS-943MM. PMcG

Datel Inc., *11 Cabot Blvd., Mansfield, MA 02048; (508) 339-3000; fax (508) 339-6356.* **CIRCLE 697**

Mini 6-Pin Package Aims At Portable-Market Apps

The Micro-6 is a new package that addresses the needs of the portable electronics market with a smaller footprint and lower cost. The package

offers the same power-handling capacity as the popular 8-pin SOIC, but occupies only one-fourth of the footprint. A new leadframe design increases the thermal transfer from the bottom of the chip through the leads of the package; four of the package's six leads are connected directly to the chip's pad area and the heat is quickly spread over the package footprint.

The power rating offered is over 1.5 W, with power densities in excess of 150 mW/mm^2. The first two products being offered in the new package are p-channel power MOSFETs with on-resistances of only 0.2 Ω and drain currents in excess of 2 A. The IRLMS5703 offers a BVDSS of -30 V, while the IRLMS6702 has a BVDSS of -20 V. The devices are targeted for notebook and PDA load-management switching, cellphone power management, buck/boost converters, and for backlight inverters. At volumes of 100-k pieces, the IRLMS5703 is priced at $0.20 and the IRLMS6702 is priced at $0.21, with quantities available now. PMcG

International Rectifier, *100 North Sepulveda Blvd., El Segundo, CA 90245; fax-on-demand (310) 252-7100, fax (310) 252-7171; Web: http://www.irf.com.* **CIRCLE 698**

Longer-Duration Record And Playback Chips Introduced

The ISD33000 series of 3-V (2.7 to 3.3 V) products offers longer recording durations than previous products developed by Information Storage Devices (ISD). The products are optimized for cellular and portable phone systems in which the supply is being standardized at 3 V. The company also expects users of voice pagers, personal voice organizers, PDAs, and portable instrumentation to build the product into their equipment.

Like all ISD products, the memory is nonvolatile and a new AutoMute facility has been added to considerably reduce background noise occurring during the playback of silent periods or pauses. The ICs support both Microwire and SPI (serial peripheral interface). A Universal Sound Development and Programming System offers a PC-based, sound file editor and programmer for the series. A Windows-compatible version of the software lets users graphically edit and program one or more sound files onto multiple ISD33000 chips. A complete system for programming eight devices simultaneously costs about $2000. A development system for the ISD33000 series also is available. The series comes in recording durations of 1 to 4 minutes in die form, 28-pin SOIC, PDIP, or TSOP packages. Prices for 10,000 pieces range from $7.95 to $13.20 depending on the duration, the packaging, and the temperature requirements. PMcG

Information Storage Devices Inc., *2045 Hamilton Ave., San Jose, CA 95125; (408) 369-2400; fax (408) 369-2422; Web: http://www.isd.com.*

CIRCLE 699

Multichannel, Amp-Filter Boards Serve Sigma-Delta ADCs

A family of VMEbus-based amplifier-filter boards offer up to 32 channels of programmable differential amplifiers and precision fixed-frequency 3-pole analog filters on a single-width, B-size (6U) board. Each amplifier-filter channel features programmable gains in steps from –12 dB to +60 dB in 6-dB steps, Butterworth or Bessel filters with corner frequencies from 100 Hz to 100 kHz, and single-ended outputs to provide precise signal conditioning for wideband signals in VMEbus systems. The VM32PAFF boards are aimed at systems using sigma-delta analog-to-digital converters (ADCs). The board first boosts the signal, then filters out unwanted frequencies before sending the signal to the ADC. Per channel costs for the VM32PAFF boards range from $432.50 in low-volume applications (an 8-channel board) to $206.60 in applications with over 800 channels. JN

***Frequency Devices Inc.**, 25 Locust St., Haverhill, MA 01830; (800) 252-7074, ext. 160; (508) 374-0761; fax (508) 521-1839.* **CIRCLE 713**

Conditioning Options Offered For PC-Based Data System

Four signal-conditioning options are available for the WaveBook/512, a PC-based, 1-MHz, portable, multichannel digitizer. Both the WBK12 low-pass filter card and WBK13 low-pass filter card with simultaneous sample and hold (both field installable) can be programmed as eight-pole elliptic filters with cutoff frequencies of 400 Hz to 100 kHz. Or they can be programmed as eight-pole linear-phase filters with cutoffs from 400 Hz to 50 kHz. Users also can program each card for full-scale input ranges of from ±50 mV to ±5 V (or +100 mV to +10 V unipolar). Total capacity is 72 channels.

The WBK14 dynamic signal module allows users to expand their systems in eight-channel increments to 64 channels of dynamic inputs from ICP-style transducers. Each channel has its own constant-current source for transducer biasing, ac coupling, programmable gain, programmable low-pass filtering, and sample-and-hold circuitry. The WBK15 eight-channel, multipurpose isolated signal-conditioning module accepts any combination of eight optional 5B multipurpose, isolated-input, signal-conditioning modules. It features eight cold-junction sensors for thermocouple measurements. Eight modules can be connected, for a total of 64 channels. The WBK12 costs $2495; the WBK13, $2995; the WBK14, $3495; and WBK15, $1195. Delivery is in four weeks. JN

***IOtech Corp.**, 25971 Cannon Rd., Cleveland, OH 44146; (216) 439-4091; fax (216) 439-4093.*
e-mail: sales@iotech.com
Web: http://www.iotech.com
CIRCLE 714

Handheld Graphical Multimeter Uses Bright Backlit Display

The 867B Graphical MultiMeter uses a new backlight technology employing blue LEDs. The broadband, sky-blue light is converted to white backlight by an amber filter. When this technology is coupled with transmissive LCDs, the result is a higher contrast and significantly brighter image than offered by other displays. The LED backlight, developed by Nichia of Japan, uses less than half the power other backlights need to produce the same intensity. The Graphical MultiMeter's display is twice the size of a typical handheld digital multimeter display. The 867B's basic dc accuracy is 0.025%. The meter can read small currents with a 10-nA resolution. Optional software logs meter readings to a PC for later analyses through the meter's computer interface. In addition, continuous monitoring is possible using the Trend Graph feature, which plots a signal's performance over time. The 867B costs $695. An entry-level model, the 863, costs $495.

***Fluke Corp.**, P.O. Box 909, Everett, WA 98206; (800) 443-5853 or (206) 347-6100; fax (800) 358-5332; e-mail: fluke-info@tc.fluke.com; Internet: http://www.fluke.com*
CIRCLE 715

Units Source And Measure High Voltage Or High Current

The Model 2410 high-voltage SourceMeter and Model 2420 high-current SourceMeter combine precision voltages and current sources, respectively, with a high-resolution digital multimeter and measurement firmware. The 2410 generates voltages from ±5 mV to ±1100 V and measures voltage from ±11 mV to ±1100 V. The 2420 generates currents from ±500 pA to ±3 A, and measures currents from ±100 pA to ±3A. Resistances from 1 μΩ to 200 MΩ can be measured. Source accuracy (1 year) varies from 0.02% to 0.88%, depending on instrument and measurement range. The units can make more than 1000 nonbuffered 4-1/2-digit readings per second over an IEEE-488 bus, or 2000 readings per second into memory. The memory buffer stores up to 5000 5-1/2-digit readings. Both the Model 2410 and Model 2420 cost $4995. JN

***Keithley Instruments Inc.**, 28775 Aurora Rd., Cleveland, OH 44139-1891; (800) 552-1115; (216) 248-0400; fax (216) 248-6168; e-mail: product_info@keithley.com; Internet: http://www.keithley.com.*
CIRCLE 716

Wavelet Analysis Tool Debuts For Signal, Image Processing

With its innovative graphical user interface (GUI) and a set of wavelet routines, the MATLAB Wavelet Toolbox helps engineers learn and apply wavelet techniques when developing commercial signal and imaging products. The toolbox is integrated with the MATLAB technical computing environment, which develops algorithms to improve data compression and noise removal in applications such as audio, image, and video communications. Engineers can examine phenomena that are local, multiscale and/or non-stationary.

Wavelet analysis avoids the tradeoffs between time and frequency resolution that's inherent in Fourier analysis. Also, designers can view and explore data details that other signal-analysis techniques miss, such as trends, discontinuities in higher derivatives, self similarity, and breakdown points. Analysis often can compress or de-noise a signal without appreciable degradation, even when preserving both high- and low-frequency components.

The Wavelet Toolbox includes a tutorial on wavelet fundamentals, applications, and reference documentation. It also integrates with MATLAB and other toolboxes, especially for signal processing, image processing, neural networks, and fuzzy logic. ASCII m-file source code is provided to view and customize algorithms. On top of that, continuous wavelet transforms, 1-D and 2-D discrete wavelet transforms, and wavelet packet transforms are included.

Support for popular wavelet families include Biorthognal, Daubechies, Haar, Mexican Hat, Meyer, Morlet and Symlets. The toobox comes with a book that provides a theoretical foundation and includes MATLAB-based exercises and examples.The MATLAB Wavelet Toolbox, which requires MATLAB 4.2.c.1, is now shipping for Windows-based PCs, Macintosh systems, and all Unix-based workstations. Pricing starts at $895. ML

The MathWorks Inc., *24 Prime Park Way, Natick, MA 01760-1500; (508) 647-7000.*
e-mail: info@mathworks.com
CIRCLE 700

Operating System Targets Handheld Computing Devices

The Eden OS V2.0 is an improved embedded real-time operating system for 16- and 32-bit handheld applications (e.g., PDAs, electronic organizers, PICs, and smart mobile phones), set-top boxes, and web browsers. The operating system requires only 256-kbytes of ROM and 128-kbytes of RAM, is completely portable, and is processor-independent.

Composed of a suite of interchangeable modules, it allows designers to customize operating-system capabilities to maintain product differentiation and brand identity through unique functions. Eden supports all popular low-cost, low-power 32-bit RISC processors, including Advanced RISC Machines' ARM7100, Hitachi's SH1 and SH3, Motorola's MPC821 and MPC823, Philips' OCP/DINO and the basic MIPS core. The operating system is also suited for complete ASIC-based systems using core microprocessor technologies.

Designed as an open operating system with an open API and GUI, Eden OS V2.0 allows manufacturers to integrate existing technology into new products with shortened development time and reduced development overhead. The system also can be scaled down to optimize functionality and meet the requirements of available memory space. Using the Dynamic Linking and Loading facility for field upgrades, system patches, software debugs, and functional enhancements provides an easy path to system modifications. Processor independence allows manufacturers to select a processor and tailor hardware for target markets in terms of functionality and price point.

In addition to licensing the operating system, Eden provides system design consultancy, hardware-interface-layer porting and customization, server customization, ROM application software development, and PC Companion Application software development and application support. The license fee is negotiated according to features and other services required. ML

Eden Group Ltd., *The Chapel, Rainow, Cheshire, England SK10 5XF; +44(0)1625 576050; fax: +44(0)1625 576041.* **CIRCLE 701**

Encryption Software Integrates Data Compression

MUM 1.0 developed by Hi/fn Inc. is the first available encryption product to incorporate data compression for security without compromising network efficiency. The product is a processor-independent software implementation of standard RC4, DES, and Triple DES data encryption, HMAC-SHA, HMAC-MD5 keyed hash functions, and LZS and MPPC (Microsoft point-to-point compression) used in Internet, intranet, and client-server networks.

MUM 1.0 first compresses incoming data to reduce network bandwidth requirements by 4 to 1, then encrypts the data using industry standard encryption. DES (Data Encryption Standard) employs a 56-bit key and encrypts data in 64-bit blocks. Triple DES encrypts three times, each with a different 56-bit key. RC4 is a stream cipher that uses a variable-length key.

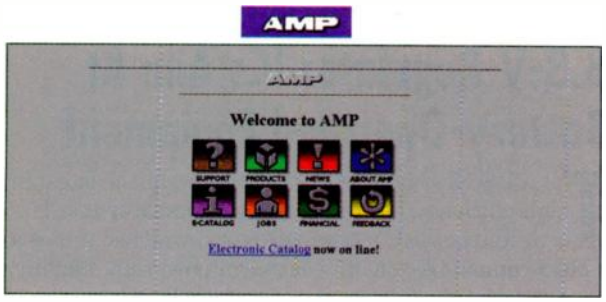
LZS data compression provides 4-to-1 lossless data compression for platforms ranging from desktop computers to servers within network environments. MPPC data-compression technology is used in routers, firewalls, remote-access servers, and ISDN products that interoperate with Windows NT servers.

MUM 1.0 is available now under an annual license fee arrangement. For applications not requiring data encryption, the Hi/fn 9710/9711 compression coprocessors are cost-effective hardware alternatives to software-only solutions for routers, firewalls, and remote-access servers. The 9710 compresses and decompresses data in the LZS format, and the 9711 compresses and decompresses data in both the LZS and MPPC formats. Each coprocessor provides 8-Mbyte/s compression throughput and 15-Mbyte/s decompression throughput. They also support pipelined operations, require no CPU intervention between operations (no latency), and support up to 2048 simultaneous histories.

In volumes of 10,000 or more, unit pricing is $17.20 for the 9710 and $19.20 for the 9711. ML

Hi/fn Inc., *12636 High Bluff Dr., San Diego, CA 92130; (619) 794-4550.*
CIRCLE 702

HOME PAGE WEB SITE



http://www.amp.com

http://www.astec.com

http://www.harris.com

http://www.intel.com

http://www.oei.omron.com

http://wwwsemiconductors.philips.com/ps

http://www.pharlap.com

PICMG Chooses Millipacs2 Family For Compact PCI Spec

Solid mechanical design, integrated shielding capabilities, easy coding features, takes less board space. These attributes swayed the PCI Industrial Computer Manufacturer's Group (PICMG) toward electing the IEC 1076-4-101 connector family, dubbed Millipacs2, for its Compact PCI specification. The standard Millipacs2 wouldn't fit into conventional Eurocard (inch-based) dimensions, however, since it's a metric connector in multiples of 25 mm (needed to fit the mechanical parameters of a conventional DIN 41612. Therefore, one of the connector modules (type B) had to be modified from 25 positions to 22.

A 3U Compact PCI, using a standard 100 mm by 160 mm Eurocard, contains a standard type A Millipacs2 module with polarizing and coding features, and a modified type B Millipacs2 module that provides 220 pins for the PCI interface. As a result, the Compact PCI bus now offers a passive backplane; is electrically identical to PCI so that standard PCI silicon can be used; permits convection cooling; and allows "hot swapping" of cards when the unit is operating. *RE*

Framatone Connectors International, *145 rue Yves Le Coz, 78035 Versailles Cedex; phone: 33-(1) 39 49 21 83; fax: 33-(1) 39 49 20 00; Web: http://www.fciconnect.com.* **CIRCLE 590**

80C51 Microcontrollers Feature Increased Speed, Lower Power

Targeting hand-portable, battery-powered applications such as pagers, PCMCIA cards, and mobile phones, a new range of 80C51 and derivative microcontrollers possess 50% more speed and up to 75% lower power consumption. Their operating voltage range is from 2.7 to 5.5 V. The redesigned 80C51 core pushes the maximum clock frequency from 24 to 33 MHz, and makes parts fully static in operation. Consequently, the system clock can be stopped to reduce standby power consumption without losing the contents of memory registers or affecting the state of the microcontroller.

The devices' operating power consumption, which on a 5-V supply is already half of that of existing 805C1s, can be reduced even further by exploiting their low-voltage capabilities. Consumption can be halved again by operating at 3 V, giving an overall savings of up to 75% compared to existing devices. The first members of the redesigned family are available now in masked ROM form. OTP and ROM-less versions will be available during the second quarter this year. The entire line will be migrated to the new core by the end of 1997. *RE*

Philips Semiconductors, *P.O. Box 218, 5600 MD, Eindhoven, The Netherlands, phone: +31 40 272 20 91; fax: +31 40 272 48 25.* **CIRCLE 591**

3.3-V Regulator ICs Aim At Battery-Operated Equipment

The A8186SLU and A8187SLT represent the latest in high-efficiency, low dropout 3.3-V regulator ICs. Except for the SLU's "enable" input, which supplies a CMOS-compatible "on/off" control for power-up, standby, or shutdown, the devices are identical. The devices are suited to optimizing efficiency and maximizing battery life in equipment such as cordless and cellular telephones, palmtop computers, and personal digital assistants.

A PMOS "pass" element provides a typical dropout voltage of only 85 mV at a load current of 60 mA, and typical quiescent current is only 45 µA at an input voltage of 6 V. The "sleep" current in standby mode on the A818SLU is less than 1 µA. Such a low dropout voltage permits deeper battery discharge before output regulation is lost. Moreover, the quiescent current doesn't rise as the dropout voltage is approached. Each device delivers a regulated continuous 3.3-V output at up to 75 mA under normal operating conditions, or 150 mA (transient) under worst-cases scenarios. They come in surface-mountable, small-outline, plastic transistor packages . *RE*

Allegro MicroSystems Inc., *Balfour House, Churchfield Rd., Walton-on-Thames, Surrey, KT12 2TD, England; phone: (44-1932) 253-355; fax (44-1932) 246-622.* **CIRCLE 592**

Testing 1, 2...New Modes For The 6113 Radio BTS Tester

By adding two new test modes to its 6113 digital radio base-station tester, Racal's instrument now should provide manufacturers and operators with a complete base-transceiver-station (BTS) solution. The in-service test facilities of the 6113's Base Station On-air Service System (BOSS) make it possible for digital radio network operators to monitor and make parametric measurements of base transceiver stations during normal two-way call traffic.

With its new R&D validation mode, the BTS system enables test and product support departments of network operators' and manufacturers' R&D organizations to develop a wide range of test scenarios, recreating specific faults or marginal conditions. The 6113's protocol generation and analysis system coupled with the Air Interface Monitor Emulation (AIME) software package converts a standard 6113 into an RF (Air Interface) protocol monitor/emulator. The combination of the 6113 BTS tester and AIME acts as a GSM mobile, supplying full logging and time-stamping of Layer 2 and Layer 3 signaling as well as the traffic on the uplink and downlink. *RE*

Racal Instruments, *P.O. Box 3620, Western Rd., Bracknell, Berkshire RG12 1WL, England; phone: (01344) 388000; fax (01344) 388061.* **CIRCLE 593**

Executive Editor Roger Allan's editorial in the Jan. 20 issue, "The Government And R&D Funding," elicited a number of responses. The following represents a sample of the feedback we received:

I am part of the "some in the private sector" that you mentioned who has an inherent "distrust" of the government. I was taught to be resourceful, thrifty, and practical. The government is none of these. It doesn't have to be, and will never have to be.

Anything that is worthwhile, desirable, and affordable, the free market can and will deliver. Why do you want the Government to make those decisions? If you accept the Government choosing the projects that are worthwhile, then you limit peoples' imaginations, turning them into followers and not leaders.

You also then accept all of the mandatory baloney that goes along with all government funds—like micromanagement of private companies, Affirmative Action "boondoggles," ISO 900X, Total Quality Management, and other worthless theories. Mandatory = required. And you thought this was a free country.

Let us keep our wages without these big government rip-offs. Freedom is the message we need.

Bruce Acker
via e-mail

I found your editorial very interesting and I think it's an important issue to bring up. Coincidentally, I was looking at some data on R&D in Israel. The Israeli government promotes R&D in industry (about 70% on electronics) within the framework of a special law. I think that this is one of the key elements contributing to the significant Israeli industrial growth.

You should take time to visit the Israeli government's homepage to get some more information on R&D. Their Internet address is: *http://www.israel-mfa.gov.il/facts/sci/fsci4.html.*

Tsipi Landen
Public Relations Manager
Chip Express

I'll tell you what I think about your editorial.

I think you must be a modern liberal; i.e., a radical egalitarian. Am I right?

Bert Sawyer
Arcadia, Calif.

I just read your Jan. 20 article on Silicon MEMS *("Silicon MEMS Technology Is Coming Of Age Commercially," p. 75)* and found it to be very informative. In case you ever write a follow-up article, you might be interested to know that SMC has dedicated its Wafer Fabrication Facility to offer foundry services to the MEMS industry. We're currently working with customers in the ink-jet print head and pressure sensor area and have produced over 20 million MEMS devices in the last five years. We think this service can be very valuable because there are a lot of MEMS startup companies that have sprung up from universities or other research groups, and our experience and infrastructure can help them get into high-volume production.

Douglas Finke
Vice-President and General Manager
SMC Wafer Foundry Business Unit

I felt compelled to write this note to congratulate you on your special report on Silicon MEMS technology. This is by far the most informative report I've seen on the subject.

I would be interested in any future writings you do on the this topic, particularly on non-silicon based MEMS and packaging of systems. You commented in your report that there is more to MEMs and microsystems than just silicon. I was one of the few at Kona that support the notion—from direct experience.

Dr. Robert Mehalso
President
Microtec Associates

I am trying to locate the proceedings from the Commercialization of Microsystems '96 Conference that you mentioned in your excellent article. I contacted SEMI, but they are not familiar with it. Please let me know where I can get a copy.

Dr. Robert N. Castellano
The Information Network

A limited number of Conference Proceedings are available on a first-come, first-served basis from:
Professor Steven Walsh
New Jersey Institute of Technology
School of Management
University Heights
Newark, N.J. 07102-1982
(201) 596-3294 (Telephone)
(201) 596-3074 (Fax)
e-mail: walshs@admin.njit.edu.

Incidentally, our apologies for not providing the right attributions to the Commercialization of Microsystems '96 Conference. Besides the Engineering Foundation and SEMI, who were mentioned in the article as co-sponsors, there were two other co-sponsors, The National Science Foundation and The New Jersey Institute of Technology. Dr. Steven Walsh of NJIT, as well as Dr. William Carr of NJIT and Dr. Robert Warrington of Louisiana Tech University, were the conference's three co-chairpersons.—Ed.

Lee Goldberg's Jan. 20 Technology Briefing *("To Infinity And Beyond!", p. 20)* struck home with me. I was one of many kids who grew up in the 1960s with the Apollo program as a major backdrop in my development, providing no shortage of inspiration to make science and engineering my career (even if I couldn't be the first man to set foot on Mars!).

Hopefully, the piece was written with tongue-in-cheek. Although I'd also like to see a resurgence of interest in space exploration, doing it by making a spectacle little different than professional wrestling ain't the way to do it. Finding a real mission is the first step.

As a kid, I was amazed every time I encountered an adult opposed to the Moon Program, claiming that the money could be better used for Earthly concerns. Sadly, I am close to becoming such an adult. Robotic spacecraft can do most, if not all, of our planetary and Earth-orbit exploration. As romantic as it is for the human spirit to send men and women into space, it just isn't cost-effective. Without an exciting goal which includes the direct involvement of people going into space, there isn't the dramatic impact that would be necessary to garner wide public support to subsidize the high costs involved in a resurgent space program.

Bill Lenihan
Hughes Aircraft Co.
El Segundo, Calif.

EE CURRENTS & CAREERS

Exploring employment and professional issues of concern to electronic engineers

What You And Your Company Can Expect From Each Other

Michael Sciannamea

With every passing day, new challenges are presented to both employers and the technical workforce. Factors such as global competition, deregulation, and the increased influence of financial leaders and investors have led many companies to dramatically change their employment practices. Downsizing and restructuring are now common in most organizations. As a result, workers, especially engineers, should expect that companies will act in their own self-interest.

For any company to grow and enhance its economic strength, it would seem that the effective nurturing of the relationship between the employer and employees would be paramount for success. That means having highly competent and dedicated engineering and science professionals on hand, and being able to attract new talent for future expansion.

But engineers everywhere have to adapt to the competitive atmosphere that now exists. Of course, they have to devote themselves to their job; however, they must be aware that anything can happen. They must realize that employers may have to make decisions that could adversely affect their careers.

So what does this all mean for you? And at the same time, you may be wondering what exactly does your employer owe you? Naturally, most engineers would expect to be paid a fair and decent wage for their work, but what else? What about issues such as job security, opportunities for advancement, or working conditions? At the same time, what should your employer expect from you? Obviously, they expect you to do your job, and to do it well. But what about issues such as staffing needs, intellectual property, performance appraisals, and productive practices?

It's In The Book

To provide a basis for discussion, the Institute of Electrical and Electronics Engineers (IEEE) has recently released its "IEEE-USA Guidelines for Professional Employment." It covers subjects such as career outlook, recruitment, ethics, compensation, intellectual property, and performance appraisals, from both the standpoint of the employer and of the engineer. It outlines the interests and objectives of individuals and organizations. The guidelines have been designed to help employers and technical professionals foster mutually satisfactory relationships.

But according to Paul J. Kostek, Chair of the IEEE-USA Career Policy Council, the publication is exactly what it is meant to be—a guideline. "The IEEE does a great job of writing standards," says Kostek, "but not company rules. This publication is specifically designed to encourage dialogue between engineers and their employers."

The guidelines are a direct result of research conducted by leaders in industry, academia, human resources, and company management. It also is a combination of two previous IEEE-USA documents; one that dealt with professional practices, and the other that focused on engineers in the workplace. Kostek hopes that this new publication will inspire engineers to pay more attention to their careers and their roles in their companies. "Engineers should be more proactive instead of reactive," he says.

Employment Conditions

Evidence suggests that the interests of both engineers and their employers would be best served if the following factors are in place at any given organization: Belief in the company's product and the importance of the employee's role in the company's success; a fair amount of employment stability; a system that gives fair and equitable monetary credit to all who have participated in the company's success; and an environment that demonstrates to young people (students) that engineering is a good career choice.

Of course, no organization is perfect. Various circumstances can and will affect how employers and employees approach their roles. For example, the XYZ Company, after years of increasing sales and high profits, is undergoing some financial difficulties. What will management do? What can the employees expect?

As previously mentioned, the guidelines do not provide definitive answers. However, they give people on both sides something to consider. The guidelines suggest that employers should practice good-faith measures such as staffing conservatively to avoid short-term cycles of hiring and layoff. They also suggest using temporary measures such as four-day work weeks or temporary across-the-board pay cuts to avoid cyclical layoffs.

But engineers must adapt to these kinds of situations as well. They can't assume that a job will last forever, or that the company will take care of them in dire circumstances. In that case, the guidelines suggest that engineers must continuously improve their skills, and should take responsibility for developing their own careers and professional growth. In other words, they should be prepared to face the employers' ever-changing business and technical needs.

That Delicate Balance

Kostek says that even though the guidelines are geared toward engineers that are currently employed, he indicates that university students are keeping a close eye on the industry.

"Younger people know what's going on," he says. "Most colleges and universities today teach their engineering students that they have to be prepared for anything when they venture into the workplace."

One area that attracts an increasing amount of discussion is how engineers should balance work against their outside interests. The question that seems to be on every employer and employee's mind is: How much work is too much? The answer is that there is no answer. Every employee and employer's situation is different.

While the guidelines don't specifically address how to achieve "that delicate balance," it does indicate that employers should show concern for the well-being of their employees by offering flexible working periods (when possible), suitable working conditions, and stable employment. Employees, on the other hand, should be able to realize the constraints and trade-offs associated with their jobs, such as overtime. The guidelines also suggest that employers should not use unpaid overtime from salaried personnel to make up for insufficient assigned personnel or inadequate project planning.

Kostek notes that in the past, young engineers would offer to work outrageous hours. They worked long hours not only to get the job done, but also to show their bosses that they had initiative. "That's no longer the case," says Kostek. "Unlimited overtime is not wanted by younger workers. They want a career, but they also want time for a family."

Ethics In The Workplace

To be successful, most employers find that it is only in their best interest to require all managers and employees to conduct themselves as professionals and adhere to strict ethical standards. The guidelines point out that defining what is right and what is wrong is often subject to individual interpretation. It suggests that ongoing communication between employers and employees is essential so as to establish boundaries of ethical behavior in their own individual organization.

Since ethical issues are not always clear-cut, conflicts should be resolved within the organization, usually through an established review process. The IEEE-USA suggests that company policies should conform to all applicable laws and regulations of the country in which the company resides. In addition, these policies should not conflict with the Codes of Ethics of their employees' professional societies.

But engineers have to hold up their end of the bargain, too. If a situation occurs, they must be able to fully cooperate to achieve a mutually agreeable solution. Engineers also are expected to separate from employers whose ethical behavior is unacceptable.

The guidelines are intended for engineers and their employers to understand the current and future conditions of the workplace.

One area that wasn't specifically addressed in the guidelines is sexual harassment in the workplace. Kostek notes that companies have to take it upon themselves to make sure that harassment of any kind is not tolerated at any time. "There are times when it should be understood, and you don't need to write it down," he says.

How'm I Doin'?

Many engineers are interested in knowing if their employers think that they're doing a good job. By their very nature, performance appraisals are very subjective. For the organization to advance, performance feedback needs to be given when praise is deserved or the need for improvement arises, and not just at predetermined review periods. Without an appraisal process, judgements on pay raises, promotions, and separation will be deemed covert and may surprise, even shock, the employee.

"Performance appraisals were not always looked on as an important factor in the workplace," says Kostek. "But without knowing how you're doing, an employee will not take the initiative necessary to improve, and the employer will not be able to achieve its goals."

The IEEE-USA guidelines suggest that employers should offer a formal, written performance appraisal process. The appraisals should be based on previously agreed-upon goals and objectives, both for progress on the job and the employee's personal growth. Engineers should learn what is expected from them, and view the appraisal process as an opportunity to provide valuable input. They need to see how their performance affects the relationship between improving the product and emphasizing productivity and profitability.

During the course of a typical engineering career, engineers may have the opportunity to advance from a technical to a managerial position. The IEEE says that employers should let employees know what the process is in selecting someone for a managerial position. It also suggests that companies should promote from within whenever possible, so as to give current employees an opportunity to achieve personal goals. On the other hand, engineers should realize that with a promotion to a managerial position comes increased responsibility.

As mentioned previously, the guidelines are not intended to be the hard and fast rules that all technical organizations and engineers have to live by. But they are intended to help both parties clearly understand the current and future conditions of the workplace. These guidelines can provide insight and guidance toward behavior that will be beneficial to both the company and the employees.

The "IEEE-USA Guidelines for Professional Employment" is available for $6.95 each for IEEE members, and $8.95 for nonmembers. To obtain a copy, contact the IEEE United States Archives, IEEE-USA, 1828 L St., Suite 1202, Washington, DC 20036-5104; (202) 785-0017; fax (202) 785-0835; Internet: http://www.ieee.org/usab.

Michael Sciannamea is chief copy editor at Electronic Design.

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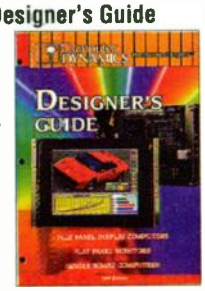

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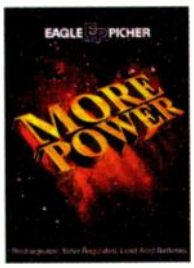

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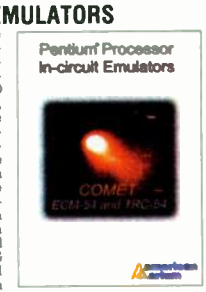

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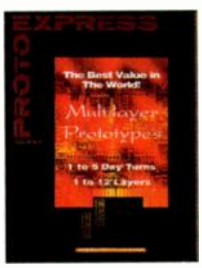

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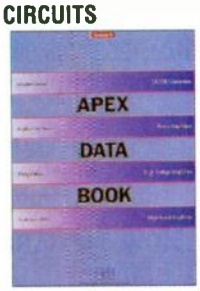

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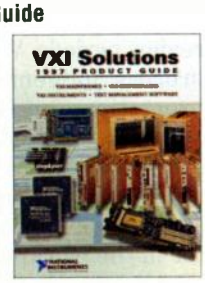

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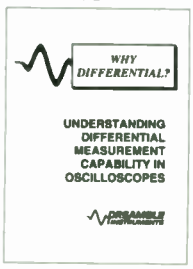

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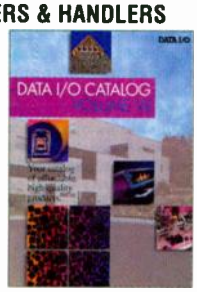

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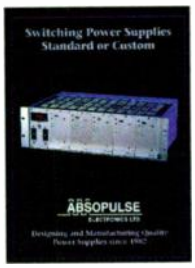

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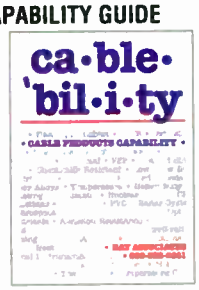

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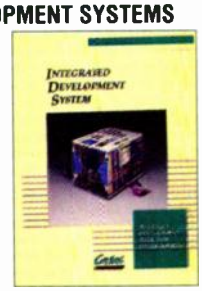

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APPLICATION NOTE

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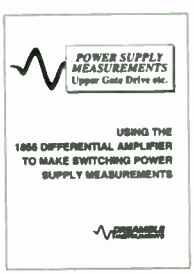

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PREAMBLE INSTRUMENTS

ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

HARTING har-mik

Harting har-mik 4 color brochure shows and describes comprehensive range of 0.050" pitch miniature connectors designed to meet the requirements of Internal and External connections of the future. Reduced size: contact density. 847/519-7700 or Fax: 847/519-9771.

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HARTING ELEKTRONIK, INC.

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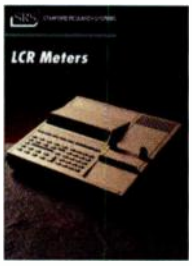

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ROLYN OPTICS CO.

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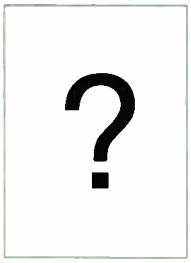

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W65C02S - BASED PRODUCTS

Western Design Center's product selection and developer guide describes our 65C02-BASED CMOS low power IC microprocessors. Included is information about our chips, boards and licensable cores.

www.wdesignc.com.

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INNOVATIVE INTEGRATION

BATTERIES WITH A FUTURE

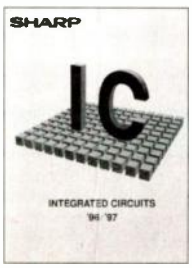
Eagle-Picher covers their line of Keeper II lithium batteries, designed for standby applications where long-life is required in this 4 page brochure. Specifications, diagrams of internal construction and graphs of discharge characteristics supplement the detailed listing of features of these batteries.

CIRCLE 302

EAGLE-PICHER INDUSTRIES, INC.

SHARP FIFOs

First-in, First-out memories are just the stuff the no-nonsense design environment of the '90s is meant to build on. Used as data buffers between systems operating at different speeds, FIFOs conserve valuable board space, streamline design tasks and reduce system cost. Sharp's new 1997 IC Short Form Catalog is packed with information about Sharp FIFOs.



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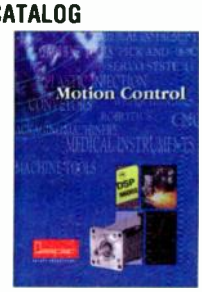
SHARP MICROELECTRONICS

MOTION CONTROL CATALOG

GESPAC' intelligent motion controller uses a 40MHz MC56002 DSP to control 2 or 4 DC, AC or brushless motors. Versions of the board are available for the VME, G-64 and soon for the ISA and Compact-PCI buses. The board comes with a powerful PC based software package that helps you automatically determine the mechanical characteristics of the drive assembly and more.



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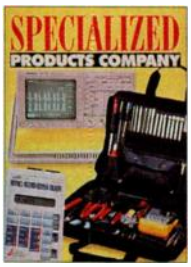

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NEW TEST & MEASUREMENT CATALOG

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KEITHLEY INSTRUMENT

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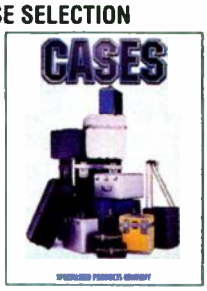

CIRCLE 263

SPECIALIZED PRODUCTS COMPANY

YOUR NEW PRODUCTS INFORMATION SOURCE

EE Product News

Time-to-market is critical. But to succeed in today's intensely competitive electronics marketplace, products must be made up of the "right stuff"—the right semiconductors, power sources, passive components, connectors, etc.

Each month, EEPN's editorial staff reviews thousands of these devices and components, as well as hundreds of design, assembly and test products, and selects those it feels can play an important role in differentiating your designs from your competitors'.

For the time-to-market-conscious engineer, the time to read EE Product News is each and every month.

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. . . helps get you to market first with the best design.

Next month, EEPN will publish special sections on these four product categories:

- **ROMs, PROMs, EPROMs, EEPROMs & Flash Memories (monolithic & memory modules)**
- **Passive Components (Resistors, Capacitors, Etc.)**
- **Optoelectronic Components**
- **CAE/CAD Software**

And during the next quarter of '97, we'll bring you information on 12 other highly active areas of the new products mart:

APRIL

- Microcontrollers & Related Chipsets
- Power & Battery-Management ICs
- Cooling Products
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- Prototying Products

MAY

- Audio, Video & Multimedia ICs
- Cabinets & Enclosures
- Booth-By-Booth Guide To New Products Debuting at the New England Electronics Industry Forum (formerly Electro)
- Test & Measurement Accessories

JUNE

- Discrete Semiconductors
- Displays & Indicators
- Wire & Cable & Assemblies

LATE-BREAKING PRODUCT NEWS & DISTRIBUTORS' CORNER

And to help you get to market fast with the right design, *EE Product News* has added to its extensive lineup of special sections two new pages: Late-Breaking Product News to give you information on important new products entering the marketplace at press time; and Distributors' Corner to keep you informed of the availability of products through distribution channels.

These two pages, plus *EE Product News'* existing Product-Related News page, which reports on new sources of products and services, help make *EE Product News* your complete new products publication.

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- *Silicon - GaAs*
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- *Knowledge of RF product and test attributes*
- *RF circuit technologies*
- *Assembly and test technologies*

RF SENIOR ELECTRICAL ENGINEERS

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- *RF Product design and development*
- *S-Parameter theory*
- *AC circuit design*
- *Simulator tools*

RF DEVICE MODEL ENGINEERS

- *RF device characterization*
- *Model extraction*
- *Maintenance of device model libraries*

RF APPLICATIONS ENGINEERS

- *RF Systems knowledge, Wireless Terminals/Infrastructure (Amplifier design and test)*
- *Device definition and planning*
- *RF products knowledge*
- *Characterization of new products/ systems/circuits*
- *Intimate knowledge of customer requirements*

SENIOR RF PRODUCT MANAGERS

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SBL-1-1	0.1-400	5.5	45	40	+7	7.25
SBL-3	0.025-200	5.5	45	40	+7	7.25
• SBL-11	5-2000	7.0	35	30	+7	18.75
SBL-1LH	2-500	5.8	68	45	+10	5.65
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• SBL-1XLH	10-1000	6.0	40	55	+10	7.25
SBL-2LH	5-1000	5.9	61	54	+10	8.20
SBL-3LH	0.07-250	4.9	60	53	+10	8.20
• SBL-11LH	5-2000	7.0	45	30	+10	19.70
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SBL-1ZMH	2-1100	6.5	40	25	+13	11.70
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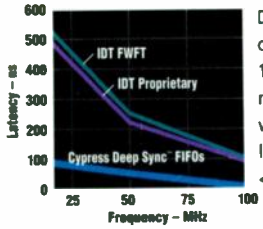

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"They" said it couldn't be done, but we did it anyway—broke through the density barrier with *standard-pinout* synchronous FIFOs. Cypress's CY7C4261/71 16K/32K × 9 and CY7C4255/65 8K/16K × 18 Deep Sync™ FIFOs offer the speeds and densities you need for high-bandwidth applications using the same industry standard synchronous (clocked) architecture used for lower-density sync FIFOs.

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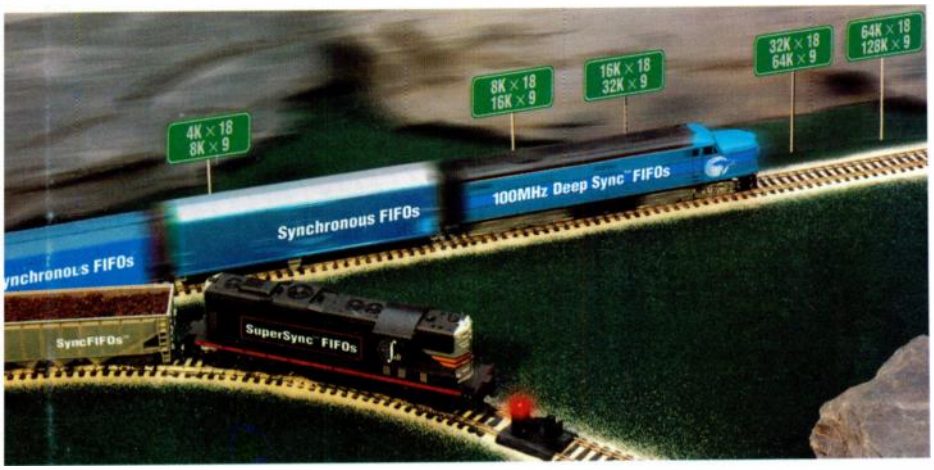

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No redesign. No timing issues. No pinout changes. No need to learn a new architecture. Just plug our Deep Sync FIFOs into your existing board to achieve the highest performance possible. No other FIFO supplier makes it this easy to upgrade your buffering solution!

The First-Word-Fallthrough Fallacy

Don't be fooled by FIFO features hype. Why should you wait 12.5 clock cycles for the first word of data when you can get it (and all the rest!) in less than 2 cycles? That's a savings of almost 500 ns!

Standard Sync FIFO Buffering Solutions for Today *and* Tomorrow

If you're looking for sync FIFOs offering the highest densities, fast cycle times, small packaging, low cost (less than $1/KByte), and the fastest time-to-market, look no further than Cypress. Our roadmap will keep you on track with devices that are deeper and wider, yet still socket-compatible with standard sync FIFOs.

Deep Sync FIFO Feature Comparison

IDT	CYPRESS	CYPRESS ADVANTAGE
Sync Architecture		
Proprietary FWFT	Industry Standard	All Cypress sync FIFOs are pin-compatible
Frequency Select Pin		
FS Select pin	Clocks can be async	Does not limit range of operation
Depth Expansion		
Serial cascade	Token passing	Low latency and low power
Power (f=20MHz)		
×18: –180mA ×9: –150mA	–100mA –50mA	Lower power Lower power
×9 Package		
10 × 10 TQFP	7 × 7 TQFP	Smallest ×9 packaging for all sync FIFOs

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