# ELECTRONIC DESIGN

FOR ENGINEERS AND ENGINEERING MANAGERS - WORLDWIDE

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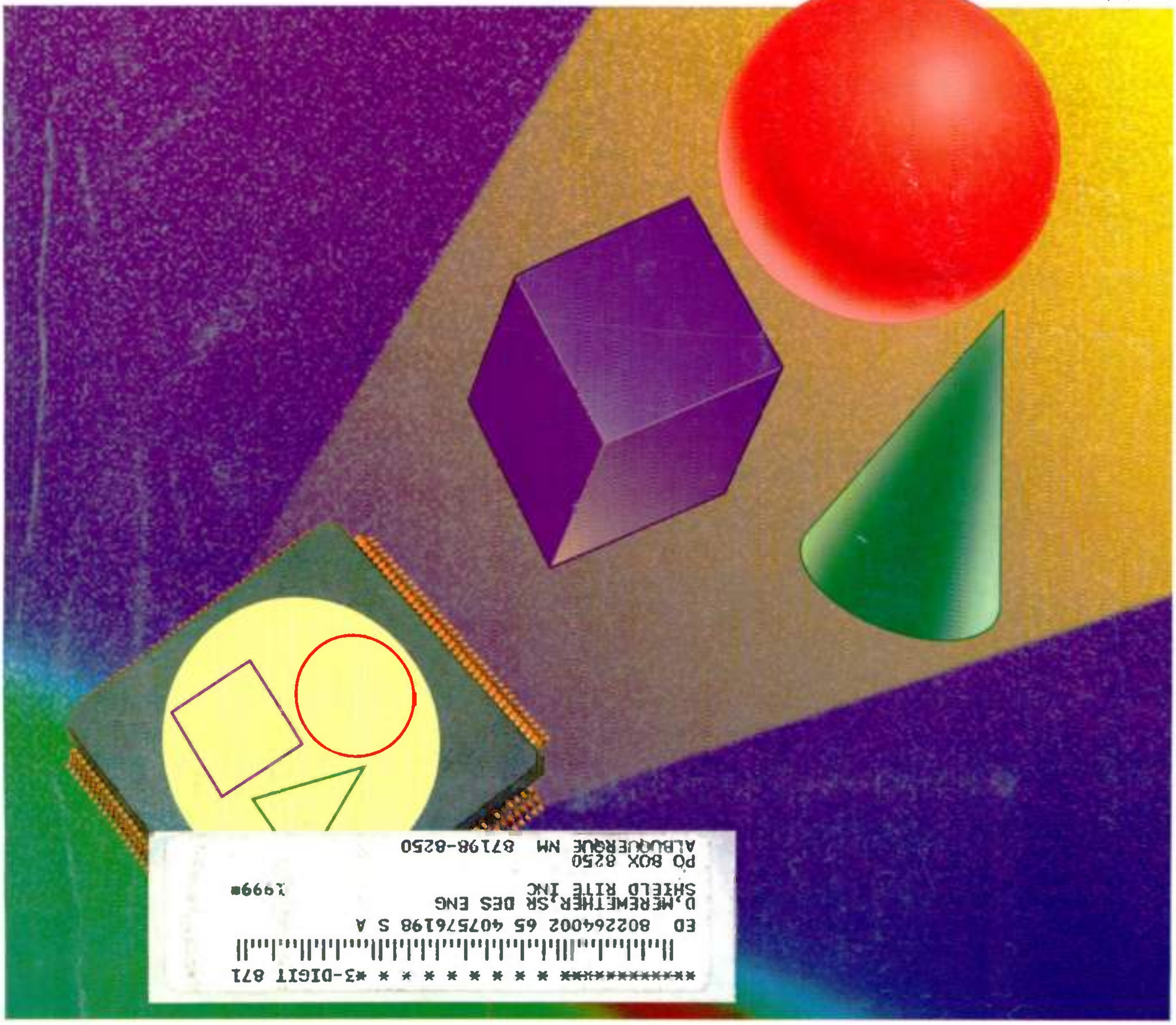
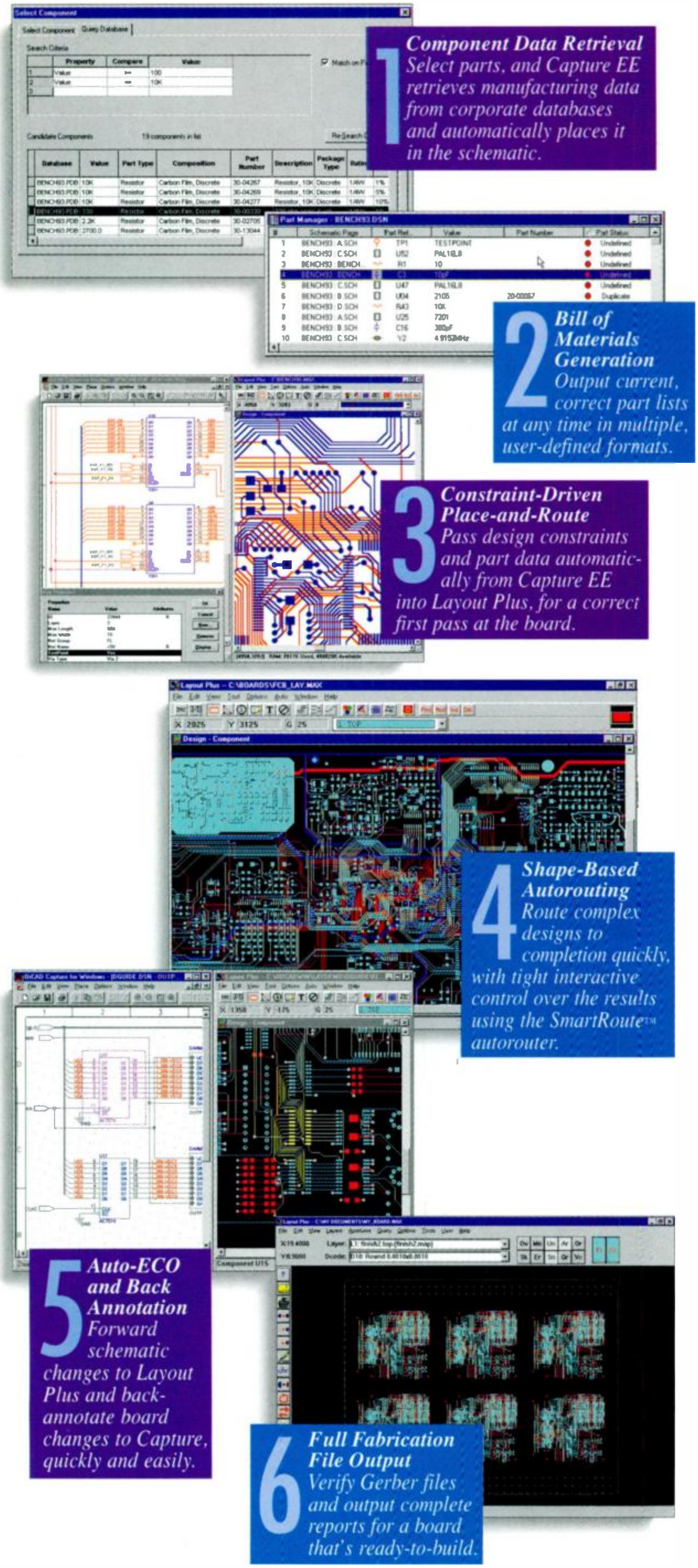
May 1, 1997



## 3D Accelerator Chip Adds A Third Dimension To 2D Graphics p. 83

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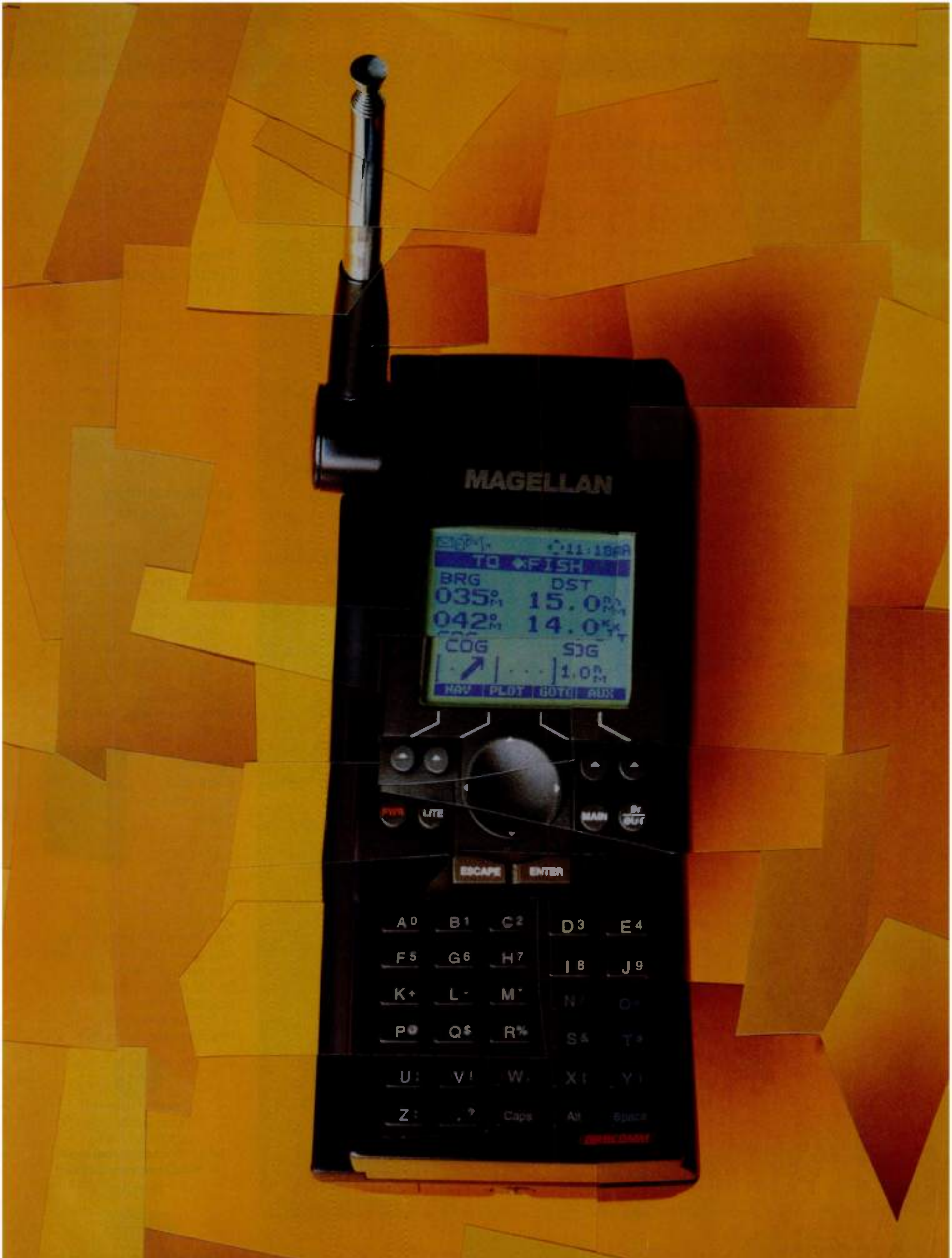
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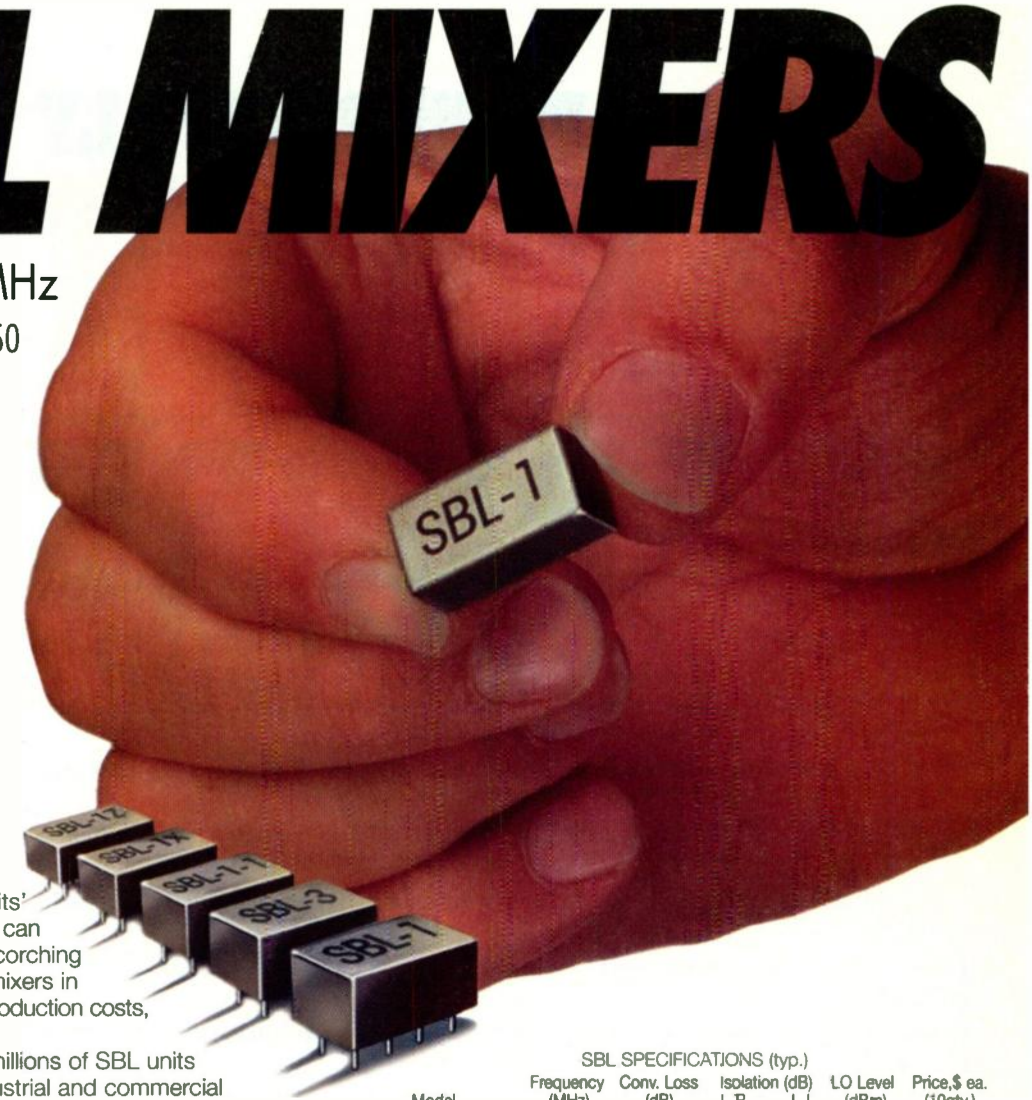


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F 143 Rev A

# ELECTRONIC DESIGN

*May 1, 1997 Volume 45, Number 9*

## EDITORIAL OVERVIEW



### TECH INSIGHTS



### TECH INSIGHTS



### DEPARTMENTS



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# ELECTRONIC DESIGN

May 1, 1997 Volume 45, Number 9

## EDITORIAL OVERVIEW



COVER ILLUSTRATION BY:
BRUCE JABLONSKI



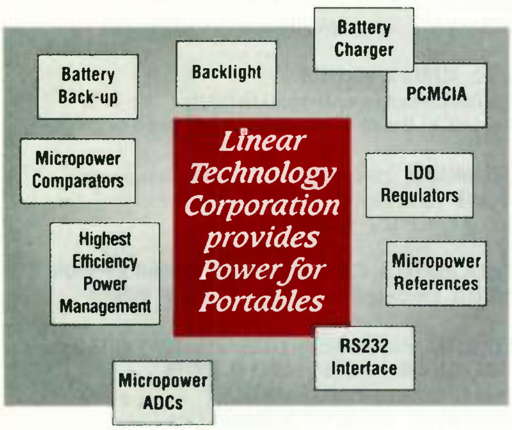
Jesse H. Neal Editorial Achievement

| | |
|---|---|
| 1967 First Place Award | 1978 Certificate of Merit |
| 1968 First Place Award | 1980 Certificate of Merit |
| 1972 Certificate of Merit | 1986 First Place Award |
| 1975 Two Certificates of Merit | 1989 Certificate of Merit |
| 1976 Certificate of Merit | 1992 Certificate of Merit |

# LTC1439: Multiple Output, High Efficiency, Low Noise Synchronous DC/DC Controller


Linear Technology's new LTC®1439 multiple output DC/DC controller offers breakthrough technology advancements that make designing notebook computers and other portable electronics easier. Now you can add the multimedia and communications features you want without worrying about noise and efficiency tradeoffs. Here are just some of the breakthroughs offered by the LTC1439:

- The exclusive Adaptive Power™ output stage delivers high efficiency and low quiescent current (<300μA) while maintaining constant frequency over two decades of load current.
- Dual controllers drive N-channel power MOSFETs exclusively and operate at up to 99% duty cycle for extremely low dropout.
- Extra output voltages are easily added thanks to a linear regulator controller and secondary winding feedback loop.




- The start-up sequence is fully programmable and an internal power-on-reset (POR) timer is provided.
- A true Phase-Locked Loop (PLL)allows shifting the switching frequency or synchronizing it to an external source.
- Industry's broadest input voltage range: From 3.5V to 36V.

### *New DC/DC Controller Family Powers Portable Electronics*

Does your portable product need single, dual, or multiple output voltages with high efficiency and low noise? Linear Technology has you covered with our complete LTC1439 DC/DC controller family.

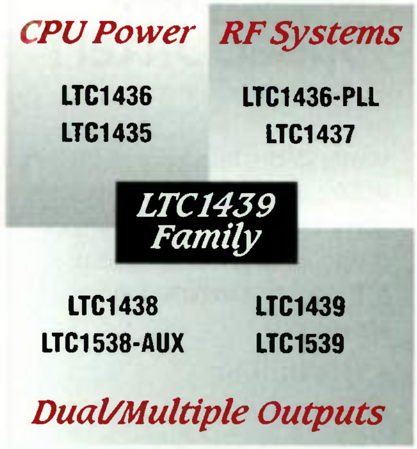
All members of the family drive N-channel power MOSFETs in a fixed-frequency current mode architecture. Some of the devices feature Adaptive Power operation which maintains a constant operating frequency while reducing switching losses at low output currents.

An auxiliary linear regulator controller can be used to add additional low noise, low dropout output voltages such as 2.9V or 12V. And a special secondary feedback pin allows secondary windings to be regulated independent of the primary load.

Most of the LTC1439 family include a power-on-reset (POR) timer which generates a signal delayed by $2^{16}$ switch cycles after the output is in regulation. An additional comparator is also available for use as a low battery comparator.

Complete control of the operating frequency is available. You can choose the frequency, shift it over a 2:1 range, or synchronize using a self-contained phase-locked loop (PLL). Preset 5V and 3.3V outputs are available, or output voltages may be adjusted over a 1.2V to 9V range. Output currents may be programmed from 500mA to 10A.

You are also in control of regulator start-up. Separate run pins for each DC/DC and linear controller allow complete freedom in supply sequencing. Dual controller versions are available which shut down all functions to a minuscule 15μA supply current or




leave a 5V standby regulator and auxiliary comparator active for keep-alive applications.

LTC1439 family members are available in a variety of surface mount packages including SO (narrow), QSOP, and SSOP styles.

### *Portable Power Control: A Full Range of Solutions*

The LTC1439 family is only the latest in Linear Technology's wide selection of power control products for portable electronics. Some of the other product families available include battery chargers, battery-backup controllers, PCMCIA switching matrices, and power management switches.

For more information on the LTC1439, contact Linear Technology Corporation, 1630 McCarthy Blvd., Milpitas, CA 95035. 408-432-1900. Fax: 408-434-0507. For Literature only, call 1-800-4-LINEAR.

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## MAY 1997

**47th Electronic Components & Technology Conference, May 18-21.** The Fairmont Hotel, San Jose, CA. Contact Jim Bruorton, Electronic Industries Association, 2500 Wilson Blvd., Arlington, VA 22201-3834; (864) 963-6621.

**Finishing '97 Conference & Exposition, May 19-22**. Rosemont Convention Center, Rosemont (Chicago), IL. Contact Society of Manufacturing Engineers; (800) 733-4763.

**19th IEEE International Conference on Software Engineering, May 19-23.** Boston, MA. Contact W. Richard Adrion, Dept. of Computer Science, University of Masachusetts/Amherst, 307 LGRC, P.O. Box 34610; Amherst, MA 01003-4610; (413) 545-2742; e-mail: adrion@cs.umass.edu.

**IEEE Instrumentation & Measurement Technology Conference (MTC '97), May 20-22.** Chateau Laurier, Ottawa, Ontario, Canada. Contact Robert Myers, Conference Coordinator, 3685 Motor Avenue, Suite 240, Los Angeles, California 90034; (310) 287-1463; fax (310) 287-1851; e-mail: bob.myers@ieee.org.

**OEMed Midwest, May 21-22.** Rosemont Convention Center, Rosemont, IL. Contact Exposition Excellence Corp., 112 Main St., Norwalk, CT 06851; (203) 847-9599; fax (203) 854-9438.

**OEM Electronics Midwest, May 21-22.** Rosemont Convention Center, Rosemont, IL. Contact Exposition Excellence Corp., 112 Main St., Norwalk, CT 06851; (203) 847-9599; fax (203) 854-9438.

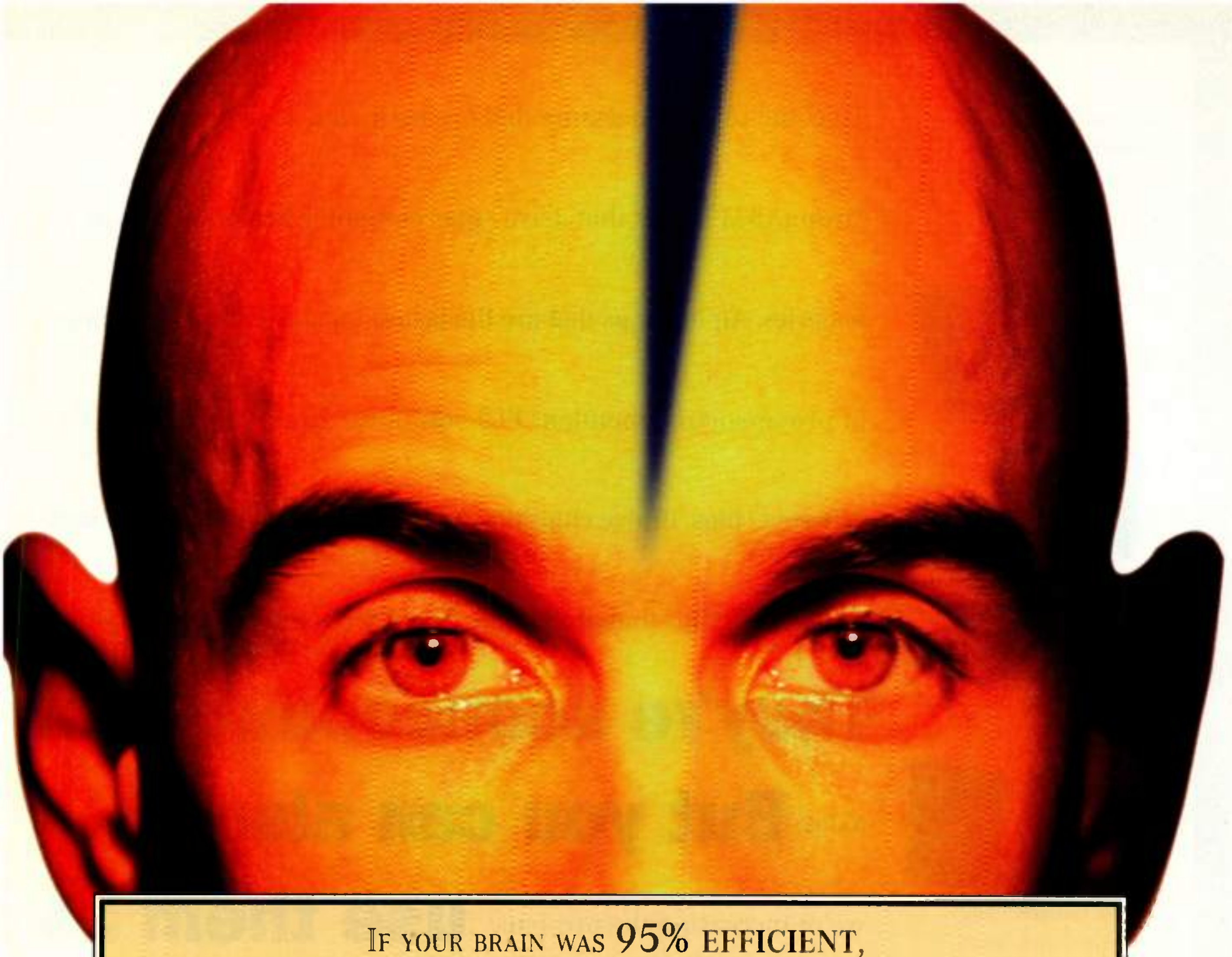
**Canadian Conference on Electrical & Computer Engineering, May 25-28.** Delta Hotel, Newfoundland, Canada. Contact David Collett, Newfoundland & Labrador Hydro, P.O. Box 12400, St. Johns, NF, A1A 4K7, Canada; (709) 737-1372; fax (709) 737-1782; e-mail: t.d.collett@ieee.org.

**Fifth IEEE International Conference on Properties & Applications of Dielectric Materials (ICPADM), May 25-30.** Sheraton Walker Hill, Convention Center, Seoul, Korea. Contact Joon-Ung Lee, Department of Electrical Engineering, Kwangwoon University, 447-1 Wolgye-Dong, Nowon-Ku, Seoul, 139-701, Korea; (82)-2-910-5144; fax (82)-2-942-0107.

**Next Generation Telephony West: Voice Over the Internet, May 28-30.** Hotel Monaco, San Francisco, California. Contact (800) 822-6338 or (202) 842-3022 ext.317; Internet: http://www.brp.com.

## JUNE

**IEEE International Conference on Neural Networks, June 1-5.** Houston, TX. Contact Nicolaos B. Karayiannis, Dept. of Electrical & Computer Engineering, University of Houston, Houston, TX; 77204-4793 (713) 743-4436; fax (713) 743-4444.



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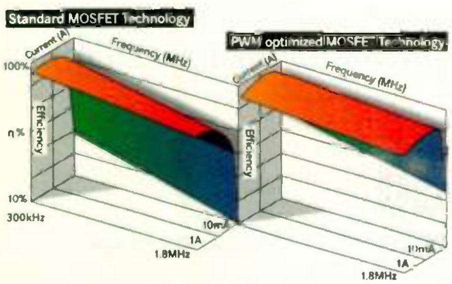


Our MOSFETs can significantly raise DC/DC conversion efficiency from 85% to as high as 96.2843%. And what can you do with that? Create smaller, lighter products, extend battery life of current products, or develop something in between. In other words, anything your cerebellum can come up with.

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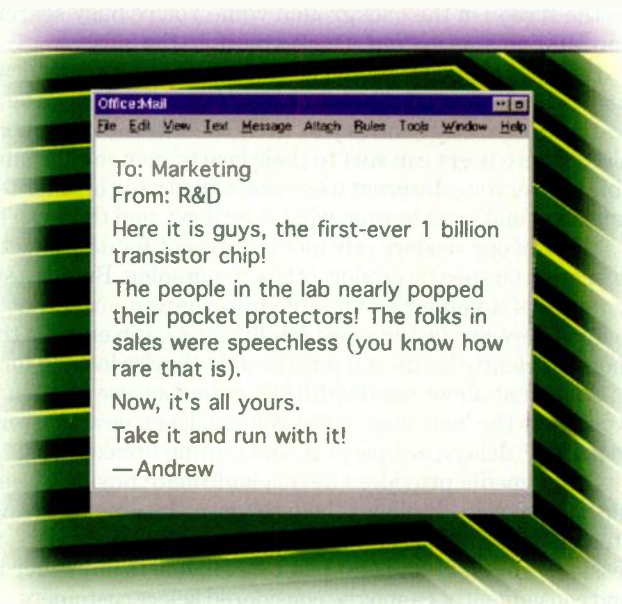


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# The Internet: Push Or Pull?

A new word has been added to the jargon of Internet users and on-line content providers: push. The word has been splashed on the covers of *Business Week* and *Wired* magazines, on the front page of the *Wall Street Journal*, and in the Business Section of the *New York Times*, to name a few publications. Just what is push technology? It's the idea that Internet content providers will push data directly to an Internet user over specialized channels, rather than having that user "pull" the data from the Internet at his or her convenience. For example, if you want the latest weather forecast, you shouldn't have to search for it. It should come directly to your screen. The same goes for news, sports results, stock market data, etc. Web browsers could have this kind of information on the screen in the background while you're busy searching the Internet for hard-to-find information. There's merit to the idea.

But if it's pushed too far, it sounds to me like TV broadcasting. Just give them soap operas, G-rated movies, or whatever all day, and the users will come. This scenario is exactly contrary to what the Internet was meant to be all along—a place where users can surf to their hearts' content, for information that's available to everyone. Internet users don't need a big brother telling them what they can have (and by extension what they don't, and thus, can't have).

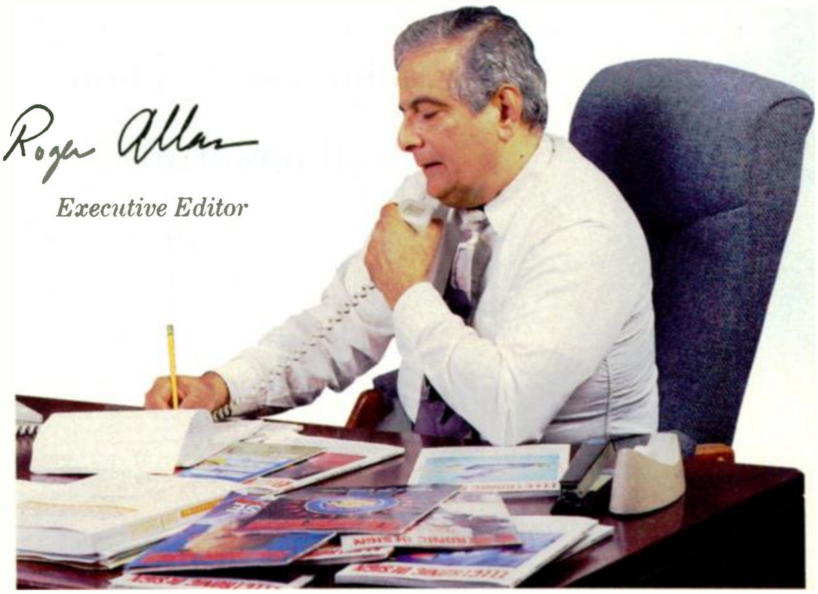
Many of our readers rely on the Internet for data sheets and applications information on specific products they're pursuing. But it's a sure bet they wouldn't want all of a vendor's available information pushed at them. What's really needed here are faster, more-intelligent search engines that let Internet users more efficiently locate and pull the data they're looking for.

And what about bandwidth? Overzealous use of push technology certainly won't help the 'net congestion problem. Even now, most net users are resigned to periodic delays, lost packets, and routing breakdowns.

Large media providers have a legitimate business reason for championing push technology. It allows them to target Internet users as true subscribers instead of mere hits. However, these same Internet users, whether they're professionals or amateurs, are just as available to any other information provider, and consequently, cannot be considered select customers.

In the long run, the push approach risks alienating Internet users by turning them off with a flood of information they can't follow. Many of us have already experienced information overload by merely subscribing to a few e-mail lists and e-zines about topics that really interest us. I think it's far better to have an open Internet environment than one dominated by a handful of large media providers. What do you think? *rallan@class.org.*

Roger Allan
*Executive Editor*

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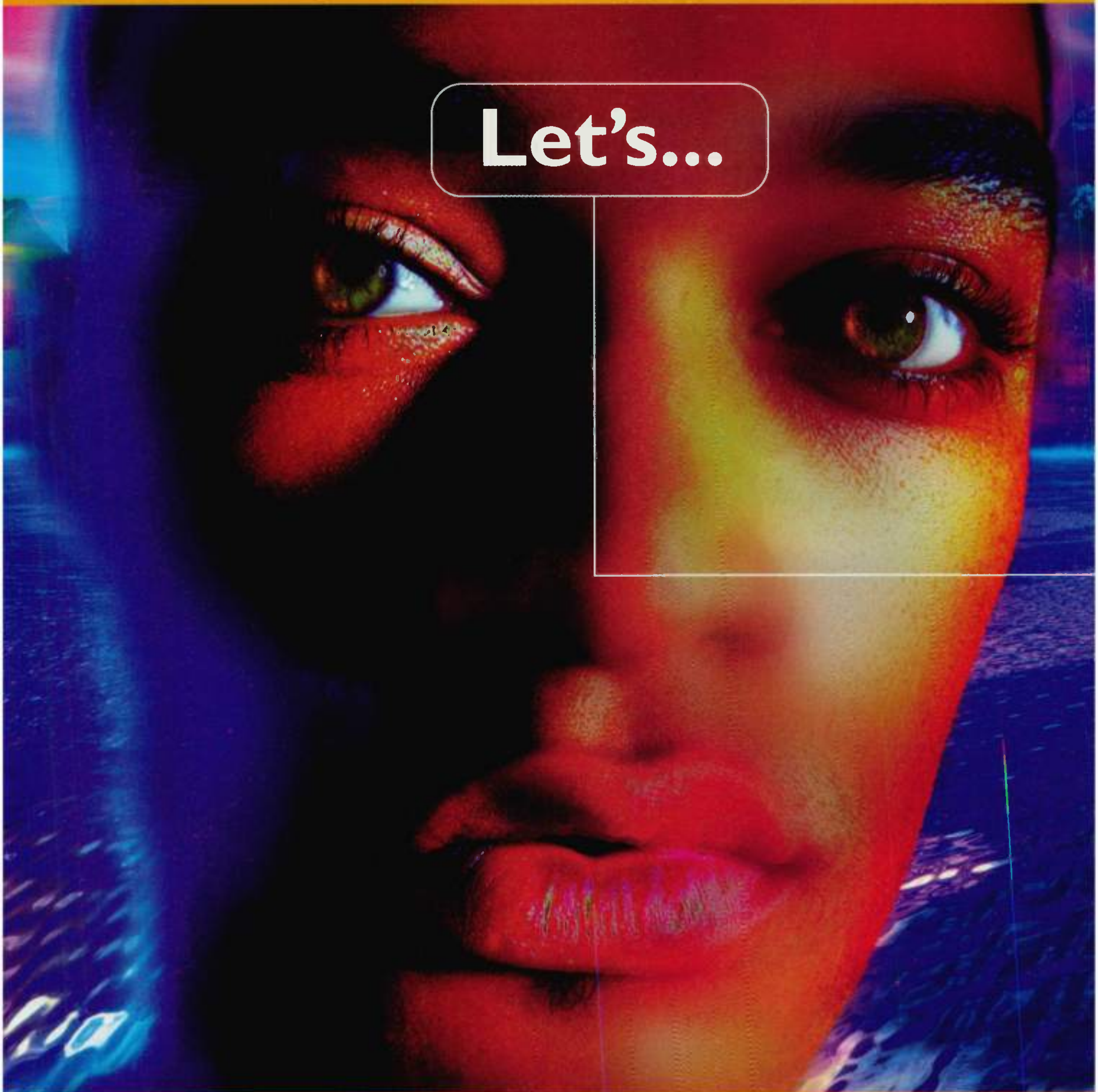
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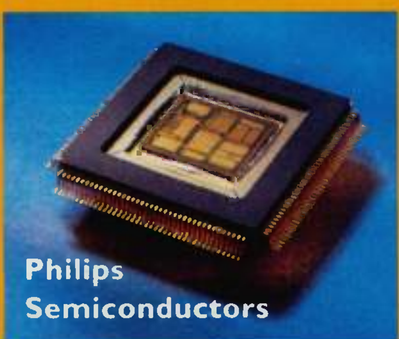
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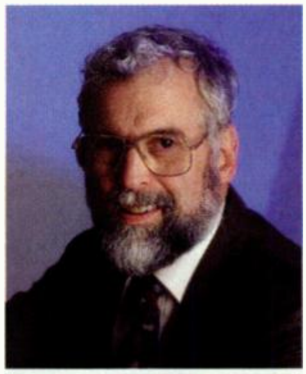
# The "Crazy Aunt In The Basement"

During his first Presidential campaign, Ross Perot revived an image that has been latent in the American mindset. It was that of the "crazy aunt who lives in the basement. Everybody knows she's there, but nobody talks about her." Perot was alluding to issues of the economy, but this image of dysfunction and denial can be applied to other areas, such as software tools and software quality.

One of the distinct messages I got from the recent Embedded Systems Conference in Boston was that there is a growing dissonance between what people expect to be able to do with tools and what they expect to pay for them.

I admit to being one of those who rejoiced that the advent of Windows as a serious development environment would stimulate expectations for tools significantly lower in price than those available under Unix. This somewhat naïve notion was based on the existence of several very fine C++ integrated development environments, all priced around $500.

While the Windows-based C++ IDEs are all excellent products, they sell in very high volumes that cannot be compared to the more specialized tools needed by embedded developers. Yet the expectation of many developers still is that such tools should be, to put it bluntly, cheap. Indeed, there has been a tendency for many embedded tool vendors to try to bring the first generation of their Windows-based products in at significantly lower prices than those products' Unix counterparts. This has not been a long-term advantage.



TOM WILLIAMS
Embedded Systems/Software

Given the prevalence of some genuine horror stories of cost overruns, missed ship dates and just plain failed projects, it seems time we rethink some of the stories we've been telling ourselves around the crazy aunt in the basement. The point is, we know she's there just like we know that investment in quality up-front can save us a fortune in the long run. But experience in the trenches shows it's not as rosy as we'd like to believe.

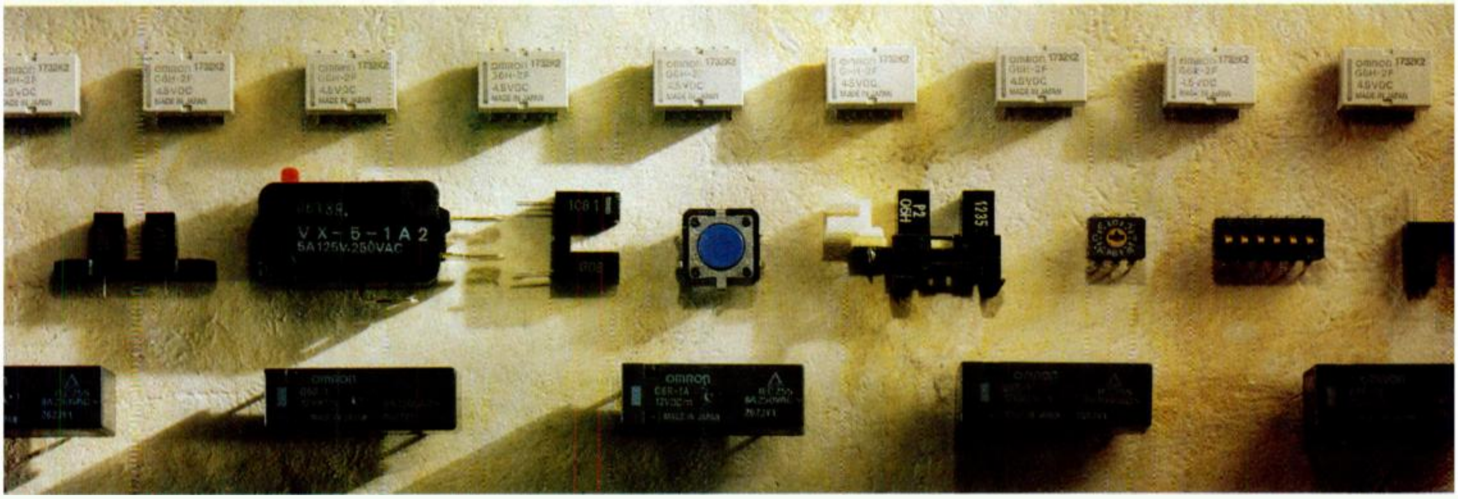
How does one really evaluate the quality or usability of a given tool, and also the ability to use that tool with other tools? Or whether that tool is really appropriate to the job at hand? When things don't go right, how do you figure out, or—more importantly—how long does it take to figure out what is wrong? Have you discovered some problem with a compiler the vendor didn't realize was there? Is there some reason the TCP/IP stack you bought doesn't want to work with the RTOS you think it should work with?

How much expensive engineering talent has to sit on the phone with another vendor's support people? And, having spent time getting tools to work, is your organization now under pressure to rush development or not test quite as much in order to meet the implacable deadline? Thus does the disease ultimately spread to the hands of the end-user?

And from a vendor's point of view, what is the cost of all those incoming support calls? What is the real cost of a bug that goes out the door? Well, we know the answer to these rhetorical questions, don't we? Whatever the actual numbers, the answer is: "A heck of a lot more than investing in quality tools and thorough testing in the first place." Yes, we all know it, but like the crazy aunt in the basement, we haven't really wanted to acknowledge it, looking for maybe a way around the cold, hard fact.

It's understandably scary to be the first vendor to say, "Yes, my tool costs $32,000, but it will absolutely pay for itself many times over in terms of reliability, thoroughness, ease of use and meeting time-to-market requirements." The alternative, however, is a dynamic, vibrant industry that could be ever so much more so if it weren't squandering millions in productivity trying to retro-fix things that should already work. It's a huge problem, but the only way to start solving it is to frankly admit to ourselves that it exists. *(Tom William's e-mail address is: tomwillm@ix.netcom.com.)*

# If You Think Omron Only Makes Relays, Read Between Our Lines.

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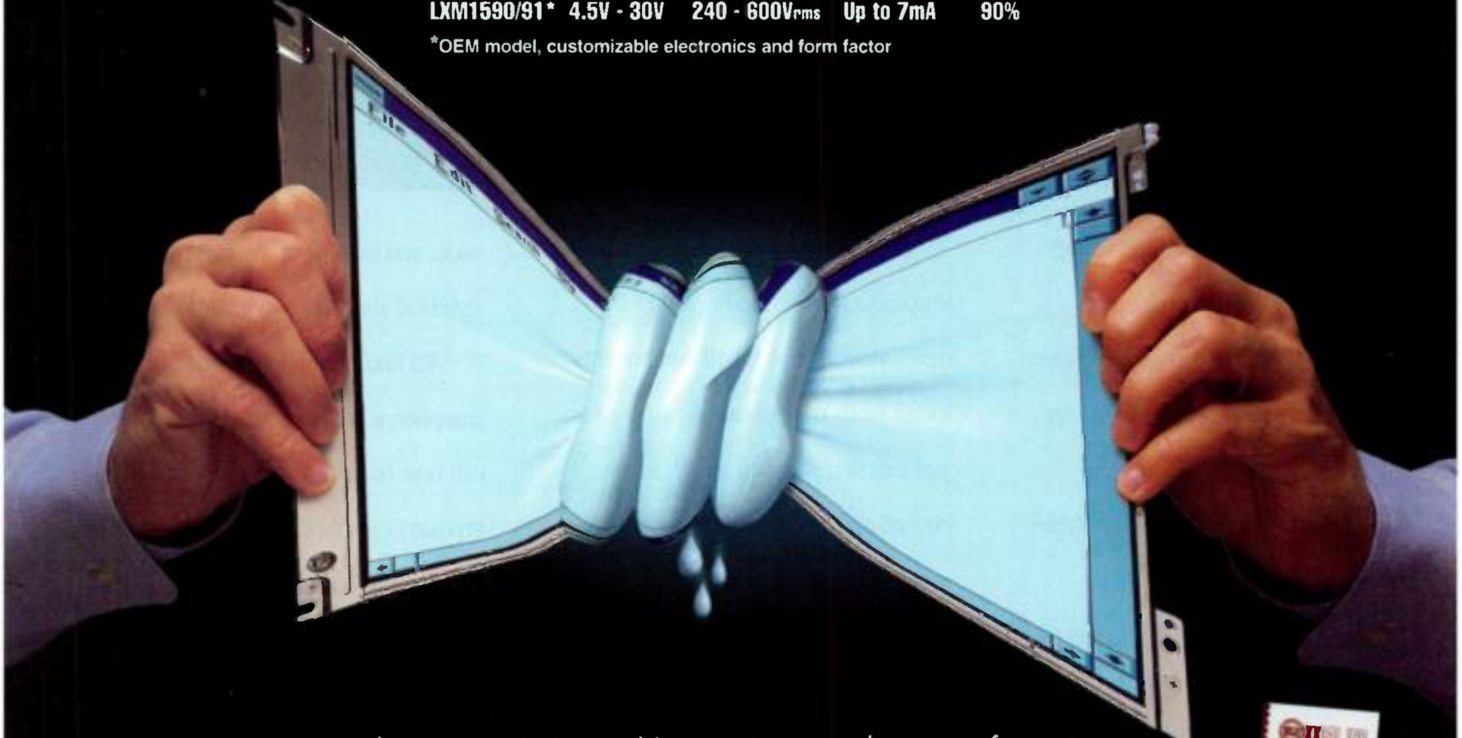

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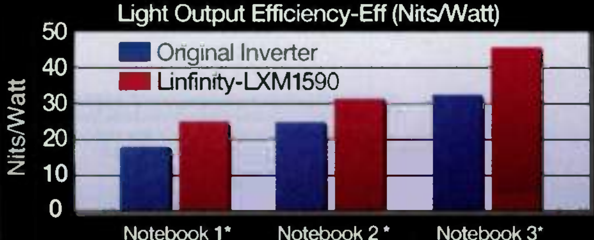

* Top of the line models from major manufacturers

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## Industry Group Formed To Champion VDSL Standards

While the world champs at the bit for more bandwidth in its telecom networks, a group of semiconductor, modem, and communications network equipment firms recently formed a coalition to promote development of interoperable standards for very-high-speed digital subscriber loop (VDSL) technology.

As currently defined by ANSI's T1E1.4 committee, VDSL is a collection of physical-layer transmission schemes and protocols intended for short-haul, high-speed applications. They would provide a choice of several symmetric and asymmetric line-rate profiles, with transmission speeds ranging from 13 to 52 Mbits/s. The group, which includes companies like Analog Devices, Broadcom, Harris Semiconductor, Lucent Technologies, Orckit, and Brooktree/Rockwell, is hoping to accelerate the standards process by developing system specification proposals to be presented to the ANSI working group.

After much analysis, all members of the coalition have endorsed the use of single-carrier, line-coding technologies, including carrierless amplitude/phase (CAP) and quadrature/amplitude modulation (QAM) for VDSL's downstream link. Agreement on recommendations for upstream transmission technologies is anticipated later this year. According to the coalition's new release, despite some member company's involvement with multicarrier technologies, such a discrete multitone (DMT), the mono-carrier approach was endorsed unanimously. This was because VDSL is intended to operate over shorter distances than its slower cousin, ADSL, and the cost/power sensitivity of local-loop applications.

For further information, contact Phil Lazowick at Broadcom Corp., 16251 Laguna Canyon Rd., Irvine, California 92618; (714) 450-8700; Internet: http://www.broadcom.com. LG

## Nonlinear Dielectrics Offer Microwave Tuning Alternative

Materials called nonlinear dielectrics can provide very precise, continual broadband or fine-tuning of high-performance passive microwave and RF devices. Researchers at Los Alamos National Laboratory used the materials to develop an electrical tuning technique that can replace the clumsy and relatively crude mechanical method that requires tuning screws built into the devices.

The method takes advantage of the fact that an electrical field induces changes in some dielectric thin films that can be used to control electrical tuning. The dielectric tuners are easily adjusted for differing requirements or equipment, and they can be miniaturized and integrated into conventional circuitry.

The researchers say the turners are better than semiconductors for some applications and are well-suited for high-performance microwave equipment used in wireless communications, which demand high peak-power capacity or fast switching speeds. For more information, contact Gary Kliewer at (505) 665-2085, or through e-mail at garyk@lanl.ogv. JN

## High-Speed Encryptor For WAN Traffic Under Development

Scheduled for roll-out in late 1998, work has begun on the development of a low-cost, high-speed encryptor for U.S. government and commercial applications. Dubbed TACLANE, the encryptor is a joint project undertaken by GTE, Needham, Mass., and Mykotronox, Torrance, Calif., and is intended to dramatically reduce the cost of network security. It will provide key-agile encryption capable of supporting multilevel applications at rates suitable for broadband backbone applications.

The TACLANE system is intended for providing economical high-performance encryption over IP and ATM networks, such as the Global Broadcast System (GBS). It also can replace more conventional trunk encryptors, further reducing network security costs. Additional information on TACLANE can be found on the World Wide Web at: http://www.rainbow.com, and http://www.gte.com. LG

## Lubrication-Free Low Friction Wire Is Environment-Friendly

A new resistance wire, called Low Friction, employs a modified surface structure that reduces friction to the point where lubrication during coiling and other forming operations is eliminated altogether. As a result, according to its manufacturer, Swedish-based Kanthal AB, the need to clean with the environmentally harmful trichlorethylene, or using other organic solvent-based methods, is eradicated.

Conventional coil manufacturing requires that an oil-based lubricant is used on the wire's surface to reduce friction during the forming process. Friction damage can scratch the wire, and the coil will develop large pitch variations. This leads to uneven temperature distribution and reduces the coil's effective lifetime. If a lubricant is used, it must be cleaned off using trichlorethylene.

By eliminating the harmful lubrication process, not only is there a significant savings monetarily, but more importantly, impact on the environment is reduced dramatically. In addition, the new material should provide a more uniform and higher production quality with fewer steps in the production process. Time also is saved: For high-temperature applications that require a very clean surface, such as in the making of tubular elements, the wire need only be cleaned in water at a temperature of around 90°C.

For more information, contact Victor Vanguele in Bethel, Conn., at (203) 744-1440, fax (203) 748-2229; or Richard Fareham at Stoke-on-Trent, U.K. at +44 1782 22 48 00, fax: +44 1782 20 26 06. RE

## Manufacturing Breakthroughs Made In YAG Microchip Lasers

YAG lasers (YAG = yttrium-aluminum-garnet) produced through a collective manufacturing process, may pave the way for mass production of compact, robust, and reliable components that are maintenance-free and able to adapt to many telemetry applications. For instance, a laser telemeter used to measure flight time, otherwise known as a chronometer, measures the time taken by a light wave to reach a target and return to a receiver.

To meet the needs of telemetry, the laser must emit a beam of a few kilowatts in peak value. Concerning precision and selectivity, the laser must offer very low divergence (around one milliradian).Other characteristics such as $TEM_{00}$ transverse mode and pulse duration, as well as being simple, compact, reliable, and low cost, are just as essential.

The production process for the microchip starts with a single-crystal bar of yttrium-aluminum-garnet, measuring one inch in diameter. Developed by the Grenoble-based company Crismatec (Saint Gobain Group), the crystal bar is cut up into fine slices around one millimeter thick, each of which is optically polished. A saturable absorbent (YAG crystal doped with quadrivalent chrome Cr4+) is deposited by liquid-phase epitaxy on the slice of amplifying crystal so that it can generate pulses in Q-switch mode.

The next step involves polishing the rear face to eliminate the deposit. The YAG crystal is inserted into a cavity and mirrors are placed directly by thermal evaporation or physical vapor deposition. One of the mirrors will be transparent to a wavelength of 0.808 µm to let the pumping beam through, but will reflect the full laser beam generated at 1.064 µm. The other mirror is partially transparent at 1.064 µm, while reflecting the pumping beam. The operation supplies between 200 and 300 YAG microlasers.

A laser diode is mandatory for pumping when YAG microlasers are used in telemetry. Pumping can be indirect, using a pigtail-type optical fiber of one or two meters, or indirect with or without a microlens. Sfim ODS's lasers are able to emit continuously or in pulsed Q-switch mode. The continuous YAG microlaser is dedicated to interferometry or spectroscopy applications. It emits a beam of 10 or 50 mW in the near infrared spectrum (1.064 µm). According to Jean-Pierre Herriau, sales manager at Sfim ODS, "the new developments will make it possible to clear the 100-mW mark."

Possible applications other than laser telemeters include lidars, the marking and treatment of materials with the highest levels of infrared energy, and the alignment and plotting after frequency is doubled using a KTP crystal.

For additional details concerning the lasers, contact Jean-Pierre Herriau, Sfim ODS, 14, rue Paul Dautier, 78941 Velizy, France; phone: (33.1) 34 63 39 37; fax (33.1) 34 63 39 06. RE

## Data-Storage Technology Is Focus Of Joint Development Agreement

Imation Corp, Oakdale, Minn., and TeraStor Corp., San Jose, Calif., shook hands on a joint venture to develop media for a new class of rewritable mass storage based on TeraStor's breakthrough Near Field Recording technology. According to Imation, Near Field Recording creates a new category of multipurpose mass-storage technology, leveraging a combination of hard-disk and optical technologies.

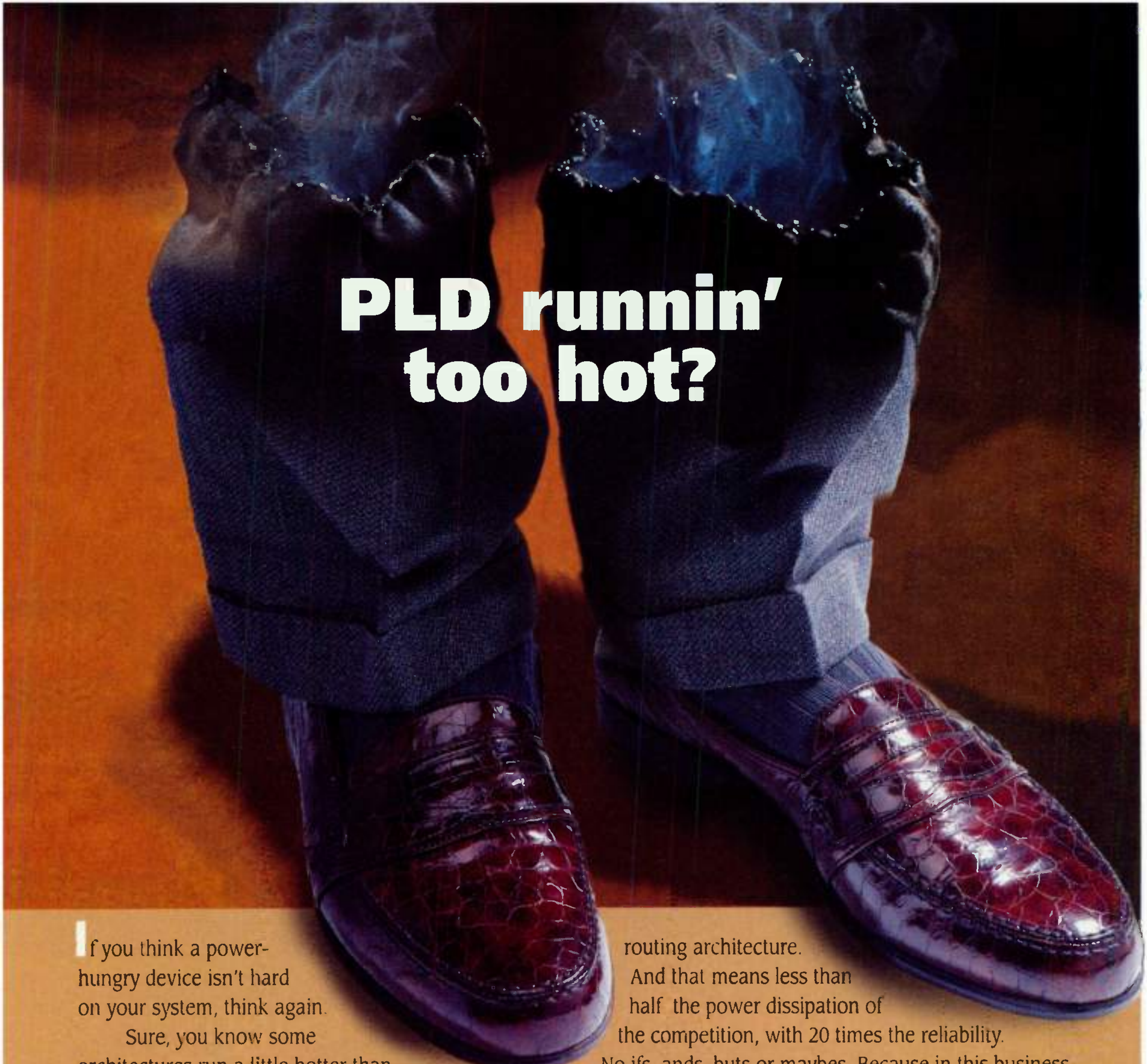
Significant improvements are expected in performance, a ten-fold capacity advantage, and a lower-cost -per-gigabyte than current storage options. Other advantages of using Near Field Recording technology are that it builds on existing removable hard disk (HDD) and magneto-optical technologies, and that it delivers random access performance. Furthermore, the technology isn't constrained to only fixed or rigid media; and it's form-factor-, platform-, and operating-system-independent.

Near Field Recording technology combines three patented technology advances. First, there's the "flying head," which is a modified version of the flying read/write head found in conventional hard-disk drives. The head flies at a controlled distance over the recording media, thus eliminating the cost of a servo system for focus. The "solid immersion lens," the optical element in the head that's closest to the media, significantly reduces the magnetic bit cell size, which increases recording density. And "first surface recording" material on the surface of the substrate, and then recording on that "first" surface. With this ability, lower-cost substrates can be used, and higher areal densities are achievable.

According to Imation, the anticipated capacity and performance characteristics of Near Field Recording technology would make it ideal for business customers who manage local-area and enterprise networks connecting end users of PCs and workstations. At the same time, the technology should be competitive with other solutions for the desktop user.

For further information, call Imation at 1 (888) 466-3456, or surf into the company's web site at: http://www.imation.com. TeraStor can be contacted at (408) 324-2110; fax (408) 324-2143. RE

*Edited by Roger Engelke*

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# Synthesis Technology Migrates Towards The High-End Design Environment

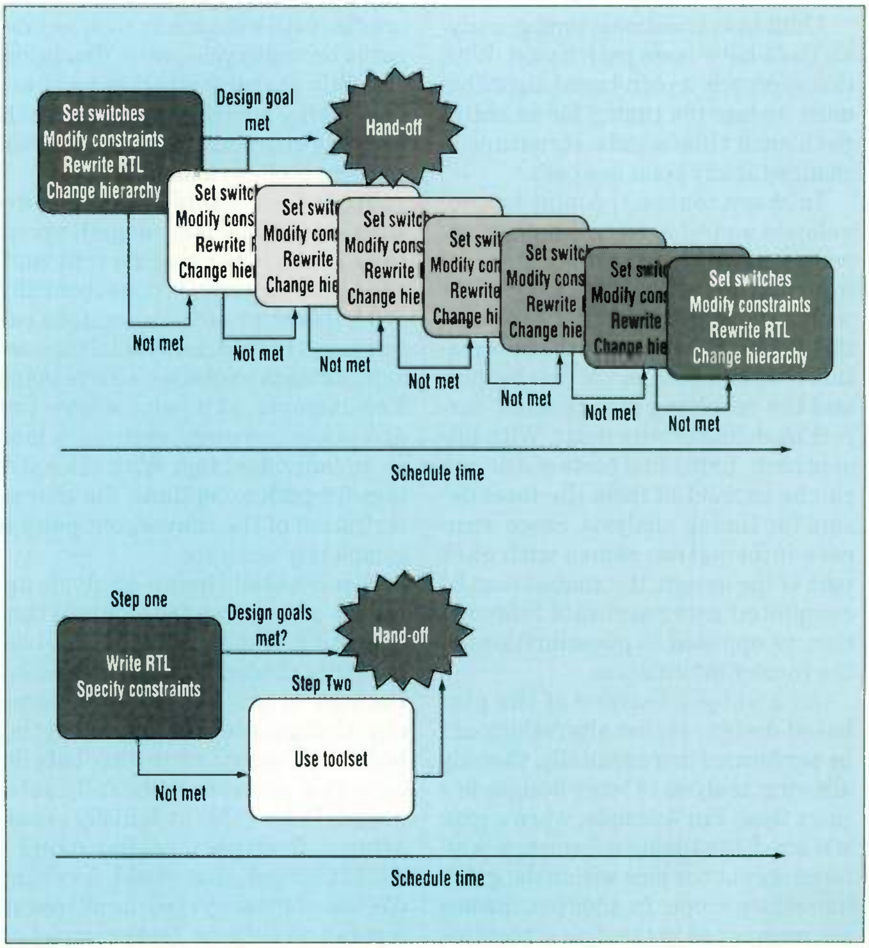
Since its inception and implementation, synthesis has worked to dramatically shape the face of the Electronic Design Automation (EDA) industry, propelling designers into a world of test vectors and iterations. In fact, synthesis technology has virtually revolutionized the design paradigm, becoming synonymous with design and enabling a more automated approach. Little about the technology has changed over the years, and, in truth, nothing really needed to change. The technology worked well for chips on the order of 5000 to 30,000 gates. But with the advent of deep-submicron (DSM) designs, its ability to be used, as is, in high-end designs has come into question.

Ambit, Santa Clara, Calif., recognizing the need to find a way for synthesis to be migrated into the cutting-edge designs of tomorrow, has developed a number of technologies to pick up where the traditional synthesis methodology and its increasingly apparent limitations have left off *(see the figure)*. In particular, the company's attempts at a synthesis technology espouses a three-fold approach: a pin-based timing analyzer, new technology mapper, and an innovative modular and programmable architecture. The benefits of this technology coupling are substantial, giving a five times improvement in capacity; reducing the time spent in synthesis phase by half; and for a given area, at least 10% better quality of timing results.

As gate counts near the 100,000 - 200,000 mark, many difficulties with traditional synthesis methodology have come to light. At this magnitude of gate counts, chip integration, achieving desired chip performance, and modeling DSM technology accurately, can be formidable tasks. Additionally, there are the endless iterations needed through the synthesis and layout processes. And, with high gate counts, the timing analysis virtually breaks down. Today's designer, forced to work under pressure from shorter design cycles and time-to-market goals, simply doesn't have the time, or the resources, to make traditional synthesis techniques work in a cutting-edge, DSM world. Compounding all of these problems is that constraint management through hierarchy and time budgeting is still done manually.

In part, the difficulties arise because at the heart of traditional synthesis is a combined algorithmic and rule-based technology mapping approach that is unable to work with very big library elements. The overall effect of this approach, coupled with its strict, serial-format implementation, is that it can be cumbersome to use on large designs, thereby necessitating large run times. In contrast, Ambit's newly developed technology mapper is based on a parallel algorithm approach using a Boolean, as opposed to a tree-based, algorithm. Multiple choices of design types and performance goals are evaluated in parallel. The algorithm with the best improvement or implementation wins.

Because the technology mapper can evaluate all possible implementation choices in parallel, it is much quicker than traditional synthesis technology. And, since it can map to much bigger cells, the quality of the design is better. An added benefit is that its solutions are more predictable, due to the fact that it allows for an accurate convergence of mapping results. Conse-




**Traditional synthesis technology faces a number of limitations that make it difficult to migrate into a high-gate-count, deep-submicron-design environment. The hierarchical synthesis technology proposed by Ambit, on the other hand, is specifically intended for use in cutting-edge designs, and can be easily implemented into the current design methodology. It significantly cuts the number of design iterations and speeds the synthesis process. Rather than endlessly tweaking a design, Ambit's design approach is direct—write RTL, specify constraints, then push a button. To accomplish this task, a number of technology advances, such as the pin-based timing engine, and hierarchy capability, needed to be developed.**

quently, as constraints get tighter there is a better margin of improvement. And, small changes in the constraints do not cause wild swings in the synthesis results.

Since the parallel-algorithm technology mapper does not maintain a cumbersome rule set, faster run times can be achieved. The technology offers a less stringent code requirement, as well. Larger cells, an 8:1 multiplexer, for example, can be located in the middle of a design, without setting special optimization switches, or using any special programs in the source code. The use of an algorithmic approach during the optimization process also means there is less memory consumption because the number of iterations is substantially decreased.

Until now, traditional timing-analysis tools have been path based. With this approach, a path-based algorithm must update the timing for an entire path each time a gate structure is changed at any point in a path.

In sharp contrast, Ambit has developed a pin-based technology approach in which all necessary timing information is kept at every point within the netlist, and at every pin in the design. For each net, the information is stored both at the driving pins and the receiving pins to allow correct modeling of wire delay. With this approach, individual parts of a design can be extracted from the total design for timing analysis. Since accurate information comes with each part of the design, the analysis can be completed using accurate information, as opposed to guestimations of the correct information.

As a unique feature of the pin-based design, netlist alterations can be performed incrementally, thereby allowing analysis of large designs in a short time. For example, when a gate is resized, the timing information is altered only at the pins within the gate's immediate scope. In addition, queues are maintained in the data structures that indicate additional nodes that are out of date. Those nodes are updated only if they are involved in further optimization operations.

The pin-based timing-analysis engine offers a number of benefits over the more traditional path-based approach, including improved timing and accuracy. In fact, it allows million-gate designs to be timed using moderate CPU and memory space. And, due to its high accuracy (roughly 99%) during timing optimization, correct gate selection, gate sizing, and buffering is guaranteed. The pin-based technology also is an order of magnitude faster than the path-based techniques currently in use.

Two additional technology advances, accurate exception characterization of false paths and multicycle paths, and automatic converging time budgeting, are incorporated into the pin-based timing-analysis approach.

Characterization refers to the process of extracting timing constraints for a subdesign given a mapped netlist. The difficult part of this task is being able to accurately predict path exceptions such as false paths or multicycle paths. Traditionally this characterization has been done using a path-based approach, meaning characterization of path exceptions is often random.

To deal with this limitation, designers typically include path exceptions in the lower module time budgets. This inclusion is done manually. With this approach, exceptions can be easily tracked. Individual tags are kept for each exception source point. For example, at a point where two exceptions converge, each one is kept as an individual tag. With the extra tags for path exceptions, the characterization of the convergent point is completely accurate.

A pin-based timing-analysis approach also allows for accurate time budgeting. Traditionally, the time budget is distributed between combinatorial logic in multiple pieces of hierarchy. Using a proprietary, budgeting technology algorithm to distribute delays, this process can be fully automated. It does this by initially generating a first-pass netlist using a default budget, that would, for example, use a 50% duty cycle on all module inputs and outputs. Once completed, an automatic timing budgeter would distribute the delays through the design's hierarchy.

Another innovative technology advance developed by Ambit is a fully programmable, modular architecture that supports multiple, simultaneous delay calculators such as linear and nonlinear, DCL, and user-defined. With this type of architecture, the designer can create design-independent custom optimization techniques. Designers also can write a generic transform for the design, to make the appropriate netlist alteration and improve the quality of results on the chip. The transform can then be applied to future designs for consistent results.

Programmability of the synthesis technology implementation is possible because the architecture's environment is built around the standard programming language, TCL. With procedures and built-in functions, long complex scripts in older languages can be quickly rewritten, without having to depend on outside tools such as perl. In addition, the TCL capability allows the use of either customized or off-the-shelf optimization techniques.

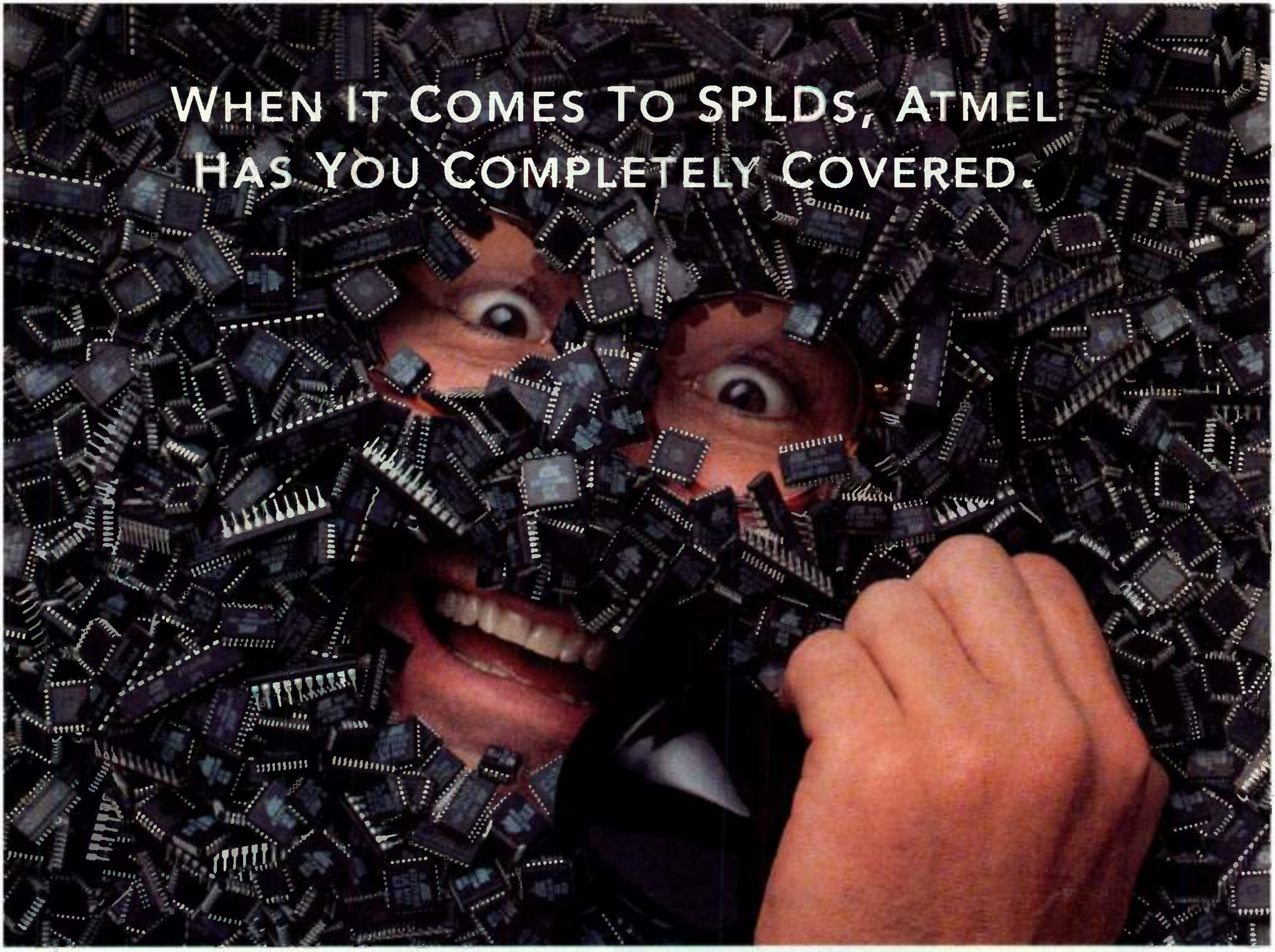
The synthesis technology, proposed by Ambit, also is unique in that it is truly hierarchical—able to work on hierarchical designs, and not just individual modules. With a new hierarchy constraint-management technique in which constraints do not need to be repeatedly applied, the synthesis technology is able to accommodate the needs of million-gate designs with minimal intervention.

By comparison, using traditional synthesis techniques, a design must be broken down into modules. The individual modules are each synthesized, then integrated back together. The integration is dictated by a set of constraints applied to every level of the hierarchy. At this point, the design, now in the form of a chip, is run through a time-consuming, static timing analysis. During this time the designer is forced outside the native synthesis static-timing tool for chip-level sign-off.

With Ambit's utilization of an optimization technique with a capacity significantly larger than traditional synthesis technology, static timing analyses run times are an order of magnitude faster. This allows the native synthesis tool to be a static timing sign-off engine for a large chip.

For more information, contact, Ambit Design Systems, 2933 Bunker Hill Road, Suite 215, Santa Clara, CA 95054; (408) 566 8000.

**Cheryl Ajluni**

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|---|---|---|---|---|---|---|
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| 20V8 | 7 | 10,15,25 | 10,15,25 | | | |
| 22V10 | 5,7 | 10,15,25 | 15,20,25 | 12,15 | 10,15 | 25 |

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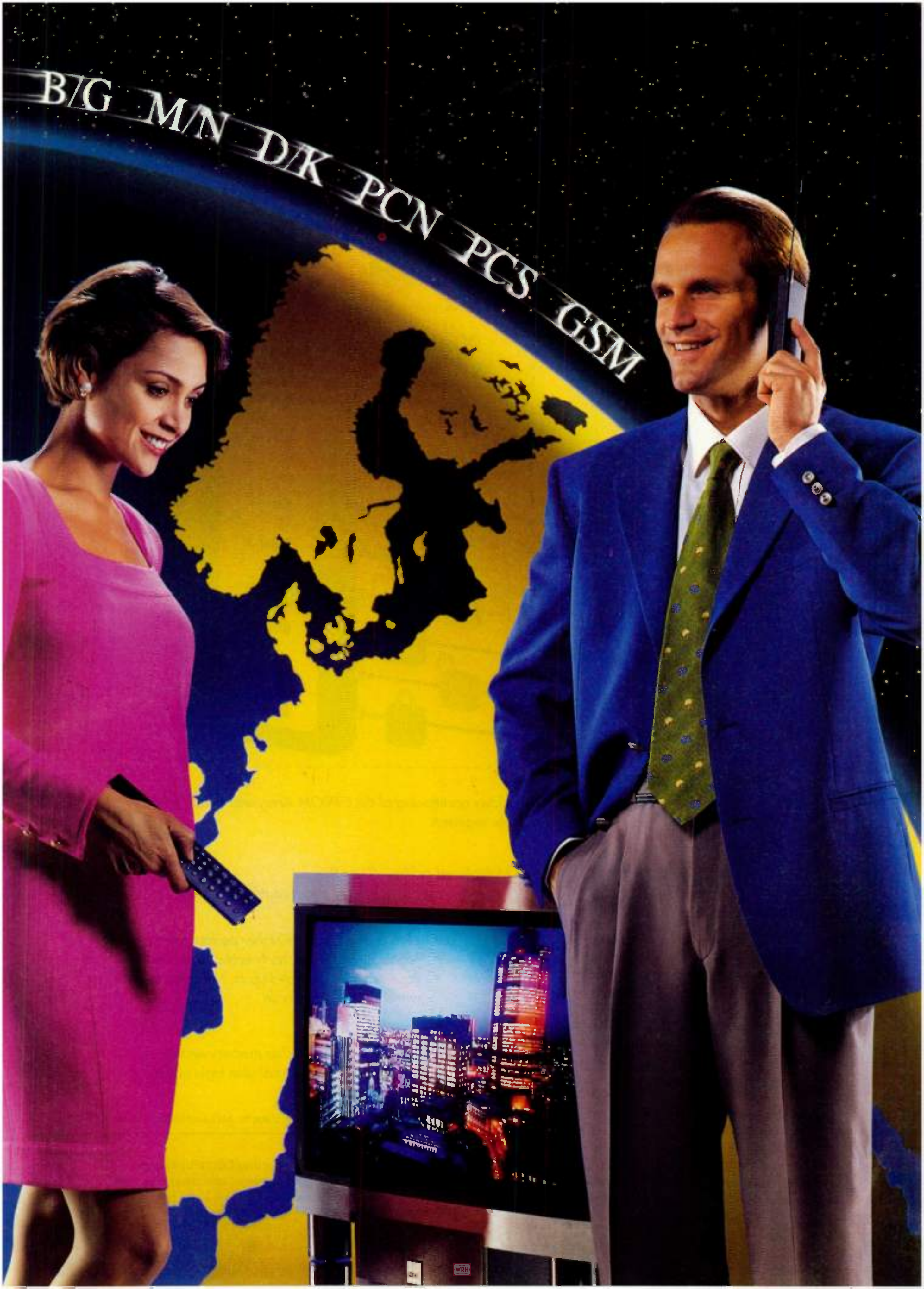
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# Design Techniques And Communications Advances Take The Spotlight At CICC'97

The 19th Custom Integrated Circuits Conference (CICC), to be held May 5-8 at the Santa Clara Westin Hotel and the Santa Clara Convention Center in Calif., provides a multifaceted demonstration of the latest design techniques, circuit architectures, advanced processing, design tools, and test techniques for custom ICs. This year, 24 technical session will cover analog technology, data communications, data processing, multimedia, low-power design techniques, RF circuit design, design tools, and many other topics. Four tutorials, three panel sessions, as well as several exhibitor marketing sessions in addition to a general exhibition that runs concurrenly with technical paper sessions, round out the program.

Opening the conference will be a quartet of educational sessions on Monday, May 5. These tutorials provide backgrounders on Advanced Interconnects, Design and Analysis of Submicron ULSI Interconnects, MOSFET Modeling and Spice, and On-Chip ESD Protection Techniques. Technical paper presentation sessions will provide designers with a full palette of technology developments that will be used to create the next generations of analog and digital circuits *(see the table)*.

The Keynote presentation by Dr. Henry Samueli, cofounder and vice president of Broadcom Corp., examines broadband communications ICs and how they will enable wide-area networking in the 21st century. Nearly a third of the technical presentations will address all types of communications such as RF wireless, telecommunications, and data communications, and one of the three evening panels will also focus on RF IC design. The focus on communications is a major change from past CICCs, demonstrating the impact communications is having on the overall industry.

For conference regisgtration, contact CICC, 101 Lakeforest Blvd., Ste. 270, Gaithersburg, MD 20877; (301) 527-0902 (ph); (301) 527-0994 (fax); *http://ieee.org/conference/cicc*. For hotel reservations, call (408) 986-0700.

**1997 CUSTOM INTEGRATED CIRCUITS CONFERENCE (CICC) TECHNICAL PROGRAM**

| | | | | |
|---|---|---|---|---|
| Monday, May 5<br>8:00 a.m.-5:00 p.m. | **Education sessions**<br>• IC design • Wireless IC design • Interconnects and Spice modeling | | | |
| Tuesday, May 6<br>8:00-9:30 a.m. | **Session 1**<br>**Keynote address**<br>Broadband Communications ICs: Enabling wide-area networking into the 21st Century | | | |
| 10:00 a.m.-Noon | | Session 2<br>Data transmission and equalization | **Session 3**<br>IC reliability | **Session 4**<br>Keeping in synch: PLLs and their application |
| 2:00-5:00 p.m. | **Session 5**<br>Analog techniques | **Session 6**<br>Core-based chip design | **Session 7**<br>Clocking and low-power methodologies | **Session 8**<br>Analysis for deep submicron |
| Wednesday, May 7<br>8:30 a.m.-Noon | **Session 9**<br>RF IC technology | **Session 10**<br>Analog and digital test | **Session 11**<br>Audio and video DSPs | **Session 12**<br>Circuit techniques, image storage and processing interfaces |
| 2:00-5:00 p.m. | **Session 13**<br>Data converters | **Session 14**<br>Digital communications | **Session 15**<br>Library design and modeling | **Session 16**<br>RF modeling and simulation |
| 8:00-10:00 p.m. | **Session 17**<br>**Panel discussion:**<br>"Smith chart meets Spice," a CAD nightmare in RF IC design | **Session 18**<br>**Panel discussion:**<br>What should it cost to test your chip? | **Session 19**<br>**Panel discussion:**<br>Fab capacity: Estimating the market | |
| Thursday, May 8<br>8:30 a.m.-Noon | **Session 20**<br>Wireless ICs | **Session 21**<br>Fab technology for wireless applications | **Session 22**<br>DSP for communications and networking | **Session 23**<br>Power, interconnect, and noise analysis |
| 2:00-5:00 p.m. | **Session 24**<br>Radio circuit design techniques | **Session 25**<br>Innovations in programmable device architectures | **Session 26**<br>Physical design automation | **Session 27**<br>Low-power, low-voltage circuits |

# Core-Based Design Leads The Way To Flexible System Solutions

*Multiple Design Approaches Come Together At CICC To Build High-Performance, Low Power Digital Circuits.* **DAVE BURSKY**

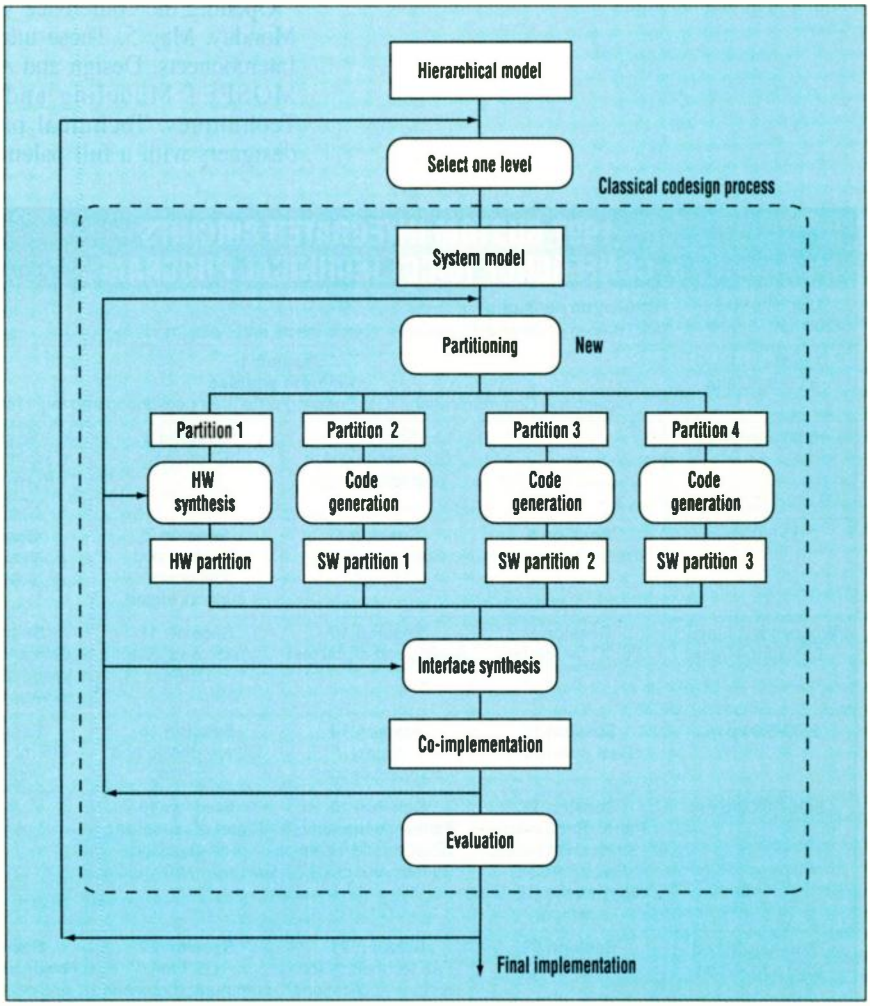
Time-to-market issues have figuratively pushed designers' backs to the wall, demanding previously unheard of turn-around time deadlines that just a few years ago were thought to be impossibly short. One key aspect that has helped to reduce the design cycle is the reuse of circuit functions from one chip design to another. The reuse of intellectual property (IP) has become a new aspect of custom circuit design—designers are not only crafting their circuits more modularly so that sections can be split off and used in other designs, but blocks are being designed elsewhere where they can be imported and incorporated into any company's current design.

At the upcoming Custom Integrated Circuits Conference (CICC), a full session and papers scattered in other technical presentation sessions highlight some of the core-based and building block developments that will make designing the next generation of chips much quicker and easier. In Session 6, for example, all the papers are devoted to core-based design approaches, with the lead presentation by the Alta Group of Cadence Design Systems Inc., Sunnyvale, Calif., examining the use of virtual prototyping to speed circuit development (paper 6.1). By assembling blocks of IP and even representations of physical structures such as a control panel, simulations can be done to validate the architecture or functionality of the system.

However, as the author, James Rowsen, pointed out, verification is one of the most difficult design problems today due to the limited amount of computer horsepower available, and the limited ability to accurately model many aspects of a design. But the problem can be made more tractable by splitting verification into a set of independent tasks, which can then be executed on different engines or going to more optimized algorithms for evaluation.

## Exploring Design Space

Examining the hardware and software partitioning for the modeling of a design, researchers from Ecole Polytechnique of Montreal, Quebec, Canada, and Mentor Graphics Corp., Wilsonville, Ore., detail a hardware/software partitioning approach based on a new use of hierarchical modeling. In a typical codesign process, the input is the system model specified as a set of blocks or operations with all their interdependencies. The input language can be an HDL or a programming language. The model is then partitioned to assign input blocks to hardware or to software,




**1. By enhancing the typical codesign methodology through the addition of multiple partitioning stages to more efficiently explore the design space, the scheme developed by the Ecole Polytechnique of Montreal and Mentor Graphics provides a means to better analyze the design alternatives and find the most optimal solution.**

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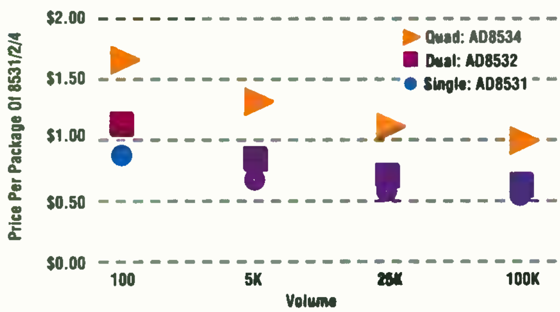


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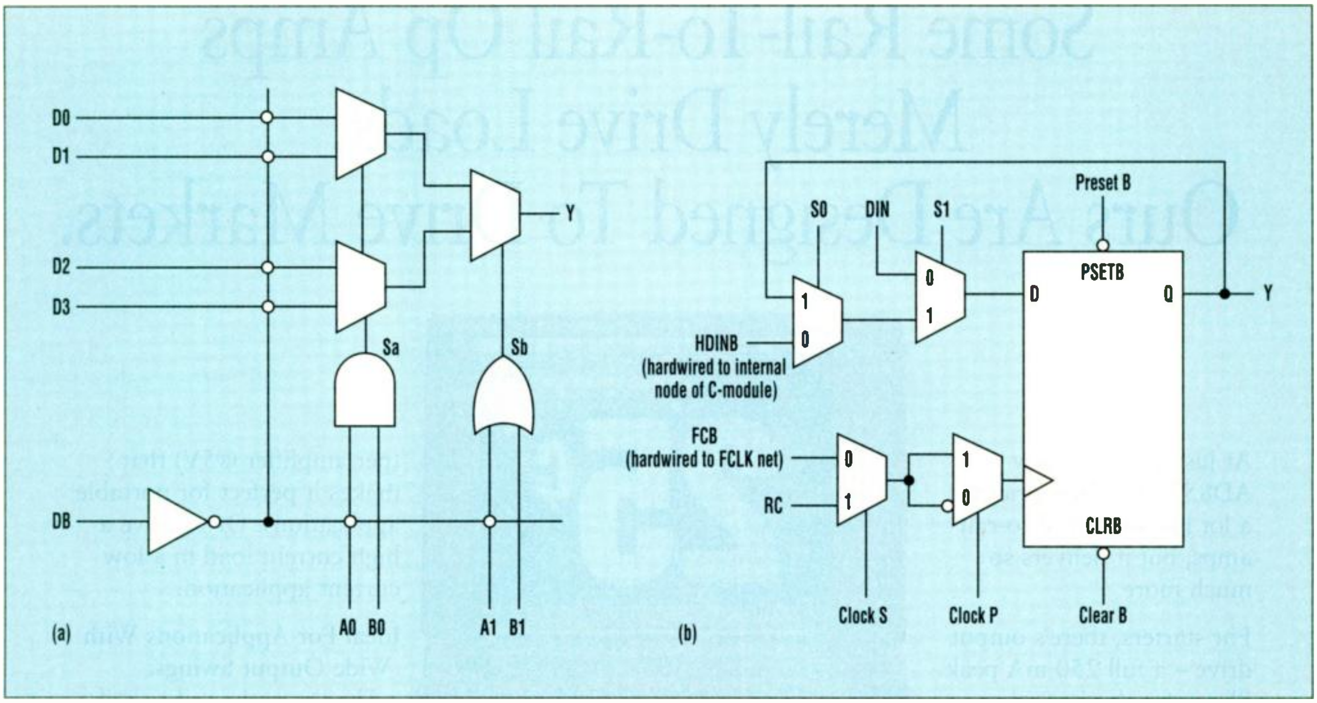



**2. An enhanced logic cell (a) developed by Actel for use in a high-density sea-of-modules architecture can map over 4000 useful logic functions. An accompanying flip-flop cell (b) includes Preset and Clear inputs as well as multiple control inputs that can configure the circuit to meet the user's needs.**

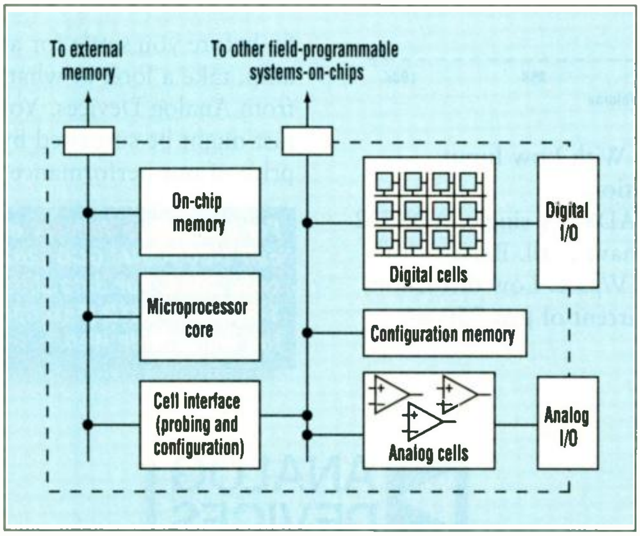
guided by a cost function that takes into account the estimated performance for both hardware and software and the communication overhead *(Fig. 1)*.

The improved scheme developed by the researchers allows a more efficient exploration of the design space by enhancing the classical process with a range of abstraction levels such that each level provides a new model, in terms of complexity, for the same input system. Four modeling techniques are used: Finite state machines for control and communication systems, flowgraphs and trees for DSP applications, communicating processes for concurrent systems, and object-oriented models for software applications.

Furthermore, based on the granularity of the modeling techniques, two classes of models are available—those that consider the input system behavior only at the operation level, and those that consider the input system behavior only at the process or functional-block level. The new modeling system employs a variable granularity level to allow the designer to start with an input behavior at the process level, codesign it, and if the performance constraints are not satisfied, select a deeper level of granularity to increase the number of basic blocks.

When creating models of IP blocks, defining the timing abstraction model is one of the more-difficult tasks. In paper 6.3, Cadence Design Systems, in conjunction with the University of Michigan, Ann Arbor, examines a methodology for creating timing models of large blocks (>5000 transistors) through the use of static timing analysis. The methodology captures the block's propagation delays and the slew rates at its outputs. More importantly, the scheme abstracts all the internal setup, hold, and loop constraints of the block. By using all the abstracted information, an accurate block timing model can be created and used to represent the block's temporal behavior.

Lastly, in paper 6.4, several perspectives of the recently initiated Virtual Socket Interface Alliance (VSIA) will be presented by Laurence Cook of Toshiba America Electronic Components Inc., San Jose, Calif. The VSIA's goal is to level the playing field of ASIC vendors by defining a common set of interface standards for integrating virtual components (blocks of IP software, firmware, hardware) into system ASICs. By doing so, it will be easier for ASIC designers to obtain blocks of IP




**3. A merging of CPU, programmable logic, and configurable analog circuits let the researchers at SIDSA, Mikron, the University Politecnica de Catalunya, and the Universidad de Seville create a true field-programmable system-on-a-chip that can accept analog or digital inputs and deliver analog or digital results.**


AQ 18



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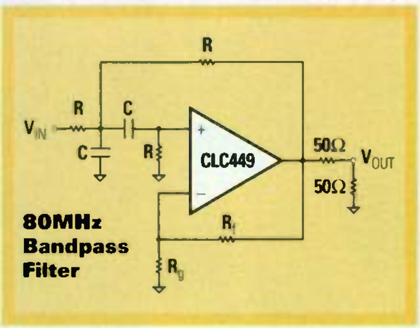


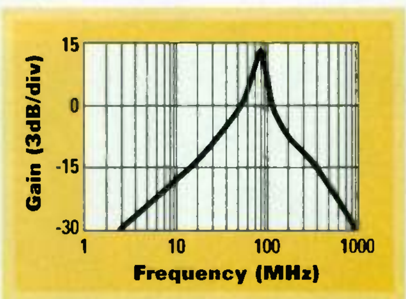


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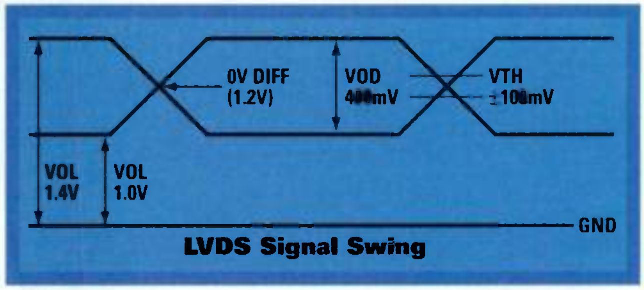

LVDS Signal Swing

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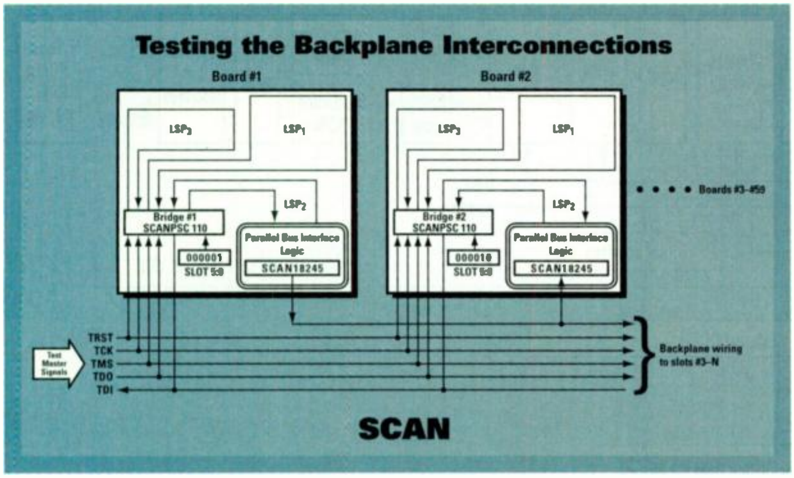


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and import them into their design. The scheme also will make it easier for IP providers to create and distribute new blocks/functions.

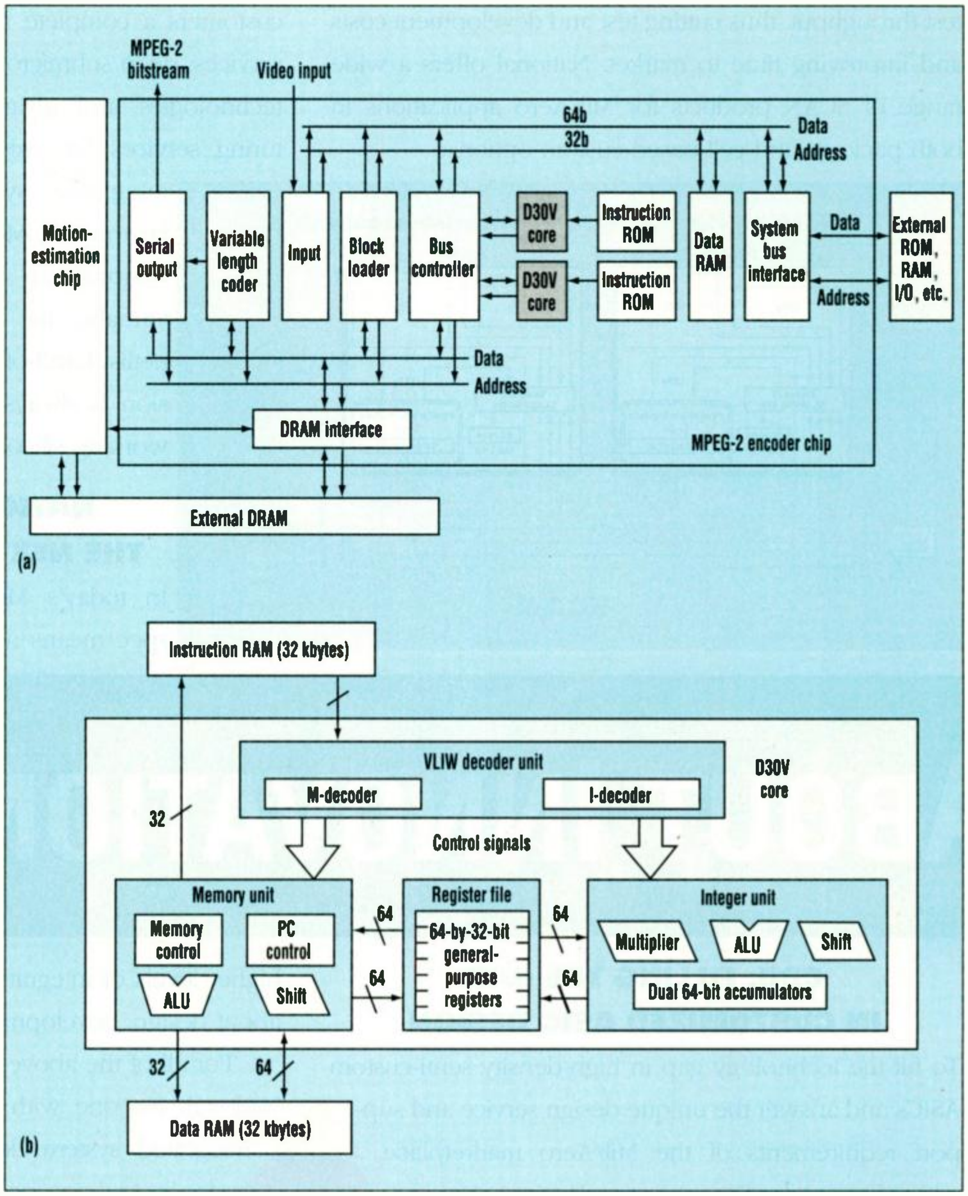
Additional discussions of design library creation and dedicated building blocks are distributed throughout the conference, but Session 15 clusters a number of such presentations to discuss library design and modeling. In paper 15.2, designers from Kyoto University, Japan, detail P2Lib, a process-portable cell library and the tools used to create the library elements. One distinctive feature of the library and tools is the ability to quickly characterize the timing and power dissipation of the blocks. The analysis is done with an analytic-oriented methodology in conjunction with circuit simulation tools for accurate characterization.

## Dynamic Logic

Another tool developed by researchers at the Department of Electrical Engineering at the University of Washington, Seattle, employs a self-timed dynamic-logic structure as the basis for creating a logic family. Detailed in paper 15.3, the clock-delayed domino logic was developed to provide non-dual-rail gates with inverting or noninverting outputs. That makes the logic as easy to synthesize as static circuits and allows synthesis tools developed for static circuitry to be readily usable on this logic. Synthesis tests performed using benchmark circuits developed by the Microelectronics Research Center of North Carolina (MCNC, in Research Triangle Park) yielded speed improvements of from 2.17 to 6.28, compared to their static-logic counterparts.

Creating a logic model to better simulate and then fabricate a circuit, designers at Toshiba America Electronic Components, San Jose, Calif., detailed a full-function Verilog model of the logic for a phase-locked loop (paper 15.6). While most other models bypass the actual phase-lock function, this model accurately represents all the major characteristics of a PLL and allows the simulation of the effects of actual filter elements. Furthermore, the model will provide accurate representations of clock deskew from a clock tree as well as model the synthesis of other frequencies from a clock input.

Most of the library blocks created by the tools will be reused in various chips, possibly through the use of compilers that will custom configure a library block the system under design, or in many cases, as a predefined block that will just be "dropped" in. One example, presented in paper 15.1, described a reusable embedded DRAM macrocell developed by designers at Lucent Technologies, Murray Hill, N.J. Another is a 16-by-16-bit left-to-right carry-free multiplier presented as paper 22.7 by researchers from Lucent Technologies and Bell Laboratories, both of Allentown, Pa. The multiplier block can operate at 200 MHz when fabricated using a 0.35-µm CMOS process and was developed as a building block for use in next-generation digital-signal processors. Another block described in paper 12.5 covers a




**4. The heart of a real-time MPEG-2 encoder/decoder chip (a) developed by Mitsubishi Electric consists of a pair of dual-issue RISC processor cores that operate at a 250 MHz clock rate (b). Each core includes 32-kbyte instruction and data caches and employs a very-long-instruction-word architecture to allow the full encoder chip to deliver a peak throughput of 1 gigaoperation per second.**

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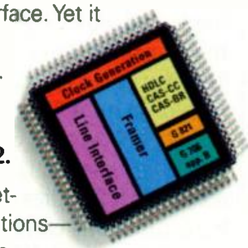


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250-MHz dual-port cursor RAM developed by Mitsubishi Electric Corp., Itami, Japan.

One logic area that can quickly leverage the IP is the programmable logic arena, which takes the IP, synthesizes the required logic, and then configures the programmable chip to overlay that logic on its configurable array. To make it easier to assimilate more complex IP blocks, designers at the programmable logic suppliers are defining new base-array architectures. For example, in paper 25.1, designers from Actel Corp., Sunnyvale, Calif., have crafted a high-performance, high-density sea-of-modules architecture that takes advantage of the company's novel metal-to-metal antifuse configuration elements.

Able to implement arrays with densities of from 5000 to 200,000 gates the sea-of-modules approach includes an improved logic cell, a flexible interconnect architecture, and full-featured "fracturable" flip-flops that are intermixed with the logic cells. The cell is an enhanced version of the multiplexer-based cell used in the company's previous FPGA families *(Fig. 2)*. Over 4000 logic functions can be mapped into the cell, and several different hierarchical cell clusters are then built from the logic cells and the flip-flops.

Another synthesis-efficient array, detailed by researchers from the Microelectronics Group of Lucent Technologies, Allentown, Pa., in paper 25.3, highlights architectural improvements over previous OrCA families that make the chips in the 3C/3T family friendlier to logic synthesis tools. The array architecture includes look-up table combinatorial logic, an abundant number of flip-flops, and PAL-type decoder blocks, all grouped in a twin-nibble fashion. The basic programmable logic cell contains a programmable function unit (PFU) and a supplemental logic and interconnection cell (SLIC). Together, they provide a flexible building block that supports typical glue logic and most common functions that make up behavioral-level code, such as adders, subtractors, counters, accumulators, comparators, multipliers, and single- and dual-port RAMs.

A research project at the Department of Electrical and Computer Engineering at the University of Toronto, Ontario, Canada, has led to the development of an FPGA architecture that employs cluster-based logic blocks to achieve a more area-efficient logic array. Detailed in paper 25.5, the cluster analysis assumes "n" basic logic elements in a cluster, with each element consisting of a 4-input look-up table, a D-flip-flop, and a simple output multiplexer. The study examines the optimization of the logic to determine the best number of logic elements to put into a cluster, the total number of distinct inputs that the programmable routing can provide to each cluster, and how those factors affect chip area-efficiency. As a result of the analysis, the researchers concluded that a cluster containing four basic logic elements would be the optimal size.

Low power consumption is the thrust of an FPGA family developed by Altera Corp., San Jose, Calif., and detailed in paper 25.2. Designed for 3.3-V operation, the FPGAs will offer capacities of up to 130 kgates and employ some internal circuit tricks to deal with the interface requirements as system power supplies go from 5 to 3.3, and eventually, to 2.5 V. In a second presentation in the same session (paper 25.4), designers from Altera provided details of a 5000-gate complex PLD fabricated with electrically-erasable configuration elements and a configurable frequency multiplier that allows the chip's internal clock frequency to run at up to 140 MHz, thus allowing the circuit to handle high-speed buses and other high-performance system needs. The EEPROM-based configuration cells are programmed through a serial interface that also is capable of being used as a JTAG-compatible test port.

## Analog Goes Digital

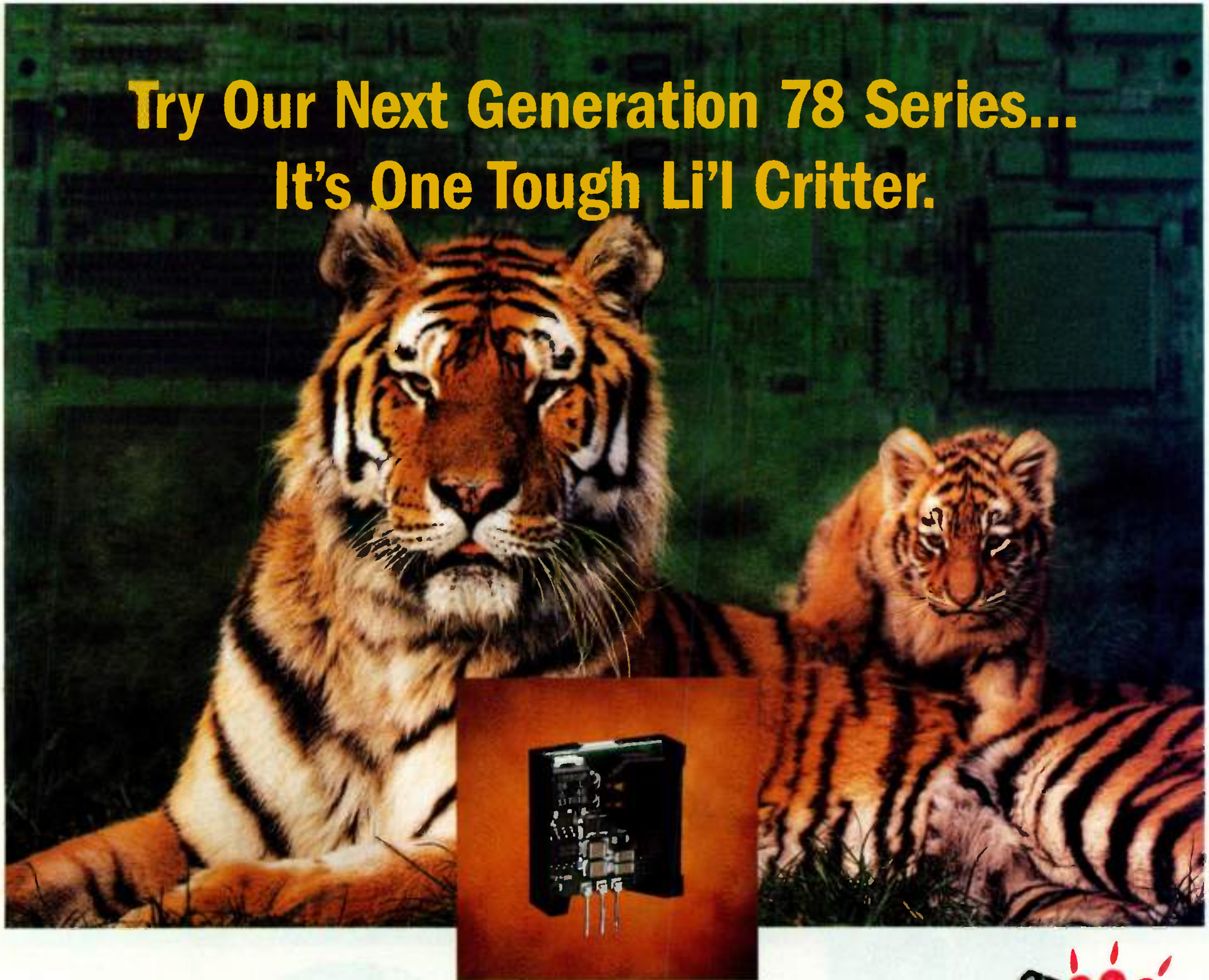
Although digital logic lends itself best to field configurability, many analog systems would love to have a field-programmable analog circuit. Just such a development will be described in paper 25.6—a joint effort between designers at Motorola Inc., Tempe, Ariz., the University of Arizona, Tucson, and Pilkington Micro-Electronics Ltd., Cheshire, U.K. The array consists of a sea of switch-capacitor-based analog cells that is surrounded by configuration logic. Some RAM is local to each analog cell, and that memory helps control the function of the cell. The analog array can be programmed to perform many of the routine tasks associated with control systems: Linear and non-linear signal processing capabilities to provide a wide range of waveform generation functions, or various phase and magnitude characteristics.

Offering mixed-signal capabilities along with an on-chip processor core and blocks of programmable logic, a novel chip developed by SIDSA, Parque Tecnologico de Madrid, Spain, in conjunction with WML of Solihull, England, Mikron GmbH, Eching, Germany, the Universitat Politecnica de Catalunya, Barcelona, Spain, and the Universidad de Sevilla, Spain will be detailed in paper 6.4. The chip contains a set of programmable and interconnectable analog cells, a block of programmable logic, and an 8051-equivalent microcontroller core implemented with synthesis tools *(Fig. 3)*.

The FIPSOC (field-programmable system on a chip) project will rely on a fully-integrated design and prototyping environment that is being developed to configure and evaluate the circuit. The tools must not only handle the logic configuration needs of the FPGA section, but the analog configuration as well, not to mention the programming needs of the 8051 microcontroller. The chip is fabricated using a 0.5-µm triple-metal CMOS process provided by Atmel Corp.'s ES2 division in Europe. The configuration cells in the array are MOS transistor switches controlled by RAM look-up tables.

The use of modular design techniques and reusable building blocks is fairly obvious in functions such as multimedia circuits, which often require "standard" functions such as multipliers, ALUs, and memory arrays. A real-time MPEG-2 encoder/decoder chip developed by Mitsubishi Electric, for example, includes dual, identical CPU cores on the chip along with dual 32-kbyte caches and many other blocks needed to perform the MPEG encoding in real time *(Fig. 4a)*. Designers estimate that the chip is about 20% smaller using the dual CPU approach that if they were to have created a chip employing dedicated logic.

The processor core consists of a 250-MHz, dual-issue RISC CPU, a hardware block that decodes very-long-instruction words for execution on the CPUs, a 64-word-by-32-bit gen-

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|---|---|---|
| **Test** | **Method** | **Conditions** |
| Mechanical Shock | MIL-STD-883D, Method 2002.3 | Condition A, 500G peak, 1 mSec, half sine, 5 shocks, 2 directions, 3 axes, (30 shocks total) |
| Mechanical Vibration | MIL-STD-883D, Method 2007.2 | 4 four-minute sweeps, 4x each axis, total time 48 minutes, 20 to 2000 Hz logarithmically |
| **ENVIRONMENTAL ENDURANCE TESTING** | | |
| **Test** | **Method** | **Conditions** |
| Thermal Shock | MIL-STD-202F, Method 107 | 200 cycles, -40°C to +125°C, 15 minute dwell time |
| Humidity | MIL-STD-202F, Method 103 | 85% relative humidity (non-condensing), 85°C ambient, 240 hours, Vin=Vmax, Iout=10% Imax |
| Accelerated Life | MIL-STD-202F, Method 108 | 1000 Hours, 60°C ambient, Vin=Vmax, Iout=Imax |
| **ESD QUALIFICATION TESTS** | | |
| **Test** | **Method** | **Conditions** |
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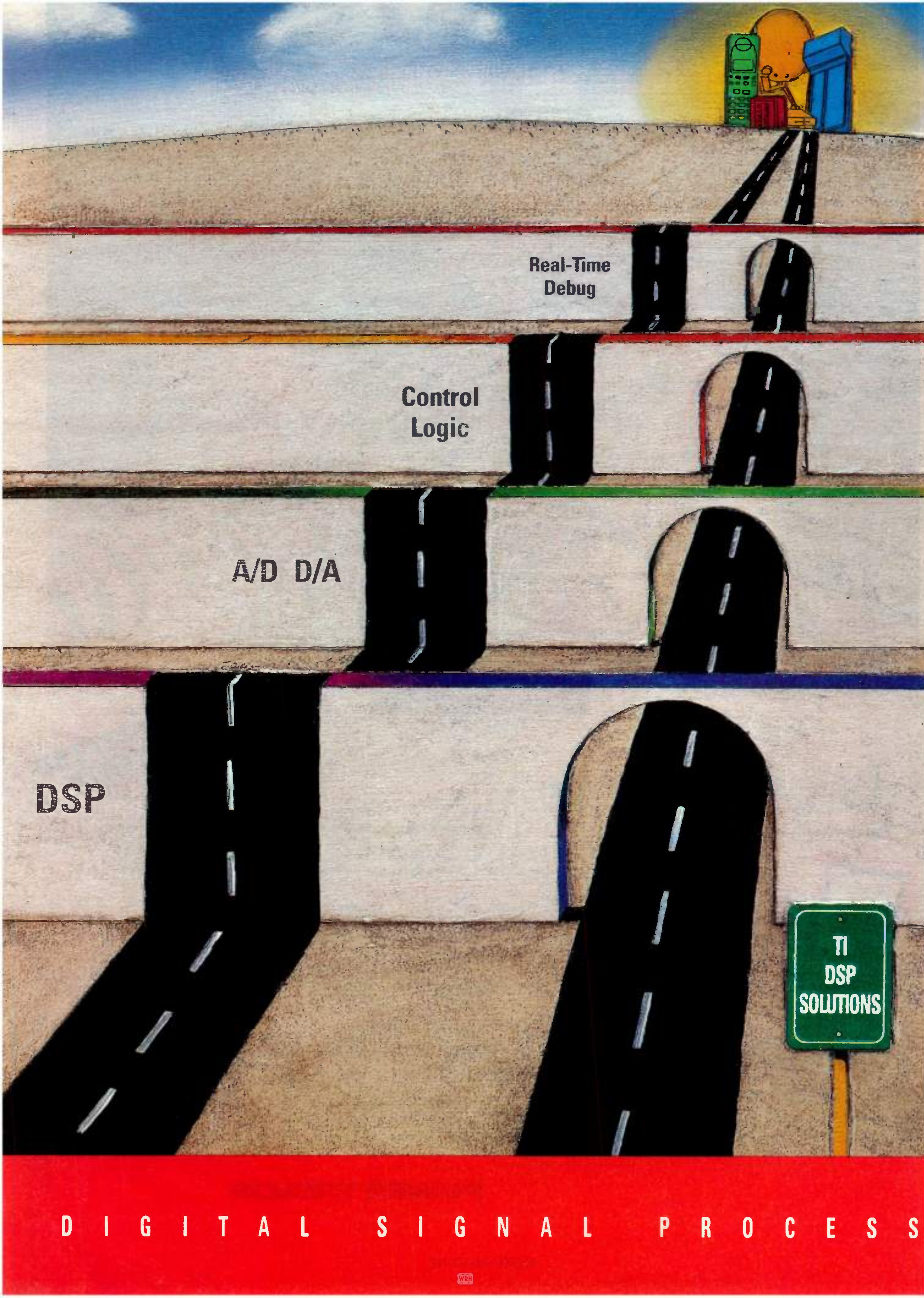
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eral-purpose register file, an integer unit with ALU, a pipelined 32-bit multiplier, and dual 64-bit accumulators, and a memory unit that controls access to the caches *(Fig. 4b)*. When performing encoding, the chip employs both of the 250-MHz cores. The first performs the steps of coding mode decision, subtracting the previous frame, discrete cosine transformations, quantization, rate control, and scan. The second processor performs the IQ, inverse DCT, and reconstruction steps, as well as system control tasks. Externally, just some DRAM for the data buffering and a motion-estimation chip must be connected.

### On The Edge

Eying visual communications, paper 11.2 describes the VLSI implementation of a single-chip encoder/decoder developed by the Department of Information Systems Engineering at Osaka University, Japan. The circuit incorporates a new scheme for a detailed edge detector that can seek the horizontal and vertical edges simultaneously, thus saving time. The circuit also can reuse the central processing element array for both the vector quantization and motion estimation, thus reducing the amount of on-chip logic, and keeping the chip area to 72.24 $mm^2$ and the power consumption to just 147 mW when running at 10 MHz. The chip can deliver QCIF images (176 by 144 pixels) at 10 frames/s with a bit rate of less than 30 kbits/s.

Tackling JPEG encoding and decoding, researchers at Sanyo Electric Co. Ltd., Anpachi-gun, Gifu, Japan, have a developed a compression and decompression chip that can handle VGA-size images (640-by-480 pixels) at up to 30 frames/s or handle still images with resolutions of up to 2048 by 2048 pixels. In their presentation, paper 11.3, designers at Sanyo described the new JPEG compression and decompression core that includes the DCT and inverse DCT, a quantization and inverse-quantization block, and the Huffman coding/decoding block. Most of the blocks can execute in parallel, thus reducing the time needed to process the data—the chip can average one symbol per clock cycle.

Discrete wavelet transforms will be the topic of paper 11.4 from the Department of Electrical Engineering at National Taiwan University, Taipei, Taiwan, R.O.C. The wavelet technology allows designers to implement a very efficient architecture for the one-dimensional discrete wavelet transform decomposition. The approach employs two stages of systolic decimation filter banks to guarantee a high throughput and optimal computation time. The wavelet technique decomposes data into components of different frequencies, such that there is good time resolution at high frequencies and good frequency resolution at low frequencies. This approach is good for analyzing signals that have discontinuities or sharp spikes.

Also in this session, a pair of papers, one from NEC Corp., Tokyo, Japan, and another by Texas Instruments (TI) Inc., Dallas, (papers 11.5 and 11.6, respectively) spell out in detail different approaches to audio decoding functions for Dolby AC-3 and MPEG playback. The NEC effort led to the creation of a building-block that can be added to a design library as a core. TI designers, on the other hand, crafted their decoder as a separate chip with a dedicated 16-bit RISC processor at its center.

# High Frequency Dominates CICC's Analog World

*Op Amps, Amplifiers, Filters, Photodetectors, Modulators, And Data Converters Are All On The Agenda.* **PAUL McGOLDRICK**

In recent years, the CICC has been accused of being just a little too commercialized. However, at this year's event, attendees may find it refreshing to experience a range of analog technology papers that are much less commercially-oriented and are more in the research spirit that IEEE conferences usually are.

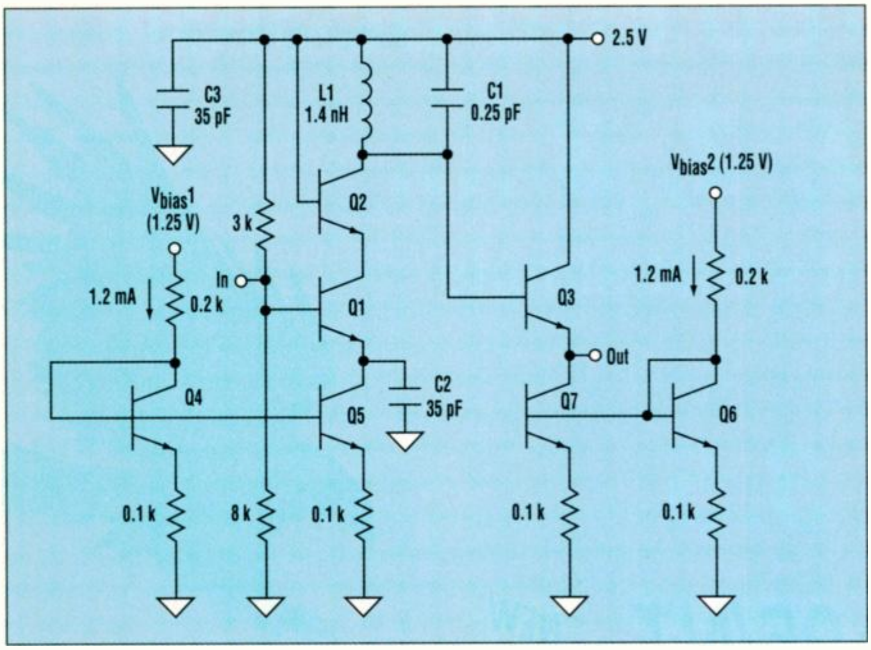
In the analog world, the preponderance of development work appears undoubtedly at the high-frequency end of the spectrum. Although there also will be a number of low-power, low-voltage designs presented for sample-and-hold uses, op amps, and log amplifiers, many of these designs are intended for further penetration of the RF market by reducing cost, improving performance, or just changing the parameters about how we think about some problems.

An invited paper from the University of California at San Diego looks at the thorny area of what technology will win out for which part of the integration of the single-IC radio. The extremists at either end of the process spectrum won't like the results, but the analysis presented makes sense.

In some other papers, researchers detail several single-chip receivers, but the circuits were designed for somewhat specialized applications rather than serve as a general-purpose receiver. Additional presentations at the conference describe research on low-voltage circuits that operate at supply levels of 1 V.

### Analog Techniques

Sample-and-hold amplifiers (SHAs) are crucial pieces at the data-acquisition interface of multi-step analog-to-digital converters (ADCs) and also serve as timing and bandwidth-limitation solutions at the input of one-step flash and interpolative-architec-




**1. Fabricated with a production SiGe process, this low-noise amplifier developed by IBM operates at 6.25 GHz and exhibits a minimum noise factor of 2.2 dB and a gain of 20.4 dB.**

ture ADCs. SHAs are fundamentally difficult to design because they are always the limiting factor in the overall performance potential of the acquisition system.

Behzad Razavi, a researcher at the University of California at Los Angeles, provides an overview of design techniques for SHAs in high-speed, low-voltage ADCs with various architectures (paper 5.1). Some design examples for newer developments are described covering a series CMOS sampler, distributed sampling, switched emitter followers, all-npn series sampling, and speed-up using an emitter follower and current impulse in a biCMOS SHA.

Particularly useful is a novel technique for measuring the output spectrum of an SHA by re-sampling with another SHA integrated on the same chip, guaranteeing that the second SHA only samples the held levels, and also relieving problems of 50-Ω terminations in testing.

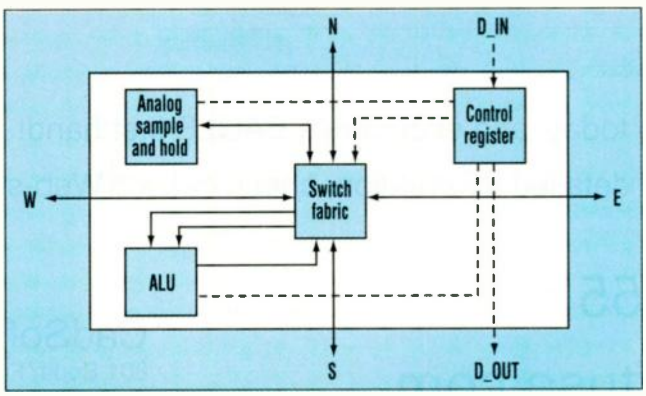
Analog Devices Inc., Wilmington, Mass., describes a wideband sampler based on a charge-domain gated $g_m$ cell. The sampler yields a measured spurious-free dynamic range (SFDR) of 72 dB at 160 Msamples/s with a 320.25-MHz input frequency (paper 5.2). Instead of a switched current source in the tail of a differential pair, the charge-domain device uses a charge source in the tail; a fully-depleted charge transfer creates the sampling pulse that changes domains from the input voltage signal to the output charge signal.

The test cell has been implemented in a 2-μm CMOS/CCD technology. Two different test set-ups were required to measure performance in both the signal and noise arenas. SFDR was constant from low frequencies up to 320 MHz, and then fell fairly steadily to 55 dB at 960.25 MHz. Simulations suggest that about 18 dB might be added to the SFDR. The small area used by the sampler also suggests that practical architectures could use multiple samplers, also making the circuit suitable for other applications such as ultra-low-power discrete-time amplifiers.

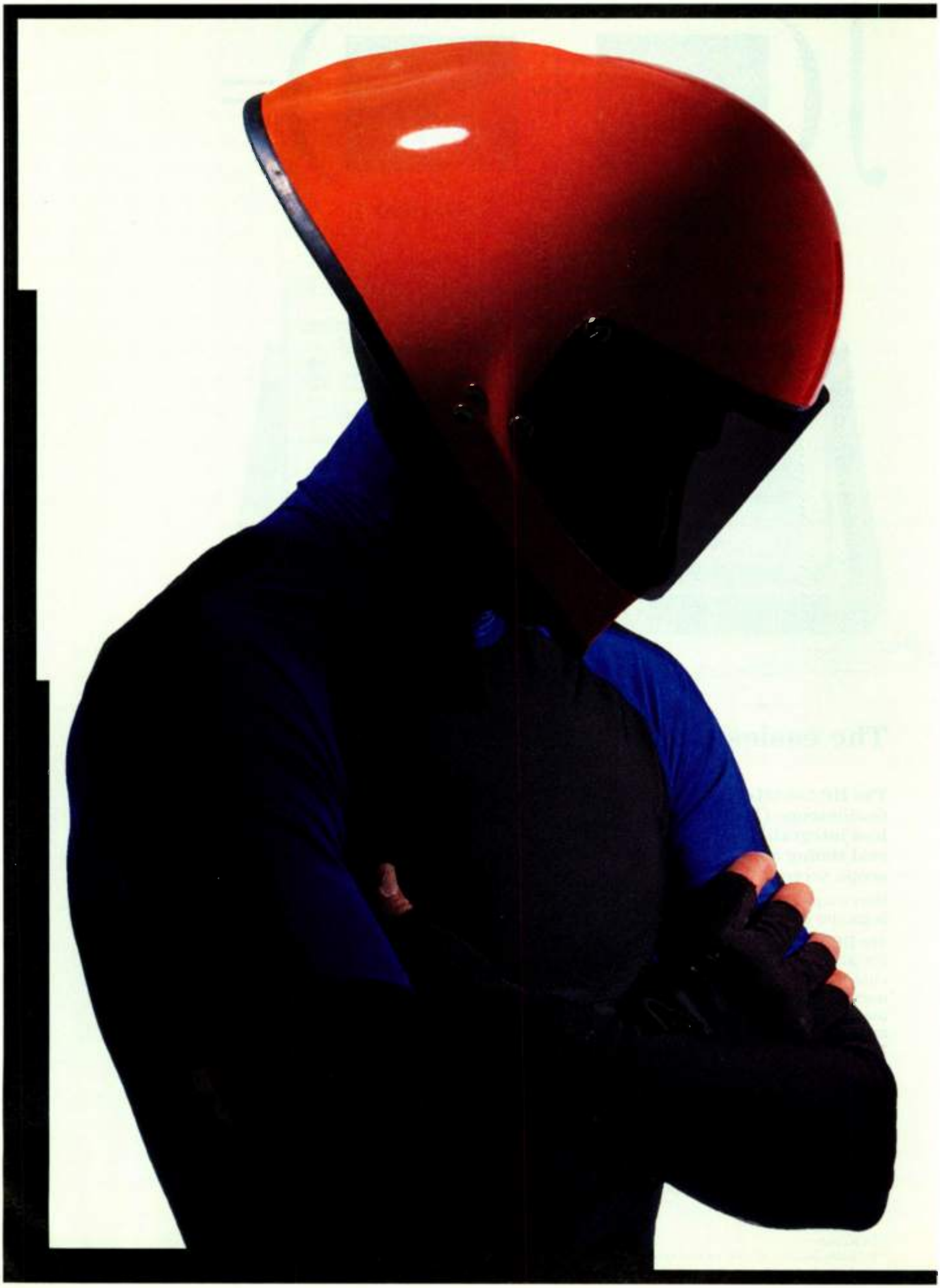
Fully-balanced analog circuits offer the best immunity to interference from digital noise, a situation typical in mixed analog/digital circuit implementations. Existing examples of fully-balanced circuits require complicated design procedures such that the designer has to start from scratch even if a single-ended version of the circuit exists. Two new general methods of a fully-balanced design are presented by Toshiba Corp., Kawasaki, Japan (paper 5.3). The designs help to considerably reduce the design time and still yield high-performance results; the systems use a new architecture that can be directly related to the single-ended circuit.

In what has become a year of op amp developments, the Catholic University of Leuven, Heverlee, Belgium, describes a fully-differential CMOS op amp with a complementary rail-to-rail input stage and a Class AB output stage (paper 5.4). The input stage has a novel biasing scheme that uses a current-regulating loop to keep the sum of the biasing currents constant. The $g_m$ variation is less than 4% while the 0.7-μm CMOS technology can handle supply rails from 1.5 to 3.3 V. The unity-gain bandwidth is 4.3 MHz with a load capacitance of 15 pF and a power consumption of 300 μW.

Helsinki University of Technology, Espoo, Finland, will present two papers associated with their design work for digital communications. The first paper involves a new temperature-compensated logarithmic amplifier that uses seven cascaded limiting current amplifiers for piece-wise approximation of the log function, and a current peak detector for a 60-dB dynamic range of signal amplitude with a temperature accuracy within ±1 dB from -20 to +80°C. The amplifier was built in a 1.2-μm CMOS process and can operate with a supply as low as 2.2 V while




**2. The individual cell architecture of a multiple cell array developed at the Massachusetts Institute of Technology for mixed-signal calculations of pixel values in early vision applications. The results are then sent off-cell for additional processing.**



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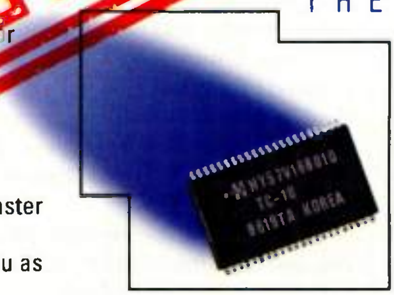


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|---|---|---|---|---|
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| 32MB | 4M x 72 | 3.3V | 66/83/100MHz | 4k |
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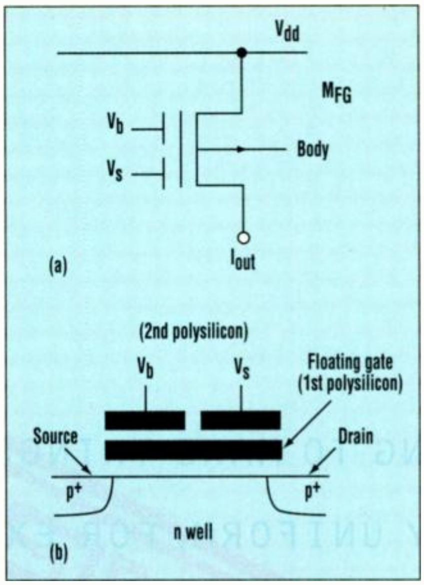
consuming about 3 mW (paper 5.5).

The second paper discusses the design, for Nokia, of a 3-V, $g_m$C-filter with on-chip tuning for the low-voltage channel selection for CDMA communications (paper 5.6). The chip also has a low current consumption (typically 16 mA) and employs a novel floating-resistor transconductor. The seventh-order elliptical ladder filter uses 14 transconductors with an extra one on the input to compensate for a 6-dB loss in the prototype.

The filters are tuned with capacitor matrices that employ a 5-bit digital control interface. This approach uses more chip area than does tuning the transconductor, but it also has a lower power consumption. Results show a passband gain in excess of 30 dB, a ripple of less than 1 dB, and a minimum stopband rejection of 57 dB. The circuit is fabricated on a double-polysilicon, double-metal, 1.2-µm CMOS process.




**3. The University of New South Wales' floating-gate MOSFET current source in circuit form (a), and its cross-section (b). The two-input gate structure allows for device operation in a DAC to be at less than 1 V.**

## Advanced RF ICs

The whole topic of high-level integration for wireless communications is liable to bring out as many opinions as there are people asked. An invited paper from Lawrence Larson from the Center for Wireless Communications at the University of California at San Diego, summarizes the trade-offs between the competing technologies in what is a hugely complex arena that many would argue from their own vested interests (paper 9.1).

The predictions are that the semiconductor content of a cellular handset will fall from the current \$76 to about \$58 by the year 2000, primarily because of the increased integration using CMOS. The logical extension of such CMOS integration to the radio functions to form a "single-chip CMOS radio" might seem plausible but the technical requirements are considerably more multidimensional. Compared to the digital IC, where power, speed, and yield are the major performance metrics, the RF IC also has to contend with issues of noise, linearity, gain, and efficiency.

Larson covers the systems requirements and the candidate technologies with time-to-market issues as well as performances. "In these areas," Larson concludes, "traditional silicon bipolar and GaAs technologies possess an edge at this time. Nevertheless, in the long run, CMOS technology will acquire many of these qualities, and silicon bipolar and GaAs technologies will find themselves increasingly pressed by competition with CMOS in the 1-to-2.5-GHz frequency range. RF CMOS is one of the most actively researched areas in the integrated circuits community."

One of the newer technologies, silicon-germanium, (SiGe), was able to report on a low-noise amplifier (LNA) at this year's International Solid-State Circuits Conference with a 0.95 dB noise figure, a power gain of 10.5 dB and a 2-mW power dissipation at 2.5 GHz. That results in a figure-of-merit of about 5.5 $mW^{-1}$ {gain/(dc power × noise figure)}. At CICC, impressive numbers also are reported for a 6.25-GHz LNA using SiGe with a minimum noise figure of 2.2 dB, a gain of 20.4 dB and a dissipation of 9.4 mW, from IBM's T.J. Watson Research Center, Yorktown Heights, N.Y. (paper 9.2). The LNA was fabricated using the company's standard production-level technology with three levels of aluminum metallization and conventional intermetal dielectric layers.

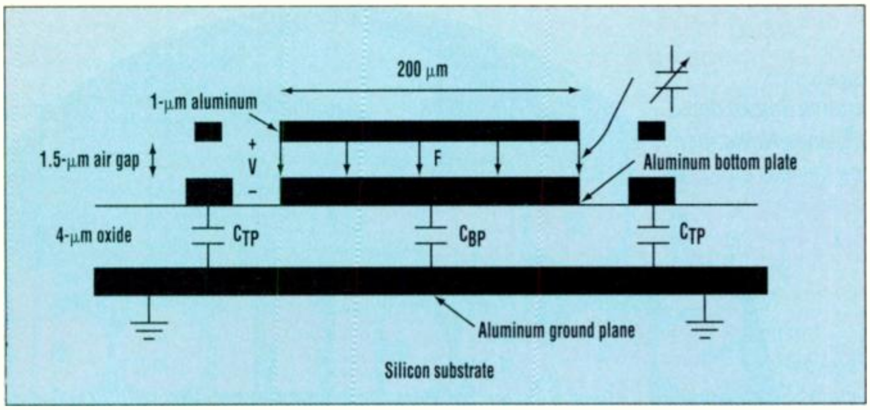
The LNA consists of a cascode amplifier with an emitter-follower output stage *(Fig. 1)*. The effective impedance of the on-chip tank LC load is increased with the common-base cascode transistor (Q2) while the input transistor is biased with a resistive divider. Current mirrors (Q4 and Q6) provide bias currents to the current sources (Q5 and Q7) in the two stages. Capacitor C2 bypasses the current source in the input stage and also modifies the input impedance.

The circuit was designed for operation at 5.8 GHz but a process change modified the specific capacitance of the on-chip capacitors to set the peak at 6.25 GHz with the 3-dB bandwidth extending from 5.5 to 7 GHz. A higher figure-of-merit could be achieved by replacing the input current source with an inductor, reducing supply-rail needs to about 1.8 V and reducing power consumption.

What is probably the first integrated front-end receiver with an integrated image filter will be reported by Carleton University, Ottawa, Canada, and Nortel, Ottawa, Ontario, Canada, for the 1.9-GHz DECT band (paper 9.3). Using an external 2.2-GHz local oscillator for high-side mixing, the input LNA is followed by an image reject filter tuned at the image frequency of 2.5 GHz positioned before the Gilbert mixing cell for conversion to the IF. Conversion gain of 33.5 dB is achieved with a noise figure of 4.9 dB and 50 dB of image rejection at 2.5 GHz. The image rejection can be tuned over the 2.4-to-2.63-GHz range. The part was fabricated in Nortel's 0.5-µm silicon bipolar technology that provides an $f_T$ of 25 GHz. Current consumption is 15.9 mA at 3 V. Further work is taking place to improve linearity and to match the RF input.

Hewlett-Packard (HP) Laboratories, Palo Alto, Calif., reports a significant breakthrough in RF power amplifier technology with a 1-W monolithic 800 to 900-MHz low-cost digital CMOS device operating at only 2.5 V (paper 9.5). Typically, a GaAs, LDMOS, or biCMOS amplifier for these frequencies required a supply of about 5 V to achieve a 1-W output. Although the HP amplifier is primarily designed for constant-amplitude applications, the potential exists for linearization using envelope elimination and restoration techniques.

Input matching to the power amplifier is provided by a T-network transforming a 200-Ω resistive load to 50 Ω.




**4. A micromachined variable capacitor, built on a silicon substrate that can be included in monolithic devices such as VCOs, was developed at the University of California at Berkeley. The capacitance is adjusted by bias voltage's electrostatic action that moves the more flexible plate closer to the fixed plate.**

Gain stages were fabricated as bandpass stages with inductive loads, needing no dc headroom and avoiding the low-frequency saturation problems of cascaded differential-pair amplifiers. Three stages, working in the Class A mode, then in Class AB, drive the third stage at the rail-to-rail voltage for Class C/D operation to drive a switched-mode output stage, similar to a Class-D amplifier. Small-signal gain is better than 30 dB with power-added efficiency at 42% for the 0.8-µm fabrication process.

One of the limitations on the implementation of direct-conversion receiver techniques is the process of local-oscillator (LO) self-mixing, where leakage of the LO signal back to the input amplifier stage and the antenna is reflected back to the mixer where it is converted as a dc offset. A balanced harmonic mixer from Toshiba Corp., Kawasaki, Japan, has a structure that is inherently symmetrically balanced, separating the LO, RF and baseband signals (paper 9.6). The measured results show that dc offsets caused by self-mixing are reduced to levels that are less than the noise level.

## DVB, Filters, And Arithmetic

Hyundai Electronics Industries, Kyoungki-do, Korea, and Odeum Microsystems, San Jose, Calif., present an elegant single-chip DVB-compliant receiver with variable-rate QPSK demodulation, Viterbi decoding, de-interleaving, and Reed-Solomon decoding (paper 11.7). Using a fixed-rate sample clock, the design seamlessly handles data rates from 1 Msymbol/s to 45 Msymbols/s.

The symbol rate can be controlled within 0.01% of the desired value with possible timing errors corrected through a symbol-tracking PLL. The Viterbi decoder accepts 3-bit soft-decision samples of the I and Q components of the received signal with the core architecture tuned to a rate of 1/2. Depuncturing logic with an associated FIFO buffer precedes the core logic to equalize the data rates for the higher data rates of 2/3, 3/4, 5/6 and 7/8.

Unlike conventional schemes where the encoder output is re-encoded to compare with the input to verify synchronization, the scheme here is to use the principle of convolution coding such that the convergence length is substantially different in the in-sync and out-of-sync conditions. A novel change also is made in the Reed-Solomon decoder, where one Euclidean ALU with its associated register arrays is time-shared to replace 16 ALUs. This block is clocked at twice the speed of the others in order to keep up with the input data. The result is that the decoder has been implemented with fewer than 14,000 gates.

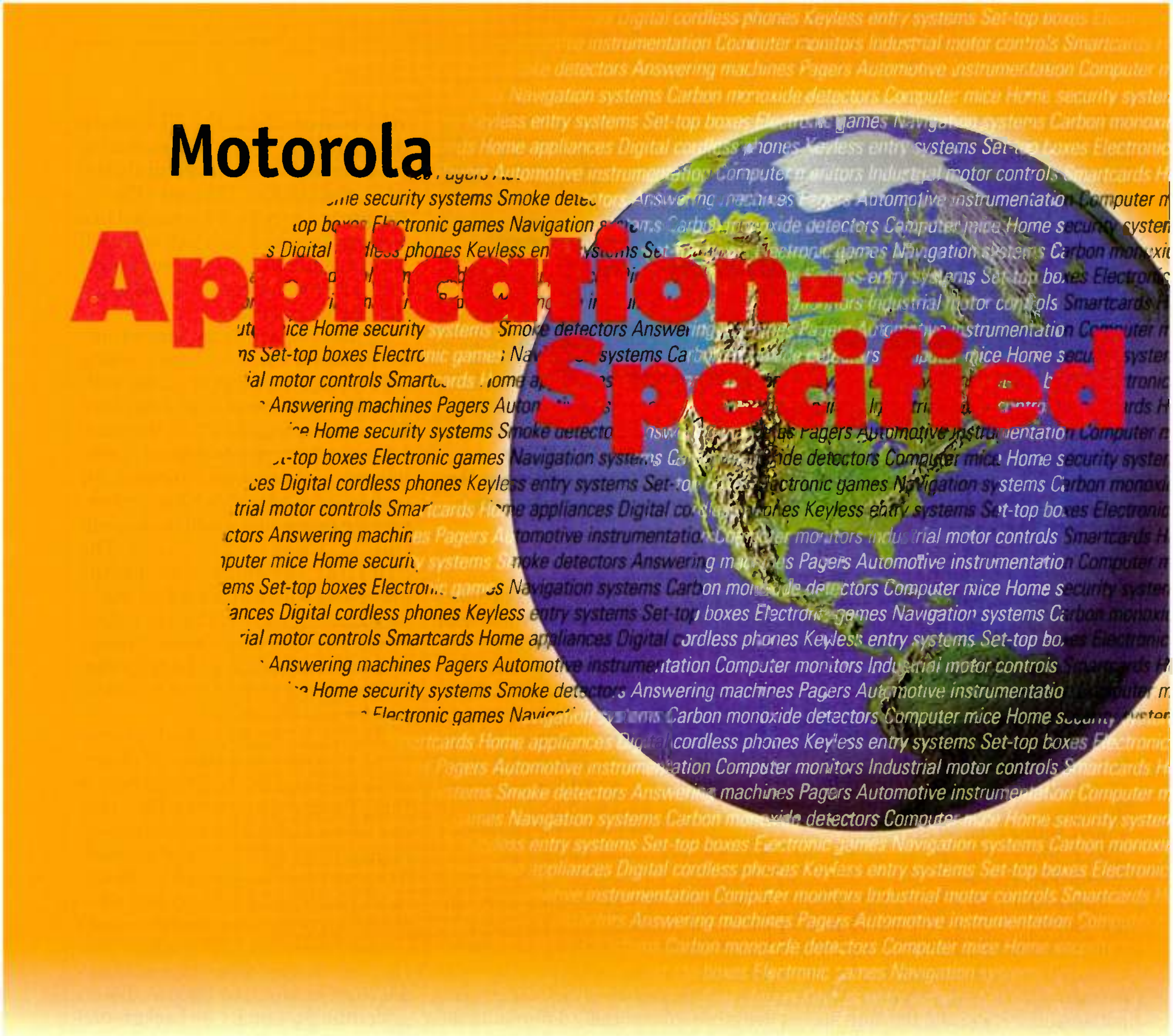
A programmable analog arithmetic circuit is presented by MIT, Cambridge, Mass., with addition, subtraction, multiplication, and division at 7 bits of resolution (paper 12.6). The circuit was designed for use in early-vision systems and can allow low-power operation while retaining most of the flexibility of a digital processor. The architecture of a single cell consists of a digital control register, an analog SHA to store data, the ALU and a switch fabric, which routes analog data among the storage unit, the ALU, and the four I/O lines *(Fig. 2)*. The processor cells are arranged in a rectangular array in which each cell can communicate with its four neighbors, all of which can be executing a different instruction.

In the complete array, limited only be the size of the die, the processing cells receive a stream of analog voltages from the imager for each pixel. The system requires that the pixel values and any mathematical operation from its neighbors are used for such tasks as edge detection. Any remaining processing would be done off-chip in a digital processor. The ADC/DAC combination used in the processing is limited in the first implementation by the fact that the output cannot go above the reference voltage or below zero. As a result, outputs cannot be higher than 255 or be below zero for subtraction.

A position-sensitive photodetector using CMOS with a 16-by-16 binary array is discussed by the University of Oulu, Finland (paper 12.7). The array can detect multiple spot positions simultaneously with sub-pixel accuracy. The array consists of a 16-by-16-element photodetector array and additional circuitry for global threshold setting, re-setting, and readout. Settings can be done from either an external current input, or from a current generated internally by background illumination sensors in the vicinity of each array corner. These sensors consist of four photodiodes sized the same as the pixel photodiodes, thereby producing the same current levels. The triggering level can be set from 0.5 to 4 times the average background illumination levels.

## Data Converters

An invited paper from the Catholic University of Leuven, Heverlee, Belgium, discusses the problems encountered as voltages are lowered on CMOS ADC operations (paper 13.1). At a supply rail of less than 2 V, it is no longer possible to implement switched-capacitor converters. That is due to the fact that there is no longer enough overdrive to turn on the transistors used as switches. Techniques will be discussed in the presentation to

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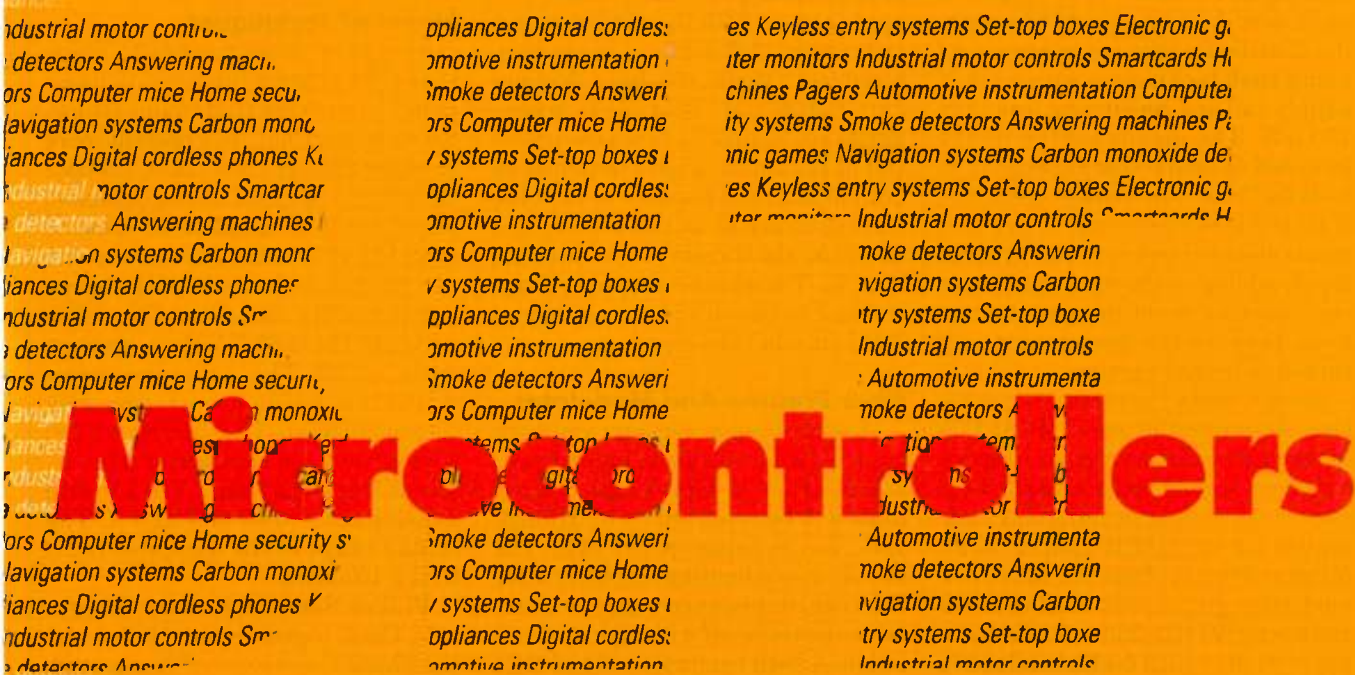


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show how to employ switched op amps instead of the voltage-multiplying techniques that have been suggested up to now. A 12-bit, Δ-Σ ADC operating at audio frequencies is introduced using such techniques with a 1.5-V supply rail and consuming less than 100 μW. The disadvantage of the switched op amp is that although it allows for "true" low-voltage operation, it introduces additional active elements at each integrator, except at the input, adding to the die area. Power consumption is not increased, however, because the devices are only turned on for half the time.

Oregon State University, Corvallis, Ore., describes the use of MOSFETs in their accumulation region as capacitors for a second-order switched-capacitor Δ-Σ modulator, using only basic digital 1.2-μm CMOS (paper 13.2). Measured results from the 16-bit, 3-V modulator give a peak SNR of 96 dB and a peak S/THD (2nd to 5th harmonics) of 94 dB with a 6-kHz bandwidth, 5.4-mW dissipation and a 3.6-V capacitor bias. The results show that it is possible to design high-linearity switched-capacitor circuits without double-polysilicon capacitor techniques. The prototype suffered from requiring large drive voltages which should be corrected by increasing the input capacitors.

A more conventional implementation using capacitors will be presented in paper 13.3 by researchers at the Nokia Mobile Phones R&D Center, San Diego, Calif. In their design of a second-order demodulator, they fabricated high-resolution Δ-Σ DACs with a 0.5-μm low-power CMOS process, employing double-polysilicon and triple-level metal interconnections. The design neatly combines the DAC and second-order filter into the same step, eliminating the conventional post-analog filter. The resulting reduction in die size to 0.18 mm$^2$ and power to 700 μW are impressive, along with a dynamic range of 85 dB and an audio bandwidth of 300 to 3400 Hz.

A 0.9-V supply DAC has been developed by the University of New South Wales, Sydney, Australia, using a standard 1.2-μm CMOS technology. An experimental 6-bit DAC was fabricated and it exhibited less than a 0.46 LSB linearity error, a 5-Msample/s conversion rate and a power consumption of 320 μW. To operate in the 1-V supply range, a new floating-gate MOSFET current source was developed *(Fig. 3)*. Both the current-source and current-switch functions are combined into a single, two-input floating-gate PMOS transistor, MFG, whose inputs are $V_s$ and $V_b$. Since the potential of the floating gate depends on both inputs, it is possible to turn the current-source on and off with $V_s$, and to control the current output with the bias, $V_b$. The minimum supply voltage is equal to the threshold voltage of MFG plus the turn-on voltage.

## Fiber Preamp And Modulator

A wide-dynamic-range and high transimpedance silicon bipolar preamplifier for 10-Gbit/s optical fiber links will be reported on by Hitachi Ltd., Tokyo, Japan (paper 14.3). The circuit uses a limiting amplifier after the transimpedance stage to overcome the trade-off with high dynamic range. A 3-dB bandwidth of 10.5 GHz was achieved with a transimpedance of 1 kΩ, a dynamic input range of 2 mA pk-pk and an equivalent noise current input of 12 pA/√Hz using 35-GHz bipolar technology. The transimpedance fluctuation was only 0.5 dBΩ from 50 MHz to 8 GHz, attributed to the optimization of the function resistance and the bias network. The transimpedance could be doubled to 2 kΩ using the circuit's differential outputs. The device is linear for input currents of less than 400 μA pk-pk (400-mV output voltage.)

Hong Kong University of Science & Technology, Clear Water Bay, Hong Kong, and Broadcom Corp., Irvine, Calif., will present work on an all-digital implementation for a broadband PAM and QPSK modulator, avoiding the design pitfall of the separate DAC function at the transmitter being provided by a non-system designer (paper 14.5). Here, the transmit DAC and FIR filtering functions are merged with significant reductions in complexity. The modulator produces a direct analog output at either baseband or IF. The implementation is very efficient because all computations are performed in the analog current domain while the analog multiplier employs a current-division technique that is suitable for digital CMOS processes. Coefficient tap-weights are in digital form and can be easily modified.

## Novel RF Techniques

In one of those pushes to show that CMOS has a life outside baseband, Level One Communications, Sacramento, Calif., will present work in paper 20.3 on a low-noise, 1.6-GHz CMOS PLL with an on-chip, passive, loop filter. The complete IC consists of an LC VCO using spiral inductors, divider, phase detector with charge pump, and the loop filter. The reference used is at 61.5 MHz, a division ratio of 26. The reference tone feedthrough is below -80 dBc with phase noise at -105 dBc/Hz at 200 kHz offset from the carrier. The device is functional from 2.7 to 5 V with a dissipation of 90 mW at 3 V. The tuning range of the oscillator is 1.6 GHz ± 100 MHz.

Philips Semiconductors, Sunnyvale, Calif., together with UCLA and the Sharif University of Technology, Tehran, Iran, explains their work on a method for precise wideband quadrature signal generation, necessary for any number of modern wireless systems (paper 20.4). The oscillator output, fed from an integrator, passes through an improved ECL divide-by-two stage to give the quadrature signals. Any output phase error is converted to an error signal which is fed back to correct the difference. A phase accuracy of better than 0.5° was achieved over an output frequency range of 40 to 500 MHz without external tuning.

The scheme's accuracy depends on the phase detector that is a modified Gilbert cell. This must be highly symmetrical and the layout used was such that circuit and layout mismatches should also be corrected by the loop. The part is being called the level-locked loop (LLL) and is fabricated in 1-μm biCMOS.

Concorde Microsystems, along with the University of Tennessee, Knoxville, Tenn., will describe a single-chip, direct-conversion receiver for the VLF band of 10 to 100 kHz, providing both analog and digital I and Q outputs (paper 20.5). The VLF band has advantages for short-range RF sensing over the conventional portable bands. Up to about 100 feet, magnetic-wireless detection is simple, sensitive and requires


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United States  Europe  Latin America  Caribbean  Canada  Mexico  Japan no license. The receiver implemented consists of a low-noise preamplifier, a direct-conversion mixer with I and Q outputs, and dual baseband IF stages with pin-programmed gain. The I and Q local oscillator signals are also pin-programmed in the PLL followed by a pin-programmed post divider. The receiver is designed for the reception of phase-modulated signals in the 10 to 100 Hz range.

The University of California at Berkeley presents work on a micromachine-based variable capacitor for VCOs (paper 21.3). The capacitor is fabricated on a silicon substrate allowing its incorporation in a monolithic design *(Fig. 4)*. The capacitor consists of a thin aluminum plate suspended in air nominally 1.5 µm above a bottom aluminum layer and anchored with four mechanical folded-beam suspensions acting as springs. The low sheet resistance allows for the achievement of high Q factors. The size of the plate is a compromise between the achievable capacitor values and the warping of the plate. With a chosen plate size of 200 by 100 µm, the nominal capacitance is 200 fF.

When a dc bias is applied across the capacitor, an electrostatic force pulls the top plate down, reducing the air-gap and increasing the capacitance by up to 50%. A prototype VCO built using the technique in a Colpitts configuration and with a commercially available inductor achieved a 400-fF tuning range from a nominal capacitance of 800 fF. The circuit, where the parasitics increased the overall capacitance to about 2 pF, exhibited a measured Q of 62 at 1 GHz.

A GSM receiver will be described by Bell Laboratories (Lucent Technology), Murray Hill, N.J., using a modified low-IF conversion process (paper 24.4). The process has the LO and RF bands overlapping so that the output IF is low, but not actually direct conversion. This avoids some of the current problems of direct conversion with significant demands on the baseband filters.

However, when the dc offsets are moved away from the IF sufficiently, ac coupling can simply be used to remove them. The dynamic range issues that are present with direct conversion are still a concern with low-IF techniques, and Bell experimented with a double-low-IF (DLIF) receiver that reconverts the low-IF outputs back up to frequencies where low-cost ceramic filters can be effective. The low-pass filters at the first IF need only be low-order to provide image rejection for the second conversion. For GSM, Bell used half the channel spacing for the first IF (at 100 kHz) and then used 10.7 MHz for the second, a standard in consumer applications.

# EDA-Tool Improvements Advance Next-Generation Circuit Designs

*Submicron, RF, Clocking, And Low-Power Design Solutions Emerge At CICC.* **CHERYL AJLUNI**

With the EDA industry migrating to smaller-geometry designs while incorporating greater complexity with higher-speed and lower-power circuitry, designers are faced with many challenges. All too often, there's just not enough time or money to search for solutions. In fact, many designers are forced to piece together makeshift solutions from a grab bag of current design flows and available tools. Even though this approach has a number of limitations, it gets the job done. For the typical designer working against tight time-to-market deadlines, just getting the design out of the door is the bottom line. But for some, the special challenges of deep-submicron, radio circuit, system clocking, and low-power designs, make even achieving the bottom line a difficult task.

As designers venture into the deep-submicron design area, they are faced with many issues that didn't exist previously. The complete domination of gate delays by interconnect delays, and the emergence of a host of issues related to device parasitics have questioned the very usability of current tools and methodologies. Toward this end, two sessions at the CICC, Session 8—Analysis For Deep Submicron, and Session 26—Physical Design Automation, take a hard look at many of the concerns and issues related to deep-submicron design and current feasible options for designers floundering in a state of confusion.

## Gigascale Challenges

In Session 8, Paper, 8.1, from researchers at the Georgia Institute of Technology, Atlanta, details the derivation of a stochastic interconnect distribution for gigascale integration (GSI). The distribution can be used for on-chip random logic networks and describing optimal architectures for multilevel wiring networks. This multipurpose derivation can be employed in a number of ways: to enhance a critical-path model for clock-frequency estimation, to estimate dynamic power dissipation in signal wires, or to determine the optimal scaling of the cross-sectional dimensions of interconnects in a multilevel network. With this interconnect information chip size can be determined.

Compared to other distributions which describe only local interconnect requirements, this new distribution offers an all-encompassing description of local, semi-global, and global wiring requirements. The researchers used the optimized three-tier network distribution on a test chip and effectively showed that it could provide a 0.46X


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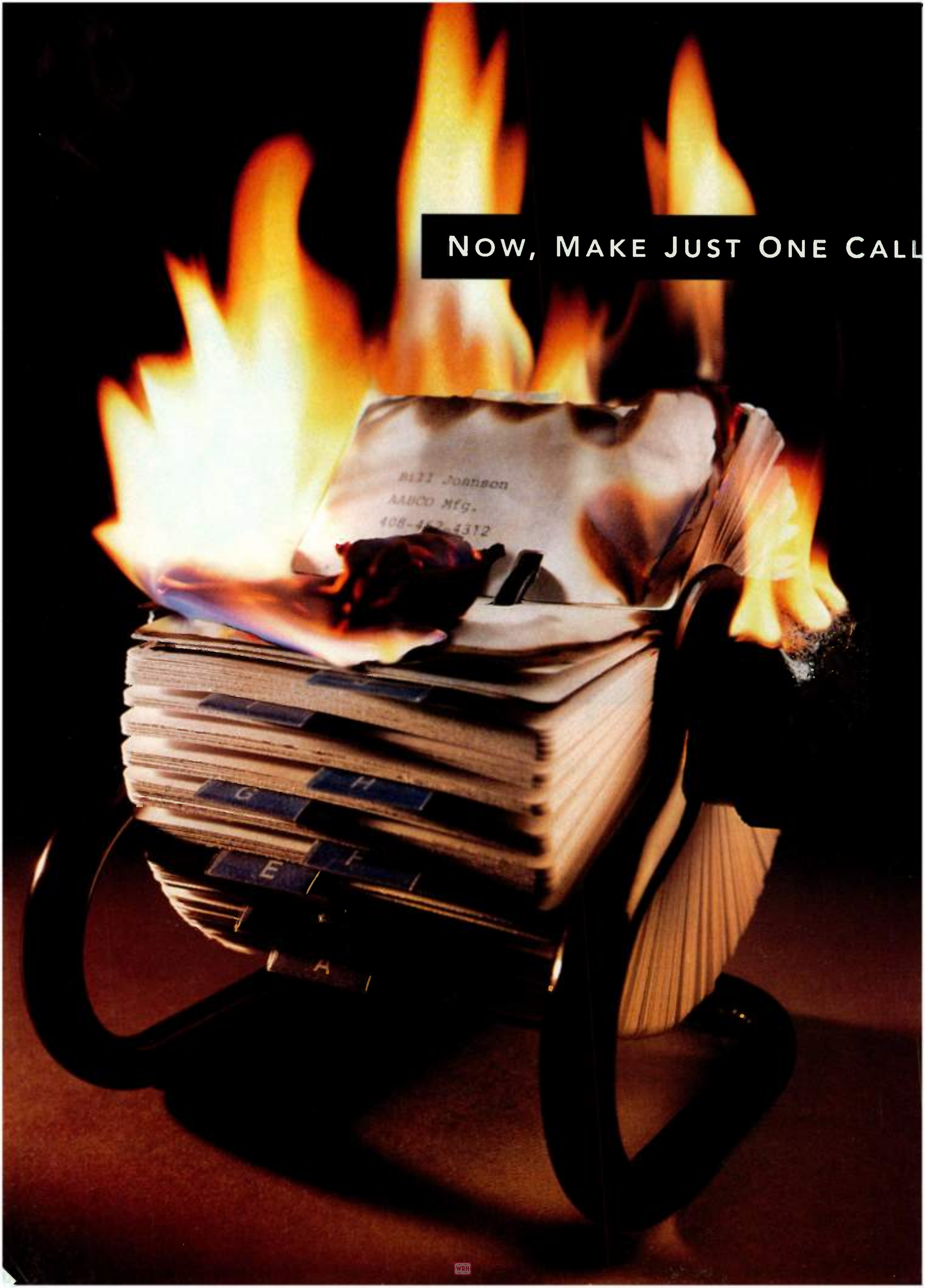
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reduction in chip size, or a 1.7X increase in clock frequency over the more conventional two-tier design.

Inherent in the ability of designers to design ICs is the use of accurate and complete models for circuit simulation. Without these models, it is virtually impossible to correctly characterize the circuit elements and parasitics that comprise the IC. Papers 8.2 and 8.4, from Motorola Inc., Tempe, Ariz., and Carnegie Mellon University, Pittsburg, Penn., respectively, address the issue of accurate models.

Paper 8.2 provides more of an overview of the issues related to compact modeling. Details of some of the common and not-so-common guidelines for compact modeling and characterization are offered, along with some of the typical numerical weaknesses and corresponding solutions. In addition, researchers examine some of the often-overlooked aspects of high-frequency modeling.

Conversely, Paper 8.4 describes a technique for generating sparse RC-interconnect macromodels. The technique works by inserting an artificial intrinsic delay in the transconductance terms between distant ports. This design is possible thanks to the low-pass filter characteristic of the RC-interconnect circuits. It effectively lightens the computational load during circuit simulation. With the delay in place, the ports are decoupled. Because any error that has been introduced can then be measured in terms of the poles and residues of the RC circuit, accuracy versus sparsity trade-offs can be easily made.

## Constraint-Driven Placement

Session 26 attacks the deep-submicron issue from another angle by examining the placement and routing (P&R) problems with their corresponding solutions. In Paper 26.1, Cadence Design Systems, San Jose, Calif., details the development of a new constraint-driven placement tool. This tool, the Device-Level Placer (DLP), attacks the problem of full-custom mixed-signal design by providing the designer with a quick way of obtaining feasible layout configurations and exploring the effects of applying different sets of constraints.

The DLP software works by using a direct approach based on a combination of techniques. These techniques include a force-directed placement, augmented by a min-cut partitioner that has been modified to guarantee the enforcement of an entire set of geometric constraints and iterative optimization. Any infeasible P&R configurations, typically due to overconstraints, are automatically detected and the designer is notified. The tool is capable of handling full-custom layouts of cells with large sets of geometric constraints.

Paper 26.4 addresses a technique for placement of large-scale gate arrays using a fast-placement-improvement algorithm. Developed by Mitsubishi Electric Corp., Hyogo, Japan, the algorithm consists of a new cell-padding phase and a fast-iterative-improvement phase. In the padding phase, local-routing chip congestion is reduced by expanding the size of the cells in the congested regions and relocating them to eliminate the cell overlap. Relative-cell positions are preserved throughout the relocation process. The iterative improvement phase then minimizes the objective function that takes the local congestion into account. Its speed is derived from the use of a new gain-estimation method to determine the best position in which to move a cell.

Papers 26.2 and 26.3 from the University of Washington, Seattle, and NTT System Electronics Laboratories, Kanagawa, Japan, respectively, focus on routing. The first paper offers a solution to the over-the-cell routing challenge that occurs in VLSI physical-design automation. A newly developed, multilayer, graph-based router that can handle obstacles on any layer, specifically addresses this problem. It works by improving the performance of a maze router with rip-up and reroute (R&R) capability.

The second paper presents an overview of a routing methodology and CAD tools used in designing a gigabit/s LSI IC with deep-submicron technology. Net-classification techniques are employed, along with a high-performance router and a high-precision delay analyzer. The analysis is based on a top-down/bottom-up hierarchical approach. To show the use of the tools, the presentation describes how the methodology was employed to design an ATM switch-element LSI using 0.25-µm CMOS/SIMOX technology. The resulting chip had a throughput of 40Gbits/s and an internal clock frequency of 312 MHz. Designing radio circuits for use in the wireless/personal communications electronics market is another area that poses difficulty for today's designer, and is addressed in Session 24—Radio Circuit Design Techniques. The challenge is how to effectively deal with the section of the system operating at RF.

Many designers would like to be able to deal with RF the same way they deal with analog—by breaking the design into blocks, then simulating the different blocks separately. The blocks are then brought back together towards the end of the design cycle. All too often, though, when this method is used, interface problems occur that can wreak havoc with a design. And, with the signal frequencies, time constraints, and types of analysis required in RF design, using simulators such as Spice often results in poor accuracy, and drains on computation resources.

## Better Simulation Tools

A few general- and special-purpose simulation tools have emerged in recent years specifically targeted for use in RF design, but, generally, they have not been understood well enough to be used properly. Paper 24.1, a combined effort from researchers at Washington State University, Pullman, Wash.; Lucent Technologies, Murray Hill, N.J.; Bell Labs, Allentown., Penn.; and Lucent Microelectronics, Allentown, Penn., specifically addresses this lack of understanding by attempting to demystify the features and limitations behind some of the tools currently available.

Some of the basic concepts related to RF design, as well as RF simulation techniques, also are presented. The rest of the session details the methodologies used and results of work done on five RF-based designs including a 900-MHz RF low-noise amplifier in a 0.9-µm CMOS (University of California, Los Angeles in conjunction with Broadcom Inc., San Jose, Calif.), a 2-V low-power single-ended 1-GHz CMOS direct-upconversion mixer (KU Keuven, Heverlee, Belgium, Lucent Technologies and Bell Labs , Murray Hill, N.J.), a biCMOS double-low-IF receiver for GSM (Samsung Electronics Co. Ltd., Kyunggi, Korea), a fully inte-

grated 5-MHz-IF digital FM demodulator (University of Illinois, Urbana), and a completely integrated single-chip PLL with a 34-GHz VCO using 0.2-μm E-/D-HEMT-Technology (Fraunhofer Institute of Applied Solid-State Physics, Freiburg, Germany).

Another session, Clocking And Low Power Methodologies (Session 7), takes a hard look at how the increasing demands of VLSI chip design continue to challenge the limits of power and performance, specifically focusing on workable design and analysis techniques. A total of seven papers cover a variety of topics including a 3D parasitic distributed RLC extraction method for evaluation of the clock delay of VLSI multilevel interconnects (Texas Instruments Inc., Dallas), and a genetic algorithm approach for estimating the maximum power dissipation and instantaneous current through supply lines for CMOS circuits (University of California at Santa Barbara).

Of special interest is a hierarchical decomposition for single-stage clock designs presented in Paper 7.1. The technique works by splitting the design into global and local distributions, and replacing the leaf wiring of the clock route with shortest-path-style routing. This technique, ideal for designing the interconnect distribution for single-stage clock circuits, can offer performance improvements in the 3X area, reduce the total wire used by 6%, and reduce the runtime by an order of magnitude on clock circuits with a few hundred to a few thousand latches.

Researchers from IBM Microelectronics, Essex Junction, Vt.; Cadence Design Systems, San Jose, Calif.; and First PASS, NW Palm Bay, Fla., in Paper 7.2, also report on the development of a comprehensive clock methodology. Specifically optimized for microprocessor designs or other large integrated functions containing smaller sub-blocks or cores, the methodology incorporates a number of different components. Some of those components include the clustering and balancing of clock loads, multiple-clock domains, a balanced clock router with variable-width wires to minimize skew, hierarchical clock wiring, automated verification, an interface to the Cadence Design Framework II environment, and a complete network model of the clock distribution, including loads.

The methodology provides for good performance, and is able to minimize the design time without consuming large amounts of wiring tracks or adding needless wiring capacitance. Researchers will report on how this methodology was used to create an entire clock network—including verification, in less than three days with a clock skew for the entire chip of approximately 180 ps.

In Paper 7.5, researchers from Toshiba Corp., Kawasaki, Japan, describe an automated design technique that reduces power by using two supply voltages. The approach employs an Extended Clustered Voltage Scaling (ECVS) structure for synthesis, along with P&R techniques. The structure synthesizer works by clustering the gates off the critical paths. This design effectively reduces the voltage, saving power. Then a P&R tool assigns either the reduced or unreduced voltage to individual rows to minimize area overhead. As tested on the random logic modules of a media processor chip, the combination of techniques was able to reduce the power by an average 47%, with a random logic area overhead of 15%. Additionally, no degradation in the performance of the chip was witnessed.

# New Architectures, ICs, Processes To Open Communication Frontiers

*Developments In Wireless And ATM Systems Are Featured At This Year's CICC.* **LEE GOLDBERG**

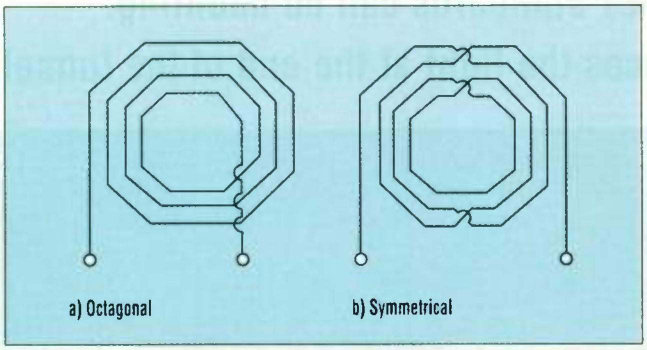
Making the ICs for the next generation of communications networks is not simply a matter of smaller, faster, and cheaper. While the speed and density of mircochips continues to climb at a surprisingly predictable rate, they are invariably outpaced by the performance requirements of the emerging Gigabit networks and universal wireless services. The real keys to electronics' steady evolution are the quantum-leap innovations that lie beyond Moore's curve, in the realm of solid-state physics, information theory, and advanced mathematics.

Developments presented at the CICC will pave the way not only for tomorrow's ICs, but will serve as a foundation for technologies whose impact will be felt for many years to come. While the conference has yielded a wealth of developments in all areas of communications, perhaps the two that will see the most activity are wireless and ATM systems.

## Wireless Developments

As wireless systems become more widely employed for both voice and data, several issues have arisen that may limit their aggressive price/performance goals. For example, the trend toward using on-chip passive components is very promising, but the performance limitations of micromachined capacitors and inductors are still far from ideal. In paper 20.2, "A Fully Integrated Spiral-L.C. CMOS VCO Set with Prescaler for GSM and DCS Systems," researchers from ESAT-MICAS, Heverlee, Belgium, and Toshiba Corp., Tokyo, Japan, describe a methodology for optimizing the design of spiral inductors, and how

it is applied to VCOs operating in the 900 MHz and 1.8 GHz regions. Designs were done with a standard 0.4-μ CMOS process. According to the authors, the inductor's series resistance and its parasitic coupling to the substrate must be minimized to provide the phase-noise performance and power efficiency required by cellular and PCS systems.




**1. These on-chip inductors were developed for use in high-performance VCOs that operate in the 900- and 1800-MHz region. An octagonal profile (a) yields a better inductance ratio than square profile inductors. The symmetrical configuration allows the use of a single inductor in a perfectly balanced differential oscillator (b).**

Rather than using exotic techniques such as forming inductors with bonding wire, the authors applied finite-element analysis and simulation to look at how the conventional method of forming them in the chip's metallization layers could be optimized. From this work, three important principles can be derived. The first states that the width of the conductor traces cannot be made extremely large, otherwise the inductor will suffer from excessive high-frequency resistance, due to increased skin effect. Next, the inductor's spiral must not be filled up with conductor traces to the middle of the coil, since the inner loops contribute much more to internal eddy current effects than to the component's overall inductance. Finally, a coil's surface area must be limited to minimize substrate losses.

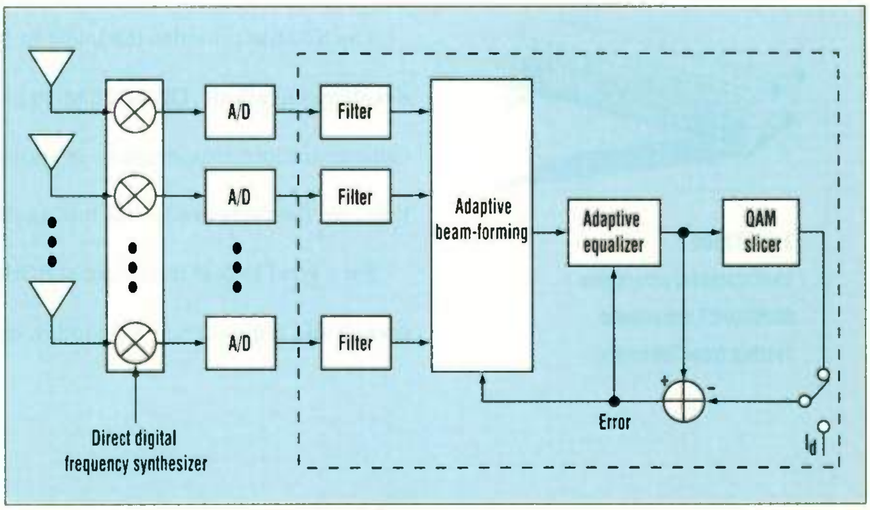
Using these lessons, an unusual coil shape was devised, which combined an octagonal profile (for better inductance/resistance ratio), and a nested symmetrical coil layout that minimized surface area and allows the use of a single inductor in a perfectly balanced differential oscillator (*Fig. 1*). The resulting designs yielded inductor Qs of 5.6 and 8.6 for the 900 MHz and 1.8 GHz oscillators, respectively, and were successfully incorporated into VCO/prescaler chips with excellent results.

Also in session 20, the Integrated Circuits And Systems Laboratory at UCLA, Los Angeles, Calif., will deliver a thorough overview discussing the "Challenges in the Design of Frequency Synthesizers for Wireless Applications" (paper 20.1). The presentation explains that frequency synthesis was more difficult to achieve than most electrical functions insofar as it involved performing algebraic operations on frequencies. This type of task is much more difficult than on more commonly manipulated properties, such as current and voltage. The authors also examined the challenges faced at the architectural and circuit design level, and provided a detailed analysis of the advantages and disadvantages of many of the most popular solutions (including integer-N, fractional-N, dual-loop, and direct digital synthesis) employed today.

Another area where significant advances are being made is in active antennas. Active antennas use phased-array techniques to shape their active region, allowing satellite systems, wireless LANs, and cellular networks to more highly segment coverage areas and resist multipath and fading effects. Generally, these systems have been bulky and expensive, but researchers from Broadcom Corp., Irvine, Calif., and the Integrated Circuits And Systems Laboratory at UCLA, will address the issue in their paper, "A 42-Mbit/s, Multi-Channel Digital Adaptive Beamforming QAM Demodulator for Wireless Applications" (paper 14.4). This presentation describes how advanced DSP techniques could be used to combine inputs from multiple antennas to create a "virtual" phased-array receiver.

The paper uses a wideband coherent M-ary quadrature-amplitude modulation (M-QAM) modem as an example. The modem they describe uses a frequency-hopped RF front-end, operating in the 2.4-GHz unlicensed ISM band. The receiver's adaptive beam-forming network is designed to reject co-channel interference or provide anti-jamming capability. A chip to perform these functions was fabricated in 0.8-μ CMOS. It is fed by a four-channel front-end that de-hops the signals from the antennas and feeds each signal to its own analog-to-digital converter (*Fig. 2*).

The digitized signals from the front




**2. A multi-channel, multi-antenna digital receiver can use its DSP capabilities to create an adaptive beam-forming system to "steer" its sensitivity, resolve multipath problems, and compensate for other fading phenomena. In this example, frequency-hopping signals from multiple antennas are fed through a front end where they are "de-hopped," digitized, filtered, and fed to the adaptive beam-forming filter (ABF) network. A decision-feedback network continuously adjusts the ABF's filter weight values.**

end are fed into the demodulator chip, which performs a digital downconversion to baseband while simultaneously separating the complex I and Q signals of the QAM signal. After more filtering, the four channel signals are combined with the adaptive beam forming weights into a single, complex signal. These weights are derived from an adaptive feedback network that also is embedded in the chip.

## Evolving IC Processes

At conferences like CICC, it is quite apparent that new developments in semiconductor processing technology will continue to play a major role in defining the shape of tomorrow's communications. Much of this research is aimed at producing high-frequency devices on ordinary silicon, using as much standard CMOS processing technology as possible. By avoiding exotic materials and processes, developers hope to bring the cost of wireless, broadband, and other high-frequency communications applications within the reach of the average consumer.

One excellent example of this will be a discussion on employing "Thin-Film Silicon on Insulator Technology for Portable Wireless Communications" (paper 21.1), prepared in a joint effort between Motorola's Communication Products Laboratory, Mesa, Ariz., and the Electrical Engineering Department of the University of California, Los Angeles. The paper provides a detailed look at the state-of-the-art thin-film silicon-on-insulator (TFSOI) technology. Both bonding-and-etchback and implanted-oxygen techniques are explored, while contrasting their relative advantages and disadvantages.

## Meeting ATM's Challenges

Despite persistent rumors of its demise, ATM is alive and well, and living in an increasingly large number of network backbones, telecommunications networks, and other broadband infrastructures. With its standards finally approaching maturity, the next hurdle ATM will face is the development of appropriately priced line-interface and switching components that can handle the high speeds and complex protocols.

Switching and cell processing functions can either be handled by fast, general-purpose RISC processors, or by state machines, fabricated in dedicated logic. While programmable processors such as the RISC types have the advantages of being able to track changing applications requirements and standards, they cannot typically handle data rates much above 155 Mbits/s.

On the other hand, dedicated logic is fast, but costly in terms of gate count, and runs the risk of being obsolete as ATM standards evolve. One recent trend is a hybrid approach, which employs a processor whose architecture has been optimized for processing ATM cells. To date, only Maker Communications, Waltham, Mass., has a commercially-available architecture employing an ATM-optimized CPU, but there is considerable interest in this approach.

Following this trend, an ATM-optimized processor will be presented in session 22 by the NEC Corp., Kawasaki, Japan. Entitled "An ATM Application-Specific Integrated Processor" (paper 22.1), the presentation spells out the details of a new dedicated architecture that consists of a custom-crafted CPU core, a pipeline input cell buffer, and a content-addressable memory (CAM). This architecture is intended to give the chip both high performance and reconfigurability.

The researchers identified a group of "primitive" ATM functions, such as accepting incoming cells, extracting header information, and recognizing different types of cells and processing them accordingly. Depending upon their complexity and how much the functions varied from cell to cell, they were implemented in various ways, as hardwired logic, software-programmable logic, dedicated instructions within the CPU, or short groups of macro instructions that the processor carries out.

The cell processor was implemented as a four-stage pipeline architecture, with state-machine controlled memory buffering at each stage. The on-chip CAM was used to compress memory size requirements and speed the execution steps within the processor.

ATM switching also is an area undergoing significant innovation. In small-to-medium-sized applications, many designers are turning to a shared-memory architecture, which stores incoming cells in a multi-byte-wide memory. A controller reads the cell's address and tells the appropriate output port where to find it. If additional intelligence is added, priority queue buffering can also be implemented.

In "A Single-Chip Controller for 1.2 Gbit/s Shared Buffer ATM Switches," researchers from both the Japanese and U.S. divisions of NEC describe their switch design efforts, the switch architecture, and its potential applications. The controller uses standard external SRAMs to form the switch's cell buffers, header translation tables, and control memories, thus greatly reducing the amount of specialized silicon required. The chip can support multiple line interface speeds, using a standard UTOPIA II interface. It also employs a novel buffer control scheme known as "re-queuing" which enables very high throughput multicast switching.

## A New Look At The PHY Layer

The issues surrounding the physical layer of ATM also will be addressed at CICC. Among those papers, one of the most intriguing is "A Skew-Tolerant CMOS Level-Based ATM Data-Recovery System With PLL Topology" (paper 22.3), presented by the University of Leuven, Heverlee, Belgium. It demonstrates a novel approach to data recovery for high-speed networks that uses high-speed multi-sampling techniques rather than a PLL or DLL.

A test chip was fabricated from standard cells in 0.7-µ CMOS. From initial tests, it appears to be fairly immune to wander, clock- and data-jitter, and propagation phase shift. The 622-Mbit/s data-recovery system is capable of operating with a 25% tolerance on the absolute position of the signal's edge through the use of an intelligent sample selector, whose function is to extract the correct data from an oversampled input. In addition to any performance issues, the elimination of on-chip PLLs bypasses the costly and difficult task of implementing a few highly demanding analog functions on a predominantly digital chip.

# Test Papers Target Mixed-Signal, Design-For-Test Topics

*Open-loop Feedback Helps Speed Verification Of A Charge-pump PLL's Operating Frequency Range Without Frequency Measurements.* **JOHN NOVELLINO**

A lot of work has been done in recent years on design-for-testability (DFT) strategies for digital circuits. But mixed, analog-digital circuity is becoming more popular, and DFT techniques for these designs are not as well developed. Taking note of that, Session 10 of the Custom Integrated Circuits Conference (CICC) includes a paper by G. Devarayanadurg, P. Goteti, and M. Soma from the University of Washington, Seattle, who present a testability strategy for embedded charge-pump phase-locked loops that takes advantage of boundary scan.

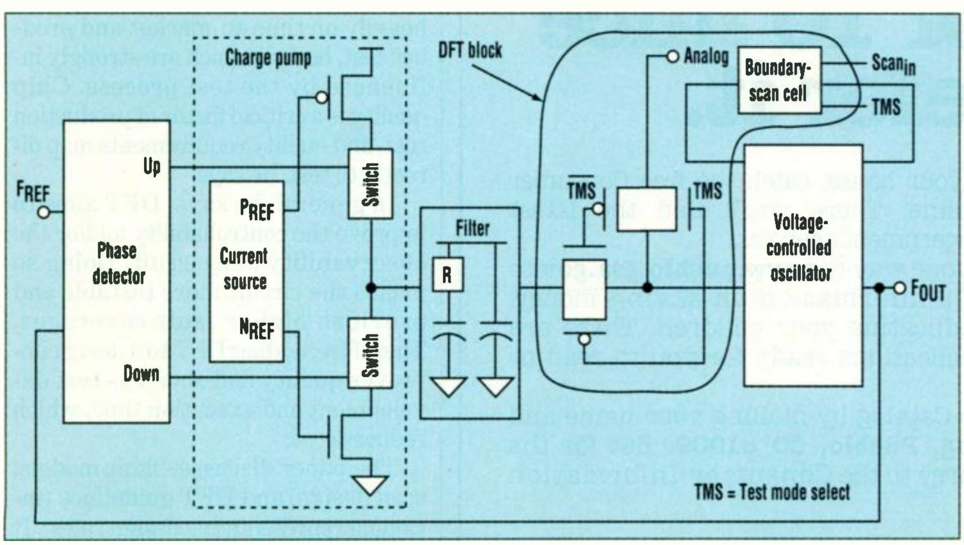
The proposed technique verifies the operating frequency range of the PLL without the time-consuming frequency measurements. Instead, the authors use the fact that the PLL's operating range depends on the frequency range of its voltage-controlled oscillator (VCO). They propose converting the circuit's closed-loop system with tight feedback and large variations in time constants into an open-loop circuit. They add a test pin for an analog test signal and use an IEEE-1149.1 scan register to shift in voltage values and disable the VCO feedback *(see the figure)*. This technique allows them to characterize the VCO by sampling its dynamic delay, which takes nanoseconds instead of the milliseconds needed for a frequency measurement.

The area overhead for the DFT block was less than 10%. The authors say that neither the lock characteristics of the PLL, nor its operating frequency range were affected by the DFT block. A 5% shift in the time axis was noted.

A wider discussion of DFT for mixed-signal circuits is featured in a paper examining ways to improve the testability of mixed-signal ICs by Gordon W. Roberts of the Microelectronics and Computer Systems Laboratory at McGill University, Montreal, Quebec, Canada. Roberts notes that these days analog circuitry often is embedded in a mixed-signal device with no external I/O access. And with the inherent difficulties of testing analog circuitry, compared to digital circuitry, the analog testing could cost as much as 50% of product's total cost.

Roberts looks at some of the testing problems of analog circuitry. For example, a digital circuit's function can be described by a closed-form expression, like a set of Boolean equations. But analog functionality is always described by a nominal behavior and an uncertainty range, with acceptable error typically as little as 0.1% to 1%.

The author describes some possible solutions to the analog measurement problem, including two proposed analog test buses and built-in self-test techniques. One bus, which would allow 100-MHz operation, involves observing a node voltage at an external pin by first converting the voltage to a current using a local V-to-I circuit, then moving it off chip through the bus. Also discussed is the IEEE-1149.4 test bus, which would be compatible with the IEEE-1149.1 boundary-scan standard. That proposal is scheduled for a vote next year.




**A proposed technique for increasing the testability of embedded charge-pump phase-locked loops adds a pin for an analog test signal and uses an IEEE-1149.1 boundary-scan register to shift in voltage values and to disable the voltage-controlled oscillator feedback.**

A third paper in the session, from Thomas Almy of Tektronix Inc., Beaverton, Ore., describes a way to make precise at-speed timing measurements via boundary scan. The technique embeds timing-analyzer macros on an ASIC to take advantage of IEEE-1149.1 and make timing measurements with a resolution 32 times smaller than the clock period. The technique uses the boundary-scan Runbist command and transmits measurement commands and results over the scan chain. The work was done under a Defense Advanced Research Projects

Agency research contract.

The design incorporates 16 channels, each of which can capture or drive up to 62 events. More events can be handled by dividing a test into a sequence of bursts. The scheme was successfully used to make on-chip, at-speed timing measurements, and was more accurate than traditional automated test equipment.

### Improvements Sought

According to the author, the technique can be improved by converting the analyzer design into ASIC macros. Making the design more flexible reduces its size when its full capability is not needed. Finding a way to control the analyzer and circuit under test, without the need for a fast external pattern generator additionally improves the technique. Also, Tektronix contracted with LogicVision Inc., San Jose, Calif., to incorporate the timing analyzer into its test synthesis tools.

For designers not yet convinced of DFT's importance in the overall success of a project, the session includes a tutorial that lays out the benefits, in fact the necessity, of using some kind of DFT technique for complex digital ICs. Alluding to the old practice of design engineers completing their work and then "throwing the design over the wall" to the test engineer, a tutorial on DFT will be presented by the IC Business Div. of Hewlett-Packard Co., Palo Alto, Calif.

The author, Peter C. Maxwell, notes that economic success depends heavily on time-to-market and product cost, both of which are strongly influenced by the test process. Chip quality is a critical factor of production cost, and quality requirements map directly to test, he says.

In general, he says, DFT aims to improve the controllability and/or the observability of a circuit. Doing so makes the circuit more testable and provides higher fault coverages. Therefore, adding DFT to a design improves quality and shortens test development and execution time, which reduces cost.

The paper discusses fault models, scan design, and DFT guidelines (including representative design rules). It also examines some cost/benefit tradeoffs and concludes with some components needed for a composite test suite.

# EIF '97 Highlights Technology Advances

*Design Engineers, Engineering Managers, And Company Management All Will Find Topics Of Interest At The Electronics Industries Forum.*

**John Novellino**

The Electronics Industries Forum (EIF) of New England, the conference and exhibition formerly known as Electro, will make its debut May 6-8 at the World Trade Exhibition Center, Boston, Mass. The highlight of the Forum from the design engineer's viewpoint will be the Technology Summit, with its 44 sessions covering seven tracks: Concurrent engineering, automated test technology, electromagnetic compatibility, microelectronic assembly, computers and networks, communications, and biomedical electronics.

Four other summits—International Standards, Supply Chain, Education and Industry, and Regional Development—will appeal to the entire range of disciplines involved in the electronics industry. A trade show featuring manufacturers of components, devices, and systems will accompany the approximately 120 sessions in the conference and technical programs.

"Our overall goal is to ensure that New England continues to be the breeding ground for technical innovations in this country," said Fausto Molinet, president of Matrix International and chairman of the Technical Summit. "Our goal will be accomplished by educating engineers and executives about the very latest developments in electronic manufacturing and design."

Besides emerging technologies, the conference will cover business growth strategies, retaining jobs in New England, global marketing, and access to capital. "The Forum will bring together representatives from the entire electronics marketplace—from company managers to engineers, from government officials to venture capitalists, and from university professors to the engineering leaders of the future," said Pete McCloskey, president of the Electronic Industries Association (EIA). The EIA and the IEEE Region I are among the 24 business, government, and educational organization that formed a strategic alliance to sponsor the EIF.

The concurrent engineering track tackles a subject that is becoming more important as time-to-market goals shrink. One session, TC2, presents case histories from three major companies to show how virtual prototyping supports concurrent engineering by demonstrating detailed product functionality, even at the concept stage. As a result, says speaker Donald M. Stewart of The Concurrency Group, various disciplines, and potential customers, can contribute to the product early in the design process. Another session, TC6, offers tips on how to use product platform planning to implement product strategies. The speaker notes that using common platform elements provides a number of benefits, but many companies have problems transitioning from single-project to multiple-project planning.

With the increase in the use of electronic equipment, including wireless devices, and the mandatory standards imposed in Europe last year, electromagnetic compatibility (EMC) is another issue of concern for many designers. Three sessions in the EMC track discuss various government and industry standards. Session TE2 focuses on the Federal Communications Commission's (FCC) technical requirements that ensure the compatibility of radio transmitters and electronic equipment and recent and proposed changes in equipment authorization requirements. Another session, TE3, will provide an update on the European EMC standards and regulatory issues, including certification procedures. Finally, the multiple standards of industry groups for shielding effectiveness of conductive paints and coatings, gaskets, and enclosures will be the subject of session TE5.

**One session describes material and process improvements that may reduce the cost of MCM substrates.**

In the communications arena, two of the six sessions revolve around Inferno, Lucent Technologies' operating system for multimedia, consumer, and network applications. Both presentations include representatives from Lucent among the speakers. Session TT5 will introduce Inferno to attendees and discuss some early applications. Session TT6, comprising a workshop and tutorial, goes into more detail.

Three of the four remaining sessions involve RF and wireless technology. TT3 is a shortened version of a tutorial on the principles of high-efficiency RF power amplifiers in classes B through F. TT4 discusses wireless local loops, which are 1- to 10-GHz systems being using to provide POTS in Eastern Europe, Asia, and the Middle East. Higher-frequency versions (upper K band) are being looked at to offer competitive services in the U.S. The third session, TT2, examines the application of fractal mathematics to antenna design. The small profiles of antenns based on fractal matehmatics can be integrated into the transceiver casing, and thus made invisible to the consumer.

Flow-control topics and switching predominate in the computers and networks track. Sessions TN2 and TN3 take up rate-based flow control and quantum flow control, respectively. Flow control for packet-data-based data networks is discussed in session TN4. This presentation examines interactions between TCP/IP and network flow-control mechanisms and across interfaces between packet and cell networks. It considers packet quantum flow control as a core network capability.

An important issue in IP switching networks is the definition of a flow and its granularity, which can vary over a wide range. Session TN5 looks into the trade-offs that must be considered and the limitations of the current technology. The session contends that there is no one right aggregation level in IP switching systems, and that parameter should be left to network designers to optimize.

A strong emphasis on multichip modules (MCMs) and ball grid arrays (BGAs) are highlights of the microelectronic assembly track. Session TM3 notes that although MCMs can improve performance and reduce the size of electronic packages, cost issues have inhibited their use. But the Consortium for Vehicle Electronics was started to address this and other problems. The presentation describes several material and process improvements that potentially can reduce the cost of MCM substrates. Promising techniques include replacing expensive high-temperature resins with multifunctional epoxies, using alternative reinforcements to enhance laminate dimensional stability, and primary imaging with liquid resists

A session on flip chip technology for BGAs reviews the several flip chip assembly processes available and their suitability for different markets. The presenter argues that solder-bumped flip chips meet the widest range of current product requirements. The various solder-bumping processes also will be analyzed for their strengths and weaknesses for both IC packaging and direct chip attach methods.

| How Valuable | Circle |
|---|---|
| Highly | 525 |
| Moderately | 526 |
| Slightly | 527 |

## EIF '97 TECHNOLOGY SUMMIT TRACKS

| Concurrent Engineering | Automated Test Technology | Electromagnetic Compatibility | Microelectronic Assembly | Communications | Computers and Networks | Biomedical Electronics |
|---|---|---|---|---|---|---|
| Tuesday, May 6<br>10:00-10:45 a.m.<br>Motivators and metrics for product development | Tuesday, May 6<br>10:00 A.M.-Noon<br>Automated test systems development trends | Tuesday, May 6<br>10:00-11:00 a.m.<br>Medical device EMI–ANSI issues | Wednesday, May 7<br>1:00-4:00 p.m.<br>Advanced microelectronics packaging technology | Wednesday, May 7<br>1:00-1:45 p.m.<br>Evolution of a multistage switching network with broadcast traffic | Wednesday, May 7<br>2:15-3:00 p.m.<br>Fuzzy systems theory and applications | Wednesday, May 7<br>2:30-3:30 p.m.<br>New electronic circuits in optical analytical chemistry analyzers |
| 10:45-11:30 a.m.<br>Three case histories of virtual prototypes to support concurrent engineering | 2:30-5:00 P.M.<br>Test instrumentation development trends | 11:00 a.m.-Noon<br>Recent advances in FCC EMC and equipment authorization requirements | 4:15-5:00 p.m.<br>SMT solder paste printing: A training perspective | 1:45-2:15 p.m.<br>Fractal antenna applications in wireless telecommunications | 3:00-3:45 p.m.<br>Rate-based flow control | Thursday, May 8<br>8:45-9:45 a.m.<br>Novel applications of spectroscopy for diagnostic breath testing |
| 11:30 a.m.-12:15 p.m.<br>Design for quality (DFQ) for new products | Wednesday, May 7<br>10:00 A.M.-Noon<br>Future automated test challenges and technologies | 2:30-3:30 p.m.<br>Update on European EMC standards and regulatory issues | Thursday, May 8<br>8:45-9:30 a.m.<br>Low-cost multichip module substrates | 2:15-2:45 p.m.<br>High-efficiency RF power amplifiers, classes B though F–Principles | 3:45-4:30 p.m.<br>Quantum flow control | |
| 2:30-3:30 p.m.<br>Design for environment and life-cycle management | | 3:45-5:00 p.m.<br>Hearing aid-digital cell-phone interference issues | 9:30-10:15 a.m.<br>High-volume excimer laser drilling of vias for MCM and BGA applications | 3:00-4:00 p.m.<br>Current state of wireless local loop | 4:30-5:15 p.m.<br>Flow control for packet data networks | |
| 3:45-5:00 p.m.<br>Designing for optimum performance | | Wednesday, May 7<br>8:45-9:15 a.m.<br>Shielding effectiveness–Why don't we have a consensus industry standard? | 10:30-11:15 a.m.<br>Flip chip technology for ball grid array | 4:00-5:00 p.m.<br>Introduction to Inferno and applications of Inferno in communications | Thursday, May 8<br>8:45-9:30 a.m.<br>Levels of flow aggregation in IP switching networks | |
| Wednesday, May 7<br>8:45-9:45 a.m.<br>Secrets to successfully implementing strategy through product platforms | | 9:15-9:45 a.m.<br>Electrostatic discharge–A tutorial | 11:15 a.m.-Noon<br>BGA component considerations and a method for ball attachment | Thursday, May 8<br>8:45 a.m.-1:00 p.m.<br>Workshop and tutorial on Inferno in programming and systems applications | 9:30-10:15 a.m.<br>Overview of tag switching | |
| 10:00-10:45 a.m.<br>ISO 9000 in product design and team structure for new product development | | 10:00-11:00 a.m.<br>Noise filtering on cables | Noon-1:00 p.m.<br>Photonics packaging automation | | 10:00-1:00 p.m.<br>Internet tutorial: Putting up your billboard on the information superhighway | |
| 10:45-11:30 a.m.<br>Making concurrent engineering work in your company | | 11:00 a.m.-Noon<br>EMC systems design | | | 10:30-11:15 a.m.<br>Access to the home: Cable modems | |
| 11:30 a.m.-12:15 p.m.<br>Breakthrough approach to engineering-design problem solving | | | | | 11:15 a.m.-Noon<br>Access to the home: ADSL | |

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PRODUCT FEATURE

Data sheets on products like these can be found at www.penton.com/ed/

# Transceivers Support Nearly Any Wireless Data Application

The SX04x family of spread-spectrum baseband controllers simplifies the design of direct-sequence wireless data systems by integrating all of the baseband circuitry required to implement a radio. Depending on an application's requirements, designers can choose different controllers with data rates ranging from 1 to 16 Mbits/s, and compatibility with the soon-to-be-finalized IEEE 802.11 wireless data standard. All the chips have a high level of programmability, enabling designers to tailor parameters such as data rate, chipping code length, and modulation format for a particular application.

Each SX04x transceiver controller contains a generic microprocessor interface and a full-duplex transmit receive message processor circuit. The transmit section includes a data scrambler, packet generator, CRC generator, pseudonoise (PN) code generator, and modulation mode formatter

In the receive section, functions such as the PN code generator, synchronization and tau-dither tracking loop, integrate-and-dump control, data descrambler, packet decoder CRC checker, demodulator, and RSSI, are all handled on-chip. The chip's baseband output, input, and receive PN code lines simplify interfacing to the SX051 IF transceiver IC or any other radio's IF section.

For many controller applications, the SX043 transceiver's low cost and flexibility make it a good choice. With a programmable chipping rate of up to 64 Mchips/s, it can support a maximum data rate of 2 Mbits/s using QPSK or DQPSK modulation, and a PN code of length 63.

At lower chipping rates, it can generate code lengths of up to 2047 chips. This allows designers to select an optimal combination of transmitted power, system process gain, system bandwidth, and data rate for a particular application.

The SX043's highly programmable architecture also enables it to employ a wide variety of well known other modulation schemes, including QPSK, DQPSK, and 8/16-level QAM. Its user-controlled shutdown modes and 3.3-V (with 5-V option) operation make it ideal for power-sensitive handheld portable applications. Transmit-only and receive-only versions of the processor (SX041 and SX042) are available for cost-sensitive, single-direction applications.

To accelerate the development process, a complete ISA bus-based evaluation kit also is available. It includes the DEV043 ISA bus PC interface card, an interface cable, a fully functional baseband development board, and a set of software drivers. Using this software, the baseband section can be programmed and operated under the control of any

## PRODUCT FEATURE

Data sheets on products like these can be found at www.penton.com/ed/

standard PC with an open ISA bus slot. A breadboard area on the baseband pc board and complete source code listings permit designers to make additions and modifications to both the hardware and software.

If higher data rates are required, the SX049 spread spectrum transceiver can be used to support data rates of up to 16 Mbits/s. Capable of both half- and full-duplex operation, the SX049 shares many basic features with the SX043, but in addition supports independent transmit and receive codes, as well as selectable code scrambling to facilitate so-called "spectral whitening." It supports packetized synchronous protocol (HDLC), including abort sequence generation and checking, automatic zero insertion/deletion, and address field recognition.

Transmit- and receive-only vari- nts of the SX049 also are available the SX047 and SX048, respectively) plications where unidirectional ration is desired.

If standards-based wireless data is desired, the SX045 will enable rapid development of equipment that supports the IEEE 802.11 wireless data standard. While its architecture borrows heavily from the other SX04x series, it has additional features that help it perform the radio control and data-transfer functions of the physical-layer convergence procedure (PLCP) and PHY layers, providing an integrated control/data interface between the Media Access Controller (MAC) and the radio.

With its generic microprocessor interface (8 bits of data, 6 bits of address), the SX045, sports 16-byte transmit and receive buffer FIFOs with programmable capacity flags. Its programmable 11-bit recirculating PN code generator is fully programmable, with a default setting to the 802.11 standard.

Besides selectable data rates and modulation formats (1-Mbit/s DBPSK and 2-Mbit/s DQPSK), the controller has an on-chip despreading and early/late-correlator tracking loop that assists in precise tracking of the receiver's correlation peak. Interface to the radio includes a clear-channel assessment circuit, a radio control port, as well as a Digital-to-Analog Converter (DAC) that can be used to control the RF amplifier's power level.

Available now from the manufacturer, the SX043 is priced at $18 each in 10,000-piece quantities. The companion SX041 and SX042 cost $8 and $13 each respectively. The DEV043 development kit is available for $495. Sampling now, and available in production quantities in May of this year, the SX049 transceiver controller is priced at $21 each, with the SX047 and SX048 costing $10 and $15, respectively. The SX045 802.11 transceiver is due out in the second quarter of this year, and is anticipated to cost below $10 each in lots of 10,000.

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*Pocatello, ID 83201*
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## JUNE

**Canadian Wireless '97 Conference and Trade Show, June 3-5.** Palais des Congres, Montreal, Quebec, Canada. Contact Monique Trottier, CWTA, 275 ruse Slater St., Suite 2004, Ottawa, Ontario, Canada K1P 5H9; (613) 233-4888; e-mail: mtrottie@cwta.ca

**International Symposium on VSLI Technology, Systems, and Applications, June 3-5.** Grand Hyatt Hotel, Taiwan, China. Contact T. P. Ma, Dept. of Electrical Engineering, Yale University, 15 Prospect St., New Haven, CT 06520-8284; (203) 432-4211; fax (203) 432-7769.

**Mixed Signal Test Workshop; June 3-6.** Seattle, WA. Contact M. Soma; (206) 685-3810; e-mail: soma@ee.washington.edu.

**American Control Conference (ACC '97), June 4-6.** Albuquerque Convention Center, Albuquerque, NM. Contact Steven Yurkovich, Department of Elec. & Engrg., Ohio State Univ., 2015 Neil Ave., Columbus, OH 43210; (614) 292-2586; fax (614) 292-7596; e-mail: s.yurkovich@i.ee.org.

**IEEE International Conference on Communications (ICC 97), June 8-12.** Montreal, Canada. Contact Celia Desmond, Stentor, Fl. 6b, 33 City Center Dr., Mississauga, Ontario L5B 2N5, Canada; (905) 615-6507; fax (905) 615-8421; e-mail: celia.desmond@tc.resonet.com.

**IEEE/MTT-S International Microwave Symposium (MTT 97), June 8-13.** Convention Center, Denver, CO. Contact John Dunn, Dept. of Electrical & Computer Engineering, University of Colorado, Campus Box 425, Boulder, CO 80309; (303) 492-5920; fax (303) 492-5323; e-mail: dunn@boulder.colorado.edu.

**IEEE International Symposium on Circuits & Systems (ISCAS 97), June 9-12.** Hong Kong Convention & Exhibition Centre, Hong Kong. Contact ISCAS '97 Secretariat, Department of Electrical & Electronic Engineering, University of Hong Kong, Pokfalam Rd., Hong Kong; (852) 28592710; fax (852) 25598738; e-mail: iscas97@hkueee.hku.hk.

**34th Design Automation Conference (DAC '97), June 9-13.** Anaheim Convention Center, Anaheim, CA; Contact MP Associates Inc., 5305 Spine Rd., Suite A, Boulder, CO 80301; (303) 530-4333; fax (303) 530-4334.

**ASIA TELECOM '97 (TIA), June 9-14.** Singapore, Asia. Contact (703) 907-7736.

**IEEE International Conference on Consumer Electronics (ICCE), June 11-13.** The Westin Hotel O'Hare, Rosemont, IL. Contact Diane D. Williams, 67 Raspberry Patch Dr., Rochester, NY 14612-2868; (716) 392-3862; fax (716) 392-4397.

**Virginia Tech/MPRG Symposium on Wireless Personal Communications, June 11-13.** Campus of Virginia Tech, Blacksburg, VA. Contact MPRG Conference Coordinator Jenny Frank (757) 686-3765, or Jack Lilly, (540) 231-4849 or

**International Solid-State Sensors and Actuators Conference (Transducers 97), June 15-19.** Hyatt Regency Hotel, Chicago, IL. Contact Kensal D. Wise, 1246 EECS Building, University of Michigan, 1301 Beal Ave., Ann Arbor, MI 48109-2122; (313) 764-3346; fax (313) 747-1781.

**IEEE Digital Cross Connect Systems Workshop VII (DCS 97), June 16-19.** Banff Park Lodge, Banff, Alberta, Canada. Contact James H. Simester, Lucent Technologies, P.O. Box 3030, Room 4J-526, 101 Crawfords Corner Rd., Holmdel, NJ 07733-3030; (908) 949-7336; fax (908) 949-2724; e-mail: sims@bostare.ho.att.com.

**Third Conference on Object-Oriented Technologies & Systems (Coots 97), June 16-20.** Marriott Hotel, Portland, OR. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

**IEEE International Conference on Systems, Man, and Cybernetics, June 16-20.** Hyatt Orlando, Orlando, FL. Contact James M. Tien, Chair, DSES Department, Rensselaer Polytechnic Institute, Troy, NY 12180-3590; (518) 276-6486; fax (518) 276-8227; e-mail tienj@rpi.edu.

**IEEE/ASME International Conference on Advanced Intelligence Mechatronics, June 16-20.** Contact Hideki Hashimoto, Institute of Industrial Science, University of Tokyo, 7-22-1, Roppongi, Minato-ku, Tokyo 100, Japan; (81) 3 3402 6231 ext. 2359; fax (81) 3 3423 1484.

**IEEE Sixth International Fuzzy Systems Conference, June 20-25.** Barcelona, Spain. Contact Ramon Lopez De Mantaras, IIIA-CSIC Campus U.A.B., 08193 Cerdanyola del Valles, Spain; (34) 3-580-95-70.

**IEEE Power Electronics Specialist Conference (PESC 97), June 22-27.** Regal Riverfront Hotel, St. Louis, M Contact Philip T. Krein, University Illinois, 1406 W. Green St., Urbana, I 61801; (217) 333-4732; e-mail krein@uipesl.ece.uiuc.edu.

**IEEE International Symposium on Information Theory, June 29-July 4.** Ulm, Germany. Contact Han Vinck, Institue of Experimental Mathematics, University of Essen, Ellernstr. 29, 45326 Essen, Germany; (49) 201 3206458; fax (49) 201 3206425.

**Sixth IEEE International Fuzzy Systems Conference, June 30-July** Barcelona, Spain. Contact Ram Lopez de Mantaras, IIIA-CS Campus U.A.B. 08193 Cerdanyola del Valles, Spain; (34) 3 580 95 70.

## JULY

**Fifth USENIX TCL/TK Workshop, July 14-17.** Tremont House Hotel, Boston MA. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

**IEEE Power Engineering Society Summer Meeting, July 20-25.** Intercontinental Hotel, Berlin, Germany. Contact Executive Office, IEEE Power Engineering Society, Post Office Box 1331, Piscataway, New Jersey 088- 1331; (908) 562-3864; fax (908) 9- 1769.


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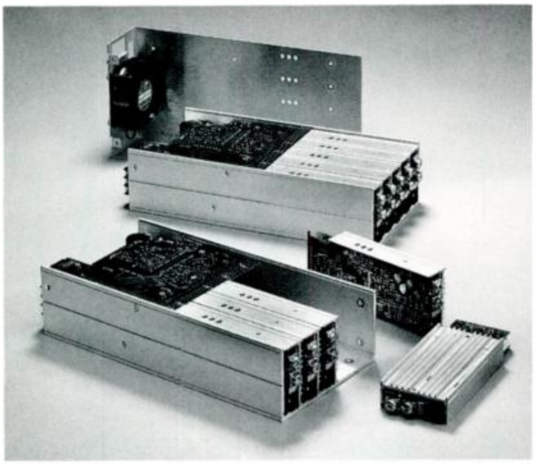
# Lambda's UltraFlex® Series



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Lambda's UltraFlex Series gives you the flexibility you need to cope with today's fast-paced new product development cycles and relentless time-to-market schedules.

| | |
|---|---|
| **Customized Power Supplies Available In 2 Weeks** | Lambda has a complete selection of standard, off-the-shelf modules with varying combinations of output voltages, currents, and system interface/monitoring signals. This ensures that your power supply is tailored to your specific needs without the high cost associated with a custom supply. And prototype quantities are shipped in just two weeks. |
| **Compact Packages** | These high density, low profile packages measure only 2.5 x 5-inches, fitting easily into tight system enclosures. |
| **Fully Regulated & Independent Outputs** | Lambda provides 1 to 10 fully regulated and independent outputs which can be used as + or – polarities. Select from 2V to 48VDC output modules to power any combination of logic, analog, or ancillary circuits. |
| **Universal AC Input or 48VDC Input** | The 85-265VAC wide range input meets worldwide requirements, minimizing inventory and reducing system integration costs. Wide range 36V-75VDC input is also available. |
| **Power Factor & Harmonic Correction** | Active power factor and harmonic correction circuitry ensures compliance to EN60555-2 and EN61000-3-2, while improving input power quality, line regulation, AC noise immunity and reliability worldwide. |
| **System Interface & Monitoring Signals** | AC Power Fail, Global Inhibit, Module Inhibit, Output Good, Margin/Remote Adjust, Current Monitor, and Active Current Share ensure ease of system design and integration. |
| **International Safety Agency Approvals** | Safety agency approvals to UL1950, CSA22.2 No. 234, EN60950/IEC950, and the CE mark (Low Voltage Directive) ensure compliance worldwide. |
| **Meets Worldwide EMI Requirements** | Conducted EMI meets FCC/EN Level B specifications on all AC input models. |
| **Input Transient Protection** | Input transients, input noise, and ESD protection per EN61000-4-2/4/5 Level 3, ensure reliable operation through a multitude of operating conditions. |
| **Fixed Frequency Converters With Sync Input** | Minimizes output noise and provides a means to externally sync the power supply, avoiding system-sensitive frequencies. |
| **Remote Sense** | All outputs have remote sensing capability to offset external voltage drops, due to load lead losses or isolation diodes. |

# How To Configure Your Standard UltraFlex Po

**1. Select Your Power Supply Case.**
Refer to the Case Configuration and Output Module Code Guide. Base your selection on the total output power you need—either 400W or 600W—and the corresponding package size.

**2. List The Required Output Voltages and Curre Your Output Modules.**
Refer to the DC Output Module Codes Guide. with 2V to 48V outputs. You may choose as m up to five module slot widths. Single output mo higher current requirements (refer to the currer

U A K 1-

## UltraFlex Series

## Case Configuration & Output Power Code

| OUTPUT POWER (WATTS) | CASE SIZE (INCHES) | WEIGHT LBS. | CASE CODE | INPUT VOLTAGE |
|---|---|---|---|---|
| **400W** | 2.5 x 5 x 10 | 5.5 | A | 85-265 VAC |
| **600W** | 2.5 x 5 x 11 | 6.0 | B | 85-265 VAC |
| **600W** | 2.5 x 5 x 12 | 6.5 | C | 36-75 VDC |

(cases hold up to 5 module slots)

## Interface Signal Option Code

| SIGNAL CODE | | DESCRIPTION OF INCLUDED SIGNALS & FUNCTIONS |
|---|---|---|
| J | = | NO OPTIONAL SIGNALS: The standard DC Output Module has Remote Sense, Overcurrent and Overvoltage Protection. |
| K | = | INPUT SIGNALS (Global): Input Power Fail, 5V Standby, Global Inhibit, Fan Stop/Thermal Alarm, Fan Inhibit, Sync Input. |
| T | = | OUTPUT MODULE SIGNALS: Module Inhibit, Margin, Remote Adjust, Output Good, Current Monitor & Current Share: Active Current Share & Module Inverter OK. |
| Z | = | INPUT SIGNALS (Global): Input Power Fail, 5V Standby, Global Inhibit, Global Output Good, Fan Stop/Thermal Alarm, Fan Inhibit, Sync Input & OUTPUT MODULE SIGNALS: Module Inhibit, Margin, Remote Adjust, Output Good, Current Monitor & Current Share: Active Current Share & Module Inverter OK. |

Notes: 1. Output Module Signals and Current Share options only available on single output modules.

2. Global Output Good Signal is provided with Input Signals option when individual modules have Output Signals option.

3. Signals are valid with outputs loaded.

## Input Voltage & EMI Code

1 = PFC, 85-265 VAC, 50/60 Hz, Class B EMI

4 = DC INPUT, 36-75 VDC, EN55022A

**Example:**

The above model (UAK1-HJJP) number is for an UltraFlex Power Supply, 400 Watts, 2.5x5x10 -inch Standard Case, Input Signals (Global) 85-265VAC, PFC, Class B EMI Input, with 4 Output Modules (defined at right).

| | |
|---|---|
| H = 5V/60A | (2-slots) |
| J = 12V/17A | (1-slot) |
| J = 12V/17A | (1-slot) |
| P = 24V/8.5A | (1-slot) |
| Total | 5-slots |

ver Supply

s You Need, and Select

ıe modules are available y modules as you need—ıles may be paralleled for share option).

**3. Select Your Input and Output Interface Signals.**
Refer to the Interface Signals Option Code Guide. Select the fully configured Z option for 2 week delivery on prototype quantities.

**4. Call 1-800-LAMBDA-4 for pricing and delivery.**

**5. For sample configurations and pricing, please turn to the next page.**

H J J P

## Output Module Codes

400 & 600 watt cases (A, B, or C Cases) can hold up to five module slot widths.

| OUTPUT VOLTAGE | MAX CURRENT AMPS @ 50°C | MAX POWER WATTS @ 50°C | Vout ADJUST RANGE | SLOT WIDTH | MODULE CODE |
|---|---|---|---|---|---|
| **SINGLE OUTPUT MODULES** | | | | | |
| **2V** | 30.0 | 66 | 1.8–2.2 | 1 | A |
| **2V** | 60.0 | 132 | 1.8–2.2 | 2 | B |
| **2V** | 100.0 | 200 | 1.8–2.2 | 3 | C |
| **3.3V** | 30.0 | 108 | 3.0–3.6 | 1 | D |
| **3.3V** | 60.0 | 216 | 3.0–3.6 | 2 | E |
| **3.3V** | 100.0 | 330 | 3.0–3.6 | 3 | F |
| **5V** | 30.0 | 150 | 4.5–6.0 | 1 | G |
| **5V**[3] | 60.0 | 300 | 4.5–6.0 | 2 | H |
| **5V** | 100.0 | 500 | 4.5–6.0 | 3 | I |
| **12V** | 17.0 | 204 | 10.8–13.2 | 1 | J |
| **12V** | 30.0 | 360 | 10.8–13.2 | 2 | K |
| **12V** | 50.0 | 600 | 10.8–13.2 | 3 | L |
| **15V** | 14.0 | 210 | 13.5–16.5 | 1 | M |
| **15V** | 24.0 | 360 | 13.5–16.5 | 2 | N |
| **15V** | 40.0 | 600 | 13.5–16.5 | 3 | O |
| **24V** | 8.5 | 204 | 21.6–26.4 | 1 | P |
| **24V** | 15.0 | 360 | 21.6–26.4 | 2 | Q |
| **24V** | 25.0 | 600 | 21.6–26.4 | 3 | R |
| **28V** | 12.0 | 336 | 25.2–30.8 | 2 | 8 |
| **36V** | 11.0 | 396 | 32.4–39.6 | 2 | 3 |
| **48V** | 4.0 | 192 | 43.2–52.8 | 1 | S |
| **48V** | 8.0 | 384 | 43.2–52.8 | 2 | T |
| **48V** | 12.5 | 600 | 43.2–52.8 | 3 | U |
| **DUAL OUTPUT MODULES**[5] | | | | | |
| **12V & 5V**[3] | 10.0 & 4.0 | 150 | ±10% | 1 | V |
| **5V & 12V**[3] | 10.0 & 4.0 | 150 | ±10% | 1 | W |
| **12V & 12V**[3] | 10.0 & 4.0 | 150 | ±10% | 1 | Y |
| **15V & 15V** | 8.0 & 3.0[1] | 150 | ±10% | 1 | Z |

**NOTES:**

1. Peak Rating 10A and 4A for up to 1 minute.
2. Other output voltages are available. Contact the factory with your specific needs.
3. When using the 600W AC Case B, derate as follows:
   H Module: 5V@55A W Module: 5V@8A, 12V@4A
   V Module: 12V@8A, 5V@3A Y Module: 12V@8A, 12V@3A
   These modules have no derating up to 40°C for the 600W case.
4. Spaces and dashes shown in the above catalog number are not used when entering order.
5. On dual output modules, output 1 has the highest current rating.

# Sample Configurations Global Input Signal Option

## UltraFlex Quad Output

| MAX POWER | OUTPUT 1 | OUTPUT 2 | OUTPUT 3 | OUTPUT 4 | UNIT PRICE PER DELIVERED QUANTITY 1 | 5 | 10 | 25 | MODEL |
|---|---|---|---|---|---|---|---|---|---|
| 400W | 5V@30A | 12V@17A | 12V@10A | 5V@4A | $702 | $585 | $540 | $502 | **UAK1-GJV** |
| 400W | 5V@30A | 12V@17A | 12V@4A | 5V@10A | 702 | 585 | 540 | 502 | **UAK1-GJW** |
| 600W | 5V@30A | 12V@30A | 12V@4A | 12V@10A | 814 | 732 | 666 | 610 | **UBK1-GKY** |
| 600W | 5V@30A | 24V@15A | 12V@4A | 12V@10A | 814 | 732 | 666 | 610 | **UBK1-GQY** |
| 600W | 5V@60A | 12V@17A | 12V@17A | 5V@30A | 897 | 807 | 734 | 673 | **UBK1-GHJJ** |
| 600W | 5V@60A | 12V@17A | 12V@4A | 12V@10A | 814 | 732 | 666 | 610 | **UBK1-HJY** |
| 600W | 3.3V@30A | 48V@8A | 12V@4A | 12V@10A | 814 | 732 | 666 | 610 | **UBK1-DTY** |

## UltraFlex Pent Output

| MAX POWER | OUTPUT 1 | OUTPUT 2 | OUTPUT 3 | OUTPUT 4 | OUTPUT 5 | UNIT PRICE PER DELIVERED QUANTITY 1 | 5 | 10 | 25 | MODEL |
|---|---|---|---|---|---|---|---|---|---|---|
| 400W | 5V@30A | 12V@17A | 12V@4A | 5V@10A | 48V@4A | $822 | $685 | $633 | $587 | **UAK1-GJSW** |
| 600W | 5V@60A | 12V@17A | 12V@4A | 5V@10A | 24V@8.5A | 947 | 852 | 775 | 710 | **UBK1-HJPW** |
| 600W | 5V@60A | 12V@17A | 12V@4A | 5V@10A | 48V@4A | 947 | 852 | 775 | 710 | **UBK1-HJSW** |

**Notes:**

1. These models include wide range 85-265VAC PFC input, FCC/EN Level B EMI Filter, Input Signals (Global), and Overtemperature Protection.
2. All outputs include Remote Sense, Overcurrent & Overvoltage Protection.
3. Output number does not represent output location.
4. Single output modules may be paralleled for higher current ratings with current share option.
5. Total output power and individual output current ratings may not be exceeded.
6. Output ratings are valid from 0 to 40°C. See previous page for 50°C ratings.
7. Output Module Signals and Current Share are optional. Contact the factory for price and availability.
8. Output Module Codes must be in alphanumeric order.

**AC Input**
line.................................85-265VAC, 47-63 Hz (Case A&B).

**DC Input**
36-75VDC on Case C.

**Inrush Current**
Less than 40A peak.

**Efficiency**
75% typical at nominal line voltage.

**EMI**
Conducted EMI conforms to EN55022, Level B, and FCC Docket 20780 Part 15, Subpart J, Class B for AC input versions. Conducted EMI to EN55022A for DC input models.

**Power Factor and Harmonic Correction**
All models are compliant with EN60555-2 and EN61000-3-2, with up to 250 VAC input. Power factor is 0.998 typical at full load.

**Input Transient and ESD Protection**
IEEE-C62.41, Category A3; IEEE-587 Category B; EN61000-4-2/4/5 Level 3.

**Regulated Voltage**
line regulation.............Less than 0.1% for line variations from 85-265VAC. Less than 0.2% for dual output modules.

load regulation............Less than 0.4% for load variations from no load to full load and full load to no load. Less than 0.8% for dual output modules.

cross regulation..........Less than 0.1% between single output modules. Less than 3% between dual outputs with 25% load change on high current output.

ripple and noise..........Less than 0.33% or 15mV RMS. Less than 1.0% or 50mV pk-pk (less than 50mV pk-pk on 5V and 12V outputs) on single output modules. Less than 1.0% or 50mV pk-pk on dual output modules.

temperature coefficient...................0.02%/°C.

**Output Adjustment Range**
±10% of nominal output voltage on all models.

**Thermal Protection**
The power supply will shut down in the event of an overtemperature condition (the fan will continue to operate). To restore operation, the supply must cool down and the AC input must be recycled.

**Overcurrent Protection**
Overcurrent protection on single output modules limits the current from 110% to 120% of current rating on outputs greater than 400W. (110% to 150% of current rating on outputs less than 400W.) Upon removal of the overload condition, normal operation resumes automatically.

**Overvoltage Protection**
Factory-set overvoltage protection from 120% to 130% of nominal output on single output modules. Dual output modules have factory-set overvoltage protection of 120% to 140% of nominal. Internal circuitry will shut down the individual output module. Reset the OVP by cycling the input power.

**Preload**
External preload is not required on single output modules. Dual output modules require 1A minimum load on the highest current output (Output #1).

**Dynamic Response**
±25% load change (from 75% base at a rate of 1A/µsec) will result in output deviation of less than 2% or 100mV peak (125mV for less than 5V outputs). Output recovery to within 1% of nominal to be less than 300µsec.

**Holdup Time**
The output voltage will remain within regulation limits for 20msec at full load with nominal 115/230VAC line input.

**Remote Sensing**
Remote Sense compensates for total cable drop of up to 0.5VDC. Available on all outputs.

**Isolation Ratings**
Conforms to safety agency requirements.

**Cooling**
Cooling is provided via an internal DC operated ball-bearing fan.

**Operating Temperature Range**
Full operation from 0°C to +50°C with 100% rated power on most models. Derate linearly from +50°C to 50% power at +65°C. Derate H, V, W and Y models in 600W case starting at +40°C to 50% power at 55°C.

**Storage Temperature**
-40°C to +85°C.

**Military Specifications**
Shock — MIL-STD-810E, Method 516.4, Procedure I.
Vibration — MIL-STD-810E, Method 514.4,Category I,TP1.

**Mounting**
Two mounting surfaces on all models.

**Physical Data**

| Case Code | Weight Lbs. Net | Weight Lbs. Ship | Dimensions (inches) |
|---|---|---|---|
| A | 5.5 | 7.5 | 2.5 x 5 x 10 |
| B | 6.0 | 8.0 | 2.5 x 5 x 11 |
| C | 6.5 | 8.5 | 2.5 x 5 x 12 |

**Safety Agency Approvals**
The UltraFlex Series meets UL 1950, CSA 22.2 No. 234, TUV, EN60950/IEC950, and SELV. All models carry the CE mark to indicate conformance to the Low Voltage Directive.

**Guarantee**
Lambda's three year guarantee includes labor as well as parts. Guarantee applies to operation within published specifications at the end of three years.

# ELECTRONIC DESIGN QUICK LOOK

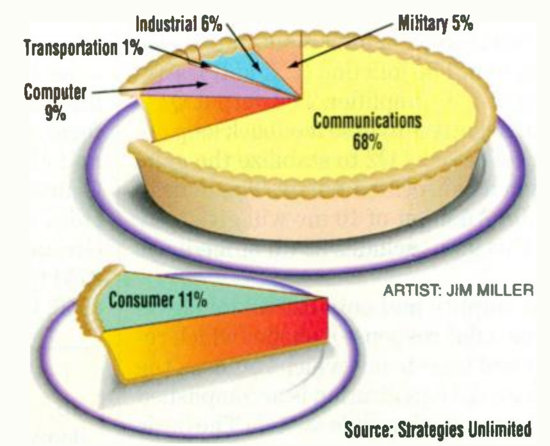
■ Edited by Mike Sciannamea and Debra Schiff

## MARKET FACTS

## Slicing Off A Piece Of The GaAs Pie

According to a new report, "GaAs IC and FET Market Review and Forecast 1996-2000," from Strategies Unlimited, the worldwide market for gallium arsenide (GaAs) RF and digital semiconductor devices will spill over the $2 billion mark in 2000. GaAs integrated circuit (IC) and transistor (FET) demand is expected to expand 15% per year over the next four years from $1.3 billion in 1996 to $2.2 billion in 2000. This market is driven by a strong global demand for communications applications, such as data and satellite communications and wireless telephones. These applications will be eating up 68% percent of the demand for GaAs ICs and FETs at the millennium. Consumer-targeted applications, such as cable and satellite TV will be serving up 11% of the world market. Computer networking applications will see 6% of the market, and military and transport applications will swallow the remainder of the world market, 6%. In comparison to discrete devices, GaAs ICs are a faster growing commodity, expected to expand their market share from over 60% in 1996 to 75% in 2000. The push for greater production of wireless telephones will see analog IC sales rising from $655 million to $1.3 billion at the turn of the century. That growth represents a 19% annual increase. Exploding rates of data communication are responsible for the rise of GaAs digital ICs in gigabit communication networks—from $115 million in 1996 to $327 million in 2000. The jump is seen as an annual growth of 30%. As far as the world share of GaAs device production goes, North America took 47% of shipment revenues in 1996, shadowed closely by Japan with 44%. European production saw 7% of world shipments. The new report reviews the applications, markets, suppliers, and technology for GaAs RF, digital and microwave devices. The report is priced at $3950. Contact Strategies Unlimited, 201 San Antonio Circle, Mountain View, CA 94040; (415) 914-3438; fax (415) 941-5120; Internet: http://www.strategies-u.com. *—DS*

**World GaAs IC And FET Market In 2000**




Source: Strategies Unlimited

## THE ENVELOPE, PLEASE

The very prestigious Medal of Excellence in Engineering from Vrije Universiteit Brussels, Belgium, was recently awarded to Joseph Keithley, founder of Keithley Instruments. The faculty of the engineering department presented the award to Keithley for his career contributions to engineering.

Previous recipients of the award include W. Brandt Goldsworthy, William Hewlett, S. Honda, and David Packard.

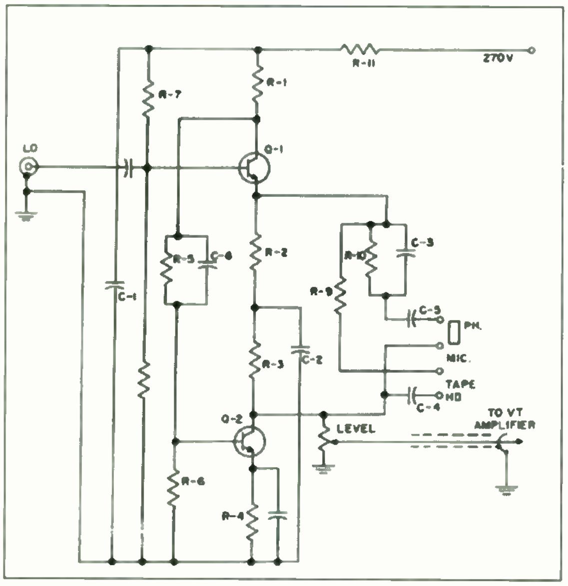
Keithley Instruments was founded in Keithley's small workshop in Cleveland, Ohio, in 1946. The shop manufactured extremely sensitive scientific test and measurement instruments. Particular uses for the equipment included measuring very low levels of current, voltage, or resistance.

Keithley was elected to the National Academy of Engineering in 1992 for his contributions to electronic test and measurement. That same year he received the Cleveland Engineering Society Leadership Award. Keithley is a Fellow in the Institute of Electrical and Electronics Engineers, as well as a Fellow of the American Association for the Advancement of Science.

## 40 YEARS AGO IN ELECTRONIC DESIGN

# Ideas For Design: Hybrid Hi-Fi Amplifier, L. Feldman and S. A. Lipsky, Madison Fielding Corp., Brooklyn, N.Y.

The development of a highly stable transistorized preamplifier has yielded a hum, noise, and microphonic-free "front end" for a standard vacuum tube audio amplifier. As even the best vacuum tube preamplifiers have not yet been able to yield hum figures much in excess of 60 db below full output, a transistorized unit is a considerable design improvement.




The circuit uses two npn transistors in the common emitter configuration. The input stage Q1 is a grounded emitter configuration with emitter resistor R2 bypassed to avoid a high input impedance (50,000 ohms) by means of emitter degeneration. The junction R2 and R3 is bypassed to ground by C2. Q2 operates as a high-gain amplifier. The output Q1 is fed to the base of Q2 through C6. An overall negative inverse feedback loop operates between the emitter of Q1 and the collector of Q2 to stabilize the gain, reduce distortion and provide equalization as described below. The overall gain of the preamplifier is better than 34 db. An input of 10 mv will give 0.5 v output at 1000 cps in the phono position. This gain includes 22 db of feedback used for equalization.

The transistor circuit is called upon to amplify and equalize all low level sources such as microphone (which requires a flat response), phono (which requires the RIAA playback characteristic) and tape-head (which requires the 7-1/2 in. per second NARTB playback curve). All equalization is accomplished by feedback for improved distortion by a three-position slide switch. The basic amount of feedback is about 22 db, leaving enough bass boost for the tape-head playback curve down to 40 cps.

In the diagram, the switch is shown in the phono position where C4 determines the bass cross-over frequency, R10 determines the mount of mid-frequency feedback, and C3 determines high frequency de-emphasis. In the microphone position, only resistive feedback is employed (flat response) and in the tape-head playback position, the cross-over feedback is altered and de-emphasis is removed. *(Electronic Design, May 1, 1957, p. 78)*

*This was one of the early Ideas for Design, which is still one of the magazine's best-read sections. And we're also still looking for good ideas to publish. In addition, we've increased our author stipend tenfold from $10 to $100 in the past forty years.—SS*

***Editor's Note:*** *The May 1, 1957 editorial masthead was the first in which the name of one of the industry's most experienced editors appeared: George Rostky got his start in publishing with us, moved to other magazines, later returned to Electronic Design as Editor-in-Chief, and is now Editor Emeritus at one of our worthy competitors, EE Times. Happy Anniversary, George!—SS*

## BACK TO SCHOOL

*"Management Problems of the Technical Person in a Leadership Role"* is a seminar designed to assist technical specialists in making the transition to manager/supervisor. Among the topics that will be discussed include discovering what it takes to shift from technical specialist to effective leader; preparing solutions for common problems encountered by technical managers; and learning to get what is need from nontechnical people. The seminar fee is $195 per person, and will be held in various locations around the country. For dates and other information, contact Fred Pryor Seminars, 2000 Shawnee Mission Pkwy., Shawnee Mission, KS 66205; (800) 938-6330; fax (913) 722-8585.

*"Intranets: Design & Implementation"* is a two-day workshop examines the business needs that an Intranet will address, the real system requirements and costs associated, and how to provide the necessary infrastructure, tools, and training to its users. Other topics of discussion include possible Intranet applications, database integration, system and user management, available products and services, and client and server components. Course fee is $795. For more information, contact American Research Group, 114 Edinburgh So., Cary, NC 27511; (919) 461-8600; fax (919) 461-8646; Internet: http://www.arg.com.

### FEEDBACK LAND

So, we've begun hanging a few items on the old (and we do mean OLD) cubicle walls here in Hasbrouck Heights, but there's still space for a letter from you. All fancy stationery aside, it's really the suggestions that concern us. Of course, we like love letters and fan mail, but like any good section in a successful magazine, we need to change and grow. Please send us your input. E-mail us: Mike Sciannamea at **mikemea@class. org,** or Deb Schiff at **debras@ csnet.net.** Stamp afficionados may send their paper goods to: QuickLook, *Electronic Design*, 611 Route 46 West, Hasbrouck Heights, NJ 07604. Our fax number is (201) 393-0204.

## CONFERENCE CALL

The Society for Information Display's 1997 edition of its annual Symposium, Seminar, and Exhibition (SID '97) will be held May 11-16 at the Hynes Convention Center, Boston, Mass. The event is described as a forum for discussion on advances in electronic-display products, technology, systems, applications, manufacturing, and testing. SID '97 includes over 60 technical sessions, 330 exhibit booths, and an evening panel session. Among the topics to be discussed in the technical sessions are display-addressing techniques, optical components, display phosphors, and interactive display systems. Featured are celebrations of two of the display industry's most significant anniversaries: The 100th anniversary of the invention of the Braun tube—the first modern cathode-ray tube (CRT)—and the 25th anniversary of the first active-matrix liquid-crystal display (AMLCD). For conference registration and other information, contact Mark Goldfarb, Palisades Institute for Research Services, 1745 Jefferson Davis Hwy., Suite 500, Arlington, VA 22202; (703) 413-3891; fax (703) 413-1315.

The 14th International Conference on Testing Computer Software will be held June 16-19 at the Sheraton Premiere (Tyson's Corner), Washington, D.C. Test engineers, software engineers, development managers, and test managers are among the industry professionals who are urged to attend the conference. Some of the topics that will be addressed at the conference are the management of software testing, the application of various software testing techniques, and Year 2000 Conversion testing. Full-day technical session subjects include "Foundations of Software Testing Techniques," "Automating Software Testing," and "Testing for Year 2000." Vendor exhibits of products and services complete the conference program. For more information, contact USPDI, 612 Ethan Allen Ave., Suite 100, Takoma Park, MD 20912; (301) 270-1033; fax (301) 270-1040; e-mail: admin@uspdi.org.

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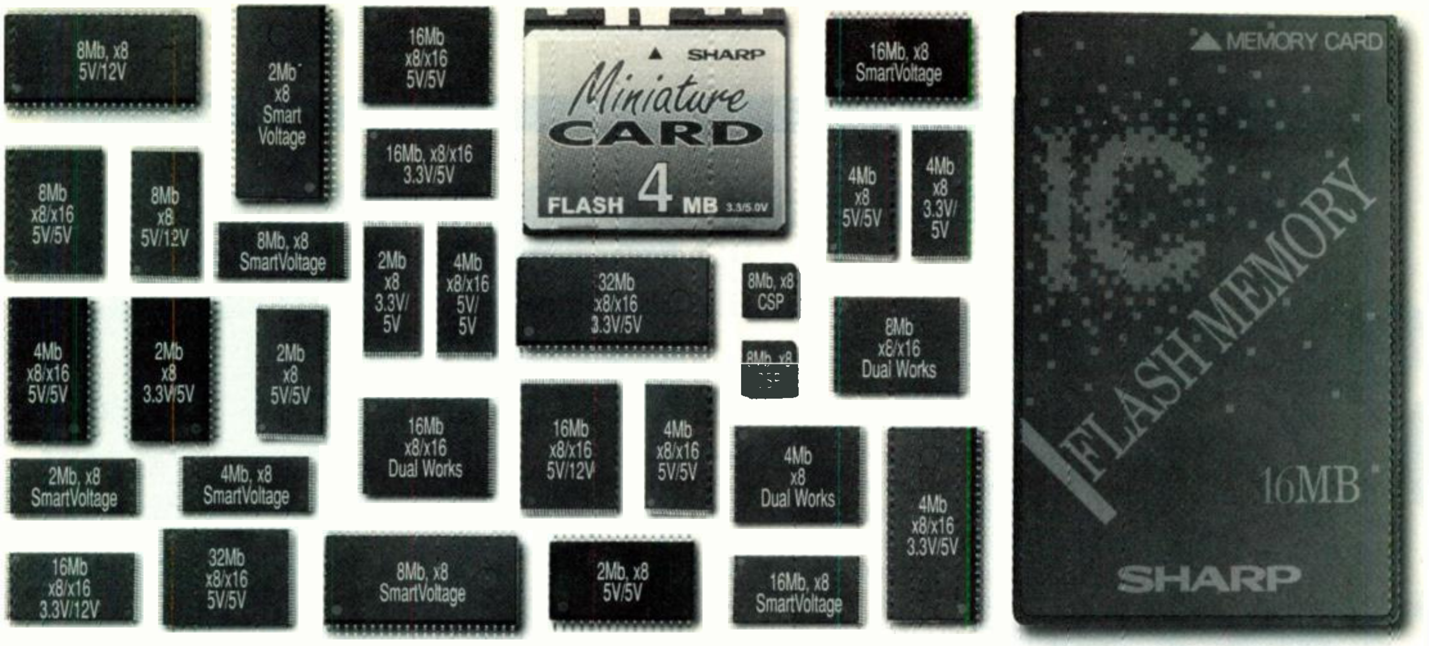


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TECH INSIGHTS / QUICKLOOK

# ISOuch—Compliance Pain

If your company is having some trouble implementing its ISO/QS-9000 quality initiatives, take heart—there's help available. Rob Kantner, author of "ISO 9000 Answer Book," QS-9000 Answer Book," and "Get ISO 9000—Or Get Lost!" looks at "ISO 9000: 10 Common Pitfalls" in the Winter 1997 issue of "Myriad Views" from Informative Graphics.

The first pitfall is "working around the ISO/QS-9000 system." This translates into not implementing the ISO 9000 system completely. Kantner's example is the issue of customer complaints and general problem solving techniques. One thrust of the ISO structure is to institute a categorical documentation system, and use that system in daily business affairs. In the past, companies addressed issues by treating them as one-time-only occurrences, solved the problems as they came up, failed to document them, and went on with business as usual. This first pitfall sees employees continuing to treat their corrective/preventive measures in the same manner. Another place where this pitfall crops up is in the "approved vendor" process. Employees are continuing to buy from unapproved vendors. New products and processes are introduced into manufacturing without proper documentation. All of these issues will be picked up in internal audits, which, if the documentation were followed, would be held on a regular basis.

### Audit Policy

The second pitfall, "playing cat-and-mouse with registration assessors," can be answered with the adage "honesty is the best policy." Consultants tell businesses that they shouldn't volunteer any information to the assessor, just answer the questions and move on with the audit. By taking this tack, it tells employees that it's policy to hide mistakes, fudge results, and treat assessors as inquisitors. But for ISO/QS-9000 to work, the company's performance can only be improved by getting an effective assessment of the process. Dealing with the problems that crop up at any company in an honest and open way allows them to be addressed in an equally realistic way.

Pitfall Three, "appointing a junior person as management representative," deals more with the politics of an organization than the ability of the individual to actually do the job. Coming into a business during the ISO/QS-9000 process can be more than overwhelming. What is needed in this position is an individual who has the confidence of top management, years of experience in the company, respect of all involved, and someone who truly understands the process. Most of all, this person must have the attitude of improving the company's worth by implementing the ISO 9000 system.

### Correcting The Corrections

"Inhibiting the corrective action process," Pitfall Four, addresses the problems that arise when companies fool around with the corrective/preventive action process. According to Kantner, they do this by publishing a list of "permissible" topics for corrective action requests (CARs), restricting who can initiate CARs, and insisting that CARs be approved by managers before reviewed. These restrictions limit the power of CARs. In the ISO 9000 process, all employees should have the power to issue CARs and submit them to impartial individuals for consideration. Although some companies brag about the small number of CARs that are issued, the real number they should be examining is the number of frivolous CARs that are initiated.

In the ugly end of the business is Pitfall Five, "using the ISO/QS-9000 system to discipline people." In some cases when a CAR is written or an internal audit goes badly, the employee most closely involved gets written up or is reprimanded. What should be happening is that names are left out and functional titles are used instead. If it is an employee performance issue, management should treat it as a training issue. If further incidents occur, it then becomes a personnel issue—but outside of the ISO/QS-9000 system.

Pitfall Six, "working the corrective action process only partway," seems pretty self-explanatory, but common sense doesn't always prevail. Even if a company has the ISO 9000 corrective/preventive action subprocess implemented, it must be followed up. When CARs aren't followed up, companies will find the same causes showing up in their future CARs. The source of the problem often isn't found until a pattern appears in the CARs. Not only is the follow-up process required by the standard, but it is key to the corrective/preventive process.

Another political pitfall, number seven, "appointing only supervisors and managers as auditors," can lead to dissension among the ranks. By forming an internal ISO/QS-9000 audit team made up of individuals from every level and function of the company, compliance heads are spreading out the workload, involving people in the process who ordinarily don't have a lot of "power" in the organization, and promoting teamwork in the company.

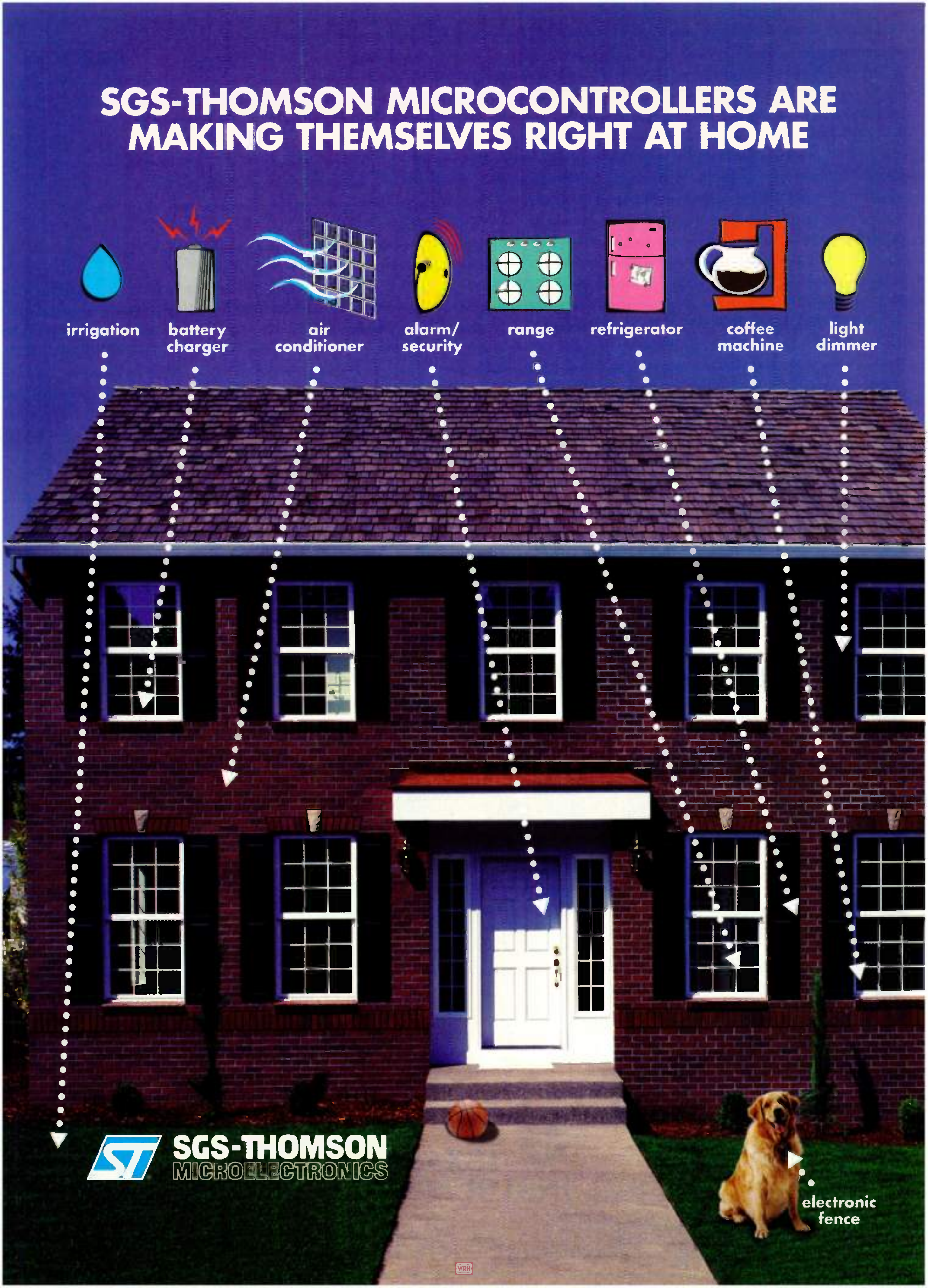
The eighth pitfall, "creating bales of procedures, work instructions, and forms," may seem tough to avoid, but following the Bauhaus tradition of "Less Is More" does work. Standard operating procedures don't need to fill volumes. People just won't use them, if that's the case. Quality policies can be kept to under 50 pages. Auditors aren't interested in the size of your documented process, they want to see how you implement it.

Pitfall Nine, "having a vague, meaningless quality policy statement," means that the company is trying to protect itself from failing quality audits. Quality policy statements must be pertinent to the company and customers. Related goals and objectives must be specific and measurable, and easily understood.

Finally, "accepting less than full compliance with the system" is a trap that employers fall into when their staff falls short, and they decide to just "work around" them. Tolerating that behavior defeats the purpose of ISO/QS-9000, creating two systems: the official and the real. Management must work to get all workers on the team, and keep them there.

Rob Kantner may be reached at (313) 722-4334, or via his web site: http://www.cris.com/~rob4334/iso.htm.

*—DS*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# LET OUR MICROS MAKE YOUR PRODUCT A HOUSEHOLD WORD

The reason SGS-THOMSON's 8-bit ST62 family of MCUs is making itself at home in so many household appliances can be summed up in one word: *Value*. ST62 devices deliver more performance in less space for less money. Even the core is optimized for cost-effective operation. Add ESD protection and unmatched noise immunity and you begin to understand why the ST62 is opening doors to consumer applications that remain closed to ordinary MCUs.

All ST62s contain ROM, RAM, an 8-bit timer with 7-bit programmable prescaler and multifunctional individually programmable I/O ports. Also available: Devices with high-current buffers to directly drive LEDs or TRIACs, along with a wide range of peripherals such as PWM and LCD drivers. A wide operating voltage range and robust design allow ST62 microprocessors to be powered directly from a battery or the main with minimum external components.

In addition to the extensive ST62 family, SGS-THOMSON offers other 8-32 bit micro solutions such as ST7, ST9, ST10 and ST20 families. All of these products are fully supported with extensive development tools including C compilers for most families. So why not let our micros help make your product a household word. To find out more fax 617-259-9442, write SGS-THOMSON, 55 Old Bedford Road, Lincoln, MA 01773, or e-mail: info@stm.com. And visit our web site at **http://www.st.com**

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- thermostat
- scale
- programmable timer
- vacuum cleaner
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**ST7**
Powerful industry standard 8-bit core, surrounded by numerous advanced peripherals. 3K to 48K of ROM with different RAM sizes. Choose EPROM and OTP versions for proto-typing. On-chip EEPROM is also available for integrated data storage.

**ST9**
8/16-bit micro family fills requirements of most advanced computer, consumer, telecom, industrial and automotive applications.

*Service and Technology*



For More Info Turn Page

READER SERVICE 142

## HOT PC PRODUCTS

In the "big news of 1997" category, Boca Research shipped their first 56K Internet Modem at the end of February. Boca's unit uses Rockwell Semiconductor Systems' K56Plus chip set. Boca had been testing Rockwell's chip set since late January.

Boca is one of the founders of the Open 56K Forum, which is an industry-wide coalition of technology leaders in the communication and computer industries that are trying to achieve widespread implementation of the 56K modem technology. Their focus is on finding a 56K protocol that will ensure interoperability between modem brands.

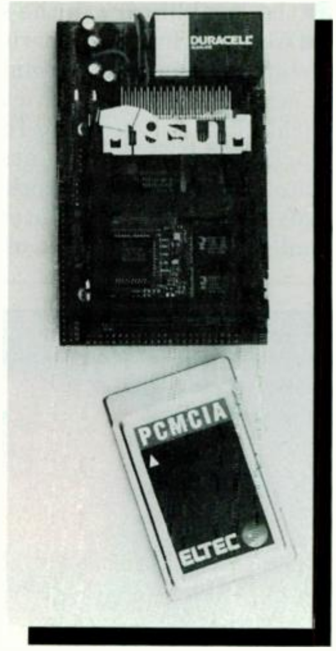
The 56K technology, called K56flex by Rockwell, works on the assumption that there is a purely digital connection to the phone network that ISPs and corporations already use for remote access. The slower modems, on the other hand, run on the thinking that both ends of the modem conversation have an analog connection to the public-switched telephone network. The transmission speeds are limited to 33.6 kbits/s because the data signals must be converted from digital to analog and back again.

The K56flex technology digitally encodes the downstream (from the ISP to the user) data instead of modulating it. The method is asymmetrical, though, because typical upstream transmissions—usually consisting of mouse clicks and keyboard commands to the central site—require less bandwidth. The upstream transmissions will continue to be sent at the 33.6-kbits/s rate. The technology is primarily targeted toward Internet users who tend to download big files such as sound, video, or multimedia files.

The new modems will be shipped with CompuServe, America On-Line, and NETCOM's NETCOMplete Internet software, as well as Total Entertainment Network Internet gaming software. Pricing is expected to run between $149 and $169.

For more information, contact Boca Research, 1377 Clint Moore Rd., Boca Raton, FL 33487-2722; (561) 997-6227; fax (561) 997-7189; Internet: http://www.bocaresearch.com.

Cybox is a battery-powered pocket-sized PC. Cybox uses an Intel 386EX processor, 1-16 Mbytes DRAM, flash EPROM, and a complete 3.3-V design. Featuring two PCMCIA slots and a graphic interface for standard monitors and flat-panel displays, the unit measures 12 cm by 8 cm by 2 cm (about 4.7 in. by 3.1 in. by 1.5 in.).




The Cybox Design Sample, on the other hand, comes with 4 Mbytes of flash EPROM and 4 Mbytes of RAM. The Design Sample comes with BIOS and ROM-based DOS. There also are utilities that support the burn-in of user applications into the flash EPROM, or the installation of an interlink connection to another computer via a serial line.

Both units are available from American ELTEC. The Design Sample allows users to create application-oriented hardware and software configurations. Examples of these applications include data acquisition, mobile Internet access, navigation systems, and plant control.

Pricing for the Cybox Design Sample begins at $2000.

For more information, contact American ELTEC Inc., 101 College Rd. East, Princeton, NJ 08540-6601; (609) 452-1555; fax (609) 452-7374; Internet: http://www.eltec.de.

Drag and Zip version 2.0 is a software program that allows users to manage their compressed files and archives with the zip, tar, and gz extensions. The tool also lets Internet surfers decode their encoded files from within Windows 95 or NT.

The new software from Canyon Software gives PC users new ways of extracting and viewing their zip files through a flexible zip file manager that works with both Explorer and Canyon's Drag and File program. Embedded folders can be listed in the zip file listing or in a left-hand window, as in Explorer. Additionally, multiple zip files can be viewed one at a time. Drag and Zip 2.0 is the only zip file viewer that includes a virus scanner.

Users can create self-extracting zip files. Within these zipped files, regular files may be launched or viewed. For users who send their files to other users who may not have the program, auto-launch self-extractors can be created. These self-extractors will extract the files from the archive, then automatically launch the application to which the file belongs.

Zip files that have been encoded with Uuencode and MIME formats can be unencoded with Drag and Zip. On the flip side, Drag and Zip also will create files encoded with Uuencode and MIME formats. The new version's file viewer now supports ASCII text, bmp, pcx, and some tif formats.

The program requires users to have 486 or better machines that have 8 Mbytes of RAM and 2 Mbytes of hard disk space.

Sample versions of the Drag and Zip version 2.0 program can be downloaded at C/NET's download.com site (http://www.download.com), Canyon Software's World Wide Web site (http://www.canyonsw.com) or Bulletin Board System (415) 453-4289, or from Canyon's forum on CompuServe (GO CANYON).

Drag and Zip is priced at $30. Drag and Zip users with the 32-bit version can upgrade at no extra charge.

For more information, contact Canyon Software , 1537 Fourth St., Suite 131, San Rafael, CA 94901; (415) 453-9779; fax (415) 453-6195.

# Information Mine Fields

Education and the entire concept of the local library in the state of West Virginia are experiencing a metamorphosis. West Virginia's public schools and libraries are working with VTLS Inc. to bring InfoMine workstations to residents in the state's rural areas. The workstations provide access to the Internet, e-mail, and a large number of library catalogs throughout the state.

The plan between West Virginia and VTLS entails installing 175 InfoMine workstations in at least one high school in each county, and in selected rural public libraries. The obvious benefit of the program is that the team is bringing the Internet and numerous sources of information to residents in West Virginia's rural areas who've never had them before. As it stands today, 120 of the workstations have been installed.

At the workstations, the software available to users includes the VTLS EasyPAC, VTLS Z39.50 Client, a terminal emulator program, and Netscape. Staff at West Virginia's libraries also have access to the VTLS EasyCAT. The EasyCAT software allows librarians to download and edit bibliographic records from West Virginia's union catalog. Along with VTLS' on-site training of the librarians, the company developed a 45-minute training video to train future users.

Each InfoMine workstation is protected by a security software package. The security software ensures the integrity of the workstation's configuration. Additionally, the InfoMine workstations are outfitted with new laser printers.

The Internet is pumped through the libraries' computers via subhubs using T-1 lines. The information superhighway's traffic is monitored by VTLS to prevent busy lines. Also, statistical information that is intended to contribute to the upgrading of the lines will be collected from the traffic monitoring. According to the director of the West Virginia Library Commission, Dave Childers, the InfoMine system is already being used on a consistent basis with very few problems.

The funding for the InfoMine project came from three grants. For the purchase of the Internet workstations, installation, software, and training, the U.S. Department of Education granted the project $2.5 million. The U.S. Department of Commerce and the Appalachian Regional Commission each granted the project $225,000 and $55,000, respectively, for salaries and the purchase of additional workstations, network equipment, and telecommunication services and software.

The project is a statewide initiative between VTLS, The West Virginia Network for Educational Telecomputing, the State Department of Education, and the West Virginia University.

For more information, contact VTLS Inc., 1800 Kraft Dr., Blacksburg, VA 24060-6351; (540) 557-1200; fax (540) 557-1210; Internet: http://www.vtls.com.—*DS*

## FREE STUFF

A full-line catalog of engineered system components from Nolu Plastics Inc. helps guide users through the steps in specifying conveyor components, leveling pads, rollers, handles, guide rails, position indicators, and stock and custom extrusions. For a free catalog, contact Nolu Plastics Inc., 900 C Tryens Rd., Aston, PA 19014; (610) 358-1770.

Hewlett-Packard Company's 1997 edition of its Test & Measurement Catalog is now available. Included are descriptions of over 1500 products, systems, and services. Also featured are product-comparison charts, tutorial material, and descriptions of other available literature. For a free catalog, contact Hewlett-Packard, 3000 Hanover St., Palo Alto, CA 94304; (800) 452-4844, ext. 5177; Internet: http://www.hp.com/go/tmc97.

## OFF THE SHELF

*"The New Manufacturing Engineer—Coming of Age in An Agile Environment"* published by the Society of Manufacturing Engineers (SME) articulates the role of the manufacturing engineer in the 21st Century. The book examines why the role of manufacturing engineers has changed and why they will be the catalysts for success in manufacturing. Topics that are addressed include manufacturing technologies, inventory and expense control technologies, and manufacturing performance metrics. The 320-page book is priced at $45 ($39 for SME members). For more information, contact SME, One SME Drive, P.O. Box 930, Dearborn, MI 48121-0930; (800) 733-4763; fax (313) 271-2861; Internet: http://www.sme.org.

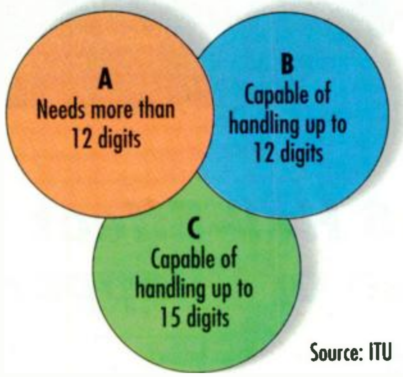
*"Software System Testing and Quality Assurance"* shows readers how to create and maintain reliable, robust, high-quality software. The book covers unit testing to system testing, and also provides an overview of new techniques for security testing, recovery testing, configuration testing, background testing, and performance testing. Integration testing strategies help to ensure that software components are compatible, while a wide range of techniques find and repair bugs at the unit and system levels. The 358-page book is priced at $55.95. For more information, contact the Penton Institute, 1100 Superior Ave., Cleveland, OH 44114; (800) 223-9150; fax (216) 696-6023; Internet: http://www.penton.com.

# It's "T Time," Says ITU

The International Telecommunication Union (ITU) recently requested all telecommunications administrations that their telephone switches and networks should be able to handle international telephone numbers up to 15 digits in length. Until now, most telecommunications switches dealt with numbers of 12 digits or less. But because of plans by a number of telecommunications carriers to introduce 15-digit numbers, it was necessary to upgrade switching equipment to enable the continued free flow of telecommunications traffic between countries.

To deal with this situation, the ITU designated 11:59 p.m., December 31, 1996, as "Time T." All ITU Member States were notified of the need to upgrade equipment to enable them to continue to receive normal traffic. Time T also stipulated that additional digit analysis capabilities be brought into service, with 7-digit analysis required on some international calls. (The complete timetable for network changes is detailed in ITU-T Recommendations E.162 and E.165.)

The ITU made sure that the requirements of Time T were implemented in a coordinated way across the world. Countries that failed to comply with Time T and did not expand the number-handling capacity of their equipment would only be able to make operator-assisted calls to countries that had expanded their numbering plan to 15 digits *(see the figure)*.




Source: ITU

Subscribers and users in Country B would not be able to call subscribers in Country A, who need more than 12 digits, while all subscribers and users in Country C would be able to call all subscribers in Countries A and B. The service providers/operators in Country A, who could normally receive calls from all over the world (Countries A, B, and C) would only be able to receive calls from Country C. Calls from Country B would not be successful because the latter did not have the necessary digit capability.

Calling subscribers and users in Country B, who prior to Time T had direct contact with all subscribers in Country A, would no longer be able to call subscribers in Country A directly. The negative impact of noncompliance with the requirements of Time T would have been both on the called subscribers and service providers/operators in Country A, as well as on the calling subscribers, users, and the involved service providers/operators in Country B.

According to the ITU's Telecommunication Standardization Bureau, the implementation of network upgrades had gone smoothly, and consumers should not experience any difficulties in placing international calls. The ITU-T Study Group 2 had given 10-years' prior notice and planned and managed the worldwide move to 15-digit network capacity. To date, most countries have made the transition and implemented the new procedures without much difficulty.

For further information on these and other international telecommunications developments, contact the ITU, Place des Nations, CH-1211 Geneva 20 Switzerland; +41 22 730 51 11; fax +41 22 733 72 56; Internet: http://www.itu.ch.—*MS*

## QUICKNEWS

In response to an International Data Corp. research study that showed the worldwide unmanaged Ethernet hub market growing at a rate of 92% from 1995 to 1996, Allied Telesyn International has cut its prices on 4- and 8-port unmanaged hubs 30% and 35%, respectively. Additionally, the study found that the unmanaged hub market remains steady at 14.2 million ports in 1996.

Providing the same functionality as the larger hubs (network partitioning, no configuration requirements, and packet regeneration), the unmanaged hubs also come with network diagnostic LEDs located on the front. The LEDs help in fault isolation and troubleshooting.

Pricing on Multiport Twisted-Pair Micro Hubs is as follows: for the AT-MR415T 4-port hub, $74 (down from $106); for the AT-MR815T 8-port hub, $96 (down from $148).

For more information, contact Allied Telesyn, 19015 N. Creek Pkwy., Suite 200, Bothell, WA 98011; (206) 481-3784; fax (206) 483-9458; Internet: http://www.alliedtelesyn.com.

Expanding on its Nijmegen, The Netherlands, plant, Philips Semiconductor has invested another $15 million in the company's discrete RF product line. The discrete products wafer fab at Nijmegen is one of five separate wafer fabs at the site.

Now, a total production area of 3000 square meters is operational. All critical wafer handling areas meet class-100 clean room requirements. Products that are currently manufactured at the Nijmegen plant include CATV modules, cellular-phone RF power modules, general-purpose broadband transistors, and video modules.

The $15 million investment will be going to special equipment required in the double-polysilicon process to produce Philips' new fifth generation RF wideband transistors. Equipment to be installed initially includes EPI-layer deposition, fine-line metallization, and rapid thermal anneal machines.

The rapid thermal annealing process is paramount to the implanted dopants in the first layer of epitaxial polysilicon. There are very steep doping profiles required in the base and emitter regions of the RF wideband transistors. Additionally, new wafer test equipment will be installed at the plant.

The packaging technology also is essential here. The new transistors must maintain their performance and meet new miniaturization levels.

For more information, contact Philips Semiconductors, 811 E. Arques Ave., P.O. Box 3409, Sunnyvale, CA 94088-3409; (408) 991-3614; fax (708) 296-8556; Internet: http//www.semiconductors.philips.com.

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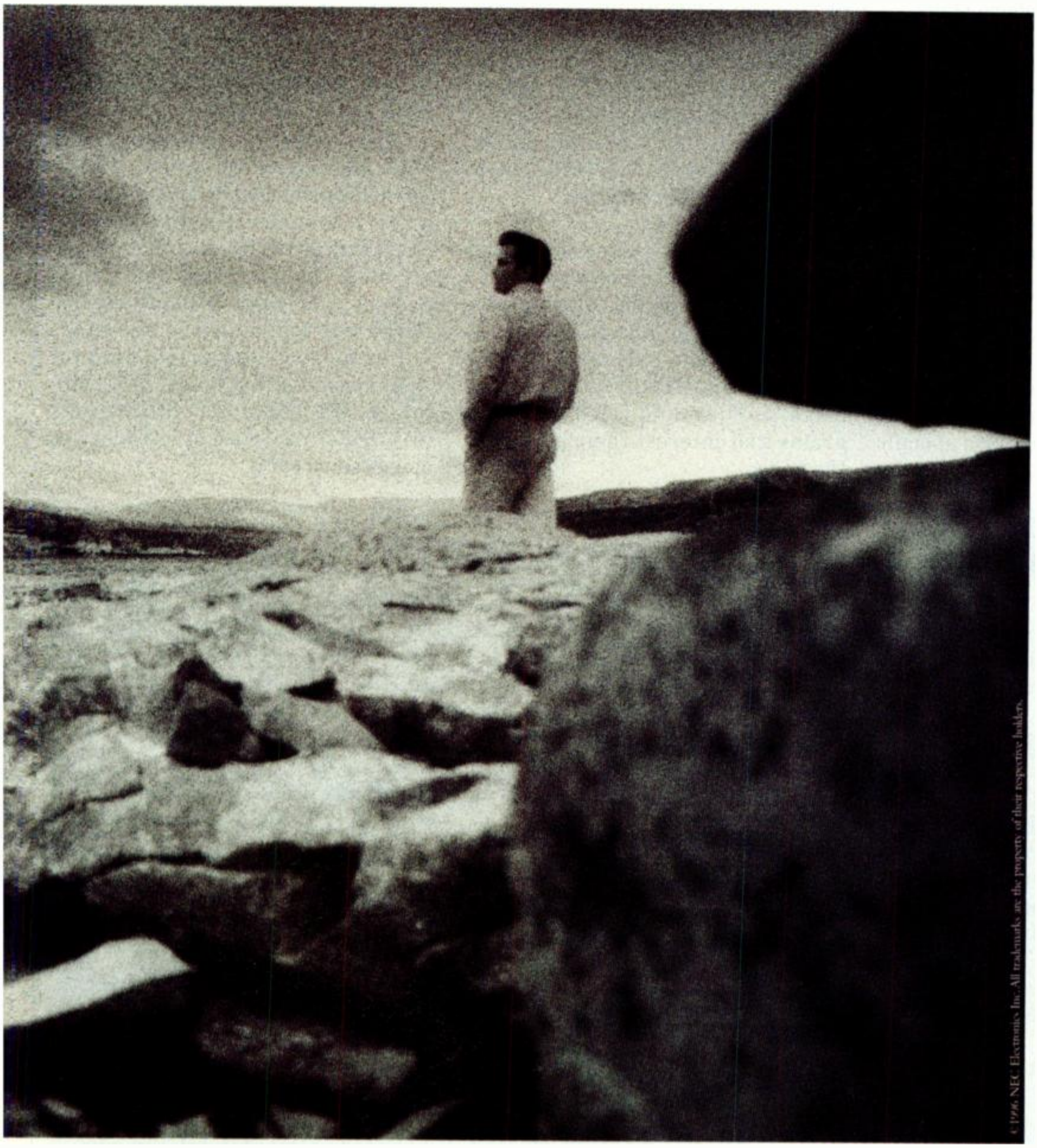


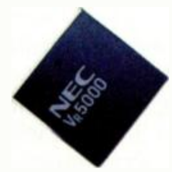


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| | VR4100 | PPC403GA | VR4300 | PPC603 | VR5000 | PPC604 |
|---|---|---|---|---|---|---|
| Frequency | 40MHz | 25MHz | 133MHz | 80MHz | 200MHz | 100MHz |
| Bus Interface | 32-bit | 8/32/64-bit | 32/64-bit | 32/64-bit | 64-bit | 64-bit |
| I-Cache Size<br>D-Cache Size | 2KB<br>1KB | 2KB<br>1KB | 16KB<br>8KB | 8KB<br>8KB | 32KB<br>32KB | 16KB<br>16KB |
| Pin Count/Package | 100 PQFP | 160 CQFP | 120 PQFP | 240 CQFP<br>256 BGA | 272 BGA<br>223 CPGA | 304 CQFP<br>256 BGA |
| SPECint92/SPECfp92 | 45 VAX MIPS | --- | 80/60 | 75/85 | --- | 128/120 |
| SPECint95/SPECfp95 | --- | --- | --- | --- | 5.5/5.5 | --- |

NEC

READER SERVICE 150

## INTERNET NEWS

Introducing SemioMap, the first Java Discovery Search application. Brand-new company Semio Corp. makes the software available at their web site—**http://www.semico.com.** The tool uses data visualization to display logical connections between text and ideas via graphical maps.

Java Discovery Search works by analyzing and categorizing text in real time. If a user wants to find information about a certain topic, a query would be entered and the content would be returned. The search would then yield results in a number of different categories and subcategories in a format that resembles a box diagram with data placed in descending importance.

Currently, the two types of searches available are exhaustive and solution. Exhaustive searches look for all the relevant documents. Solution searches look for a specific answer to a specific query.

Discovery Search technology works on a different premise—look for information about the subject and organize that information so that users can understand what's available. SemioMap allows users to examine their results without scanning or reading large numbers of documents. Essentially, it does the job of several web surfers by indexing content as they go along.

For more information, contact Semio Corp., One Twin Dolphin Dr., Redwood Shores, CA 94065; (415) 802-2940; fax (415) 802-2942.

For the Internet user who likes everything to come to them in a personalized manner, Open Sesame is the place to go. All surfers have to do is click on the URL and all of the latest books, CDs, upcoming concerts, movies, and television programs that interest them pop up on the page.

The site works by taking a quick interest profile, and updating it when users click on different places in the site. Through its Learn Sesame intelligent agent the site becomes more adept at choosing information that the user prefers the more often the user visits the site. Open Sesame uses both user clustering and repetitive behavior learning technologies to deliver personalized information and suggestions to the user.

Open Sesame is updated on a daily basis, and needs no proprietary desktop software other than a standard web browser or e-mail package. Partnership programs are available for both Open Sesame and Learn Sesame. The Open Sesame service can be used for free at the web site.

For more information, contact Open Sesame, 55 Wheeler St., Cambridge, MA 01238; (617) 491-3474; fax (617) 868-0780; Internet: http://www.opensesame.com.

## Master's Degree By Satellite

Remote education has been steadily evolving with the technological advances of the Internet, as well as satellites. A surprising amount of undergraduate and graduate degree programs are churning out well-educated students who've received in-depth instruction by the use of advanced satellite television technology. One such institution taking advantage of the technology is the National Technology University (NTU). The school has offered a master's degree program in management of technology since 1989.

Founded in 1984, the school's philosophy is based on bringing technology education to the workplace. Currently, NTU is the only university in the United States to offer technical managers a degree program in management of technology that lets them stay on the job while interacting with top engineering and management professors via the school's satellite system.

Professors participating in the masters of technology program at NTU represent such higher-education icons as Lehigh University, George Washington University, Georgia Institute of Technology, Rensselaer Polytechnic Institute, and Rutgers University.

The NTU program allows master's students to integrate their education with their current job, and advance their professional development—an ideal situation for most technology professionals. The school stresses that their master's program is not a "techno-business degree where technology courses are merely add-ons to traditional MBA course work," according to NTU's chair of the management of technology program, Al Bean.

Designed to anticipate and respond to industry needs, the two-year program is focused on a global-economy outlook. The program comprises an integrative field research project, a sequential set of nine courses, and a two-week international study mission. Each class has approximately 30 students. The students progress as a group, concentrating on the complexities of strategic business knowledge in the context of technology.

The courses take an in-depth look at business and management, engineering, and science disciplines. Additionally, the program covers areas such as innovation issues and methodologies; bringing new technologies to market; technology transfer; integrating technology into an organization's strategic objectives; and managing business, finance, international science, technical resources, and technology issues.

Students who are already participating in the program have gained the advantage of building a very wide network comprised of a number of top computer, telecommunications, technology, and science professionals.

For more information on the program, contact National Technical University, 700 Centre Ave., Fort Collins, CO 80526-1842; (970) 495-6400; fax (970) 484-0668; Internet: http://www.ntu.edu.—DS

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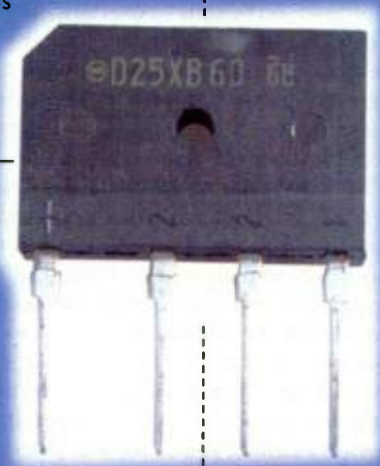


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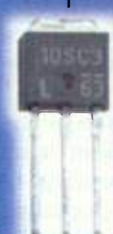

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READER SERVICE 164

## Y2K UPDATE

Back in late January, the Year 2000 Information Center (**http://www.year2000.com**) conducted an informal survey of its visitors, asking various questions about their companies' Year 2000 Date Change (Y2K) plans. The results were surprising in some cases and frightening in others. Approximately 1100 people completed the survey. Following is a discussion of the study results with accompanying commentary by Peter de Jager.

On the subject of user groups, 38% of the respondents answered that they were not members of user groups and that they did not plan to join any in the future; 44% said that they weren't members of user groups at the time of the survey, but intended to join one in the future; and 18% of the respondents replied that they were members of user groups. De Jager found that it was "surprising that 38% of the respondents have no intention of joining a Y2K user group, especially when that is the number one source of 'unbiased' vendor information."

In a related question, "Is your company a member of an Industry-based Y2K Forum?" 53% of those responding answered that they weren't and didn't plan to in the future, 29% answered that they weren't, but planned to join one, and 18%, again answered that they were members of a Y2K Forum. According to de Jager, "The benefits which can be generated from these forums exceed just feedback on vendors. These groups have the ability to set standards and even force vendors to comply with these standards."

### WHO REALLY KNOWS THE SCORE

Bear in mind that de Jager's survey is completed by "mostly the programmers/analysts," and that the results tend to be a bit more reliable than those found with the managers who "tend to paint a rosy picture." More demographics will be coming in the future as more participants fill out the survey.

Speaking of management, another question directly addressed the higher-ups' awareness of the Y2K compliance issue. Answering "Do you believe your company's executive management is aware of the real risks involved in this project?" 24% said "no," 63% said "yes," and 13% said "don't know." Since a quarter of the decision makers are unaware of the real risks, the question is, de Jager says, "who's going to bring them up to speed?"

Taking a look at media exposure, 69% of the respondents said that they thought that there hasn't been enough coverage of the issue, 28% thought that the coverage matched the size of the problem, and 3% expressed that there is too much coverage of Y2K. "The press is still in the early awareness stages, and the interviews reflect that," says de Jager. Examining the information available, most of it comprises press releases of new tools, licensing agreements, and consulting services. Additionally, the articles which explain the story of Y2K are nearly identical in nature, blaming the programmers for their "lack of foresight." Stories will change dramatically by the end of 1998, exclaiming failed systems, widespread panic, and exorbitant programming and reprogramming rates.

### SCARY NUMBERS

One of the frightening numbers of the survey is the 11% of respondents who replied that their organizations had not performed a Y2K Impact Assessment and do not plan to. Odds are they won't be in business by then if the rest of their policy consists of this "head-in-the-sand" approach. More frightening numbers: 30% of the respondents have yet to start an Impact Analysis and only 18% have completed their Impact Analysis. These figures "seem to fly in the face of other surveys which claim 85% of CIOs say they do have a plan, but verifies my observations that no more than 35% of all companies are 'really' working on this project," asserts de Jager.

More scary numbers are in the replies to the question, "Based upon your assessment, what percentage of your software applications (including vendor software) will be impacted by the Y2K unless fixed?" Of the respondents, 10% said that 0% to 10% of their applications would be affected, 6% said 0% to 20%, 5% said 20% to 30%, 5% said 30% to 40%, 5% said 40% to 50%, 6% said 50% to 60%, 7% said 60% to 70%, 9% said 70% to 80%, 9% said 80% to 90%, and a whopping 28% said that they just didn't know. According to de Jager, the 28% with no idea of what percentage of their software would fail at the millennium correlates with the 30% of respondents who have yet to perform an Impact Analysis. Even more notable, "41% of the respondents found more than 50% of their applications to be Y2K incompatible," says de Jager.

The final question of the survey, "Based upon your project plan, what percentage of these applications do you intend to fix, replace, renovate?" again reinforced fact that a large percentage of the Y2K-aware community still has a long way to go before their systems are compliant. Dipping into the numbers, 7% of the respondents replied that they would fix or replace 0% to 10% of their software applications, 2% said 0% to 20%, 3% said 20% to 30%, 2% said 30% to 40%, 2% said 40% to 50%, 2% said 50% to 60%, 3% said 60% to 70%, 4% said 70% to 80%, 5% said 80% to 90%, 35% said 90% to 100%, and 36% said that they didn't know how many software applications they would repair or replace at the millennium. De Jager says that he's concerned with the "36% of the respondents who have no idea how much work is ahead of them."—DS

### Wanted: An Embedded Systems Engineer

According to Peter de Jager, one of the most-needed experts the Y2K industry needs is the Embedded Systems engineer. "Despite all the allegations of the press, we are VERY reluctant to speculate about the areas in which we're not experts," he says. So, step up to the plate if that's your background—your input is quickly becoming crucial. E-mail Peter de Jager at pdejager@ hookup.net, or call his office: (905) 792-8706.


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## FLIPPING THROUGH THE INTERNET ROLODEX

**http://www.hh.avnet.com:** Sail into the new Hamilton Hallmark homepage to find easily-accessible links to the company's products, resources, services, and events. Supplier product announcements can be found, as well as prices and availability of 25,000 products, in the Products section. Reference design kits, leading technical publications, technical advice, and FAQs can be spotted in the Resources section. ASIC design services also can be found at the site.

**http://www.cemacity.org:** Looking for the Consumer Electronics Manufacturers Association (CEMA)? Search no more, because CEMA's homepage has all the latest information on the Consumer Electronics Show (CES), in addition to all the CEMA-sponsored trade shows including CES Mobile Electronics and CES Habitech. In the Convention Center, visitors will find exhibitor lists, fact sheets, programs, events, and registration for housing and attendance. Press releases are found in the CEMACITY Gazette. Members and future members can meet at Town Hall, and e-mail CEMA membership staff. The Government Plaza features the latest testimony from Capitol Hill and CEMA's position on various issues.

**http://www.industry.net/kavlico:** Don't get caught in the undertow on your way to Kavlico's new homepage! The pressure and position sensor manufacturer has put its company and product information on over 80 screens linked to the homepage. Descriptions about the company's manufacturing facility, pressure sensor technology, automotive and diesel engine applications, HVAC and industrial pressure sensors, and OEM sensor modules can be found here. Detailed specifications for voltage output pressure sensors and 4 to 20 mA current output pressure transmitters are at the site, as well as a synopsis of Kavlico's electromechanical position sensors for aerospace applications. E-mail contacts for visitors to the site also are available.

**http://www.spectran.com:** Visitors to SpecTran's new site will find that it features information on the company's communication-grade and specialty optical fibers, cables, and related products. Visitors to the site can pick up SpecTran's latest news releases, financial highlights, and information on career opportunities. Additionally, there is a literature library comprising the company's annual report, 10K report, quarterly report, product information, and technical articles. Also found at the site are brochures on SpecTran's three subsidiaries.

**http://www.micromo.com:** Swimming through the sea of URLs on the web might lead you to MicroMo Electronics' page. The web site was started in response to customer survey results that said that customers wanted up-to-date product and technical information available on the World Wide Web. MicroMo's main products are coreless motors and related technologies. Featured items at the site include new applications notes, selector guides, annotated links to other engineering sites, technical and Internet tutorials, and a downloadable catalog. The catalog comes in Portable Document Format, and can be read via Adobe Acrobat Reader, which is available for downloading at the site.

**http://www.compliancenet.com:** Compliance-conscious 'net surfers will probably want to stop off at The Boxleitner Group's ComplianceNET site. The continuously-updated directory has complete listings of legally mandated regulations and standards for hundreds of electronic and electrical products for countries worldwide. Topics found at the site include electromagnetic compatibility, product ergonomics, product environmental requirements, product quality requirements, and product safety. Also, proposed regulations and standards are listed here. The directory is indexed by country and product, providing an easy way to track a standard or regulation. A free test of the directory is available at the site.

## JULY

**IEEE Signal Processing Workshop on Higher Order Statistics, July 21-23.** Banff Centre for Conferences, Banff, Alberta, Canada. Contact Keh-Shin Lii, Department of Statistics, University of California, Riverside, 900 University Ave., Riverside, CA 92521; (909) 787-3836; fax (909) 787-3286; e-mail: ksl@ucrstat.ucr.edu.

**IEEE Nuclear & Space Radiation Effects Conference (NSREC '97), July 21-25.** Snowmass Conference Center, Snowmass, CO. Contact Dennis B. Brown, Naval Research Laboratory, Code 6612, Washington, DC. 20375; (202) 767-5453; fax (202) 404-8076; e-mail: dbbrown@ccfnrl.nvy.mil.

## AUGUST

**40th Midwest Symposium on Circuits and Systems, Aug. 2-6.** Hyatt Regency Hotel, Sacramento, CA. Contact Sharon Baumgartner, Department of E&CE, University of California, Davis, CA 95616; (916) 754-6216; fax (916) 752-8428; e-mail:mwscas97@ece.ucdavis.edu.

**IEEE International Geoscience & Remote Sensing Symposium (IGARSS '97), Aug. 4-8.** Singapore International Convention Exhibition Centre, Suntec City, Singapore. Contact Kwoh Leong Keong, CRISP, National University of Singapore, Faculty of Science, Lower Kent Ridge Rd., S 119260 Singapore; (65) 7727838.

**Memory Technology, Design, & Test Workshop, Aug. 11-12.** San Jose, CA. Contact F. Lombardi; (409) 845-5464; e-mail: lombardi@cs.tamu.edu.

**IEEE International Symposium on Electromagnetic Compatibility (EMC '97), Aug. 18-22.** Contact John Osburn, EMC Test Systems LP., 2205 Kramer Lane, Austin, TX 78758; (512) 835-4684 ext. 669; fax (512) 835-4729.

## SEPTEMBER

**Telecom Interactive '97, Sept. 8-14.** Geneva, Switzerland. Contact (703) 907-7736.

**Fifth European Congress on Intelligent Techniques and Soft Computing (EUFIT '97), Sept. 8-12.** Aachen, Germany. Contact Promenade 9, 52076 Aachen, Germany; (49) 2408 6969; fax (49) 2408 94582; e-mail: eufit@mit-gmbh.de; Internet: http://www.mit-gmbh.de/elite/elite/eufit.html.

**ICSPAT/DSP WORLD 1997, Sept. 14-17.** San Diego Convention Center, San Diego, CA. Contact Denise Chan, Miller Freeman Inc. (415) 278-5231; e-mail: dsp@exporeg.com.

**MCM Test Workshop, Sept. 14-17.** Napa Valley, CA. Contact Y. Zorian, (408) 453-0146 ext. 227; e-mail: zorian@lvision.com.

**International Conference on Solid State Devices and Materials (SSDM), Sept. 16-19.** Act City Hamamatsu, Hamamatsu, Japan. Contact Secretariat of SSDM '97, % Business Center for Academic Societies Japan, 5-16-9 Honkomagome, Bunkyo,Tokyo 113, Japan; (81) 3 5814 5800; fax (81) 3 5814 5823; e-mail: confg3@bcasj.or.jp.

**Thermionic Workshop, Sept. 21-23.** Cannes, France. Contact B. Courtois; (33) 35 76 7 46 15; e-mail: bernard.courtois@imag.fr.

**AUTOTESTCON '97, Sept. 22-25.** Disneyland Hotel, Anaheim, CA. Contact Robert C. Rassa, Hughes Aircraft, P.O. Box 92426, MS R07/P553, Los Angeles, CA 90009-2426; (310) 334-4922; fax (310) 334-2578; e-mail: rcrassa@ccgate.hac.com.

**Electrical Overstress/Electrostatic Discharge Symposium, Sept. 23-25.** Santa Clara Convention Center, Santa Clara, CA. Contact ESD Association, 7902 Turin Rd., Suite 4, Rome, NY 13440-2069; (315) 339-6937; fax (315) 339-6793.

**Fifth China International Electronics Exhibition (CIEE '97), Sept. 24-28.** China International Exhibition Centre, Beijing. Contact Gu Jinjing, CEIEC, P.O. Box 140, Beijing, 100036 China; (011) 8610 6822 3909; fax (011) 8610 6821 3348

**Eastern Regional Conference on Crystal Growth & Epitaxy, ACCGE/East-97, September 28-Oct. 1.** Bally's Park Place Hotel & Casino, Atlantic City, New Jersey. Contact Louis G. Casagrande, (516) 346-6379; fax (516) 346-3670; e-mail: Lou_Casagrande @atdc.grumman.com, or Ed Porbansky, Conference Secretariat, 163 Carson Dr., Colonia, NJ 07067; (908) 382-1806.

**Embedded Systems Conference, Sept. 29-Oct. 3.** San Jose Convention Center, San Jose, CA. Contact Miller Freeman Inc. (415) 278-5231; e-mail: esc@exporeg.com.

## OCTOBER

**OEMed Northeast, Oct. 1-2.** Bayside Expo Center, Boston, MA. Contact Exposition Excellence Corp., 112 Main St., Norwalk, CT 06851; (203) 847-9599; fax (203) 854-9438.

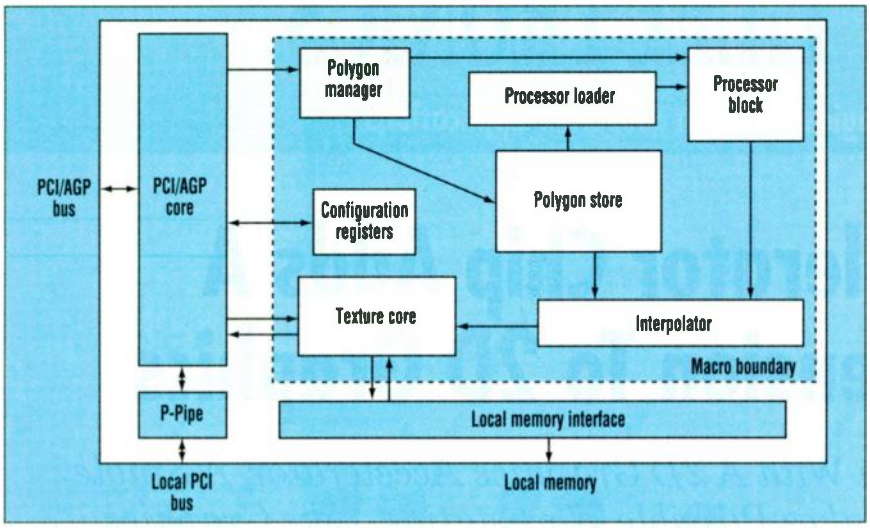
**OEM Electronics Northeast, Oct. 1-2.** Bayside Expo Center, Boston, MA. Contact Exposition Excellence Corp., 112 Main St., Norwalk, CT 06851; (203) 847-9599; fax (203) 854-9438.

**IEEE Ultrasonics Symposium, Oct. 7-10.** Marriott Hotel, Toronto, Canada. Contact Stuart Foster, Dept. of Medical Biophysics, Room S-658, Sunnybrook Health Science Ctr., 2075 Bayview Ave., Toronto, Ontario, M4N 3M5, Canada; e-mail: stuart@owl.sunnybrook.utoronto.ca.

**Sixth IEEE International Conference on Universal Personal Communications, Oct. 12-16.** Hotel del Coronado, San Diego, CA. Contact Gail Weisman, IEEE Communications Society, 345 E. 47th St., New York, NY 10017; (212) 705-7018; fax (212) 705-7865; e-mail: g.weisman@ieee.org.

**Sixth IEEE International Conference on Universal Personal Communications (ICUPC '97), Oct. 13-15.** Contact Tony Acampora, MC 0409, Bldg EBU1, UCSD, 9500 Gilman Dr., La Jolla, CA 92093-0409; (619) 534-5438; fax (619) 534-2486; e-mail: acampora@ece.ucsd.edu.

**Conference on Domain-Specific Languages (DSL), Oct. 15-17.** Red Lion Resort, Santa Barbara, CA. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.




**1. In the TEX chip is a major processing block containing an array of parallel processors and logic to implement the polygon processing and control. Another portion of the chip contains the P-Pipe logic, which provides a PCI-to-PCI bridge to where a 2D PCI graphics processor can be attached.**

bandwidth transfers. Most of the operations needed to compute translucency, hidden-surface removal, and antialiasing require high-speed computations to perform real-time operations. One of the more-complex operations, the true-perspective correction, also requires a division operation per pixel, thus making it one of the most math-intensive operations.

Bus bandwidth becomes the limiting factor for Z-buffering and various surface attributes. For anisotropic texturing, coherency is not the same and caching is more difficult because of the different possible shapes used for texturing.

In addition to the strong polygon support, the key block on the chip that lets the circuit deliver top-notch 3D graphics is the overall PixelSquirt II technology, which alleviates the main bottleneck in interactive 3D graphics, the pixel fill rate *(Fig. 1)*. The technology is based on the concept of parallel fixed-purpose processors that maximize the fill rate based solely on the geometry (XYZ) of the triangles. The "processor" in this case has been shrunk to a point that a large number of processors can be included on a custom chip at a very cost-effective price.

As mentioned earlier, the TEX chip can achieve near-workstation performance—on a 1024-by-768, 24-bit per pixel screen with a 30-Hz frame rate, the circuit can deliver 10,000 triangles/frame (300,000 triangles/s, with each triangle a MIP-mapped 100-pixel element with bilinear texturing using RGB lighting. This can be achieved for real applications executing on a PC that operates with a 33-MHz PCI bus, with 1 to 4 Mbytes of optional texture memory, and employs the Triton II or better motherboard chip set.

Theoretical peak performance of the TEX-based system includes the ability to deliver 150 million textured pixels per second (each pixel is MIP-mapped and has bilinear texturing), or deliver 1 million polygons/s, with each polygon containing 10 pixels with RGB lighting, RGB specular, fog, alpha, and floating-point input. Top resolution of 1024 by 768 pixels with 24 bits/pixel at 53 frames/s (10,000 polygons/frame, tri-MIP-mapped and Z-buffered) can be achieved—yielding a pixel data rate of more than 150 Mpixels/s.

To deliver the rendered images for games, VRML environments, and other applications, the TEX processor places minimal overhead on the host processor, and appears mostly as a PCI or AGP device attached to the host. However, it contains several additional buses, one of which is a local PCI bus. That bus is generated by a block called the P-Pipe, which implements a PCI-to-PCI bridge to allow additional functions such as a 2D graphics processor to be included on the same board. All PCI traffic except the polygon list (10 Mbytes/s) is moved to the back end of the P-Pipe over this bus to communicate with the 2D PCI graphics chip. The host PCI bus is a master/slave interface and includes big- and little-endian support for various hosts.

To achieve high performance texture mapping, an on-chip high-performance DRAM texture storage area of 1 to 4 Mbytes (or more) would ideally be required. However, by incorporating a local memory bus interface on the chip, it's designers were able to locate that memory off chip without any significant performance penalty. That memory can be formed using multibank DRAMs or synchronous graphics DRAM (SGRAM).

The overall flow of data through the TEX chip is similar to that of the PIX processor, with one significant difference—the TEX can write directly to a 2D device's linear or rectangular frame buffer, as well as to main memory. That is possible since the host is no longer directly involved in the pixel texture mapping operations. Inputs to the TEX chip are in the form of a Y-sorted triangle list, similar to the PIX chip, but the format has been enhanced for lower-overhead application programming interface support. Improvements in this area include the addition of scatter-gather DMA and floating-point input formats.

To do the integration effectively, designers had to carefully balance the work done by the processor array and that done by other logic. Thus, the processor array employs an on-chip "active-triangle" display list to render a scene in scanline raster order. The engine starts by reading a driver-prepared display list from memory to update the on-chip list and then, after setup, visibility determination, and interpolation, starts to deliver the rendering data, beginning with the topmost texel (or a blend of texels) for each pixel in the scene in left-to-right, top-to-bottom order (as how one would normally read a page of text).

After being textured and accumulated (for translucent pixels), the resultant pixel stream passes into the formatter block on the chip, which buffers, dithers, and formats the data. The resulting 3D image is sent directly to the 2D frame buffer, either over the host PCI bus or through the P-Pipe. Floating-point format conversion, from 32-bit floating-point notation to 16-bit integer values, also is incorporated on the chip. This capability is optimized for reading application-programming in-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terface format software with little driver (software) overhead—offloading the task from the CPU and giving better overall 3D performance.

In addition to the basic operation at 33-MHz for the PCI host-bus interface, the 3D accelerator also can run that interface at the 66-MHz speed required by the AGP interface. A local DRAM bus with a selectable 32- or 64-bit memory bus width and the P-pipe local PCI bus also are incorporated on the chip. Lastly, the memory interface includes support for SGRAM and multibank DRAM to maximize the data transfer rate.

The on-chip AGP support lets it handle the double-clock option, which clocks the bus at 133 MHz. Also, the AGP includes a split-transaction capability, which allows the bus to hide the 20+ clock latency of read operations, allowing those clock periods to be reclaimed for other uses. Lastly, the AGP interface provides virtual address translation for easier data manipulation.

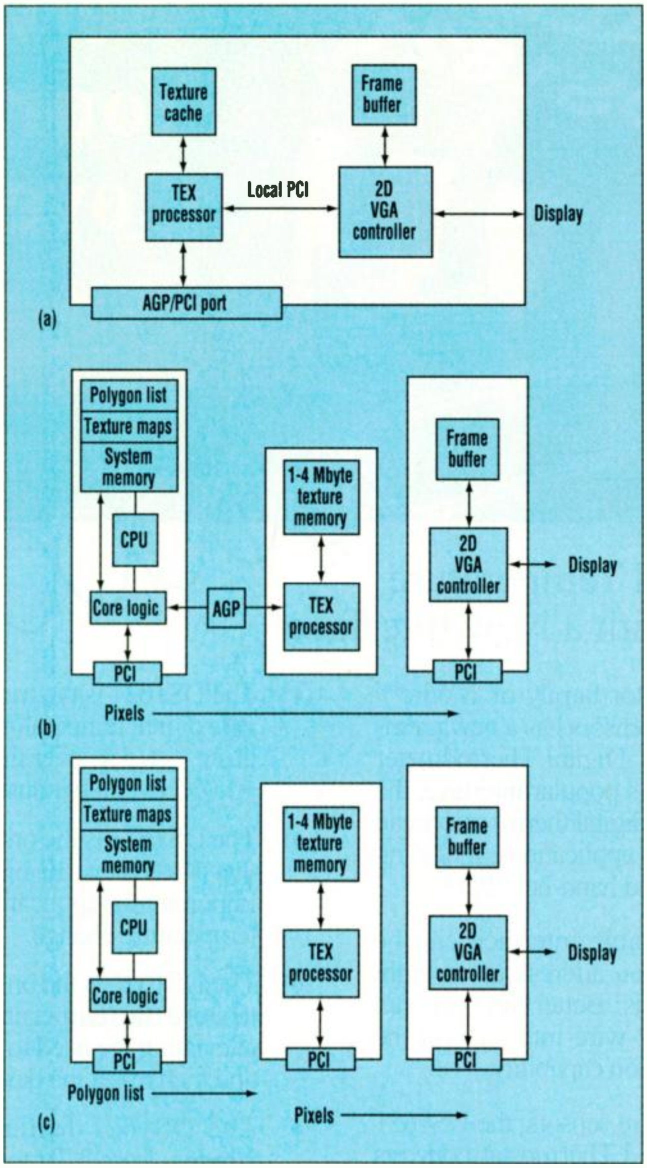
The internal polygon manager on the chip determines when to load primitives, and where to store them once loaded. The first word of the primitive describes the type of primitive (point, line, triangle), and determines how many additional words are needed to fully specify the primitive. A full description of the primitive includes data detailing the primitive type, the point color and alpha, the line color and alpha and perspective correction, and many triangle aspects. Those aspects include the triangle type (flat, Gouraud shaded, textured), RGB color (flat, Gouraud) or texture ID and ST (texture coordinates to sub-texel accuracy for bi-linear) coordinates (textured), triangle texture antialiasing (texture: point, bi-linear, or MIP-mapped), and triangle options such as per vertex Alpha, fog, specular, MIP-mapped. Triangle texture options include the address (local), size (power of two), MIP-map flag, texel format (16/24/32-bit, etc.), and wrapping vs. clamping for each S and T.

The multiple-bus architecture of the TEX chip makes it simple to implement various system solutions that cater to different price points. In the complete 2D/3D system on a card that plugs into a PCI or AGP port, the TEX chip provides the host interface, while tying into on-board texture memory and generating the local PCI bus from the P-Pipe port. That local PCI bus connects to the 2D VGA graphics chip, which in turn, sends the data to the display *(Fig. 2a)*.

Alternate system architectures include a scenario in which the TEX chip is on a separate AGP add-in card with only the texture memory *(Fig. 2b)*. In this case, the 3D information transfers bidirectionally over the AGP port, while the host system transfers pixel data to the PCI-based 2D display engine. In a third option, the TEX chip, the host system, and the 2D graphics accelerator are all transferring the display lists and the pixel data over the PCI bus *(Fig. 2c)*.

An additional interface on the chip includes a universal serial bus port to aid in system configuration. For video support, the chip also can perform 4:2:2 YUV-to-RGB color conversion, bilinear interpolation scaling, and provide support for multiple video windows. The chip operates from a either a 3.3- or 5-V supply but internally operates at 3.3 V, while the I/O lines can interface to either 3.3 or 5-V systems.

Both Reality and S-MOS have developed drivers for Microsoft Windows 95, Windows NT, Direct X support, and other operating environments. Also available are software tools for developing custom drivers.




**2. Various 3D graphic subsystem architectures can be implemented with the TEX processor. In this first example (a), the TEX chip connects to the host PCI or AGP port and the 2D graphics processor connects to the PCI bridge port. Or (b), the TEX chip can be used on a separate card that connects to the host via the AGP port, while the 2D graphics subsystem connects to the host over the PCI bus. Lastly (c), a PCI only approach can be used, in which the TEX subsystem is on one card, the 2D legacy graphics on a second card, and both connect to the host via the PCI bus.**

## Price And Availability

*The TEX 3D accelerator comes in a 208-lead TQFP In 10,000-unit quantities, the TEX chip sells for $35 apiece. Samples will be available in the fourth quarter, with production quantities available in early 1998.*

*S-MOS Systems Inc., 150 River Oaks Parkway, San Jose, CA 95134; Sandeep Gupta, (408) 922-0200; http://www.smos.com.*

*Reality Simulation Systems Inc., 150 River Oaks Parkway, San Jose, CA 95134; (408) 435-5565.* **CIRCLE 538**

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# Videoconferencing Is Getting Better And More Affordable

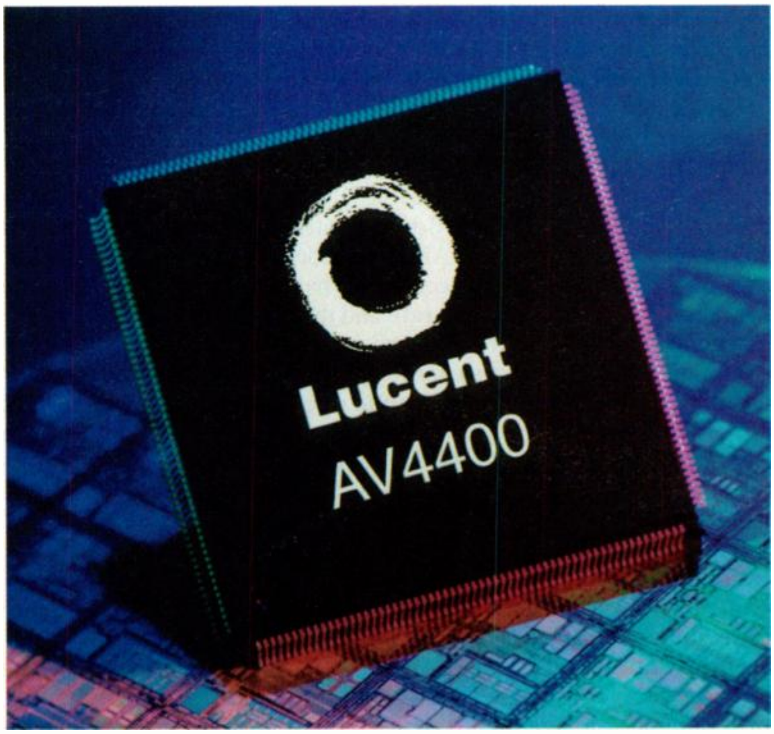
*Dedicated Chips, High-Power Microprocessors, And Innovative Software Are Making Possible High-Quality And Low-Cost Computer-Based Videoconferencing Systems.*

Jules H. Gilder

SPECIAL REPORT

Videoconferencing has been capturing peoples' imaginations ever since AT&T demonstrated its original PicturePhone over 30 years ago. The problem then, as it is now, was bandwidth. In the 1960s, the enormous amounts of data that had to be sent to produce a quality video image and sound in real time required the use of leased telephone lines. Because of the expense of the lines, and the specialized equipment needed to implement videoconferencing, its use was limited to large companies that could afford the investment.

The situation is significantly different today. Currently, the market for videoconferencing systems is over $3 billion. By the year 2002, the market is expected to grow to $35 billion. True, bandwidth is still the key issue, but semiconductor and software technology have joined forces to make it manageable at a reasonable cost. Whereas early systems would cost hundreds of thousands of dollars to implement, today's systems cost in the hundreds or thousands.




Art Courtesy: Lucent Technologies

In addition, leased telephone lines are no longer required. POTS (Plain Old Telephone Service) lines can be used to get quite acceptable results with video-frame rates of 6 to 15 frames per second (fps). This is sufficient for situations where there is very little motion by the parties If the ability to show continuous motion is needed, then an ISDN telephone line will be required. With ISDN and the appropriate hardware, frame rates of 20 to 30 fps can be achieved, yielding results that are close to broadcast-quality video.

Despite the hardware and software advances, standards are still the key to the success of videoconferencing. Despite the availability of industry standards, there's a lack of interoperability among different videoconferencing systems designed to the same standard *(see "Standards are the key," p. 96)*. Nevertheless, the emergence of dedicated video processors has propelled videoconferencing to new heights.

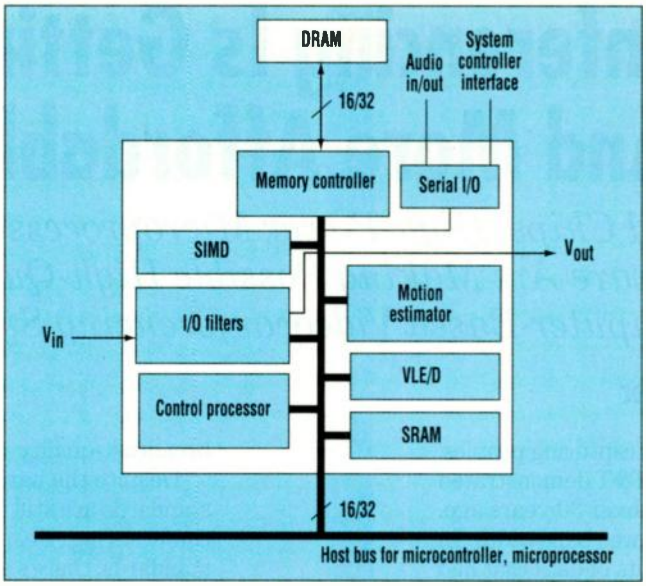
## Video Processors

Ever since PCs appeared on the scene, designers have been repeatedly faced with the same question: "Should the video problem be solved with dedicated hardware or software?" And the answer is always the same: "It depends." The arguments are always the same. The hardware approach is faster, but it's more expensive. The software approach is cheaper, easier to install, and easier to maintain and upgrade. So why should it be different when it comes to videoconferencing? It isn't.

When videoconferencing was first conceived, engineers instinctively knew they could do it. It required specific hardware and was expensive, but they knew what had to be done. A software solution wasn't even considered because many of the hardware developments (e.g., high-speed modems, inexpensive personal computers, and digital cameras) that make a software solution possible didn't exist yet. As the supporting hardware became available and consumer demand for videoconferencing grew, an inexpensive software solution became feasible.

The factor that will determine whether you go with a hardware or software solution is the desired video-image quality. For the highest quality, you still need to use dedicated videoconferencing processors. Three major suppliers of videoconferencing chips are Lucent Technologies with its AVP-III processor, 8x8 Inc. with its Video Communication Processor (VCP), and Texas Instruments with its TMS320C8x family of processors.

The three-chip AVP, the original audio/video processing device for building a videoconferencing system, was introduced back in 1992 by AT&T. Last year, Lucent Technologies, an AT&T spin-off, introduced the AVP-III, a third-generation 0.35-µm CMOS single-chip version, the AV4400.




**1. The AV4400 single-chip video/audio processor is at the heart of Lucent Technologies AVP-III videoconferencing processor. The AV4400 implements the ITU H.32x standards, along with microcode and host software. Based on a 32-bit RISC processor, the AV4400 features video scaling at the input and output, forward and reverse discrete cosine transforms, variable-length encoding and decoding (VLE/D), hardware motion estimation, a 16- or 32-bit host interface and direct connection of up to 2 Mbytes of DRAM for frame storage.**

The AV4400 is fully compliant with ITU-T international standard H.320 (which contains the specifications for ISDN videoconferencing), and the H.324 standard (which contains specifications for videoconferencing over regular telephone lines). Each of these "umbrella" standards contains additional standards that define the video and audio compression algorithms that must be used. For example, H.261 and H.263 specify the techniques to be used for video compression for ISDN and POTS systems, while G.723 and G.728 are standards that specify compression for audio systems on POTS and ISDN systems. JPEG and MPEG-1 support also are built into the chip. The AV4400 has a 32-bit RISC processor core with an associated programmable signal-processing array.

The AV4400 connects to its host processor via a 16- or 32-bit interface that allows the host to initialize and control registers and internal SRAM *(Fig. 1)*. It also allows input and output of compressed and uncompressed audio and video.

The chip requires no external SRAM, but instead uses conventional or synchronous DRAM. Although 3.3-V DRAM is preferable, 5-V DRAM also can be used. The control processor on the chip is a 32-bit RISC processor. It contains a 3-kbyte data-word instruction SRAM. The processor performs coding control (dynamic adjustment of frame rate and quantization), global control (servicing requests for the various coprocessors), bit stream header encoding and decoding, and memory management.

The AV4400 can be programmed to work in one of two modes—constant frame rate or constant quality. According to James G. Rank, Lucent's Product Marketing Manager for visual communications solutions, most people use the constant-quality mode. That means, if there's a lot of motion, the frame rate will decrease, but the image quality will stay the same. In the constant-frame-rate mode, the user generally doesn't care about the video image. He just needs to send a certain number of frames per second. The price you pay for this mode of operation, if you have a lot of motion, is "blockiness."

Using a dedicated videoconferencing chip doesn't tie up the processing power of a CPU, and allows it to perform data-sharing operations that would otherwise be impossible. To foster this sharing of data and applications during a video conference, Lucent has licensed data collaboration software from Data-Beam Corp. and is making it available to OEMs. The software is known as the Collaborative Computing Toolkit. It provides third-party developers with building blocks for adding real-time, multipoint, and data-sharing capabilities to new or existing applications, based on ITU's T.120 standard.

## A Pair Of Engines

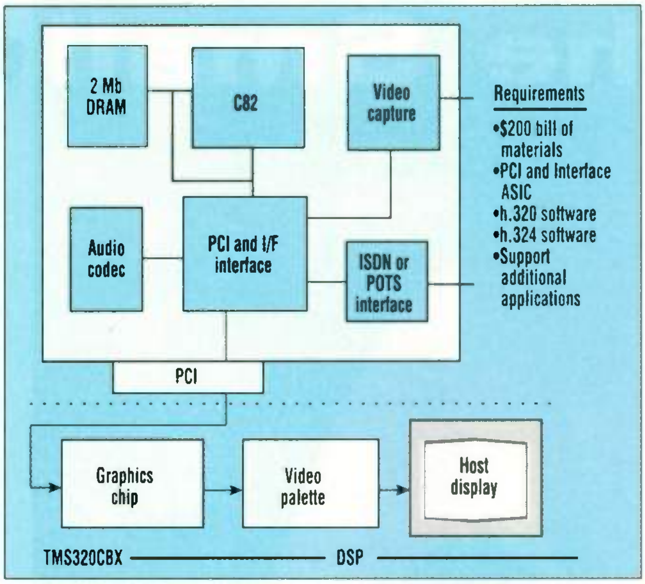
The VCP chip from 8x8 Inc. is another contender for videoconferencing applications *(Fig. 2)*. The 0.5-µm CMOS chip performs all of the processing required for various video compression and decompression algorithms. Its programmable architecture enables it to perform both MPEG encoding and decoding. It handles H.320, H.323, H324, and various fractal and wavelet-based algorithms.

The chip, notes Kevin Deierling, 8x8's Director of IC development, is a custom one. It gets its processing power from two internal programmable engines. The first, a vision controller, is a 32-bit MIPS-X RISC engine that performs higher-level functions such as syntax decoding, system multiplexing, and frame-rate conversion. The second, a vision processor, is a single-instruction, multiple-data (SIMD) 64-bit programmable DSP specially architected to perform video processing.

Whereas most DSPs are good at performing multiply-accumulate (MAC) operations, the SIMD DSP in the VCP chip can do eight MACs at the same time. As a result, instead of working on a single pixel at a time as most other DSPs do, the 8x8 chip can work on eight pixels simultaneously.

This processing engine performs the core video codec tasks of motion search, motion compensation, discrete cosine transforms (DCTs), and inverse DCTs. In addition, specialized programmable hardware provides bit-

slice Huffman encoding and decoding. Also, dedicated hardware performs video pre- and post-processing, including input and output scaling and temporal filtering. Temporal filtering is particularly valuable with noisy analog video signals.




3. The TMS320C82 processor from Texas Instruments can be used with a graphics chip and video palette to implement a videoconferencing system that costs less than $200.

An advanced 0.35-µm version on the way, the VCPex, will have MPEG-2 decode support, and will be able to overlay text over live video with no impact on the encoding or decoding process.

Like the Lucent AVP-III processor, the VCP chip supports CIF (Common Intermediate Format) resolutions of 352 by 288 pixels, which are specially designed to make it easy to display the image on either a PAL or NTSC system. It also supports QCIF (Quarter CIF) resolutions of 176 by 144 pixels. While these resolutions might lead you to believe that the size of your image would be small, especially on a large, high-resolution screen, that's not necessarily the case, because the processor can scale the video image to occupy the full screen.

In fact, notes Deierling, if you take a 352-by-288-pixel image and scale it up to full screen size using VGA resolution (640 by 480 pixels), it produces an image that is the same quality you'd get with VHS video tape. Of course, the image can be scaled larger, like 1024 by 768 pixels, but then you start to see some problems such as blocking artifacts (checkerboard patterns on the video image). Filters are available that can deal with this, but that involves a tradeoff of the filtering for the sharpness of the image.

The company feels that it won't be long before H.323-based products for use on LANs and intranets will catch up to, and even pass, ISDN chips. Presently, a company using videoconferencing spends tens of thousands of dollars to set up a special videoconferencing room with an ISDN line. With H.323, if you have a dedicated ISDN line, you can call out to one of your other sites and then simply run a packet-based protocol, PPP, over the same ISDN line. Suddenly, suddenly everybody's desktop with an H.323 capability added can then go out through this ISDN gateway. So, instead of having just one special room for videoconferencing, everyone on the LAN can have that capability.

Texas Instruments (TI) has developed two general-purpose DSP ICs optimized for video processing—the TMS320C80 and TMS320C82. According to Rick Rinehart, TI's C8x Program Manager, the TMS320C80 has about 1.5 times the processing power of the TMS320C82. The C82, he continues, is meant to be used in systems with data rates up to 128 kbits/s, while the C80 processor is ideal for rates above 128 kbits/s.

The less-expensive C82 saves board space by consolidating multiple processors into a single chip *(Fig. 3)*. It integrates two DSPs and a RISC master processor on the same silicon. Another cost and space-saving feature is on-chip cache memory, which eliminates the need for external, high-cost SRAM to support each DSP. Instead, the system's memory uses lower-cost DRAM. Instruction cache memory for each DSP consists of 4 kbytes, and data RAM is 12 kbytes. The 0.5-µm CMOS 3.3-V chip is housed in a 240-pin PQFP. Each of the DSPs on the chip has a 64-bit instruction word. Says Rinehart, "It would take 10 to 15 typical DSPs and general-purpose microprocessors to equal the performance of the C82 in video applications."

2. The VCP Video Communication Processor from 8x8 Inc., shown here in a videoconferencing board, is a hybrid dual-processor chip that contains a 32-bit MIPS-X RISC engine that operates as a vision controller. It handles syntax decoding, system multiplexing and frame-rate conversion. Its 64-bit programmable DSP is designed to perform video processing.

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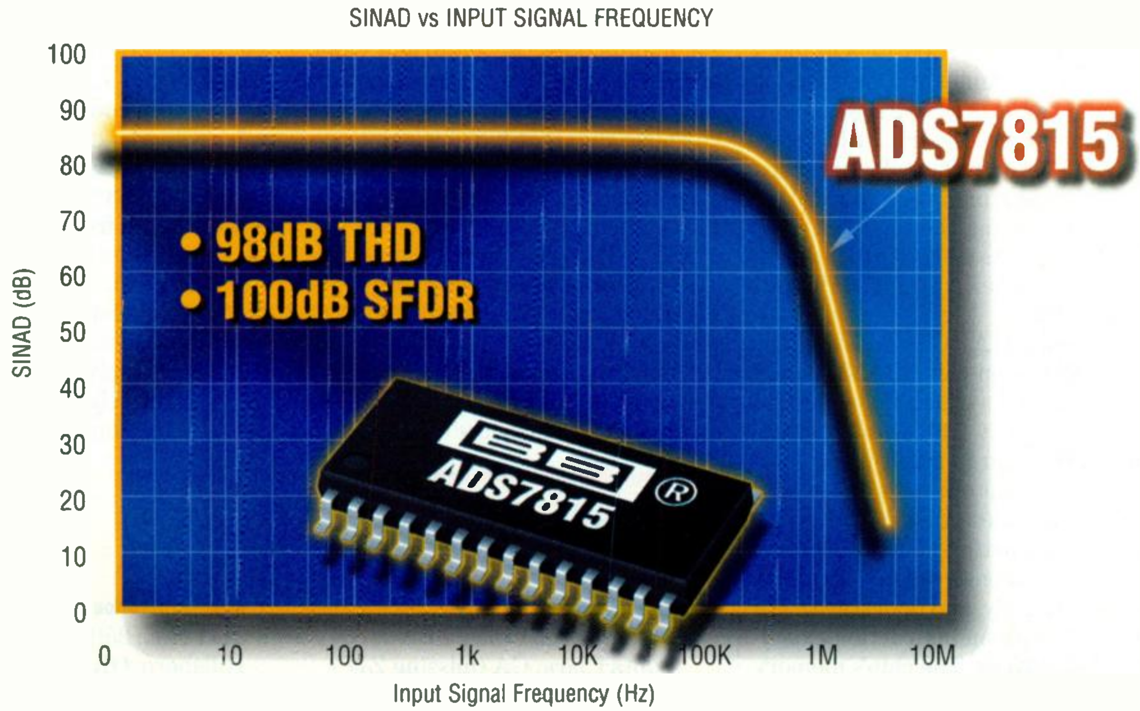


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|---|---|---|---|---|---|---|---|---|---|
| ADS7813 | ±2 | 16 | 40 | 30 | 87 | –96 | 16 | 11302 | 84 |
| ADS7815 | ±4(Typ) | 15 | 250 | 250 | 84 | –96 | 16 | 11364 | 85 |
| ADS7821 | ±3 | 16 | 100 | 100 | 86 | –94 | 16 | 11323 | 86 |
| ADS7825 | ±2 | 16 | 40 | 50 | 86 | –90 | 16 | 11304 | 87 |

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For higher-performance systems such as full-room videoconferencing systems, designers can use the C80 processor. Like the C82, it integrates multiple processors on a single chip. In this case, however, there are four 32-bit DSPs along with a RISC processor. This chip is housed in a 305-pin ceramic PGA package.

One of the newest chips to be used for videoconferencing comes from Analog Devices. Part of Analog's SHARC DSP family of processors, it is known as the ADSP-21061. A key feature of this processor is its low cost, $49 in OEM quantities. It increases MFLOPS performance per dollar while maintaining code and pin compatibility with its more expensive predecessors: the ADSP21060 and ADSP21062.

The new SHARC processor features 1-Mbit of on-chip SRAM, 6 DMA channels and 2 serial ports with 240 Mbit/s capability ( 40 Mbit/s bidirectional). Housed in a 240-pin PQFP package, the unit operates at 5 V. The processor in the ADSP-21061 is the same 32-bit floating point DSP found in the more expensive members of this processor family, and operates at 120 MFLOPS with an instruction execution time of 25 ns. The chip's memory is organized into two banks for both dual operand fetches and independent core and DMA fetches. As a result of dual-ported memory, all I/O can occur in parallel with the core processing unit. The host/external port interfaces with up to 4 gigawords of off-chip memory, other peripherals, other SHARC processors in a cluster and a host processor

A low-cost development kit is available to go along with this inexpensive processor. Dubbed the EZ-KIT Lite, this DSP development systems sells for just $179. It offers both an ADSP-21061-based add-in board and an optimizing ASNSI C compiler, code compactor, linker, loader, instruction-level simulator and runtime library.

### Software Libraries Available

To make these processors suitable for use in videoconferencing, TI has developed assembly language software libraries that allow the processors to implement the ITU H.320 and H.324 videoconferencing standards. TI does not, however, support the H.323 standard because they stopped developing libraries for these processors and assigned the software development team to work on programs for next-generation products. Software libraries are available to third parties, who then make them available to customers who purchase the C8x chips.

Audio coder standards G.722, G.723, and G.728 also are supported in libraries, meaning that the same chip can handle both the audio and video processing. This contrasts with dedicated videoconferencing chip sets that have one chip that handles video, another that does the audio compression, and yet another one that does the echo cancellation.

IAT AG, Vogelsang-Turgi, Switzerland, a European company that is going public soon, will be doing a lot of work with these processors, particularly in the development and maintenance of the software libraries. Another company using the chips is Sony, whose monitor division produces the Mini 1000 desktop videoconferencing system. The C82 also is being used by a Japanese manufacturer of standalone video telephones, and an American telecom company that is coming out with a similar product.

Because the TI chips are programmable, unlike dedicated video processors, they can be programmed to adapt to changing standards. "When we first started," recalls Rinehart, "there was an H.261 video coder and a G.728 audio coder. Later, the G.722 coder was added. Subsequent to that, the standard was modified again to include the H.263 video standard. So the H.320 evolved from a single video, single audio codec standard to one that includes several audio and video standards. As technology improves, the ITU modifies the standard appropriately to take advantage of the better video quality that becomes possible. Because our support for these stan-

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dards is implemented in the assembly language software that runs on our programmable processor, we've been able to accommodate these changes by just upgrading our software modules. There has been no hardware change required at all."

As far as a total software approach to videoconferencing using the computer's own CPU, such as the one supported by Intel, Rinehart notes that the performance you can get from such systems is limited. The Pentium does pretty good at the low picture resolutions it currently supports and the 28,800-bit/s bandwidth that is now commonly available.

"If that's the biggest bandwidth pipe that ever ends up on people's desktops or in their homes, then Intel is going to be very successful," says Rinehart. "But, if you look at what it takes to do H.263 at 15 fps, that's well beyond what Intel is able to deliver with the MMX, and in order to get quality videoconferencing, you will need a coprocessor. That will continue to be true as long as the bandwidth available to us continues to grow."

He points out that the increased use of the Internet and video-on-demand systems coming into the home will foster that bandwidth growth. These higher-frame-rate, higher-resolution applications will require more computing power and increase the demand for video coprocessors.

When designing a videoconferencing system, there are several things

## Standards Are The Key

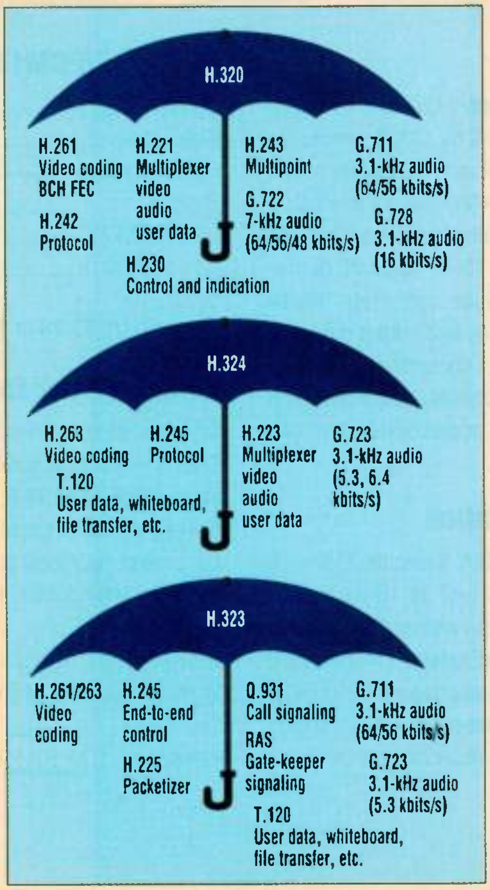
A key issue for today's videoconferencing systems is interoperability. Although there numerous types of videoconferencing systems available, most are incompatible with each other. As videoconferencing becomes more popular, standardization becomes more critical. Recognizing this, the International Telecommunications Union (ITU) has drawn up a set of standards that are platform-independent and will insure that videoconferencing System A will be able to talk to System B.

Just because there's an industry standard doesn't mean that complete compatibility is automatic. The problem is the ITU deliberately writes the standards so they are platform-independent both from a hardware and a software point of view. However, when an individual vendor tries to implement the specification, there's always a chance for ambiguities to crop up.

To illustrate the point, consider describing to two different people how to build a house. Now ask one to build the right side and the other one to build the left. Chances are pretty good that the two halves would not fit together. Until you actually try to fit the pieces together, you don't realize that you didn't get enough information. The same is true of industry standards. Ambiguities always crop up during the implementation phase, and the parties involved have to agree on how to account for them. Once they do, an implementor's specifications have to be written.

The initial videoconferencing standard, H.320, came out in 1992 and deals only with ISDN-based systems. While popular in Europe, ISDN videoconferencing systems have not become as popular or widely available in the U.S *(see the figure)*.

More recently, with the availability of 28.8 kbit/s modems and sophisticated compression techniques, the ITU developed a videoconferencing standard, H.324, designed for regular telephone lines. Approved only last year, the standard will insure that all videoconferencing systems, whether standalone or computer-based, and whether hardware- or software-driven, will be able to talk to each other. The standard specifies a common method for video, voice and data to be shared simultaneously over a single analog line. Voice data is compressed down to 6000 bits/s and assures that the quality will be as good as that on current long-distance calls. The rest of the bandwidth, over 22,000 bits/s, is used by the compressed video. Should any bandwidth problems arise, all efforts are made to maintain the audio connection, and the video data is allowed to suffer the consequences.




Another standard, H.323, deals specifically with LAN-based videoconferencing. This is another area where industry experts see much potential growth. The reason for the expected growth here is that intranets and corporate LANs are growing rapidly, and simple text-based e-mail is being replaced by video e-mail. In addition, as the Internet overcomes its growing pains and becomes a more reliable messaging medium, video e-mail will emerge, and videoconferencing via the Internet will become more popular. And, by having a videoconferencing gateway on an intranet, everyone one on the intranet can get videoconferencing capability.

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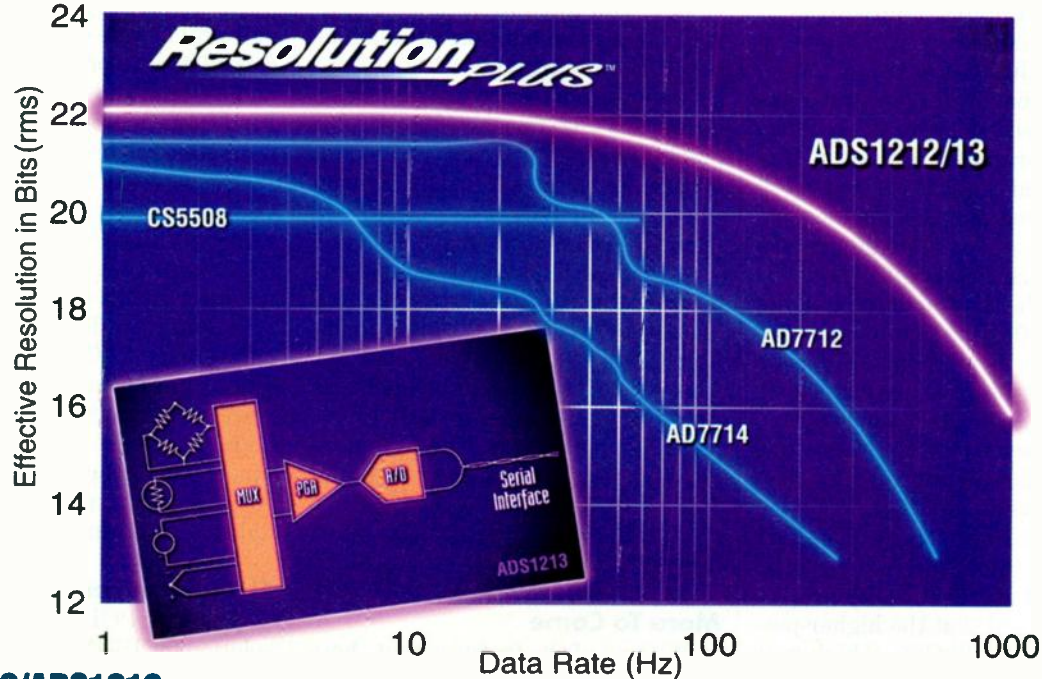


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| Model | INL (%FSR) | DNL (Bits) | Resolution (Bits at 10Hz) | Resolution (Bits at 1kHz) | Power Dissipation (mW) | FAX*LINE*# | Reader Service # |
|---|---|---|---|---|---|---|---|
| ADS1210 | ±0.0015 | No Missing Codes | 24 | 20 | 26 | 11284 | 88 |
| ADS1211 | ±0.0015 | No Missing Codes | 24 | 20 | 26 | 11284 | 89 |
| ADS1212 | ±0.0015 | No Missing Codes | 22 | 16 | 1.4 | 11360 | 90 |
| ADS1213 | ±0.0015 | No Missing Codes | 22 | 16 | 1.4 | 11360 | 91 |

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that engineers must take into account when selecting a chip or chip set to do the job. As mentioned earlier, increasing bandwidth is key. Within three years, predicts Rinehart, we're going to need to support bandwidths of 1.5Mbit/s full duplex, which will give us real TV-quality compressed video. That kind of bandwidth and quality is going to be needed before videoconferencing is embraced by the consumer in a big way, and that can be supported now with a programmable solution.

Rinehart notes that designers should realize that digital cameras are going to be the standard input device. Also, a flexible solution must be used because as we've already seen, standards in this area are constantly changing, and you don't want to have to produce new hardware every time a new modification to the specification is approved.

Cost is another factor. Rinehart says that the $70 cost of the TMS320C82 will eventually drop to around $40, and that the higher-performance TMS320C80, which now costs about $150, also will come down in price. Even at today's prices, the cost of a videoconferencing solution is not high. In fact, in addition to the 4 Mbytes of EDO DRAM required by the H.320 software libraries, you only need five chips to build a videoconferencing system using TI's C8x processor chip: The chip itself, a system control ASIC (FPGA), a video-capture chip, an analog-to-digital converter (ADC), and an ISDN interface. Total chip cost is about $175. One thing to be aware of is that if you decide to use TI's C8x processors, you'll need to license the software libraries. That runs between $50,000 and $100,000.

## Looking Good

When all is said and done, quality is what turns out to be important in a videoconferencing system, and video quality is best when dedicated hardware is used. Bear in mind that there are no objective standards for measuring quality. You can look at resolution and frame rate all you want, but they're tied to the data rate and the blockiness effect. With a 28.8-kbit/s modem, you can get a frame rate of 10 to 12 fps with a little bit of motion. With no motion at all, that rate can jump to 15 fps. That assumes QCIF resolution of 176 by 144 pixels.

If you need to use a higher-resolution image, you're going to have abandon POTS and opt for ISDN as your transmission medium. With ISDN, you get much more bandwidth. For example, you can combine two B channels and get 128 kbits/s. This allows you to increase your resolution to a CIF format of 352 by 288 pixels. That's four times the amount of data. Nevertheless, ISDN can handle that and still give you a solid frame rate of 15 to 20 fps.

If that's still not good enough, and you need something approaching broadcast quality, you can go to 384 kbits/s and get a frame rate of 30 fps. This type of throughput would be required for telemedicine or distance-learning applications. The ITU standards define data rates as high as 2 Mbits/s and the AV4400, the CVP, and the TMS320C8x processors support that data rate.

## More To Come

With all of the features that these videoconferencing chips contain, you might think there'd be little room for improvement. Not so. Although Lucent's Rank would not comment on if his AVP-III chip would be upgraded, when it might happen, or what new features it would contain, he did speculate on some things that may be included in a new version of the chip. These include additional audio processing algorithms such as an acoustic echo cancellation function, support for MPEG-2, support for DVD, and built-in modem capability. He even noted that a CMOS digital camera is now available on a single chip, and it also might be possible to include that.

The comprehensive capabilities of Lucent's AVP-III videoconferencing chip has attracted much attention, and several manufacturers have already announced products that are based on it. Among the first is Boca Research's BocaPRO Video Phone Elite. Designed by Boca with the help of Lucent Technologies and software from MultiMedia Access Corp., the unit has a suggested retail price of $399 and can be used with a home-video camcorder or a desktop color camera that also is available from Boca.

The BocaPRO Video Phone Elite is a PCI-bus-based card that supports connections to the desktop via the ITU H.324 (POTS) specification. It uses a single dial-up line to send simultaneous audio and video. The unit's real-time compression and decompression of audio and video signals provides for a video-frame rate of 15 fps. It uses echo cancellation to produce a high-quality audio signal and can accept NTSC or PAL camera inputs. Even 486-based computers can be used.

The power of the AVP-III chip becomes evident with VIC Hi-Tech Corp.'s Video Packer Pro. This is a codec card that makes it possible to use plain-vanilla 486 PCs for videoconferencing applications. The card comes with VIC's Global Phone 2.0 videoconferencing software. The software also permits application sharing and supports TWAIN scanning of documents and images into a whiteboard for simultaneous viewing during videoconferencing sessions.

## ELSAvision For Windows NT

The first PCI-based, single-board solution for ISDN, videoconferencing, and multimedia for the Windows NT platform is ELSAvision from ELSA, Inc. Using the VCP chip from 8x8 Inc., the ELSAvision board combines H.320 videoconferencing with a 128-kbit/s ISDN adapter, collaborative computing software, and MPEG-1 video playback. One other feature of the board is its ability to transfer high-resolution still images. Detailed still pictures (704 by 575 pixels or four times the CIF resolution) can be sent and saved at the remote station.

While many videoconferencing systems use a 176-by-144- or 352-by-288-pixel image that only takes up a small portion of the video screen, the ELSAvision card goes far beyond that. It can display a 30-fps video conference at the maximum resolution of the user's graphics adapter up to 1600 by 1200 pixels. All of this extra processing power does not come cheap, however; the system sells for $1499. Included in that price is the PCI board that contains the videoconferencing interface, an analog camera, headset, Intel ProShare Premier 2.0 application sharing software, and communications software.

Another product that uses 8x8's VCP chip is produced by 8x8 itself. Known as the ViaTV Phone, this $499

product is designed to be connected to your telephone line and television set and gives you videoconferencing capability without a computer. The unit comes with an integrated video camera that has a resolution of 752 by 480 pixels.

The unit was developed, according to 8x8's Deierling, in an effort to increase the demand for the company's VCP chip. Deierling notes that his chip sells very well in high-end videoconferencing systems, but there's not enough volume there. Hence the push into the consumer market.

## The Software-Only Approach

Not everyone developing videoconferencing systems is using a dedicated processor chip. In fact, few semiconductor manufacturers besides Lucent and 8x8 are offering a complete hardware solution. Even National Semiconductor has developed and is selling software codecs—known as NS Video Codecs—to handle the compression and decompression needed for videoconferencing applications.

Today, most videoconferencing systems use the software-only approach. In fact, the two biggest vendors of videoconferencing systems—PictureTel and Intel—which account for over 80% of the market according to a recent Frost & Sullivan report, use the software approach. PictureTel actually has products that use both the hardware and software approach, but they seem to be putting a lot of effort into software these days. Connectix, a manufacturer of inexpensive video cameras ideal for videoconferencing applications, also uses the software approach, and has just announced an agreement with PictureTel and will soon be releasing a H.324-compatible product.

The attractiveness of software codecs is that they can run on any machine. In addition, there is no need to buy expensive add-on hardware, and installation is quick and easy. You also don't have to open up your computer to install any hardware. Another plus is the ease with which it can be adapted and updated to accommodate new interfaces. Instead of changing hardware, you only have to install a new software driver.

Software-based videoconferencing systems is where much of the action is these days, especially in the consumer market. Many companies are offering software-based products, including Connectix, Creative Labs, and Intel. Low cost is the key attraction of this technology, with packages starting as low as $9.95.

Connectix manufactures inexpensive digital video cameras for use with computers, so it's not surprising that the company would put together a package that would make it easy for a user to implement videoconferencing on his or her computer. Priced at only $49 for just the software or $149 with a black and white Connectix QuickCam digital camera, and $249 with a color QuickCam, the VideoPhone 2.0 package is available for both PC and Macintosh computers. It requires a 28.8-kbit/s modem, an ISDN connection, or a TCP/IP network. User-friendliness is designed into the software and it automatically negotiates call settings. This takes into account the speed of your computer, connection speed, and compression formats available. The program then selects the best frame size, color depth, frame rate, video and audio compression, and bandwidth available.

**When all is said and done, quality is what turns out to be important in a videoconferencing system.**

Performance of this system depends on the type of processor in your computer and how you make your connection to the receiving computer. John Beaver, software developer at Connectix, notes that the system will work well on a computer with a 90- or 100-MHz Pentium processor. However, the company recommends that a 133-MHz Pentium machine be used to take advantage of the more aggressive compression technologies built into the product without having to worry about what else is running on your system.

If you're going to make your videoconferencing connection via the Internet, you can expect to get good audio and see video at the rate of only 1 to 3 fps. By using two computers equipped with DSVD-enabled modems and making a direct-dialed connection between the two computers, performance will jump to between 6 and 8 fps. And, if both computers are connected to each other via a 10BaseT network configured as TCP/IP, performance increases to 8 to 15 fps, depending on network traffic.

Best known for its standard Sound Blaster audio cards, Creative Labs has several entries in the videoconferencing arena. The least expensive of these is Video WebPhone, Personal Version. Priced at $9.95, this full-featured program offers live video and high functionality. Unlike many video-phone services that require users to go to a central server to communicate, this program allows users to simply type in the recipient's e-mail address to make the connection. The program requires a 28.8-kbit/s modem, an ISDN line, a LAN or intranet, and can deliver color video at a rate of 12 fps. Some features of this videoconferencing software include the ability to capture and save video snapshots, full-duplex voice communications, a fully integrated voice-mail system, MIDI music-on-hold capability, mute microphone for off-line conversations, the ability to send message via an on-line Notepad, and encryption to keep conversations private. A more advanced version of the program that can handle four telephone lines with conferencing capabilities is available for $49.95. Still another version of the product, a hardware/software combination, comes bundled with a video camera and sells for $169.

Creative's high-end videoconferencing product is known as ShareVision PC3000 and sells for $699. The package includes a PC communications card, a video-capture and compression card, a high-speed V.34 modem, a hands-free audio headset, and the ShareVision PC3000 software which allows you to collaborate with others via interactive whiteboards and application sharing.

ShareVision uses a Vector Adaptive Transform Processing (VATP) algorithm to compress a user's voice, video image and computer data (in the form of real-time application sharing, interactive whiteboards or file trans-


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fers) to the point where they can be transmitted on the narrow bandwidth of a telephone line. Typical compression ratios are 350:1. The result is a video rate of up to 15 fps.

Although the Intel ProShare Conferencing Video System 200 is hardware/software bundle, the videoconferencing functions that are normally found on dedicated chips is performed in software. The hardware that comes with this $1499 system includes an ISA-bus ISDN card, an Intel Smart Video Recorder Pro motion-video card, a video camera with a tilting stand, and an earpiece. The software implements the H.320-compatible codec so the system is compatible with videoconferencing systems from other manufacturers. The system also features a multipoint control unit that lets you link several colleagues together in a single video conference.

The software provides a lot of functionality, including a video answering machine that delivers a video greeting when you're not available and will record the caller's video message. Extending this concept a bit further, Intel has included a conference-recording machine so you can record important conferences and play them back later.

ProShare also features a multipoint notebook into which document images, spreadsheets, and so on can be imported and marked up with others in the conference. Collaboration is encouraged even more with the software's multipoint application sharing that allows conference participant to take turns editing a shared document directly in the software application it was created in.

For all its power, system requirements for ProShare seem extremely modest. Intel specifies a DX2 processor running at 66 MHz as the minimum CPU needed along with 16 Mbytes of RAM and 45 Mbytes of hard-disk space.

*Jules Gilder is a freelance writer specializing in high-technology subjects including consumer electronics. He may be reached at (718) 259-4752.*

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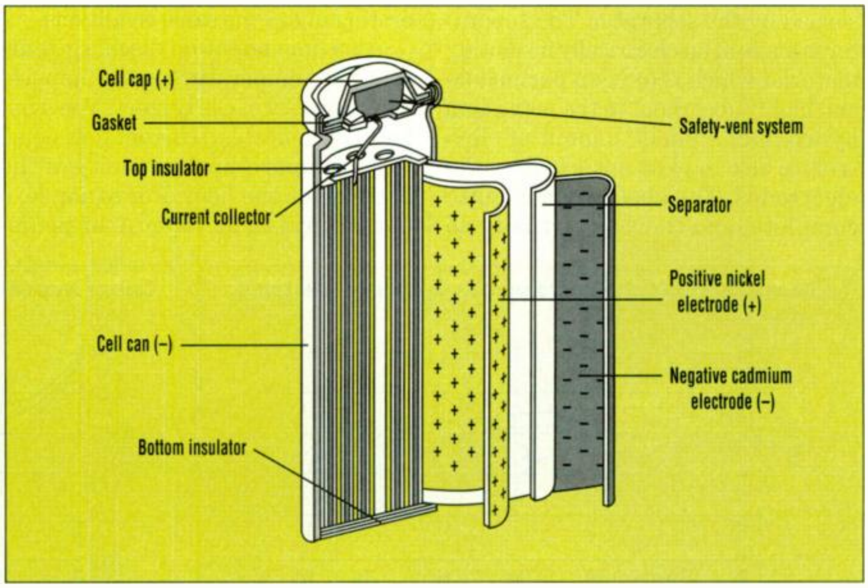
As portable electronic devices proliferate, supplying inexpensive, long-lasting power from an ever-shrinking battery package remains a challenge. While significant advances have come in the form of rechargeable lithium-ion (Li-Ion) and related chemistries, their prohibitive cost has relegated these chemistries to high-end applications where long life is essential. A low-cost alternative is the tried-and-true nickel-cadmium (NiCd) battery which, despite its carcinogenic content, remains very popular in the highly competitive consumer market where cost is everything. This end of the market is so competitive that nickel-metal hydride (NiMH) batteries, which come at a reasonable cost premium, are finding it difficult to gain a foothold despite their "green" status.

Along with cost, a common perception that there is a considerable technological difference between NiCd and the relatively new NiMH batteries, is contributing to the slow penetration of NiMH. While there are some differences, mostly with respect to charging, the two chemistries are in fact, quite similar.




**1. The primary difference between NiCd and NiMH batteries lies in the chemical make-up of the negative electrode. Where cadmium is used in the NiCd cell, hydrogen, in the form of a metal hydride, is used in the NiMH cell to give it greater capacity.**

## Structure

All batteries are made of one or more electrochemical units called cells. The cells may be connected in series, in parallel, or both to form a battery of a given voltage and capacity. The cell consists of three major components; the anode, the cathode, and the electrolyte, (*Fig. 1*). The anode is the negative electrode, and is referred to as the reducing or fuel electrode. It supplies electrons to the load (external circuit being powered) as it is reduced during operation. The cathode is the positive electrode, and is referred to as the oxidizing electrode. It accepts electrons from the load and is oxidized during operation. The electrolyte is an ionic conductor. Electrons, as ions, are transferred between the anode and cathode via the electrolyte.

The primary difference between NiCd and NiMH batteries lies in the chemical make-up of the negative electrode. Where cadmium is used in the NiCd cell, hydrogen is used in the NiMH cell. In both cases, the negative electrodes are made using a highly porous, sintered-nickel structure as the substrate. The active material (cadmium for the NiCd, hydrogen in the form of a metal hydride for the NiMH) is then introduced into the substrate by an appropriate bonding process. The use of hydrogen in fabricating the negative electrode provides a higher energy density than can be obtained using cadmium. Consequently, the negative electrode can take up less volume in the NiMH cell, leaving room for a larger-volume positive electrode for greater battery capacity for a given battery size.

Everything else is essentially the same for both electrochemistries. The positive electrode is made by using a porous, sintered-nickel substrate which is subjected to a multistep process resulting in the precipitation of nickel hydroxide as the active material. A solution of potassium hydroxide serves as the electrolyte. Though the electrolyte is an aqueous solution, a minimum amount is used, and it is absorbed by the separator. The separator is made of an electrically insulating material which is oxygen permeable and highly absorbent to the potassium hydroxide. A small amount of electrolyte also may be absorbed by the electrodes. The absorption is quite complete, and there is virtually no free-liquid electrolyte in the cell. The oxygen permeability of the separator is important in facilitating the diffusion of oxygen to the negative electrode for oxygen-recombination at the end of charge and during overcharge.

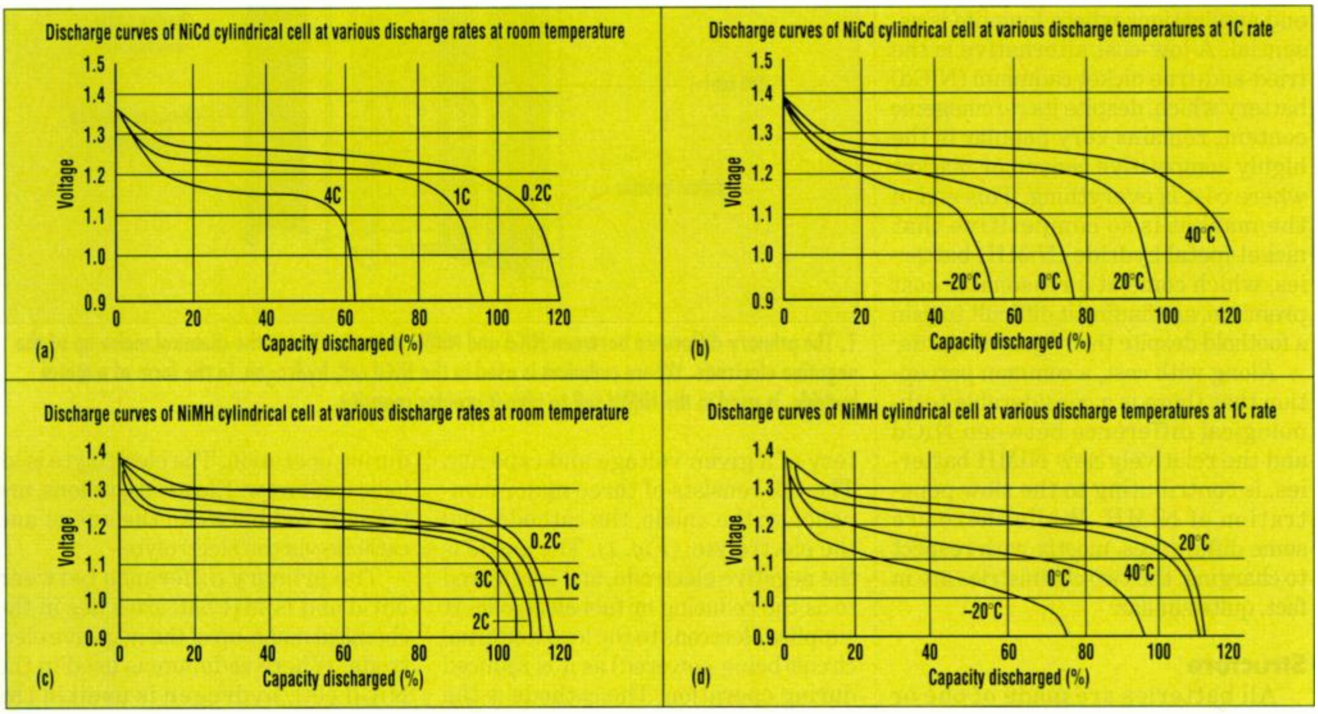
## Performance

As might be expected of two such similar electrochemistries, the discharge characteristics are essentially the same, for NiCd (*Figs. 2a and 2b)* and for NiMH (*Figs. 2c and 2d)*. Both types are characterized by a flat discharge profile with a discharge voltage that is dependent on current and/or temperature. Generally, the higher the current or the lower the temperature, the lower the operating voltage. This correlation is due to the internal resistance increasing with increasing current and lower temperatures. Even so, these batteries outperform most other types of portable secondary (and primary) batteries operating under the same conditions.

Also dependent on discharge current and temperature is the ampere-hour capacity of the battery. The symbol "1C" indicates a current flow equal to the ampere-hour capacity of the battery for one hour. For example, a battery rated at 700 mA-hr is discharging (or charging) at a rate of 1C when 700 mA of current flows through the battery. A rate of C/10 (or 0.1C) would be 1/10 the capacity. Typically, the best performance range for NiCd is between -20° and 30°C. NiMH does the best from 0° to 40°C. Again, as discharge rate increases or temperature decreases, the capacity decreases. Specially designed cells are available for operation in extreme temperature or load conditions.

The ampere-hour capacity also is dependent on end voltage. End voltage or cut-off voltage is the voltage at which discharge current to a load is stopped, e.g. when the circuit is opened. Most battery manufacturers recommend an end voltage of one volt per cell. The cells can be discharged to a lower voltage, but this is not recommended because damage to individual cells can result.

As might be expected, service life also is affected by operating conditions. Most manufacturers specify a service life of about 500 to 1000 charge/discharge cycles, depending on operating conditions. The service life will decrease under more demanding operating conditions. Storage also is a factor. Batteries should be stored in a cool (20° to 30°C), dry place. High tem-




**2. As might be expected of two such similar electrochemistries, the discharge characteristics of NiCd (a and b) and NiMH (c and d) batteries are essentially the same. Both types are characterized by a flat discharge profile, with a discharge voltage that is dependent on current and/or temperature. Generally, the higher the current or the lower the temperature, the lower the operating voltage.**

peratures during storage, charging, or operation can shorten service life.

A truly accurate prediction of battery life is virtually impossible due to the variability in conditions to which the battery can be exposed. These conditions include rate of charge, overcharge, and discharge; cycle frequency; operating and charging temperatures; battery age; cell components; and design.

## Polarity Reversal

Polarity reversal can occur in battery packs containing three or more cells connected in series. It is unlikely that all of the cells making up a battery pack will have the same capacity, so as the pack discharges, the lowest-capacity cell will reach full discharge first. If discharge continues beyond this point, the cell can be driven into a reversed-polarity condition.

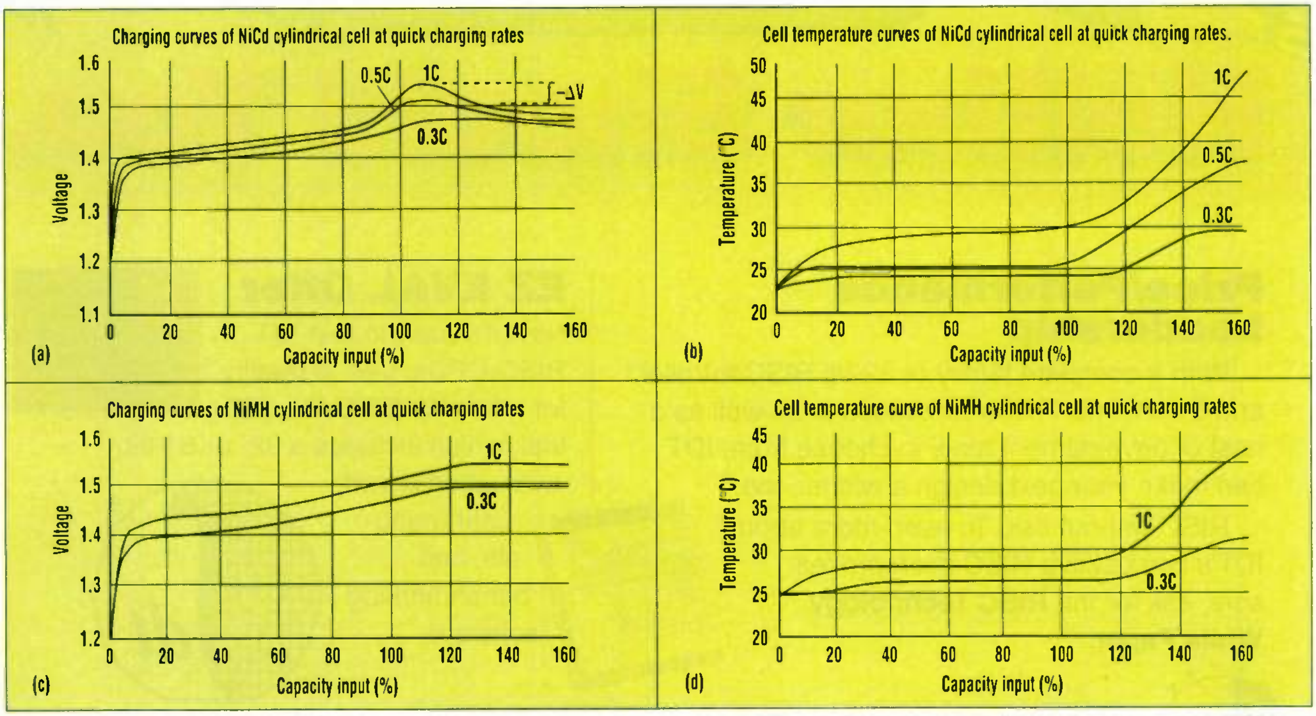
The polarity reversal occurs in stages beginning with complete depletion of the positive electrode, which starts the generation of hydrogen gas within the cell. A small amount of the gas may be absorbed by the negative electrode, but then pressure begins to build in the cell. Next, the negative electrode reaches complete discharge and begins to generate oxygen. The internal cell pressure continues to build until the safety vent opens and deterioration results.

Cell-capacity matching can help minimize the effect, but the best way to avoid it is to set a one-volt-per-cell cutoff voltage for battery packs containing 3 to 10 series-connected cells. A higher cutoff voltage is recommended for batteries containing more than 10 cells in series, or for discharge rates exceeding 1C.

## Charging

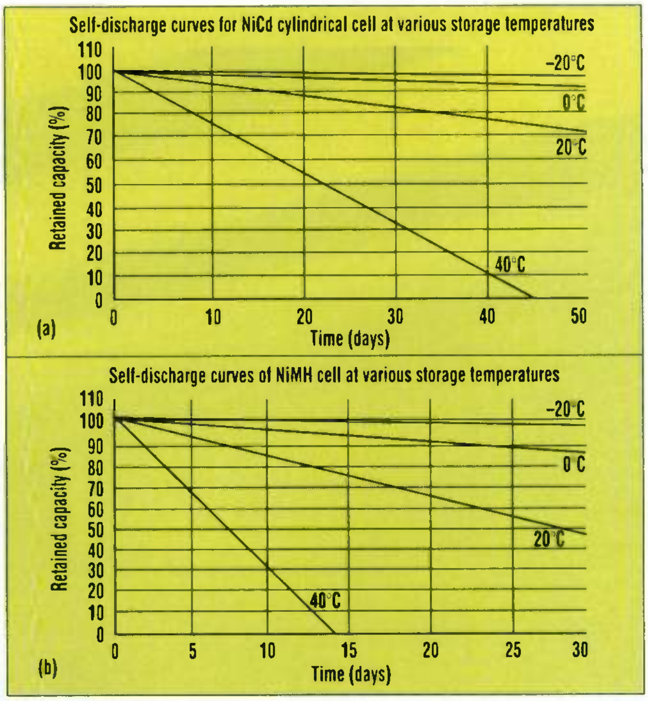
Charging a sealed NiMH battery is very similar to charging a sealed NiCd battery (*Figs. 3a, 3b, 3c, and 3d*). Constant current charging is recommended for both systems and the highest capacity is attained by charging to about 150% of the charge input. Excessive heat or internal pressure build up (overcharge beyond the oxygen recombination ability) must be avoided in both cases. Nevertheless, from an application standpoint, charging methodology is perhaps the most critical difference between NiCd and NiMH batteries.

As mentioned previously, the NiCd electrochemistry is considerably more tolerant of overcharge than NiMH. The reasons involve increases in temperature and pressure inside the cell during charging and overcharge. The charge reaction of NiCd is endothermic while that of NiMH is exothermic. Therefore, the NiCd cell will not heat up during charge, but will begin to heat as it reaches full charge and goes into overcharge. The NiMH cell will begin generating heat as soon as charging begins. The overcharge reaction is exothermic for both electrochemistries. As full charge is approached and as the cell moves into overcharge, a significant increase in cell temperature will occur. Because the NiMH cell temperature starts rising at the beginning of charge, its temperature will be higher than that of the NiCd cell at this point. Continued overcharge, even at the standard rate of C/10, will be accompanied by continued temperature rise in the NiMH cell, and damage will occur. The temperature of the NiCd cell, on the other hand, will stabilize while overcharge at the C/10 rate continues, and no damage will occur. In fact, it's best for both battery types to terminate charging at any rate exceeding C/20, once 150% charge input is reached.




**3. From an application standpoint, charging methodology is perhaps the most critical difference between NiCd and NiMH batteries—with NiCd (a and b) being considerably more tolerant of overcharge than NiMH (c and d). Constant-current charging is recommended for both types, and the highest capacity is attained by charging to about 150% of charge input. Excessive heat or internal pressure build up (overcharge beyond the oxygen recombination ability) must be avoided in both cases.**

The charge-input percentage is a measure of the amount of input current (charge current) to the battery over time, relevant to the specified battery capacity. For example, a 1.2-A-h battery charging at a rate of C/10 (120 mA) would reach 150% charge input in 15 hours. A charge rate of C/20 to C/40, considered a maintenance charge, can be continued indefinitely. Also referred to as trickle charging, the low rates are intended to compensate for the self-discharge of the battery, although they're typically only about 1% of capacity per day for both types.




**4. NiCd (a) and NiMH (b) batteries can be stored in either a charged or discharged state. Both types are considered to have poor charge retention during storage, with the rate of discharge depending on cell design and storage temperature. The discharge mechanisms include a slow decomposition of the electrodes. The condition is reversible by subsequent charging, and has no permanent effect on battery capacity.**

Another consideration and potential problem is gassing. As the cell begins to overcharge, the positive electrode starts to generate oxygen gas. The negative electrode recombines the oxygen gas which keeps the internal pressure from building to a damaging level. Of course, there is a limit to this ability which, in turn, sets the maximum overcharge rate that can be tolerated. The charge rate must be below that which causes oxygen gas generation to exceed the gas recombination rate. The maximum charge rate will be lower at lower temperatures because the oxygen recombination is slowed down, causing the internal pressure to build faster for a given charge rate at lower temperatures. In any case, if the internal pressure becomes too great, a built-in safety vent will open to vent the gas. A loss of electrolyte will ensue, causing a reduction in the capacity and overall performance of the cell. One manufacturer of battery-charge controller ICs has a patented process by which the battery is "burped" periodically during fast charge to relieve the build up of internal gasses.

Fast charging is typically done at rates of 0.5C to 1C. Some special techniques may allow even higher rates. NiMH is generally more suited to fast charging although specially designed fast-charge NiCd batteries are available. Very careful and precise control must be exercised at these high charge rates. The most challenging aspect of fast charging is in terminating the charge before too much overcharge occurs. Several methods are in use, and often more than one is employed to ensure success.

Probably the most popular termination method for fast charging NiCd batteries is negative delta voltage detection (-ΔV). When a NiCd battery is charged at high rates, a characteristically sharp rise in cell voltage occurs just as the cell reaches about 100% charge input. The voltage peaks at about 120% to 125% charge input, then begins to fall off. The decreasing voltage (-ΔV) is taken as an indicator of full charge and can be used to trigger either a complete shut off or a reduction in charge current.

This method is less suitable for fast-charge termination of NiMH batteries because the voltage swing is much less pronounced, therefore more difficult to detect. The method is, however, used with NiMH, but virtually always in combination with one or more other termination methods. Charge rates below C/2 do not produce a readily detectable -ΔV, even in NiCd batteries.

A slightly less risky method used for NiMH fast-charge termination is zero ΔV detection. Rather than waiting for a drop in voltage, the charge is terminated when the voltage has peaked and is holding steady.

The preferred charge termination method for NiMH is delta temperature/delta time (ΔT/Δt). The temperature rise is monitored and timed. The charge is terminated when a predetermined incremental temperature rise is detected. This method is not significantly influenced by ambient temperature and provides long cycle life.

Delta temperature cutoff minimizes the influence of ambient temperature by using it as a reference. The charge is terminated when a rise in cell temperature, above the ambient temperature, exceeds a predetermined value. This method requires a specific cutoff value for each type of battery which is determined by the size and number of cells used, their configuration, and the battery's heat capacity.

Charge termination based only on a fixed cell-temperature value (temperature cutoff) is easily rendered inaccurate by the influence of ambient temperature, and can lead to overcharge or undercharge by causing late or early charge cutoff. Such a method may be used to back up other termination schemes, but should never be used as a primary method. Timed charging is sometimes used for low charge rates or topping charges. A topping charge may be applied immediately after the termination of a fast charge to ensure a complete charge. Timed charging is not used as a primary termination method for fast charging because the charge state of the battery, before charging, is not always known.

Many battery manufactures recommend a three-step charging method. The first step is a fast charge, typically at the 1C rate and terminated by the -ΔV or ΔT/Δt termination method. Then the topping charge is applied at the C/10 rate and terminated by a

timer after 30 minutes to 1 hour. The final step is a maintenance charge at a rate between C/20 and C/50. The maintenance charge may be of indefinite duration.

It is considered good practice to employ a thermal cutoff device to protect the battery from heat damage by opening the circuit if the battery temperature exceeds about 60°C. Some designs for this incorporate a thermal switch in the battery pack itself where it can best detect the battery temperature, protecting the battery from overheating.

## Storage

NiCd and NiMH batteries can be stored in either a charged or discharged state. Both types are considered to have poor charge retention during storage, with the rate of discharge depending on cell design and storage temperature (*Figs. 4a and 4b*). The mechanisms include, among other things, a slow decomposition of the electrodes. The condition is reversible by subsequent charging, and has no permanent effect on battery capacity. Long storage periods (i.e. over one year), may result in significant self-discharge and an increase in internal resistance. In this case, the battery should be cycled (charged and discharged) two or three times to restore full capacity.

Longer storage times or higher storage temperatures may require more cycles for full recovery. Except for specially designed cells, storage at temperatures above 30°C should be avoided, because permanent damage due to seal and separator deterioration can result. As mentioned above, storage temperatures should remain in the range of 20° to 30°C.

## Memory Effect

This term is mostly associated with NiCd batteries, because NiMHs are less prone to the effect, although it can appear in both battery types under certain conditions. Memory effect, technically known as voltage depression, describes a condition of apparent low capacity due to repetitive cycles of shallow discharge and recharge. That is, the battery is only partially discharged, to about the same degree each time, and then recharged. Upon subsequent attempts at full discharge, the output voltage steps down to a lower value for the latter portion of the discharge period.

The battery seems to remember the lower capacity defined by the shallow cycles and does not deliver full capacity all the way out to the original cutoff voltage. The drop in discharge voltage occurs because the active materials inside the cell that are not included in the shallow discharge-charge cycling undergo a change in physical characteristics, increasing resistance. The effect is most pronounced when the discharge termination occurs at higher-end voltages (i.e. 1.2 V per cell), and is accelerated by operation at higher temperatures.

The discharge rate also is a factor. At higher discharge rates, the depth of discharge is less for a given end voltage—less of the active material is cycled, causing a greater loss in capacity. Improvements in battery technology and charging techniques have kept this problem to a minimum. This has given some manufacturers of both NiCd and NiMH batteries the confidence to now claim that their products display "no memory effect."

Although chemistry is said to be a much slower-moving science than electronics, battery technology constantly improves. The parameter limits stated or implied in this article are generalized. Battery manufacturers take advantage of subtleties in electrochemistries and tweak their products to enhance certain features or to suit specific applications. Don't be surprised to find batteries with performance and specifications that exceed those discussed here.

*Stephen R. Wood is a Senior New Product Development Engineer for TelAlert, Covington, GA.*

References:


Various published technical literature and specifications from GP Battery Marketing Inc.

D. Linden, *Handbook of Batteries*, second edition, McGraw-Hill: New York, NY, 1995.


| HOW VALUABLE | CIRCLE |
|---|---|
| HIGHLY | 528 |
| MODERATELY | 529 |
| SLIGHTLY | 530 |

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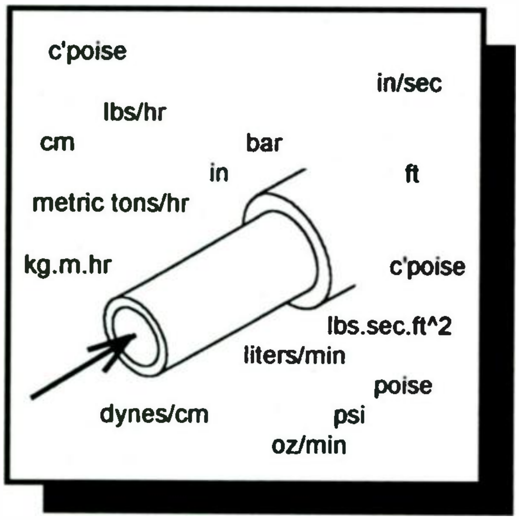
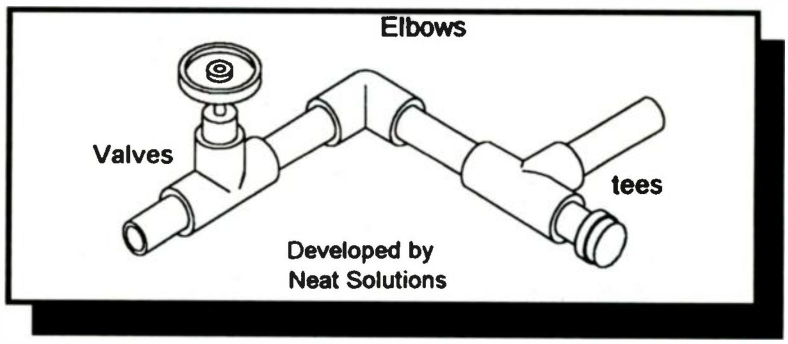



FLUIDTOOLS solves liquid and gas flow problems including escaping gas problems. It can solve for diameter, length, flow rate, pressure, or viscosity when doing liquids. Gas problems solve for quantity and DPSI.

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# Smart Battery Standards Simplify Portable System Design

*Due To Their Ability To Normalize The Interfaces Between Batteries And Their Host Systems, SBS And SMBus Have Quickly Become De Facto Standards.*

**DALE STOLITZKA,** National Semiconductor Corp., Analog Products Division, 2900 Semiconductor Dr., Santa Clara, CA 95052-8090; (800)-272-9959; http://www.national.com.

The continuing boom in portable electronics is largely dependent upon the growing sophistication of portable energy sources and the circuits that manage their usage. Today's battery-management circuits are designed to optimize battery-charging functions and routinely report back to the user on the battery status. When these management circuits are packaged with the batteries in an integrated energy pack, the combination becomes an intelligent battery.

The intelligent battery communicates with the host computer and provides fuel-gauging and charge-control capability. These batteries monitor the environment and the operating conditions, calculate the state of the battery's charge, and communicate with the host through a simple interface.

Industry-wide standards for smart battery designs, with particular reference to the host-to-battery interface, have become necessary to ensure cost-efficiency, to improve design integrity, and to streamline the system designer's tasks. After a period of standards development and refinement, the leading standard which has emerged is the Smart Battery System (SBS). Its associated communications standard is the SMBus.

Ownership of the SBS is in the hands of a broad-based Core Group, including Duracell, Energizer, Toshiba, Varta, Intel, Benchmarq, Linear Technology, Maxim, Mitsubishi, and National Semiconductor. SBS was developed by Intel and Duracell.

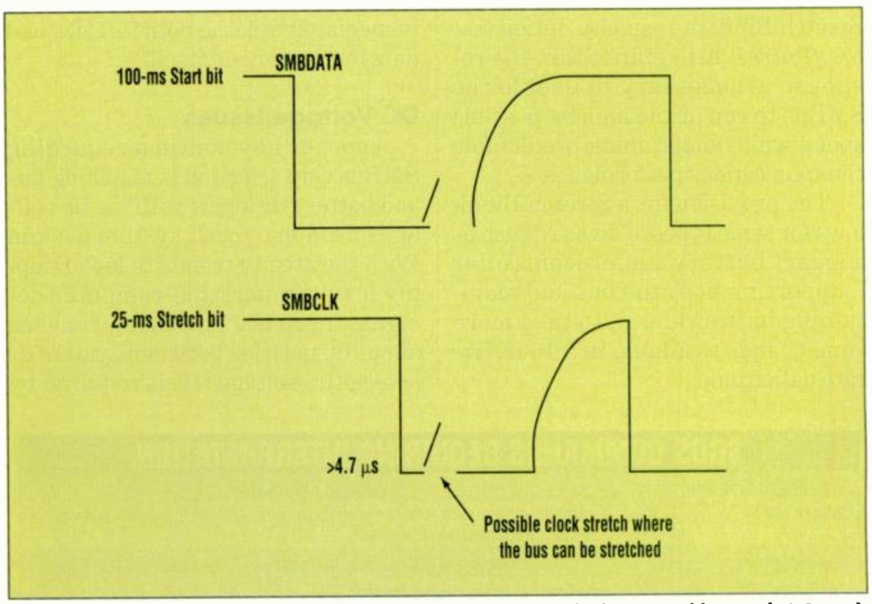
Under the guidance of the SBS Core Group, SBS and SMBus have become the de facto smart-battery standards. The newly established SBS Implementers Forum is actively soliciting industry participation to ensure that future versions of SMBus will address needed improvements such as simplified addressing of multiple batteries, the addition of error management and opportunities for cost reduction.

## Smart Battery Features

In multiple-battery systems, the host needs some type of mechanism to discern between separate batteries. However, the SMBus architecture currently only has provisions for a single-battery address, rigidly assigning the hexadecimal address 16H to any smart battery in the system. Today's system architectures, therefore, require an additional hardware mechanism called a battery selector, which the host must set to communicate with or charge each specific battery. Because the SMBus specification already has two data bits in reserve for expansion purposes, these are being considered for use to allow designers to have direct addressing of multiple batteries in a system.

Error management on the SMBus is another key improvement. Noise on the bus is already a concern and will grow significantly with the advent of more powerful batteries and power switching among batteries and other systems on the bus. The use of error detection and management methods, such as parity checking or cyclic redundancy check (CRC) to maintain data integrity will become imperative with the next generation of Smart-Battery notebooks.

The Implementers Forum also may consider how a battery can operate in a master-only host system where sys-




**1. Adequate Start-bit response enables the SMBus to run at the highest possible speed. A Stretch bit allows for some devices, such as a smart-battery's microcontroller, to take more time than is available in a 100-kHz-rate data frame.**

tem peripherals, including the battery, are only slaves rather than masters and slaves. The hardware cost in this design choice is less because each node does not need to be a master (50% less logic). However, the downside is more host overhead for polling the bus to determine the status and requirements of each node. This option will likely be an architectural choice structured to be compatible with existing master/slave Smart Batteries.

As with many standards, there remain a number of key issues that system designers should keep in mind when selecting chip sets to implement their smart battery systems. These include command set variations, ac-timing issues, and dc-voltage issues.

Although support of the smart battery Data Specification (SBDS) is a basic requirement for any selected chip set, not all implementations are exactly alike. Some may not even support the full SBDS command set, focusing upon only the key commands and gracefully ignoring others. In addition, there are certain basic commands that may require some level of interpretation, depending upon the chip set and/or battery *(see the table)*.

### AC Timing Issues

Two key considerations with regard to an SMBus chip set's ac characteristics are the ability to respond to the SMBus 100-kbps Start Bit and the capability for taking advantage of the Stretch Bit data-response option *(see the figure)*. Adequate Start Bit response is necessary to enable the SMBus to run at the highest possible speed while maintaining predictable communications performance.

The provision for a Stretch Bit allows for some types of devices, such as a smart battery's microcontroller (supporting both the bus and maintaining battery data), to take more time than is available in a 100KHz-rate data frame.

**The intelligent battery communicates with the host computer and provides fuel-gauging and charge-control capability .**

The Stretch Bit allows the SMBus chip set to hold down the bus clock for a specified period of time before responding to a data request. In the case of a smart battery, this can be very useful in providing time for the microcontroller to fetch battery status data from data memory and deliver it to the bus, all within a single, stretched clock cycle. Depending upon the hardware chip design, such a multistep operation might take as much as 100 ms, however the SMBus specification does not allow for Stretch Bits of longer than 25 ms.

Unless the SMBus chip set and microcontroller are rigidly designed and selected to meet the 25-ms requirement, the integrity of the data response and the predictability of the bus can be negatively impacted. Therefore, the SMBus specification requires that a slave device, which exceeds the 25-ms requirement, must immediately release both its clock and data lines and reset itself.

### DC Voltage Issues

Another key concern regarding SMBus chip selection is matching bus and battery dc levels with the dc voltages used in overall system design. With the steady trends to lower supply levels in portable-computer designs, there is an evolving concern about disparities between system dc levels, the voltage levels required by the SMBus specification, and the smart battery's internal voltages. Most logic systems assume that all chips communicating within a common system will be operating at the same $V_{CC}$ levels, however with a smart battery system, such as assumption is typically not the case. The battery's chips are getting their supply locally regulated and the BIOS chip on the host side is receiving its power from the host.

For instance, with emerging new 2.5-V logic devices, the host's BIOS chip may only be able to drive to its maximum $V_{CC}$ of 2.5 V, with the actual output voltage ranging somewherebetween 2- and 2.4- V. Since the SMBus specification requires that an input level for a high should be at least 1.4 V, it will recognize the BIOS chip output as a logical high.

However, most silicon devices in smart batteries are looking for logical highs that are a percentage of their voltage levels (typically at 3 or 5 V). A 3-V device would be looking for 70% of its supply voltage, or at least 2.1 V to recognize as a logical high. Obviously, this inconsistency could lead to misinterpreted logical highs and a resultant degradation of data accuracy and integrity.

While overall system designers can temporarily get around this problem by continuing to use 3- and 5-V logic, in the long run the responsibility is on the semiconductor manufacturer and the battery system designer to ensure that the smart battery silicon can consistently recognize the 1.4-V logical high levels used in SMBus.

More information on SBS and SMBus can be obtained from the SBS specifications home page website at http://www.mediacity.com/~sbs/.

*Dale Stolitzka is the senior systems design manager for the Analog Division at National Semiconductor. He graduated from Cornell University with M.S. and B.S. degrees in applied physics with concentrations in electrical engineering.*

**SBDS COMMANDS REQUIRING INTERPRETATION**

| SBDS Command | Area of Concern |
|---|---|
| Battery Mode | Calibration bit is different between batteries. All bits in this command are not supported by all vendors. |
| Alarm Warning | Broadcast frequency varies from 10 s to over 60 s between vendors. |
| Max Error | Is it fixed at 2% or truly meaningful? |
| Battery Status | Are error warnings supported? What does initialized mean, and when is it set or clear? |
| Device Chemistry | Types must be in text, only some chemistries are specified. |

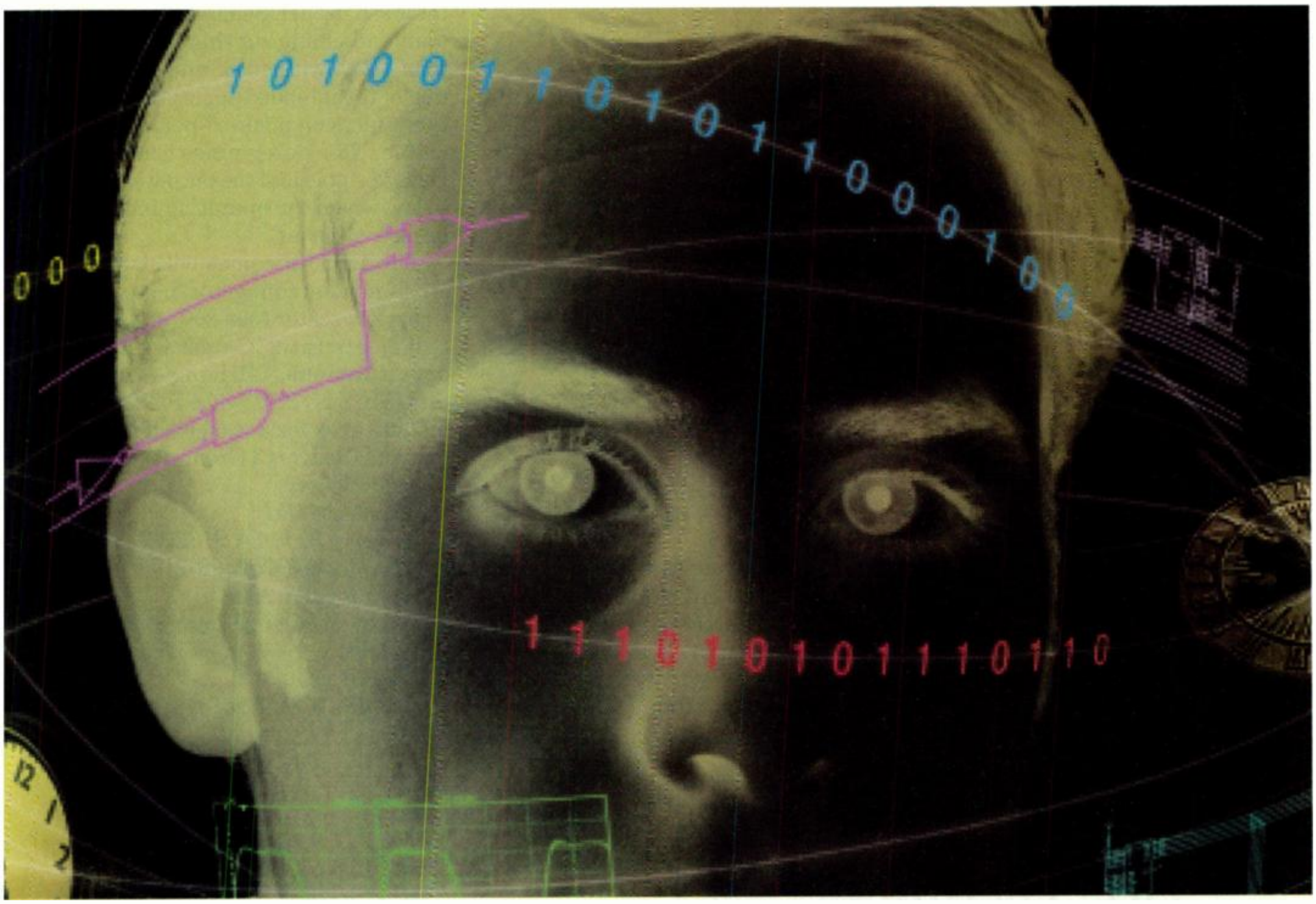
| HOW VALUABLE | CIRCLE |
|---|---|
| HIGHLY | 545 |
| MODERATELY | 546 |
| SLIGHTLY | 547 |

RECHARGEABLE BATTERIES

## MANUFACTURERS OF RECHARGEABLE BATTERIES

| Manufacturer | Available chemistries | Standard sizes available | Custom options | Output voltage range | Maximum energy density | Charge retention | Charge/ recharge cycles | Charge time | Operating temperature range |
|---|---|---|---|---|---|---|---|---|---|
| Bolder Technologies Corp.<br>Wheat Ridge, CO<br>Ann Johnson<br>(303) 422-8200 ext. 556<br>fax (303) 422-8180<br>e-mail: ann.johnson@boldertmf.com<br>CIRCLE 494 | Lead acid | 9/5 subC | Not at this time | Nominal 2.1 V | 28 Wh/kg; 68 Wh/L | Charge loss of about 0.2% per day | Over 500 | Less than 15 min | TBD |
| Eagle Picher Industries<br>Seneca, MO<br>Earl Anderson (417) 776-2256<br>fax (417) 776-2257<br>CIRCLE 495 | Lead acid | 0.5 to 60 Ah | Yes | 2 to 24 V | 37.5 Wh/kg | 97% per month | Over 200 | 16 to 24 hrs | -50° to 74°C |
| Energizer Power Systems<br>Gainesville, FL<br>Energizer Fulfillment Service<br>(800) 57-POWER<br>http://www.energizer.com<br>CIRCLE 496 | NiCd | AA, AAA, Cs, 18650 | Yes | 1.2 V | 150 Wh/L; 50 Wh/kg | 1% loss per day | 500 | 15 min (minimum) | -20° to 70°C |
| | NiMH | | | 1.2 V | 200 Wh/L; 60 Wh/kg | 1% loss per day | 500 | 1 hr | -20° to 50°C |
| | Li-Ion | | | 3.6 V | 300 Wh/L; 120 Wh/kg | 0.3% loss per day | 500 | 1 to 2 hrs | -20° to 60°C |
| Hawker Energy Products Inc.<br>Warrensburg, MO<br>Kalyan Jana (800) 964-2837<br>fax (800) 283-2948<br>e-mail: info@hepi.com<br>CIRCLE 497 | Sealed lead acid | 2.5 to 40 Ah | Yes | Any multiple of 2 V | Over 35 Wh/kg | Less than 19% discharge per week | 400 (full DOD) | Less than 1 hr | -65° to 65°C |
| Maxell Corporation of America<br>Fairlawn, NJ<br>(201) 794-5900<br>fax (201) 796-8790<br>CIRCLE 498 | Li-Ion, NiMH, Li-$MNO_2$ | NiMH=AAA, Lithium= 18650, 17650, 14650 | No | 1.2 to 3.6 V | - | - | - | - | - |
| Plainview Batteries Inc.<br>Plainview, NY<br>Bernie Erde (800) 642-2354<br>fax (800) 249-2876<br>CIRCLE 499 | NiCd, NiMH | Range of button and prismatic cells | No | Nominal 1.2 V | N/A | NiCd retains 50% over 1 yr; NiMH retains 70% over 1 yr | 500 to 1000 | NiCd, 12 hr; NiMH prismatic, 1 hr | Charge: 0° to 55°C; Discharge: -20° to 55°C |
| Portable Energy Products Inc.<br>Scotts Valley, CA<br>Darrell Musick (408) 439-5104<br>fax (408) 439-5118<br>e-mail: darrell.pep@aol.com<br>http://www.portable-energy.com<br>CIRCLE 500 | Sealed lead | 2 to 5 Ah | Yes | 2 V per cell | 106 Wh/L | Loses 2% to 3% per month on shelf | 200 to 2000 depending on DOD (average is 500) | 8 to 10 hrs | -20° to 50°C |
| Rayovac Corp.<br>Madison, WI<br>DeAnne Boegli (608) 275-4414<br>fax (608) 275-4577<br>e-mail: boegli@rayovac.com<br>http://www.rayovac.com<br>CIRCLE 501 | Alkaline | AAA, AA, C, D | No | 1.5 V | - | - | 25 | - | - |
| TNR Technical Inc.<br>Sanford, FL<br>(800) 346-0601<br>fax (407) 321-3208<br>e-mail: tnrbattery@aol.com<br>http://www.batterystore.com<br>CIRCLE 502 | NiCd, NiMH, sealed lead acid | 50 mAh to 10 Ah | 1/3 AAA to Super F | 1.25 to 3.6 V | - | - | 500 to 1000 | 1 to 12 to 14 hrs | - |
| Ultralife Batteries Inc.<br>Newark, NY<br>Greg Smith (201) 930-4900<br>fax (201) 930-1144<br>e-mail: ubigreg@aol.com<br>http://www.ulbi.com<br>CIRCLE 503 | Li-Ion | Call company | Yes | 4.2 to 3.4 V | 125 Wh/kg; 250 Wh/L | Over 90% per month (ie: batteries lose less than 10% of charge per month) | Over 500 | 1 hr | -20° to 60°C |
| Eagle-Picher, Technologies Div.<br>Joplin, MO<br>Bob Cottingham (417) 623-8000<br>fax (417) 781-1910<br>bcott@epi.tech.com<br>http://www.epi-tech.com<br>CIRCLE 512 | NiCd | 2 to 100 Ah | Yes | 1.2 V | 91 hrs/L | 80% after 30 days | Over 40,000 | 1 hr | -40° to 75°C |
| | Li-Ion | 300 mAh to 10 Ah | Yes | 3.6 V nominal | 123 Wh/kg | 10% or less/month | 1500 | 2.5 hrs | -18° to 45°C |
| | Zn-Air | 5 to 150 Ah | Yes | 1.4 V | 88 to 220 Wh/kg | 36 hr activated or 5 yr dry | 50 to 125 | - | -2.9° to 50°C |
| | Lead acid | 0.5 to 60 Ah | Yes | 2, 4, 6, and 12 V | 37.5 Wh/kg | 97% per month | Over 200 | 16 to 24 hrs | -50° to 74°C |

# What you need is a logic analyzer that can manage time.



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Dealing with the pressures of today's deadlines means having to get things done yesterday. And the fastest, most accurate way to debug your designs is with the TLA 700 Series logic analyzer. We've combined microprocessor trace with 500-picosecond timing through the same probes simultaneously, as well as 500-picosecond resolution across all channels and an optional 5GS/s DSO. No logic analyzer is better or easier to use for identifying elusive hardware/software problems. Test Drive a TLA 700 logic analyzer and decide for yourself. Call 1-800-426-2200, when prompted press 3, and request code 3004 today, or visit us at www.tek.com/mbd/tla700

## For a Test Drive, contact:

AT&T Capital; Continental Resources; Electro Rent Corp.; GE Capital; McGrath Rent Corp.; Telogy.

**Tektronix**

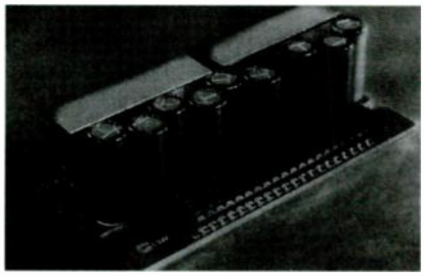
PRODUCT FEATURE

Data sheets on products like these can be found at www.penton.com/ed/

# IC And Power Module Designed To Drive Intel's Klamath Processor

Designed to Intel's voltage-regulator-module (VRM) specification for Klamath motherboards, the MP60-F VRM is the second in a family of next-generation modules from Semtech Corp. to target such high-end microprocessors. Previous modules catered to the Pentium Pro, P54C, and P55. The module is rated for 14.5 A and includes a 5-bit programmable output voltage ranging from 2.0 to 3.5 V in 100-mV increments, and from 1.8 to 2.05 V in 50-mV increments.

Offered as a quick solution for improved time to market, the module uses the company's SC1151 standard buck voltage-mode controller, which comes with a 5-bit digital-to-analog converter, a power-good signal, and shutdown, overvoltage, and overcurrent protection. The controller is able to regulate the output voltage to within 1% of the programmed value, operates at a fixed frequency of 100 kHz, and has an efficiency of 85%. The remaining silicon (MOSFET and Schottky diode) needed to produce the power supply are placed externally on the MP60-F module.



Also contained on the module are a series of low-ESR electrolytic capacitors, giving a total capacitance of 7000 µF. By keeping the ESR below 10 mΩ, the leading-edge transient is kept to less than 120 mV for a 12-A load transient—well within Intel specifications.

The buck converter's output inductor is set at 4 µH. Semtech doesn't recommend changing this value more than ± 25% without careful consideration of the intended application due to the effects on peak-to-peak current ripple. This determines the output voltage ripple and the output current, below which the operating mode will be discontinuous.

The MP60-F comes with a 40-pin VRM header connector, has an efficiency of greater than 80% at full load, and meets Intel Klamath VRM 8.1 specifications. Pricing for the SC1151CS is $2.75, while the MP60-F module goes for $14.50 each in 1000-unit lots. Delivery is from stock.

*Semtech Corp.*
*652 Mitchell Rd.*
*Newbury Park, CA 91320-2289*
*Alan Moore (805) 498-2111*
*fax (805) 498-3804*
*e-mail: amoore@semtech.com*
*Web: http://www.semtech.com*

CIRCLE 513

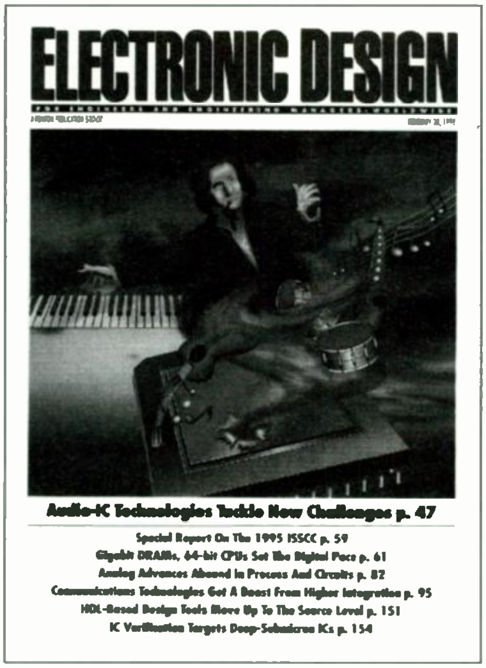
PATRICK MANNION





# STRATEGIC PARTNERS WORKING TOGETHER

Information has always been a part of the developmental strategy needed for success in the OEM market. In today's fast-paced, competitive global market environment, technology information has become a priority. Systems designers not only want to know what their strategic supply partners are doing today, but where they're going. Designers and suppliers must now work in tandem to align enabling technology with the customer's system requirements. These strategies demand strong partnerships in the development of competitive products.




A third strategic partner completes this alliance. This partner's mission is to observe and report today's product availability by its editorial staff of respected experts, while constantly probing for the next generation of enabling technology. The constant flow of exclusive and vital information helps to bring systems designers and suppliers together as strategic partners. It also provides engineers and engineering managers with an enhanced ability to bring more competitive products to market, faster.

*Electronic Design* is that strategic information partner — a partner who provides the information that helps the systems designer make those critical decisions that stay the course of the technology road map.


*Your Strategic Information Partner.*

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PRODUCT FEATURE

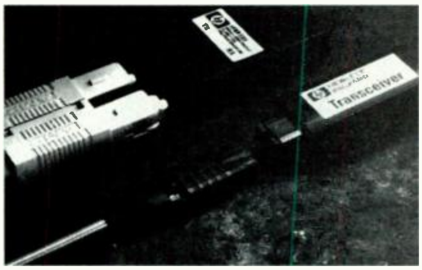
Data sheets on products like these can be found at www.penton.com/ed/

# Miniature Fiber-Optic Interconnection Doubles Port Densities

Although much progress has been made toward getting fiber-optic technology down to the local loop, cost and space requirements remain major stumbling blocks. In an effort to overcome these hurdles, AMP Inc. along with Hewlett-Packard, has announced support for the freshly minted Mini-MT fiber-optic interconnect. They see Mini-MT as the next step beyond SC connectors for 100-Mbit and 1-Gbit Ethernet, as well as 622-Mbit ATM applications.

According to Mike Peppler, Director of Product Marketing for the Optical Interconnection Systems group at AMP, the key to the connection system is the ability to fit a two-fiber, duplex connector in the space of a single SC connector or RJ-45 UTP interface. As a result, port densities will double in network and similar applications.

The connector uses a proven ferrule technology similar to the multifiber MT style, but in a smaller size. Fibers are on 0.750-μm centers. The connector is field-installable and has fewer pieces than the SC interface to reduce labor costs. The system allows use of ribbon fiber, which is smaller and less expensive than zipcord fiber and is easier to pull.




The transceiver has a profile of 9.8 mm and comes in a 10- or 20-pin DIP, giving it half the footprint of a standard SC duplex transceiver. Target data rates are 100 Mbits/s to 1.6 Gbits/s. Depending on the data rate and application, the devices will use either a 1300-nm LED, 1300-nm laser, or a 850-nm VCSEL for multimode or single-mode interfaces.

With multisourcing a key prerequisite, the connector is being developed jointly by AMP, Siecor, and USConec. AMP and Hewlett-Packard, under a multisource agreement, are independently developing the transceivers in conjunction with standards bodies. Samples are available now, with production quantities scheduled for the third quarter of this year.

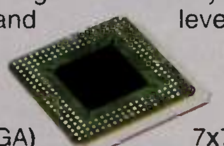
***AMP Inc.***
*P.O. Box 3608*
*Harrisburg, PA 17105-3608*
*Alan Sappe(egu) (717) 986-5160.*
***Hewlett-Packard Co.***
*5301 Stevens Creek Blvd.*
*P.O. Box 58059*
*Santa Clara, CA 95052-8059*
*Inquiries: (800) 537-7715, ext.9920.*
**CIRCLE 514**

**PATRICK MANNION**


# IC Packaging Light Enough To Make Your Ideas Fly.

An exciting new generation of ultra-compact laptops, PDAs, camcorders and wireless products is taking off right now. Launched on the wings of dramatically thinner and lighter IC packaging.

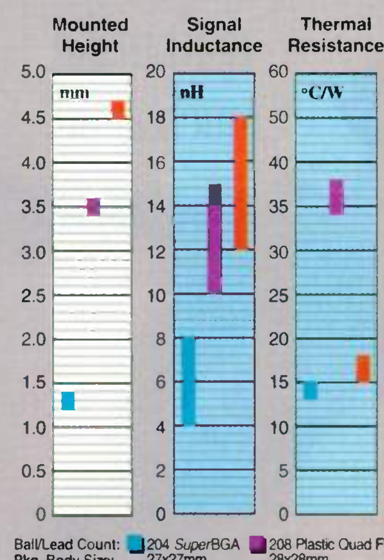
Introducing *patented Super*BGA, high performance ball grid array (BGA) IC packaging from Amkor.



Low-profile 1.2mm and 1.4mm mounted heights, enable you to down-size your best ideas and improve their performance. Advanced materials and multilayer capabilities boost speeds beyond 1.0 GHz. Direct attachment of the die to *Super*BGA's built-in heat spreader substantially increases power handling capabilities while providing EMI/RFI shielding. Moisture sensitivity exceeds JEDEC level 2 requirements.

With ball counts from 20 to 680, and body sizes from 7x7mm to 50x50mm, microprocessors, DSPs, ASICs, amplifiers and gate arrays will be soaring to new performance heights.

So why just get your ideas off the ground when you can make them fly. Call the Amkor service center nearest you or (602) 821-2408 ext. 2000.

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Tel: 602.821.5000
**USA Midwest/East**
Tel: 214.580.1879

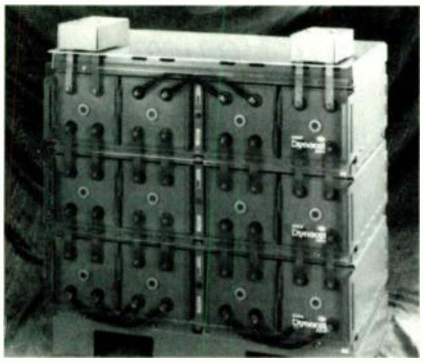
READER SERVICE 194

**POWER**

Data sheets on products like these can be found at www.penton.com/ed/

## VRLA Battery Has High Ampere-Hour Rating

The DDH valve-regulated lead-acid battery ranges in capacity from 120 Ah to 4000 Ah in 24- or 48-V configurations, and 2000 Ah in a non-paralleled configuration. The battery fits in 19-,



23-, or 30-in. relay racks, and targets wireless and telecommunications backup applications. A proprietary seal allows plates to grow without stressing the cover or post seal. Pricing starts at $4050 for 24-V, 120-Ah systems, and delivery is two weeks.

***Yuasa-Exide Inc.**, P.O. Box 14145, Reading, PA 19612-4145; (800) 538-3627; fax (610) 372-8613; alfoss@yuasa-exide.com; http://www.yuasa-exide.com.*

CIRCLE 567

## Fast Charger Protects And Conditions Li-Ion Batteries

The ABP1175-LIC is a fast-charger board for Li-Ion batteries that includes a pre-charge qualification cycle that detects shorted, open, or damaged cells. Other features include a low charge current to condition the battery when the battery voltage drops below the low-voltage threshold and LED charge status and fault indication. A two-phase fast-charge cycle provides regulated constant current in phase one and regulated constant voltage in phase two. Fast charge terminates upon the detection of a minimum charge current and/or a maximum time out. Pricing is from $229 and delivery is 12 weeks.

***ABP**, 11407 Potomac Oaks Dr., Rockville, MD 20850; Eyal Halevy (301) 424-1760; fax (301) 424-5222.*

CIRCLE 568

## Multiple NiMH or NiCd Button Cells Come In Single Package

The Integrated Battery comprises two, three, or four 35- to 500-mAh, 1.2-V NiMH or NiCd button cells in a single sealed, nickel-plated, cold-rolled-steel case. The integrated construction

reduces the possibility of intercell connection failures and short circuits. Nominal voltages are 2.4, 3.6, and 4.8 V.

***Plainview Batteries Inc.**, 23 Newtown Rd., Plainview, NY 11803; (516) 249-2873; fax (516) 249-2876.*

CIRCLE 569

## POWER

Data sheets on products like these can be found at www.penton.com/ed/

### Lithium Batteries Are Custom

This line of lithium batteries comes with three different chemistries and can be custom engineered to specific OEM requirements. Available

chemistries are lithium-thionyl chloride with energy densities ranging from 500 to 600 Wh/kg and 80% capacity retention for 10 years, as well as rechargeable lithium-ion polymer and lithium-ion inorganic.

***Battery Engineering Inc.**, 1636 Hyde Park Ave., Hyde Park, MA 02136; Robert Fay (617) 361-7555; fax (617) 361-1835;*
*e-mail: info@batteryeng.com*
*Web: http://www.batteryeng.com*
**CIRCLE 570**

### Lithium Cells Provide Extended Service Life

These lithium thionyl chloride, coin-size batteries have an output of 3.6 V and an operating lifespan rated at over 10 years. The devices have an operating temperature range of -55° to 75°C, with a 125°C upper limit available on some models. The hermetically sealed batteries come in a range of configurations, including 1/10 D, 1/6 D, and BEL

versions.

***Tadiran Electronic Industries, Inc.**, 2 Seaview Blvd., Port Washington, NY 11050; Sol Jacobs (516) 621-4980; fax (516) 621-4517; Internet: http://www-tadiranbat.com.* ***CIRCLE 571***

### Synchronous Boost Converter Operates Off 1V

Designed for low-voltage operation, the UCC3941 synchronous boost converter features 1-V-input operation startup guaranteed under full load on the main output, with operation down to 0.4 V. The device allows a step up to 3.3 V, 5 V, or an adjustable output at 500 mW for a single cell. An auxiliary 9-V output is provided. Other features include an adjustable output power limit control and an adaptive current mode to minimize switching and conduction losses. Pricing is $2.78 each per 1000 and delivery is 10 to 12 weeks.

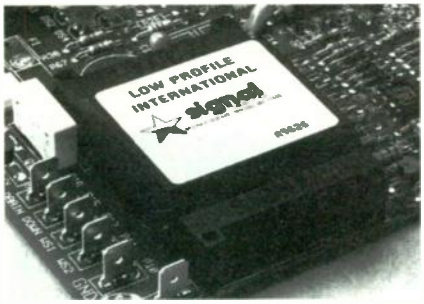
***Unitrode Corp.**, 7 Continental Blvd., Merrimack, NH 03054-0399; Mickey McClure (603) 424-2410; fax (603) 429-8963; http://www.unitrode.com.*
**CIRCLE 572**

## PASSIVE COMPONENTS

Data sheets on products like these can be found at www.penton.com/ed/

### Planar Transformers Feature Low Profile

The Low Profile International Series planar transformers are pin-for-pin compatible with the existing industry standard for low-profile transformers.




The devices are designed to meet VDE 0805, and can be interchanged with the company's Flathead Low Profile printed-circuit-mount transformers. Available in 2- and 6-VA versions, the devices have heights of 0.72 in. and 0.895 in., respectively. Output voltages range from 5 to 230 V.

*Signal Transformer Co., Inc., 500 Bayview Ave., Inwood, NY 11096-1792; (516) 239-5777; (516) 239-7208.* **CIRCLE 573**

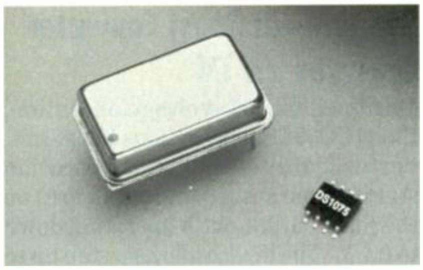
### Varicaps Target Low-Voltage Communications

Specially designed for operation at 3 V in portable equipment, the BB155 varicap replaces the TV tuners typically used in these applications. This reduces the capacitance spread from ±10% to a maximum of ±5%. Their typical value is ±3%. This translates to a spread of 45.2 to 49.8 pF at 0.34 V and 24.55 to 26.70 pF at 2.82 V. The BB155 comes in a surface-mount SOD323 package. Pricing is $0.12 each in volume.

*Philips Semiconductors, P.O. Box 218, 5600 MD Eindhoven, The Netherlands; +31 40 2 722091; fax +31 40 2 724825.* **CIRCLE 574**

### Accurate Oscillator Needs No External Reference

Packaged as an 8-pin SOIC, the DS1075 EconOscillator provides 1% accuracy with no external timing components. If greater accuracy is required, an external crystal reference can be added to the circuit. Features

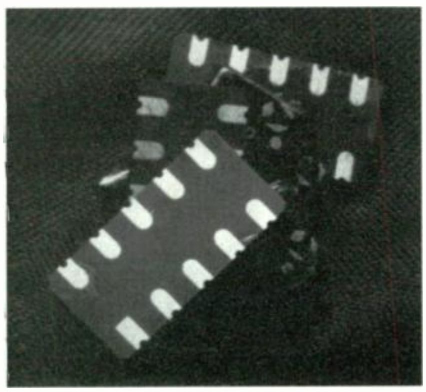


include on-chip enable and power-down functions, and a programmable on-chip prescaler and divider for multiple operating frequencies over the 0.2- to 100-MHz range. Pricing is $1.70 each per 1000.

*Dallas Semiconductor, 4401 South Beltwood Pkwy., Dallas, TX 75244-3292; Rob Brown (972) 371-3719; fax (972) 371-3715; Internet: http://www.dalsemi.com.* **CIRCLE 575**

### SAW Filter Targets CDMA Applications

The FB F033 is a 210.38-MHz SAW filter that's compatible with CDMA PCS phone architectures. The filter comes in a hermetic SMT package and has a

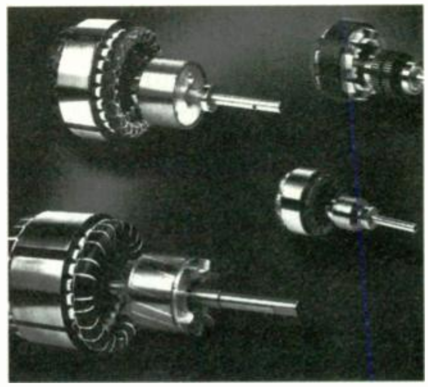


bandwidth of over 1.26 MHz.

*Thomson Components and Tubes Corp., Special Products Div., 40G Commerce Way, Totowa, NJ 07511; (201) 812-9000; fax (201) 812-9050.* **CIRCLE 576**

### Rotor And Stator Components Are Interchangeable

Available without motor housings or end caps, these rotors and stators are designed to allow interchangeability to eliminate the need for matched sets. This is further facilitated by tight tolerances on the stator OD, bearings journals, and shafts. Precision ball bearings

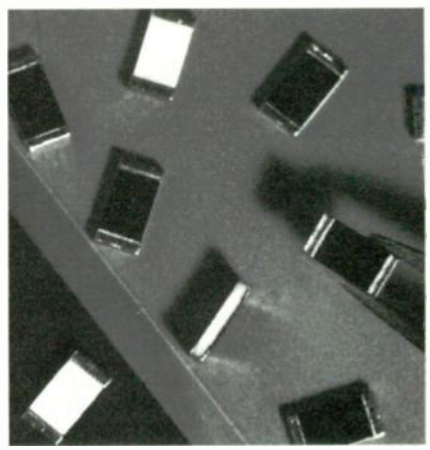


can be incorporated into the rotor. Depending on size, voltage ratings are available up to 250 V, with output ratings of 1/500 to 1/2 horsepower.

*Eastern Air Devices Inc., 1 Progress Ave., Dover, NH 03820-5449; Karen Russo (603) 742-3330; fax (603) 742-9080.* **CIRCLE 577**

### Resistor/Capacitor Array Terminates High-Speed Circuits

Comprised of one resistor and one capacitor in series, the RCC18 chip comes in a 1206-size package and is designed for the termination of high-speed digital circuits. The device has a



resistance range of 100 to 300 Ω and a voltage rating of 50 V. The capacitance range is 22 to 100 pF. The resistance and capacitance tolerance is 20% while maintaining a dissipation factor of 5% maximum. The chip comes on 8-mm tape with 5000 pieces/reel. Pricing is $35 each in 1000-unit lots and delivery is 8 weeks.

*Rohm Electronics, 3034 Owen Dr., Nashville TN 37013; Fred Froutan (615) 641-2020; fax (615) 641-2022.* **CIRCLE 578**

# System Two

## A New Standard For Audio Testing

Leading edge performance has been a defining feature of Audio Precision products since the inception of our company in 1984. Thousands of our System One audio analyzers are in use worldwide, selected by design engineers for high performance and by test engineers for our comprehensive programmable analog and digital audio measurement capabilities.

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System Two is a true Dual Domain analyzer. Other test instruments may have both analog and digital inputs and outputs ... but they're not true Dual Domain! They rely on performance-limiting converters to pass analog signals back and forth to a DSP core of digital-only hardware. Passing signals through a/d or d/a converters for every measurement robs the test instrument of performance. System Two includes separate, independent hardware for direct audio measurements in both domains, plus additional and extensive interface measurement capability including jitter measurements, eye patterns and all other parameters described in AES3, the serial audio interface standard.

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READER SERVICE 99

# Obtain Higher Effective Resolution For Temperature Measurements

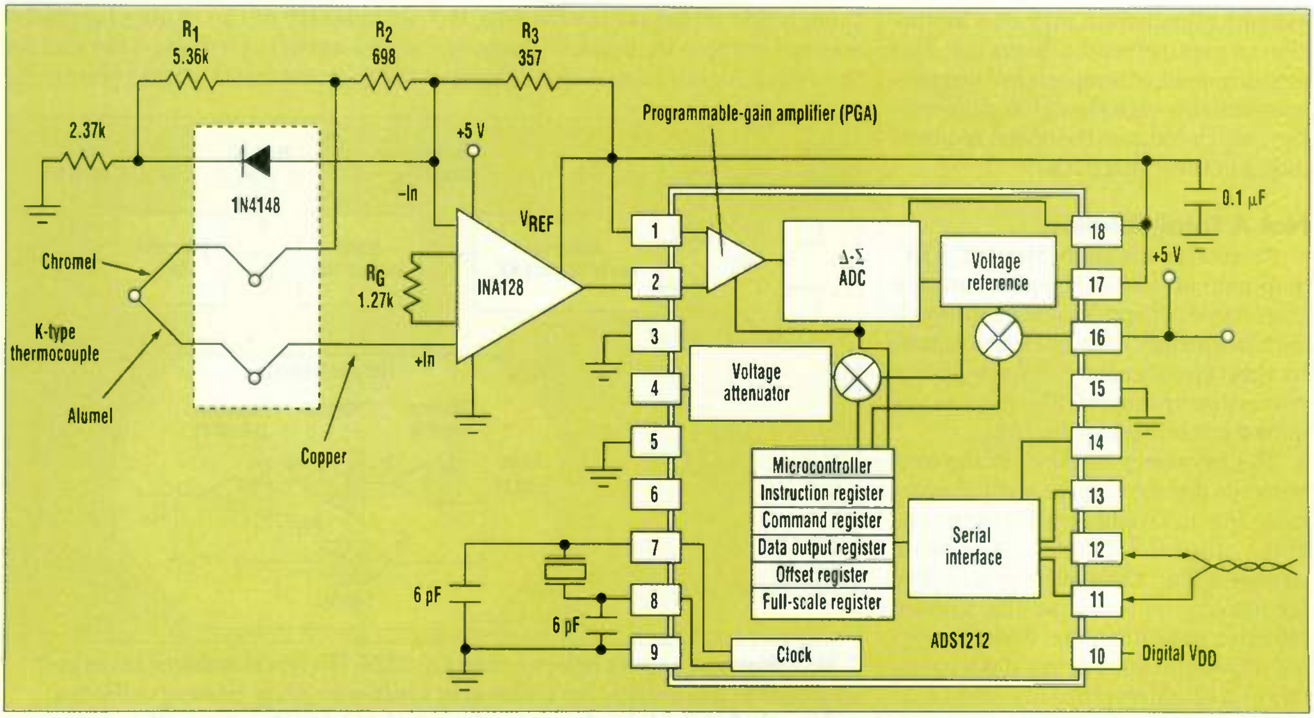
*Combining Hardware and Software Techniques In Δ-Σ ADC Circuits With Front-End Analog Gain Can Provide The Right Performance.*

**BONNIE C. BAKER,** Burr-Brown Corp., 6730 S. Tucson Blvd., Tucson, AZ 85706; (520) 746-7984; fax (520) 746-7467; e-mail: *baker_bonnie@burr-brown.com.*

Measuring small signals from sensitive process-control sensors has always been a challenge for the analog designer. Sensing elements, such as thermocouples, RTDs and bridges, have outputs that produce voltages from hundreds of millivolts to several volts. In contrast, prior to analog signal conditioning of these sensors, the delta output voltages of these sensors that represent a change in temperature, pressure, light, etc., are relatively low—in the sub-millivolt or millivolt range. These small deltas are usually the signal of most interest in process-control or instrumentation systems.

Careful analog signal conditioning, in combination with a 12- to 16-bit analog-to-digital converter (ADC), usually captures the pertinent information from the sensors. In this design topology, the task of signal enhancement falls on the analog front end, which is usually expensive and susceptible to noise. An alternative approach would be to use a high-resolution ADC, thereby reducing or completely eliminating the need for a complex analog front end.

Delta-Sigma (Δ–Σ) converters have significantly improved the achievable resolution and accuracy of ADCs while also lowering the overall system price. These converters digitize analog voltages to extremely high de-




**1. A thermocouple can be interfaced with an instrumentation amplifier and a Δ-Σ ADC to achieve 21-bit accuracy for a full-scale input range of 50 mV. the cold-junction compensation circuit shown uses a diode an a resistive network on an isothermal block.**

**TABLE 1: OVERSAMPLING (TURBO) MODES FOR BURR-BROWN'S ADS1212 ADC**

| Sample rate (Hz) | Turbo 1 (bits, rms) | Turbo 2 (bits, rms) | Turbo 4 (bits, rms) | Turbo 8 (bits, rms) | Turbo 16 (bits, rms) |
|---|---|---|---|---|---|
| 10 | 20 | 21 | 21 | | |
| 20 | 19 | 20 | 21 | 21 | |
| 40 | 18 | 20 | 21 | 21 | 21 |
| 50 | 17 | 19 | 20 | 21 | 21 |
| 60 | 17 | 19 | 20 | 21 | 21 |
| 100 | 15 | 17 | 19 | 21 | 21 |
| 250 | 12 | 14 | 16 | 19 | 20 |

grees of resolution, up to 20 to 24 bits, rendering least significant bit (LSB) sizes equal to or better than 1 million divisions of full scale ($2^{20}$ = 1,048,576). A 22-bit-accurate ADC has a dynamic range equivalent to 132 dB. If the dynamic range of the system ADC is relatively high, the cost of the application can be lowered. In addition, system complexity is reduced, making the design easier.

A Δ–Σ converter intended for industrial type measurements is optimized for accurate, low-frequency data conversions. Techniques such as input modulation by the use of integration and digital filtering nearly eliminate the analog anti-aliasing filter, while achieving greater accuracy. The trade-off for superior performance in accuracy is frequency. The sampling bandwidth may be a limitation in some circuits, however, the measurement of temperature or pressure variables are slow-changing entities, which reduces the speed requirements of the signal path.

## Not A Total Solution

As good as it sounds, the Δ–Σ ADC does not solve all of the problems for these types of applications. Although digital filtering techniques are utilized by this type of converter, even higher resolution or bandwidths may be required in a critical application.

The frequency response of the converter is dictated by the level of oversampling and sophistication of the on-chip digital filters. A lower oversampling ratio leads to a higher frequency response, but also a lower effective resolution. The design trade-off of resolution versus data rates when Δ–Σ converters are used in a system are examined in this article. Although the Δ–Σ converter brings the circuit designer considerably closer to achieving the desired results, the total application may still require additional resolution and speed.

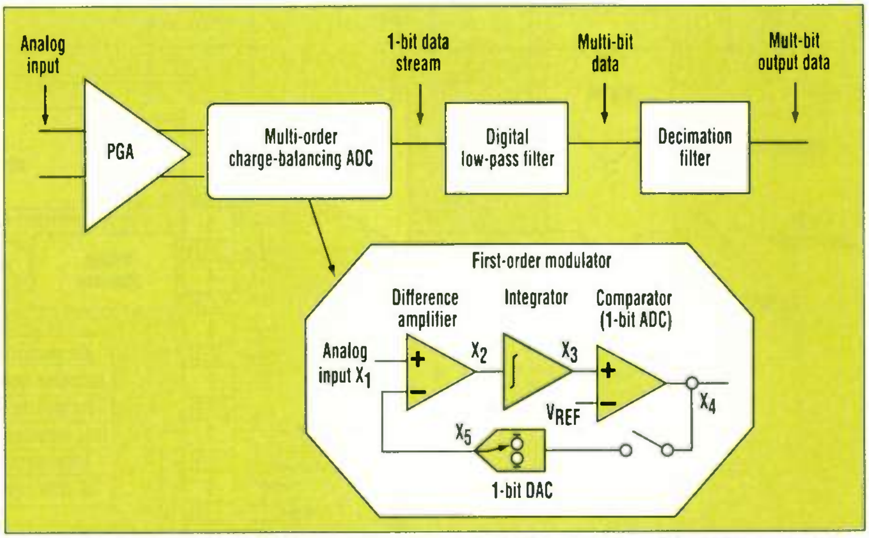
Enhancements of a system containing a Δ–Σ ADC can be achieved with digital software gain techniques and the addition of front-end analog gain blocks. Digital gain beyond the capability of the ADC is attainable using techniques such as microcontroller or microprocessor data shifting, sometimes termed "software gain." The technique of shifting the output bits of the ADC in the microprocessor is not new. However, the arrival of Δ-Σ ADC technology necessitates a reexamination of this technique.

The use of software gain can change a 20-bit system with a signal gain of 1, to a 14-bit system with a gain of 64. Although this technique is effective, it does not increase the dynamic range of the ADC. An additional analog gain stage is required in hardware to achieve higher effective resolution. With this new design approach, the combination of using the Δ–Σ ADC's internal gain, the converter's oversampling capability, software digital gain, and hardware analog gain, allows one to easily achieve an overall system gain as great as 1024 and resolutions up to 15 bits *(Fig. 1)*. With this type of performance, industrial process-control systems can take full advantage of Δ-Σ ADCs.

## How Is It Done?

How does a Δ–Σ converter obtain its good dynamic range? The fundamental design topology of the ADC is based on a single-bit quantizer with a digital filter. This is in contrast to the multi-bit architectures used in converters such as sub-ranging or successive-approximation devices.

A state-of-the-art Δ–Σ converter has an input programmable-gain amplifier (PGA), a multi-order charge-balancing ADC (which replaces the single-bit quantizer), offset and full-scale system calibration capability, and a programmable digital filter *(Fig. 2)*. These four functional blocks assimilate to allow for a high resolution converter that has more analog and digital functions than ever before. In this manner, the Δ–Σ ADC has reduced the complexity of the analog input circuitry as well as lightened the load for the microcontroller or microprocessor




**2. Block diagram of a generic high-performance Δ-Σ ADC. This type of modulator has an input programmable-gain amplifier that's followed by a multi-order charge-balancing section that performs the first step in low-frequency noise-reduction, and digitizes the signal ones and zeros. This stage is followed by a digital low-pass filter.**

on the digital side of the device.

To understand the function of the multi-order charge-balancing ADC, a conceptual drawing of a first-order stage is shown in the insert (*Fig. 2, again*). Following the signal path around the digital servo loop, the voltage at the analog input of the single-bit quantizer is differentiated against the output ($X_5$) of the 1-bit digital-to-analog converter (DAC). The difference of analog input $X_1$ and the output of the 1-bit DAC results in an analog voltage at $X_2$. $X_2$ is integrated resulting in a negative- or positive-sloping output with time ($X_3$).

The sign of the slope at the output of the integrator is dependent of the sign of the input signal at $X_2$. When the voltage at $X_3$ equals the comparator reference voltage, the output of the comparator changes from a 1 to a 0 or a 0 to a 1, depending on the previous state. The digital output of the comparator ($X_4$) is clocked into the 1-bit DAC, as well as clocked into the digital filter stage. At this time, the 1-bit DAC clocks its analog output voltage change to the difference amplifier. This creates a completely different output voltage at $X_2$, causing the integrator to create a sloping output in the opposite direction.

The output of the multi-order charge-balancing converter in is a 1-bit digital stream. The series of ones and zeros at $X_4$ is not only sent to the servo 1-bit DAC, but also to the digital filter stage. The digital filter of the $\Delta$–$\Sigma$ converter uses oversampling and averaging techniques, processing the signal to higher accuracy. Common digital filter blocks used in $\Delta$–$\Sigma$ conversion systems are either finite impulse response (FIR) or infinite impulse response (IIR) types. The FIR digital filter is more stable than the IIR filter and has a linear phase response. On the other hand, the IIR digital filter has a sharper transition region allowing for a lower-order filter than the FIR filter would require for the same general filtering results. Usually the digital filter and decimation filter functions are combined, affecting the dynamic range and the output data rate collectively.

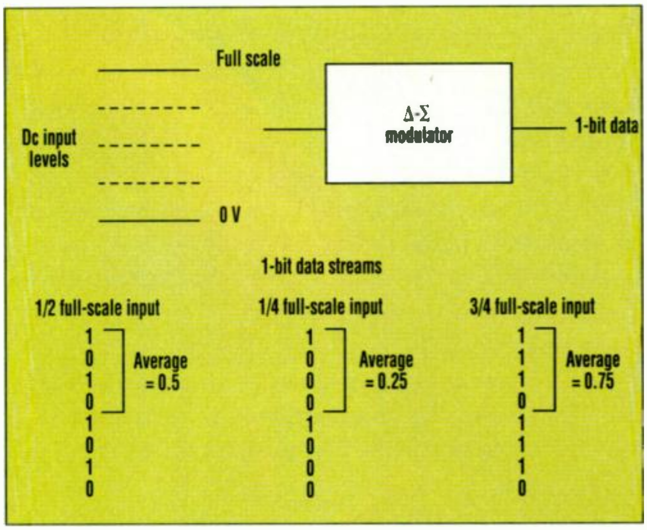
Recalling the signal output of the charge-balancing converter in, the output at $X_4$ is a series of digital ones and zeros (*Fig. 2, again*). The output state of the charge-balancing converter (a 1 or a 0) is clocked into the digital filter and stored in a FIFO register. The clock used at this point in the signal path is called the sampling

**TABLE 2: TABULAR REPRESENTATION OF THE EFFECTS OF DATA SHIFTING USING A MICROCONTROLLER SHIFT-REGISTER ALGORITHM AND BURR-BROWN'S ADS1212 ADC**

| Gain | System gain | Input range | Effective resolution | DB21 (MSB)/ DB20 | DB19/ DB18 | DB17/ DB16 | DB15/ DB14 | DB13/ DB12 | DB11/ DB10 | DB9/ DB8 | DB7/ DB6 | DB5/ DB4 | DB3/ DB2 | DB1/ DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PGA = 1 | 1 | 5V | 20 | 2.5/1.25 | 0.625/ 0.3125 | 0.156/ 0.078 | 0.039/ 0.0195 | 0.009/ 0.0048 | 0.0024/ 0.0012 | 0.0006/ 0.0003 | 0.00015/ 0.000076 | 0.000038/ 0.000019 | 0.000009/ $4.8 \times 10^{-6}$ | X/X |
| PGA = 2 | 2 | 2.5V | 20 | 1.25/0.625 | 0.3125/ 0.156 | 0.078/ 0.039 | 0.0195/ 0.009 | 0.0048/ 0.0024 | 0.0012/ 0.0006 | 0.0003/ 0.00015 | 0.000076/ 0.000038 | 0.000019/ 0.000009 | $4.8 \times 10^{-6}$/ $2.4 \times 10^{-6}$ | X/X |
| PGA = 4 | 4 | 1.25V | 20 | 0.625/ 0.3125 | 0.156/ 0.078 | 0.039/ 0.0195 | 0.009/ 0.0048 | 0.0024/ 0.0012 | 0.0006/ 0.0003 | 0.00015/ 0.000076 | 0.000038/ 0.000019 | 0.000009/ $4.8 \times 10^{-6}$ | $2.4 \times 10^{-6}$/ $1.2 \times 10^{-6}$ | X/X |
| PGA = 4 SWG = 2 | 8 | Equivalent FS = 0.625V | 19 | 0.3125/ 0.156 | 0.078/ 0.039 | 0.0195/ 0.009 | 0.0048/ 0.0024 | 0.0012/ 0.0006 | 0.0003/ 0.00015 | 0.000076/ 0.000038 | 0.000019/ 0.000009 | $4.8 \times 10^{-6}$/ $2.4 \times 10^{-6}$ | $1.2 \times 10^{-6}$/X | X/X |
| PGA = 4 SWG = 4 | 16 | Equivalent FS = 0.3125V | 18 | 0.156/ 0.078 | 0.039/ 0.0195 | 0.009/ 0.0048 | 0.0024/ 0.0012 | 0.0006/ 0.0003 | 0.00015/ 0.000076 | 0.000038/ 0.000019 | 0.000009/ $4.8 \times 10^{-6}$ | $2.4 \times 10^{-6}$/ $1.2 \times 10^{-6}$ | X/X | X/X |
| PGA = 4 SWG = 8 | 32 | Equivalent FS = 0.1562V | 17 | 0.078/ 0.039 | 0.0195/ 0.009 | 0.0048/ 0.0024 | 0.0012/ 0.0006 | 0.0003/ 0.00015 | 0.000076/ 0.000038 | 0.000019/ 0.000009 | $4.8 \times 10^{-6}$/ $2.4 \times 10^{-6}$ | $1.2 \times 10^{-6}$/X | X/X | X/X |
| PGA = 4 SWG = 16 | 64 | Equivalent FS = 0.078V | 16 | 0.039/ 0.0195 | 0.009/ 0.0048 | 0.0024/ 0.0012 | 0.0006/ 0.0003 | 0.00015/ 0.000076 | 0.000038/ 0.000019 | 0.000009/ $4.8 \times 10^{-6}$ | $2.4 \times 10^{-6}$/ $1.2 \times 10^{-6}$ | X/X | X/X | X/X |
| PGA = 4 SWG = 32 | 128 | Equivalent FS = 0.039V | 15 | 0.0195/ 0.0009 | 0.0048/ 0.0024 | 0.0012/ 0.0006 | 0.0003/ 0.00015 | 0.000076/ 0.000038 | 0.000019/ 0.000009 | $4.8 \times 10^{-6}$/ $2.4 \times 10^{-6}$ | $1.2 \times 10^{-6}$/X | X/X | X/X | X/X |
| PGA = 4 SWG = 64 | 256 | Equivalent FS = 0.0195V | 14 | 0.0009/ 0.0048 | 0.0024/ 0.0012 | 0.0006/ 0.0003 | 0.00015/ 0.000076 | 0.000038/ 0.000019 | 0.000009/ $4.8 \times 10^{-6}$ | $2.4 \times 10^{-6}$/ $1.2 \times 10^{-6}$ | X/X | X/X | X/X | X/X |

Note: FS = full scale, PGA = the gain setting of the ADC, SWG = software gain. The system gain is the combined gain of the ADC and the software gain. The input range is determined by the ADC input range plus the effects of software gain. As the bits are shifted to the left, the MSB is "thrown away" reducing the full-scale range of the overall system.

clock. The sampling clock is a derivative of the system clock, the PGA gain, the oversampling rate and the decimation ratio. In the case of the Burr-Brown ADS1212 and ADS1213 ADCs, the oversampling rate, also known as the Turbo rate, is adjustable to 1, 2, 4, 8 or 16.




**3. The simplest digital filter is an averaging system in which the analog signal is clocked into the filter as a series of representative ones and zeros. This example illustrates a 4X averaging filter, where 4 digits are taken and averaged, giving an overall higher resolution than the original 1-bit system. This filter provides a sin (x)/x transfer function that can be used to effectively eliminate line frequency. Although this filter increases resolution, it also requires more time than an FIR or IIR digital filter.**

## Digital Filtering

Both the digital filter and decimation filter, or combination thereof, utilize arithmetic tools to reduce the system noise, consequently achieving a conversion process with a higher dynamic range. This filtering action can be best understood by examining the most simplistic digital filter, the averaging filter *(Fig. 3)*.

With this filter topology, as with all filter topologies, a predetermined number of samples are required to compute the final value. The digital averaging filter waits an appropriate number of clock pulses for its FIFO register to fill with ones and zeros from the charge-balancing converter stage *(Fig. 3, again)*. Once the register is full, the ones and zeros are averaged to arrive at the computed output value which is presented at the output of the ADC.

To observe this operation, consider the three different dc input levels. In this averaging digital filter, the FIFO register has four positions. If the input to the Δ–Σ charge-balancing converter is approximately one-half full scale, the output of the charge-balancing converter would be a steady stream of alternating ones and zeros with a 50% duty cycle. Consequently, the FIFO register would be filled with an equal number of ones and zeros. Since the digital filter averages a predetermined four samples at a time, the average of four binary numbers resulting from a one-half full-scale-range input would be 0.5. If the dc analog input is changed to one-quarter full scale, the resultant output of the charge-balancing converter would change to a string of the code 1000. This would result in an output value of 0.25. It is useful to note that the original system was only capable of producing either a one or a zero. By definition, this system is a 1-bit digitizer. By collecting samples from this stream of ones and zeros at consistent time intervals and averaging by a factor of four, the 1-bit system is transformed to a 2-bit system.

Four time samples of the 1-bit data at the output of the modulator are averaged; but in fact, any number of samples can be used in the calculation. As shown, the accuracy of the conversion process improves with the increase in the number of samples that are averaged. Unfortunately, there is a design trade-off for this particular digital filter. More samples mean higher dynamic range, but also increased conversion time. The conversion time of the simple averaging digital filter can be decreased with alternative approaches like a rolling average filter or a variety of more sophisticated filters.

Oversampling in conjunction with digital filtering is a technique used to reduce the quantization noise level in the system. From an analog designer's perspective, this could be translated as increased system gain. Consequently, analog circuit complexity is simplified because of a reduction of analog gain, possibly resulting in the elimination of a gain stage.

To illustrate this point, a 12-bit ADC with a full-scale range of 1 V is used. The LSB size of this converter would be 244 mV. The system LSB size can be reduced 4X by implementing an external analog gain of 4 V/V. In this case, the system would be able to resolve to an LSB size of 61 mV. In digitizing systems, the signal-to-noise ratio (SNR) is improved with increased oversampling.

The conversion process will have a theoretical 6-dB or 1-bit improvement in the SNR for an oversampling factor of 4. If the oversampling of the system is increased 16X, it would be equivalent to applying a gain of four, in that the LSB size has changed from 244 mV to 61 mV.

A user of Burr-Brown's Δ–Σ ADCs can select the desired oversampling ratio (or Turbo mode, as specified by Burr-Brown). For example, if a device such as the ADS1212 is configured in a Turbo mode 1 (oversampling = 1), the charge-balancing converter oversamples at 20 kHz allowing the ADS1212 to achieve 20 effective bits at 10 Hz. In contrast, a Turbo mode 2 configuration oversamples at 40 kHz. The effective resolution with respect to frequency is shown *(Table 1)*.

In the table, a combination of Turbo mode (or oversampling multiple) and decimation ratio is changed resulting

**TABLE 3: TEMPERATURE COEFFICIENTS OF VARIOUS THERMOCOUPLE TYPES**

| ISA Type | Metals used for wires | Temperature coefficient (µV/°C at 0° C) |
|---|---|---|
| E | Chromel/constantan | 58.5 |
| J | Iron/constantan | 50.2 |
| K | Chromel/alumel | 39.4 |
| T | Copper/constantan | 38.0 |

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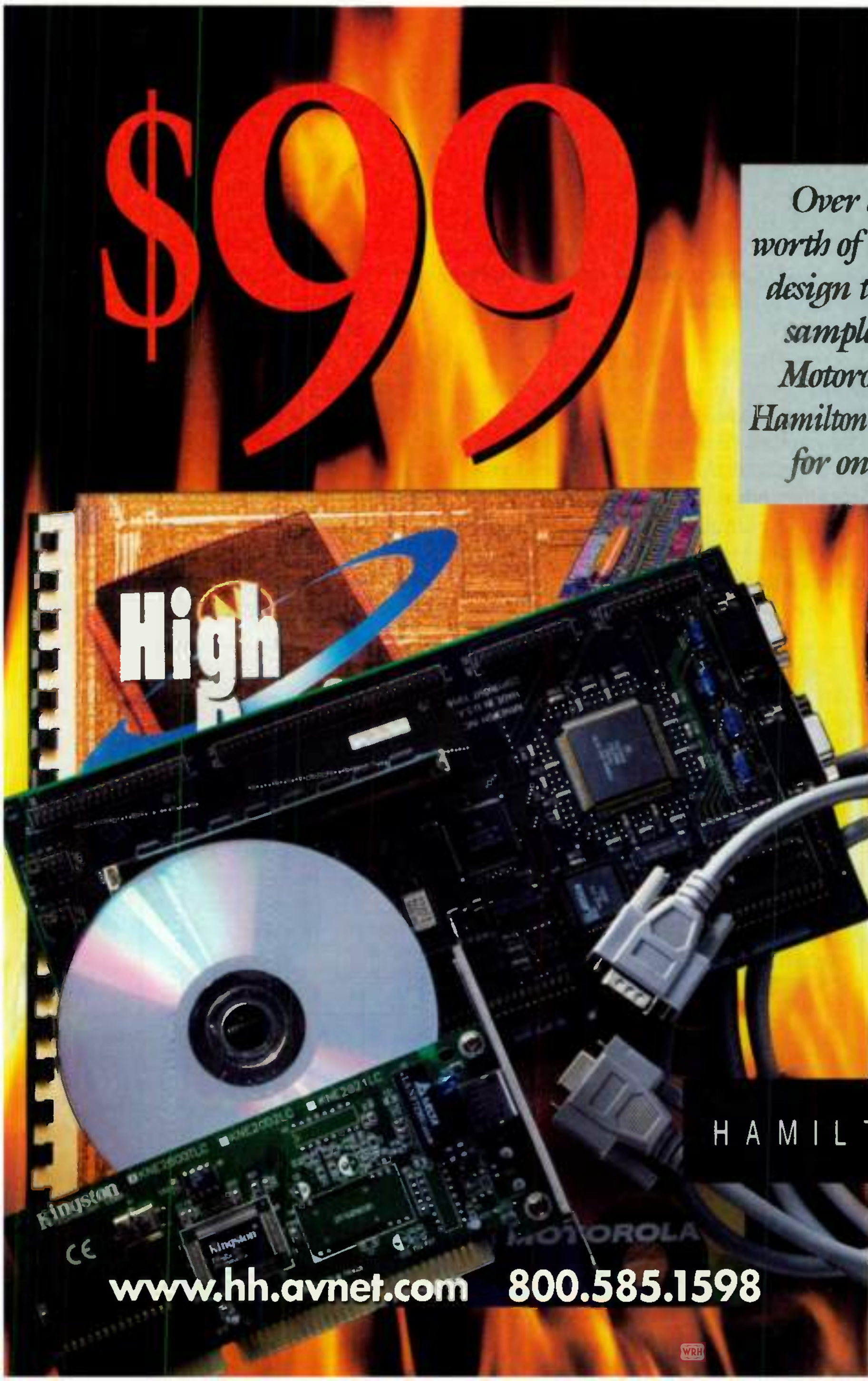


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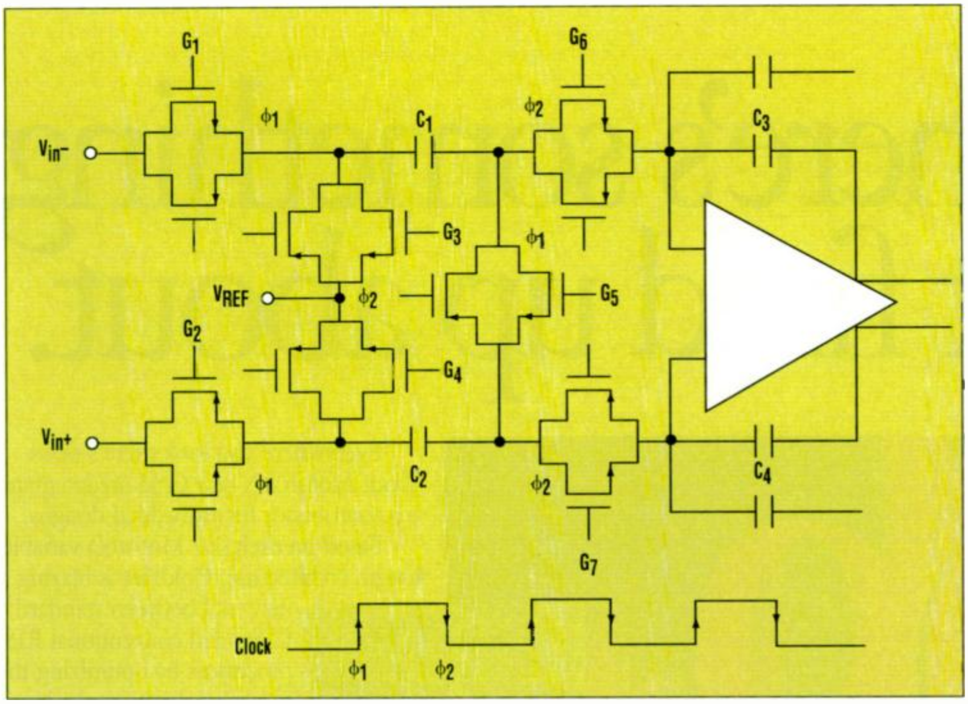



**4. The input stage of the Burr-Brown ADS1212/1213 Δ-Σ ADC uses a switched-capacitor topology($C_1$ and $C_2$, $C_3$ and $C_4$) to sample the signal as well as perform the gain function.**

in a change in the data rate and the effective bits at the output of the Δ-Σ converter, the ADS1212. As the Turbo mode increases, the effective bits resolution also increases. As the decimation ratio is decreased, the sample rate increases. The ADS1212 is configured with a gain setting of one and a 1-MHz clock.

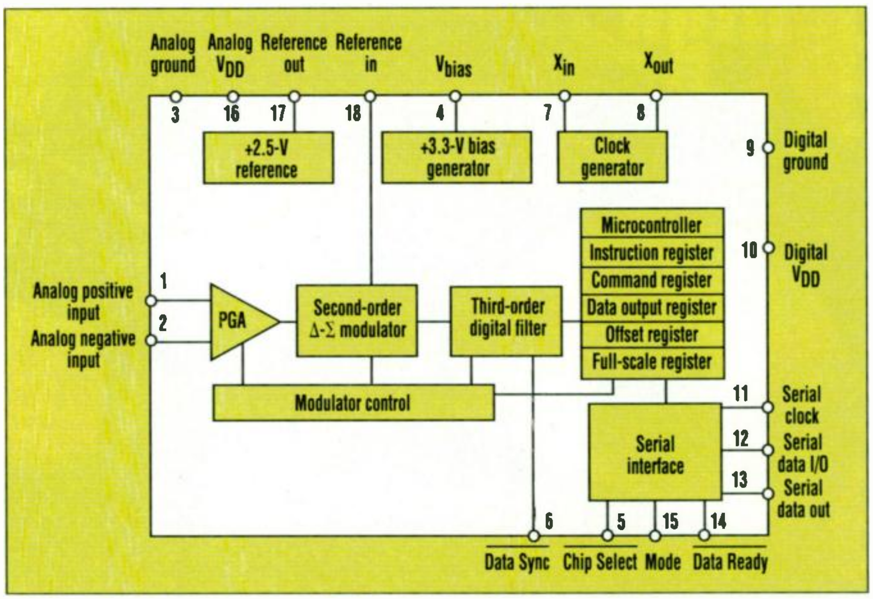
## Signal Gain On-Chip

With the Δ–Σ converter, oversampling is used effectively to improve the dynamic range or reduce the quantization noise levels of the conversion process. To further enhance the effective resolution of the converter, the converter is configured with a differential input and a PGA stage. User-selectable PGA gains of 1, 2, 4, 8, or 16 are possible.

The circuit implementation of the PGA stage is shown, where the inputs are differential, followed by a switched-capacitor amplifier *(Fig. 4)*. A combination of oversampling and capacitor gain is used to achieve the specified gains. The input signal to the PGA stage of the converter is clocked onto the front-end capacitors (C1 and C2) on the rising edge of the sampling clock. The charge that's stored on these capacitors is then transferred to the second pair of capacitors C3 and C4) on the falling edge of the sampling clock. If the PGA gain is one, the first signal is sent forward from the second pair of capacitors to the modulator at the time of the next rising clock edge. Additionally, the input signal is sampled a second time and that charge is stored on the first pair of capacitors (C1 and C2).

For PGA gains greater than one—like a gain of two—the second rising clock edge does not transmit the signal from the second capacitor pair to the modulator section. The second pair of capacitors (C3 and C4) retain the original charge from the first sample and adds it to the charge from the second sampled input. In this manner the charge on the second pair of capacitors is approximately doubled. As the gain of the PGA stage is increased to 2, 4, 8, or 16, more time is required to fully sample the input.

A functional diagram of the complete Δ–Σ ADC is shown *(Fig. 5)*. The input to this converter rejects common-mode voltages to 160 dB because of its differential inputs. The accuracy/resolution capability are enhanced with the programmable system offset calibration, as well as, the full-scale range calibration capacity with the on-chip microcontroller. A Δ–Σ converter, such as the ADS1212 or ADS1213, are precision, wide-dynamic-range, 22-bit, devices operating from a single +5-V supply. The ADS1212 is a single-channel ADC and the ADS1213 is a 4-channel multiplexed version of the ADS1212. These products offer 3-wire serial interface capability, a command structure, and a register set that allows




**5. The full representation of a Δ-Σ ADC is shown above. Not only does this circuit digitize the input signal with a combination of noise-shaping and noise-reduction techniques, it also relieves the microcontroller of some overhead tasks such as offset and full-scale calibration.**

interfacing to all of the popular microprocessors. In addition, the differential inputs are useful when a direct connection to transducers is required.

### Software-Added Gain

Initially, the converter should be optimized using the internal PGA gain and oversampling features of the ADC. Subsequent increases in gain are performed by shifting the data within the registers of the microcontroller or microprocessor. Software data shifting changes the relative weighting of the data bit while keeping the dynamic range of the converter constant. In this manner, the relative weighting of the data bit is decreased, or in terms of gain, there's an increase in signal gain.

The concept of software data shifting is shown *(Table 2)*. The first four rows of information in the table illustrate the effects of changing the internal PGA gain of the converter. For example, a PGA gain of 2 will provide a system gain of 2 with an input range of 2.5 V. The converter shown in the table has 22-bits of actual output, but its effective RMS accuracy is 20 bits with a 10-Hz bandwidth. The effective LSB size, with the converter set to a gain of 2, is 2.4 mV. To further enhance the LSB size, a gain of 4 can be selected. In this case, the effective LSB size is 1.2 mV.

A further gain of two can be implemented with software shifting. Each shift to the left provides additional gain of 2X. For instance, a software gain of 16 is equivalent to shifting the bit registers by four positions. Note that the value of the LSB size has not changed, but has changed positions in the output word from the DB2 position to the DB6 position in the byte.

**Δ-Σ converters have significantly improved the achievable resolution and accuracy of ADCs while also lowering the overall system price.**

Although this technique is effective, it does not increase the dynamic range of the converter. In contrast, the software gaining technique is a low-cost approach to enhancing the gain of the system, at the expense of increased microcontroller overhead time.

### Front-End Analog Gain

The Δ–Σ converter has the ability to enhance the accuracy of the signal conversion by means of its internal PGA gain and digital filter stages. In the event that the optimum combination of the two internal stages of the converter cannot provide the required system LSB size, other methods like an external input gain stage using an instrumentation amplifier can be used.

For example, an optimum configuration for the ADS1212 with a data rate of 10 Hz would be a Turbo (oversampling-rate) setting of 4 and a PGA gain setting of 4. For a 10-Hz data rate and zero input, the effective output RMS noise level of the ADS1212 would be about 0.975 mV RMS (typically). In a system where the thermocouple is connected directly to the converter's inputs, one LSB for a K-type thermocouple, which has a delta output range of 50 mV for a temperature delta of 1250°C, would equal about 6.094 m°C. The effective resolution for this system would be 21.3 bits RMS. This is not a practical solution, however, since the K-type thermocouple output range of 50mV (maximum) would never achieve the converter's full-scale input range of 2 V.

Using an external instrumentation amplifier, like the Burr-Brown INA128, as an analog gain stage changes the effective full-scale and dynamic range of the overall system *(Fig. 1, again)*. The instrumentation amplifier is followed by the Δ-Σ converter and, finally, the microcontroller. With the converter properly configured for optimum internal analog gain and digital filtering, the overall circuit achieves the best SNR performance.

Sensing devices, such as thermocouples, RTDs, and strain gauges respond to physical or mechanical occurrences. These occurrences are converted to voltages or currents that are conditioned in the electronics of the process-control system.

The sensitivity of these temperature sensors or strain gauges varies, depending on their construction. For example, the thermocouple is an inex-

**EQUATION LISTINGS**

$$\begin{aligned}\text{INA128 output noise} &= \text{noise (@10 Hz)} \times \sqrt{10} \times \text{(gain of INA128)} \\ &= 10\text{ mV}/\sqrt{\text{Hz}} \times 3.1623 \times 40 \\ &= 0.1265\ \mu\text{V rms}\end{aligned} \quad (1)$$

$$\text{System noise (referred to output)} = \sqrt{(\text{INA128 output noise})^2 \times (\text{gain of PSA}) + (\text{ADC noise})^2}$$

$$\text{Effective system LSB (referred to input)} = \frac{\text{System noise (referred to output)}}{(\text{INA128 gain}) \times (\text{PGA gain})} \quad (2)$$

$$\text{Effective system LSB (referred to input)} = \frac{1.007\ \mu\text{V rms}}{40 \times 4}$$

$$\text{Effective system LSB (referred to input)} = 6.295\text{ nV rms}$$

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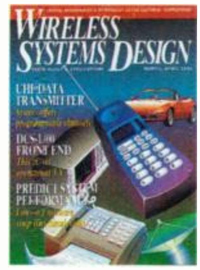


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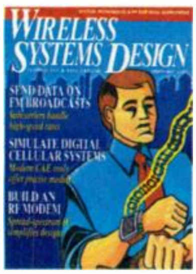


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pensive way to sense large temperature changes in the ranges of 0 to 1700°C. Two dissimilar metals are connected together to construct a thermocouple. An EMF voltage is created as a result of the temperature difference from one end of the metals to the other. The sensitivity of four different thermocouples is shown *(Table 3)*.

The temperature-sensing system previously illustrated uses a K-type thermocouple whose sensitivity is 39.44 μV/°C at 0°C and typically operates over 0 to 1250°C *(Fig. 1, again)*. The delta output voltage response of the thermocouple for 0 to 1250°C would be about 50 mV.

In this circuit, the 2.5-V voltage reference of the converter biases the diode and also sets the common-mode voltage of the inputs and the output stage reference of the instrumentation amplifier. The optimal full-scale INA128 output swing of 2.25 to 4.25V is achievable with the common mode of the thermocouple inputs biased to 2.25 V (implemented with resistor R3). The INA128 output swing restrictions dictate that the gain of the instrumentation amplifier is 40 V/V. The 1N4148 diode has drift characteristics of -2 mV/°C. It is physically located on the isothermal block along with wire junctions of Alumel/copper (135.9 μV/°C at 0°C) and Chromel/copper (96.5mV/°C at 0°C). This offsets the undesirable temperature effects of these wire junctions. A voltage divider across the diode (R1 and R2) is used to subtract the errors generated by the two junctions of Alumel/copper and Chromel/copper.

The optimum configuration for the ADS1212 with a data rate of 10 Hz would be a Turbo (oversampling rate) setting of 4 and a PGA gain setting of 4. For a 10-Hz data rate and zero input, the effective output RMS noise level of the ADS1212 would be about 0.975 μV RMS. This is approximately 21-bit accuracy with a full-scale input range of 2 V. For a full-scale input of 50 mV, which is the voltage range that the thermocouple is capable of producing from 0 to 1250°C, the effective resolution of that input range is a little better than 15-bit accurate.

With the INA128 in the circuit configured for a gain of 40, the output noise of the instrumentation amplifier is: (see equation 1 listing).

The effective LSB size at the thermocouple is about 6.3 nV RMS. This is calculated with the following formula: (see equation 2 listing).

In the system where the INA128 is placed in the signal path, one LSB for a K-type thermocouple would equal about 0.157μ°C. Note that this is almost a 40X improvement over the system with the Δ–Σ converter alone. The ideal effective resolution of this entire system is approximately 23 bits RMS to a full-scale input range of 50 mV. Since the converter is capable of only 21-bit accuracy, it limits the effective resolution of the system to 21 bits with a full-scale range of 50 mV.

In general, a combination of PGA and oversampling of the Δ–Σ ADC should be implemented as a first-pass attempt to improve system resolution of the circuit. If additional accuracy or resolution is required, external analog gain is a viable option.The finishing touches of the signal conditioning is performed by the microcontroller, where software gain or bit shifting is used. Using these three techniques or any combination is an effective way of tackling the challenging design problems when dealings with sensor measurements.

Suggested Reading:


- 1996 Burr-Brown Corp. Seminar Manual, Chapter 1, *LI-447*, Burr-Brown Corp.
- "Delta Sigma A/D Conversion Technique Overview," *AN-10, Crystal Semiconductor, Corp.*
- "Programming Tricks for Higher Conversion Speeds Utilizing Delta Sigma Converters," *AB-106*, Bonnie C. Baker.
- "Giving Δ–Σ Converters a Little Gain Boost with a Front End Analog Gain Stage," *AB-107*, Bonnie C. Baker.


*Bonnie Baker is Senior Applications Engineer, Data Products Div., at Burr-Brown. She holds an MSEE from the University of Arizona, Tucson.*

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# Low-Offset And Low-Power Universal Op Amps Arrive

*A Pair Of Wide-Bandwidth, Low-Power Op Amps Offer Designers Basic Building Blocks That Can Play Many Roles In Analog Or Mixed Systems.*

**Frank Goodenough**

For analog designers, 1997 can be classified as the "Year of the Op Amp." It all started at the International Solid State Circuits Conference (ISSCC) this past February with a number of papers that described some very innovative op amps. Many of these devices, however, are still in the development stage, and will not be appearing anytime soon on distributors' shelves. On the other hand, a few amplifiers have reached the so-called merchant market-packing specifications that may be broad enough to qualify them for the title of universal op amp in years to come.

One of these op amps, Motorola's MC33502, has already seen the merchant market light-of-day (ELECTRONIC DESIGN, *Feb. 17, p. 87*). Now, two more ISSCC '97 op amps are headed for widespread availability. From Texas Instruments (TI) comes the TLC4501/02 (single/dual) family, potentially the ultimate universal precision op amp for systems powered by the ac line. It offers self-calibration at power-up, which cuts the maximum offset voltage of some models to less than 50 µV.

A trio of general-purpose, low power amplifiers from Maxim also are included in the op amp class of '97. The MAX4162, and its dual and quad siblings, the MAX4163 and MAX4164, also rate universal status for their ability to handle a wide range of different applications. They offer 200 kHz of bandwidth at a maximum quiescent current of a mere 35 µA from a single 5-V rail. Moreover, they couple an open loop gain of 90 dB with a rail-to-rail I/O swing.

A third IC op amp, a power op amp from Burr-Brown that sports rail-to-rail I/O and is rated at 70 V and 3 A, also is headed for the merchant market *(see "Power Op Amps Sport Rail-to-Rail I/O Control Up To 3 A At 70 V," p. 150)*.

Both the TLC4501/02 and the MAX4162/3/4) are in the mold of universal devices of yesteryear, the OP-07 and the 324. The OP-07 was noted for handling precision tasks, while the 324 was known for its general-purpose and low-power abilities.

The digital self-calibrating TLC4501 may be the ultimate precision IC op amp because its forebearers, the chopper stabilized IC op amp and the analog auto-zero IC op amp, never really caught on. That may have been due to the continuous noise from the chopper, the advent of very-low offset voltage op amps such as the OP-07, or the even-lower offset voltage op amps that followed it. On the other hand, their high cost may have done them in. The TI amplifiers offer much better noise performance than the older devices. For example, peak-to-peak input noise from 0.1 to 10 Hz is less than 1.5 µV (typical).

## Op Amp, Heal Thyself

In the simplest of terms, self-calibration in the TLC4501 and its kin occurs during the first 300 ms after power is applied (*Fig. 1*). At power-up, both op amp input pins are switched to ground and the negative feedback loop is opened. During the 300 ms self-calibration period, a successive approximation (SAR) analog-to-digital converter (ADC) inside the TLC4501 measures the offset voltage and stores it in a register.

When conversion and storage are complete, the op amp inputs are reconnected and the digital word in the SAR register representing the offset voltage is applied to the CAL-DAC (Calibration digital-to-analog converter. It's also the DAC in the SAR ADC.). The CAL-DAC's output current is applied to the op amps input via the current mirror formed by FETs M30/M31 (*Fig. 1, again*). The self-calibration circuit bucks out the offset to less than 100 µV worst case (offset for some family members runs under 40 µV). Moreover, the offset after calibration is repeatable to within 3 µV following successive calibrations. The circuit handles offsets up to 5 mV.

When a calibration (cal) is complete, most of the calcircuitry drops out of the normal signal path through the op amp so that the cal operation and circuits do not interfere with op amp operation or performance.

Generally, a cal is performed only at power up, but a "cal-on-command" is available and could be required if the system's initial conditions change with time or temperature. However, a cal requires removing power from the op amp for over 300 ms, not a happy thought in most systems. To eliminate the need for cal-on-command, the basic design is optimized for superior dc characteristics. As a result, offset voltage drift vs. temperature is less than 1 µV/°C, while bias current runs 1 pA, CMRR (Common-Mode Rejection Ratio) is specified at better than 90 dB, open-loop gain typically comes in at better than 120 dB, and PSRR (Power-Supply Rejection Ratio) runs 90 dB.

Since the precision data acquisition systems for which this op amp is aimed often see a wide range of dc common-mode voltages, a CMRR at dc on the order of 120 dB is often necessary.

While they run off 5-V rails, these self-calibrating op amps also offer virtually rail-to-rail output characteristics, swinging their output within 100 mV of either rail. Moreover, they can drive loads of less than 1000 Ω and maximum output current runs 50 mA. For short-circuit protection, output current cuts off if the load draws +60 mA or -70 mA for more than 1 µs.

Other TLC4501/02 specifications

suiting it for universal precision applications include good ac specifications. For example, unlike many precision op amps, it easily handles high frequency sine waves. Unity gain bandwidth approaches 5 MHz, full-power bandwidth is rated 1 MHz, and at 10 kHz, THD (total harmonic distortion) driving 1000 Ω with 2.5 V, runs less than 0.08%%. It also handles high-speed pulses. Slew rate is specified at a minimum of 1.5 V/µs, and the output settles to 0.01% of final value in 2.2 µs.

The TLC4501/02 are not micropower op amps like the Maxim family of devices, but they're not power hogs, either. A single op amp typically requires just 1.5 mA from a 5-V supply.

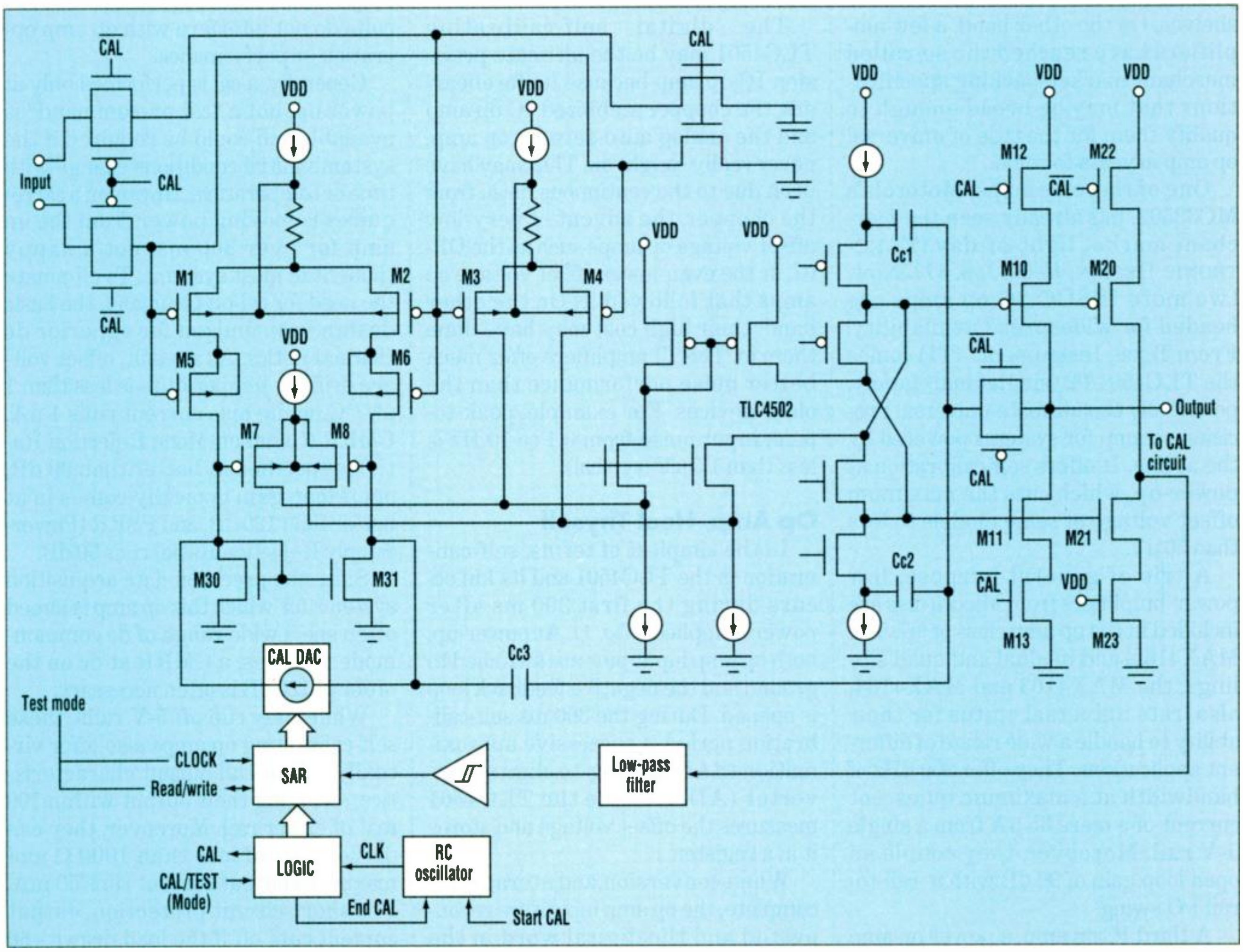
## Digitally-Compatible CMOS

The TLC4501/02 amplifiers are built on a 1-µm digital CMOS process. They use no bipolar transistors or JFETs (*Fig. 1, again*). They represent a general purpose precision op amp that can be incorporated in a mixed-signal "system-on-a-chip." Alternatively, both the technology and the architecture lend themselves to a custom system-oriented design that can correct for system offsets, and/or cal-on-command.

To achieve high performance, TI's IC design team chose a three-stage topology with two gain stages followed by the rail-to-rail complementary common source class AB output stage *(Fig. 1, again)*. To maximize CMRR, the input MOSFET pair, M1 and M2, are cascoded by MOSFETs M5 and M6. The extra FET input pair, M3 and M4 bypass the 2nd amplifier stage at high frequencies to improve closed-loop stability. This typical analog circuit-design "trick" mandates matching the transconductance of M1 and M2 with that of M3 and M4.

MOSFET switches the M12 and M13 output node into a high impedance state during cal. The full-scale output current from the CAL DAC runs about 10% of the input FET 's "tail" current. It modulates the current in each input FET to adjust the offset. As noted earlier, during cal, the op amp is completely removed from the signal path. The output transistors (M10 and M11) are cut from the power rails leaving the output floating while the small replica FETs (M20 and M21) provide the op amps' output signal to the CAL circuit. Compensation capacitors Cc1, Cc2, and Cc3 are no longer required because the feedback loop is open. The op amp runs open loop and acts as the ADC's comparator.

An on-chip RC oscillator (bottom of figure) runs the SAR algorithm during cal. As the offset voltage approaches zero, the op amp enters its linear operating range. Due to the circuit's high gain and wide bandwidth,




**1. An on-chip SAR-ADC performs self calibration in the TLC4502 op amp at power up. It measures the IC's offset voltage, stores it digitally in a register and when calibration is complete, applies it to the CAL DAC the output of which nulls the input offset voltage via current mirror M30/M31.**

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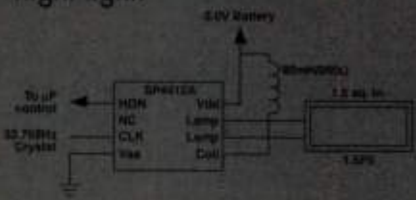

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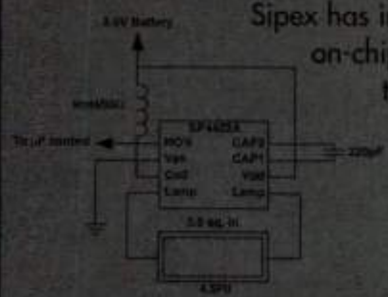

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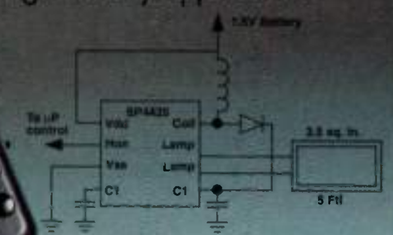

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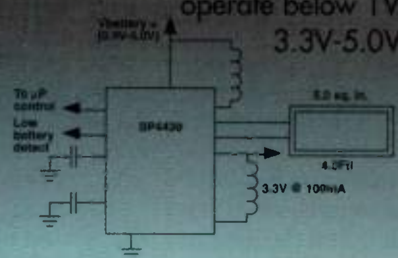

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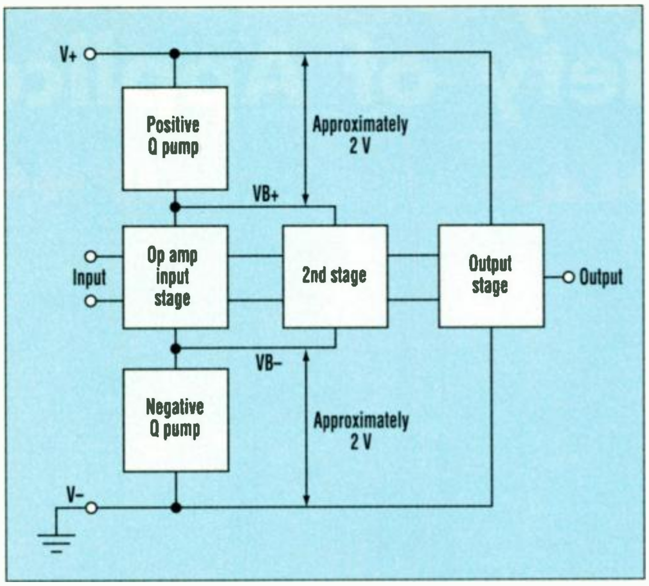
high-frequency noise may drive the output from rail-to-rail, potentially limiting the accuracy of the offset, nulling operation. To eliminate this problem, the IC's designers inserted a low-pass filter, followed by a Schmitt trigger, between the op amp's output and the SAR.

## Micropower R-R I/O

Most op amps today perform tasks that a few years ago would have been done by an amplifier built with a couple of discrete transistors. Now, it's easier, quicker, and—from a system point of view—cheaper to just buy an op amp, drop it in, and forget about any circuit design. And most applications require just a few dB, or at most tens of dB, of gain at frequencies between dc and a few tens of kilohertz.




**2. A pair of charge pumps (Q pumps) in the MAX4162 provide the op amp with rail-to-rail input specifications by boosting the plus and minus supply rails (V+ and V-) by approximately 2 V.**

In the days of split-V supply rails, the 741 and the 324 could easily drive 1000-Ω loads with a few volts (peak-to-peak). Today, as supply rails drop in both voltage and quantity (no more split supplies), and low-power portable systems abound, designers demand single-supply, micropower, general-purpose op amps that offer rail-to-rail input and output while driving a practical load. And the Maxim MAX4162 op amp family handles those applications well.

These devices offer the analog system designer, who must beg for every pA of supply current, a device for many general-purpose op amp applications. For example, while aimed at portable systems, a few of these op amps could drop into a line powered system, upgrading it (or fixing a mistake) without demanding a review of the power budget. Not only do they offer a unity-gain bandwidth of 200 kHz, but they provide this bandwidth at a maximum quiescent current of just 35 µA from a single 5-V rail.

As if that were not enough, these op amps offer rail-to-rail input and output from either a single 2.7- to 10-V rail or a split supply (1.35 V to 5 V). That is, the specification calls for a CMRR of 76 dB for input voltages from 0.25 V below the minus rail to 0.25 V above the plus rail. The output typically swings to within 30 mV of the plus rail and to within 18 mV of the minus rail.

Operating conditions for the previous specifications and those that follow occur while running off a 3-V rail with a 10-kΩ load connected to 1.5 V. Typically, while putting out 1.4 mA, the output can still swing to within 150 mV of the plus rail and closer than 250 mV to the minus rail. Maximum output (short-circuit current) runs 15 mA.

The op amp's designer did not sacrifice basic op amp specifications to achieve wide-bandwidth, and rail-to-rail I/O coupled with single-supply micropower operation. That is, it's a "real" op amp. Typical offset voltage is rated at less than 1 mV, offset temperature coefficient is less than 2 µV/°C, and open loop gain is better than 100 dB.

## Pumping Charge

Over the past few years, a number of analog IC op amp designers have taken on the challenge of coming up with a device whose input could swing beyond both rails. Early attempts were in bipolar processes, and more recently—as high-performance CMOS op amps became popular—in CMOS. To achieve rail-to-rail inputs, IC designers, using both processes, created two relatively conventional long-tailed pair (differential) input stages operating in parallel. One stage uses p-type transistors (pnps or p-channel FETs) the other uses n-type transistors (npns or n-channel FETs). The n-type devices handle input signals more positive than the plus rail, the p-type devices take on signals more negative than the minus rail.

All of these op amps perform their basic task of providing a rail-to-rail input. However, most early amplifiers suffered from severe crossover distortion around zero. That is, as operation shifted between p- and n-type devices, offset voltage often changed significantly at the shift point. Newer rail-to-rail input op amps call for trimming the offsets of both input stages closely to zero to beat the problem (an expensive process). In a more recent attack on the problem, the designer substituted an n-channel depletion-mode FET for the p-channel FET, thus demanding a nonstandard CMOS process.

The designer of the MAX4162 family took a different tack. He kept a conventional differential input stage but added a pair of charge pumps (Q pumps) that produce VB+ and VB- (*Fig. 2*). The regulated output of the two charge pumps raise the supply voltages for the input stage, the folded-cascode second stage and the gate-drive voltage for the output (3rd) stage, approximately 2 V above and below the signal-referenced supply rails, V+ and V- which tie to the op amp's pins.

That is, if operating from a single 3-V supply, the plus and minus supply rails for the op amp's first two stages sit at +5 V and-2 V, respectively. In addition, the gate drive (gate-to-source voltage) for the plus and minus output stages can be greater than their drain-to-source voltage.

If a designer is familiar with charge pumps, it's the obvious way to provide an op amp with rail-to-rail input specifications. But it's not easy to put Q-pumps on a chip with an op amp. It has been tried before, albeit unsuccessfully, because the noise developed by the pumps when they switch the input supply rails can become a major problem. In these op amps, the switching noise appears on the boosted supply rails, but only 100 μV of it rides on the op amp's output.

The op amp's 200 kHz unity-gain-bandwidth also helps eliminate that noise problem. That's because the noise typically runs between 500 and 700 kHz, well beyond the op amp's bandwidth. Moreover, it's coherent, so it can be filtered from a signal simply by adding a capacitor in parallel with the feedback resistor.

The noise also is output-related and does not change with closed-loop op amp gain. A low-pass filter between the output of each pump and each boosted supply rail helps keep the noise on the op amp's output below 100 μV. Most op amps boasting of rail-to-rail outputs employ gain in the third (output) stage, taking the output from the common collectors or drains of complementary output transistors. Such op amps with three gain stages are more difficult to compensate. Instead, the Q-pumps contribute to the op amp's rail-to-rail output performance. As noted earlier, they increase the gate-drive voltage of the common-source connected, output-stage MOSFETs, thus turning them on harder with smaller signals.

## PRICE AND AVAILABILITY

*Heeding its broad general application, as well as its aim at portable applications, Maxim's MAX4162 has been crammed into a tiny 5-pin SOT-23-5 and also into the more common SO-8 package. It operates over the "extended" industrial temperature range of -40 to +85°C. It runs with as much as 10 V between its supply pins. In quantities of 1000, pricing starts at $0.75 each. In similar quantities, the dual MAX4163 goes for $1.20 each, while its quad sibling the MAX4164 goes for $2.10 each (that's less than 53 cents per op amp). Small quantities are available from stock.*

*Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, Calif., (408) 737-7600.*

*The dual version of Texas Instruments self-calibrating op amp the TLC4502 comes in the common 8-pin SOIC. In quantities of 1000, the C version, which offers a maximum offset voltage of 100 mV and operates over the commercial temperature range, goes for $1.18 each. Small quantities of the single, dual, and quad versions are available from stock.*

*Texas Instruments Inc. Semiconductor Group, SC-96061, Literature Response Center, P.O. Box 172228, Denver, CO 80217; (800) 477-8924, ext. 4500.* **CIRCLE 551**

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PRODUCT INNOVATION

# Power Op Amps Sport Rail-to-Rail I/O Control Up To 3 A At 70 V

*General-Purpose Power ICs Handle 0.5 A And 3 A, Driving 22 Ω And 136 Ω While Operating From A Single 70-V Supply.*

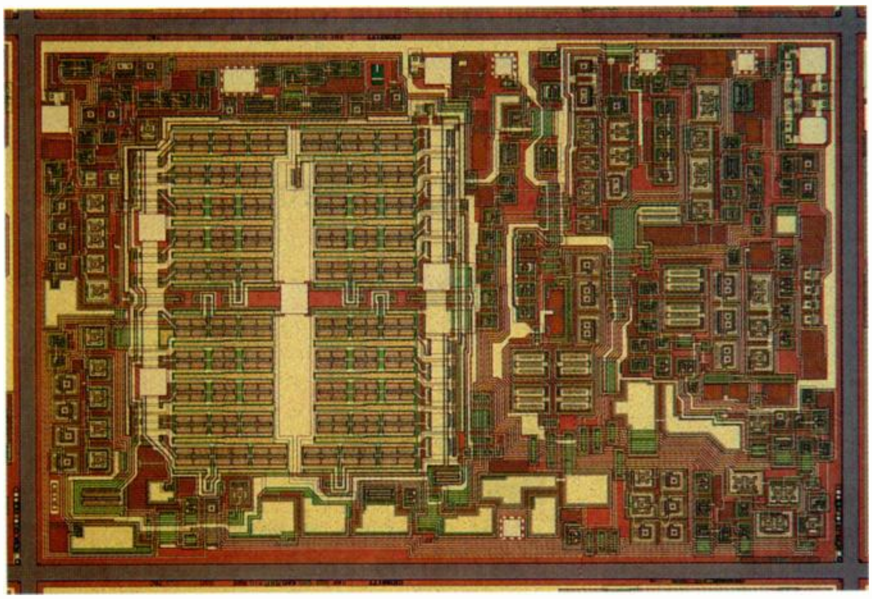
**Frank Goodenough**

When most system designers think power ICs, they think switching devices such as simple MOSFETs with self-protection features, high-voltage MOSFET drivers (virtually all of which sport on-chip self-protection), pulse-width-modulated (PWM) motor drivers, complete PWM switching regulators, or even linear-voltage regulators such as the low-dropout (LDO) regulator. However, there is another kind of linear-power IC, the power op amp. And a pair of op amps from Burr-Brown, the OPA547 and OPA548, are truly power ICs *(Fig. 1)*.

However, most power op amps lack features that users of many small-signal op amps today take for granted. But Burr-Brown's OPA547 and OPA5481 offer three such features:

- Single-supply operation. These ICs operate with the positive supply rail anywhere between 8 V and 70 V, if the negative supply rail is at 0 V.
- Rail-to-rail input. The input commom-mode voltage can swing from 100 mV below the negative rail to within 3 V of the positive rail and still perform in a linear mode while providing a common-mode rejection ratio (CMRR) of 80 dB.
- Rail-to-rail output. While continuously putting out 3 A, the OPA548's output can swing from 3.5 V above the negative rail to 3.7 V below the positive rail. While continuously putting out 500 mA, its lower-power sibling, the OPA547, can swing its output from 1.6 V above the negative rail to 2.2 V below the positive rail.

Both the OPA547 and OPA548 also offer the system designer two features not found in most power op amps: A programmable current limit, and a shutdown pin that also indicates the status of the on-chip thermal shutdown circuit.



**1. The two power transistors in the Burr-Brown OPA547 op amp (large blocks) each consist of 120 individual BJTs, each with an emitter ballast resistor.**

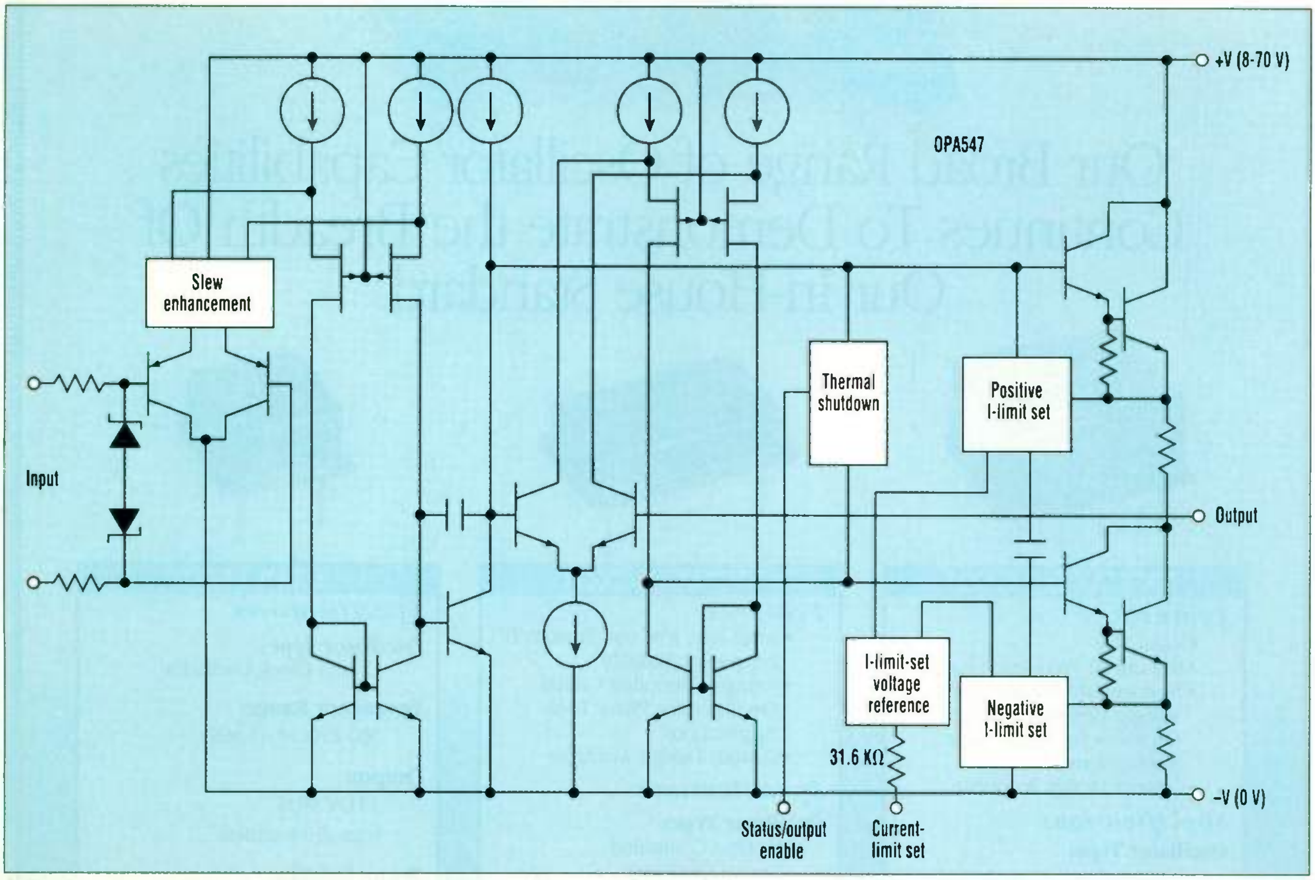
Aimed at applications ranging from low-power, programmable power supplies and servo-motor drivers to audio amplifiers, these are real op amps. Neither dc nor ac specifications have been sacrificed to achieve operation from a single-supply rail and provide rail-to-rail I/O. For example, while operating from split ±35-V supply rails, both op amps sport a maximum offset voltage of ±5 mV that varies just ±25 µV/°C, and a typical voltage noise of 90 nV/√Hz. While driving 10 Ω with 60 V p-p, the 3-A OPA548 features a typical open-loop gain of 90 dB, a typical gain-bandwidth product of 1 MHz at a gain of 1, a slew rate of 10 V/µs, typical full-power bandwidth of 54 kHz, and total harmonic distortion (THD) at 1 kHz of 0.05%. Its 500-mA sibling, the OPA547, offers similar or better performance. While the continuous current rating of the OPA548 runs 3 A, the chip handles peak output currents of 5 A. The 500-mA OPA547 handles peaks of 750 mA.

As noted above, conventional split-supply operation also is possible. But it need not split at 35 V, because both op amps operate with as little as 8 V between the supply pins. The positive rail could be set at 65 V and the negative rail at -5 V, or vice-versa. Alternatively, the devices can still run in a digital system if powered from a 3.3-V logic rail and a negative ECL rail.

Quiescent current draw under no load conditions is not a critical issue. Still, it's less than ±12 mA maximum and that typically drops to 4 mA during thermal shutdown.

## Fancy Features

Both the OPA547 and OPA548 offer the system designer several features not found on all power op amps. These include a DAC/resistor programmable current limit and a shutdown (or output-enable) pin that also displays the status of the on-chip automatic thermal shutdown circuit. The automatic ther-




**2. The Burr-Brown OPA547 op amp sports user-programmable current limits which can be set digitally by connecting a voltage or current DAC to the current-limit-set pin. The status of the thermal shutdown circuit is another feature available to users.**

mal shutodwn circuit is mandatory today on power ICs of all flavors.*(Fig. 2)*.

Connecting a voltage or current DAC (or a resistor tied to the negative rail) to either chip's current-limit-set pin lets the user program the current limit digitally with a DAC (referenced to the negative rail). Alternatively, the user sets a fixed current with a resistor connected to the negative rail. Tables on the data sheets define the resistor value, or the DAC current or voltage, for a wide range of currents between 0 and currents above each chip's rated current. Leaving the pin open cuts the current off at zero. Connecting it to the negative rail sets the OPA547 current at 750 mA and the OPA548 current at 5 A, limiting their peak currents.

The 31.6 kΩ resistor located between the current-limit-set pin and the I-limit-set voltage reference is trimmed to provide those maximum current limits *(Fig. 2, again)*. The positive and negative I-limit-set circuit blocks cut off the drive to the npn output stages when the current limit is reached.

During normal operation, the dual-function Status/Output-Enable pin normally sits at least 2.4 V above the negative rail. It can be left open or pulled to that voltage. Pulling the pin low (to at least 800 mV above the negative rail) disables the output in under 10 µs. The thermal shutdown circuit goes into operation when the die temperature hits approximately 160°C. It resets when the die has cooled to 140°C. The voltage on the status pin drops to 800 mV above the negative rail when the thermal shutdown signal kicks in. Note that all voltages on the Status/Output-Enable pin are referenced to the negative rail. If these op amps are running off a single positive supply (with the negative rail connected to 0 V), their logic voltages are compatible with most of today's logic. However if the op amps are running off split or negative supplies, the negative rail may be -70 V. In that case, special circuits (provided on the data sheet) will be required to interface with any conventional logic (optical isolators may be the simplest way).

The op amps are built on a 70-V bipolar process that allows vertical npn and lateral pnp transistors, as well as p-channel JFETs. The OPA547 and OPA548 differ chiefly in the size of their output transistors. The OPA547's output transistors take up a little less than half the die while those in the OPA548 take up about 70% of its die. Each of the npn output transistors in the OPA547 consists of an array of 120 individual transistors, each with its own emitter-ballast resistor *(Fig. 1 again)*.

## Price And Availability

*The OPA547 and OPA548 come in the staggered-lead, 7-pin, TO-220 package and the 7-lead DDPAK for surface mounting. Their specifications hold over the extended industrial temperature range and they can operate over the military temperature range. In quantities of 1000, the OPA547s go for $4.09 each. In similar quantities, the OPA548s are priced at $5.45 each.*

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# Optimizing Compiler Technology Streamlines Complex Systems

*Embedded Applications Are Driving The Evolution Of Optimizing Compilers That Speed Up Software Development And Simplify Code Debugging.*

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Today's high-quality optimizing compilers have made assembler language programming necessary only to access special processor instructions. Compiler technology continues to advance, bringing with it advantages for embedded-software applications for mainstream processors that will be brought to market in the near term.

A complete software development environment consists of a compiler, assembler, linker and debugger, object-module display tools, debug information stripper, source editor and browser, "make" or other project management facility, and object-code libraries. Desktop environments such as those from Microsoft or Borland are tightly integrated. They feature a rich, interactive, fully integrated set of development tools, all accessed from a single graphical user interface. Templates for standard functions are offered. The editor is language-aware, and guides the user into the most appropriate context for editing his or her program.

The user interfaces of environments used for embedded development still lag their desktop counterparts, but they do offer support for a wider variety of execution environments. Embedded development is almost always cross-compilation. The compilation system runs on a host system, and the program being developed is intended to run on an embedded CPU in a custom execution environment. The challenge is to make the bridge from host to target invisible. A seamless connection between host and target boosts productivity more than a slick environment on the host. Code compiled and linked on the host should be conveniently downloaded to the target. The host-side debugger should be able to readily examine and modify code and data using symbolic notation.

Compilers for embedded development are based on the same technology as desktop and workstation environments. However, they are required to provide better access to the hardware. The following nine compiler features are common:

• Robust support for writing in-line assembler within high-level language

**COMPILER OPTIMIZATION TECHNIQUES**

| Optimization | Local | Function-level | File-level | Program-wide | Profile-driven |
|---|---|---|---|---|---|
| Peephole optimization | ✓ | | | | |
| Tail-call elimination | ✓ | | | | |
| Memory-access coalescing | ✓ | | | | |
| Constant folding and propagation | ✓ | ✓ | | | |
| Common subexpression elimination | ✓ | ✓ | | | |
| Strength reduction | ✓ | ✓ | | | |
| Loop-invariant code motion | ✓ | ✓ | | | ✓ |
| Instruction scheduling | ✓ | ✓ | | | |
| Dead/unreachable code elimination | ✓ | ✓ | ✓ | ✓ | |
| Register allocation | ✓ | ✓ | ✓ | ✓ | ✓ |
| Parameter passing in registers | ✓ | ✓ | ✓ | ✓ | ✓ |
| Branch optimizations | | ✓ | | | |
| Variable live-track separation | | ✓ | | | |
| Global variable migration to registers | | ✓ | | | ✓ |
| Loop unrolling | | ✓ | | | ✓ |
| Function inlining | | ✓ | ✓ | ✓ | ✓ |
| Superblock formation | | | | | ✓ |
| Basic block rearrangement | | | | | ✓ |

functions for performance-critical code or providing access to specialized hardware.

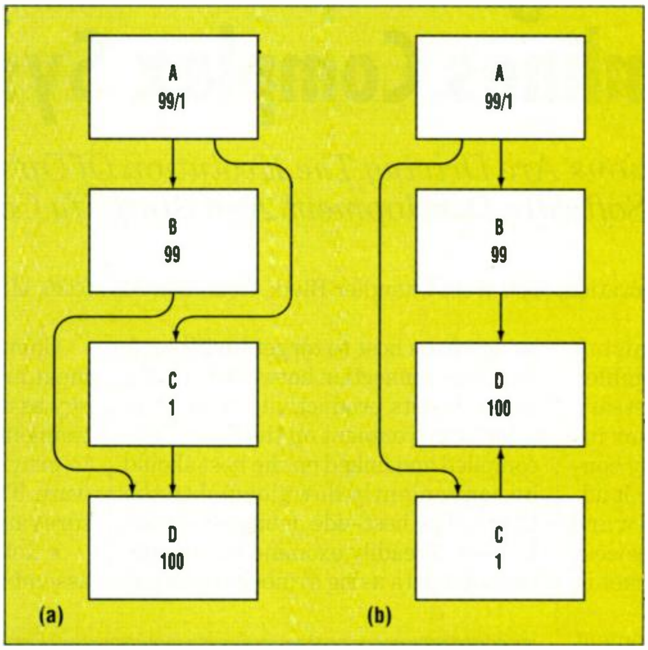
- Correct implementation of the volatile keyword in the presence of compiler optimizations so that hardware registers may be accessed and modified reliably.
- The ability to create position-independent code when a memory-management unit is unavailable.
- Support for thread-specific or task-specific data sections to enable creation of reentrant programs.
- Facilities for burning code into ROM.
- Direct support in the compiler for writing interrupt routines.
- Well-defined Application Binary Interfaces and object module format standards to allow interoperability of development tools from independent vendors.
- The ability to interface with real-time operating systems.
- The ability to customize structure layouts and alignments of data objects.

There are many categories of programming languages: functional languages designed for symbol manipulation, interpretive languages such as awk and perl, languages designed for set manipulation, parallel programming languages, and so on. C and C++ are likely to dominate embedded software development for the foreseeable future. Java has just appeared on the horizon. It promises many of the benefits of C++, and is vastly simpler. There is tremendous appeal in creating a universally executable program using Java. However, it is uncertain if Java's operating environment is viable. The performance hit from interpretation and the additional development and debugging issues raised by adding an interpreter to the mix make it hard to predict the final acceptance of Java.

## Optimization Expectations

An application designer may be more concerned with either speed or memory space. Unfortunately, optimizing for one usually penalizes the other. This tradeoff is particularly true for RISC processors. Most compilers offer switches for selecting code space or run time as the overriding consideration during optimization.

Application run-time performance is usually the chief concern of the designer, but sometimes, particularly in cost-sensitive embedded applications, speed may have to be traded for memory. Frequently, using less memory simply means avoiding optimizations that offer speed ups, but increase code size.




**1. In a basic block-rearrangement scheme, code block C is executed far fewer times than blocks A, B, and D (a). If the compiler has profile information on the relative usage of each block, it can move a seldom-executed block of code so that it is not in the sequence with frequently-executed blocks (b). The cluster of frequently-executed instructions can then run more efficiently.**

An extreme example of code space reduction is offered by some compilation systems that generate compressed machine code. The programmer designates which functions in his program are not time critical (such as error-handling functions), and the compiler or linker compresses the machine code generated for the functions. The compiler generates special code for calling compressed functions. Instead of transferring control to a compressed function, an intermediate routine is called. The routine expands the code of the function (possibly on the stack), before jumping into the code to execute it. Naturally this is slow, but the expectation is that such functions are rarely executed.

Most designers are willing to trade some memory space for enhanced performance. As the size of the source-code window examined by the compiler is expanded, optimizations improve because the compiler can make more informed decisions. Unfortunately, compile time and memory requirements make it impractical to always examine the largest possible window. As the source code window expands, compiler algorithms take ever longer to run, in the worst case, taking exponentially as much time as the size of the window. File boundaries form another barrier. When a compiler begins looking across source files to generate code, dependencies between source files are introduced. A change in one file may require recompilation of other files.

An added dimension comes from introducing run-time profile information into the optimization process. The compiler may tailor its optimizations based on a run-time profile.

## Compiler Optimizations

*Constant Folding and Propagation*—Programmers rarely write expressions containing only constants, but constant expressions arise from the use of symbolic constants. Constant folding occurs when the compiler recognizes expressions with constant operands and performs the computation at compile time. Constant propagation takes known constant values of variables and substitutes them into later references to the variables. The two techniques feed on each other. Folding can lead to recognition of variables with constant values, and propagation can yield more folding opportunities.

*Common Subexpression Elimination*—This optimization recognizes and eliminates repeated occurrences of the same computation. After a result has been computed it is saved in a register (if available) or memory, and

reused when needed later. Most programmers avoid common subexpressions, but they can arise from behind-the-scenes code generation for array or structure member references.

*Loop-invariant Code Motion*—In this technique the compiler systematically examines every loop in the program and moves sub-expressions that do not change inside the loop to a point outside the loop where they are computed only once.

*Strength Reduction*—Strength reduction seeks to replace expensive operations with cheaper ones. For instance, a multiply or divide by a power of two may be converted to shift-left or shift-right. Array indexing within a loop may be replaced by a pointer that is incremented with each loop iteration.

*Function Inlining*—Function inlining is the process of replacing the body of a function at its point of call. An immediate saving occurs by eliminating the call-return overhead. Further speed improvement is obtained from elimination of unnecessary checks as described in dead code removal, below. A more subtle, but measurable speed up is derived from improved use of the instruction cache.

*Dead Code Removal*—This optimization removes code that cannot be reached or performs no useful computation. Dead code may occur from maintenance performed on the program. It also may be caused by optimizations such as function inlining coupled with constant propagation. For example, a function may check a parameter value and perform one of several possible actions. At some point the function may be called with a constant parameter value. If the function is inlined, the constant parameter flows into the function body and allows the compiler to strip away all code except that which handles the case selected by the constant value.

*Instruction Scheduling*—For superscalar processors or even processors with queued-memory accesses, rearranging instructions to maximize parallelism speeds up program execution.

*Register Allocation*—Holding values in registers is faster than reading and writing values from memory. Efficient allocation of available machine registers is an important compiler optimization. A programmer coding in assembler language can manage machine registers quite effectively up to a certain code size and complexity. Beyond that, a compiler is better equipped to optimize scarce register resources.

*Peephole Optimization*—This optimization consists of minor touch-ups to the code within a two or three-instruction window. For instance, two adjacent instructions may be combined into a single, more complex instruction. Separate compare and branch instructions can be merged into a single compare-and-branch instruction.

*Processor-specific Optimizations*—As the name implies, these are specific to a particular processor, and may range from simple peephole optimizations to specialized instructions to perform complex operations. For instance, using a block-move instruction to replace a call to "memcpy."

*Loop Unrolling*—This technique reduces the cost of setting up a loop relative to performing useful work within it. By replicating the body of the loop multiple times, the number of iterations of the loop is reduced, lowering the number of instructions wasted in managing the loop itself.

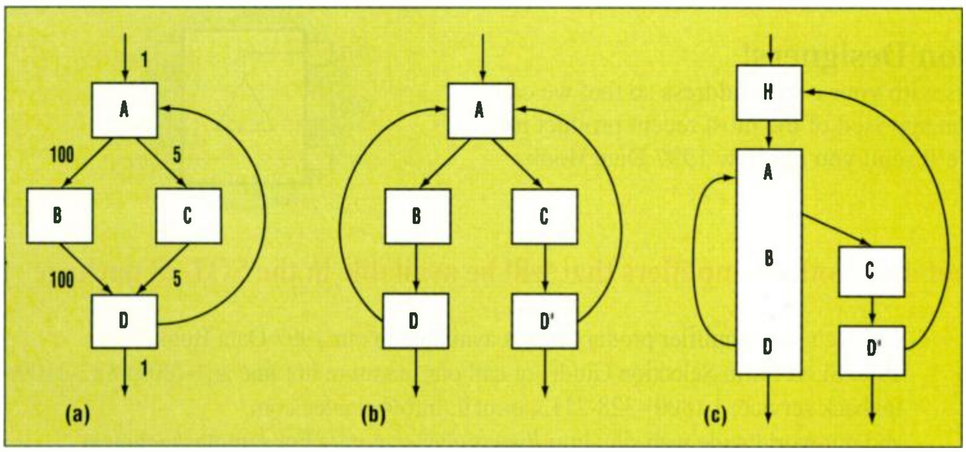
A summary of optimization techniques categorized by the source code examined is given in the table. Some optimizations are feasible only when profile information is available. Others are improved by profile information.

## Performance Profiling

The ability to profile application programs is included in most compilation systems. Profiling is either statistical or precise. Statistical profiling is less intrusive, but the information is approximate. Precise profiling is intrusive, but yields better information.

Statistical profiling uses a periodic timer interrupt. The code space of the program is divided into equal sized buckets with a counter associated with each bucket. At each timer tick the program counter value is used to select the associated bucket and its counter is incremented. Running the program for a sufficient length of time produces a statistical program profile. The data is typically displayed as a histogram of source function versus time. This profile is useful in identifying hot spots in the program for hand-tuning. However, since the hierarchy of function calls is not captured, a low-level utility routine may show up as heavily executed, with no indication of which higher-level routine is causing the frequent execution.

Some compilation systems offer a compiler-code generation option that generates extra code to collect execution counts. A simple approach places code to increment a counter in each basic block. More sophisticated compilers select a strategic subset of basic blocks from which complete and precise execution counts of




**2. In superblock formation, the compiler replicates certain blocks and trades an increase in code size for larger blocks of code that can be optimized more effectively. Since block C executes fewer times than block B (a), the compiler moves C out of the loop in a series of steps. A new block, D', is cloned from block D (b). And from D', an new empty block, H, is created that permits C to be moved out and a superblock to optimize the sequence of instructions (c).**

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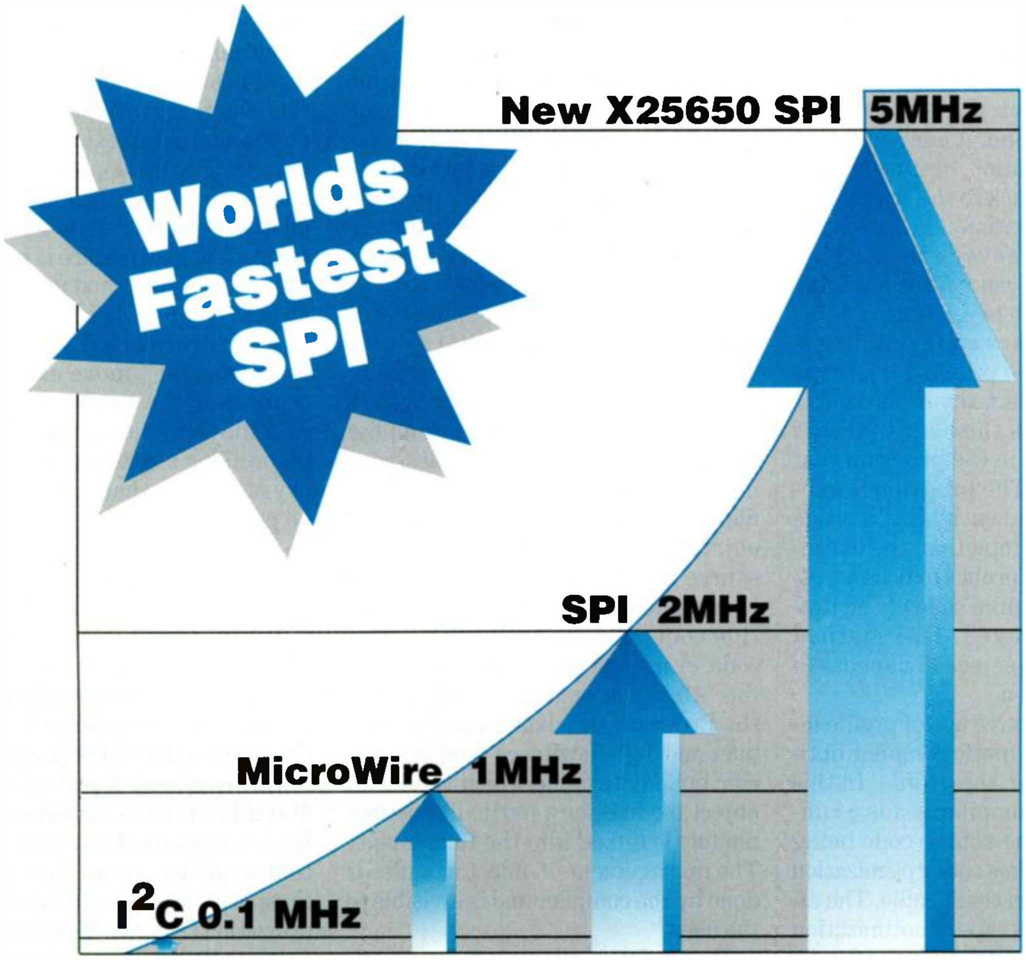


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A variation on precise profiling is user-instrumented profiling. The compiler does not insert any probes on its own. It requires the user to insert probes at points in the program that are of interest. The program is executed as usual and each hit of a probe is counted. At completion, the execution counts of the probes may be correlated with the source code of the program and displayed. This method highlights user-selected aspects of program execution.

The most effective use of profile information is automatic compiler optimization based on the profile. In this technique, the compiler reads a runtime profile of the source code being compiled and makes code optimization decisions based on that profile. The effectiveness of this type of optimization has long been recognized in academia, but industry adoption has been slow for a number of reasons. Recently, however, most of the barriers to using profile-driven optimization have been removed.

Although simple in concept, profile-driven optimization presents substantial management issues that have made it difficult for users to adopt:

- Two compilation steps are needed—the instrumentation step and the recompilation step. Users are required to ensure that their sources do not change between these steps.
- There are two sets of object files to manage—instrumented objects and recompiled objects. In a traditional makefile environment this is possible only with manual and error-prone shuffling of object files.
- A change in even a single source file renders a profile useless since there is such a tight correlation between the instrumentation counters and the source code.
- Incremental profiling, or collecting a profile of a subset of the source files at a time, is not supported.

Recently, production compilation systems have appeared that solve all of these problems. The solution has been to redesign the user interface to support automated object-module management and source-file dependency analysis, and to store the profiles in a more flexible format.

The development of a sophisticated object-module management system with integrated source code dependency checking, was a breakthrough in simplifying profile-driven compiler optimization. A Program Database, implemented as a directory on a host file system, stores multiple versions of object modules derived from a single source module. Source modules may be compiled with profile instrumentation code, may be built with debug code, or may be optimized using a profile. All object modules reside within the Program Database, and the compiler and linker switches used in a specific build determine which version of object module for a particular source module is linked into the final image. The management of object modules is done by the compiler and is invisible to the user.

Dependency analysis is automatically performed by the system. For instance, if a source module has changed then the module is recompiled before it is linked into the program. However, if there are effects of the changed source on other source modules, then those modules also are recompiled before being linked into the program. Only those recompilations are performed that are required by interfile dependencies.

Since multiple versions of object modules are stored in the Program Database, it is always possible to find a reusable object module, even though the last build of that module used different compiler switches. For instance, substitutions can be used to alternate between debug and optimized program versions, with both versions of the object modules transparently stored and retrieved from the Program Database. Few or no compilations might actually be issued to obtain a requested program version, depending on the source changes made to the program.

Allowing profiles to be reused after small program changes was another significant improvement in the usability of profile-driven compilation. With this capability profiling may be incorporated into the test and debug cycle, or even the development cycle, without requiring that profile-driven compilation be preceded by a profile-gathering step. This feature is based on the concept of a stretched profile, wherein an existing profile is extrapolated to fit a slightly changed source program. Naturally, the more extensive the changes to the source, the less accurate the stretched profile. Incremental profiling also is supported. If memory is so tight that a program cannot be profiled all at once, a full profile can be obtained by collecting profiles for disjoint program pieces, and then merging the partial profiles.

Some of the performance benefits of automatic profile feedback can be illustrated with two optimization examples that are only feasible with runtime knowledge of the program.

*Basic Block Rearrangement*—Matching the execution sequence of basic blocks (in time) with their textual sequence in the object program (in space) improves instruction cache utilization (*Fig.1a*). The example illustrates the rearrangement of an *if-then-else* statement in which the *then* part is executed much more frequently than the *else* part. The *if* condition is represented by block A. The *then* and *else* parts are blocks B and C, respectively. Block D represents the statements after the *if-then-else* statement. The numbers within the blocks indicate execution counts (true/false counts in the case of the *if* statement). The run-time profile indicates that block B is executed 99 times, while block C is executed only once. Normally, a compiler would lay the blocks down in the order A, B, C, and D. However, with profile information at hand, a better order is A, B, D, and C (*Fig. 1b*). The rarely executed code in block C is moved out of the way. Blocks A, B, and D form a cluster of instructions that is frequently executed.

*Superblock Formation*—A superblock is a single-entry multiple-exit sequence of instructions. Superblock formation is a process of selective code replication to form larger and larger blocks that can be very effectively optimized. For example, the loop formed by basic blocks A, B, C, and D consists of an *if-then-else* statement. At run time the *then* part (block B) is executed 100 times out of 105. The compiler moves block C out of the loop in successive steps *(Fig. 2a)*. Then, block D is cloned to create D' *(Fig. 2b)*. Next, a new empty block, H, is created. D' transfers to H, which falls through to A *(Fig. 3c)*. The structure now consists of two nested loops. Loop A, B, and D is nested within loop H, A, B, D, C, and D'. Finally, blocks A, B, and D are merged into a single superblock that may be optimized without interference from block C.

## Debugging Aids

An important consideration when evaluating a compilation system is debugging support. Regrettably, as the code is more aggressively optimized it becomes more obscure and harder to debug. The ability to debug optimized code is very useful in reducing time-to-market of production software. There are two main schools of thought when it comes to debugging optimized code—truthful behavior and expected behavior.

In providing expected behavior, the compilation system is determined to present the user with a view of the program that is based exactly on the source code as written. No recourse is needed to the generated code. The user may examine and modify variables, set breakpoints at source statements, and step through the program just as though it had been naively compiled to maintain a one-to-one relationship between source code and object code. As one might imagine, maintaining this illusion becomes harder as optimizations increase, variables migrate between registers and memory, and code is rearranged and deleted. Many solutions for modeling common compiler optimizations are available, and this is an area of active academic research. However, providing expected behavior is not always possible.

Truthful behavior is the other extreme. It takes a pragmatic approach, involving the user in the optimizations performed, forcing him or her to debug the program as it appears in the generated code. This approach is easier to implement, but not very user-friendly. The debugger may often suppress information when it cannot guarantee its correctness.

The best approach combines the expected behavior with truthful behavior. As long as possible, expected behavior is provided. When information is lacking or an operation requested by the user cannot be performed, the debugger falls back to truthful behavior. With newer object-module formats such as IEEE-695 and ELF/DWARF, considerable flexibility is available to the compiler to represent the mapping between source and object code. A usable debugging environment may be provided in the presence of extensive compiler optimization.

**As processor architecture departs from the traditional scalar model, the burden on the compiler increases.**

The DWARF debugging information format specification is rich enough to meet the needs of source-level debugging of all major programming languages. Two important issues are addressed by DWARF: the mapping between program variables and their machine representations, and the mapping between source statements and the machine instructions that implement the statements.

To adequately capture the location of a variable through its lifetime, DWARF has location expressions and location lists. Location expressions allow a variable's location to be determined in a language-independent manner even if complex addressing mechanisms are used. Location lists allow a variable to move back and forth from memory to register(s), yet provide the debugger with precise information about the location of the variable at any point in the program.

To deal with compiler optimizations that add, delete or duplicate code, DWARF has the ability to express a many-to-many relationship between source statements and machine instructions. Thus, if a function is inlined at multiple sites, setting a breakpoint at a line in that function may be handled by the debugger by setting breakpoints within each instance of the inlined function. DWARF also can deal with optimizations that produce shared code (e.g. common subexpression elimination) and optimizations that eliminate code altogether.

## Future Trends

Some of the newer processor architectures such as digital-signal processors (DSPs), present a challenge to C and C++ compiler writers. C and C++ were designed for conventional processors. Their expressions and control structures map easily on to the processor's instruction set. In fact, direct access to the hardware was one of the goals of the designers of C. As processor architecture departs from the traditional scalar model, the burden on the compiler increases. At the next level of complexity, superscalar processors require that the compiler keep separate issue paths busy. More specialized architectures such as DSPs cause compilers significant problems.

Most DSPs are single-instruction-multiple-data processors, that is, a single instruction has the capability of operating on multiple pieces of data in parallel. To exploit these architectures while compiling standard C or C++ programs requires that the compiler extract parallelism in the program. This function is difficult, and most DSP algorithms tend to be coded in assembler language. Very-long-instruction-word (VLIW) processors, as well as multiprocessors exacerbate this problem. This is an area of active academic research.

Compiler optimization technology will continue to evolve with processor architecture. In the past, processor designs were undertaken without much consideration for the compiler. Large areas of silicon were underused because designers neglected to take compilers into consideration. However, compiler and processor interdependence is increasing. Early RISC architectures placed a considerable burden on the compiler to exploit the performance potential of the processors. The newer VLIW-style architectures make compiler awareness imperative if the processor is to be utilized to its capacity.

The embedded area has traditionally lagged the desktop by several years. In the past, retired or unsuccessful desktop processors have found their way into embedded applications. This environment is quickly changing. The processing demands of embedded applications are accelerating. Mainstream desktop CPUs will find their way into high-performance embedded applications ever sooner. As a consequence, desktop development environments will be used in the embedded arena, as well.

The rich, graphical user interfaces that we have come to expect on the desktop will be taken for granted in the embedded arena. Tighter integration between host and target tools will shorten the software development cycle. Debugging of optimized code also is going to be increasingly important. Software developers will demand the ability to optimize their code, yet not give up debugging capabilities. To shorten software development cycles, compiler optimizations will be enabled from the start. Performance demands will result in whole-program and profile-driven compiler optimizations entering the mainstream. Overall, increasing performance and usability demands placed by software developers as well as continued evolution of processor architecture make this an active area both for research and for deployment of commercial software development environments.

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# CASE Tool Automatically Generates Code From Graphical Designs

A new CASE tool uses a newly developed standard notation to design and analyze object-oriented software, visually animate execution behavior, and automatically generate code from designs. Dubbed Rhapsody by iLogix, the tool keeps the activity of developing code at the higher design level for as far into the project as possible. This addresses the classic conflict between the need to take time to plan a design and the rush to start manually writing code. Given the size and complexity of today's 32-bit embedded designs, iLogix maintains that the only way to achieve reasonable schedules is to concentrate activity on higher-level design.

Rhapsody uses the Unified Modeling Language (UML), which was recently submitted to the Object Management Group (Framingham, Mass.) as a proposal on standard object models and notation. UML is a synthesis of three popular design and notation methodologies: The Jacobson Use Case method, the Object Modeling Technique (OMT), and the Booch notation. These have evolved in UML into, respectively, message sequence charts, object model diagrams, and state charts. Message sequence charts describe interactions between objects and their environment, such as external events, time-outs, and the actions of other objects. Scripts that describe the use case being modeled can be added to a notation column on the sequence chart.

Object model diagrams are static diagrams that describe the elements and relationships that comprise the structure of the system. In an object-oriented scenario, they show class inheritance. State charts model complex event-driven behavior. Tools for expressing behavior, including states, historical properties, transitions, and compound transitional connectors, are available from a tool bar. State charts are hierarchical to show greater levels of detail of state machines within larger objects. Once created, state charts can be animated to validate the behavioral model before code is generated. The UML also includes a management-level browser view of the system which appears as a directory tree showing the relationship between all of the elements in the code. The browser allows viewing, partitioning, and modification of the entire object model.

UML models can be used to automatically generate production C++ source code. Code generation can produce complete executables or specific files such as source, libraries, or make files. Code generation also can be customized to meet the needs of embedded and real-time systems. Rhapsody works with commercially available development environments and compilers. For the Windows95 and WindowsNT environments, it supports Microsoft Visual C++; for SunOS and

*(continued on page 162)*

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*(continued from page 161)*
Solaris, it uses Sun SC3; and for the VxWorks real-time embedded environment, it supports the GNU gcc 2.6-95 compiler. The integration with integrated development environments (IDEs) such as Visual C++ gives the modeling world of Rhapsody access to code editing, management, and debugging facilities bundled with IDEs.

Once code is generated, it can be compiled using one of the third-party tools. Compiler messages can be viewed in a window in the design environment. Clicking on a compiler error takes the focus of the process to the location of the error. The user has a view of the error's area within the design environment and also within the source code.

Rhapsody's animation capability is designed to tightly couple the design (i.e., the high-level graphical representation of the system) to the actual implementation running on the target. Animating the message sequence chart lets you follow the message flow between objects.

State-chart animation displays the behavior inside of objects. The state-chart animation is hierarchical, making it possible to delve deeper into the state transitions that take place within objects. Finally, the animation capability of the project browser lets you follow the changing data values within objects.

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# Simulation Tool Models Nonlinear Dynamic Systems As Building Blocks

A building-block approach to designing and simulating nonlinear, continuous time systems is possible with Simulink 2. Simulink 2 provides a library of several hundred prebuilt blocks that can be selected and connected together using a graphical editor to build a model of a dynamic system. Once built, the model can be run and will generate data to further refine the design. Virtual oscilloscopes can be attached to points of the model to monitor behavior.

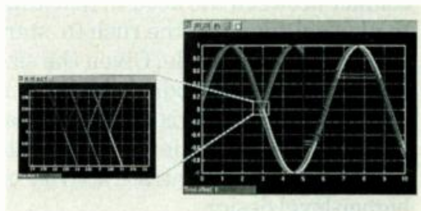
The simulation tool is a response to the need for the accurate modeling of nonlinear systems and in complex control applications for automotive and aerospace design applications. Another sizable application area involves the design of DSP-based systems, such as radar and acoustics.

A large selection of "solvers" for complex differential equations are available. These can model the behavior of a system in continuous time. In addition, the tool provides triggering and enabling state events that can instantaneously change the dynamics of the nonlinear system to replicate real-world conditions. Working with the Matlab 5 design and math analysis tool, Simulink 2 can provide a complete virtual prototyping environment.

Simulink 2 is used by connecting various functional blocks, such as "gain" blocks, filters, integrators, summation blocks, and user-defined custom blocks, to build a model of the "plant" or system to be simulated. Other blocks, such as PID blocks, are used to model a controller that's wrapped around the plant to form a closed-loop system. Matlab 5 provides input stimulus for the model and receives and analyzes the numerical data generated by the simulation.

The combination of complex differential equations for nonlinear simulation with state events gives the tool the ability to model a system's response to changing real-world conditions. For example, a plant may be running under a given set of conditions such as an engine idling with the clutch freewheeling. When the clutch is engaged, a load is placed on the plant and power may be applied. These two events signal discrete state changes that immediately change the nonlinear dynamics of the system. This will require perhaps a new set of differential equations or change the structure of the existing equations to model the new conditions.

Such state changes can be used to design systems that require multiple modes of control, for example aircraft operating at different altitudes and airspeeds or under different flight rules such as combat. In addition, Simulink 2 supports modeling so-called "stiff" systems that may have higher and lower frequency dynamics in the same model. For instance, a system may have high frequency dynamics to model its electrical behavior and lower frequency dynamics to model mechanical behavior.



Simulink 2 is designed to be integrated with the Matlab 5 analysis tool. In fact, it requires Matlab 5 to operate. Simulink 2 models the physics of the system, which can be developed by putting together the blocks from the library or custom blocks written in C, Fortran, or the Matlab language. Matlab may, for example, be used to define a custom control algorithm. That algorithm then can be placed in the controller portion of the simulation.

When the simulation runs, the results can be viewed on one of the virtual scope displays, and the model can be interactively fine-tuned. Alternatively, the numerical data generated by the simulation can be fed back into Matlab 5 for analysis and refinement. The analysis then produces improved control laws that are fed back to the simulation. This iterative process lets users refine their prototype until it works to their liking.

In addition to its general analysis tools, Matlab 5 incorporates a number of toolboxes for specialized design and analysis. These include control design, fuzzy/neural systems, and many others. It also has its own programming language, which generates Simulink blocks from the analysis activity.

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**TOM WILLIAMS**

## *har-bus 64* New 160 Pin Connector For VME64

New connector series satisfies the new 64-bit computer architecture's requirement for higher speeds, more I/O and additional functionality. Offering a five row connector solution that is 100% backward compatible with the popular 96-pin Eurocard connectors, the new ***har-bus 64*** has 160 pins with preleading contacts for live insertion. New contact rows can be used to improve signal speed of VME bus and as ground contacts. Current 96-pin Eurocard connectors mate to the 160 pin connectors, allowing all PCB's to be used in new or existing backplanes.

**READER SERVICE 325**

## *har-pak*®2.5MM High Density Connector system

Developed for backplane and daughterboard applications in modern rack systems. The 5 row 2.5 mm connector design offers solderless PCB terminations, optimum utilization, of space three dimensional modularity, high contact density, EMI protection, and the ability to double-side surface mount components on daughter cards without loss of a 15mm card pitch. The *har-pak* connector system permits using a three dimensional 2.5mm grid. With the exceptional capabilities of the connector, only one connector style is required to solve your power, signal, ground, and high data rates, simplifying the design and manufacturing of future systems. The compliant pin technology utilizes the same 1mm plated through hole standard for many DIN 41612 compliant pin technologies.The consistency in design uses the many years of manufacturing and design experience already available. These attributes combined can lead to new advancements in board-level designs:15mm card pitch with double sided surface mounted daughter cards, butterfly or mid-plane techniques, modular design both horizontally and vertically, low number of system components combination with other standardized packaging systems, and lower applied costs.

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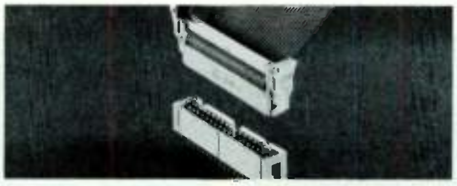
## New SEK "Press'n Snap" Press In Header

The new "press'n Snap" low profile press-in headers can be added to single or double-sided surface mount printed circuit boards any time after reflow. Press-in terminations of the two row .100" pitch headers permit easy installation into plated through holes without soldering. Removable temporary inserts allow any flat die to press the connectors. The straight header is shrouded by four plastic walls and available in versions from 6 to 64 contacts. The mating connectors are flat ribbon terminated socket connectors from HARTING's SEK range. These can be latched to the headers by using the locking levers installed onto the strain relief. The levers secure the socket connector to the end walls of the header. Placing the



locking levers on the socket instead of the PCB header saves valuable board real estate.

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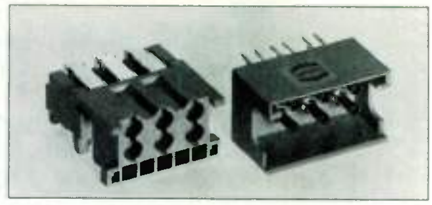
## NEW HIGH DENSITY MICRO-COAXIAL CONTACTS



Designed for high speed data transfer rates. Can be used in the iec 1076-4-2 2.5mm High Density connector system, *har-pak®*. Provides more space efficiency, high frequency capabilitiy, easy handling, low applied cost and application with current equipment and emerging metric equipment practices. Designed for PCB termination on both daughter card to backplane connection; allowing users to bring signal directly into the backplane without a cable transition.

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# CONNECT

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**HARTING's *har-bus 64*** connector series satisfies the new 64-bit computer architecture's requirement for higher speeds, more I/O and additional functionality. Offering a five row connector solution that is 100% backward compatible with the popular 96-pin Eurocard connectors, the new ***har-bus 64*** has 160 pins with preleading contacts for live insertion. New contact rows can be used to improve signal speed of VME bus and as ground contacts. Current 96-pin Eurocard connectors mate to the 160 pin connectors, allowing all PCB's to be used in new or existing backplanes.

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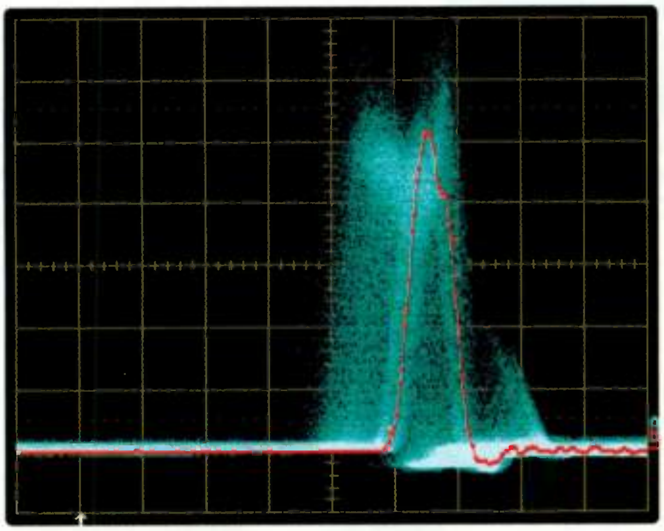

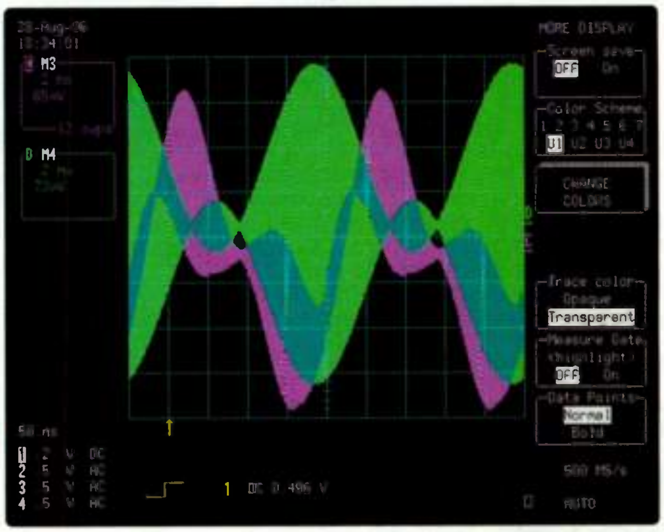


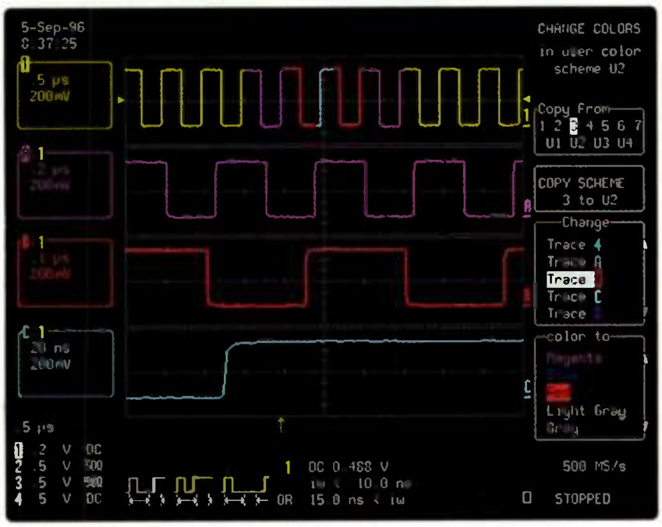


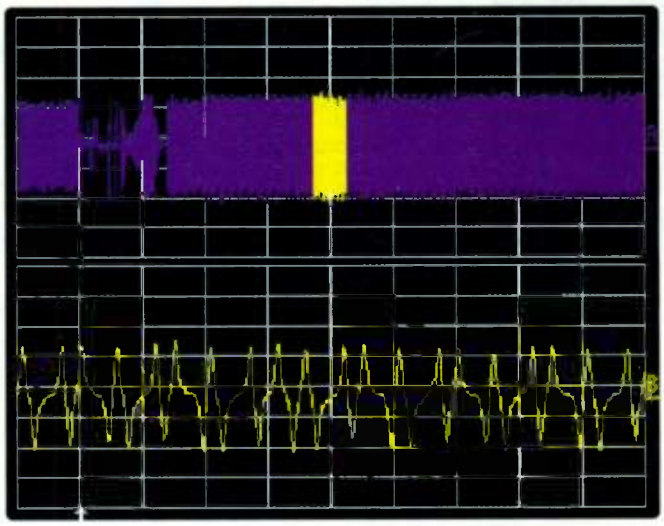

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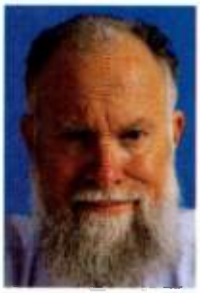
BOB PEASE

# Bob's Mailbox



*Hi, Bob:*

Your column about teamwork inspired me. This letter is about impedance matching, or maybe architecture....

*Pat's Rule #1:* Teams must "happen;" they can be guided but they cannot be *forced* to occur. Very nonlinear.

If we gather the right cohort, the result is almost magical. But the wrong cohort is just a "group;" a team that didn't "jell." It will generate tremendous internal strife and small results; entropy at its finest.

The business community's present approach to teamwork treats everyone like gas molecules: Put enough of them together and maybe "the magic" will happen. It's seeking critical mass but it's getting liquefied employees. *And it doesn't know why.*

Scientific method is supposed to begin with observation, then proceed to hypothesis and testing. Unfortunately, lots of folks skip the observation and proceed directly to the testing. They'd do well to fall back a bit....

Consider groups that occur in nature, like animal packs. Dogs and humans are much alike, so they are a good candidate. Every pack has a leader, an "alpha." No pack has two alpha members for very long; one will be driven away; the remaining members will be subservient. And they will form an effective internal "pecking order."

A pack with small internal strife is a very effective organism. In fact, it's so effective that we humans have laws to protect us from it. Unfortunately, we humans also fancy ourselves "superior" to other animals, so we form our packs arbitrarily, then wonder why they fail.

And we generate endless discussions about the "qualities of leadership" then jam the boss's kid into the alpha position even though he or she has a naturally subservient personality (relative to other members of the pack).

*Pat's Rule #2:* Employees are valuable because if you add one, or take one away, you change the entire nature of the pack. Major transfer function revision. Not necessarily bad, but *way different!*

I don't talk much about this stuff because the people around me generally don't like to picture themselves accordingly. But I do use it as a gauge, especially when I'm seeking an impedance match with a new customer (internal or external). I think of it as the "personality domain."

I look for the "alphas;" the movers and shakers in their organization. And I try to identify the "doers" as well. Each is useful; each is necessary; each can help my company thrive, even if they don't (or cannot) explicitly recognize their own roles.

This pastime also helps me identify (and avoid) organisms with severe internal strife; a strong impedance mismatch; a poor transfer function. They won't succeed until they change, but they could drag my company (my pack) down in the process.

And now the disclaimer: *Pat's Rule #3:* I'm only occasionally correct (but I survive). The operative posture is the "observation" mode; I try to stay there as much as possible. And I try to inhibit my ego. Your readers can respond to this letter at *71501.2521@compuserve.com.*

***PAT BARRETT, PE***
***Barrett & Associates Engineering***
***Portland, Ore.***

*Your analogies seem realistic: People are (generally) all different, and they interact differently (unpredictably) when put in groups. When projects gets so complicated they can't be done by 1 or 2 people, the team problems sure do add a whole new complexity. And recognizing that you can survive despite being right only a fraction of the time—sounds like true enlightenment!! TNX!—RAP*

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

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# PENTON'S

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## Product Mart

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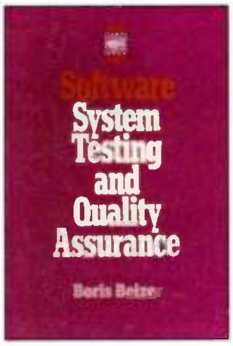
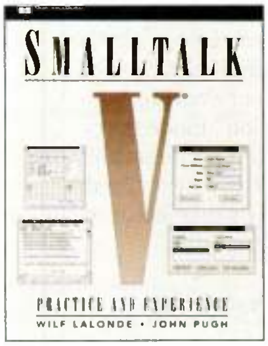
**Software System Testing and Quality Assurance**
*Boris Beizer*




This guide shows readers how to create and maintain reliable, robust, high-quality software. Using non-technical, easy-to-follow language, the author covers the gamut from unit testing to system testing and provides new and effective techniques for security testing, recovery testing, configuration testing, background testing, and performance testing. Integration testing strategies ensure that software components are compatible, while a wide range of techniques find and repair bugs at the unit and system levels.

**358 pages, hardcover book, $55.95, Item B2454PM**

**Smalltalk/V: Practice and Experience**
*W. Lalonde & J. Pugh*

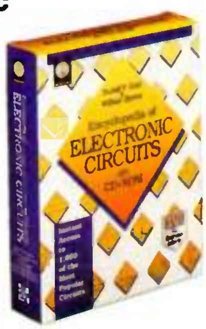



Devoted to applications programming in Smalltalk. Each chapter is based on a column published in JOOP and Smalltalk topics are addressed within the context of practical and useful case studies, such as the design of classes with multiple representations, the importance of generalization, and the use of multi-level facilities and encapsulators. The accompanying disk provides full source code.

**185 pages, softcover book, $39.00, Item DB2566PM**

### CD ROM

**Encyclopedia of Electronic Circuits on CD-ROM**
*R. Graf & W. Sheets*

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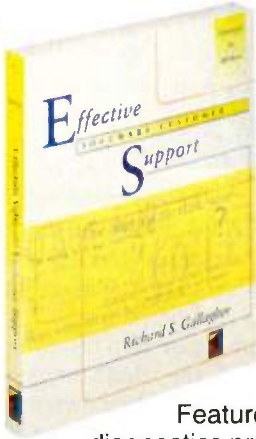
### Books

**Effective Software Customer Support**
*Richard S. Gallagher*




A fundamental resource to providing high-quality, cost effective customer support services in today's mass-market software industry. Examines the relationship between a software support operations and its surrounding organization, the role of support data in the product marketing and development process, and recent issues such as electronic support forums and support automation. Features include software problem diagnostics procedures; coverage of support automation tools that help control costs and provide customer feedback to the rest of the organization; practical suggestions for running day-to-day operations in a support center; and guidelines for dealing with software customers.

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# The Well-Stocked Toolbox

*Some Handy Resources To Keep You Up To Date.*

During the initial planning for this column, in thinking about what would be a good analog related theme, we came up with the idea of those **Tools and Tips** which an analog engineer finds useful. That moniker then became the name of this column. Let's spend some space on what this can mean to the reader.

First, to keep a flavor of diversity, the tools and tips need not always be electronic circuits related, but rather any topic which could, directly or indirectly, be a useful analog engineering tool. And, what the heck, it also can be for just fun now and then, since we're all human.

This thinking first evolved into the Internet-related columns, which not only provide useful information on getting started and communicating effectively, but hopefully also allow you to enjoy the process. But more importantly, these kinds of tools and tips open an avenue for you. The path leads to some of the greatest sources of information, ones which it would seem downright careless to disregard. Sure, it takes some extra work, and perhaps learning a few new computer tricks, but the end result is worthwhile. This topic reiterates a broader point from above—it often takes some real work to survive in today's world.

Other tool examples are books and software, which will be discussed more specifically from time to time, particularly when a new or important development takes place.

Speaking generally, traditional textbooks and other key technical literature are obviously important tools in the analog engineer's bag of tricks. And, this is another area in which you will need to keep updated on an ongoing basis. A staple of key analog design references should be part of your library, headed up at the top by textbooks and handbooks of analog design techniques. You also should be reading and filing magazines with analog design related content, such as *Electronic Design*, as well as its *Special Analog Supplements.*

TIP: You also can supplement this with archival information from the *ED* website.[1] Some companies also publish their own technical journals, containing worthwhile tutorial information in addition to standard product information. Examples here would be such publications as Hewlett-Packard's *Hewlett-Packard Journal*, (*http://www.hp.com/*) and *Analog Dialogue* from Analog Devices.

Whenever you can, try to attend manufacturers' seminars. They offer closer insight into the techniques and technology behind the latest parts. Also, they are unusually good opportunities to meet factory personnel, and to query them firsthand on the latest devices. Having participated in several Analog Devices seminar tours over the last few years, I can say that they are well-timed occasions for bringing designers in the field and application engineers together. They also can establish dialogues useful to both parties.[2]

WALT JUNG

These sources should be supplemented by manufacturers' catalogs, application notes, and seminar books. Since many manufacturers are now deemphasizing the huge printed catalog required for a large product line, you'll also want to supplement your printed catalogs. Three ways to supplement your cache of catalogs are with CD-ROM versions, vendors' fax-back services, or World Wide Web site acquired data sheets. Component manufacturers' and distributors' web sites also can provide great sources of much broader technical information.

TIP: A useful resource which has numerous semiconductor homepage links is Gray Creager's website: *http://www.scruznet.com/~gcreager/index.htm*. The links of Dan Burke's site let you bypass top level stuff and go directly to the relevant data sheet search engine page. See: *http://www.crhc.uiuc.edu/~dburke/databookshelf.html.*

You also can establish one-on-one contact with vendor application engineers for specific technical support on their products. Here "specific" is intended to convey that this type of support is meant to help you in the most effective application of the manufacturer's part. It is not intended to be a general open-ended consultation source (no one would ever try to misuse application resources like that, would they?). Check your vendor's catalog or web site for specifics on contacting them by phone, fax or e-mail. You'll probably find that the array of extra help that's potentially available to customers is definitely not something that will make you wish for the "good old days." For example, availability of the complex modern evaluation and demo boards for IC parts is something relatively unheard of until recently, and these boards can definitely make your design job both faster and easier.

Your electronic distributors can be useful in many ways, beyond the basic availability of parts. They also are a continuous source of catalog information on their various lines, so get to know your distributors.

TIP: A useful website with links to many U.S. distributors (complete with URLs and other contact information) can be found at: *http://www.hitex.com/chipdir/dist/us.htm.*

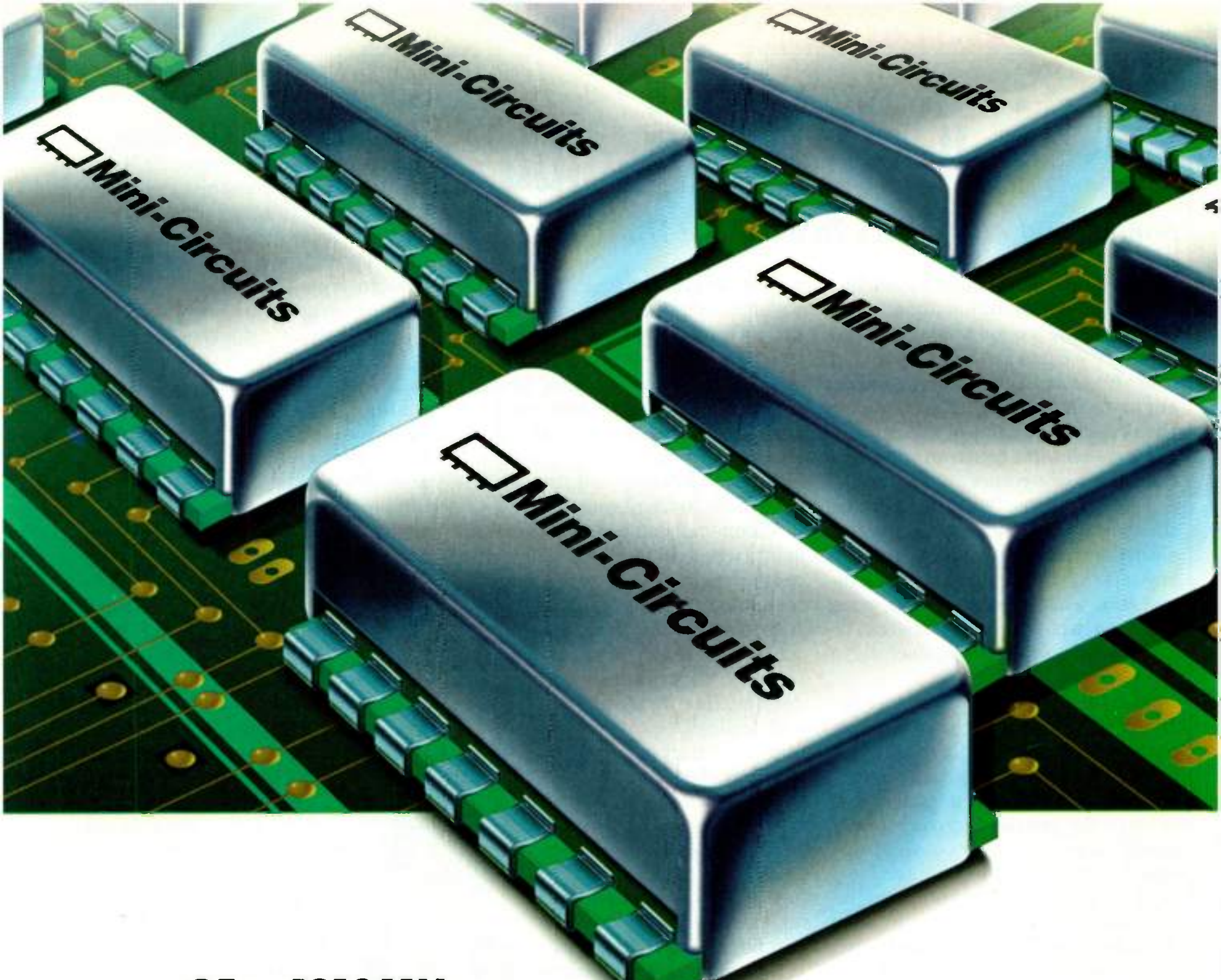
So, those are some of the **tool and tip** necessities related to analog design and its support. This article is but a start, and you may have some additional input or comments for a future column. Feel free to write and share your thoughts on these or other analog issues.


*References:*

1. The Electronic Design site is at *http://www.penton.com/ed/resource/index.html.*
2. The Analog Devices website at *http://www.analog.com* has the contents of recent seminars and *Analog Dialogue* on line.



*Walt Jung is a corporate staff applications engineer for Analog Devices, Norwood, Mass. A longtime contributor to Electronic Design, he can be reached via e-mail at Walter.Jung@Analog.com.*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Circle 520

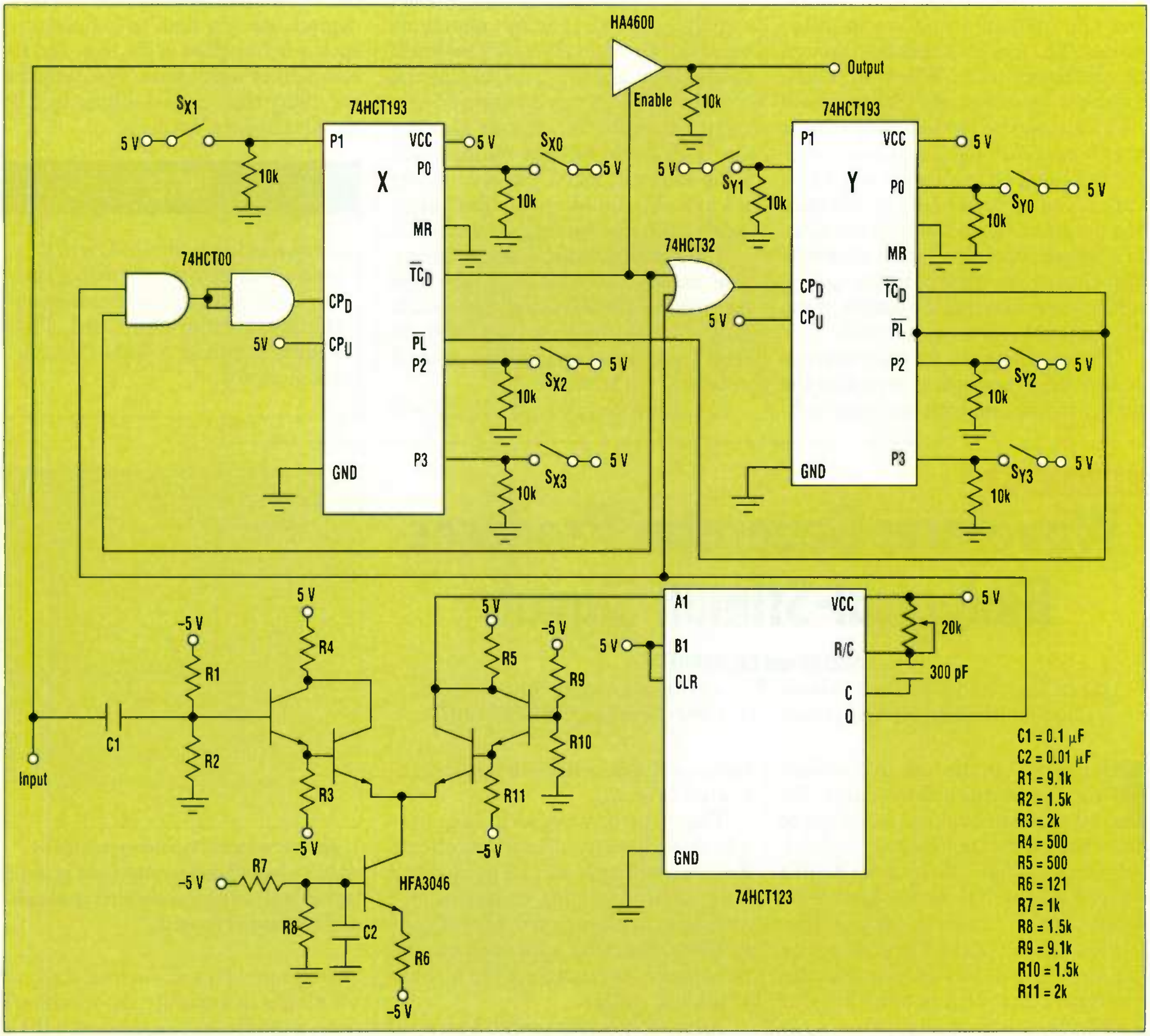
# Digital Control Selects Analog Cycles And Burst Frequency

**ALAN ERZINGER and RON MANCINI**
Harris Corp., Semiconductor Sector, P.O. Box 883, MS58-095;
Melbourne, FL 32902-0883.

Repetitive pulse bursts are required for impulse testing and for burst data-transmission schemes. Impulse testing subjects the device under test to a unit impulse or doublet, and the response waveform is analyzed to determine the circuit's performance.

Burst data-transmission systems send out repetitive pulse bursts. The pulse burst repetition rate is decoded by filtering to select between different transmitting systems, and the number of pulses in a burst form a command. It's easy to design pulse burst systems with digital circuits, but the results are better when analog circuits are used because triangular waveforms and sinewaves fit the theory much better. Also, these waveforms produce much less ringing and overshoot during transmission than digital waveforms.

Figure 1 illustrates the transmitted signal and the continuous sinewave from which it's derived. Because the HA4600 buffer has an enable/disable feature, it will pass or reject the input waveform depending on the state of the enable pin *(Fig. 2)*. The trick is to control the enable input to the HA4600 so that it passes the number of input cycles required to form the burst count, while it rejects the number of input cycles required to form




**2. Incorporating digital control logic, this analog system can generate pulse-burst input waveforms up to 10-MHz with little degradation.**

the correct repetition frequency.

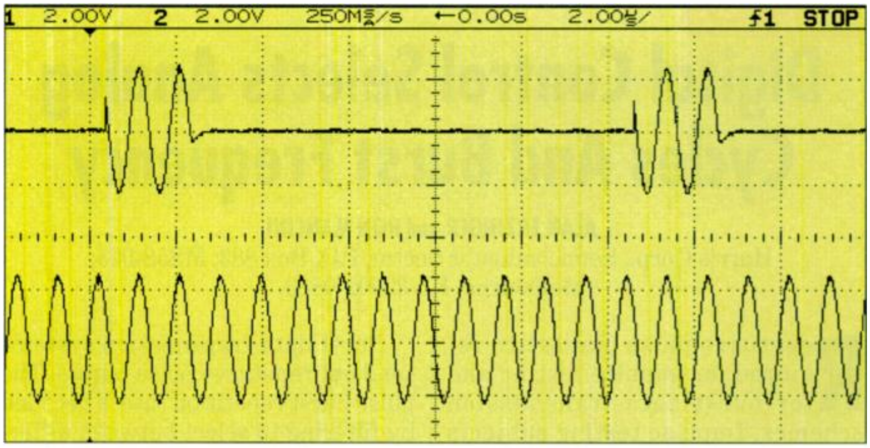
The input signal also is present at the input to the HFA3046 transistor array, which has been configured as a high-speed, high-gain comparator. The comparator squares up the input signal and applies it to the inputs of the two counters, X and Y. The X counter controls the buffer enable, and it determines how many cycles of the input waveform get passed to the output. The four switches, $S_{x0}$ through $S_{x3}$, are binary-coded. Consequently, if two switches ($S_{x0}$ = 1 cycle and $S_{x1}$ = 2 cycles) are closed, three cycles of the input sinewave will be passed to the output.

Furthermore, the input signal is connected to the Y counter, which controls the repetition rate by determining the off period between pulse bursts. The four switches $S_{y0}$ through $S_{y3}$ are binary coded. When all of these switches are closed, the off period will be 16 times the period of the input waveform. With the X and Y counters set as described earlier, the repetition rate is the reciprocal of (16+3) times the period of the incoming waveform. If a longer repetition rate is desired a flip-flop or another counter can be added in series with the output of the Y counter to extend the off time.

The specifications for the comparator are very demanding, including the ability to function with low input voltages, very low storage delays, fast switching speeds, and no reflections back to the input. No off-the-shelf comparator met these requirements, so the HFA3046 was configured as a comparator. R6, R7, and R8 bias the long-tailed transistor at 10mA, which is the optimum point for speed. R5 and R6 are small enough to discharge quickly, thus preventing saturation.

The HA4600 was chosen for the enable amplifier because of its very high bandwidth (480 MHz), and low cost. If gain is required, a HA5020 or HFA1145 enable op amp can be used instead of the HA4600.

Configured as shown, the circuit will handle 10-MHz input signals with little degradation. The limit on frequency response is the speed of the logic and the comparator delay time. The comparator delay time can be eliminated by one-shotting out the delay.




**1. The photo shows an analog burst-transmitted signal and the continuous sinewave from which it's derived. Only a minor amount of crossover distortion can be observed in the burst-output waveform, which will typically have a negligible effect on the system function.**

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Read the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a $300 Best-of-Issue award.

*Circle 521*

# Waveform Generator Produces Biological-Stimuli Signals

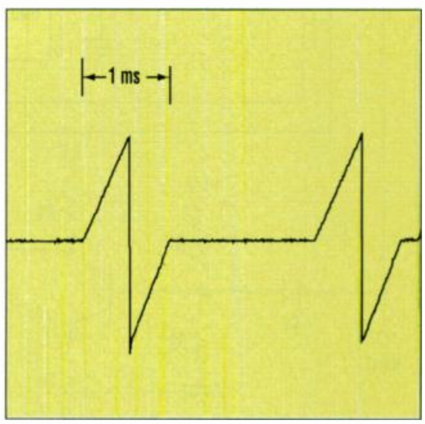
**J. MILLAR and T.G. BARNETT**

Queen Mary and Westfield College, University of London, Mile End Rd., London, England E1 4NS; phone: 0171-982 6366; fax: 0181-983 0467.

Electrical simulators are widely used in biological research for the study of evoked potentials in man and other applications. Indeed, versions are on sale in local health stores or via mail order for treatment of pain. However, for the stimulation to be most effective, the pulse shape needs to be a certain configuration: It has to be bipolar and have only one edge, similar in form to two sawtooth waveforms back-to-back with the second inverted *(Fig. 1)*.

This type of waveform is generally described as a Zeta waveform. Zeta waveforms can be generated very easily by using commercially available arbitrary waveform generators. But this approach can be expensive, particularly for a "one-of-a-kind" project.

Another possible solution would be to use a PROM and digital-to-analog converter. However, the best solution is to generate the waveform from analog components with little time and effort and low cost.




**1. Zeta waveforms, typically produced by arbitrary waveform generators, are essential for maximum efficacy in electrical simulators used in biological research.**

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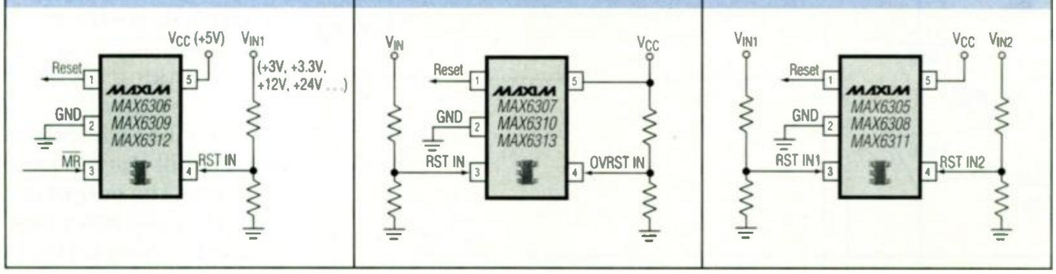


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- Factory-Trimmed $V_{CC}$ Reset Thresholds; 2.5V to 5.0V in 100mV Increments
- Guaranteed Reset Valid to $V_{CC}$ = 1V
- Guaranteed Over Temperature
- Immune to Short $V_{CC}$ Transients
- 5-Pin SOT Package

| PART | FACTORY-TRIMMED $V_{CC}$ RESET | ADJUSTABLE UNDERVOLTAGE RESET | ADJUSTABLE OVERVOLTAGE RESET | MANUAL RESET INPUT | OUTPUT |
|---|---|---|---|---|---|
| MAX6305 | | ✔ | | | |
| MAX6306 | ✔ | ✔ | | ✔ | Open-Drain $\overline{\text{RESET}}$ |
| MAX6307 | ✔ | ✔ | ✔ | | |
| MAX6308 | | ✔ | | | |
| MAX6309 | ✔ | ✔ | | ✔ | CMOS $\overline{\text{RESET}}$ |
| MAX6310 | ✔ | ✔ | ✔ | | |
| MAX6311 | | ✔ | | | |
| MAX6312 | ✔ | ✔ | | ✔ | CMOS RESET |
| MAX6313 | ✔ | ✔ | ✔ | | |


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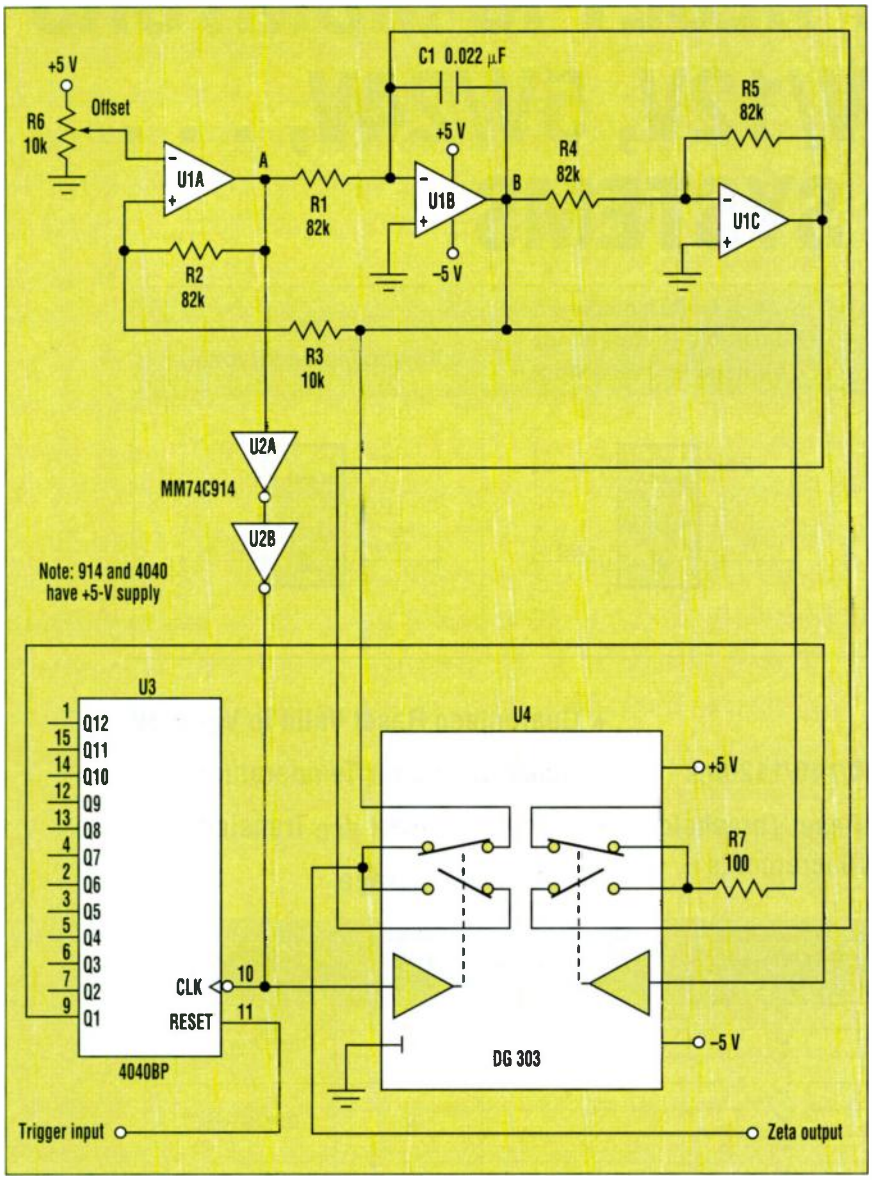
Circle No. 127 - For U.S. Response
Circle No. 128 - For International




**2. This simple and compact circuit offers a low-cost alternative to using arbitrary waveform generators for producing Zeta waveforms.**

The circuit operates as follows *(Fig. 2)*: U1A and U1B form a triangle waveform generator using R6 to offset the output so that it's a positive-going signal. The amplitude is set by R2 and R3, and the ramp's rate of rise is set by R1 and C1. Using the values shown, the output has an amplitude of ±1 V with rise and fall times of 0.5 ms giving a total Zeta duration of 1 ms.

U1C provides an inverted output of U1B. When the reset pin on U3 is triggered, its Q1 output goes low and the short across C1 by one half of the analog switch (U4) is removed. At this time, the output of U1A will be negative and the output of U1B will start to ramp up. During this time, the output of the circuit is taken via the other half of the analog switch from U1B.

When the ramp reaches its positive voltage threshold, the output of U1A goes positive and U1B will start to ramp down. The output of U1A is taken via U2A and U2B (both inverting Schmitt triggers with special input circuitry that protects the input from negative voltages and allows them to level shift) to the clock input of U3. It's also taken to the analog switch, which now takes the output of the circuit from U1C (which has an output ramping up from the negative maximum to 0 V). At 0 V, the output of U1A will go negative, resulting in the Q1 output of U3 going high and again shorting C1. This produces 0-V output until the next trigger input resets U3 and the cycle is repeated.

Circle 522

# Special BIOS Interrupt For Real-Time Data Acquisition And Control

J. JAYAPANDIAN
IGCAR, Materials Science Div., Kalpakkam, PIN 603102, Tamil Nadu, India;
fax 0091-04114-40360; e-mail: msd@igcar.ernet.in.

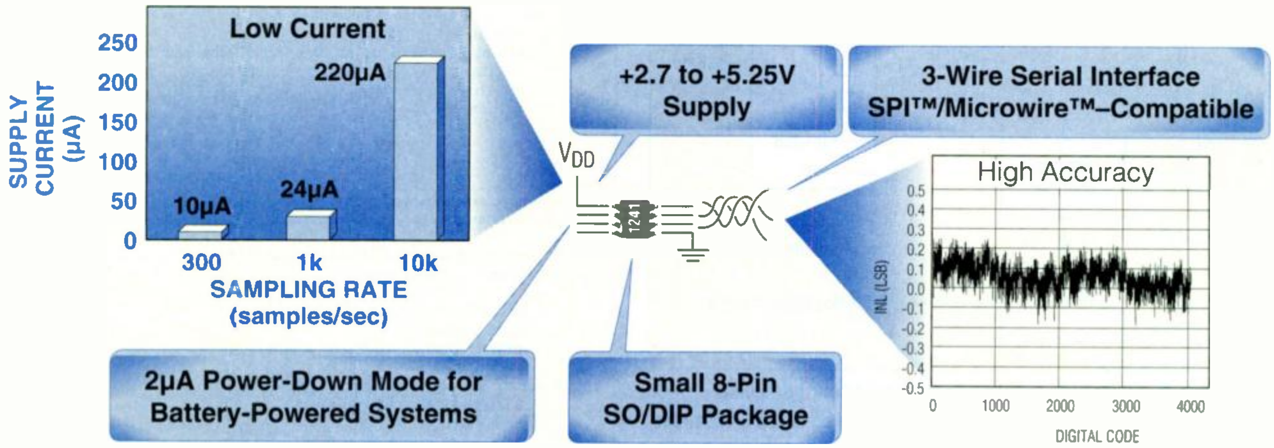
A PC's BIOS contains a special "dummy" interrupt (INT 1CH) that does nothing unless a routine is provided for it. At startup, the vector for the interrupt points to an IRET (interrupt return) instruction. When the interrupt is called, it simply returns *(see the figure)*.

The INT 1C interrupt is a hardware interrupt that automatically occurs 18.2 times per second, and the "dummy" interrupt is invoked by the BIOS timer interrupt after it updates the time-of-day count. This "dummy" interrupt is available in all PCs and can be used for data acquisition and control in process control instrumentation. Some examples are sensing

# NEW 2.7V 12-BIT ADC IN SO-8 DRAWS ONLY 10µA

10-BIT VERSIONS ALSO AVAILABLE

## 1- to 8-Channel Serial ADCs Combine Low Power, Small Packages and Performance




The new MAX1241 ADC is designed for 3V, 3.3V, and 5V applications. It requires only 0.9mA at 73ksps, and only 10µA at 300 samples/sec, which helps keep you well within your power budget in portable and battery-powered applications. The MAX1241 complements existing 4-channel (MAX1247) and 8-channel (MAX147) devices (see table). For 10-bit applications, use the pin- and software-compatible MAX1243/MAX1249 and MAX148, which have 1, 4, and 8 channels, respectively.

### Choose Maxim's Low-Power & Small-Footprint ADCs

| PART | RESOLUTION (BITS) | NUMBER OF CHANNELS | PACKAGES | MAXIMUM SPEED (ksps) | 2.7V to 5.25V OPERATION | AUTO-POWERDOWN |
|---|---|---|---|---|---|---|
| MAX1241 | 12 | 1 | 8-Pin SO/DIP | 73 | Yes | Yes |
| MAX1247 | 12 | 4 | 16-Pin QSOP/DIP | 133 | Yes | Yes |
| MAX147 | 12 | 8 | 20-Pin SSOP/DIP | 133 | Yes | Yes |
| MAX1243 | 10 | 1 | 8-Pin SO/DIP | 73 | Yes | Yes |
| MAX1249 | 10 | 4 | 16-Pin QSOP/DIP | 133 | Yes | Yes |
| MAX148 | 10 | 8 | 20-Pin SSOP/DIP | 133 | Yes | Yes |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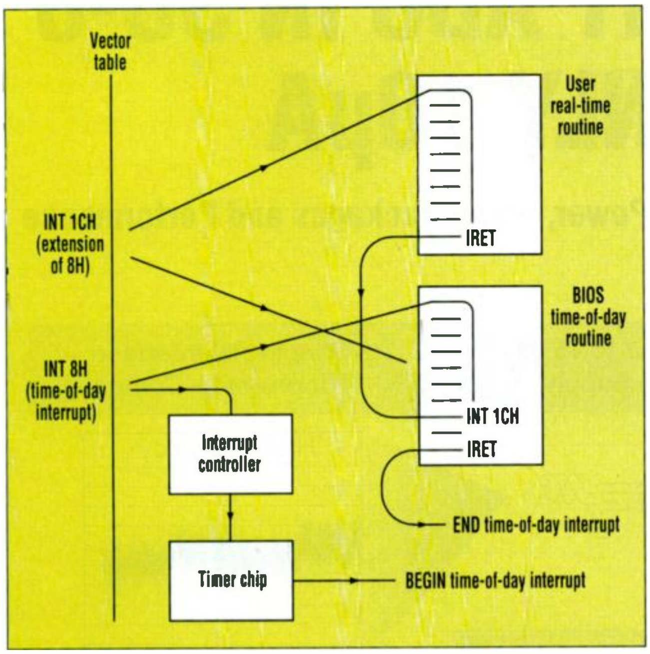


**By changing the vector to point to a procedure in your particular program, a PC's "dummy" interrupt (INT 1CH) can be called 18.2 times per second for use as a real-time timing reference.**

```
/* Sample Program written in Turbo "C" uses "1C" Interrupt: */

#include <stdio.h>
#include <dos.h>
#include <conio.h>

#define INR      0X1C      /* 0X1C - The clock tick interrupt */

void interrupt ( *oldhandler) (void);
        int count=0;
void interrupt handler(void)
   {
      /* disable interrupts during the handling of the interrupt */
          disable();
      /* increase the global counter */
          count++;
      /* reenable interrupts at the end of the handler */
          enable();
      /* call the old routine */
          oldhandler();
   }

int main(void)
   {
      /* save the old interrupt vector */
          oldhandler = getvect(INTR);

      /* install the new interrupt handler */
          setvect(INTR, handler);

      /* loop until the counter exceeds 100 */
          while (count < 100)
          printf("count is %d\n",count);

      /* reset the old interrupt handler */
          setvect(INTR, oldhandler);
          return 0;
   }
```

and controlling of pressure, flow, furnace temperature, a motor's RPM, etc.

To take advantage of this feature, simply change the vector for this interrupt to point to a procedure in your program. Then that procedure will be called 18.2 times per second. Care should be taken to minimize execution time when writing this interrupt handler. Typically, 18 times per second is a sufficient amount of time for the interrupt handler to achieve its tasks.

Variables in process control instrumentation are very slow compared to this INT 1CH time of occurrence. Looking at the figure, the variable COUNT is incremented by one every INT 1CH until the count reaches 100.

A similar procedure can be written in the place of COUNT, for both sensing a port in the add-on card and writing an appropriate control function value to the control port. The data written to the control port may be for proportional, integral, differential, or on/off control functions.

In the figure, the vector for interrupt 1CH is changed to point to a procedure called COUNT. Remember that once the vector is changed, COUNT will immediately be invoked every 18th of a second. Be very careful about saving changed registers.

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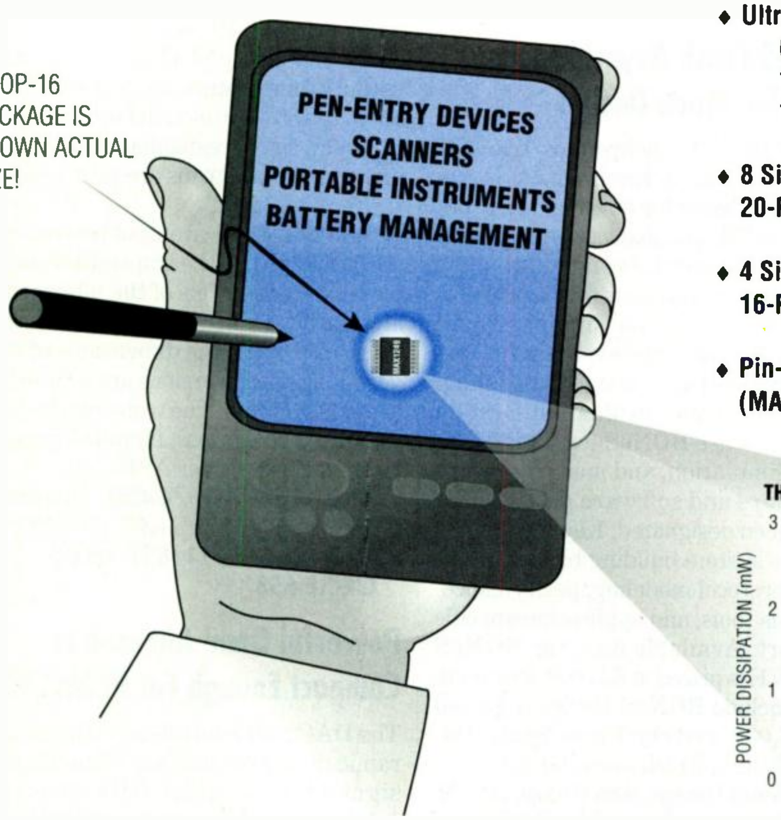
# FIRST 2.7V 10-BIT ADCs USE LOWEST POWER

## 100µA @ 10ksps, 1µA Power-Down—Ideal for Portable Devices

The MAX148/MAX1249 reduce power requirements in 3V 10-bit applications. They are the lowest power 3V ADCs available and the only ones with a power-down mode. In addition, these 10-bit ADCs are the first to operate down to +2.7V. Other features include a 3-wire serial interface and space-saving packages. The 8-channel MAX148 comes in a 20-pin SSOP, while the 4-channel MAX1249 comes in an even smaller 16-pin QSOP (about the same area as an 8-pin SOIC)! For portable applications, look to the MAX148/MAX1249 for your lowest power, lowest voltage, and smallest size solutions.

QSOP-16 PACKAGE IS SHOWN ACTUAL SIZE!

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- Ultra-Low Supply Current:
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  - 100µA @ 10ksps
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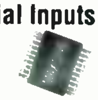
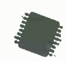
- 8 Single-Ended/4 Differential Inputs, 20-Pin SSOP Package } MAX148



- 4 Single-Ended/2 Differential Inputs, 16-Pin QSOP Package } MAX1249



- Pin-Compatible 12-Bit Upgrades (MAX147, MAX1247)

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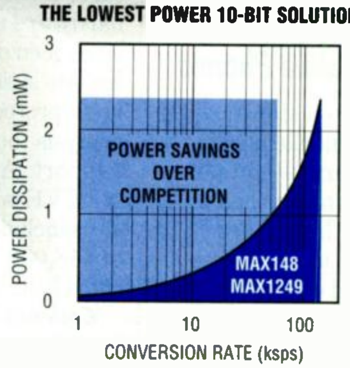



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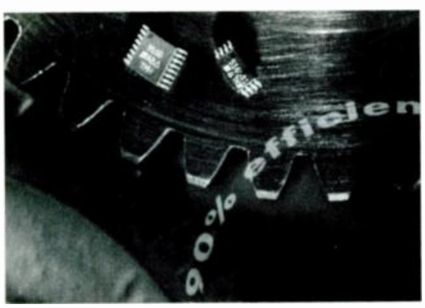
## T1 Signals Mapped To SONET/SDH Formats

The QT1M chip maps four T1 1.544-Mbit/s signals to and from North American-based SONET or ITU-based SDH formats. For SONET applications, the T1 signal is mapped asynchronously to and from a Virtual Tributary 1.5 within an STS-based signal. For the ITU's SDH applications, the T1 signal is assigned into a Tributary-Unit 11 using either the VC-3 or VC-4 mapping hierarchy. The QT1M meets both ANSI T1.105-1995 and Bellcore GR-253-CORE Issue 2 standards. The chip supports new standards capabilities, including 3 bit RDI, unequipped code detection/alarms, and path label mismatch detection/alarms. Potential applications include add/drop multiplexers, terminal multiplexers, digital loop carrier systems, digital crossconnect systems, and single and dual unidirectional rings. The QT1M is provided in a 160-pin plastic quad flat package and requires a single 5-V supply. LG

*TranSwitch Corp., 8 Progress Dr., Shelton, CT 06484. (203) 929-8810; fax (203) 926-9453.* **CIRCLE 655**

## Chip Set Lengthens Li-Ion Battery Life In Mobile Phones

A new chip set offers a significantly longer battery life in mobile phones using lithium-ion batteries—total converter effectivity is more than 90%. The set consists of the high-speed PBM IC Si9160BQ and the application-specific N- and P-channel complementary



MOSFET Si6801DQ. According to the manufacturer, the Si9160BQ is the first fully integrated controller that works with a frequency beyond 1 MHz. It allows synchronization in the system clock above the signal and signal-processing frequencies. On the other hand, its frequency is well beyond the carrier frequencies, eliminating potential disturbances. The chip set's core element is the Si9160BQ controller. This chip has its own voltage reference of 1% band separation, a clock of 600 kHz to 2 MHz, a 25-MHz, low-voltage, error-correction amplifier, a fast differential amplifier, and delay circuitry in the nanosecond range. At 3.5 V, the power MOSFET Si6801DQ has an on-resistance of 180 mΩ. Its effective input capacity is 0.79 nF. AV

*Temic, P. O. Box 35 35, 74025 Heilbronn, Germany; fax +49-7131/99 33 42.* **CIRCLE 656**

## BONeS Crack Asynchronous-Transfer-Mode Design

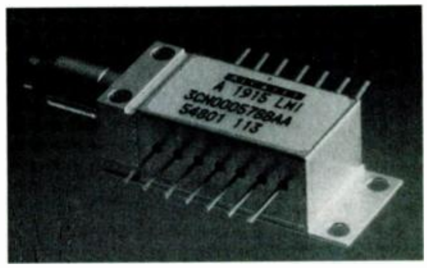
The BONeS Asynchronous Transfer Mode Verification Environment is created specifically for quick and easy design of ATM-compliant products, especially in the wireless and multimedia design domains. It's the first tool to provide comprehensive support for all three areas of high-level design: system architecture, protocol modeling, and performance evaluation. System architects use BONeS for design capture, simulation, and analysis before hardware and software partitioning have been designated. Key capabilities include system building blocks, multilayer protocol modeling, performance-analysis tools, and application-specific support. Available now, the BONeS ATM VE is priced at $25,000. Prerequisites include BONeS Designer, priced at $18,000, and the Finite State Machine Editor, which costs $6000. LG

*Cadence Design, Alta Group, 555 N. Mathilda Ave., Sunnyvale, CA 94086. (408) 733-1595; (408) 523-4601.* **CIRCLE 657**

## Integrated Module Family Adds Long-Reach Capability

A recent addition to the family of STM-4/OC-12 integrated modules offers "long reach." The device features a dispersion capability of up to 3200 ps/nm and an optical span of up to 160 km, according to the G652 optical-fiber standard. Sensitivity is -35 dBm, and overload capability is better than -8 dBm.

The 1914 SDH family consists of transmitter and receiver modules that provide interfaces for SDH or SONET systems operating at 622 Mbits/s.



They're compatible with applicable ITU-T, Bellcore, and ANSI standards. These modules are used in transmission systems like digital cross-connects or add-drop multiplexers, as well as ATM switches. Requiring a single 5-V power supply, the SDH family operates within a temperature range of 0 to 70°C or -40 to +85°C. Functions such as clock recovery, signal reshaping, data retiming, and digital alarms are provided by the receiver modules.

Automatic optical output power control is assured by the transmitter modules. The dimensions of the intermediate-reach versions are 23 mm by 35 mm by 11 mm, while the dimensions of the very-long-reach versions are 57 mm by 51 mm by 11 mm. The transmit module contains a cooler-less, pigtailed coaxial laser and laser driver ASIC. AV

*Alcatel SEL AG, 70430, Stuttgart, Germany; phone +49-711/821-43843; fax +49-711/821-46055.* **CIRCLE 658**

## Powerful Omni Antenna Is Compact Enough For PCMCIA

The DAC2450 is an ultra-miniature ceramic dielectric antenna element, designed for use in 2.4-GHz wireless LAN cards. This round, vertically polarized patch antenna features a low profile of 6.5 mm, suiting it for mounting within expanded PCMCIA Type 2 cards. Its unique design provides omnidirectional capability and is resistant to the types of interference that are caused by operation near large metallic objects, such as automobiles and computer equipment. With a center frequency of 2450 MHz, it exhibits a 3-dB receiving bandwidth of 100 MHz, a 50-Ω impedance, and a peak gain of 0 dBi.

Available now, the DAC2450 costs $5 each in 1000-piece quantities. LG

*Toko America Inc. 1250 Feehanville Dr. Mount Prospect, IL 60056; (847) 297-0070; fax (847) 699-7864; Web: http://www.tokoam.com.* **CIRCLE 659**

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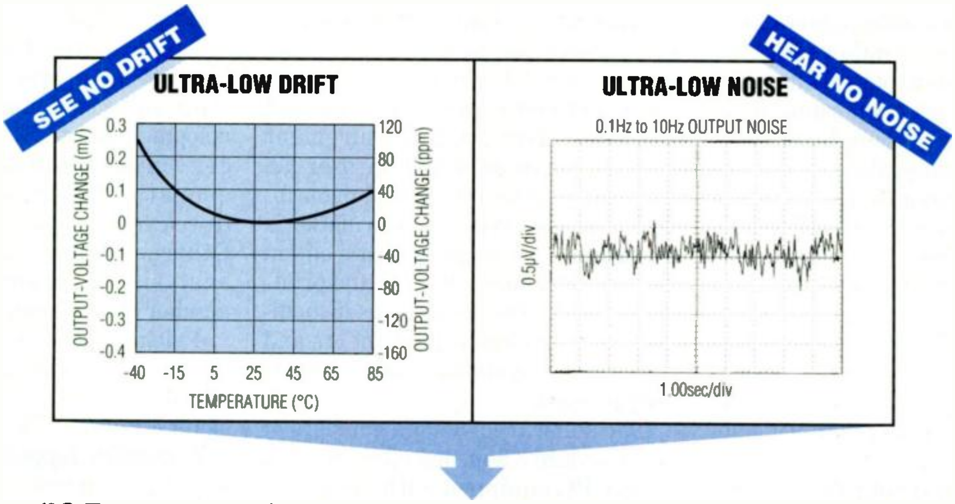


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- 1.5μV$_{p-p}$ Noise (0.1Hz to 10Hz)
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| PART | TYPICAL OUTPUT VOLTAGE (V) | TYP/MAX TEMPCO (ppm/°C) | INITIAL ACCURACY (%) | MAX NOISE* (μV$_{RMS}$) | OPTIONAL NOISE REDUCTION & VOLTAGE TRIM | PRICE** ($) |
|---|---|---|---|---|---|---|
| MAX6225A | 2.5 | 1.0/2.0 | ±0.04 | 2.8 | Yes | 4.65 |
| MAX6241A | 4.096 | 1.0/2.0 | ±0.025 | 4.0 | Yes | 4.65 |
| MAX6250A | 5.0 | 1.0/2.0 | ±0.02 | 5.0 | Yes | 4.65 |
| MAX6225B | 2.5 | 2.5/5.0 | ±0.1 | 2.8 | Yes | 2.25 |
| MAX6241B | 4.096 | 2.5/5.0 | ±0.1 | 4.0 | Yes | 2.25 |
| MAX6250B | 5.0 | 2.5/5.0 | ±0.1 | 5.0 | Yes | 2.25 |

* 10Hz ≤ $f$ ≤ 1kHz **1000-piece price, FOB USA.


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## Debugging Tools Support Windows Developers

SoftICE Windows debuggers for Windows NT and Windows 95 are kernel-mode components that can be installed as a boot driver, system driver or automatic driver for on-demand debugging. SoftICE for Windows NT also can be installed as a manual driver for debugging any program running on Windows NT or system-level code. Moreover, it debugs all system modules, including boot drivers, system drivers, system services, all Win32 and Win16 applications, DLLs, and all DOS programs, including DOS extender applications.

Additional features include software and hardware breakpoints, conditional C breakpoint expressions, and debugger-macro and system-wide object search facilities. Other capabilities are hierarchical object directory display, Win32 fault trapping and exception handling, symbolic display of OS internals, and system-wide event monitoring.

The product works with both retail and checked versions of Windows NT. System requirements include an Intel 386/486/Pentium single-processor platform, Windows NT 3.51 or NT 4.0 Beta, 16 Mbytes of RAM minimum, and 2.5-Mbyte disk space. SoftICE for Windows 95 offers many of the features of the NT version for debugging 16- and 32-bit Windows applications, including support for dynamically loadable virtual device drivers. System requirements are IBM-compatible 386, 486, or Pentium PC running Windows 95, 2 Mbytes of hard disk space, and compatibility with Microsoft, Borland, Symantex, and Watcom C compilers. ML

***NuMega Technologies,** 9 Townsend West, Nashua, NH 03063; (603) 889-2386 or 800-4-NUMEGA; e-mail: info@numega.com*
***CIRCLE 660***

## Software Simplifies Analysis Of Inertia Generators

A new Windows-based software program can help designers of mechanical drive systems quickly calculate the inertia generated by individual rotating drive components. The program uses physical dimensions supplied by the user to calculate inertia. Because the physical data may not always be available in a single format, the program accepts a variety of physical data for each parameter.

The designer lays out the system by dragging and dropping icons representing up to eight system components in series, such as a single lead screw, a parallel cylinder or rod, a pulley, a nip roller, conveyor pulleys, and a gearbox. Different measurement systems can be used, and the user can make notes within the program for future reference. When the calculation is completed, the program prints out an application data sheet. Both the printout and exit screen can be user-modified for individual requirements and preferences. Extensive help screens are provided.

The software package consists of two standard 3.5-in. diskettes that run on any PC equipped with Microsoft Windows. Sizing and Selecting Software for Inertia Generators can be downloaded from WeCell BBS. ML

***Warner Electric Advertising Dept.,** 449 Gardner St., South Beloit, IL 61080; (815) 389-3771; WeCell BBS: (815) 389-6440.*
***CIRCLE 661***

## Integrated Environment Motorola Processor Systems

Embedded Support Tools Corp. (EST Corp.) has integrated its visionICE scalable emulation system with Software Development Systems' SingleStep source-level debugger and the Wind River Systems Tornado development environment for supporting the Motorola 68300, PowerPC, and ColdFire-based microprocessor families. With plug-and-play compatibility thanks to SDS's SingleStep source-level debugger, visionICE provides one integrated environment under a single interface. It can handle every phase of the embedded life cycle, from hardware debugging to driver development to C source debugging.

Features of the visionICE/SingleStep integration include support for IEEE695 compilers such as CrossCode, as well as the Elf/Dwarf and PowerPC EABI embedded standards; Flash programming capabilities; crash diagnostics; real-time operating system support; and high-end emulation. Integration with Tornado provides a background debug mode support for the Tornado development environment.

Developers of deeply embedded applications with minimal target resources can use a BDM connection to port the VxWorks real-time operating system to custom hardware, and then debug their applications. EST's visionICE can be customized to fit any development strategy, from low-cost target control through full-scale trace emulation. Modules for multiple trace/event systems, overlay memory, Ethernet communications, and logic analysis can be shared across any number of development seats.

Pricing for the visionICE components is $4250 for the base visionCONTROL system and $6800 for the visionNET system. ML

***Embedded Support Tools Corp.,** 120 Royall St., Canton, MA 02021-9725; (617) 828-5588; fax: (617) 821-2268.*
***CIRCLE 662***

## Accurate Sparc Model Suits Embedded Designs

CAE Plus Inc. has come up with a clock-edge accurate C Sparc model for the embedded-system IC market. Included in the model are the SPARC and coprocessor plus I/Os. The model has a five-stage pipeline with register forwarding, delay instruction with annul option, plus eight register window and three read/write ports for register files. It accurately models stalls resulting from load dependencies and executes the instructions from instruction memory identical to real hardware. C models developed by the company provide RTL accuracy with execution speed 1000 times faster than HDL simulation speed. They require no simulator and can be executed simultaneously on multiple PCs. System IC specifications must be validated prior to RTL coding. The company's modeling specialists and processor architecture experts can modify the SPARC model based on custom implementation architecture and instruction set, and deliver a customized clock-edge accurate C model in a few weeks.

***CAE Plus Inc.,** 9130 Jollyville Rd. #340, Austin, TX 78759; (512) 338-0165; fax (512) 338-0192.*
**CIRCLE 663**

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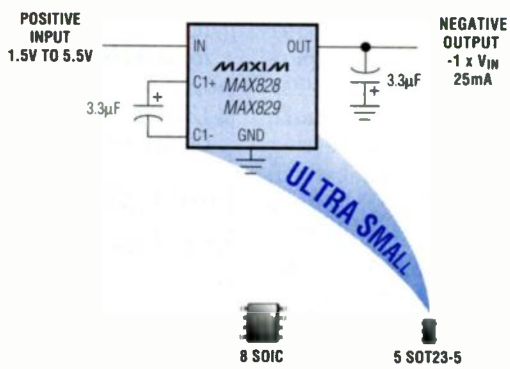


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| | mm² | 31.0 | 8.3 | 8.3 |
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| fosc (kHz) | | 10 | 12 | 35 |
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Circle No. 135 - For U.S. Response
Circle No. 136 - For International

## RTOS Adds Features For Safety-Critical Designs

The OSE Delta real-time operating system includes features designed specifically for building safety-critical applications. The RTOS detects errors in programming or those due to hardware failure and automatically invokes action to handle the error and ensure the system remains in a safe state. Blocks of processes, redirection tables, user numbers, and powerful memory configurations allow developers to build an application providing maximum safety and high performance. Supervisory features enable processes to request supervision of other processes and resources. If processes or resources being supervised become inaccessible (process killed, network failure, or remote board failure), the process requesting supervision is notified so that it can take appropriate action. OSE Delta is the fourth implementation level of the OSE message-based RTOS family, which brings special capabilities for fault tolerance, safety-critical applications, run-time configuration, and distribution. ML

***Enea OSE Systems AB**, P.O. Box 232, Nytorpsvagen 5B, S-183 23 Taby, Sweden; +46(0)8 638 50 00; fax: +46(0)8 638 50 50.* **CIRCLE 664**

## New Feature Set Enhance Object Request Broker

The Orbix 2.1 object request broker from Iona Technologies is a performance-critical ORB with real-time solutions providers ISI, VXWorks, and QNX. Several new features provide a 25% performance improvement over previous versions, including full Cobra 2.0 features and full Internet Inter-ORB Protocol (IIOP) standardization for point-to-point transport at the wire level.

Orbix 2.1 now supports the Dynamic Skeleton Interface, which allows a server to receive an operation call, even for an object of which no knowledge is known prior to compile time. New extended filter support allows Orbix 2.1 to deliver symmetric response mechanisms for transactions. This detection service supports both client and server failures and initiates appropriate actions.

Distributed free with Orbix 2.1 is OrbixNames, which allows objects to be named independent of any properties of the object, such as its server or host name. Also, GUI features for Windows developers provide access to tools such as Visual Basic, PowerBuilder, and Delphi for linking local and remote OLE and ActiveX objects into developer applications. An optimized portability allows Orbix 2.1 to bring together specific features (such as multithreading and support of Asynchronous Winsock on Windows NT) of numerous operating systems into a coherent development environment. Orbix 2.1 costs between $2500 and $5000 per developer license, depending on operating system. ML

***Iona Technologies Inc.**, 201 Broadway, Floor 3, Cambridge, MA 02139; (617) 679-0900; fax (617) 679-0910.* **CIRCLE 665**

## Prototyping System Tests Real-Time Embedded Designs

Embedded-system developers can now use the tailorable code-generation techniques of Statemate Magnum from i-Logix Inc. to generate a virtual prototype that runs on the host platform. It also can create an embedded prototype that runs on the target processor under the VxWorks RTOS of the Tornado development environment of Wind River Systems Inc. Systems then are able to be tested in a realistic environment, minimizing the time and expense of building multiple physical prototypes.

Providing an interactive cross-development environment, the Tornado tool suite incurs little or no overhead in target resources. Included are the VxWorks scalable real-time operating system, which executes on the embedded target processor, and communications options such as Ethernet, serial line, BDM, ICE, or ROM emulator for target connection to the host. Tornado also supports the use of third-party and custom tools.

In a typical example, automotive power-train engineers can model the functionality and behavior of the power train in Statemate Magnum's graphical language, verify system behavior through graphical simulation, then automatically generate code that runs under VxWorks on a target processor in the car. Through i-Logix's Graphical Back Animation technology, the software running in the car can be observed at the graphical level in Statemate Magnum. ML

***i-Logix Inc.**, Three Riverside Dr., Andover, MA 01810; (508) 682-2100.* **CIRCLE 666**

## Reference Drivers Tie PCI Cards To Windows NT

Windows NT Reference Drivers developed by Blue Water Systems Inc. are available for PCI card designs using the S5933 PCI interface chip from Applied Micro Circuits Corp. (AMCC). The drivers support the AMCC Matchmaker Development Kit for the S5933 chip sets. Source code is available on request from Blue Water Systems, or on the company's Web site at *http://www.bluewatersystems.com.* Samples for controlling the interface chip include pass-through mode accesses, bus mastering, and mailbox usage.'

The PCI Reference Drivers are based on Blue Water Systems' WinDK Class library and the WinDK Device Driver Development Kit for developing high-speed device drivers for Windows NT 3.51 and 4.0. They're intended for use as a template for commercial NT drivers. Also, they can be expanded upon using WinDK for attaching new hardware to Windows NT platforms. The WinDK Kit supports Microsoft's Windows NT DDK kernel mode driver development, including registry, resource/port assignment, event logging/debugging/trace functions, multiple queues, address mapping, filtering, and so on. PCI Reference Drivers are available at no charge.

The WinDK Device Driver Development Kit for Windows NT 4.0 or 3.51, including six months free support and 90 days free upgrades, is $795. An introductory price of $595 is available for the WinDK Intel version. System requirements are NT 4.0 or 3.51, Intel, Alpha, PowerPC, and Microsoft Visual C++ version 4.x. ML

***Blue Water Systems Inc.**, 190 West Dayton, P.O. Box 776, Edmonds, WA 980-0776; (206) 771-3610.*

***Applied Micro Circuits Corp.**, 6195 Lusk Blvd., San Diego, CA 92121; (800) 755-2622.* **CIRCLE 667**

## Infrared Transceiver Modules Meet IrDA Standards

Three new infrared data-link modules, the IRM 3001, IRM 3105, and IRM 6000, provide point-to-point connectivity in half duplex mode. When combined with the appropriate software, the modules meet the standards of the Infrared Data Association (IrDA). The modules are specifically designed for transmission over short distances up to one meter, eliminating the need for cables and associated interconnect mechanical issues. Even with very close positioning, there is, according to the manufacturer, no signal overload.

The transceiver module supports data rates of 9.6 kbits/s to 115.2 kbits/s with a supply voltage between 3.2 V and 5.5 V and a transmission angle of ±30°. Power consumption in standby mode is below 1 mA. The IRM 3001 and IRM 3105 modules measure 13 mm by 6 mm by 6 mm, while the slim-line version IRM 6000 has dimensions of 9.1 mm by 4.1 mm by 4.3 mm.

The IRM 3105 and IRM 6000 incorporate DIL connections, and the IRM 3001 has single-in-line connections. Other designs with supply voltages down to 2.7 V and data rates up to 4 Mbits/s are currently beign developed. AV

*Siemens Semiconductors, Infoservice RK F/B3, 90713 Fuerth, Germany; fax: +49-911/978 33 21.*

CIRCLE 490

## IC Enables DC Supplies To Be Housed In Slim-Line Power Plugs

A high-voltage BCD Powerlogic IC allows constant-voltage/constant-current dc supplies to be housed in universal slim-line power plugs that plug directly into 90- to 280-V ac-line supplies. Target applications for the IC include fast chargers for cellular and cordless telephones.

The TEA 1401, otherwise known as the Self-Oscillating Flyback Power Supply Controller, derives feedback on output voltage and current from an auxiliary winding on the isolation transformer, eliminating the need for any current- or voltage-sensing circuitry on the secondary side of the transformer.

Furthermore, it includes an on-chip 650-V/0.5-A DMOS switching FET. Therefore, the only other components required in an electronic power plug capable of charging 10- to 20-W loads are an ac-line supply filter and rectifier, a miniature transformer, and a few passive components and diodes. The component runs at frequencies up to 145 kHz. AV

*Philips Semiconductors, Marketing&Sales "TEA1401t Power Plug IC," P.O. Box 218, 5600 MD, Eindhoven, The Netherlands; telephone: +31 40 27 22 091; fax:+31 40 27 24 825.*

CIRCLE 491

## Time-Gated Power Meter Targets Digital Radio Testing

The latest RF & microwave power meter designed by Sematron UK adds a time-gated measurement option and power sensors specifically aimed at the new generation of digital radio communications systems. Time gating makes it possible to accurately measure average power within a user-specified time slot, or within a user-defined portion of any time slot.

The new power meter, called the Giga-tronics 8540C, can perform this measurement more accurately and at a lower cost than, say, spectrum analyzers or digital radio test sets. Thus, the meter allows for wider test limits and guarantees specifications, increasing throughput and production yield and reducing rework costs.

Complementing the novel power meter is a new range of sensors that give measurement capability to 40 GHz. One such sensor is the 80601A, which can provide up to 30 fully settled power measurements per second. It also handles the wide bandwidth required for testing CDMA and similar modulation schemes used in wireless local loop equipment.

The 8540C comes in a compact (215 mm by 89 mm by 368 mm) bench mount case. A wide range of options are available, such as rack-mount kits, rear-panel connectors, and additional internal memory for storing up to 128,000 "burst-mode" readings for subsequent download. RE

*Sematron UK Ltd., Sandpiper House, Aviary Court, Wade Rd., Basingstoke, Hant RG24 8GX, phone: 01256 812222; fax: 01256 812666.* CIRCLE 492

## DC-DC Converter Outputs Range From 24 to 110 V

Generally speaking, dc-dc converters offer a reliable and cost-saving alternative to secondary batteries. For instance, they have lower operating and maintenance costs. They also have reduced capital replacement costs and a longer system lifetime. One such example is the PU 1000, the latest dc-dc converter offered by Polyamp AB. It's able to provide output voltages from 24, 48, 60, to 110 V dc using input voltages varying from 24 to 440 V dc. The device is certified to a number of key industry standards, such as the CE mark.

According to the company, the PU 1000 can test all of its equipment to higher levels than that required by international directives. It's conventional cooling system features an efficiency of more than 90%. Moreover, up to ten units can be connected in parallel. RE

*Polyamp AB, P.O. Box 925, S-191 29, Sollentuna, Sweden; phone: +46 8 359 350; fax: +46 8 96187; e-mail: info@polyamp.se; Web: http://www.polyamp.se.*

CIRCLE 493

*Edited by Roger Engelke*

**Gender Equity For EE's**

I am responding to your Feb 3. "EE Currents & Careers" article *("Give Your Daughters Legos And Erector Sets..." p. 179)*. Although not an Electronic Engineer, I have held various technical positions in electro-mechanical manufacturing and data communications cabling distribution design since 1981. My childhood consisted of playing with toy blocks, Lincoln logs, Legos, horses, and cars. I was considered a "tomboy." I have two brothers and both are engineers.

I firmly believe that in today's job market, it is a much more difficult process to prove credibility and level of expertise and experience as a woman in the field of engineering. My memories of various past job interviews recalled some unusual discussions which a potential employee may wish to anticipate and create witty and/or serious responses for the interviewer. One time, an older gentleman who was interviewing me spread out a schematic larger than his desk in front of me and asked what I would do if the device did not work. I said, "First, I would see if it was plugged in." Another time, a rather portly gentleman asked if I would be able to lift their standard piece of equipment (weighing 75 lbs.). My response was, "I can pick it up and play catch with you, if you like." Often, the interviewer will ask if I am "put off" by foul language in the workplace. You may guess my response on that one.

One time, the president (a Mechanical Engineer) of a company presented me with a fabrication and design issue for my "test." I made my suggestions on the spot. I was hired for that job, and when I arrived for my first day of work, he had already implemented my suggestion. A headhunter recently said to me, "I have spoken to 50 people with your industry certification and not one was a woman." My response to that was, "Oh yes, 10% of us are women." Of course, that figure was off the top of my head, I think it is closer to 6%.

Beth R. Levin, RCDD
Seaside Park, N.J.

*The road to being accepted for innate talent and ability to excel in a position is often littered with landmines. From sensitivity to language to learning the difference between assertive and aggressive, my journey in traditionally male-dominated fields has been filled with challenges. Then, thankfully, there are those gentlemen who have taken a mentoring posture in our professional relationships. And, I agree that one of the most important assets in any situation is a sense of humor.—Debra Schiff*

**A Spacey Proposal**

I concur with your Feb. 17 editorial *("Where Do Our Priorities Lie?" p. 18)*. As a project that would be a practical national science (and engineering) project, I propose the development of the Lunar Power System. This type of system has the potential of solving global energy and environmental problems while stimulating meaningful growth in science and engineering. It entails colonizing the moon and is the most reasonable next step for space development. Recent cost-benefit analyses indicate that it is the least expensive way to meet the world's energy requirements by the year 2010 (approximately 18 terawatts). If the $100 billion that may be spent on the space station were spent on the LPS over a ten-year period, it could result in approximately 10 gigawatts of clean energy for the Earth. The economy of scale associated with the LPS rapidly reduces the cost per gigawatt so that less than one cent per kilowatt-hour is realistic for global scale energy levels (18 terawatts).

Dan Greenwood
President
NETROLOGIC Inc.

**HP And Lee de**

Regarding Andrew Aiken's Feb. 3 letter concerning Lee de Forest's presence at the Hewlett-Packard Company in 1957:

Speaking as someone who was present at the time, I'd like to offer a clarification. Mr. de Forest was not working at Hewlett-Packard; he was visiting, as consequence of his visit to the 1957 WESCON show at which he was featured. Posing at a lab bench with Bill Hewlett and Barney Oliver was no more than somebody's idea of a nifty photo opportunity.

Someone who actually was working at HP at the time was Cy Elwell, by whom de Forest was employed at the early part of his career. It was clear from Cy's many stories of the old days that de Forest was definitely not a favorite of his. Yet pictures taken during that same visit show Cy and de Forest smiling at each other, even shaking hands, or perhaps with arms draped around shoulders—I can't recall for sure.

Interested parties who want to know more about de Forest's deserved position—or lack of same—in the early history of electronics would do well to read the autobiography of de Forest, Lessing's biography of E.H. Armstrong, and Tom Lewis' recent book on de Forest, Armstrong, and Sarnoff.

Larry Johnson
Los Altos, Calif.

**NASA And Me (Or You)**

Regarding the Jan. 20 Technology Briefing *("To Infinity And Beyond!" p. 20)*:

I agree completely with your agenda for NASA, but don't go to work there. The first thing that will happen is that you will find out that there are rules against lobbying and advertising—after all, NASA already gets government money and it is somehow unfair for it to act like it is important in the "eyes of the customer." Your PR activities would be taken as having the appearance of self-promotion and that would be too much for the ethics department to have to deal with.

It's a real conundrum. If there was a way to work in space R&D without using government money, I'd be working there already; but there isn't, at least not yet. I could work for a private company, but I still couldn't do this work except on contract to the government. As it is, since this is the only source of funding for space exploration, I currently work as close to the top of the food chain (and at the best place within the "stupid rules laden" system) as I can get—JPL.

More power to you. I'd like to see your editorial on the front page of the Los Angeles Times (with them in favor, of course).

Courtney.Duncan@Jpl.Nasa.Gov
via e-mail

## Strong Communication Skills Improve Advancement Possibilities

### Robert Keenan

Attitudes and philosophies are changing in today's business world. Gone are the hierarchal structures of the 1950s, 60s, and 70s. Enter flatter organizations and cross-functional teams in the 90s. These new approaches have reinvented traditional company cultures. All employees in today's business environment, especially engineers, have had to adapt to these changes to survive and succeed.

In the past, engineers were perceived simply as people sitting at workbenches designing projects morning, noon, and night. Managers saw engineers as the behind-the-scenes players who developed the company's products. But now, engineers are seen by managers as important business tools who develop manufacturable products while cutting costs through extensive interaction with marketeers, sales personnel, and customers.One of the musts in this environment is having a firm grasp on the technology. At the same time, however, the development of strong communication skills is becoming a growing necessity for engineers.

Norm Tarowsky, education manager for Hewlett-Packard (HP) Co.'s Components Group, San Jose, Calif., says that possessing good communication skills is extremely important for engineers. He says that companies in the past saw engineers as people who worked in the backroom. However, Tarowsky says that companies now view engineers as people who have to work in teams, collaborate with people on a worldwide basis, and also work with other departments when developing products. To operate in these environments, HP needs engineers with strong communication skills.

Lucent Technologies' Microelectronics Group, Berkeley Heights, N.J. also wants their engineers to have excellent communication skills. For example, Judy Miller, senior manager of Microelectronics International University for Lucent, says that in a factory setting, engineers must have the ability to communicate changes and in high-level designs to the non-technical hourly workers *(see "Improving Oral Communication Skills," p.185)*.

Overall, engineers need to improve interpersonal skills that encompass reading, writing, oral, listening, and critical thinking skills. One of the programs developed at the college level to address these issues for young engineers is the WRITETALK Communication System.

**WRITETALK**

The WRITETALK Communication System is set up to improve engineering communication skills on college campuses. IEEE President Charles Alexander and James Watson, president of Watson Associates, Mansfield, Ohio, developed the program in 1987 with the help of Wayne Bennett. According to Alexander, the basis for WRITETALK is to incorporate programs to improve communication skills in the engineering curriculum, not through additional courses outside the core engineering program. He says that separate courses—such as public speaking and composition—do not instill the importance of communication to young engineers. By implementing communication topics in a technical curriculum, young engineers will learn the importance of these skills.

> **An engineer's success is directly proportional to his or her ability to communicate.**

According to Watson, the goal of the WRITETALK program is to help students become aware of and develop a process for gaining good communication skills. The program is designed to improve a wide variety of communication skill sets such as effective technical communication, time management, memo writing, resume and cover-letter writing, oral presentations, listening skills, group interaction, interpersonal skills, and laboratory report writing.

Alexander says that improving these skills allows engineers to be more successful in the workplace. "An engineer's success is directly proportional to his or her ability to communicate," he says.

Rutgers' Wireless Information Networking Laboratory (WINLAB) New Brunswick, N.J., and Virginia Tech's Mobile and Portable Research Group (MPRG), Blacksburg, Va., do not use the WRITETALK program, but incorporate developing communication skills in their engineering classes. At WINLAB, the development of communication skills in the technical curriculum arrives in the form of writing papers and oral presentations. Jack Holtzman, professor of electrical and computer engineering and associate director of WINLAB, agrees that incorporating these skills in technical classes raises their importance in students' minds.

Holtzman notes that one major communication problem students have is selecting information when making presentations. "Students tend to flood the audience with details," he says. By incorporating presentations into course work and providing feedback, WINLAB students learn how to stress the main points and main conclusion of their presentations. "It makes them think: Why am I doing this and what's important?" adds Holtzman.

Ted Rappaport, professor of electrical engineering and director of MPRG, says that during the past few years, industry companies have conveyed a need for engineers that can write and communicate effectively. Like Rutgers, MPRG incorporates project and oral presentation components to its class work. Beyond that, graduate students make presentations to potential MPRG sponsors. "Their ability to convince sponsors about the importance of their research is how we stay in business," says Rappaport.

Rappaport indicates that his students are savvy and demonstrate good oral communication skills when an audience is defined for them. However, he is concerned about student's writing skills. "This is one skill that we could do better across the board," he adds. As a result, graduate students spend as much time on improving writing skills as they do on enhancing research and analytical skills in the MPRG program.

Overall, MPRG and WINLAB have seen success when incorporating communication skills in their technical programs. Rappaport says that program-sponsor companies favorably remark on MPRG graduate's communication skills.

Holtzman says that the feedback he receives on WINLAB's graduates is that they have a running head start due to the total education package—which includes their communication skills.

### Training Programs

But young engineers only make up a part of the total wireless community. To help engineers on staff, companies have turned to training programs to

# Improving Oral Communication Skills

When the word "communication" is mentioned to most engineers, thoughts of RF transmission and Internet connection immediately jump into mind. But, the word also has another meaning. In today's business environment, more engineers are working in teams, dealing with customers, and making presentations at trade shows and conferences. In this environment, the engineer must be an efffective communicator.

One communication skill most companies look for in an engineer is strong oral skills. As a result, engineers who improve their oral skills are a more marketable commodity.

Here are some tips that can help engineers improve their oral communication skills.

*1. Know Your Audience*—Today's engineers increasingly find themselves making presentations to customers, team members, and management. In an August 1995 article in the *Public Relations Journal*, James Beckham, Jr. says that to better deal with customers or companies, a speaker must identify topics that are important to the audience.

James Watson, president of Watson Associates, Mansfield, Ohio, agrees. In *The Communication Connection*, Watson says, "Each audience member is different in their need for information. It is important to recognize different needs."

*2. Anecdotes*—In any oral communication situation, formal or informal, anecdotes can improve the quality of a presentation. By using anecdotes or stories, the engineer can make points clearer to the audience, and the audience can more easily relate to the speech.

"Think of the last time you were sitting with friends and wanted to express an idea or make a particular point. You probably told a story to bring that point home," Beckham says. He adds that anecdotes are one technique that can be used to make a thought more understandable.

*3. Delivery*—Preparation is very important in any oral communication situation. But, delivery is equally as important. If not properly delivered, even the best researched speeches or sales presentations may flop.

One way to effectively deliver a presentation is rehearsal. Through rehearsal, an engineer first becomes acquainted with the presentation.

Acquaintance with the speech, however, is only half the battle. In her book *"How to Write & Give a Speech"* (St. Martin's Press, New York, 1992), Joan Detz says that presenters should become comfortable with the gestures, pauses, and emphases they will use during the speech. "It is not enough to know the content of your speech," she says. Detz suggests that people rehearse their presentation in front of a mirror or a small group.

When delivering a presentation, good eye contact also is vital. "When you look at people, they believe you care about them," Detz says. By looking audience members directly in the eye, Detz says that the speaker creates sincerity. She adds that by making contact with as many people as possible, the speaker can get the audience more involved in the speech.

Eye contact also provides immediate feedback to the presenter. By making visual contact with audience members, an engineer can tell how he or she is doing and can make adjustments during the speech to increase audience interest.

During delivery, the speaker should consider rate, variety, emphasis, clarity, volume, and rhythm. By evaluating all of these areas during rehearsal, the overall effectiveness of the presentation can be improved. Another delivery tip is to avoid reading a speech word-for-word. A better technique is to develop an outline which serves as a guide to the presentation.

*4. Style*—Presenters must develop their own style when making an oral presentation. According to Watson, style cannot be taught.

In the March 1994 issue of *Boardoom Reports*, Ed English, public speaking trainer for the American Management Association, Leawood, Kans., says that presenters must perfect the communication styles and techniques that work best for them. "What works for one person might not help another."

improve communication skills.

Lucent, Motorola, and HP offer development programs for engineering staff members. Engineers meet with their managers and decide on the skills that need improvement. Communication skills are one topic covered in these meetings. Once an engineer decides what communication skills need to be improved, he or she seeks out a course or courses to respond to those needs.

Lucent, Motorola, and HP offer many different avenues for technical people to improve their communication skills. Solutions are available through classroom environments, seminars, workshops, satellite conferencing, CD-ROMs, the Internet, and local-area network (LAN)-based systems.

One reason for several teaching platforms is time constraints on engineers. "It seems like engineering time is precious," Lucent's Miller says. "It is tough for engineers to break away from work." However, Miller says the classroom environment is not being eliminated—particularly for communication courses.

Clearly, companies stand to benefit by encouraging engineers to improve their communication skills. Sandy Pallett, regional training consultant for Motorola University, Tempe, Ariz., says that by encouraging engineers to hone their communication skills, Motorola believes that it can meet customer needs better and gain a competitive advantage in the marketplace.

Not surprisingly, engineers have started to realize the need for improved communication skills. "I think the recognition is there," Pallett says. "Engineers realize that in order to get their work done they have to talk to and influence another human being."

*Robert Keenan is an associate editor at Wireless Systems Design Magazine. He may be contacted at 611 Route 46 West, Hasbrouck Heights, NJ 07604; (201) 393-6250; e-mail: robkwsd@aol.com.*

| How Valuable | Circle |
|---|---|
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| Moderately | 549 |
| Slightly | 550 |

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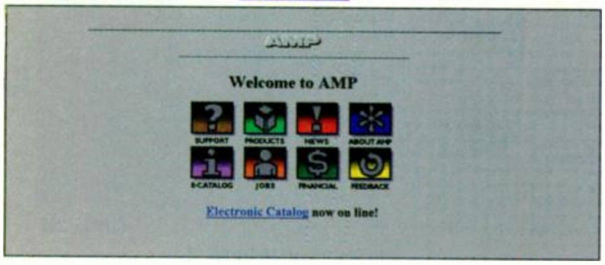


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# ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

## ROM Short Form

AMI's masked ROMs offer low-power, drop-in replacement for EPROMs without the added cost. The 3-volt parts work in 2.7- to 3.6-volt battery applications. The low-volt devices work in 3- to 5.5-volt applications. For information on AMI's masked ROMs, call Tamara Drake, (208) 233-4690 or visit our home page at http://www.amis.com.


CIRCLE 250

**AMERICAN MICROSYSTEMS INC.**

## SINGLE BOARD COMPUTERS

ICP Acquire Inc. is a manufacture of single Board computers, provide Backplane, rackmount chassis , and Industrial Power supplies. Including: 3-20Slot BP, 386/486/Pentium SBC, 3-20Slot chassis, DC-12V/24V-48V PS and 85-265V AC PS. Contact Allen, phone: 415-967-7168


CIRCLE 251

**ICP ACQUIRE, INC.**

## HI PERF CABLE ASSEMBLIES

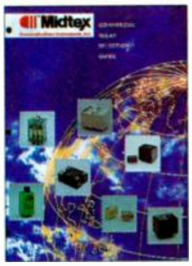
Brochure for engineers needing to know the current level of advanced capabilities in the integrated design and manufacture of microminiature cables and high density terminations.

CIRCLE 252

**PRECISION INTERCONNECT**

## COMMERCIAL RELAY SELECTION GUIDE

Informative 12-page relay selection guide features Midtex's broad line of industrial and general purpose relays. Midtex designs, manufactures and markets low-level relays. Midtex designs, manufactures and markets low-level relays, PC board power relays, general purpose relays rated at 3 Amps to 15 Amps to 30 Amps, time delay relays and solid state relays. Call (915) 772-1061 for a free Commercial Relay Selection

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**MIDTEX**

## RF/IF DESIGNER'S GUIDE

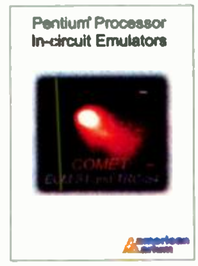
180 page RF/IF Designer's Guide is looked with informative features such as practical articles, definitions of terms, environmental and reliability test procedures, answers to frequently asked surface mount technology questions, and more! It also contains the most complete and up-to-date specifications and price information about all Mini-Circuits signal processing components.


CIRCLE 254

**MINI-CIRCUITS**

## COMET IN-CIRCUIT EMULATORS

American Arium has been the primary market supplier of Pentium® processor In-circuit Emulators since 1991. In 1995, the company introduced their Pentium® Pro In-circuit Emulator. Recently, American Arium announced the release of Comet In-Circuit Emulators. These were specifically designed for the embedded software developer, with special attention paid to the 66Mz real-time trace engine and ultra-accurate breakpoints. The Comet ECM-54 is a portable low cost solution which provides processor control through the Intel defined, JTAG debug port. Comet TRC-54 is a full featured In-Circuit Emulator with American Arium Data Capture Technology.




CIRCLE 255

**AMERICAN ARIUM**

## CRYSTAL OSCILLATOR CATALOG

A new product catalog and selection guide from Champion technologies features their full line of crystal oscillators. Technical information, specifications and mechanicals are featured in this catalog for over 60 of Champion's VXCOs, TCXOs, VCTCXOs, data clocks and related products. Frequency ranges up to 155.52 MHz for general purpose to high frequency or tight stability applications.

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**CHAMPION TECHNOLOGIES**

## DEVICE PROGRAMMERS & HANDLERS

The Data I/OÒ catalog is the direct-order source of affordable tools for users of programmable devices. From design software to device programming and automated handling systems, the Data I/O catalog offers unbeatable values on the high quality tools you need. Call 1-800-332-8246, ext. 806


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**DATA I/O**

## INTERNATIONAL SOURCE BOOK

The International Source Book offers detailed specifications on Ecliptek's through-hole and surface-mount crystals, oscillators, and inductors. Visit our internet site at http://www.ecliptek.com.
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**IRONWOOD ELECTRONICS**

## 1997 DATA ACQUISITION CATALOG

IOtech's 1997 catalog describes its PC-based data acquisition and IEEE 488 hardware and software products. These include parallel-port- and PCMCIA-based portable data acquisition systems; ISA-bus-based data acquisition boards; associated signal-conditioning products; and IEEE488 instruments, controllers, and accessories. Tel: (216) 439-4091 Fax: (216) 439-4093 E-mail: sales@iotech.com WWW: http://www.iotech.com

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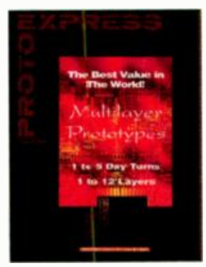
**IOtech, Inc.**

## MULTILAYER PROTOTYPE

Award winning quick turn multilayer prototype manufacture specializing in 24 hour to 5 day turns, for commercial and milspec boards (Milp-55110E) on FR4 and polyimide materials. Our capabilities also include "blind and buried" vias, full body gold, carbon baste, metal core boards, small hole drilling, and net list testing.

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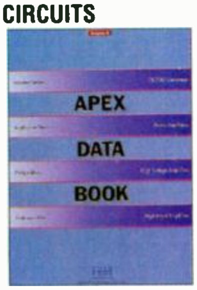
**PROTO EXPRESS**

## POWER INTEGRATED CIRCUITS

The 7th edition Apex Power Integrated Circuits data book contains complete product data sheets and applications notes for Apex Microtechnology's power Amplifier PWM Amplifier and DC/DC Converter product lines. Call: 1-800-862-1021; Fax: 1-520-888-3329; Email: Prolit@TeamApex.com

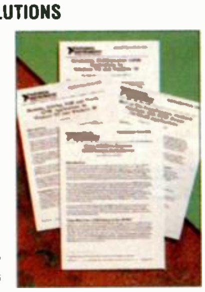



CIRCLE 262

**APEX**

## WINDOWS NT/95 GPIB SOLUTIONS

National Instruments delivers four new application notes to ease test system development. Enhance system performance with HS488 - the new standard for high-speed GPIB, handle GPIB events using asynchronous callback functions, develop multithreaded GPIB applications and run existing DOS/win 16 GPIB Applications, all with industry standard NI488.2M software for windows NT and windows 95.



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**NATIONAL INSTRUMENTS**

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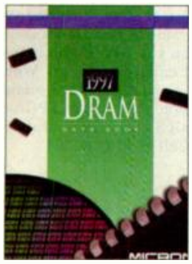
**YOUR COMPANY**

# ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

## 1997 DRAM DATA BOOK

Virtually the entire book is new! Features Micron sync DRAM data sheets, SDRAM DIMMs and SODIMMs, updated info on -5 EDO timing, plus new data on the SGRAM and SGRAM SODIMMs. Includes waveforms, block diagrams, timing parameters and more, in over 1,100 pages. Request your copy today!
www.micron.com/mti

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MICRON SEMICONDUCTOR

## POLYFOLD AIR FILTERS

Polyfold air filters from Universal Air filter are the company's newest entries into general purpose air filtration where high dust holding capacity and low resistance are required. The filter comes in both permanent and disposable models. Uni-Foam media is used in permanent models and polyester media is used in disposable varieties. Polyfold filters meet the following standards and classifications: UL Class 2, UL 94 HF-1; Bellcore TR-NWT-000078 and more.


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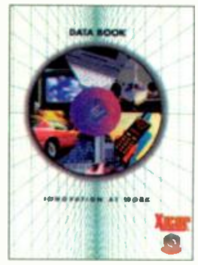
UNIVERSAL AIR FILTER

## FREE! FREE! FREE!

Xicor's broad line of in-the-system programmable semiconductor integrated circuits retain information even when system power is lost or turned off. In-the-system programmability telecommunications, consumer, computer industrial, automotive and military products to adapt to changing software and operation environments. Call (408) 432-8888 Ext. 3336.

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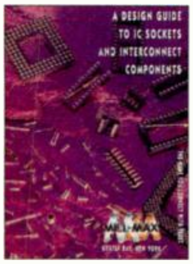
XICOR

## DESIGN GUIDE TO IC SOCKETS

MILL-MAX features its newly expanded family of precision machined interconnect components including PCB pins, wrapost & solder terminals plus a complete line of SIP, DIP & PGA sockets. The guide highlights over 70 new products in pins, surface mount components & large I/O PGA sockets. A glossary, application notes make the MILL-MAX catalog your primary resource for Maximum Interconnect Solutions.

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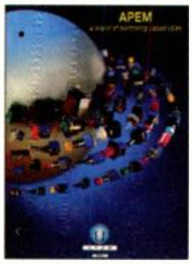
MILL-MAX

## JUMBO CATALOG

APEM's jumbo 340 page catalog features: Subminі & mini toggles, rockers, paddles & pushbuttons, including washables. DIP switches including models for automatic insertion, surface mounting and washables. Industrial toggles, rockers, paddles & pushbuttons, including lighted models and antivandal pushbuttons. Extensive offerings of switch hardware and accessories, including sealing boots and indicator lights.




CIRCLE 269

APEM

## 80186, 80196, 8051 EMULATION

Signum Systems has released its 1996 catalog of in-circuit emulators. This full line catalog includes Intel processors, Texas Instruments DSP's Zilog controllers, and National Semiconductor HPC family. Call (800) 838-8012 for information. Internet address: ww.signum.com


CIRCLE 270

SIGNUM SYSTEMS

## HARTING har-mik

Harting har-mik 4 color brochure shows and describes comprehensive range of 0.050" pitch miniature connectors designed to meet the requirements of Internal and External connections of the future. Reduced size: contact density. 847/519-7700 or Fax: 847/519-9771.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Tanner Research offers powerful, easy to use, PC/MAC/Unix design tools for IC, MCM and MEMS applications. Output CIF & GDSIL. Send for free demo and literature, or download from our web page at www.tanner.com. PH: 818-792-3000, Fax: 818-792-0300, E-Mail: sales@tanner.com


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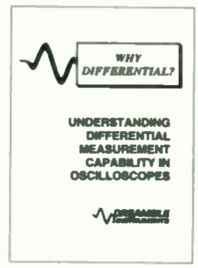
TANNER RESEARCH

## DIFFERENTIAL MEASUREMENTS

A discussion of sing;e-ended and differential scope measurements on ground referenced and floating signals. differential amplifier characteristics such as common mode rejection ratio and commen mode range are covered. 1-800-376-7007

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PREAMBLE INSTRUMENTS

## TELECOM SOLUTIONS DATABOOK

Teltone's 224-page Databook features a wide range of products for network interface applications, including: DTMF Receivers, DTMF Transceivers w/Call Progress Detection, MF Trunk Signaling ICs, Call Progress Tone Detectors, Line Sensing Relays, test tools including Telephone Line Simulators and ISDN Line Simulators, application notes, and more. For your copy call 1-800-426-3926 or 206-487-1515, E-mail at info@teltone.com.


CIRCLE 274

TELTONE

## "X86 and 683xx/HC16 Design Tips"

Free application note shows how to use in-circuit emulation to isolate real-time events. Set clock-edge triggers, and then use trace to display system status and the source code leading up to the event. For immediate response: WEB page: www.microtekintl.com
Voice: 800-886-7333


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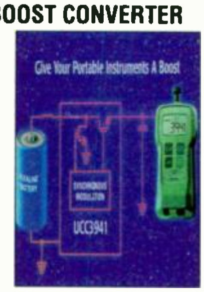
MICROTEK INTERNATIONAL

## 1V SYNCHRONOUS BOOST CONVERTER

Unitrode Corporation's UCC3941, a 1V synchronous boost converter, is optimized to operate from low input voltages such as those provided from a single or dual cell battery. Ideal for demanding applications such as pages and PDAs, the UCC3941's wide input voltage range can also accommodate such power sources as alkaline, NiCd and NiMH batteries. For more information, please contact Mickey McClure at (603) 424-2410.

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UNITRODE

## MicroSim® DesignLab™

Interface Technologies distributes Version 7.1 of MicroSim DesignLab and MicroSim Pspice A/D with Schematics. Version 7.1 supports long file names in Windows 95 and Windows NT, includes DXF export, enhanced simulation libraries, library browser and search engine, and automated move, select and edit in MicroSim PCBoards. Call 1-800-357-1636 or browse http://www.i-t.com for more information.


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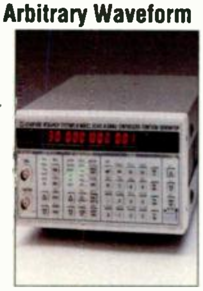
INTERFACE TECHNOLOGIES

## 30 MHz Function and Arbitrary Waveform

The DS345 creates synthesized (DDS) sine, square, triangle and ramp waveforms with 1 mHz frequency resolution. Arbitrary Waveforms of up to 16k points with 12 bit resolution can also be generated. Capabilities include AM, FM, PM and burst mode as well as linear and logarithmic frequency sweeps. The GPIB and RS-232 interface option provides easy communication with computers and includes software for creating arbitrary waveforms.



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STANFORD RESEARCH SYSTEMS

## Short-Form RAFI Switch Catalog

A 36 page catalog, "A Selection of RAFI Products, No. 9608," features a select group of RAFI nonilluminated and illuminated pushtutton switches, keylock and selector switches. Drawings, specifications, accessories and complete part numbers are included. Most RAFI components are VDE approved; some are UL recognized and CSA certified. Contact Gina Wegner, (800) 334-7729.


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C&K COMPONENTS, INC.

# ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

## SWITCHING POWER SUPPLIES

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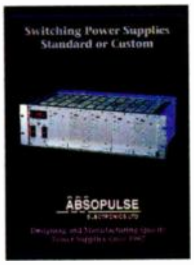


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ABSOPULSE ELECTRONICS LTD.

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ACCUTRACE INC.

## MACINTOSH-BASED EDA TOOLS

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CAPILANO COMPUTING

## ON-LINE CATALOG

Visit http://www.keyelso.com and quickly locate up-to-date Electronic Hardware and Interconnect Components. Website includes photos, drawings and specifications. Listings include PCB Components & Hardware, Interconnect Components, Battery Connectors & Holders, Mechanical Hardware, Panel Hardware plus a monthly product spotlight. General information such as capabilities and ISO 9002 are clearly defined.


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KEYSTONE ELECTRONICS CORP.

## THE SMARTEST PROGRAMMER

The catalog covers our entire product line and includes comprehensive supported device listings, all available options and features, and a complete price list. For information, call Yvon J. Blais Phone: (407) 649-3335, FAX: (407) 649-3310


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DATAMAN

## LOW COST 16-BIT CONTROLLERS

Easy to program in Borland/Microsoft C/C++. Low Cost, High quality, Reliable, Compact, Made in U.S.A. More than 20 controllers with ADC, DAC, solenoid drivers, relay, PC-104, PCMCIA, LCD, DSP motion control, 10 UARTs, 100 I/Os. For industrial control, test, and data acquisition. Customer boards design. Save time and money. Phone: 916-758-0180, FAX: 916-758-0181. tern@netcom.com
http://www.tern.com


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TERN, INC.

## V-SYSTEM/VLOG

Model Technology offers simulations for VHDL, Verilog and mixed-HDL on workstation and PC platforms. Model Technology provides technology- leading solutions for all your ASIC and FPGA needs. Model Technology's suite of HDL tools are fully compliant with leading industry standards. For more information, call 503-641-1340 or visit our home page http://www.model.com


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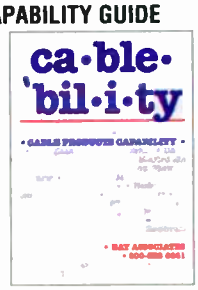
MODEL TECHNOLOGY

## CABLE PRODUCTS CAPABILITY GUIDE

Designed to aid engineers in their cable, wire, assembly, and high-tech interconnect applications, this free Cable Products Capability Guide from Bay Associates, Menlo Park, CA, features the company's unique products, services, materials and processes.

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BAY ASSOCIATES

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Master Bond Inc., Hackensack, NJ manufactures over 3000 grades of adhesives, sealants and coatings. Line cosists of epoxies, anaecobics, cyanoacrylates, silicones and acrylics. One and two part systems are available. Tel 201-343-8983.


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MASTER BOND INC.

## RELIABILITY PREDICTION

Catalog describes the RelCalc2 software package, which automates Mil-HDBK-217 or Bellcore on your PC, and allows quick and easy reliability analysis of your electronic products. Phone: (818) 991-0057, Fax: (818) 991-1281

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T-CUBED SYSTEMS

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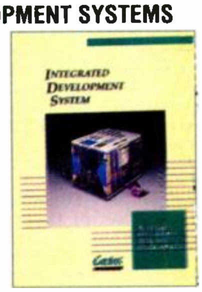
Z-WORLD ENGINEERING

## INTEGRATED DEVELOPMENT SYSTEMS

IN CIRCUIT EMULATORS FROM CACTUS LOGIC PROVIDE REAL TIME, SOURCE LEVEL DEBUGGING FOR 8051, 68HC11,Z80/180, 6502,80251, AND 8085 FAMILIES OF MICROPROCESSORS.

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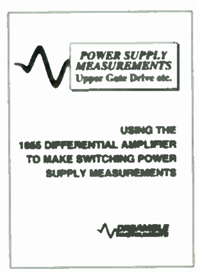
CACTUS LOGIC

## APPLICATION NOTE

Covers how to make safe and reliable measurements on switching power supplies operating on line. Includes such difficult measurements as upper gate drive and transistor saturation characteristics. Tells how to quantity measurement corruption caused by high dv/dt common mode. 1-800-376-7007

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PREAMBLE INSTRUMENTS

# ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

## PRECISION-EXPANDED

MicroGrid precision expanded foils in ferrous, nonferrous, precious and alloyed metals. light, flexible, mesh-like material for EMI/RFI/ESD shielding, electrical and heat conductivity. Process variations include: annealing, stretching, flattening & sellvage edging.

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**DELKER CORPORATION**

## THE MULTICHIP PRODUCTS DIVISION

The Multichip Products Division of American Microsystems, Inc. provides design, manufacture and test services to customers needing a multichip solution. AMI offers a full range of substrate, die attach and packaging for multichip products. For more information on MPD, call (208) 233-4690 or visit our home page http://www.amis.com

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**AMERICAN MICROSYSTEMS INC.**

## OFF-THE-SHELF-OPTICS

Free 130 page product catalog from Rolyn, largest supplier of off-the-shelf optics. 24 hour delivery of simple or compound lenses, filters, prisms, mirrors, beamsplitters, reticles, objectives, eyepieces & thousands of other stock items. Custom products & coatings also. Phone: (818)915-5707, Fax: (818) 915-1379

CIRCLE 297

**ROLYN OPTICS CO.**

## FLAT FLEX CABLE

Meritec's Multi-signal Interconnects Terminated to Flat Flex Cable. This cable assembly saves space, is cost effective and easy to install. The low profile. overmolded strain relief is designed for critical mechanical applications. The folding and flexing features of the flax flex cable solve difficult routing requirements. The assemblies are available with 31 or 41 conductors.

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**MERITEC**

## W65C02S - BASED PRODUCTS

Western Design Center's product selection and developer guide describes our 65C02-BASED CMOS low power IC microprocessors. Included is information about our chips, boards and licensable cores.

www.wdesignc.com.


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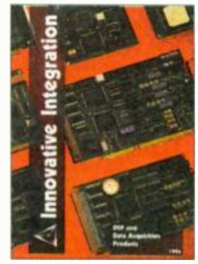
**WESTERN DESIGN CENTER**

## INNOVATIVE INTEGRATION

Innovative Integration sells Blazingly Fast Data Acquisition Products. FREE DSP & Data Acquisition Products Catalog Call 818-865-6150, Fax: 818-879-1770. Email: techsprt@innovativedsp.com or web: http://www.innovativedsp.com

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**INNOVATIVE INTEGRATION**

## MODEL TECHNOLOGY

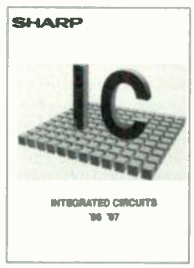
Model Technology offers simulation solutions for VHDL, Verilog and mixed-HDL on Workstation an PC platforms. Model Technology provides technology-leading solutions for all your ASIC and FPGA needs. Model Technology's suite of HDL tools are fully compliant with leading industry standards. For more information, call 503-641-1340 or visit our home page http://www.model.com


CIRCLE 302

**MODEL TECHNOLOGY**

## SHARP FIFOs

First-in, First-out memories are just the stuff the no-nonsense design environment of the '90s is meant to build on. Used as data buffers between systems operating at different speeds, FIFOs conserve valuable board space, streamline design tasks and reduce system cost. Sharp's new 1997 IC Short Form Catalog is packed with information about Sharp FIFOs.

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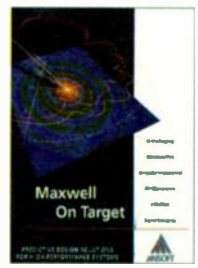
**SHARP MICROELECTRONICS**

## MAXWELL ON TARGET

Electromagnetics based EDA solutions for high speed and high frequency design. 2D/3D RLGC extraction and SPICE model generation for high speed interconnects, IC packages. Signal integrity, ground bounce, and EMI enclosure design rules. S-parameters, antenna parameters including gain, directivity for RF and microwave design.




CIRCLE 304

**ANSOFT**

## A WEALTH OF SWITCH INFORMATION

Grayhill's 320 page catalog provides you with electromechanical switch data, reference material, dimensional drawings and photos. Catalog No. 1 includes information on DIP Switches, rotary Switches, Keyboards and Keyboard Modules. the detailed information allows the catalog user to select the proper product for their application right down to the part number. Phone: (708) 482-2131. Fax: (708) 345-2820.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**GRAYHILL, INC.**

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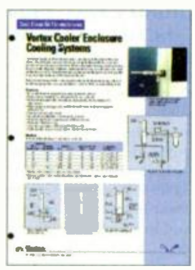


CIRCLE 306

**ITW VORTEC**

## NEW SWITCHING REGULATORS

Power Trends, Inc. has released a new 80 page full-line catalog for its complete line of Integrated Switching Regulators and DC to DC converters. the catalog introduces significant new products along with extensions to existing product lines. Complete specifications, photos and standard applications are provided for each product along with mechanical configuration options and ordering information.


CIRCLE 307

**POWER TRENDS, INC.**

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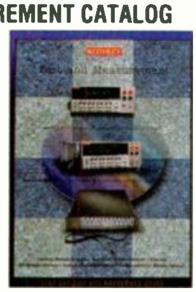
## NEW TEST & MEASUREMENT CATALOG

Keithley offers its new 1997 catalog of test and measurement instruments including DMMs, electrometers, precision sources, voltmeters, source-measure units, power supplies, switch systems and more. Phone: 800/552-1115. FAX: 216/248-6168 http:// www.keithley.com



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# ELECTRONIC DESIGN CATALOG/LITERATURE REVIEW

## OMRON RELAYS, SWITCHES, MORE

Standard Product Catalog shows Omron's most popular relays, switches, and sensors. The 176 page catalog also includes card readers, time delay relays, totalizers, limit switches and temperature controllers. Literature sent only to addresses in the U.S.A. Omron Electronics, Inc. Call toll-free 1-800-55-OMRON or e-mail EDLit@oei.omron.com


CIRCLE 308

OMRON ELECTRONICS, INC.

## P&B RELAYS & BREAKERS

Catalog lists stock relays and circuit breakers from Potter & Brumfield products division. Describes electromechanical, solid state and time delays, as well as thermal and magnetic circuit breakers. Numerous options. Fax: (812) 386-2072, email: info@ae.sec.siemens.com


CIRCLE 309

SIEMENS ELECTROMECHANICAL

## NEW SWITCH CATALOG

The ALL-NEW, color E-Switch catalog contains 28 additional pages, including new lines of DIP, pushbutton, and gold tact switches. The catalog gives complete specifications for pushbutton, toggle, rocker, power, lever, slide, rotary, keylock, DIP, and tact switches. SMT and lighted versions available. 612-504-3525, http://www.e-switch.com.


CIRCLE 310

E-SWITCH

## ENCLOSURES & ACCESSORIES AVAILABLE

Bud Industries' new Standard Products Catalog provides technical data and ordering information on over 3,000 products ranging from large relay racks and cabinets to desktop and portable instrument cases including a full line of NEMA and other plastic enclosures. Also included is information on computer workstations, custom fabrication and a wide range of enclosure accessories.

CIRCLE 311

BUD INDUSTRIES, INC.

## B&K PRECISION

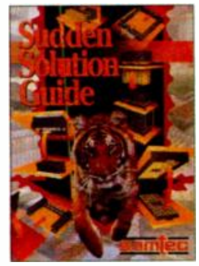
B&K Precision's full line catalog features their family or Universal Device Programmers which offer comprehensive device libraries, excellent performance, and high flexibility at a competitive price. Four different models program EPROMs, EEPROMs, Flash Memories, MICROs, PALs, EPLDs, GALs, PEELs, EPLAs, and bipolar PROM devices, and they are ideal for TTL, CMOs, DRAM and SRAM IC resting.

CIRCLE 312

B&K PRECISION

## NEW FULL LINE SAMTEC CATALOG

Samtec's new Sudden Solutions Guide F-197 features Board Interface Systems for unique solutions for card-to-board, board-to-board and off-board applications. Patented flex-card systems, micro, surface mount and standard pitch board-to-board systems, and right-angle and cable systems are shown. Phone: 800-SAMTEC-9 (800-726-8329) Fax: 812-948-5047.

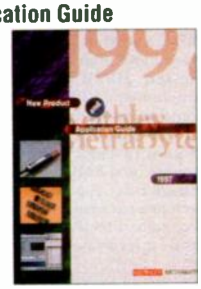



CIRCLE 313

SAMTEC

## New Product & Application Guide

This new Keithley Metra-Byte publication covers board-level data acquisition and communication products, including multi-function analog, digital I/O, and stepper-motor control boards; signal conditioning accessories; PC-based instruments; and PC/IEEE 488 and RS-232/422/485 interfaces. Also covered are data acquisition



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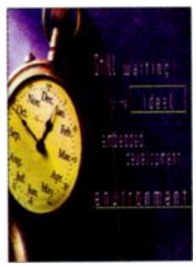

CIRCLE 315

MICROTEC

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CIRCLE 316

APPLIED MICROSYSTEMS

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The OrCAD Desktop Solutions demo CD is filled with everything you'll need to evaluate out solutions. and try them out with your own designs: product overviews, data sheets, third-party information, evaluation versions of OrCAD's software, and more, Call OrCAD DIRECT at 1-800-671-9505 or visit our web site at http://www.orcad.com


CIRCLE 317

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## OrCAD Layout Products

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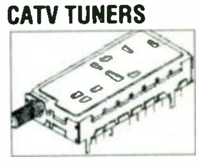
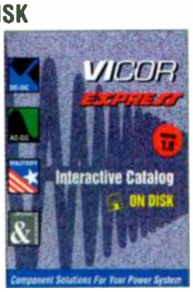


CIRCLE 319

SHARP MICROELECTRONICS

## FREE CATALOG ON DISK

Vicor's interactive electronic catalog guides users through the selection and configuration process for the company's complete line of modular power solutions. Contact: Vicor Express. Phone: 800-735-6200 E-mail: vicorexp@vicr.com

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## THERM-O-DISC

This new20 page catalog showcases Therm-O-Disc's full line of NTC and PTC thermistors including disc, rod, glass encapsulated, and the new surface mount configurations, plus inrush current suppressors, ceramic current limiters, linear PTC's, temperature switches, varistors and NTC assemblies.
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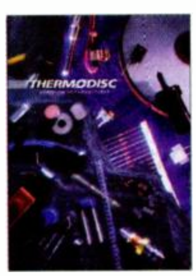


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THERM-O-DISC.

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| May 27 | 4/17/97 |
| June 9 | 4/30/97 |
| June 23 | 5/14/97 |
| July 7 | 5/29/97 |
| July 21 | 6/11/97 |
| August 4 | 6/25/97 |
| August 18 | 7/9/97 |
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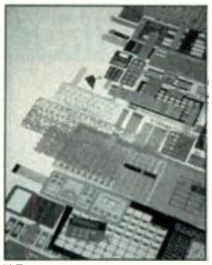
| October 1 | 8/22/97 |
| October 13 | 9/3/97 |
| October 23 | 9/12/97 |
| November 3 | 9/24/97 |
| November 17 | 10/8/97 |
| December 1 | 10/22/97 |
| December 15 | 11/5/97 |


LOGICAL DEVICES CIRCLE 408



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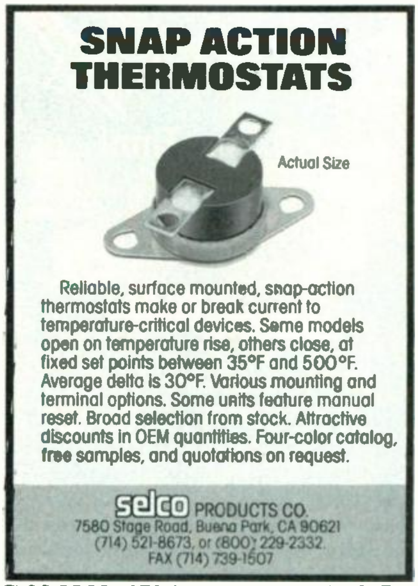


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| POWER TRENDS | 307 | 191 |
| POWER TRENDS | 160 | 47 |
| PREAMBLE INSTRUMENTS | 273,294 | 189,190 |
| PRECISION INTERCONNECT | 205 | 121 |
| PRECISION INTERCONNECT | 252 | 188 |
| PRODIGIT ELECTRONICS | 426 | 197 |
| PROTO EXPRESS | 415,261 | 193,188 |
| QUICKLOGIC | 181 | 103 |
| ROLYN OPTICS | 297 | 191 |
| SAMSUNG SEMICONDUCTOR | 180 | 80HHII* |
| SAMTEC USA | 313 | 192 |
| SAMTEC USA | 163 | 104 |
| SELCO PRODUCTS CO. | 417 | 195 |
| SGS-THOMSON | 142 | 80RST* |
| SHARP | 303,319 | 191,192 |
| SHARP | 233 | 80LM* |
| SHINDENGEN AMERICA | 164 | 80EE* |
| SIEMENS | 305 | 192 |
| SIEMENS AG | 165 | 34-35 |
| SIEMENS COMPONENTS | 230 | 45* |
| SIGNATEC | 418 | 194 |
| SIGNUM SYSTEMS | 270,419 | 189,193 |
| SIPEX CORPORATION | 166 | 147 |
| SMART MODULAR | 191 | 82 |
| SOFTWARE SYSTEMS VERTRIEB | 427 | 197 |
| STANFORD RESEARCH SYSTEMS | 278 | 189 |
| SYNERGY SEMICONDUCTOR | 167 | 78-79 |
| T-CUBED SYSTEMS | 289 | 190 |
| TANNER RESEARCH | 420 | 195 |
| TANNER RESEARCH | 272 | 189 |
| TECHRON | 168 | 123 |
| TEKTRONIX | - | 69* |
| TEKTRONIX | - | 77* |
| TEKTRONIX | - | 109* |
| TEKTRONIX | - | 119* |
| TELTONE | 274 | 189 |
| TEMIC | 169 | 13 |
| TERN, INC. | 285,421 | 190,196 |
| TEXAS INSTRUMENTS | 170 | 80Q* |
| TEXAS INSTRUMENTS | 172 | 48-49 |
| TEXAS INSTRUMENTS | 171 | 80KK* |
| THERM-O-DISC | 173,321 | 120,192 |
| TRILOGY DESIGN | 422 | 196 |
| UNITRODE | 276 | 189 |
| UNIVERSAL AIR | 174 | 120 |
| UNIVERSAL AIR FILTER | 266 | 189 |
| VACUUMSCHMELZE GMBH | 175 | 139 |
| VICOR | 176,320 | 91,192 |
| VITESSE SEMICONDUCTOR | 185 | 6 |
| WESTERN DESIGN CENTER | 299 | 191 |
| XICOR, INC. | 206,207 | 36,157 |
| XICOR, INC. | 267 | 189 |
| XILINX | 178 | 29 |
| Z-WORLD ENGINEERING | 292,423 | 190,193 |
| Z-WORLD ENGINEERING | 179 | 161 |

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International **

# ELECTRONIC DESIGN

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1. Your Project Responsibility: Are you involved with Design/ Development projects? 1. Yes ☐ 2. No ☐

2. Your principal job responsibility: (check one only)
   1. ☐ Design & Development Engineering Management
   2. ☐ Design & Development Engineering
   3. ☐ General Corporate Management

   ☐ Other (please describe) ____

For internal use only ____

3. ☐ Your principal job function: (Insert or circle one code only)

07. Design & Development Engineering Management (including R&D - circuits)
12. Design & Development Engineering (including R&D - circuits)
11. Executive & Operating Management (engineering/technical)

01. Corporate & Operating Management (non-engineering)
03. Manufacturing & Production Management (non-engineering)

13. Engineering Services Engineering (evaluation, quality control, reliability, standards, test)
08. Engineering Services Management (evaluation, quality control, reliability, standards, test)
14. Manufacturing & Production Engineering
09. Manufacturing & Production Engineering Management

23. Other (please be specific) ____

4. ☐ What is the PRIMARY end product or service performed at this location? (Insert or circle one code only )

21. Mainframe, Mini/Super Computers
22. PCs, Workstations, Servers
23. Laptops, Notebooks, Hand-helds, and other mobile computers
24. Other Computer/Computer Systems
02. Computer peripherals: disk drives, terminals, printers, plotter
03. CAE/CAD/CAM systems
04. Software manufacturer/developer
05. Computer systems integrator
06. Office & business machines
07. Communications systems & equipment
30. Networks/Software - LAN, WLAN, WAN, etc.,
31. Cellular, Consumer Phones, RF & Microwave Systems
08. Industrial controls, systems, equipment & robotics
09. Electronic instruments, ATE systems, design/test equipment
10. Medical electronic equipment
11. Avionics, marine, space & military electronics
12. Government & military
13. Automotive and other ground vehicles
14. Consumer electronics & appliances
15. ICs & Semiconductors
16. Other components, materials, hardware & supplies
17. Electronic sub-assemblies (boards, modules, hybrids and power supplies)

28. Other (please be specific) ____

5. Do you buy through distributors? ☐ Yes ☐ No
6. Do you design wireless systems or systems that include wireless subsystems or components? ☐ Yes ☐ No
7. Do you design hand held, portable, mobile, nomadic transportable or other products with low power requirements? ☐ Yes ☐ No
8. Do you have or have access to a CD ROM? ☐ Yes ☐ No
9. Do you subscribe or have access to the Internet? ☐ Yes ☐ No
10. Products you specify or authorize purchase of: (Check all codes that apply)

**A Digital ICs**
01 ☐ Microprocessor Chips & Support ICs
02 ☐ 4/8/16 bit uPs/uCs
04 ☐ 32-bit and larger CISC uPs/uCs
08 ☐ RISC uPs/uCs
16 ☐ Digital Signal Processors
32 ☐ Video Controller

**A2**
01 ☐ Video Compression/Decompression
02 ☐ Logic ICs
04 ☐ Storage Controller
08 ☐ Memory - DRAM, SRAM
16 ☐ Memory - ROM, PROM, EPROM, EEPROM, Flash
32 ☐ Memory Modules

**A3**
01 ☐ ICs, other

**B Analog/Mixed-Signal Circuits**
01 ☐ Mixed Signal Devices
02 ☐ Converter ICs & Modules
04 ☐ Linear ICs & Modules
08 ☐ Communications ICs
16 ☐ Audio Processing
32 ☐ Power Semiconductor Devices

**B2**
01 ☐ RF Devices
02 ☐ Hybrid Devices
04 ☐ OP Amps

**C ASICS**
01 ☐ Gate Arrays
02 ☐ FPGA
04 ☐ Programmable Logic Devices (PLD)
08 ☐ Standard Cells
16 ☐ Custom LSI/VLSI
32 ☐ Megacell Functions (CPU cores, etc.)

**C2**
01 ☐ Analog Cells

**D Components**
01 ☐ Capacitors, Resistors, Potentiometers
02 ☐ Display Devices
04 ☐ Relays, Switches, Keypads
08 ☐ Fans
16 ☐ Sensors & Transducers
32 ☐ Microwave Components–Hardware & Crystals

**D2**
01 ☐ Fiber-optic/Optoelectronics
02 ☐ Transformers & Inducters
04 ☐ Fuses
08 ☐ Blowers & Fans
16 ☐ Circuit Breakers

**E Interconnections & Packaging**
01 ☐ Connectors & Sockets
02 ☐ Wire & Cable
04 ☐ Fiber-optic Cable
08 ☐ Enclosures
16 ☐ Materials
32 ☐ Printed Circuits

**E2**
01 ☐ EMI/EMC Components & Materials

**F Power**
01 ☐ Power Supplies
02 ☐ Batteries

**G Test & Measurement**
01 ☐ Logic Analyzers
02 ☐ Development Systems
04 ☐ Oscilloscopes
08 ☐ Other Test Instruments
16 ☐ ATE
32 ☐ Field Test & Service Equipment

**G2**
01 ☐ Communications/Test Equipment
02 ☐ Data Acquisition Hardware/Software
04 ☐ EMI/EMC Test Equipment

**H Computers & Workstations**
01 ☐ Minicomputers
02 ☐ Workstations
04 ☐ Personal Computers

**I Computer Boards**
01 ☐ CPU Boards
02 ☐ Analog I/O & Converter Boards
04 ☐ Memory
08 ☐ Disk/Tape Controllers
16 ☐ Communication/Interface
32 ☐ Graphics & Imaging Boards

**I2**
01 ☐ DSP Boards
02 ☐ Other Special Purpose Boards

**J Communications**
01 ☐ Modems
02 ☐ LAN/WAN Hardware & Software
04 ☐ ISDN Hardware

**K Design Automation/CAE/CAD**
01 ☐ Digital/Analog Simulators
02 ☐ PCB Layout Tools
04 ☐ IC Design Tools
08 ☐ Design Entry Tools
16 ☐ Synthesis Tools
32 ☐ CASE Tools

**K2**
01 ☐ HDL Based Tools
02 ☐ Workstation Based Tools
04 ☐ PC Based Tools
08 ☐ CAE/CAD Software

**L Software**
01 ☐ Software Tools, Dev. Systems and/or High-Level Language
02 ☐ Utility Software Packages & Serv.
04 ☐ Operating Systems
08 ☐ Real-time Operating Systems
16 ☐ Productivity Tools
32 ☐ Compilers/Interpreters

**L2**
01 ☐ Emulators/Debuggers

**M Computer Peripherals**
01 ☐ Disk/Tape Drives
02 ☐ Computer Terminals
04 ☐ Monitors
08 ☐ Graphics Terminals
16 ☐ Printers/Plotters
32 ☐ I/O devices (Mice, keyboards, etc.)

**M2**
01 ☐ PCMCIA Cards
02 ☐ CD-ROM, including WORM & R/W
04 ☐ Multimedia Peripherals

☐ **NONE OF THE ABOVE**

11. Number of employees in your company? ____

12. Please check the publications that you receive personally addressed to you by mail: (check all that apply)

**N**
01 ☐ Computer Design
02 ☐ ECN
04 ☐ EDN
08 ☐ EE Times
16 ☐ Electronic Product News

**O**
01 ☐ Electronic Products
02 ☐ PC Week

☐ **NONE OF THE ABOVE**

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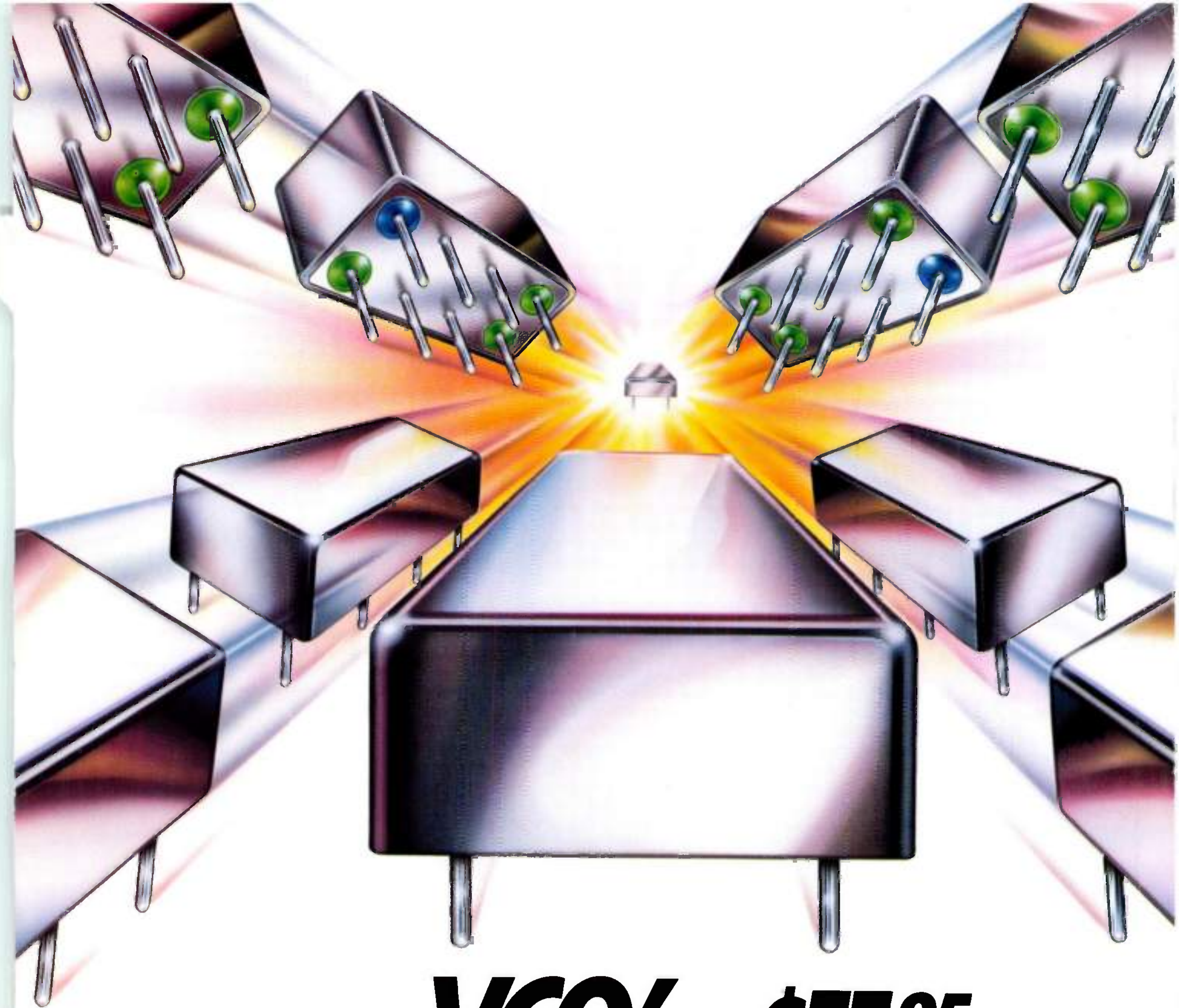

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| | POS-150 | 75-150 | -103 | -23 | 20 | 11.95 |
| | POS-200 | 100-200 | -102 | -24 | 20 | 11.95 |
| | POS-300 | 150-280 | -100 | -30 | 20 | 13.95 |
| | POS-400 | 200-380 | -98 | -28 | 20 | 13.95 |
| | POS-535 | 300-525 | -93 | -26 | 20 | 13.95 |
| | POS-765 | 485-765 | -85 | -21 | 22 | 14.95 |
| | POS-1025 | 685-1025 | -84 | -23 | 22 | 16.95 |
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| NEW | POS-1400 | 975-1400 | -95 | -11 | 30* | 14.95 |
| NEW | POS-2000 | 1370-2000 | -95 | -11 | 30* | 14.95 |

*Max. Current (mA) @ 8V DC.

Notes: Tuning voltage 1 to 16V required to cover freq. range 1 to 20V for POS-1060 to -2000. Models POS-50 to -1025 have 3dB modulation bandwidth, 100kHz typ. Models POS-1060 to -2000 have 3dB modulation bandwidth, 1MHz typ. Operating temperature range: -55°C to +85°C.

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