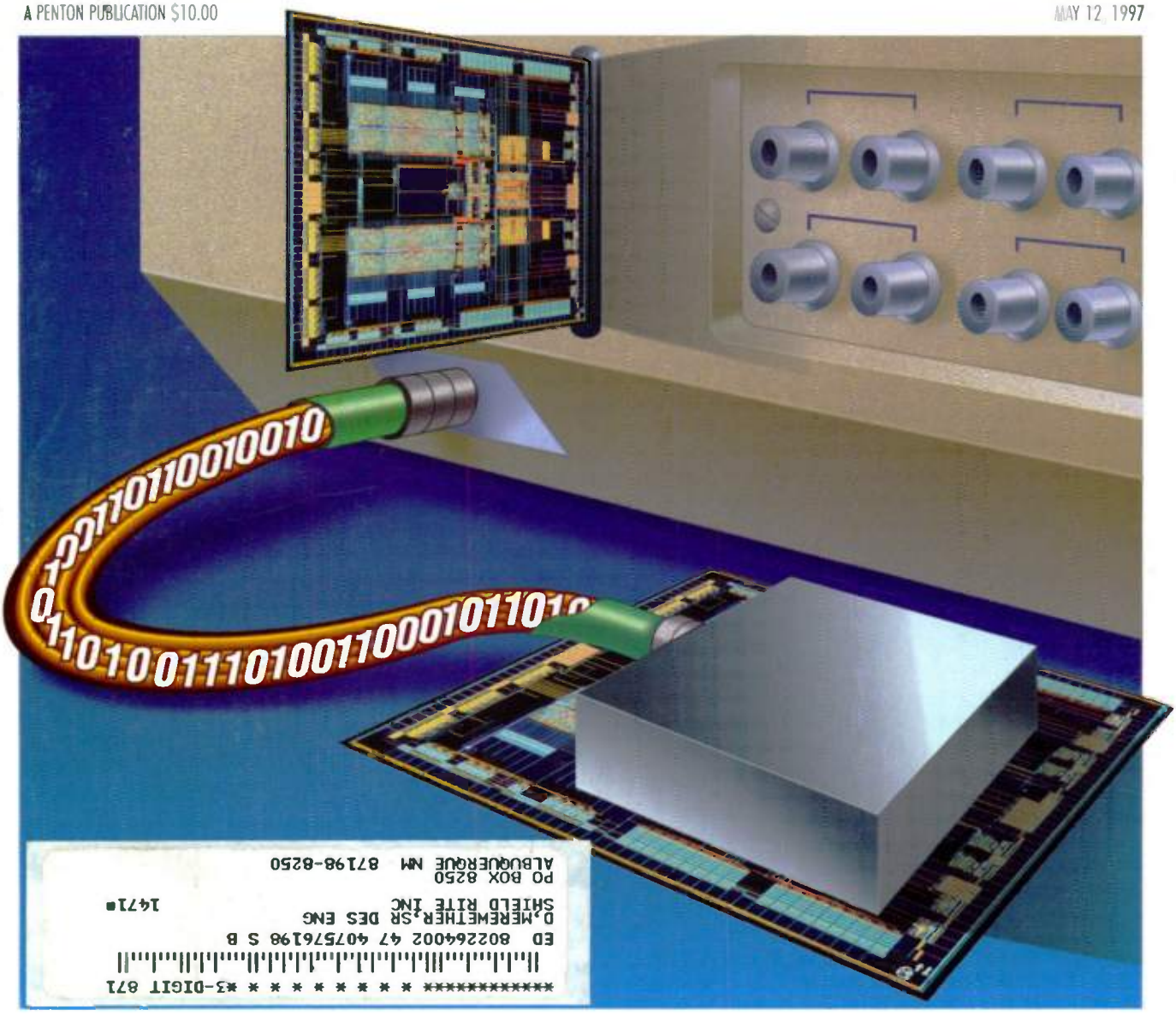
ELECTRONIC DESIGN

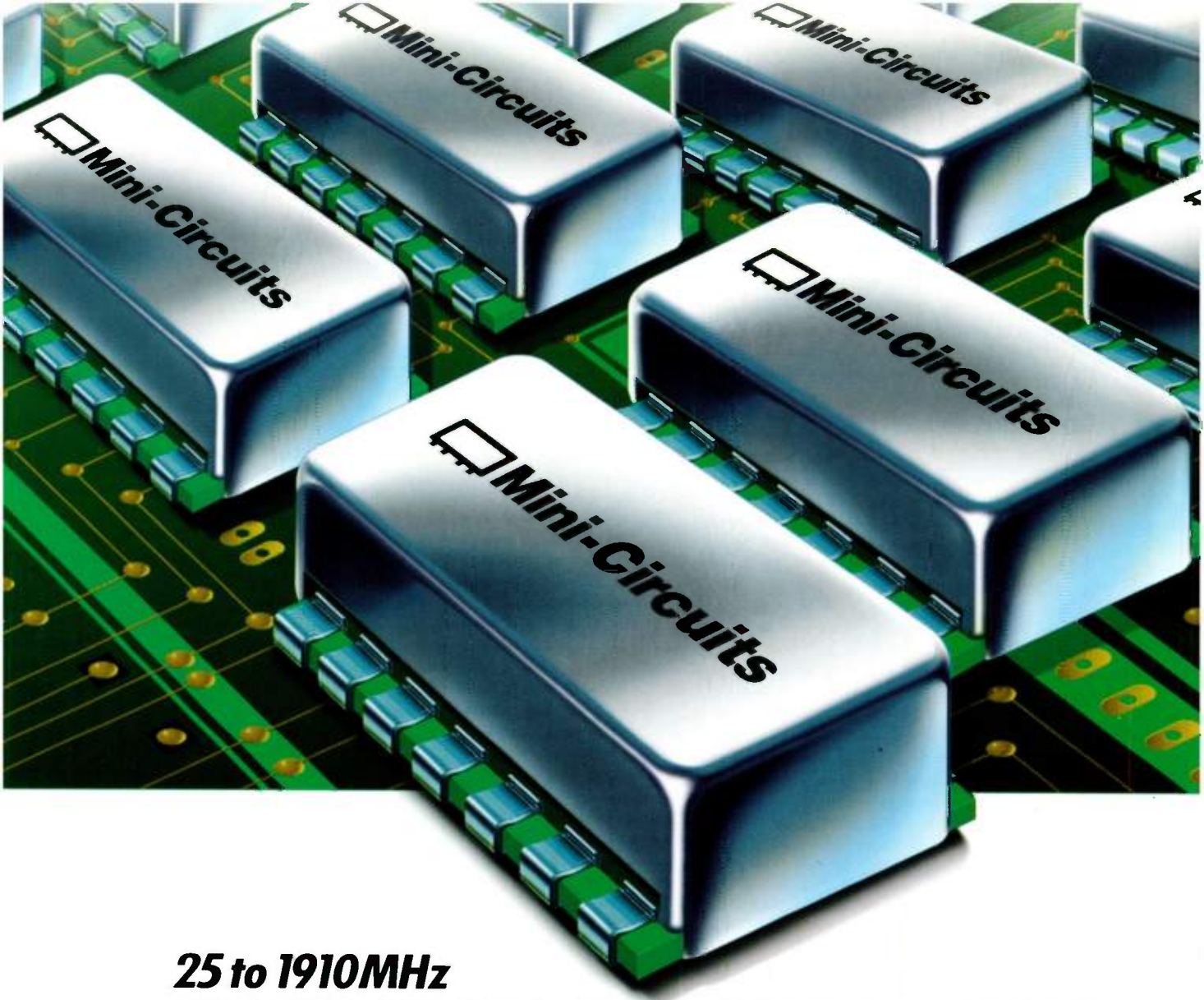
FOR ENGINEERS AND ENGINEERING MANAGERS-WORLDWIDE

A PENTON PUBLICATION $10.00

MAY 12, 1997



Fibre Channel Transceiver Ups Bandwidth, Maintains Design Ease p. 69



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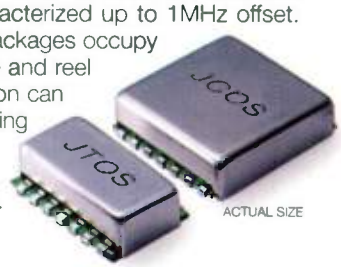

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JCOS-820BLN	807-832	-112	-24	14V	25 (@10V)	49.95
JCOS-1100LN	1079-1114	-110	-15	20V	25 (@8V)	49.95

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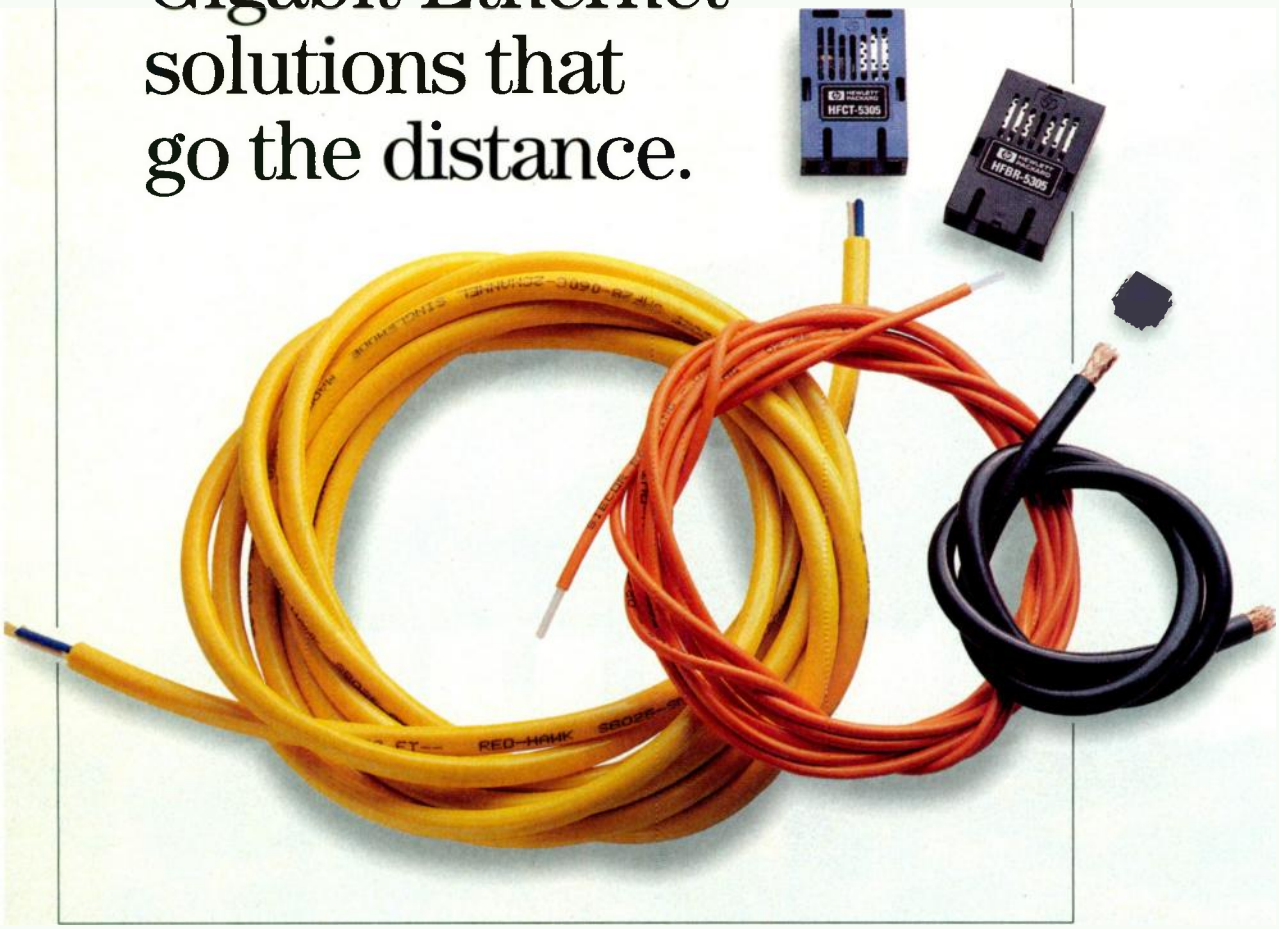

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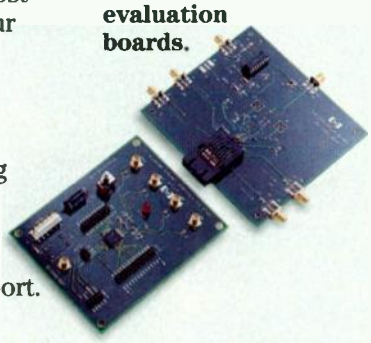

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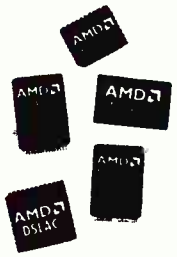

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ERA-3	DC-3000	20.8	12.1	3.8	23.0	35	2.10
ERA-3SM	DC-3000	20.2	11.5	3.8	23.0	35	2.15
ERA-4	DC-4000	13.5	▲17.0	5.5	▲32.5	65	4.15
ERA-4SM	DC-4000	13.5	▲16.8	5.2	▲33.0	65	4.20
ERA-5	DC-4000	18.8	▲18.4	4.5	▲33.0	65	4.15
ERA-5SM	DC-4000	18.5	▲18.4	4.3	▲32.5	65	4.20
ERA-6	DC-4000	11.3	▲18.5	8.4	▲36.5	70	4.15
ERA-6SM	DC-4000	11.3	▲17.9	8.4	▲36.0	70	4.20

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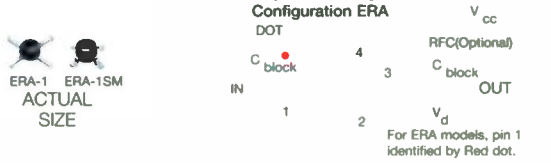
120x60	.002, .047, .068, .1 µf



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ELECTRONIC DESIGN

May 12, 1997 Volume 45, Number 10

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May 12, 1997 Volume 45, Number 10

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TEST & MEASUREMENT

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International Symposium on VSLI Technology, Systems, and Applications, June 3-5. Grand Hyatt Hotel, Taiwan, China. Contact T. P. Ma, Dept. of Electrical Engineering, Yale University, 15 Prospect St., New Haven, CT 06520-8284; (203) 432-4211; fax (203) 432-7769.

Mixed Signal Test Workshop; June 3-6. Seattle, Washington. Contact M. Soma; (206) 685-3810; e-mail: soma@ee.washington.edu.

American Control Conference (ACC '97), June 4-6. Albuquerque Convention Center, Albuquerque, NM. Contact Steven Yurkovich, Department of Electronics & Engineering, Ohio State University, 2015 Neil Ave., Columbus, OH 43210; (614) 292-2586; fax (614) 292-7596; e-mail: s.yurkovich@i.ee.org.

IEEE International Conference on Communications (ICC 97), June 8-12. Montreal, Canada. Contact Celia Desmond, Stentor, Floor 6b, 33 City Center Dr., Mississauga, Ontario L5B 2N5, Canada; (905) 615-6507; fax (905) 615-8421; e-mail: celia.desmond@tc.resonet.com.

Microwave Symposium (MTT 97), June 8-13. Convention Center, Denver, Colorado. Contact John Dunn, Dept. of Electrical & Computer Engineering, University of Colorado, Campus Box 425, Boulder, Colorado 80309; (303) 492-5920; fax (303) 492-5323; e-mail: dunn@boulder.colorado.edu.

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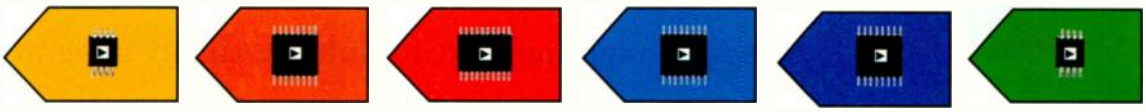

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Interface	Serial	Serial	Serial	Parallel	Parallel	Serial
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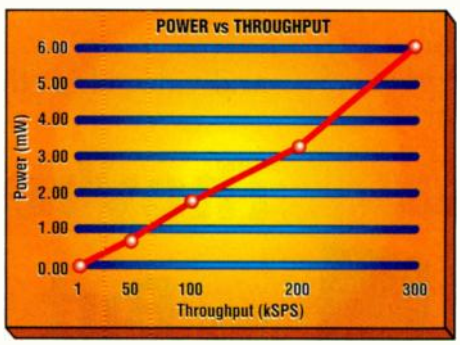

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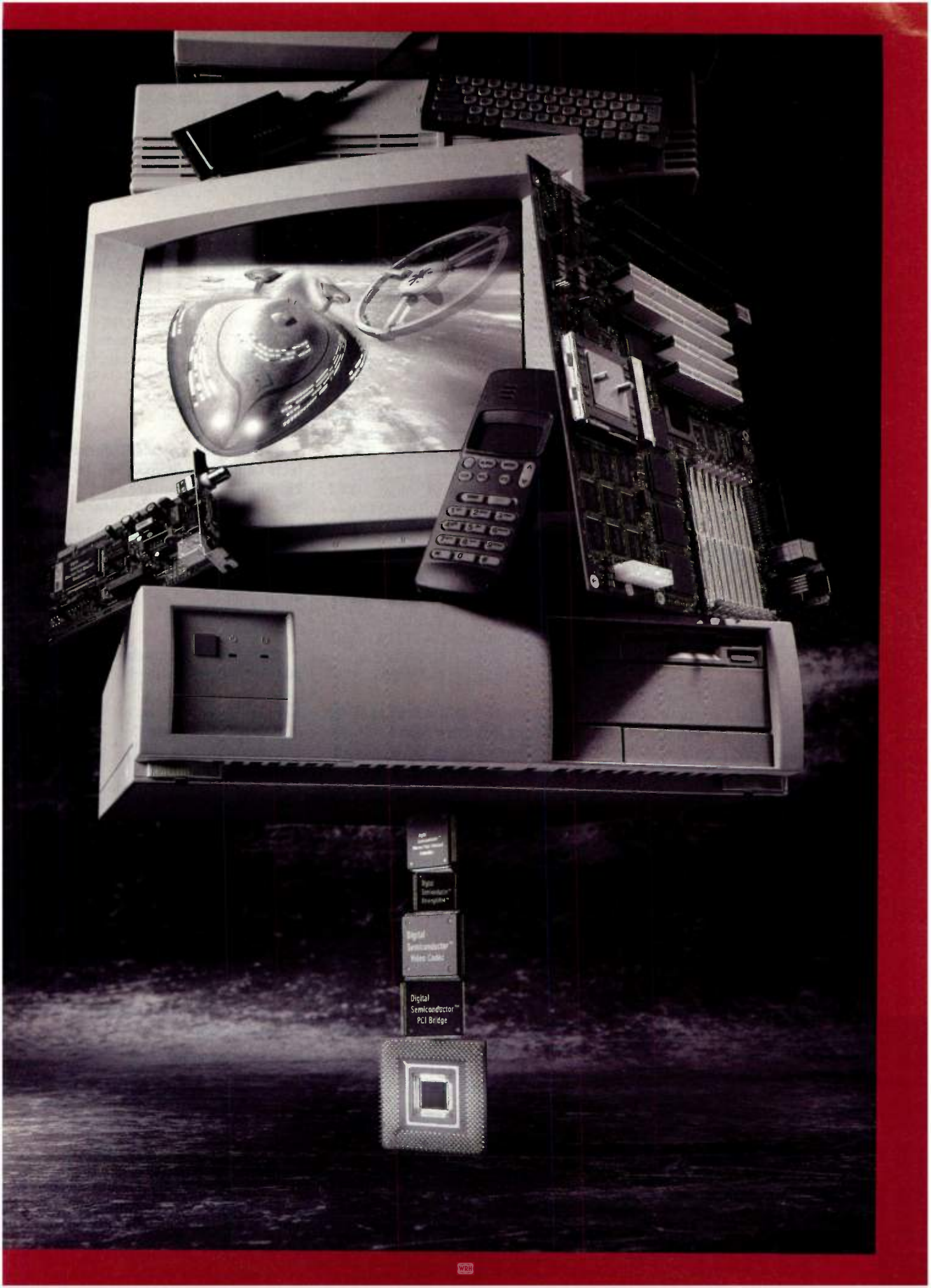
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JUNE

IEEE International Symposium on Circuits & Systems (ISCAS 97), June 9-12. Hong Kong Convention & Exhibition Centre, Hong Kong. Contact ISCAS '97 Secretariat, Department of Electrical & Electronic Engineering, University of Hong Kong, Pokfalam Rd., Hong Kong; (852) 28592710; fax (852) 25598738; e-mail: iscas97@hkueee.hku.hk.

34th Design Automation Conference (DAC '97), June 9-13. Anaheim Convention Center, Anaheim, CA. Contact MP Associates Inc., 5305 Spine Rd., Suite A, Boulder, CO 80301; (303) 530-4333; fax (303) 530-4334.

ASIA TELECOM '97 (TIA), June 9-14. Singapore, Asia. Contact (703) 907-7736.

IEEE International Conference on Consumer Electronics (ICCE), June 11-13. The Westin Hotel O'Hare, Rosemont, IL. Contact Diane D. Williams, 67 Raspberry Patch Dr., Rochester, NY 14612-2868; (716) 392-3862; fax (716) 392-4397.

Virginia Tech/MPRG Symposium on Wireless Personal Communications, June 11-13. Campus of Virginia Tech, Blacksburg, VA. Contact MPRG Conference Coordinator Jenny Frank (757) 686-3765, or Jack Lilly, (540) 231-4849.

International Solid-State Sensors and Actuators Conference (Transducers 97), June 15-19. Hyatt Regency Hotel, Chicago, IL. Contact Kensal D. Wise, 1246 EECS Building, University of Michigan, 1301 Beal Ave., Ann Arbor, MI 48109-2122; (313) 764-3346; fax (313) 747-1781.

IEEE Digital Cross Connect Systems Workshop VII (DCS 97), June 16-19. Banff Park Lodge, Banff, Alberta, Canada. Contact James H. Simester, Lucent Technologies, P.O. Box 3030, Room 4J-526, 101 Crawfords Corner Rd., Holmdel, NJ 07733-3030; (908) 949-7336; fax (908) 949-2724; e-mail: sims@bostare.ho.att.com.

Third Conference on Object-Oriented Technologies & Systems (Coots 97), June 16-20. Marriott Hotel, Portland, OR. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, California 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

IEEE International Conference on Systems, Man, and Cybernetics, June 16-20. Hyatt Orlando, Orlando, FL. Contact James M. Tien, Chair, DSES Department, Rensselaer Polytechnic Institute, Troy, NY 12180-3590; (518) 276-6486; fax (518) 276-8227; e-mail: tienj@rpi.edu.

IEEE/ASME International Conference on Advanced Intelligence Mechatronics, June 16-20. Contact Hideki Hashimoto, Institute of Industrial Science, University of Tokyo, 7-22-1, Roppongi, Minato-ku, Tokyo 100, Japan; (81) 3 3402 6231 ext. 2359; fax (81) 3 3423 1484.

IEEE Sixth International Fuzzy Systems Conference, June 20-25. Barcelona, Spain. Contact Ramon Lopez De Mantaras, IIIA-CSIC Campus U.A.B., 08193 Cerdanyola del Valles, Spain; (34) 3 580 95 70.

IEEE Power Electronics Specialist Conference (PESC 97), June 22-27. Regal Riverfront Hotel, St. Louis, MO. Contact Philip T. Krein, University of Illinois, 1406 W. Green St., Urbana, IL 61801; (217) 333-4732; e-mail: krein@uipesl.ece.uiuc.edu.

IEEE International Symposium on Information Theory, June 29-July 4. Ulm, Germany. Contact Han Vinck, Institute of Experimental Mathematics, University of Essen, Ellernstr. 29, 45326 Essen, Germany; (49) 201 3206458; fax (49) 201 3206425.

JULY

Fifth USENIX TCL/TK Workshop, July 14-17. Tremont House Hotel, Boston Massachusetts. Contact USENIX Conference Office, 22672 Lambert Street, Suite 613, Lake Forest, California 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

IEEE Power Engineering Society Summer Meeting, July 20-25. Intercontinental Hotel, Berlin, Germany. Contact Executive Office, IEEE Power Engineering Society, P.O. Box 1331, Piscataway, New Jersey 08855-1331; (908) 562-3864; fax (908) 981-1769.

IEEE Signal Processing Workshop on Higher Order Statistics, July 21-23. Banff Centre for Conferences, Banff, Alberta, Canada. Contact Keh-Shin Lii, Department of Statistics, University of California, Riverside, 900 University Ave., Riverside, California 92521; (909) 787-3836; fax (909) 787-3286; e-mail: ksl@ucrstat.ucr.edu.

IEEE Nuclear & Space Radiation Effects Conference (NSREC '97), July 21-25. Snowmass Conference Center, Snowmass, Colorado. Contact Dennis B. Brown, Naval Research Laboratory, Code 6612, Washington, DC 20375; (202) 767-5453; fax (202) 404-8076; e-mail: dbbrown@ccfnrl.nvy.mil.

AUGUST

40th Midwest Symposium on Circuits and Systems, August 2-6. Hyatt Regency Hotel, Sacramento, California. Contact Sharon Baumgartner, Dept. of E & CE, University of California, Davis, California 95616; (916) 754-6216; fax (916) 752-8428; e-mail:mwscas97@ece.ucdavis.edu.

IEEE International Geoscience & Remote Sensing Symposium (IGARSS '97), Aug. 4-8. Singapore International Convention Exhibition Centre, Suntec City, Singapore. Contact Kwoh Leong Keong, CRISP, National University of Singapore, Faculty of Science, Lower Kent Ridge Rd., S 119260 Singapore; (65) 7727838.

Memory Technology, Design, & Test Workshop, Aug. 11-12. San Jose, California. Contact F. Lombardi; (409) 845-5464; e-mail: lombardi@cs.tamu.edu.

USENIX Windows/NT Workshop, Aug. 11-13. Sheraton Hotel, Seattle, WA. Contact USENIX Conference Office, 22672 Lambert St., Suite 613. Lake Forest, California 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org.

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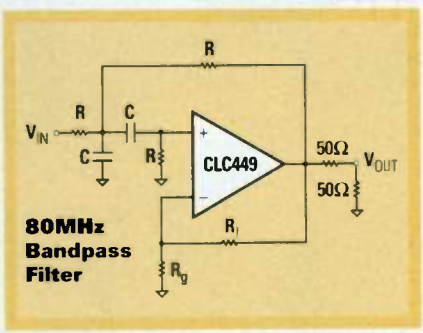
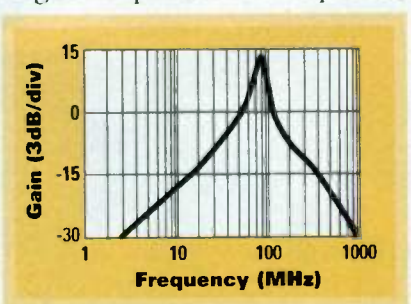
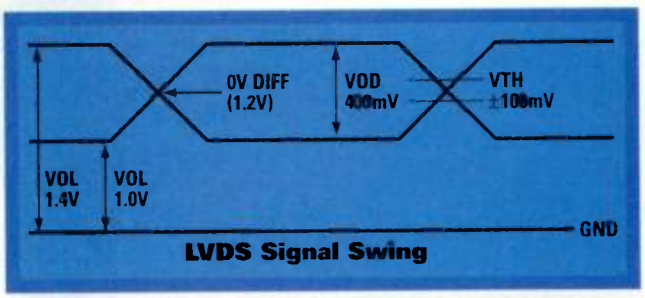




With ample bandwidth for high-speed active filters, for example, our new CLC449 wideband current feedback amplifier delivers the signal processing performance required in today's Mil/Aero applications—along with excellent differential gain and phase values, wide dy-namic range, and a very low power consumption rate.

And our new Low Voltage Differential Signaling, or LVDS, quad line driver-receiver devices offer a data-link solution for Mil/Aero applications such as target tracking, video, and other point-to-point (<10m) data transmissions where both high speed and very low EMI are essential. Pin-compatible with lower-performance LS, FAST, and CMOS RS-422 components, National's QML LVDS driver-receivers deliver bandwidths up to 77.7MHz (155.5Mbps), faster switching, and low noise at supply currents as low as 25mA (driver) and 11mA (receiver).

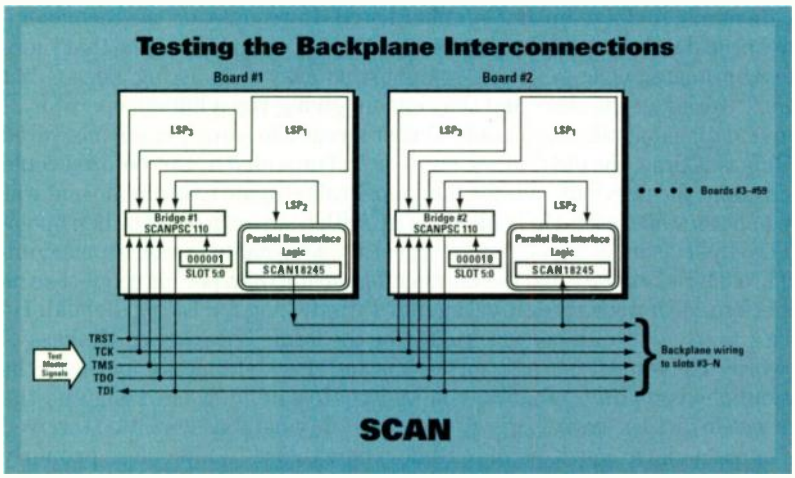


SCAN: BECAUSE THERE'S NO ALTERNATIVE TO RELIABILITY

To ensure that today's Mil/Aero systems can be tested quickly and economically, National helped create the IEEE 1149.1 Standard for Boundary SCAN Test. Boundary SCAN addresses the physical access issues raised by today's dense, complex circuit board designs

AT NATIONAL IT'S

and advanced packaging techniques. So the SCAN test strategy improves system fault coverage and improves test throughput, thus cutting test and development costs and improving time to market. National offers a wide range of SCAN products for Mil/Aero applications in both package and cell-based custom options.



Each partner brings its unique core competencies to CBU, offering Mil/Aero customers a complete range of design services, deep submicron development technologies, and advanced manufacturing services for producing highly-integrated system-on-a-chip custom CMOS solutions. National can accept designs at virtually any stage. But from netlist hand-off to prototypes, the CBU's mission is always the same: Provide "first-time" working silicon in less than 12 weeks.

ABOUT INNOVATION.

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In today's Mil/Aero environment, meeting spec means more than simply upgrading. It means improving performance while reducing scale, and reaching the market faster than ever. And that takes higher levels of integration, and truly forward thinking about design, development, and delivery strategies.

For all of the above, there is no better partner than National. No one with our expertise in mixed-signal integrated system design, process technology, or tools. And no one with our commitment to creating customized solutions to both technical and development problems. If you're looking for the next level in Mil/Aero system design, not just the next upgrade path, look to National.

CBU: FILLING THE GAP IN CUSTOMIZED ASIC DESIGN

To fill the technology gap in high-density semi-custom ASICs and answer the unique design service and support requirements of the Mil/Aero marketplace, we've formed the Customization Business Unit, or CBU. A partnership with Cadence Spectrum Design Services of San Jose, California, and Aspec Technology of Sunnyvale, California, the CBU operates as a single business unit headed by National.

CBU Business Methodology

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WRH

EDITORIAL

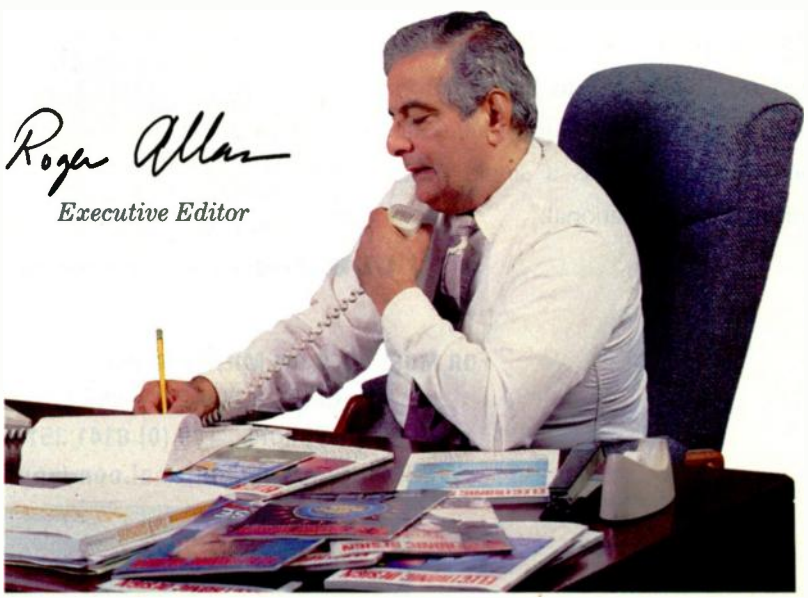
Technology's Weak Link

The other day, I dialed an out-of-town "information" operator to obtain the telephone number of a travel agency. Besides having to spell out the very simple agency name for her (which she did not know how to), she could not, for the life of me, find a telephone number listed, I presume, on the technologically advanced database that she was using. (Some of you might argue that there are many automated voice-response systems that ask "what listing please," but these don't work half the time, and they end up giving you a human operator). I hung up and dialed again, and I could almost swear the same person answered again. Only this time, she did find the number and provided it. But before I could complain about the previous call, she hung up. I called again to complain and was provided another operator. He hooked me up with a supervisor who then apologized. The supervisor asked me for the travel agency's name to look up the number and I told him I already had the number. I gave it to him per his request so he could check to see if it was the travel agency I was asking for. Lo and behold! He came back to say that number was really for the local "Nicaraguan Embassy." Not to worry. He asked me to stay on the line and checked that number with the local telephone company. What do you know? He said he was wrong and the number was in fact the travel agency's after all. "My database must be screwed up," he explained. Or was it he didn't know how to use it, much less properly spell the travel agency's name? Probably both.

So much for technology! It's only as good as the person behind it. Judging from my experiences and I'm sure many of yours, the quality of service provided by human telephone operators leaves a lot to be desired. Even the best databases are useless if the operator can't spell. It's times like these that make me want to say "to heck with technology!" I'm sure I can get better results by using a regular telephone book where I can look up listings myself without having to deal with the failings of technology and its human link.

This situation is not unique to telephone service. It also extends to the office,, where advanced applications software packages like Word, dBase, PowerPoint, and Excel are underutilized for lack of proper training and, in some cases, mistraining by those who weren't properly trained in the first place. It points to a real problem in the kinds of support and service personnel we have helping us with the latest technological tools. The bottom line is "are we really ready for technology?" Proficiency in reading, writing, and spelling are being taken for granted. Is this the foundation that will carry us into the 21st Century with all the advanced technological tools we now possess? I shudder to think.

rallan@class.org



Roger Allan

Executive Editor

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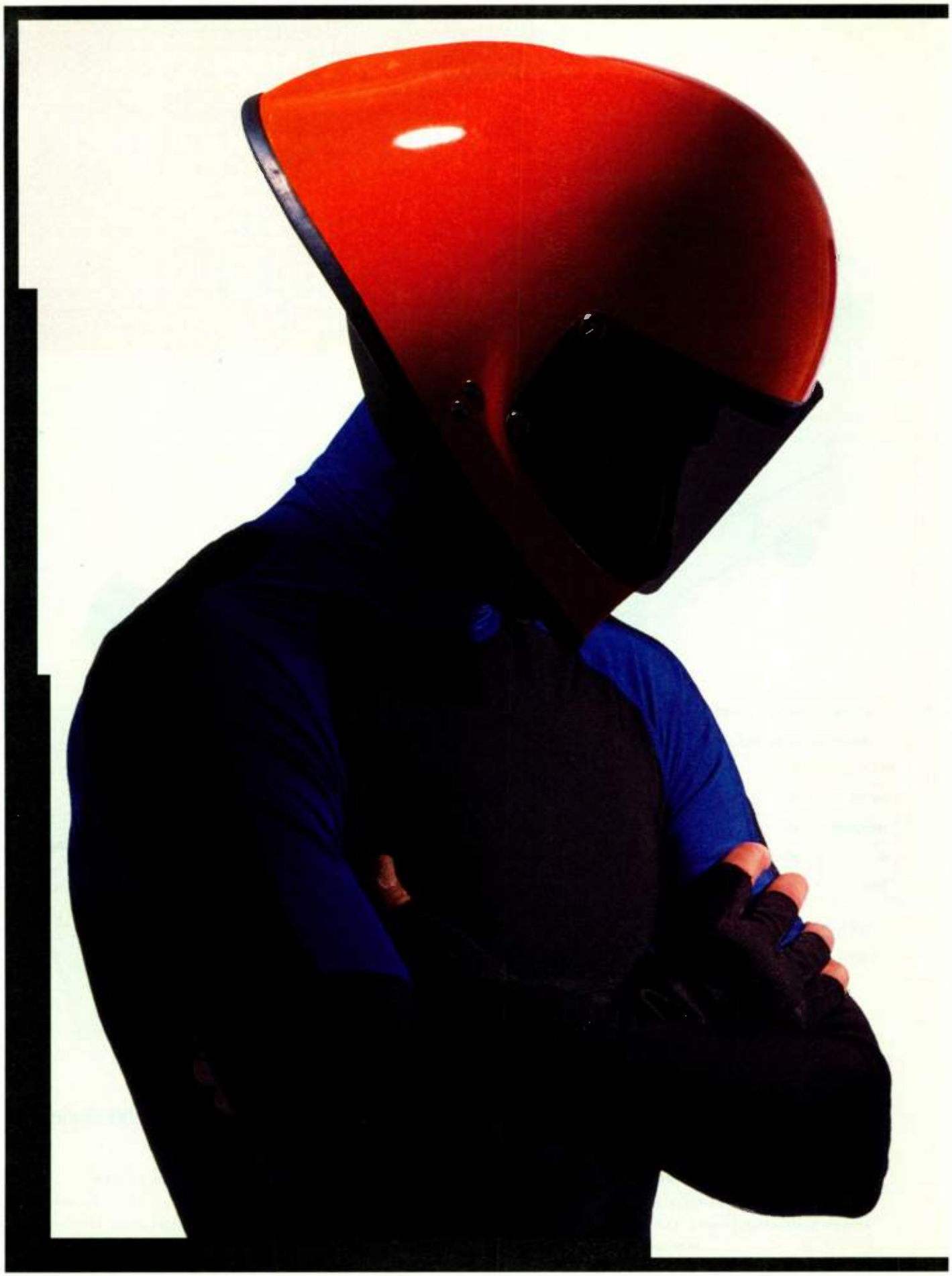

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SYNCHRONOUS DRAM MODULES

Size	Config.	Volt.	Speed	Refresh
32MB	4M x 64	3.3V	66/83/100MHz	4k
32MB	4M x 72	3.3V	66/83/100MHz	4k
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READER SERVICE 128

"Baaaaaaaaaaaa!"

From BGA to TSSO and the dozens in between, keeping track of your myriad packaging options—and their acronyms—is getting to be a bit of a feat in itself. Add to that the task of evaluating each new option in the light of an upcoming design, and its enough to keep all but the bravest packaging wannabes at bay. Look at the list. You have old faithfuls like DIP, QFP, PQFP, SO, and PLCC being upstaged by the likes of BGA, PBGA, MBGA, SBGA, FC BGA, FC, CBGA, FCPBGA, SON, TSON, MCM, MCP, and DCA, to mention just a few. The plethora of acronyms alone tells us something big is happening in packaging. Real big. Big enough to make even Dolly the sheep go "Baaaaaaaaaaaa."

But it wasn't always this way. Time was when packaging was more of an afterthought, reserved for those more interested in mechanical issues than true "Electronic Engineering." Suddenly, the whole landscape changed. Higher integration brought higher levels of dissipated power within a given-size semiconductor package. Then the size of the package began to shrink as portability became the issue. As packaging density increased, functions per square inch took priority. To handle the higher levels of functionality, processing speeds jumped up, opening the gate not only to greater power dissipation and its associated heat problems, but also to transmission-line effects such as crosstalk and reflections along pathways that were once regarded as simply a means of getting electrons from point A to point B. Reducing these effects requires a shortening of the distance between system components, thereby increasing packaging density yet again in a never-ending dance.

PATRICK MANNION
COMPONENTS & PACKAGING

So, what's the overworked and underpaid design engineer to do? For those who've kept their heads out of the sand, the alphabet soup of packaging options could be looked on optimistically as a sign that their plight is not being ignored by the packaging gurus. Of the many options they have proffered, none have garnered as much interest in such a short time as the general category of chip-scale packages (CSPs). Widely accepted as being between 1 and 1.2 times the size of the die perimeter (some rebellious, fringe lunatics go as far as 1.5x), CSPs come with many advantages, including a space savings of up to 80%.

However, there are a number of gotchas. While routing of a low number of I/Os is relatively straightforward, when the number of I/Os starts to exceed 200, routing needs to be done on expensive multilayer boards with tight 2- or 3-mil line spacings. Heat dissipation also is a problem. CSPs can handle up to 2 W, but anything beyond that requires some sort of bulky external heat-sink option. Shipping and handling also remains problematic. The level of placement sensitivity and accuracy CSPs require cannot be met by current pick-and-place machines without some level of modification. Though one easily adaptable method of shipping CSPs is in GelPaks, in both 2- and 4-.. sizes.

While solutions to the above are imm ent, testing is proving to be the CSP's Achilles' heel. From the die to the package to the board, ensuring design and connection integrity is fraught with problems. Thermo-mechanical wear of solder joints, particularly between the package and the board, is the main cause of failure. At issue is a lack of data on solder-joint reliability and the very limited data on cycles-to-failure of assembled packages. The available data often does not even apply to your particular environmental and cycling conditions. To help with this problem, the Jet Propulsion Laboratory (JPL) in California is organizing a micro-type BGA consortium to deal with these issues. Already responsible for the building and testing of almost 400 test vehicles for BGAs, JPL hopes to directly apply what it has learned to studying the interplay of package type, I/O counts, PWB materials, and manufacturing variables on quality and reliability of assembled CSPs. For more information on the micro-type BGA consortium, contact Reza Ghaffarian at (818) 354-2059. By the way, can you guess which two packaging acronyms I made up in the first paragraph? *pcmann@ibm.net.*

We've Got Your Busses Covered

Direct-to-Digital Temperature Measurement with a New Interface

The Dallas Semiconductor family of 1-Wire™ and 3-wire temperature sensors has a new member: the 2-wire DS1621 Digital Thermometer and Thermostat. With this popular interface, the industry's most accurate digital thermometer can now serve a host of new applications, including PCs, microprocessors, and hand-held PDAs.

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Like our other temperature sensors, the DS1621 Digital Thermometer and Thermostat converts temperature directly to a 9-bit digital number in less than one second, eliminating the need for an A/D converter. The DS1621 can also function as a standalone thermostat with a user-definable and changeable set point.

And that's not all.

- The DS1621 is the **most accurate** digital temperature sensor in the industry: ±0.5°C over the commercial range and ±1.0°C over the industrial range.
- The DS1621 is the only digital temperature sensor that can achieve **13-bit (or 0.03125°C) resolution**, important for applications that monitor fast rates of temperature change.
- The DS1621 is the only digital temperature sensor to **store the temperature limits in EEPROM**, alleviating the need to power up to default limits and then re-set the device.
- The DS1621 features a **wide power supply range**—from 2.7V to 5.5V—in a single device.
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White LED Developed Through Luminescence Conversion

Up to now, the only way to create white light was by combining three different diodes in a single case called a tripled. That's no longer the case: Scientists at the Fraunhofer Institut fuer Angewandte Festkoerperphysik (Fraunhofer Institute for Applied Solid State Physics), Freiburg, Germany, have developed a white light-emitting diode, and it just recently left the laboratory. Siemens AG, Munich, Germany will manufacture these devices and plans to offer the first commercially available samples of these white LEDs by early 1998.

The idea comes from the generation of white light through luminescence conversion. Blue-emitting diodes based on gallium nitride were combined with luminescent dyes, creating bright light emission at changed wavelengths. The resulting mixture of colors is visible as white light. These "LUCO LEDs" (luminescence-conversion LEDs) allow light emission in a wide color range depending on the emission of the dyes used. Arbitrary color tones of the spectrum, such as turquoise, purple, or magenta, are also possible.

The scientists use a LED chip bonded to a reflector cup that's embedded in an epoxy resin matrix containing organic dye molecules. It's encapsulated by using standard LED technology in transparent epoxy resin. When excited by the blue LED, the organic dye emits green light at a wavelength lambda(max) of 520 nm. Yellow- and red-emitting LEDs were realized in the same manner using perylene-based Lumogene F dyes from BASF of Ludwigshafen, Germany. The electroluminescence (EL) spectrum of the blue LED strongly overlaps with the absorption spectrum of the green-emitting dye.

In the same way, white-emitting LUCO LEDs have been made by adding green and red emitting dyes to the epoxy resin. The corresponding C.I.E. chromaticity coordinates are close to the equal-energy point where x = y = 1/3.

The principle of luminescence down-conversion of blue-emitting LEDs isn't restricted to organic luminescent materials, though, because the wide field of inorganic phosphor materials offers interesting solutions of LUCO LED applications. For example, the physicists at the Fraunhofer Institute have created a white-emitting LUCO LED using an ordinary blue chip as a primary light source and a yellow-emitting converter. The whole principle is the subject of two patent applications. *AV*

BGA Design And Production Get A Double Boost

Despite stringent reliability requirements and overall difficulty of the substrate manufacturing process, BGAs are increasingly being chosen as the optimum solution for high-performance, highly integrated ICs. While the market currently stands at around 150 million units for 1997, Dataquest forecasts that this will reach 2.4 billion by 1999. Recognizing the potential, two companies, working independently, have announced plans that should go a long way toward realizing these forecasts. Assembly Test Services (STATS) has announced the opening of a design center that will help customers determine the packaging specifications for complex integrated circuits requiring BGA packages, while ProLinx Labs announced an agreement with Unicap Electronics Industrial Corp. to form a $42 million facility focused on producing semiconductor BGA packages based on ProLinx's technologies.

The STATS design center, located at the company's facility in San Jose, Calif., will assist customers in designing the BGA packaging substrate, identifying power and ground requirements, determining input/output assignments for each pin, and conducting the thermal/electrical simulation work for the chips. The goal is to help the customer design the most appropriate package for their specific device.

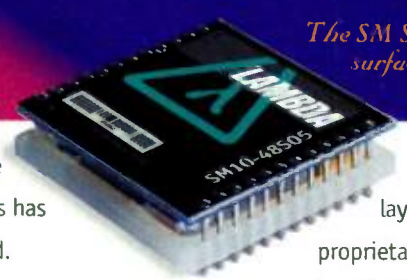
STATS offers the over-molded and thermally enhanced BGAs in package sizes of 27 by 27 mm and 35 by 35 mm on each side. A variety of packages for diverse, high-pin-count integrated circuits also are offered. These include QFPs, (64 to 240 leads), thermally enhanced QFPs, TQFPs (32 to 208 leads), PLCCs (44, 68, and 84 leads), and 225- to 388-lead BGAs.

The proposed facility will help alleviate the difficulties encountered in obtaining laminate substrates. Unicap, one of the five largest pc-board companies in Taiwan, will provide manufacturing technology and know-how, while ProLinx will provide the engineering expertise and support to implement the Micro-filled Via (MfVia) process used to produce ProLinx's ViperBGA substrate. Contact STATS Packaging Design Center at (408) 526-2070, or Alex Chenok Jr., ProLinx Labs, at (408) 227-0707 ext. 110. *PM*

PCI Hot-Plug Spec Enables Hot Replace, Upgrade, And Expansion

There's a new PCI specification in the works. What a surprise. The twist on this one, though, is that it's an off-shoot of the existing desktop PCI standard. It's called the PCI Hot-Plug Specification, and it enables the insertion and removal of PCI adapter cards without having to power down the system. This capability allows for several implementations, including hot replace (replacing adapter cards in running systems); hot upgrade (upgrading existing adapter cards with new versions of cards and drivers); and hot expansion (adding previously uninstalled cards and associated software drivers to a system). The place where these capabilities are most required is in mission-critical server applications, where any system down time could result in a significant loss. The Hot-Plug specification is now available for review on the PCI Special Interest Group (SIG)

HAVEN'T YOU BEEN STUCK WITH THESE PINS LONG ENOUGH?



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(We'd be happy to go into more detail, but then it wouldn't be proprietary anymore.)

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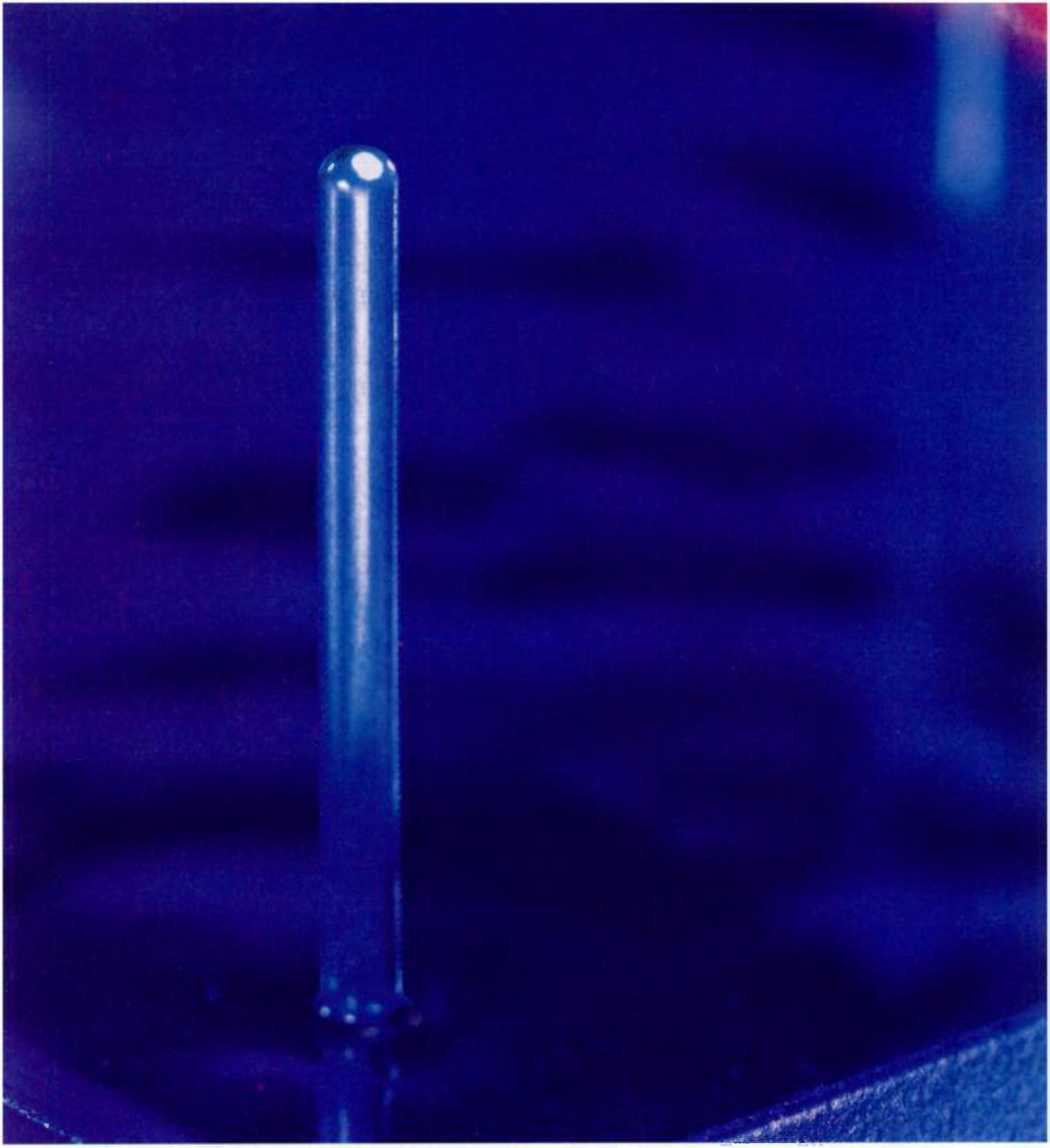

And we're not talking about a few high-priced, custom SM converters for some obscure application. We're talking about a line that'll be 56 models long. Ranging from 5 watts to 30 watts. With a profile of .4 of an inch or less to minimize board pitch.

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Or you can get stuck with something else.

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Internet site at http://www.pcisig.com. The burden of the specification implementation has been placed on the system vendor rather than the adapter-card manufacturer. As a result, existing PCI cards should operate properly in a Hot-Plug backplane. *RN*

Alliance Forms To Promote Small PCI And Advance The Standard

Small PCI (SPCI) is an alternative implementation of the PCI local bus for use in embedded applications where space is at a premium. To help promote SPCI and advance the standard, the SPCI Alliance is currently being set up. The goals of the alliance include making the standard and related documents more widely available; forming committees to extend, improve, and clarify the SPCI specification; promoting SPCI; and developing an SPCI newsletter and Internet site. SPCI employs the form factor of PC Cards, but is electrically similar to standard desktop PCI. It's suited for mobile systems, handheld terminals, set-top boxes, and communications switch boxes. SPCI offers a software-compatible upgrade to such buses as STD, PC/104, and PCMCIA. It also can be used as an upgrade within an existing system. The SPCI Alliance is being formed by Conference ConCepts Inc., Poway, Calif. They can be reached at (619) 673-1372. For technical information regarding SPCI, contact Lance Leventhal at (619) 756-3327. *RN*

Miniature, Low-Cost Optical Interface Receives Approval

Designed as a miniature, low-cost alternative to duplex multimode and single-mode SC connectors, an optical interconnect, tentatively named "Galaxy," uses a V-groove alignment technique and an RJ45-comparable plug-and-socket configuration. The connector thus eliminates the need for ferrules, alignment sleeves, and corresponding couplings while maintaining optical, mechanical, and environmental performance. In addition, the connector fully complies with ANSI/TIA/EIA 568A and ISO 11801 premises cabling and corresponding component standards.

Proposed by the 3M Telecom Systems Div., the interface received final approval at the Feb. '97 Fibre Channel Association ASC-X3t11 Technical Committee meeting. The interface is 50% smaller than duplex SC connectors, has a PCI-mezzanine-compatible height, and requires no precision components. The V-groove self-alignment and three-piece snap-in assembly allow the connector to be installed in under two minutes in the field. Fiber bow maintains optical contact.

Specifications to date include an attenuation of 0.75 dB (max), a return loss of -20 dB for multimode and -26 dB for single mode, and a coupling strength of up to 40 newtons. The connector is currently in beta testing and is due out in the third quarter of this year. For further information, contact 3M at (512) 984-1800. *PM*

Electronic Cleaning Innovator Establishes Presence In U.S.

Zestron Corp., a leader in the European market for electronic component and board cleaning products and services for more than 20 years, has now established a major presence in McLean, Va., to serve its expanding customer base and develop new markets. A subsidiary of Dr. O.K. Wack Chemie GmBH, the company provides a full range of cleaning agents and services, including cleaning materials and turnkey process development.

According to Dr. Stefan Koschmieder, vice president of Zestron, the company's strength lies in its ability to provide a complete solution to cleaning problems by offering fully integrated services. These include materials selection, project engineering, installation, and start-up of new cleaning processes. "By outsourcing these functions, our customers save resources which would otherwise go toward developing in-house expertise" he said.

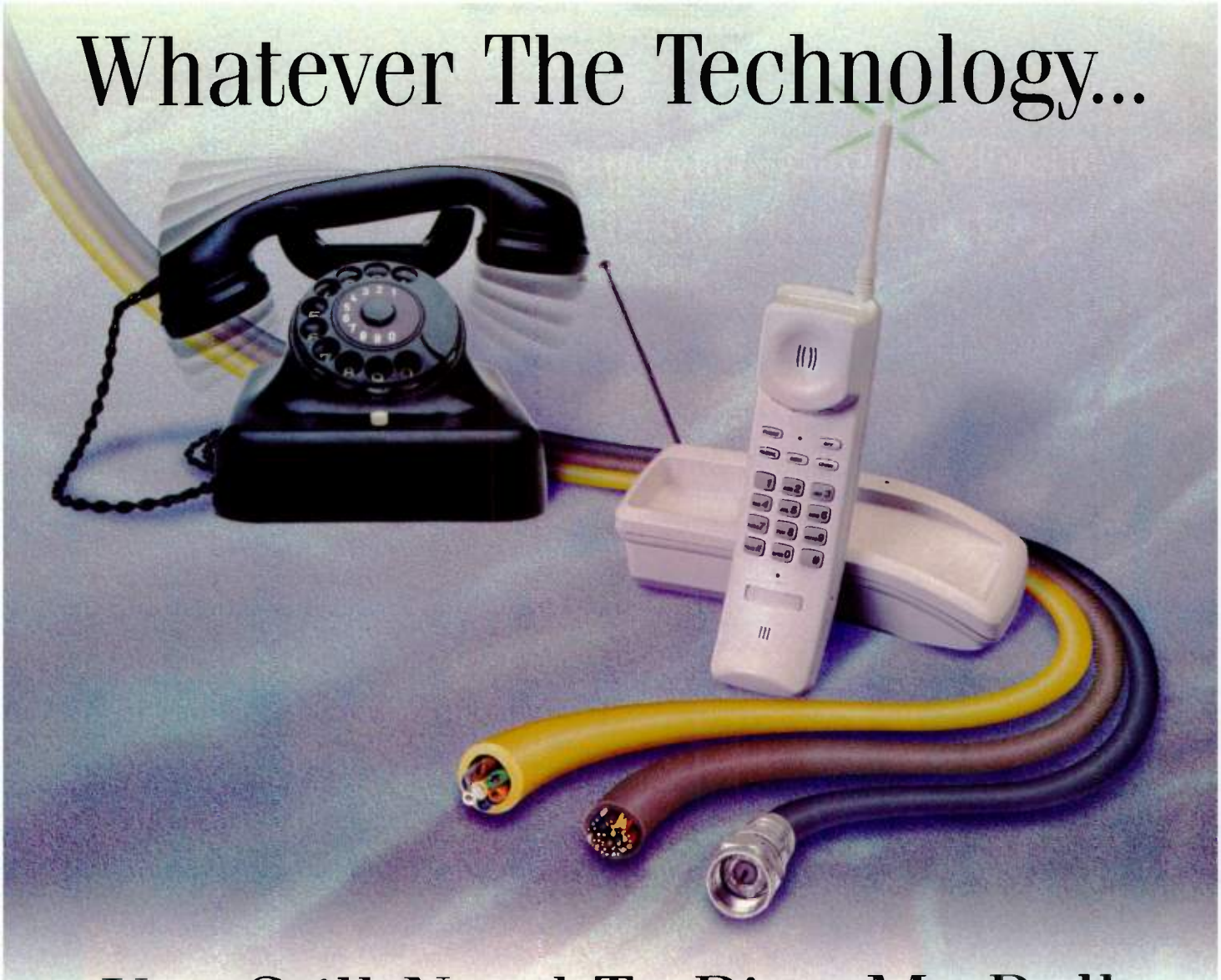
Zestron's U.S. location will include a fully equipped applications laboratory, comprehensive sales and technical services, and distribution and manufacturing capabilities. Its process labs will take test samples from customers, clean them under real process conditions, and return them to the customers for inspection, along with process and materials recommendations. For more information, contact Dr. Stefan Koschmieder, Zestron Corp., 21641 Beaumeade Circle, Ashburn, VA 22011; (888) 999-9116; fax (703) 821-9248. *PM*

Web Site Created To Simplify Pc-Board Quoting Process

PCB-Quote Inc.,Cupertino, Calif., has launched a web site that allows design engineers and purchasing agents to obtain multiple quotes for layout, fabrication, and assembly of printed circuit boards. The site, located at *http://www.pcb-quote.com*, is free to users.

At the site, users can enter their contact information once, and register with a user name and optional password. Thorough RFQ forms cover all aspects of pc-board creation. Visitors need only fill out one form per project, then select from a list of over 200 vendors. Vendors can be listed in either compact form (one per line) or expanded to a full screen with detailed technical and business specification. The quote request is automatically e-mailed to each selected vendor, who responds directly to the prospective customer. Any customer can request to have their own AVL (Approved Vendor List) included in their profile. Contact Mihai Beffa at (408) 345-9714; fax (408) 996-0590, or visit the website. *PM*

Whatever The Technology...



You Still Need To Ring My Bell

How will your design keep in stride with the explosive pace of information technology with both new and old means of connectivity? Whether your design requires a fiber, twisted pair or coaxial cable line - the push is to develop the ring signal at the curb within the remote switching module (RSM). The new UCC3750 is the first monolithic ringer circuit to make fiber to the curb a reality, and with its pin selectable reference frequency, it guarantees to ring your bell with optimum versatility. By generating a high voltage AC ring signal and a DC offset voltage in a single power conversion, your design is streamlined in less space and with the most cost-effective solution.

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Micrel's IttyBitty™ Op Amps.
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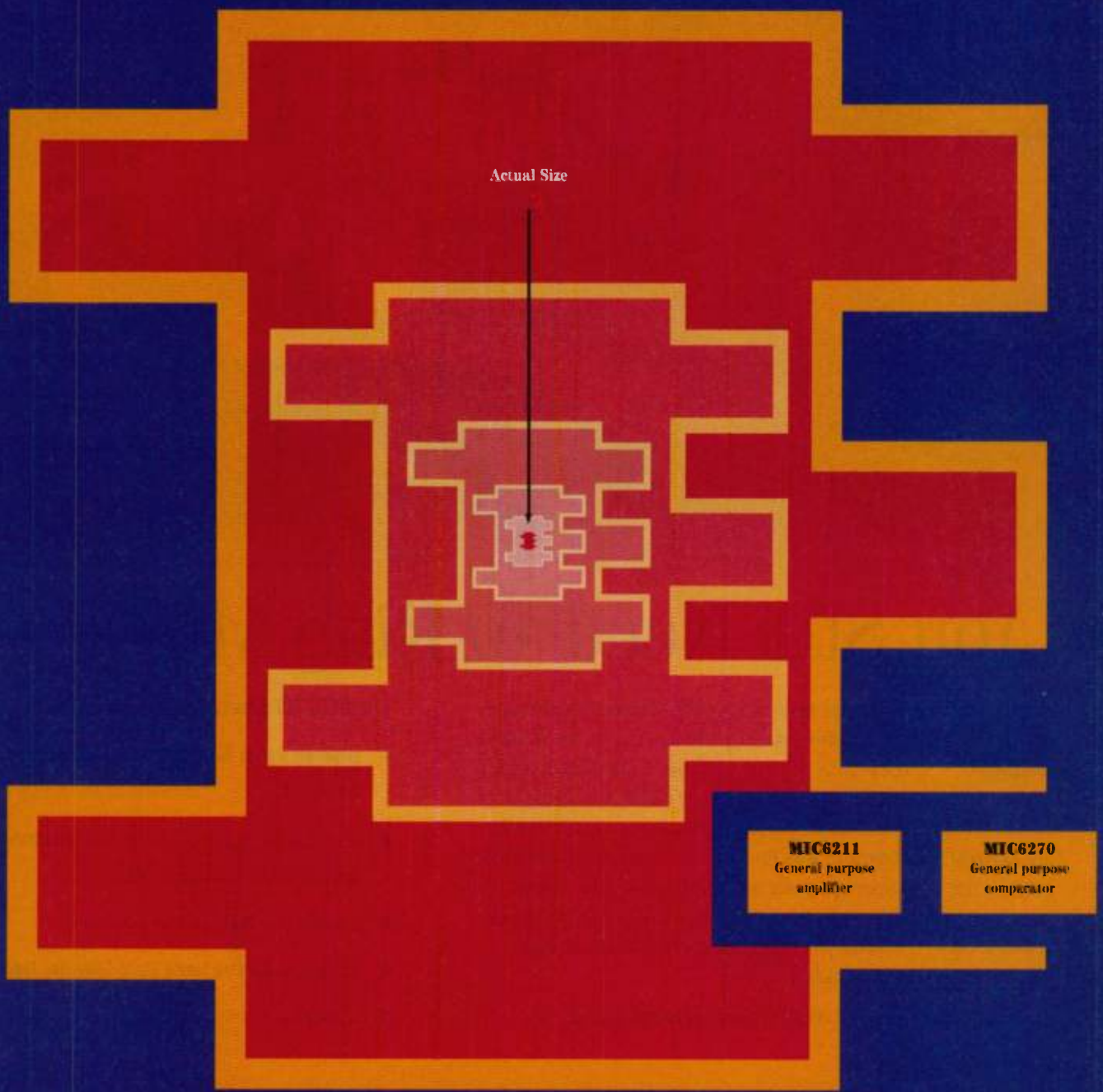

ANALOG DESIGN SOLUTIONS 2

Low-Power, High-Performance Op Amps In Micrel's IttyBitty™ SOT-23-5 Packaging

Because of customer demands for smaller and higher-performance op amps for the wireless and telecom markets, Micrel has developed a family of op amps that meet high-density systems requirements with low power, guaranteed high performance, and ultratiny packaging.

Micrel's IttyBitty™ and MM8™ packages are the smallest in the industry, saving critical board space and weight and minimizing signal path length–resulting in higher system performance and higher system packaging density.

IttyBitty SOT-23-5 Packaging

Micrel's IttyBitty and MM8 packages are the ideal solutions for designers of high-density systems such as cell phones, pagers, USB devices, PCMCIA cards and portable instrumentation. They are also ideal for applications where amplifier proximity to a sensor and/or short signal path is critical.

Guaranteed Performance Specs

Micrel's amplifiers carry performance beyond functionality. Operating from a single or split supply, performance is specified and guaranteed with supply voltages as low as 2.4V, most with supply currents less than 1mA.

Guaranteed Temperature Range

To ensure reliability in a wide variety of environmental conditions, Micrel amplifiers provide characterized and specified performance over a temperature range from $-40°C \le T_A \le +85°C$.

MICREL PART NUMBER	TECHNOLOGY	V_{SUPPLY}	I_{SUPPLY}	GBW	TCV_{OS}	GAIN ERROR	SR	V_{OS}	Ib	RESPONSE TIME
Op Amps										
MIC6211	Bipolar	±2.5V to ±18V	2.0mA	2.5MHz	4µV/°C	–	6V/µs	2mV	50nA	–
MIC7101	CMOS	2.4V to 15V	250µA	1.6MHz	1µV/°C	–	1V/µs	3mV	1pA	–
MIC7102	CMOS	2.4V to 15V	250µA	1.6MHz	1µV/°C	–	1V/µs	3mV	1pA	–
MIC7111	CMOS	2.4V to 10V	25µA	50kHz	2µV/°C	–	15mV/µs	3mV	1pA	–
Comparators										
MIC6270	Bipolar	±2.5V to ±18V	300µA	–	–	–	–	2mV	25nA	1.3µs
MIC7211	CMOS	2.4V to 16V	7µA		1µV/°C	–	–	3mV	0.04pA	4.0µs
Instrumentation Amp				–						
MIC6251/2	Bipolar	±2.5V to ±18V	2.0mA	2MHz	7µV/°C	0.5% max.	6V/µs	4mV	50nA	–

Extended Common-Mode Range

These devices feature an input common-mode range that extends beyond the supply voltage rails.

Key User Benefits

- Input common-mode range extends beyond supply voltage rails
- Guaranteed performance with supply voltages as low as 2.4V
- Low supply current
- Guaranteed performance over the full industrial temperature range of –40°C to +85°C
- IttyBitty SOT-23-5 package saves space and weight

MIC6251/2
Instrumentation amplifiers

MIC7101/2
Single and dual operational amplifiers

MIC7111
Rail-to-rail input and output amplifier

MIC7211
Rail-to-rail input comparator

For more information on Micrel's new family of low-power, high-performance op amps, call 1-800-401-9572.
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Micropower 12-Bit A/D for Portable Applications

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Benefits	Sipex	Linear Tech	Condition
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Power	0.56mW	2.2mW	@5v and 90µs
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Linearity	1 LSB	2 LSB	
Crosstalk	-120dB	-66dB	CH1 = 1MHz sqr wave, CH0 = 4.5v

SP8538 is a direct replacement for (Linear Tech) LTC 1298.

73dB Signal to Noise Ratio at a mere 1.25mW. Plus, the simple 3-wire SPI serial interface works easily with a wide range of microprocessors and microcontrollers. Noisy environments? The SP8538 with its "True" differential inputs and a Common Mode Noise Rejection (CMR) of 110dB @ 60Hz is the solution to your problem.

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High-Sensitivity Force Measurement May Quantify The Spin Of An Electron

Scientists from Stanford University and IBM's Almaden Research Center have developed a technique for measuring forces in the attonewton (10^{-18} newton) range. The measurement uses a microscopic cantilever 1000 times thinner than a human hair. The cantilever was designed for use in a new instrument the team is developing, a magnetic resonance force microscope (MRFM).

The MRFM has taken images at the micron level, according to team members. "The key to extending MRFM capability to the atomic scale is the ability to detect forces at the attonewton level," says Dan Ruger, IBM's Nanoscale Studies Manager. "This is the motivation for developing the new ultrasensitive cantilevers." Researchers hope the system will be able to measure the spin of a single electron for the first time.

Information on the new technique was presented at the American Physical Society meeting in Kansas City, Kan., by Timothy Stowe, a graduate student in applied physics at Stanford. Co-authors were Rugar, Thomas Kenny, assistant professor of mechanical engineering at Stanford; IBM visiting scientists David Botkin and Koichi Wago; and Stanford applied physics graduate Kevin Yasimura.

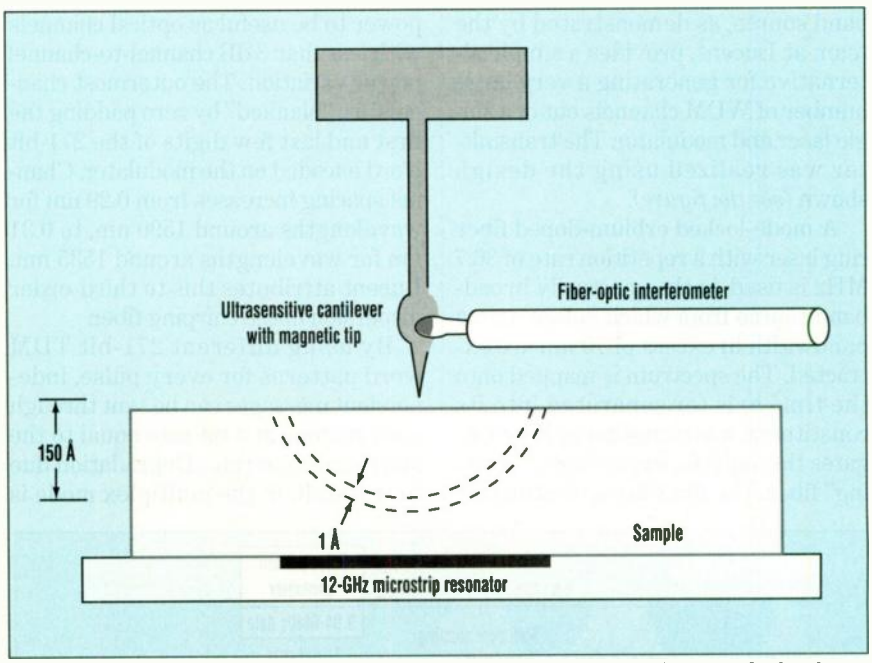
The MRFM combines the scanning tunneling microscope's ability to image individual atoms with magnetic resonance imaging's (MRI's) ability to tell one kind of atom from another. Like an MRI system, the new microscope uses an RF coil to excite a magnetic resonance in a sample, and by varying the frequency, the microscope can be tuned to interact only with specific types of atoms. But rather than using the same coil to detect the magnetic signals coming from the atoms, the new microscope employs the cantilever, whose tip is magnetized *(see the figure)*.

As the RF coil periodically reverses the polarity of the atoms in the sample, the magnetic force between the cantilever's tip and the sample oscillates, causing the cantilever to vibrate. An optical-fiber interferometer records the vibrations. As the tip is scanned over the sample's surface, it responds to magnetic signals from specific atoms within an annulus on the sample's surface. By recording variations in the amplitude of the cantilever's vibration at different positions, the scientists can make a three-dimensional map of the positions of the resonant atoms.

The cantilever—measuring 230 μm by 5 μm by less than 600-Å thick—is made of silicon because it minimizes the mechanical damping that occurs when the cantilever vibrates. It also is compatible with semiconductor processing techniques. The researchers started with a material called silicon-on-insulator, which consists of a very thin layer of silicon bonded onto a layer of silicon oxide that coats a silicon wafer. They etched the cantilevers out of the silicon layer, then chemically removed the underlying oxide.

The new microscope holds the promise of revolutionizing the study of biological processes at the molecular level, say the researchers. It also could impact the study of electronic materials at the atomic level.

John Novellino



The magnetic resonance force microscope being developed by researchers from Stanford and IBM uses a microscopic silicon cantilever that allows measurement of forces in the attonewton range.

Single, Ultrafast Laser Transmits Data Over 206-Wavelength Information Window

Using a single femtosecond laser, 1 km of single-mode fiber, and an electro-absorption modulator, researchers at Lucent Technologies' Bell Labs have devised a low-cost, reliable, and scalable method of performing wavelength-division multiplexing (WDM) on upwards of 206 channels—the largest number of channels ever reported for a WDM source. With their "chirped pulse" WDM transmitter, Lucent researchers may well have set the stage for low-cost fiber-optic routing in the local loop.

The method relies on the ability of the femtosecond laser to emit a short, 100-fs, broadband light pulse that is then propagated through the "chirping" fiber. Here, the natural tendency of different wavelengths in a light pulse to travel through an optical medium at different speeds causes

each wavelength to arrive at the end of the fiber at a slightly different moment in time. This allows the data to be encoded sequentially onto the WDM channels using the single data modulator. The bit rate of each channel is 36.7 Mbits/s (the repetition rate of the laser) and the channel spacing is 36 GHz (0.3 nm).

To date, experiments in WDM have depended on an individual laser corresponding to each wavelengthof light required for each channel. The wavelength stabilization and data encoding of such a large number of narrowband lasers has so far proven to be both a logistic and financial nightmare, thus limiting the success of this method to between 50 and 132 channels so far. Spectral slicing of a spectrally-broadband source, as demonstrated by the team at Lucent, provides a simple alternative for generating a very large number of WDM channels out of a single laser and modulator. The transmitter was realized using the design shown *(see the figure)*.

A mode-locked erbium-doped fiber ring laser with a repetition rate of 36.7 MHz is used as the spectrally broadband source from which pulses with a bandwidth in excess of 70 nm are extracted. The spectrum is mapped onto the time axis (or separated into its constituent wavelengths) as it propagates through the single-mode "chirping" fiber. The fiber has a total dispersion figure of D = -340 ps/nm. This stretches out the pulses to a duration of about 20.7 ns (corresponding to 76% of the bit period), with a nearly-linear time-wavelength relationship. An electro-absorption modulator (EAM) with a 12-GHz bandwidth is inserted at the output of the fiber to define and encode data onto each channel sequentially in time using a TDM-multiplexed pattern generator synchronized to the 271st harmonic (9.942 GHz) of the laser repetition rate. A 10% fiber tap inserted at the output of the chirping fiber is used to dynamically adjust the bias on the EAM and equalize its output.

Of the 271 possible wavelength slots defined by the modulator, 206 can be identified with sufficient optical power to be useful as optical channels with less than 3 dB channel-to-channel power variation. The outermost channels are "blanked" by zero padding the first and last few digits of the 271-bit word encoded on the modulator. Channel spacing increases from 0.29 nm for wavelengths around 1590 nm, to 0.31 nm for wavelengths around 1535 nm. Lucent attributes this to third-order dispersion in the chirping fiber.

By using different 271-bit TDM word patterns for every pulse, independent messages can be sent through each channel at a bit rate equal to the laser repitition rate. Degradation due to crosstalk in the multiplex mode is less than 1 dB.

According to Martin Nuss, staff scientist at Bell Labs and one of the builders of the prototype multiplexer, "The key enabling factor is the fact that femtosecond lasers in the 1.5-µm frequency range have only become practical within the last couple of years with the advent of erbium-doped fiber. The "chirped"-pulse encoding scheme is simply something nobody else thought of."

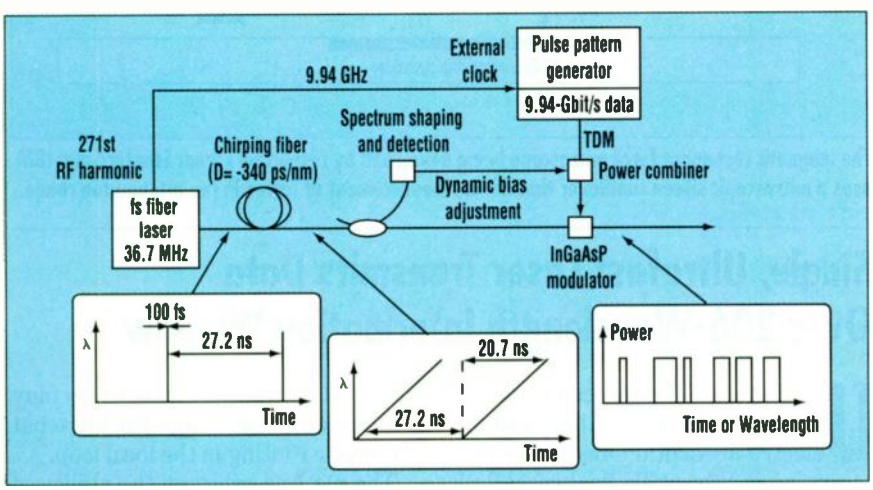
Elegance and simplicity are the design's chief attractions. The modulator is a conventional electro-absorption TDM modulator, chosen over a lithium-niobate modulator because it is more compact and less expensive. It is well capable of operating at the aggregate data rate for each channel (the experiments ran it at 10 Gbits/s).

The modulator not only determines the position but also the spacing between channels, a key parameter when a splitter in the field is subjected to temperatures from -40° to +80°C. With these variations, the passband of the splitter will change, and these changes must be tracked. In the case of Lucent's device, tracking can be accomplished by simply adjusting the timing of the modulator. With previous schemes using multiple lasers, each laser had to be adjusted individually on the fly.

While the 36- to 40-Mbit/s-per-channel data rates now possible are sufficient (if not ideal) for fiber-to-the-curb or to-the-home applications with their 40- to 50-Mbit/s data-rate requirements, Lucent is now focusing on scaling the device up to the terabit/s range. This may be achieved by lessening the dead space between emissions. Although this can be done by raising the repetition rate of the laser emitter, eventually, the rate will be too high for the TDM to track accurately. The research team instead is working on a parallel modulator scheme whereby all the even channels are encoded by one modulator and all the odd channels by the other. While the relatively high cost of the femtosecond laser also is also an issue, it is expected that the cost will drop as demand increases over time.

For more information, contact Martin Nuss at Lucent Technologies' Bell Labs at (908) 634-3433.

Patrick Mannion



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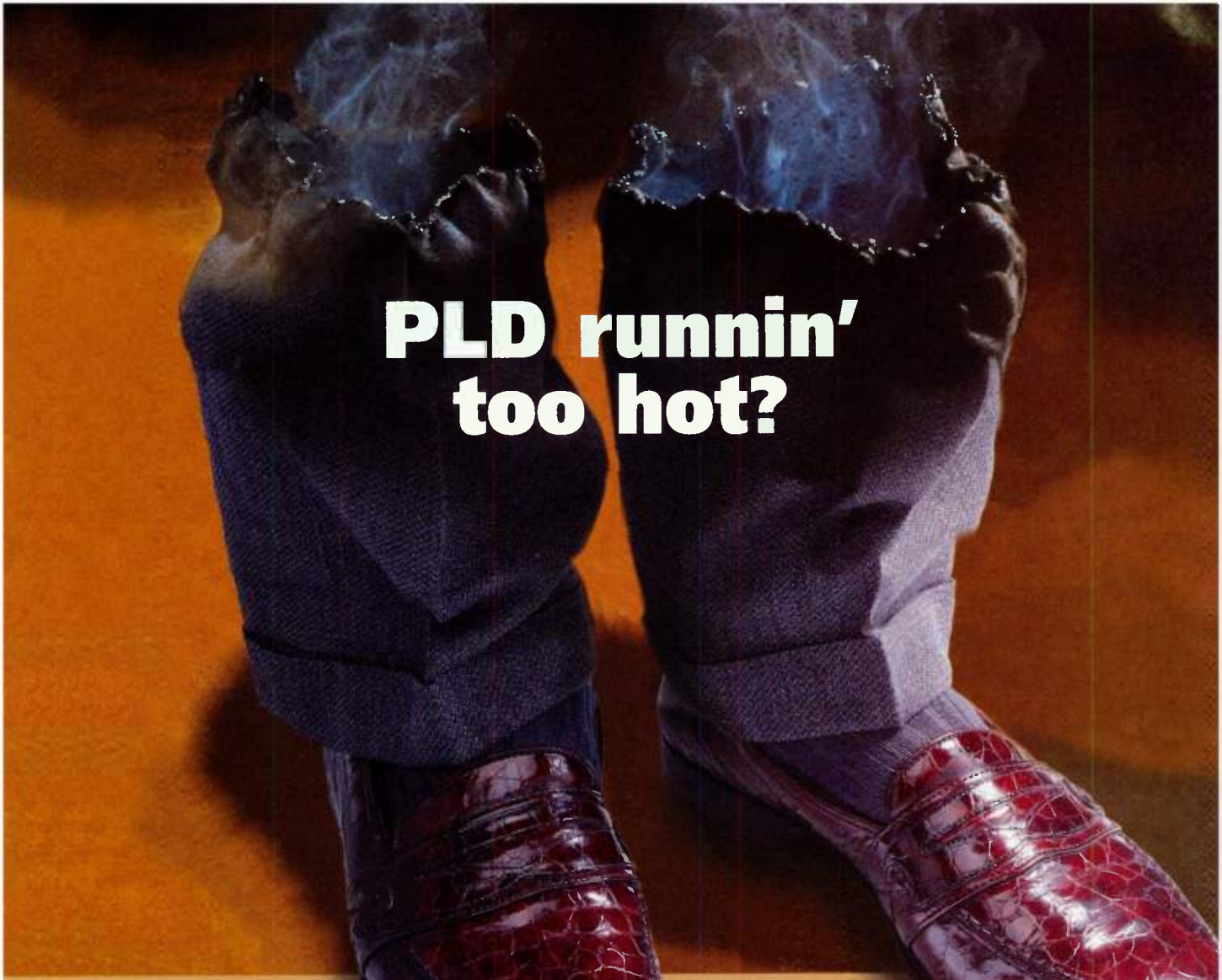

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SID Conference Highlights The Road To Invention

Innovative Developments In CRTs, LCDs, And FEDs Will Encourage New Applications For Displays.

Cheryl Ajluni

Much excitement surrounds this year's Society For Information Display (SID) Conference, as it gears up to celebrate two of the most significant events to ever take place in the display industry: the 100th anniversary of the invention of the Braun tube and the 25th anniversary of the fabrication of the first active-matrix liquid-crystal display (AMLCD). The conference and exhibition, scheduled for May 11-16 at the Hynes Convention Center in Boston, Mass., will commemorate these events with a series of papers to be presented Tuesday, May 13. The papers will review the history and significance behind these inventions. In addition, a special exhibition, aptly titled "From Braun tube to the FED in 100 years," will be open for viewing daily in the lobby of the exhibits area.

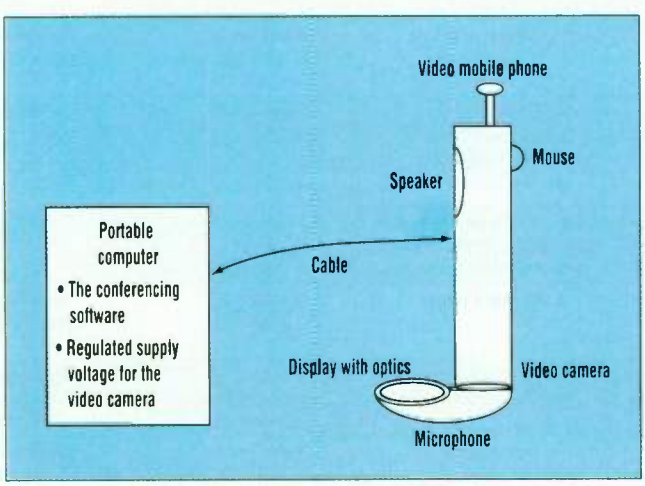
In keeping with the theme of inventions that have shaped an industry, the conference is packed with over 60 technical sessions focusing on such subjects as AMLCDs for projection and desktop applications, display-addressing techniques, optical components, CRT deflection and magnetic radiation, display phosphors, miniature CRTs, interactive display systems, field-emitter displays, plasma displays, color printing, and large-area display systems for home theater and electronic cinema. With short courses planned for Sunday, a variety of technology and application seminars, and an evening panel session, not to mention over 330 exhibition booths, there is bound to be something for everyone *(see the table)*.

Applications Galore

One of the truly exciting parts of the SID Conference and Exposition is the realization that much of the research and development it highlights may one day form the basis for consumer products. This year, attendees are able to hear about many of these new applications firsthand.

A collaborative effort from a group of researchers at the Tampere University of Technology, Tampere, Finland, and the Nokia Research Center, Video Technologies Laboratory, Tampere, Finland, for example, yielded the development of a video mobile phone that offers on-line teleconferencing capabilities. Highlighted in "A teleconferencing implementation using a miniature electroluminescent display," the development is expected to help significantly advance the use of mobile phones.

The device combines a mobile video phone with an electroluminescent (EM) display and an integrated mouse to allow mobile teleconferencing *(Fig. 1)*. The phone is connected to a 66-MHz networked computer with a minimum of 16 Mbytes RAM that is running the Intel ProShare videoconferencing software. This software package was chosen because it enables easy photo exchange and transfer of files and business cards between conference participants.



1. A proposed mobile video phone uses an electroluminescent display, which keeps the weight down and allows operation in both high- and low-brightness environments.

The EM display, chosen for its high resolution (640 by 480 pixels with a 5- bit gray scale) and light weight, is mounted on a movable external module. A monochrome video camera is mounted on the bottom of the Nokia phone, and a mouse input device is mounted on the backside. The camera's power comes from the computer's 12-V supply via an auxiliary voltage converter within the computer's chassis.

To test the setup, a conference connection was estab-

lished between two computers. One computer used the video mobile phone as an I/O device while another computer used identical conferencing software, a conventional CRT monitor, and an ordinary color camera. The video image quality of the teleconference was determined to be acceptable. Continuing work on the video mobile phone will now focus on making it commercially viable as a consumer product.

Another interesting development, a new 3D imaging technology, comes from Floating Images Inc., Westbury, N.Y. Described in "A new real-depth 3D imaging technology not requiring special glasses or other visual aids," the technology offers a combination of hardware and software components that allow the user to view off-the-screen 3D images. The authors hope their development will become the standard for home and arcade video games, computers, corporate presentations, Internet/intranet viewing, and television.

Traditional 3D technologies are flat on a screen and typically require special glasses to be viewed. In contrast, the Floating Images technology provides traditional depth cues such as perspective, background, and image occlusion, in addition to horizontal and vertical binocular parallax and accommodation. Because the accommodation coincides with convergence, viewing of these images does not produce headaches, fatigue, or eye-strain, regardless of how long they are viewed. These difficulties are often associated with both the stereoscopic or autostereoscopic displays.

To use this technology, the imagery, whether video or computer generated, must be formatted for the Floating Images platform. Existing software can be reformatted. An adapter attached to a television or computer monitor, or plugged into an existing projection system enables 3D projection in midair. Although, to date, an adapter has only been fabricated for a 20-in. display (at a cost to manufacturers of under $25), the authors foresee no limit to the size of such a device.

A device that has gained much notoriety in recent months is the smart card. Typically used for applications such as cash cards, telephone cards, and toll booth payment cards, (and often coupled with sensor technology), the smart card's use has been slowed by issues of durability, reliability, and limited functionality. Researchers from the University of Stuttgart, Germany in "Bistable FLC- and Choles-

1997 SOCIETY FOR INFORMATION DISPLAY CONFERENCE TECHNICAL PROGRAM

Tuesday, May 13					
7:30 A.M. to 9:00 A.M.	**Applications Seminar A-1** Display market forecasting	**Applications Seminar A-2** LCD optical performance modeling			
10:40 A.M. to noon	**Session 4** Direct-view AMLCDs	**Session 5** Bistable nematic LCDs	**Session 6** FEDs	**Late-news papers**	**Session 7** Novel display devices
2:00 P.M. to 3:20 P.M.	**Session 8** New AMLCD technologies	**Session 9** Bistable reflective LCDs	**Session 10** Field-emission devices: Electron trajectories	**Session 11** Color CRTs I	**Session 12** Display systems architecture
3:40 P.M. to 5:00 P.M.	**Session 13** AMLCD structures	**Session 14** LCD conduction/ electroclinics	**Session 15** Color plasma displays	**Session 16** Thin CRTs	**Session 17** Head-mounted 3D visualization displays
8:00 P.M. to 10:00 P.M.	**Evening Panel E-1** The CRT: Still going strong or facing extinction?	**Evening Panel E-2** FPD manufacturing in the U.S.	**Evening Panel E-3** Display technologies Asian companies are betting on		
Wednesday, May 14					
7:30 A.M. to 9:00 A.M.	**Applications Seminar A-3** Low-power display module electronics	**Applications Seminar A-4** FPD inspection, test, and repair			
9:00 A.M. to 10:20 A.M.	**Session 18** Microdisplays	**Session 19** LC alignment	**Session 20** FED materials and structures	**Session 21** Color CRTs II	**Session 22** Backlighting systems
10:40 A.M. to 12:00 noon	**Session 23** Large-area AMLCDs	**Session 24** Advances in TN- and STN-LCDs	**Session 25** Phosphors	**Session 26** CRT screens and coatings	**Session 27** Applications: Display lighting
Thursday, May 15					
7:30 A.M. to 9:00 A.M.	**Applications Seminar A-5** Display module design	**Applications Seminar A-6** Backlighting for direct-view and projection displays			
9:00 A.M. to 10:20 A.M.	**Session 28** Projection display components	**Late-news paper**	**Session 29** Organic EL	**Session 30** CRT deflection technology	**Session 31** Applications: Plastic substrates and laminates
10:40 A.M. to 12:00 noon	**Session 32** Display reflectance and contrast	**Session 33** Wide-viewing angle I	**Session 34** Electroluminescent displays	**Session 35** FPD manufacturing: Processes	**Session 36** Applications: Display addressing & electronics
2:00 P.M. to 3:20 P.M.	**Session 37** Large-area display systems	**Session 38** Wide-angle viewing II	**Session 39** Synthetic vision displays in the transportation industry	**Session 40** FPD manufacturing: Color filters	**Session 41** Applications: Display optics
3:40 P.M. to 5:00 P.M.	**Late-news paper**	**Session 42** Reflective color LCDs	**Session 43** Human factors and measurements	**Session 44** FPB manufacturing: Substrate structures	**Late-news papers**

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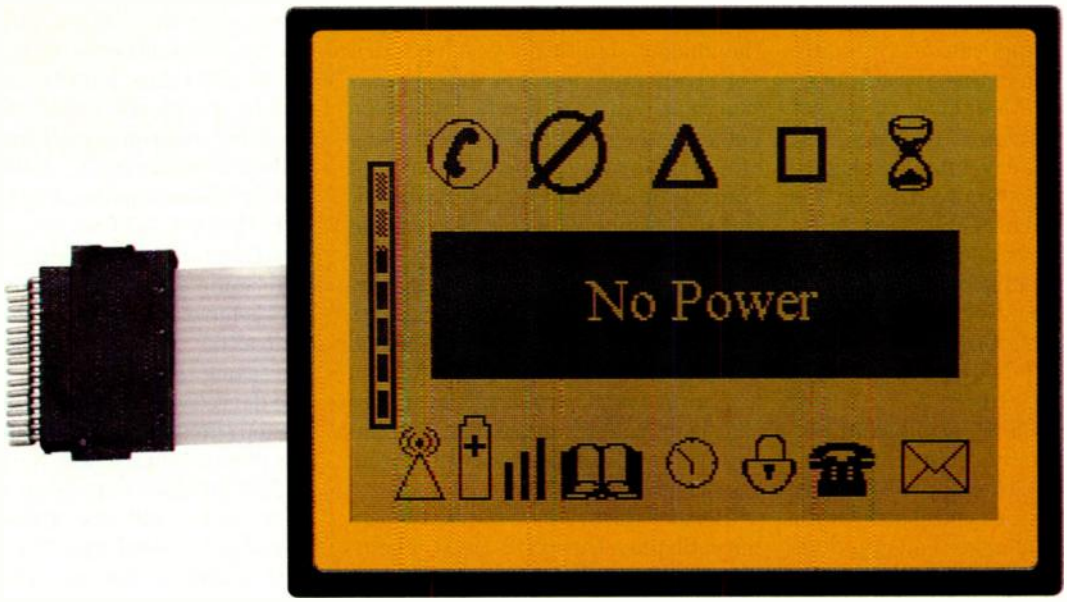

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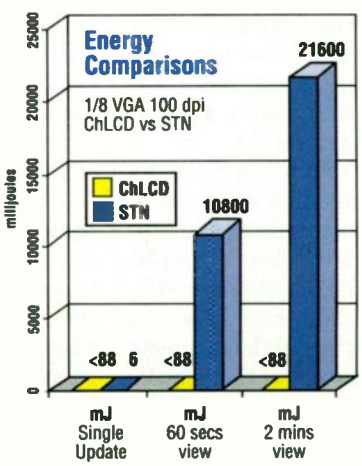
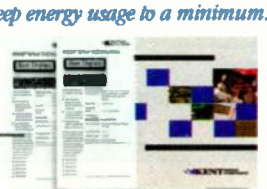


Unlike STN displays which use power to continuously refresh images, ChLCDs do not require refreshing to keep energy usage to a minimum.



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teric LC displays on plastic substrates for smart card applications," detail a potential solution to these limitations.

They developed two types of bistable reflective displays: a cholestric liquid crystal in a surface-stabilized cholestric texture mode (SSCT) and a surface-stabilized ferroelectric liquid crystal (SSFLCD) with flexible plastic substrates. They also came up with a new manufacturing technique for the ferroelectric liquid crystal that yields good substrates and a cell gap of 1.6 μm.

The SSCT display stands out because it is backed by a simple and inexpensive manufacturing process that does not require the typical polarizers. It also exhibits a larger cell gap than the SSFLCD. The SSFLCD, on the other hand, offers a reduced sensitivity against pressure and bending, as well as a small switching voltage of only ±2.8 V.

Because they can display nonvolatile information for a long time without requiring any energy, the bistable displays are prime candidates for smart cards. The flexible displays also can be mass produced at a very low cost.

An innovative automotive application comes from researchers at the Optoelectronic Computing Systems Center at the University of Colorado at Boulder. As presented in "An automotive HUD implemented with a planarized, 640-by-512 LCOS microdisplay," the invention consists of a heads-up display (HUD) that projects a virtual image in front of the vehicle, near the driver's direct line-of-sight. The unit, which employs a liquid-crystal on-silicon (LCOS) microdisplay as the imager, significantly reduces driver strain and improves driver reaction times, since the drivers eyes need not leave the road. The device is being aimed at the navigation display and route guidance information, traditional instrument cluster gauges, and other human-machine interface data.

During operation, an image generated by the microdisplay is first magnified into a larger real image. The real image is then further magnified into a 229-mm-by-165-mm virtual image that is viewed by the driver. The image is viewed at a distance of 2 m from the driver.

Besides the 640-by-512-pixel LCOS microdisplay, the optical system employs a 50-mm F/1.3 C-mount objective lens, a double-element field lens (consisting of a diffraction grating and Fresnel lens), and a dash-mounted holographic optical element. The unaltered windshield serves as the system combiner. The display's active matrix backplane, designed for a nominal electronic refresh rate of 8000 frames per second, is composed of 640-by- 512 DRAM-style pixels fabricated in a 1.2-μm CMOS process, and has a 0.7-in diagonal active area. CMOS circuitry is used for on-chip clocking and control, shift registers, and test structures.

From researchers at the Armstrong Laboratory's Human Engineering Div., Wright-Patterson AFB, Ohio, and the Night Vision Corporation, Lincolnwood, Ill., comes a night vision goggle (NVG) that demonstrates a significantly improved field of view of up to 100°. As detailed in "Development and evaluation of the panoramic night vision goggle," the NVG relies on the use of four image-intensifier tubes, instead of the usual two, to provide the wearer with better situation awareness, improved look-under and look-around unaided vision, and reduced operator fatigue.

In the past, NVGs have typically offered fields of view ranging from 30° to 40°. Some specialized, non-fielded, NVGs have delivered fields of view as wide as 60°. But in the earlier devices, increasing the field of view would lead to a decrease in resolution. The use of the four image-intensifier tubes solves this dilemma in the new NVG.

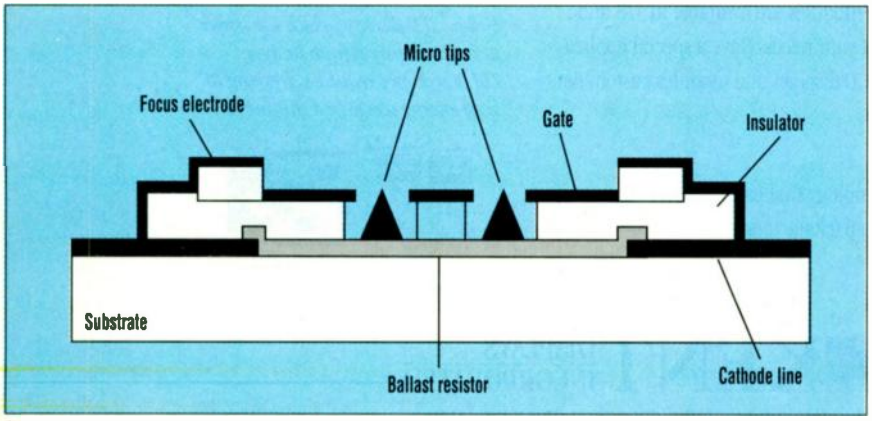
The goggles consist of dual eyepieces, tilted and fused together, integrated with folded optics, and a total of four objective lenses to provide the user with a true panoramic view. The panoramic NVG features an intensified, partial-overlap field of view of 100° horizontally by approximately 40° vertically. The central 30° horizontal by 40° vertical portion is completely binocular. The right 35° portion is seen with the right eye only and the left 35° portion is viewed by the left eye only.

On The CRT Front

The CRT has played a vital role in the growth of the display industry over the years, with the Braun tube as the first modern CRT. The CRT's length and volume, however, have led to research in other technologies in an effort to build large-area, flat-panel televisions. The LCD and plasma display panel (PLD) have been considered, but are expensive. In answer to this dilemma, researchers from Sony Corporation's Atsugi #2 Technology Center, Atsugi-City, Japan, have developed and built a prototype flat-Trinitron color CRT.

Detailed in "A newly developed super-flat Trinitron color CRT," the 26-V, 16:9 aspect ratio CRT incorporates completely flat face glass as well as a host of other innovative developments, including tempered glass, engineering film, and a technique for supressing aperture grille vibrations. To help reduce specular reflection and improve contrast, the CRT's surface is treated with an antireflection film. The flat screen is achieved by removing the horizontal curvature.

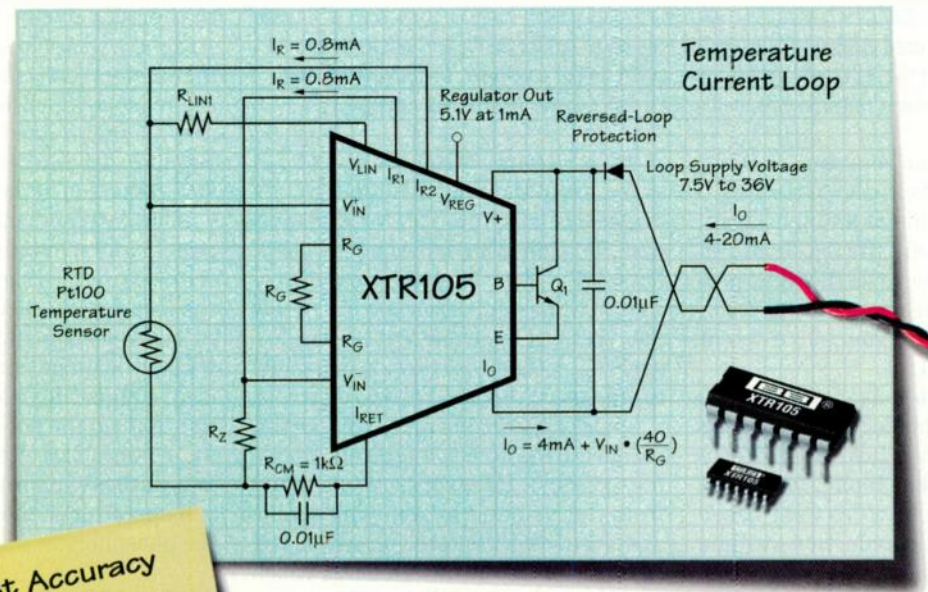
The result of all these improvements is a large-sized CRT with a fully



2. This gated-field emitter is a field emision display (FED) using an in-situ focus-gate design employs an additional electrode with the same potential at the cathode line. The micro tip of the field emitter is connected to the cathode line by a ballast resistor.

4-20mA

New Generation Transmitter IC



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XTR105 is a new generation 4-20mA transmitter IC with precision on-board linearization circuitry. Its low-drift instrumentation amplifier input stage beats bulky discrete op amp circuits. Laser trimmed performance eliminates troublesome adjustments and reduces your manufacturing costs. Versatile excitation current sources (two, 800µA) are suited to a wide range of sensors including RTDs, bridges, potentiometers and others.

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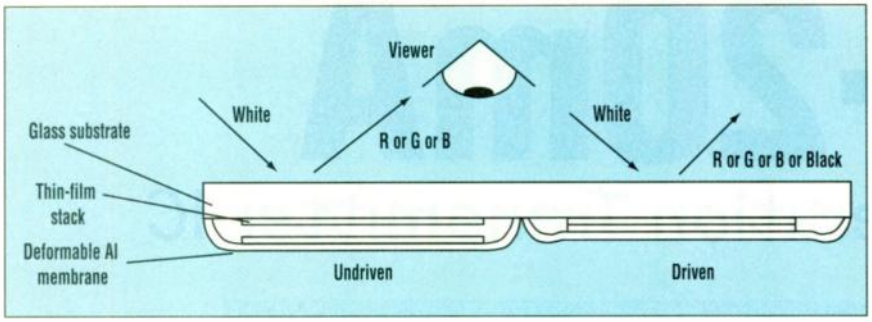

3. The IMod MEMs-based display technology is based on an optical cavity that can be deformed to change the color of the reflected light with the application of a voltage. Traditionally IMods have exhibited low power requirements, and require only passive matrix addressing.

flat screen that can reproduce images without geometric distortion, and with less reflection of ambient light. As an added benefit, the flat-Trinitron CRT can be produced on the same production line as the conventional Trinitron tube with a minimum investment in new equipment.

Other companies also are researching flat-CRT technology. Researchers from the Kanazawa Institute of Technology, Ohgigaoka, Japan, for example, have developed a flat CRT based on an electrostatic deflection system. Their paper, "A new type of flat CRT with line-heated cathodes," describes a tube that employs a line-heated cathode to emit an electron beam. Using a pair of electrodes to simultaneously control focus and deflection, the structure of the electrodes in the CRT is significantly simplified, so it can be built at a low cost.

The CRT consists of many modules incorporating cathodes, glass posts, support vanes, electrodes, and glass plates. The cathodes are stretched vertically between flat-glass posts set behind the device's support vanes, to help prevent vibration. Modulation electrodes are placed behind the cathodes, and a cover electrode is placed in front of the cathodes. An aperture, cut in each segment of the cover electrode, allows for the emission of electrons from the cathode. On top of the cover electrode are horizontal focus and deflection electrodes insulated from one another. Vertical focus and deflection electrodes, placed at the side of the support vanes, are formed by painting the vanes with a silver paste. The support vanes are sandwiched between a front glass plate and a back glass plate, protecting the tube from atmospheric pressure.

In a similar development, researchers at the Philips Research Laboratory, Eindhoven, The Netherlands, have developed an experimental 17-in. flat CRT with a panel thickness of only 1 cm. The design, described in "A new flat, thin-CRT technology," uses a linear wire cathode at one side of a panel to emit electrons into vertical channels. Then, the electrons are transported parallel to the screen by the hop transport process. Electrons are extracted from the channels by applying a voltage pulse to horizontal electrodes at the rear side of the extraction plate, which contains rows of exit holes. These electrons then enter a constriction plate used to equalize the average energy of the electrons. Two- or three-fold beam switches are then used for color-dot selection. Then the electrons accelerate towards the phosphor screen.

Advances In FEDs

FEDs, or Field Emission Displays, have shown a great deal of promise in recent years as a challenger to the AMLCD. A development out of the Industrial Technology and Research Institute, Chutung, Taiwan, heightens that challenge. In "A CRT-like field emission display," the researchers describe a gated-field emitter with an in-situ focus-gate design *(Fig. 2)*. The design's strengths are its inherent simplicity and efficiency

With a well-focused field emission, for example, the anode can be placed away from the cathode plate such that all high-voltage and high-efficiency phosphors can be directly applied to the FED. In addition, this design allows for high-energy input, high resolution, and a long lifetime. Tests showed that an in-focus, structured FED allows a cold-cathode free-electron beam, with a 330-μm-by-330-μm pixel size, to be confined to the diameter of a 450-μm light spot on a phosphor screen, at a distance of 5-mm.

From the Research and Development Center of Futaba Corp., Chiba, Japan, comes "A new structure and driving system for full-color FEDs." This low-power driving system was made possible through improvements to the duty cycle of the FED, and a structure that allows for better focusing of electron beams. Compared to the more conventional single-matrix type of single-anode driving system, Futaba's driving scheme allows for an 80% reduction in the terminals.

This development of full-color FED panels and a driving system using a simple structure significantly improve the focusing characteristic of the cold-cathode electron beam. Image display without leakage emission also is realized, suggesting the potential to further reduce the power consumption of full-color FEDs. Research is ongoing in the areas of improving the structure and operation of the FEDs, along with the phosphors.

As For LCDs And FPDs...

On the LCD front, a new high-speed drive scheme for bistable reflective cholestric displays has been developed that reduces the addressing time to a mere 50 μs. The most significant impact of this development is that the fast addressing opens the door for the use of cholestric liquid crystals in video-rate applications.

According to "High-speed dynamic drive scheme for bistable reflective cholesteric displays," by researchers at the Liquid Crystal Institute, Kent State University, Ohio, the advance uses a five-phase process. These phases include preparation, preselection, selection, post-selection, and evolution. The state of the material after addressing depends only on the voltage in the selection phase, which is typically about 50 μs long. The voltages in the other phases are fixed at appropriate values, and the drive waveform is implemented using a pipeline algorithm. With this drive scheme, up to 1000 lines of the bistable cholestric display can be updated in less than 0.1 second.

Another innovative development comes from Etalon Inc., Iridigm Dis-

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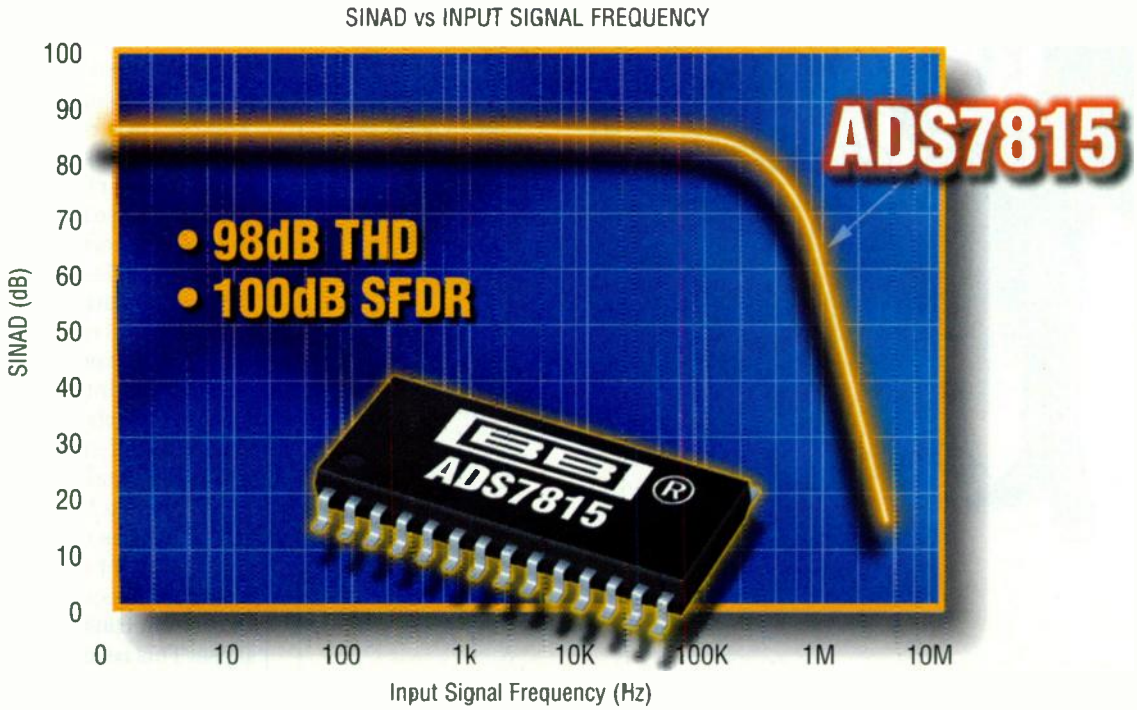

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Products	INL (LSB)	NMC* (Bits)	Sample Rate (kHz)	Power (mW)	SINAD (dB)	THD (dB)	Resolution (Bits)	FAX*LINE* Number	Reader Service #
ADS7813	±2	16	40	30	87	–96	16	11302	85
ADS7815	±4(Typ)	15	250	250	84	–96	16	11364	86
ADS7821	±3	16	100	100	86	–94	16	11323	87
ADS7825	±2	16	40	50	86	–90	16	11304	88

*No Missing Codes. *For Technical Information: http://www.burr-brown.com/Ads/ADS7815-Ad.html*

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play Corp., Boston, Mass., and is discussed in "Interferometric modulation: A MEMs-based technology for reflective flat-panel displays." The authors came up with a micromachined, deformable optical cavity whose reflected color changes with the application of a voltage. Known as an interferometric modulator (IMod), the display can achieve switching speeds of greater than 50 kHz, and a prominent hysteresis. Experimental models of the IMod suggest the potential for greater than 80% reflectivities, and contrast ratios of greater than 40:1. With this performance, the display shows promise for use with video-rate, full-color reflective FPD's.

This MEMs-based display technology, which addresses many of the shortcomings of other MEMs modulators around today, relies on the phenomenon of interference to alter the color of reflected light *(Fig. 3)*. It consists of a self-supporting, deformable membrane and a thin-film stack, both residing on a transparent substrate which acts as the mirrors of an optically resonant cavity. When a voltage is applied, electrostatic forces are produced that cause the membrane to collapse. This reaction causes in a change in the color of the reflected light, which is determined by the distance between the membrane and the stack.

Since the device operates in a binary fashion, it can easily switch from one color to another, or from one color to black. To achieve a full-color display, three sets of IMods are needed, with dimensions selected to allow red-black, green-black, and blue-black switching respectively. Arranged in RGB stripes, the color white can be achieved by an additive mixture of all three stripes. Also, true-black and white displays are possible by combining alternating sets of IMods.

For further information regarding the SID 1997 Conference, contact Mark Goldfarb of the Palisades Institute for Research Services Inc., 1745 Jefferson Davis Hwy., Suite 500, Arlington, VA 22202; (703) 413-3891; fax (703) 413-1315.

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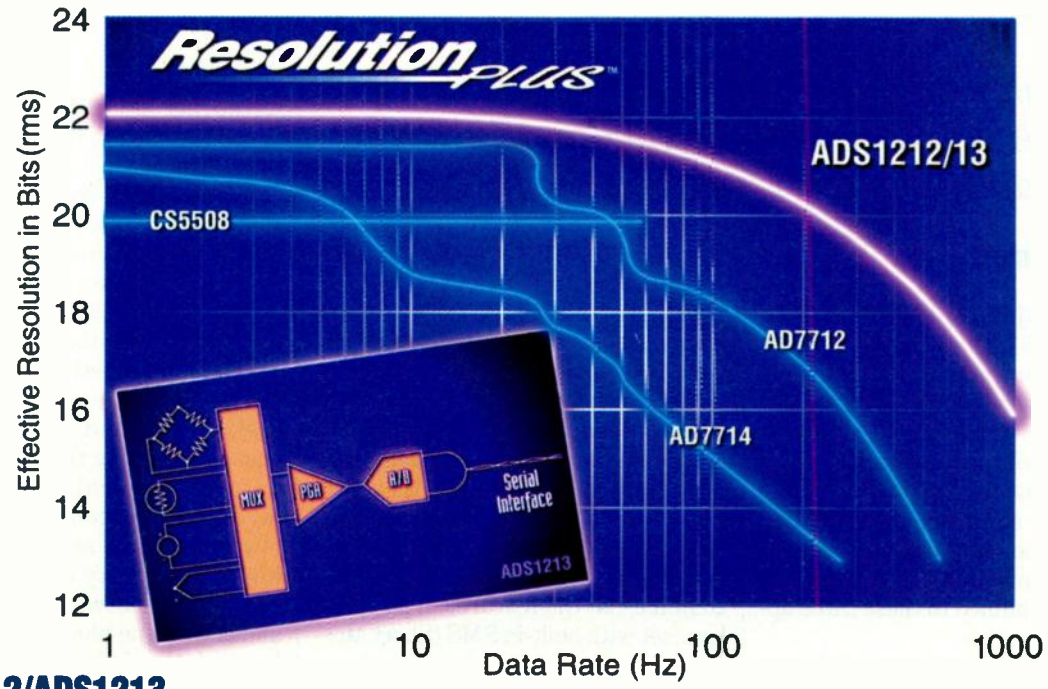

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ADS1211	±0.0015	No Missing Codes	24	20	26	11284	90
ADS1212	±0.0015	No Missing Codes	22	16	1.4	11360	91
ADS1213	±0.0015	No Missing Codes	22	16	1.4	11360	92

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CONFERENCE REVIEW

Security, Telecommunications, And Multimedia Share Spotlight At CeBIT

Although Finished Products Are The Main Focus, A Number Of Chip Vendors Exhibited Their Latest System-Level Offerings.

Alfred Vollmer

Three major topics dominated CeBIT '97, the world's biggest computer and communications show, recently held in Hannover, Germany—security, telecommunications, and multimedia. Although CeBIT is usually a show for finished products (and not for components), several semiconductor manufacturers presented new products that were not necessarily confined to these three application areas.

The major focuses in terms of security were on smart card technologies and Internet security. As was the case at CeBIT '96, transmitting data securely over the Internet was on everybody's mind this year, but with another viewing angle. There were many Internet security solutions (including cyber cash) that were featured, and in most cases, the key element for each solution was a cryptographic chip card.

In the telecommunications arena, GSM (Global System for Mobile Communications) and DECT (Digital European Cordless Telephone) were the major innovation areas. For example, Motorola Corp., Schaumburg, Ill., and Philips Consumer Communications NV, Eindhoven, The Netherlands, both displayed cellular phones weighing less than 100 grams. Philips' "Genie" phone is claimed to be the lightest cellular phone available, and also the only one that is voice-controlled. It ends calls automatically and offers voice-dialling of up to 10 prestored numbers. Siemens AG, Munich, Germany, displayed the first cellular phone with a color display.

An environmentally-friendly solution was presented by Nokia. They featured a solar battery pack for the 1611 phone that allows easy recharging by exposing the battery pack (or the whole phone) to sunlight. In addition, there were several solutions that allowed data transmission over cellular phones without special adapters where only a cable to the PC is needed.

The GS18 mobile phone handset from Ericsson Mobile Communications AB, Stockholm, Sweden, that combines all the features of a typical handset with built-in SMS (Short Message Service), fax, data, and phone book management. Another interesting solution was the GSM data cards that were exhibited by Ericsson and Nokia Mobile Phones Ltd., Espoo, Finland. Ericsson's GC25 GSM data card fits into any type III PC card (PCMCIA) slot on a PC. By using the embedded Windows software and an antenna, the GC25 enables users to connect to any data network or fax.

Nokia's PC card GSM phone is even smaller and fits into a PC Card type II or III compatible slot with an antenna already included. It works with basic Windows 95 applications such as Microsoft Phone, Microsoft Exchange, and Netscape Navigator, as well as communications applications including Microsoft Mail, WinFax PRO, and ProComm Plus. By using this card with a headset, a multimedia PC also becomes a cellular phone. Both products were designed within the Mobile Data Initiative, a collaboration between Intel Corporation, Santa Clara, Calif., various equipment manufacturers, and GSM network operators.

In the multimedia sector, exhibitors from the Asia-Pacific region were dominant. Adding to the trend of offering more functionality on smaller boards at lower prices, color scanners and image processing software were all the rage at CeBIT '97. And most of these scanner manufacturers were from Taiwan.

While several companies (including Philips and Panasonic) featured their first DVD solutions, Philips launched a new generation of non-DVD CDs with its CD-Rewriteable (CD-RW) drives. CD-RW disks allow data to be overwritten directly and repeatedly in the same way as a floppy disk. The disks are based on a new phase-change recording technology in which data is represented in a recording layer by repeated transitions from low-reflectivity amorphous areas to high-reflectivity crystalline areas. Transitions between the amorphous and crystalline phases are induced by heating the recording layer with a laser of varying intensity during recording. They offer a storage capacity of up to 650 Mbytes and are compliant with the International Orange Book Part III specifications. This means that they can be read using Multi-Read CD-ROM drives or CD recorders with CD-RW capability.

New Systems Solutions

Philips Semiconductors NV, Eindhoven, The Netherlands, announced a newDVD system solution for single/dual layer DVD-ROM applications. The chip set offers 2 x DVD and 16 x CD performance and works with all known DVD mechanisms. "Manufactured using 0.65-micron technology, Philips' DVD ROM solution already matches the highest operating speeds currently available," said John Benson, International Product Marketing Manager, Consumer ICs at Philips' Southampton, U.K., facility. "As we move to 0.35-mm technology and greater integration, the opportunity for system improvements is tremendous."

At the heart of this system solution is the SAA7335 DVD decoder/DSP and the SAA7381 block decoder/host interface, which provides all the nec-

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Products	Bits	Speed (MHz)	Supply (V)	Power (mW)	REF	FAX*LINE* #	Reader Service #
ADS900	10	20	3	54	Int	FAX*LINE* 11347	80
ADS901	10	20	3	49	Ext	FAX*LINE* 11340	81
ADS902	10	30	5	130	Ext	FAX*LINE* 11359	82
ADS930	8	30	3/5	66 @ 3V	Int	FAX*LINE* 11348	83
ADS931	8	30	3/5	63 @ 3V	Ext	FAX*LINE* 11349	84

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essary functions and features for the whole DVD data processing section. Both provide Constant Angular Velocity (CAV or lock-to-disk playback), pseudo-Constant Linear Velocity (CLV), and standard CLV modes. In CAV and CLV modes, a multimedia feature allows audio playback without the need to change disk speed.

The SAA7335 DVD-CD decoder/DSP is compatible with a DVD-CD systems such as DVD-ROM, CD-i, CD-ROM, and Video CD. Featured on its chip is an analog-to-digital converter (ADC) and a channel equalizer, as well as a dual-pass error correction unit. It also supports MPEG-based applications and has several motor-control options. For DVD de-interleaving, the decoder/DSP uses 32 kbytes of external SRAM. It has an integrated IDE (ATAPI) interface with automatic packet command sequencer and does not require any additional drivers to connect to the host PC. By using the implemented UDMA interfaces, it can be connected to standard SCSI drives. Real-time error detection and correction also are included on the chip, and the SAA7381 can operate with between 0.5 and 16 Mbytes of DRAM.

Chip Sets: Can't Have Just One

Advanced Micro Devices (AMD), Inc., Sunnyvale, Calif., announced its 640 chip set, a system solution for socket 7-compatible processors including AMD's K6 MMX processor and the K5 processor. The chip set includes the 640 system controller and the 645 peripheral bus controller. The 645 device features Ultra DMA/33 for the ATA/IDE interface providing a 33 Mbits/s high-speed transfer rate with added CRC to ensure integrity of data transfer, allowing swift execution of multimedia applications.

The new chip set's integrated DRAM controller supports up to six 64-bit banks of FPM, EDO, or SDRAM with optional ECC to ensure data integrity. A single design can be configured with different memory technologies and capacities to address the price/performance ratios of the high-performance multimedia home PC, robust mission-critical commercial PC, or low-cost PC.

SGS-Thomson Microelectronics NV, Saint Genis, France, exhibited its PC-on-a-chip. The ST PC consumer chip is a monolithically-integrated solution consisting of a 486-CPU core along with graphics and video controller, a PCI local bus controller, and core logic functions such as interrupt, I/O, DMA, and ISA bus. The device's performance is comparable with the performance of a typical P90 level system. In addition to the fully-static 32-bit x86 processor, the chip contains a 64-bit local bus interface running at 66 MHz, a 64-bit windows accelerator that is VGA-compatible, and a 64-bit DRAM controller for both graphics and system memory.

The chip comprises a standard PC chip set peripheral controller, an ISA bus controller with selectable ISA clock, and a PCI 2.1-compliant controller with master/slave and arbitration functionality. In addition, an IDE controller including bus master with scatter/gather capability and multiword DMA support for fast IDE drives is integrated on the chip. An NTSC/PAL encoder and a VIP interface also are included in the 368-pin ball grid array package.

Texas Instruments (TI), Dallas, displayed their new PCI bus products. For very demanding multimedia applications in notebooks, TI has announced the 130+-Mbyte/s line of CardBus controllers that approach the 132 Mbytes/second limit of the PCI bus used in most PCs.

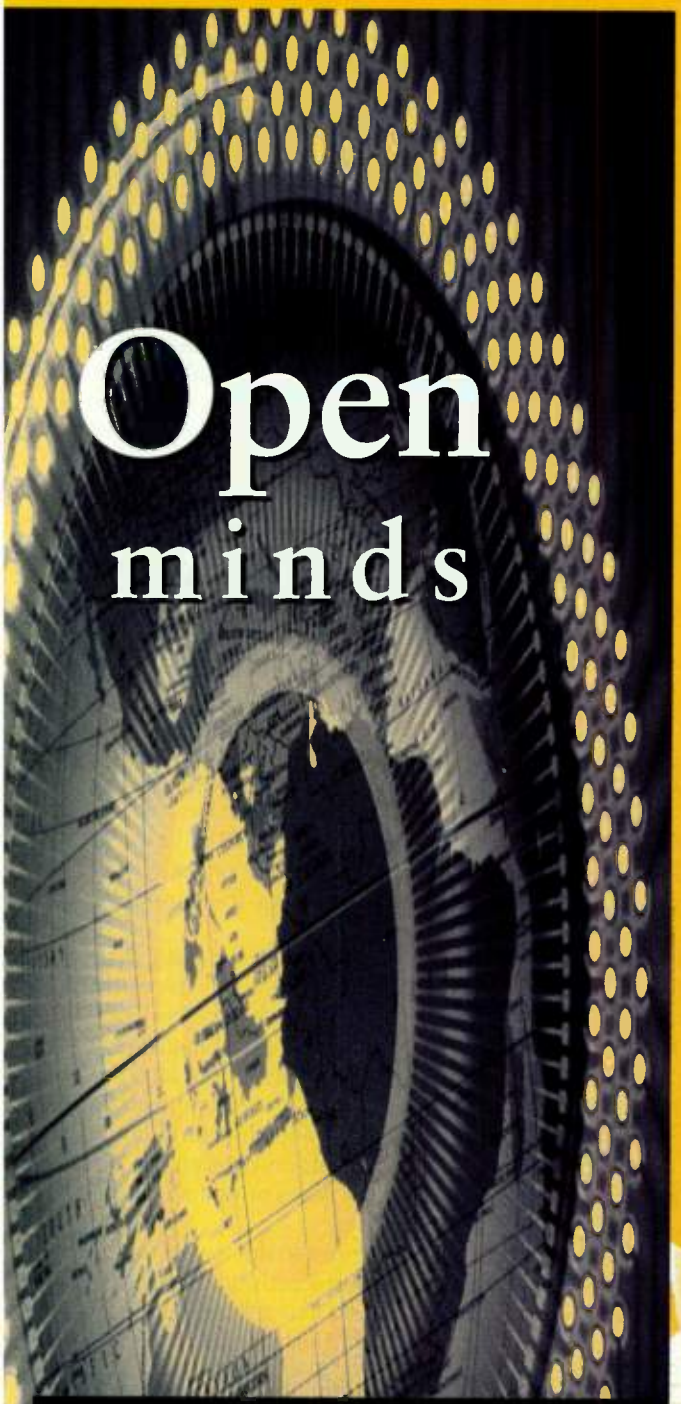
This increase in performance to nearly three times the speed of CardBus controllers allows users to run applications such as a high-speed network and video processing simultaneously. The new family of CardBus controllers, designated as the PCI12 series, was designed to meet the needs of systems complying with the Microsoft PC 97 hardware design guidelines including the ACPI (Advanced Configuration Power Interface) requirement. The PCI1250 allows Windows operating systems to conserve battery life by powering down the CardBus controller when not in use and shutting down circuitry when a CardBus or PC Card is not inserted. The PCI12 series works with either a 3.3- or 5-V bus system.

Another new IC from Texas Instruments is the PCI2030 device, which interfaces two 32 bit PCI buses. In systems requiring more than four PCI slots, one or more additional PCI buses are required which can be provided by a PCI-to-PCI bridge. The PCI2030 supports the full 132 Mbytes/s transfer rate of the PCI bus and is compatible with either 3.3- or 5-V PCI signaling environments. It implements the same FIFO architecture as other PCI interface chips from TI. Besides complying with the current versions of the PCI specification (Version 2.1) and the PCI-to-PCI bridge specification (1.0), the PCI2030 offers a number of additional capabilities.

One such feature simplifies the configuration of complex PCI-based systems by supporting both logical and physical location addresses. The PCI2030 also provides two additional programmable address decode windows that exceed the address granularity requirements specified by the PCI and PCI-to-PCI bridge specifications. System designers can use these decode windows to implement memory and I/O addressing schemes featuring much greater precision than those offered by standard PCI systems. These additional address decode windows can be beneficial for programming memory and I/O windows for notebook PC docking stations and PCI add-in cards.

With a feature known as subtractive decoding, PCI systems can accommodate older ISA-based boards or devices. Normally, PCI-based systems have difficulties handling ISA devices because the system's plug-and-play software will not assign addresses to ISA devices. Any ISA address issued on the primary PCI bus would go unclaimed if the targeted ISA device is located on the secondary or other lower-level PCI bus. The PCI2030 eliminates this problem by automatically forwarding unclaimed addresses to successive PCI buses until the ISA device is found.

According to Analog Devices, Norwood, Mass., the ADAM 200 digital telephony hardware and software reference design offers the possibility to develop a feature telephone with an integrated scalable digital answering machine, caller ID, and full-duplex speakerphone at a low cost. Based on a fixed-point DSP core, the ADAM 200 architecture offers a components bill-of-materials of under $22.



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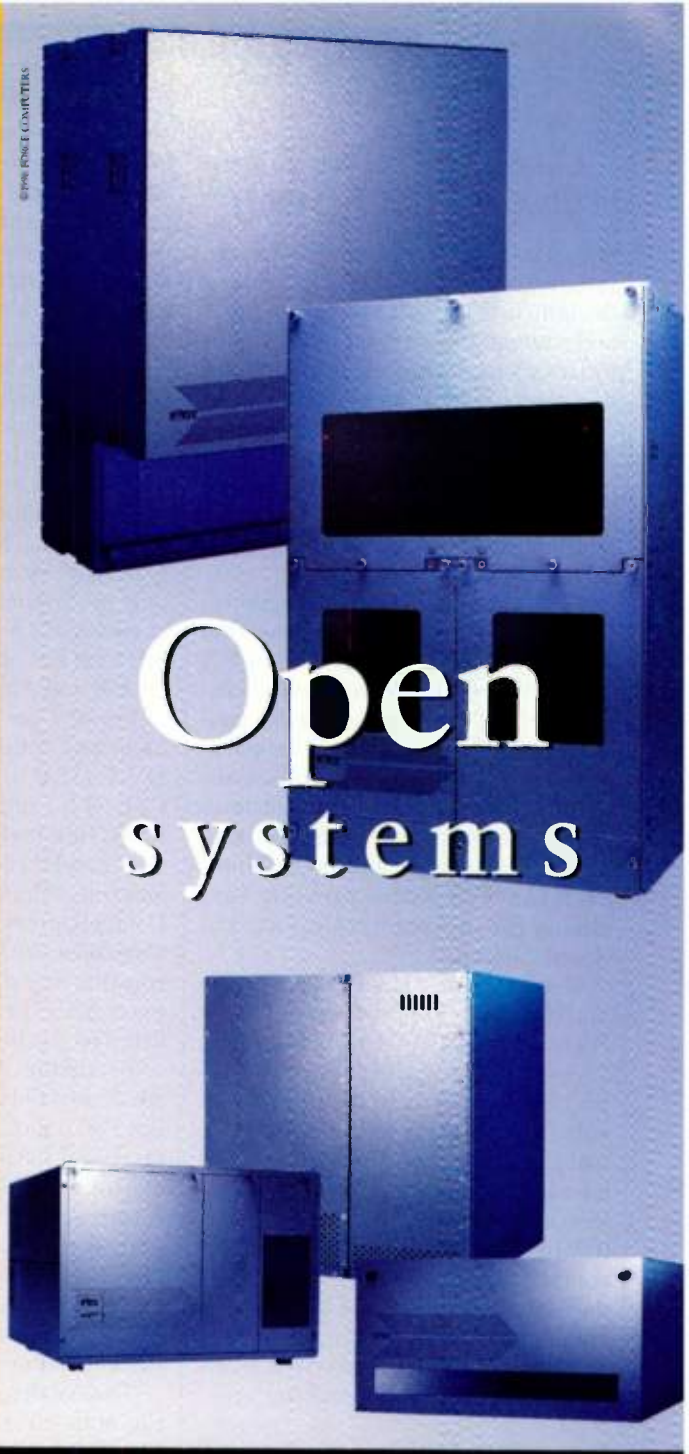


READER SERVICE 122

Analog Devices also is active in the GPS (global positioning system) receiver business. The company displayed its reference design for system integrators and OEMs.The receiver designs include software correlator and navigation processors to compute the user's position, velocity, and time to a position with accuracy of better than 30 meters without S/A (selective availability). Both eight-channel parallel receivers are reprogrammable and form a complete GPS receiver by adding a standard RF front end and GPS antenna.

ITT Intermetall GmbH, Freiburg, Germany featured its new Video Pixel Decoders VPX 3225D and VPX 3224D, which are the second generation of video-acquisition ICs for consumer video and multimedia applications. All of the processing necessary to convert an analog video signal into a digital component stream are integrated into a single 44-pin IC. Moreover, the VPX 3225D provides text slicing for intercast, teletext, and closed-caption.

For example, these chips provide multistandard color decoding for NTSC-M, NTSC-443, PAL-BGHI, PAL-M, PAL-N, PAL-60, SECAM ,and S-VHS. On the chip are two 8-bit video ADCs with clamping and automatic gain control (AGC), as well as four analog inputs with integrated selector for 3 composite video sources (CVBS), 2 Y/S sources (S-VHS), or 2 composite video sources for all standards. Information about the intercast standard, which is entirely supported by this chip, can be found on the Internet at *http://www.intercast.org*.

Proper Modulation

A multistandard modulator compatible with all world standards, including PAL, NTSC, and SECAM, has been announced by the Semiconductor Group of Siemens AG, Munich, Germany. The TDA 6060XS combines the functions of a digitally programmable PLL with a multistandard video modulator and a programmable sound FM and AM modulator.

The new IC is suitable for all modulator boxes such as those used for video recorders, games, satellite receivers, and set-top boxes. The PLL permits the frequency of the modulator oscillator to be set from 30 MHz to 950 MHz in increments of 250 kHz, while tuning is controlled by a microprocessor via an I^2C bus. The internal reference frequency is 62.5 kHz and the modulator block includes a gain-adjustable video amplifier, a double-balanced mixer working as AM video modulator, a frequency and amplitude-stable balanced oscillator for the VHF, hyperband and UHF range, a sound modulator for FM and AM modulation, a programmable sound carrier oscillator, and a reference voltage source. The sound carriers are generated by an oscillator that is digitally programmable on the chip to frequencies of 4.5 MHz, 5.5 MHz ,and 6.0 MHz for FM only, as well as 6.5 MHz for FM and AM.

For low-cost passive ISDN cards, Siemens Semiconductors launched its IPAC (ISDN PC Adapter Circuit, PSB 2115) single-chip solution. The IPAC integrates an S0 ISDN transceiver and three HDLC controllers. It integrates the PSB 2186 ISDN Access Controller and the PSB 82525 HDLC Controller in a single chip and does not require any external components; even ASIC or PAL modules for addressing can be omitted.

In addition, the PSB 2115 opens up whole new fields of applications. When the B channel FIFO buffer is configured with 128 Mbytes, it supports new chip applications featuring USB, the future serial PC port. An additional port for B channel data replaces the switching network in applications involving more than one S0 port which allows to transfer six B channels via the PCM interface.

To save designers time and money, Siemens offers the reference board SIPB 72115 used to develop a passive ISDN PC card based on the IPAC. In addition to the complete hardware data (circuit diagram etc.) it incorporates a full software package including the D channel protocols for DSS1 (Euro ISDN), NI-1 (U.S.), SESS (U.S.), and NIS (Japan).

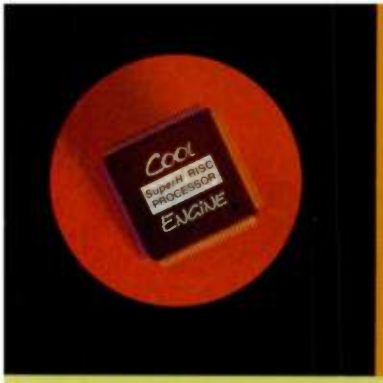
Another method of integration was chosen for ISDN line card controllers. Instead of integrating several existing one-chip U interface controllers into a single chip to reduce line card size, Siemens Semiconductors decided to split-up the U interface again into an Analog Front End (AFE) and a Digital Front End (DFE) which together form the UK0 interface. Due to the different process technologies used for AFE and DFE, a higher level of integration was achieved by splitting up and integrating several digital components on one chip, and several analog components on another separate chip, even though just a few years ago, the monolithic integration of an entire U interface (analog and digital elements together) in a single chip was introduced by Siemens. A chip set consisting of one AFE and one DFE, both of which come in an MQFP-64 package, can handle four U interfaces.

The DFE device is available in two pin-compatible versions: DFE-Q (PEB 24911) for the 2B1Q line code, and DFE-T (PEB 24901) for the 4B3T line code. For example, the DFE-T offers full duplex transmission and reception of the UK0 interface signals according to the FTZ guideline 1TR220 of Deutsche Telekom, who has already installed more than two million basic rate access ISDN lines. For use in the U.S., Japan, or many other countries, the plug-in-compatible DFE-Q is available.

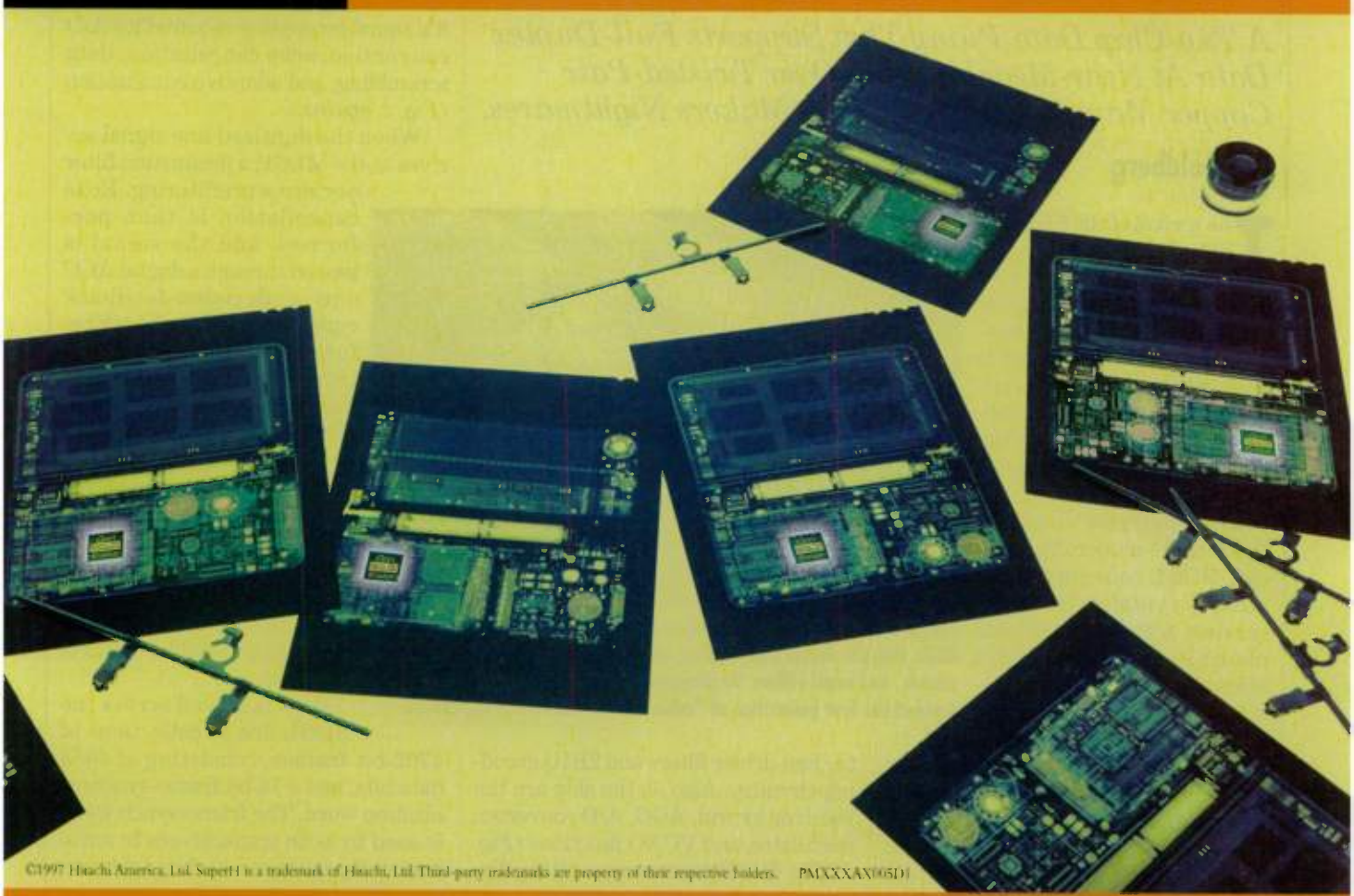
The DFE-T transmits data with a user bit rate of 144 kbit/s over standard local telephone loops. However, it also has a 1 kbit/s maintenance channel for transmission of data loop back commands and detected transmission errors. The subscriber loop length without a repeater ranges up to 4.2 km with 0.4-mm^2 wires or up to 8.0 km on 0.6-mm^2 wires.

Featured in the device are a number of communications utilities: an adaptive echo cancellation, an adaptive equalization, automatic polarity adaption, and clock recovery unit for frame and bit synchronization. It also provides for the transition of ternery to binary data and vice versa by applying coding, decoding, scrambling, descrambling, and phase adaption techniques. A built-in wake-up unit for activation from power-down state is implemented as well. For testing purposes (loop 1 in LT), an analog test loop at the UK0 interface may be switched.

How Valuable	Circle
Highly	545
Moderately	546
Slightly	547



Five out of seven Windows® CE Handheld PCs share the same inside secret.



The Hitachi SuperH RISC Cool Engine. The de facto standard for Windows CE Handheld Personal Computers.

The electronics revolution is headed off the desktop and out into the world at large. Case in point: the Windows CE Handheld Personal Computer (H/PC).

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If you're looking closely at Personal Access CPUs, we think there's a good chance the SuperH RISC processor is going to be in your picture, just like it is for the new H/PCs from Casio, Compaq, Hewlett-Packard, Hitachi and LG Electronics.

You can get the inside scoop at 1-800-446-8341, ext. 1000. Or visit our web site at **www.hitachi.com.**

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A TOTALLY NEW VISION

MDSL Chips Lay The Cornerstone For Cost-Effective Broadband Access

A Two-Chip Data Pump That Supports Full-Duplex Data At Near-Megabit Rates Over Twisted-Pair Copper May Give Cable Modem Makers Nightmares.

Lee Goldberg

The arrival of the SK7072x chip set may be giving the cable modem industry more than a few sleepless nights. This highly integrated data pump chip set is designed to make a wide variety of multi-rate, digital-subscriber-loop (MDSL) applications simple and inexpensive to implement.

Vastly superior to conventional cable-modem technology, MDSL delivers full-duplex, symmetric data services across twisted-pair phone lines at rates of 272 kbits/s to 784 kbits/s. Transmission distances of up to 22,000 ft. mean that MDSL can reach homes and small offices over existing local loops, without special line conditioning. Using POTS splitting technology (adding an RF splitter to the line to separate traffic), it is possible to maintain normal voice service while simultaneously using the same lines for data transmission.

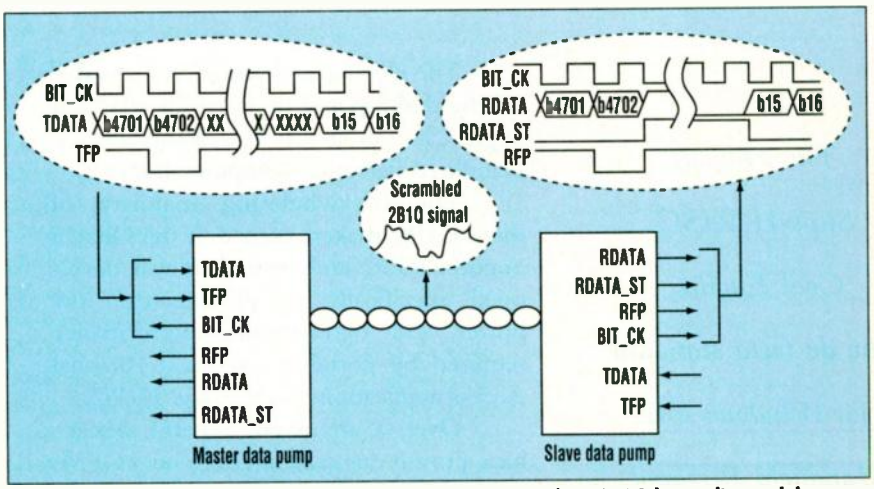
Now, a two-chip set, consisting of the SK70720 MDSL DSP (MDSP) and the SK70721 integrated-analog front-end (IAFE), can make inexpensive MDSL equipment a reality, both on the subscriber-side, and in the central office. Together, the chips form a complete, variable-rate transceiver that provides full-duplex communication on two wires using echo-canceller-with-hybrid and 2B1Q line coding technology *(Fig. 1)*. For most applications, the data pump does not require a microprocessor to control it, reducing both development time and production cost.

The IFAE is a fully integrated front-end IC which includes transmitter line-driver filters and 2B1Q encoding circuitry. Also on the chip are the receiver hybrid, AGC, A/D converter, modulator, and VCXO functions *(Fig. 2)*. The MDSP incorporates all the digital signal processing required for A/D conversion, echo cancellation, data scrambling, and adaptive equalization *(Fig. 2, again)*.

When the digitized line signal arrives at the MDSP, a decimation filter performs prefiltering. Echo cancellation is then performed, and the signal is passed through a digital AGC and a decision-feedback equalizer (DFE) network before the data signal is extracted and passed to the host system. When not processing signals at a furious rate, the MDSP is pressed into service as a transceiver controller. This design eliminates the need for using the host system or a separate controller chip to perform transceiver activation and other state-machine control functions.

Data is moved across the MDSL line as collections of 4702-bit frames, consisting of 4688 data bits, and a 14-bit frame-synchronization word. The frame-synch word is used by both transceivers to automatically activate and deactivate

Whether it's Web surfing, distance learning, or telecommuting, this MDSL chip set delivers full-duplex, near-megabit bandwidth to homes, schools, and small offices. By dropping the cost of MDSL, Level One has enabled the first generation of "cable killer" information appliances.



1. Level One's two-chip multi-rate DSL data pump (MDP) employs 2B1Q line coding and data scrambling to produce a signal that's robust enough to carry high-rate data across twisted-pair phone lines for up to 22,000 feet. The incoming data stream is broken down into 4688-bit-long frames, with a 14-bit frame synchronization header appended to it.

Fig. 1

While other digital scopes are in this mode 99.9935% of the time,

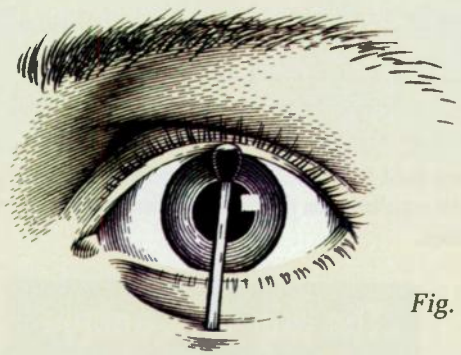
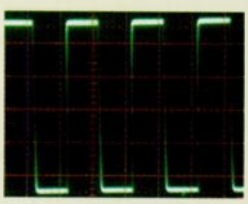


Fig. 2

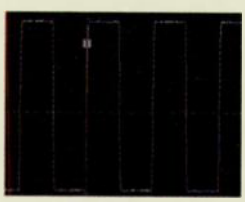
the InstaVu™ family is wide awake.



Analog

If you think your digital scope is giving you a live, real-time picture of your waveform, it's time to wake up.

Most digital scopes acquire a few hundred waveforms or so a second, missing all the rest. So you could miss an infrequent glitch simply because your scope is "blind" when it happens.



Conventional DSO

Not with the InstaVu™ acquisition family from Tektronix, though.

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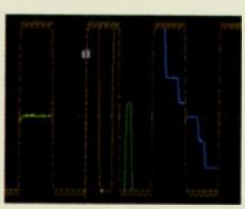
What's even more powerful about Tektronix InstaVu acquisition scopes is that they now start at under $10,000. So, for the price of other DSOs, you can get one that's several orders of magnitude faster and more accurate.

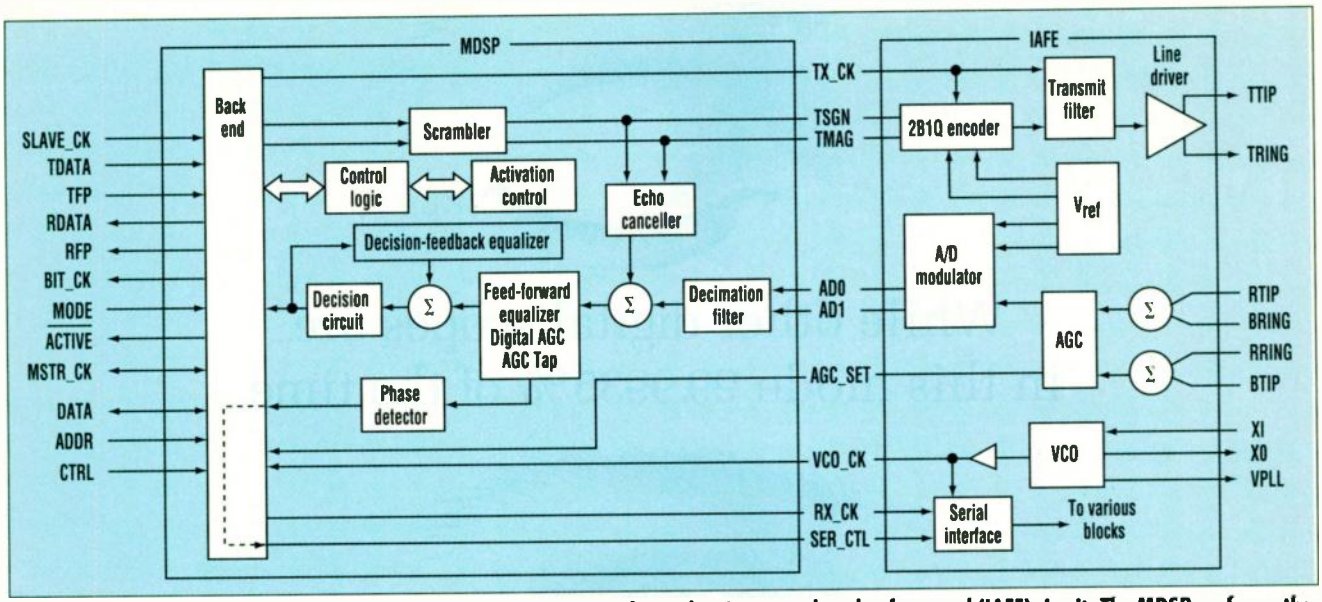
Call 1-800-426-2200 (code 500) for more information on the InstaVu acquisition family, or visit our Web site at www.tek.com. And open your eyes to a new standard in digital oscilloscopes.



InstaVu™

	TDS520B	TDS540B	TDS724A	TDS754A	TDS784A
Bandwidth	500 MHz	500 MHz	500 MHz	500 MHz	1 GHz
Channels	2 + 2	4	2 + 2	4	4
Max. Sample Rate	1 GS/s	2 GS/s	1 GS/s	2 GS/s	4 GS/s
Max. Record Length	250K	500K	250K	500K	500K
Max. Wfm. Acquisition Rate	100,000 Wfm/s	100,000 Wfm/s	180,000 Wfm/s	400,000 Wfm/s	400,000 Wfm/s
Display	Monochrome	Monochrome	Color	Color	Color

Tektronix



2. The MDSL transceiver consists of a specialized MDSL DSP (MDSP) chip and an integrated analog front-end (IAFE) circuit. The MDSP performs the data scrambling, adaptive equalization, and echo cancellation on the digitized signal, and extracts a bit stream. The IAFE performs all the line-interface, encoding, and clock-generation functions.

themselves upon the beginning and end of a transmission. The MDSP's frame is completely transparent to the data, and permits transport of both unframed, time-division multiplexed data, or data streams with their own framing information.

The overall performance of the transceiver is impressive, with 784-kbit/s rates possible for distances of up to 17,000 ft. on 24 AWG cable (12,800 ft. over 26 AWG). Rates of 272 kbits/s are possible for 22,000 ft. on 24 AWG or 16,000 ft. over 26 AWG. While not as high as the multimegabit downstream rates achieved by asymmetric digital-subscriber-line (ADSL) technologies, MDSL uses a much simpler line-coding scheme and offers a fully symmetric data path.

This bandwidth symmetry is less critical for downstream-intensive applications such as web browsing and video downloads, but quite necessary for small office/home office (SOHO) environments. Tasks like video-conferencing, high-speed file transfers, and remote LAN access all benefit from symmetric, near-megabit data rates. Equally important in telecom applications, is that the power consumption is low. Depending upon the data rate at which it's operating, the chip set draws between 500 and 900 mW from a single 5 V supply. This feature makes it a good candidate for line-powered applications.

The chip set's unique ability to adjust its line rate enables it to automatically adapt to variations in line conditions.

The chip set's ability to adjust its line rate enables it to adapt to variations in line conditions. This adjustment can be performed automatically, with the transceivers on each end negotiating with each other, or, if desired, the rate can be set by an external controller. Some applications require that data be transported at an externally controlled rate that varies little from a nominal payload rate. The MDSP has a variable-rate operating mode that allows the variations—specially marked dummy bytes are stuffed, as needed, to fill a packet frame.

A complete development kit is available for the SK70720 and SK70721 chips. The kit includes two transceivers and all components necessary to activate an MDSL link without external hardware or software. It can be used to evaluate the chip's performance, or begin prototype work on an MDSL product. The evaluation board is comprised of two printed-circuit boards that mate together with PGA connectors. The motherboard provides clock, oscillator, power supply, and signal connectors. The data pump daughter card contains both transceiver chip sets, and is configured for one of the specified line card rates. Daughter cards are available for operation at 272-, 400-, 528-, and 784-kbits/s.

The board allows bit-error rate measurement with fixed data patterns to facilitate transmission reach and noise margin testing using a twisted-pair line or loop emulator. It also supports the chip set test modes for transmit pulse template, output power, and power spectral density measurements.

Price And Availability

The MDSL chip set, consisting of the SK70720 MDSP and the SK70721 IAFE are available now, in full production. Packaged in 44-pin and 28-pin PLCCs respectively, the chip set sells for under $20, in OEM quantities.

Level One Communications Inc., 9750 Goethe Rd., Sacramento, CA 95287; contact Kate Soleil, (916) 855-5000, ext. 4743; e-mail: kates@level1.com. **CIRCLE 541**

How Valuable	Circle
Highly	542
Moderately	543
Slightly	544

PRODUCT FEATURE

Data sheets on products like these can be found at www.penton.com/ed/

Video Scaling Processor Delivers Independent H, V, Zoom Ratios

Avoiding the need for external memory, the gmZ1 video-scaling processor provides a single-chip, zoom-only solution that offers programmable horizontal and vertical front and back porches on the input data. Designers can use the chip to create systems with fully-programmable zoom ratios with high quality levels, because it includes both horizontal and vertical filtering. In addition, the chip performs spatial de-interlacing of the video inputs (even and odd input lines are correctly spatially positioned in the output frame).

Applications of the gmZ1 include video-compression cards, video walls, standards-conversion equipment, multisync LCD panels for CRT replacement, projection display systems, home theaters, and other display-based systems. The chip, developed jointly with Apple Computer Inc., Cupertino, Calif., for Apple's multimedia systems, also includes a display timing generator. The generator can drive active-matrix LCD panels or the digital micromirror display engines developed by Texas Instruments—all with minimal off-chip support logic. On-chip spatial line doubling provides conversion from NTSC/PAL video to line-doubled progressive-scan video.

Timing parameters are fully programmable and dithering logic on the chip helps enhance the pixel color depth for 18-bit panels. However, the chip can support panels with up to 24 bits/pixel. Furthermore, the chip supports 16-bit YUV input video and delivers NTSC/PAL square pixels for CCIR601 compatibility. The circuit provides a glueless interface to Philips SAA7110/7111 color decoders and converts YUV signals to RGB. Also, RGB can be used as an input to the chip—24-bit RGB pixel data can be accepted at clock rates of up to 84 MHz, or a 48-bit RGB data stream can be handled at data rates of 42 MHz. On the output side, the chip delivers either a 24-bit RGB data stream at 84 MHz or a dual 48-bit RGB data stream at 42 MHz.

Samples of the gmZ1 are immediately available. In OEM quantities, the chip sells for $55 each.

Genesis Microchip
2071 Landings Dr.
Mountain View, CA 94043
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CIRCLE 460

DAVE BURSKY

PRODUCT FEATURE

Data sheets on products like these can be found at www.penton.com/ed/

Hardware Reference Design Kit Simplifies Concurrent Software Development

Wireless data networking products with capacities of up to 4 Mbits/s can be quickly and efficiently developed using the WLANKITPR1-EVAL, a complete reference design and hardware platform. The kit is based on the PRISM WLAN chip set. a highly integrated 2.4 GHz, spread-spectrum data transceiver. The kit is intended to help OEM's concurrently develop device drivers, application software, and hardware designs. It includes two FCC-approved, Type 2, PCMCIA wireless LAN (WLAN) cards with integral antennas, as well as driver and media-access-controller software with a pair of single-user licenses.

In addition, each kit features a suite of Windows-compatible diagnostic software for measurement and display of packet error rate and throughput. The WLANKITPR1-EVAL supports transmission distances of 300 feet indoors, and 3000 feet outdoors. Another evaluation kit, announced earlier this year, facilitates hardware

design by enabling RF designers to perform lab measurements on PRISM-based receivers. It provides uncovered circuit boards and RF antennas in lieu of antennas.

Operating at 2.4 GHz, the PRISM chip set uses direct-sequence spread-spectrum (DSSS) modulation to form wireless data connections that can be used as a LAN. It also suits bar-code scanners, security systems, point-of-sale-terminals, manufacturing control systems, and audio systems. It can operate on supply voltages ranging from 2.7 to 5.5 V.

Though the system is designed to accommodate the IEEE 802.11 wireless data standard, its software-oriented architecture doesn't dictate a particular media-access-control (MAC) protocol. This permits development of non-standard systems that are optimized for a particular application. In custom applications, the PRIZIM system can support data rates of up to 4 Mbits/s. The WLANKITPR1 -EVAL costs $995.

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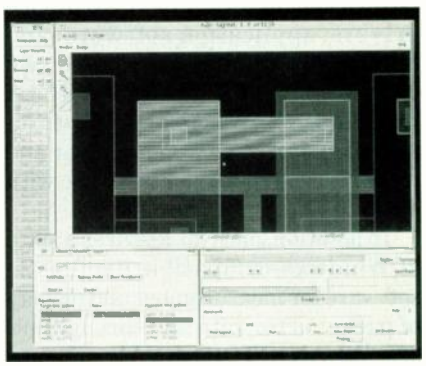
PRODUCT FEATURE

Data sheets on products like these can be found at www.penton.com/ed/

Extraction and Analysis Tools Target DSM Design Environment

When designing in true deep submicron (DSM) environments—0.25-µm geometries and below—the physics of component interactions within a device start to control the design process. Interconnect delays create gate delays, and increased height-to-width interconnect ratios lead to quick consumption of silicon real estate. To deal with these issues, designers must extract and analyze huge amounts of parasitic data, which can be a daunting task.

A new set of tools, Vampire RCX and ConcICe, address these issues by allowing designers to perform fast full chip hierarchical extraction and data reduction while maintaining a high level of accuracy. The first tool, Vampire RCX, an advanced 3D formula engine for extraction, has the ability to extract and view resistance and capacitance values for selected nets and paths in a given design. Its inherent flexibility allows designers to control the amount of accuracy versus runtime for a given extraction. Also, because



it's fully hierarchical, the tool can be scaled to the largest capacity design.

Vampire RCX identifies and probes for RC elements, such as cross-coupling capacitances, and area and fringe capacitances, from critical nets. The extraction is based on equations and criteria defined and specified by the user. Once the extraction is complete, the extracted devices and connectivity for problem interconnects is displayed via an on-line integrated graphical display. All data is output in either Distributed Standard Parasitic Format (DSPF) or Spice format.

Coefficients and parasitic rules, used by the 3D formula engine, are automatically generated using coefficients generator technology. Although traditionally a manual process, automated generation of such information significantly decreases the derivation time from weeks to virtually minutes. Automatic coefficients and parasitic rules generation also succeeds in eliminating any error due to human intervention.

The technology works by soliciting input from the user on process-specific information, such as minimum widths and thicknesses. A predefined set of generic structures are run through a

(continued on page 62)

ELECTRONIC DESIGN QUICK LOOK

Edited by Mike Sciannamea and Debra Schiff

MARKET FACTS

Traffic Troubles ITS Market

Although it might make you feel better to honk the car horn when stuck in traffic, the answer really lies in the ability to prevent traffic back-ups. According to a recent study from Frost & Sullivan, "U.S. Intelligent Transportation Systems Market," not only is the problem of traffic congestion at an all time high, but it's adding to the monumental issues of gas wastage and increasing air pollution. One new set of technologies intended to change the face of gridlock as we've come to know it is intelligent transportation systems (ITS). The U.S. government has defined the five segments of intelligent transportation systems as: Advanced Public Transportation Systems (APTS), Advanced Traffic Management Systems (ATMS), Advanced Traveler Information Systems (ATIS), Advanced Vehicle Control Systems (AVCS), and Commercial Vehicle Operations (CVO). For the most part, the government's participation in intelligent traffic systems only falls in the APTS, ATMS, and CVO segments. The Department of Transportation supports this market by direct funding of ITS programs, research, and state projects. Legislation that supports the direction of ITS also is managed by the Department of Transportation. Among the states who have actively involved Transportation Departments are California, Georgia, Kentucky, New York, and Oregon. In private industry, the main end-users of ITS are fleet operators, delivery services, independent paratransit operators, private security services, shipping services, and shuttle and taxi services. The new report projects that the APTS market will maintain a steady growth pace throughout 2002. The growth is attributed to the market's historical success, and results seen in the adoption of this service in the public sector. Frost & Sullivan asserts that every public transit agency that has adopted ITS technologies has reported significant gains in efficiency. Potential growth also lies in the private sector. The combined effects of congestion, pollution, and rising costs associated with automobile and road maintenance, are expected to increase, thus sending more private investors to find new options for transportation alternatives—mainly APTS. The report also contends that the biggest trend in ITS is to develop a system that monitors more roadways and uses less equipment. Of course, the real goal is to accomplish this task while spending less money. Two ideas that have been examined are monitoring toll tags and cellular phone signals to statistically determine traffic flow. The early stages of ATMS will be concentrated on establishing traffic management centers and installing roadway sensors. Typically, the cost for installing roadway sensors is $200,000 per mile for the new roads, and $1,000,000 per mile for retrofitting. Other points of potential growth are closed-circuit television cameras, automated toll and parking systems, and variable message signs. One sector of the market is already a viable presence, but it has two major barriers to mass acceptance. ATIS consists of autonomous systems and advisory systems. The autonomous systems operate independently, unlike the advisory systems that require real-time data input to find the best possible route for the driver. Advisory systems also are tied to a standardized communications infrastructure. The structure comprises communication links that are either infrared or RF signals, which are geographically defined. AVCS is based on collision warning systems and intelligent cruise control systems. Also found in this segment are pedestrian detection systems and vision enhancements. CVO owes much of its success to the trucking industry, primarily its complex communications methods.

For more information, contact Frost & Sullivan, 2525 Charleston Rd., Mountain View, CA 94043; (415) 961-9000; fax (415) 961-5042.—*DS*

Percentage Of Projected Revenues By System

40 YEARS AGO IN ELECTRONIC DESIGN

Plug-In Transistor Amplifier

The Model 196 transistorized amplifier is a high gain, low-power, plug-in type amplifier designed for servo and audio applications. The unique feature of this amplifier is its gain stability over a range of operating temperatures from -55 to +55 C. This stable gain is achieved through dc feedback to stabilize the operating point, and ac feedback to achieve broad band-width, high input impedance and good wave form. Two models are available: Model 196 shown above is equipped with germanium transistors, suitable for environmental temperature from -55 C to +55 C, and Model 198 using silicon transistors for temperatures from -60 to +125 C. Taber Instrument Corp., 111 Goundry St., N. Tonawanda, NY. *(Electronic Design, May 1, 1957, p. 46)*

This brief piece is rather sparsely populated with details, but it does reflect the state of the art of the time: Transistor amplifier modules in production.—SS

Tubes, Even Transistors, Obsolete

At the International Symposium on the Theory of Switching, Harvard University, several predictions were made concerning the future of tubes and transistors in large scale computers. Dr. Theodore H. Bonn of the Remington Rand Div. of Sperry Rand saw the vacuum tube as obsolete for computers now being designed by the newer transistors and magnetic amplifiers. A second speaker, Dr. Herbert Callen, looked even further into the future and foresaw the eventual decline of the transistor in favor of new ferromagnetic films, which will carry the speed of switching to as little as one-billionth of a second. Dr. Callen predicted a time when the upper limit of computing speed would be limited only by the time necessary for a pulse to travel from one point in a computer to another. The thin ferromagnetic film switch is theoretically capable of this speed, equal to the speed of light. *(Electronic Design, May 15, 1957, p. 7)*

Dr. Bonn was proven correct, but did he foresee the tremendous advances in VLSI circuitry? As for Dr. Callen: who knows? He could be right after all.—SS

Skeptical of Computer Advantages

Present day electronic equipment for data processing is not suited to the needs of all but a few giant retail organizations and many of these are skeptical of the vaunted advantages, according to Milton Woll, Research Director of the Retail Research Institute of National Retail Dry Goods Association.

Of the basis of a study of data processing equipment of member stores of the NRDGA, Mr. Woll pointed out that most retailers were not yet using mechanical tabulating equipment let alone electronic. Although there is a great interest among retailers in all parts of the country in the development of automatic data processing equipment, most store managements feel that the cost of the equipment available is much too high to justify its installation.

Mr. Woll was critical also of the grandiose approach to electronic applications and indicated his preference for a gradual and experimental type of approach. He expressed conviction that the step-by-step licking of one problem after another is the only way to make progress in adjusting to the tremendous procedural rigidity of data processing. *(Electronic Design, May 1, 1957, p.11)*

It may appear that Mr. Woll was being over-conservative. However, the early history of computers is studded with grandiose claims and unfulfilled promises, but seeing it from our current perspective, he wasn't far off.—SS

THE ENVELOPE, PLEASE

In recognizing the outstanding accomplishments of professionals in the management science and operations research fields, the award to follow is the Franz Edelman Award for Achievement in Management Science and Operations Research. Dr. Franz Edelman, one of the forefathers of management science, was responsible for management sciences activities at RCA. RCA has one of the oldest industrial operations research and management sciences departments in North America.

This year's award carries a $10,000 first place award, in addition to $5000 in other prizes. The 26th annual international competition is sponsored by the Institute for Operations Research and Management Sciences, and its practice section, the College for the Practice of the Management Sciences.

One of the finalists of this year's competition is William Swart, the dean of the Newark College of Engineering at the New Jersey Institute of Technology (NJIT). Jackie Hueter and Swart authored, "An Integrated Labor Management System for Fast Food Operations." Hueter is the director of restaurant systems engineering at Taco Bell.

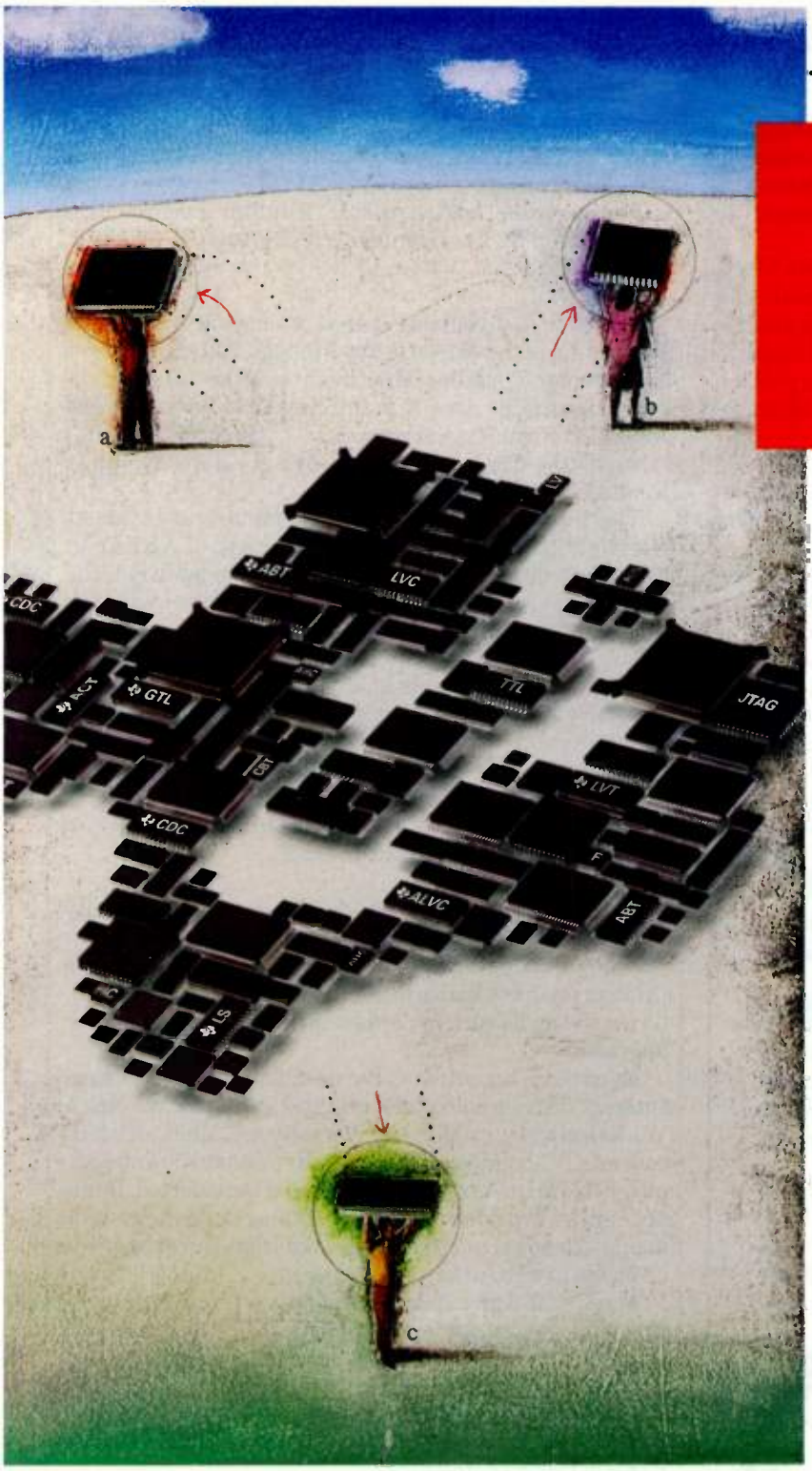
The study looks at operations models used to develop a new Labor Management System for the Taco Bell Corporation. The new system yielded a savings of over $43 million since 1993. Additionally, cost savings from the new management system have provided an increase of 20% or more in sales and earnings for each year through 1995.

A past recipient of the Franz Edelman Award, Swart has been the Newark College of Engineering dean and professor of industrial and manufacturing engineering at NJIT since 1994. Prior to his tenure at NJIT, Swart chaired the Department of Industrial Engineering and Management Systems at the University of Central Florida.

For more information, contact NJIT, University Heights, Newark NJ 07102-1982; (201) 596-3434; fax (201) 642-4380; Internet: http://www.njit.edu./News/news.html.

—DS

A D V A N C E D S Y S T E M L O G I C



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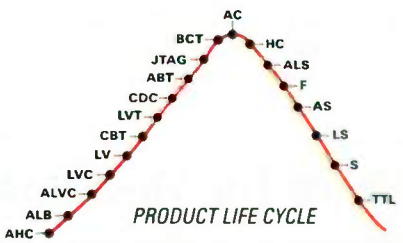

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TEXAS INSTRUMENTS

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INTERNET NEWS

One of the more interesting phenomena of the Internet is the on-line classroom. People in Idaho graduating from Alaska University on-line are becoming less uncommon than ever. Another important innovation of on-line education is the development of the specialized virtual classroom.

One company, EduSoft Ltd, has launched its Virtual Classroom, featuring 43 courses in mathematics and physics. These courses are aimed at junior high and high school students, but individual home users also could find some of the courses useful. All of the interactive problem-solving sessions are offered in English and Spanish, and are free to the public.

The mathematics courses consist of seven subjects, 22 courses, and over 200 interactive sessions. Subjects covered are Algebra, Pre- and Basic Algebra, Arithmetic, Geometry, Probability, Statistics, and Trigonometry.

The physics courses cover Electrical, Fluid, Mechanical, and Thermal systems, as well as Optics and Acoustics. The physics arm of studies has 21 courses and over 200 interactive sessions.

Future plans for EduSoft include adding a connectivity feature to the company's English Discoveries CD-ROM program in order to connect to the Virtual Classroom site. Users would then be able to access updated material, additional games, workbooks, and chat groups. Eventually, the site will evolve into a Virtual Campus, providing real-time Distant Learning sessions to schools and individuals.

For more information, contact EduStar America Inc., 590 Herndon Pkwy., Herndon, VA 20170; (703) 708-9250; fax (703) 708-9255.

If you ever find yourself in need of some facts about the evolution of the Internet, try Find/SVP's U.S. Internet Consumer Timeline. The timeline is the result of research from "The American Internet User Survey," "The American Financial Services Survey," and other studies taken by the Emerging Technologies Research Group at Find/SVP.

The timeline lists a number of historical Internet Highlights, beginning from the 1969 birth of ARPANet to Apple's dumping of eWorld in 1996. In addition, the timeline projects what the face of the Internet will look like over the next three years.

Market shares are measured for Internet browsers and modem speeds. Projections are given for the types of technologies and tools that will be used, as well as user trends.

For more information on the Internet Timeline, contact Find/SVP, 625 Avenue of the Americas, New York, NY 10011; (212) 645-4500; fax (212) 645-7681; Internet: http://www.etrg.findsvp.com/ timeline.

The nature of catalog publishing has dramatically changed with the advent of the World Wide Web. Nowadays, companies that do most of their business through products that are described in catalogs use the Internet to handle such important issues as price changes or upgrades.

Even more important is the distribution of the catalog. Internet distribution is infinite. Prostar Interactive Media Works has a new catalog-building software, MiniCat, which converts PC-created catalogs into Hypertext Markup Language (HTML). As soon as the material is converted, Internet Service Providers can put the catalog up on the system, making the electronic version of the catalog will be made available to web surfers everywhere.

MiniCat also gives users the ability to transfer their entire catalogs to a single self-running disk. After receiving an electronic catalog, a customer can print out selected pages of the catalog, and fax in their order from the catalog. The photos are resizable, enabling greater detail. MiniCat allows users to store more than 200 photos and hundreds of pages of text on a single disk.

Electronic publishing has now emerged as a proven way to cut costs dramatically. One of the biggest costs that catalog businesses have to absorb is reprinting an already expensive (and existing) catalog simply because the prices have changed.

For additional information on MiniCat, contact Prostar Interactive, 13880 Mayfield Pl., Richmond, British Columbia, Canada V6V2E4; (800) 432-2949; Internet: http://www.minicat.com.

FLIPPING THROUGH THE INTERNET ROLODEX

http://www.vwww.com: Stop in at the Virtual World Wide Web (VWWW) to try out Viscape, the world's fastest 3D browser. VWWW comprises over 30 3D pages, with content such as an art gallery featuring a tribute to mathematical art, "Dancing Numbers" is a simulation area with training applications; meeting places, and virtual arcade games. In addition, the most popular areas of VWWW are the University, Exhibition and Shopping Mall. And for those looking for another way to get the attention of fellow surfers, VWWW is taking advertising. The site is maintained by Superscape Virtual Reality Software.

http://www.suppliersonline.com: Click here for a guide to the metals industry. AlloyTech has put together Metal Suppliers Online, a searchable database of the production capability and inventory of over 2200 North American metals producers and service centers. Visitors to the site can use the Find A Supplier search feature to look through an alphabetized listing or search by product. Suppliers can then be contacted with the site's Global E-mail option, or via the 250+ company links at the site for pricing or general information. There also is a comprehensive materials properties area, with over 5000 ferrous and non-metals described there.

http://www.ecliptek.com: Surf into Ecliptek's interactive web site, and check out their number generator. Information on standard and custom products, price and delivery, application notes, representative and distributors, as well as corporate information can be found here. The company's complete line of quality crystals, oscillators, and inductive products is described at the site. Detailed specification sheets also can be downloaded (they come in .pdf format, so be sure to download Adobe Acrobat ahead of time).

http://www.elect-spec.com: Now here's a site for inventors, small companies, and any other folks that are looking for some free exposure for their new products. The site is truly looking out for the new product that just might not see press or Internet publicity otherwise. It works by inventors or designers sending in their electronic, electrical, or electromechanical products that look like they've got market potential. The process is free, and the products need not have been offered for commercial sale previously. Submissions may include their own product descriptions, or may incorporate the services of Electronic Specialists to expose the product's best features and benefits. Photo touch-ups also are free.

UL-Certified Software

In response to the ever-expanding demand for certification, Underwriters Laboratories (UL) Inc. has now made available a certificate service for software-controlled products. The new service is in accordance with the Standard for Software in Programmable Components, UL 1998.

Because more manufacturers are using microprocessors and software to control their products, vendors and customers worldwide are increasingly asking for third-party reviews. These reviews look at performance and safety tests that the manufacturers conduct on their own software-driven product lines. But, more important than the reviews themselves, the software must meet internationally-recognized safety criteria.

With UL 1998, the reviews start early in the software design process, and continue through the development process. Like most quality control processes, the new standard is designed to catch safety issues early on through testing. The bottom line for most companies who are using this methodology for continuous testing throughout the process is meant to save additional costs and time.

The laboratory standard is well on its way to international acceptance, since it harmonizes with other internationally-recognized software safety standards. Standards in programmable industrial equipment safety are an important consideration in this changing marketplace, especially because acting preventively, rather than reactively, is quickly becoming the trend.

Covering risks for electrical shock, fire, and general injury, UL's Programmable Systems Certificate also authorizes companies to apply the UL Mark, which certifies that their products meet electrical and mechanical functioning safety standards. UL also performs certification services for companies who wish to meet ISO 9001.

For more information, contact Underwriters Laboratories Inc., 12 Laboratory Dr., P. O. Box 13995, Research Triangle Park, NC 27709-3995; (919) 549-1400; fax (919) 549-1842; e-mail: flyntj@ul.com.—*DS*

QUICKNEWS

Allied Telesyn has developed a family of fiber-optic-based Fast Ethernet adapter cards. The AT-2560FX adapters improve network responsiveness by raising throughput and lowering the drain on the CPU.

These cards feature the superior noise immunity of fiber, allowing them to serve network segments of up to 2 km. Using the full-duplex advantage, the adapters can receive and transmit data simultaneously, increasing throughput in switched and dedicated backbone environments.

The AT-2560FX series of cards supports the IEEE 802.3U 100Base-FX Ethernet-over-fiber specification. Using a self-configuration feature, they support such network operating systems as Windows NT, 95, and 3.x; Windows for Workgroups; Novell NetWare and Personal NetWare; Banyan Vines for client and server; DEC Pathworks; and IBM LAN server. Able to detect over 96% of the more than 5000 known computer viruses, McAfee's VirusScan software is included free with the adapter cards.

There are two versions of the AT-2560FX card: The AT-2560FX/ST which uses a twist-on connector for use with existing fiber-optic cable and connectors, and the AT-2560FX/SC which uses a push-on connector for new cable installations. Both are priced at $449 in single quantities and $8000 for counts of 20 cards. All units come with a lifetime guarantee and free technical support.

For more information, contact Allied Telesyn, 19015 N. Creek Pkwy., Bothell, WA 98011; (206) 481-3784; fax (206) 483-9458; Internet: http://www.alliedtelesyn.com.

Hitting the small office, home office (SOHO) market, Asanté Technologies has released its FriendlyNet line of 10Base-T hubs. The new plug-and-play Ethernet and Fast Ethernet hubs will be joined by bridges and switches.

According to research by Infonetics Research, LAN equipment sales in the SOHO market will be skyrocketing in the next three years, from $1.7 billion last year, to $7.95 billion in 2000. Infonetics defines SOHOs as companies with 25 computers or less, and no MIS support or central dial-in site.

FriendlyNet Ethernet hubs feature auto-partitioning capability, collision and link activity/integrity, and diagnostic LEDs for monitoring power. The five-port hub is priced at $79, and the eight-port version is priced at $99.

For more information, contact Asanté Technologies, 821 Fox Lane, San Jose, CA 95131; (408) 435-8388; (408) 432-7511; Internet: http://www.asante.com.

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www.pueblo.gsa.gov (It's the cat's meow.)

A public service of this publication and the Consumer Information Center of the U.S. General Services Administration

Y2K UPDATE

In terms of preventing business-wide failure during the Year 2000 date change (Y2K) dilemma, one of the most important measures to take is to identify sources of excessive resource demands. Because Y2K entails massive code changes, the buzz around the industry is that these changes will adversely affect application performance. And, since nothing happens within a vacuum, the additional time constraints that will be required to resolve failures in applications is going to impact a company's schedule for redeployment. One company that's addressing this issue is Programart Corporation.

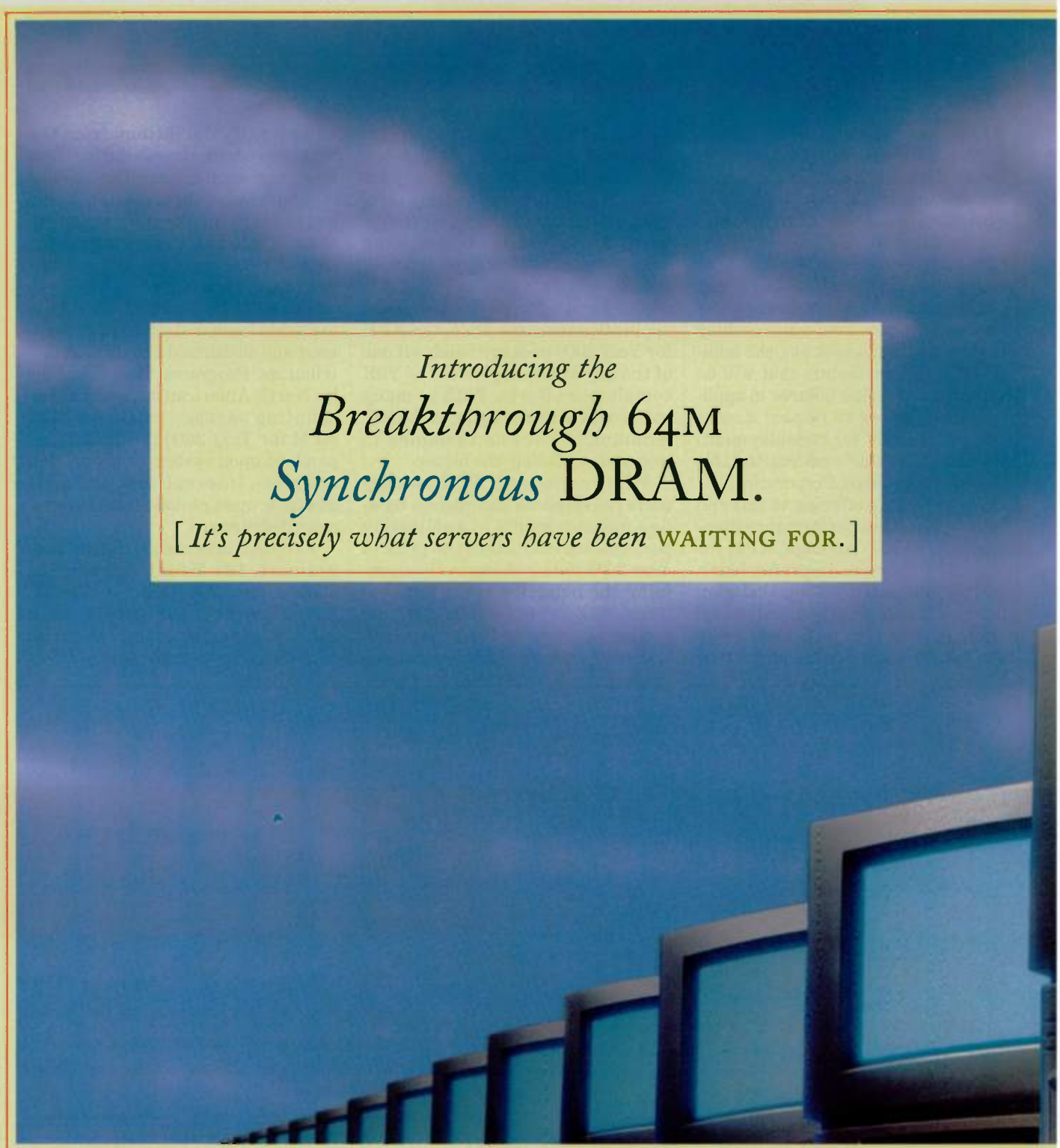
Programart's offering to this end is an application performance management (APM) package. APM for Year 2000 provides IS professionals with an integrated solution that comprises software tools and customized training. Two such tools included in the package are Strobe and APM-Power. The importance of the customized training is evident when staff members who aren't very involved in the process become integral members of the compliance team. This situation is becoming more common as Y2K approaches.

Enabling enterprises to quickly identify and address the sources of application resource drain, the APM for Year 2000 package heads off one of the key stumbling blocks of Y2K compliance efforts. With so many businesses at risk of dying at the millennium, the fewer variables to worry about failing, the better.

With Programart's APM package, users can establish and manage baseline measurements of application performance characteristics prior to Year 2000 coding changes. By examining the behavior of the applications, Y2K professionals can then compare "before and after" application performance characterizations and identify deviations from the baseline measurements during Year 2000 regression testing. The baseline measurement information helps users pinpoint the programming statement that's responsible for causing excessive CPU consumption or excessive wait time.

The APM for Year 2000 package is available immediately from Programart and authorized Programart distributors. Programart has a deal for its North American customers, discounting package pricing for the APM for Year 2000 to $21,250 (dependent upon system configuration and size). International pricing is available upon request from Programart distributors.

For more information contact Programart, 124 Mount Auburn St., Cambridge, MA 02138; (617) 661-3020; fax (617) 498-4010; e-mail: info@programart.com; Internet: http://www.programart.com.—*DS*



Introducing the

Breakthrough 64M *Synchronous* DRAM.

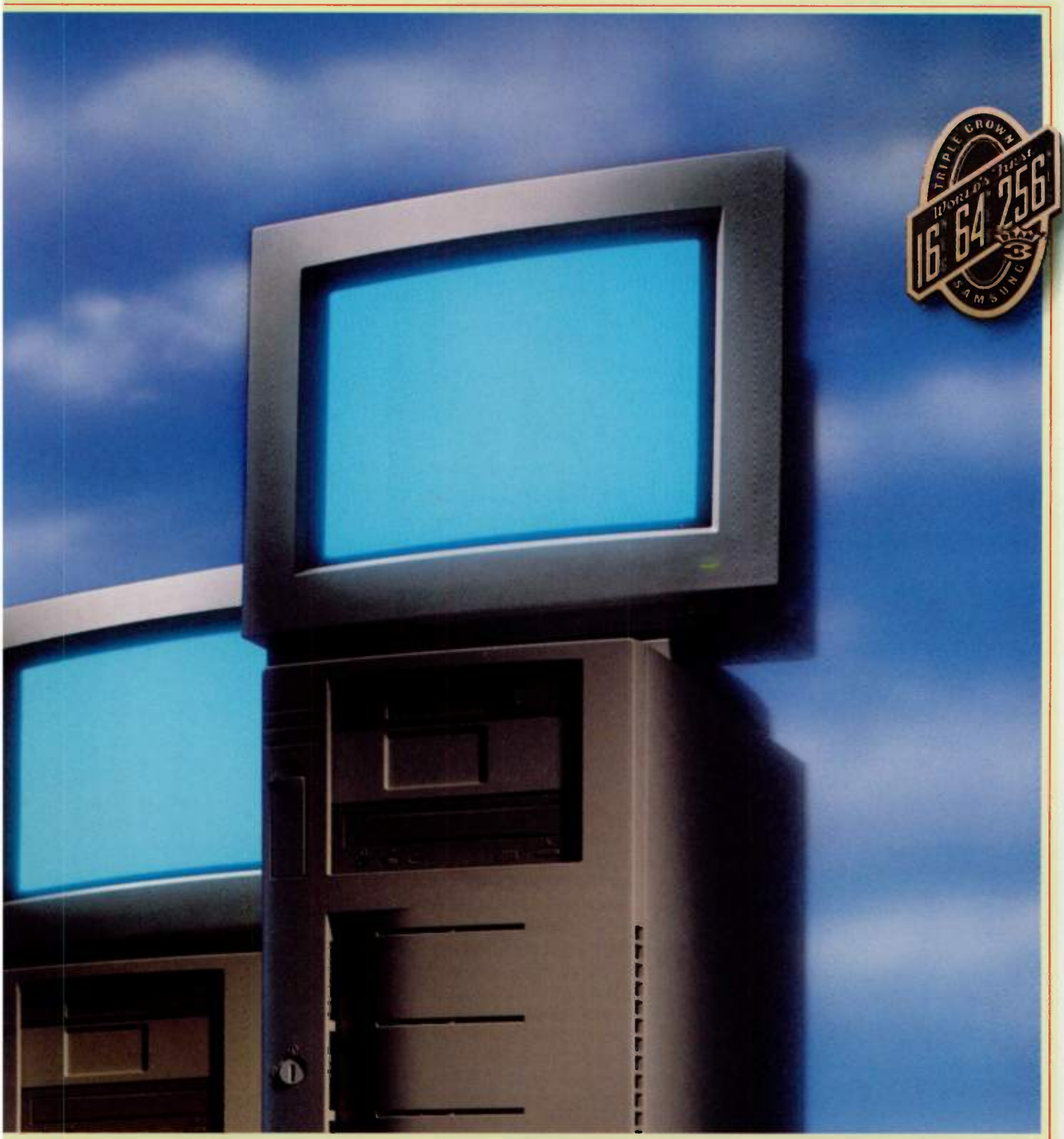
[*It's precisely what servers have been* WAITING FOR.]

You know something's up when you see a bunch of network servers voluntarily queuing up out in the street.

Well, what they seem to know is what you should too: the performance-boosting part that servers crave, the 64-meg Synchronous DRAM, is now available in volume production, or at least it is here at Samsung.

We've had working samples of this 100 MHz chip for some time. And just as we were with samples, we're ahead of the competition with actual production too.

What that in turn means is that you're now in a position to put yourself ahead of your own competition too. Because the 64-meg part gives you the density you absolutely require for servers (and in many cases for workstations), while also delivering the performance advantages you can only get from the new



Synchronous design.

Like we said: the part everybody's been waiting for.

At Samsung, we're proud of this breakthrough product because, like the first 16M, 64M, and even 256M DRAM, and like many of our leadership SRAMS, the new SDRAM helps extend our worldwide leadership in memory products.

But more than that, we're proud it can help our customers continue to attain leadership too.

And incidentally, we promise you won't have to wait in line.

For details on the new SDRAM, please call 1-800-446-2760 today.

Or write to SDRAM Marketing, Samsung Semiconductor Inc., 3655 North First Street, San Jose, California 95134.

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LETTERS FROM LONDON

Cashing In The Chips?

PETER FLETCHER
FIELD CORRESPONDENT

You're alone in a strange city and slightly lost. A street map would be useful—and you know just where to get it. You have your notebook computer and your digital mobile phone You can connect to the Internet, search out the web site for Mapquest or Multi-Media Mapping,and zoom in on the right town—or maybe your GPS device can do it for you.

But wait—you must pay for the map. Only around 50 cents or so, but that's too small for a credit-card transaction, and you're not too happy about sending your card details from the street.

Collecting cash for spontaneous purchases of information is a problem that's been on the minds of many since on-line information services first set out to attract casual callers in the late 1970s. In 1979, we tried public coin-operated videotex terminals here in the U.K. They were not successful. Back then, the public was not ready to grasp the idea of paying for ephemeral information, let alone searching out a strange machine to do it.

The hype around the Internet has changed that attitude, while pocket-sized computers and data-ready mobile phones means you don't have to search out a public "pay-terminal"—but the question remains: How can the information provider find a way of getting paid on the spot for the hard work put into getting together the information you need at any particular time?

AT&T's European telecom network operator, Unisource, says it has the answer. A trial in the U.K. and The Netherlands is underway of a system designed to accept "electronic cash" over a GSM cellular network. According to Julian Wilson, Service Development Director, the idea is "to put the equivalent of a combined cash dispenser and vending machine in people's pockets."

It all hinges on the use of an "electronic wallet"—a "smart card" the size of a standard credit card, but with an embedded processor and memory, able to securely store credit units in any currency—and to be replenished when the current balance gets to zero. Participants in the trial known as MobIDIC include Mondex, an electronic wallet issuer owned jointly by various European banks; Apple Computer, who will supply 100 Newton Message Pad 2000 pen-input computers; Nokia Mobile Phones, whose GSM telephones and data adapters will be used; and a handful of other information providers.

Here's the process. First, the Newton is equipped with a card-reader that can extract from and pay "cash" into the electronic wallet card. Next, the Newton has to be linked with the mobile phone. It must have the right software loaded—a purpose-designed net browser that can handle the "banking protocols." It also must be robust enough that if the radio link with the cellular network breaks down before a completed transaction, no charges are levied.This set-up would retail for about $1000 in Europe. But Wilson is enthused by the variety of "personal integrated communicators" about to hit the market. They combine GSM communications with computing power in a pocket-sized bundle and should sell for under $500 before year's end.

Will anyone want to use them? Statistics show that there are more users of electronic wallets and mobile phones in Europe than Internet subscribers. Using the Newton's infrared communications capability, Wilson says it is easier to transfer cash from one wallet to another. I sympathize with a character from "The Hitch-Hiker's Guide to the Galaxy." Faced with payment in electronic cash, Rooster says, "If you can't scratch a window with it, I'm not interested." Maybe I'm just old-fashioned.

Peter Fletcher is Electronic Design's U.K. correspondent. His e-mail address is: panflet@cix.compulink.co.uk.

OFF THE SHELF

"Applied Cryptography, 2nd Edition" is a comprehensive survey of modern cryptography. The book details how programmers and electronic communications professionals can use cryptography to maintain the privacy of computer data. Also described are dozens of cryptography algorithms and advice on how to implement them. This new edition includes the latest protocols for digital signatures, authentication, secure elections, and digital cash, along with information on key management and cryptographic implementation. The 758-page book is priced at $49.95. Contact John Wiley & Sons Inc., 605 Third Ave., New York, NY 10158-0012.

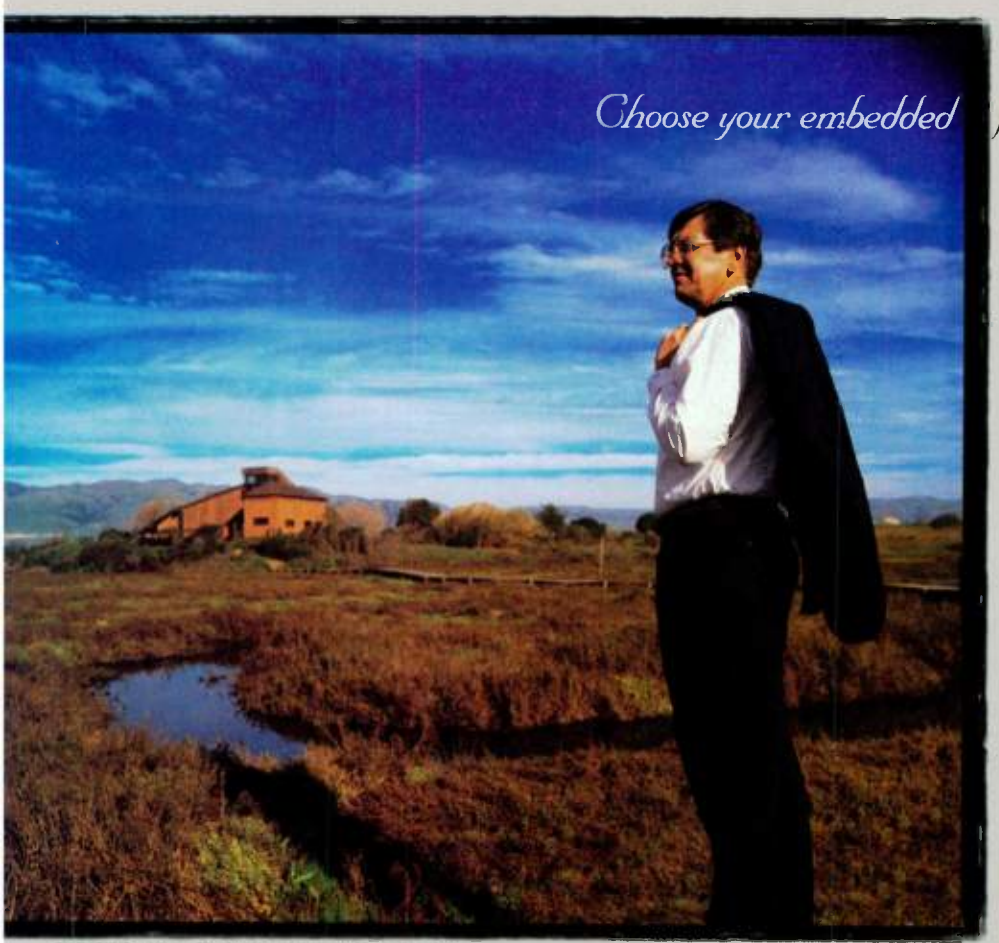
"Workstation Buyer's Guide" helps buyers understand the acronyms, terms, and the fiction of sales pitches from the facts to help them make the best workstation purchase. Major topics include assessing CPU performance, I/O versus switches, Unix versus Windows, and evaluating graphics benchmarks. Priced at $19.95, the 33-page book contains tables, charts, illustrations, and a glossary. Contact CAD/CAM Publishing Inc., 1010 Turquoise St., #320, San Diego, CA 92109; (619) 488-0533; fax (619) 488-6052; Internet: http://www.cadcamnet.com/circ.

"Oracle: The Complete Reference, Electronic Edition" gathers all major Oracle definitions, commands, functions, features, and products together into a single reference. Included is a beginner's guide to Structured Query Language (SQL), tips and techniques for developing Oracle products, and examples of the use, design, and maintenance of databases. A CD-ROM features all of the tables in the printed book. The 1150-page book is priced at $55. Contact Osborne/McGraw-Hill, 2600 Tenth St., Berkeley, CA 94710; (510) 549-6600; fax (510) 549-6603; Internet: http://www.osborne.com.

"THE INTERNET IS QUICKLY TRANSFORMING SOCIETY.

TO STAY AHEAD OF THE MARKET, WE NEED LEADING TECHNOLOGIES IN *volume.*"

FRANK MARSHALL, VP/GM Core Business Products at Cisco Systems



processor wisely.

"The business of moving information is exploding, thanks to the rapidly expanding use of the Internet. As the worldwide leader in networking for the Internet, Cisco is expected to set the pace.

"One way is to work long hours. Another way is to form alliances with leading suppliers such as NEC. Like Cisco, they're committed to building products that will have a profound impact on the emerging information economy.

"One of NEC's products, the $V_R5000^{™}$ 64-bit embedded processor, proved to be the best choice for use in the Route Switch Processor in the Cisco 7500 router. First, it's a great architecture for high-speed data communications. But more importantly, NEC was able to produce this leading-edge technology in the volume we need.

"NEC is a quality supplier able to meet Cisco's expectations for a product's entire life cycle. Which, as you know, keeps getting shorter and shorter.

"The fact is, working with suppliers like NEC allows us to play a part in the rapid transformation of the way the world does business."

For more information on NEC's V_R Series™ MIPS™ RISC embedded processors, call *1–800–366–9782*. Ask for Info Pack #195.

"Cisco selected NEC's V_R5000 embedded processor because we needed a leading-edge product that could quickly be produced in volume."

NEC

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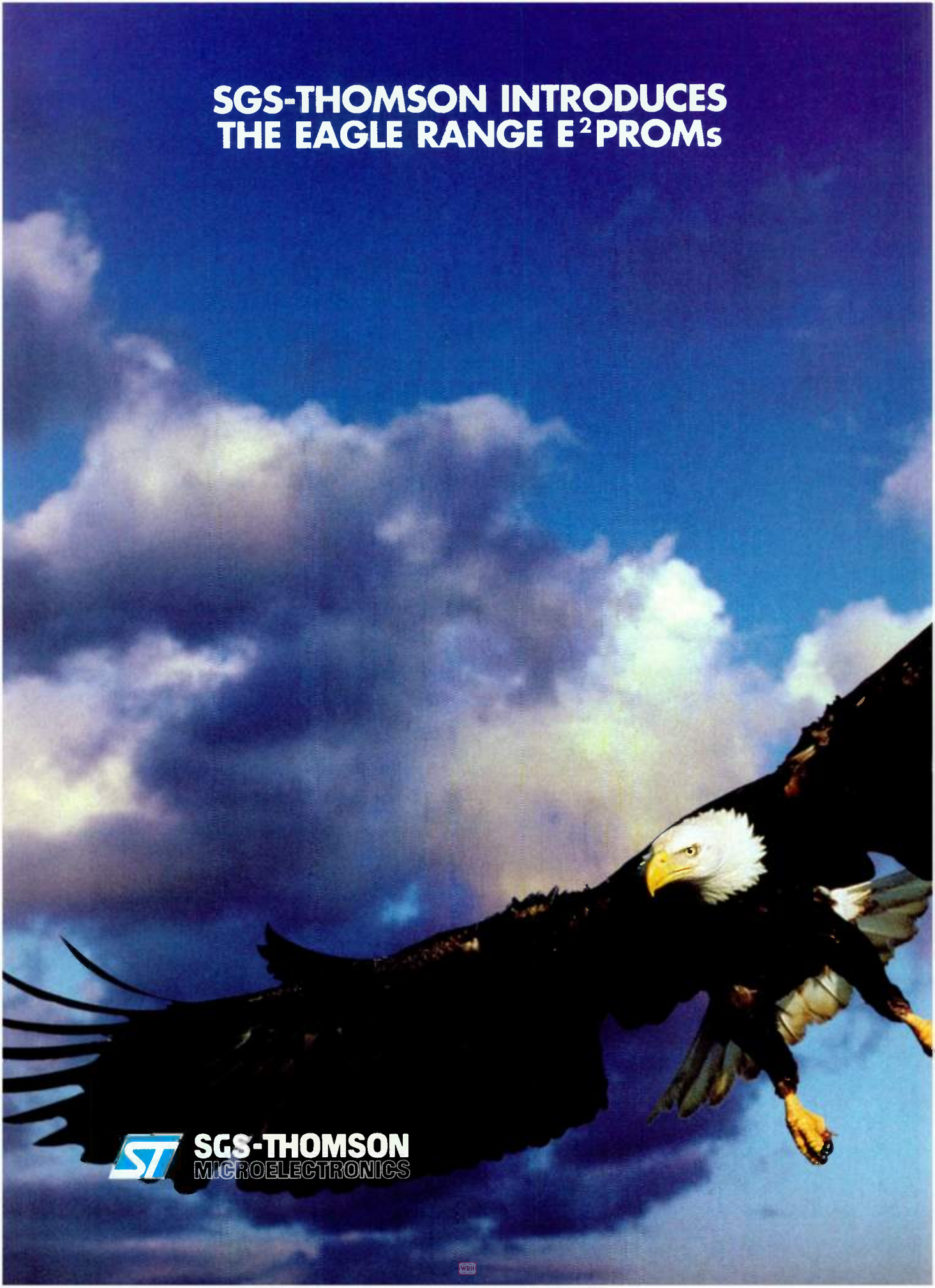
SGS-THOMSON INTRODUCES THE EAGLE RANGE E^2PROMs



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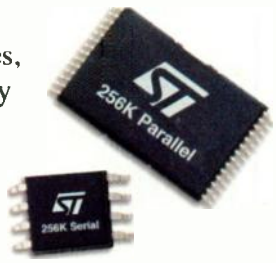

Now, for the first time, you can get high density 256K E^2PROMs in cost-saving serial as well as parallel.

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Count on a million erase/write cycles over the entire operating temperature range — not just room temperature. Get more performance out of less space with ST's own advanced 0.6μ technology. And maximize your design opportunities with a range of operating voltages down to 1.8V.

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E²PROMs THAT MAKE YOUR DESIGNS FLY

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MICROWIRE™	ST93C06	ST93C46 ST93CS46	ST93C56 ST93CS56	ST93C66 ST93CS66	*1H97* M93C76	*Q197* M93C86				
I²C		ST24C01 ST24W01 M2201* ST24LC21*	ST24C02 ST24W02 M34C02*	ST24C04 ST24W04	ST24C08 ST24W08	ST24C16 ST24W16 ST24164*				
EXTENDED I²C						ST24E16	*NEW!* M24C32	*NEW!* M24C64	*Q496* M24128	*NEW!* M24256
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PARALLEL						M28C16 M28C17		M28C64C M28C64		*NEW!* M28256

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  - Page Load Timer Status
- SOFTWARE DATA PROTECTION

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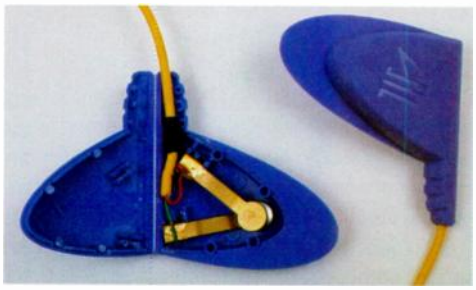
Picking The Right Contacts



Every now and then something eyecatching comes along, and we decide that it's far too nifty to keep to ourselves. This little item is one of those eyecatchers.

As is the case with most frustrated musicians (and some "real" musicians as well), we sometimes find ourselves playing air guitar. We've all gone through the embarrassment of having someone walk into a room where we're strumming away on a tennis racket, howling away to the music. This rite of passage has even been celebrated in several movies in the last ten years.

Now we have the opportunity to play along with some platinum album holders just by using the V-pick. Shown here, the V-pick from Virtual Music Entertainment, Andover, Mass., is used to activate the interactive, virtual music video game, "Quest For Fame." V-pick, the game controller, sends the vibrations caused by the player's strumming to the software via a 10-ft. long cable that runs from the V-pick to a computer port. The V-pick gives the user the sensation of playing guitar chords, even if the virtual pick is being strummed against the refrigerator door. But the real work of the pick is done by the contacts.

In finding the right contacts to do the job, Virtual Music sought the help of Nortstan Inc., Waukegan, Ill. Norstan, well known as the horn contact supplier for the three big auto makers in the U.S., worked with Virtual Music's engineering subcontractors to formulate a precision electrical contact for the V-pick.

The major issues at play in the search for the ideal contacts were wear and corrosion resistance, reliability in varied environments (such as recently flooded basements or stuffy attic apartments), repeatability, and welding requirements. According to Tom Pencak, Chief Engineer at Norstan, "The art in engineering contacts lies in coming up with just the right witches brew, while keeping cost to a minimum."

In the V-pick, there are two contacts making up the single circuit. While the player is strumming along, one contact is banging away at the other. Considering that this banging causes wear, Pencak decided that a base metal with a nickel plate on it would be best for the application. Previously, the Virtual Music had been using brass.

Norstran brought their cost-saving experience to the table, introducing the engineers to a steel solution. They decided to use steel because the nickel was going to be acting as the conducting surface. Subsequently, the cost of the contact set went down.

In the design, Norstran took the V-pick contact from a two-part to a one-part contact. They changed the design so that just one component would be welded to a blade. Again, the cost of the V-pick decreased because the previous design's materials were more expensive and costlier to assemble.

In the V-pick, there are two contacts. While the player is strumming, one of the contacts is fixed while the other is movable. These contacts are bouncing during the action, causing one contact to hit the other, registering a hit in the computer. When the hit happens, a strum sound is played.

The game works by taking the player on a trip through the performance life of a guitar player. The object of the game is to play well enough to play in a big concert. During the game live action and cartoon graphics guide the player along the path of guitar stardom. But, when a player strums the V-pick at the wrong time, though, the music goes flat. Consequently, the player is sent down to the minors and then chastised appropriately.

For more information, contact Norstan Inc., 2421 Delany Rd., Waukegan, IL 60087; (800) 244-8338; fax (847) 662-8789; Internet: http://www.norstaninc.com.—*DS*

BACK TO SCHOOL

"Designing Multimedia for Maximum Interactivity" is a two-day seminar that looks at the interactive application marketplace, and will help guide attendees to begin constructing effective, interactive multimedia. Some of the topics that will be discussed include defining interactivity, creating interactivity, content design and organization, and using development models and templates. Seminar cost is $695, and will be held in various locations around the U.S. Contact Influent Technical Seminars, 498 Concord St., Framingham, MA 01702; (888) 333-9088; fax (508) 872-113; Internet: http://www.influent.com.

"Software Licensing Agreements" is a seminar designed specifically for software users, sellers, and developers who buy software, CD-ROMs, multimedia, or use the Internet. The one-day workshop will review the software acquisition cycle, and then analyze the key depts of a software licensing agreement. Participants will learn how to draft and negotiate software use rights, licensing fees, royalties, and payment terms. Registration fee is $495, and the workshop will be held in various locations in the U.S. Contact the Professional Learning Center, 4521 Campus Dr., Suite 283, Irvine, CA 92612-2699; (714) 725-0758; fax (714) 725-9953; Internet: http://www.plci.com.

Constructive Criticism Time

It's that time of year again—Spring. Synonymous with yard sales, block parties, and new puppies, Spring at *Electronic Design* means annual reviews. We take a good hard look at ourselves and start making lists of things to improve. Part of this process involves you, our readers. Let us know how the QuickLook section can better meet your needs. E-mail **Mike Sciannamea** at **mikemea@class.org**, or **Deb Schiff** at **debras@csnet.net**. Interesting stationery should be sent to: QuickLook, *Electronic Design*, 611 Route 46 West, Hasbrouck Heights, NJ 07604. Our fax number is (201) 393-0204.

TRUDEL TO FORM

JOHN D. TRUDEL
CONTRIBUTING EDITOR

I stand here before you blushing, the high-tech business guru whose own business got crunched by the recent "America on Hold" meltdown. I got mail, phone calls, and several media interviews on this one.

The interesting thing was that most missed the point. Certainly, Steve Case's PR machine did its best to spread confusion. What happened had little to do with "Internet congestion," technology, price cutting, or market uncertainty.

AOL's core business strategy has been and still is to carpet bomb the world with disks. Plug in, turn on, and anyone can cruise Cyberspace. Service is cheap and local dial-ins are everywhere. AOL looks good, but its' a trap.

Last fall, Case reported to Wall Street that he was losing *one-third* of his customers each month. He had been doing hocus-pocus with his accounting to obscure AOL's marketing costs. Adjusting that wiped out all the profits AOL had ever made. Case's business model is unusual: The first mass-market instance I've seen where a major firm depends on unhappy customers.

It will be hard for AOL to change. Churning and burning your customers is expensive, and Case is now promoting a product he doesn't have—unlimited service. His competitors can make money at $20 a month, but he can't. He can only deliver the profits he needs at that price point if his system is not used by many who pay for it.

Case's business model is like a chain letter. At a one-third churn rate and 9 million subscribers, squeezing an extra month from those canceling is $60 million dollars per month of pure profit. If he stops abusing customers, he takes a profit hit.

A few years ago, a PC company, Zeos, vanished the same year they won awards for "best products." Their PCs looked good on benchmarks, but were so compromised they were almost useless to customers. The one I bought had five ISA slots, but only one could be used due to blockage by a heat sink. I had to fight my way past a six-month stall to get my money back.

After fleeing AOL, I was snagged by a nasty bug in the popular e-mail program, Eudora. It has a nice feature that lets you mail to large lists without publishing the addresses. I tested it, and it worked fine. Unfortunately, when I tried to mail my new address to several thousand contacts, it regurgitated endless pages of addresses, some of which were sensitive. (My readers and colleagues are very kind. I got several supportive notes and only one "remove," but I was mortified.)

What these cases have in common is fundamental: Products that give good first impressions, but contain fatal flaws. The key question is: "What is business about?" Peter Drucker says it is about "profitably creating customers." Western MBA training says it is about "profits." The two views are as different as chalk and cheese.

This suggests a good test: Forget what firms say. Treat benchmarks and reviews with caution. Instead, watch what companies do when they have problems.

Top companies reveal and fix customer problems, regardless of short-term profit impact. The Tylenol case is famous, and Intel did the same to fix the Pentium bug. Why do Japanese firms, with exceptions, do so well? Largely because of trusted quality and a willingness to stand behind their products.

John D. Trudel, CMC, provides business innovation consulting to selected clients. Lectures, keynotes, and workshops also are available. He is the author of "High Tech with Low Risk." The Trudel Group, 33470 Chinook Pl., Scappoose, OR 97056; (503) 640-5599; fax (503) 543-6361; e-mail: jtrudel@ystis.net; Internet: http://www.trudelgroup.com.

EYE ON ISO 9000

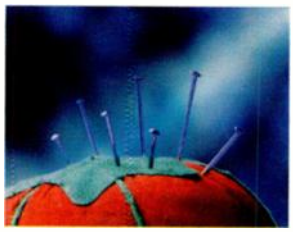
Quadtech Inc. has recently received ISO 9001 certification. Formerly known as GenRad Instruments, the company offers a complete line of precision LCR meters, Hipot testers and safety analyzers, LCR standards, decades, and calibration and repair services. Contact Quadtech Inc.,100 Nickerson Rd., Marlborough, MA 01752; (800) 253-1230; fax (508) 485-0295; Internet: http://www.quadtech-inc.com. **CIRCLE 485**

Bemis Manufacturing Co. has earned ISO 9001 certification. The company manufactures compression molded, injection molded, and extruded products for such applications as building products, health care products, gardenware,causal furniture, and housewares. Contact Bemis Manufacturing Co., 300 Mill St., P.O. Box 901, Sheboygan Falls, WI 53085-0901; (414) 467-4621; fax (414) 467-8573. **CIRCLE 486**

Racal Instruments Inc.'s Irvine, Calif. facility has achieved ISO 9001 certification. The company is a manufacturer of an extensive line of precision electronic measurement test products. Contact Racal Instrument Inc., 4 Goodyear St., Irvine, CA 927118; (800) 722-2528; fax (714) 859-2505. **CIRCLE 487**

Centurion International Inc. has achieved ISO 9001 registration. The company, specializers in engineering design, development, and medium- and high-volume manufacturing, designs and manufactures battery packs for wireless communications and computing devices. Contact Centurion International Inc., P.O. Box 82846, 3425 N. 44th Street, Lincoln, NE 68501; (402) 467-4491; fax (402) 467-4528. **CIRCLE 488**

Fairchild Corporation's Rosan business unit of Fairchild Fasteners unit has received ISO 9001 certification. The company manufactures aerospace fasteners for use in a variety of applications. Contact Fairchild Fasteners/Rosan, 3130 W. Harvard Street, Santa Ana, CA 92704; (714) 641-8800; fax (714) 641-8801. **CIRCLE 489**



HOW MANY TOKO LL'S CAN YOU PLACE

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Such a micro size may seem impossible, but not to Toko engineers. The LL1005 (inductance range 1.0 to 27.0 nH) is merely the latest addition to Toko's micro-miniature line of ceramic multilayer chip inductors available from Penstock. With an 0402 footprint and an 0.05 profile, *the LL1005 is the world's smallest*–by far.

Toko's cutting edge design and leadership in ceramic multilayer technology helps in other ways, too. Toko chip inductors offer higher current handling capabilities (up to 1 amp) and tolerance as low as 3% on some values. Plus:

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- Reflow solderable
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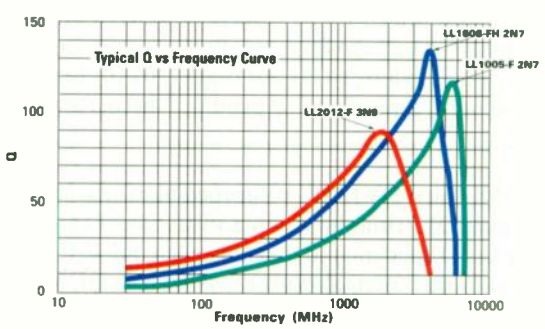
- Quick delivery

As the world's largest RF/microwave distributor, Penstock is the design engineer's link to Toko's advanced technology. We inventory more than 5 million Toko parts –*in stock*– and serve the engineering community from over 25 sales offices throughout North America and Europe. With **Toko** and **Penstock**, you always know, there's nothing more advanced–or more readily available– anywhere in the world.



Toko LL Prototyping Kits Available

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In Northern California call: 1-408-745-8190
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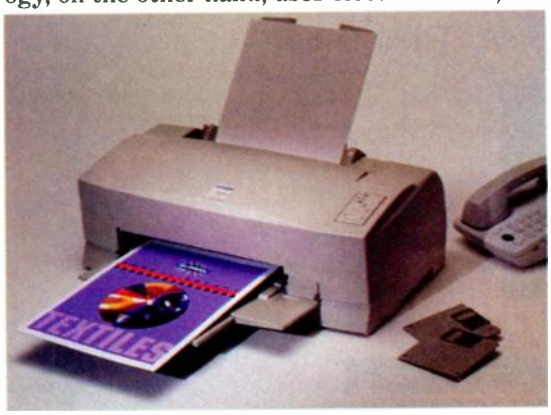
READER SERVICE 162

HOT PC PRODUCTS

The Epson PicturePerfect Imaging System is the technology behind Epson's jump from 720 to 1440 dpi ink-jet resolution in its color printers. The imaging system includes the print head, ink, media, printer driver, and printer engine.

The highest ink-jet resolution available is the result of Epson's piezoelectric technology. Most ink-jet manufacturers use thermal technology, which boils the ink and spits it out onto the page. Piezo technology, on the other hand, uses electro-



mechanical pressure to accurately and consistently place uniform ink droplets on the page. Photo-quality printing is seen through the second process, without using special "photo" inks.

Epson uses a special piezoelectric print-head design, named Micro Piezo, in its new Stylus Color 600 and 800 units. The Micro Piezo uses super micro dots that are 30% smaller than previous models, to create realistic fleshtones, smooth color gradations, and a wider range of halftones. Another feature of the new print head is more nozzles with higher ink-ejection frequencies, making for much faster print speeds.

Because the inks for these new printers don't have to be boiled, Epson has a broader ink selection. The new QuickDry inks are highly concentrated and are designed to work with various paper qualities including photo-quality ink jet paper, glossy film, ink jet cards, transparencies, and iron-on transfer paper.

Epson's new printer driver uses the company's new AcuPhoto halftoning module in the color translation process. The driver selects the most appropriate profile to fit the data being printed—whether it's text-only, photographic, or a combination of both. New utilities also have been built into the driver. Head cleaning, nozzle checking, and print-head alignment are all checked by the driver.

The Stylus Color 600 is priced at $299, and the Color 800 is priced at $449. Both printers use IEEE-1284 parallel and high-speed Mac serial standard interfaces, and the Color 800 also uses Ethernet and LocalTalk.

Contact Epson America Inc., 20770 Madrona Ave., P. O. Box 2842, Torrance, CA 90509-2842; (310) 782-0770; fax (310) 782-5220; Internet: http://www.ea.epson.com.

The ZiVa-Card DVD-PC reference platform by C-Cube Microsystems and Diamond Multimedia, is an add-in board that allows PC OEMs to bring their DVD solutions to market more quickly.

PC add-in card manufacturers, as well as OEM-PC manufacturers can use ZiVA decoder technology to take full advantage of Dolby Digital (AC-3) sound technology. Dolby Digital gives users a true home-theater experience, as well as the surround sound effect. The new reference platform also features a high level of integration.

The ZiVA-Card gives users full 30 fps playback, 5.1-channel audio output, optimized audio/video synchronization, on-board digital copy protection security, and MacroVision 7 for anti-taping protection.

The board can be stuffed in various formats, enabling it to conform to a variety of PC and graphics architectures.

For more information, contact C-Cube Microsystems, 1778 McCarthy Blvd., Milpitas, CA 95035; (408) 944-6300; fax (408) 944-8132; Internet: http://www.c-cube.com.

Working Model 3D for SolidWorks, Solid Edge, and Mechanical Desktop are three integration releases of the motion simulation CAD software. SolidWorks is a product of SolidWorks Corp. (Concord, Mass.), Solid Edge is put out by Intergraph Software Solutions (Huntsville, Ala.), and Mechanical Desktop is a product of Autodesk Inc. (San Rafael, Calif.).

These new releases of Working Model 3D use Knowledge Revolution's Automatic Constrain Mapping (ACM) technology. The new technology allows engineers to translate solids and assembly constraints from the three programs to mechanically-joined systems in Working Model 3D in a seamless manner.

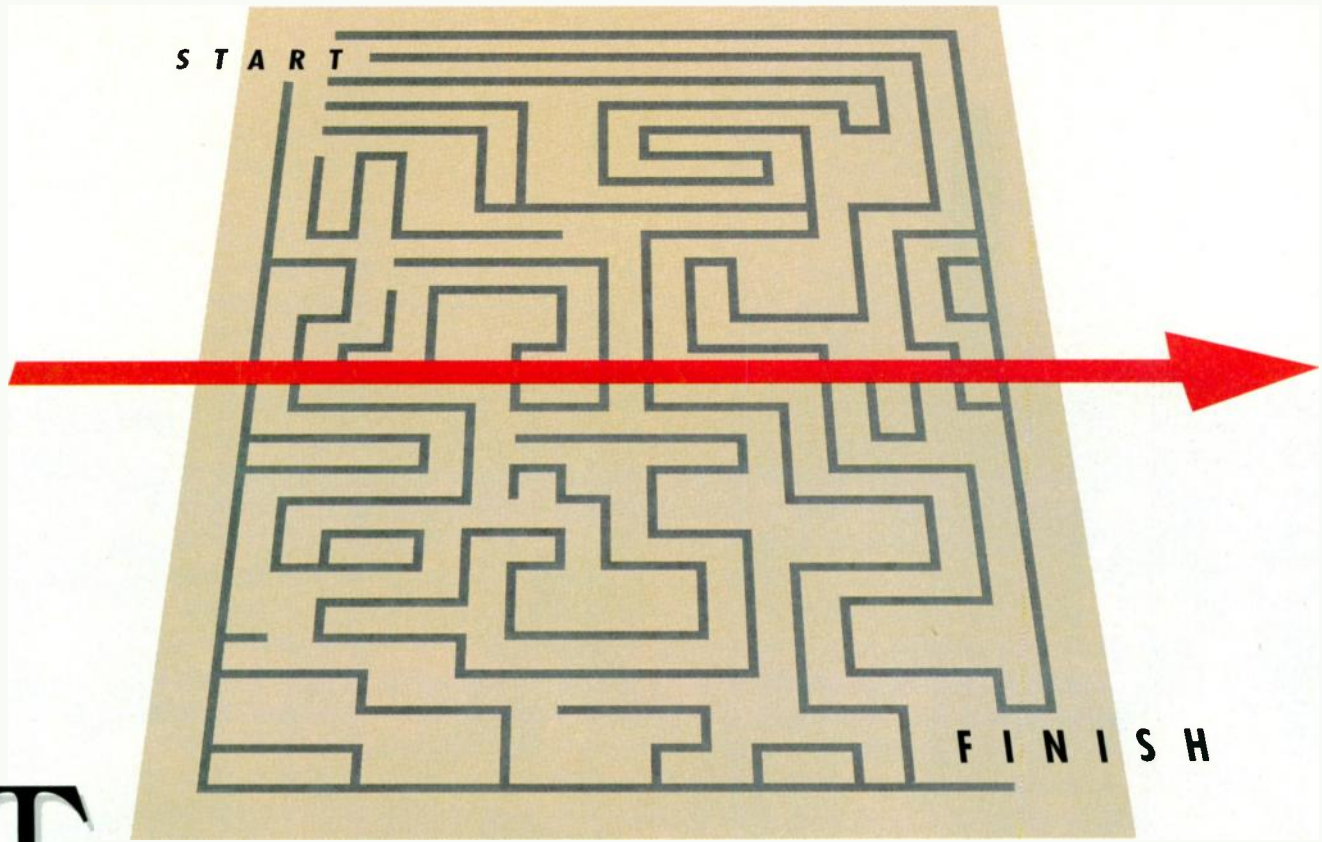
The integrated CAD and simulation tool is designed to cut down on expensive prototyping, and speed time-to-market.

For more information, contact Knowledge Revolution, 66 Bovet Rd., Suite 200, San Mateo, CA 94402; (415) 574-7777; Internet: http://www.workingmodel.com.

Simulink 2 is a nonlinear simulation software tool that allows complex systems design engineers to have more functionality and modeling and analysis capabilities. The solution, from The MathWorks, includes an advanced simulation engine for faster and more accurate simulations of continuous-time systems.

Among the significant features included in the package are ordinary differential equation solvers, support for state events, support for enabled and triggered subsystems, an expanded block library, masking capability, scope block with zoom and autoscale, signal and port labeling, and on-line documentation in HTML.

For more information on the Simulink 2 software tool, contact The MathWorks, 24 Prime Park Way, Natick, MA 01760; (508) 647-7000; fax (508) 647-7001; Internet: http://www.mathworks.com.



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- Lower return loss/VSWR through bypass.
- Repeatable insertion loss.
- A wide variety of configurations and options, all in rugged, cost-effective, space-saving packages.

These innovative RF relays mark the end of two previous intrinsic signal path concerns. First, four connecting points are removed. Also, two changes of materials are eliminated. Together, these enhancements reduce the distance your signals must travel, maximizing signal integrity.

We don't mind your signals repeating themselves, we just want to prevent them from getting lost in the maze. Get the straight scoop on high frequency relay innovations by calling **1-800-594-0855** today.

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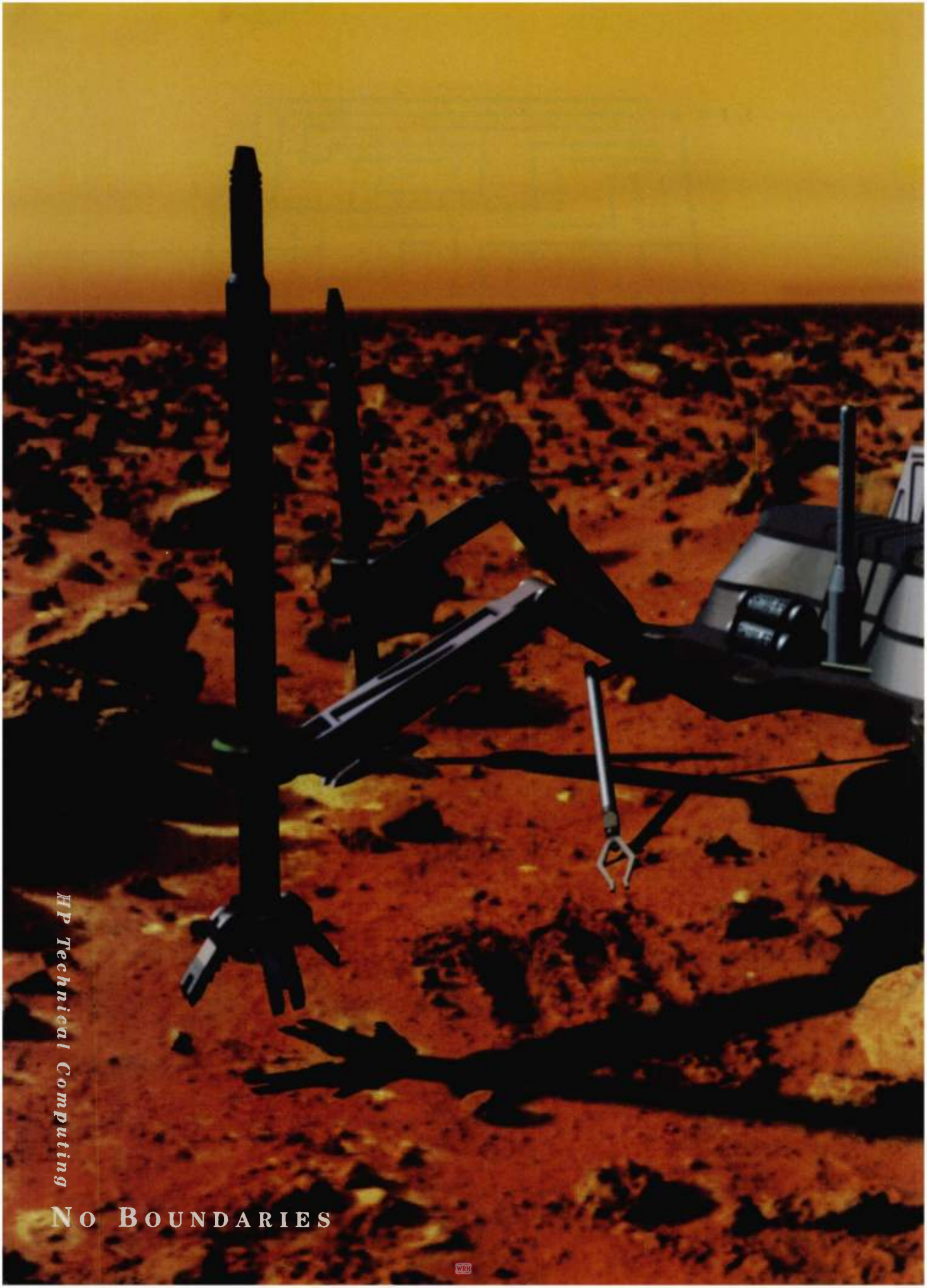
HP Technical Computing
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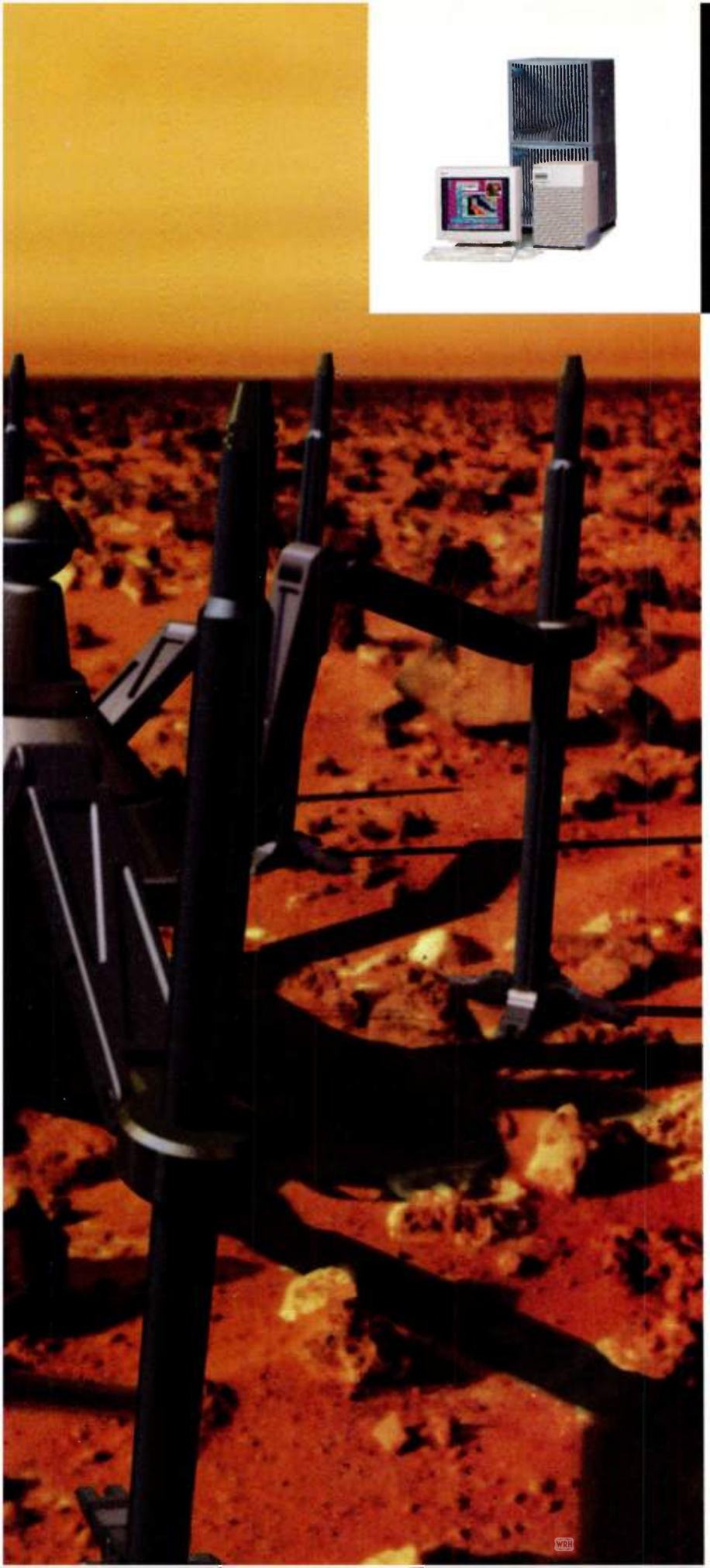

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HEWLETT® PACKARD

SARC Fishing For Computer Viruses

You're typing the final report to be presented in the morning to your department head on the project your team's been working on for the past six months. Suddenly, you hear a strange clicking noise as you type. You look at your monitor, and the following message stares you in the face:

The FORM-VIRUS sends greetings to everyone whos reading this text. FORM doesnt destroy data! Don't panic!

Of course, you panic. Your computer, and very likely your company's entire network, has been infected with an insidious computer virus. All that work with all that data is now just wasted effort.

The previous scenario seems to be happening more frequently these days than ever before. Some of the most common computer viruses are WM.Concept (the most prolific virus), Form.A, AntiEXE.A, and Boot-437. In fact, as of this past February, 259 macro viruses have been documented, up from a total of 42 in April 1996 *(see the figure)*. And these viruses are wreaking all kinds of havoc. Roughly 35% of them have been classified as "deliberately destructive," compared to 10% in 1993. And these viruses are not only being created by hackers from some technical university in Massachusetts, California, or New York. They're also coming from virus "hot spots" like India, New Zealand, and Australia. And with the explosion of the Internet, viruses aren't just passed along by the simple exchange of floppy disks between co-workers. You have to be wary of the type of file you're downloading off of some ftp site from New Delhi, Auckland, or Sydney.

To combat the expanding problem of computer viruses, Symantec Corporation's AntiVirus Research Center (SARC) is a team of virus experts who are continuously developing identification and detection for computer viruses. As new viruses appear, SARC provides either a repair or delete operation, thereby keeping users protected against the latest virus threats. Symantec provides virus definitions to users that are free of charge, easy to obtain and install, and are updated monthly.

According to their mission statement, SARC is "committed to providing swift, global responses to computer virus threats, proactively researching and developing technologies that eliminate such threats and educating the public on safe computing practices." Some of SARC's current anti-virus products include Norton AntiVirus (NAV) for DOS Windows 3.1, NAV Internet for Netscape, and NAV 2.0 for Windows 95. Anti-virus products for Macintosh, Novell, and Windows NT also are available.

Norton AntiVirus technology provides users with flexible and adaptable anti-virus security solutions. For example, LiveUpdate detects an Internet connection or modem, automatically connects it to a Symantec server, then downloads and installs the latest virus definitions. In addition to receiving Symantec's monthly virus definition updates, LiveUpdate users can install software patches and obtain product information.

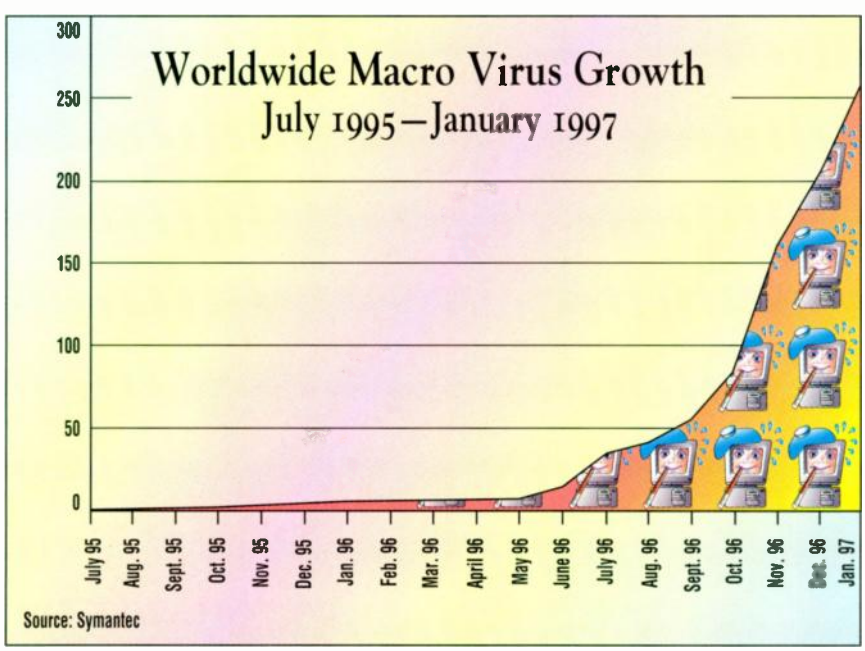
SARC's Seeker is an artificially intelligent web-spider system that searches the World Wide Web for new and unknown viruses. Seeker is based upon three of Symantec's advanced modular anti-virus technologies: The Seeker file retrieval system, the Bloodhound virus-trait (heuristic) scanner, and the Symantec AntiVirus Research Automation system (SARA). Bloodhound detects viruses by inspecting suspect files for virus-like behavior.

In fact, the Bloodhound heuristic technology has been shown to detect upwards of 80% of new and unknown viruses. If a program exhibits virus-like behavior, it is passed on for further analysis to SARA. The SARA module takes a virus sample, extracts its unique qualities, and develops a Symantec detection and repair scheme in under 5 minutes.

However, virus detection is not all that SARC does. They also will inform you of virus *hoaxes*. In the last few years, many announcements have surfaced of a new virus that, according to the information providers, "will destroy your computer's internal hard drive, and will render your Internet connection useless." (They probably will say that this virus might end civilization as we know it.)

As evidenced by the "Good Times" hoax, people will put out information that a new virus will cause incredible havoc. SARC detects hoaxes and provides accurate information so you and your company won't have to invest time and money to combat a new virus every day.

For more information, contact SARC, 2500 Broadway, Suite 200, Santa Monica, CA 9404-3063; (310) 453-4600; fax (310) 449-7041; Internet: http://www.sarc.com.—*MS*



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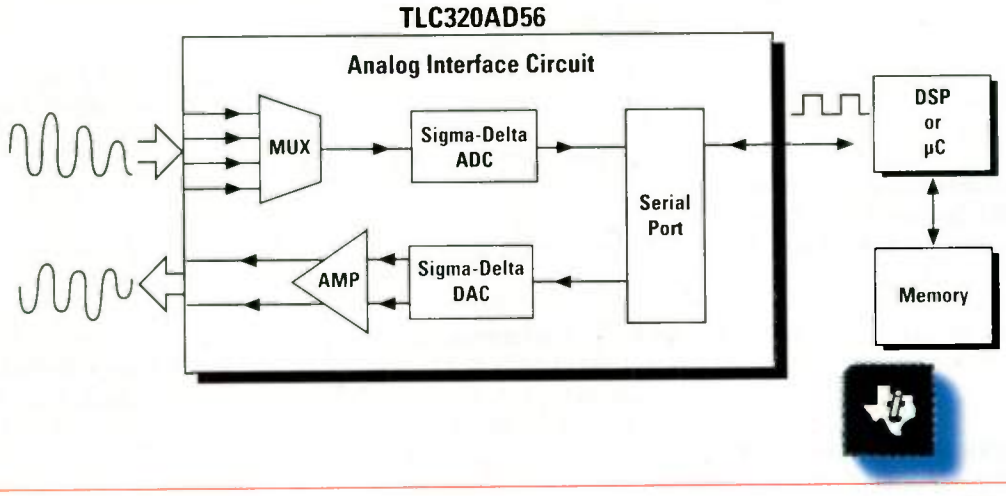

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Fourth IEEE International Conference on Image Processing (ICIP '97), Oct. 26-30. Fess Parker's Red Lion Resort, Santa Barbara, CA. Contact Sanjit K. Mitrea, Electrical & Computer Engineering, University of California, Santa Barbara, CA 93106-9560; (805) 893-3957; fax (805) 893-893-3262; e-mail: mitra@ece.ucsb.edu.

11th Systems Administration Conference (LISA '97), Oct. 26-31. Town & Country Hotel, San Diego, CA. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

19th Annual International Conference of the IEEE Engineering in Medicine & Biology Society, Oct. 29-Nov. 2. Sally Chapman, Secretariat, National Res. Council of Canada, Bldg. M-55 Rm. 393, Ottawa, KIA OR8, Canada; (613) 993-4005; fax (613) 954-2216.

19th International Conference of the IEEE Engineering in Medicine & Biology Society, Oct. 30-Nov. 2. Chicago Marriott Downtown, Chicago, IL. Contact Meeting Management, 2603 Main St., Suite 690, Irvine, CA 92714; (714) 752-8205; fax (714) 752-7444; e-mail: embs97@ieee.org; Internet: http://www.eecs.uic.edu/-embs97.

NOVEMBER

IEEE International Test Conference (ITC), Nov. 1-5. Sheraton Washington Hotel, Washington, DC. Contact ITC, 655 15th St., N.W., Suite 300, Washington, DC. 20005; (202) 639-4164; fax (202) 347-6109.

IEEE Global Telecommunications Conference (GLOBECOM '97), Nov. 3-7. Phoenix, AZ. Contact Nigel Reynolds, 15436 N. First Ave., Phoenix, AZ 85023; (602) 942-5583; fax (602) 942-4542; e-mail: nigelaz@aol.com.

WESCON '97, Nov. 4-6. San Jose Convention Center and Santa Clara Convention Center, San Jose and Santa Clara, CA. Contact Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045-3194; (800) 877-2668; fax (310) 641-5117; e-mail: wescon@ieee.org.

IEEE Intelligent Transportation Systems Conference (ITS '97), Nov. 9-12. Boston Park Plaza Hotel, Boston, MA. Contact Richard Sparks, 8 Richard Rd., Bedford, MA 01730; (617) 862-3000; fax (617) 863-0586; e-mail: r.sparks@ieee.org.

23rd Annual Conference of IEEE Industrial Electronics (IECON '97), Nov. 9-14. Hyatt Regency Hotel, New Orleans, LA. Contact Michael Greene, 200 Broun Hall, Electrical Engineering, Auburn University, Auburn, AL 36849-5201; (334) 844-1828; e-mail: greene@eng.auburn.edu.

Asian Test Symposium, Nov. 17-19. Akita, Japan. Contact Y. Takamatsu, (81) 89 927-9955; e-mail: takamatsu@cs.ehime-u.ac.jp.

DECEMBER

36th IEEE Conference on Decision & Control, December 8-12. Hyatt Regency, San Diego, California. Contact Ted E. Djaferis, Department of Electrical & Computer Engineering, University of Massachusetts, Amherst, Massachusetts 01003; (413) 545-3561; fax (413) 545-1993; e-mail: djaferis@ecs.umass.edu.

Workshop on Internet Technology & Systems (WITS), Dec. 9-12. Marriott Hotel, Monterey, CA. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

JANUARY 1998

Annual Reliability & Maintainability Symposium/Product Quality & Integrity (RAMS), Jan. 20-22. Anaheim Marriott, Anaheim, CA. Contact V.R. Monshaw, Consulting Services, 1768 Lark Lane, Cherry Hill, NJ 08003; (609) 428-2342.

Seventh Security Symposium, Jan. 26-29. Marriott Hotel, San Antonio, TX. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

IEEE Power Engineering Society Winter Meeting, Jan. 31-Feb. 5. Tampa, FL. Contact Jim Howard, Tampa Electric Co., P.O. Box 111, Tampa, FL 33601; (813) 228-4653; fax (813) 228-1333; e-mail: j.howard@ieee.org.

FEBRUARY 1998

IEEE International Solid-State Circuits Conference (ISSCC '98), Feb. 5-7. San Francisco Marriott, San Francisco, CA. Contact Diane Suiters, Courtesy Associates, 655 15th St. N.W., Washington, DC 20005; (202) 639-4255; fax (202) 347-6109; e-mail: isscc@courtesyassoc.com.

IEEE Applied Power Electronics Conference and Exposition (APEC '98), Feb. 15-19. The Disneyland Hotel, Anaheim, CA. Contact Pamela Wagner, Courtesy Associates, 655 15th St., N.W., Suite 300, Washington, DC 20005; (202) 639-4990; fax (202) 347-6109; e-mail: pwagner@courtesyassoc.com.

MARCH 1998

Sixth Annual Embebbed Systems Conference East, Mar. 31-Apr. 2. Chicago's Navy Pier Festival Hall, Chicago, IL. Contact Miller Freeman Inc., 600 Harrison St., San Francisco, CA 94107; (415) 905-2354; fax (415) 905-2220; http://www.embedsyscon.com/.

APRIL 1998

Southeastcon '98, Apr. 10-15. Hyatt Regency, Orlando International Airport, Orlando, FL. Contact Parveen Ward, ECE Dept., University of Central Florida, Orlando, FL 32816; (407) 823-2610; fax (407) 823-5835; e-mail: pfw@ece.engr.ucf.edu.

MAY 1998

IEEE International Conference on Evolutionary Computation, May 3-9. Ankorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@akaska.net.

IEEE International Conference on Neural Networks (ICNN '98), May 3-9. Anchorage, Alaska. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, Alaska 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@akaska.net.

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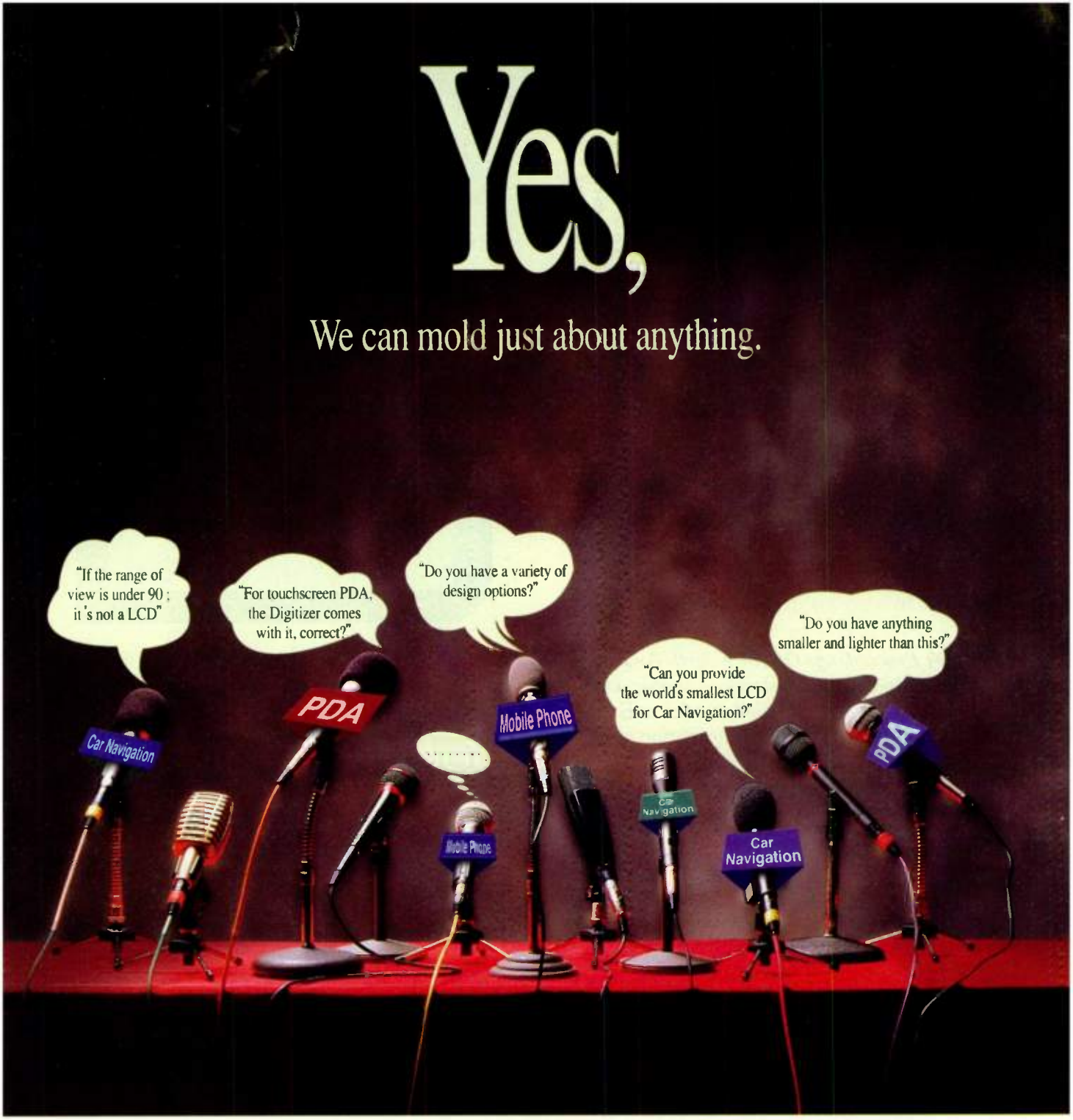

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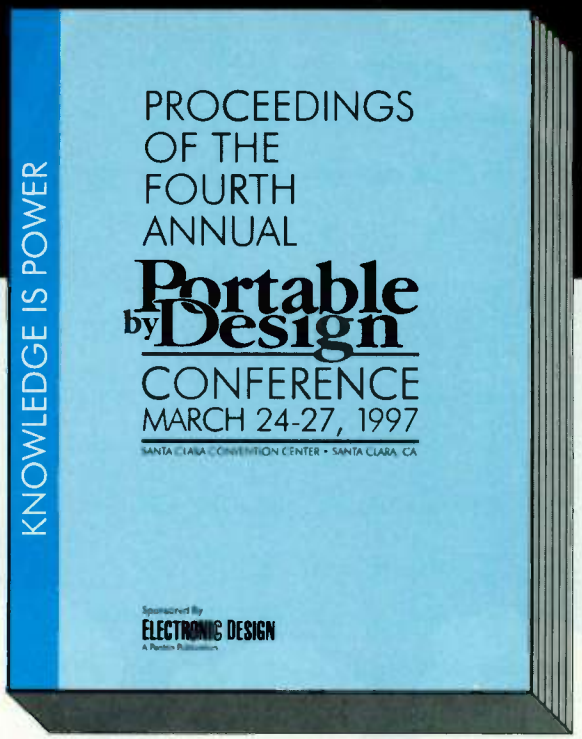

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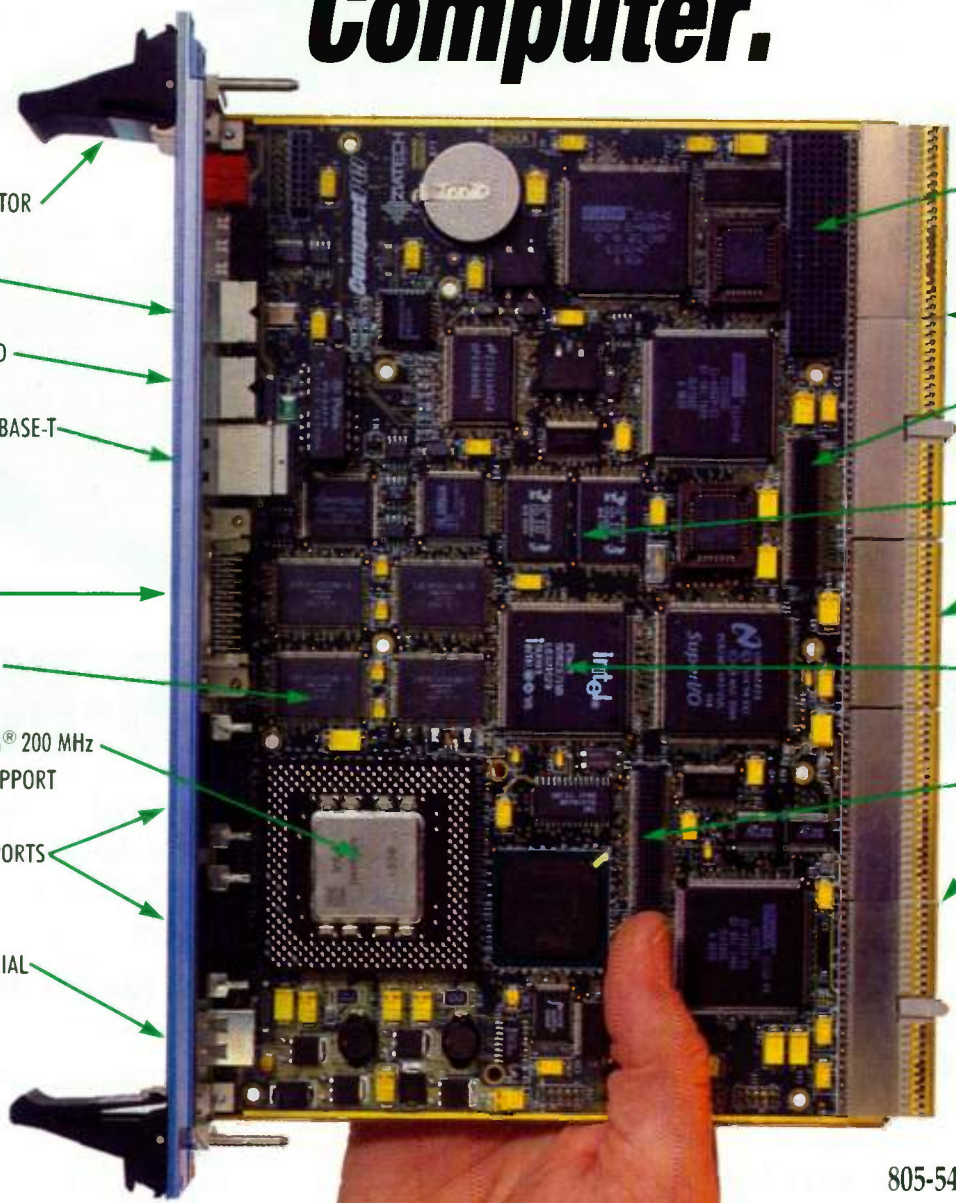

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Fibre Channel Transceiver Ups Bandwidth, Maintains Design Ease

Four Independent 8-Bit Channels Allow Four Times The Amount Of Data To Be Handled, But At A Manageable Clock Frequency.

Richard Nass

Interface discussions over the last few years have often centered on the different flavors of SCSI—where its headed, where the bandwidths will be, and how long it will take to get there. One reason the designers of SCSI products are working so feverishly to develop products is because the competition is heating up. One competitor, IEEE 1394, also known as Firewire, is a serial interface currently specified for 400 Mbits/s operation. But Firewire hasn't yet seen the light of day. A second competitor, and one that is starting to surface in real products, is Fibre Channel, also a serial interface.

Fibre Channel is recognized as a high-end interface, currently for workstations and higher performance systems. Firewire on the other hand, is destined to be a PC-based solution (also for the Macintosh, where Firewire got its origin). To help pave the way for Fibre Channel, Vitesse Semiconductor Corp., Camarillo, Calif., has developed the VSC7214, a four-channel, 8-bit, parallel-to-serial and serial-to-parallel transceiver chip. The VSC7214 is intended for high-bandwidth interconnections between buses, backplanes, and other subsystems.

One of the primary targets for a product like the 7214 is in switches, where high transfer rates are common. Designers of these systems are looking for an alternative to SCSI which, in their eyes, is running out of bus width and speed.

Built For Speed

The designers at Vitesse have been working with Fibre Channel for about six years. The architecture of the company's fourth-generation 10-bit transceiver, the VSC7125, formed the basis of the VSC7214. The 7125 takes 10 bits of encoded data on a 10-bit bus, latches the data into the chip, then serializes it out at a rate of 1 Gbit/s. The part employs a 106-MHz input clock, which is multiplied so the shifting of bits takes place at 1.06 GHz. On the receive side, the opposite takes place. When serial data comes in, a clock-recovery unit uses the edges of the data to determine the clock's basic location, then uses that recovered clock to resample the data and deserialize it on a 10-bit bus.

One of the challenges of this process is the synchronization that must occur. In other words, when the bits are divided amongst the channels, they must reappear in the same order they were sent. Because the paths they take may be of varying lengths, that's not as easy as it sounds. This is one of the functions that's handled transparently by the 7214. The word-synchronization requirements at the receiver end require the transmitter end to generate a word-synchronization event. A word-synchronization event must be sent to each receiver channel after power-up for the elasticity buffer to be properly initialized.

The 7214 handles many of the same functions of the 7125, except that it ties together four transceivers, while the 7125 is a single-channel device. As a result, it can send and receive four times the amount of data in the same amount of time. A common application is where a 7214 in one system commu-

nicates with another system over a copper cable or fiber optics. In this configuration, the 7214 acts as a remote 32-bit bus extender *(Fig. 1)*. A second application, albeit with similar characteristics, is the case where the communications are seen as a remote quad 8-bit bus extender *(Fig. 2)*. Here, four independent 8-bit signals are sent, rather than a 32-bit signal.

Two other applications, while similar to the first two, have the 7214s communicate over a backplane rather than a copper or fiber link. In the local 32-bit bus extender, all the reference clocks are frequency locked. Here, multiple transmitters could be driving a common receiver and multiple receivers can be used in parallel. The receiver output bus is timed to the reference clock, and the transmitter and receiver reference clock are at the same frequency, although probably not in phase.

In the fourth application, the local quad 8-bit bus extender, all the reference clocks in the systems are at the same frequency. Here, multiple transmitters could drive a common receiver. Multiple parts can be used in parallel because the receivers' output bus is timed to the reference clock.

8B/10B Encoding

The functionality of the 7214 is embedded in such a way that it's hidden behind 8B/10B encoders. Fibre Channel signals typically employ an 8-bit word of raw data. The Vitesse technique adds 2 bits to ensure that the signal contains the maximum run length and is dc-balanced. Hence, the name 8B/10B encoding, which is an industry-standard mechanism. One benefit of 8B/10B encoding and decoding is that it improves the quality of the transmitted data, making it easier to recover the clock signal at the receiving end.

The two encoded characters that are added to each transmission character designate a positive- or negative-beginning disparity. Positive disparity means more "ones" than "zeros" in the previously transmitted sub-block of data. Measuring the disparities is what helps maintain the proper dc balance. An equal number of ones and zeros (neutral disparity) in a sub-block pass through the system without changing the signal's running disparity.

The encoder's 10-bit output is fed into a multiplexer that serializes the parallel data using the synthesized transmit clock. The least significant bit is transmitted first. The serial output ports consist of differential PECL output buffers operating at either 10 or 20 times the input clock rate. A loop-back control pin is employed to internally connect the four serial outputs directly to their corresponding serial inputs for on-chip diagnosis.

At the receiver, each channel contains an independent clock-recovery unit (CRU) that accepts the differential serial inputs on the PECL input pins. The CRU then extracts the high-speed clock and retimes the data. The CRU is completely monolithic and requires no external components. It automatically locks on data; if there's no data present, it will lock to the reference clock which helps maintain a well-behaved reference clock. As a result, there's no need for an external lock-to-reference pin.

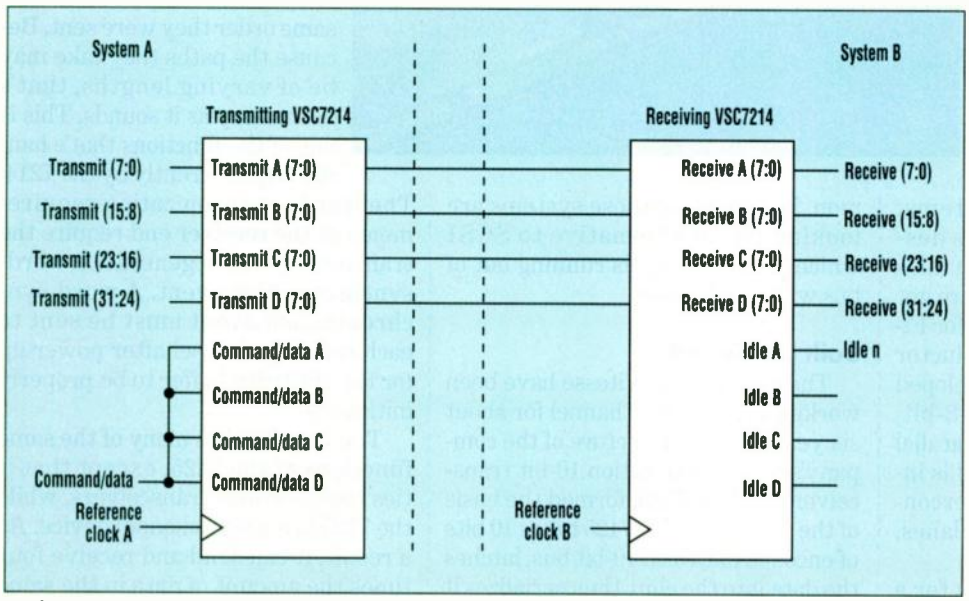
The 7214's unique four-channel design lets the part operate in two different fashions. First, it can operate as four independent 8-bit data streams. The more interesting application comes with the use of 32-bit data that must be moved from point A to point B. The 7214 is responsible for taking the 32-bit data, dividing it into four separate 8-bit streams, then reconstructing it at the receiving end.

Getting In Sync

To accomplish this reconstruction, all four data streams are synchronously latched into the chip on the transmit byte clock and are then serialized. After they go out, they may go on different paths. The traces on the board or the cables may not be the same. Therefore, they will arrive at the receiver at slightly different times. The chip recovers the data on each channel independently, and then employs an elasticity buffer that goes across all four outputs to resynchronize the data from a channel-to-channel perspective. This removes the time delay burden of the cable length. In other words, data can travel on paths of varying lengths without causing an error at the receiving end.

The elasticity buffers on each channel are provided to help realign the serialized data. Even if the four serial inputs are generated from the same reference clock, distances in routing can introduce phase differences between the four channels which require the deskewing that's done in the elasticity buffers.

The data coming from the decoder is clocked into the elasticity buffer by the recovered clock from the channel's CRU. The data is clocked out of the elasticity buffers using



1. The VSC7214 Fibre Channel Transceiver, from Vitesse Semiconductor Corp., can operate as a 32-bit bus extender, communicating with another system over a copper cable or fiber-optic link.

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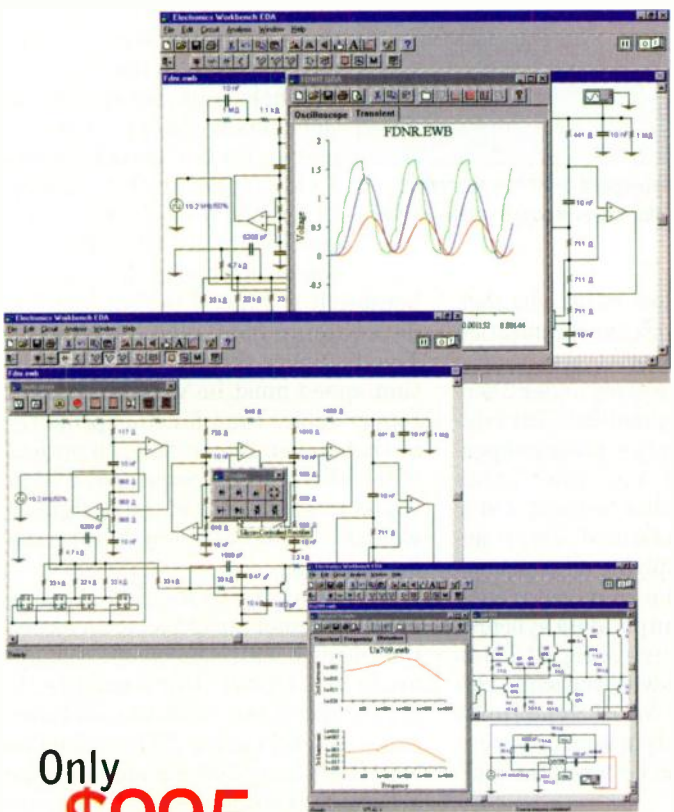

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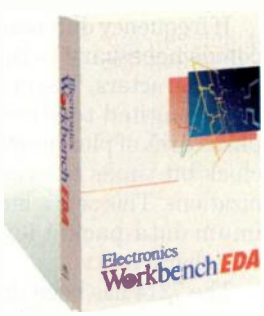

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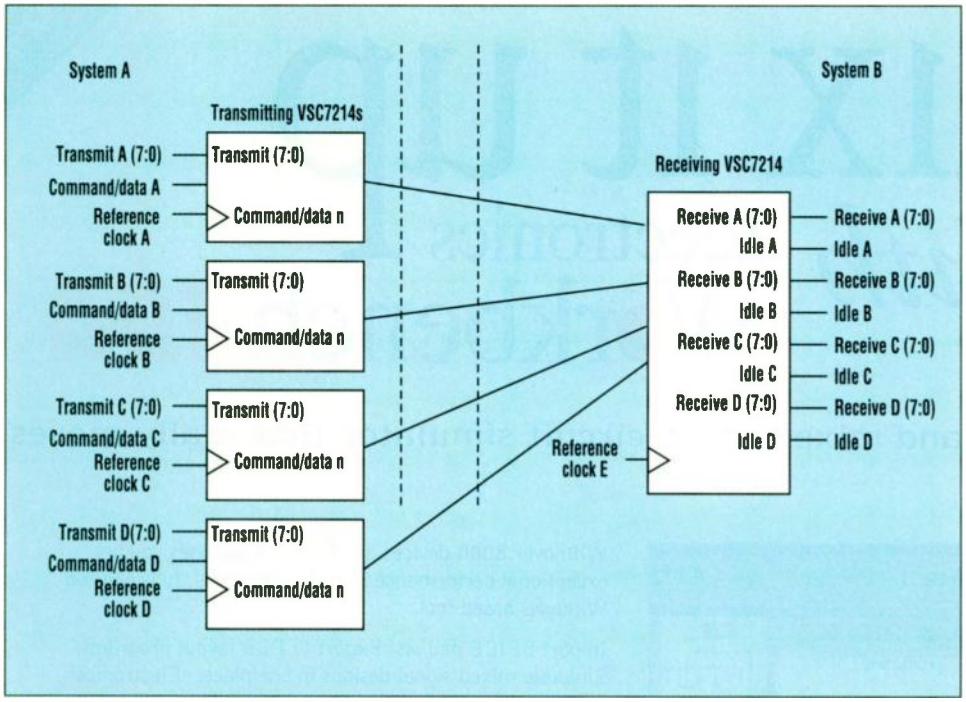

2. A second design option is to view the VSC7214 as four independent high-speed 8-bit bus extenders. Like the 32-bit bus extender, communications with another system take place over a copper cable or fiber-optic link.

the recovered clock or the reference clock. If all four transmitters sending data to the receiving end exhibit the same frequency as the reference clock, the frequency-lock pin is set high. If any of the transmitters are at a frequency that differs from the reference clock, the frequency-lock pin is set low.

If frequency differences occur, it becomes necessary to insert or delete Idle characters. The elasticity buffers are designed to allow a maximum phase drift of plus or minus two serial-clock bit times between resynchronizations. This sets a limit on the maximum data-packet length between Idle characters.

The 7214 has been designed so that realignment of data that was already properly aligned won't cause an error or loss of data. However, if character or word alignment occurs, whereby the relationship of the incoming serial data to the output parallel data changes, the data written prior to the synchronization event could be corrupted or duplicated. This has the potential to cause a system error.

In addition to the elasticity buffers, each channel contains a Loss of Synchronization State Machine (LSSM). The LSSM is responsible for detecting and handling the loss of bit, channel, word, and word-clock synchronization in a controlled manner.

By maintaining a skew under 2 serial-clock bit times, multiple 7214 devices can be used in synchronous operation. By tying multiple 7214s together in a parallel fashion, wider bus widths can be formed. This is accomplished by supplying all transmitting chips with the same reference clock, making all output data synchronous. On the receive side, all 7214s would be supplied with the same reference clock. The Word Sync Input and Word Sync Output signals ensure the synchronization between the multiple receivers.

Multiple Transceivers

In the case of multiple 7214s, Idle characters must be added or dropped from the channels simultaneously. To implement this, one VSC7214 is arbitrarily chosen as the master and its Word Sync Output is driven to the Word Sync Inputs of all the 7214s at the receiving end, including itself. The Word Sync Output is asserted prior to the 7214 adding or dropping Idle characters, ensuring that all the 7214s operate simultaneously.

The maximum packet length is based on both the operating clock frequency and the frequency difference between the transmit and the receive clocks. To increase the maximum packet length, the frequency offset should be decreased, or the reference clock should be increased.

On the transmit side, the 7214's four channels are all clocked simultaneously using a common transmit clock (REFCLK), which also is used as the reference clock for the on-chip multiplying phase-locked loop (PLL).

Another way to get the high-speed data transfer that's offered by the VSC7214 without employing the four channels is to simply turn up the clock frequency and employ a single-channel device. To keep pace with the 7214, the clock would have to be cranked up to 4 GHz. The reason for not going that route is because it is difficult to deal with the data coming in at such a high rate. The distances the data can travel at that speed must be very short, and copper cables can't function properly at that speed. As a result, an optical method would be required, which would raise the cost of the design, as well as considerably lengthening the design time.

By taking the route of the 7214, a board designer should have an easier time dealing with components that operate at 1 Gbit/s. For example, 1-Gbit/s optics are available, and continue to fall in price. There also are copper systems that can operate over a distance of 30 meters.

Price And Availability

The VSC7214 is housed in a 160-pin plastic quad flat pack measuring 28 mm on a side.

The part is sampling now, with production expected to begin shortly. Contact the company for pricing.

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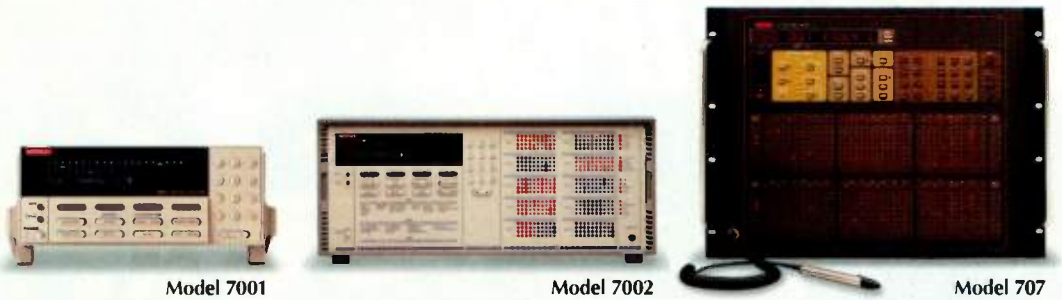

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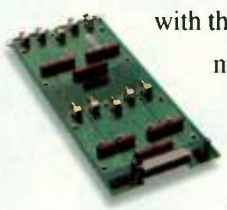

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• Current range	10fA – 5A	10fA – 5A	100fA – 2A	100fA – 2A
• Voltage range	30nV – 1.3kV	30nV – 1.3kV	5μV – 1.3kV	5μV – 1.3kV
• Ohms range	nΩ – TΩ	nΩ – TΩ	nΩ – TΩ	nΩ – TΩ
• Frequency range	DC to 18GHz	DC to 18GHz	DC to 200MHz	DC to 200MHz
• Scanning speed	Up to 225 ch./s	Up to 400 ch./s	200 setups/s	200 setups/s
• Card slots	2	10	6	1
• Main display	VFD	VFD/LED	LED	LED
• Memory locations	100	500	100	100

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PC GRAPHICS WATCH

New Developments In CompactPCI

Joe Pavlat, Vice-President, Pro-Log Corp.; President, PICMG

There's been an explosion of interest in the emerging CompactPCI specification from both suppliers and customers. This new industrial-computer platform is simple in concept, using PCI-based silicon and software in the Eurocard format popularized in the U.S. by the VMEbus. Bringing the leverage of the $200 billion-plus desktop PC market to the industrial and telecommunications markets, CompactPCI offers high performance (132-Mbyte/s transfer rate at 33 MHz and 32 bits; double that at 64 bits), rugged packaging, 3.3-V operation, and the passive-backplane architecture required by mission-critical applications.

The specification was developed in 1995 by a group of suppliers and users under the auspices of the PCI Industrial Computer Manufacturers Group (PICMG), now boasting over 240 members. CompactPCI products are being developed by both traditional PCI passive-backplane industrial-computer suppliers and VMEbus manufacturers.

In 1996, the CompactPCI Technical Committee refined the specification. Revision 2.0 has just been completed, with a number of corrections, enhancements, and improvements. A "short form" on the specification can be downloaded from the PICMG Internet site at www.picmg.com. The most notable change is in the specifying and numbering of connectors. The original specification allowed for both 3U (100 by 160 mm) and 6U (233 by 160 mm) form factors, but little detail was defined for the extra connector space available on the 6U format. This larger format holds promise for the telecommunications and computer-telephony markets, where the extra connectors offer large I/O space out the rear of the card. These three additional connectors have been formalized in location and pin count (315 total) and are already being used for rear panel I/O and sub-buses.

The original 220-pin CompactPCI connector, required for both 3U and 6U boards, has been broken into two 110-pin connectors, called J1 and J2 (J1 is at the bottom). CPU and 64-bit boards use all 220 pins, but 32-bit plug-in boards only need J1's 110 pins. This frees J2 for rear panel I/O in 3U systems, although keying must be carefully employed to avoid plugging the wrong type of card into the wrong socket.

6U boards can have up to three additional connectors, J3, J4, and J5, immediately above J1 and J2. The connectors are numbered sequentially from the bottom. J3 has 95 pins and is located right in the center of the board. J4 and J5, with 110 pins each, are above J3, and are symmetric with J1 and J2, mirrored along the center of the board. All three connectors are available for user I/O or additional buses.

Revision 2.0 has some mechanical enhancements when compared to the original specification. The high insertion and extraction force of a fully-loaded 6U board (over 100 lbs.) was a problem when the standard Eurocard mechanics specified by the original standard were employed. A new standard, borrowed from VME64 (IEEE as 1101.10), defines new connectors that also had high insertion and extraction forces. This standard, now mandatory for CompactPCI, provides an insertion/extraction mechanism whereby each front panel has a lever (two for 6U boards) that cams the board in and out of the chassis and backplane.

The IEEE 1101.10 standard provides for a 1-cm ground pin that contacts chassis ground before any connectors are engaged. This helps to align a board being inserted and also discharges any static or potential difference between the card being inserted and the chassis. Cards also have a ground strip running along the top and bottom that engage grounding clips built directly into the card guides. In addition, there's a provision for an ESD shield between front panels which is intended to reduce emissions and help suppliers meet tough new European CE requirements.

One reason why the telecommunications and computer telephony markets are eager to embrace CompactPCI is the abundance of extra pins that can be used for rear panel I/O, especially on 6U boards. Telecom equipment manufacturers typically like "clean" front panels, with messy wiring such as phone lines moved to the rear. Far from being just an appearance issue, a clean front panel reduces the time needed to replace a failed board and can reduce down time. 6U CompactPCI boards have 315 pins available for rear panel I/O.

Until recently, rear panel I/O had never been standardized. Fortunately, the IEEE has a new specification, called 1101.11, that provides for a standard way of constructing rear panel I/O. The 1101.11 spec allows rear-panel breakout cards, called transition boards, to plug into the rear of the backplane, mirroring the way a front card plugs in, using all the same mechanics. The only difference is the card depth. The CompactPCI community is largely standardizing on an 80-mm card depth.

While already improving the core specification, a number of corollary specifications designed to work with CompactPCI also are in development. Subcommittees are now developing hot-swap functionality; defining standard methods for bridging to extend systems beyond eight slots; combining CompactPCI and VME64 in the same system, and developing a standardized SCSA/HMVIP sub-bus on J4 for computer-telephony applications.

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Compact-Code Processor Shrinks System Memory

With Various Forms of Compact Instructions, Designers Working With Compressed-Code-Processors Must Keep An Eye On Performance.

BILL JACKSON, Silicon Graphics Inc., 2011 N. Shoreline Blvd., Mountain View, CA 94039; (415) 933-3302, and
PAUL COBB, LSI Logic, 1551 McCarthy Blvd., Milpitas, CA 95035; (408) 954-4647.

Years ago, performance at any cost was the focus of most computer system designs. But lately, economy is increasingly becoming the watchword as many systems engineers cross beyond the performance-at-any-cost threshold into the new price/performance realm of lower-cost systems such as network computers (NCs).

Higher chip integration, advanced packaging, and new generations of submicron processing are all helping to bring down systems cost. However, in virtually every system, the big ticket item has historically been system memory to accommodate growing amounts of CPU code. But by reducing the code size, the required amount of system memory also can be reduced.

When opting for a compact-code CPU, systems designers must determine whether the instruction set actually has the savings it promises. During the encoding process, going from a 32-bit instruction set architecture (ISA) to a 16-bit one, there will obviously be some trade-offs. A major one is the latitude many different types of instructions offer to a designer, because there aren't as many bits to specify different operations.

Another issue deals with the number of registers that can be easily accessed. A field in each instruction chooses the general-purpose registers that will be utilized in a certain operation. Occasionally, there can be more than one field per instruction. As instruction width shrinks and the number of bits is reduced, there won't be as many bits left to specify registers. Therefore, the number of general-purpose registers that can be referenced is restricted. This means that performance trade-offs will have to be made.

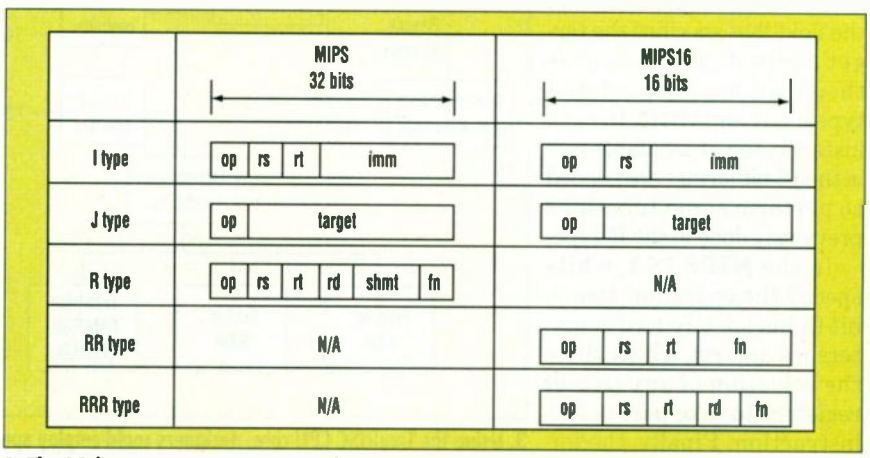
For example, recording a particular software function from 32- to 16-bits may require more than straight mapping. In some cases, those functions will need a sequence of more than one 16-bit instruction. When that operation is executed, it will require more clock cycles, which represents a potential performance loss. Hence, a difficult trade-off in designing a compact instruction set is figuring out whether the lion's share of 32-bit performance can be preserved. Worst case is to develop a highly compact instruction set, but it forces the CPU to jump through so many hoops that performance is dramatically reduced.

Then there is the question of implementing the new instructions in silicon. Using a complex encoding method can likely deliver impressive code size, but the penalty is a slow, arduously long and complex decode operation, which again adversely affects CPU performance because it will drag down the maximum clock frequency the CPU design can achieve in any given process technology.

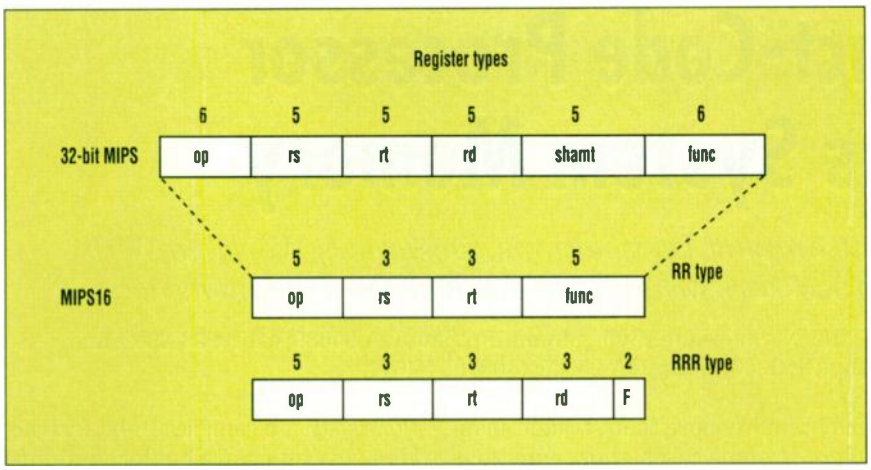
The best of all pragmatic worlds is to carefully select the correct instructions so that a compact 16-bit instruction set can easily be decoded into 32-bit instructions executed by the same CPU. An example is the MIPS16 Application Specific Extension (ASE) used in LSI Logic's TinyRISC TR4101 processor core.

A unique Jump and Link Exchange (JALX) instruction is the linchpin that permits the TR4101 to switch between 32- and 16-bit code. JALX is one of 38 instructions comprising the MIPS16 compressed ASE, a subset of the MIPS ISA. Extend is another new instruction, which allows the definition of special instructions with long opcodes (greater than 16 bits). Extend's major benefit is that it effectively provides 32-bit instructions within a 16-bit program. In many cases, using an extended instruction with the larger associated immediate field can replace the equivalent of up to four 16-bit instructions.

The MIPS16 ASE, which includes support for 64-bit operands, slices the number of 32-bit MIPS instructions by about a third from the original 106 plus



1. The 32-bit MIPS instruction set architecture and the MIPS16 Application Specific Extension are similar. In the Immediate (I) type instruction, one register field (rt) is omitted, leaving only the operation (OP), source register (rs), and the immediate field.



2. The 32-bit MIPS register has a 6-bit OP, three register fields (5 bits each), 5 bits for the shift-amount (SHAMT) field, and a 6-bit function that modifies the basic operation.

32-bit instructions. A set of instruction variances in this format can be expressed in MIPS 32-bit code, but not in the compressed code. Consequently, a multi-instruction sequence is used in these cases to achieve the same effect. Those sequences are utilized sparingly, yet they contribute to overall code savings.

Instruction types between the 32-bit MIPS ISA and the MIPS16 ASE don't change drastically, exemplifying the approach taken to evolve the compressed code from the current MIPS architecture. In the I or Immediate type, one register field (rt) is omitted, leaving only the operation (OP), source register (rs), and the remaining portion of the instruction is devoted to the immediate field *(Fig. 1)*.

The J or Jump type format used for Jumps and Branches is narrowed down, as well, in the field that specifies the target address. The R-type is then split into two related types: RR and RRR. In each instance, fewer available bits in the 16-bit format are needed to perform some functions previously done in the R-type.

In the MIPS ISA, 6 bits specify the operation; two 5-bit fields specify two registers (rs and rt), which allow the selection of any pair of registers to take part in this instruction. Finally, the immediate field is 16 bits wide. In MIPS16 ASE, the operand field is 5 bits, the rt field is omitted, and the rs is pared down to 3 bits, so that only one of eight registers can be selected. Previously, one of 32 registers was employed in 32-bit MIPS. Omitting the rt field means the previous contents of a register are now replaced with the result of the new operation. This isn't necessarily true in 32-bit MIPS. For example, the value of one register is increased by the immediate value in MIPS and then saved in a different register.

Operation code in the Jump/Branch instruction for MIPS16 is 5 bits compared to 6 in 32-bit MIPS. The target field, which specifies a Jump or Branch destination, is reduced from 26 to 11 bits. Consequently, the number of different kinds of Branch specified in 32-bit MIPS is curtailed. With the 6-bit OP in 32-bit MIPS, there can theoretically be up to 64 different types of Branches.

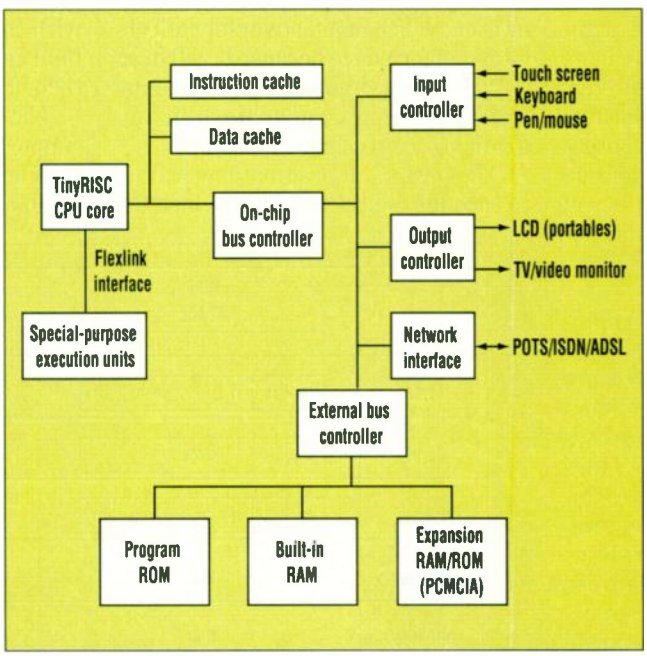
In MIPS16 with a 5-bit OP, there are less than 32. The 32-bit MIPS 26-bit target field permits a wide range for Jumps and Branches, anywhere within a 228-byte range. MIPS16 permits a range of 213. If a Jump needs to be further out than this in MIPS16, a multi-instruction sequence is needed to achieve the same effect.

As for register types, 32-bit MIPS has a 6-bit OP, three register fields, each of which could be any one of 32 registers, 5 bits for the shift amount (SHAMT) field, which specifies instructions that perform arithmetic or logical shifts, and a 6-bit function that modifies the basic operation *(Fig. 2)*. MIPS16 RR-type has a 5-bit OP, 3 bits each for rs and rt, and a 5-bit function. The RRR-type maintains the 5-bit OP and 3 bits each for rs and rt, but adds a 3-bit rd register field, although the function field is restricted to only 2 bits for modification purposes.

Sometimes, instruction steps taking 32 bits in 32-bit MIPS can be directly encoded in either of the RR- or RRR-type 16-bit formats. However, there will be cases in which a combination of instruction steps are attempted. But they won't be accommodated in either RR or RRR. When that occurs, a multi-instruction sequence must be implemented. RR and RRR types will be used extensively for such basic integer manipulation as ANDs, ORs, and XORs.

Saving on memory cost by employing via a compact code CPU, however, is only a part of the overall answer engineers are seeking. Other design issues include architectural flexibility and determining how reusable and scalable an ASIC processor core can be. A design may require additional or different functionality for competitive differentiation.

In this case, the designer may opt for specific cores and



3. Using the TinyRISC CPU core, designers could employ specific cores and building blocks to add the required functionality. In the example of an Internet browsing system, a fast multiply-divide unit can be added to perform several modem tasks in firmware.

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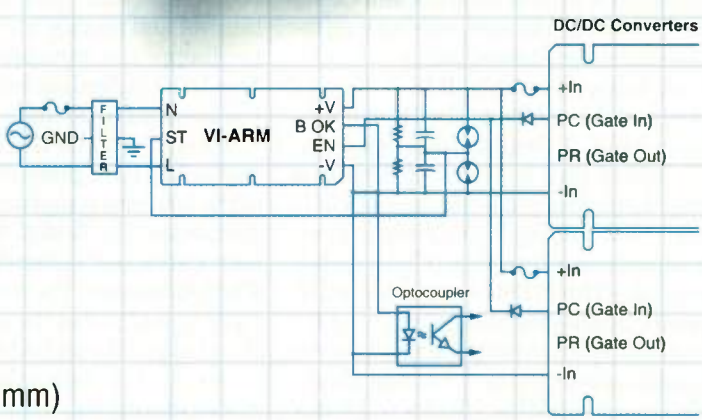

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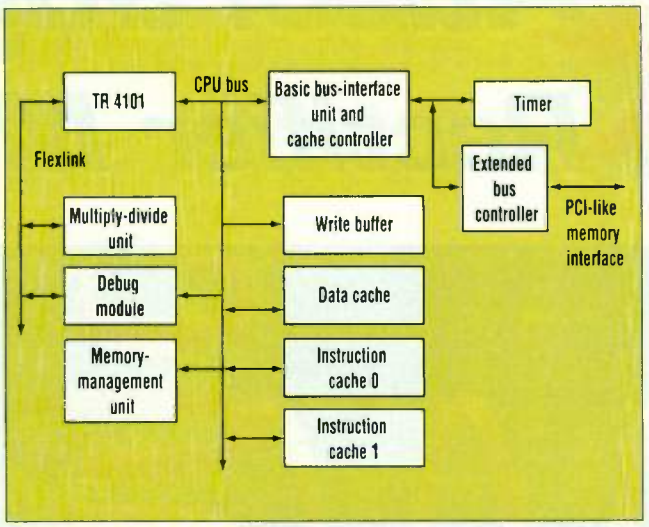
building blocks to add that functionality to the network-interface circuitry of an NC design *(Fig. 3)*. Here, a fast multiply-divide unit (MDU) can be added to perform several modem tasks in firmware. This results in another cost savings because it eliminates a separate DSP chip or modem chip set.

Other functional units the designer can bolt onto the CPU include peripheral controllers like ROM or DRAM and/or video controllers and I/O. In effect, the designer can pack considerable functionality of various flavors onto the network interface such that only a limited amount of passive analog components are needed to complete the interface to a phone or cable line or to a digital subscriber line (DSL). This higher level of integration further cuts the system's costs.



4. The FlexLink interface connects the TinyRISC CPU to the specialized cores, using a building block approach. Such blocks include a bus-interface unit and cache controller, multiply-divide unit, extended bus-interface unit controller, timer, write buffer, debug module, a two-way set-associative instruction or direct-mapped cache, and a data cache.

Utilizing the classic off-the-shelf-chip approach to NC designs precludes this level of flexibility and stunts and the possibility of the system's cost savings. As for the ASIC core approach, many chip vendors label their processor cores as reusable. But they also lack this critical flexibility and cost savings because those RISC cores embed the integer unit (IU), multiplier, memory management unit (MMU), and cache controller into the core, making it an inflexible, self-contained unit.

A truly reusable RISC core is stripped down to only the IU and register filter. A flexlink interface is included to give systems designers a way to partially customize the CPU core, thus making it extendible. Next, a coprocessor interface (COP) turbocharges the RISC core's compute power by allowing designers to tightly connect special-purpose processors. Lastly, access to the CPU bus allows different building blocks to be designed around the CPU. Consequently, considerable latitude is provided for designing with various cores and building blocks to comply with specific NC designs.

The TR4101's flexlink interface is the linchpin for the reusability feature, which can extend the standard MIPS instruction set to any of a number of other different instructions. Typical instructions that could be added to the MIPS core include multiply-add, multiply-subtract, find first set bit, find first clear bit, and saturate instructions. It also can be used for multiple-cycle instructions, although it's more appropriate for single-cycle instructions.

The flexlink interface is a carte blanche for selecting and bolting on to the CPU any number of functions such as a multiplier, barrel shifter, or pixel-manipulation engine. This way, the NC designer can open up the instruction set and modify it without having to change the core processor logic. TinyRISC's flexlink interface allows the designer to do that.

Here's how the flexlink interface works. The CPU presents two subfields of the instruction register and rs and rt operands at the flexlink interface when each instruction's execute stage starts. Flexlink decodes the instruction, executes it, and writes the results back on the rd bus at the end of the cycle.

The CPU handles the register-file update during the write-back stage. If the instruction needs more than one cycle, the flexlink can either stall the CPU using the normal stall mechanism or alternately write the results into its own holding registers, which need to be read later with some user-defined flexlink instructions.

The RISC CPU core should contribute cost savings and efficiencies, as well as scalability. The TR4101 offers a cost-efficient building block approach for implementing integrated system-on-a-chip designs. It can run either 16- or 32-bit instructions on the same processor and operate with a combination of blocks and modules including: Basic bus-interface unit and cache controller, multiply-divide unit, extended bus-interface unit controller, timer, write buffer, debug module, a two-way set-associative instruction or direct-mapped cache, and a data cache *(Fig. 4)*.

Cygnus offers tools that support the MIPS16 ASE. They are based on the Open Software Foundation (OSF) GNU tool chain. Cygnus has announced its intentions to be a provider of the assembler, compiler, linker, locator, and architectural simulator for the MIPS16/TinyRISC architecture. These tools are available free via the Internet.

The transition from a 32-bit MIPS development environment to that of MIPS16 is made simple. The software developer can begin with a 100 % MIPS application, and step-by-step convert the routines to MIPS16. Compilers, linkers, and debuggers have full support for both instruction formats. A flag to the compiler controls whether it generates 32-bit MIPS or MIPS16 instructions. The remainder of the code-development process, which includes linking and debugging, is the same for both MIPS binaries, MIPS16 binaries, and mixed binaries.

Bill Jackson, Manager, Market Development, Embedded Applications, holds a BSEE from the University of Pittsburgh and an MBA from Boston University. Paul Cobb, Applications Engineering Manager at LSI Logic, is responsible for worldwide design coordination and supervision of the company's MIPS-based 32-bit MiniRISC and TinyRISC microprocessor designs.

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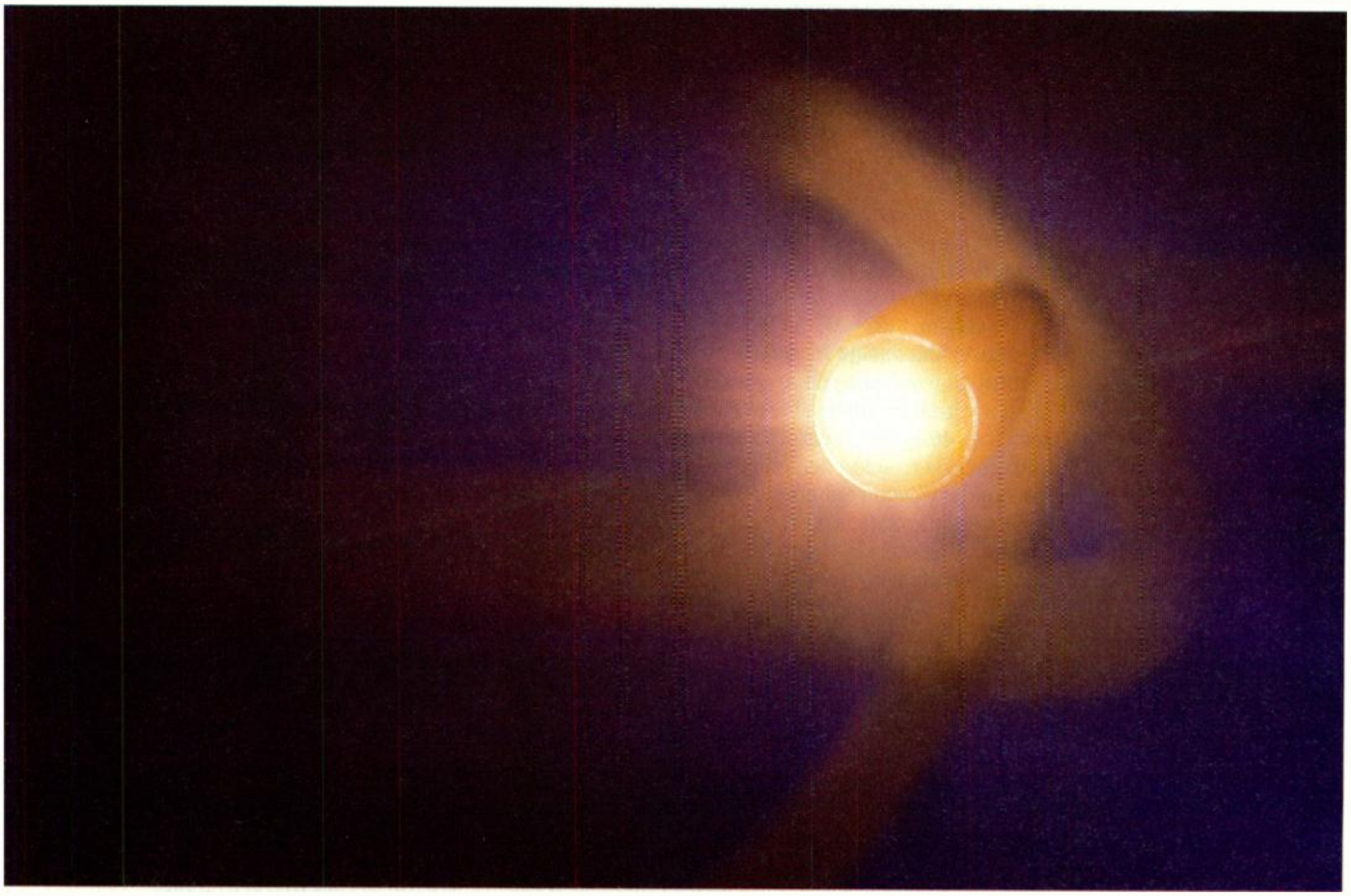

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WHAT'S ON BOARD

Easing the design of MMX-enhancement Pentium systems, the Spectrum CPU module from MicroModule Systems Inc., Cupertino, Calif., gives designers a complete CPU subsystem on a 49-by-54-mm daughtercard. Measuring just 5-mm thick, the module is available in three speed grades—clock rates of 133, 150, or 166 MHz—and is pin-compatible with the company's previous-generation Pentium modules. Each module contains the Pentium CPU, a PCI chip set, 256 kbytes of secondary cache memory, tag RAM, and a temperature sensor. The module's compact format lets designers create wearable and embedded systems that can deliver top-notch audio, communications, and graphics/video with minimal external support logic. BIOS support is available from IBM, Systemsoft, and Phoenix Technologies. Sample prices for 166- and 150-MHz modules are $1679 and $1239, respectively. Contact Howard Green, (408) 864-5986; http://www.mms.com.

Taking control of the CPU subsystem design for space-critical applications, designers at Intel Corp., Santa Clara, Calif., have crafted the Mobile Module, a pre-assembled CPU subsystem building block. The module measures 2.5 by 4 by 0.4 in., and uses two 140-pin connectors to provide the motherboard-to-module interface. Intended to solve design issues such as data flow between the CPU and the secondary cache memory, low-voltage power-supply distribution, high operating currents, and thermal management, the modules provide a common set of electrical, thermal, and mechanical interfaces. At the outset, the modules will include the Pentium with MMX extensions; future versions will include the Pentium Pro. The 150- and 166-MHz versions with the MMX Pentium CPUs sell for $428 and $631, respectively, in 1000-unit lots. Both versions include 256 kbytes of secondary cache and the north-bridge portion of the 430TX PCI chip set. Contact Intel at http://www.intel.com or through a local sales representative.

Giving designers a two-chip solution for portables and desktops, the 430TX chip set developed by Intel Corp., Folsom, Calif., is the company's first chip set to incorporate the dynamic power management architecture (DPMA), it can reduce chip-set power consumption by up to 75%. The chip set also supports the ultra-DMA transfer mode for the IDE storage interfaces, thereby improving the playback speed of large multimedia files. In addition, it's the first mobile chip set to support the Universal Serial Bus (USB) and concurrent PCI (PCI 2.1). Other functions include support for synchronous and extended-data-output (EDO) DRAMs, all basic AT-system functions, a real-time clock, an IDE interface, and a general-purpose I/O port. In lots of 1000, the 430TX chip set (the 82439TX and the 82371AB) sells for $34 per set and is available from stock. Both chips come in 324-contact ball-grid array packages. Contact Intel at (916) 356-3104; http://www.intel.com.

A new docking-station chip set provides PCMCIA, Cardbus, and ISA expansion capability, as well as the ability to handle hot docking. Developed by Opti Inc., Milpitas, Calif., the FireFox chip can auto-detect different devices that are hot-inserted into the expansion slots. The chip can detect 3.3- or 5-V PCMCIA cards and docking interfaces, and 3.3-V CardBus cards. The 82C824 FireFox chip will change pin functions accordingly as each interface is detected. Also available for docking-stations is the FireBridge chip set, which provides the PCI docking and the PCI-to-ISA control interface. The FireBridge I (82C814) supports either a 3.3- or 5-V docking interface (the host interface can also use either 3.3- or 5-V levels). Included is an eight-level FIFO buffer that improves system bandwidth by offloading the primary PCI bus through the FIFO. The other chip, the FireBridge 2, supplies the PCI-to-ISA bus control and includes ISA bus-mastering IDE interfaces to support up four drives. The FireBridge 1 is priced at $12 in lots of 10,000, while the FireBridge 2 circuit is priced at $16 in 1000-unit quantities. Sampling will begin in June of this year. Contact Don Clegg, (408) 486-8000; http://www.opti.com.

PCI-PCI Bridge Simplifies Design-In Process

Developers looking to add PCI capabilities to a desktop, workstation, server, add-in card, or docking-station platform can take advantage of the PCI2030 PCI-to-PCI bridge, which offers a transfer rate of 132 Mbytes/s. The device interfaces two 32-bit PCI buses, removing the typical four-slot

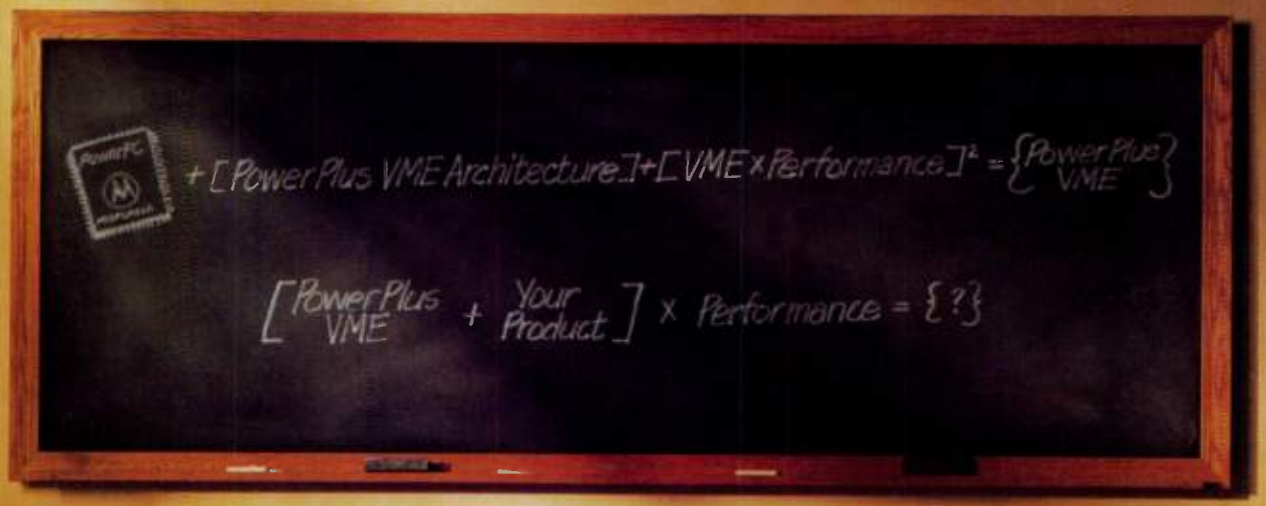
limitation. The bridge also can be used on a multifunction card to buffer the electrical loading the card presents to the PCI bus.

The PCI2030 is compatible with either 3.3- or 5-V environments. With a secondary bus arbiter, the chip supports up to six external masters on the secondary PCI bus. Additional devices can be supported using external arbitration. Programmable single- or double-tier arbitration on the secondary bus gives high-priority devices greater access to the PCI bus.

The part's six low-skew clock outputs can be individually disabled, minimizing the clock skew to just 0.3 ns, giving designers the necessary propagation skew margin. Unused clock outputs can be individually disabled to reduce power consumption. And, by supporting the PCI Clock Run protocol, the IC allows the clock speed to be altered dynamically to lower the power consumption. For multiprocessor environments, a resource-locking feature prevents the CPUs from getting out of synchronization by allowing one CPU to update a shared-memory resource without interruption from the other CPUs in the system.

Housed in a 176-pin thin quad flat pack, the PCI2030 sells for $17 each in lots of 1000.

Texas Instruments Inc., *Semiconductor Group, SC-97009A, Literature Response Center, P.O. Box 172228, Denver, CO 80217; (800) 477-8924, ext. 4500; http://www.ti.com.* **CIRCLE 490**



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It should be easy—it's simple addition. Your final equation is to solve for your product's increased performance. Keep in mind, it will definitely include multiplication. Haven't solved the problem yet? Then call us to find out how our PowerPlus VME Architecture products can add to your product's performance. Or register at our website, and we'll even send you a free poster of all our off-the-shelf VME products. And if one of them isn't suitable, we'll customize one for you. So considering all the possibilities, the range of PowerPlus VME products is—well, you do the math.

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PRODUCT FEATURE

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Low-Cost RAID Controller Brings High-End Features to PCI Bus

An active/active-failover feature is common on high-end, workstation-based, SCSI-to-SCSI disk-array controllers. Thanks to the DAC960SX, that functionality is now available on a low-cost PCI-based board. Transfer rates of 30 Mbytes/s can be sustained for sequential files. For random-access applications, up to 1600 I/Os per second can be performed. In addition, it's possible to pair the board with a second DAC960SX board to further enhance performance and add the active/active failover capability.

Under normal operating conditions, two DAC960SX boards operate in tandem to nearly double I/O performance. If either controller should fail, the active/active-failover function is invoked, and the still-functioning board takes over the tasks previously performed by the failed controller. Any data that's in the write-back cache is protected because it is mirrored between the two controllers' caches.

The DAC960SX is built with three wide UltraSCSI channels; two connect to the disk drives and the third connects to the host. An Intel i960 CPU handles the RAID processing and cache management. An optional daughterboard, the DBI960SX, adds three wide UltraSCSI channels.

The DAC960SX, intended for installation in an external subsystem, is connected using a standard SCSI port. As a result, the board is hardware and operating-system independent and doesn't require any special drivers. With 16 Mbytes of cache memory and a battery backup module, the DAC960SX sells for $2969. When combined with a 5.25-in. housing and an LCD monitoring and configuration panel, the subsystem sells for $4324.

Mylex Corp.
34551 Ardenwood Blvd.
Fremont, CA 94555
(510) 796-6100
http://www.mylex.com.
CIRCLE 554
RICHARD NASS

Miniature LCD Measures 0.25 in. But Projects To A 20-in. Screen

One of the limiting factors of a portable system is the size of the display. The 320-by-240-pixel monochrome Cyber Display is out to eliminate that limiting factor, boasting a 0.25-in. diagonal active area. The miniature display is built with a transmissive active-matrix liquid-crystal-display (AMLCD) technology featuring a resolution that results in sharp, bright images.

In an application, the Cyber Display would be viewed through a lens that makes the display appear as the equivalent of a 20-in. diagonal screen at a distance of 5 ft. from the viewer. The rectangular lens measures 14 by 18 by 7 mm and is placed 17.6 mm from the display and backlight module. When combined with a solid-state backlight, the display consumes less than 70 mW of power, while producing an image brightness of 20 foot-lamberts.

In sample quantities, the Cyber Display sells for $75. Large quantities, available in the third quarter, will cost well below $50 each. A developers kit also is available for $495. It includes

the display, a lens, a backlight, the necessary drive electronics, a power supply, a video cable, and documentation. A color version is in the works as well.

Kopin Corp.
695 Myles Standish Blvd.
Taunton, MA 02780
(508) 824-6696
CIRCLE 555
RICHARD NASS

Digital-Audio-Tape Drive Triples Capacity Of Previous Version To 24 Gbytes

Employing the Digital Data Storage-3 (DDS-3) technology, the STD124000N Digital Audio Tape (DAT) drive from Seagate Technology Inc., can hold up to 24 Gbytes of information on one tape.The company says the drive triples the capacity and doubles the performance of its previous generation drives, the DDS-2.

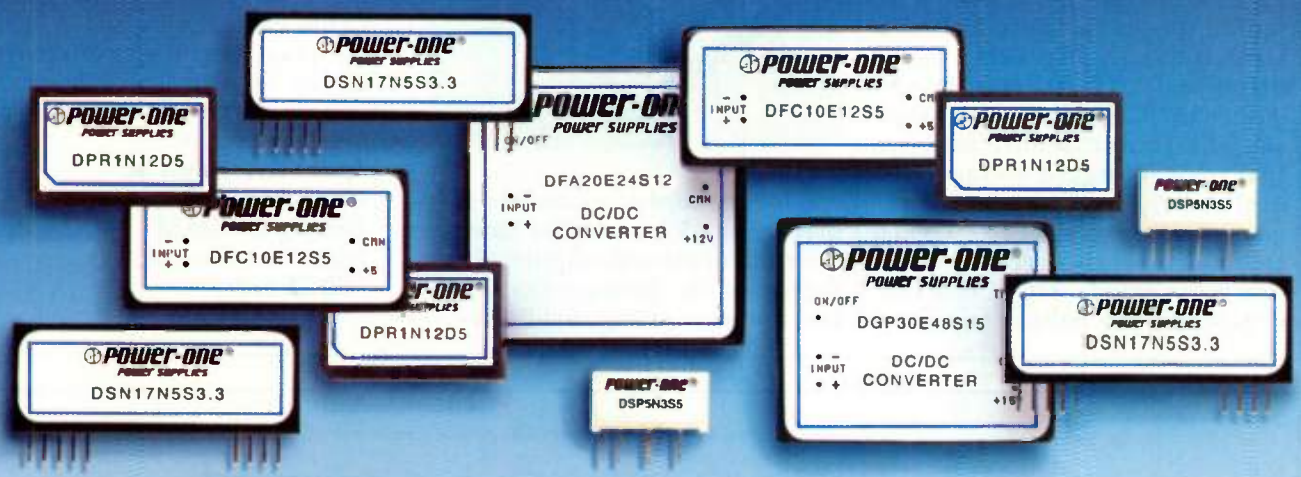
Aimed at backup applications, the STD124000N has a native capacity of 12 Gbytes, which is doubled using a hardware-based compression technique. The drive achieves a data-transfer rate of 2.2 Mbytes/s and is fully read- and write-compatible with DDS-2 and DDS-1 media. A fast SCSI-2 interface is employed.

The improved specifications result from higher performance heads and an improved read channel. Other features include enhanced self-cleaning, energy-saving options, and fewer components, which produces higher reliability.

The DDS-3 advanced metal-particle media incorporates a ceramic layer that coats each magnetic particle to protect against oxidation, making the media more reliable. The media's dual coating supplies a thin magnetic layer that also improves the overwrite and distortion performance. The STD124000N comes in 3.5- and 5.25-in. form factors, as well as an external configuration.

Seagate Technology Inc.
1650 Sunflower Ave.
Costa Mesa, CA 92626
(714) 966-4714
http://www.seagate.com.
CIRCLE 556
RICHARD NASS

DC/DC Just Got Better.



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DFA6	6	9-27, 20-60		•	•		•		•	
DFC6	6	3.5-16		•	•		•		•	
DFC10	10	9-18, 18-36, 36-72	•	•			•		•	
DGP12	12	3.5-16		•			•		•	
DFC15	15	20-60		•			•		•	
DSN17	17	4.5-6, 6.5-15.5	•	•						
DFA20	21	9-18, 18-36, 36-72	•	•			•		•	
DGP30	30	36-72		•			•		•	
Dual Output products provide the indicated Vout as one positive and one negative output										
DSP1	1	4.5-5.5		+/-		+/-	+/-	+/-	+/-	+/-
DFC10	10	9-36, 18-72		+/-			+/-		+/-	
DGP12	12	3.5-16		+/-			+/-		+/-	
DFC15	15	20-72					+/-		+/-	
DFA20	20	9-18, 18-36, 36-72		+/-			+/-		+/-	
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DGP20	20	9-18, 18-36, 36-72		•			+/-		+/-	

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PRODUCT FEATURE

Data sheets on products like these can be found at www.penton.com/ed/

Intelligent Memory Card Complies With CompactFlash Specification

One of the more innovative applications for flash memory involves storage in a digital camera. That's one of the places that the designers of the CompactCard targeted when building the 2-, 4-, or 8-Mbyte card. Built by Lexar Microsystems to the CompactFlash Association specification, the card operates from a single supply at either 3.3 or 5 V.

The card, which measures 1.433 by 1.685 by 0.130 in., is about one-fourth the size of a standard PC Card. It weighs 0.5 g. Other potential applications for the memory card include handheld computing devices and industrial embedded platforms that require rugged storage. The card can withstand an operating or non-operating shock of 2000 Gs and operates properly over a temperature range of 0° to 60°C. The MTBF is rated at one million power-on hours.

The CompactCard contains an intelligent ATA interface, eliminating the need for flash file systems or device drivers. As a result, users can

employ the card as a standard disk drive. The ATA controller handles the unique characteristics of the flash memory, thereby relieving the host software of any modifications.

The intelligent architecture also includes background pre-erase of flash-memory blocks, high-speed host-to-buffer burst transfer rates, buffering of the data to and from the flash memory, and logical-to-physical sector addressing. The card is built with NAND-type flash memory supplied by Samsung Electronics and Toshiba.

The CompactCard offers a write performance of 1.0 Mbytes/s, a read specification if 3.0 Mbytes/s, a write current of 37 mA, a read current of 32 mA, and a standby current of less than 1 mA. Data can be burst from the host at a rate of 20 Mbytes/s. The 4-Mbyte card sells for under $60 in large quantities. Lexar Microsystems also manufactures flash-based PC Cards and flash modules for embedded applications.

Lexar Microsystems Inc.
47421 Bayside Pkwy.
Fremont, CA 94538
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CIRCLE 557
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WRH

4.5-Gbyte Disk Drive Spins At 7200 RPM

The 4.5-Gbyte Barracuda 4XL hard-disk drive is chock full of high-end features, starting with a spin rate of 7200 rpm. It also includes magneto-resistive heads, a PRML read channel, an embedded servo, and an Advanced SCSI 2 architecture. The internal data rate is 140 Mbits/s. The 1-in. high drive stores its data on just four platters, which helps keep the MTBF rating at one million hours. Various UltraSCSI interface solutions are offered, from an 8-bit, 20-Mbyte/s narrow channel to a 16-bit, 40-Mbyte/s wide channel. A single-connector attachment (SCA) also is available for RAID applications. Samples of the Barracuda 4XL 4.5-Gbyte hard-disk drive are available now. Production will start before the end of the second quarter. A 2.2-Gbyte model also is available.

***Seagate Technnology Inc.**, 920 Disc Dr., Scotts Valley, CA 95066; (408) 439-2859; http://www.seagate.com.* **CIRCLE 473**

PICMG-Based Industrial SBCs Hold Alpha CPU

A family of single-board computers, based on the 64-bit 21164 Alpha microprocessor, is aimed at large computer-telephony applications. Built to the PICMG specification, the boards fit into the Digital Modular Computing Components (DMCC) family. The host Alpha processor run s at 366 or 500 MHz. The board integrates up to 2 Mbytes of synchronous RAM, up to 512 Mbytes of main memory, and all standard I/O ports. DMCC server-management functions include a PCI interrupt accelerator and an operator control panel. Operating system support currently includes Unix, Windows NT, and VxWorks. Support for OpenVMS will follow by the end of the summer.

Two 19-slot backplanes are available to operate with the DMCC family of Alpha-based single-board computers. The slot combinations are 13 PCI, five ISA, and one CPU, or 10 PCI, eight ISA, and one CPU. A 20-slot enclosure can be deployed in either rack-mount or tower configurations.

***Digital Equipment Corp.**, Maynard, MA 01754; (800) AXP-4-VME; http://www.digital.com.* **CIRCLE 474**

GOLFING NEWS **by Mike Hensen**

Ex-Navy engineer puts armor-piercing material on a driver. Outguns steel and titanium on distance.

PGA professionals outhit their titanium drivers by 25 and 50 yards

YALESVILLE, CT – And you thought steel and titanium were tough. Well, steel and titanium can't penetrate an armor-plated tank or sink a warship. To pierce their defenses the military had to make something so powerful it had to keep it secret... so powerful that once it was declassified, some innovative company would surely apply it to the face of a golf club to add distance.

One has and it doesn't bode well for golf's current state-of-the-art metal, titanium. A well-known professional outhit his own titanium driver with the new club by 25 yards. Another Tour professional outhit his titanium driver by almost 50 yards!

The new driver is the creation of a former Naval Ordnance engineer who used to apply the material to the tips of torpedoes, and a small golf company in Connecticut. Together, they have adapted it to the hitting surface of a steel driver. They say

"The harder it's hit, the farther it goes."

their adaptation is proprietary and a patent has been applied for.

All the company will say is that the new metal is a sort of ceramic titanium, ceramic for hardness and titanium for strength and lightness. The material – called TC-20 – is twice as hard as steel and 70% harder than titanium. It whacks a ball with such force that at club-head speeds of 120 MPH – the level of longball champs – the new club split the cover on some balls.

TC-20 also increases a golfer's accuracy by holding the ball on the face of the club four times longer than steel and titanium. This makes off-center shots far less likely to hook or slice, and allows a good golfer to draw and fade the ball with more control. I watched a top Tour professional test the club at a PGA Tournament. Here's what he told me.

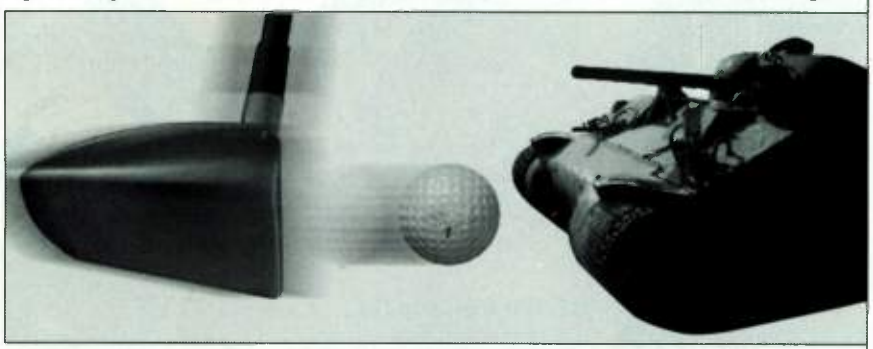
"I'm hitting the ball 30 yards past my driver and controlling it like a five-iron. You see all my competitors smiling at me? That's not admiration. It's worry."

The company's Research Director explained the club this way...

"It's basic physics. The harder you hit a ball, the farther it goes, and Condor® Armor-Pierce (the club's name) clobbers a ball like a battering ram. It not only launches it farther down range than any thing else on the market, its TC-20 face reduces a ball's normal spin rate. A lower spin rate keeps the ball flying longer and at a lower trajectory for a longer roll.

"Condor Armor-Pierce also reduces *abnormal* spins that cause off-center shots to hook and slice. That's why he's outhitting his titanium driver by 30 yards and controlling 300-yards shots like a five-iron. It's a pleasure to watch, isn't it?

"You know who he is? (I said I did.) He loves the club. I wish he weren't tied up with a big company. He would shoot in the 50's with the Condor Armor-Pierce. Imagine that on TV. Titanium drivers would be history before he changed shoes, especially at Condor Armor-Pierce's price."



Once-secret TC-20 is used on shells to penetrate tanks and warships, and on spacecraft to withstand heat on re-entry. It is twice as hard as steel, 70% harder than titanium.

The once-secret TC-20 is backed up by a stainless steel head the same size as a titanium driver (250 cc's) for maximum forgiveness. To maximize clubhead speed it comes with a 45-inch, 100% graphite shaft.

You can test the Condor Armor-Pierce for 30 days by calling **1-800-285-3900** any time or day or faxing 1-203-284-1623. Or you can send your name, address and check (or cc number and expiration date) to NGC Golf (Dept. TC-24), 60 Church St., Yalesville, CT 06492. The club cost only $119.00 (a fraction of the cost of titanium clubs) and you can add the 3 and 5-woods for only $99.00 each. Shipping is only $10.00 no matter how large your order. Specify regular or stiff flex, men's or ladies', when your order. Right-handed only. There's a 30-day money back guarantee, if the clubs are returned undamaged.

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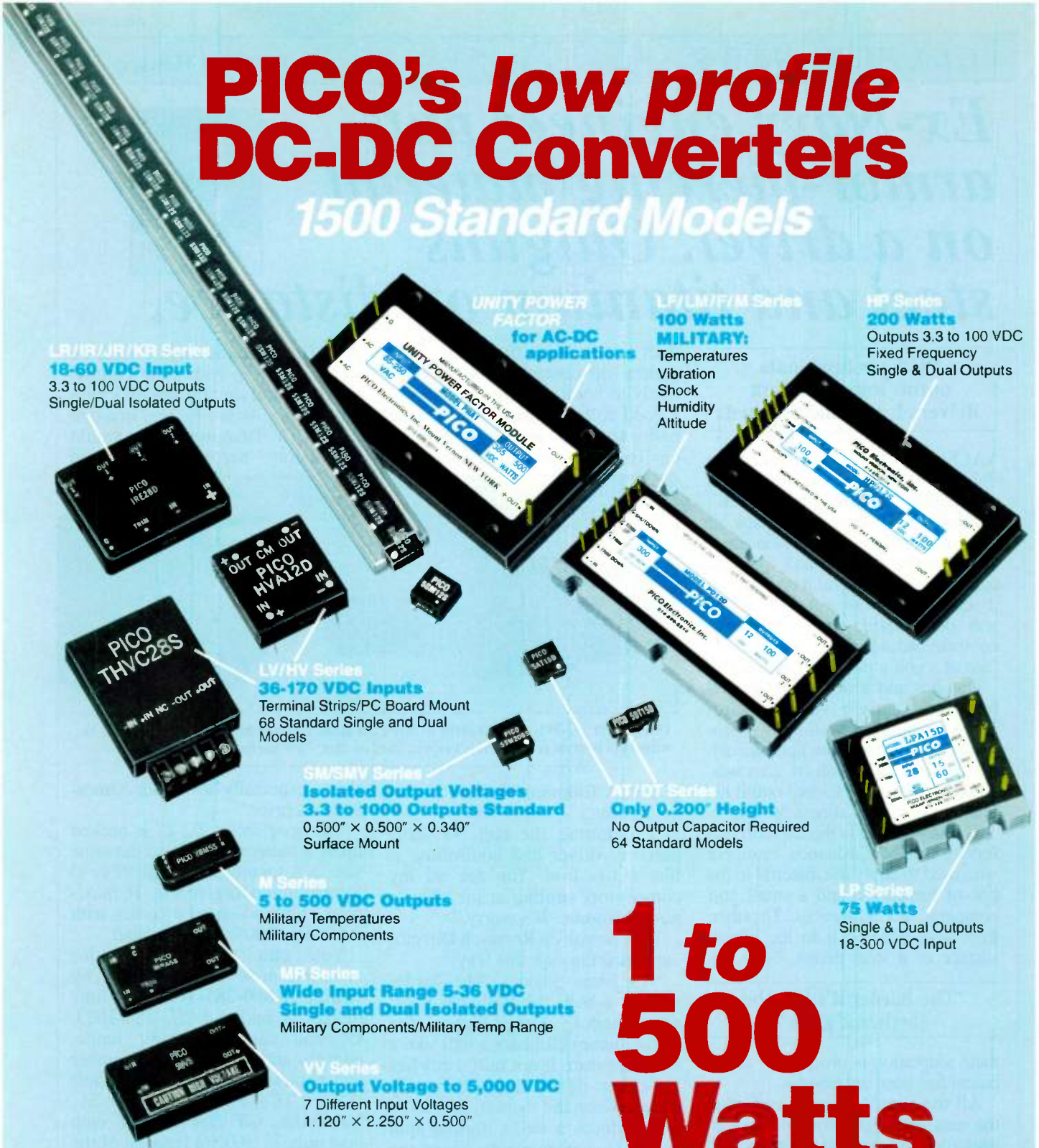

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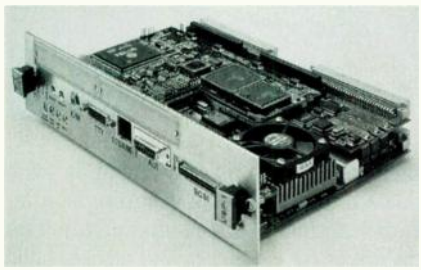
Data sheets on products like these can be found at www.penton.com/ed/

Sun-Compatible Subsystem Holds 200-MHz UltraSparc CPU

The USP-1 is a VME64 processor subsystem built with a 167- or 200-MHz UltraSparc 1 microprocessor. Designed as a two-board set, the subsystem is 100% Sun-compatible. A third



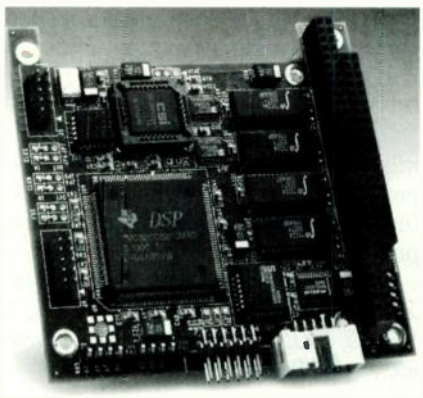
VMEbus slot can be employed to hold one or two SBus controllers, although the subsystem holds two SBus boards without the optional controller. A crossbar memory architecture supplies 600 Mbytes/s of sustained bandwidth combines with dual Ethernet and SCSI-2 ports to suit the subsystem for database-retrieval, audio, video, and imaging applications. Up to 1 Gbyte of DRAM can be employed using screw-down memory-expansion modules. These modules have a greater shock and vibration tolerance than standard SIMMs. Also included is 1 Mbyte of user-definable flash memory.

Themis Computer, *3185 Laurelview Ct., Fremont, CA 94538; (510) 252-0870; http://www.themis.com.*

CIRCLE 475

DSP Modules Fit PC/104 And AT/ISA Form Factors

Two low-cost, high-performance DSP modules, based on the Texas Instruments TMS320C32 chip, are available in PC/104 and AT/ISA form factors. Called the Spirit-32, the modules offer DSP capabilities and up to four channels of the analog-to-digital and digital-to-analog conversion. The modules are suited for such embedded applications as active process control, telecommunications testing equipment, and instrumentation. The Spirit-32 series features two banks of internal 256-by 32-bit zero-wait-state SRAM, 64-by-32 bits of cache memory, and a serial interface off the main memory bus. The modules can be customized to meet specific application needs. Options in-



clude processor speed, memory size and type, flash ROM size, digital I/O interfaces, and other custom interfaces. Memory is expandable to 2 Mbytes. Also featured is a suite of development tools. Available immediately, a 60-MHz module sells for $795 each in lots of 100.

RadiSys Corp., *5445 NE Dawson Creek Dr., Hillsboro, OR 97124; (503) 615-1100; http://www.radisys.com.*

CIRCLE 476

Squeeze 72 Mbytes Onto One Flash Chip

Designers of embedded systems looking for an integrated high-capacity storage solution can take advantage of the DiskOnChip Series 2000, which stores up to 72 Mbytes in one 32-pin JEDEC package. The flash-memory device also is available in 2-, 4-, 8-, 12-, and 24-Mbyte versions. The DiskOnChip fits into the standard EPROM socket that appears on many embedded CPU boards and motherboards. The part contains the company's Flash Transition Layer (FTL) firmware and TrueFFS transparency for hard-disk emulation and compatibility. Write speeds of 250 kbytes/s are attainable, as well as a read speed of 700 kbytes/s and burst-transfer rates of 5 Mbytes/s in either direction. Power specifications include 60 µA in standby mode, 25 mA in read mode, and 30 mA in write mode. The DiskOnChip operates from a single +5-V supply. The operating temperature range is 0° to 70°C, with enhanced (-25° to 75°C) and extended-temperature (-45° to 85°C) versions planned.

M-Systems Ltd., *4655 Old Ironside Dr., Suite 200, Santa Clara, CA 95054; (408) 654-5820; http://m-sys.com.*

CIRCLE 477

Data sheets on products like these can be found at www.penton.com/ed/

Flat-Panel Display Fits In A Drawer

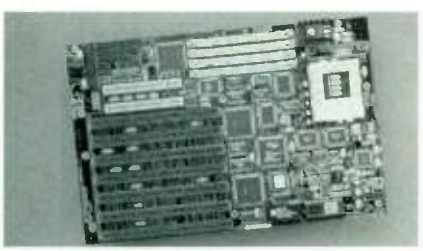
One way to conserve space is to mount your monitor inside a drawer. That's exactly what is accomplished by the VueMiser series of industrial drawer-mount 12.1-in. flat-panel displays. De-

signed to replace color CRTs in standard 19-in. instrument racks, the VueMiser reduces front-panel height from 10U to 1U and power consumption from 17 to 24 W. Displays are available with resolutions from 640-by-480 to 1024-by-768 pixels. Options include keyboards, trackballs, and resistive touch screens. On-screen menus offer easy set up and adjustment. Available now, prices for the VueMiser display system start at $3040.

National Display Systems, *761A University Ave., Los Gatos, CA 95030; (408) 395-8688.* **CIRCLE 478**

Pentium Motherboard Offers Six EISA Slots

Six full-length EISA slots are the key feature of the Galileo 1 Pentium motherboard. The board also includes a ZIF socket to hold a CPU running at 75 to 200 MHz, 16-bit audio, on-board



Ultra SCSI, and a flash-based AMI BIOS compatible with all major operating environments. The EISA bus offers a maximum bandwidth of 33 Mbytes/s. A parallel and two serial ports are included, as well as a mouse port and an audio port. The Galileo 1, built to a standard Baby AT form factor, is suited for such applications as video or multiport I/O servers and high-speed scanners. The board supports up to 128 Mbytes of DRAM using SIMMs. Available immediately, prices start at $399 in lots of 1000.

Integrated Business Computers, *2685C Park Center Dr., Simi Valley, CA 93065; (805) 527-8792; http://www.ibc.com.* **CIRCLE 479**

Low-Cost Monitor Measures 21 in.

The Visual Sensations family of monitors has a new member, the VS-21, a 21-in. modes compatible with both PCs and Macintoshes. The display is suited for applications that require detail and high-end graphics, such as desktop publishing, imaging, and computer-aided design. The VS-21 delivers 1600 by 1200 pixels at a flicker-free refresh rate of 75 Hz, a 0.28-mm dot pitch, and an automatically adjusting horizontal scanning frequency from 28 to 117 kHz. The VS-21 complies with the Swedish MPR-II standard for radiation emissions, and meets the U.S. EPA Energy Star and VESA DPMA standards. Available immediately, the VS-21 sells for $1599.

KDS USA, *12300 Edison Way, Gadren Grove, CA 92841; (714) 379-5599; http://www.kdsusa.com.*
CIRCLE 480

Core-Logic Chip Works With StrongARM Processor

A single-chip core-logic device, the 21285, enables the StrongARM SA-110 microprocessor to operate in PCI-based environments. The device makes the StrongARM processor suitable for embedded applications, such as networking servers and clients, office automation, storage control, telecommunications, and PC add-in cards.

Features of the 21285 include a synchronous DRAM interface, a flash ROM interface for device initialization, DMA and interrupt controllers, programmable timers, an intelligent I/O message unit, parallel and serial ports, and a PCI bus arbiter. The chip also supplies the four clocks and chip selects needed for SDRAMs. A complete tool set is available to aid in building a StrongARM-based design. This includes an evaluation module and a software-development kit. The kit adds a compiler, linker, assembler, debugger, and functional simulator model. Sam-

ples will be available by the end of the second quarter, with volume production starting in the third quarter. The 21285 StrongARM core-logic chip sells for $19.50, in lots of 10,000.

Digital Equipment Corp., *Maynard, MA 01754; (508) 568-5102; http://www.digital.com/semiconductor.*
CIRCLE 481

Portable Computer Holds MMX-Enabled Processor

Intel's MMX technology is now available on a mobile platform. The Extensa 660 series is built with an MMX-enabled 166-MHz Pentium processor, up to 80 Mbytes of EDO DRAM (16 Mbytes comes standard), and 256 kbytes of secondary cache memory. The main storage comes in the form of a removable hard-disk drive, holding either 1.35 or 2.1 Gbytes. The internal peripherals are connected to a 33-MHz PCI local bus, while external expansion is done through a pair of CardBus-ready PC Card sockets. One socket also supports Zoomed Video. Two color display options are available—a 12.1-in. Super VGA DSTN LCD or a 11.3-in. Super VGA TFT LCD. Each offers a maximum resolution of 1024 by 768 pixels. The video subsystem is enhanced using a NeoMagic MagicGraph 128ZV chip. A PCI card expansion slot lets users connect a peripheral card directly to the PCI bus. This can be used for such applications as Fast Ethernet, FireWire (IEEE 1394), or MPEG-2 video. Batteries with two chemistries are available—NiMH or Li-Ion. Available now, the Extensa 660 series of portable computers starts at $3299.

Texas Instruments Inc., *P.O. Box 6102, MS 3242, Temple, TX 76503; (800) TI-TEXAS; http://www.ti.com.*
CIRCLE 482

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White Mountain DSP offers a full emulation and debug tool set for SHARC development. Another first in the industry, the Mountain-ICE/WS emulation system for Sun workstation platforms (shown) provides complete multi-DSP debugging support for both the ADSP-21060 (4 Mbit) and ADSP-21062 (2 Mbit) SHARC devices. And you know White Mountain DSP will continue to expand its range of options to enable you to work with SHARCs and not get bitten.

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White Mountain DSP, Inc., 20 Cotton Road, Nashua, NH 03063 (603) 883-2430 Fax: (603) 882-2655 E-mail: *Info@wmdsp.com*

READER SERVICE 185

Avoiding Design Pitfalls In Multiprocessor DSP

Overall System Performance Can Be Seriously Affected If Several Factors Are Not Addressed In The Design.

GORD WAIT, Spectrum Signal Processing Inc., 100-8525 Baxter Pl., Burnaby, British Columbia, Canada V5A 4V7; (604) 421-5422; fax: (604) 421-1764.

Applications that use digital-signal processing (DSP) methodologies have become commonplace in today's world of ever-more sophisticated industrial and consumer products. DSP is, essentially, the application of mathematical operations to a series of digital samples representing physical-world signals such as audio waves, or complex analog-sensor samples such as ultrasound or CAT-scan sensor arrays.

At one end of the spectrum, relatively simple single-chip DSP designs are used in devices such as modems and cellular phones. These DSP subsystems are usually driven by size, cost, and power constraints. On the other end of the spectrum are high-performance, multiprocessor, multiboard, DSP systems used for the real-time (or near real-time) processing of massive-signal input streams. Examples of that application include telephone switching or substation equipment, medical imaging systems, and seismic analysis systems.

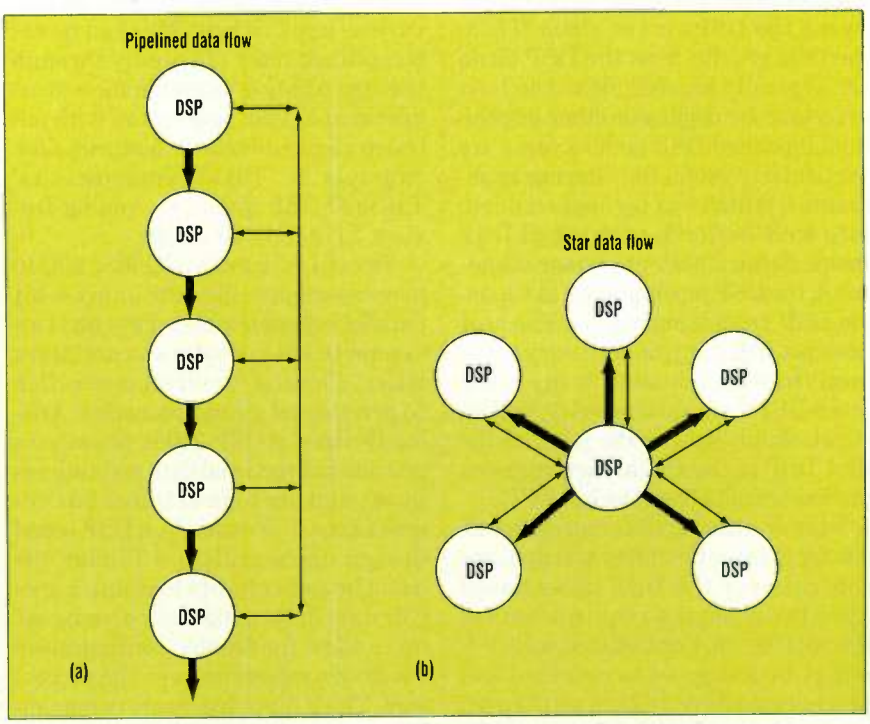
The design of high-performance DSP systems for today's most-demanding applications requires the juggling of a variety of factors. Designers of high-end, multiprocessor DSP systems must be aware of at least four significant pitfalls that can dramatically impact overall system performance:

- Optimizing data flow through the system.
- Dealing with host system bus trade-offs.
- Choosing the best-fit, real-time operating system (RTOS) for their application.
- Ensuring optimal interface design for handling inputs from the A/D array.

These issues become more important when the multiprocessor DSP system is intended to provide enough flexibility and programmability to meet a variety of high-performance end-use applications. The creation of such commercially adaptable DSP systems requires that the underlying architecture be flexible, scalable, and cost effective without sacrificing any of the raw performance and robustness needed to meet specific application requirements.

Optimizing Data Flow

Data flow through the whole system can be a major design challenge

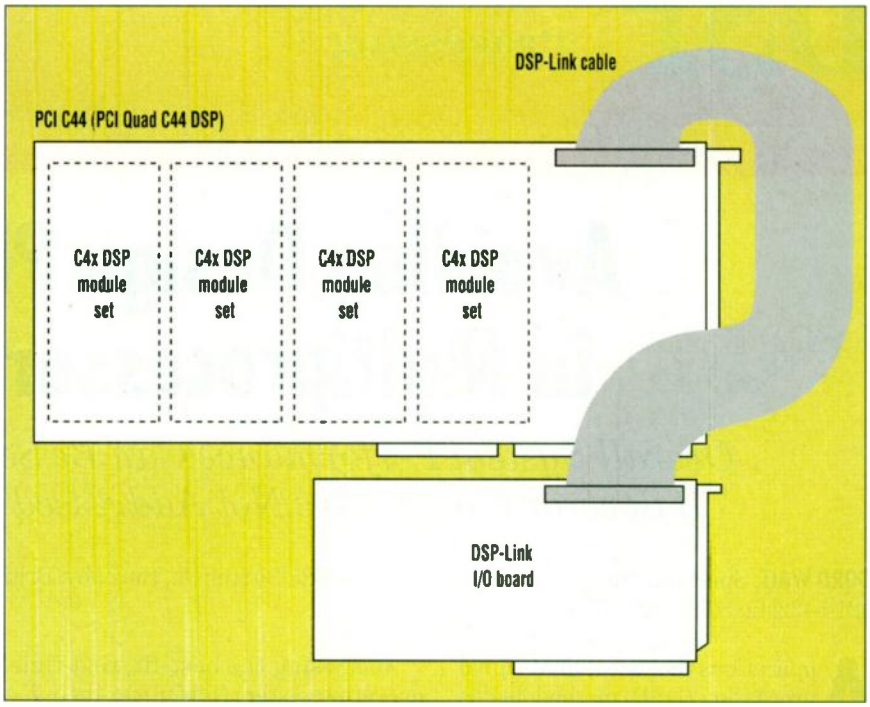


1. Two types of data-flow architecture are used in multiprocessor digital signal processing systems, pipelined (a) and star (b). Pipelining moves data in a linear flow through DSPs, while star depends on a central processor to move data among DSPs.

for multiprocessor DSP architecture. By using DSP processors with multiple communication ports and a flexible-wiring method (i.e., ribbon cables), optimal data flow architecture can be configured by the designer. This technique avoids performance bottlenecks and/or underutilized processing capacity. Typical data flow configurations for multiprocessor DSP systems include pipelined and star architectures. Pipelined architecture has the data flowing linearly through the processor chain *(Fig. 1a)*. Star architecture uses multiple processors clustered around a master processor that controls the data flow *(Fig. 1b)*. In all architectures, one processor is given the task of configuring the rest of the processors in the system and handling the communications between the DSP subsystem and the host.

In a pipelined architecture, the first DSP in the pipeline usually receives inputs from the A/D converter or sensor subsystem, conducts a portion of the DSP processing (e.g. initial data filtering), and then passes the data on to the next DSP for subsequent processing. Interprocessor communications, DSP tasks, and data flow are conducted via high-speed serial or parallel communications channels between the DSPs in the chain. Then, the final results from the DSP chain are typically handed off to the host processor for display or other disposition. Pipelined DSP architectures are particularly useful for filtering applications, which can be broken down into well-defined, sequential DSP tasks. From a host-processor standpoint, the DSP pipeline looks like a single DSP processing engine. The host does not incur any unnecessary overhead from participating in any of the inter-DSP data-flow activity, but instead, simply sets up the job with the first DSP in the chain, then receives the final results from the last DSP.

Star or other architectures can allow for greater flexibility and dynamic control over the DSP tasks based upon the changing requirements of the application. For instance, one DSP might be assigned to retrieve and process data directly from an I/O port, while others might be tasked to offload bottlenecked processing tasks or to carry out parallel DSP functions on data from a shared memory location.



2. An external I/O board connected to DSP modules gives system designers flexibility when adapting the system to specific design tasks. Standard modules, such as Spectrum's DSP Link, provide a separate I/O bus, thus offloading the system bus.

One of the key issues in the creation of cost-effective, commercial off-the-shelf DSP systems is to design in enough flexibility so that the data flow can be adapted to the specific needs of various applications. This can be accomplished most efficiently through the use of high-performance, programmable DSP processors with on-board communications features. One example is Texas Instruments' TMS320 DSP family or Analog Devices' SHARC DSP family.

Texas Instruments' TMS320C40 processors provide four or six 8-bit parallel communication ports and two separate sets of address and data buses, allowing for direct connection to private and global memories. Analog Devices' ADSP-2106x processors provide bidirectional data and address buses and six bidirectional bus request lines. For example, a DSP board design using multiple TI320C40s could be either hardwired into a specific data flow configuration, or be set up to allow for flexible configuration via ribbon cables between the processors. The built-in hardware communications port (8-bit parallel) on the TI320C40 can then be used to control interprocessor communications, set up DSP tasks, and run multiple datapaths in parallel.

Building in such flexibility to the DSP architecture not only enables the reconfiguration of DSPs at the board level, but opens the door for maximizing DSP performance with configurable multiboard systems sharing the same chassis. Individual DSPs on separate boards can be directly connected via ribbon cables, adapting the systemwide hardware building blocks to the specific demands of the application. At the same time, this use of direct-interboard DSP data flow preserves more of the system's backplane bus bandwidth for use by the host processor, and allows optimal load balancing throughout the system.

Trade-offs In Bus Selection

The two host system bus environments typically used for today's DSP systems are VME and PCI. Traditionally, high-performance multiprocessor DSP systems have been built around the VME bus because of its legacy of performance, robustness, ruggedness, and form-factor flexibility. In recent years, PCI bus systems have gained significant acceptance. This is driven largely by their options for lower-cost implementations, and by the wide

range of commercially available PCI hosts and peripherals. Because most DSP applications have historically been built around VME environments, the market for new DSP capabilities almost always requires that they be offered in VME configurations to extend existing legacy environments. In addition to providing applications continuity, VME environments also allow for much greater scalability of the overall system. A VME chassis can physically support significantly more printed-circuit boards than a typical desktop PCI-bus machine. For instance, VME-based DSP systems using as many as 20 boards are not unusual.

The VME standard is already very mature and internationally accepted. It allows for a broad range of provensystem implementation choices such as: ruggedized or militarized chassis options, multiple board sizes (e.g. 3U, 6U, 9U), and widespread installed bases in industrial, military, medical, and telecommunications industry segments.

The PCI bus is rapidly gaining acceptance as the primary alternative to VME for new DSP system configurations. Due to the phenomenal worldwide growth of PCI-based PCs, the PCI bus has opened up significant cost-reduction opportunities for DSP system implementations. The volume leverage and competition in the PC marketplace also has fed a continued explosion of low-cost, standardized graphics cards, peripherals, and I/O options, designed for plug-and-play usage in PCI systems.

At the same time, the dramatic increases in the performance of Pentium and Pentium Pro processors have challenged the dominance of the RISC-based host environments traditionally used in legacy DSP systems. The result of these combined trends is that a very powerful, Pentium-based, multiple-DSP, PCI-bus system can now be created at a fraction of the cost of traditional VME based systems. In the future, new multiple-slot, industrial-grade, PCI-based solutions like Compact PCI will begin to compete for the same market as the VME-based solution.

The bottom line, from a DSP system developer's standpoint, is that new designs and architectures must include options for both VME- and PCI-bus environments. The installed base of legacy systems will continue to fuel new deployment of VME solutions, while the cost/performance leverage of PCI-based systems will open a whole new range of applicable DSP opportunities.

Choosing The Right RTOS

The third factor in optimizing a multiprocessor DSP design is the choice of an appropriate RTOS. In a typical high-performance, multi-DSP system, the RTOS runs in an embedded mode on the individual DSPs. The RTOS thereby delivers the required data flow and processing performance, while allowing the host processor to continue to operate the overall system within the native mode (e.g. Windows 95, NT, Solaris).

Key factors in choosing an RTOS include:

- Ensuring that it is robust enough to handle the DSP processing load.
- Support for interoperability with either NT or UNIX host systems.
- A small enough kernel for embedded operation in limited DSP memory space.
- A high-level, DSP-oriented instruction set for rapid programming.
- Options for hand optimization of low-level code when required.

One of the major functions of the embedded RTOS is to provide a standardized environment for real-time inter-DSP coordination and communication. This environment includes functions such as interrupt handling and memory allocation. Additionally, it must provide all handshaking functions with the host OS.

The RTOS kernel also must be fairly small to run on the individual DSPs, which typically only have 2 Mbytes or less of on-board memory. Consequently, DSP board designers are constantly making trade-offs between the features that they would like to see supported in the RTOS, and the overall size limitations of the DSP processors' RAM and/or ROM.

In addition to running within limited space on individual DSPs, optimal system performance demands that the RTOS be able to allow for distributed operations, and support parallel programming of DSP tasks. To ensure extensibility, the RTOS structure should make it easy for the programmer to migrate tasks from a single DSP to a split mode, running on multiple DSPs. In this case, the RTOS should support the programmers by automatically restructuring the interprocessor communications, memory-to-memory copy functions, resource allocations, etc., to seamlessly partition the tasks among the processors.

Key functions that should be supported within a DSP-oriented embedded RTOS include:

- True multitasking.
- Dynamic process creation.
- Synchronized message passing.
- Semaphores.
- Real-time clock management.
- Dynamic handling of any number of nodes.
- Accessing of raw link hardware, if required.
- Modular run-time for minimum memory use.

The DSP designer's ultimate aim is to select a flexible RTOS system, combining minimum run-time overhead with maximum control over the hardware. For instance, 3L's Parallel C product is a distributed microkernel that runs on the TI320 family and provides all of the parallel programming features discussed above. By avoiding the overheads associated with a full-blown operating system, Parallel C focuses on running whole parallel programs rather than juggling competing and conflicting user tasks.

Because the designer's RTOS decision will intrinsically impact the overall system performance and hardware design, it is important that the OS be selected at the beginning of the process, when the overall architecture is defined. This decision will avoid subsequent pitfalls in which the RTOS either lacks the flexibility to extract full performance from the hardware configuration, and/or the RTOS cannot run optimally within the DSPs' available memory.

Optimal Interface Design

A DSP board design is ultimately only as good as the noise floor for the data that it is processing. To ensure accuracy, the design needs to move signals from the analog sensor environment to the DSP engine with the least amount of system-contributed noise. While the A/D conversion is typically

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BIST's Advantages Make It A Logical Choice For More Designs

As designs get bigger and more complex, it may not be a question of whether BIST is best, but whether any other methodology will work.

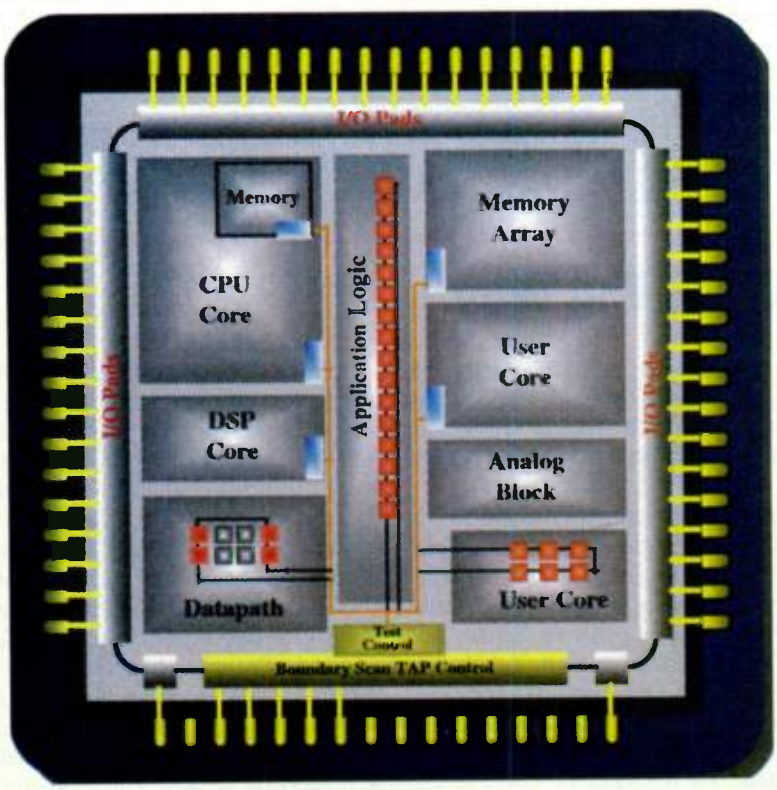
John Novellino

SPECIAL REPORT

Most designers are now convinced that they need to design testability into their circuits. If they're going to move into the six- and seven-figure gate range–as many of them are–some kind of design-for-testability (DFT) technique is mandatory to properly test the IC. But, the real challenge is the search for the silver bullet, that one "best" technique that will deliver 100% fault coverage with little or no overhead, or performance penalty. Well, that's just not going to happen. But built-in self-test (BIST) is a technique that has come pretty close in many designs already, and promises to be a major force in the future.

BIST offers a number of advantages: repeatability, reusability, reduced development time, reduced test time, lower test system costs, etc. As the size and complexity of ICs increases, however, it won't be a matter of whether BIST is better than traditional external testing, but whether external testing is even possible. Automatic test-pattern generation (ATPG) programs have helped considerably, but even ATPG has its limits. How long it takes to generate massive vector files and run the tests, as well as the price of the tester are often the deal breakers.

The desire to reuse logic blocks and the tests developed for them, is an important consideration in the choice to go with BIST. "Many of the advantages of BIST have been ignored in the past (with the one exception being the military-aerospace industry) because the overhead associated with the change in design style up front and the silicon area have outweighed the benefits," according to Ian Burgess, BIST product manager at Mentor Graphics' Design-For-Test Group, Wilsonville, Ore. "But now we are seeing a driving force for BIST, caused by the explosion in the complexity of ICs, that is forcing the design community to accept design reuse and, with it, test reuse."



Art Courtesy: Mentor Graphics Corp.

When designers reuse logic blocks, or buy blocks from third-party suppliers of cores, they'd just as soon use an existing test. This is especially important in the case purchased cores, which usually cannot be modified for DFT purposes, says Burgess. And BIST is important to core suppliers because it ensures a testable circuit without compromising the supplier's intellectual property.

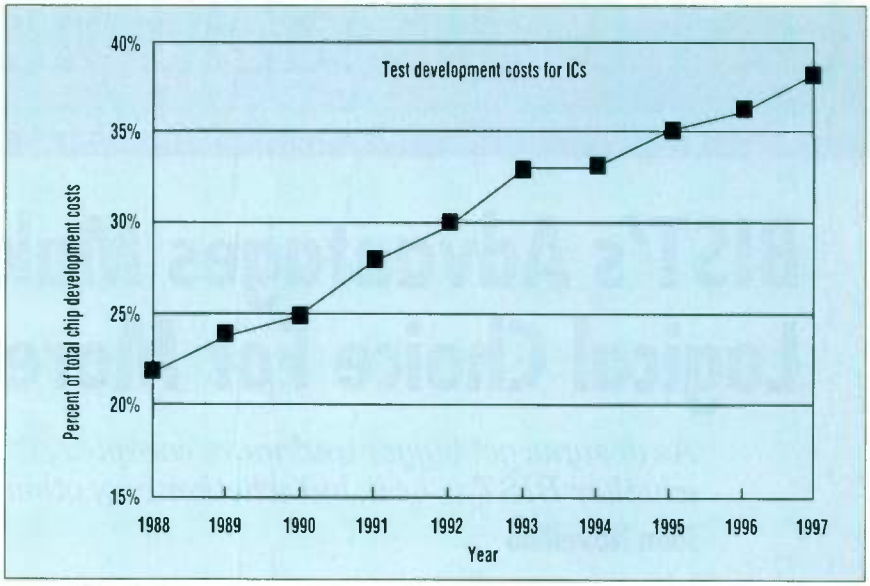
In recent years, the front end of the design cycle has been greatly shortened by the use of high-level languages. If fact, they have provided the huge increase in IC complexity. Testing hasn't kept up, however.

"Unfortunately, test has remained primarily a back-end (that is, process-specific, post-synthesis)

function that relies on cumbersome back-end analysis tools and expensive automatic test equipment to provide the testing solution," says Robert P. Smith, vice president of marketing and business development at LogicVision Inc., San Jose, Calif. "Because of this and because of the increasing complexity of new designs, test development costs have become the single most expensive element of the total ASIC development cost."

Smith cites an estimate from Integrated Circuit Engineering Corp., Scottsdale, Ariz., saying that up to 40% of the IC development cycle is consumed with test development. He adds that an estimate from Dataquest states that test-development costs are approaching 40% of total ASIC development costs *(see the figure)*.

Because BIST is extremely scalable, it is well-suited as a DFT technique for ever larger designs. For a 100-kgate design, the overhead needed to support logic BIST, memory BIST, and the IEEE-1149.1 controller and boundary scan might approach 3500 gates, says Smith. That's a 3.5% overhead. At one million gates, the BIST overhead would rise only slightly, to about 3700 gates, he says. Overhead is now only 0.37%. "The point is that BIST structures remain relatively static in size even though the circuits they are testing may be growing dramatically," says Smith.



Due to relatively faster advances in design automation, as compared to test development automation, test costs are becoming a bigger portion of total IC development costs.

In fact, more than 60% of designs are now pad-limited rather than gate-limited, says Smith. So in the majority of cases, BIST-area overhead is zero, because the real estate is there for the taking.

There are two basic types of BIST: BIST for memory or regular structures, and BIST for random logic, notes Shianling Wu, a technical manager at Lucent Technologies in Princeton, NJ. Deterministic test-pattern generation works best for memory BIST, and pseudorandom techniques are usually employed for random logic, although pseudo-exhaustive patterns can be used. Regular-structure BIST outperforms competitive techniques in fault coverage, development time, and area overhead, says Wu.

"Designers, though, need to worry about the types of faults the regular-structure BIST algorithm catches," she

System BIST On The Way

The promise of BIST extends not just to IC testing, but to board- and system-level testing, as well. That promise is a step closer with the recent announcement of a BIST technology prototype for testing board-level interconnects.

The board-level technology is the first of its kind, and is key to the development of a complete system-level BIST solution that leverages BIST at the chip, board, and system levels, according to LogicVision Inc., San Jose, Calif. The company worked closely with Lockheed Martin Advanced Technology Lab (LM-ATL), Camden, N.J., to develop the prototype as part of a Defense Advanced Research Projects Agency project called Rapid Prototyping of Application-Specific Signal Processors (RASSP). LM-ATL is the prime contractor for RASSP.

"RASSP's charter is to support the development and commercialization of key, emerging technologies," said Jim Saultz, RASSP program director at Lockheed Martin. "We see LogicVision's BIST as such a technology, and one that could very well reshape the way electronics are designed and tested."

The technology prototype generates and inserts BIST technology automatically, so design engineers can implement BIST simply and easily, without having to become BIST experts. The prototype includes:

- generation of an RTL-level controller to verify the interconnects via an algorithmic test;
- support for boundary-scannable device insertion;
- testing of sequential and combinational cluster logic; and
- back-end support tools such as design-rule checking, fault simulation, fault reporting, and test signature generation.

Steve Pateras, director of system BIST products at LogicVision, said the company also is working on an IEEE-1149.5 system-level controller. All the technology needed for system-level BIST should be ready within several months, he said. The company is looking for partners willing to participate in the validation process before bringing actual products to market.

RASSP funding helped LogicVision develop mem-BIST-XT, a BIST solution for board-level memory arrays. That product was introduced last October.

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says. "This requires working with device vendors to make sure the algorithm indeed is catching the types of faults that the manufacturer agrees are important."

According to Wu, pseudo-exhaustive patterns can provide high fault coverage for random-logic BIST, but increase area overhead. With pseudo-random patterns, designers can choose full-scan, partial-scan, or even circular-scan implementations. Full scan offers little flexibility to avoid selecting flip-flops in the high-speed regions of the IC, she says. On the other hand, partial scan allows designers to select a subset of the strategic flop-flops, and thus play around with the trade-offs.

"Random-logic BIST tools that offer both full- and partial-scan-based solutions give designers choices," says Wu. "Fault coverage can always be brought up by adding test points, especially for random-pattern-resistant faults." She notes that some scan-based random-logic BIST methods provide a scan mode that is useful for diagnostic and debugging purposes. The circuit can be placed in either BIST or scan mode.

A number of factors, often design specific, influence the decision of how to implement BIST. Issues include whether the BIST logic will be shared between blocks on an IC, the selection of algorithms for different memory types (multiport, DRAM, SRAM, etc.), and how the different self-tests will be scheduled on the chip.

"There also is the important issue of diagnostics," says Mentor's Burgess. "Adding diagnostics to BIST allows you to carry out deeper analysis on why a design fails, but it also adds overhead in terms of silicon and time. In some cases where extra intrusion into a core was required to achieve high fault coverage with BIST, designers have reverted to ATPG to 'top up' the coverage."

One of BIST's important advantages is that it makes true at-speed testing much easier because the test signals do not have to be transferred from an external tester. For very fast chips, however, the designer must make sure the BIST structures are tied into the on-chip clock management system, says LogicVision's Smith. "At 100 MHz and above, clock-skew management becomes critical to guaranteeing chip performance and reliability," he says. "Thus, the BIST structures must also use the same scheme so that accurate at-speed tests can be made."

BIST may not be the best solution for an entire chip, so the first thing a designer should do is decide which logic will use BIST, and what infrastructure will link the different blocks together, says Wuudiann Ke, DFT principal consulting engineer, and Chit Mallipeddi, vice president, Cadence Design Systems. They highly recommend integrating BIST within the IEEE-1149.1 (JTAG) infrastructure.

BIST's main advantage is that it can be reused at different levels—chip, board, or system—and at different stages in a product's life cycle such as manufacturing, installation, and field, say Ke and Mallipeddi *(see "System BIST On The Way," p.102)*. They agree that BIST is especially suitable for regular-structure logic, for which it provides good fault coverage with lit-

tle overhead, but say it's not as good for random logic, especially logic with multiple clock domains.

As a result, individual test strategies will vary, with multiple methods probably needed. "[Different techniques] are complementary in some ways," they say. "BIST can be reused; scan provides good diagnosability, while IDDQ (quiescent current) can detect some reliability-related faults that cannot be detected by BIST and scan. Your test strategy should be based on your unique test requirement and test economics."

In fact, the use of multiple test strategies is a key requirement for deep-submicron designs, notes Tom Jackson. Jackson works at Viewlogic Systems Inc.'s Marlboro, Mass. headquarters, but is a member of the Sunrise Test team, Fremont, Calif. "For example, you might have several types of embedded memories and an embedded DSP, along with a high content of data path," says Jackson. "Each of these entities requires a different testing strategy. The memories will use BIST; the data path will use partial scan, and the embedded processor will use functional patterns."

Jackson says there are basic scan-based BIST strategies and some partial-scan adaptations. But most successful BIST implementations at this time use full-scan techniques.

BIST will cause some changes in the automatic test equipment (ATE) industry, but that will take some time. For designs that use only BIST, ATE costs should be reduced drastically. But as Jackson notes, most designs will use a mixture of BIST and other DFT techniques, so ATE will still be needed.

BIST itself requires only a low-speed, small-memory device as an external controller. A PC or older ATE will handle the job. The external unit sends a simple protocol to the chip (the IEEE-1149.1 test access port is the recommended route) that starts the BIST operation. After the BIST has run, the controller scans the results out of the chip (again via the test access port), and displays them as pass or fail.

How Valuable	Circle
Highly	548
Moderately	549
Slightly	550

Practical Design Techniques For Memory BIST

Although It's An Excellent Way To Ensure The Testability Of Memory, Applying Memory BIST To ICs And Systems Takes Some Planning.

IAN BURGESS, Mentor Graphics Corp., 8005 S.W. Boeckman Rd., Wilsonville, OR 97070-7777; (503) 685-1329;
GREG YOUNG AND JAY JAHANGIRI, Texas Instruments Inc, Systems Group; Test Technology Center for Excellence, 6500 Chase Oaks Blvd., Plano, TX 75023; (972) 575-2585.

As ICs absorb more system functionality, the percentage of silicon real estate devoted to memory is getting bigger and more difficult to test. Fortunately, built-in self-test (BIST) offers a viable way to test both embedded and system-level memories, without significant silicon overhead or sacrifice in system performance. Indeed, through its at-speed capability, BIST significantly improves the quality of testing without appreciably impacting test time.

BIST is well-suited for testing memory because it supplements, rather than replaces, other test techniques such as scan. Memory suffers from different types of faults than random logic does. The most common faults, which occur in the memory cell array, are stuck-at, transition, and coupling faults. Another common fault occurs in the address decoder. These distinctive fault classes require a set of specialized test algorithms.

The algorithms, commonly known as marching algorithms, are targeted at BIST. They can typically be implemented with a reasonable gate count—about 1500 gates for a 32-bit-wide memory. Furthermore, localizing the test onto the IC via BIST allows the test to be performed at speed using the system clocks. This technique improves test quality by detecting timing-related faults.

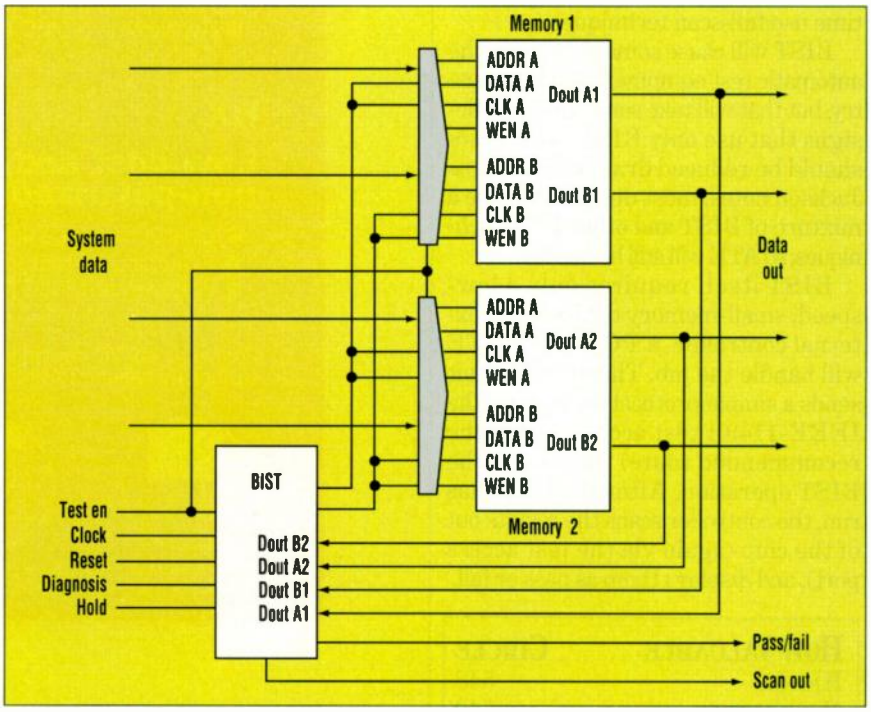
Memory BIST employs a test stimulus generator, a response comparator, and a controller that interfaces to the memories-under-test through simple multiplexing of the memory pins. In test mode, the patterns generated by the BIST are written to and read from the memories, and checked against the expected response in the comparator. In its simplest form, all that BIST requires external to the IC is a test-enable input pin, clock, and fail-flag output pin.

Texas Instruments' Systems Group has been using memory BIST for approximately 10 years. The company's memory-BIST strategy focuses on providing the most efficient test possible, with the least impact to performance, area, and test execution time. Typically, these BIST designs execute autonomously at the system clock frequencies, apply data through existing parallel data buses, and take advantage of parallel execution across several memories simultaneously.

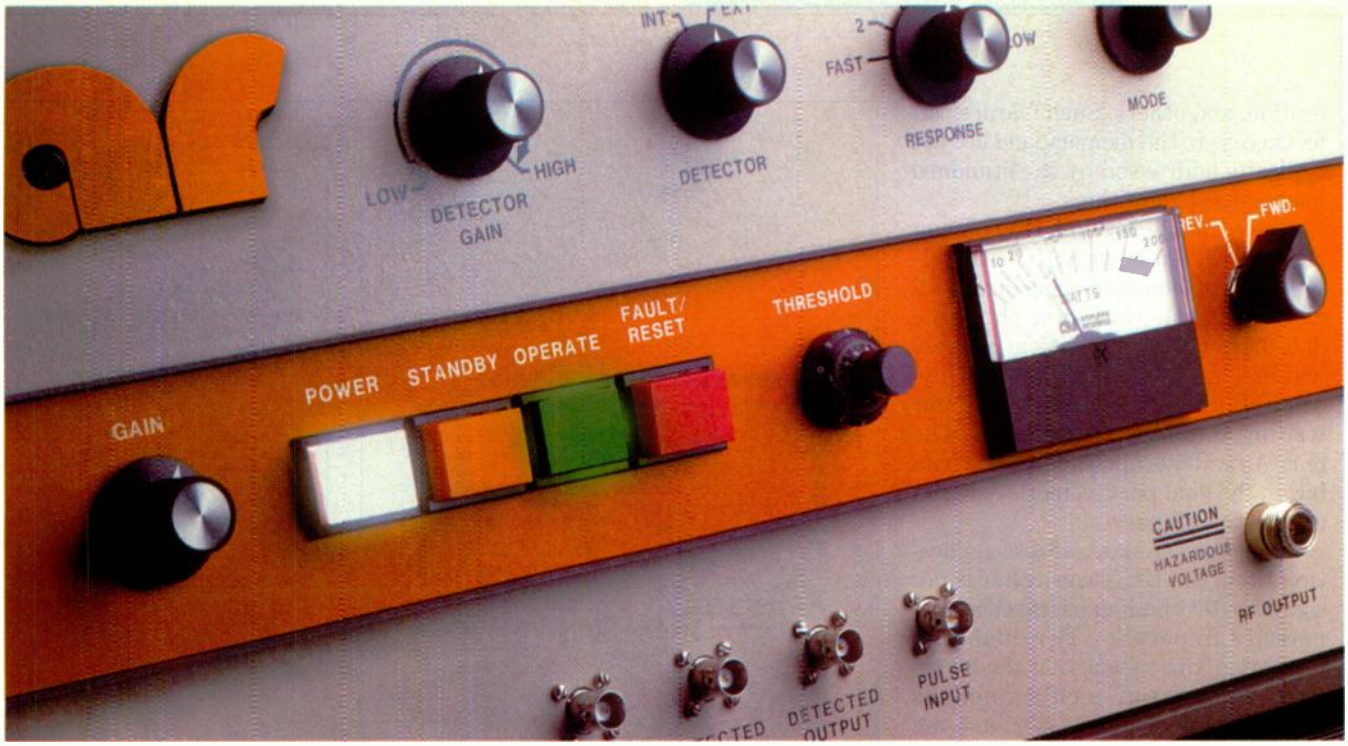
A popular scenario involves the use of a marching algorithm of 10N length, applying an appropriate number of different data backgrounds (for example, 3333, 0F0F, 00FF) to ensure detection of all coupling faults.

Designing For BIST

While memory BIST has many advantages, experience shows that it is not a trivial design exercise. Selection of the test algorithm is often relatively straightforward, based on trade-offs surrounding the type of memory, targeted failure modes, desired fault detection/isolation, test execution time, and physical constraints. However, special attributes of the memory, not initially obvious, can complicate testing. These include multiple read and write ports, special addressing modes, synchronous versus asynchronous op-



1. Designing the memory BIST controller's state machine and multiplexers into separate blocks minimizes the routing impact on the address and data lines.



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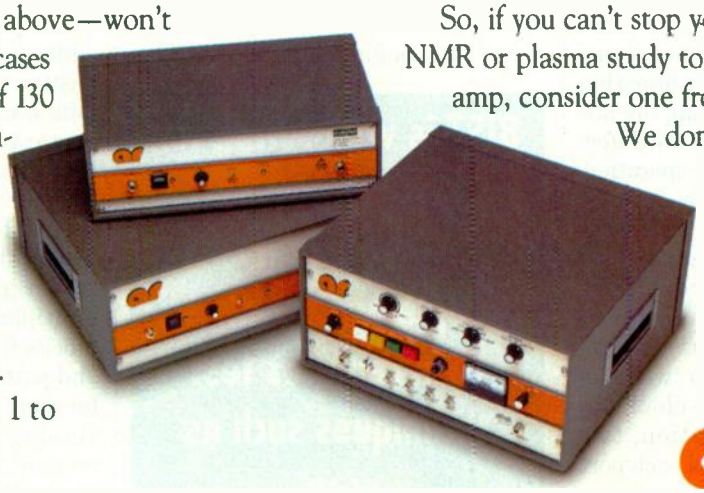

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eration, and others. Such features affect access to the memory, and are not typically addressed by the standard memory test algorithms.

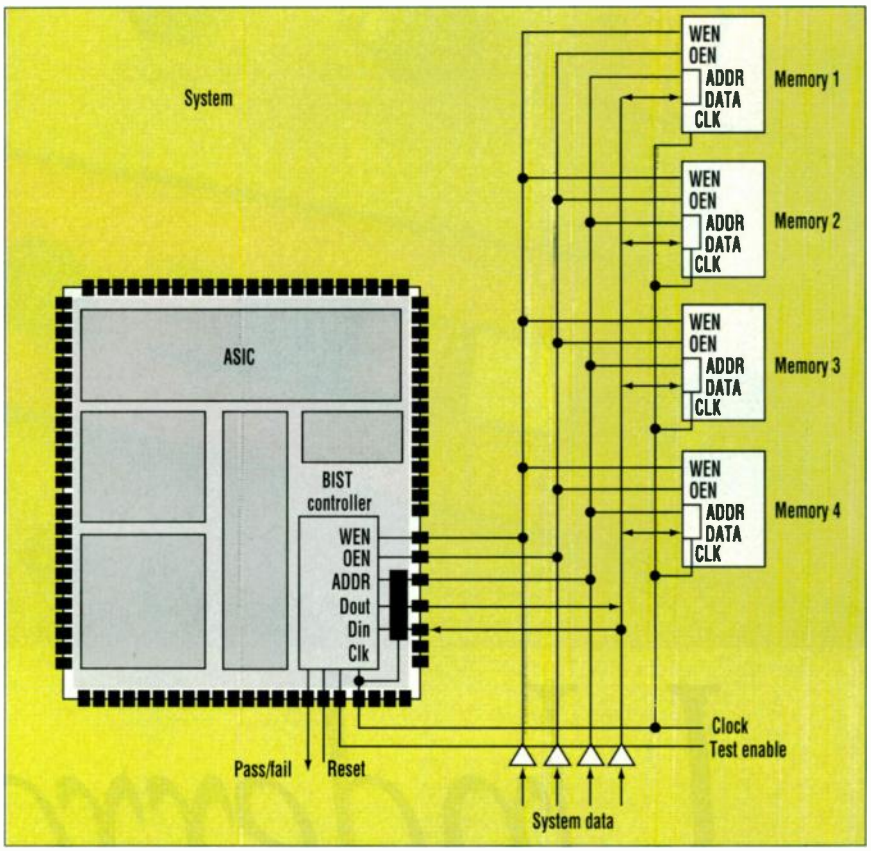
One example is two FIFO memories embedded in an ASIC. The FIFOs are implemented using dual-port, clocked RAMs that have the same data-bus width, but different address widths—a 144-by-34 bit and a 560-by-34 bit. Both memories use port A for writing and port B for reading. The port A read bus and the port B write bus in the dual-port memories are unused in this scenario.

To ensure the shortest test-application time, the BIST controller is designed to test both memories simultaneously, in parallel. For dual-port memories, this means that the corresponding port of each memory is tested simultaneously. Because the memories are of different sizes, the controller disables the smaller memory when its address space is exceeded. This strategy results in a maximum test time equal to the test time for the larger memory.

This memory configuration presents a number of other challenges in the BIST design. Dual-port RAMs typically have a design constraint on simultaneous access to a memory location from both ports. That is, the operation (read or write) will not be guaranteed when the same address is being applied to both ports A and B. Because the memories are used as FIFOs during normal system operation, the FIFO controller ensures that this error is never encountered.

However, the traditional memory march test requires that back-to-back read and write operations occur at the same address location. To overcome this limitation, the march algorithm must be modified such that the addresses applied to each port are different for each read and write operation. The exact values used for the inactive port are arbitrary, as long as the addresses always remain different.

Another challenge involves the handling of asynchronous clocks. A FIFO memory is typically used to provide data transfer between two independent (asynchronous) clock domains. In a FIFO operation, two asynchronous clocks control each port of the memory, one for the write operation and the other for the read. If two asynchronous clocks were used to apply march patterns from a BIST controller, the controller would become too complex and unmanageable.



2. BIST also can be used to test system memory arrays and SIMMs at speed. The BIST controller can be placed inside one of the system's ASICs or on a reconfigured FPGA.

Therefore, BIST should be implemented using a single clock, with the nonprimary clock multiplexed with the primary clock during test mode. Although multiplexing or gating clocks is usually not an attractive methodology, it is less of a burden in this case. The clock is only switched once at the beginning of the test, remains at a constant frequency for the duration of the test, and then is switched back to the functional clock.

BIST is well suited for testing memory because it supplements, rather than replaces test techniques such as scan.

Finally, the BIST controller must account for the physical placement and routing on the chip. This design is especially important when multiple memories share the same BIST controller. The controller multiplexes the system signals during testing to control and observe the memories. It requires placing a multiplexer on every address, data, and control signal. To ensure maximum performance and minimum routing overhead, it is important to place these multiplexers adjacent to the memories.

Since place-and-route tools use the logical hierarchy of the design for physical placement, the BIST controller must be designed so that the multiplexers are placed in separate blocks from the finite state machine and pattern generators. In practice, for multiple memories, this means designing the multiplexers for each memory into their own hierarchical blocks *(Fig. 1)*.

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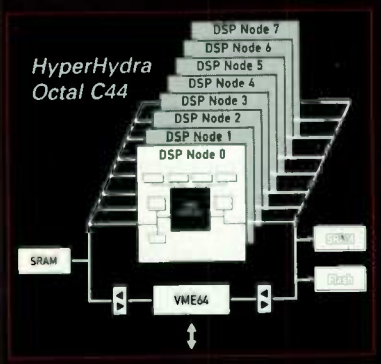

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when applying memory BIST is diagnostics. Along with detecting a memory failure, it is important to extract diagnostic information from the test—usually a bit map of the failing memories to determine the common failure modes. This procedure can take up a lot of valuable time during production test. Consequently, a robust-memory BIST controller should be designed to support two modes of operation, a simple pass/fail mode for typical production and field test, and a diagnostic mode for failure analysis.

During the diagnostic operation, the BIST controller outputs the failed address, expected and actual data, and the controller state through a dedicated scan pin. Because the information is scanned out, the BIST controller doesn't force any constraints on the amount of diagnostic data that can be extracted or stored.

External Memories

BIST also is useful for testing off-chip memory when access is limited or test execution time is critical, for example, when a memory is not directly accessible by a system processor, or when the software overhead (wait states, pipelining, etc.) incurred by using the march algorithm causes too long an execution time. To apply BIST, a controller is designed into one of the ASICs or FPGAs in the system that interfaces to the memories. Only this time, the controller tests the memories through the primary pins of the ASIC or FPGA.

An example involves testing four off-the-shelf Motorola 32k-by-8 SRAMs arranged in a 32k-by-32 memory array. From the BIST-controller perspective, the memory array is treated as a single memory device. Diagnostic information, such as the failed data bits, can be used to isolate to the physical memory device. As with embedded memories, a 10N march algorithm with appropriate data backgrounds is applied.

While the basic design and application of the BIST is straightforward, external memories also present some unique challenges. One obvious difference between external off-the-shelf memory and embedded memory is bidirectional data buses. Most embedded memories have separate data buses for reading and writing. But most off-the-shelf memories use bidirectional buses to minimize pin count.

Fortunately, the bidirectional bus itself is not a real issue when implementing BIST for off-chip memories. The bidirectional buffer at the device's I/O splits the data into unique input and output buses. The BIST looks identical to that used for embedded memories, except that an output enable signal needs to be added to control the direction of the bidirectional buffer during the test.

Timing is another issue when using BIST to test external memories. The timing associated with interfacing to external memories depends on the delay through the ASIC/FPGA pins, the board-level signals, and the memory (access time). Designers can resolve these issues by adding registers to the I/O of the ASIC/FPGA and the memory to pipeline the signals between devices *(Fig. 2)*.

To apply BIST in this situation, the controller must account for the multicycle paths between it and the target memories. The simplest way to accomplish this is to stretch the read and write cycle times of the BIST controller to match the multicycle delay. While this is not a truly pipelined BIST architecture, it may be adequate if the increase in application time does not violate the overall test execution time constraints. This technique allows the same BIST controller architecture to be used with only minor changes in signal timing.

Ian Burgess is the BIST product manager for Mentor Graphics' Design-For-Test Group. He holds a bachelor of engineering degree from the University of Liverpool, United Kingdom.

Greg Young is a member of the group technical staff at Texas Instruments Systems Group. He received his BSEE degree from Southern Methodist University, Dallas, Tex.

Jay Jahangiri joined Texas Instruments Systems Group in December 1995, as an electrical engineer. He received his BSEE degree from the University of Texas at Arlington.

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The eight modules include low-frequency and RF multiplexing, matrix and general-purpose switching, and digital input/output, analog output, and event counting functions. Users can configure a system for up to 120 single-ended channels or 96 matrix cross points. To avoid unscheduled downtime, a relay maintenance system automatically counts every individual switch closure and stores the total in nonvolatile memory on the module.

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Options include the ability to increase memories to 1 Mbyte per channel. Also, for mixed-signal testing, an 8-bit TTL and ECL digital output is available for use as a pattern generator. A special digital editing mode helps in creating digital patterns.

An internal disk drive and floppy drive simplify waveform storage for future use. The units are IEEE-488.2-compatible and have printer output support.

The LW420A costs $18,950; the LW410A goes for $13,945. The upgrades to 1-Mbyte memories cost $4995 for the LW420A and $3495 for the LW410A. The optional 8-bit digital output costs $1995. Delivery is in four to six weeks.

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Emulator Software Performs Code Coverage Analysis

Version 1.8 of the WinKSE software package for the KSE5 in-circuit emulator includes code coverage analysis that supplies documented proof of full program execution. Also, any Windows application now can be integrated with the debugger software and operated using a uniform interface.

The software employs the KSE5's simulation memory as a TAG memory for the complete documentation of all addresses accessed by the application program. The user also can partition the simulation memory. This enables program error detection to be carried out in the simulation memory while the code coverage analysis is done in the TAG memory. This saves the time it would take to transfer the program under test to the target memory for error detection. Code coverage results can be stored on the computer hard disk or printed out.

Any Windows application can be integrated in the debugger and cued as a push button under WinKSE, so popular editors and compilers from any manufacturer can be used without leaving the debugger environment. Frequently used commands can be stored as icons.

The software is standard on new KSE5 emulators. For current KSE5 users, an upgrade package costs $635.

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MEETINGS

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Seventh IEEE International Fuzzy Systems Conference, May 3-9. Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

IEEE/IAS Industrial & Commercial Power Systems Technical Conference (I&CPS), May 4-7. Edmonton, Alberta, Canada. Contact Marty Bince, Modicon Canada Ltd., 5803 86th St., Edmonton, Alberta T6E 2X4, Canada; (403) 468-6673; fax (403) 468-2925.

IEEE International Conference on Acoustics, Speech & Signal Processing (ICASSP '98), May 12-15. Seattle Convention Center, Seattle, WA. Contact Les E. Atlas, Dept. EE(FT 10), University of Washington, Seattle, WA 98195; (206) 685-1315; fax (206) 543-3842; e-mail: atlas@ee.washington.edu.

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IEEE/MTT-S International Microwave Symposium (MTT 98), June 7-12. Baltimore Convention Center, Baltimore, MD. Contact Steven Stitzer, Westinghouse Electric Corp., P.O. Box 1521, MS 3T15, Baltimore, MD 21203; (410) 765-7348; fax (410) 993-7747.

USENIX 1998 Technical Conference, June 13-17. Marriott Hotel, New Orleans, LA. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

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IEEE International Geoscience & Remote Sensing Symposium (IGARSS '98), July 6-10. Sheraton Seattle, WA. Contact Tammy I. Stein, IGARSS Business Office, 2610 Lakeway Dr., Seabrook, TX 77586-1587, (281) 291-9222; fax (281) 291-9224; e-mail: tstein@phoenix.net.

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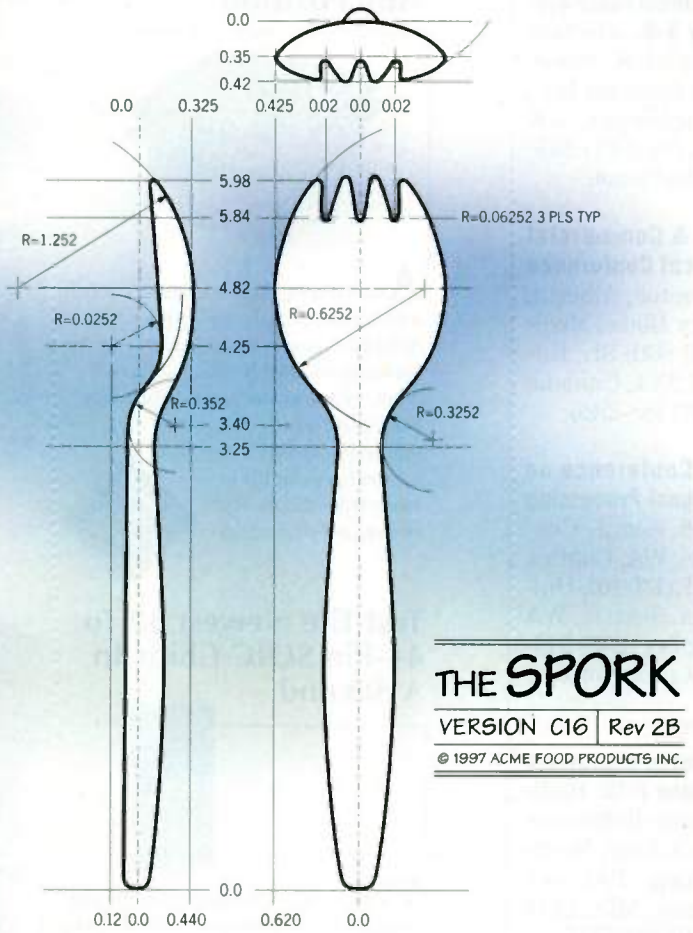

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Jules H. Gilder and Dave Bursky

SPECIAL REPORT

From being a niche market reserved for a few only a couple of years ago, 3D graphics have mushroomed and are now widely accepted in the mainstream PC market. In fact, it is estimated that the 3D graphics chip market will grow to $1.5 billion by the year 2000, with 3D graphics controllers increasing from 7 million in 1996 to 70 million in 2000.

Why the big interest in 3D? Because it gives users the ability to simulate what appear to be real-world situations on their computer screens. For example, try running games like Doom, Descent, or Flight Simulator on your PC, and you'll begin understanding why 3D graphics has suddenly become such a hot area for hardware designers. Unlike conventional 2D imaging that presents images on a flat surface that can be moved over but not through, in the 3D world, you can actually move through a scene and experience comparatively realistic, or fantastically unrealistic, virtual worlds.

Courtesy: Cirrus Logic.

Until recently, the market was dominated by professional applications such as CAD (computer-aided design) and animation. Today, a second major application area has developed—the consumer market, where 3D is being used in games and World Wide Web pages. The demands of these two environments are quite different. The CAD environment requires a great deal of precision in rendering (the actual drawing of the 3D image on the 2D screen), which is typically done at high resolutions and refresh rates on large workstation monitors.

On the other hand, the consumer environment focuses on fast frame rates in games and achieving good-looking visual effects, some of which would not be applicable to the professional environment. According to Niles Burbank, product manager for desktop graphic components at ATI Technologies, a manufacturer of 3D graphics chips and cards, the differentiation between these two environments is becoming less clear due to the emergence of a number of 3D business applications. These include VMRL browsers for corporate intranets and 3D presentation software such as a 3D version of PowerPoint.

The problem with 3D imaging, however, is that it takes a lot of computing power and memory. Part of that power is used to handle the lighting, shading, and texture-mapping that makes a drawn object look so real, you'd think its a photograph. Additional computing power is required to handle the animation of images where a scene is constantly redrawn with only minor changes in each

one. When each of these images is played back in sequence, there is the illusion of movement.

To achieve a realistic sense of motion, the images, also called frames, must be played back at a fast-enough rate, which most people agree is about 30 frames per second (fps). If the image is a simple one, like a bouncing ball, it's easy to achieve the 30 fps rate. But as the scene becomes more complex and you add the shading, lighting, and sound needed to make it more realistic, you start to run out of computing power. That's why 3D graphics chips have suddenly become such a hot item.

The challenges of achieving the high-speed computations needed for realistic 3D graphics has led to the development of many different approaches to implement the compute elements required. At the low end, the host CPU (an Intel Pentium or similar CPU in the PC) performs most of the computations, and thus the system provides minimal 3D capabilities. The forthcoming MMX-enhanced CPUs promise to improve the graphics capabilities, but as 3D applications are developed, the increasing demands being placed on the CPUs are taxing their computational abilities.

This is why everyone in the industry, including Intel, is looking to offload many of the time- and horsepower-consuming tasks that 3D computation requires onto special graphics processing and accelerator chips. 3D processing requirements are so high, in fact, that even the next generation Klamath-class processors do not have enough horsepower to do setup, in addition to managing the game play and implementing the game's artificial intelligence, geometry transforms, and lighting.

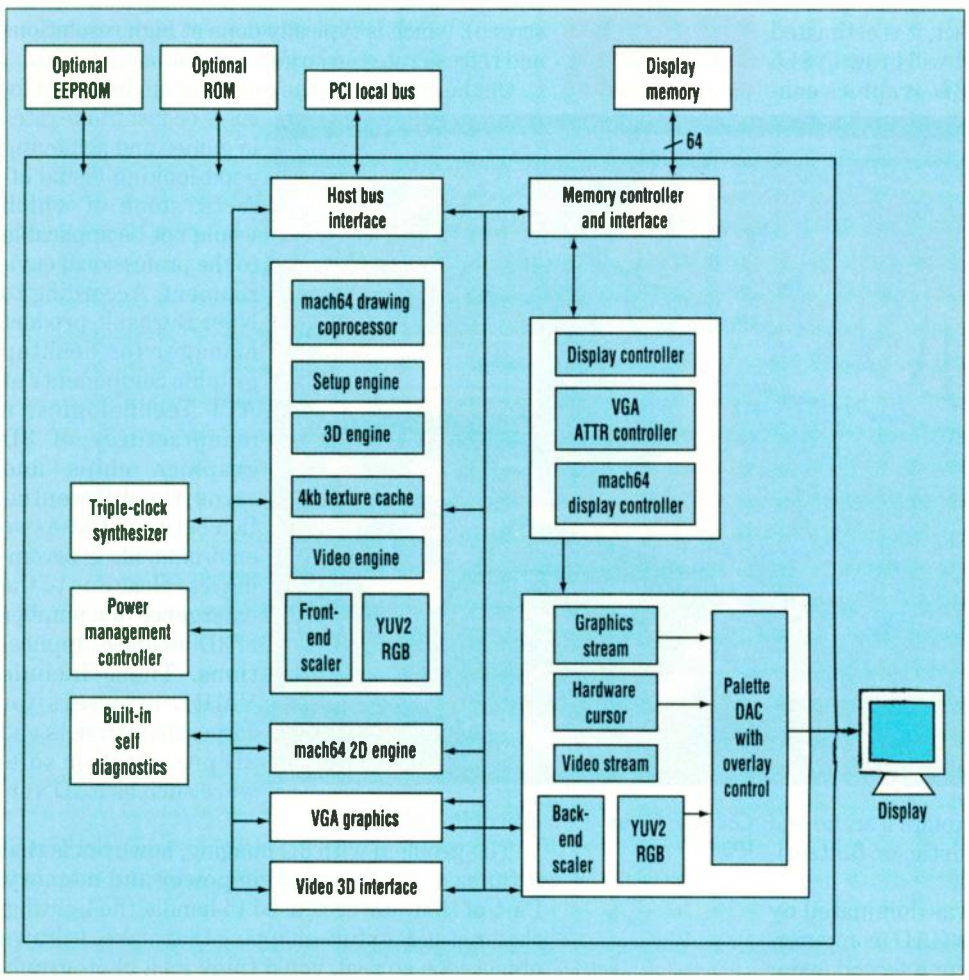
New Chips Abound

There has been a great deal of activity in the last year in the 3D graphics chip market. By some industry accounts, as many as 25 chip vendors have announced the availability of 3D chips and/or the existence of 3D chip development programs. Some of the advances incorporated into these new chips include the integration of floating point set-up engines, compatibility with SGRAM or RAMBUS memory interfaces, support of Digital Video Disk (DVD), and support for Intel's new Accelerated Graphics Port (AGP) *(see "All About AGP," p. 125).*

As noted, there are over 25 companies vying with each other for a share of the 3D chip market. Some of the early players include companies such as ATI, 3Dlabs, and S3, which introduced products starting in about 1995. Since those first product introductions of just two or three years ago, the field has increased with many small and large companies joining in

Intel itself has an AGP graphics project—called the i740GT—that should come to fruition in the second half of this year, and Microsoft also has started a multicompany project called Talisman—an architecture that can be used to implement high-end 3D graphics. The Intel chip is actually a three-company effort—Intel is partnering with Lockheed Martin (Real 3D) for the 3D algorithms, and also with Chips and Technology, who is supplying the 2D graphics portion of the chip to handle the legacy applications.

Some of the other players in the AGP market include Chromatic Research, Cirrus Logic, Dynamic Pictures, Intergraph, Mitsubishi, NeoMagic, Real3D, Rendition, Trident Microsystems, TriTech Microelectronics, S-MOS Systems, and Yamaha Systems Technology. Although many of the chips contain similar functional blocks, there are major differences between them. Some will include the floating-point setup engine, others will leave that task for the host system CPU. Others include dedicated hardware for multimedia, while others will rely



1. An advanced graphics controller, the 3D Rage Pro from ATI Technologies, takes full advantage of Intel's Accelerated Graphics Port (AGP) with 133-MHz operation. The chip's high performance comes from a setup engine that can process up to 1.2 million triangles/s, a rate much greater than the industry average.

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on off-chip MPEG or media accelerators for scaling and motion video. With the increased use of TV-style monitors, some chips also are starting to offer NTSC/PAL video outputs that can directly drive a VCR or television set.

ATI Technologies, one of the early players in the graphics controller market, introduced their first 3D chip, 3D Rage, at the 1995 Comdex show. The chip was used on add-in cards and motherboards (it was in the high end of IBM's Aptiva line). Since then, ATI has introduced several other products: The 3D Rage II, which doubled the performance of the original 3D Rage; the 3D Rage II Plus DVD, which is similar to the 3D Rage II, except that it adds a block of logic that performs motion compensation in hardware, thus improving the frame rate playback of MPEG 2 by 20 to 30%; and the latest chip, the 3D Rage Pro, which was unveiled earlier this year. This latest release by ATI delivers a significant improvement in performance and is one of the first chips to support the 2X (133 MHz) operating mode of the AGP interface. When operating at top speed, the chip's framebuffer memory bus has a peak bandwidth of more than 800 Mbytes/s, thanks to the use of 100-MHz synchronous graphics DRAMs The on-chip geometry setup engine allows the circuit to process 1.2 million triangles/s. *(For more details on the Rage Pro, see the product story on p. 127.)*

The chip unleashes the full potential of the AGP interface and, at the same time, takes advantage of 100-MHz synchronous graphics RAMs, an on-chip floating-point setup engine, an internal 4-kbyte texture cache, an integrated 230-MHz output DAC, and enhanced MPEG-2 motion compensation to provide the high throughput *(Fig. 1)* When evaluated with the WinBench 97 benchmark, the Rage Pro delivers a rating of over 100 million when driving a 1024-by-768 pixel display with 16 bits/pixel.

By offloading the setup function from the CPU, the 3D Rage Pro significantly improves the performance of the entire 3D pipeline and allows the CPU to focus on 3D geometry and lighting transformations. Most other setup engines only accept fixed-point parameters, which requires the CPU to perform the floating-point to fixed-point conversion. Such a conversion requires about 100 CPU clock cycles, thereby consuming consumes most of the CPU's resources.

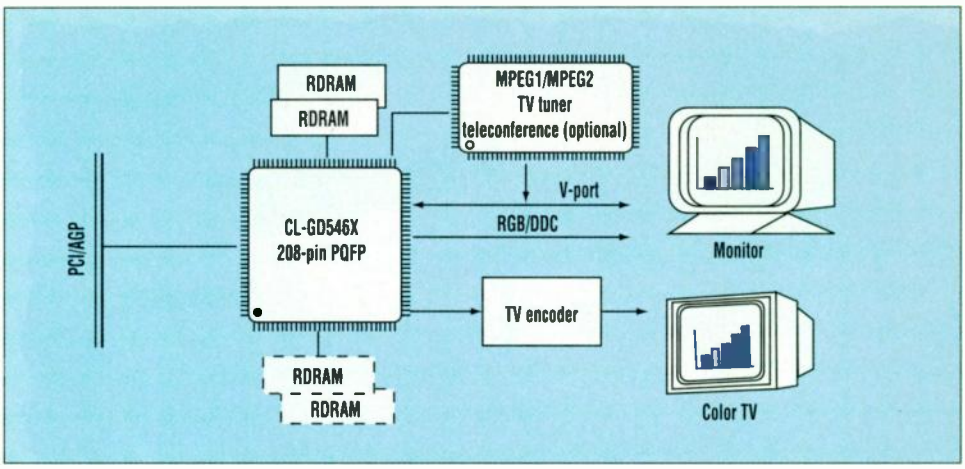
The motion compensation enhancements go beyond the compensation circuits first released in the company's 3D Rage II+DVD chip. By offloading the computations from an MMX-capable CPU, the 3D Rage Pro improves the software DVD/MPEG-2 frame rate by 20% to 30%. That will allow the company to offer a low-cost hardware DVD solution by using the IBM MPEG-2 decoder that connects to the Rage Pro via the AMC port, and thus give the system the ability to deliver no-compromise full frame-rate DVD playback.

Current 32-bit systems are limited to a peak bandwidth of 133 Mbytes/s, and since that bandwidth must typically be shared with other PCI devices connected in a system, the actual available bandwidth is much lower. However, future PCI devices could offer double that if the bus frequency is doubled, either by actually doubling the clock rate, or by using both the rising and falling edges of the 33-MHz clock. In the meantime, if there is a slower device connected to the PCI bus (and most add-in devices are of the slower, 33 MHz variety), the bus is thrown into its slower operating mode and the bandwidth of your graphics card drops accordingly.

Cirrus Logic also is sampling an AGP-based 3D graphics controller chip. Called the CL-GD5465, it's a 64-bit accelerator based on the previously released Laguna 3D PCI accelerator. Unlike the 3D Rage Pro, the chip does not contain a built-in setup engine.

Bob Brummer, director of strategic marketing for Cirrus Logic, notes that a setup engine is not necessary for the commercial market, which is what the CL-GD5465 chip is targeted for. He explains that 3D is still in its infancy, and there aren't that many 3D applications existent. For now, rendering acceleration (which is what the Cirrus Logic chip does) is probably going to be sufficient enough to get the job done. Any bottlenecks that appear are likely to come from other things in the system like the Ethernet or modem connect, and not from setup. Brummer does admit, however, that as more powerful applications appear, a setup engine will be necessary.

For that reason, Cirrus Logic is working on a more advanced 3D chip that will include a setup engine. It will have a 128-bit architecture and will leverage the high bandwidth of RAMBUS memory by incorporating a dual-channel RAMBUS into the design to get a data transfer rate of 1.2 Gbytes. The CL-GD5465 uses a single RAMBUS interface to deliver a transfer rate in excess of 600 Mbytes/s. Other advantages of RAMBUS memory are that it is as affordable as conventional



2. The CL-5465 3D graphics accelerator IC from Cirrus Logic is a third-generation device based on the company's TextureJet technology that provides efficient texture-map management. External RDRAMs allow textures to be loaded into the accelerator and to be updated quickly from off-screen graphics memory.

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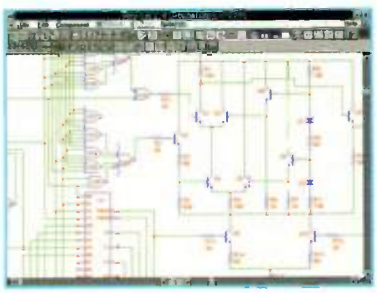

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DRAM, and it uses a high-speed, 8-bit interface that minimizes the number of controller pins required for the memory interface. This makes it possible to use the less expensive 208-pin IC package.

The CL-GD5465 *(Fig. 2)* is based on Cirrus Logic's TextureJet technology first unveiled last year in the Laguna 3D (CL-GD5464) product (ELECTRONIC DESIGN, *Dec. 2, 1996, p. 163*). The TextureJet architecture calls for a hardware texture manager and a sophisticated PCI/AGP bus mastering scheme. Along with the RAMBUS RDRAMS, it allows textures to be loaded and updated quickly from offscreen graphics memory. Textures are important because they enhance the 3D image, making it look more realistic.

Rendering High Performance

Gearing its products to the high performance end of the market, Dynamic Pictures has developed the Oxygen 3D graphics chip, a rendering and texturing processor. Unlike other developers of 3D graphics chips, Dynamic Pictures doesn't sell the chips to other board manufacturers, but instead sells its own family of 3D graphics controllers. They currently consist of the Oxygen 102, Oxygen 202 ,and Oxygen 402 accelerators. All the cards use the same basic chip and vary only in the number of graphics processors on the board—one, two or four chips respectively.

Intel, author of the AGP spec, has indicated that it will be releasing a number of graphics processor chips that are designed around the AGP bus. The first of these chips is expected to be the 740GT. Although Intel is not commenting on the chip, other than to acknowledge that it exists, rumors describe it as being able to support 800-by-600 resolution, 64 million colors, and deliver motion video at rates of up to 30 frames/s.

Able to leverage their experience with graphics workstations, designers at Intergraph have developed several 3D graphics solutions. At the high end is a three-chip set they use internally for a two-board set dubbed RealiZm3D. The chip set allows the board to perform dynamic 3D rendering at resolutions of up to 1824 by 1024 pixels at speeds exceeding 1.2 million, 3D lit, true-color Z-buffered Gouraud-shaded triangles/s, and up to 25 million bilinear filtered pixels/s.

Support circuitry on the chips allows the hardware to provide such effects as atmospheric haze, mist, and smoke, in addition to rendering and rotation. The three-chip solution covers the lower end of the graphics resolution and consists of a graphics engine and two resolver chips (a higher resolution solution adds two more resolver chips). A geometry accelerator can also be added to further speed the computations.

The resolver chips each provide up to 128 graphics planes, including double-buffered 24-bit true-color, 8-bit alpha and 8-bit stencil, and each perform the pixel operations on the contents of the 16- or 32-Mbyte frame buffer , which is accessed with either a 128- or 256-bit data path. The graphics engine chip, which accelerates polygon setup, rasterization, Gouraud shading, and antialiasing, also contains the texture processor which can address a separate texture memory of up to 64 Mbytes.

Chip Sets Deliver The Goods

Mitsubishi, in conjunction with Evans & Sutherland, has developed a chip set that aims to deliver the features and high performance of a 3D graphics workstation on a Windows NT platform.

Real 3D, a division of Lockheed Martin, has developed the R3D/100 chip set for 3D graphics acceleration. Real 3D has recently partnered with Intel to produce graphic chips, and it's likely that Intel's 740GT chip will use this technology. The R3D/100 chip set is designed for use with OpenGL and where real-time true 3D texture mapping is needed. It features an integrated geometry engine, graphics processor, and a texture processor.

The geometry engine delivers 66 MFLOPS of dedicated compute power for the setup calculations for drawing primitives, accelerated rasterization, and texture LOD calculation. Performing the graphics compute, the raster chip includes a full 32-bit RGBA Gouraud-shaded color path, and performs full 24-bit depth computations. Lastly, the texture processor delivers true perspective-corrected textures on image maps as large as 2048 by 2048 pixels. The chip includes up to 8 Mbytes of texture memory and handles a wide range of filtering algorithms and texture map formats. All three chips come in 352-contact BGA packages and as a set consume about 6 W from a 3.3-V supply. Together they deliver a throughput of up to 750,000 25-pixel lit, Gouraud-shaded, z-buffered, fogged, textured 3D polygons/s and up to 1.5 million 10-pixel z-buffered, fogged, stenciled 3D vectors/s.

Rendition has developed Verite V1000, a 300-MIPS processor that was designed for the add-in card market, specifically for game programs. The V1000 processor contains two main processing blocks, a RISC engine, and a pixel engine. The RISC processor is used as a setup engine. It has an instruction cache and a data cache. The pixel engine has a dedicated texture cache that it uses to perform texture mapping—the application of a two-dimensional image to the surface of a three-dimensional object.

The V1000 connects directly to the PCI bus via a bus-mastering interface. A 64-bit memory interface allows inexpensive EDO RAM to be used. Between 2- and 16-Mbytes of memory can be used. Jay Eisenlohr, vice-president of marketing at Rendition, says that advanced chain-command DMA is supported by the chip so its possible to get data transfer rates as high as 100 Mbytes/s.

Since today's games go up to 50 Mbytes/s for a frame rate of 30 to 40 fps, Eisenlohr says that the V1000 is more than enough to meet today's needs. He believes that games in the future will require more geometry processing and higher frame rates. The result will probably be a tripling of data transfer rates to 150 Mbytes/s. The cost of the Verite V1000 is about $40.

S3, a major player in the graphics interface arena, also has several 3D processor chips. The ViRGE/GX2 Home PC/TV accelerator is the first device of its type to include support for TV-output and dual display capability. This is on top of its support for AGP and Digital Video Disk (DVD) playback. It delivers a full set of 3D rendering features including MIP mapping, tri-linear filtering, and perspective correction of textures to create images that are free of annoying visual artifacts such as "sparkle" and

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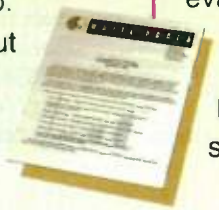

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"jaggies." The chip costs $29 in quantities of 10,000.

S-MOS Systems has a 3D graphics and rendering engine designated SPC1516 and nicknamed TEX. It features 800-by-600 resolution and a frame rate of 30 fps. Unlike many other chips, the TEX chip does not include the legacy 2D VGA accelerator/controller on the chip, and can be used in systems that already have a 2D graphics controller installed. This chip provides a superset of the features released in the company's previously-released PEX 3D processor that provided a low cost upgrade for PCI 2D graphics systems.

Based on a proprietary pixel-processing architecture called Pixelsquirt that was developed by Reality Simulation Systems, the chip can perform real-time Z sort operations. By doing such operations on chip, designers no longer have to store the Z-buffer data in local memory. That results in a significant savings in both memory cost and data traffic, particularly as image resolution increases (ELECTRONIC DESIGN, *May 1, p 83).*

Providing photorealistic outputs, the Pyramid3D graphics processor developed by TriTech Microelectronics combines a highly-integrated 3D pipeline with a geometry engine and pixel processor that renders images at up to 50 million pixels/s. To lower the chip cost for cost-sensitive applications, TriTech designers also offer the TR25202, which has no on-chip geometry processor.

The TR25201 can drive monitors at resolution levels of up to 1600 by 1200 pixels, and thanks to an on-chip "primitive" processor, can deliver more than 1 million triangles/s. Those triangles can be delivered with movie special effects such as radiosity texturing, bump mapping, Gouraud and Phong shading, optional Z buffering, edge anti-aliasing, specular intensity, multiple textures of the pixels, linear and nonlinear fog/haze, mist, blending and transparency.

A 3D controller chip for desktops, the 3D Image 985, was recently unveiled by Trident Microsystems. The chip includes DVD capability and is based on the company's rCADE3D accelerator and rendering engine. The chip supports SGRAMs and includes an on-chip setup engine and a video output processor. Housed in a 316-contact BGA package, the chip includes a double-speed AGP interface that operates at 133 MHz. Performance is further enhanced by using the AGP sideband addressing mode and by using remote storage of textures in main system memory. This results in a 20% to 50% improvement in speed while using a smaller frame buffer.

The rCADE accelerator provides a 3D rendering rate of 1.2 million polygons/s and the on-chip setup engine can free up the host CPU by offloading 50% of the 3D computing task. Que-based pixel processing conserves bandwidth while maximizing the time available for pixel drawing operations. Also

All About The Advanced Graphics Port

In April 1996, Intel introduced a method by which a graphics accelerator could directly access data stored in system memory. Called AGP for "Advanced Graphics Port," this high-bandwidth, low-latency connection to system memory allows all transactions between the host and the graphics accelerator to be processed quicker than normally possible with the PCI bus. The AGP interface is based on the PCI 2.1 bus specification, which has been extended to support a higher data-transfer rate. It does this by adding three major extensions to the PCI spec. First, it allows deeply-pipelined Read and Write requests to memory to hide access latency to main memory, along with faster transfer rates. Next, new sideband signals that allow the demultiplexing of address and data to overlap processing of memory requests are added, and higher bus clock rates (66 or 133 MHz) increase the bandwidth.

Consistent with the PCI 2.1 spec, AGP moves away from 5-V signals and requires only a 3.3-V signal for I/O. Although the PCI 2.1 spec is the basis for AGP, this new interface is implemented as a physically separate bus from the PCI or ISA buses, also requiring a different connector. The new connector is designed to meet the demanding electrical requirements of this faster bus and also allows for the new sideband signals. Seven new pins and several more ground pins are required to meet the higher data rates involved. Sixteen new signals are defined by the AGP spec, and all of them must be present on core logic chips. At least four signals are required for master devices (graphics chips), and most of the graphics controllers will need either seven or fifteen new signals, depending on which particular addressing mode is selected.

The additional number of pins required for the graphics controller will push most controllers from the traditional 208-pin plastic quad flat pack (PQFP) package toward a higher pin-count ball-grid-array (BGA) package which will handle the I/O signals and provide more groundlines to minimize signal noise.

Intel has already defined three modes of operation for AGP: A 1X mode that operates at 66MHz and has a bandwidth of 256 Mbytes/s; a 2X mode that operates at 133 MHz with a bandwidth of 512 Mbytes/s; and a high-speed extension to the original AGP spec that further doubles the speed to 266 MHz and 1 Gbyte/s. This 4X mode of operation is primarily targeted at high-end workstations and other high-performance platforms, and will be incorporated into the AGP specification during the fourth quarter of this year. AGP-based computer systems are expected to become available in the second half of this year.

The AGP can reduce the cost of implementing 3D systems because 3D applications not only require sufficient memory for on-screen data, but also enough memory to support 3D information such as z-buffering, and the storing of texture maps. This can boost the memory requirements of 3D to four times that is required for 2D applications. AGP-enabled systems can store textures in system memory, allowing for larger textures without the added cost of large frame buffers.

included on chip is a 64-bit 2D GUI accelerator, two hardware video windows that support video conferencing and reduce CPU loading by as much as 30%, and ClearTV, a technology that scales the CRT image into an NTSC/PAL TV signal without the loss of edge and corner data and without flicker.

One of the earliest companies providing 3D graphics chips, 3Dlabs has now evolved the chips through several generations, from the 1995 release of the Glint 300SX for high-end systems and the Permedia I chip in 1996 for cost-sensitive systems. Also released to support the Glint or Permedia processors was the Delta setup engine which helps accelerate the geometry pipeline processing. Now, 3Dlabs has the second-generation families soon to pop out of the oven, starting with the Gamma chip.

The Gamma chip is the first of the company's products to be AGP-compliant and the chip designers incorporated a complete geometry and lighting pipeline, a first for commodity 3D graphics chips. Therefore, the chip will be able to accelerate the complete 3D geometry pipeline, including transforms, lighting, clipping, and setup processing. The resulting throughput yields a processing capability of 3.3 million polygons/s (with transforms, lighting, and backface culling enabled capabilities).

The on-chip computing power of the geometry engine provides 1 GFLOP of floating point processing power, freeing the host CPU for other tasks. It contains a hardwired floating point processor that requires no RAM or ROM for program storage and no program sequencer or instruction set.

Following the release of their 1 million polygon/s Glint 500TX processor in the latter half of 1996, designers at 3Dlabs set their sights on a next-generation design for release later this year. The Glint MX processor will deliver two to five times the performance of the 500TX, and yet will be hardware and software compatible. Also coming in a more highly integrated version of the Permedia processor, the Permedia II, which includes an on-chip RAMDAC and 100 MFLOPS Delta setup engine and MPEG-2 acceleration capability.

Available for about one year, the Power VR chip, developed jointly by NEC Electronics and Video Logic Ltd (United Kingdom), has been used in various graphics cards and computers (the Compaq Presario computers, for example). The next generation Power VR chip, the PCX2, improves the image quality, provides higher display resolutions, and reduces system costs vs the original chip set. The company claims the the chip can out perform chips such as the Voodoo Graphics chip from 3Dfx by up to 40% and the S3 Virge processor by at least an order of magnitude.

When running the Microsoft Direct3D benchmark, the chip delivers a sustained fill rate of 40 Mpixels/s when executed on an Intel Pentium Pro 200-MHz system with 640 by 480 pixel resolution, a 16-bit color palette and a 75-Hz display. The benchmark result is about 25% better than most rivals. To achieve such results, designers enhanced the logic to first support higher resolution images, both 800 by 600 and 1024 by 768 pixel screens with 16- or 24-bit color. .

At last month's Microsoft sponsored Windows developers conference, a new family of graphics engines dubbed the Big Cats family (the first chip was internally code named Tiger), was unveiled by Philips Semiconductors. The first two chips in the series, the SAA9725 and 9726 provide 2D and 3D graphics capabilities respectively, and a follow-on chip, the SAA9727 will include a higher performance 3D engine that supports full triangle setup at a rate of 1 million triangle/s, as well as MPEG-2 video and MCA/AC-3 audio decoding for DVD playback. The chips will support 2-, 4- or 8-Mbytes of SGRAM, SDRAM or EDO-RAM and incorporate a 220-MHz RAMDAC that will allow screen resolutions of up to 1600 by 1200 pixels with pixel depths of up to 32 bits. The first two chips will have PCI interfaces, while the SAA9727 will also offer an AGP interface option.

In addition to the dedicated 3D graphics chips, designers at Philips have, for the past 18 months, been developing a multifunctional architecture employing a very-long-instruction word processor. The Trimedia TM-1000 can not only handle the audio and video manipulation, but also can support 3D graphics. Initially released for operation with a 100 MHz internal clock speed, an enhanced version that can run 30% faster (133 MHz) gives the chip more bandwidth to do more. The wide instruction word allows the chip to perform multiple independent operations in parallel (up to six operations), allowing the chip to readily handle the complex computations that are needed for 3D graphics or multimedia applications.

To feed the processor the data and commands so that it can execute at such a high rate, dual RAMBUS memory ports on the chip provide an aggregate memory bandwidth of up to 1300 Mbytes. Additionally, the chip's internal cache was doubled to 8 kbytes from the previous 4 kbytes employed the Mpact 1. Further, to enhance 3D texturing, a 2-kbyte texture cache was also integrated on chip.

Part of the high throughput is also due to to the addition of a scalable 3D pipeline that delivers close to a tenfold improvement in 3D graphics performance versus today's available accelerators. An on-chip floating-point unit deliver over 500 MFLOPS of compute power for 3D geometry and setup operations as well as for other multimedia functions. At 1 million triangles/s (50 pixel, textured, Gouraud-shaded, Z-buffered, perspective-corrected, bilinear filtered, and alpha-blended with fog), the MPact 2 processor should let the chip compete in the high end segment of the market for late 1997 and 1998. But like the Trimedia processor, the MPact 2 does much more that just graphics. It also can deal with multimedia video and audio streams.

Although SGS-Thomson has a deal with Chromatic for the media processor, they are involved with NVidia to develop a graphics-only solution to 3D imaging. The result is the RIVA 128, a 128-bit 3D multimedia accelerator that provides 2D and 3D graphics at commodity prices.

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Dave Bursky may be reached at dbursky@class.org.

How Valuable	Circle
Highly	600
Moderately	601
Slightly	602

PRODUCT FEATURE

Data sheets on products like these can be found at www.penton.com/ed/

Accelerated 3D Graphics Controller Delivers Workstation, Arcade Performance

Operating at the full 133-MHz clock rate of the advanced graphics port interface, the 3D Rage Pro graphics accelerator from ATI Technologies delivers 3D imagery at performance levels befitting a workstation or arcade graphics systems. While the chip unleashes the full potential of the AGP interface, it takes advantage of 100-MHz synchronous graphics RAMs, an on-chip floating-point setup engine, an internal 4-kbyte texture cache, an integrated 230-MHz output DAC, and enhanced MPEG-2 motion compensation to provide the high throughput. When evaluated with the WinBench 97 benchmark, the Rage Pro delivers a rating of over 100 million when driving a 1024-by-768-pixel display with 16 bits/pixel.

The internal floating-point setup engine can deliver a throughput of 1.2 million triangles/s, greatly improving the performance of small triangles that add detail to 3D scenes. The chip also provides a fill rate of up to 75 million textured pixels/s. Thanks to the 133-MHz AGP mode, the controller has access to large amounts of main memory textures through the AGP execute mode or PCI scatter-gather bus-master mode. Larger textures allow the circuit to provide more detail and realism than has previously been available in 3D content.

In addition, the 4-kbyte on-chip texture cache reduces memory bandwidth requirements and latency. The processor also incorporates texture compositing, single-pass trilinear filtering, specular highlighting, video texturing, and vector-quantization texture decompression.

By offloading the setup function from the CPU, the 3D Rage Pro significantly improves the performance of the entire 3D pipeline by allowing the CPU to focus on 3D geometry and lighting transformations. Most other setup engines only accept fixed-point parameters, which requires the CPU to perform the floating-point to fixed-point conversion. Such a conversion requires about 100 CPU clock cycles, which consumes much of the CPU's resources.

A 64-bit-wide interface on the SGRAM memory port allows the port to pull in data at up to 800 Mbytes/s from the low-latency frame buffer. That bandwidth is higher than that of any other mainstream graphics processor, and matches the high throughput needs of the AGP interface. Furthermore, the memory interface also can support standard or EDO DRAMs, synchronous DRAMs, or dual-ported window RAMs. Memory

sizes of 2 to 8 Mbytes are supported by EDO, SDRAM, or SGRAM, and from 4 to 16 Mbytes by the WRAM.

In addition to the 3D performance enhancements, the 3D Rage Pro also provides support for digital-versatile-disk (DVD) subsystems as well as MPEG video playback. To accomplish that, the chip incorporates enhanced motion compensation acceleration, four-tap horizontal and two-tap vertical DVD scaling circuits, a de-interlacing filter, a video-on-graphics-overlay capability, the ability to handle multiple video streams and perform color-space conversion, scatter-gather bus mastering, and a planar YUV mode. Furthermore, the circuit includes the ATI Multimedia Channel (AMC) video input port and supports high-quality NTSC and PAL TV outputs with the optional companion ImpacTV chip.

The motion-compensation enhancements go beyond the compensation circuits first released in the company's 3D Rage II+DVD chip. By offloading the computations from an MMX-capable CPU, the 3D Rage Pro improves the software DVD/MPEG-2 frame rate by 20 to 30%. That will allow the company to offer a low-cost hardware DVD solution by using the IBM MPEG-2 decoder that connects to the Rage Pro via the AMC port. This enables the system to deliver no-compromise full-frame-rate DVD playback.

Able to support display resolutions of up to 1600 by 1200 pixels with refresh rates of 85 Hz, the on-chip 230-MHz DAC allows systems to meet the European or U.S. display refresh requirements. For even higher performance systems, the chip can be configured to work with the dual-ported window-RAMs and an external 250-MHz DAC. To provide higher-quality images, the chip is the first commercial graphics circuit to also include edge antialiasing, a feature most CAD users deem a necessity.

To provide quick response to display operations, the Rage Pro includes a 128-level-deep command FIFO buffer. Control registers are 32 bits wide and are memory mapped for easy setup. Both the DDC1 and DDC2B+ serial interface for plug-and-play monitors are included, as is power-management logic for full VESA DPMS and EPA Energy Star compliance. Upon power-up, the chip also performs several diagnostic tests, and a built-in scan port allows for simple external testing.

Drivers are available for all popular operating systems and application programming interfaces, including Windows NT 4.0, NT 5.0, Windows 95, Memphis, OS/2, MAC OS, DirectX, OpenGL, Heidi, and QuickDraw3D. That allows support for 3D applications such as the Cosmo player VRML 2.0 browser from Silicon Graphics Inc.

The chip comes in a 256-contact ball-grid-array package, and in lots of 10,000 units sells for $30 apiece. Samples are immediately available. Also available are a 66-MHz AGP version with a 200-MHz DAC and a PCI-version of the chip for systems that need an even lower-cost solution—the chip includes a 33-MHz PCI interface and comes in a 208-lead PQFP. It's pin-compatible with the previous-generation 3D Rage II+DVD controller.

ATI Technologies Inc.
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Thornhill, Ontario, Canada, L3T 7N6
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http://www.atitech.com.

CIRCLE 640

DAVE BURSKY

PRODUCT FEATURE

Data sheets on products like these can be found at www.penton.com/ed/

Two-Chip Set Simplifies CCD Camera Subsystems

The CS7615 and CS7665 provide the timing signals, analog-to-digital conversion, and color-space conversion necessary to transform the output of a CCD imaging chip and deliver a YCrCb data stream. Developed by Crystal Semiconductor, the chip set can work with virtually any four-phase vertical CCD array, with array dimensions ranging from 175 to 1000 pixels in the X or Y directions. The on-chip timing generator uses an external master clock or crystal, and the internal phase-locked loop provides the internal master clock for the timing generator.

The CS7615 contains all of the analog processing circuits, including a 10-bit ADC, the multi-sync CCD timing generator, an integrated correlated double sampler, a 38-dB automatic-gain-control block, a block-level clamp circuit, and an inter-IC serial port for chip-to-chip communications with the companion circuit and the rest of the system. The analog output of the CCD array can be connected directly to the CS7615's inputs, thus eliminating the need for an external buffer amplifier. The pixel data then is double sampled (to improve noise performance) and gain adjusted, prior to being digitized by the ADC. Feedback from the ADC holds the image black level at code-16, easing compliance issues with the ITU-601 standard.

The chip supports full ITU-601 compliance for imagers up to 720 pixels wide, and is compatible with both NTSC and PAL timing requirements. In addition, the circuit can be programmed to operate with imagers ranging from 175 to 1000 pixels wide, allowing lower- or higher-resolution imaging arrays to be used.

The CS7665 digital video color-space processor, which supplies the rest of the functionality needed for the camera, generates the 4:2:2 component digital video output signals. The chip accepts the MYCG data from the CS7615 and processes the data into the YCrCb formatted component digital video. This provides individual Hsync, Vsync, and Href signals along with the video data to support older analog video encoders and the current zoom-video port definition.

Internal processing includes color separation, automatic white balance adjustment, (user) programmable gamma correction curves, square pixel interpolation, and output formatting. Configuration data also is loaded into the chip over its inter-IC serial interface, while a limited, secondary inter-IC bus master provides a host-system interface for downloading setup parameters.

Included is an advanced color anti-aliasing filter that prevents both incorrect color and color noise—factors that can undermine image quality in compression-based systems. Consequently, problems such as "rainbow" effects and sparkling or false colors can be eliminated with a special glass filter. Furthermore, the chip includes programmable saturation control and fully-programmable color separation matrix coefficients.

The CS7615 and 7665 come in 44- and 64-lead thin PQFP packages, respectively, and as a chip set sell for $35/set in lots of 1000 sets. In large OEM quantities, the price drops to less than $15/set. Samples are available from stock.

Crystal Semiconductor Corp.
P.O. Box 17847
Austin, TX 78760
Alan Hansford, (512) 445-7222.

CIRCLE 641

DAVE BURSKY

3D Graphics Accelerator Adds Realism To Laptops

By optimizing its high-performance Virge 3D accelerator core and the circuitry around it for portable systems, designers at S3 came up with the ViRGE/MX, a 3D/2D graphics accelerator for notebook computers. It's the first notebook chip to include a TV-out NTSC encoder as well. This improved 3D accelerator, as opposed to the company's previously-released Aurora64V+ chip, is targeted at high-performance notebook computer applications. ViRGE/MX can support both LCD and CRT monitors as well as provide a high-quality NTSC or PAL composite output thanks to a 3-tap adaptive flicker filter. That output can drive video monitors and VCRs. The chip also provides an S-video output.

The DuoView display mode enables simultaneous display of different images on the notebook LCD and a connected video monitor. Consequently, presentation applications and other applications that need more display area can make use of the second display more effectively. To handle the dual screens, the ViRGE/MS includes independent refresh-rate support so that the notebook LCD can be run at 800 by 600 pixels, while a monitor might be configured to display data with 640-by-480-pixel resolution.

To deliver the high throughput needed for 3D and 2D graphics, the ViRGE/MX controller packs a 64-bit memory interface that can tie into either synchronous graphics DRAMs (SGRAMs) that clock at 83 MHz or extended-data-out DRAMs (EDO DRAMs) operating at 66 MHz. The SGRAMs will provide the highest-performance system solution, but the EDO DRAM alternative can be implemented at a low cost, allowing the computer manufacturer to offer a lower-cost alternative to the high-end model.

As part of the 3D graphics capability, the chip includes an advanced 3D rendering capability that performs Z-buffering, perspective correction, and transparency operations, as well as bilinear/tri-linear filtering, MIP-mapping, and even atmospheric effects. Both flat and Gouraud shading and texture mapping also is possible on the images. The video playback portion of the chip also contains some advanced features to ensure good images—the circuits perform horizontal and vertical interpolation, chroma-key and color-key determination, RGB to YUV color-space conversion, Alpha blending, double buffering, and HSB control. These features help reduce flicker when play-

(continued on page 129)

A PENTON PUBLICATION

MAY 1997

CAREER OPPORTUNITIES

IN ELECTRONIC ENGINEERING

Strategies For Professional Development

A Special Career Supplement To:

WIRELESS SYSTEMS DESIGN

ELECTRONIC DESIGN

Microwaves & RF

THROUGHOUT THE WORLD, THERE'S ONE WORD FOR

communications test solutions:

Manufacturing Engineer
The primary responsibility of this new position is to fully support the transfer of RF/microwave products from Japan to Morgan Hill. A BSEE/BSET or equivalent and 3+ years' experience in RF/microwave instrument manufacturing is required. **JOB CODE 900S**

Applications Engineer
Individual will be involved in all aspects field technical support to include, installation support, equipment engineering support, ATPs, customer service support, field & beta trials, training. BSEE or AA in electronics degree or equivalent, 5 to 10 years minimum experience with a telephone company in the areas of tech support, or equivalent maintenance engineering in the private line area. Experience with a centralized private line test system highly desirable experience with Pcs using communications programs and terminal emulation desirable. **JOB CODE 761M**

Product Marketing Engineer
This technical staff position will support the Vector Network Analyzes/Component Test product line by writing application notes, performing product evaluations, conducting product demonstrations, & organizing and delivering new product and competitive information. Position requires approximately 20-25% US/International travel. BS in Engineering/Physics or equivalent technical experience excellent verbal/writing skills, knowledge of microwave and millimeterwave markets are desired. **JOB CODE 720R**

Test Engineer
Will make precision instrumentation for the rapidly growing wireless communications industry. Will work on complex RF and microwave equipment in calibrating, troubleshooting and improving production processes. Must possess a BSEE or equivalent, excellent technical, verbal and written skills, with RF and microwave knowledge a definite plus. Strong problem-solving and root cause analysis also required. **JOB CODE 900S**

Manufacturing Engineer
Support production with product flow analysis for an exciting, new, portable RF measuring instrument line. You'll be part of an energetic cross-functional team to assist with development/definition of next generation of products/test methods. Requires a BSEE or equivalent with strong analytical skills and the ability to communicate effectively. **JOB CODE 470T**

Embedded Software Engineer
Develop embedded software for a high volume portable product used in the cellular communications market. Work also will include occassional embedded hardware design. Bring your energy and enthusiasm to this fast paced, dynamic team! A BS/MSEE/CE or equivalent and 1+ years embedded system experience necessary. **JOB CODE 610B**

Visual Basic Development Engineers
Software Developers are needed for a client-server Network Test and Management product on Windows 95/NT. Responsibilities include all aspects of product development. Requires a BSCS (MS preferred) and 2+years' experience. A strong software methodology background in C/C++, experience with setting up and configuring Windows 95/NT environments and VB3/4 is essential. X.25. TCP/IP(winsock) and DLL writing experience a plus. **JOB CODE 650J**

RF Design Engineer
RF and system design from requirements definition through production release. You will be involved with product definition, design, and performance verification. A strong background in high frequency RF design, analog circuit design and strong analytical skills, along with your ability to handle engineering assignments with little guidance are a must. Familiarity with Vector Network Analyzers and design experience with RF/Microwave test equipment are a plus. **JOB CODE 610R**

Microwave/Millimeter Design Engineer
Responsible for Microwave/Millimeter component and sub-system design, from requirement definition through product release. Requires knowledge of Touchstone or Libra (similar CAD) and 3+ years' related engineering experience. You should be familiar with Mixer, Frequency Multiplier, Oscillator, Filter, Switch, Coupler, Up/Down Converter in Microstrip, Suspended Substrate, Finline and Wave-Guide. A MSEE or equivalent is preferred. **JOB CODE 620L**

Software Engineer
Be responsible for the generation of module level specifications, coding documentation and testing of programs. To qualify, you must have a BSCS/MSCS or equivalent and 3+ years' experience. Proficiency in C, C++ programming designing Motif GUI and practical experience with embedded SQL utilizing Oracle and Informix RDBMS is essential. Knowledge of Solaris, OSF/I, telephony, BellCore specifications and experience with rule based systems are a plus. **JOB CODE 650O**

Engineering Manager (Systems)
Manage a group of engineers chartered to design specialized RF and microwave instrumentation systems. Interface with customers to determine system design requirements. Requires a BSEE or equivalent (MSEE preferred) and 10+years' experience in microwave instrumentation design. Knowledge of microwave communication, radar and electronic warfare systems, a plus. The candidate should have both interface and ATE test experience. **JOB CODE 610G**

Product Marketing Manager
Define and oversee market strategy for our portable instruments product line. Responsibilities include market research, new product definition, promotion, and application support. Requires a BSEE or equivalent (MBA preferred) plus experience in RF/microwave measurements. Knowledge of s-parameters, wireless communications measurement techniques and a good balance of business, technical and people skills are key. **JOB CODE 720M**

R&D Section, Manager, Windows
Managing a team of development engineers, you'll focus on software and systems architecture including Object-Oriented Design and Network Management (TMN and SNMP). Requires a BSCS or equivalent (MS preferred) and 7+ years' experience with TMN, CMISE and SNMP management platforms. Language skills should include C, C++ and Visual Basic. **JOB CODE 650P**

North American Regional Marketing Manager
Represent Wiltron MMD in North America. Interface with customers and the AW sales organization. Make decisions regarding overall sales strategy (market share) in the region and provide feedback to product marketing. Good understanding of RF and microwave products and North American Market is essential. **JOB CODE 731S**

Product Manager — RFTS
Responsible for product marketing of the Anritsu Wiltron remote fiber-optic test systems (RFSTS). Oversee all phases of product cycle from new product definition and justification, to pricing recommendations. Requires a BSEE or equivalent and 5+ years' in marketing. Travel is required. **JOB CODE 800P**

Director of Marketing
Organize and supervise the marketing department for all Telecom division products. Lead the division strategic planning process. Manage and recruit product managers to achieve marketing objectives. BSEE and MBA preferred and 15+ years' experience, preferably in marketing. **JOB CODE 800P**

Mechanical Design
Design and document instrumentation enclosure and assembly including sheetmetal, mechanical and cast components. Perform environmental analysis and testing of completed instruments. Requires a BSME or equivalent and 3+ years' related experience. Familiarity with plastic injection molding, die casting, DFM, sheetmetal and part design is a plus. **JOB CODE 610T**

Staff Accountant Analyst **JOB CODE 810H**
Test Technician **JOB CODE 470W**
Buyer/Planner **JOB CODE 510L**

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an Anritsu Company

Electronics Engineers Will Be Among The Few

COLLEGE GRADUATES WILL STILL BE IN DEMAND BY COMPANIES IN TEN YEARS

Paul McGoldrick

The numbers being produced by the State Employment Departments in the western U.S. should be of concern for those leaving college in the next ten years, unless you are an engineering graduate. The number of jobs requiring a college degree are being estimated such that 1.5 graduates will be chasing each job that will be available. In the same time frame nearly five times as many jobs will be created but they will require only a high school diploma or on-the-job training; and guess what? There will be a shortage of about 30% of people to fill those jobs.

If ever there was a reason to get good grades in college, the above surely tells it all; if you graduate in the lower third, you will have effectively wasted the time and money it took to put you through the process. With the choice of employees available, there will be a softening of salaries for the college-educated jobs. Inevitably, there will be a general increase in remuneration for the lower-education jobs, plus an overall push by those who need the employees for easier immigration laws and requirements. At the moment, it is relatively easy to bring

AREA (business) needs	Major vacancies
SAN DIEGO	
Applied Digital Access (network management)	Software engineers for SNMP, real-time and embedded applications. ASIC design engineers. SONET/ATM/Frame Relay software engineers. SONET hardware engineers.
Brooktree (multimedia/graphics/VLSI) All BSEE or higher All levels	Multimedia design verification engineer. Multimedia senior IC design engineer. Multimedia senior software engineer. Graphics IC design engineers. Graphics DSP engineer. Graphics software engineer (Windows.) VLSI senior design engineer. VLSI senior software engineer. VLSI staff design engineer.
Camino NeuroCare (critical care monitoring products) Both BSEE or higher Both 4+ years experience	Senior software engineer for C and assembly language. Quality engineer for new product safety and quality.
CliniComp International (electronic patient charts for hospitals)	Director, hardware engineering for digital, RISC and display systems. Embedded systems software engineers, design and maintenance. Software engineers.
ComStream (digital communications) All BSEE or higher All 3+ years experience	ASIC designers for cable modems, burst and SCPC satellite, and PC transport. Systems development engineer for burst and SCPC satellite systems. Hardware engineer for RF, analog, digital DVB, MPEG and FPGA. Telephony engineers for interface and signaling.
DENSO (CDMA/PCS products)	Senior embedded software engineers with C/C++. Senior software engineers for call processing.

a degreed person into the country and very difficult to bring in, for employment purposes, someone less educated. This could be looked at as a "dumbing-down" of the workforce, but it is in fact a reduction in the costs of the workforce, with the creation of so many service-type positions and an effective watering down of the entry-level degreed person's salary. Fortunately for our profession, it is still estimated that in ten years there will be 0.8 electronics engineers chasing each opening. That is, of course, if you are the employee and not the employer. It is still true today that good design engineers can really only be unemployed if they want it that way, or even deliberately go about it. In other engineering areas, there are other hot spots as well.

Firewalls

In the magazine business, we frequently have meetings with both marketing people and design engineers at companies. In our own specialty areas, we know the really good engineers and their products because of the way that they approach them and the results they achieve. Fortunately, there is a firewall between information we are exposed to and the recruiters and HR people of other companies, but it certainly can be said that technology editors at magazines see more of the aptitudes that are available than many managers do. At a recent meeting with an analog semiconductor company, the design engineer for two different products was present; both designs were top- notch; both were realized on the first pass of silicon; both will make the company a lot of money; and both were developed in parallel. Joking with him about how the company better be looking after him, he told me the status of his salary, bonus, and stock plan as a kind of check against market value. He has nothing to be worried about.

Three thousand people a month have been entering Santa Clara County.

But where are the current vacancies in the engineering market? As always, most of them are in Silicon Valley, but hot areas exist in San Diego, Oregon (Silicon Forest), North Carolina, and the Greater Los Angeles area (the Southland to television newscasters.) If you are looking for a job in Silicon Valley and you don't live there already, you should be aware of a few things. The first is that you are not alone; 3000 people a month have been entering Santa Clara county in the last year. That has put incredible pressure on the housing market with rental prices increasing about 50% in one year, and the availability of reasonable housing extremely limited. A great time for sellers, a lousy time for buyers.

At the same time, the overall level of unemployment in the Valley is so low that getting any kind of support staff is difficult, and once you have them, you need to be real nice to keep them. Valley life is reflected pretty well in the *San Jose Mercury News* where the employment ads now reach an average of 5 pages for the "Computer" category and about 8 pages for the "Engineering" category. Surprisingly, there are now more ads in the Monday issues than Sunday. Advertisements also are on billboards, radio, and TV commercials, and even in the sponsorship messages on the local PBS station (KTEH.)

In Oregon, the newspaper of record is *The Oregonian* and the Sunday issue is now running about 6 pages of high-tech jobs in a much more difficult-to-read format. Quality of life in the Portland area is not nearly as high as it used to be. Houses in Beaverton, the electronic suburb of Portland, are now fetching $150,000 to $200,000. That is still way below the $300,00-$400,000 range of Santa Clara county but there is, as yet, no equivalent of proposition 13 in Oregon to limit property taxes. And while there is no sales tax and gas is 20 cents per gallon cheaper than California, personal income tax is quite high. The same is true of

Northwest Washington. At the southernmost end of the state, a suburb of Portland, is a small, but growing, high-tech area in Camus fueled by the building of some wafer fabs, not all of which are yet in operation. At the northern end of the state, the areas of Tacoma, Seattle, and Everett are dominated by software and Boeing, while the growth city is Spokane. There is still aerospace and a growing number of electronic companies. One advantage of living in the south of Washington State is that there is no state income tax and sales-tax-free Oregon is just a bridge away. (But don't try to live in Washington and register your vehicle in Oregon: they will get you!)

San Diego Boom

The greatest boom in the last six months has been the San Diego corridor; it is almost like every manufacturer got the same idea at the same time. Although San Diego is a delightful area to live in, there are major traffic problems to and from the industrial parks. But if you are an RF engineer with a free spirit and a love of the outdoors, there could be a lot worse places to work and live.

Silicon Valley has its own rules about the market for engineers; there is basically no area of expertise that does not have work available to the experienced engineer. For entry-level, there are numerous opening at the established manufacturers and the applicant only really need satisfy the interviewer that he or she is aware a business is there to make money and that he wants to design successful products. Nobody wants to hire trouble; that is all too easy to do.

So, this issue we are focusing on some other areas of the country with what is available *(see the Table)* and as can be seen the RF designer is still way up there on the needs list with a surprisingly good showing for VLSI design. In

AREA (business) needs	Major vacancies
SAN DIEGO Cont'd.	Senior digital hardware engineers for micro controllers, memory, audio. Senior RF design engineers. Senior communications systems engineers for CDMA and IS-95.
General Instrument (network communications) All BSEE or higher Most 4+ years experience	Real-time embedded firmware developers for digital satellite receivers. Systems integration engineer for satellite, broadcast, or cable distribution. CMOS/VLSI engineers for high-speed designs.
I-Bus (backplane technology) All BSEE or higher Most 5+ years experience	Senior design engineer with microprocessor design experience. Software engineer for Intel Assembly and C languages. In-process quality engineer.
Kokusai Comm. Systems (digital cellular and PCS)	RF engineers for front-end systems and modulators/demodulators design. Baseband engineers for CDMA, GMS, CDMA, CDPD. Software engineers for digital cellular products. Cellular field test engineer for across-the-board testing.
L G InfoComm (CDMA/PCS development) All BSEE or higher All 2 + yrs. experience (college grad program)	C/C++ software engineer for CDMA/IS-95 mobile terminals or digital switches. RF systems engineers for application programs in C/C++/Chill. DSP engineers for voice codec algorithms. ASIC engineer for logic-level design of mobile terminals.
Nokia (cellular/PCS products) All BSEE or higher Most 3+ years experience (some entry-level)	RF design engineers for front-end work. RF transmitter design engineers up to 2 GHz. RF systems engineers to simulate RF system architecture. RF synthesizer design/PLL engineer for up to 2 GHz. Software engineer for Windows-based PC tools. Cellular software engineer for embedded systems or communications protocols.
QUALCOMM (CDMA products) All BSEE or higher	Software engineers for embedded systems, telephony protocols in C/C++. Digital systems engineers. VLSI Spice Modeling engineers to characterize for foundries.

AREA (business) needs	Major vacancies
LOS ANGELES/SOUTHLAND	
Aerojet (space-based systems) All BSEE or higher All levels	Digital circuit design engineers for mixed-signal and digital ICs. Systems analysis engineers for EO sensor systems. Software engineer for mission ground data processing.
Litton Guidance and Control (test equipment) BSEE + 5 years experience	ATE software engineers with C/C++ and JAVA.
Rockwell Semiconductors (VLSI and modems)	RF IC design engineers. Mixed signal VLSI design engineers. ASIC design engineers Device validation engineers. GaAs transmitter design engineer. GaAs design engineer (characterization.)
Silicon Systems (mass storage ICs)	Servo control engineer for hard disk and optical disk. Systems engineer for reading, modeling and simulation with C and MATLAB.
Teradyne (VLSI and Memory Test) All BSEE or higher	Hardware design engineer (Memory) for ASICs, PCBs, systems. Analog/mixed-signal design engineer (Memory.) Software communications engineer (Memory) for inter-process comms. System software engineer for hardware/software interface architecture (Memory.) Hardware development engineer (VLSI) for high-speed ASIC/FPGA. Analog design engineer (VLSI) for data acquisition and power electronics. Software design engineer (VLSI) for ATE control with C++.
NORTH CAROLINA	
Ericsson (wired and wireless comms.) All levels of experience	Electrical engineers for design of baseband analog and audio for high volumes. QA and verification engineers for hardware and software. Embedded systems software engineers with C/C++.
Hot Chips and Salsas (processor for multimedia) All BSEE or higher	Logic design engineers for internal bus controls, cache, and interfaces. DSP software engineers with experience in MPEG/3D/audio codecs. *NOTE: Salsas is "Systems And Lots of Software Applications."*
WASHINGTON	
Hewlett-Packard (wireless communications)	Software productivity and tools engineer for embedded systems development.
Packet Engines (Gigabit Ethernet)	Digital ASIC designers for standard cell and gate arrays. Deign engineer for PCB and systems-level networking products. Software engineers for Ethernet bridging with C/C++. Software diagnostics/test engineers for systems protocols
TEXAS	
Dell Computers (PCs and workstations) All levels of experience	Hardware design engineers for systems and motherboard designs.

AREA (business) needs	Major vacancies
TEXAS Cont'd. NORTEL (digital telecomms.)	RF engineering design managers. ASIC design engineers. Hardware engineers. Software design engineers. Senior RF design engineers.
FLORIDA Digital Lightwave (high-speed networks) All BSEE or higher Most 2+ years experience	Hardware engineer for FPGA/ASIC design for high-speed ATM/SONET/SDH. Software engineers for C/C++ embedded systems. Systems test engineer for telecom testing.
NEW MEXICO Philips Semiconductors (telecomm. ICs)	Test engineers for mass-storage, programmable, and IEEE-1394 products.
NEW JERSEY Anadigics (GaAs devices) All BSEE or higher	Senior design engineers for fiber and linear MMIC amplifiers, clock-recovery ICs. Senior RF component design engineers for FETs, diodes, and passives. Advanced GaAs design engineer for PAs, receivers, and bias stabilization. Cellular radio-controller designer. Test engineers for production and probe.

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Applications Engineers (3 openings)

Responsible for in-factory technical support of RF semiconductors, including design of demonstration circuits, authoring of application notes, creation of design tools, focused design-in support to customers, and support of new product introductions. Requires a BSEE, 2 years' applicable RF design experience, some WW customer travel, and excellent written/verbal communications and presentation skills. Knowledge of simulation programs (Touchstone, MDS, SPICE) preferred. Openings to support: power devices and transistors; building block mixers, modulators, and amplifiers; device modeling. **Ad #5104**

GaAs Power MMIC Design Engineer

Design cellular/PCS power amplifiers and other front-end components in state-of-the-art PHEMT GaAs technology. Work with marketing and RF system engineers to define products for emerging PCS cellular/cordless handsets and wireless data terminals in the 0.8-6.0 GHz frequency range. As part of a cross-functional team, support the product characterization, transfer to high-volume manufacturing and development of customer application support. Requires an MSEE/PhD plus 3 years' experience or a BSEE plus 5 years' experience in GaAs MMIC design. Relevant experience should include at least one commercial handset power product successfully transferred into production. Strong communications and interpersonal skills are also essential. Occasional travel required. **Ad #5105**

RF Circuit Design Engineer

Design and develop new RF Power Products (100mW-4W) using both GaAs FET and Si BJT technologies. Perform electrical and mechanical simulation, verification and characterization, interactive refinement, and documentation resulting in products suitable for high-volume offshore manufacturing. Requires a BSEE with 3 years' experience in RF Power Amplifier design. **Ad #5106**

Test Engineers (2 openings)

As a leader or key member of a product development team you will have responsibility for test engineering tasks associated with development of new semiconductor products. Perform detailed characterization of new transistors and RFICs including test system definition, test fixture development, DC and RF wafer probing, test board design, test software development and test system integration with auto-handling equipment. Perform statistical and error analysis of test data, work with manufacturing engineering to ensure smooth transfer of new products from R&D to Manufacturing, and participate in data sheet and application circuits definition and development to ensure the success of new products. Requires a BSEE and expertise in at least one of the following: high frequency testing, ATE software development, ANA error correction and calibration techniques. Desired experience in: automated source- and load-pull test, RF test using auto-handling equipment, high frequency wafer probing, and project management. **Ad #5107**

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Work with HP internal and external semiconductor IC suppliers to develop, update and improve the quality of CAD tools. Use Cadence Analog Artist and HP-EESOF tools to develop libraries, integrate device models into the schematic capture tools, develop parameterized layout cells, write extraction and design verification rules, and customize the Cadence environment to improve the user interface. Investigate new tools and look for new methodologies to improve designers' efficiency and reduce development cycle time, work with design kits from various IC suppliers to provide on-site support, development and training. Requires a BS or MS in electrical engineering or related discipline and at least 3 years' experience with Cadence Artist tools or related software. Experience with programming is helpful as well as familiarity with semiconductor processing. Excellent written/verbal communication skills desired. Some travel may be required. **Ad #5108**

Silicon RFIC Design Manager

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Interviewing The Interviewer: Questions An Engineer Should Ask

RECRUITERS AND HR PERSONNEL FEEL IT IS IMPORTANT FOR ENGINEERS TO ASK QUESTIONS DURING AN INTERVIEW.

Robert Keenan

In today's volatile electronics market, engineers are a prime commodity. To fill engineering positions, companies have turned to constant advertising, trade shows, career shows, and technical recruiters to find and fill their engineering openings. As a result, today's engineers find themselves receiving more phone calls from recruiters and attending more interviews.

The interviewing process can be one of the most stressful parts to any hiring process. In entering any interview, an engineer needs to be prepared to answer questions and sell themselves to a company's human resources staff and engineering management.

But, the interviewing process is not just a stage for companies to find out information. It also is an arena for engineers to find out as much information as possible so they can decide whether this is the right atmosphere and company to work for. To make this determination, engineers must ask questions during the interview to flush out as much information about the position and company as possible.

In *The Essential Book of Interviewing* (Times Books, 1995), Arnold Kanter says that the interview process is designed for both the interviewer and interviewee to obtain information. "Indeed, as the hiring process continues, the interviewee becomes as much the information gather as the information giver."

In his book *The Perfect Interview: How To Get The Job You Really Want* (AMACOM, 1997), John Drake recomends that people enter every interview situation with the understanding that they are there to determine if the position is right for them. "Entering the interview with the awareness that both you and the interviewer are meeting so you can learn from each other can be very helpful."

To accomplish this, Drake says that a candidate should ask questions that help you determine if this is the job you want, make a positive impact on the interviewer, and provide insights into what you should highlight about your background and qualifications.

According to Alan Savage, staffing specialist for TriQuint Semiconductor, Beaverton, Ore., an engineer needs to find out as much information as possible about a company during the interview process. "The engineer is making a major decision." Hence, the engineer needs to make sure a company fits his or her employment needs. Asking appropriate questions is one way to accomplish this.

Roger Coker, staffing manager for Texas Instruments, Dallas, agrees. During the interview process, the interviewer's goal is to obtain as much information about a candidate as possible. But, Coker says it also is an opportunity for engineers to obtain as much information about a company as they need. "If they don't ask questions during the interview, the engineer may walk away without the answers they need."

Beyond compatibility, asking questions provides other benefits to the engineer. Savage says that it is important for an engineer to show they have a sincere interest in the company during an interview. He says that one important way to show that interest is by asking questions.

"Questions show that the candidate is interested in learning about the company," says Marti Wilmes, employment manager for Hewlett-Packard, Santa Rosa, Calif.

Questions also can be a tool for the engineer. Jeffrey Allen, in his book *The Complete Q&A Job Interview* (John Wiley and Sons, 1988), says that candidates can use questions to lead the interviewer into their strongest areas.

Savage agrees. He says that questions

TEN QUESTIONS TO ASK HUMAN RESOURCES PERSONNEL

1. What is the reason for the vacancy?
2. Were any internal candidates being considered or were considered; if so, why are you looking outside the organization?
3. Does the company promote from within? If so, is there a waiting period for applying for promotions and/or transfers?
4. Tell me about the organization's compensation program, i.e., performance reviews, compensation reviews, merit increases, etc.?
5. What type of educational or training programs are available for employees and what is the general philosophy toward individual development?
6. What is the salary range for this position?
7. Tell me about the organization's culture.
8. Tell me about the company's history and its future plans.
9. What is the turnover rate for the organization?
10. What is the turnover rate for the department that I would be working in?

Source: Humanex

can help the engineer strengthen technical competency with a company. For example, if an engineer has a strong background in computer-aided design (CAD), he or she can ask about the CAD tools used at that company. Once the company answers this question, the engineer can then state his or her proficiency with those tools. Thus, the engineer was able to inform the recruiter about his or her strengths by starting with a question.

The real trick to asking questions during an interview is directing the right questions to the right person. In today's interview process, the engineer will most likely meet with at least one member of human resources and one engineering manager. The information the human resources personnel can provide is somewhat different than the information an engineering manager can provide. Thus, questions an engineer should ask a human resources person and engineering manager are somewhat different. Human resources personnel knowledge is greatly different than that of the engineering manager.

Questions For HR

Nance Cohen, technical recruiter and owner of Cohen and Associates, Calabassas, Calif., says that when dealing with human resources people, engineers should ask questions about the work environment of a company--both physical and emotional. For example, some of these questions might include:

•How do employees handle stress in this company?

•Is this a company where every employee works 12 hour days?

•After work, does everybody go there own separate ways?

•Is the company supportive of an individual if he or she has a personal issue?

By asking these types of questions, she says that an engineer can get a sense of a company's work environment.

According to Andrea Foster, director of human resources for ANADIGICS, Inc., Warren, N.J., culture questions are very important. She says that these questions not only allow the engineer to get a feel for what is important to the company, but also allow the company to get a feel for what is important to the engineer.

Denise McCarney, recruiter for Philips Semiconductors, Sunnyvale, Calif., agrees. She says that the engineer should consider the following questions:

•Tell me about the culture at this company?

•Why would a person come work here?

•What is it in the culture that attracts engineers to come work for this company?

•What are some of the things in the company's culture that aren't so attractive?

•What kinds of people am I working with?

When talking about culture, a company's ethical standards also should be explored. To dig up this information, Coker feels that the engineer should ask:

TEN QUESTIONS TO ASK ENGINEERING MANAGERS

1. What do you consider to be the "ideal employee"?
2. What skills and experience does an individual need to possess to be successful in this position?
3. What is your management style?
4. What are the opportunities for advancement from this position and within this department?
5. How long have you been here? What has kept you here so long or what attracted you to this organization?
6. What would be the top five responsibilities of this position?
7. What are the major challenges of this position?
8. How will I be held accountable and by whom?
9. Will I be an "individual contributor" in this position, or work as part of a team?
10. What "bugs" you about the company? What needs to be worked out to make this a better place for everyone to work?

Source: Humanex

•Does the company have an ethics department?

• What efforts is the company making to promote diversity in the workplace?

Beyond culture, the engineer might consider asking the human resources person about company policies. For example, Coker says that the engineer should ask questions about how the company is making the workplace friendlier to the employee:

•Does the company offer elderly and/or child care?

•Does the company offer flex time?

•Does the company have policies and considerations for working mothers?

•What is the company's policy on maternity leave?

With health care costs continually on the rise, questions about company benefit plans also are critical. During the interview, engineers need to find out as much information as possible about 401K plans, medical plans, retirement plans, education benefits, and vacation leave.

"Engineers probably don't pay enough attention to benefits," Coker says. "Many plans look similar on the surface, but they are not."

Richard Daly, president of Humanex, Inc., Powell, Ohio, a human resources consulting company, says that the engineer needs to drill benefit questions. He says that engineers must make sure they understand 401K plans, education plans, and work family benefits before accepting any position.

One way to get a better understanding of benefit plans is by reading a company's policy and procedure book. In general, most engineering companies provide candidates with this information. But, if this type of book is not provided, Daly says that it is important for the engineer to ask for it.

Questions For Technical Management

Questions on the engineering side are a bit different. Technology and management style are the key focuses when interviewing with an engineering manager.

Daly says that when meeting with engineering management, the interviewee has to focus on the technology. To do this, he says the engineers should ask about new technology growth, systems they will be working on, what are the advancement and learning opportunities, and where is the engineering department going. "The engineer has to find out what the company is doing."

It also is equally as important to know where the company is going with technology. As a result, McCarney says that engineers need to think and ask questions that cover broader company issues. For example, she says that the engineer should inquire about the company's customers, the production stage of a product, the length of the project, future technologies, research and development budgets, as well as cutting-edge technologies.

The only problem with focusing on the broad picture, according to Wilmes, is that engineers sometimes forget the narrow picture—specific job description and responsibilities."Engineers need to know what their job is going to look like."

Savage agrees. "Sometimes a candidate makes assumptions which are greatly different than what the job is." As a result, he says that the engineer needs a tight description of the job they are interviewing for.

To draw specifics about a position, Cohen suggests asking:

•What will my duties and responsibilities be in this position?

•Who will I report to?

•What is the chain of command?

Ben Garfinkle, president of MetroVantage Personnel Services, Laguna Niguel, Calif., says the engineer also should consider asking:

•Am I going to be an individual contributor?

•Am I going to be a team leader?

•What is required of me?

•What do you see me contributing at this company?

Once the engineer has a strong understanding of specific job description and technology, questions should be asked about management style. According to Dave Hicks, senior technical recruiter for Micro Communications Executive Search, North Andover, Mass., 70% of a job is interaction with other people. As a result, he says that engineers must determine is they are going to enjoy working with the staff at a particular company. One important way to determine this is by questioning managers about their leadership approach.

But, addressing management style is not easy. As a result, Daly says that engineers should consider asking generic

TEN QUESTIONS TO ASK THE EXTERNAL RECRUITER

In today's recruiting environment, companies are using as many recruiting approaches as possible when hiring engineers. One approach is to employ a headhunter (or technical recruiter) to fill position openings. When dealing with these recruiters, engineers should be prepared to ask questions. Below are 10 questions the engineer should consider asking these recruiters.

1. Why has the company decided to use a search firm to fill this position?
2. Is this a retained search or a contingency search and why?
3. How many candidates have you presented and how many do you anticipate presenting?
4. Describe the profile you are trying to fill.
5. How long have you worked with this client and how many searches have you completed for them?
6. What does the company do well?
7. What does the company not do so well?
8. How would you describe the company's "people practices" (traditional, modern, etc.)?
9. Why do you like working with this company?
10. Who does the position report to?

Source: Humanex

questions to find out this information. For example:

•What kind of a manager are you?

•Can you tell me a little bit about your management style?

•Give me a behavioral instance when you were at your best as a manager?

Compensation

Arguably one of the trickiest areas to deal with during an interview is compensation. There is no doubt that salary is important to any person interviewing with a company. As a result, it is important that questions about compensation find their way into the interview process. The trick is asking these questions at the right time.

"There are very few jobs in which salary or compensation is not or primary concern," Drake says. "As an applicant, you need to know what the organization expects to pay you. This is not an item about which you need to decide whether or not to ask; it is more a matter of when to ask it."

Cohen says that discussions about compensation should never be brought up by the candidate. By bringing up compensation issues too early, she says that the engineer may portray to the company that money is all they are concerned about.

Hicks agrees. "Let the company make the first move." He says that placing too much emphasis on compensation can send the wrong message to the company.

Daly takes a different view. He says that if pay is important to an engineer, and if it has not been brought up during an interview, then the engineer should bring it up. But, he says that it has to be done carefully. "It is dangerous to be seen as a person who is in it for the money." To avoid this problem, he suggests asking question such as:

•What is the salary range on this position?

•Do people generally start above or below the midpoint of that range?

•Does this company do sign-on bonuses?

•Does the company offer its employees stock option plans?

Daly says that it is better to start with these broader questions before getting more focused on specific salaries, sign-on bonuses, or stock options.

McCarney has no problem with a person bringing up salary during an interview. "They should be open to talk about what's on their mind." And if this is a concern, she says that it is better to get the issue out in the open up front.

Coker agrees. But, he does suggest saving compensation issues to the end of an interview process. "I would pursue everything else first," Coker says. "If salary is not brought up to you first, then I would bring it up at the end of the interview."

When the issue of compensation does find its way into the interview process, there are some key points that the engineer must find out. Holly Faust, technical recruiter and co-owner of Hudson Consulting, Teaneck, N.J., says that once an engineer receives an offer, there are some fair and important questions he or she must ask.

•What is the incentive and bonus plan? What is it based on? Is it based on profit? Or is based on work performance?

•What is the minimum and maximum and maximum on a job title?

•When do I get performance reviews?

•When am I eligible to enroll in the company's 401K plan?

•When am I eligible for money for school?

•When do I get the sign-on bonus?

•What is the liability of my sign-on bonus?

•Does the company offer stock options?

QUESTIONS ENGINEERS NEED TO ASK THEMSELVES

"It takes a lot of time and money to bring in a person to interview," says Nance Cohen, technical recruiter and owner of Cohen and Associates, Calabassas, Calif. As a result, she says that the engineer must consider all the issues involved in making a career change before even walking into an interview.

"You have got to know what you are looking for and how you will accomplish those goals," says Holly Faust, technical recruiter and co-owner of Hudson Consulting, Teaneck, N.J. The main way an engineer can accomplish this, according to Faust, is by evaluating career goals and plans to fulfill those goals.

MetroVantage Personnel Systems, Laguna Niguel, Calif., has developed a questionnaire to help engineers make this evaluation. Below are the 11 questions the survey says engineers needs to ask themselves before changing jobs.

1. What are my feelings in regard to my current salary?
2. What are my feelings with respect to my current salary as compared to peers in my field?
3. What are my feelings toward my relationship with managers within the company?
4. What are my feelings toward my relationship with co-workers and peers within the company?
5. What are my feelings as to the potential for growth opportunities and promotions within my company?
6. What are my feelings in regards to the growth and expansion of my company within its industry?
7. What are my feelings with respect to being able to creatively apply my knowledge within my company? Are my contributions being recognized?
8. What are my feelings regarding my responsibilities and assigned projects?
9. What are my feelings as to the extent of my benefits and leisure time?
10. What are my feelings concerning the location and distance of my company from my home?
11. What are my feelings regarding the idea of remaining at my company for the next five years?

Need To Improve

As with many things, some engineers are better at asking questions and some are not. But, in general, McCarney says,"Engineers can do better."

A majority of the engineers, according to Coker, walk into an interview with TI, answer questions, and ask very few in response. "They should ask questions."

But, don't overdue it. Some engineers ask too many questions. Coker says that some engineers enter a company and ask a long list of questions. In turn, that may have the interviewer talking more than he or she would like. As a result, he says that the engineer needs to ask the right amount of questions to strike a balance during the interview

Daly agrees. "The human resources person is trying to have you talk 85% of the time," he says. "If the human resources staff member is talking for half the time, they will not like that."

Another problem to avoid is pressure. Some engineers feel that they have to ask questions. But, according to McCarney, they don't. "Engineers think if they don't ask a question its bad. It's not. Don't put yourself under that kind of pressure."

Ken Levine, employment manager for Tellabs Wireless Systems Division Burlington, Mass., has encountered similar situations. He says that it is OK to not have a question at the end of an interview. "Don't ask a question just to ask. Then you sound silly." However, he says that engineers should leave the door open so they can call the human resources person after the interview to ask questions. He says, that the engineer can say: "I'll probably have a million questions after I leave. Can I call you?"

The important thing to remember is that questions vary from person to person. Thus, the questions one engineer might ask may be greatly different than the questions another person may ask. Cohen says that every engineer has different things that are important to him or her. "Make sure you ask whatever is important to you."

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Job Hunting on the Internet: All Sorts of Opportunities Abound

THE INTERNET SPEEDS THE HIRING PROCESS BY ALLOWING ENGINEERS TO QUICKLY POST A RESUME AND ACCESS JOBS LISTINGS.

Eric L. Hausler

Type http://www.engineeringjobs.com into your web browser and you will arrive at the Engineering Jobs.Com web site, a career clearinghouse tailored especially for engineers. A click on the company employment pages and you are greeted with this message: "The companies listed here all have permanent hiring pages and most of them are always hiring." What follows is a seemingly endless list of links to the Engineering Openings pages at companies around the globe. Searching for a job on the World Wide Web can be that easy.

The Internet is revolutionizing the way that employers and job candidates find each other. Today's headhunter is a search engine that accepts keywords and returns an armload of job opportunities. According to John Sumser, editor of Electronic Recruiting News, an on–line newsletter:

http://www.interbiznet.com

"There are over 3,500 employment related web sites, listing over 1 million jobs around the net." Job hunting on the World Wide Web is becoming a valuable tool for employment seekers—"over 40% of all new users cite finding a job as a primary reason for getting on the Internet, while at least 95% of all college job searches include the Internet at some level," says Sumser.

As search engines become more sophisticated, employers are able to find job candidates that meet their qualifications using keywords or phrases that search through mountains of online resumes. Until recently, the Internet has been most often used by high-tech people to find jobs with other high-tech companies. However, Sumser sees a good future for all job hunters on the Web, both technical and non-technical. He points to the increase in non-technical employment opportunities listed at sites such as AT&T and J.P. Morgan as a positive sign that the Internet is becoming the place to find jobs.

Sumser cites a number of factors as contributing to the increased role of the Internet in today's employment market. "We will be facing white-collar labor shortages shortly. Demographic shifts, plus decreased loyalty, plus increased projectization, will equal shorter tenure jobs for at least a generation. The Web has emerged just in time to resolve this economic transition."

Low-Cost Search

The average job seeker can post his or her resume on one of the Internet's many recruiting sites for only a few dollars per month, if that. It is a passive way to monitor and apply for better opportunities, stay abreast of the job market, and still remain safe in a current job.

Employers also are citing other reasons why the Internet works. They are using the Internet to go right to the market with their needs. This translates to money saved on hiring costs, and streamlines the search process.

Companies can find candidates that match their needs profiles right away, instead of having to weed through an endless sea of resumes. Many companies, including Compaq Computer, Microsoft, IBM, and Texas Instruments, scan the resumes they receive into a huge database which can be searched by key word or phrase.

Bill Looney, vice-president of Photon-Technology International Inc., a New Jersey manufacturer of proprietary electro-optical instruments, recently advertised a position for a Senior Electronics Engineer on The Monster Board:

http://www.monster.com.

The Monster Board is a massive career site on the Web that offers the gamut of employment-related services. It currently has more than 50,000 job postings. Visitors to the site can upload or build a resume, find employer profiles, search job listings by state, industry, company, discipline or a keyword, or tap into the Monster Board's vast career-support databases.

"The whole process is more flexible on both sides," says Looney, explaining why his company has opted to post job openings on the Monster Board."It allows us to find a person who more closely meets our needs. With the newspaper we get too diverse a population of returns. Here we can target specific areas for expansion, and weed out candidates that don't meet our credentials."

So far, Photon Technology has received high-quality responses from their Monster Board listings. He attributes this to the fact that the company is allowed to post much more detail about the job, the company, and the qualifications they seek in a candidate than in the traditional classified ad.

IEEE Offers Help

One of the best places to begin a job hunt on the Web is the employment assistance pages of the IEEE-USA:

http://www.ieee.org/jobs.html.

The IEEE has a national job listing service available to its members that are posted on nine autoresponse files. The job listings are broken down by eight regions within the United States, and one outside the United States. To gain access to the service, job seekers send e-mail to the designated Internet addresses, and the requested files will be sent within a few minutes. The listings are updated weekly, and remain posted for 30 days.

The employment assistance pages also provide links to other employment resources and resume databases, an entry-level assistance page, employment assistance help files, and a regularly updated schedule of technical job fairs around the United States. Also listed are numerous publications, videos, and guides that will help members identify various skills and talents, develop a job market, write resumes, improve interviewing techniques, and survive changing job markets.

IEEE-USA also has an agreement with Resume-Link:

http://www.resume-link.com

or call Resume-Link at (614) 529-0429). Members can submit their resumes along with an information form that will be placed onto a national database that will be used by employers to fill job openings.

Optimizing your search

Here are some helpful hints to optimize your search:

•Keep track of the sites you visit by bookmarking them.

•Start out your search on a particular site at the Help desk or What's New area to learn about their services.

•Find out what keywords or phrases are the industry buzzwords employers are looking for and include them on your resume.

•As always, an error-free and easy to read resume is essential.

•Keep written notes of the resumes you e-mail or fax including dates and addresses, so you can track how your job hunt is going.

•Stay up-to-date on interviewing and hiring practices in your industry by using resources available on the Internet. These career support resources used to cost hundreds of dollars; now they are mostly free.

•Set up personal search engines on sites such as Career Builder and the Monster Board. They will notify you of new openings in your field.

Searching Out The Sites

There are over 3500 employment-related sites on the World Wide Web with more going on-line everyday. Here are a few of the most popular sites today to start you out in your search.

•***IEEE USA:***

http://www.ieee.orgs.jobs.html

The IEEE's employment assistance site has links to a National Job Listing Service, Resume Referral Services, a special entry-level assistance page, employment assistance help pages, job fair listings, and other types of Internet career resources.

•***Engineering Jobs .Com:***
http://www.engineeringjobs.com/

This site is a mecca for engineering career information. The site has resume linking, job database searches, links to other engineering-related sites, information on professional societies, and reference help for engineers.

•***The Monster Board:***
http://www.monster.com

This particular site is aptly named because it has over 50,000 job listings. It will track and find your own personal job listings by region, state, or keyword. It allows you to build a resume and cover letter on-line, will notify you of new listings in your field, and offers a wealth of career support help. No fee for use.

•***Job Banks USA:***
http://jobbankusa.com/

Job Banks USA provides employment and resume information to employers, candidates and recruiters.

•***CareerBuilder:***
http://www.careerbuilder.com

This site has listings and links, but also allows you to format a personal search engine that will notify you of new listings by e-mail.

•***E-Span Career Connection:***
http://www.espan.com/

E-Span is an all-around career site. It has job listings and career support services that contain a wealth of information. This information includes travel and relocation help, local city news abstracts, business indexes, site links, and an on–line human resources center.

•***Jobtrak:***
http://www.jobtrak.com

Jobtrak is a good career resource for students and recent college/university graduates. Employers have teamed up with college/university career centers to target graduates or students from specific schools. Students and alumni must contact their university or college career center for a password to access employment opportunities on Jobtrak.

•***Yahoo- Employment:***
http://www.yahoo.com/Business/Corporations/Employment_Services

Yahoo is a giant search engine that combs the Web for information. This is their employment services link. It is a good starting point for a more general search of the Web for employment opportunities.

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- C/C++
- CDMA/wireless communications a plus

Sr. Software Engineers
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- Mac, Windows NT & UNIX preferred

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- MSEE preferred

Sr. Communication Systems Engineer
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Successful Candidates Need More Than Just Technical Skills

RECRUITERS SAY THAT PASSION, AS WELL AS EXPERTISE, IS THE STUFF GOOD ENGINEERING TEAMS ARE MADE OF.

Linda L. Hudson

In the defense industry, an engineer's most valuable resume item is a solid security clearance. Engineers cleared to the very highest levels—particularly those with skills in critical areas—"are worth their weight in platinum," says Greg Likins, a college recruiter with the TRW Data Technologies Division, Redondo Beach, Calif. Likins' division is the software development arm of TRW's Space and Defense Group.

As far as recent college graduates, his division looks primarily for computer science backgrounds. But since clearances are so tough to get, TRW and other defense contractors have had to "open up the filter" and look for candidates who majored in a hard science or other engineering disciplines and also are interested in software.

"We find it's easier to train someone to do software than to train them to do science," Likins says." We want people who are rigorous in their standards."

He says that scientific creativity also is a very positive attribute in the defense industry, where people are needed to develop huge, complex systems." How you handle yourself in uncertain situations" is very important in his industry, he notes, where the norm is to develop one-of-a-kind software and hardware. "We're looking for people who enjoy being creative in a scientific way."

Likins says one important attribute is a commitment to reliability rather than time-to-market." Our reliability standards would probably be the kiss of death for consumer electronics."

In San Diego's "Wireless Valley," cellular and wireless systems manufacturers compete side-by-side for engineering talent that will give them a competitive edge. Engineers are in great demand nonetheless, especially in radio frequency (RF) specialties. But candidates must survive rigorous screening and interviewing processes designed to pinpoint the optimum mix of technical skills and behavioral attributes.

Phil Goodrich, Human Resources manager at Nokia Mobile Phones' Research and Development Center, says they are "now looking for very experienced people." Not only is Nokia looking for people with industry experience, but engineers "who actually have handset experience." Occasionally, the company will hire infrastructure engineers, then train them on the handset.

Entry Level Engineers Turn To RF IC

Goodrich says "entry level" candidates with a BSEE and at least two years industry experience are most often hired into the RF or RF integrated circuit (RF IC) areas. Within the RF area, engineers will be trained as systems, synthesizer, or transmitter designers. RFIC engineers generally are promoted to positions of greater responsibility within that area.

Candidates fresh out of school need a masters or doctoral degree with "specific hands-on experience" to be considered. Internships or cooperative study programs between companies and universities are considered useful experience. Goodrich emphasizes that only candidates with post-graduate degrees are considered. "With a bachelor's degree and no industry experience, candidates don't bring enough to the table," Goodrich says.

Nokia's human resources recruiters are responsible for screening candidates, and will use a 10-to-20-question worksheet to conduct preliminary telephone interviews. If a candidate makes it to the next step, results from the worksheet are used to prepare a technical team of eight to 10 people for an all-day, on-site interview. First, a candidate delivers a one- to two-hour presentation on his or her

GRAPHICS CHECKLIST

GENERAL REQUIREMENTS

Experience
- 2 years minimum

Technical Skills
- Specific to position

Behavioral Skills
- Team orientation
- Risk-taking
- Tolerance for ambiguity
- Written and oral communication
- Creativity
- Managerial/busines talent
- Coping
- Passion for their work

SPECIAL REQUIREMENTS

Defense
- Security clearance
- Commitment to reliability vs. time-to-market

College Hires
- BS--some
- MS/PhD--Yes, with hands-on experience

skills. Then, the team breaks up for a series of two-on-one sessions on specific technical areas. Finally, the human resources recruiter conducts a "behavioral" interivew.

Behavioral interviews are common throughout industry. These interviews seek to find out about people's motivations and work values, whether an individual feels more comfortable as a team leader, team player, or as one who works alone. Whether candidates fit in a particular corporate "culture" also is important.

Goodrich admits that the schedule is grueling, but necessary."One engineer with 13 years in the industry said it's incredible how things have changed since he interviewed."

Most companies break down their technical needs into major focus areas and grade the behavioral skills expected by the level of experience—that is, whether the candidate engineer is just out of college or graduate school or has worked some years in industry.

Skills For Specific Technical Areas

Intel, Santa Clara, Calif., has six main technical focus areas, according to Technical College Recruiting Programs Manager Craig Walker. These are IC engineering, IC manufacturing, facilities, hardware engineering, hardware manufacturing, software engineering, and information technology. Within each of those categories are subcategories, each with its own required set of specific skills.

For example, within IC engineering, the category of very large-scale integrated (VLSI) circuit design requires specific knowledge of how to design microchips and logic and Complementary-Metal-Oxide-Semiconductor (CMOS) circuitry. In hardware engineering, systems integration engineers are very important. Intel, of course, not only makes chips, but also hardware systems such as servers and personal computer (PC) motherboards.

"For people outside of Intel, one of our least understood areas is software engineering," adds Walker. "People think of Intel as hardware or ICs. Often they don't understand our need for a broad range of job assignments." These range from software development to quality assurance and design automation. Specific skill sets reflect the variety of Intel's interests: C++, UNIX, assembly language, compilers, local-area networking, Integrated Services Digital Network (ISDN), graphical user interfaces (GUIs), and multimedia.

Candidates for positions at Intel go through three or four technical interviews and one behavioral, "debriefing" interview by the HR recruiter. Generally, interviews are conducted one-on-one.

"We encourage technical people to use behavioral interview techniques," Walker says."Rather than ask closed-end questions, we like to ask candidates about their experience and let them discuss it. For example, we may ask for detail about how they've solved problems." This way, he says, they often can determine the quality of a candidate's problem-solving skills.

> Behavioral interviews help companies find out more about an engineer's motivations, work values, and fit within a company.

The level of experience Intel requires is based on specific needs, "although most openings look for three to five years' experience," according to Walker. "But our need is so tremendous that we will look at all levels of experience." However, he adds, "we expect a very high level of technical experience for all college recruits and experienced engineers."

The key behavioral attributes Intel looks for are tied to an engineer's experience.

For example, says Walker, a college hire should demonstrate problem-solving and communications skills and the ability to work in a team environment.

"About 80% of what we do is in a team environment, although there are needs for individual talent as well," Walker says.

More experienced engineers need to demonstrate a greater number of behavioral skills, "with the precise combination of attributes dependent on specific job requirements," Walker says.This skill set includes tolerance for ambiguity, commitment to task, managerial skills, coping, decisiveness, spoken and written communication, assertiveness, creativity, and team-building.

The behavioral interview also is used to determine whether a candidate will fit in comfortably with Intel's corporate culture."We look for balance," Walker says. For example, he says, a college candidate with a 4.0 grade point average would need to have worked in industry or have cooperative work-study experience--or even to have played a team sport--to demonstrate the balance sought in Intel's team-oriented environment.

Business Backgrounds Are Useful

At Lucent Technologies in Murray Hill, N.J., the optimum combination for recent college graduates would be some technical and some business background. Even if the focus of a position is chiefly technical, says Madelyn Buckley, University Relations and College Recruiting manager, "some forward thinking and leadership tools" to go along with technical skills are extremely desirable. She says the best candidates have a ratio of technical to management skills of about 70/30.

She points out that a standard screening interview conducted by her department for a recent college graduate would include a skills inventory to gauge management potential along with several technical questions.

An interview with someone with an advanced degree and perhaps four years experience would combine technical questions and management issues focused on behavioral attributes such as problem resolution, teamwork, and network building. High-scoring candidates might then be screened into a pool of employees with leadership potential and be put on a fast track to a leadership posi-

tion.

Technical interviews are carried out by managers from business operating units.

Buckley says Lucent's goal is to be competitive in hiring top talent. To do that, she says, the company works very hard to achieve a "balance between high tech and high touch." In other words, Lucent tries to reach candidates quickly. For college hires, for example, the company attempts to identify and contact candidates in their junior rather than their senior years.

Looking For Passion

The Sony Technology Center in San Diego, Calif., has some 400 engineers working in 17 different business units, so required skill sets can vary greatly. Although half of all engineers are hired directly from four-year universities, all successful candidates must have "some relevant work experience," according to Employment Supervisor Whitney Godeke.

For college hires an internship or "co-op" work-study experience on the resume "is a must," she says, along with a degree in electrical engineering, mechanical engineering, or computer science, and a grade point average of 3.0 or better.

College hires usually are first interviewed on their campuses before being asked to the Sony facility. In San Diego, they are interviewed by the hiring manager, team members, and a person designated as a mentor.

This panel interview is critical--not just to determine technical expertise, but to find out key behavioral attributes. Do they seem like long-term prospects, or will they be bored in six months? Do they demonstrate initiative? Can they learn quickly or do they need lots of handholding?

Candidates with industry experience must first pass a telephone screening interview conducted by a recruiter on the HR staff. The recruiter verifies information on the resume. An RF engineering candidate, for example, would be asked to define code division multiple access (CDMA) and ISDN.

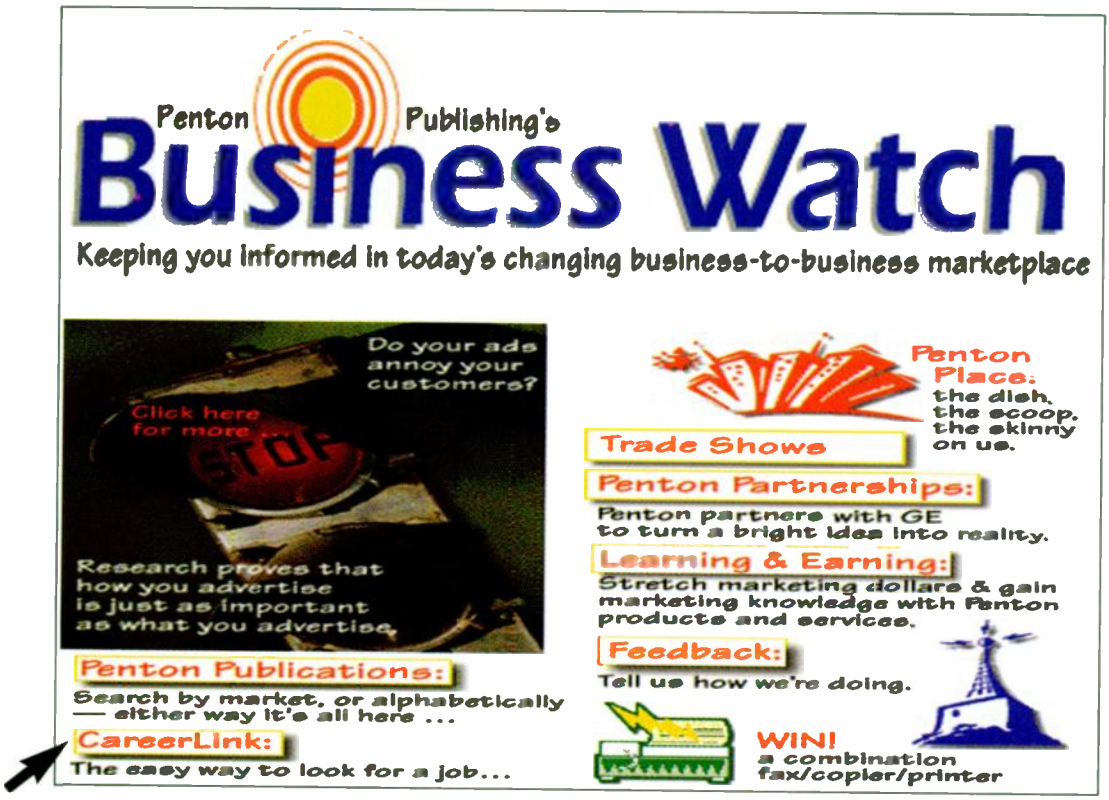
Godeke says that since most higher-level engineering candidates are from outside San Diego, it is important to identify the truly strong candidates before flying them in for on-site interviews.

Once there, the candidate is questioned by a panel comprised of the department manager and several technical team members. Godeke says "panel interviewing" is a common characteristic of Japanese companies like Sony. Panel members ask "in-depth questions about projects, the types of technical processes used, and so on, to find out if the candidate's skills are directly transferable."

Directly-related industry experience is important, but so is "a passion for what they do," Godeke adds. The San Diego Technology Center develops consumer electronic products from televisions to wireless and cellular telephones. Godeke says Sony wants people who want to design the latest HDTV, who want to be able to walk into a store and say, "I designed that."

"To be really innovative, you have to have that passion."

Linda L. Hudson is a freelance writer and editor. She may be contacted at 733A Loma Verde Ave., Palo Alto, CA 94303; (415) 424-9828; fax (415) 424-1440.



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Stress Kills: You're Not An Effective Employee If You're Dead

WORKING SMARTER, NOT HARDER, IS THE MORE EFFECTIVE ROUTE TO SUCCESS.

Paul McGoldrick

This column is being devoted to the "Winning Formula" for engineers. Not a trivial topic, and one that is going to be spilt into some number of issues of this supplement. We will try to cover the topics of training/education, organization, hours worked, project control, discipline, and even try to gain an understanding of the office politics that, of course, do not exist in anybody's organization!

But while pondering this whole area, it was realized that the most important ingredient in an engineer's career success is survival; and a considerable element of modern survival can be tightly linked to reducing stress. We all know people who thrive on stress, who seem to find that doing everything at the last minute at full throttle gives them the adrenaline to work at what they feel is their best. It's probably arguable. Most of those persons that leave things to the last minute are, in fact, procrastinators, so that the average stress level over the life of the project is probably not that high.

That is not the case in situations, particularly for lead engineers and managers, where there are multiple paths happening and coming towards fruition at about the same time as one another. There, the stress can be a continual weight and not learning to handle it can result in failure in the workplace, often quite dramatically, and personal failure. If it is handled well, stress can be positive, healthy, challenging, and stimulating, eventually resulting in a creative charging of energy that can lead to peak performance.

ARE YOU STRESSED?

Is your sleep regularly interrupted?	N	S	O
Do you get irritable?	N	S	O
Do you notice your concentration slipping?	N	S	O
Do you have frequent indigestion?	N	S	O
Do you suffer headaches?	N	S	O
Do you have trouble deciding things?	N	S	O
Are you drinking excessively?	N	S	O
Are you smoking excessively?	N	S	O
Is it difficult to relax?	N	S	O
Are you unsure of your abilities?	N	S	O
Do you get breathless quite suddenly?	N	S	O

If you scored three or more "oftens" (O) you need to think about the way you are living/working. If you scored more than five "Oftens" you could be a heart attack waiting to happen.

Five or more "sometimes" (S) and you probably need to change things before they overwhelm you.

Five or more "nevers" (N) show that you are coping really well.

The numbers produced both in North America and Europe suggest that since the 1950s, stress among managers has grown by about 500%, with 50% of senior engineers complaining of work overload with longer hours and less support, and the majority recognizing in themselves the symptoms of stress in irritability, sleep disorders and tiredness. And unlike yesteryear, many of the traditional ways of reducing stress have become unavailable: The extended family tends not to be there; our neighbors are probably strangers, we don't know our doctor—if we even have one through our medical plans—and religious support is not something most publicly seek.

We also are an incredibly mobile society, and our symptoms of stress are as likely to be showing up in a conference room 5000 miles away as in the checkout line of the local supermarket. You can understand, although not support, the action of a pop group that was touring the U.S. a few years ago. After visiting about 30 cities they were so stressed out that one night they completely trashed a hotel room. The release of tension was obviously something they should have gotten out of their systems on the golf driving range or swimming, or in some other physical exercise; but they didn't. The story was that the road-show manager gave the hotel twice the estimated damages with the comment, "Have one on us." It was not reported whether the hotel manager was sufficiently stressed out himself to take advantage of the gift.

Relax And Laugh

The absolute center of reducing stress is relaxation; Some people can escape the day just by laying down for 15 minutes at the end of the work period repeating positive thoughts to themselves, thinking of their breathing, and just plain unwinding. Twenty and thirty years ago, people would stop off at the nearest lounge and relax over a drink; the medical profession frowns on that, of course, insisting that going to a juice bar with your peers probably can help you un-

wind. Others among us have no colleagues around at the end of the working day, so we have to come out of the work coma in different ways.

An engineer in a west coast semiconductor manufacturing company owns two cougars—quite legally—and they serve to relax him. Just as it is politically incorrect to drink alcohol in the 1990s to relax, it is equally unacceptable to barrel about the highways in your vehicle to get it all "out" of your system; but the gym, aerobics, golf driving, volleyball, etc. are all acceptable and, according to the experts, good for that winding down; but, of course, if some of your stress is due to people in your office environment, you probably shouldn't relax with them.

Some of us can wind down with a walk on the beach, but that is difficult to do when you finish an article at 2 in the morning. But always, for nearly everybody, tension can be released with laughter. If you can laugh at it, you can live with it. Laughter allows you to look at things differently, it encourages positive thoughts about things, it makes you want to take action, and it restores our faith. The presence of a related Dilbert cartoon on the wall of a cubicle in Silicon Valley can be an unsaid, or a muted, laugh at a situation without having to state it to the world.

Most experts agree that reducing your dependency on seriousness is a necessary first step to making your problems look like problems instead of mountains. It also is essential for the engineer to be healthy and well-nourished: mentally, spiritually, physically, and emotionally. When you think of some engineers' work habits (in startups, in particular), you can see a lot of factors that aren't in the nourishment cycle where they need to be. Whether anybody can be well-nourished in all areas at the same time is questionable, but we should set things up so that we can be as close as possible.

But healthy eating has to be accompanied by physical and mental relaxation, exercise, and some form of enrichment which should be spiritual, but has no need to involve anything religious. Exercise is particularly important because the actual process distracts from work-related problems and there is a natural tranquilization caused by the release of endorphins—mood-elevating chemicals released by the brain—a much more natural booster than caffeine or chocolate or nicotine or depressants like alcohol. And there is certainly nothing wrong with being physically more healthy at the same time.

Naturally Stress-Free

It is annoying to some that a certain percentage of the population are so totally laid-back and naturally relaxed. Their personalities are enviable for most of us, most of the time. There are, however, times when a good explosion seems like the right way to go: An indicator to others that something or another is really important to you. But even if you are not a member of the naturally-relaxed club there are changes that we can force on ourselves to change our lifetime habits; the more difficult it is for us to change those habits is probably a good indicator of the degree to which they needed to be changed.

Having seen many engineers go through the stress cycles, and then finding ways out of them, it is indeed a marvel to watch a human who believed that his headaches would never go, that indigestion was a permanent thing in life, that he would never again be able to sleep properly again, that concentrating longer than his kids would be impossible, that the fatigue and loss of self confidence are telltale signs of aging, and trying to find the right set of solutions for himself.

It is not infrequent to be asked to call someone during the weekend to finalize a project or to talk about progress, or whatever. My theory is that if I were happy to be called during my time off, I should be happy to call other people: But I am not. If you decide that the weekend is a non-work time, then don't; if you need your own space, your own music, your own bath oils to promote your relaxation, then make sure that those

around you understand that and do not intrude.

For many, the rigors of the commute are as stressful as the working day. Some of the biggest decisions we ever make are about where we live, but few people truly consider the effects of the commute on their lifestyle; they will justify it, they will excuse it, they will declare how it will improve: but it never does. In the Bay Area, we have seen commute times increase by 500% in the last two years; reverse commutes are disappearing; freeways that were empty are now parking lots because of dormitory housing.

If the act of changing residence is scary, look for other ways to reduce the commute load: Is there a mass transit solution or part-solution? Can you telecommute? Do you feel comfortable/are you allowed to work a flex-schedule (both days and times)? If there is no relief in these ways, think again, seriously, about moving or changing jobs or both. You are no good to anyone in a fully-stressed state.

Your Own Space

Putting your personal stamp on your work space is an important, and rarely considered, need. Photos you can share, posters, fun stuff; show your sense of humor to everybody else and you will share in it yourself. And get yourself organized. When you get a piece of paper in your hand deal with it, don't "file" it for tomorrow; if you get an e-mail, answer it; if you can answer the phone then do, don't build up the voice mails.

If there is something that you need to do regularly, then set that time aside to do that task. Whatever those tasks are, don't ignore them; if you can learn to perform such activities like a mini-vacation, it can even become a pleasant interlude.

Above all, keep your cool. You may have a boss who likes to vent his spleen on a daily basis at meetings: Don't let it get at you. If it does, change jobs.

Paul McGoldrick is analog editor at Electronic Design. *He has been in senior management positions at a number of companies, as well as being the lowly, picked-upon engineer at a bench. He can be contacted at* ED*'s San Jose office at (408) 441-0550, ext. 113, or by e-mail at 102447.346@compuserve.com.*

Company Profiles

Northrup Grumman Corp. Electronic Systems Division

Headquartered in Rolling Meadows, Il., Northrup Grumman Corp's Electronic Systems Division develops RF and infrared countermeasure systems for the U.S. and international defense electronics markets. This company offers engineers a chance to work with leading-edge technology for advanced electronics systems design and development.

Winner of the R&D 100 Award, Northrup Grumman's Electronic Systems Division is known for its advanced RF internal countermeter system. It also is leading the development of an advanced infrared countermeter system.

Northrup Grumman Electronic Systems Division employs approximately 2500 employees, including 1400 engineers. In the next year, the Electronic Systems Division plans to add 300 engineers to its software, systems, electro-optical, and radar divisions.

Company headquarters is located at:
600 Hicks Road
Rolling Meadows, Il. 60008

Wiltron Company

Headquartered in Morgan Hill, Calif., Wiltron Company has been a pioneer in the design and manufacture of advanced microwave and telecommunications products. The company's products perform access, test, and performance monitoring on more than 2 million circuits used by 35 telecommunications companies in 10 countries around the world.

Wiltron is a part of the Anritsu Corp. family of Japan. The company has approximately 600 employees currently on staff.

Company headquarters is located at:
490 Jarvis Drive
Morgan Hill, Calif. 95037

Hewlett-Packard Co. Components Group Communications Semiconductor Solutions Division

Hewlett-Packard Co. Components Group's Communications Semiconductor Solutions Division is a leader in developing RF semiconductors targeting the wireless revolution. This division is growing its product line of silicon and GaAs RF semiconductors in industry-leading small packages. Over the past year, Communications Semiconductor Solutions Division has developed PIN diodes for cordless, cellular, and paging systems; an amplifier and mixer in SC-70 packages; high-performance GaAs PHEMT in new packages for low-cost DBS and TV receive-only applications; a tiny modulator/mixer for digital wireless applications; and highly integrated chip sets for cordless, data, and unlicensed PCS systems.

Founded in 1961, Hewlett-Packard'sComponents Group is a worldwide organization which employs over 11,000 people in manufacturing, assembly, and sales. The Components Group's Communications Semiconductor Solutions Division has openings for engineers in its marketing, applications, design, and test departments.

Company headquarters is located at:
350-370 West Trimble Road
San Jose, Calif. 95131-1096

Company Profiles

INTEL CORP.

Intel Corp is a leading chip developer and product manufacturer for personal computers, networking, and communications systems. Some of the company's leading products include next-generation microprocessors and software for the Internet.

Intel has offices in eight U.S. markets: Phoenix, Ariz.; Albuquerque, N.M.; Santa Clara, Calif.; Sacramento, Calif.; Portland, Ore.; Seattle-Tacoma, Wash.; Salt Lake City, Utah; and Fort Worth, Texas (where the company's newest manufacturing site is being built). It has positions open in IC engineering, IC manufacturing, hardware systems, information technology, and software engineering. Resumes can be sent to the company through the Internet at http://www.intel.com.

Company headquarters is located at:
P.O. Box 1411
Folsom, Calif. 95763

DENSO Wireless Communications

DENSO Wireless Communications is a leading developer of CDMA-based cellular phones and private wireless systems for the international market. Currently, the company is positioned to develop and introduce digital CDMA phones, PCS phones, PHS phones, and PHS base stations for the wireless market.

DENSO Wireless Communications is backed by the DENSO Corp., an international company that has worked over 50 years in the electronics industry and has annual sales topping $13 billion. Over 64,000 employees in 22 countries contribute to the 340 product lines manufactured by the DENSO Corp.

Located in Carlsbad, Calif., DENSO Wireless Communications has ongoing openings for technical professionals. The company seeks software engineers, RF engineers, digital hardware designers, communications engineers, and mechanical engineers. For more information, visit the company's website at http://www.densolabs.com. Responses can be e-mailed to the company at jobs@densolabs.com.

Company headquarters is located at:
2131 Palomar Airport Road
Carlsbad, Calif. 92009

Rockwell Semiconductor Systems

Rockwell Semiconductor Systems is a worldwide developer of modems and wireless communications devices. In 1996, the company's cordless phones, employing 900-MHz direct-sequence-spread-spectrum (DSSS) technology, reached volume production. These phones offer greater range, superior voice quality, and higher security. Focusing on next-generation technology, Rockwell also has announced that 56-kbits/s download rates are possible for the modem market. Employing 54,000 people, Rockwell Semiconductor Systems is seeking to hire over 300 engineers in the next year, Opportunities are available for RF engineers, wireless system designers, marketing personnel, DSP engineers, mixed-signal engineers, and software systems designers.

Company headquarters is located at:
4311 Jamboree Road
Newport Beach, Calif. 92660-3095

Raltron Manufactures and Supplies One of the Widest Lines of High Technology and high Quality Crystal Units, Oscillators and Filters to Electronic Original Equipment Manufacturers Around the Globe. Our Manufacturing and Engineering Facility Located in Miami, Florida has the Following Positions Available:

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■ Inside Sales and Regional Sales:

Requires 3-5 Years Experience with Electronic Sales.

■ Production Manager:

Requires 5-8 Years Crystal Oscillator Experience relating to manufacturing.

Fax Resume To: 305-594-3974 or Mail Resume to RALTRON ELECTRONICS, HR Dept., 2315 NW 107th Ave., Miami, Florida 33172. See our home page at www.raltron.com

SSE

SSE, a leading manufacturer of satellite earth station components and systems for the worldwide satellite communications market has the following career opportunities:

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Systems Engineer
Systems Engineering Mgr.

In Scottsdale, Ariz.:
Modem Design Engineer
Embedded Software Engineer

In Vienna, VA.:
Federal Sales Mgr.

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Company Profiles

ANADIGICS, INC.

ANADIGICS, Inc. is leading supplier of gallium-arsenide (GaAs)ICs. These ICs are used in cable television, fiber optics, wireless communications, Direct Broadcast Satellite, and ETACS systems. ANADIGICS is the highest volume GaAs IC manufacturer. It is known for developing the first single-chip GaAs power amplifier for commercial cellular telephones and the first single-chip Direct Boradcast Satellite dowconverter.

Founded in 1985, ANADIGICS has approximately 400 employees, which includes about 100 engineers. At ANADIGICS, an engineer will find constant innovation using GaAs technology in low cost, high volume consumer electronics applications.

Company headquarters is located at:
35 Technology Drive
Warren, N.J. 07059

ANADIGICS®

Inspired by the challenges of change, we're creating the technologies for the future.

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If a front row, cutting edge opportunity appeals to you, there's no better place to be than ANADIGICS, Inc., a world leader in the design and manufacture of high frequency GaAs ICs for consumer electronics, satellite systems, cellular telephones, cable TV, and local area networks.

SENIOR DESIGN ENGINEERS

Independently designs and develops new IC products to volume production. Duties include electrical, mechanical layout packaging and assembly design. Products include Fiber Optic MMICs, linear MMIC amplifiers, clock recovery ICs, etc.

BSEE and at least 5 years of directly related experience with GaAs or RF MMIC design required. Must have broad background with characterization and applications of ICs for RF and Microwave, as well as experience with GaAs MMIC design, fiber optic systems/components and clock recovery circuit design(PLL). Will need to work independently and with minimal supervision, train engineers and technicians and have knowledge of personal computers for design and test applications. Having supervised small design engineer team is a plus. Some travel required. ***JOB #96-178/COEE***

SENIOR DESIGN ENGINEERS

Independently designs and develops new RF IC products to volume production. Duties include electrical, mechanical layout, packaging and assembly design. Characterizes, models and analyzes devices such as FETs, diodes and passive components. Designs and purchases test fixtures and setups. Provides customer support on technical matters.

BSEE required, MSEE or higher a plus. Must have 5 years of directly related experience and broad background in characterization and applications of ICs for RF and Microwave. Will need to work independently with minimal supervision and train other engineers/technicians. ***JOB #96-280/COEE***

APPLICATIONS ENGINEER

Characterizes devices for data sheets while providing a variety of customer information, including technical advice via telephone/ fax and traveling to customer sites to perform problem resolution as needed.

BSEE or equivalent required along with at least 3 years of RF microwave design experience and thorough knowledge of RF test equipment/measures. Strategic thinking and customer communication skills essential; knowledge of receiver and power amplifier design issues desired. ***JOB #97-75/COEE***

DESIGN ENGINEER, Advanced GaAs Design

Responsibilities involve RF IC circuit design, including power amplifiers, receivers and bias stabilization; simulation layout and engineering evaluation and device characterization.

BSEE and 2-3 years of experience with RF IC design required. ***JOB #96-265/COEE***

DEVICE ENGINEER

Electrically characterizes new devices and circuits. Supervises layout, manufacture, and assembly of new devices and develops test program for new devices. Evaluates new equipment for processing/device development and testing. Supports the improved M gauge resistivity program used in manufacturing. Conducts technology development for advanced passive components.

BS in Electrical Engineering, Physics or equivalent and at least 5 years of experience assembling and manufacturing power devices required. Must have design experience in power devices, specifically GaAs FETS. Background in device physics, processing, modeling and thermal design essential. ***JOB #95-72/COEE***

SENIOR ASSEMBLY/ PACKAGING ENGINEER

Responsible for new process development, continuing process improvement/cost reduction; troubleshooting, defining production control monitor systems; performing audit to process specification: writing process specifications; setting up new equipment and assisting in transfer of new products from Engineering to Production.

Must have electronic packaging experience; die attach, wire bonding, encapsulation, plastic molding, cleaning, epoxy adhesive and assembly, marking systems and molding compounds. ***JOB #96-17/COEE***

TEST ENGINEERS

Designs, builds and maintains RF/Microwave Rack and Stack Test Systems; writes, compiles, debugs and documents production test and probe programs; generates schematics, drawings and equipment specifications as needed and provides guidance for test technician on system troubleshooting and repairs.

Must have RF/Microwave knowledge and 3+ years of experience. Exposure to PC/Automated testing required. Knowledge of Visual Basic/Basic Programming and RF/Microwave test equipment essential. ***JOB #96-146/COEE***

PACKAGING ENGINEER

Designs and develops surface mount packages.

BS/MS in Mechanical Engineering or Materials Science and at least 2 years of experience in electronic packaging or equivalent required. Will need background in thermal characterization, analytical skills and qualification of materials. ***JOB #96-144/COEE***

PRODUCT ENGINEERS

Monitors yield, analyses, summarizes and provides corrective action for electrical or visual failures. Designs experiments, Fab through life test, to improve processes for higher yield products; determines lot/wafer dispositioning; verifies quality final test and calibration.

BSEE required. Must have at least 5 years of experience or similar technical background. Will also need basic knowledge of semiconductor fabrication, testing and packaging. ***JOB #96-198/COEE***

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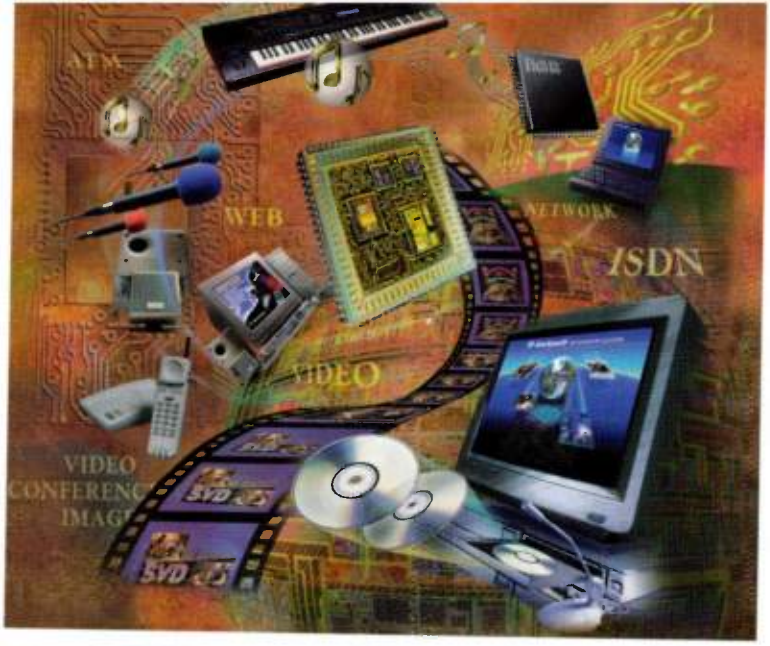

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Rockwell Semiconductor Systems not only designs and manufactures leading edge semiconductor components - we create the complete semiconductor systems solutions OEMs demand to beat the competition in getting personal communications products to market.

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Our semiconductor systems solutions already power most of today's fax and data modem products. We're committed to becoming the global leader in semiconductor solutions for all personal communications electronics products, and we have the financial firepower to make it happen.

You want to create the future?

Rockwell Semiconductor Systems will continue to develop exciting ideas and methodologies, lead the way into the future of personal communications electronics, and keep the challenges coming. All in a rewarding environment that fosters excellence.

You want to work for Rockwell Semiconductor Systems!

VLSI ENGINEERING
(Dept. Code: CAR-0501-V)

RF IC Design Engineer
Mixed Signal VLSI Design Engineer
DSP Software Applications Engineer
DSP Architect
Device Validation Engineer
ASIC Design Engineer
Mixed Signal Layout Designer

WIRELESS ENGINEERING
(Dept. Code: CAR-0501-W)

DSP Firmware Engineer
DSP Systems Engineer
Embedded Systems S/W Engineer
Hardware Development Engineer
Integration & Test Engineer
Product Applications Engineer
RF Systems Engineer
Systems Software Architect
Speech Implementor/Analyst
Systems Architect/Analyst

MARKETING
(Dept. Code: CAR-0501-K)

Product Applications Engineer
Market & Technology Planning Manager
Strategic Business Manager
Product Marketing Manager
Product Manager
Technology Planning Manager
Channel Marketing Manager
Marketing Development Manager

SALES
(Dept. Code: CAR-0501-S)

Sales Commissions Analyst
Field Applications Engineer
(Boston & San Jose)
Account Executive
Regional Sales Manager
(Mid-Atlantic)

SYSTEMS ENGINEERING
(Dept. Code: CAR-0501-Y)

Manager, Advanced Audio Product
Manager of Multimedia Application System Integration & Test
System Software Staff Engineer
System Firmware Staff Engineer
Imaging Processing Development Engineer
Imaging Systems Engineer
Lead Developer for Multimedia Applications
Sensor Engineer
Firmware & H/W Audio Development Engineer
Communication H/W Development Engineer
Speech Processing Engineer
Signal Processing Development Engineer

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PRODUCT FEATURE

(continued from page 128)

ing back video streams.

On the host side, the ViRGE/MX chip will offer both PCI and AGP interfaces. On the system side, it includes the company's Streams Processor video accelerator, which delivers high-quality video with arbitrary stretching (thanks to both horizontal and vertical interpolation) to the zoom-video interface. Drivers are available for Windows 95, Windows 3.11, Windows NT 4.0, and future OS releases from Microsoft (e.g., Memphis and Windows NT 5.0 workstation), as well as other OSs such as IBM's OS/2 version 3.0. Application programming interfaces are available for many libraries—Direct 3D, BRender, RenderWare, OpenGL, and so on.

The chip can handle screens with resolutions of 640-by-480, 1024-by-768, 800-by-600, 1280-by-1024 pixels, and other formats, as well as thin-film active-matrix panels with 9-, 12-, 18-, or 24-bit/pixel color depths, or double-twist STN panels with 8-, 16-, or 24-bit color depths. Additional features include auto-expansion and centering for VGA text and graphics modes on SVGA and XGA panels, and panel data polarity switching for EMI reduction. A 64-by-64-by-2-pixel hardware pop-up icon is available in all modes. Users can store eight separate bit maps to provide a selection of icon options.

In terms of notebook applications, designers at S3 paid considerable attention to power management. First, the chip operates from a 3.3-V supply but I/O lines are 3.3- and 5-V tolerant. Second, the circuit includes a standby/suspend capability to reduce power during idle periods. Finally, the chip includes dynamic power management that deactivates blocks of logic that aren't used during specific operations, minimizing the active power consumption. The ViRGE/MX comes in a 256-contact plastic ball-grid-array package that measures just 27 mm on a side. In large OEM quantities,the chip sells for $38 each in lots of 10,000 units. Samples are immediately available.

S3 Inc.
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Santa Clara, CA 95052
Peter Wicher, (408) 588-8000
http://www.s3.com
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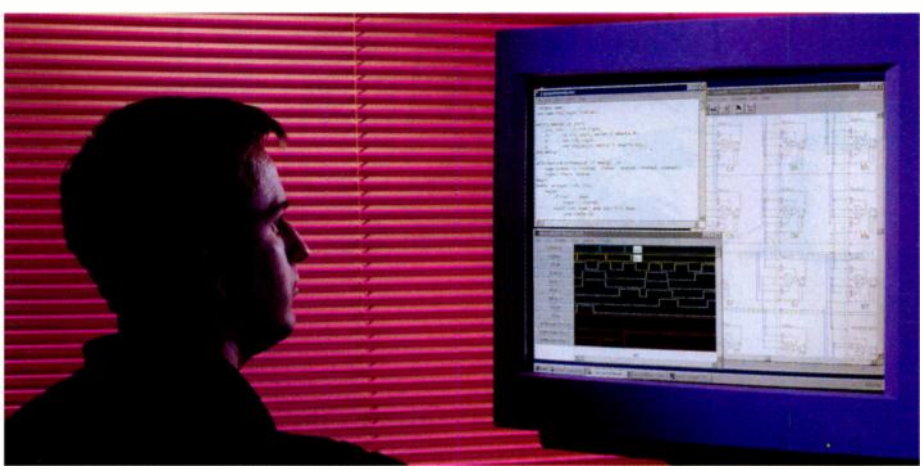
- "VHDL for Programmable Logic" book



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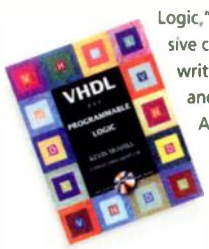

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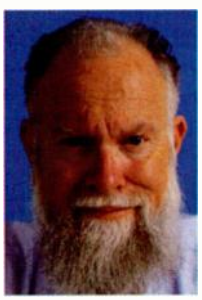
BOB PEASE

What's All This Web Stuff, Anyhow ?

Once upon a time, the world was a simpler place. There was no Internet; there were no Web Pages. While I am in favor of simplicity, I will not argue that we should (necessarily) all go back to a simpler age. But there certainly are some amazing things going on—and not all very useful or good.

YES, I do have a website. You could look it up yourself if you go to: *http://www.national.com/design*. My home page there is cleverly hidden as "good stuff." The actual site is *http://www.national.com/rap*. There are about 7 categories of good stuff there. More later.

My first interaction with the Web was about a year ago, when my column on "Speaker Cable Stuff" had just come out. One of my friends drew my attention to a Usenet News Group, where some fellow had made comments about my ideas on speaker cables. He said that he was "ROTFL" about some of the things I had said. I figured out this meant "Rolling On The Floor Laughing." He tried to say: "Ha, ha." But he must have held down his "ha" key too long, and he said "ha" 76 times. At that point, I tried to figure out why he thought it was so funny.



BOB PEASE OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

He claimed that since I had said that you could make a low impedance cable by connecting several cables IN PARALLEL to drive from an amplifier to a load, such as a speaker, I was stupid and full of baloney. He observed that if you parallel several cables, you do not get a low impedance cable, you just get a disastrous and impossible-to-analyze mess.

I tried writing to this guy. I tried to explain that if you have one signal driving through a length of coax cable (such as 50-Ω cable) into a resistive load (such as 40 or 50 or 60 Ω), then you can easily make a reasonable estimate of what will happen at the far end. Now, if you have (for example) 10 such coax cables, each independently driving a resistive load, the voltages will not change. THEN if you tie together the far ends of the ten 50-Ω cables each driving a resistive load—such as ten 50-Ω loads—still, nothing changes. The voltage response remains the same, but the cable's impedance IS effectively 5 Ω, and it's good for driving a 5-Ω load. It is NOT hard to analyze, not a mess. So, paralleling several cables to form a low-impedance cable that can drive a low-impedance load, with low phase shift and low reflections, is NOT an insane exercise, but actually a fairly simple, high-performance circuit to analyze—by symmetry.

I sent a note of explanation to the "ROTFL" guy. He never replied. He never gave any acknowledgement that I had a valid answer. So, if that is the way that the Internet works, then I am not impressed that this is a fair game.... people "flame" you with no provocation, and there's almost no defense against it. But, what did you expect in a domain where most of the information is HaTeMaiL?

I've looked at several good websites, and a few dozen mediocre ones, and some bad ones. I went to the "useless" site: *http://www.go2net.com/internet/useless*, and checked out a few of their "useless" websites. Yeah, there sure is a lot of useless information. For example, I am amused by the story of the coffeepot at CERN in Geneva Switzerland, that has its own website: *http://www.cl.cam.ac.uk/coffee/coffee.html*. If you work at CERN and you want to know if there's enough coffee in the pot to justify a long walk to the coffee room, then for *you*, it's *useful*, because *you* can *see* if the pot is full. For everybody else, *useless*. A friend urged me to look at the images from the Slug Video Camera at the Dream Inn from the Image Processing Lab at University of California, Santa Cruz: *http://sapphire.cse.ucsc.edu/SlugVideo/dream-inn.html*. Impressive, but not very useful. If you tell me about INTERESTING websites, I'll be interested.

I tried to access a site for old orphan computers, as mentioned in a letter we published in *Electronic Design* a few months back. Apparently that site was discontinued, but Brian Mork found the new location, at: *http://www.pas.rochester.edu/~tgpt/orphan*. They discuss several kinds of obsolete computers, but not the Tandy Model 102 or the ADAM.

On the other hand, there are some *new* sites that are virtually impossible to access. Some of the Anglophiles in our neighbourhood recommended the new site of the Queen of England at *http://www.royal.gov.uk*. I tried 10 times. I even tried at midnight when one would not expect them to be "too busy." I never did get in until I tried at 2:15 a.m. The site was very stately and classy—as you would expect.

But Pease, why are you wasting your time looking for the little mouse under the Queen's chair? Personal waste of the company's computer time? Not really. If I find something done nicely or properly, it may be useful in my next website. On the other hand, if I find annoying or objectionable features, I'll try to avoid them. If I find obsolete, out-of-date, or out-of-order sites—of which there are many—I'll try to learn from the experience.

I've checked out a few other good sites, and I'd like to mention them here. If you are interested in some vigorous hiking or trekking in Nepal, check out Peter Owens' site at: *http://www.Instantweb.com/p/peterowens*. It has the same basic information about hikes that you could get by mail, plus extra

BOB PEASE

information about the travel. And you can easily request detailed info on any particular hike—which will be delivered to you by e-mail. No waste of trees nor postage.

Wilderness Travel in Berkeley has gone online with their own site: *http://www.wildernesstravel.com.* I have not seen it yet, but they are pros in the travel business, and I've enjoyed trekking with them.

I really don't spend too much time at the Doctor Science site at *http://www.drscience.com*, but I have used the correct form at that site to request a daily hit of humor, which is delivered in my e-mail. I did send a question to the good Doctor:

"Dear Dr. Science: I just got to work and checked out your Questionable Hall of Fame, and at the end, the note said, 'Return Home.' So I did. And now my boss is mad at me. And my wife is mad at me. Why do you send me messages like that, Dr. Science?" Questions like that, I send to *drscience@drscience.com.*

On a professional note, I can recommend the site of Kimmel-Gerke Associates: *http://www.emiguru.com.* As I say on my lecture tour, "These guys are as good at getting you out of trouble above 1 MHz as I am below 1 MHz."

Similarly, I recommend you take a look at DAC/I Associates: *http://www.cyberspy.com/daci* for worst-case analysis of circuits. They have some good old Design Analysis Newsletters posted, too.

When it comes to product planning and business ideas, I regularly go to John Trudel's website: *http://www.trudelgroup.com.*

Don Lancaster has a lot of good write-ups on the topics of self-publishing and printing-on-demand. And electronics. And he has posted many links to Pseudoscience, Paranormals, and the Skeptics who try to rebut the flakey guys with the bad science. Start in at *http://www.tinaja.com.*

I found a guy promoting his new historical novel on the Web—check it out at *http://www.goodamerican.com.* I don't think I'll buy his book, but I agree that his advertising and promotional tactics make good sense. You can get a free peek at several pages of his book, and see if you want to buy it. I plan to do that with my books.

I have checked out Amazon Books, which has a very broad selection of books and some truly riotous book reviews by readers. Start at: *http://www.amazon.com.* I recommend the site of Rich Hanson, the purveyor of the venerable Tandy Model 102 Laptop Computers: *http://www.the-dock.com/club100.html.*

Also see the site of the other little Word Processor with 128k of memory: *http://www.alphasmart.com.*

Note to aficionados of guitar folk rock: I have recently become enamored of the sounds of "Babes with Axes," a group of 4 women who play guitars and sing and write their own songs. Their site has some music samples—not that I can tune in. Their site is at: *http://www.efn.org/~gordon_k/babes.shtml.*

I am still learning how to navigate on Netscape. I often crash and burn. The computer still gets locked up occasionally. And our Web Expert Gary still gets amazed at the way I get into trouble. When some guys wrote me messages at my website's response page, I tried reading some of them, and each message consisted of the first half of one message *and* the last half of the previous message. He had never seen that before. Fortunately, the next day, the problem went away.

One day, all my bookmarks went away. The next day, they all came back. Gary agrees that sometimes, the computer just doesn't seem to like me. It can tell who is sitting in front of it, and it does nasty things just because it knows it's me. Meanwhile, I keep threatening it, if it doesn't behave, I'm gonna throw it off the roof. If I hadn't just paid my tax bill, I could write a check and buy this insolent workstation—and throw it off the roof....

There are still all sorts of amazing things out there in "cyberspace," and some of them come and camp on your doorstep. One guy sent me a picture of a computer that caught fire. Since I didn't know what it looked like before it caught fire, it wasn't very educational. I could not guess why or how it caught fire. But it took me several minutes to erase the picture—all 17,000 lines.

Back on the subject of *my* website. What's in it? A good set of recent columns. So, if you need to look up a recent column, we'll try to keep a good set posted. We're still working on that. We have 18 columns in there, but we are not caught up yet. There's also a set of older applications information that have NOT been published recently. The first one was a good set of info on the Dielectric Absorption (or "soakage") of capacitors that was first printed in 1982. Several people have already said that they found it useful. The next is a reprint from *IEEE Micro* Magazine: "Third Thoughts on Fuzzy Logic." I confirmed several old opinions, and made some new positive observations. I'll print more stuff there. There is a link to my lecture: *http://www.national.com/events/peasetour.html*—and it is complete with a list of the topics I am likely to be discussing, and the form to use to sign up for the lectures.

There's a link to *Electronic Design* at *http://www.penton.com/ed.* Several people have pointed out to me that it had a neat page that you could use to sign up for a free subscription to the magazine. When you're all done, you looked for the link to hit to send it. There wasn't any!! You were supposed to print out this form and mail it or fax it in. Fortunately, this is being fixed. But when I mentioned this situation at my lectures, it always got a good laugh! There are a few "horrible" pictures. I'll have to add more.

There's a page that makes it very easy to send e-mail to me: *rap@webteam.nsc.com.* (I probably shouldn't have admitted that, but it's true.)

After I spent a while driving around to various web sites, I began to appreciate more of what Gary had done for me: In a lot of places, when you *click* on a page, you wait 15 or 25 (or more) seconds, and finally some eye-popping scene pops up. Apparently, a lot of guys think that if you *can* do snazzy, blinking, bouncing graphics, then you *should.* Yeah, but I find it annoying that so little information wastes so much time. Yeah, I know that "a picture is worth a thousand words." It may cost you 10,000 words worth of information, and when you get it, after a long wait, you discover that you don't want it.

When you hit on *my* home page, the text comes up in about 4 seconds. Then while you are reading the text, about 7 seconds later, the graphics pop up. I like that a lot better than waiting 10 or

BOB PEASE

20 seconds before you can see *anything*. I'm glad Gary did that right.

What else should I put on my website? What do you think? You tell me.

For example, what if I told you that you could get a full 20 seconds of video of RAP throwing 3 computers off a roof?—or a 30-second lecture on op amps?? This would take minutes to get all the bytes into your computer. So, you set the command, and hit the *receive file* button when you leave work at night, and when you get in to work the next morning, the bytes are all ready for you. After all—why should your computer be finished with work just because *you* quit and go home?

What can I say about the Web? It drives me crazy. It's the slowest way to do some things, and a pretty good and quick way to do other things. It's fun *and* frustrating. It encourages people to send me questions that I cannot answer. But I'm a big boy, and I'm learning to live with that, and I've learned some work-arounds. At first, when I wanted to send a reply to a question, the response got sent—but the person's e-mail address got left off. Not very helpful. *Fortunately*, I did not erase any of the messages before I discovered this. I had to find an alternate *Reader*, so I could read a message and send a note back, and *not* erase the vital information. Never a dull moment!

P.S. I nearly forgot to say this, because it's easy to get enthusiastic about the Web: I forgot to include real phone numbers and real addresses for the companies with the good WEBSITES. Not nice. I really don't like to discriminate against guys who don't go on the Web.

So. (1) If you DO go on the Web, you can look up these addresses and phones in the new section on LISTS.

(2) If you CAN get on e-mail but NOT on the Web, send me a message at *rap@webteam.nsc.com* and I'll e-mail the LIST to you.

(3) If you CAN'T get on e-mail, just mail me a letter, and I'll send you that LIST.

All for now. / Comments invited!
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READER SERVICE 141

HOWARD JOHNSON

Planning For Signal Integrity

Today's advanced digital products are built using PCI, GTL, BTL, and other popular high-performance bus driver chips designed to run at 33, 66, and 100 MHz or more. These products are fast. It takes planning, experience, and more than a little lab work to get digital designs to work with such fast parts.

At these extremes of speed, even simple problems, like ringing, can become complex. For example, a typical 3.3-V gate does not need a terminator to drive a 2-in. unloaded trace. The results just naturally work out all right *(see the Figure, $C_L = 0$)*.

But, add a single 5-pF load to the end of that same trace and it will begin to ring violently, taking an extra 2 ns to settle to within acceptable voltage margins after each transition. Is that kind of extra time built into your timing calculations? Nowadays, it had better be. Capacitive loading can sometimes (but not always) markedly worsen ringing and settling problems on unterminated lines.

If you are trying to cut it close with logic timing (and who isn't), loading effects like this can really ruin your day. To get some help, check out the nifty new simulation tools now available for dealing with signal integrity problems.

The basic assumption with all computer simulations is this: If you can develop a simulation method that has good correlation to the real world, then you can use it to simulate your pc-board trace layouts before you build them. And what's more, you can make the computer check every single trace, with every combination of worst case loads, which is something most of us don't have the time to do in the lab. With the right software, a computer can debug a whole month's worth of signal integrity problems without ever committing to a pc-board's fabrication cycle. Of course, the key to this whole approach is a good correspondence between your simulator and the real world.

Presently, there are (at least) three different approaches to signal integrity simulation:

- General-purpose Mathematical calculation environments, like MathCad, Mathematica, and Matlab.
- Analog simulation tools, like Spice, HSPice, and Pspice.
- Specialized signal integrity simulators, like HyperLynx, Cadence, Mentor/Interconnectix, and View Logic/Quad Design.

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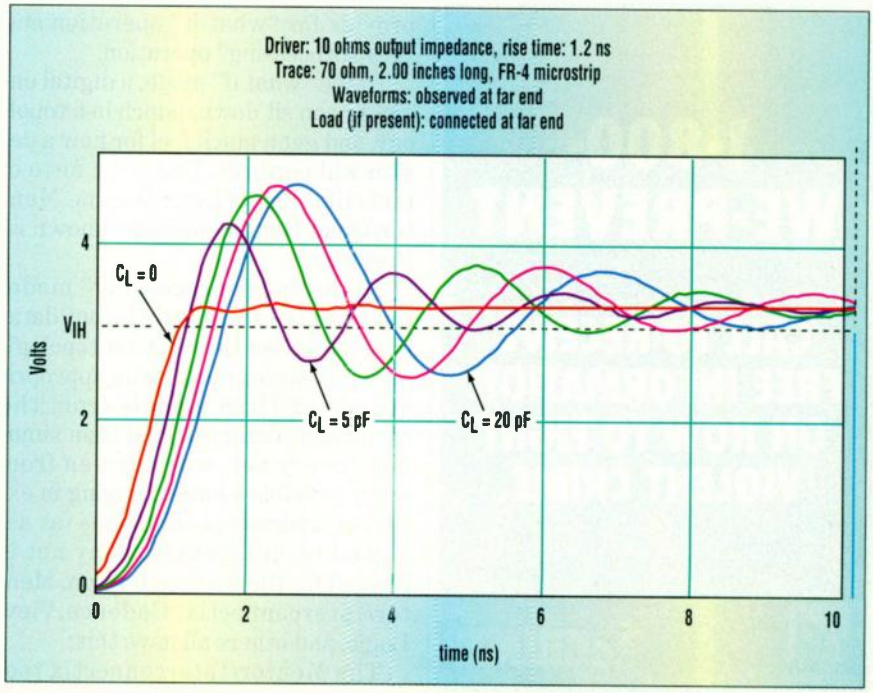
General-purpose mathematical calculation tools will let you mix together pictures, equations, and explanatory text in the same document. Using their general-purpose math libraries, it is possible to simulate the performance of practically any digital transmission structure.

Especially good for long-distance LAN communication problems involving frequency-dependent losses (like the skin effect) the flexibility of these tools is invaluable. They also have the advantage of being able to simulate a great number of different worst-case scenarios, including random topologies, peculiar noise sources, and various flavors of crosstalk.

The biggest disadvantage to the general-purpose tool approach is the degree of customization required to model any particular problem. If you do the customization yourself, it probably won't have much of a user interface. It may also be extremely awkward to import your trace layout database and work with it. 'Nuff said.

Traditional analog simulation tools can adequately simulate the most common digital scenarios. Spice, HSpice, PSpice, and all the other Spice variants have good models for handling simple loss-less, distortionless transmission lines. These models are appropriate for simulating ordinary printed circuit boards with only a few traces. One nice advantage of working with analog simulation tools is that many of them have a good GUI front-end, with schematic capture capability. That lets you draw a pictorial representation of your circuit, double-check the drawing to



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make sure it's right, and then submit the completed circuit to the simulator. The pictorial process cuts down on errors.

Spice works exceptionally well when you have good circuit models of both the transmitter and receiver circuits. Its prediction of overshoot and ringing waveforms are surprisingly accurate, given good enough models. The biggest drawbacks to using Spice are that it has no provision for importing a trace layout database, and it has no general way to properly assess crosstalk on your layout.

Whatever method you choose, start simple and keep it closely tied to physical reality.

Specialized signal integrity tools attack the trace simulation problem from two new angles. First, they use IBIS models for the driver and receiver. The IBIS models specify, for each driver, a V-I curve to be used in the low state, a V-I curve to be used in the high state, and a finite speed at which the driver transitions from one curve to the other. This arrangement is not perfect, but it's definitely useful. Second, they offer a compact, user-friendly interface, optimized for signal integrity work. The user interfaces for most signal integrity tools provide for "what-if" operation and "post-processing" operation.

In the "what if" mode, a digital engineer can sit down, punch in a topology, and get a quick feel for how a design will perform. That's the forte of tools like HyperLynx and the Mentor/Quad Design package known as Preview.

In the "post-processing" mode, the software scans your layout database to extract the relevant topological information, picks up an appropriate set of IBIS models from the component database, and then simulates every net, when driven from every possible source. Ringing in excess of desired specifications (as assigned by net class) for any net is flagged for the user's attention. Mentor/Interconnectix, Cadence, View Logic, and others all have this.

The Mentor/Interconnectix tool goes one step further than the others. It actually adds terminators to fix broken nets, re-simulates them to verify compliance with specifications, and then generates change files as needed to show the additional parts. Pretty neat stuff. Of course, the problem with this level of automation is that the raw source information that you type into the system (that is, the IBIS models, the ringing specifications, and the allowed terminator topologies) must be 100% correct for the system to function properly. As with any CAD automation tool, the quality of your library determines the quality of the final result.

Whatever method you choose, start simple and keep it closely tied to physical reality. Try simulating one lowly NAND gate driving a 10-in. unterminated line, and check to see if your results match what you see on the bench. If there are discrepancies, work on the simulator (or your probing technique) until they match. If you are working with logic as fast as 1 ns, your model will need to include packaging parasites (IBIS can do that). As your confidence with the simulator increases, branch out to more complex topologies.

Periodically, return to the bench for corroboration. Remember, simulation is always fun, but it's only helpful if you are sure the simulator matches what's really going on in your design.

Dr. Howard Johnson (howiej@sigcon.com) is the president of Signal Consulting Inc., a high-technology consulting firm specializing in solving high-speed digital design problems. He is the author of "High-Speed Digital Design: A Handbook of Black Magic" (Prentice-Hall, 1993), and a frequent guest lecturer at both the University of Oxford and UC-Berkeley. For information about his ongoing series of on-site workshops for digital engineers, visit Signal Consulting's website at http://www.sigcon.com.

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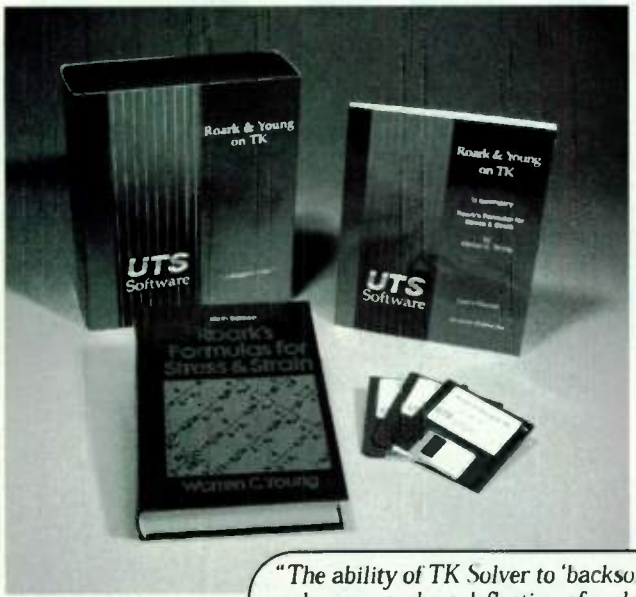

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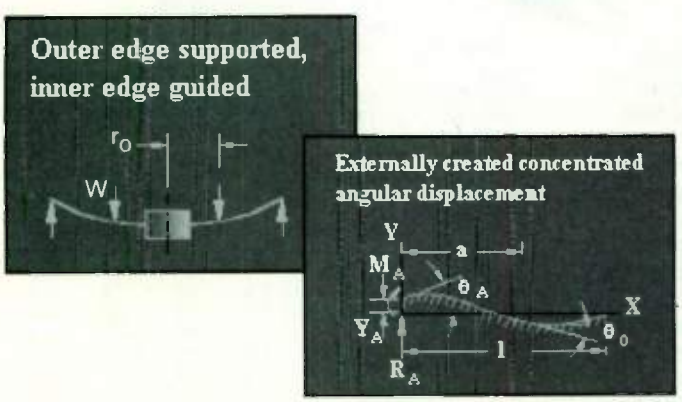

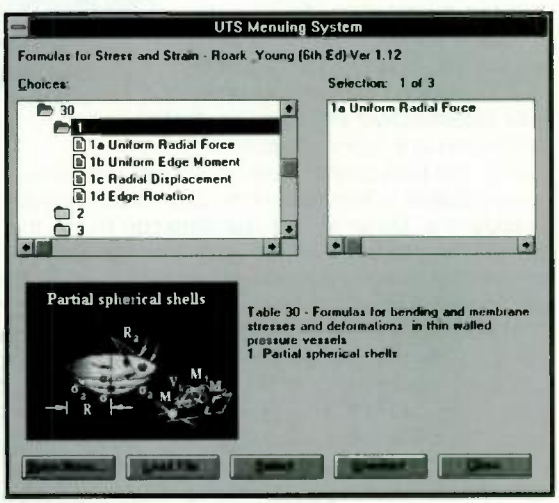

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SBL-1-1	0.1-400	5.5	45	40	+7	7.25
SBL-3	0.025-200	5.5	45	40	+7	7.25
• SBL-11	5-2000	7.0	35	30	+7	18.75
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• SBL-1XLH	10-1000	6.0	40	55	+10	7.25
SBL-2LH	5-1000	5.9	61	54	+10	8.20
SBL-3LH	0.07-250	4.9	60	53	+10	8.20
• SBL-11LH	5-2000	7.0	45	30	+10	19.70
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Circle 520

Add An RS-232 Output To Any PIC Microprocessor

RON TIPTON
TDL Electronics, 5260 Cochise Trail, Las Cruces, NM 88012-9736;
(505) 382-8175; fax (505) 382-8810; e-mail: RTipton@zianet.com.

Some PIC microprocessors have a built-in serial interface module while others do not. The latter group includes the 16C54, '55, '56, '70, '71, '72, and others. Adding a serial output to these processors takes but a few lines of code *(Listing 1)*.

All of these PIC microprocessors execute one instruction cycle for every four clock cycles. Most assembly instructions complete in one instruction cycle, although a few (such as GOTO) take two cycles. The first step is to write the RS-232 output instructions. Then calculate their execution time, and finally, find the delay count needed to give the correct bit time based on clock frequency and baud rate.

In Listing 1, the first "block" of code (between START and GOTO DY1) sets up the 8-bit data length and generates one start bit. The delay count loaded into TEMP sets the bit duration. The second code block (between LOOP and GOTO LOOP) transmits the number in VALUE one bit at a time, least-significant bit first. Again, the delay count in TEMP sets the bit duration. The final code block generates one stop bit.

Clock frequency divided by baud rate should be at least 400 to get adequate baud-rate accuracy. As an example, the clock frequency should be 480 kHz minimum for 1200 baud. This gives an instruction cycle time of 8.33 µs. At 1200 baud, one bit time is 833.33 µs. Therefore, the first code block should use that amount of time to send the start bit. The first five instructions take 41.65 µs; 833.33 µs minus 41.65 µs equals 791.66 µs. Thus, the DY1 to GOTO DY1 loop must be repeated enough times to use up this interval.

The DECFSZ instruction uses one instruction cycle, the GOTO uses two; N = 791.66/3(8.33) = 31.68. This rounds up to 32 . If needed, a NOP will add a one instruction cycle delay. As long as the bit duration is within 2 or 3%, it's close enough.

The Listing 1 routine was written to drive an inverting RS-232 driver. If you want to use this code without the inversion, then the BCF PORT_B,Tx instructions (clear Tx bit in register PORT_B) would be changed to BSF (to set the Tx bit) and vice versa. The port and Tx bit can be changed to any available I/O pin by consulting the appropriate PIC data sheet. This code can be embedded in a higher-language program such as "C" or Pascal. Merely define COUNT, TEMP, and VALUE as 8-bit integers and remove the memory variable definitions.

Listing 2 shows a simple MS-DOS BASIC program to test the serial output. It read 20 values from the serial data stream and displays them on the monitor screen. The RS-232 transmit routine operates in "broadcast" mode, that is, handshaking with the receiver isn't used. A two-wire connection, signal, and common is all that's required. However, you may have to connect DTR to DSR and RTS to CTS at the receiving end to get your PC serial port to respond.

```
; RS-232 Transmit routine for PIC Microprocessors
;
;  This routine generates 1 start bit, 8 data bits and 1 stop bit, no
;   parity (8,N,1). This code is for a 480 kHz clock and 1200 baud
;   output. These parameters can be easily changed, see text.
;
;  Place the number to be sent in VALUE, then call the routine.
;
;  Memory variable definitions
TEMP   EQU    8
COUNT  EQU    9
VALUE  EQU    0xA

;  Port and pin definitions
PORT_B EQU    6
Tx     EQU    4

START:
     MOVLW    8
     MOVWF    COUNT
     BCF      PORT_B,Tx      ; zero start bit (clear bit 4 in reg 6)
     MOVLW    32             ; delay count for 480 kHz clock
     MOVWF    TEMP
DY1:
     DECFSZ   TEMP,1
     GOTO     DY1
LOOP:
     BCF      3,0            ; clear carry bit, bit 0 in reg 3
     RRF      VALUE,1        ; rotate value bit to carry, LSB first
     BTFSC    3,0            ; skip next instruction if carry is clear
     BSF      PORT_B,Tx      ; send data bit if equal to one
     BTFSS    3,0            ; skip next instruction if carry is set
     BCF      PORT_B,Tx      ; send data bit if equal to zero
     MOVLW    30             ; delay count for 480 kHz clock
     MOVWF    TEMP
DY2:
     DECFSZ   TEMP,1
     GOTO     DY2
     DECFSZ   COUNT,1
     GOTO     LOOP
     BSF      PORT_B,Tx      ; send stop bit = 1
     MOVLW    32             ; delay count for 480 kHz clock
     MOVWF    TEMP
DY3:
     DECFSZ   TEMP,1
     GOTO     DY3
```

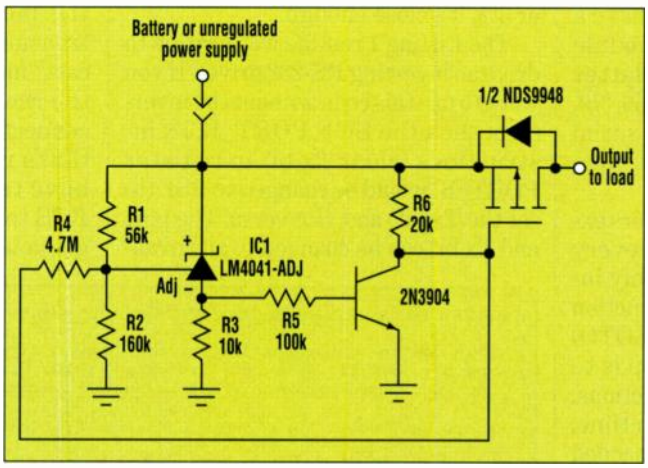
```
REM      PIC RS-232 Demo program
REM      Reads RS-232 output and displays value on screen

       CLS
       J% = 0
       OPEN "COM1:1200,N,8,1,CD0,CS0,DS0,OP0,BIN" FOR INPUT AS #1
M1:    VALUE$ = INPUT$(1, #1)
       PRINT ASC(VALUE$)
       J% = J% + 1
       IF (J% < 20) GOTO M1
       CLOSE
       END
```

Circle 521

Simple Circuit Shuts Off System When Supply Voltage Is Low

KERRY LACANETTE
National Semiconductor Corp., 6377 E. Tanque Verde Rd., Tucson, AZ 85715; (520) 751-3769; fax (520) 751-2379.

Many low-cost and portable systems, including small consumer electronic products, operate from unregulated power supplies such as batteries or external, plug-in "power bricks." These power sources sometimes produce lower-than-nominal output voltages--either through normal battery discharge, "brownouts," or simply connecting the wrong "brick" to the system. When supply voltage drops below a minimum threshold, it's often good practice to disconnect the supply from the system to prevent poor performance or erratic operation.



This low-cost, space-saving circuit will shut down a portable system when the supply voltage drops below a minimum threshold.

The circuit shown accomplishes this with minimal cost, board space, and complexity *(see the figure)*. In addition, the active components are available in tiny, "SOT-23" packages. IC1 is an LM4041 adjustable voltage reference that serves here as a programmable voltage detector. It does this by operating in an unconventional configuration. Typically, the LM4041 develops a voltage between its positive and negative terminals that forces 1.24 V between its "+" and "ADJ" pins. With R3 in the circuit, however, IC1's "-" pin will be near ground when the voltage across R1 is less than 1.24 V, and about a volt below V+ when the voltage across R1 is greater than 1.24 V.

When the supply voltage is in the normal operating range (above about 4.6 V in the circuit shown), the voltage across R1 will be greater than 1.24 V. This pulls the LM4041's "-" pin high, turning on the npn, which then turns on the p-channel MOSFET by pulling its gate low. In this condition, power is supplied to the load through the p-channel device.

When the supply voltage drops below the normal operating range, the LM4041's "-" pin goes low, turning off the npn and the MOSFET pass device, which removes power from the load. R4 provides hysteresis to avoid supply modulation near the switching threshold.

By selecting R1 and R2 properly, you can choose the threshold voltage to fit the needs of your system according to:

$$R2/R1 = (V_{low}/1.24\ V) - 1$$

where V_{low} is the low-voltage shutoff threshold. By proper choice of R1 and R2, this circuit will work well for shut-off voltages in the range of about 4.5 to 10 V. The lower limit is determined by the pass FET's threshold voltage and the upper limit is determined by IC1's maximum supply-voltage rating. Higher cutoff voltages can be accommodated with minor circuit changes. The maximum supply voltage for the circuit shown is approximately 30 V.

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Circle 522

Read 16 Digital Inputs Using A PC's Serial Port

YONGPING XIA
23008 Arlington Ave., Torrance, CA 90501.

Illustrated is an interface circuit that allows a PC to read 16 channels of digital inputs *(see the figure)*. The circuit is connected to the PC's COM1 serial port directly. The same serial port also powers the circuit so that no additional power supply is needed.

There are four directly accessible input lines (pin 1, 6, 8, and 9) in a RS-232 serial port. These four lines are expanded by two dual four-input multiplexers (IC-1 and IC-2) to accept 16 inputs. The inputs can be on/off switches or open-collector/drain transistors between each input line and ground. Each of the input lines has a 100k pull-up resistor to set logic high when the switch is off.

Two output lines (pins 4 and 7) control the selection of the input channels. Each line condition allows the PC to read four input channels under the control of the C program *(see the listing)*. Output pin 4 also provides

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The MAX836/MAX837 voltage monitors are similar to the MAX834/MAX835, except they come in a 4-pin SOT143 package and do not have a latched output.

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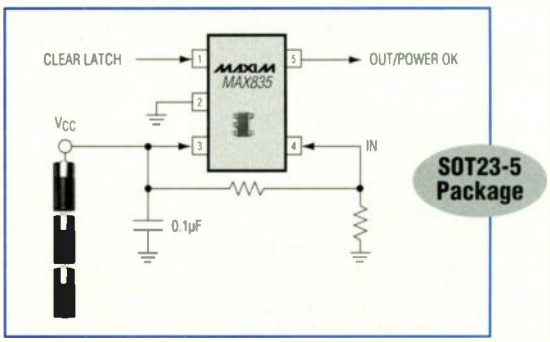
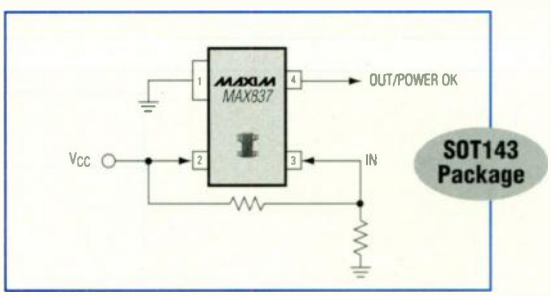


The MAX835 has a push/pull output while the MAX834 has an open-drain N-channel output driver.



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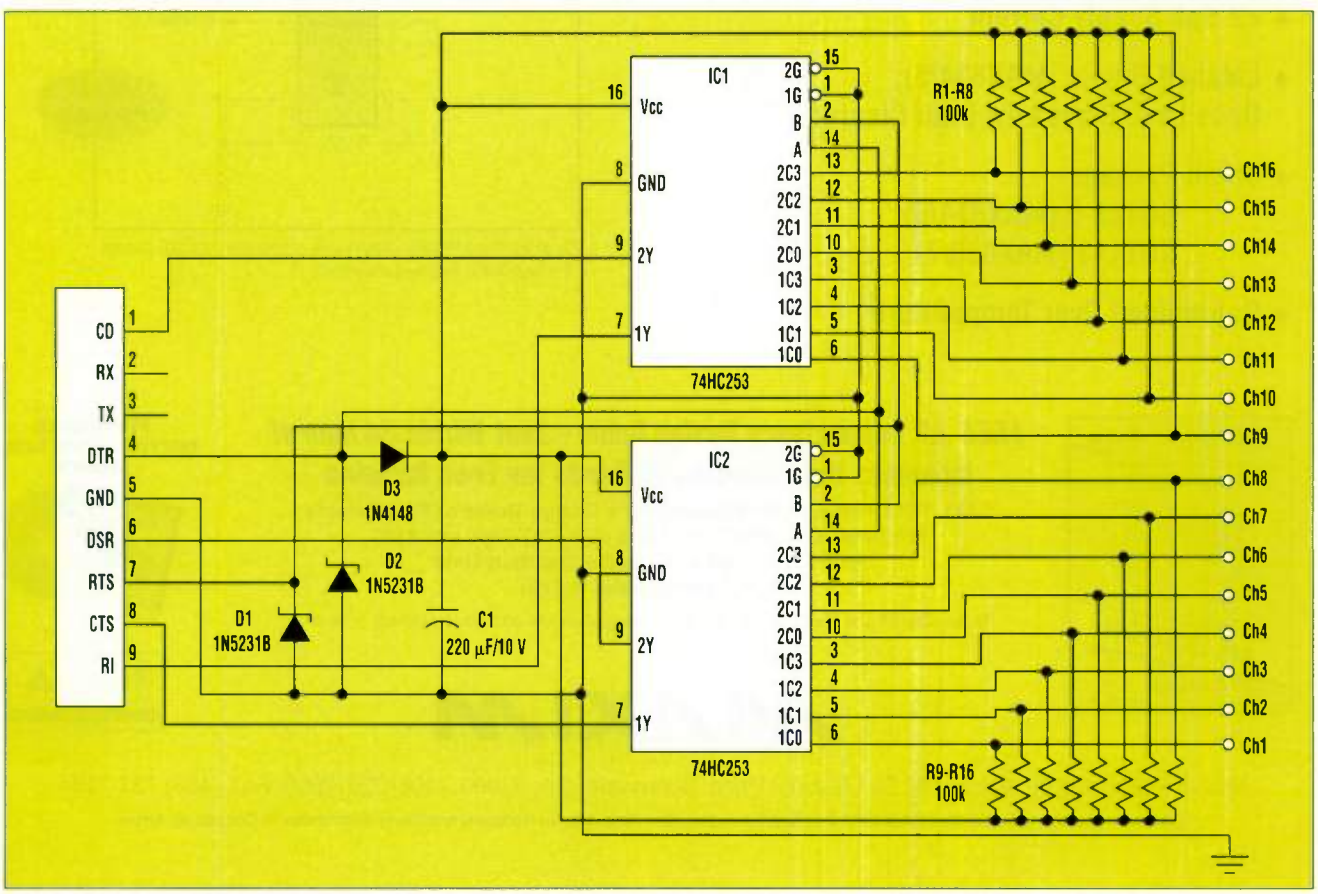
Circle No. 150 - For International

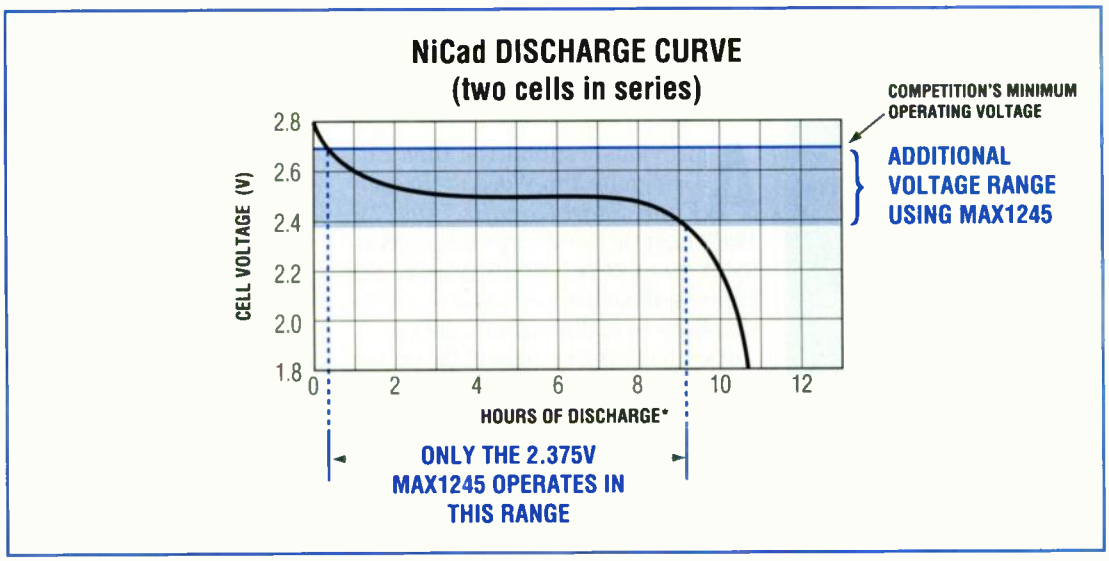
the power supply for ICs through diode D3. C1 holds the energy to power ICs when pin 4 is low. Once pin 4 is high, C1 will be charged up again. Because the serial port provides both positive and negative current outputs, two Zener diodes (D1 and D2) are used to limit the voltage range of output lines within -0.6 and +5.1 V.

```
#include <stdio.h>
#include <dos.h>
#include <time.h>
#include <conio.h>

#define MCR     4                       /* control register
*/
#define MSR     6                       /* status register
*/

unsigned long  count[16], ch_old[16], ch_new[16];
int  i, base_add1=0x3f8, base_add2=0x2f8;

void set_port(void)
{
  outportb(base_add1+MCR, 0x03);    /* DRT high, RTS high
*/
  delay(1000);
}

void read_port (void)
{
  int data;
  for (i=0; i<4; i++)
    {
     outportb(base_add1+MCR, i);
     delay(5);
     data=inportb(base_add1+MSR)/16;
     delay(5);
     ch_new[8+i]=data&0x01;
     ch_new[12+i]=(data&0x02)/2;
     ch_new[i]=(data&0x04)/4
     ch_new[4+i]=(data&0x08)/8;
    }
  for (i=0; i<16; i++)
    {
     if (ch_new[i]==0)
{
if(ch_old[i]==1)
          count[i]++;
       ch_old[i]=0;
     }
    else
      ch_old[i]=1;
   }
}
void dis_data(void)
{
  for (i=0; i<9; i++)
   {
    printf("Channel %d =  %d\n", i+1, count[i]);
   }
  for (i=9; i<16; i++)
   {
    printf("Channel %d =  %d\n", i+1, count[i]);
   }
}

void main(void)
{
  int read_data;
  char temp;
  clrscr();
  set_port();
  gotoxy(60,24);
  printf ("Hit any key to quit");
  do{
     gotoxy(1,1);
     read_port();
     dis_data();
     delay(10);
    } while(!kbhit());
}
```

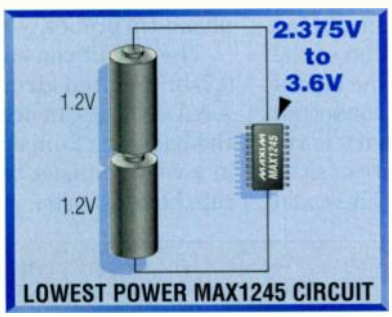


This simple data acquisition circuit allows a PC to read 16 digital inputs while deriving its power supply directly from the PC serial port.

LOWEST VOLTAGE 12-BIT ADC OPERATES BELOW 2.4V



Operating at the lowest voltage saves power, since ICs typically dissipate less power as the voltage decreases. The 8-channel, serial 12-bit MAX1245 ADC has guaranteed performance down to 2.375V, making it the lowest voltage 12-bit ADC available. Its low voltage allows operation from two standard NiCad, NMH, or alkaline batteries, saving size, weight, and cost in portable applications. With two cells it operates longer; its minimum operating voltage is closest to battery end-of-life. The MAX1245 also meets 2.5V ±5% power supply requirements (2.375V minimum), making it ideal for your most demanding low-power applications.



- **Guaranteed Operation Down to 2.375V**
- **3-Wire Serial Interface Compatible with SPI™, QSPI™ and Microwire™**
- **8 Single-Ended or 4 Differential Inputs**
- **1µA Powerdown Mode**
- **Small 20-pin SSOP Package**
- **Sampling Rate: Up to 100ksps**

* Total system current of 85mA (MAX1245 current < 1mA).
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Circle No. 152 - For International

Circle 523

Improved Short-Circuit Detector

F. PATTERSON SMITH
Spectrum Probe, 207 E. Prospect Ave., N. Wales, PA 19454; (215) 661-9107.

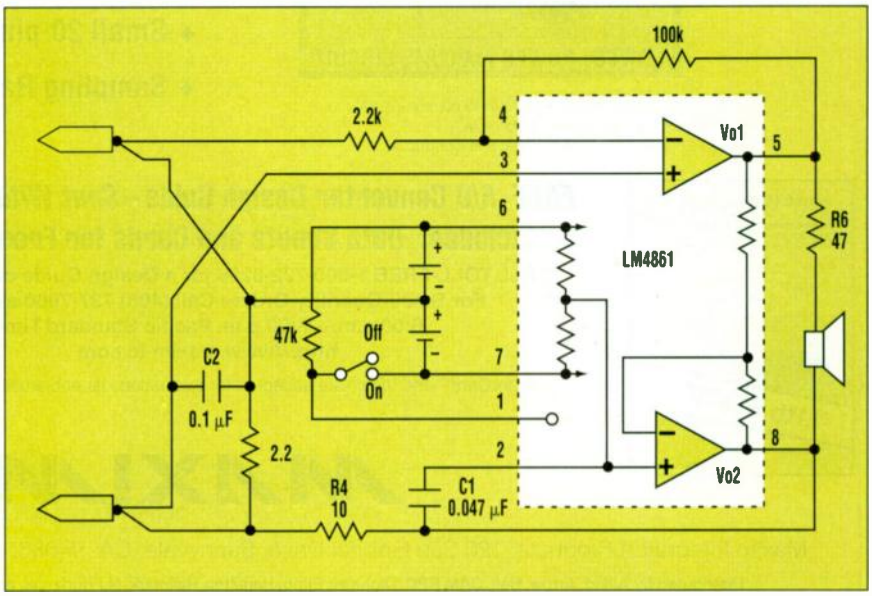
A previously submitted Idea For Design by Jim Wood (" *'Beeper' Finds Short Circuits,*" *Oct. 24, 1996* "BEST OF ISSUE" SPECIAL SUPPLEMENT TO ELECTRONIC DESIGN, *p. 18)* impressed me because of the circuit's simplicity to realize a useful gadget. It suffers, however, because of the power required: ±12 V @ approximately 60 mA—hardly a small portable gadget! This is used to develop a ±100-mA current audio square wave. With the availability of audio ICs designed for two-cell battery operation, it seemed that a better solution could be found. National Semiconductor's LM4861 fills that requirement.

The circuit designed differs in the oscillator and its frequency control *(see the figure)*. The normal Vo2 (-1) amp has capacitive positive C feedback rather than a series R shunt C on the negative input. Variation of the Vo1 amp's output changes the bias of the oscillator Vo2 since it's connected internally. The pitch polarity is reversed—frequency decreases as the short circuit is approached. This could be avoided, but the virtue of reducing the speaker volume when the leads are open would be lost. It is relatively quiet when not being used.

A two-cell supply, together with the load resistor R4 reduction to 10 Ω, creates a ±130-mA square wave to the short circuit. Reasonable speaker level is set by reducing R6 to approximately 47 Ω. The maximum current drain is approximately 80 mA. The capacitor C2 eliminates some circuit instability.

Typically, with the center-tapped battery, a double-pole On-Off switch is required. By using the shutdown mode of the LM4861, the unit can be turned Off (0.6 μA residual) by a single-pole logic switch. All of the notes in Jim Wood's article apply. Note the differential input requirement and the recommendation of piercing phono-tip probes.

The circuit can easily be built on a 0.7-in^2 printed circuit board. Using AAA cells, it can occupy the space in the back of a 2-in. speaker, resulting in a very compact tester that can locate board shorts.

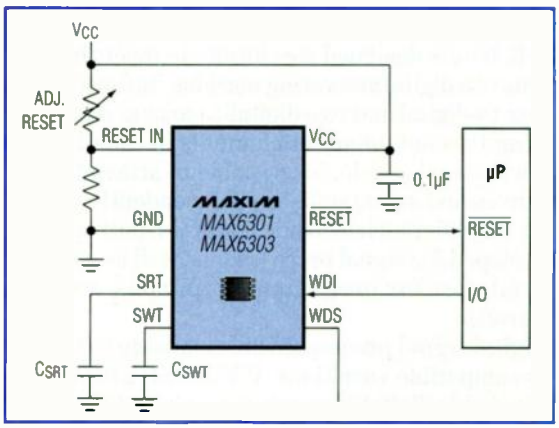


This short-circuit detector improves on an earlier Idea For Design by employing the LM4861, which ultimately makes it a much more compact, battery-powered tester.

COMPLETELY ADJUSTABLE RESET + WATCHDOG IC HAS ONLY 4µA I_{SUPPLY}

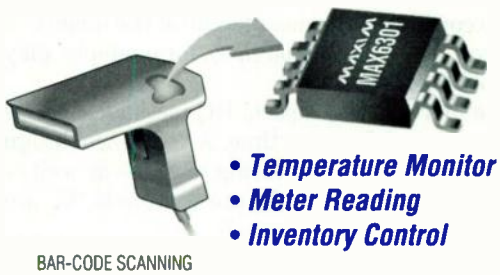
- Adjustable Reset Trip Threshold: ≥1.22V
- VCC Monitor 2.0V to 5.5V
- Adjustable Reset Timeout Delay
- Adjustable Watchdog Timeout
- Power-Supply Transient Immunity
- DIP/SO/µMAX Packages
- Wake-Up Timer
- 4 Output Versions:

PART	RESET OUTPUT	OUTPUT DRIVER
MAX6301	Active Low	Open Drain
MAX6302	Active High	Open Drain
MAX6303	Active Low	Push-Pull
MAX6304	Active High	Push-Pull



Get complete flexibility: set your timeout delays and trip thresholds as needed.

Perfect for Portable Monitoring and Data Logging Systems



The MAX6301-MAX6304's low supply current, wake-up timer, and ability to set short timeout delays, make them ideal for portable monitoring and data logging.

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Circle No. 153 - For U.S. Response
Circle No. 154 - For International

Digital Answering Machine And Feature Phone In Dual Codec

The "SAM" chip set consists of a double codec with amplifier, analog switching network, and a digital signal processor that's responsible for the answering machine functions and—depending on the degree of functionality—for further feature functions. The dual codec PSB 4851 is designed specifically to meet the requirements of a digital answering machine. It consists of two analog-to-digital and two digital-to-analog converters serving two independent channels in the digital range. On the analog side, it's possible to attach three signal sources and signal sinks via independently programmable amplifiers. The module features a port specifically developed for signal processing as well as a standard serial port for programming purposes via a microcontroller.

The digital signal processors are available in three upwards-compatible variations. While PSB 2168 is intended for simple digital answering machines, PSB 4850 offers additional speakerphone functions. PSB 4860 even offers advanced speakerphone features like full-duplex operation with acoustic echo suppression. The answering machine operates in two modes: HQ (high quality) and LP (long play), providing a recording time of 7 or 19 minutes, respectively, with 4 Mbits of storage capacity. According to the manufacturer, the quality of the HQ recording is good enough to, for example, play music on hold functions.

To create more storage space, HQ messages can be recompressed into LP at any time. A reference design for a feature phone with answering machine as well as the source code of modular software written in "C" are available. *AV*

Siemens AG, *Semiconductor Group, P.O. Box 80 17 09,81617, Munich, Germany; phone: +49-89/4144-0; fax: +49-89/4144-4694.* **CIRCLE 470**

Attain 155 MHz In Fundamental Mode With Thin Quartz Plates

Thinner quartz plates, which create high frequencies, result when the quartz crystal frequency is inverse proportional to its thickness. For example, a 15-MHz quartz crystal in fundamental mode corresponds to a thickness of 100 mm and a 150-MHz device corresponds to a thickness of 10 mm. By using standard semiconductor technology, such as lithography and etching, it's now possible to manufacture very thin quartz plates.

To mechanically stabilize the quartz plate, only the inner part of the quartz crystal is etched down to the desired frequency, representing an "inverted mesa structure." The quartz then looks like a vibrating membrane mounted in a picture frame. The housing starts with the standard HC-52 at a height of 5.45 mm. HC-52 slim-line packages as well as SMD flat packs are in the works.

Furthermore, the same company has announced VCXOs for SONET and SDH applications that are housed in a DIL-14 package. These oscillators offer a pulling range of ±100 ppm for frequencies between 44.736 MHz and 155.52 MHz. Their stability is specified to be smaller than ±15 ppm within the temperature range from -20°C and +70°C. The power-supply voltage of the VCXOs, which are available with HCMOS and PECL outputs, is 5 V. *AV*

KVG Kristall-Verarbeitung GmbH, *Waibstadter Str. 2 - 474924, Neckarbischofsheim, Germany; phone: +49-7263/648-0; fax: +49-7263/61 96.* **CIRCLE 471**

Subrack For 19-In. Racks Offers Two Horizontal-Rail Types

Based on the IEC standard 297-3 (DIN 41494), the subrack system Europac Pro for 19-in. racks provides two versions of horizontal rails. Depending on the requirements, a lightweight version with single-hole mounting or a stable heavy-duty version with double-hole mounting is available. The rail surface is anodized, making it scratch resistant; however, all surfaces required for contacts remain conductive.

In contrast to its predecessor, horizontal Eurodac Pro rails are automatically centered with a specially-designed screw. Three versions of side plates with an identical grid pattern are available for different mechanical requirements. Because guide rails serve as a connection between a subrack and plug-in unit, they have to meet various requirements. For example, there's a longer guide funnel that facilitates the positioning and insertion of boards.

Suitable accessories are available for keying of slots and the board retainer. Keying is realized by means of pins in the guide rail head and corresponding pins in the handle of the plug-in unit. There are a total of 64 keying positions. By adding shielding components, all subracks can be shielded. Pluggable RFI springs ensure contact between front panel and horizontal rail, between the 19-in. brackets of the side plate and the front panel as well as between the horizontal rail and the cover plate. An additional cabinet control system CCS 10 offers remote controlling of operational data in networking cabinets. This unit can be temperature- or humidity-controlled. It also can be triggered by, for example, door alarm contacts, bringing unauthorized access to attention. Furthermore, it offers three digital inputs that can be used for smoke or motion detectors. *AV*

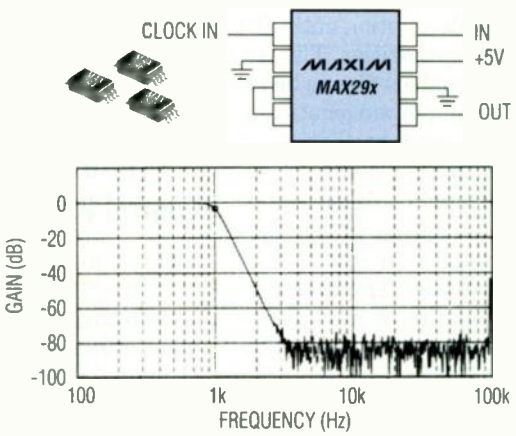
Schroff GmbH, *P. O. Box 3, 75332 Straubenhardt, Germany; phone: +49-7082/794-695; fax: +49-7082/794-200.* **CIRCLE 472**

SMALLEST 8TH-ORDER LOWPASS FILTERS FIT IN SO-8

Elliptic, Butterworth and Bessel with No External Parts

Maxim's MAX291/MAX295 (Butterworth), MAX292/MAX296 (Bessel), and MAX293/MAX294/MAX297 (Elliptic) 8th-order lowpass switched-capacitor filters now come in a space-saving 8-pin SO package. All three filter types have fixed responses; set the filter's corner frequency by simply choosing an appropriate clock rate.

- 8-Pin SO and DIP Packages
- No External Components
- +5V or ±5V Supply Operation
- THD + Noise: -70dB Typical
- Cascadable for Higher Orders



The MAX291's 8th-order Butterworth response has 48dB per octave rolloff with no passband ripple.

PART	TYPE	CORNER FREQUENCY RANGE	CLOCK:CORNER	COMMENTS
MAX291	Butterworth	0.1Hz to 25kHz	100:1	No Passband Ripple
MAX292	Bessel	0.1Hz to 25kHz	100:1	Fastest Settling
MAX293	Elliptic	0.1Hz to 25kHz	100:1	133dB/Octave Rolloff
MAX294	Elliptic	0.1Hz to 25kHz	100:1	205dB/Octave Rolloff
MAX295	Butterworth	0.1Hz to 50kHz	50:1	No Passband Ripple
MAX296	Bessel	0.1Hz to 50kHz	50:1	Fastest Settling
MAX297	Elliptic	0.1Hz to 50kHz	50:1	133dB/Octave Rolloff

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Circle No. 156 - For International

Cross-Compatible Encryption Software Guards PC Files

RSA SecurPC is an encryption technology for protecting valuable information assets stored in laptop and desktop computer files. Cross-compatibility enables users to exchange encrypted files across multiple platforms and transparently secure information throughout multinational enterprises. Operating systems supported include Windows 3.1x, Windows 95, Windows NT and Macintosh.

An Emergency Access file-recovery feature enables administrators to split emergency decryption authority among multiple authorities. The AutoCrypt feature enables files to be encrypted on-demand or automatically. A single file or an entire hard drive can be encrypted with a few mouse clicks.

With RSA SecurPC, users can exchange encrypted files by giving them the equivalent of a combination lock for a file's secret key. The user provides the combination or pass phrase to the person that needs to decrypt the file. SecurPC's self-extracting option allows secured files to be shared with persons not using the RSA SecurPC. Integrated into the host operating system, SecurPC appears as part of the Explorer in Windows 95, a part of the File Managers for Windows 3.1 and NT, and in the Finder on the Macintosh.

Trial versions of RSA SecurPC are available for free downloading to users worldwide from the company's web site at http://www.rsa.com. Pricing is $129 per unit in single copies. Site-license discounts are available. Upgrade pricing for current users is $39. ML

Security Dynamics Technologies Inc., *20 Crosby Dr., Bedford MA 01730; (617) 687-7000; fax (617) 687-7010; e-mail: info@secureid.com.* **CIRCLE 668**

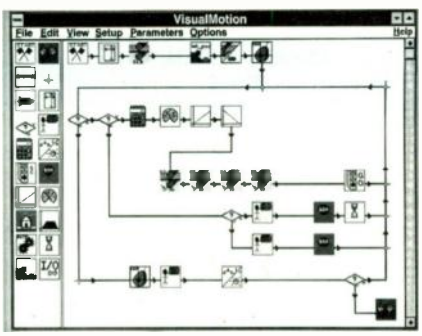
Developer's Kit Targets Embedded Software Designs

The C/C++ x86 SDK software developer's kit from Beacon Development Tools integrates the company's C/C++ x86 compiler with the SoftProbe Simulator/Debugger and Link&Locate 386 technologies of Systems & Software Inc. The SDK supports all x86 32-bit development efforts involving the Intel 386, 486, and Pentium processors, National Semiconductor's NS486 family, and AMD's embedded 386, 486, and ELN3xx families. Four different configurations are available for various tool-set requirements. The SDK can be used with other compilers from Microsoft, Borland, and Watcom. Beacon's customized version of the SoftProbe Simulator/Debugger provides an intuitive graphical front end for debugging embedded applications on the Beacon QED emulator. Link&Locate provides absolute linking, locating, and file building for the SDK. The SDK hosts on all WIN32 platforms. ML

Beacon Development Tools, *3307 Northland Dr., Ste. 270, Austin, TX 78731; (512) 454-6211 or 800-769-9143; fax (512)467-8960.* **CIRCLE 669**

Interface Simplifies Motion-Control Programming

VisualMotion 5.0 provides a graphical user interface for point-and-click programming, operation, and management of Indramat CLC multi-axis coordinated motion controls and digital drives. The programming environment includes easy Dynamic Data Exchange for real-time interfacing with



applications such as InTouch from Wonderware Software Development Corp. or Microsoft's Visual Basic programs. The interface runs on any IBM PC/AT-computer with Windows 3.1 or higher and 4 Mbytes of RAM. The user builds a motion-control sequence on-screen by clicking on applicable motion icons in a logical sequence. Each icon represents a step in the motion-control application.

VisualMotion 5.0 uses a serial communications link between the PC/AT and Indramat's CLC control to access all CLC configuration and operational programs and data. A single CLC control module simultaneously controls up to four independent tasks with up to 40 axes of coordinated or non-coordinated motions. VisualMotion 5.0 also allows access to drives on the fiber-optic-based SERCOS interface standard (IEC 1914) for real-time high-speed digital communication. ML

Indramat, *5150 Prairie Stone Pkwy., Hoffman Estates, IL 60192; (847) 645-3600; fax (847) 645-6201; Web: http://www.industry.net/indramat.*
CIRCLE 670

OS-9 RTOS Supports Wireless Communications

The Wireless OS-9 is aimed at pagers, cellular phones, personal digital assistants, industrial controllers, and other wireless communications devices. The basic OS-9 RTOS functions as a computer brain that resides in a communications device. It processes inputs and gives instructions to the rest of the device in real time. The wireless version adds new power-management, user-interface, and communication features to meet the requirements of wireless communications designs.

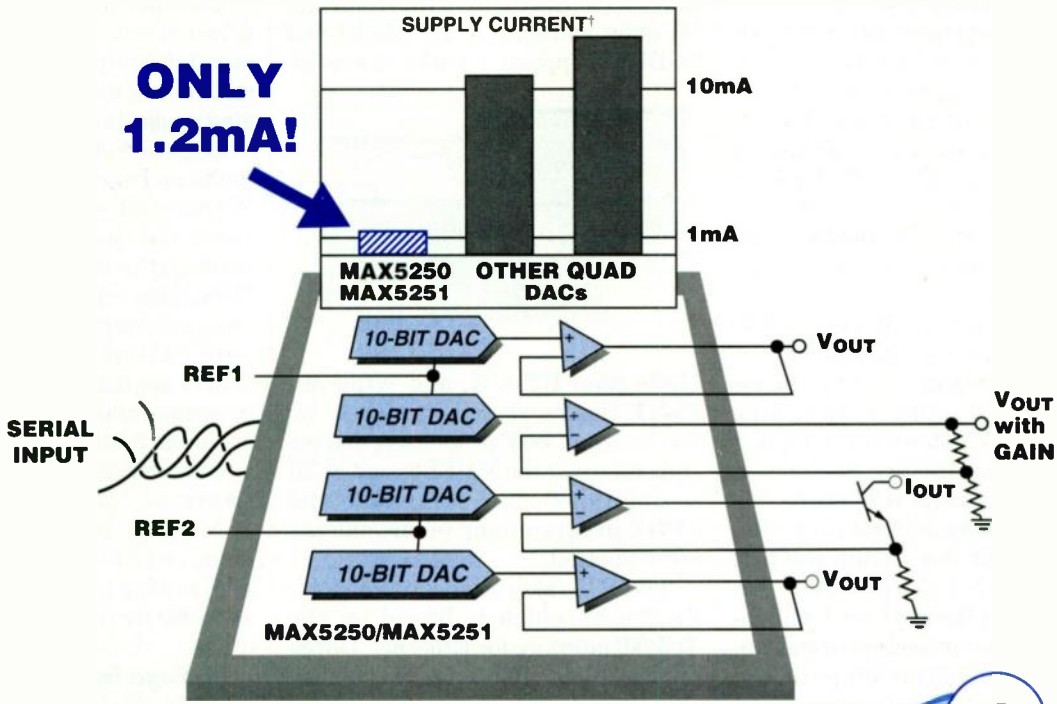
Wireless OS-9 can identify power parameters or network characteristics and communicate them to other components within the device to ensure correct response to existing conditions. It also features a set of tools that allows the manufacturer to create an appropriate user interface for these applications. Some may require only limited low-resolution black-and white graphics and a few input buttons. Others may require high-resolution color windowing and pen-based character recognition.

Microware's Multimedia Application User Interface (MAUI) offers multiple levels of application programming interfaces, such as keyboards, touch screens, and pens, as well as output devices like audio and visual displays. Wireless OS-9 supports various microprocessors, such as the Motorola 68K family, the PowerPC family, and the 32-bit X86 family, including the National Semiconductor NS486SXF. It also supports the TCP/IP and X.25 protocols. ML

Microware Systems Corp., *1900 N.W. 114th St., Des Moines, Iowa 50325; (515) 224-1929; fax: (515) 224-1352.* **CIRCLE 671**

10-BIT QUAD DACs CUT CURRENT BY 10x

3V and 5V DACs Use Less Than 300µA/DAC for Instrumentation and Communications



- Rail-to-Rail Outputs
- 20µs Settling Time
- Power-On Reset
- 20-Pin DIP/SSOP Packages
- 10µA Power-Down Mode
- +3V (MAX5251) and +5V (MAX5250) Operation

For lowest power 10-bit applications, select the +5V MAX5250 or the +3V MAX5251 quad DAC for your next design. These devices require less than 300µA/DAC, and feature power-on reset, rail-to-rail outputs, power-down, and direct access to the amplifier's inverting input (for varied output configurations).

† Supply current includes the external reference current for MAX5250/1.

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Finger-Image Access For Windows NT

Designed to prevent unauthorized access to sensitive data files, NRIdentity is a software solution that adds finger-image-based user authentication to the Windows NT password-based log-on process. To access a Windows NT-based workstation or network equipped with SAF/Windows NT, an authorized user enters a user ID, then places an index finger on an NRIdentity personal authentication desktop or keyboard scanner. The SAF/Windows NT then verifies the user's identity and automatically completes the log-on by delivering the user's password to the operating system.

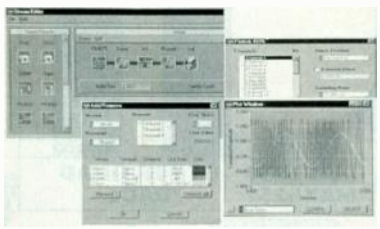
Users of non-SAF/Windows NT-equipped client workstations on a Windows NT network can continue to use password-based authentication. Also, users of SAF/Windows NT-equipped workstations can use password-based authentication to access Windows NT servers and domains that aren't secured by SAF/for Windows NT. SAF/Windows NT also provides a feature that locks the keyboard and obscures the monitor during a user's absence. A touch of the finger on the scanner unlocks the workstation. NRIdentity SAF/Windows NT requires MIcrosoft Windows NT (3.51 or higher) plus an appropriate version of Microsoft SQL Server (6.5 or higher). Pricing is $199 per workstation (excluding the fingertip scanner). ML

The National Registry Inc., *11831 30th Court North, St. Petersburg, FL 33716; (813) 573-3353; Web: http://www.nrid.com.* **CIRCLE 672**

Software Allows Real-Time Viewing Of Data Acquisition

A file-transfer language (FTL) developed by Pentek Inc. allows graphical viewing of data-acquisition operations in real time. FTL is a file-management system for VMEbus-based DSP and data-acquisition subsystems and includes software libraries for initializing, organizing, sorting, and retrieving data. Included is data-streaming support for single-channel or multichannel ADCs and DACs, SCSI disk and tape drives, local RAM disks, digital I/O, TMS320C40 comm ports, host workstation file systems, and all VMEbus devices.

The multitasking FTL has a GUI interface that automates the setup and control of the I/O interfaces for transparent operation to the application developer. Through GUI connections to a multistreaming shell, FTL supports National Instruments' LABWindows/CVI, Entropic Waves (Sun and HP only), and Math Works' Matlab and DaDisp. Supported workstations include Sun, HP-UX, and Windows 95/NT. Host workstations connect via the Internet, DSP processors, and peripherals over the VMEbus and SCSI storage devices. C-language and SPOX programming environments are supported.



The FTL also supports Pentek's Swiftnet, which is based on the TCP/IP interface for Ethernet. Development tools can be run on the host, while maintaining remote access to VME target systems. Including the GUI interface, pricing for the FTL starts at $5000 for Windows and Unix, and at $7000 for Unix. Delivery is 4 to 6 weeks. ML

Pentek Inc., *One Park Way, Upper Saddle River, NJ 07458-2311; (201) 818-5900, ext. 720; fax: (201) 818-5904; e-mail: news@pentek.com; Web: http://www.pentek.com.*
CIRCLE 673

Debuggers Target Windows Applications

BoundsChecker 4.0 is an automatic error-detection tool for Windows developers. This version is fully integrated into the Visual C++ debugger and supports the Borland Delphi 2.0 compiler and IDE. It can find errors in OLE components and ActiveX controls along with errors in executables and DDLs, API references, source code, and C/C++ callable modules — including third-party modules. System requirements include a PC-compatible Intel 386 system or above, Microsoft Windows 95 or NT 3.51, 16-MB RAM minimum, and 11-Mbyte disk space.

BoundsChecker 4.0 for Windows NT or 95 sells for $499 in the professional edition and for $299 in the standard edition. SoftICE is an advanced Windows NT debugger implemented as a kernel-mode component that can be installed as a boot driver, system driver, or automatic driver for on-demand debugging. It also can be installed as a manual driver for debugging applications or system-level code.

Because SoftICE handles processor faults and exceptions not handled by Windows NT system resources, such as video and console I/O, it can debug through the most difficult problems. Debugging capabilities include all system modules (boot drivers, system drivers, system services), Win32 and Win16 applications and DLLs, DOS programs and extender applications, and so on. System requirements include an Intel 386/486/Pentium single processor system, Microsoft Windows NT 3.51 or NT 4.0 Beta, 16-Mbyte RAM minimum, and 2.5-Mbyte disk space. SoftICE pricing is $699 for Windows NT and $999 for the Windows NT/95 bundle. ML

NuMega Technologies, *9 Townsend West, Nashua, NH 03063; (603) 889-2386.* **CIRCLE 674**

Tools Develop Device Drivers For Motorola Controllers

DriveWay 3DE (Device Driver Design Environment) technology consists of two tools that help to reduce device-driver development time, cost, and risk of embedded systems designs using the Motorola MPC 860 and MC68360 embedded microcontrollers. DriveWay-360 and DriveWay-MPC860 deliver a graphical representation of the microcontroller, whereby users can define the drivers and their functions using point-and-click selections. DriveWay 3DE then automatically constructs tailored, efficient, fully tested, and documented drivers. The tools also include on-line microcontroller data that helps users understand the structure of the microcontroller and how best to use its capabilities. Pricing for each tool starts at $33,000 for a one-year license. ML

Aisys Inc., *4633 Old Ironsides Dr., Suite 105, Santa Clara, CA 95054; (408) 327-8820.* **CIRCLE 675**

Scope, Meter Combo Makes Quick, Stable Measurements

The ScopeMeter 123 merges the functions of an oscilloscope, multimeter, and paperless recorder into a handheld instrument weighing 2.5 lbs. The instrument's "connect and view" capability allows users to move quickly from one

test point to another and always get a stable waveform without adjustments. A proprietary circuit continuously analyzes input signals and a microprocessor uses the information to control instrument settings. The two-channel unit displays scope waveforms and meter readings simultaneously. Users can access 26 measurement functions from a simple menu list.

The scope has a 20-MHz bandwidth, and the multimeter is a true-RMS, dual-channel 5000-count meter with 0.5% accuracy. Two screen images and 10 user setups can be stored in nonvolatile memory. An RS-232 interface allows downloading of measurements to a PC or printer. Flexible test leads are shielded against noise pickup and can be used for both scope and meter measurements. A backlit LCD screen has three brightness levels. The highest is used when the unit is ac-powered. Two levels are available in battery operation, with the NiCd batteries lasting up to five hours between charges. The ScopeMeter 123 costs $995. JN

***Fluke Corp.**, P.O. Box 9090, Everett, WA 98206; (800) 443-5853; fax (800) 358-5332; e-mail: fluke-info@tc.fluke.com; http://www.fluke.com.*

***Fluke Europe B.V.**, P.O. Box 1186; Eindhoven, The Netherlands; +31 (40) 644-200; fax +31 (40) 644-222.*

CIRCLE 676

Modules Let Programmers Handle Many Applications

Users can configure the XPRO LC device programmer for almost any application, including research and development, production, or field service. Interchangeable hardware modules for the unit's base allow it to support both generic (EE/EPROM single or gang programming in DIP or PLCC), and device-specific applications. A PAL/GAL module is available with both DIP and PLCC sockets. Other modules support Altera MAX, Microchip PIC (single or gang), Motorola 68hcxxx, and Xilinx XEPLD devices. The base unit measures 5 by 11 by 3 in. and weighs 3 lbs. The XPRO LC base unit costs $495. JN

***Logical Devices Inc.**, 130 Capital Dr., Golden, CO 80401; (800) 315-7766; Web: ttp://www.logicaldevices.com.*

CIRCLE 677

PC-Based Instruments Offer Standalone-Type Performance

The DAQ family of PCI-, ISA-, and PCMCIA-based instruments give PCs the capabilities associated with standalone instrumentation. The first six products in the family are the DAQScope (in PCI, ISA, and PCMCIA versions), the DAQMeter (PCMCIA), and the DAQArb (PCI and ISA versions). The DAQScope features two channels, 20-Msample/s sampling, a 15-MHz input bandwidth, 8-bit vertical resolution, and a 662-ksample memory. Random interleaved sampling allows repetitive sampling of recurring waveforms.

The DAQMeter is a 5-1/2-digit true-RMS (20 Hz to 25 kHz) digital multimeter that takes up to 60 readings per second. Ranges include 20 mV to 250 V dc and ac, and resistance from 200 Ω to 20 MΩ. A separate shunt module is available for current measurements. The DAQArb offers one channel with 40-Msample/s sustained waveform generation. It features 12-bit vertical resolution, 2 Msamples (expandable to 8 Msamples) of waveform memory, and 32-bit direct digital synthesis for generation of frequencies to 16 MHz. Waveform linking and looping help create longer and more complex waveforms.

All of the instruments come with probes and software needed for immediate use. The DAQScope for the PCI bus (PCI-5102) and PCMCIA slot (DAQCard-5102) cost $1195. The ISA version (AT-5102) is $995. The DAQMeter goes for $695. The DAQArb costs $2995 for both the PCI (PCI-5411) and ISA (AT-5411) versions. JN

***National Instruments Corp.**, 6504 Bridge Point Pkwy., Austin, TX 78730-5039; (800) 258-7022; (512) 794-0100; fax (512) 794-8411*

e-mail:info@natinst.com

Internet: http://www.natinst.com.

CIRCLE 678

PCI-based A-D Board Captures Data At 500 Msamples/s

The CompuScope 8500/PCI is a PCIbus-compatible analog-to-digital card that samples at up to 500 Msamples/s with 8-bit resolution. The card comes with software that allows users to operate it like an oscilloscope with no further programming required. The Flash analog-to-digital chips used for the sampling provide a 45-dB signal-to-noise ratio and a 250-MHz bandwidth. At sampling rates up to 100 Msamples/s, the card uses bus mastering to take advantage of the PCI bus' fast transfer rates to write data directly to the host PC's DRAM. An onboard high-speed FIFO memory allows the card to stream data to the PC even during bus latencies. At rates to 500 Msamples/s, the unit stores samples in on-board memory of up to 2 Mbytes.

The CompuScope 8500/PCI-128K costs $6995. Software drivers for DOS, QNX, Windows 3.1, Windows 95, and Windows NT cost $250 each. LabVIEW, LabWindows CVI, and HP VEE drivers also cost $250 each. JN

***Gage Applied Sciences (U.S.) Inc.**, 1233 Shelburne Rd., South Burlington, VT 05403; (800) 567-4243 or (514) 337-6893; fax (514) 337-8411;*

kmccurry@gage-applied.com;

http://www.gage-applied.com

CIRCLE 679

Real-Time Kernel Supports DEC Processor Family

A new version of the C Executive real-time kernel from JMI Software now supports the StrongARM processor developed by Digital Equipment Corp. C Executive is a ROMable, multitasking operating system kernel for real-time embedded systems that offers a complete execution environment for applications written in the C language. An optional file system, called CE-DOSFILE, replicates the PC/DOS file structure on external media. Thus, StrongARM-based systems can read and write PC/DPS diskettes and hard disks. The file system provides contiguous files for use in high-performance data-acquisition applications.

Other features include CE-VIEW, which is a system-level debugging tool for testing on the target system; the optional CE-TCP TCP/IP communications package; and CE-SNMP, which adds SNMP support. JMI also will offer a StrongARM version of PSX as an extension to C Executive. PSX provides a 60% subset of POSIX.1 calls to ensure a smooth migration path from C Executive to full POSIX compliance. The initial C Executive and PSX release supports the StrongARM SA-110 on Digital's EBSA-110 evaluation board. The board supports SA-110 processors running in the range of 88.3 to 287 MHz. The development package for C Executive costs $2500, and $3750 for the PSX. ML

JMI Software Systems Inc., 904 Sheble Lane, P.O. Box 481, Spring House, PA 19477; (215) 628-0840; fax: (215) 628-0353; e-mail: inquiries@jmi.com.
CIRCLE 680

Development Tool Supports Data Acquisition

DAPtools OCX developed by Microstar Laboratories is a tool for developers using Visual Basic 4.0 (32-bit) or Delphi 2.0 under the Windows 95 and Windows NT operating systems. DAPtools OCX includes the DAP OCX to interface with the company's a-Series and e-Series data-acquisition processor boards. Also included is on-line reference documentation for both the DAP OCX and DAPL, the operating system that runs on DAP boards. DAP boards have on-board intelligence implemented as DAPL, a multitasking real-time operating system for high-performance real-time data acquisition and control applications on a PC. Boards containing 486 processors are shipped with DAPL 2000, a 32-bit implementation of DAPL. DAPL runs a data-acquisition application on a DAP, free from any delays imposed by Windows NT, Windows 95, or other programs. Prices for 486-based DAP models start at $2195, including DAPL 2000. DAPtools OCX costs $95. Using DAPtools OCX under Windows NT requires Accel32, the DAP driver for the Windows NT OS, which costs $95. ML

Microstar Laboratories Inc., 2265 116th Ave. N.E., Bellevue, WA 98004; (206) 453-2345; fax: (206) 453-3199.
CIRCLE 681

Software Tools Perform Waveform Analysis

Windaq Playback Software for Windows is a PC-based waveform recorder that provides real-time data acquisition for reviewing and analyzing captured waveforms without leaving the Windows programming environment. The Windaq/EX option adds a variety of frequency analysis, digital filtering, and statistical analysis capabilities to those of the standard Windaq package. These include X-Y plotting for examining the relationship between two channels by designating one as the independent (X-axis) variable and the other as the dependent (Y-axis) variable. Once plotted, analysis features such as X-Y excursions and instantaneous rate of change are possible.

Another feature sends waveform data from a selected channel to a DAC on Dataq's DI-200 series hardware. This allows waveform data from disk to be played back on an analog device such as a speaker or chart recorder, or to be processed externally. Windaq also has a data-import translator for National Instruments' LabVIEW waveform data files. The translator converts LabVIEW waveform data for display and analysis in Windaq. Other data-import translators supported include: any spreadsheets (CSV), ASYST, DADiSP, and others. ML

Dataq Instruments Inc., 150 Springside Dr., Suite B220, Akron, OH 44333; (330) 668-1444; fax: (330) 666-5434.
CIRCLE 682

Development Tools Support MIPS And Tiny RISC

The GNUPro software-development tools are now available for the MIPS16 instruction set architecture from MIPS Technology and LSI Logic's 16/32-bit TinyRISC microprocessor. These tools will allow users to develop C and C++ applications optimized for the TR4001 TinyRISC MPU. The GNUPro port to the TinyRISC MPU will originate from the same single-source tree as the platforms currently distributed by Cygnus Support, providing a smooth migration path for products making the transition to the TinyRISC MPU. The GNUPro toolset consists of the GNU C/C++ compilers, remote source-level debugger with GUI, macroassembler, linker/loader, libraries, binary-file utilities, and instruction set simulator. ML

Cygnus Support, 1937 Landings Dr., Mountain View, CA 94043; (415) 903-1400. **CIRCLE 683**

Interface Allows Two-Wire Debugging For 8051s

The TIU-51 S-tag Target Interface Unit from Signum Systems is a two-wire debugging interface for connecting 8051 microcontroller-based embedded systems to the company's debugging, testing, and prototyping tools. It provides an RS-232 connection to the host PC running the development tools and an S-tag connection to the embedded system being developed. Using the interface requires just two pins (one input and one input/output) and a small monitor. The RISM monitor is provided in 8051 source-code form for linking with the rest of the user's application. S-tag doesn't impose any timing requirements on the target system and has zero CPU usage when idle.

The TIU-51 allows systems without a spare communications device (UART) for debugging purposes to be easily connected to any RISM-compatible debugger. It also can act as a logic-level converter for systems with a spare UART but without the necessary RS-232 interface logic. TIU-51 is priced at $250. ML

Signum Systems, 11992 Challenger Court, Moorpark, CA 93021; (805) 523-9774; fax (805) 523-9776.
CIRCLE 684

Cool Products Heat Up Thermal-Solution Catalog

Temperature-control products needed in varying degrees of cooling applications are detailed in Lytron Inc.'s (Woburn, Mass.) latest catalog *1997 Total Thermal Solutions*. The 52-page book provides specs, performance data, and selection guidelines. Among the products focused on are recirculating chillers, ambient cooling systems, copper and stainless-steel heat exchangers, oil coolers, and cold plates. Featured new products include low-cost OEM coils specially designed for large-volume OEM applications, and a selection of compact, brazed-plate liquid to liquid heat exchangers. Call (617) 933-7300. RE

CIRCLE 504

Fox Trots Out Frequency-Control Product Guide

Quartz crystals, clock oscillators, temperature- and voltage-controlled crystal oscillators, real-time clock modules, and crystal filters are all covered in a new technical catalog from Fox Electronics, Sellersville, Pa. Included within its 84 pages is technical and application information on a broad range of pin-through and surface-mount components. The technical section also provides design notes on, and theories of, operation for both crystals and oscillators. For a copy of *Fox Frequency Control Products, Vol. 17*, call 1 (888) GET-2-FOX; fax: (941) 693-1554; Web: http://www.foxonline.com. RE

CIRCLE 505

It's Not About A Circus, But Rings And Seals Get Spotlight

Miniature O-rings and seals are the main attraction in Apple Rubber Products' (Lancaster, N.Y.) latest brochure. Called MicrOring seals, they are defined as any O-ring less than 1 mm in either inside diameter or cross section. More than 2000 sizes are available, down to 0.008 in (0.20 mm), which is the smallest O-ring around. Important considerations for selecting microminiature O-rings, such as groove design, along with a comprehensive size chart, are included. For more information, call 1 (800) 828-7745; fax (716) 684-8302; e-mail info@applerubber.com. RE

CIRCLE 506

SmartLink Modules Measured Up In New Catalog

SmartLink measurement modules are highlighted in the new *Network Measurements Catalog* from Keithley Instruments Inc., Cleveland, Ohio. Its 52 pages offer details on the modules, application examples, a module selection guide, tutorial information, and an OEM developers section for incorporating the modules into a company's own products. The tiny (1 by 1.25 by 6.5 in.) modules allow laboratory-grade measurements anywhere: to a remote PC or controller, or display/store results for local monitoring. If you'd like the catalog, call (800) 552-1115 or (216) 248-0400; fax (216) 248-6168. RE

CIRCLE 507

Databook Jogs Memory Products Into The Mainstream

White Microelectronics, Phoenix, Ariz., which is known for producing military memory products, has published its first *Commercial Data Book*. The book includes data sheets for SRAM, flash, DRAM plastic MCMs, and upscreened plastic encapsulated microcircuits (PEMs) among its 268 pages. The modules are based on various JEDEC standard technologies, such as PLCC, ZIP, and SIMM. Also discussed is the company's Plastic Plus selection. With this concept, the company procures commercial off-the-shelf PEMs and upgrades them using military qualification and test methods. Call (602) 437-1520; fax (602) 437-9120. RE

CIRCLE 508

Everything You Need To Know About PLCs But Were Afraid...

The second comprehensive edition of *Programmable Controllers: Theory and Implementation* from Industrial Text and Video Co., Marietta, Ga., contains over 1000 pages on PLCs and process control-related issues. First, the fundamentals are explored; then there's in-depth discussions of advanced PLC topics and applications. Each chapter contains updated information relevant to current technology and five new chapters about recent technology developments, some of which have never before been explained in print, were added. For more details, call 1 (800) 752-8398; fax (770) 240-2209. RE

CIRCLE 509

Operator-Interface Products Brochure Shifts Into High Gear

Easy-to-use operator-interface products for the automotive industry are featured in a new brochure from Total Control Products Inc., Melrose Park, Ill. Multilevel products include: Level 0: thumbwheels, panel displays, etc.; Level 1: QuickMarquee Message Centers and Workstations, etc.; Level 2: QuickPanel operator interfaces, etc.; and Level 3: TCS industrial computers, etc. Company history as well as worldwide technical and sales support are outlined. To get the brochure, call 1 (800) THINKOI, or fax (708) 345-5670. RE

CIRCLE 510

CD-ROM Contains Proceedings Of SEAM '95 Conference

The MacSciTech Users Association, Worcester, Mass., announced the publication of the CD-ROM proceedings from the group's third technical symposium "Scientific & Engineering Applications of the Macintosh" (SEAM'95). All abstracts and most of the proceedings from the San Francisco, Calif. conference are jammed into the package. There's also a number of commercial demonstration packages on the disk, such as the math software Maple V from Waterloo Maple and KaleidaGraph graphing software from Synergy Software. Movie shorts of various presentations include the keynote speaker Adam Engst. The CD-ROM costs $59 for MacSciTech members, and $89 for non-members. Call (508) 755-5242; fax (508) 795-1636. RE

CIRCLE 511

The Patent Question

As one involved in the patent system for many years as an inventor, I found your Mar. 3 EE Currents and Careers article *("If You Have A Brainstorm, Get A Patent Attorney," p. 201)* to be a fine contribution to the average engineer's understanding of the subject. I do, however, have a few observations which might be of interest. The second paragraph contains errors of fact and implication. The term is now 20 years from date of issue as opposed to the stated 17 years. A patent is in effect a chattel deed to a wasting asset with the meets and bounds defined in the claims. At the time of expiration, the invention is no longer property, but only a public record for general research or free use.

Under the heading of "the four basic parts", the gratuitous "it is not uncommon for some or all of the claims to be rejected on the first action by the examiner: relatively few applications are filed" is an interesting quotation. I have never heard of any case where all claims were not rejected on first examination.

I found the numbers cited particularly interesting some 2200 examiners and 170,000 applications per year reduces to 77 applications per examiner per year. What do the other 2200 employees do? In most cases, a thorough search of the patent office records without the use of the facilities available only to patent office employees takes an experienced searcher less than eight hours average including generation of an analysis and written report. Where does the rest of the time (paid for not by the taxpayers but by the applicants) go? Could it be possible that more "service" isn't what we need?

The recent and currently proposed changes in our patent system are without exception bad for the future of our republic. The huge increases in filing fees to make the patent office "self supporting," rejection of all claims at first office action, early publication, maintenance fees, and most egregious of all, the concept of reexamination by request, are examples of bad rules and laws. When the costs rise to the current heights (to enrich lawyers and fatten the treasury), the small, independent inventor is denied his Constitutional rights if he or she can not buy them at an outrageous price.

Richard K. Snook
President, RR Technology Development Inc.
Tucson, Ariz.

Ol' Reliability

In the VENN diagram on the workstation display on the cover of the Mar. 3 issue, you've listed Delay, EMI, Manufacturing, Thermal, and Routability. Whatever happened to Reliability? Isn't that one of the big plusses of concurrent engineering and development on the screen?

John Peter Rooney
jprooney@foxboro.com

Thanks For The Memory Cells

Your article in the April 1 issue on single-electron MOS transistors *("Single-Electron MOS Transistor Holds Promise For A Tiny Memory Cell," p. 29)* was very interesting. I'm currently responsible for all memory qualification (DRAM, SRAM, EEPROM, FLASH, etc.) at AG Communications Systems.

There are a few comments I'd like to make. First, based on this technology, it appears that a very large memory matrix would be possible. If so, from a practicality standpoint, the time to program/define the matrix, based on your gate pulse of 10 ms, would be extremely long. To reduce this time, as you know, you could either reduce the tunnel oxide thickness or increase the size of the channel width. However, with a reduction in oxide thickness, you can run the risk of punch through. And of course, increasing the size of the channel width takes away from your overall cell size.

Secondly, have you considered the effects of Alpha particles on the memory cell? Current packaging technologies and purity of materials may enter greatly into the reliability of this new memory cell. I would recommend you look into the construction techniques of DRAM cells for some ideas on how to make your cell more resistant to Alpha particles. Typically, you do not see these types of problems with floating gate cells. However, since the scale of your design is so small, I would recommend that you take these types of issues into account!

One more point: I know the type of issues I have discussed here are related to commercial products with respect to continued and consistent operation, parameters, and reliability. However, I feel that if these types of issues are not kept in mind, even though new research seems promising, it could only delay the eventual introduction of such new discoveries into the marketplace.

David Giammarrusco
giammard@agcs.com

What Do The People Know?

It seems to me that public perception plays little if any role in the professional well-being of U.S. engineers, the majority of whom are salaried engineers. The employers, the supply/demand ratio, and the engineers' skill levels determine the status of engineers.

I would be just as happy if the public thought little of me, just as long as the boss showed appreciation for my talent. And for the self-employed engineer, the public also plays little part in his/her well-being. It is the clients whose perceptions matter.

I happen to be a Senior Member of the IEEE and am active in its professional programs. For the IEEE to expend more than a cursory effort in polishing our image to the public would be, I think, a waste of scarce IEEE funding. So whether or not the IEEE is in the best position to influence public perception of the profession is beside the point.

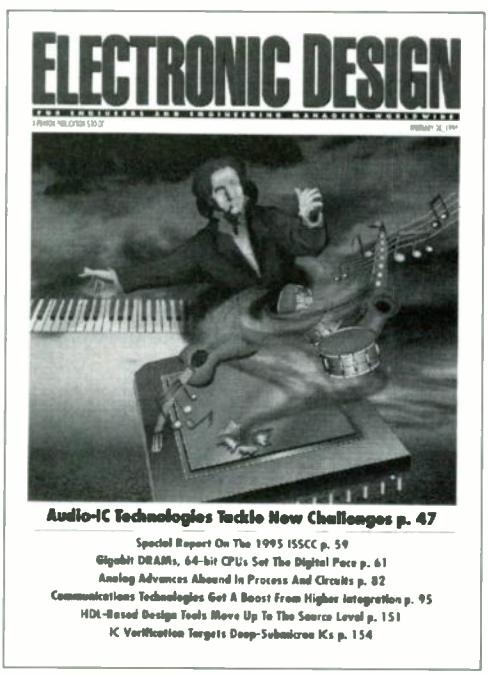
My image to the public will be enhanced when I drive my BMW 740 into my four-car garage next to my five-bedroom house in Great Neck Estates. Since this is not likely, given the strong industry control over wages, I have to settle for more modest circumstances. And there is little the IEEE or public opinion can do about this.

Robert Bruce
r.n.bruce@ieee.org

Readers are encouraged to send their letters and comments to: Letters Editor, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604; fax (201) 393-0204; e-mail: mikemea@class.org.

STRATEGIC PARTNERS WORKING TOGETHER

Information has always been a part of the developmental strategy needed for success in the OEM market. In today's fast-paced, competitive global market environment, technology information has become a priority. Systems designers not only want to know what their strategic supply partners are doing today, but where they're going. Designers and suppliers must now work in tandem to align enabling technology with the customer's system requirements. These strategies demand strong partnerships in the development of competitive products.



A third strategic partner completes this alliance. This partner's mission is to observe and report today's product availability by its editorial staff of respected experts, while constantly probing for the next generation of enabling technology. The constant flow of exclusive and vital information helps to bring systems designers and suppliers together as strategic partners. It also provides engineers and engineering managers with an enhanced ability to bring more competitive products to market, faster.

Electronic Design is that strategic information partner — a partner who provides the information that helps the systems designer make those critical decisions that stay the course of the technology road map.

Your Strategic Information Partner.

ELECTRONIC DESIGN

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Exploring employment and professional issues of concern to electronic engineers

Contract Engineering Offers Alternate Employment Path

Richard F. Tax

Employment opportunities for engineers can be quite tenuous, what with corporate mergers and buyouts, plant closings, the ebb and flow of military contracts, technology changes, the number of new engineering graduates and other market forces. In fact, according to the Deutsch, Shea & Evans High Technology Recruitment Index that tracks supply and demand for engineers, over a 30-year period between 1960 and 1990, only 22% of the time was there enough room for new engineers in the market without displacing older ones. As a result, there's a good chance that at some point in an engineer's career, he or she will be out of work and looking for a way to earn a living, preferably in the same technical or engineering capacity.

One route back to employment is through contract engineering, a relatively new term for what used to be called "job shopping." Other than being a direct or permanent employee of a company, contract engineering is a way that engineers can market their services. Actually, the idea of a permanent employee also is becoming passé, because there is little that is permanent in today's multifaceted, ever-changing workplace. With the steady influx of engineering graduates into the market, older, more experienced engineers often find themselves displaced out of permanent or direct employment.

Contract engineering is a three-party arrangement between you, the contract engineer (CE), a contract house (CH) or job shop, and the client company (CC). The CC can be any company—aerospace, military, auto manufacturer, medical, computer, consumer, etc.—that has need for temporary help and hires CEs to fill a short-term need. In simple terms, the CC needs manpower and calls a CH who, in turn, contacts a CE that has the experience and background that the CC requires.

You as a CE are hired as a direct employee of the CH, who then leases you out to its client. Your work is almost always performed on-site at the location of the client. And your skills are purchased by the CC from the CH for a specific hourly price and for a specified period of time. Keep in mind that the employment or purchase order can be terminated at any time for almost any reason, and your employment can be either extended or terminated just as quickly. Although the CC is not your direct employer, they are the ones you must satisfy since they control your longevity at the company and job assignment.

Is It Right For You?

Some engineers are forced into contract engineering because of a layoff, age discrimination, or various employment conditions. Others believe that working as a direct employee conveys a false sense of job security in an era in which technological, economical, and social forces make the future uncertain.

On the other hand, contract engineering is sometimes a vehicle for getting a position as a direct employee. If you prove valuable to the client, they may opt to hire you as a direct employee and keep your skills.

Contract engineering as a career is not for every engineer, but one should be aware of its pros and cons and how it can pay the bills when times are difficult. Engineers who have developed very marketable design specialties have spent most of their careers as CEs, and the type and level of skill plays a role in one's success. However, there are down times when there is no work, no matter how great the skills Some CEs wind up unemployed a significant amount of the time, so a legitimate question to ask yourself is whether you could stand a year out of work living on unemployment insurance and savings.

The Nuts And Bolts

Contract engineering is an honest way to make a living. When you work, you get paid for every hour, including overtime (there are no free lunches for anyone in the business). The contract house makes money on every hour that you work, so overtime work must be paid or the CH loses their percentage. Your relationship with other engineers on the job is important, and working for nothing deprives another engineer of an opportunity. You will be working with other CEs and direct employees. Note: Not every person you will be working with is an engineer, so you must be able to strike a balance, and set an example for a pro-

Contract Engineering: Definitions and Pay Structure

Direct Labor Rate (DLR) : An engineer's gross pay.

Billing Rate (BR) : The gross amount the contract house bills the client.

BR = DLR + profit + overhead + expenses

BR = DLR (1 + x) or BR = DLR (1 + 0.35) or 35 cents on the dollar.

Overtime: Depends on individual state labor laws and usually paid at the time-and-a-half rate.

fessional and friendly relationship.

You most likely will never meet the personnel at the CH, and may only speak with them by phone to keep them informed about your weekly time card. However, they play an important role in your success by searching for a position for you. This third-party arrangement is important since their assistance and contacts will help you to obtain employment, and they are motivated to do so by profit. There is nothing better than having others recommend you for a position, and they may know about a job around the corner that you will never hear about. The CH also will call you about out-of-town opportunities if you let them know that you are willing to travel. A key point to remember: The CH provides the service for and is obligated to the client company and not to you. You only benefit because the CH needs something to sell—you are the commodity.

If you are willing to travel, you have a better opportunity to select the type of work that will continue to enhance your skill level and keep you current. In addition, age is never a problem. Experience usually comes with age and the more useful experience you have, the more valuable you will be to the client. CCs look for engineers who have done, in the past, exactly what they wish them to do in the present.

Once you leave state-of-the-art engineering design, your future as a CE will begin to decline. This can happen when there is an oversupply of engineers and fewer opportunities to enhance one's skill level. However, even if you don't feel especially strong in a specific field, you may still find employment as a CE in an engineering support role. Speak with a CH representative about different types of opportunities.

Pay for CE's working at the same CC location can vary by a factor of 2:1, with the unknowing or new CE being the victim. So, the more engineers know, the higher the hourly pay rate will be. Like any employment situation, supply and demand is the driving force behind compensation, with today's hourly rate creeping back to the rates of the mid-1980's, or roughly $40/hour and a no-benefit package for degreed engineers. Some engineers at the moment are getting half this figure. Currently, RF and software engineers are getting much more.

In the three-party situation of contract engineering , two labor rates are involved: The Billing Rate (BR) that the contract house charges the client company, and the Direct Labor Rate (DLR) that the house pays the engineer. There are a few variables in these numbers, such as benefits, which may complicate the issue, but these can be tabled to simplify things.

The delta or difference between the BR and the DLR is a variable, and since it includes overhead, business expense, and profit, it is something the CH will maximize, even at a cost to the engineer. Billing rates will vary from a low of 1.1x DLR to 2xDLR, with 1.35xDLR being a fair number, with vacation and holiday pay included. A rate of 1.25xDLR is reasonable for a no-benefit package. Your goal is to get the DLR up and keep the delta at a reasonable level *(see the table)*.

To keep things simple, a DLR of $40/Hr. is approximately $80,000 per year, or $40 x 2000 hours/year. This sounds like a pretty reasonable salary until you subtract the cost of health insurance, benefits, pension, and down time.

Down time is the period between jobs when you have zero income or just unemployment insurance to live on. When you stay on a job to the end, you can expect a period of unemployment or down time before landing a new assignment. Down time varies due to supply and demand and your marketable skills. It's best to be prepared by keeping your resume up-to-date and sending it out to as many contract houses as possible to improve your opportunities. You shouldn't depend on one CH for your livelihood. The only sure way to eliminate down time is to get a new assignment before completing the old one. Some engineers have a nose for this and seem to pick up a new assignment just as the old one terminates. These are the most successful contract engineers.

Playing The Game

Let's take a look at how an engineer can start, or at least sample, the experience of contract engineering. Initially, you must get your resume out to as many contract houses as possible. Get the names, addresses, and telephone numbers of contract houses from advertisements, other engineers, and publications. One source of contract houses is Contract Employment Weekly, published by C.E. Publications Inc., P.O. Box 97000, Kirkland, WA 98083; (206) 823-2222; e-mail: publisher@ceweekly.com. This should get a new CE off to a good start.

Your computer, word processor, and fax/modem will enhance your effort to get the message to the contract houses. Their fax machines are on 24 hours a day, so you can cut costs by sending out your resume when telephone rates are lowest. Keep a log to record all of your efforts and contacts by date. Keep a record of all CH's, contacts, and names of people you speak to, and especially the members of the CC that you speak to during telephone interviews. Once your resume is in the hands of the CH, you should follow-up with weekly telephone calls to keep CH personnel aware that you are available and interested. If you don't have one, get an answering machine and keep your telephone line open for important calls. If family members answer the phone, make sure they know how to take a message since it may be

The AEA—A Voice For Engineers

The American Engineering Association Inc. (AEA), based in Fort Worth, Texas, is a strong advocate for advancing the professional and economic agenda of US engineers. The AEA is involved in many of the issues described in the accompanying article: employer-employee relations, salaries, unpaid overtime, loss of jobs, layoffs, and many others that affect the lives and welfare of engineers. For information on how to learn of their work, or how to become a member, contact them at P.O. Box 820473, Fort Worth, TX 76182-0473; (817)656-2324; Internet: http://www.aea.com. E-mail: aea@aea.org.

about your next assignment.

Assuming you did your homework and prepared a good resume, you should begin receiving calls from CH personnel. Initial negotiations will begin when a CH representative calls you about a job or just an introduction. The conversation will start with your availability and the requirements the client needs filled. Tell them what you have done and know what is on your resume. Keep the conversation friendly and maintain a positive attitude. Don't mention what you don't do and don't voluntarily disqualify yourself. Your goal is to get the interview and the assignment. Remember, the CH representative wants to get you an assignment, so they will make their money.

Next, they will bring up the rate of pay. How much will you accept? If you don't know, ask them what the company is paying their other people with similar skills, education, and experience. Forty dollars per hour is quite reasonable for engineers today and higher for specialists and software people. It is most important here to know what is going on, so keep informed by speaking with your friends and associates about the job market and rates at different companies. You are not locked into a DLR until after your interview with the CC and you go to contract with the CH.

Once completing the initial interview and negotiations with the CH representative, and assuming a match can be made between skill, DLR, and availability, the CE will be introduced to the client company for their interview. The CC representative (usually the staffer you will be working with) will have reviewed your resume and made a preliminary evaluation of your qualifications. The CC/CE interview is just one more step in the hiring process and getting this far is a plus. A discussion on interviews is another subject. But, try to talk about the actual work and how you can contribute to the project. Terms and fees are not discussed with the CC representatives. That is the function of the CH.

Assuming the interview was successful, the process continues with an agreement between you and the CH on the particulars of the contract, i.e., starting date, DLR, overtime rate, per diem, and benefits. You will receive a package and contract from the CH by overnight mail to lock things up.

With regards to overtime, contract engineers do not work without being paid. Overtime pay is agreed upon before the assignment begins. Overtime is controlled by state labor laws that specify time-and-a-half for hourly workers. Since you are paid on an hourly basis, you should be getting the time-and-one-half rate. CE's should check with the state Wage and Hour Bureau to determine how overtime is paid and who is qualified to receive it.

Per diem (PD) is money paid for living expenses when one is on a temporary assignment away from home that usually lasts for less than one year. Per diem for contract engineers is much different than it is for direct employed engineers. Normally, direct engineers receive an expense package when the company sends them on assignment out of town. This package will cover travel to the location plus complete coverage of meals and lodging expenses. Per diem for CE's is rare due to fact that enough engineers are willing to work without it to the detriment of the whole engineering community.

When a contract engineer takes a job out of town (i.e., 100 miles from home), one might expect the CC and CH to pay the business expenses or per diem. However, it is extremely rare for company-provided per diem for CE's to exceed $15 per day, even when government employees were getting more than $100 per day at the same location—another symptom of an oversupply of engineers.

To ease the pain, contract houses will break out a portion of your pay check, if you qualify, for PD and pay you the Federal Recommended Rate for the geographic location of the company. This is taken off the top of your pay check and not taxed. Government Publications 463 and 1542 cover travel expenses and per diem rates for different parts of the country. (You can get these publications from the Internet at http.//www.irs.ustreas.gov.) You may have to justify expenses at the end of the year, so be careful and accurate. Some contract houses try to base your overtime rate on your base pay less the specified PD rate. You shouldn't tolerate this and get some advice when you need it.

Although not as significant as PD, vacation/holiday pay is still about 6 % of your gross. Just be aware that it may be available and negotiate for it when you can. Again, this also will depend on the individual and the demand for his or her skills.

The contract you sign is an agreement between you and the contract house alone. It is an agreement between two parties but, it also is influenced by law. Preliminary verbal agreements will precede the contract and, as mentioned, may begin as early as your first contact with the CH. Usually, the hourly pay rate is suggested prior to an interview with the CC, but is not tied down until the contract is signed. Try to delay the signing of any contracts between the contract house and yourself until you feel confident and satisfied. You can usually wait until the day or week you start the assignment.

The contract will specify your DLR, overtime rate, vacation, holiday, benefits, per diem, and some other clauses that may try to deprive you of opportunities. When you are not sure about something, ask and find out more. If you don't like a specific clause, cross it out and initial the change. The contract also will include a Patent Agreement that you *should not* sign. The client company will want you to sign their Patent Agreement, and you cannot assign your patent rights to both parties.

One of the best ways to help engineers is to keep them informed. Knowing the job market, pay, benefit packages, and where to market their skills will enhance their income *(see "The AEA—A Voice For Engineers, p. 158).* In the long run, this will help raise rates across the nation. It is essential that engineers remain productive, get what they are worth, and have the opportunity to enhance their skills through the practice of their profession.

Richard Tax has worked as a contract engineer for 20 years and is currently vice-president of the American Engineering Association, a professional organization dedicated to the enhancement of the engineering profession and American engineering capabilities.

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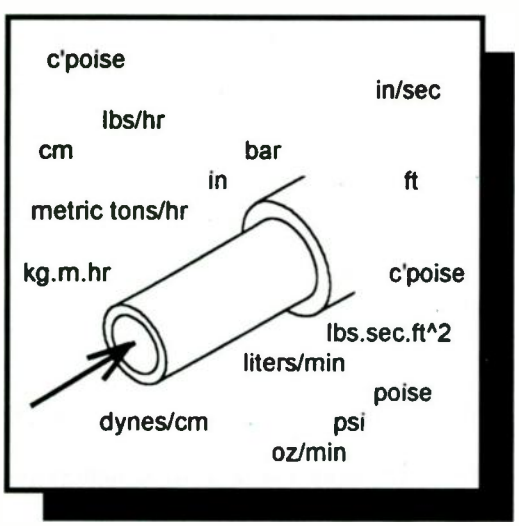

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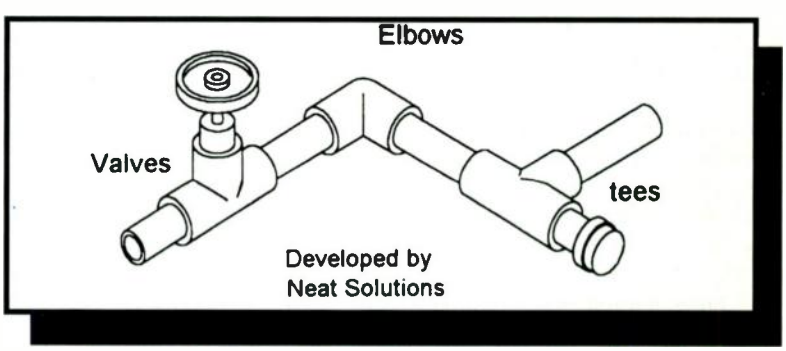

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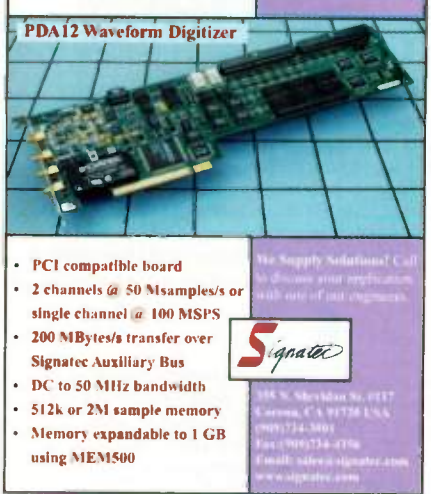

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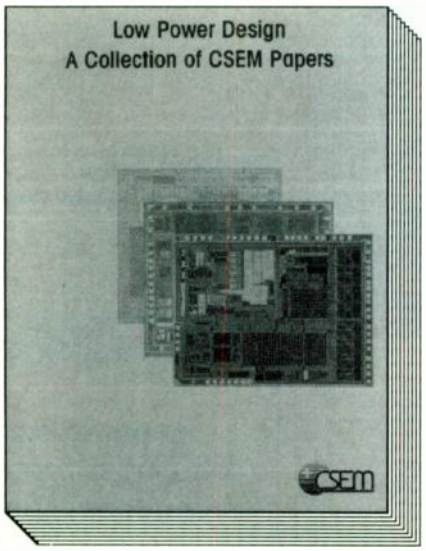

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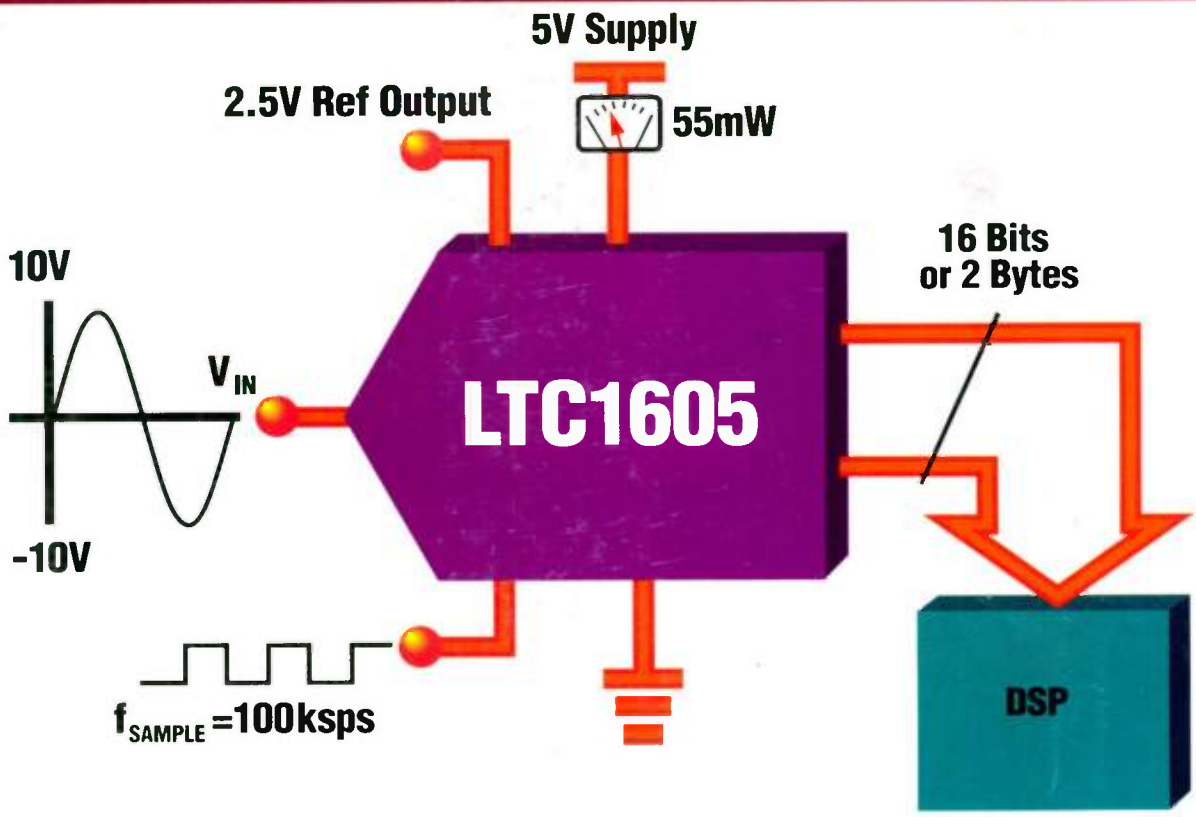

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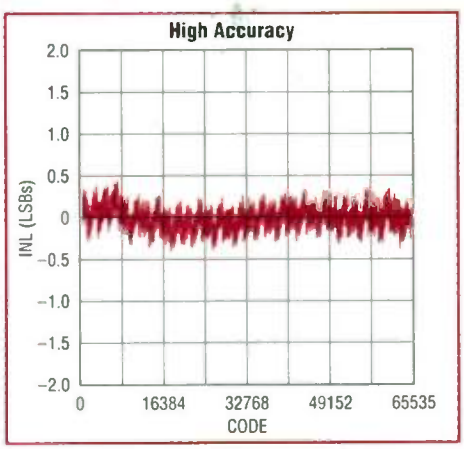

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