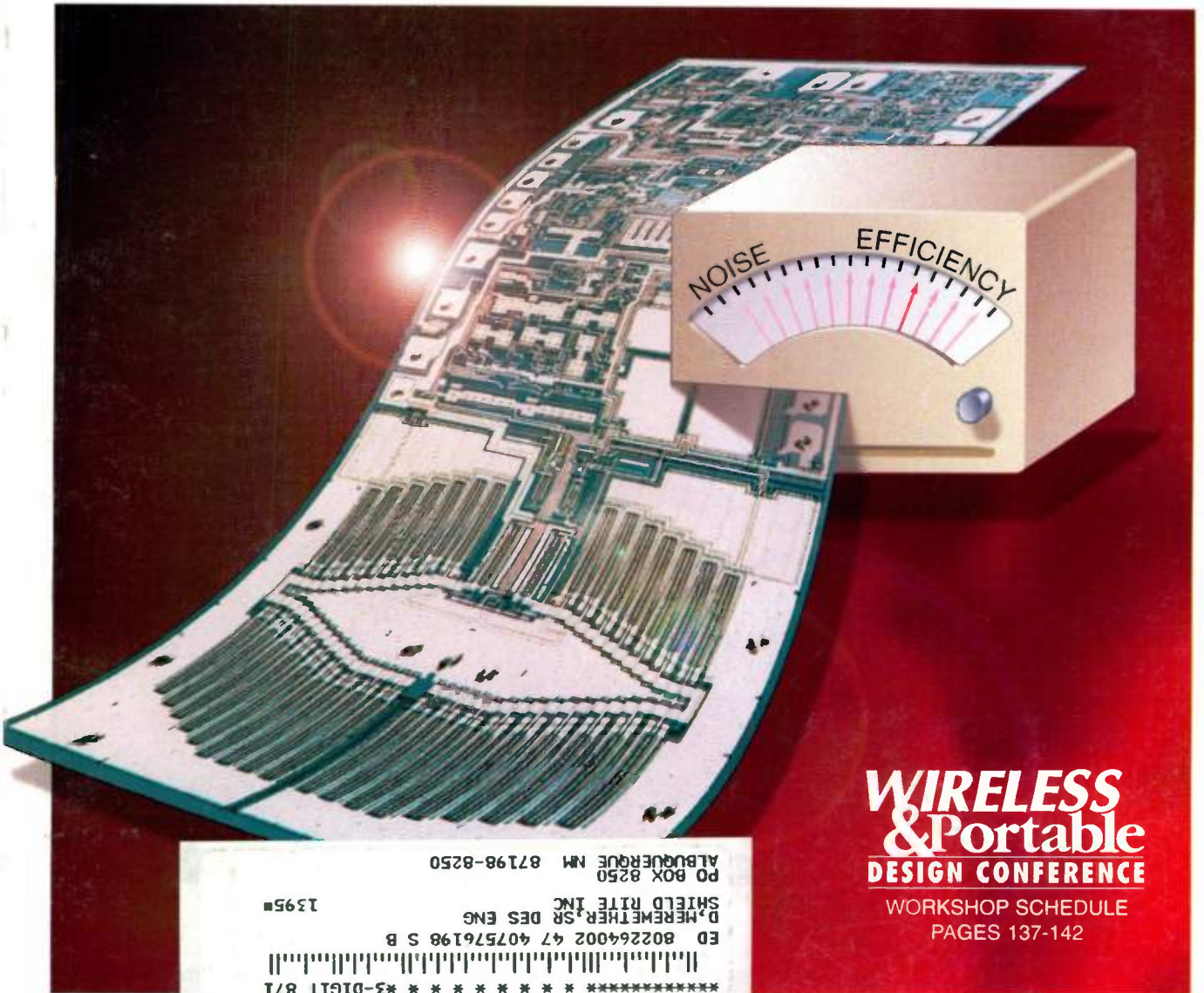


ELECTRONIC DESIGN

FOR ENGINEERS AND ENGINEERING MANAGERS - WORLDWIDE

A PENTON PUBLICATION \$10.00

AUGUST 18, 1997



**WIRELESS
& Portable
DESIGN CONFERENCE**

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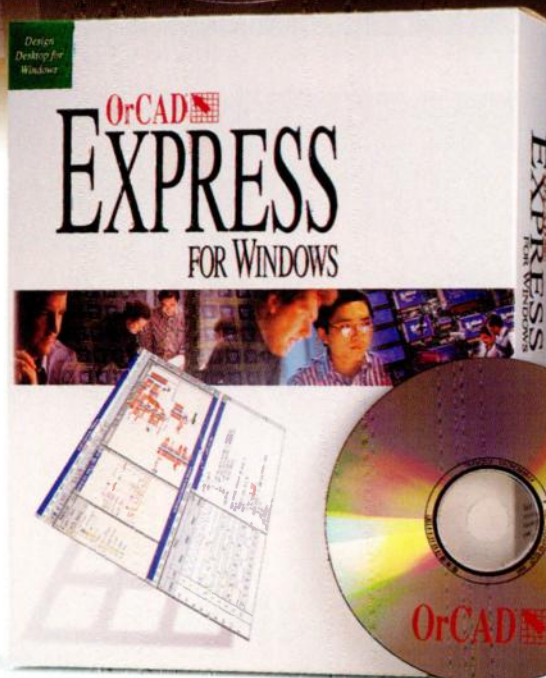
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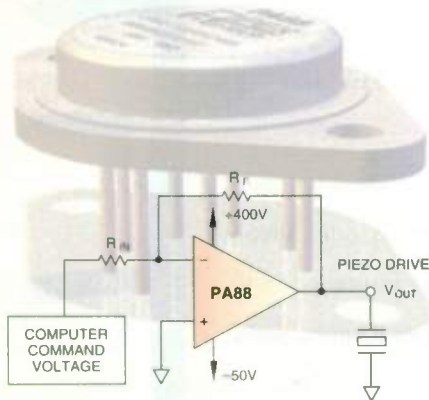
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For high voltage amplifiers, why look anywhere else?

The Power Miser

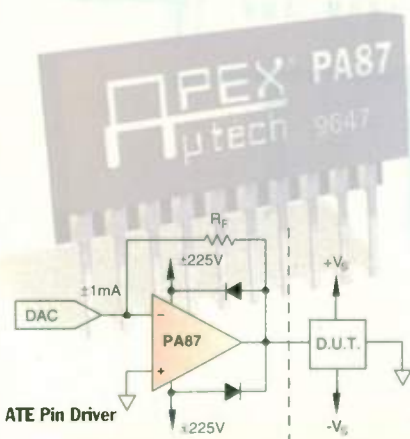
When concerned about system power supply drain or heat buildup, the PA88 offers cool running with only 2mA max standby current. With a total supply rating of 450V and an output capability of 200mA peak, the PA88 is up to your design challenges. The PA88M is the military screened version.



Low Power Micro Positioning

The Cool Runner

The PA87 combines a 450V total supply with 200mA of continuous output current while running cool at only 3.8mA max standby current. This makes the PA87 an attractive solution for driving large capacitive loads and powering piezoelectric applications. A 10-pin SIP package also means the PA87 saves board space and the EK42 evaluation kit makes the PA87 even easier to apply.



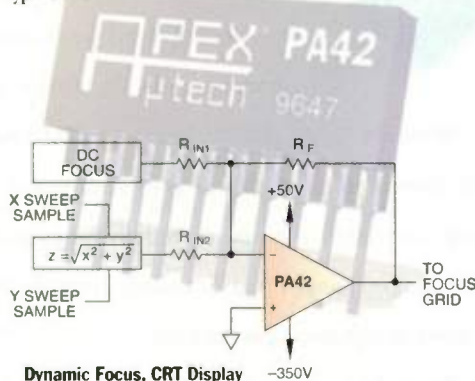
ATE Pin Driver

KEY PRODUCT SPECIFICATIONS

Part #	Supp	OUT PEAK	STANDBY	Slew Rate
PA08	30V-300V	200mA	8.5mA	30V/μs
PA41	100V-350V	120mA	2mA	40V/μs
PA42	100V-350V	120mA	2mA	40V/μs
PA85	30V-450V	350mA	25mA	1000V/μs
PA87	100-450V	300mA	3.8mA	20V/μs
PA88	30V-450V	200mA	2mA	30V/μs
PA89	150V-1200V	100mA	6mA	16V/μs

The Penny Pincher

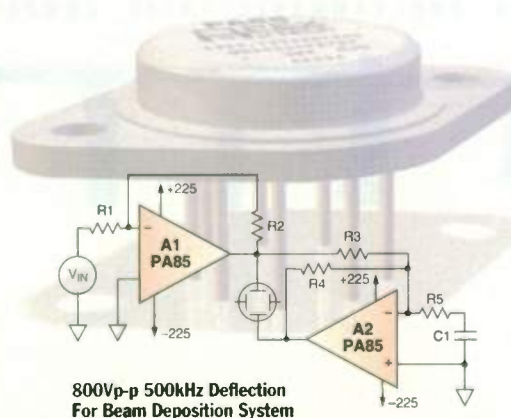
Monolithic technology makes the PA42's \$17.90 price tag in 10K pieces mighty attractive. With a footprint of less than one fourth that of a TO-3 package, the PA42 is THE choice for high density applications. The basic stats of this monolithic rate it up to 350V total supply and 120mA of output current. And with the EK42 evaluation kit, it's quick and easy to apply the PA42 in your prototype circuit.



Dynamic Focus, CRT Display

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If it's speed you need, the PA85 is the fastest high voltage op amp you can buy. A slew rate of 1000V/μs, a total supply capability of 450V and peak currents to 350mA, the PA85 is well suited to high speed drives for PZTs, optical switches and other capacitive loads. The gain bandwidth product of 100MHz insures AC fidelity. It's also available in a military screened version, the PA85M.



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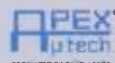
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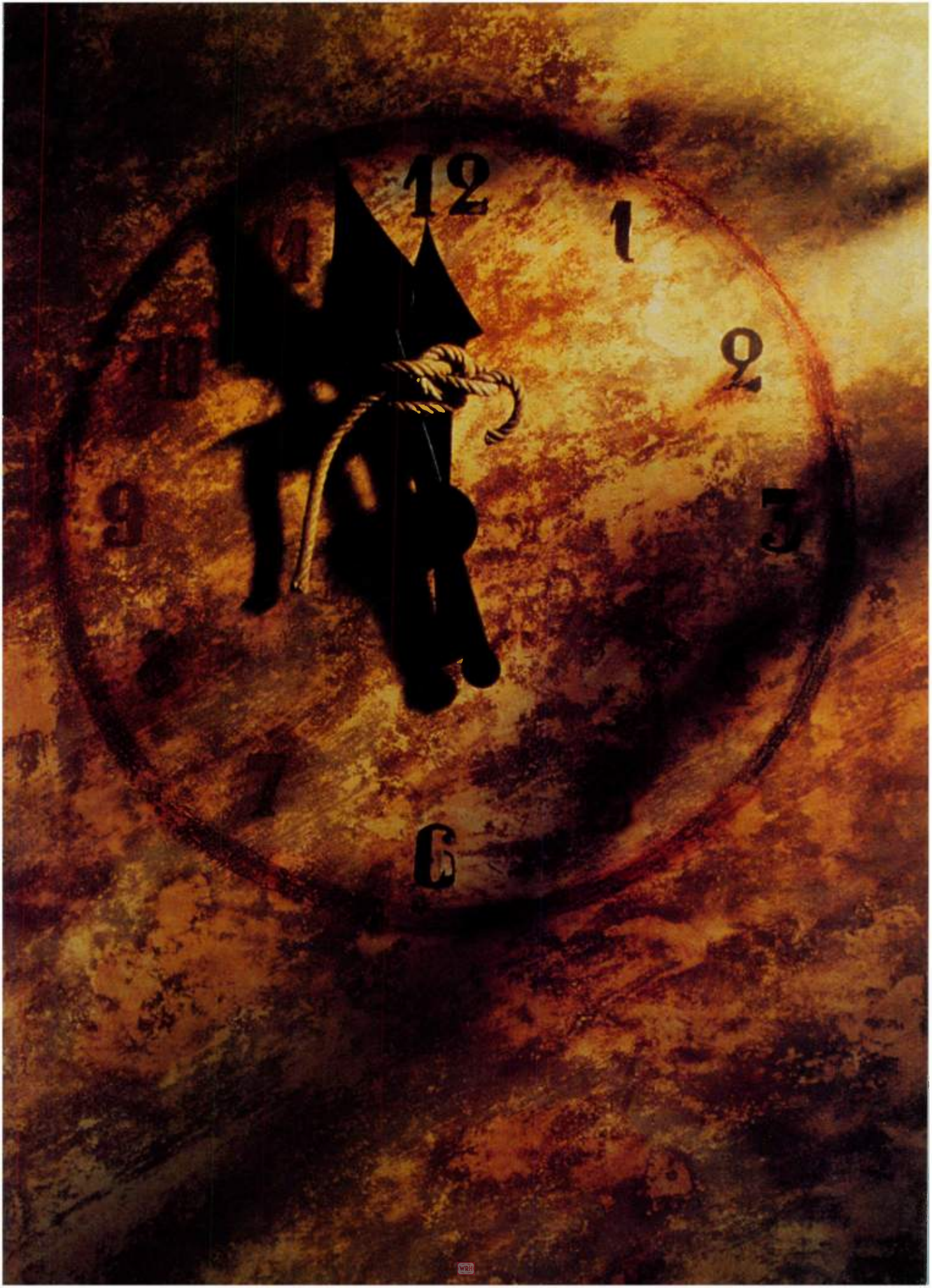
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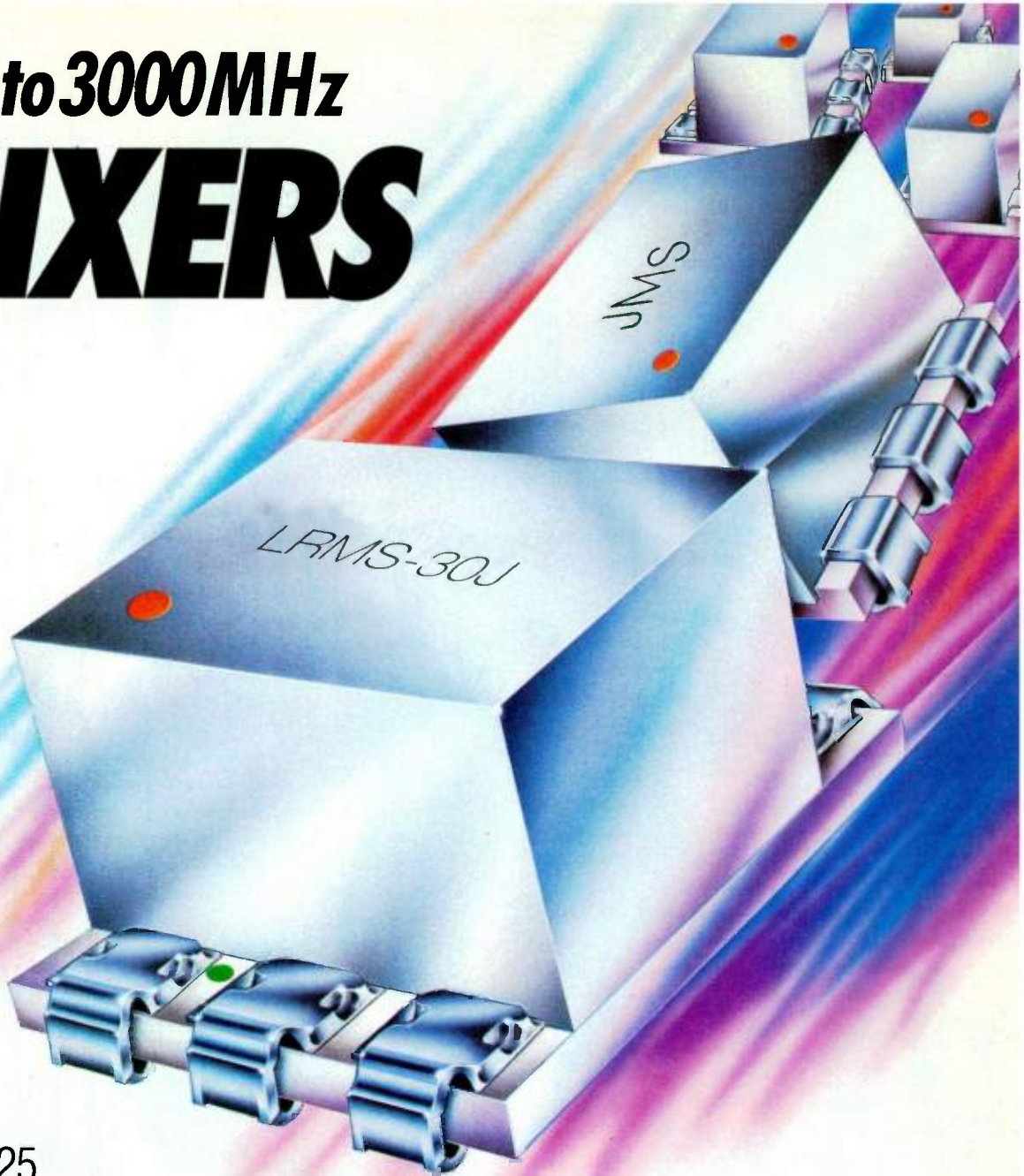


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JMS-1H	+17	2-500	DC-500	5.90	50	50	11.45
JMS-2L	+3	800-1000	DC-200	7.0	24	20	7.45
JMS-2	+7	20-1000	DC-1000	7.0	50	47	7.45
JMS-2LH	+10	20-1000	DC-1000	6.5	48	35	9.45
JMS-2MH	+13	20-1000	DC-1000	7.0	50	47	10.45
JMS-2H	+17	20-1000	DC-1000	7.0	50	47	12.45
JMS-2W	+7	5-1200	DC-500	6.8	60	48	7.95
JMS-5	+7	5-1500	DC-1000	6.0	50	30	9.95
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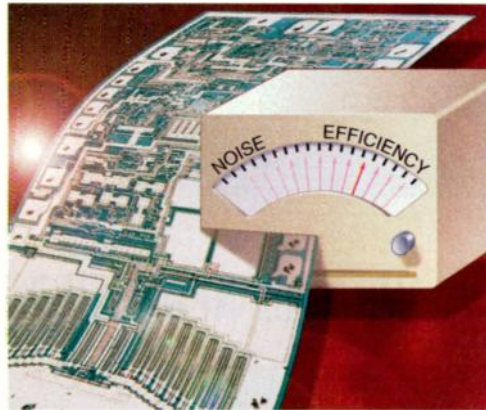
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ELECTRONIC DESIGN

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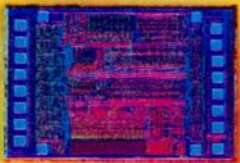
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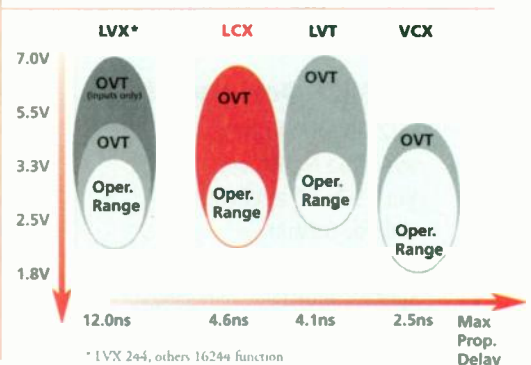
Power Supply	2.0-3.6V	
Drive (IoL/IoH)	24mA/-24mA (min)	
Supply Current (Icc)	1µA	
Speed (Tpd)	3.0ns	
Noise VolP(V)/VolV(V)	.7/- .6	

Over-voltage Tolerance Specifications*

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3-STATE Output Leakage (IoZ)	(0 ≤ Vo ≤ 5.5V)	1.5µA
Power-Off Leakage Current (Ioff)	(Vi or Vo = 5.5V)	1.5µA

* typical values represented unless otherwise specified

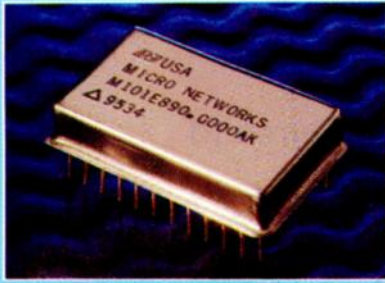
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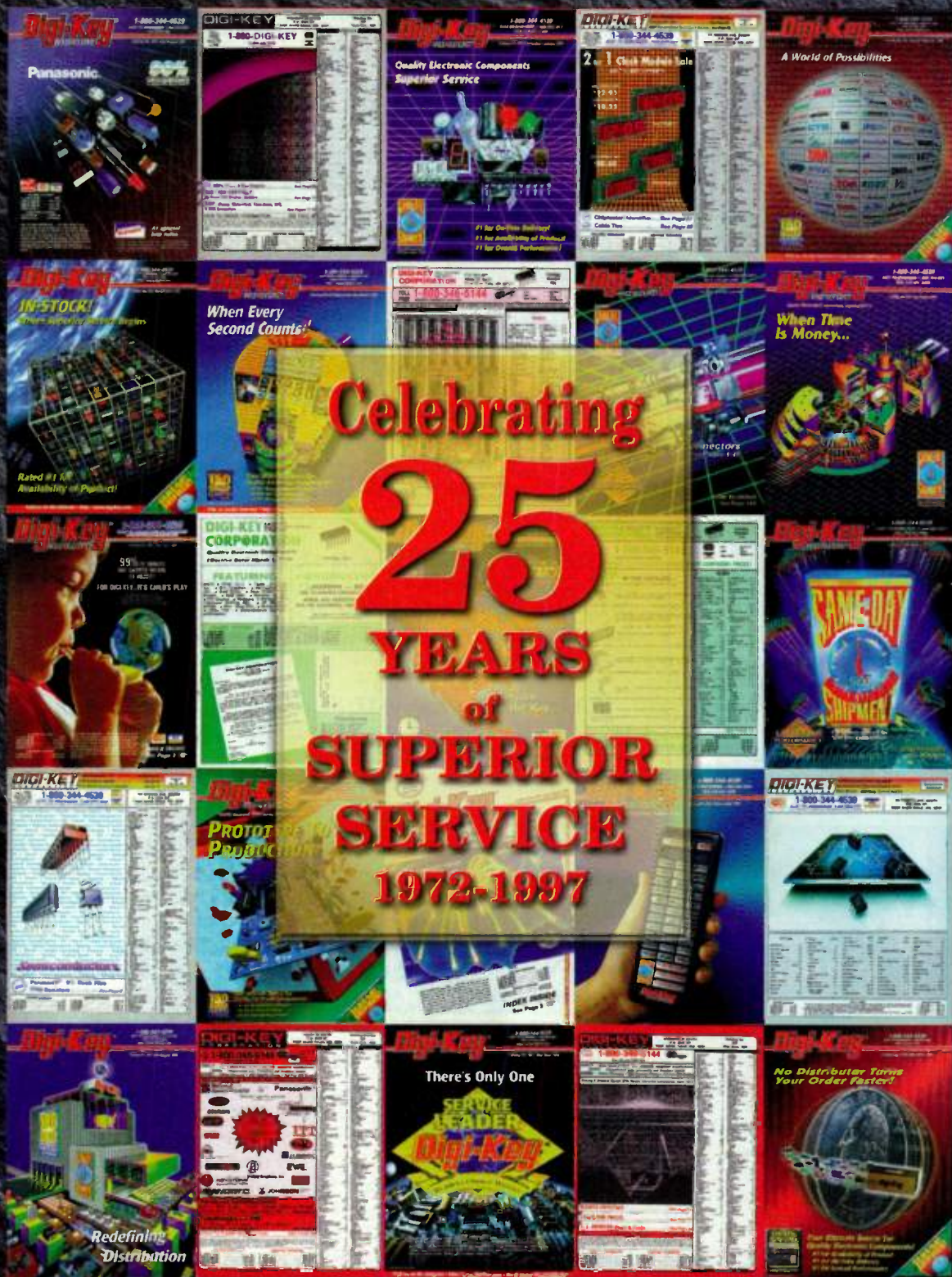
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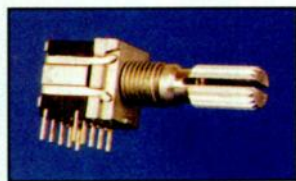
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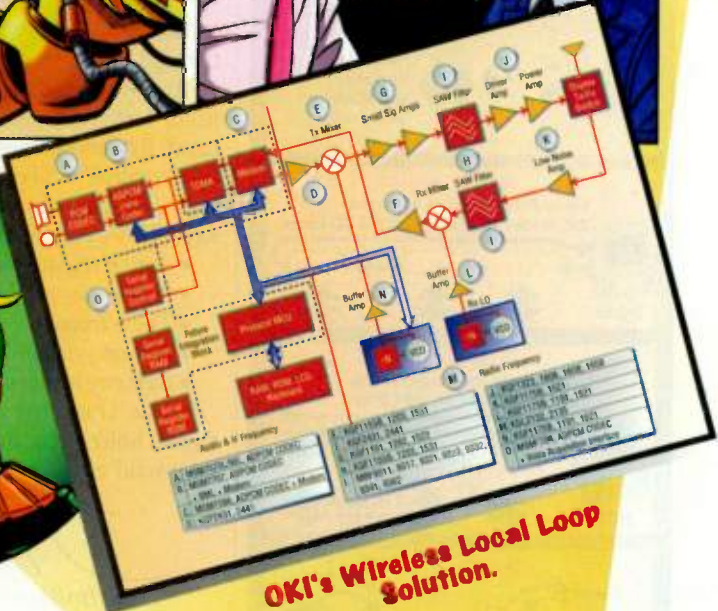
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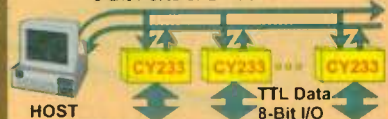
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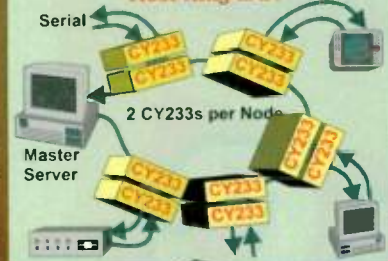


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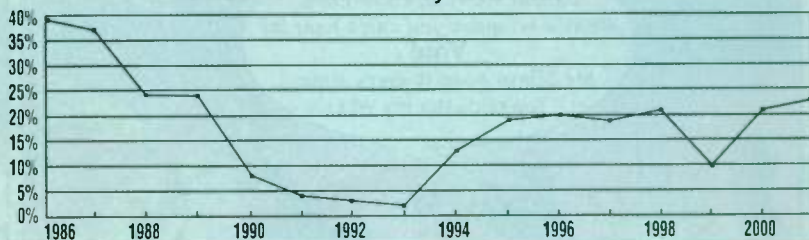
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Riding The EDA Roller Coaster

If you look below at the line chart of the electronic design automation (EDA) software market from 1986 to 2000 it would make a great design for a roller coaster: Plenty of steep drops, sudden turns, and rapid climbs. It may be thrilling to some, and frightening to others. It is obviously not a market for those who have queasy stomachs.

There are about 290 companies out there who believe that the EDA ride is worth taking, even with all of its ups and downs. Why? As you can see from the Dataquest chart, the EDA market is expected to take off (again) around 1999 and rapidly climb into the year 2000 and beyond.

EDA Growth History and Forecast



Source: Dataquest

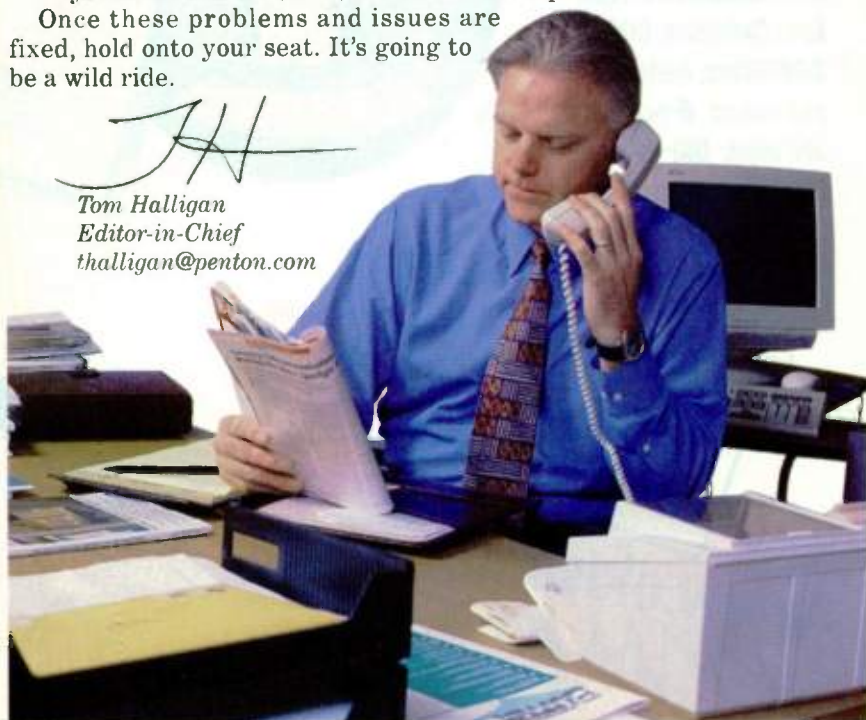
But first there will be a shakeout, predicted to begin next year and continue through 1999.

According to Gary Smith, a Dataquest analyst who tracks the EDA market, in the last three years, there have been 56 mergers or acquisitions. On the other hand, five companies decided get off the roller coaster for good. Smith says that the "turmoil" will continue, but get this: He predicts there will be two EDA software startups for every merger. "The market is going to grow like mad," he says. However, he says that a few issues have to be ironed out first:

- A new register-level-transfer (RTL) methodology toolset must be completed.
- A new physical verification toolset must be completed.
- The Virtual Socket Interface Alliance (VSIA) defines the virtual socket.
- A new system-level language must be introduced (IC-SLDL).
- System-level macro (SLM) tests must be completed.

Once these problems and issues are fixed, hold onto your seat. It's going to be a wild ride.

Tom Halligan
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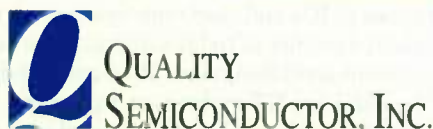
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To DAC And Beyond

This June, I attended the Design Automation Conference (DAC). Most people who go to DAC hope to gain insight into new tool development and get a feel of what's happening in the industry. With a fractured toe, I limped up and down every isle of the convention center, weaving my way through the demo suites. When it was over, I left with two bags full of information on company partnerships and new product announcements, a suitcase full of freebies, and sore feet. I also came away with some thoughts on how the design automation industry is shaping up.

For starters, we keep hearing about the consumerization of the industry, and how the lines between its various segments are starting to blur. But what does this really mean in application? LogicVision Inc., San Jose, Calif., may have an answer. Their BIST technology has surpassed the traditional boundaries of test and measurement. Their solution fits into traditional test applications, and is a vital component in the design stage. This is largely due to the migration toward systems on a chip which often brings the inaccessibility of current probing techniques. After all, you just can't hook up some probes to an IC and take measurements. But, with BIST embedded on the chip, once physical implementation is completed, verification of functionality will be possible. As a result, LogicVision is pioneering the link between traditionally disjointed test and EDA methodologies.

What about verification? Ask 10 people and you'll get 10 different answers. Today's verification challenges are not the same as before. It depends on the type of design you are doing and whether it is cutting-edge or mainstream. In any event, the verification challenge has always been real, but until now, people didn't fret over it. So, verification is not new. In fact, it resembles Intellectual Property (IP). But with the changing landscape of the EDA industry, the implications and definitions of verification and IP have taken on greater significance.

Other conclusions from DAC? First, deep submicron (DSM) design, verification challenges, and IP are three topics that won't go away any time soon. But the good news is that perhaps they aren't as close as we once thought; at least as far as the average mainstream designer is concerned. According to Gary Smith's 1996 *Semiconductor Design Pyramid*, 13% of the EDA community are power users; a whopping 71% are mainstream users; and 16% are late adopters. It's easy to forget that most of today's designers are mainstream, because the "sexy" topics that are discussed in the media are the ones that are being explored by the leading edge, high-end, power-user designer. (Smith is the EDA analyst for Dataquest, San Jose, Calif.)

But, let's not sell today's mainstream designer short. They face enormous challenges like getting tools with the needed functionality and ability to interface with other point tools. And what about the problem of evaluating new tools? You can't just shop for EDA tools the way you do for a new car. So how do today's mainstream designers buy their EDA tools? Very cautiously. They can't afford to buy a tool that won't work the way they need it to, or that will take them months to integrate into their company's design methodology.

Unfortunately, the needs of mainstream designers are often misunderstood and misrepresented. Why? Because instead of asking, we end up telling them what to care about and what problems they'll be facing in the future. To reverse the trend, *Electronic Design* has surveyed a group of engineers who design all types of ICs and electronic systems. A market study by *EDA Today* has helped paint a picture of today's mainstream designers, comprised mostly of board- and system-level designers. Most use Windows 95, 3.1, and DOS, but expect to shift to Windows NT in the next 18 months. And most IC/ASIC designers are working at 0.5-micron design rules and gate counts ranging from 20,000 to 150,000.

So, what do mainstream designers see as their upcoming challenges and crucial tool needs? E-mail me your thoughts at cjajluni@class.org.



CHERYL AJLUNI
DESIGN AUTOMATION

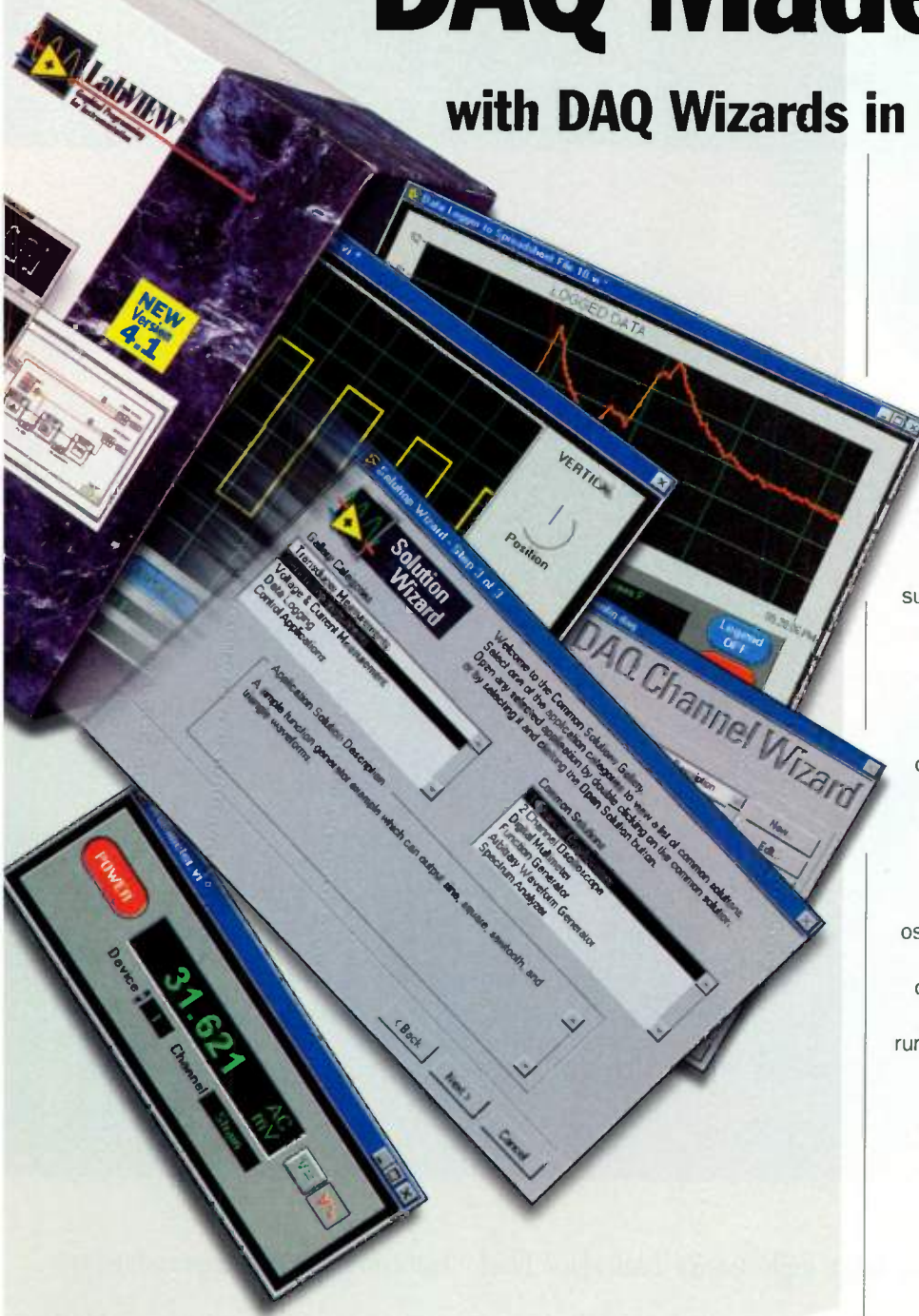
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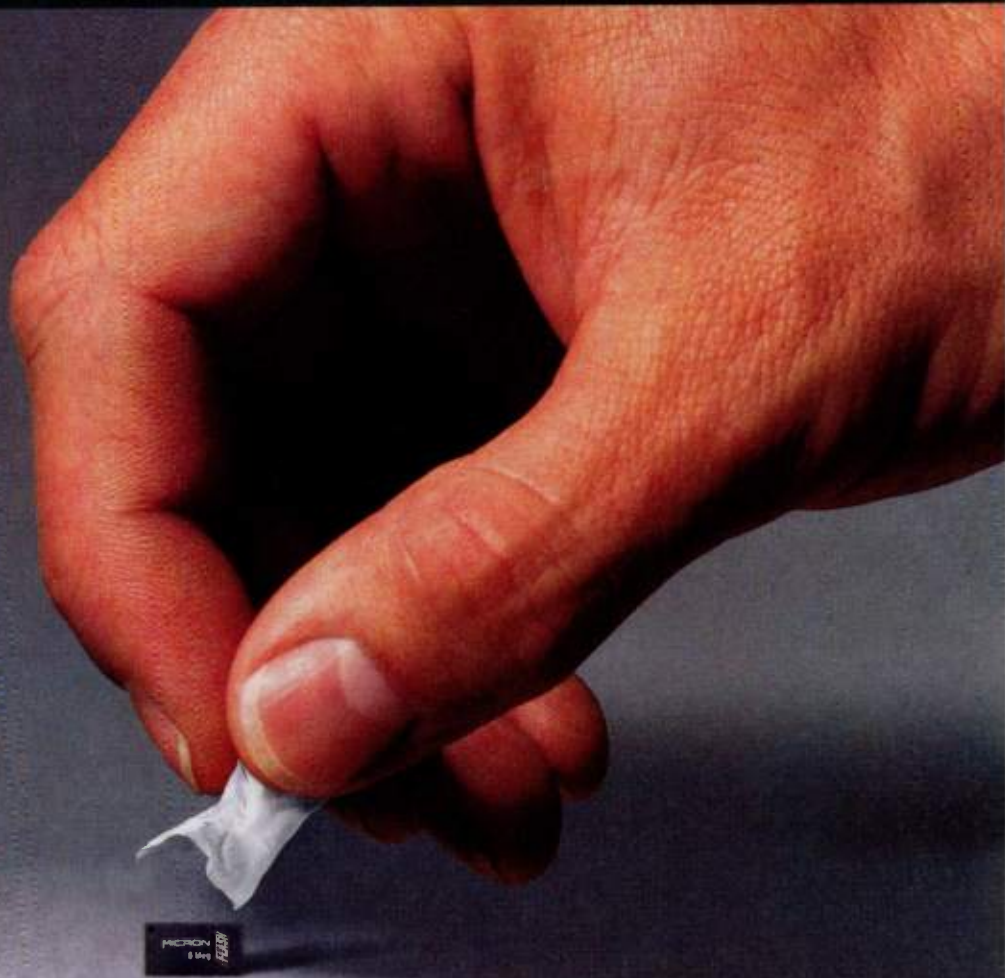
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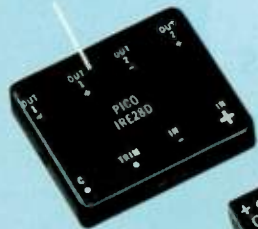
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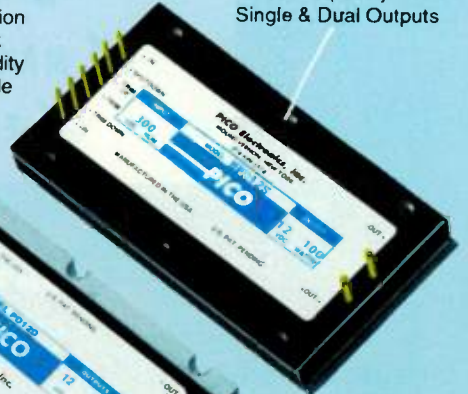
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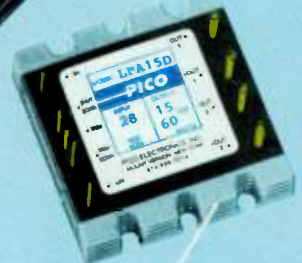
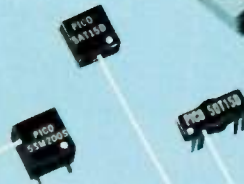
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Cytoperfusion To Revolutionize Diagnostic Laboratory Testing

Cutting a task that takes from six to eight hours down to less than 10 minutes seems like fantasy. However, that fantasy has become reality in the world of diagnostic laboratory testing of cells and chromosomes, thanks to a new technique called cytoperfusion. Developed by Grace Bio-Labs (GBL), Bend, Ore., the technique also eliminates the use of hazardous chemicals and uses 10,000 times less test reagent.

Says Dr. Charles McGrath, president and founder of GBL, "Using cytoperfusion and the instrumentation we've developed, some 2400 tests a day can be run, all with improved accuracy, safety, reproducibility, and cost efficiency." Current technology allows one medical technologist to perform about 20 tests per day.

The company is developing a four-module cytoanalyzer for rapid cell and chromosome testing. The four modules are the "cytolizer," "cytoflow," "lyofile," and an imaging platform. The cytolizer is a specialized benchtop specimen "freeze-dryer" that renders specimens permeable. The cytoflow is a benchtop manifold which filters reagents under pressure through the permeable specimens. Lyofile, a cassette-based specimen storage device, will retrieve specimens and move them from module to module using a robotic mechanism. The imaging platform—a microscope and photography station—performs image capture and transport.

When the cytoanalyzer operates as a four-unit module, tissue specimens are placed on a tissue disk that can hold 20 samples, which resembles that of a child's viewfinder toy. The disk is retrieved from a storage cassette via the lyofile mechanism, and is placed on the cooling platen of the cytolizer. After freeze-drying, the disk is either stored in the cassette or moved to the filtration platen of the cytoflow for assay. A computer-selected probe clip set is moved into place on the cytoflow and the reaction and washing steps are performed. The reacted specimen is moved to the imaging stage, where it's photographed and stored for transport and analysis.

Typical applications will be in the diagnosis and prognosis of cancer, the causes and treatments of AIDS, chromosome study, drug development, and the detection and screening of disease-causing microorganisms. Contact GBL at (541) 317-9656. *RE*

Benchmarks Will Look At Multimedia Performance

A new set of benchmarks is coming our way, this time to measure multimedia system performance. The Multimedia Benchmark Committee (MBC) will answer to the Graphics Performance Characterization (GPC) Group, which operates under the auspices of the Standard Performance Evaluation Corp. (SPEC).

The new group will develop standardized benchmark suites to help vendors and users compare and improve multimedia system performance. All MBC benchmarks will be designed for portability across platforms and architectures. Members of the MBC include Advanced Micro Devices, Apple Computer, Chromatic Research, Digital Equipment Corp., IBM, Intel, Motorola, Philips Semiconductor, SGS-Thomson Microelectronics, and Sun Microsystems.

The group's initial MPEG-2 benchmark will test processor, memory-system, and graphics performance at the systems level. It will specify acceptable quality levels and provide guidelines for MPEG-2 ISO compliance. Members of the MBC also will develop standardized procedures and formats that ensure uniform reporting of results. A beta version of the MBC's first benchmark, which measures MPEG-2 decoder performance, is expected by the end of the year. Future benchmarks will cover MPEG-2 encoding, speech recognition, 3D positional sound, 3D entertainment-oriented graphics, and multimedia Java-enabled Web pages.

The benchmarks will run on Windows NT, MacOS, Windows 95, various versions of UNIX, VRTX, and OS-9000. Information on the MBC is available by surfing into their web address at <http://www.specbench.org/gpc>, or by sending an e-mail to Ahmad Zandi, MBC chair, at ahmad.zandi@eng.sun.com. *RN*

Thermal Oxidation Improves Battery Performance

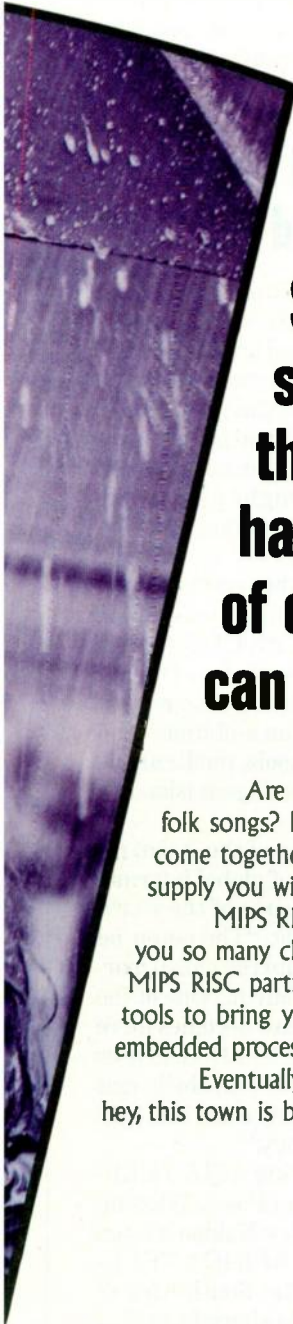
By using thermal oxidation to change the electrochemical behavior of the form of carbon used in batteries, researchers at the University of Buffalo in New York were able to enhance the batteries' current-carrying capabilities. According to Deborah Chung, PhD and university professor of mechanical and aerospace engineering, using thermal oxidation to change the electrochemical behavior of carbon black improves the electron transfer rate in batteries. Carbon black, which consists of particles (e.g., powder) bound together by an oil or some other polymer rather than filaments or fibers (like some other carbons), is the most frequently used form of carbon in batteries.

Thermal oxidation involves heating carbon in the presence of oxygen, creating carbon bonds that change carbon black's morphology (form and structure) in addition to improving electrical conduction. Employing this process changes carbon black's particle size and increases its macropore density, allowing the carbon-black particles to "hang together" without a binder. And, because the types of binders used "tend to be a material that degrades in a chemical environment like batteries," says Chung, "eliminating the binder will not only enhance the batteries' ability to conduct current, it also will save processing costs." Call the University of Buffalo at (716) 645-2626; fax (716) 645-3765. *RE*

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Monster Magnetic Fields Used To Evaluate Materials' Resistance

In an experiment that may help in the design of superconductors and better semiconductors, an international team of scientists created an extremely strong magnetic field, then blew it up to determine its effect on sample materials. A series of four such tests were conducted at the Los Alamos National Laboratory, New Mexico, by researchers probing how material conducts electricity in extreme conditions.

The team placed the material samples inside an electromagnet and cooled the samples to a few degrees above absolute zero. The magnet was surrounded by about 35 lbs. of explosives, which were arranged to produce a perfectly uniform implosion. In the millionths of a second before the equipment was destroyed, sensors measured how the samples' electrical resistance changed as the magnetic field was squeezed and concentrated by the blast. The sustained fields in the electromagnets reached 60 tesla. Momentary pulsed fields hit 850 tesla.

"We have gotten excellent results," said Laurence Campbell, Los Alamos project leader. "We've gotten higher fields at lower temperatures than ever seen before." The team included scientists from Australia, Belgium, Germany, Japan, and Russia, along with Los Alamos researchers. The laboratory is home to a branch of the National High Magnetic Field Laboratory, a U.S. consortium dedicated to magnetic field research. *JN*

Technology Agreement Will Make System-On-A-Chip Design Easier

Higher design complexity and time-to-market pressures has made the task of fabricating advanced chips ever more difficult. This problem is complicated further by the industry's migration to systems on a chip (SOC). Mentor Graphics, Wilsonville, Ore., and Chartered Semiconductor, San Jose, Calif., are attempting to ease this burden through a joint technology agreement intended to empower users with the reliability and productivity needed to get systems designs to market quicker.

As part of the agreement, Mentor's Inventra business unit will be responsible for developing and supplying standard cells. It also will develop and supply memory and datapath libraries for Chartered's 0.35- μ m fabrication process, and a design kit comprising the cell libraries, cell attributes required for use with HDL, and logic synthesis tools offered by various suppliers. Both companies will develop test chips based on a subset of Inventra's CoreAlliance pre-designed blocks of circuits, for design verification in silicon.

It's expected that with this joint technology agreement, it will be possible for IC design teams to leverage quicker access to silicon-proven libraries and intellec-

tual property in designs. This will also be the case with Chartered's manufacturing processes for chip fabrication. As a result, engineering teams will be free to focus its efforts on the value-added tasks and key differentiators for its systems on a chip. To obtain additional details on this technology partnership, surf into <http://www.mentorg.com.ca>

Asia Telecom Beats All Forecasts; South Africa Gets Nod For '98

The fourth regional telecommunications exhibition and forum, ASIA TELECOM 97, was held this summer in Singapore. It attracted approximately 40,000 visitors from 104 countries, who came to participate in the forums and visit the 476 exhibitors. Apart from the large number of ambassadors and government ministers, the event also attracted external investors who went to see what role they might play in the world's biggest and most rapidly expanding telecommunications market.

The prime minister of Singapore, the secretary-general of the International Telecommunications Union (ITU), and the CEO of Motorola (Mr. Christopher Galvin) spoke at the opening ceremonies. During Galvin's presentation, the prime minister announced a pilot program for Singapore ONE—an ambitious program that would link businesses, schools, public areas, and some 800,000 households as an intelligent island by the end of 1998.

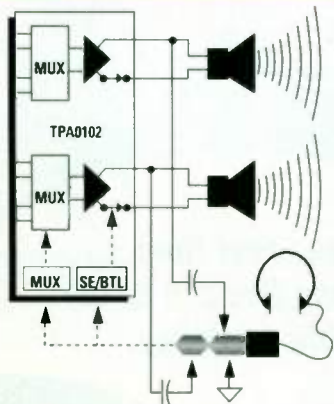
Galvin emphasized the importance of the Asian region and observed that the benefits of global information highways would extend to all parts of the world more quickly than previously thought. "The potential for emerging economies to leapfrog into the global marketplace is greater than ever," said Galvin. "One of the ironies of technology is that as software becomes more complex and sophisticated, the product for the end user becomes easier to operate." He added, "This challenges old assumptions about how innovation occurs and how rapidly a culture adopts new technology."

Singapore also was the venue, during ASIA TELECOM 97, for South Africa's Minister of Posts, Telecommunications, and Broadcasting, Mr. Jay Naidoo, to sign an agreement with the ITU to host AFRICA TELECOM 98. This exhibition will be held at South Africa's National Exhibition Centre in Johannesburg from May 4-10, 1998. Naidoo remarked that this would signal "the rebirth of the African continent wired into the global information society."

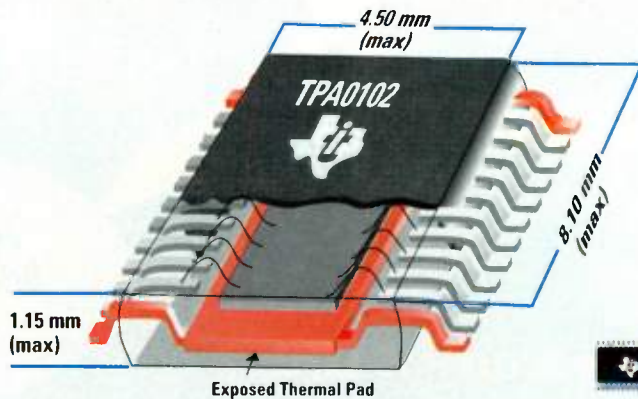
The next TELECOM event will be TELECOM INTERACTIVE 97, a new forum and exhibition focusing on interactive and multimedia services and applications, held in Geneva from September 8-14. The next World TELECOM also will take place in Geneva from October 10-17, 1999. *PMcG*

Edited by Roger Engelke

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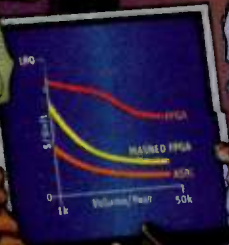
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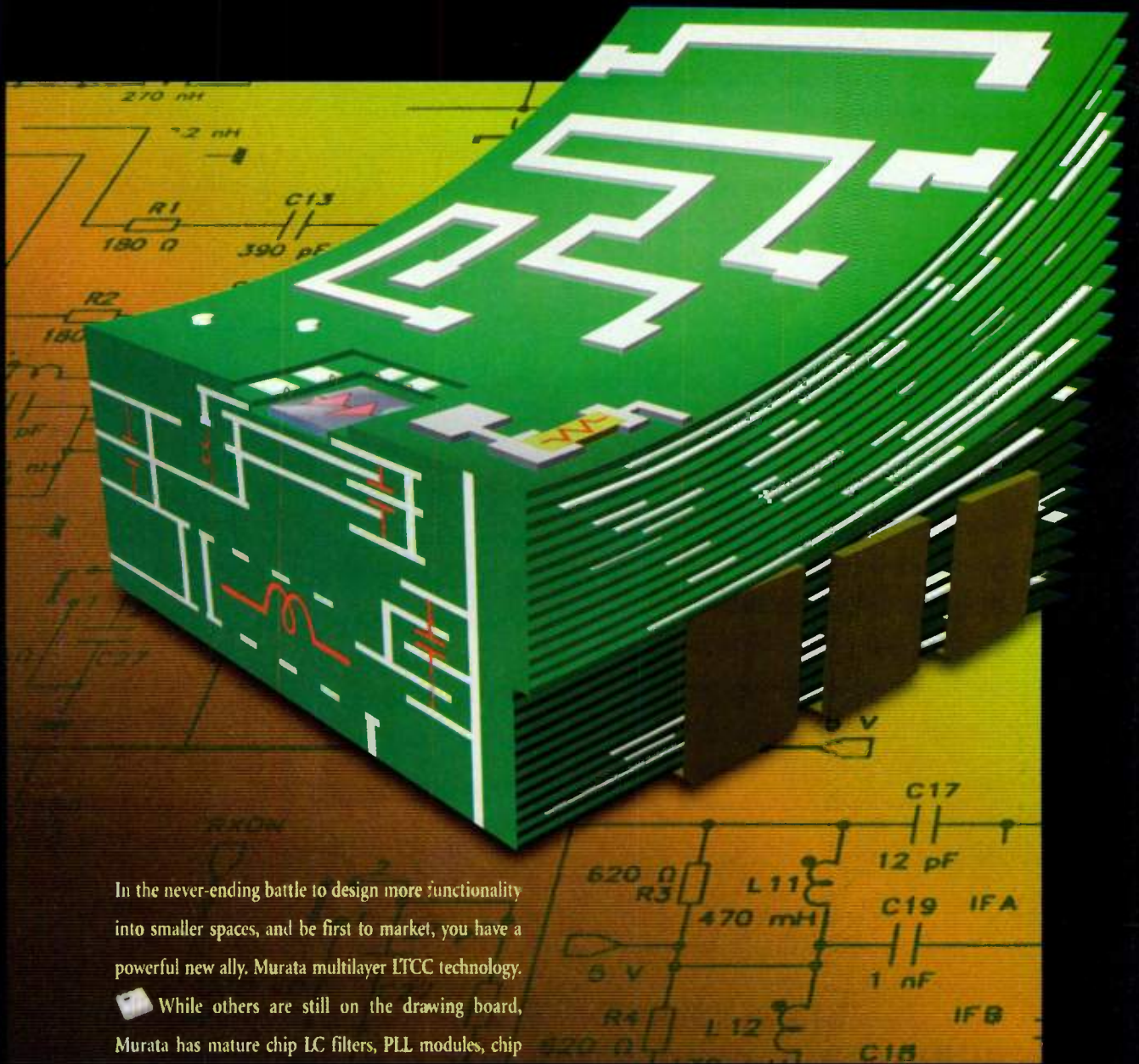
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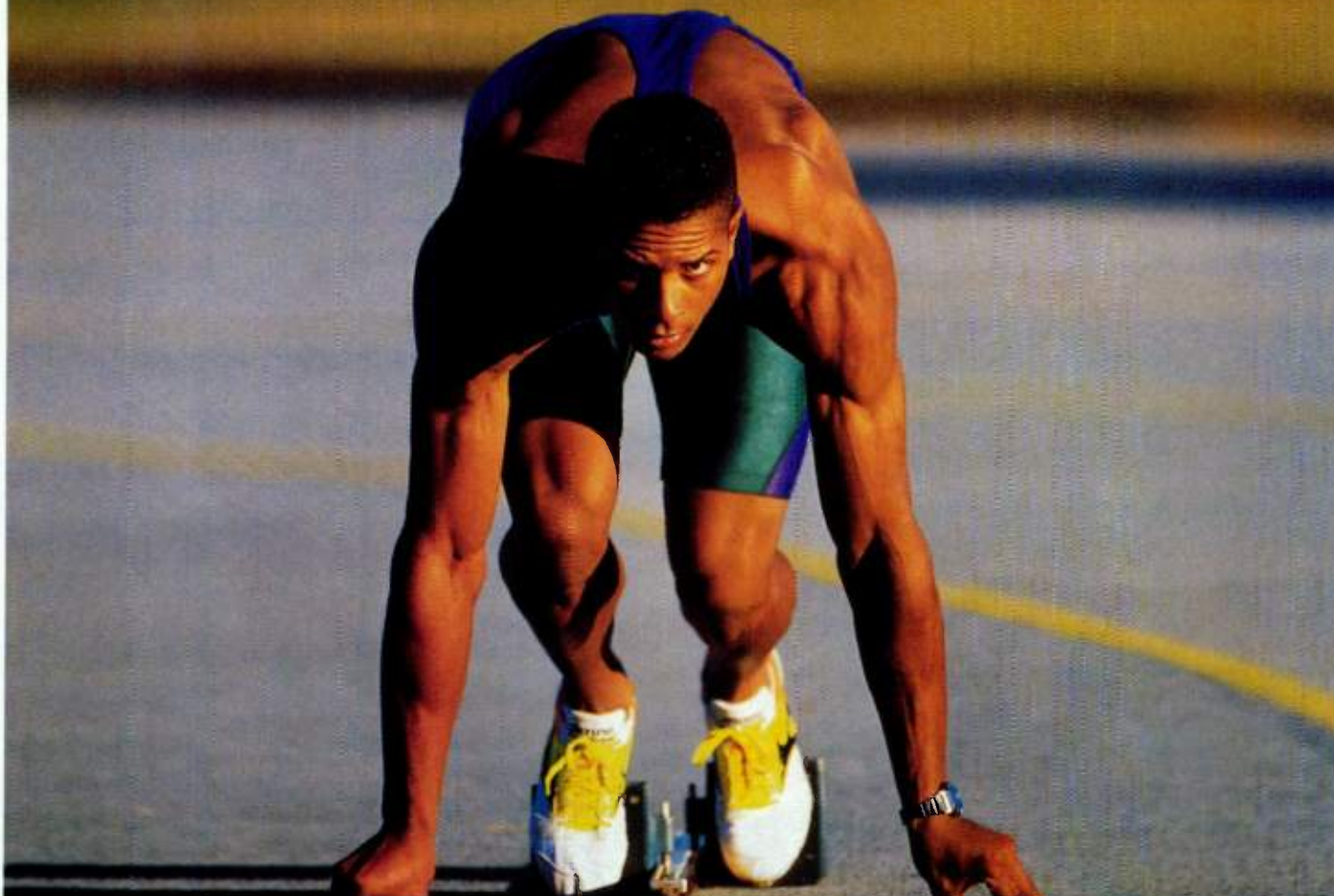
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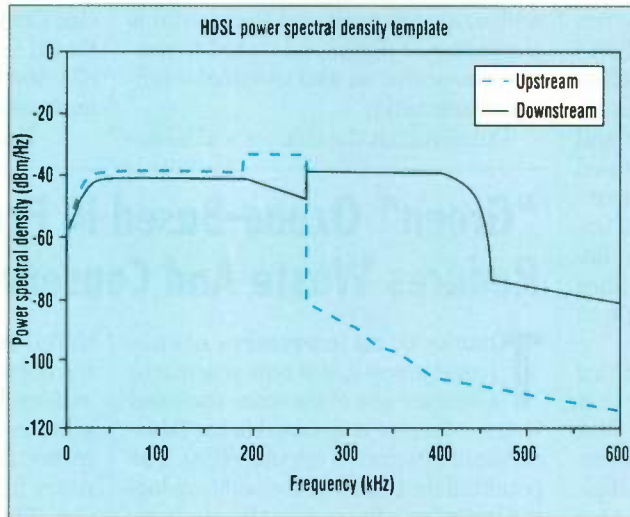
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Proposed Standard Could Double The Capacity Of T1 Lines And Residential Broadband Networks

If accepted by the T1/E1 Committee, a new technology that proposes to double the capacity of current high-rate digital subscriber (HDSL) lines could be available early next year. Known as HDSL2, the proposed standard uses sophisticated line coding, spectral shaping, and adaptive filtering to deliver full-duplex digital traffic at up to 2 Mbits/s over a single pair of twisted-pair copper wires. Since current T1 and HDSL services require four wires to carry the same amount of data, carriers will be able to stretch their limited inventories of installed copper twice as far as they struggle to meet the increasing demands for business and Internet access services.

The present HDSL standard was developed in 1992 and uses a 2B1Q line code to deliver T1 (1.544 Mbits/s) and E1 (2.048 Mbits/s) services over two twisted pairs at distances of up to 12,000 feet. It is now used throughout the world by local exchange carriers (LECs) and network service providers to carry telco trunk services, as well as provide subscribers with high-speed digital lines. HDSL's popularity is largely due to the fact that it eliminates the need for repeaters and specially conditioned lines required by the original T1/E1 technologies.

Three companies are collaborating on



1. HDSL2's power spectral density template illustrates how spectral shaping of the upstream and downstream waveforms controls the signal energy created in the upper frequencies.

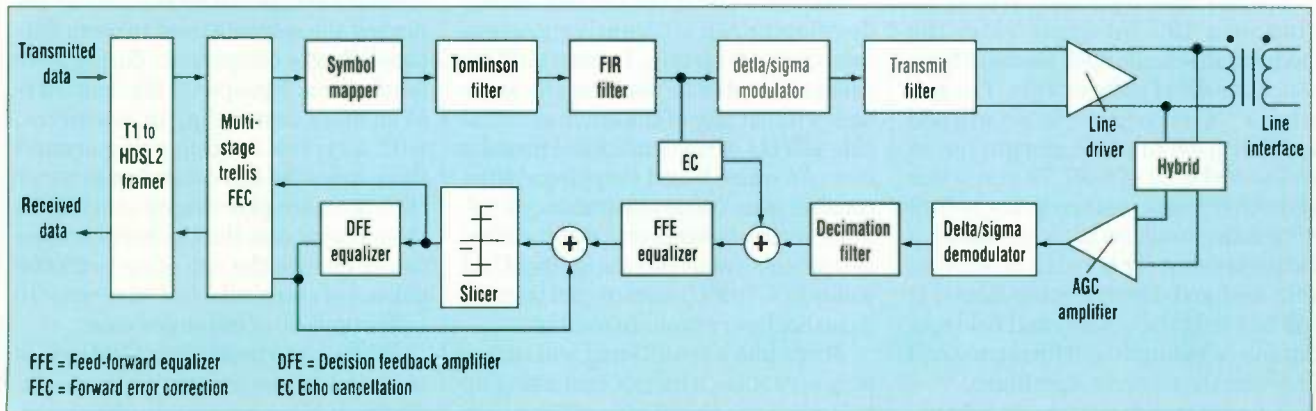
the HDSL2 standard development, with Level One, Sacramento, Calif., and PairGain, Cerritos Calif., planning to jointly develop the first silicon implementations. PairGain and ADC Telecommunications, Minneapolis, Minn., will develop systems based on the technology. The trio has defined a line code, modulation scheme, and forward-error correction (FEC) scheme that provides the same performance and service over a single line that HDSL currently provides over a single twisted-pair line.

The joint HDSL2 proposal has been submitted to the T1/E1 committee along with the support of Adtran Corp., a major manufacturer of communica-

tions equipment. If adopted, HDSL2 is intended to be an open standard, with no licensing fees attached to it. Its ability to transmit data at 30 times the speed of today's fastest analog modems makes it an attractive and potentially inexpensive way to deliver Internet access, remote networking, and other high-speed digital services to businesses and residences.

One of the most significant challenges in developing the HDSL2 technology was to double the line transmission rate without causing excessive crosstalk within a standard 50-pair wire bundle. As a result, a central component of the proposed standard is a spectrally shaped waveform. To accomplish this, HDSL2's developers chose to use a relatively simple pulse-amplitude modulation (PAM) scheme that produces three information bits per transmitted symbol. Additional PAM states are included to support FEC. Spectral shaping is used to reduce the waveform's unwanted high-frequency components (Fig. 1).

By carefully controlling the energy distribution in the higher frequencies, HDSL2 signals can coexist with existing T1, HDSL, or ADSL services, while providing good performance even in worst-case environments that contain a mixture of other signals. The amount of spectral energy is sharply limited above approximately 270 kHz in the upstream path, and around 480 kHz in the downstream direction. Finally, FEC encoding is used to add several dBs of noise



2. Block diagram of an HDSL2 system illustrates how the digital bit stream is mapped into a constellation of phase/amplitude symbols, pre-distorted, and spectrally shaped before transmission. On the receive side, the incoming signal undergoes a similar process in reverse, along with digital echo cancellation.

immunity against EMI and crosstalk from other wire pairs.

A block diagram of the system shows how a transmitted T1 bit stream is multiplexed and converted to an HDSL frame format, with frame synch words and an embedded overhead channel added (*Fig. 2*). It is then passed through a multistage trellis encoder to provide error detection and correction. Once the data is mapped into a constellation of amplitude symbols, the digital representation of the waveform is passed through a Tomlinson (least-mean squared function) filter that pre-distorts the pulse shape to match the line characteristics.

The signal then passes through a fixed-coefficient FIR-type filter that performs the spectral shaping that helps to compensate for channel distortion and minimize crosstalk. The digitized stream then passes through a delta/sigma modulator and is converted to an analog signal and filtered before it is coupled to the line.

Adaptive filtering and equalization is used throughout the system to compensate for the extremely variable and nonlinear characteristics encountered on phone lines. In the case of the transmitters' Tomlinson filter, it derives its coefficients by sending a test sequence to the far-end receiver at startup. Using a mean-square error minimization correlation algorithm, the receiver then calculates the equalizer coefficients needed to compensate for line distortion and sends them to the transmitter.

No hardware to evaluate the proposed standard has been constructed yet, but the extensive simulations that the model has been subjected to indicate that it will have excellent performance and noise resistance. When running at a 10^{-7} bit-error rate, the modulation scheme itself seems to have about one dB of noise margin. The system's FEC-encoding scheme will add another 5 dB of noise margin for an end-to-end total of 6 dB. To verify this and other performance goals before committing to silicon implementation, a hardware test jig is being fabricated with LSI and discrete components. It will be used in laboratory and field conditions to evaluate performance and fine-tune the receiver algorithms.

A prototype chip set is already under development. Other than an input and an output digital-to-analog con-

verter (DAC), the HDSL2 transceivers' signal path will be all-digital. The initial system will consist of three chips: A modem core, a digital chip containing the FEC and framer circuitry, and an analog front end that contains the analog-to-digital and digital-to-analog conversion, as well as signal conditioning circuitry.

Details about the chip set and its an-

ticipated availability are not public yet, but a safe bet would be to anticipate its arrival during the later half of 1998.

For further information about HDSL2, contact Tom Agler at Level One Communications Inc., 8750 Goethe Road, Sacramento, CA, 95827; (916) 855-5000; fax (916) 854-1192; e-mail: tagler@level1.com.

Lee Goldberg

"Green" Ozone-Based IC Process Reduces Waste And Conserves Water

Thanks to an innovative ozone-based process, it is now possible to eliminate one of the more toxic and water-intensive steps used in the fabrication of integrated circuits (ICs). The potential for reducing the semiconductor industry's impact on the environment is so significant that process' inventor, Robert Mathews, founder of Legacy Systems Inc., Fremont, Calif., was awarded the 1997 Presidential Green Chemistry Challenge award.

Since its early days, the semiconductor industry has relied on an acid-based method of removing photoresist from wafers between each of the 10 to 20 lithographic steps required to form the transistors and lay up the metallic interconnections on a microcircuit. Known affectionately as the piranha-etch process, it involves a toxic soup, usually consisting of sulfuric acid and hydrogen peroxide, heated to between 70°C and 150°C. Besides the thousands of gallons of toxic waste it generates, a single photoresist stripping station can consume up to three-and-a-half million gallons of pure water per year in its rinse process.

Mathews has spent the last decade developing, an alternative process known as Coldstrip. It uses chilled, ozonated water to perform the same task without any of the environmental side-effects of the traditional piranha etch. An ozone-based stripping station consists of an ozone generator, gas diffuser, recirculating pump, water chiller, and process vessel (*see the figure*). Cold water (2°C to 9°C) is employed because it can hold more ozone in solution.

Much like a traditional wet-stripping operation, a carrier containing up to 50 wafers is placed in an etchant bath (also known as a weir). With Coldstrip, the weir provides a continuous flow of

chilled ozonated water flowing up from the bottom of the bath and around the wafers. Dissolved ozone comes out of solution and attacks the resist's carbon-carbon double bonds, converting it directly into carbon-dioxide gas and water. The gas then bubbles out of solution, leaving the water clean, with no residue or flakes associated with acid-based stripping processes. Up to 15,000 Å of photoresist can be removed from a wafer in less than 25 minutes.

Once the water passes over the wafers, it spills over the weir's sides where it is captured, rechilled, reozonated, and recirculated. In contrast, conventional stripping processes use and discard over 100 gallons of clean, deionized water for the multiple rinses needed to process a single batch of wafers. This translates into over three million gallons of water a year per stripping station, given a semiconductor fabrication line's normal throughput. Besides considerable water savings, the process also eliminates the need to handle and dispose of roughly 8400 gallons of toxic etchants each year. Similar savings can be realized by replacing the solvents used to clean flat-panel display components during their fabrication. Flat-panel fabrication is even more demanding of resources, with a typical system using around three times the solvent and rinse water than a wafer-processing station. In these operations, the Coldstrip process can eliminate the use of up to 25,000 gallons of chemicals, and save over 10 million gallons of water per year.

While quite promising, Coldstrip is not a cure-all for the semiconductor industry. It is not completely effective on some types of hard-baked photoresist materials which do not have free hy-

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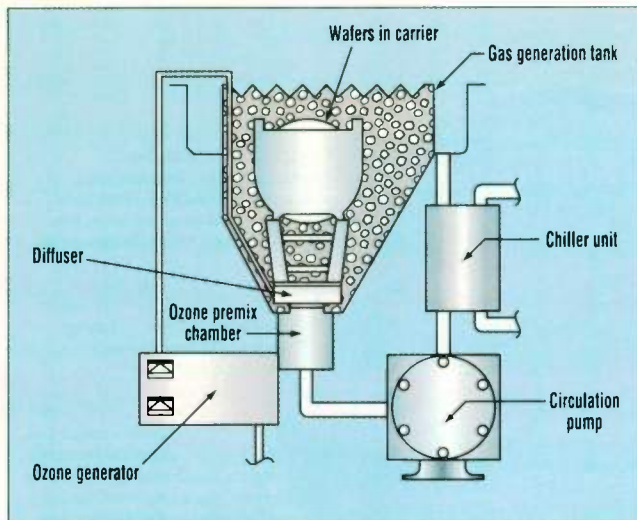
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droxyl groups available at the film's surface to react with the dissolved ozone. In these cases, smaller amounts of traditional solvents will still be required.

An alternative process known as ashing is sometimes used on these hard photoresists. It involves reducing the resist coating to an ash in a high-temperature oven and then removing it with solvents. By adding a filtration system, a modified version of the Coldstrip process can be used to clean the ashed wafers.

Other environmentally safe alternatives, such as frozen carbon-dioxide slurry and a frozen argon/nitrogen cleaning mixture also are being investigated for specific surface-cleaning tasks within the semiconductor and flat-panel display manufacturing processes. For removal problems which cannot be accomplished any other way, Legacy also plans to work



The Coldstrip photoresist removal process uses a standard wet-stripping bench, refitted with a cold-ozone injection system and water-recirculating system. Eliminating the acid etch and flow-through rinse lets the closed-cycle stripping system save up to 3.5 million gallons of water a year.

manufacturer has tested the Coldstrip process on a trial basis in one of its larger facilities. After six months of intensive testing, they installed an ozone stripping station in their production facility. Once this production testing proves successful, the conversion of their main manufacturing facilities could begin as early as this month. Evaluations are underway with several other large U.S. semiconductor IC manufacturers. Coldstrip has received an even warmer welcome overseas. Two major Asian semiconductor IC manufacturers are placing stations in their production lines this summer.

For more information, contact Carl Muti at Legacy Systems Inc., 8701 Harrogate Court, Raleigh, NC 27613; (919) 870-4606; fax (919) 676-7041; e-mail: CarlMuti@compuserve.com.

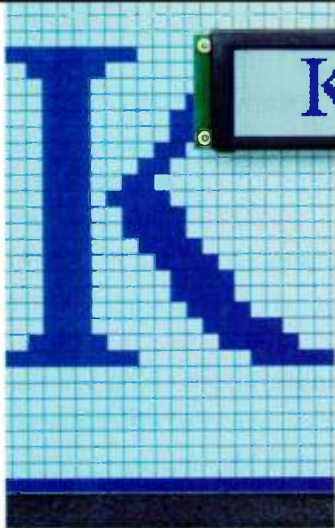
Lee Goldberg

with the EPA to develop a hybrid solution which uses extremely small amounts of conventional solvents to augment its ozone-based process.

At least one leading U.S.-based IC

manufacturers are placing stations in their production lines this summer.

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TECH INSIGHTS

■ Exploring issues for advanced power-supply design

Power-Supply Designers Trade-Off Efficiency For Noise With Switcher IC

Two Off-Chip Resistors Let Designers Adjust Slew Rates Of Voltages Across The Switch And Currents Flowing Through It.

Frank Goodenough

Switching regulators, or switch-mode dc-dc converters, are noisy, albeit typically very efficient, devices. The harmonics of the switcher's fast-rising voltage and current pulses create the noise which shows up as radiated and conducted electromagnetic interference. This noise disturbs nearby circuits such as microprocessors and low-level, analog front ends. In addition, the noise interferes with the operation of sensitive RF receivers some distance away. Increasing the rise and fall times of the switching pulses (by lowering the circuit's slew rate) cuts noise, but raises the switching losses. Consequently, the efficiency of the switcher is reduced. Switching losses occur when there is voltage across a converter's power switch while current is flowing through it.

Until now, trading off efficiency for noise was not a simple task. However, a team from Linear Technology Corp. (LTC) designed a 1-A pulse-width modulation (PWM) switching regulator (controller plus on-chip power switch or switches), the LT1533. This IC allows a power system's designer to adjust the slew rates of both the voltage pulses across the switch and the current pulses going through it with a pair of off-chip resistors R_{VSL} and R_{CSL} . They connect their respective pins to ground (Fig. 1).



Resistor R_{VSL} sets the voltage slew rate and R_{CSL} sets current slew rate. Varying them between 4 k Ω and 68 k Ω adjusts the voltage slew rate from 80 V/ μ s to 5 V/ μ s and from 7 A/ μ s to 0.4 A/ μ s. The spread in efficiency, typically 7%, is a function of the exact circuit used and its layout.

A Closer Look

The LT1533 is a fixed-frequency, current-mode PWM switching regulator, or switcher (Fig. 1, again). Current-mode circuits and many other functional blocks have been deleted from this simplified block diagram for clarity. Typical of cur-

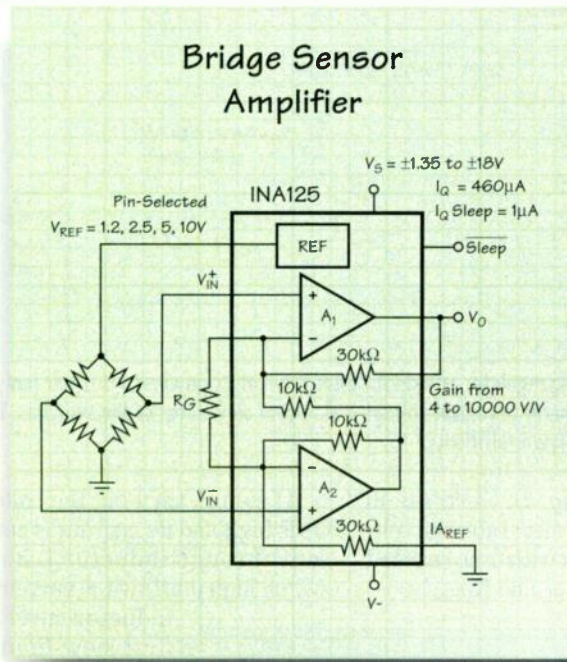
rent-mode switchers, controlling the peak switch current of each oscillator cycle not only regulates the output voltage, but also provides both fast response to input-voltage transients and quick current limiting. The oscillator drives a toggle flip-flop, alternately enabling power transistors (a pair of 0.3- Ω npn power switches). These switches operate in a linear mode and run turned off and in saturation.

According to Jim Williams, staff scientist at LTC, "The magic in the design of this switcher is the local feedback loop each power switch operates in." This loop controls the rate at which npn switches QA and QB transition through their linear regions. Although both of these transistors are loop controlled (operating in their linear region) when switching, they're allowed to turn both fully off and fully on to maintain efficiency. When off or on, the loop is open. The combination of slew control in the linear region and loop recovery from the npn transistors' nonlinear off and on states demands an extremely wideband, well-behaved loop—the chip's "magic."

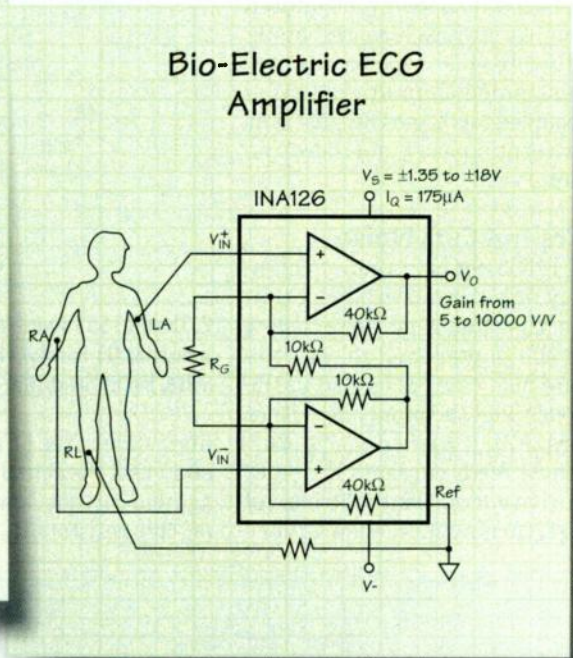
The LT1533 offers the designer a couple of additional noise reducing tricks. For example, the oscillator can be set to run at frequencies between 20 and 250 kHz with external resistors and

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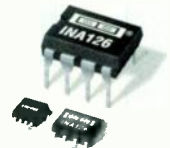
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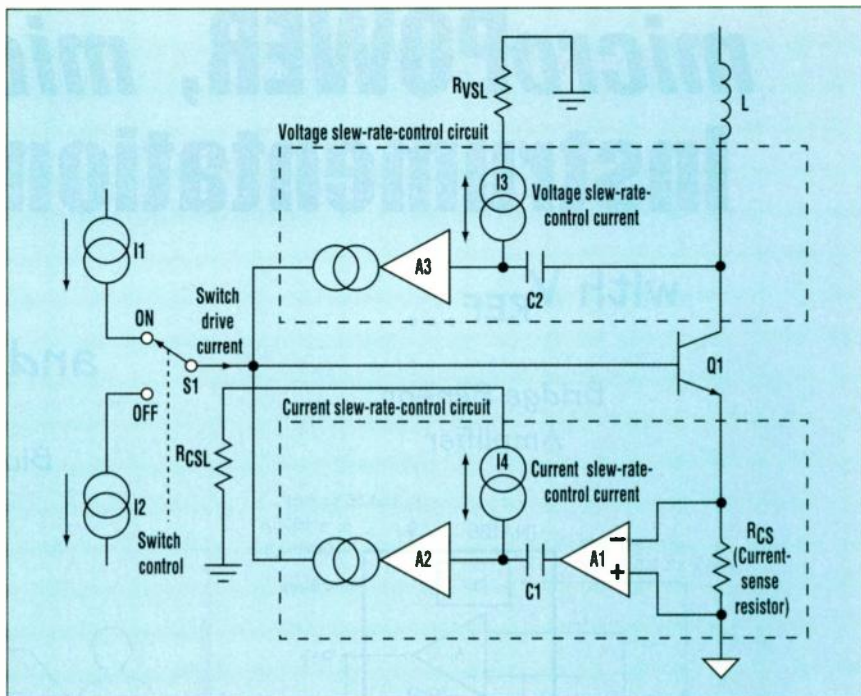
capacitors connected to several pins. This wide range of operating frequencies lets the system designer avoid sensitive frequencies where the oscillator's fundamental or its harmonics may interfere with system operation.

However, to maximize efficiency while maintaining low noise, LTC recommends operating at 40 kHz or lower. Alternatively the oscillator can be synchronized with a system clock to avoid beat frequencies in the audio or subaudio range. In addition, the push-pull converter-circuit topology, facilitated by the pair of switches, represents an inherently low-noise topology. It produces less noise than other transformer-coupled topologies because current flows continuously, and there's no flyback interval.

Slew-Control Cuts Noise

The LT1533 not only reduces high-frequency noise dramatically by controlling both voltage and current slew rates in the power switch, but the technique also controls noise in the catch diodes and the input and output capacitors (Fig. 1, again and Fig. 2).

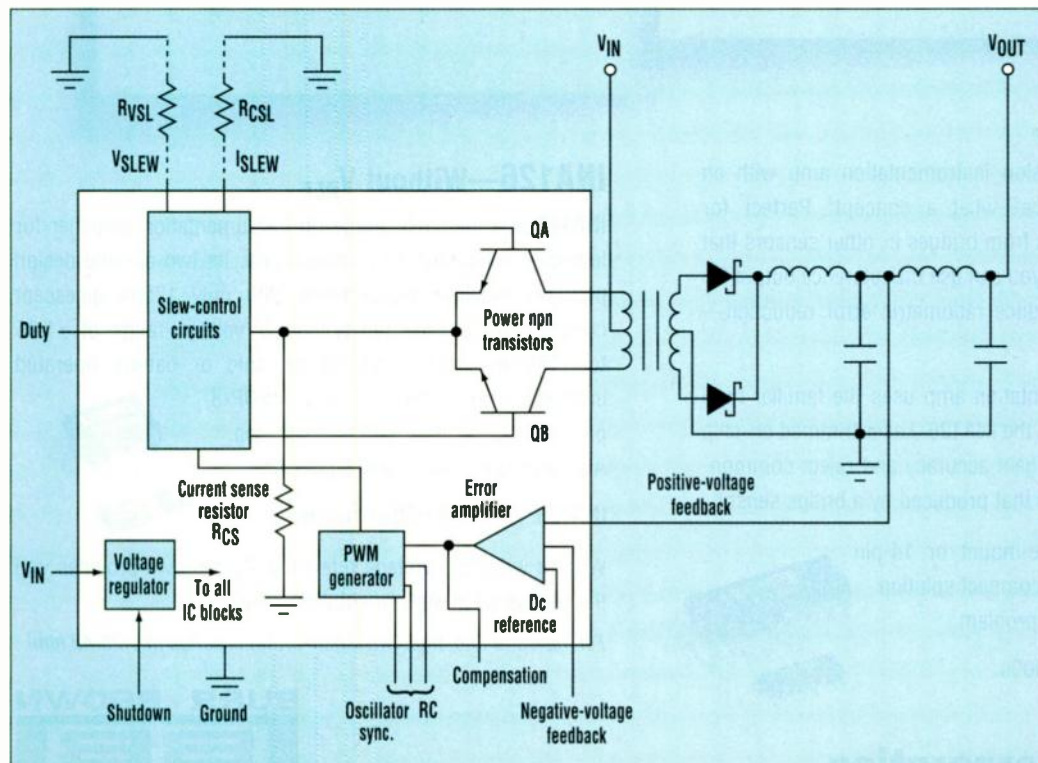
Switch S1 feeds currents I1 and I2 (switch drive current) into the base of switch Q1, turning it on even at very



2. The LTC1533 switching regulator adjusts the base drive of its power-switch pair (only transistor Q1 is shown here) to control voltage and current slew rates of the switches. This cuts noise, but at the cost of lower efficiency.

high slew rates (Fig. 3). Currents I3 and I4 set the actual slew rates for voltage and current slew with user-selected off-chip resistors R_{VSL} and R_{CSL} .

At switch turn-on, the collector of Q1 is high and its current is zero. Current through inductor L holds the switch high until switch current equals inductor current. The



1. This single-chip switching regulator lets a power-system designer cut noise by controlling the current and voltage slew rates of the chip's pair of 1-A power switches QA and QB. Control is accomplished with R_{VSL} and R_{CSL} .

first slew-limiting action occurs as current builds in Q1. Fixed-gain amplifier A1 senses switch current, a function of the voltage across R_{CS} , and amplifies it. As the current through Q1 increases, the circuit generates a current through C1 proportional to the switch-current slew rate. This current is summed with I4 and the difference is amplified by amplifier A2. A2's output current becomes I1, which controls the npn-transistor's current slew rate.

When switch current exceeds inductor current Q1's collector would normally fall low at a rate limited only by diode and switch parasitic capacitance. To control voltage slew

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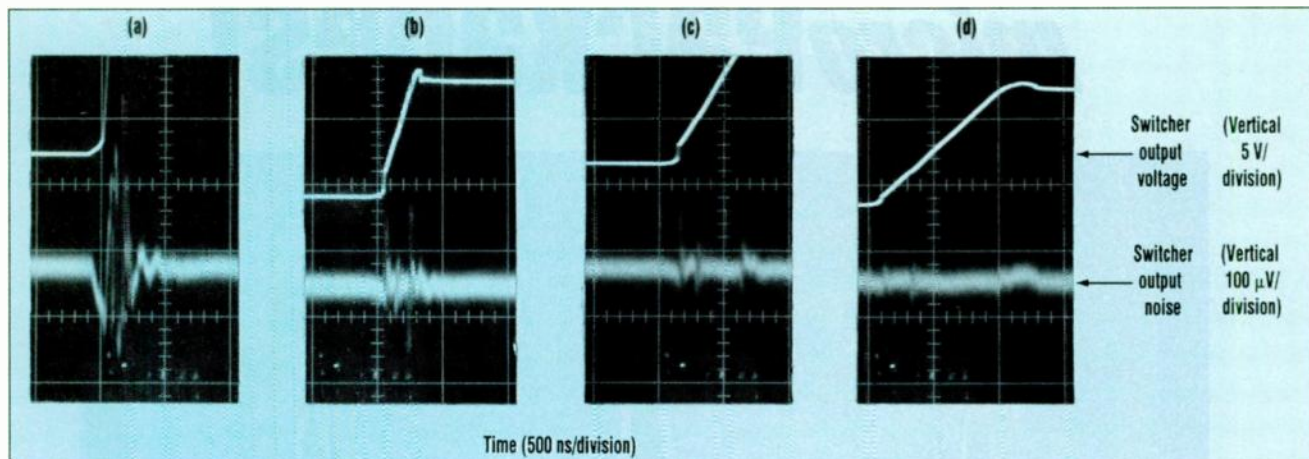
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4. Switching noise (lower trace) is reduced to virtually zero (d) from over $400 \mu\text{V}$ (a) by decreasing the slew rate (upper trace).

rate the current through C2 is summed with I3 and the difference amplified by A3. A3's output clamps the base current of Q1, stopping its rise—in turn stopping any rise in Q1's current—and forcing the switch voltage to fall at a controlled rate.

When Q1 turns off, current and voltage must be controlled in the reverse order. Switch S1 flips to provide reverse base drive, and the polarity of I3 and I4 are reversed. Almost immediately, switch current falls slightly below inductor current. Under normal conditions this action would cause the switch voltage to slew up, limited only by diode and switch capacitance. C2 senses voltage slew and A3 controls switch base drive, limiting switch rise time. Switch current remains essentially constant during voltage slew.

When switch voltage reaches the level where the catch diode turns on, switch current normally drops rapidly. This action creates fast B-field transients around the switch, diode, and output capacitor lines. A1 and C2

"The magic in the design of this switcher is the local feedback loop each power switch operates in."

come into play at this time. They sense the decreasing switch current and control the base drive via A2, forcing a controlled decrease in switch, diode, and capacitor current. The phenomena described here is best understood with a figure showing relative switch waveforms operating with controlled switch drive. Current and voltage-slew limiting do not occur simultaneously. One must take over after the first is completed. This function demands a very fast-responding control loop to avoid crossover glitches that would create additional noise spikes.

These four oscilloscope pictures

were taken at four different switch slew rates (upper traces) ranging from over $100 \text{ V}/\mu\text{s}$ (a) to $10 \text{ V}/\mu\text{s}$ (d) (Fig. 4). In Photo A, the noise is over 0.4 mV peak. Cutting the slew rate has reduced it to below 0.050 mV peak, which is about the equivalent of the noise from a $50\text{-}\Omega$ resistor in a 100-MHz bandwidth.

Like most converters today, the LT1533 carries a full suite of self-protection features. These include cycle-by-cycle current limiting, thermal shutdown, and undervoltage lockout.

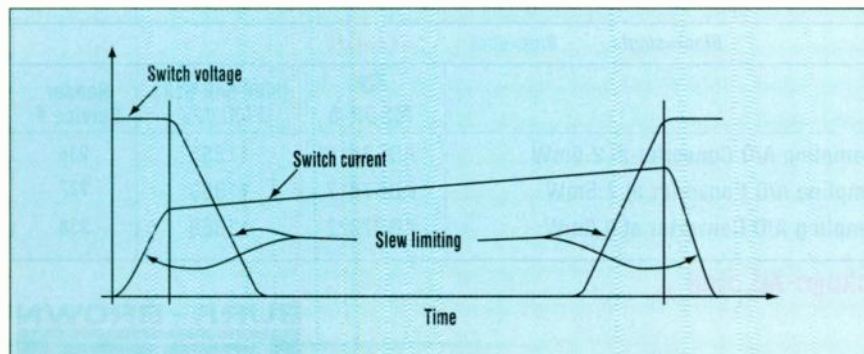
While Figure 1 shows the output connected to the positive-voltage feedback pin, this converter can handle negative output voltages by bringing negative feedback from the output to the negative-voltage feedback pin. Tying the Duty pin to ground overrides the PWM and other control circuits, and produces a 50% duty-cycle waveform at the collectors of the power switches. Slew-rate control, however, is in effect.

An internal linear regulator lets the LT1533 run off 2.7 V to 25 V , and it typically needs 9.2 mA from the supply rail. Under shutdown conditions it typically needs less than $20 \mu\text{A}$.

PRICE AND AVAILABILITY

The LT1533 comes in a 16-lead SOIC. Devices are available rated for commercial and industrial temperature range operation. Pricing in quantities of 50,000 starts at \$3.75.

Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035; contact Jim MacDonald, (408) 432-1900, ext. 2361. CIRCLE 525



3. The current and voltage slew-rate-limiting circuits on the LT1533 do not operate at the same time. At turn-off, the current limit goes first, followed by the voltage limit.

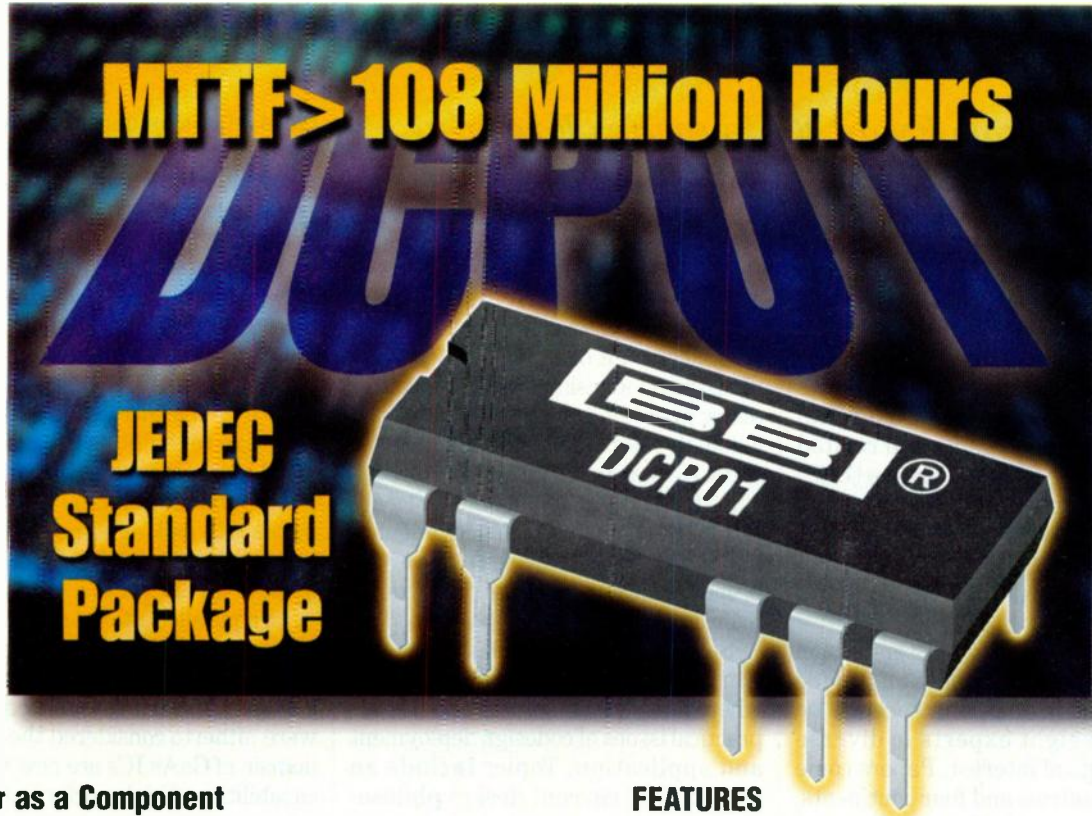
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DCP010515DP	5V	±15V	75%	1000Vrms	400kHz	14-Pin PDIP	11356
DCP011512DP	15V	±12V	76%	1000Vrms	400kHz	14-Pin PDIP	11382
DCP011515DP	15V	±15V	76%	1000Vrms	400kHz	14-Pin PDIP	11382
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RF And Analog Dominate This Year's European Solid State Circuits Conference

Presentations From 20 Countries Examine Leading-Edge Device Developments.

Peter Fletcher

It has been 20 years since the annual European Solid State Circuits Conference (ESSCIRC) was held in Southampton, England. Back then, the focus was very much on the digital world of data processing and related topics. At this year's conference (ESSCIRC '97), a large proportion of papers selected for presentation, both orally and in poster sessions, relate to radio-frequency (RF) and analog topics (see the program grid).

Some 72 oral and 23 poster-session papers were selected from a total of 185 submissions. In addition, there will be talks from eight experts in diverse fields of topical interest. Papers come from 20 countries and four continents, 25% of them outside Europe. Technical Program chairman W. Redman-White points out that a noticeable feature of the conference is the large number of papers covering both analog and digital topics that relate to communications and high-frequency applications.

The conference takes place at Southampton University, Sept. 16-18. On Monday, Sept. 15, there's a workshop on "Hardware and software codesign" and a tutorial on "RF receiver design." On Friday, Sept. 19, another codesign workshop on "Low-power and low-voltage design" will take place.

Jean-Marie Laporte from the Open Microprocessor System Initiative Management Office (OMIMO), the organizer of the workshop, says that one accepted definition of "system level integration"—devised by market analysts at Dataquest—is an IC with one computer engine, "significant" on-chip memory, and over 100,000 used gates. He comments, "Devices that are currently being developed make that definition look pedestrian."

Laporte's more modern definition is that of a device that crosses the boarder

between being a "logic IC" and an "integrated system" when it contains a substantial amount of embedded software. "This seemingly simple addition causes many problems, since it changes the whole development paradigm," he asserts. He maintains the inclusion of software forces the deployment of "codesign"—the concurrent development of hardware and software to allow the proper management of the time it takes to bring such a product to market.

Seven papers in Monday's codesign workshop are followed by a session where audience and presenters discuss practical issues of codesign deployment and application. Topics include an overview of current design philoso-

phies and techniques, the use of codesign principles in the development of reconfigurable computers, and reuse of hardware and software intellectual property (IP) objects.

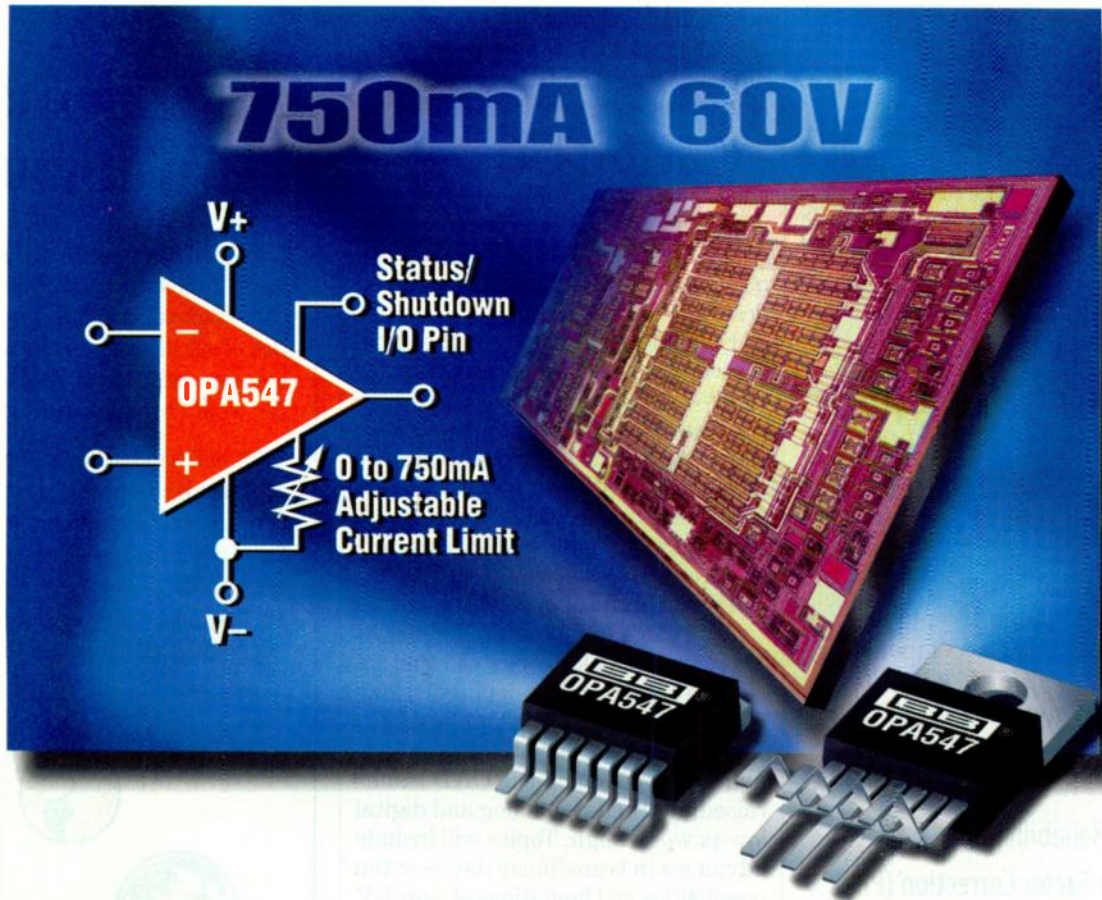
Two papers will cover practical aspects. One sets out problems encountered during the design of a GSM telephone baseband processor chip with both RISC and DSP cores. The other describes the successful application of codesign techniques to an embedded solid-state system for a complex telecommunications application. A final paper will look at some of the design tools that are available for deployment in codesign projects.

In a parallel tutorial session, RF design aspects will be thoroughly thrashed out under the leadership of Peter Mole of Nortel, U.K. He says that circuits that were hitherto considered the exclusive domain of GaAs ICs are now within the capabilities of high-performance silicon

ESSCIRC '97 TECHNICAL PROGRAM

Time and day	Session	Session	Session
Mon. Sept. 15	Workshop: Codesign (10:00 a.m.-12:15 p.m. and 1:30-3:00 p.m.) Tutorial: RF design (11:00 a.m.-12:15 p.m. and 2:00-5:30 p.m.)		
Tues. Sept. 16 9:15-10:00 a.m.	Invited paper Taking DRAM from 4 Mbytes/s to 4 Gbytes/s		
10:30 a.m.-noon (1:45-2:15 p.m. for session 1.1)	1.1 Low-frequency analog I	1.3 Data converters I	1.5 Digital communications circuits
2:30-3:40 p.m.	1.2 Oscillators and PLLs	1.4 Mixed-signal systems I	1.6 Logic circuits I
Wed. Sept. 17 9:15-11:00 a.m.	2.1 RF analog I	2.4 Data converters II (to 10:30 A.M.)	2.7 Memories I
11:15 a.m.- 12:15 p.m.	2.2 RF analog II	2.5 Neural and fuzzy logic (from 10:55 a.m.)	2.8 Memories/DSP
2:45-4:30 P.M.	2.3 RF analog III	2.6 Sensor interfaces I	2.9 Low-frequency analog II
Thurs. Sept. 18 9:15-11:00 a.m.	3.1 Oscillators and PLLs II	3.5 Analog filters I (to 10:30 a.m.)	3.9 DSTP architectures (to 10:30 a.m.)
11:15 a.m.- 12:15 p.m.	3.2 Oscillators and PLLs III	3.6 Analog filters I (to 12:30 p.m.)	3.10 Mixed-signal systems II
2:45-3:30 p.m.	3.3 Sensor interfaces II	3.7 Modeling and matching I	3.11 Logic circuits II
4:05-5:00 p.m.	3.4 Sensor interfaces III	3.8 Modeling and matching II	3.12 Logic circuits III
Fri. Sept. 19	Workshop: Low power/low voltage (8:30 a.m.-12:15 p.m. and 2:00-3:30 p.m.)		

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bipolar technology. Also, fine-line CMOS processes also are capable of producing ICs suitable for RF applications.

Mole explains, "The tutorial is aimed at looking at what performance is required in the receiver of a modern digital radio and what circuit design techniques are needed to implement key low-noise amplifiers (LNAs) and mixer blocks in both silicon bipolar and CMOS technologies." Design requirements will be presented from the point of view of a radio equipment manufacturer, while design issues raised by these requirements will be tackled from the IC designer's perspective.

Five intensive papers will be presented, covering the design of bipolar receivers; the developments of the input transistor in a bipolar mixer; the design of CMOS receivers; and mixer design with special consideration on the effects of topology on noise, intermodulation, compression, isolation, and power consumption. A fifth paper will be forthcoming under advisement.

At week's end, Joe Borel of SGS Thomson Microelectronics will lead another workshop on designing for low-power and low-voltage applications. There will be six papers followed by a panel discussion on the CAD issues raised by trends in analog and digital low-power design. Topics will include advances in translinear devices; the possibilities and limitations of sub-1-V operation of CMOS devices for very low-power circuits; low-power RF design; the design of a digital signal processor for operation at 1 V; high-level low-power design methodology, and power estimation of reconfigurable IP blocks.

Full conference details and accommodations can be obtained from the Local Secretariat, ESSCIRC '97, Dept. of Electronics & Computer Science, University of Southampton, Southampton Hants S017 1BJ, U.K.; +44 1703 592733; fax: +44 1703 593029; e-mail: jlc@ecs.soton.ac.uk. Details also are available on the conference's World Wide Web site at <http://www.esscirc.org>. Attendees can make arrangements on-line at <http://www.webc.co.uk/conference>.

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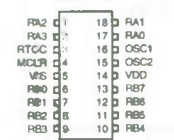
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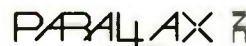


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We've Seen The Future, And It Lies In DVD

DVD Offers A Capacity That's Near 10X Over CD-ROM In Its First Implementation, With Even Higher Capacities Just Over The Horizon.

Richard Nass

DVD—it has the potential to replace the existing tens of millions of CD-ROM drives as well as the tens of millions of VCRs. But the big question is, when? The first PC-based drives are starting to ship and the consumer models are already on the shelves.

Many consider DVD to be the replacement for CD-ROM. Considering its specifications, that seems like a likely scenario. However, CD-ROM makers aren't resting on their laurels. In fact, those drives continue to evolve at an astounding pace (see "CD-ROM Designers Forge Ahead," p. 58).

CD-ROM offers a 650-Mbyte capacity, compared to 4.7 Gbytes for the first generation of DVD. DVD will quickly evolve to 9.4 Gbytes, as drive makers learn to utilize both sides of the disk. There's also an 8.5-Gbyte double-layer specification in the works that would evolve to 17 Gbytes when both sides of the sides are used.

Like CD-ROMs, DVD drives will find a place in both PCs and consumer-electronics boxes. Hopefully, by then, most of the political issues that have plagued DVD to this point will be behind us (see "DVD Must Conquer A Whirlwind Of Issues," p. 54).

In the PC-based units, drive and system makers agree that further integration is required to make the DVD drives more cost effective. The same is true for the consumer units, which can be had for around \$500. Widespread acceptance will come when they hit around \$200. According to most estimates, that price drop should occur by the end of 1998.

There are essentially three types of DVD implementations. One is the complete hardware so-

lution, where all the audio and video decoding is handled by dedicated hardware. The second is the hardware-assist method, where a general-purpose processor handles all or part of the decoding. An example of this implementation is an MPEG decoder working on the video portion while the host CPU is dedicated to the audio data (MPEG-2 is the chosen compression algorithm for DVD data). The last implementation is the software-only version, where all the decoding, both audio and video, is run on the host CPU.

The software alternative is by far the most cost-effective, as it takes advantage of hardware that's already resident in the system. However, it requires most or all of the host CPU's bandwidth. In extreme cases, the processor isn't powerful enough to handle the DVD data streams. In these cases, the video can become fuzzy, jerky, or unsynchronized with the audio. In most instances, a higher-end Pentium II microprocessor would be required, and the video shouldn't contain any "killer bit streams." Otherwise, the video quality could be jerky, where fewer than 30 frames/s can be displayed.

There are some applications that are suited to software-based DVD, where video quality isn't of the utmost importance. Zoran Corp., Santa Clara, Calif., offers a software flavor of DVD called SoftDVD. According to the company, SoftDVD can be a viable solution when bundled with the Pentium II-equipped systems that will be available by the end of the year.

The MPEG committee designated a series of bit streams that are designated as killer bit streams,

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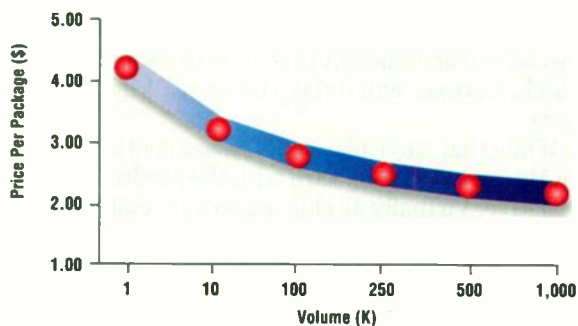


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which are used for evaluation purposes. They typically require a huge amount of overhead processing and additional memory bandwidth to maintain the 30-frame/s rate as well as the synchronized audio and video. The most common killer bit stream is one where a large amount of motion vectors are passed from one frame to another.

According to Darren Neuman, director of engineering for DVD Prod-

ucts at LSI Logic, "The way the disks are encoded, you can't control what the bit streams are going to look like when they come off the disk. They can come off as relatively normal streams for most of the disk, but for a high-motion sequence in a movie, all of a sudden the player breaks up. The software solutions will have a hard time because our estimates show that it's about 10 times harder to decode killer bit streams

than normal bit streams."

Most of the drives that are shipping today are built with a five- or six-chip solution. One of the top priorities of the DVD chip vendors is to significantly reduce that number, eventually down to just a single chip. The drives currently available are primarily built with standard off-the-shelf components and a large number of simple ASICs.

The basic building blocks of the

DVD Must Conquer A Whirlwind Of Issues

In the past year, some significant steps have been taken toward the implementation of DVD technology, such as the adoption of the DVD standard. However, progress is impeded by several major issues. For example, since its inception, the DVD Consortium has been stymied by the specter of antitrust. Exacerbating that issue are signs there are factions within the group that are working against it for their own interests. On a positive note, however, the DVD Consortium has done a fine job of standardizing the physical aspect of a DVD disk.

From the broader view, it has become virtually impossible for DVD Consortium members to discuss DVD products, per se, because the entire group would be in violation of antitrust laws. Hence, no one is talking about specific methodologies required to move DVD technology into more cost-effective systems, thereby expanding it into the consumer, computer, and communications sectors.

As a result, chip makers have no other option but to pick up the DVD technology ball and help the industry move as expeditiously as possible. But even within these ranks, there are problematic areas. So-called "point solutions" represent the most prevalent issues for DVD systems designers, essentially because the potential for future design migration is either highly restricted or nil. In these instances, chip makers are supplying multichip solutions with little or no apparent signs of advancing the technology with increased functional integration or a roadmap of how their products will evolve over time. In effect, this lack of planning leaves the DVD systems designer high and dry.

What the DVD systems designer wants to see is a product roadmap complete with functional integration details based on evolving deep submicron technologies. Such a roadmap should include the availability of a low-cost, single-chip DVD solution combining front- and back-end functions with a real-time audio/video Codec chip by early 1999. Around that time, the required level of process integration will be enough to give DVD systems designers more functional integration. Additionally, the cost of DVD system electronics content, which accounts for about 70% of the total system's cost, will be

lower.

Another trouble spot is DVD copy protection. Currently, though, the Copy Protection Technical Working Group (CPTWG) is expected to look favorably on a Matsushita draft to support the inclusion of watermarking technology in all DVD systems by 1999. Watermarking is the term coined for embedded, imperceptible, unremovable information in multimedia data.

In return for agreeing to the watermark provision, the CPTWG, composed of executives from Hollywood movie studios and computer and consumer electronics makers, surrendered to the PC industry's demands for a software-based Content Scrambling System (CSS). But the catch is that PC makers won't move forward until they are granted a license to implement CSS descrambling in software on a PC. Even if that occurs, Hollywood will be subject to hackers and the resulting losses of major revenues from theft of their intellectual properties. Consequently, it's highly probable that Hollywood will be reluctant to release titles on DVD media, which, in turn, will delay the overall industry even more.

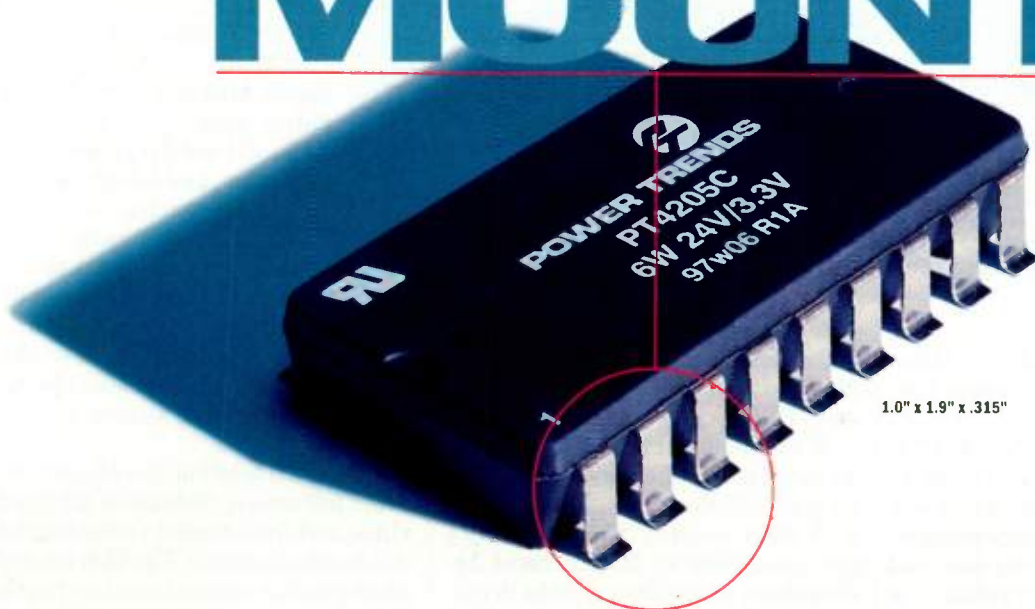
While that particular set of issues continues to brew, OEMs are moving forward with the hardware-based alternative. Virtually all chip makers are embracing CSS-descrambling silicon. For example, LSI Logic pairs a standalone CSS chip with its single-chip DVD decoder. By early next year, plans call for integrating CSS into the audio/video decoder silicon, thus providing systems designers more cost savings.

Perhaps the most significant issue DVD systems engineers face is cutting the cost of their designs. The industry's goal is to reduce DVD-player and DVD-PC costs by more than 60% over the next two years. Besides the continuing functional integration and use of deep submicron processes, it'll also be important for chip makers to include in their devices wide design flexibility so that systems engineers can apply those chips in DVD-player and DVD-PC applications, as well as in set-top boxes.

Contributed by Alain Bismuth, director of marketing, DVD Products, Consumer Products Div., LSI Logic, Milpitas, CA; (408) 954-4920.

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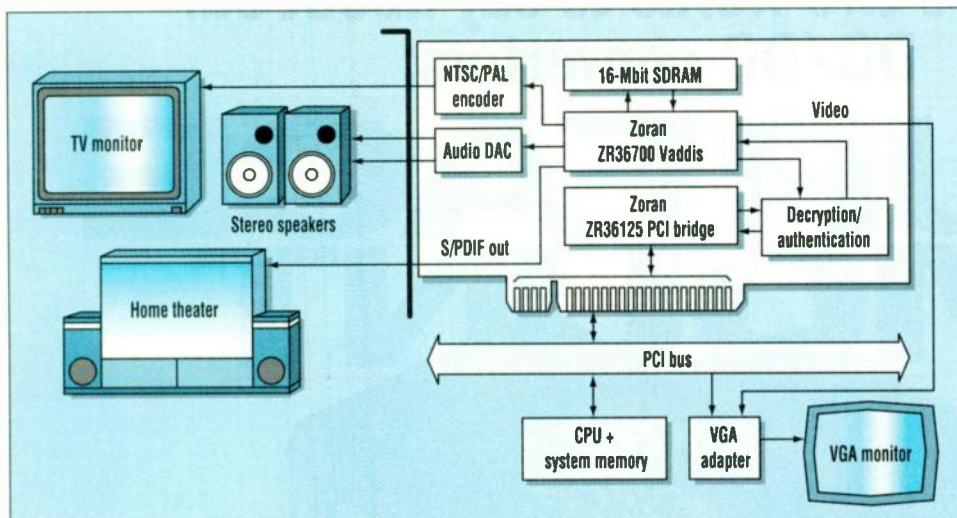
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5W	12V	0.6A	—	PT4204
7W	+5V / -5V	1A ea	—	PT4301
7W	+5V / +3.3V	1A ea	—	PT4302
15W	3.3V	4.5A	—	PT4110
15W	5V	3A	PT4104	PT4101
15W	12V	1.2A	PT4105	PT4102
15W	15V	1A	PT4106	PT4103



POWER TRENDS

READER SERVICE 157



1. A full-blown DVD encoder board can be built with the Zoran Vaddis chip and a small number of other components. It works with one 16-Mbit SDRAM, an NTSC/PAL encoder, an audio DAC, a decryption chip, and a PCI bridge.

DVD drive include an MPEG video decoder, an audio decoder, a copy-protection descrambler, a CPU, a DAC for the audio output, an NTSC PAL encoder for video output, and 16 Mbits of DRAM. The power of the processor is dependent on the feature requirements of the drive. A very-low-end box could get by with a relatively cheap 8- or 16-bit processor. For a high-end box, a mid-range to high-end 16-bit CPU would be required.

All In A Single Chip

A single-chip decoder, developed by LSI Logic Inc., Milpitas, Calif., handles the functionality of the five-chip solutions, including MPEG-2 audio and video decoding, Dolby Digital or AC-3 audio decoding, picture- and letter-box decoding, on-screen graphics, and system parsing. One of the key features of the LSI L64020 is that it operates with one 16-Mbit synchronous DRAM. This design produces a lower overall cost compared to the traditional four 4-Mbit DRAM chips.

For the "no-compromises" platform, Zoran also offers a hardware-based solution, based on the Vaddis DVD encoder (the ZR36700). The part handles the audio and video portions of DVD in a single chip. Like the LSI Logic part, it works with one 16-Mbit SDRAM. The Vaddis' embedded programmable DSP core can execute up to 40 MIPS. To build a DVD system using the Vaddis chip, designers need only add an

NTSC/PAL encoder, an audio DAC, 16 Mbits of SDRAM, a decryption chip, and a PCI bridge (Fig. 1).

SGS-Thomson Microelectronics, Lincoln, Mass., offers a pair of single-chip MPEG decoders. The STi3540 and 3560 employ the company's patented Memory Management Architecture, which allows for the decoding of NTSC pictures in just 10.5 Mbits (12 Mbits for PAL). As a result, up to 5.5 Mbits of the 16-Mbit buffer are available for additional bit-stream buffering, which helps simplify the PCI interface.

The 3560 is aimed at high-end, full-hardware implementations, while the 3540 is targeted toward lower cost systems because it requires the audio decoding to be handled in software. Because the two devices are pin-com-

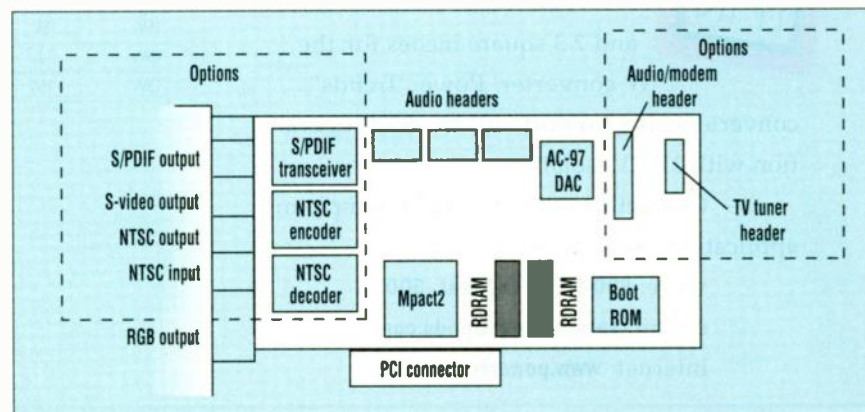
patible, designers can develop two similar boards aimed at different price points.

Containing the functionality to handle both 3D graphics and DVD, the Mpact2 multimedia processor hails from Toshiba America Electronic Components Inc., San Jose, Calif. As the second-generation part, the Mpact2 (TC80310SB) can process 7200 MOPS, which allows it to handle MPEG-1 and MPEG-2 video, high-end wave-table audio, 2D and 3D graphics acceleration, and telephony and videoconferencing functions. The multimedia functions are enabled by the Mpact2 mid-aware software, developed by Chromatic Research Inc.,

Sunnyvale, Calif. Because the Mpact2 is software upgradeable, its features can evolve as new code is developed.

As a DVD solution, the Mpact2 delivers full-screen, 30-frame/s MPEG-2 video, and five-channel Dolby Digital AC-3 audio decoding. The high level of functionality comes from the part's DSP core as well as the use of dual concurrent Rambus channels, which allow for a 1.3-Gbyte/s bandwidth (Fig. 2). Samples of the Mpact2 are available now, with production slated for October.

Toshiba America's Consumer Products Div., Wayne, N.J., also is responsible for a consumer-level (non-PC) DVD player. The SD2006 contains outputs for S-Video, component video, AC-3 digital audio, and standard ana-



2. The Mpact2 chip can be used as both a DVD solution and a 3D graphics subsystem. For the DVD portion, it delivers full-screen, 30-frame/s MPEG-2 video and five-channel Dolby Digital AC-3 audio decoding. The high performance comes from the use of dual concurrent Rambus channels.

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6-Pin Single	CNY17	X	X	X	X
	CNY17F	X	X	X	X
	SFH600	X	X	X	X
	SFH601	X	X	X	X
8-Pin Dual	ILD615	X	X	X	X
16-Pin Quad	ILQ615	X	X	X	X

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READER SERVICE 160



log audio. Like its PC counterparts, it can handle multiple aspect ratios, multiple languages, and clear slow motion and freeze frame.

One of the first systems to ship with

a DVD drive is the Destination, from Gateway 2000 Inc., North Sioux City, S.D. The Destination Big Screen PC/TV employs a traditional PC architecture as well as a cable-compati-

ble tuner for connection to other video sources such as laser-disk players, game machines, or VCRs. Gateway's DVD solution, which plays DVD, standard audio CDs, and CD-ROMs, takes

CD-ROM Designers Forge Ahead

The CD-ROM makers are starting to feel the heat—the DVD manufacturers are breathing right down their necks. In an effort to hold off the competition, the CD-ROM designers continue to push the performance envelope. Two examples are proof of that phenomena: the OTI-9220 four-in-one controller from Oak Technology Inc., Sunnyvale, Calif., and the AIC-9570 Ultra ATA controller from Adaptec Inc., Milpitas, Calif.

The OTI-9220 actually rolls a pair of industry-leading components into one die. It's based on the Oak OTI-912 controller and the Sony CD-DSP processor. As a result, engineers have an easy migration path from previous designs. To further simplify that process, hardware reference designs are available with firmware.

The OTI-9220 packs four functions into one IC. It contains a CD-ROM decoder, a digital-signal processor, a digital-to-analog converter, and a digital servo controller. In addition, it also holds an IDE/ATAPI interface and a 128-kbyte (64 kbits by 16 bits) DRAM buffer (see the figure). The chip supports constant-angular-velocity (CAV) drives at peak data rates up to 20X. Such transfer rates are attainable because the controller supports the PIO Mode 4 and Multiword DMA Mode 2 timing requirements of a 120-ns cycle time for an entire 31-block transfer.

The IC's DSP uses the servo error signals as feedback data to properly position the optical head over the disk. The algorithms run on the DSP also allow the head to quickly jump from track to track upon request. The amplified RF signal from the optical head is routed from the digital phase-locked loop where the clock signal is extracted. The serial data stream is then sent to a demodulator, stored temporarily in RAM, then passed through the error-correction circuitry.

The second controller, the AIC-9570, tops out at a

50X throughput. The part supports the ATAPI interface, as well as the Ultra DMA protocol, which enables host data transfers up to 33 Mbytes/s (double the standard ATAPI rate). The move to 50X was made possible by the use of on-the-fly error correction, a high buffer bandwidth, and automated ATAPI commands. Integrating the error correction directly into the controller increases the data reliability while reducing overall system cost.

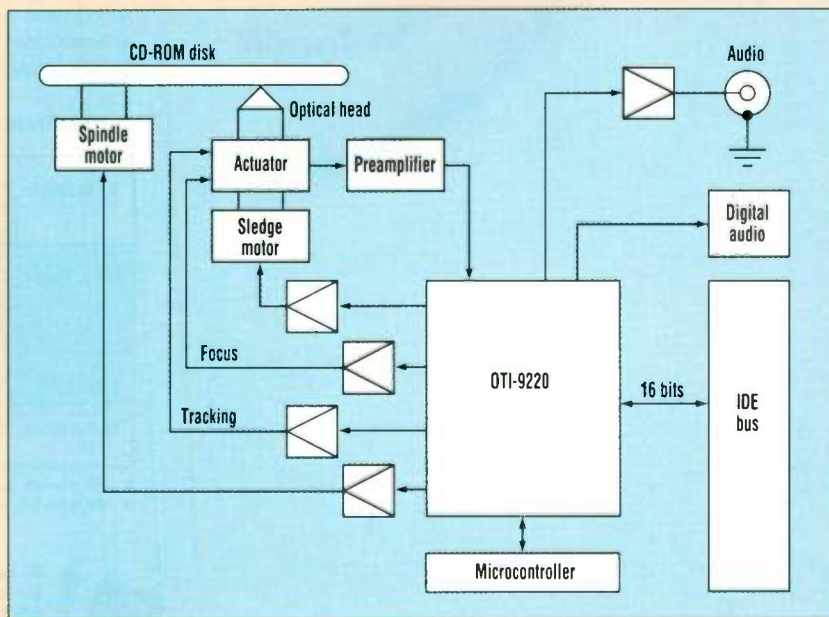
One of the key features of the AIC-9570 is that it provides a migration path to higher performance interfaces, including SCSI and IEEE 1394 (Firewire). The firmware that's bundled with the Adaptec part was developed in a modular, scaleable fashion. As a result, designers can port the code more easily, while moving from a 24X drive to a 50X model. The firmware is based on a single-processor, 24-MHz design with a user-configurable EPROM.

A technique that's called Adaptive Audio Steaming allows the CD-ROM drive to read audio and graphical data at equal speeds, up to 50X. Traditionally, drives

had to slow down to 1X to read the audio data. The spinning up and spinning down of the motor resulted in excess wear, which is now eliminated. Now, the excess data is stored in a buffer until it's needed by the host.

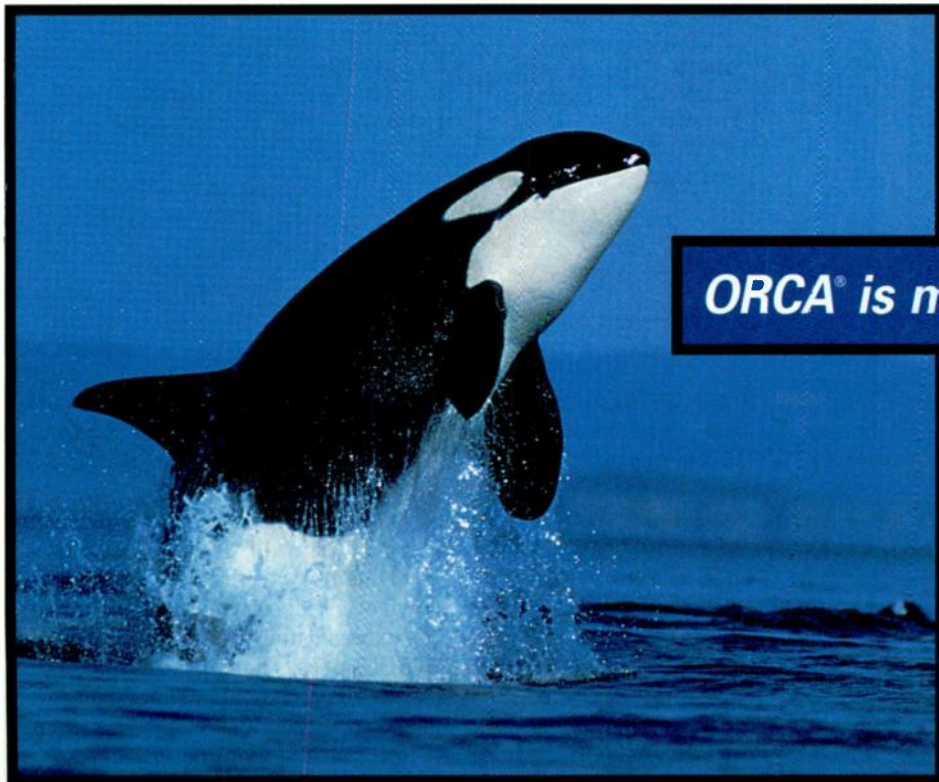
The AIC-9570 chip supports two memory types: EDO and fast-page-mode with a 16-bit-wide interface. The wide interface improves bus utilization, re-

sulting in faster access to information and other peripherals. The integrated frequency synthesizer reduces the number of clock sources needed by the controller. One low-frequency clock source generates the high-speed clocks needed to attain the high buffer bandwidth. It also eliminates the need for a 1X audio clock.



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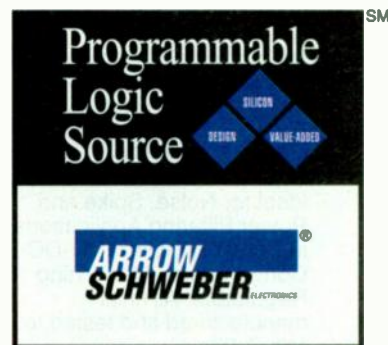
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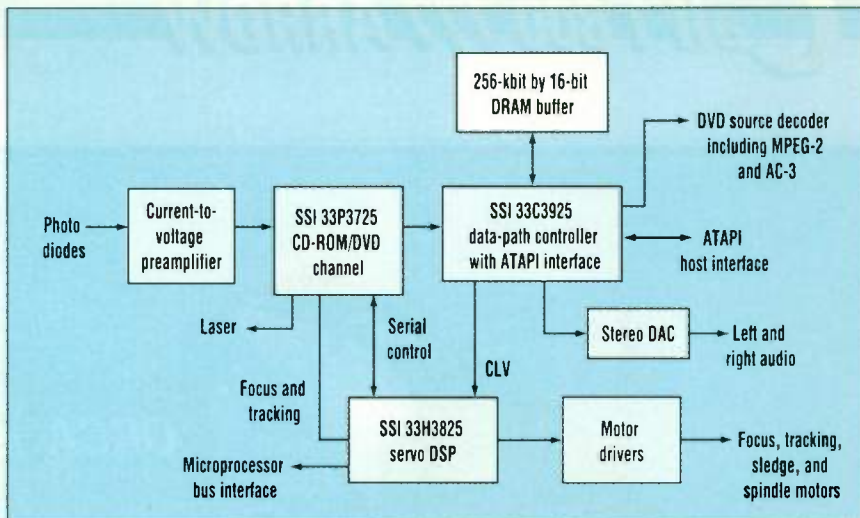


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3. The Silicon Systems DV25 chip set provides the electronics needed to handle the drive-control functions. The three-chip set includes the 33P3725 DVD/CD channel, the 33H3825 DSP servo, and the 33C3925 data-path controller.

advantage of the Mpack media processor. The Destination displays the DVD video in its native 720- by 480-pixel resolution, displaying a crisp, clear video image.

An example of the hybrid hardware/software solution comes from Sigma Designs Inc., Fremont, Calif. The company's REALmagic Hollywood DVD MPEG-2 playback card handles the video portion, while the audio operations are handed off to the host CPU. According to the company, with a system based on a 133-MHz Pentium processor, there's no degradation of audio, video, or the synchronization of the two.

Sigma Designs also has developed an intuitive user interface to control the DVD playback. It comes with interactive menus; instant rewind; fast forward; and search to title, chapter, and track. It also lets the user enjoy multiple aspect ratios—wide screen, letter box, and pan-scan.

DVD Recording

The drives discussed to this point are all classified as read-only, or DVD-ROM. Hitachi America Ltd., Brisbane, Calif., is working on a rewritable, or DVD-RAM, drive. The DVD-RAM drive is compatible with DVD-ROM, but adds the capability of storing up to 5.2 Gbytes of information (2.6 Gbytes on each side of the disk). According to the company, DVD-RAM prices will rival CD-ROM prices by the middle of next year.

Three models will be available from Hitachi, the GF-1000 and GF-1050, which employ ATAPI and SCSI-2 interfaces, respectively. The GF-1055 is an external unit that connects through a SCSI port. The transfer rate on the Hitachi DVD-RAM drives differ depending on the format of the disk employed. For example, a DVD-RAM disk operates at 1.38 Mbytes/s, the DVD-ROM disk runs at 2.76 Mbytes/s, and a CD-ROM disk works at 1.20 Mbytes/s.

While the video and audio decoders seem to get the bulk of the spotlight, the unsung portion of the DVD drive is the drive-control electronics. Developed by Silicon Systems Inc., Tustin, Calif., the DV25 chip set includes the 33P3725 DVD/CD channel, the 33H3825 DSP servo, and the 33C3925 data-path controller. The set contains the major functions required to build a DVD drive (Fig. 3).

Included in the 33P3725 channel are the servo functions, an RF amplifier, automatic gain and laser-power control, synchronization, a data slicer, and a data-recovery PLL. The 33H3825 is based on a Texas Instruments DSP. Its functions include CD and DVD control of focus, an MCU interface, and speed control.

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READER SERVICE 167

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Design Techniques For Plug-and-Play In "Smart Homes" And Consumer Products

Industry Puts Its Weight Behind Standards For Networked Home Subsystems.

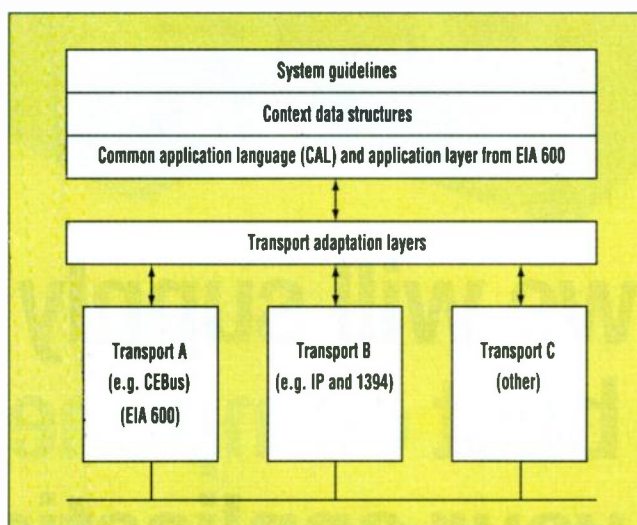
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There is a growing market for household subsystems that use network communications to offer improved features of security, entertainment, energy savings, and convenience. Lighting systems are available that provide a lived-in look; professionally installed security systems are well-integrated; audio and video equipment—marketed in the form of home theater—deliver value to the consumer, and utility companies are providing new levels of energy management choices to the consumer.

All of this sounds rosy, but it would be a lot nicer if these systems were easier to install and worked together more seamlessly. It's also important that these systems have the ability to work on a fast, reliable, ubiquitous network like the power line or at RF. On the contrary, integration today is achieved through expensive custom design and installation, and the average house incorporating such services is 5000 square feet—not the broad market targeted by consumer electronics companies.

A group of manufacturers have come together to create the Home Plug-and-Play (HomePnP) Specification (see "Status of the HomePnP specification," p. XX) The intent of this specification is that standalone subsystems may continue to be delivered as before, but with the addition of HomePnP features so that they may be more easily integrated into a home-



1. Depicted is a home plug-and-play arrangement. The lowest blocks represent the application layer and its associated common application language (CAL) contained in the EIA-600 (CEBus) specification.

control system harmonized with the activities of the occupants.

HomePnP Development

Two factors contributed to the motivation for these companies to develop HomePnP. First, networked products have a more prevalent market presence: Whether manifested as a digital camcorder linked to a PC, or a lighting system that works through the TV remote control, or an Internet browser, the networking boom has reached all kinds of devices. Second, the technology pieces are in place to allow low-cost, high-quality communications to be added to existing products without significantly affecting cost. Differentiating products by the simple addition of a network-communications capability enables new value-added features. These products

can, but don't have to be, "connected-to-the-world" super-appliances and can be truly diverse in the consumer electronics spectrum.

The developers have contributed several key concepts for the creation of a robust home-systems technology. Among the most important breakthroughs are:

- A common device language
- Transport-protocol independence
- Status, listener, and request objects
- Subsystem loose coupling,
- HouseMode and State Vectors
- Configuration processes

HomePnP is noteworthy as much for the problems it does not try to solve as for those it does. Transport-protocol independence is one of the primary goals, and the specification deals with the application layer and higher by addressing three major functional areas. The lowest block represents the application layer and its associated common application language (CAL), contained in the openly available EIA-600 (CEBus Standard), avoiding expensive language translation gateways between products (Fig. 1).

The context-data structures block indicates the extensive product models that have been developed using CAL's syntax, representing tremendous industry consensus-building, by defining the functional product building blocks for security, lighting, environmental, energy-management, util-



DESIGN NOTES

The "Smart Rock": A Micropower Transponder

Design Note 161

Dale Eager

INTRODUCTION

A "smart rock" is a locating device that is buried at a specific site. It is interrogated by a portable source and responds with information about its position, identification number or any data that it has collected since its last interrogation. Ideally, a smart rock, once placed, will wait, listening for its interrogator, for many years, or even for decades. A smart rock buried on a nature trail might send its identification number to a traveler's handheld transponder, which would decode the identification number and play a message describing the surrounding sights. It could also be used to direct the traveler which way to turn at a trail junction. Smart rocks are sometimes placed along the edges of cliffs so that interrogators built into vehicles, such as bulldozers, will cause them to stop before they get too close to the edge.

THE MICROPOWER SUBCIRCUITS

The Oscillator

Figure 1 shows the LTC[®]1440 implementing a micropower oscillator. This circuit provides the references for both voltage and frequency needed in our rock; it draws only a few microamps of battery current.

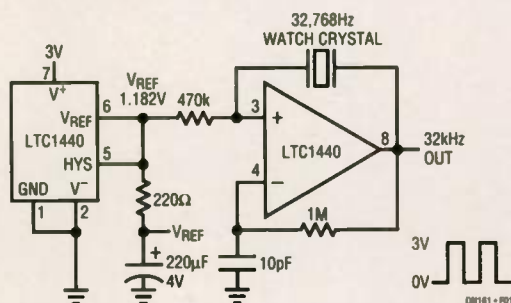


Figure 1. Ultralow Power Crystal Oscillator

IF Amplifier

Figure 2 details the IF amplifier, which has a gain of 2500 at a center frequency of 20Hz. By selecting the LT1495 for our amplifier, we can do this while consuming only 2μA.

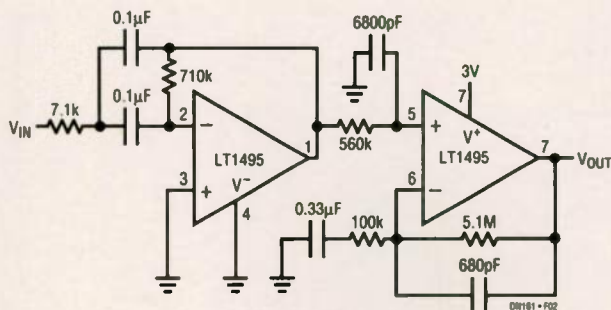


Figure 2. Ultralow Power IF Amplifier (Gain of 2500 at 20Hz)

Power Driver

Figure 3 introduces the LTC1480 ultralow standby power RS485 transceiver. In our rock, we only use the LTC1480 in its transmit mode, where it provides currents of about 100mA. The rest of the time the LTC1480 is shut down, drawing a microampere of quiescent current.

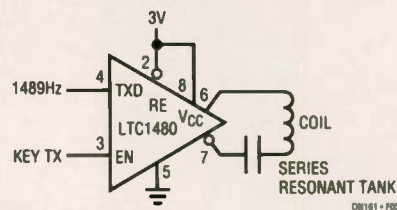


Figure 3. Hefty Driver with Ultralow Sleep Current

THE SMART ROCK SYSTEM

Receiver

The 32kHz reference frequency generated by Y1 and U1B (as shown in Figure 4) is divided by eleven in U2 and by two in U3A to yield 1489.5Hz, the local oscillator frequency. This LO output is applied to mixer Q3 while Q1 and Q2 are fully enhanced, causing C4 and L1 to act as a parallel resonant antenna. The output of the mixer, Q3, is fed into the IF amplifier created by U5A and U5B, where the signal

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is multiplied by approximately 2500. When the signal on U5B Pin 7 reaches 1.2V_{P-P}, Q4 turns on, pulling the START signal line low.

Transmitter

Once the interrogating tone burst is over and the IF amplifier's output has decayed below 1.2V_{P-P}, Q4 stays off and R11 is allowed to charge C11, raising the voltage on the START node. When the threshold of the clock pin of U3B is crossed, the Q output goes high and the \bar{Q} signal goes low. D5 quickly discharges C13, pulling the D pin of U3B low and preventing false retriggering of U3B. D3 pulls the START signal low, preventing an early termination of a transmit cycle caused by IF overload. Q1 and Q2 turn off, causing C4 and L1 to form a series resonant circuit connected to the output of U4 (the power driver). At the same time, U4 is enabled and drives the LO frequency into the series resonant tank circuit. This transmitting action continues until R12 discharges C12 to the threshold of the reset pin (Pin 13) of U3B, at which time the flip flop is reset ($\bar{Q} = 3V$). U4 is disabled and Q1 and Q2 are enhanced.

Blanking

Resetting the flip-flop causes the \bar{Q} output to toggle to 3V, which causes D3 to go into the blocking state, releasing the START signal from its forced low condition. Because the delay of R13 and C13 is longer than the delay of R11 and C11, U3B is clocked into the off state ($\bar{Q} = 3V$, the state in which it already exists) as the START signal goes through the clock pin's threshold. Meanwhile, the IF amplifier's output is decaying from the disturbance of transmitting. It decays to well below 1.2V_{P-P} before R13 charges C13 to the threshold of the D pin of U3B. This prevents false tripping while waiting to enable the reception of the next interrogation signal.

CONCLUSION

It is easy to design circuits that, when powered by a single lithium cell, will last for years or even decades while performing real-world significant functions. Linear Technology offers an extensive line of nanopower ICs, including precision operational amplifiers, comparators, voltage references, analog-to-digital converters and line drivers and receivers.

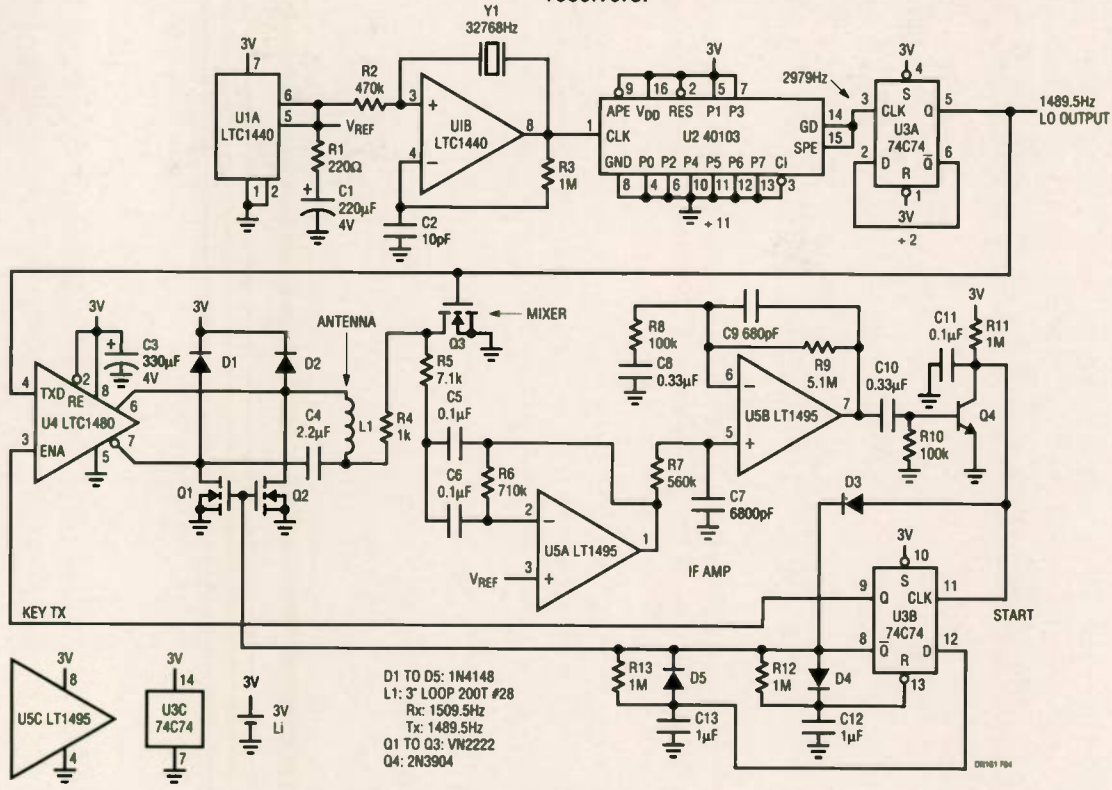
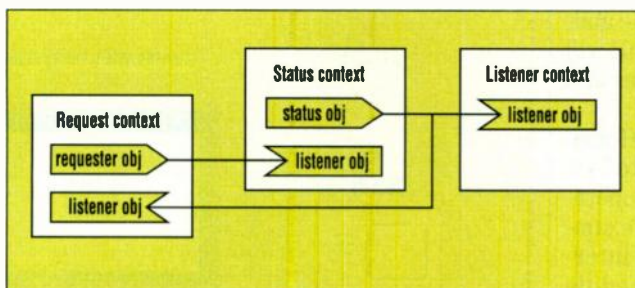


Figure 4. (Lapis Orbus Astutus)

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ity, computer, and entertainment applications. Shown in the top block are the system guidelines that codify many of the device behaviors necessary to build installable products. These guidelines cover some difficult subjects that have not been previously addressed.



2. Within the common application language (CAL) of the EIA-600 specification there are three formalized object types — Status, Listener, and Request objects. In a smart-home system involving the home's air-conditioning system, the request causes the air conditioner to change state which in turn is announced by the Status Object and received by all active Listener Objects.

Single Protocol

HomePnP allows manufacturers to use a single-application protocol and to separately select an appropriate, independent, transport net-

work (there may be more than one in the home). The application layer expects certain services to be provided by the underlying transport. Since HomePnP is intended to run on established consumer electronic protocols, such as CEBus and IEEE 1394 (FireWire), the demands on the underlying transport are minimal.

Although CAL has always been an object-oriented language, HomePnP has formalized three object types—Status, Listener, and Request Objects, which form the basis of inter-subsystem interoperability through an HomePnP characteristic; Loose Coupling, in which subsystems report status information to all other interested HomePnP subsystems, allowing designs without specific knowledge of other vendors' products. For example, a security system might be designed to provide a warning if the air conditioner is activated while the windows are open. Without Loose Coupling, the security system would have to understand the cooling system in enough detail to interrogate it.

With Loose Coupling, the security system simply includes the appropriate Listener Object from the environment monitoring which, by default, receives reports from the air conditioner; allowing the security system to use this information—or not—according to its own design.

In the above example, the cooling-mode status change may have resulted from direct-user input or a timer expiration. It also is possible to effect a status change over the network through a Request Object. In this example, a PC may include an environment Request Object that is

loosely coupled to the air conditioner and can activate it by transmitting a message using its own application software. The request causes the air conditioner to change state which, in turn, is announced by the Status Object and received by all active Listener Objects. Such connections are depicted using icons (*Fig. 2*).

Another important tool for home-system integration is the notion of a State Vector; in particular, one titled House Mode that reflects the user's operating goal for the house, which is shared by subsystems. The information for these vectors is abstracted from the details of the subsystem and is hierarchical, with the first defining element of the House Mode being the state, which can be Occupied, Unoccupied, or Uncertain, and the second being probability, with the two possible values of certain and probable. The remaining three elements are house-state modifiers that add increasing details to the desired operating state of the house.

The hierarchical nature of House Mode is reflected in the fact that a listening device can parse the vector and operate at its own level of understanding. Even though the Status Object may be reporting a House Mode as occupied: certain: asleep: 55 minutes remaining, the lighting subsystem may operate some lights based solely on the occupied versus unoccupied state. Another subsystem might make use of the full vector to warm the house before the occupants awake.

Installation And Configuration

The remaining area in which the HomePnP design has paved the way

for advanced home systems is to provide device-installation tools for more complex configurations, but not requiring them for the majority of consumers who will start small and add to their system incrementally.

The configuration process can be divided into three phases. The first configures devices for basic communication dealing with the "leaky" nature of the two most popular media: Power-line carrier and RF. Because packets from one house could potentially

be overheard by devices in a neighbor's house, special handshaking steps are taken to avoid house-to-house interaction.

The second phase allows devices that contain Status Objects to ask the network for a unique instance number to assign to that status, necessary for cases where there may be more than one provider of a status. For example, consider a clock that is available on the network and a second time provider is installed. The second provider gets the chance to ask if there is another clock, and when the first declares its presence, the new provider asks for the next instance to become the second provider of time.

The third configuration phase allows devices containing Listener Objects to ask for the availability of matching status objects, constituting what HomePnP calls automatic binding. Continuing the clock example, a VCR containing a time Listener Object is installed after the above referenced clocks are on-line. During configuration, the VCR broadcasts a query for available time providers and, generally, it would bind to the first instance of time; the query can contain qualifiers, however, so that the listener can bind to a particular type of provider. For example, the VCR might first ask for direct-broadcast-satellite-time before accepting any time that is available.

Other topics being dealt with by HomePnP are:

- **Grouping products:** Geographical zoning, scenes, and even multifamily dwellings are to be covered.
- **Scheduling:** One of the better utili-

ties of networked products is the ability to schedule events. HomePnP will provide detailed data structures and editing techniques.

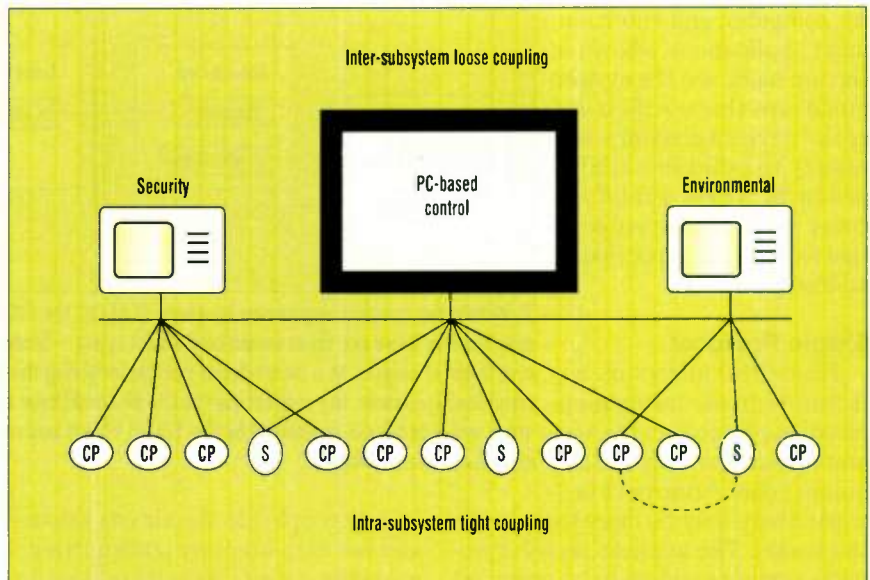
- **Locking:** One of the tools that HomePnP will provide is the ability to lock all or part of a device for certain operations. Locking is important, for example, to prevent a product from interfering with a complicated schedule creation that is taking place over the network.

- **Security and privacy:** Applications require several levels of security commensurate with the protection needed and the complexity that can be afforded. At the more robust end of the spectrum are utility energy-management systems and security systems, usually requiring both authentication and encryption. Convenience products typically need only simple anti-spoofing protection. HomePnP will address the security issues in detail.

- **User interface:** Another advantage to be gained from networked products is the ability to create distributed-user interfaces. HomePnP also will define user-interface contexts and objects to allow interoperability with other HomePnP devices.

Getting Started With HomePnP

The first step is to consider the most likely transport protocol for your



3. Concepts such as subsystem Loose Coupling in a HomePnP architecture for smart homes allow a natural layering of device complexity.

products. Although any transport protocol will support HomePnP, most companies are targeting either CEBus or FireWire. Next, think about your product's position in the overall hierarchy created by HomePnP. Concepts such as subsystem Loose Coupling allow a natural layering of device complexity (Fig. 3). Subsystem controllers in the inter-subsystem Loose Coupling region tend to be more advanced in both their communications

needs and their local processing requirements. Sensors (S) and control points (CP) populate the intra-subsystem region. These devices are simpler, numerous, and highly cost-sensitive.

Some Early Products

Intellon Corporation has created a family of CEBus-compatible power-line ICs for the HomePnP market. The SSC P400, with a parallel host interface, supports all of the CEBus

Status Of The HomePnP Specification

Honeywell, Intel, Interactive Media Systems, Microsoft, Smart Corporation, and Thomson Consumer Electronics initiated the work to define HomePnP. It has now been embraced by dozens of companies that are contributing to its development and completion, allowing it to be published by the CEBus Industry Council (CIC) as a provisional specification on March 31, giving manufacturers a chance to build and test products in a "Plugfest" environment.

The first Plugfest will take place next month and will allow product vendors an opportunity to test both their HomePnP implementations and the HomePnP Specification. Feedback from this Plugfest will be incorporated in Release 1.0 to be available in September. Additional Plugfests are planned as new HomePnP products become available. Products under development by CIC members for the first Plugfest include: Energy management, environmental control, lighting, and PC-based products.

The CIC is an organization incorporated as a nonprofit

corporation to develop and enlarge the market for products compliant with the CEBus Standard and/or the common application language (CAL) as implemented in the HomePnP specification. The Council maintains the value of its certification marks while facilitating interoperability among products, and with multiple-transport protocols through the maintenance of the standard and specification, its application database, product testing, and conformance certification.

For more information on the development of the HomePnP Specification or on the Interoperability Technical Committee, contact the CIC by phone, (317) 545-6243; e-mail, cebus-staff@cebus.org; or on the World Wide Web at <http://www.CEBus.org>. For more information on Intellon's family of CEBus compatible power-line ICs for the HomePnP market, contact the company at (352) 237-7416, or on the Web at <http://www.Intellon.com>. Domosys Corporation can be contacted by phone at (418) 681-8022; e-mail, info@domosys.com; or on the Web at <http://www.domosys.com>.



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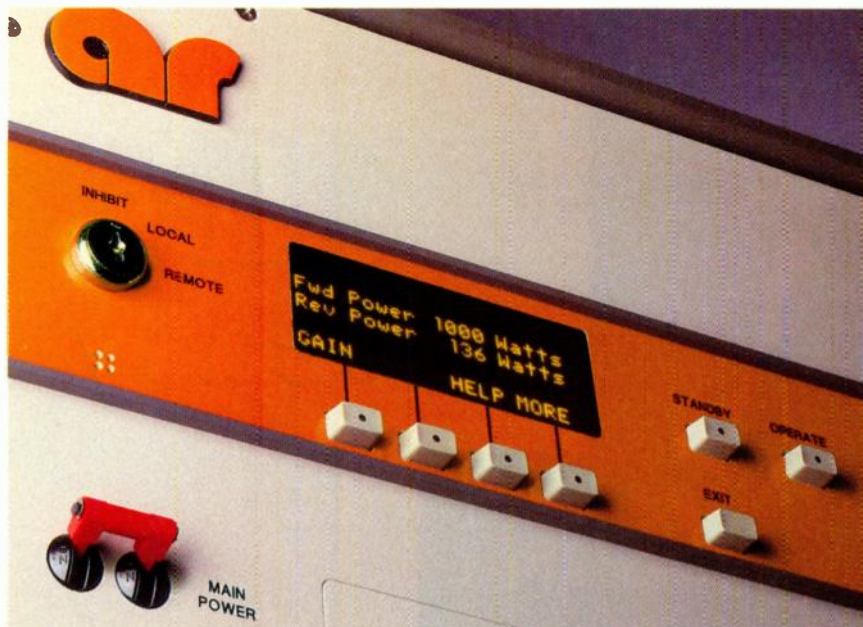
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Domosys Corporation, Quebec City, Quebec, Canada, is developing a CEBus-compliant power-line carrier IC. Known as the CEWay, it integrates the lower two layers (Physical and Data Link) of the CEBus Standard. This chip is scheduled to be available in the third quarter. In addition, Domosys' CEBox software system for product developers—released last December—is being upgraded to include the HomePnP Specification. CEBox is intended to bring the easy development of both CEBus and HomePnP products within the reach of all developers.

The authors are the co-chairs of the CEBus Industry Council Interoperability Technical Committee.

Larry Stickler is the program manager of Home Plug and Play at Honeywell Corporation. He has been with Honeywell for 11 years, and has holds and MSEE from the University of Illinois, Urbana-Champaign.

Brian Markwalter is the director of strategic marketing at Intellon Corporation. Prior to joining Intellon, he was a staff engineer at the Electronic Industries Association (EIA). He is a graduate of Georgia Institute of Technology, Atlanta, earning both a BS and MSEE.

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Continuous enhancements in IC technology enable a wide variety of new, smaller systems to deliver higher performance with lower power requirements than ever before. To take advantage of the IC improvements, designers must provide new supply voltages: 3.3 V for now, and 2.5 V in the near future. In many cases, components that use these lower voltages must be employed side-by-side with older, 5-V parts. These mixed-voltage environments could create a variety of design challenges, especially when using digital circuits that may not be specifically designed to operate in mixed-voltage environments.

For the past 30 years, 5 V has been the standard supply voltage for digital circuits. It was born as the best compromise among the competing interests of processing capabilities, bipolar circuit requirements, power consumption, and required system noise immunity. When CMOS gradually supplanted LS-TTL in the 1980s, it adopted this popular supply voltage, as well as the standard 5-V logic level definitions ($V_{oh} > 2.4$ V, $V_{ol} < 0.4$ V, $V_{ih} > 2.0$ V, $V_{il} < 0.8$ V), despite the fact that these definitions were dictated by bipolar TTL circuit considerations and did not naturally apply to the more symmetrical CMOS structure (Fig. 1).

The relentless pressure to achieve higher speed, higher density, lower cost, and lower power consumption drives

CMOS IC manufacturers to employ ever-thinner gate oxides and smaller geometries, with minimum feature dimensions dropping from 2 μ m in the early 1980s, to 0.8 μ m in 1990. Since then, they've dropped to 0.6 μ m, 0.5 μ m, and currently 0.35 μ m, with a few companies already starting to employ 0.25- μ m features. By early 1998, several companies also expect to place processes with 0.18- μ m features into production.

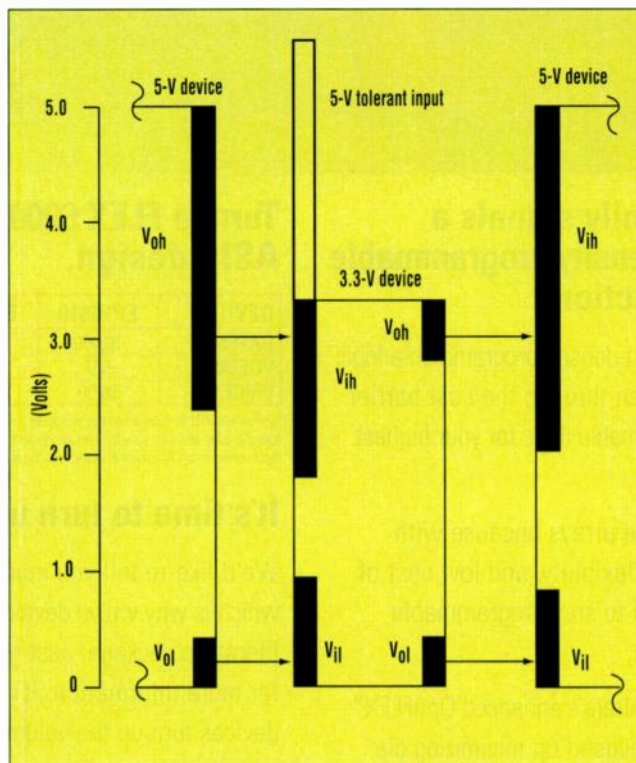
The entire industry, from designers and manufacturers to users, bene-

fits from this rapid process migration, but the transition is coming at a price. The power-supply voltage must decrease to compensate for the smaller features (Fig. 2). At 0.35 μ m, CMOS circuits do not reliably tolerate a 5-V supply voltage. Thus, the JEDEC standards committees had already put in place a 3.3-V power supply standard, which the logic industry adopted. Similarly, at 0.25 μ m, for optimum circuit reliability, the supply voltage must be lowered further to 2.5 V, and for 0.18- μ m technology circuits

will probably operate most reliably when powered by 1.8 V. Although there is no direct mathematical relationship, it is interesting to note the accidental, simple numeric relationship between minimum supply voltage and maximum supply voltage.

The lower supply voltage brings the benefit of lower-power operation, since power consumption is proportional to the square of the supply voltage. Compared to a chip operating at 5 V, a similar circuit running from 3.3 V consumes half the power, and a circuit running from 2.5 V consumes only a quarter of the power. This is a welcome reprieve from the unavoidable power increase and associated thermal problems brought about by higher circuit complexity and ever faster clock rates.

However, the user who wants to take advantage of the technical and economic benefits of smaller process geometries faces several



1. Matching up the voltage windows to ensure I/O compatibility between 3.3- and 5-V logic families ensures that mixed systems will operate without any logic incompatibilities. The lower operating voltage of the 3.3-V devices limits the maximum high value for the logic swing, but still provides a significant region of overlap for compatibility.

Another big idea from Motorola.




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new issues:

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- How to interface between CMOS devices with different supply voltages.
- How to cope with supply-voltage sequencing.

Supply Distribution

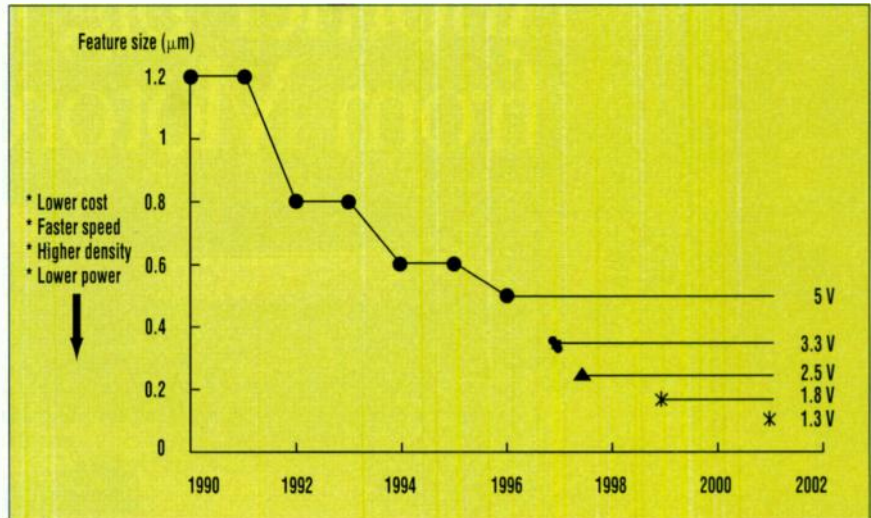
At today's circuit speeds, the pc board and its analog characteristics play a strong, if not dominating, role in determining digital system performance. Even modest-length (3-in.) interconnects must be treated as transmission lines, and ground and V_{CC} planes must be kept reasonably free from synchronous and asynchronous voltage transients.

To accomplish this task, the designer must pay attention to each signal path, including the complete current loop—from the positive supply connection through the IC and interconnects, back to ground distribution, through the decoupling capacitors, and back to the positive supply terminal. Modern designs require pc boards with at least four layers, and usually more. At least one inner layer must be dedicated as a ground plane and must be kept as undisturbed as possible.

Any major hole in the ground plane would force the ground current to take detours, which increases the inductance and causes ground voltage spikes. In simple designs, 5- and 3.3-V supplies can share a common power plane. However, the 3.3-V distribution requires greater attention, because it affects the signal-noise margin more than on the 5-V plane.

The 3.3-V supply can either be brought in from off-board, or generated by an on-board 5-V-to-3.3-V dc-to-dc converter. The latter method has been pioneered and proven by the PentiumPro, with very compact and inexpensive switchers for up to 12 A. The switchers are now available from many manufacturers (NSC, Linear, Maxim, Cherry, and traditional power-supply houses).

Also, low-impedance ceramic decoupling capacitors are needed to supply the dynamically changing I_{CC} inside the chip, and to provide a return path for external current changes. These instantaneous current peaks are much



2. As process technology migrates downward, the supply voltage must be reduced to prevent electrical stresses from internally destroying the circuits. Although there is no direct mathematical relationship, at a feature size of 0.25 μm , the optimum operating voltage is 2.5 V, and when features drop to 0.18 μm , the supply voltage should drop to 1.8-V.

higher than the average dc current, which will typically fall between 100 mA for small FPGAs and 2 A for the larger FPGA chips.

To demonstrate the importance of good V_{CC} decoupling, let's assume the example of a synchronous, single 40-MHz clock design consuming 1 A. Most of the current flow will be in the first 5 ns of the 25 ns clock period. This 5-A peak current must be supplied by the sum of the decoupling capacitors. In this example, $5 \text{ A} \times 5 \text{ ns}$ creates a 250-mV drop on a 0.1 μF decoupling capacitance. That figure is, at best, on the borderline of acceptability.

To improve the scenario, first examine the capacitors. Decoupling capacitors must have very low inductance and series resistance. The total capacitance value is less important, as long as it exceeds 0.1 μF .

The best way to achieve low impedance at gigahertz speeds is to use multiple capacitors in parallel. Use 0.01- to 0.1- μF ceramic capacitors, mounted very close to each V_{CC} pin and directly connected to the ground plane. Some board manufacturers also elect to use an extremely thin (down to 2 mils or 0.05 mm) dielectric layer between the ground and V_{CC} planes to achieve excellent distributed decoupling capacitance.

Second, keep the lines very short. A 0.25-in. (6-mm) long narrow trace represents an inductance of 20 nH. A current transient of 100 mA/ns causes a

voltage drop of 2 V across this inductance, which is unacceptable.

Ground bounce describes the dynamic voltage difference between the on-chip ground and the system ground plane. It's caused by current changes in the chip-to-package bonding wire and the lead frame inductance. In the best of cases, this inductance is as low as 3-to-5 nH. Fast output-current changes cause the chip internal ground to bounce up and down with respect to the system ground plane.

Look Out For Ground Bounce

The ground bounce becomes a serious problem when many outputs change simultaneously, at a fast slew rate, and in the same direction. Wide 32-bit address/data buses are a notorious example. The ground-bounce problem might be slightly relieved at 3.3 V, since the output swing is reduced from 5 V, while the input threshold, and noise immunity are unchanged from the typical 5-V logic with its TTL-like inputs.

Luckily, synchronous single-clock systems tolerate surprising amounts of ground bounce. The disturbing output transitions occur a few nanoseconds after the active clock edge, but data inputs are sampled a few nanoseconds before the next active clock edge—well after the ground bounce has settled, usually in about 5 ns. As long as the ground or V_{CC} changes do not directly upset internal flip-flops,

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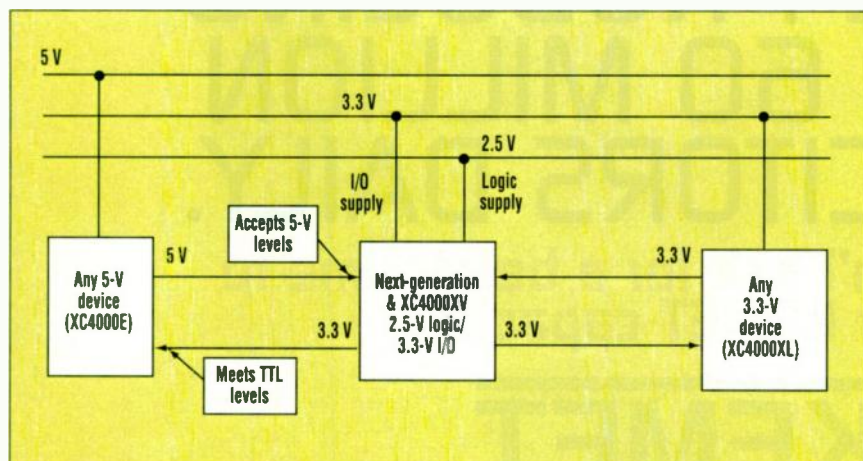
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3. A typical mixed-voltage logic system can employ 5-V, 3.3-V, and 2.5-V logic, and have the logic interoperate, as long as the designer pays careful attention to power distribution and interface requirements. In the center of the circuit above, a next-generation 2.5-V FPGA could offer 5-V compatibility on its I/O lines to tie into the 5-V device shown on the left, and offer 3.3 V compatibility for the device on the right.

and as long as all asynchronous inputs, have good noise margins, ground bounce looks scarier than it really is. But it must remain a concern for all system designers.

To minimize ground bounce, crosstalk, and other external noise, several FPGA suppliers include a slew-rate-limited output option. It is individually programmable for each pin, so the user can slow down the transition rate on all noncritical outputs.

Consider Supply Currents

Supply-current values become critical for large chips that are clocked at high rates. These large, high-speed chips are often heavily pipelined. System designers are tempted to run the chips up to their thermal limits, perhaps with a glued-on or clipped-on heatsink and even a built-in small fan. For example, the Intel PentiumPro and DEC Alpha CPUs dissipate 15 W to 30 W, drawing dc currents of 6 A to 12 A, with significantly higher transient currents supplied by the decoupling capacitors. At a given upper limit of practical power dissipation, lower V_{CC} levels result in higher operating currents, which in turn, require more care in V_{CC} distribution and decoupling methods.

Electromagnetic interference (EMI) is another concern, and a reason for designers to brush up on their high-frequency analog skills. The large current swings generate significant amounts of high-frequency noise

since the voltage and current transition times are about 1 ns. Designers must pay more attention to board layout, transmission-line design techniques, and shielding approaches to ensure reliable system performance.

Mixing The Levels

Since all supply voltages share a common ground, there are no problems interfacing logic-Low levels in either direction. All potential problems are in interfacing logic-High levels. When 3.3-V logic High drives a 5-V input, there is no problem when the 5-V device has a TTL-level input threshold

of about 1.3 V. This fact is true for most CMOS devices. The driving 3.3-V output High level is close to V_{CC} , well above the required V_{ih} of 2.0 V.

However, when a 5-V logic High drives a 3.3-V input, the High 5-V output voltage often will force excessive current into the 3.3-V input. The input pins on older Xilinx 3.3-V FPGAs, and on most other manufacturers' 3.3-V devices, have a clamp diode between each pin and V_{CC} to protect the circuit against electrostatic discharge (ESD). This diode starts conducting when the pin is driven more than 0.7-V positive with respect to its V_{CC} .

This internal diode presents a problem in mixed-voltage systems, because it clamps whenever a 5-V logic High is driving a 3.3-V input. In newer logic products, Xilinx has overcome the drive problem by eliminating the clamp diode between the pin and V_{CC} . The pins can be driven as high as 5.5 V—irrespective of the actual supply voltage used by the receiving input. (For an overview of what Xilinx did to overcome the problem, see “*The Diode Elimination Challenge*”, see below.)

These devices are, therefore, unconditionally 5-V tolerant, and the user can ignore all interface precautions. Excellent ESD protection (up to several thousand volts) is achieved in the Xilinx devices through the use of a patented diode-transistor structure that does not connect to V_{CC} .

The Diode Elimination Challenge

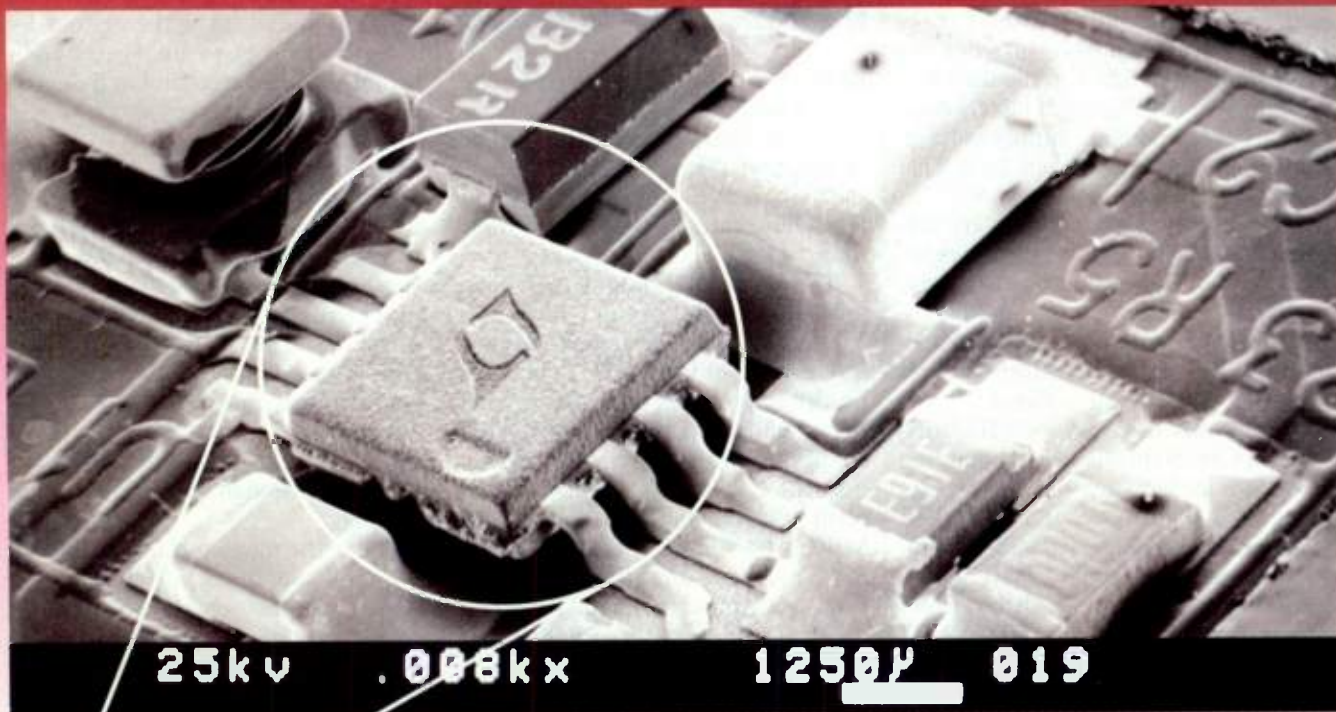
In developing the XC4000XL I/O buffers, designers at Xilinx faced the challenge of trying to make the I/O buffers compliant with the PCI specification while offering 5-V tolerance.

PCI compliance requires a clamping diode to V_{CC} , while 5-V tolerance, on the other hand, cannot have the diode on the input. To meet both requirements, designers found that they could not tie the n-well of the p-channel output transistor to the 3.3-V V_{CC} , since the parasitic diode would prevent the I/O pin from going substantially more positive than 3.3 V.

To satisfy these conflicting requirements, an internal diode was added to each output, with its cathode connected to an internal V_{tt} rail. For PCI compliance, this rail must be connected externally to the appropriate V_{CC} supply (5 V or 3.3 V). For 5-V tolerance, the V_{tt} rail is left floating.

Since the XC4000XL devices do not have a diode between the n-well of the p-channel output transistor and the chip V_{CC} pin, electrostatic-discharge protection against positive-going voltage spikes is provided by dedicated proprietary bipolar circuits that are turned on by junction breakdown when the inputs exceed 7 V.

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The LT1307: 600kHz 1 volt low noise switcher.

to 1V while using only 60 μ A quiescent current so you can squeeze your battery dry.

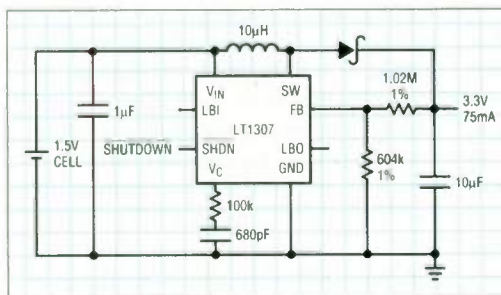
And the LT1307 delivers load currents of up to 75mA at

3.3V or up to 40mA at 5V, from a depleted 1V battery. The device also includes a handy low-battery detector with a 200mV reference. Need higher voltage? The LT1307 is great for generating 12V for flash memory or LCD bias up to 28V. So you can save space in a variety of DC/DC conversion applications.

The LT1307 is available in MSOP, SO-8 and 8-pin PDIP

packaging, with 100-piece prices starting at \$2.50 for MSOP. Want to learn more about this tiny power converter? Contact Linear Technology Corporation, 1630 McCarthy Blvd., Milpitas, CA 95035-7417. 408-432-1900. Fax: 408-434-0507

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From a design perspective, it is important to remember that directly connecting an active-High 5-V CMOS output to an active-High 3.3-V output creates contention and must be avoided.

When 3.3-V inputs are driven from a 5-V TTL-level output with an n-channel pull-up transistor, the input current is naturally limited to less than a few milliamps—even when the 5-V supply is at 5.25 V while the 3.3-V supply is at 3.0 V, a very unlikely combination. At nominal supply voltage levels, the current is about 1 μ A. This interface poses no problems.

If non-5-V-tolerant inputs are driven from a CMOS-level complementary, rail-to-rail output, the user must somehow limit the current. A 1-k Ω resistor can limit the current to less than 2 mA, but causes a slight speed penalty (1 k Ω \times 35 pF = 35 ns).

In the case of a 3.3-V logic High driving a CMOS threshold 5-V input, the best advice is to avoid it. An active-High 3.3-V output cannot be pulled higher, since the internal pull-up transistor represents about a 50- Ω impedance for any current in either direction. A pull-up resistor to 5 V is therefore meaningless. If the internal pull-up transistor is disabled (open drain output), the pin can be pulled higher, until the ESD clamp becomes conductive. The device pins in the XC4000XL series can be configured as open drain, and an external resistor can pull them all the way to 5 V, albeit with an RC speed penalty.

Sequencing The Supplies

Any system with more than one supply voltage faces the possibility that the voltages will be applied in an undefined or uncontrolled sequence. For most ICs, this means the designer must calculate the maximum current potentially flowing into the pins of the unpowered device. The current value depends on the powered-up device's output structure (complementary outputs drive the highest current) and on the voltage compliance (impedance) of the unpowered V_{CC} distribution net.

If the distribution net is held rigidly to ground, the undesired current will be high. If the unpowered V_{CC} net can easily be pulled High, the current will be far less. Most inputs

Supply-current values become critical for large chips that are clocked at high rates.

will tolerate 50 mA for a few seconds, and 10 mA for unlimited time. For significantly higher currents there might be the short-term risk of latch-up, and the long-term risk of metal migration if the high current persists for thousands of hours.

The XC4000XL family of devices are 5-V tolerant, even when their V_{CC} is zero. These devices, therefore, have no problem with arbitrary power sequencing or even with hot plug-in at the board level. When 5 V is applied first, there is no current into the FPGAs. When 3.3 V is applied first, the device outputs can be kept three-stated by connecting the 5-V V_{CC} line as an active-Low global three-state input to the 3.3-V devices, again eliminating any undesirable current.

One common goal by many system designers today is to migrate existing 5-V system designs to 3.3 V. Often, it can be a simple matter of replacing the appropriate 5-V FPGAs and other logic chips with their 3.3-V equivalents. Xilinx and other FPGA suppliers now offer 3.3-V FPGAs that are functionally and pin-out compatible with their 5-V cousins.

The only required accommodation is that the pc board must accept the V_{CC} change-over. Additionally, another voltage regulator or switching supply might be needed. Mixed 5-V/3.3-V systems will be common for several years to come, so it is important to give the user the maximum amount of freedom and cause the least amount of rework when migrating to the lower supply voltages of the future. And, in the near term, future mixed systems also will have to deal with 2.5-V devices, adding to the distribution headache—5-, 3.3-, and 2.5-V supplies will be needed to power all the devices (Fig. 3).

And that future isn't very far off. There is already a movement by logic

suppliers to create a standard logic family that operates from a 2.5-V supply. Although that changeover won't happen overnight, there will be a significant momentum since it will likely be less traumatic than the change from 5 to 3.3 V. Most FPGA suppliers will probably use 2.5 V for the internal logic core, while running the I/O from 3.3 V. Again, it will be the system designer's challenge to provide the additional V_{CC} , distributing and decoupling it appropriately.

More Pins Probable

However, if the systems are already tuned for logic operation at 3.3 V, then the use of 2.5-V logic should not be a concern when it comes to signal-level incompatibilities. Most suppliers will increase the number of V_{CC} and perhaps ground pins. The designer might want to plan ahead and leave these designated pins unused in the 3.3 V design. All in all, the transition to 2.5 V will be easier than the earlier change to 3.3 V.

After the move to 2.5 V will come the transition to 1.8 V. However, it is too early to know exactly what will be required to make that transition. Of course, 1.8-V logic will not directly interface with 5-V logic, and the interface standards for 1.8-V systems have not yet been determined. The industry is planning to accommodate direct interfacing between three successive generations: 5 V to 3.3 V to 2.5 V, or 3.3 V to 2.5 V to 1.8 V.

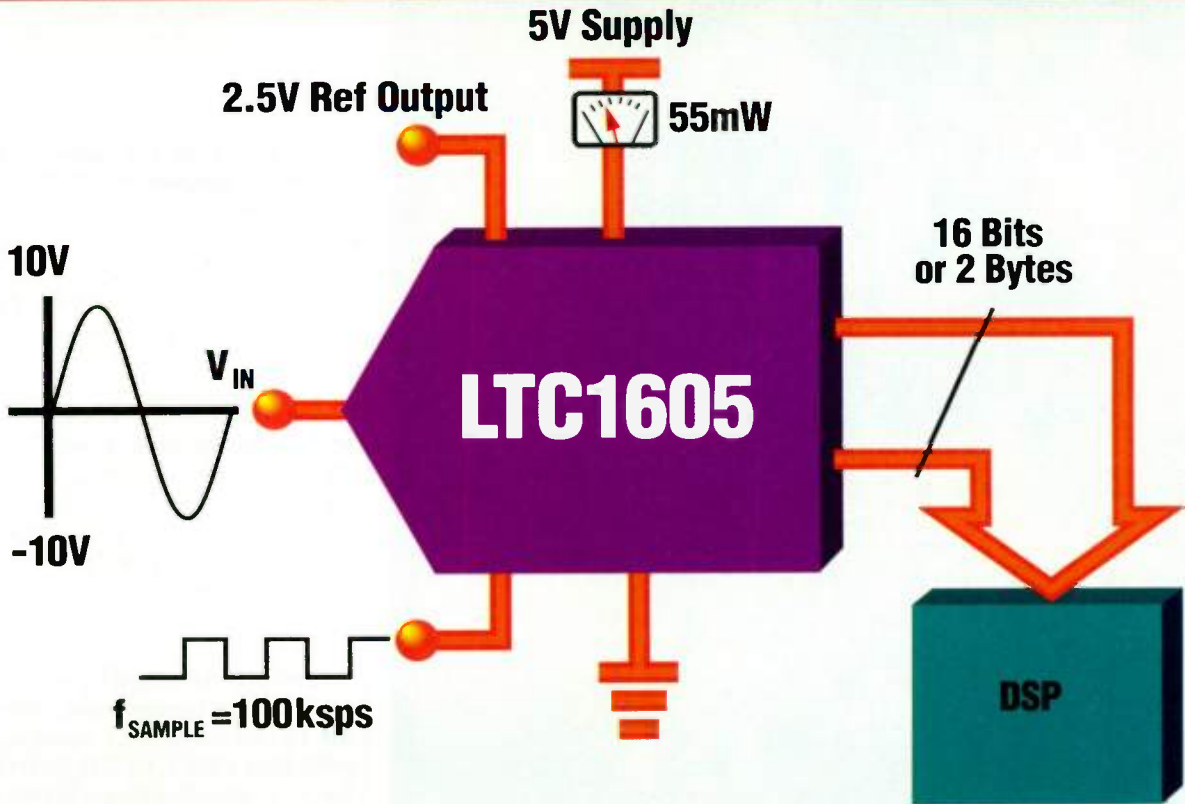
Peter Alfke has held the position of director of applications, engineering since joining Xilinx in 1988. He holds the equivalent of an MSEE from the Technical University in Hannover, Germany. Prior to joining Xilinx he held application engineering positions at Fairchild, Zilog, and Advanced Micro Devices.

Recommended reading:

High-Speed Digital Design, a Handbook of Black Magic, H. Johnson and M. Graham, 1993 Prentice Hall.

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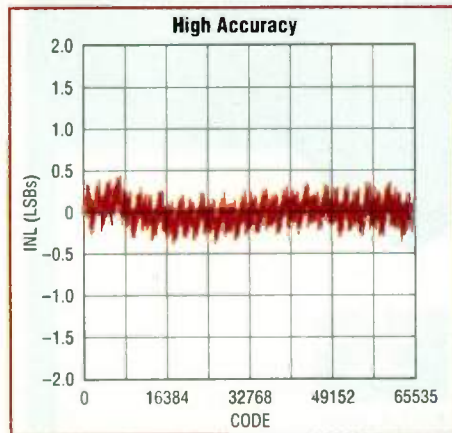


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MEETINGS

OCTOBER

NEPCON Texas '97, October 7-9. Informat, Dallas, Texas. Contact Reed Exhibition Companies, Customer Service, (800) 467-5656; fax (203) 840-9656; e-mail: inquiry@nepcontexas.reed-expo.com; Internet: <http://nepcon.reedexpo.com>.

Seventh International Conference on Artificial Neural Networks, (ICANN '97), October 8-10. Lausanne, Switzerland. Contact ICANN '97, Ecole Polytechnique Federale De Lausanne, LAMI, CH-1015 Lausanne, Switzerland; fax +41 21 693 5656; e-mail: icann97@epfl.ch; <http://www.epfl.ch/icann97>.

Sixth IEEE International Conference on Universal Personal Communications, October 12-16. Hotel del Coronado, San Diego, California. Contact Gail Weisman, IEEE Communications Society, 345 East 47th Street, New York, New York 10017; (212) 705-7018; fax (212) 705-7865; e-mail: g.weisman@ieee.org.

Sixth IEEE International Conference on Universal Personal Communications (ICUPC '97), Oct. 13-15. Contact Tony Acampora, MC 0409, Bldg EBU1, UCSD, 9500 Gilman Dr., La Jolla, California 92093-0409; (619) 534-5438; fax (619) 534-2486; e-mail: acampora@ece.ucsd.edu.

Conference on Domain-Specific Languages (DSL), October 15-17. Red Lion Resort, Santa Barbara, California. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, California 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: <http://www.usenix.org>.

ICSPAT/DSP World 1997, October 15-17. San Diego Convention Center, San Diego, California. Contact Denise Chan, Miller Freeman Inc., (415) 278-5231; e-mail: dsp@exporeg.com.

IEEE Holm Conference on Electrical Contacts, October 18-22. Wyndham Franklyn Plaza, Philadelphia, Pennsylvania. Contact Wendy Rochelle, IEEE Conference Services, 445 Hoes Lane, Post Office Box 1331, Piscataway, New Jersey 08855-1331; (908) 562-3870; fax (908) 981-1769; e-mail: w.rochelle@ieee.org.

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VHDL International User's Forum (VIUF) Conference, October 19-22. Hyatt Regency Crystal City Hotel, Arlington, Virginia. Contact VIUF, (415) 329-0510.

IEEE Telecommunications Energy Conference (INTELEC '97), Oct. 19-23. World Congress Centre, Melbourne, Australia. Contact Robert N.K. Thuan,

Network Products-Telstra Corp. Level 14, 242 Exhibition St., Melbourne, Victoria 3000, Australia; +61 3 634 6216; fax +61 3 632 3607

Sensors Expo, October 21-23. Cobo Convention Center; Detroit, Michigan. Contact Expocon Management Associates Inc., (203) 256-4700; e-mail: sensors@expocon.com; Internet: <http://www.expocon.com>.

Fourth IEEE International Conference on Image Processing (ICIP '97), October 26-30. Fess Parker's Red Lion Resort, Santa Barbara, California. Contact Sanjit K. Mitra, Electrical and Computer Engineering, University of California, Santa Barbara, California 93106-9560; (805) 893-3957; fax (805) 893-893-3262; e-mail: mitra@ece.ucsb.edu.

11th Systems Administration Conference (LISA '97), October 26-31. Town & Country Hotel, San Diego, California. Contact USENIX Conference Office, 22672 Lambert Street, Suite 613, Lake Forest, California 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: <http://www.usenix.org>.

SYSTEMS 97, Oct. 27-31. Munich Trade Fair Center, Munich Germany. Contact Messe Munchen GmbH, Messagelände, D-80325 Munchen, +49 (89) 51070; fax +49 (89) 51 07506; Internet: <http://www.sysems.de>; e-mail: info@messe-muenchen.de.

19th Annual International Conference of the IEEE Engineering in Medicine & Biology Society, Oct. 29-Nov. 2. Sally Chapman, Secretariat, National Res. Council of Canada, Bldg. M-55 Rm. 393, Ottawa, KIA OR8, Canada; (613) 993-4005; fax (613) 954-2216.

19th International Conference of the IEEE Engineering in Medicine & Biology Society, October 30-November 2. Chicago Marriott Downtown, Chicago, Illinois. Contact Meeting Management, 2603 Main Street, Suite 690, Irvine, California 92714; (714) 752-8205; fax (714) 752-7444; e-mail: embs97@ieee.org; Internet: <http://www.eecs.uic.edu/~embs97>.

NOVEMBER

IEEE International Test Conference (ITC), Nov. 1-5. Sheraton Washington Hotel, Washington, DC. Contact ITC, 655 15th St., N.W., Suite 300, Washington, DC. 20005; (202) 639-4164; fax (202) 347-6109.

Voice, Video, & Data Communications Conference & Exhibition, November 2-6. Dallas, Texas. Contact SPIE Exhibits Department, Post Office Box 10, Bellingham, Washington 98227-0010; (360) 676-3290; fax (360)-647-1445; e-mail: exhibits@spie.org.

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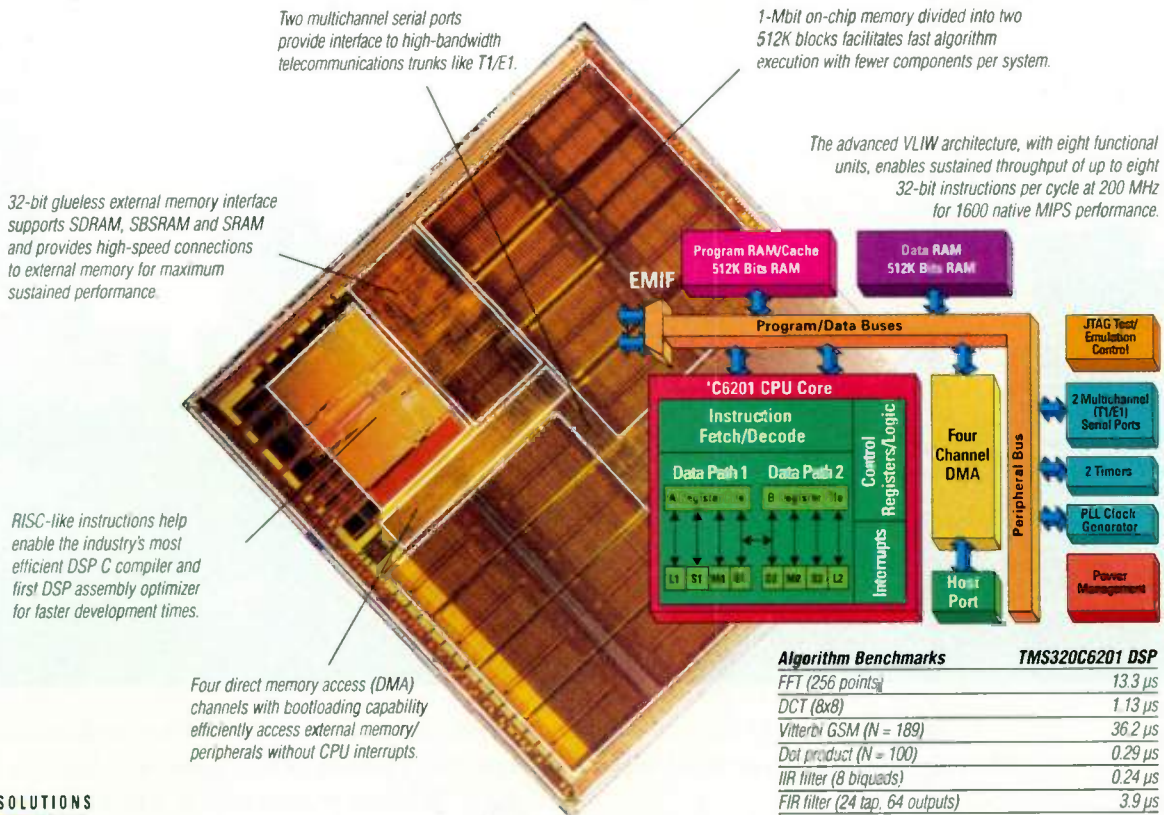
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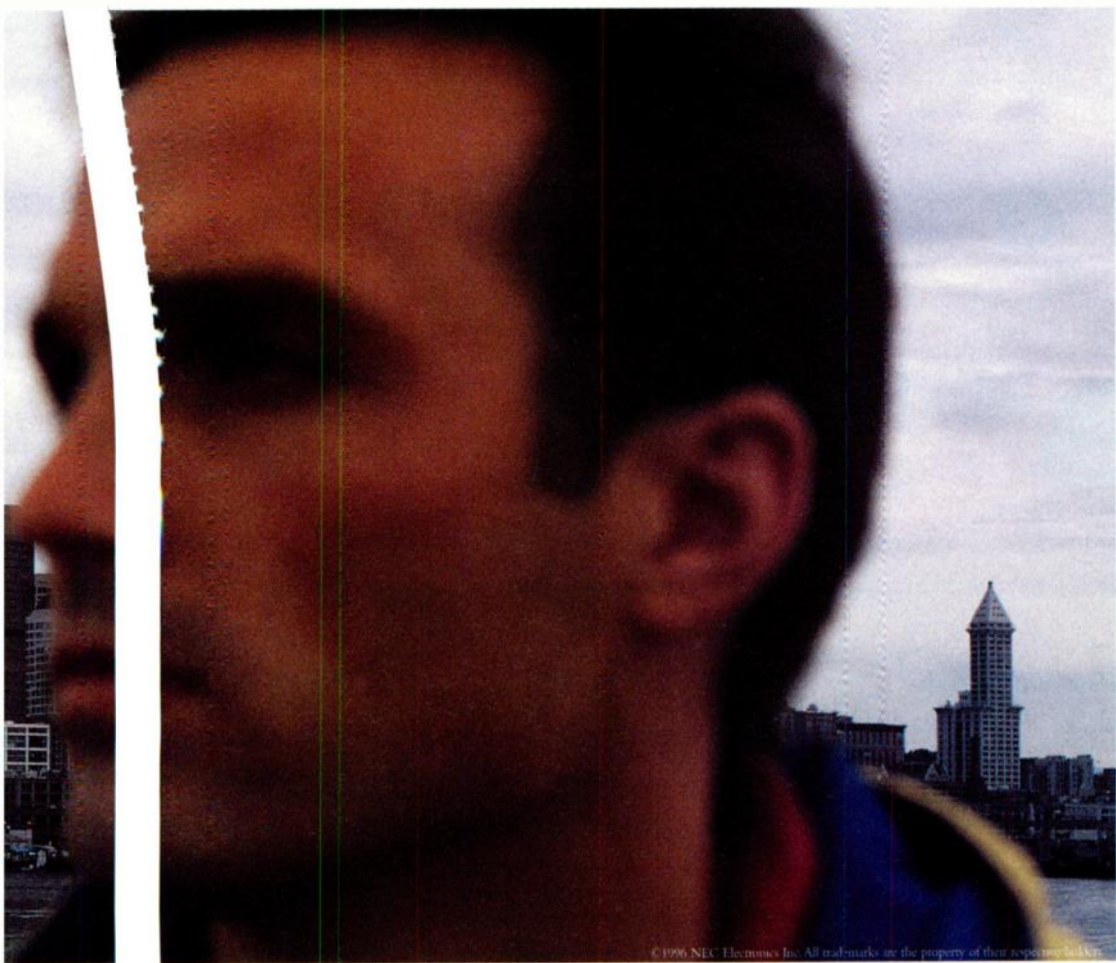
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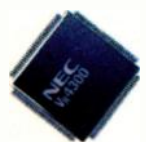
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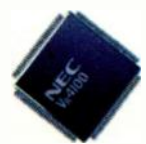
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ELECTRONIC DESIGN QUICK LOOK

■ Edited by Mike Sciannamea and Debra Schiff

MARKET FACTS

If You Can't Take The Heat...

High-temperature plastics are those polymers that continue to perform in temperatures in excess of 200°C. Consultants at Kline & Company, Fairfield, N.J., have been studying the high-temperature market, and have seen the worldwide growth of these polymers expand from an \$800 million market in 1984 to \$2.9 billion in 1996. According to the company, the market comprises a group of 10 polymers: Fluoropolymers, liquid-crystal polymers, polyamideimides, polybenzimidazole, polyetherimides, polyimides, engineered thermosets, polyketones, polyphenylene sulfide, polysulfone derivatives, high-temperature polyamides, and polycyclohexane dimethylterephthalate. Over the past several years, according to Kline & Company, some of these polymers have enjoyed 20% consumption increases per year. The impetus behind the growth has been attributed to several points. The electronics industry is steadily moving in the miniaturization direction, in addition to surface-mount assemblies. In the automotive industries, there are increases in the use of chemical and temperature resistant polymers for "under-the-hood" applications. There also have been

moves made to replace metals in hostile and corrosive environments with high-performance polymers. And, as consumer, dental, medical, and industrial products continue to evolve, uses for high-temperature, lightweight polymers increase. Out of the nearly \$3 billion market, 40% is found in the electrical and electronics sectors. The most widely used plastics in that category are fluoropolymers, liquid-crystal polymers, polyimides, polyphenylene sulfide, and high-temperature polyamides. Typical applications include circuit boards, connectors, wire and cable, relays, and switches.

In the automotive sector, camshafts, fuel lines, fuel rails, gaskets, impeller shafts, intake manifolds, and valve covers are all experiencing the trend toward high-temperature plastics. Seeing the greatest difference between temperature requirements, the aerospace market intends to use polymers in military aircraft, jet engines, missiles, and space applications. Typical aerospace applications include composite matrix resins, structural components, housings, coatings, adhesives, and engine



components.

For more information, contact Kline & Company, 165 Passaic Ave., Fairfield, NJ 07004; (973) 808-3389; fax (973) 227-6291.—DS

EYE ON ISO 9000

Mini-Circuits, manufacturers of RF, IF, and microwave components for the wireless communications industry, has achieved ISO 9001 certification. The certification covers all activities at the company's Brooklyn, N.Y. headquarters, and Deer Park, N.Y., and Branson, Mo. locations. Contact Mini-Circuits, P.O. Box 350166, Brooklyn, NY 11235; (718) 934-4500; fax (718) 332-4661; e-mail: sales@minicircuits.com. **CIRCLE 490**

Andrew Corporation's Earth Station Antenna business unit has received ISO 9001 registration. The antennas come in a number of sizes for applications such as corporate networks, broadcast network distribution, and international communications. Contact Andrew Corporation, 10500 W. 153rd St., Orland Park, IL 60462; (708) 349-3300; (708) 349-5222; Internet: <http://www.andrew.com>. **CIRCLE 491**

SMTEK Inc. has recently received ISO 9001 certification. The engineering services company provides a full range of circuit card design, material management, production, and test services to the high-reliability commercial, medical, military, and aerospace markets. Contact SMTEK Inc., 2151 Anchor Court, Newbury Park, CA 91320; (805) 376-2595; fax (805) 376-2686. **CIRCLE 492**

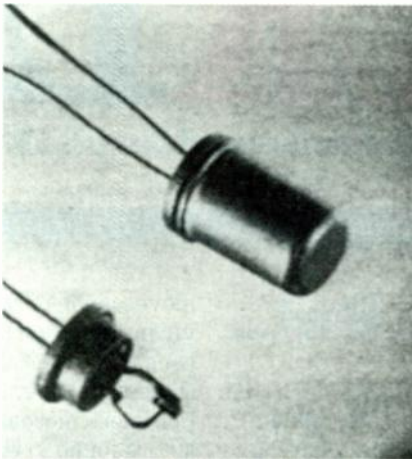
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Four-Layer Diode: Bistable

The low-power, four-layer switching diode is a two-terminal silicon device which can exist in either of two states: an open or high-impedance state (1 to 100 megaohms) and a closed or low-impedance state (1 to 10 ohms). It is switched from one state to the other through control of the voltage and current values.

It is driven to its closed state by application of a voltage greater than the critical breakdown point, and it will continue to be conductive as long as a current greater than a critical holding current is maintained. When the current is reduced below the holding value, the device regains its open state. While the parameters are controllable over some breadth in manufacturing, typical ranges of values are as follows: firing voltages range from 20 to 60 v; holding currents are 25 ma or somewhat less at about 1 v; the switched-current capacity is in the order of 100 ma; and maximum power dissipation is on the order of 1 mc, though theory indicates that rates to 10 mc can be reached. Beckman Instruments Inc., Dept. ED, Shockley Semiconductor Lab., Mountain View, Calif. (*Electronic Design*, August 1, 1957, p. 89)

By 1957, William Shockley had set up his own company in what was to become Silicon Valley. The company was well-stocked with luminaries such as Gordon Moore and Bob Noyce, but they were soon to leave Shockley and move out on their own, forming Fairchild Semiconductor.



Non-Linear Computing Component—Function Of Two Variables

Called the Function of Two Variables, Model F2V provides an output voltage which is an arbitrary function of two independent varying input voltages. A family of curves is produced with smooth interpolation in two directions. This surface may be visualized as a tent with 36 poles, where the height of each pole is individually adjustable between ± 50 v.

This computing component fills a need for an instrument capable of providing instantaneous solutions for problems in data reduction and computing involving functions of two variables. Extensions of the principles involved make possible functions of three or more variables. Specifications include: Input range, $x = 0$ to $+50$ v, $y = 0$ to $+50$ v. Output range, -50 to $+50$ v. Impedance, less than one ohm. Allowable load impedance, 30 K minimum. Power requirements, 300 v dc at 150 ma, 115 v ac 50-60 cps or 150 w. Rack mounted. Dimensions $19 \times 8\frac{1}{8} \times 16$ in. George A. Philbrick Researches, Dept. ED, 230 Congress St., Boston 10, Mass. (*Electronic Design*, August 15, 1957, p. 95)

Bob Pease often mentions his experiences at Philbrick, which he joined in the early 1960s. This instrument, although it appears to be a major step forward in precision analog technology, didn't have a name that exactly rolls off the tongue—"Function of Two Variables." It's too bad Bob couldn't have had a shot at naming it. Bob does recall the instrument—in fact, he still has a copy of the original data sheet.

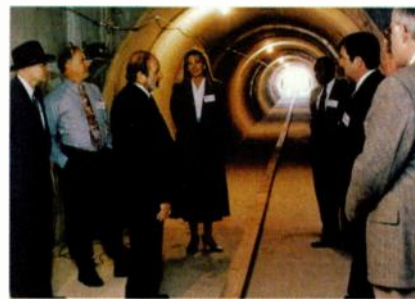
He has this to say about the F2V: "This monstrous analog mini-computer had 36 one-turn controls (pots) on its front panel. You could use those pots to manipulate the gains of 50 interpolated segments, and generate a 'control surface'. Inside, it used 14 op amps, 85 vacuum diodes, 100 precision resistors, (and 150 mA at ± 300 V) to generate an output voltage that was a piecewise linear arbitrary function of two input voltages. These days, Fuzzy Logic is typically used to do this—probably a lot less drifty!"—SS

Test Tunnel In Texas

Cutting the crimson ribbon to open the new test tunnel facility, Dr. Thomas E. Charlton, the group president of communications systems for Andrew Corporation said that now Radiax cable will be fully evaluated in the systems environment. The new Radiax cable test tunnel facility (shown below) is in Denton, Texas. Andrew Corporation supplies communications systems equipment to the cellular, personal communications systems, and land mobile radio (broadcast and common carrier) markets worldwide.

The Radiax brand of cable is a solution specifically designed for wireless communications problems in confined areas such as buildings and tunnels. The radiating cable functions as a continuous distributed antenna. The cable features a multiband capacity, allowing multiple frequency bands to use the cable at the same time. Therefore, Radiax can be used as a backbone antenna for buildings and tunnels.

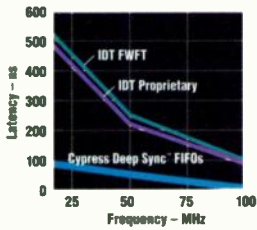
In the outer conductor, Andrew Corporation has inserted carefully controlled slots. These slots allow a portion of the internal coaxial power to be radi-



ated in a uniform manner, along the entire length of the cable. Interestingly, if an RF signal is transmitted in the vicinity of the Radiax cable, it will, conversely, be coupled into the coaxial mode. Then, it will be carried along the cable to an appropriate receiver.

Built to capture accurate information on DCS performance for a number of actual system environments, the Radiax cable test tunnel facility is a 400-ft. long tunnel that uses both circular and rectangular cross sections. Prototype cables and RF distributed system applications can be tested there.

Contact Andrew Corporation, 10500 W. 153rd St., Orlando Park, IL 60462; (708) 349-3300; fax (708) 349-5222; Internet: <http://www.andrew.com>.—DS



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x9 Package		
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KMET'S KORNER

...Perspective on Time-to-Market

BY RON KMETOVICZ

President, Time to Market Associates Inc.

P. O. Box 1070, 100 Prickly Pear Rd., Verdi, NV 89439; (702) 345-1455; fax (702) 345-0804

The column's companion chart illustrates a common occurrence in business—early success followed by a rather precipitous fall from the pinnacle of good fortune. In the illustration, the example company turns its first profit in 1992. Growth from 1992 to 1993 and from 1993 to 1994 runs within, or near, the triple digits; profit increases slow from 1994 to 1995; in the 1995 to 1996 period, the rise comes to an end as the enterprise shows significant profit decline; and, in the 1996 to 1997 period, profit erosion continues. It's a definite "good news" and "bad news" situation. In the early period, the financial health of the company, as measured by profits, exhibited robust trends. Then, something changed to produce a complete performance reversal.

Many factors may contribute to the decline in the financial health of a business, but one element, the loss of quality leadership, occurs most often. In the example cited, three individuals formulated the success profile of the 1992 to 1994 period. Two basically ran the company's product development programs while the third built and managed the company's marketing and distribution channels. The

trio worked as a team, constructively disagreed on many topics, but came together, as required, to address competitive, market, and other business-related issues. These individuals were respected internally and externally to the company. In 1994, after a major disagreement with a newly appointed chief executive officer, the trio moved to pursue other interests. When the leaders departed, those who remained knew they would be missed; they just did not know the degree.

The chart points out another key phenomenon—that of leadership merits. The exit transpired in 1994, the first major profit decline did not become highly visible until 1996, a two-year lag. Many inside the firm saw no connection between the missing contributors and the deteriorating business. After all, the new management team raised profits in 1995. If they could do it once, factors other than management must be the cause. In reality, the programs, initiatives, and systems put into place by the departing staff contained significant in-



RON KMETOVICZ
CONTRIBUTING EDITOR

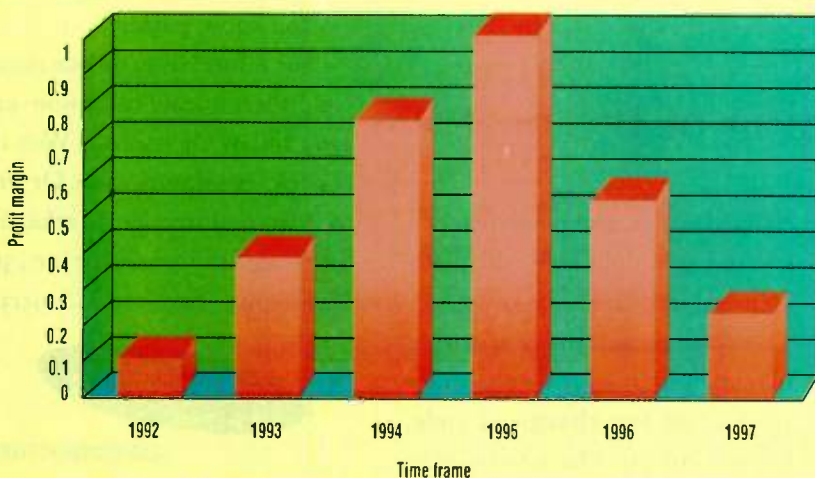
ertia, many taking more than a year to fully expire. Essentially, no replacements would have been necessary to sustain these activities; people merely found themselves immersed in their roles and gladly took credit for the good things that happened in 1995. For a period of time, the new chief executive and the reorganized management

team looked good. But the bubble burst in 1996. The new team had to initiate action on their own, and, as the data shows, what they did was not good enough.

Sadly, for the company's employees, the period of pain emerges in 1996 and 1997. 1996 marks the time when the existing management team moved to implement a few of its own impoverished programs. In 1997, they found them not to work. Concurrently, the board makes changes in the management and leadership of the company, as all within the organization struggle to initiate a turnaround. More time elapses before knowing the effectiveness of the changes—some work, many do not. The attempts continue until profitability is restored or the firm goes broke. That is the hard and dumb way to run a business!

The easy and smart way requires the preservation of critical leadership skills within the enterprise. And it's not that hard to keep leaders! First, the management team must know who the leaders are and what they do for the company. Armed with the knowledge and the ability to communicate, the company and the leaders within it can agree on the conditions of employment. A lot of recognition and a bit of reward generally sets the stage for long and happy relationships as profit dollars pour in.

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TRUDEL TO FORM



JOHN D. TRUDEL
CONTRIBUTING EDITOR

Throughout our nation's history, the U.S. has done well at innovation. That era may be ending. I'm not optimistic about the outcome of the patent wars. It's been a long time since we had visionary leaders like Franklin, Washington, and Lincoln.

The sad thing about the patent debates in Congress is not corruption, but ignorance. Oh, corruption is there. Great gobs of foreign money flow through the Commerce Department, and that's wrong. Still, what might do us in, I think, are our own outmoded tools for deciding "truth"—the single loop learning of the MBAs, lawyers, and

flacks. As the adage says, "the fault is not in our stars, but in ourselves."

Patent Commissioner Bruce Lehman is telling Congress to vote for H.R. 400 and S. 507 because patents are now granted in 19 months. His false data is magnified and refined by the legions of lobbyists who infest Washington, and then spoon-fed to Congress and the press.

Why worry? If patents really do process that quickly, and it may get better, then who cares if we publish patent filings at 18 months, "just as they do in the rest of the world?" (Actually, they don't, but that's another story.) The buzzword is "harmonization." All together now: "Hummmmmmm."

Lehman's lies are clever, often containing elements of truth, per Western legal protocols. After all, it's becoming an art form—miscommunication by bullet charts and selective facts. **Q:** "How fast do patents issue?" **A:** "Only 19 months, boss. No problem."

Still, any form of early patent disclosure can be lethal. If you rip a baby from the womb before the proper time, you risk its life. If you disclose your secret inventions to competitors before you have patent protection, they can pirate your work. If H.R. 400 and S. 507 pass, their lawyers can file re-examination proceedings, delay you, and steal your work.

Also, averages can deceive. You can drown in a lake with an average depth of 1 ft. Actually, 19 months is not the time from initial filing to the granting of the patent. It is the time from the last office action to grant or withdraw, and only for the simple patents without interferences or splits.

Many patents interfere with other patents and have to be re-filed, or are split by the patent office into multiple filings. In one infamous case, that took 43 years, the patent office made the inventor split his original patent into 30 separate applications. He spent his whole life re-filing and waiting.

Lehman blames the inventors, actually the victims, for causing long patent office delays. (These extreme cases are rare, less than 0.0013%. Most are caused by government secrecy orders.) Lehman calls these "submarine patents" and uses them, not his agreement with Japan, as the reason to destroy the best patent system in the world. Believe it or not, his story is working. It gives Congress and the Clinton Administration the excuse they need to take the money and do what the lobbyists want.

The General Accounting Office says that the typical patent takes about four years. The killer patents, those that start new industries, take much longer. A Hall of Fame group of inventors, including several Nobel Prize winners, wrote to President Clinton saying their key patents took a decade. He has yet to respond.

Truth is now hard to come by in our society. That's our fault, not Japan's.

John D. Trudel, CMC, provides business innovation consulting to selected clients. Lectures, keynotes, and workshops also are available. He is the author of "High Tech with Low Risk." The Trudel Group, 33470 Chinook Pl., Scappoose, OR 97056; (503) 640-5599; fax (503) 543-6361; e-mail: jtrudel@gstis.net; Internet: <http://www.trudelgroup.com>.

OFF THE SHELF

Quality Software Management Vol. 4: Anticipating Change illustrates how to create a supportive environment for software engineering—an environment where an organization can realize long-lasting gains in quality and productivity by learning to manage change. The book analyzes process change from a broad range of perspectives. Topics include: "Modeling How Change Really Happens," "Planning for the Future Organization," "Why Software Projects Fail," and "Three Levels of Process Improvement." The 504-page book is priced at \$50. Contact Dorset House Publishing Co., 353 W. 12th St., New York, NY 10014; (800) DH-BOOKS; fax (212) 727-1044; Internet: <http://www.dorsethouse.com>.

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Designing Object-Oriented Software enables users to create significantly more robust software applications using basic object-oriented (OO) design principles and a specific design process, responsibility-driven design. The book is applicable to any software effort, even those not using OO languages and environments. It features user-oriented design tools such as the collaborations and hierarchy graphs; coverage of classes, responsibilities, systems, and protocols; real-world considerations for choosing a programming language; evaluating and implementing a design; and testing an implementation. The 314-page book is priced at \$48. Contact The Penton Institute, 1100 Superior Ave., Cleveland, OH 44114; (800) 223-9150; fax (216) 696-6023; Internet: <http://www.penton.com>.

BOOK REVIEW

There are books and then there are BIG books. *The Electronics Handbook* happens to be one massive production from CRC Press, published in cooperation with the IEEE Press. The book is organized into 24 sections, with a total of 156 chapters written by over 180 authors. Each chapter is followed by three vitally useful elements. The first is a definition of terms used in the chapter, the second calls on the references used, and the third offers sources of further information.

These are, perhaps, the most important tests of a book of this nature. There cannot be, in the space that is available in *The Electronics Handbook*, absolute, all-defining coverage of the pertinent material. The best books in this class will lead you to the other areas that might be helpful or which can more closely examine a specific area of interest. *The Electronics Handbook* does both quite

well. In the areas where this reviewer has expertise, there are many references and leads that are logical; some are missing, some are there that would be arguable.

The organization of *The Electronics Handbook* in its sections and corresponding chapters is well done. With the section breakdown and the Contents and Indices, it's not hard at all for readers to find the material for which they're searching.

Most of the authors involved in the book are both known names and well-grounded in their inclusion. The editing has produced a standard of writing that is easy to follow and read. Some of the text layouts are tiring, but that is, quite probably, a result of the publishers' need to keep the dimensions of the book in a manageable range.

There are some areas in *The Electronics Handbook* where the emphasis comes a little too much from

an academic viewpoint. Additionally, there are some serious holes in processing technologies and IC designs. In some cases where there are holes, the references will direct readers to the right places.

Overall, I am glad to have this one on my bookshelf. By the way, *The Electronics Handbook* book is 2575 pages long. However, the book is a useful guide to areas of electronics where the reader might have little or no expertise. *The Electronics Handbook* also serves as a good reminder of technologies in the reader's own specialty. Having it all in one place makes it even more useful, and for what the book offers, the price is extremely attractive.

The Electronics Handbook (ISBN: 0-8493-8345-5) is priced at \$115, and is available from CRC Press Inc., 2000 Corporate Blvd., NW, Boca Raton, FL 33431.

Paul McGoldrick

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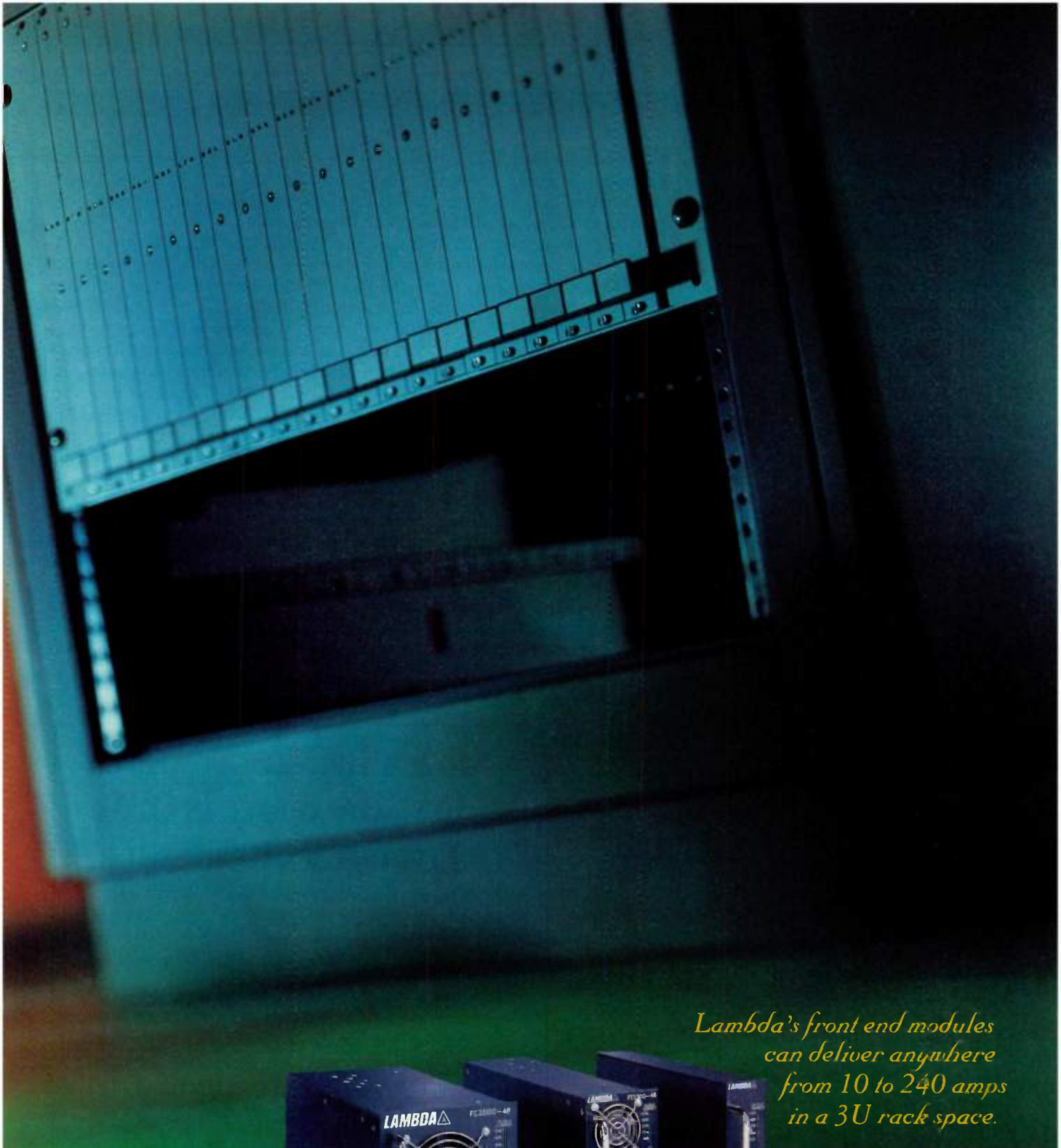


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INTERNET NEWS

How do YOU define taxation without representation? The Internet is opening the possibilities with all kinds of e-commerce options popping up all over the World Wide Web (not to mention the other webs out there). If you're looking to a guide through the madness, try *Taxation of Cyberspace*, by Information Technology Association of America (ITAA) and Deloitte & Touche LLP.

According to ITAA, the book examines current and possible taxation of cyber transactions. The authors are looking to stimulate discussion leading to the formation of tax policy regarding the Internet. Both tax professionals as well as information technology professionals will benefit from this collection of information.

Electronic business that begins within the borders of America's 50 states is subject to all kinds of different tax laws, depending on the state you do business in. Consequently, en-

terprises are trying to find sources of reliable information about how they can function in cyberspace. To get a true understanding of the real impact of taxes on the Internet, it's important to understand that we're not just talking about taxes levied on items bought and sold on the Internet. We're also talking about transactions that could involve taxation, including the service of providing access to the Internet, as well as the actual sale of goods and services.

In the beginning of this year, New York's Taxation and Finance Department said that Internet users are not responsible for sales or telecommunication taxes during access. But, Texans are, and the Texas government also is tacking on sales tax to information provided to subscribers by Internet content providers/purveyors. Additionally, the Lone Star state is taxing fees charged by Internet companies for the service of building

and maintaining sites. As of this writing, Colorado, Georgia, Illinois, and Ohio have so far remained out of the fray.

Also addressed in *Taxation of Cyberspace* are the vagueries associated with income and sales tax collection obligations. The book takes a state-by-state approach to state income taxes, state sales and use taxes, state telecommunications taxes, and state and local taxes on gross receipts. It's tough enough dealing with the tax system as it stands, without having to deal with its application to the Internet.

Federal and international tax issues also are extensively covered in the new book. The book is priced at \$150 for ITAA members and \$200 for nonmembers.

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L I S T S

FLIPPING THROUGH THE INTERNET ROLODEX

http://www.calstart.org: Clicking on this URL will bring you to Calstart's new, enhanced World Wide Web site. The site features thousands of pages of electric vehicle, natural-gas vehicle, and advanced-transportation information. Key web offerings include the Electrical Vehicle Recharge and Natural Gas Vehicle Refuel Site Directory, Industry Yellow Pages, Clean Car Catalog, Fleet Resource Center, and News Center. The recharge and refuel site directory provides the user with easy-to-use maps for those hard-to-find recharging/refueling stations. The yellow pages list hundreds of industry companies. Data for clean-vehicle fleet operators can be found at the resource center, and news is updated daily at the News Center.

http://www.waldmann-lighting.com: Web surfers on the lookout for task-lighting information can look to Waldmann Lighting's new site for the latest facts. The company's lines of office, machine-tool, and electronic inspection lights are all shown here. Lighting articles providing practical specification information also can be found here. Special sections focus on magnification lighting, lamps and ballasts, and ergonomic issues. Task lighting is examined here, along with tips for machine shop lighting. The site honors catalog ordering on all products.

http://www.whitemicro.com: Point your browser to White Microelectronics' new site for the most up-to-date information on the company's military and commercial memory products. Complete item listings and specifications, including entire data sheets are here. Visitors to the site will find all this information on SRAM, Flash, EEPROM, DRAM, mixed modules, and processors. The site also has broken these memory sectors down into ceramic monolithics and multichip modules, Plastic Plus (upscreened COTS devices), and commercial MCMs. Typical applications for the company's offerings include aerospace systems and high-end military systems. Other links at the site include new product high-

lights, company information, and sales and distributor information.

http://www.equipetech.com: A new site that focuses on high-precision robotic systems for the flat-panel display and semiconductor industries has recently made its way onto the World Wide Web. Equipete

Technologies also is featuring its new line of vacuum cluster tools at the site. The company's line of atmospheric transfer robots are listed here, with links to each on the Product Information page. Detailed corporate information, as well as company press releases, also can be found at the site.



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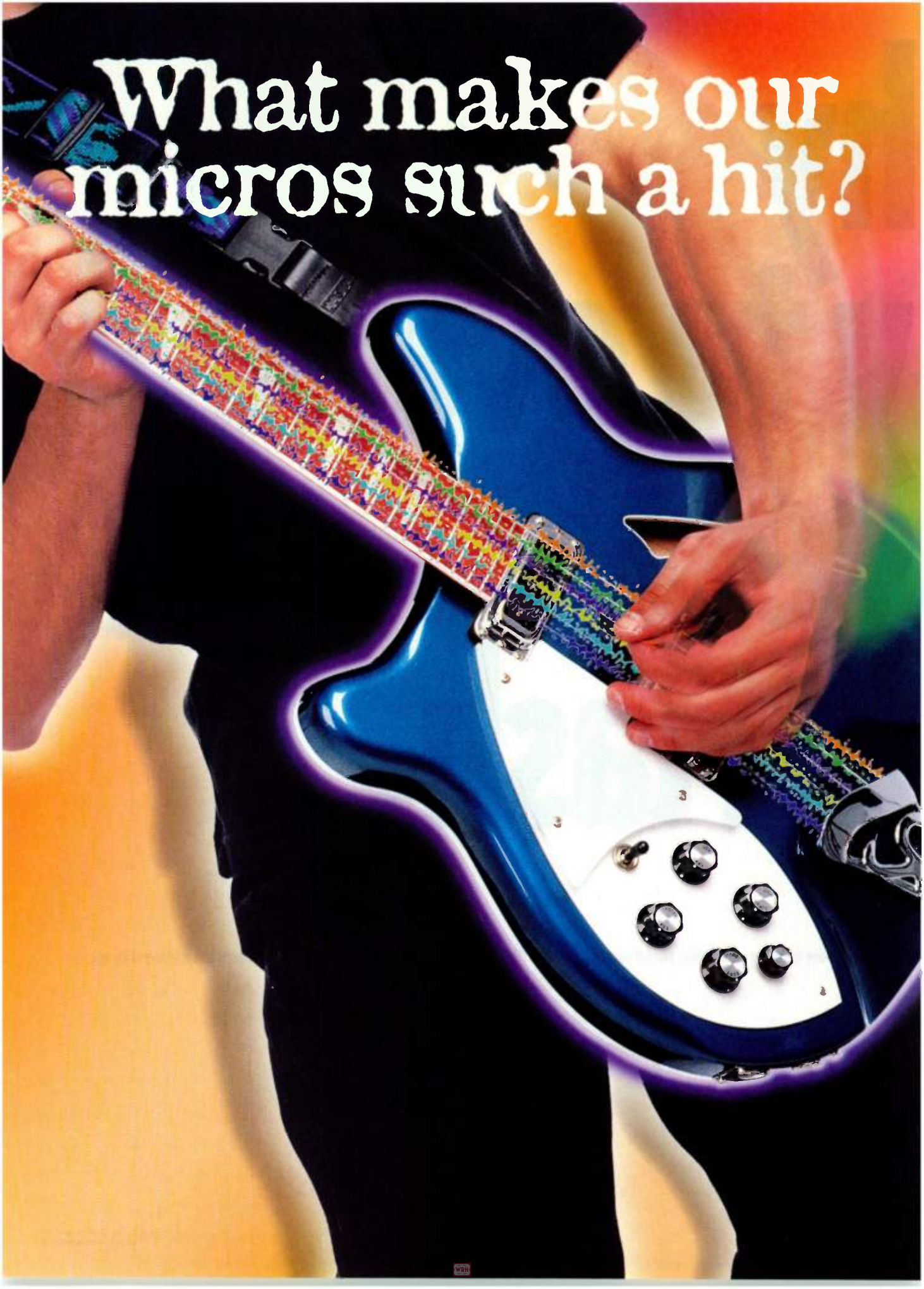
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Novice or expert, micro design-ins have never been easier, thanks to SGS-THOMSONS's Windows[®]-based *automatic code generator*, the unique ST62 Realizer. Virtual equipment like oscilloscopes and Boolean, numeric, sine and square wave generators let you test for success *before* your design is complete. Optional stand-alone starter kits make 8-bit micro development as easy as A-B-C.

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To get you from design to market as quick as possible, ST backs you with ROM, FlashROM and OTP-based ST62 micro versions. World-class manufacturing resources mean you can expect high-volume ROM turnarounds equal to or better than anything in the industry.

COMPLETE

SGS-THOMSON supports you with a ST62 device for virtually any 8-bit application. From micros with 1K program memory and the basic complement of peripherals to 8K devices with 16-bit AR timers, SPIs, UARTs, LCD drivers and more on-chip. Regardless of your application, ST backs you with everything you need to make your 8-bit micro design a hit.

Device	Program Memory Type				Program Memory	RAM x8	EEPROM x8	Timers	A/D Inputs	Serial Interface	I/Os (High Current)	Others	Package
	ROM	EPROM	OTP	Flash ROM									
ST6200	•	ST6201	•	•	1K	64	-	1x8-Bit	4x8-Bit	-	9 (3)	-	DIP16/SO16
ST6201	•	•	•	•	2K	64	-	1x8-Bit	4x8-Bit	-	9 (3)	-	DIP16/SO16
ST6203	•	ST6201	•	•	1K	64	-	1x8-Bit	-	-	9 (3)	-	DIP16/SO16
ST6208	•	ST6220	•	•	1K	64	-	1x8-Bit	-	-	12 (4)	-	DIP20/SO20
ST6209	•	ST6220	•	•	1K	64	-	1x8-Bit	4x8-Bit	-	12 (4)	-	DIP20/SO20
ST6210	•	ST6220	•	•	2K	64	-	1x8-Bit	8x8-Bit	-	12 (4)	-	DIP20/SO20
ST6215	•	ST6225	•	•	2K	64	-	1x8-Bit	16x8-Bit	-	20 (4)	-	DIP28/SO28
ST6220	•	•	•	•	4K	64	-	1x8-Bit	8x8-Bit	-	12 (4)	-	DIP20/SO20
ST6225	•	•	•	•	4K	64	-	1x8-Bit	16x8-Bit	-	20 (4)	-	DIP28/SO28
ST6230	•	•	•	•	8K	192	128	1x8-Bit/1x16-Bit AR	-	SPI/UART	20 (4)	-	DIP28/SO28
ST6232	•	•	•	•	8K	192	<128	1x8-Bit/1x16-Bit AR	-	SPI/UART	30 (9)	-	SDIP42/QFP52
ST6235	•	•	•	•	8K	192	128	1x8-Bit/1x16-Bit AR	-	SPI/UART	36 (12)	-	QFP52
ST6240	•	•	•	•	8K	216	128	2x8-Bit	12x8-Bit	SPI	24 (4)	LCD	QFP80
ST6242	•	•	•	•	8K	216	128	2x8-Bit	6x8-Bit	SPI	18 (4)	LCD	QFP64
ST6245	•	•	•	•	4K	140	128	2x8-Bit	7x8-Bit	SPI	19 (4)	LCD	QFP52
ST6246	•	•	•	•	4K	140	128	2x8-Bit	-	SPI	20 (4)	LCD	SDIP56
ST6252	•	ST6262	•	•	2K	128	-	1x8-Bit/1x8-Bit AR	-	-	9 (5)	LCD	DIP16/SO16
ST6253	•	ST6260	•	•	2K	128	-	1x8-Bit/1x8-Bit AR	7x8-Bit	-	13 (6)	-	DIP20/SO20
ST6255	•	ST6265	•	•	4K	128	-	1x8-Bit/1x8-Bit AR	-	-	21 (8)	-	DIP28/SO28
ST6260	•	•	•	•	4K	128	128	1x8-Bit/1x8-Bit AR	7x8-Bit	SPI	13 (6)	-	DIP20/SO20
ST6262	•	•	•	•	2K	128	64	1x8-Bit/1x8-Bit AR	-	-	9 (5)	-	DIP16/SO16
ST6263	•	ST6260	•	•	2K	128	64	1x8-Bit/1x8-Bit AR	7x8-Bit	-	13 (6)	-	DIP20/SO20
ST6265	•	•	•	•	4K	128	128	1x8-Bit/1x8-Bit AR	13x8-Bit	SPI	21 (8)	-	DIP28/SO28
ST6280	•	•	•	•	8K	320	128	1x8-Bit/1x8-Bit AR	12x8-Bit	SPI/UART	22 (10)	LCD	QFP100
ST6285	•	•	•	•	8K	288	128	1x8-Bit/1x8-Bit AR	8x8-Bit	SPI/UART	12 (4)	LCD	QFP80

ROM and OTP (except 624x and 628x) available in both automotive and industrial temperature range

OTP = ST62Txx

EPROM = ST62Exx

FlashROM = ST62Pxx

The ST62 range is also backed by a full range of windows based support software including a C compiler, debuggers, macro-assembler, linker and simulator and many others

For more information fax 617-259-9442
Complete product information at <http://www.st.com>



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Y2K UPDATE

As is the case with most of the transactions that are now taking place in the electronics market, Y2K concerns appear to be linking together to offer potential clients the greatest number of services possible. One company that continues to stretch its limits even further is Unisys Corporation. Recently, two different arms of the company entered into agreements that will increase Unisys' value as a Y2K service provider.

The first strategic teaming agreement involves Unisys' National Insurance practice and Scruggs Consulting, Argyle, Texas. The object of the teaming will be to provide actuarial and information services within the North American insurance market. Scruggs will be bringing the actuarial, management, and information-related consulting skills regarding property and casualty insurance to the table, while Unisys also will offer its management consulting, as well as its systems integration skills regarding Year 2000 migration, imaging, Call Center implementation and productivity, Internet/electronic commerce, and portfolio management services to the agreement.

The other improvement to Unisys' offerings is the addition of SEEC's new Smart Change 2000 solution to the company's Y2K toolset. This move makes SEEC a preferred Unisys A Series COBOL analysis and remediation software tool provider. Basically, Unisys can now market the Smart Change Factory tool suite.

SEEC's Y2K tool suite is a family of programming language analyzers and software redevelopment tools. One of the tools featured in the suite is SEEC COBOL Analyst 2000. The PC tool works by analyzing the impact of the century date change on COBOL-based information systems.

Offering a wealth of language and platform options, Smart Change Factory supports Unisys A Series, IBM MVS, DOS/VSE, and Digital VMS VAX COBOL. By providing this support, the tool slims down the number of programs needed to solve multi-vendor problems encountered in the

Y2K compliance challenge. Unisys' TEAM2000 skill centers and service offerings will all use SEEC's tools.

The TEAM2000 program is a worldwide internal professional development curriculum specifically designed to evaluate Y2K issues. TEAM2000 is offered through the Information Services Group Client Education arm of Unisys.

One of the courses offered is the "Year 2000 Awareness" one-day workshop. The workshop is organized around several presentations and "brainstorming" exercises engineered to spark participant awareness. Potential risks of inaction and ideas for successful Y2K resolution are presented in the interactive workshop.

Further in the educational program of TEAM2000 is "The System Redevelopment Methodology (TSRM) and Year 2000 Workshop." Participants in the workshop will learn the skill of the HCL James Martin methodology of Y2K analysis and planning. Both workshops can be held in-house or at a Unisys location.

For more information, contact Unisys Corporation, P. O. Box 500, Blue Bell, PA 19424-0001; (215) 986-2243; Internet: <http://www.unisys.com>.

Computer Associates International also has added a new element to its CA Discover 2000 solution, CA-Fix/2000. The automated tool offers another option to dealing with date analysis and correction of COBOL source code. The company is marketing CA Discovery 2000 as "an end-to-end solution for Year 2000 compliance."

Able to correct an entire application in a single pass, CA-Fix/2000's technology is based on comprehensive data and logic-flow analysis. The tool consists of three phases: Discover, Find, and Fix. Discover looks at the application to identify missing components. Find analyzes the application to inform the user which date fields need to be changed. And, Fix corrects the application.

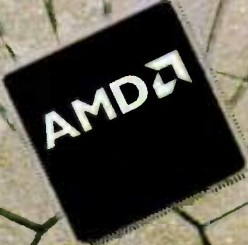
Contact Computer Associates International Inc., One Computer Associates Plaza, Isladia, NY 11788; (516) 342-5224; fax (516) 342-5329; Internet: <http://www.cai.com>.—DS

FREE STUFF

The Electronic Industries Association (EIA), along with its governing body for semiconductor device standardization, JEDEC, is making a number of semiconductor component standards available for downloading from its World Wide Web site free of charge. At present, 33 standards and publications are available on-line, including semiconductor package outline specifications; reliability test methods on surface mount moisture sensitivity; and various procedures manuals. The documents are available by accessing the JEDEC web site at <http://www.eia.org/jedec/>. As each existing and new JEDEC standards are approved, they will be posted to the web site.

National Semiconductor Corp. has made available a free design kit to help designers develop high-speed active filters. The evaluation board consists of an input buffer, followed by four cascaded Sallen Key filter sections, realized with two dual op amps. The board was designed using surface mount components, making the resistors and capacitors interchangeable. To obtain the design kit, contact National Semiconductor Corp., 4800 Wheaton Dr., Fort Collins, CO 80525; Internet: <http://www.national.com/see/activefilter>.

Burr-Brown Corp. has released an electronic data book that offers designers a comprehensive set of product selection tools available in a CD-ROM catalog. The catalog combines a parametric search engine, product selection trees, and a keyword search with applications support for quick location of appropriate products. The electronic database features over 3000 pages of high-performance linear and mixed-signal product data sheets, applications bulletins, performance graphs, and detailed specifications. For a free copy of the catalog, contact Burr-Brown Corp., P.O. Box 11400, Tucson, AZ 85734; (800) 548-6133; fax (800) 548-6133; Internet: <http://www.burr-brown.com/>.



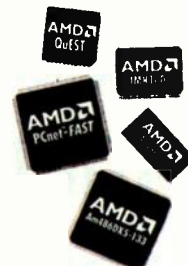
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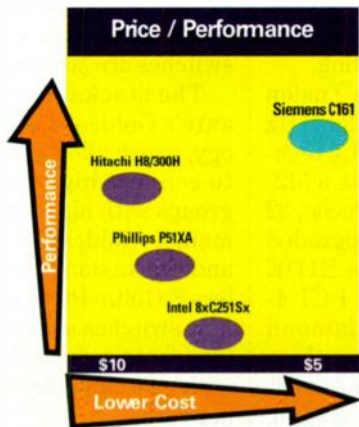
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Marshall
IT'S ABOUT TIME



HOT PC PRODUCTS

Two new PCs from Micron Electronics are the ClientPro XLU and the Millennium MME with Fusion 3D. The ClientPro XLU is designed to support business applications, while the Millennium MME supports gaming and Internet entertainment experiences. Both start at under \$3000.

The ClientPro XLU combines Intel's Pentium II processor with advanced management and networking features. By using this particular processor, Micron has hedged its bets against obsolescence, and lowered the total cost of ownership for the user.

Network connectivity is covered through Micron's participation in 3Com's Network Ready program. Micron will ship the ClientPro XLU with the 3Com network interface already configured and installed.

The new business tool comes standard with a 233-MHz Intel Pentium II processor, 512 Kbytes internal L2 secondary cache with DMI support, a 16x EIDE variable-speed CD-ROM drive, a 2.1-Gbyte SMART EIDE hard drive, a 3.5-in. floppy drive, PCI 64-bit 3D video, MPEG with 4 Mbytes of EDO RAM, upgradeable wavetable audio with speakers, a 17-in. Micron monitor, Microsoft Windows 95 or NT, 3Com Fast EtherLink XL PCI 10/100

Phoenix NoteBIOS 4.0 system software is advanced object-oriented firmware designed specifically for portable PCs. The new software from Phoenix Technologies is currently being shipped with Sony's new VAIO PCG-705C and PCG-707C notebook PCs. VAIO, short for Video Audio Integrated Operation, is the graphical interpretation of the convergence of analog and digital worlds, says Sony.

The two models are Sony's first forays into the notebook PC market. Additionally, the new notebooks are fitted with 12.1-in. Active Matrix screens, 128-bit Graphics Accelerators with 2 Mbytes of video RAM, and Direct 3D.

NIC, Intel LANDesk Client Manager, and a five-year/three-year Micron Power limited warranty.

Technologies such as Self-Monitoring, Analysis, and Reporting Technology (SMART) and LANDesk are integrated to provide the user with preventative maintenance such as disk-drive alert, self-diagnosis, and real-time monitoring and alerting.

The Millennium MME with Fusion 3D also is based on Intel's 233 MHz Pentium processor (with MMX technology). It comes standard with a 512-kbyte pipeline burst SRAM cache, 32 Mbytes of SDRAM (can be upgraded to 128 Mbytes), a 3.1-Gbyte EIDE hard drive, a Monster 3D PCI 4-Mbyte graphics card, a Diamond Stealth Pro DX 4-Mbyte graphics card, a 32-voice wavetable, an Advent Black 370 speaker/subwoofer system, a 56-kbit/s modem/fax, Universal Serial Bus connections, a 24x variable-speed CD-ROM drive, a 100-Mbyte Iomega Zip drive, Micron's new bundle of games, a Microsoft Sidewinder Pro Joystick, a 17-in. color monitor, and a five-year/three-year Micron Power limited warranty.

Contact Micron Electronics Inc., 900 E. Karcher Rd., Nampa, ID 83687; (208) 893-3434; fax (208) 893-3424; Internet: <http://www.micronpc.com>.

Sony uses PowerPanel, BatteryScope, and MultiKey SMC51L from Phoenix Technologies in the PCG-705 and PCG-707C to promote longer battery life. Built into SMC's new Ultra I/O controller (FDC37C957FR), the MultiKey/SMC51L is an advanced keyboard BIOS item. Sony's new notebook PCs have the distinction of being the first laptops to use the new microcontroller.

Sony's new notebook PCs start at \$3500.

For more information, contact Phoenix Technologies Ltd., 411 East Plumeria, San Jose, CA 95134; (408) 570-1000; fax (408) 570-1001; Internet: <http://www.phoenix.com>.



IntraStack and IntraSwitch from Asanté are two new switches designed to improve intranet information flow while integrating the switching structure with Windows NT servers. The IntraStack is a 10/100 stackable Fast Ethernet switch and the IntraSwitch is a 10+100 desktop switch. Both switches are scalable.

The stackable switches use Asanté's Goldcard connector technology, which allows network managers to connect high-bandwidth workgroups with high-speed network segments. Goldcard connects the base and expansion modules via a cableless 2-Gbit/s PCI expansion bus. The new switches are unique in that they integrate intranet-based software with switching hardware to manage networks.

Included with the switches are built-in HTTP servers. These servers allow the manager to configure network devices via any standard web browser. The servers also integrate with IntraSpection, the company's web-based network management software. By integrating either of the two switches with IntraSpection, users will have automated intranet software updates, interactive management linkage, unified web security, and intranet services monitoring.

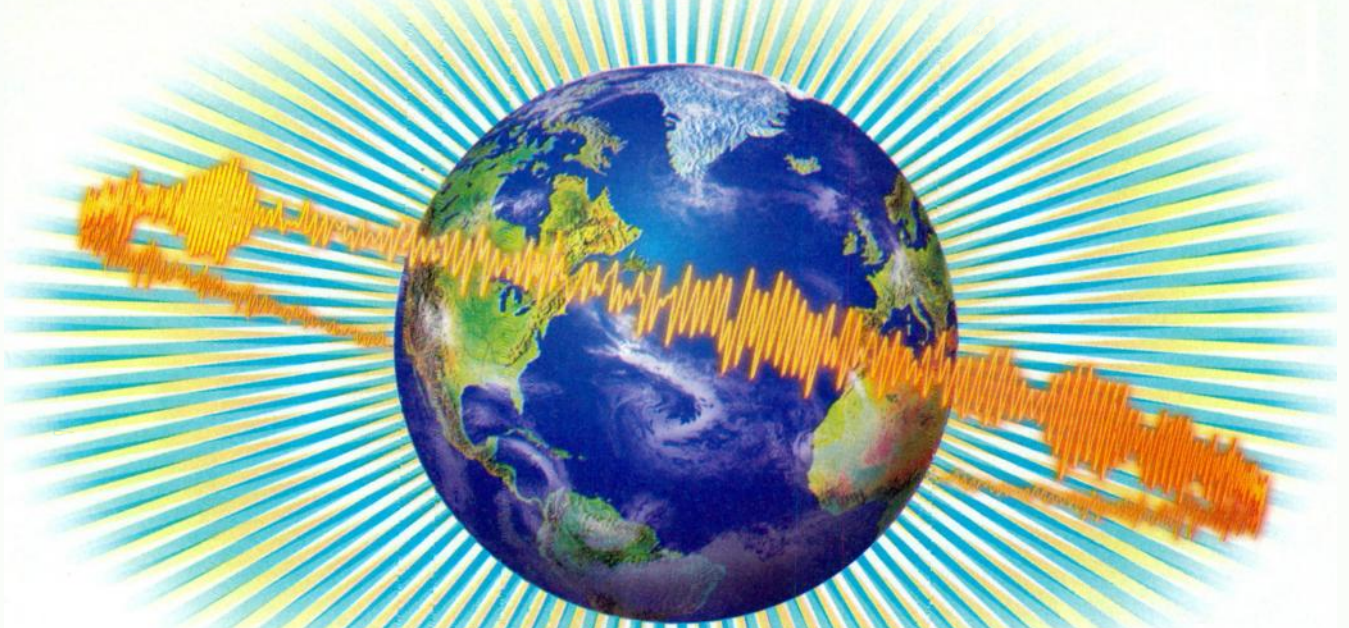
IntraStack supports up to 46 Fast Ethernet connections or a variety of switched 10 or 100 copper or fiber links (half or full duplex). The unit is stackable up to three high, supporting 14 dual-speed 10/100 switched ports on the base unit.

IntraSwitch features 24 10-Mbit/s ports and three high-speed "fat pipes." The design promotes configuration flexibility to support legacy Ethernet LANs and dedicated switched connections of graphics intensive workgroups.

IntraStack is priced at \$4750 for the 14-port base module and \$6295 for the 16-port expansion module. IntraSwitch is priced at \$2750. Both switches carry a three-year warranty and free technical support.

Contact Asanté, 821 Fox Lane, San Jose, CA 95131; (408) 435-8388; fax (408) 432-1117; Internet: <http://www.asante.com>.

FIELD PROGRAMMABLE ANALOG ARRAYS



It's an Analog World.

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For digital system designers making do in an analog world, life can often become, well...a real rat's nest. But with Motorola's new family of Field Programmable Analog Arrays (FPAA), the industry's first true analog counterpart to Field Programmable Gate Arrays (FPGA), digital designers can now create custom analog IC designs with the same flexibility as a digital FPGA.

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Motorola's FPAA architecture provides flexible arrays of analog building blocks, which can be configured and interconnected by software to create circuit functions that solve real-world signal processing problems. When used with supporting CAD tools, FPAA's enable analog IC designs with low risk and minimum design expertise.

Complete Software Solution

Motorola's EasyAnalog™ software, which provides a friendly user interface in a Microsoft Windows™ environment, allows designers to construct complex analog circuits by selecting, placing and wiring high level analog circuit blocks like biquad filters, summing amps, integrators, and more. The circuits can then be downloaded to the FPAA via the PC computer's serial port. Users can do rapid prototyping,

and deployment of leading-edge products for a variety of applications, without spending extensive design time on custom ASICs or being limited by the capabilities of standard parts. And like our FPGAs, the FPAA can be reprogrammed whenever desired.

Get the Kit NOW!

The MPAA020 FPAA is available in Development System Evaluation Kit #MPAA3DS that includes an evaluation board with a component breadboard area, user's manual, PC interface cable, and power supply. Plus a CD-ROM containing Motorola's EasyAnalog interactive design tool.

Ready to start enjoying the flexibility previously limited to digital programmable semiconductors? Then Motorola's new FPAA family is for you. For more information visit our website at <http://sps.motorola.com/fpaa>.

The Future of Programmable Technology is Motorola.



MOTOROLA
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Imagine Being Able To Look At A Digital Design Problem This Way.



This view of system behavior was provided by the HP 16500C logic analysis system and the HP 16505A prototype analyzer.



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What Is Known-Good Die And How Do You Get There?

The Lack Of A Well-Defined Test Process, Or Even A Standard For The "Known Goodness" Of Bare Die, Hasn't Hurt—So Far.

John Novellino

Normally, the lack of a consistent standard against which you can measure a product's performance would seriously hinder its growth potential. Add the disagreement about how the product should be defined and the product should be dead in the water. Not so with known-good die (KGD), the unpackaged, bare die that are sold with the assurance, in one form or another, that they will work as expected when placed by customers into their multi-chip modules (MCM).

Designers have steadily increased their use of KGD in MCMs, perhaps even to the point of specifying them when the design doesn't really need their space savings and performance advantages. And there still is no firm definition of what constitutes KGD, or standard for what processes should be employed to ensure known good die.

KGD, defined one way or another, are available from several major semiconductor manufacturers and die-processing companies. The main reason for wanting bare die "certified," if you will, as known to be good is that once they are placed on MCM substrates, problems caused by individual die can be difficult to diagnose and result in costly repairs or low MCM yields.

Obviously, a rigid, mathematically based definition of "known good" is what most customers would like. How confident can the customer be that the die will work when it is placed in the MCM? But semiconductor manufacturers seem to

shy away from such definitions. Instead, they prefer to define KGD as having the same performance, quality, and/or reliability as their packaged counterparts. As good as the packaged parts may be, however, customers are left to wonder whether that's good enough for MCM applications, which have a different set of economic rules.

And make no mistake, very high confidence levels are important to the economic viability of many MCMs. The first-pass module yield is directly related to the number of die in the module and the confidence level. For instance, Gene Cloud, vice president of marketing at Micron Technology Inc., Boise, Ida., notes that a high-performance microprocessor MCM containing 10 components, each with a 95% chance of remaining fully functional

through manufacturing, would result in a module yield of only 60% (Fig. 1).

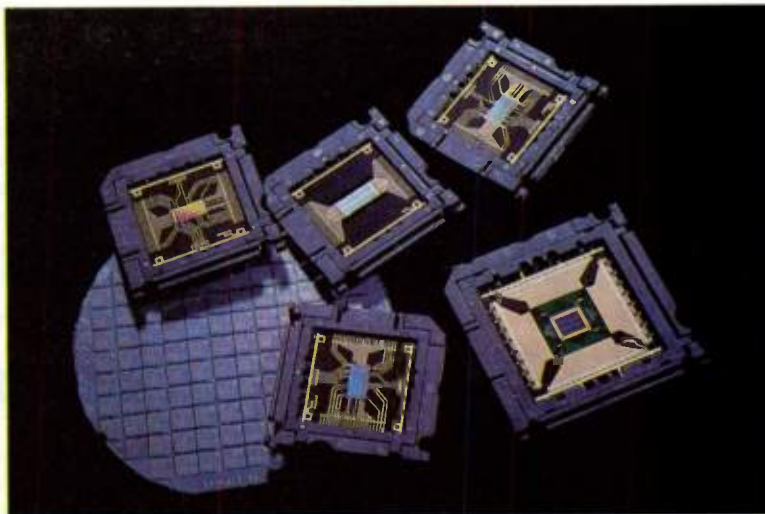
Too Much Rework

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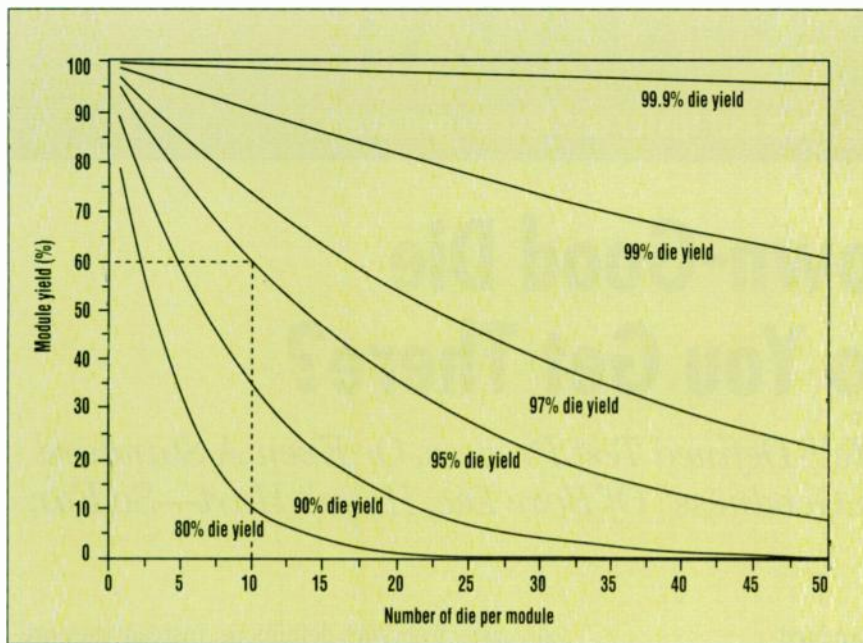
At those levels, module rework and scrap costs could make up a large portion of the final module cost. If electrical and manufacturing defects could essentially be removed at the bare die level, the MCM's yield could top 99%.

Thus Alan Wood, Micron Technology's KGD manager, defines KGD as die that's fully tested and burned-in in the same manner as a packaged part would be. Micron Technology uses an authorized die distributor, Chip Supply Inc., of Orlando,

SPECIAL
REPORT



Art Courtesy: Chip Supply Inc.



1. Module yield is directly related to the confidence level and the number of die used. For yields that make multichip modules economically practical, designers must use die that have a very high confidence level.

Fla., to do the testing and to supply customers.

The availability of fully tested and burned-in KGD significantly reduces module rework, decreases cycle time, and drives down the cost of the final product. It also improves module reliability, allowing designers to develop more complex and cost-effective MCMs. As for whether the designer must specify KGD or can get away with less expensive devices, Wood says it's basically a matter of how many die will be used in the module and how mature the particular die are, because mature die have very high yields.

Potential users of bare die could use some educating on that point, notes Mitch Myers, president of Semi Dice Inc., a wafer processor and die distributor in Los Alamitos, Calif. Myers says that there may be as many definitions of KGD as there are people involved in the industry, but his definition is: a die that has been tested to the same parameters as a packaged device. After 21 years in the business, he's often heard that you can't use bare die unless it's known-good die. That's not totally true, he says.

"In fact, the majority of devices that we supply are older technologies, so the manufacturing processes are pretty much pat," says Myers. "The devices have been made the same way for years

and years and the yields are up. We're talking about a lot of logic devices or linear devices for which known-good die testing is throwing your money away. The devices are proven. The manufacturing processes are proven."

The added expense and processing for KGD are needed when the die being used are newer, less mature devices, and are more complex and expensive. He says, "If it's newer devices and high-pin-count devices, then they probably need to have

known-good die. Then again, I think most of the die being sold today are not those devices."

The problems involved in testing bare die are the biggest factors inhibiting the growth of the industry, according to a survey conducted by Semi Dice. The company distributed the 15-question survey to the majority of the major semiconductor manufacturers earlier this year. In answer to the question, "What technical factors currently effect the broader use of bare die?" 36% of respondents picked the inability to test ac parameters (Fig. 2). The second highest answer (25%) was yield considerations, which might even be construed as related to the difficulty in testing the bare die.

Myers believes that for KGD use to really take off, testing must be performed by the manufacturers. "Third-party houses just do not offer the economies of scale that the manufacturers can provide," he says.

Ed Perrott, president of Chip Supply, agrees that the economy of scale of packaged parts dwarfs that of bare die. He estimates that a semiconductor manufacturer that is doing well in the bare-die business is selling about 98% packaged devices and 2% die.

Guaranteeing Specs

Perrott has his own perspective on what KGD means. "Known-good die has very little to do with functionality, whether the part is good or bad," he says. "It has to do with the ability to

KGD Event Emphasizes Applications

With the theme "Competitive system solutions using die products," the Known Good Die Industry Assessment Workshop will focus on system-level applications of KGD and on reducing costs in manufacturing and implementation (shipping media, handling) of KGD. The annual workshop's goal is to promote a continuing dialog between suppliers and users of KGD. This year's meeting, the fourth, will be held at the Embassy Suites Hotel, Napa Valley, Calif., September 17-19.

Representatives of the international community have been invited to participate in this year's meeting. Speakers from the European Commission's Good-Die project and the Electronic Industries Association of Japan are scheduled to present updates on work in their regions.

The Workshop is sponsored by Sematech, the research and development consortium of 10 semiconductor manufacturers; the Microelectronics and Computer Technology Consortium; and the Electronics Industry Association (EIA). For further information contact Eric Samuelson at the EIA at (703) 907-7546; fax (703) 907-7549; e-mail: kgd@eia.org.

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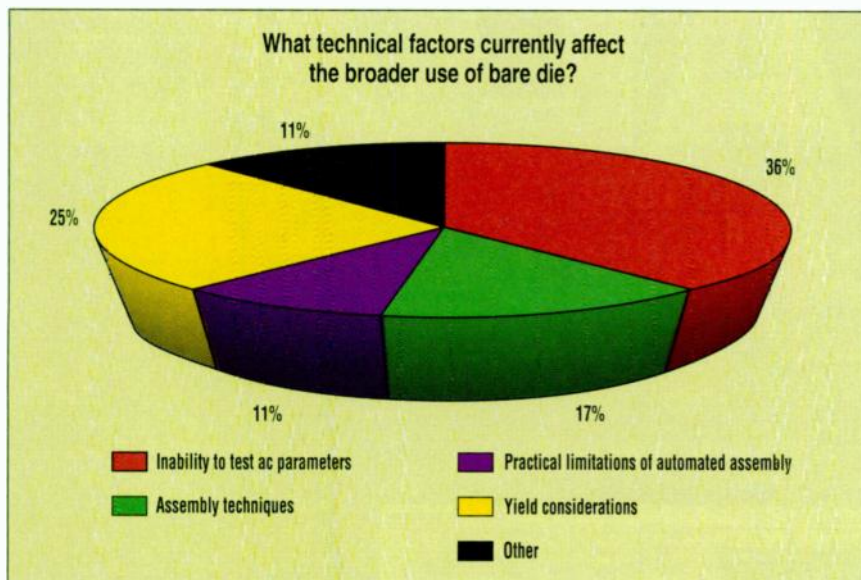
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2. The problems involved with the testing of bare die are the biggest factors affecting the growth of their usage, according to a survey by Semi Dice Inc.

guarantee certain characteristics, whether the part functions over the temperature extremes that you might want, and whether the part has the reliability that it needs," says Perrott.

Using bare die, particularly in MCMs, offers more advantages than just space and weight savings. Putting several die closer together and eliminating package interconnections boosts performance by cutting propagation and transition delays. Also, fewer interconnects can increase reliability in the finished product.

But, as always, there are trade-offs. The lack of interconnects also makes it difficult (that is, expensive) to test 100% of the devices for all the ac and dc parameters tested in a packaged part. Wafer-level testing means the die is not well isolated. Probe-tip capacitance problems slow down readings and make it hard to test at-speed, says Perrott. Also, you need precise lengths of coaxial cable to measure speed.

Those trade-offs may lead to misunderstandings among potential customers, who can't see why they should pay as much, or even more, for a part that doesn't come with a package. Perrott notes that it may cost from \$0.19 to \$0.30 to package and test a memory device as a 32-44-pin plastic part. Eliminating that cost doesn't leave much room to economically test the part as a bare die. The economics improve when you're dealing with a microprocessor or FPGA that would nor-

mally go into a more expensive, ceramic pin-grid array, says Perrott.

Neither scenario, however, takes into account the fact that manufacturers are set up to make millions of packaged parts a day, but have to disrupt their processes to handle relatively very small orders for bare die. Perrott compares that scenario to ordering an unpainted car from General Motors. The automaker would have to charge extra for the special handling.

To cut the cost of testing, Chip Supply is buying an automated die loader from Bear Technology, Plano, Tex. The loader will take the die off the membrane, put it into a temporary package, put a lid on the package, and place it into a carrier. After testing, the assembly goes back into the machine, which takes it apart and puts the die into a wafer pack. The loader, which interfaces with Chip Supply's test equipment, should handle about two million parts a year, allowing the company to approach packaged-part price parity.

Look At The Total System Cost

Rather than concentrating on die cost, potential users of bare die should look at the total system cost, the size and weight savings, and the ability to integrate additional functions, according to Sherb Bridges, business unit manager for National Semiconductor's die products group, South Portland, Maine. National's standard for KGD is basically that they will meet

their data sheet specifications just like a packaged part, he said.

As for what type of testing should be done to achieve that goal, Bridges said the company likes to discuss the customer's needs, then come up with a solution. "We prefer customers not to test themselves," he says. "For one thing, we don't like to release certain vectors and software, etc. And also, we're the experts in semiconductor testing and processing. So tell us what yields you need, tell us the application, and tell us the quality. Let us determine the processing and testing."

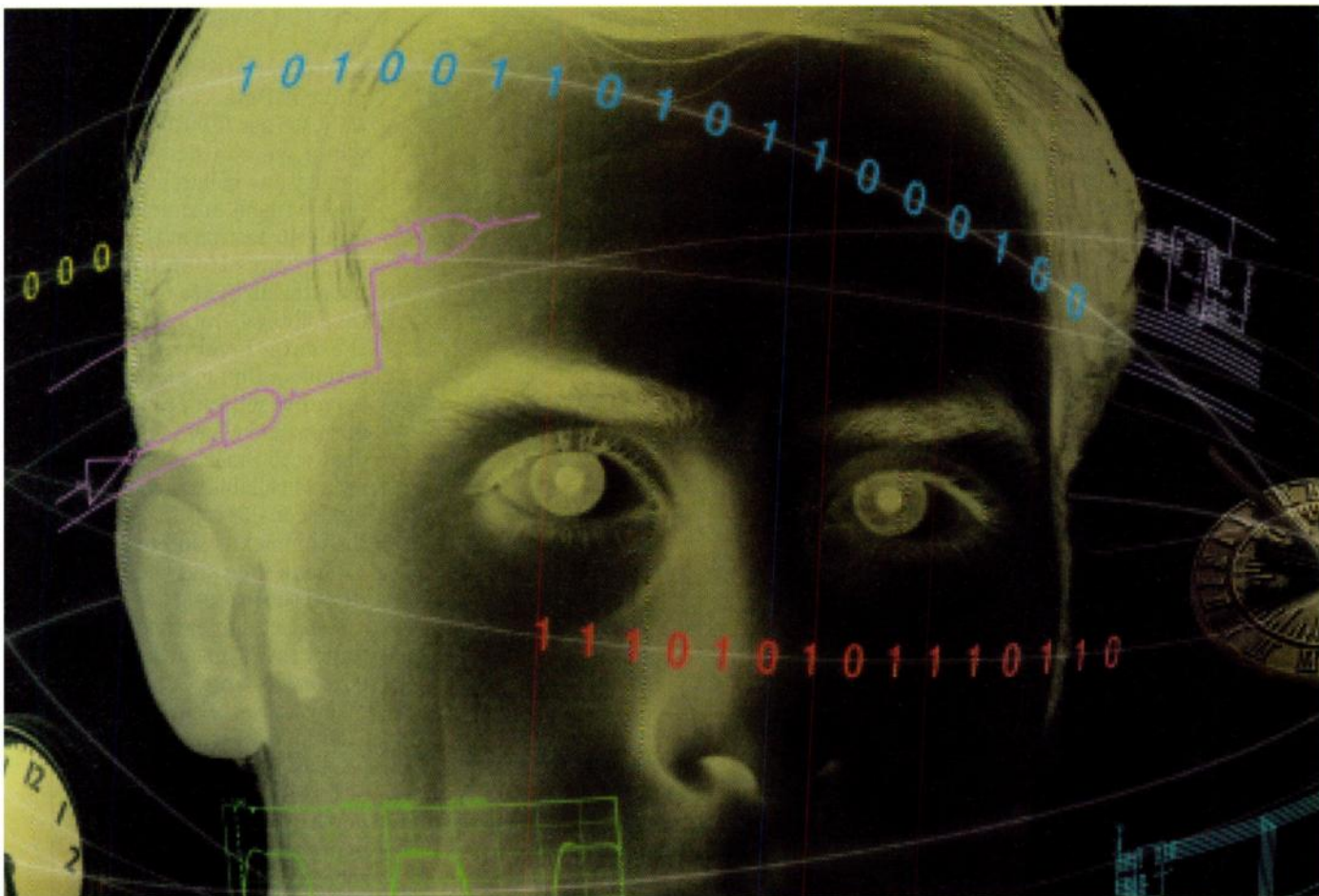
National prefers to do all testing on the wafer, and has developed hot and cold temperature probes so that die can be tested from -55°C to +140°C. Some products require burn-in, however, and in those cases the company uses temporary die carriers. These carriers allow the die to be handled individually through burn-in and electrical test.

The decision to burn in depends on the application as well as the device. "In most cases, it's a combination of the application that the product is going into as well as the historical yield data on that product from a packaged standpoint," says Bridges. "If the packaged parts don't require burn-in, then we don't burn the die in. If they do require burn-in, then we look closely at the application. If it's going into a military application, a space application, or a life or death type of application, we look closely at whether it requires burn-in. If it does, we advise the customer."

Besides directly supplying die to customers, National maintains working arrangements with three die processors. "Our feeling is that for high-volume applications, we're the experts and we're very cost-effective," says Bridges. "But we can't serve the total market. Die processors have an extensive customer base and a very good sales force that understands die. They having testing expertise as well, and they know how to service the smaller accounts as well as the larger accounts. So it's almost like another distributor for us."

Third-party suppliers can probably do a good job generating KGD for many devices, but may have a problem with the more complex devices, notes Weldon Beardain, KGD and MCM manager at Texas Instruments' Semiconductor Div., Midland, Tex. "The

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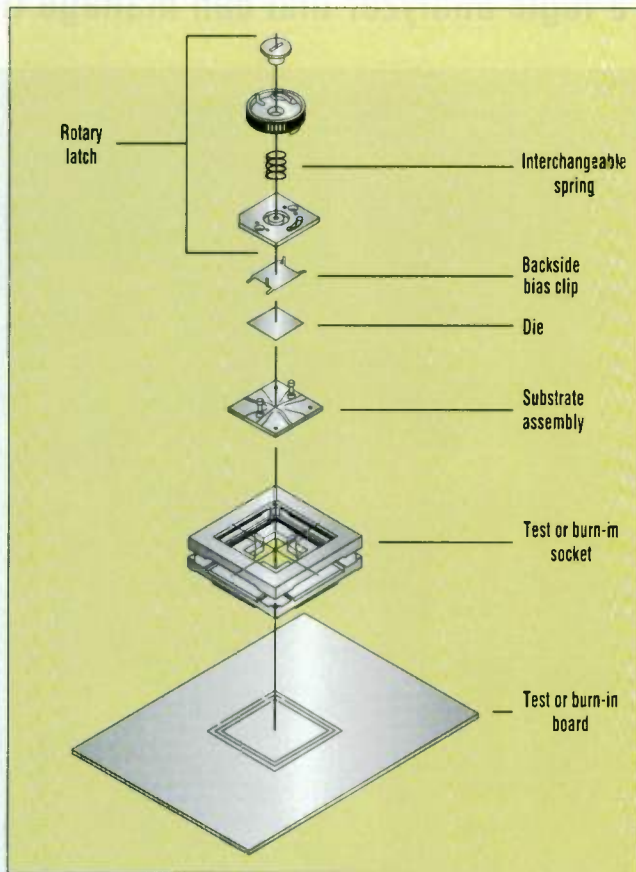
real problem comes if I were to give them some of our most advanced DSP chips," says Beardain. "The third-party folks would not have the test infrastructure to test those products. The vector sets have been optimized for a certain brand of tester. If I were to give them the test program and vector set there's no possible way that they would be able to use them on their test equipment without several man-years of work unless they exactly duplicate our test equipment."

TI defines KGD as having the same reliability and quality as the packaged part, says Beardain. For commercial parts, that means the die is warranted to the packaged version's data sheet parameters, and has the same reliability, assuming the user properly places the die and maintains the correct operating range. Military die also have the same performance and reliability as their packaged counterparts.

A misconception that customers may have is that KGD means that every die is tested and burned-in. That's not even done for every part in TI's commercial catalog of packaged parts, says Beardain. "In today's commercial market, I think you'll find that if burn-in doesn't buy you anything it may not be done on the flow at all," he says. Burn-in is pretty expensive for the commercial market. "So typically, if we can't get a product to the reliability level that we think it needs to be without burn-in, we'd probably be reluctant to offer it as a commercial KGD," he says.

Brute Force May Be Needed

But TI's major KGD thrust in the military area is in its DSP family. For a number of those products the company uses what Beardain calls brute-force methods for making sure they are sufficiently tested. One option is to place each die into a temporary chip carrier based on TI's DieMate technology, which also is used by some other die suppliers (Fig. 3). Other flows offer the die in tape-automated bond



3. A temporary die carrier, such as this DieMate system from Texas Instruments, allows semiconductor manufacturers or die processors to individually test die as if they were packaged parts.

form, and for those products the company can do a temporary attachment to a tab tape.

For small and experimental runs, the die may even be placed in a standard package with temporary wire bonds. After it has been run through the required tests, the bonds are removed. Beardain says TI has developed some proprietary mounting compounds that can be baked out after test.

Intel Corp. also uses the DieMate system for burn-in testing of bare die. The temporarily packaged ICs are run through the same test flow as the company's packaged parts, including hot-and cold-temperature testing, says Steve Heimlich, marketing manager for Intel's die product line in Chandler, Ariz.

"Basically, the way we look at known-good die is as another packaging option within certain product lines," he says. "So the way we see it, the quality and reliability has to be consistent with our packaged parts." But because KGD means different things to differ-

ent people, Intel doesn't use the term, calling their products the SmartDie line instead.

Another process Intel employs is SmartSort. "Basically, we use it with products when we can achieve our quality and reliability objectives without burn-in, and we do all our testing at the wafer level," says Heimlich. "We have the ability to test across the full temperature range at the wafer level with all full screens, timing, etc." To determine which parts need burn-in and which can be handled with SmartSort, a quality and reliability group analyzes considerations such as the complexity and maturity of the device and the maturity of the process.

Heimlich agrees that it's better for the IC manufacturer to do the testing, if possible. "They know the product best. They know best how to test the product," he says. "The trade-off is that to do die-level testing you have to have a commitment to doing it, and the resources and support to be able

to do it. I don't know that every company has that." If not, it makes sense to have a third-party supplier who specializes in bare die do the testing.

As to when designers should specify die, Heimlich says Intel's basic position is that die are appropriate in systems where packaged parts won't fit. "So if a package solution works in one of our customer's designs, we encourage then to use packaged parts," he says. "If it doesn't fit in their design, then they have the option and the flexibility of using die."

The company's not out to convert package customers to bare die. "What we're trying to do is provide customers with a little more flexibility so they can meet whatever form-factor objectives they have for their products," says Heimlich. "

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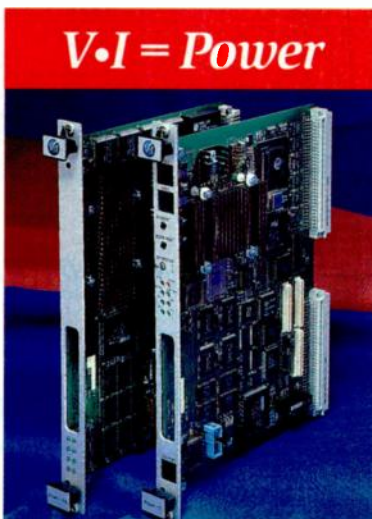


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UPDATE ON THE INTERNET

Tools And Protocols Link Embedded Systems Over The Internet

According to Jerry Fiddler, president of Wind River Systems, "The Internet is going to radically change how you think about what an embedded system is. It's no longer just something by itself; now, it's something you can monitor and control from any browser."

The ability to access and control small, remote instruments and networked devices of all types from equally small and mobile handheld devices, as well as desktops, is making the network into the interface. Devices that until recently might have a set of switches or some buttons as a user in-

terface are now sprouting graphical-user interfaces (GUIs). They can now be controlled remotely with graphical switches, buttons, and gauges.

The prominence of the network and graphical interface means that, from a user's point of view, a number of remote, geographically dispersed embedded devices can theoretically be integrated in one client display and appear to the user as one device. All the individual networked devices could exchange data with the user and with each other. If such devices were small, dedicated instruments, for example, it would still be possible to access the full, up-to-date

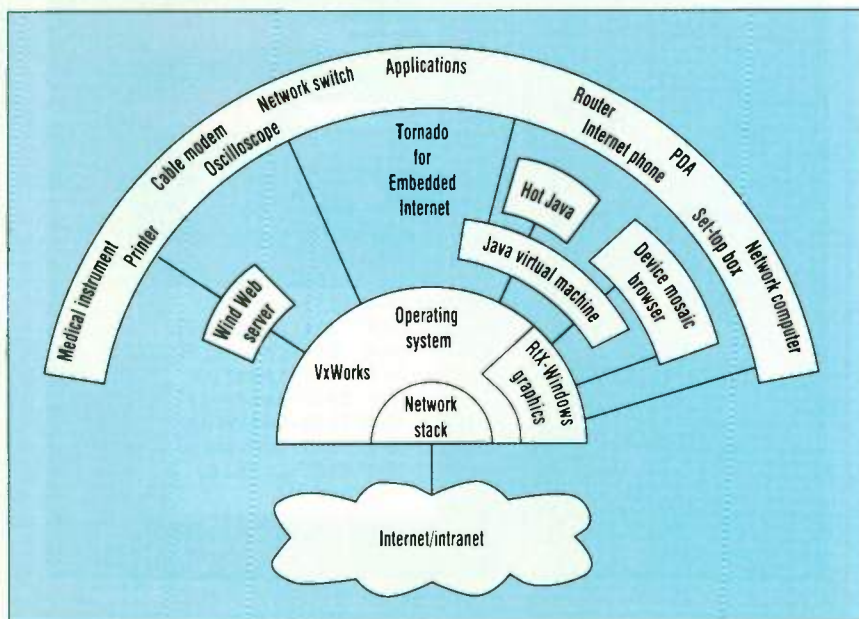
user manual on the whole system simply by having a link from the dedicated devices to a larger server. To the user, it would still appear as one system. And it would be a system that could be reconfigured and redesigned at will.

Of course, making all this happen requires an infrastructure, operating systems, tools, and services designed for creating embedded systems that can work on the Internet. And more companies are providing enabling technologies for doing just that. Specifically, tools need to address server technology, runtime support, HTTP, browsers, and Java. In addition to companies like Wind River Systems and Integrated Systems Inc. (ISI) that are providing comprehensive development support for a broad range of Internet-enabled systems, there are those focusing on more specialized areas and very small devices.

Wind River Systems has put together a suite of components called Tornado for Embedded Internet that are integrated into their Tornado development environment. The company's flagship real-time embedded operating system, VxWorks, is part of the suite, but remains unchanged. The other components are specifically aimed at developing embedded systems for the Internet. Integration with the Tornado environment provides access to over 100 third-party development tools (*Fig. 1*).

Many embedded devices will have to play the role of small Internet servers, and an embedded HTTP server will look different than a server does for desktop systems. For one thing, it has to be like any other embedded component—small, ROMable, and portable. The WindWeb server can get down to as little as 10 kbytes and can be accessed by any browser. Secure sockets and an authentication facility provide security.

While servers aimed at the desktop allow two-way communications through forms, interacting with an embedded device is different from just pulling up pages. Most all of what goes on with embedded Internet devices is



1. Aimed at developing embedded systems for the Internet, the Tornado environment provides components with over 100 third-party development tools.

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dynamic. The server is sending changing data at a periodic rate. That data may dynamically change graphical elements representing gauges or other indicators on the client display. There needs to be a way to closely link the display to the data. WindWeb uses dynamic "value tags" that get to variables and functions within the application and speed the update between the user and the remote device.

A Mapping Scheme

WindWeb also provides a mapping scheme to separate the content, i.e., the HTML pages or user interface elements that will be placed on an embedded server, from the programming or the actual code that runs the device. The content developer, who is more of a graphics designer than a programmer, can link files in a form, for example, to function calls in the program through a symbol table created by the application programmer. That way, the page developer need not and can not get to the program code. He or she needs no knowledge of C or C++ programming and doesn't have to modify any code to establish links to the user interface. In addition, the look and feel of the interface can be changed without having to modify the underlying code.

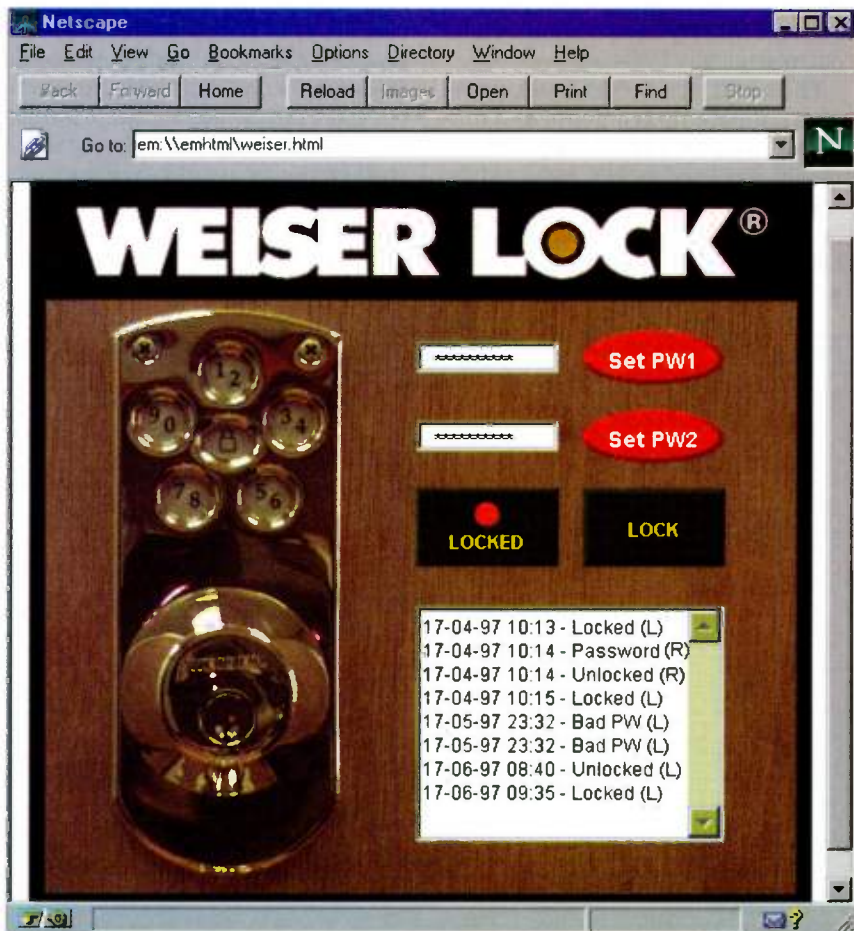
ISI has a small, scalable HTTP server called pSOS/HTTP Server that can be linked with existing pSOS applications or used to build new embedded Internet applications. The package is compliant with HTTP 1.0 protocol and supports the common gateway interface (CGI) 1.1 protocol, as well as the HTML 3.0 upload capability. The pSOS/HTTP Server can be implemented as a diskless system or provided with a file system manager to operate with disk or ROM.

The CGI capability lets a user start a task or application on demand from a web browser. The CGI application can

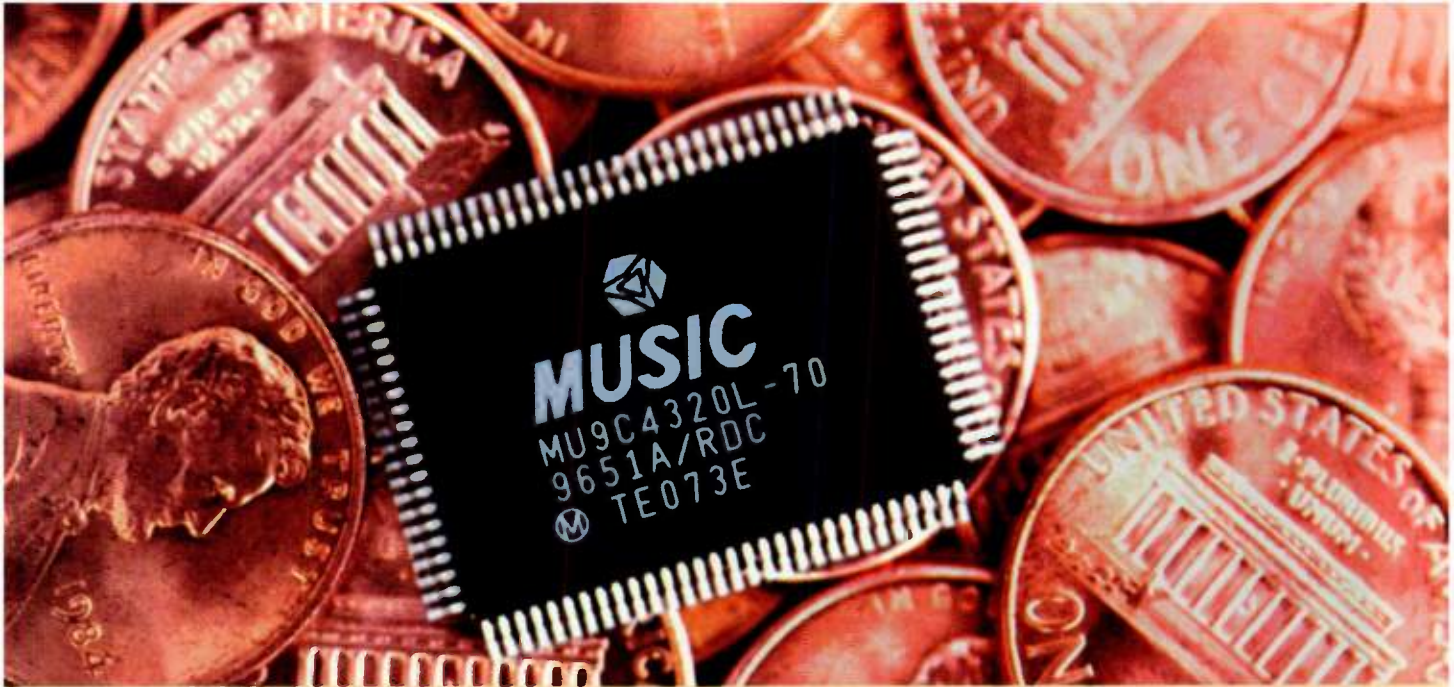
be directly linked to the HTTP application or dynamically loaded at the time of the request. Either way, the CGI application has a way to communicate data and parameters with the browser. HTML (or Java applets) can be used to build a user interface to remotely interact with the embedded system. ISI also provides two security measures. IP filtering maintains a list of approved client IP addresses. The IP address of the user logging on is compared with the list and only approved IPs are processed. In addition,

the server supports user name and password authentication to determine "who are you?" in addition to "where are you calling from?"

For the user-interface design, Tornado for Windows supplies a graphics package called RtX-Windows. It's based on the X11 standard graphics API and is supported by a sizeable set of drivers for different graphic display devices, such as LCD panels. In addition, Wind River has licensed browser technology from Sun Microsystems in the form of its HotJava, and from Spy-



2. Because the emObjects can be made to look like gauges, sliders, switches, or knobs, they can be customized and combined with other elements to give the appearance of the device under control.



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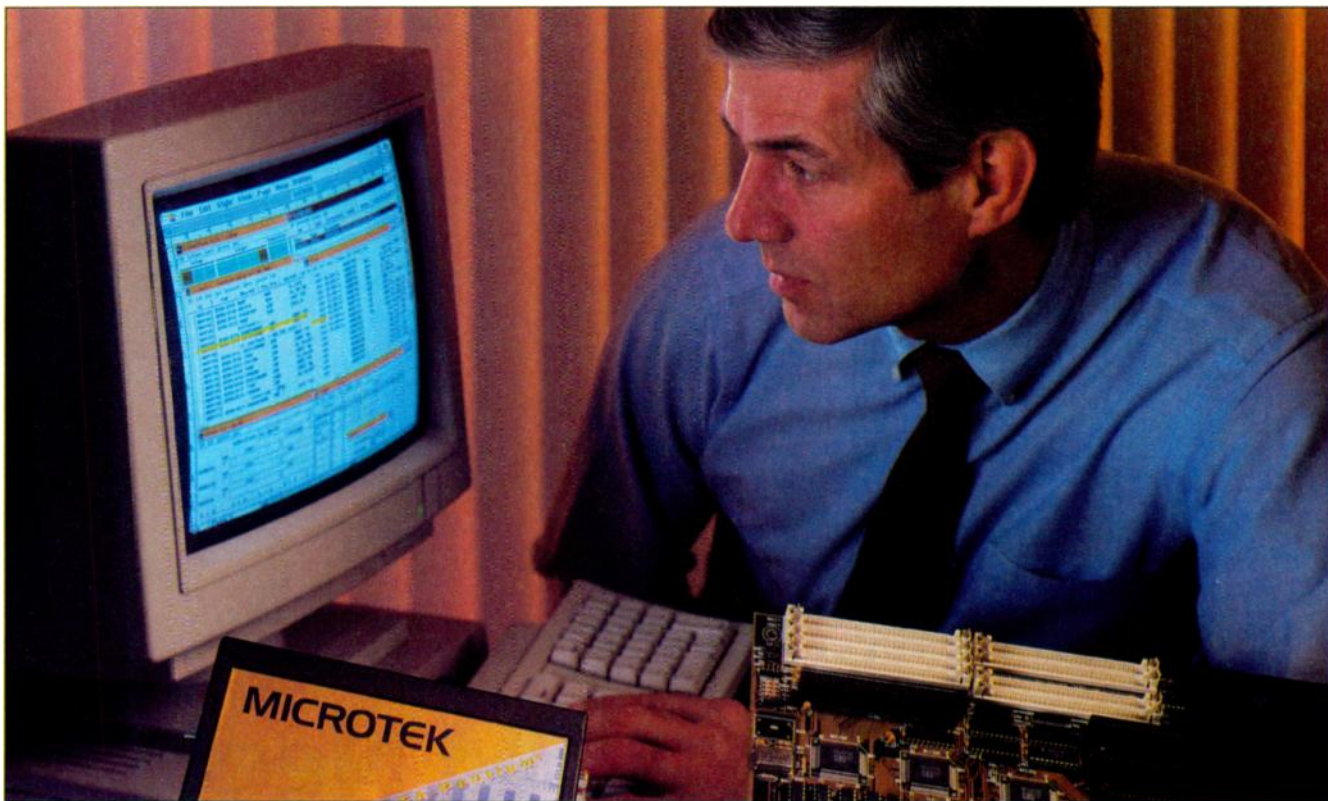
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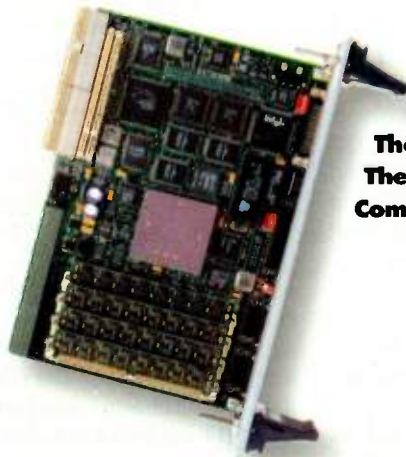
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EMBEDDED COMPUTERS MEMORY MODULES FLASH CARDS COMMUNICATIONS PRODUCTS

glass Technology in the form of its Device Mosaic. Device Mosaic is a modular browser that can be adapted for various embedded and handheld devices such as personal digital assistants (PDAs).

Finally, there's support for Java. Wind River has licensed Java from SunSoft to maintain the 100% certification of compliance. Specifically, they have licensed the JavaOS which includes the language and an OS kernel. However, the JavaOS kernel has been stripped out and substituted with the VxWorks kernel.

"Java has received the most press, but really is only one component of the embedded Internet picture," says Wind River's Fiddler. Putting Java on top of VxWorks has made it possible to link Java threads to VxWorks tasks so that applets can communicate directly with the underlying embedded application.

ISI supports Java on its pSOS system of embedded real-time software. Because pure Java as defined by Sun Microsystems is not real time, ISI offers a real-time version called PERC. PERC was developed by Newmonics, Ames, Iowa, in a clean-room version developed according to the Java language specification that includes some real-time extensions. PERC currently doesn't support the abstract windowing toolkit (AWT) of pure Java, but Newmonics is trying to define a subset of the full AWT functions for building user interfaces in embedded systems. This means that there's probably no close communication between Newmonics' efforts and those announced by Sunsoft to develop an EmbeddedJava. Unless there's eventually one standard, the usefulness of Java for applications involving embedded Internet devices will be less clear.

Getting Even Smaller

Embedded Internet devices require a lower size limit. For example, to directly connect to the Internet, they need a TCP/IP stack. TCP/IP has been a stable protocol for a long time, but is now getting leaner and more efficient. The latest version BSD 4.4 stack offers a 15% to 20% performance increase and takes fewer CPU resources. Still, very tiny net-

worked devices won't be able to afford the memory overhead required by TCP/IP. Connection to the Internet is still possible, however, through proxy servers that connect to the Internet and route traffic to small devices over a simpler network, such as a serial link. In addition, storing HTML pages, let alone Java applets, is not an option for many smaller devices.

A company known as emWare has found a way to network devices built around 8-bit microcontrollers in such a way that they can be accessed and controlled by a standard Internet browser running on a PC—devices as small as residential door locks connected to home security systems. Systems based on emWare's embedded micro-interface technology (EMIT) also can be scaled up to very large systems. Naturally, to accommodate very small designs, the bulk of the software functionality must reside on the client system and not on the embedded server.

EMIT implements a very small, special-purpose web server that can fit in just 750 bytes of ROM and about 32 bytes of RAM. Called emMicro, the tiny server communicates with the underlying state machine on the microcontroller, using a simple serial communication protocol called emNet to send 5- to 64-byte packets over most transports, including wireless. The combination of emMicro with emNet constitutes the "thin server" of the EMIT system.

The "fat client" part of the scheme includes emManager, which runs on a PC

in about 250 kbytes and communicates with a standard Netscape web browser. The beauty of EMIT is the small amount of data that's passed between the client and server. The data, in the form of "microtags," are 1- or 2-byte packets that define device controls. On the server side, the exchange variable depends on the underlying control software. That software could be as simple as a state machine running on an 8-bit microcontroller, or a complex RTOS-based application on a 32-bit processor. For example, an arriving microtag might deliver a value to a variable that tells the controller to set a valve.

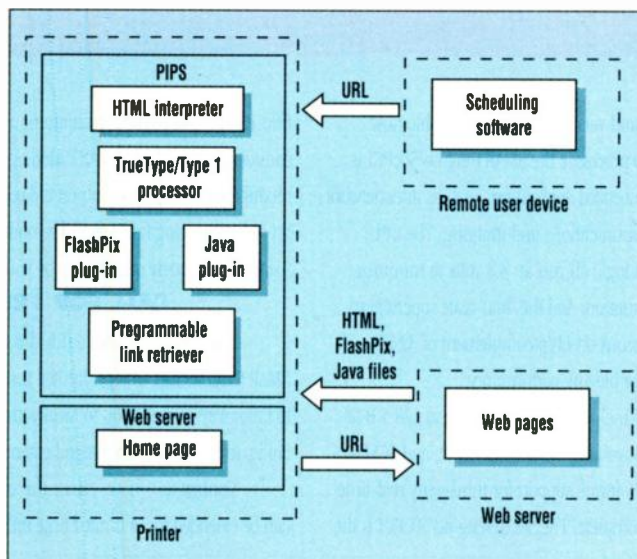
On the client side, microtags undergo "dynamic expansion." The client-resident emManager can recognize each microtag's ID and associate it with an emObject, which then blossoms into the elements in the user interface that displays data and can be manipulated for control. These emObjects are contained in a library of small, pre-programmed functions. These functions are small Java applets that reside on the client side rather than the embedded server side. Each microtag is associated with an emObject on the client side and with a program variable on the server side.

The emObjects look like gauges, sliders, switches, buttons, or knobs, and can be customized or combined with emObjects and user-created graphic elements to obtain user interfaces that look just like the device under control (Fig. 2). Because the only data actually exchanged are the microtags containing IDs and variables, the network traffic is very low.

Normally, an EMIT system would exist on a private dial-up or closed network using the emNet protocol. For access from anywhere in the world over the Internet, there would have to be a proxy server that could run TCP/IP, and an application that could communicate with the EMIT-based system over a serial or wireless link.

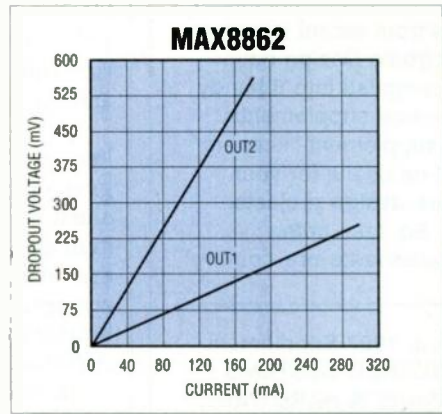
Legacy Systems

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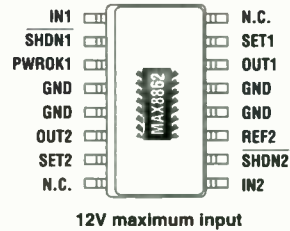
3. Expandable with plug-ins, the basic HTML engine can support its own web page, with the right browser technology.

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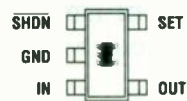
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systems for Internet connectivity in the form of its IPoint product. Vadem has designed a single-chip platform around the NEC V30MX CPU core. The VG330 includes the 32-MHz, 80186-compatible core along with an LCD controller, keyboard controller, real-time clock, PCMCIA controller, and a power-management unit.

The software includes a real-time kernel, a communications library, a graphics and user-interface library, and a set of core utilities for memory management and for managing data structures, such as hash tables, strings, and lists. Between these libraries and the user applications is an API to allow development in C.

The software suite is designed to stay relatively simple and to keep memory overhead to a minimum. For example, the communications library contains a compact TCP/IP stack, along with SLIP, PPP, modem, and dialing functions, but leaves out some optional features in the link and transport layers. Normally, OEM would support SLIP or PPP, but not both, given the dedicated nature of most embedded applications. User-interface support comes in the form of a set of display functions and drivers and an object-oriented set of mechanisms for drop-down menus, text entry, labels, and other widgets.

Vadem envisions the type of systems designed with IPoint as available over direct dial-up from a client, or able to access the Internet themselves using a proxy service running on a server connected to the Internet. The Internet POP would be the point of universal Internet access, but the IPoint-enabled devices could call their POP and leave data to be retrieved by the client or forwarded on.

Vadem provides examples and reference designs for retrofitting existing embedded systems with IPoint Internet capability. The development aids include two versions of the library—one for debugging on a PC, the other for development and debugging directly on the target system. Sample applications, including an e-mail and a net-connect application, are provided, as well as a linker/loader and a ROM conversion utility.

Direct Web Printing

In the spectrum between general tools for embedded Internet devices to

specialized solutions, Pipeline has opted to focus on a new paradigm for printing. The company has developed an HTML interpreter for OEM printer manufacturers that let a printer download and print pages directly from the web. In current desktops, web pages can be printed, but only indirectly by translating the HTML page format to the printer's native language such as Postscript, PCL, or GDI.

The HTML interpreter is the first stage in Pipeline's effort to develop a comprehensive system it calls Power-Page Internet Printing System (PIPS). As a system embedded in a printer, PIPS could be used with browser technology that Pipeline is licensing from other vendors to allow automatically accessing and printing of a list of web pages.

The basic HTML engine can be expanded with plug-ins, such as Flash-Pix image compression or Java (Fig. 3). With the browser technology, it can support its own web page. Users could then access the printer remotely to tell it to get certain pages that can't be printed from a handheld device.

In addition to the HTML interpreter, which is a piece of portable software, Pipeline offers a core-based ASIC processor based on the Hewlett-Packard PA-RISC architecture. The W90100 microcontroller contains a rich mix of peripherals designed for imaging, including integrated JBIG compression technology, parallel and serial interfaces, and an 80486-compatible bus design. OEMs can choose to use the software and processor as an integrated solution or move the code to existing or new hardware designs.

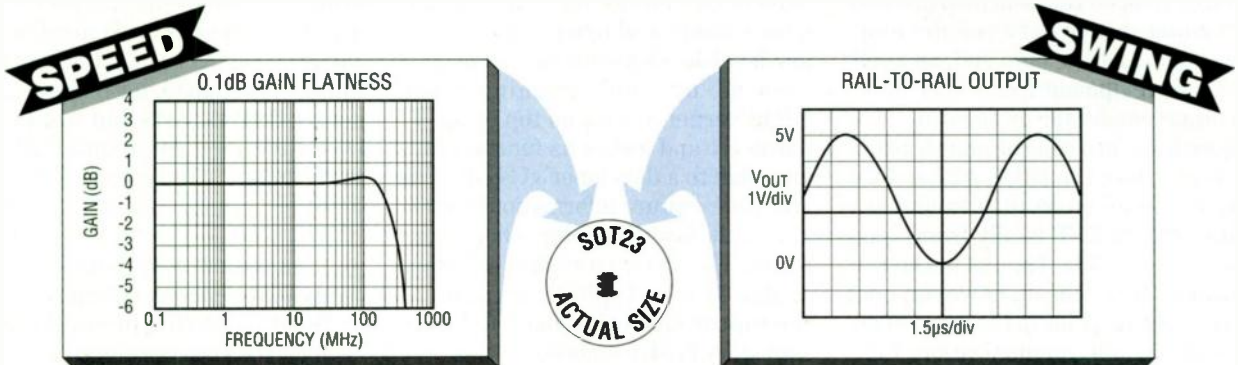
As more organizations move to Internet protocols and establish their enterprise networks as intranets, embedded Internet devices will continue to proliferate. This is especially true as users become more mobile and companies see the advantages of "virtual intranets" behind security firewalls on the Internet. The range of products that will incorporate Internet technology appears endless.

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UPDATE ON DSP DEVELOPMENT

Standard Interfaces Are Helping To Smooth The Road To DSP Development

The road to digital signal processing (DSP) development is getting smoother. At the low end of the spectrum, a new DSP/BIOS API has been developed that will help promote interoperability between development tools. At the high end, an application development framework offers an object model for integrating DSP algorithms into telecommunications systems. Both the BIOS API and the object model currently target the TMS320C54x DSP family from Texas Instruments (TI). Thanks to the raw power of DSP silicon, however, both developments point to the trend of implementing telecommunications functions that were previously built in hardware entirely, in software.

System-Level Functions

While there are a number of quality tool suites available for developing DSP algorithms, interoperability between tools has been hampered by the need to reinvent system-level facilities for nearly every project. Recently, Spectron Microsystems Corp. announced an implementation of Texas Instruments' DSP/DBIOS API called BIOStation.

BIOStation consists of two parts: a target-resident preemptive multitasking kernel and a set of visual, host-based, real-time analysis monitoring and capture tools. The kernel takes about 1024 16-bit words (2 kbytes), and provides basic tasking, preemptive I/O, capture, and statistics services. The set of tools in the BIOStation takes advantage of these kernel facilities, and can make the kernel services available to a wide range of development tools. In addition, the kernel capture and statistics services provide instrumenting applications so that they can supply real-time information to other host-based tools. All those tools that adhere to

the BIOS standard will be able to exchange information.

By using the DSP/BIOS, developers can develop algorithms and device drivers to address application needs more quickly, and bypass much of the low-level development needed to get a system up and running. The BIOS/kernel resides on top of the TI hardware and makes its function calls available to a developer's C code. The real-time capture information is available to the host computer, where it can be used by debuggers and software analysis tools. Applications that use the capture facilities also can be designed for field diagnosis.

A development board incorporating the DSP/BIOS API, the Tiger 542/PC, is available from DSP Research. The kit includes BIOStation, with the kernel running on the board and the tools hosted on a PC. The Tiger 542/PC uses the TMS320C542

processor, and offers a choice of 64 kbytes or 256 kbytes of SRAM. It provides a mix of peripherals including stereo 16-kHz ADCs and DACs, 2 8-bit DACs, an RS-232 UART, and an RJ-11 telephony interface.

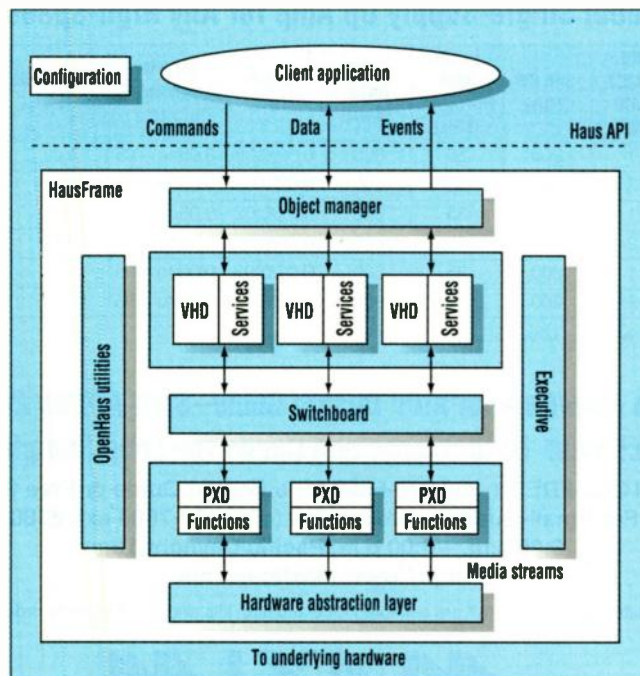
An Applications Framework

Development of DSP algorithms is still the province of specialists. However, the field of applications that can use those algorithms is much larger, and growing every day. Telecommunications specialists, for example, may not be DSP experts, but need to use DSP functionality to build dynamically configurable systems. These may include private-branch-exchange (PBX) and key systems, feature phones, voice-over networks, and computer telephony systems.

To address this need, HotHaus Technologies has developed an object-model and software framework that lets developers bind core DSP algorithms together, interface them to hardware channels, and provide low-level services such as arbitration and task management.

HausWare Renaissance is a software architecture that resides on DSP hardware and manages objects and their connections. There are two types of objects: virtual HausWare device drivers (VHDs) and physical device drivers (PXD) (see the figure). VHDs are connected to PXDs via a software crossbar switch (the "switchboard") within Renaissance. Objects are connected under the control of a client application through its API called the HAPI (Haus API). The application can disconnect one set of drivers, load another set from memory, and connect them as needed. PXDs and their associated low-level functions connect to the underlying hardware channels via the hardware abstraction layer (HAL).

VHDs can be plain old telephone service (POTS) phones, full-duplex speaker phones, voice terminals, etc.

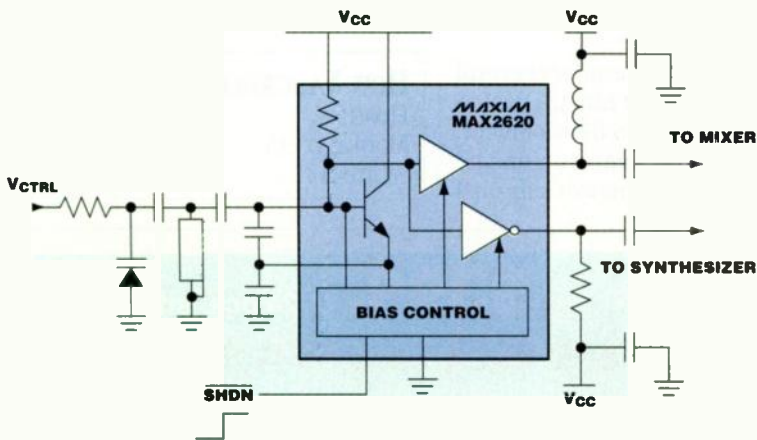


HausWare Renaissance connects virtual device drivers (VHDs) that implement communications applications such as voice terminals, fax devices, and modems to physical device drivers (PXD) and hardware communication channels via a software crossbar switch. The software framework runs on DSP hardware with its own real-time executive. It communicates with client applications such as switches and routers via its own application programming interface (API).

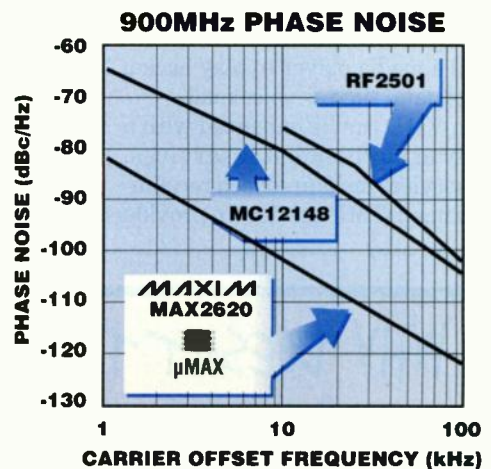
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Each VHD comes with a set of basic services. For example, the POTS phone includes DTMF detection and activity detection. The full-duplex speaker phone has line-echo cancellation and a media player to play back a buffer of data, such as voice mail.

Each VHD can be enhanced with a number of supplemental services. These services include speech recognition, faxing, DTMF service (to provide

caller-selected menus, caller ID, and modems. However, the framework also includes a set of utilities and services called OpenHaus that allows third-party developers create custom VHDs and services.

In addition, HotHaus offers several software development kits (SDKs) to aid in client-application development. Client applications can run on the same DSP as the framework or on a

separate microcontroller. For example, a router or telecom switch might perform its routing algorithms on a microcontroller and manage the DSP operations on the DSP processor via the HAPI interface. The SDK includes the TI C compiler, a JTAG emulator board, and a debugger. Another SDK includes DSP hardware modules with telephony interfaces so that software developers can get started before hardware is available.

On a simple level, it is possible to use the drag-and-drop user interface from a PC to configure a communication system on a DSP board without writing a single line of code. Normally, however, the user interface would be replaced in a deployed system by a client application that could be written in C or even Visual Basic.

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PRODUCT FEATURE

Software Makes It Possible To Store Code And Data On A Single Flash Device

Designers of compact embedded systems are always looking for ways to reduce component count in their systems. Many applications, such as cellular phones, modems, and engine control systems, store control

code in flash memory while storing system and user data in EEPROM. The reason is that until now flash memory hasn't been able to read code and write data in parallel. While flash memory can read individual bytes, it must per-

form writes by block and most devices are unable to suspend the write operation if there's an instantaneous need to execute code. Intel, Santa Clara, Calif., has developed a method based on software that lets certain devices with a write-suspend capability perform read and write operations in parallel without the burden of additional circuitry.

In most current cellular phone designs, for example, there may be three types of storage: flash memory to store program code, EEPROM for permanent data storage (settings, phone numbers, etc.), and a certain amount of SRAM for temporary data storage and program execution stack. Getting both program and data storage on one device in a cost-effective manner has been a challenge.

Intel looked at several approaches to the problem, including the idea of combining flash and EEPROM technologies on a single die. While such an approach might have worked technically, it didn't address the cost issues of EEPROM, which has considerable lower density than flash and costs about 30 times more per bit.

Adding duplicate I/O circuitry to allow flash memory to read and write concurrently would have added cost, as well as raise issues of isolation because of the differences in read and write voltages. Moreover, there still would have been a need for software to manage the data-storage process because of the byte-readable/block-erasable nature of flash. Putting two flash dies in one package would have added complexity to the manufacturing process and resulted in devices with a fixed code/data boundary. This in turn would have necessitated a range of options for customers with differing needs and would make manufacturing inefficient.

Intel's FlashFile family of devices and the newly introduced line of Smart 3 advanced boot-block flash memories have the ability to suspend the write cycle as well as the read cycle. It's therefore possible to use a software solution to read and write to the same device without adding any more circuitry. In fact, any other manufacturer's flash devices can use the same technique provided they can suspend the write cycle and the read cycle.

Called Flash Data Integrator (FDI), the software manages storage on a sin-
(continued on page 106)

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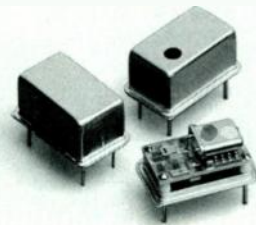
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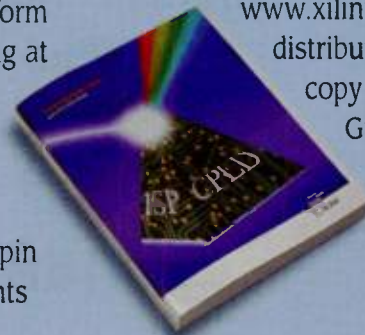
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READER SERVICE 171

PRODUCT FEATURE

(continued from page 104)

gle device and provides real-time interrupt handling for code execution using a familiar EEPROM-like user API. The FDI takes advantage of CPU idle time to buffer data in the SRAM and store it in the flash memory. Intel's analysis revealed that in a typical GSM phone, there can be up to 70% idle time. Of course, the processor still must respond instantly to interrupts such as someone

starting to speak or enter a number. Analysis also showed that current designs have enough leftover SRAM space to easily buffer the data prior to storage without increasing SRAM.

FDI foreground manager temporarily queues data to be stored in a portion of SRAM and waits for CPU idle time. It also prioritizes flash write requests. When the CPU goes idle, the write/erase operation begins. The FDI background

manager moves the data from SRAM to flash and performs flash reclaim. Should there be higher priority interrupts, the background manager halts the write/erase operation until the higher priority task completes. It then resumes until the operation is completed.

FDI also provides manufacturers with flexibility in defining their code/data boundaries. The amount of memory on the device that's to be allocated to code or data is set at compile time. The Smart 3 family now comes in 4-, 8-, and 16-Mbit versions, with eight 8-kbyte data blocks and 64-kbyte main blocks for added flexibility. Designers are better able to change their mix of code and data as a product evolves without changing the device. The FDI software is distributed royalty-free in C source code. Once compiled, it requires about 2 kbytes of RAM in the system. It uses familiar EEPROM-like commands such as: open, close, delete, get, read, write, and reclaim.

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Software Math Coprocessors Rival Hardware Speeds

Thanks to a library of ROMable, re-entrant software routines, designers can make cost, performance, and memory trade-offs that enable floating-point computation in systems at speeds comparable with those of hardware coprocessors. The SuperSpeed soft coprocessor math libraries created by Log Point Technologies, Mountain View, Calif., use a method of numerical processing called exponential floating-point processing (EFP). EFP is based on a fully logarithmic data structure and fast logarithmic and exponential data conversions.

EFP requires the use of a new normalized number type. For single-precision operations, the normalized number is represented by a 32-bit word consisting of a sign bit and a 31-bit un-

(continued on page 108)



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PRODUCT FEATURE

(continued from page 106)

signed biased exponent. The exponent has an 8-bit integer portion and a 23-bit fraction portion. For a normal single-precision EFP value of v , the 31-bit exponent is the base-2 logarithm of the magnitude of v .

For 16-, 32- and 64-bit microprocessors, the libraries can provide precision of 20, 22, or 24 significant bits in the 32-bit format using between 17

and 55 kbytes of memory. The libraries also are available for 8-bit microprocessors and microcontrollers in a 24-bit data version for DSP applications, as well as the full 32-bit format.

The soft coprocessor libraries come in two architecture versions. The M architecture performs best on processors with fast 32-by-32-bit integer multiply capability. The N architecture uses lookup tables to make up the speed of

integer multiply. By using look-up tables, the N architecture can offer trade-offs in terms of memory size. The choice of lookup-table size affects the number of significant bits of precision attained. For example, 7-place precision requires 55 kbytes, while 6-place precision requires only 17 kbytes.

Functions supported by the soft coprocessor include: add, subtract, multiply, divide, square, square root, cube root, power, $2x$, ex , $10x$, \log_2 , \ln , \log_{10} , xy , sine, cosine, tangent, arcsine, arccosine, arctangent, and arctangent2. It also performs data conversions between 32-bit EFP format and 32-bit IEEE 754 floating-point, integer, and ASCII representations of decimal numbers. The execution speed of these functions compares favorably with conventional execution using a hardware floating point coprocessor.

For developers who utilize C++, Log Point provides a class library with operator overloading. C++ doesn't directly provide data type overloading. Thus, the library called "efloat" replaces the float data type by adding a preprocessor command that will go through the source file and change all references from "float" to "efloat." Then the program is recompiled with that class library and all floating point operations are processed in exponential floating point in the log format. No other changes are required.

Programmers needn't concern themselves about the mechanics of the calculation, but instead simply code their algorithms the way they always have. In addition, there's a number of C source soft coprocessors available for use with popular compilers.

Log Point also provides extensions to the GNU compilers, which lets developers recompile existing C code without alteration. A drop-in math library executes the "float" operations replaced by the "efloat" routines. Log Point also offers a set of no-proprietary C code forms at no cost to tool vendors who make modifications or extensions to support the EFP libraries.

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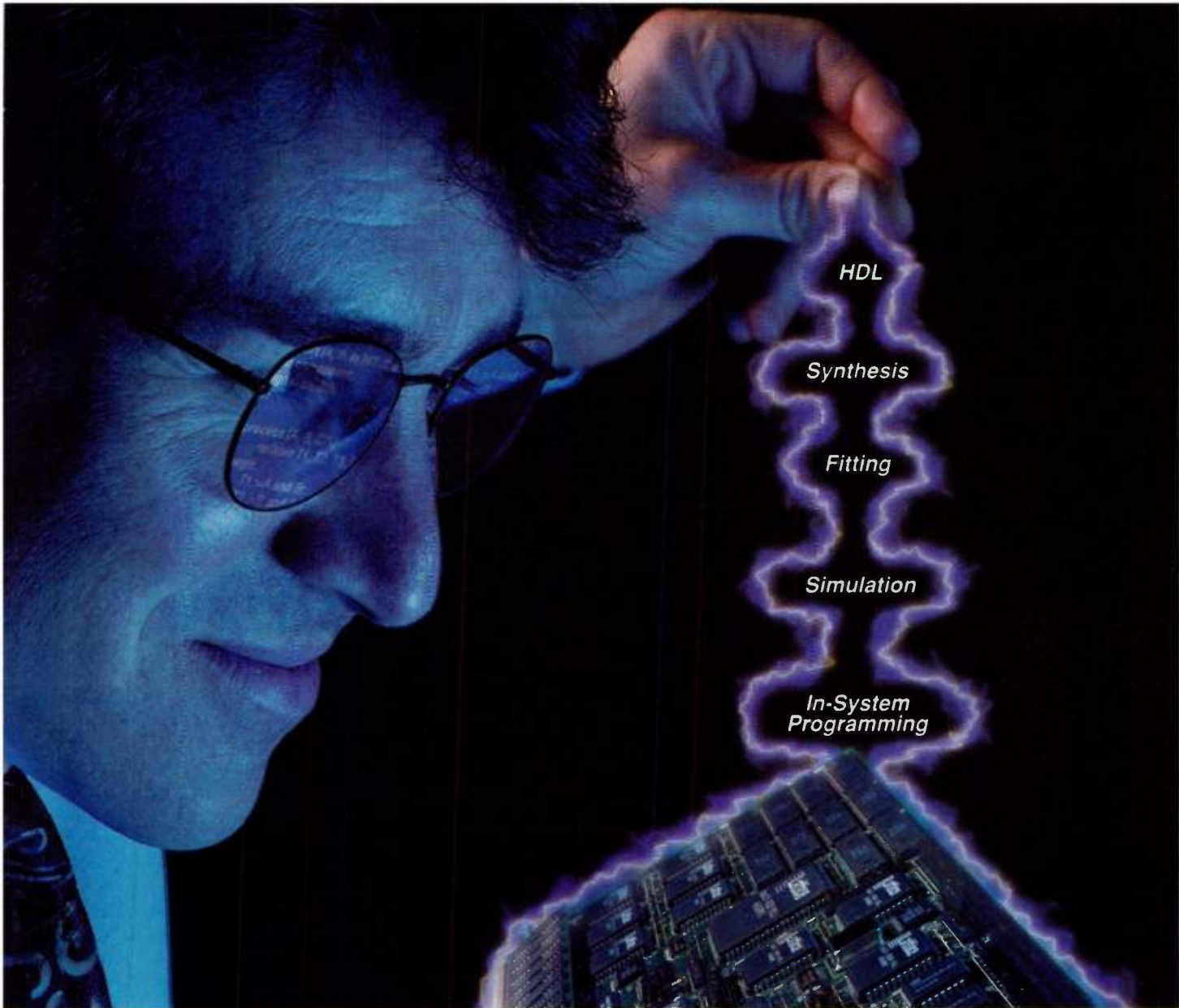
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Virtual Prototypes Move Toward Automatic Test Suite And Code Generation

As much as 50% of development time can be spent on the user interface of a typical embedded system. This isn't just designing the "look and feel" of knobs and displays. The human-machine interface (HMI)

truly defines the functionality of the system. Get that right and you've gone a long way toward setting and fulfilling design requirements.

Rapid PLUS, created by Emultek, Herndon, Va., includes tools that let de-

signers produce a realistic graphical representation of a user interface, whether it's a cellular phone, an aviation system, or a medical instrument. Connecting it to an underlying state machine will then activate the graphical representation to check how a human user will interact with it. A fully functional model of the user interface (and external outputs under control of the system) should be a full functional prototype. But that's just the first step.

Rapid PLUS includes a graphical editor with a library of HMI objects; the user can create additional objects. By hooking objects and their functions together with the logic editor, you can define the look and behavior of a virtual prototype with no programming. From the virtual prototype, you're able to generate an interactive HTML document that's a specification report. The report contains screen captures of each object, e.g., each button of a cellular phone as well as a textual description of each object's relationship to everything else. Finally, the specification report contains all of the underlying state diagrams that apply to the virtual prototype.

Rapid PLUS is currently able to automatically figure out all of the possible states that a system can be in. As you enter test cases, the tool keeps track of those that have yet to be exercised. Test cases can be listed in HTML format with complete captures of the inputs and outputs. Emultek is moving toward complete automatic generation of test scripts.

The fourth capability of Rapid PLUS is full automatic code generation, which Emultek is co-developing with Motorola (it's expected to ship toward the end of the year). From the virtual prototype, you will be able to automatically generate C or C++ code. That code can then be embedded in the target system and connected to the functional algorithms to drive the HMI. The prototyping, specification report and test script modules are available today and the automatic code-generation module will be released in September.

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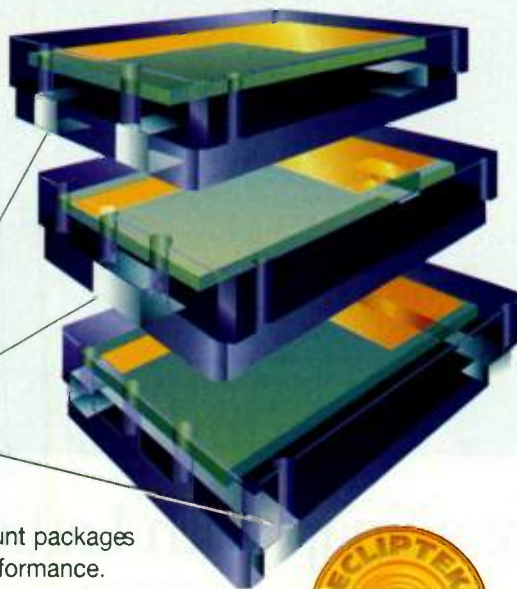
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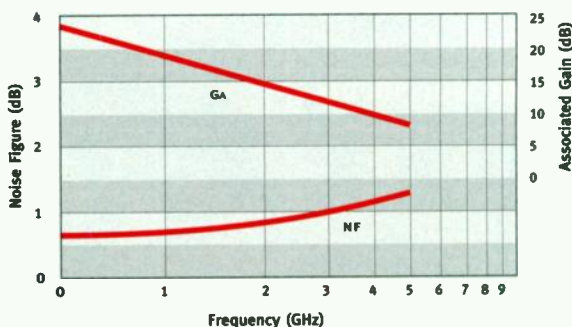
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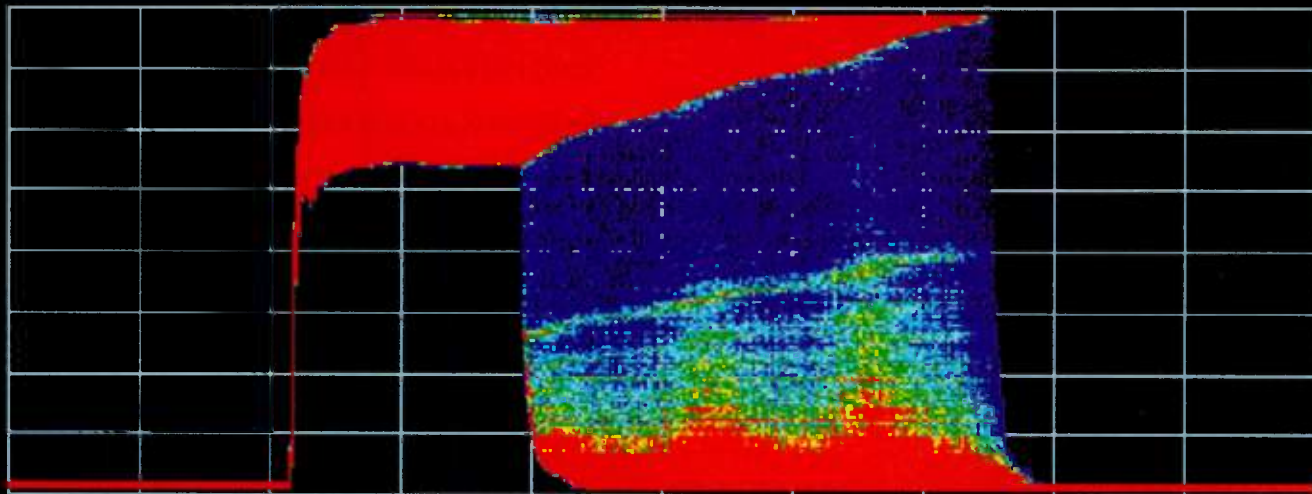
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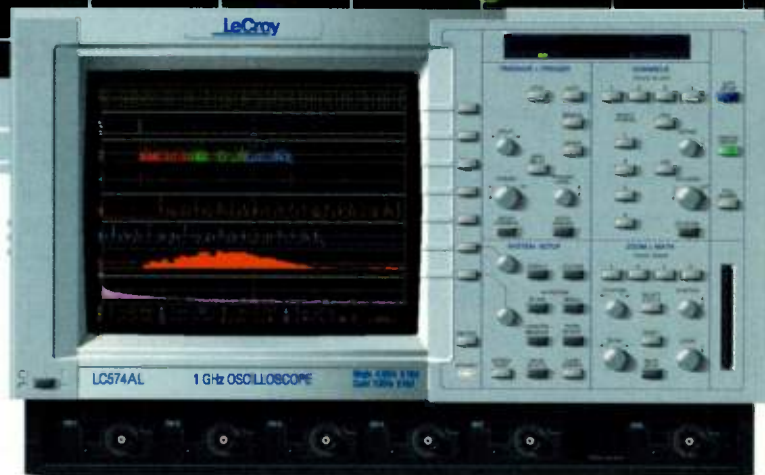
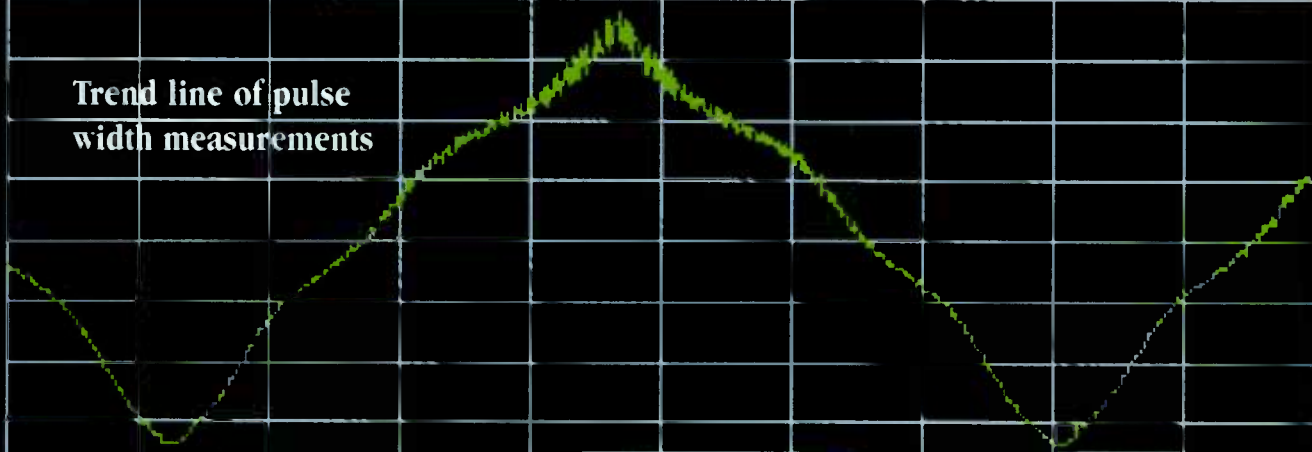
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MSB

BOB PEASE

Bob's Mailbox

Dear Bob:

What is "World Class" as discussed in the June 23 Bob's Mailbox that arrived today?

Consider Mensa. They recruit from the top 0.5% or so of the smart folks in the world. In the USA that's about a million, give or take a few hundred thousand. Way too many!

Consider pro athletes. Maybe 0.1% as many as those eligible for Mensa, in any particular league. Say a thousand or so. Still too many.

Consider the best of the best. Maybe 1% of any given pro league are recognized as "World Class." So, $0.005 \times 0.001 \times 0.01 = 0.0005\%$ would be a good upper limit.

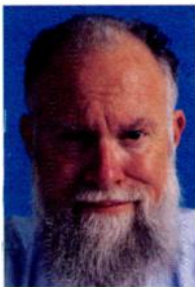
Therefore, 25 or 30,000 out of the world are candidates for the title "World Class," from which field you get the Olympic Medalists, Nobel Prize winners, self-made billionaires, and engineers who can build an amplifier with a usable seven-decade logarithmic response.

If your product stands out that far, it's World Class. Examples that spring readily to mind are the Model T Ford; the VW Beetle; the DC-3 (C47); the Piper Cub; the IBM electric typewriter; the Tektronix Scope; the H-P Audio Oscillator; the PDP-8; the 741 op amp; the Philbrick Op-Amp Book; the Howland circuit; the 6800 microprocessor; and the Swiss Army knife. Not to mention a whole lot of stuff from L&N, General Radio, and all those other people who meant "0.01% forever" when they said "0.01%" in their spec sheets.

And Jim Williams and Bob Pease, who know what they're talking about.

JIM TAYLOR
via e-mail

Jim: True, there aren't a lot of world class op-amp designers around. There aren't a lot of world-class voltage-regulator designers—or ballet dancers, or crane operators, or wide receivers, or sopranos, or left-handed pitchers. But when you add up ALL the classes of excellent, talented people, there sure are a lot of world-class people. OK?—RAP



Dear Bob:

I've written before to compliment you on your column; I still say it's great, but have another reason to write this time. You always seem to have a lot of practical advice; those cherished gems of wisdom learned from the school of experience. A fellow pro-

fessor and I were discussing the challenges students face in prototyping their circuit designs. They start with simple series and parallel circuits on the standard white protoboards.

Since such circuits always seem to work well there, they begin to assume that these nice protoboards are useful for all circuits. It's not until they reach RF classes that they learn some of their limitations. Then they learn about options such as vector boards, perf boards, wire wrapping, and soldering over a ground plane. It would be nice if there were some kind of practical guide to the prototyping options, their strengths and weaknesses, etc. With your experience and bent toward the practical, it strikes me that you might know of such a guide, be it an article in a periodical, a manual, a book, or whatever.

I hope you're not overwhelmed by e-mail, and that you'll have a minute to respond to this one.

BARRY LUNT

Assistant Professor
Electronic Engineering Technology
Brigham Young University
via e-mail

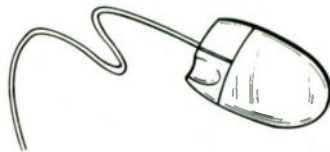
Well, yes, I am real busy, but you are right: Students are not learning about breadboarding skills. How can we encourage them? Technicians and engineers, too. Readers??—RAP.

All for now. / Comments invited!
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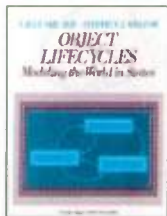
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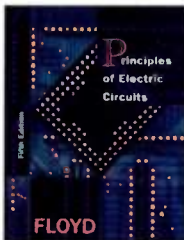


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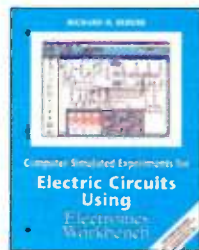


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HOWARD JOHNSON

The Real Truth About Crosstalk

Crosstalk is a fact of life in modern digital systems. We can't eliminate it, but it's our job to figure out how to control it, manage it, and to just plain live with it.

Consider the circuit shown in the figure below. In the terminology of crosstalk, the gate at position (A) is the aggressor, and the gate at position (D) is the victim. Whenever the aggressor changes state, we observe a pulse of crosstalk at the victim. If you're doing dense, high-speed designs, this is probably an all-too-familiar scenario.

One of the fascinating things about crosstalk is its *directionality*. Crosstalk waveforms are a function of the *direction* of current flow. For example, in the figure, by reversing the direction of current flow on the aggressive trace, the crosstalk received on the victim will reverse polarity.

Directionality is an important concept, so I'll go over it step-by-step. First, set up the circuit as shown in the figure. Measure the crosstalk at (D) when the gate at (A) switches from low to high. You'll see a negative blip of crosstalk at (D) coincident with the arrival at position (B) of the aggressor signal.

Next, reverse the direction of current flow on the aggressive signal. This means rearranging the circuit to place the aggressive driver on the right at position (B) and its triple load on the left at position (A). Repeat the crosstalk measurement, again observing at position (D). This time, you will see a *positive* blip of crosstalk (a reversal of polarity).

The polarity reversal tells us that we're not dealing with capacitive

crosstalk. Many digital engineers assume that crosstalk is primarily a capacitive effect. It isn't. Mutual capacitance between two single-ended circuits can only cause positive crosstalk.

The polarity reversal indicates that the interference is due (at least in part) to mutual inductive coupling. That's the same kind of coupling you get in a transformer. It is well-known that reversing the leads on the primary winding of a transformer will reverse the polarity of the voltage on the secondary. Coupled pc-board traces act in much the same way. If you think of each pc-board trace as a little loop of current, you can see how the "crosstalk" transformer works.

First, imagine current from the gate at position (A) flowing out through the aggressor trace to the load at (B). From there the current returns, along the power and ground system, to the gate at (A). The aggressive current makes a loop. Think of this loop as the primary winding of a transformer.

The secondary winding of that same transformer lies nearby. It is the loop formed starting with the gate at position (C), moving out along the victim trace to the load, and back along the power and ground system returning to the gate at (C).

These two loops behave in many ways almost exactly like a weakly-coupled, single-turn transformer.

The existence of transformer-type mutual inductive coupling between traces has profound implications for

digital designs. For one thing, it implies that crosstalk may vary depending on the applied load in our circuits.

For example, in the figure, *assuming we are working with a short pc-board trace*, the aggressor current will be a strong function of the total applied load. The heavier the load, the more aggressor current we will draw, and the more crosstalk we will generate. The triple-load network in the figure will generate nearly three times as much crosstalk as a similar net with a similar

topology having only one load.

This loading effect is particularly acute when driving banks of SIMM memory modules. Such traces tend to be very short, but heavily loaded, so that the drive currents are almost totally dominated by the load capacitance of the SIMM receivers. As we plug in more SIMM modules, crosstalk goes up.

So if you are trying to debug a crosstalk problem on a dense multilayer board, knowledge of how trace loading affects crosstalk can help you uncover, and fix, the problem.

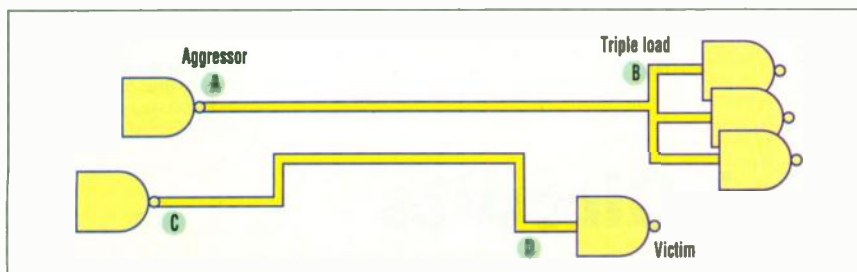
And if you are trying to manage crosstalk from first principles so it comes out right on the first spin, look into the new crosstalk prediction tools that feature IBIS I/O modeling. Most of these new tools are capable of calculating crosstalk, including the loading effects, in an automated, highly efficient manner.

Dr. Howard Johnson (howiej@sigcon.com) is president of Signal Consulting Inc., a high-technology consulting firm specializing in solving high-speed digital design problems. He is the author of "High-Speed Digital Design: A Handbook of Black Magic" (Prentice-Hall, 1993), and a frequent guest lecturer at both the University of Oxford and UC-Berkeley. For information about his ongoing series of on-site workshops for digital engineers, visit Signal Consulting's website at <http://www.sigcon.com>.

This concludes Dr. Johnson's 8-part series on digital design topics. We're glad he was able to steal enough clock cycles from his "high-speed" schedule to share his useful insights with *Electronic Design's* readers.—Ed.



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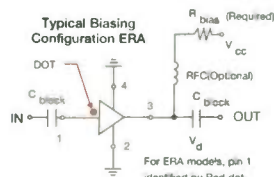
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Circle 520

Video Monitor Adapter Enhances Oscilloscope

WAYNE SWARD

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Video signals can be difficult to display on an oscilloscope. Normal trigger circuits in most oscilloscopes have trouble getting a stable trigger from the combined vertical and horizontal sync signals, color burst, and picture signal in a composite video waveform. Even the "TV Sync" trigger detector available in some low-cost oscilloscopes is inadequate to obtain a stable display.

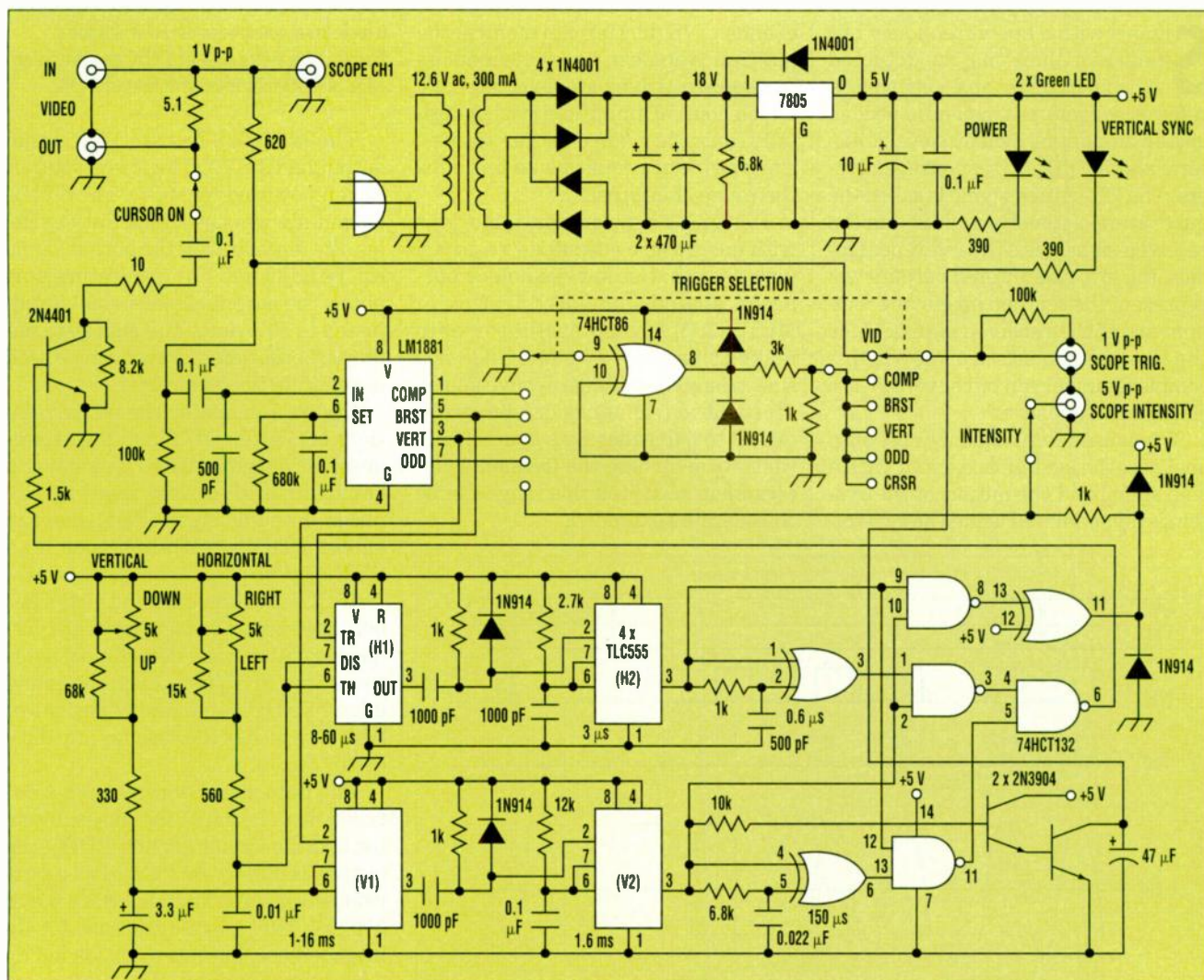
The circuit shown monitors a composite video signal and provides sta-

ble sync pulses for the external trigger of an oscilloscope (see the figure). The Trigger Selector switch chooses Video, Composite Sync, Color Burst Sync, Vertical Sync, Vertical Odd Field Sync, or Cursor Position for the oscilloscope. Two timer chains provide a rectangular cursor (width and height approximately 8% of the full screen). The cursor is movable across the full width and height of the screen by adjusting the Horizontal and Vertical Cursor Controls.

The circuit provides a positive Intensity pulse for the oscilloscope Intensity (Z-axis) input. This permits close inspection of any portion of the video signal corresponding to the position of the cursor. If the oscilloscope is hooked up to a color demodulator as a vectorscope, this feature highlights the demodulated color on the vectorscope display. This is useful in applying color correction or enhancement as part of a video-editing setup.

The circuit contains a Power LED and a Vertical Sync Indicator LED. The Cursor On switch allows the movable cursor to be observed on a video monitor attached to the Video Out connector. The Intensity switch controls the Intensity pulse to the oscilloscope.

The LM1881 Sync Detector separates the various sync signals from the composite video into stable logic pulses. Color burst sync, which occurs at the



This circuit can monitor a composite video signal, as well as provide stable sync pulses for the external trigger of an oscilloscope.

start of every horizontal line, is applied to a 555 CMOS timer. The timer output pulse width is adjusted by the Horizontal Cursor Control over the full width of the line. This output pulse drives a second 555 timer which establishes the cursor window width. The output of this second timer drives a 74HCT86 exclusive-OR gate through an RC circuit, providing a short positive pulse corresponding to the start and end of the horizontal cursor window.

Vertical sync, which occurs at the start of every vertical field, is similarly processed by a parallel set of timer circuits to establish the start and end of the vertical cursor window. The 74HCT132 NAND gates combine these signals into the desired square cursor. The resulting square cursor drives the 2N4401 transistor. When switched on, the transistor reduces the amplitude of the video signal at the Video Out connector through the volt-

age-divider action of the 5.1- Ω and 10- Ω resistors. This results in a gray cursor surrounding the area of interest on a video monitor. The 0.1- μ F capacitor protects the transistor from any dc voltage on the video.

The fixed resistors associated with the Horizontal and Vertical Cursor Controls provide the range of timing adjustments shown. Their values may be modified to account for tolerances of the other components.

Circle 521

Swept Sine Oscillator Has Quadrature Output

ODD ARILD OLSEN

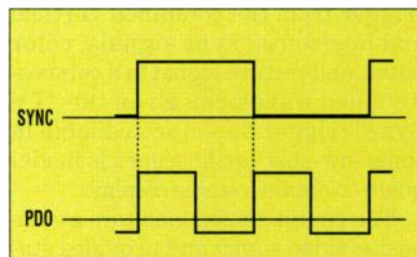
Prediktor AS, Postboks 296, N-0852, Oslo, Norway.

Signals with a known frequency but unknown phase may be detected using an in-phase and a 90° shifted reference signal, as frequently used in lock-in amplifiers, synchronous detectors, and frequency-response analyzers. The 90°-shifted signal is called the quadrature signal. By multiplying the received signal with the reference signals, the low-pass filtered outputs will represent the real and imaginary components of the received signal. Once the two components are known, this complex number can be converted into amplitude and phase.

When used for frequency response analysis, the system is excited with a sine signal and the output of the system is demodulated using the two ref-

erences. Neglecting harmonics, the multiplication can be performed using square-wave reference signals, which control amplifiers with a digitally controlled gain of either +1 or -1. The frequency must be swept over the range of interest.

Designing a swept-sine generator with quadrature output isn't a trivial task, though. For low-frequency purposes, an undocumented feature of Maxim's MAX038 oscillator chip makes this easy. The MAX038 is a sine, triangle, and square-wave generator whose frequency can be swept over 2 to 3 decades by a control current. By switching the frequency-determining capacitor, this range can be considerably extended.



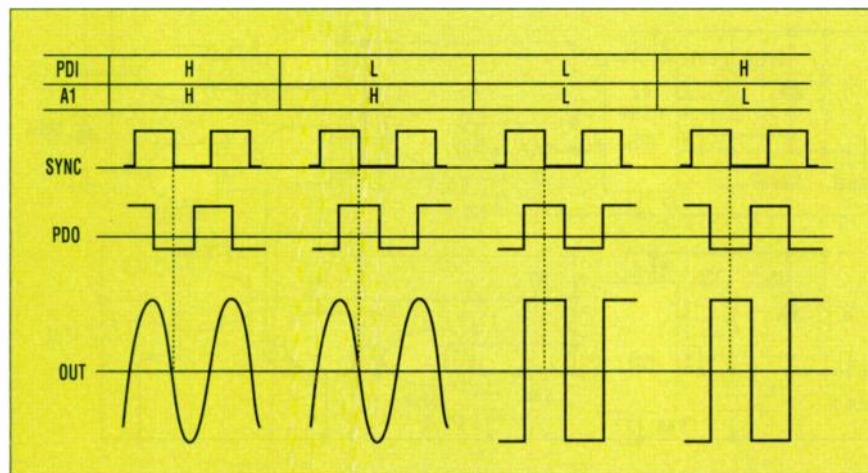
2. When PDI is connected to SYNC instead of a logic level, the phase detector output's frequency is twice that of SYNC and the rising edge of PDO coincides with that of SYNC.

The MAX038 has an OUT signal output and a SYNC logic level output (when powered by ± 5 V). The SYNC output always has a 50% duty cycle, but the duty cycle of the output signal can be adjusted. For quadrature purposes, the output signal should be adjusted to 50% duty. The chip also contains a phase detector that can be used to generate the quadrature.

Figure 1 indicates the phase relations of SYNC, OUT, and the phase detector output (PDO). By setting a constant high or low level at the phase-detector input (PDI), one can select PDO to either lag or lead SYNC by 90°.

If PDI is connected to the SYNC output instead of a logic level, the frequency of the phase detector output is twice that of SYNC. Also, the rising edge of PDO coincides with that of SYNC, which is the case for any duty cycle (Fig. 2).

The data sheet doesn't give a detailed description of the phase detector and the circuit driving PDO—the output is simply described as a current source switching between 0 and 500 μ A. This may be the case for its intended use, but not when loaded by a resistor to ground. When left open, the output alternates between about

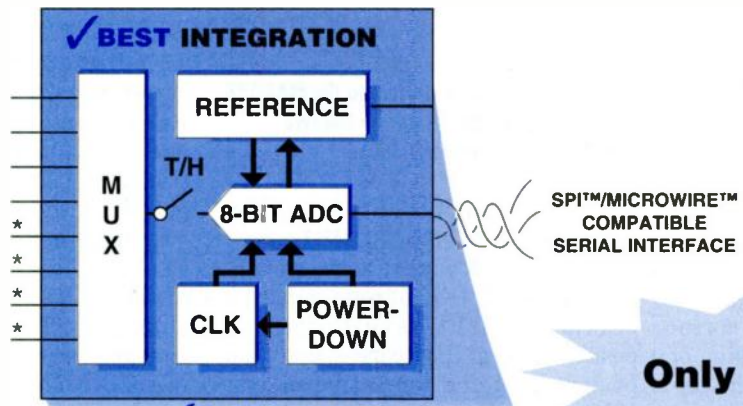


1. Given are the phase relations of SYNC, OUT, and the phase detector for the MAX030.

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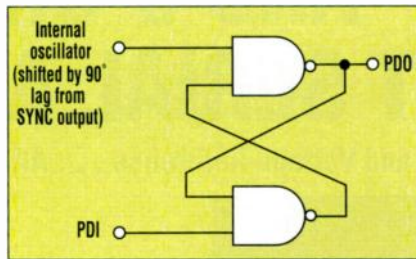
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-2.3 and +4 V. The negative voltage apparently is an internal level with a source resistance of 10 to 15 k Ω . When loaded by 5 k Ω , the output swings between about -0.7 and +3.2 V. Being uncertain about the effects of loading on internal chip operation, a high-impedance load (i.e., a CMOS gate input) is recommended.

Ed-The following supplemental information about the MAX038 was provided by Roger M. Kenyon, senior member of the Applications Dept. technical staff at Maxim:

Mr. Olsen's analysis of the relationships between the SYNC pin and the OUT pin is correct. In sinusoidal mode, the rising edge of SYNC corresponds to the rising zero-crossing of OUT. In square-wave mode, the rising edge of SYNC precedes the rising edge of OUT by 90°. Internally, the input signal received by the phase detector is a 90° lag phase-shifted SYNC signal (Fig. 3). Therefore, as demonstrated by Mr. Olsen, if the PDI



3. The phase detector internal to the MAX038 can basically be represented by the two NAND gates as configured here.

pin is held high in sinusoidal mode, then a positive edge at PDO corresponds to a valley at OUT and a negative edge at PDO corresponds to a peak at OUT. If PDI is held low, then a positive edge at PDO corresponds to a peak at OUT and a negative edge at PDO corresponds to a valley at OUT. Because of this internal phase shift, the SYNC and PDO outputs are ideally suited for developing quadrature signals for OUT.

A typical application for the inter-

nal phase detector involves PLL operation. The signal applied to PDI is compared to the internal SYNC signal. If the PDI signal has 50% duty cycle and is the exact frequency of the MAX038, the average output current of PDO is 250 μ A (the output current range for PDO is from 0 to 500 μ A). This current generates a voltage across a "gain" resistor (R_{PD}) and an RC compensation network. This voltage is applied to the FADJ pin controlling the frequency of the MAX038 output. If the signal applied to PDI varies in frequency, the duty cycle of the PDO output changes and the average voltage applied at FADJ changes. This change in voltage changes the output frequency of the MAX038 to match the frequency applied at PDI. The value of R_{PD} determines the range of the applied PDI signal so that the MAX038 remains "locked." The maximum value of R_{PD} is around 4.7 k Ω . Values above this will overdrive the FADJ input.

Circle 522

Full-Wave Signal Rectifier Uses Just One Transistor

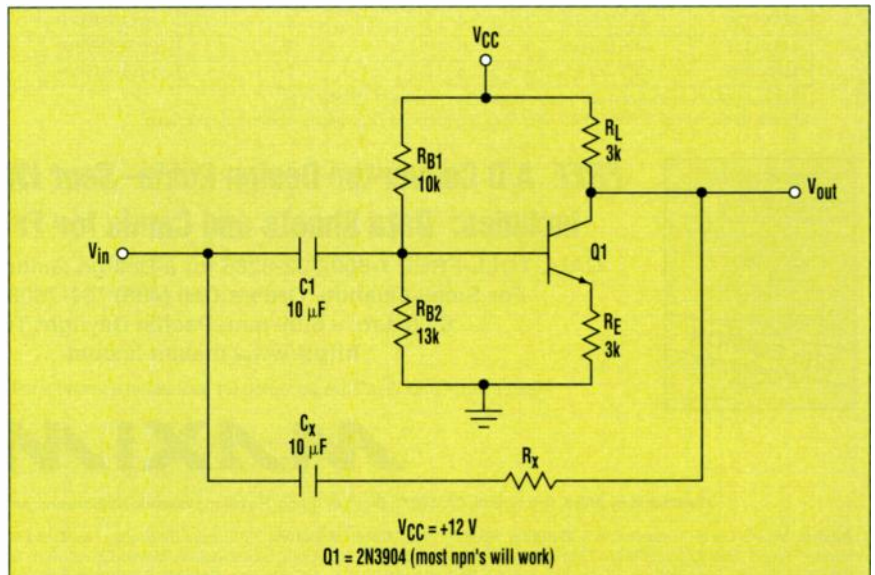
DAVID L. ALBEAN

Thomson Consumer Electronics, 101 W. 103rd St. 46290., MS INH 700, Indianapolis, IN 46201-2598; (317) 587-4950; fax (317) 587-6779.

The simple circuit shown accomplishes full-wave signal rectification with only one transistor (Fig. 1). This is done by exploiting the "gain reversal" phenomenon exhibited by a saturated bipolar transistor. This circuit will find applications as a signal-level detector (AGC detector), rectifier, or signal-presence detector.

To understand the operation of this circuit, first assume that the transistor is biased in saturation. The bias conditions are established by R_{B1} and R_{B2} . R_L and R_E are chosen for the desired gain/dc offset at the output. This circuit configuration is simply a saturated common-emitter (CE) amplifier.

For the following analysis, the component values given are used. Consider a sinusoidal input signal. For a negative-going V_{in} , V_{out} can swing positive. The gain experienced by the signal is



1. By taking advantage of a saturated bipolar transistor's "gain reversal" phenomenon, this circuit can perform full-wave signal rectification with using only one transistor.

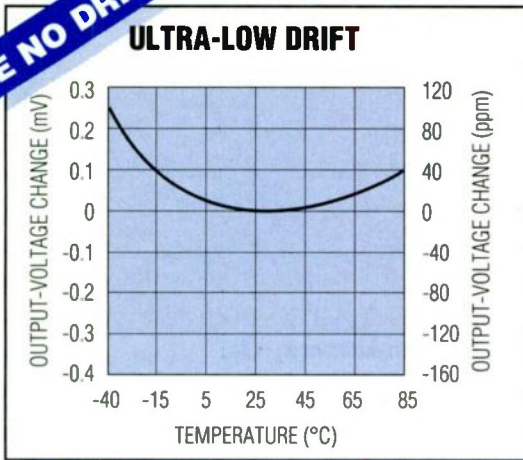
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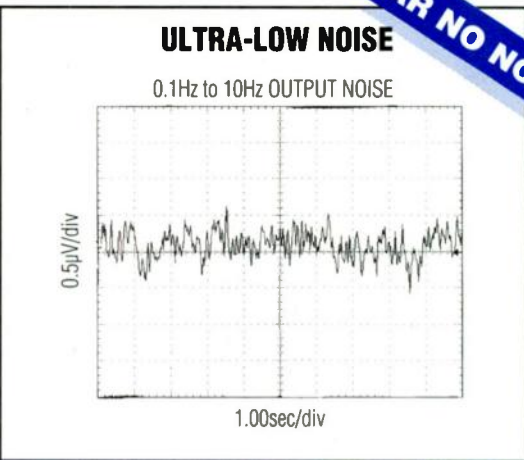
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MAX6325	2.5	1.0	\pm 0.04	2.8	Yes	6.70
MAX6341	4.096	1.0	\pm 0.025	4.0	Yes	6.70
MAX6350	5.0	1.0	\pm 0.02	5.0	Yes	6.70
MAX6225A/B	2.5	2.0/5.0	\pm 0.04/ \pm 0.1	2.8	Yes	4.65/2.25
MAX6241A/B	4.096	2.0/5.0	\pm 0.025/ \pm 0.1	4.0	Yes	4.65/2.25
MAX6250A/B	5.0	2.0/5.0	\pm 0.02/ \pm 0.1	5.0	Yes	4.65/2.25

* 10Hz \leq f \leq 1kHz **1000 pc. price, FOB USA.



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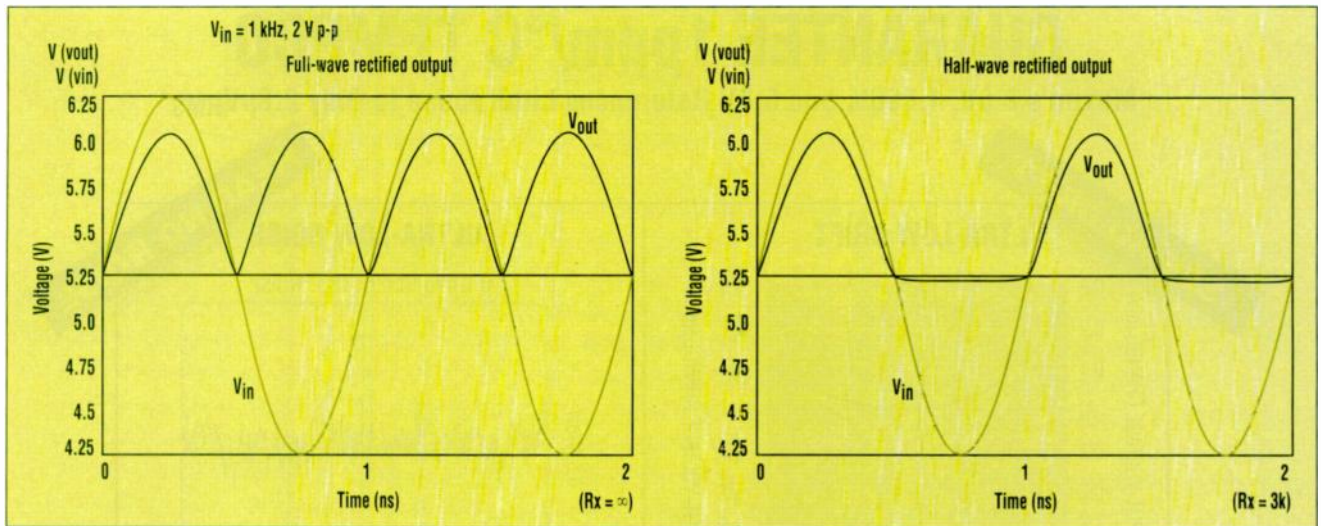
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Circle No. 134 - For U.S Response

Circle No. 135 For International



2. A full-wave rectifier is realized by setting $R_x = \infty$ (a). Half-wave rectification is predicted at $R_x = 3k$.

about: $-(R_L \parallel R_X)/R_E + (R_L/(R_L + R_X))$ (normal operation of a CE stage). However, for a positive-going input signal, the collector-base junction becomes forward-biased (the transistor is saturated) and the transistor operates as an emitter-follower. At this point, the collector is acting as the emitter usually does under forward bias. The gain expression then becomes: $1 + (R_L/(R_L + R_X))$. Full-wave rectifier action requires the gain for positive and negative signals be equal in magnitude, but opposite in sign. For a gain of 1, set R_X to infinity; this reduces the above equations to: $(R_L/R_E) = 1$.

An npn transistor is used to get a positive-rectified output. Using a pnp transistor (and reversing connections as appropriate) will produce a negative-rectified output. To choose element values, start with the following (for C_1, C_X coupling capacitors, use as large a value as necessary for the fre-

quency range of interest):

1. Ensure saturation: $V_{CC} - I_C(R_L + R_E) < V_{cesat}$
2. Choose I_C .
3. Choose R_L, R_E for desired gain.
4. Choose the R_{B1}, R_{B2} divider consistent with above.

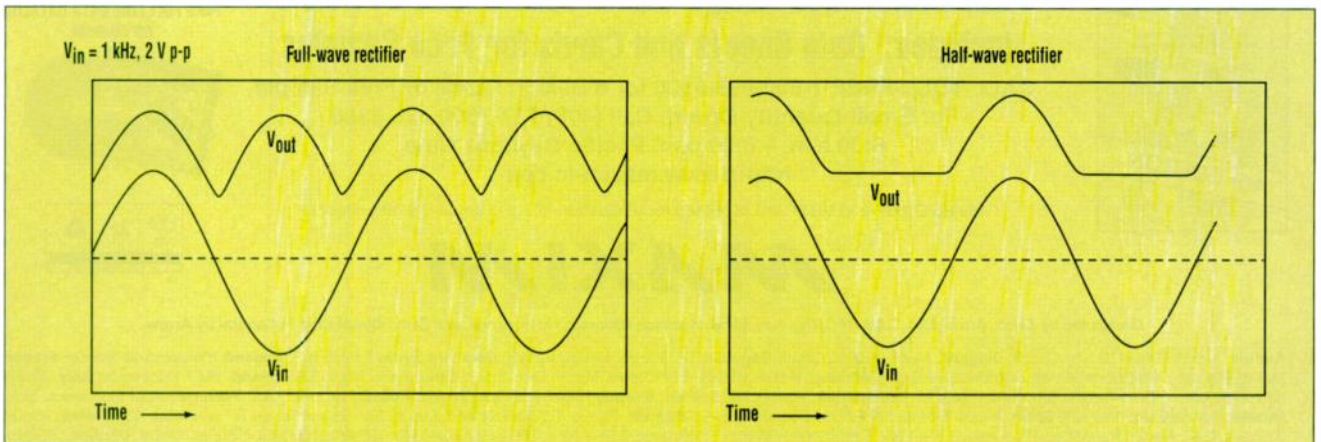
Design for a gain of 1 ($R_X = \text{infinity}$) and $I_C = 2 \text{ mA}$ yields: $R_{B1} = 10k; R_{B2} = 13k; R_L = R_E = 3k$. Gains between 1x and 2x can be achieved, but R_X must be included as indicated in the more complex design equations.

Start with these equations. Iterate with Spice to get optimal values (Fig. 2). This circuit is difficult to simulate accurately due to its inherent nonlinear operation. Thus, performing transient analyses in Spice will produce the best results (Fig. 3). It's important to have a good transistor model to accurately predict the circuit's behavior

in saturation. Also, including BR (reverse beta) in the Spice models is important because the circuit's operation relies on reverse operation of the transistor. Check this circuit at higher operating frequencies using Spice transient analyses as well.

A couple of notes to consider:

1. Gain is limited to a minimum of 1. Gain scaling and dc offset can be accomplished with a subsequent stage.
2. Use R_X as a "symmetry" trim. This will give the rectifier a gain closer to +1 for a positive input. A half-wave rectifier can be made by choosing values that result in $(R_L \parallel R_X)/R_E = (R_L)/(R_L + R_X)$. This equality will exactly cancel the positive and negative gains for negative-going half cycles, resulting in half-wave rectification (the transistor will act as an emitter follower only for positive inputs). For the example, $R_X = 3k$ will produce a half-wave rectifier.



3. Measured waveforms verify the full-wave (a) and half-wave (b) performance predicted by the Spice analysis.

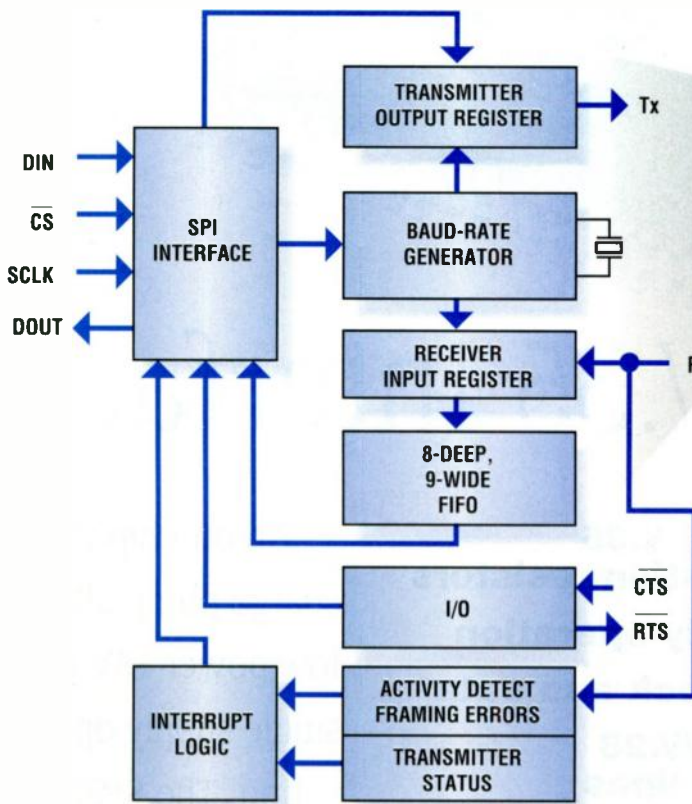
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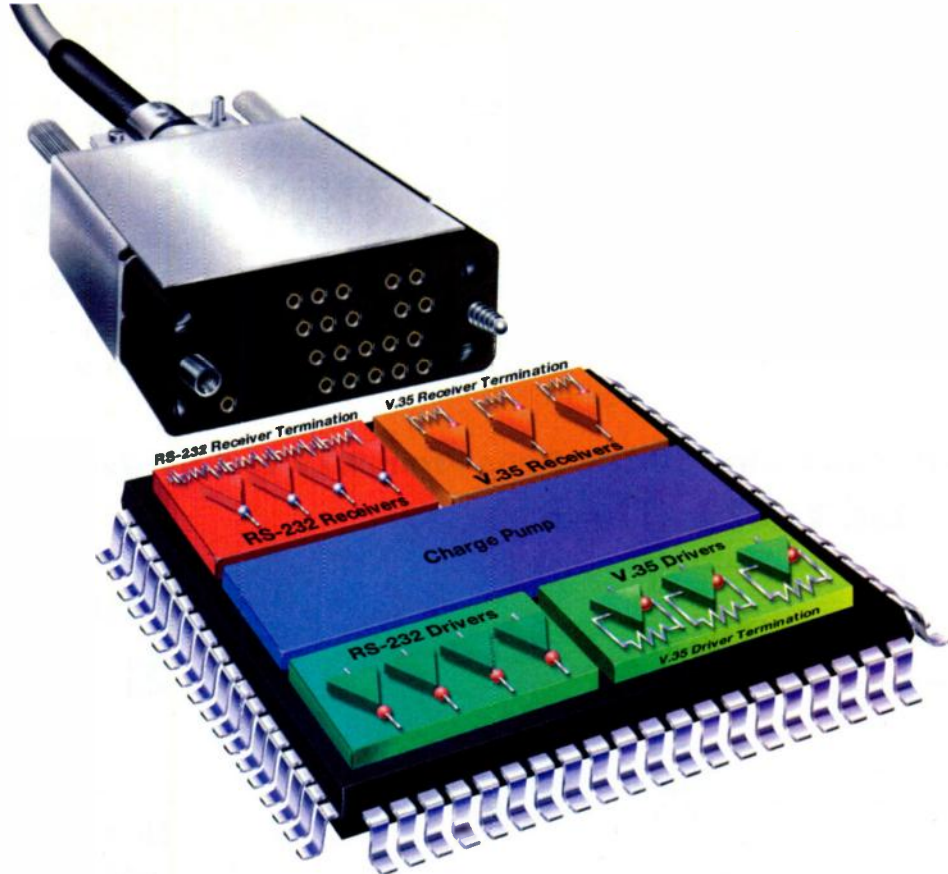
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Circle No. 137 For International



Simplified V.35 Interface

The SP320 is the world's only single chip V.35 transceiver. Featuring the highest level of integration, the SP320 includes all the line drivers and receivers necessary for a complete V.35 port without the need for external termination resistors.

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- **V.35 clock and data**
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- **NET1/NET2 certified**

An on-chip Sipex charge pump allows low power +5V only single supply operation. The SP320 is NET1/NET2 certified and is ready for your next V.35 port design. Call a Sipex applications engineer today to see how simple a V.35 port can be!



Versatile IQ Demodulator For Digital Signals

Targeted at DBS receivers and other digital communications systems, the UPC2781 demodulator has an operating frequency range from 440 to 520 MHz. The device integrates an AGC amplifier, a set of double-balanced mixers, oscillators, buffer amplifiers, and I/Q buffer amplifiers. It also features an on-chip 90° phase shifter and can achieve ±0.5 dB amplitude balance, with ±2° of phase balance, and 35 dBc of IM3 distortion. Available now in a 20-pin SSOP, the UPC2781 costs \$2.65 each in quantities of 10,000. LG

California Eastern Labs, P.O. Box 54964, 4590 Patrick Henry Dr., Santa Clara, CA., 95054-1817; (408) 988-3500. CIRCLE 560

DECT Hardware/Software Combo For Voice, Data, WPBX, And WLL

Designers can create a wide variety of cordless phone and data products for home, SOHO, and full-scale corporate users with the ABC family of integrated DECT baseband controllers and RF solutions. The entire ABC (ADPCM Baseband Controller) family of processors fully complies with the GAP standard for DECT signal and call processing. A full suite of development tools, protocols, and user-interface software also is available, as well as several complete RF interface designs.

For baseband processing, the PDC5091 provides a single-chip foundation for any DECT handset application. In addition to the mandatory GAP features, it supports hands-free operation. For single-cell base stations in homes and small offices, the PDC5092 interfaces to analog phone lines and offers full GAP functionality, as well as on-chip support for an external answering machine function. Chips that support digital and multiple phone lines are available. There's also software to support repeater and relay applications with multiple cells.

Low-cost wireless data applications can be quickly developed for the chips using a data-transmission protocol package. The OM5878 implements a proprietary communications protocol over a DECT air interface. It provides a transparent V.24 connection at 9600 bits/s. On-chip encryption of all wireless

data traffic ensures maximum security. Applications include laptop/PC links, point-of-sale terminals, credit-card verification, and remote data logging.

RF solutions for handsets and base stations include an integrated double conversion, a superheterodyne transceiver, a design implemented in discrete components, and a series of pre-manufactured RF modules.

Pricing and delivery information available on request. LG

Philips Semiconductors, P.O. Box 218, 5600 MD, Eindhoven, The Netherlands; (+31) 40-272-20-91; fax (+31) 40-272-48-25; www.semiconductors.philips.com. CIRCLE 561

On-Chip RF Macrocells Speed Semi-Custom Wireless Designs

Designers can enjoy most of the benefits of full-custom RF IC designs at a fraction of the time and expense. VersaTILE RF ICs are silicon substrates containing arrays of uncommitted bipolar and/or biCMOS circuit macros that can be configured using the chip's upper two metal layers. Intended for a diverse range of applications, including cellular, PCS, wireless LANs, two-way pagers, and satellite communications, the first samples of a VersaTILE design can be delivered in 12-16 weeks, much shorter than a full-custom design. If high production volumes are required, the VersaTILE design can be easily translated to a full-custom chip that is fabricated using the same 0.6-µm process.

Depending on the chip selected, a wide variety of macros are available. These include RF building blocks and critical support circuits, such as bias networks. For example, a bipolar analog circuit macro contains silicon nitride capacitors, polysilicon resistors, bias networks, and transistor arrays.

A typical biCMOS VersaTILE frame can contain several complex analog macros, plus a pair of biCMOS phase-locked loops and bipolar prescalers. A charge pump and analog switch and prescaler interface can be included as well. Targeted at low-voltage subscriber and mobile equipment market, most VersaTILE ICs can run on supplies from 2.7 to 5.5 V. The ever-growing library of macro functions includes RF amplifiers, up and down converters, modulators and demodulators, discriminators, PLLs and

charge pumps, prescalers, dividers, multipliers, and analog switches. LG

Fujitsu Microelectronics Inc., 3545 N. First St., San Jose, CA 95134; (800) 866-8608 or (408) 922-9000; fax (408) 922-9179. CIRCLE 562

Three-Chip AMPS/TACS Phone Cuts Cost, Stretches Talk Time

Integrating both RF, IF, baseband, and user-interface sections into a three-chip set, the AMPS/TACS-XL provides a low-cost, high-performance platform for cellular phones. Only an off-the-shelf IF downconverter, LNA, power amplifier, and a few passive components are required to implement a complete AMPS/TACS phone. All control and signal processing is performed within the chip set, eliminating the need for an external microcontroller. Due to its high level of integration, the AMPS/TACS-XL makes it possible to produce a complete cellular handset with a BOM of under \$65.

The AMPS/TACS-XL includes the CQT1010 processor chip, which handles audio and baseband processing, plus control functions. It's CASP architecture uses an array of specialized processors connected by a high-speed on-chip bus to perform voice and IF processing. Besides reducing space requirements and component costs, the phone only runs the processors needed to perform a particular operation at any given time. This results in substantial power savings in both operating and standby modes.

The phone's CQT1020 audio/RF processor employs a sigma-delta converter, which eliminates the need for a second IF strip, ceramic filters, and additional external components. The CQT1030 transmitter integrates a VHF VCO, a frequency synthesis circuit, an upconverting mixer, and amplifier driver circuit.

Type-approved AMPS call processing software and a full development environment allow for rapid product development and addition of custom features. Housed in compact TQFPs and SSOPs, the AMPS/TACS-XL is available now. Pricing is \$15 in production quantities. LG

ComQuest Technologies Inc., 527 Encinitas Blvd., Encinitas, CA 92024-3740; Alex Katouzian, (619) 633-1618; fax (619) 633-1677, www.comquest.com. CIRCLE 563

Low-Power, Dual Band Receiver For TDMA and GSM Handsets

The TQ9222 is a dual-band receiver, capable of operating in both the 800-MHz cellular and 1900-MHz PCS bands. This low-power part runs off a single 2.7- to 5.0-V supply and is designed specifically to meet the requirements of both the GSM and IS-136 TDMA standards. It integrates two separate LNA/mixer circuits to maximize the LNA's dynamic range while maintaining high overall performance. This dual-mixer architecture allows it to cover a wide high-side LO frequency range, with IF frequencies ranging from 70 to 140 MHz.

RF performance in both bands yields a conversion gain of 20 dB, a noise figure of 2.8 dB, and an input third-order intercept point of -10 dBm. To simplify both the design and manufacture, most ports on the chip are internally matched to 50 Ω . When operating in the cellular band, the TQ9222 consumes just 10 mA of 3.0 V power, and 20 mA in PCS mode. A detailed data sheet, evaluation board, and applications support will be available for the device. Sampling during the third quarter of this year, the TQ9222 is housed in a 24-pin QSOP package. Pricing is anticipated to be \$5.00 each in 100,000-piece quantities. LG

TriQuint Semiconductor, 2300 NE Brookwood Pkwy., Hillsboro, OR 97124; (503) 615-9000, fax (503) 615-8900, www.triquint.com. CIRCLE 564

Subminiature SAW Filters For GSM And PCS Applications

Designed for use in wireless systems with higher IFs, the SF246ZA-005 meets all of the requirements of the GSM air interface standard while operating in the 240-MHz band. With a center frequency of 246 MHz, the filter has a passband of ± 80 kHz. Its minimum rejection figure at ± 400 kHz is 25 dB, and 45 dB at ± 800 MHz, with a typical insertion loss of less than 6 dB.

Available from stock, the SF246ZA-005 is housed in a subminiature "Z" surface-mount package. Pricing is \$5 each, in 1000-piece quantities, with substantial discounts for production volumes. LG

Toko America, 1250 Freehanville Dr., Mount Prospect, IL 60056; (847) 297-0070, fax (847) 699-1194, info@tokoam.com, www.tokoam.com.

CIRCLE 565

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New Circuit Design Tools

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The missing link for CAE software.

Featuring configurable schematics with access to all IsSpice simulation properties; gone are the days of copying schematics to make new test setups or to run different kinds of simulations. Now, use your schematic as a design

notebook, document key circuit configurations and component test data with the same drawing used to define your production design. Go even further and design production acceptance tests and fault isolation procedures. Here's the new product line up.

◆ Design Validator

Design Validator sets a new standard for project continuity and design verification. Use the IsSpice4 analog and mixed mode simulator to automatically test and record circuit behavior. You can easily set limits and alarms that monitor design progress.

◆ Test Designer

The ATE specialist's standard produces acceptance test designs and fault diagnostics. Includes interactive and automatic methods for test sequencing and test synthesis.

The screenshot displays the Magnetics Designer software interface. On the left, a 'Model Properties' window shows parameters for a Laplace model. In the center, a circuit schematic is shown with components like a transformer (T1), a diode (D1), and resistors (R1, R10, R11). On the right, a 'Configurations' window shows a list of configurations and isolated layers.

Parameter	Ref Des	U1	>>Value
Part number	U1	LAPLACE	
Model	U1	LAPLACE1	
Type	U1		
Code Model	U1	s_idr	
Unknown type	U1	NODES	
Node 1	U1	9	
Node 2	U1	15	
Code Model	U1	Parameter	
in_offset	U1	0	
gain	U1	3.1415	
num_coeff	U1	1	
den_coeff	U1	2.31	
out_ic	U1		
divisions	U1	1	

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READER SERVICE 196

intusoft

Low-Cost Power Amp Handles 1900-MHz CDMA

Intended for PCS 1900 applications, the AWT1903 has a high level of linearity to minimize spectral regrowth and meet the other demands of CDMA operation. The three-stage, single chip, class AB amplifier typically exhibits a 26 dB gain, -12-dB return loss, 33% efficiency, and output power of 28 dBm, with an ACPR of 33 dBc at a 1.25-MHz offset. Its integrated bias-control circuit makes it easy to implement temperature compensation and power-conservation functions.

Packaged in a thermally enhanced 28-pin SSOP, the AWT1903 is available now. It is priced at \$8 each in lots of 100,000. LG

Anadigics Inc., 35 Technology Dr., Warren, NJ 07059; (908) 668-5000; fax (908) 668-5132, www.anadigics.com.
CIRCLE 566

Versatile DECT-Based Chip Set For PCS, WLL, And Other Apps

Suitable for both PCS and wireless local loop applications, the world's first chip set to support the new PWT1900 PCS standard also can provide line-quality voice service in wireless PBX systems. In addition, the highly integrated solution can be used to adapt European DECT platforms from their GFSK modulation scheme to the $\pi/4$ DQPSK modulation required by the U.S. PWT1900 specification.

The set consists of four analog/mixed-signal chips: the MAX2411 RF transceiver, MAX2511 IF transceiver, MAX1007 power control/RSSI, and the MAX1005 IF undersampler. Together, they perform all radio functions for wireless handsets, except power amplification.

The two-oscillator system employs a shared-IF SAW filter for both transmit and receive functions, which reduces parts count without sacrificing performance. Radios using this set of components can be programmed to receive PCS signals at any portion of the spectrum from 1850 MHz to 1990 MHz. Available now, the four-chip set is priced at \$15 in quantities of 100,000 or more. LG

Maxim Integrated Products Inc., 120 San Gabriel Drive, Sunnyvale, CA 94086; Hans Dropmann, (408) 737-7600; fax (408) 737-7194. CIRCLE 567

DMM Test Leads Designed to IEC1010 Standards

Designed for comfort yet ruggedly durable, Pomona's latest test leads feature silicon insulated wire for enhanced voltage protection and longer service life. Precision manufacturing and the best materials assure accurate contact. Available in Pomona's Test Companion™ Kits, and test probe and lead sets.

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Programmable Downconverter Supports Cellular Standards

The HSP50214PDC is a software-driven digital downconverter that lets the user define and pack multiple demodulation schemes into a single cellular radio. It converts digitized IF data into information that can be processed by a standard DSP. Intended for multimode receivers in base stations, test sets, and other applications, the downconverter has an interface port that allows a host controller of a microprocessor to program any or all of its 12 software controlled functions. These include downconversion, tuning, decimation filtering, digital gain control, resampling, FM discrimination, Cartesian-to-polar conversion, and AGC.

Each of the downconverter's 12 sections may be programmed or disabled depending on the air interface to be received. This allows it to be programmed to process a various cellular and PCS signals, including AMPS, GSM, PCS 1900, IS-54 (TDMA), IS-95 (CDMA), and IS-136 (enhanced TDMA).

On-chip processing sections include an input level detector, several NCOs, CIC and halfband decimating filters, and a 255-tap programmable FIR filter. The HSP50214PDC maintains a 14-bit dynamic range throughout its internal processing to ensure the highest possible signal quality.

An evaluation board and a full suite of Windows-based development-support software is available for the HSP50214PDC. The evaluation board plugs into any ISA-bus-compatible computer. It contains the analog-to-digital and digital-to-analog converters plus a TMS3320C50 DSP chip, allowing it to perform demodulation of FM, FSK, BPSK, and QPSK signals. Loopback and diagnostic functions also are included. Driver circuitry permits direct connection for driving standard multimedia speakers.

Sampling now, the HSP50214PDC will be in full production by September of this year. Packaged in a 120-lead quad flat pack, the downconverter is priced at \$14.95 each in 10,000-piece quantities. LG

Harris Semiconductor, P.O. Box 883, Melbourne, FL 32902-0883; (800) 4-HARRIS, ext. 7728. **CIRCLE 568**

1998 DAC DESIGN METHODS CALL FOR PAPERS

DAC is the premier conference devoted solely to the field of Design Automation. All aspects of the use of computers as aids to the design process are welcome, from conceptual design to manufacturing.

The Design Methods track focuses on innovative methodologies for the design of electronic circuits and systems, as well as creative experiences with design automation in state-of-the-art designs.

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M1 Design methodologies and case studies for specific design tasks

- M1.1 Design entry and specification
- M1.2 Simulation, analysis, modeling and estimation
- M1.3 Verification, test and debugging
- M1.4 Physical design, module generation, design for manufacturing
- M1.5 Logic and high-level synthesis
- M1.6 System-level design, embedded-system design and co-design
- M1.7 Other

M2 Design flows and case studies for specific application domains and platforms

- M2.1 Board and MCM
- M2.2 FPGA, rapid prototyping and reconfigurable computing
- M2.3 ASIC
- M2.4 Microprocessor, multiprocessor and networking
- M2.5 Multimedia and consumer
- M2.6 DSP, communications and wireless
- M2.7 Other (automotive, medical, optical, ...)

M3 Design technologies and technology drivers

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- M3.2 High-performance design: timing, clocking and power distribution
- M3.3 Low power design
- M3.4 Mixed-signal, analog, and RF
- M3.5 New devices, sensors, MEMS
- M3.6 Other

M4 Integration and management of DA systems

- M4.1 Management of DA systems, design interfaces
- M4.2 Standardization issues
- M4.3 Distributed, networked, and collaborative design
- M4.4 Intellectual property, design reuse and design libraries

Other topics of interest to DA researchers, developers, managers and users are encouraged. For questions regarding the suitability of your topic, or for assistance with the preparation of your proposal, contact DAC at the address below.

SUBMISSION TO DAC: A submission to DAC can be a regular paper or a proposal for a panel, tutorial or a special session (a group of related papers or tutorials). You should contact all of the participants mentioned in your proposal for your panel, tutorial, or special session before submission.

DEADLINE: Submissions should be postmarked no later than **October 10, 1997**. All submissions will be reviewed. Notice of acceptance will be mailed by **February 23, 1998**.

For more information and specific requirements for submission please contact: **Design Automation Conference®**
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Tester Upgrades Allow Evaluation Of PCM Modems

A set of upgrades and options for the Series II telephone network emulator allow the test system to support development, manufacturing test, and evaluations of PCM modems, which use a new modulation scheme to achieve transmission rates faster than those of previous analog telephone connections. To test these modems, the telephone network emulator must provide analog access on the side of the modem that faces the consumer modem and digital access on the side that faces the Internet service provider. The company's solutions include a modification to the Series II that disables analog-to-digital and digital-to-analog conversion. This allows the instrument to be used with an external channel bank to facilitate testing of PCM modems. Also, a new module for the Series II provides full emulation of channel bank functions, including analog-to-digital and digital-to-analog conversion, signalling, and impairments. Finally, a new automatic modem test system that incorporates the Series II enhancements will be available. Call for price and availability information. JN

Telecom Analysis Systems Inc., 34 Industrial Way East, Eatontown, NJ 07724; (908) 544-8700; fax (908) 544-8347;

76546.2353@compuserve.com

CIRCLE 569

Lab Supply Features Two Well-Regulated Outputs

The Model 83B829 linear power supply provides two isolated dual-range dc outputs. Each can be set to either 0-40 V dc at 0.3 A or 0-20 V dc at 0.6 A. Both are full-range adjustable by 10-turn potentiometers on the front panel. Each output has a 3-1/2-digit meter that shows either voltage or current, as selected by the operator. Load regulation drops to less than 0.01% +3 mV for a change in output from full load to no load. Line regulation drops to less than 0.01% +2 mV for any line-voltage change within the unit's operating ranges of 105-125 V ac or 210-250 V ac. The supply's ripple and noise is less than 200 μ V rms, and stability is better than 0.10% +5 mV total drift for 8 hrs., after a 30-min. warmup. Output terminals include five six-way posts, two for each section and a



common ground, on the front panel, and a two-section terminal strip at the rear. The Model 83B829 costs \$1050. Delivery is in one to two weeks. JN

Technology Dynamics Inc., Mid-Eastern Industries Div., 100 School St., Bergenfield, NJ 07621; (201) 385-0500; fax (201) 385-0702. CIRCLE 570

Power Analyzer Includes Spread-Spectrum Capability

The Model 4500 digital sampling power analyzer has a carrier frequency range of 1 to 40 MHz for pulse, CW, and spread-spectrum signals. Its accuracy, speed, and resolution suit it well for testing in CDMA, GSM, digital television, and radar applications. The instrument measures peak and average power by continuously sampling the signal at up to 500,000 samples/s and accurately converting each sample. A built-in precision calibrator further ensures accuracy. A variety of sensors cover a peak power range of -40 to +20 dB and an average range from -50 to +20 dBm. Spread-spectrum capability allows the Model 4500 to provide events-versus-level statistical analysis, so the unit can display CDMA signals. The analyzer can perform a number of automatic measurements in both the statistics and pulse modes. The Model 4500 costs \$15,000, with delivery in four to six weeks. JN

Boonton Electronics Corp., 25 Eastmans Rd., Parsippany, NJ 07054-0465; (201) 386-9696; fax (201) 386-9191; boonton@boonton.com. CIRCLE 571

CompactPCI Bus Analyzer Fits On 3U Card

The PBTC-315 is a 3U single-slot card that contains a complete logic analyzer for the PCI bus in 3U and 6U CompactPCI systems. The analyzer can monitor and trigger on PCI bus activity in 32- and 64-bit systems. The card has its own processor and RS-232 ser-

ial port, with all needed firmware resident in flash PROMs. Consequently, it's non-intrusive and offers stand-alone operation relative to the host computer being analyzed. Users can operate the card from a PC running the company's graphical user interface, BusView for Windows, or Windows NT; or from a standard ASCII terminal like VT100 or a terminal emulator. A sampling rate of up to 33 MHz is available across 91 PCI signals, plus up to eight user-defined signals taken through the front panel. Standard trace memory is 64 ksamples; a 256-k-sample trace is optional. Other features include four full-width trigger words, a 16-level trigger sequencer, and real-time statistical analysis. The PBTC-315 starts at \$8495 and is available immediately. JN

VMETRO Inc., 1880 Dairy Ashford, #535, Houston, TX 77077; (281) 584-0728; fax (281) 584-9034. CIRCLE 572

Emulator Handles AMD Am186ED To 40 MHz

The Q.E.D. in-circuit emulators now support Advanced Micro Devices' Am186ED. The emulator accommodates all of the microcontroller's key features, including the internal DRAM controller, both TQFP and PQFP packages, and clock rates to 40 MHz at 5 V. The Q.E.D. tracks the relocation of the processor's execution memory from chip-select defined space directly to DRAM space, thus allowing complete breakpoint and execution trace functionality. Fully qualified trace memory is 64k bus cycles deep with address, data, status, timestamp/interval timing, and 16 logic-state input channels. A complex hardware breakpoint system features an independent state machine using the address, data, status, event counter, and logic-state inputs collected for each bus cycle. Overlay memory of 1 Mbyte is standard, and the system comes with Paradigm PowerPack, which has a customized version of the Paradigm Debug software. Call for price and availability information. JN

Beacon Development Tools, 3307 Northland Dr., Suite 270, Austin, TX 78731; (800) 769-9143 or (512) 454-6211; fax (512) 467-8960; e-mail: info@beacontools.com.

CIRCLE 573

ANALOG

Inverter Brightens CCFL Screens With Less Power

The LXM1653 inverter module uses a patented current-synchronous zero-voltage-switching (CS-ZVS) technology by Linfinity Microelectronics to yield brighter screens in cold-cathode fluorescent lamp displays. With the CS-ZVS technique, more efficient dimmable CCFL inverter circuits can be designed. Also, improved magnetics reduce inverter size and power requirements.

The narrow, 7.4-mm-high module converts unregulated dc voltage from a battery or ac wall adapter to the high-voltage, high-frequency sine wave required to ignite and operate a CCFL. It regulates the line voltage and lamp current and permits lamp dimming with the use of a single synchronous power stage comprised of a pair of complementary low-loss power MOSFETs. Dimming is controlled by an external potentiometer or PWM signal. Full-bridge operation provides peak efficiency operating with lamps needing less than 5 W of power at in-

put voltages between 6.5 and 18 V. The inverter supports both monochrome and color displays with a single lamp.

To prevent leakage currents from circulating between the display panel, system ground, and inverter ground, the LXM1653 uses a floating-output drive in which the high-voltage side of the inverter transformer isn't referenced to ground. Greater inverter efficiency results in a wider dimming range, increased brightness, and more uniform illumination. The floating output drive also senses the secondary-side lamp current for accurate lamp-current regulation. Other features include open-circuit and short-circuit protection, and a 10- μ A sleep current.

The LXM1653 is intended for driving LCD backlight lamps in portable computers, LCD-based monitors, PDAs, portable instruments, automotive displays, and entertainment centers. Pricing is \$26.00 each in quantities of 1000. ML

Linfinity Microelectronics, 11861 Western Ave., Garden Grove, CA 92841; (714) 898-8121 or 800-877-6458. CIRCLE 574

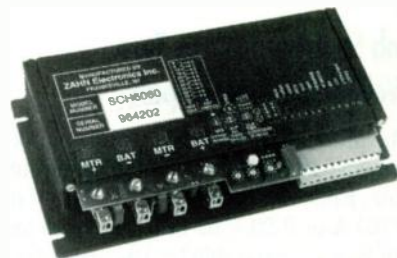
Triac Driver Coupler Blocks 600 V

The IL440 triac driver optocoupler consists of a GaAs infrared emitter optically coupled to a detector made of a small triac chip and a non-zero crossing network. When optically excited, the triac's output triggers the gate of a larger external triac for switching on ac power. The output detector can block up to 600 V for controlling off-line voltages up to 240 V ac. The device is used for protective separation against electrical shock within the maximum safety ratings. Typical applications include motor control, high-current triac drivers, solid-state relays, and small-switch ac loads. The emitter and detector are housed in a standard 6-pin plastic DIP. Pricing in quantities of 10,000 is \$0.54 each. ML

Siemens Components Inc., 19000 Homestead Rd., Cupertino, CA 95014; (408) 257-7910. CIRCLE 575

Surface-Mount Technology Shrinks Servo Amplifier

Initially designed for use in electric vehicles, the SCH5560 dc servo amplifier has been reduced in size by applying surface-mount technology and acid-etched bus bars. The module contains 28 power MOSFETs connected in parallel that switch at a crystal-controlled



frequency of 31.25 kHz to chop the heavily filtered dc bus and drive a dc motor. Current feedback is via Hall sensors. The SCH5560 is rated at 120 A peak and 60 A continuous with a 18- to 44-V bus. Input control signals are isolated from the power output. It costs \$660 from stock for small quantities, and 6 to 8 weeks for orders of 25 or more. Other higher-voltage versions range in price up to \$1020. ML

Zahn Electronics Inc., 4133 Courtney St., #5, Franksville, WI 53126; (414) 835-9200. CIRCLE 576

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We'd Like To Take A Bow

Frank Goodenough's April 14 cover story ("*Dense MOSFET Enables Portable Power Control*," p. 45) is one of the best articles we've ever seen about power MOSFETs in any engineering publication.

It is rare to encounter someone outside the business itself who understands so well the significance of these devices—which is growing more from year to year—for portable electronic systems.

Frank is the type of person who does make the effort to understand and who succeeds in drawing out of us, and communicating to the nonspecialist readership, the significance of what we're accomplishing with our technology and know-how. And he seems to get better at doing this with each passing year.

The service he and *Electronic Design* perform for the design community is thus invaluable, whether the subject is Temic MOSFETs or the products of a competitor. Our industry relies on articles like those to help digitally-oriented designers (which constitute the majority) better understand the importance of analog and power functions in their systems. We believe, and our customers have confirmed, that these in-depth articles are important to your readers. They also are important to us, since a magazine with such broad experience and impact as *Electronic Design* ensures that they are read by engineers in emerging fields that even we do not know about. Without this kind of coverage, our jobs would be much more difficult.

We are indebted to Frank and to *Electronic Design* as a whole for its success in approaching this task and for contributing to the overall knowledge of the electronics industry.

Linda Cosner
Director, Marketing Communications
Temic Semiconductors
Santa Clara, Calif.

Generally Speaking

Your April 14th editorial ("*Embedded Systems Change The Equation*," p. 18) may be old news to you, but I've only just received it.

It is interesting how you work through the need for multiple disci-

plines to arrive at the conclusion that the average engineer must know beyond his or her area of responsibility.

New Zealand's electronics industry is principally small-scale stuff, with few manufacturers turning out 10,000 pieces of anything. Naturally, we tend to have many more companies that don't have Cadence design tools or departments with hundreds of ASICs specialists. Around here, we're constantly finding ways to do things that other people throw money at.

One of our local distributors has been waging a campaign over the past few months that doesn't fit that picture. The Avnet Group has launched an applications engineering service, and I have a hard time seeing how it can add value to their silicon sales on the small scale we have here. In more than 10 years in the industry here, I have yet to meet a representative from any distributor that could tell me anything technically interesting beyond being able to hand over technical data for my perusal. Yet Avnet has launched this campaign to tell R&D people that we're not specialized enough, and that this is hurting us internationally.

Maybe I'm misguided, or I'm too stuck in my ways, but give me a clever generalist, and I'll soon have him or her picking up new tools. But give me a clever specialist, and who's to say how much general background this person has or can reasonably be able to pick up? I know which one I would choose for my projects.

Arnim Littek
Digi-Tech Ltd.
Wellington, New Zealand

A Little Of That Human Touch

I agree with nearly all of your May 27 editorial ("*An Unfolding Orwellian Prophecy*," p.18), but I have one point to make. You said that all that is missing are some technical hurdles in packaging and testing before this can become a reality. I think it may be a bit more complicated than that.

The problem stems from the code that "recognizes" the threat or other situation and decides on the response. Remember that you are suggesting that the vehicle take action regardless of driver inputs. The folks at Airbus

learned a hard lesson when a demonstration flight at a major airshow of the new aircraft with "fly-by-wire" controls turned into a crash in front of thousands of people.

Why? The pilot wanted to make a low approach followed by climbout. For some reason, the aircraft "wanted" to land and simply would not respond to the pilot's throttle inputs to select take-off power. The designers thought they could produce a system that was smarter than the pilot. Tough assignment at best, maybe impossible. There are just too many things that can happen, too many sets of possibilities that can confuse the computer.

I, like you, would LOVE to see advances in automotive controls to make up for the appalling lack of skill and/or attention exhibited by many drivers. What about those drivers that ARE paying attention? I can think of situations, depending upon traffic and road conditions, when the right course of action would be to swerve to miss the car in front, instead of braking. You might even need hard application of throttle or a modulated application of brakes. There is simply no way that a microcontroller can provide that kind of flexibility. Given the number and variety of inputs that a driver can respond to, I'm not sure a supercomputer could do an acceptable job.

Bob Jones
JONESR@ll.vsn22.med.va.gov

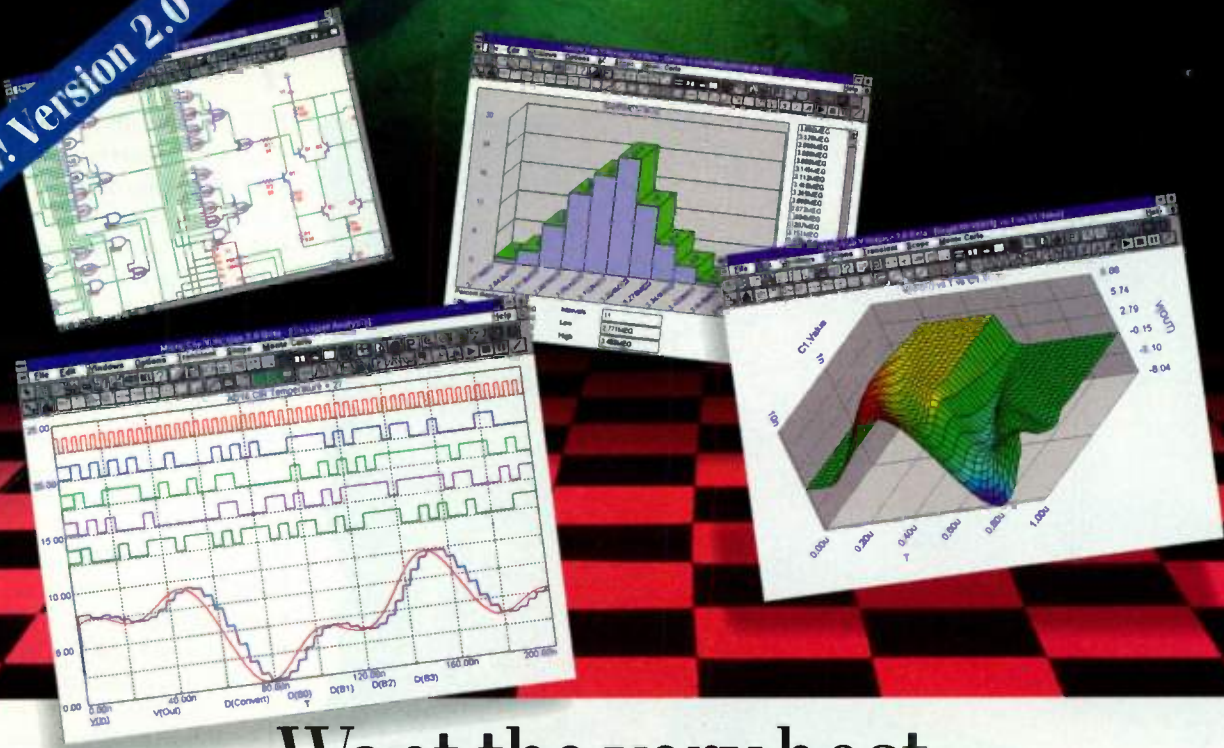
Corrections

On page 158 of the May 12 issue, the sidebar to the *EE Currents & Careers* article contained the incorrect World Wide Web address for the American Engineering Association. The correct address is: <http://www.aea.org>.

On page 135 of the May 27th issue, the incorrect pricing was given for Endevco's 7591 and 7592 series of accelerometers. The correct pricing should have been \$350 for the 7591, and \$250 for the 7592. We apologize for the errors.—Ed.

Readers are encouraged to send their letters and comments to: Letters Editor, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604; fax (201) 393-0204; e-mail: mikemea@class.org.

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"A thumbnail look at what is happening in the world of distribution."

■ PolySwitches In Europe

The Electronics Division of Raychem Corporation, Menlo Park, Calif., has announced an agreement with Arrow Electronics to distribute its full line of PolySwitch products through 18 countries in Europe. Arrow, the world's largest component distributor, already has an agreement with Raychem for distribution of the resettable fuses in all of North America and most of Asia. The agreement is the first to be made by Raychem in Europe and will triple the number of the salespersons handling the product line. PolySwitch fuses are high-impedance polymers in the off-state, and low impedance when no circuit fault exists.

■ Distribution/Mfr. Seminar

A two-day seminar will take place this Sept. 18-19 to align marketing efforts between manufacturers and distributors, giving them the tools to focus their joint marketing efforts. The seminar, to be held at the O'Hare Rosemont Suites Hotel, Chicago, Ill., is designed for one representative from a manufacturing company to be paired with one representative from a distribution company. Work sessions are very open and care will be taken to ensure that direct competitors are not in the same workgroup. The seminar, "Strategic Industrial Marketing 2000," is directed at CEOs, presidents, directors of marketing, and sales managers, and is sponsored by NEDA. Further details can be obtained from Industrial Market Information Inc. at (612) 379-3939. Participation is limited to 25 manufacturer/distributor pairs at a cost of \$2195 per pair.

■ Voice-Recording ICs

One of the fastest-growing component resellers, Digi-Key Corporation, has been chosen by Information Storage Devices (ISD), San Jose, Calif., to offer

a channel for the small-quantity purchase needs of some users. The analog voice record and playback chips designed and manufactured by ISD will be offered in DigiKey's catalog, which contains over 70,000 products from over 180 manufacturers, and is updated every 60 days. Digi-Key has built its reputation on customer service with a heavy commitment to inventory and an order-entry-to-shipment process that is accomplished in under 30 minutes.

■ Embedded Pen Computing

Looking to offer their embedded-PC customers a turnkey system-software platform, Annasoft Systems, San Diego, Calif., have announced a distribution agreement with Communications Intelligence Corporation (CIC), Redwood Shores, Calif., whereby they will sub-license CIC's family of pen products to designers of embedded-PC systems; the agreement includes CIC's handwriting recognition, notepad, and signature security products for DOS and Windows (3.1 and 95 and CE) platforms. As a leading provider of Microsoft operating systems to the embedded-systems market, the CIC products add to the flash-emulation software, custom BIOS products, and real-time enablers they already offer. CIC is a leading supplier of pen-computing software products to hardware manufacturers.

■ Board-Level Interconnects

The broad product base of Samtec Inc., New Albany, Ind., is now available through Capstone Electronics Corp., Aurora, Colo., a division of Arrow Electronics Inc. Samtec manufactures board-level interconnects for the electronics industry with SMT and through-hole, board-to-board, card-to-board, and off-board systems on 0.1- and 0.05-in. pitch, and for 2-, 1-, 0.8-, and 0.64-mm pitches. Samtec is a privately

held corporation with manufacturing facilities in Singapore, Scotland, and Germany; they are both ISO 9001- and 9002-certified. Capstone operates 11 regional centers and one ISO-9002-certified connector-assembly super-center.

■ Mass Distribution For Monitors

The Visual Sensations product lines of monitors from KDS U.S.A., Garden Grove, Calif., have been added to the retail and government sales lines of CompUSA, Dallas, Texas, giving KDS their first mass-merchant retail distributor. Sales volume is expected to exceed more than 15,000 units monthly. The complete range of the Visual Sensations product line is from a 14-in. analog monitor up to their latest 21-in. high-end digital monitor for PC- and Macintosh-compatible use. The monitors are designed for multimedia home and business applications up to high-end graphics applications like desktop publishing and computer-aided design. A high-speed product-replacement program called KARES will be offered with the deliveries from CompUSA. KDS U.S.A. is a subsidiary of Korea Data Systems, Seoul, South Korea; CompUSA has more than 125 superstores nationwide.

■ Datacom Handbook

Many distributors are being left out in the growing and profitable segment of datacom because of a lack of education and confusion with products. This is the view held by GC Electronics, Rockford, Ill., who have put together a datacom handbook for both distributors and datacom contractors. They also added a new computer and datacom catalog to simplify and clarify ordering. The increasing use of telephones, fax machines, computers, and video and portable communications has caused the market for datacom products to be one of the fastest growing in the world. GC also is introducing two new datacom product displays for distributors of all levels of interest and commitment: A bulk contractor display and a 4-ft. "most popular" products display, both expandable as business expands.

■ Tube Company Adds Flat Panels

Well-known for their manufacture and distribution of electron tubes, CRTs and power semiconductors, Richardson Electronics Ltd., LaFox, Ill., has added

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the industrial color display products of Aydin Corporation to its line card. Aydin is a leading manufacturer of display equipment and computer systems for military and industrial applications that include high-resolution flat panel displays, small-screen autosync monitors, and large-screen Spectrum autosync color monitors. The flat-panel displays are available in 13- and 16-in. sizes with resolutions to 1280 x 1024 with PCI and S-BUS graphics cards for total digital interfacing. The products will be sold through Richardson's Display Products Group which has an established niche through cross-referencing CRTs and offering conversion of raw CRT types to an original manufacturer's part number; the company has 60 sales offices and 24 stocking locations worldwide including ISO 9002-registered distribution centers in the USA and Europe.

■ Web Address On NASCAR Trunk

Web address <http://www.squared.com> on the trunk lid of the NASCAR No. 81 Ford Thunderbird represents only a little of the corporate ink that sponsor Square D Co., Palatine, Ill., has invested in the vehicle. Driver Kenny Wallace has yet to make it big, but Square D sees a payoff from the car through its distributors, the primary channel for the company's electrical distribution, control and automation products. Last year Square D entertained 6800 customers worth more than \$500 M of annual business, with distributors paying the company to host their own customers at NASCAR events where racing provides a bond that seals. Sponsorship also includes a sales incentive and merchandising program featuring a slew of Square D racing premium products like a \$3000 go-cart decked out like the Wallace Thunderbird.

■ Technology Exposition

Combining a vendor fair, hands-on training sessions and keynote addresses from industry leaders makes the 1997 Technology Exposition from Pioneer-Standard Electronics Inc., Cleveland, Ohio, different from most such events. The exposition is designed to provide engineers, buyers and managers with information on new technology, trends and products; there will be classroom-style training sessions from more than 20 industry-leading companies to give engineers an advanced look

at where many different technologies are headed, how they will impact designs, and how to implement them. An admission fee of \$25 covers the vendor fair, a choice of four seminars and keynote addresses.

Dates and locations are: Atlanta, 8/19-20; Minneapolis, 8/27-28; San Jose, 9/9-10; Irvine, 9/16-17; Dallas, 9/24-25; Toronto, 10/8-9; Agoura Hills, 10/21-22; and Cleveland, 10/28-29. Call Pioneer-Standard at (888) TEC-EXPO. Registration can also be done on-line at <http://www.pios.com/expo/teceexpo.htm>.

■ Change In RF Direction

The sole source for NEC RF and microwave semiconductors in the U.S. and Canada has long since been California Eastern Laboratories (CEL) of Santa Clara, Calif., whose partnership with NEC dates back to the 1950s. At that time the little known NEC used CEL to develop data sheets and catalogs in English and an extensive test and applications facility to offer North American engineers the characterization data they needed. CEL has now restructured their sales to include national distribution agreements with Reptron Electronics, Bell Industries/Milgray Electronics, and Mouser Electronics. For the Canadian provinces they have added Anthem Electronics Canada Ltd. CEL will continue to operate its own sales offices, with field engineers helping to manage distributor sales at the local level. CEL is an employee-owned company. In addition to distribution, it provides market intelligence to NEC and operates, with NEC, an RF IC design center in Santa Clara; products designed there are manufactured in Japan.

■ New COO Position Created

David W. Fradin, formerly president of Harvard Custom Mfg., has joined IEC Electronics Corp., Newark, N.J., as president and the newly created position of Chief Operating Officer. Russell Stingel, formerly president and CEO, will continue as CEO and Chairman of the board of directors. Fradin's prior experience includes his presidency of EMD Assoc., a number of positions in General Electric and Alcoa Laboratories. He holds a BS degree in Engineering Physics from Cornell, a Ph.D. in Physics from Harvard and an MBA from the Wharton School at the University of Pennsylvania.

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Monday, September 15th

WORKSHOP #1 8:30 AM - 5:00 PM

Designing With DC-to-DC Converters

Eric Persson
Analog Circuit Design Consultant

Dozens of power-converter and switching-regulator ICs are currently available in the marketplace. The key for designers is choosing the one that is best suited to their particular application. But there are the inevitable questions, such as what about the magnetics? What kind of capacitors work best? What is the optimal method of laying out the circuit board so the converter can be tested, and that it will work properly without radiating noise and interference? The answers to these questions and other related issues will be found in this informative, full-day workshop.

About the Lecturer

Eric Persson is an analog-circuit-design consultant. He is an internationally-recognized expert on power-electronics circuits and applications, particularly concerning the design, layout, and troubleshooting of power-converter circuits.

Pre-registration...\$300.00 On-site...\$325.00

WORKSHOP #2 8:30 AM - 5:00 PM

Working With the IrDA Serial Infrared Protocol

This training class examines different aspects of the IrDA standard. Topics include an introduction to IrDA (9.6 Kbits/s to 4 Mbits/s), which includes the hardware specification, the protocol software specification, and the available products (transceiver modules, controller ICs, protocol software, adapters, and peripherals); implementation consideration; test guidelines; compliance testing; interoperability testing; next-generation AIR (Advanced IrDA); and an IrDA product demonstration.

About the Lecturers

Dr. Lichen Wang has 30 years of industrial experience designing products in the areas of communication software, system hardware, IC testing, and artificial intelligence for AT&T, Rohm, Stanford Linear Accelerated Center (SLAC), etc. He co-authored the IrDA protocol specification for compact embedded devices (the IrDA-Lite specification). He has been actively involved in many of the IrDA committees and special interest groups (SIG).

Dr. Keming W. Yeh has 26 years of industrial experience in engineering and management in the IC, LCD, system, and microsensor industries. He was one of the early participants in the formation of PCMCIA and IrDA. He founded and is the president of ACTISYS Corp and holds 10 patents in IC, I/O, and IR device designs.

Pre-registration...\$300.00 On-site...\$325.00

WORKSHOP #3 8:30 AM - 5:00 PM

Wireless Transceiver Design

Syed M. (Moti) Ahmed
Analog Communications, Inc.
(Flemington, NJ)

For engineers and technicians who design subscriber and infrastructure RF and microwave equipment, this popular course offers a thorough treatment of wireless transceivers and their functional blocks. The workshop describes RF and microwave transmitters and receivers and their implementation in personal communications systems, with transceivers for air interface standards such as IS-54 and IS-95 used as examples.

Topics include the antenna, duplexer, receiver, transmitter, and synthesizer subsystem blocks, as well as power-amplifier topology and linearization schemes. Other topics include digital signal processing (including IF digitization), and modulation techniques such as AM, FM, QPSK, GMSK, and QAM.

About the Lecturer

Syed M. (Moti) Ahmed is President of Analog Communications, Inc., of Flemington, NJ, a consulting firm specializing in PCS, CDMA, and cellular designs. He has more than 15 years of experience in designing subsystems and receivers for terrestrial and satellite-communications systems. He has designed a wide variety of RF ICs in GaAs, while at Microwave Semiconductor Corp., RCA Solid State Division, and Bell Laboratories.

Pre-registration...\$300.00 On-site...\$325.00

WORKSHOP #4 8:30 AM - 5:00 PM

RF Power Transistors and Amplifiers—Principles and Practical Application

Norman E. Dye
Normandie Consultants
(Phoenix, AZ)

This comprehensive course provides engineers who design or integrate power amplifiers and transmitters into wireless communications systems with a solid foundation in the nuances of RF power generation and transmission. This course, taught by Norman Dye, a veteran in the field of RF power transistor implementation and amplifier design, focuses on device selection and achieving the highest performance in wireless circuits.

Participants will learn about FET and bipolar characteristics, how power transistors differ from their small-signal counterparts, how to choose between transistor types for various applications, and about biasing, amplifier design, wideband impedance matching, circuit construction, circuit selection (distributed or lumped, single-ended, parallel, push-pull), and frequency compensation and negative feedback.

About the Lecturer

Norman E. Dye has been chief product engineer for microwave ferrite devices, head of microwave

group in the Government Electronics Division, and product manager for RF power products in the Semiconductor Products Sector of Motorola, Inc. He has more than three decades of experience in RF power transistor and amplifier design and applications, and has given seminars on RF transistors throughout the US, Asia, and Europe. He has published numerous technical papers, and co-authored with the late Helge Granberg the book *Radio Frequency Transistors, Principles, and Practical Applications*. He is currently President of Normandie Consultants (Phoenix, AZ).

Pre-registration...\$300.00 On-site...\$325.00

WORKSHOP #5 8:30 AM - 5:00 PM

Wireless Design Made Simple

Al Scott
Besser Associates (Los Altos, CA)

This two-day tutorial-level course is ideal for technical managers and marketing professionals who need to know about RF and wireless technologies, but don't want to suffer through lengthy and complex mathematical explanations. This lively and informative course includes one day devoted to RF principles, systems, and devices and one day on wireless terminology. This second day highlights wireless systems at a block-diagram level and provides insights into different modulation techniques, system functions (such as error correction and voice coding), and wireless markets.

About the Lecturer

Allan Scott is a consultant based in Los Altos, CA with lengthy expertise in the development and manufacture of microwave equipment for radar and communications systems, including affiliations with Bell Laboratories, the US Navy, Hughes Aircraft Co., Sylvania, Teledyne, and Varian Associates.

Pre-registration...\$600.00 On-site...\$625.00

Tuesday, September 16th

WORKSHOP #5 8:30 AM - 5:00 PM

Wireless Design Made Simple (Continued from Monday)

WORKSHOP #6 8:30 AM - 5:00 PM

Wireless RF Circuit Design, Part 1 (Monolithic versus discrete small-signal amplifiers)

Les Besser
Besser Associates (Los Altos, CA)

This one-day workshop examines the choice between using and designing monolithic integrated-circuit (IC) amplifiers versus discrete small-signal amplifiers in wireless systems. The course begins with a review of commercially-available discrete devices and monolithic ICs for low-noise and low-distortion amplification. The workshop progresses into RF and microwave small-signal linear-amplifier design techniques.

The course will explore broadband RF stability and circuit stabilization techniques, and evaluate impedance matching, gain, and noise performance and their trade-offs using lumped and distributed circuit components.

About the Lecturer

Les Besser is President of Besser Associates (Los Altos, CA), an organization of teaching professionals dedicated to high-frequency-electronics continuing education. Known by many as the *Father of Microwave CAE*, he founded software supplier Compact Engineering and developed the first commercial microwave CAE program, Super-Compact, before starting Besser Associates in 1985.

Pre-registration...\$300.00 On-site...\$325.00

WORKSHOP #7 8:30 AM - 5:00 PM

Oscillator Design Principles

Randall W. Rhea
Eagleware Corp.
(Stone Mountain, GA)

For designers who have resorted to modifying an existing oscillator design to create a new one, this course, one of the industry's most consistently popular, is a superb resource.

The course describes a unified method for the design of L-C, crystal, SAW, and T-Line oscillators using a variety of active devices. Topics include S-parameters, amplifier concepts, limiting and starting, noise, biasing, broadband tuning, tuning linearity, and pulling SAWs and crystals. Numerous oscillator examples are presented throughout the course, including SAW, quartz crystal, inductor/capacitor, and distributed types, as well as a broadband UHF VCO, and bipolar, FET, and MMIC devices.

About the Lecturer

Randall W. Rhea is the author of the books *Oscillator Design and Computer Simulation*, *HF Filter Design and Computer Simulation*, and *Cable Television Signal Distribution*. He teaches workshops on oscillator and filter design throughout the world, and founded Eagleware Corp. (Stone Mountain, GA), a prominent supplier of RF and microwave design software, in 1985. He founded Noble Publishing in 1994, which publishes books and videos for the RF and microwave industry, and publishes *Applied Microwave & Wireless* magazine. He received his MSEE degree from the University of Illinois and MSE degree from Arizona State University.

Pre-registration...\$300.00 On-site...\$325.00

WORKSHOP #8 8:30 AM - 5:00 PM

Measuring the Wireless Transmission Spectrum

Morris Engelson
Joint Management Strategy
(Portland, OR)

Anyone working with wireless signals needs this one-day course. Anyone who uses a spectrum analyzer and would like to become more efficient and effective with the instrument should also attend this course. In short, this powerful workshop provides comprehensive insights into different types of wireless signals, such as digitally-modulated signals, electromagnetic interference (EMI), radio-frequency interference (RFI), pulsed signals, high-power signals, broadcast signals, television signals, and effective methods for measuring these signals with a spectrum analyzer. The course explains the many different measurements that are possible on the signals themselves and within a given bandwidth.

About the Lecturer

Morris Engelson is known to many for his long tenure at Tektronix, Inc. (Beaverton, OR) and his association with that company's many lines of high-performance benchtop and portable spectrum analyzers. He now heads the management/technology consulting firm Joint Management Strategy in Portland, OR. His expertise in spectrum analysis is obvious from his two well-written texts on the topic: *Modern Spectrum Analyzer Theory and Applications* and *Modern Spectrum Analyzer Measurements*.

Pre-registration...\$300.00 On-site...\$325.00

Wednesday, September 17th

WORKSHOP #9 8:30 AM - 5:00 PM

Wireless RF Circuit Design, Part 2 (Low-noise amplifiers)

This one-day workshop, which can be taken as a stand-alone course or as a followup to Workshop #6 (Wireless RF Circuit Design, Part 1), is intended to help engineers involved with low-noise-amplifier (LNA) design, including single-stage and multi-stage LNAs. The course teaches LNA design by means of the *available gain* design approach. The workshop considers gain, noise, linearity, stability, and impedance-matching techniques for bipolar and FET amplifiers. Lossless feedback techniques are also examined to improve the input match of an LNA. Interactive computer-aided-engineering (CAE) and computer-aided-design (CAD) techniques will be used by means of video-projection to help students fully understand the topics covered. Illustrative examples contrast trade-offs in price, performance, availability, and flexibility in wireless systems applications.

About the Lecturer

Please see the writeup under Workshop #6: Wireless RF Design, Part 1.

Pre-registration...\$300.00 On-site...\$325.00

WORKSHOP #10 8:30 AM - 5:00 PM

Introduction to Digital Modulation Methods

Harold Walker
Pegasus Data Systems
(Middlesex, NJ)

It is safe to say that all of tomorrow's wireless communications systems will utilize digital modulation schemes. Consequently, anyone who designs or tests wireless products should be well-versed in just how these complex higher-order modulation techniques function and are implemented. In this course, presented by Harold Walker of Pegasus Data Systems (Middlesex, NJ), the basic relationships common to all methods will be discussed including E_b/N_0 , C/N, SNR, P_e , BER, and Shannon's Limit. In addition, the latest advancements in digital modulation schemes will be described along with what the future will bring.

About the Lecturer

Harold Walker, CEO of Pegasus Data Systems, has worked extensively with various modulation schemes, and his patents include microwave transmission of multiple TV channels, quadrature modulation in TV, multiplexing FM subcarriers, pay TV methods, and VPSK modulation. As an adjunct professor, he has taught electronics at the University of Tennessee and computer science at New York Institute of Technology.

Pre-registration...\$300.00 On-site...\$325.00

WORKSHOP #11 8:30 AM - 5:00 PM

Antenna and Array Design for Wireless Communications

Dr. Naftali (Tuli) Herscovici and
Dr. Steven R. Best
Cushcraft Corporation
(Manchester, NH)

Antenna design and implementation require innovative thinking as wireless communications capability finds its way into more and more small portable devices. For anyone tasked with the challenges of integrating antennas into portable designs, this course is absolutely essential.

The course, taught by Cushcraft's chief scientist Naftali Herscovici, and Steven Best, the company's director of engineering, covers a broad array of antenna topics, from fields and basic concepts to software and simulation. Areas of discussion include E and H field, and near-field and far-field theory, elementary antennas such as dipoles and loops, propagation, and types of antennas.

About the Lecturers

Dr. Naftali (Tuli) Herscovici is chief scientist with Cushcraft Inc. (Manchester, NH), and has served as a research associate with Gordon McKay Laboratory at Harvard University, as senior project engineer with Seavey Engineering, and as a senior antenna designer at Chu Associates. He is the author of the book *Analysis of Aperture-Coupled Printed Antennas and Transmission Lines*, and has written more than two dozen papers on antenna design for

IEEE and other journals. He is currently chairman of the Boston Chapter of the IEEE Antenna and Propagation Society.

Dr. Steven R. Best is director of engineering at Cushcraft, has held antenna engineering positions at D&M/Chu Technology, is Vice President of Parisi Antenna Systems, and has written numerous papers and articles on antenna design. He received his Ph.D. in Electrical Engineering from the University of New Brunswick.

Pre-registration...\$300.00 On-site...\$325.00

WORKSHOP #12 8:30 AM - 5:00 PM

Materials and Processing for RF/Microwave Hybrids

Richard Brown
Richard Brown Associates, Inc.
Consultant,
Hybrid Microelectronics
(Huntington, CT)

The growing demand for wireless communications products and continuing development of monolithic microwave integrated circuits (MMICs) is forcing system and product designers to choose between hybrids and MMICs (i.e., discrete devices versus a complete system on a chip or, more often, somewhere in between). This one-day workshop begins with a comparison of MMICs and hybrids, followed by a discussion of transmission lines and impedance matching in RF/microwave hybrids. It continues with a review of conductor and substrate material properties and a discussion of processing technologies suitable for hybrids.

About the Lecturer

Richard Brown is a technical consultant in hybrids, with more than 30 years of experience in thin-film, thick-film, electroplating, and substrate technologies. His career includes stops at Bell Telephone Laboratories, RCA Solid State, and Alcoa, where he managed a technology team that implemented thin film on high-temperature co-fired ceramics for multichip modules (MCMs). He holds seven US patents and is the author or co-author of numerous publications, including the text *Materials and Processes for Microwave Hybrids*, which was published in 1991 by the International Society of Hybrid Microelectronics (ISHM).

Pre-registration...\$300.00 On-site...\$325.00

WORKSHOP #13 8:30 AM - 5:00 PM

EMC Problems and Solutions for Portable Electronics

William D. Kimmel
Kimmel Gerke Associates
(West St. Paul, MN)

This full-day session focuses on common electromagnetic-compatibility (EMC) problems in portable electronic equipment and solutions for those problems. The session starts with the *Physics of EMI*, emphasizing the frequency-amplitude time impedance and dimensions (FAT-ID) approach to grounding and shielding as related to portable design. It continues with a number of case histories of EMC problems and subsequent solutions, providing a nuts-and-bolts approach to the design issues commonly encountered in electronics design.

About the Lecturer

William D. Kimmel is a principal in leading consulting firm Kimmel Gerke Associates. He has more than 30 years experience in electromagnetic-compatibility (EMC) design and troubleshooting in military, automotive, industrial, medical, and commercial applications.

Pre-registration...\$300.00 On-site...\$325.00

Thursday, September 18th

WORKSHOP #14 8:30 AM - Noon

Introduction to Spread Spectrum

Jack M. Holtzman
Wireless Information Network
Laboratory (WINLAB) of Rutgers
University (New Brunswick, NJ)

Anyone who needs to understand spread spectrum modulation and the code-division-multiple-access (CDMA) method in order to develop wireless products will benefit greatly from this course. This course, taught by WINLAB Associate Director Jack Holtzman, provides a thorough background in spread spectrum concepts, benefits, implementation, and impact on system design. This course covers capacity, processing gain, power control, multipath, synchronization, code sequences, interference cancellation, and many other topics.

About the Lecturer

Dr. Jack Holtzman worked with AT&T Bell Laboratories for 26 years, where he was head of the teletraffic theory and system performance department. In 1990, he joined Rutgers University, New Brunswick, NJ, where he is professor of electrical and computer engineering, and associate director of the Wireless Information Network Laboratory (WINLAB). He is also director of the Wireless Communication Certificate Programs. Dr. Holtzman's current areas of work include spread spectrum, handoffs, resource management, location estimation, propagation, and wireless system performance.

Pre-registration...\$200.00 On-site...\$225.00

Four Days of Technical Sessions

In addition to its diverse workshops, The Wireless & Portable Design Conference offers a wide range of technical sessions, consisting of half-hour presentations by individual authors followed by a five-minute question-and-answer period.

These technical sessions will cover topics of interest to design engineers in need of design solutions for wireless and portable systems, such as cellular communications systems, PCS, and WLANs.

Topics will include:

- ★ Designing with current and future battery technologies
- ★ Controllers for portable devices
- ★ Amplifiers for cellular and PCS systems
- ★ Components and circuits for wireless data systems
- ★ Packaging solutions for portable and wireless integrated circuits (ICs)
- ★ Practical analog and digital measurements for wireless systems
- ★ Coping with higher clock frequencies in digital systems
- ★ Achieving true omnidirectional coverage in cellular and PCS base stations
- ★ Wireless antenna technologies
- ★ Modulation techniques for present and future communications systems

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To qualify for Advance Registration Discounts, this form must arrive before August 29.

A comprehensive conference package will be mailed to you immediately upon receipt of your form.

ON-SITE REGISTRATION

- Monday - Wednesday, September 15 -17
7:30 a.m. - 5:00 p.m.
- Thursday, September 18
7:30 a.m. - noon

STEP #1 TYPE OR PRINT CLEARLY *For additional registrations, please duplicate this form.*

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STEP #2 PLEASE REGISTER ME FOR THE FOLLOWING WORKSHOPS OR TECHNICAL SESSIONS:

WORKSHOPS

		Advance	On-Site
<input type="checkbox"/>	Workshop #1 Designing With DC-to-DC Converters <i>Monday, September 15- 8:30am - 5:00pm</i>	\$300	\$325
<input type="checkbox"/>	Workshop #2 Working With the IrDA Serial Infrared Protocol <i>Monday, September 15- 8:30am - 5:00pm</i>	\$300	\$325
<input type="checkbox"/>	Workshop #3 Wireless Transceiver Design <i>Monday, September 15- 8:30am - 5:00pm</i>	\$300	\$325
<input type="checkbox"/>	Workshop #4 RF Power Transistors and Amplifiers—Principles and Practical Application <i>Monday, September 15- 8:30am - 5:00pm</i>	\$300	\$325
<input type="checkbox"/>	Workshop #5 Wireless Design Made Simple <i>Monday, September 15- 8:30am - 5:00pm</i> <i>Tuesday, September 16- 8:30am - 5:00pm</i>	\$600	\$650
<input type="checkbox"/>	Workshop #6 Wireless RF Circuit Design, Part 1 (Monolithic versus discrete small-signal amplifiers) <i>Tuesday, September 16- 8:30am - 5:00pm</i>	\$300	\$325
<input type="checkbox"/>	Workshop #7 Oscillator Design Principles <i>Tuesday, September 16- 8:30am - 5:00pm</i>	\$300	\$325
<input type="checkbox"/>	Workshop #8 Measuring the Wireless Transmission Spectrum <i>Tuesday, September 16- 8:30am - 5:00pm</i>	\$300	\$325
<input type="checkbox"/>	Workshop #9 Wireless RF Circuit Design, Part 2 (Low-noise amplifiers) <i>Wednesday, September 17- 8:30am - 5:00pm</i>	\$300	\$325

WORKSHOPS

		Advance	On-Site
<input type="checkbox"/>	Workshop #10 Introduction to Digital Modulation Methods <i>Wednesday, September 17- 8:30am - 5:00pm</i>	\$300	\$325
<input type="checkbox"/>	Workshop #11 Antenna and Array Design for Wireless Communications <i>Wednesday, September 17- 8:30am - 5:00pm</i>	\$300	\$325
<input type="checkbox"/>	Workshop #12 Materials and Process for RF/Microwave Hybrids <i>Wednesday, September 17- 8:30am - 5:00pm</i>	\$300	\$325
<input type="checkbox"/>	Workshop #13 EMC Problems and Solutions for Portable Electronics <i>Wednesday, September 17- 8:30am - 5:00pm</i>	\$300	\$325
<input type="checkbox"/>	Workshop #14 Introduction to Spread Spectrum <i>Thursday, September 18- 8:30am - noon</i>	\$200	\$225

TECHNICAL SESSIONS

		Advance	On-Site
<input type="checkbox"/>	Technical Session Full Conference (Includes All Technical Sessions, Keynote, Reception, digest.)	\$350	\$400
<input type="checkbox"/>	Technical Session Single-day Conference	\$150	\$200
<input type="checkbox"/>	Keynote Luncheon	\$25	\$30

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**Wireless & Portable Design Conference
WORKSHOPS AT A GLANCE**

Monday, September 15th

- 8:30 - 5:00 #1 Designing With DC-to-DC Converters
- 8:30 - 5:00 #2 Working With the IrDA Serial Infrared Protocol
- 8:30 - 5:00 #3 Wireless Transceiver Design
- 8:30 - 5:00 #4 RF Power Transistors and Amplifiers—
Principles and Practical Application
- 8:30 - 5:00 #5 Wireless Design Made Simple

Tuesday, September 16th

- 8:30 - 5:00 #5 Wireless Design Made Simple
(Continued from Monday)
- 8:30 - 5:00 #6 Wireless RF Circuit Design, Part 1
(Monolithic versus discrete small-signal amplifiers)
- 8:30 - 5:00 #7 Oscillator Design Principles
- 8:30 - 5:00 #8 Measuring the Wireless
Transmission Spectrum

Wednesday, September 17th

- 8:30 - 5:00 #9 Wireless RF Circuit Design, Part 2
(Low-noise amplifiers)
- 8:30 - 5:00 #10 Introduction to Digital Modulation Methods
- 8:30 - 5:00 #11 Topic: Antenna and Array Design for Wireless
Communications
- 8:30 - 5:00 #12 Materials and Processing for RF/Microwave Hybrids
- 8:30 - 5:00 #13 EMC Problems and Solutions for Portable
Electronics

Thursday, September 18th

- 8:30 - Noon #14 Introduction to Spread Spectrum

H O T E L A C C O M M O D A T I O N S

A block of rooms has been reserved at the Boston Marriott Burlington. To make your reservations, please call 1-800-228-9290 or 1-800-371-3625. When making your reservations, please mention the Wireless & Portable Design Conference and take advantage of our \$154 group rate. The Boston Marriott Burlington is conveniently located on Routes 128 and 3A, and is just minutes away from Boston's Logan Airport.

Keynote Luncheon

Mr. Thomas Leonard
Chief Executive Officer
Alpha Industries (Woburn, MA)

Join us for lunch on Monday, September 15th, at 12:00 noon for an informative talk by one of the area's leading technology managers, Mr. Thomas Leonard, CEO of Alpha Industries in Woburn, MA.

With over 30 years experience in the high-frequency industry, Tom is a respected manager of one of the world's foremost wireless RF semiconductor suppliers. He is also a strong proponent of total-quality-management (TQM) and world-class manufacturing techniques, both in force at Alpha. Come for lunch and catch Tom's talk on TQM and its place in wireless manufacturing.



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Today's CEOs — How They Got There, And Where They're Going

Debra Schiff

The face of upper management appears to be changing. According to a recent study by executive search firm Christian & Timbers, a little less than a third (31%) of new (one-to-five years in the position) CEOs are rising to the top from the sales and marketing fields. Going back a few years to the late 1980s and early 1990s, most of the CEOs came from operations and finance (47%). Of the CEOs with 11 years or longer in their position, 50% rose to their status through the operations and finance track.

Christian & Timbers' study looked at 111 CEOs, 34 of whom have been CEOs for one-to-five years, 49 of whom have been CEOs for six-to-ten years, and 28 of whom had 11-or-more years of CEO experience. Two of the other categories that spawned CEOs in the study were operations and engineering and general manager. Increasingly, fewer general managers are becoming CEOs. Of the longest-tenured CEOs, six (21% of those polled) rose through the ranks from general manager status. In the six-to-ten year sector, five (10%) of the CEOs had previously been general managers. And the sinking trend continues, with three of

the one-to-five years study participants giving up their general manager title to become CEO.

The opposite trend is working in the operations and engineering category. From the study, two CEOs with 11 or more years in the position came up through operations and engineering, representing only 8% of the CEO population polled. Of the 49 CEOs with six-to-ten years of experience 14% (seven) CEOs were operations and engineering professionals. And, in the "new" CEO sector, seven (21%) of the CEOs came from operations and engineering backgrounds. None of the CEOs who participated in the study had been CEOs prior to their current position. All of the respondents were vice presidents or had similar titles at the same level.

How They Spend Their Time

When the CEOs were asked what they spent the majority of their time on, there was a big difference between how the "new" CEOs answered and how the 11 years or more group responded. The group with more experience was split between administrative tasks, reactive problem solving, and

dealing with customers (all 21%). Otherwise, they were involved in visiting operations/managing direct reports (15%), decision making/strategy (11%), or dealing with suppliers (11%).

The "new" CEOs flipped the triangle over and spent the lion's share of their time dealing with customers (29%) or making decisions/planning strategies (26%). Dealing with suppliers was third on their list, weighing in at 24% of the participants saying that this was their primary job function. At the bottom of the list were visiting operations/managing direct reports (12%), reactive problem solving (6%), and administrative tasks (3%).

Similarly, the six-to-10 years group responded that the primary function of their position is to deal with customers (27%). Also following the "new" CEO pattern, decision making/strategy took second place (23%), with dealing with suppliers closing up the gap with 18%. Taking a lower priority are visiting operations/managing direct reports (16%), reactive problem solving (10%), and administrative tasks (6%).

It appears from the survey that function follows form. If you come from a background of sales and marketing, it simply makes sense that you're bound to spend the majority of your time dealing with customers. But the contrast between the traditional CEO and the new CEO is so sharp that it poses some interesting questions. Is the trend toward sales and marketing professionals rising to the top a function of a "money first" strategy, rather than a "quality first" strategy? Is this the direction that education was going while the "new" CEOs were in college? Will the new CEOs be at the same firm in, say, 11 or more years? All rhetoric aside, Christian & Timbers rates the three top functions for the new CEO, dealing with customers, decision making/strategy, and dealing with suppliers/managing direct reports to be of paramount importance to a CEO's success. They base that assertion on thousands of interviews they've con-

HOW CEOs SPEND MOST OF THEIR TIME

Job Functions	Number of years as CEO		
	1 to 5	6 to 10	11+
Dealing with customers	29%	27%	21%
Decision making/strategy	26%	23%	11%
Dealing with suppliers	24%	18%	11%
Visiting operations/managing direct reports	12%	16%	15%
Reactive problem solving	6%	10%	21%
Administrative tasks	3%	6%	21%

ducted regarding which tasks make CEOs successful.

Order Of Succession

Another zone of opposition for the CEOs is the question of succession. To hire a successor or not, that is the question. The new CEOs greatly accept the idea, with 85% of the respondents affirming that they have planned for succession. They have a person in mind that they are specifically grooming to take over the position. Also in the same camp are the six-to-10-year respondents who approved their succession program by 71%. The other end of the spectrum saw the 11-years-or-more CEOs greatly disapproving of the process, with only 29% having a successor already in place.

Through the company's interviewing process, Christian & Timbers determined that the new crop of CEOs have adapted to today's mobile work environments and have fully accepted the succession procedure as an element of the managerial process. The executive search firm also says that

the traditional CEO will more likely keep his or her position, and has not put much thought toward succession.

How's The Team Doing?

On making a judgement call about how their executive teams are doing, the CEOs all pretty much agreed that their teams need some work. Of the new CEOs, 68% said that they did not feel that they had a strong executive team. The six-to-10 year category also felt that their teams needed some work (53%). And, the traditional CEOs largely agreed (64%) that their teams were not satisfactory.

According to the interviewers, CEOs as a group, "are never completely satisfied" with their teams. The six-to-10 years group did have the highest confidence in their teams, with a 37% vote of confidence. This approval is probably due to the CEOs time in reengineering the team. The "new" engineer hasn't had the time to do the work on the team, yet, and the tenured CEO typically keeps the people who've helped him or her step up the ladder

along the way (no matter how bad performance may get).

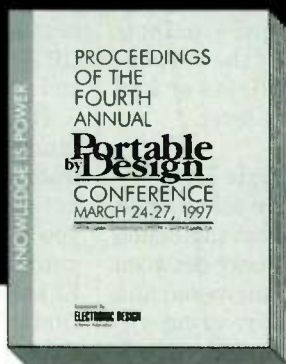
As For The Future...

In looking at the evolution of the role of CEO over the next five years, there appears to be no significant difference between the amount of time a CEO has in his or her back pocket and their opinion of the future. The largest percentage (34%) think that what is needed is an improvement in leadership. Generally (30%), the CEOs believe that the role of the CEO will become increasingly more difficult in the years to come. Some CEOs (19%) think that the role will remain the same through the turning of the century, and 17% declined to comment.

For more information on Christian & Timbers' "Private Company CEO Study," contact Jeffrey Christian, One Corporate Exchange, 25825 Science Parke Dr., Suite 400, Cleveland, OH 44122; (216) 464-8710; fax (216) 464-6160; Internet: <http://www.ctnet.com>.

Debra Schiff is a copy editor at Electronic Design.

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AUGUST 1997



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R&D Hardware-Digital Design Engineer

In this position, you will be responsible for developing state-of-the-art telecommunication test equipment. Duties will involve conceptual design and prototype validation at the board level of high-speed microprocessor/DSP based technology. Requirements include a MSEE/CS or equivalent; 4+ years' related experience; and a strong background with digital logic design, FPGA and ASIC. Must be familiar with development tools such as Viewlogic or OrCAD, VHDL, timing analyzers/simulators or MathCAD. You must also be proficient in C/C++ to develop low-level software drivers. Experience with DS1/3, ATM, Frame Relay or a telecom background a plus. **JOB CODE 650R**

R&D Firmware Design Engineer

Develop state-of-the-art telecommunications test and measurement technology for transmissions networks, including interfacing with hardware/firmware development engineers to develop real time embedded functions using C/C++, 68xxx and RISC assembly languages. Requires an MSCS/BSEE or equivalent, 2+ years' experience, and knowledge of software design methodologies, including concurrent design techniques. Excellent documentation skills a must and experience with DS3/T3/T1 Telecom Interfaces and X.25, ATM, Frame Relay protocols is a plus. **JOB CODE 650R**

RF Design Engineer

In this key position, you will perform RF and system design from requirements definition through production release. You will be involved in product definition, design, and performance verification. Requires a BSEE/MSEE or equivalent, 5+ years' experience in high-frequency RF design and analog circuit design. Strong analytical skills and the ability to work independently are musts. Familiarity with Vector Network Analyzers and design experience using RF/Microwave test equipment preferred. **JOB CODE 610R**

Software Section Leader/Architect

In this position, you will review/apply SW architecture and partitioning techniques toward the development of telecom systems products, as well as be directly involved in the design of firmware/workstation-based systems. In addition, you will manage an R&D development group for Windows 95/NT-based systems. Requires an MSCS or equivalent, 8+ years' R&D experience, including 5+ years' in communications and 3+ years in management or a project lead role. You must also have 3+ years' direct C/C++ experience with SQL Db. Visual Basic experience a plus. **JOB CODE 650J**

Applications Engineer

Provide installation support, equipment engineering support, acceptance test procedures (ATPs) customer service support, field and beta trials, and customer training. In addition, you will be involved with sales/marketing efforts such as sales presentations and marketing related activities. Requires a BSEE or equivalent and 5+ years' experience with a telephone company or telecommunications manufacture in a similar technical capacity. Experience in private line testing and X.25 networks desired. **JOB CODE 761M**

- Electronic Technician** **JOB CODE 360B & 900S**
- Production Test Technician** **JOB CODE 470W**
- SMT Technician** **JOB CODE 371R**
- Acctg. Professional** **JOB CODE 810H**
- Fab Operator** **JOB CODE 621K**
- Assemblers** **JOB CODE 400W**

Embedded Software Engineer R&D

Requires a BSCS/MSCS or equivalent and 4+ years' experience developing software for real-time, multi-tasking embedded system using C. In addition, you must also have a working knowledge of TCP/IP and X.25 protocols in the embedded system, experience with good software development methodology, and excellent communications skills. Prior experience with digital telephony and telecom test equipment is a definite plus. **JOB CODE 650S**

Microwave/Millimeter Design Engineer

Responsible for Microwave/Millimeterwave component and sub-system design, from requirement definition through product release. Requires knowledge of Touchstone or Libra (similar CAD) and 3+ years' related engineering experience. You should be familiar with Mixer, Frequency Multiplier, Oscillator, Filter, Switch, Coupler, Up/Down Converter in Microstrip, Suspended Substrate, Finline and Wave-Guide. An MSEE or equivalent is preferred. **JOB CODE 620L**

Manufacturing Engineering Manager

Manage the manufacturing, test and process engineering functions for a vertically integrated electronic manufacturing organization. This includes transitioning new products from development to production, supporting production assembly/test operations, and sustaining engineering of existing support. Requires a BSEE or equivalent, and knowledge of electronic assembly/test operations, including SMT, mechanical, test automation, process control, PCB and sheet metal fabrication/finishing. Familiarity with electronic component technologies, telecommunication standards, and domestic/foreign agency compliance testing preferred. Prior supervision/management experience and data communications knowledge a plus. **JOB CODE 584M**

Microwave & RF Design Engineer

Responsible for Microwave & RF component and sub-system design from requirement definition through pilot run release. This person will be involved in CKT design, performance verification, setting specifications, sustaining the product in the production line, and training manufacturing and production personnel to work on new designs. Requires an MSEE or equivalent with knowledge of Touchstone, Libra (or similar CAD), and E-M simulation. Related engineering experience in amplifiers, oscillators, modulators, filters, switches, up/down converters, and receivers is a plus. **JOB CODE 620L**

Manufacturing Engineer - Telecom Products

Working within a product team environment, you will be responsible for introducing and sustaining our exciting line of Telecom Test Instruments, including fiber optics, high-speed digital and analog test instruments. In addition, you will handle new product introduction, product reliability enhancement, component sourcing, production support, and cost/material analysis. Requires a BSEE or equivalent, 2+ years' Telecom industry experience, the ability to perform electrical circuit analysis, and excellent communication skills. Experience with electromagnetic compliance work, ORCAD and CADKEY tools is desirable. **JOB CODE 584K**

Specials Manager

In this key position, you will manage 5-7 engineers developing special products for Microwave Manufacturing Instruments and components. In addition, you will design/test special products, including electrical, mechanical and firmware design. Requires a BS in EE/CS/ME or equivalent and 5+ years' experience in design or manufacturing/test engineering. Supervisory experience desired. **JOB CODE 610R**

Engineering Manager (Systems)

Manage a group of engineers chartered to design specialized RF and microwave instrumentation systems. Interface with customers to determine system design requirements. Requires a BSEE or equivalent (MSEE preferred) and 10+ years' experience in microwave instrumentation design. Knowledge of microwave communication, radar and electronic warfare systems a plus. The candidate should have both interface and ATE test experience. **JOB CODE 610G**

Director of Marketing

Organize and supervise the marketing department responsible for all Telecom division products. Lead the division strategic planning process. Manage and recruit product managers to achieve marketing objectives. Requires a BSEE or equivalent (MBA preferred) and 15+ years' experience, preferably in marketing. **JOB CODE 800P**

North American Regional Marketing Manager

Represent Wiltron MMD in North America. Interface with customers and the A W sales organization. Make decisions regarding overall sales strategy (market share) in the region and provide feedback to product marketing. Good understanding of RF and microwave products and North American Market is essential. **JOB CODE 731S**

Metrologist

Establish and maintain a Z540/ISO guide compliant calibration system, as well as support production, test and development engineering in calibration issues. Requires a technical degree or equivalent and 3+ years' experience in calibration. **JOB CODE 570B**

Technical Support Engineer

Provide technical support, troubleshoot/repair system and module levels, and evaluate Wiltron development products. Requires an AS degree or equivalent (BA/BS in a technical discipline preferred), as well as a strong background in telephony and telecommunications. An understanding of VMS, UNIX, Windows, and LAN protocols (X.25, LAT, TCP/IP) is desired and some domestic/International travel may be expected. **JOB CODE 320B**

Test Engineer

This new position will be responsible for supporting the Spectrum Analyzer product line. Duties will involve test procedures, software and fixture design. A BSEE or equivalent and 5+ years' experience in a production test engineering environment is required. Knowledge of RF and microwave measurements is desirable. **JOB CODE 900S**

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Silicon Valley Is Again An Engineering Hotbed

NEW OPPORTUNITIES ARE CROPPING UP AT AN EXTREMELY FAST RATE IN THE ENGINEERING WORLD'S LAND OF PLENTY.

Paul McGoldrick

We promised that in this issue we would try to break down the EE market in Silicon Valley to see what was happening. The real surprise I found in analyzing the situation, and in talks with the hiring managers, was the low number of vacancies advertised in the Valley, even though the jobs really are there! This is quite a change in the last couple of months, and needed further investigation.

Meanwhile, our tables this month show some selected vacancies in both the Valley and in San Diego, which in contrast, is advertising like gangbusters on a national level. There is, quite obviously, a major shortage of talent for the CDMA industries in San Diego, and the advertising reflects this. Again, it is a good time to be in San Diego if you are an RF engineer, particularly with PCS experience. But there are vacancies in all the disciplines. There are even good old-fashioned analog developments taking place in the cable-TV industry business of GI (General Instruments).

Other interesting jobs available include a multitude of multimedia challenges at Rockwell Semiconductors (formerly Brooktree), where they also are working on networking problems and wireless systems, while Sensormatic is at the leading edge of a new video revolution with the storage and recording of video as pure data. AMCC is breaking completely new processing ground with their ex-

tremely fast communications ICs, and a start-up — InfoGation — is working on the development of multimedia car navigation and communications systems.

Philips Semiconductors is about the only conventional semiconductor manufacturer who is advertising for staff across the board, but the jobs in all the other companies exist. If you are an effective IC design engineer, the unemployment rate is virtually zero. All the IC companies are limited in their rate of development of new products by the limitations of their design staff. So, if you are in that fortunate category of engineer, particularly for analog circuits, and more particularly RF, choose the company you want to work for and go knock on the door. It won't stay closed for long.

National Semiconductor is looking for software engineers by the bucket. The new management has targeted consumer products as one its core markets, and the production of

Information Appliances is intensely software-heavy.

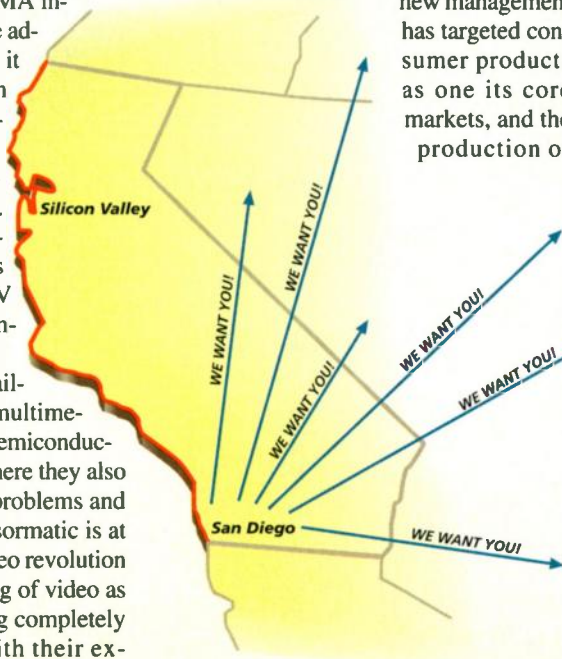
When you start talking with human resources people at the various semiconductor companies, you get a feel for some of their frustrations. It doesn't seem to matter how often they advertise, they say, they just don't get the qualified people applying. When they really have to hire somebody, they will use a recruiter with all the additional expense that entails. They don't like it, but there is no choice.

The biggest expense is, of course, when they need to get staff into the Valley from somewhere else. As we have noted before, the creation of design centers away from headquarters is at its most ambitious right now. But if there is only a single design person, or a couple, the expense of creating such a center is usually not justifiable. And there are a number of lead roles where people have to be on-hand in the physical locale of the main company offices.

It is difficult to get any idea about what the incentives are averaging to bring people into Silicon Valley simply because the companies don't want to talk about it, and the employees regard the deal they make as being personal. But without knowing the exact dollars, employers are offering signing bonuses, home deposits, larger stock options, and guaranteed bonuses. So, if you are involved in such a negotiation, you should know that there are many things you can target.

Apart from the semiconductor manufacturers, there are vacancies all over. The network companies in the Valley are probably the most vigorous in their expansions, and if you look at a company like Cisco, their weekly vacancy lists are hundreds of pages long. The same is true of a company like NET. Recommending people, as an existing employee, is now commonly paying \$500 and, in some cases, up to \$5000. This is true of an amazingly high percentage of employers.

This is serious consideration at the moment. The ingress into Santa Clara county is now averaging 3000 a month; housing is getting tighter and more expensive. Even



getting a hotel room in Sunnyvale, for example, can be difficult at short notice, because of the number of newcomers who are having to stay in such places until they can get settled. But the Valley has been through all this before.

What happened in the '80s was that the Valley reached a point where it seemingly could not absorb any more humanity. Employers began to realize that they couldn't get the employees they needed, and there were several major relocations to Nevada,

Colorado, and Oregon. The housing market went into a major spiral at the same time that the economy went south. The numbers in 1997 are much larger. Because of increased housing east of the Bayout towards I-5, and south of the Bay, in places like Morgan Hill and Gilroy, the humanity absorption is much larger. Several major road projects support that increase.

But is the breaking point going to come again? It is noticeable that every road improvement seems to be negated after just 3

or 4 months. The unemployment rate for engineers is less than 1% overall, and considerably less than that for virtually all the categories our readers fall into. Movement of personnel between companies, even with stock options in place, has been increasing. And people will leave for another job for some fundamental reasons: To save crossing a bridge in their commute, to have the luxury of one or two days a week telecommuting, or because a new employer offers day-care. Most of the pre-

Company (business)	Major vacancies
SILICON VALLEY:	
AMD (CAD Technology Group) Sunnyvale	CAD and methodology manager Mask design engineers MTS CAD design engineers
Circuit City R&D (multimedia) Santa Clara	Group leader/ASIC engineer
DSC Communications (Digital Switches) Petal	Design and development software engineers Test and quality software engineers Systems software engineers Design and test hardware engineers Systems engineers Product line managers
Fujitsu Microelectronics (LSI Technology) San Jose	Logic designers -- embedded controllers Staff applications engineer (embedded processors) Senior staff architect (imaging & communications) Circuit design engineers Design technology manager IP applications manager
Hewlett Packard (microwave instrumentation) Rohnert Park/Santa Rosa	RF and microwave engineers Software engineers Test software technicians
IKOS Systems (Design Verification Tools) Cupertino	Software engineers Applications engineers Product marketing engineers
Imatron (CT and EBT Scanners) South San Francisco	Senior software engineers Software engineers
National Semiconductor (Information Appliances) Sunnyvale/Santa Clara	Software engineers -- EDA Software engineers -- Modeling Software engineers -- CAD front-end
Philips Semiconductors (Communications Products) Sunnyvale	Software engineers -- Verification Software engineers -- CAD Software engineers -- Physical design TDMA project leader Senior RF systems engineers Mixed-signal circuit design engineers RFIC design engineers Test engineers Product engineers Senior DSP system engineers Analog design engineer Digital IC design group leader Senior digital IC design engineer Analog IC design group leader Senior analog IC design engineer Senior engineers (read channel) Senior test engineer Mixed signal test engineer Applications engineer
(Mass Storage) Sunnyvale	
Synopsys (EDA Software) Mountain View	Software engineers R&D software engineers Multimedia hardware engineers Emulation board design engineers Corporate applications engineers IC design methodology managers Customer support engineers Telecom program manager Director of product marketing Product marketing managers Technical marketing manager -- simulation

Company (business)	Major vacancies
SAN DIEGO:	
AMCC (GHz communications ICs)	Analog circuit design engineers Digital circuit design engineers Product development engineers Standard cell architects Gate array architects Digital logic designers Layout designers Methodology development engineer Bipolar/BiCMOS circuit design engineer Characterization engineers Design automation engineers ASIC product marketing manager PCI product marketing manager Senior process engineers Process integration engineers
Cymer (Excimer Lasers)	Technical training instructor Laser test engineers Product marketing engineers Process engineers Compliance/electrical engineer Reliability engineer Systems engineer Director of product development Lithography engineer Senior quality engineer Customer systems engineers Technical support manager Pulsed-power physicist
DENSO Wireless Communications (CDMA/PCS Products) Carlsbad	Senior embedded software engineers Embedded software engineers Software configuration management engineer Software test engineer Windows software engineer Digital hardware engineers Senior RF design engineers RF design engineers Senior Communication systems engineers Test & verification engineers
General Instrument (Television & Data Systems)	Firmware engineers VLSI engineers Systems integration engineers Systems test engineers
InfoGation (Car Navigation)	Senior software engineers
LG InfoComm (LAN) (CDMA Samsearch)	ATM development team leader Software systems leader Software engineers DSP engineers DSP leader ASIC engineers Telecommunications engineers
(CDMA Samsys)	R & D leader engineer/manager RF systems engineer RF engineer Field test engineer Software engineer Hardware design engineer
Qualcomm (CDMA Products)	Analog ASIC design engineers RF ASIC design engineers Component engineers (RF, analog)

vious retention factors involving money simply aren't working any more because the numbers offered by the different companies are comparable and the promises just as good. The exceptions are still the start-ups that conventionally offer "barely alive" salaries but with extraordinary rewards possible if things go right. Working for adrenaline is for the minority.

It really is a wonderful time to be a design engineer or manager in Silicon Valley; let's hope it stays that way.

Paul McGoldrick is Analog Editor at Electronic Design; he can be reached at (408) 441-0557, X 113 or by e-mail PMcGoldrick@compuserve.com

Company (business) & digital)	Major vacancies
Rockwell Semiconductor (Digital Infotainment)	Interconnect systems engineers Software engineers VLSI CAD engineers VLSI design engineers VLSI RF product engineers VLSI mixed-signal test engineers
(Network Access)	Applications engineer DSP engineers Embedded software engineer Mixed-signal IC design engineers RF IC design engineers Analog IC design engineers IC layout designers IC product engineers IC test engineers RF system engineers Software engineers Software test engineers
(VLSI Engineering)	Applications engineers DSP engineers Hardware engineers IC layout designers Product marketing engineers Project engineers Software engineers Staff/senior systems engineers Systems engineers Systems and VLSI architects
(Wireless Communications)	ASIC design engineering manager ASIC design engineers CAD engineers Design automation engineers IC design engineers System administrators Staff CAD engineers Senior software engineers
Sensormatic Video Products (Video Storage)	Digital test engineers Mixed-signal test engineers DSP engineers Layout designers Manager, RF systems Protocol applications engineers RF design engineers RF product engineers RF systems engineers Speech processing engineer System architects
Sony-WTC (Wireless: CDMA & AMPS) manager	Senior software engineer Embedded software engineer Telecom engineer
engineer	Software engineers Systems test engineers Quality assurance engineer Interop/field test engineer Software quality assurance
	Production test engineer User interface software engineer Call processing software engineer ASIC design engineers Test tool design engineer Interface engineer Quality assurance manager DSP/CDMA system software
	RF design engineers Field test engineers Accessories design engineer

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RF CAE/CAD DESIGN TOOLS ADMINISTRATOR

You will create and manage the overall CAE/CAD tool environment within the RF Design Engineering Department. This will involve installing/maintaining/upgrading appropriate software, setting up project directories, creating script files/macros, managing CAE/CAD libraries, plus developing standards, procedures and application notes.

Requires a BSEE or equivalent, 5+ years' experience with 2+ years in CAE/CAD tool management. Experience with UNIX, CAD workstation IC layout tools (Opal, Onyx, Jade, etc.), PCB tools (PCAD), and circuit simulators (MicroSim, HP/EESof, HP/HFSS, LEX, Touchstone, Spice, etc.) required. Familiarity with hardware design processes and associated documentation practices desirable.

SENIOR/LEAD RF/MICROWAVE DESIGN ENGINEER

You will lead the technical design and implementation, project management and proposal efforts for communications hardware subsystems for satellite ground station applications. You may also expand into technical program lead engineering or functional engineering management.

Requires a BSEE or equivalent and 10+ years' experience in hardware and systems design of communications subsystems. Specific skills include supporting system-level link analysis, allocating system-level specifications to hardware architectures, analog and digital interfaces and associated critical parameters.

View our home page on the world wide web: www.lmwdl.com. Then send your resume, indicating position of interest, to: Lockheed Martin Western Development Laboratories, Professional Staffing COEE8/97, P.O. Box 49041, 3200 Zanker Road, San Jose, CA 95161-9041. FAX: (408) 473-4062. E-Mail: jobs@wdl.lmco.com.

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Project Engineer

Apply your skills in technical management elements of software projects where accountability includes budget, manpower, scheduling and material. Responsibilities include providing technical leadership in the resolution of complex technical problems in a team environment and also ensuring that project specific performance variables like manpower and material utilization are appropriately optimized. Requirements include proficiency with C, C++, Ada, 5-7 years experience. BSEE, BSCS, MS preferred.

Software Developers

Design and implementation of real-time embedded software systems using C, C++ and Ada. BSCS, BSEE and 3-10 years experience.

Systems Engineers

Perform systems analysis, design, fabrication, integration and testing of complex IR countermeasures systems. IR modeling, simulation, signal processing desirable. BS/MS in Optics/Physics a must.

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Design and direct the integration of complex IR countermeasure systems in laboratory, field and flight test environments. Design integrated test and analysis products for support of system test and evaluation.

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Electro-Optical Engineers

Apply your experience in the integration of laser IR lamp based and/or laser systems, IR focal plan arrays and digital data interfaces and servo control. BS/MS in EE/Optics required and a working knowledge of data collection, processing, analysis and programming skills with C, C++, Ada desirable.

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Engineering Shortages Still High In The Electronics Industry

QUALIFIED ENGINEERING TALENT IS STILL AT A PREMIUM FOR DSP, RF/MICROWAVE, SEMICON, SOFTWARE, AND TEST COMPANIES.

Robert Keenan

T

he lines have been drawn. The bidding wars have started. Now, companies are meeting face-to-face on the battlefield.

From the sounds of this scenario, you may think that companies are going head-to-head for market share. Or maybe they are fighting it out to see which technology will dominate and change the face of the engineering market. Although those interpretations are accurate, one scenario is missing—the hunt for qualified engineers.

Electronic devices are finding their way into more homes, with more people depending on tools such as the Internet and the cellular phone. This penetration and acceptance has sparked rapid growth in the engineering industry. And with rapid growth comes increased job openings. But the problem is that there aren't enough engineers in today's market to fill the positions that companies have open. As a result, today's engineers are asking for and receiving higher salaries than in the past.

This can be best illustrated in the 1997 *Salary and Fringe Benefit Study* distributed by the Washington, D.C.-based U.S. Activities Division of the IEEE. The study claims that the primary incomes—including base salaries, net earnings, commissions, and bonuses—of engineers has increased 7.5% over the past two years, while the Consumer Price Index has only increased 5.8% (Fig. 1). This equates to an increase in median (or midpoint) salary from \$67,000 in 1995 to \$72,000 in 1997 (Fig. 2).

In addition, one out of every six engineers surveyed received stock options during 1996. For those who received these options, their average estimated present value was \$7100, with a few members reporting options valued at \$100,000 or better. As the numbers show, the qualified engineer is the hottest product on the market. As a result, they are in the driver's seat during the recruiting process.

The electronic industry is broken down into many market segments—digital-signal-processor (DSP), RF/microwave, semiconductor, software, microprocessor/microcontroller, and test and measurement markets make up a few of these segments. In these markets, the search for qualified talent is an overriding theme. The only difference is in their hiring needs.

DSP'S VIEW

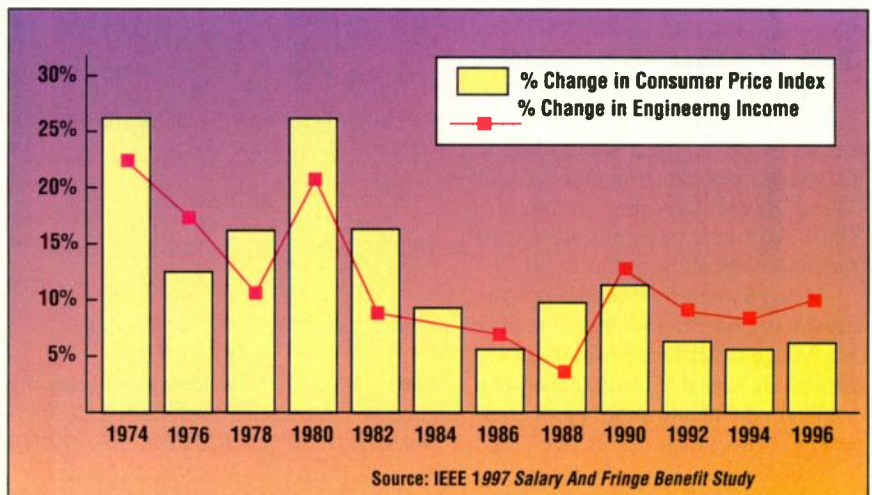
"DSP engineers are hard to get and hard to keep," says Barry Jinks, president

and CEO of Spectrum Signal Processing Inc., Burnaby, British Columbia, Canada. "Everyone is recruiting DSP engineers all of the time."

Jinks says that the reason that DSP talent is so difficult to find is that DSP systems are difficult to design. DSPs involve multilayer hardware/software schemes, making them challenging to design. "The road is littered with those who have failed to design with DSPs effectively," says Jinks.

Tom Willey, vice president of Zilog Inc., Campbell, Calif., agrees. Zilog received many resumes for a DSP job posting. But, according to Willey, only a few of those that responded are qualified candidates.

John Beck, DSP design engineering manager for Analog Devices Inc., Norwood, Mass., claims that the shortage is caused by two factors. The first is the rapid deployment of DSP technology. Beck says that this has forced companies to seek engineers with a new level of expertise. The second factor is the growth of the DSP industry as a whole. To meet growing needs, companies have refocused recruiting efforts. Beck says that Analog Devices has focused on DSP hotbeds such as Austin, Texas and Israel, to land recruits.



1. Over the past two years, engineering salary increases have outpaced the Consumer Price Index.

Roger Coker, staffing manager for Texas Instruments (TI), Dallas, takes a slightly different approach about the hiring trends in the DSP industry. He disagrees with people who feel there is a shortage of qualified DSP engineers. On the contrary, Coker says, "Instead of a shortage, there is just a tremendous demand for that talent." In fact, he says that every time a new technology or new product hits the market that includes a DSP, TI has to increase its engineering staff.

When seeking engineers, DSP companies seek a variety of skills. For example, DSP Software Engineering Inc. (DSPSE), Bedford, Mass., seeks engineers with good theoretical signal-processing skills as well as knowledge of communication theory, linear-system theory, and stochastic mathematics. In addition, the company wants practical skills. John Dellamorte, vice president of engineering, says that DSPSE looks for engineers that can debug and solve problems. He says that the company also needs engineers who can quickly research and stay on top of changing industry trends and standards.

Graychip Inc., Palo Alto, Calif., looks for engineers with strong analytical skills. Joe Gray, president, says that the company needs engineers that can analyze problems and determine the trade-offs needed to solve those problems. TI looks for designers with a strong understanding of systems and chips. According to Coker, a marriage between these two backgrounds works best for TI.

THE SOFTWARE DILEMMA

Arguably the most difficult technical talent to find in the market today is the software engineer. According to Laurie Harper, staffing manager for Wind River Systems, Alameda, Calif., software openings are one of the most difficult positions to fill.

Mike Burgher, executive vice president and chief technical officer for Microware, Des Moines, Iowa, agrees. He says that he has never seen such a demand and shortage of engineers throughout his entire adult working career. To explain, Burgher quotes a study which says that 250 million new software positions have been added in the electronics indus-

try. "It is as crazy as I have ever seen it."

"Finding qualified people has been a challenge," says Jane Helfen, staffing manager for several of Hewlett-Packard Co.'s (HP), Santa Rosa, Calif., divisions. Compared to a year ago, she says that it takes longer to fill a software engineering position.

When looking to fill positions, HP seeks engineers with a computer science/electrical engineering background along with an understanding of C and C++ programming, object-oriented design for windows and UNIX systems,

user interface and graphical-user interface design, and embedded systems software design. In addition, Helfen says that the company looks for candidates with communications systems knowledge as well as a fundamental understanding of RF and microwave technology.

At Wind River Systems, the focus is on engineers with real-time embedded programming backgrounds. However, Harper says that the company also needs engineers with operating system (OS) and networking (asynchronous transfer mode (ATM), TCP/IP, etc.) experience.

Microware, along with other software companies, looks at college students that have taken compiler and OS classes. Although this course background is important, it is not the only deciding factor for Microware. In fact, Burgher says, "We are looking for young engineers that are fired up, bright, and team players." If the engineer has these capabilities, he says that Microware can teach and mold the engineers.

No matter what skills or experience companies look for from software engineers, one thing remains true: It is a buyer's market. To land a software engineer, companies must first offer a competitive salary. But companies also must provide signing bonuses and a challenging work environment to land a top-notch software engineer.


RF CHALLENGES

Pushed by continued growth in the wireless industry, the hunt for RF engineers is still on the minds of many companies. One of the prime needs for these companies is for applications engineers. Mark Burkett, vice president of engineering for California Eastern Laboratories (CEL), Santa Clara, Calif., says that applications engineers must help customers effectively use products. As a result, he says that these engineers must have good communications skills as well as an understanding of the real issues that are shaping the wireless design market.

Companies also are on the prowl for qualified design engineers. Burkett says that CEL needs designers that have experience with integrated circuit (IC) design, power transistor design, and silicon and gallium ar-


MEDIAN SALARY CHANGE 1995-1997

CIRCUITS AND DEVICES

1995  \$70,000

1997  \$75,000

INDUSTRIAL APPLICATIONS

1995  \$60,850

1997  \$66,000

COMMUNICATIONS TECHNOLOGY

1995  \$70,715

1997  \$75,000

ELECTROMAGNETICS AND RADIATION

1995  \$65,718

1997  \$78,000

COMPUTERS

1995  \$64,400

1997  \$71,000

ENGINEERING AND HUMAN ENVIRONMENT

1995  \$76,000

1997  \$82,078

ENGINEERING AND POWER ENGINEERING

1995  \$65,000

1997  \$67,000

SIGNALS AND APPLICATIONS

1995  \$72,000

1997  \$76,000

Source: IEEE 1995 and 1997 Salary And Fringe Benefit Study
ILLUSTRATION BY CHERYL GLOSS

2. Numbers from studies run by the U.S. Activities Division of the IEEE show an increase in median (or midpoint) salary for engineers across several disciplines.

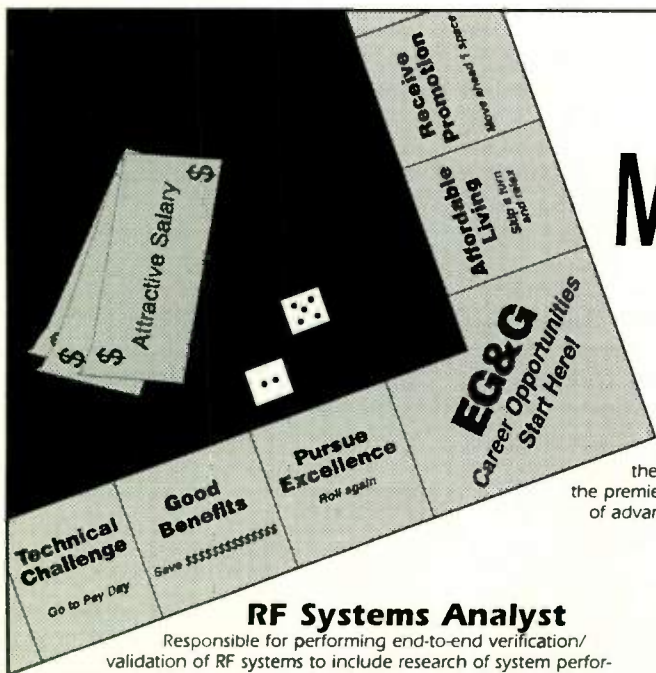
senior (GaAs) experience.

Nance Cohen, technical recruiter and owner of the technical recruiting firm Cohen Associates, Calabassas, Calif., agrees. She says that companies need engineers with 5 to 7 years experience in

bipolar IC design as well as engineers with a strong understanding of silicon and GaAs technologies.

There is no question that the need for application and design engineers is high in the RF and microwave market. But the

real catch is the system-level engineer. "The need for system-level engineers is very heavy right now," says Ben Garfinkle, president of MetroVantage, a technical recruiting firm located in Laguna Niguel, Calif.



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RF Systems Analyst

Responsible for performing end-to-end verification/validation of RF systems to include research of system performance criteria, preparation of test planning, directing/conducting tests, test analysis and report preparation. Additionally, the selected individual will develop instrumentation criteria to evaluate test objectives. Requirements include a BSEE or related electronic program degree with 3 or more years of experience directly related to radar system evaluation.

Senior Engineer

Firmware/Software

Responsible for the design, development, coding and testing of firmware/software for embedded processors in radar systems including the specification of commercial hardware and/or custom digital hardware for VME bus systems. Requirements include a BSEE and a minimum of 4 years experience in firmware/software development for embedded real-time systems using C/C++, multitasking operating systems (VRTX, pSOS, VxWorks), Unix based software development, and digital hardware design.

Engineering Technologist

PWB Design

Responsible for the analysis and design of electronic packaging and pilot production management, including mechanical and PWB design and documentation, fabrication coordination, and the development of the product structure breakdown for efficient production. Requirements include 6-8 years of experience working at an engineering level involved in solving R&D, manufacturing software, electronic packaging, analysis and design problems. Experience in radar and RF theory and concepts a plus.

Software Engineer

Responsible for developing software for project control and information technology applications. Duties will include system/software requirement specification, analysis, design, implementation, testing, documentation and maintenance in a disciplined software engineering environment. Requirements include a BSCS or equivalent and experience with Windows NT, Visual Basic, SQL, MS Project, MS Access, MS Office/VBA and OLE/COM. Experience with OOA/D; client-server, N-tier and distributed architectures; C++, Ada95, Delphi, GUI design, ODBC, MS SQL Server and Oracle highly desirable.

Engineers

Microprocessor Hardware/Software

Responsible for designing, coding, testing, documenting and implementing real-time microprocessor hardware and software for data instrumentation systems. Requirements include a BSEE or BSCE and a minimum of 3 years experience in microprocessor systems design and integration.

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CAREER OPPORTUNITIES

At the system level, companies are looking for engineers with an understanding of RF communications theory. But, the best candidates, according to Garfinkle, combine this RF theory with an understanding of wireless air-interface standards such as time-division multiple access (TDMA) and code-division multiple access (CDMA).

The search for qualified RF system-level engineers is so difficult that five wireless companies (AT&T Wireless, Ericsson, Lucent Technologies, Motorola, and AirTouch Cellular) and several universities have banded together to form the Global Wireless Education Consortium (GWEC), located in Mankato, Minn.

The goal of the GWEC, according to Executive Director Misty Baker, is to increase the quality and quantity of RF engineers and technicians. To do this, companies and institutions must work together to set up wireless programs.

These programs will provide students with basic RF training while offering engineers an introduction and overview of the wireless industry and the technologies that are shaping this market. "Engineers will at least know the difference between TDMA and CDMA," says Baker.

The GWEC programs will combine course work with internship programs. According to Baker, the internship is a driving force behind the program. The benefit is that students get hands-on experience in wireless technology while providing sponsor companies with a look at how well a young engineer will perform in a work environment.

"GWEC is a true collaboration," Baker says. Industry companies and education institutions are coming to the table to share and jointly develop resources to train young engineers.

TESTING THE WATERS

For any electronic, microwave, or wireless product to work, companies must first go through extensive test and measurement phases. As a result, test and measurement companies also have experienced rapid growth. And with business growth comes internal growth, leading to the increase of engineering staffs.

The challenge for test and measurement companies, according to John Gates, technical recruiter for Tektronix's, Beaverton, Ore., Measurement Business Division, is that they are competing for the same engineers as their customers. For example, he says that when Tektronix develops a system to test cellular handsets, that system requires expertise in how the cellular phone works. To effectively develop the test system, Tektronix must hire engineers that have a system-level understanding of the product. "We must have engineers capable of building those products." As a result, Gates says that these companies also compete for the same engineers as their customers.

But the same is true for the customers. When developing any product, engineering companies need quality engineers to evaluate the product's performance. As a result, the test and measurement industry's customers need qualified test

engineers on staff who can perform these crucial evaluations.

"The test engineer is crucial to finding out and solving problems," says Ray

GWEC programs forms to increase RF engineering and technician talent.

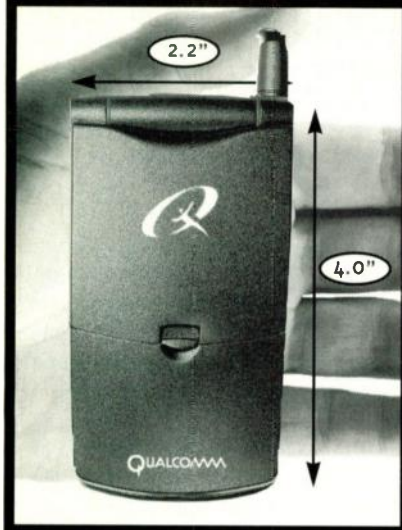
Evans, human resources supervisor for Wiltron, Morgan Hill, Calif. "Everybody is competing for high-quality test engineers." This competition, he says, has made it difficult for test and measurement companies to find engineers.

When looking at recruits, companies in the test and measurement industry have varying needs. However, the need for software expertise generally ranks at the top of many companies' lists. "Overall, we [Tektronix] are looking for a lot more software engineers than we used to," says Gates.

When looking for software engineers, Ron Brazee, human resources specialist for HP's Test and Measurement Division, Spokane, Wash., says that he seeks both college and experienced engineers. For college grads, the company looks for C or C++ experience and a UNIX background. For experienced engineers, Brazee says that the company looks for 3 to 5 years experience. But the real experienced engineer catch, according to Brazee, is the software engineer with an

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RF Subscriber Engineers

We are looking for RF Subscriber Engineers at all experience levels to help design QUALCOMM's expanding CDMA subscriber product line in both cellular and PCS bands. You will be involved from product conception to high-volume manufacturing. Responsibilities include all aspects of subscriber transceiver design: RF system analysis, RX/TX chain analysis, circuit level design, component and RF ASIC specification and evaluation. BSEE required; MSEE preferred. Experience in handset design, RF CAD, and design for high-volume manufacturing a plus.

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CAREER OPPORTUNITIES

RF or wireless background.

Toni Piwonka-Corle, program manager, says that Tektronix's Wireless Product Line needs embedded software engineers with experience in writing drivers and with real-time operating systems. This sector also looks for software candidates with an understanding of signaling and communication protocols, such as CDMA, as well as some hardware background. Piwonka-Corle says that a hardware background provides a broader understanding of how their entire system works.

Despite a surge in the need for software people, test and measurement companies still need hardware engineers. David Tarver, president of Telecom Analysis Systems (TAS), Eatontown, N.J., says that his company looks for engineers with experience with RF, digital, and analog hardware.

Tektronix also is on the hunt for quality hardware talent. Gates says that Tektronix is looking for a lot of RF people as well as technical talent that can design and develop components, such as receivers and synthesizers.

SEMICONDUCTORS

When searching for engineering talent, the semiconductor industry is no different than the DSP, RF/microwave, software, and test and measurement markets. Demand for engineering talent is at a premium.

In fact, Mike Jones, vice president of human resources and information services for Microchip, Chandler, Ariz., says that the semiconductor industry reached full employment two years ago. As a result, he says that finding any engineer in the semiconductor industry is a difficult task.

"We need more engineers than we can find," says Jeremy Bunting, strategic marketing manager for Vitesse Semiconductor, Camarillo, Calif. "It is harder to find technical talent than it was two or three years ago."

And, the need for engineers in this segment of the market does not seem to be slowing down. "I believe that the need for engineers will still be high two years from now," says Bryan Flake, human re-

Semiconductor companies need more engineers than they can find.

sources manager for American Microsystems, Inc. (AMI), Pocatello, Idaho. When evaluating their hiring practices, semiconductor companies look for two different types of

engineers: Design and process.

For example, AMI has a strong need for design engineers. Anita Rotert, human resources manager, says that AMI is actively seeking engineers with semiconductor experience, a digital or analog background, and project management skills.

Vitesse also is searching for design talent. Bunting says that Vitesse needs engineers that are experienced in high-bandwidth circuit design and also in the design of digital communication ICs that can run over 1 Gbit/s.

AMI's Flake says that it has always been difficult to fill design engineer openings. But, now with the building of new fabrication centers and the rapidly rising movement to new processes, it is getting equally as tough to fill the process side. He says that as more fabrication facilities are constructed, the supply of engineers is stretched that much thinner.

One method of improving the pool of process talent is to work with local universities. ANADIGICS, Warren, N.J., is sponsoring a course at Somerset Technical Institute, Bridgewater, N.J., to train students in the wafer-fabrication process. Andrea Foster, director of human resources, says that the goal is to increase the company's recruiting pool.

AMI also is working with local colleges and universities to improve their process engineering talent. The primary goal is to have these institutions teaching process skills that will be needed two years down the road and beyond. Flake says that the company wants these schools to teach students skills that AMI and other semiconductor companies will need in the future.

Robert Keenan is an associate editor at Wireless Systems Design magazine. He can be reached at 611 Route 46 West, Hasbrouck Heights, NJ 07604; (201) 393-6250; fax (201) 393-6297; e-mail: robkwsd@aol.com.

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Senior RF/Antenna Design Engineer

Requires BSEE/MSEE with 5 or more years of antenna and/or RF circuit design experience. Responsible for modeling development, fabrication, and testing of antenna elements, beamforming networks, and arrays, as well as RF circuit design of antenna system components.

Senior RF/Antenna Design Engineer

Requires MS with emphasis on electromagnetic engineering and 5 or more years experience in the design of integrated FSS and RAS technology into antenna systems over the microwave spectrum. Responsible for the design fabrication and test of low observable antennas and structures.

Senior RF/Microwave Design Engineer

Requires a BSEE with 3 or more years hands-on experience developing RF/microwave active and passive circuits. Responsible for RF/microwave circuit design and analysis for developing active and passive circuits for a wide variety of commercial and military antenna systems. Previous experience designing LNAs, HPAs, filters and switch networks with emphasis in the use of linear/non-linear and EM simulators is highly desired.

Senior Analog/Digital Circuit Design Engineer

Requires a BSEE or equivalent with 8 or more years applicable experience. Will perform highly complex engineering tasks which may include applications, electrical, electronics, software, and mechanical using advanced, innovative and original techniques and principles. Will also design, debug and test space-based controller electronics that interface with customer control and status monitoring systems, and customer-designed RF receive modules; select and specify the required power supplies and the associated signal and power distribution cable harnesses. Designs will incorporate the use of state machines, microprocessors, programmable gate arrays, digital circuits, and/or analog circuits at a minimum. Experience with programmable gate arrays and software programming are highly desired.

RF Design Engineer I

Requires BSEE with 3 or more years of experience. Required skills include the use of computer-based tools for analysis and layout, operation of RF test equipment, and the ability to do bench level construction and/or modifications of hardware. Responsible for the design, layout, analysis, and testing of RF components and antennas over primarily the UHF and microwave frequency range.

Antenna Test Engineer

Requires a BSEE and 2 or more years experience in RF and microwave testing. Responsible for preparing test procedures and coordinating electrical and environmental testing of advanced antenna systems. This includes but is not limited to qualification tests in accordance with MIL-STD-810, environmental stress screening and acceptance tests. Must demonstrate working knowledge of RF test equipment including network analyzers, spectrum analyzers, antenna range and RF test equipment.

Antenna Marketing Manager

Requires BSEE/MSEE with 8 or more years electromagnetic engineering experience with emphasis on Electromagnetic Radiation (antennas) Phenomenon. Responsible for supporting New Business Development and marketing of advanced antenna technology and subsystems. Experience in developing and fielding complex antenna subsystems for both military and commercial customers, ability to apply the Ball advanced antenna and RCS technologies on a real time basis at potential customer facilities, and ability to develop innovative and practical solutions to complex system requirements in a team atmosphere are required. Must be business oriented to initiate and aid development of practical products in challenging markets. Extensive travel required.

Senior EMI/EMC Engineer

Requires BSEE Degree with 8 or more years experience in EMI/EMC analysis with RF circuit design capability. Systems level experience a plus.

RF Technician

Requires an Associate's Degree in EET with 2 or more years electronics experience, a strong mechanical aptitude, and knowledge of soldering techniques and Smith Chart applications. Must have experience testing antenna patterns and be computer literate in MS Office 95 and Windows 95. Familiarity with antennas, wave propagation, anechoic chambers, network analyzers, and HAM radio is desirable. As an RF Technician in the advanced antenna and video systems organization, work will include designing, fabricating and testing state of the art antenna systems for all types of military vehicles, NASA missions, and military weapons systems.

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The Winning Formula: It's Not Unusual That Dilbert Is In A Meeting

“LET’S TAKE A MEETING” OFFERS OPPORTUNITIES TO GET COGENT POINTS ACROSS TO THE RIGHT PEOPLE IN THE RIGHT SETTING.

Paul McGoldrick

If there was ever a topic that really makes the majority of us groan, it is meetings. Whether it is too many, too long, useless, nonproductive, or negative, we all have strong opinions of the meetings that take place in our companies. In the spirit of this “Winning Formula” column, we must try to understand meetings and how to make them useful and productive events, rather than destructive of our time and energy.

The entire culture of a company seems to be determined by the sorts of meetings that take place and the way they are used to make decisions, to implement decisions, or just to give the appearance of offering some kind of democratic or quasi-democratic process. You are either in a position to be the person calling various meetings, or you are a participant, or you are both. Often when you are just the attendee, you may feel that you are limited in your ability to actually make a meeting positive. But there are things that you can do to push things in a direction that others will quickly pick up on, agree with, and help with.

By far the most important decision that you must make if you control meetings is whether the thing is needed at all! It is an obvious but critically important up-step. A meeting that is unnecessary is never going to be a happy one, and will sour all future efforts. There are some basic rules to decide the necessity of calling

a physical, around-the-table, or teleconference meeting:

1. There should be at least three people who have a need to share the same information, or need to agree a decision at the same time.
2. There is a need to get feedback that might not be forthcoming in an e-mail exchange or a reporting system on paper.
3. There is a need to read the body language of the attendees.

The latter is one of the reasons that teleconferences fail; because of time latency in the systems, coupled with a less-than-perfect picture quality, it is often difficult to read the response of the people at the other end of the call.

TYPES OF MEETINGS

It is said that there is no new plot pos-

sible for a story; all of them have been told and re-told so that the modern author can only reinvent a plot with a new environment to it. The same can be said of meetings. There are three basic types of meetings with a myriad of variations on those types. Those three are planning, review, and postmortem. The planning meeting looks forward at a task, project, road plan, department direction, or company future depending on the level of the meeting. The review meeting looks at the ongoing situation, and the postmortem looks backwards at what has been, happened, or done. It is my contention that mixing these directions in the same meeting will not give the results that the organizer thought.

Within each category of meeting there are various degrees of intensity and depth of discussion. If you take, as an example, a review meeting of a design for a new part: There will be the in-depth meeting of the design team itself, with leader and, maybe, someone even more senior in the engineering group at the company. There also might be a design review with far less depth, involving the marketing people, giving them an understanding of the product features

that have/have not been achieved, other hooks that have been left in the product, costs, time factors, and so on. These would be entirely different sessions and absolutely must not be mixed up with one another. A third type of review meeting might take place when the principal customer for the part needs to understand more than the marketing people, but less than the design team. It might be led by marketing, rather than engineering, and the agenda may have political connotations that may not be understood by everyone.

It is important to realize what sort of meeting you are involved in and, like the servants of Victorian England, “know your place.” But we all have to hold



ILLUSTRATION BY:
CHERYL GLCSS

our tongue at the right moment, even if it is incredibly difficult because of our nature. If a meeting is with a customer, for example, you absolutely have to take your lead from the marketing or sales people present. It is your product, but it is their customer. For most, the customer is on a need-to-know level, unless you are specifically told otherwise. It would be different in a meeting with just fellow employees, even from different departments. It is not a matter of taking the opportunity to be some kind of whistleblower on someone else; it is a matter of allowing the company integrity to remain whole by making sure all of your concerns are laid out and discussed.

THE POSITIVES, AND OTHERWISE

Great things really can come out of meetings; they can be positive, productive events where decisions can be made at a rate that is far faster than any other means. They can be informative, with everyone equally briefed in the same fo-

TABLE 1	
THE POSITIVES OF MEETINGS	THE NEGATIVES OF MEETINGS
Productive	Time-wasting
Informative	Ego slapping
Supportive	Personal vendettas
Synergistic	Inappropriate subjects
Educational	Too long
Avoiding duplications	Wrong timing
Multihueded thinking	Badly led
Freeform discussion	Wrong attendees
Real questions possible	Too much consensus

rum. Understandings of the situation should be the same in each of the attendee's minds. They can allow for enormous amounts of support to be given to those areas and individuals that clearly need them. They can be synergistic, both within the same department and between departments, cross-pollinating information and views. They can be educational, they can avoid duplicated effort, and

they can allow many heads to get together and really throw out information and ideas in a freeform manner. Best of all, meetings allow you to hear peoples' true views, and will allow them to ask questions that might not ordinarily be welcomed in one-on-one discussions.

On the other hand, a badly-organized meeting can be thoroughly negative and a total waste of time for all participants.

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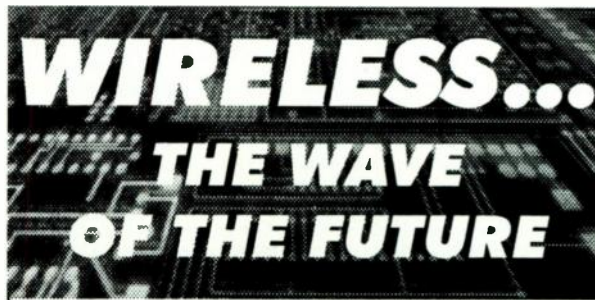
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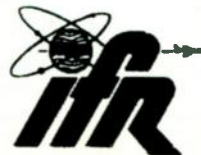
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Typical of the things that can go wrong are personal vendettas surfacing at the table, or when someone seems to be determined to slap the ego or credibility of someone else. And surely, none of us have been at meetings that meander

hopelessly off the subject and become entirely inappropriate in the discussions? Then the time allotted becomes ignored and things get even worse. Most such meetings are simply just badly led or they have the wrong participants, but

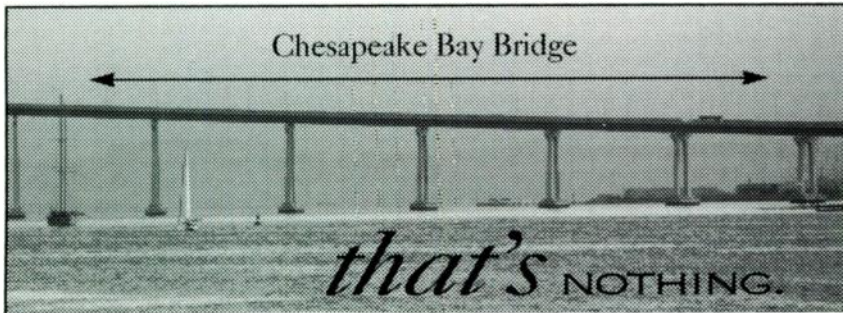
there also are those where the meeting has been scheduled at such an awkward time or place that some of the people just want to get back at anybody they can.

The worst meetings are those where there is too much consensus between parties. The sort of meeting where everyone seems to love anyone else, and because you can't criticize in those circumstances, absolutely nothing gets done.

RUNNING THE MEETING

With real estate it is location, location, location; with meetings, the most important things are agenda, agenda, agenda. If there is no agenda, don't have the meeting. If you're running the meeting put out an agenda at least 48 hours before; if it can be done earlier and is open to additions from others, that is even better. Make sure that the people you invite for the meeting are relevant to the tasks and planning that is to be undertaken. Don't miss out people either; apart from ignoring a section of views that could be relevant, you will create concern in them about their position in the company, their futures, etc. It is surprising how many managers don't realize, or forget, that their employees really care about what goes on in the company.

Start the meeting on time; if people are late, then that is their problem, not of the others who have made it on time. Holding up a meeting for one latecomer does not make sense to busy people. Once you get into the agenda, stick with it; don't allow anybody to go off on a tangent to something somewhere else. You may have your boss there who loves doing that—find a way to get past him/her back to the agenda. The worst deviations



Chesapeake Bay Bridge

that's NOTHING.

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Hardware Engineers

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- RF Systems Engineers
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- DSP Engineers
- IC Design Engineers
- Mechanical Engineers
- Technical Hardware Managers
- Components Engineers
- TDMA/CDMA/GSM Professionals
- VLSI Engineers
- Digital Designers/FPGA/DSP

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- Software Engineers (Windows)
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- Technical Hardware Managers

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- Lotus Notes Developers
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- Wireless Infrastructure Products
- Program Managers

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TABLE 2

Running A Meeting

- Agenda, agenda, agenda
- Keep to it
- Allow no personal stuff
- Take no disciplinary action
- Keep decent notes
- Send Minutes out right away
- Spell out action items
- Review all action items
- Allow "any other business" -- within limits
- Set a duration
- Keep to it
- Convenient time and place
- No re-runs on decisions
- No dictatorships
- Traffic cop OK

CAREER OPPORTUNITIES

are caused by fellows of the company coming in with enthusiastic but mistaken stuff that can cause chaos. Don't allow personal material to come up. If it is obvious someone is having a spat with someone else and wants to bring it to the table, shut them up. If they won't be well-behaved, treat them like the children they are and make them take a time-out.

Of the really awful things that I have seen happen at meetings, one of the worst was to be present when a person actually got fired! It was totally unexpected, an explosion from a company president when things clearly weren't going toward the decision he wanted. There is a place for disciplinary action and it is not at a meeting with another dozen people present. We haven't had public executions for some time and most civilized people would not care to be at them.

Keep decent notes at the meeting and have someone else take the minutes so you can concentrate on getting an efficient conversation going in the shortest time. The meeting minutes should be prepared and distributed within 24 hours while everything is still fresh in the attendees' memories. Spell out clearly the action items agreed and the WHO and the WHEN they are required. Anybody who is actioned in this way should be required to confirm back to you that the item is correct. It doesn't matter how trivial the item is, get people into the habit. The review of action items should be the first item on the agenda of the next meeting.

When any other business is raised at the end of the meeting, do your best to get it shelved until the next meeting, confirming that it will be an agenda item. If it positively has to be dealt with, then do so as quickly as possible. If it needs follow-up outside the meeting, then try and get it switched to a one-on-one thing with, if necessary, a report back to the next meeting. It should be major exception to policy that a meeting runs over time and you should do everything possible to avoid it happening. Listen to the attendees if any say that the meeting time or place is bad for them for the future. In general, morning meetings — not too early! — are the most productive. Meetings after lunch are usually the worst for producing tangible results.

One of the most critical things to prevent at meetings is the inevitable attempt to rehash decisions. Unless there have been major changes in circumstances, there are few occasions when a group's



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You will analyze, design, simulate and characterize Si Bipolar/BiCMOS/GaAs RFICs, working in multi-disciplinary team environment using an integrated product development approach. Requires eight or more years' experience in RFICs; previous design of 900 MHz and 2 GHz up/down converters, IF amplifiers, LNAs, mixers and AGC amplifiers for CDMA, AMPS, PCS applications. BSEE or MSEE preferred. Code: 345-96

RF SYSTEMS ENGINEERS

You will analyze, design, develop and simulate RF systems architecture (DC to 2 GHz) for next generation of cellular phones, working in multi-disciplinary team environment using integrated product development approach. Requires a minimum of seven years' experience in RF communication systems. BSEE or MSEE preferred. Code: 400-97

RF TRANSMITTER DESIGN ENGINEER

You will analyze, design, simulate and characterize RF transmitter systems up to 2 GHz, working in multi-disciplinary team environment using integrated product development approach. Requires three or more years' experience in RF communication systems; experience with power amplifiers, filters, gain control and modulators. BSEE or MSEE preferred. Code: 401-97

RF SYNTHESIZER DESIGN/PLL ENGINEER

You will design, simulate and characterize frequency synthesizers to 2 GHz, working in multi-disciplinary team environment using integrated product development approach. Requires at least three years' experience in RF communication systems; experience with VCO, frequency dividers, phase comparators and filter designs. BSEE or MSEE preferred. Code: 403-97

RF ENGINEERS

You will design RF circuitry, requiring demonstrated knowledge of amplifiers, oscillators, mixers, filters, dynamic range, impedance matching, noise and distortion. Requires at least two years' experience in RF communication systems. BSEE preferred. Code: 371-96

RFIC TEST ENGINEER

You will design automatic test fixtures and software for R&D testing of RFIC devices ranging from 800 MHz to 2000 MHz. Requires BSEE and two plus years' ATE experience. Programming experience with HP VEE or LabVIEW desirable. Code: 403-97

RF TEST ENGINEER

You will develop automated test software and procedures for RF/analog circuits. Experience using cellular test equipment, GPIB (HP VEE/LabVIEW) programming and CDMA/AMPS knowledge a plus. Will consider highly motivated entry-level RF Engineers with BSEE. Code: 404-97

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choices should be revisited. There are even fewer times when the tales of events past should be raised at a meeting as an example of what, or what not, to do in the future. Things change in our industry at a fast-enough pace that the past is an interesting discussion for another venue.

JUST AN ATTENDEE

No one should think of themselves as just attending a meeting; you must think of yourself as a full-time participant with your own important views. You must be willing to speak out without waiting for a direct invitation. Being proactive in this way is not seen, generally, as being a negative.. But when you do speak out, be rational, to-the-point, and accurate. When you make points, do so as suggestions, not as a law that will be broken over your dead body; you just might be inviting that to happen. If you feel that the discussion is getting lost, bring it back by saying something that you know is agreeable to most and is directly relevant to the topic. You can't take over the meeting, but you will be reminding the chair about what is what. Don't get upset and don't get personal.

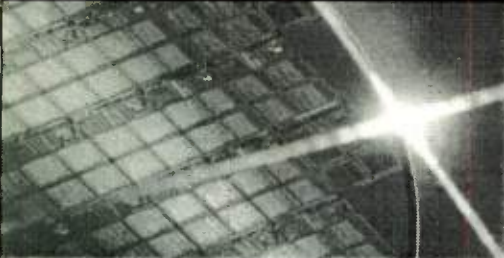
Do your homework on the agenda so that you know where you will be called on to offer an update, a report, a suggested direction, or even where you might want to volunteer. Bring materials with you that are relevant. Do not assume that the meeting can be disturbed for phone messages; turn off your pager, your phone, and your beeping watch.

In your areas of relevance keep good notes, and ensure that when you get the minutes, your action items will be in general agreement with the official views. If you feel that you shouldn't be at that particular meeting, then talk to the chair outside of the room afterwards. And a last word to senior people, those more senior than nearly all, or even all, of the participants: Be on time, keep quiet, appreciate the professionalism of your more junior colleagues, and if something needs to be addressed, do it afterwards through the proper channels.

Meetings can be positive and productive, but everybody has to work to get the results that everyone wants.

Paul McGoldrick is Analog Editor at Electronic Design. He can be contacted at ED's San Jose office at (408) 441-0550, X 113, or by e-mail at PMcGoldrick@compuserve.com.

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will develop new CAD methodologies that significantly improve design productivity and support our entire suite of engineering tools; develop tools and capability not available from third party vendors; train new engineers; evaluate and select new CAE tools. Requires BS/MS and a minimum of 5 years experience in CAE tool support/development. Must be able to program in C or any of the UNIX shell languages. Experience with Cadence and/or Synopsys tools is an advantage. Job Code: FET

CAE Back End Tool Specialist

will develop IC layout methodologies to reduce time to market and increase productivity. You will be responsible for all back end tools including: Place & Route Root methodologies, cell compilers, device level place & route tools for our sub-micron technologies. Knowledge of hierarchical verification techniques is a plus. Programming experience in C or and Shell programming is desirable. Knowledge of C, or Shell programming is a plus. Job Code: BET

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Hot Job Spots Report Increase In Openings

OPPORTUNITIES ABOUND FOR ENGINEERS WHO MAY BE LOOKING TO RELOCATE ELSEWHERE.

Patricia L. Walker

It remains a very favorable market for those engineers with the skill sets to meet the communication industry's ferocious needs for product development.

Recruiters and staffing managers across the USA estimate that job openings for engineers in this sector have increased by about 20% over last year's number of openings.

This trend also is supported in the recent Management Recruiters International Inc. (MRI) survey for the second half of 1997. Its projected increases in

executive/managerial/professional hiring for the last half of 1997 (see related map) show that 2.9% more companies, or up to 52.5% of companies across the country, are planning to add new staff in the remainder of the year. Leading the surge is the telecommunications and information technology sectors, according to the MRI survey of 4900 executives.

"What is going on today in the entire information technology arena is not to be believed. It is a frenzied area with tens of thousands of unfilled positions," comments Alan R. Schonberg, president of MRI.

Recruiting firms polled by this publication also concur that the demand is nationwide, and the hot hiring spots that were there earlier this year still remain.

These include San Diego, Seattle, Dallas and Austin, Raleigh-Durham, and Silicon Valley. Other selected cities in the Southeast and Southwest and Mid-West also are actively seeking electronics engineers.

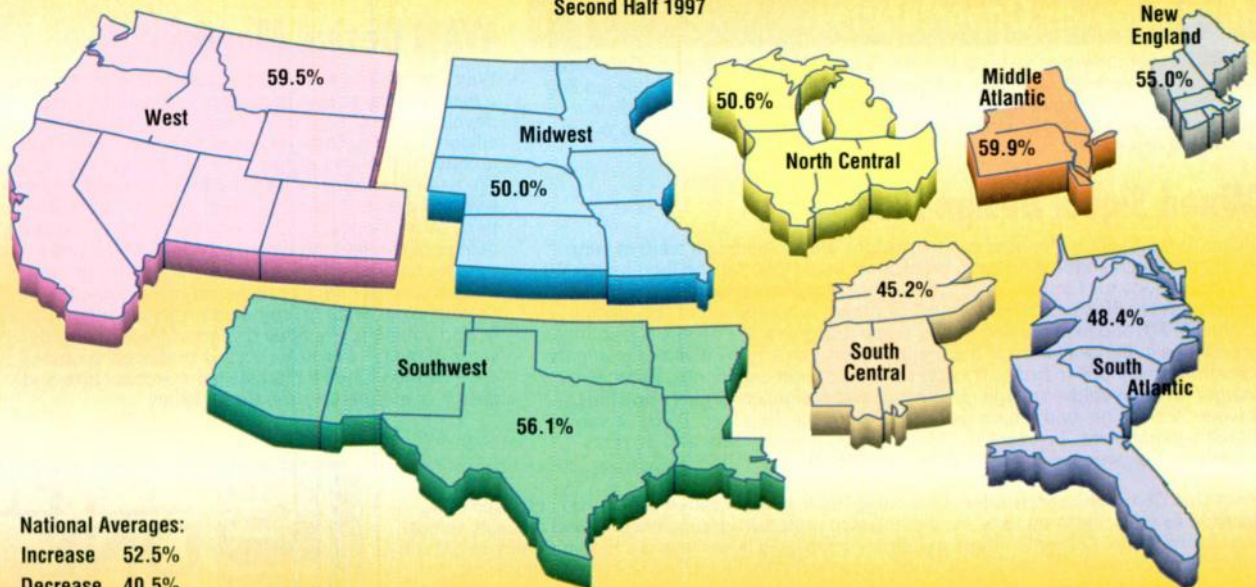
MID-ATLANTIC COMES ALIVE

A new area that has come alive recently has been the Mid-Atlantic states (Maryland, Virginia, Pennsylvania, and New Jersey) and the Northeast in general is picking up, notes Louis Schwartz, vice president of Technical Employment Consultants in Pennsylvania. Wireless opportunities are the strongest as well as openings for RF engineers. The demand is mostly for design engineers, but there also are some positions for manufacturing, he said.

The MRI survey confirms that the Mid-Atlantic region has showed the largest gain in all employment new hires over the first half of 1997. It is closely followed by the West.

On the East Coast, demands for wireless and PCS engineers are pushing the

**Projected Increases in Executive/Managerial/Professional Hiring
Second Half 1997**



National Averages:
 Increase 52.5%
 Decrease 40.5%
 Maintain 7.0%

Source: Survey conducted by Management Recruiters International, Inc.

market the hardest from small companies to large, David Hicks, senior recruiter for Micro Communications Executive Search in Massachusetts reports. Also competing close behind are demands for RF and test engineers.

He notes that although designers are in great demand at the moment, he expects that the demand for engineers in the manufacturing departments will return once projects now under design are put into production.

LARGE FIRM INFLUENCES

Opportunities in select cities like Chicago, Indianapolis, and Seattle are mainly defined by the individual large companies in these places and their needs at the moment.

In Florida, for example, Harris Corp.'s main need is for software engineers with computer science or electronic engineering degrees. The company has hired about 200 college graduates in the past 12 months, 70% of them to help fill its technical needs, according to Ron Hutt, senior manager in Human Resources. He expects the company will hire equally as many in the next 12 months. OKI Telecom reports that the Atlanta area has a strong demand for mostly software engineers and SAP consultants.

Meanwhile in Seattle, Allied Signal Corp. is on the lookout for engineers with specific backgrounds in silicon microstructure design and 5 to 10 years experience. The supply is very tight in the Northwest area, says Allied's Steve Darr, but this fluctuates with what is happening at Boeing.

Likewise, Hewlett-Packard's Wireless Infrastructure division in California is looking for engineers experienced in high linearity power amplifiers. New standards are creating a demand for this specialized field.

Then, there also is the impact of the recent merger of 3COM Corp. and U.S. Robotics Corp., creating the largest business in networking. Will they keep two operations in Chicago and the West Coast? recruiters ask. This could change the job situation in Chicago. The company has yet to reveal what it plans to do.

Typical of what is driving the frenzy for electronics engineers is the statement by the 3Com chairman Eric Benhamou at the announcement of the merger. "The next wave of growth in networking will be led by companies that offer faster access to the network, that build more intelligence into the network, and that lower the cost of network ownership."

SUNSHINE AREAS REMAIN THE HOTSPOTS

The sunshine areas continue to have a strong demand for communication industry engineers across the board, but many recruiters note that the decision by a qualified engineer to move to the area many times is challenged by a number of other factors.

As Lionel Eras president of AZTech Recruiting Co. in Arizona, points out, the San Diego demand is huge, but it is also not an easy area in which to relocate. Housing availability is tight and the cost of living is high. Unless companies are more willing to help the candidate make the move, they may not get him or her.

Eras also notes that making a move to a specific region is often a lifestyle or environment decision, such as those of environment and low-cost housing that attract EEs to Arizona, which continues to be one of the top 10 hot spots.

Hutt of Harris Corp. concurs that life-style often influences the decision. "We recruit mainly from the Southeast, Northeast



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HYUNDAI
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and Midwest," he says. The Florida lifestyle appeals to residents in these areas more than residents in California.

Sometimes an area needs a little publicity to attract the right candidates. The Dallas wireless firms, for example, have been running cooperative advertising and web pages about the Dallas area to attract the much desired-engineers to their area.

RECRUITING OUTSIDE THE U.S.

Some firms are starting to go outside the country to find the skill sets they need specifically in the wireless sector. Manny Rao, vice president for Recruiting Services Inc. in Ohio, notes. Recruiters report having successfully placed engineers from Canada. They are finding it easier because of the NAFTA agreement.

Richard Gorberg, senior recruiter for Fortune Personnel Consultants in North Carolina, sees firms starting to look overseas for VLSI engineers, considered

to be by many the tightest supply problem in the U.S. They are generally looking at Europe, India, and China, he says.

But, attracting an engineer from Europe will not be that easy, Eras points out. The quality of life and salaries are not that much different from the U.S., and the market for engineers there also is tight. He expects the U.K. would be the logical first place for a search for engineers, but he also notes that engineers in France, Germany, and Italy are interested in coming. It is a matter of offering the right motivation.

The demand in the software sector has been so great that some companies are setting up their own operations overseas to make use of the engineer pool in various countries. Others are contracting with foreign firms to handle some of the design overload.

DEMAND OUT TO THE YEAR 2000

Regardless of where the communication industry gets its qualified engineers,

one theme repeats throughout the employment campaign. The intense demand for engineers in the RF, wireless, VLSI, digital, circuit design, software and software systems is expected to continue out up to the year 2000.

There are so many projects, underway that the demand looks strong for the next 3 to 4 years, recruiters generally agree. And there is no exception that this trend will slowdown for the next few years. There will be some fallout, they caution, as companies rush to produce competitive products. Some of these projects or products will fall by the wayside, casualties of competition.

But in general, recruiters and staff managers alike see the volume of current projects underway and the continued push for more communication products. This will keep the demand for skilled engineers at high levels for the next three to four years, and possibly beyond that.

Pat Walker is a former Staff Director of the IEEE

Communications Sector

The implementation of new digital television and radio broadcast services has created great career opportunities at Harris Corporation's Broadcast Division, one of the world's largest producers of radio and television equipment. The following immediate opportunities are available:

These positions require a BSEE or related technical degree, advanced degree preferred.

RF Solid State Circuit and Power Amplifier Design Engineer

Challenging positions that call for driven, RF engineers with a minimum of 3-5 years' experience in the design of linear class A/AB and non-linear class C/D, RF Amplifiers, power dividers, combiners and control/monitor circuits for high power VHF/UHF applications. Must be experienced in Solid State amplifier design utilizing MOSFET's, and a champion of design for low cost, manufacturability and high reliability. Ideal candidate will have the skills to manage small projects as well as the capability of being a hands-on, individual contributor.

Sustaining Engineer

Will provide product support, develop performance/cost reduction improvements and develop special products to meet specific customer requirements. This position involves RF circuit and system design, simulation and testing of FET or Bipolar devices; linear (class A/AB) circuits; power dividers, combiners; and control/monitor circuits.

If you are interested in working with state-of-the-art equipment in a professional and challenging environment, please send your resume to: **Shawn Oberreiter, Supervisor, Human Resources, Harris Corporation, P.O. Box 4290, Quincy, IL 62305-4290. EOE M/F/D/V.**



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RF Design

Perform RF subsystem performance/cost trade-off studies, design, simulation, layout, prototyping and testing of RF circuits (up to 2 GHz plus). Familiarity with receiver/transmitter architectures. Experience in RF PWB packaging, RF CAD tools (HP/EEsof, Sonnet) essential.

Production RF

Digital/analog circuits, stripline/microwave circuits, producibility, testability, test specs, and RF circuits operating in DC to 2 GHz range.

Production Systems

System level integration, RF/Digital comm. systems, fault isolation, microprocessor based design. ADA, FORTRAN, 1553, and X.25 muxes a plus.

Production Test

Eight years experience in test equipment design, RF test, IEEE-488, DFT, testability/productivity requirements. Knowledge of Labview/Labwindows or VEE a plus.

Combine your talents with our resources for an incredible career. In return for your expertise, we offer a highly competitive salary and comprehensive benefits. You may mail/fax/e-mail your resume to: **Human Resources, Mail Code 11A03SG, GEC-Marconi Hazeltine, 164 Totowa Road, CN 975, Wayne, NJ 07474-0975, fax: (973) 633-4455, or e-mail: jobs@systems.gec.com.** Please visit us on the Web: <http://www.systems.gec.com>. We are an equal opportunity employer, m/f/d/v. U.S. citizenship required. We can only respond to candidates under consideration.

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Engineering Companies Work Hard To Retain Engineers

TO KEEP QUALIFIED ENGINEERS ON STAFF, COMPANIES ARE REEVALUATING PAY SCALES, MANAGEMENT ISSUES, AND ENVIRONMENTS.

Robert Keenan

The hunt for qualified engineers, especially in the fields of RF and software, is a continuing saga for today's electronic companies. Companies are searching for more engineers, and are finding fewer qualified people to fill positions. These companies have turned to constant advertising, technical recruiters, billboards, colleges, and career shows to find talent. The problem is that there are not enough candidates in the market to fill all of the openings. In the wireless industry alone, estimates say that the need for qualified engineers will remain strong into the next decade.

One approach to solve this problem is to recruit less-experienced engineers, recent graduates, or engineers from other industries, and train them in the basic engineering principles of electronic, microwave, and wireless technologies. But, there are two problems to that approach: Cost and lost time. In the wireless industry alone, estimates say that companies spend over \$50,000 in training and engineer in basic RF and wireless technology. And those numbers do not include the approximate nine months of lost work time the company spends to train the engineer.

With the pool of engineering talent decreasing and the cost of training increasing, today's electronic, microwave, and wireless companies are working hard to keep the engineers they have on staff. "Retention is a major issue," says Jon Curley, manager of employment and college relations for M/A-COM Inc., Lowell, Mass.

"It is essential to our success to hang onto our knowledge," says Bryan Flake, human resources manager for American

Microsystems Inc. (AMI), Pocatello, Idaho. "There are not enough engineers out there to trade one for another." Mike Perna, manager of human resources in the Sector Technology Organization of Motorola's Semiconductor Product Sector, Phoenix, Ariz., agrees. He says that if an engineer leaves, they not only leave a position open, they also take their assets and abilities with them.

One major reason why companies are working hard to keep their engineers is cost. "We conservatively estimate that if a person leaves, it takes 40% of their annual salary to replace them," says Curley. "And that does not take into account lost opportunities for the company."

"A rule of thumb in human resources is that turnover costs are expensive," says Richard Daly, president of Humanex, Powell, Ohio, a human-resources consulting firm. "People estimate that losing an engineer can cost 60 to 70% of that person's salary plus bonuses."

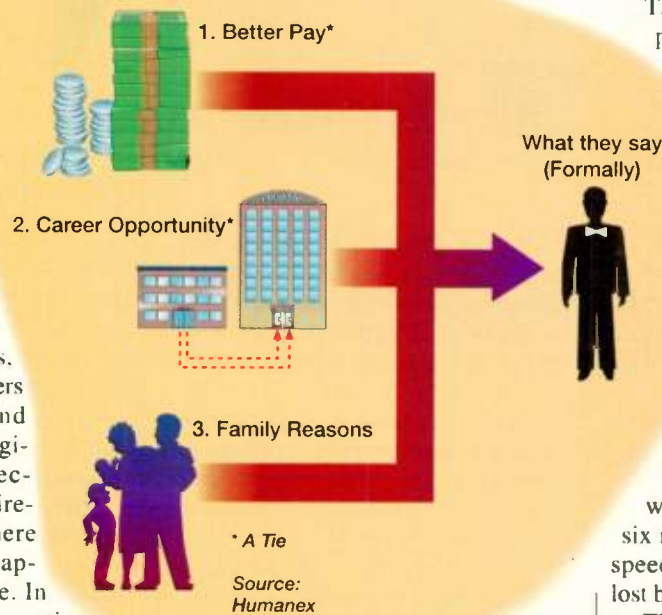
The cost of replacing an engineer appears in two main forms--direct and indirect. Direct costs include advertising fees, recruiting fees, training, and salary bonuses. When evaluating direct cost, companies also must consider rising salaries. Today's engineers are demanding and receiving higher salaries. As a result, it is more costly to bring them on staff.

Indirect costs, on the other hand, appear in two forms: Lost productivity and lost business. Daly says that when an engineer walks out the door, it will take about six months to get another person up to speed, leading to lost productivity and lost business.

The bottom line, according to Daly, is that losing an engineer is expensive. "It is a good idea to keep them around."

Therefore, companies must strive to keep the engineers they have. To do this, engineering firms have had to reevaluate many aspects of their operations, busi-

Top Three Reasons For Leaving The Company



1. During formal exit interviews, employees named better pay, career opportunity, and family reasons as the top three driving forces for leaving a company.

ness structure, pay scales, and human-resources policies.

A study distributed by Humanex provides some reasons why an engineer leaves a company. During formal exit interviews, employees claim that better pay, career opportunity, and family reasons are the top three driving forces for their departure from a company (Fig. 1).

But, these answers drastically change when the employee enters an informal setting. In this setting, the study shows that management issues, career promotion, and individual development are the three main factors why an employee has changed jobs (Fig. 2).

As a result, the goal for today's engineering companies is to address these issues and make changes in their company policies, operation, and culture. By doing this, companies stand a better chance of holding on to their engineering staff.

Without a doubt, management has a big influence on whether an engineer stays or leaves a company. In fact, in the study distributed by Humanex, management issues were the number one reason why an employee left a company. As a result, companies must continually reevaluate their managers and their management style.

"Managers are very important in creating an environment," says Dyer Matlock, vice president of engineering for Harris Corp.'s Semiconductor Division, Melbourne, Fla. "Management can clearly create a lot of barriers." Thus, the goal for the manager, according to Matlock, should be to lower barriers and foster an atmosphere where engineers feel they are "part of a bigger whole."

"The engineering manager must be able to build a rapport with people," says Dennis Lowry, executive director of human resources for Pacific Bell Mobile Services, Pleasanton, Calif. "Managers have to know their engineers as well as the engineers know themselves."

According to Mike Perna, finding the right manager is a challenge for a com-

pany. He says that to keep an employee, the manager must earn the respect of the engineering staff. To do this, the manager must possess many skills. They must match strong technical and business backgrounds with the ability to listen to the needs and concerns of his or her staff and to involve engineers in the direction and development of projects. The problem is finding people that offer all of these skills. "We haven't been able to solve that mystery yet," Perna says.

Daly says that companies have to work on management issues. To do this, companies must upgrade the skills sets of their managers. He says that managers must

concerns of the engineering staff. Daly says that engineering manager has to work their hardest to meet the needs of his or her staff.

Reevaluating management issues, however, only makes up one part in the formula to retain engineers. If a company wants to keep an engineer, they must support and offer a technically challenging environment. Engineers, by their nature, are technical people. As a result, companies must provide them with the technical challenge as well as the tools to solve those challenges.

To offer a technically challenging environment, Lowry says that companies must provide an atmosphere in which engineers fully utilize their skills. "The minute the engineer feels under utilized, their dissatisfaction goes up." But, according to Lowry, just using their skills is not enough. Companies have to take it one step further. He says that companies must challenge engineers to go beyond their skills.

Curley agrees. "The work they (the engineers) are being offered not only needs to be challenging, it needs to offer professional growth—something for the engineer to build their career on."

"Engineers don't want to be obsolete," says Daly. "They want to be on projects that will provide them with skills that will make them better down the road."

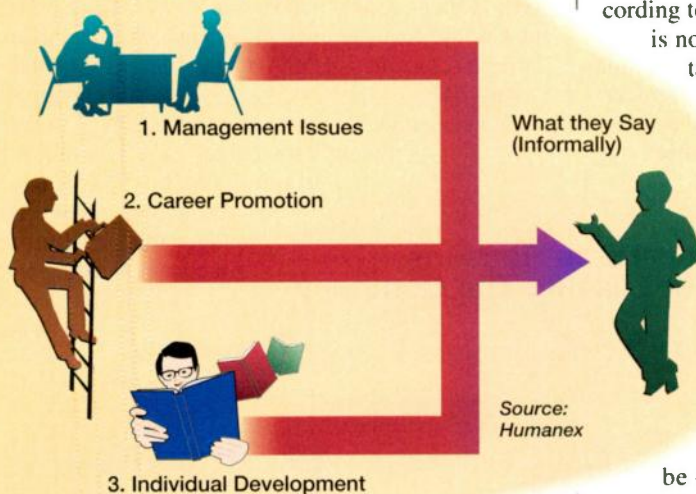
To provide these skills, Perna says that companies must invest in the engineer. One way to invest is by providing staff members with the latest engineering tools and equipment. Another way is to send them to seminars, trade shows, and conferences so they can improve their technical background.

Daly says that the engineer's main concern is whether or not they are acquiring the skills they need to be successful in the future. By investing in them, companies can help the engineers acquire the skills they seek.

In the study distributed by Humanex, career promotion also proved to be a main concern for engineers when they are leaving a company.

Advancement for an engineer is a bit

Top Three Reasons For Leaving The Company

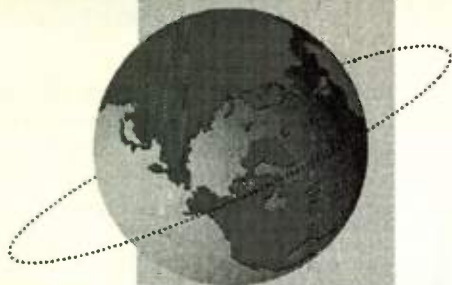


learn to
1. During formal exit interviews, employees named better pay, career opportunity, and family reasons as the top three driving forces for leaving a company.

deal with problems on a case-by-case situation and must recognize that every person is unique. He adds that good managers figure out who the engineer is and what motivates them.

One way an engineering manager can be successful is by finding out the needs of his or her staff. To do this, Daly suggests meeting personally with staff members and ask them what their needs or concerns are. Matlock agrees. "Managers must listen to their staff."

But, just listening is not enough. The critical step is acting on the needs and



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Assume responsibility in customer support and return areas. Customer support includes technical discussions, generating data on devices, and providing customers with test fixtures, circuit boards, etc. Customer returns include evaluating parts returned by the customer and resolving related issues. The product line for the above is unmatched FETs and HEMTs, internally matched FETs, and MMIC products. Requires BS/MS in Microwave Engineering, with 8+ years of multi-tasking, record-keeping, and hands-on testing. Good overall experience with microwave circuits/control circuitry involving GaAs or silicon devices. Familiarity with microwave test equipment such as network analyzers, etc. (Dept. AEM)

Senior GaAs LSI Design Engineer (Mixed Signal)

Participate in the development of a GaAs LSI for high-speed data communication systems and/or telecommunication systems, with IC design responsibilities for circuit design and layout through prototype generation to transfer to production. Requires a BSEE and 5 years' experience or an MSEE and 3+ years' experience. Candidates must have experience with UNIX and engineering workstation tools such as HSPICE and CADENCE. (Dept. SGE)

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MMIC Design Engineer

Will participate in the development of high-performance microwave and millimeterwave GaAs MMICs for commercial markets. This position requires a BS degree and 3+ years' experience in MMIC product design. Candidates must have experience with device characterization techniques such as loadpull and chip-level active and passive element evaluation. Modeling experience is preferred. Familiarity with software tools such as Touchstone, HP-MDS, AutoCad and microwave test equipment is essential. (Dept. MDE-2)

Lightwave Lab Engineer

Provide application notes and technical support to Fujitsu and customers. You will work with the lightwave lab application group to help design the product development program. Requires a BSEE/MSEE and 3+ years' experience in fiber optic device development or in teaching fiber optics and/or compound semiconductor theory. Must have good communication skills and be willing to travel. (Dept. LLE)

Lightwave Lab Applications Manager

Take overall responsibility for providing application notes and technical support to Fujitsu and customers. You will also manage the lightwave lab application group to implement the product development program. Requires an MSEE/PhD in EE and 3+ years' experience in fiber optic device development or teaching fiber optics and/or compound semiconductor theory. Must have good communication and management skills and be willing to travel. (Dept. LLAM)

Area Sales Manager, Lightwave

We are seeking an individual who possesses technical expertise and sales skills to assume responsibility for direct sales of our lightwave product line consisting of lasers and detectors for high-speed digital, local loop and analog CATV communication systems. You will develop an in depth knowledge of applicable components and systems and create solutions to customers' needs and problems. Requires a BS/MS in EE or Physics and 3+ years' engineering experience in electro-optics or fiber communications. Sales experience, including new account development is a plus, but not mandatory. Travel up to 25%. (Dept. ASM)

GaAs IC Marketing Manager (Digital IC)

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Microwave Technician

Your primary objective will be to support device development/application engineers, prepare prototype samples, etc. You will perform microwave device/module testing, maintain test records, stations and components. Requires an AA in electronics and 4 years' experience. The ideal candidate will be able to tune and test microwave chips and components, be familiar with test equipment such as Network Analyzers, the DC tester curve tracer, etc. (Dept. MT)

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Transferable Skills Are The Key To Landing The Next Job

BEING A "JACK-OF-ALL-TRADES" MAY GIVE ENGINEERS MORE JOB OPTIONS.

Patricia L. Walker

If you are a wireless, RF, digital, VLSI, circuit design, software or software systems engineer with 3 to 6 years experience, you are the ideal job candidate for the numerous openings across the nation for engineers in the communication industry. The Catch-22 is this: Do you have the right skills, and are they transferable?

While the job openings are numerous throughout the U.S., companies are being very "picky" about the skills an experienced engineer will bring to a job. A position can remain open for many months, some staffing managers say, until they find the right person with the right skills.

An experienced engineer must be careful not to get him/herself into a niche or set of skills that will not be transferable elsewhere, cautions Elizabeth Whitesides, administrator at Panasonic in North Carolina. "For example, we are looking for very specific skill sets in wireless and RF satellite design," she says, including a masters degree in EE and 5 to 10 years experience. "Sometimes it takes a year to fill the position."

Whitesides' caution about transferability also is echoed by Richard Gorberg, senior recruiter at Fortune Personnel Consultants. An engineer could be qualified in a given specialty such as RF, but his skills must be "usable and transferable" in that specialty. He has to ask himself, Gorberg says, "Are the skills I am picking up on the job readily transferable to another company or product?" that is, are they highly sought-after skills elsewhere?

According to recruiters, an electronic or computer science engineer from a good school and with 3 to 5 years experience and the right skill sets can expect 2 to 4 job offers in the current market.

There are similarities in the demand for certain engineers that are appearing across the board. Design engineers are in great demand at the moment, more than manufacturing or applications engineers. The tightest sector, the greatest demand with a limited supply, is VLSI engineers, and some companies are already looking outside the U.S. for their candidates. IC chip design positions also are hard to fill.

Meanwhile, phone, cable, and Internet companies are requiring equipment to build out their services quickly. Combined with the current corporate desire to develop families of products rather than be one service, the result is firms are rapidly raising the demand for more design engineers in these fields.

The surge also is creating a stronger need for some skill sets, not previously in as great a demand. One such area is the openings for test and quality assurance engineers with an emphasis on the EE degree and not an ME degree. The intense push to design new products and get them quickly to the market has increased the demand for quality metrics and quality procedure talent, recruiters note.

The competition to produce communication products is so intense that a company has to decide whether to design it or partner-up with another firm, explains Gorberg. If they enter into a partnership, the quality engineer has an important role in establishing a good business alliance.

Another area with increasing job openings is the millimeter wave radio field. The increased use of cellular phones is forcing companies to use millimeter wave, short-haul radios to get around the radio interconnect cell site demand, a staffing manager for Hewlett-Packard's Wireless Infrastructure Division, notes.

HP is also looking for engineers who are skilled in high linearity amplification. It is such a new field that 3 to 5 years experience is all that can be expected.

But hope and opportunity for the engineer who does not necessarily have the exact skill sets for a job is not lost. Met with the challenge of filling these many job openings, companies are revealing their willingness to retrain and crosstrain.

Lionel Eras, president of AZTech Recruiting Co., sees a trend developing with EEs working in the electronic divisions of automotive companies. It is like the early 1990s, he said, when defense and aerospace were downsizing. Good engineers from the electronic automotive sector can be retained for these newer segments of the industry.

Those engineers wanting to travel abroad also can find such opportunities, according to Manny Rao, vice president of Recruiting Services Inc. U.S.-based companies are installing production overseas.

Regardless of the heady competition for good talent, whether or not a company will pay relocation expenses to some of the "hot spots" of demand appears to be a contrite issue. Not all companies are willing to pay such expenses, while others are paying the expenses and giving a sign-on bonus.

Some recruiters report RF design, wireless, and test and quality engineers are offered sign-on bonuses, relocation expenses, and real estate commissions paid. Others say relocation packages are not as lucrative as 5 years ago. Yet, some firms are instituting new attractions, such as flexible hours, day-care centers, and 4-day or 9-day two-week work weeks.

Eras of AZTech notes that the while the San Diego demand is huge, many of the smaller companies are still reluctant to relocate people, and they continue to look within their own area.

Martin, however, has the reverse situation. She says the companies will pay relocation expenses. The problem is that many are government contractors and must find U.S. citizens for their positions. Other recruiters also report that defense contractors are having a difficult time competing for qualified engineers in the current market. U.S. citizenship does not grow, they say.

Pat Walker is a former Staff Director of the IEEE

Company Profiles

QUALCOMM Inc.

QUALCOMM Inc. employs over 7000 people and is a leader in digital wireless communications technologies. The company develops, manufactures, licenses, and operates advanced digital wireless communications systems and products.

QUALCOMM is the developer of code-division multiple access (CDMA) spread-spectrum technology, which is the cornerstone of many advanced communications systems such as personal communications services (PCS) and wireless local loop (WLL). The company manufactures infrastructure and telephones based on this technology. QUALCOMM's other major product areas include the geostationary satellite-based OmniTRACS mobile communications system (recipient of the Computerworld Smithsonian Award), applications-specific integrated circuits (ASICs) for CDMA and other applications, the Eudora Pro e-mail software package, and, in conjunction with others, the Globalstar low-earth-orbit (LEO) satellite communications system. At QUALCOMM, engineers will work with innovative digital technologies and will be assigned responsible duties with an active role in their team's effort.

Company headquarters is located at:
6455 Lusk Boulevard
San Diego, CA 92121

ANADIGICS, Inc.

ANADIGICS, Inc. is leading supplier of gallium-arsenide (GaAs) ICs. These ICs are used in cable television, fiber optics, wireless communications, Direct Broadcast Satellite, and ETACS systems. ANADIGICS is the highest volume GaAs IC manufacturer. It is known for developing the first single-chip GaAs power amplifier for commercial cellular telephones and the first single-chip Direct Broadcast Satellite downconverter.

Founded in 1985, ANADIGICS has approximately 400 employees, which includes about 100 engineers. At ANADIGICS, an engineer will find constant innovation using GaAs technology in low cost, high volume consumer electronics applications.

Company headquarters is located at:
35 Technology Drive
Warren, N.J. 07059

Ball Aerospace & Technologies Corp.

Based in Broomfield, Colo., Ball Aerospace & Technologies Corp. (BATC) is a pioneer in microwave, spacecraft, communications, and electro-optical technologies. BATC's two divisions--Aerospace Systems and Telecommunication Products--provide services to a wide range of customers including NASA, the Department of Defense, commercial customers, and the academic community.

A subsidiary of Ball Corp., Muncie, Ind., BATC was founded in 1956. The company employs approximately 2200 people. BATC has engineering openings in RF/antenna design, microwave analog and digital-circuit design, antenna production and test, spacecraft, mechanical, optical, and software.

Company headquarters is located at:
P.O. Box 1062
Boulder, CO 80306

Fujitsu Compound Semiconductor, Inc.

Fujitsu Compound Semiconductor, Inc. (FCSI) is a U.S.-based distribution and R&D arm of Fujitsu Ltd's Compound Semiconductor Group, a worldwide supplier of optoelectronic and microwave semiconductor components.

Headquartered in San Jose, Calif., FCSI serves North America, South America, and selected international locations as a distributor of microwave and lightwave gallium-arsenide (GaAs)-based semiconductor products used in the communications industry. With sales exceeding \$125 million per year and over 15 years experience, FCSI provides its customers with a combination of local engineering and technical support backed by the manufacturing strength of Fujitsu's Japanese and overseas factories. For more information, visit the company's web site at <http://www.fcsi.fujitsu.com>. Resumes can be e-mailed to jobs@fcsi.fujitsu.com.

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Northrup Grumman Corp. Electronic Systems Division

Headquartered in Rolling Meadows, Ill., Northrup Grumman Corp's Electronic Systems Division develops RF and infrared countermeasure systems for the U.S. and international defense electronics markets. This company offers engineers a chance to work with leading-edge technology for advanced electronics systems design and development.

Winner of the R&D 100 Award, Northrup Grumman's Electronic Systems Division is known for its advanced RF internal countermeasure system. It also is leading the development of an advanced infrared countermeasure system.

Northrup Grumman Electronic Systems Division employs approximately 2500 employees, including 1400 engineers. In the next year, the Electronic Systems Division plans to add 300 engineers to its software, systems, electro-optical, and radar divisions.

Company headquarters is located at:
600 Hicks Road
Rolling Meadows, Ill. 60008

Level One Communications

Level One Communications provides silicon connectivity solutions for high-speed digital-signal telecommunications and networking applications. The company's components are critical in connecting links in today's telecommunications and data communications local-area network (LAN) and wide-area network (WAN) applications. In addition, these components are key building blocks for the intranets and Internets of the future.

Level One combines strengths in analog and digital circuit design with communications systems expertise to provide mixed-signal solutions with increased functionality and reliability. Located in Sacramento, Calif., Level One Communications has revenues of \$112 million and employs 400 people.

Company headquarters is located at:
9750 Goethe Road
Sacramento, CA 95827

Wiltron Company

Headquartered in Morgan Hill, Calif., Wiltron Company is a recognized leader in the design and manufacture of advanced microwave and telecommunications test instruments and systems. The company offers communications, test, and monitoring solutions to service providers and equipment component manufacturers throughout the world.

Wiltron Company is a member of the Anritsu Corp. based in Japan. Wiltron currently employs 600 people.

Company headquarters is located at:
490 Jarvis Drive
Morgan Hill, CA 95037

DENSO Wireless Communications

DENSO Wireless Communications is rapidly becoming a leader in the international market for cellular phones and private wireless systems. The company's engineering staff at its R&D facility has been developing CDMA-based phones and private wireless systems for international customers and is positioned to develop and introduce these products to the U.S. market.

DENSO Wireless' commitment to wireless technology is backed by DENSO Corp., a diverse international company with annual sales topping \$13 billion and over 50 years of success in the electronics industry. Over 64,000 employees in 22 countries contribute to the 340 product lines manufactured for a variety of industries.

DENSO Wireless Communications is located in Carlsbad, Calif., just north of San Diego. The company has just announced the construction of a new 77,000-sq. ft. facility. For more information visit the company's web site at <http://www.densolabs.com>. Responses can be e-mailed to the company at jobs@densolabs.com.

Company headquarters is located at:
2131 Palomar Airport Road
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Reliability Engineer

Develops life test strategies and performs life test studies; analyzes life test data and project reliability performance; interacts with designer and product engineers in developing and planning reliability programs, as well as with the FA laboratory in the analysis of test failures. Also conducts studies to determine thermal characteristics of various designs and packages.

BSEE or Physics degree and at least 3 years of applicable experience required. Must have familiarity with microwave circuitry design and troubleshooting. Computer literacy essential. **JOB #96-65/MFR**

Device Engineer

Electrically characterizes new devices and circuits. Supervises layout, manufacturing and assembly of new device and develops test program for new devices. Evaluates new equipment for processing/device development and testing. Supports the improved M gauge resistivity program used in manufacturing. Conducts technology development for advanced passive components.

BS in Electrical Engineering, Physics or equivalent and at least 5 years of experience assembling and manufacturing power devices required. Must have design experience in power devices, specifically GaAs FETs. Background in device physics, processing, modeling and thermal design essential.

JOB #95-72/MFR

Senior Design Engineer

Independently designs and develops new RF IC products to volume production. Duties include electrical, mechanical layout, packaging and assembly design. Characterizes, models and analyzes devices such as FETs, diodes and passive components. Designs and purchases test fixtures and setups. Provides customer support on technical matters.

BSEE required, MSEE or higher a plus. Must have 5 years of directly related experience and broad background in characterization and applications of ICs for RF and Microwave. Will need to work independently with minimal supervision and train other engineers/technicians. **JOB #96-280/MFR**

RF Microwave Technician

Performs full characterizations of new products, including electrical mechanical and thermal tests; sets up, calibrates and maintains test equipment, such as RF probe station, vector network analyzer and spectrum measurement equipment; designs/ fabricates soft and hard board based test fixtures and prototype circuits for engineering purposes; procures material, components and services for product development.

Associate's degree in Electronics or equivalent and at least 5 years of directly related experience required. Broad background in characterization and applications of RF and microwave components essential. Must be familiar with such software programs as Microsoft Excel/Word and AutoCAD. Ability to work with minimum supervision necessary. **JOB #97-57/MFR**

Senior Thin Film Engineer

Duties involve sustaining and improving existing thin film deposition processes.

Master's or Ph.D. in Engineering or Physics or Material Science required. 3 years of semiconductor experience essential. Must have knowledge of evaporation, sputtering and PECVD. **JOB #96-206/MFR**

Packaging Engineer

Designs and develops surface mount packages.

BS/MS in Mechanical Engineering or Materials Science and at least 2 years of experience in electronic packaging or equivalent required. Will need background in thermal characterization, analytical skills and qualification of materials. **JOB #96-144/MFR**

Training Manager

Conducts assessment of training needs and develops programs to meet them; evaluates, designs and delivers training programs and processes that'll enable us to improve effectiveness of our Human Resources.

B.S. in Business or education-related discipline required. Advertising degree and training certifications a plus. 5-8 years of experience in Training and Development essential. Must have knowledge of instructional system design and development. Will need ability to apply abstract and critical thought processes.

Strong interpersonal, written communication and training leadership skills required. **JOB #97-191/MFR**

Director of Package Development

Designs and develops new high frequency, low cost packages, as well as develops manufacturing process required for high volume production.

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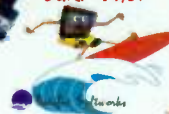
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PART	MHz	MHz	MHz
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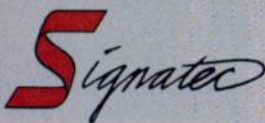
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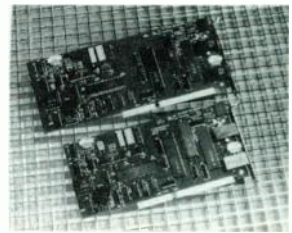
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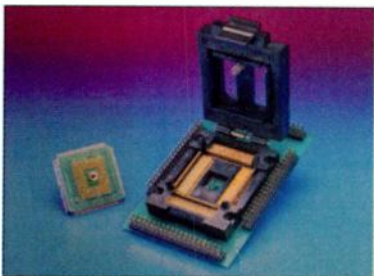
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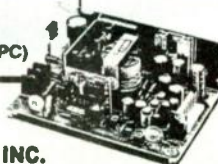
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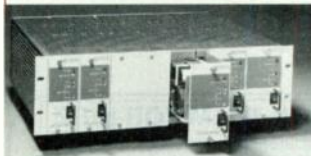
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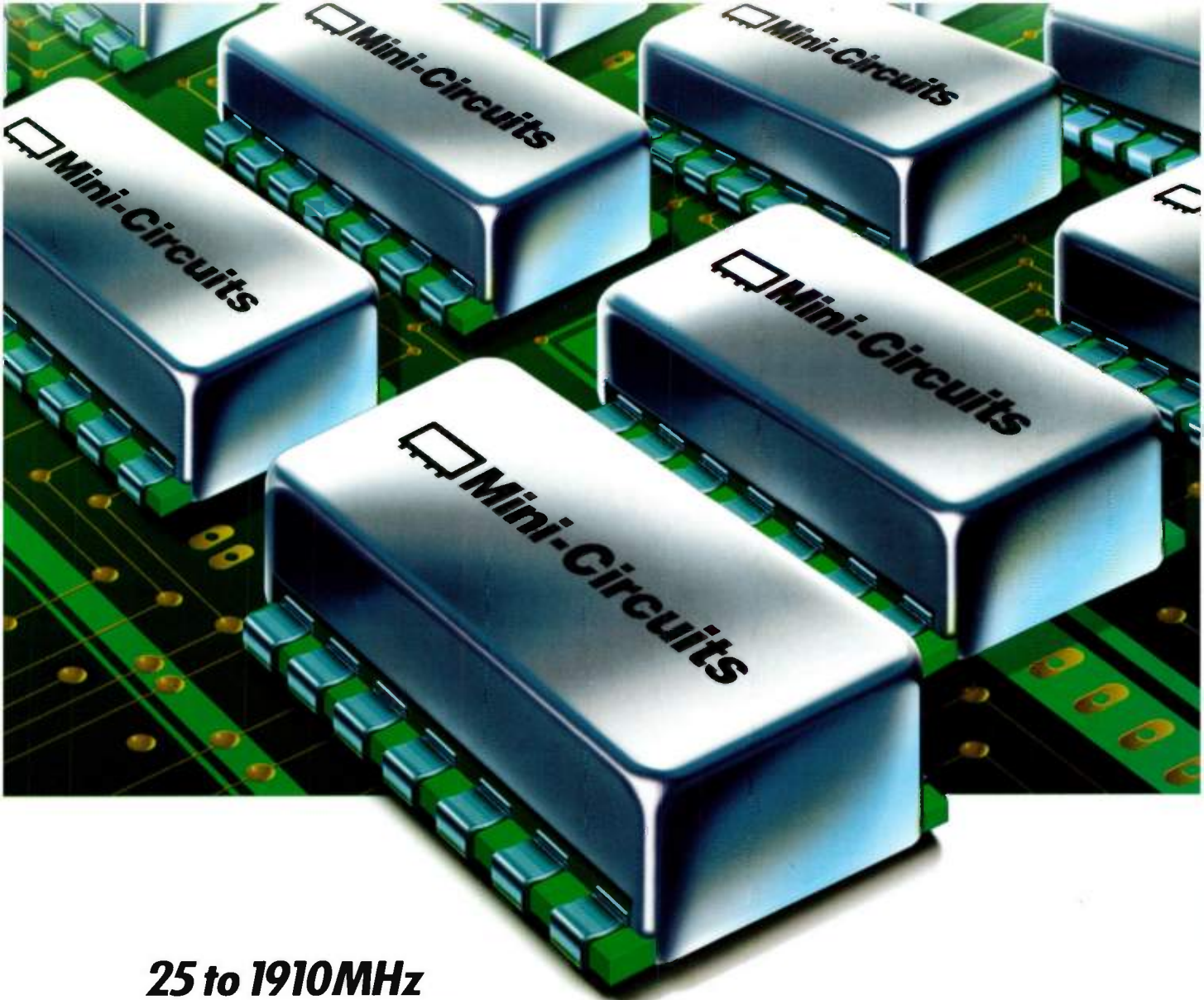
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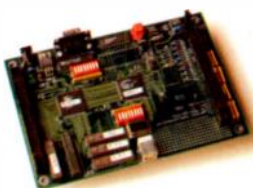
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