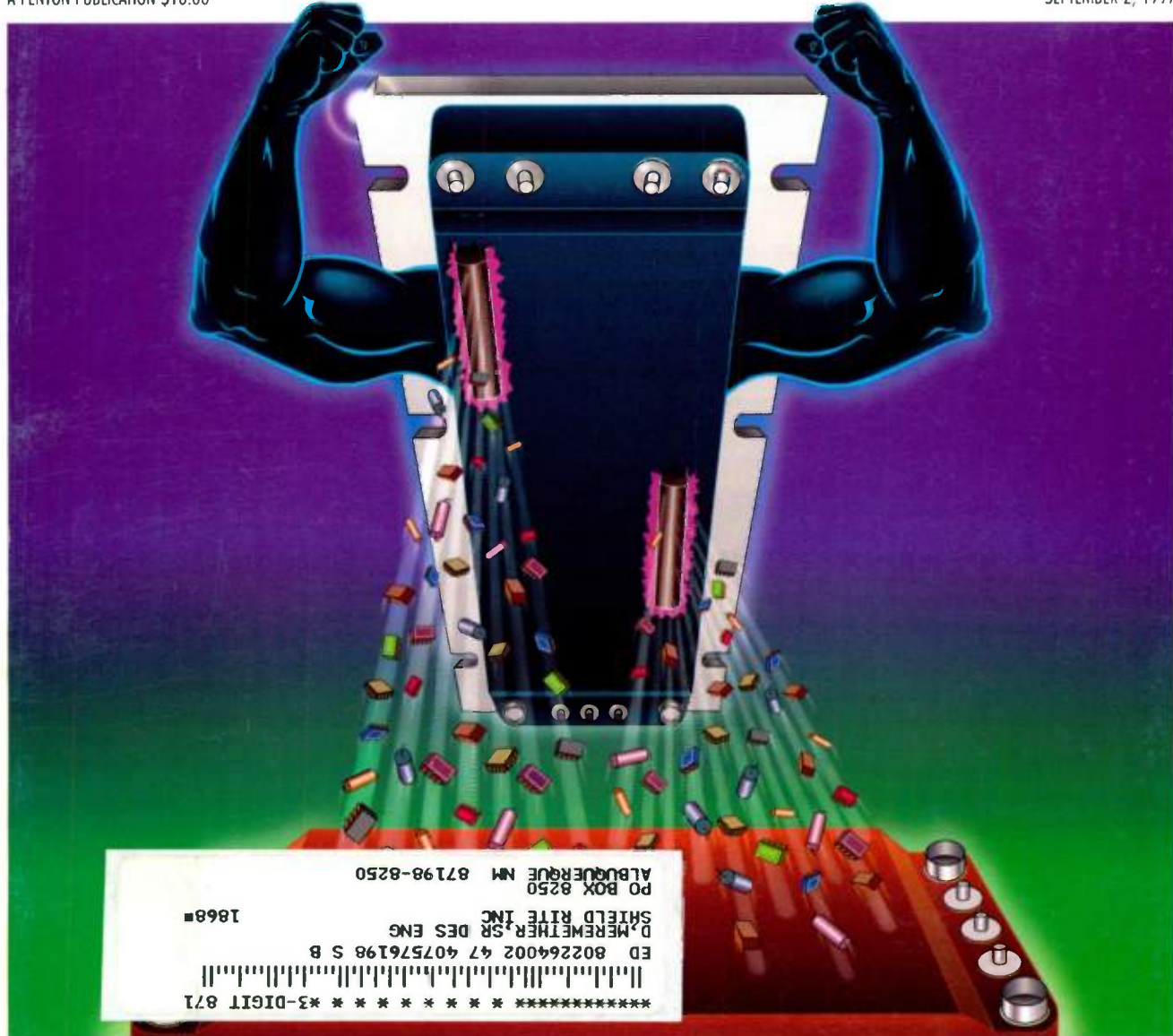


ELECTRONIC DESIGN

FOR ENGINEERS AND ENGINEERING MANAGERS - WORLDWIDE

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SEPTEMBER 2, 1997



New DC-DC Converters Flex Their Muscles p. 40

Line-Driver Design For Broadband Communications Applications p. 46

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C32-Based Design Roars With An X86 Host p. 85

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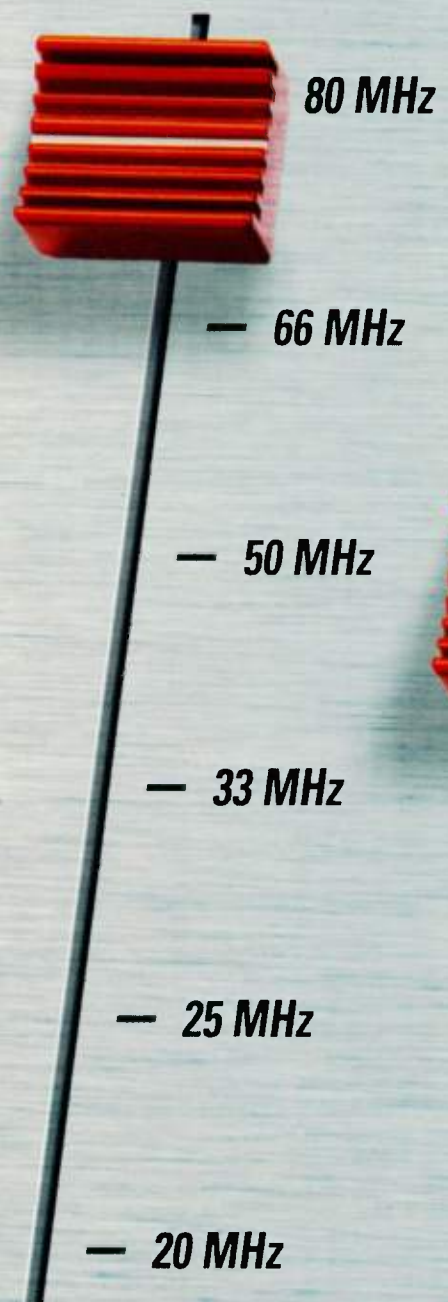
Take The Mystery Out Of AC Termination p. 136

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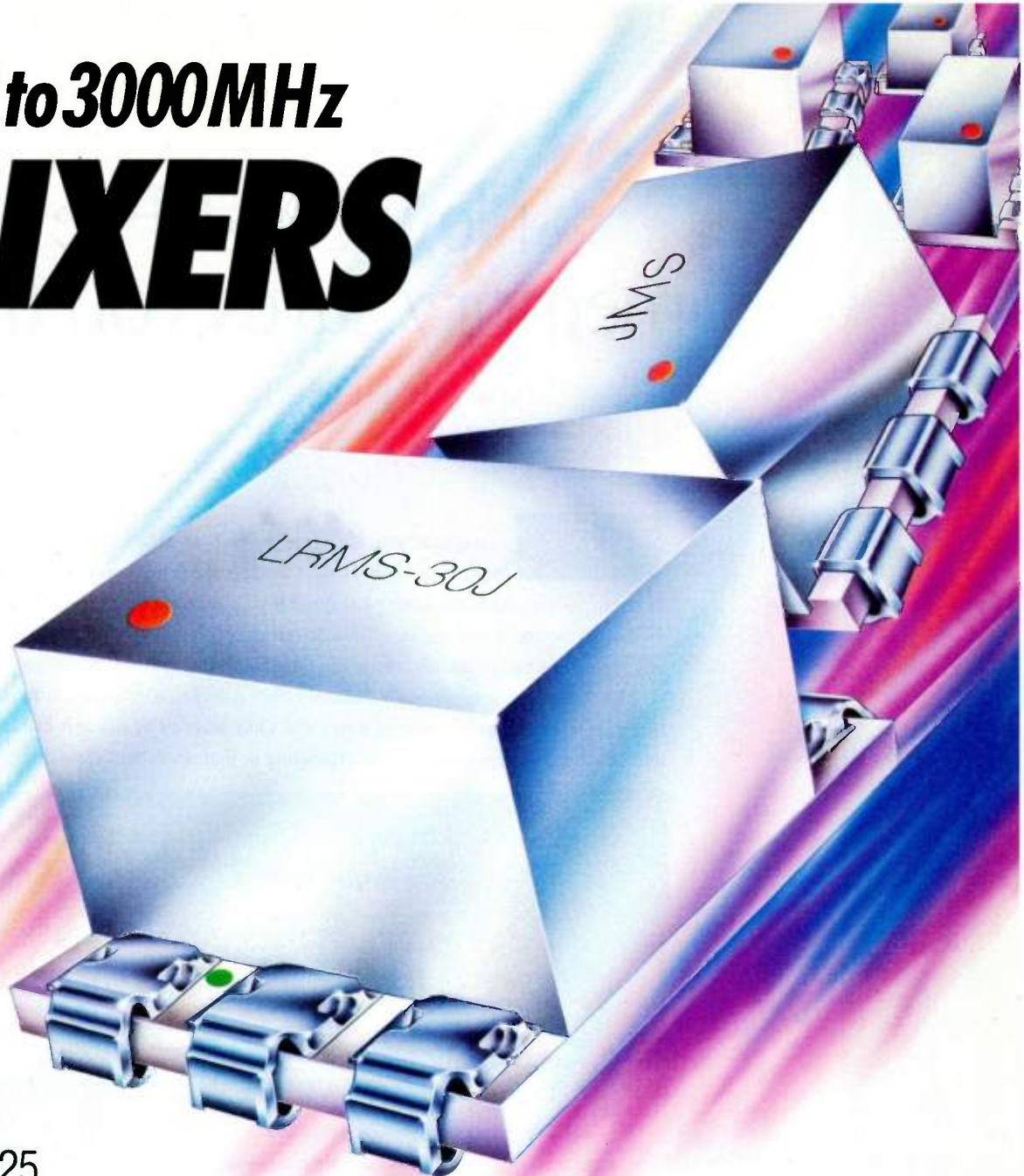
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JMS-2LH	+10	20-1000	DC-1000	6.5	48 35	9.45
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September 2, 1997 Volume 45, Number 19

EDITORIAL OVERVIEW



■ New DC-DC Converters Flex Their Muscles 40

■ Line-Driver Design For Broadband Communications Applications 46

■ Instrument-On-A-Card Standard Makes The Most Of PCI 65

■ C-32-Based Design Roars With An X86 Host 85

■ 1997: The Year Of The Rail-To-Rail I/O IC Op Amp 97

■ Capacitor Options And Advances For High-Frequency Applications 111

■ Take The Mystery Out Of AC Termination 136

TECH INSIGHTS

40 Second-Generation DC-DC Converters Up Power Density And Lower Cost

• Using the latest integration technology and innovative magnetics, the converters also improve reliability and speed time-to-market.

COVER
STORY

46 Line-Driver Design For Broadband Communications Applications

• Following is a practical guide to designing low-power, low-distortion circuits for XDSL and cable modem systems.

65 Instrument-On-A-Card Standard Makes The Most Of PCI

• A new class of instrumentation products fits neatly in between PCI-based computer boards and the more expensive VXIbus architecture.

TECH INSIGHTS

72 Update On Ion Implanters

• Low-energy Ion implants target shallow junctions for deep-submicron ICs

74 Product Features

DSP

85 Get The Most Out Of The TMS320C32 With An x86 Host

• Squeezing performance from a C32-based DSP system doesn't require black magic; just careful design with attention to detail.

ANALOG OUTLOOK

97 1997: The Year Of The Rail-To-Rail I/O Op Amp

• Low-power, low-voltage devices in tiny packages sporting rail-to-rail inputs and outputs dominate the scene.

DEPARTMENTS

Upcoming

Meetings12, 80HH
.....81,162

Editorial18

• Sharing the profits and the risks

Technology Briefing ...20

• When encryption is outlawed, only outlaws will encrypt

Technology

Newsletter25, 28

Technology

Breakthrough31

• Sophisticated techniques are being applied to lower voltage and power levels for analog ICs

Info Page10

• (how to find us)

EE Currents & Careers .193

Index of Advertisers ..208

Reader

Service Card208A-D

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ELECTRONIC DESIGN

September 2, 1997 Volume 45, Number 19

EDITORIAL OVERVIEW

PIPS

111 Capacitor Options And Advances For High-Frequency Applications

• Recent technology advancements greatly improve the reliability and cost of surface-mount capacitors in wireless designs.

116 Product Update: Resistors, Transformers, And Inductors

118 PIPS Products

BOARDS & BUSES

135 PC Graphics Watch

• Specifying and procuring flat-panel displays

136 Take The Mystery Out Of AC Termination

• Understanding how to implement ac termination, helps maintain the power and cost levels in high-speed buses.

150 The BUSIness Report

• Here come the PCI buses, part II

152 What's On Board

154 Boards & Buses Products

165 Ideas For Design

- Circuit allows any 8051 microcontroller to speak IrDA
- Use a tiny microcontroller with a large keypad
- Automatic phase detector for digital communications

173 Pease Porridge

- What's all this errata stuff, anyhow?

177 Walt's Tools And Tips

- The readers respond:

181 European Products

182 New Products

- Digital ICs
- Communications
- Analog
- Test & Measurement

190 New Literature

192 Readers' Response

QUICKLOOK

Market Facts80C

40 Years Ago80D

Off The Shelf80D

Document Reader Picks Up Errors In The Blink Of An Eye80F

Quick News80H

The Envelope, Please ..80J

Y2K Update80L

Internet Rolodex80N

Hot PC Products80P

Trudel To Form80R

Halftime Report: 1997 U.S. Electronics Sales Up 9%80W

A Notable Class80W

Off The Shelf80Z

Tips On Investing80Z

Internet News80DD

Candid Photography .80DD

White Collar Blues Makes The Scene80FF

It's That Time Again! 80FF

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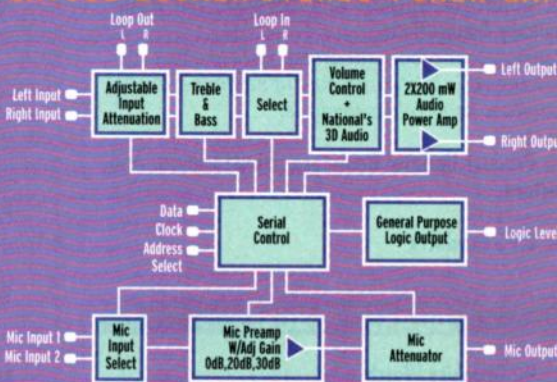


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Family Specifications

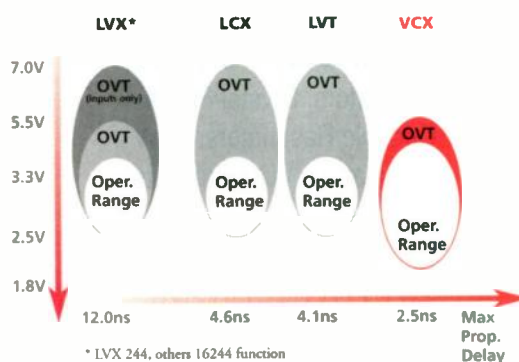
Power Supply (Vcc)	1.8-3.6V
Drive (IOL/IoH)	+/-24mA @ 3.0V Vcc +/-18mA @ 2.3V Vcc +/-6mA @ 1.8V Vcc
Supply Current (Icc)	0.25µA
Speed* (Tpd)	1.8ns @ 3.3V 2.0ns @ 2.5V 3.0ns @ 1.8V
Noise VolP/VoLV	0.8V/-0.8V @ 3.3V 0.6V/-0.6V @ 2.5V 0.25V/-0.25V @ 1.8V

Over-voltage Tolerance Specifications*

Input Leakage Current (Ii)	(0≤Vi≤5.5V)	0.04µA
3-STATE Output Leakage (IoZ)	(0≤Vo≤5.5V)	0.04µA
Power-Off Leakage Current (Ioff)	(Vi or Vo=5.5V)	0.25µA

* typical values represented

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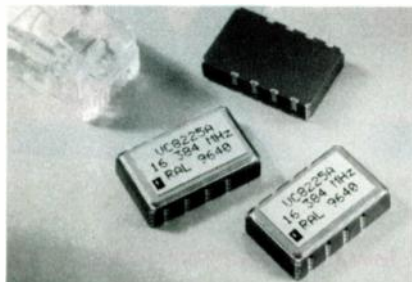
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The Vision Show, Sept. 16-18. Santa Clara Convention Center, Santa Clara, California. Contact Automated Imaging Association, Ann Arbor, MI, (313) 994-6088; fax (313) 994-3338.

International Conference on Solid State Devices and Materials (SSDM), Sept. 16-19. Act City Hamamatsu, Hamamatsu, Japan. Contact Secretariat of SSDM '97, Business Center for Academic Societies Japan, 5-16-9 Honkomagome, Bunkyo, Tokyo 113, Japan; +81 3 5814 5800; fax +81 3 5814 5823; e-mail: config3@bcasj.or.jp.

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Thermionic Workshop, Sept. 21-23. Cannes, France. Contact Bernard Courtois, +33 35 76 7 46 15; e-mail: bernard.courtois@imag.fr.

ISS'97: World Telecommunications Congress, September 21-26. Toronto, Canada. Contact The Pinnacle Group: Victoria Lord, (416) 588-2420; Jane Tucker, (416) 588-3522; Internet: <http://www.ISS97.org>.

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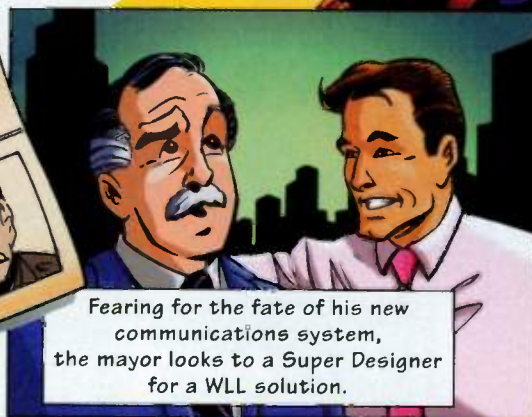


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THE CANCELLER™
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and anybody else
who gets in the
way of design
completion.



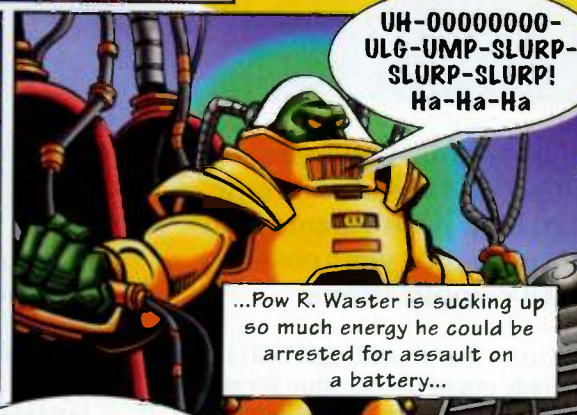
Fearing for the fate of his new
communications system,
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for a WLL solution.



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god of communications, sees
everything's compatible. Or else...



In the city, Echo-Echo
is making every phone conversation
sound like heavy metal in a trash can...



UH-00000000-
ULG-UMP-SLURP-
SLURP-SLURP!
Ha-Ha-Ha

...Pow R. Waster is sucking up
so much energy he could be
arrested for assault on
a battery...



...and frequency interference
is creating cross-talk.

Hello?
Where?
You?
Are you?
What?
Goodbye.
There.
This?
Uh?



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coming! Well, being a Super
Designer means having
Super Friends.

And, a fast way to reach them!

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Let's go.

Pow. R. Waster's mine. Hey Waster. My 3V's outlasting your 5V! How's that for a CODEC moment!

Get a whiff of this GaAs! That oughta stop you "freqs" from mixing it up and making cross-talk.

Con-grat-u-lations!!!
Super "D."

GULP!!! Hope he's not thinking of running for mayor!

Cancel me this, Echo-Echo. What's so quiet you can't hear it?
You!
My 55ms does it every time...
You're outta my WLL!

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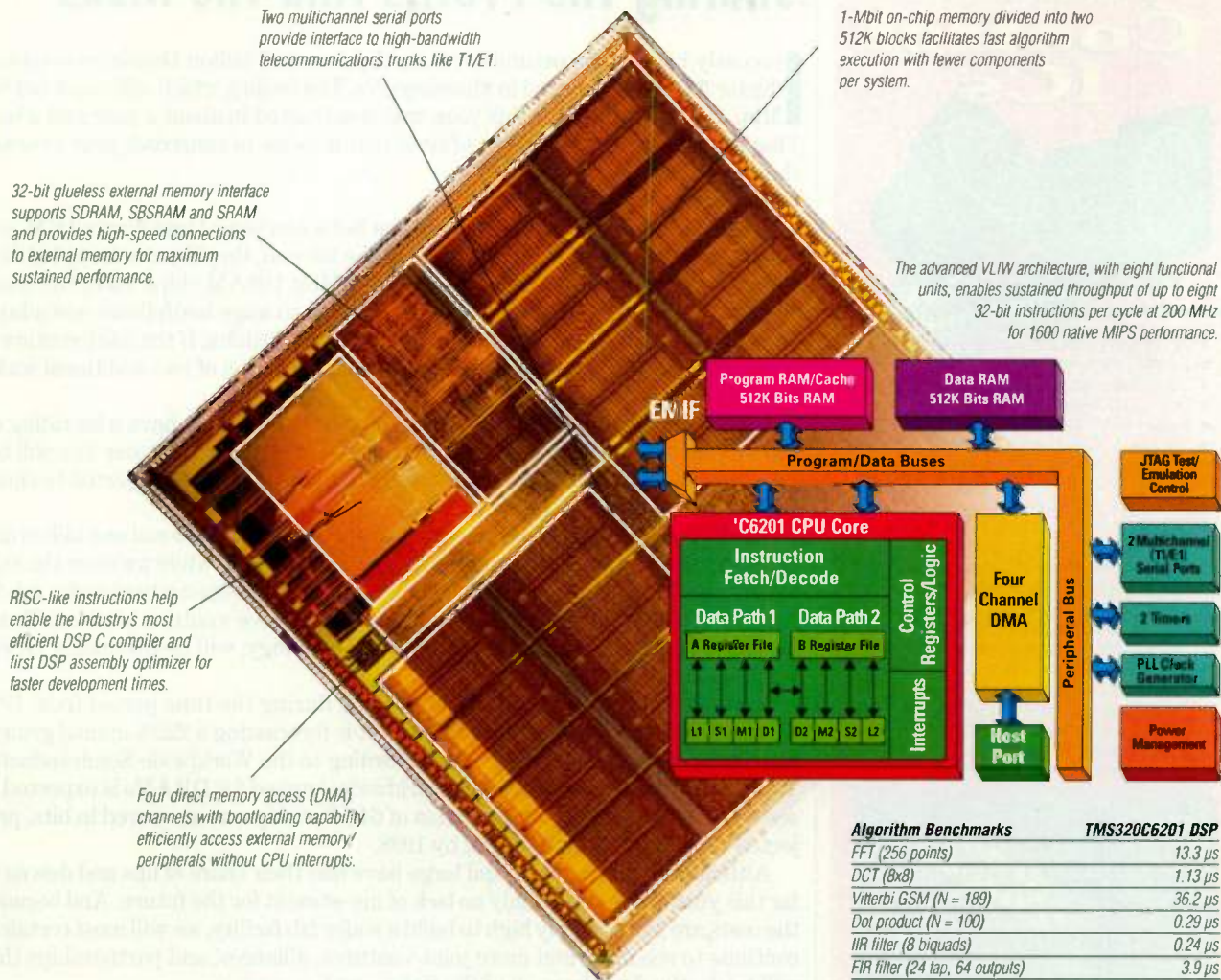
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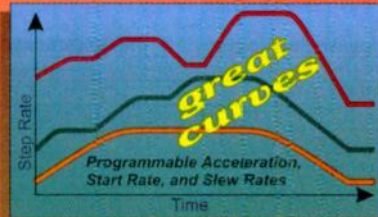
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Sharing The Profits And The Risks

I recently had the opportunity to tour the new \$1.6-billion Dominion semiconductor fab facility located in Manassas, Va. The facility, which will crank out 64-Mbit DRAM chips later this year, was constructed in about a year and a half. That's about the same amount of time that it takes to construct your average shopping mall.

Amazing.

The Dominion fab is a joint venture between long-time rivals IBM and Toshiba. And although they're friends at the fab end, they'll continue to battle it out at the product level once those new 64-Mbit DRAM chips leave the dock. However, the cost of a modern-day fab makes strange bedfellows nowadays, even for such industry heavyweights as IBM and Toshiba. If the joint venture is successful, the site's master plan allows for construction of two additional wafer fab facilities.

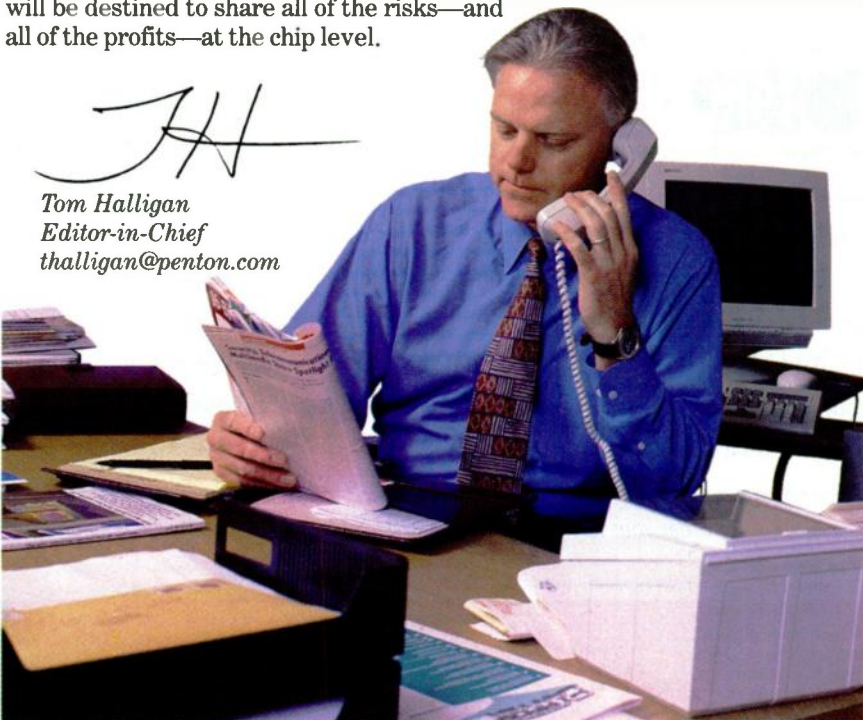
It is an impressive facility and both companies obviously have a lot riding on the success of the 64-Mbit DRAM. Production of commercial wafer lots will begin soon. The fab should reach full speed next year when it is expected to churn out 1100 wafer starts per day.

In addition, IBM has said it also will be spending an additional one billion dollars to upgrade its existing semiconductor facilities. And while we're on the subject of new facilities, Temic Semiconductors is about to open a new wafer fab facility in Itzehoe, Germany. The facility, a cooperative venture between Temic and the Fraunhofer Institute for Silicon Technology, will be producing power semiconductors.

In regard to the 64-Mbit DRAM market, during the time period from 1995 through 2001, the research firm Dataquest is forecasting a 225% annual growth rate for 64-Mbit DRAM chips. And according to the Worldwide Semiconductor Trade Statistics Organization, the worldwide demand for DRAMs is expected to see "strong growth," with production of 64-Mbit chips, as measured in bits, projected to surpass 16-Mbit output by 1998.

Although chip makers by and large have had their share of ups and downs so far this year, there is certainly no lack of investment for the future. And because the costs are so incredibly high to build a wafer fab facility, we will most certainly continue to see more and more joint ventures, alliances, and partnerships that will be destined to share all of the risks—and all of the profits—at the chip level.

Tom Halligan
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Less Firmware; One Processor for Multiple Channels

But the DS2152 then goes on to add features to increase flexibility with two goals in mind. First, it incorporates more functions in the hardware, eliminating the expense and time required for firmware or external hardware development. Second, the new chip reduces processor real-time servicing. One processor can now service multiple channels, reducing board space consumed and costs for additional chips.



The New Features Menu

● **Crystalless Jitter Attenuation:** A single T1 clock source can now serve up to 28 channels, greatly reducing the board space required and the cost of multiple crystals. This feature is especially advantageous in multi-port designs.

● **Hardware Voice Signaling Support:** The DS2152 can move signaling across the user's backplane without firmware intervention, which unburdens the host from handling the real-time voice signaling and leaves it free to perform other functions.

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● **Per-Channel Conditioning:** The user can "groom" each DS0 channel independently as required, especially useful in Fractional T1 applications and for testing and provisioning DS0 channels.

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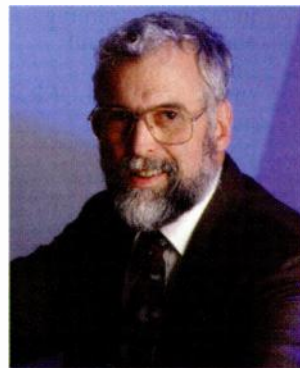
READER SERVICE 104

When Encryption Is Outlawed, Only Outlaws Will Encrypt

The Clinton Administration's efforts to control export of strong encryption by way of a key escrow recovery scheme have now been unmasked as a blatant attempt to control the domestic use of encryption by Americans as well. Never mind that this is quite possibly unconstitutional. That pales before the fact that it is simply impossible. Strong encryption is leaking out everywhere around the world and the government is caught on the horns of its own paradoxes.

Trying to restrict the export of encryption technology makes the rather bizarre assumption that Americans are the only people who can develop encryption. Heck, the Russians do a pretty good job of it, and anybody in the world can get it from them. A Russian company called Elvis+, in which Sun Microsystems has about a 10% interest, used Sun's SKIP protocol to develop a network security system software called SunScreen SKIP E+. The code was not developed in the U.S. and can be downloaded from <http://www.elvis-plus.com>. The Justice Department is reportedly "looking into" the matter.

An even stranger situation is the fact that Justice Department lawyers have conceded in court that, while it may be illegal to export encryption software in binary form on a disk or over the Internet, it is perfectly legal to export the printed source code in a book. This makes the further weird assumption that Americans are the only people who can type. Copies of the source code books for Phil Zimmermann's *Pretty Good Privacy* (PGP) have been mailed to a site in Norway where their 6000 pages are being scanned and will be compiled and made available for anyone to download. PGP 5.0 will be available for Windows 95, NT, and Macintosh. The site—<http://www.ifl.uio.no/pgp>—is rejecting any e-mailed or uploaded copies that may be sent to it. Since the code was legally exported on paper, what are the Feds going to do? Norway is probably not going to enforce U.S. export laws.



TOM WILLIAMS
EMBEDDED SYSTEMS/SOFTWARE

On top of all this, strong encryption is leaking out in products. Microsoft and Netscape have received special permission (what makes them so special?) to export 128-bit key encryption software to overseas banks. Phil Zimmermann's PGP Company has announced a deal with Qualcomm to integrate PGP into the latest release of the popular Eudora e-mail program. The as yet unbroken and unpatented Blowfish algorithm by Bruce Schneier is now in use in some 40 products. Some of these have encryption keys up to 448 bits long. Information on Blowfish is available at <http://www.counterpane.com>.

Federal courts are already working on cases involving First Amendment rights. Mathematics professor Daniel Bernstein received a sympathetic ear from the U.S. District Court in California when he argued that he was being illegally restricted from teaching his Snuffle algorithm, disclosing it at academic conferences, or publishing it in journals or on-line discussion groups without a license. If it's legal to publish Phil Zimmermann's source code, why is it illegal for Bernstein to publish his algorithms?

The government's desperate—and ultimately pathetic—attempts to read its citizens' mail and invade their privacy will only work against it. Successful restriction of the export of strong encryption will simply cede that lucrative market to foreign competition.

Restriction will not and cannot succeed. It can, of course, land selected individuals in a lot of trouble. However, the only effective restrictions will apply to companies and individuals who wish to conduct legitimate business. Terrorists and criminals will not be affected. Any American who wishes to may obtain and use strong encryption in e-mail with foreign Internet sites today. Any foreigner who wishes to may obtain and use strong encryption in e-mail with American Internet sites today. tomwillm@ix.netcom.com

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READER SERVICE 247

OLED Technology Energizes Flat-Panel-Display Development

It's been a few years since the concept of high-definition television (HDTV) on thin flat-panel displays (FPDs) that could hang on a wall was introduced. However, turning this concept into reality has become a much more daunting task than what was originally anticipated.

It's assumed that HDTV technology is well defined and understood, and that ultra-lightweight, ultra-thin FPDs exist. While the former, according to many experts, is still years away, the second half of the equation seems to be closer than first thought. This is due to a development by a team of scientists (from Princeton University in New Jersey and the University of Southern California) involving an independently controlled, tunable, three-color organic light-emitting device (OLED).

The technology hinges on a vertically stacked pixel architecture that can provide independent tuning of color, gray scale, and intensity. This is possible because within each color element of the LED, the primary colors red, blue, and green can be continuously and independently varied. This allows the device to emit any mixture of the constituent colors. Such an approach is a radical departure from the color wheel utilized by the more conventional CRTs, and is expected to produce very bright, intense true color displays with higher resolutions than previously possible.

Although the stacked architecture is itself an innovative advance, the components critical to its success are the highly transparent organic light-emitting diodes (TOLEDs). Their development ensued from the fact that because organic LEDs needn't be in a crystalline form to be deposited on a substrate, they could be layered much thinner than was ever possible beforehand. At such thickness, the scientists then could capture and leverage the OLEDs' transparency to radiation, which leads to significant improvements in brightness, energy efficiency, and cost effectiveness. Because of these benefits, the technology is being eyed as a future replacement technology for liquid crystal displays (LCDs). For further information, call the company at (610) 617-4010. CA

Design Guidelines Define Portable Digital Cameras

The increasing use of imaging in the desktop and portable PC environments has led to the creation of a multicompany standard for low-cost, easy-to-use PC-compatible digital still-image cameras. These cameras will allow users to capture, enhance, store, and share images with improved compatibility and ease of data handling. The Portable PC Camera '98 design guideline is supported by Intel Corp., Santa Clara, Calif., Hewlett-Packard Co., Palo Alto, Calif., Eastman-Kodak, Rochester, N.Y., and Microsoft Corp., Redmond,

Wash. It combines the use of Kodak's FlashPix file format with flash-memory-based electronic film cards, and the universal serial bus (USB) interface, along with MMX-enabled host CPUs and a digital still-image camera capable of 640-by-480-pixel resolution.

The FlashPix format is a platform-independent file architecture that was designed with the Internet in mind, allowing images to be opened quickly, easily edited, and saved quickly. The format includes calibrated color spaces and multiple image resolutions. To keep the camera simple and inexpensive, the guideline suggests that the camera consist only of the lens, image sensor, image capture logic with analog-to-digital conversion, simple compression logic that incorporates the proposed TIFF/EP compressed image format, and both a USB and a memory-card interface. The images captured by the camera are stored as electronic files using the proposed compression extension for TIFF files (TIFF/EP), which would become the equivalent of "digital negatives." All of the remaining image processing—image decompression, 8-bit to 24-bit interpolation, image enhancement/manipulation, and file formatting—will be done on the host MMX-enabled PC. The resulting file output, which is the image file format that's used for the FlashPix standard from Kodak, is an open standard that's available on the Kodak web site.

Software drivers from Microsoft are part of the recently announced Windows'98 and NT 5.0 operating systems—the still image architecture (STI). They also include support for both USB and 1394 serial interfaces. These drivers implement "push" model support (users can initiate action at the peripheral) as well as standard "pull" action (users at the host can initiate an action). For additional information on FlashPix, go to Kodak's web site: <http://www.kodak.com/daihome/flashpix/flashpix-home.shtml>; for the STI drivers, check out Microsoft's web site: <http://www.microsoft.com/hwdev/pcfuture>; and for Intel: <http://developer.intel.com/design/pc98>. DB

Joint Effort Targets Unified Verification Design Flow

Verification has become the most pressing concern for most ASIC designers, forcing EDA tool vendors to come up with workable verification solutions that can easily fit into today's design flows. Such solutions can be rather difficult to achieve, though, since design flows from one company to another can vary dramatically. On top of that, current verification solutions consist of a host of point tools that must somehow be interfaced. What designer has the time to worry about interfacing tools?

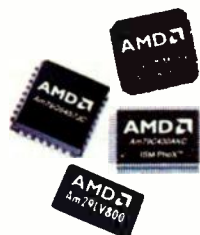
In an attempt to wade through the quagmire of disjointed solutions, Lucent Technologies, Murray Hill, N.J., and Precedence, Campbell, Calif., have joined forces in a three-year development effort to create a unified design flow for ASIC verification. Under the



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agreement, Lucent will purchase and standardize its design-verification environment on Precedence's simulation backplane software technology, SimMatrix Backplane. The two companies will then move to integrate Lucent's proprietary technology ATTSIM, a multilevel, mixed-signal, high-performance simulator, into the SimMatrix backplane using Precedence's Integration Design Environment (IDE). Consequently, users of the completed verification design flow will have access to an integrated multi-kernal solution, which will include as a bare minimum the V-system from Model Technology, Visual HDL from Summit Design, and NSIM from IKOS. This backplane and unified design flow will subsequently be distributed to groups within Lucent for use in designing high-end ASICs.

If successful, this technology agreement will serve as a model for future implementations of unified design and verification flows. Contact Precedence at (408) 345-4880; Internet: <http://www.precedence.com>. CA

Solutions Eyed For Hardware And Software Co-Verification

With more and more hardware and software components being embedded into IC designs, major issues surrounding component design and verification are unfolding. Looking to provide solutions for designers facing these issues, two EDA companies, Viewlogic, Marlboro, Mass., and IKOS, Sunnyvale, Calif., have joined forces in a technology agreement. Under the terms of the agreement, the companies will work together to develop high-performance co-development solutions for the design of embedded systems, as well as hardware/software co-verification solutions.

Many of the issues stem from growing complexity and shrinking market windows, placing tremendous pressure on designers to accelerate the integration of hardware and software—even before silicon prototypes are available. Traditionally, a hardware prototype has been required to verify the software. This meant that software developers had to wait until the hardware design was complete. But, when problems are found in the hardware prototype using this design scenario, they can be deadly both cost- and time-wise.

By concentrating on designing interfaces between a host of development and verification tools, the companies hope to show that hardware/software verification of traditional embedded systems as well as systems with Intellectual Property (IP) cores is possible using a high-performance virtual model of the hardware. With such an approach, software bottlenecks can be reduced substantially.

During the first phase of the technology agreement, interfaces will be developed for the EagleI and EagleV products from Viewlogic, coupled with the Voyager and Gemini mixed-level simulation products from IKOS. The next phase will focus on creating an interface to

IKOS' VirtuaLogic and Avatar in-circuit emulation products. For additional information, contact IKOS at <http://www.ikos.com> or (408) 255-4567. CA

Computers Will Have To Go Into Deep Freeze To Meet Goals

The industry's projected goal for the year 2007: gigascale integration. That means single high-performance chips with feature sizes of 0.1 μm and containing nearly 1 billion transistors, operating at 1 GHz. To reach that goal, according to Kenneth Rose, professor of electrical, computer, and systems engineering at Rensselaer Polytechnic Institute, Troy, N.Y., high-performance computers are going to have to get very, very cold. Rose said at an Electromechanical Society meeting in Montreal, Canada, that the move to gigascale integration in the next ten years makes it necessary to re-examine the potential of cryoelectronics—electronic devices that operate at extremely low temperatures.

Rose, who is a member of Rensselaer's interconnect research center, indicates that interconnects are a major limiting factor in the move to faster, more powerful computers. And, current proposed changes in interconnect materials and design can overcome some, but not all, of their limitations. But if the new chips are cooled to 77K (-196°C), they will meet the goals targeted for 2007: Testing has shown that it's possible to design chip packages that can dissipate sufficient heat to maintain this temperature.

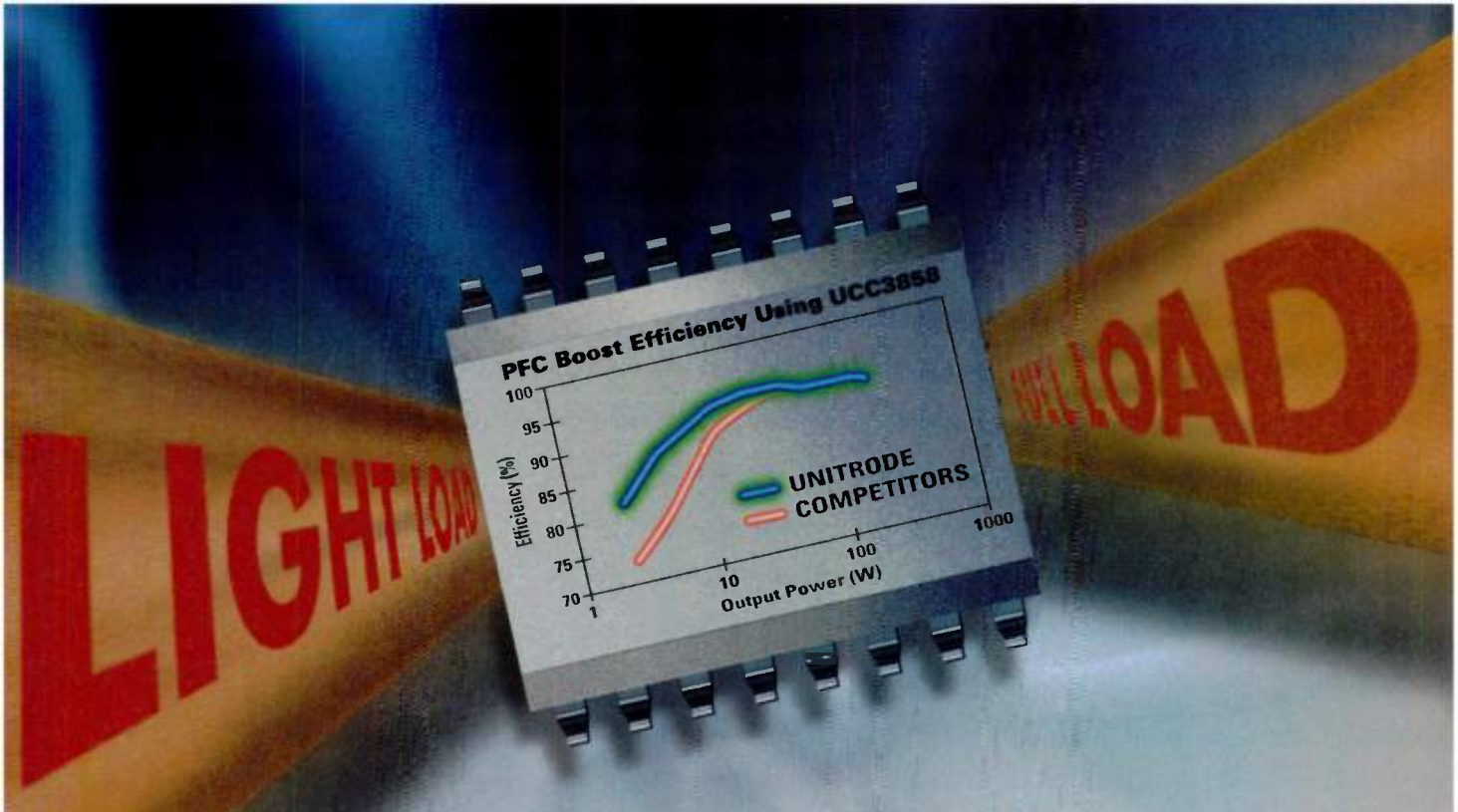
Interconnects, which are now made of aluminum, will switch to copper. This will offer about half as much electrical resistance. Replacing silicon dioxide insulation with polymers will accelerate the chip further. More resistance can be cut on the longest wires by making them fatter, with more wiring layers.

Cooling interconnects reduces resistance because of changes that occur on the atomic level, i.e. eliminating lattice-structure vibrations. Refrigeration was considered by industry before, but other approaches were taken. Nonetheless, gigascale integration is pushing materials to their limits, which seemingly makes cryoelectronics one of the best options.

Cost-effective, compatible cooling is critical if cryoelectronics is to be successful, says Rose. The package that holds the chips must dissipate heat more efficiently than any packages now being used. In conjunction with Intermagnetics General, which manufactures superconductors, Rose created a nine-chip silicon package can do just that. Microchannels 100 μm wide and about 200 μm deep help remove heat. As mentioned before, the package was successfully tested at 77K in liquid nitrogen. At this temperature, the resistance on the interconnects would be cut by at least a factor of six.

For more information, call (518) 276-2981; e-mail: kröse@unix.cie.rpi.edu. RE

Edited by Roger Engelke



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Sophisticated Techniques Are Being Applied To Lower Voltage And Power Levels For Analog ICs

Most designers trying to lower IC power levels beyond those reached by cutting the supply-voltage rails, and/or trying to recover the speed lost by that supply voltage cut, are doing so by working on digital logic. They are using sophisticated circuit techniques such as adiabatic logic

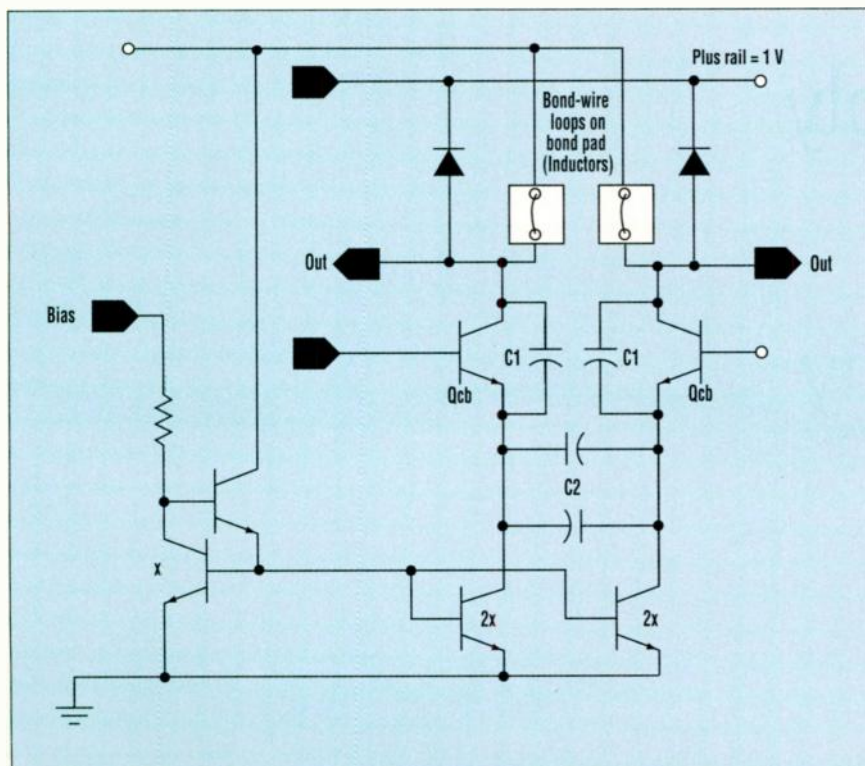
(also called charge-recovery logic) and process-based multithreshold CMOS. A few brave souls have now taken some of these techniques with conventional analog functions by using a few of the same circuit tricks.

For example, designers from the Massachusetts Institute of Technol-

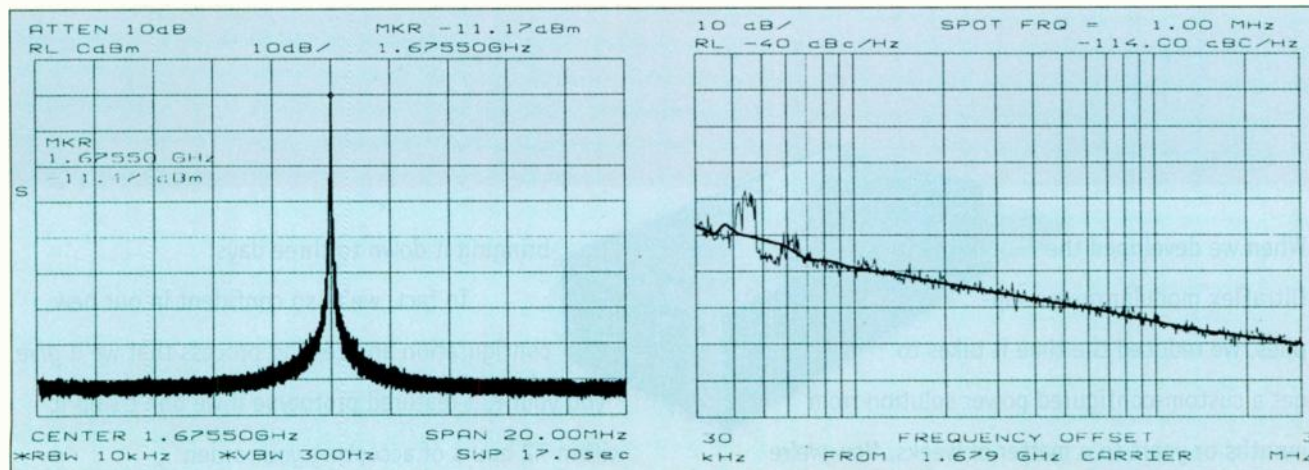
ogy (MIT), Cambridge, Mass., and Analog Devices Inc., Wilmington, Mass., have come up with a voltage-controlled oscillator (VCO) on a single chip, including the resonator, that runs at 1.8 GHz. Moreover, it dissipates just 5 mW running off a 1-V power supply—one of the “analog-only tricks” employed that helped get the resonator on the chip. The team used bond wires as inductors to get the circuit’s “Q” or “quality factor” to a practical value relative to that achieved by spiral inductors printed on oxide over silicon substrates (Fig. 1). In addition, they reduced noise (jitter) by impedance matching in the feedback circuit (Fig. 2). As a result, the output spectrum of the VCO is very narrow, and phase noise runs at -114 dBc/Hz.

A team from Oregon State University, Corvallis, developed a 4-stage CMOS op amp that runs off 1.8 V. It’s a true op amp providing a stable gain of over 110 dB coupled with a unity gain bandwidth of 21 MHz at a phase margin of 68°. It dissipates just 19 mW while running off a 2-V rail.

In addition, a team from Analog Devices built a 13-bit digital-to-audio converter (DAC) that, while running at an update rate of close to 50 kHz, took just 0.6 mW from a 3-V supply rail. Basically a binary weighted charge redistribution DAC, it is built from an 8-bit course DAC overlapped



1. This 1.8-GHz voltage-controlled oscillator (VCO) contains a 2.1-nH on-chip inductor sporting a Q of 13. It was built from loops of bond wire 2-mm long bonded to pads at each end.



2. The output of a spectrum analyzer shows the 1.8-GHz voltage-controlled oscillator (VCO) to be virtually free of phase noise. This makes it suitable for use in low-power RF transceiver front ends.

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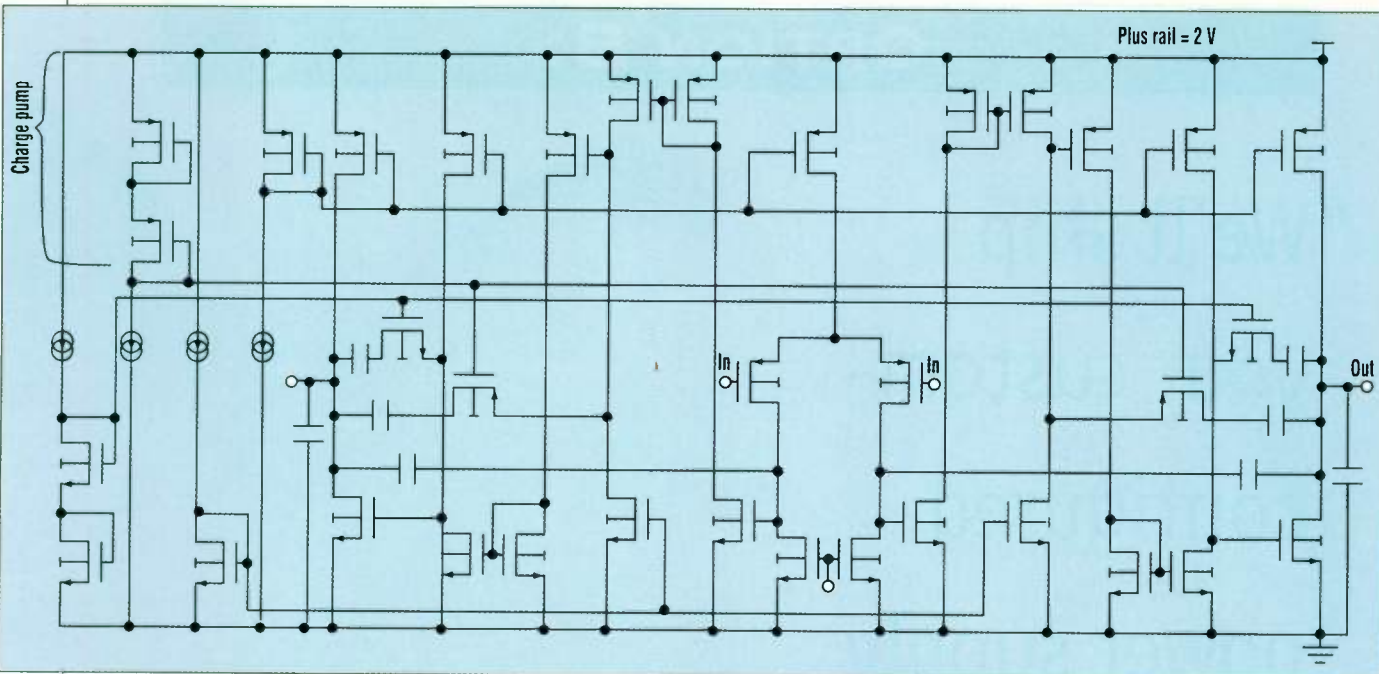
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3. This low-power CMOS op amp employs 4 cascaded stages. An internal charge pump raises their common-mode voltage (CMV).

with a 10-bit fine DAC to get 13-bits of resolution.

A 5-mW 1.8-GHz VCO

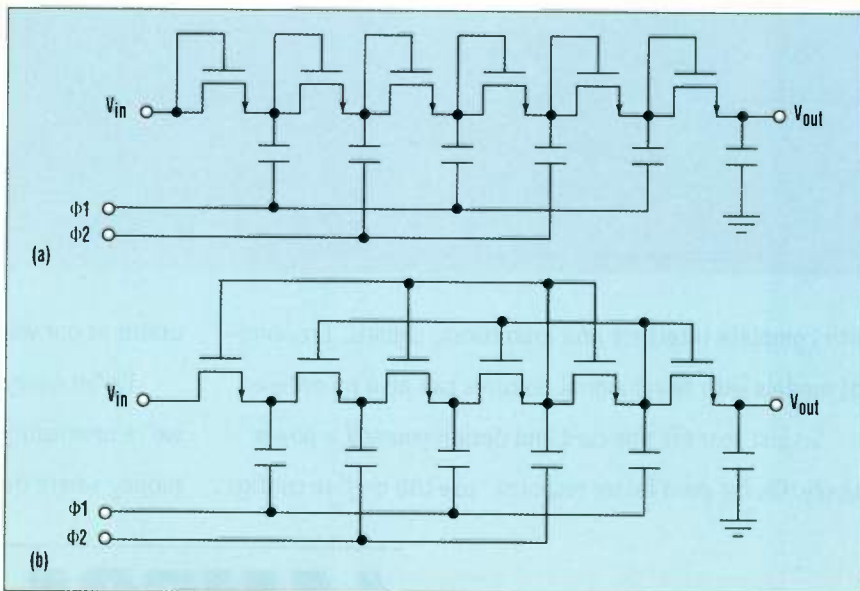
As portable wireless communication products have become high-volume consumer devices operating in the 1-to-2-GHz band, there has been a push to integrate RF front-end circuits in high-yield silicon IC processes. VCOs remain a basic element in most RF transceivers, and their performance (output noise spectrum) can severely limit the capabilities of wireless data transmission systems. Therefore, any well-integrated VCO must sport both low noise and low power.

The MIT/Analog Devices VCO design team had access to Analog Devices' ADRF bipolar process, which offers the designer a veritable cookie jar of devices including double-polysilicon npn transistors with a cutoff frequency (f_t) of 25 GHz, n+ capacitors, and two levels of aluminum-copper (AlCu) metallization. The design team preferred tried-and-true bipolar junction transistors (BJTs) for this application because they sport a lower noise figure at the operating frequency for a given level of power consumption relative to that available from today's high-speed CMOS processes. The team concluded that a VCO with the desired minimum noise should be possible at lower power with BJTs.

The trick was to get an inductor with a high enough Q, because in a typical oscillator, phase noise is inversely proportional to the square of the Q factor. (It should be noted that Inductor Q = the ratio of the inductor's reactance to its resistance or XL/R .) Typically, the way to integrate an inductor is to deposit a spiral inductor on a layer of oxide that has been grown on the silicon substrate. However, many processes cannot produce high-Q inductors—the resistance is too high and the resistance of the sub-

strate below the oxide provides a parasitic resistance that looks like it is in series with the coil. The parasitic resistance is coupled to the substrate by the oxide's parasitic capacitance.

A few processes with some combination of a very-high-resistance substrate, multiple, metal (ideally gold) layers, and maybe a thicker layer of oxide have produced Qs of 10 to 15. The MIT/Analog Devices team discovered all their process could achieve at 1.8 GHz, for inductances up to 11 nH, was a Q of only 2 to 5. Therefore, they moved



4. The efficiency of a classic Dickson charge pump (a) was increased by the circuit of (b).

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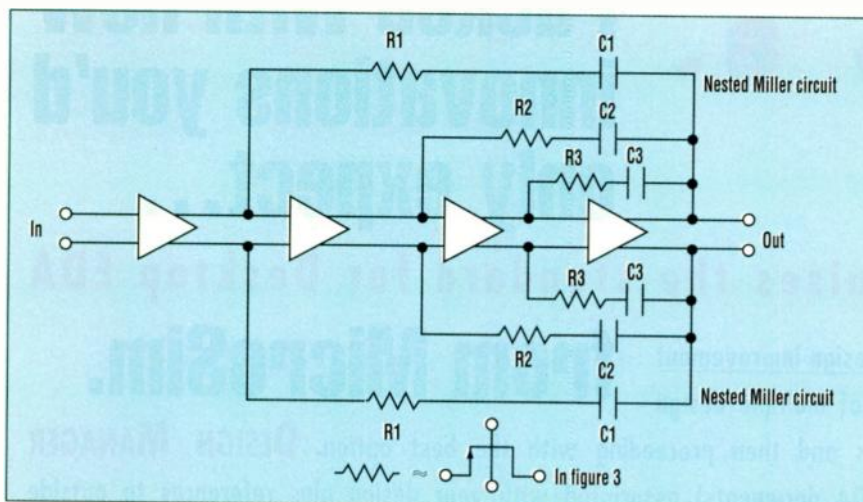
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5. The resistors in the nested Miller frequency compensation circuit consist of p-channel MOSFETs.

to another approach. They used loops of bond wire, bonded at both ends to a bonding pad. Using 1-mil (25.4- μm) aluminum bond wire 3-mm long created inductances with values between 0.7 and 4.5 nH with Q s between 11 and 15 at 1.8 GHz (Fig. 1, again.)

For the VCO itself, they built a one-port structure consisting of two parallel bond wires, each 2-mm long and connected by the top metal at one end. Including self-inductance, mutual coupling, and parasitic capacitance, the final device yielded a 2.1-nH inductor sporting a Q of 13 at 1.8 GHz. Simulation revealed that allowing for skin effect and the coil's resistance of 0.8 Ω , a Q of 28 should result. This suggests that the substrate effects remain significant. Consequently, while the Q of bond-wire inductors rises with their height above the chip, they also may benefit from thicker oxide. Of course, the sticking point here may be the molding of the IC. The molding process could really move the inductor around and change its Q .

As noted earlier, to further cut phase noise and create a clean spectrum, the researchers impedance-matched the positive-feedback loop created by capacitors C_1 , C_1 , and C_2 (Fig. 1, again). Optimizing the loop minimizes noise and helps create the VCO's low-jitter spectrum analyzer curves of Figure 2. The VCO tunes smoothly (almost linearly) from 1.64 GHz to 1.69 GHz with a control voltage from 0 to 5 V.

A 19-mW 1.8-GHz Op Amp

It's virtually impossible to design low-voltage, single-cascoded-stage, op

amps running off supply rails as low as 1.8 V. However, as noted earlier, a team from the Oregon State University came up with a high-performance device in a 0.6- μm n-well CMOS process. They came up with an op amp consisting of four cascaded stages using "nested Miller" compensation (Fig. 3). This amplifier employs a unique charge-pump circuit that performs two functions. It raises the amplifier's common-mode voltage (CMV) bringing it closer to the supply rails. In addition, it tracks the effects of process variations, temperature, and supply-voltage variations on the compensation components.

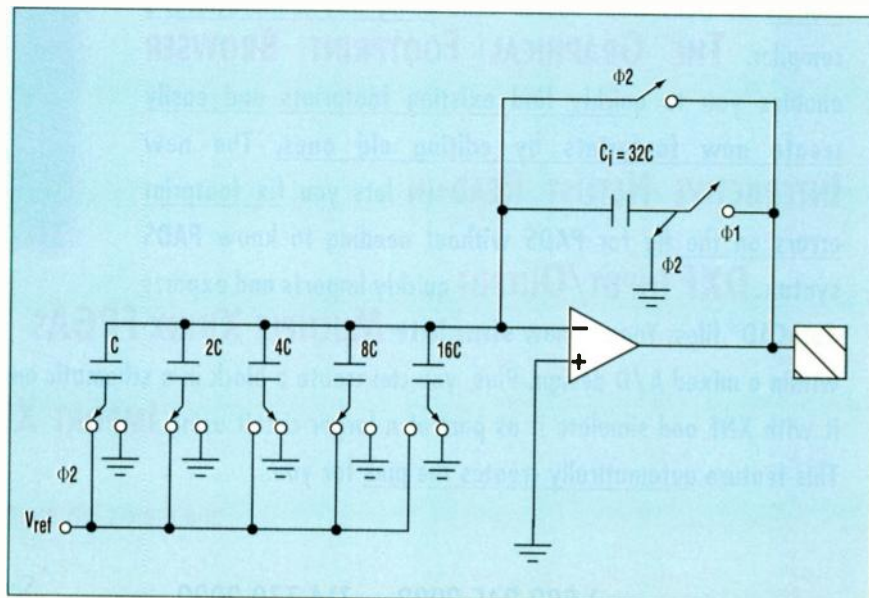
The team upped the efficiency of the classical Dickson charge pump by pro-

viding first-order clock-feedthrough cancelation op amp (Fig. 4). The nested Miller frequency compensation in the 4-stage design requires six capacitors and six MOSFETs which act as variable resistors (Fig. 5). The process-sensitive charge pump output is applied to the gate of each MOSFET to stabilize the nested Miller frequency compensation. Simulation indicated the charge pump raised the CMV 145 mV when running off a 1.2-V rail. Upping the CMV by 145 mV increases the available overhead by 12%.

A 0.6-mW 45-kHz 13-Bit DAC

Switched-capacitor (charge-redistribution) technology has been largely avoided in the design of general-purpose DACs because of the need for clock circuits and to avoid switching noise on the continuous-time output. Instead, most work has focused on switched-current and resistive-ladder DACs. However, in most of today's mixed-signal ICs, polysilicon capacitors provide the best component matching per unit area. Therefore, it makes sense to use polyoxide-polysilicon capacitors in a high-resolution converter. For highly-integrated mixed-signal ICs, where a clock is readily available, a capacitor-based DAC can save area and power relative to one based on matching currents or voltages in transistors and/or resistors.

The Analog Devices team came up with a design technique suitable for im-



6 This basic 5-bit charge-redistribution digital-to-analog converter (DAC) moves charge from the 5 input capacitors to the integrating capacitor C_f .

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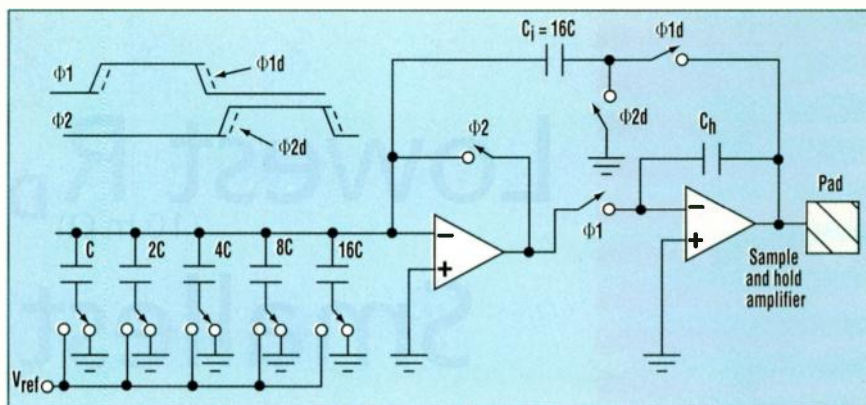
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7. This complex 5-bit charge-redistribution DAC contains a zero-order sample-and-hold amplifier that autozeros the output.

plementing a low-power, small-area, high-accuracy switched-capacitor DAC. In a this type of DAC, samples of charge proportional to the unit capacitor value C , the reference voltage V_{ref} , and the digital input word, are sampled onto the array of input capacitors during phase 2 (Fig. 6). During $\Phi 1$, charge from these input capacitors is integrated onto the integrating capacitor C_i to generate an output proportional to the digital input word.

The switch in parallel with C_i performs two functions: It removes charge from the integrating capacitor on a sample-by-sample basis, and it auto-zeroes the amplifier, preventing the op amp's offset voltage from appearing at the output. The converter still needs a sample-and-hold amplifier (SHA) to remove each charge sample from the integrating capacitor to avoid putting the "reset" voltage on the output at every cycle.

The DAC team's SHA adds a second op amp to perform the "HOLD" function (Fig. 7). It allows the output to be held at its previous value while the integrating capacitor is being reset. During $\Phi 2$, when the previous output value is being removed from the integrating capacitor, the output is held constant on the hold capacitor C_H . When a new word is to be evaluated during $\Phi 1$, the two op amps are cascaded forming a two-stage op amp. The hold capacitor forms the two-stage op amp's compensation capacitor.

To put it another way, the new circuit now looks exactly like the circuit in Figure 6. That is, during phase 2, the first half of the amplifier auto-zeros the DAC while the second half of the amplifier holds the continuous-time output stable at the previous value. The sec-

ond op amp's offset gets divided by the gain of the first stage when referred to the input.

The auto-zero function also removes the amplifier's low-frequency $1/f$ noise because it performs a correlated double-sampling of the first op amp's input referred noise. The circuit also drives the output directly, eliminating the need for an additional amplifier. As if that were not enough, the switched-capacitor DAC itself consumes no static power. That is, this analog technique that has been redistributing charge for some 20 years inherently employs techniques just now coming of age in the digital arena (adiabatic logic moves charge around rather than throwing it away.)

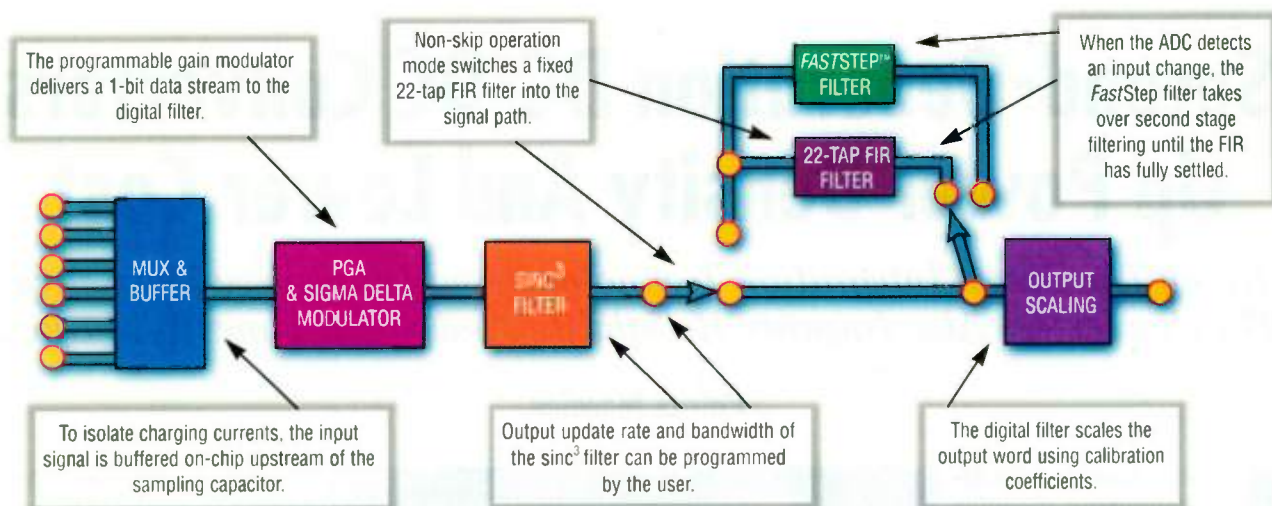
The 13-bit DAC looks similar to the 5-bit circuit of Figure 7 except that an 8-bit DAC has been added between the two op amps, and the zero-order SHA performs deglitching. In addition, the integrating capacitor and the parasitic capacitance at its output is precharged, further cutting power.

The three developments were described at the International Symposium on Low Power Electronics '97 (ISLPED'97) at the Monterey Convention Center, Monterey, Calif.

For more information on the VCO, contact Don Hitko of MIT at (617) 258-8142; e-mail: dahitko@mtl.mit.edu. For more information on the charge-pump op amp, contact D.J. Allstot of the Dept. of ECE, Oregon State University at (541) 737-6739; e-mail: allstot@ece.orst.edu. For more information on the DAC, contact Lapoe Lynn of Analog Devices at (617) 937-1315. e-mail: lapoe.lynn@analog.com.

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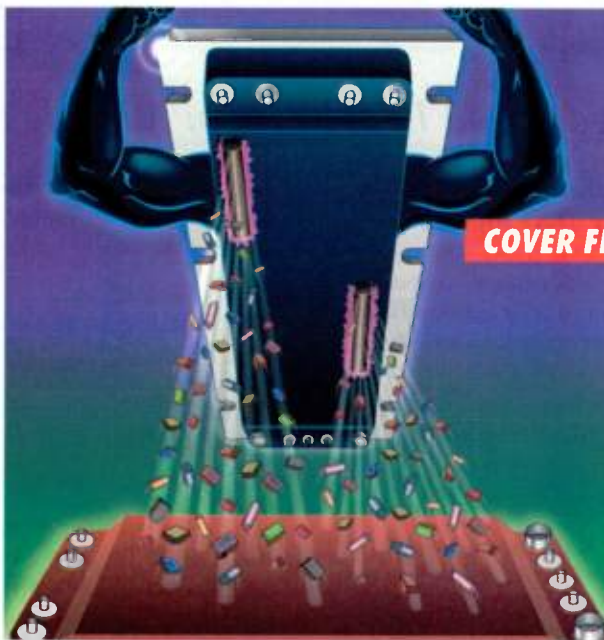
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Patrick Mannion

Although high-density dc-dc converter modules have been popular since their introduction in the mid-80s, the inherent limitations of their basic designs have been a major handicap in terms of power density, cost, and turn-around time. To exacerbate the situation, the rocketing demand for these devices in increasingly varied and demanding applications has maxed out the original design to the extent that nothing short of a complete redesign is required.

Stepping up to the challenge, Vicor Corp., Andover, Mass., has introduced what it defines as the "second generation" of dc-dc power modules, called the VI-300 series. Based on the company's patented zero-current-switching (ZCS) and zero-voltage-switching (ZVS) power-processing architectures, the modules incorporate recent advances in control integration, packaging, magnetics, and noise and thermal management. The end result brings the devices closer to the "ideal power component" with a tripling in power density, higher reliability, lower cost, and faster time to market.

The converters come in a number of standard versions, and are an integral part of the company's overall Concept 300 strategy, which includes advanced factory and design automation. Plans for the near future include making the



COVER FEATURE

modules available in an unlimited variety of standard versions, to the extent that the line between custom and standard modules will become almost indistinguishable.

First-Generation Power

While first-generation converters, or power components, provided many benefits at the time, including reduced size and faster time-to-market, their relatively high cost and inability to break the 100-W/in.³ barrier limited their widespread use in mainstream markets. In addition, first-generation power-converter manufacturers had

to adapt the concept of the product to available manufacturing technologies. As a result, few of the processes used in their manufacture are specifically tailored for power devices. For example, the surface-mount technology used to mount the over 200 components in a typical first-generation converter has been borrowed from mainstream electronic manufacturing, while the magnetic structures used are often slightly modified, 30-year-old pot-core technologies and carryovers from telecom applications. As such, they were designed to process signals, not power, so they tend to limit power density while adversely affecting noise and heat man-

agement. In addition, the generic TO-220 packages used for the switching devices limit mounting options and are plagued with excessive parasitic inductance and capacitance, again leading to high noise levels.

The limits of first-generation power components were stretched and pulled to suit popular applications such as telecom, industrial, ground-based military, and high- to mid-range electronic data procession (EDP), and other areas that could afford the custom modifications. As applications expand into other systems, including low-end, high-volume EDP and busi-

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READER SERVICE 149

WB

ness equipment, the unsuitability of these devices, in terms of power density, ruggedness, cost, and turnaround, has become obvious.

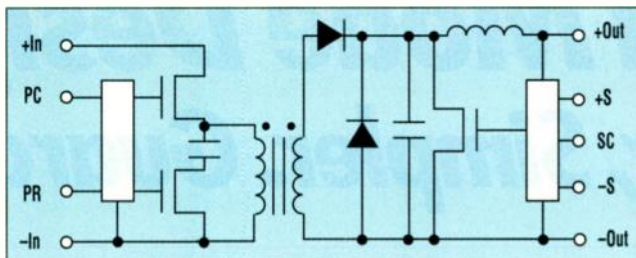
Complete Redesign

To overcome the constraints of first generation power components, Vicor started from scratch with a design based on its patented ZCS/ZVS high-efficiency, low-noise, high-frequency power-processing architecture (Fig. 1). A complete redesign of the control, magnetic, switching, and packaging elements of the modules has resulted in a component with a power density of up to 120 W/in.³ in three package sizes—maxi (4.6 by 2.2 by 0.5 in.); mini (2.28 by 2.2 by 0.5 in.); and micro (2.28 by 1.45 by 0.5 in.).

The modules have one-third the number of parts of their predecessors and can be ordered pre-configured in nine input ranges, and nine output voltages. Resistors can be used to trim up or trim down the output voltage if necessary. Custom models can be ordered with any input voltage from 4.5 to 450 V, any output voltage from 1 to 100 V, and at any power level up to 600 W. Two pin styles, four baseplate options, and a variety of data collection and reporting options are available. The devices have an operating temperature range of -55° to over 110°C and come in three product grades—C, T, and M. User-defined grades also are available.

Other specifications include a no-load to full-load regulation of 0.1%, a programmable output of 10% to 100%, conversion efficiencies of up to 92% depending on the voltage combination and power level chosen, and an input-to-output isolation voltage of 3000 V rms. All models are parallelable with N+M fault tolerance and current sharing, and are phased-array-control compatible. Paralleling architectures include dc- and ac-coupled single wire.

The end result, as far as the power-supply designer is concerned, is a high-power-density component, with a wide range of options, and with high reliability, that reduces the cost of a power supply from \$0.50 to \$2/W down to \$0.25 to \$1/W (see the table).

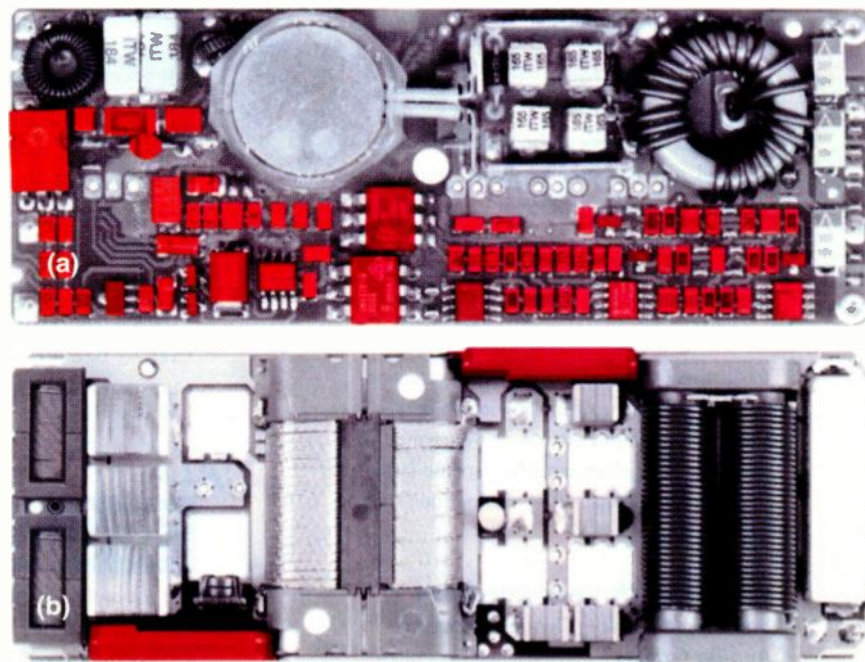


1. The VI-300's ZCS/ZVS power-processing architecture enables efficient, low-noise, high-frequency operation. The main switch is common drain for improved thermal and noise management, the reset switch is common source for ease of control, while a secondary reverse boost switch narrows the frequency range and allows for synchronous rectification.

Key to the VI-300 converter's design is its high level of component-level integration (Fig. 2). With the aid of hybrid technology and a Class 10,000 clean room, the device packs all control functions and active circuitry into two (primary and secondary side) ICs occupying a total volume of less than 1/10 in.³ each. As a result, the parts count has been slashed from the typical 115 to 200 parts of first-generation components of down to 35. The ICs, or "brains," are molded and include a copper plate that is soldered directly to the baseplate to provide a thermal escape path to the baseplate. The devices are

the traditional potted-core magnetics with their primary and secondary windings laid concentrically on top of one another (Fig. 3). This close proximity of input to output, necessary for efficient magnetic coupling, also can lead to electrical coupling of primary to secondary windings via parasitic capacitance. This coupling can result in unacceptable levels of common-mode noise.

With second-generation devices, the potted-core design has been replaced by proprietary plated-cavity cores that use copper armor, plated onto the ferrite core, to more closely confine the magnetic flux to couple widely sepa-



2. The control circuitry in the first-generation power module, marked red in (a), has been integrated into two (primary and secondary side) ICs, or "brains," marked red in the second-generation module, (b). The end result is a reduction in parts from a typical 115 to 200 down to 35, with the ensuing savings in cost and increase in reliability. The scheme also provides extra room for the power train.

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MicroPower, Precision CMOS Op Amp, $I_Q=20\mu A/\text{Chan.}$	OPA336	OPA2336	OPA4336	11380	350
Precision Single-Supply Op Amp, $I_Q=250\mu A$		OPA234		11318	351
MicroPower, Single-Supply Op Amp, $I_Q=350\mu A/\text{Chan.}$	OPA237	OPA2237	OPA4237	11327	352
Low Distortion, Wideband Op Amp, 450MHz	OPA642			11190	353
Low Distortion, High Gain Op Amp, 900MHz	OPA643			11191	354
Wideband, Unity-Gain Stable Op Amp, 560MHz	OPA650	OPA2650		11264	355
Wideband, Gain ≥ 2 Op Amp, 950MHz	OPA651			11265	356
Wideband Current-Feedback Op Amp, 900MHz	OPA658	OPA2658		11268	357
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A/D Converters			MSOP-8	(800) 548-6133 FAX LINE#	Reader Service #
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12-Bit, Bipolar, Serial Output—200kHz Sampling A/D Converter at 2.5mW			ADS7817	11369	360
12-Bit, Unipolar, Serial Output—75kHz Sampling A/D Converter at 0.6mW			ADS7822	11358	361

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rated primary and secondary windings. The wider separation provides greater isolation and therefore lowers input-to-output parasitic capacitance and noise. The plated cavity also serves to conduct heat away from the transformer to the baseplate, thus increasing the power-handling capability of the power train allowing the transformer to handle a power density of 1000 W/in.³, with a 30°C rise.

The power-train assembly itself is contained between the baseplate and a terminal block assembly, with input and output pins recessed. The modules may be wave-soldered or plugged into inboard or surface-mount terminals. Proprietary sockets handle up to 100 A.

Switching Elements

The switching elements, mounted to the baseplate, have done away with the TO-220 package with its high parasitic inductance and capacitance and high thermal impedance. Instead, the VI-300 devices use a proprietary, low-noise, integrated power device (IPD) that has an order of magnitude lower parasitic effect.

The IPDs are soldered to 20-mil-thick, electrically and thermally conductive, primary and secondary shields, inset within the grounded aluminum baseplate. In addition, the thermal path from the MOSFET die to the baseplate has been reduced through the elimination of a number of layers and the use of materials such as kapton, in place of epoxy and a Faraday shield. This shortening of the path has helped reduce the thermal impedance from junction to baseplate

The advances made in the converters are backed by equally significant advances in the methods used to manufacture them.

($R_{\theta JB}$) from the 3°C/W typical of the VI-200, to 1.5°C/W for the VI-300.

The advances made in the overall design of the VI-300 have been complemented by equally significant advances in the technology used to manufacture them. Instead of the generic assembly lines that have simply been adapted for power components, Vicor has invested in a custom, fully automated assembly line specifically designed for the assembly of second-generation power components.

The second-generation factory is designed to accommodate four lines and ancillary processes, with a theoretical total capacity of one module every two seconds. According to Vicor, the total cycle time, when the line

is fully up and running, is predicted to be approximately four hours.

To further augment its VI-300, and follow through on its Concept 300 strategy, Vicor has created a user interface, called the Vicor Design Assistance Computer (VDAC), that will run from the customer's site and give the customer the flexibility to spec components from a remote location at any time of the day or night. Between the factory floor and VDAC lies the ABM which automatically generates the necessary bill of materials. The ABM communicates directly with the computer-integrated manufacturing process to produce the required product, in quantity, in a matter of days.

PRICE AND AVAILABILITY

The maxi module, 600 W, 375-V (250 to 425 V) input, 48-V output, is priced at \$248. The mini module, 300 W, 375-V (250 to 425 V) input, 12-V output, is priced at \$148. The micro module, 150 W, 48-V (36 to 75 V) output, is priced at \$112. Standard modules are shipped in four to eight weeks in quantity. For more information, contact Vicor Express at (800) 735-6200.

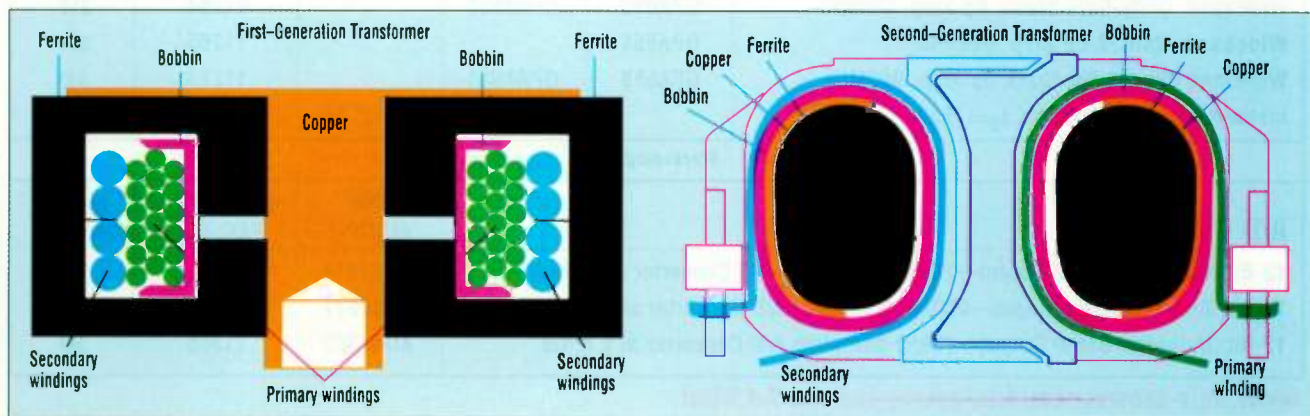
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HOW VALUABLE

HIGHLY
MODERATELY
SLIGHTLY

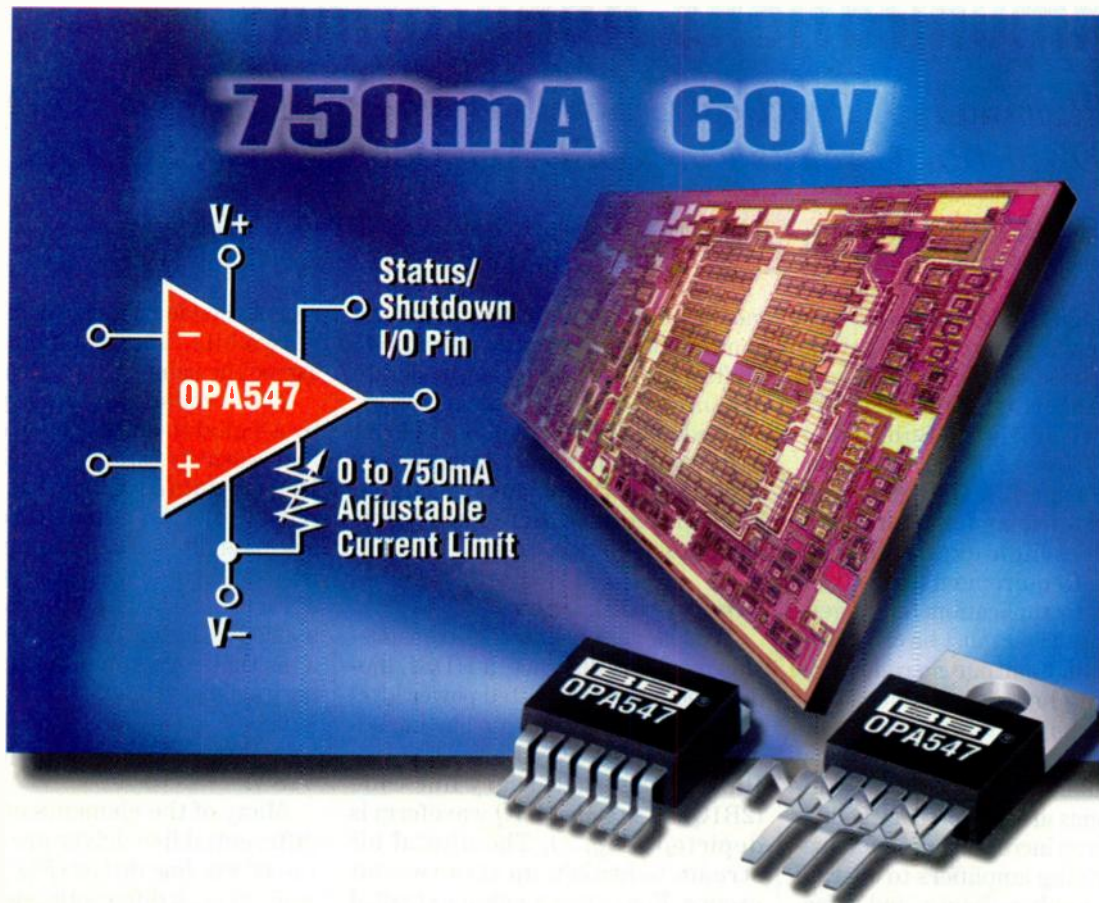
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3. With primary and secondary windings concentrically on top of each other, first-generation transformers achieved adequate magnetic coupling. However, electric coupling due to parasitic capacitance can lead to excessive common-mode noise. To avoid this, second-generation transformers place the primary and secondary windings far apart, but contain the magnetic flux using a copper armor plated onto the ferrite core. The armor also conducts excess heat to the baseplate.

Power Op Amp!



OPA547—simple to use and it packs power with a peak output of 750mA (500mA continuous). It's ready-made for driving heavy loads such as motors, valves, solenoids, speakers, or as a programmable V/I source.

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More Control

OPA547 gives you more control over your high output current circuitry. Current limit and thermal shutdown protect it from overload. A single low power resistor, potentiometer, or a programming voltage sets the current limit. A logic output signal

on the status I/O pin tells you if thermal shutdown has occurred. You can even apply a logic signal to this same pin to shut down the amplifier, forcing the output stage to a high impedance state and reducing the quiescent current. The easy-to-use OPA547 has the options you need to control your high power loads.

Key Specifications

- Output Current750mA peak, 500mA continuous
- Output Voltage at 100mA.....(V_-)+0.8V to (V_+)-1.5V
- Supply Voltage.....8V to 60V single supply
- Slew Rate.....6V/ μ s
- Packages: 7-lead DDPack surface mount and 7-lead TO-220
- Priced from \$4.08 in 1000s

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Line-Driver Design For Broadband Communications Applications

Following Is A Practical Guide To Designing, Low-Power, Low-Distortion Circuits For XDSL And Cable Modem Systems.

EAMON NASH, Analog Devices Inc., 804 Woburn St. Wilmington, MA 01887; (617) 937-1239, e-mail: eamonnash@analog.com.

Even though highly integrated chip sets for wired communications standards such as High Bit-rate Digital Subscriber Line (HDSL), Asymmetrical Digital Subscriber Line (ADSL), and HFC are being implemented using LSI CMOS technology, the line-driving function generally requires high-quality bipolar amplifiers. Requirements vary from application to application, but in general, the line driver must be capable of delivering high-output current while maintaining low signal distortion. Bipolar technology is generally favored by IC designers when designing such amplifiers. However, because today's modems are predominantly digital, there is an increasing need for analog line-driving amplifiers to operate from low supply voltages, and sometimes from single supplies.

Within these constraints, the line-driver designer has a number of architectural degrees of freedom that make the design task a little easier. If a high signal swing (compared to the supply voltage) is required, differential line driving can be used to double the available peak-to-peak voltage of the signal. If transformer coupling is necessary, a step-up or step-down transformer can be used to optimize signal size. However, this does change the current demand on the amplifier.

In power-critical applications, component selection is not a trivial matter of finding devices with low quiescent current. In considering the "total" power consumption of the driver, one has to look at the quiescent power consumption, the power delivered to the load, the dynamic power, or the power that the amplifier must consume to deliver the requisite power to the load.

HDSL is becoming popular as a

means of providing full duplex data communication at rates up to 1.544 Mbits/s (2.048 Mbits/s) over moderate distances via conventional telephone twisted-pair wires. Traditional T1 (E1 in Europe) requires repeaters every 3000 to 6000 ft. to boost the signal strength and allow transmission over distances up to 12,000 feet.

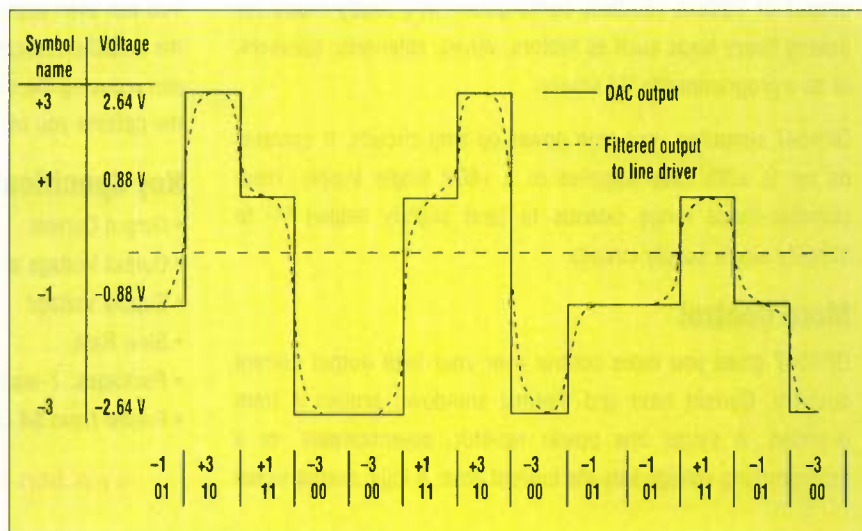
Driving HDSL Lines

To achieve repeater-less transmission over this distance, a HDSL modem requires transmitted power level of +13.5 dBm (assuming a line impedance of 135 Ω). HDSL uses the Two Binary One Quaternary line code (2B1Q). A sample 2B1Q waveform is depicted (Fig. 1). The digital bit stream is broken up into two-bit groups. Four analog voltages (called quaternary symbols) are used to rep-

resent the four possible combinations of two bits. These symbols are assigned the names +3, +1, -1, and -3.

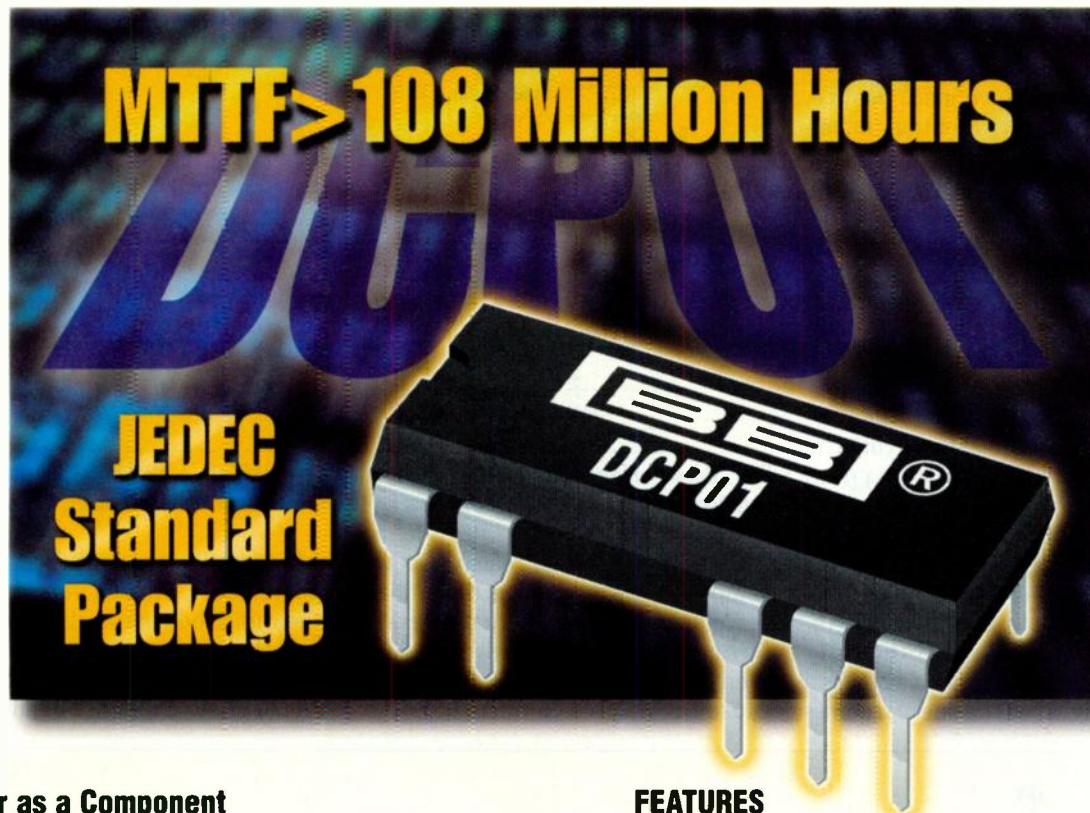
These voltage levels are produced by a digital-to-analog converter (DAC) that is usually part of an Analog Front End Circuit (AFEC). Before it's applied to the line, the DAC output is low-pass filtered and acquires the sinusoidal form shown in the dotted line of Figure 1. The filtered signal is then applied to the line driver. The line voltages that correspond to the quaternary symbols +3, +1, -1, and -3 are 2.64 V, 0.88 V, -0.88 V, and -2.64 V. This results in a peak-to-peak line voltage of 5.28 V.

Many of the elements of a classic differential line driver are shown in the HDSL line driver (Fig. 2). A 6-V peak-to-peak differential signal is applied to the input. The differential gain



1. Data transmitted on HDSL lines are coded with 2B1Q (2 bits 1 Quaternary) which consists of 4 discrete voltage levels. Each level or symbol corresponds to a 2-bit sequence. The discrete voltage levels are produced by a DAC, filtered and applied to a line driver. The line driver must deliver a peak-to-peak voltage amplitude to the line of 5.28 V to the line. This corresponds to a power level of +13.5 dBm ($R_L = 135 \Omega$).

Isolated DC/DC Converters



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- -40°C to +100°C Operation
- Remote On/Off
- Synchronizable
- No Derating
- 1W Output
- 14-Pin PDIP



Products	V _{IN}	V _{OUT}	Efficiency	Isolation	Switching	Package	(800) 548-6133 FAX/LINE#
DCP010505P	5V	5V	71%	1000Vrms	400kHz	14-Pin PDIP	11336
DCP010512P	5V	12V	72%	1000Vrms	400kHz	14-Pin PDIP	11366
DCP010515P	5V	15V	73%	1000Vrms	400kHz	14-Pin PDIP	11367
DCP010505DP	5V	±5V	71%	1000Vrms	400kHz	14-Pin PDIP	11336
DCP010512DP	5V	±12V	72%	1000Vrms	400kHz	14-Pin PDIP	11357
DCP010515DP	5V	±15V	75%	1000Vrms	400kHz	14-Pin PDIP	11356
DCP011512DP	15V	±12V	76%	1000Vrms	400kHz	14-Pin PDIP	11382
DCP011515DP	15V	±15V	76%	1000Vrms	400kHz	14-Pin PDIP	11382
DCP012405P	24V	5V	65%	1000Vrms	400kHz	14-Pin PDIP	11383
DCP012415DP	24V	±15V	76%	1000Vrms	400kHz	14-Pin PDIP	11383

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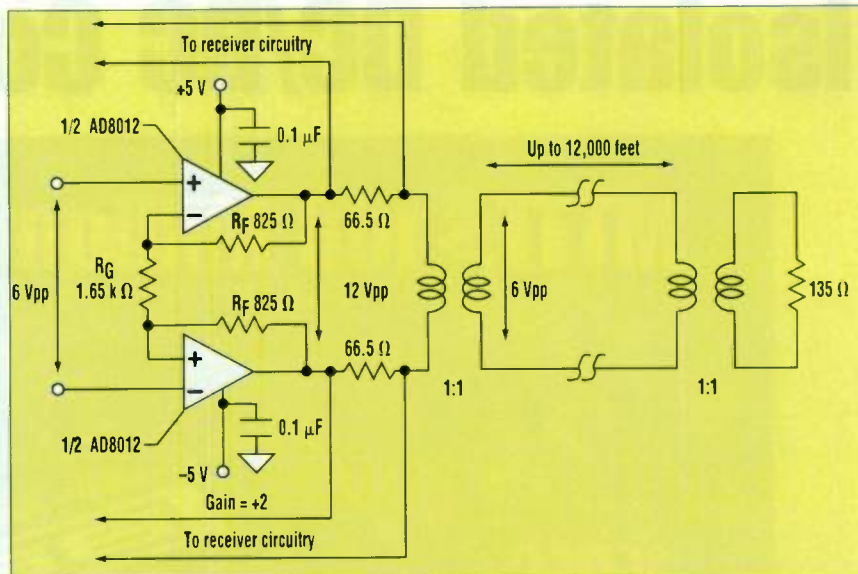
READER SERVICE 82

of the amplifier ($1+2R_F/R_G$) is set to +2, so that the resulting differential output signal is 12 Vpp.

As is normal in telephony applications, a transformer galvanically isolates the differential amplifier from the line. In this case, a 1:1 turns ratio is used. To correctly terminate the line, it is necessary to set the output impedance of the amplifier to be equal to the impedance of the line being driven (135 Ω in this case). Because the transformer has a turns ratio of 1:1, the impedance reflected from the line is equal to the line impedance of 135 Ω ($R_{REFL} = R_{LINE}/\text{Turns Ratio}$). As a result, two 66.5- Ω resistors correctly terminate the line.

The immediate effect of back-termination is that the signal from the amplifier is halved before it is applied to the line. This doubles the power that the amplifier must deliver. On the other hand, the back-termination resistors also another important role.

Full-duplex data-transmission systems like HDSL simultaneously transmit data in both directions. As a result, the signal on the line and across

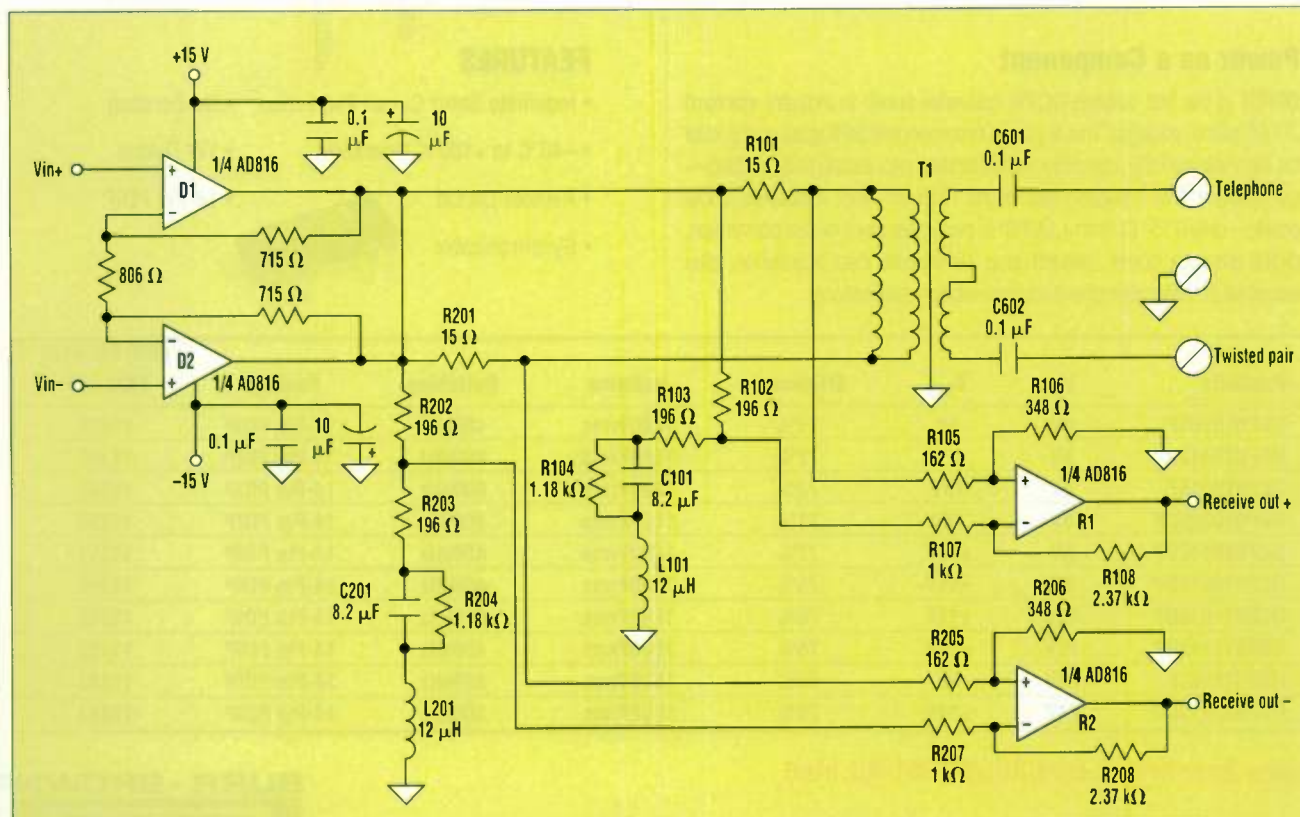


2. A "classic" differential driver has an amplifier gain of $(2R_F/R_G + 1)$. Because the line must be back terminated, the amplifier must generate twice the voltage that it ultimately transmits.

the back-termination resistors is the composite of the transmitted and received signal. The termination resistors are used to tap off this signal and feed it to the receive circuitry. Because the receive circuitry "knows"

what is being transmitted, the transmitted data can be subtracted from the digitized composite signal to reveal the received data.

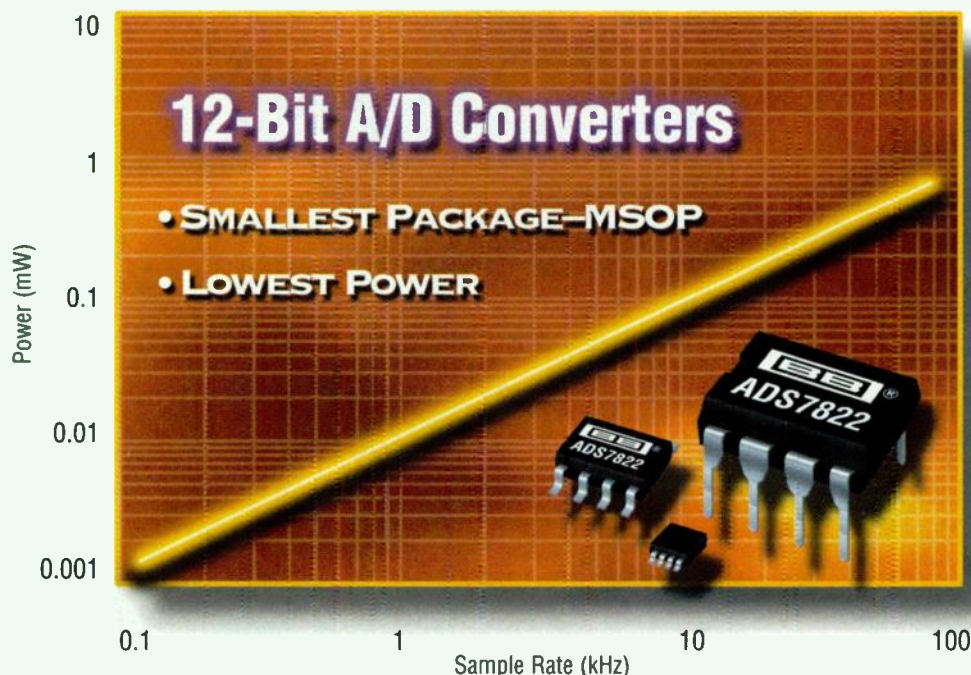
Driving a line with a differential signal offers a number of advantages



3. A complete ADSL transceiver can be built using 4 op amps. Two high power devices provide a differential line drive of +20 dBm. Two low-noise op amps tap off the composite signals (sum of transmitted and received signal) on the back-termination resistors. Using frequency dependent impedance matching, the transmitted signal is eliminated from the receive amplifier, revealing the differential received signal.

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Key Specifications

Micro Power	0.54mW at 75kHz
	0.06mW at 7.5kHz
Supply Voltage	2.7V
Power Down	3µA
Packages: 8-Pin DIP, SOIC, MSOP	
Pricing is \$4.64 in 1000s	

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Products	Resolution (Bits)	INL (LSB)	NMC* (Bits)	Sample Rate (kHz)	Power (mW)	SINAD (dB)	THD (dB)	FAXLINE#	Reader Service #
ADS7816	12	±1	12	200	1.9	72	-84	11355	362
ADS7817	12	±1	12	200	2.3	71	-83	11369	363
ADS7822	12	±0.75	12	75	0.54	71	-82	11358	364
ADS1286	12	±1	12	20	1	72	-85	11335	365

*No Missing Codes. For Technical Information: <http://www.burr-brown.com/Ads/ADS7822-Ad.html>

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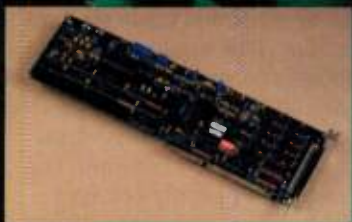
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compared to a single-ended drive. Because the two outputs are always 180 degrees out of phase relative to one another, the differential signal output is double the output amplitude of either of the op amps. As a result, the differential amplifier can have a peak-to-peak swing of 16 V (each op-amp can swing to ± 4 V), even though the power supply is ± 5 V.

In addition to this, even-order harmonics (2nd, 4th, 6th, etc.) of the two single-ended outputs tend to cancel one another out. So, the total harmonic distortion (THD) decreases compared to the single-ended case, even as the signal amplitude is doubled. This is particularly advantageous for the case of the second harmonic. Being very close, as it is, to the fundamental filtering becomes difficult.

Differential line driving also helps to preserve the integrity of the transmitted signal in the presence of electromagnetic interference (EMI). EMI tends to induce itself equally on to both the positive and negative signal line. As a result, a receiver with a good common-mode rejection ratio (CMRR), will amplify the original signal while rejecting induced (common mode) EMI.

Transformer Design

Increasing the peak-to-peak output signal from the amplifier in the previous example, combined with a variation in the turns ratio of the transformer, can yield further enhancements to the circuit. The output signal swing of the AD8012 can be increased to about ± 3.9 V before clipping occurs. This increases the peak-to-peak differential output of the amplifier to about 15.6 V. Because the signal applied to the primary winding is now bigger, the transformer turns ratio of 1:1 can be replaced with a turns ratio of about 1.3:1 (from amplifier to line). This steps the 7.8-V peak-to-peak primary voltage down to 6 V. This is the same secondary voltage as before,

thus making the resulting power delivered to the line the same.

The received signal, which is small relative to the transmit signal, will however be stepped up by a factor of 1.3. Amplifying the received signal in this manner enhances its signal to noise ratio and is useful when the received signal is small compared to the transmitted signal.

The impedance reflected from the 135- Ω line now becomes 228 Ω ($1.3^2 \times 135 \Omega$). With a correctly terminated line, the amplifier must now drive a total load of 456 Ω (114 $\Omega + 114 \Omega + 228 \Omega$), considerably less than the original 270- Ω load. This reduces the drive current of the amplifier by about 40%.

More significantly, however, is the reduction in dynamic power consump-

tion; that is, the power the amplifier must consume to deliver the load power. Increasing the output signal so that it is as close as possible to the power rails minimizes the power consumed in the amplifier.

But there is a price to pay in terms of increased signal distortion. Increasing the output signal of each op amp from the original ± 3 V to ± 3.9 V reduces the spurious-free dynamic range (SFDR) from -65 dB to -50 dB (measured at 500 kHz).

The theoretical limit to this signal maximization would be the case of using an ideal rail-to-rail amplifier to transmit a square wave. Because the square wave would be swinging all the way to each rail, there would be no dynamic power consumption in the am-

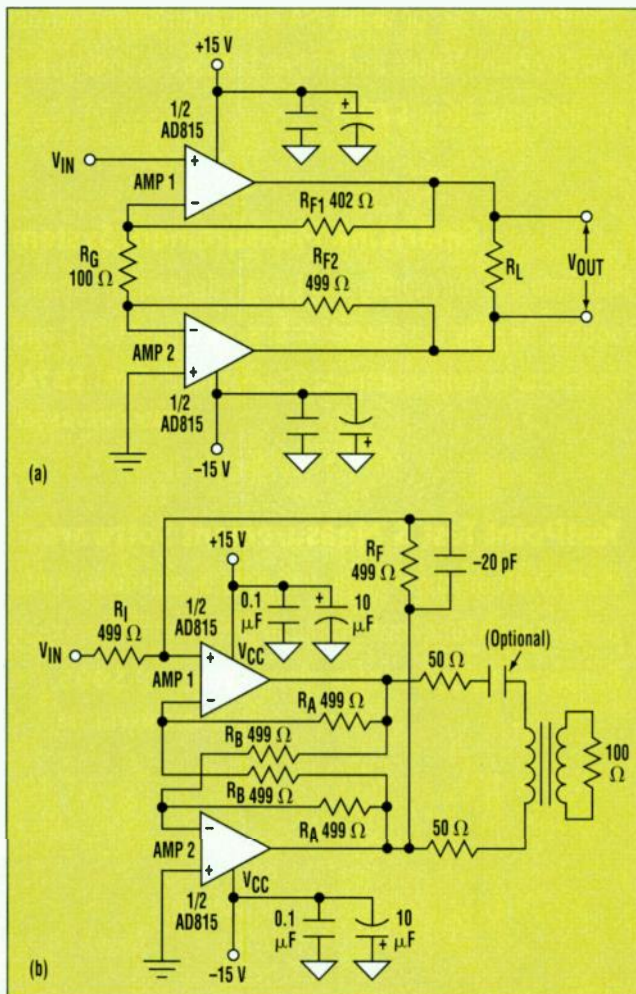
plifier. This would reduce the power consumed within the amplifier to the simple product of quiescent current and the difference between the two power supply voltages.

A Differential Transceiver

ADSL is a means for exchanging data between a telephone central office (CO) and the home via conventional telephone twisted-pair (POTS). Originally envisioned as a technology to deliver video-on-demand over phone lines, ADSL's asymmetrical data rates (up to 6.144 Mbits/s downstream, and 640 kbits/s upstream) lend themselves very well to surfing the Internet.

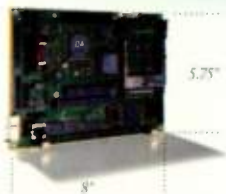
Most ADSL applications use either carrierless amplitude and phase (CAP) or discrete multitone (DMT) as modulation schemes. To transmit data over distances up to 18,000 ft., both standards call for a line power of +20 dBm to +26 dBm. This is based upon a line impedance of either 100 or 135 Ω .

A complete transceiver circuit for ADSL is shown using a quad op amp (AD816) that was designed primarily for providing an integrated solution for the transmit and receive functions of an ADSL modem (Fig. 3). The transmit-



4. Single-ended to differential conversion can be accomplished in a number of ways. A simple "three resistor" amplifier works well at various gains. However changing the gain involves changing at least two of the resistors. In addition, the noise gains of the two op-amps always differ by one. At the cost of some extra passive components, an alternative circuit can eliminate both of these problems.

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Demystifying dBm: A Primer On Power

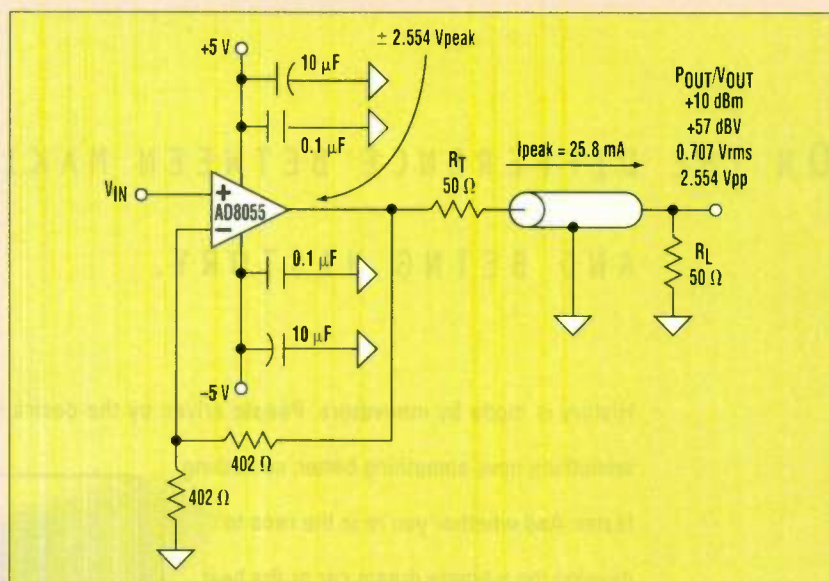
Signal levels in wired communications applications are usually specified either in dBm or dBmV. The drive capability of operational amplifiers on the other hand is usually specified in terms of peak output voltage and current. Because of differences in terminology, choosing a suitable line driving op amp can be difficult and confusing.

In order to understand how the two specs are related, it's a good idea to start with a few definitions.

Line Impedance: This is the size of the termination resistor on the line that is being driven.

Crest Factor: The peak to average (or rms) ratio of a signal. While a sine wave has the familiar crest factor of (2, the crest factor of modulated signals varies depending upon the modulation scheme. Crest factors typically range from 1.3 to 5.5.

Driver Load Impedance: The impedance that the amplifier has to drive. This impedance is the sum of the impedance that is reflected from the line and the amplifier's back termination resistors



a. Assuming a constant load impedance of 50-Ω, dBm and mW units can be related to dBmV and volts. For a different line impedance, the mV and dBmV scales will shift upwards or downwards relative to the dBm and mW scales.

The dBm unit is defined as the power level in dB relative to 1 m, i.e.

$$\text{Power(dBm)} = 10 \log_{10}(\text{Power} / 1 \text{ mW})$$

Since power in watts is defined as the rms voltage squared, divided by the line impedance, we can also write this as:

$$\text{Power(dBm)} = 10 \log_{10}((V_{\text{rms}}^2 / R) / 1 \text{ mW})$$

From this, it can be inferred that 0 dBm is equal to 1 mW, 10 dBm is equal to 10 mW, +30 dBm is equal to 1 W, etc... Because impedance is an integral component of this equation, it is always necessary to specify a line impedance-value when talking about dBm levels. The dBmV unit is defined as the volt-

age level, in dB, relative to 1 mV, i.e.

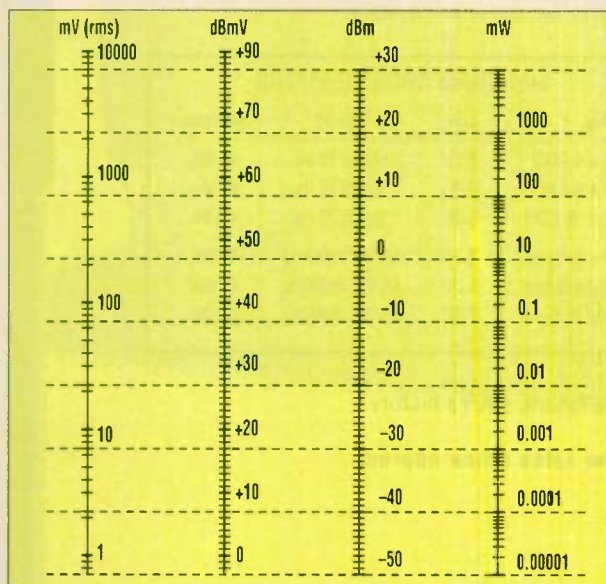
$$\text{Voltage(dBmV)} = 20 \log_{10}(V_{\text{rms}} / 1 \text{ mV})$$

Therefore, 0 dBmV is equal to 1 mV, +60 dBmV is equal to 1 V, etc.

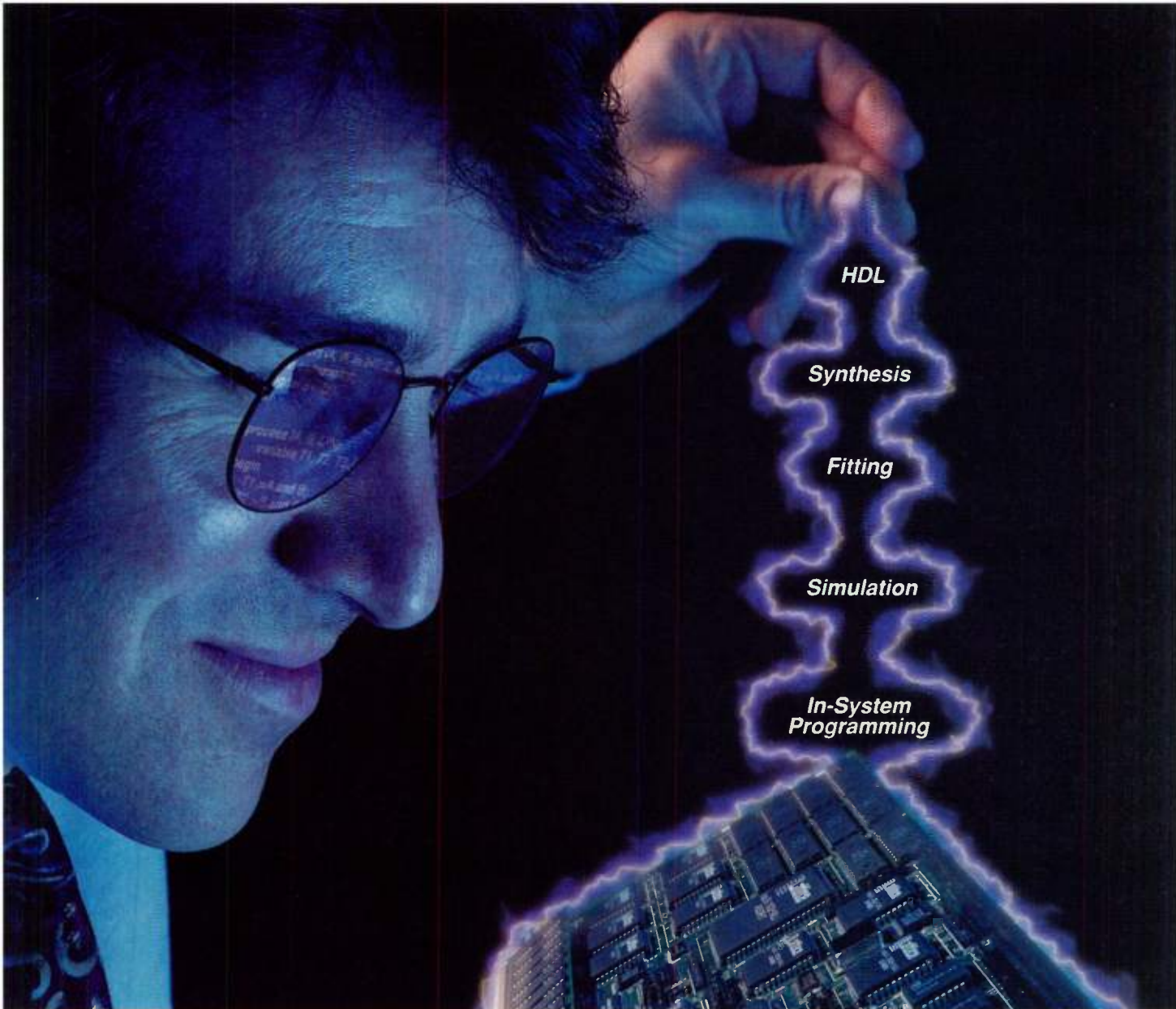
Figure a shows how mV, dBmV, dBm and mW relate to each other. This is, however, only valid for a load impedance of 50 W. If the load impedance were 75 W for example, the mV and dBmV scales will be shifted downward relative to the dBm and mW scales.

Consider this example. The operational amplifier in Figure b is required to deliver a power level of +10 dBm to a line which has a 50-W load impedance and is back-terminated. The signal being transmitted is determined to have a crest factor of 1.8.

A power level of +10 dBm corresponds to an rms voltage of 0.707 V (+57 dBmV). From the crest factor, the peak voltage is calculated at 1.27 V. Because half of the voltage is lost in the 50-W back-termination resistor, the op amp must be able to deliver a peak output voltage of 2.54 V. This corresponds to a peak output current of 25.4 mA.



b. A line-power requirement (in dBm) alone does not give the designer enough information to select a suitable line driver. In order to convert the dBm power requirement back to peak voltage and current requirements, the line impedance and the crest factor of the signal must be known.



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ted signal is applied to the V+ and V- terminals of the differential amplifier formed by high-output power op amps D1 and D2. The received signal is amplified by two low-noise op amps R1 and R2.

The transmit/receive block is commonly referred to as a hybrid, whose function is to deliver maximum transmit signal power to the line, while suppressing the transmitted signal in the receive circuitry. The figure of merit for the performance of the hybrid is known as trans-hybrid loss. This is a measure, in decibels, of the suppression of transmit signal by the receiver circuitry.

The power amplifiers of the AD816 (D1 and D2) are arranged in a differential configuration that receives its inputs from the differential outputs of a DAC. The outputs differentially drive the transformer primary with a turns ratio of 1:2. The line on the secondary

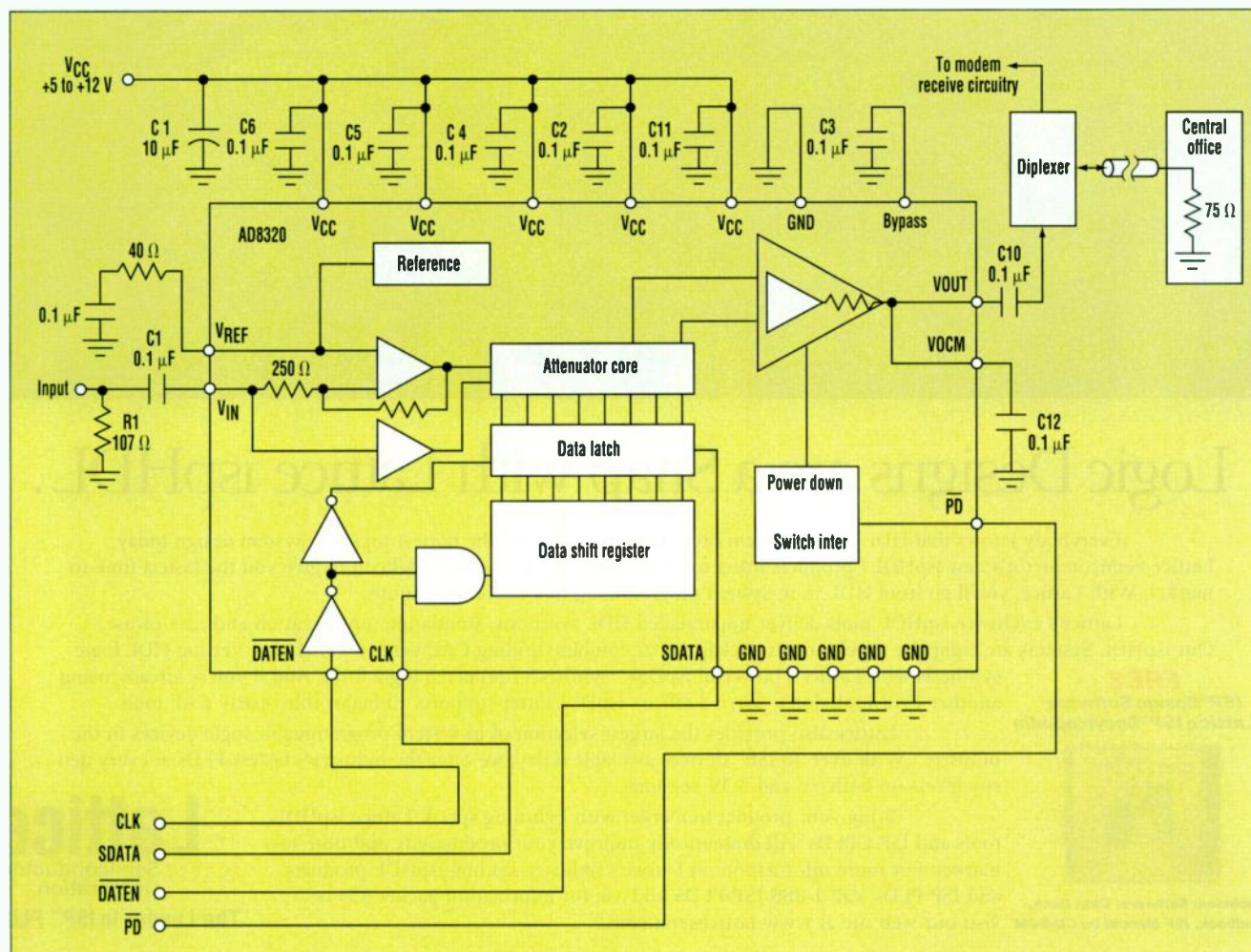
side of the transformer has an impedance of 120 Ω . As a result, one quarter of this resistance (30 Ω) is required for correct back-termination on the primary side due to the impedance scaling by the square of the turns ratio. This resistance is divided in half (15 Ω) and put on each side of the drive buffers for symmetry (R101 and R201).

The receive section (R1 and R2) is configured as a pair of difference amplifiers that together produce a differential output. This received signal is composed of the receive signal in addition to the transmitted signal attenuated by the trans-hybrid loss.

The circuit is highly symmetrical, so a single-ended explanation can be easily generalized to understand the differential operation. The output of D1 drives the top of the primary of T1 through R101. A voltage divider is formed by R101 and all the down-

stream circuitry comprised of T1, the transmission line, and its termination. For an ideal transformer, transmission line, and termination, this will appear to be 15 Ω ; thus the signal appearing at Pins 1 and 2 of T1 will be the output of D1 divided by two in the ideal case. This signal also is applied to the input of R1 via R105.

R1 is configured as a difference amplifier. The negative side (Pin 2) is driven by another signal that is a divided down version of the output of D1. This circuit is formed by R102 as one side of the voltage divider along with R103, C101, R104 and L101 as the other half of the divider. If the frequency-dependent impedance part of this circuit matches the transformer, transmission line, and termination impedance, then the signals applied to both sides of the difference-amp-configured R1 will be the same, and the transmit signal will



5. A programmable gain amplifier lends itself to driving a cable modem's upstream or return path. The use of a dynamic output impedance of 75 Ω cuts the required amplifier voltage swing in half, as compared to an externally terminated amplifier. This allows an output voltage of 3.1V peak-to-peak (58 dBmV) while operating on a single supply as low as 5V.



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be subtracted out by the circuit.

In a real-world situation, it is not practical (or even possible) to subtract out all of the transmit signal (100% trans-hybrid loss) to provide a first-order cancellation. This, however, goes a long way toward reducing the dynamic range of the RCVOUT signal. The overall performance of this circuit depends on the ability to build a lumped element network that matches the impedance of the transmission line over the frequency range required for ADSL (from about 20 kHz to 1.1 MHz).

The circuits formed by D2 and R2 and the AD816 are totally symmetric with those formed by D1 and R1 and work in the same fashion.

The receive signal from the telephone line creates a differential signal across the primary of T1. There is, however, a two-to-one reduction in amplitude due to the turns ratio of T1. This differential signal is applied to the + inputs (Pins 3 and 12) of R1 and R2. The receive amplifiers buffer this signal and present a differential output at Pins 1 and 14. There is no significant receive signal applied to the negative inputs of R1 and R2 due to the attenuating effects of R101 and R201 and the low output impedances of D1 and D2.

As a result, the overall circuit provides first-order cancellation of the transmit signal and differential buffering of the receive signal.

Power Considerations

The line driver in this example delivers a power level of about +20 dBm to the line. With a line impedance of 120 Ω , this corresponds to an rms voltage level on the line of 3.5 V. Because the line interface transformer has a (step-up) turns ratio of 1:2 and because of the presence of the two 15- Ω back-termination resistors, each amplifier must deliver an rms voltage of 1.7 V.

In ADSL systems that use DMT, there is a need to transmit signals with crest factors as high as 5.3. This high crest factor results from short (typically 10 μ s) signal peaks that rarely occur (on average $1:10^7$). But, the amplifier must supply the requisite voltage and current when these peaks do occur.

Based on this, each op amp in the above example is required to occasionally deliver peak voltages of ± 9 V (i.e. 5.3×1.7 V) and peak currents of ± 300

mA. This peak-to-average ratio necessitates relatively high power-supply rails (± 15 V in this case).

The large amount of headroom between the supply rails and the rms signal level increases the dynamic power consumption in the amplifier to levels that are close to the amplifier's quiescent power. When doing power-consumption calculations for heat sinking purposes, it is important to remember that package-power consumption is the sum of quiescent and dynamic power, not the sum of quiescent and load power.

It follows that dynamic power consumption can be reduced by reducing the power supply voltages. While it would be prudent to reduce the power supply to a level that allows the op amps to deliver the required peak voltage (± 9 V in this case), signal clipping may be tolerable in some applications. In DMT applications, clipping of peak voltages tends to manifest itself as an increase to the level of the noise floor. This will at some point begin to degrade the bit-error rate (BER). The best approach in such an optimization scheme would be to reduce the power supply voltages until the BER begins degrading below an acceptable minimum.

Some ADSL applications call for a line power of 26 dBm. Because there is little scope to further increase the output voltage of the op amps, this power level would be achieved by increasing the turns ratio of the transformer to as much as 4:1. In this case, R101 and R201 would be 3.75 Ω , and the peak current of the AD816 (1 A) would be the drive limit of the transmitter.

Heat Sinking

To ensure reliability, the temperature of the silicon die (usually referred to as the junction temperature) should be maintained at less than 175°C. For this reason, the IC package will require some form of heat sinking in most applications.

Normally, amplifiers like this will be soldered directly to a copper pad on the printed-circuit board. An important component of the resulting die-to-ambient thermal resistance (θ_{JA}) is the thermal resistance between the package and the copper pad. The lowest thermal resistance is achieved by employing a direct soldered connec-

tion between the package-to-copper pad. The use of heat-sink grease either with or without a washer will increase this number.

Single-To-Differential Conversion

If the signal to be delivered to a line is single-ended, a single-ended-to-differential transformation must be implemented if the line is to be driven differentially (Fig. 4).

In Figure 4a, Amp 1 has its + input driven with the input signal, while the + input of Amp 2 is grounded. Thus, the - input of Amp 2 also is driven to virtual ground by negative feedback. As a result, Amp 1 is configured for a noninverting gain of five ($1 + R_{F1}/R_G$).

The -input of Amp 1, which has the same voltage as Amp 1's +input, serves as an input to Amp 2, configured as an inverting amplifier with a gain of -5 ($-R_{F2}/R_G$). Thus, the two outputs move in opposite directions with the same gain to create a balanced differential signal.

This circuit can work at various gains with proper resistor selection. But, in general, at least two resistor values have to be changed to change the gain of the circuit. In addition, the noise gains ($1 + R_F/R_G$) of the two op amps will always differ by one (5 and 6 in this case). This gives the two op-amps differing closed-loop bandwidths. Signals at frequencies close to the closed-loop bandwidth will be unsymmetrically amplified as a result.

A second circuit that has none of these disadvantages is shown in Figure 4b. Each of the AD815's current feedback op amps is configured as a unity gain follower by the feedback resistors (R_A). Each op-amp output also drives the other as a unity gain inverter via the two R_{BS} .

If the +input to Amp 2 is grounded and a small positive signal is applied to the +input of Amp 1, the output of Amp 1 will be driven to saturation in the positive direction and the output of Amp 2 will be driven to saturation in the negative direction. This is similar to the way a conventional op amp behaves without any feedback.

Now, if a resistor (R_F) is connected from the output of Amp 2 to the +input of Amp 1, negative feedback is provided, which then closes the loop. An input resistor (R_I) will make the circuit look like a conventional inverting op-amp config-

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Single-Supply Line Driving

Line driving in a single-supply environment presents some unique challenges. Signals must have a common mode level that lies somewhere between ground and supply usually at $V_{\text{supply}}/2$. Because the output signal must swing within a smaller range, headroom between the signal and the power supply rails also becomes an issue. Trying to get around this problem by using a rail-to-rail amplifier would seem to be an easy solution. However, in a line-driving context, there are some potential pitfalls to this approach.

Product datasheets usually specify the rail-to-rail performance of an amplifier under fairly light loading conditions. This may mean that the amplifier can only come to within 1 or 2 V of the rails when delivering high current. This problem is compounded by the reality that signal distortion generally degrades as signals swing close to the power-supply rails (even under light loading conditions). Typically, a rail-to-rail amplifier should maintain at least 500 mV of headroom to each rail to preserve its specified distortion level.

Cable Modems

Emerging cable-modem standards are a good example of an application where the line driver must operate in a single-supply environment. Because this modem circuit is predominantly digital, needing only a single supply to operate, economic necessity demands that the analog line-driving circuit also make do with a single supply.

Depicted is a single-supply line-driving circuit for the "upstream" or return path of a cable modem (home to central office) (Fig. 5). The input to the line driver, modulated in QPSK format, will generally be supplied by a DAC or a specialized QPSK modulator such as the AD9853. Because the input of the amplifier has a dc bias

level of 1.9 V, the input signal will normally be ac-coupled. The amplifier has an input impedance of 250 Ω . To give the circuit the 75- Ω input impedance, which is popular in video applications, an external 107- Ω shunt resistor to ground is added.

Cable modem standards in both Europe and the U.S. demand that the amplitude of the transmitted signal be variable. This allows the modem to compensate for the variation in signal attenuation as a result of differing distances to the central office. Either the line driver or the device driving it must be able to vary the amplitude of the signal. In this example, the gain of the amplifier can be programmed over a 36-dB range (-10 dB through +26 dB) through an 8-bit serial interface.

To correctly terminate the line, the amplifier must present an output impedance also of 75 Ω . In this application, an external back-termination resistor is not necessary because the amplifier has a built-in or dynamic output impedance of 75 Ω . This halves the requisite output voltage compared to applications where an external back termination resistor must be added. As a result, the amplifier is capable of delivering an output level of 58 dBmV (about 3.1 Vpp) on the line, while operating on a single voltage of as little as +5 V.

Because data transfer by cable is intermittent, especially in the case of Internet access, upstream data is transmitted in bursts. While transmitting, the amplifier cannot be powered down (by pulling the Power Down line low). This reduces the quiescent current to one-third of its nominal value. However, the device's 75- Ω output impedance is maintained during power-down mode. This fulfills the requirement that all devices connected to a particular diplexer maintain a 75- Ω output impedance at all times so that the diplexer itself can maintain a 75- Ω impedance to the line.

Eamon Nash is an application engineer with Analog Devices' Advanced Linear Products Group and holds a BE in Electronics from the University of Limerick, Ireland.

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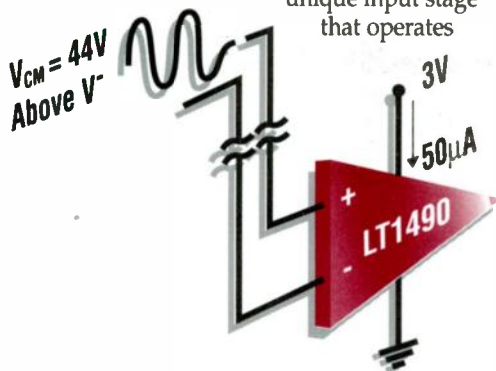
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Suggested Further Reading on the Web:

DN134: Telephone Ring-Tone Generation

LT MAGAZINE: The LT1490/LT1491 Over-the-Top Dual and Quad Micropower Rail-to-Rail Amplifier, Feb '96 p.18

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	LT1490	LT1491	800	6	84	180	0.06	50	2	44
	LT1466L	LT1467L	390	7	83	120	0.04	75	2.3	16
	LT1366	LT1367	475	6	81	400	0.13	520	1.8	36
	LT1368	LT1369	475	6	81	160	0.065	520	1.8	36
	LT1498	LT1499	475	2.5	81	10 MHz	6	2.2 mA	2.2	36

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In This Issue...

- ▲ First Universal Micropower Rail-to-Rail Op Amp Pg.1
- ▲ 56-Year Operation on Two AA Batteries! Pg.2
- ▲ Precision Performance from 1.8V to 36V Pg.2
- ▲ Micropower, Guaranteed Low V_{OS} from Rail-to-Rail Pg.3

- ▲ The Highest Precision Op Amp. Period. Pg.3
- ▲ 16-Bit Accuracy from Rail-to-Rail Pg.4
- ▲ 6V/µs, 10MHz Op Amp is Stable with 10,000pF Pg.4

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For battery and sensor applications where supply current is paramount, the **LT1495** dual and **LT1496** quad rail-to-rail op amps

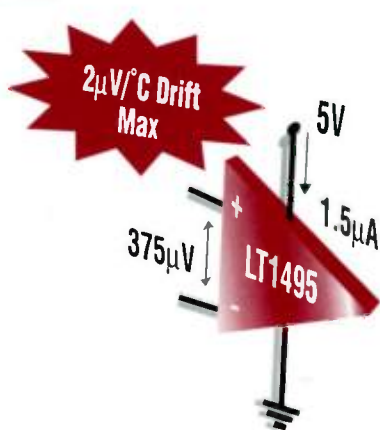
furnish precision performance with minuscule power drain, 1.5 μ A max. Accuracy of the amplifier is not compromised by the current level: input offset voltage is 375 μ V maximum with maximum drift of 2 μ V/ $^{\circ}$ C, input offset current is 100pA maximum. The devices also feature a unique input stage which allows operation with common mode voltages above the positive supply.

Features:

- Low Supply Current: 1.5 μ A Max
- Low Offset Voltage: 375 μ V Max
- Very Low V_{OS} Drift: 2 μ V/ $^{\circ}$ C Max
- "Over The Top Input" Common Mode = 10V at $V_S = 3V$
- Output Sources and Sinks 500 μ A Load Current
- Wide Supply Range: 2.2V to 36V

Price: \$3.35 ea/1K pcs
Packages:
Dual 8-Lead SO, DIP
Quad 14-Lead SO, DIP

Circle No. 212



Precision Performance from 1.8V to 36V

Sense current with battery voltages as low as 1.8V

Operating over a wide 1.8V to 36V supply range, the **LT1366** dual and **LT1367** quad combine low offset voltage and high gain with rail-to-rail operation. Offset voltage is 475 μ V maximum across the entire rail-to-rail input range.

The devices can easily drive 2k loads: with a 2k load, the open-loop voltage gain is 500V/mV minimum.

Two versions of the amplifier are offered which differ in frequency compensation. The **LT1366** and **LT1367** have

conventional compensation, and are stable with load capacitances of 100pF or less. The **LT1368** dual and **LT1369** quad are compensated for use with a 0.1 μ F output capacitor which improves supply rejection and lowers output impedance at high frequencies.

Features:

- Wide Supply Range: 1.8V to 36V
- High A_{VOL} : 500V/mV Minimum Driving 2k Load
- Low Offset Voltage: 475 μ V Max
- High Common Mode Rejection Ratio: 81dB
- High Output Drive: 30mA

Price: \$3.50 ea/1K pcs
Packages:
Dual 8-Lead SO, DIP
Quad 14-Lead SO

Suggested Further Reading:
DN89: Applications of the **LT1366**: Rail-to-Rail Amplifier
LT MAGAZINE: The **LT1366** Family: Precision, Rail-to-Rail Bipolar Amplifier, Oct '94 p.13

Circle No. 214



For literature only: call 1-800-4-LINEAR

www.linear-tech.com

Micropower, Guaranteed Low V_{OS} from Rail-to-Rail

Requiring only 75 μ A maximum per amplifier, the **LT1466L** dual and **LT1467L** quad deliver 12-bit accuracy from a 3V supply. Input offset voltage is only 390 μ V maximum across the entire rail-to-rail range and the minimum open-loop gain of 400V/mV into a 10k load virtually eliminates all gain error. Operating from supplies as low as 2.3V, the LT1466L/LT1467L are ideal for battery applications.

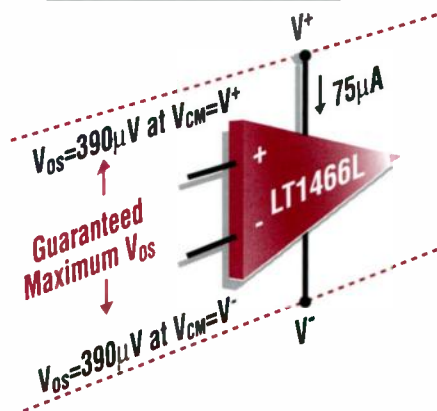
Features:

- Low Supply Current: 75 μ A Max
- 390 μ V V_{OS} Max for $V_{CM} = V^-$ to V^+
- High Common Mode Rejection Ratio: 83dB Min
- Low Input Offset Current: 3.6nA Max
- Wide Supply Range: 2.3V to 16V

Price: \$4.15 ea/1K pcs
Packages:
Dual 8-Lead SO, DIP
Quad 16-Lead SO

Suggested Further Reading:
LT MAGAZINE: New Rail-to-Rail Amplifiers: Precision Performance from Micropower to High Speed, Dec. '96 P. 18.

The LT1466L/LT1467L ease design by guaranteeing a maximum V_{OS} value at both supply rails



Circle No. 216

The Highest Precision Op Amp. Period.

The **LTC1152** has the best DC specs of any op amp with maximum 10 μ V offset voltage, 100nV/ $^{\circ}$ C input offset voltage drift, 100pA input bias current and 115dB min CMRR. A high frequency onboard charge pump eliminates the crossover distortion and limited CMRR imposed by competing technologies. The LTC1152 also includes a shutdown feature which drops supply current to 5 μ A and puts the output stage in a high impedance state.

Features:

- Ultralow Input Offset Voltage: 10 μ V Max
- Ultralow Input Offset Drift: 100nV/ $^{\circ}$ C Max
- Output Drives 1k Load
- Operates from 2.7V to 14V Total Supply Voltage

Price: \$3.15 ea/1K pcs
Packages:
Single 8-Lead SO, DIP

Suggested Further Reading:
LT MAGAZINE: The LTC1152 Rail-to-Rail Operational Amplifier, June '94 p.3

Virtually error-free DC performance, very little drift over time and temp, and very low noise at low frequencies



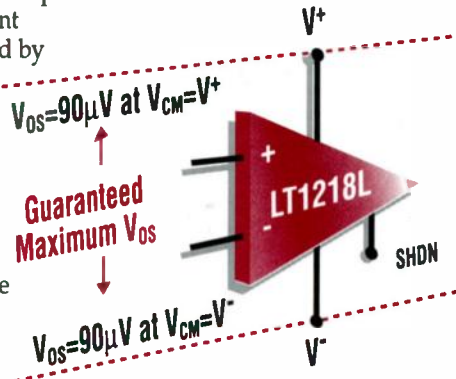
Circle No. 218

16-Bit Accuracy from Rail-to-Rail

90 μ V maximum offset voltage is guaranteed across entire input range

The **LT1218L/LT1219L** single op amps feature a low input offset voltage of 90 μ V maximum and 16-bit linearity (5V supply) over the entire rail-to-rail input range. The excellent linearity is obtained by using a patented technique, which trims the offset voltage twice, once for inputs at the positive supply, then again for the inputs at the negative supply.

The resulting common rejection of 97dB min is much better than competitive amplifiers.



Circle No. 220

Features:

- 90 μ V Max V_{OS} for $V_{CM}=V^-$ to V^+
- High Common Mode Rejection Ratio: 97dB Min
- Wide Supply Range: 2V to 16V
- Shutdown Mode: $I_S < 30\mu A$

Price: \$2.90 ea/1K pcs

Packages:

Single 8-Lead SO, DIP

Suggested Further Reading:

LT MAGAZINE: New Rail-to-Rail Amplifiers: Precision Performance from Micropower to High Speed, Dec. '96 P. 18.

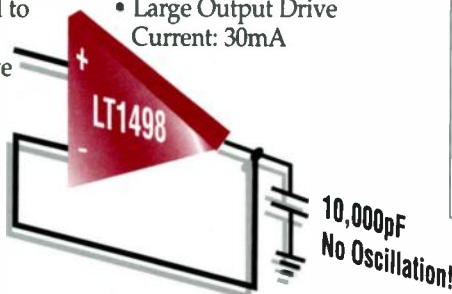
6V/ μ s, 10MHz Op Amp is Stable with 10,000pF

With 110dB PSRR, the LT1498/LT1499 maintain performance over a supply range of 2.2V to 36V

Combining speed with DC precision, the **LT1498** dual and **LT1499** quad rail-to-rail amplifiers are ideal for low voltage signal conditioning. Used as a unity-gain buffer in a 3V 12-bit system, the LT1498/LT1499 are guaranteed to add less than 1LSB error. The devices have the ability to drive capacitive loads up to 10,000pF without oscillating, easing design requirements.

Features:

- 475 μ V Max V_{OS} for $V_{CM}=V^-$ to V^+
- Wide Gain-Bandwidth Product: 10MHz
- High Slew Rate: 6V/ μ s
- Low Supply Current per Amplifier: 2.2mA
- Large Output Drive Current: 30mA



Price: \$3.80 ea/1K pcs

Package:

Dual 8-Lead SO, DIP

Quad 14-Lead SO

Suggested Further Reading:

DN50: High Frequency Amplifier Evaluation Board
LT MAGAZINE: New Rail-to-Rail Amplifiers: Precision Performance from Micropower to High Speed, Dec. '96 P. 18.

Circle No. 222

For more details, contact Linear Technology Corporation,
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Instrument-On-A-Card Standard Makes The Most Of PCI

A New Class Of Instrumentation Products Fits Neatly In Between PCI-based Computer Boards And The More Expensive VXIbus Architecture.

John Novellino

Its fast transfer rates and plug-and-play capability make the PCI bus an excellent replacement for PC-based test applications now running on the ISA bus, which will no longer be available on new PCs in the future. PCI-based PCs, however, have only three or four open slots, not enough for some applications, and even those slots may disappear in the not-too-distant future. VXIbus is a very good high-performance alternative, but it offers more performance, and higher costs, than some applications warrant.

A good solution would fit somewhere in between. As a result, National Instruments Corp., Austin, Tex., came up with the PCI eXtensions for Instrumentation (PXI) specification. PXI is an open specification that supplies all the benefits of the PCI bus, using the CompactPCI form factor, while adding features aimed at test applications. Concurrent with the announcement of PXI, National introduced 11 PXI-compliant products, including two mainframes, a controller, and eight instrument, data-acquisition, image-acquisition, and interface boards.

PXI offers the same electrical features as PCI, including 132-Mbyte/s data transfers and plug-and-play capability to facilitate interoperability of devices from different manufacturers. Consequently, PCI-based silicon, firmware, drivers, operating systems, and applications software can be cost-effectively applied to the new specification. Mechanically, PXI peripherals can run in CompactPXI systems and CompactPCI devices function in PXI systems, although the benefits of the instrumentation extensions are available only when PXI peripherals are used in PXI systems.

National notes that CompactPCI, a standard of the PCI Industrial Computer Manufacturers Group, is a rugged form factor with better mechanical integrity, easier installation and removal of hardware components, and more expansion slots that can be found in desktop computers (Fig. 1). Multiple-segment PXI systems offer many more slots than desktop PCs can. Within this architecture, the PXI specification delivers higher and more carefully defined levels of environmental performance that are needed in the vibration, shock, temperature, and humidity extremes of industrial applications.

The added instrumentation extensions include features that will be familiar to VXIbus users: An integrated trigger bus and reference clock for multiboard synchronization, a star trigger bus for precise timing, and local buses for sideband communication between peripherals (Fig. 2). The new specification also requires environmental testing and an active cooling system.

The initial products introduced include two mainframes. The PXI-1000 is a 300-W, 3U-size chassis that holds a system controller and up to seven PXI or CompactPCI modules. It features integrated, filtered, forced-air cooling and remote power inhibit capability. Users can easily remove the power supply and cooling fans as a single unit. A 19-in. rack-mount kit is available. The PXI-1000 costs \$1995. The PXI-1010 combination mainframe houses up to eight PXI/Com-



1. The PXI instrumentation architecture is based on the CompactPCI form factor. A basic mainframe holds a controller in from one to three slots and up to seven instrumentation modules.

pactPCI modules and four SCXI signal-conditioning modules. The unit, which can be rack-mounted, provides integrated, forced-air cooling for both types of modules. The PXI-1010 is priced at \$2995.

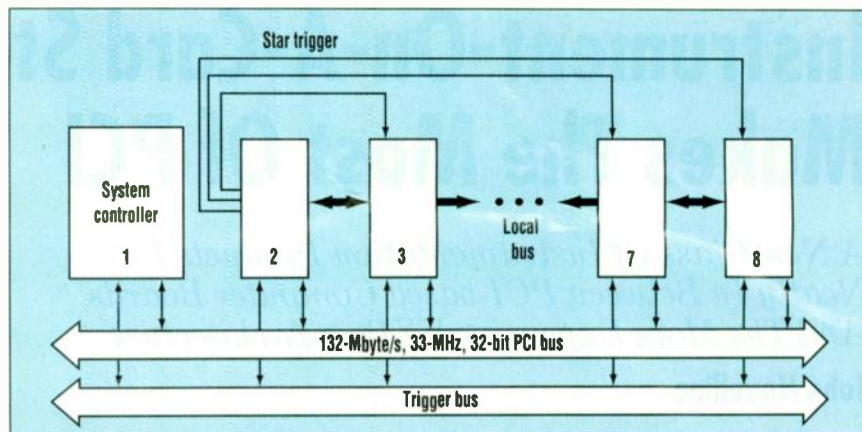
Two controller modules are being offered. The PXI-8155 is a 3U-size device with a 166-MHz Intel Pentium microprocessor with MMX technology. This controller comes with a 2.2-Gbyte hard drive, 16 Mbytes of RAM, PCI SVGA capability with 2 Mbytes of VRAM, and a 3.5-in., 1.44-Mbyte floppy drive. Included is a standard keyboard and mouse connectors, a USB port, a serial port, and a parallel port. Windows 95 is preloaded. The controller takes up only one active slot, and costs \$2995.

Options available include an Ethernet port, IEEE-488.2 port, and an additional serial port for \$1000 and a 233-MHz MMX Pentium for \$900. Ordered with the options, the controller becomes the PXI-8156.

Two multifunction data-acquisition modules, the PXI-6070E and the PXI-6040E, feature 1.25-Msample/s and 250-ksample/s digitizing, respectively. Both boards, members of National's MIO family of products, offer 16 analog inputs, 12-bit resolution, two 12-bit analog outputs, eight digital I/O lines, two 24-bit up/down counter-timers, and analog and digital triggering. The PXI-6070E costs \$1995, and the PXI-6040E is \$1195.

The PXI-5102, part of the company's DAQScope line, provides functions similar to those of a two-channel digital oscilloscope. The module has a 15-MHz bandwidth, with 20-Msample/s digitization and 8-bit vertical resolution. For repetitive waveforms, random interleaved sampling is available. Memory depth is 663 samples. The module accepts inputs from 50 mV to 5000 V. It features flexible analog and digital triggers, software-selectable ac/dc coupling, asynchronous pulse-train generation, and National's VirtualBench Scope software. The module is priced at \$1495.

A GPIB interface delivers data transfer rates of 1.5 Mbytes/s using the IEEE-488.1 3-wire handshake, or 7.7 Mbytes/s using the high-speed HS488 protocol. The company's proprietary TNT4882C ASIC performs the basic talker, listener, and con-



2. Instrumentation features included in the PXI specification include an integrated trigger bus, a star trigger capability, and local buses for communications between peripherals.

troller functions required by IEEE-488.2. The interface costs \$495.

The PXI-6533 digital I/O interface performs single-point input and output, pattern generation, and high-speed data transfers using a wide range of handshaking protocols. With PCI bus mastering, the module can do burst-mode handshaking operations at up to 20 Mwords/s, where a word is an 8-, 16-, or 32-bit pattern. Other features include optional wired-OR outputs, edge or pattern detection triggering for pattern generation applications, and six customizable handshake protocols. The interface costs \$1195.

The PXI-1408 image-acquisition module supplies high-accuracy, monochrome image acquisition meeting RS-170, CCIR, NTSC, and PAL video standards from up to four sources. The unit acquires frames in real time and transfers them directly to system memory. It costs \$1395.

PXI and CompactPCI computers can act as embedded controllers of

VXI- or VME-based instrumentation systems through the PXI-8320 system-extender module. Using the Multisystem eXtension Interface bus (MXI-2), the module makes a PXI controller perform as though it were plugged directly into the VXI or VME backplane. The unit costs \$1495.

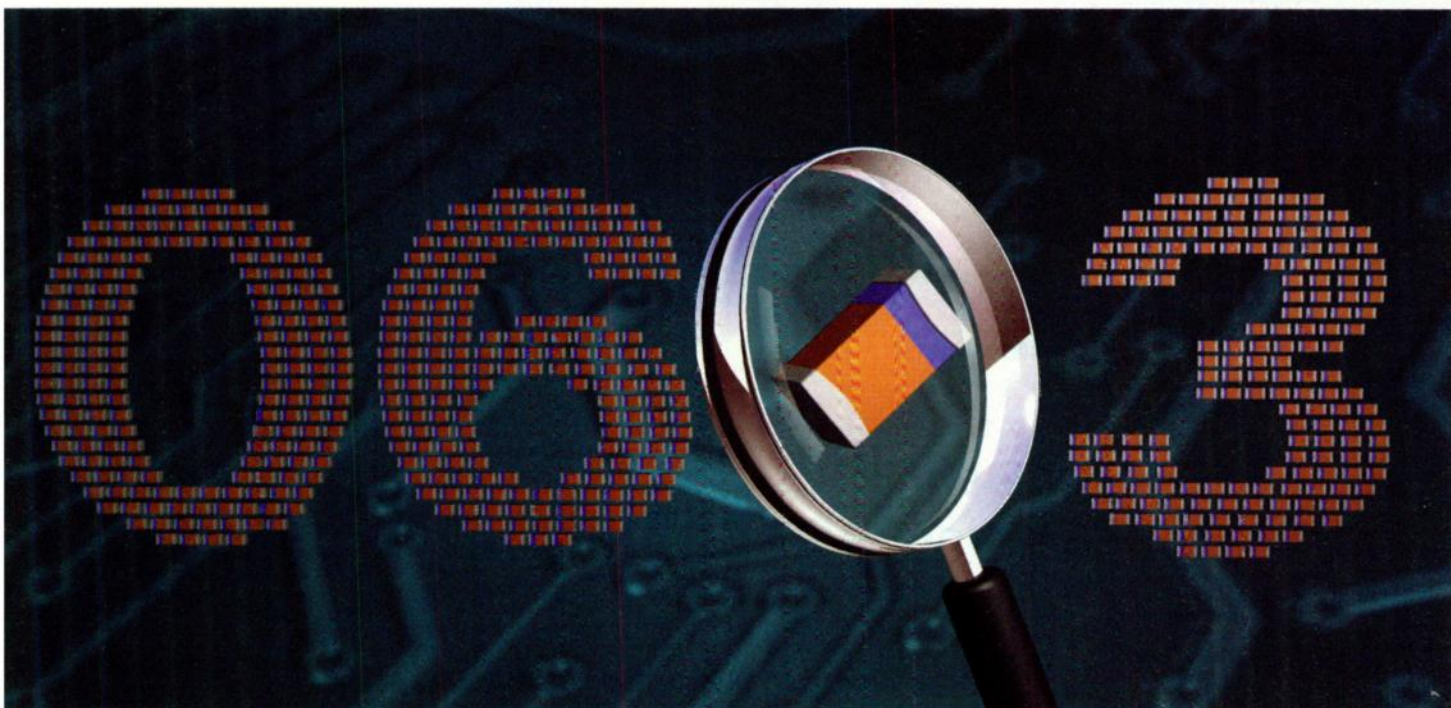
For users who want to employ PXI peripherals directly in a VXI system, the VXI-P302 is a one-clot, C-size VXI card that holds up to two PXI boards. The card holder costs \$1495.

National notes that like other bus architectures, PXI specifies rigid mechanical and electrical requirements to ensure that products from multiple vendors will work together. But unlike some specifications, PXI also specifies software requirements to ease systems integration.

For instance, the specification defines Windows 95 and Windows NT as standard software frameworks for PXI, and specifies system-level software requirements. As a result, industry-standard programming environments and all of National's virtual instrument software products—including LabVIEW, LabWindows/CVI, ComponentWorks, Measure, and VirtualBench—are compatible with the PXI hardware. In addition, all PXI peripherals must include appropriate device driver software, which eliminates the need for costly development efforts by end users.

The mechanical aspects of PXI and CompactPCI are governed by Euro-card specifications (ANSI 310-C, IEC 297, and IEEE-1101.1), which have long been used in industrial environments. Both the 3U (100-mm-by-160-

All PXI peripherals must include driver software, which eliminates the need for costly development efforts by end users.



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Design Validator sets a new standard for project continuity and design verification. Use the IsSpice4 analog and mixed mode simulator to automatically test and record circuit behavior. You can easily set limits and alarms that monitor design progress.

◆ Test Designer

The ATE specialist's standard produces acceptance test designs and fault diagnostics. Includes interactive and automatic methods for test sequencing and test synthesis.

The screenshot displays the Magnetix Designer software interface. On the left, there's a 'Code Model Properties' panel with tabs for 'Label', 'Tolerance/Sweep', and 'Failure Modes'. Below it, a 'Properties' table lists parameters like 'Ref Des', 'U1', 'Model', 'Type', 'Code Model', 'Nodes', 'Node 1', 'Node 2', 'Code Model', 'in_offset', 'gain', 'num_coef', 'den_coef', and 'out_ic'. In the center, a circuit schematic is shown with components like a transformer (T1), a diode (D1), and resistors (R1, R2). To the right of the schematic, there are two plots: a waveform plot showing a sine wave and a plot showing a step function. Below the schematic, there's a 'Configurations' panel with a table listing configurations like 'Production', 'Components', 'Closed Loop', 'Open Loop', and 'SafeT offset'. To the right of this, there's a table for 'Included Layers' with entries like 'Core Circuitry', 'Feedback', 'OP 2', 'Test', and 'Test3'.

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INSIGHTS

STANDARD

mm) and 6U (233.35-mm-by-160-mm) form factors are supported. The most recent additions to the Eurocard specifications (IEEE-1101.10 and 1101.11) address electromagnetic compatibility, user-defined mechanical keying, and other packaging issues that apply to PXI and CompactPCI systems.

PXI-compatible backplanes must supply the complete PXI feature set, all of which are implemented through the boards' J2 connectors. The J1 connector is used for 32-bit PCI features. On the 6U card, connectors J3, J4, and J5 are reserved for possible future use and need not be implemented. Any 3U board can work in a 6U chassis by adding an adapted panel.

The controller slot is at the left end of the bus segment. Limiting the system slot to this one location (a CompactPCI system slot can be at any location on the backplane), simplifies integration and increases the compatibility between controllers and chassis from multiple vendors. To the left of this slot are two slots without connectors to the backplane. These slots are meant for expansions of the system controller, so that no peripheral slots are wasted on such use.

"The time was right to develop the PXI specification," according to Carsten Puls, PXI product manager. "Several key technologies came together at the same time. PXI delivers the performance of PCI with the industrial form factor of CompactPCI. PXI also delivers the latest electrical and software extensions found in other high-performance virtual instrumentation systems."

PRICE AND AVAILABILITY

Prices for the PXI product line are as stated above. Most products will be available during the third quarter of this year. The PXI-1010 combination mainframe, the PXI-5102, and the VXI-P302 will be available in the fourth quarter. Contact the company for a copy of the PXI specification.

National Instruments Corp., 6504 Bridge Point Parkway, Austin, TX 78730-5039; (800) 258-7022; (512) 794-0100; fax (512) 794-8411; e-mail: info@natinst.com; Internet: www.natinst.com. **CIRCLE 525**

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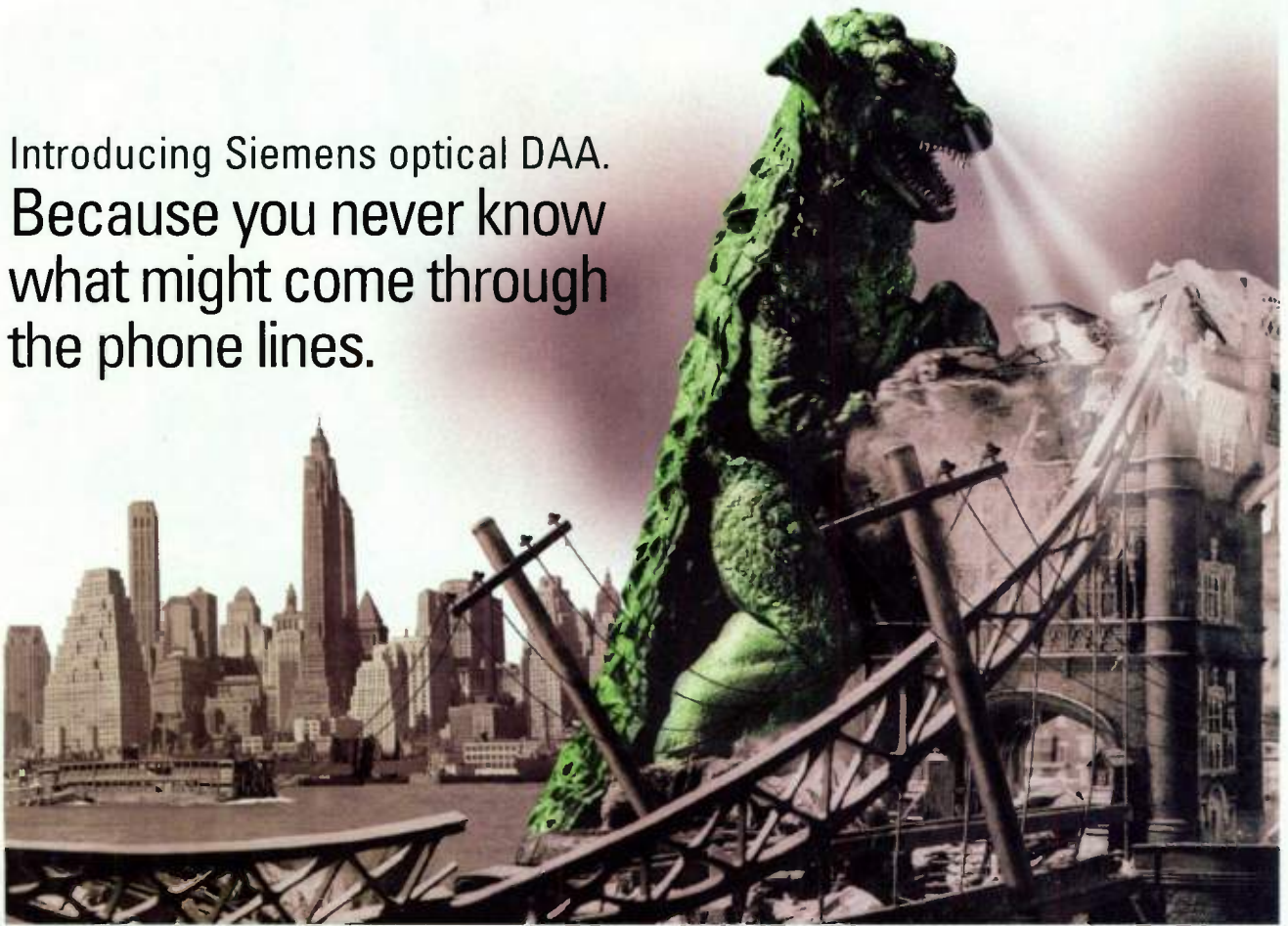
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Hook Switch Control	✓	✓
Caller ID	✓	
Snoop Mode	✓	
Line Sense	✓	
Voltage/Frequency Converter	✓	✓
Power Mgmt.	✓	✓
Wake on Ring	✓	✓
Thermal Protection	✓	✓

The opto solution that shrinks interface/isolation problems.

Today's increasing modem speeds and decreasing device sizes can make the traditional transformer and circuitry solution seem like an unwieldy monster. Now the leader in optocoupler technology breaks through the transformer barrier with the new DAA2000 and DAA2100.

Smaller size. Giant capability.

The Siemens DAA2000 is ideal for applications in PC modem cards with multimedia capabilities and extremely tight real estate requirements. The DAA2100 is the lower-cost

solution for internal and stand-alone modems where space is not an issue. The DAA2000 utilizes two 24-pin TSSOPs, while the 2100 uses two 24-pin SOICs. And both kits include two 8-pin Slimline IL388 linear optocouplers, with specifications to easily assemble the DAA function directly onto the mother board.

Special features tame distortion and power management.

The DAA2000 and DAA2100 are all-analog solutions, operating down to 2.7 V on the modem side, with distortion numbers flat across the whole band. And both include built-in ring detect and

hook-switch control. In addition, the DAA2000 offers extra features such as snoop mode and built-in overcurrent/thermal limiting. So whether you have a tight space or a tight budget, with Siemens DAA2000 and DAA2100 you'll find a perfect fit.

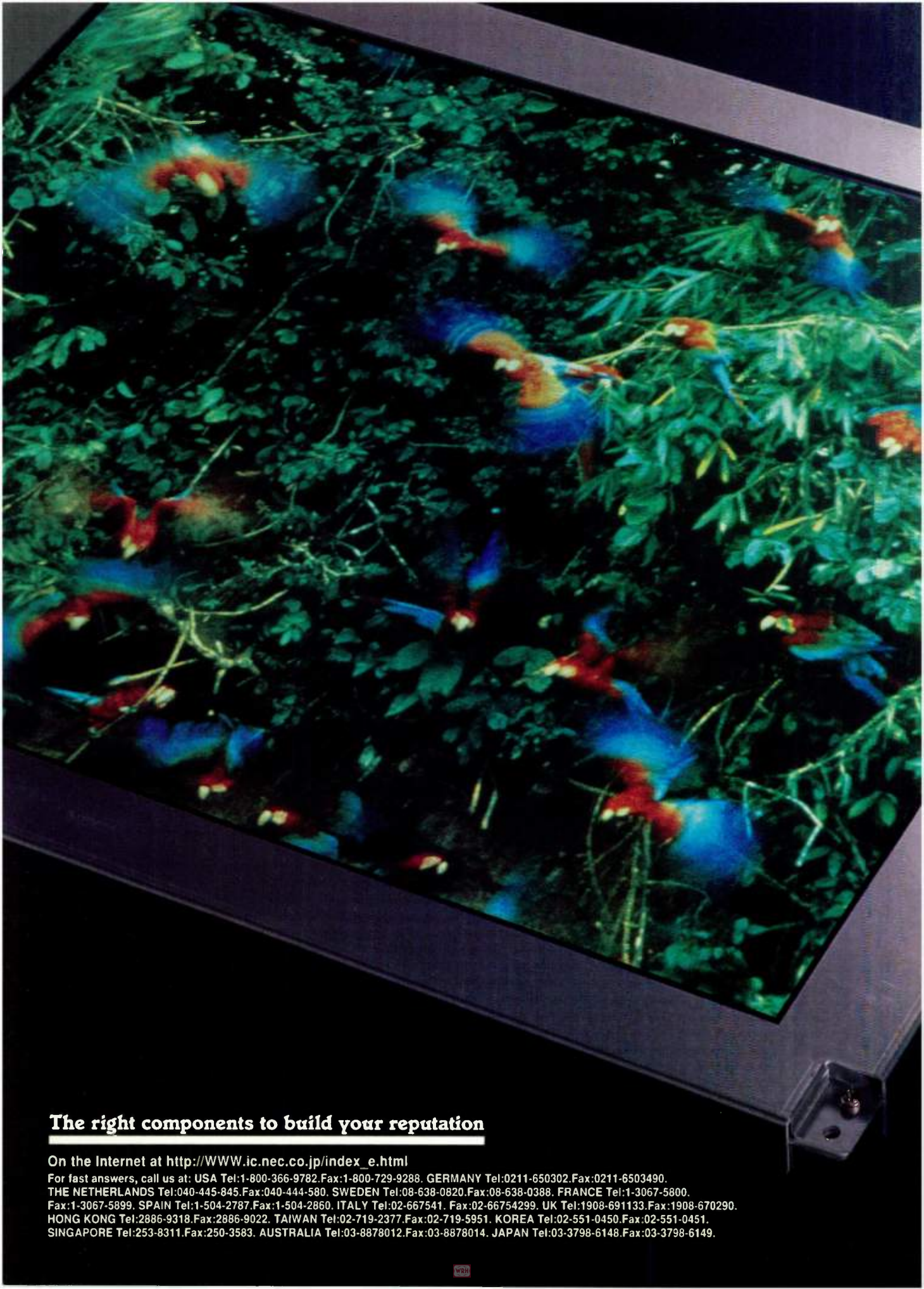
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TECH INSIGHTS PRODUCTS

PRODUCT FEATURE

8-Bit RISC MCU Incorporates Both Flash And EEPROM

ARISC-based 8-bit microcontroller family that executes one instruction per clock (except for branch operations that require two cycles), the AVR (advanced RISC) series devised by Atmel merges flash and EEPROM storage onto the same chip. The AVR microcontrollers can deliver throughputs of up to 1 MIPS/MHz and are targeted at low-cost applications that require in-system updates.

The first member in the family, the AT90S1200, packs 1 kbyte of flash memory (bulk erasable) for program storage and 64 bytes of electrically erasable (byte alterable) PROM for data/variable storage. Both memories can be loaded while in the system via a three-wire serial peripheral interface (SPI) port included on the chip. The EEPROM block is guaranteed for 100,000 erase/write cycles.

In addition to the on-chip memory resources, the MCU includes 32 general-purpose working registers, fast

context switching, an instruction set of 87 commands, an address reach to 8 Mbytes, 15 programmable I/O lines, an 8-bit timer with 8-bit prescaler, a programmable watchdog timer, and an analog comparator—all in a 20-lead package. Additional members in the AVR family have been designed and will be released later this year.

Several AVR MCUs are slated for release this quarter. The S2313, for instance, doubles the flash and EEPROM capacity and adds 128 bytes of SRAM and a UART. The S8515 pushes the flash up to 8 kbytes, the EEPROM and SRAM to 512 bytes each, also contains the UART, and doubles the package pin count to 40 leads. For really cost-sensitive applications, there's the S1220. It takes the 20-lead S1200 and then reduces the pin count to just eight leads.

Targeted for fourth-quarter release, the S4414 offers half the flash,

implanter. The patented dose-control system used in the ULE2 implanter has an energy-pure 200 eV capability (without deceleration) and charging control based on the RF PlasmaCell

EEPROM, and SRAM of the S8515, but in all other aspects is identical. The S4414 will provide a scaled memory option, while the S4433 will be the first family member to also pack an analog-to-digital converter along with 4 kbytes of flash, 256 bytes of EEPROM, and 128 bytes of SRAM. It will come in a 28-lead package.

There will be two versions of the chips: One capable of operating over a 2.7-to-6-V supply range and running at a top clock speed of 4 MHz, while the other will operate over a 4-to-6-V range and offer a top clock speed of 16 MHz. In the sleep mode, the microcontroller's current drain drops to less than 1 μ A.

To support software development, the company has created a suite of development tools—an assembler and AVR Studio, which is a total integrated debugging environment for simulation and real-time emulation. *(continued on page 75)*

HIGH-PERFORMANCE NETWORK TRANSCEIVER SOLUTIONS

How Bellcore compliance makes our transceiver

PRODUCT FEATURE

(continued from page 74)

An ANSI-compliant C compiler is available as well as an evaluation board and in-circuit emulator.

The 20-pin AT90S1200 microcontroller price starts at \$1.80 each in quantities of 1000 units. Some of the development tools are available as a free

download from the Atmel web site.

Atmel Corp.

2325 Orchard Pkwy.

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Fast Touchscreen Boasts Speed, Accuracy, And Durability

The TouchTek Premier line is a fast, accurate, and durable five-wire resistive touchscreen, suited for environments that have the flexibility to use alternate input methods such as a gloved hand, pen, fingernail, or credit card. TouchTek Premier features a topsheet with improved optical qualities and scratch-resistant finishes, new electronics, and new manufacturing processes.

The TouchTek Premier touchscreen consists of a hard-coated, chemically resistant, polyester top-

sheet that's overlaid 0.0001 in. from a thin sheet of glass coated with a transparent conductive surface. It works with both curved as well as flat sensors.

In operation, voltage is applied to the topsheet. As the user presses the screen, the topsheet compresses into contact with the glass sensor, and voltage flows to each of the four corners in proportion to the distance from the edge. The integrated controller then calculates the position of the finger or stylus based on the current flows.

For greater durability and accuracy, TouchTek Premier sensors employ a proprietary five-wire voltage linearization technique that enables all measurements to be read off the stable glass on the bottom layer, as opposed to the flexing topsheet. Unlike four-wire designs, if the polyester topsheet is damaged, the touchscreen still operates. Touches are accurate to within less than 1%. The same software drivers work with either resistive or capacitive touchscreens to ensure that there's compatibility with popular software platforms.

TouchTek Premier touchscreen kits start at \$315 for a 10.4-in. flat touchscreen kit, which includes the sensor, controller, and software drivers. Volume discounts are available.

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IC Reduces Component Count In Highly Functional Speakerphone

The MC33215 speakerphone and telephone-line interface circuit developed by Motorola simplifies phone design: Only a generic ringer and dialer IC are needed to complete the device line up for a highly func-

tional speakerphone. The IC provides the ac and dc line termination, two- to four-wire conversions, line-length AGC, and DTMF transmission. The speakerphone is half-duplex and the controller has signal and noise moni-

toring amplifiers for the base microphone and loudspeaker. The circuit is designed to be operated at line currents down to 4.0 mA, enabling parallel operation with a conventional phone.

Within the line driver and supply section of the IC (operating power is taken from the telephone line), the termination can be real or complex with adjustable impedance. Supply points are provided for the loudspeaker amplifier and peripherals as well as for the base microphone and handset. For the handset operation, there are transmit and receive amplifiers, differential microphone



inputs, a sidetone cancellation network, and muting for the microphone and earpiece. Separate inputs are given for DTMF and auxiliary signaling.

Also included are a large number of design hooks provided in the speakerphone operation, which incorporates integrated amplifiers for both the differential-input microphone and loudspeaker. For added output drive, the loudspeaker amplifier can be externally powered up to 5 V.

Switches and attenuators are supplied for smooth switching between receive and transmit, while signal and background noise monitors are incorporated in both channels. The switching depth for hands-free operation is adjustable, as are the switch-over and idle-mode timing. In addition, a dial-tone detector is located in the receive channel.

The MC33215 has a specified operating temperature range of 0 to +70°C, and is available in a 42-pin shrink DIP through-hole (SDIP-42) or a 52-pin quad flat-pack surface mount (TQFP-52). Pricing for both is \$2.55 in 10,000-piece lots.

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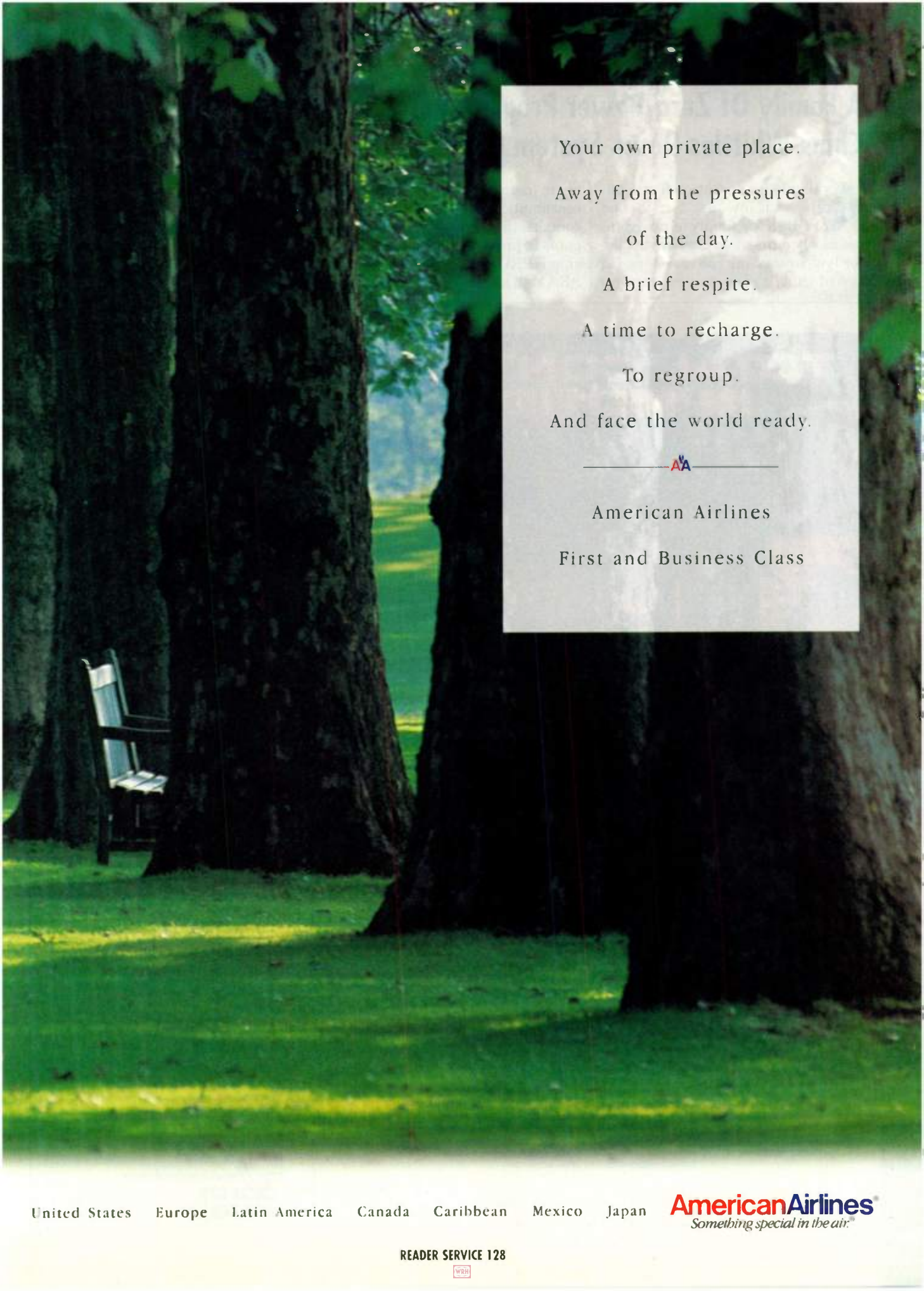
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A photograph of a lush green forest. In the foreground, a wooden bench with a striped cushion sits on a grassy clearing. The bench is positioned between two massive, ancient-looking trees with thick, textured bark. Sunlight filters through the dense canopy of green leaves, creating dappled light on the ground and the bench. The overall mood is peaceful and secluded.

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PRODUCT FEATURE

A Family Of Zero-Power Programmable Chips Whittles Down System Power

Available for operation from supplies as low as 2.7 V, the ZPSD5XXV family of programmable system devices provide support for low-voltage microcontrollers. On top of that, a zero-power standby

mode further reduces system power consumption. The ZPSD5XXV series contains the equivalent of about 5000 gates of programmable logic plus on-chip EPROM (32 to 128 kbytes) and SRAM (2 kbytes), yet consumes less

power than a single 22V10 or EPROM. This helps extend the useful life of a battery that powers a system containing the ZPSDs.

The ZPSDs have a standby current of just 1 μ A when powered by a 2.7-V supply. When running at 1 MHz, the ZPSDs draw just 0.76 mA—that's about 3% of the current that a multi-chip solution might typically consume. A 5-V version of the ZPSDs, the ZPSD5XX series, offers comparable power reductions for systems running at 5 V. It draws just a mere 7 mA when operating at 4 MHz, while a multichip solution could typically consume over 100 mA. Standby current also is low—just 10 μ A—which is more than an order of magnitude less than the multi-chip solution.

A dual-bus architecture in the ZPSD5XX and XXV families allows the chips to off-load MCU tasks so that the MCU can perform additional functions once ZPSDs receive their tasks. Additional support logic on the ZPSDs includes four 16-bit timer-counters, an 8-level priority interrupt controller, 40 individually configurable I/O lines, a configurable interface that can handle any 8- or 16-bit multiplexed or non-multiplexed address/data bus microcontroller, and an automatic power-down controller.

The 5-V ZPSD devices have memory access times of 70, 90, or 150 ns, which is fast enough to support MCUs that operate at speeds of up to 40 MHz. The 2.7-V devices can be accessed in 200 ns, which should be fast enough to support virtually all 3-V microcontrollers. The PSDsoft design tools developed by the company for use on Windows 95 or Windows 3.x systems offer easy-to-use pull-down menus to configure the ZPSDs. The tools include a proprietary version of Data I/O's ABEL logic design software, and Simucad's Silos III Verilog is used for full-chip simulation. Prices for the 5-V ZPSDs start at \$8.58 each in lots of 10,000 units for the 150-ns version, and \$9.09 apiece for the 250-ns version of the 2.7-V devices.

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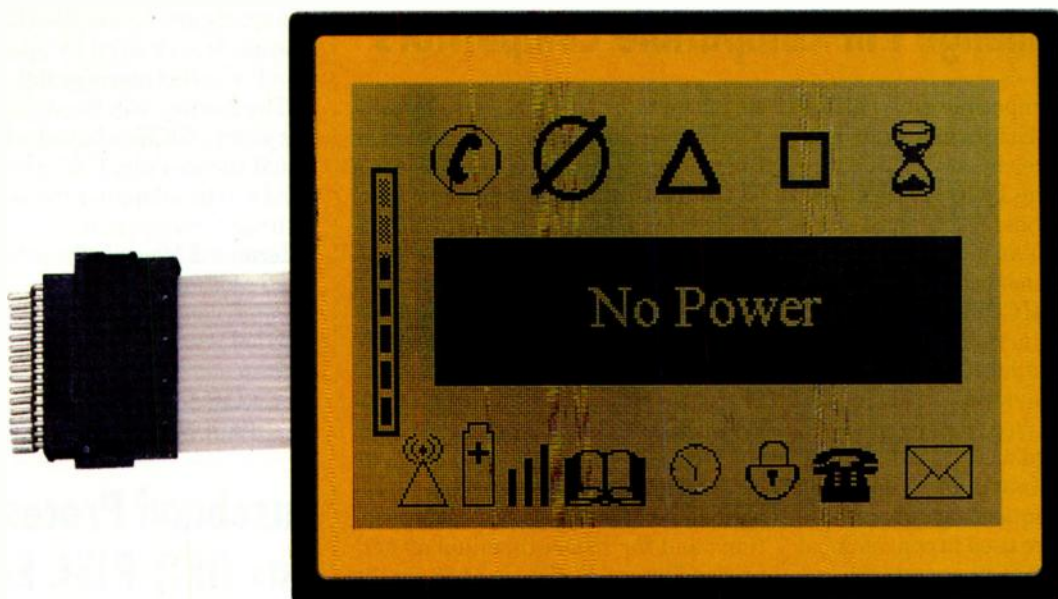
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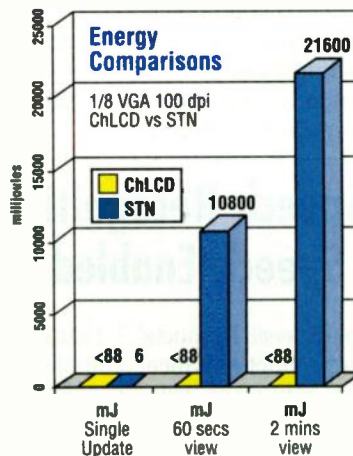
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READER SERVICE 152

W33

SLICs Challenge Pin-Compatible Competitors

Three pin-compatible alternatives to a line of Ericsson subscriber-line interface circuits (SLICs) are for high-volume DCO, PABX, and ISDN applications. A fourth SLIC is compatible with an alternate pin-out version of the same basic Ericsson IC. The HC5513B, HC5523, HC5526, and HC5515 from Harris Semiconductor are the only available drop-in alternate-source versions of Ericsson SLICs. They're free from latchup and simplify line-card or terminal-adaptor layout by eliminating the need for power-supply sequencing at turn-on.

The SLICs are used in conventional telephone-line cards to provide the last link between the DCO and the copper pair leading to the customer's home, and in ISDN terminal or network adapters to allow the connection of analog telephones. In addition to matching the telephone network's four-wire connection to the telephone's ring and tip wires, SLICs provide battery feed, overvoltage protection, ringing, supervision, hybrid, and test functions.

The new SLICs differ among themselves primarily in longitudinal balance, the common-mode rejection ra-

tio of the two-wire/four-wire hybrid. For shorter loop applications such as fiber in the loop, the HC5513B has a 55-dB longitudinal balance and costs \$5.56 each (industrial grade) in quantities of 10,000. With a 58-dB longitudinal balance, the HC5523 is intended for CO and longer loop DCO applications. Costing \$6.04 each for the industrial grade, this SLIC differs from the HC5513B in that it integrates a 17.3-k Ω resistor in the saturation guard circuit that monitors tip-to-ring voltage.

The HC5526 has a 53-dB longitudinal balance for non-U.S. CO applications and for ISDN terminal or network adapters. Pricing is \$4.75 for the industrial temperature range and \$4.20 for the commercial version. The HC5515 is identical to the HC5526 in function and price, but it matches the Ericsson PBL3860 pinout.

They come in 28-lead PLCCs or 22-pin plastic DIPs.

Harris Semiconductor,
P.O. Box 883,
Melbourne, FL 32902-0883;
1-800-4-HARRIS, ext. 7680.
CIRCLE 579

MILT LEONARD

Enhanced Speech-Recognition Products Accelerate Speech-Enabled Applications

Lernout & Hauspie Speech Products' latest launch of product enhancements will allow computer-telephony developers to create faster speech-enabled applications for a wider range of platforms and processors. This includes the general availability of their multilingual automatic speech recognition (ASR) and text-to-speech (TTS) technologies under SCO OpenServer on Dialogic's Antares DSP platform. Antares-based speech products for Windows NT are now in beta test.

There also will be a host-based version of ASR technology, which will allow developers to create applications with DSP cards, offering a cost-effective approach to designs for the small and medium-sized office markets. On top of that, the expansion of coding and decoding capabilities to the Pentium MMX processor was enhanced so

that faster speech-over-the-Internet applications could be developed.

By adding the SCO OpenServer support with 12 channels of ASR and 24 channels of TTS, support is available for a variety of telephony operating systems, including Unixware, DOS, and OS/2, with Windows NT in beta test. The offerings allow multiple speech technologies on a single board. The host-based support allows developers to add ASR to small office systems using the native processing power of an Intel Pentium rather than a separate DSP board.

In a separate development, the company launched a voice-operated calling and answering module for cellular phones. The module, a joint development with Cardian (an industrial applications development company based in Belgium), offers user-friendly

prompting and hands-free dialing. The module is activated by speech command or a mechanical switch.

The module will be available later this year to OEMs who can sell and self-brand the module. End-user applications will be adapted to be compatible with most mobile phones.

Lernout & Hauspie Speech Products
20 Mall Rd.
Burlington, MA 01803
(617) 238-0960
fax (617) 238-0986
CIRCLE 580
PAUL McGOLDRICK

Baseband Processor Has DSP, RISC Engine

The GEM301 is the first member of a family of communication processors employing the OakDSPCore digital signal processor and an ARM7 Thumb RISC-based processor core. The tandem processor platform supports the advanced operating systems and man-machine interfaces (MMIs) required for current and emerging digital cellular/PCS standards.

In its current incarnation, it has been optimized to handle the baseband processing and control tasks for GSM cellular phones. It has software-selectable settings for full- and half-rate speech coding. The GEM301's OakDSPCore processor, aided by on-chip accelerator logic, performs all GSM layer 1 signal processing, while the ARM7 RISC CPU is responsible for the protocol stack and MMI. The ARM7 also handles peripheral functions, including the system timer, serial interfaces, DMA controllers, SIM, watchdog, and UARTs. The two processors communicate via a shared memory interface.

A highly integrated GSM phone (the GEM301) is sampling now, with full production slated for later this year. Pricing will be about \$15 in quantities of 100,000.

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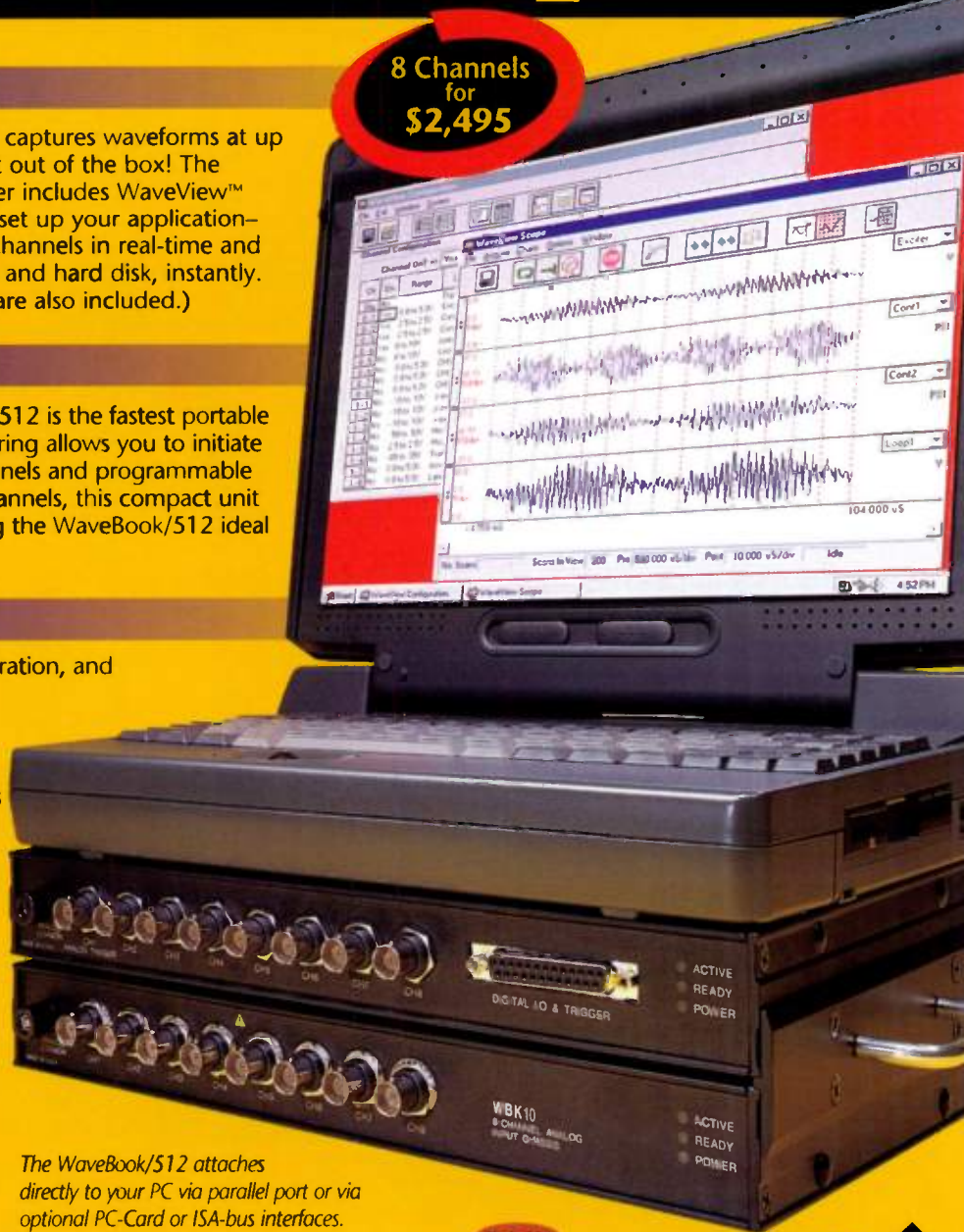
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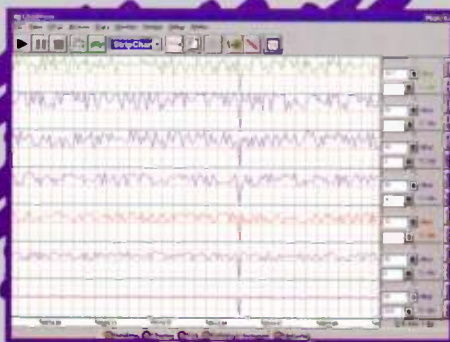
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ELECTRONIC DESIGN QUICK LOOK

■ Edited by Mike Sciannamea and Debra Schiff

MARKET FACTS

Going Plaid

Because the nature of today's electronics industry is to expand in a worldwide direction, trends in the marketplace show outsourcing from America as one of the largest chosen means of producing the highest quality product. According to a recent survey by Al Paul Lefton Company, there appears to be a draw to Scotland. Why would an American company choose to establish and operate a plant in Scotland? The primary reasons given were a highly skilled workforce, high-tech infrastructure, relatively low operating costs, university-industry support, and an efficient distribution system. Of the U.S. companies surveyed, 97% said that the performance of their plants' in Scotland is at least equal to, and improving on, their other plants, especially those in the electronics fields. Since 1990, 76% of the U.S. manufacturing plants have introduced new products—10% of those have produced over 50 new products in that same time period. Of those new products, according to 82% of the plants surveyed, their introduction had been either successful or very successful. As far as changes in management go in the Scottish-American experience, the companies said that in addition to the new product and process introductions, the entire series of events proceeded in a very positive manner. The same goes for the experience with the Scottish workforce across all levels of employment. Since 1990, 59% of all the plants had new manufacturing

methods or process innovations. Of those manufacturing changes, 91% of them proved successful or very successful. As far as testimonials from individual companies were concerned, BBR Systems, DuPont, Level Nine, Lexmark, Simple Technology, and Smart Modular Technology all had praise to offer for the Scottish manufacturing experience. BBR Systems is currently investing \$1.62 million in a new data networking manufactur-

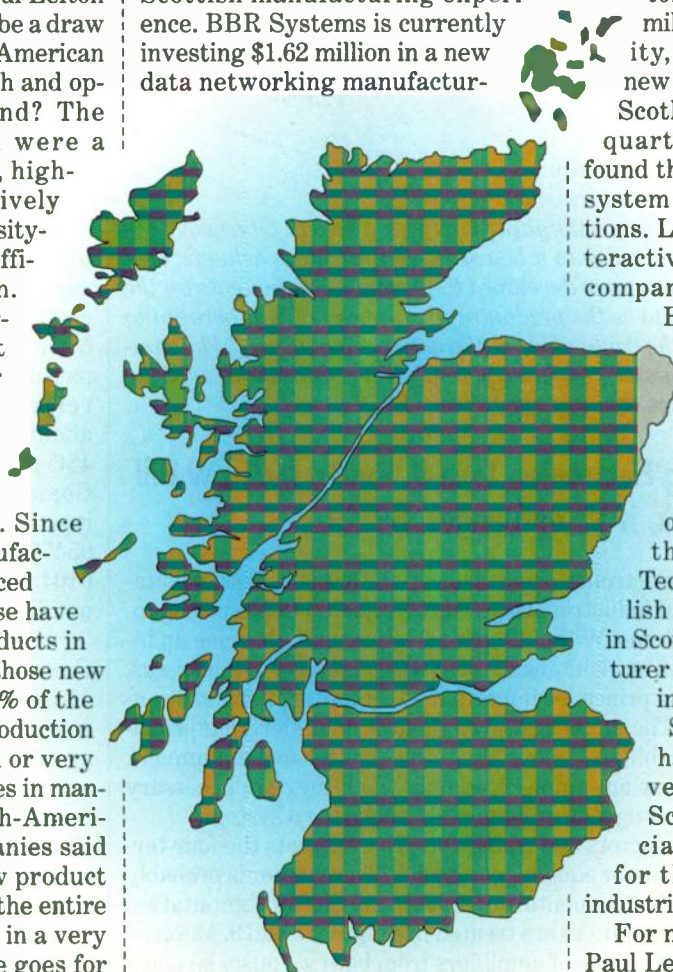
ing operation based in Glenrothes, Scotland. The company supplies cable anchoring and control hardware to the power utilities, telecommunications, and cable television industries. The company projects that their Scottish projects will create approximately 80 new positions over the next three years. DuPont Photomasks is investing over \$31

million in its new Scottish facility, and expects to create 100 new jobs there. Level Nine chose Scotland for its European headquarters because the company found the labor skills and education system superior to their other options. Level Nine builds highly interactive on-line applications. The company is currently creating

British tourism and travel information sites. Lexmark is investing \$42 million in a 90,000-square ft. facility in Scotland to manufacture laser and ink jet printers. At print time, over 500 individuals work at the assembly plant. Simple Technology also plans to establish its European headquarters in Scotland. The memory manufacturer plans to create over 360 jobs in the next five years. Finally, Smart Modular Technologies has planned a \$12 million investment in East Kilbride, Scotland. The company specializes in memory products for the computer and telecom industries.

For more information, contact Al Paul Lefton Inc., 100 Independence Mall West, Philadelphia, PA 19106-1111; (215) 351-4250; fax (215) 351-4299; e-mail: jtalbot@Lefton.com.—

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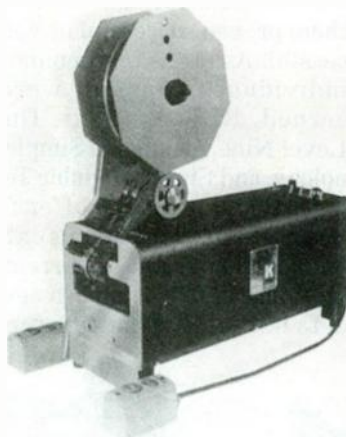
40 YEARS AGO IN ELECTRONIC DESIGN

Wire-Wrap Machine

In this solderless wire-wrap unit, two laterally adjustable wrapping tools are mounted side by side, spaced to accommodate the component used. This new technique is designed for the automated assembly of axial-lead components. Tape-mounted components are fed from a reel to a set of gripper jaws that pluck a single component from the tape into the wrapping position. The components leads are simultaneously placed into a set of "side-loading" wrapping bits, the gripper maintaining contact with the leads at either end of the component body. The "side-loading" bits fold the leads from the tangential position to an axial position in the bits. The assembly (component, gripper jaws and wrapping tools) moves forward to position each wrapping bit over a terminal. The wrapping bits then rotate in opposite directions, forming a solderless wrapped connection with each lead of the component. The total cycle time for this operation is two seconds.

The process is designed to use commercially available components. Permanent connections with the lowest known resistance and high reliability are made. The elimination of heat and protection provided by the gripper jaws during the operation gives maximum care to the component. The simplicity of this type of connection results in increased reliability of commercial electrical equipment. Gardner-Denver Co., Dept. ED, Keller Tool Div., Grand Haven, Mich. (*Electronic Design*, Sept. 1, 1957, p. 74)

Note that this machine wraps the component leads themselves around a terminal post, rather than interconnecting backplane wires on a board. Of course, the wire-wrapping technique evolved into a board interconnection scheme, and component-insertion machines were developed to place the components on the board. Gardner Denver grew to be the predominant supplier of wire-wrapping machines, and, in fact, held the trademark on the name "Wire Wrap." The company jealousy guarded that asset, continually reminding editors who used the term in describing any other company's machines.—SS



New Books: Engineering Electronics, John D. Ryder, McGraw Hill Book Co., Inc., New York, N.Y., 666 pages, \$9.50.

Fundamental concepts of electronics—particularly the areas of instrumentation, computation and general industrial usage—are projected to industrial applications and completed systems. Without letting his treatment become an instruction book in the operation or maintenance of a particular piece of apparatus, Dr. Ryder discusses operating principles important to computer, industrial control, and servomechanisms. The emphasis throughout is on underlying principles and basis circuits applicable to various electronic devices and equipment. Mathematics and circuit theory are emphasized only when they are necessary for a lucid description or advantageous in completely analyzing a system.

In the chapter on semi-conductors and transistors, Ryder treats the four-terminal network theory for transistor equivalent circuits. This chapter is probably the "strongest" in the book. Fundamentals of analog and digital computation and circuits common to both computers are treated in chapters 8 and 9. Material is included on the frequency response of amplifiers from both a sinusoidal and a pulse standpoint. (*Electronic Design*, Sept. 1, 1957, p. 98)

Dr. John D. Ryder's books were standard texts in many engineering schools of the '50s and '60s. I don't recall this one, but its broad scope might indicate that it was a textbook intended for engineering students other than EE majors.—SS

OFF THE SHELF

A Digital Signal Processing Primer offers an introduction to digital signal processing (DSP), with emphasis on digital audio and applications to computer music. The book covers topics such as phasors and tuning forks; the wave equation; sampling and quantizing; feedforward and feedback filters; comb and string filters; periodic sounds; transform methods; and filter design. In addition, the book features questions and suggested experiments that may help readers understand and apply fundamental DSP theories and techniques. The 314-page book is priced at \$37.75. Contact Addison-Wesley Publishing Co. Inc., 2725 Sand Hill Road, Menlo Park, CA 94025; (800) 822-6339; e-mail: aw.eng@aw.com; Internet: <http://www.aw.com/eng>.

PGP: Pretty Good Privacy is a freely available encryption program that protects the privacy of files and electronic mail. It uses powerful public key cryptography and works on virtually every platform. The book is a technical user's guide and offers a behind-the-scenes look at cryptography and privacy. It describes how to use PGP and provides background on cryptography, PGP's history, battles over public key cryptography patents and U.S. government export restrictions, and public debates about privacy and free speech. The 430-page book is priced at \$29.95. Contact O'Reilly Technical Publishing, 101 Morris St., Sebastopol, CA 95472; (800) 998-9938; fax (707) 829-0104; e-mail: order@ora.com; Internet: <http://www.ora.com>.

Communications Network Test & Measurement Handbook provides comprehensive and up-to-date coverage of all the methodologies, data, and reference material necessary to master network instrumentation. Readers will learn to apply all the test, measurement, and monitoring tools critical to network performance. The 800-page book is priced at \$89.50. Contact McGraw-Hill Inc., Customer Services, P.O. Box 545, Blacklick, OH 43004; (800) 722-4726; fax (614) 755-5645; Internet: <http://www.mcgraw-hill.com>.

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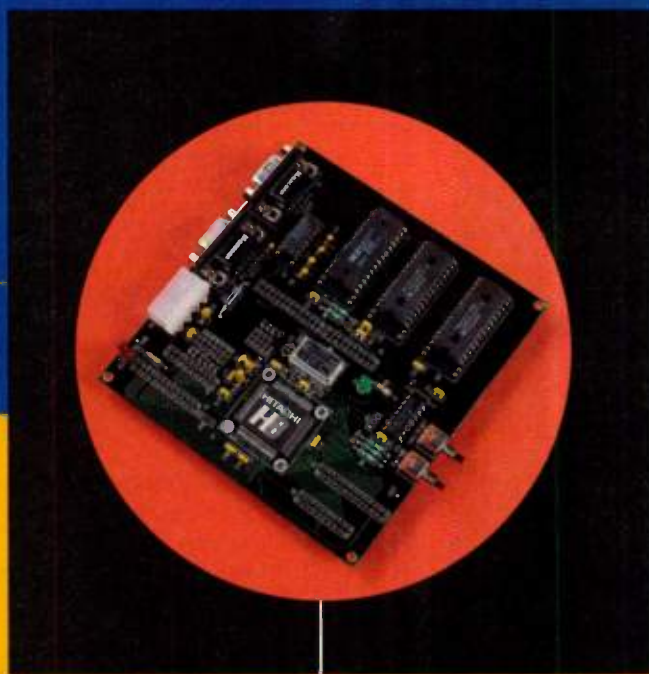
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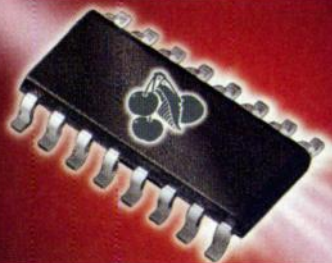
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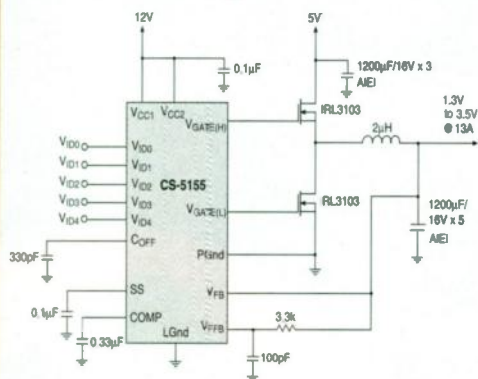
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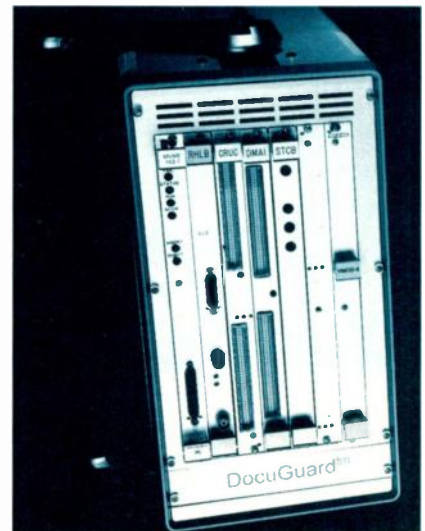
A CHERRY Company

Document Reader Picks Up Errors In The Blink Of An Eye

Here's an industry that you probably never put any thought toward: Laser and World Wide Web print-mail document integrity. In the print and print-mail inspection game, the primary concern is speed. How fast a company gets its mail out to the market is often dependent on how many errors need to be fixed before it can go out to the public. The number of errors needing to be corrected directly reflects the cost of the job, hence the old time = money postulate.

One company that has a solution to the problem of how to increase speed in printing while maintaining a high level of quality is Inspectron Corporation. Their DocuGuard is a print and print-mail inspection system that can read and verify printed information at web speed. According to the company, DocuGuard has the ability to read a wider range of characters at a higher speed than any other technology currently available in the U.S.

Information that the inspection system is capable of verifying includes bank statements, checks, coded forms, labels with high security specifications, and tickets. Typical errors that DocuGuard can detect are alphanumeric accuracy and matching, as well as sequencing. The technology can read alpha, numeric, alphanumeric, 1D and 2D bar codes, and graphic characters at extremely high speeds. DocuGuard is capable of making programmed decisions at machine speeds of up to 2750 ft/min.



For those readers interested in name dropping, in Europe, Bemrose Printing has used the technology to verify check numbers, Bording Purup AS verifies airline ticket bar codes with DocuGuard, Meiller Comcard GmbH uses it to verify credit card accounts, the German Lottery uses the verification system in their personalized lottery distribution, Bell & Howell uses DocuGuard in mailing systems and inserters, and Sigma Schede uses it in verifying business forms.

DocuGuard is based on a PSOS Real-Time operating system, and uses a VME bus. The system can be incorporated into other systems by OEMs or into existing print and print mail systems for particular enterprises. The technology was originally developed by Swedish company Rotocheck AB.

For more information, contact Inspectron Corporation, 150-F New Boston St., Woburn, MA 01801-6297; (617) 938-3700; fax (617) 938-5515.—DS

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READER SERVICE 135



QUICKNEWS

The ABCs Of Card Readers—

With the new security, encryption, and encoding standards quickly becoming realities, it's timely that smart-card readers are now being offered to OEMs and PC manufacturers. One company with a new smart-card interface architecture is SCM Microsystems. Their solution is called SmartOS.

SCM Microsystems is offering OEMs, integrators, and PC and peripheral device manufacturers a variety of smart-card reader technology from low-cost, single chips with software to full-featured multifunction controller chip sets with software. OEMs and integrators only pay for the components they need.

The smart-card technology is universal (card independent) and circumvents obsolescence via an upgradeable firmware component. The universal element is key in that electronic commerce will be conducted with a variety of different kinds of smart cards, from credit cards to company-issued photo-ID cards.

SmartOS allows smart cards to be integrated into an assortment of PCs and standalone devices. New applications include desktop, notebook, or network computers; USB or serial devices; keyboards; point-of-sale terminals, and vending machines. SmartOS' advantage lies in its flexibility. By being able to function either as an interface chip or a complete chip and firmware package, the solution allows designers to use only the essential components, thereby cutting cost.

SmartOS comprises three elements: SmartOS Firmware, SCM Microsystems' Interface Chip, and SCM Microsystems' Multifunction Interface and Controller Chip Set. The firmware gives the user the means to read and write information to and from all smart cards. It also can be upgraded to support new industry standards, operating systems, and/or smart cards.

The interface chip functions as the bridge between the smart card and the SmartOS layer. Similarly, the multifunction interface and controller chip set links the smart card to the SmartOS layer, but also supplies an LCD display output, keypad, and serial and parallel communication.

The pricing structure is varied, de-

pending on the needs of the integrator. For example, OEMs could possibly pay \$5 per unit, in quantities, for the interface chip and software solution. The full-featured, multifunction interface and microcontroller chip-set solution could run \$15 per unit, in quantities.

For more information, contact SCM Microsystems Inc., 131 Albright Way, Suite B, Los Gatos, CA 95032; (408) 370-4888; fax (408) 370-4880; Internet: <http://www.scmmicro.com>.

Speaking Of Cards— Now that many executives spend most of their time on the road with handheld PCs instead of bulky notebooks, effective handwriting recognition software has become an increasingly more valuable commodity. Teaming up for that purpose are SanDisk Corp. and Advanced Recognition Technologies (ART). Recently, SanDisk said that they would be bundling ART's smARTwriter PLUS for Windows CE with their CompactFlash memory cards.

smARTwriter PLUS supports English as well as European character sets. The software requires less than 100 kbytes and is loaded into system RAM. It allows users to write characters or symbols anywhere on their handheld PC screen to launch applications or enter words or figures into such programs as Pocket Word or Pocket Excel. Included within the software package is smARTwriter, smARTscribble, and Ink Pad.

CompactFlash memory cards are nonvolatile, requiring no power to retain data. They are rugged, removable cards being designed into new Windows CE-based handheld computers. The cards are available in 2-, 4-, 6-, 8-, 10-, 15-, and 20-Mbyte capacities.

For pricing and other product information, contact Bob Goligoski, SanDisk Corporation, 140 Caspian Ct., Sunnyvale, CA 94089; (408) 542-0463; fax (408) 542-0403; Internet: <http://www.sandisk.com>.

Far And Array— Breaking the storage barrier in video, CLARiiON is now offering the VF2000 Disk Array. The storage system uses internal code designed specifically for the video in-

dustry. The VF2000 also can be configured to store over 200 hours of broadcast-quality video.

One of the more prominent features of the solution is its fault-tolerance and performance levels. According to the company, typical SCSI-based storage subsystems only maintain peak performance levels for minutes at a time. CLARiiON's disk array sustains its peak performance levels for months at a time.

Always a plus, the VF2000 is scalable. When the user adds storage capacity, storage processors can be added. If a field-replaceable component fails, the user can hot swap it in under 60 seconds without tools.

In the high-bandwidth category, the CLARiiON VF2000 boasts a sequential read performance of over 30 Mbytes/s and a sequential write performance of over 22 Mbytes/s. The company sustains this performance via thermal calibrations of disks and other functions.

The VF2000 is based on a powerful RAID 3 engine. It features raw storage of 176 Gbytes in desk-side models or up to 704 Gbytes in the rackmount unit.

For more information, contact CLARiiON, Coslin Drive, Rt. 9, Southboro, MA 01772; (800) 67-ARRAY; (508) 480-7950; Internet: <http://www.clariion.com>.

Show Me The License Fees—

Eight companies (Fujitsu Ltd., General Instrument Corp., Lucent Technologies, Matsushita Electrical Industrial Co., Mitsubishi Electric Corp., Philips Electronics N.V., Scientific-Atlanta Inc., and Sony Corp.) and one university (Columbia) make up the patent pool created to license MPEG-2. MPEG-2, the digital video compression standard comprises 33 patents. Dimitris Anastassiou, professor of electrical engineering at Columbia developed one of the MPEG-2 compression technologies with one of his graduate students. Columbia will begin receiving licensing fees this year.

Contact Columbia University, 304 Low Library, Mail Code 4321, 535 W. 116 St., New York, NY 10027; (212) 854-5573.

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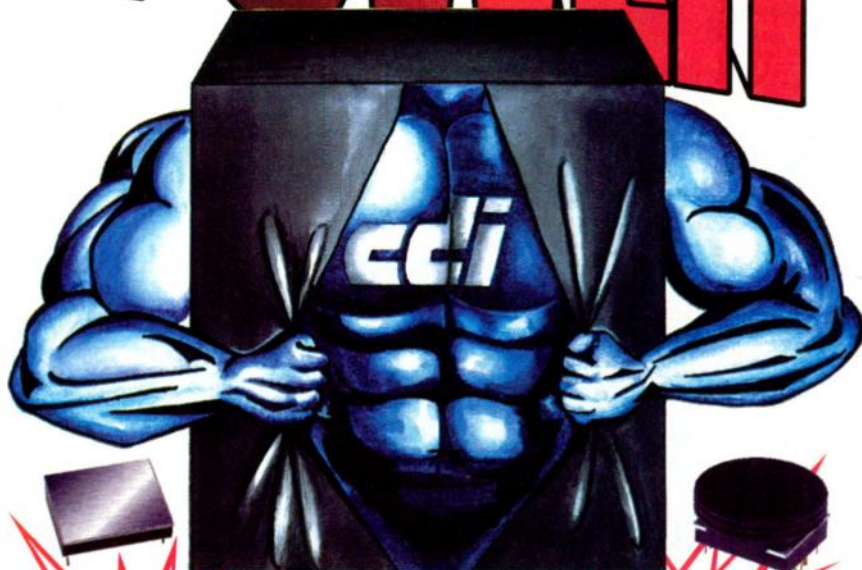
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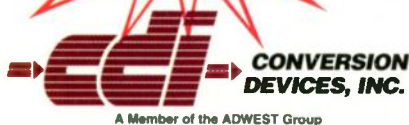
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READER SERVICE 122

THE ENVELOPE, PLEASE

Congratulations go out to Sandia National Laboratories whose researchers garnered eight of *R&D Magazine's* 100 most significant technological innovations of 1996. The technical trade publication stipulates that the winners must be applied inventions, rather than ideas that still have a ways to go before they're actually usable.

The following are brief descriptions of Sandia's winners:

- **Biological Microcavity Laser**—The device uses tiny fingers of laser light to image blood cells. Analysis is provided within minutes.

- **Nonvolatile field effect transistor device**—The memory technology uses protons to maintain screen memory when power fails. The key to the fab process is the hydrogen bath.

- **Filmetrics F-30 optical probe**—This device reflects visible or near-infrared light from films to measure their growth rates.

- **Hierarchical High-Performance Storage System (HPSS)**—The HPSS is the result of collaboration between industry, universities, and national laboratories to develop mass storage system software. Sandia's part in the story was developing algorithms to keep the systems secure.

- **Aztec**—The library of equation solvers free up scientists to focus on more fundamental issues in their problems.

- **GEOSEIS mini-hole seismic surface initiation system**—Within the system is the semiconductor bridge which sets off explosions to help seismic exploration.

- **Closed Loop Induction Process Controller**—This technique monitors the physical characteristics of a material as it undergoes changes during heating.

- **PQ2000 Power Quality System**—The system is a battery-based energy storage and delivery system that monitors and transfers power in lines before tragedy strikes.

For more information, contact Sandia National Laboratories, Albuquerque, NM 87185-0617; (505) 844-8066; fax (505) 844-6367; Internet: <http://www.sandia.gov>.—DS

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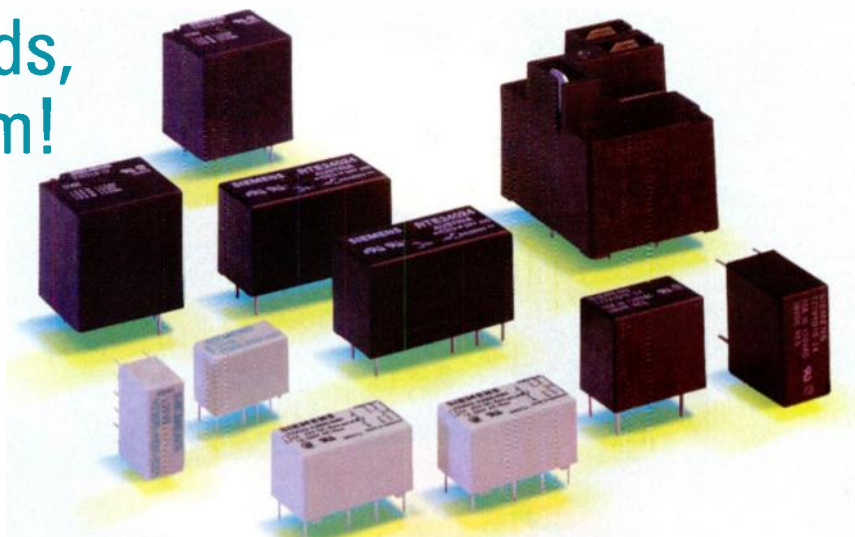
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Y2K UPDATE

Ever since the Year 2000 Date Change dilemma began to surface (on a widespread level), all kinds of vendors have been coming forward with their solutions. Two schools of thought emerged: Change the fields from two to four or work around the problem by using bridging technology. Then came the mass

media. Even *Newsweek* covered it—on the cover. I'll wager that *Time* will call it the "Bug of the Year."

Something different that I stumbled upon in my Internet travels is the Platinum Welcome 2000 site at <http://www.platinum.com/y2k>. One of the biggest advantages I could see from the site was the quick wait time.

In just a few seconds the page popped right up. OK, I'll admit that I do have a problem with graphics-heavy sites that take longer than three minutes to load.

Welcome 2000 is primarily a vehicle to sell Platinum's own solutions, but the site also profiles actual case studies.

Even more distinctive are the video clips of Y2K project managers telling their stories. Information technology managers will certainly find what they need here, especially in terms of conversion techniques, software requirements for compliance, and analysis tips.

The Weekend Planner arm of the site allows visitors to take a look at the scope of their conversion effort. Site visitors simply fill out a simple template and then they can see their progress. It also can help managers prevent snags in future compliance efforts.

Links featured at the site include Application Lifecycle, Business Intelligence, Consulting Services, Data Warehousing, Database Management, Education, Industry Applications, Internet and Intranet, Security, and Systems Management.

The site also features The Y2K Library, which contains a glossary of terms and links to useful and pertinent articles and sites. Anyone who has done any kind of research at all on his or her specialty knows that once a viable source for information is found, it often leads to other important sources. Platinum's Welcome 2000 site is no exception.

And, of course, if you do happen to be looking for solutions, Platinum has plenty of them. From their TransCentury Analysis to their Process Continuum, Platinum has the entire compliance covered. But, I'd definitely have to say that the most useful and defining part of the site is the real experiences with Y2K related here.

For further information on the Welcome 2000 site or the company's Y2K solutions, contact Platinum Technology Inc., 1815 S. Meyers Road, Oakbrook Terrace, IL 60181-5241; (630) 620-5000; fax (630) 691-0718.—DS



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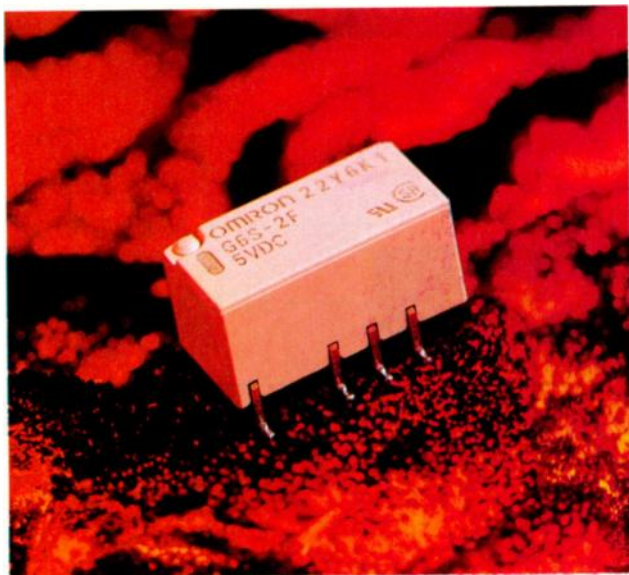
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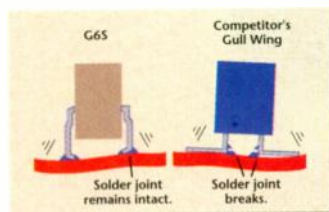
<http://www.ias.ie.philips.com>: Another site from Philips is the Philips Industrial Automation Systems' site. The decision to bring the company's machine automation information to the World Wide Web was based upon the fact that despite the company's presence in Europe, they needed to open up their position to the worldwide arena. At the site, visitors can find industrial automation systems facts, news, customer support, and upcoming events. Philips' 140-page industrial automation systems catalog is featured at the catalog (it's also available on paper). FAQs, technical information, and support tips will be updated regularly.

<http://www.wyle.com>: Recently, Wyle Electronics and IBM Interactive Media teamed to produce an easier-to-navigate World Wide Web site. At the site, visitors will find hundreds of links to Wyle's suppliers, including semiconductor manufacturers and computer products suppliers. Also featured at this web address are current issues of Wyle's RResources magazine, TechDirect, and entry forms for Idea Quest. TechDirect is Wyle's subscription information search program. Idea Quest is Wyle and *Electronic Engineering Time's* annual design contest for engineers. Samples of past entries can be obtained from the site as well.



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HOT PC PRODUCTS

Studio Suite is a studio management software package that allows all kinds of studios to organize their environments to optimize production and cut costs. Targeted toward professional, project, and video studios, Studio Suite eliminates the confusion associated with multiroom studios, as well as the home studio that's just breaking into the business. The software is cross-platform compatible, and features networking capabilities.

Modules included in the management software include Bar Code Labels, Calendar, Calls & Letters, Click-n-Book, Contacts, Equipment Inventory, Invoices, Maintenance, Part Inventory, Patchbay Labeler, Production Orders, Recall Sheets, Recording Budgets, Sample Librarian, Sessions, Tape Labels, Tape Library, Tape Stock, and Track Sheets.

The relational tool suite allows users to enter data only once to use it



throughout the entire system. Ever mindful of security measures, AlterMedia has made Studio Suite password protectable. My favorite feature, of course, is that the software is Y2K compliant.

Company name, address, phone number, and logo all can be entered into the software to be generated into letterhead and return address information on all printouts. A convenience, especially for extremely busy studio professionals, the spell checker is built in.

In the Contacts module, the user need only fill in the zip code for the city and state to be entered by Studio Suite. Four different standard-sized address and phone books come with the module. Holiday mailings are monitored automatically. The program will even print custom holiday envelopes. E-mail, web site information, express shipping, and credit card account information are all organized in this module. A feature not ordinarily found in software such as this is a tracking system for musicians' union affiliations.

The Calendar feature of Studio Suite is very easy to use, with color coding for events. The Click-n-Book aspect of the software allows studio managers to simply click on an hour to book a meeting or a session. If the user clicks on a magnifying glass, details of that session are easily revealed. Daily Overviews show the entire day's events at a glance.

Song and Track Sheets allow users to organize up to 56 tracks per song/reel. Instrument selection is menu based. The track status, whether it's the Master, Safety, Work Track, or any other track, is selectable. Information can be sorted by artist, engineer, label, producer, song, time-code start, or a number of other variables. Always important in this time of instantaneous lawsuits, samples and their publishers are tracked per song. Additionally, users will find built-in lyric sheets.

Equipment is tracked down to the serial number. Each room's equipment is monitored, providing an ideal listing service for insurance forms. The connectors used for each piece of equipment, as well as the cables and snakes attached to it, leading to the piece of equipment to which it's attached at the other end, are all noted in Studio Suite.

Maintenance reports develop a history of the repair costs, auto-totaling the total repair cost across the life of a piece of equipment. Speaking of cost, Studio Suite is priced at \$349.

For more information, contact Alter Media Inc., 2850 Delk Rd. #55B, Marietta, GA 30067; (800) 450-5740; fax (770) 303-0976; Internet: <http://www.studiosuite.com>.—DS

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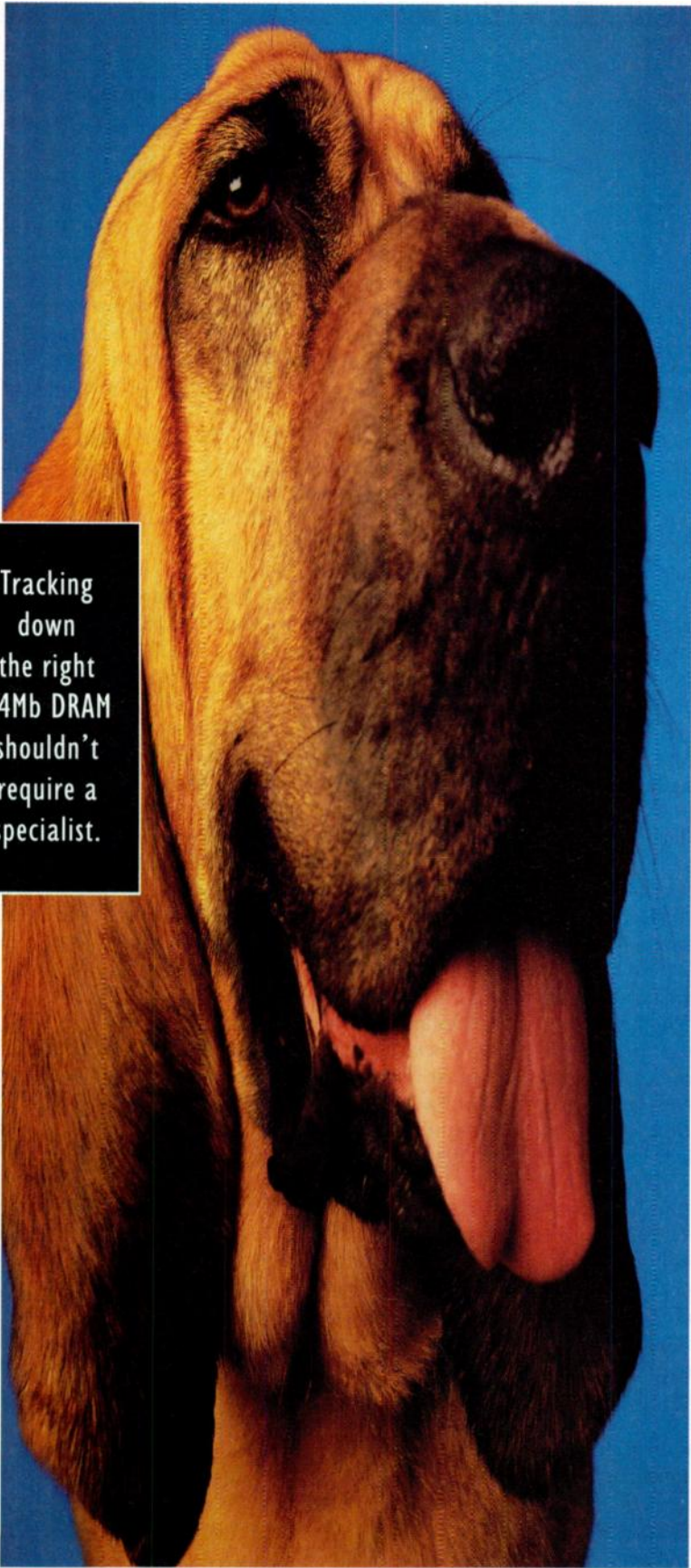


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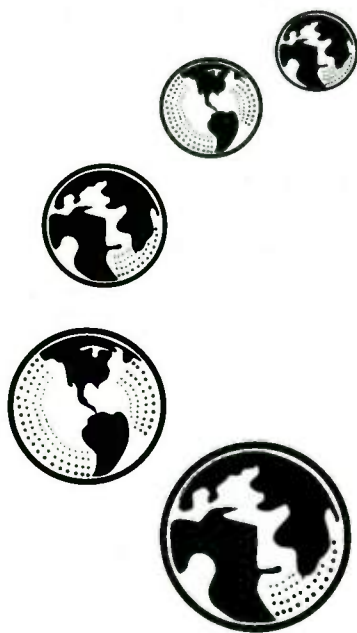
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L I S T S

TRUDEL TO FORM



JOHN D. TRUDEL
CONTRIBUTING EDITOR

Thank you for your support during the Patent Wars. I will try again to close the topic with a summary and move on.

The bills in Congress, H.R. 400 and S. 507, are lengthy and linked on my web page. They totally rewrite and sell off our patent system. There are five key points.

First is to shorten the term of patents. This damage was done in 1994, and we have not been able to repair it. In the past, administrative delays were buffered by the fact that patent term was 17 years after issue. The term is now a shorter 20 years after filing.

Second is to publish patent applications 18 months after filing. This gives your trade secrets to your competition before you have a patent to protect them. In the past, these were secret unless and until a patent issued.

Third is that even before your patent is granted, your competitors can oppose your pending patent application, thereby shortening the term of your patent. This "reexamination" is new and unique.

Fourth is that huge firms can focus the full fury of their litigation attorneys against you to oppose your patent in the Patent Office. Hearings used to be private matters between you and the patent office. Parts of the new bills make the PTO a private entity. Parts legalize (foreign) gifts and donations. This is all new.

Fifth is that the competition will have your attorneys running all over the world to take depositions, review foreign documents in foreign languages, and take evidence under foreign legal systems. This too will come out of your patent term and pocket.

The details are endless. Reexamination can continue even after you get a patent, just by paying fees to the patent office. Prior rights accrue to anyone in the world who has used your invention first. Perjurious witnesses will be prosecuted under the laws of the foreign country that will receive free use of the patent if prior user rights are obtained. Many think that it will take the courts decades to sort out all the changes. Some expect Constitutional challenges.

The big guns are thundering. Patent Commissioner Bruce Lehman told the *San Jose Mercury News* that critics of his bill are "in the Timothy McVeigh category." An April 15 missive to Congress from the Executive Office of the President said the administration "strongly opposes" restoring our patent term because "it would undermine the internationally agreed upon rule for a patent term of 20 years from the filing of the patent application."

Unfortunately, many of America's large multinational firms are lined up on the Japanese side—even the venture capital community is now neutral.

If Lehman succeeds, independent inventors and small firms will be severely affected. It may take a few years for venture capital to become a desert. Still, by the end, I predict that the Japanese redesign of our patent system will strangle even the largest U.S. technology firms.

"We create our own future," dear friends. We could work together to improve our nation's infrastructure to create jobs and gain competitive advantage. Instead, we allow foreign interests in Washington to take control, and we fight over the table scraps. That is *guanxi* capitalism and we allow this corruption at our peril.

John D. Trudel, CMC, provides business innovation consulting to selected clients. Lectures, keynotes, and workshops also are available. He is the author of "High Tech with Low Risk." The Trudel Group, 33470 Chinook Pl., Scappoose, OR 97056; (503) 638-8644; fax (503) 543-6361; e-mail: jtrudel@gstis.net; Internet: <http://www.trudelgroup.com>.

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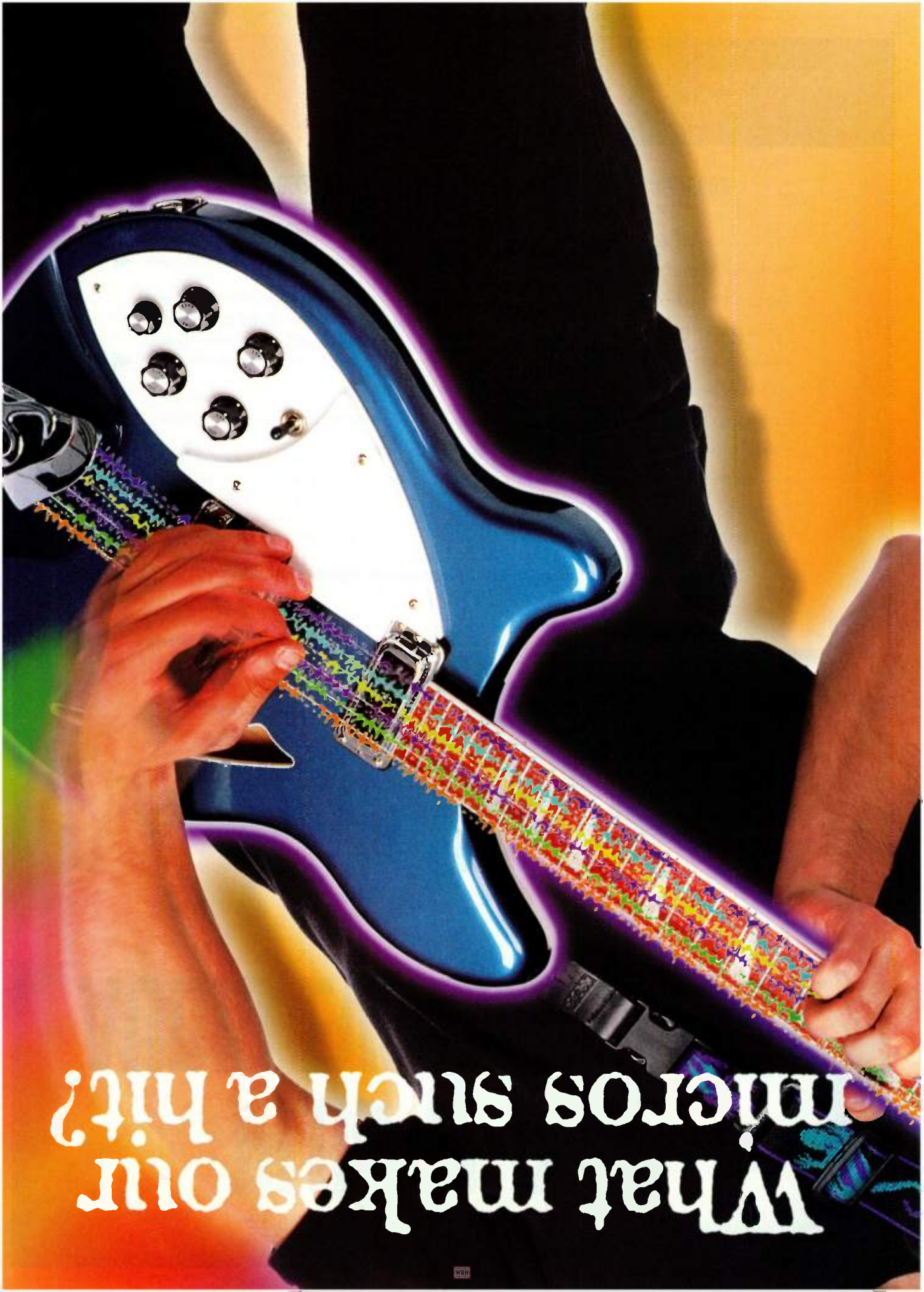
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ST62 MICROS. SOUND SOLUTIONS. ANY WAY YOU PLAY IT.

EASY

Novice or expert, micro design-ins have never been easier, thanks to SGS-THOMSONS's Windows®-based *automatic code generator*, the unique ST62 Realizer. Virtual equipment like oscilloscopes and Boolean, numeric, sine and square wave generators let you test for success *before* your design is complete. Optional stand-alone starter kits make 8-bit micro development as easy as A-B-C.

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SGS-THOMSON supports you with a ST62 device for virtually any 8-bit application. From micros with 1K program memory and the basic complement of peripherals to 8K devices with 16-bit AR timers, SPIs, UARTs, LCD drivers and more on-chip. Regardless of your application, ST backs you with everything you need to make your 8-bit micro design a hit.

Device	Program Memory Type				Program Memory	RAM x8	EEPROM x8	Timers	A/D Inputs	Serial Interface	I/Os (High Current)	Others	Package
	ROM	EPROM	OTP	Flash ROM									
ST6200	•	ST6201	•	•	1K	64	-	1x8-Bit	4x8-Bit	-	9 (3)	-	DIP16/SO16
ST6201	•	•	•	•	2K	64	-	1x8-Bit	4x8-Bit	-	9 (3)	-	DIP16/SO16
ST6203	•	ST6201	•	•	1K	64	-	1x8-Bit	-	-	9 (3)	-	DIP16/SO16
ST6208	•	ST6220	•	•	1K	64	-	1x8-Bit	-	-	12 (4)	-	DIP20/SO20
ST6209	•	ST6220	•	•	1K	64	-	1x8-Bit	4x8-Bit	-	12 (4)	-	DIP20/SO20
ST6210	•	ST6220	•	•	2K	64	-	1x8-Bit	8x8-Bit	-	12 (4)	-	DIP20/SO20
ST6215	•	ST6225	•	•	2K	64	-	1x8-Bit	16x8-Bit	-	20 (4)	-	DIP28/SO28
ST6220	•	•	•	•	4K	64	-	1x8-Bit	8x8-Bit	-	12 (4)	-	DIP20/SO20
ST6225	•	•	•	•	4K	64	-	1x8-Bit	16x8-Bit	-	20 (4)	-	DIP28/SO28
ST6230	•	•	•	•	8K	192	128	1x8-Bit/1x16-Bit AR	-	SPI/UART	20 (4)	-	DIP28/SO28
ST6232	•	•	•	•	8K	192	<128	1x8-Bit/1x16-Bit AR	-	SPI/UART	30 (9)	-	SDIP42/QFP52
ST6235	•	•	•	•	8K	192	128	1x8-Bit/1x16-Bit AR	-	SPI/UART	36 (12)	-	QFP52
ST6240	•	•	•	•	8K	216	128	2x8-Bit	12x8-Bit	SPI	24 (4)	LCD	QFP80
ST6242	•	•	•	•	8K	216	128	2x8-Bit	6x8-Bit	SPI	18 (4)	LCD	QFP64
ST6245	•	•	•	•	4K	140	128	2x8-Bit	7x8-Bit	SPI	19 (4)	LCD	QFP52
ST6246	•	•	•	•	4K	140	128	2x8-Bit	-	SPI	20 (4)	LCD	SDIP56
ST6252	•	ST6262	•	•	2K	128	-	1x8-Bit/1x8-Bit AR	-	-	9 (5)	LCD	DIP16/SO16
ST6253	•	ST6260	•	•	2K	128	-	1x8-Bit/1x8-Bit AR	7x8-Bit	-	13 (6)	-	DIP20/SO20
ST6255	•	ST6265	•	•	4K	128	-	1x8-Bit/1x8-Bit AR	-	-	21 (8)	-	DIP28/SO28
ST6260	•	•	•	•	4K	128	128	1x8-Bit/1x8-Bit AR	7x8-Bit	SPI	13 (6)	-	DIP20/SO20
ST6262	•	•	•	•	2K	128	64	1x8-Bit/1x8-Bit AR	-	-	9 (5)	-	DIP16/SO16
ST6263	•	ST6260	•	•	2K	128	64	1x8-Bit/1x8-Bit AR	7x8-Bit	-	13 (6)	-	DIP20/SO20
ST6265	•	•	•	•	4K	128	128	1x8-Bit/1x8-Bit AR	13x8-Bit	SPI	21 (8)	-	DIP28/SO28
ST6280	•	•	•	•	8K	320	128	1x8-Bit/1x8-Bit AR	12x8-Bit	SPI/UART	22 (10)	LCD	QFP100
ST6285	•	•	•	•	8K	288	128	1x8-Bit/1x8-Bit AR	8x8-Bit	SPI/UART	12 (4)	LCD	QFP80

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Halftime Report: 1997 U.S. Electronics Sales Up 9%

By the time you read this, football season will be underway. And with that comes everybody's favorite part of a television broadcast of a game—the halftime report. (O.K., it's a stretch.) Anyway, the halftime report gives you a chance to catch up on what's gone on so far, and what the future (or in this case, the second half) might be like.

In keeping with that spirit, a new report from the Electronic Industries Association (EIA) indicates that U.S. factory sales of electronics equipment, components, and related products totaled nearly \$219 billion for the first half of 1997. That figure represents a 9% increase over the 1996 first-half figure of \$200 billion.

In response to the increase in the numbers, Peter F. McCloskey, EIA's president, said, "The electronics industry continues to lead our nation's economy in growth and productivity. With every product sector showing growth over 1996, we are right on target for a strong year-end showing."

Following is a breakdown of the first-half 1997 numbers according to product sector:

- The Computers & Peripherals sector reached \$42.2 billion. According to the study, that's a growth of 6% over the 1996 figure of \$39.9 billion year-to-date (YTD).
- Electronic Components sales rose over 9% to \$70.5 billion, a 9% increase over last year's YTD figure of \$64.5 billion.
- The Telecommunications sector

saw strong growth in early 1997—hitting \$29.6 billion. That's up 14% over the 1996 figure of \$26.1 billion YTD.

- Defense Communications product sales are up 6% from last year's YTD figure of \$13.2 billion to \$14.1 billion.
- Sales of Electromedical Equipment rose by 7% from \$4.9 billion YTD in 1996 to \$5.3 billion in 1997.
- Consumer Electronics enjoyed an 8% increase to \$4.9 billion YTD in 1996 to \$5.3 billion in 1997.
- Industrial Electronics sales saw a 4% rise, with \$16.7 billion in the first half of 1997, over the 1996 YTD total of \$16.1 billion.
- The Other Related Products category in the report totaled \$35.4 billion, a 16% increase over the 1996 YTD figure of \$30.4 billion.

The EIA notes that Defense Communications products include specialized and defense-related communications and tracking devices. In addition, the Consumer Electronics category includes domestically manufactured audio, video, and blank media products. Significant amounts of products that are belong to the Telecommunications and Computer/Peripherals categories are sold through consumer channels, but are not separately identified within these areas.

For further information on this study, contact the EIA, 2500 Wilson Blvd., Arlington, VA 22201-3834; (703) 907-7500; fax (703) 907-7501; Internet: <http://www.eia.org>.

—MS

A Notable Class

There is a unique class of engineers whose art is concentrated on audio and video equipment and musical instruments. For that particular breed of engineer, Underwriters Laboratories (UL) has put together a new two-day seminar, "Audio/Video and Musical Instruments: Designing for Compliance to UL 6500 and IEC 65." The seminar will take place October 23-24 in Chicago, Ill.

Design engineers, as well as product safety managers and manufacturers, are encouraged to attend the new seminar. Basic safety topics, general construction techniques, and testing requirements used in UL 6500 compliance will be taught at UL's seminar. In addition, the seminar instructors will compare UL 6500 to other international standards in order to clarify the differences and similarities for confused participants.

Techniques for completing the ever-pertinent paperwork needed in the UL 6500 and IEC 65 submission process will be featured at the compliance seminar. Also covered at the UL seminar is strategic planning for the design and testing of future products. Important in the age of cross compatibility, the seminar instructors will explain how to relate UL 6500 to IEC 65 in designing products that will comply with both standards.

Representing UL at the seminar will be a group of instructors who are engineers from the Labs. The UL instructors work with clients on a regular basis to meet Canadian and IEC 65 requirements. Their qualifications include years of experience in product design and international compliance. Additionally, these instructors have extensive resumés in the audio and video industries in the product safety testing fields.

Appearing on over 10 billion products a year, the UL Mark has represented public safety on over 17,000 types of products for more than 100 years. The nonprofit laboratories have five U.S. locations: Northbrook, Ill.; Melville, N.Y.; Santa Clara, Calif.; Research Triangle Park, N.C.; and Camas, Wash. For more information, e-mail: seminars@ul.com or call (847) 272-8800.—DS

Correction

On page 48AA of the July 21 edition of QuickLook, one of the web site reviews that appeared in the "Flipping Through The Internet Rolodex" section needs clarification. TechOnLine is the name of the company whose web site is at <http://www.techonline.com>. The company has no affiliation with "DSP Group." The site is an information source for digital signal processing (DSP) information, including product and technology catalogs and company and product information. We apologize for the error.—Ed.

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OFF THE SHELF

The Beginner's Guide to Tube Audio Design is a primer for what vacuum tubes do and how to use them. The book shows readers how to design the building blocks that turn tubes, resistors, capacitors, and other hardware into amplifiers that make music reproduction possible. Specific topics addressed in the book discuss simple gain circuits, multistage basics, output stages and transformers, and stability networks. Included is a hands-on guide to construction techniques, tools, and to choosing components and tools. A special supplement includes three previously published working designs, complete with instructions, for readers to build for themselves. The 134-page book is priced at \$24.95. Contact Old Colony

Sound Lab, P.O. Box 243, Peterborough, NH 03458-0243.

The I²C Bus: From Theory to Practice guides readers through the world of microcontroller-managed serial buses that will enable them to design an I²C bus-based system for most applications. The book features examples of modular solutions at various levels of complexity, instruction on building bridges to other buses, and an accompanying diskette containing I²C bus instruction software. For more information, contact John Wiley & Sons Inc. 605 Third Ave., New, York, NY 10158-0012.

Analog Electronics: An Integrated PSpice Approach concentrates on

the introductory material associated with analog electronics. The book starts with a description of the basic active devices: diodes, transistors, and integrated circuits. It also includes discussions of frequency response, oscillators, filters, power supplies, and the interface between analog and digital circuitry. Key features of the text include simple circuit examples for each device discussed, descriptions and uses of simple equivalent circuits, chapters on the frequency response of RC networks and negative feedback, and over 200 worked examples and some 400 problems. For more information on the book, contact Prentice Hall Inc., One Lake St., Upper Saddle River, NJ 07458.

TIPS ON INVESTING

Investors are faced with many options that only individuals with the incentive to devote enormous amounts of time to research can hope to make consistently good decisions about their investments.

Investors also are aware, as never before, of the increasing costs of funding basic financial goals—educations for our children or grandchildren, a comfortable retirement, or the best care for an elderly relative. These goals should be approached from a long-term perspective, and many individual investors are uncertain how to develop a long-term investing strategy that is likely to enable them to work toward their aims.

Many investors find that they are best served by working with financial consultants to retain one or more of the many investment management firms that construct individual portfolios designed to meet the needs of each client. Professional investment management was once available only to large institutions and extremely wealthy individuals who could afford to commit millions of dollars to long-term investments. However, the industry has evolved, and now individual portfolio management is accessible to a wider spectrum of investors.

Professional investment managers offer various management styles, investment strategies, and portfolio options. These professionals—some of whom manage billions of dollars in assets for pension funds and other large institutions—sift through information that must continuously be analyzed to develop and implement a coherent investment strategy.

Professional managers are conversant with the histor-



HENRY WIESEL
CONTRIBUTING EDITOR

ical behaviors of the financial markets, and they spend much time following stock and bond activity. They also monitor economic and political developments that must be factored into a long-term plan to keep it flexible enough to be responsive to short-term challenges and potential opportunities in the investing environment. Some managers work under a clearly defined investment discipline which removes the emotional aspect that often skews the individual investor's decisions. These managers also have access to institutional-level trading capabilities that produce significant economies of scale.

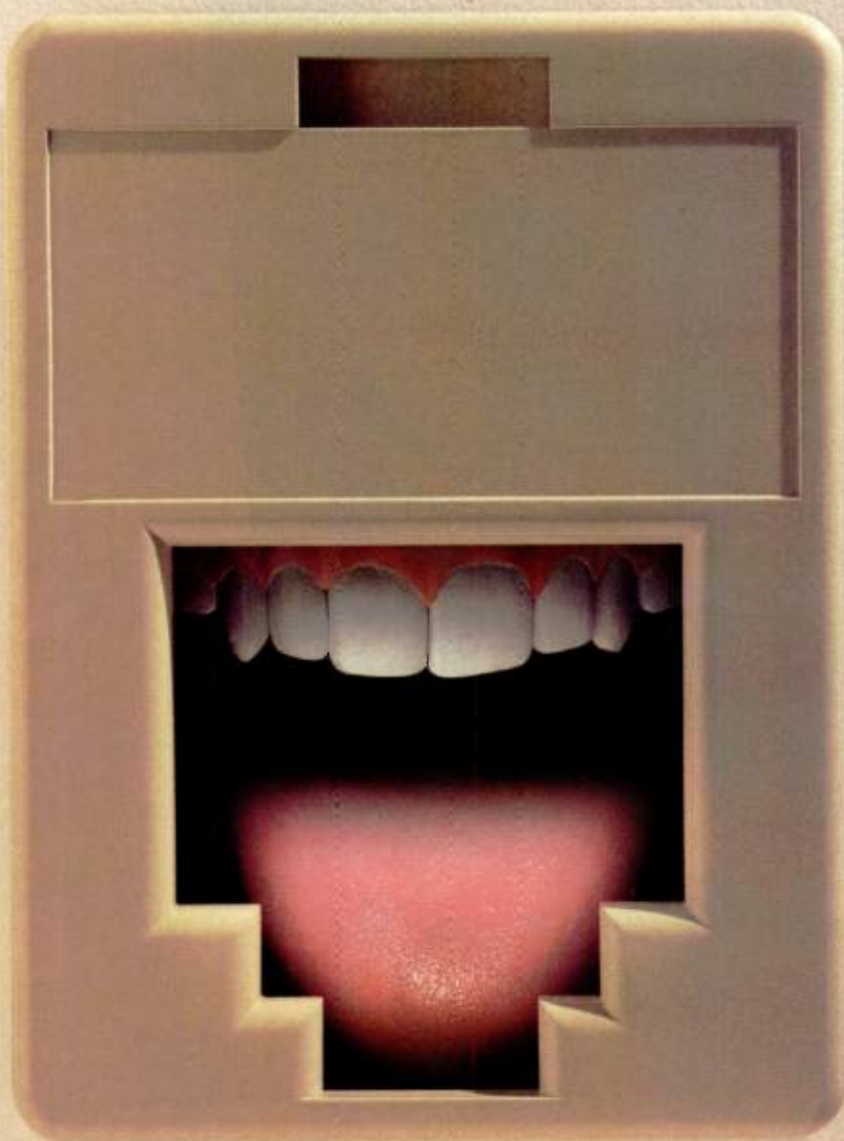
A financial consultant can guide you through the steps of defining your investment goals, identifying the professional manager(s) who will handle your account(s), and monitoring the activity of the managers you choose. It's usually best to stay with a manager through a market cycle, unless your goals or risk tolerance change.

Professional portfolio management is one method of making intelligent investment decisions. It can provide the investor with an organized basis of comparison for evaluating options, with the definition of his or her individual financial goals and a plan for pursuing them, and with regular feedback about the portfolio's performance. For many investors, the results of this method may be highly satisfactory.

Henry Wiesel is a vice president, financial consultant, and qualified pension coordinator at Smith Barney. He may be contacted at 1040 Broad St., 2nd Floor, Shrewsbury, NJ 07702; (800) 631-3331, ext. 8563.

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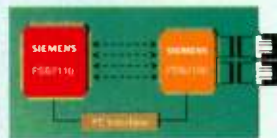
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Because our new 8-bit MCU, the KS88P0916, is a one-time-programmable EPROM part that is identical to our KS88C0916 *masked* part in footprint, electrical

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part. And you can then continue to build the product exactly as you have for the fast-out-the-gate version, over its entire life. Because with our minimal price premiums, there's little or no reason to switch to the masked part.

Let's say your product revolves around information that changes on a regular basis—and up till now, you've had to burn a new mask every time.

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STILL A Generation AHEAD.

INTERNET NEWS

The newest version of TakeFive Software's integrated, cross-platform development environment is nothing to sneeze at. SNIFF+ 2.3.1 can significantly pump up software development cycles. The object-oriented tool also includes the SNIFF+J Java Edition, which is a toolset that's been optimized for rapid Java development.

In the all-important edit-debug cycle, Java developers now have a new integrated graphical debugger with SNIFF+J. Because SNIFF+ preprocesses C and C++ code, Java developers can use all of the development tools that they typically would use with those code languages. The new tool's enhanced memory management also allows developers to create their complex applications more efficiently. Responding to the reuse trend, the SNIFF+J browsers allow developers to reuse their Java beans (components) and libraries. The browsers also enable developers to look at their projects at any level of detail.

The open development environment works independently of most of the other elements in the system, such as the tool environments, programming language, target system, or host environment. All the development tasks are pared down to one unified working environment. Developers can use Windows 95, NT, or UNIX operating systems. Browsers and cross-references for C, C++, CORBA IDL, FORTRAN, and Java are supplied with SNIFF+. The key to the tool is its cross-compatibility. Developers can easily jump from one programming language to another without having to learn how to negotiate a new environment. Even more flexible, SNIFF+ includes an Open Parser API to provide plug-in support for programming languages not already supported by the tool.

SNIFF+ carries a \$2990 price tag for a floating license, \$1995 for a Windows node-locked license, and \$995 for a Java parser. SNIFF+ 2.3.1 is available at the company's World Wide Web site below.

For more information, contact TakeFive Software Inc., 20813 Stevens Creek Blvd., Suite 200, Cu-

pertino, CA 95014; (408) 777-1440; fax (408) 777-1444; Internet: <http://www.takefive.com>.

With the advent of the World Wide Web, "agent" took on a new meaning. One particular agent, WebPosition Agent 1.0, works with site managers to let them know exactly where their site ranks with the premier search engines. It also shows these managers how to improve their sites' visibility.

WebPosition Agent for Windows 95/NT works by automating web site monitoring via search engines. The searches are organized by keyword, phrase, or URL. Reports are then sent back to each individual search engine. The 10 search engines that come included with the agent are AltaVista, Excite/AOL Netfind, HotBot, InfoSeek, LinkStar, Lycos, OpenText, WebCrawler, Yahoo, and YellowPages.

If the agent is used as a marketing tool, according to Innovative Solutions and Technologies (IST), developer of WebPosition, it has the potential of raising web-site traffic. Competitors' sites can be monitored. Ineffective keyword choices and lost pages can be identified and addressed. The marketing information derived by these 10 engines will provide a method for web managers to find new ways of helping other people find the site as quickly as possible.

WebPosition can be scheduled to run on a daily, weekly, or monthly basis, as well as on-demand. Automated tasks can be given to multiple search engines to run simultaneously. The agent alerts the user when a site or a page has been indexed. Off-line browsing also is supported by the tool. Auto-dialing and Internet connection is performed automatically in Windows 95/NT.

WebPosition PRO includes 10 domains and is priced at \$289. WebPosition Standard comes with 2 domain names and unlimited keywords, and is priced at \$189. Trial versions are available at the company web site.

Contact IST Inc., 2831 S. Monroe Ave., Joplin, MO 64804; (417) 781-3282; fax (417) 781-3299; Internet: <http://www.webposition.com>.

Candid Photography

If you find that people tell you that you're a particularly photogenic engineer, you may want to consider sending in a photo of yourself to the National Building Museum, Washington, D.C. Planning for National Engineers Week (February 22-28, 1998), the museum is inviting engineers to submit candid shots of themselves or others at work. The new exhibit is entitled, "Breaking Through: The Creative Engineer."

The exhibit, sponsored by the Institute of Electrical and Electronics Engineers (IEEE) along with over 50 other organizations, will feature a wall of photographs of actual engineers. Some of the photos will be those submitted, while others will be of historical figures or engineers included elsewhere in the exhibit. Amongst the photos will be quotations from the engineers about what they perceive to be creativity in their profession.

The curator of the new exhibit is Robert Friedel, the former director of the IEEE Center for the History of Electrical Engineering. Friedel is the force behind the call for the photos and is asking specifically for engineers to supply shots taken in the office or lab, or at the computer. Additionally, participants should supply some creative writing with their photos, regarding inventive engineering.

If you do plan to submit a photo of yourself (or a lab partner) demonstrating your creativity at work, here's where to send it:

Breaking Through
National Building Museum
401 F St. N. W.
Washington, DC 20001

Included should be a black-and-white or color photo; names and occupations of the individuals in the photo; location and date of the photo; creative thoughts; name, address, and phone number of the person submitting the snapshot, and a signed statement giving permission to use the photos and quotations in the exhibit. Send a self-addressed, stamped envelope, too, if you'd like the materials returned to you.—DS

Electronic Design

Product Mart

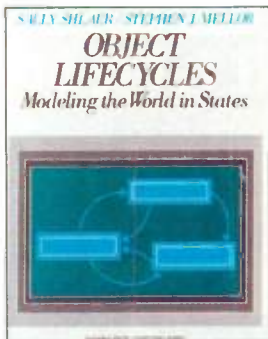
Book

Object Lifecycles Modeling the World in States

Sally Shlaer & Stephen J. Mellor

This book describes a practical and pragmatic object-oriented approach to domain analysis by showing how to model the dynamic behavior of a system in terms of state and process models. Provides a strictly defined, multi-level formalism powerful enough to be mapped into a variety of designs; techniques for formalization of object lifecycles, dynamic relationships, contention problems, and thread of control analysis; and a ready-to-use tailoring of 2167A's analysis DID's, with justification and detailed instructions for compliance. Includes language-independent notation for Object-Oriented Design (OODLE) and strategies for code generation from OOA models using Recursive Design.

251 pp, softcover book, \$45.00, Item B2547PM



Book

Object-Oriented Multidatabase Systems

Edited by Omran A. Bukhres & Ahmed K. Elmagarmid

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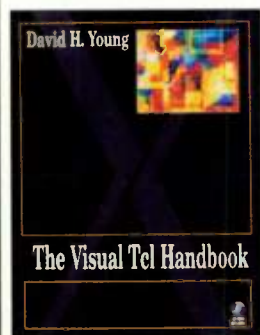
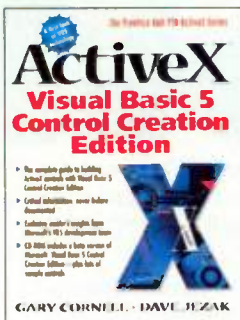
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The Visual Tcl Handbook

David H. Young

Organized into four parts, this text focuses on examples of the most commonly used commands with explanations that put the commands in a practical context. The introduction demonstrates state-of-the-art scripting using Tcl's architecture; the following overview highlights TclX commands; Visual Tcl discusses widget-building commands, callbacks and design strategy, and concludes with command

pages of references for Tcl, TclX, Vt and Vx. Features example code and user interface design topics driven by real-world UNIX administration tasks. The accompanying CD contains the complete SCO Visual Tcl 1.0 run-time and development environments.

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White Collar Blues Makes The Scene

Blues is a musical form unique to America. The blues tradition has helped us share our sorrow and shown us how to transform our agonized cries into triumphant anthems. Born out of slavery and hard times, blues music has brought comfort and joy to generations of oppressed souls in farms and factories. Now in its latest incarnation, blues has finally arrived in the newest land of oppression: the corporation.

Although conceived as a comedy album, "Certified Business Blues," by Marketing Mike & The Suits, manages to deliver some pretty authentic blues riffs along the way. If you can imagine what might happen if Dilbert were to participate in an all-night jam session with the Blues Brothers, you might have a sense of the mayhem this rowdy little band has managed to unleash from its basement recording studio.

The album's producers/writers/performers—Marketing Mike and his wife, Mrs. Mike—are actually well-known high-tech public relations consultants in California's Silicon Valley. After suffering through years of ritual abuse at the hands of corpora-

tions, their revenge is at hand in this prickly little CD. Nothing is sacred as the band unleashes its wrath upon a variety of topics, ranging from greedy, inept managers to the absurd language of modern business. Among



the standout cuts are: "I Survived the Reorg (But I Wish They'd Laid Me Off)," "Voice Mail Hell," and "Cubicle Blues."

In their song, "Corporate Speak," The Suits gleefully skewer the collection of platitudes, euphemisms, and doublespeak that passes for commu-

nication with employees in most companies. Among the best examples are; "right-sizing" equals "layoffs", "redeployment" is actually "you're demoted," and "employee empowerment" is really "give us twice the work for the same paycheck." For anyone who has ever carried a pager, or cellular phone, "High-Tech Leash" should strike home. It describes the plight of an overworked employee who can't get away from his job, no matter how far or fast he or she runs.

While not every song is a gem, the combination of Mr. and Mrs. Mike's vocals and the musicians backing up The Suits in this album manage to give several selections the soulful authenticity of old-time blues. In any case, all the lyrics are delightful, and deserve ear-play at the company Christmas party, in the car after a trying day, or secretly broadcast across your building's PA system. Priced at \$14.95 for a CD, and \$9.95 for cassette, "Business Blues" is much cheaper than a case of aspirin, and probably more effective at helping you cope with workplace stress. Contact BizBlues Records at (800) 254-5945 to place your order, or look up their World Wide Web site at: <http://www.bizblues.com>.

Lee Goldberg

It's That Time Again!

Though you may still be working on your tan as of this writing, it's time to look ahead to the new year. Especially if you're a designer of OEM portable and mobile products. Why, you ask? Because the fifth annual **Portable by Design Conference**, sponsored by *Electronic Design*, will take place Feb. 9-13, 1998, at the Santa Clara Convention Center, Santa Clara, Calif. And if you're interested in participating in the technical program, it's time for you to get out of the sun and get to work!

The editors of *Electronic Design* are soliciting technical papers for presentation at the **1998 Portable by Design Conference**. Designers are invited to share their expertise by submitting proposals for papers that emphasize problem solving and provide insights regarding the design of portable products. Following are some

of the topics that will be presented at the conference:

- Low-power microprocessors and microcontrollers
- Hardware- and software-based power-management techniques and power-control circuits
- Low-power analog design and power-control circuits
- PCMCIA
- Displays
- Packaging and thermal issues
- Battery management
- Battery technology
- Communications and connectivity

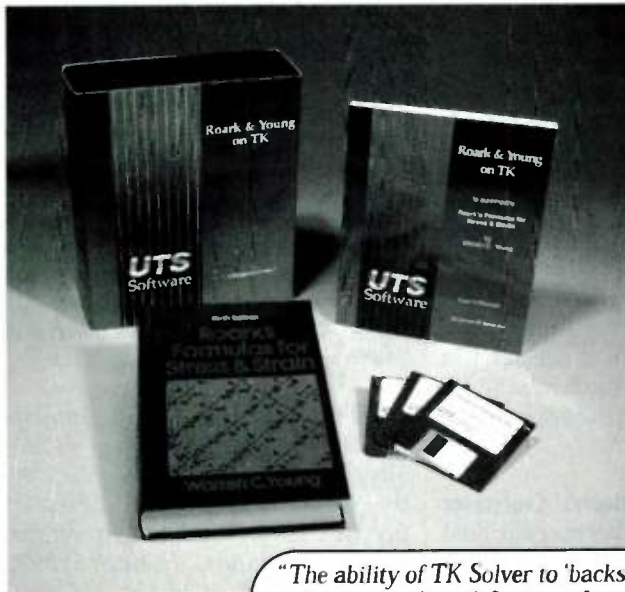
If you're interested in participating, send an abstract describing your proposed paper by Sept. 26 to: Program Chair, **Portable by Design Conference**, c/o *Electronic Design*, 611 Route 46 West, Hasbrouck Heights, NJ 07604; fax (201) 393-0204; e-mail: portable@class.org. If you have any questions, call (201) 393-6090.—MS

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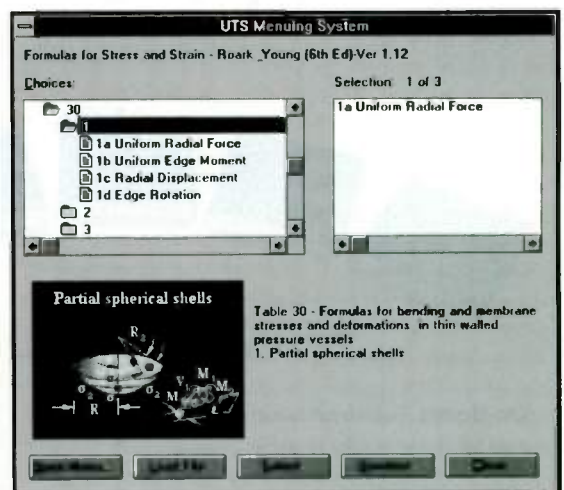
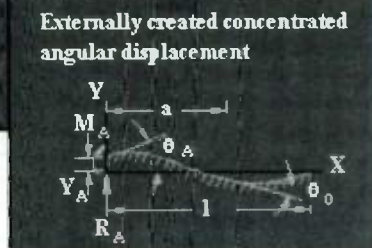
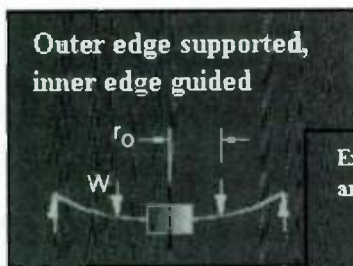
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AUTOTESTCON '97, September 22-25. Disneyland Hotel, Anaheim, California. Contact Robert C. Rassa, Hughes Aircraft, Post Office. Box 92426, MS R07/P553, Los Angeles, California 90009-2426; (310) 334-4922; fax (310) 334-2578; e-mail: rcrassa@cgate.hac.com.

Electrical Overstress/Electrostatic Discharge Symposium, Sept. 23-25. Santa Clara Convention Center, Santa Clara, CA. Contact ESD Association, 7902 Turin Rd., Suite 4, Rome, NY 13440-2069; (315) 339-6937; fax (315) 339-6793.

Fifth China International Electronics Exhibition (CIEE '97), Sept. 24-28. China Inter-

national Exhibition Centre, Beijing. Contact Gu Jinjing, CEIEC, P.O. Box 140, Beijing, 100036 China; (011) 8610 6822 3909; fax (011) 8610 6821 3348.

Eastern Regional Conference on Crystal Growth & Epitaxy, ACCGE/East-97, September 28-Oct 1. Bally's Park Place Hotel & Casino, Atlantic City, New Jersey. Contact Louis G. Casagrande, (516) 346-6379; fax (516) 346-3670; e-mail: Lou_Casagrande@atdc.grumman.com, or Ed Porbansky, Conference Secretariat, 163 Carson Drive, Colonia, New Jersey 07067; (908) 382-1806.

Embedded Systems Conference, Sept. 29-Oct. 2. San Jose Convention Center, San Jose, California. Contact Liz Austin, Miller Freeman Inc., (888) 239-5563; (415) 538-3848; e-mail: esc@mfi.com.

PCI Plus Europe Developers' Conference and Expo, Sept. 29-Oct. 2. International Conference Center/Messe Berlin, Berlin, Germany. Contact Anna-books, 11838 Bernardo Plaza Ct., San

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PCI Plus Europe, Oct. 1-2. The International Conference Center (ICC), Messe Berlin, Germany. Contact Active Exhibitions Europe at Post Office Box 2114, 5300 CC Zaltbommel, The Netherlands. (31) 418 512999; fax (31) 418 515115; e-mail: active@otsgroup.nl; Internet: http://www.aexpo.com, or Anna-books, 11838 Bernardo Plaza Court, San Diego, CA 92128; (800) 462-1042; fax (619) 673-1432; e-mail: 73204.3405@compuserve.com; Internet: http://www.annabooks.com.

Fourth International CAN Conference (ICC), Oct 1-2. Berlin, Germany. Contact CAN in Automation, Am Weichselgarten 26, D-91058 Erlangen, +49 9131-601091; fax +49 9131-601092.

IPCWorks '97, Oct. 5-9. Hyatt Regency Crystal City, Washington, D.C. Contact David Bergman, vice president, technical programs, (847) 509-9700 ext 340; fax (847) 509-9798.

NEPCON Texas '97, October 7-9. Info-mart, Dallas, Texas. Contact Reed Exhibition Companies, Customer Service, (800) 467-5656; fax (203) 840-9656; e-mail: inquiry@nepcontexas.reedexpo.com; http://nepcon.reedexpo.com.

IEEE Ultrasonics Symposium, Oct. 7-10. Marriott Hotel, Toronto, Canada. Contact Stuart Foster, Dept. of Medical Biophysics, Room S-658, Sunnybrook Health Science Ctr., 2075 Bayview Ave., Toronto, Ontario, M4N 3M5, Canada; e-mail: stuart@owl.sunnybrook.utoronto.ca.

Small Space Solutions

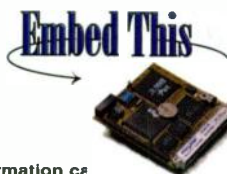
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DESIGN NOTES

LTC1474/LTC1475 High Efficiency Switching Regulators Draw Only 10 μ A Supply Current – Design Note 162

Greg Dittmer

Maximizing battery life, one of the key design requirements for all battery-powered products, is now easier with Linear Technology's new family of ultralow quiescent current, high efficiency step-down regulator ICs, the LTC1474 and LTC1475. The LTC1474/LTC1475 are step-down regulators with on-chip P-channel MOSFET power switches. These regulators draw only 10 μ A supply current at no load while maintaining the output voltage. With the on-chip switch (1.4 Ω at $V_{IN} = 10V$), minimal external components are necessary to make a complete, high efficiency (up to 92%) step-down regulator. Low component count and the LTC1474/LTC1475's tiny MSOP packages provide a minimum-area solution to meet the limited space requirements of portable applications. Wide supply voltage range (3V to 18V) and 100% duty cycle capability for low dropout allow maximum energy to be extracted from the battery, making the LTC1474/LTC1475 ideal for moderate current (up to 300mA) battery-powered applications.

The peak inductor current is programmable via an optional current sense resistor to allow the design to be optimized for a particular application and to provide short-circuit protection and excellent start-up behavior. Other features include Burst Mode™ operation to maintain high efficiency over almost four decades of load current, an on-chip low-battery comparator and a shut-down mode to further reduce supply current to 6 μ A. The LTC1475 provides ON/OFF control with pushbutton switches for use in handheld products.

LT, LTC and LT are registered trademarks of Linear Technology Corporation. Burst Mode is a trademark of Linear Technology Corporation.

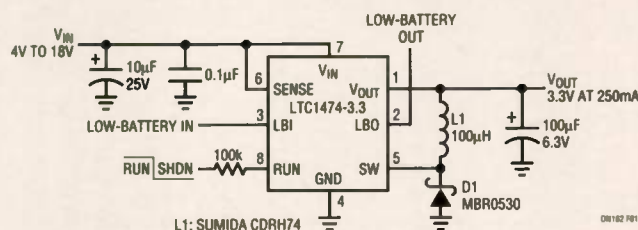


Figure 1. High Efficiency Step-Down Converter

Inductor Current Control

Excessive peak inductor current can be a liability. Lower peak current offers the advantages of smaller voltage ripple ($\Delta V = I_{PEAK} \times ESR$), lower noise and less stress on alkaline batteries and other circuit components. Also, lower peaks allow the use of inductors with smaller physical size. The LTC1474/LTC1475 provide flexibility by allowing the peak switch/inductor current to be programmed with an optional sense resistor to provide just enough current to meet the load requirement. The sense resistor value required to set the desired peak inductor current is easily calculated from $R_{SENSE} = 0.1/(I_{PEAK} - 0.25)$. Without a sense resistor (that is, with Pins 6 and 7 shorted) the current limit defaults to its maximum of 400mA. Using the default current limit eliminates the need for a sense resistor and associated decoupling capacitor.

3.3V/250mA Step-Down Regulator

A typical application circuit using the LTC1474-3.3 is shown in Figure 1. This circuit supplies a 250mA load at 3.3V with an input supply range of 4V to 18V (3.3V at no load). The SENSE pin is shorted to V_{IN} to set the peak inductor current to the 400mA maximum to meet the load requirement. Since the output capacitor dominates the output voltage ripple, an AVX TPS series low ESR (0.15 Ω) output capacitor is used to provide a good compromise between size and low ESR. With this capacitor the output ripple is less than 60mV.

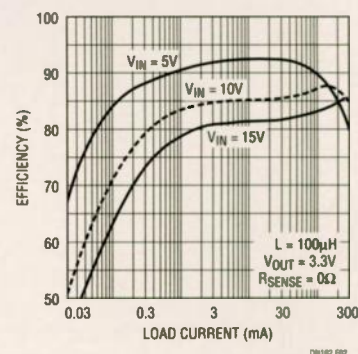


Figure 2. Efficiency vs Load for Figure 1's Circuit

The efficiency curves for the 3.3V/250mA regulator at various supply voltages are shown in Figure 2. Note how the efficiency remains high down to extremely light loads. Efficiency at light loads depends on low quiescent current. The efficiency drops off as the load decreases below about 1mA because the non-load-dependent 10 μ A standby current loss then constitutes a more significant percentage of the output power. This loss is proportional to V_{IN} and thus its effect is more pronounced at higher V_{IN} .

Care must be used in selecting the catch diode to maximize both low and high current efficiency. Low reverse leakage current is critical for maximizing low current efficiency because the leakage can potentially approach the magnitude of the LTC1474/LTC1475 supply current. Low forward drop is critical for high current efficiency because loss is proportional to forward drop. These are conflicting parameters, but the MBR0530 0.5A Schottky diode used in Figure 1 is a good compromise.

3.3V/10mA Regulator from a 4mA to 20mA Loop

The circuit shown in Figure 3 is a 3.3V/10mA regulator that extracts its power from a 4mA to 20mA loop. This circuit demonstrates how an LTC1474/LTC1475-based regulator

is easily optimized for such low current applications. The 2 Ω sense resistor limits the peak inductor current to 40mA to minimize current ripple and provide good efficiency (84%). The 330 μ H inductor is a good value to use at this current level to keep the frequency low enough to avoid excessive switching losses without being so large that DCR losses are significant (see inductor section of the data sheet). The Zener diode at the input clamps the input voltage to 12V, which is then converted to 3.3V. This enables the 4mA (min) input current to be more than doubled at the output.

LTC1475 Pushbutton ON/OFF Operation

The LTC1475 provides the option of pushbutton control of ON/OFF mode for handheld products. In contrast to the LTC1474's ON/OFF mode, which is controlled by a voltage level at the RUN pin (ground = OFF, open/high = ON), the LTC1475 ON/OFF mode is controlled by an internal S/R flip-flop that is set (ON) by a momentary ground at the $\overline{ON}$ pin and reset (OFF) by a momentary ground at the LBI/OFF pin. This provides simple ON/OFF control with two pushbutton switches. A simple implementation of this function is shown in Figure 4.

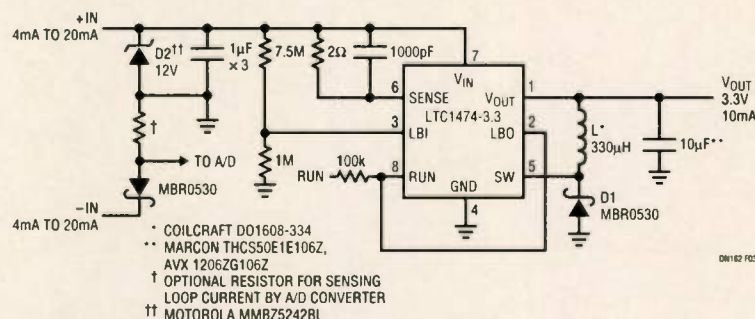


Figure 3. High Efficiency 3.3V/10mA Output from 4mA to 20mA Loop

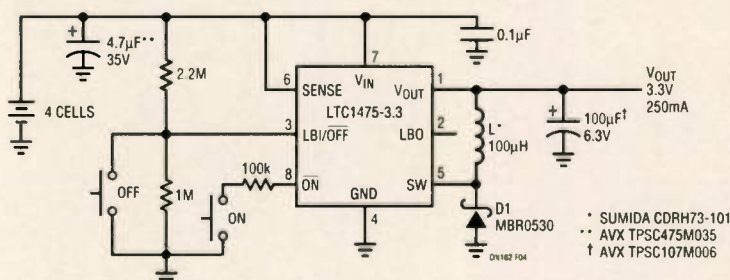


Figure 4. Pushbutton ON/OFF 3.3V/250mA Regulator

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IEEE Telecommunications Energy Conference (INTELEC '97), Oct. 19-23. World Congress Centre, Melbourne, Australia. Contact Robert N.K. Thuan, Network Products-Telstra Corp. Level 14, 242 Exhibition St., Melbourne, Victoria 3000, Australia; +61 3 634 6216; fax +61 3 632 3607

Sensors Expo, Oct. 21-23. Cobo Convention Center; Detroit, Michigan. Contact Expocon Management Associates Inc., (203) 256-4700; e-mail: sensors@expocon.com; Internet: <http://www.expocon.com>.

Fourth IEEE International Conference on Image Processing (ICIP '97), Oct. 26-30. Fess Parker's Red Lion Resort, Santa Barbara, CA. Contact Sanjit K. Mitra, Electrical & Computer Engineering, University of California, Santa Barbara, California 93106-9560; (805) 893-3957; fax (805) 893-893-3262; e-mail: mitra@ece.ucsb.edu.

11th Systems Administration Conference (LISA '97), Oct. 26-31. Town & Country Hotel, San Diego, CA. Contact USENIX Conference Office, 22672 Lambert Street, Suite 613, Lake Forest, CA 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: <http://www.usenix.org>.

SYSTEMS 97, Oct. 27-31. Munich Trade Fair Center, Munich Germany. Contact Messe Munchen GmbH, Messsegelände, D-80325 Munchen, +49 (89) 51070; fax +49 (89) 51 07506; Internet: <http://www.sysems.de>; e-mail: info@messe-muenchen.de.

19th Annual International Conference of the IEEE Engineering in Medicine & Biology Society, Oct. 29-Nov. 2. Sally Chapman, Secretariat, National Res. Council of Canada, Bldg. M-55 Rm. 393, Ottawa, KIA OR8, Canada; (613) 993-4005; fax (613) 954-2216.

19th International Conference of the IEEE Engineering in Medicine & Biology Society, Oct. 30-November. 2. Chicago Marriott Downtown, Chicago, Illinois. Contact Meeting Management, 2603 Main Street, Suite 690, Irvine, California 92714; (714) 752-8205; fax (714) 752-7444; e-mail: embs97@ieee.org; Internet: <http://www.eecs.uic.edu/~embs97>.

NOVEMBER

IEEE International Test Conference (ITC), Nov. 1-5. Sheraton Washington Hotel, Washington, DC. Contact ITC, 655 15th St., N.W., Suite 300, Washington, DC 20005; (202) 639-4164; fax (202) 347-6109.

Voice, Video, & Data Communications Conference & Exhibition, Nov. 2-6. Dallas, TX. Contact SPIE Exhibits Dept., P.O. Box 10, Bellingham, WA 98227-0010; (360) 676-3290; fax (360)-647-1445; e-mail: exhibits@spie.org.

IEEE Global Telecommunications Conference (GLOBECOM '97), Nov. 3-7. Phoenix, AZ. Contact Nigel Reynolds, 15436 N. First Ave., Phoenix, AZ 85023; (602) 942-5583; fax (602) 942-4542; e-mail: nigelaz@aol.com.

WESCON '97, Nov. 4-6. San Jose Convention Center and Santa Clara Convention Center, San Jose and Santa Clara, CA. Contact Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045-3194; (800) 877-2668; fax (310) 641-5117; e-mail: wescon@ieee.org.

IEEE Intelligent Transportation Systems Conference (ITS '97), Nov. 9-12. Boston Park Plaza Hotel, Boston, MA. Contact Richard Sparks, 8 Richard Rd., Bedford, Massachusetts 01730; (617) 862-3000; fax (617) 863-0586; e-mail: r.sparks@ieee.org.

Productronica '97, November 11-14. Messsegelände, Munchen, Germany. Contact Messe Munchen GmbH, Messsegelände, D-80325 Munchen, Germany; +49 (89) 51 07-0; fax +49 (89) 51 07-506; e-mail: info@messe-munchen.de; Internet: <http://www.Productronica.de>.

23rd Annual Conference of IEEE Industrial Electronics (IECON '97), Nov. 9-14. Hyatt Regency Hotel, New Orleans, Louisiana. Contact Michael Greene, 200 Broun Hall, Electrical Engineering, Auburn University, Auburn, Alabama 36849-5201; (334) 844-1828; e-mail: greene@eng.auburn.edu.

Asian Test Symposium, Nov. 17-19. Akita, Japan. Contact Y. Takamatsu, +81 89 927-9955; e-mail: takamatsu@cs.ahime-u.ac.jp.

IPC National Conference: Solutions for Ultra-High-Density PWBs, November 20-21. Biltmore Hotel, Santa Clara, California. Contact John Riley, IPC director of education, (847) 509-9700 ext. 308.

DECEMBER

36th IEEE Conference on Decision & Control, December 8-12. Hyatt Regency, San Diego, California. Contact Ted E. Djaferis, Department of Electrical & Computer Engineering, University of Massachusetts, Amherst, Massachusetts 01003; (413) 545-3561; fax (413) 545-1993; e-mail: djaferis@ecs.umass.edu.

Workshop on Internet Technology & Systems (WITS), Dec. 9-12. Marriott Hotel, Monterey, California. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, California 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: <http://www.usenix.org>.

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Annual Reliability & Maintainability Symposium/Product Quality & Integrity (RAMS), January 20-22. Anaheim Marriott, Anaheim, California. Contact V.R. Monshaw, Consulting Services, 1768 Lark Lane, Cherry Hill, New Jersey 08003; (609) 428-2342.

Photonics West, January 24-30. San Jose, California. Contact the SPIE Exhibits Department, Post Office Box 10, Bellingham, Washington 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

Seventh Security Symposium, January 26-29. Marriott Hotel, San Antonio, Texas. Contact USENIX Conference Office, 22672 Lambert Street, Suite 613, Lake Forest, California 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: <http://www.usenix.org>.

IEEE Power Engineering Society Winter Meeting, January 31-February 5. Tampa, Florida. Contact Jim Howard, Tampa Electric Co., Post Office Box 111, Tampa, Florida 33601; (813) 228-4653; fax (813) 228-1333; e-mail: j.howard@ieee.org.



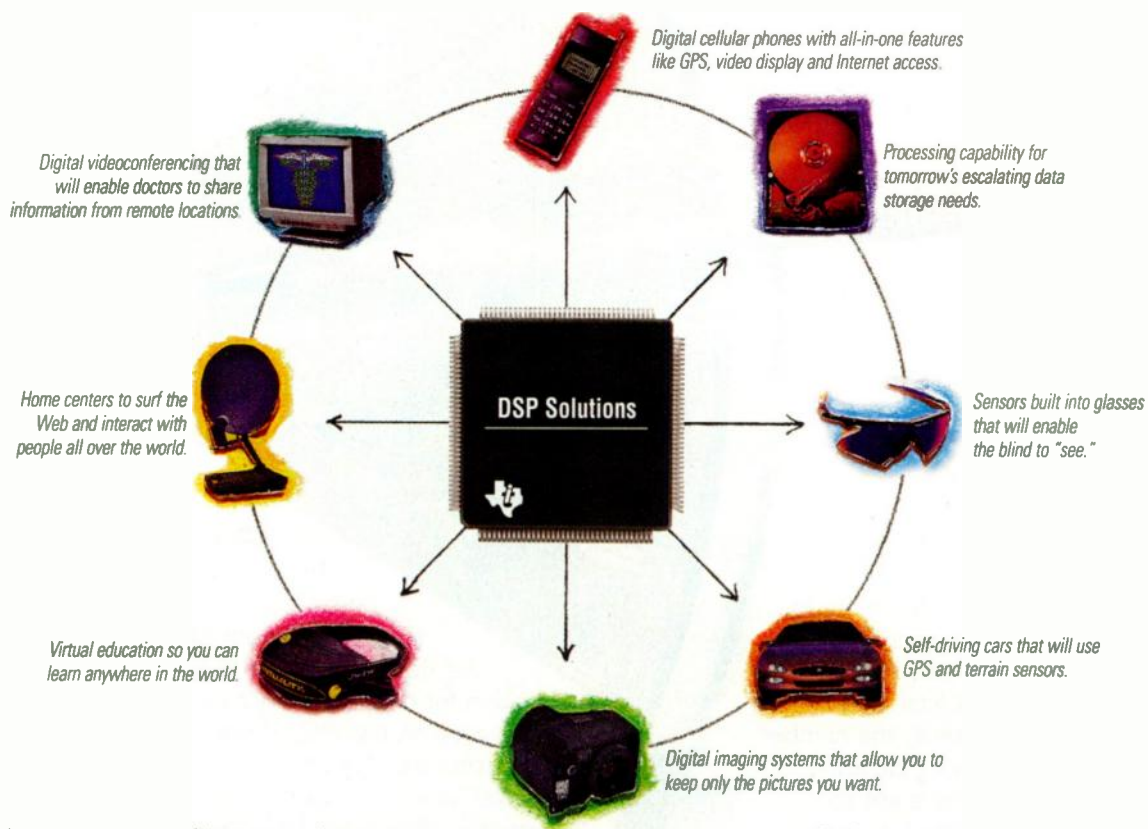
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Get The Most Out Of The TMS320C32 With An x86 Host

Squeezing Performance From A C32-Based DSP System Doesn't Require Black Magic; Just Careful Design With Attention to Detail.

CHRIS STOLARIK, RadiSys Corp., 5445 N.E. Dawson Creek Dr., Hillsboro, OR 97124; (503) 615-1100.

Getting the most out of a Texas Instruments (TI) TMS320C32 digital signal processor (DSP) does not require black magic, but it does take careful design with attention to details. The C32, which has been available for years, is still a very versatile floating-point processor able to operate at 30 MIPS/60 MFLOPs while requiring a minimum of board space and carrying a relatively low price tag. These attributes make it well-suited for use in modems, industrial controls, and similar computation-intensive applications that involve high-resolution or high-sampling rates. For designers

of these systems, a floating-point processor means there are no round-off errors, hence algorithm programming is much easier.

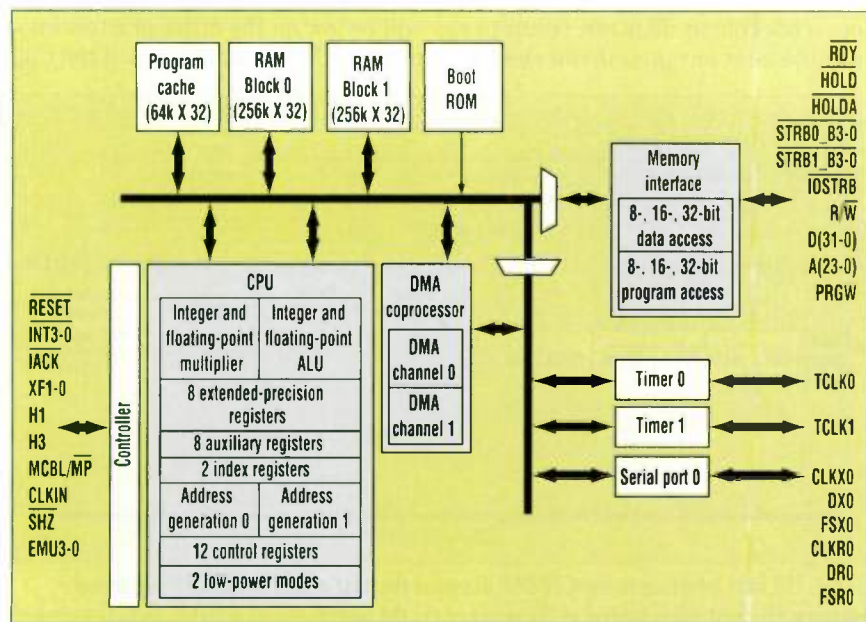
The TMS320C32 is available in 40-, 50-, and 60-MHz versions. The internal memory comes in two banks of 256 words, and there also is an on-board cache of 64 words (Fig. 1). Memory, Flash, I/O devices, host interfaces, and other peripherals are attached to the part's one main bus. In addition to the main bus, peripherals also can be interfaced to the C32 serial port, which peaks at 15 Mbits/s. Two timer/counters are available for inter-

facing to external interrupts and/or internal timers. For external memory, the C32 has three memory spaces (each with programmable wait states), flexible boot loading, and two channels of DMA.

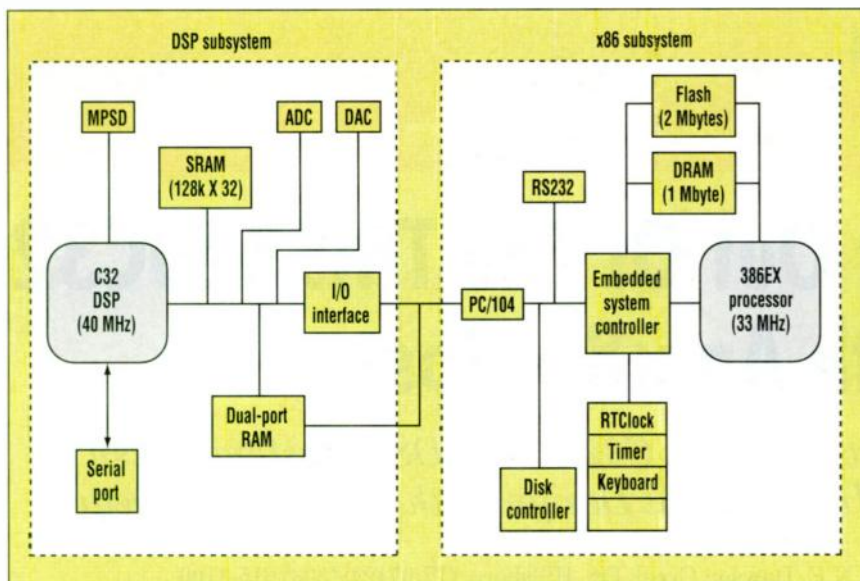
C32 With x86

Some C32s are used in standalone applications, but many are used in computer peripherals that operate under the control of a host CPU, such as an x86 microprocessor. For applications that require many higher end services, such as a graphical-user interface (GUI) or data-storage facilities as well as signal processing, a C32 and an x86 offer the best performance for the price. By partitioning tasks between the C32 and its host x86, designers can optimize performance by assigning each processor the tasks for which it is best suited—the DSP can perform computation-intensive algorithms such as FFTs, filtering, matrix computation, and vector operations, while the x86 handles the physical display, data logging, storage, and the overall system control and configuration functions.

A significant benefit to this arrangement is that the DSP can run in real-time with its support activities handled by the host. An example of an application in which this is important is a machine-vision system performing product inspection. In this instance, the DSP performs I/O pre-processing in real time while the host compares the results against preset templates to



1. This block diagram shows the C32 digital signal processor's internal architecture, including the two blocks of 256-by-32 internal memory.



2. The system-level architecture for a C32/x86-based system shows how the design is partitioned such that each processor performs the tasks for which it is best suited. The two processors communicate via an I/O mapped or dual-port-memory mapped interface.

determine whether or not a given product meets specifications.

Another benefit of using an x86 host is that both hardware and software for most applications are readily available. Designers can significantly reduce system development time and cost by taking advantage of this wealth of resources.

Designing a host-based C32 system requires careful analysis of the system's requirements. For example, what kind of human interface will be required? Will there be a full-blown Windows NT system with a fancy GUI or a simple LCD display? Equally important is the interface between the host CPU and the C32.

Let's examine the architecture for a system using a C32 DSP and x86 microprocessor (Fig. 2). The x86 system shown is an embedded Intel386 EX with its associated Flash, DRAM, disk controller, and peripheral interface. Also shown is the data path from the x86 to the DSP's I/O interface. This path is the popular ISA bus or the PC/104 bus.

Host Bus Selection

When the host is the CPU in a personal computer and the C32 is a plug-in peripheral, the interface will be dictated by the available bus expansion slot—typically either an ISAbus or PCIBus slot. Although virtually all new x86 computers are equipped with

a PCIBus to accommodate internal peripherals, there are a huge number of legacy computers built around the ISA bus that are still in use. As a result, many peripheral makers still provide ISAbus expansion cards.

Designers can easily implement ISA in small systems by using PC/104 components. The PC/104 is a system bus which is electrically equivalent to ISA, but has a small form factor more suited to embedded designs. PC/104 cards stack on top of one another rather than plugging into a backplane. This can result in a notable cost savings if the system

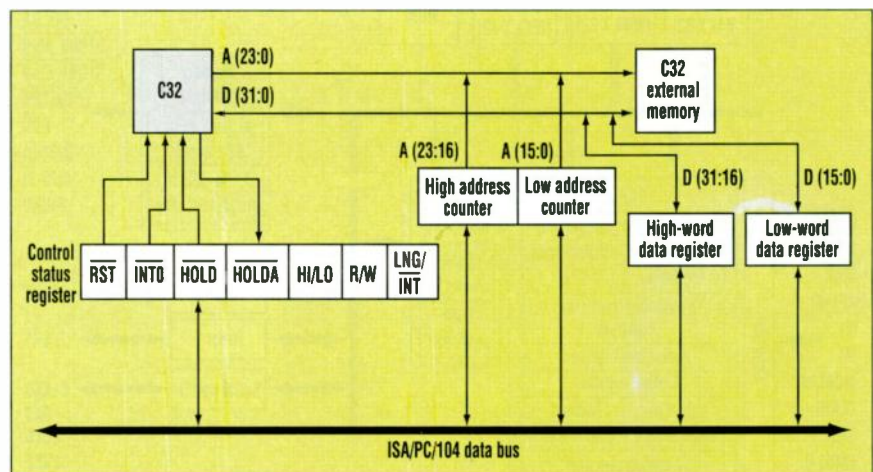
uses only a few cards.

A good example of a host-based C32 system using a PC/104 interface consists of a RadiSys EPC-30 single board computer (SBC) and a SPIRIT-32 PC/104 DSP board. The EPC-30 SBC is built around the Intel386 EX processor that, even in this age of 266-MHz Pentium processors, can easily handle the majority of DSP command and control applications. The SPIRIT-32 PC/104 DSP board is plugged into the EPC-30's PC/104 expansion connector. Such a configuration offers all of the benefits of a PC and a DSP in a small, low-cost package.

Host Interface

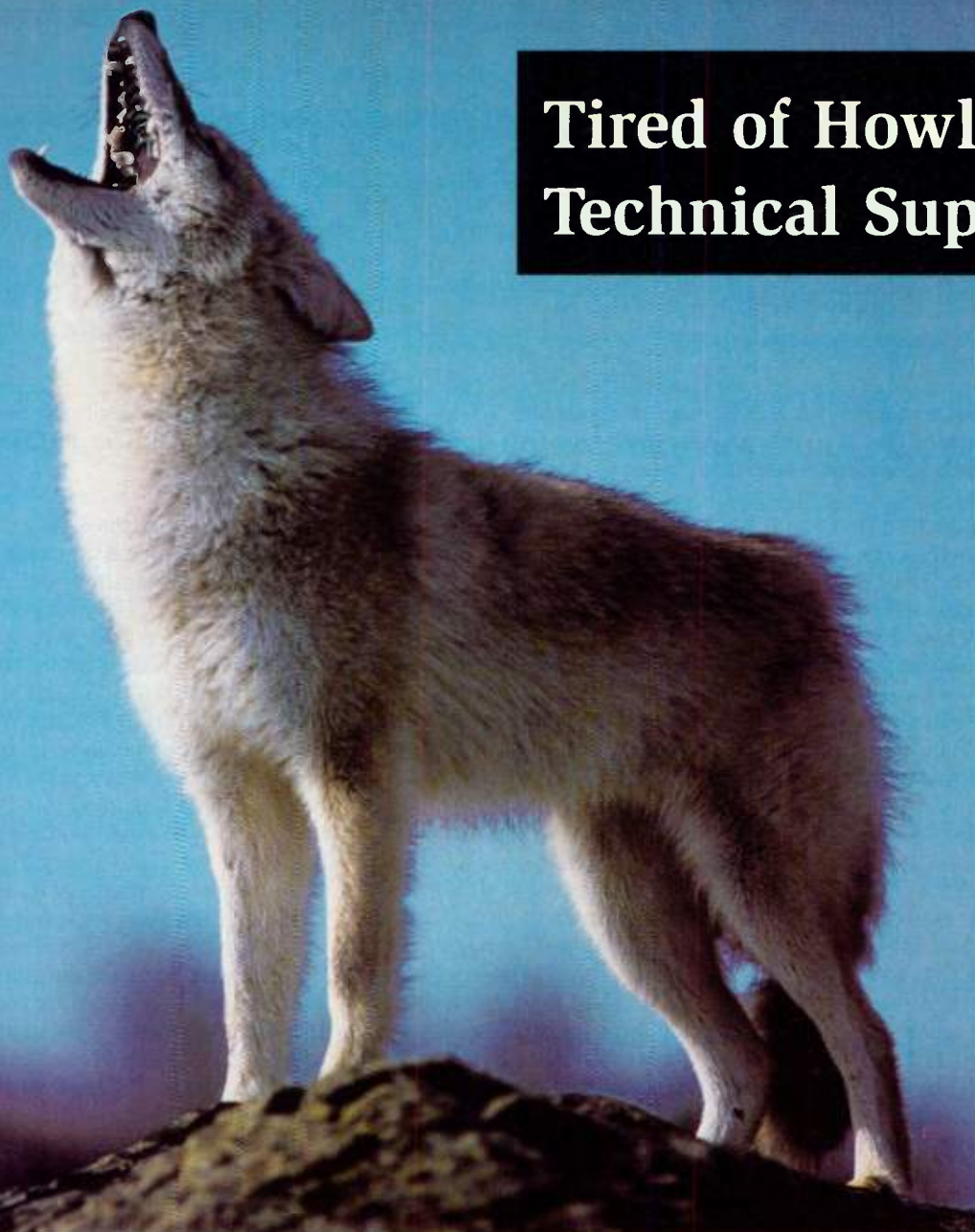
A critical element in the DSP-to-host interface is a datapath with enough bandwidth to support the required throughput. Designers have to make provisions for either processor to initiate communications with the other while providing the host CPU with some control over the C32's activities (reset and interrupt control, for example). Also, designers will have to match data widths if the datapath between the host CPU and C32 is other than 32 bits wide.

Datapath bandwidth requirements vary considerably, depending on the application involved. If the host CPU's communications with the C32 are limited to issuing control commands, bandwidth requirements will be low on the order of a few kilobytes/s. On the other hand, if the C32



3. This ISA host interface to the C32 DSP provides the host access to the C32's external memory. The host gains control of the memory via the control status register. Data is accessed with the high-word and low-word data registers. The address counters provide incrementing addresses for block transfers.

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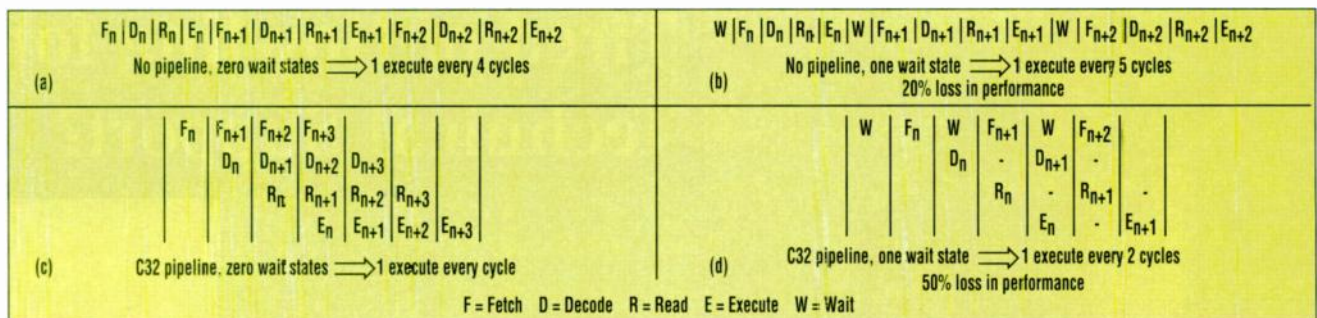
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4. A CPU without a pipeline incurs a 20% loss in performance when going from zero-wait-state program memory (a) to one-wait-state memory (b). The pipelined architecture of the C32 provides program execution at the rate of one instruction every clock cycle (c). However, the C32 is impacted even more severely when using one-wait-state program memory, incurring a 50% loss in performance (d).

processes video/image data that the host CPU needs to access, the bandwidth requirements can be quite high, in the range of tens of megabytes/s. A VME or PCibus is the best choice for these applications.

The C32 provides two signals, **HOLD** and **HOLDA**, to allow a host CPU to assume control of its external memory bus. To gain control of the C32's memory, the host CPU asserts the **HOLD** signal. The C32 then completes its current task, then asserts the **HOLDA** (hold acknowledged) signal. Upon receipt of the **HOLDA** signal from the C32, the host CPU begins accessing the C32's external memory. While **HOLDA** is asserted, the C32 tristates its address and data buses and memory control signals, allowing the host CPU to drive these signals and access the memory. The C32 will suspend any external accesses while **HOLD** is asserted, but will continue to run internally until the external bus is needed. The hold cycle completes when the host deasserts the **HOLD** signal.

One implementation of an ISA host interface has a control register, a pair of address counters, and a pair of data registers (Fig. 3). The host initiates sending or receiving of the data from the C32 external memory by writing to the control/status register and setting a bit that will put the C32 on Hold.

Once the C32 is put on Hold, as verified by reading the status of the **HOLDA** bit, the host writes the target address into the two 16-bit address counters, sets the direction of the transfer by writing to the read/write bit, and sends data to the data register. The address counters increment every other ISA transfer

for a 32-bit access to the C32 and every transfer for a 16-bit access.

Need For External Memory

Because the C32 has only 2 kbytes of internal memory, organized as two banks of 256-by-32-bit words, virtually all host-based and standalone applications will require the use of an external memory. Designers have a number of memory alternatives to choose from, each with its own advantages and disadvantages. As is often the case in electronic design, the choice comes down to a trade-off between cost and performance. However, because the C32 has a pipelined architecture and can perform an instruction fetch every 33 ns, it's even more necessary that the external memory be able to keep pace.

To demonstrate the necessity for fast program memory, let's examine how a program instruction is executed. To execute an instruction on any processor, four steps must take place. First, the program needs to be fetched from memory. Next, it's necessary to decode the instruction. Third, any operands required for the instruction need to be read. Finally, the instruction needs to be executed.

On processors without an instruction pipeline, each of these steps happens sequentially. The C32 has separate units dedicated to each of the fetch, read, decode, and execute operations. This pipelined architecture allows it to overlap these actions for several instructions, the result being that an instruction can complete execution every cycle.

Now, let's look at what happens when the program is stored in external memory, and look at the impact of inserting wait states for the external

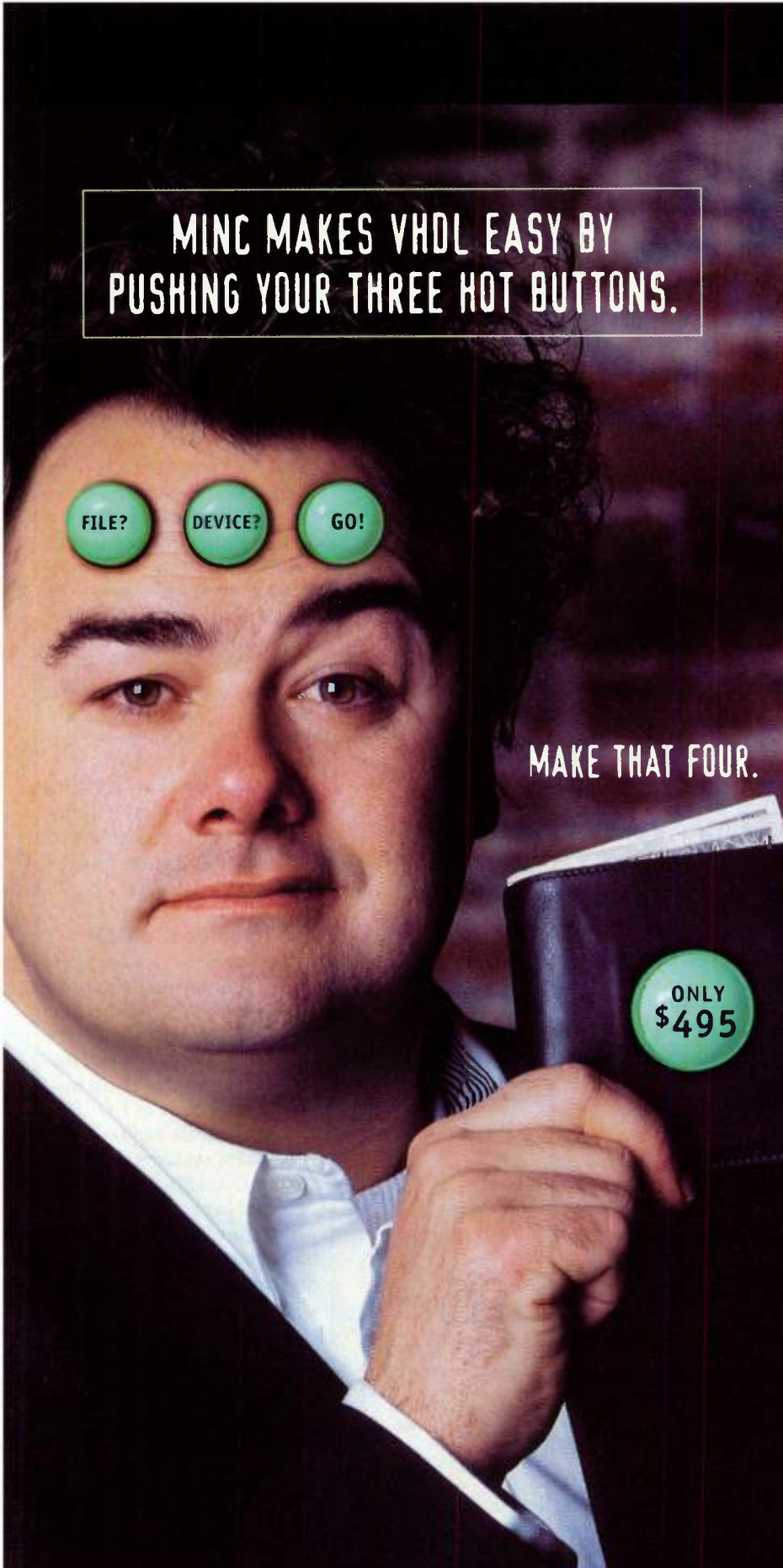
memory access. In the case of the non-pipelined processor, a best-case operation will complete an instruction every 4 cycles (Fig. 4a). If a wait state is inserted for the program fetch from external memory, then an instruction will complete every 5 cycles, a 20% loss in performance (Fig. 4b). With the C32's instruction pipeline, an instruction completes every cycle (Fig. 4c). By inserting a wait state into the program fetch, the pipeline stalls and an instruction completes every 2 cycles, a 50% loss in performance (Fig. 4d).

If any of the read or execute phases require access to external memory, then the performance is further degraded when wait states are required. Due to the increased performance loss when slow memory is used, it's more critical with the C32 than with other processors that zero-wait-state memory be used.

Selection Of External Memory

In most cases, designers will find that SRAM is the best choice for external program memory. Using SRAM will provide a zero-wait-state memory without any external logic. For a 60-MHz C32, an SRAM with 15-ns access time will provide such a solution.

In general, DRAM is less expensive than SRAM and also has a greater storage capacity. Also, DRAM manufacturers have invested considerable effort towards improving its performance. Today, DRAM comes in a variety of flavors, ranging from basic page-mode DRAM to more exotic devices, such as extended data output (EDO) DRAM, synchronous DRAM (SDRAM), Rambus DRAM (RDRAM) and double-data-rate (DDR) DRAM. The fastest of these



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can transfer data to the C32 with no wait states.

The performance improvements available from advanced DRAM devices result from their I/O architectures, which increase the maximum rate at which data can flow into the memory bus—important when large blocks of data have to be transferred. But if the application instead calls for frequent but short data transfers, which is the case with program fetches, the ability to get the first bits of data out of the memory (latency) is much more important. The latency of any DRAM, regardless of its I/O architecture, is typically in the 60-ns range. Of perhaps greater importance, these devices require external logic that adds to the bill-of-materials cost and occupies board real estate. These are critical concerns in the kind of applications for which the C32 is intended. Because of these factors, designers usually find that 15-ns SRAM is the only practical choice.

Although SRAM generally costs more per bit than DRAM, the memory needs of a C32 are usually modest. The actual size of the external memory depends on the application's requirements, but it's typically in the 32- to 64-kbyte range. As a result, the cost differential between SRAM and advanced-I/O DRAM is usually negligible. Designers developing applications that require large blocks of data to be transferred between the memory and the C32 may find it practical to combine SRAM with DRAM to minimize cost and real-estate requirements.

Some designers may opt for a small amount of dual-port memory in addition to the DRAM and SRAM. Both the DSP and x86 have access to the memory where real-time parameters and data can be sent back and forth without halting the DSP or the x86.

DSP Memory Interface Design

Although the C32 has limited internal memory, it does

provide three built-in chip selects that enable external memory and other peripherals to be partitioned with a minimum of external decode logic. Two of the three chip selects—Strobe 0 space and Strobe 1 space—can perform zero-wait-state reads in one clock cycle. To capitalize on the speed of the SRAM, it should be connected to one of these high-speed strobe spaces. The other high-speed strobe space can be used to support a Flash memory or perhaps firmware in ROM. The third chip select—I/O Strobe space—requires two clock cycles for data transactions and can be used to support slower peripherals.

The wait states of all three of the chip selects are programmable, which reduces the need for external logic to generate wait states. In this manner, memories and peripherals with wait state requirements can be placed in separate programmed strobe spaces with wait states programmed accordingly for each device.

External memory is accessed by the C32 through a 32-bit parallel bus. Because the C32 is a 32-bit machine, it can fetch 32 bits of data from the memory each time it executes a memory access. Of course, not all peripherals are 32-bit devices. SRAM, for example, is commonly organized as a byte-wide device. This is not a problem, however, because four of these 1-byte-wide devices can be connected across the C32's 32-bit bus.

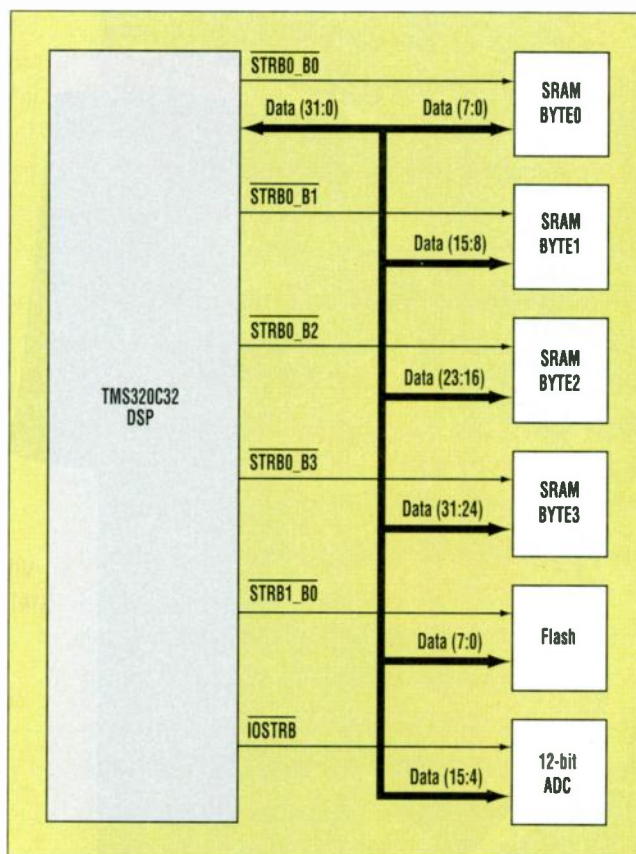
In a typical external memory bus configuration, Strobe 0 space is connected to zero wait state SRAM (Fig. 5). The SRAM consists of four 1-byte-wide devices to span the 32-bit data bus. Each of the Strobe space 0 byte enables (STRB0_B0,1,2, and 3) is connected to the corresponding byte of the 32-bit data word, acting as a chip enable. A byte-wide Flash EEPROM is connected to Strobe space 1, utilizing only the byte enable for the low byte, STRB1_B0. Finally, a 12-bit a-d converter (ADC) is connected to the

I/O Strobe space. Note that the data from the ADC is aligned with D[15:4]. This allows the C32 to recognize the data as a 16-bit short integer data type.

I/O Interface To DSP

DSPs starve without optimal I/O function. The host bus is one I/O for DSP, but in most applications, the DSP's serial port or a peripheral extending from the main bus also are sources of I/O. The I/O peripherals can be data-acquisition systems that capture and condition data from external events. In these applications, the peripheral might contain an analog-to-digital converter (ADC) to digitize analog data. The digital data might then be analyzed by the C32, which could be configured to act as an FIR filter or to perform an FFT on the acquired data.

When connecting parallel ADCs to the external memory bus as peripherals, it should be done so that the C32 need do as little preprocessing as possible before the data is available for use.



5. This typical configuration illustrates the flexibility of the external memory bus. Strobe 0 space is connected to 4-byte-wide SRAMs, each with its own byte enable, STRB0_BX, providing a 32-bit memory. Strobe 1 space is connected to a 1-byte-wide Flash EEPROM. The I/O Strobe space is used to access an a-d converter.

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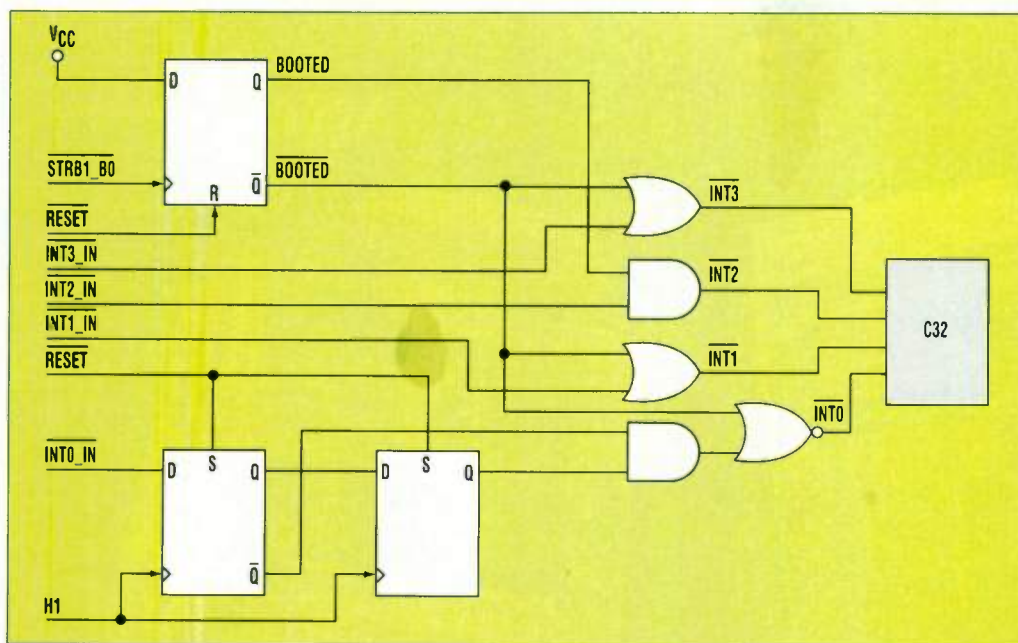
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6. Coming out of reset, this circuit will drive the C32 interrupt lines with the code indicating boot load from Strobe 1 space. Once the bootloading begins, the interrupt lines return to their normal mode of operation. INT0 is conditioned for level triggering, and INT1-INT3 can be used for edge-triggered operation.

These ADCs are available with a wide range of resolutions. The converter's output will be in an integer format, either two's complement or unsigned. The C32 recognizes integers as either 16-bit (short) or 32-bit (single-precision) data types. If the ADC outputs 16 bits or less, designers can eliminate the need for bit shifting in software by aligning the converter's most significant output bit (MSB) with data bit 15 on the C32's external memory bus. This enables the C32 to access it as a single-precision integer.

Boot Loader And Startup

Once the memory has been partitioned and the locations that will hold the program instructions allocated, the next step is getting the program into the C32. The C32 has two boot loading modes: microprocessor mode and microcomputer boot-loader mode, which are chosen through the MCBL/MP mode-select pin.

The C32's microprocessor boot-loading mode requires the program code to be present and available to it when it comes out of a reset. Designers can accomplish this with an EEPROM or EPROM preloaded with the application program. However, these kinds of devices are relatively slow, and not well-suited for running an application. Even if speed were not an is-

sue, by their very nature they are not operationally flexible. If the application program needed to be altered, an EPROM would have to be replaced because its contents can't be altered while it is installed in its host.

An even better approach is to load the application into the C32's main memory while it's in reset so that the program is immediately available from high-speed memory when the C32 comes out of reset. However, this approach requires an external processor to load the program into the C32's memory. For this reason, the C32's microprocessor mode is used primarily in embedded applications for which a host processor, such as an x86 microprocessor, is present.

The C32's microcomputer's boot-loading mode accepts code from its external memory interface or its serial port and loads the program into its main memory itself. In this mode, the C32's memory map changes to incorporate an internal ROM that runs the boot loader code. To indicate to the C32 where the application is to be found, its four external interrupt pins must be driven with a specific code. This imposes another mode of functionality on the interrupt pins, which dictates the need for external logic to support both modes.

In their normal mode of operation,

the external interrupts can interrupt the C32's internal CPU or one of two DMA controllers. The choice of CPU or DMA controller interrupt can significantly affect the C32's performance.

When a CPU interrupt is serviced, a five-cycle latency occurs between the execution of the last program instruction and the first instruction of the interrupt service routine (ISR) while the C32 performs the necessary operations to save the current location in program execution and branch to the ISR. Also within the ISR, the C32 must perform a context save on any registers that will be altered dur-

ing the ISR. This can be a significant amount of overhead in a real-time application. Also, after the interrupt has been serviced, a similar amount of overhead is incurred while the C32 returns to its normal program flow.

Often the overhead associated with a CPU interrupt is justified, but sometimes the task requesting the interrupt is very simple. For example, the task of copying the output of an ADC into memory is simple and straightforward. In this situation, a DMA interrupt is a much more efficient choice. Because the two DMA controllers are treated by the CPU as peripherals, they can operate in parallel virtually without overhead. As a result, they can service an interrupt request without interfering with the CPU's operations.

The C32's CPU interrupts can be either level triggered or edge triggered. A level-triggered interrupt is recognized (internal interrupt flag set) when the external interrupt input is held low for one or two clock cycles. If the interrupt input is held low for three or more clock cycles, multiple interrupts will be generated. If only one interrupt is desired, designers will have to provide external conditioning logic to ensure that the external interrupt input is held low for just one clock cycle. An edge-triggered request de-

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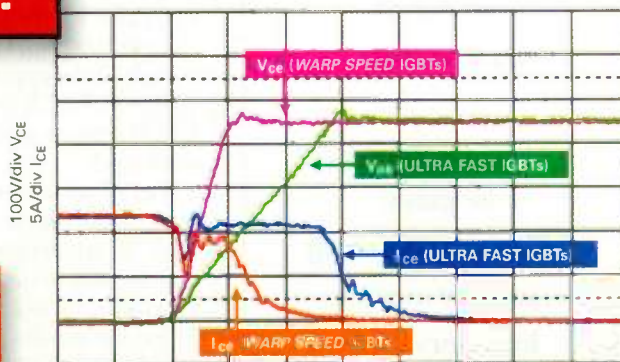


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depends not on the level present on the interrupt input pin, but rather on a high-to-low logic state transition to make its presence known. Once the transition is seen, an interrupt flag is set internally and the C32 may begin servicing the request.

Although the C32's CPU can be interrupted with either edge or level triggering, the DMA controller can only be interrupted with level triggering. Because of this, designers must ensure that the interrupt request exists only long enough for the intended DMA transfer or transfers to be performed. If the interrupt remains asserted beyond that point, more DMA activity will occur than intended and the system will not behave as planned.

Depending on what the C32 is doing at the time and whether or not there are other interrupt requests queued, an interrupt request may not be serviced for several clock cycles. Some external devices need a handshake signal from the C32 notifying it that its interrupt request is actually being serviced. To accommodate these peripherals, the C32 is equipped with an interrupt acknowledge output pin, $\overline{\text{IACK}}$, that normally is high. If the application software executes an $\overline{\text{IACK}}$ instruction, the C32's $\overline{\text{IACK}}$ output pin will go low for one clock cycle.

Let's look at an example of some external logic that could be used to drive the C32 interrupts (*Fig. 6*). A D flip-flop is used to determine how the interrupt pins should be interpreted. The reset condition will set $\text{BOOTED} = 0$, driving $\text{INT}[3:0]$ with the code 1011, indicating that the C32 should boot load from Strobe space 1. When Strobe space 1 is accessed, STRB1_BO will toggle, clocking the flip-flop and causing BOOTED to go high. At this point the $\text{INT}[3:0]$ interrupts will follow the external sources $\text{INT}[3:0]_{\text{IN}}$. In this example, $\text{INT}[3:1]$ are treated as edge triggered interrupts. $\text{INT}[0]$ is conditioned to provide a 1-clock-cycle-wide pulse every time it goes low, so it can be used as either a level triggered interrupt or as a DMA interrupt.

System Integration With C32

Even though the C32's internal memory is too small to hold an applica-

tion, designers will find it very useful for two important reasons. First, writes to the internal memory take only one clock cycle, while writes to the external memory take two. There is an additional one-clock-cycle penalty in the external write timing if the write immediately precedes a read operation. Therefore, the C32's internal memory makes a fairly good variable memory that designers writing in C can use as the site of the C environment's stack. By so doing, designers can significantly reduce the time required to write to the stack.

The C32's architecture is such that two reads from the internal memory can be executed in a single clock cycle. This makes it well suited as a variable memory for instructions that require two operands such as a multiply. The two values that are to be multiplied can be resident in the C32's internal memory, eliminating the need to waste a clock cycle bringing the values in from external memory. Using the C32 internal memory for variable storage also prevents the pipeline from stalling when both program and data access are required during the same clock cycle.

Designing an x86 and DSP-based system is not difficult. The difficulty lies in developing the debug diagnostics, manufacturing tests, and application run-time library to facilitate data transfer between the x86 and DSP. RadiSys offers reference designs for x86 and DSP with the associated software. As operating systems and GUIs become more complex, and speeds of graphics boards and PC peripherals increase, the host CPU will always be burdened and will not be able to do real-time processing. A DSP coupled with a host CPU makes a perfect combination for achieving high performance at low cost.

Chris Stolarik is a hardware engineer with the DSP division of RadiSys. He received a BSEE from Carnegie-Mellon University, Pittsburgh, Pa., and a MSEE from Johns Hopkins University, Baltimore, Md.

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ANALOG OUTLOOK

■ Exploring the world of analog, mixed-signal and power developments

1997: The Year Of The Rail-To-Rail I/O IC Op Amp

Low-Power, Low-Voltage Devices In Tiny Packages Sporting Rail-To-Rail Inputs And Outputs Dominate The Scene.

Frank Goodenough

Who would have believed that 1997 could be called "The Year of the Op Amp?" They have been moving toward ubiquity since the days of George Philbrick's plug-in, vacuum-tube-based K2. Philbrick's modular op amps, amongst others, intensified the need for the company's 709 and 741 IC op amps. Followed by the quad LM324, these innovators truly unleashed op amps on the world. While the 741 and 324 are still widely used, even for new designs, they are not the universal devices they first appeared to be.

While the microprocessor has grown from 4 to 64 bits, IC op amps have totally obliterated their modular and vacuum-tube ancestors. Like the modules before them, IC op amps have proliferated and become unique specialty items with few second sources. It's hard to believe, but when Intel announced its first 4-bit microprocessor, most op amps were still modules, and Philbrick was still selling an occasional K2. Today, a designer uses one model IC op amp for high speed or bandwidth, another for high-input impedance, and still another for low drift. The universal op amp is only now arriving in the form of some micropower devices with rail-to-rail I/O.

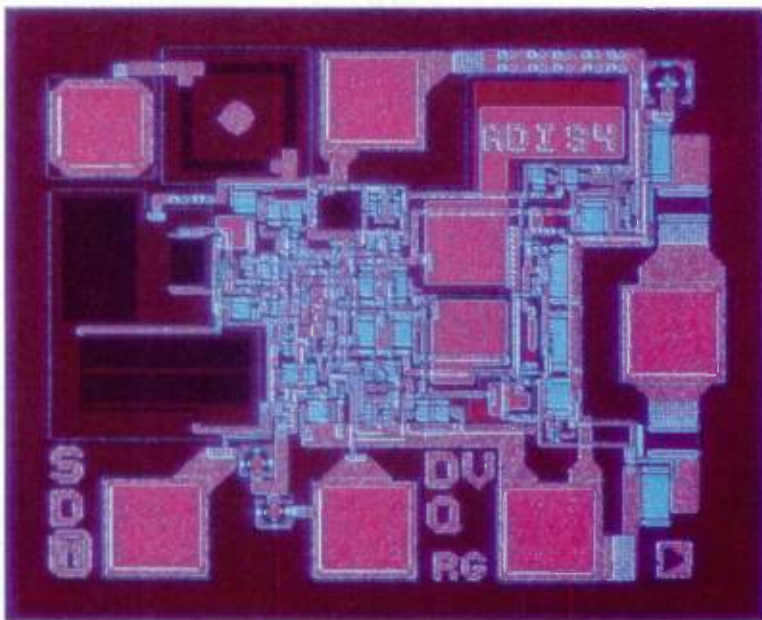
The demand for op amps that are compatible with digital systems has driven some of the proliferation and specialization in the form of devices that can run off a single 5-V rail, the so-called "single-

**SPECIAL
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supply" op amp. However, even these devices have followed the path of their split-supply kin. None are universal. One family is designed for high-speed applications in which they are often handling digital signals (driving output lines to other ICs or peripherals). Other devices provide low drift. Still others provide high-input impedances.

The last few years have seen the following new challenges presented by analog-IC and mixed-signal-system designers:

- Operation between a negative supply rail and a single positive rail.
- Operation from a single positive supply rail at voltages below 5 V, and, if possible, below 1 V, without significant degradation of dc or ac common-mode rejection ratio (CMRR), offset voltage, or other specifications. Ideally, the op amp also should operate from split supply rails of ± 15 V or even greater.
- The input common-mode voltage (CMV) can move at least 100 mV below the negative rail, and at least 25 mV above the positive rail without significant degradation of dc or ac common-mode rejection ratio (CMRR), offset voltage, or rail-to-rail input; and without the output inverting.
- The output voltage can swing beyond either supply rail, or at least swing within 100 mV of both rails (rail-to-rail output).
- Micropower operation. That is, provide good dc and ac specifications while operating at currents be-



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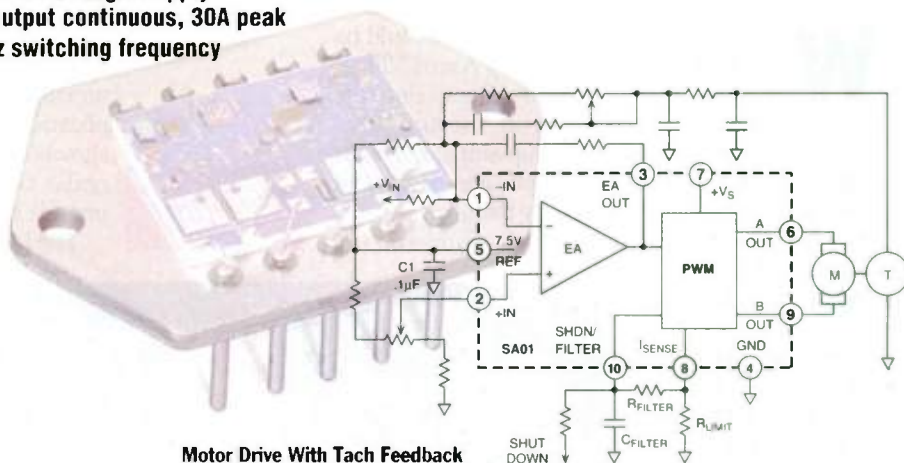
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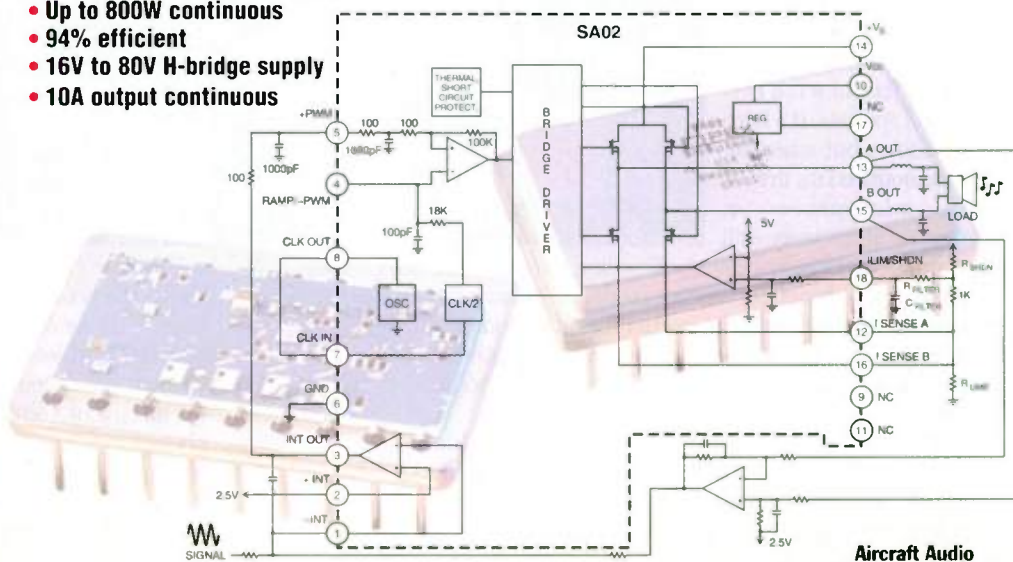


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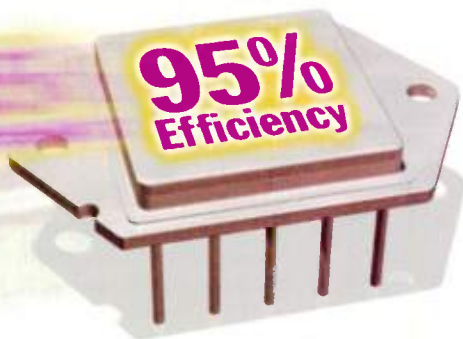
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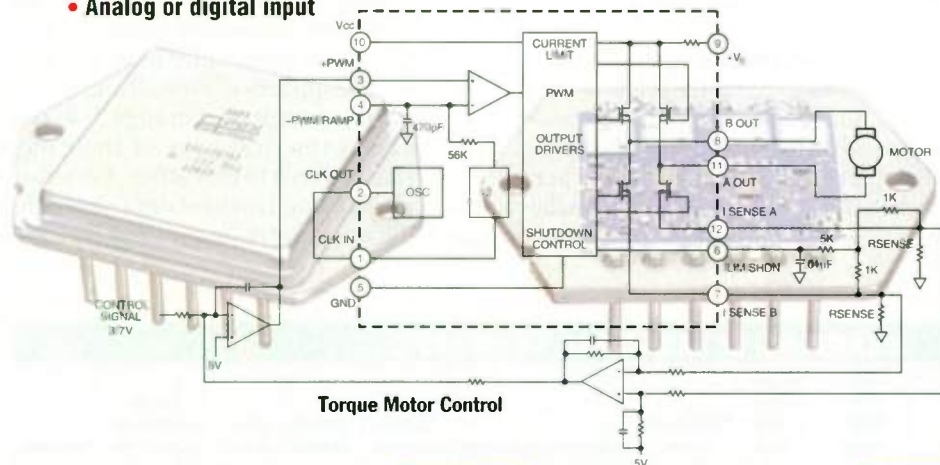


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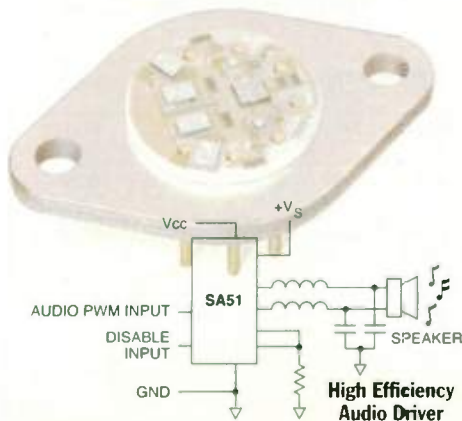
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- 97% efficient
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- 5A output continuous

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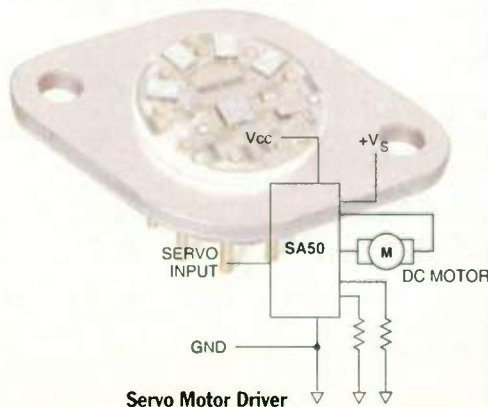
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- 97% efficient
- Up to 80V H-bridge supply
- 5A output continuous
- Internal PWM generation

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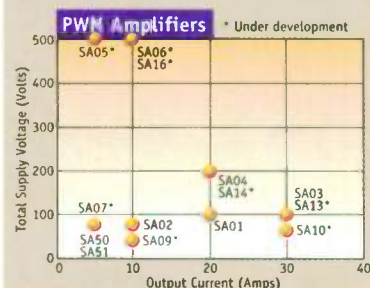


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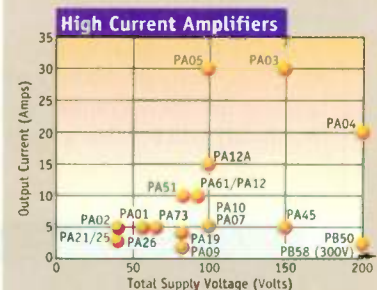
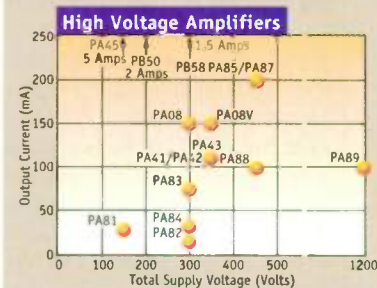


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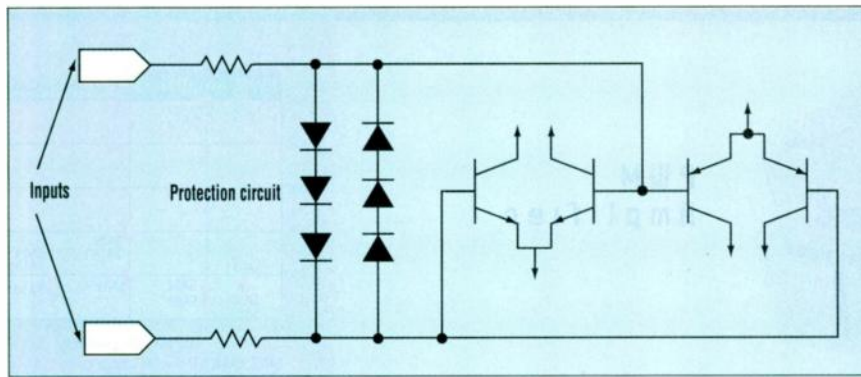
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1. Most rail-to-rail op amps sport input stages composed of two long-tailed pairs, one using npn and one using pnp transistors. The resistor and diodes form the input-protection circuit.

low 2 mA (an arbitrarily high value of current—0.1 μ A might be closer). System designers would take zero quiescent current if offered such a device.

- The die must be small enough to fit in a tiny package such as the 5-lead SOT-23, the TSSOP-8, or the SO-8.

- System designers also would like bias currents on the order of a few picoamps, offset voltages that stay below 1 μ V, and stable full-power 3-dB bandwidths beyond 10 MHz.

In the past, analog-IC designers have come through with a variety of op amps to fill this upcoming niche which eventually will become a large canyon.

However, for some applications, split supplies will never go away. Instead, like some systems today, they will operate from ± 5 V. Some analog-system designers aiming at noisy industrial applications will still demand a pair of split ± 15 -V rails and state-of-the-art IC op amps to ride on them.

Taking Requests

Regarding the aforementioned list, many single-supply op amps are available for various applications. Most ground-sensing op amps permit the CMV to drop at least a few millivolts below the negative rail, but their output

cannot come close to the positive rail.

Because microprocessor and digital-system supply rails have dropped well below 5 V, system designers need single-supply op amps that can run effectively off the same low-voltage rails. When operating with low supply voltages, every millivolt of available headroom becomes vital to maintaining output-voltage swing. Allowing their inputs to swing beyond the power rails maximizes the op amps' input-voltage swing. In many systems, the input-voltage swing is unknown (or is an unexpected transient) at the time of design. Voltage and current noise floor also must be at a minimum to maximize headroom.

Early Op Amps

If their CMVs exceeded the supply rails, their output voltage became inverted. If positive, the output went negative, and vice versa. Today, many of these op amps have been fixed, and very few IC op amps announced during the last 10 years suffer from the drawback. Suppliers of virtually all rail-to-rail IC op amps print in large, bold type across the first page of their data sheets words to that effect. For example, Analog Devices' data sheets for this species of op amp say, "DOES NOT

A SAMPLING OF RAIL-TO-RAIL I/O OP AMPS

Company	Part number	Input CMV range		CMRR over CMV range	Single-supply voltage range	Quiescent current	Output-voltage range		Output current	Offset voltage	Bias current	Stable unity gain bandwidth	Package
		Conditions	Voltage				Conditions	Output					
Analog Devices	AD8532	$V_s = +3$ V, $R_L = 2$ k Ω to ground	0 V to 3 V	34 dB	2.7 V to 6 V	1 mA	$I_L = 10$ mA	100 mV to 2.85 V	250 mA	25 mV	50 pA	3 MHz	TSSOP-8
	OP296	$V_s = +3$ V, $I_L = 100$ μ A to ground	0 V to 3 V	60 dB	3 V to 12 V	60 μ A	$I_L = 100$ μ A	70 mV to 2.85 V	4 mA	0.3 mV	35 nA	0.35 MHz	TSSOP-8
Maxim	MAX4163	$V_s = +3$ V	-0.25 V to +3.25 V	70 dB	2.7 V to 10 V	40 μ A	$R_L = 10$ k Ω	30 mV to 2.82 V	15 mA	4 mV	100 pA	0.2 MHz	μ MAX
	MAX4123	$V_s = 2.7$ V	-0.25 V to +2.95 V	78 dB	2.7 V to 6.5 V	750 μ A	$R_L = 250$ Ω , $V_s = 2.7$ V	330 mV to 2.47 V	50 mA	0.2 mV	150 nA	2 MHz	μ MAX
Motorola	MC33502	NA	0 to V_s	74 dB	1 V to 7 V	1.2 mA	$V_s = 1$ V, $R_L = 600$ Ω	16 mV to 95 mV	13 mA	0.5 mV	40 fA	4 MHz	SO-8
	MC33202	NA	0 to V_s	60 dB	2 V to 7 V	0.9 mA	$V_s = 5$ V, $R_L = 600$ Ω	250 mV to 4.85 V	50 mA	8 mV	200 nA	2 MHz	SO-8
SGS-Thomson	TS3V912	NA	0 to V_s	NA	2.7 V to 14 V	NA	$V_s = 3$ V, $R_L = 600$ Ω	1.9 V	40 mA	2 mV	300 pA	0.8 MHz	SO-8
Linear Technology	LTC1152	$V_s = 5$ V	-300 mV to 5.3 V	115 dB	2.7 V to 14 V	3 mA	$R_L = 1$ k Ω , $V_s = 5$ V	0 V to 4 V	12 mA	10 μ V	100 pA	1 MHz	SO-8
	LTC1366	$V_s = 3$ V	0 to V_s	76 dB	1.8 V to 15 V	375 μ A	$I_{\text{sink}} = 2.5$ mA, $V_s = 3$ V	0 V to 2.82 V	30 mA	NA	45 nA	0.3 MHz	SO-8

CMRR = common-mode rejection ratio; CMV = common-mode voltage; NA = not available.

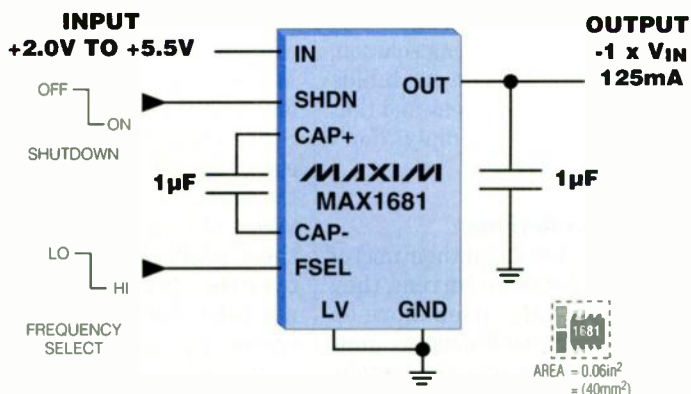
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PHASE INVERT."

There's a classic story about this phenomena. Since the story is true, the names have been changed to protect the guilty.

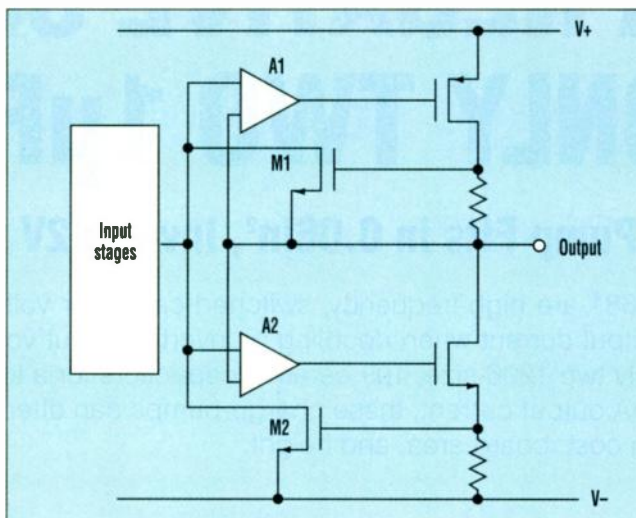
It seems that Joe, an application engineer at a well-known analog-IC company (then, a start-up), had a telephone call from Tom, a system engineer at the Smokey Diesel Locomotive Works. Tom reiterated the inversion problem to Joe who agreed "... that the problem exists. ..."

But, says Tom, "yours doesn't do it." "Yeah," says Joe, "we fixed it." "Well," says Tom "we fixed it in the software. Now when we use your op amp, every time the CMV exceeds the supply rail, the locomotive goes into reverse." Joe's quick-thinking solution, based on knowing that no one builds millions of locomotives a year and that software is sacred, was simply "don't use our op amps."

Deintegration Arrives

As digital systems and their microprocessors cry for more current, they are finding they also need more op amps. The need for additional op amps is usually discovered after the system, its pc boards, and its final physical rendition are fully determined. "No way," say the system's marketers. They will not give the system designer one more cubic millimeter of system volume or a few additional milliwatts of power for the desperately needed op amps. But again, the analog-IC-design cavalry has arrived in the nick of time with tiny micropower op amps. These op amps sport a suite of specifications thought unobtainable in any op amp just a few years ago. And more arrive every day in ever-smaller surface-mount packages.

Today, op amps ride at the forefront of this deintegration phenomena. While more designers put millions of transistors on a chip, a few are doing just the opposite. They squeeze analog "glue" func-



2. Like most CMOS op amp rail-to-rail output stages, this one uses a pair of complementary MOSFETs in a common-source connection. A typical op amp would use them in a common-drain (follower) mode.

tions such as op amps, references, low-drop-out regulators (LDOs), discrete MOSFET power switches, and even data converters into a plethora of tiny SOT-, SO-, and TSSOP-based packages. Digital functions, compatible with the latest sub-half-micron CMOS devices, also are being squeezed into these packages, which are sprinkled over the system wherever they are needed, including previously unusable spaces on pc boards.

Placing these analog and digital glue

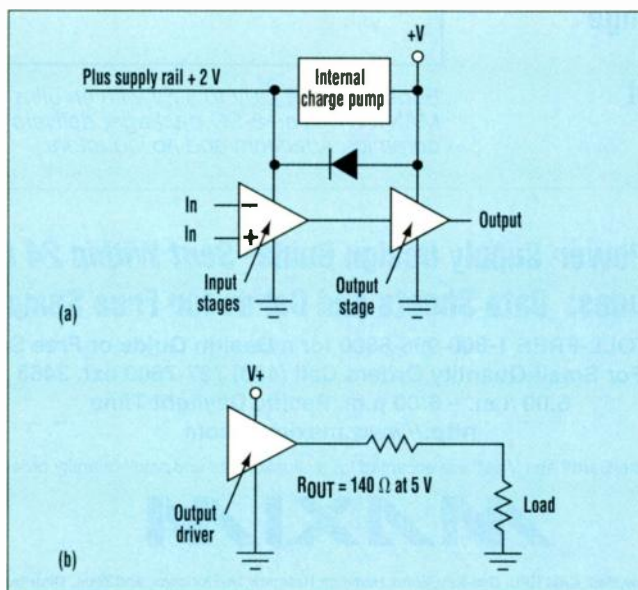
functions exactly where needed on a pc board eliminates inches-long, board-area-using, speed- and bandwidth-killing, crosstalk-generating signal lines. These long, sensitive, signal lines are required if the glue is buried somewhere in a mixed-signal ASIC, only a few millimeters away from the point of need. No place-and-route EDA software can handle those problems.

In addition, both analog and digital glue ICs of this genre can take advantage of more exotic processes that bring higher voltage ratings and/or higher speed to the glue than that offered by most mixed-signal ASICs trying to track Moore's Law. Moreover, in or-

der to be used anywhere on a pc board, these new op amps must need virtually zero power. Present system supplies are probably already or soon will be, running at peak-rated load or beyond it.

Virtually all IC op amps designated rail-to-rail by their manufacturers can handle input CMVs well beyond their positive and negative rails. However, very few applications actually sport signal voltages that go beyond the rails. Therefore, their input CMV range is often specified as the supply rails. In addition, outputs will not reverse if the CMV goes a volt or so beyond the rails.

But where do system designers turn if they know their input voltage may swing well beyond normal supply rails? One approach is to try a high-voltage, power op amp such as those made by Apex and Burr-Brown. For example, Burr-Brown's 70-V OPA547 single-supply op amp swings at least 100 mV below the negative rail and to within 3 V of the positive rail (ELECTRONIC DESIGN, May, 1, p. 150). If an op amp can handle a 70-V (or higher) supply rail, there is little need to be able to swing the input or the output above it.



3. In addition to its internal charge pump which boosts the Linear Technology LT1152 op amp's input stages' supply voltage by 2 V (a), the output stage looks like a voltage source in series with a resistor that varies with the supply voltage (b). The output impedance runs about 140 Ω at 5 V.

Op Amp Year

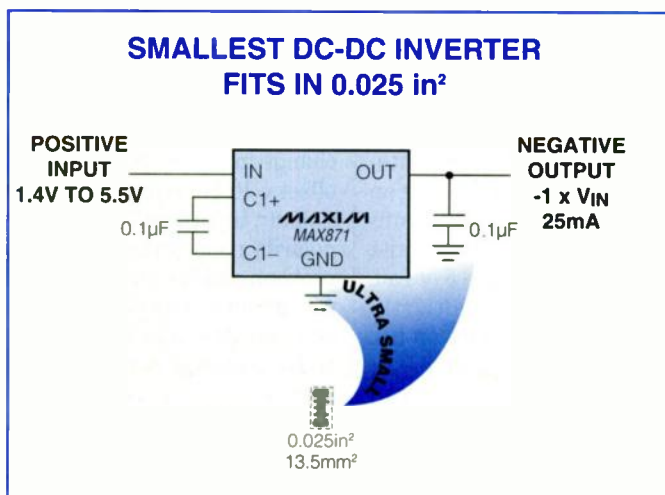
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Oscillator Frequency (kHz)	10	12	35	125	500
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ference (ISSCC) papers, one from Motorola, and the other from Texas Instruments (TI). Both soon became merchant-market products. The Motorola op amp is a dual device with a rail-to-rail I/O that operates off single supply rails as low as 1 V from which it typically draws just 1.2 mA. TI's CMOS op amps are the single TLC4501 and the dual TLC4502. These op amps use a digital auto-calibration (auto-zero) architecture which provides chopper-stabilized op amp performance without the attendant chopper noise. They meet some of the seven previously listed needs of the mixed-signal system designers.

Around the same time, Maxim Integrated Products introduced three op amps, the MAX4162/4163/4164 (single/dual/quad). Each of these uses just 35 μ A of current from a single 5-V rail, and their unity-gain-bandwidth still runs 200 kHz. The TI devices, on the other hand, sport a unity-gain bandwidth of 5 MHz. But, as always, speed costs power and the TI op amps need 1.5 mA from a 5-V rail. While not rail-to-rail input, the CMRR of the TI op amps runs on the order of 90 dB. The TI chips can be considered rail-to-rail output op amps since they can swing within 100 mV of either rail.

Maxim's op amps are true rail-to-rail I/O devices. Their input CMV, which does not invert, swings 250 mV beyond either rail while maintaining a CMRR of at least 70 dB (typically 100 dB).

All rail-to-rail op amp designers employ some sort of neat analog-circuit techniques to equip the op amps for carrying out two unique tasks: handling in-

put voltages beyond either rail, and swinging their output voltages close to both rails. To handle an input CMV to, or beyond, the supply rails, most rail-to-rail input op amps use a unique input stage built with some combination of p- and n-type transistors (MOS or bipolar). Usually p-type long-tailed pairs handle input signals close to the negative rail and n-type pairs handle signals close to the positive rail.

Most of these op amps suffer from severe nonlinearities in the region where the input signal moves between p- and n-type devices. At this point, the user may see a drop in CMRR and/or a significant change in offset voltage. For example, offset voltage polarity can change. Additionally, in bipolar devices bias current polarity usually changes polarity. This problem could potentially cause large errors if source impedances at the positive and negative inputs are not very small and/or matched (a return to pre-picoampere-bias-current days when matching IC op amp signal-source impedances was vital). Offset current, rather than bias current, is again, the name of the game. Newer devices have more sophisticated p- and n-type circuits which eliminate most of the problems. In addition, op-amp designers have moved to some other technique such as charge pumps or a depletion-mode FET to handle some of these problems.

Pumping Charge

The MAX4162 family of op amps use a pair of on-chip charge pumps to beat the problem. The pumps create floating 2-V supplies that are inserted between

the op amps' first two stages' positive and negative supply-rail pins and the circuits they power. To the outside world, the input and second stage appear to have a positive rail 2 V higher than the chip's input supply, and a negative rail that's 2 V lower than the negative rail. Motorola took a different tack with their MC33502 op amp, mentioned earlier. It has an n-channel MOSFET that operates in the depletion mode for voltages close to the negative rail and moves smoothly into the enhancement mode for voltages closer to the positive rail (ELECTRONIC DESIGN, Feb. 17, p. 87).

Virtually all rail-to-rail op amp output stages employ a common-collector/common-drain (rather than the more common emitter-follower/source-follower) output (third) stage. The Maxim 4162 trio of devices do so as well. In addition, the use of the charge pump on the second stage (but not on the third stage) brings the gate of the output MOSFETs high enough to drive their drains typically within 30 mV of the positive rail.

Ideally, the output load of rail-to-rail op amps is connected to a stiff voltage source (a virtual or phantom ground) halfway between the positive and negative rail in order for its output to swing positively and negatively when there is no negative supply rail below ground. SGS-Thomson offers the TS3V912, a dual, rail-to-rail I/O op amp combined with a dual, rail-to-rail I/O comparator that also contains an adjustable phantom ground. For some applications the output load is connected to the positive or negative rail.

Manufacturers' List

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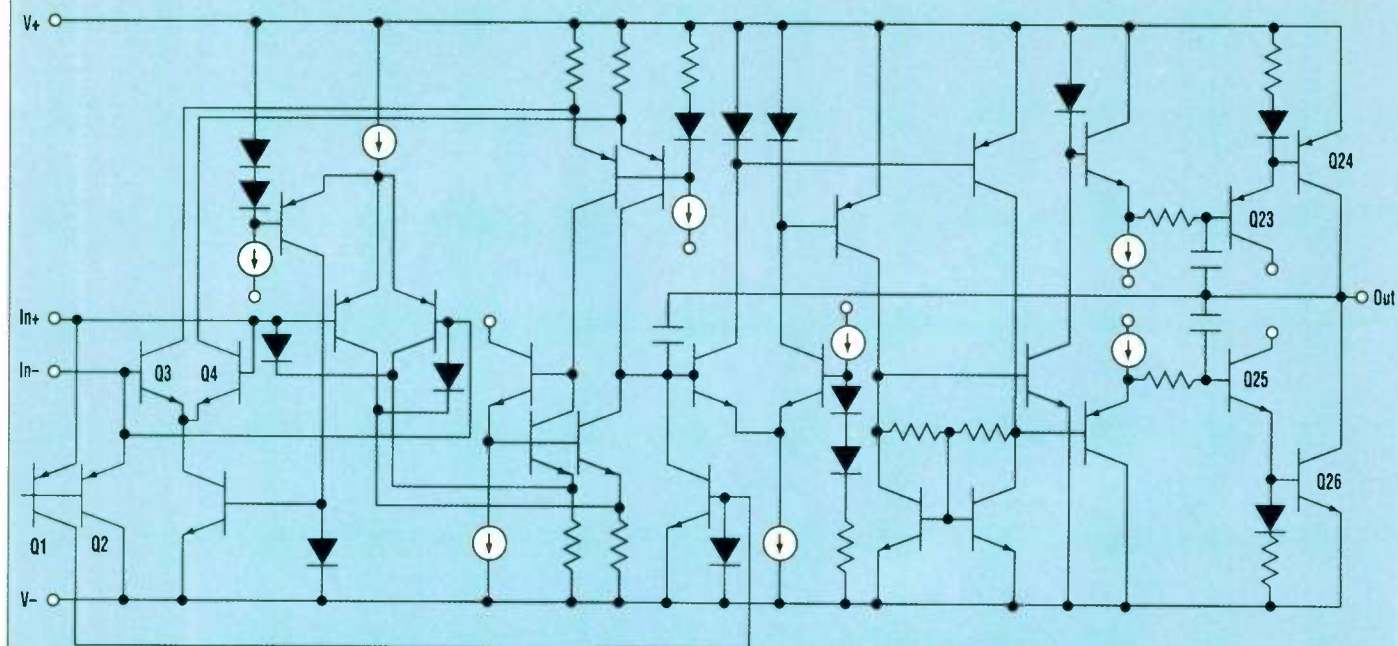


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4. The Linear Technology LT1366 rail-to-rail I/O op amp employs a typical bipolar input stage consisting of pnp transistors Q1 and Q2, and npn transistors Q3 and Q4. The output uses complementary pnp/npn transistors Q23/Q24 and Q25/Q26, respectively.

Rail-to-rail I/O op amps are very difficult to compare because each supplier calls out their unique specifications under different test conditions. For example, some suppliers provide specifications at two different supply voltages with different test conditions for each.

Many op amps that profess to be rail-to-rail types are, in fact, not. These include high-speed, high-voltage, and high-power/high-voltage models which no one can call micropower devices. Many of these devices have unique specifications. However, a sampling of true or nearly true rail-to-rail op amps can be helpful (*see the table*). When examining data sheets, the designer should look at these factors carefully.

The table covers a sampling of rail-to-rail I/O micropower op amps, most of them duals, in tiny, TSSOP-8 or smaller proprietary packages. If singles, in most cases they're available in five-pin SOT packages or the SO-8. In most cases they operate with split supplies.

Many of the op amps whose CMV cannot swing to the positive rail are very wideband devices. Examples include the ground-sensing EL2150 from Elantec, which handles CMVs to within 1.2 V of a 3- or 5-V single supply rail. It not only sports a 0.1-dB bandwidth of 30 MHz, but it draws just 3 mA from its

supply (3-dB bandwidth runs 125 MHz). And Analog Devices' ground-sensing AD8052 (dual) swings its output to within 15 mV of both rails. Its input can drop 200 mV below the negative rail and climb to within 1 V of the positive rail. The true claim to fame of this TSSOP-8 voltage-feedback op amp is a 3-dB bandwidth of 110 MHz and 0.1-dB bandwidth of 12 MHz. It's fully specified for operation from 3-, 5-, and ± 5 -V rails. When powered from a 5-V rail it puts out 45 mA at 4.5 V, but needs just 6.5 mA.

Maxim's MAX4162 family is their first rail-to-rail op amp line to use charge pumps. Earlier devices such as the MAX4122/4123/4124/4129 use bipolar transistors (*see the table, again*). They use a typical input stage consisting of npn and pnp transistors to handle voltages beyond both supply rails (*Fig. 1*).

Micrel recently jumped into the rail-to-rail op amp fray with the dual MIC7101 and MIC7111. The input of the MIC7101 can handle inputs that run 300 mV beyond either rail and run off supply rails from 2.4 V to 15 V. The MIC7111 provides a rail-to-rail output as well. Both come in the five-pin SOT.

Motorola's MC33502op amp operates with supply rails at just 1 V, but its data sheet only specifies operation at 5 V. However some performance specifica-

tions are provided at lower voltages (*see the table, again*). In addition to the "Smartmos" rail-to-rail op amp, Motorola also has a family of bipolar op amps (the dual is the MC33202) that uses a scheme similar to that of *Fig. 1* to handle voltages exceeding the supply rails.

Each op amp designer, depending on available process capability, has their own favorite way of handling rail-to-rail I/O problems, and designers at SGS-Thomson are no exception. Their dual CMOS TS3V912 uses a common source output stage to which it adds a unique driver consisting of amplifiers A1 and A2 and MOSFETs M1 and M2 (*Fig. 2*). A1 and A2 perform three functions: they translate dc levels to drive M1 and M2, they stabilize the current in the output stage, and they provide gain to drive the output stage hard. M1 and M2 limit the short-circuit current in the output stage.

To beat the input rail-to-rail problem, designers at Linear Technology (LTC) combined a single charge pump with zero-drift (chopper stabilizing) circuitry to create a very high precision rail-to-rail I/O op amp, the LTC1152. The precision applies to the low offset voltage and low offset drift. The floating 2-V pump's output is inserted between the chip's power-supply pin and

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an internal bus that powers the first stages of the op amp, thus providing the output stage drive (Fig. 3a). The op amp also features an output stage that sinks or sources 10 mA from a single 5-V supply while maintaining rail-to-rail output swing under most loads. With a 5-V supply the output stage looks like a perfect rail-to-rail voltage source in series with $140\ \Omega$. It lets the output swing to 4.4 V with a $1000\text{-}\Omega$ load (Fig. 3b). This resistance increases as the supply voltage drops, and running off a 1.5-V rail typically provides an output swing of 1.3 V across $1000\ \Omega$. It hardly can be considered as micropower—the op amp needs 3 mA from its supply.

Like Maxim, not all of LTC's rail-to-rail op amps use charge pumps. Some bipolar devices use their version of the dual npn- and pnp-input stage technique. These include the dual LT1366 (see the table, again). They beat the aggravated change in offset voltage and its attendant distortion and degraded CMRR by trimming npn and the pnp input stages separately (Fig. 4). As a result, they have a typical CMRR of over 90 dB. They also specify a maximum offset voltage shift of $425\ \mu\text{V}$ as the CMV is moved from zero to the supply rail. For the dual LT1366, the difference in offset shift is $900\ \mu\text{V}$ between the two amplifiers over the same range of CMVs.

Burr-Brown has jumped into the rail-to-rail I/O IC op-amp arena with their OPA336 (single, dual, and quads). This CMOS device has a p-FET first stage and an n-FET second stage. However, it is not a true rail-to-rail input device, but rather a ground-sensing op amp because its input can swing from 200 mV below the negative rail to 1 V below the positive rail. It should be noted that even under these conditions the offset voltage varies no more than $\pm 125\ \mu\text{V}$. Also, unique Class-AB control circuits let the output swing within a few mV of both rails. Like many ground-sensing op amps not covered in this report, if the input signal is well controlled there's no need for the CMV to be able to reach the plus rail. But as supply voltages get lower, and they will, that need becomes even greater.

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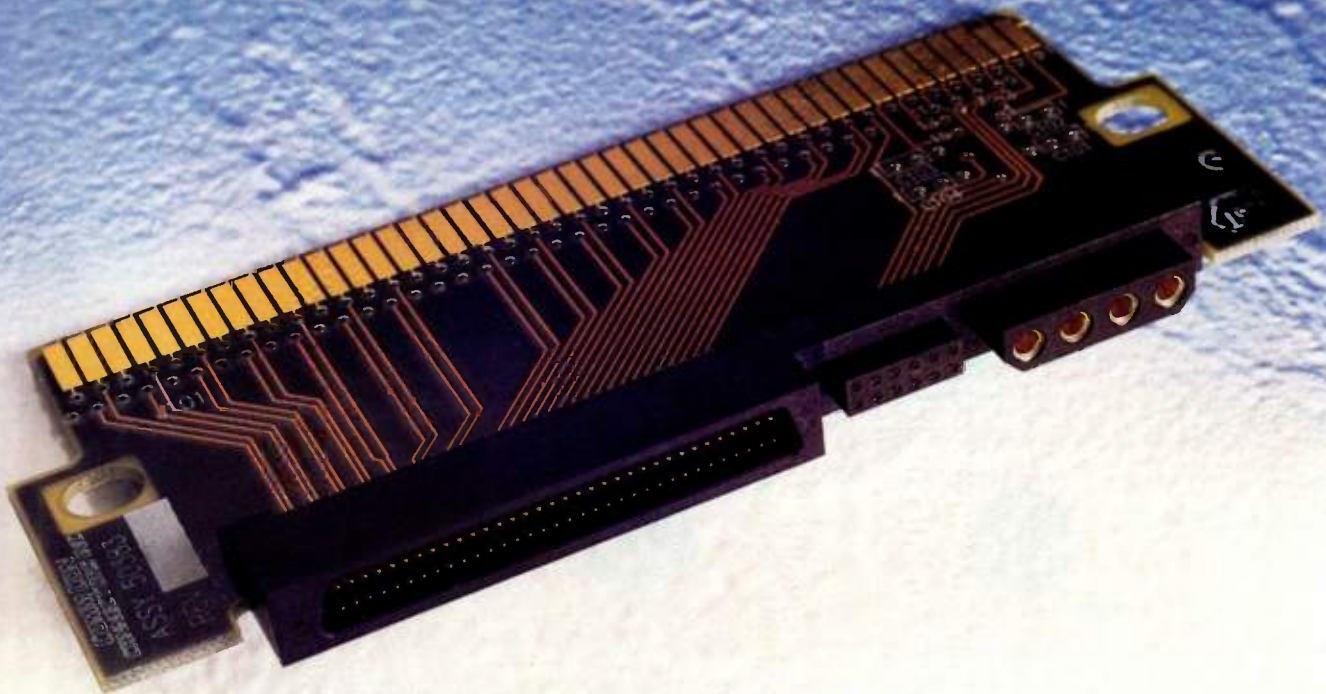
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Capacitor Options And Advances For High-Frequency Applications

Recent Technology Advancements Greatly Improve The Reliability And Cost Of Surface-Mount Capacitors In Wireless Designs.

DAVID RITCHEY, Philips Components, 1440 Indiantown Rd., Jupiter, FL 33458; (561) 745-3354; fax: (561) 745-3692.

Designers working on high-frequency, wireless applications must always be aware of the fact that at high frequencies, and over wide temperature ranges, the characteristics and performance of some capacitors will change. These changes can affect impedance, capacitance, equivalent series resistance (ESR), and equivalent series inductance (ESL).

While ceramic multilayer capacitors (CMCs) are often the capacitor of choice for high-frequency applications, the cost of achieving the close capacitance tolerances needed to prevent series and parallel resonance, among other effects, has been a frustration. However, thanks to new processes and technologies, this situation is changing. In addition, a trend toward integration of passive devices is saving extremely valuable space and improving reliability, while reducing parasitic effects and overall cost.

Ranking The Choices

There are four well-established capacitor choices—mica, film, solid tantalum, and CMCs (*see the table*). While mica capacitors score high in reliability, resistance-to-pulse voltage, high-frequency use, and long life, they suffer from limited range, a lack of surface-mount compatibility, limited availability, and high cost. Film- and solid-tantalum capacitors score well in capacitance range, pulse-voltage resistance, dc voltage dependency, and reliability. However, they score on the

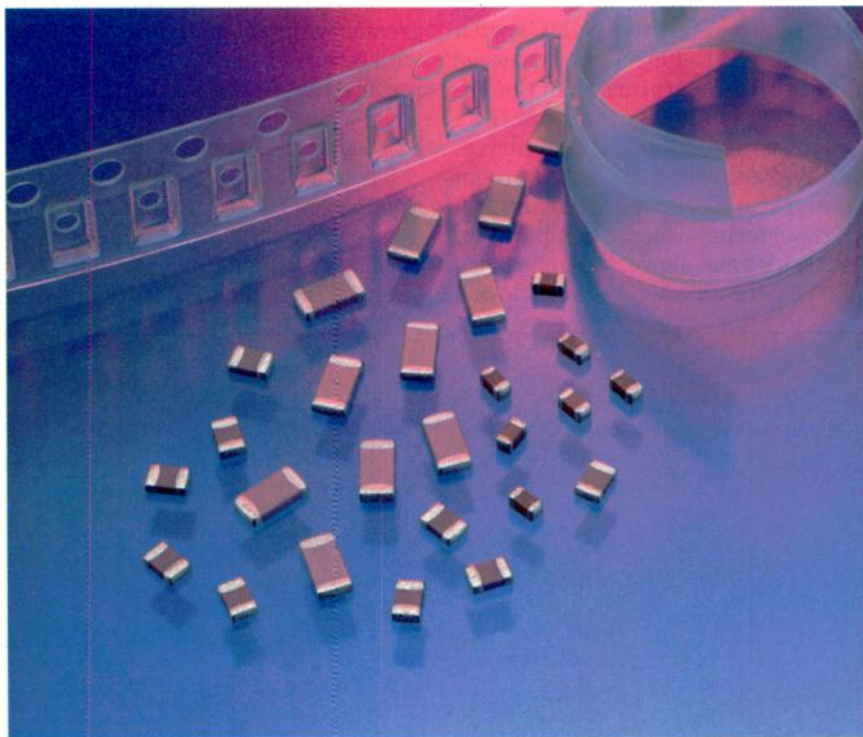
low side in applications beyond 300 MHz. On the other hand, CMCs (in an NPO dielectric) fare well in nine of the 10 primary characteristics, with only one average score.

In general, the need to pack more performance into less space—and the cost associated with that—make surface-mount tantalums and ceramic chip capacitors more desirable than

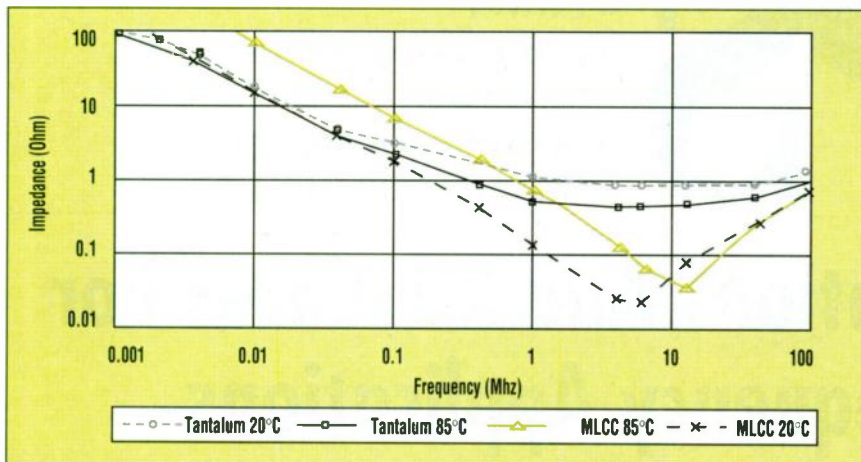
film- and leaded-type capacitors in high-frequency applications (*Fig. 1*).

Tantalum Vs. Ceramic

Because their capacitance and voltage ranges are in the same ballpark, surface-mount ceramic devices often directly compete with surface-mount tantalums. However, as the operating frequency and temperature changes,



1. The need for better frequency response, greater reliability, and more performance in less space—as well as the cost considerations—make surface-mount ceramic chip capacitors more desirable than tantalum, film, and leaded-type capacitors in high-frequency applications.



2. As a general rule, above 200 kHz, the impedance of a Y5V-based CMC becomes considerably less than that of a tantalum capacitor of the same value (in this case, 1 μ F).

there are a number of areas in which the two can be clearly differentiated. These areas include impedance, dc stability, and capacitance.

Impedance behavior at high frequencies is one key area where ceramic surface-mount devices offer performance advantages over other capacitor technologies, including tantalum. In applications such as decoupling, impedance often influences—and frequently determines—anticipated performance levels.

Generally, at frequencies below 100 kHz, the impedance of CMCs with Class 2 or X7R dielectrics increases more with temperature than the impedance of tantalum capacitors (Fig. 2). However, at 100 kHz and above, CMCs offer lower impedance at room temperature. Between 100 and 200 kHz, performances are comparable. At 200 kHz and above, the impedance of a Y5V-based CMC becomes lower

than that of a tantalum capacitor of the same value. For more temperature-stable X7R capacitors, the impedance is nearly the same as tantalum through to about 10 kHz.

Dc stability, or the ability to maintain capacitance under dc bias, is typically good for solid tantalums. CMCs, however, surrender some capacitance when a dc-bias voltage is applied.

Capacitance reduction as the operating frequency increases is another design consideration. The effect of increased frequencies on capacitance is greater with tantalum capacitors than with ceramic multilayer chips. It is especially true of lower-voltage tantalums.

Parasitic Elements

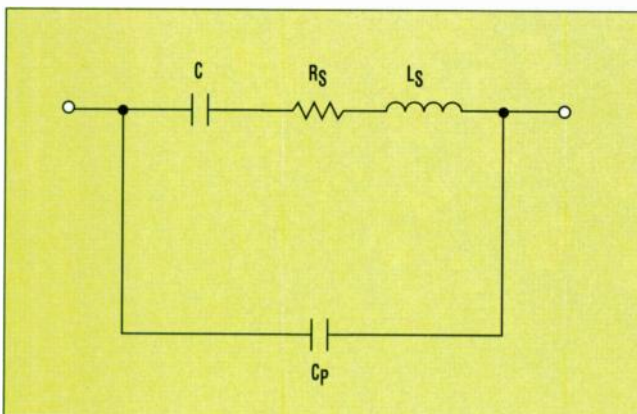
Though closer to the ideal capacitor than film and solid tantalums, ceramic caps still contain parasitic elements that become critical at higher frequencies (Fig. 3). In an ideal capacitor, as fre-

quency increases, impedance steadily falls (Fig. 4). At gigahertz frequencies, parasitics cause a capacitor to behave as a resonant circuit with series and parallel resonant frequencies. Series resonance occurs when the reactance of the parasitic series inductance (L_s) equals the capacitor's (Fig. 3, again). At frequencies below series resonance, the impedance is mainly capacitive; above series resonance, it is mainly inductive. The series and parallel resonance points shown are only the first series and parallel resonances; others may occur at higher frequencies (Fig. 4, again).

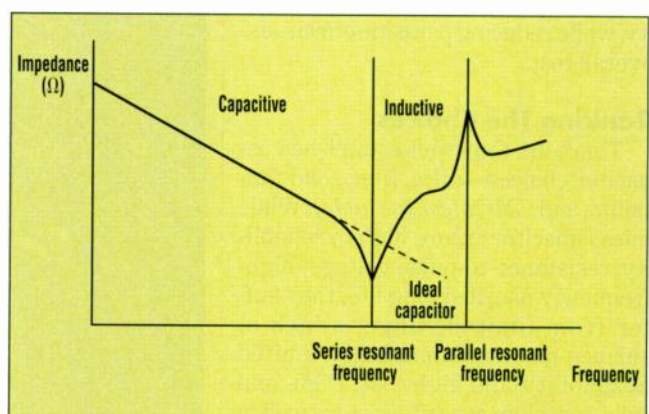
Since it is the capacitive properties that are required for blocking, filtering, and matching, the capacitor should be operated below its series resonant frequency. For example, in the blocking function, where the capacitor is connected in series with the line to block dc current flow, the inductive nature of the capacitor, beyond its series resonant frequency, causes it to exhibit gradually higher insertion loss. This loss results in high-frequency roll-off of the signal.

Trimming Costs

Capacitors from different suppliers with identical ratings for capacitance, dissipation, and voltage, often perform quite differently in a high-frequency transceiver circuit. Because these circuits operate at high frequencies, the dc capacitance of the device chosen must often be less than 1 pF. Standard, low-value capacitors, however, are usually available with tolerances of ± 0.25 pF, which can be around 10%, and, in some cases, even 50% of the value of the capacitor. Because determining how



3. An equivalent circuit of a typical ceramic multilayer capacitor shows the primary capacitance C , equivalent series resistance R_s , and the parasitic elements of inductance L_s and capacitance C_p .



4. At gigahertz frequencies, parasitic components cause the ideal capacitor to exhibit series and parallel resonances. The points shown are only the first instances; others may occur at higher frequencies.

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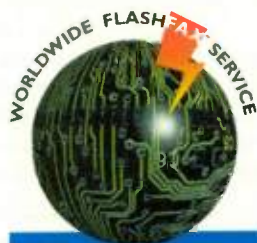
The newest microprocessors are pushing power supply designers to use low equivalent series resistance (ESR) capacitors to control ripple current and ripple voltages. Other factors including power dissipation capabilities, lower voltages, miniaturization, surface mount assembly and operating frequencies also affect the designer's selection of filter capacitors.

For frequency filtering below 500kHz, Sprague's 593D solid tantalum chip capacitor offers the best combination of low ESR, good power dissipation, and a machine friendly flat surface for consistent placement.

Like all solid tantalum chip capacitors, the 593D is extremely stable under temperature changes and time. In addition, it has no end-of-life constraints or known wear out mechanisms for excellent reliability and stability.

The 593D features values ranging from 1.5 μ F to 330 μ F, and voltages from 6.3 to 50. This product is in an industry standard molded chip package for full compatibility with existing pad layout designs.

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Available in a Miniature
Film Capacitor
with 5mm Lead Spacing



Roederstein Electronics, Inc. has expanded its MKP 1840 series of metallized polypropylene film capacitors to include a miniaturized version with the highest C-values available with 5mm lead spacing. Fully auto-insertable, these capacitors allow the design engineer to take advantage of a much reduced printed circuit board footprint while maintaining the superior characteristics of the polypropylene dielectric.

Polypropylene's excellent stability, very low dielectric absorption, high insulation resistance and low dissipation factor make these capacitors ideally suited for use in designs where precision is required, such as audio and instrumentation applications. Most commonly these capacitors are used in oscillators, timing and LC/RC filter circuits, high frequency coupling/decoupling, cross-over networks, and sample and hold circuits.

Roederstein's MKP 1840 capacitors are also self-healing and do not exhibit a piezoelectric effect. The new 5mm lead-space capacitors are available in C-values up to .10 μ F and in a 100-volt rating. Larger sized capacitors are available in higher voltages and capacitance values up to 10 μ F. All are encapsulated in flame-retardant cases.

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0612 Capacitor
Cuts Inductance
by More Than Half



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The Vitramon chip (VJ0612) provides standard inductance levels as low as 0.3nH. The package dimensions are 0.062" L x 0.126" W with thicknesses from 0.020" to 0.038". Standard capacitance range is from 8200pF to 0.22 μ F with tolerances of $\pm 5\%$, $\pm 10\%$, $\pm 20\%$ and voltage ratings of 25V and 50V.

This combination—available in a robust, easily mounted package—makes the VJ0612 ideal for use in new designs where low inductance is important as well as for improving the performance of existing circuitry.

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COMPARISON OF CAPACITOR OPTIONS

Characteristic	Mica	Film	Solid tantalum	CMC (NPO)
Capacitance range	-	+	+	+/-
Size/cost	-	-	+	+
HF use (>300 MHz)	+	-	-	+
Res. Pulse Voltage	+	+	+	+
Bipolarity	+	+	-	+
Lifetime @ T>85°C	+	+	-	+
Breakdown voltage	+	+	-	+
DC voltage dependency	+	+	+	+
SMD compatibility	-	+/-	+	+
Reliability	+	+	+	+

Key: ++ = superior; + = good; +/- = average; - = poor.

much an individual component will deviate from specification is impossible, circuit manufacturers have resorted to trimming each circuit to ensure predictable behavior. For CMC manufacturers, trimming means that they are not forced to use expensive narrow-tolerance, microwave CMC devices.

Thanks to recent improvements in screen printing and electrode manufacturing, new varieties of narrow-tolerance CMCs are becoming available. They have an improved price/performance ratio, making them a more attractive alternative to trimming. The use of base-metal-electrode (BME) technology to replace noble metals in the inner electrodes opens the door for thinner electrode and ceramic layers—allowing for greater capacitance values for a given size. Tighter control of the final value of that capacitance is provided by the use of finite-element-analysis techniques during manufacture.

The new narrow-tolerance capacitors provide higher reliability and stability with voltage and temperature variations, and come with AgPd or NiSn terminations that handle reflow or wave soldering. Along with X7R and Y5V, the BME CMCs also come with a Z5U dielectric. With BME technology, and other process improvements, the falling cost of narrow-tolerance CMCs has made them a more viable and welcome alternative to the time and expense of individually adjusting capacitance values.

designers should consider. The parasitics generated by discrete components are dramatically reduced by replacing several discretes with one component. These integrated packages also outperform thick-film products at high frequencies. In developing the new technology, Philips compared a silicon IPC filter with discrete components. The result was that the IPC solution attenuated noise 10 dB more than the discrete configuration.

In addition to reducing board space, integrating passive components simplifies handling in manufacturing and cuts time spent on reordering and inventory of components. Resistor networks, resistor/capacitor networks, and combinations of inductors and capacitors in standard SSOP, QSOP, SOIC, and SOT-23 packages are now available. While unit cost of integrated devices is several times that of discretes, the technology offers savings of up to 40% in assembly and purchase costs. Cellular phones are among the most promising markets for integrating passive components.

David Ritchey is senior product/application engineer at Philips Components, where he previously spent 16 years as a ceramic process engineer at the company's monolithic capacitor surface mount and thru-hole facilities. Prior to that, he spent 10 years at capacitor manufacturer CAL-R Inc.

Consider Integrating Passives

Integrating passive components in a standard silicon package is another promising move high-frequency circuit

HOW VALUABLE

HIGHLY
MODERATELY
SLIGHTLY

CIRCLE

558
559
560

"Glad I thought of that!"

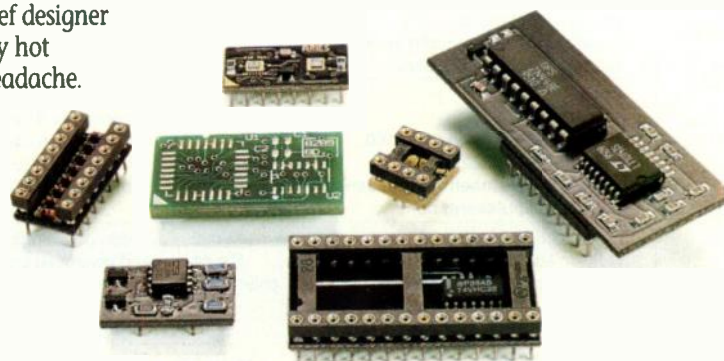
"Upgrading boards already in production used to be a nightmare. Then I discovered ARIES Correct-A-Chip™ technology. Now it's a dream."

THE PROBLEM

"Things change fast in this business...too fast, sometimes. Just when I'd get a new board into production, my phone would ring. The chief designer just had a vision! The boards must change!...we had some pretty hot discussions, let me tell you. *They* had a new toy – *I* had a new headache.

THE SOLUTION

"A friend at another company told me she used to have the same problem, and solved it with Aries Correct-A-Chip technology. She said Aries could let me change from through-hole to SMT, work with any kind of footprint, even crank up performance in the same board space. And she was right! Those design changes don't bother me anymore. In fact, now that I'm plugged into Correct-A-Chip, I sleep like a baby. Thanks, Aries!"



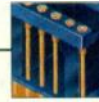
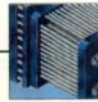
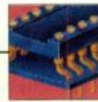
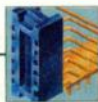
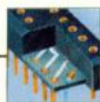
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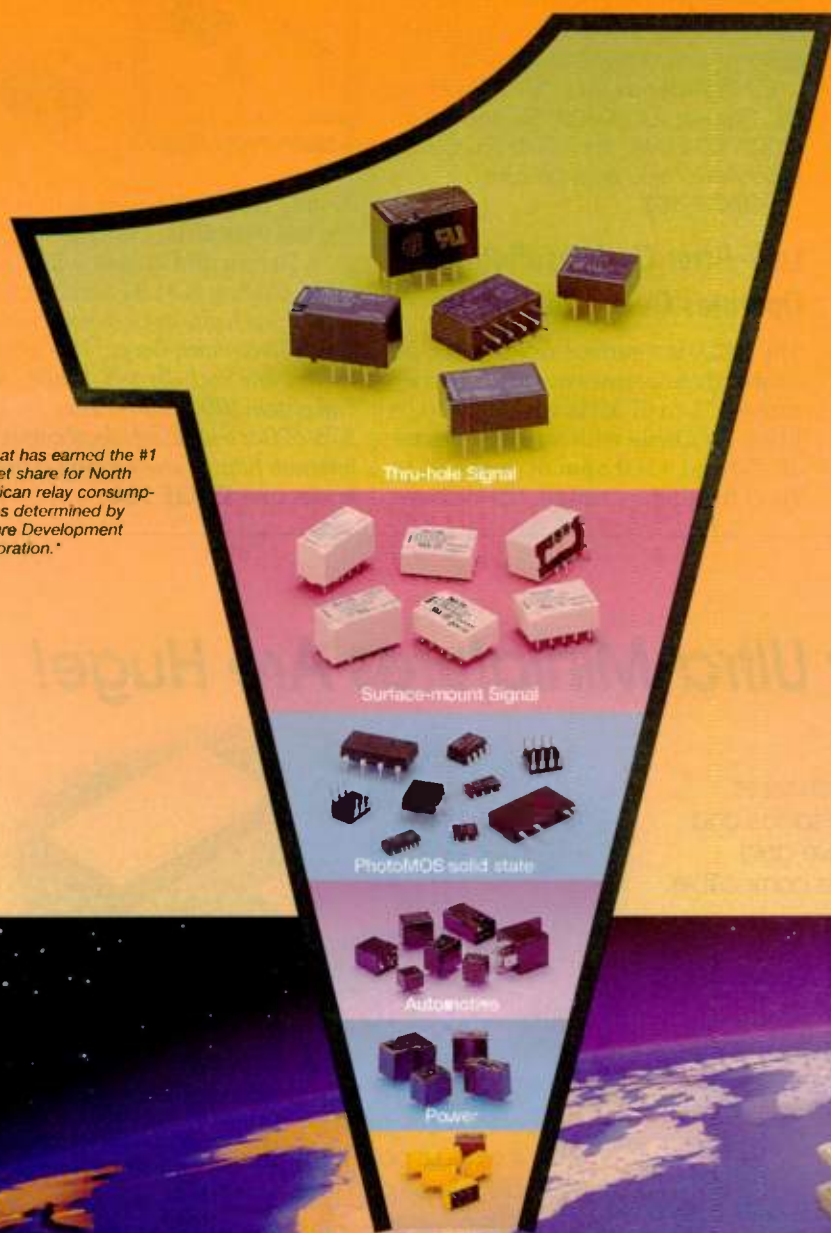
PRODUCT UPDATE: RESISTORS, TRANSFORMERS, AND INDUCTORS

Manufacturer	Device	Description	Price & availability	CIRCLE
API Delevan Inc. East Aurora, NY Denis Kohlhausen (716) 652-3600 Fax (716) 652-4814 E-mail: apisales@delevan.com http://www.delevan.com	LP Series inductor	Measuring less than 0.050 in. high, these low-profile, wire-wound inductors come in a range of 4.7 to 1000 nH. A variety of tolerances are available, and packaging is on tape and reel.	\$0.64 to \$0.69 each per 1000; six weeks ARO.	502
BI Technologies Corp. Fullerton, CA Janet Vaniman (714) 447-2371 Fax (714) 447-2400 E-mail: jvaniman@ni.net	Tantalum nitride resistor network	This line of tantalum nitride-based resistor networks have a power rating per resistor for isolated configurations of 100 mW at 70°C and a power rating for bussed configurations of 75 mW at 70°C. Resistance values range from 10 to 270 Ω and 10 to 130 Ω , respectively. A standard TCR rating is available at 50, 100, and 200 ppm/°C.	Under \$0.50 each in quantity; six to eight weeks ARO.	503
KOA Speer Electronics Inc. Bradford, PA Dawn McGriff (814) 362-5536, ext. 266 Fax (814) 362-8883	LPC 9040 inductor	Capable of carrying dc currents up to 1.55 A, this wire-wound inductor has a resistance of 0.06 Ω and comes with inductance values ranging from 10 to 680 μ H. Tolerances are $\pm 10\%$ and $\pm 20\%$ and dimensions are 0.35 (diameter) by 0.19 (high) in.	\$0.85 each; 10 weeks.	504
Bicron Electronics Company Canaan, CT Frank Pierzga (860) 824-5125, ext. 305 E-mail: info@bcn.com http://www.bcn.com	STP1726 Solenoid	The STP1726 is a 0.54-in.-diameter push/pull tubular solenoid for computers, business machines, and electronic security devices. The solenoid generates up to 15 oz. of force at a distance of 0.05 in. with 10% duty cycle. The device includes shock- and noise-abatement features, and can be easily mounted using 2-56 NC-2B threaded taps.	Under \$4 each in quantity.	505
Caddock Electronics Inc. Roseburg, OR Applications Eng. (541) 496-0700 Fax (541) 496-0408	MP725 power resistor	This D-PAK-style, surface-mount power resistor is rated at 25 W at a case temperature of 25°C. The electrically isolated heat sink can be soldered to the assembly. Features include resistance values from 0.020 Ω to 1.00 k Ω and tolerances of $\pm 1\%$, $\pm 5\%$, or $\pm 20\%$.	1% tolerance, \$1.63 each 1000; eight weeks ARO.	506
Cal-Chip Electronics Inc. Warminster, PA Sales Dept. (215) 672-5500 Fax (215) 672-5501	Type CN resistor array	Available in three standard case sizes, 0603, 0805, and 1206, these thick-film chip resistor arrays have tolerances of ± 1 or 5%. Resistor powers range from 0.063 W at 70°C to 0.125 W at 70°C, depending on package size. The temperature coefficient is ± 200 ppm/°C.	\$0.18 to \$0.065 each per 5000; four weeks ARO.	507
Prem Magnetics Inc. McHenry, IL Derek Brooke (815) 385-2700 Fax (815) 385-8578 E-mail: sales@premmag.com http://www.premmag.com	SPT-049 transformer	This low-profile transformer targets V.34 modem applications and comes with B.S.I. approvals. The device measures 0.520 (long) by 0.460 (wide) by 0.400 (high) in. Primary to secondary creepage distance is 2.5 mm (min), the turns ratio is 1:1, and the impedance is 600 Ω . The hi-pot rating is 1500 Vrms.	\$3 each in quantity.	508
Pulse San Diego, CA Mukesh Mehta (619) 674-8190 Fax (619) 674-8262 E-mail: mukeshmehta@pulseeng.com http://www.pulseeng.com	T5005-T5010 transformer	These surface-mount, low-profile transformers target ISDN S interface applications. The devices use the company's interlock base construction for uniform positioning and can withstand 235°C solder reflow temperatures. Each provide 2000 Vrms isolation and are approved to UL 1459 and UL 1950.	\$2.60 each per 10,000.	509
Noble U.S.A. Inc. Rolling Meadows, IL Tom Guarise (847) 364-6038 Fax (847) 364-6045 http://www.nobleusa.com	XV092 Series potentiometers	These board-mounted rotary potentiometers snap in for both vertical and horizontal configurations, and feature a film element that reduces noise and wobble. Resistances range from 5 k Ω to 500 k Ω with linear, audio, and reverse-audio tapers. The maximum operating voltage is 50 V ac or 20 V dc, and the power rating is 0.05 W.	\$0.20 each per 5000.	510
OakGrigsby Inc. Sugar Grove, IL Jeff Shaw (800) 625-8333 Fax (800) 432-9625 E-mail: jshaw@oakgrigsby.com	700 Series encoder/potentiometer	The device is offered as the first push-button mechanical encoder/potentiometer to combine digital or analog circuitry in an 0.890-in. package. The rotary encoder has a life rating of 100,000 cycles and can be installed directly to a pc board with a mounting bracket.	\$1.50 to \$2 each per 1000; eight to 10 weeks ARO.	511
Spectrol Electronics Ontario, CA 91761 Charles Fixa (909) 923-3313, ext. 111 Fax (909) 923-6765	Power- Ω resistor	This non-inductive, planar power resistor is made from a ceramic substrate with an embedded thick-film cermet resistive element. The device meets MIL-STD-202 and MIL-R-22097, and dissipates up to 40 W/in. ² The resistor is available in ranges from 1 to 100 k Ω .	\$0.25 each in quantity; six to eight weeks ARO.	512
Sprague-Goodman Electronics Inc. Westbury, NY Bernice Feller (516) 334-8700 Fax (516) 334-8771	GLZ Series inductors	These epoxy encapsulated, surface-mount inductors measure only 1.0 by 0.5 by 0.5 mm (0402 size) and come in 20 models with an inductance range of 1.0 nH up to 39 nH. Standard tolerance is $\pm 5\%$ and the self-resonant frequency is up to 6 GHz.	\$0.32 each in quantity; eight weeks ARO.	513
Tocos America Schaumburg, IL Bob Kruse (847) 884-6664 Fax (847) 884-6665 E-mail: sales@tocos.com http://www.tocos.com	FF08 trimming potentiometers	These general-purpose, enclosed, carbon trimming potentiometers have a temperature coefficient of ± 250 ppm and a resistance range of 100 W to 1 MW with a $\pm 25\%$ tolerance. The devices measure 0.350 in. in diameter and 0.350 in. high.	\$0.17 each per 1000; stock to eight weeks.	514
UltraCoil Inc. San Diego, CA Darin Valley (619) 674-6686 Fax (619) 674-6685 E-mail: dvalley@ultracoil.com	High-Q inductors	This line of high-Q (50 to over 100) surface-mount inductors target impedance-matching, circuit-isolation, and RF-filter applications. The devices come in 0603, 0805, and 1008 sizes with a wide range of inductance values. The wire-wound devices feature gold flashing terminations and come in tape-and-reel packages.	\$0.20 to \$0.25; three to five weeks.	515

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VCXOs Operate Over Range Of 32 To 120 MHz

The full-size S1510 and the half-size S1519 voltage-controlled crystal oscillators (VCXOs) are designed for phase-locked loops and are available over a frequency range of 32 to 120 MHz. The devices have a frequency stability of ± 25 or ± 50 ppm over all conditions and have an absolute pull range of ± 25 , ± 50 , ± 75 , or ± 100 . Linearity can be specified at either 5 or 10%. The oscillators are HCMOS-compatible and can drive both high-speed CMOS and TTL loads. Available in standard 14- or 8-pin DIP, the devices are in an all-metal, resistance-welded package with an operating temperature range of 0° to 70°C or -40° to 85°C . A tri-state version also is available in a full-size, six-pin package. Pricing is from \$7 to \$18 each per 10,000; delivery is from stock to 12 weeks.

SaRonix, 151 Laura Lane, Palo Alto, CA 94303; Sales Dept. (800) 227-8974; fax (415) 856-4732; e-mail: saronix@connectinc.com; Internet: <http://www.saronix.com>. **CIRCLE 582**

100-F, Double-Layer Capacitor Comes In Small Package

Measuring 35 by 50 mm, the DynaCap Model DZ-2R5D107 double-layer capacitor produces 100 F of capacitance with less than $0.08\text{-}\Omega$ resistance. For applications requiring large bursts of power with an instantaneous recharge capability, the capacitor is capable of one million cycles with no degradation in performance. Pricing is from \$23 each per 1000; delivery is six to eight weeks ARO.

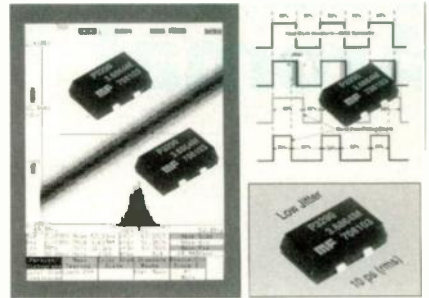
ELNA America Inc., 5770 Warland Dr., Cypress, CA 90630; Satoshi Konishi (800) 700-ELNA; fax (714) 761-9188; <http://www.elna-america.com>.

CIRCLE 583

Low-Jitter Clock Oscillator Operates Over 1 to 67 MHz

The P3290 is a surface-mount clock oscillator that operates over a frequency range of 1 to 67 MHz with only 10 ps jitter. Available with stability grades of $+50$ and $+100$ ppm over the 0° to 70°C frequency range, the devices

have an output symmetry of 40/60 or better when driving loads to 50 pF. The oscillator runs off a 5-V supply, is compatible with CMOS and TTL logic, and has a maximum current draw at 5 V of



35 mA. The plastic-encapsulated package has overall dimensions of 9.8 by 14 by 4.70 mm and comes with four J-leads. Pricing is \$1.95 each per 10,000; delivery is from stock to six weeks.

MF Electronics Corp., 10 Commerce Drive, New Rochelle, NY 10801; Martin Finkelstein (800) 331-1236; fax (914) 576-6204; e-mail: mfsales@mfelec.com; Internet: <http://www.mfsales@mfelec.com>. **CIRCLE 584**

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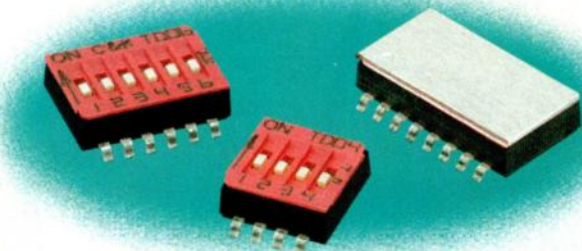
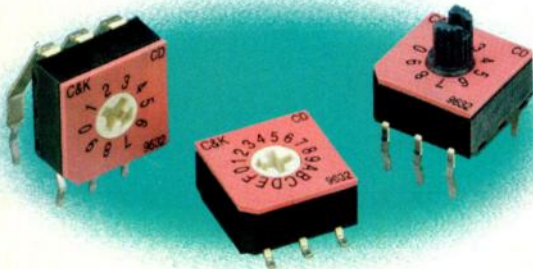
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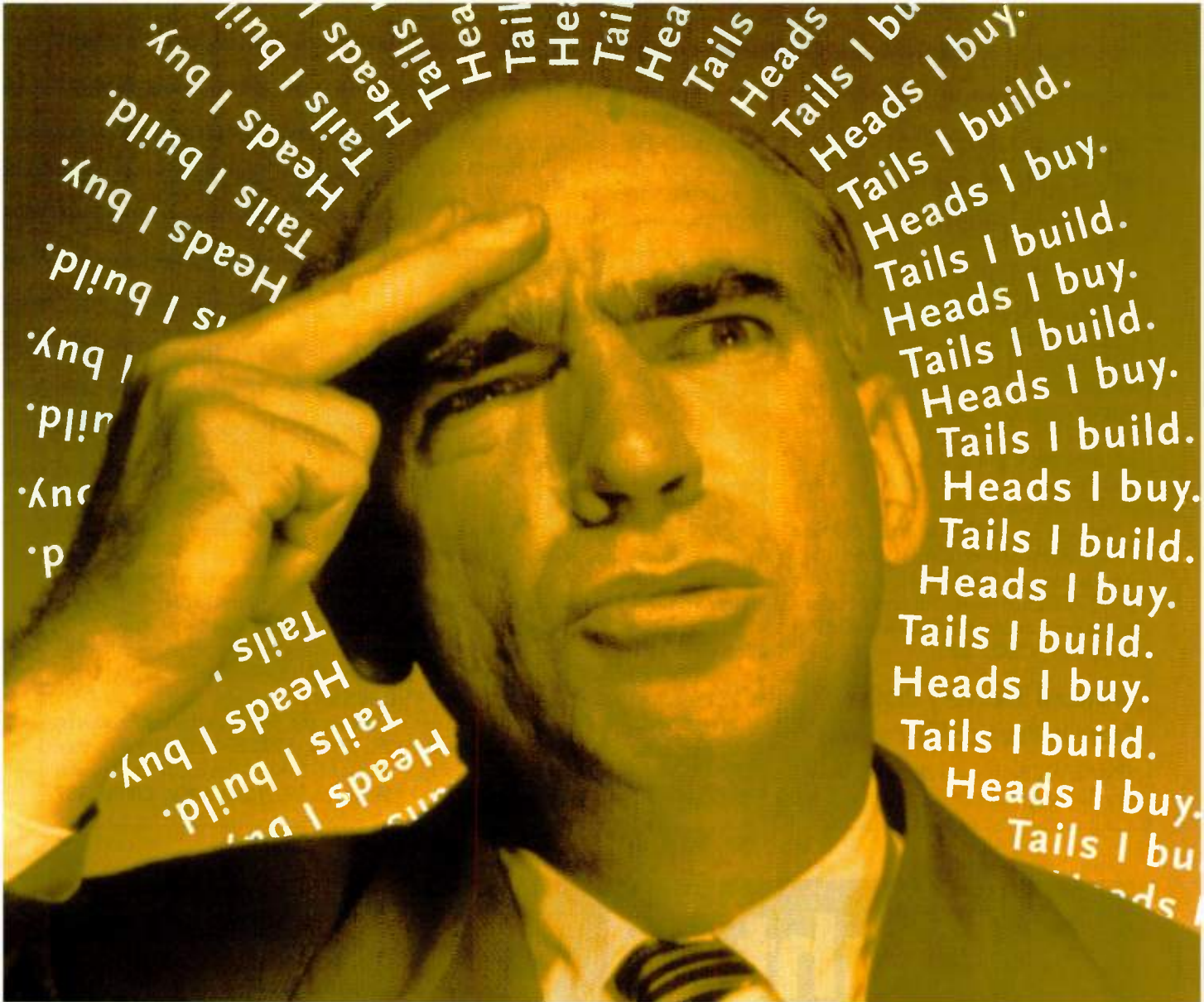
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READER SERVICE 194

High-Temperature Fuses Are Rated At Up To 5 A

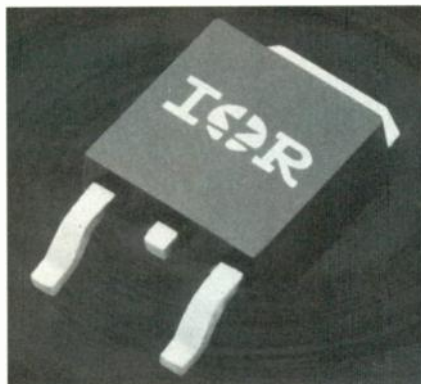
Available in surface-mount or axial-leaded versions, the EIA 1206 fuse is hermetically sealed and rated at 5 A at temperatures of up to 150°C. The surface-mount version has a flip-chip design for mounting on any side, while the axial-leaded version mounts with lead holes as close as 0.2 in. The fuses are UL- and CSA-approved from 200 mA to 3 A at 125 V; approvals are pending for 4 to 5 A at 32 V. Pricing is from \$0.34 each per 5000 and delivery is from stock to six weeks.

Schurter Inc., 1016 Clegg Ct., P.O. Box 750158, Petaluma, CA 94975-0158; Sandy Hansen (800) 848-2600; fax (707) 778-6401; e-mail: shansen@schurterinc.com; Internet: <http://www.schurterinc.com>. **CIRCLE 585**

Standard Recovery Diodes Come In Plastic SMT Package

The 8EWS Series are standard recovery diodes in a plastic surface-mount

package (D-PAK or TO-252AA) that are rated at 800 to 1600 V. Based on a moat process used in stable, high-voltage input diodes, the devices operate



off line voltages from 110 to 380 V, handle up to 8 A, and under thermal cycling show no forward voltage change or leakage current drift. Pricing starts at \$0.30 each in large quantities.

International Rectifier, 222 Kansas St., El Segundo, CA 90245; Sales Dept. (310) 322-3331; fax (310) 252-7171; <http://www.irf.com>. **CIRCLE 586**

Schottky Diodes Have Fast Fast Reverse Recovery Times

The BAT54 series of Schottky barrier diodes comprise the BAT54LT1 (single) and BAT54SLT1 (dual) and feature a reverse recovery time of 5.0 ns (max). Housed in an SOT-23 package,



the 30-V devices have a forward voltage of 0.35 V (typical) at $I_F = 10$ mA dc. Total capacitance is 10 pF (max) and forward power dissipation is 200 mW. Pricing for the BAT54LT1 is \$0.11; the BAT54SLT1 is \$0.18 each.

Motorola Semiconductor Products, SPS-Z207, 5005 E. McDowell, Phoenix, AZ 85008; Kimi Fodroczi (602) 244-5902; fax (602) 244-5406. **CIRCLE 587**

Lighted Quality



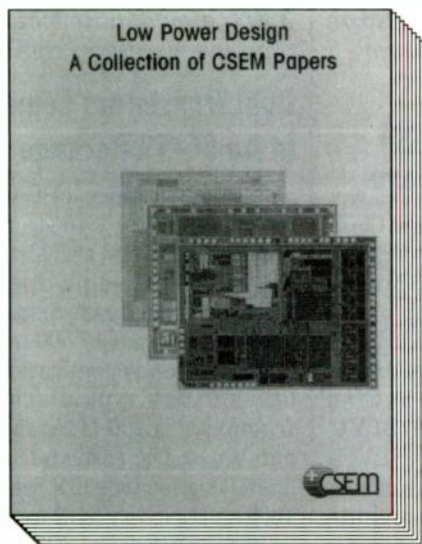
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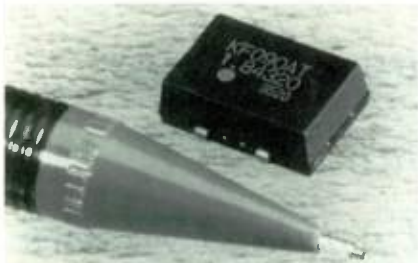
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Pin-for-pin and function-for-function interchangeable with the standard SG615 oscillator, the KFO90AT is offered as a low-cost alternative for cost-



sensitive applications. The J-leaded component drives up to 10 TTL gates or a 50-pF HCMOS load and runs off a 5-V supply. The input current varies between 25 mA and 60 mA within the frequency range of 1.8 to 67 MHz. The oscillator maintains a frequency stability of ± 100 ppm and has an operating temperature range of -10° to 70° C. Pricing for a 20-MHz device is \$1.74

each per 1000, or \$1.43 each per 10,000; delivery is stock from 10 to 12 weeks.

Fox Electronics, 5570 Enterprise Parkway, Fort Meyers, FL 33905; Customer Service (888) GET-2-FOX; fax (941) 693-1554; e-mail: sales@foxonline.com; <http://www.foxonline.com>

CIRCLE 588

Voltage Suppressors Target Portable And Video Systems

Part of the company's SLV Series, these low-voltage (2.8 V) transient voltage suppressors offer overvoltage protection for power, video, and communication ports. IEC 1000-4 compliant, the devices offer up to four bidirectional lines (SLVDA) of protection in an SO-8 package. Single unidirectional (SLVU and SLVG) and bidirectional (SLVE) versions also are available in surface-mount packages. Features include greater than 15-kV ESD protection, a peak pulse power of 300 W, a reverse standoff voltage of 2.8 to 3.3 V, and a capacitance of between 50 and 100 pF. Pricing is: SLVU2.8, SLVG, SLVE

\$0.62; four-line SLVDA2.8 \$3.26 each per 1000, with immediate availability.

Semtech Corp., 652 Mitchell Rd., Newbury Park, CA 91320-2289; Tom Dugan (805) 498-2111; fax (805) 498-3804; e-mail: npsmtchtd@aol.com; <http://www.semtech.com>. CIRCLE 589

Dual Transistors Come In An SC-59 Package

The IMX18T146 is a SOT-23-size device comprising two standard, independent, A06 npn transistors in a six-pin SC-59 package. Specifications include a breakdown voltage of 80 V, a collector current of 500 mA, a gain of 100 (min.), and a saturation voltage of 0.25 V (0.05 V typical). The transition frequency is 100 MHz at $I_C = 10$ mA and $V_{CE} = 2$ V. Availability is on 3000- or 10,000-piece reels. Pricing is \$80 per 1000 and delivery is 12 weeks ARO.

Rohm Electronics, 3034 Owen Drive, Nashville, TN 37013; Sales Dept. (800) 955-ROHM; fax (615) 641-2022; <http://www.rohmelectronics.com>.

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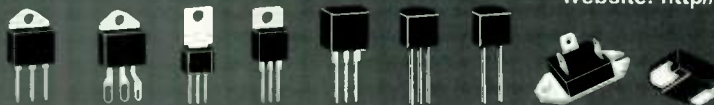


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POWER

Compact DC-DC Converters Have A Wide Input Range

Measuring 2 by 2 by 0.4 in., the 3000WFR series of 30-W dc-dc converters have a 2:1 input voltage range and an MTBF of over 750,000 hours. Features include 500 V dc input-to-output isolation, continuous short-circuit protection, an output-voltage accuracy of $\pm 2\%$, and a line/load regulation figure of $\pm 1.0\%$. The device's operating temperature range is -25° to 71°C .

CP Clare Corp., 78 Cherry Hill Dr., Beverly, MA 01915-1048; Sales Dept. (847) 797-7000; fax (847) 797-7023; <http://www.cpclare.com>. **CIRCLE 591**

NiMH Prismatic Battery Is Lightweight And Rugged

The 530-mAh PH-530 is the latest addition to the company's line of plastic-case prismatic NiMH batteries. The device outputs 1.2 V, weighs 13.3 g, and has a lifespan of 1000 cycles. Recharging can be done over a range of rates from continuous trickle charging to fast

charging at a 2C rate. The rigid, glass-filled polyimide case is hermetically sealed. Pricing is \$1.25 each per 25,000. Delivery is two to three weeks ARO.

Plainview Batteries Inc., 23 Newton Rd., Plainview, NY 11803; Bernie Erde (800) 642-2354; fax (516) 249-2876.

CIRCLE 592

Dual-CCFT Inverter Targets Sharp LCD Panels

The LS520 dual-CCFT inverter module is offered as only the second such device to provide built-in brightness control. Designed for powering backlights on Sharp LCDs, the module outputs 3.9 W per tube and can drive 6-, 12-, and some 14-in. displays. It also is compatible with Toshiba and NEC displays with a JST connector. The module measures 130 (long) by 20 (wide) by 13.5 (high) and provides an open-circuit output voltage of 1500 V rms. Pricing is \$29 each per 1000 and delivery is 12 weeks ARO.

Xentek Power Systems Inc., 1770 La Costa Meadows Dr., San Marcos, CA

92069; Scott Sato (760) 471-4001; fax (760) 471-4021; <http://www.xentek.com>. **CIRCLE 593**

Backlight Inverter Supports Four CCFLs And LCDs

The LXM1640 inverter module supports four cold-cathode fluorescent lamps and targets LCDs from 15 to 20 in. and over. The inverter converts a 12-V-dc supply and allows for an ad-



justable lamp current of up to 5.5 mA for each lamp. Features include a 3:1 brightness ratio, a sleep current of 30 μA (typical), output short-circuit protection, and output open-circuit protection. Pricing is \$59 each per 1000.

Linfinity Microelectronics Inc., 11861 Western Ave., Garden Grove, CA 92841; (800) 877-6458; fax (714) 893-2570. **CIRCLE 594**

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READER SERVICE 139

POWER

Compact, 65-W AC-DC Supply Has Multiple Outputs

The UP065 Series ac-dc switching power supply measures 3.0 by 5.0 by 1.2 in., outputs up to 65 W, and has three outputs. Two of the outputs are



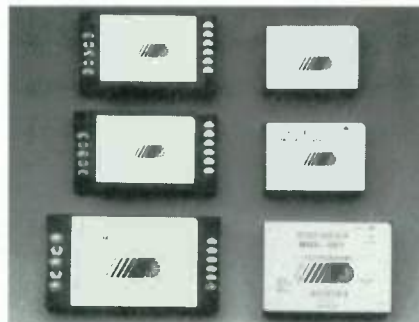
regulated to within $\pm 1\%$, while the third has high pulse-current capability. Features include 75% minimum efficiency, continuous short-circuit protection, a built-in EMI filter, and a universal input of 90 to 264 V ac. All models in the series are UL-, CSA-, and TUV-approved. Pricing is under \$40 each in quantity.

International Power Sources Inc.,

200 Butterfield Drive, Ashland, MA 01721; Jack Schwartz (508) 881-7434; fax (800) 226-2100; Internet: <http://www.intlpower.com>. **CIRCLE 595**

Miniature AC-DC Switchers Have Low-Leakage Option

Covering the range of 5 to 30 W, this line of ac-dc switching power supplies is UL-, CSA-, TUV-, and CE-approved. A special IEC-601-1-compli-



ant, low-leakage version for medical applications also is available. The supplies have a universal input of 50 to 256

V ac, come in pin-mount and chassis-mount packages, have single, dual, or triple outputs, and operate over an ambient temperature range of 0° to 50°C. An LED power-good indicator and an output adjustment potentiometer are provided. Pricing is \$29 each in quantity and delivery is four weeks ARO.

Astrodyne, 300 Myles Standish Blvd., Taunton, MA 02780; Paul Charrette (508) 823-8080; fax (508) 823-8181.

CIRCLE 596

Power-Factor-Corrected, 375-W Switcher Has Four Outputs

The LN Series switching power supply handles 375 W, comes with four outputs, and has input power factor correction (0.99). The supply comes in a fan-cooled case, measures 2.5 by 5 by 11 in., and takes a 90- to 264-V ac input. The main output is 5 V dc at 45 A, complemented by a 12-V dc, 12.5-A or 14.5-A output. These share a common ground. Two auxiliary outputs are selected from 5 V dc at 5 A, 12 V dc at 2 A, (continued on page 128)

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POWER

(continued from page 126)

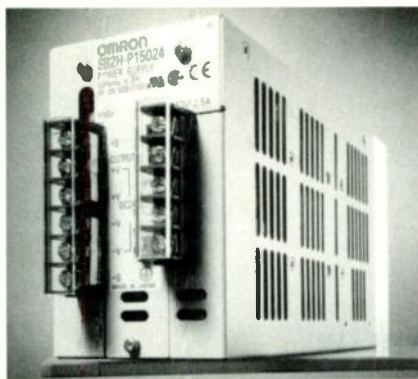
and 24 V dc at 1 A. Other voltages are available on special order. Features include 0.5% line regulation on all outputs, 1% load regulation on the 5- and 12-V high-current outputs, and 3% load regulation on the low-current outputs. Pricing starts at \$385, down to \$0.67/W in quantity. Delivery is five days for samples and eight weeks for quantity.

Unipower Corp., 3900 Coral Ridge Drive, Coral Springs, FL 33065; John Jimenez (954) 346-2442; fax (954) 340-7901; e-mail: sales@unipower-corp.com; Internet: <http://www.unipower-corp.com>.

CIRCLE 597

Universal AC-DC Supplies Have Power Factor Correction

The S82H series of switching power supplies include power factor correction and range in power from 100 to 600 W with inputs from 100 to 240 V ac. Available output voltages are 5, 12, 15, and 24 V. Features include remote sensing and voltage adjustment, remote control, and overload and overvoltage protec-



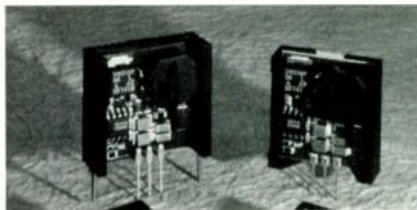
tion. Approvals include UL, CSA, VDE, and CE. Pricing starts at \$305 and delivery is from stock for the 24-V output 100-, 300-, and 600-W versions.

Omron Electronics Inc., 1 East Commerce Dr., Schaumburg, IL 60173; Sales Dept. 800-55-OMRON; fax (847) 843-8081. **CIRCLE 598**

Plug-In Switching Regulators Are Low Cost

Based on the company's original 78 Series, the PT78/79 Series of integrated,

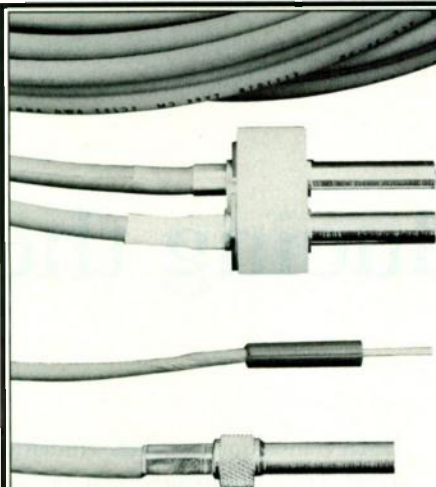
plug-in switching regulators are offered as a low-cost alternative. The series comprises the PT78ST1 and PT78HT2 1.5-A and 2-A positive step-down regulators, respectively; the PT78NR1 1-A, plus-to-minus con-



verter; and the PT79SR1 1.5-A negative step-down converter. Features include a conversion efficiency of over 85%, overtemperature and short-circuit protection, and compatibility with the company's 78/79 Series linear regulators. Pricing is \$7.95 each per 1000.

Power Trends, 27715 Diehl Rd., Warrenville, IL 60555; Don Matthiesen (800) 531-5782; fax (630) 393-6902; e-mail: sales@powertrends.com; Internet: <http://www.powertrends.com>.

CIRCLE 599



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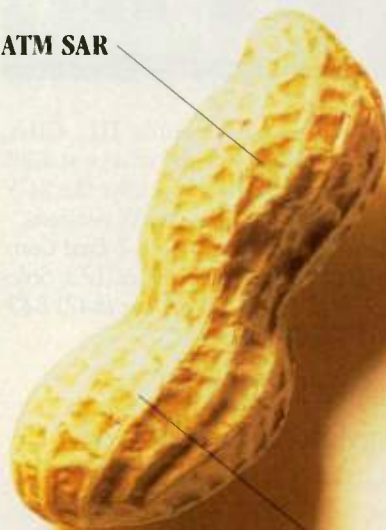
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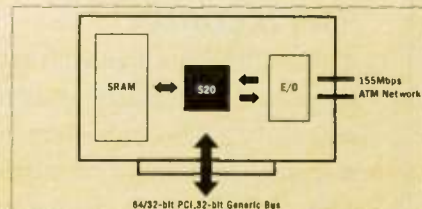
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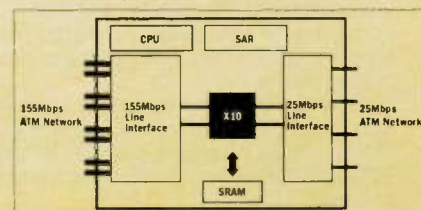
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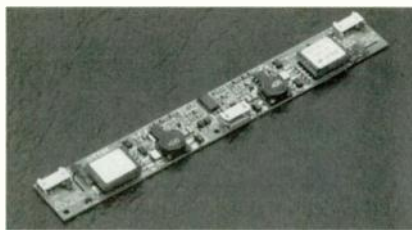
READER SERVICE 171

W25

POWER

DC-AC Inverter Powers Dual CCFL Backlight For 14-in. LCDs

Requiring just 7 W, the CXA-P1212-VJL is an efficient dc-ac inverter designed to power a dual-CCFL backlight for color or monochrome 14-in. LCD displays. The inverter features dual outputs with individual current feedback control for each lamp, an 8-mm profile, and a footprint of 25 by 180



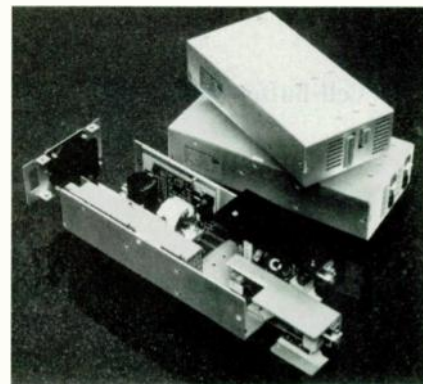
mm. Other features include a soft-start circuit, an open-circuit startup

voltage of 1500 V, and an output current of 6 mA into each lamp. Pricing is \$18 each per 1000, with immediate availability.

TDK Corp. Of America, 1600 Feehanville Drive, Mt. Prospect, IL 60056; Pat Carson (847) 390-4478; e-mail: power@tdkca.com; or on the Internet: <http://www.tdk.com>. **CIRCLE 600**

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Initially available in the 400- to 800-W range, the SSI ModuPower Series of high-power-density switch-mode power supplies come in a modular form for flexibility and quick turn-



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Switching Systems International, 1590 Sinclair St., Anaheim, CA 92806; Jack Pouchet (714) 996-0909; fax (714) 996-2753. **CIRCLE 601**

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(continued on page 132)

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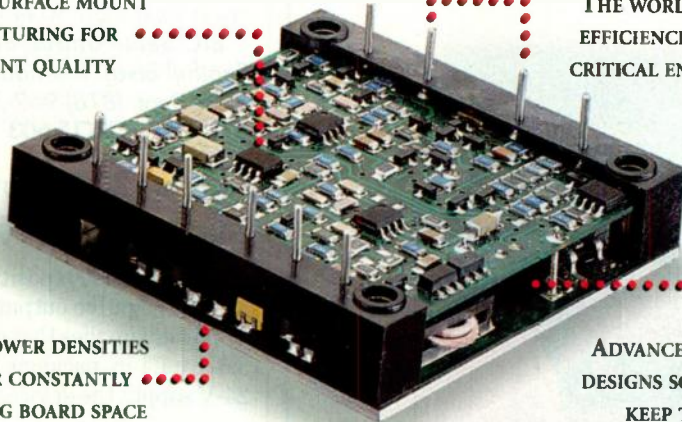
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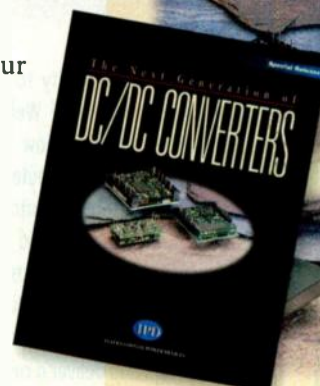


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POWER

(continued from page 130)

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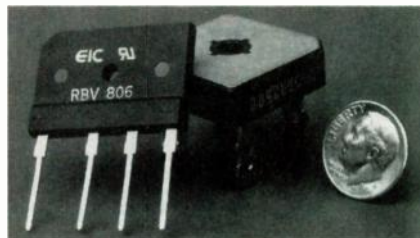


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EMCO, 11126 Ridge Rd., Sutter Creek, CA 95685; Sales Dept. (209) 223-3626; fax (209) 223-2779; e-mail: sales@emcohighvoltage.com; Internet: http://www.emcohighvoltage.com.

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PC GRAPHICS WATCH

Specifying And Procuring Flat-Panel Displays

Mike Grote, National Information Display Labs, Sarnoff Corp.

When system integrators go comparison shopping for flat-panel displays (FPDs) they usually end up wasting lots of time. They can't efficiently compare FPDs from different manufacturers because comprehensive evaluation standards aren't in place. Fragmented and incomplete, existing standards bewilder and overwhelm users. In addition, the critical performance characteristics determining image quality of FPDs aren't completely specified and procedures for measuring them aren't in place. As a result, users rely on their subjective judgment rather than on photometric measurements to guide them.

VESA's Flat Panel Display Measurements (FPDM) Workgroup is helping to rectify this problem with an easy-to-use display measurement standard. The FPDM Workgroup was formed to develop voluntary standards for the measurement of flat-panel displays and to give a clear focus to the development of accurate and practical display measurement procedures.

Display users and system developers must efficiently and cost-effectively specify, compare, procure, and use display monitors that meet their needs. They have to adjust and maintain the display's performance for their particular applications and environments. They also must determine when the display should be readjusted and/or replaced. Finally, they need manufacturers to provide high-performance displays whose avail-

ability and improvement is driven by commercial markets and competition.

In April 1995, VESA began developing a suite of unambiguous measurement procedures from which manufacturers and users can pick and choose. The group's initial goal was to define a suite of basic measurements (SBMs) for the characterization of direct-view flat-panel displays of all technologies including LC, EL, plasma, and FE. The suite is a small set of the most important measurements selected from all the procedures contained in the FPDM standard. The standard provides guidelines for the setup procedure, analysis, and reporting of each measurement. The FPDM standard procedures will yield results that are accepted, used internationally, and consistent with CRT displays. The long-term goal is to expand the scope of standards to include projection systems that house flat-panel image sources, HMDs, HUDs, and CRTs.

The workgroup is leveraging the latest information through a collection of evolving display-measurement standards (IEC, ISO, ANSI, HFES, NAPM, SAE, EIA, EIAJ, NIDL, NIST, and others), and through individual companies' experience and techniques. The standard is based heavily on the LCD measurement standard of the Electronics Industries Association of Japan (EIAJ). Many of these methods are reproduced with the EIAJ's permission.

The unnecessary and expensive waste of purchasing over- and under-specified displays is minimized when

standardized measurements provide the exact performance criteria for display selection. Objective performance reports will enable users and operations and maintenance personnel to track display performance over time. It also will let them identify and quantify drifts that impact display image quality to determine cost-effective monitor-adjustment schedules, and implement and plan for equipment replacement.

The FPDM document is not a compliance standard—it's a voluntary practice describing good metrological practices. It helps users make correct and unambiguous measurements by using the widest variety of low-cost test equipment available.

The ultimate benefit of establishing measurement standards and promoting their use is to ensure that manufacturers are providing high-quality displays. To this end, the FPDM document provides commercially-accepted procedures, through which users will be able to clearly specify their needs to display makers. The document empowers users to do efficient comparison shopping for displays for specific environments. Finally, commercially accepted display measurement standards will minimize "specsmanship" and spur competition and innovation.

The FPDM standard contains over 60 procedures organized into nine major photometric measurement sections including: Setup; center-screen measurements; resolution and artifacts; temporal performance; luminance and color uniformity; viewing-angle characteristics of luminance, color, and contrast ratio; and screen reflections. Electrical and mechanical measurement procedures are included for characterizing power consumption, luminance efficiency, display size, and strength.

For further information on the FPDM standard, contact VESA at (408) 435-0333, or on the Internet at: <http://www.vesa.org>.

Take The Mystery Out Of AC Termination

Understanding How to Implement AC Termination, Helps Maintain The Power And Cost Levels In High-Speed Buses.

DR. JOHN NEMEC, California Micro Devices Corp., 215 Topaz St., Milpitas, CA 95035; (800) 325-4966 or (408) 263-3214; Internet: <http://www.calmicro.com>.

Today's high-speed bus applications require the use of terminations to enable proper system operation. System designers can select from various termination options to achieve the optimal balance between performance and cost. Various choices include standard parallel termination, series-resistor termination, dual or Thévenin termination, diode termination, and ac termination. Of these choices, ac termination has the potential to maintain signal integrity while reducing power consumption in high-speed applications.

High-speed buses using a point-to-point configuration of drivers and sources are tailor-made for the ac-termination alternative. Results of the analysis show that the capacitor can charge almost completely, and still provide effective termination. In addition, the relatively small current requirement of ac termination results in significant power supply cost savings.

In multidrop environments (both in a single driver with multiple receivers, and multiple drivers with multiple receivers), ac termination has some limitations. Depending on the signal levels required, ac termination may not be able to achieve the desired signal levels at any arbitrary point along the line, unless the line is short. Other termination types may be better suited for these designs, and careful analysis is required.

In high-speed systems, the signal-edge rates and bus speeds approach the propagation delay of the bus, making appropriate selection and termination a necessity. Many high-speed systems also use CMOS devices, or similar logic, which have large swings in driver output signal levels. Com-

bined with low-impedance buses (typically 47 Ω to 70 Ω), common in practical pc-board traces, using parallel or Thévenin termination for a transmis-

sion line in these environments has significant disadvantages. Specifically, the added power needed due to a constant dc current flow through the ter-

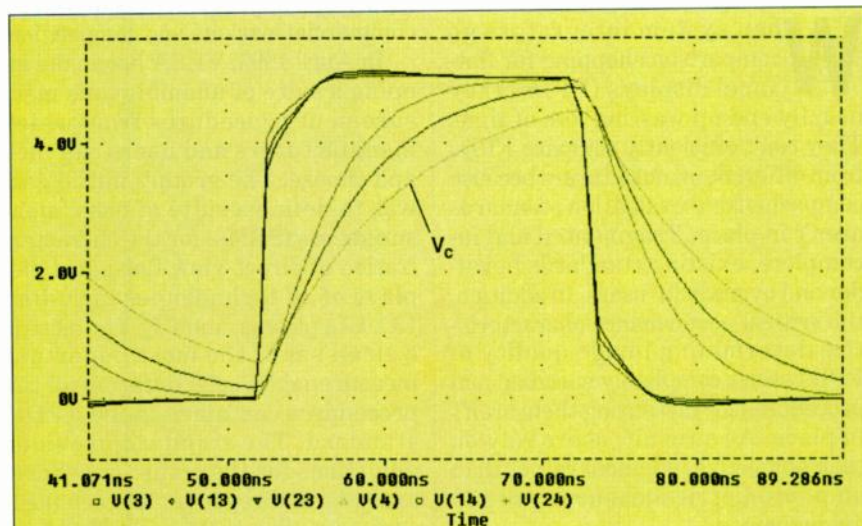


Figure 1a

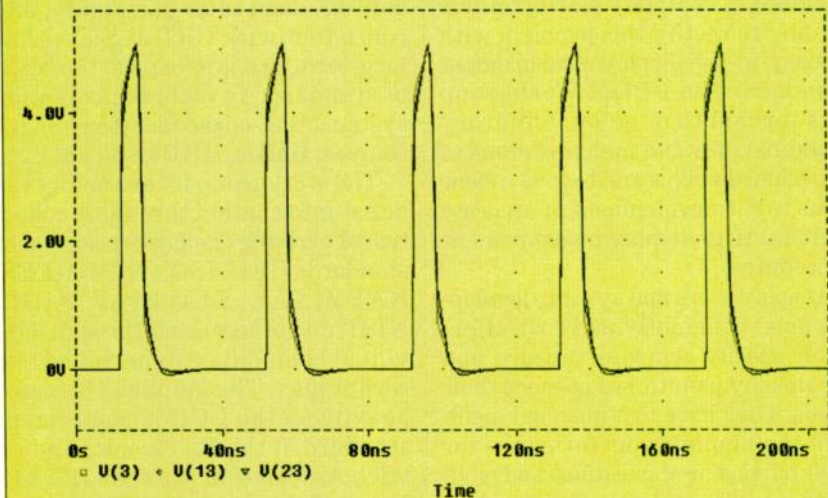


Figure 1b

1. Based on the requirement to make the overshoot reach the driver's open circuit voltage, the signal amplitude maintains acceptable noise margins, using values of $R_s = 10, 15$, and 20 W (a). In addition, the overshoot and edge-to-edge interaction is held to a minimum (b).

TWO COOL!

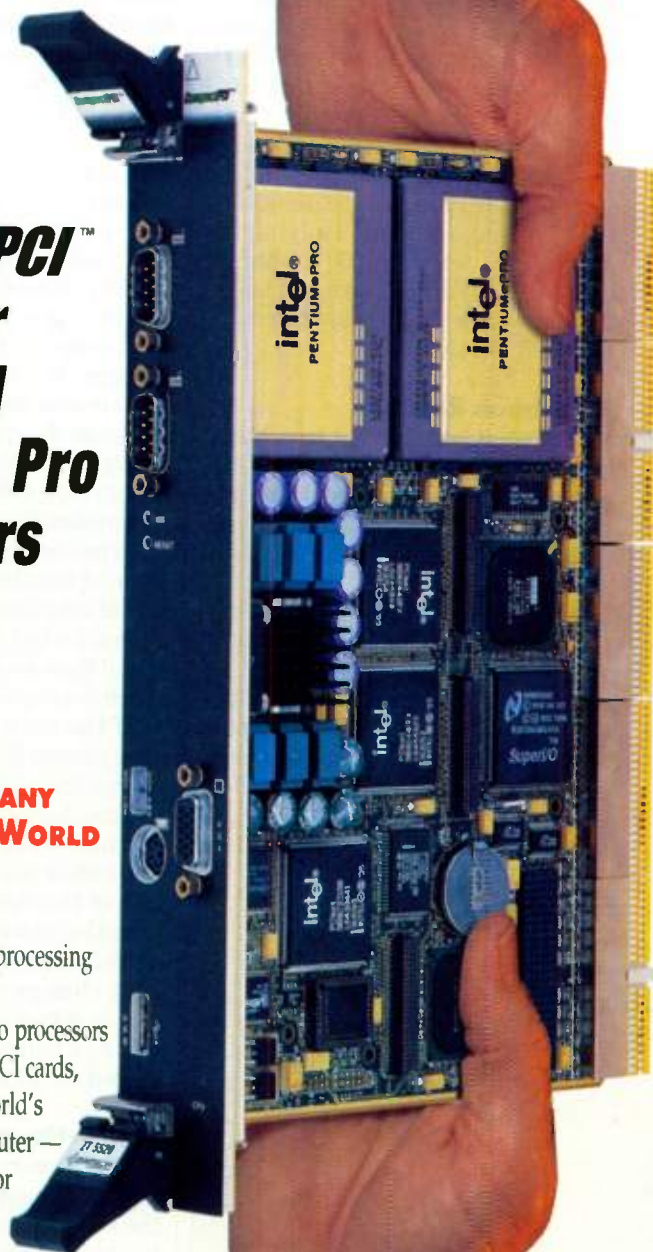
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mination resistor can be a serious drawback. In larger systems, several watts of power may be wasted, or additional cost may be incurred to provide a separate power supply.

The ac termination alternative consists of a resistor in series with a capacitor. The resistor performs the termination and the capacitor blocks the dc average current, saving considerable power. Additionally, ac termination can match the bus impedance, like pure resistor terminations, but with minimal signal reflection. And, it can be placed at the end of the transmission line while maintaining the signal integrity, like parallel and Thévenin terminations.

Optimum Design

Optimum ac termination for a point-to-point application is achieved when the peak amplitude of the first signal reflection on the transmission line equals the driver's open-circuit voltage. Meeting this criterion results in a terminated signal with sufficient amplitude to achieve acceptable noise margins, while keeping signal overshoot and edge-to-edge interaction to a minimum. The design involves the calculation of the capacitance value for the ac termination.

When driver rise times are relatively small and the bus propagation delay is significantly less than the signal edge-to-edge times, equation (1) can be applied (see sidebar p. XX), where t_D = propagation delay (ns); Z_0 =

characteristic impedance of the transmission line; R_S = source impedance; and G = source reflection coefficient.

Solving for the optimal termination capacitance value gives rise to equation (2) in the sidebar.

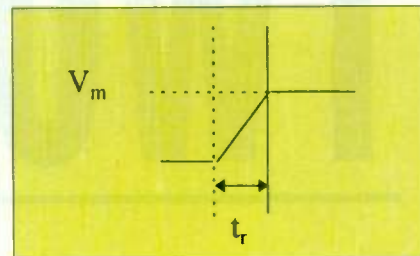
In a practical example, a system employs a 66-MHz data bus which must be terminated. The bus impedance, including loading effects for this system, is 60 Ω . The bus has a one-way 0.8-ns propagation delay. The driver on the bus has an internal 10- Ω impedance, and rise and fall times equal to 600 ps. Signal edge-to-edge time is 15 ns.

Inserting the values from the above example and multiplying the propagation delay by 1000 to obtain a result in picoFarads gives a termination capacitance value shown in equation (3) in the sidebar.

Simulation Results

When this termination capacitance is plugged into a Spice simulation, the signal amplitude maintains acceptable noise margins, while keeping overshoot and edge-to-edge interaction to a minimum (Fig. 1a and b).

Note that the terminated waveform rises to some initial voltage, which is determined by the driver voltage and the ratio of the driver's internal impedance to the bus impedance. The capacitor begins to charge, causing a reflection, and the termination voltage begins to rise. The waveform then reaches a peak, after which



3. When a signal is sent down a transmission line with ac termination, it can be modeled as a linear ramp going from 0 to V_m with a rise time of t_r . At the end of t_r , the signal remains at V_m .

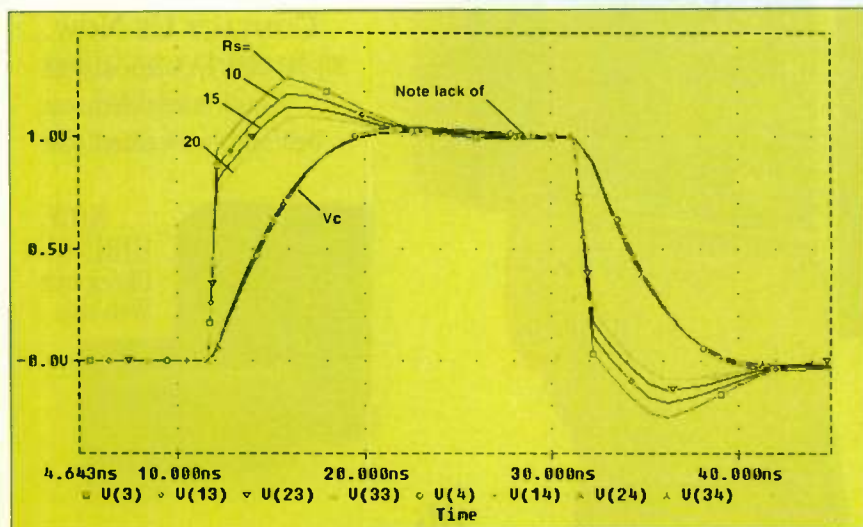
it remains relatively flat. This plateau indicates that reflections are minimized. Using larger or smaller capacitor values results in ringing or edge-to-edge interactions.

There may be a timing budget impact depending on the desired noise margins. The signal waveform rises or falls to some initial value and then continues as the capacitor charges or discharges. If this initial amplitude is within acceptable noise margins, then ac termination has no more impact on the timing budget than a standard parallel termination. If, however, the initial amplitude isn't sufficient, the timing budget must include the additional time required for the signal to reach the required level.

If the capacitor is made excessively large, it can retain a significant charge from edge-to-edge, causing a walking baseline that's duty-cycle dependent. Thus, for short duty cycles (for either the logic high or low portion of the signal), edge-to-edge interaction is a concern. Effects on the waveform would appear as a significant change in the initial voltage reached just after the edge arrival, and as a longer time to reach the required signal levels.

A Low-Power Solution

The power dissipated in an ac termination resistor equals the square of the voltage across the resistor divided by the resistance. This figure is equal to the square of the area between the capacitor and termination voltage (Fig. 2). Note that power is dissipated only when transitions occur, and therefore, power is duty-cycle dependent. Also, the area between the capacitor and termination voltage is about 25% to 30% of the whole area of



2. The square of the voltage across the resistor, which is equal to the square of the area between the capacitor and termination voltage, divided by the resistance is equal to the power dissipated in an ac termination resistor. In this simulation, $V_c(2t_D)/V_S=1$.

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the termination voltage. Because power dissipation is based on the square of the voltage, ac termination will consume less than 10% of the power consumed by parallel termination under the same conditions.

Based on this analysis, the system designer can charge the capacitor almost completely while providing effective termination. The signal current through the termination resistor can be a small fraction of the current through a parallel termination. (Parallel termination also may include dc power-supply current.) This design can significantly reduce the power-supply cost.

Point-to-Point Applications

For practical ac-termination applications, the termination resistor value equals the transmission-line impedance. The interplay between the capacitance and other system conditions makes the termination-capacitance value more difficult to determine. Whether a design can benefit from ac termination requires determination of specific performance issues and factors which may contribute to the loss of signal integrity. This analysis considers the effects of signal rise time, reflections, overshoots, and undershoots in determining an optimal ac termination design.

Rise-Time Effects

The system designer must know under which conditions a signal edge retains its integrity and timing position. A slow edge may invalidate the capacitance value computed in the optimum design. A signal launched down a transmission line with ac termination can be modeled as a linear

ramp from 0 to some maximum voltage, V_m , with a rise time of t_R , after which the signal remains at V_m (Fig. 3). V_m may be smaller than the driver amplitude due to the driver's source impedance. Assume that the driver is relatively stiff with a source impedance, R_S , less than the characteristic impedance of the transmission line, Z_0 . The launched signal amplitude, V_m , is related to the open-circuit driver signal amplitude, V_S , by equation (4) in the sidebar, where Z_0 = the transmission line's characteristic impedance; R_S = the source impedance; and G = the source reflection coefficient.

In the region where the linear ramp is occurring (Fig. 4), the reflected voltage, V_r , is shown in equation (5) in the sidebar, where t_R = rise time; C = termination capacitance; and V_0 = any initial voltage on the capacitor due to previous conditions.

The reflected voltage in Region 1 starts at 0 (when $V_0 = 0$) and increases. The total voltage at the termination will be larger than the incident voltage. The effect of ac termination is to steepen the edge rate slightly and reduce the apparent arrival time of the signal.

In Region 2, the initial ramp is completed and the reflected voltage is shown by equation (6) in the sidebar. In this equation, the time origin is at the beginning of Region 2 and is not the same as t in the previous equation. For very small rise times, t_R can be taken to 0, Regions 1 and 2 combine, and the reflected voltage is shown in equation (7) in the sidebar, where V_{ra} is the reflected voltage using a zero rise-time approximation. The zero rise-time approximation is valid if

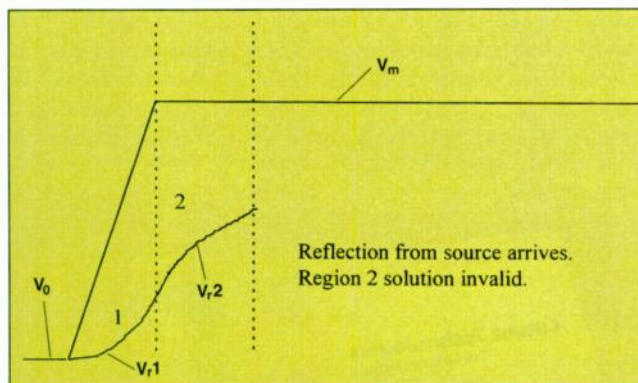
$Vr1(t_R)$ is small compared to V_m .

Using the series expansion for the exponential function, $Vr1(t_R)/V_m$ is on the order of $t_R/4Z_0C$. This suggests that under most circumstances (where $t_R < Z_0C/2$), the rise time of the driver signals is fast enough to have negligible effect on termination performance. Using this result, the driver rise time is neglected and the equation for the optimum value of capacitance can be derived.

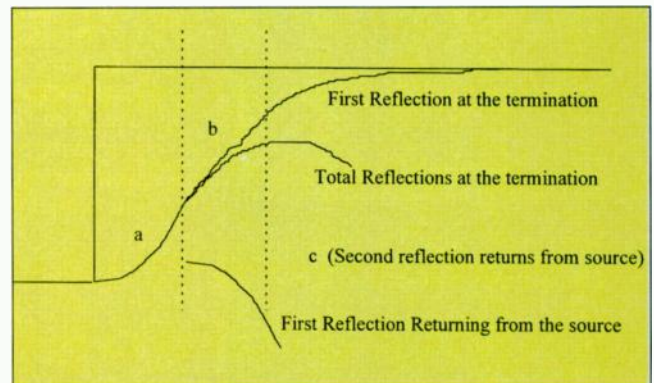
The result from the previous equation indicates that the reflected voltage is rising toward V_m , with a time constant of $2Z_0C$. The total voltage at the termination end is rising toward $2V_m$. The reflected signal will travel back to the source, be reflected, and return to the termination end (Fig. 5).

The reflection from the source will arrive at the termination end of the line, change the voltage waveform, and cause another reflection back to the source. Because the reflection coefficient at the source is negative (low source impedance), the reflection from the source will be opposite in polarity from the reflection at the termination. The series of reflections should quickly reduce in amplitude and die away in a manner comparable to what happens in a close, but not exact, ac termination condition. The largest amplitude overshoot will occur with the first reflection at the termination end, and (approximately) when this reflection arrives back from the source. The peak amplitude above V_m is shown in equation (8) in the sidebar.

A Spice simulation of $V_{r_{max}}$ for various values of Z_0C gives a comparison of the peak overshoot from the simulation versus the predicted values from the previous equation (Fig. 6). Note



4. This plot shows an example of signals with finite rise and fall times at the end of an ac-terminated transmission line.



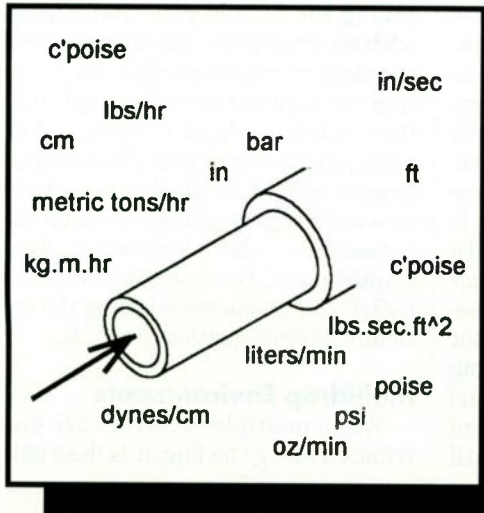
5. When the first reflection returns from the source, the signal will be reflected and return to the termination end.

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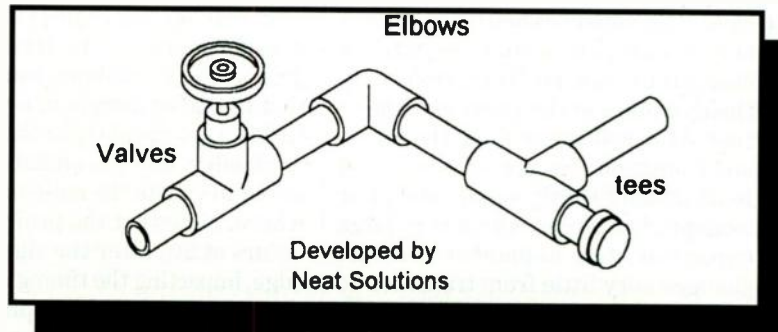
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that the result is in terms of the launched signal amplitude, V_m (not the open-circuit driver amplitude), and that the overshoot is measured with respect to V_m .

It's desirable to keep the overshoot low to prevent the forward biasing of semiconductor structures in components connected to the line. Moreover, having large overshoots indicates large reflections which could upset the signal integrity, creating an error in a clocked-in value. Additionally, large reflections will be present at a subsequent signal transition, disrupting the signal integrity associated with the signal's new state.

Solving for Z_0C gives the minimum capacitance value required to limit the overshoot to $V_{r_{max}}$ as shown in equation (9) in the sidebar.

Determine The Optimum Value

System designers also must consider the effect of reflections and the capacitor's charge state on subsequent signal transitions. When a new transition occurs, the capacitor will be charged to some level determined by the dynamics of the previous transition. Also, reflections from the previous transition may not have summed to an insignificantly small value. For example, in a circuit with a very large capacitor, the capacitor voltage changes very little from transition to transition. The capacitor will eventually charge to the signal's average level. Reflections will be negligible, and the voltage at the termination point will be ideal. However, the source generally isn't stiff and may have an internal impedance on the order of $10\ \Omega$ or more. For a $50\text{-}\Omega$ line, the signal amplitude will be $5/6$ of the open-circuit drive level or a little over 4 V p-p for a 5-V driver. A large termination capacitor will tend to charge to about 2.5 V (for a 50% duty cycle), and the signal swing at the line's termination end will be about 0.5 V to 4.5 V . The results are a reduced signal amplitude and a decrease in the logic 0 noise margin. These drops suggest a very large capacitor isn't suitable for practical source impedances. In addition, this situation makes these signals duty-cycle dependent. As the duty cycle changes, the average charge on the capacitor changes, resulting in a wandering baseline that reduces the noise

TABLE 1

R_S/Z_0	t_D/Z_0C
0.1	0.105
0.2	0.223
0.3	0.357
0.4	0.511
0.6	0.916

TABLE 2

R_S/Z_0	$Z_0C/t_D \text{ min.}$
0.1	2.05
0.2	1.80
0.3	1.55
0.4	1.35

margin to the input logic thresholds.

An overshoot may be desirable in some specific situations. Designers could use the overshoot to make up for amplitude loss due to the source impedance. Complete analysis of the entire transient may be required. Moreover, only specific regions in the signal waveform may be of interest. For example, the overshoot could ensure that the noise margin of a data line is within a set-up and hold time around a clock edge, and the signal may be allowed to violate the noise margin elsewhere. Note that the peak overshoot occurs at $2t_D$ after the signal's rising edge, impacting the timing budget and possibly limiting the applicability of this technique. One must wait until

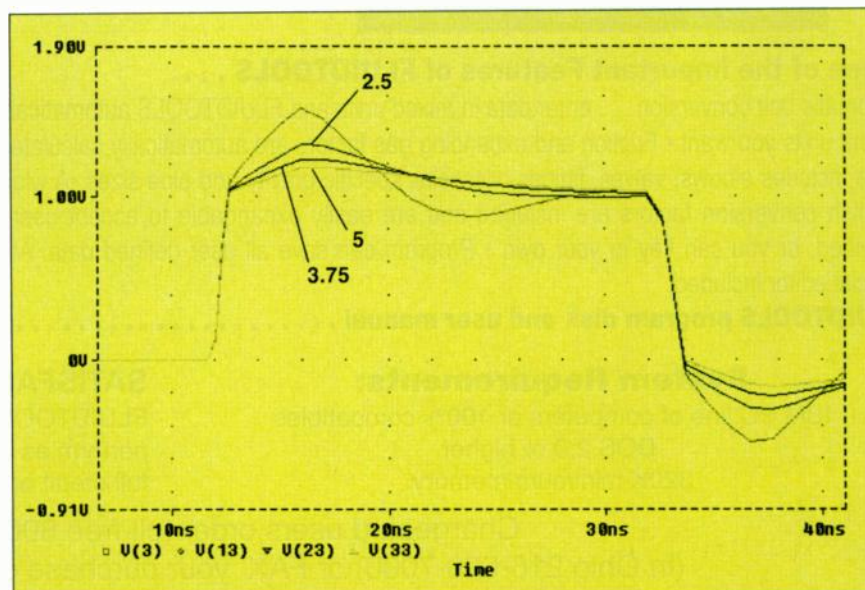
the overshoot brings the signal to the appropriate level, which could be as long as $2t_D$. Determining the maximum value of capacitance in all these cases requires simulation.

Edge-To-Edge Interaction

Meeting the criterion that the first overshoot peak reach the driver's open-circuit voltage (V_S) drives the termination to the steady-state voltage. If the driver were to maintain its state indefinitely, the capacitor would charge to V_S and all reflections would die away; there would be no current in the transmission line and the termination voltage would be at V_S . Designing such that the termination voltage reaches V_S is an optimum condition for reaching a quiescent state and for minimizing edge-to-edge interaction. This solution is a best-case scenario, giving the fastest rise time-signal with no overshoot. The analysis and simulation results confirm that setting the capacitance value such that the peak overshoot is equal to the open circuit driver provides an optimum solution for reducing noise margins and minimizing edge-to-edge interactions. By imposing this requirement, the minimum value of t_D/Z_0C can be calculated using the optimum design equation (Table 1).

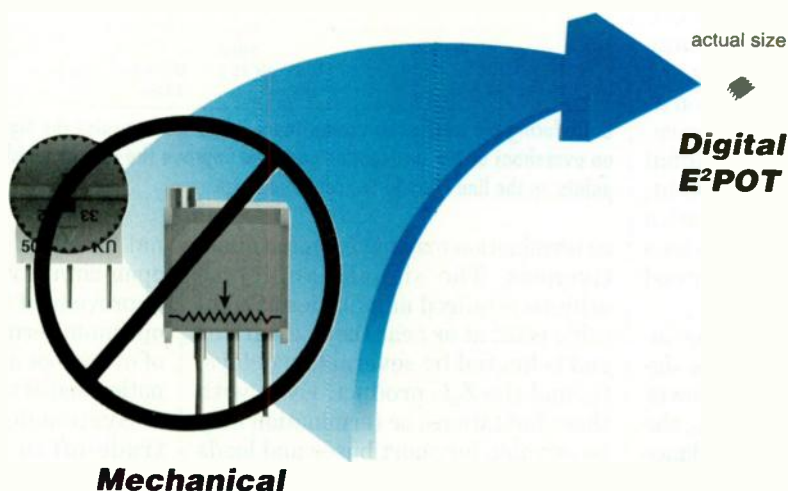
Multidrop Environments

When multiple receivers are distributed along the line, it is desirable



6. When $V_{r_{max}}$ is solved for various values of Z_0C , the result gives a comparison of the peak overshoot from the simulation versus the predicted values. In the plot, $V_0 = 0$ and $R_S = 0$.

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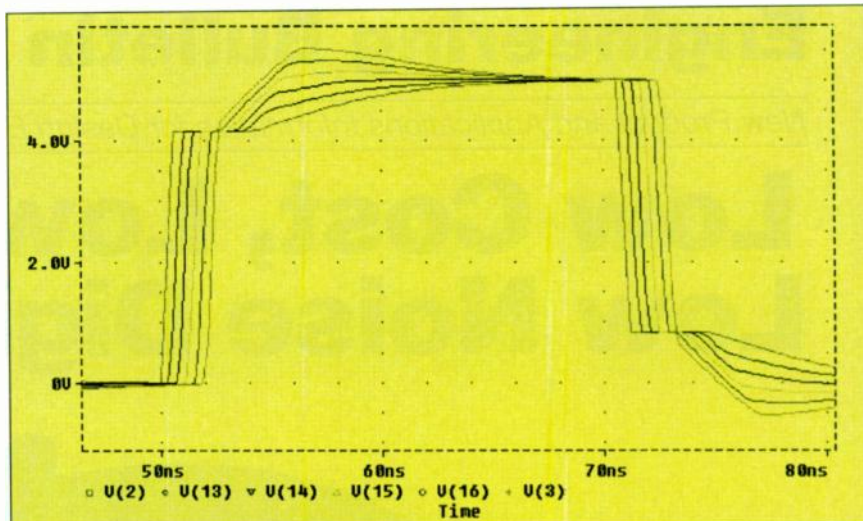
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to have signal integrity at each receiving point. With optimum termination and a 10- Ω source resistance, R_S , the curves show the signal at equally spaced points along the transmission line (Fig. 7).

The left-most curve at the rising edge is the signal at the driver, and the curves at successively later times are at positions along the transmission line from the source to the termination. Note, in particular, the first curve (driver end)—the signal rises rapidly to V_m and then rises to V_S only after many t_D times. Successive signals down the transmission line show incremental improvement reaching the optimum termination at the furthest point on the line. The results indicate that, while the signal overshoots are virtually nonexistent, the time it takes for a signal to reach a given level above V_m increases as a receiver moves toward the driver end of the line.

These simulations present three interesting results: as expected, the signal level is initially better with lower source impedance; after about $4t_D$, the signals under larger source impedance reach higher levels faster than signals under smaller source impedance; and all signals appear to monotonically increase to the driver's open circuit voltage. If a time constant is attributed to the rising curves, it is roughly Z_0C by empirical determination.

With multidrop receivers, depending on the signal level needed at a particular time after the signal transition,



8. Reducing the termination capacitance is one way to raise the signal levels (while accepting an overshoot at the termination end) and improve the rate at which the signal at the other points on the line rises to the required level.

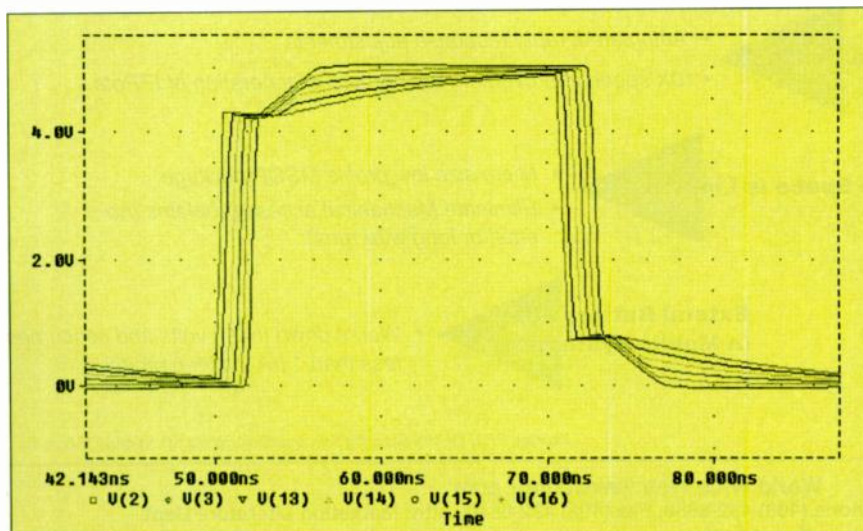
ac termination may have limited effectiveness. The signal's ability to achieve required amplitudes at a receive point at or near the line's driver end is limited by several line delays, t_D , and the Z_0C product. Even with these limitations, ac termination may be suitable for short buses and loads clustered toward the end of the line opposite the driver.

An approach to raising the signal levels, if required, is to reduce the termination capacitor value, accept an overshoot at the termination end, and improve the rate at which the signal at the other points on the line rise to the required level (Fig. 8). The receivers in about the last half of the bus see sig-

nal levels at or above the driver's open-circuit voltage within $3t_D$. This improvement is considerable over the optimum termination at the expense of overshoot at points near the termination end of the line.

System designers must make a trade-off in tolerating overshoot above the optimum design level (and some ringing) to ensure improved signal level toward the driver end. This technique also could impact the timing budget. Note that the time it takes a signal (at some given point along the line) to rise (or fall) to a given level could exceed the time it takes for the terminated signal to reach its peak. As a result, the clock edge would be required to be moved later in time to guarantee successful clocking-in of the signal. The situation improves as the driver source impedance decreases. This decrease allows the signal amplitude to reach the desired level without compromise, providing that a low enough impedance can be achieved in the driver. Since multiple reflections are involved, simulation is the best approach in selecting the optimum ac-termination capacitor value.

Even though the smaller source resistances improve the levels, the signal's apparent rise time at the line's driver end actually gets slower. If the source resistance must be so greatly increased as to require a series termination at the driver, and no termination at the opposite end of the transmission line, it's better to select



7. This simulation shows signals at multiple receive points along a line when employing the optimum termination and a 10-W source resistance

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EQUATIONS

$$\frac{t_D}{Z_0 C} = \ln\left(\frac{1-G}{-2G}\right) = \ln\left(\frac{Z_0}{Z_0 - R_s}\right) \quad (1)$$

$$C = \frac{t_D}{Z_0 \times \ln\left(\frac{Z_0}{Z_0 - R_s}\right)} \quad (2)$$

$$C = \frac{0.8\text{ns} \times 1000}{60\Omega \times \ln\left(\frac{60\Omega}{60\Omega - 10\Omega}\right)} = 73\text{pF} \quad (3)$$

$$V_m = V_s \frac{Z_0}{R_s + Z_0} = V_s \frac{1-G}{2} \quad (4)$$

$$V_{rl}(t) = -2Z_0 C \frac{V_m}{t_r} + V \frac{t}{t_r} + \left(\frac{V_0}{2} + 2Z_{0C} \frac{V_m}{t_r}\right) e^{\frac{-t}{2Z_0 C}} \quad (5)$$

$$V_{r2}(t) = V_m + \left(\frac{1}{2} V_{rl}(t_r) - V_m\right) e^{\frac{-t}{2Z_0 C}} \quad (6)$$

$$V_{ra}(t) = V_m + \left(\frac{1}{2} V_0 - V_m\right) e^{\frac{-t}{2Z_0 C}} \quad (7)$$

$$V_{r_{\max}}(t) = V_m + \left(\frac{1}{2} V_0 - V_m\right) e^{\frac{-2t_D}{2Z_0 C}} \quad (8)$$

$$Z_0 C = \frac{t_D}{\ln\left(\frac{V_m}{V_m V_{r_{\max}}}\right)} \quad (9)$$

$$V_b(t) = (1+2G)V_m - 2GV_m \frac{t}{2Z_0 C} e^{\frac{-t}{2Z_0 C}} - 2V_m \left(G + e^{\frac{-t}{2Z_0 C}}\right) \quad (10)$$

$$V_{cb}(2t_D) = 2V_s \left[1 - e^{\frac{-4t_D}{2Z_0 C}} + G \left(1 - e^{\frac{-2t_D}{2Z_0 C}} \right) - G \frac{2t_D}{2Z_0 C} e^{\frac{-2t_D}{2Z_0 C}} \right] \left(\frac{1-G}{2} \right) \quad (11)$$

another termination alternative.

When the termination is at the opposite end of the line from the driver, ac termination can be used in a single source, multidrop situation. Because the desired signal characteristics degrade as the receivers move from the termination end to the driver end, it's advantageous to have the receivers clustered near the termination end of the line. To achieve good signal characteristics at the receiver closest to the driver, the termination capacitance must be lowered to achieve acceptable signal levels within a given time from the signal edge. This design comes at the expense of overshoot at the termination end. Moreover, the section of the line with the clustered receivers will have a lower characteristic impedance than the unloaded section of the line between the driver and the first receiver. This technique requires that the line be designed for different unloaded impedance in these two line sections so that when loaded, the line impedance will be constant over the entire length.

Multiple Drivers On The Line

When multiple drivers or sources exist along the transmission line, it's appropriate to terminate both ends of the line. As indicated in the multidrop analysis, the optimum termination capacitance is determined by the line's propagation delay. However, as the source moves along the line, the optimum capacitance value changes, and the termination dynamics change as a result of the driver's position. No optimum solution exists for multiple driver configurations, only trade-offs, unless the line is short. Simulation is the simplest way to determine system performance (*Fig. 9*).

In the multidrop and multisource environments, it was observed that the signal amplitude near the driver took a longer time to rise to its final level than the signal at the termination end. If the initial amplitude of the signal is sufficient for the required noise margin, then the optimum design can be used. However, if this amplitude is not sufficient, the timing budget must be adjusted accordingly.

To minimize the adjustment, it may be desirable to let the signal at the termination end overshoot the

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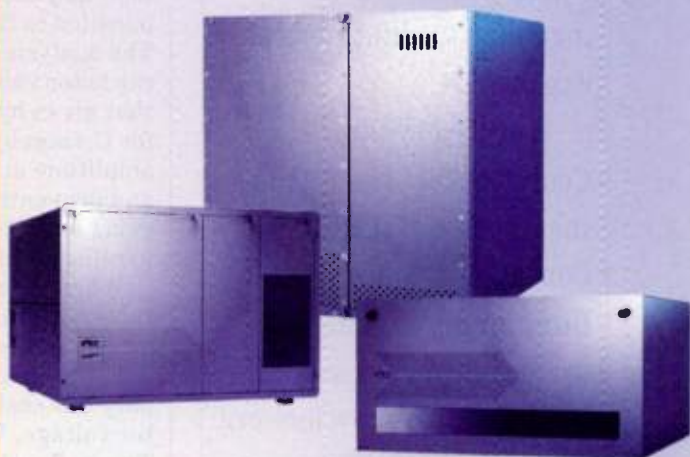
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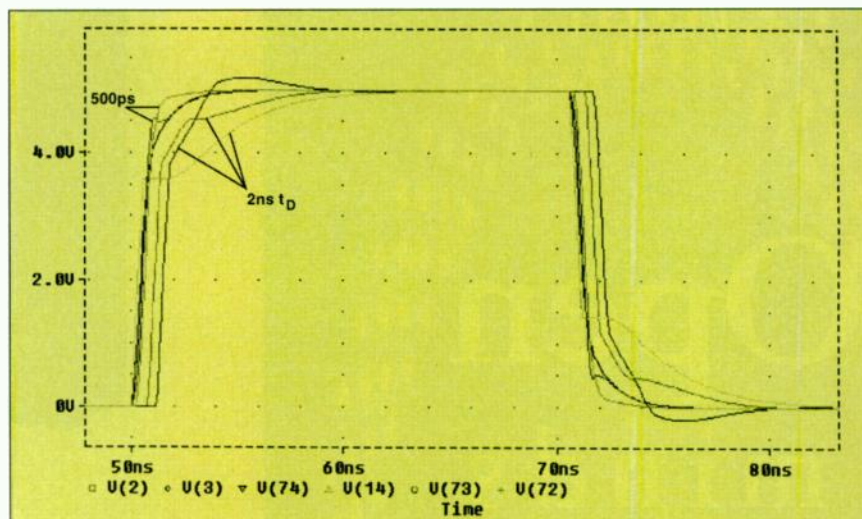


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9. In a multidriver environment with short lines, ac termination can be quite effective. In this example, the driver resistance is 10 Ω and the termination capacitors at each end of the line are adjusted to give the best results.

driver's open-circuit voltage so as to gain signal amplitude elsewhere.

Knowing that reducing the capacitor value increases the reflections, it's possible that subsequent reflections may cause the signal at the termination to fall below its final value. The analysis in this section seeks a capacitor value that is smaller than that given by the initial calculation for C , thereby increasing the signal amplitude at the multidrop points, and preventing undershoot (signal going lower than the final value due to reflections).

When the reflection returns from the source and arrives at the line's termination end, the charging conditions on the capacitor change. To simplify this analysis, the initial capacitor voltage, V_0 , is taken to be zero. The reflection returns from the source delayed by $2t_D$ and multiplied by the source reflection coefficient, G . The equation for the voltage at the termination (less the incident voltage, V_m) in the region after the reflection from the source arrives at the termination end ($t > 2t_D$) is shown in equation (10) in the sidebar.

In this equation, t is referenced to the beginning of this region. The results show that the overshoot voltage will decline toward the value $(1+2G)V_m$. With a large overshoot, the large reflection can return (inverted), and at some time in the future cause the signal to undershoot the desired value. This undershoot may occur at

any time following the initial overshoot peak. Though it's difficult to do a complete analysis, it's reasonable to suppose that if the capacitor voltage ever rises above V_S , the termination effect is reduced to the point that large amplitude reflections will continue. This result suggests that prolonged ringing can be suppressed if the capacitor voltage is not permitted to rise above V_S during Region b (Fig. 4, again). Examining the capacitor voltage in Region b, the voltage at the end of the validity of Region b ($t = 2t_D$) is defined by equation (11) in the sidebar.

This voltage is in terms of the open-circuit source voltage, V_S . By requiring that the capacitor voltage never rise above V_S (i.e., keeping the termination voltage from undershooting V_S), another criterion is set for determining the minimum value of the capacitor. If it's desirable to allow larger than optimum overshoots for multidrop situations, using this criterion will minimize undershooting the steady-state level at the termination end (Table 2).

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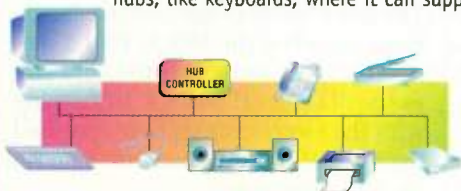
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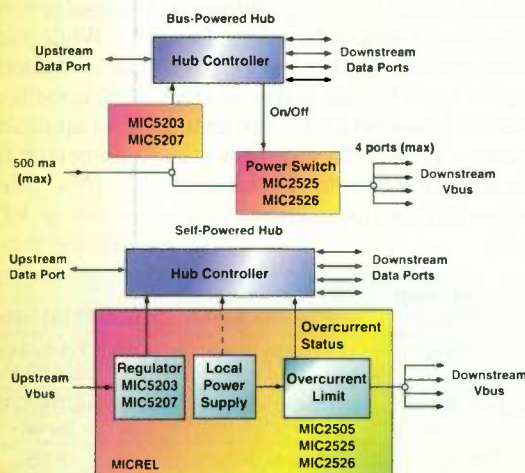
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Here Come The PCI Buses, Part II

In my July 21 column, I detailed seven of the 12 PCI spec that are in the semi-open domain. In this column, we'll look at the remaining five.

8. *IPCI (Industrial PCI)*—This specification comes from Europe, with most of the interest in Germany. The boards fit the 6U Eurocard format (233.35 by 160 mm), but they use a 2-mm METRAL connector, which is incompatible with the Z-Pack connectors used in CompactPCI. Like every other PCI board spec, they splatter the signal and ground pins in a different pattern. Word is that interest in this variant is waning, while interest in CompactPCI is gaining. We'll wait and see if the EEC comes out with some mandate that validates IPCI, but I doubt it will survive.

9. *Conduction-Cooled PMC (CCPMC)*—This spec defines a conduction-cooled version of the original PMC mezzanine card for use by the military. The board has "stiffeners" to eliminate warping, and thermal-conduction areas where heat is removed by physically connecting the card to a heat-sinking surface.

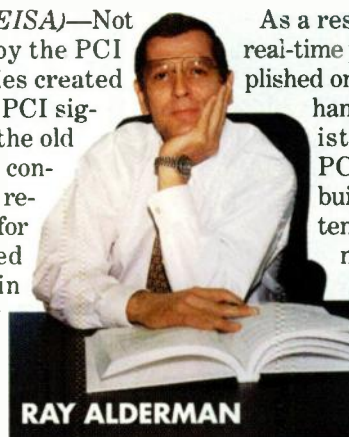
All computers (including the desktop) will have to adopt some kind of conduction-cooling method. With the latest processor chips dissipating 30 W or more, and with huge DRAM footprints generating enough heat to cook a frozen pizza, there's no way that forced-air cooling can remove the heat from the box without sounding like a wind tunnel. There's always liquid cooling, but that just turns computer designers into plumbers, and the cost is still too high. Of all the challenges in computer designs today, thermal management is the most pressing, and CCPMC is one solution. The CCPMC spec is controlled by VITA and is being constructed by the VSO (VITA Standards Organization), an ANSI-accredited standards developer.

10. *PISA (PCI and EISA)*—Not to be overshadowed by the PCI frenzy, a few companies created PISA, which puts the PCI signals and protocols on the old EISA form factor and connector. While ISA was released in the early 80's for PCs, EISA (Extended ISA) was released in 1987 and supported by only a few companies. This is another vertically inserted desktop board that uses a high-density, card-edge connector.

11. *IEEE P1996 HiRel PCI*—With so many PCI mechanical specs being constructed, and all the other adjunct standards for bridging and live insertion under development, a few companies decided to roll all this chaos into one document called High Reliability PCI. The board size is in hard-metric dimensions based on the IEEE 1301.1 mechanical specs, or roughly the same size as the 3U and 6U boards. In keeping with the metric purity, they specified the 2-mm METRAL connector found in the 1301.1 document.

These cards aren't compatible with any other PCI variant mentioned here due to the pure hard-metric board dimensions, and their unique signal pattern on the connector. What's being done in P1996 also is being done with CompactPCI, except for the mechanicals, the connector, and the pinout.

12. *P2CI*—Because PCI is a non-deterministic bus, it creates problems in many hard-real-time applications. Several companies decided to add PCI as a sub-bus to the VMEbus and retain the determinism needed for sophisticated applications. This specification places the signals on the P-2 five-row DIN connector on the VME cards and replaces the old VSB.



RAY ALDERMAN

As a result, you have the hard real-time processing being accomplished on the VMEbus, and PCI handling the nondeterministic peripherals on the PCI sub-bus. Computers built in this manner are often called "hybrids." To remove bottlenecks and improve processing power, hybrid architectures have been used in mainframes and minicomputers for years. Now, many

desktop computers apply this concept when you consider AGP as a graphical sub-bus to PCI. This specification is being handled by VITA under the VSO.

For every one of the specs mentioned, there's at least one proprietary version being done by companies trying to protect their margins and create customer loyalty in a commodity market. Industrial-control manufacturers don't want users buying cheap I/O cards from third-party board shops. And, the telcos don't want you buying cheap line cards and putting them in their PBX equipment.

PCI chip life-cycles are measured in months, typically 15. Often, when one chip goes away, the replacement chip is a totally different animal. The registers can be in different places, and the bits are in different positions. Since all of these variants use the same API and the same chips, the problem is universal across all implementations.

While you may think I'm not too enthused about the PCI architecture, it is a good technology for certain low-end applications. But I wouldn't recommend it for sophisticated tasks.

Ray Alderman is the Executive Director of VITA. He can be reached at exec@vita.com.

	Industrial PCI (IPCI)	Conduction-Cooled PMC (CCPMC)	PISA (PCI & ISA)	IEEE P1996 HiRel PCI	P2CI Sub-bus on VME
Board size	6U: 233.35 by 160 mm	74 by 143.75 mm	12.3 by 3.9 in.	6SU: 115 by 213 mm 12SU: 255 by 213 mm	6U: 233.35 by 160 mm
Connector	2-mm METRAL: pin and socket	1-mm pin & socket	0.050-in. edgecard	2-mm METRAL: Pin and socket	0.1-in. 60-pin DIN
Spec owner	SIPS	VITA	unknown	IEEE	VITA
URL	www.sips.com	www.vita.com	www.pcisig.com	www.ieee.org	www.vita.com

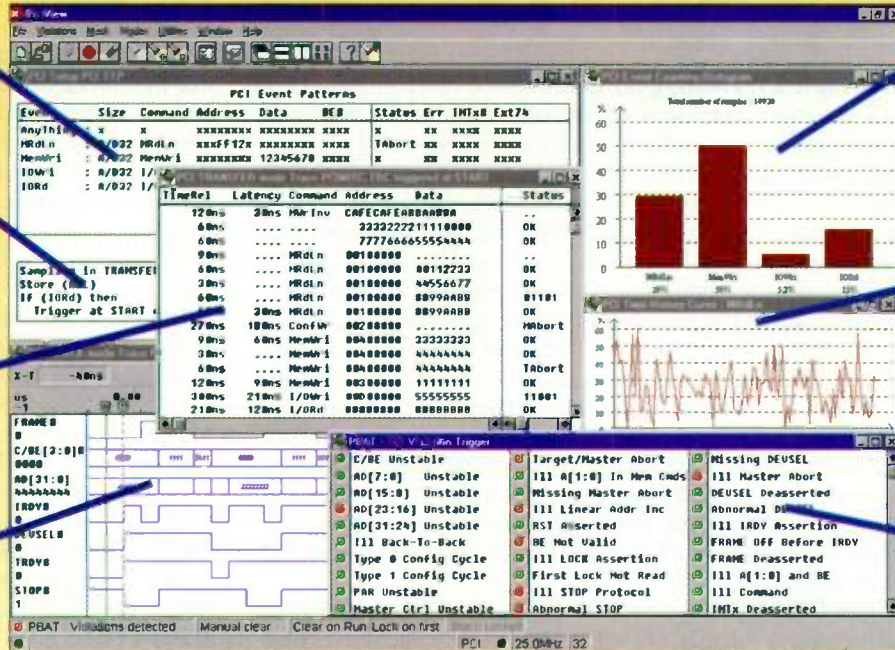
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WHAT'S ON BOARD

Able to handle data rates up to 3.125 Mbits/s, the OX16C952 dual-channel UART and parallel port lets designers increase serial transfer speed while maintaining 100% software compatibility with all PC UARTs. The 68-lead PLCC provides pin compatibility with the TI TL16C522 UART. The chip, developed by Oxford Semiconductor Ltd., Abingdon, Oxon, U.K., can be used in PC add-in cards, high-speed modems, ISDN terminal adapters, laser printers, and other equipment requiring high serial bandwidth. Both serial channels can be programmed for any one of 64 possible baud rates, and each can sustain the 3-Mbit/s maximum transfer rate. Each channel includes 128-byte-deep FIFO registers on the transmit and receive ports to buffer incoming and outgoing data, thus allowing data to transfer while the rest of the chip is preparing the next block of data. The on-chip IEEE 1284-enhanced parallel-port interface gives system designers a Centronics-compatible port for printers or other parallel data transfers. The serial ports are IrDA-compliant and the chip has a low-power sleep mode. The UART blocks can be treated as intellectual property to implement custom serial controllers. In large volumes, the OX16C952 sells for \$5. Contact James Lewis at (44) (0) 1235-86141 or on the web at <http://www.oxsemi.com>.

Designers using HC-type CMOS logic have benefited from a high-performance family called AHC for over a year. However, offerings only included chips with 8-bit bus widths. The Widebus family from Texas Instruments (TI), Sherman, Texas, includes a collection of 16-bit-wide bus interface circuits that reduce chip counts, power consumption, and board area. With multiple power and ground pins on the packages, the chips lower system noise by about 20% vs. HCMOS devices. The family's basic part number is SN74AHC16xxx, with the xxx referring to the specific interface type—latches, registers, buffers, inverting buffers, and so on. There are three specialized logic families—the GTL 1655 that includes a universal bus transceiver for high-drive backplanes; the SSTL16837, a bus driver for synchronous DRAMs that implements the stub series-terminated logic interface; and the CBLTV family of 3.3-V digitally controlled bus switches. The GTL1655 handles drive currents of 100 mA and uses Gunning-transceiver logic (GTL) signaling levels to provide switching speeds up to 160 MHz and propagation delays of 5 ns. The SSTL16837 can drive 3.3-V address signals from a low-voltage memory controller to SDRAMs with bus speeds over 75 MHz. Prices are \$7.50 apiece for the GTL1655, \$6.24 each for the SSTL16837, and from \$0.50 to \$1.75 each for the CBLTV switches, depending on configuration. Widebus devices range from \$0.55 to \$0.65 each in 1000-unit lots. Samples are available from stock. Contact TI at (800) 477-8924 or on the web at <http://www.ti.com>.

The C500 family of standard 8-bit 80C52-compatible microcontrollers now offers USB support. The first two products in the line are the C540U and the C541U. The C540U has 4 kbytes, while the C541U has 8 kbytes plus a synchronous serial interface and a programmable watchdog timer. Two transfer speeds are available—1.5 and 12 Mbits/s. The higher speed is used for voice and video applications, while the lower speed can be used for game controllers, pointing devices, keyboards, and so on. Adding USB support makes the microcontrollers suitable for telecommunications, computer peripheral, and consumer applications. The optimized memory management and mode speeds suits them for computer-telephony integration products. The chips' protocol supports four transfer types—control, interrupt, bulk, and isochronous. Control reads the information in the descriptors contained in device registers. Isochronous transfers are needed for telecommunications devices to guarantee a constant transfer rate. Both parts are sampling now. In 100,000-unit lots, the C540U sells for \$3; the C541U costs \$3.50. Contact Siemens at (408) 777-4500, or visit their web site at <http://www.sci.siemens.com>.

19-In. Monitor Carries
17-In. Price Tag

The viewable area of the V95 PC monitor measures 18 in. (it's specified as a 19-in. monitor), while the cost is comparable to a 17-in. display. Suitable for such tasks as graphics design, imaging, and web applications, the monitor features a 0.26-mm dot pitch (0.22-mm horizontal by 0.14-mm vertical) to produce clear images, even at the maximum resolution of 1600 by 1280 pixels. It also delivers a refresh rate of 88 Hz at a resolution of 1280 by 1024 pixels for flicker-free viewing on PCs and Macintoshes. An Invar shadow mask employs a special alloy that withstands high heat levels to extend the CRT's life without degrading image quality. On-screen menus simplify the adjustment of image quality, size, position, and geometry. The V95 exceeds MPR-II and EPA Energy Star requirements and meets the Swedish TCO standard for reducing heat emissions and power consumption. The monitor should sell for \$995.

Optiquet Corp., Walnut, CA; (800) 843-6784 or (909) 869-7976; <http://www.optiquet.com>.

CIRCLE 500

Modem Utilizes The
Power Of The Processor

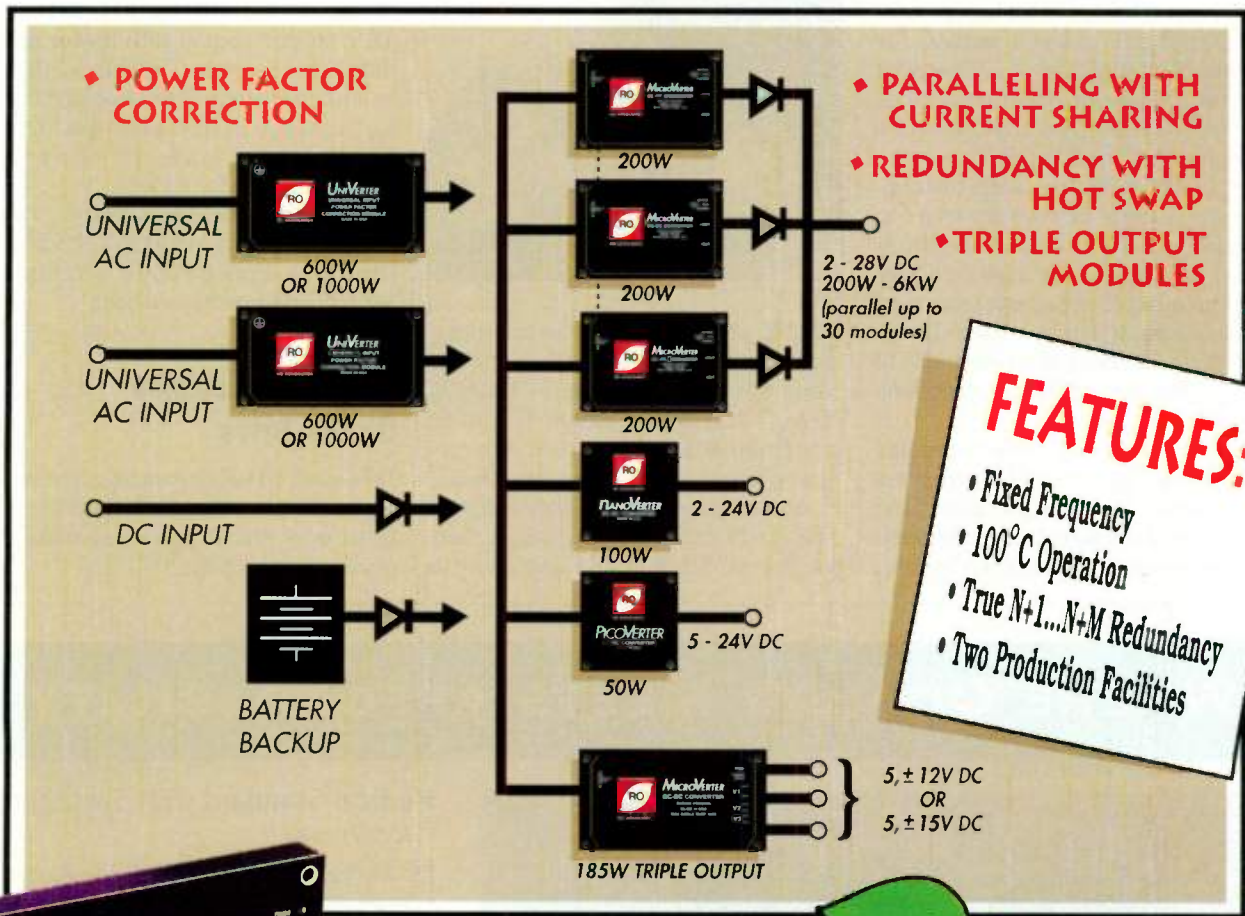
With the increasing speeds of today's microprocessors, it makes sense to employ some of that power for communications. For this reason, Motorola's Information Systems Group has developed a software-based 56-kbit/s modem. Because its brains come from the host CPU, it can be manufactured at a lower cost than traditional modems. The modem also is easier to upgrade and requires less components. As a result, the software modem is suited for portable applications. Motorola's version of the software modem is compatible with the K56flex technology that's backed by Rockwell International and Lucent Technologies. The technology allows for a 56-kbit/s download speed and a 33.6-kbit/s upload speed.

Motorola Information Systems Group, 50 E. Commerce Dr., Schaumburg, IL 60173; (508) 261-4756; <http://www.mot.com/isg>.

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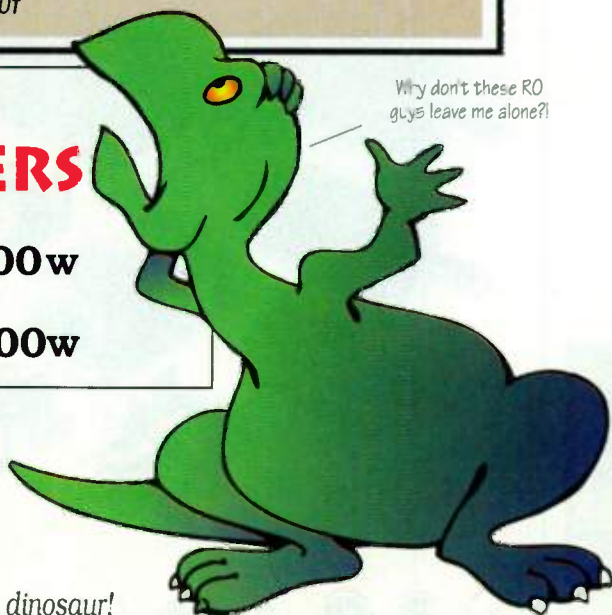
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READER SERVICE 92

Mouse Controller Addresses Touchpad Applications

Thanks to the TR88L811 from TriTech Microelectronics, there's more than one way to move a mouse. The touchpad and mouse controller offers a solid-state alternative to the common mechanical mouse, with a highly integrated solution that's suited for portable computing devices. Designed for resistive touchpad technology, the controller also offers an advantage over conventional capacitive-type touchpad input devices, with the ability to use a finger for cursor control or a plastic pen stylus to capture handwriting or graphics. As a result, a user can type a letter using the touchpad mouse to initiate normal menu-driven commands, then switch to pen mode to add a signature or annotate sections for emphasis.

The TR88L811 controller contains all of the circuitry needed to drive a four-wire resistive touchpad, detect and digitize the touch coordinates, filter extraneous noise, and output serial data.

Users can choose either MS Mouse format or "absolute coordinate" mode (for graphical capture). In MS Mouse mode, the controller operates with standard MS Mouse drivers. The chip has input pins for mechanical mouse buttons, but also can internally translate a "tap" or



"double-tap" on the pad into the corresponding "click" and "double-click" actions of a standard mouse button. "Drag" action also can be initiated though either a double tap and slide motion on the pad or with the conventional mechanical button. In addition, the TR88L811 implements an "Auto Cursor Motion" function, allowing a user to

extend a move or drag operation over long distances across the PC display.

The TR88L811 also is suited for CRT and LCD touchscreen overlays as well as PDAs and electronic organizers. It operates from a 3.3-V supply and draws only 2 mA when active. An automatic power-down mode is initiated reducing current to less than 2 μ A if there's no pad activity for more than three seconds. The chip, available in a plastic surface-mount package, costs \$3 each in 1000-piece quantities. An evaluation system with a touchpad is available for \$250.

TriTech Microelectronics Inc., 1440 McCandless Dr., Milpitas, CA 95035; (888) 253-8900; Internet: <http://www.tritechmicro.com>.

CIRCLE 605

DVD, CD-R Combine On One Drive

DVD and CD-R drives are gaining in popularity, but they both tend to go in their opposite directions, meaning

(continued on page 156)

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(continued from page 154)

that there's little compatibility between the two. Now, thanks to the SDR-130 from Samsung, CD-R, DVD-Video, DVD-ROM, CD-ROM, and CD disks all can be employed in the same drive. The drives ship with the hard-



ware to handle MPEG-2 video and AC-3 audio. The drives' specifications include a 220-ms access time for DVD-ROM (150 ms for CD-ROM) and transfer rates of 1.35 Mbytes/s for DVD-ROM and 1.2 Mbytes/s for CD-ROM. The performance is bolstered by a 512-kbyte memory buffer. For CD-R disks, the drives feature a specially designed one-lens, two-laser system. The drives can be mounted either hori-

zontally or vertically. User controls include volume, eject, quick play, advance, and an LED indicator. Bundled drivers support MS-DOS, Windows 3.1, Windows 95, Windows NT, and OS/2.

Samsung Electronics America Inc.,
105 Challenger Rd., Ridgefield Park,
NJ 07660; (201) 229-4000; Internet:
<http://www.sosimple.com>.

CIRCLE 606

Kit Allows Users To Videoconference Over The 'Net

All the tools a user needs to have live videoconferencing sessions are contained in the HOW-R-U Internet and direct home videoconferencing kit. The kit consists of a PCI-based full-motion video-capture card, the Desktop Color Camera from Phillips, and VDOPhone videoconferencing software from VDONet. The fully integrated solution works with an existing PCI card to provide high quality videoconferencing services either over the Internet or on a direct-dial

basis. The C210 PCI video-capture card supports both full-motion video and still-image capture, and generates full-screen (640- by 480-pixel resolution) or window-sized live video. It provides two composite video inputs, one S-Video input, and supports NTSC, PAL, and SECAM video standards. The C210 also features true plug-and-play performance and ships with an easy-to-use video capture utility, a TWAIN driver, and a full-motion video capture and playback utility. The supplied camera is a lightweight, digital camera that displays 24-bit true-color images and incorporates contrast and back-light compensation to maintain correct light exposure. The required board that's not supplied is a SVGA video card with hardware assisted video playback acceleration. Available now, the HOW-R-U videoconferencing kit sells for \$300.

**Tekram Technology, 46712 Fremont
Blvd., Fremont, CA. 94538; (510) 353-
6099; <http://www.tekram.com>.**

CIRCLE 607

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According to ITAC Systems, the Mouse-Trak is more than just a mouse. Its streamlined, ergonomic design has comfortable molded contours that improve on ease-of-use and comfort. Aimed at PCs and workstations, the input device requires very little desktop space (it's half the size of a traditional mouse pad). Its intuitively located keys offer tactile guide features to help distinguish them. The keys are preprogrammed to perform common functions, including primary click, primary double click, primary drag, auxiliary click, and right click. No special drivers are required to run the Mouse-Trak. However, users can reprogram the mouse from the keypad, either for left-handed use or to reassign functions from one key to another. The mouse is built with ruggedized bearings, shafts, and a hardened phenolic ball. Available now, the Mouse-Trak is priced at \$199.

ITAC Systems Inc., 3113 Benton St.,

Garland, TX 75042; (800) 533-4822 or (972) 494-3073; Internet: <http://www.mousetrak.com>. CIRCLE 608

Low-Cost 8-Bit Gray-Scale Scanner Adds File Compression

Incorporating a file-compression capability, the RT-9600W keyboard-scanner works within networked systems where shared memory resources often limit the size of image files. The software's 8-bit gray scale and 100- to 400-dot/in. resolution enable any printer to be employed as a copy machine by scanning documents ranging in size from business cards to 30-in. newspaper columns. It also operates with most fax applications. The RT-9600W's annotation and page control features lets users rotate, flip, trim, cut, crop, and copy text, or add highlights, sticky notes, freehand drawings, lines, and arrows. Scan time for a typical document is less than six seconds, and preset scan modes for articles, letters, business cards, and photos help reduce errors and ensure high-quality results. The bundled optical-character-

recognition software turns scanned documents into editable text, ready for use with most word processings. The RT-9600W is priced at \$127.

NMB Technologies Inc., 9730 Independence Ave., Chatsworth, CA 91311; (800) 662-8321; Internet: <http://www.nmbtech.com>. CIRCLE 609

Controller Board Upgrades IDE To Ultra ATA

The CSA-6460U PCI-to-IDE controller board helps upgrade motherboards to the high performance and reliability of Ultra ATA. According to the board's designers, it results in a 14% performance increase over traditionally enhanced IDE (EIDE) controllers. The board is based on CMD's PCI0646U standalone Ultra ATA controller ASIC. This controller implements all the functionality of the Ultra ATA standard, which effectively doubles the speed of the disk-drive interface while maintaining backward compatibility with existing EIDE hard drives and software. UI- (continued on page 160)



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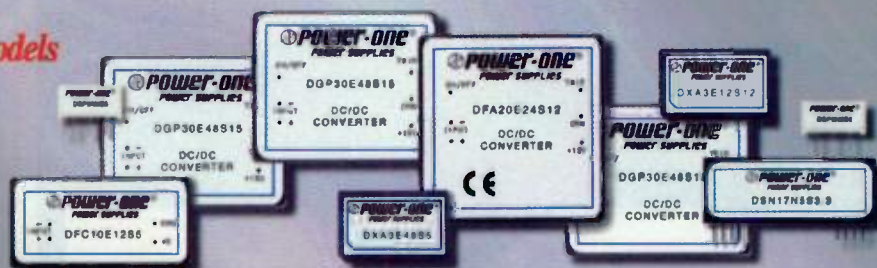
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(continued from page 158)

tra ATA drivers are bundled for most popular operating systems. The drivers identify all connected IDE devices and fine tune the PCI0646U's data-transfer parameters to extract the maximum performance from each connected device. Full CRC data protection increases the integrity of transfers across the interface. The CSA-6460U controller is also compliant with the latest PC97 specifications and is PCI version 2.1 compliant. Available immediately, it sells for \$59 each in quantities of 1000.

CMD Technology Inc., 1 Vanderbilt, Irvine, CA 92618; (714) 454-0800; <http://www.cmd.com>. **CIRCLE 610**

Low-Cost Digital Camera Doesn't Skimp On Features

One technology that's quickly gaining popularity is the digital camera. Not only is the quality of the camera increasing, but the prices are falling rapidly. One example is the RDC-300, a digital camera that can connect to a



television or a PC, or it can operate as a standalone unit with its built-in 1.8-in. color LCD. The camera employs square-pixel technology on its 350,000-pixel CCD. Other features include a 38-mm auto-focus lens; 640- by 480-pixel, 24-bit resolution; and 4 Mbytes of flash memory that can store up to 100 images in a standard JPEG format. The camera comes bundled with a remote-control IR sensor, an automatic or manual flash, exposure compensation, and a timer. An ac adapter is available as an option. Weighing just 225 g, the RDC-300 measures 125.8 by 34 by 72.6 mm. It runs on four AA batteries. PhotoStudio software is included with the camera, which lets users manage and manipulate images on a PC or Macintosh. The PDC-300 digital camera sells for \$450.

Ricoh Consumer Products Group, 475 Lillard Dr., Sparks, NV 89434; (800) 225-1899; Internet: <http://www.ricohcpg.com>. **CIRCLE 611**

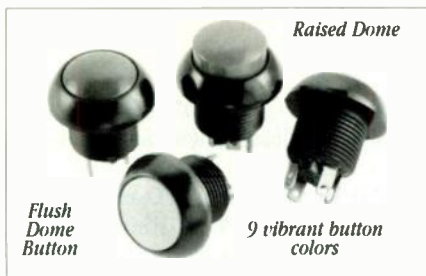


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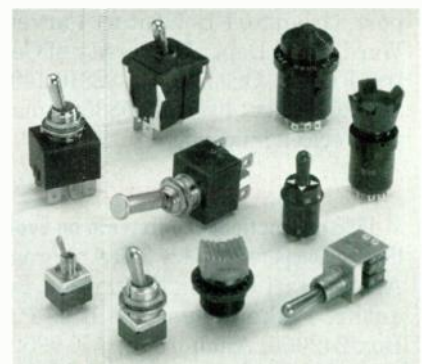


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FEBRUARY 1998

IEEE International Solid-State Circuits Conference (ISSCC '98), Feb. 5-7. San Francisco Marriott, San Francisco, CA. Contact Diane Suiters, Courtesy Associates, 655 15th St. N.W., Washington, DC 20005; (202) 639-4255; fax (202) 347-6109; e-mail: isscc@courtesyassoc.com.

IEEE Applied Power Electronics Conference and Exposition (APEC '98), February 15-19. The Disneyland Hotel, Anaheim, California. Contact Pamela Wagner, Courtesy Associates, 655 15th St., N.W., Suite 300, Washington, DC 20005; (202) 639-4990; fax (202) 347-6109; e-mail: pwagner@courtesyassoc.com.

38th Israel Conference on Aerospace Sciences, Feb. 25-26. Tel-Aviv & Haifa. Contact Technion-Israel Institute of Technology, Haifa 32000, Israel; 972-4-8292713; fax, 972-4-8231848; e-mail: alic@aerodyne.technion.ac.il.

MARCH 1998

Sixth Annual Embbedded Systems Conference East, Mar. 31-Apr. 2. Chicago's Navy Pier Festival Hall, Chicago, IL. Contact Miller Freeman Inc., 600 Harrison Street, San Francisco, California 94107; (415) 905-2354; fax (415) 905-2220; Internet: <http://www.embedsyscon.com/>.

APRIL 1998

Southeastcon '98, Apr. 10-15. Hyatt Regency, Orlando International Airport, Orlando, FL. Contact Parveen Ward, ECE Dept., University of Central Florida, Orlando, FL 32816; (407) 823-2610; fax (407) 823-5835; e-mail: pfw@ece.engr.ucf.edu.

MAY 1998

IEEE International Conference on Evolutionary Computation, May 3-9. Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@akaska.net.

IEEE International Conference on Neural Networks (ICNN '98), May 3-9. Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK

99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@akaska.net.

IEEE World Congress on Computational Intelligence, May 3-9. William A. Egan Civic and Convention Center, Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc. P.O. Box 242064, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

Seventh IEEE International Fuzzy Systems Conference, May 3-9. Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

IEEE/IAS Industrial & Commercial Power Systems Technical Conference (I&CPS), May 4-7. Edmonton, Alberta, Canada. Contact Marty Bince, Modicon Canada Ltd., 5803 86th St., Edmonton, Alberta T6E 2X4, Canada; (403) 468-6673; fax (403) 468-2925.

IEEE International Conference on Acoustics, Speech & Signal Processing (ICASSP '98), May 12-15. Seattle Convention Center, Seattle, WA. Contact Les E. Atlas, Dept. EE(FT 10), University of Washington, Seattle, WA 98195; (206) 685-1315; fax (206) 543-3842; e-mail: atlas@ee.washington.edu.

JUNE 1998

IEEE/MTT-S International Microwave Symposium (MTT 98), June 7-12. Baltimore Convention Center, Baltimore, MD. Contact Steven Stitzer, Westinghouse Electric Corp., P.O. Box 1521, MS 3T15, Baltimore, MD 21203; (410) 765-7348; fax (410) 993-7747.

USENIX 1998 Technical Conference, June 13-17. Marriott Hotel, New Orleans, LA. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, California 92630; (714) 588-8649; (714) 588-9706; e-mail: conference@usenix.org; Internet: <http://www.usenix.org>.

JULY 1998

IEEE International Geoscience & Remote Sensing Symposium (IGARSS '98), July 6-10. Sheraton Seattle, WA. Contact Tammy I. Stein, IGARSS Business Office, 2610 Lakeway Dr., Seabrook, TX 77586-1587,

(281) 291-9222; fax (281) 291-9224; e-mail: tstein@phoenix.net.

IEEE Power Engineering Society Summer Meeting, July 11-17. Sheraton Hotel, San Diego, CA. Contact Terry Snow, San Diego Gas & Electric, P.O. Box 1831, San Diego, CA 92112; (619) 696-2780; fax (619) 699-5096.

IEEE Power Engineering Society Summer Meeting, July 12-16. Sheraton San Diego Hotel & Marina, San Diego, CA. Contact Terry Snow, San Diego Gas & Electric, P.O. Box 1831, San Diego, CA 92112; (619) 696-2780; fax (619) 699-5096; e-mail: t.snow@ieee.org.

SPIE's Annual Meeting & Optical Instrumentation Show, July 19-24. San Diego, CA. Contact SPIE Exhibits Dept., P.O. Box 10, Bellingham, WA 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

IEEE Nuclear & Space Radiation Effects Conference (NSREC '98), July 20-24. Newport Beach, CA. Contact Jim Schwank, Sandia National Laboratories, P.O. Box 5800, MS-1083, Albuquerque, NM 87185-1083; (505) 844-8376; fax (505) 844-2991; e-mail: schwanjr@sandia.gov.

AUGUST 1998

AUTOTESTCON '98, Aug. 24-27. Salt Palace Convention Center, Salt Lake City, UT. Contact Robert Myers, Myers/Smith Inc., 3685 Motor Ave., Suite 240, Los Angeles, CA 90034; (310) 287-1463; fax (310) 287-1851; e-mail: bob.myers@ieee.org.

OCTOBER 1998

IEEE International Conference on Systems, Man, & Cybernetics, Oct. 12-14. Hyatt Regency La Jolla, La Jolla, CA. Contact M.A. Jafari, Dept. of Industrial Engineering, Rutgers University, P.O. Box 909, Piscataway, NJ 08855; (908) 445-3627; (908) 445-5467; e-mail: jafari@gandalf.rutgers.edu.

NOVEMBER 1998

Photonics East & Electronic Imaging International Exhibition, Nov. 1-6. Boston, MA. Contact SPIE Exhibits Dept., P.O. Box 10, Bellingham, WA 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

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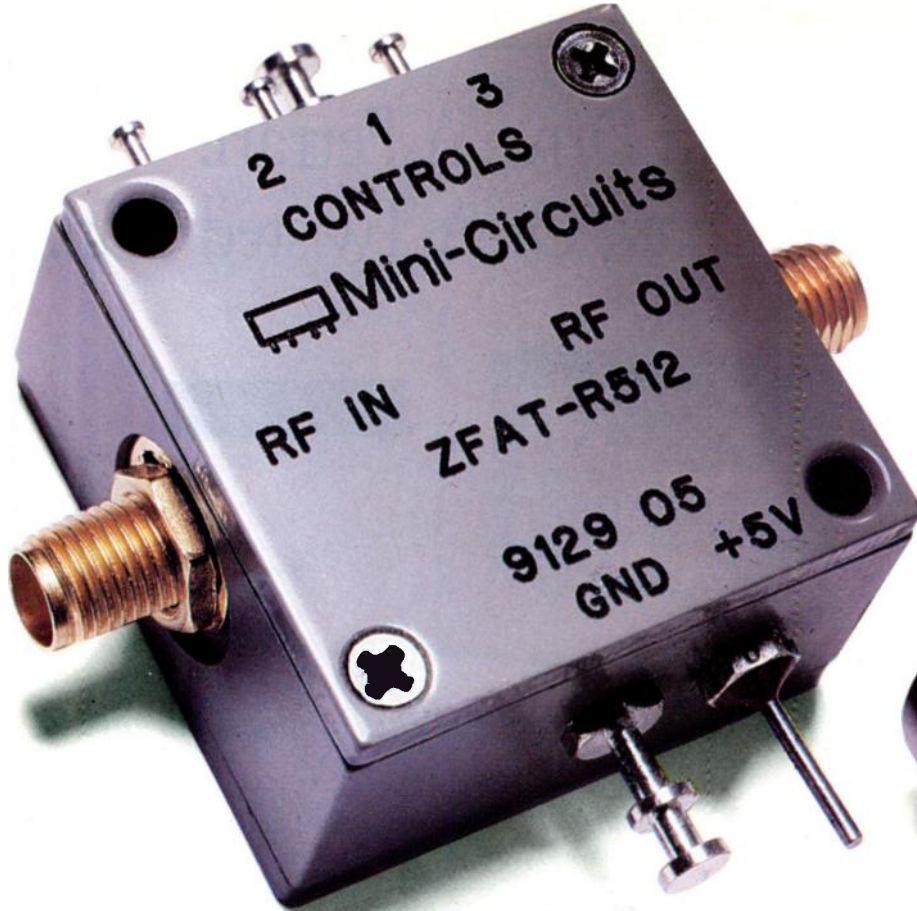
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2.5 0.32	5.0 0.5	13.0 0.6	20.0 0.8	25.0 0.7
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Circle 520

Circuit Allows Any 8051 Microcontroller To Speak IrDA

JOHN WETTROTH

Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086; (408) 737-7600.

With the circuit design described here, any derivative of the 8051 microcontroller can communicate using the serial-infrared (SIR) format established by the Infrared Data Association (IrDA). Communication is a two-stage process in which the microcontroller first transmits via a "bit-banged" SPI serial interface to a tiny UART (IC1). The UART then formats the message in IrDA mode.

Note that the UART included in many 8051 derivatives isn't IrDA-compatible, and can't easily be made as such. The circuit shown, however, can easily be added to an existing 8051 system with a minimum of cost, power, and software overhead.

IC1 includes an IrDA timing mode in addition to the conventional UART timing modes (see the figure). It's capable of 115 kbaud, but in this case the optical components shown limit the data rate to 4800 baud. The components are inexpensive, though, and most IrDA devices support data rates as low as 2400 baud. If necessary, the maximum 115 kbaud is easily attainable with high-quality optical components such as the HP-1000 IrDA module. Most IR LEDs and photodiodes are acceptable for this application, but to avoid being swamped by visible light, the photodiode should include a filter. If necessary, you can place an external ambient-light filter in front of an unfiltered photodiode.

The operating voltage can range from 2.7 V to 6 V, subject to limitations imposed by the 8051. Power-supply current is about 1 mA for IC1, plus 1 mA per megahertz for most variants of the 8051. Timing for the SPI interface isn't critical. The UART performs all real-time processing, so the processor clock can have any reasonable frequency. Unlike most system clocks, this one doesn't require time and temperature stability.

In the MAX3100-8051 driver code,

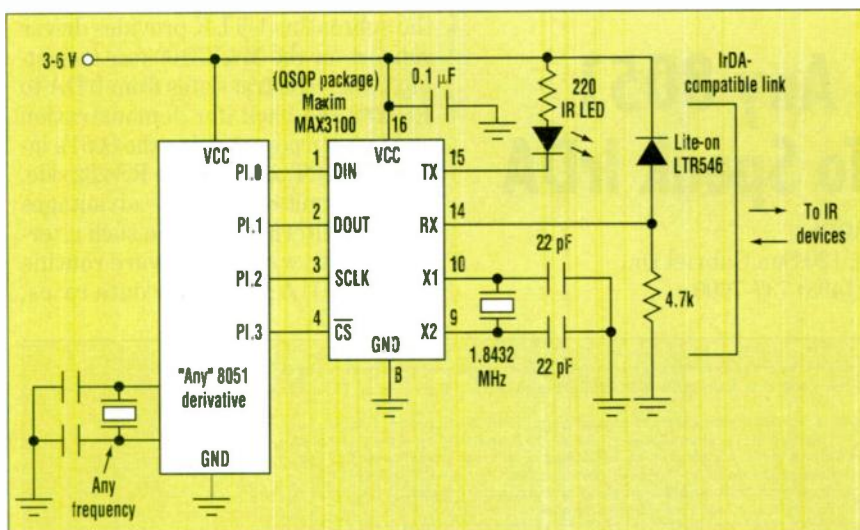
the subroutine UTLK provides driver support for the MAX3100 (see the listing). This code translates from IrDA to RS-232 and back (for demonstration and test purposes), using the 8051's internal UART to talk on the RS-232 side.

The circuit offers other advantages over the alternatives. One such alternative is to write a software routine for IrDA UARTs at low data rates,

```

;*****
;IrDA CODE FOR MAX-3100 UART-8051 based
;*****
;MAX-3100 UART demonstration and test code for the 8051 that
;bidirectionally translates IrDA to 232 and 232 to IrDA. Both the
;8051 and IrDA sides run at 9600 baud. All receivers are polled
;to keep code easy to follow. Testing was done with an HP-100
;Palmtop for IrDA and PC running a terminal program. The primary
;purpose of the code is to demonstrate the UART.
;*****
;CONSTANTS
PCON EQU 87H
;PORT PIN DEFINITIONS-BIT BANGING IP
DOUT BIT P1.0 ;data out (from uart)
DIN BIT P1.1 ;data in (from UART)
SCLK BIT P1.2 ;serial clock
CS BIT P1.3 ;chip select-act low
IRQ BIT P3.2 ;(irq) polled in this code
;RAM LOCATIONS
TX1 EQU 10H ;transmit regs
TX2 EQU 11H
RX1 EQU 12H ;receive regs
RX2 EQU 13H
;*****
ORG 0H
BEGIN:MOV SP,#70H ;initialize stack
CLR SCLK ;clear sclk-normally low
;initialize 8051 internal uart
MOV TMOD,#20H ;t1 baud
MOV TH1,#253 ;reload value baud 9600/xtal 5.5M
MOV SCON,#50H ;uart-m1,tx and rx
MOV PCON,#80H ;double baud rate bit
MOV TCON,#40H ;start baud timer
;initialize max3100 uart-irda mode at 9600 baud
MOV TX1,#0E4H ;high byte of config-R ints
MOV TX2,#0CAH ;9600 baud irda mode and two stops
CALL UTLK ;send to uart-write config
;*****MAIN ROUTINE LOOP*****
LOOP: JNB IRQ,URCV ;data avail from 3100 uart?
NRCV:JBC R1,RCV51 ;check for 8051 rcv-tx out irda
JMP LOOP ;hang here forever
;byte received from 3100 uart-get it and send out 8051 uart
URCV: MOV TX1,#0 ;read data
MOV TX2,#0 ;read data
CALL UTLK ;send to 8051 uart-get data to rx
MOV A,RX2 ;get data to acc
MOV SBUF,A ;send out on RS-232 side 9600 baud
JMP LOOP ;back to top
;byte received from 8051 uart-get it and send out 3100 uart
RCV51:MOV A,SBUF ;data from 8051 uart
MOV TX1,#80H ;tx data
MOV TX2,A ;data to irda
CALL UTLK ;send to uart-send data out IrDA
JMP LOOP ;back to top
;*****
;SUBROUTINES
;UTLK-talk to uart-main routine
; send 16 bits from TX1 TX2 and rev 16 to RX1 RX2
UTLK: CLR CS ;activate cs
MOV A,TX1 ;get high byte
CALL BYTS ;send out
MOV RX1,A ;get received 1
MOV A,TX2 ;get high byte
CALL BYTS ;send out
MOV RX2,A ;get received 2
SETB CS ;set CS high
RET ;DONE
;*****
;BYTS-shift out & in 8 bits with spi clocking-from and to acc
BYTS: MOV R4,#8 ;8 bits to send
SETB DIN ;make sure din is input
B8LP: RLC A ;get msb of acc to carry
MOV DOUT,C ;put out on pin
SETB SCLK ;clock high-clock
MOV C,DIN ;get data after clk high
CLR SCLK ;clock low
MOV ACC,0,C ;put in lsbit of a
DJNZ R4,B8LP ;loop til 8 bits
RET ;done
;end of code
END

```

Adding this "bit-banged" IC enables 8051 microcontrollers to communicate using an IrDA data link.

but the software is tricky. It uses up to 100% of the CPU's attention when active, and is impractical above 2400 baud. You also can generate IrDA tim-

ing with discrete logic or a PAL, but that approach is expensive, power-hungry, and requires an external baud generator for the clock source.

Circle 521

Use A Tiny Microcontroller With A Large Keypad

SAMUEL KEREM

Infrared Fiber Systems, 2301-A Broadburch Dr., Silver Spring, MD 20904; (301) 622-7134; fax (301) 622-7135; e-mail: samuelkerem@juno.com.

Like a student needing just one more night to prepare for a coming exam, a microcontroller designer often wishes for just one more I/O line as a project approaches its final stages. Even for the relatively capable 8X752 microcontroller at 28 pins, with its high processing power, direct connection of a 5×5 keypad would steal 10 I/O lines from a total of 21 lines, or would require a special interface.

For a small, low-cost 16-pin microcontroller like SGS-Thomson's ST6201/2, with only 9 I/O lines, the prospect of using any keypad isn't a glamorous one. Fortunately, the microcontroller designers have included an 8-bit analog-to-digital converter (ADC) into this microcontroller. The ADC may not be completely suitable to monitor high-resolution sensors, but it can be an excellent resource for scanning a keypad of theoretically up to 256 keys. Without being too ambitious, I will de-

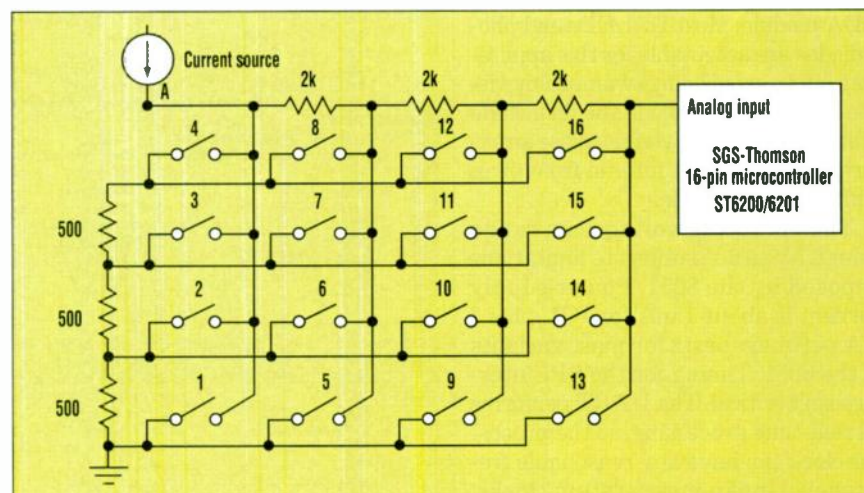
scribe a connection for a 16-key keypad. Having 16 keys makes the design (hardware and software) much simpler,

but the following guidelines also will work for a larger number of keys.

The 4×4 keypad shown is a typical layout, except that the rows and columns are separated by resistors (see the figure). The resistance between point A and ground—R(n)—depends on which key (n) is pressed: 0 Ω if the first key is pressed, 0.5 kΩ if the second is pressed, and so on with steps equal to 0.5 kΩ, up to 7.5 kΩ if the 16th key is pressed. $R(n) = (n - 1) \times 0.5 \text{ k}\Omega$. The current source will excite the resistor network and the resulting voltage drop will be measured by the ADC. For a 0-5 V analog-to-digital range, a current source slightly higher than 2.5 V/7.5 kΩ = 0.33 mA is suggested. For instance, the value 0.34 mA fits the bill; it will offset the voltage drop, excluding jumps of 2 LSBs due to possible analog-to-digital conversion noise. Also notice that only half of the maximum input range is used. This makes it possible to:

1. Get a 17th condition: No key is pressed when the ADC data equals 0xFF.
2. Get the pressed key's number by shifting the analog-to-digital conversion data three bits to the right (or division by 8).

The larger the keypad, the more attention you must pay to the resistor values and tolerances, ADC noise, and the accuracy of the current-source setting. In addition, if the result of the 256 divide by keys' number isn't power of 2, your software will be a little more complicated. Another approach might be just to use the second analog input for an additional 16 keys.



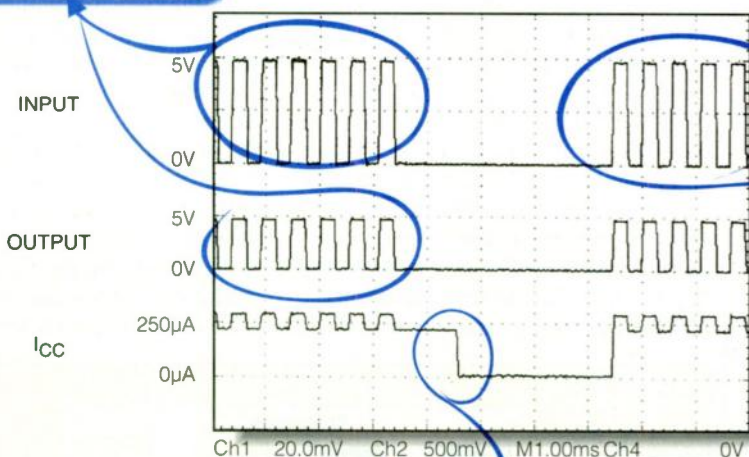
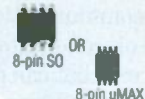
An 8-bit ADC, included in this microcontroller, makes it possible to, at least in theory, scan keypads with up to 256 keys. Illustrated here is a typical 4×4 keypad layout using this microcontroller, with the only exception being that the rows and columns are separated by resistors.

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Circle No. 158- For U.S. Response

Circle No. 159- For International

Circle 522

Automatic Phase Detector For Digital Communications

EDUARD BERTRAN and FRANCISCO LOSCIUTO

Universitat Politècnica de Catalunya, Dept. of Signal Theory and Communications, c/Jordi Girona, 1-3, 08034-Barcelona, Spain; phone: +34 3 4015938; fax +34 3 4015910; e-mail: tsceba@eupbl.upc.es.

Digital communications equipment based on coherent detection need receivers that can generate a carrier synchronized signal from a suppressed carrier transmission. For example, in a two-phase carrier receiver such as BPSK, a common solution is to use a 2nd-order law device. If its input is a tone of frequency f_0 with information in the phase Φ , its output is given by:

$$A \cos^2(2\pi f_0 t + \Phi) = A \frac{\cos(4\pi f_0 t + 2\Phi) + 1}{2}$$

This signal is passed through a PLL that operates as a narrow-band band-pass filter around the frequency $2f_0$. Hence, if $\Phi = 0$, the output phase also is 0. And if $\Phi = 180^\circ$, the output phase is $2 \times 180^\circ = 360^\circ = 0^\circ$. Therefore, phase discontinuities are removed, and the PLL output is a continuous phase signal of frequency $2f_0$, where phase modulation has been eliminated. Then, a divider by 2 is sufficient to have a carrier synchronized with the received modulated signal. The same applies when using 4th-law devices with quadrature-carrier receivers, such as QPSK or QAM.

With this solution, we have a single phase, but its value can't be guaranteed. For example, in a BPSK transmission, it can be stated that the PLL output is a synchronized carrier of frequency f_0 , but there's no way of knowing whether the relative phase is 0° or 180° . A mistake in the relative phase can result in unexpected changes of the received "zeros" or "ones," and vice versa. A block diagram depicts the carrier recovering process and the demodulator for a BPSK modulated signal (Fig. 1). The automatic phase detector is shown in the dashed lines.

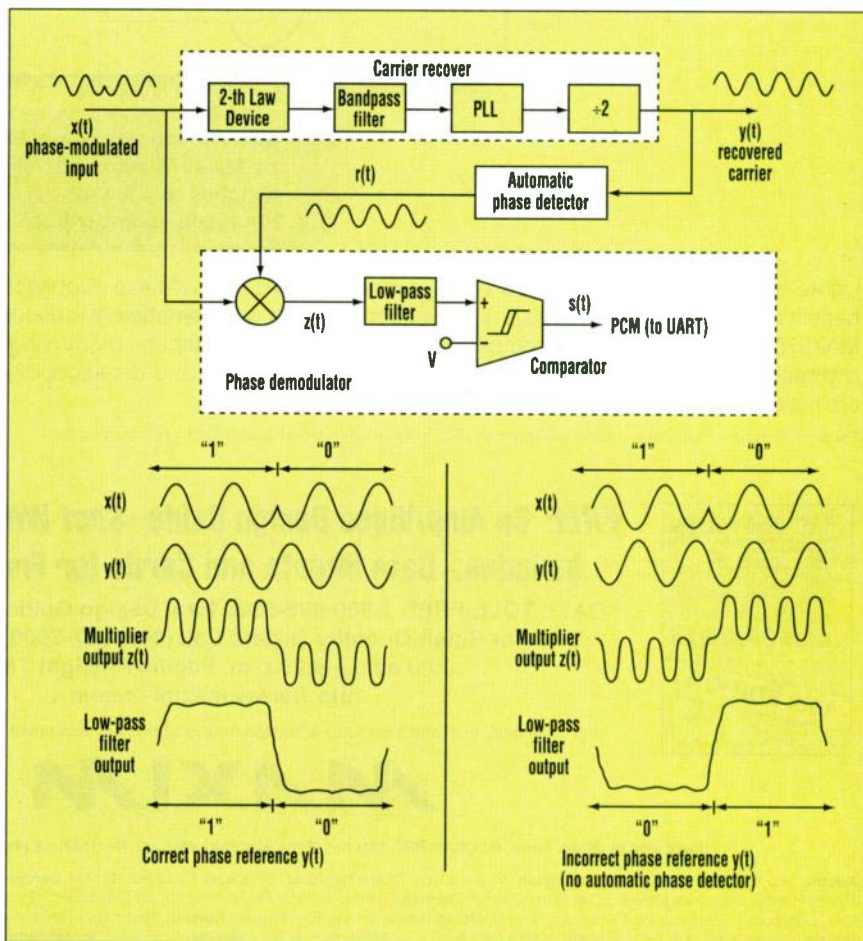
In non-differential encoding, a phase reference adjustment is required to avoid false decoding. The

usual solution is to transmit a known preamble at the start of some messages to permit phase adjustment. This is a good solution, albeit time-consuming in terms of preamble synchronization (training process). The approach presented is an alternative to phase discrimination based on the parity error bit of the UART. This alternative is useful in asynchronous phase communications and requires no preambles between the transmitter and the receiver. The circuit is based on the HD-6402 IC, which permits hardware

detection of the parity error (Fig. 2).

The circuit operates on the principle that the correct phase reference permits a correct demodulation and, consequently, minimizes (and ideally, nullifies) reception errors. Incorrect phase references increase errors and, consequently, the number and the frequency of pulses in the parity error (PE) pin in the UART. The low-pass $R_a C_a$ filter after the PE output gives a voltage value proportional to the number of errors, much like a voltage-to-frequency converter.

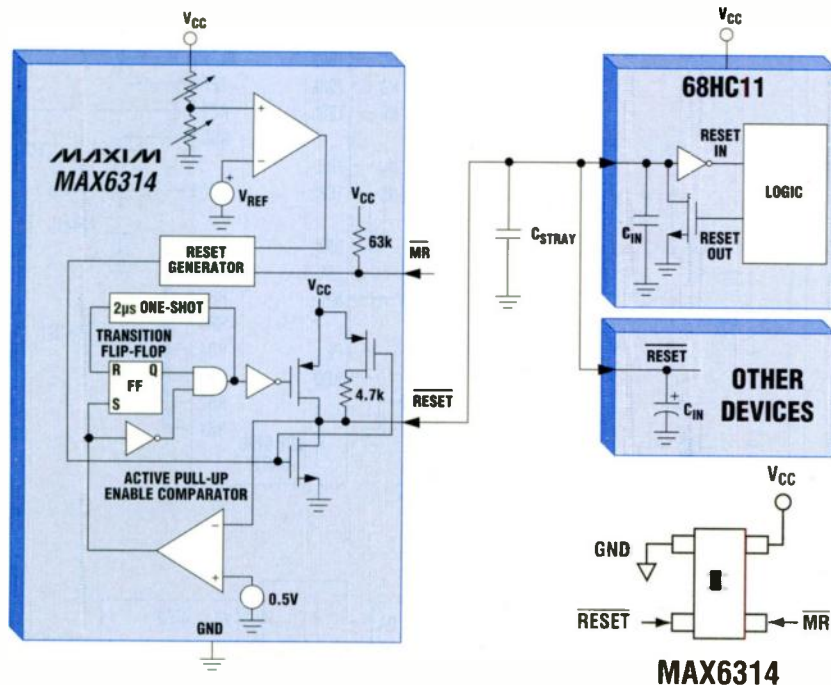
If this voltage is sufficient to activate the analog comparator (TL082 op-amp-based), the binary counter (4520) modifies their outputs. These outputs select, through the multiplexer (4052), one of the four phase references (0° , 90° , 180° , and 270°) given by the shift register (4015), whose outputs QA through QD are shifted versions of the recovered carrier. This system runs continuously like a tracking loop, until the correct phase reference is presented to the demodulator.



1. Shown is the carrier recovering processing and the demodulation for a BPSK modulated signal. The automatic phase detector is outlined in a dashed box.

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The MAX6314 avoids this problem by actively driving $\overline{RESET}$ to its high state when it detects that the 68HC11/16 has ceased pulling $\overline{RESET}$ low.

The MAX6314 is also well suited as an enhanced replacement for open-collector reset ICs used with wired-OR reset buses. The internal 4.7k Ω eliminates an external component. And because the MAX6314 disconnects the 4.7k Ω pull-up resistor when asserting reset, the supply current is a low 5 μ A, even when $\overline{RESET}$ is low.



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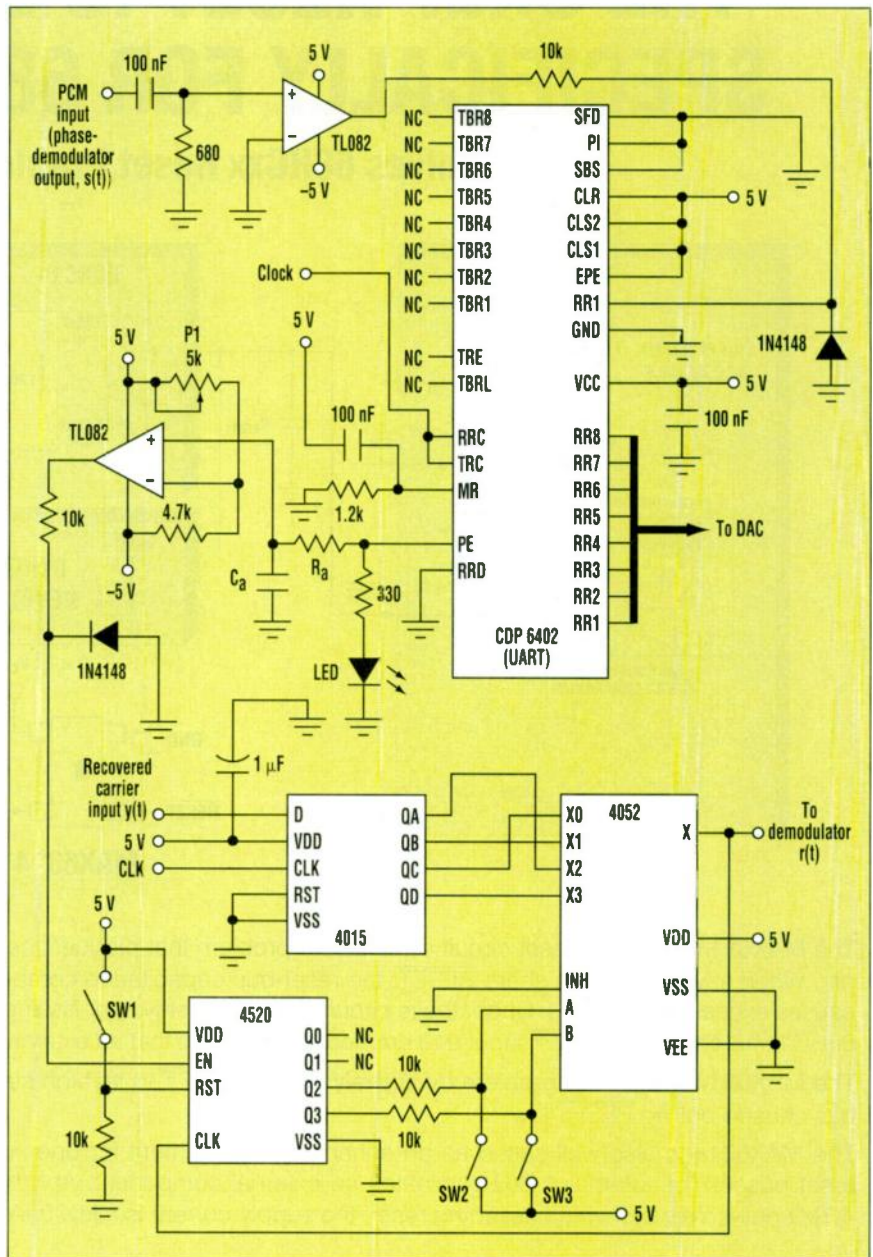
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2. This circuit, which is an alternative to phase discrimination, is based on the parity error bit of the UART, using the number and frequency of the pulses to lock in the correct phase reference.

At this moment parity errors are scarce, and a low voltage is presented to the analog comparator. This stops the phase tracking, and the system remains in the correct phase reference.

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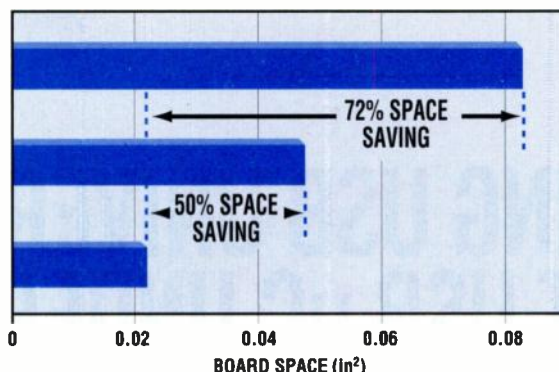
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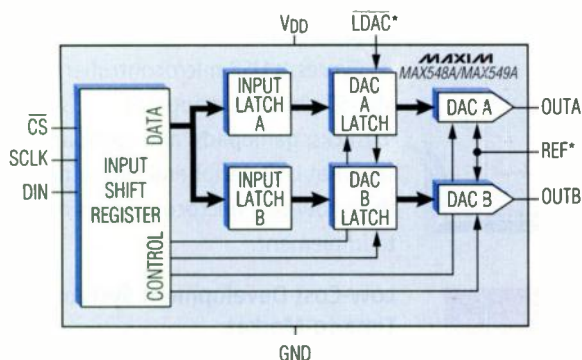
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CY7C634xx	256 Bytes	8 KB	31	40-pin DIP 48-pin SSOP
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What's All This Errata Stuff, Anyhow?

This was GONNA be a Floobydust column, but it turns out that this will be one chock-full of some of RAP's Errors:

(a) I was partly correct when I said that 1 meter was exactly 39.370000 inches, and 1 km = 3280 ft. + 10.000 in. It did *used to be*. That was the statement in my 1958 *CRC Handbook of Chemistry and Physics*. But then they changed it later on in 1958. The U.S. inch was changed by 2 ppm, to exactly 2.540000 cm. The NBS did not ask my permission. The CRC did not recall my book. Hey, it's only an error of 2 ppm. Most people wouldn't notice the difference. But if you were buying a square mile, you wouldn't want to be cheated out of 111 square feet.

About a dozen guys wrote to correct me. They were right. Note: I had sent the draft of my column, with this old error, to 60 guys within NSC, and none of them noticed my error.



BOB PEASE

OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

(b) I stated in a recent column on Measurement that a thumbnail was not 1-mm thick. It was, I said, more like 0.5 mm. But one guy spotted that I multiplied my 12 milli-inches by 39.37 instead of dividing by 39.37. So, it was really more like 0.3 mm. I am usually fairly careful about my dimensional analysis by saying out loud, "1 inch = 2.54 centimeters = 25.4 millimeters; and one milli-inch is 25.4 micrometers. Then 12 milli-inches is about 12×25.4 micrometers, which is equal to 300 mi-

crometers, or about 0.3 millimeters." But I got sloppy. Dumb error.

(c) Likewise, I said that a Ranchette (which is equal to 0.5 picoacre) was 0.9983 milli-inches in radius. JUST ONE GUY, Charles Wilson, questioned me—he computed 0.99915 mils in radius. He was right. I was wrong. I had neglected to take the square-root. So, one Ranchette is an area equivalent to a circle 0.99915 milli-inches in radius.

(d) Similarly, I explained very plainly and correctly, several months ago, that 9 old copper pennies weighed within 1% of an ounce, but it took 11 new zinc pennies to weigh that much. Yet in the March 3 issue on page 188, I was sloppy and said that 9 new pennies weighed an ounce. WRONG!!!! I sorry!

(e) I stated that you can send only as much as 1.99 pounds of U.S. mail at the first class rate for \$3.00. But Robert Klabis pointed out that if you get an Express Mail Envelope (free at any Post Office) you can fill it up, and mail it for that \$3.00 fee, even if it's over 2 lb. Now, it's hard to squeeze more than 2.5 lb of copy-paper into one of those envelopes. But if you have to send 4 copies of *Electronic Design*, weighing up to 3.5 lb., you can send that for \$3.00. Not too bad, when you consider that a 13-ounce package also goes for that price.

(f) In my recent column on Web Sites, I mentioned the coffeepot at CERN that had its own web page. Two guys wrote in to observe it was NOT at CERN, but at Cambridge University in England. I got fooled by some misleading text in a newspaper story. SORRY!!!

(g) One guy observed that if you use the right interpretation, and if you had some cylinders smaller than others by exactly the right amount, you could get 8 cylinders to "touch" each other. Well, if you go out to "The Four Cor-

ners" area, and you use a definition that Colorado "touches" Arizona (which is diagonally opposite), while Utah "touches" New Mexico, then you would agree that he made 8 cylinders that "touch" each other (*see the figure*). But I don't like that definition—nor that solution. When I get 7 cylinders to "touch," they really TOUCH.

(h) I got some e-mail from a mathematician, Mr. Alan Kaplan, who found it hard to believe that I could cut a torus into 13 pieces. But I talked him into it. Then HE pointed out that if you considered a hollow toroidal shell (instead of just a solid torus), you could cut it into 14 pieces. Well, I found that hard to believe. Think of the piece that's labeled 2 in the April 14 issue. If you consider it as a solid, you can cut that into 3 pieces. But if you consider it as a thin shell, it is now cut into 4 pieces. So, he was right! While many patterns of cuts will make exactly as many pieces of surface as of solid, here's a case where the number is *not* the same. And that is the solution I showed in my Column!

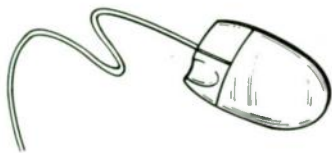
(i) I told some people on my lecture tour that Avogadro's Number had been changed from 6.0228 to 6.047 $\times 10^{23}$. Everybody was astonished. Why? Well, first I think I must have miscopied the number. Maybe it was changed from 6.02283 to 6.022147. A minor change of perhaps -0.011%. This occurred about 15 years ago, we THINK, and the reason was to base the number on atoms of CARBON (instead of OXYGEN), which could be done more precisely. This may be because carbon does not have as many screwy isotopes as oxygen does. I'm not sure if that makes the number of atoms any easier to count....

(j) I said that a thermal "pilot generator" used in a gas stove must be some funny animal, because it could not be a series connection of several thermocouples. Well, somebody gave me an old "pilot generator." I busted it open. Guess what was inside! A series connection of (N) thermocouples, with about $7 \mu\text{V}/^\circ\text{C}$. That's reasonable.

(k) I built my water detector with steel wires pressing on a thin piece of sugar cube. I still have not had any false alarms. (Ants out here don't attack sugar.) But when I put water on it a couple of times, it did not contact really well. So, I took some old gold-plated

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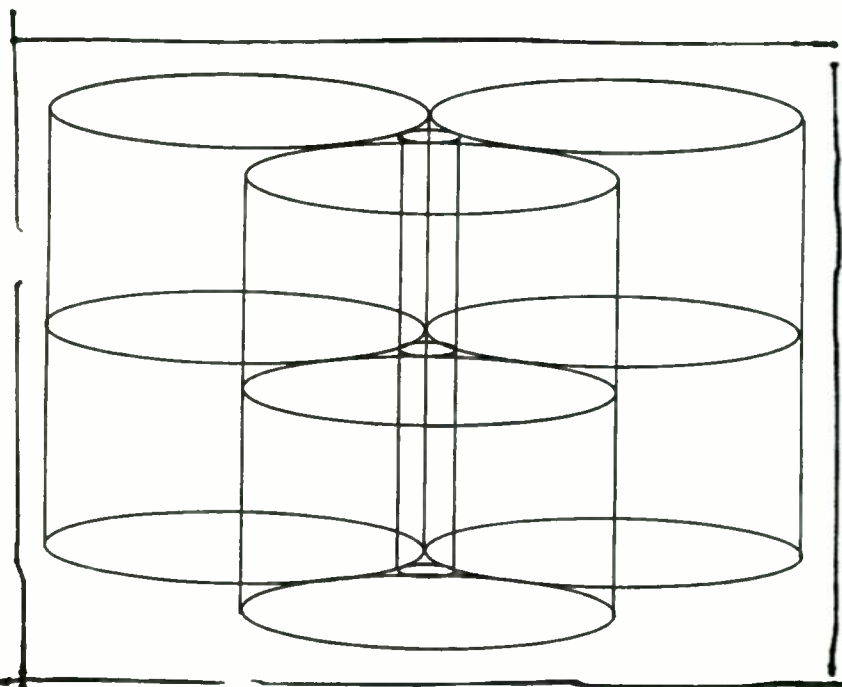
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BOB PEASE



Submitted by Mike Deering, Sr. Project Engineer, TRW Automotive Electronics, Farmington Hills, Mich.

transistor leads and set them up to act as the contacts off on the side where they never touch the sugar. They seem to be more reliable for contacting. One guy proposed a plastic clothes-pin. That sounds OK, but if you laid it down in an upright way (horizontal pivot), the water would not hit the sugar until it was 1/4-in. deep. Solution is to lay it on its side, with vertical pivot. That would work pretty well—especially if you add gold-plated contacts.

(l) I said the number of miles around the Annapurna Loop was about 205. I got more information from different guidebooks. That old number may have been true before newly constructed roads lopped off 40 miles. Now it's probably more like 166 to 163. Bezruchka's book states that the mileage is "more than 150 miles (330 km)." Well, 330 km equals about 205 miles, so that is probably what it *was* originally. But in Nepal, they don't usually talk about the *miles* of a trail. They count it by the *hours*. Still, 165-odd miles is not so bad for 22 days. More like 7.5 miles per day, rather than 9.3. Of course, we will take a lot of day hikes after we get to camp.

(m) For years I've remembered that the length of the Harvard Bridge is 364.4 smoots. In June, I walked across the bridge to Cambridge to go to see some guys at Draper Labs. I said I avoided the expense of a cab,

and the JERK on the MBTA trolleys, by walking across the Bridge. They asked me how long the bridge was. I told them how many smoots it was. They said, "AND???...???" and I added—"and one ear." That is the correct length of the bridge. One smoot is about 5 ft 11 in., named for Oliver Smoot (MIT '62) who was laid down end-to-end with himself, 364.4 times, to calibrate the length of the bridge whereby Massachusetts Avenue crosses the Charles River to go to Boston. By forgetting the "one ear," I made an error of the order of 40 ppm. This is perhaps 20X bigger than the error involved in the revision of the meter's calibration vs. the inch. But I just had to include this to heckle Roger Engelke and Mike Sciannamea and make them grouchy. The ranchette is not exactly a standard measure of area. But the smoot is well known in Boston and Cambridge Mass. They can both be found in the Webster's Third, Unabridged, International—well, at least in MY copy...

All for now. / Comments invited!
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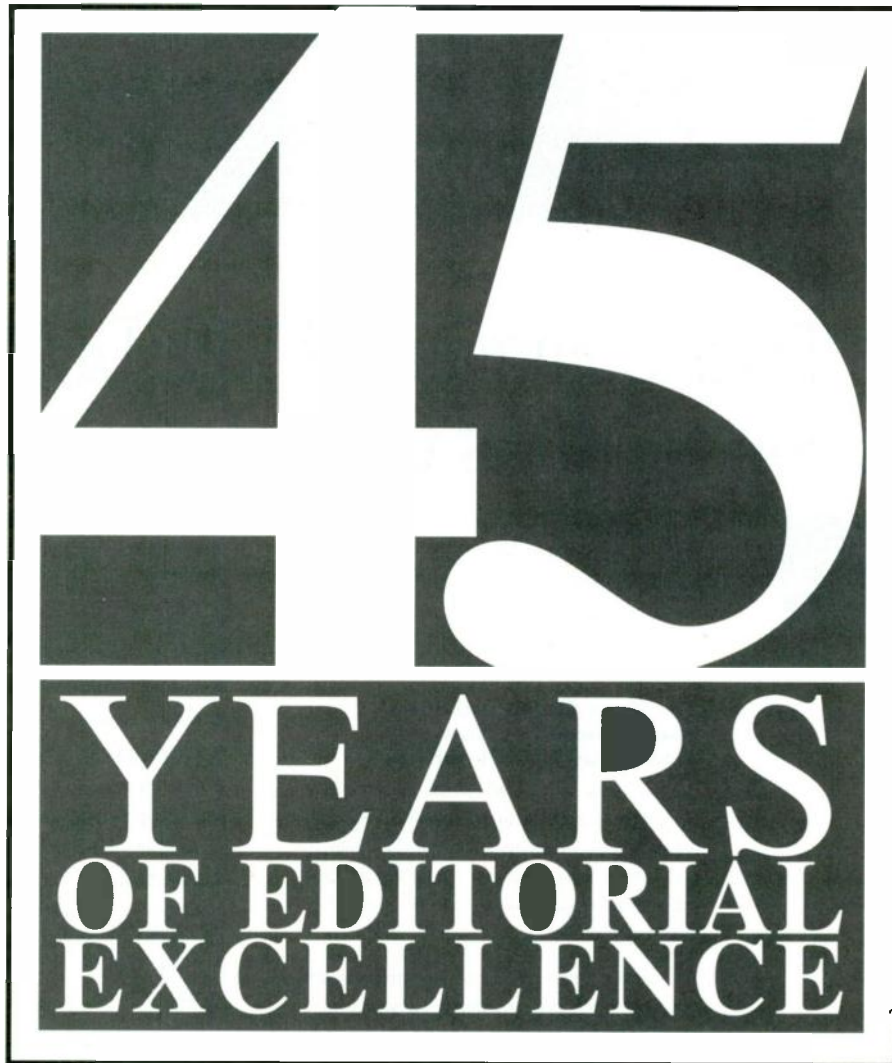
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A P E N T O N P U B L I C A T I O N

The Readers Respond:

Another Mailbag Of 'Tool & Tip' Reactions.

Since the last time we summed up reactions to this column (June 9), several more installments have gone by. That, along with the earlier columns not reviewed due to publishing lags, provides quite a mailbag, and a good point to sample a variety of reader feedback.

Analog's Shrinking World (April 1): This topic must have been pretty much on target, as certainly no one wrote in to object to the basic theme. Rather than that, virtually all responses received on this column agreed that the shrinking world phenomenon of surface-mount isn't necessarily helping analog performance. In many respects, it is creating near-term problems for designers.

But, there is one positive aspect of IC performance within the smaller packages which was originally mentioned, and also showed up in reader feedback. This is simply the overall reduction of parasitics. Certainly for cases where power dissipation isn't a performance limitation, smaller packages do help, with less parasitic effects and correspondingly better high-frequency performance. But from the designer's perspective, this can really be a two-edged sword. Why? The ultimate performance can indeed be better, but the route to getting there may be more difficult than ever. Breadboarding is much more difficult, if not outright impractical, so lots of time and money can be spent finalizing a design. In the long term, more complete models will help with simulating designs before prototyping, at least for those system portions where models do exist. Unfortunately, for LSI analog and mixed-signal IC components, the model world right now is a relatively barren landscape.

What can help leapfrog the design impasse is more work by the IC vendors in characterizing their complex analog parts within the complete system environment, and then providing the customer with evaluation boards that reflect this aggregate effort. The board then becomes a practical means of demonstrating viability of a part for

an intended function. The customer is then able to adapt the pc-board design of the evaluation board for their own system, with the knowledge that some minimum performance levels will be realized. And without the major time/expense efforts involved in multiple iterations of a sophisticated high-frequency layout. A case in point of just this context was the evaluation board for the AD8116 16x16 crosspoint switch, which underwent multiple passes before the desired isolation performance was realized.

The Well-Stocked Toolbox (May 1): This one drew a number of responses with the same general theme—that people like to be provided with links to useful design-related websites and other info sources. This is an understandable thing, so as long as they appear useful, we'll try to keep them coming.

Readers Respond (June 9): In this first piece reviewing early columns and reader reactions, some issues were raised that brought even further useful responses.

Related to e-mail, I invited reader responses on solutions for combating SPAM, and got an interesting and useful response from reader Michael Guthrie. **TIP:** He describes his version of a SPAM filter trick as follows:

Dear Walter:

My solution to the SPAM problem is right in your column. I keep multiple mail boxes. Since Juno is free, I use it whenever a message is likely to generate SPAM. Hence, my mail comes in presorted! One box for direct contact in business, another to register on web sites and for USENET, etc. Since you can have as many Juno boxes as you want, just use different boxes for different purposes. It also allows you at times to figure out where the SPAMmer got the address.

So, perhaps an answer may sometimes be lying just under your nose, eh? Thanks to Michael for sharing his useful anti-SPAM tip with us.

Personally, I prefer a single mail program that can scan multiple mailboxes, and then sort downloaded mail into folders (including the trashbin). But, I also realize that our tech-world complexities can often be very non-accommodating, forcing us to use proprietary software for those services that insist on it. But, alas, if only we had some recourse for an e-mail address that has already found its way to various SPAM lists (short of outright abandonment, that is).

TIP: Here's some miscellaneous book news. First, with regard to the June 9 column's book list, there are several interesting developments. Sergio Franco's book, *Designing with Operational Amplifiers and Analog Integrated Circuits*, from McGraw-Hill, should be out in a second edition by the time this column appears.

A couple of readers asked about my own (as then reported) OOP book, *IC Op Amp Cookbook*, 3d Ed. I'm now happy to say it is available again.

Another reader wrote to say that Jim Roberge's *Operational Amplifiers: Theory and Practice* (Wiley, 1975 ISBN 0-471-72585-4), should also have been on the "top ten" list. This is a point with which I basically don't argue. However, all such lists must get whittled down. But, I'd still rate the (OOP) Roberge

book a close #11, and I do hope to see it in a new edition someday. In the interim, readers may be able to find it via the OOP sources in the June column.

Dan Sheingold, editor of *Analog Dialogue*, wrote about a new (and free) offering by various ADI engineers. A collection of 23 different chapters that originally appeared in *Analog Dialogue*, the 53-page (plus index) book, *Ask The Applications Engineer* can be requested from the ADI literature center at (800) 262-5643.

Low Noise Power For Analog Circuits (June 23 Analog Special Issue): This one drew a couple of responses from some old co-workers, more to say hello than anything of major interest in the column itself. But, I'm always glad to hear from old friends, especially if a current topic is of interest in your work. So, don't be bashful!

Another reader wrote to say that



WALT JUNG

the bootstrapped supply configuration used in the regulator of that column may be of help to him in a higher voltage version. Due to space constraints in the June 23 article, higher voltage modifications didn't get addressed, but they are nevertheless feasible. In that circuit, the ultimate limit is the maximum rail voltage of the op amp used, or typically 36 V for such types as the AD797 (used in earlier versions of the basic design). And, you also need to satisfy the startup voltage criteria, as was generally outlined in the article. If anyone needs details on setting up regulators appreciably higher than 18 V, drop me a note. This has been done, and with sufficient interest, it could be a future topic.

EEs And the Audio Hobby (July 7): This one, with a theme of DIY audio projects and related source information, drew more in terms of both quantity and quality of mail than any other column thus far. Naturally, I find this just delightful, since audio is my hobby as well as yours. So, my special thanks to all who wrote in. Why? For providing a mandate to feature more audio-related topics in future columns!

To take some sample reader reactions, Rich Compeau wrote in and described a power amp project he and Bob Krebs recently tackled.

Hi Walter:

Several of us at work enjoyed your article "EEs And The Audio Hobby" in the July 7 issue of Electronic Design. It hit pretty close to home!

The latest power amp is an all-FET, two-stage, single-ended Class A amp biased for a load of 3 Ω . It utilizes servo bias, servo-offset reduction, a regulated high-voltage front-end supply, and an unregulated high-current supply. There is no active current limiting circuit (the Hexfets will probably protect the fuses). It has low NFB (<10 dB) and no capacitors outside of the power supply and servo loop compensation networks. The Zobel is implemented as an L-R. The efficiency is only about 10% (great for Northern climates), but the sound is pretty incredible!

In designing and building this amp there were many challenges—cutting and drilling aluminum; thermal calculations and heat sinking; prototyping and pc-board design and layout; reliability calculations; procurement of expensive and hard-to-find compo-

nents; procurement of used test instrumentation, which sometimes worked; high-current power-supply design and protection; modular construction concepts; creation of SPICE models; disconnection of the smoke detector over my bench, and, treatment of minor burns....

In bringing a major DIY project to fruition, Rich has described experiences going far beyond basic design and calculation tasks, which also well illustrates the diversity of skills required to build a sophisticated audio project from start to finish. Thanks for sharing this story with us, Rich. I hope your interesting amplifier is ultimately published as a DIY project.

Barry Bolling, a former student of Marshall Leach's at Georgia Tech, wrote in to describe building the low TIM amplifier referenced in the footnotes of the July 7 column. Excerpted from his "Background" notes from the cited web page, Marshall Leach has this to say about this amplifier:

The Leach Amp v4.2, is the latest update of the "Low TIM Amplifier" which I originally published in Audio Magazine. The Georgia Tech students who built it never referred to it as the "Low TIM Amplifier." They always called it "The Leach Amp." Over the years, I have seen countless versions of the amplifier built by students and others. All of the bugs have been worked out, and the amplifier should perform flawlessly if it is built with patience and care. This is an advanced construction project. I do not recommend that someone tackle it who has not had experience with electronic construction and assembly.

The Leach amplifier, with its maturity and all of the well documented technical details should be a good DIY project for audio-minded EEs.

Ian Haynes, a U.K. reader and audio enthusiast, wrote that I missed another U.K. publication covering DIY audio, namely *Hi-Fi World*. While I have seen them on occasion, this hasn't been occurring regularly or recently. What I have seen dates to three years ago, and featured then was an interesting class-A power-amp project with bipolar output devices. For those who wish to investigate this one, you can reach them at: Hi-Fi World, Audio Publishing Ltd., 64 Castellain Rd., Maida Vale, London W9 1EX,

+44(0)171-289-3533; fax: +44(0)171-289-5620.

In the July 7 column, I also talked about the new Telnet Internet access feature of The Audiophile Network (TAN), a popular and useful audio forum. However, I didn't offer details of use. As it turns out, this is simplicity itself if you are running Windows 95.

TIP: To get started, all you need to do is create a shortcut to the Windows 95 Telnet utility, which by default is: C:\WINDOWS\TELNET.EXE

You do this by logging into your C:\WINDOWS directory with Explorer, locate the TELNET.EXE file, and drag it to the desktop. Presto, you now have a Telnet shortcut! Then, click on this Telnet icon to bring up the program and start your Winsock. Once connected, under the Connect menu, select Remote System, which brings up a dialog box. Enter "TANet.com" for Host, "telnet" for Port, and "vt100" for Termtype, then Connect, and you should then soon see the TAN login prompt. After entering your particulars and logging in, you'll want to check the recent on-line messages for other user preferences in Telnet packages.

However, the above is just a quick start for anyone with Windows 95 running. You'll ultimately want a more sophisticated Telnet program. Fortunately, the TAN website offers more in the way of setup detail, and you'll want to visit <http://www.TANet.com>.

Do so, and follow the instructions to acquire and setup up the advanced Telnet utility, "Netterm." You will then be able to start up your Telnet and log onto TAN from your browser.

Finally, one other category of mail received on the July 7 column were publisher inputs on audio books. As a given, I'm always interested in new books, and welcome any new information on the same. A couple of book reviews are in the works, and audio topics are also planned.

That's it for this mailbag installment. Many thanks to those who took the time to write in. I encourage you all to keep those card and letters coming.

Walt Jung is a corporate staff applications engineer for Analog Devices, Norwood, Mass. A longtime contributor to Electronic Design, he can be reached via e-mail at Walter.Jung@Analog.com.

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READER SERVICE 172

Auto-Adjustment Processor Targeted At VHS VCRs

The TDA9725 Y/C auto-adjustment processor is designed to eliminate the complex alignment problems previously required in the record/playback channels of VHS video recorders. The single-chip solution accepts a composite video baseband signal (CVBS) and converts it to a frequency-modulated luminance and 627-kHz chrominance signal for recording onto the tape. It also processes the playback signal to reconstruct a CVBS output. The IC interfaces to both glass and CCD delay lines. Phase-locked loops are used extensively by the TDA9725 to lock the entire processor to a 20.24-MHz crystal-controlled VCO frequency. These control loops ensure that all on-chip luminance and chrominance filters remain calibrated over the chip's entire operating temperature range, eliminating the need for circuit alignment. All of the required emphasis/de-emphasis, deviation control, and white-dark clipping functions are handled on-chip as well. The TDA9725 can be pin-voltage programmed to handle PAL, SECAM, or NTSC video signals, and it features a number of special "trick" modes in addition to standard and long-play record/playback modes. Due to the color sequence correction in the long-play still mode, the device is said to provide significantly better picture quality in an area of VCR performance that's usually rather poor. The TDA9725 comes packaged in a 52-pin shrink DIP. *AV*

Philips Semiconductors, P. O. Box 218, 5600 MD Eindhoven, The Netherlands, phone: +31 40 272 20 91; fax: +31 40 272 48 25. **CIRCLE 564**

DECT Monitor Helps To Visualize Air Interface Protocol

Designed for developing DECT software and installing as well as maintaining DECT systems, the DECT protocol monitor WG CPM-10 makes possible the visualization of the DECT air interface protocol. It's implemented on a 1/2 slot ISA card. Functions include testing of program modifications and troubleshooting installed networks. The WG CPM-10 also serves as a monitor during statistical evaluation of radio operation. Housed in an IBM-compatible computer, the card is supplied with MS Windows 3.1x-compatible software. Due to its modularity, multiboard solutions also are possible. For easy access when reproducing past measurements, protocol data and test instrument settings can be stored. The DECT protocol monitor includes the simultaneous display of MAC, DLC, and NWL layer information, as well as real-time filtering of messages and PMID. For future test applications, software updates will be supplied on disk. *AV*

Wandel & Goltermann GmbH & Co., P. O. Box 12 62, 72795 Eningen, Germany, phone: +49-71 21/86-16 16; fax: +49-71 21/86-13 33. **CIRCLE 565**

Platinum Temperature Sensors Available In SMD Package

A platinum temperature sensor developed by Heraeus Sensor-Nite—dubbed SMD1206—meets the DIN EN 60751 and CECC 40401-004 standards. It comes packaged in an SMD package that can be automatically handled by pick and place machines allowing the use in high volume productions. The unit's dimensions are 3 mm by 1.5 mm by 0.6 mm. SMD sensors are primarily used to compensate the temperature on the surface of electronic assemblies. This compensation is necessary because the temperature significantly influences the signal flow in an electronic circuit. For high-precision electronics (e.g., in trade weighing systems or for brightness control in LCDs), temperature compensation is a must. Another platinum temperature sensor from the same manufacturer is housed in a standard SOT-223 package, which is intended for SMT as well. This device is equipped with a cooling fan that significantly improves the thermal contact to the printed-circuit board and reduces the error due to self-heating. The 1000- Ω temperature sensor measures with an accuracy of $\pm 0.5\%$ over a temperature range from -50° to $+150^\circ\text{C}$ with a maximum drift of 0.04%. *AV*

Heraeus Sensor-Nite GmbH, Reinhard-Heraeus-Ring 2363801 Kleinostheim, Germany; phone: +49-61 81/35 52 11; fax +49-61 81/35 809. **CIRCLE 566**

PWM Generator IC Performs Variable-Speed Motor Control

The SA828 three-phase PWM generator IC is designed for cost-sensitive, high-efficiency ac induction motor drive systems. Switching carrier frequencies up to 24 kHz allow ultrasonic operation of inverter power switches, while the power waveform is stored in an on-chip ROM. Two standard waveform options are available: sine plus third harmonic (a popular means of increasing motor power output for a given line supply voltage to the inverter) or pure sine. Other waveforms can be provided upon request. The SA828 operates as a standalone microprocessor peripheral that requires the microprocessor's attention only if the frequency or the amplitude of the output waveform needs to be changed. Any of the popular 4- or 8-bit microprocessors or controllers can be interfaced with the SA828. Another IC, the SA838, is a single-phase variant that targets applications such as uninterruptible power supplies or single-phase induction motor drives. Both ICs come in both plastic DIPs and SOPs in a temperature range of -40° to $+85^\circ\text{C}$. *AV*

GEC Plessey Semiconductors, Cheney Manor, Swindon, Wiltshire, SN2 2QW, Great Britain; phone: +44 17 93 51 81 28; fax: +44 17 93 51 84 81. **CIRCLE 567**

Edited by Roger Engelke

Microcontroller Family To Add Flash-Based Models

Flash-memory technology combined with the 80C51 8-bit microcontroller architecture has yielded flash-based MCU family that will become a superset of both the 8XC52, 54, and 58, and the 8XC51FA, FB, and FC families. The new series, the 8X51RA+, RB+, RC+, and RD+, promises to open new market areas in which systems can be field updated or upgraded without replacing key components. It will also allow for a more economical manufacturing model because in-system configuration can take place at any point in the system manufacturing process.

The first of the new flash MCUs will be the 89C536 and 89C538, which will contain 16- and 64-kbytes of flash, respectively. The 64-kbyte version provides enough memory to support high-level languages such as C and C++. Both chips also will feature 512 bytes of RAM. Other on-chip resources include the company's advanced programmable counter array that supports complex timing and time-measurement applications, and a hardware watchdog timer that interrupts the CPU if it's caught in a loop or other unexpected condition. MCUs in the "+" series will operate from supplies ranging from 2.7 to 5.5 V, and at internal clock speeds of up to 33 MHz.

ROM-based versions of the RA+ MCUs sell for as little as \$2.95 each in lots of 25,000 units, while the flash-based 89C536 sells for \$14.99 apiece in small quantities (500 units). ROM and EPROM versions are available immediately; the flash-based MCUs will be available in the fourth quarter. DB

Philips Semiconductors, 811 E. Arques Ave., Sunnyvale, CA 94088; David Fair, (408) 991-2000; Internet: <http://www.semiconductors.philips.com>.

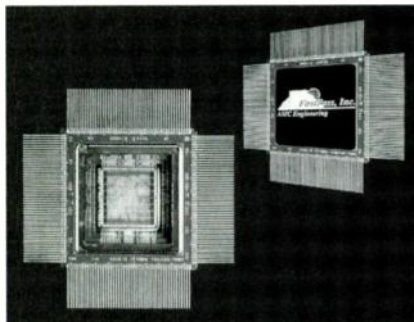
CIRCLE 485

Rad-Hard Controller Handles MIL-STD-1553B And 1773

The essential services node (ESN)—a multipurpose, multifunction device fabricated as a rad-hard ASIC—provides a solution to common design problems when space-systems designers create systems that use MIL-STD-1553B and 1773. The chip incorporates a 1553 bus controller, remote

terminal and monitor, the UT69R000 16-bit embedded microcontroller, two 8254-equivalent counter-timers, an 8255 parallel port, two 8251 UARTs, and other support functions.

The 16-bit MCU on the chip provides the host function for the UARTs and 1553 interface, and can be used to interface to additional devices through the 8255 parallel data port. Prior to this chip, designers would have had to



use multiple discrete chips, resulting in a much higher power budget, a component-laden board, a heavier weight, and an overly complex system.

Jointly designed between UTMIC and FirstPass, the ESN requires SRAMs and PROMs along with external applications-specific support devices. The ESN will be housed in a 208-lead PGA or a 196-lead flat pack, and now complies with QML Q and V. Price will depend on the level of radiation hardness required. Samples are immediately available from FirstPass. DB

UTMIC Microelectronic Systems Inc., 4350 Centennial Blvd., Colorado Springs, CO 80907; Anthony Jordon, (719) 594-8000; or on the web at <http://www.utm.com>.

FirstPass Inc., 651 Topeka Way, Ste. 500, Castle Rock, CO 80104; Greg Lannan, (303) 688-6866; or on the web at <http://www.firstpass.com>. **CIRCLE 486**

Serial Flash Data Memory Delivers 1 To 16 Mbits

The Serial DataFlash memory provides designers with a serial interface high-density flash memory designed specifically for data-storage applications, such as digital telephone answering machines, digital camera image storage, or data in pagers. Devices in the family will initially include 5- and 2.7-V 4-Mbit memories (the 5-V AT45D041, and the 2.7-V AT45DB041), with 1-, 2-, 8-, and

16-Mbit devices slated for introduction later this year. The chips are based on the same NOR flash-memory technology the company uses for its parallel-access flash memories.

Sector size on the chips is small, which allows wear-leveling algorithms to maximize memory life—the 1-, 2-, 4-, and 8-Mbit devices have sector sizes of 264 bytes, while the 16-Mbit device will have a 528-byte sector. Also on-chip are two 264-byte RAM buffers. These enhance the chip versatility and flexibility by allowing data to be transferred from the main array into a buffer, where it's changed and then transferred back into the main array from the buffer. The buffers also allow the chip to handle a sustained stream of incoming data.

The AT45D041 and AT45DB041 are available in 28-lead SOICs and TSOPs. Price for the AT45D041 in an SOIC package is \$6.71 each in 1000-unit lots; samples are available immediately. DB

Atmel Corp., 2325 Orchard Pkwy., San Jose, CA 95131; Richard De Caro, (408) 441-0311; or on the Internet: <http://www.atmel.com>.

CIRCLE 487

Synchronous Burst SRAMs Run At Up To 166 MHz

A quartet of high-speed 4-Mbit synchronous burst SRAMs are available with either pipelined or flow-through output modes. Clock speeds range up to 117 MHz for the two flow-through versions, and up to 166 MHz for the pipelined versions. Flow-through devices have a 2-1-1 access capability, while the pipelined devices have a 3-1-1 access sequence. The CMOS SRAMs include 128-kword-by-36-bit flow-through and pipelined versions (the GVT71128E36/G36), and 256-kword-by-18-bit flow-through and pipelined versions (GVT71256E18/G18). All four are housed in 100-lead thin PQFPs and sell for as little as \$66.88 each in lots of 1000 units (10-ns version of the flow-through memory, and 4-ns/117-MHz version of the pipelined SRAM). Later this year, the memories will be offered in 119-contact plastic BGA packages. DB

Galvantech Inc., 3080 Oakmead Village Dr., Santa Clara, CA 95051; David Hayes, (408) 566-0688; Internet: <http://www.galvantech.com>.

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Oxford Semiconductor Ltd., 68 Milton Park, Abingdon, Oxon, OX14 4RX, England; phone: +44 1235 86 14 61, fax+44 1235 82 11 41; www.oxsemi.com.

CIRCLE 489

GSM Phone Chip Set Has Two CPUs, All RF Stages

A complete four-chip set that's fully compliant with the GSM900 standard is now available. The GEM300 supports both full- and half-rate speech coding, and requires only three SAW filters and a power amplifier to complete the core design of a GSM cellular phone. The same basic design can be adapted to support DCS1800 or PCS1900 by changing only one IC.

Comprising four ICs, the GEM300 includes the GEM301—a digital cellular dual-band processor; the GEM302—a baseband and audio interface; the GEM303—an RF front-end and processor; and the GEM304 IF processor. The GEM 301 incorporates both an OakDSPCore and an ARM7 RISC processor. The Oak, augmented by on-chip accel-

erator logic, is used for layer-1 signal processing. The 32-bit ARM7 core operates the GSM protocol stack and supports the handset's operator interface.

The GEM302 performs all of the handset's baseband processing tasks. It incorporates the transmit and receive codec, audio codec, and a power amplifier control DAC. Also included is the differential I/Q interface, a pair of 12-bit delta-sigma converters, antialiasing filters, and GMSK modulation circuitry. IF and RF processing are handled by the GEM303 and GEM304 circuits. They employ an integral I/Q modulator and single sideband mixer transmitter; in addition to a dual-conversion receiver architecture.

An extensive set of development tools are available, including evaluation and development platforms and PC-based software tools that enable emulation and code debug. LG

GEC Plessey Semiconductors, 1500 Green Hills Rd., Scotts Valley, CA 95066-4922; (408) 438-2900; fax (408) 438-5576; www.gpsemi.com.

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COMMUNICATIONS

SONET/SDH Line Interfaces Shrink Size And Cost

The TM311DVA and TM311TRFVA transceiver line interfaces are compact, integrated surface-mount packages that contain all of the components necessary for both STM-1 (311.04 Mbit/s) and E4/STM-1 (278.528

former coupling to match impedances of the ECL circuit and cable plant within a particular application to provide a minimum of -15 dB of return loss. The wide-band pulse transformers also offer high isolation and transient damping, as well as dc suppression. The units' integrated filtering permits them to operate under noisy conditions at full line rates over 175 meters of coaxial cable.

Priced at \$25 each in 1000-piece quantities, the TM311DVA is available now. The TM311TRFVA, which includes loss-of-signal detection, costs \$33 in similar lot sizes. LG

Pulse Components Division, Two Pearl Buck Court, Bristol, PA 19007-6812; (215) 781-6400; fax (215) 781-6403.

CIRCLE 491

Voltage-Variable Attenuators For PCS, WLAN, And WLL Apps

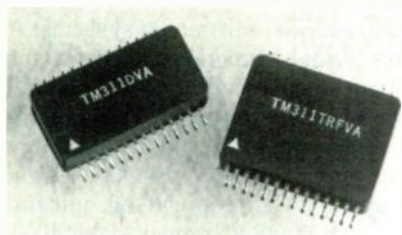
The SM-515003 and SM-516003 are a series of voltage-variable attenuators (VVAs) designed for use in personal communications service, wireless LAN, and wireless local loop trans-

ceivers. They're cascadable with themselves or any other 50- Ω VVAs, without the need for external components. The SM-515003 covers an operating range of 3 to 30 MHz, while the SM-516003 is designed to cover the 300- to 3000-MHz frequency range. Both attenuators operate on 5 V and require two analog control voltages per section with a range of -3 to 0.0 V, drawing less than 15 μ A of current.

These devices retain linearity and digital compression and can act as an AGC function of radio signals. The SM-515003 is well suited to communications and data-transfer functions in post-down-converter IF processing. It's designed for very low VSWR, (1.8:1 typical), and can provide up to 70 dB (typical) of isolation at 100 MHz.

Available now, both VVAs are housed in a 16-lead SOIC. In 10,000-piece orders, the SM-515003 costs \$2.10, and the SM-516003 goes for \$2.40. LG

Samsung Microwave Semiconductor, 1530 McCarthy Blvd., Milpitas, CA 95035; (408) 433-2222, fax (408) 432-3268. CIRCLE 492



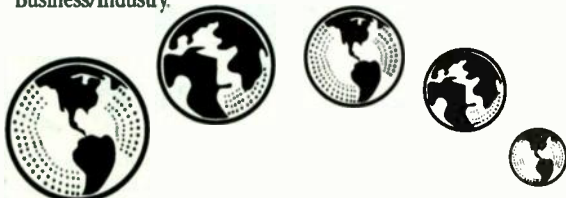
Mbit/s) applications. Capable of transmitting and receiving full duplex data at E4 and STM-1 rates, they replace several previously separate components currently required to perform the signal amplification, transmission, and filtering tasks required by the ITU-T/G.703 specifications.

Both transceivers utilize trans-

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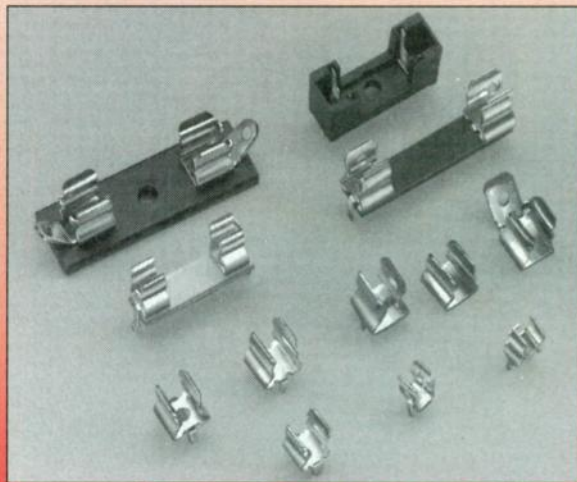
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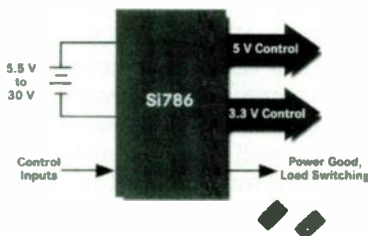
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ANALOG

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Two power controllers developed by Temic Semiconductors are pin-compatible and functionally equivalent drop-in replacements for the MAX786 dual-output power controller. The Si786CG



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Both controllers convert 12-V battery-pack energy or the 18- to 24-V output of an ac-to-dc wall converter to the 5-V and 3.3-V supply voltages used by notebook computers. The less-than-500- μ A quiescent current

per converter prolongs battery life. The micropower linear regulator further conserves battery power by keeping power management and backup circuitry alive when the step-down circuitry is shut down. The comparators can be biased at any voltage between 2.7 V and the input voltage to simplify battery monitoring or provide sufficient voltage to enhance the gate of a low on-resistance n-channel FET used to switch power to different zones in a system.

The Si9130CG omits comparator circuitry not required for many applications and instead provides a pin-programmable output of 3.3-, 3.45-, or 3.6-V for the second converter. Both controllers have a 25- μ A shutdown current, and are available in a 22-pin SSOP package for operation over the commercial temperature range. Unit pricing in quantities of 1000 is \$6.30 for the Si9130CG and \$7.20 for the Si786CG. ML

Temic Semiconductors, 2201 Laurelwood Rd., Santa Clara, CA 95054-1595; (800) 554-5565, ext. 25.

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technique is used for the display. The acquisition memory is partitioned into segments corresponding to the display resolution. For every segment of points in the memory, the scope detects and displays the maximum and minimum value, ensuring that the user can see any signal change on the display. JN

Yokogawa Corp. of America, 2 Dart Rd., Newnan, GA 30265; (800) 258-2552; fax (707) 251-2088; <http://www.yca.com>. **CIRCLE 495**

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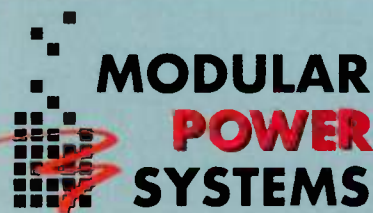
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CIRCLE 568

Get The Long And The Short (Form) Of Component Line

A four-page short-form catalog summarizes the components available from RAF Electronic Hardware, Seymour, Conn. The RAF components are used in pc boards, instruments, and electronic equipment. A wide selection of English- and metric-sized hardware ensures that readers will find the correct style, size, material, and finish for their application. The catalog illustrates and describes eight hardware lines, including standoffs, spacers, captive panel screws, thumbscrews, non-metallic washers, and a full line of handles. A convenient fax-back form lets readers request evaluation samples, additional RAF literature, or sales assistance. For a free copy of the *Electronic Hardware* catalog, call RAF at (203) 888-2133, or fax (203) 888-9860. You can also e-mail the company at info@rafhdwe.com. LM

CIRCLE 569

Brochure Details Compact Field And Lab Recorder

An eight-page brochure from Astro-Med Inc., West Warwick, R.I., pro-

vides details on a compact, two-channel field and lab recorder. Learn all about the Dash II recorder, which features laser-quality printing, built-in DSP filtering, an internal rechargeable battery, and a front-panel floppy-disk drive. The brochure contains complete specifications for Dash II and a variety of full-size, un-retouched chart samples. Special features are highlighted in four close-up photos and a large callout page. Call the company at (800) 343-4039 or (401) 828-4000 for a free copy of the brochure. LM

CIRCLE 570

Learn How Mechanical Assemblies Are Made

Precision Mechanical Assemblies is the latest color brochure from Allied Devices Corp., Baldwin, N.Y. Allied Devices is a leader in the contract manufacturing of such devices. To provide the reader with an understanding of Allied's integrated approach, the brochure features eight completely different mechanical assemblies. It describes the engineering, prototyping, manufacturing, testing, and documentation requirements of each assembly. It also highlights production lot sizes, scheduling, material, and assembly details for each of the eight examples. The result is a comprehensive understanding of the company's engineering and contract-manufacturing capabilities. To receive a free copy of the brochure, call Allied Devices at (516) 223-9100, or fax (800) 338-4232. LM

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CIRCLE 571

One-Piece Optical Components All In One Brochure

A new brochure from Opticon Corp., N. Billerica, Mass., describes a wide range of optical components that feature monolithic structures with integral mounts. These streamlined components ease assembly, and reduce weight and other design restrictions. The Opticon Superior Optical Components brochure details the company's

ability to fabricate metal, ceramic, and composite optics into one-piece designs that eliminate separate mounting structures. This makes the components lighter, thermally stable, and more rigid. Custom engineering capabilities and examples also are discussed. The categories of optics included in the six-page publication include flat, spherical, and aspheric optics; telescopes; and microscope objectives. For more information about the free brochure, call (508) 663-6105. LM

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Tune Into High-Speed Digital Radios And Modems

SiCOM Inc., Scottsdale, Ariz., is offering a six-page brochure that outlines the company's low-cost, high-speed digital communications products based on a breakthrough DSP technology. The brochure highlights SiCOM's advances in very-high-speed digital radios and modems; interference-tolerant HF, VHF, and UHF digital radios; and the custom ASICs that drive these products. Four datasheets serve as a supplement to the brochure. The datasheets detail the company's radios, transceivers, modems, and ASICs. For free copies of the brochure or datasheets, call (602) 483-2867, ext. 269; fax (602) 483-7986; or e-mail: info@sicom.com. LM

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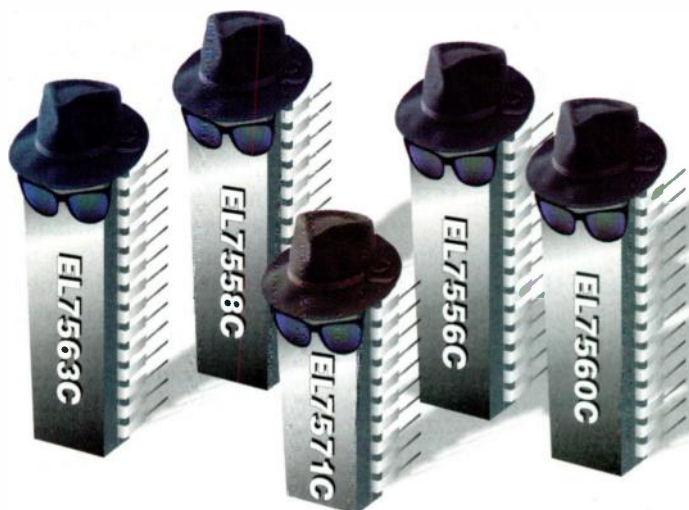
Suck Up The Facts About A New Compact Vacuum Pump

A four-page brochure from Stokes Vacuum Inc., Philadelphia, Pa., describes the company's new compact pumping system for semiconductor production. The Stealth Pump is a compact vacuum pumping system with a very small footprint. The pump is a clamshell design with a water jacket for cooling, and has no heat exchangers. Included in the brochure are performance curves, specifications, and drawings of all available models. For more information about the free brochure, call Stokes at (215) 831-5400, or fax (215) 831-5420. LM

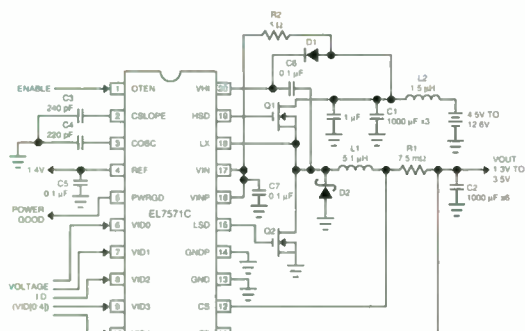
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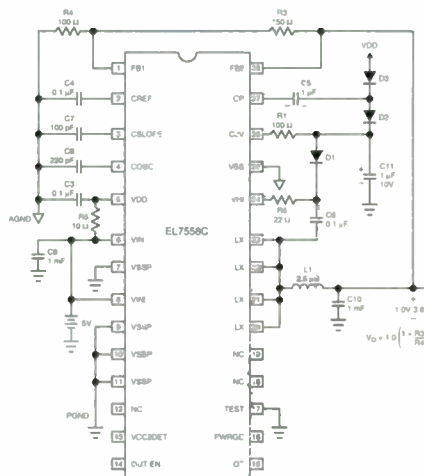
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Issuing A Wake-Up Call

Re: Your July 7 Editorial (*"The Future Is (Almost) Here,"* p. 14):

You are most certainly correct in your assessment of our institutions. I will never forget the business major in my college that us engineers helped tutor because he had managed to graduate high school without learning algebra! (In fairness to the U.S., he WAS from Canada.)

I would also assert (with many learned scholars) that our success here in the U.S. was started by the World War II veterans who entered college on the G.I. Bill, but it was SUS-TAINED by the massive math and science push during the '60's fueled by Sputnik and the Cold War. After reaching the moon and the '70's, this was allowed to decay, and we now have scientifically illiterate teachers graduating illiterate students and Martian rocks named Barnacle Bill.

Let me give you an example—the retired couple in Florida who taped U.S. Representative (and Speaker of The House) Newt Gingrich on their cellular phone. The illiterate media didn't know to ask if it was even legal to tape record a phone conversation (FCC law); that monitoring two sides of a cell-phone conversation requires TWO receivers, probably controlled by cell-phone hardware if anyone changed cells; and that there were very few scanners ever sold in the U.S. that could pick up 900-Mhz band. Result? News, broken laws, and no hard questions.

Tim Wolf

trw90@juno.com

Inspiring Kids To Be Engineers

I just finished reading your July 7 editorial and I must say that I wholeheartedly agree with what you are saying about our lack of dedication toward the education of grades K through 12. However, I wish that you would also bring up the fact that there aren't enough engineers going out to schools and speaking to our grade- and high-school kids to inspire them to science and mathematics as a career.

Not long ago, I went back to my old high school and gave a speech to the tenth-grade kids in a minority engineering program. I spoke to them about what we do as engineers and the type of things they should be prepared

for in studying to become an engineer. I raised some huge interests when I started to bring on topics that involved most of the kids in the class: "How do pagers and cellular phones really work?" Half of the kids in the class had a pager or cell phone, but only one really knew how it worked to a certain extent.

My hope is that you would encourage more engineers and industry leaders to volunteer their time to speak to our next generations in order to spark their interest in the science and mathematical fields. Back when I was in middle school, an engineer came in from Boeing and told us that they were looking for a lot of engineers, and they also make a lot of money. But that never interested me very much, let alone allowed me to understand what an engineer does. It's almost like a secret "Nerd" society where people don't have the same kind of respect for the profession like they do for lawyers and doctors.

John Ling

jling@eng.claircom.com

The Solutions Are The Problems

When I first read your July 7 editorial, I was mildly worried about the "problem" reported therein—that being "concerned about our ability to replenish our technological brain trust."

As I continued reading, however, I became increasingly horrified—not by the problem that you reported, though. Rather, the things I find alarming are the problems that you do not report, and the "solutions" that you appear to endorse.

You may make an observation that the Council on Competitiveness is nonpartisan and nonprofit. That, however, does not mean that it lacks an agenda. I have found "business, labor, and university leaders" (no parents were included in the "forum," I note with some sadness) to be flush with agendas of all sorts—few of them contribute to the general good.

You also point out that the children you employed as examples are not in need, due to "the good fortune" they had which was "more than most kids" receive. This good fortune consisted of their own curiosity and the willingness of adults to satisfy their curiosity. Those things are hardly inventions of this generation. Will children cease to

be curious about engineering, and adults lose the desire to explain things to curious children, unless some central authority (excuse me, I meant to say "partnership") assures that they continue?

Besides, your suggestion that partnerships be formed involving governments is so nonsensical as to be frightening. How, exactly, is a "partnership" to be formed between someone who can be put in jail and the one who can jail him? A .44 magnum always beats four aces.

We may indeed be facing a current of future paucity of engineers. However, the idea that the marketplace must not be left alone to address a temporary shortage, but must instead be "managed" by those who "know best" to produce (it is hoped) the same result, is an example of the kind of thinking that has led to the very difficulty you employ it to address. This kind of thinking has made the U.S. the most schooled and least educated country in history, and the longer it holds sway, the less likely we will be to right ourselves.

Chuck Kriel, PhD

chuck@dtc.net

QVC, HSN, WWW?

I recently read your June 23 editorial (*"There's No Business Like Web Business,"* p. 14) and I wanted to let you know that I currently don't buy anything on the Web. But one thing I often do is search for parts, availability, pricing, products, and technical info. We must realize that few people are actually buying over the Internet, but we must admit that more people will do it as more security is added (not just firewalls, but user-ID numbers). I believe that in a few decades (say 20 years, if there's nothing better than the Internet by then), millions of people will be purchasing on the Web.

Vincent Hunter

vhnuter@comlab.com

Letters to the Editor, including the writer's name, address, and daytime phone number, should be sent to: Letters Editor, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604; fax (201) 393-0204; e-mail: mikemea@class.org. Letters may be edited for space and clarity. Names will be withheld upon request.

EE CURRENTS & CAREERS

■ Exploring employment and professional issues of concern to electronic engineers

Information Technology Shortages Could Be Less Dire Than Predicted

Robert A. Rivers

According to a recent study and report from the Information Technology Association of America (ITAA)¹, the future for companies seeking to hire information technology (IT) workers in the next few years looks bleak. It concludes that employers will face shortages of 191,000 IT professionals in the coming years. The ITAA report is not unlike one in 1990 by the Policy Division of the National Science Foundation that predicted a shortfall of 700,000 engineers and scientists by the turn of the century. For engineers and IT professionals, the question is, can you rely on these types of reports to make career decisions?

One problem with such reports is

the methodology used to make the predictions. They peer so far into the future that their forecasts cannot possibly account for the rapid changes taking place in technology and in society as a whole. For example, the National Science Foundation report did not foresee a dramatic loss of 435,000 engineering jobs in the early and mid-'90s as the economy struggled through a recession and subsequent recovery. Nor did it anticipate the downsizings, consolidations, mergers, and buyouts so prevalent in this decade that often result in job losses.

The ITAA report is not without its biases with respect to the survey data and the methodology used to project a shortage of 191,000 IT workers. This

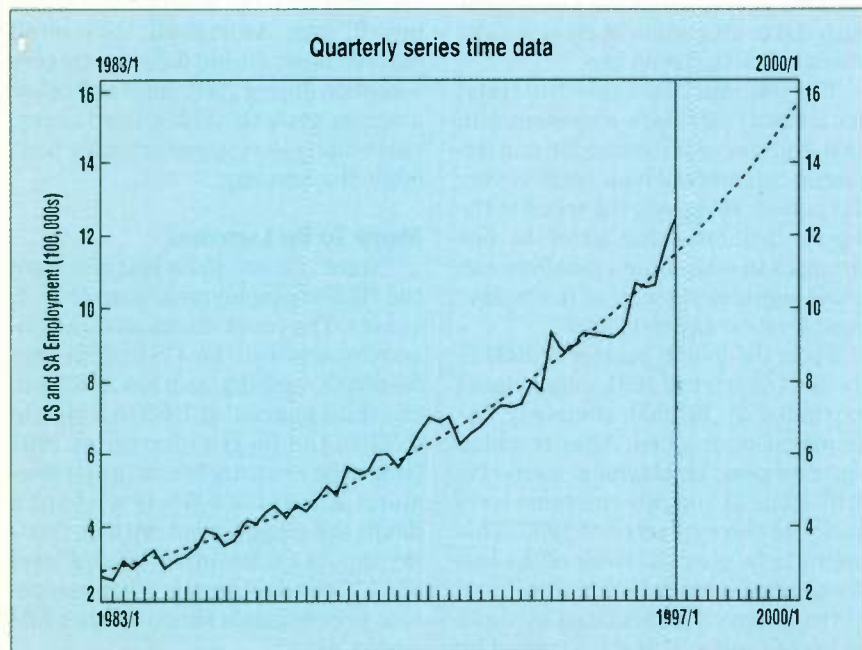
large number was derived from an extension of responses from 149 out of 1000 IT companies and 122 out of 1000 non-IT companies. There was an average projected vacancy level of 33 positions per IT employer and between 4 and 5 per non-IT employer. Multiplying these figures out gives survey counts of 4917 for IT employers and an estimated 549 for non-IT employers for a grand total of 5466 vacancies.

This small number of responses makes it probable that the survey had a significant bias. In fact, the ITAA's statistical consultant called attention to the low response as a likely bias. In addition, their failure to statistically validate any follow-up survey and how the extension from 5466 to 191,000 was arrived at should raise a few eyebrows. There are other problems with the methodology so that only the 5466 vacancy number can be accepted from the ITAA report.

A specific problem is that vacancy data from employers is only a small part of the information necessary to determine supply-demand imbalances. For example, the number of applications was not supplied nor was the number of individuals interviewed. The number of offers made and at what salary levels is important data also not provided in the ITAA report. The number of hires is a key statistic as is the number of reductions in workforce and the people who leave voluntarily, but none of this information was provided in the report. Vacancies can be deceiving and can balloon if employers offer lower salaries, so they should not be taken as an indicator of real demand.

The Big Picture

The fact is that IT is becoming increasingly important and growing



1. U.S. Bureau of Labor Statistics data for employment of Information Technology professional workers over a 14-year period shows a rapidly rising exponential growth rate or trend line (dashed line). The actual number of jobs at any given time is shown by the solid curve that overlays the trend line. Note that the data are projected out to the year 2000.

faster than most other areas of technology. From the first quarter of 1983 to the first quarter of 1997, the Bureau of Labor Statistics (BLS) of the U.S. Department of Labor reports that employment in two main categories of IT, Computer Science (CS) and Systems Analysis (SA), has grown from 260,000 to 1,258,000 (*Fig. 1*). When combined with computer programmers, total IT employment is almost as large as that of all the engineering specialties.

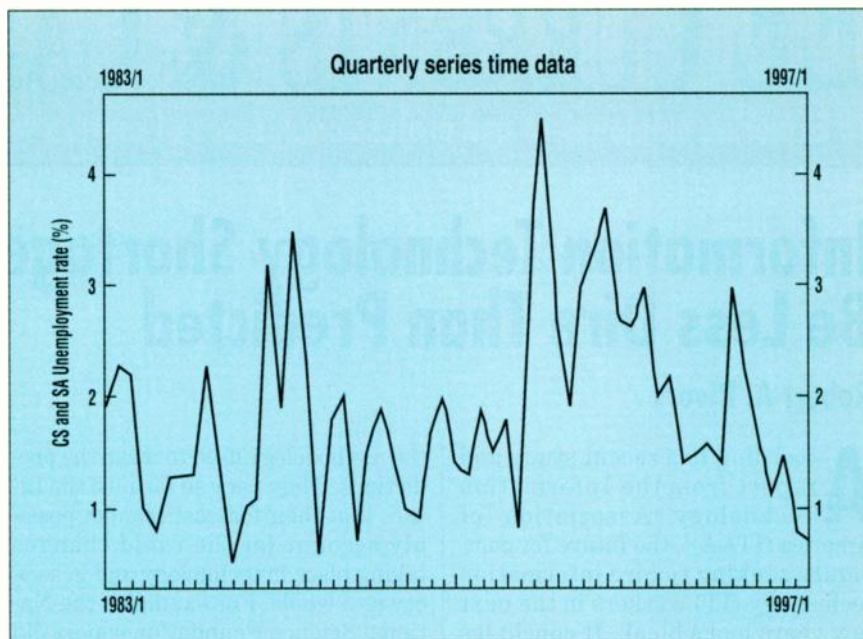
Will there be continued growth in IT? Looking at the past history of CS and SA employment, the trend line in Figure 1 shows that growth has been exponential and is rising at a rate of 10.69% per year. The actual data—number of jobs held—exceeds the trend line in some years and falls below it in others, as is to be expected. Both the trend line and deviations from it are important indicators of what has been happening in IT employment and what will likely happen in the future. Both of these attest to the fact that growth will continue until the turn of the century.

Note that the trend line is plotted to the first quarter of the year 2000. The importance of the trend line is that it represents a massive momentum for growth. Major influences are necessary to change a trend. The trend line is the central tendency of the forecast around which subsequent data will fall.

Despite the major trend for IT growth, there are periods when the number of real jobs held fall below the trend line quarter after quarter. One such period was the fourth quarter of 1991 until the fourth quarter of 1993. Between the third and fourth quarters of 1991, CS and SA employment fell by 80,000 workers. After that market adjustment, employment grew but did not recover to the trend line until the fourth quarter of 1993.

Down To Details

In addition to employment statistics, the BLS keeps unemployment data on the IT market (*Fig. 2*). The data shown covers the same period as the employment data in Figure 1 and shows a great deal of volatility. Part of this is due to the BLS survey rotation of their household sample, but the other part is real. The high point in terms of unemployment is the fourth



2. Unemployment data for Information Technology workers over the same 14-year span as in Figure 1 illustrates some wild swings over the years. The high point for unemployment at 4.5% was reached during the fourth quarter of 1991, a time that the country was mired in a recession. The average rate, however, over the time period is about 2%.

quarter of 1991, which shows a peak unemployment rate of 4.5%. That rapid increase in unemployment is a direct reflection of the fall in employment by 80,000 between the third and fourth quarters of 1991. Note also that the unemployment rate remained high for two years following consistent with the continuation of employment levels below the trend line.

The continuation below the trend line for two years also is consistent with an extension of the recession and declining commercial loan volume over the period. However, the trend is the major influence for growth, but changes in economic variables can cause significant changes in employment levels at any given time.

From the fourth quarter of 1993 to the first quarter of 1994, employment expanded by 163,000; obviously, unemployment dropped. After reaching that new peak, employment seemed to drift along at roughly the same level until the third quarter of 1995. This seems to be characteristic of the last few years; periods of calm, slow, or no growth activity punctuated by rapid hiring of people. This is illustrated by the rapid expansion of employment between the third quarter of 1995 and the first quarter of 1996 when employment again moved sharply upward at

the rate of 148,000 new jobs.

But between the first and third quarters of 1996, a relative calm settled in, with job gains flattening out. Then beginning in the third quarter of 1996 and continuing through the first quarter of this year, a significant expansion occurred with the addition of 194,000 new IT jobs. As a result, the overall pattern is expansion followed by consolidation during good times and below average growth during hard times, particularly during recessionary periods in the economy.

More To Be Learned

There is more to be learned from the BLS unemployment data (*Fig. 2, again*). The curve shows that the unemployment rate for CS and SA professionals varied from a low of 0.5% in the third quarter of 1985 to a high of 4.5% in the fourth quarter of 1991 (when the economy was in deep recession). A level of 0.5% is without a doubt full employment with no floating supply. On the other hand, a level of 4.5% denotes a crisis when competent professionals simply cannot find employment.

Over the 14-year period covered by the curve, the mean unemployment rate is 1.912% with a standard deviation of 0.894. This means that 62% of

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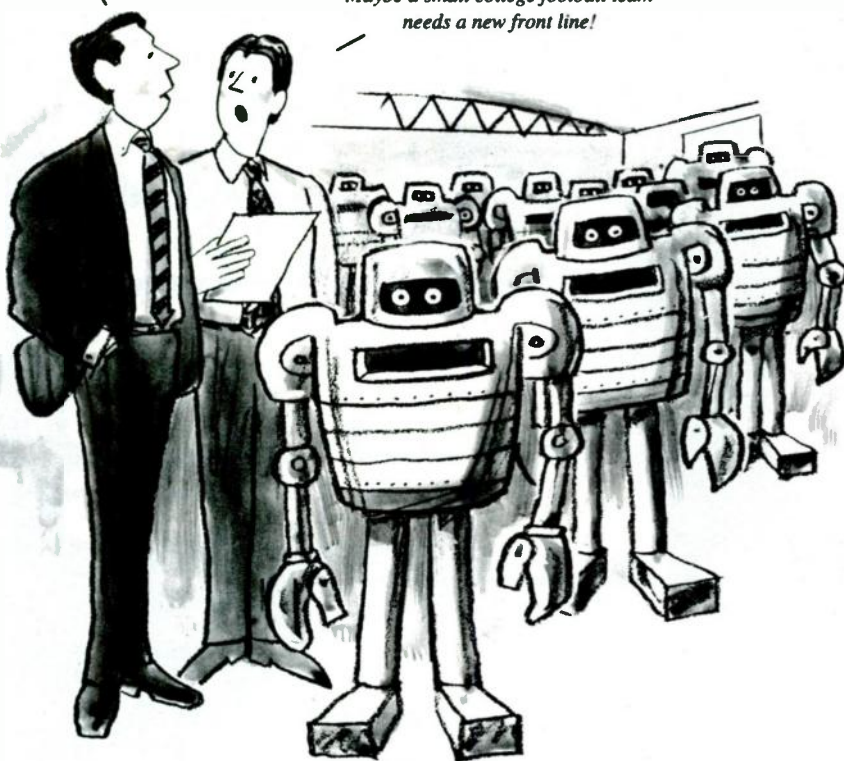
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the time, the unemployment rate is between 1.018% and 2.806%. Of course, you can't compare the unemployment rates of professional and technical workers to the rate for the population as a whole. CS and SA workers are a subset of the professional and technical group that has experienced above average growth and high demand over much of the 14-year period of the BLS data. Thus, a 6% or 7% unemployment rate for the general population might correspond to a 2% rate for IT workers.

Unemployment above the 3% level was experienced in 1986 as a result of a slowdown in the economy triggered by actions of the Federal Reserve Board, the group that sets interest rates for the U.S. banking system. Again in 1991, high rates contributed to the record unemployment rate of 4.5% for IT workers. Recovery from the last recession brought unemployment levels down to 0.8%, virtually full employment for the IT profession.

The forecast for IT employment—CS and SA workers—for the year 2000 is 1,575,000 workers, following the growth trend of 10.69% per year. Going through the '90s, the absolute volatility is getting greater and the employment increases also are growing. In the first quarter of this year, the volatility is estimated to be 8%, leading to a potential variation in employment of 126,000 above or below the trend line forecast for the year 2000. But watch for Federal Reserve Board actions that could slow the economy and slow the rate of IT employment growth. Continuing high levels of venture capital investment and public offering financing will cause the growth rate to go above the trend line.

References:

1. Miller, Harris N. "Help Wanted: The IT Workforce Gap At The Dawn Of A New Century," Information Technology Association Of America, Arlington, Va.

Robert A. Rivers is a consultant specializing in engineering and IT manpower issues, and is publisher of the Engineering Manpower Newsletter. He can be reached at (508) 544-3942; e-mail: engineermanpowernews@webtv.net.

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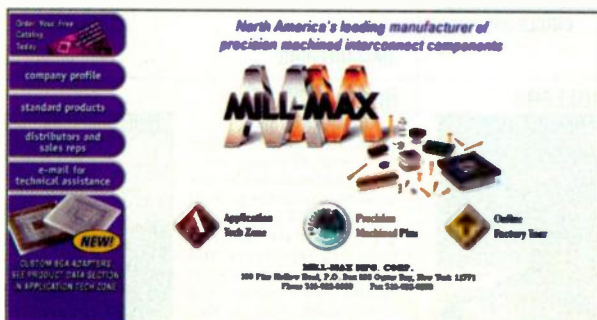
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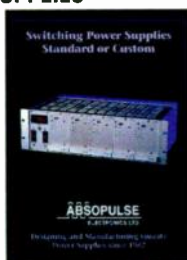
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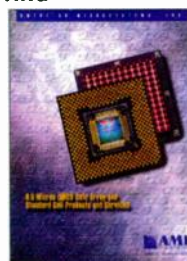


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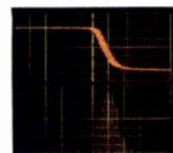


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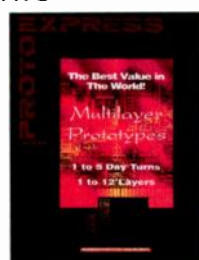


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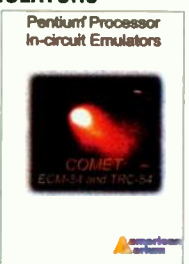


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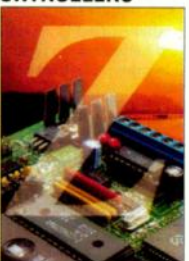


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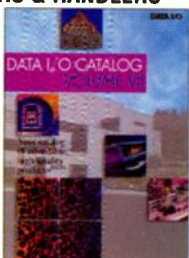


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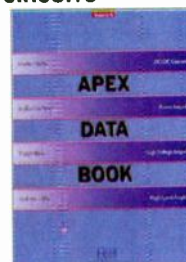


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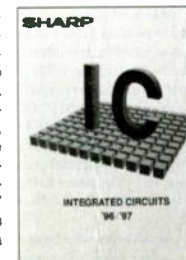


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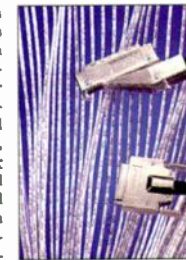
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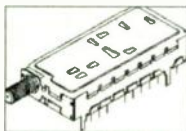
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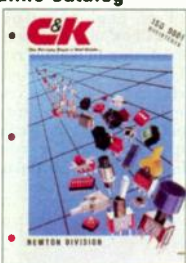


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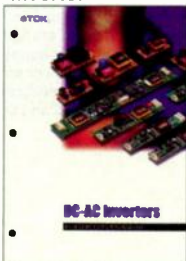


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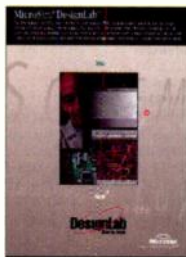


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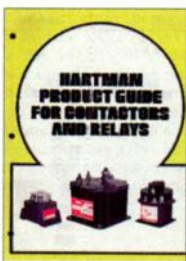


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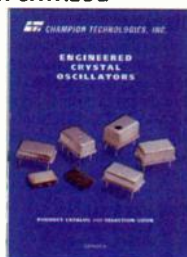


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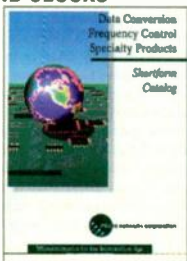


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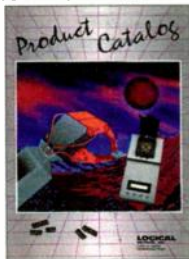
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MICRO NETWORKS CORP.

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Product Literature News Announcement

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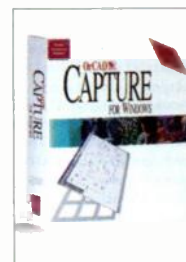


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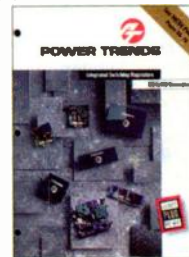


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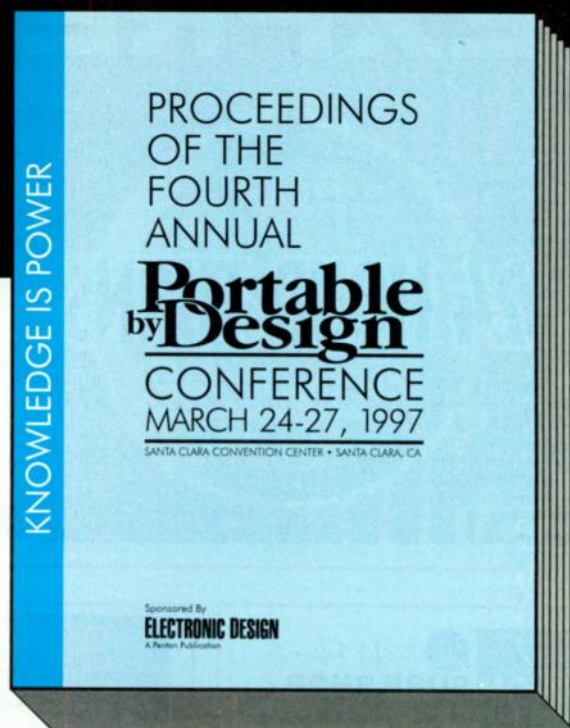


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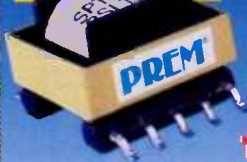
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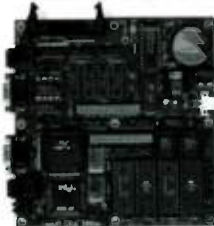
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INDEX OF ADVERTISERS

Advertiser	RS #	Page	Advertiser	RS #	Page
A/D ELECTRONICS	327	198	MICROSIM CORPORATION	300	35
ABSOLUTE	250	198	MICROTEC INC.	287	200
ACCUTRACE INC.	411,251	204,198	MICROTEK INTERNATIONAL	312	202
ADVANCED MICRO DEVICES	238	26-27*	MILL-MAX MFG CORP.	274	199
ADVANCE POWER INC.	126	800*	MINC INCORPORATED	170	89
ALLIED ELECTRONICS	127	21	MINI-CIRCUITS	164-165	Cov3
ALLEGRO MICROSYSTEMS	127	175	MINI-CIRCUITS	166-167	4
ALTERA CORPORATION	128	Cov2,1	MINI-CIRCUITS	168-169	164
AMERICAN AIRLINES	77		MIPS TECHNOLOGY	204	22-23
AMERICAN ARIUM	271	199	MODEL TECHNOLOGY INC.	254,290	198,201
AMERICAN MICROSYSTEMS	258,316	198	MOTOROLA MICROCOMPUTER	230	53
AMPHENOL INTERCONNECT	248	200	MOTOROLA SEMICONDUCTOR	-	59
ANALOG DEVICES	-	136	MULTIDYNAMICS, INC.	261,303	187
ANALOG DEVICES	-	39	NATIONAL INSTRUMENTS	172	198,202
APEX MICROTECHNOLOGY	284	200	NATIONAL INSTRUMENTS	-	180
APPLIED MICROSYSTEMS	308	202	NATIONAL SEMICONDUCTOR	-	8
ARIES ELECTRONICS	129	115	NEC ELECTRONICS	245	121
AROMAT CORPORATION	241	117	NEC CORPORATION	171	128-129
AUDIO PRECISION	131	179	NEEDHAMS ELECTRONICS	174	183
AVX CORPORATION	132	67*	NIPPON ELECTRIC	205	70-71
AVX CORPORATION	132	105**	NKK SWITCHES	-	120
BULEY ELECTRIC CO	97	108	NOHAU CORPORATION	401	205
BURR-BROWN	350-361	43	NORLAND PRODUCTS INC.	307	202
BURR-BROWN	82	45	OCTAGON SYSTEMS	402	204
BURR-BROWN	88	47	OKI SEMICONDUCTOR	206	14-15*
BURR-BROWN	362-365	49	OMRON ELECTRONICS	118,291	80H*,201
C & K COMPONENTS INC	297	201	ONTIME ELECTRONICS	283	200
CADSOFT COMPUTER INC	302	202	ORCAD SYSTEMS	311	202
CEDKO ELECTRONICS	412	204	OTTO CONTROLS	299	201
CELESTICA INC.	133	95	OVERNITE PROPOS	403	203
CESIWID INC.	329	199	PACIFIC SOFTWARES	404	203
CHAMPION TECHNOLOGIES	294	201	PENTEK INC.	246	84
CHERRY SEMICONDUCTOR	108	80F*	PENTON	176	80EE*
CIRCUIT COMPONENTS	413	203	PHILIPS SEMICONDUCTOR	178	63
COILCRAFT	136	109	PHILIPS SEMICONDUCTOR	207	54-55**
COMM CON CONNECTORS	134	110	PICO ELECTRONICS	104	20-38
CONEC CORP.	135	80G*	POTTER & BRUMFIELD	179	80K*
CONVERSION DEVICES	122,292	80J*,201	POWER-ONE INC	309	159
CYBERNETIC MICRO SYSTEMS	98	18	POWER TREND	309	202
CYPRESS SEMICONDUCTOR	-	172	PRECISION INTERCONNECT	181,285	96,200
DALLAS SEMICONDUCTOR	137	19	PREM MAGNETICS	405	205
DATA I/O CORPORATION	264	199	PROTEL TECHNOLOGY INC.	296	201
DATAMAN	282	200	PROTO EXPRESS	414,257	203,198
DELTRON INC.	231	186	PURDY ELECTRONICS	105	12
DIGI-KEY	138	11*	QT OPTOELECTRONICS	182	6
DPA SOLUTIONS INC.	139	125	RALTRON ELECTRONICS	106	106
DY 4 SYSTEMS INC.	140	157	RLC ENTERPRISES	415	205
E-SWITCH	93,310	186,202	RO ASSOCIATES INC.	92	153
EAGLE PITCHER INDUSTRIES	234	76	ROLYN OPTICS	266	19*
ECLIPTEK CORPORATION	277	200	SAMSUNG SEMICONDUCTOR	208	14-15**
ELANTEC INC.	141	191	SAMSUNG SEMICONDUCTOR	209	32-33**
ERG INC.	281	200	SAMSUNG SEMICONDUCTOR	115	80B8CC*
FAIRCHILD SEMICONDUCTOR	330	200	SAMTEC INC.	183,313	133,202
FAIRCHILD SEMICONDUCTOR	143	9	SANTO DENKI	183	19*
FAIRCHILD SEMICONDUCTOR	144	9	SGS-THOMSON	141	80T.V*
FORCE COMPUTERS	147	37	SHARP MICROELECTRONICS	288,289	200,201
FOTRON SOURCE	235	154	SHARP MICROELECTRONICS	229	80X 9*
GENERAL DEVICES COMPANY	99	80P*	SHINDENGEN AMERICA	185	80M*
GESPAC INC.	146	91	SIEMENS COMPONENTS	187,188	69,80AA
GO DSP	100	12	SIGNAL TRANSFORMER	247	24
HARRIS SEMICONDUCTOR	147	107	SIGNATEC	408	205
HEWLETT-PACKARD	242	13	SIGNUM SYSTEMS	406,265	203,199
HEWLETT-PACKARD	370	105*	SIMEX CORPORATION	328	199
HITACHI SEMICONDUCTOR	141**	186	SIMEX CORPORATION	318	30
HITACHI SEMICONDUCTOR	148	80E*	SPECIALIZED PRODUCTS	279	201
HITEX-SYSTEMTECHNIK	101	94**	STANFORD RESEARCH SYSTEMS	276	200
HYUNDAI ELECTRONICS	203	26-27**	STEWART CONNECTOR	189	74-75
HYUNDAI ELECTRONICS	113	54-55*	SYNERGY SEMICONDUCTOR	276	198
HYUNDAI ELECTRONICS	202	68-69**	T-CUBED SYSTEMS	190	123
ICP ACQUIRE INC.	263	199	TALLA-COM	190	123
ILC DATA DEVICE CORP	111-112	78	TANNER RESEARCH	270	199
ILLINOIS CAPACITOR	110	80L*	TOK CORPORATION	301	201
IMAGING INC.	260	198	TECHRON INDUSTRIAL	237,298	124,201
IMAGING INC.	123,325	180,202	TECCOR ELECTRONICS	238	122
INNOVATIVE INTEGRATION	400,267	204,199	TEKTRON MICROSYSTEMS	107	108
INTEL	-	2-3	TELEDYNE RELAYS	191	11**80I*
INTERACTIVE IMAGE	149	41	TELONE	269	199
INTERFACE TECHNOLOGIES	293	201	TERN INC.	407,262	205,198
INTERNATIONAL POWER	150	131	TEXAS INSTRUMENTS	227	16-17
INTERNATIONAL RECTIFIER	151	93	TEXAS INSTRUMENTS	228	82-83
INTUSOFT	124-125	67**68	TEXAS INSTRUMENTS	369	80S*
IOTECH INC	320-326	80A-8*	TODD PRODUCTS	280	200
IRONWOOD	268	199	TOSHIBA AMERICA	-	80Q*
JANCO CORPORATION	102	114	TRACEWELL POWER	315	202
KEITHLEY INSTRUMENTS	317	201	TRANSISTOR DEVICES	192	126,189
KEITHLEY INSTRUMENTS	116,366	50-51	TROMPETER ELECTRONICS	89-90	127
KEMET ELECTRONICS	153	134	UNITRODE INTEGRATED	193,306	29,202
KENT DISPLAYS INC.	152,304	79,202	UNIVERSAL AIR FILTER	95,259	158,198
KEYSTONE ELECTRONICS	224	156,185	VALOR ELECTRONICS	194	119
KILOVAC CORPORATION	295	201	VICOR	195	87
LAMBDA ELECTRONICS	177	32-33*	VISHAY INTERTECHNOLOGY	196	113
LATTICE SEMICONDUCTOR	243	57	VIMETRO, INC.	197	151
LECKROY TEST & MEASUREMENT	252	198	VNIC	278	200
LINEAR TECHNOLOGY	61	Cov4	WESTERN DESIGN CENTER	272	199
LINEAR TECHNOLOGY	26	73	XANTREX	121	132
LINEAR TECHNOLOGY	-	64A-D	XENTEK POWER SYSTEMS	253	198
LINEAR TECHNOLOGY	-	80IJJ*	XICOR	117,286	143,200
LOGICAL DEVICES	301	201	XILINX	198	145
LUCENT TECHNOLOGIES	201	60-61	Z-WORLD ENGINEERING	410,274	203,199
LUCENT TECHNOLOGIES	130	39	Z-WORLD ENGINEERING	96	156
M-TRON INDUSTRIES INC.	94	158	ZANDAR TECHNOLOGIES	409	205
MASTER BOND	255	198	ZIATECH CORPORATION	199	155
MAXIM	154-155	101			
MAXIM	156-157	103			
MAXIM	158-159	167			
MAXIM	160-161	169			
MAXIM	162-163	171			
MEGATEL COMPUTER	103	80HH*			
MERITEC	305	202			
MICREI SEMICONDUCTOR	114	149			
MICRO NETWORKS	331	201			

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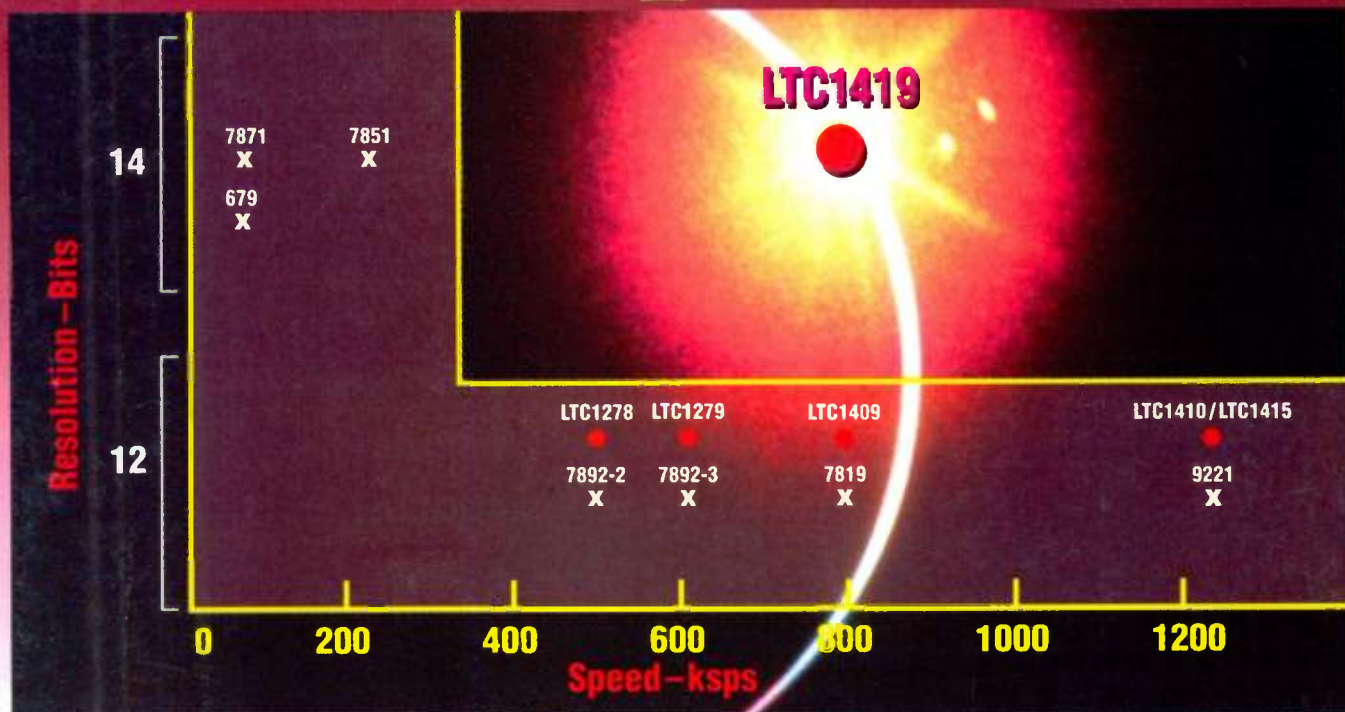
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