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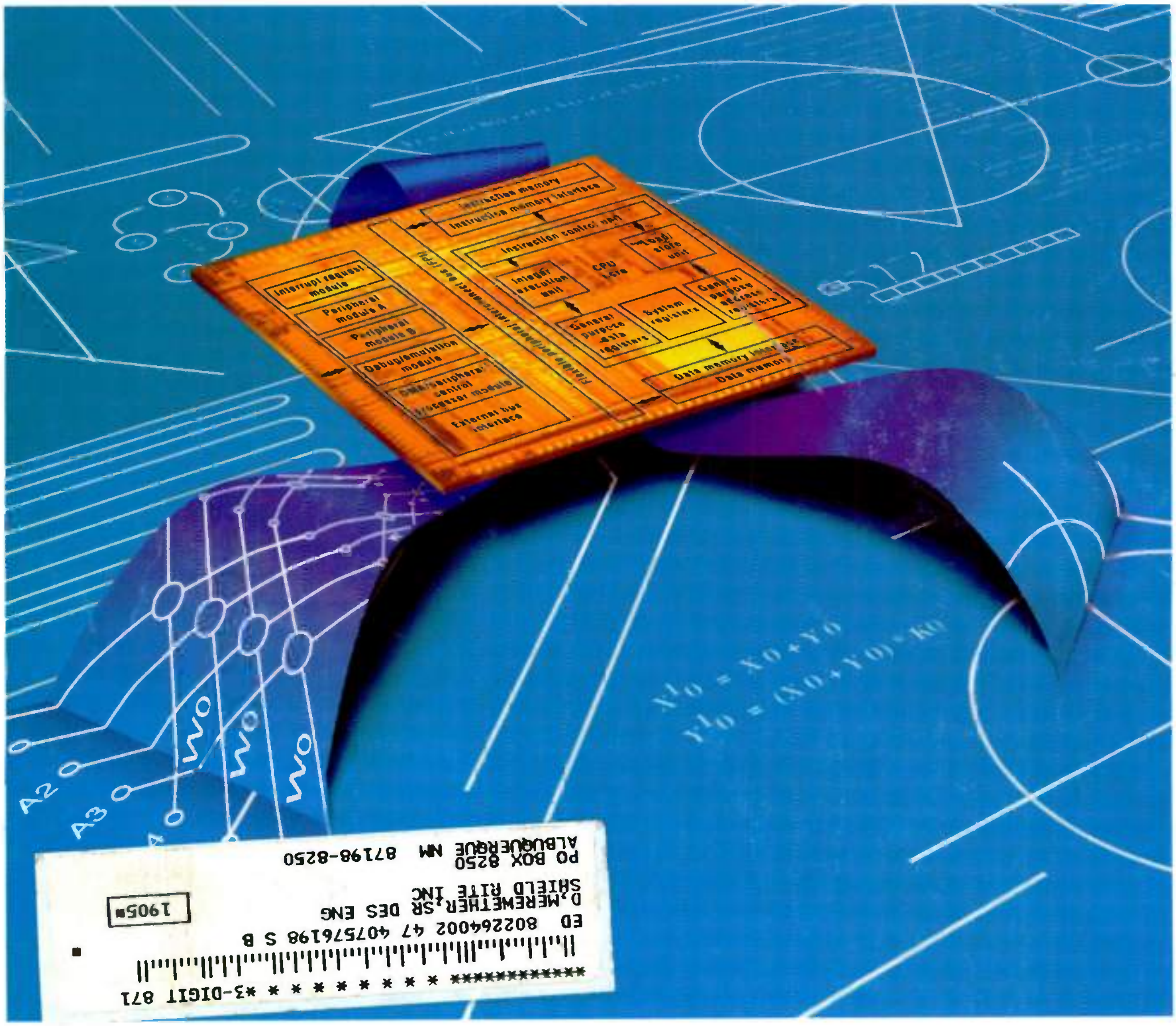
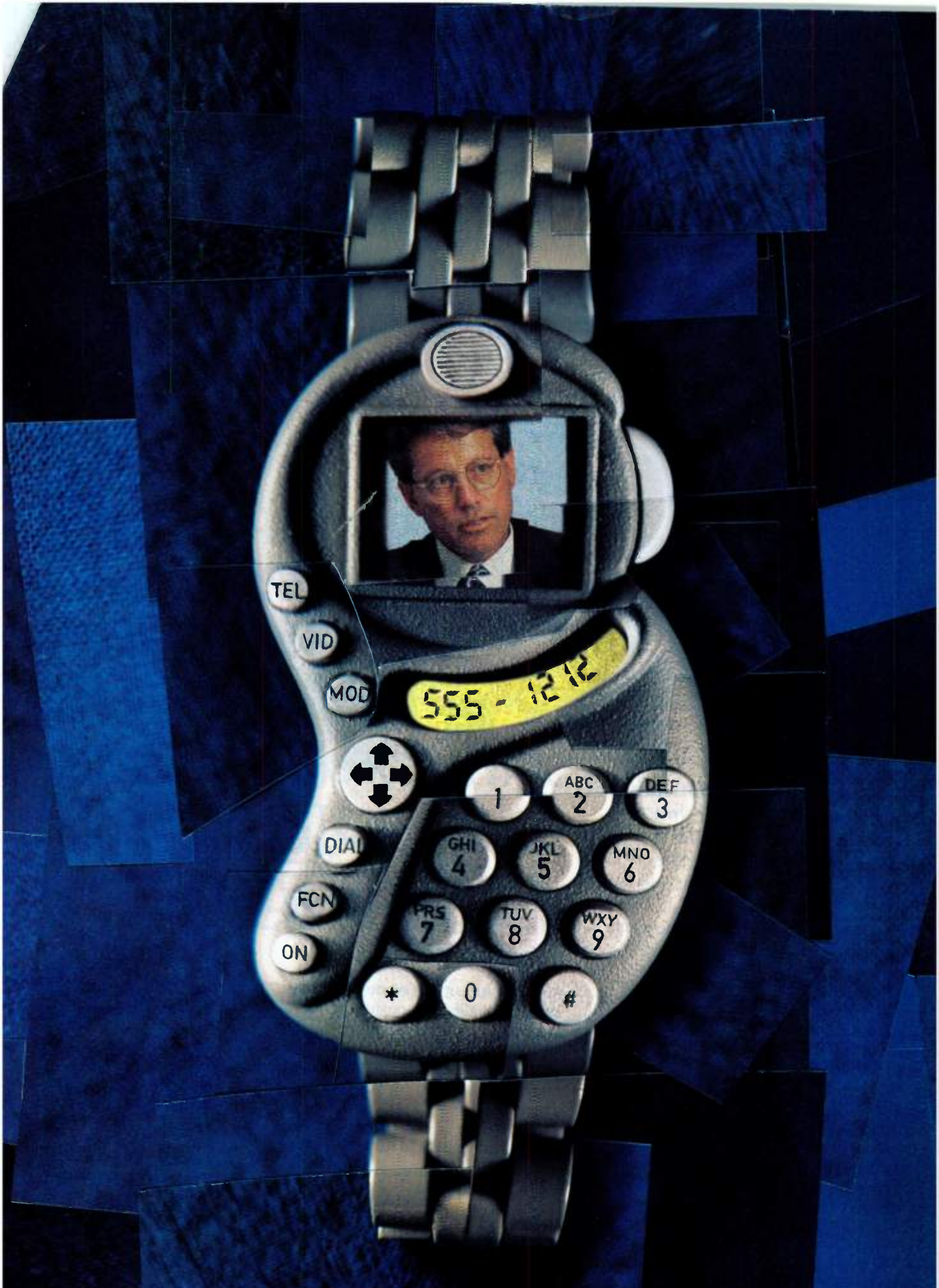


RISC Controller Merges DSP And Control Functionality p. 39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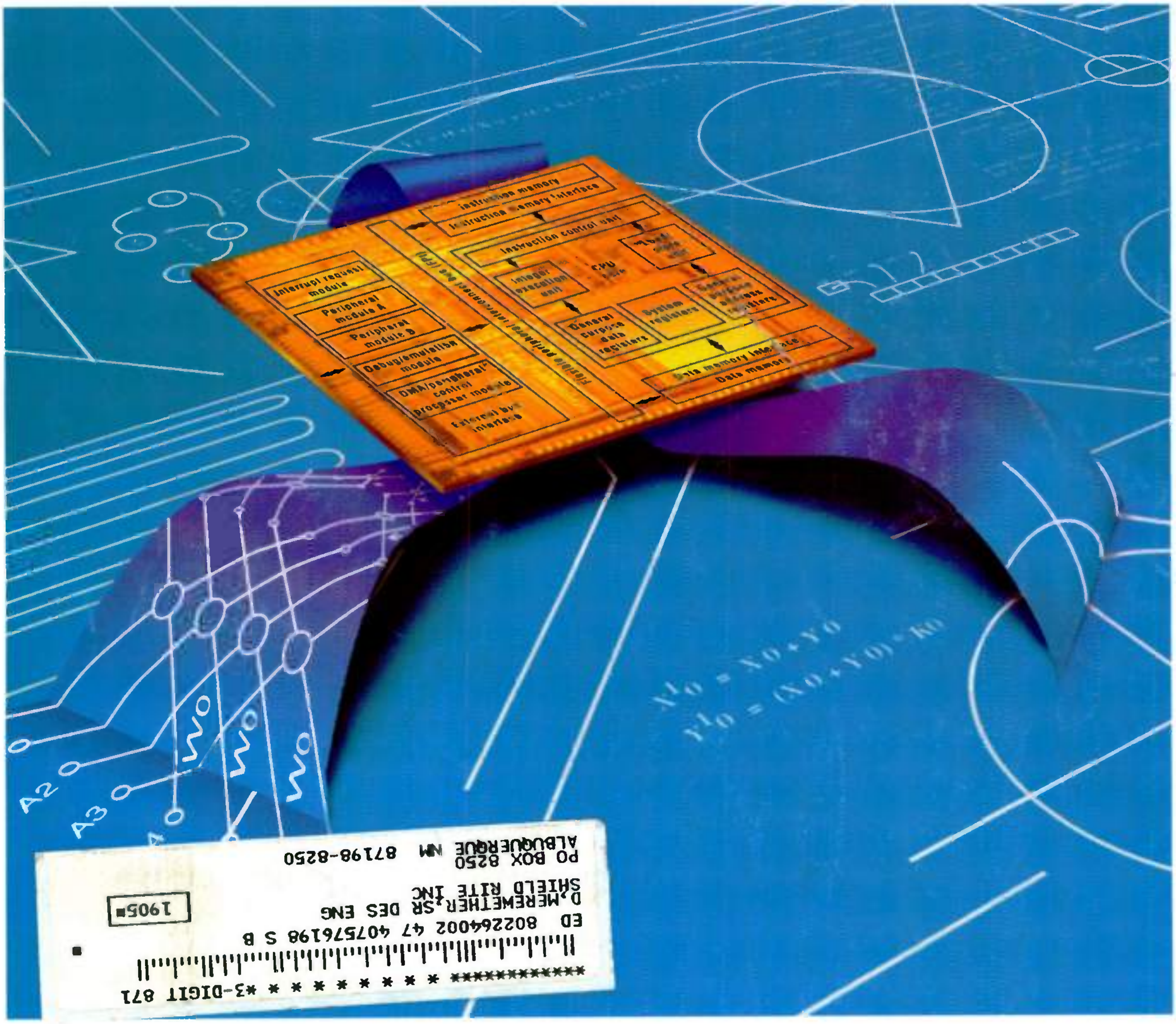

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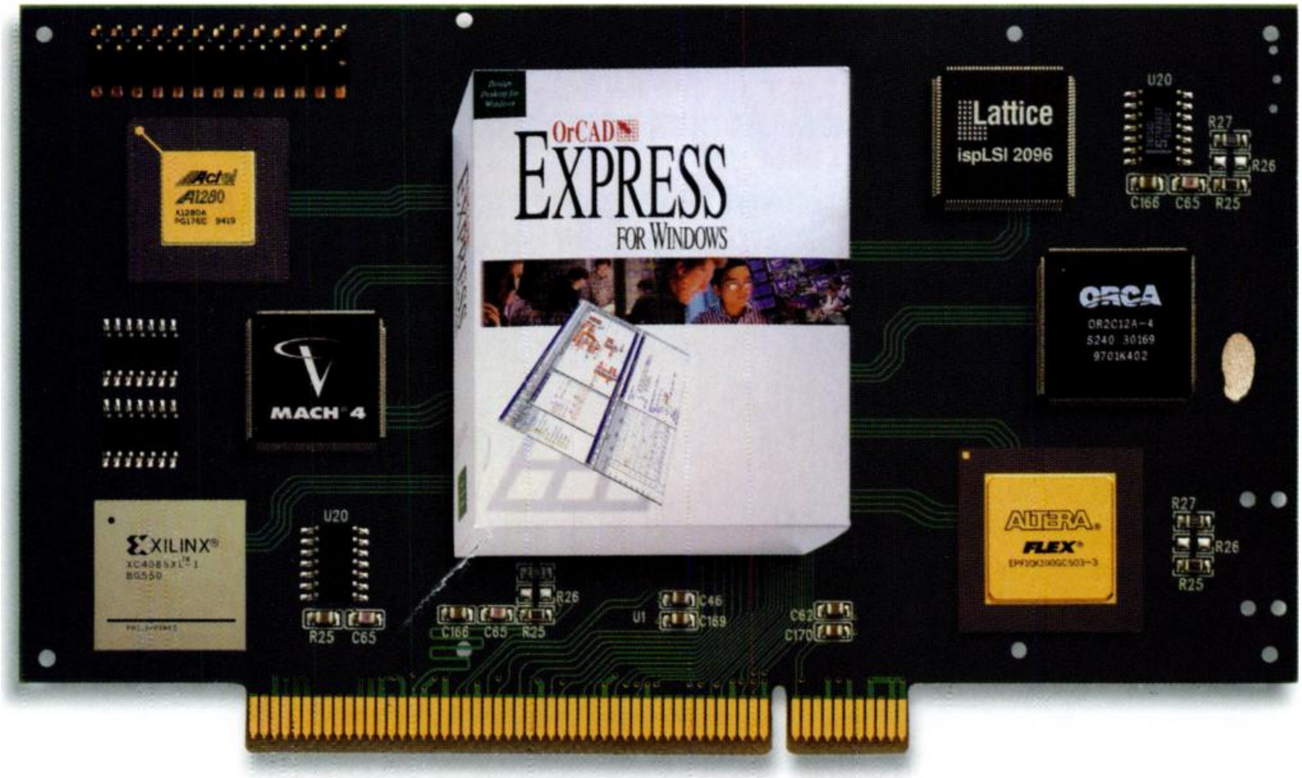

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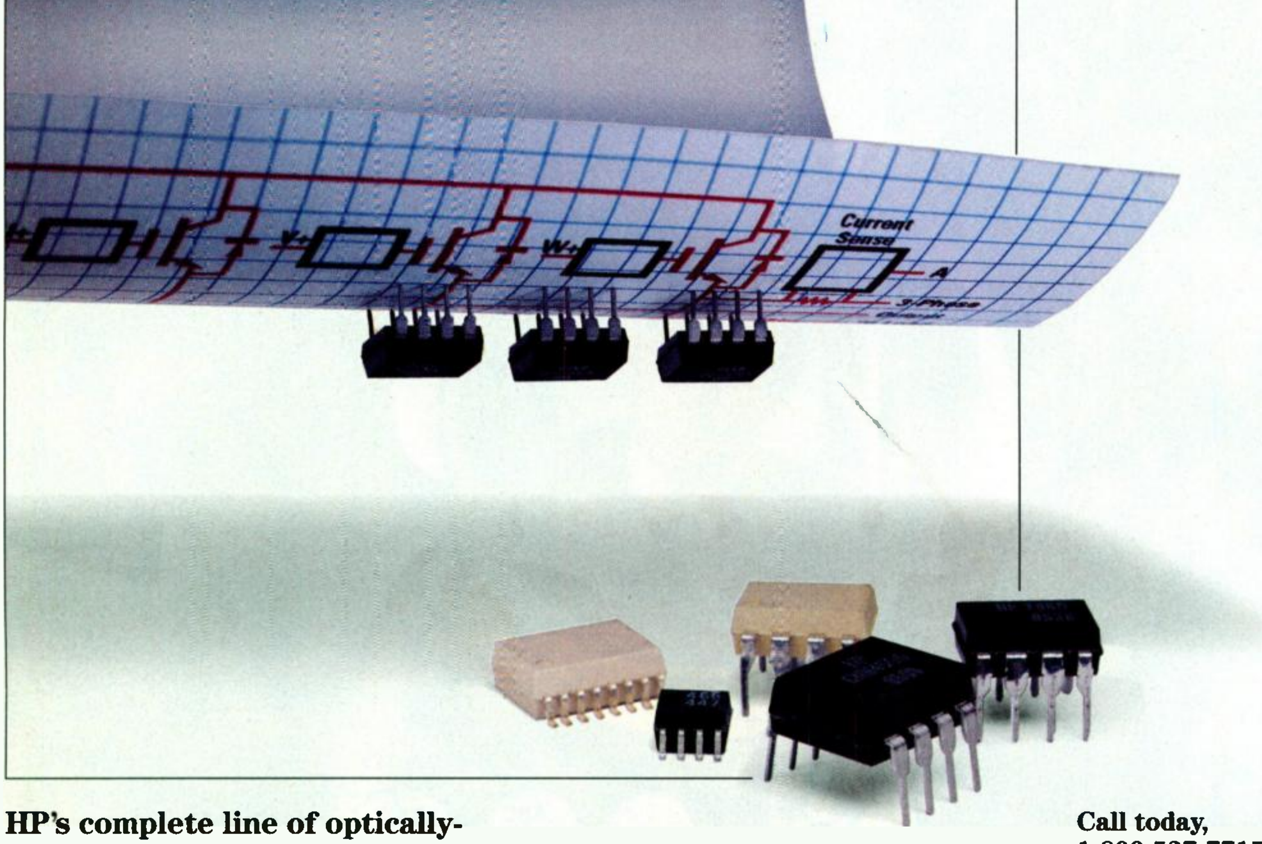

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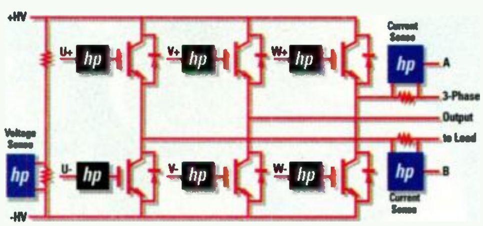

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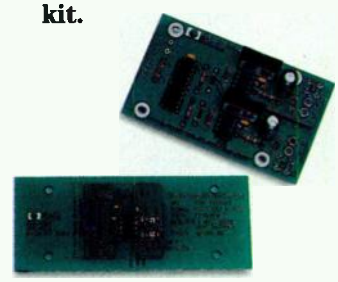

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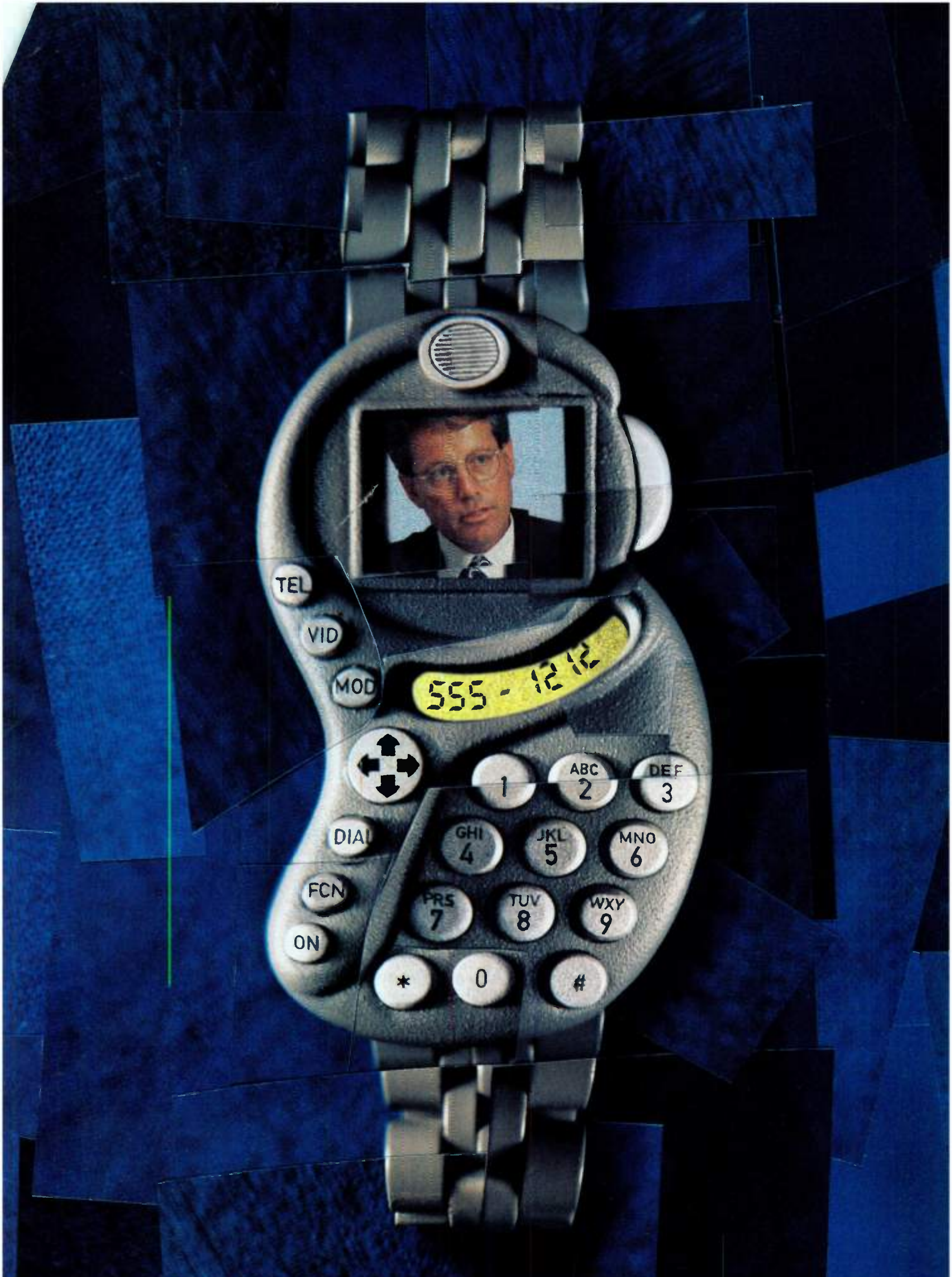
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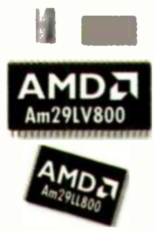

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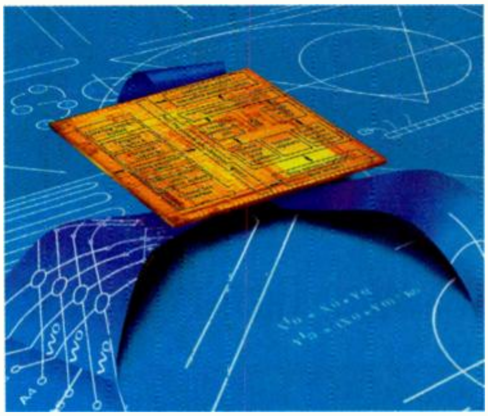

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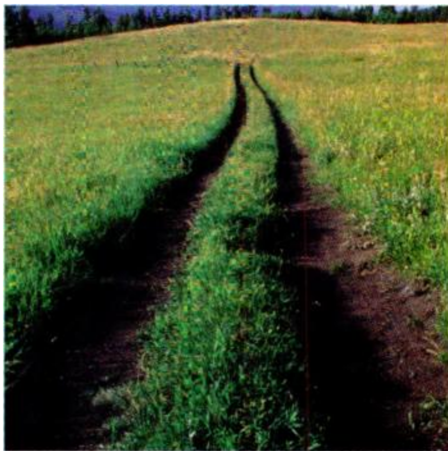

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QUICKLOOK

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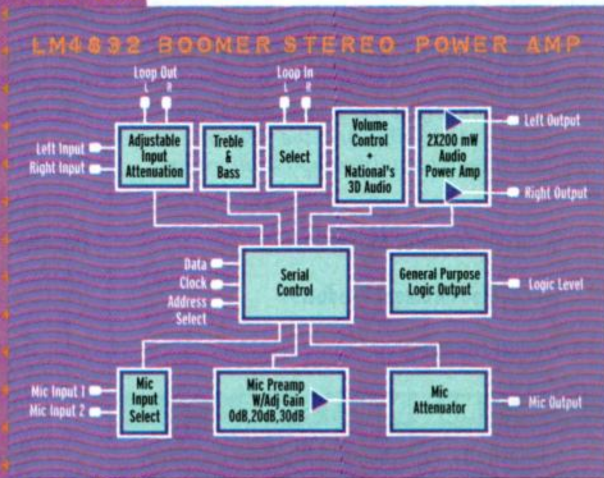

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Managing Editor: **BOB MILNE** (201) 393-6058 bmilne@class.org

Technology Editors:

Analog & Power: **FRANK GOODENOUGH** (617) 227-4388 75410.2361@compuserve.com
Communications: **LEE GOLDBERG** (201) 393-6232 leeg@class.org
Power, Packaging, Components & Optoelectronics: **PATRICK MANNION** (201) 393-6097 pcmann@ibm.net
Computer Systems: **RICHARD NASS** (201) 393-6090 richnass@class.org
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Editorial Headquarters:

(201) 393-6060 Fax: (201) 393-0204 E-mail: edesign@class.org
P.O. Box 821, Hasbrouck Heights, N.J. 07604

Field Correspondents:

West Coast Executive Editor:
DAVE BURSKY (San Jose) (408) 441-0550, ext. 105; dbursky@class.org
Western Regional Editors:
CHERYL J. AJLUNI (San Jose) (408) 441-0550, ext. 102; cjajluni@class.org
TOM WILLIAMS (Scotts Valley) (408) 335-1509 tomwillm@ix.netcom.com
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Chief Copy Editor: **MICHAEL SCIANNAMEA** (201) 393-6024 mikemea@class.org
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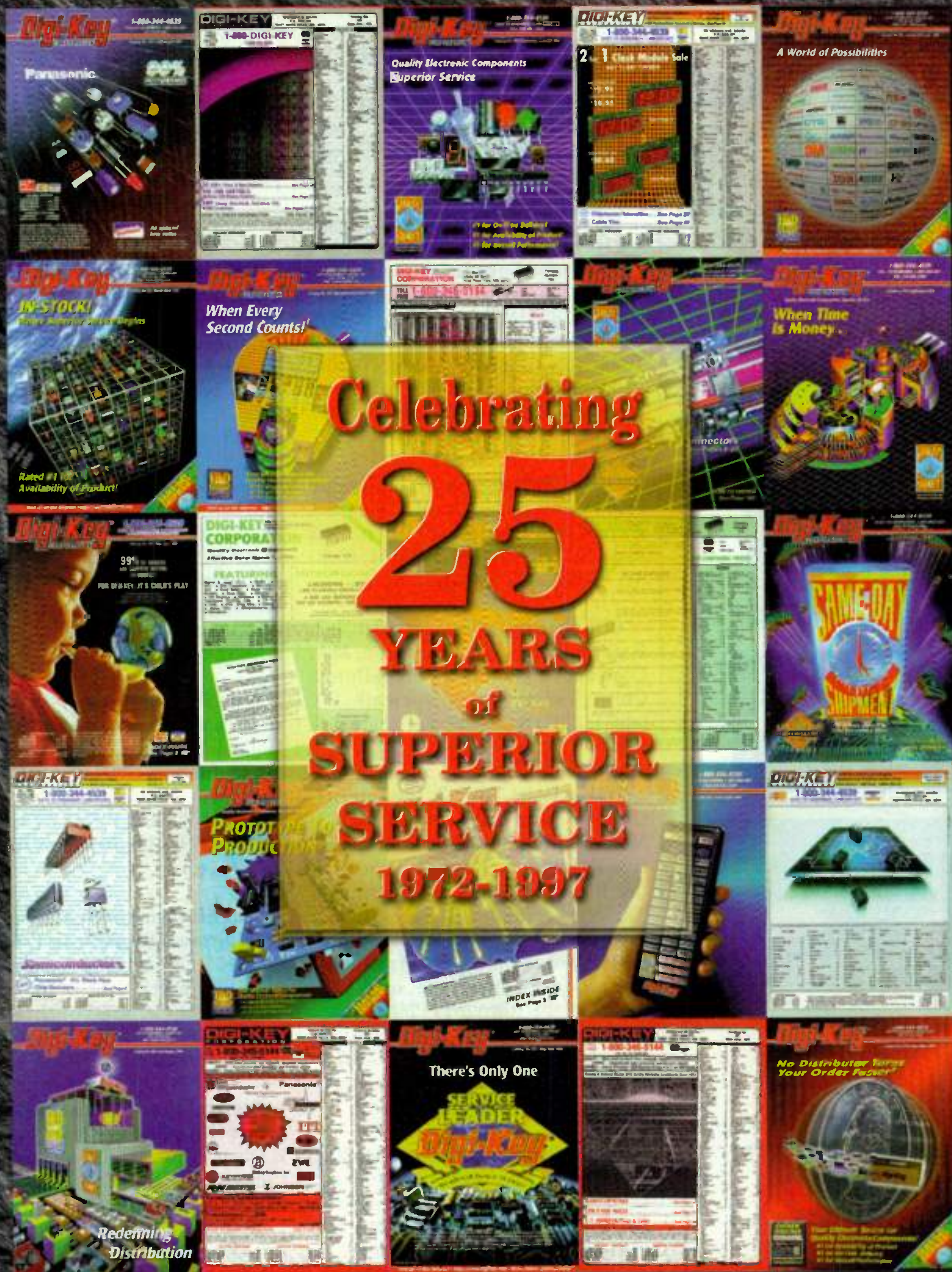
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PCI Plus Europe Developers' Conference and Expo, Sept. 29-Oct. 2. International Conference Center/Messe Berlin, Berlin, Germany. Contact Annabooks, 11838 Bernardo Plaza Ct., San Diego, California 92128; (800) 462-1042; fax (619) 673-1432; 73204,3405@compuserve.com; Internet: http://www.annabooks.com

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PCI Plus Europe, Oct. 1-2. The International Conference Center (ICC), Messe Berlin, Germany. Contact Active Exhibitions Europe at Post Office Box 2114, 5300 CC Zaltbommel, The Netherlands. (31) 418 512999; fax (31) 418 515115; e-mail: active@otsgroup.nl; Internet: http://www.aexpo.com, or Annabooks, 11838 Bernardo Plaza Court, San Diego, CA 92128; (800) 462-1042; fax (619) 673-1432; e-mail: 73204.3405@compuserve.com; Internet: http://www.annabooks.com.

Fourth International CAN Conference (iCC), Oct 1-2. Berlin, Germany. Contact CAN in Automation, Am Weichselgarten 26, D-91058 Erlangen, +49 9131-601091; fax +49 9131-601092.

IPCWorks '97, Oct. 5-9. Hyatt Regency Crystal City, Washington, D.C. Contact David Bergman, vice president, technical programs, (847) 509-9700 ext 340; fax (847) 509-9798.

Seventh Connecticut Vendor Show, Oct. 7. Aqua Turf Contry Club, Plantsville, Connecticut. Contact Gary DiBlanda, (203) 929-8431 ext. 330.

NEPCON Texas '97, Oct. 7-9. Infomart, Dallas, TX. Contact Reed Exhibition Companies, Customer Service, (800) 467-5656; fax (203) 840-9656; e-mail: inquiry@nepcontexas.reedexpo.com; Internet: http://nepcon.reedexpo.com.

IEEE Ultrasonics Symposium, Oct. 7-10. Marriott Hotel, Toronto, Canada. Contact Stuart Foster, Dept. of Medical Biophysics, Room S-658, Sunnybrook Health Science Ctr., 2075 Bayview Avenue, Toronto, Ontario, M4N 3M5, Canada; e-mail: stuart@owl.sunnybrook.utoronto.ca.

Seventh International Conference on Artificial Neural Networks, (ICANN '97), Oct. 8-10. Lausanne, Swizerland. Contact ICANN '97, Ecole Polytechnique Federale De Lausanne, LAMI, CH-1015 Lausanne, Switzerland; fax +41 21 693 5656; e-mail: icann97@epfl.ch; Internet: http://www.epfl.ch/icann97.

Sixth IEEE International Conference on Universal Personal Communications, Oct. 12-16. Hotel del Coronado, San Diego, California. Contact Gail Weisman, IEEE Communications Society, 345 E. 47th St., New York, NY 10017; (212) 705-7018; fax (212) 705-7865; e-mail: g.weisman@ieee.org.

Sixth IEEE International Conference on Universal Personal Communications (ICUPC '97), Oct. 13-15. Contact Tony Acampora, MC 0409, Bldg EBU1, UCSD, 9500 Gilman Dr., La Jolla, CA 92093-0409; (619) 534-5438; fax (619) 534-2486; e-mail: acampora@ece.ucsd.edu.

Conference on Domain-Specific Languages (DSL), October 15-17. Red Lion Resort, Santa Barbara, California. Contact USENIX Conference Office, 22672 Lambert Street, Suite 613, Lake Forest, California 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

ICSPAT/DSP World 1997, October 15-17. San Diego Convention Center, San Diego, California. Contact Denise Chan, Miller Freeman Inc., (415) 278-5231; e-mail: dsp@exporeg.com.


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IEEE Holm Conference on Electrical Contacts, Oct. 18-22. Wyndham Franklyn Plaza, Philadelphia, PA. Contact Wendy Rochelle, IEEE Conference Services, 445 Hoes Ln., P.O. Box 1331, Piscataway, NJ 08855-1331; (908) 562-3870; fax (908) 981-1769; e-mail: w.rochelle@ieee.org.

VHDL International User's Forum (VIUF) Conference, Oct. 19-22. Hyatt Regency Crystal City Hotel, Arlington, VA. Contact VIUF, (415) 329-0510.

IEEE Telecommunications Energy Conference (INTELEC '97), Oct. 19-23. World Congress Centre, Melbourne, Australia. Contact Robert N.K. Thuan, Network Products-Telstra Corp. Level 14, 242 Exhibition St., Melbourne, Victoria 3000, Australia; +61 3 634 6216; fax +61 3 632 3607

Sensors Expo, Oct. 21-23. Cobo Convention Center; Detroit, MI. Contact Expocon Management Associates Inc., (203) 256-4700; e-mail: sensors@expocon.com; Internet: http://www.expocon.com.

Fourth IEEE International Conference on Image Processing (ICIP '97), Oct. 26-30. Fess Parker's Red Lion Resort, Santa Barbara, CA. Contact Sanjit K. Mitrea, Electrical & Computer Engineering, University of California, Santa Barbara, CA 93106-9560; (805) 893-3957; fax (805) 893-893-3262; e-mail: mitra@ece.ucsb.edu.

11th Systems Administration Conference (LISA '97), Oct. 26-31. Town & Country Hotel, San Diego, CA. Contact USENIX Conference Office, 22672 Lambert Street, Suite 613, Lake Forest, CA 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

SYSTEMS 97, Oct. 27-31. Munich Trade Fair Center, Munich Germany. Contact Messe Munchen GmbH, Messegelande, D-80325 Munchen, +49 (89) 51070; fax +49 (89) 51 07506; Internet: http://www.sysems.de; e-mail: info@messe-muenchen.de.

19th Annual International Conference of the IEEE Engineering in Medicine & Biology Society, Oct. 29-Nov. 2. Sally Chapman, Secretariat, National Res. Council of Canada, Bldg. M-55 Rm. 393, Ottawa, KIA OR8, Canada; (613) 993-4005; fax (613) 954-2216.

19th International Conference of the IEEE Engineering in Medicine & Biology Society, October 30-November 2. Chicago Marriott Downtown, Chicago, Illinois. Contact Meeting Management, 2603 Main Street, Suite 690, Irvine, California 92714; (714) 752-8205; fax (714) 752-7444; e-mail: embs97@ieee.org; Internet: http://www.eecs.uic.edu/~embs97.

NOVEMBER

IEEE International Test Conference (ITC), Nov. 1-5. Sheraton Washington Hotel, Washington, DC. Contact ITC, 655 15th St., N.W., Suite 300, Washington, DC 20005; (202) 639-4164; fax (202) 347-6109.

Voice, Video, & Data Communications Conference & Exhibition, Nov. 2-6. Dallas, TX. Contact SPIE Exhibits Dept., P.O. Box 10, Bellingham, WA 98227-0010; (360) 676-3290; fax (360)-647-1445; e-mail: exhibits@spie.org.

IEEE Global Telecommunications Conference (GLOBECOM '97), Nov. 3-7. Phoenix, AZ. Contact Nigel Reynolds, 15436 N. First Ave., Phoenix, AZ 85023; (602) 942-5583; fax (602) 942-4542; e-mail: nigelaz@aol.com.

WESCON '97, Nov. 4-6. San Jose Convention Center and Santa Clara Convention Center, San Jose and Santa Clara, CA. Contact Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045-3194; (800) 877-2668; fax (310) 641-5117; e-mail: wescon@ieee.org.

IEEE Intelligent Transportation Systems Conference (ITS '97), Nov. 9-12. Boston Park Plaza Hotel, Boston, MA. Contact Richard Sparks, 8 Richard Rd., Bedford, Massachusetts 01730; (617) 862-3000; fax (617) 863-0586; e-mail: r.sparks@ieee.org.

Productronica '97, Nov. 11-14. Messegelande, Munchen, Germany. Contact Messe Munchen GmbH, Messegelande, D-80325 Munchen, Germany; +49 (89) 51 07-0; fax +49 (89) 51 07-506; e-mail: info@messe-munchen.de; Internet: http://www.Productronica.de.

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Executive Editor: **ROGER ALLAN** (201) 393-6057 rallan@class.org
Managing Editor: **BOB MILNE** (201) 393-6058 bmilne@class.org

Technology Editors:

Analog & Power: **FRANK GOODENOUGH** (617) 227-4388 75410.2361@compuserve.com
Communications: **LEE GOLDBERG** (201) 393-6232 leeg@class.org
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New Products: **ROGER ENGELKE JR.** (201) 393-6276 rogere@csnet.net
Contributing Products Editor: **MILT LEONARD**

Editorial Headquarters:

(201) 393-6060 Fax: (201) 393-0204 E-mail: edesign@class.org
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Chief Copy Editor: **MICHAEL SCIANNAMEA** (201) 393-6024 mikemea@class.org
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SEPTEMBER 1997

Embedded Systems Conference, Sept. 29-Oct. 2. San Jose Convention Center, San Jose, California. Contact Liz Austin, Miller Freeman Inc., (888) 239-5563; (415) 538-3848; e-mail: esc@mfi.com.

PCI Plus Europe Developers' Conference and Expo, Sept. 29-Oct. 2. International Conference Center/Messe Berlin, Berlin, Germany. Contact Annabooks, 11838 Bernardo Plaza Ct., San Diego, California 92128; (800) 462-1042; fax (619) 673-1432; 73204, 3405@compuserve.com; Internet: http://www.annabooks.com

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OEMed Northeast, Oct. 1-2. Bayside Expo Center, Boston, MA. Contact Exposition Excellence Corp., 112 Main St., Norwalk, CT 06851; (203) 847-9599; fax (203) 854-9438.

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PCI Plus Europe, Oct. 1-2. The International Conference Center (ICC), Messe Berlin, Germany. Contact Active Exhibitions Europe at Post Office Box 2114, 5300 CC Zaltbommel, The Netherlands. (31) 418 512999; fax (31) 418 515115; e-mail: active@otsgroup.nl; Internet: http://www.aexpo.com, or Annabooks, 11838 Bernardo Plaza Court, San Diego, CA 92128; (800) 462-1042; fax (619) 673-1432; e-mail: 73204.3405@compuserve.com; Internet: http://www.annabooks.com.

Fourth International CAN Conference (iCC), Oct 1-2. Berlin, Germany. Contact CAN in Automation, Am Weichselgarten 26, D-91058 Erlangen, +49 9131-601091; fax +49 9131-601092.

IPCWorks '97, Oct. 5-9. Hyatt Regency Crystal City, Washington, D.C. Contact David Bergman, vice president, technical programs, (847) 509-9700 ext 340; fax (847) 509-9798.

Seventh Connecticut Vendor Show, Oct. 7. Aqua Turf Contry Club, Plantsville, Connecticut. Contact Gary DiBlanda, (203) 929-8431 ext. 330.

NEPCON Texas '97, Oct. 7-9. Infomart, Dallas, TX. Contact Reed Exhibition Companies, Customer Service, (800) 467-5656; fax (203) 840-9656; e-mail: inquiry@nepcontexas.reedexpo.com; Internet: http://nepcon.reedexpo.com.

IEEE Ultrasonics Symposium, Oct. 7-10. Marriott Hotel, Toronto, Canada. Contact Stuart Foster, Dept. of Medical Biophysics, Room S-658, Sunnybrook Health Science Ctr., 2075 Bayview Avenue, Toronto, Ontario, M4N 3M5, Canada; e-mail: stuart@owl.sunnybrook.utoronto.ca.

Seventh International Conference on Artificial Neural Networks, (ICANN '97), Oct. 8-10. Lausanne, Swizerland. Contact ICANN '97, Ecole Polytechnique Federale De Lausanne, LAMI, CH-1015 Lausanne, Switzerland; fax +41 21 693 5656; e-mail: icann97@epfl.ch; Internet: http://www.epfl.ch/icann97.

Sixth IEEE International Conference on Universal Personal Communications, Oct. 12-16. Hotel del Coronado, San Diego, California. Contact Gail Weisman, IEEE Communications Society, 345 E. 47th St., New York, NY 10017; (212) 705-7018; fax (212) 705-7865; e-mail: g.weisman@ieee.org.

Sixth IEEE International Conference on Universal Personal Communications (ICUPC '97), Oct. 13-15. Contact Tony Acampora, MC 0409, Bldg EBU1, UCSD, 9500 Gilman Dr., La Jolla, CA 92093-0409; (619) 534-5438; fax (619) 534-2486; e-mail: acampora@ece.ucsd.edu.

Conference on Domain-Specific Languages (DSL), October 15-17. Red Lion Resort, Santa Barbara, California. Contact USENIX Conference Office, 22672 Lambert Street, Suite 613, Lake Forest, California 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

ICSPAT/DSP World 1997, October 15-17. San Diego Convention Center, San Diego, California. Contact Denise Chan, Miller Freeman Inc., (415) 278-5231; e-mail: dsp@exporeg.com.

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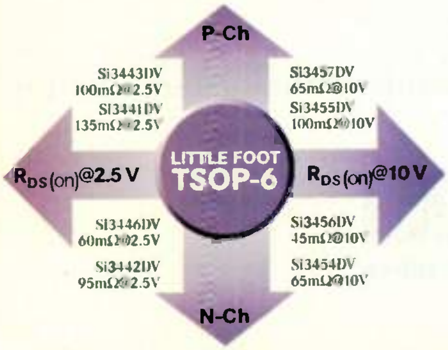

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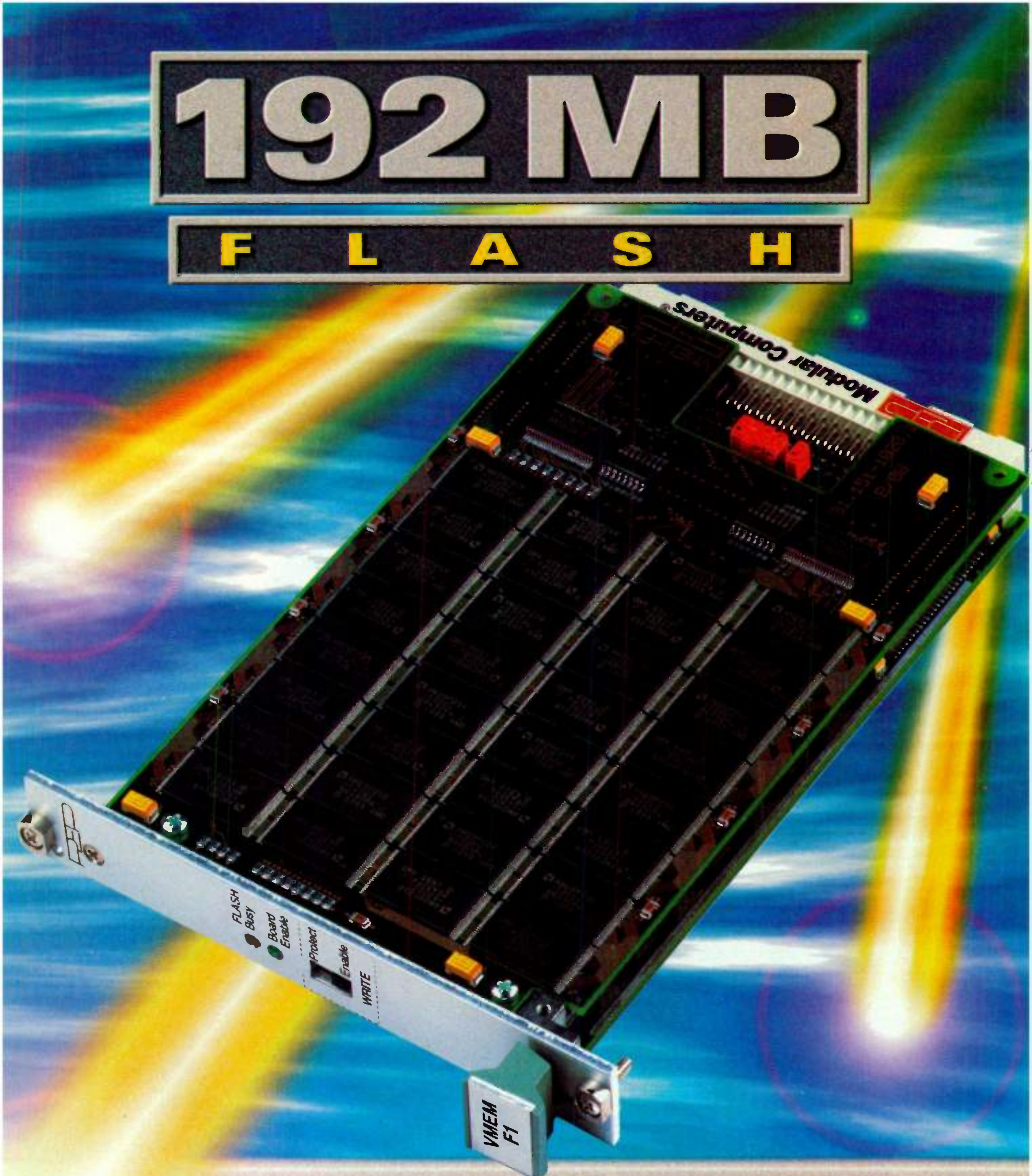
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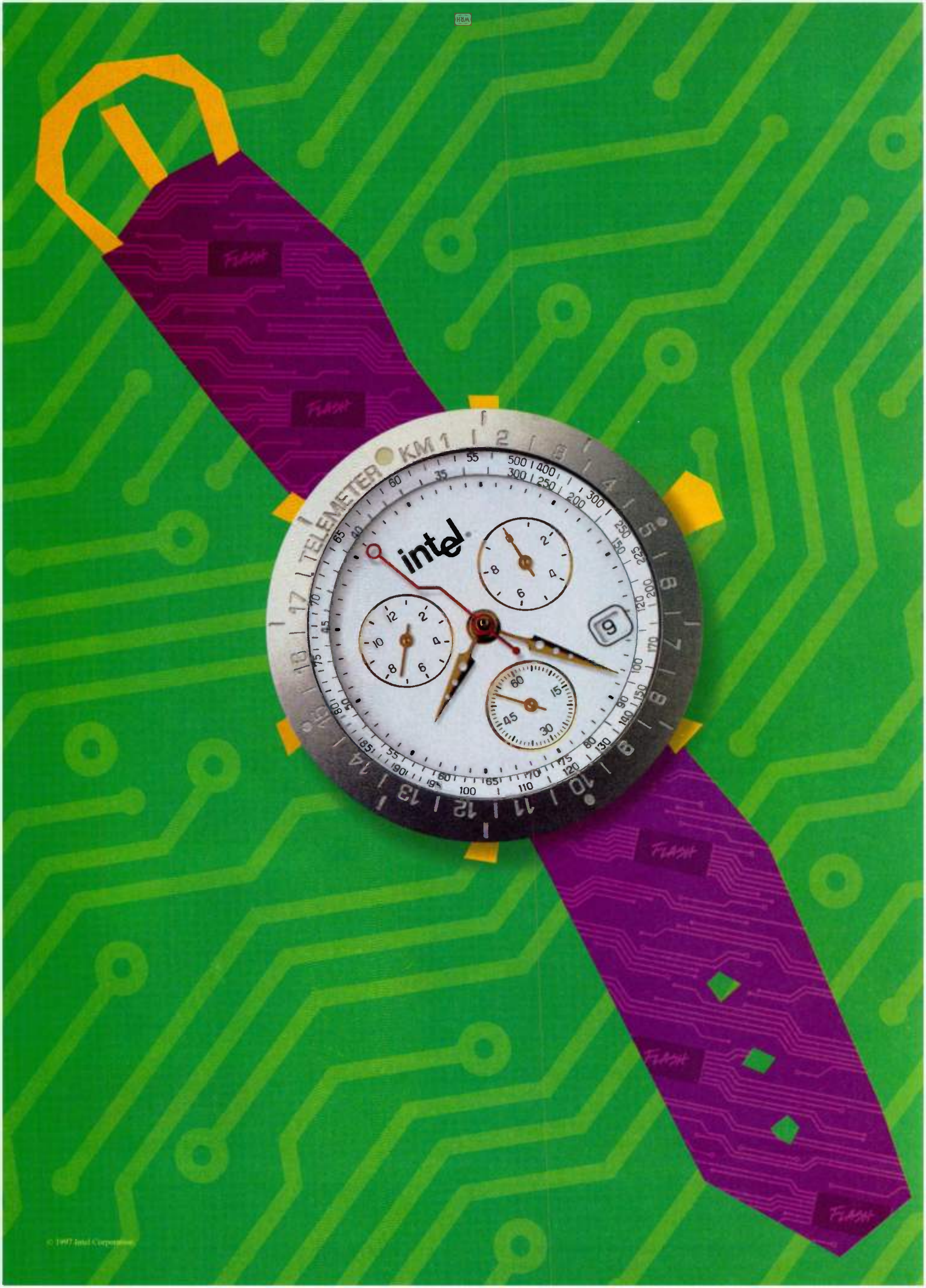
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Ditching The Cardboard Box

In the early 1940's, a team of Japanese scientists took more than a year to do the calculations necessary to model the flow of air around a cylinder. I guess they hadn't heard of U.S. Govt. Contract W-670-ORD-4926. If they had, they might have waited a few more years before attempting this pioneering work in the mathematics-intensive field of Computational Fluid Dynamics, or CFD for short. Mostly used to examine theoretical aerodynamics of wings and turbines, CFD also applied to airflow in industrial situations for process flows and flows through buildings. Although now at the leading edge of efforts to alleviate thermal flow problems in computers and other electronic systems, CFD's progress was hindered by a lack of tools capable of performing the hundreds of thousands of detailed calculations required to obtain any sort of reliable model.

That was where Contract W-670-ORD-4926 came in. Signed on June 5, 1943, the contract gave the go-ahead for the University of Pennsylvania to develop the Electronic Numerical Integrator and Computer (ENIAC). ENIAC was up and running by Feb. 15, 1946, and is considered to be the first electronic digital computer. Using 18,000 vacuum tubes and occupying a room measuring 30 by 50 ft., the 30-ton, 150-kW machine could perform additions in 0.2 ms and multiplications in about 2.8 ms—about 1000 times faster than the electromechanical machines of the day.


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ENIAC was designed to solve ballistic problems for the war effort. In the abstract, this may sound more exciting than modeling the airflow around a cylinder, but in practice, the calculations were just as tedious and labor-intensive. Retired in October 1955, ENIAC's descendants played a key role in work done on CFD at Imperial College, London, during the 1960's and 70's. Until the 1980's, however, the programs used for CFD were generic and had to be tailored to the application. The programs were large, hard to use, expensive, and swamped the computer systems available at the time.

With the proliferation of electronic systems in the late 80's, particularly high-powered desktop and portable computers, Flomerics Inc., Marlborough, Mass., and more recently Fluent Inc., Lebanon, N.H., were formed to apply CFD technology to the heat dissipation and thermal management problems specific to electronics applications. Flomeric's primary goal was to move CFD from a highly specialized skill to one a general design engineer could quickly learn. For this to happen, the CFD program had to be made smaller so it could run on available systems, and had to be more intuitive. To achieve this, a number of simplifications were made, particularly in reference to combustion, boiling, and supersonic flows.

The resulting program, called Flotherm, has caught on with EDA vendors such as Cadence and Mentor Graphics. Ideally, the Electronic Engineer (EE) would generate the board layout file, pass it through Autotherm (Mentor) or Thermax (Cadence), and pass the result down to the Mechanical Engineer (ME). The ME would then import the the file into Flotherm and add it to other system components. The optimized board layout is then passed back to the EE. In practice, this is often a one-way route with the EE handing off the board file to the ME to deal with. In any case, the end result is the elimination of the overused mock-up board with load resistors in a cardboard box held together with tape.

The scheme relies on manufacturers to supply compact models (a network of thermal resistances) of their devices. These models have a minimal amount of grid elements relative to a detailed model of the semiconductor package and so make significant savings in the computational time needed. They also preserve intellectual property rights. Intel has already provided a compact model of its Pentium processor. For more on CFD and Flotherm, contact Steve Addison of Flomerics at (408) 954-7332, or see his presentation on CFD at the *Wireless & Portable Design Conference* at the Boston Marriot Burlington Hotel, Sept. 15-18, in Burlington, Mass. *pmannion@penton.com.*

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READER SERVICE 113

Microlithography Yields Polymers That Emit Patterns Of Light

Polymer LEDs are coming! Polymer LEDs are coming! Well, at least that's a distinct possibility thanks to a development by researchers at the University of Rochester, N.Y., and Hewlett-Packard's Solid State Technology Lab, Palo Alto, Calif. They created the first light-emitting diode made of polymers that can be treated with everyday chemical techniques to emit patterns of light. This achievement should help to evolve plastic LEDs from indicator lights on electronic devices into increasingly sharp and sophisticated displays—even LED-based computer monitors or TV screens.

The research team created the LED by putting to work on polymers the same microlithographic technique used in silicon circuitry. Basically, silicon techniques were employed to make the plastics that might someday supplant silicon as the material heart of electronics.

Guillermo Bazan, lead researcher and an associate professor of chemistry at Rochester, along with graduate student Michelle Renak and HP researcher Daniel Roitman, made the patterned LED by implanting a poly (paracyclophene) film with a compound called triphenylsulfonium trifluoromethanesulfonate, a photoacid generator that produces triflic acid when exposed to light. When the film reacts with the acid, it's converted to poly (p-phenylenevinylene), which has the light-emitting properties characteristic of an LED and is one of the best-conducting plastics known.

Scientists produced patterns of light by placing a "mask," which is essentially a cover with a pattern of holes cut into it, over the light-sensitive polymer mix before it's exposed to light. When the light shines through the mask, the triflic acid produced remains localized in the spots that were illuminated, and distinct patterns of light-emitting regions are created. The process is so precise that Bazan's LED emits individual pinpoints of light only five thousandths of a millimeter in width.

The team is now working on an LED that can emit pinpoints of different colors of light. The microlithographic technique might also be used someday to make polymer microchips by patterning conducting grids on polymers, much like the way silicon chips are made. Call (716) 275-1626, or e-mail: *bazan@chem.chem.rochester.edu*. *RE*

Analog/Mixed-Signal VHDL Extensions Nearing Completion

With many digital designers now being forced to design with analog and mixed signal, the push is on to develop the analog/mixed-signal (A/MS) versions of the well-known Verilog and VHDL high-level design languages (HDLs). The VHDL analog/mixed signal extensions have been the responsibility of the IEEE Working Group 1076.1, headed by Alan Vachoux of Lausanne University in Switzerland.

As of July 21, ballots for the extensions were officially mailed, along with a language reference manual (LRM) draft, to 175 experts worldwide for review and voting. Also mailed with the ballots was a packet of related materials that included a tutorial, a language design report, white papers, validation reports from Japanese members, and a set of model examples from the University of Southampton. Formal approval of the specification is expected no later than the first quarter of 1998.

The next Working Group meeting is scheduled to take place sometime between October 19-23 in Washington D.C. at the VIUF (VHDL International Users Forum) Fall 1997 conference. At this time, the IEEE balloting process of the analog/mixed signal extensions will be discussed, as well as an update on work being done by the IEEE Validation Committee Work Group. To obtain further information on this VHDL extension, except for the incremental Draft LRM and the integrated draft LRM, check out the *http://www.vhdl.org/analog* web site. For further information on ballots, etc., visit the group's Internet address: *http://www.vhdl.org/analog/wwwpages/ballot.html*. *CA*

Six New Specifications Expand Capabilities Of ATM

During its July meeting in Montreal, Canada, the ATM Forum ratified six new specifications. These new specifications greatly enhance ATM's ability to interoperate with existing LAN and WAN technologies, and enable rapid development of applications.

The first of the specifications approved is the Multiprotocol over ATM (MPOA) 1.0, which provides a network layer routing framework that maps routed and bridged traffic to ATM-switched virtual channels. The second is the LAN Emulation Over ATM (LANE) 2.0, which uses the LANE User-to-Network Interface (LUNI) to make possible LANE services to be distributed across multiple serves for scalability and reliability of emulated LANs.

The third ratified spec is the Inverse Multiplexing for ATM (IMA) 1.0, which allows multiple T1 or E1 lines to be multiplexed into a single ATM interface. Next is the Voice and Telephony Over ATM (VOTA) 1.0, which offers support for 64 kbits/s, G.711 PCM-encoded switched voice services to ATM terminals. Then there's the Frame-based User-to-Network Interface (FUNI) 2.0, which enables enhanced support for switched ATM services across a low-speed frame-based interface. Finally, the Dynamic Bandwidth Utilization in 64-kbit/s Time Slot Trunking Over ATM Using Circuit Emulation Services (DBCES) 1.0 provides support for legacy services, enabling telephone communications across ATM networks. Copies of the complete specifications are available from the ATM Forum's Web site at *http://www.atmforum.com*. *LG*

IPC Land-Pattern Calculator Available On The Internet

The Institute for Interconnecting and Packaging Electronic Circuits (IPC) has made the IPC-SM-782 Surface Mount Land Pattern Calculator available for computation on the Internet. The IPC-SM-782 has served as the standard for creating independent SMT land patterns since it was released as a written standard in 1987.

Initially, to keep up with the introduction of new technologies, the IPC came up with an electronic spreadsheet for the standard. Thus, designers were able to save considerable time by performing the complex land pattern calculations from component input information. Its one downfall, though, was its inability to access databases created by users outside of the local computer system.

To placate that problem, the IPC Designers Council took the spreadsheet calculator, developed by the IPC Surface Mount Land Pattern Subcommittee, and placed it on the Designers Council web site. Designers can search an approved land pattern database (meaning that the component has been adopted by the EIA or EIAJ), or search the user database by either a manufacturer name or part number. Not only are land patterns shown, but the assumptions behind the calculations are given as well.

To create a new land pattern on the SM-782 calculator, the designer has to follow several steps. First component data must be input, as well as the fabrication and assembly tolerances. The designer's goals for solder joint fillets also will have to be submitted. Upon completion of these inputs, the calculator will return calculated values as a three-place decimal for the land geometry. Finally, the designer is asked to evaluate and adjust these calculations to produce even grid increments. If the results are unsatisfactory, the designer can easily modify them.

After a final review, the designer can submit the new land patterns to the Designers Council. A one-time registration process is required so that the council can contact a designer should questions arise.

To log into the calculator web site directly, go to: *http://search.ipc.org/SM782/default.asp*. It can also be reached through the IPC home page at *http://www.ipc.org*. Or for more information, call Lisa Williams, IPC project manager, at (847) 509-9700, ext. 379; e-mail: *willi@ipc.org*. *RE*

Group Gets Funding To Develop MTA Computer

The University of California at San Diego (UCSD) has received an award of $1.9 million from the Defense Advanced Research Projects Agency (DARPA) to develop the Tera MTA (for multithreaded architecture) supercomputer. UCSD and the San Diego Supercomputer Center (SDSC) will lead a research team that includes representatives from Boeing; the California Institute of Technology; Jet Propulsion Laboratory (JPL); Sanders (a Lockheed Martin company); the Naval Command, Control, and Ocean Surveillance Center; and Tera Computer. Tera designs and builds high-performance MTA platforms for simulation and database applications.

The Tera MTA, which lends itself to a multiprocessor design, employs processors that support up to 128 threads of execution. It also makes use of a shared-memory configuration to boost performance. Until now, MTAs were observed primarily through simulations and models. Now an actual evaluation can be done. A single-processor prototype was recently developed that ran 1.31 times faster than a Silicon Graphics Cray T90 using the NASA NAS Parallel Integer Sort benchmark. For more information, contact the SDSC at (619) 534-5032 or on the Internet at *http://www.sdsc.edu*. Or, call Tera Computer at (206) 325-0800; Internet: *http://www.tera.com*. *RN*

Licensing Program Launched For MPEG-2 Technology Patents

Digital video should take a step toward worldwide implementation with the inception of MPEG LA's MPEG-2 patent portfolio license. The portfolio is expected to contain 33 U.S. patents essential for using MPEG-2. Holders of the patents are Columbia University, Fujitsu, General Instrument, Lucent Technologies, Matsushita Electric Industrial, Mitsubishi Electric, Philip Electronics, Scientific-Atlanta, and Sony. Licensors will license their essential MPEG-2 patents to MPEG LA (MPEG Licensing Administrator, located in Delaware) for sublicensing to manufacturers and content providers.

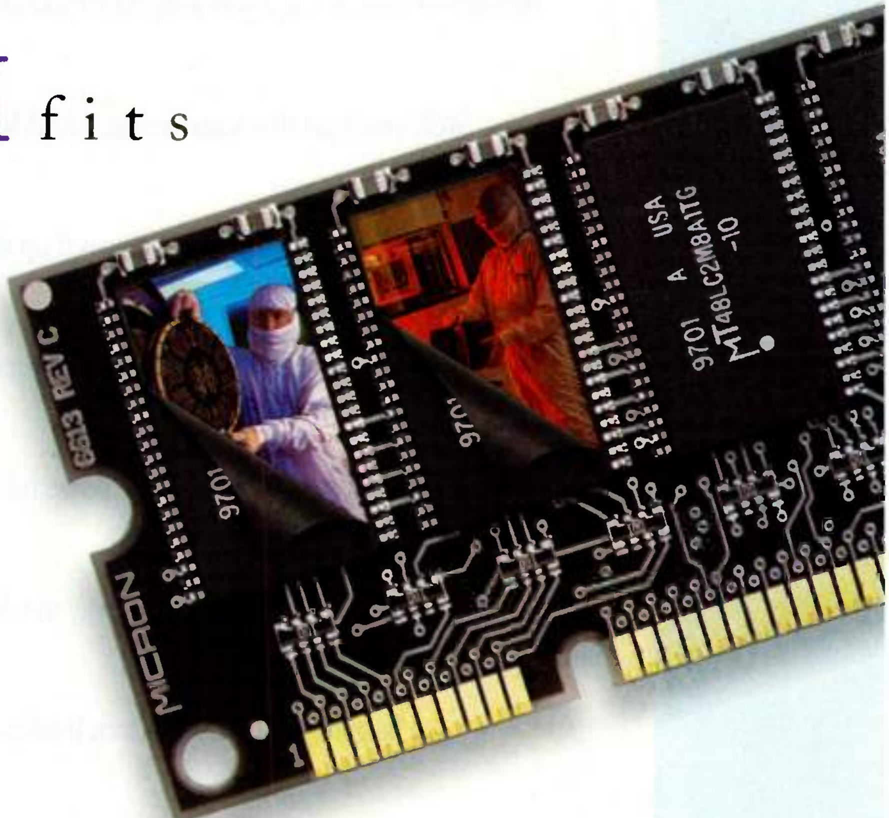
Portfolio royalty rates will range from $4 for a TV set-top box or computer incorporating an MPEG-2 encoder or decoder, to $6 for a camcorder using both an MPEG-2 encoder and decoder. Packaged products such as digital versatile disks (DVDs) will incur a royalty of $0.04 if sold for consumer use and $0.40 if sold for commercial rental.

MPEG-2 (Moving Picture Expert Group) is the fundamental technology underlying the efficient transmission, storage, and display of digitized moving images and sound tracks crucial to high-definition television (HDTV), direct broadcast by satellite (DBS), digital cable TV systems, and all other forms of digital video delivery. MPEG-2 compresses digital information by reducing spatial and temporal redundancies in binary data streams, thereby conserving transmission resources and storage space.

For more information, call (303) 331-1880; fax (303) 331-1879; e-mail: *bfuta@mpegla.com*. *RE*

Edited by Roger Engelke

Everything **we know** about **SDRAM** fits on a **DIMM.**



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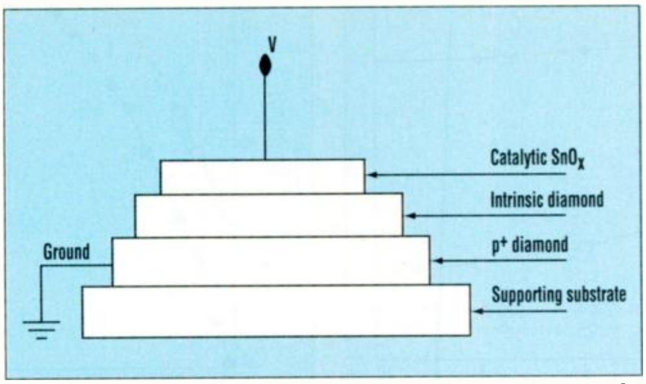
READER SERVICE 172

Diamond-Based Microelectronic CO And O_2 Gas Sensor Shows Promise For High-Temperature, High-Sensitivity Operation

As the saying goes, "diamonds are forever," and if the researchers at Physitron Corp., Huntsville, Ala. have any say in it, diamond-based microelectronic gas sensors may go on operating forever, under nearly any temperature condition. Diamond is a wide-bandgap material that's capable of operating at temperatures in the range of hundreds of degrees Celsius.



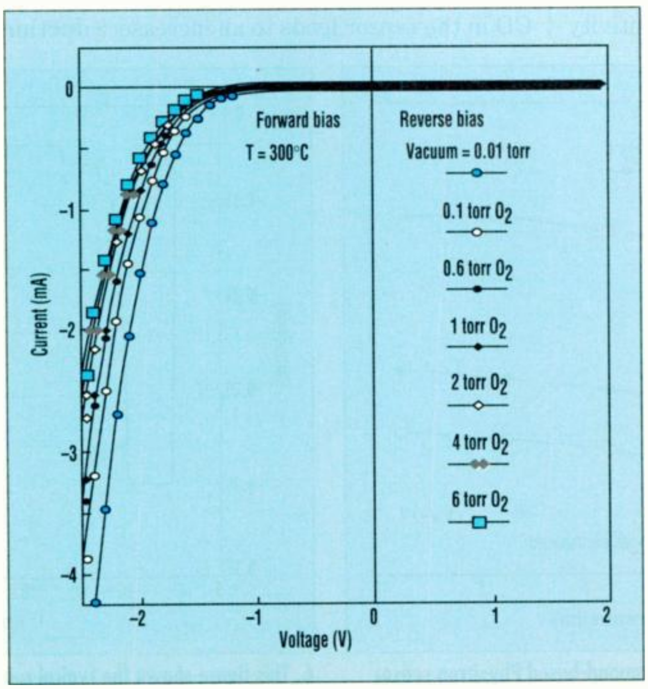
1. This figure depicts the structure of a diamond-based oxygen and carbon-monoxide sensor made by plasma-enhanced chemical-vapor deposition. It is being developed by Physitron Corp.

Physitron is developing these sensors for the detection of carbon-monoxide (CO) and oxygen (O_2) gases at elevated temperatures well beyond the reach of conventional silicon-based sensors. So far, in testing, the sensors have produced favorable results at temperatures as high as 300°C, detecting less than 1 ppm of hydrogen and a few ppms of O_2 and CO. But the potential exists for much-higher-temperature operation.

Such sensors have applications in industrial process control, nuclear power plant monitoring, mine safety, home-environment monitoring, and automotive exhaust emissions and engine monitoring. Similar efforts to produce high-temperature gas sensors also are being investigated with other wide-bandgap materials such as silicon-carbide (SiC).

The basic development for the sensors was started at the Department of Electrical and Computer Engineering, Vanderbilt University, Nashville, Tenn. Physitron is working with Vanderbilt University to further develop the sensor and commercialize the device under Small Business Innovative Research (SBIR) funding provided by the Kennedy Space Center (KSC), NASA. The NASA KSC funded effort includes both a hydrogen sensor and an oxygen sensor. These devices are similar in design, construction, and operation. The discussion that follows focuses on the CO and O_2 sensors.

In the Physitron effort, diamond was used in conjunction with tin-oxide (SnO_x) to form what the company calls a CAIS (Catalyst Adsorptive Insulator Semiconductor) structure. Due to its sensitivity to gases at elevated temperatures, SnO_x was the ideal choice. To make the sensor, a silicon-compatible process was employed. Gas detection was accomplished by measuring the change in oxygen gas vacancies in the SnO_x layer when it was exposed to CO and O_2 gases.



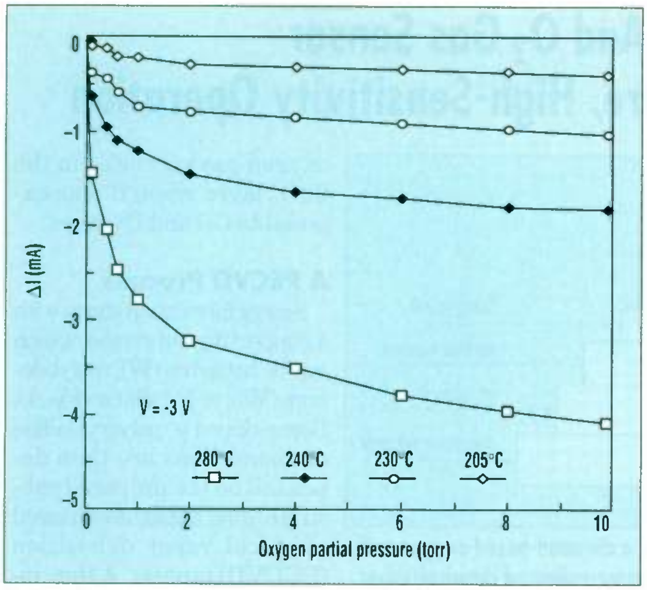
2. Shown here are the IV characteristics and oxygen adsorption for the diamond-based Physitron sensor for forward and reverse-bias regions.

A PECVD Process

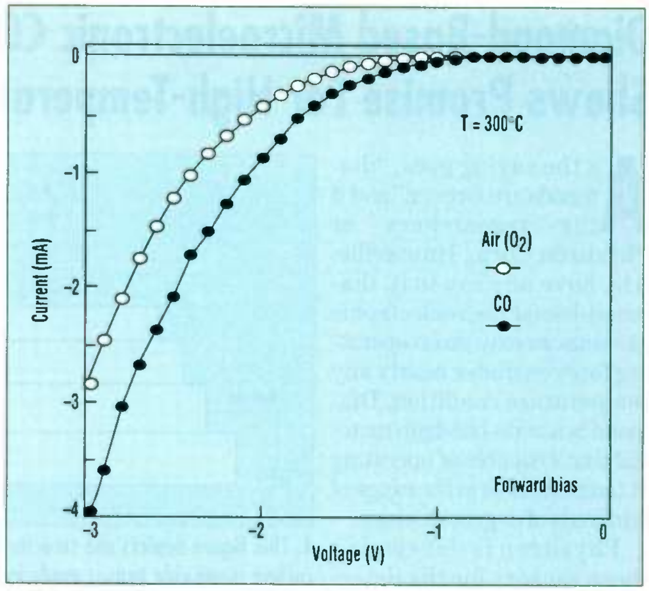
Sensor fabrication starts with a supporting substrate, which can be tungsten (W), molybdenum (Mo), or p^{++} silicon *(Fig. 1)*. Boron-doped p^+ polycrystalline diamond films are then deposited on the prepared substrate using a plasma-enhanced chemical vapor deposition (PECVD) process. A thin, intrinsic (undoped) diamond layer is next deposited on the p^+ diamond layer. Films are deposited by using a mixture of 99% hydrogen gas and 1% methane gas in a microwave source operating at a frequency of 2.45 GHz with 1.5 kW of power. and running at a temperature of 850°C.

The films are annealed for one minute in an argon (Ar) atmosphere at a temperature of 800°C. Then a SnO_x electrode is formed by depositing 800 Å of Sn on intrinsic diamond. A thermal-oxidation process follows at 400°C for one hour. Finally, a catalyst platinum (Pt) layer that's under 500-Å thick is evaporated on the SnO_x film to complete the CAIS structure.

Current-voltage (I-V) characterizations of the gas sensor are performed with positive bias voltage applied to the gate with the substrate grounded *(Fig 1, again)*. I-V characterizations were performed at 300°C in a vacuum of 0.01 torr. The change in oxygen gas concentration was detected by the large change in the forward device current *(Fig. 2)*. Even for higher vacuum levels of 6 torr, the I-V curve remains fairly constant. As the oxygen gas concentration increases, the device's forward current decreases by several milliamperes at a vacuum level of 6 torr *(Fig. 3)*. The sensor's gas sensitivity



3. As oxygen gas concentration increases in the Physitron diamond-based sensor, there is a large change in the sensor's current—a decrease of several milliamperes at a pressure of 6 torr.

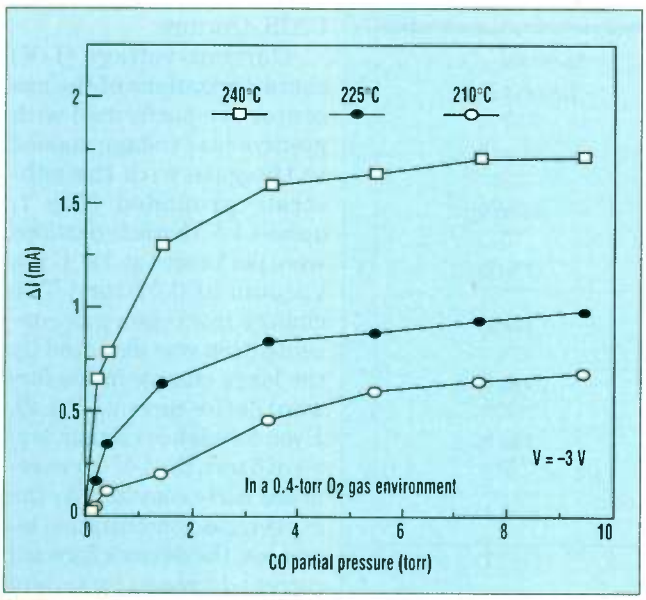


4. This figure demonstrates the IV characteristics for the Physitron diamond-based sensor for oxygen and carbon-monoxide gases. Data was obtained at a temperature of 300°C.

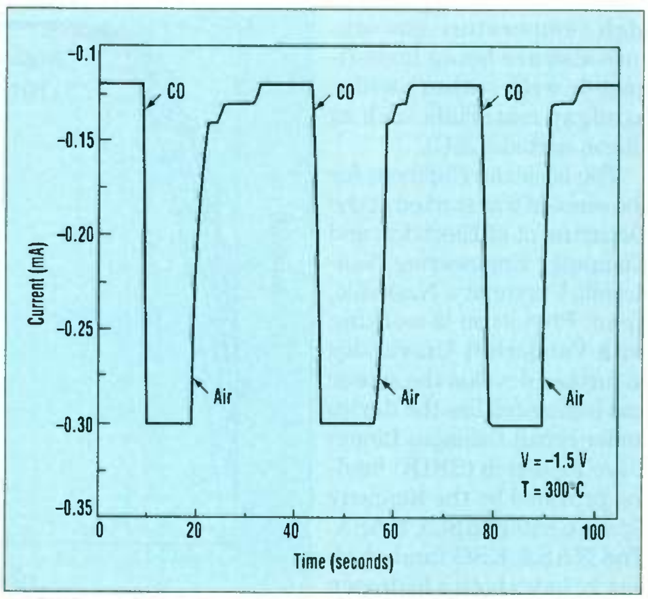
can be measured in terms of the change in device current at a fixed voltage and a constant temperature versus gas partial pressure at different temperatures. The negative direction of the curves indicates the decrease in device current as oxygen is adsorbed *(Fig. 3, again)*. The curves show a rapid increase in ΔI at low oxygen gas concentrations, followed by a saturation trend at high oxygen gas concentrations. Also observed is an increase in the device's sensitivity to detecting oxygen gas with increasing temperature. For a fixed vacuum level of 10 torr, ΔI was recorded as -0.4, -1.8, and -4.08 mA, for temperatures of 205°C, 240°C, and 280°C, respectively.

The sensor also was tested for its I-V characteristics while detecting CO gas flowing at a rate of 10 ml/minute in an O_2 ambient at a temperature of 300°C *(Fig. 4)*. The reduction reaction between pre-adsorbed oxygen and CO in the sensor leads to an increase in device current. The device's I-V characteristics go back to its value in air when the CO gas is turned off.

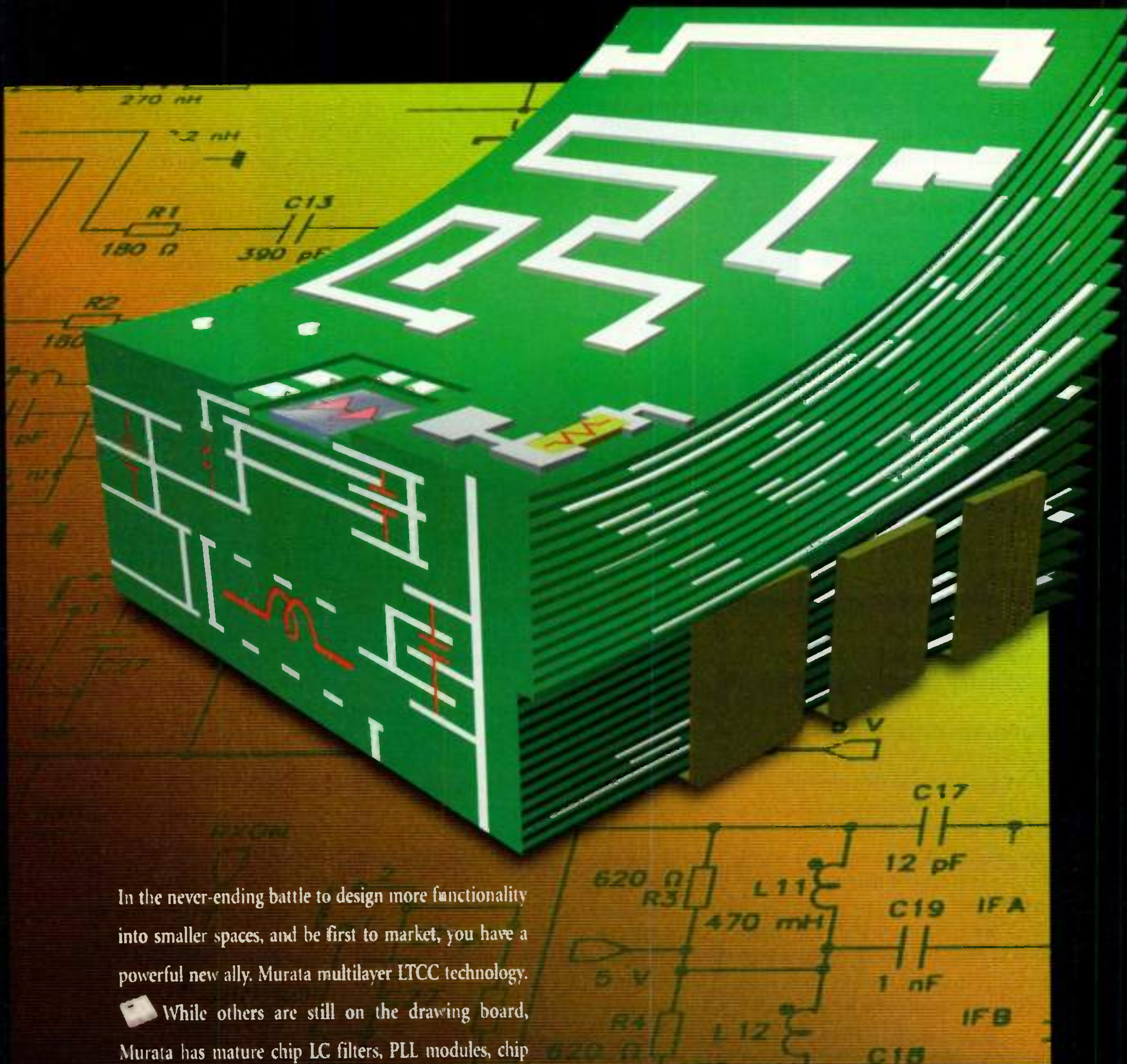
Figure 5 shows the sensor's steady state response for the reducing gas, CO, in a 0.4-torr environment of oxygen at several operating temperatures and a fixed bias voltage. The positive directions of the curves in Figure 5 versus the negative directions of those in Figure 3 reveal that the introduction of CO gas (or the reduction of pre-adsorbed oxygen by



5. The steady state response of the diamond-based Physitron sensor shows the change in device current as a function of carbon-monoxide partial pressure and temperature.



6. This figure shows the typical reproducibility of the diamond-based hydrogen and carbon-monoxide sensor from Physitron. Device response and recovery times are in seconds.



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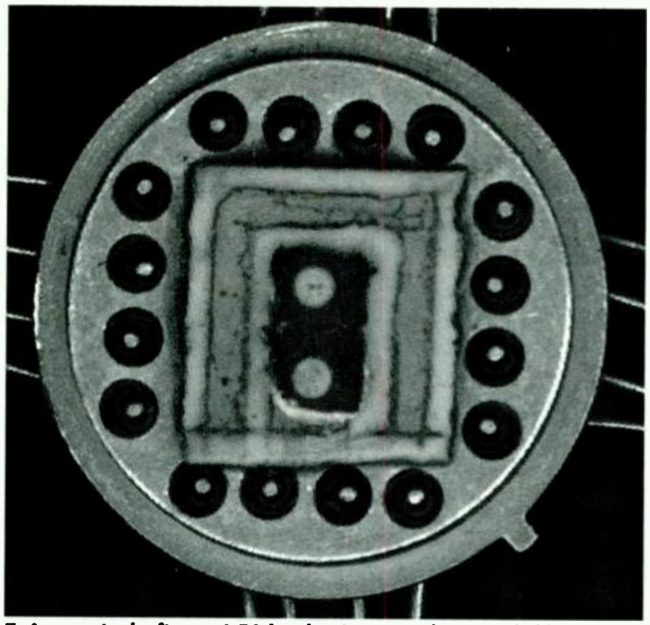
CO) increases the sensor's current. There's also an increase in ΔI with increasing temperature in the sensor's steady state response for CO gas. In a 9.4-torr environment of CO gas, ΔI is measured as 0.7 mA, 1 mA, and 1.5 mA for temperatures of 210°C, 225°C, and 240°C, respectively. There's no response to CO gas in the ambient with oxygen gas present.

Measurements made indicated that the sensor has typically reproducible results for O_2 and CO gases at a temperature of 300°C *(Fig. 6)*. The device's same transient behavior shows a response time in seconds, revealing that the response is fast enough and highly sensitive at that temperature.



7. As seen in the figure, A TO header, 1.5 cm in diameter, holds the Physitron diamond-based oxygen and carbon-monoxide sensor.

Oxygen Vacancies

Gas detection with the diamond-based sensor is achieved by the modification of the oxygen vacancies in the SnO_x film when it is exposed to oxidizing or reducing gases. SnO_x is a widegap semiconductor material with excess metal ions or oxygen vacancies, which act as donors, contributing electrons to the conduction band. When oxygen gas is introduced from the atmosphere at high temperatures, atomic oxygen can diffuse into the bulk region from the surface, leading to a decrease in the number of oxygen vacancies in SnO_x. Since the conductivity of SnO_x arises from the oxygen vacancies, the decrease of oxygen vacancies also decreases the conductivity. This modifies the voltage distribution that's across the SnO_x/intrinsic-diamond structure, leading to the decrease in the sensor's current.

CO detection is attributed to the reduction reaction between oxygen and CO, leading to the decrease of oxygen atoms (or increase of oxygen vacancies) in SnO_x. Increasing the oxygen vacancies also increases the conductivity of SnO_x, causing the sensor's current to recover in the presence of CO gas.

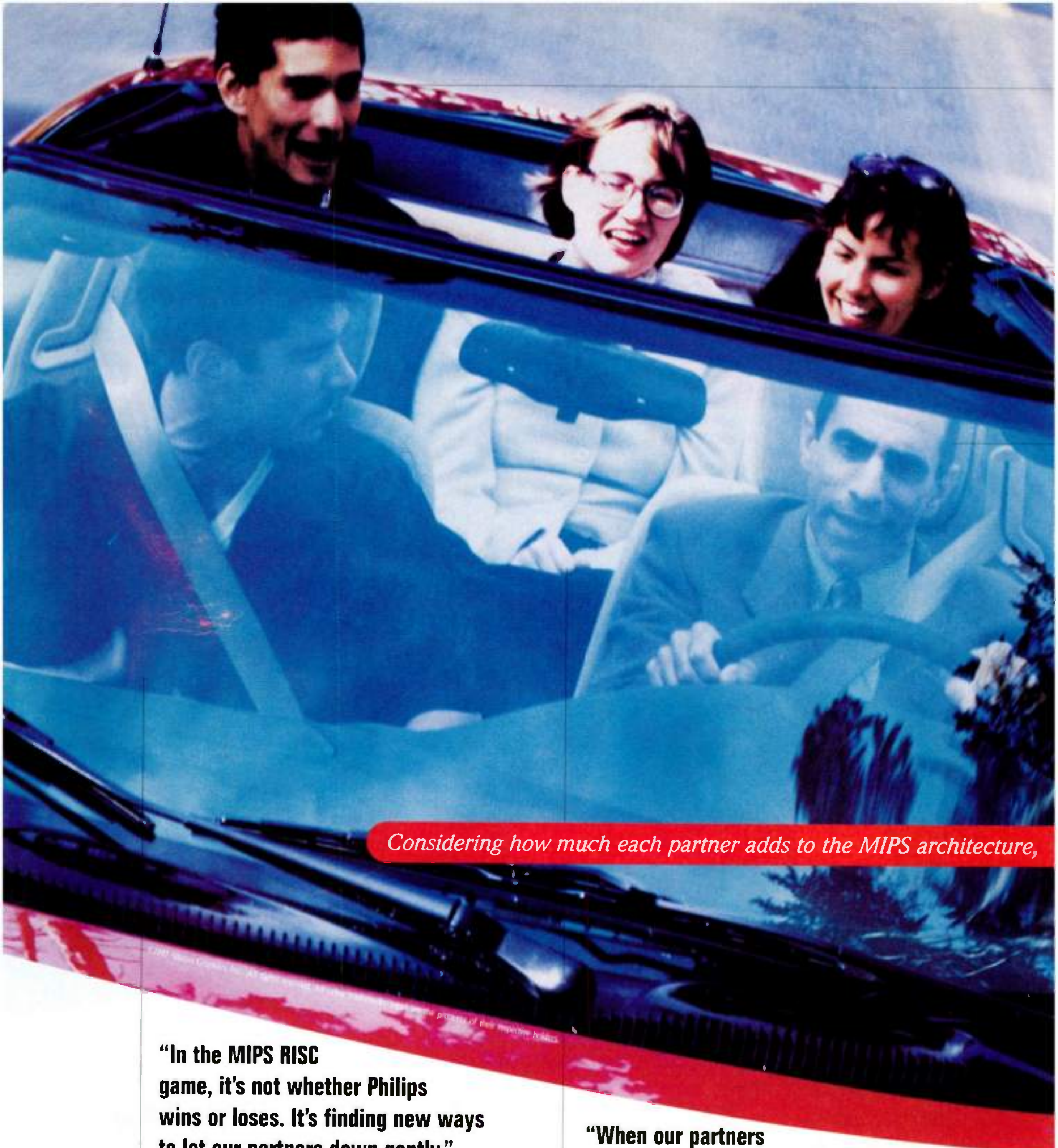
The sensor has been packaged in a TO header, 1.5 cm in diameter *(Fig. 7)*. Two devices are in the header to allow for background subtraction and temperature compensation. In addition, a heater is built into the substrate to allow operation at temperatures that enhance the sensor's responsivity. Future versions will incorporate the two devices as well as the heater into a single monolithic chip. The sensor can also be configured to sense other chemicals through design variations.

Physitron Corp. is looking for industrial partners to help further develop, manufacture and sell this technology. The sensor project is managed by T.G. "Bo" Henderson, vice president for Advanced Technology Applications.

For further information call (205) 534-4844; fax (205) 534-4846; e-mail: *bo@physitron.com*; the World Wide Web: *http://www.physitron.com*; or write to Physitron Corp., 3304A Westmill Dr., Huntsville, AL 35805.

Roger Allan

READER SERVICE 207



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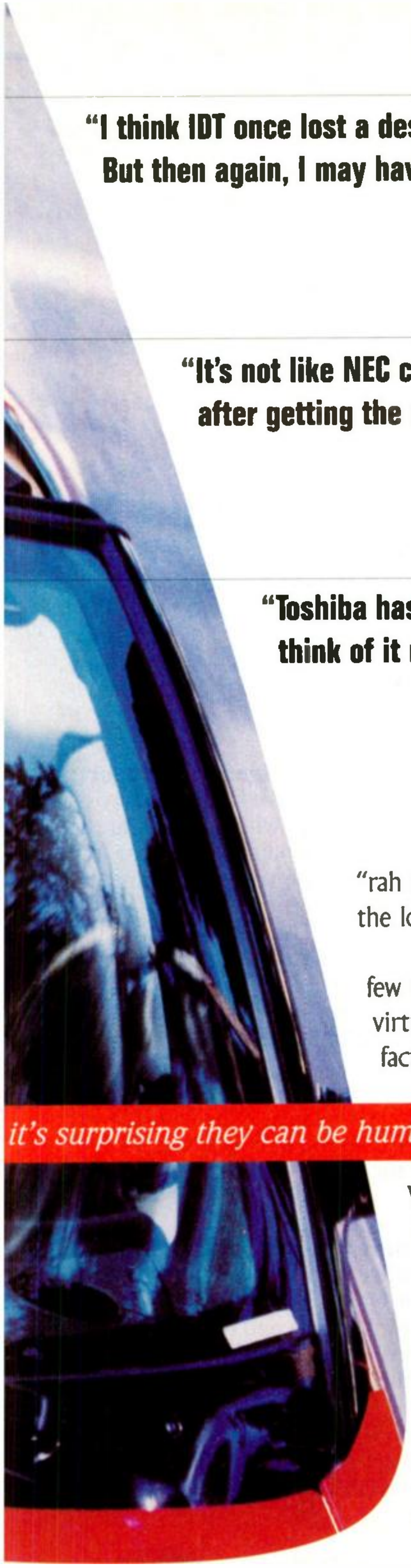

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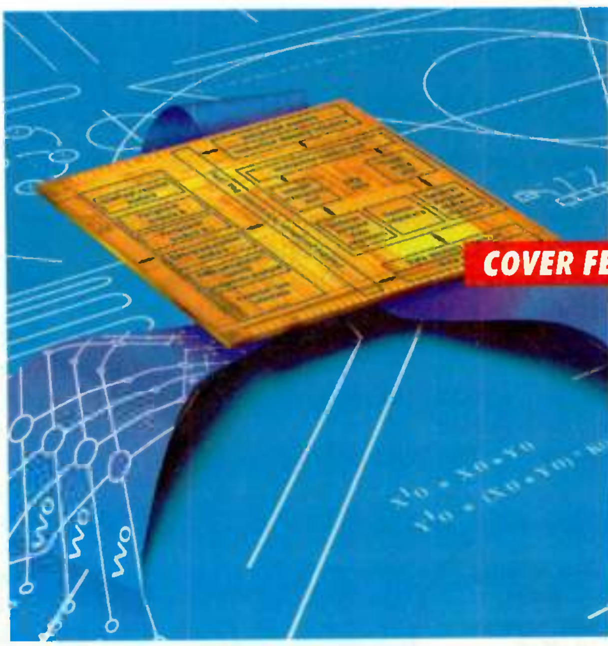
RISC Controller Merges DSP And Control Functionality

Tricore Processors Ease System Design By Combining The Best Features Of DSPs And High-Performance Embedded Controllers.

Dave Bursky



COVER FEATURE

In any complex control system, it is a rarity to not find the system employing either a 16- or 32-bit embedded controller or a digital-signal processor (DSP), or both a controller and a DSP chip. However, as power, space, and programming requirements force designers to look for chips that consume less power, provide higher levels of system integration, or can be programmed more efficiently, suppliers of controllers and DSP chips are merging the separate architectures so that a single chip can perform both control and signal-processing functions.

Several companies have tried to tackle such system needs by integrating separate DSP blocks onto embedded controllers, or adding simple DSP-type hardware support and instructions (multiply-and-accumulate (MAC), for example) to the CPU's instruction set. These first-generation solutions still require somewhat independent programming for the DSP and control operations, thus providing little synergy and program-code savings. Now, a more highly integrated solution, the Tricore processor family developed by Siemens, provides designers with a unified DSP/controller architecture that results in a single-chip solution that has a high code efficiency and consumes less than 1 W when running at 100 MHz.

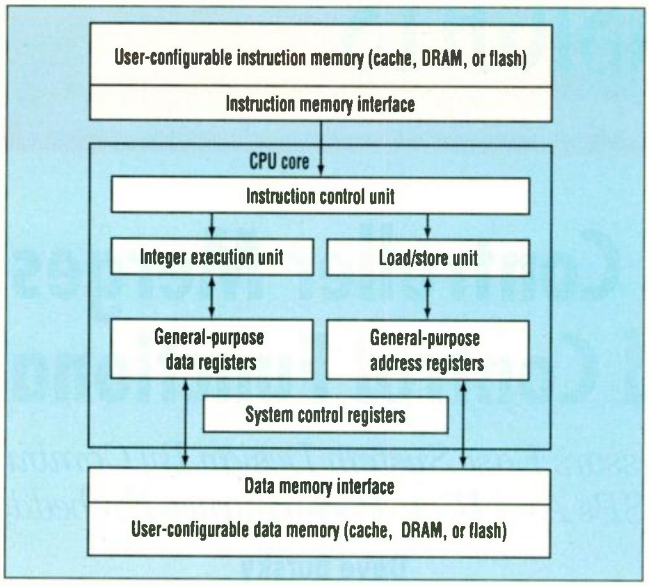
To achieve the high level of integration and performance, designers at Siemens started with a high-performance, three-instruction-issue 32-bit RISC CPU core. The core is based on a novel real-time multitasking engine that takes advantage of high-capacity on-chip memories and nanosecond context switching to provide control and DSP functionality from a single core. The core will be used as both a building block and as the heart of a family of standard products.

As mentioned earlier, Siemens will offer the Tricore in two forms—as a core and as part of a family of standard products. As a core building block, it allows designers to craft their own system-on-a-chip using the core and additional memory and peripheral building blocks (megacells) from the Siemens design library or custom blocks they create. As part of a family of standard products, it can be programmed and immediately be put to work.

The first chip in that standard family will contain the Tricore processor, a 2-kbyte instruction cache, a 2-kbyte data cache, a 2-kbyte data SRAM, two 64-kbyte blocks of embedded DRAM—one for data storage and one for program storage—and a generous selection of peripherals. Those peripherals include two UARTs, a synchronous serial channel, general-purpose timers, a watchdog timer, two DMA channels, an external bus interface that includes a controller for external memory, a boot-ROM interface, and a JTAG test port with on-chip debug support, all in a 144-lead plastic quad-sided flat package (Note: The 2-kbyte instruction cache can be used as both program memory and cache, 1 kbyte at a time).

The Tricore logic will initially be fabricated in a 0.35-µm CMOS process. It will operate at clock speeds of up to 100 MHz from a 3.3-V supply and deliver an average sustained throughput of about 130 MIPS. With such speed and the multitasking architecture, the core can deliver any combination of instruction performance—80 microcontroller

MIPS and 50 DSP MIPS or 40 microcontroller MIPS and 90 DSP MIPS, etc., depending on the problem to be solved. In 1999, Siemens expects to release a faster, 150-MHz version with a throughput of close to 200 MIPS, as well as a 100-MHz enhanced version with on-chip single-precision floating-point math. Even higher-performance, architecturally enhanced versions are planned for the new millennium.



2. The Tricore consists of the CPU and associated data and instruction memories. The CPU includes 32 general-purpose 32-bit registers that are subdivided into 16 data registers, 16 address registers, and a trio of system control registers. The superscalar 32-bit CPU in the core can issue up to three instructions simultaneously and executes a mix of 16- and 32-bit instructions to maximize code efficiency.

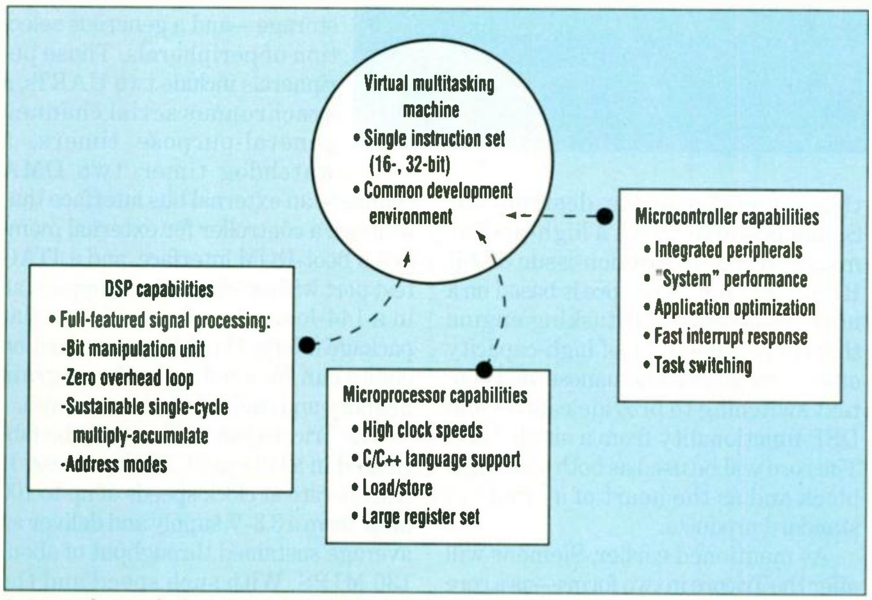
Many Applications

Applications for the combined DSP/control capability abound. One example is in the forthcoming generations of high-storage-capacity disk drives, which will require more exacting control and signal processing. With this single chip, designers can not only perform the control logic operations, but also the head positioning using a closed-loop DSP servo algorithm. The combined functionality (including the on-chip flash and RAM) could result in a single-chip solution where previous systems would require as many as five chips. DSP-based modems also would be good examples of where the Tricore would do well—the single chip would replace a DSP engine, a microcontroller, some RAM and flash memory, and other logic. Multifunction peripherals such as combination desktop faxes/scanners/printers also could take advantage of the functional integration offered by the merged control and DSP engine.

The "virtual" multiprocessor approach made possible with extremely fast context switching allows the Tricore to consolidate the functions of multiple 8/16-bit controllers and DSPs *(Fig. 1)*. By taking the key features of DSP engines, microprocessors, and microcontrollers, the processor is poised to deliver the best system performance versus price when compared to the other current solutions of separate DSP and controllers, or combined DSP/controller cores on a single chip.

The multitasking approach used in the processor needs some explanation. A task is an independent thread of control, and there are two types of tasks: software-managed tasks and interrupt service routines (SMTs and ISRs, respectively). SMTs are created through the services of a real-time kernel or operating system and are dispatched under the control of scheduling software. ISRs are dispatched by the hardware in response to an interrupt. In the CPU, ISRs refer only to code that is invoked by the hardware directly. SMTs are sometimes referred to as User Tasks, assuming that they will execute in user mode. Each task is allocated its own permission level and individual permissions are enabled/disabled primarily by I/O-mode bits in the program status word register.

Associated with any task is a set of state elements known collectively as the task's context (everything the processor needs to define the state of the associated task and enable its continued execution). The context is divided into an upper context, which consists of address registers of A10 to A15, data registers D8 to D15, and two program status registers; and a lower context, which consists of address registers A2 to A7 and data registers D0 to D7 plus the program counter. Upper context registers are designated as nonvolatile for the purposes of function calling. The remaining address registers—A0, A1, A8, and A9—are defined as system global registers and are not included in either context partition, and are not saved and restored across calls or interrupts. The operating system



1. By combining the key aspects of high-performance digital signal processors, microprocessors and microcontrollers, the Siemens Tricore architecture provides designers with a 32-bit RISC-based engine that delivers top-notch signal processing and control performance.

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PCM1719	DAC	16/18	96dB	100dB	-88dB	48kHz	+5V	28-Pin SSOP	11343	83
PCM1720	DAC	16/20/24	96dB	100dB	–90dB	96kHz	+5V	20-Pin SSOP	11333	84
PCM1723	DAC	16/20/24	94dB	96dB	–88dB	96kHz	+5V	24-Pin SSOP	11344	85
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will normally use them to reduce system overhead.

In the processor, tasks are switched when a trap or interrupt is taken, or when a return from exception is executed. The operating system causes a synchronous task switch by modifying the processor's return context pointer and issuing a return from the system call trap that invoked the OS. To take an interrupt, the interrupt control logic synthesizes a CALL instruction and inserts it into the execution stream. When the synthesized CALL is executed, the upper context is automatically saved and restored by hardware, while saving and restoring the lower context is left as an option for the new task. Linked lists are used to connect contexts when multiple interrupts are nested. And, since the core uses a wide bus to memory, all upper context registers can be saved or restored in two cycles.

Efficient Instructions

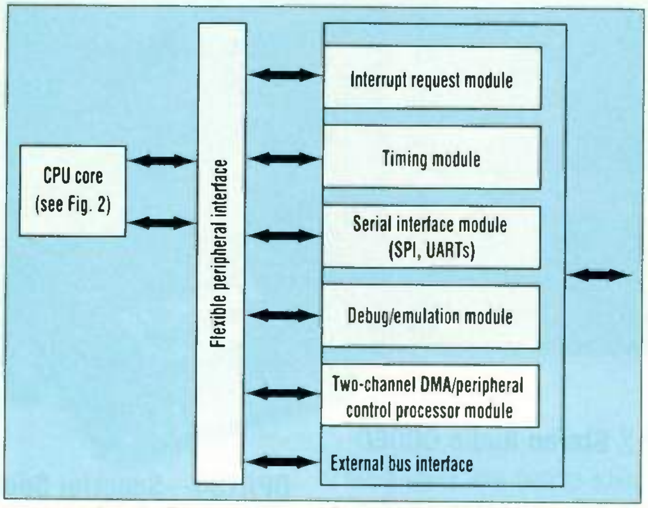
To obtain the seamless DSP and control capability, the Tricore processor employs a unified instruction set that contains a rich set of data types and addressing modes. In addition, the instruction set includes both 32- and 16-bit instruction formats, which can be freely intermixed, allowing the compilers to produce extremely compact program code, and achieving an estimated 30% savings in code space versus a 32-bit-only instruction set. Even though much attention was paid to saving code space, the core can address a 4-Gbyte unified data, program, and I/O address space, eliminating potential restrictions of a limited address range.

To handle DSP operations, the CPU was given the capability to perform saturating arithmetic, zero-overhead looping, and two 16-by-16-bit MAC operations in a single cycle. Also included in the core are instructions for Min, Max, Limit, and Subtract Absolute (for distance measurements). The processor handles complex addressing modes—butterfly and circular—such as needed for fast Fourier transforms—and real, complex, and matrix addressing.

Furthermore, the arithmetic unit can perform operations on packed data, executing two 16-bit or four 8-bit operations in parallel (two 16-by-16-bit or four 8-by-8-bit multiplies, for example), thus further speeding calculations. Word sizes also are flexible, with the processor capable of performing operations on 8- to 64-bit data words. The processor supports a wide range of data types as well—Boolean, bit strings, character, signed fraction, address, signed/unsigned integer, and IEEE 754 floating-point information.

Complementing the unified instruction set is a large, uniform register set (32 general-purpose registers—16 for addressing, 16 for data—plus three system registers—two for program status and one that serves as a program counter), and the ability to integrate large amounts of memory on the chip (up to 2 Mbytes of DRAM, or 512 kbytes of flash, or large blocks of SRAM, ROM, OTP, or some combination of these). Furthermore, thanks to the large design library available from Siemens, designers have a wide variety of peripheral building blocks they can select from to incorporate on application-specific versions of the chip.

The core itself consists of a 32-bit data path structured in a Harvard-style load-store architecture that can issue up to three instructions per cycle (*Fig. 2*). High DSP throughput also is supported by the ability of the core to sustain one MAC operation per cycle thanks to zero-overhead loop operation and the ability to load up to four 16-bit operands per cycle. Math operations can be performed with saturating arithmetic commands, which, in many cases, will result in more efficient coding and eliminates the need to set a mode bit. Floating-point operations are done in the first implementation of the Tricore via software emulation, although, as mentioned earlier, hardware floating-point support is planned for future versions.



3. Connecting the Tricore to the on-chip peripherals and the external world, the flexible peripheral interface bus provides an 800-Mbyte/s demultiplexed 32-bit address, 64-bit data path for peripheral support functions to tie into. In the first off-the-shelf version of the Tricore processor, the peripheral functions included on the chip comprise an interrupt request module, a timing module, a serial interface module, a debug and emulation module, and a two-channel DMA control module.

Bit and Boolean operations also are critical for various controller operations, and the Tricore comes replete with a large assortment of bit operations—bit logical, bit-field insert and extract, bit-field double extract, and others. Also included in the core is a fast hardware-supported task-switching mechanism (via a wide bus to memory) that allows the core to switch from a control to a DSP task in just two cycles (less than 100 ns). Interrupts are processed as injected tasks, thus keeping the program flow relatively simple.

To facilitate many of the high-speed operations, the core employs a wide memory interface (128 bits wide in the first implementation). Such a wide bus eliminates many of the bottlenecks that are typically encountered in integrated solutions that place DSP and CPU blocks on the same chip and only use a 32-bit bus. Thus, the wide bus allows the CPU to save the contents of up to 16 registers in two to four cycles when executing a CALL or interrupt operation. That also reduces the interrupt latency by avoiding long multicycle instructions.

As noted earlier, interrupts are implemented as hardware-injected CALL instructions; the target address of the CALL is calculated from the interrupt's hardware priority, which is a number in the range of 1 to 255. The interrupt priority number indexes a vec-

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Beyond The Core

The Tricore also is capable of controlling multiple on-chip peripherals and includes powerful memory protection and on-chip debug support. On-chip peripherals are interconnected to the core via the flexible peripheral interconnect (FPI) bus, which is a core-independent demultiplexed bus with up to 32 address bits and 64 data bits *(Fig. 3)*. It can handle a peak throughput of up to 800 Mbytes/s when clocked at 100 MHz.

The bus allows an unlimited number of peripheral modules to be connected, but only up to 16 masters (masters can initiate and control transactions, slaves only support simple reads and writes of registers, and master/slave blocks support advanced features such as split read transfers and error handling). Data can be transferred in 8-, 16-, 32-, or 64-bit wide words over the bus. Split transactions can be done to accommodate functions with long response times.

Memory support includes multiple protection modes (User 0, no peripherals; User 1, regular peripherals; and Supervisor, all peripherals and system registers. The memory also is protected with code and data-range tables, thus eliminating writes to code and read-only data, and execution of data. A CALL depth counter prevents runaway recursion and "return-to-nowhere occurrences," while a null-pointer check avoids potential wild null pointers. Debug support includes debug triggers for flexible breakpoints, and a bidirectional debug port that permits an emulator to access the internal state and communicate with a debugger.

The processor also includes a real-time trace feature to provide designers with a nonintrusive cycle-accurate trace capability. On a set of four pins, the processor can provide on a cycle by cycle basis the following information: the number of sequential instructions, whether the instruction is a loop operation, a relative or absolute branch, an indirect branch (along with the address), or an exception and interrupt (with the associated address). Addresses are sent through an additional 4-pin output in eight cycles via a FIFO buffer.

To aid in development, Siemens has created an instruction set simulator that it includes in the Tricore Design Kit. The simulator allows designers to benchmark the performance of the core against both dedicated DSP chips and general-purpose controllers that contain DSP enhancements. Initial results of simulations done using customer benchmarks indicate the DSP performance is equal to or better than both types of competitive chips, with the added benefit of the functional integration.

For software and hardware development Siemens has pulled together a variety of tools, some internally developed, some available from third-party suppliers (Tasking, Green Hills Software, Accelerated Technology, Nohau, Hitex, Ashling, Kontron, and others) that support high-level-language software development, compilers, real-time operating systems, simulators, and debug tools. These tools will complement the hardware and ASIC development tools that will allow designers to custom-craft their ideal solution. The typical hardware design flow might start with a Verilog or VHDL description, which can then go to logic synthesis tools and then on to a simulator/fault/timing analyzer and finally on to chip layout once known flaws are eliminated.

PRICE AND AVAILABILITY

The initial version of the Tricore will be ready for sampling in the second quarter of 1998. The processor will be housed in a 144-lead PQFP and will sell for between $10 to $15, depending on the volume. Although physical samples are not immediately available, the software tools are and designs of application-specific versions can start at once.

Siemens, 10950 N. Tantau Avenue, Cupertino, CA 95014; Tapan Joshi, (408) 895-5005; fax (408) 895-5020; e-mail: tapan.joshi@sci.siemens.com; Internet: http://www.siemens.com. **CIRCLE 540**

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Showcasing The Latest Advances In Bipolar And BiCMOS Processes

This Year's BCTM Demonstrates That 50 Years Later, The Bipolar Junction Transistor Is Still Growing Strong. **Frank Goodenough**

Conventional wisdom says that fine-geometry CMOS "can do it all." Design software will take intellectual property (IP) from a dozen different companies and put them all on one chip. In addition, the foundry's process, designed by software, will ultimately put high-voltage motor drivers, high-speed, high-resolution analog-to-digital converters (ADCs), and precision dc references onto a single chip, along with 0.1-µm fully depleted silicon CMOS on thin-film silicon-on-insulator (SOI) running multithreshold adiabadic logic at 1 GHz off a 1-V rail.

But it also is fairly common knowledge that bipolar devices couple a higher mobility and a higher transconductance than MOS devices (under many conditions, they offer lower noise for a given current). As a result, low-cost, exotic, bipolar or biCMOS processes will always be around to bail out the system designer with some form of deintegration.

Deintegration is defined as analog or digital functions in a tiny package to be sprinkled where needed throughout a system based on a mixed-signal "system on a chip" that after being built, can't cut it due to nonarbitrary limits on speed, accuracy, voltage, and output drive. That is, a couple of deintegration ICs, each built on a different process but using bipolar junction transistors (BJTs), can often save a system designer's project.

The 1997 Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), to be held in Minneapolis, Minn., Sept. 28-30, like its predecessors, remains a showcase for the latest versions of these standout processes waiting in the wings, with most of them designed for RF or communications circuits.

A short course on Sunday, Sept. 28, is devoted to the design of RF ICs. It consists of three separate two-hour presentations: "Process technology for low-power RFD applications," "Plastic packaging for RF/microwave applications," and RF ICs: Design for manufacture" *(see the conference table).*

Papers in several sessions are devoted to either RF or communication ICs or devices *(see "Bipolar Developments At BCTM Will Expand Communications Capabilities," p. xx).* Not only that, but most processes today can be simulated *(see "Advanced Models Eyed As Key To Accurate Simulation, p. xx).*

Two panel discussions are set for Monday evening, Sept. 29. The first is to come up with the top bipolar IC circuits of all time. The second is entitled "What the heck are universities teaching electrical engineers?"

BCTM papers remaining are divided up into four categories:

• Six papers cover silicon germanium (SiGe) processes, with four of them devoted to IBM's process.

• Four papers cover high-voltage devices ranging from 60 to 600 V.

• Four papers cover processes aimed at digital devices including a 0.25-µm biCMOS SRAM process.

• Five papers cover analog and mixed-signal processes, including a buried triple biCMOS pn-junction for color detection.

1997 IEEE BIPOLAR/BiCMOS CIRCUITS AND TECHNOLOGY MEETING

Time	Sunday, Sept. 28	
8:30 a.m.-5:00 p.m.	**Short course** Process technology for RF, packaging for RF, and design for manufacturability	
	Monday, Sept. 29	
8:45 a.m.	**Keynote speech—Simon Atkinson** The outlook of bipolar/biCMOS for future telecom ICs	
9:50 a.m.	Statistical modeling	SiGe biCMOS and advanced bipolar technology
12:00 noon	**Luncheon speaker—Jim Early** Celebration of the "50th anniversary of the bipolar transistor"	
2:00 p.m.	RF design	biCMOS technology
3:50 p.m.	RF circuits and components	Physics and novel devices
8:00 p.m.	Top 10 bipolar circuit ideas of all time	What the heck are universities teaching electrical engineers?
	Tuesday, Sept. 30	
8:30 a.m.	Analog circuits	Modeling of power devices
10:30 a.m.	Power devices	Interconnect, modeling, and extraction
2:00 p.m.	Communication circuits	High-performance SiGe HBTs/BJTs
3:50 p.m.	Late news I	Late news II

TABLE 1. A COMPARISON OF STANDARD HBTs AND HBTs DESIGNED FOR HIGHER B_{VCEO}

Parameter	Standard HBT	High-BV_{CEO} HBT
Beta (β)	113	97
V_A	61 V	132 V
B_{VCEO}	3.3 V	5.3 V
B_{Vebo}	4.2 V	4.1 V
f_t	48 GHz	28 GHz
f_{max}	69 GHz	57 GHz

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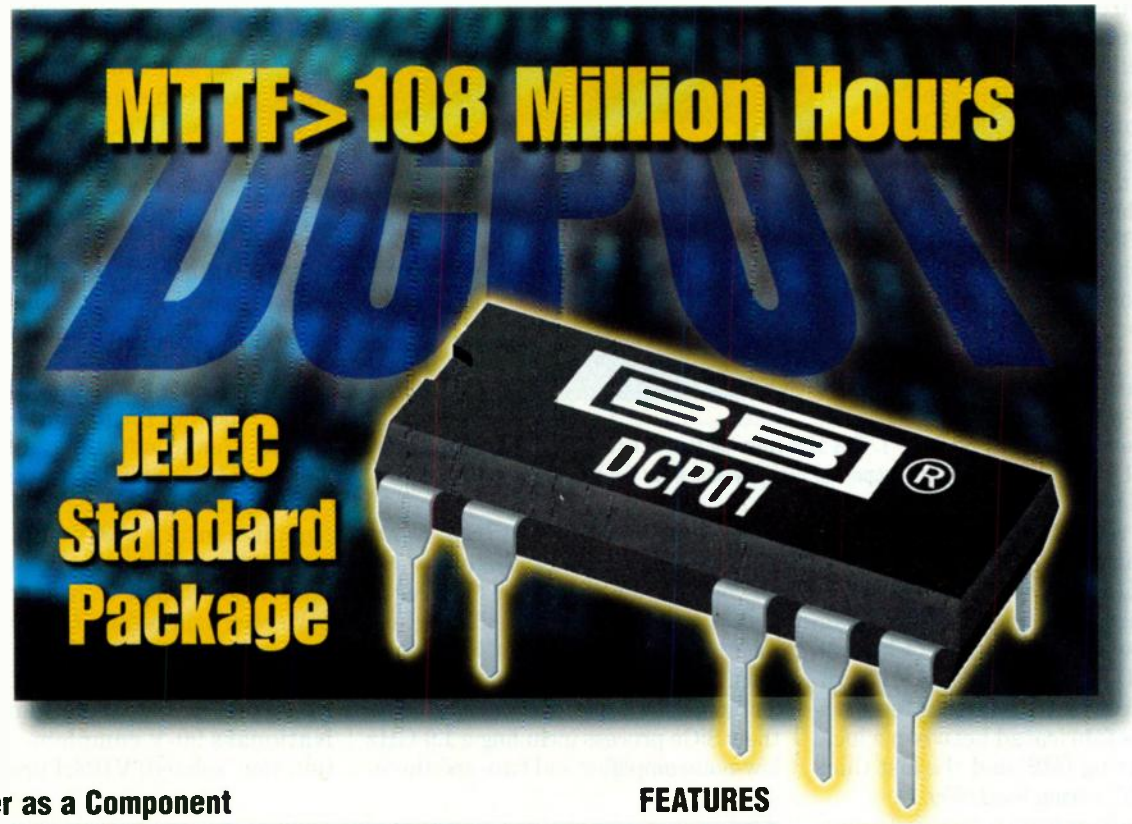

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DCP010512P	5V	12V	72%	1000Vrms	400kHz	14-Pin PDIP	11366
DCP010515P	5V	15V	73%	1000Vrms	400kHz	14-Pin PDIP	11367
DCP010505DP	5V	±5V	71%	1000Vrms	400kHz	14-Pin PDIP	11336
DCP010512DP	5V	±12V	72%	1000Vrms	400kHz	14-Pin PDIP	11357
DCP010515DP	5V	±15V	75%	1000Vrms	400kHz	14-Pin PDIP	11356
DCP011512DP	15V	±12V	76%	1000Vrms	400kHz	14-Pin PDIP	11382
DCP011515DP	15V	±15V	76%	1000Vrms	400kHz	14-Pin PDIP	11382
DCP012405P	24V	5V	65%	1000Vrms	400kHz	14-Pin PDIP	11383
DCP012415DP	24V	±15V	76%	1000Vrms	400kHz	14-Pin PDIP	11383

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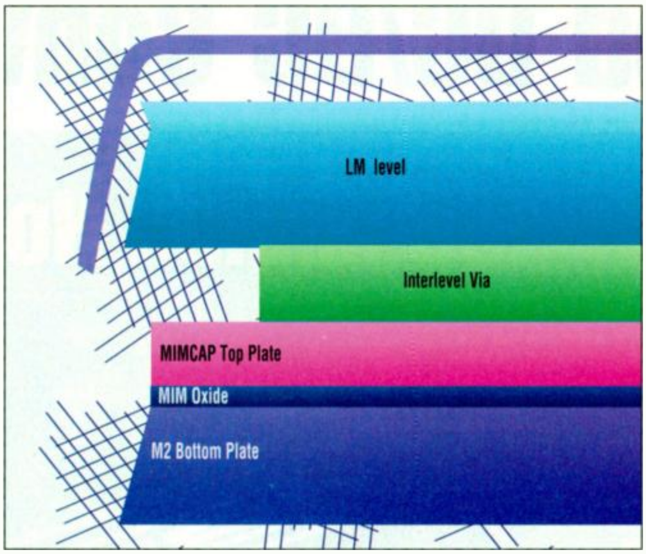
No matter how fast a process runs, at some point system designers still need resistors, capacitors, and if any kind of measurements are being made, a voltage reference. And after building a number of high-speed mixed signal and RF circuits for their biCMOS SiGe process, three IBM teams explored these items and came up with three separate papers.

One IBM team investigated the effect of their process on polysilicon resistors. A joint team from IBM and Analog Devices, Wilmington, Mass., developed a unique new metal-insulator-metal (MIM) capacitor on the process, and a joint Auburn University, Auburn, Ala./IBM team came up with a bandgap reference. The team came up with a planar, MIM capacitor that offers a higher Q for RF applications than conventional capacitors. However, it can handle low-frequency tasks such as bypassing. Dubbed the MIMCAP, it is superior to conventional substrate capacitors. It is fabricated between a local metal wiring (M2) and the last thick metal (LM) wiring level *(Fig. 1)*.



1. This SEM cross-section of a corner of a SiGe HBT shows the MIM/dc capacitor IBM developed for the process.

The resistor team performed a number of experiments on the process window for the polysilicon resistor in their SiGe HBT process. The accuracy and stability of these resistors is critical to maintaining a precise current in some analog and mixed-signal circuits. They studied the effects of implant energy, dosage, and polysilicon structure on the polysilicon resistor itself and on the p-i-n diode and npn transistors from the process. They came up with a low-temperature-coefficient resistor, the manufacture of which does not effect the speed of the other active devices the process puts on the same die.

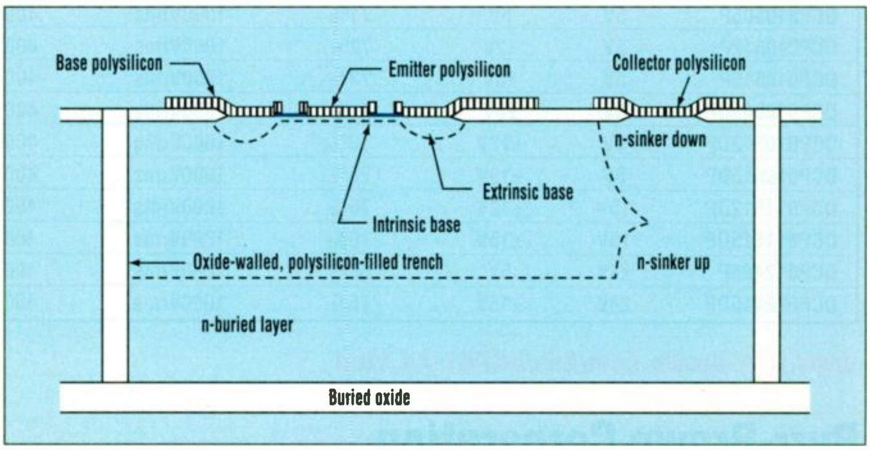
The reference team came up with a conventional bandgap which they simulated successfully on Spice. A fourth IBM-team paper describes additional process steps added to that of their basic 47-GHz RF HBT in order to build several new structures with similar performance. These include an n-FET and a p-FET and an npn HBT with a breakdown voltage of 5.3 V instead of 3.3 V for use as an output device in RF circuits in lieu of GaAs MESFETs *(see tables 1 through 3. Note: For more information on SiGe, contact David Harame at IBM, Essex Junction, Vt., at (802) 769-0111).*

The two remaining BCTM SiGe papers come from Temic, Heilbron, Germany, and the University of Southampton, England. The Temic team describes a number of circuits they fabricated on their SiGe process including a 1.9-GHz low-noise amplifier, and two- and three-stage RF power amplifiers. The relative performance of silicon BJTs, GaAs MESFETs, and SiGe HBTs in similar circuits also is discussed. The Southampton team simulated the effect of enhanced boron out-diffusion from the base of a SiGe HBT due to an extrinsic base implant. If the HBTs are built on a CMOS process, ideally the implants also are used to fabricate the source and drain of the p-channel FETs and the HBT's extrinsic base.

Speed combined with high voltage on the same chip? "Conventional wisdom" says no way. But a team at National Semiconductor, Santa Clara, Calif., didn't listen. They describe a process that puts complementary 170-V npn and pnp transistors on the same chip with 30-V npns. High-voltage transistors on ICs have been built before but now they've been built with an ft of 1 GHz (the f_t of the pnp transistor is a mere 900 MHz). These process engineers started with National's 90-V complementary JI (junction isolated) VIP3H process and

TABLE 2. A SUMMARY OF nFET AND pFET DEVICES

Parameter	nFET	pFET
Threshold voltage—linear (long)	0.58 V	-0.55 V
Threshold voltage—saturated (20x.5)	0.56 V	-0.40 V
$L_{effective}$ (0.5 µm drawn)	0.36 µm	0.36 µm
g_m, sat.	190 mS/mm	103 mS/mm
Series resistance	440 Ω-µm	2000 Ω-µm
I_{drain}, sat.	468 µA/µm	231 µA/µm
Source/drain capacitance per area	0.91 fF/µm^2	0.86 fF/µm^2



2. This fast high-voltage silicon-on-insulator (SOI) process allows the building of 170-V complementary npn and pnp transistors.

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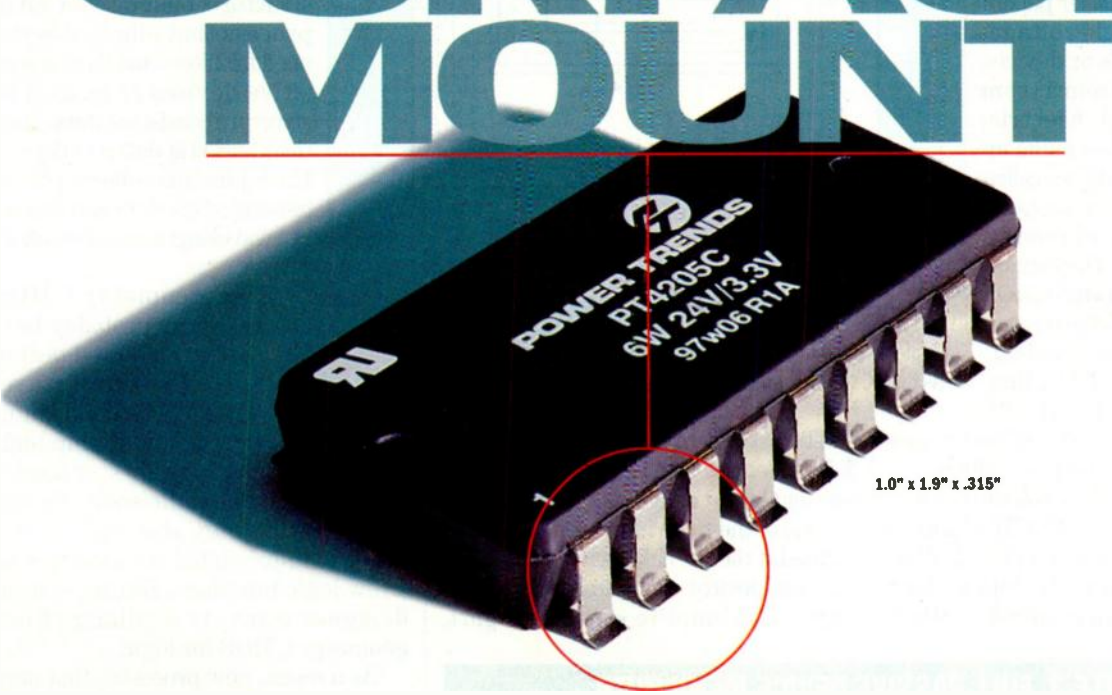

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	Outputs		Input Voltage Range	
Power	Vo	Io	18 - 40V	36 - 75V
3W	2V	1.5A	—	PT4201
5W	3.3V	1.5A	PT4205	PT4202
6W	5V	1.2A	PT4206	PT4203
6W	12V	0.6A	—	PT4204
7W	+5V / -5V	1A ea	—	PT4301
7W	+5V / +3.3V	1A ea	—	PT4302
15W	3.3V	4.5A	—	PT4110
15W	5V	3A	PT4104	PT4101
15W	12V	1.2A	PT4105	PT4102
15W	15V	1A	PT4106	PT4103

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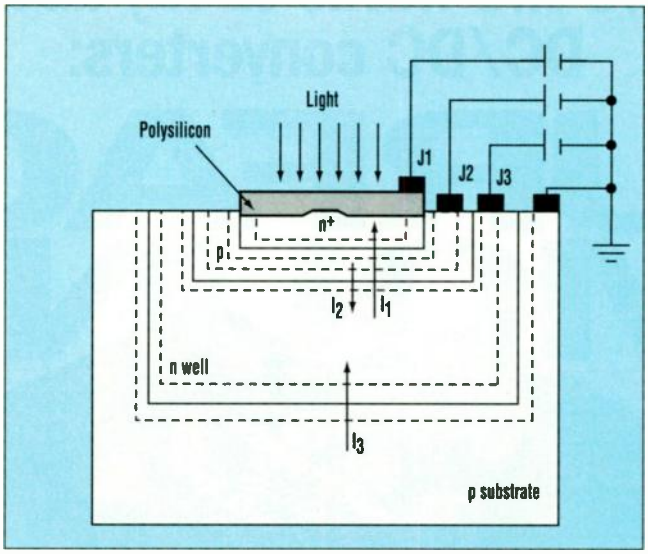
with a few modifications put it on bonded wafers in dielectrically isolated tubs *(Fig. 2)*.

This SOI process will be used for video CRT drivers, high-power audio amplifiers, and subscriber-line interface circuits (SLICs). Other papers describing high-voltage, power-control ICs or devices include a paper from a team from Mitsubishi Electric, Hyogo, Japan. They came up with a new kind of device called a DAD (dual-action device). Both p- and n-channel versions are rated at 600 V. They are directly driven by on-chip CMOS logic and in turn drive on-chip lateral IGBT "totem poles." Like the National BJTs, they also are built on an SOI substrate. Both employ "resurf" techniques to enhance their breakdown voltage.

The remaining high-voltage devices are described in a pair of biCMOS papers from Texas Instruments (TI), Dallas, and Toshiba, Kawasaki, Japan. Both cover processes that put 60-V MOSFETs on the same process as 5-V MOSFETs along with a variety of low-voltage and high-voltage bipolar devices.

One of the more interesting chips described at the BCTM, a color detector (an "analog" device), comes from a device designer at Alcatel Telecom, Stuttgart, Germany. Most color detectors require at least three separate photodiodes per pixel, each with a separate bandpass (RGB) color filter between it and the source of color. This paper describes a single bipolar structure, built on a biCMOS process that eliminates the need for filters and 3 photosensitive devices *(Fig. 3)*. The structure consists of three junctions buried at different depths. Each junction collects photogenerated carriers and results in a wavelength-sensitive photo current.



3. Triple pn junctions J1, J2, and J3,allow the building of a color-detection IC that needs no color filter or additional pixels.

Fine-geometry CMOS processes can probably handle most or all digital design limits for the near future. However, if system designers must move to a unique chip built on an "exotic" (by their standards) process just to handle some special analog tasks, they also will try and use it to improve the performance of a few logic functions. But no system designer wants to challenge fine-geometry CMOS for logic.

As a result, new processes that only improve digital performance may not be acceptable. They must be able to build high-performance analog functions, such as references as well—and that means the βV_A product of bipolar devices from the process must be 1000 or better. On the other hand, most advanced analog processes can handle digital functions without any problem. And since most RF circuits are (or can be) virtually devoid of current sources, they do not necessarily need a process with a good βV_A product.

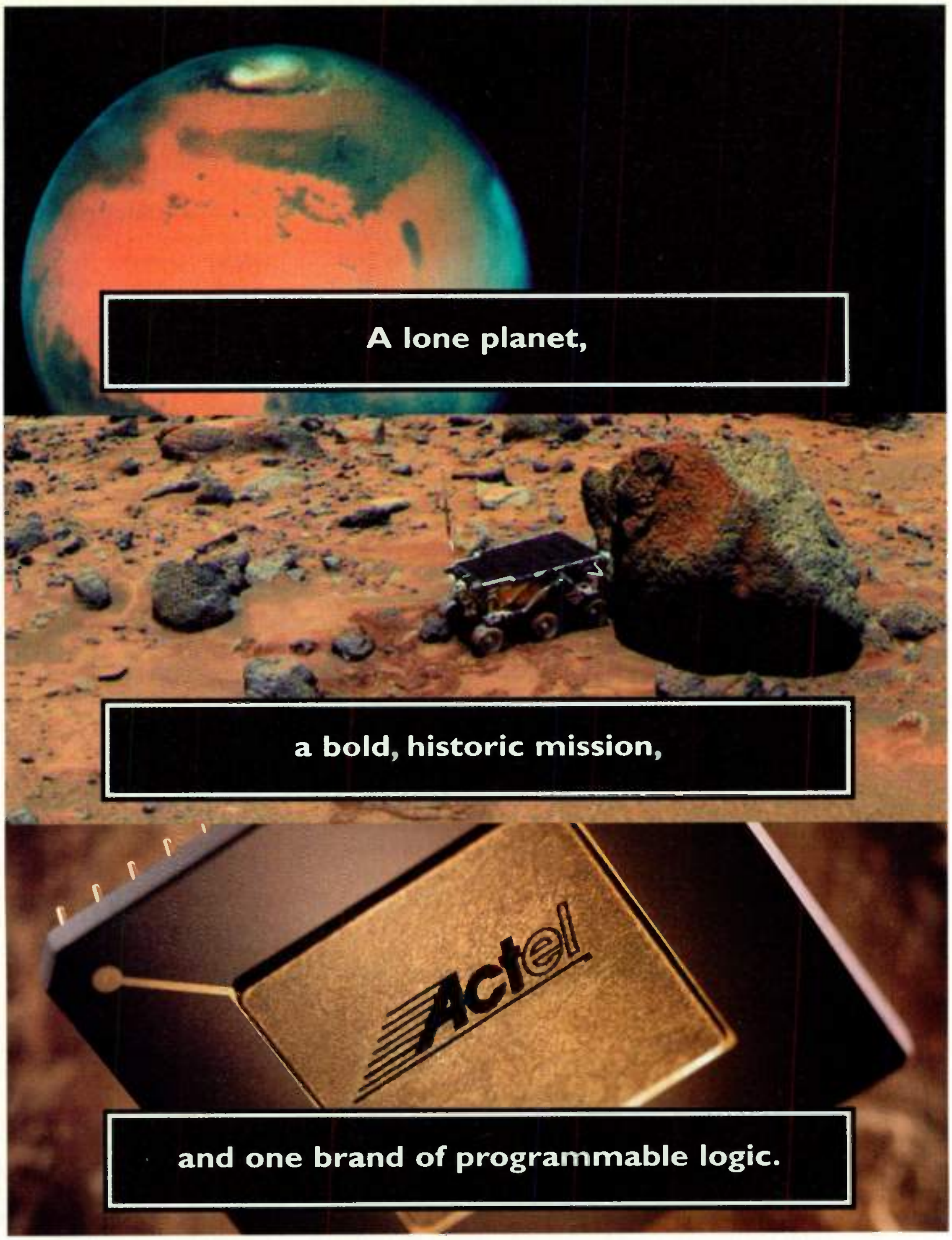
TABLE 3. FULL PASSIVE DEVICE MENU WITH RELEVANT MEASUREMENT VALUES

Device	Value
Implantable resistor	1.6 kΩ/square
Polysilicon resistor	342 Ω/square
DC capacitor	1.52 fF/μm^2
MIM capacitor	0.695 fF/μm^2
Inductor (6-turn)	10 nH
Inductor Q (0.8 GHz)	3.8
Substrate diode V_f (5 x 5 μm^2)	213 mV (@100 μA)
p-i-n diode V_f (2 x 20 μm^2)	790 mV (@100 μA)
Varactor V_f (2 x 20 μm^2)	810 mV (@100 μA)

Bipolar Developments At BCTM Will Expand Communications Capabilities

Research Presented At BCTM Aims To Boost Wired/Wireless Communications Performance, With Availability Predicted Within A Year. **Lee Goldberg**

The 1997 Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), to be held on Sept 28-30 in Minneapolis, Minn., is a great place to get a firsthand look at the emerging bipolar developments that will help shape the future of the communications industry. Although MOS technology has dominated the spotlight for much of the past decade, this conference underscores the fact that, at least today, there are still areas where there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is no substitute for the inherent speed, linearity, and flexibility of bipolar devices.

The communications market is one of these areas, a place where bipolar technology is leading the way and enabling the realization of ever-more sophisticated products. Attendees at BCTM will have the opportunity to get a good look at developments that will push performance, power, and price barriers for RF devices, wireless and optical networks, and high-speed signal pocketing.

RF Device Developments

Among the more interesting recent trends in RF devices is on-chip passive components. Although it has been possible to fabricate micro-inductors and capacitors on silicon for several years, their utility has been limited by the lower "Qs" that the low resistivity of the doped substrates has permitted. Attendees to Session 5 will see an interesting solution to this dilemma, as researchers from Bell Labs, Murray Hill, N.J., present "An approach for fabricating high performance inductors on low-resistivity substrates" *(Session 5.3)*.

The new process they developed involves using layers of porous, unoxidized silicon to isolate spiral inductors from the actual substrate. Using an isolation layer up to 250-µm thick, the researchers successfully fabricated 9-nH inductors with Q's of 5 at 1.8 GHz using the standard metallization layer that also is used for forming interconnects on the IC's surface. The porous silicon layer is created using an electro-chemical etching process.

Larger inductors with values of up to 150 nH also were fabricated that proved useful to nearly 1 GHz. Besides discovering valuable design trade-off methodologies for optimizing inductor in a given application, the team is optimistic about further developments that will yield even higher quality components. This capability is becoming increasingly important as wireless systems become more integrated and consumer-oriented.

The chronic problem of thermal instability in power transistors was addressed by a team from Stanford University, Stanford Calif., and Ericsson Components, Kista, Sweden. In their paper, "Improved performance and thermal stability of interdigitated power RF bipolar transistors with nonlinear base ballasting" *(session 9.1)*, the authors note that emitter ballast resistors are usually used to prevent the gain collapse and thermal instability experienced by bipolar transistors with interdigitated structures when different parts of the chip heat unevenly during high-power operations. The problem with this approach is that the ballast resistor value is extremely critical and may still degrade performance.

Instead, the scientists proposed a novel scheme that employs a nonlinear base ballast resistor implanted on each finger of the base structure. Their research indicates that there is little or no performance degradation of the transistor under normal operating conditions. The test transistor was modeled and then fabricated with a depletion-mode MOSFET serving as the base resistor. Initial tests show that this technique is very effective for HBTs, although not quite as effective for BJT structures. If adopted commercially, this technology may help extend the talk time and operational life of battery-powered wireless equipment, as well as reduce the thermal problems associated with high-power RF circuits.

Walk On The Wireless Side

RF-based wireless systems will be one of the major beneficiaries from the developments at BCTM. Sessions 3 and 5 contained a wealth of developments that should show up in the commercial world within the next one to five years. Among the more interesting offerings in session 3 is "An integrated silicon bipolar receiver subsystem for 900-MHz ISM band applications" *(session 3.2)*. In this paper, Jeff Durec from Motorola, Tempe, Ariz., describes a wide band dual-conversion receiver subsystem that can be used for a wide variety of data and voice applications, including cordless telephones.

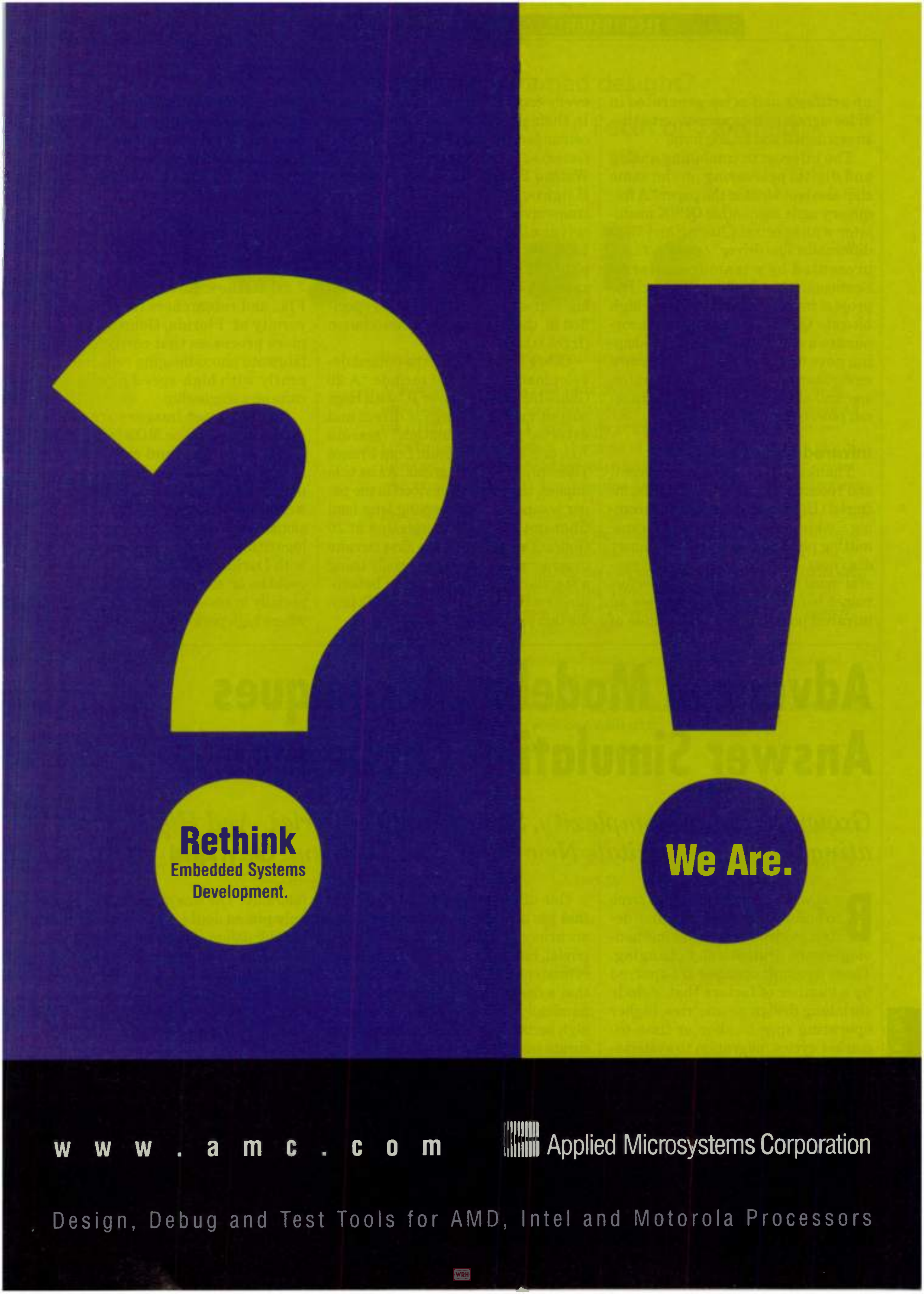
Capable of operating on voltages from 2.7 to 6.5 V, the circuit incorporates an LNA, two mixers, two oscillators, a second LO amplifier, a dual-modulus prescaler, an IF amplifier, RSSI circuitry, a coil-less demodulator, and power-down control logic, and provides up to 118 dB of dynamic range. In addition to discussing the chip's architecture and performance, the author provides interesting insights as to how the shielding and isolation between the various subsystems was implemented. The use of on-chip passives will probably become one of the more significant challenges for engineers as RF products become increasingly integrated.

Also of note was the paper "A silicon bipolar broadband PLL building block integrated circuit" *(session 5.1)*, presented by a team from Hughes Research Labs, Berkeley, Calif., and the University of California. The IC block integrates a prescaler with a selectable divide ratio, a phase detector, a VCO suited for production testing, and has an operating range from 500 MHz to 9 GHz. Since it is a prototype for commercial applications, it was housed in an inexpensive 16-pin plastic DIP. Commercial descendants of this component should find their way into satellite receivers, PCS equipment, and other emerging markets where multi-GHz applications are becoming consumer-oriented.

High-performance, wideband applications such as cellular base stations will probably benefit from the discussion on digital AGC circuitry posed by Jim Bales of National Semiconductor, Fort Collins, Colo. In his paper, "A biCMOS digitally controlled variable gain wideband amplifier" *(session 5.2)*, Bales explains that many high performance digital radio systems are now incorporating digitally controlled amplifiers ahead of the their analog-to-digital converters (ADCs) to limit incoming signal amplitudes. The single-chip amplifier presented in the paper is capable of running with nearly any existing high-speed ADC, and permits incremental gain adjustments in 6-dB steps across its entire –18 to +24 dB range.

Filters And Signal Processing

One of the more interesting papers at BCTM discusses how active filtering is becoming increasingly important in multimedia applications. Presented by Micro Linear Corp. researchers, "A biCMOS reconstruction filter with Sinx/X correction" *(session 7.4)*, illustrates how a bipolar chip that integrates multiple multi-pole filters and a clamping circuit can be used to clean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MOS, CMOS, GaAs, and discrete. In particular, the paper examines a number of models ranging from full 3D and transmission lines to lumped elements. Designer fundamentals and a practical understanding of the principles used in modeling and analysis also are presented.

A number of other papers highlighted at this year's conference focus on either improvements to existing models for simulation or on the development of new models. One example is "Simultaneous Extraction of Thermal and Emitter Series Resistances in Bipolar Transistors," a joint effort by researchers at Carleton University's Department of Electronics, Ottawa, Canada; Rockwell Semiconductor Systems, Newport Beach, Calif., and Northern Telecom Ltd., Ottawa, Canada. The method, which is applicable to other compact models such as VBIC or the SPICE Gummel-Poon model with self-heating, ensures mutually consistent values by performing these extractions simultaneously. This method also allows for the accurate determination of these values from data measured in an operating region where both series voltage drop and self-heating are important. As a result, it can provide a highly accurate prediction of actual characteristics.

Accurate bondwire modeling has taken on particular significance in recent years due to increasing frequencies in both analog and digital ICs. These bondwires are often used to interconnect ICs and packages. Typically, an estimation of the wire inductance is used to model the electrical behavior of the bondwires. In critical applications, though, the ability to accurately predict inductance becomes an issue. According to a paper from the Delft University of Technology, The Netherlands, "Microwave Modeling and Measurement of the Self- and Mutual Inductance of Coupled Bondwires," it is now possible to consider the modeling of bondwires based on the wires' geometry in conjunction with an inductance estimation derived using the Neumann equation. This technique works by comparing Neumann's inductance formula with measured self- and mutual inductances at microwave frequencies up to 10 GHz. After the measurement data is unembedded for parasitic capacitances and the coplanar interconnect line, the self- and mutual inductances can then be extracted. This technique has been proven to work for microwave measurements spanning the 45-MHz-to-10-GHz range, with differences of less than 10% between the calculated self-inductances and the measurements.

Statistical Spice modeling and simulation have traditionally been necessary steps in IC design in modern bipolar and BiCMOS technologies. In the area of statistical modeling, three papers at the conference stand out. The first, from Analog Devices, Limerick, Ireland, discusses a new methodology by which Spice-level model parameters can be derived from E-test (WAT) data for a 0.6μm BiCMOS process. Effectively, the technique works by transforming a database of E-test parameters into a desired database of Spice model parameters. Initially, an independent uncorrelated subset of E-test parameters is isolated. Then, correlated Spice-level device model parameters, measured using traditional approaches, are related to this core E-test parameter subset. A system of equations, including linear and interaction terms, can then be derived that link the model parameters to the E-test subset. The paper, "Statistical Modeling for a 0.6μm BiCMOS Technology" details the generation of these Spice-level parameters and addresses how it enables the extraction of accurate worst-case models for MOS and bipolar junction transistor (BJT) devices.

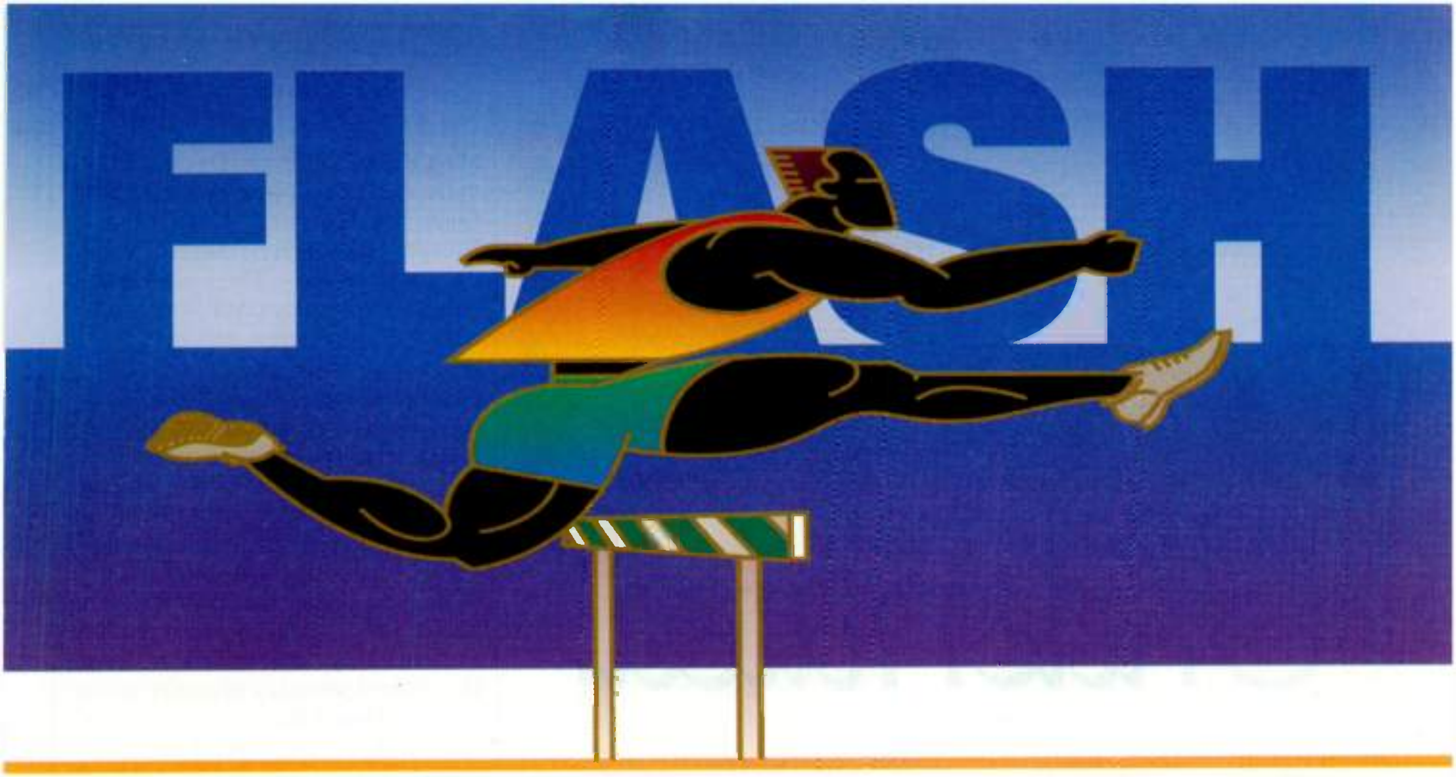
In a similar paper, "Efficient Statistical BJT Modeling, Why β is more than $1_c/I_b$," from Motorola Inc., Tempe, Ariz., a new method for generating distributional statistical BJT models is presented. The method is based on process-control data, process and geometry-level modeling, sensitivity analysis, and backward propagation of variance (BPV). This technique allows for the accurate modeling of BJT electrical behavior with a minimum of characterization effort. The process-control data is used to infer variations in process parameters, and takes only minutes to run on an engineering workstation. This method has been shown to work for a doubly diffused, vertical PNP transistor. While the method also has application to such devices as polysilicon emitter transistors and lateral PNPs, different formulations of the original method are required for successful modeling.

Another statistical Spice model, presented in "A Scaleable, Statistical Spice Gummel-Poon model for SiGe HBTs," was developed through a joint effort from IBM Microelectronics Division, Hopewell Junction, N.Y.; Hughes Space and Communications Company, Los Angeles, Calif.; and the IBM Microelectronics Division, Burlington, Vt. The model successfully proves that both scaling and statistics can work within the constraints of the Spice Gummel-Poon (SGP) model for a SiGe heterojunction bipolar transistors (HBT) process. The joint effort accurately models the ac and dc characteristics of an open-ended set of devices with up to 10X variation in either dimension. It uses simulation language extensions built into the HSpice circuit simulators to implement a model for the SiGe HBT process. SGP parameters are then scaled from input layout dimensions using simple equations. The resulting dc and ac fit is considered acceptable for most applications. Once a good fit is obtained across a statistically relevant range in emitter sizes, a statistical model can then be developed using the Monte Carlo distribution capability built into HSpice.

Modeling Bipolar Parasitics

A number of other developments are now making it possible to accurately model the parasitic behavior of bipolar devices that are used in advanced smart-power technologies. The first comes from Motorola Inc., Tempe, Ariz., and is detailed in "A Four-Terminal Compact Model for High-Voltage Diffused Resistors with Field Plates." The development is a four-terminal resistor model that accounts for depletion, inversion, and accumulation at the surface due to metal field plates, as well as the depletion-pinching effect at the sides and bottom of the resistor diffusion. In this method both the junction-depletion-pinching effect and the MOS-surface effect on resistor behavior are taken into account.

A method for improving bipolar transistor models is detailed in "Mod-



A JUMP AHEAD

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For more information on Flash MCUs from the leader in on-chip memory integration, please contact Motorola at (800) 765-7795, ext. 999 or visit http://www.mcu.motsps.com.

FLASH MICROCONTROLLERS

Device	CPU	Flash	Memory	Timer	Peripherals	Package
68HC912B32	16-bit	32K	1K SRAM, 768 EEPROM	16-bit	A/D, 4 PWM, SCI, SPI	80 QFP
68HC916R1	16-bit	50K	2K SRAM	CTM7	2 SCI, SPI	132 PQFP
68HC916X1	16-bit	50K	2K SRAM	GPT	A/D, 2 PWM, SCI, SPI	120 QFP
68HC916Y1	16-bit	48K	4K SRAM	TPU, GPT	A/D, 2 PWM, 2 SCI, SPI	160 QFP
68HC916Y3	16-bit	100K	4K SRAM	TPU2, GPT	A/D, 2 PWM, 2 SCI, QSPI	160 QFP
68F333	32-bit	64K	4K SRAM	TPU	A/D, SCI, QSPI	160 QFP

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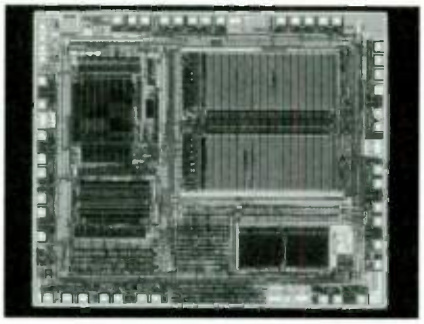
eling Parasitic Bipolar Devices in Advanced Smart-Power Technologies," from the University of Bologna, Bologna, Italy, and ST-Microelectronics, Catania, Italy. The model is successful in correctly predicting the behavior of the reverse current gain. It also is especially useful for modeling parasitic devices of the complex multi-terminal bipolar and MOS transistors found in advanced smart-power technologies. At the heart of the technique is a new formulation for reverse current gain that allows good modeling of parasitic bipolar transistors. This new formulation takes into account high injection effects in light-doped regions. It is currently being utilized to design the control circuitry of smart-power integrated circuits.

An alternative strategy to circuit-oriented power-device modeling is presented in "A Distributed Regional Modeling Approach for Power Bipolar Devices in Circuit Simulation," from the Laboratory of Analysis and Systems Architecture in Toulouse, Cedex, France. Most modern day circuit-oriented semiconductor models, which are either behavioral or physics based, deal only with specific kinds of devices and involve various assumptions. By comparison, the distributed regional model deals with any power device and guarantees the compatibility of various semiconductor models in terms of physical concepts, validity domain, accuracy, homogeneity of parameter identification procedures, and similarity of implementation in the simulator. It is based on a 1D regional partition of device structures coupled with a corresponding organization in submodels of the simulator semiconductor device library. In effect, it eliminates the one-device, one-model approach for bipolar device circuit simulation. Instead it uses a regional view to modeling with a new partition of the model library. This new partition is comprised of an adaptable assembly of a limited number of submodels associated with well-identified regions of semiconductor structures. In other words, the library will only contain the primitive building blocks of the power device models. When these building blocks are linked together the user can obtain an homogeneous set of power semiconductor device models.

Programmable Chip With CPLD, EPROM And SRAM Adds System Supervisory Features

Now that system supervisory functions have been added to the PSD7XX series of programmable system devices, these chips can set the desired power-on reset voltage, program the desired reset pulse width, provide a system watchdog timer, and detect power failures to switch in battery backups. In addition to the supervisory functions, the PSD7XX family includes a 2500-gate CPLD, up to 128 kbytes of EPROM, 512 bytes of battery-backed SRAM, and 27 configurable I/O lines. An on-chip programmable interface allows these devices to tie into microcontrollers from Intel, Motorola, Philips, Siemens, and others.



The out-of-tolerance voltage detector on the chips can be programmed to either of two trip points (4.75 or 4.5 V). The trip point also can be driven from an external source (2.5 to 5 V). As soon as the voltage falls below the programmed trip point, the PSD7XX automatically disables any internal and external SRAM, as well as its own I/O lines. The detector can cause the circuit to switch to standby operation from an alternative power source. When the voltage level returns to normal, the PSD7XX can restart where it left off with the same data in SRAM. A debouncing filter guards against false resets that might result from noise.

Ensuring the PSDs don't get caught in endless loops, the watchdog timer can be programmed to count from 1 µs to several seconds, using an internal 2 kHz clock or an external clock. If not continually initialized, it will cause a system reset when it reaches the terminal count. This will break the system out of an undesirable condition.

A programmable power-on reset allows the system to clear any inappropriate condition that the PSD7XX may have gotten itself into during power-on. Different system chips require different pulse widths, the longest of which must be accommodated during the power-on reset stage. Thus, pulse widths can be programmed to any value ranging from 8 ms to 1 second, based on either the internal 2-kHz oscillator or an external clock signal. The power-on-reset signal level also can be programmed to either of two predefined levels or set to any value by using an external voltage reference.

The internal logic and memory resources on the PSD7XX devices are similar to the resources included on previous PSD families—2500 gates of programmable logic optimized for use with microcontrollers. The logic includes direct bus connections between the logic flip-flops and the microcontroller, which streamlines the interface and saves many logic gates. The 27 I/O lines are fully programmable and can serve as inputs, outputs, or bidirectional signal lines. On-chip EPROM comes in three options—32-, 64-, or 128-kbytes; on-chip SRAM is 512 bytes for all chips

A simple set of Windows-based software tools is provided so that designers can manipulate the features. A decompiler included in the toolset allows previous PSD designs to be uploaded, decompiled, and modified. The PSDSoft tools automatically and transparently optimize logic so that the flip-flop configuration and product-term allocation result in the most efficient use of the silicon.

Samples of the PSD7XX devices are available immediately and sell for as little at $6.67 each (the PSD711S1-15J) in lots of 10,000 units. The chips are housed in 52-lead ceramic and plastic chip carrier packages. The PSDSoft tool suite sells for $495., and a version that includes the PSDSilos Verilog simulator sells for $1295. Users that already have the basic PSDSoft tool can purchase the PSDSilos software for $995.

WSI Inc.
47280 Kato Rd.
Fremont, CA 94538
David Raun, (510) 656-5400
http://www.wsipsd.com
CIRCLE 509
DAVE BURSKY

Single-Chip CCD Image Processors Optimized For 3-V Operation Feature Wide Gain Range

The XRD4460 and XRD44L60 (optimized for a 3-V rail) are single-chip processors for analog image paths from charge-coupled devices (CCDs). They're targeted at the video and imaging markets, and applications in digital video, digital still cameras, color copiers, and scanners. Using a single-chip analog front end reduces the size and weight for high-performance portable products. The ICs use a 10-bit architecture for matching to any existing digital video system, and the CMOS fabrication provides good overall control of power consumption.

The ICs contain a correlated double sampling (CDS) input, which has become the method of choice for most companies in reducing errors in the black areas of the CCD signals. The output passes through a large-range (32 dB) programmable gain amplifier (PGA) into the 10-bit low-power ADC. The digital output also is used in a feedback loop to control offset automati-

(continued on page 62)

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cally. The PGA and offset codes are controlled through a simple serial interface. An on-board timing generator for the sample-and-hold and conversion requirements is driven from off-board clamp, clock, and shading signals.

The inputs to the integrated circuits can be either single-ended or differential while the sampling rate is up to 15 MHz. At that speed and with tristate outputs, the 5-V IC dissipates 250 mW, while the 3-V version dissipates 150 mW. In the power-down mode, the dissipation drops to a typical 1 mW. Exar indicated that this is the first in a family of imaging products. Its goal is to further integrate horizontally and vertically, and follow a road map that takes advantage of future developments in speeds and resolution in conversion technology.

The XRD4460 is fabricated in CMOS and is packaged in a 48-pin TQFP. Available now, the IC is priced at $5.95 in 1000 unit quantities.

Exar Corp.
48720 Kato Rd.
Fremont, CA 94538
(510) 668-7000
fax (510) 668-7017
CIRCLE 510
PAUL McGOLDRICK

Programming Language Simplifies The Use Of ISP-Capable PLDs

A new programming language dubbed Jam promises to simplify the in-system programming (ISP) of many programmable logic devices that are ISP-capable. Developed by Altera, the Jam language will be offered to companies with no license fee. The company also has proposed the language to the Joint Electronic Devices Engineering Council as an industry standard. Because it addresses many programming issues for multi-manufacturer ISP-capable devices through the chips' four-pin JTAG test ports, the vendor-independent Jam standard will result in smaller programming file sizes and shorter programming times.

A consortium of companies consisting of PLD suppliers, programming tool manufacturers, and test systems manufacturers is backing the Jam proposal. By using Jam, designers can eliminate the confusion of multiple proprietary file formats, vendor-specific algorithms, large file sizes, and long programming times. The Jam language is optimized for programming devices through the IEEE 1149.1 TAP controller that's part of JTAG standard, and allows the specification of both the programming data and the programming algorithm in one file. Once created, the file contains all of the information required to program a specific design across multiple PLDs connected in a JTAG daisy chain.

Two software components comprise the Jam programming solution—the Jam Composer and the Jam Player. The composer creates the Jam file required to program a specific design into a specific device, while the Player interprets the Jam file and programs the target device. The Composer typically resides on the development tools that accept the configuration pattern developed by the PLD logic design tools. The Player can either reside in the PLD tools or locally on the board containing the PLDs to be configured.

Included in the Jam language are constructs such as For-Next loops and other commands that make it code-efficient. A fully expanded file to program a 128-macrocell PLD typically exceeds 20 Mbytes, while the equivalent file would require only about 8 kbytes when created with Jam. Moreover because the Jam Composer includes chip-specific programming algorithms, each PLD can be programmed with the optimum pulse width. This minimizes the programming time required for each device and often reduces the system programming time by a factor of ten or more.

The initial version of the Jam Composer supports flash-based PLDs; additional enhancements will be forthcoming to support RAM-based FPGAs, EEPROM, and flash-memory chips and MCUs that have on-chip programmable storage. Initial versions of the Composer will support PLDs from Altera and Cypress Semiconductor, programming tool suppliers such as BP Microsystems and Data I/O, and test-systems companies such as Teradyne, GenRad, Asset InterTech, Gopel, and JTAG Technologies B.V.

Copies of the Jam language specification and the Jam Composer/Player as well as sample files can be downloaded from the Altera Website at *http://www.altera.com*. A developers kit that contains a PC-compatible CD ROM, a programming cable, and some documentation also can be ordered through the website.

Altera Corp.
2610 Orchard Pkwy.
San Jose, CA 95134-2020
Craig Lytle, (408) 894-7000
CIRCLE 511
DAVE BURSKY

Code-Efficient 21-MIPS/20-MHz RISC CPU Mixes 16-Bit And 32-Bit Commands

The first silicon to implement the MIPS-16 instruction set, which comprises the R1900 processor core and the TMP1904AF processor, can operate at a clock speed of 20 MHz and deliver a throughput of about 21 MIPS. The processors have two instruction set modes, one that executes full 32-bit commands and another that executes the new space-efficient 16-bit commands (some of which are actually 32-bits long, i.e., Jump/Link and Extend operations). Although the MIPS-16 instruction set architecture does define several 64-bit data-processing instructions, they're not implemented on the initial versions of the R1900.

Each command set contains less than 100 instructions (85 for the 32-bit
(continued on page 63)

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set and 52 for the 16-bit set) and most execute in a single cycle. The 32-bit instructions are upwards-compatible with the commands of the R3900 microprocessor and the R3000A, except for some coprocessor and translation lookaside buffer instructions. A five-level pipeline—instruction fetch, decode, execute, memory access, and register write—is employed to exe-[c]ute the commands, which gives the [app]earance of executing one command [ev]ery clock cycle. Only the 32-bit ex[ten]sions to the 16-bit commands re[qui]re two clocks to execute.

The CPU core includes 4-kbytes of [ins]truction cache and 1-kbyte of data [ca]che, both two-way set associative, and 1 kbyte of high-speed data RAM. Surrounding the core to form the TMP1904F is a DRAM controller that handles four banks of either fast-page-mode or extended-data-out DRAM; a ROM controller that supports ROM, EPROM, EEPROM, flash, and SRAM; a DMA controller that provides two independent channels; and an interrupt controller that handles eight internal sources and six external sources. Additional functions include a three-channel 24-bit upcounter, a watchdog timer, a dual-channel UART for serial communications, and three parallel I/O ports.

Internally, the chip's memory (IM) and processor data (G) buses operate at 20 MHz, while the IM bus clock can be slowed to 1/2, 1/3, or 1/4 the speed of the G bus clock. The IM bus also features a bus-sizing capability that allows it to communicate with 8-, 16-, or 32-bit peripherals.

The chip was designed for low-power operation, and can run from a 3.3-V power supply while consuming less than 15 mA when running at 20 MHz. Due to its low power, the chip can be housed in an inexpensive 160-lead PQFP. In 10,000-unit lots, the TMP1904AF sells for just $17.50 each. Samples are available immediately. The design files for the core are available through the company's ASIC design library.

Toshiba America Electronic Components Inc.
1060 Rincon Circle
San Jose, CA 95131
Mark Meisberger, (714) 455-2200
http://www.toshiba.com/taec
CIRCLE 512
DAVE BURSKY

Features Reduced To 0.3 µm Boost Performance And Lower Cost Of FPGAs

A process shrink to features of just 0.3-µm for the ORCA OR2TxxA family of SRAM-based field-programmable gate arrays gives designers eight members that range in density from 4000 to 40,000 usable logic-only gates (with up to 100,000 equivalent gates possible when using [on]-chip RAM blocks). The chips will [off]er improved performance, with [spe]ed grades ranging from a –2 to a –[6]. The higher-speed versions permits [fun]ctions such as a 128-word by 17-bit [FIF]O register to run at internal [spe]eds of 50 MHz. That's fast enough [to h]andle the speed requirements of [the] Utopia II interface in ATM sys[tem]s. Lookup table speeds will improve by almost 50%, while external clock-to-output delays will improve by about 20%.

Thanks to the smaller features and an advanced bond-pad pitch of just 3.2 mils, the chips will shrink by about 19%, which is considerably smaller than those in the original 0.35-µm 2T family. As a result, cost is reduced. The chips will be able to support 5-V tolerant interfaces by using 5-V tolerant I/Os. The architecture supports synchronous and dual-port RAM blocks for telecommunications and data-communications applications, and a 4-bit-by-1-bit multiplier in each logic block for many advanced signal-processing applications.

The first chip to be sampled will the OR2T15A-6, which will pack about 15 kgates. Samples are immediately available, with production slated for the fourth quarter of this year. An even higher-performance process, employing 0.25-µm features, will be used for the higher-density parts. These parts will be sampled in the late fourth quarter. In a 208-lead shrink, quad-sided flat package, the OR2T15A–3 sells for $49.80 each in lots of 10,000 units, while the –6 speed version sells for $99.30 in similar quantities. The new 0.3-µm devices will be supported by standard CAD tools, and by Lucent's ORCA Foundry software, Version 9.15.

Lucent Technologies Inc.
555 Union Blvd.
Room 30L-15P
Allentown, PA 18103
(800) 372-2447
http://www.lucent.com/micro/fpga
CIRCLE 513
DAVE BURSKY

Low-Density High-I/O-Line FPGA Fills Family Need Using Just 3 Kgates

To fill in the the low-density side of pASIC 2 family of FPGAs, designers at QuickLogic came up with the QL2003. It contains about 3000 usable gates and a high I/O line count—118 pins—in comparison to [mo]st other programmable chips of comparable complexity. Very little power is consumed when on standby—only about 1% of the power required by complex PLDs that pack about 7500 gates.

Thanks to the one-time programmable antifuse technology employed by the pASIC 2 family, the logic can be implemented on very small chips. As a result, the QL2003 becomes an inexpensive solution. The 144-lead version of the QL2003 sells for about $17.75 in quantities of 100 pieces. Large volume prices can go as low as $9.65 apiece. Internal logic implemented on the QL2003 can operate fast, thanks in part to the triple-metal 0.35-µm process used to fabri-
(continued on page 64)

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cate the FPGA. For example, 16-bit counters can run at a rate of 200 MHz; an 8-bit accumulator can operate at 70 MHz; a sum-of-products state machine can clock at 150 MHz; and a simple datapath can operate at 250 MHz.

Like other members in the pASIC family, the on-chip logic cells can be configured as either a wide-input cell for high speed, or as up to five smaller cell fragments for greater utilization. That allows the development tools to perform 100% automatic placement and routing, which enables users of HDL to stay at the high level and concentrate on generating an optimal logic flow. A JTAG test port also is available on the chip that allows for in-system functional testing.

The company's QuickWorks design software, which is priced at $2995, supports all QL devices for both schematic- and HDL-based designs. The QuickTools package provides design support on Unix- or Windows-based platforms. Versions of the QL2003 are available in either 5-V or 3.3-V options; the 5-V versions also operate at 33 MHz to provide PCI compliant I/O signals if needed.

QuickLogic Corp.
1277 Orleans Dr.
Sunnyvale, CA 94089-1138
Ed Smith, (408) 990-4000
http://www.quicklogic.com
CIRCLE 514
DAVE BURSKY

Intelligent Display Controller Works With AMLCD VGA And XGA Flat Panels

Panel vendors along with system OEMs will reap the benefits of an intelligent panel controller, the SiI201. The programmable part, developed by Silicon Image Inc., supports multiple panel-timing configurations for active-matrix LCD Super VGA (800 by 600 pixels) and XGA 1024 by 768 pixels) resolutions. Combining the chip with the company's patented PanelLink technology results in reduced time-to-market, lower power consumption, lower overall system costs, and the flexibility to add some new features in the future.

By incorporating the SiI201 into a design, the system maker can eliminate a panel-controller ASIC that typically carries a high pin count. This part would be used to control such functions as row and column timing. The SiI201 is compatible with VESA's Plug and Display (P&D) specification. This means that it supports an automatic power-down mode within the panels to allow for hot-plugging.

The SiI201's programmability gives OEMs the flexibility to differentiate their products. With automatic configuration of timing and control signals, the part works with most popular column drivers. Programmable registers are employed to set the timing values that optimize row-select timing pulses, resulting in a high-quality display output. The part also can be programmed to mirror pixel data for support of flat-panel displays that are used as overhead projectors. In addition to the display enable, the IC can handle up to two control signals for customized features. And designers can choose whether to employ normal or inverted clock outputs.

Using the SiI201, data can be sent to the column driver in one of three methods. It can send one pixel per clock for 18 or 24 bits/pixel; two pixels per clock, halving the clock frequency for 36 or 48 bits per clock cycle; or, using a dual-edge clock, data can be sent on the clock's rising and falling edges.

The use of the PanelLink technology ensures that the chip will support most flat-panel displays. It defines a single interface that spans VGA to HDTV resolutions and supports active and passive LCDs as well as plasma displays. PanelLink uses transitional minimized differential signaling (TDMS) over a scalable architecture, and permits additional control signals without the need for separate control lines. With its dc balancing, data can be transmitted over several meters using standard copper twisted-pair cable, or over several hundred meters using fiber optics.

The SiI201 programmable intelligent flat-panel controller is available now in large quantities. Housed in a 100-pin TQFP, it sells for $9 each in lots of 10,000.

A second offering from Silicon Image is a chip set that enables reliable, scalable high-speed data transmission for flat-panel displays. The chip set consists of a transmitter and a receiver, the SiI140 and SiI141. The SiI140, acting at the transmitter, is embedded into the host system, while the receiving SiI141 is designed directly into the panel.

Silicon Image Inc.
10131 Bubb Rd., Cupertino, CA 95014; (408) 873-3111; Internet: http://www.siimage.com.
CIRCLE 515
RICHARD NASS

Chip Bridges From UltraSCSI To Ultra2 SCSI

Backward compatibility between UltraSCSI and Ultra2 SCSI is available using the AIC-3860 multipurpose chip. A second feature of the part is that it extends the cable length normally associated with the UltraSCSI specification. Cables of up to 25 m can be used between the host system and the peripherals. This is critical for applications that address large, com[illegible] configurations, such as cluste[illegible] servers, where various periphe[illegible] are shared by multiple servers.

The device functions as a sin[illegible] ended SCSI to low-voltage differe[illegible] (LVD) transceivers. By combining [illegible] chip with an Ultra2 SCSI contro[illegible] designers can employ today's Ul[illegible] SCSI drives and future Ultra2 S[illegible] units on the same bus without affe[illegible]ing performance. Ultra2 SCSI drives are expected to ship in the early part next of year. Without the AIC-3860, combing the two flavors of SCSI would default the entire system down to the slower speed and also shorten the allowable cable length. Available immediately, the AIC-3860 multi-purpose chip sells for about $15, depending on volume. RN

***Adaptec Inc.**, 691 S. Milpitas Blvd., Milpitas, CA 95035; (408) 945-8600; Internet: http://www.adaptec.co[illegible]*
CIRCLE 516

ELECTRONIC DESIGN QUICK LOOK

■ Edited by Mike Sciannamea and Debra Schiff

MARKET FACTS

Showing Up For Displays

With all the new flat-panel displays making large showings on the trade circuit, the question floating around the floor is "What about cathode ray tubes?" The answer, according to "Cathode Ray Tubes 97," by Stanford Resources, is that they're going strong and expected to remain that way through the turn of the century. The most recent edition of the report looks at all aspects of the global cathode ray tube (CRT) market. The report asserts that despite the market flocking to flat-panel displays, the CRT market will remain the largest global electronic display industry segment, when it comes to value, through 2003. According to Stanford Resources, the main pull of CRT technology continues to be its consistently improving price/performance ratio. The report focuses on competitive display markets, manufacturer profiles, manufacturing cost forecasts, success strategies, and technology trends. And, for those with a taste for numbers, included is a worldwide CRT Display Market Database that covers the market from 1995 through 2003. The database breaks down the market into total value in millions of dollars, total quantity of shipments sold, and the average selling price of a CRT. Six general display application sections (business/commercial and computer, communication, consumer, industrial, and transportation) each have their own subcategories that are examined as well. Specifically, the report sees the worldwide CRT market for computer applications growing from $11 billion this year to $13 billion in 2003. In the consumer arena, the market is expected to grow from 175 million units in 1997 to 224 million units in 2003. The average selling price per unit for the worldwide CRT market is expected to stay at $101 for the next five years.

Worldwide CRT Market

Source: Stanford Resources

Art: James Miller

Contact Stanford Resources, 3150 Almaden Expwy., #225, San Jose, CA 95118; (408) 448-4440; fax (408) 448-4445; Internet: http://www.stanfordresources.com.—**DS**

XTRA

With this summer's release of *Contact*, there's been a renewed interest in SETI (Search for Extra-Terrestrial Intelligence). Tipped off by a recent e-mail from Richard Factor, the founder and president of the SETI League, I checked out their site *http://www.setileague.org*. It's an interesting site that really explains everything from radio astronomy to Project Argus (about 5000 small radiotelescopes from around the world monitoring the sky).

The SETI League, according to their web site, "is a worldwide group of amateur and professional radio astronomers, radio amateurs, microwave experimenters, and digital signal processing enthusiasts who have banded together in a systematic, scientific search of the heavens to detect evidence of intelligent, extra-terrestrial life."

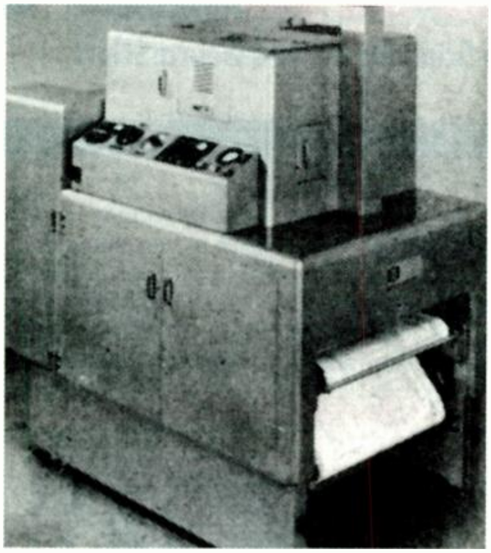
In 1993, Congress cut all NASA funding to SETI, which previously ate up about one-tenth of 1% of NASA's budget. This action prompted Factor to found the nonprofit scientific organization in 1994.

Though not associated with the League, SETI@home also is worth a glance or two (*http://www.bigscience.com/setiathome.html*). Visitors to the site can download a block of cosmic-noise-pattern data and software that allows their computer to analyze the data in the background. And what's really cool is that the program acts as a screen saver, allowing the viewer to monitor the progress of the project.

If you'd like further information on this organization, contact The SETI League Inc., P. O. Box 555, Little Ferry, NJ 07643; (201) 641-1770; fax (201) 641-1771; e-mail: info@setileague.org.—**DS**

40 YEARS AGO IN ELECTRONIC DESIGN

Xerographic Printer Prints Drawings From Microfilm



A low-cost method of producing enlarged engineering drawings from microfilm is done in a XeroX Copyflo 24-in. continuous printer, an automatic device that reproduces drawings up to two ft. wide at a speed of 20 fpm. The time for processing of any one frame is only a few seconds. No ink is issued. The prints are dry on emergence and may be used immediately. The printing process is completely automatic.

Individual microfilm frames are mounted in die cut apertures of cards punch-coded for various sorting purposes, and emerge from the printer in the order of entry. Up to 400 prints of a single frame may be had via a push button that repeats the exposure. A miss detector is built into the film head and will stop the card-feed mechanism if a card fails to appear. Another function of the detector is to stop the machine when the card stock is exhausted. The Haloid Co., Dept. ED, 2-20 Haloid St., Rochester 3, N.Y. *(Electronic Design, Sept. 15, p. 129)*

This printer is the humble beginning of Xerox as we know it. The word comes from "xerography," a word coined by a professor from Ohio State University, derived from the Greek words for "dry" and "writing." The Haloid Company then registered the trademark "Xerox" for its new line of copiers. It would be another year before "Xerox" would become part of the company name, when The Haloid Company became Haloid Xerox. Another name change occurred in 1961, when the company settled on Xerox Corporation, shortly after it had introduced the first automatic office copier to use ordinary paper, the Xerox 914.—**SS**

High-Frequency Negative Resistance Device, Patent No. 2,794,917, W. Shockley (Assigned to Bell Telephone Labs., Inc.)

The diode oscillator uses a semiconductive material having a first zone containing a predominance of mobile charge carriers of one type and a second zone which is characteristically essentially free of mobile charge carriers of this one type. A barrier exists between the zones. An injector of minority charge carriers of the one type is associated with the second zone. An electrode is connected to the first zone, and a voltage bias is provided between the injector and the electrode which biases the junction in its high resistance direction. An impedance having a reactive component in series resonance with the reactance of the semiconductive material at a frequency—the period of which falls between two-thirds and twice the effective transit time of the one type of charge carrier—is provided between the injector and the carrier. *(Electronic Design, Sept. 15, 1957, p. 161)*

As noted in the Aug. 4, 1997 issue, by this time in 1957, William Shockley had already left Bell Laboratories and was heading up Shockley Semiconductor Laboratories in the nascent Silicon Valley. Judging from the September announcement of a new patent being granted there was a significant lag time between the filing and the issuing of patents.—**SS**

EYE ON ISO 9000

Instead of the list of companies that have received ISO 9000 certification that you normally see under this column heading, we'd like to feature a product that could help your company get a mention in this space in the near future.

Chek-MATE 9000 is a software solution from I^{n}Technology Corporation designed to help organizations manage ISO 9000 compliance, audit requirements, and corrective action requests. The customizable software reduces the time and cost of audit and corrective action management, and helps to foster better communication between departments in an organization.

Check-MATE 9000 maintains current ISO 9000 criteria on line. Its manual and complete ISO 9000 glossary are available to users at any time they wish to access them.

The software lowers the costs of ISO 9000 audit activities by decreasing the time needed to conduct and compile internal audit reports. Chek-MATE 9000's closed-loop reporting capabilities merge all of the audit reports into a single report for management review.

A data-entry window automatically formats the appropriate form or report, which can include nonconformance summaries, detailed summaries, and follow-up audit reports.

Chek-MATE 9000 is part of I^{n}-Technology's PERFORMSuite '97 business improvement package, a solution for implementing, tracking, and reporting improvement activities throughout an organization. PERFORMSuite also includes BaSE '97 for Malcolm Baldrige business assessments and Proper for managing improvement initiatives.

Available for Windows 3.1, 95, and Macintosh operating environments, Chek-MATE 9000 is priced at $594 for a single-user license, including 12 months of unlimited technical support and upgrades. Multiple-purchase discounts, network prices, and site license prices also are available.

Contact I^{n}Technology Corporation, 4575 Hilton Pkwy., Colorado Springs, CO 80907; (719) 531-9680; fax (719) 531-5702; Internet: http://www.intechnology.com.—**MS**

Making digital audio sound a bit better!

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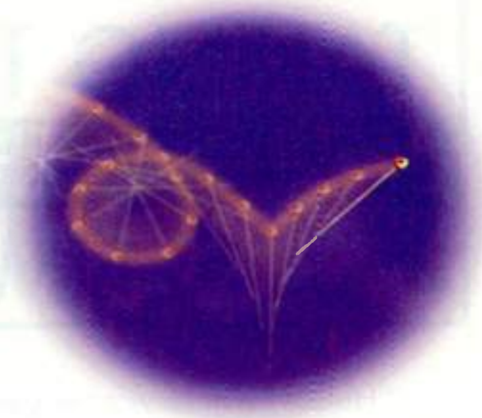
HIGH DYNAMIC
SOUND



Gaining 6dB in Signal-to-Noise performance is easy with AKM's 105dB+ ADCs and DACs. Doubling the sampling frequency is a snap with a range of 96kHz, 20- and 24-bit devices. Getting -6dB in price may even be possible, too – AKM's volume manufacturing capability allows standard pricing that sounds great!

Our full range of audio ADCs, DACs and Codecs covers your total circuit requirements – whether you need maximum performance, the highest level of integration, or the highest performance at a given cost level.

AKM's High Dynamic Sound converters – called HiDS™ – provide remarkable dynamic range and distortion-free audio performance. The innovative designs include our new proprietary dual-bit delta-sigma architectures. Wherever you see the HiDS logo, you are assured of the highest audio performance and quality.

Keep your eyes – and ears – on AKM! With our aggressive new product schedule, enormous capacity in a world-class fab, and a growing portfolio of audio patents, AKM is the leader to trust both today and tomorrow.

*For more information, including a free copy of our new **Product Selection Guide** or **Multimedia Audio Data Book**, call us at 1-888-AKM-SEMI (1-888-256-7364) – or visit our website at **http://www.akm.com**.*

*If you plan to be at the 103rd AES Convention in New York in September, please stop by the **AKM booth #1087**. You'll like what you hear!*

AKM Digital Audio IC Sampler

	Bits	Channels ADC	Channels DAC	Comments
AK4324	24	–	2	105dB, 96Hz, 24-bit DAC
AK4520A	20	2	2	Highest performance integrated codec
AK4526	20	2	6	Ideal codec for AC-3 requirements
AK4540	16	2	2	AC'97 Compliant Codec for PC applications
AK5392	24	2	–	115dB 24-bit ADC
AK7712A	20	2	4	Integrated codec with fully programmable on-chip DSP

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Japan: Asahi Kasei Microsystems Co., Ltd.
TS Building, 24-10, Yoyogi 1-chome
Shibuya-ku, Tokyo 151
Phone +81-3-3320-2062 • Fax +81-3-3320-2072

Europe: Asahi Kasei Microsystems Co., Ltd.
22 The Courtyards, Hatters Lane, Croxley Business Park
Watford Herts WD1 8YH, United Kingdom
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READER SERVICE 128

FOR ALL THE ENGINEERS WHO TAKING TIME OFF THIS YEAR, YOU WITH A MUCH DESERVED FROM LIMITATIONS.

"Holiday" is not a word in your vocabulary these days. You've got more important things to think about—like changing the way people live and work.

With something this important on your shoulders, you don't need bits and pieces of solutions. You need a whole product for your embedded designs. You need the total system solution NEC's V_R Series™ MIPS® RISC processors provide.

You get it all. 64-bit technology that speeds data throughput and meets high bandwidth design requirements. A high level of on-chip integration and PCI Bus companion chipsets. And a broad range of development and debug tools to get you to market faster, including RTOS, compilers, simulation tools, evaluation boards and reference designs.

And you get something else that's just as powerful as our products: our commitment. We offer a comprehensive long-term roadmap - a scalable architecture with a solid future. So no matter if your designing low-power smart phones, protocol converters, gaming machines, set-top boxes, DVD or any other office, networking or consumer application, NEC gives you the price/performance and advanced, high-capacity, high-quality processors and manufacturing expertise you need.

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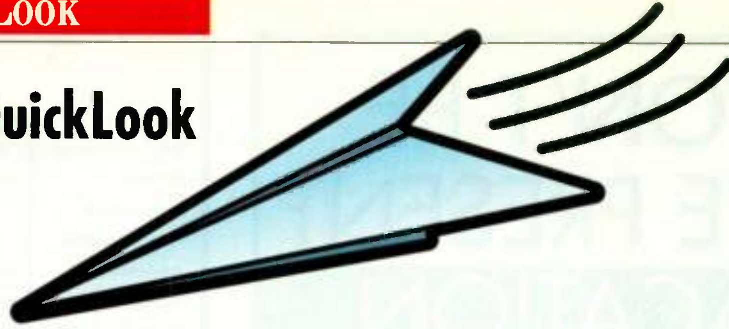
Because even though you can't take a trip around the world right now, the V_R Series can surely help you design a product that can change it for the better.

See us at Embedded Systems Conference West

Booth #528

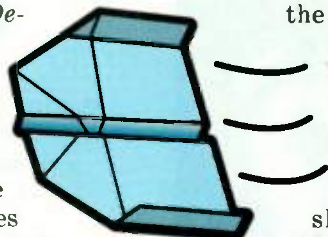
V_R SERIES PROCESSORS

Enter The First Annual QuickLook Paper Airplane Contest



As is the case with most things in life, there's a story behind this one. In the middle of July, I began to think about paper airplanes. Then, I thought about engineers. By nature, according to our Communications/Networking editor Lee Goldberg, engineers are problem solvers. Throw a wrench into the works, and they'll be the first to dive in after it.

So, here I am in Cubicle Land wondering how I can tie paper airplanes to *Electronic Design*. Of course, I asked around.



Lee, a licensed private pilot, was very excited about the idea of having a paper airplane contest. He also deserves the credit for fleshing out the tie. What he said was, "How about, 'how many electronics can you fit onto a paper airplane and still make it fly?'"

An Idea Takes Flight

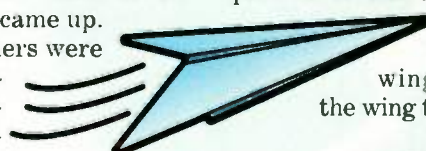
Then we brainstormed about all kinds of possibilities. Did we want to judge the submissions on guidance and control, length of flight, weight, or size? Well, the brainstorming led us in the direction of another of our resident pilots, Test and Measurement editor John Novellino. He offered the following guidelines:

- The airplane must be fashioned from paper. No balsa wood planes, no thin plastics, and no metal sheeting.
- Glue and paperclips are acceptable, but use common sense. If the plane's going to be weighed down by stuff other than electronics, your possibilities for showing off your creativity will be greatly limited.
- The plane must be fully assembled when it reaches the offices of *Electronic Design*. None of us is interested in taking the fall for your plane not working because we didn't put it together properly.
- The plane cannot have a wingspan larger than 3 ft. If I can't carry the thing, it's not going to participate in the contest.
- Just for those who think like Bob Pease (who defined himself as "thinking like a cheater,") a paper airplane with electronics is NOT a piece of paper crumpled around a transistor radio. That's just not going to fly here.

A Word From Our Sponsor

In the middle of our discussions, in the middle of the hallway, PIPS editor Patrick Mannion and Boards and Buses editor Rich Nass began offering their opinions. They stressed that we should have stringent guidelines, while I argued that what I really wanted to see from our readers was creativity.

"How cool would it be," I said, "if some design engineer came up with a paper airplane that would fly itself, right out of the box?" Then the discussion of motors came up. Some were for, others were against, but in order to keep creativity from being stifled, we decided to allow motors in the contest.



So, how are our contest participants going to power these motors, or any other electronics on their planes, for that matter? Lee suggested that we hit up battery companies for their support in the contest.

1-800-Batteries

Of the battery companies, 1-800-BATTERIES came forward to sponsor the contest.

The company has agreed to furnish lithium batteries to the first 100 contest entrants. They also put up the prizes. First place is a $150 gift certificate and second place is a $50 gift certificate, both to be used for purchases made through the 1-800-BATTERIES catalog.

Hi. I'm An Engineer. Fly Me.

When John and I spoke about the guidelines, he stressed that the submissions really ought to display some elements of flight. So, the public library of River Edge, N.J. supplied us with *Paper Airplanes*, by Nick Robinson (Quintet, 1991).

Just a quick lesson: "...the amount of resistance is related to how fast the object is moving throught the air..." Drag is the combination of resistance and turbulence, both of which are the result of a bulky design encountering the air. Thrust, in real airplanes, is usually supplied by huge engines and propellers. In our case, most of these planes will get their thrust from our editors throwing them forward. According to *Paper Airplanes*, "lift is the force that acts on the wing to move it upwards and hence to keep a plane in the air. It is caused by having a greater air pressure under the wing than above it, so the wing tends to rise."

How To Enter

The first 100 entrants to send a self-addressed stamped envelope to QuickLook, *Electronic Design*, 611 Route 46 West, Hasbrouck Heights, NJ 07604 will receive one lithium battery from 1-800-BATTERIES.

All participants must submit a photo of the plane (in addition to the plane itself), their names, occupations, company names, and a short explanation of their designs with each paper airplane. What we're looking for here is creativity. The more ingenious your design, the better you'll do. Our editors here will perform the judging. None of the planes will be returned, so bear that in mind when you ship them off to N.J.

All paper airplanes should be received by January 1, 1998. Any questions about the contest should be e-mailed to: debras@csnet.net or faxed to Deb Schiff (201) 393-6242. Good luck!—DS

1394.

August 1995
Sony releases the 1394 camcorder with TI silicon

December 1995
TI is instrumental in the first IEEE specification

July 1996
Another first: TI's software team develops the LYNXSOFT Software V1.0

April 1994
After receiving the "Most Significant Technology" award at Fall COMDEX '93 for its 1394 serial bus, TI releases the first PHY and LINK silicon to market

November 1995
TI forms the first 1394 software development team

June 1996
TI ships the first and only backplane PHY and also introduces a broad range of designer kits

21-5131

M I X E D S I G N A L

SINCE 1994.

In 1994, Texas Instruments became the first supplier to release a complete 1394 silicon solution. And our lead over the competition increases every day through our growing portfolio of IEEE 1394 products and software. So TI customers are first to market with built-in 1394 solutions, putting them far ahead of the competition. And to keep our customers first in line, we continue to set new precedents every day. So when you need 1394 solutions, make TI your first, and only, stop. TI, the leader in 1394 solutions.

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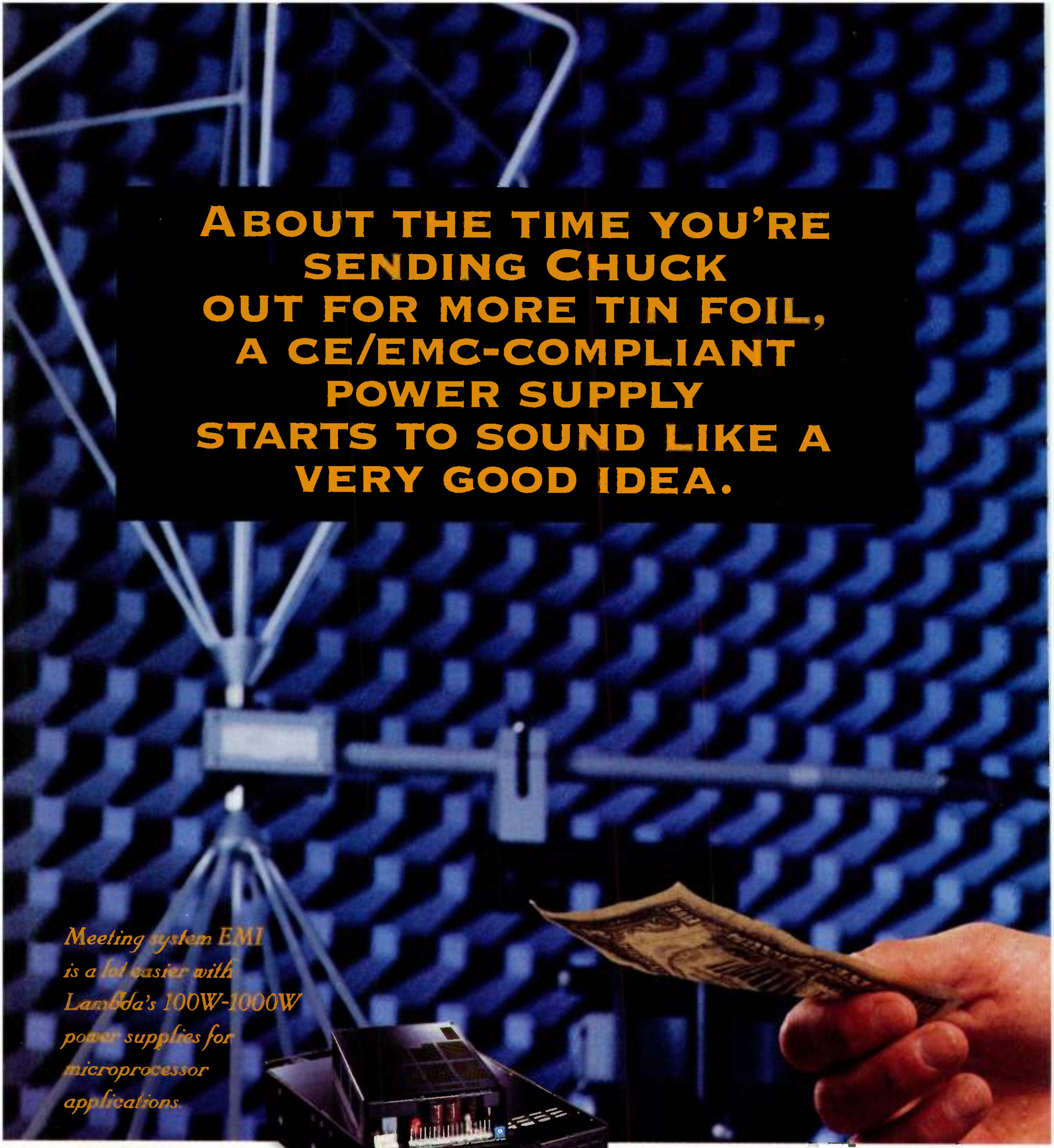
& ANALOG

TEXAS INSTRUMENTS

About the time you're sending Chuck out for more tin foil, a CE/EMC-compliant power supply starts to sound like a very good idea.



Getting your system to meet EMI standards can be an arduous task if your power supply comes from a company that considers it to be your problem, not theirs.

But at Lambda we supply solutions, not just power. Our 100W-1000W PFC power supplies for microprocessor-based applications already meet CE standards for both conducted and radiated EMI. We have our own in-house EMC and lightning strike measurement facilities, so we know these supplies can stand the test of worldwide regulations, as well as the test of nature.

Our new RP series addresses your logic needs with 500, 750 and 1000 watt models featuring

3.3 or 5 volt auxiliary outputs, and main outputs that adjust from 3 to 5.75 volts. There are plenty of output configurations and remote signal options available, so you'll find one that fits your application without time-consuming re-design or modification.

To bring your products to CE compliance you don't need foil, ferrite chokes, and EMI gaskets — you just need to give us a call at 1-800-LAMBDA-4, ext. 8823.

LAMBDA www.lambdapower.com/rp

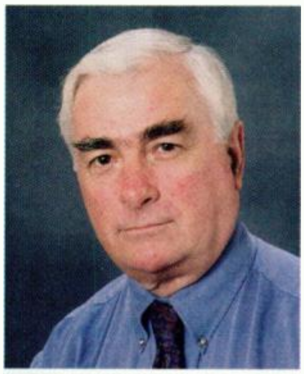
READER SERVICE 177

LETTERS FROM LONDON

The Really Personal Computer Has Arrived

When the term "Personal Computer" was coined in the late 1970s, it was used simply to define a computer intended for the use of one person at a time. Depending on the environment in which it was used, it may have been reserved exclusively for the use of one person in particular who may have adapted its software content and appearance to suit his or her own personal tastes.

Two computers I've used this summer, however, are of a breed that takes the "personal" aspect through to the ultimate meaning of the word. Both are truly pocket-sized—meaning that I could keep them about my person at all times. They also are personal in the sense that I'd trust them with information that I need to have at all times. But more than that, they are personal in the sense that the choice of which I like best is almost totally subjective and as personal to me as the wristwatch I wear.



PETER FLETCHER
FIELD CORRESPONDENT

The two computers are the Series 5 made by Psion plc., London, and the Velo 1 made by Philips Electronics B.V, Eindhoven, The Netherlands. Technically, the two machines are similar. Their physical dimensions are almost the same—about 6.5 by 3.5 by 1 in. Both have 32-bit RISC processors—ARM for the Psion, MIPS for the Velo. Both have high-resolution, backlit LCD screens of about the same size and quality. Both have several megabytes of memory—8 Mbytes for the Psion, 4 Mbytes for the Velo. Both use multitasking software—Psion's own EPOC 32 system for the Series 5, and Microsoft's Windows CE on the Velo. Both offer sophisticated word processing, spreadsheet, communications, diary, and contact programs. And both can be easily integrated with a desktop computer by either a physical serial wire or infrared link.

Reading the data sheets, they could almost be twins. But, they are not the only two. Other manufacturers will soon be launching similar products, including Hewlett-Packard, Compaq, Casio, and Microsoft. Psion also has been signing up licensees for its EPOC operating system.

Given that these computers basically have the same functionality, the choice between them comes down to a matter of personal taste. In the end, my choice was the Psion, because for the first time in a computer that small, I've found a keyboard on which I can really type. Since I write for a living, that's important to me. My son, a computer programmer, preferred the Velo because he liked the familiar feel of the Microsoft software and its similarity to what he usually uses. Although, he liked the Psion's built-in OPL object-oriented programming language.

I had intended to write a classic review of each of these machines. In particular, I wanted to work out which might be better for a design engineer. I suppose the Psion's programming language might tip it marginally, if you want to write data-acquisition software or add hardware to turn it into a pocket oscilloscope. However, talking to other people and finding that some liked the things I didn't and vice versa, I concluded that if I wanted to be fair and objective, I'd have to restrict myself to the measurable facts and stick strictly to the data sheets. You, too, can do that by browsing the World Wide Web at **http://www. psion.com or http://www. velo1.com** .

So, like recommending restaurants to friends, I hesitate to say which one is absolutely the best. My only recommendation is that if you want (as opposed to need) a pocket computer, choose the one that suits you, rather than simply accepting someone else's choice.

Peter Fletcher is Electronic Design's U.K. correspondent. His e-mail address is: panflet@cix.compulink.co.uk.

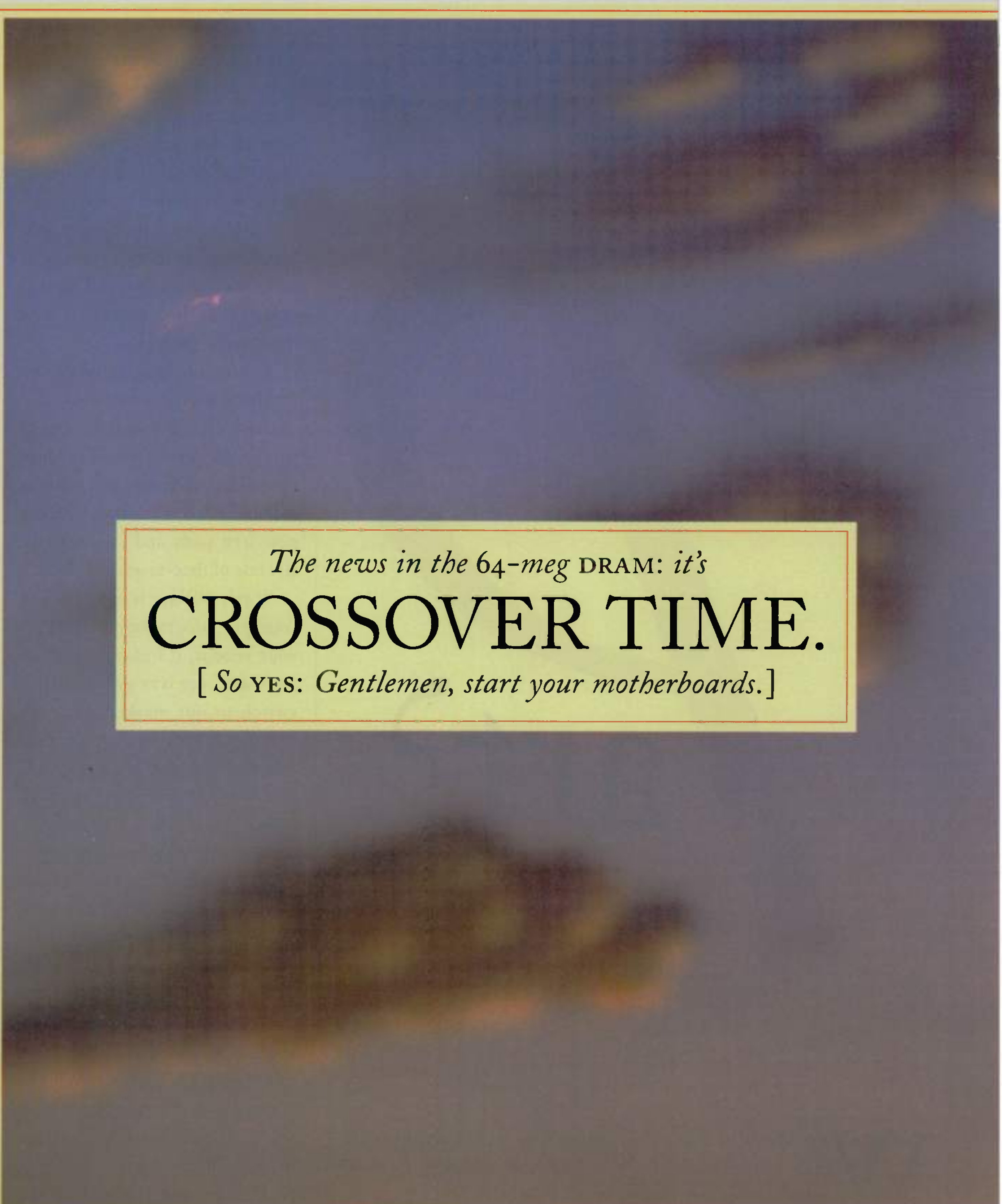
OFF THE SHELF

Developing USB PC Peripherals is a guide to the Universal Serial Bus (USB) specification version 1.0. The book provides a step-by-step methodology while following thorough design practices. It contains graphics, firmware, software code examples, and key industry contact numbers to assist readers in developing USB PC peripherals. An accompanying disk includes the sample code from the book for a WDM driver, the USB microcontroller firmware, and host application software. The book is priced at $29.95. Contact Annabooks, 11838 Bernardo Plaza Court, San Diego, CA 92128-2414; (800) 462-1042; fax (619) 673-1432; Internet: http://www.annabooks.com.

Asynchronous Transfer Mode (ATM) Networks addresses issues in developing ATM networks. The book lays the groundwork for future research papers on obstacles on the road to ATM, communication subsystems for high-speed networks, ATM requirements, congestion control mechanisms, video sources, multimedia networking performance requirements, and other key subjects. The 228-page book is priced at $75. Contact The Penton Institute, 1100 Superior Avenue, Cleveland, OH 44114; (800) 223-9150; fax (216) 696-6023; Internet: http://www.penton.com.

Introduction to Modern Statistical Quality Control and Management Techniques covers variables and attributes control charts, and topics of quality function deployment (QFD), benchmarking, ISO 9000 certification, quality awards, and the seven quality management tools. The book looks at the lives and contributions of the four main quality innovators: Shewhart, Deming, Ishikawa, and Juran. The 368-page book is priced at $54.95. Contact St. Lucie Press, 2000 Corporate Boulevard, N.W., Boca Raton, FL 33431; (800) 272-7737; fax (800) 374-3401; Internet: http://www.slpress.com.

(AN ITEM FOR THE OLDE CURIOSITY SHOPPE.)



The news in the 64-meg DRAM: *it's*

CROSSOVER TIME.

[*So* YES: *Gentlemen, start your motherboards.*]

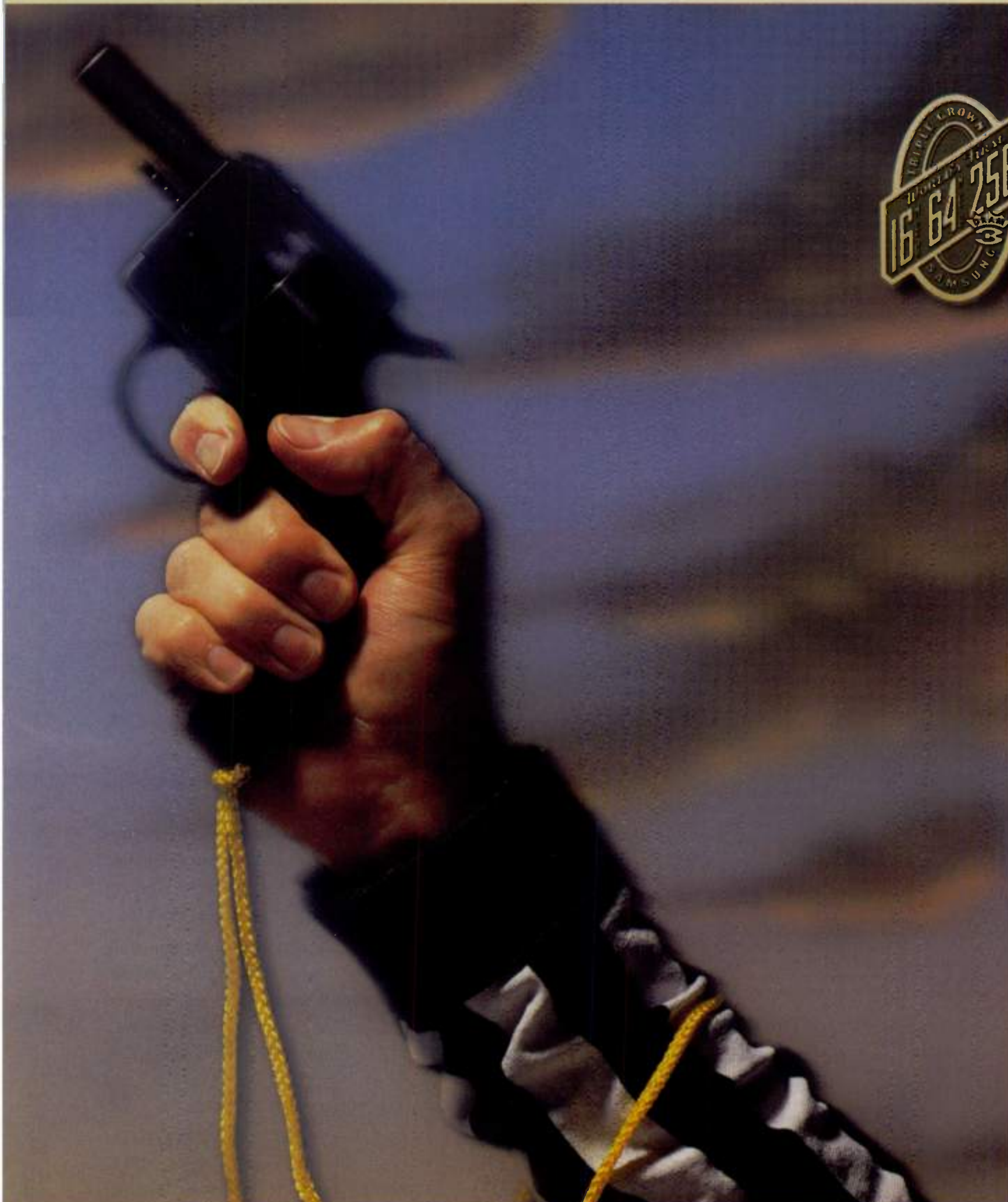
When something as important as DRAM crossover is ready to happen, you want to be prepared.

And what we have to tell you is exactly that: it's ready to happen.

Which means you're going to be able to capitalize on the competitive advantage the 64-meg can give you.

But only if you are in fact prepared. Designed in, ramped, ready to go. With your motherboards started.

Because like most races, this one belongs to the swift.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OFF THE SHELF

The Electrical Engineering Handbook, 2nd Edition is a complete reference for answering questions encountered by engineers in industry, government, or academia. The book's 12 major sections encompass the entire field of electrical engineering, including circuits, signal processing, electronics, electromagnetics, electrical effects, and energy. Also covered are trends in the fields of communications, digital devices, computer engineering, systems, and biomedical engineering. Nearly 2000 terms are defined and explained, and the book includes over 1700 figures and 3000 equations and formulas. The book is priced at $110, plus $9.95 shipping and handling for the first volume and $3.95 per additional volume. Contact CRC Press, 2000 Corporate Blvd. N.W., Boca Raton, FL 33431-9868; (800) 272-7737; fax (800) 374-3401; Internet: http://www.crcpress.com.

Sensors Handbook provides advice on selecting and using the optimum sensor for any given application. The book gives readers information on the use of sensors to measure size, speed, color, temperature, pressure, volume, flow-rate, orientation, and other characteristics in the management of complex processes. Featured are descriptions of hands-on applications in fields ranging from manufacturing engineering, aerospace, and defense, to pharmaceuticals, medicine, agriculture, and the environment. The 1024-page book is priced at $115. Contact McGraw Hill Inc., P.O. Box 545, Blacklick, OH 43004-0545; (800) 722-4726; fax (614) 755-5645; Internet: http://www.mcgraw-hill.com.

High-Sensitivity Radio Astronomy discusses how high sensitivity is leading to understanding and breakthroughs in radio spectral-line analysis, radio continuum observations of galaxies, cosmology, pulsars, and radio emission from stars. New and enhanced instruments are thoroughly reviewed, and featured is a glimpse of the telescopes planned for the future. The 300-page book is priced at $69.95. Contact Cambridge University Press, 40 W. 20th St., New York, N.Y. 10011-4211.

TIPS ON INVESTING

Asset allocation is one of today's hottest investment topics. When you allocate your assets, you decide how much money to commit to various asset types to address your investment goals.

Asset allocation has become even more important in recent years due to the globalization of the world economy and the volatility of economic indicators and financial markets. It diversifies your portfolio and could help improve your overall potential return while reducing risk. The way you allocate assets could have a major impact on your portfolio's return.

HENRY WIESEL
CONTRIBUTING EDITOR

Asset allocation is a highly personalized process that considers all aspects of your goals, investment objectives, and financial resources. If you're already retired, chances are your primary goal is to provide sufficient income to maintain your lifestyle while preserving capital for the future. At the same time, you have to preserve your buying power. Therefore, you must consider how inflation and taxes will affect your ability to maintain the lifestyle you're accustomed to.

If retirement is far in your future, your focus is on building a nest egg while setting money aside for other objectives: Educating children, buying a second home, or paying for your current lifestyle. Whatever your goals, your financial needs are complex. But they could be manageable when you allocate your assets properly.

After identifying your financial goals, define your risk tolerance. Are you conservative, moderate, or aggressive? This will determine how much you should allocate to the major asset classes—stocks, bonds, and cash instruments—which have different combinations of potential risk and reward. You also should evaluate the relative importance of the major investment objectives:

Growth: The ability of an investment to appreciate in value over a period of time. Individual stocks and equity-based mutual funds and variable annuities are among growth-oriented investments.

Income: The ability of an investment to provide current and/or future income. Government, corporate, and municipal bonds are excellent choices. Fixed annuities provide tax-deferred investing for future income.

Liquidity: The ability to turn an investment into cash as needed with minimal risk or penalty. Money market funds, certificates of deposit, and savings accounts are highly liquid.

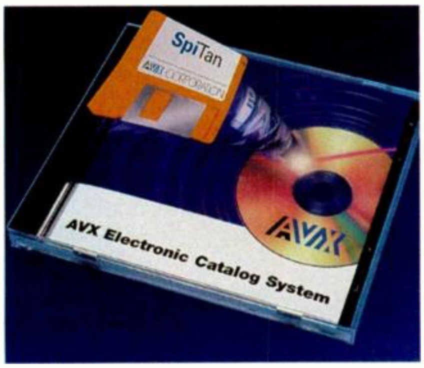
Taxability: The ability of an investment to maximize your after-tax return. Municipal bonds and tax-deferred annuities make sense for the tax-sensitive investor. Every investor can take advantage of the tax-deferred opportunities such as IRAs or 401(k)s.

Whatever your goals, it's a good idea to have some combination of each class in your portfolio. Consult with a financial advisor for more information.

Henry Wiesel is a Vice President, Financial Consultant, and Qualified Pension Coordinator at Smith Barney. He may be contacted at 1040 Broad St., 2nd Floor, Shrewsbury, NJ 07702; (800) 631-3331, ext. 8563.

FLIPPING THROUGH THE INTERNET ROLODEX

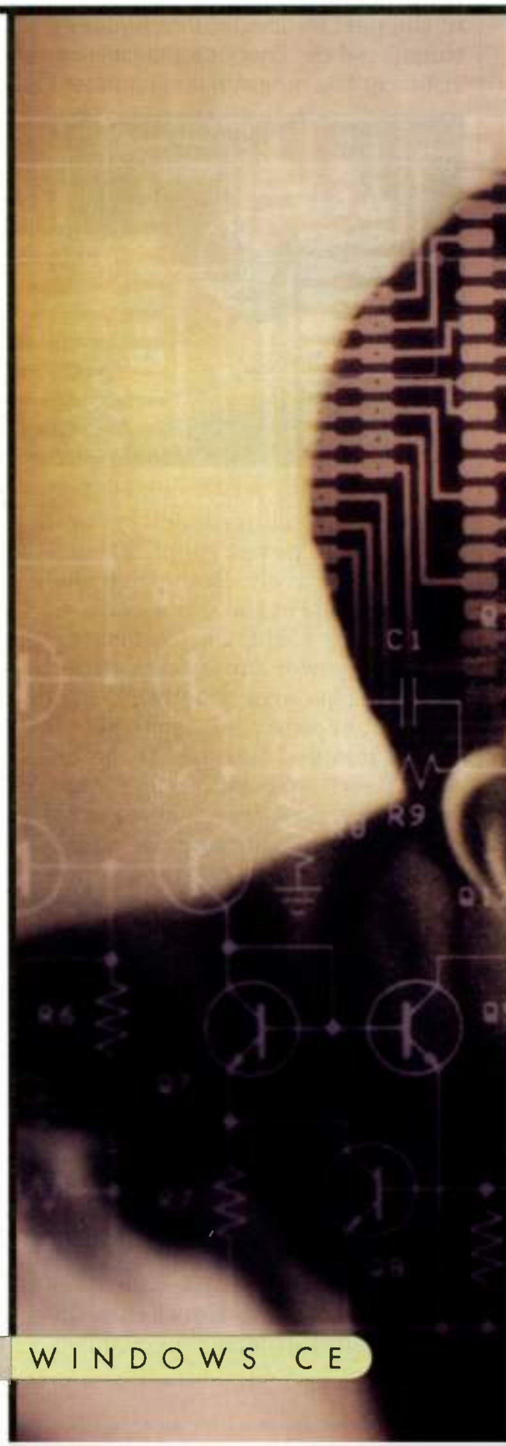
http://www.avxcorp.com: Engineers investigating Spice information on tantalum capacitors should point their browsers to AVX Corporation's new site. The site features AVX's SpiTan, an interesting bit of software that is specifically designed around tantalum capacitors. Users can just click and point to enter the product type, case size, capacitance value, voltage rating, frequency, and temperature of the operation. Then, the program provides the impedance of the part over a wide frequency range, and the equivalent series resistance. The program is reminiscent



of SpiCap and CALCI, which deal with ceramic chip capacitors and switch-mode power supply capacitors, respectively. Both programs also are found at the site. Details on the company's MLC and tantalum capacitors, power supply capacitors, resistor chips, arrays, networks, and integrated passive components all can be found at the site. Technical data on such topics as thin-film inductors, SMT fuses, transient suppressors, filters, piezos, and timing devices also can be accessed at this site. And, if visitors are so interested, they have the opportunity to search AVX's financial summaries, and can even browse through a corporate overview.

http://www.randmh.com: How exactly do you spell e-commerce? R-A-N-D. Rand Materials Handling Equipment Company's new World Wide Web site allows all visitors to search it's database for a wide range of materials handling equipment, and packaging products. In addition, the database is incorporated into the site's on-line ordering mechanism. When a surfer clicks on any of the listed products, the link will take that person to a detailed product data page. Complete product specifications are found at this page, including photographs, pricing, and ordering information. Items listed include dock boards and plates, safety ladders, pallet trucks, bulk storage racks, flammable storage cabinets, industrial storage cabinets, pallet racks, open and closed shelving, wire shelving, canvas basket trucks, hand trucks, shelf trucks, hoppers, workbenches, and stools. Visitors to the site also are encouraged to watch for a new monthly featured product as well as bonus buys.

YOU DIDN'T GO THROUGH 16,000 HOURS OF PHYSICS TO DESIGN A PRODUCT JUST LIKE EVERYONE ELSE.



You paid a lot of dues to get here. And you're not about to waste it all by designing a bland (yawn) expected (yawn) Windows® CE application.

But to create the best, you need to start with the best. And NEC's V_R Series™ MIPS® RISC processors are clearly superior because they offer you a total system solution - the whole product to meet your needs.

NEC offers a family of high-performance processors designed and optimized for Microsoft® Windows CE-based applications, not just a partial solution. The V_R4101™ and V_R4102™ provide high MIPS/Watt for low-power, battery-operated devices, and the V_R4300™ gives you impressive 64-bit performance. You also get companion PCI chipsets and a broad range of design development and debugging tools to get you to market faster, including RTOS, compilers, simulation tools, evaluation boards and Windows CE reference designs.

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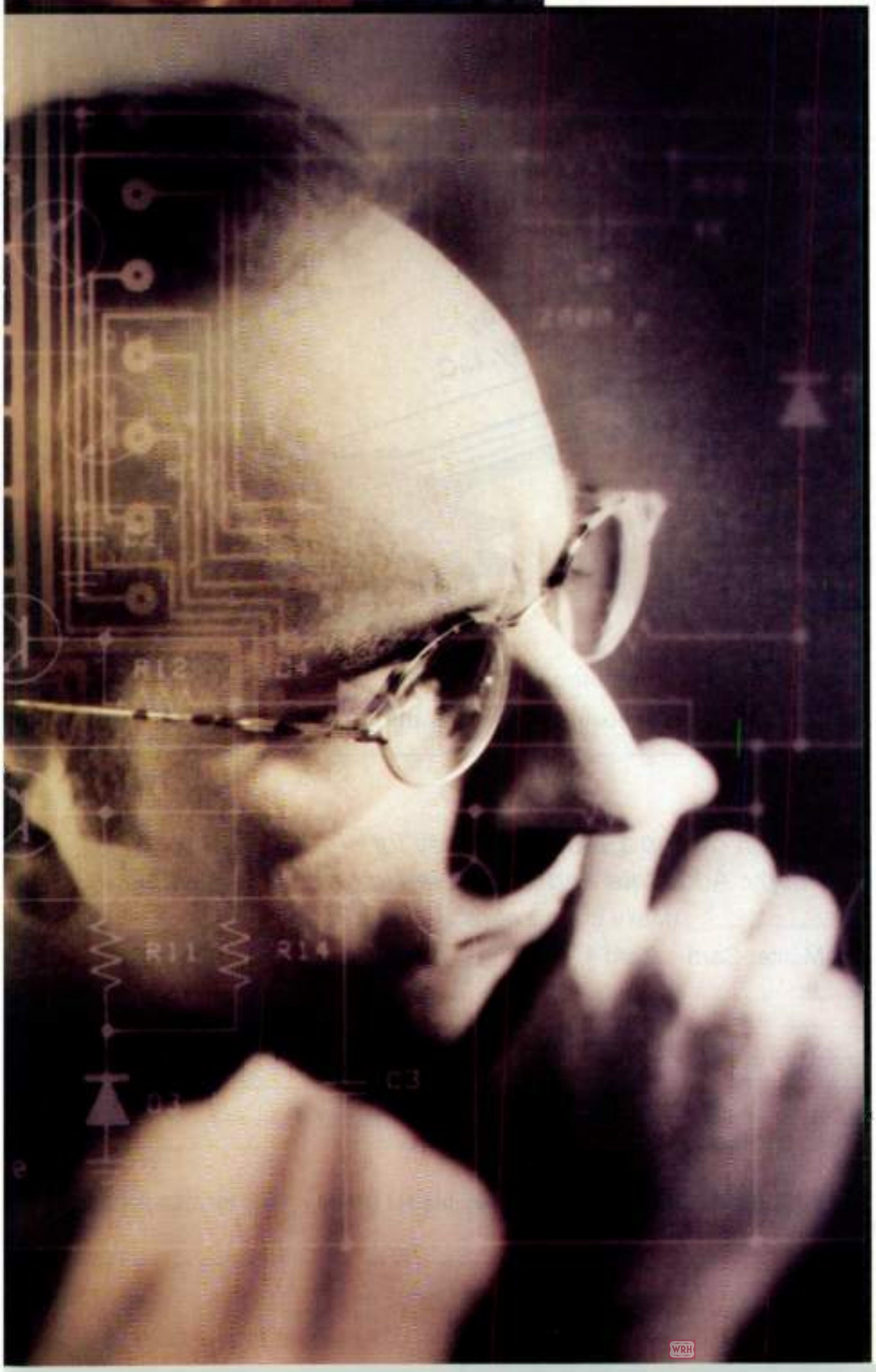
Get started today. Just call **1-800-366-9782** to find out how to speed your next Windows CE design with your V_R Series Design Kit.

Anyone can calculate the mass of the earth. But not everyone can create a Windows CE product that changes it for the better.

V_R SERIES PROCESSORS WINDOWS CE

V_R SERIES / WINDOWS CE

	V_R4101™	V_R4102™	V_R4300™
Pipeline Frequency	33Mhz	66MHz	100/133MHz
I/D Cache	2 / 1	4 / 1	16 / 8
Dhrystone MIPS	37	74	131/177
Power Consumption	200mW	250mW	1.8/2.2W
Supply Voltage	3.3V	3.3V	3.3V
MIPS/W	185	320	
Windows CE Support	V1.01	V2.0	V2.0
Feature Highlights	5 Ch. DMA Cont. RAM/ROM Cont. Serial Interface IrDA™	Soft Modem 4-mode PMU 10-bit DAC/ADC Single-cycle MAC	High-perf. MMU Single/Double Precision FP Ideal for high performance embedded applications



V_R4101. Created for Windows CE products, it offers ultra-low power and incredible MIPS per Watt.

V_R4102. Delivers Windows CE hand-held computer applications tremendous power and performance in a high-integration system on a chip.

V_R4300. Ideal where high-performance and low-cost drive your design. Offers outstanding MIPS per dollar.

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READER SERVICE 191

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Career rankings are important to most professionals, especially engineers. The Institute of Electrical and Electronics Engineers (IEEE) has made it their business (amongst other things) to collect and disseminate information pertaining to the careers of engineers. One way of finding this important data is through asking the engineers themselves.

Via a call for papers, IEEE-USA (United States Activities) is looking for success stories from engineers to include in its 1998 Careers Conference, "Engineering Careers into the 21st Century: Maximizing Individual and Organizational Growth." The conference, scheduled for April 30-May 1, will be held in Phoenix, Ariz. Individuals who think that their current research or expert opinions could prove useful to the conference are encouraged to send in proposals and 500-word abstracts.

The following are topics the IEEE-USA is looking to target:

- Benchmark practices for developing engineers to succeed in new models of work.
- Case studies of successful environments that provide engineers with career development or new career-management opportunities.
- New designs for development and maintenance of engineering careers.
- Partnerships among employers and engineers, associations, or universities that foster successful careers for engineers.
- Retention and development of engineers in a tight labor market.

All proposals must be in to the IEEE-USA by Oct. 1. The Institute will notify speakers between Nov. 1-15. Papers must be in by Feb. 1, 1998.

Send all correspondence to: IEEE-USA, 1828 L St., N.W., Suite 1202, Washington, D.C. 20036-5104. Any questions may be directed to Scott Grayson at (202) 785-0017, ext. 339, or e-mail: s.grayson@ieee.org.

Another very popular and extremely useful function of the IEEE is to supply its members with directories and other forms of literature. Two recent releases are the "1997 National Directory of Electrotechnology Consultants," and "The IEEE Standard Dictionary of Electrical and Electronics Terms, Sixth Edition." Both publications are two volumes that today's engineer will find invaluable.

The national consultants directory was produced by the IEEE-USA's Alliance of IEEE Consultants' Networks. It's mission is to help raise the awareness of the engineering community to the IEEE's self-employed members who live in the U.S. This year's volume is the second annual national directory.

Packed with over 400 electrical, electronics, management, and software consultants, the directory is indexed by category and by state. There also is a listing of specialties. Additionally, the directory includes information on local referrals.

"The IEEE Standard Dictionary of Electrical and Electronics Terms" has a lineage that goes back to the 1941 "American Standard Definitions of Electrical Terms." The publication is also known as IEEE Std 100. This edition includes all the IEEE-approved standards for defined terminology through December 1996.

Each term in the dictionary is categorized by its technical subject area. Of course, all the abbreviations for those areas are within the first seven pages. The terms also are referenced to the publications or standards in which they appear.

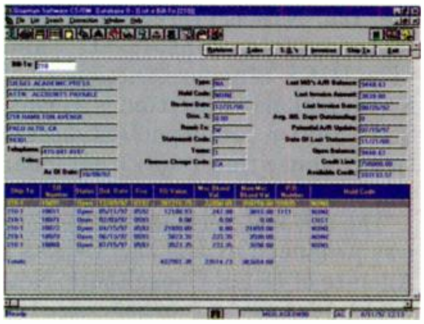
For free copies of the directory, contact William Anderson at (202) 785-0017, ext. 330, or e-mail him at w.anderson@ieee.org.

For information on obtaining the standard dictionary, contact Christopher Currie at (202) 785-0017, ext. 324, or e-mail: c.currie@ieee.org. Information also may be obtained through the previously mentioned address.—DS

HOT PC PRODUCTS

StarMan, developed by Quantum Software and marketed by Bradmark Technologies, is designed to act as a graphical-user interface (GUI) for Computer Associates' ManMan (previously ASK ManMan). The Windows-based application works as a client/server GUI for the HP3000 version of ManMan, the 20-year-old manufacturing management software used by such manufacturers as Compaq, Spectra-Physics, and Ace Controls.

Traditionally, ManMan's display screens are limited to showing only one aspect of the manufacturing, order entry, or order management data at a time. Users have toggled between two sessions on the HP3000, but this method draws on the network resources. Managers also had to "dumb down" their systems in the past because they were using fully loaded PCs to house the ManMan system without the Windows interface.



StarMan still incorporates the HP3000 as the server and still uses ManMan as the primary application, but works with both to bring the inventory process into the '90s. It does not use terminal emulation. Instead, StarMan uses Visual Basic to create the Windows display.

One of the primary advantages to using the new system with ManMan is the increased productivity. According to Bradmark, StarMan increases the performance of the HP3000 by about 50% by distributing the processing power between the server and the PC. As a result, the server's CPU overhead also drops 50%.

A useful option that network managers might want to consider is the StarMan development kit. With this kit, developers can integrate other host-based legacy applications into Windows, Internet, and/or intranet applications on the PC. With this option, users can truly integrate ManMan data with any number of applications, including e-mail Microsoft Word, and Excel.

Pricing for the StarMan GUI is based on system-tiered pricing. Prices range from $10,000 for an HP3000 Mocel 918 to $75,000 for Model 997X8. Volume discounts are offered.

Contact Bradmark Technologies, 4265 San Felipe, Suite 800, Houston, TX 77027-2913; (800) 621-2808; fax (713) 621-1639; Internet: http://www.bradmark.com.

Vodavi Communications Systems is introducing a new member of its video communications family, TeleSight 320, a desktop videoconferencing system that complies with H.320 standards.

The system has value in the home and office. When TeleSight is used over an ISDN line, it can bring video communications at the rate of 30 fps, allowing for simultaneous file sharing at each end of the communication. It also functions as an ISDN terminal adapter at 128 kbits/s. TeleSight is bundled with Microsoft's Net Meeting, which allows home offices to communicate with branch offices.

The system is available in kits and fully configured turnkey systems on Pentium-based PCs. The kit includes cabling, a single-board CODEC, telephone handset, camera, and software. The turnkey system comes with an output for a second monitor or TV, a second camera input, and a second microphone connection. The kit is priced at $1395; the turnkey system goes for $3995.

Contact Vodavi Communications Systems Inc., 8300 E. Raintree Dr., Scottsdale, AZ 85260; (602) 443-6054; fax (602) 483-0144; Internet: http://www.vodavi.com.

INTERNET NEWS

The ever-present greed for speed can now be satisfied through the use of Speed Surfer. The new PC utility from Kiss Software jump-starts Internet browsers and modems so users can fly through their Internet experience. Speed Surfer is compatible with both Netscape and Microsoft Explorer.

Speed Surfer's style is to use smart agents in zipping up access times. Most standard accelerators just load all the links of the page currently on view. Speed Surfer's technology loads the text, links, and graphics on the pages that the user is most likely going to visit next.

All the preloaded data is stored on the hard drive, providing the fastest access times to linked pages. Frequent users benefit from Speed Surfer's smart agent technology because it learns the habits of the user as he or she surfs the 'Net. Consequently, Internet access is speedier, which results in lower connect costs.

Speed Surfer requires a 486 or better PC running Windows 95 or NT 4.0, a direct Internet connection (SLIP/PPP), 8 Mbytes of RAM, and Netscape 2.0 or higher or Microsoft Explorer 3.0.

The software is priced at $29.95, but a free, downloadable 30-day trial version is available at the company's web site.

For more information, contact Kiss Software Corporation, 5000 Birch St., Suite 4000, West Tower, Newport Beach, CA 92660; (714) 979-KISS; fax (714) 832-7805; Internet: http://www.kissco.com.

Another new high-speed Internet technology that's recently become available is OverVoice from CAIS Internet, a division of CGX Communications. OverVoice uses existing telephone wiring to bring simultaneous phone service and 24-hour access to the Internet to select populations in multi-dwelling units. The first hotel to offer the service is the Washington Marriott hotel in downtown Washington D.C.

The OverVoice connection to the Internet clocks in at 1.54 to 10 Mbytes/s. Real estate developers such as Charles E. Smith Residential Realty Inc., in the Arlington Courthouse Plaza Apartments, Arlington, Va., have capitalized on the distribution and licensing agreement by offering enhanced communication services to their renters that they wouldn't have gotten elsewhere.

Residents at the Courthouse apartments who live on the top six floors, can try out the service for no charge for six months. After the trial, the fee for the service is expected to rise to between $40 and $50 per month. That's about the price tag for a standard Internet dial-up account and a dedicated phone line for Internet access.

Users don't have to dial in or dedicate a phone line to Internet use. They can carry on a conversation at the same time they're sending e-mail to business or personal contacts. According to CGX Communications president Ulysses Auger II, "The phone became a utility of mass appeal and mass use because it was always on 24 hours a day." As with phone service, people use the Internet 24 hours a day, except those who need to disconnect to use the phone. OverVoice eliminates this limitation.

The technology marries the Ethernet standard with the average home PC. Users need only purchase an Ethernet card, which typically costs from $17 to $30 in an average computer retail store.

OverVoice works by connecting the multidwelling units to an Ethernet hub located within the building. A high-speed line is connected to the hub, which, in turn, is connected to the OverVoice Aggregator. The proprietary device aggregates the Internet traffic on site, as opposed to at the telephone company's central office.

Contact CAIS Internet, 6861 Elm St., McLean, VA 22101; (703) 448-4470; fax (703) 790-8805; Internet: http://www.cais.net.

IPC Completes Major Benchmark Study

The Institute for Interconnecting and Packaging Electronic Circuits (IPC) has just completed a major study, "The IPC Study of Quality Benchmarks for Printed Wiring Boards," to determine the performance levels and production quality of North American printed wiring board (PWB) manufacturers.

Participating were fifty North American PWB companies, representing $2 billion in sales in 1996. They examined records on quality, customer performance, and finances

Highlights from the report include: Sales per employee ranged from $54,000 to $194,000. The median was $97,000; participants averaged customer returns on shipments of 2.1% based on dollars and 2.5% based on actual boards; and on-time delivery by laminated manufacturers and process consumable suppliers averaged 93% and 95% respectively.

For more information on the report, or how to become a participant in the next IPC benchmark, contact Kim Sterling, IPC director of market research, at (847) 509-9700, ext. 305; e-mail: KimSterling@ipc.org.—**MS**

KMET'S KORNER

...Perspective on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
P. O. Box 1070, 100 Prickly Pear Rd., Verdi, NV 89439; (702) 345-1455; fax (702) 345-0804

RON KMETOVICZ
CONTRIBUTING EDITOR

A few weeks ago, in need of isolation from city, suburbia, and responsibility, six of us ventured to central Nevada on a backpacking trip. For a week, we remained completely isolated and made no contact with other humans. I brought along a few issues of *Scientific American* for entertainment.

An article featured in the July issue titled "Taking Computers to Task" provided ample material for thought under the stars. A graph embedded within the text burned an image into the neural structure of my brain. By equating area to the number of commands in two versions of Microsoft Word, a graphic representation of the complexity of Word 2.0c (311 commands) to Word 97 (1033 commands) resulted. My first reaction when seeing this: Instead of learning Word, I could have learned the basics of Japanese. But, upon careful reflection, I found an error in my logic—I do not own Word 97 and, if I did, I would not know how to use its 1033 commands. My software shelf contains Word for DOS, Word 2.0, Word 6.0, and some old DOS word processors. Overall, I have probably spent close to $500 on word processors over the past 10 years. On the latter versions, I use only a fraction of the functions they contain. So why do I continue to have them in my possession?

To determine if these new products improve my writing productivity, I am running a simple experiment on the generation of this column. Going back to the late 80's, I'm using the word processor in Works for DOS, the oldest word processor remaining in my possession. I think and type with it at the same rate as with the new editions. The new versions are no better, or worse, for creating original text. As a by-product of the experiment, I also found the old software to be very easy to use. Simply put, for me, the new tools do not improve my productivity when creating original material, and they really offer minimal ease-of-use benefit. In effect, the answer to building my collection lies elsewhere.

I was forced into buying them! Customers, associates, and friends—for reasons that are known only to them—moved to the new editions. After a period of time, a file generated by the upgrade shows up in my computer. When this happens, I'm off to the software store to purchase the new release. This way, I stay in lockstep with those eagerly adopting change while concurrently preserving my image. Along the way, many other suppliers benefit from the push forward. Usually, new software means a new hard disk and more memory. After two upgrade cycles, it's a new computer.

However, I'm beginning to see cracks in the old model; maybe even a revolt. The installed base of computer users seems to be losing interest in upgrading to more complex word processors, spread sheets, databases, and presentation software. They want product with demonstrated and measurable improvements in productivity, a trend that goes completely against supplying product with increasing complexity.

From a time-to-market perspective, I encourage product developers to review their portfolio of products under development. Pay very close attention to those users that are being weighed down by an abundance of functionality with minimal performance boost. Rethink all business issues about the product; determine if it might be in your best interest to cancel the effort. Look for ways to concentrate on functionality to increase productivity, and do it at reduced cost. Then, after you've taken these steps, build a new product offering to meet the new market conditions.

To obtain an e-mail copy of "The Complete List of Reasons for Late Product Information," contact Mr. Kmetovicz at kmetovicz@aol.com

QUICKNEWS

It's A Gas—Industrial gas company Praxair has recently introduced two new systems to help monitor and control chemicals and gases used in the fabrication of semiconductors. Praxair's two new offerings are the Ultrapurge 2000 gas control unit and the Praxair Materials Management System. The Materials Management System is based on Praxair's Intellution FIX32 SCADA system.

Ultrapurge 2000's advantage is that it is an automated gas control system with communication capabilities. It works with standard equipment and protocols. Ultrapurge 2000 is compliant with RS232, RS485, Ethernet, and LONworks.

The Materials Management System is designed to increase chemical and gas delivery automation and reliability. It functions by integrating existing gas systems and providing users with access to all gas system operating data. The system can work across multiple platforms to control gas delivery systems.

For more information, contact Praxair Inc., 39 Old Ridgebury Rd., Danbury, CT 06810; (203) 837-2032; fax (203) 837-2454.

This DIVA Works—Cutting out the extra hardware, Eicon Technology has introduced an ISDN server card that packages highly integrated analog, digital, and mobile communications all in one unit. Since the majority of businesses participating in American commerce are of the small-to-medium-sized variety, they often need the multifunctionality of these types of products in order to stay afloat financially. The DIVA Basic Rate ISDN (BRI) server, at a reasonable $700, allows these enterprises to do that.

DIVA BRI uses two B-channels and digital signal processing technology to provide users with simultaneous analog and ISDN transmissions. The new card lets corporate LAN users hook up to a variety of ISDN providers. Additionally, DIVA BRI users can use the connection to send and receive faxes. Remote users have the option of using ISDNs, modems, or GSM mobile phones to access and transfer data.

The server card offers full software support for a large range of operating systems and client/server cards in the DIVA family of products. Communication standards CAPI and PPP also are supported. Always important, international standards are supported by DIVA BRI.

For more information, contact Eicon Technology, 14755 Preston Rd., Suite 620, Dallas, TX 75240; (800) 803-4266; fax (972) 239-3304; Internet: http://www.eicon.com.

The Missing Link—Source Media and LSI Logic have teamed to produce an advanced interactive TV chip. Billed as an ASIC, the chip will connect analog to digital in the multimedia television blitz that promises to change an entire generation's view of MTV. Services such as e-mail and Internet access, and a link to advanced analog set-top boxes, will be available with the chip.

Based on Source Media's Interactive Channel operating system, the ASIC uses patented frame storing capabilities to enable high-speed multimedia activity. The key to the chip is that it brings digital functionality to analog systems.

In comparison to Source Media's first-generation design, the ASIC delivers 100 times the number of gates (about a quarter of a million). LSI Logic's end of the bargain is to supply the foundation, their embedded high-performance RISC MIPS processor core, for the chip.

The Interactive Channel operating system includes traffic updates; news, weather, and sports; games; directory assistance; TV programming guides; educational programming; and catalog shopping.

Contact Interactive Channel, 5400 L.E.J. Freeway, Suite 680; Dallas, TX 75240; (972) 701-5420; fax (972) 701-5455.

Measuring Industry Needs

A new study recently developed and published by the National Institute of Standards and Technology's (NIST) Electronics and Electrical Engineering Laboratory looks at the measurement needs of an industry in the midst of fundamental change. It is expected that in the future, the most successful competitors in this sector will be those organizations that will best use modern technologies to produce less expensive technology.

Authored by NIST staff members Gerald J. Fitzpatrick, James K. Olthoff, and Ronald M. Powell, "Measurement Support for the U.S. Electric-Power Industry in the Era of Deregulation" indicates that sweeping changes are currently taking place in the U.S. electric power industry as a result of deregulation, and with that increased competition in providing electric power. Along with these changes are the real possibilities of lower prices and increased supply, as well as minimal increases in associated capital facilities. As a result, the study suggests that the industry as a whole must fully exploit the capabilities of new and existing technology to achieve these goals.

The study identifies the measurement capabilities that power producers and distributors will need to meet these increasing challenges to a business sector that has an impact on the lives of every U.S. citizen and company, has annual sales exceeding $208 billion, and employs over 440,000 people.

In laying out the NIST's recommendations, the study's basic approach is to characterize:

- The driving forces behind deregulation's changes in the electric power industry;
- The technologies needed to address the changes;
- The specific measurement support needed from the NIST to assist industry in making these technologies happen.

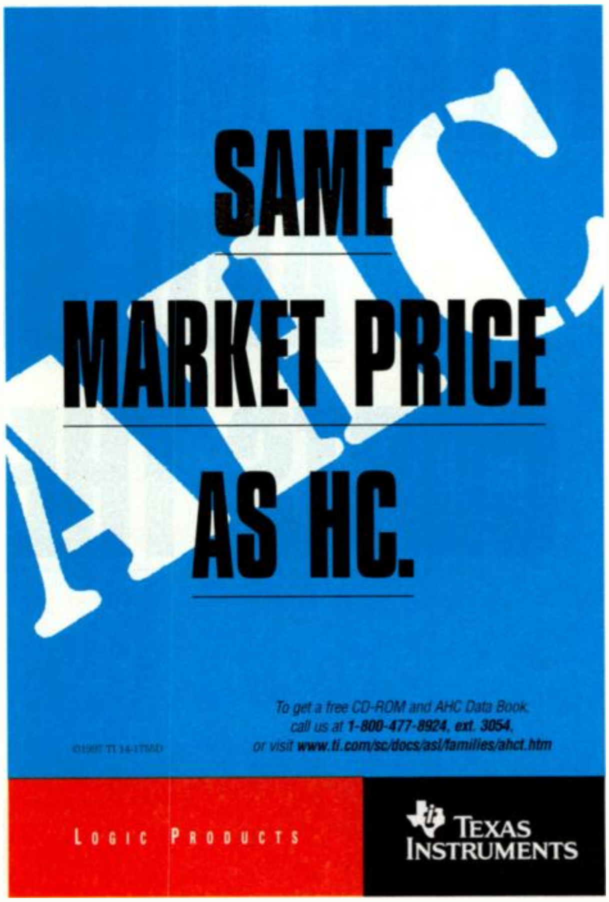
These issues are discussed with four industry concerns in mind:

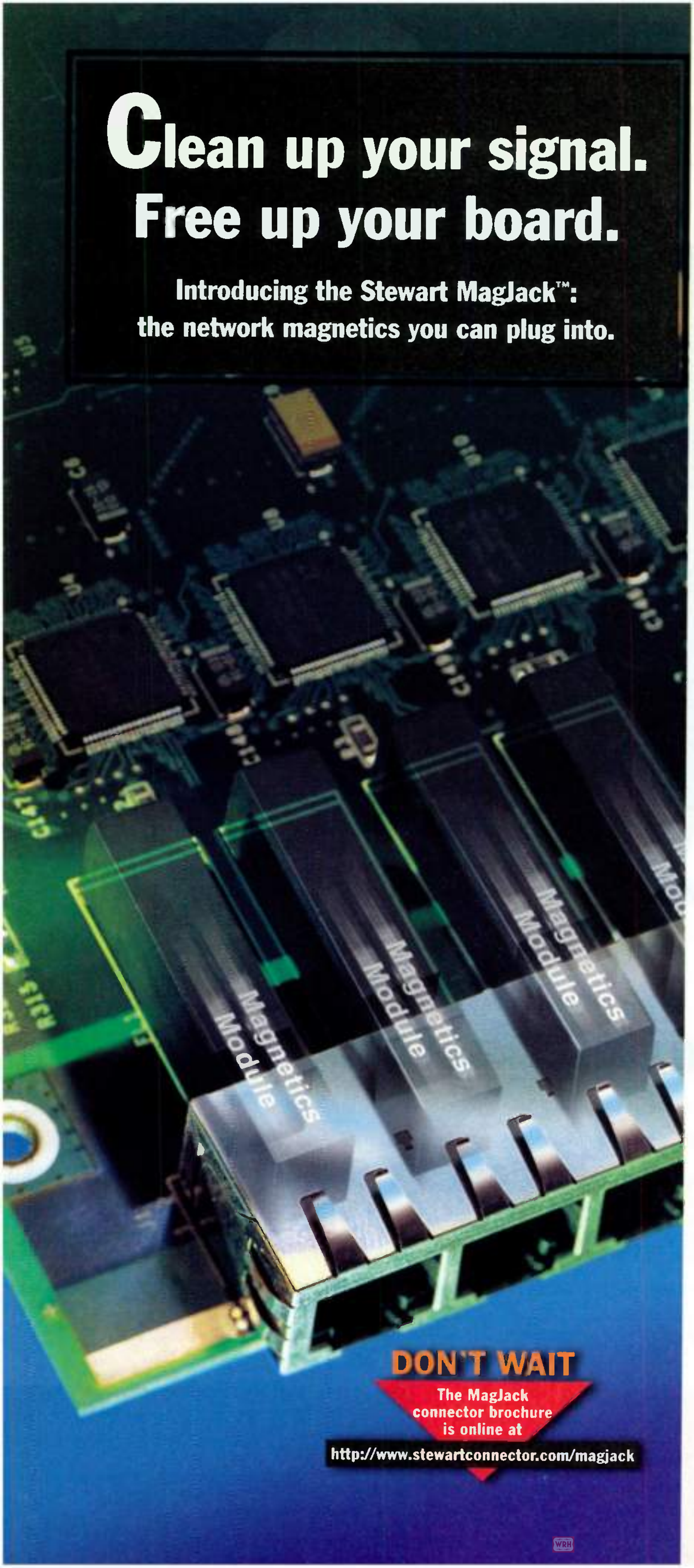
(1) Transmission and distribution efficiency, reliability, and stability;
(2) Equity in trade and international competitiveness;
(3) Global warming and health effects;
(4) Power quality.

For this all to make sense to those who need to know and become fully informed, the study uses these keywords to get the point across: Competition; deregulation; electric-power distribution; electric-power generation; electric-power industry; electric-power transmission; electric utilities; electrical-equipment industry; electrical measurements; electrical quantities; electricity; measurement capability; metrology; and utilities.

The NIST stresses that the industry itself is still uncertain about what kind of changes will be taking place in the next few years. Their aim is to maintain close contact with the industry in order to maintain a proper perspective on the needs and associated priorities required for the NIST's response. To that end, the study was developed by the NIST in consultation with industry, government, and university experts. The NIST invites comments on the report's assessment of the measurement needs of the electric power industry as well as the agency's role in meeting them. The NIST's purpose is to assure that its resources are applied as effectively as possible in support of the U.S. electric-power industry and its customers nationwide.

Those interested in obtaining a single copy of the report (NISTIR 6007) may contact James K. Olthoff, Metrology B344, NIST, Gaithersburg, MD 20899-0001; fax (301) 948-5796; e-mail: jamesolthoff@nist.gov. Multiple copies also are available from the National Technical Information Service, Springfield, VA 22161; (703) 487-4650; fax (703) 321-8547; e-mail: orders@ntis.fedworld.gov. Use Order #PB 97-152508.—**MS**





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Hardware And Software Co-Verification—Key To Co-Design

Increased Software Content, Design Complexity, And Time-To-Market Pressures Drive Designers To Validate Systems In New Ways.

SERGE LEEF, Mentor Graphics Corp., 8005 S.W. Boeckman Rd., Wilsonville, OR 97070-7777, (503) 685-7000; e-mail: serge_leef@mentorg.com.

It's not news that in the past decade the composition of embedded systems has undergone drastic changes. Everyone in the EDA industry is aware of lower CPU prices, advanced ASIC technology, and shorter time-to-market windows. However, the combination of these trends dramatically increased the critical need for comprehensive hardware/software co-verification. As a result, current system design methodologies are measurably strained and sometimes pushed to obsolescence, forcing designers to reexamine modern design practices.

Advances in manufacturing technology and the turning of microprocessors and microcontrollers into commodities instigated dramatic decreases in complex, 32-bit CPU prices, with embedded system designers being the principal beneficiaries. Enormous computing capacity has suddenly become available to be used in previously underpowered systems. These CPUs, seen mostly in high-end computing, routinely started showing up in printers, telephones, appliances, and autos.

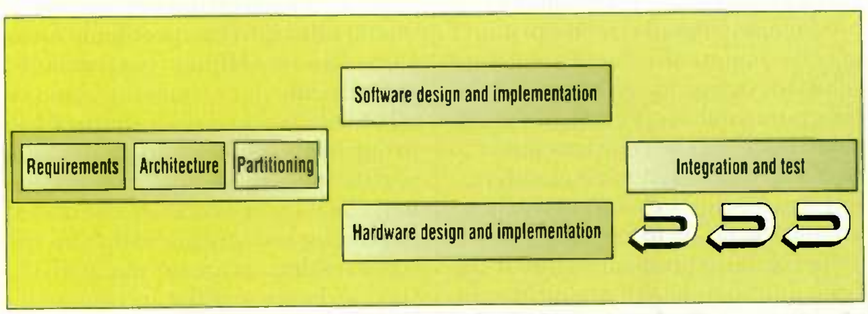
The appeal of high-end processors was so strong that many design teams overlooked the inherent challenges associated with the surrounding hardware and software. Elaborate external interfaces presented by these 32-bit processors called for complex interface logic to handle communications between the CPU and ASICs. Where assembly language drivers and diagnostics were commonplace in the 8- and 16-bit CPUs, the 32-bit machines demanded more voluminous and complex software to manage all the resources that new CPUs brought into the game.

The fact that 32-bit CPUs utilize complex hardware structures such as pipelines, caches, and pre-fetch buffers, made writing the software in assembly language impractical. The software had to be written in C or C++ to take advantage of optimizing compilers. Simple schedulers and microkernels had to be replaced with sophisticated real-time operating systems (RTOS). While the hardware surrounding the CPU had to incorporate increasingly sophisticated interface logic, the software component of embedded systems also increased in both size and complexity.

ASIC vendors started providing sizable functional blocks such as embedded cores in conjunction with the traditional ASIC library elements. The high ASIC gate capacity and preexisting cores provided the possibility of creating large scale systems-on-silicon that, in extreme cases, include a CPU core, a DSP core, and up to 500,000 gates of custom logic. Clearly, the growth in size and complexity of ASIC content in embedded systems has placed a huge validation burden on the design teams. These changes also have made some of the existing tools and practices obsolete. Very large ASICs demand high memory usage and high computational throughput in simulation. Traditional use of logic and HDL-based simulation technologies is no longer adequate as the sole verification strategy. Because maximizing the chances of first-time success is crucial, many ASIC design teams are forced to reevaluate their verification strategies *(Fig. 1)*.

Solution Drawbacks

During the design and implementation phase of a hardware/software project, different organizations address



1. This diagram depicts the product phases of a typical embedded system development project. In addition to responding to market trends, designers are forced to reexamine this design process to perform comprehensive verification of their designs.

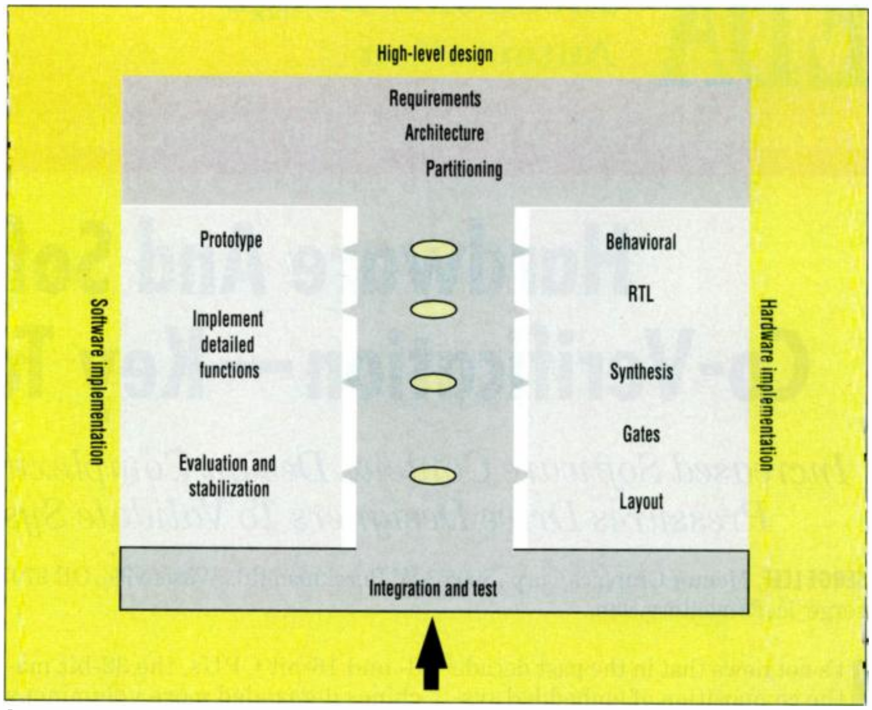
the hardware and software components of the design. For the most part, the design proceeds simultaneously, but the software team is limited in what it can complete without a physical prototype of the target design. What they can do is complete the high-level design of the software and some of the algorithm development and validation. But much of the debug and integration work cannot even begin until a hardware prototype is available.

Consequently, most designs are performed in a serial fashion. The hardware is designed, validated, and prototyped. Then the software is debugged and integrated on that prototype. The problem with this approach is that once the hardware is prototyped, changes are expensive and time-consuming to implement.

In theory, Integration and Test are the final series of checks prior to the release of the system to manufacturing. In practice, it is the first time that completed hardware and independently developed software come together as a system. At this time, numerous issues surface: misinterpretations of interface definition, out-of-date specifications, poorly communicated changes, and ineffective performance modeling. In many cases, the real software and integration debugging begins only after the hardware has been built. This debug and integration can take up to half of the project schedule.

As problems are uncovered in the integration phase, developers look for the fastest and most inexpensive ways to fix those problems. Given time and cost requirements, hardware problems are often fixed by changing the software. Unfortunately, only so much can be done in software, and the functionality or performance goals of the product may be compromised with a software solution. Occasionally, there may be programmable logic elements in the circuit that can be reprogrammed to work around hardware problems, but again, this method is working around the problem, not fixing it.

To fix these problems without the time and expense of changing the hardware, they must be discovered before hardware prototypes are created. The software must be run on the hardware while it is still in simulation, that is, a virtual prototype. Before virtual prototyping can be accomplished, the designer must be able to simulate hardware at speeds sufficient to make software execution feasible. In most cases, this means that overall simulation performance must be increased by a factor of at least 1,000 times over the current execution speeds of traditional simulation products (one to ten instructions per second). Then, the debug and development environments for the hardware and software must be brought closer together.



2. By moving system integration forward in the design cycle, as illustrated above, the risk of finding bugs late in the design process, when they are more difficult and more costly to fix, can be significantly decreased.

True Co-Verification Available

A comprehensive hardware/software co-verification environment would alleviate the problems mentioned above. Higher performance can be achieved by moving some or all of the code and data space of the program into the software domain, partitioning the design. In this manner, the memory references related to reading and writing of data in the software domain are not simulated in the hardware simulator. Removing this work from the hardware simulator can greatly improve the performance of the system. The disadvantage is that the effect of those memory references cannot be seen in hardware simulation.

While the presumption that code and data references are uninteresting is correct (most of the time), there are times when all bus activity is significant from the perspective of hardware simulation. There is a commercial product, Mentor Graphics' Seamless CVE, that maintains comparable levels of performance, and provides greater accuracy by allowing the designer to dynamically repartition the memory.

When memory references and their effects are not important, the designer can map those memory references in the software domain. At a later time in the same simulation, those memory references can be remapped into the hardware domain. This technique allows the designer to make trade-offs between the level of performance and the level of detail expected in the hardware simulation.

Integration And Simulation

Seamless CVE simulates the entire system by integrating software and hardware simulation with debug tools. To create a hardware/software co-verification environment, the tool synchro-

tense pressure on the embedded system design teams to meet tight deadlines and hit narrow market windows. While in mature markets, such as automotive and consumer, the electronic subsystem may not be in the critical path, dynamic market participants can ill afford major schedule slips that frequently result from having to change boards or ASICs during the Integration and Test phase of the design process.

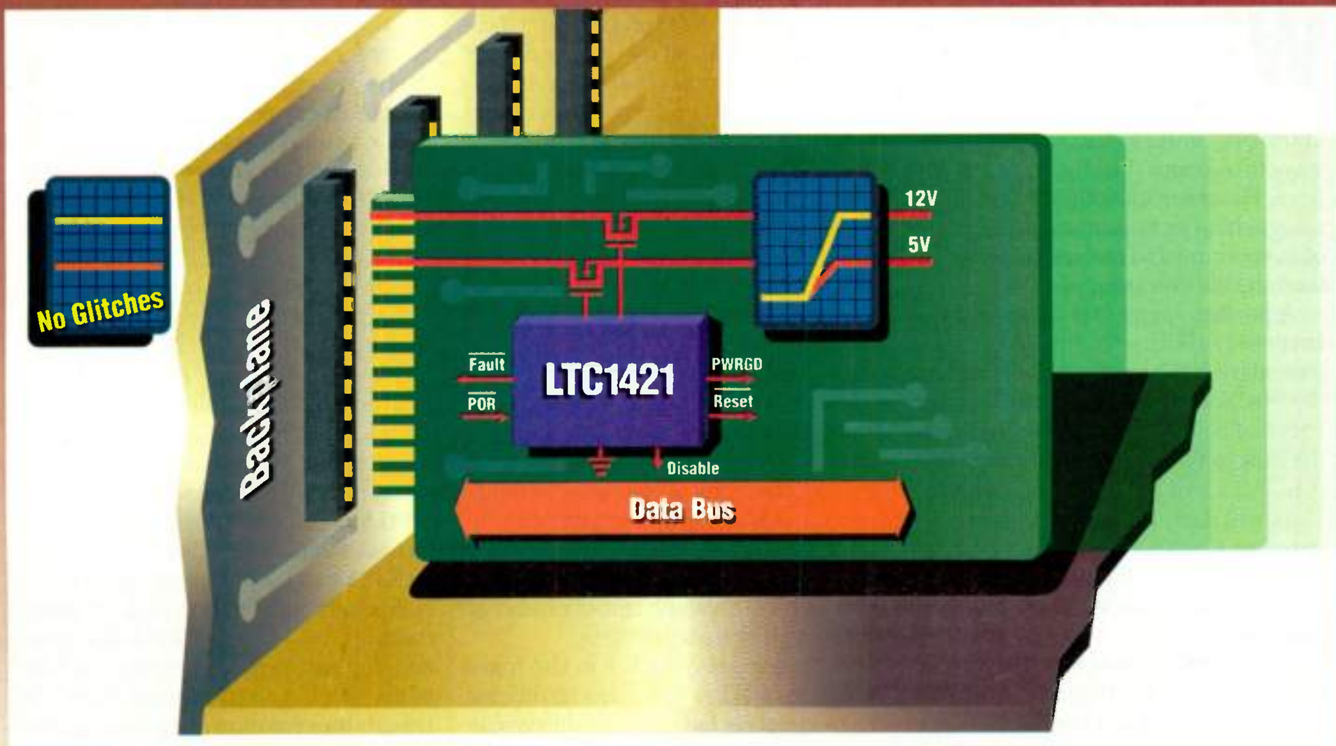
Today's system design cycle time is dominated by software and hardware/software interface issues. Through the use of virtual prototyping techniques, design teams can realize significant time savings by catching hardware/software interface bugs prior to building a physical prototype. Availability of a tool such as Seamless CVE has demonstrated that a practical architecture for implementing a virtual prototype environment is now possible. Co-verification using a virtual prototype allows these integration tasks to begin before the hardware prototype is built. Optimization algorithms allow large amounts of software to be verified in concert with the simulated hardware before a hardware prototype is built and debugged.

The key to success lies in the intelligent kernel that enables the engineer to optimize performance and accuracy while maintaining synchronization between software and logic simulation. While hardware/software co-verification is only one component of a larger overall hardware/software co-design methodology, it's a crucial component that leverages existing verification tools and techniques to provide practical value for current designs.

Serge Leef is the Director of Engineering for Mentor Graphics' Co-Design Business Unit. He has been with Mentor Graphics for seven years and has been responsible for many simulation programs including Seamless CVE. Prior to Mentor Graphics, Serge worked on EDA tools and technologies at Silicon Graphics and Intel. Serge holds a BSEE and a MSCS from Arizona State University, Tempe.

How Valuable	Circle
Highly	537
Moderately	538
Slightly	539

Hot Swap Safely!



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Features

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EDA WATCH ON WINDOWS NT

What Will It Take For Electronic Design To Shift To Windows NT?

We've all seen the projections. In just a matter of time, the EDA market will shift to Windows NT, making Unix expendable. We all know that shifts of this magnitude always take longer than the "experts" believe. However, once they begin, technology shifts pick up an amazing amount of momentum and change things more than anyone ever imagined.

A perfect example is the rise of the Internet; another is the dominance gained by EDA workstations back in the '80s. So, is the EDA industry on the verge of a new growth era, driven by the shift to Windows NT? I predict that it is. And while I don't believe that Unix will die (although it will be relegated to niche applications), I do believe the vast majority of electronics designers will make Windows NT their platform of choice.

Recent Dataquest studies project that the market for Windows NT EDA products will grow at a compound annual rate of over 90% between 1995 and 2000. Dataquest predicts that during the next three years most mainstream engineering departments will shift to NT.

But the big question is: When will design engineering groups move en masse from Unix to NT? Here are my thoughts.

Change Can Be Difficult

The main reason we have not yet seen the mass migration is fairly obvious. Windows NT is relatively new, and most people resist new technology simply because change can be painful. Shifting to a new design platform causes pain for many companies because of their large investments in existing equipment, infrastructure, customization, training, and legacy designs. It is usually companies with less invested in the "old way of doing things" that first adopt new technologies. For them, the costs and pain of the status quo are more intense than the pain of adopting new technologies.

EDA suppliers must streamline the shift to NT to make it easier for the engineering enterprise. I think a perceived lack of tools to promote and facilitate the transition has been another barrier to the mass migration to NT. Suppliers must address the common needs of mainstream designers, and deliver NT solutions (not just point tools) that deliver superior value.

So far, there has been a dearth of support for legacy designs. The coexistence of Unix and NT will be a near-term requirement for many engineering groups, so Windows NT EDA solutions must be compatible with existing design environments. EDA vendors often recommend a wholesale replacement of existing design environments. This works for some groups, but many others want to retain certain tools or legacy designs that continue to be efficient. They want vendor support for this transition environment, along with the smooth transfer to NT of the remaining legacy designs.

Another delay factor in the mass adoption of NT is that some traditional EDA suppliers have a vested interest in maintaining the status quo. Their prices and business models were justifiable for the more expensive Unix platform. Now, Microsoft and Intel have shown it's possible to deliver more value at a lower cost, and mainstream EDA customers expect the same from their suppliers. After all, the primary reasons for shifting to Windows NT are to improve productivity and reduce costs.

So, what kinds of engineering enterprises have moved to EDA on NT? The first to make the shift were fast-growing companies of small to medium size. In the past, these companies may have run out of steam with PC-based EDA, and were forced to move to Unix. With the advent of more powerful Intel PCs running Windows NT, they had a high-value, cost-effective alternative. Also now moving to NT are large engineering organizations motivated by the sheer value the platform delivers. The price for sustaining Unix EDA caused them to look at alternatives and investigate the productivity and cost benefits of an NT-based design enterprise. They discovered they could buy new NT platforms and new design tools for less than the cost of renewing their maintenance agreements on the older software. The decision to change was easy when the return on investment (ROI) was calculated and compared.

Will It Work For Me?

Now many might ask if Windows NT is for everyone. Well, if you design deep-submicron ICs or systems-on-silicon, perform software-hardware co-design or behavioral synthesis, or, use chip design services, you will probably find it best to stay with Unix. However, most engineers are not involved in those areas of design. Pc-board system design is ideal for the NT platform.

To satisfy the needs of the design majority and enable the shift to NT, EDA vendors should deliver an integrated suite of tools for pc-board, FPGA, and CPLD design. They should make VHDL-based design easier and more affordable. They should integrate FPGA and CPLD design tools right into the board design flow.

EDA companies should automate component information management, making it easy to select and reuse parts and eliminate errors when creating bills of material. And they should provide translators for migrating schematics designs to and from Unix EDA systems. By delivering these capabilities at affordable prices, vendors would give the majority of electronic design groups all the reasons they need to move to NT.

These new NT-based EDA solutions are now coming to market from OrCAD and others. I join Dataquest in predicting that the majority of design engineering enterprises will standardize on Windows NT in the next few years. After all, what company doesn't want to save money, increase productivity, and reduce pain?

Contributed by Jim Plymale, vice president of marketing at OrCAD. He holds a BS in electrical engineering from Portland State University. For more information on this or related topics, contact OrCAD at (503) 671-9500, or see the company's web page at http://www.orcad.com. Direct all e-mail to info@orcad.com.

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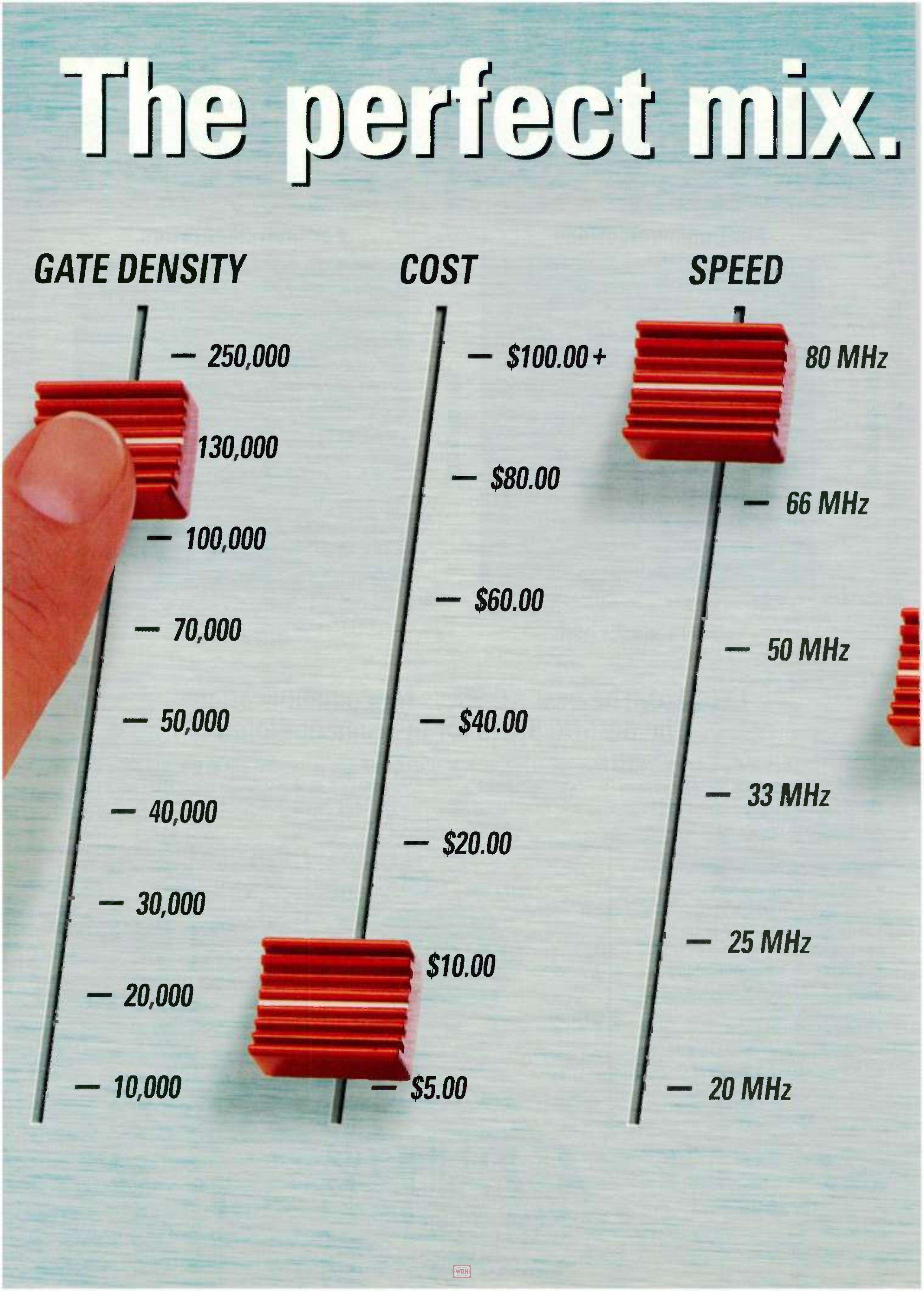
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$5.00
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66 MHz
50 MHz
33 MHz
25 MHz
20 MHz

Expert EMI/EMC Detection Possible With Front-End Software Tool

Detecting and correcting EMI/EMC (electromagnetic interference/electromagnetic compatibility) problems early in the life of a design has become essential due to stricter governmental standards and a growing public awareness. These trouble spots, which are easy to fix early on, could cause devastating results later in the design cycle.

Viewlogic Systems has now found a viable solution to early detection: Its QUIETExpert EMI analysis tool not only locates problems, but also provides advice on how to fix them in complex pc boards. Problems identified by the tool include high-speed clock noise coupled to I/O lines, or virtual antennas created as a result of connector placement.

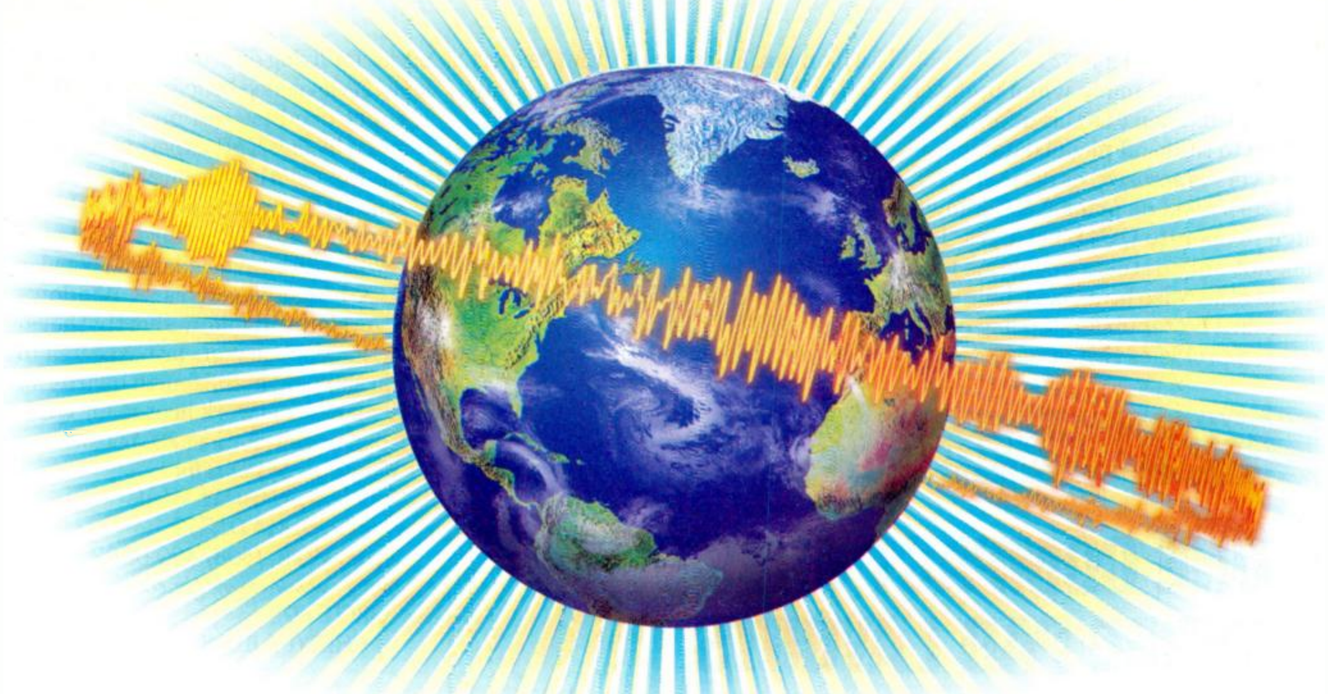
Developed with the help of EMI experts from the University of Missouri in Rolla, QUIETExpert uses the company's proven pc-board extraction technology to automatically extract board, part, and net information from the user's native layout tool. With EMC experts in short supply, the QUIETExpert tool can act as the software version of an expert in the review of a pc-board design database.

Featuring an advanced analysis engine and using rules-based criteria, QUIETExpert works to quickly uncover EMI/EMC problems. During operation, a menu guides users through product setup and pc-board database importing. With an intuitive user interface analysis, setup time can be minimized by providing simple forms for model input and net classification.

Design analysis begins immediately after database import using built-in default model parameters and DRCs. When a problem is detected, a board trace with all culprit components highlighted are graphically displayed for the designer's review. The user then simply scrolls through each problem, viewing a description and advice on potential fixes. The advice is based upon common practice and custom rules written by the user's own in-house EMC experts. The board layout can be simultaneously viewed at problem locations. All results are presented in a spreadsheet format, sorted according to radiation/susceptibility level and EMI mechanism.

QUIETExpert is simple to operate. In fact, the EMI/EMC detection analysis can be performed immediately with default model parameters and built-in DRCs. The Default DRCs may be edited or customized according to the user's needs. New DRCs may created to meet site-specific requirements or to optimize the product for individual company rules. With the spreadsheet-style model entry system, new models can be entered directly from standard datasheet sources. A complete library or databook of models is entered, and *(continued on page 80)*

FIELD PROGRAMMABLE ANALOG ARRAYS



It's an Analog World.

But for Digital System Designers We've Made it Easier to Live In.

For digital system designers making do in an analog world, life can often become, well…a real rat's nest. But with Motorola's new family of Field Programmable Analog Arrays (FPAA), the industry's first true analog counterpart to Field Programmable Gate Arrays (FPGA), digital designers can now create custom analog IC designs with the same flexibility as a digital FPGA.

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Motorola's FPAA architecture provides flexible arrays of analog building blocks, which can be configured and interconnected by software to create circuit functions that solve real-world signal processing problems. When used with supporting CAD tools, FPAAs enable analog IC designs with low risk and minimum design expertise.

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The MPAA020 FPAA is available in Development System Evaluation Kit #MPAA3DS that includes an evaluation board with a component breadboard area, user's manual, PC interface cable, and power supply. Plus a CD-ROM containing Motorola's EasyAnalog interactive design tool.

Ready to start enjoying the flexibility previously limited to digital programmable semiconductors? Then Motorola's new FPAA family is for you. For more information visit our website at http://sps.motorola.com/fpaa.

The Future of Programmable Technology is Motorola.

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PRODUCT FEATURE

(continued from page 78)
changes can be made when updates are needed. Then this this information is used to trade off model data investment versus accuracy as desired.

Users need no prior EMC knowledge to operate QUIETExpert. The tool not only detects problems that would otherwise be missed, but users can gain a better understanding of the types of problems that arise and ways to fix them. For the EMI/EMC expert, QUIETExpert offers some benefit by helping to more quickly identify difficult problems, such as traces over buried ground plan gaps. In addition, the tool can build a reduced-size pc-board database containing only the nets found to have EMI problems. Used with Viewlogic's EMI design and analysis tool QUIET, the database helps develop detailed engineering what-if scenarios for fixing difficult radiation problems. As an added benefit, the QUIETExpert product can be easily customized by any EMI expert to serve as an up-front EMI screening process.

The QUIETExpert tool, which will begin shipping in the third quarter of this year, will be available on all popular UNIX-based platforms. A Windows NT version will follow shortly thereafter. Production units are expected to begin shipping in the fourth quarter of this year. A network license for QUIETExpert sells for just $30,000.

Viewlogic Systems Inc.
293 Boston Post Rd. West
Marlboro, MA 01752
Karen Wells, (508) 480-0882
http://www.viewlogic.com
CIRCLE 492
CHERYL AJLUNI

HDL Tool Allows ASIC Architectural Analysis

Many of today's ASIC designers are having to bunch as much analysis at the front-end of a design as conceivably possible. This is virtually the only way to preempt costly bugs and the associated redesigns later in the design cycle. One area of front-end analysis that has sparked some interest is the ability to do architectural exploration. After all, what designer wouldn't relish the opportunity to examine the trade-offs associated with different possible architectures before committing to one? Not only would this save potential headaches later in the design cycle, but it would ensure that the designer, is starting with an optimized architecture.

While many would welcome this scenario, it hasn't been practical with the currently available tools. Traditionally, the designer only has time to try one architecture because it can literally takes weeks to write the necessary synthesizable RTL. By the time this much effort has been invested, the designer has already committed to the architecture and can't turn back. The trick, though, is to find the best optimized architecture up front that meets all of the constraints of a given specification.

Thanks to an interactive architectural exploration tool using a behav-
(continued on page 84)

(continued from page 80)
ioral-level hardware description language (HDL) known as Monet, such analysis is possible. The tool allows designers to quickly analyze architectural trade-offs up front in their design cycle, reducing development costs and time to market. In addition, because it allows feasibility and design to be captured together, the ASIC specification and documentation can be formally created in a manner that's easily understandable.

Monet works by automatically generating synthesizable RTL code from a specification for use with standard synthesis tools. The specification can be entered using any desired mix of behavioral, RTL, and structural VHDL. The results of the exploration are available in real-time in a VHDL output format, making it easy to simulate, generate test benches, or easily integrate with other analysis and synthesis tools.

If and when the designer's requirements change or if a different architectural approach is warranted, the designer simply makes the changes to the specification or constraints. Monet automatically produces code for each alternative architecture. Because Monet works on both single or multiple design processes, multiple alternative architectures can be easily tracked. Consequently, the designer can gradually refine virtually thousands of constraints to get an optimized architecture for a specification. So, even if the designer doesn't initially know what he wants, it's still possible to work down to one optimal architecture.

The Monet architectural exploration tool is based on the use of proprietary algorithms for behavioral scheduling and allocation. These algorithms make it possible for Monet to achieve over 10 times the performance and capacity of more conventional tools. This means designers now can analyze the results of architectural trade-offs in a matter of seconds instead of hours or days. Also, the additional capacity means that large portions of the design can be processed simultaneously. By comparison, previous tools put strict limitations on the number of operations that could be computed in a process. With Monet, there's no requirement for the design to be strictly partitioned into tiny parts; instead they can be partitioned into natural-sized pieces.

Monet offers an interactive environment in which design data is quickly visualized and interpreted. To help with the visualization, Monet provides access to interactive Gantt diagrams, state transition diagrams, and datapath block diagrams, all with cross-probing back to the behavioral specification. This capability can be used to analyze and compare architectural alternatives, and can add or modify constraints to control exploration results.

The Monet tool is available now and runs on either a Sun or HP UNIX workstation. A single floating license sells for $95,000.

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PRODUCT FEATURE

Verification Tool Targets Deep-Submicron And Systems-On-A-Chip Designers

Bearing fruit from a contract awarded back in June 1996 to develop a chip hierarchical design system (CHDS) for 0.25 µm and below, Synopsys now offers a static timing analysis tool known as PrimeTime. The tool is one of the core elements in a timing-driven design tool suite (being delivered to Sematech by Synopsys) as part of the CHDS contract. This full-chip gate-level tool is specifically intended to support the needs of systems on a chip (SoC) designers working with deep submicron (DSM), 0.25 µm and below, design geometries.

At these process geometries, the design environment begins to change. Interconnect delays start to dominate gate delays and the parasitics of the design components play a crucial role in the overall design. Couple this with complexity and capacity issues arising from the migration toward SoC and you end up with a rather difficult design environment. All of this culminates in a dramatic increase in design size and complexity that's beyond the limits of capacity of conventional verification tools. With million-gate SoC designs soon to become the norm, the industry is forced to reexamine current verification solution product offerings.

The PrimeTime tool offers a solution to this industry outcry. In fact, with both a fast execution time and low memory usage, it can provide the performance and capacity for multiple analysis runs of million gate ASICs in a single day. As opposed to current gate-level simulation, it is orders of magnitude faster. Also, its exhaustive coverage of timing-critical paths and advanced modeling features for SoC designs allow it to handle today's Intellectual Property (IP) cores.

To help designers easily transition to these tools , it was designed as a plug-in to existing synthesis-based ASIC and structured custom design flows, and accepts the same libraries and database formats as the company's Design Compiler tool. It also uses the same delay calculation subsystem and shares the same timing algorithm that ensures timing consistency. PrimeTime employs standard interfaces such as standard delay format (SDF).

Intended for mostly synchronous designs, such as in applications that include DSPs, telecommunications, and networking, the tool can be used for full-chip static timing analysis and static sign-off, or with event-driven simulation. As a result, designers can expect a whole host of benefits, ranging from faster time to market and more accuracy, to a complete verification.

With PrimeTime's graphical visualization capability, designers can actually see the results of the analysis.

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Thus, diagnosing timing problems becomes easier and quicker. To help increase designer productivity, the tool also can produce customized reports.

Another interesting feature is its advanced analysis capabilities, which enable it to handle, for example, complex clocking schemes that include support of designs with multiple clocks/phases, internally generated clocks, and gated clocks. A highly accurate block building and modeling capability provide full chip analysis, rather than just the synthesized portions.

Central to this modeling capability is a language developed by the company known as Stamp. This language makes it possible to accurately model complex custom-design blocks such as RAM and processors. PrimeTime also features timing model extraction that automatically creates high-level models from gate-level netlists. This boosts productivity in bottom-up design flows.

The PrimeTime static timing analysis tool is now available on UNIX workstations, and is fully qualified for sign-off by leading ASIC vendors including NEC, SGS-Thomson Microelectronics, and Texas Instruments. The tool sells for $35,000.

Synopsys Inc.
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Mountain View, CA 94043
(415) 962-5000
http://www.synopsys.com/
CIRCLE 494
CHERYL AJLUNI

Cycle-Based Simulator Addresses Functional Verification Challenge

Cobra, a new high-performance cycle-based simulator (CBS) from Cadence Design Systems, offers a combination of leading-edge cycle simulation performance with the ability to co-simulate hardware description language (HDL) models and system models. Coupled with the company's NC-Verilog event-based simulator, users can leverage the benefits of both cycle based and event-driven simulation in one unified verification flow.

Originally developed at the Cadence Berkeley Labs (CBL) advanced research center, the Cobra simulator is significant in that it addresses one crucial piece of the functional verification puzzle: how to handle the capacity issues of deep submicron systems on a chip designs in a timely fashion. The problem is that in this type of design environment, the amount of simulation needed to verify a design can be quite sizable. And there are few options.

Even if you try to utilize some of the other verification technologies currently on the market, there's no way to avoid having to simulate huge parts of the design. And doing this task within tight time-to-market schedules can be next to impossible.

(continued on page 90)

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Oki Semiconductor

PRODUCT FEATURE

(continued from page 88)

Using a high-speed simulator can provide a measure of relief. That's where the Cobra simulator steps in, with its high performance capacity and high speed capabilities. In fact, Cobra is specifically targeted toward applications that require significant speed, such as video, network switching, and microprocessor design.

At the heart of the Cobra cycle-based simulator lies the company's multi-value decision diagram (MDD) technology. The MDD algorithm effectively works by representing Boolean logic as a series of logical trees. It then replaces the combinatorial logic with lookup tables designated as multiple decision diagrams, improving simulation efficiency. This provides the simulator with the performance required to handle multi-million-gate capacity designs with anywhere from 30 to 100 times faster run times than today's event-driven simulators.

The Cobra simulator shares the company's SimVision front-end, and will initially offer support for Verilog HDL-based design. Support for VHDL is expected to follow shortly in 1998.

During operation, a single Verilog-based compiler targets the design to either the Cobra cycle-based simulator or the NC-Verilog event-driven simulator. This ensures both the accuracy and speed of the simulation process. To debug the design, the designer can either run NC-Verilog, which provides a more detailed simulation, or Cobra, which offers longer regression runs but an overall reduction in the time it takes to verify the design.

As compared to other cycle-based simulators on the market, Cobra can provide support for mixed behavioral-, register transfer-, and gate-level designs, as opposed to just a synthesizable subset of the Verilog hardware description language (HDL). This feature will become even more crucial as the industry migrates toward a functional block-based design environment in which any number of Intellectual Property (IP) cores is standard. Cobra offers a solution here by enabling high-speed simulation of new logic with reusable IP models.

The Cobra cycle-based simulator supports a wide array of industry standards, such as OMI (Open Modeling Interface) and the programmable logic interface (PLI 1.0). It also offers support for the new PLI 2.0 standard for simulation control and external models.

The Cobra simulator is currently in production use at a number of customer sites. It will become available in volume shipments in December 1997. A single floating license will sell for $60,000. The simulator tool runs on all Sun Microsystems, Solaris and Hewlett-Packard Unix-based workstation platforms.

Cadence Design Systems Inc.
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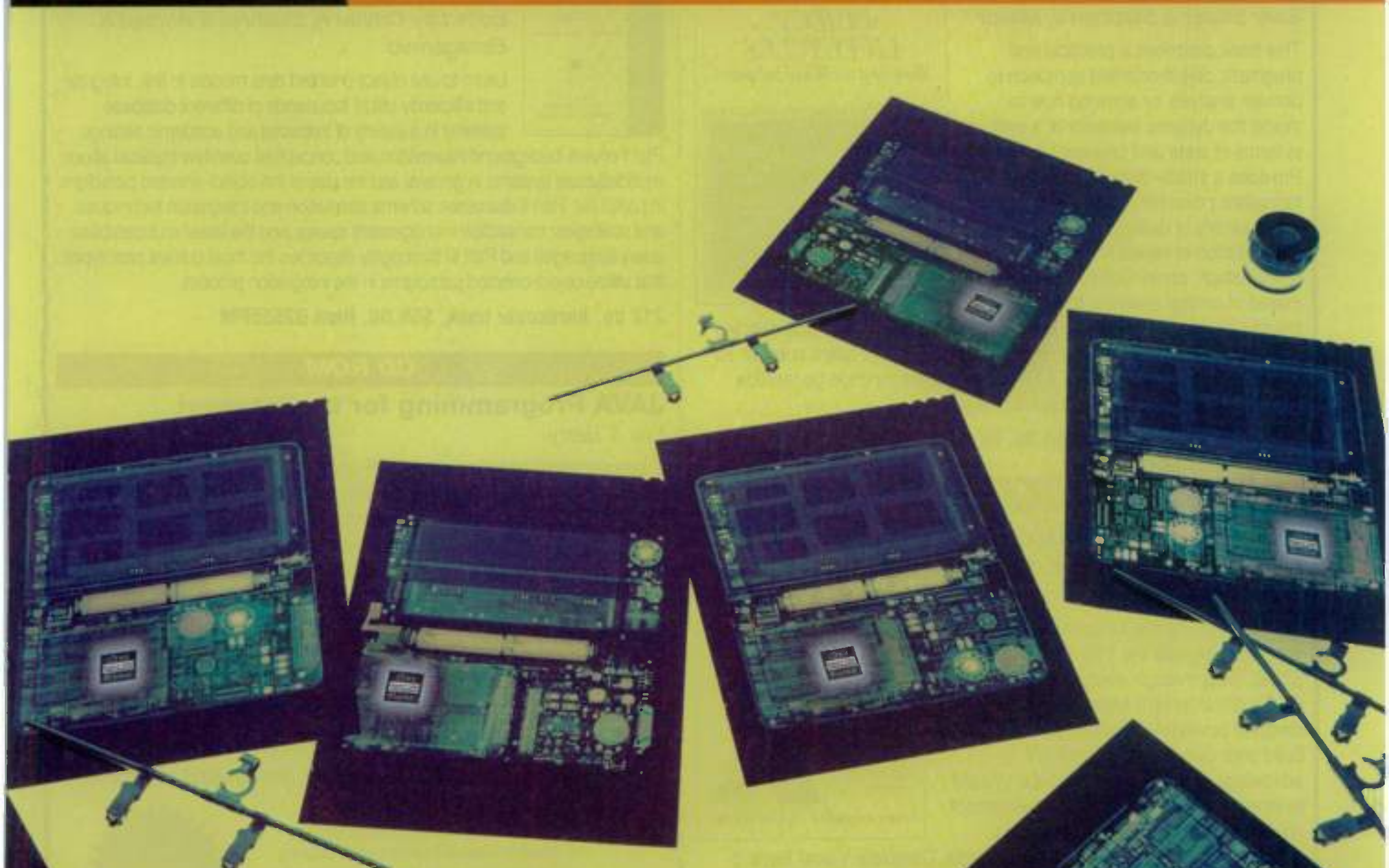
Five out of seven Windows® CE Handheld PCs share the same inside secret.



The Hitachi SuperH™ RISC Cool Engine™. The de facto standard for Windows CE Handheld Personal Computers.

The electronics revolution is headed off the desktop and out into the world at large. Case in point: the Windows CE Handheld Personal Computer (H/PC).

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Over a thousand SuperH designs have proven our capabilities to help OEMs reduce their development time. The SuperH family boasts extensive third-party support and a whole host of middleware.

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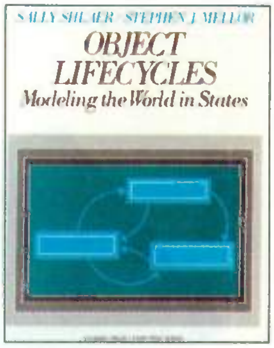
Book

Object Lifecycles Modeling the World in States

Sally Shlaer & Stephen J. Mellor



This book describes a practical and pragmatic object-oriented approach to domain analysis by showing how to model the dynamic behavior of a system in terms of state and process models. Provides a strictly defined, multi-level formalism powerful enough to be mapped into a variety of designs; techniques for formalization of object lifecycles, dynamic relationships, contention problems, and thread of control analysis; and a ready-to-use tailoring of 2167A's analysis DID's, with justification and detailed instructions for compliance. Includes language-independent notation for Object-Oriented Design (OODLE) and strategies for code generation from OOA models using Recursive Design.

251 pp, softcover book, $45.00, Item B2547PM

Books & CD ROMs

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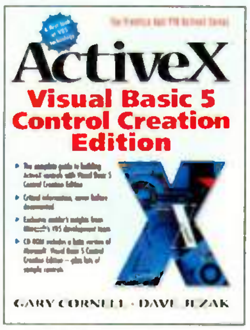
Gary Cornell & Dave Jezak

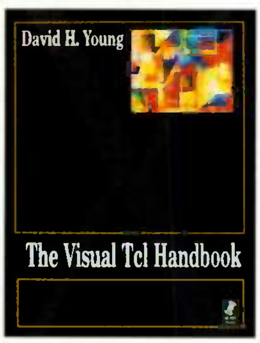


Start by learning the fundamentals of programming with the VB5 Control Edition (CCE), walk through every element of the CCE's development environment, and discover powerful templates you can use to build your own controls. Take full advantage of the Control Interface Wizard to streamline ActiveX control development and learn proven methods for testing, debugging, and deploying ActiveX controls. Complete Visual Basic 5 Control Creation Edition on CD-ROM along with ready-to-use sample controls. Allows experienced programmers to master many of the new technologies used in the full version of Visual Basic 5.

516 pp, softcover book & CD, $39.95, Item BC2847PM

The Visual Tcl Handbook

David H. Young



Organized into four parts, this text focuses on examples of the most commonly used commands with explanations that put the commands in a practical context. The introduction demonstrates state-of-the-art scripting using Tcl's architecture; the following overview highlights TclX commands; Visual Tcl discusses widget-building commands, callbacks and design strategy, and concludes with command pages of references for Tcl, TclX, Vt and Vx. Features example code and user interface design topics driven by real-world UNIX administration tasks. The accompanying CD contains the complete SCO Visual Tcl 1.0 run-time and development environments.

502 pp, softcover book & CD, $45.00, Item BC2842PM

Book

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Edited by Omran A. Bukhres & Ahmed K. Elmagarmid

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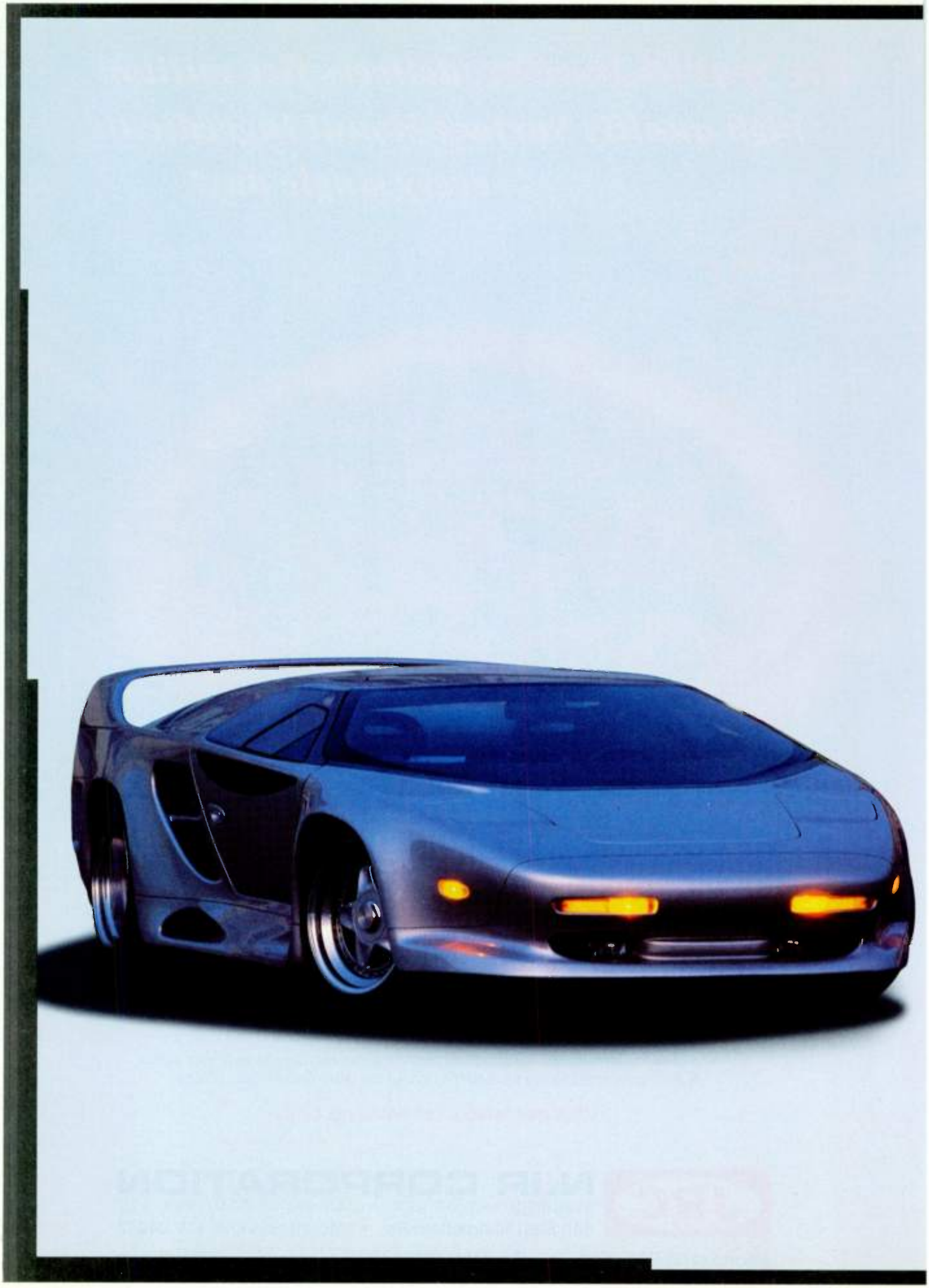

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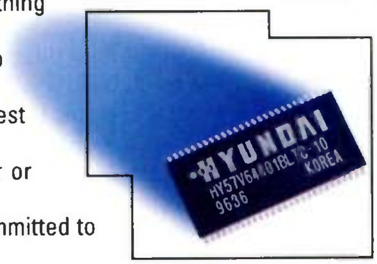

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8M x 8 EDO	3.3V	50/60/70 ns	4K/8K
4M x 16 EDO	3.3V	50/60/70 ns	4K/8K
16M x 4 Sync.	3.3V	66/83/100MHz	4K/8K
8M x 8 Sync.	3.3V	66/83/100MHz	4K/8K
4M x 16 Sync.	3.3V	66/83/100MHz	4K/8K

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Co-Verification Handles More Complex Embedded Systems

New Techniques Give Hardware And Software Designers Greater Visibility Of The Internal Workings Of Increasingly Complex Embedded Systems.

ARNOLD S. BERGER, Applied Microsystems Corp., 5020 148th Ave. N.E., Redmond, WA 98073-9702; (800) 426-3925.

The trend toward moving increasing amounts of embedded system complexity to ASIC devices has had a significant effect on the use of the classic in-circuit emulator (ICE). The problem is reduced visibility into the system's operation as designers hide more of the system functionality from the embedded software and bus-level trace views of the system. To address the issue of internal visibility, new techniques are being developed to blend the capabilities of the traditional ICE with the functionality of an HDL simulator. By combining these tools with the appropriate interface software, a very unique and powerful design methodology is created.

Since its introduction in the late 1970's, ICE has been the tool-of-choice for embedded system debugging and hardware-software integration. Many engineers have developed a love-hate relationship with the ICE. Those "ICE boxes" were often cranky and difficult to use, but no one would argue with the high degree of functionality and visibility that an ICE brought to embedded system development. By tightly integrating microprocessor run control, memory overlay, and real-time trace, the ICE uniquely addresses the needs of embedded system developers.

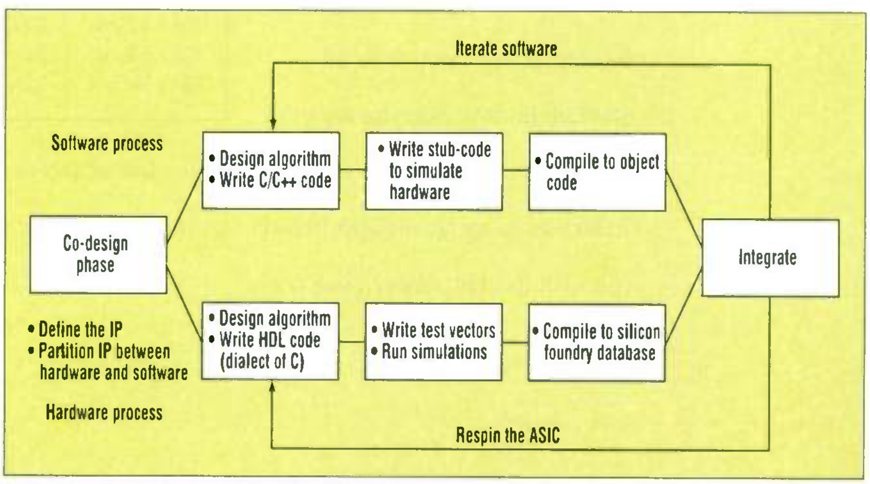
A Software-Centric View

However, the ICE takes a very software-centric view of the world. It is designed to address the flow of code and data on the microprocessor bus, up to the bus pins of the peripheral control circuitry. What goes on beyond those pins is invisible to an ICE. This state of affairs was acceptable when the only devices that shared the microprocessor bus were other commercially produced standard parts, such as UARTs, LANs, parallel I/Os, and serial I/Os. Since these peripheral devices were very well-specified and well-characterized, the uncertainty associated with the hardware-software interface was greatly diminished. The only untried and untested element was the code, and the ICE was well-positioned to control that.

Advances in ASIC technology have affected this central role of the ICE. However, the ICE, in combination with other tools, can continue to play a role in hardware-software integration, even if some of the hardware exists only as a representation in a hardware description language (HDL) simulator.

How Things Changed

As the cost and difficulty in designing custom integrated circuits dropped, the attractiveness of placing more of the value of an embedded system into an ASIC grew. As a result, designers get to the situation where they can generalize the concept of the algorithm to a combination of hardware and software. (Intellectual property is often used synonymously with algorithms.) It is the algorithm that solves the problem and adds the value to the product. For example, the algorithm may be an ASIC device and software for



1. Beyond the co-design phase, the differences between the design processes for hardware (in this case, an ASIC design using HDL-based tools) and software are disappearing.

LINEAR TECHNOLOGY DESIGN NOTES

1µA Op Amp Permits Precision Portable Circuitry – Design Note 163

Mitchell Lee and Jim Williams

A new dual op amp with only 1µA power consumption and precision DC specifications permits high performance portable applications. The LT®1495 has 375µV offset, 2µV/°C drift, 1nA bias current and 100dB of open-loop gain. These attributes, combined with careful design, make portable, high performance circuitry possible.

5.5µA, 0.05µV/°C Chopped Amplifier

Figure 1 shows a chopped amplifier requiring only 5.5µA supply current. Offset voltage is 5µV, with 0.05µV/°C drift. Gain exceeding 10^8 affords high accuracy, even at large closed-loop gains.

Micropower comparators C1A and C1B form a biphase 5Hz clock. The clock drives the input-related switches, causing an amplitude modulated version of the DC input to appear at A1A's input. AC-coupled A1A takes a gain of 1000, presenting its output to a switched demodulator similar to the aforementioned modulator.

The demodulator output, a reconstructed, DC amplified version of the circuit's input, feeds DC gain stage A1B. A1B's output is fed back, via gain setting resistors, to the input modulator, closing a feedback loop around the entire amplifier. Amplifier gain is set by the feedback resistor's ratio, in this case 1000.

The circuit's internal AC coupling prevents A1's DC characteristics from influencing overall DC performance, accounting for the extremely low offset errors noted.

The desired micropower operation and A1's bandwidth dictate the 5Hz clock rate. As such, resultant overall bandwidth is *low*. Full power bandwidth is 0.05Hz with a slew rate of about 1V/s. Clock related noise, about 5µV, can be reduced by increasing C_{COMP}, with commensurate bandwidth reduction.

0.03% Linear V/F Converter with 13µA Power Drain

Figure 2's voltage-to-frequency converter takes full advantage of the LT1495's low power consumption. A 0V to 2.5V input produces a 0Hz to 10kHz output, with 0.03% linearity, 250ppm/°C drift and 10ppm/V supply rejection. Maximum current consumption is only 13µA, 200 times lower than currently available ICs. Comparator C1 switches a charge pump comprising D1, D2 and the 100pF capacitor to maintain its negative input at 0V. A1 and associated components form a temperature compensating reference for the charge

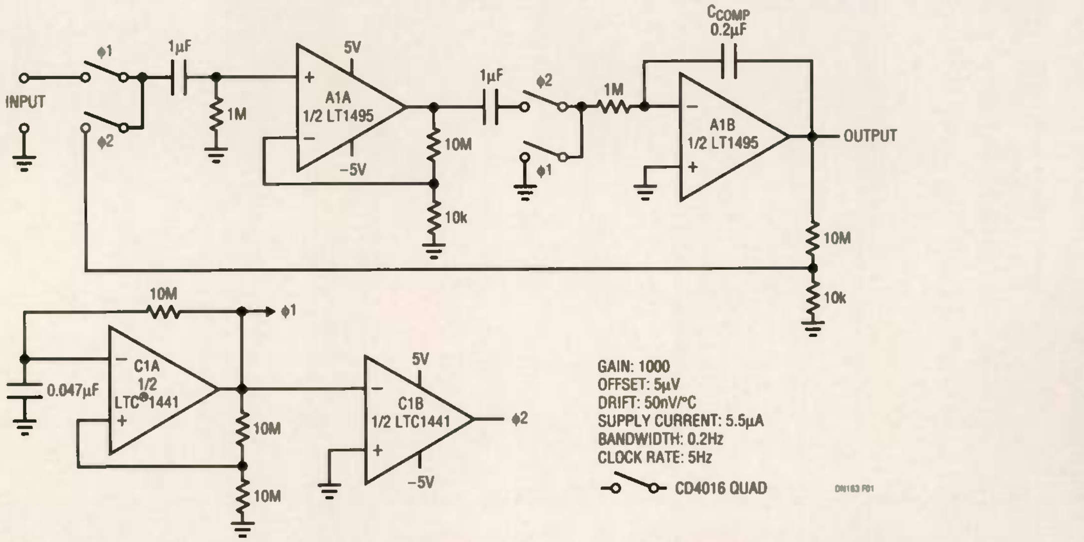


Figure 1. 0.05µV/°C Chopped Amplifier Consumes 5.5µA Supply Current

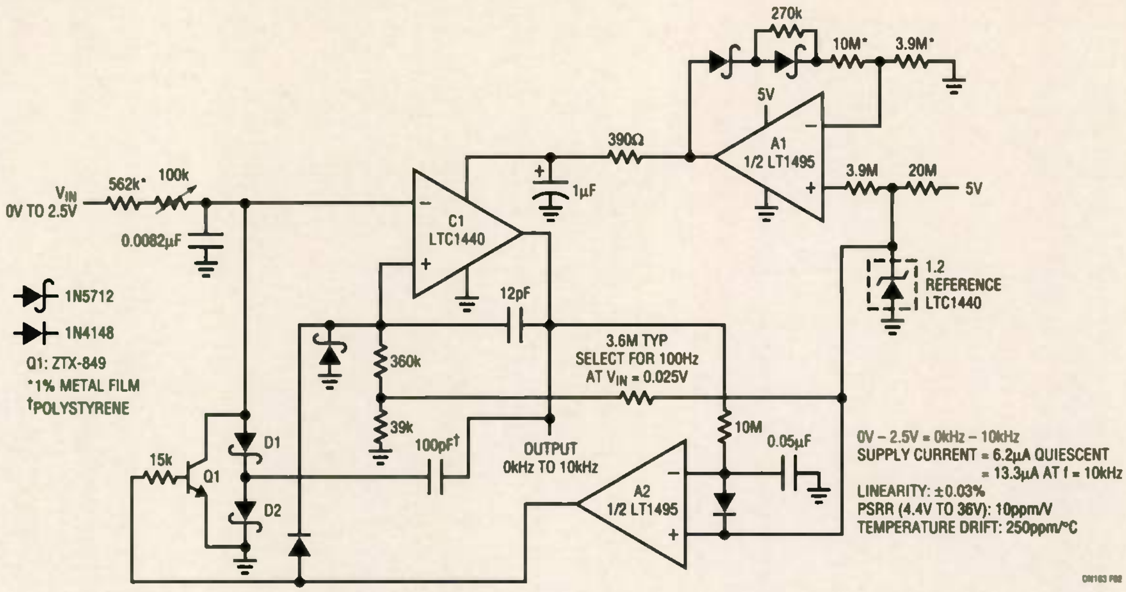


Figure 2. 0kHz to 10kHz Voltage to Frequency Converter Consumes Only 13μA

ump. The 100pF capacitor charges to a fixed voltage; hence, he switching repetition rate is the circuit's only degree of reedom to maintain feedback. Comparator C1 pumps uniorm packets of charge to its negative input at a repetition ate precisely proportional to the input voltage derived curent. This action ensures that circuit output frequency is trictly and solely determined by the input voltage.

tart-up or input overdrive can cause the circuit's C-coupled feedback to latch. If this occurs, C1's output oes low; A2, detecting this via the 10M/0.05μF lag, goes igh. This lifts C1's positive input and grounds the negative nput with Q1, initiating normal circuit action.

ortable Reference

 final circuit is Figure 3's unique portable reference, which raws only 16μA from a pair of AAA alkaline cells. Battery ife is five years—equivalent to shelf life.

wo outputs are provided: a buffered, 1.5V voltage output nd a regulated 1.5μA current source. The current source ompliance ranges from approximately 1V to –43V.

he LT1634A reference is self-biased, completely eliminatng line regulation as a concern. Start-up is guaranteed by he LT1495 op amp, whose output initially saturates at 11mV rom the negative rail. The 1μA current output is derived from fraction of the reference voltage impressed across R3.

ote that the portable reference's current output can be ulled well below common, limited only by Q1's 45V reakdown. The 1.5V output can source or sink up to 00μA and is current limited to protect batteries in case of short circuit.

Once it is powered, there is no reason to turn the circuit off. One AAA alkaline contains 1200mAH capacity, enough to power the circuit through the five year shelf life of the battery.

The voltage output accuracy is about 0.17% and the current output accuracy is about 1.2%. Trim R1 to calibrate voltage (0.1%/kΩ) and R3 to calibrate the output current (0.4%/kΩ).

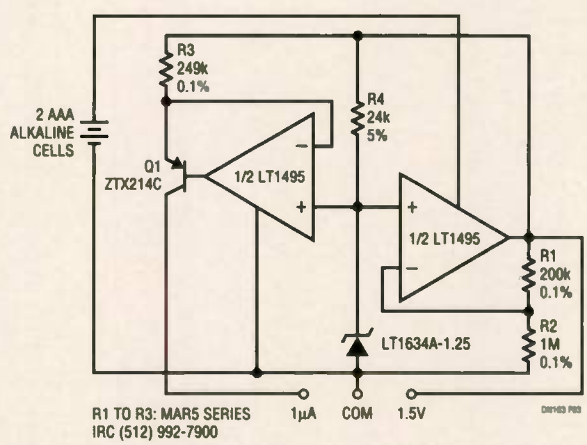


Figure 3. Portable Reference Operates Five Years on One Pair of AAA Cells

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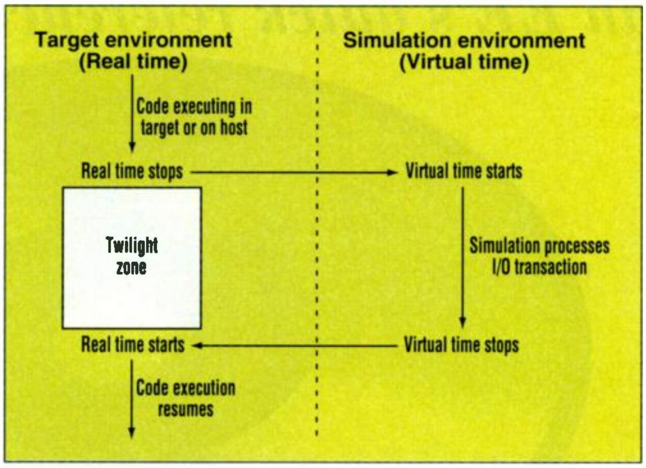
The trade-offs are easy to see. The ASIC provides speed, because it solves the algorithm in a specific manner, so it achieves performance rates that a generalized microprocessor can't duplicate. However, it cannot be reprogrammed the way a microprocessor can. (FPGAs are not part of this discussion.) The ASIC part of the algorithm is almost always more costly, since it's a physical device, than a software implementation, although RAM and ROM also adds to cost.



2. When accesses stop in the real target system and time transfers to simulation, servicing of real-time interrupts can be a problem.

Co-Design

The process of taking the algorithm and partitioning it between the ASIC device (fast, costly, and inflexible) and the code executing in the microprocessor is often referred to as co-design. The co-design effort takes place at the system design level and at the system architecture level. This is where design trade-off decisions are being made about partitioning the algorithm between the hardware and the software.

Today, once the co-design decisions are made, the processes by which hardware and software is designed are amazingly similar *(Fig. 1)*. The software designer creates algorithms and data structures that control the processor and the ASIC and process the data stream. The programs are typically written in C or C++ languages. The hardware designer follows essentially the same process, using the C-like languages of Verilog or VHDL.

Where their methods diverge is when their compiled code is ready to be used. In one case, the code compiles to object code so that it can become a memory image for the microprocessor to execute. In the other case, the code is the source file for a foundry's design database. In other words, it gets compiled to real silicon.

There are several obvious messages here:

• In today's environment, there are more similarities than differences in the hardware and software design processes.

• If they are so similar, why is there often separation between the design teams?

• Two unknowns have been added to challenge the designer. One is the hardware-software interface, which is no longer a stable, well-defined, and well-understood boundary. The other is the correctness of the algorithm represented by the new hardware itself.

Thus, it is now apparent that the value of the ICE as the linchpin tool is diminished because it can no longer provide visibility in a very significant part of the overall system software, which now encompasses embedded C or C++ code and embedded Verilog or VHDL code.

Mixing ICEs And Simulators

Once designers accept the premise that the hardware and software processes are fundamentally the same, the tool requirements can be looked at in the same way. Designers must be able to debug all of the code (C, C++, Verilog, VHDL) in a way that ensures visibility all of the time. If the key metric in embedded systems design and debug is "time-to-insight," or the time it takes to comprehend the behavior of this complex, real-time driven environment, then designers must maximize their ability to see into both code spaces at the same time.

Hardware simulators are driven by test vectors. A designer creates, manually or by automated methods, sets of vectors that represent on a clock-by-clock basis, the state of all inputs to the design. The response of the simulated design (the output of the ASIC) is compared with the expected behavior of the system.

The testing of an ASIC and verifying its functionality can be extremely labor intensive. About half the total time spent developing an ASIC is actually design work, while the rest of the effort is devoted to functional verification and developing test vectors for the silicon foundry to use in manufacturing test. Even with this effort, only about half the ASICs work is correctly in-circuit the first time.

Improve Efficiency

Clearly, there was a need to improve the efficiency of this process. Several companies have introduced similar tools that attempt to address this problem from different angles. The general architectural flow is to create a translation and communications software package that takes software instructions as its input and turns those variables into test vectors that are compatible with HDL simulators.

For example, Viewlogic Corp.'s EAGLEi automatically creates test vectors for a simulator from C or C++ code executing natively on the host computer. Special library functions replace the memory or I/O calls that would be used in the actual target system *(see code listings a and b)*. Remote procedure calls (RPCs) link the executing user's program on the workstation to the Eagle software, called a Virtual Product Console (VPC).

What if designers could use an ICE in a real target system with these co-verification tools? Suppose that the ICE could somehow recognize when the actual processor was attempting to access the ASIC device as if the ASIC actually existed. Could the emulator become the bridge that we've been looking for? Several advantages come to mind im-

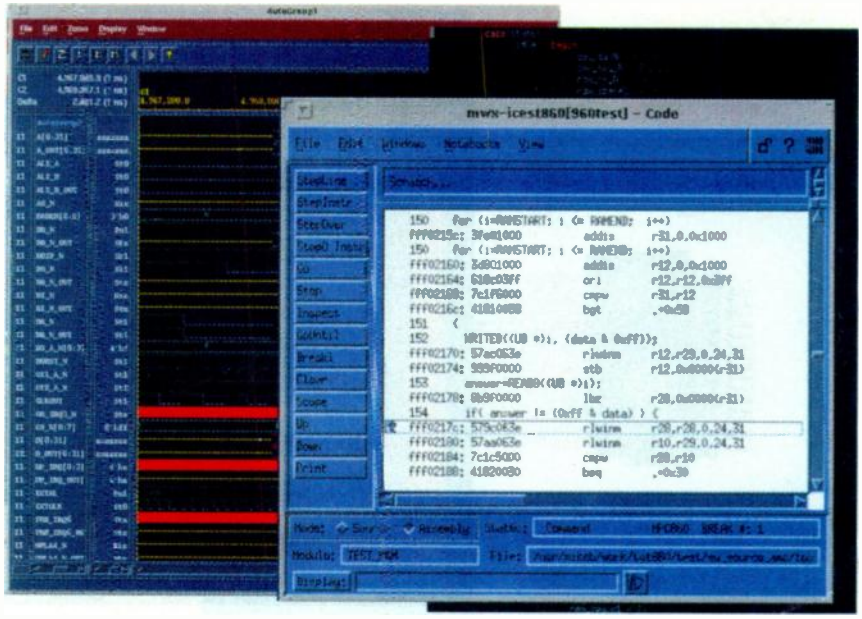
mediately:

•The actual code—C, C++, or assembly language—could be used without changing. This is extremely important if legacy code is involved.

•The actual processor would provide the stimuli and response, so processor behavior would be correct at all times.

•The emulator could provide a real time trace of all actual system activity, bus level or source level, and the simulator could provide the complementary trace information for the ASIC's internal hardware design.

•Designers would have absolute control of the target microprocessor. The emulator's unique claim is that it can absolutely rein in an out-of-control microprocessor. Thus, the emulator, through its ability to provide processor run control, gives designers overall system control and observability.



3. These results from an interactive hardware and software debugging session show a waveform view from the VCS simulator (left window), the Verilog source window from the VCS simulator (right background), and the results from the MWX-ICE debugger (foreground).

Emulator Modification

These compelling advantages led to an effort to modify a generic 68040 emulator for that purpose. The effort was successful as a proof-of-concept experiment, but several technical and customer-satisfaction issues required an alternative solution.

The end result was a device called the VSP-TAP (Virtual Software Processor-Target Access Probe). It works with an emulator or microprocessor, but it is a wholly separate device. It sits between the processor and the target system, much like a preprocessor module for a logic analyzer. The VSP-TAP monitors the activity on the pins of the microprocessor and detects when virtual accesses or interrupts are occurring. It then puts the processor in a wait state and sends the pin information to the simulation, which is running concurrently on the host computer. The interface software sends back an acknowledgment of the transaction. If the transaction is a write, the processor is released and code execution continues as before. If the transaction is a read operation, the VSP-TAP must continue to hold the processor in a wait state until the results of the read are available. This could be on the order of milliseconds or days, depending upon the complexity of the simulation.

Developing the virtual/real system around emulation-independent hardware allows the designer to put together different types of co-verification environments. For example, with a VSP-TAP and an emulator connected to the target, the emulator provides the run control, trace, and overlay memory, while the VSP-TAP supplies the virtual/real interface and the communications with the simulation running on the host. Another arrangement can use the VSP-TAP in a system in which the processor itself is used, with no ICE. The debugger would reside on a host computer, and a remote debug kernel would run in the target system. A ROM emulator could act as a LAN communications device for the debugger, but it is not necessary if a separate serial channel is available.

It is important to remember that most emulators expect that they can always regain control of the microprocessor. The assumption is that if a bus cycle hangs or aborts and the processor goes "into the weeds," the emulation circuitry can bring it back into the emulation control mode. This is significant because often when the processor is under emulation control, such as single-stepping or pausing-execution flow, it is running a real program at real speed. The program just happens to come from the emulator's control system background memory, not the target system's memory or the emulator's overlay memory.

However, many emulators will monitor certain pins of the processor, looking for state changes on these pins. If the ICE does not detect activity on these pins within a certain time period, it will attempt to assert control over the processor by generating an NMI or RESET to the processor. Unfortunately, this will ruin the program flow since the processor is not hung-up because of a defect, but is simply suspended in an extended bus cycle, waiting for the simulation to return a value.

This problem can be difficult to detect because the time-out generators are not standardized, nor are they tightly controlled. Typically, an RC circuit is used for this purpose, so one time it might time-out at 104 ms and another time at 97 ms. Also, differing amounts of LAN traffic could easily force a simulation to fail on one occasion and not on another.

This condition also is true for a debug kernel. Most debuggers use some kind of time-out mechanism to allow them to regain control of the processor. If this circuit times out due to an extended wait state, then simulation results will be erratic.

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Consequently, for a co-verification and debug environment to exist, the debug tools must be aware that the microprocessor will exhibit unanticipated behavior. In this case, very long wait states on some bus cycles.

A second issue involves the number of processors used. Some emulators use two devices: A control processor manages the overall emulation circuitry, and an emulation processor (often called a bond-out) does the actual emulation. Some emulators, however, employ one processor to both emulate the target processor and control the emulation communications with the host computer. These instruments would be at a disadvantage if the user could not control the emulator for periods of time while the processor was being waiting for a simulation transaction to complete. Consequently, emulators that use a single processor are unsuitable for use with simulation environments.

Another potential problem is more general and goes to the very core of the use model for real-time and virtual-time interfacing. What happens when a virtual transaction begins and real time stops, then vice versa? The answer is that real time and virtual time cannot overlap *(Fig. 2)*.

This means that the user cannot assume that real-time events will be properly serviced all of the time in a mixed real and virtual environment. The VSP-TAP, for example, is basically a passive device until a virtual access is detected. Then, it acts to extend the bus cycle of the processor until the virtual transaction occurs. Thus, any real-time target activity that is being controlled by the processor and monitored by the emulator can progress normally, and the emulator is an ideal tool for dealing with these interrupt-driven, real-time events. It is only when the real-time interrupts occur during the virtual accesses that problems arise.

These problems are potentially very serious. An example would be a watchdog timer generating a rest or an NMI after failing to be serviced. The key is that the designer must be aware of the operational mode of the target system and the emulator to insure that they are compatible with the notion of real time and virtual time not overlapping. There appears to be a need among users for a way to allow real time and virtual time to peacefully coexist, so work is being done on creating some form of overlapping time support.

A more subtle issue involves using an emulator to interface to a virtual target system to run real code against a virtual ASIC. This situation arises when the target hardware hasn't been completed but the software team wants to move ahead by exercising their code against the virtual ASIC. They decide to use the emulator as their target execution environment by running the code in the emulator's overlay memory. This provides all of the functionality, with the exception of target system stimuli, needed to execute real code against the virtual hardware.

However, many emulators do not drive pin activity to the bus during internal memory accesses. This would prevent the VSP-TAP from detecting the virtual accesses and the system would fail. This is especially true if the overlay memory mapper circuitry was not flexible enough to deal with small regions dedicated to ASIC interfacing.

Finally, the co-verification system must be reliable and robust. Simulations often run for long periods of time. Although the processor and target may run at full speed, the simulator—VHDL or Verilog—may run very slowly, perhaps only 10 to 100 clock cycles per second. And, since simulators are expensive programs, floating licenses are valuable corporate assets. As a result, a simulation may very well be set to run over a weekend. If it does run over the weekend and the target system locks up or the emulator glitches, there must be a mechanism in place that will at least keep track of the system state up to the failure point so that a record of what happened can be reviewed by the design team.

Since emulators are generally designed to be interactive in their use model and simulators are designed to run in a batch mode, this can be the source of incompatible behavior between the software-design environment and the hardware-design envi-

Code Listings

Listing a

```
void ramTest(unsigned int u32stAddr, unsigned int u32endAddr) {
   unsigned int u32addr, u32data, *p32data
   for (u32addr = u32stAddr; u32addr < u32endAddr; u32addr += 4)
      {
      u32data = ~u32addr;
      *(unsigned int *)u32addr = u32data;
      *p32data = *(unsigned int *)u32addr;
      if (*p32data != u32data) {
          /* error */
      }
    }
  }
```

Listing b

```
void ramTest(unsigned int u32stAddr, unsigned int u32endAddr) {
   unsigned int u32addr, u32data, *p32data
   for (u32addr = u32stAddr; u32addr < u32endAddr; u32addr += 4)
      {
      u32data = ~u32addr;
#ifdef EAGLE_VSPLINK
      vspMemWrite32(u32addr, u32data);
      vspMemRead32(u32addr,*p32data);
#else
      *(unsigned int *)u32addr = u32data;
      *p32data = *(unsigned int *)u32addr;
#endif
      if (*p32data != u32data) {
          /* error */
      }
    }
```

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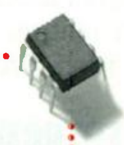

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The value of the hardware-software co-verification use model, with the emulation and simulation environments functioning in parallel, can be shown. It can be shown by examining an example problem from several different perspectives.

In the example, the application code and the ASIC are being designed and tested in parallel. After an overnight build of the software, the latest revision hangs up during accesses to a certain register within the ASIC. It isn't clear from examining the VHDL code and the C code where the problem lies.

The emulator is set to run until the hang-up occurs. The real-time trace captures the fact that the processor accesses the ASIC and the virtual ASIC returns a value, but the processor goes into an endless polling loop waiting for the ASIC to provide the proper signal. The target is restarted but this time the emulator stops code execution just prior to the virtual access. Once the emulator enters pause mode, the software designer single-steps the processor into the virtual access.

On the hardware side, the designer watches the test vector come across into the simulator and watches the ASIC simulation flow until the result vector is sent back to the interface. The vector comes back to the processor as a 32-bit data word, and the software designer sees that the bit position assigned for the status of that operation comes back as false, even though the hardware designer insisted that it was sent out as true.

A Clue To What's Going On

The last processor the hardware designer worked with was a Motorola 68030 and this design uses an Intel i960HX. Of course, it is the ever popular little-endian, big-endian mixup. The byte order was reversed because Motorola and Intel processors use different endian methods. Both designers—hardware and software—thought that they understood the specification, yet this was missed.

How each designer approaches the problem depends on his or her perspective. Suppose that the software designer is running in a mixed real and virtual target and the simulator is running on a different workstation located somewhere else, although they are joined via a common LAN. To the software designer, the virtual accesses appear the same as the real ones. The software designer sees data coming back from the ASIC and uses the emulator exactly as it was used in the past to debug the target.

In the same situation, the hardware designer sees test vectors coming into the simulator as if they were designed as actual test vectors, rather than operational code. The hardware designer can single-step, run to a source statement, look at an internal node, and do all of the operations that were previously done with a vector file. However, this time the vector generator is the real software. In a co-verification setup, the design team can display both the hardware and software debug environment on screen at the same time *(Fig. 3)*.

Obviously, the in-circuit emulator, a pre-eminent tool for hardware-software debug, can find new value as part of a hardware-software co-verification design and debug environment. But since this technology is still in its infancy, vendors are still discovering what the issues are for designers who adopt these techniques. One such issue is real-time operating systems (RTOSs). An RTOS, by its very nature, could become problematic in such an environment. However, with some simple extensions, RTOS/emulation/simulation compatibility should be rather straightforward to achieve.

Arnold S. Berger is director of the co-verification business unit at Applied Microsystems Corp., Redmond, Wash. He received his BS and PhD in Materials Science from Cornell University, Ithaca, NY.

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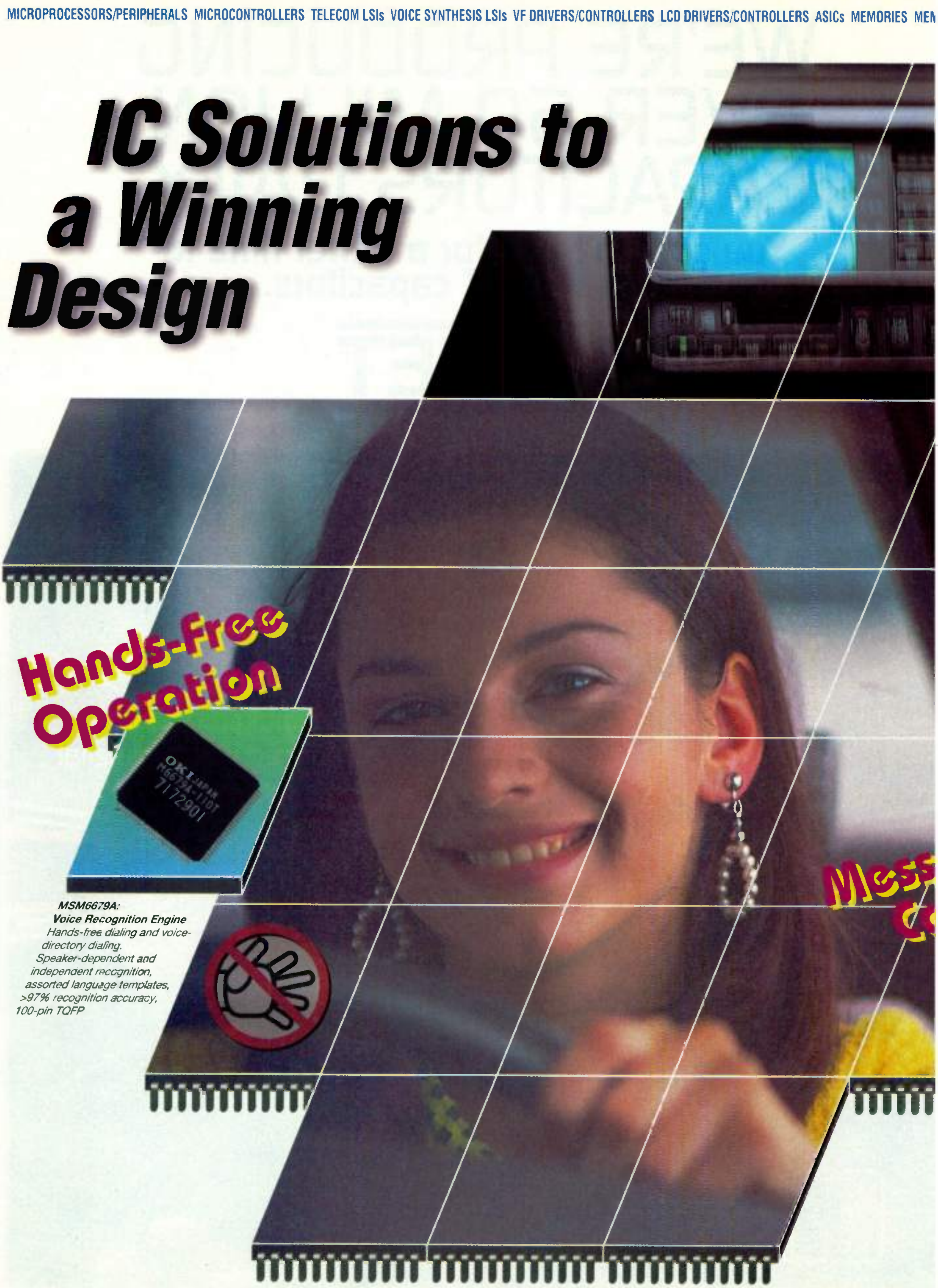

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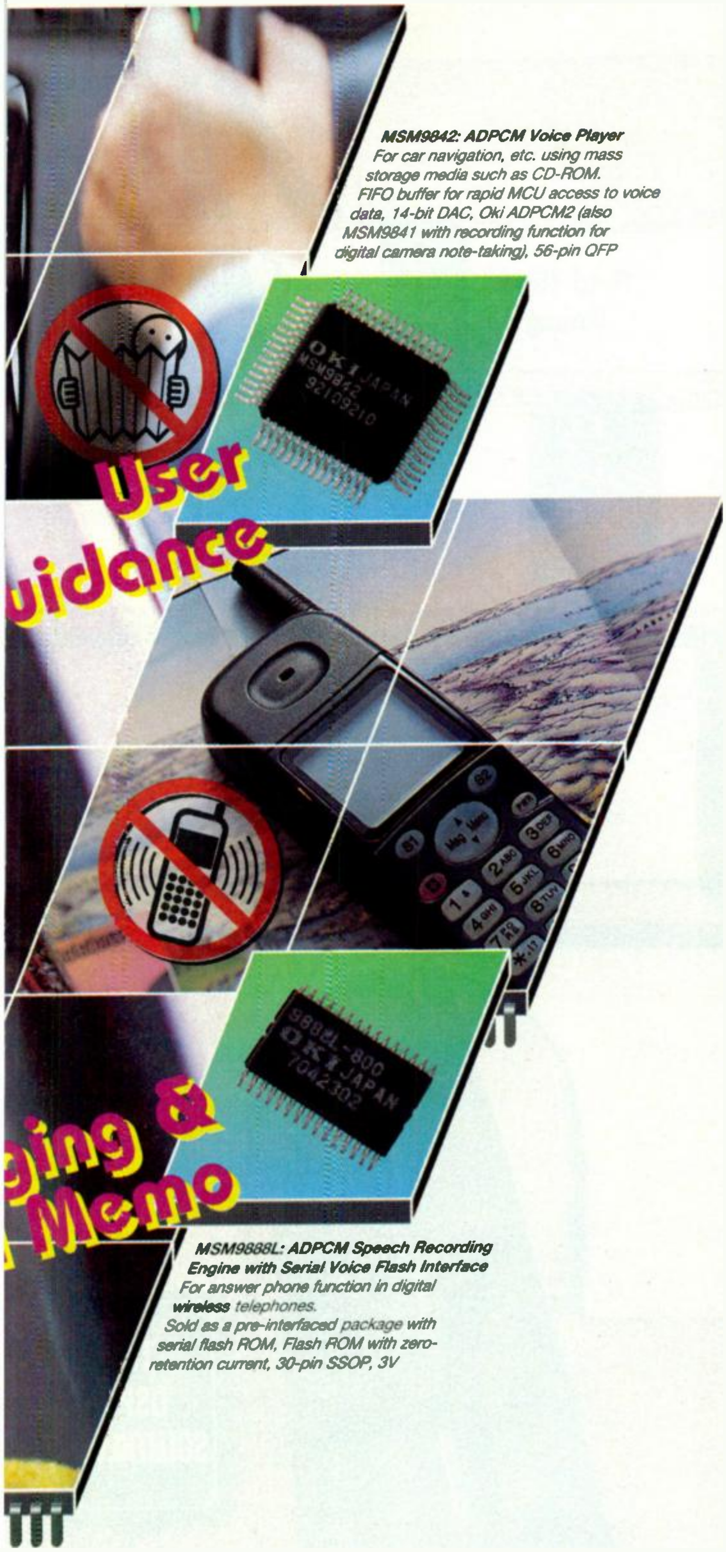

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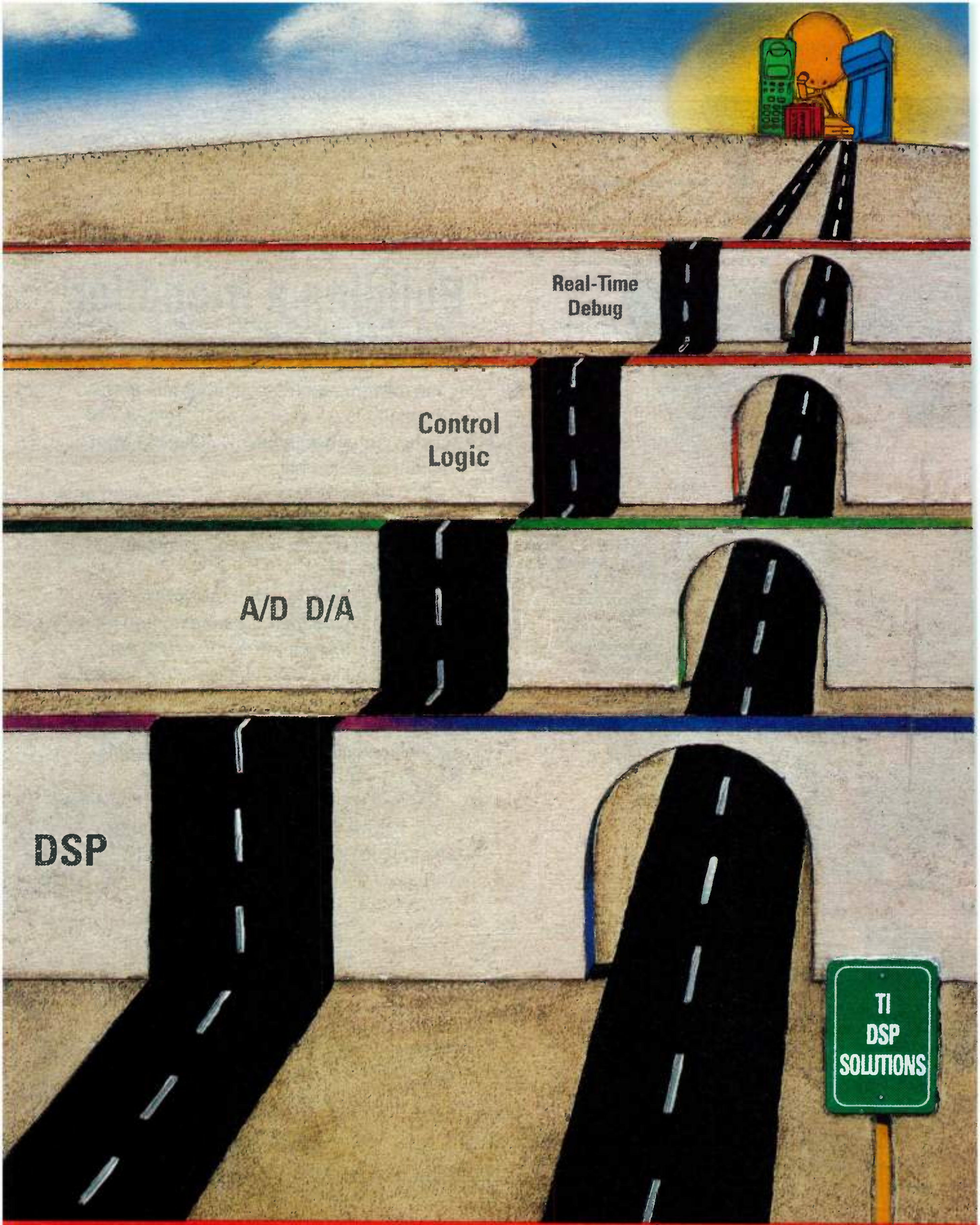

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80C186/188 Emulator Includes Software Performance Analysis

Aimed at embedded systems using the Intel 186/188 processors, the MP-186 in-circuit emulator offers a standard 32-kframe trace memory and extensive triggering. It comes with built-in software performance analysis, probe upgrades to support multiple processors, and a Windows-based source-level de-

bugger interface. Users can set up to eight complex bus events with four levels of triggering per event. Events can include any combination of address, data, external input signals, and status line activity with address ranges and inversion. Event triggers can be set or modified and trace data viewed on the fly. Performance analysis lets users measure timing and count history on various functions and modules to find potential code bottlenecks. A code coverage feature tests whether all areas of the code are executed. The emulator supports Intel 80C186/188 XL/EA, EB, and EC processors and their AMD equivalents. The MP-186 is available immediately. A system with a 32k trace, 1-Mbyte overlay memory, and target adapter costs $7495. A 128k trace is optional.

Microtek International, 3300 N.W. 211th Ter., Hillsboro, OR 97124-7136; (800) 886-7333; (503) 645-7333; e-mail: info@micrtotekintl.com; Internet: http://www.microtekintl.com. CIRCLE 496

Emulator Adds Support For 68HC12 (B32)

The MIME-800 emulator now supports Motorola's 68HC12 (B32) 16-bit microcontroller, which is designed for high-volume automotive use and safety, industrial control, wireless communications, and consumer applications. The instrument can function in a standalone mode as a software development engine (SDE), or an emulator probe can be added for full access to target hardware. Up to 5 Mbytes of memory is available on the SDE mode and 2 Mbytes of emulation memory on the probe, with further expansion possible. Other features include support for a range of target hardware architectures, the Code Coverage Plus function to test code fully for illegal or dangerous program actions, and Ethernet connectivity for remote access and downloading of code. A Windows-based front end allows a choice of PCs or Sun host computers. A dynamic link library allows easy integration with third-party tools, including C- and task-level debuggers, and the Coderight Workbench provides seamless integration of source editor, compiler, linker, and debugger. The MIME-800 is priced at $15,000.

Pentica Systems Inc., 19A Crosby Drive, Bedford, MA 01730; (617) 275-4419; fax (617) 275-6514; Internet: http://www.pentica.com. CIRCLE 497

PC-Based Emulator Handles 8x930AX, 8x930HX Systems

With the addition of the POD-930AX-12 and POD-930HX-12 boards, the EMUL251-PC emulator supports Intel's 8x930AX and 8x930HX universal serial bus architecture. The emulator board plugs into an IBM PC/XT/AT bus, and the pod boards, which plug into the target system, connect to the emulator through a 5-ft. cable. For workstation users, the emulator's LanIce version is available. For laptop use, the instrument comes in a PCMCIA card (without support for trace and shadow RAM). The emulator uses a special emulation ver-

sion of the devices and supports binary and source mode, plus all other programmable modes. An optional 128-ktrace board features advanced trace functions with sophisticated triggering. The board can be viewed, programmed, and retriggered on-the-fly without disturbing program execution. A Windows-based user interface supports symbolic assembly and high-level C debugging for popular C compilers. The POD-930AX-12 and POD-930HX-12 are available now for $3495 each. Emulator boards start at $995. The trace board costs $4295.

Nohau Corp., 51 East Campbell Avenue, Campbell, CA 95008-2053; (408) 866-1820; (408) 378-7869; e-mail: sales@nohau.com; Internet: http://www.nohau.com. CIRCLE 498

Test And Debug Connectors Aid Circuit Designers

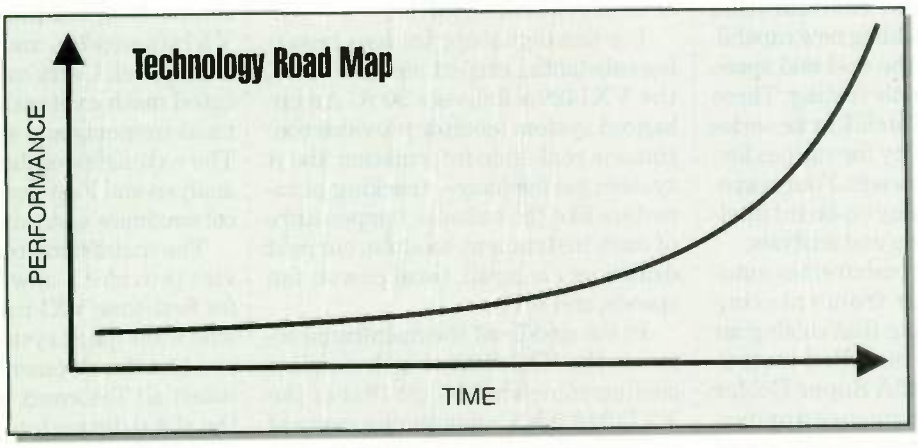
A new line of interconnection solutions is aimed at developers of systems using advanced circuit packages. Some of the tools are used for connecting test equipment like emulators and logic analyzers to various package types, including BGA, PQFP, TSOP, and other advanced types. Other tools are used to wirewrap prototype circuits in the customary 0.1-in. environment. The products include prototyping boards, adapters to connect circuits together in high-density packages, test clips, probes, various socket adapters, and device programming adapters. Call for specific requirements and prices.

Emulation Solutions, 422 Ives Terrace, Sunnyvale, CA 94087; (408) 745-1524; fax (408) 745-1526; e-mail: gabor@adapters.com. CIRCLE 499

Connection Solutions Ease Testing of BGAs, TSOPs

Two new interconnect solutions make testing of devices in BGAs and TSOPs easier. The BGA Socket and Probing System offers fast, reliable, easy-to-install connection with optimum signal integrity. It's based on an elastomeric connector array in the same configuration as the BGA package footprint. This minimizes trace lengths and adapter height, improving high-speed performance. Lead inductance is less than 2 nH. The TSOP Clip, typically used in flash memory applications, supports 28-to-56-pin packages with a wide variety of probing applications. The low-profile design and directionally conductive elastomeric connectors allow testing of ICs spaced as close as 0.030 in. The clip will remain connected even at a vertical angle. The BGA Socket and Probing System costs $1800. The TSOP Clip costs $450.

Emulation Technology Inc., 2344 Walsh Ave., Bldg. 4, Santa Clara, CA 95051-1303; (408) 982-0660; (408) 982-0664. CIRCLE 500 providing the information that helps the system designer walk the line between leading edge and bleeding edge, *Electronic Design* helps the engineer get a more competitive product to market, faster.



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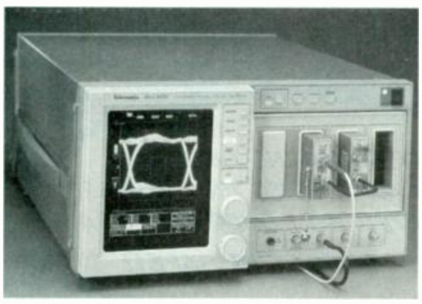
Comm Analyzer Characterizes High-Bandwidth Signals

The CSA803C communication signal analyzer features nine new communications masks, an improved error-free trigger, and a new prescaler trigger. The instrument offers a 50-GHz bandwidth, four channels, triggering to 12.5 GHz, a 10-fs sampling interval, and a



35-ps reflected rise-time time-domain reflectometer. The new masks include optical, electrical, and Gigabit Ethernet versions. The enhanced trigger has a trigger metastability of less than 0.01 ppm, making it ideal for working with

itoring of digital information. Two versions are available. The KPCMCIA-8AOU has eight unipolar outputs with a 0- to +5-V range. The KPCMCIA-8AOB has eight bipolar outputs with a ±5-V range. The cards support Windows 95 and come with the DAQWARE software package, which includes TestPoint driver software to interface with TestPoint Application Software. LabVIEW drivers are also available. The KPCMCIA-8AO costs $545.

Keithley Instruments Inc., 28775 Aurora Road, Cleveland, OH 44139-1891; (800) 552-1115; (216) 248-0400; fax (216) 248-6168; e-mail: product_info@keithley.com; Internet: http://www.keithley.com. **CIRCLE 502**

Network Spectrum Analyzer Enhanced For RF Testing

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The EMCPro is a combination electromagnetic compatibility immunity test system that meets or exceeds the requirements for CE marking as well as for testing to various other national and international standards. The instrument can be configured with two surge waveforms. In addition to the standard 1.2/50-µs combination wave required by IEC standards, an optional 10/700-µs telecom wave or 100-kHz ring wave can be added as an internal option. Its 6.6-kV surge test capability allows the unit to perform tests to ANSI C62.41 categories A and B, to the CCITT's full 5-kV limits, and to UL864's 6-kV level. EFT voltages to 4.4 kV ensure that users meet all existing EFT standards. Options include coupler/decouplers for 3-phase ac mains to 32 A, I/O and telecom line coupler/decouplers, a capacitive clamp, and an EFT attenuator. Call for prices and availability.

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PCI-Based Data-Acquisition Boards Use On-Board DSP To Free Up Host PC

The SmartDAQ family of analog PCI-bus data-acquisition boards features digital signal processors (DSPs) that perform memory and data-management tasks typically handled by the host PC. This leaves the host free to do application-critical jobs like data analysis and reporting. The on-board Motorola 56301 uses bus mastering to guarantee throughput by effectively controlling the transfer of information directly to computer memory via the computer's bus.

The first offering in the SmartDAQ family are eight boards in the KPCI-5000 series. Functions include 16 single-ended (eight differential) analog-to-digital channels or 64 single-ended (32 differential) analog-to-digital channels; two 12-bit digital-to-analog channels with waveform quality; three counter-timers; 16 digital I/O lines; and eight priority-interrupt driven digital inputs. Conversion rates available are 330 ksamples/s at 12 bits and 200 ksamples/s at 16 bits. A 1-kbyte FIFO buffer is expandable to 32 kbytes.

The DSP chip allows all analog-to-digital, digital-to-analog, digital I/O, and counter-timer operations to be performed simultaneously with no degradation of the board's aggregate sampling rate. All analog channels can be scanned at their specified frequencies, regardless of the number of channels in use. The processor is fully programmable. The boards support a wide array of software packages for Windows 95 and NT.

The KPCI-5000 will be available starting Sept. 30, priced from $1195 to $2295.

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VXI Mainframes and Analyzers Offer More Functions In Less Space

Two families of VXIbus products and a mainframe configuration service aim at adding new capabilities and reducing the cost and space required for electronic testing. Three mainframes in the IntelliFrame series offer cooling capability for various levels of performance needs. Four waveform analyzers employ on-board intelligence for processing and analysis.

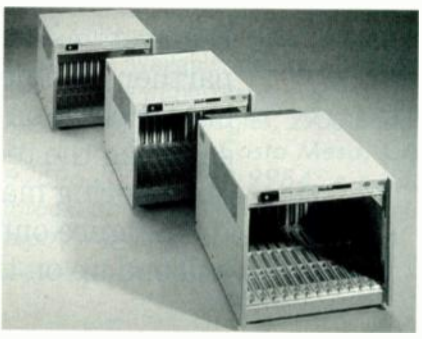
All three 13-slot mainframes automatically block air from entering empty slots, ensuring that cooling air is directed to the installed instruments. The VX1420A Super Cooler targets high-performance applications, where system density and power requirements demand the highest level of cooling. It offers closed-loop, slot-by-slot temperature monitoring and is programmable from either an internal or external controller. A quiet fan makes it suitable for benchtop use. In addition, a backplane shield helps control electromagnetic interference (EMI).

For fast digital applications requiring substantial current on the 5-V rail, the VX1420A delivers 90 A. An enhanced system monitor provides continuous real-time information about system performance, tracking parameters like the exhaust temperature of each instrument module, current drawn on each rail, total power, fan speeds, and so on.

In the middle of the mainframe series is the VX1410A, which supplies cooling somewhat below that of the VX1420A while maintaining many of the same features, including the enhanced system monitor, closed-loop cooling system, 90-A capability on the 5-V rail, and EMI shield. The front-panel display is available as an option. The VX1411A is the least expensive of the three mainframes. For quieter benchtop use, it employs variable speed fans based on the input ambient temperature and includes the backplane shielding. It's suitable for medium-performance test-system needs.

The lower-priced models are upgradable. Users can add additional cooling, programmability, and other features as test needs increase.

Four models make up the TVS600A series of waveform analyzers, which combine high-performance oscilloscope capabilities with extensive processing and analysis in a two-slot VXI module. The TVS621A and TVS641A have 250-MHz bandwidths and 1-Gsample/s digitizing rates, with two and four channels, respectively. The TVS625A and TVS645A offer a 1-GHz

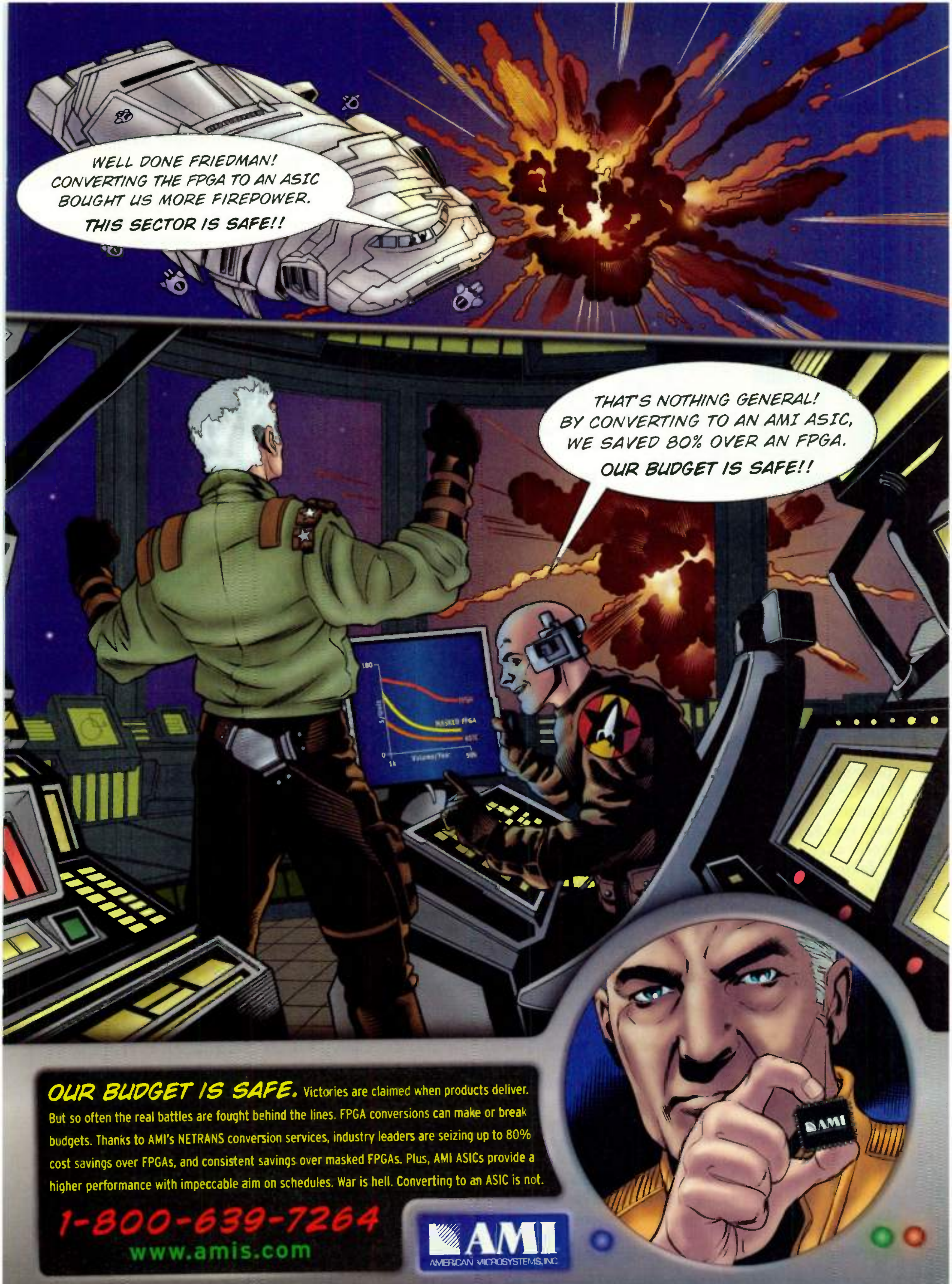


bandwidth and 5-Gsample/s digitizing, again with two channels and four channels, respectively. Record length is 15 kpoints.

Enhancements include template testing, zoned waveform measurements, statistics, measurement limit comparison, full-function drivers for VXI*plug&play*, and a versatile soft front panel. Users can define sophisticated math expressions that include measurements and signal processing. The extensive on-board DSP-based analysis and Fast Data Channel protocol maximize test throughput.

The mainframe configuration service provides a new level of support for first-time VXI users or customers who want quick system configuration and test development. Tektronix will insert all Tektronix instruments and the slot 0 device into the mainframe, load all drivers and soft front panels, set all jumper switches, and test the system to ensure operation.

The VX1420 mainframe costs $7995; the VX1410A, $6895; and the VX1411A, $5495. Delivery is in four weeks. The TVS621A waveform ana-
(continued on page 120)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Comm Analyzer Characterizes High-Bandwidth Signals

The CSA803C communication signal analyzer features nine new communications masks, an improved error-free trigger, and a new prescaler trigger. The instrument offers a 50-GHz bandwidth, four channels, triggering to 12.5 GHz, a 10-fs sampling interval, and a

35-ps reflected rise-time time-domain reflectometer. The new masks include optical, electrical, and Gigabit Ethernet versions. The enhanced trigger has a trigger metastability of less than 0.01 ppm, making it ideal for working with fast OC192 signals. It's bandwidth is dc to 4 GHz, and sensitivity is 50 mV. Jitter has been reduced to 1.1 ps RMS. The prescalar trigger extends the bandwidth to 12.5 GHz. The capabilities of the CSA803C also are being introduced in the 11801C digital sampling oscilloscope, which differs from the CSA803C by having up to 136 channels. The CSA803C and 11801C each cost $25,000 and are available 10 weeks after receipt of an order.

***Tektronix Measurement Business Div.**, P.O. Box 1520, Pittsfield, MA 01202; (800) 426-2200 (press 3, code 1027); fax (413) 448-8002.* **CIRCLE 501**

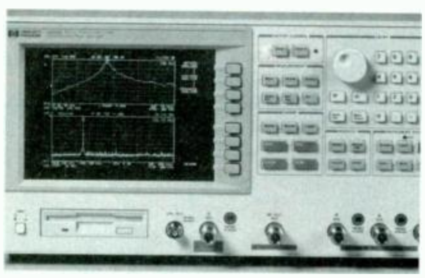
PCMCIA Card Supplies Eight 12-Bit Analog Outputs

The KPCMCIA-8AO, a 12-bit analog output card in the PCMCIA standard 2.1 form factor, can simultaneously update eight independent bipolar or unipolar analog outputs at 100 kHz. The card's on-board event timer allows it to interrupt the host PC's CPU at software-programmable intervals and generate waveform-quality outputs. Eight TTL-compatible digital I/O channels are software configurable and provide control or monitoring of digital information. Two versions are available. The KPCMCIA-8AOU has eight unipolar outputs with a 0- to +5-V range. The KPCMCIA-8AOB has eight bipolar outputs with a ±5-V range. The cards support Windows 95 and come with the DAQWARE software package, which includes TestPoint driver software to interface with TestPoint Application Software. LabVIEW drivers are also available. The KPCMCIA-8AO costs $545.

***Keithley Instruments Inc.**, 28775 Aurora Road, Cleveland, OH 44139-1891; (800) 552-1115; (216) 248-0400; fax (216) 248-6168; e-mail: product_info@keithley.com; Internet: http://www.keithley.com.* **CIRCLE 502**

Network Spectrum Analyzer Enhanced For RF Testing

The HP 4396B, a 1.8-GHz combination analyzer with network, spectrum, and optional impedance measurement functions, has been enhanced to simplify RF testing in the R&D lab as well as production. In spectrum-analysis mode, new digital-signal processing technology improves amplitude



accuracy and sweep speed, allowing the analyzer to sweep up to 100 times faster at narrow resolution bandwidth settings than units with analog technology. A new "list sweep" function helps locate low-level signals quickly. The HP Instrument-BASIC function is now a standard feature. This capability allows customized measurement, test sequences, process control, and data analysis. The HP 4396B network spectrum analyzer costs $30,600. The optional impedance measurement function is $995. Estimated delivery is in four weeks.

***Hewlett-Packard Co.**, Test and Measurement Org., P.O. Box 50637, Palo Alto, CA 94303-9512; (800) 452-4844, ext. 5401.* **CIRCLE 503**

EMC Immunity Tester Handles Multiple Standards

The EMCPro is a combination electromagnetic compatibility immunity test system that meets or exceeds the requirements for CE marking as well as for testing to various other national and international standards. The instrument can be configured with two surge waveforms. In addition to the standard 1.2/50-µs combination wave required by IEC standards, an optional 10/700-µs telecom wave or 100-kHz ring wave can be added as an internal option. Its 6.6-kV surge test capability allows the unit to perform tests to ANSI C62.41 categories A and B, to the CCITT's full 5-kV limits, and to UL864's 6-kV level. EFT voltages to 4.4 kV ensure that users meet all existing EFT standards. Options include coupler/decouplers for 3-phase ac mains to 32 A, I/O and telecom line coupler/decouplers, a capacitive clamp, and an EFT attenuator. Call for prices and availability.

***KeyTek**, 1 Lowell Research Center, Lowell, MA 01852-4345; (508) 275-0800; fax (508) 275-0850; Internet: http://www.thermovoltek.com.* **CIRCLE 504**

Anti-Aliasing Filter Gets Bandpass Option

A bandpass filter option is now available for the AAF-3, which is a multichannel, low-pass, anti-aliasing filter and amplifier board series for use in front of any analog-to-digital converter in ISA-bus-based data-acquisition systems. The bandpass characteristic results from adding high-pass filter sections to the existing low-pass sections. The maximum bandwidth is 100:1. That is, a filter with a lower cutoff frequency of 1 Hz can have a maximum upper cutoff of 100 Hz. Butterworth, Bessel, and Cauer elliptic filter characteristics provide adjustable center frequencies from 1 Hz lower cutoff to 50 kHz upper cutoff. The cutoff frequency can be controlled by any two of the on-board programmable sources and two external sources. Prices for the AAF-3 filter start at $1095. Volume discounts are available. Evaluation units are available within two weeks.

***Alligator Technologies**, 2900 Bristol St., Suite E-101, Costa Mesa, CA 92626; (714) 850-9984; e-mail: lbrooks@alligatortech.com.; Internet: http://www.alligator.com.* **CIRCLE 505**

PRODUCT FEATURE

PCI-Based Data-Acquisition Boards Use On-Board DSP To Free Up Host PC

The SmartDAQ family of analog PCI-bus data-acquisition boards features digital signal processors (DSPs) that perform memory and data-management tasks typically handled by the host PC. This leaves the host free to do application-critical jobs like data analysis and reporting. The on-board Motorola 56301 uses bus mastering to guarantee throughput by effectively controlling the transfer of information directly to computer memory via the computer's bus.

The first offering in the SmartDAQ family are eight boards in the KPCI-5000 series. Functions include 16 single-ended (eight differential) analog-to-digital channels or 64 single-ended (32 differential) analog-to-digital channels; two 12-bit digital-to-analog channels with waveform quality; three counter-timers; 16 digital I/O lines; and eight priority-interrupt driven digital inputs. Conversion rates available are 330 ksamples/s at 12 bits and 200 ksamples/s at 16 bits. A 1-kbyte FIFO buffer is expandable to 32 kbytes.

The DSP chip allows all analog-to-digital, digital-to-analog, digital I/O, and counter-timer operations to be performed simultaneously with no degradation of the board's aggregate sampling rate. All analog channels can be scanned at their specified frequencies, regardless of the number of channels in use. The processor is fully programmable. The boards support a wide array of software packages for Windows 95 and NT.

The KPCI-5000 will be available starting Sept. 30, priced from $1195 to $2295.

Keithley Instruments Inc.
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(888) 534-8453
(216) 248-0400
fax (216) 248-6168
product_info@keithley.com
http://www.keithley.com
CIRCLE 506
JOHN NOVELLINO

VXI Mainframes and Analyzers Offer More Functions In Less Space

Two families of VXIbus products and a mainframe configuration service aim at adding new capabilities and reducing the cost and space required for electronic testing. Three mainframes in the IntelliFrame series offer cooling capability for various levels of performance needs. Four waveform analyzers employ on-board intelligence for processing and analysis.

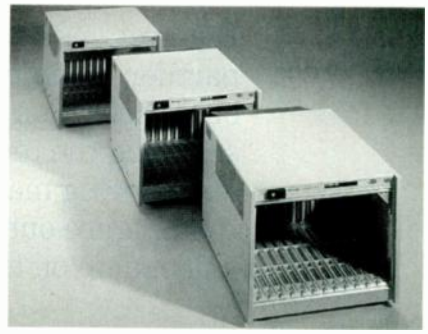
All three 13-slot mainframes automatically block air from entering empty slots, ensuring that cooling air is directed to the installed instruments. The VX1420A Super Cooler targets high-performance applications, where system density and power requirements demand the highest level of cooling. It offers closed-loop, slot-by-slot temperature monitoring and is programmable from either an internal or external controller. A quiet fan makes it suitable for benchtop use. In addition, a backplane shield helps control electromagnetic interference (EMI).

For fast digital applications requiring substantial current on the 5-V rail, the VX1420A delivers 90 A. An enhanced system monitor provides continuous real-time information about system performance, tracking parameters like the exhaust temperature of each instrument module, current drawn on each rail, total power, fan speeds, and so on.

In the middle of the mainframe series is the VX1410A, which supplies cooling somewhat below that of the VX1420A while maintaining many of the same features, including the enhanced system monitor, closed-loop cooling system, 90-A capability on the 5-V rail, and EMI shield. The front-panel display is available as an option. The VX1411A is the least expensive of the three mainframes. For quieter benchtop use, it employs variable speed fans based on the input ambient temperature and includes the backplane shielding. It's suitable for medium-performance test-system needs.

The lower-priced models are upgradable. Users can add additional cooling, programmability, and other features as test needs increase.

Four models make up the TVS600A series of waveform analyzers, which combine high-performance oscilloscope capabilities with extensive processing and analysis in a two-slot VXI module. The TVS621A and TVS641A have 250-MHz bandwidths and 1-Gsample/s digitizing rates, with two and four channels, respectively. The TVS625A and TVS645A offer a 1-GHz



bandwidth and 5-Gsample/s digitizing, again with two channels and four channels, respectively. Record length is 15 kpoints.

Enhancements include template testing, zoned waveform measurements, statistics, measurement limit comparison, full-function drivers for VXI*plug&play*, and a versatile soft front panel. Users can define sophisticated math expressions that include measurements and signal processing. The extensive on-board DSP-based analysis and Fast Data Channel protocol maximize test throughput.

The mainframe configuration service provides a new level of support for first-time VXI users or customers who want quick system configuration and test development. Tektronix will insert all Tektronix instruments and the slot 0 device into the mainframe, load all drivers and soft front panels, set all jumper switches, and test the system to ensure operation.

The VX1420 mainframe costs $7995; the VX1410A, $6895; and the VX1411A, $5495. Delivery is in four weeks. The TVS621A waveform ana-
(continued on page 120)

(continued from page 118)
lyzer costs $6800; the TVS641A, $11,800; the TVS625A, $14,500; and the TVS645A, $25,900. Delivery is in five weeks.

Tektronix Measurement Business Div.
P.O. Box 1520
Pittsfield, MA 01202
(800) 426-2200, press 3, code 1031
fax (413) 448-8002
CIRCLE 507
JOHN NOVELLINO

Windows Interface, Analog-Like Panel Make Digital Scopes Easier To Use

Almost from the introduction of the digital oscilloscope, users have complained that they were difficult to operate. At first, the basic controls had a different look and feel than they were accustomed to. Then, as more functions and advanced features were added, menus became more difficult to navigate than those in fancy French restaurants. Things have improved over the years, but apparently not enough. After more than a million dollars worth of research, Hewlett-Packard Co. discovered that oscilloscope users "say they spend too much of their time fighting test equipment instead of productively debugging designs." The company's response is a family of digital scopes with an analog-like front panel, a Windows 95-based graphical user interface (GUI), and a built-in information system, all aimed at making the viewing and analyzing of waveforms intuitive and easy.

The five models in the HP Infinium 548xxA line include two- and four-channel models with 500-MHz or 1.5-GHz analog bandwidths and from 1- to 4-Gsample/s digitizing rates. Memory depths are 32k to 64k per channel. The top model, the HP 54845A, interleaves its four 4-Gsample/s channels to achieve two 8-Gsample/s acquisitions.

The analog-like front panels don't use any menus or numeric keypads. Each channel has separate scaling and positioning controls. Trigger-setup information is clear and highly visible, and marker and measurement functions are easy to access.

HP's research also showed that users wanted a more familiar and intuitive way to access advanced features. So the company came up with a Windows 95 GUI that intuitively accesses features through dialog boxes. Unlike soft-key menu structures, the dialog boxes display all choices at once. Also, the GUI lets users grab a measurement icon and drop it on a selected waveform feature. Using zoom boxes, the operator can draw a box, click inside to expand a waveform, and zoom in on a particular portion of it for a detailed view.

Finally, a context-sensitive help button gives users access to the extensive built-in information system from the exact point where the user runs into a problem. The button is available in every dialog box. A standard feature of the system is a guide to 24 step-by-step procedures. They cover such areas as making complex measurements like noise and jitter, setting up advanced features like setup-and-hold triggers and fast Fourier transforms, and executing other common tasks, like compensating probes.

The Infinium line also introduces HP's violation trigger technology, which uses a new trigger IC to expand the offerings of trigger modes. In addition to edge, glitch, delay, logic, and video triggers, the scopes trigger on rise, fall, setup, and hold time. For example, race conditions that cause setup violations may result in unexpected logic-state transitions and be difficult for designers to isolate. Triggering the Infinium on these violations may lead to a faster understanding of a design problem's root cause.

The HP 54810A (two channels, 500-MHz bandwidth, 1 Gsample/s) costs $9995; the HP 54820A (two channels, 500 MHz, 2 Gsamples/s) is $12,495; the HP 54815A (four channels, 500 MHz, 1 Gsample/s) is $15,995; the HP 54825A (four channels, 500 MHz, 2 Gsamples/s) goes for $18,995; and the HP 54845A (four channels, 1.5 GHz, 4 Gsamples/s) is $29,995.

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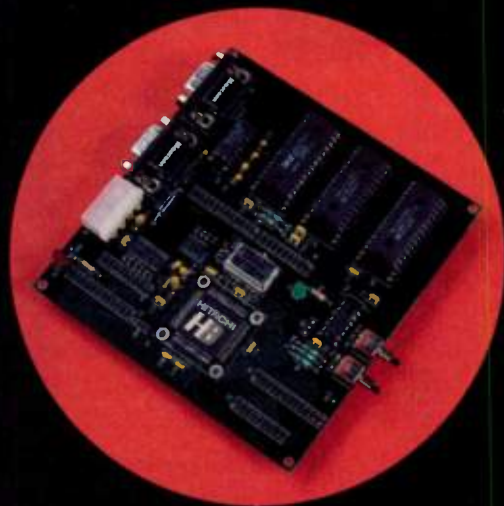

In today's hyper-competitive economy, nearly every single end-user product is being revamped to become more capable and user-friendly. If your job is to figure out how to do that, you may be asking some hard questions of your current system architecture.

Consider asking these same questions of an architecture that was developed for just this moment in time: the H8 line of embedded controllers. These 8- or 16-bit, register-based, RISC-like architectures offer efficient execution of high-level languages, record low power dissipation, an array of CPUs and large memories for complex programs. Choose from peripherals designed to enable today's target applications, including the industry's highest-density, on-chip flash for in-system programmability.

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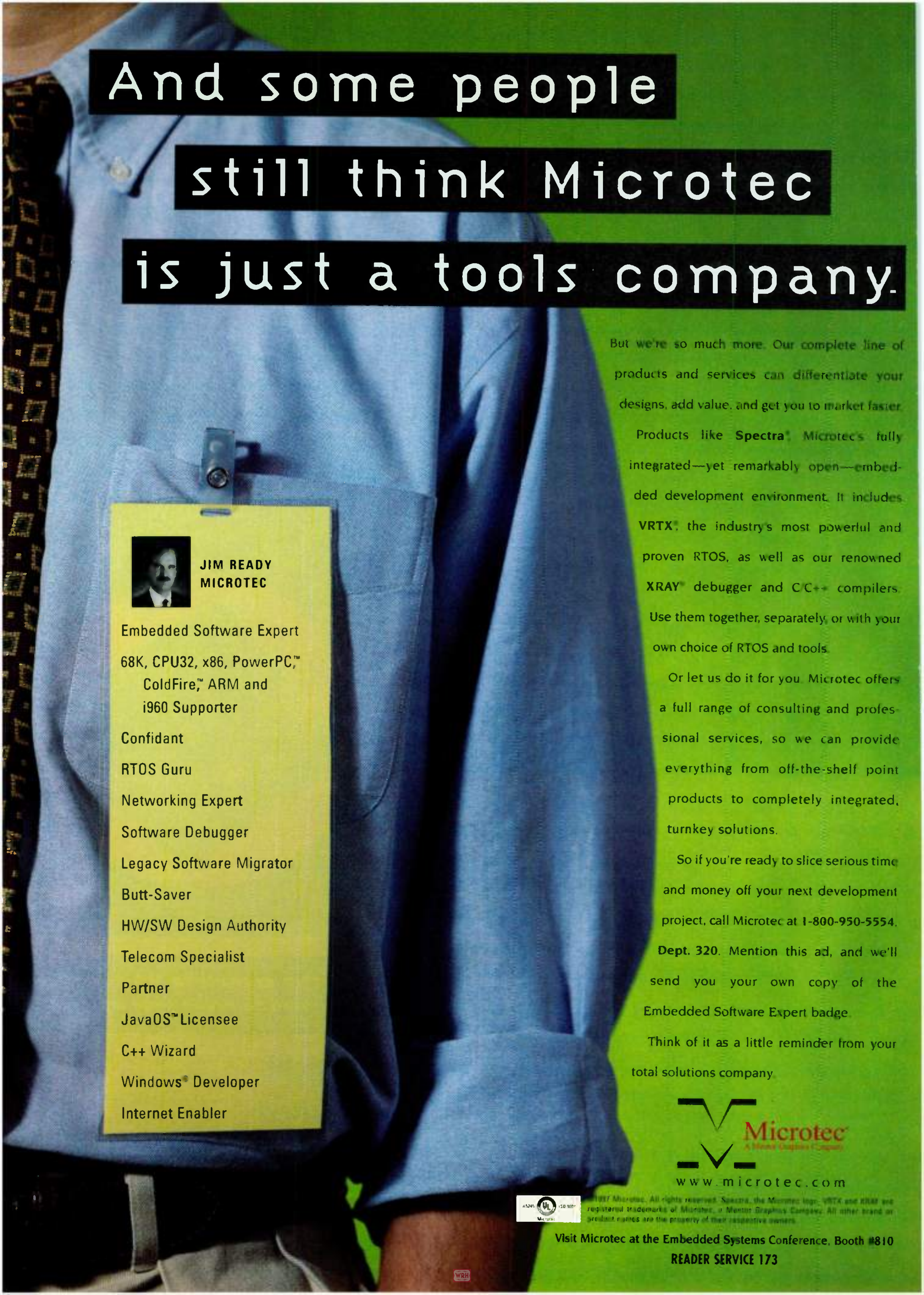
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CONFERENCE PREVIEW

Connectivity, Programming Highlight Embedded Systems Conference

Conference And Exhibition Showcases Latest Developments In Design Methods, Tools, And Technologies.

Tom Williams

Nine full-day tutorials, 150 classes, and a convention center brimming with over 200 exhibitors herald this year's Embedded Systems Conference West (ESC West), which will be held Sept. 29-Oct. 2 at the San Jose Convention Center, San Jose, Calif. The first day will be devoted to tutorials, with the following three days packed with classes and exhibits *(see the table)*. Among the dominant themes are connectivity—both via specialized industrial buses and protocols and the Internet—and ways of making designs more efficient and the design process easier.

Sure to be a popular attraction is a two-part series highlighting the spectacular success of the Pathfinder mission to Mars. "Embedded Systems on Mars" will showcase design techniques and development approaches for producing high-reliability, high-performance embedded systems better, faster, and less expensively. The discussion of the Pathfinder spacecraft will pay particular attention to the attitude and information management (AIM) subsystem. AIM manages all high-level functions during cruise, descent, and operations on the Martian surface. Also highlighted are the data-driven flight software, the object-oriented design approach, and the fault protection system.

Monday's (Sept. 29) tutorials offer in-depth coverage of topics in programming languages, real-time software development methods, connectivity, and management issues. "Stepping up to C++" is aimed at C programmers who wish to use the additional features of C++. Taking an evolutionary approach, the tutorial will discuss classes, access specifiers, constructors, destructors, derived classes, and virtual functions with an eye toward migrating people and projects from C to C++. "Object-oriented programming in Java" will cover the fundamentals of Java concepts such as package, class, interface, inheritance, and thread. Comparing Java with C++, the tutorial will introduce the basic classes in Java's core packages and give examples of their use.

IrDA And CAN Addressed

There are two tutorials that address connectivity. "IrDA infrared communications" will explore the software aspects of integrating IrDA into systems. There will be an in-depth look at the operation of the main protocol layers, including IrDA Lite and IrDA Object Exchange. "Embedded controller area networking (CAN)" offers a complete introduction to CAN including an overview of the different serial buses that are available, CAN's high-speed, short-latency protocol, and the benefits of CAN for different applications. Information on available devices, system development, and device programming will be included.

Tutorials on development methods include "Real-time object-oriented modeling" which will give an overview of the concepts of the Real-Time Object-Oriented Modeling (ROOM) method. The tutorial will demonstrate how to model using concurrent objects, with emphasis on capturing high-level architectures, complex state-machine behavior, and object reuse. "Guaranteeing real-time performance using RMA" will show how to analyze system designs using rate monotonic analysis (RMA) as a mathematically based method of ensuring that all real-time requirements can be met. The session will introduce RMA and discuss the analysis of timing in real-time systems. "The magic of hardware/software codesign, coverification, integration and experience on the bleeding edge of technology" reviews project experiences with various design tools including emulators, ROM monitors, hardware prototypes, software simulators, instruction-set simulators, and other tools. The real-life examples will suggest innovative approaches for the design of embedded systems.

Management-oriented tutorials include "Managing embedded projects" and "Software estimation and scheduling," which address some of the problems that crop up in large projects. Many of these are people problems. The first session looks at such things as dealing with difficult developers, creating and managing project specifications, and creating an environment conducive to efficient development. The second class looks at ways of scheduling large projects including the estimation process, the use of Gannt and PERT charts, adjusting resources, and project metrics.

Software topics break down roughly into issues around languages and their use, applicability, and selecting and using appropriate software development methods. In addition, the growing popularity of DSP and Fuzzy Logic are recognized in a number of classes. C, C++, and Java dominate the language topics.

Balancing C++ Pros And Cons

"Reducing run-time overhead in C++ programs" looks at ways of balancing the advantages of C++ with some of the penalties one pays in terms of code size. One of the tricks is in knowing which C++ features to use and which to avoid. "Manipulating hardware in C and C++" discusses the features of the two languages that can be used to directly manipulate hardware functions for such things as device drivers. It also presents techniques for packaging hardware interfaces as abstractions and placing data in ROM.

"Java in embedded systems" takes a realistic look at the potential for Java in embedded and real-time applications. Weighed against Java's advantages (and hype) are serious concerns about performance, code size, and real-time behavior with Java' s garbage collection mechanism. The class will draw on early experiences in trying Java in embedded applications. "Developing Java run-time applications" looks at a method of using Java as a front-end programming language and then using the GNU compiler to translate Java byte codes into machine code. The GNU linker is then used to link compiled class files to standard shared or static libraries.

"Thread support in the Java language" looks at ways to use Java's intrinsic multithread support to implement RTOS-like functions such as mutexes, queues, and semaphores. A practical example of the use of Java in a real-time system is given in "Java-based RTOS for telecommunications systems." The class looks at the benefits and drawbacks in the experience of building a system using a Java-based RTOS around a 68360 microcontroller.

Classes on programming methodology range from general introductions to object-oriented techniques and the tools that support them to specific problem areas such as debugging interrupt service routines. The latter type often spill over into the hardware domain as in "Introduction to the ColdFire EABI standard." This examines the Embedded Application Binary Interface developed by a group of over a dozen hardware and software companies to ensure the interoperability of tools and applications. Among the general introductions is a class titled "Applications of object-oriented technology to embedded real-time systems." This class starts with an introduction to the formal process of developing object-oriented software using the universal modeling language (UML) as the primary notation. It includes development of requirements via use cases, high-level analysis, refining analysis into design, and implementing the design.

A more detailed treatment of UML and object modeling is presented in a three-part class titled "Unified object-oriented methodology." The new methodology combines the advantages of Booch, OMT, and OOSE notations and provides a number of different modeling objectives. These include class, object, use case, message trace, state chart, module, and platform diagrams.

An alternative method of object modeling is presented in a two-part class titled, "Real-time development with the Shlaer-Mellor method." The heart of the method is a lifecycle-complete engineering process for organizing a system into separate domains: the architecture and the application. The behavior of these domains is then specified using object models that are then translated into code.

Moving closer to the specific needs of embedded systems is a two-part class titled "Fundamentals of multitasking." The class presents some basic approaches to decomposing a software system into tasks, scheduling tasks, and implementing intertask communication. The class includes an overview of the categories of software failures unique to multitasking embedded real-time systems. A related category, "State machines and statecharts," offers a three-part introduction to a key modeling tool for real-time designs. Emphasis is placed on Harel statecharts, which offer a hierarchical view of state machines. Real-time behavior can be modeled when Harel diagrams are teamed with state-oriented timing diagrams. The class shows the limitations of flat state models and how statecharts and timing diagrams can overcome them.

"How to simplify software for complex event-driven systems" is a two-part class that explores the challenges of systems with distributed environments, independent services and real-time constraints. Reducing the complexity of code requires analyzing various perspectives of the problem and then breaking it down into entities that represent their real-world counterparts. The second part of the class will show how traditional methods fail to give a realistic view of dynamically changing applications and how the history of an application can help reduce the number of decisions at any given branch and simplify the code.

Connectivity

Connectivity topics span the domains of hardware and software. A two-part class on "Networked embedded systems: A look at the issues, approaches and trade-offs" looks at requirements such as footprint, CPU utilization, and multiprotocol support. Approaches to supporting network infrastructure are examined form these requirements. Discussions include performance versus real-time response and trade-offs in the RTOS and protocol layer interoperability. An introductory class on "Embedded Ethernet" discusses easy ways to embed Ethernet connectivity into almost any device that generates serial, analog, or digital signals. The method lets standalone devices share data over networks with computers, MRP, SCADA, HVAC, and other systems.

"Bringing the web to the world: Adding web functionality to almost anything" looks at the need of consumer electronics manufacturers to go beyond mere connectivity. Consumer devices need to leverage the vast array of information that is now on-line. In addition to PC-like interfaces, solutions also are needed for devices with limited memory and storage such as PDAs, pagers, phones, and remote instrumentation. The Internet also offers the ability to access and manage a wide range of remote devices with open protocols.

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EMBEDDED SYSTEMS CONFERENCE WEST TECHNICAL PROGRAM

Time	Mon. Sept. 29 (tutorials)
8:30 a.m.-5:30 p.m.	**101.** Stepping up to C++. **102.** Guaranteeing real-time performance using RMA **103.** IrDA infrared communications. **104.** Managing embedded projects.**105.** Software estimation and scheduling.**106.** Object-oriented programming in Java. **107.** The magic of hardware/software codesign, coverification, integration and experience on the bleeding edge of technology. **108.** Real-time object-oriented modeling. **109.** Embedded controller area networking.

Time	Tues. Sept. 30 (classes)	Wed. Oct. 1 (classes)	Thurs. Oct. 2 (classes)
8:30-10:00 a.m.	**211.** Reducing run-time overhead in C++ programs **212.** CAN communication model and its implementation **213.** Year 2000: Planning is the key, Part 1 **214.** Software methodologies for improving interrupt performance of embedded applications **215.** Java in embedded systems **216.** CORBA and IIOP solutions for embedded systems **217.** How to simplify software for complex event-driven systems, Part 1 **218.** Introduction to microcontrollers, Part 1 **219.** New DSP solutions for digital motor control, Part 1 **220.** Rapid development of Compact PCI systems with I_2O	**311.** Translating Java to C **312.** In-system programmability of flash devices using the JTAG port **313.** Space optimization for RISC processors **314.** Security and protection in real-time operating systems **315.** USB: From abstraction to implementation **316.** Real-time development with the Shlaer-Mellor method, Part 1 **317.** Hardware/software trade-offs in microprocessor-based system design **318.** Managing embedded projects in reconstructive maintenance **319.** Embedded systems on Mars, Part 1 **320.** Networked embedded systems: A look at issues, approaches, and trade-offs, Part 1	**411.** RTOS design: How your application is affected, Part 1 **412.** Multitasking design and implementation issues in embedded systems, Part 1 **413.** Code generation from object models, Part 1 **414.** Java-based RTS for telecom systems **415.** CMOS device problems: The causes solutions of SCR latchup **416.** Adapting PC technology for set-tops **417.** Fuzzy Logic and neurofuzzy technologies in appliances **418.** Internetworking legacy LAN protocols over IrDA **419.** Debugging interrupts **420.** Introduction to embedded PCs, and analysis of embedded PC sourcing options
10:30 a.m.-12:00 noon	**221.** Manipulating hardware in C and C++ **222.** Flexible control of ac drives using CAN **223.** Year 2000: Planning is the key, Part 2 **224.** Unified object-oriented methodology, Part 1 **225.** FPGA-based embedded systems **226.** The application of Internet technologies **227.** How to simplify software for complex event-driven systems, Part 2 **228.** Introduction to microcontrollers, Part 2 **229.** New DSP solutions to digital motor control, Part 2 **230.** An introduction to Verilog	**321.** Commercial support for embedded C++ **322.** Adding removable media to embedded applications **323.** Embedded Ethernet **324.** State machines and statecharts, Part 1 **325.** Bringing the Web to the world—adding Web functionalilty to almost anything **326.** Real-time development with the Schlaer-Mellor method, Part 2 **327.** Distributed emulation: Experience and opportunities **328.** Evaluating hardware/software trade-offs **329.** Embedded systems on Mars, Part 2 **330.** Networked embedded systems: A look at issues, approaches, and trade-offs, Part 2	**421.** RTOS design: How your application is affected, Part 2 **422.** Multitasking design and implementation **423.** Code generation from object models, Part 2 **424.** Implementing Web-based management of networked devices **425.** Writing efficient code for small microcontrollers **426.** Mediators in object-oriented development **427.** Fuzzy Logic in automotive engineering **428.** Using state machines as a design and coding tool **429.** Embedded security in personal electroncis products **430.** How to create long-life Intel386 EX through Pentium Pro embedded PCs, and BIOS development for embedded PCs
2:00-3:30 p.m.	**231.** How to evaluate C++ as a language for embedded programming **232.** Adopting programming conventions **233.** Fundamentals of multitasking, Part 1 **234.** Unified object-oriented methodology, Part 2 **235.** Fundamentals of class design **236.** Developing Java run-time applications **237.** eRAM technology: Logic and micoprocessor with embedded memory technology for system-on-a-chip solutions **238.** Advanced DSP architectures, Part 1 **239.** Third-generation fuzzy processing **240.** An introduction to application-specific integrated circuit (ASIC) design	**331.** Debugging drivers with emulators and logic analyzers **332.** Inside real-time kernels **333.** Understanding the Universal Serial Bus (USB), Part 1 **334.** State machines and statechars, Part 2 **335.** Embedded operating systems platform for wireless systems **336.** The how-to's of flash: Implementing downloadable firmware, Part 1 **337.** Managing object-oriented development with ROOM **338.** Mixing C and Java in embedded systems **339.** Robust coding practices for appliances **340.** Embedding HTTP functionality for Web-based configuration and management of devices	**431.** C or C++ programming techniques, Part 1 **432.** PERC: Standard real-time extensions with the Java language **433.** Reuse-driven software processes for embedded systems, Part 1 **434.** The Streams Framework and its use for developing communications protocols in real-time embedded systems **435.** Microprocessors for consumer electronics, PDAs, and communications **436.** Reliability testing **437.** Coverification: A natural evolution in the design of embedded systems **438.** Controlling radio-frequency interface and electromagnetic radiation in pc-board designs **439.** Advances in microcontroller design for Internet appliances **440.** The Remote Procedure Calls architectures and embedded systems development
4:00-5:30 p.m.	**241.** Flash memory technology and techniques **242.** Debugging ISRs **243.** Fundamentals of multitasking, Part 2 **244.** Unified object-oriented methodology, Part 3 **245.** Focus on threads: An introduction **246.** Introduction to ColdFire EABI Standard **247.** Thread support in the Java language **248.** Advanced DSP architectures, Part 2 **249.** Application of object-oriented technology to embedded real-time systems **250.** Debugging compiled code	**341.** Using C++ efficiently in embedded applications **342.** Designing with real-time kernels **343.** Understanding the Universal Serial Bus (USB), Part 2 **344.** State machines and statecharts, Part 3 **345.** Next-generation background debug **346.** The how-to's of flash: Implementing downloadable firmware, Part 2 **347.** Fuzzy Logic and neurofuzzy applications in industrial automation **348.** Window CE in embedded applications **349.** Useful design patterns in Java **350.** Multiprocessor communication techniques	**441.** C or C++ programming techniques, Part 2 **442.** Product verification to support extended development **443.** Reuse-driven software processes for embedded systems, Part 2 **444.** Porting Unix applications to embedded real-time systems **445.** Task management in a microcontroller/DSP system with a new 32-bit microcontroller architecture **446.** Strategic needs and future trends of embedded software **447.** Early processor loading analysis **448.** Overcoming GSM design hurdles **449.** Don't reach for that target board—simulate your software! **450.** Command and control of embedded system products with speech recognition


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embedding tiny (100k) HTTP servers. These "microservers" enable users to control, configure, and retrieve data from networked devices using a standard PC-based web browser.

Two sessions deal with the details of controller area networks. One, "CAN communication model and its implementations," gives an overview of the CAN communication model and protocol specification features. These include transmission and receiving of standard and extended frames, arbitration, and information on failure handling and failure confinement. "Flexible control of ac drives using CAN" describes the use of microcontrollers with CAN functionality to deal with problems caused by distance between the drives and the master control unit.

The Universal Serial Bus (USB) is attracting attention as PC standards proliferate in industrial applications. "Understanding Universal Serial Bus" is a two-part class that presents an overview of USB with emphasis on software design issues. The class covers the protocol, bus topology, communications flow, access management, and isochronous transfers. "Universal Serial Bus: From abstraction to implementation" discusses the USB specification section dealing with the set of predetermined events that happen when a device is attached to or detached from a USB host. The class covers the attach-detach operation and device enumeration processes. Implementation and programming models are demonstrated with an Intel 8x930 microcontroller.

Optimizing Hardware Designs

Spanning the hardware/software field in connectivity is a class on the new I/O standard, I_2O. "Rapid development of Compact PCI with I_2O" demonstrates the integration of intelligent I/O that simplifies the writing, testing, and supporting of fewer device drivers. The class focuses on I_2O-based board-level and device driver solutions for PCI and Compact PCI, which enable the development of complex multiprocessing systems with ready-made interprocessor communications.

"Multiprocessor communication techniques" explores specific hardware-oriented approaches for communicating between multiple processors. Topics include communication between processors on the same board or bus as well as cable-based techniques for processors separated by distance. In response to the growing importance of Internet technology for embedded systems, "Advances in microcontroller design for Internet appliances" takes a system-level view of CPU enhancements that improve graphics performance, and enable software algorithms to replace dedicated peripherals in areas such as modem communications and audio and video telephony. Also discussed are high-integration chips, architectures for optimizing use of low-cost/high-bandwidth memory, embedded DRAM, and ASIC designs.

Memory is always a critical element of any embedded design. A number of classes look at various alternatives to memory subsystem design. "The how-to's of flash: Implementing downloadable firmware" is a two-part introduction to the wealth of design opportunities opened up by the proliferation of large-capacity flash memory devices. It also examines the challenges presented by this technology that must be overcome to design the next generation of embedded devices. A real-life example using field-upgradable firmware is presented.

"In-system programmability of flash devices using the JTAG port" looks at the difficulties and solutions for programming the flash boot device of the Intel EXPLR I 386EX evaluation board using the JTAG port on the 386EX. Also discussed are design recommendations that are applicable to all levels of X86 hardware architecture including Pentium processor designs using the Intel 430HX PCI chip set.

The appearance of large on-chip DRAM is making for faster, more compact embedded products. "eRAM technology: Logic and microprocessor with embedded memory for system-on-a-chip solutions" discusses 32-bit RISC processor designs with megabyte-level on-chip DRAM. This enables more parallel algorithms and higher-performance systems with a substantial reduction in power consumption. Examples of applications in consumer products include 3D graphics accelerators, digital cameras, and personal digital assistants (PDAs). The class also discusses design tools, integration technologies, and system-on-a-chip product development.

Technology advances are making design choices more flexible, such as the option to implement a given function in hardware or software. Making the right choice is critical to the success of a product. "Hardware/software trade-offs in microcontroller-based system design" looks at the potential trade-off between hardware cost and development time in small systems. Some of these are using small, inexpensive microcontrollers as discrete logic replacement. "Evaluating hardware/software trade-offs" discusses two examples. The first examines customizing instruction sets to meet price and power objectives without sacrificing performance. The second looks at the impact of different run-time scheduling algorithms on hardware requirements for embedded systems.

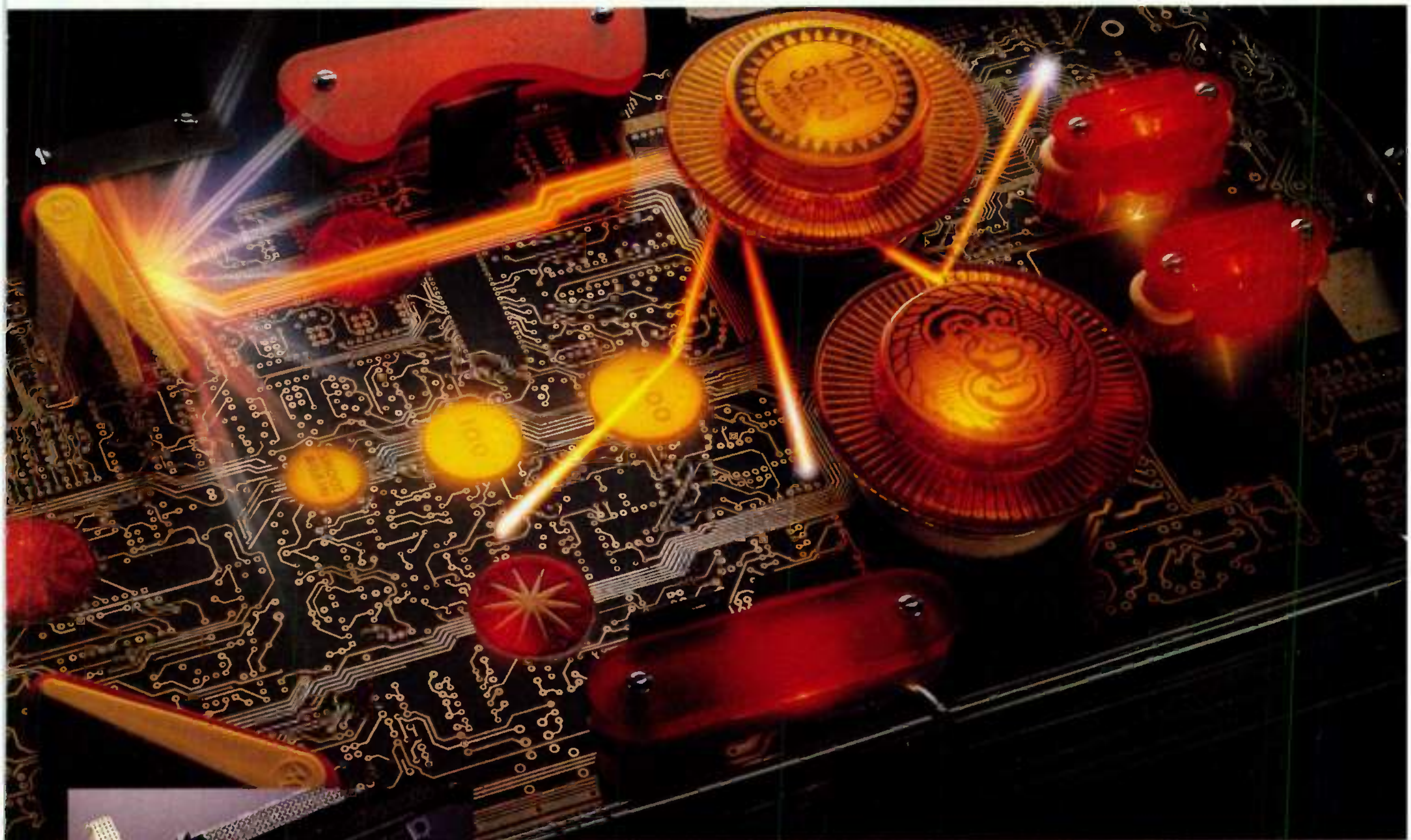
As systems shrink onto single chips, designers must concern themselves with the details of chip design and the conference offers several introductions to high-level design approaches. "An introduction to Verilog" provides a general overview of Verilog programming for hardware design. The class discusses how to define inputs and outputs, initialize registers, and design state machines and data paths. "An introduction to application-specific integrated circuit design" details step-by-step each phase of the design process from chip specification to final testing. The class discusses techniques for ensuring the design works the first time.

"FPGA-based embedded systems" looks at the potential for creating entire embedded systems (CPU, I/O, and memory) on a single FPGA. The World Wide Web can be used to help specify an embedded system. Web pages let the designer enter parameters such as number and type of I/O, memory size, and CPU capabilities. A tool called Synthia implements the circuit and returns a net list back to the designer. The class also deals with programming the FPGA-based systems.

For further information on the conference, contact Embedded Systems Conference West, c/o ARI Inc., 1515 Champion Dr., Suite 100, Carrolton, TX 75006; (972) 620-3011; e-mail: *http://www.embedded.com.*

HOW VALUABLE	CIRCLE
HIGHLY	534
MODERATELY	535
SLIGHTLY	536

At fast edge rates, the wrong interface takes on unexpected qualities.



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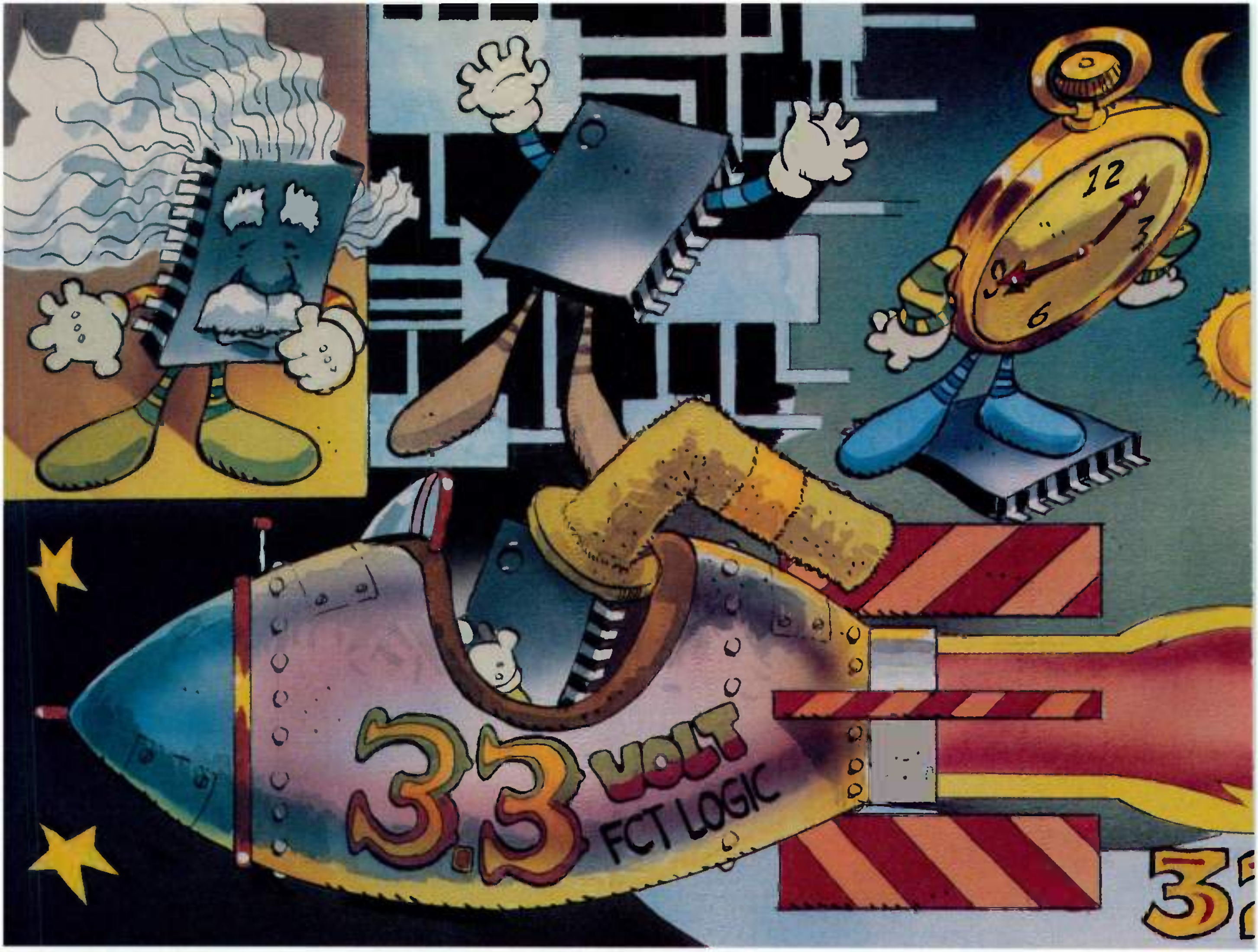

Innovation

QSI has a long-standing record of FCT logic, QuickSwitch® device, specialty memory product, and packaging innovation. Now QSI has introduced new and exciting networking products.

QSI has been at the forefront of package innovation, new and unique FCT logic devices, and specialty memory products since its beginning in 1989. The QSI family of products has grown to include some of the most innovative networking, analog, and JTAG products available today.

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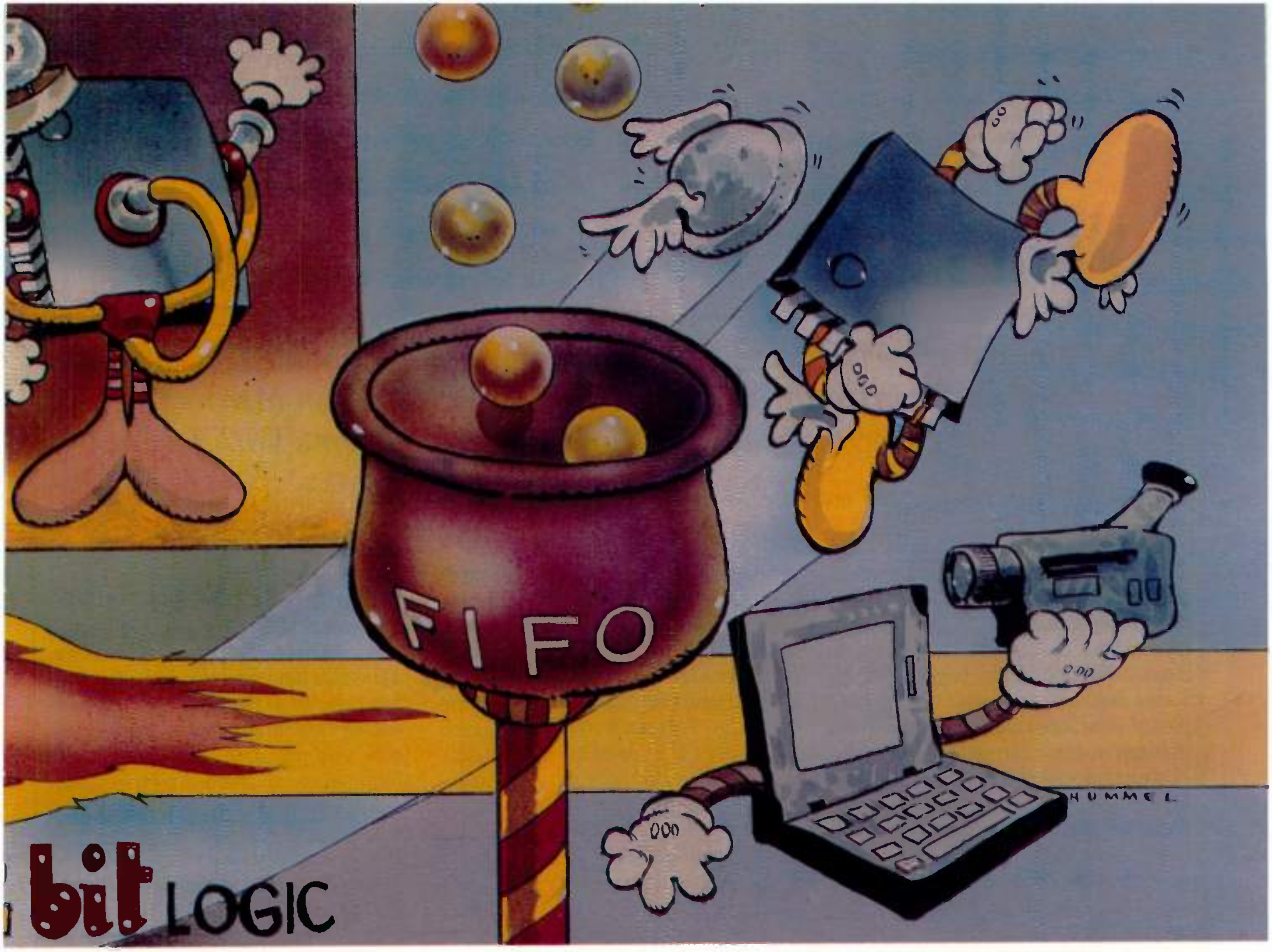

with no added power dissipation or ground bounce. All this means better overall system performance. And they are available in 8- and 16-bit configurations as well as 32-bit configurations in the new MillipaQ.

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Designing Real-Time Systems With The Unified Modeling Language

Object Methods Have Proven Invaluable For Development And General-Purpose Programming. UML Provides A Common Means Of Expressing Objects, Their Behavior, And Interactions With Users.

BRUCE POWEL DOUGLASS, i-Logix, 3 Riverside Dr., Andover, MA 01810; (508) 682-2100.

A couple of decades ago, in a galaxy far, far away, there was a pitched battle between the forces of structured methods and the denizens of hackerdom. The structured forces won, clearly and decisively, because structured methods are *better*. The principles of structured methods—functional decomposition, information hiding, and abstraction—allowed larger systems to be written in less time with fewer defects. More recently, there was a similar battle between the structured stalwarts and the revolutionary object-oriented (OO) guard. That battle also has been decided, again in the favor of the upstarts, and again because the newer methods are better.

Object-oriented methods provide an even better decompositional strategy with much better encapsulation and abstraction. There are case studies of large-scale systems in which the conclusion of the developers was that the products could not have been developed using structured methods. The size and scope of the products was just too large to have ever been achieved using traditional approaches. While the majority of new desktop software is being developed using object-oriented methods, only a small percentage of embedded systems currently use objects. According to International Data Corporation (IDC), in 1995, over 55% of the OO analysis and design market was using methodologies that now comprise the Unified Modeling Language (UML).

The UML is a third-generation OO modeling language. It adapts and extends previously published works, and contains improvements and suggestions. UML is being proposed to the Object Management Group as standard notation for object-oriented development. Since UML is meant to be used universally for the modeling of systems, it applies as well to real-time systems as it does to standard desktop software applications. It provides a rich set of notations and promises to be supported by all the major CASE tool vendors (e.g., Rational's ROSE, i-Logix's Rhapsody, Cayenne's ObjecTeam, etc.).

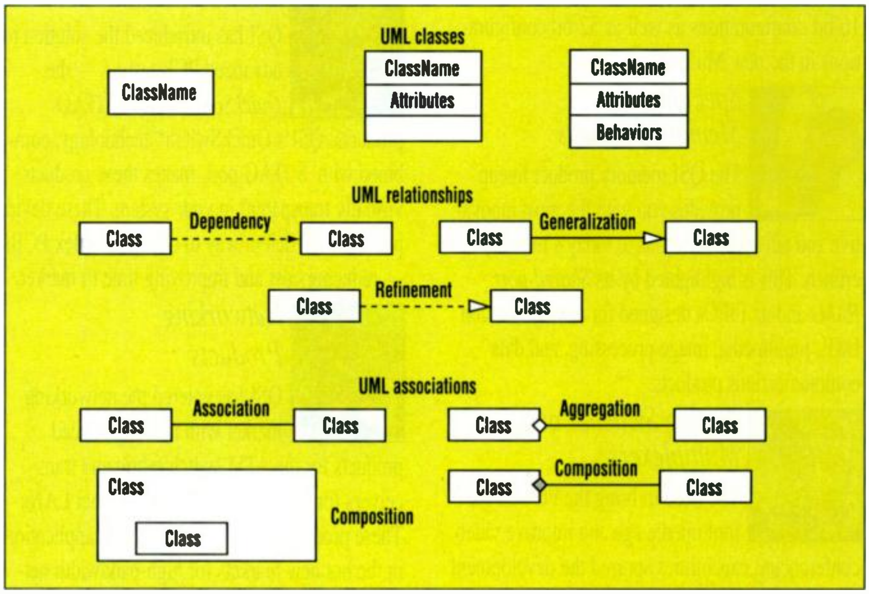
UML provides notation and semantics for a number of various models:

- Classes and objects;
- Use cases and scenarios;
- Behavior;
- Large scale logical packaging;
- Physical modeling.

UML Classes And Objects

Structured methods decompose systems on the basis of functionality. The data used by the functions is treated as an afterthought. This results in an increase in pathological coupling among functions and a decrease in the cohesion of the functions and the data on which they operate. Object-oriented methods instead decompose on the basis of objects, unifying data and the functions that operate on them. An object is an entity that contains information and the functions and operations that apply to it. In the real-time world, objects can be things like a flow sensor, a robot arm joint, or an elevator *(Table 1)*.

The *class* of an object defines its internal data structure and set of operations. When an object of some class is created, every object has exactly the same definition. That is, every object



1. Depicted are UML classes, relationships, and associations. A full description of a class includes its name, attributes and behavior at run time. Relationships between classes include dependency (parent/child), generalization, and refinement. Associations show how one class uses the services of another.

instantiated from the same class has exactly the same data items and operations. For example, every object of the *Flow Sensor* class has the data items *Flow* and *Total Volume*, as well as the operations *Get Flow( )*, *Get Volume*, and *Zero( )*. Different flow sensors have their own instances of the Flow and Total Volume variables, so that between different objects of type Flow Sensor the values of Flow and Total volume will differ. Thus, each object instantiated from the same class is identical to all other instances in terms of structure (data and behavior), but differs in terms of current values and current behavior. Most of the time, this subtle distinction between type and class can be ignored except in languages that make the distinction visible, such as Java.

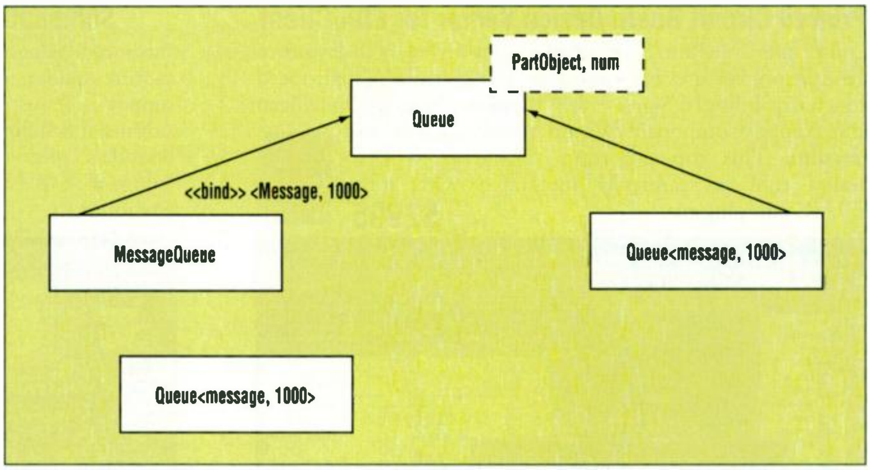
The key representation for object-oriented systems is the *class diagram*. Class diagrams show the important classes in the system and how they relate to each other. The notation uses rectangular boxes to visually indicate classes. From these classes, software objects will be created at run-time to perform the duties of the system. Some boxes display more information than others. The simple box contains only the name of the class. The 3-segment boxes give the name of the class in the top segment, a list of attributes in the middle segment and a list of operations in the bottom segment. The lists of attributes and operations shown need not be complete, since the complete definition of the class is held in the object repository provided by your CASE tool. The lines connecting the boxes represent some association between classes whose instances must communicate. UML distinguishes several different kinds of class relationships and associations *(Fig. 1)*.

UML Relationships

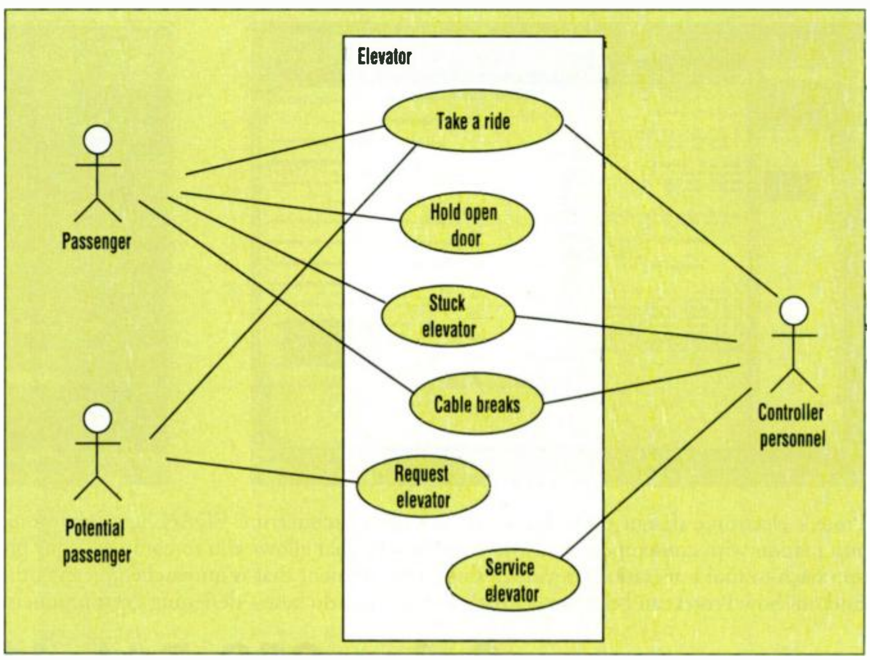
In UML, the term *relationship* is used to identify some connection between classes. One class can be a specialized version of another—this relationship is called *generalization*. For example, you might have a *sensor* class and it might be specialized into *attitude sensor*, *direction sensor*, and *speed sensor*. Generalization is one of the most powerful facilities of object-oriented methods because it allows programming by difference. One class is defined in terms of another and defined only by the differences. This relationship also is known as *inheritance*, *subclassing*, and *parent-child* relationship.

A generalization relationship means that one class inherits behavior and structure from the other; that is, one class specializes or extends the other. In UML, the more generalized class is called the *base class* or *superclass* while the more specialized class is called the *derived class* or *subclass*.

A subclass inherits all the data and behavior of its superclass. It may specialize those behaviors or extend them by adding new data and operations. A *Motor* class might have operations *Power( )* and *Speed( )*. A *DC Motor* will specialize the motor behavior by applying voltage to control the motor speed. A *Stepper Motor* can specialize the behavior by adjusting the step frequency. A *Stepper Motor* can extend its superclass by adding a



2. In refinement, an incompletely specified class is given enough information to have a unique name and parameterized values on which to operate. One technique uses the <<bind>> stereotype. UML provides stereotypes as a way to extend the expressiveness of UML itself and to more clearly specify the designer's intent. Stereotypes may be shown using gullimets, as in «bind», or using special icons.



3. A use-case diagram of an elevator system shows the ways users will interact with it. Each ellipse is an actual use case—some specific interaction with the system. The stick figures represent potential roles of users. Actor icons also could represent nonhuman elements such as other systems.

Zero( ) operation.

Implementing generalization is straightforward in C++. For example,

```
class sensor {
protected:
    int value;
public:
    virtual int getValue(void);
};

class AttitudeSensor : public Sensor {
public:
        virtual int getValue(void);
};
```

The AttitudeSensor child class can then redefine the *getValue( )* operation to do something suitable for an attitude sensor. Because *AttitudeSensor* is a subclass of sensor, it has a value attribute and a *getValue( )* function, inherited from its superclass. We define it again in the definition of *AttitudeSensor* so that we can change its behavior.

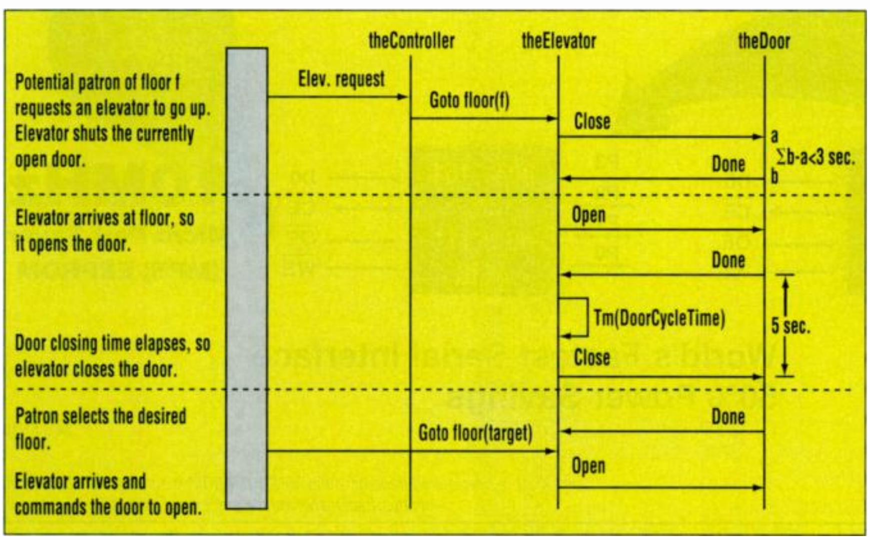
Implementing generalization in a structured language such as C is less obvious and requires the use of *ad hoc* coding rules. The simplest way is to use a struct to represent the data portion of the class and use a function pointer to implement the virtual methods, which in C++ are functions that may be overridden by subclasses. The subclass may then point to a different function. The function itself is implemented with an additional first parameter indicating the instance of the struct to which the pointer applies:

```
struct sensor {
    int value;
    int (* getValue)(sensor *this);
};

typedef sensor AttitudeSensor;
```

A *refinement* relationship describes a parameterized class (*templates* in C++ and *generics* in Ada) and the class that is created is the result of instantiation. Parameterized classes are an incomplete class specification, so no objects may be directly instantiated from a parameterized class. The refined class includes the definition of the undefined portions of the parameterized class. The undefined portions can be base types or numeric values. Container classes are most often implemented as parameterized classes. The container defines the containment behavior and structure, which is then refined to contain a specific type. A vector, for example, can define vector behavior without knowledge of the types of objects stored. The class can be refined to a vector of 1000 integers, and this class can be instantiated.

Figure 2 shows a parameterized Queue class that is in itself incompletely specified. To be complete, the type of object being queued as well as the maximum number of queued objects must be specified. Three ways to show the refinement relation appear in the figure. The first is with an explicit listing of the parameterized values on the refinement relationship itself along with the «bind» stereotype. This allows the refined class to be named, such as *MessageQueue*. Another means is to include the parameterized values between angled brackets that follow the name, as in *Queue<message, 1000>*. Lastly, the refinement relationship itself may be inferred by the presence of the parameterized values in the angled brackets, so it need not be shown. These latter two notations are useful when the refined class itself is anonymous, a common C++ idiom.



4. In a sequence diagram of the elevator scenario, vertical lines to represent objects and the messages passed between objects are shown using horizontal or diagonal arrows. Following the diagram left to right and down gives an exact sequence of messages and events that takes place between objects. For time-critical scenarios, timing noitations can be included along the left margin.

A dependency relationship means that a class depends on some service of another class, but does not have an internal reference or pointer to it. For example:

```
Class FilteredWaveform: public Waveform{
public:
        virtual int GetSample(void) {
                int x = Waveform::GetSample( );
                int pos = insert(x); // insert into internal queue wf
                return Smooth(wf, pos); // external function
                };
};
```

In this example, the FilteredWaveform GetSample( ) operation does not have a pointer or a reference to the Smooth function, but just "knows about" it. This knowledge allows its methods to be called even without a pointer.

UML Associations

A normal association implies that a client class uses some facilities of a server class. The lifetimes of the objects participating in the association are not bound together. Although an unadorned line is assumed to be a bidirectional association, by far the most common arrangement is that the client knows about the server, but not vice versa. A sensor object might act as a server to a number of clients. The sensor has no idea which objects may ask for the information, but the client objects know how to invoke the facilities of the sensor. To indicate unidirectional navigation, an open arrow may be added at the server end of the association.

Associations may be named, as in "contains" or "controls." Because the association is always named from one object's perspective, a standalone arrowhead indicates the perspective. The roles of the objects may be named by putting role labels next to the classes where the association connects. Although role names for both ends of any association may be added, it is usually enough to name one end. The other end is a simple conjugate of the first. If one role is "client," the other is likely to be "server."

An *aggregation* association means

that one object logically or physically contains another. Aggregation is shown with a small empty diamond on the "whole" end of the association. In C++, both aggregation and uses can be implemented by using either a pointer or a reference to the server or part object, as in:

```
Class Sensor {
private:
        Converter* ADC_Channel1;
        Converter& ADC_Channel2;
protected:
        int CalConst;
        int Value;
public:
        sensor(converter*C1,C2);
        virtual int get(void);
        int Calibrate(int cal);
};
```

TABLE 1. OBJECTS IN A UNIFIED MODLEING LANGAUGE

Object	Data	Operations
Flow Sensor	Flow	Get Flow( )
	Total volume	Get Volume( )
		Zero( )
Robot arm joint	Position	Step Foward( )
		Step Backward( )
		Get Position( )
Elevator	Floor location	Get Position( )
	Direction	Get Direction( )
		Add Destination( )
		Emergency Stop( )
		Alarm( )

UML allows sharing of an aggregated object by more than one owner object.

Composition is a stronger form of aggregation. It implies that there is exactly one owner object and the life of the aggregate object begins after the creation of the owner and ends before the end of the owner. The owner is explicitly responsible for the creation and destruction of the component. Composition may be implemented by pointers, references, or containment as in:

```
class Composite {
public:
   Obj1 *component1;
   Obj2 &component2;
   Obj3 component3;
};
```

The number of objects that participate in an association are known as that association's multiplicity. Often one instance of a class sends messages to one instance of another. This is a "1 to 1" association. Equally often, one instance of a class sends messages to more than one instance of another. This is called a "many to 1" relationship. UML multiplicities are shown at each end of the class association *(Table 2)*.

Objects communicate by sending messages to one another. The presence of an association necessarily implies that the objects communicate in this way. The concept of messaging is an abstraction of object communication. Object messaging may be implemented in terms of function calls (most common), a real-time operating-system (RTOS) message and event posting, or bus messaging. Abstracting object communication allows you to ignore the implementation details of object communication until design. In design, these messages will result in acceptor operations being defined in the receiving object(s) in the simplest case. Or they will be interfaces to an RTOS or communication protocol stack when the objects are in different threads or processors.

Use Cases And Scenarios

Use cases are broad-stroke descriptions of how a system will be used *(Fig. 3)*. They provide a natural high-level view of the intended functionality of the system that is understandable regardless of the technology used to implement it. This makes use cases invaluable for talking with customers and marketing executives who must specify the system to be implemented.

The large rectangle shows the boundaries of the system under development. The objects (shown using the UML-defined *actor* stereotype icon) arranged around the system are external objects that interface with the system. The ellipses inside the system rectangle indicate the use cases themselves.

Use cases are isomorphic with function points. This means that use cases *per se* are not object-oriented. They are, in fact, a functional view of the system. Generally, this means that use cases cannot be uniquely elaborated to an object view. Nevertheless, the use case diagram is a useful view for capturing and communicating high-level requirements.

A use case is a general pattern or strategy of system use. Consider the use case "Take a ride" from the elevator use case diagram *(Fig. 3)*. There are many different instances of this use case, such as when the elevator is at the floor when called, below the floor but going the right direction, or above the floor going the wrong direction. A use case always represents many different specific threads of interaction. These specific threads are called *scenarios*. Every scenario is a specific instance of a use case.

An example of a scenario from the "Take a ride" use case would be:

1. Elevator is Idle and above; the target destination is above.
2. Elevator is Idle and on the current floor; target destination is above.
3. Elevator is going up and is above the summoning floor; target is above the summoning floor.
4. Elevator is going up and is below the summoning floor; target is above the summoning floor.
5. Etc.

This is a particular path through the system functionality, but dozens of distinctly different scenarios are possible.

TABLE 2. OBJECTS THAT PARTICIPATE IN AN ASSOCIATION

Multiplicity	Description
1	Exactly one object participates
*	0 or more objects participate in the role
x..y	A range of objects participate in the role, e.g., 3..6
x,y,z	A list of possible numbers of participants, e.g., 1,3,5,6,9

UML provides two notations for modeling scenarios: The *sequence diagram* and the *collaboration diagram.*

Sequence diagrams use vertical lines to represent objects. Messages passed between objects are shown using horizontal or diagonal arrows as in the "Take a ride" scenario *(Fig. 4)*. Time flows from the top of the page down. Unless specifically annotated, only sequence of messages is shown, not exact time.

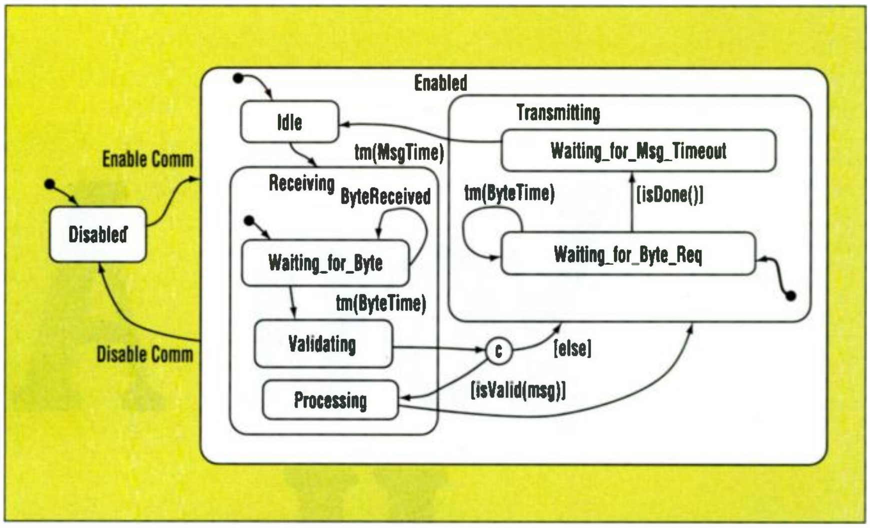
The textual annotations along the left edge of the diagram help explain the diagram. For real-time designs, exact timing must often be specified. UML allows textual annotations to be added to sequence diagrams when timing is important. There are two different notations used to specify timing. The first uses short horizontal lines with a time indication between them. The second labels the messages "a" and "b" and specifies a timing expression between curly braces. The timing specification is a constraint and UML notation places all constraints within curly braces.

Other extensions are used as well. Some are specified in the UML Notation Guide and others are provided as elaborations. For example, *Rhapsody*, the object-oriented CASE tool available from i-Logix, lets you specify the current state on the sequence diagram as well, providing an obvious visible linkage between the scenario models and the state diagrams. The other notation for modeling scenarios is the collaboration diagram. This diagram specifies the order of messages, and allows timing annotations as well. Sequence is more prominent in the sequence diagram but structure is more obvious in the collaboration diagram. Arrows attached to the messages indicate the direction the message is sent. The numbers on the messages indicate the order in which they are sent.

Real-time systems care a great deal how messages are handled between concurrent processes. UML provides icons that can be added to any message to indicate its concurrent behavior. The symbols are taken from Booch's earlier work.

These symbols can be added to the message to indicate how the concurrent processes are synchronized during the message:

- *Simple*—Simple synchronization merely denotes that the synchronization has not yet been specified.
- *Balking*—A balking rendezvous means that if the receiving task is not ready, the sending task aborts the message and continues.
- *Asynchronous*—An asynchronous rendezvous means the sender sends the message and continues without waiting for the receiver to get the message.
- *Time-out*—A time-out rendezvous indicates that the sender will wait for the receiver to be ready for the message up to some fixed time before aborting the message transmission process.
- *Synchronous*—A synchronous rendezvous means that the sender waits until the receiver is done processing the message before continuing. This is commonly implemented as a standard function call.



5. In this nested state chart, the substates "idle," receiving," and "transmitting" are nested within the state "enabled." This nesting can go down to any level. The © is a conditional connector allowing the conditional expressions to control the transition.

Behavior

UML behavioral models are based on finite state machines using the Harel statechart notation and semantics. Harel statecharts can more clearly depict complex behavior than the more common Mealy-Moore state models because they support:

- Nesting of states;
- Concurrency;
- Guards on transitions;
- Propagated events;
- Actions on transitions;
- Actions on state entry;
- Actions on state exit;
- Activities occurring as long as a state is active.

The single most important conceptual tool developed over the last 4000 years is the idea of decomposing difficult large problems into simpler smaller ones. Because Mealy-Moore state models don't provide either hierarchical or orthogonal decomposition, they don't "scale up" gracefully to large problems. As state machines get more complex, it becomes more and more difficult to represent them using flat models. Support for orthogonal components is necessary to provide the ability to model concurrency.

Consider a simple class that has 3 attributes:

- tColor color (eRed, eBlue, eGreen)
- Boolean ErrorStatus (TRUE, FALSE)
- tMode tMode (eNormal, eStartup, eDemo)

What is the "state" of an instance of this class? It is composed of the various possible values of each variable. There are 18 possible states. This example illustrates a well-known problem with Mealy-Moore state models—*state explosion*. To describe orthogonal components using a flat model, each combinatorial set of the component states forms a new state.

The other means of decomposition is the nesting of states. Just as object or functions can be composed into smaller and smaller pieces, states can be nested within other states. The semantics of orthogonal components dictate that when the object is in a state with orthogonal components, it must be in ex-

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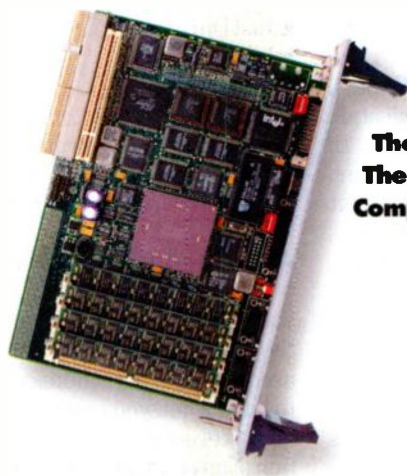

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actly one state for each currently active orthogonal component. The inclusion of orthogonal components makes UML state diagrams expressive in terms of concurrency, while the nesting makes them much more readable.

In the example of a communication controller, the states *Disabled* and *Enabled* are at the same level of abstraction *(Fig. 5)*. However, *Enabled* is decomposed into 3 primary substates: *Idle*, *Receiving*, and *Transmitting*. These latter two states also are "rich" and are further decomposed. While in the *Receiving* state, the communication controller can be *Waiting for Byte*. In this state, it is receiving a byte stream. If a time-out occurs before the next byte arrives, the controller assumes that the stream is done and then it transitions to the *Validating* state.

Within the "receiving" state, once "validating" is done, and if the received command is valid, it enters the *Processing* state during which it acts on the received message. When processing is done, the controller goes to the *Transmitting* state to send an ACK response. If the command is not valid, then it transitions to the *Transmitting* state immediately so that it can return a NAK. Nesting states in this way allows states to be decomposed, allowing the developer to break down large complex state machines into hierarchical structures.

Transitions are more elaborate in UML than even in the Harel notation. The UML syntax for transitions is:

name(argument list)[guard] ^ event list / action list(argument)

Let's examine each of field in turn.

- The *name* is the name of the transition. Often, this is the only thing specified for the transition.
- It has an optional *argument list* to indicate when data is present in the transition. This argument list is enclosed within parenthesis like a standard function call.
- The *guard* is shown in square brackets. A guard is a condition that must be met for the transition to be taken.
- The *event list* is a command-separated list of events that will be propagated as a result of this transition. This is largely how concurrent state machines communicate.
- Lastly, the *action list* specifies a comma-separated list of functions that will be called as a result of the action being taken. Each may have an argument list as well.

The syntax for transitions is rich and allows the triggering events to carry data, propagate other transitions, and initiate actions. For example, all of the following are valid state transitions:

- JustDoIt
- JustDoIt(x)
- JustDoIt(x: int)
- JustDoit(x) [x>0]
- JustDoIt [y<10] / print(y)
- JustDoIt(x,y) [x>y+10] ^Nike.MakeMoney(MuchoDinero) / print(y)

Advanced UML Features

UML provides a number of advanced notations and semantics where they are required. They don't have to be used, but like parachutes, they are nice to have when you really need them.

A stereotype is the metaclassification of an element of the UML. It identifies the type of the element within the UML metamodel. For example, predefined UML class stereotypes include Signal, Exception, Interface, Metaclass, and Utility. Predefined task stereotypes include Process and Thread.

The primary advantages of stereotypes are: They make it possible to refer to the type of the element, as in "That class is an Exception class;" and they allow UML to be extensible by the user of the method by definition of additional stereotypes. Stereotypes are indicated with the element name and are enclosed by guillemets (« ») or by special icons.

Real-time systems are often delivered on custom platforms, and the engineer must develop not only the software, but the hardware components as well. The hardware devices must be bound together with the portions of software they will run. UML provides *deployment diagrams* to show the organization of the hardware and the binding of the software to the physical devices. Deployment diagrams show various hardware devices (called *nodes*) and their physical interfaces. The type of the hardware device is given by its stereotype, such as Processor, Device, Display Memory, or Disk.

For large-scale development, UML supports the concept of *packages*. A package is a grouping of inherently cohesive entities. The class model can be packaged by area of concern, such as User Interface, Device I/O, and so on. UML uses a tabbed folder to represent a class package. Packages can contain things other than classes. Implemented code can be packaged into subsystems that represent deployed software components. Stereotypes are used to clarify the type of package («category» for the class model or «subsystem» for the code model).

UML is a third-generation, feature-rich object-oriented modeling language that is particularly appropriate for real-time systems. It provides support for the classes and object, and many kinds of associations among them, such as aggregation, uses, dependency, inheritance, and instantiation. Use cases are directly provided along with scenario modeling for detailed description of required system behavior. Enhanced finite state-machine modeling supports a number of real-time features including concurrency, event propagation, and nested states. The method itself is extensible though the definition of additional stereotypes.

UML is a powerful modeling language and has more notation and semantics than presented in this brief introduction. Interested readers are referred to forthcoming books on UML for more information. Notational guides and other information can be obtained from Rational Software's web site (*www.rational.com*) or the i-Logix web site (*www.ilogix.com*).

Bruce Powel Douglass has worked as an engineer in embedded systems for almost 20 years. He is currently working on two books on object-oriented methods for real-time systems, including "Real-Time UL: Efficient Objects for Embedded Systems" due out in November, 1997. He teaches courses in object-oriented methodologies for real-time systems, project management, and safety-critical systems design and consults and mentors companies wishing to use object methods in embedded systems. He is a member of the advisory board of the Embedded Systems Conference and is one of the UML to the OMG.

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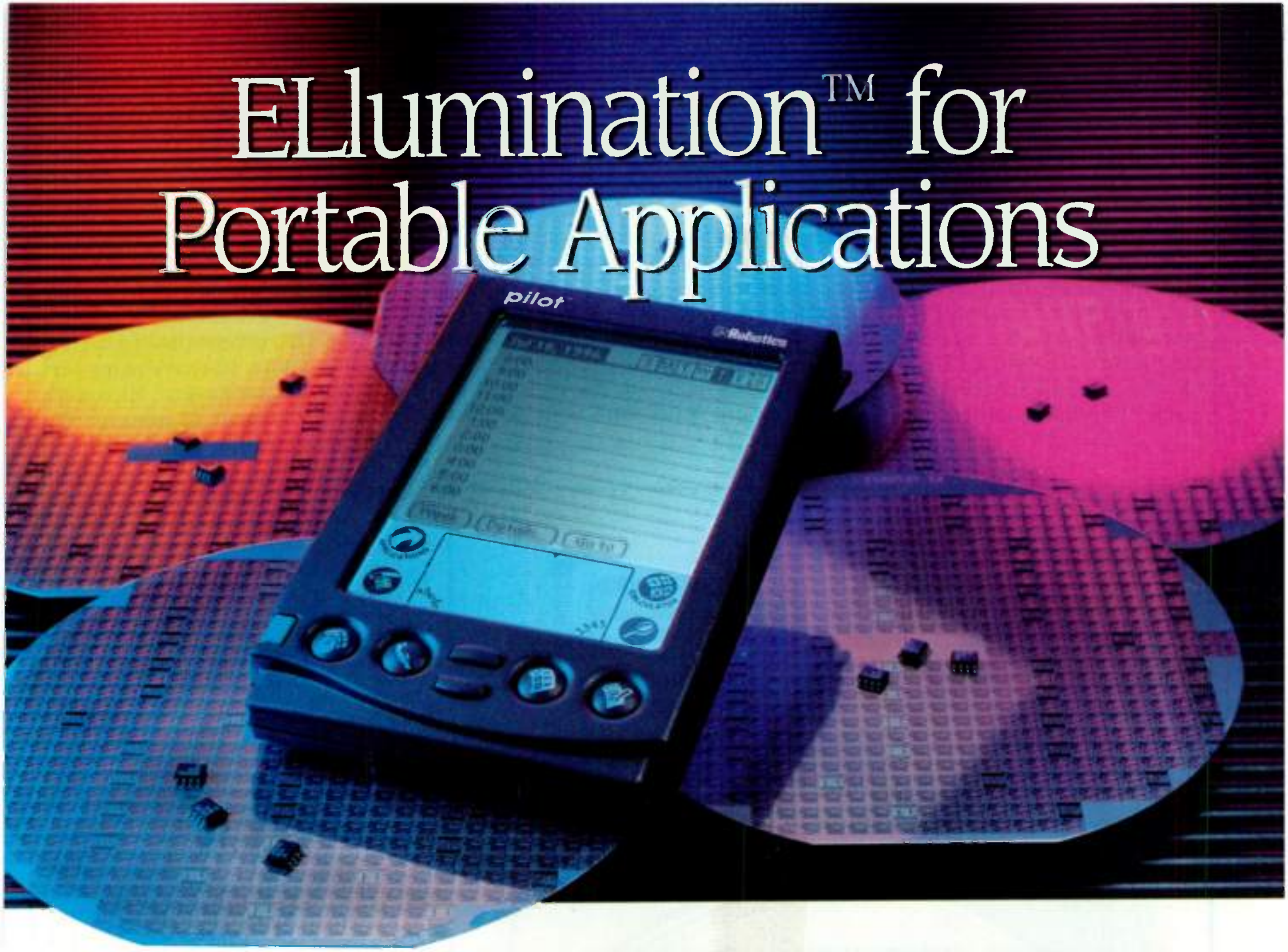

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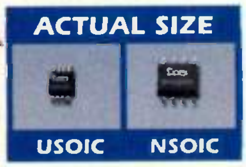

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PRODUCT FEATURE

32-Bit Operating System Rises To Challenge Windows CE

A new operating-system contender has entered the fray in the contest for the handheld computer and smart phone market. Psion Software intends to offer a broad-based OS platform, called EPOC32, that should rekindle interest in a wide range of mobile ROM-based devices.

The effort to market a generation of handheld computing and communications devices got off to a poor start a few years ago with personal digital assistants (PDAs) that didn't live up to users' expectations. Today, however, there's a resurgence of interest due partially to the Pilot PDA from US Robotics, the ever-increasing functionality of cellular phones, and the emergence of the handheld PC (HPC).

The HPC is a creature of Microsoft's Windows CE, which is itself a derivative of Windows 95 that's being targeted at handheld devices. Microsoft's blessing of the handheld arena set off a flurry of competition among other operating-system vendors for mobile computing and communication devices that has yet to be resolved (ELECTRONIC DESIGN, *May 27, p. 113*).

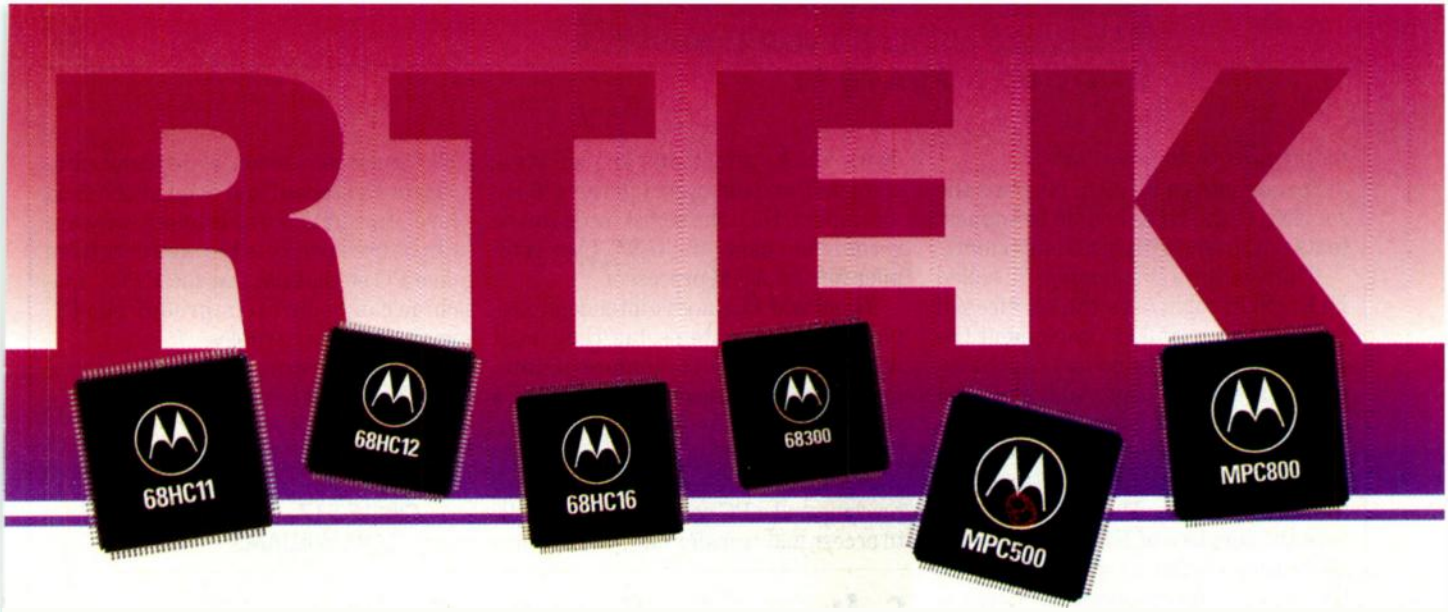
Only one of the competing OSs, GEOS from Geoworks, Alameda, Calif., was conceived from the ground up for mobile, handheld devices. Windows CE is a modified desktop OS and most of the others are real-time operating systems originally designed for a wide range of embedded applications. The issue is further confused by the demonstration by at least one manufacturer, Fujitsu, of an HPC running a full-blown version of Windows 95. Enter Psion with EPOC32.

EPOC32 uses a modular architecture based on a client/server model. A central "tower" of modules is arranged so that each module up the line uses the services of modules below. The base module consists of a real-time kernel, a set of device drivers, a user library, and a file server. Any application thread in the system that manipulates drives, volumes, directories, or files uses the API presented by the file server.

In like manner, the user library provides certain basic services to manage all user threads. One of the most important of these services is memory cleanup, or garbage collection. Because memory in handheld devices is a scarce resource, resources must be freed immediately when a thread is finished with them. This includes partially allocated resources, which must be freed if an operation fails.

Above the base module is an engine support module that provides support for application functions. These include a set of abstract base classes for graphics, a basic database management system (DBMS) and basic utilities. A text content model provides for the management of rich text. It pro-

(continued on page 146)



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(continued from page 144)

vides no fonts on its own, but uses the services of the GDI module to support fonts within the graphics component.

The user interface component called EIKON, in turn, uses the services of the graphics module to implement the GUI elements, such as toolbars, menus, and scroll bars. An application can be thought of as a user interface that sits on top of a custom application engine that defines the functionality of the user interface. The Application UI uses the services of EIKON while the application engine uses the services of the engine support module. Alternatively, applications can be written in OPL, a BASIC-like rapid application development language that can access all EPOC32 components.

Although it's highly portable among processors, EPOC32 is targeted at the ARM architecture defined by Advanced RISC Machines. Psion provides a development environment that runs on a Windows-based PC and uses Microsoft Visual C++. The WINS emulator runs under WindowsNT or Windows 95. Applications are written, compiled, and debugged in the x86 environment; then the source code can be recompiled using the GNU C++ compiler for the ARM processor.

Handheld PCs aren't intended to replace desktop systems, but they must provide for the interchange of data. Psion offers what it calls EPOC Connect software that can be extended and relabeled by licensees. The connect software runs on a PC and lets an EPOC32 machine and a PC see each other's disks to access and transfer data. It supports file format conversion, and synchronization at the record and even at the field level. In addition, the connect software can be used to access the printer drivers on a PC so that data on the EPOC machine can be printed through the PC without changing cables.

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TOM WILLIAMS

Software Configuration Tool Integrates Tightly With Development Environments

A software configuration and version control system aimed at mid-size to large-scale Windows-development organizations integrates seamlessly into a number of software-development environments. Visual Enabler from Softlab brings its own object-oriented data repository to keep track of development projects—their names and versions—down to the file level. It also includes an automatic build facility that works with the make-file features of an integrated development environment (IDE).

Integrating Visual Enabler with *(continued on page 148)*

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PRODUCT FEATURE

(continued from page 146)

one of its supported IDEs makes it look like a part of that environment. For example, Visual Enabler functions can be called from the pull-down menus of Visual C++. Initially it will directly support development environments from Microsoft. These include Visual C++, Visual Basic, and Visual J++. However, Softlab has licensed Microsoft's source code control (SCC) API, which is the API used to integrate Microsoft's own version control tool, Visual Source Safe. Thus, any IDE that supports the SCC interface can integrate with Visual Enabler.

Once Visual Enabler is integrated with an IDE, its object repository is behind the scenes. The repository is able to version any kind of file, such as source code, libraries, graphics files, and documents. Versions can exist in terms of projects or code configurations within projects. In this capacity, it follows a check-out/check-in model that allows multiple users to work on a given file at the same time.

Visual Enabler keeps track of all the multiple changes and provides collision detection to detect when one version conflicts with a previously checked-in version of a file. The tool simply detects conflicts and indicates that developers need to reconcile the differences. It doesn't support the automatic merge operations that can be found on other tools. This, according to Softlab's David Daniels, is because focus groups revealed that developers remain rather distrustful of automatic merge, and will tend to use it infrequently.

The repository maintains the histories of files in logical collections; a project can have an unlimited number of sub-projects. Projects can be labeled, branched, and merged. Labeling a project is, in essence, like taking a snapshot or baseline of that project at any given time. That enables you to say, "OK, this is our alpha release." Applying a label defines objects in a given hierarchy to be part of that particular project.

Another facility, called branching, supports parallel development by letting two branches develop off the same file. For example Project12a could be all files above the branched file plus the right branch. Project 12b would include the left branch. In addition, it is also possible to merge projects. Each snapshot of a project can be used to start a build. This requires that Visual Enabler also understand all of the dependencies that are among various files.

Visual Enabler doesn't try to replace the make-file facility of an IDE, but rather works with it. Once the IDE creates a make file, developers may go on making changes. Visual Enabler's make-file analyzer, which is based on the make-file grammar, can keep track of dependencies and keep the make file up to date. It also understands the different environmental setting for compiling and linking. This results in the creation of "build configurations," which are container classes for all of the build information.

At compile time, Visual Enabler's "one-button build" facility reads all of the build configuration choices and options that have been selected and the dependencies it has been tracking. Then it sends them to a job manager that can dispatch them to different machines on a network for a distributed build.

The ability to understand dependencies makes it possible to do impact analysis before committing to making changes in code. Often, what seems to be a rather minor change can have unforeseen consequences that may plunge a design team into major delays. This is true not only for code under development, but also for legacy code that must be maintained.

Visual Enabler has a language analyzer that can identify project dependencies at the file level boundary. Since the tool is integrated into the IDE, Softlab saw no reason to take the impact analysis further. Most IDEs have class hierarchy browsers that give the user insight into class dependencies. Currently, Visual Enabler has a language analyzer for Visual C++. Analyzers for J++ and Visual Basic will be available by the end of the year.

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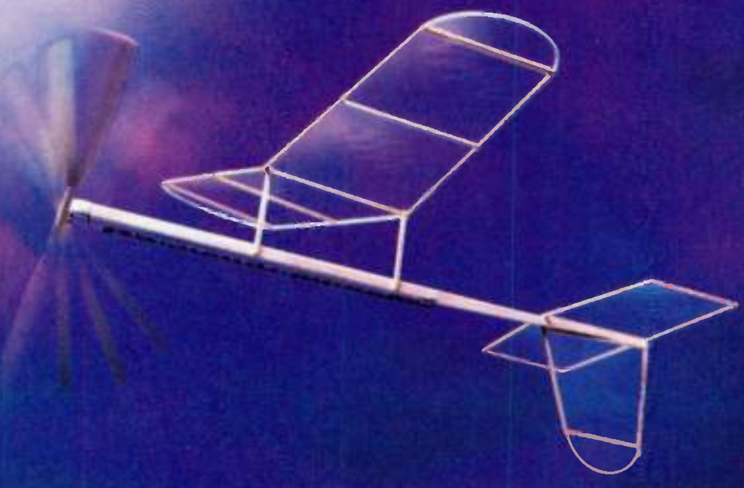

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EE2	15.0 x 9.5 x 10.0mm			
EA2	14.2 x 9.2 x 5.4mm	2c	140mW (Non-latch 3-12V)	30W (resistive) 62.5VA (resistive)
EB2	14.3 x 9.3 x 7.5mm			

The table shows specifications for standard types

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WRH

STANDARDS WATCH

Keeping Tabs On Embedded Software

Sara Killingsworth, ESOFTA Director

The embedded computing industry is enormous, with estimations of the market ranging from eighty to one hundred times the size of the reprogrammable computing market, including desktop PCs, workstations, and servers. The software portion of the embedded systems industry is huge, heterogeneous, and fragmented, with large user companies still tending to "roll their own" kernels and development tools. For these reasons, the software segment, while perpetually creative, has never formed an organization to address common goals and issues, to create a forum for entering into two-way communications with the software-user community, or to represent the embedded software segment to the industry at-large.

Unlike PC or workstation vendors in the reprogrammable computer market, the vendors/entrepreneurs representing the embedded software segment haven't enjoyed the benefits derived from an industry-recognized infrastructure. To address these various issues, the Embedded Software Association (ESOFTA) has been formed.

ESOFTA is dedicated to providing a support infrastructure as well as a unified industry forum for embedded computing software suppliers and users.

Such an association is necessary because, except for a vendor-customer relationship and one-on-one communications exchanges, there's no forum where embedded software users can discuss with software vendors their current issues and problems concerning embedded software or their specific needs for the future. This includes both large and small companies. In some respects, the association will play broker in enabling the connection for communication exchanges between users and vendors.

ESOFTA will host meetings and work with task forces to research and reach membership consensus on many pertinent issues and support any standards activities that will better the industry and its products. Software vendors currently have no venue or framework from which to follow through on some of these issues or concepts.

ESOFTA also will provide a repository for public domain software and documentation to which companies can contribute. This will be of substantial benefit to users of embedded software products.

To assist the member companies, ESOFTA will provide an assortment of communications and marketing services between companies and users. The first marketing service from ESOFTA is the compilation of the Embedded Systems Development Directory, which is a catalog of companies and their products with descriptions. The directory also contains information about many of the logic devices supported by the software tools. In addition, the group's founders believe that project engineers and programmers still need a printed compendium of resources to properly do their jobs. *Electronic Design* is printing and distributing the ESOFTA-compiled directory to be published every six months.

Other services include working with industry and market analysts in researching and analyzing market data regarding the embedded software segment.

Industry luminaries estimate the number of real-time operating-systems at more than a hundred, with all having been created over the last twenty years.

ESOFTA will use the Internet for communications and information distribution. The association's web site at ESOFTA.com contains the Embedded Systems Development Directory. The entire directory will be loaded onto the site. Eventually, however, only registered members will have products in the web-based directory version, and these member companies will receive statistical monthly reports on visitors, trends, and requirements.

Members also will communicate with users through ESOFTA's Internet facilities. And the repository for public domain software will be accessible through the ESOFTA web site.

The concept for ESOFTA grew from task force meetings of the VSO standards organization, the ANSI-accredited standards group of the VMEbus International Trade Association. This group met as the Embedded Systems Software Environment task force. The group met on issues such as device driver software, I/O, and so forth, but the consensus was that a separate organizational infrastructure was needed to handle software issues not tied to any particular bus or platform. Over time, ESOFTA should evolve into a member-driven embedded-software specifications body. A primary goal is to gain more visibility for member companies and increase awareness of their products.

For more information, call the association at (602) 991-4662 or send an e-mail to sara@esofta.com.

Latency Is The Problem

Keeping up with all the innovations in computer architecture seems impossible. Every day, we see disparate pieces of the evolution, and it leads us to believe that the process is chaotic. But, not so. Every advance in computer architecture is attacking the same basic problem with computers: Latency, or the delays in getting data from one point to another. Whether it's buses, networks, crossbar switches, or routers, every architectural innovation aims to solve some portion of the latency problem. And each one does it in a different manner, speed, and cost.

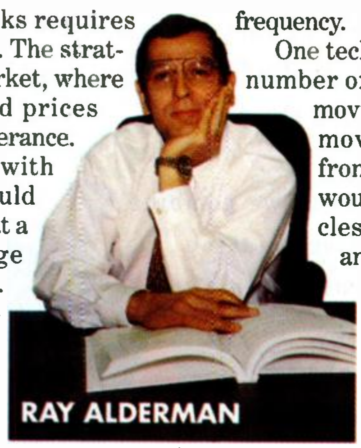
From a purist's point of view, any latency in a over 83 ps/in. (the speed of light) is man-made. The primary reasons for latency are spatial differential (distance), contention (multiple users of the same resource), and bandwidth mismatches (like a CPU that's faster than the I/O interface).

This latency problem has only surfaced in the last 10 years. The first generations of computers were all CPU-bound—the interfaces (I/O, memory, etc) could deliver data faster than the CPU could process it. Since about 1990, computers have become I/O-bound—the CPU can now process more data than the interfaces can deliver. This is essentially the result of Moore's Law, which says something like "the processing power of microprocessors doubles about every 18 months." The memory and I/O architectures, however, haven't increased their bandwidth at a similar rate.

Ultimately, there are five strategies to deal with the latency problem:

1. Simply accept latency as a characteristic of computers
2. Manage the latencies
3. Minimize the latencies
4. Overlap as many latencies as possible
5. Some combination of the previous four strategies.

Many designers simply accept the fact that latencies are a way of life. When the memory or I/O subsystem inserts wait-states, that's a sign the designer employed a tolerance strategy. The decision to tolerate latencies is often financially motivated. Matching the speeds of memory chips to high-speed CPU clocks requires more expensive RAM. The strategy in the desktop market, where margins are thin and prices drop by the hour, is tolerance. Solving the problem with higher-cost RAM would put the manufacturer at a cost disadvantage against its competitors.



RAY ALDERMAN

One latency management technique is cache coherence. When data has multiple users in the architecture, there's a problem with ensuring that every user gets the latest, updated copy of the data. If a user changes the data and sends it to a common resource (like a bus), other parties "snoop" the address to see if they are interested. If it's a common piece of data used by any other CPUs, they "snarf" the data when it comes across the bus. One "write" transaction on the bus could result in many recipients of the data. That way, when the latest copy is needed, it's already in memory and that device doesn't need to get on the bus and read the latest copy from some common global memory location. This reduces bus traffic and makes the architecture more efficient, or so the theory goes.

The problem with techniques like cache coherence is that there is a "knee in the curve" of scalability. Some coherency algorithms result in very high processor utilization up to about four CPUs, but processor efficiency drops to below 60% when the next two CPUs are added to the system. Other coherency algorithms fall apart at seven or eight CPUs. Latency management techniques work across a very small portion of the computing spectrum and are never scalable past the knee of the curve. Latency-management techniques aren't solutions to the problem. Mostly, they're just a band-aid over a bullet hole.

There are many ways to minimize latency. A popular method is to increase the clock speeds of the architecture. This always comes with a steep increase in hardware cost. Other minimization techniques can increase data-transfer bandwidth at the same clock frequency.

One technique is to reduce the number of latency cycles when moving data. For example, moving 10 words of data from memory to the CPU would take 10 address cycles (connection latency) and 10 disconnection cycles (disconnection latency) on the bus. By moving the 10 words as a packet, you only need one address cycle and one disconnection cycle for all 10 transfers. This is how DMA controllers work, and it dramatically increases the efficiency of the architecture for a fixed clock frequency.

Many computer architects argue that removing the handshakes on each individual word moved on a bus, and using a handshake on a packet of words, eliminates the guaranteed-delivery mechanisms in the architecture. Those who think this way haven't looked at the facts. Handshakes only guarantee that the handshake protocol is working. It doesn't guarantee anything about the presence or validity of the data. The only shared characteristics of the handshake and data lines on a bus is their timing relationship, and they are mutually exclusive. Without parity or CRC characters, there's no such thing as guaranteed-delivery in any computer architecture. And both of those techniques fall apart in worst-case scenarios.

Probably the most interesting technique for handling latencies is overlapping them. In other words, it's the execution of concurrent protocols, all occurring during the same time period, giving the illusion that many latencies have been eliminated. If multiple processors are using a common backplane bus, then any CPU who wants to use the bus must arbitrate for access. If the arbitration occurs on a separate set of signal lines while transactions are being accomplished on the data bus, it gives the illusion that arbitration latency in a multiprocessor system is always zero. The data bus never sees any arbitration latency, and because it's the common re-

source shared by all CPUs, its utilization is always very high.

The most effective way to combat the effects of latency is to use some rational combination of the above techniques. An example would be an architecture that uses a "look-ahead pipeline." If we have a CPU whose responsibility is to maintain efficient use of resources, and we know which devices in the architecture want to talk to each other, and we have multiple paths for the data to flow, then we have a look-ahead pipeline.

Suppose we have 10 boards in a system that communicate with each other. The main CPU can take requests for transactions on a control bus and put them in a queue. Then, the main CPU would issue transaction grants on the control bus for each set of boards that wants to communicate. So, Board 2 is talking to Board 5 on Data Channel 1, while Board 3 is talking to Board 4 on Data Channel 2, and so on. We have overlapped the arbitration, connection, and disconnection latencies with the data-transfer latencies, thereby giving the illusion that they no longer exist.

However, in this configuration, the number of data paths needed to maintain 100% efficiency in the architecture is the number of boards (N) minus 1 divided by 2, or (N-1)/2 paths. For 10 boards, that's five paths (rounding up), and this could get expensive, particularly if the data paths are parallel connections.

There is no perfect computer architecture. They all have unique problems and "abhorent behaviors" based on their topographies and protocols. Of the known latencies, protocol is the worst. Engineers can design and build super-efficient electrical and optical layers for computers. Then, the architects festoon mountains of protocol on them resulting in an inefficient system. Ethernet is a good example of this phenomenon. When the designers stuck the CSMA/CD protocol on the cable, performance went from 10 Mbits/s to a practical maximum of about 3 Mbits/s. In the final analysis, there's only one thing to remember when designing a computer architecture: Protocol kills performance.

Ray Alderman is the Executive Director of VITA. He can be contacted at exec@vita.com.

DESIGN APPLICATION

High-Speed Apps Need Intelligent Data-Acquisition Interfaces

While The Trend Is To Build The Intelligence Into The Interface, Off-The-Shelf Parts Can't Maintain The Data Rate.

RICHARD JAENICKE, SKY Computers Inc., 27 Industrial Ave., Chelmsford, MA 01824; (508) 250-1920.

Many types of data-acquisition systems contain a significant amount of knowledge about the data being acquired, the conditions under which it is acquired, and its properties after any localized preprocessing. The resulting data being transferred to the signal- or image-processing system can vary dynamically with the number of samples, frequency of arrival, reliability, and interpretation. For a real-time multiprocessing application, different types of data sets are often better suited for processing in different processor groups. The groups could vary by number or type of processors, and the amount or type of memory. While the trend is to place enough intelligence in the data-acquisition system to identify the data that needs to be processed in different processor groups, off-the-shelf interfaces to the signal processor have not been capable of using that information intelligently.

To meet the varying requirements of different applications, we define three levels of intelligence in the interface to data-acquisition systems. As each level adds more intelligence to handle more demanding application requirements, it becomes more difficult to simultaneously meet performance requirements. For each level, a COTS-based solution is described that achieves both the performance and intelligent data-acquisition functionality. The end result is a high-performance solution that's data-driven rather than processor-driven.

Fast And Robust

At the most basic level, the interface between the data-acquisition and the signal-processing systems needs to be fast and robust in the face of occasional errors. One example is a radar system, which can generate a higher data rate than most signal-processing systems can handle, yet it may occasionally have a data dropout. If the interface was expecting a fixed-size data block and doesn't receive one, it will lose synchronization. What then occurs is either hanging the system or using part of the next block to fill in the missing numbers, neither of which is a good option.

A straightforward solution is the use of a synchronization signal at the end of every data frame. Such a mechanism is provided as an option in the Front-Panel Data Port (FPDP) standard. For interfaces that implement this "synch" option, a dropout doesn't cause a problem. The end of the data frame is clearly marked, so it's possible to allow a dynamically varying data-set size. Not only does this take care of the data-drop errors, but it's also useful for applications where the data-set size naturally varies from frame to frame.

Beyond the basic level of intelligence, some applications require the ability to distribute different data frames to different groups of processors.

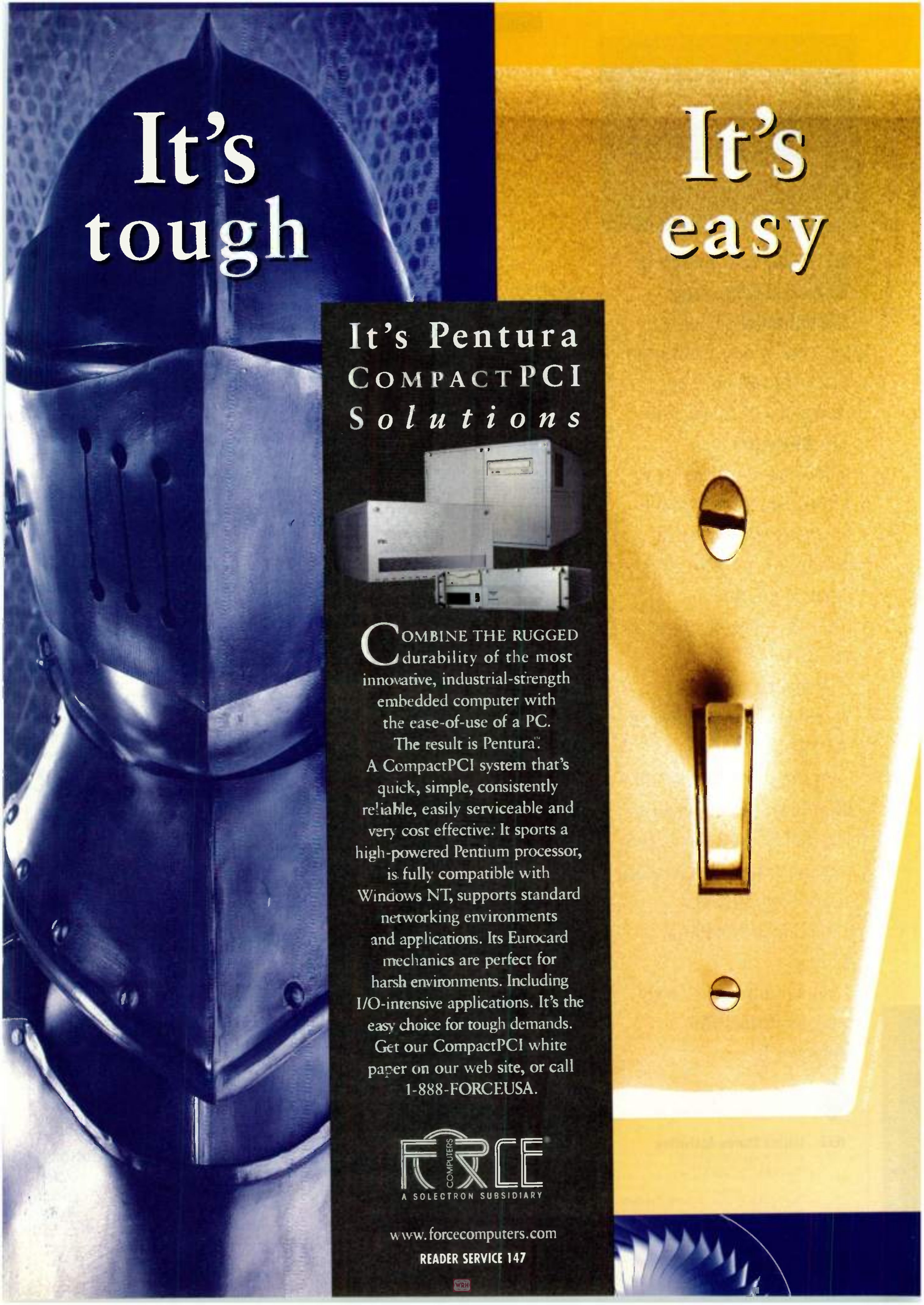
The scan line of a CT imaging system is an example where the line length varies with position in the circular cross-section.

In practice, applying this solution requires a careful interface selection because many FPDP-based products do not support the synchronization option, dynamically varying data-frame sizes, or the performance level that's defined in the FPDP specification (40 million words/s). One interface card that supports this base level of intelligence is the SKYburst 160 daughtercard. Implementing the FPDP specification, the SKYburst 160 card can handle the data dropout and dynamically varying data-set sizes.

Programmed Data Distribution

Beyond the basic level of intelligence, some applications require the ability to distribute different data frames to different groups of processors. A reason for this is that different data frames require different types of processing and possibly different types of processors. Additionally, there's the need to distribute the data to different processor groups for load balancing. When the order of distribution is known beforehand, this requires an interface of mid-level intelligence. Two examples are a radar system that varies the number of range gates and a medical imaging system that alternates between high- and low-frequency data sets.

The basic level interface typically can't handle this problem due to the combined functionality and performance. Functionally, the interface must be able to go down a list of destination addresses, sending data frames sequentially to each. For per-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formance reasons, this function must be done solely in hardware, without intervention from a programmed processor. For every microsecond taken by the processor to provide a new destination address, over 160 bytes of data are lost at 160 Mbytes/s. Practically, the data must be able to be sent elsewhere in the system, because many different processor groups aren't likely to be available on the same board as the data-acquisition interface.

The solution to this problem is to provide a programmable destination address list in the data-acquisition interface hardware. As each new frame is received, the pointer is updated to the next address in the list. A counter determines when the end of the list is reached so it can start again at the beginning of the list. Such an address list is provided by the SKYrider (real-time intelligent data envelope router) parallel I/O interface in step mode. The addresses in the list are 44-bit SKYchannel addresses, so the data is sent directly to the ultimate destination anywhere in the 16-Tbyte address space. The counter steps through the address list without processor intervention, and without copying the data along the way. By removing the processor from the loop, the data distribution becomes data-driven rather than processor-driven.

Dynamic Data Distribution

The most complex data-acquisition problems require a level of intelligence in the interface that goes beyond a predetermined address list, and necessitates choosing the destination address based on the data's contents. In a phased-array radar application, this technique could be shown through data coming from different antenna subgroup sizes being assigned to different processor groups. This information is known by the radar controller and can be known by data acquisition system, so a mechanism is needed to transport that information. New functionality is required at the receiving interface to act on the information.

Again, an interface of base-level intelligence won't be able to keep up with the data-stream rate simply by having a processor examine the incoming data and then send the data to the correct location. The solution requires a simple protocol addition that works within the FPDP specification. The information known about the data-set type set is encoded into an integer by the data-acquisition system, and placed as the first word in the data frame. The intelligent interface can then use that integer tag to determine the destination address. Note that the data-acquisition system needn't know the actual address of the destination processor group, only the type.

With the addition of a feedback mechanism, even more intelligence can be placed up front in the data-acquisition system. With information about the time taken to process a data set in a particular process group, the data-acquisition system can track which processor groups are free to accept the next data frame. It could even attempt dynamic load balancing. The feed-back mechanism could be a low-speed serial port or an additional FPDP interface flowing in the opposite direction.

FPDP provides the base for these intelligent data-acquisition interfaces. With a simple extension to this standard COTS interface, the data can be sent directly to the final destination without processor intervention. The destination choice is based solely on information provided either dynamically by the new data header or from a fixed schedule preprogrammed into the extended data-acquisition interface. In this manner, the data's arrival drives the processing. This solution provides the bandwidth required for input streams up to 160 Mbyte/s by eliminating the bottleneck imposed by a processor trying to read, evaluate, and write a data stream, all before the input buffer over runs.

Richard Jaenicke is director of marketing at SKY Computers Inc. He holds a BA in Computer Science from Dartmouth College and an MS in Computer Engineering from Rensselaer Polytechnic Institute.

How Valuable	Circle
Highly	528
Moderately	529
Slightly	530

DESIGN APPLICATION

MIL-STD-1553 Alternatives Look To Knock Off The King

Fibre Channel Is Among The Contenders With The Specifications To Offer A Challenge.

DUNCAN YOUNG and JOHN WEMEKAMP, DY 4 Systems Inc., 333 Palladium Dr., MS 212, Kanata, Ontario, Canada K2V 1A6.

In VMEbus systems, MIL-STD-1553 has long served as its backbone data bus for harsh environments. However, a number of challengers are jostling to take over. Faster interconnect technologies including Fibre Distributed Data Interface (FDDI), Fibre Channel, Asynchronous Transfer Mode (ATM), IEEE 1394 (Firewire), and Fast Ethernet are threatening to dethrone 1553 as the de facto standard high-speed data bus for harsh-environment vetronics, avionics, and naval electronics applications.

For a new backbone network to be accepted by today's demanding military industry, it must withstand harsh environments. It also must follow an international standard, have a commercial following, and offer both low maintenance and low latency. It must allow for the addition of new modules and/or boxes. It must be fault-tolerant and capable of offering isochronous video and deterministic bandwidth for command/response applications plus flexibility in data delivery protocols. And it has to be done at over 100 Mbits/s.

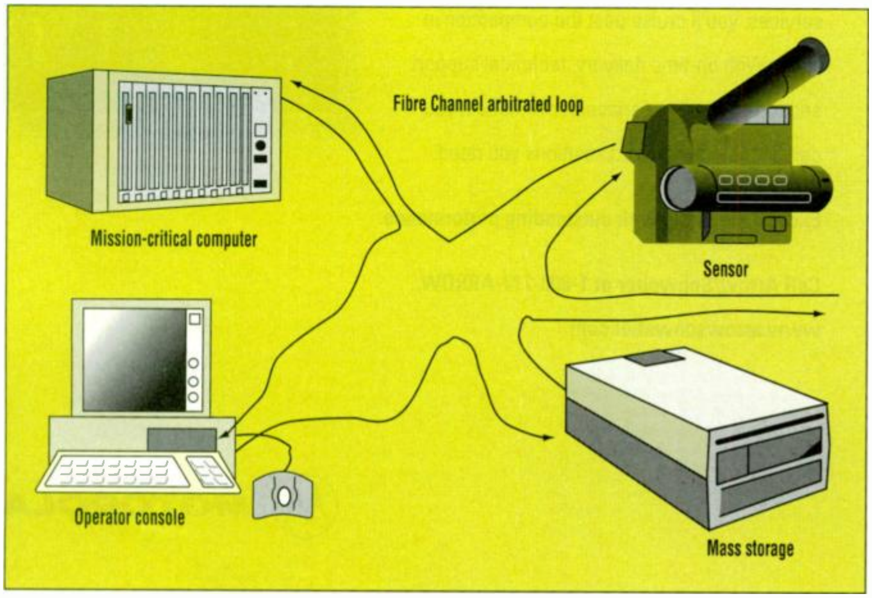
Part of the reason MIL-STD-1553 is so extensively deployed is its capability to meet most of these high-level requirements. Its longevity is a reflection of many positive attributes, including linear LAN architecture; capacity for redundancy with its inherent dual-bus approach; support for electrical isolation with transformer coupling; real-time determinism due to its control response protocol; support for nonintelligent remote terminals; and its extensive implementations in harsh environments.

Yet this popular standard is ultimately doomed because it is limited to a 1-Mbit/s data transmission rate—far too slow for the increased peer-to-peer communications required to support today's and tomorrow's data, audio, and video communication.

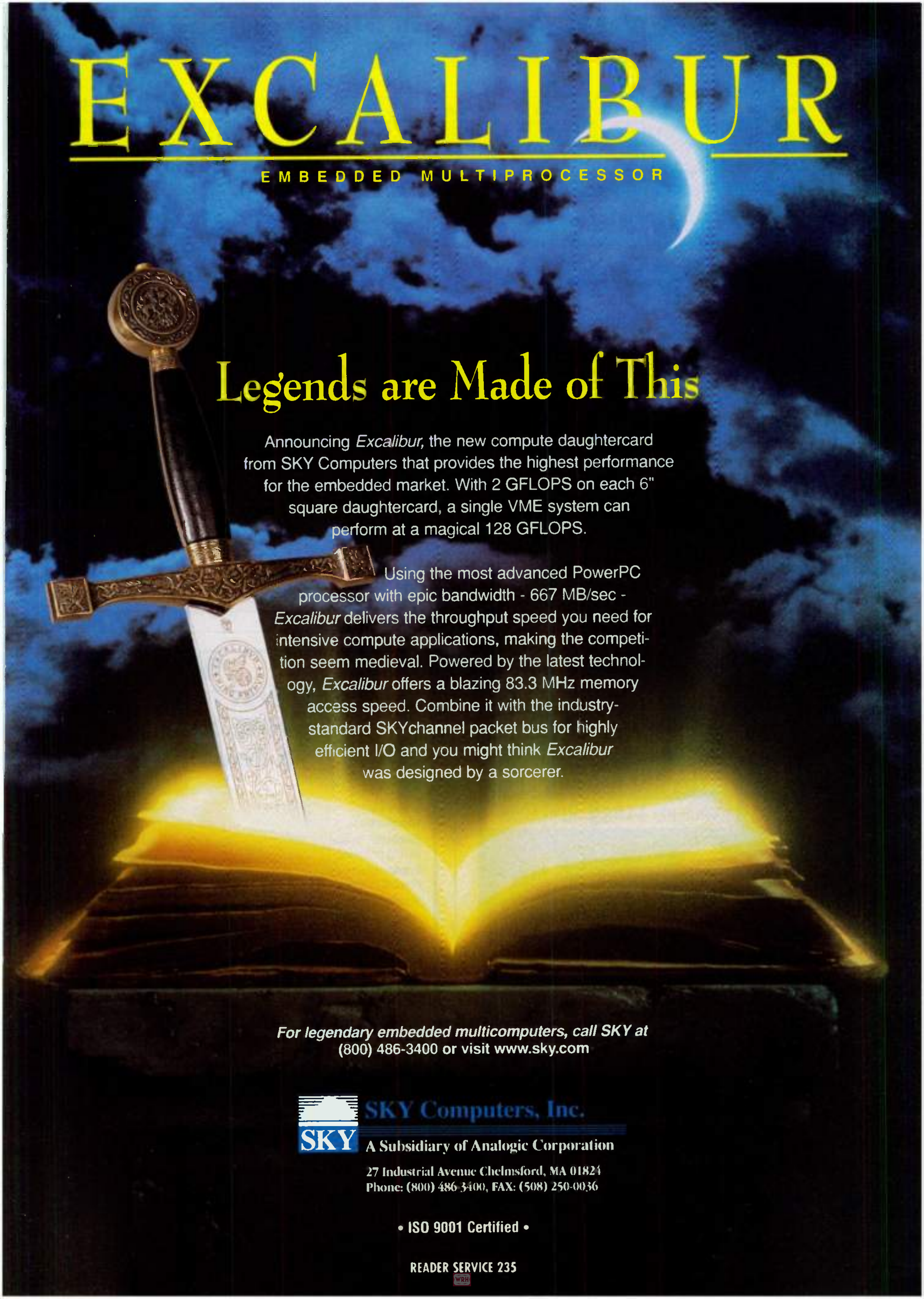
Of importance to the military industry is the simple fact that speed without high reliability is useless. Thus, of all the interconnect technologies available today, the ones that meet the criteria to support data, audio, and video distribution as a high-performance backbone communications bus are FDDI, Fibre Channel Arbitrated Loop (FC-AL), and ATM. FDDI runs at 100 Mbits/s; FC-AL operates in loop mode, with performance scaling from 100 Mbits/s to 1 Gbit/s; and ATM runs at 155 Mbits/s over copper cable and 622 Mbit/s over optical cable *(see the table)*.

Fibre Channel, one of the favorites to overtake 1553, is the generic name for an integrated set of standards defined by ANSI, which defines new protocols for flexible information transfer. It is a multivendor, multiprotocol switched-networked solution best known for its low latency and scalable high speeds. The Fibre Channel architecture is structured as a hierarchical set of five protocol layers, reflecting tremendous reliability and flexibility. It can be implemented using any serial media, including copper coax, twisted pair, or optical fiber.

In terms of adoption, FDDI has seen limited success in the large computer backbone interconnect market, taking over from proprietary solutions. The 100-Mbit/s limitation and high cost of each node adapter have been barriers to mass deployment. Hence, the growth in this market will likely migrate to Fast Ethernet and Fibre Channel. The military has shown some interest in FDDI for naval ship-board



Fibre Channel's arbitrated-loop topology allows up to 127 ports, all connected in a loop. It can be implemented using any serial media, including copper coax, twisted pair, or optical fiber. As a multiprotocol switched network, it offers a low latency and scalable speeds up to 1 Gbit/s.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Parameter	ATM	FDDI	FC-AL	1553
Data rate (Mbits/s)	155-622	100	100-1000	1
Data latency (µs, worst case)	300	36	30	60
Deterministic delivery	No	No	Yes	Yes
Bus initialization time (ms)	10.0	10.0	1.0	0.1
Intelligent nodes required	Yes	Yes	Yes	No
Thermal environment span (°C)	70	130	145	180
Approximate size (in.^{2})	20	12	12	4
Galvanic isolation	No	No	No	Yes, Xformer
Adoption in harsh environments	No	Navy	Air Force	Many
Physical layer	STP	Twinax, fiber	Twinax, fiber	Tri-ax
Guaranteed delivery (ACK)	No	Yes	Yes	Yes
Power, maximum (W)	25	12.5	10	3

applications in which the environment is benign, such as control rooms. The interface also is being evaluated for some vetronics applications.

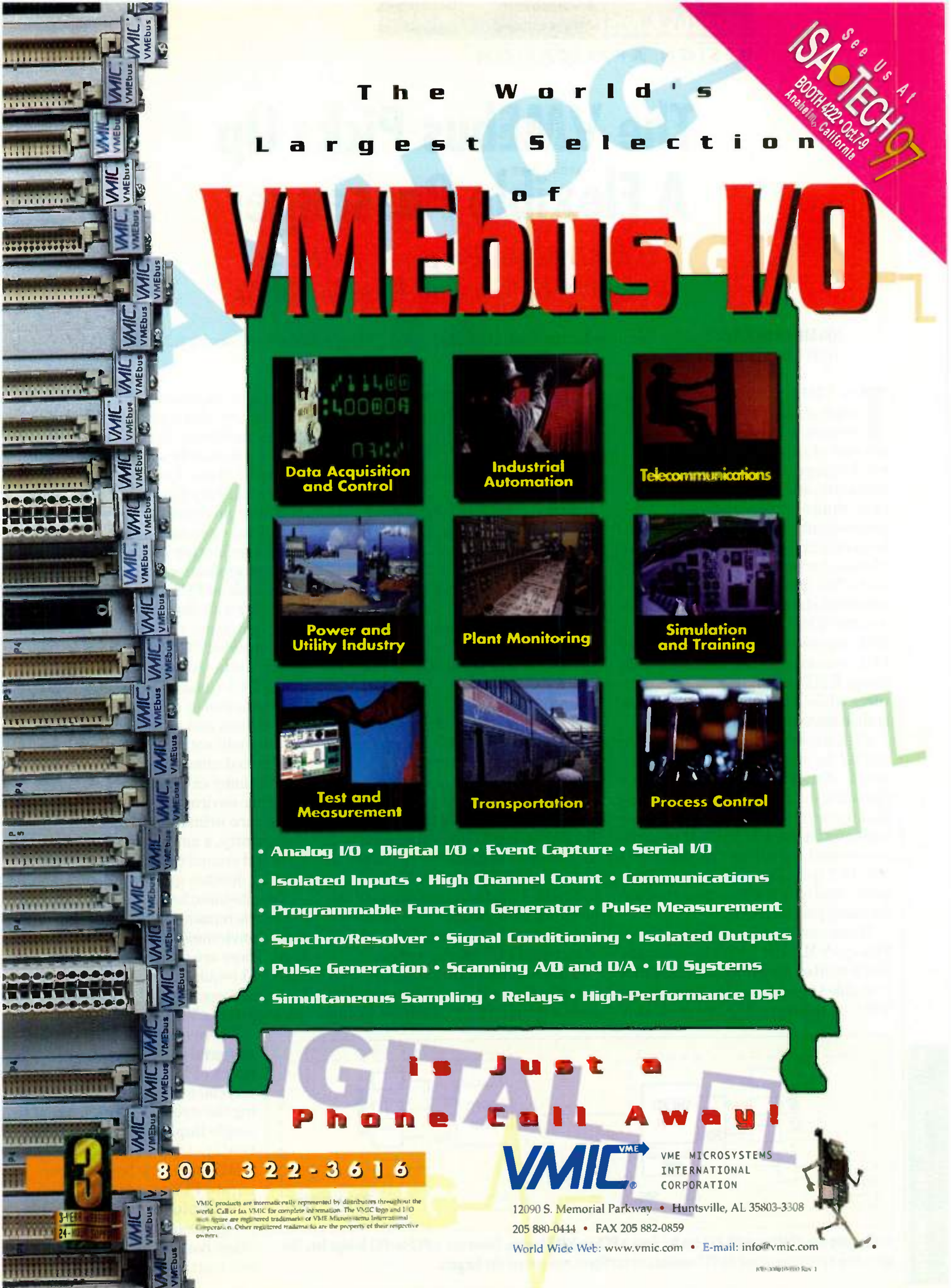
ATM is still an emerging technology, with high costs and standardization delays causing slower than projected adoption for big switch applications. The competition for the desktop connection is between ATM and Fast Ethernet, with promises of Gigabit Ethernet on the horizon. This will likely stall ATM's migration to the desktop and leave it in the telecommunication switch world. One of the early limitations of the ATM was its "lossy" protocol, which makes it less suitable for data when error-free communication is mandatory. The small 48-byte payload format of ATM consumes a lot of overhead for the typical large military data packet such as sensor data.

Fibre Channel, which is gaining popularity within the military industry, offers a high-performance low-latency network with scalable growth. The arbitrated-loop topology allows up to 127 ports, all connected in a serial or loop fashion, and offers good electrical characteristics which lead to higher data rates *(see the figure)*. Also, there's no need for a concentrator, resulting in a lower cost than switched topologies.

John Wemekamp, Director of Strategic Marketing, holds a BS degree from Queens University, Kingston, Ontario, Canada.

Duncan Young, educated in the U.K., is the Director of Marketing for DY 4 Systems.

HOW VALUABLE	CIRCLE
HIGHLY	525
MODERATELY	526
SLIGHTLY	527



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DESIGN APPLICATION

The VMEbus Picks Up A Flexible Passenger

If It's Bridged Properly, PCI Lets Designers Easily Add Functionality.

JONATHAN MORRIS, Tundra Semiconductor Corp., 603 March Rd., Kanata, Ontario, Canada, K2K 2M5; (613) 592-0714.

The VMEbus is celebrating its 16th anniversary this year. Since its inception, it has built up an incredible amount of support, with hundreds of vendors supplying component-, board-, software-, and system-level expertise in a range of environments from process control to medical imaging and telecommunications. The VMEbus' success can be attributed in large part to the fact that the technology has not remained static since its inception. Today, the VME community is exponentially increasing performance, adding PCI connectivity, fault tolerance, hot swap, EMI shielding, and other features while still remaining 100% compatible with earlier generations.

PCI, which has taken the embedded market by storm during the past few years, offers a cost savings from using the software models developed at the desktop level. The ability to leverage tools, platforms, development environments, and code from the desktop is why PCI truly shines in many environments, and why it will continue to do so for many years to come.

However, despite the presence of PCI-to-VME bridges, the software that's written for Windows-based PCs is unable to recognize the presence of VME or the many I/O and processor cards hanging off it. This prevents the operating system from being able to identify all cards in the VME system, bring them up, and appropriately configure them. Even with the latest VME standards (VME64 Extensions, Live Insertion VME, etc.) that extend VME physically toward plug-and-play capability, the software can't leverage it.

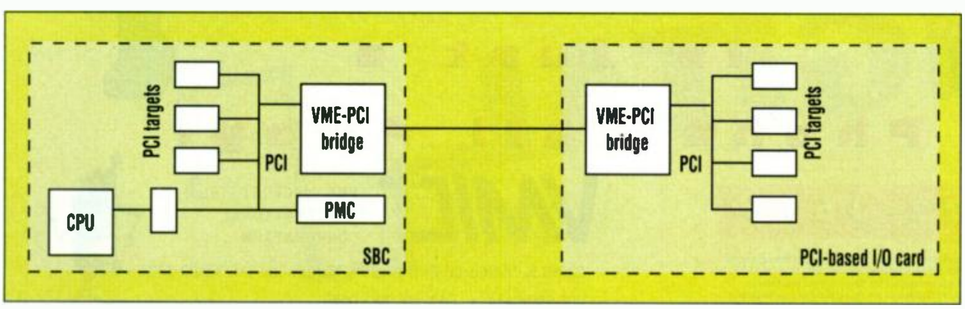
The closest bond between PC-based software and the VMEbus comes in the various flavors of industrial PCI, namely, CompactPCI, sPCI, and PC/104+. However, each of these platforms lack the installed base, investment, and range of suppliers that VME has built.

The support for legacy environments, while certainly a benefit, has sometimes been referred to as VME's Achilles' heel. The requirement for backward compatibility has hampered the growth of the VME specification. However, the PCI specification will impose an even greater straitjacket on embedded PCI platforms. Compliance to the PCI protocol is of primary importance to embedded PCI platforms if they are to leverage the availability of standard PCI interface chips.

This means that embedded PCI specifications are held hostage to the forces within the PCI SIG, a group driven by the needs of the desktop market and that embedded PCI platforms may never be able to evolve except mechanically as the needs of the embedded market changes. It becomes unlikely that features such as real-time processing, multiprocessing, broadcast operations, fault tolerance, or whatever other needs evolve in embedded applications can be addressed by embedded PCI without losing compatibility with desktop PCI.

Other issues remain unaddressed by embedded PCI. For example, a solution for hot swap on passive backplane PCI remains elusive; without the evolution of a new generation of PCI silicon and software, multiprocessing will not happen. In addition, the limited number of interrupts and long latency can cause problems for real-time environments. None of these issues are priorities within the PCI community, a community primarily centered around the needs of the commercial, desktop market.

Despite these issues, embedded PCI standards remain powerful and cost-effective environments for many applications. These are primarily applications that don't require the multi-processing, real-time response, legacy support, or other elements VME offers.



1. Merging the VMEbus with PCI can be done a PCI-to-VME bridge. However, a PCI-to-PCI bridge lets the operating system leverage its PCI routines to configure and control the targets.

There is a way to merge the powerful embedded characteristics of VME with the commercial ones of PCI, leveraging the strengths of each into a single implementation. Currently, the most powerful VME processor boards incorporate PCI as a local I/O bus and employ a PCI-to-VME bridge to access the VMEbus. Other boards in the system often contain a VME bridge,

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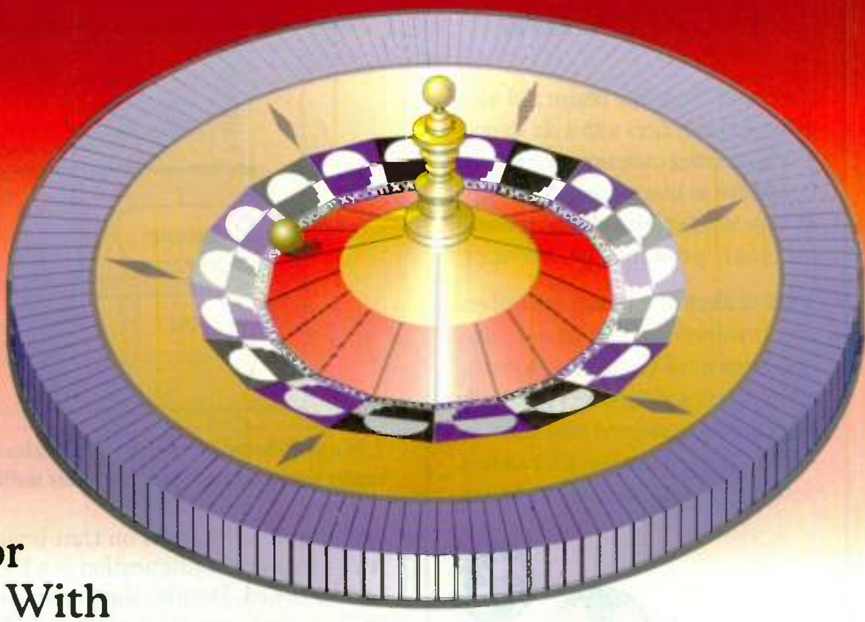

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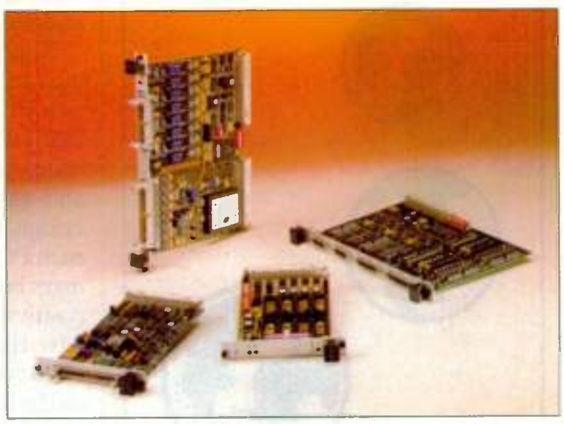

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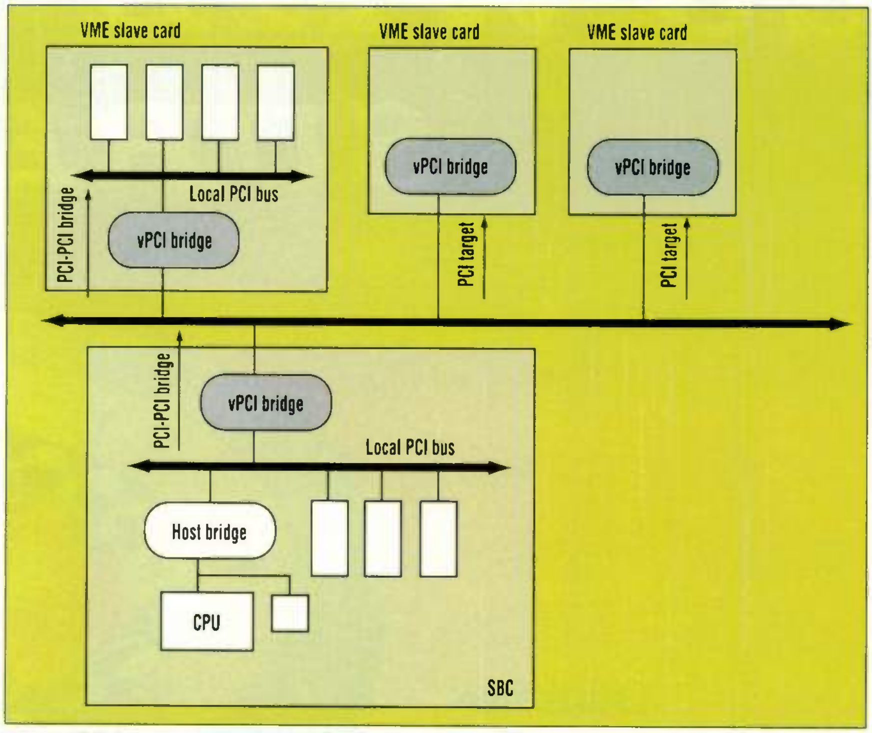
READER SERVICE 225



2. In a vPCI-based system, the VMEbus becomes transparent to the operating system. Up to 21 boards can now be added, using either multiple CPU or other I/O cards.

bridging to a PCI bus on that board. An example of configuration is a PMC carrier board. Despite the presence of PCI on that remote board and PCI targets, the operating system can't leverage its PCI routines to configure and control those targets.

This problem can be solved by having each bridge operate transparently as a PCI-to-PCI bridge *(Fig. 1)*. The VME-PCI bridge on the single-board computer identifies itself to the BIOS and operating system as a PCI-to-PCI bridge. However, instead of translating each PCI cycle on the local bus (its primary bus) into the same cycle on the opposite side (its secondary bus), it translates the cycle into a predefined VME cycle type. Then the VME-PCI bridge on the I/O card, having also identified itself as a PCI-to-PCI bridge, reverse translates that VME cycle back into the appropriate PCI cycle. This mapping can occur for each PCI cycle type: Configuration, memory, and I/O.

That solution makes the operating system aware of other PCI devices residing on VME cards in the system. However, there may be an I/O card that doesn't employ PCI, such as quad T1, ATM, or image-processing cards. These cards should appear to the host as a PCI target. The VME interface on such a card will identify itself as a PCI device using internal registers mimicking the PCI CSRs. From the operating system's perspective, these VME I/O cards have transformed into PCI add-in cards and the card's device driver will be a PCI device driver.

With this type of scheme in place, VME becomes transparent. To the operating system, the entire system becomes PCI-based. The vast wealth of PC-based software is now portable to VME systems. The term term vPCI has been coined to refer to such a system. Multiple CPU cards and other I/O cards could be added, as in any VME system, up to the standard maximum 21-slot limit *(Fig. 2)*. Maintaining the VMEbus allows for the migration of existing VME-based systems, saving investment and effort. These systems can slowly evolve, incorporating vPCI-capable cards as required.

Jonathan Morris, a Product Manager for VMEbus products, holds a BSEE degree from Queen's University, Kingston, Ontario, Canada.

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READER SERVICE 224

WHAT'S ON BOARD

A host of features have been added to a second-generation PCI-to-PCI bridge chip to increase performance. The new features of the PCI2031, developed by Texas Instruments Inc., Dallas, Texas, include burst data transfers and a deeper FIFO buffer. In addition, the chip now meets the requirements of the Advanced Configuration Power Interface (ACPI) and the PCI Bus Power Management specifications, which transfers many of the power-management functions to the operating system. Conforming to these standards ensures that the chip will support the power-management features designed into next-generation PCs, workstations, docking stations, and multifunction PCI-based add-in cards. By employing a PCI-to-PCI bridge, designers can overcome the inherent limit of three to four add-in cards in a PC. The PCI2031's automatic reconnect feature improves overall bus utilization for target devices that can't sustain bursting. Such devices burst large blocks of data using several discrete bursts, rather than one long, continuous burst. The chip helps increase system performance by allowing an initiator, such as an Ethernet or SCSI controller, to reconnect to the chip when the initiator is ready to send more data. The PCI2031 is housed in a 176-pin quad flat pack. For more information, contact Texas Instruments at (800) 477-8924, or on the Internet at http://www.ti.com.

Long life is the hallmark of the TEK-440FX motherboard. Teknor Industrial Computers Inc., Boisbriand, Quebec, Canada, the board's developers, pledge that the motherboard is 100% electrical, mechanical, and BIOS compatible with Intel's VS440FX motherboard. Based on the ATX form factor (9.6 by 12 in.), the TEK-440FX includes a 166- to 200-MHz Pentium Pro microprocessor and the 82440FX PCI chip set. Support is included for up to four IDE devices and two Universal Serial Bus (USB) interfaces. Further expansion is handled using three ISA slots, three PCI slots, and one shared slot. FM synthesis can be added to the board, as well as 256 Mbytes of DRAM, using EDO or fast-page-mode memory. Other features include a parallel and two serial ports, PS/2 keyboard and mouse connectors, and speaker and infrared ports. The TEK-440FX motherboard is compatible with most popular operating systems. For more information, contact Teknor at (800) 387-4222.

Design tools for 16X ATAPI CD-ROM drives are available in a development kit that will reduce overall design costs while speeding time-to-market. Designed by Adaptec Inc., Milpitas, Calif., the kit also gives designers a migration path from ATAPI to SCSI or IEEE 1394 (Firewire). In addition to the necessary firmware, the kit includes the company's AIC-9560, a 16X ATAPI CD-ROM controller chip that offers host transfers up to 20 Mbytes/sec in PIO or DMA modes. It also supports up to 1 Mbyte of DRAM or 256 kbytes of SRAM. The chip gives provides the flexibility to select from various DSPs and between multiplexed and nonmultiplexed microcontrollers, minimizing design changes and maintaining time-to-market. The kit allows for the integration of the AIC-33C94C, which is a SCSI controller, or the AIC-1394, a Firewire controller. Contact Adaptec at (408) 957-4595, or on the Internet at http://www.adaptec.com.

Taking advantage of the K56flex technology developed by Rockwell and Lucent, the Supra PC Card for notebook and handheld computers transfers data at 56 kbits/s. The K56flex protocol is supported by such companies as Ascend, Cisco, Compaq, and Hewlett-Packard, and over 1250 Internet Service Providers. The modem, from Diamond Multimedia Systems Inc., San Jose, Calif., is built with a sleep mode, which minimizes power consumption. The use of flash ROM allows for an upgrade to the prospective ITU standard. Other features include SRAM for accelerated processing, high-speed data-line drivers, an enhanced phone-line interface, and an accelerated PC Card interface that enables a 224-kbit/s throughput. Diamond can be reached at (360) 604-1400 or on the Internet at http://www.diamondmm.com.

Fiber-Optic Module Targets Shared-Memory Applications

Data can be transferred from node to node at speeds up to 10.6 Mbytes/s using the IP-FiberIO IndustryPack module. The card consists of a fiber-optic shared-memory interface on a Type III double-wide IndustryPack mezzanine module. The IP-FiberIO requires no special drivers, protocol stacks, or specialized software. Each IP node carries 512 kbytes of RAM linearly mapped into the hot address space. A write to any location in the node RAM by each host sends a message once around the ring updating all other nodes with the new data. The originating node removes the message from the ring when it receives it. The module is bus-independent and can be integrated into PCI, CompactPCI, VXI, VME, and other bus architectures using an IndustryPack carrier board. IP-FiberIO is available immediately. In quantities of 100, it sells for $2750 each.

GreenSpring Computers, 181 Constitution Drive, Menlo Park, CA 94025; (415) 327-1200; http://www.greenspring.com. **CIRCLE 490**

VMEbus Microcontroller Acts Just Like A PLC

Designed for industrial automation applications, the Smart2 is a second-generation VMEbus controller that's built with a modular concept. While offering the benefits of the VMEbus, the Smart2 adds the functionality of a micro-PLC. The board's COU, field-bus interface, and power supply are all designed as plug-in modules. As a result, the user can choose between field-bus controller, such as Profibus-DP and CAN. The board takes advantage of flash-based memory, simplifying driver updates. The Smart2 board runs the OS-9 operating system, but can be programmed like a PLC with the IS-aGRAF version V3.2 programming tool. Available immediately, the Smart2 controller sells for $827.

Pep Modular Computers Inc., 750 Holiday Dr., Bldg. 9, Pittsburgh, PA 15220; (800) 228-1737 or (412) 921-3322; http://www.pep.de. **CIRCLE 491**

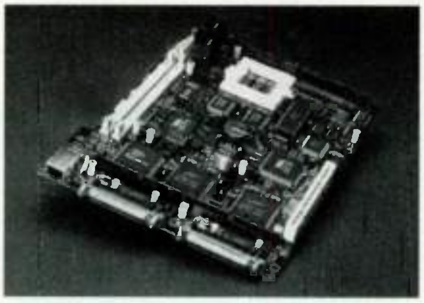
PRODUCT FEATURE

Motherboard Can Be Turned Into A High-Speed Low-Cost File Server

Using the Plug & Stor 100IN motherboard, OEMs can build file servers that boost network performance by supplying local access to shared mass-storage resources. Built with a Pentium microprocessor, the motherboard is optimized for high-speed file-server tasks and can manage printing requests for PCs and network computers (NCs) on a network.

The Plug & Stor 100IN offers a host of connectivity options. These include a 10- or 100-Mbit/s Ethernet port, two UltraSCSI wide interfaces (each interface can handle up to 14 devices), and an internal IDE port. The board is designed to operate as a standalone dedicated file server or as a network-attached storage device that's focused on network file access. Two SIMM sockets also are supplied.

The motherboard's operating system is embedded in nonvolatile memory. As a result, the OEM needn't handle any disks and there are no software licenses to manage. Upgrades can simply be downloaded to the board over the Internet. The operating system, called Embedded Server Architecture (ESA), includes a complete file system



that stores and retrieves information from any type of disk drive. There's also a print server that manages printing requests from any system on the network. A TCP/IP software layer communicates with web browsers.

Systems that are attached to the Plug & Stor network can run a variety of operating systems, including Windows NT, Windows 95, Windows 3.1, OS/2, DOS, or Unix. Unlike a traditional Windows NT file server, which is designed for general-purpose computing, the Plug & Stor is aimed directly at file-retrieval applications.

The setup process for the Plug & Stor is simple. Upon booting, the board gives the user the choice of setting up the disk drives as a RAID 1 array with mirroring for some degree of fault tolerance or as a standard disk drive. It also lets the user add password protection. An unpopulated version of the board is available now for $660 each in lots of 50. In a self-contained box with no storage (the Plug & Stor 100EX), the unit sells for $799 in similar quantities.

Creative Design Solutions Inc.
3350 Scott Blvd.
Building #9
Santa Clara, CA 95054
(408) 653-1330
http://www.creativedesign.com
CIRCLE 554
RICHARD NASS

Users Can Employ A RAID Subsystem Simply By Adding A SCSI Host Adapter

Users wishing to employ a RAID subsystem now need only turn to their SCSI host adapter if it's equipped with RAIDPlus, an enhancement to an existing line of host adapters. RAIDPlus, developed by Mylex Corp., increases the performance, security, and accessibility to data for small-office, home-office applications.

According to the company, adding RAID and a second disk drive to a server can increase data throughput up to 96%. By adding two drives, performance can be increased up to 143%. In a typical PC LAN, the greatest performance bottleneck occurs during the data-retrieval time. RAIDPlus allows for the connection of up to eight drives per host adapter.

Distributing data across multiple drives increases the security of the data. If there's a drive failure, RAIDPlus can recreate the lost data from information stored across the rest of the system. The firmware allows for RAID levels 0 (striping), 1 (mirroring), and 0+1 (striping and mirroring).

RAIDPlus firmware can be added to existing Mylex SCSI host adapters for $99. Alternatively, it comes bundled with the FlashPoint line of host adapters, which range from $179 to $499. It ships with drivers for Windows 95, Windows NT, and DOS. A utility is included to ease installation and configuration.

Mylex Corp.
34551 Ardenwood Blvd.
Fremont, CA 94555
(510) 796-6100
http://www.mylex.com
CIRCLE 555
RICHARD NASS

RF-Based Wireless Terminal Keeps Users Connected To Server

Within a predefined area, the Winterm 2930 wireless terminal maintains complete Windows functionality and access to the server in its 3.4-lb. package. Measuring about 10.6 by 9.8 by 1 in. (sloping to 1.8 in. at the rear), the battery-powered device lets users roam through a facility and communicate with the server at a distance of up to 1000 ft. For longer distances, hubs can be employed, with each hub extending the distance by 1000 ft.

The platform is compatible with DOS, Windows 3.1, Windows 95, and Windows NT. In addition, it can be combined with a multi-user operating system, such as WinFrame from Citrix Systems, or NTrigue from Insignia Solutions. Typical applications include medical facilities, inventory access, point-of-sale situations, or other places that require real-time access to a large local database. Because the data remains on the server, not the

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PRODUCT FEATURE

(continued from page 172)

client, there are no security issues that have to be dealt with.

The Winterm 2930's communications are handled by a 2.4-GHz spread-spectrum RF LAN. Compliance is maintained with the ICA 3 protocol for data transmit and receive. A pen-enabled touchscreen is combined with an 8.5-in. backlit color display (VGA resolution with 16 or 256 colors) to facilitate user input. Using a lithium-ion battery, the device can run for up to 8 hrs. on a charge. A built-in sleep mode further extends the battery life.

External peripherals can be connected to the Winterm 2930. A PS/2 port is available to employ an input device, such as a keyboard or mouse. A serial port also is available. The unit functions in temperatures ranging from 5° to 50°C. Available now, it sells for under $3000.

Wyse Technology Inc.
3471 North First St.
San Jose, CA 95134
(800) GET-WYSE or (408) 473-1200
http://www.wyse.com
CIRCLE 556
RICHARD NASS

2.5-in. Hard-Disk Drive Stores 2.1 Gbytes Of Data

Although it fits in a 2.5-in. form factor, the Marathon 2130s1 hard-disk drive stores 2.1 Gbytes of data. Aimed at portable platforms, the drive measures just 12.5 mm high. It features a 12-ms seek time, a 4500-rpm spindle speed, and an internal data rate of 71.3 Mbits/s. As a result, it can handle the current wave of multimedia applications that are bursting with audio, video, and graphics. The drive's high capacity comes from the use of magnetoresistive (MR) heads and a glass media that's resistant to non-operating shocks. It also enjoys a reinforced base casting for further reliability and sound-proofing. Operational shocks up to 125 g can be handled using the company's SafeRite shock-sensor technology. If the drive experiences a shock greater than 10 g, the write circuit shuts down, preventing overwrite of adjacent data tracks. RN

Seagate Technology Inc., 920 Disc Dr., Scotts Valley, CA 95066; (408) 439-2862; http://www.seagate.com.
CIRCLE 557

200-MHz MMX Pentium VME Fits Into One Slot

One VMEbus slot is all that's needed to hold the VS SBC/PMx, a 200-MHz MMX Pentium CPU board. Up to 64 Mbytes of 64-bit-wide EDO DRAM can be installed on the board using standard SIMMs. Up to 1 Mbyte of flash EPROM is available for the user, while an additional 512 kbytes of flash hold the system BIOS. An Ultra-SCSI, SCSI-2, or SCSI-1 interface is provided using the Symbios Logic 33-MHz 53C860 SCSI processor. The interface supports single-ended asynchronous or synchronous transfers with active termination and signal negation, resulting in data rates up to 20 Mbytes/s. The interface is accessed through a P2 DIN connector. The Ethernet interface (IEEE 802.3 10Base-5) is implemented with an AMD 79C970A device. This interface is accessed using a 15-pin D-Connector. A front-panel graphics interface provides resolutions up to 1600 by 1200 pixels with a 2-Mbyte EDO frame buffer. Other peripheral interfaces included on the board are two serial channels, keyboard and floppy-disk interfaces, and a parallel port. Further expansion is handled using dual PMC modules. Operating-system support includes VxWorks, Windows 95, and Windows NT.

***Concurrent Technologies Inc.**, 10921 Reed Hartman Hwy., Cincinnati, OH 45242; (513) 791-0073; Internet: http://www.gocct.com.* **CIRCLE 590**

Analog Input Board Suits High-Precision Applications

High-precision applications, such as sonar, vibration analysis, and instrumentation, are the targets for the ICS-110B 32-channel, 100-kHz, 24-bit analog input VMEbus board. The board also offers an optional signal-conditioning daughterboard, while maintaining a single-width 6U VMEbus form factor. The sigma-delta converter used on the board provides a small sampling skew between channels and simplifies the anti-alias filter requirements. The result is a maximized signal bandwidth that can be sampled for a given sampling frequency. The ICS-110B includes a VME slave interface with D32 block-transfer (BLT) capability and a 160-Mbytes/s front-panel data-port (FPDP) interface.

The board supplies simultaneous sampling on all channels and permits up to 32 boards to be synchronized using a front-panel local-bus connector, for up to 1024 channels of analog data. The ICS-110B includes a 64-ksample FIFO memory with half-full, full, and empty status flags. If the FPDP interface is employed, data automatically flows to the receiving DSP or CPU board without intervention from the controlling processor. The optional daughterboard features independently programmable gain control of -95.5 to +31.5 dB in steps of 0.5 dB on each channel. Relays allow an internally or externally generated analog calibration signal to be applied to all

(continued on page 178)

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channels for performance monitoring and fault location. Prices start at $3595.

Interactive Circuits and Systems Ltd., *5430 Canotek Rd., Gloucester, Ontario, Canada, K1J 9G2; 800-267-9794 or 613-749-9241; http://www.ics-ltd.com.* **CIRCLE 591**

VME-To-PCI Bridge Increases Performance And Flexibility

The next generation of the Universe VME-to-PCI bus bridging chip, called the Universe II, includes additional programming resources, increased data-transfer rates, and lower power consumption, while maintaining full Universe backwards compatibility. As a result, existing Universe users can gain higher performance without a complete redesign. Universe II can handle the memory-address orientation of the VMEbus as well as real-time and message-oriented architectures by employing a flexible interrupt structure. It adds mailboxes, location monitors, and seven software-initiated interrupts. Telecommunications applications will especially benefit from these features. In addition, the Universe II supports eight semaphores for simultaneous sharing of resources between system processes to better support multiprocessing applications. Other features include bus parking, improved arbitration mechanisms, lower overhead on linked-list DMA transfers, and longer PCI transactions to ensure that the bus bridge doesn't become the limiting factor in system performance. Deep FIFO's provide maximum bandwidth on both buses even when operating with high latency targets. The Universe II, housed in a 313-pin BGA package, is available for $160 each in lots 1000 pieces.

Tundra Semiconductor Corp., *603 March Rd., Kanata, Ontario, Canada K2K 2M5; (800) 267-7231 or (613) 592-0714; http://www.tundra.com.* **CIRCLE 592**

PMC Modules Supply Flexible Low-Cost T1, E1 Interfaces

Users can get T1 or E1 functionality in a PMC form factor using the PM/T1 and PM/E1 modules, which plug into a standard VMEbus or custom base-
(continued on page 180)

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READER SERVICE 135

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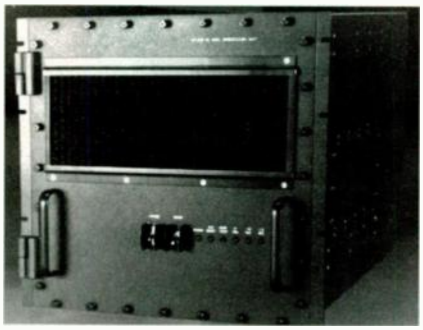
board. The modules can be employed in both voice and signaling applications, enabling users to transport multiplexed voice and signal data from one system to another over one standard interface. The interfaces can carry up to 48 (T1) or 60 (E1) voice channels from system to system and can carry signaling information such as SS7 or a combination of voice and signaling data. The modules are designed around the Motorola MPC860MH (PowerQUICC) processor, configured with 4 or 8 Mbytes of memory. Protocol support includes HDLC LAPB, LAPD, and LAPF, as well as SS7 MTP1 and MTP2. The PM/T1 and PM/E1 modules support the VxWorks real-time operating system. Future support will include the pSOS operating system. The PMC modules are fully compliant with FCC Part 68, ensuring a proper connection to the Public Switched Telephone Network (PSTN). Available immediately, the PM/T1 and PM/E1 modules sell for $816 each in lots of 1000.

***Computer Products Inc., Heurikon Div.**, 8310 Excelsior Drive, Madison, Wis. 53717; (608) 831-5500 or (800) 356-9602; http://www.heurikon.com.*
CIRCLE 593

VMEbus Enclosure Meets Rugged Specs

If you're looking for a ruggedized 18-slot VMEbus enclosure, look no further than the FS-8918. The enclosure features an internal space to mount

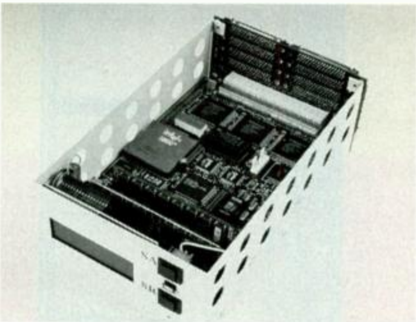


three 5.25-in. half-height drives and three 3.5-in. drives. A hinged door offers front-loading access to the peripherals, while the VME boards are loaded from the top. Up to six SCSI devices can be connected from the front panel, while the rear I/O panel can be custom configured for a particular application. Cooling occurs from front to rear, and thermal monitoring and control is available as an option. An 800-W power supply is included. The FS-8918 meets MIL-STD-810E, MIL-STD-901D, and MIL-STD 167/1 shock and vibration specifications for severe environments, and MIL-STD-461C for EMI requirements. The enclosure is available in a rack-mount or desktop configuration. Prices start at $14,950.

***AP Labs**, 5871 Oberlin Dr., San Diego, CA 92121; (619) 546-8626; http://www.sd.aplabs.com.*
CIRCLE 594

RAID Controller Increases Speed And Functionality

Designed specifically for demanding database and multimedia applications, the Regency SCSI RAID controller works with any operating system and boasts specifications of 40 Mbytes/s in burst mode, 34 Mbytes/s in sustained



read mode, and 31 Mbytes/s in sustained write mode, all at RAID level five. The controller supports RAID levels 0, 1, 0+1, 3, 4, and 5. Powered by a 40-MHz i960CF RISC processor, the Regency comes with eight UltraSCSI wide channels, two of which are dedicated to the host. As a result, multiple database servers operating at different RAID levels can use the same array. In addition, the dual host feature allows multiple Regencys to be connected in series. To protect against controller failure, two Regency controllers can be connected to the same array, thereby providing redundancy. Rather than a slave-master or mirroring configuration, the arrays operate independently in an active-active mode, which also increases read and write speeds. Available now, the Regency SCSI RAID controller sells for $4500.

***Syred Data Systems**, 272 Lanes Mill Rd., Howell, NJ 07731; (908) 886-1400; http://www.syred.com.*
CIRCLE 595

ATM On A PMC Offers Real-Time Capabilities

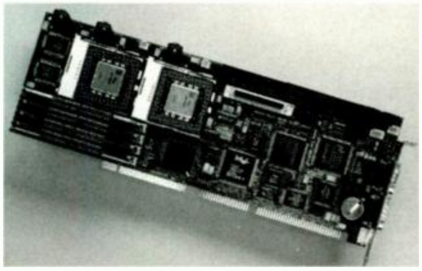
The CPMC-ATM gives VMEbus system designers a solution for direct connectivity to ATM local- and wide-area networks. The module offers high bandwidth, low-delay packet switching, and multiplexing of voice, video, and data for network applications ranging from military command and control to commercial data communications. The CPMC-ATM was specifically designed to provide deterministic network-access times, scalable bandwidth, and high-speed ATM networking capabilities up to 155 Mbits/s. The module's flexibility lets designers select from common physical interfaces or ATM networks, including 155-Mbit/s STS-3C on single- or multimode fiber optics, UTP5 155-Mbit/s STS-3c, and 25-Mbit/s UTP3. The CPMC-ATM also features a 4K VP/VC segmentation and reassembly controller, a feature that's needed for telecommunication applications. The module also provides Constant Bit Rate for real-time applications and Available Bit Rate for handling congested networks. The card comes bundled with an ATM software stack that includes LAN emulation, classical IP, RFC1483 IP over ATM, ATM Forum UNI3.1 signaling, and network-management utilities. Available immediately, the CPMC-ATM sells for $790.

***Cetia Inc.**, 58 Charles St., Cambridge, MA 02141; (617) 494-0987; http://www.cetia.com.* **CIRCLE 596**

Pair Of Pentium Microprocessors Drive SBC

Two 233-MHz Pentium MMX microprocessors drive the PCpd233 single-board computer (SBC), which conforms to the PICMG 2.0 specification. Typical applications include high-end file servers, communications and telephony systems, medical equipment, industrial controls, factory automation, and instrumentation and mea-
(continued on page 182)

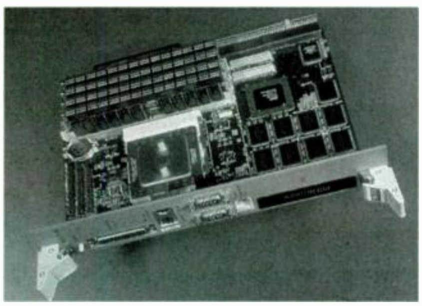
(continued from page 180)
surement systems. Features of the board include 512 kbytes of burst cache memory, 512 Mbytes of ECC RAM, a wide UltraSCSI adapter capable of 40-Mbyte/s transfers, and integrated SVGA that can handle simultaneous CRT and flat-panel displays. Peripherals connect directly to the board's PCI bus, the dual EIDE interfaces, or the two USB ports. Independent temperature monitoring is available for each microprocessor. Equipped with Phoenix BIOS, the PCpd233 offers an autoconfiguration utility.



***Industrial CPU Systems Inc.**, 111-D W. Dyer Rd., Santa Ana, CA 92707; (714) 957-2815.* **CIRCLE 597**

CompactPCI Is Fueled By 500-MHz CPU

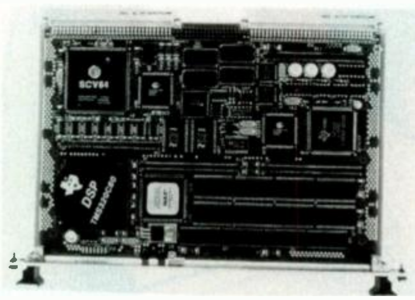
A DEC Alpha 21164 microprocessor running at 500 MHz forms the backbone of the SBC/P164 CompactPCI single-board computer. It boasts performance specifications of 15.4 SPECint95 and 21.1 SPECfp95. The board features 64 to 512 Mbytes of DRAM on a 256-bit-wide memory bus, 1 or 2 Mbytes of 12-ns tertiary cache memory, and a 64-bit PCI bus. The 6U form factor dual-slot board also contains a parallel and two serial ports, keyboard and mouse interfaces, and a PMC slot. Initially, the board will run the Windows NT operating system. By the fourth quarter, the board will support Digital Unix and VxWorks. The board also is available in a system-level tower configuration. This includes VGA graphics, a 2.1-Gbyte hard-disk drive, and a CD-ROM drive. Two 64-bit user slots are left free. A second configuration puts the SBC/P164 in a 19-in. rack. Here, six slots are available to add CompactPCI boards plus a second CompactPCI or VMEbus backplane.



***Alta Technology Corp.**, 9500 South 500 West, Suite 212, Sandy, UT 84070; (801) 562-1010; Internet: http://www.altatech.com.* **CIRCLE 598**

VME Board Displays Graphics, Video, On Dual Displays

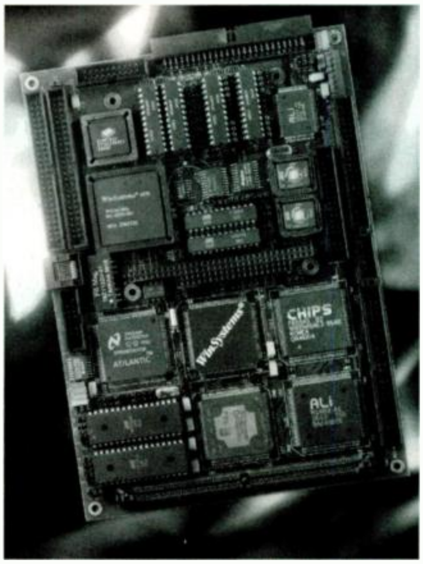
The SVME/DMV-783 VME-based graphics controller is suited for operation in harsh environments in both military and commercial applications. Designed for high-speed and imaging-processing tasks, the single-slot board is built with a TI 320C80 processor and can simultaneously update dual displays, perform high-resolution RGB/NTSC frame grabbing, and gather high-speed data from radar sets and remote sensors. The high level of performance comes from the use of two separate frame buffers and two video digital-to-audio converters (DACs). Analog and digital video overlay features allow graphics and text to be mixed with live video displays. The bundled software includes command lists, transformations, and development tools. Different versions of the board are available, depending on the user environment. Prices for the SVME/DMV-783 graphics controller start at $11,000.



***DY 4 Systems Inc.**, 333 Palladium Dr., MS 212, Kanata, Ontario, Canada K2V 1A6; (613) 599-9199; Internet: http://www.dy4.com.* **CIRCLE 599**

SBC Operates Over Wide Temperature Range

The LBC-586Plus-133 single-board computer is aimed at an exploding market—the Internet and intranets. What's unique about the low-cost board is that it operates over an extended temperature range, from -40 to +70°C. Built with a 133-MHz AMD 5x86 microprocessor, the board supports a host of software tools, including networking operating systems, Web browsers and servers, device drivers, and libraries. As a result, there's no need to develop custom networking software.



Features of the LBC-586Plus, which measures 5.75 by 8.0 in., include, a video controller with CRT and flat-panel support, a 10-Mbit/s Ethernet controller, four serial ports, a real-time clock, floppy- and hard-disk interfaces, 48 bidirectional I/O lines, and solid-state-disk support. In addition, a 16-bit PC/104 connector is available to support expansion modules. Up to 64 Mbytes of DRAM can populate the board using standard 72-pin SIMMs. A 256-kbyte secondary cache is available as an option. Two 32-pin memory socket are available to plug in EPROM, SRAM, or flash memory.

The board requires a +5-V supply and typically draws 2.0 A. List price for the LBC-586Plus-133 is $895.

***WinSystems Inc.**, 715 Stadium Dr., Arlington, TX 76011; (817) 274-7553; http://www.winsystems.com.* **CIRCLE 600**

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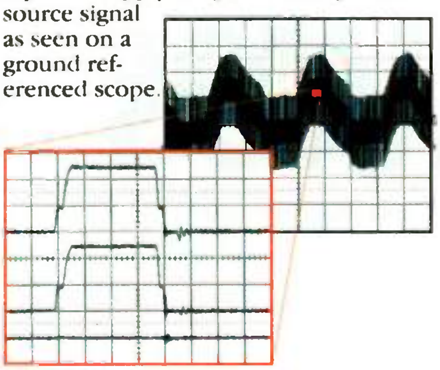

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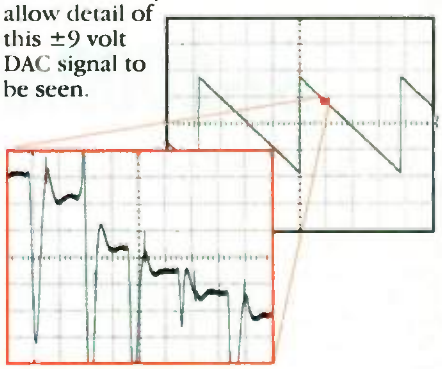
CONVENTIONAL
A scope lacks sufficient position range and lacks the ability to recover from overdrive to allow detail of this ±9 volt DAC signal to be seen.



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POS-50	25-50	-110	-19	20	11.95
POS-75	37.5-75	-110	-27	20	11.95
POS-100	50-100	-107	-23	20	11.95
POS-150	75-150	-103	-23	20	11.95
POS-200	100-200	-102	-24	20	11.95
POS-300	150-280	-100	-30	20	13.95
POS-400	200-380	-98	-28	20	13.95
POS-535	300-525	-93	-26	20	13.95
POS-765	485-765	-85	-21	22	14.95
NEW POS-900W	500-900	-95	-26	25	16.95
POS-1025	685-1025	-84	-23	22	16.95
POS-1060	750-1060	-90	-11	30*	14.95
POS-1400	975-1400	-95	-11	30*	14.95
POS-2000	1370-2000	-95	-11	30*	14.95

*Max. Current (mA) @ 8V DC.

Notes: Tuning voltage 1 to 16V required to cover freq. range. 1 to 11V for POS-25, 1 to 20V for POS-1060 to -2000. 3dB modulation bandwidth for POS-25 is 60kHz, POS-50 to -1025 is 100kHz, and POS-1060 to -2000 is 1MHz (all typ). Operating temperature range: -55°C to +85°C. 5V tuning models available. Consult RF/IF Designer's Guide or call Mini-Circuits.

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Circle 520

High-Voltage Adjustable Shunt Regulator

DON BRAY
Horton Automatics, 4242 Baldwin Blvd., Corpus Christi, TX 78405.

Occasionally, the need arises for a variable shunt regulator capable of high-voltage operation. At high voltages, multiple transistors in series overcome safe-operating area (SOA) limitations much more effectively than parallel configurations. However, with linear operation, ensuring equal power dissipation between the devices at all times can be a problem. If one device has slightly higher gain, it will minimize the voltage across itself. This leaves the other transistors with more than their share of the load, potentially exceeding their SOA boundaries.

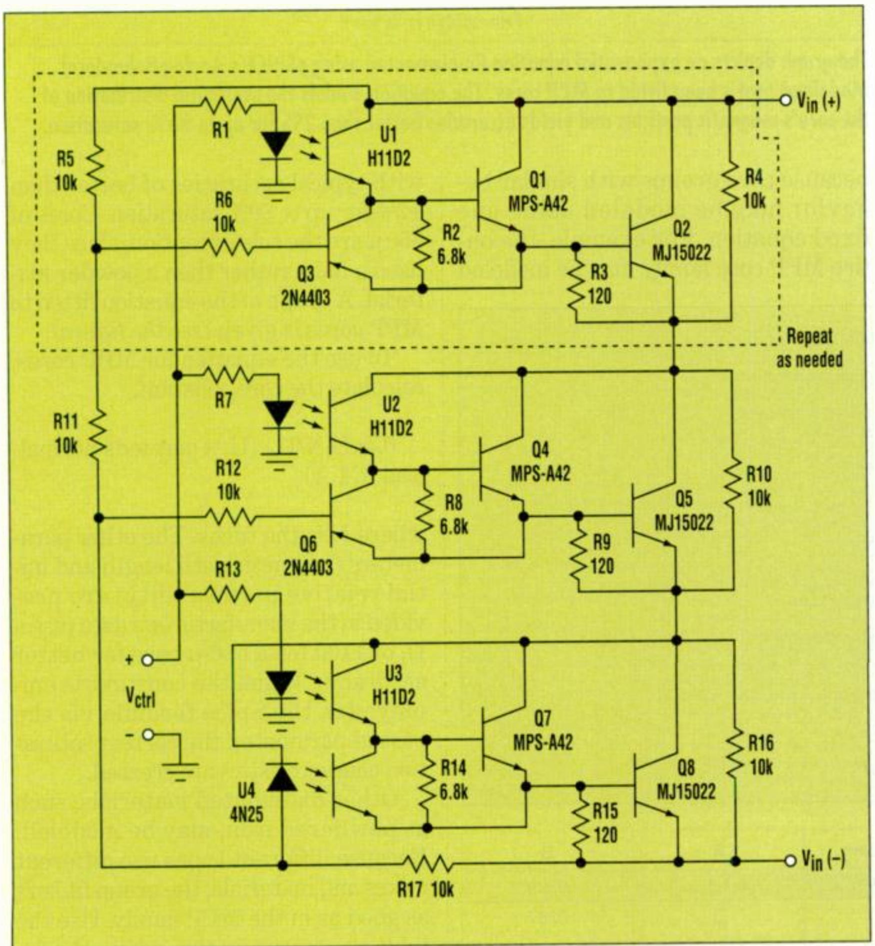
The circuit shown is optimized for high-voltage adjustable shunt regulation and includes a self-balancing feature to help equalize the voltage drops across the devices used *(see the figure)*. Furthermore, the circuit's voltage range may be extended by cascading additional stages if required.

Each stage of the regulator circuit consists of a high-voltage optocoupler (U1), driver transistor (Q1), and pass transistor (Q2) connected in an extended Darlington configuration. The control voltage (V_{ctrl}) is applied to U1 via resistor R1 and adjusts the current drawn by Q2. Resistors R2 and R3 add stability by swamping the leakage current. Resistors R4, R10, and R16 force the voltage drops to be equal across all stages when control voltage V_{ctrl} is zero and the power devices aren't conducting.

Identical resistors R5, R11, and R17 are series-connected across V_{in}. Therefore, the voltage at the junction of R5 and R11—and the voltage at Q3's base—is 2/3 of V_{in}. If the circuit is balanced properly, the voltage at the emitter of Q2 also will be 2./3 of V_{in}. The emitter voltage of Q3 is the same as the base voltage of Q2, which will be nominally (2/3 V_{in}) + 0.7 V. Hence, Q3 is just barely biased on when the circuit is balanced properly. If Q2's emitter voltage *rises* relative to the reference, Q3's base-emitter voltage also rises. The transistor shunts a larger portion of Q1's base drive, restoring the circuit's balance. If Q2's emitter voltage *drops* relative to the reference voltage, the net effect is to reduce the voltage across all of the other stages. This increases the bias on their balancing devices and again maintains equal collector-emitter drops.

On all stages except for the last one, the balancing circuit monitors the differential between the emitter of the power device (plus 0.7 V as explained before) and the reference voltage from the divider chain. This isn't possible with the last stage, since its emitter is connected directly to the low side of V_{in}. An isolated device for sensing the differential is therefore required. To balance the final stage, optocoupler U4 is used instead of a transistor. U4 monitors the differential between the collector of Q8 and a reference voltage of 1/3 V_{in}. If the collector voltage of Q8 falls below the reference voltage, U4 begins coming on. This performs an identical function to Q3, shunting base current away from driver transistor Q7 and restoring proper balance.

A four-stage version of this circuit was bench-tested using a 160-V dc input at varying currents up to approximately 2.0 A. The voltage drops across the power devices remained balanced to within 5% of the desired 40 V dc at all times. Obviously, at these power levels, a very generous heat sink (on the order of 1°C/W per device) is required.



Optimized for high-voltage adjustable shunt regulation, this multi-stage circuit includes a self-balancing feature to help equalize the voltage drops across the transistors in each stage.

Circle 521

Simple Spice File Models All Powdered Inductors

KEVAN O'MEARA
KO Systems, 10437 Laramie Ave., Chatsworth, CA 91311; (818) 341-3864.

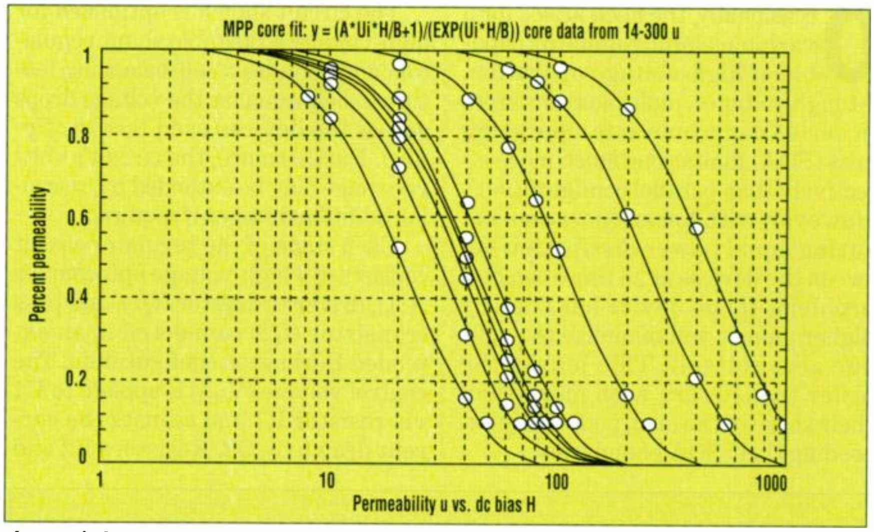
VOTE!

Read the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a $150 Best-of-Issue award.

The Spice file shown allows saturating inductors such as MPP or powdered iron cores to be modeled with relative ease. Such inductors are very common, but they feature a gradual saturation characteristic that's difficult to model even using the "real" core materials provided with some Spice programs. The model gives accurate results from no load (no saturation) to full saturation, with proper behavior at the limits. It's useful for modeling power-supply filters during large dynamic (inrush, step load) conditions.

At the heart of the model is a simple exponential equation implemented using pSPICE's Analog Behavioral Modeling. Not empirically derived, it's based on an equation that models the statistical distribution of the core's magnetic particles. Integrating the base equation gives the percent saturation (integrating it once more would give the BH characteristics).

The equation is particularly useful because core groups with similar behavior may be modeled using one fixed equation. For example, the entire MPP core family may be modeled with typical accuracies of better than ±2% for up to 80% saturation. Cores of 550 µ are the sole exception, since they used a flake rather than a powder material. A graph of the equation fitted to MPP cores is given *(see the figure)*.



The graph depicts an exponential equation (implemented using pSPICE's Analog Behavioral Modeling) that's been fitted to MPP cores. The equation models the statistical distribution of the core's magnetic particles and yields accuracies better than 2% for up to 80% saturation.

To use the equation for MPP cores, calculate the core constant:

$0.4\pi U_i N/L_m$ ($U_i \times$ oersteds normalized to 1 A)

where N is the turns. The other parameters (magnetic path length and initial relative permeability) are provided in the manufacturer's data (use a U_i of 1100 for a 550-µ core for better accuracy). When the constant is employed in the Spice formula via the passed parameter, the correct saturation characteristics are created.

Other distributed materials, such as powdered iron, may be modeled. Because different types use different mixes and materials, the group fit isn't as good as in the MPP family. Use the table as a starting point, where the degree of the fit also is indicated by the Chi Square results.

```
SPICE SATURATING CORE MODEL
LDRIVE Lin 0 {Lno_load}      ;Base (no load) inductance value
XLSAT1 Lin Lout1 Lout2 XLSAT PARAMS:Kcore={core_constant}
                             ;Saturating inductance
;**********************************************
;* saturating core subcircuit          *
;* 1-0 base inductance Li @ I=0                *
;* 2-3 output saturating inductance            *
;**********************************************
.subckt XLSAT 1 2 3 params:Kcore=100
                             ;MPP core constant = {.4 pi N Ui / Lm}
                             ;lower = less saturation
eout 2 4 value =             ;curve fit for all MPP cores
 + {v(1,0)*(1.1/3529*Kcore*abs(I(vsense))+1)
 + /(exp(Kcore*abs(i(vsense))/3529))}
                             ;keep equation on one line for PSPICE
fcopy 0 1 vsense 1
vsense 4 3 0
.ends                        ;end of subcircuit
```

Material Family	Manufacturer	Chi Square	A	B
MPP toroid	Mag Inc.	0.33	1.1	3529
Cool saturation toroid	Mag Inc.	1.1	0	9257
Powdered iron	Micrometals	0.47	0.6	4971

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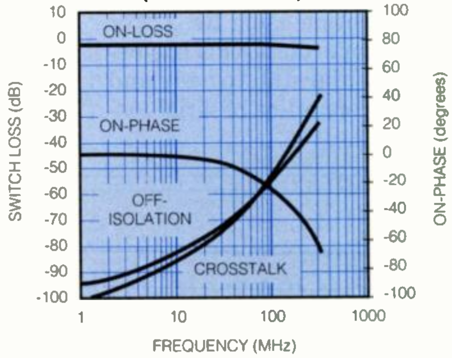
MAX4567 FREQUENCY RESPONSE (50Ω IN AND OUT)



Choose the Best Video/RF Switch for Your Application

PART	FUNCTION	R_{ON} (Ω max)	R_{ON} MATCHING (Ω max)	R_{ON} FLATNESS (Ω max)	OFF-ISOLATION 10MHz/100MHz (dB typ)	CROSSTALK 10MHz/100MHz (dB typ)	THD (%)	PACKAGES
MAX4545	Quad SPST	20	1	0.5	80/50	-88/50	0.004	20-Pin DIP, SOIC, SSOP
MAX4546	Dual SPDT	20	1	0.5	80/50	-80/50	0.004	16-Pin DIP, SOIC, QSOP
MAX4547	Dual SPDT (High-Isolation Pinout)	20	1	0.5	82/55	-84/55	0.004	16-Pin DIP, SOIC, QSOP
MAX4565	Quad SPST	60	2.5	2	80/55	-80/55	0.02	20-Pin DIP, SOIC, SSOP
MAX4566	Dual SPDT	60	2.5	2	80/55	80/55	0.02	16-Pin DIP, SOIC, QSOP
MAX4567	Dual SPDT (High-Isolation Pinout)	60	2.5	2	-83/55	-87/55	0.02	16-Pin DIP, SOIC, QSOP

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Circle No. 164 - For U.S. Response
Circle No. 165 - For International

Circle 522

Use Your Serial Port For Isolated Data Acquisition

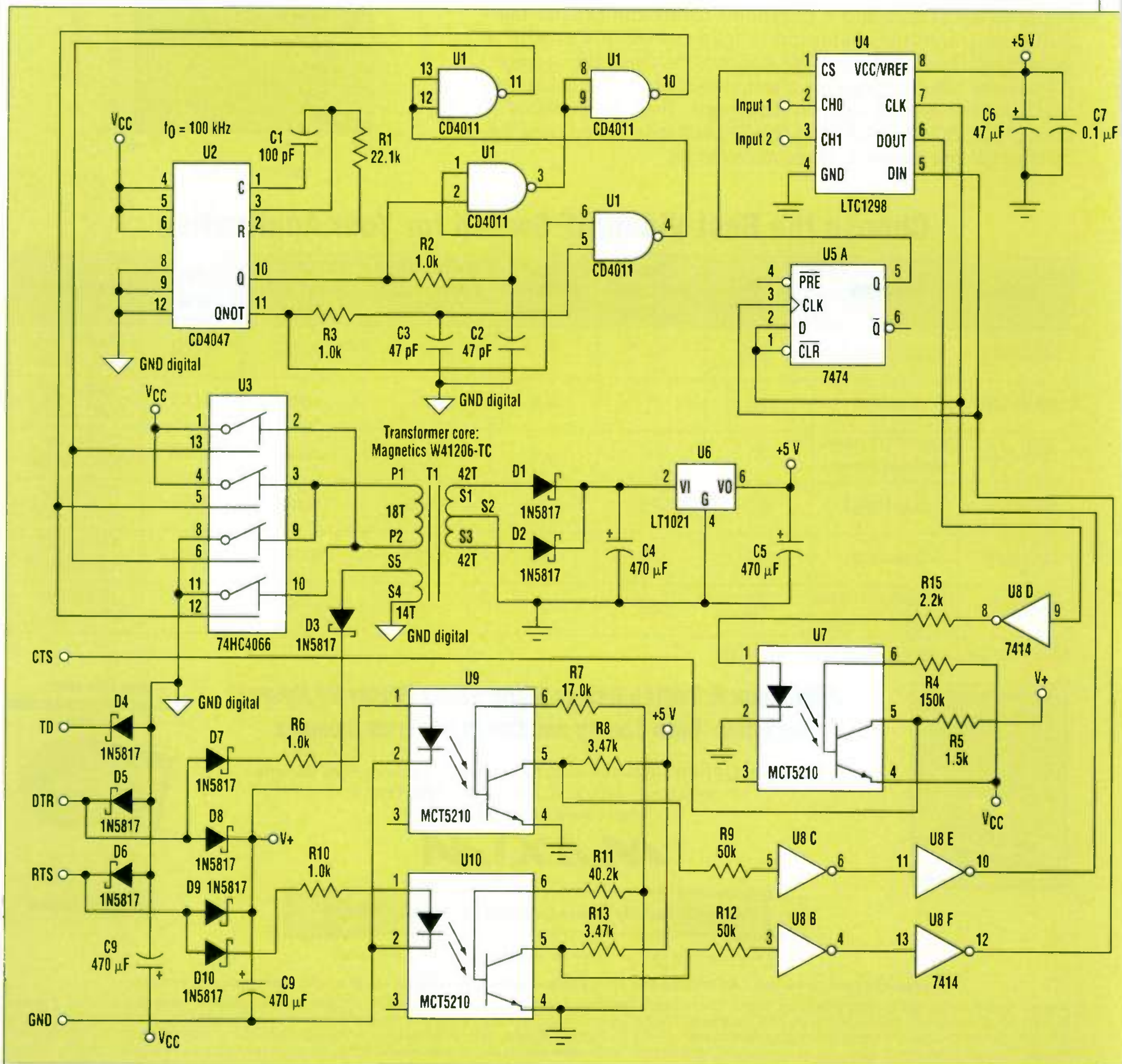
MEHRZAD KOOHIAN

Aura Systems, 2335 Alaska Ave., El Segundo, CA 90245; (310) 643-5300, ext. 112; fax (310) 526-9159; e-mail: mkoohian@aurasystems.com.

Data acquisition using RS-232 or printer ports on the PC has become popular due to easy and non-intrusive connection of serial converter modules. Industrial or medical applications, however, often will require isolation of the grounds from the PC ground for safety and/or noise immunity reasons.

The circuit shown allows for an isolated 12-bit data-acquisition system using the RS-232 port *(see the figure)*. The analog-to-digital converter can be addressed via DTR (data terminal ready), CTS (clear to send), and RTS (request to send), as shown. An isolation transformer is alternately driven with a square wave via the H-bridge-configured quad switch (74HC4066). The low on-resistance of the quad switch allows for less than 80% efficiency at I < 10 mA.

To best utilize the power available from the serial port, the TD (transmit



This circuit provides ground isolation for PC-based data acquisition systems resulting in improved noise immunity and safety.

```
/*OPTOISOLATED DATA ACQUISITION ON RS232 PORT */

#include <stdio.h>
#include <conio.h>

main()
{
  int scale_fact=2048,vout,i,j,b,d,k;
  char dat_in[5]={1,1,1,1,1},ch;

  printf ("program begins with data read \n");
  /*make DTR and RTS High to charge positive caps*/
  for (k=0;k<10000;k++) outp(0x3fc,(0x03 |inp(0x3fc)));
  /*make DTR and RTS low to charge negative caps*/
  for (k=0;k<10000;ktt) outp(0x3fc,(0xfc &inp(0x3fc)));
  while ( !kbhit() )
  {
    b=scale_fact;
    vout=0;
    for (i=0;i<5;i++)                             /*do five times*/
    {
      /*for (k=0;k<7;k++) */
      outp( 0x03FC,(0x1 | inp(0x3FC)) );          /*make DTR high (sclk low)*/
      j=4-i;
      if( dat_in[j]==1 )                          /*if Din is a 1*/
        outp( 0x3FC,(0xFD & inp(0x3FC)) );        /*make RTS a 0 (Din a 1)*/
      else                                        /*if not*/
        outp( 0x03FC,(0x2 | inp (0x3FC)) );       /*make RTS a 1 (Din a 0)*/
      /*for (k=0;k<5;k++)*/
      outp(0x3FC,(0xFE & inp(0x3FC)));            /*bring DTR low (SCLK high)*/
    }                                             /* end of 5 times loop*/
    for (i=0;i<12;i++)                            /*do 12 times*/
    {
      /*delay loop for next instruction stretch pulse*/
      for (k=0;k<2;k++)
        outp(0x03FC,(0x1 |inp(0x3FC)));           /*make DTR high (SCLK low)*/
      for (k=0;k<2;k++)                           /*time delay pulse stretch*/
        outp(0x3FC,(0xFE & inp(0x3FC)));          /*make DTR low (SCLK high)*/
      if ((inp(0x3FE) & 0x10)==0x10)              /*if CTS (input data)=16*/
        d=1;                                      /*then that bit will be a 1*/
      else
        d=0;                                      /*otherwise it will be a zero*/
      vout=vout+d*b;                              /*update Vout*/
      b=b/2;                                      /*divide scaler by two*/
    }                                             /*end of 12 times loop*/
    for (k=0;k,4;k++)
      outp (0x3FC,(0x2 | inp(0x3FC)));           /*make RTS high (Din low)*/
    for (k=0;k<4;k++)
      outp (0x3FC,(0xFD & inp(0x3FC)));          /*make RTS low (Din high)*/
    /* display to screen(slows down sample rate)*/
    printf("%d\n",vout);
  }
  outp(0x3fc,(0xfd & inp(0x3fc)));                /*make RTS low (Din high)*/
}
```

data) also is used to supply current. The TD line is usually at MARK (–12 V). Thus, the polarity of the primary circuit (connected to PC GND) is inverted to take advantage of the current available from TD, which increases the available power by 30%. The two output lines, DTR and CTS, also are inverted and initialized to –12 V (note the inversion of the rectifier diodes D4, D5, and D6).

To operate the output transistor of the U7 optocoupler, a third winding has been added to the transformer along with D3 and C8, thus forming V+. This won't be necessary if sampling frequencies are under 500 Hz. U2 provides the complementary square-wave outputs while R2, R3, C2, and C3 introduce dead time to prevent shoot-through currents. This circuit can sample at up to 1000 Hz and supply less than 5 mA at 5 V (U6 pin 6) for transducer excitation or other circuitry. Increasing the sample rate beyond 1.5 GHz would starve the optocouplers for current.

The C routine exercises the analog-to-digital converter using COM1, while taking into account the power issues *(see the listing)*. The sample rate depends on how fast the "12 times loop" is executed.

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NOVEMBER

23rd Annual Conference of IEEE Industrial Electronics (IECON '97), November. 9-14. Hyatt Regency Hotel, New Orleans, Louisiana. Contact Michael Greene, 200 Broun Hall, Electrical Engineering, Auburn University, Auburn, Alabama 36849-5201; (334) 844-1828; e-mail: greene@eng.auburn.edu.

Asian Test Symposium, Nov. 17-19. Akita, Japan. Contact Y. Takamatsu, +81 89 927-9955; e-mail: takamatsu@cs.ehime-u.ac.jp.

IPC National Conference: Solutions for Ultra-High-Density PWBs, Nov. 20-21. Biltmore Hotel, Santa Clara, CA. Contact John Riley, IPC diretor of education, (847) 509-9700 ext. 308.

DECEMBER

36th IEEE Conference on Decision & Control, Dec. 8-12. Hyatt Regency, San Diego, CA. Contact Ted E. Djaferis, Department of Electrical & Computer Engineering, University of Massachusetts, Amherst, MA 01003; (413) 545-3561; fax (413) 545-1993; e-mail: djaferis@ecs.umass.edu.

Workshop on Internet Technology & Systems (WITS), Dec. 9-12. Marriott Hotel, Monterey, California. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, California 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

JANUARY 1998

Annual Reliability & Maintainability Symposium/Product Quality & Integrity (RAMS), Jan. 20-22. Anaheim Marriott, Anaheim, CA. Contact V.R. Monshaw, Consulting Services, 1768 Lark Lane, Cherry Hill, NJ 08003; (609) 428-2342.

Photonics West, Jan. 24-30. San Jose, CA. Contact the SPIE Exhibits Dept., P.O.Box 10, Bellingham, WA 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

Seventh Security Symposium, Jan. 26-29. Marriott Hotel, San Antonio, TX. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

IEEE Power Engineering Society Winter Meeting, Jan. 31-Feb. 5. Tampa, FL. Contact Jim Howard, Tampa Electric Co., P.O. Box 111, Tampa, FL 33601; (813) 228-4653; fax (813) 228-1333; e-mail: j.howard@ieee.org.

FEBRUARY

IEEE International Solid-State Circuits Conference (ISSCC '98), Feb. 5-7. San Francisco Marriott, San Francisco, CA. Contact Diane Suiters, Courtesy Associates, 655 15th St. N.W., Washington, DC 20005; (202) 639-4255; fax (202) 347-6109; e-mail: isscc@courtesyassoc.com.

IEEE Applied Power Electronics Conference and Exposition (APEC '98), Feb. 15-19. The Disneyland Hotel, Anaheim, CA. Contact Pamela Wagner, Courtesy Associates, 655 15th St., N.W., Suite 300, Washington, DC 20005; (202) 639-4990; fax (202) 347-6109; e-mail: pwagner@courtesyassoc.com.

38th Israel Conference on Aerospace Sciences, February 25-26. Tel-Aviv and Haifa. Contact Technion-Israel Institute of Technology, Haifa 32000, Israel; 972-4-8292713; fax, 972-4-8231848; e-mail: alice@aerodyne.technion.ac.il.

MARCH

Sixth Annual Embebbed Systems Conference East, Mar. 31-Apr. 2. Chicago's Navy Pier Festival Hall, Chicago, Illinois. Contact Miller Freeman Inc., 600 Harrison Street, San Francisco, CA 94107; (415) 905-2354; fax (415) 905-2220; Internet: http://www.embedsyscon.com/.

APRIL

Southeastcon '98, Apr. 10-15. Hyatt Regency, Orlando International Airport, Orlando, FL. Contact Parveen Ward, ECE Dept., University of Central Florida, Orlando, FL 32816; (407) 823-2610; fax (407) 823-5835; e-mail: pfw@ece.engr.ucf.edu.

MAY

IEEE International Conference on Evolutionary Computation, May 3-9. Ankorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@akaska.net.

IEEE International Conference on Neural Networks (ICNN '98), May 3-9. Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@akaska.net.

IEEE World Congress on Computational Intelligence, May 3-9. William A. Egan Civic and Convention Center, Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc. P.O. Box 242064, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

Seventh IEEE International Fuzzy Systems Conference, May 3-9. Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

IEEE/IAS Industrial & Commercial Power Systems Technical Conference (I&CPS), May 4-7. Edmonton, Alberta, Canada. Contact Marty Bince, Modicon Canada Ltd., 5803 86th St., Edmonton, Alberta T6E 2X4, Canada; (403) 468-6673; fax (403) 468-2925.

IEEE International Conference on Acoustics, Speech & Signal Processing (ICASSP '98), May 12-15. Seattle Convention Center, Seattle, WA. Contact Les E. Atlas, Dept. EE(FT 10), University of Washington, Seattle, WA 98195; (206) 685-1315; fax (206) 543-3842; e-mail: atlas@ee.washington.edu.

JUNE

IEEE/MTT-S International Microwave Symposium (MTT 98), June 7-12. Baltimore Convention Center, Baltimore, MD. Contact Steven Stitzer, Westinghouse Electric Corp., P.O. Box 1521, MS 3T15, Baltimore, MD 21203; (410) 765-7348; fax (410) 993-7747.

USENIX 1998 Technical Conference, June 13-17. Marriott Hotel, New Orleans, LA. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

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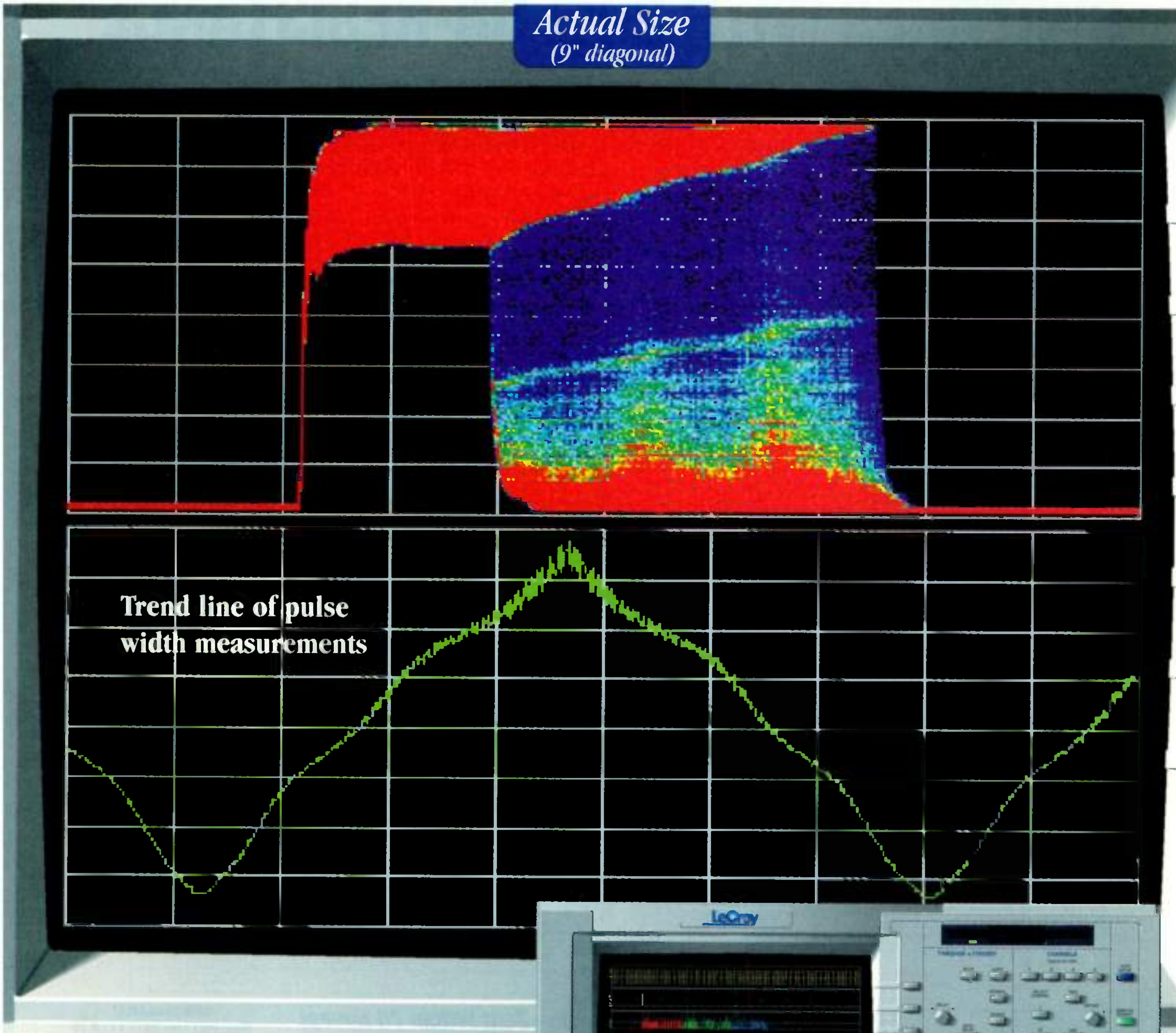

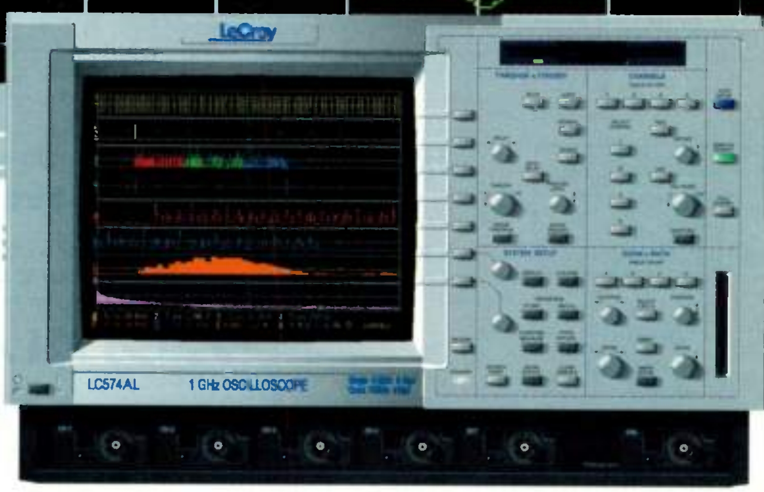

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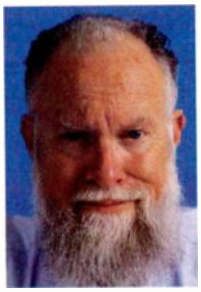
BOB PEASE

Bob's Mailbox



Bob:

What are you doing? Your column is normally something I enjoy reading—for electronics-related issues. Even when you go off on a tangent and talk about cars or oven thermostats, at least it's engineering-related. Columns about hiking would include something about batteries and solar power. This trek stuff has nothing even remotely related to the magazine's normal content. I am disappointed that you would use your column (nearly 2 pages) to solicit a vacation trip so you can save a couple of bucks. If I were reading about this in a hiking magazine, I would not feel like I was wasting my time because the article is consistent with the focus of the magazine. Obviously, that isn't the case here.

Don't get me wrong, I like hiking and camping. In fact, I like it very much. There are a lot of things I like to do. What would happen if every writer who has a column in a technical publication decided they wanted to take a vacation and began devoting their entire column to recruiting people for a particular event?

Please go back to what you do best in this field, and post vacation desires somewhere on the net or at local REI stores.

PAUL LEONARD
via e-mail

Hello Mr. Leonard—you are right. Hiking is a waste of time and energy. Reading about hiking is a waste of time and energy. Going on a BIG trek is a BIG waste of time and energy and money. But it can be INSPIRING. You get YOUR inspiration YOUR way—I'll get mine my way. If reading about that is annoying—then don't read it. But, all work and no play makes Jack a dull boy. (Or Paul.) So—I can't please everybody all the time. I'll be back to write more about electronics. But only after I get inspired.—RAP

P.S. The intent is not to "save a couple bucks"—rather, to lure other engineers/hikers along so they can be inspired, too.

Hi, Bob:

It was with great yearning in the very depths of my soul that I read your July 7 column on Trekking. A soul-cleansing trek in Nepal would once again put my spirit in equilibrium. I want to go. I need to go. I have a passport, I can swing the bread, and I can get the time off. My wife would not stand in my way. All that I need I have—except a working kidney.

Even though I self-dialyze, four weeks of dialysis supplies would more than fill a van. You see what the problem is. So here I am, in my office in Hackensack, N.J. on a rainy summer day, wishing I could go to Nepal, and knowing I can't. I will add this to the list of "I can'ts" that have come up lately. Like "can't change jobs." You can help me, though. I bet you take pretty good pictures. I would be willing to pay for film and developing in return for some prints. If I cannot go for real, perhaps I can go vicariously.

MIKE McGINN
via e-mail

Don't send me any of your money. Just remind me when I get back. I can get you some inspiring photos. We can buy NICE 8-in. × 11-in. prints for about $3. So—sit on your money. I can make a few extra prints of some very nice scenes—for cheap. Also, be sure to send me your snail-mail address someday. My wife will be taking MOSTLY 35 mm prints, and I'll be making mostly videotape. Better audio that way, I hope. So, I presume you'll like a chunk of video, too. Can do. I'll walk a few miles for you.—RAP

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer
rap@webteam.nsc.com—or:

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CE-Compliant Single-Chip CMOS Speakerphone Connects To PSTN

A new single-chip hands-free speakerphone circuit realized in CMOS technology complies with the EMC specifications (CE) for connection to the public switching telephone network (PSTN). According to its manufacturer, Austria Mikro Systeme, the AS2520 is the only monolithically integrated hands-free speakerphone set on the market that's manufactured in CMOS technology. This, in turn, decreases EMC design efforts, saving time and development costs. The chip integrates the following functionalities: line interface with power extraction, 2/4 wire conversion, speech network with speaker amplifier, switching logic with all time constants, and peak detectors. Together with a microcontroller that has a dialer and tone generator, the AS2520 performs all of the functions needed for a fully electronic hands-free speakerphone. The implementation of a new kind of voice-channel control and switching circuit accommodates a violation design approach, in which the chopper effect found in traditional speakerphones can be virtually eliminated. The IC is powered entirely from the telephone line and can operate at currents of 5 mA, allowing the parallel operation with an electronic telephone. During ringing, a dc-dc converter supplies 4 V, making it possible to use the same loudspeaker for tone ringing. *AV*

***Austria Mikro Systeme International**, Premstaetten Castle, 8141 Unterpremstaetten, Austria, phone: +43-31 36/5 00; fax: +43-31 36/5 25 01.* **CIRCLE 558**

Wall-Mount Case Family Adds EMC-Shielded Versions

The Conceptline wall-mount case product line is now available in special EMC versions. Technically, the new solution is based on RF springs that are mounted all along the inner part of the front door. When closing the door, these springs establish a conducting contact with the main part of the case. The springs consist of high-grade steel, while the contact areas of the case are galvanized with tin. The RF springs are located behind the IP gasket within the inner part of the case. This arrangement protects the springs from moisture, dirt, or dust. Therefore, the material's characteristics remain almost constant for a longer time. As a result, the IP 66 protection and the shielding attenuation of 40 dB at 1000 MHz are guaranteed for the entire lifetime of the case. For the EMC version, the Conceptline accessory program was complemented with a galvanized mounting board. This means that all devices can get large-area ground connections, which is quite important when attenuating any oscillations. *AV*

***Schroff GmbH**, P. O. Box 3, 75332 Straubenhardt, Germany; phone: +49-70 82/79 4-3 46; fax +49-7082/79 4-6 79.* **CIRCLE 559**

Eight-Channel Source Driver Comes In 20-Lead SOIC Package

The UDN298LW protected eight-channel source-driver IC is available in a 20-lead wide-body SOIC package. It's designed for use an an interface between standard low-level logic and higher-powered devices, such as relays, motors, solenoids, LEDs, and incandescent lamps. It incorporates thermal shutdown circuitry and output transient protection with clamp diodes for use with sustaining voltages of up to 35 V. Each channel includes a latch to turn off the channel if the maximum channel current is exceeded. All channels are disabled if the thermal shutdown is activated. A common fault output indicates chip thermal shutdown or any overcurrent condition. Under typical operating conditions, each of the eight outputs will source more than 100 mA continuously at an ambient temperature of 25°C and a supply voltage of 35 V. The overcurrent fault circuit will protect the device from short circuits to ground with supply voltages up to 35 V. Inputs are compatible with 5- and 12-V logic systems. *RE*

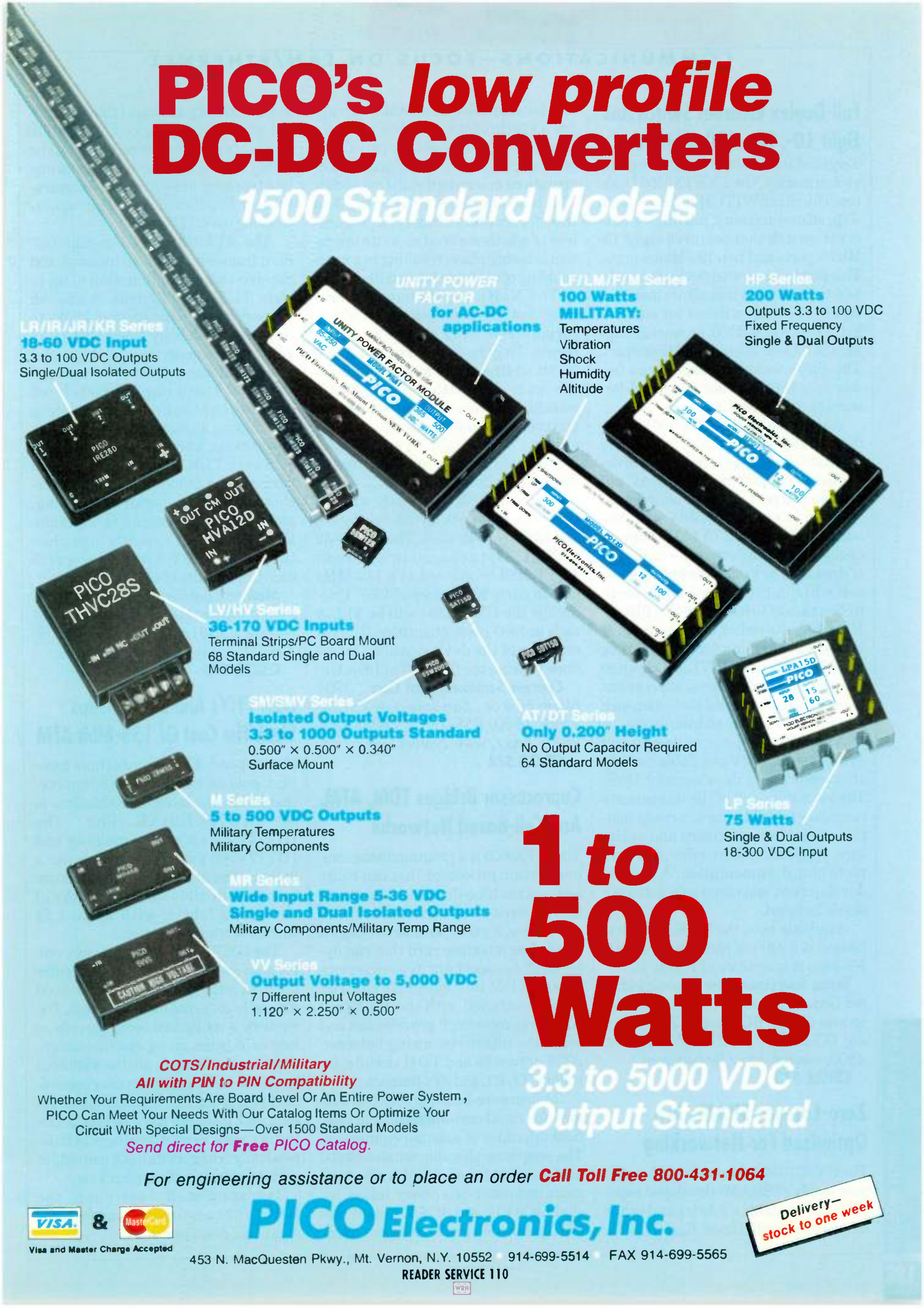
***Allegro MicroSystems Europe Ltd.**, Balfour House, Churchfield Rd., Walton-on-Thames, Surrey, KT12 2TD, England; phone: (44-1932) 253-355; fax: (4-1932) 246-622.* **CIRCLE 560**

Compact Filter Systems Designed For Computer Chassis Mounting

A series of active filters and signal-conditioning systems developed by Kemo Ltd. are configured to be able to mount into the spare 5.25-in. drive bays found in most modern PCs. The Model 100 family offers several benefits over using internal card slots. For instance, the systems exhibit inherently better screening from electrical noise, and the expanded space allows for improved layout and higher-quality analog circuit design. Furthermore, the filtering hardware is completely machine-independent and operating-system-independent. The systems feature front-panel BNC connectors, so that the signals can be taken in at the front of the PC. Rear cabling passes the filtered signal onto the user's choice of acquisition card. The signal-conditioning hardware is available in computer-controlled configurations, with an RS-232 interface that's run off the standard internal PC serial header. Manual versions also are available with its functions adjusted using front-panel switches. The completely enclosed case design means that the units can be used outside a PC chassis as well. Then they would be compact standalone "signal-conditioning boxes" or "active cable adaptors." *RE*

***Kemo Ltd.**, 3 Brook Court, Blakeney Rd., Beckenham, Kent BR3 1HG, England; phone: 0181 658 3838; fax: 0181 658 4084.* **CIRCLE 561**

Edited by Roger Engelke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READER SERVICE 110

Full-Duplex Ethernet Switch Has Eight 10-, Two 100-Mbit Ports

Targeted at the burgeoning workgroup switch market, the TNETX3100 Desktop ThunderSWITCH 8/2 is a single chip, shared-memory, full-duplex Ethernet switch that features eight 10-Mbit/s ports and two 100-Mbit/s ports. This highly integrated device forms the heart of a solution that allows manufacturers to build switches for small or home offices (SOHO), or workgroups for a BOM cost of less than $15 per port. The chip's switching engine can forward packets in either store-and-forward or cut-through mode.

All ports on the TNETX3100 are full-duplex-capable and interface to any standard SNI PHY device. They're designed to support multiple MAC addresses per port. Further address expansion is made possible with the addition of the TNETX15AE address engine, which supports more than 1000 addresses. The switch can configure itself without the help of a microcontroller, thanks to its on-chip EEPROM. If needed, the switch chip can support statistics collection for Etherstat or RMON under SNMP. VLAN capabilities and additional address support can be added via an external controller, such as the TNETX15AE address engine.

A complete reference design and evaluation kit are available to help shorten product development time. The kit includes all of the components necessary to build a market-ready solution, including a pc board and enclosure, schematics, Gerber files, and complete chip documentation. A suite of development and diagnostic software also is included.

Available now, the TNETX3100 is housed in a 240-pin package. Pricing is $65 each in quantities of 10,000. LG

***Texas Instruments Inc.**, Semiconductor Group, SC-97022, Literature Response Center, P.O. Box 172228, Denver, CO 80217; 1-800-477-8924, ext. 4500; Internet: http://www.ti.com*

CIRCLE 573

Zero-Latency SRAMs Are Optimized For Networking

The CY7C1334 is the first member in a new family of SRAMs developed especially for switching fabrics and other networking applications. Known as No Bus Latency (NoBL) SRAMs, they utilize a synchronous pipelined architecture to eliminate the latency period that occurs between the "read" and "write" operations in standard static memories. This is accomplished by allowing data transfer on every clock cycle, regardless of whether a read or write operation is taking place, resulting in a near-doubling of available bandwidth.

The NoBL RAMs have several other features that optimize their performance in networking environments. They're configured in 32- and 36-bit widths, much more suitable to the wide datapaths employed by switching fabrics. Also, a "byte write" feature allows data to be changed in a single operation, versus the "read/modify/write" method used in most conventional memories.

The NoBL SRAM family will initially consist of 64k-by-32, 64k-by-36, and 128k-by 36 devices. The 64k-by-32 CY7C1334, packaged in a 100-pin TQFP, will be offered as a 133-MHz part in early November of 1997. Pricing for the CY7C1334 will be $12.00 each in 1000-piece quantities. The remainder of the devices will be introduced during the first half of 1998. LG

***Cypress Semiconductor Corp.**, 3901 North First St., San Jose, CA 95134-1599; (800) 858-1810; (408) 943-2817; http://www.cypress.com.*

CIRCLE 574

Coprocessor Bridges TDM, ATM, And Cell-Based Networks

The MTX3020 is a programmable communication processor that can route and process time-division multiplexing (TDM) streams of voice or data. With this device, it's now possible to design a single line interface card that can dynamically support any type of service on any TDM link under its control. When combined with the MTX3010 ATM cell processor, it provides fast and seamless internetworking between ATM networks and TDM circuits, including T1, E1, and JT2 framers.

Its firmware-based architecture allows for rapid customization and easy field upgrades of existing equipment. The programmable chip set also can be configured to handle TDM traffic from most computer-telephony buses, including MVIP and SCSA. This versatile combination gives designers maximum flexibility and rapid time-to-market when developing communication products such as voice traffic over ATM (VTOA) interfaces, PBX and mobile trunking units, access concentrators, or Products for ATM internetworking over T1 lines.

The MTX3020 uses its on-chip standard framer interface to transmit and receive on any combination of up to eight T1, E1, or JT2 links. It also can support up to 16 bidirectional links to computer-telephony buses with up to 1024 virtual connections, at data rates of up to 8 Mbits/s per link. The coprocessor can arbitrarily map DS0 flows to cell payloads, including cross-link mapping for trunking applications. In Cell Relay applications, where ATM traffic is carried over T1/E1 links, the MXT3020 performs cell delineation, header-error-control (HEC) generation/checking, and cell payload scrambling/unscrambling functions. Currently in production, the MTX2030 is priced under $125 each in quantities of 10,000.

***Maker Communications Inc.**, 73 Mount Wayte Ave., Framingham, MA 01702; (508) 628-0622; fax (508) 628-0256; e-mail: info@maker.com.*

CIRCLE 575

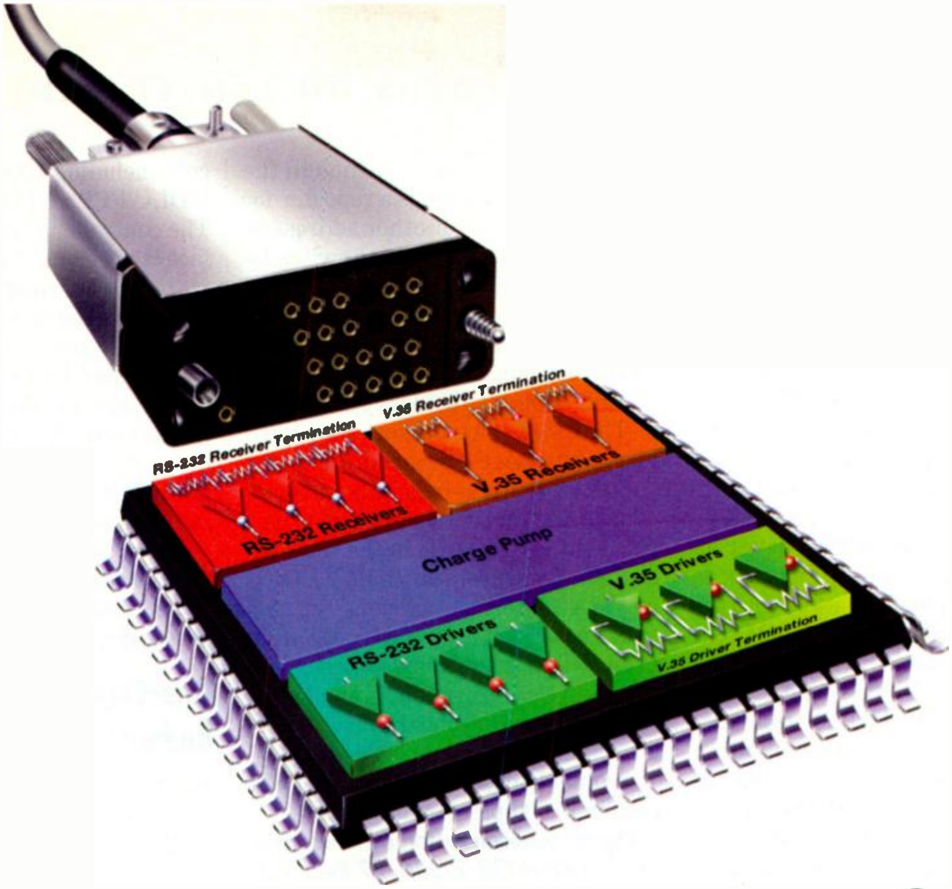
New PHYs And Switch Chips Slash The Cost Of 155-Mbit ATM

High-speed ATM connections have just gotten much less expensive, thanks the the latest introductions in the SWITCHStAR line. The IDT77V400 switching memory and IDT77V500 switch controller use a unique "fusion memory" architecture to create flexible building blocks of switching fabric, with up to 1.24 Gbits/s of bandwidth each.

The IDT77V400 switch memory employs an on-chip DRAM that can buffer up to 8K cells. This eliminates the need for costly external memory chips. The memory is configured to handle cells as long as 56 bytes, giving systems designers the opportunity to use the additional bytes for cell tagging or other specialized performance enhancements. Its data path interface has a flexible architecture that permits designers to independently configure its input and output ports to meet specific applications..

Its associated controller, the IDT77V500, also offers many features

(continued on page 200)



Simplified V.35 Interface

The SP320 is the world's only single chip V.35 transceiver. Featuring the highest level of integration, the SP320 includes all the line drivers and receivers necessary for a complete V.35 port without the need for external termination resistors.

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An on-chip Sipex charge pump allows low power +5V only single supply operation. The SP320 is NET1/NET2 certified and is ready for your next V.35 port design. Call a Sipex applications engineer today to see how simple a V.35 port can be!

Sipex

Sipex Corporation, 22 Linnell Circle, Billerica, MA 01821 Tel. 978-667-8700 Fax 978-670-9001 www.sipex.com

READER SERVICE 234

(continued from page 198)
and performance enhancements. In addition to supporting up to 8K connections without using external SRAM, it performs many advanced traffic-management tasks. These include running a fair per-VC queuing algorithm, support for several congestion control schemes, and implementation of the CBR, VBR, UBR, and ABR flow-control services. Features like a packetizing mode and multicast capability can be added to enable a variety of switching functions.

To lower the cost of PHY-layer interfaces, the IDT79155 PHY has been designed to be pin-compatible with the PMC-Sierra SUNI-LITE PHY. A completely assembled NIC card which uses the IDT79155 PHY also is available. Known as the IDT reference design, it can be used as an evaluation and development tool to accelerate product development. If desired, it can serve as a complete reference design.

Available in sample volumes now, the IDT77400/500 memory/controller will be in full production during the fourth quarter of this year. Pricing will be $43.75 each for the '400 and $55.50 for the '500, in 10,000-piece quantities. The IDT79155 PHY is shipping now in production quantities and costs $29 each in 10,000-piece orders. LG

Integrated Device Technologies, 2975 Stender Way, Santa Clara, CA 95954-3090; (800) 345-7015, faxback (800)9-IDT-FAX; standard fax (408) 492-8674; http://www.idt.com. **CIRCLE 576**

Smart 10/100 Buffered Port Switch Has Versatility, Range

The 21340 10/100 Mbit buffered port switch is an intelligent, buffered four-port repeater that can be used as a building block for constructing a wide range of cost-effective managed and unmanaged Ethernet hubs, workgroup switches, and other networking devices. It contains four auto-negotiating 10/100 Ethernet ports that can connect to either a MII or SYM physical-layer interface. Up to nine 21340s can be cascaded together, permitting construction of hubs and switches with up to 36 ports. MIBs for repeater and Ethernet-like SNMP management functions are supported.

Its high level of integration and on-chip buffers permit the construction of a new class of extremely low-cost "switched-repeaters." Although the port switch functions as a repeater for packets destined for other addresses, it's architecture allows it to switch local traffic between its internal ports, thus reducing network congestion. Per-port buffering also enables the 21340 to handle any combination of 10- and 100-Mbit traffic on its ports.

The 21340's internal switching capability also eases the severe distance and topology constraints encountered when using Fast Ethernet technology. Each of the four ports in the repeater contains its own on-chip buffer FIFOs and MAC interface, allowing the chip to be its own self-contained collision domain. This permits hubs, switches, and other networking products employing the 21340 to go beyond the normal two-level limit for cascading of devices.

Available now, the 21340 costs $25 each in 10,000-piece quantities. LG

Digital Semiconductor, attn: Susan Benard, m/S HLO2-2/J06, 77 Reed Rd., Hudson, MA 01749; (800) 332-2717, (510) 490-4753; fax (508) 568-6447; e-mail: semiconductor@digital.com; http://www.digital.com/semiconductor. **CIRCLE 577**

Smart 4-Channel Communication Controller Sports PCI Interface

The CL-CD4400 is part of a new family of intelligent communication controllers for internetworking and remote-access applications. Featuring a PCI bus host interface and an embedded ARM RISC controller, each of the device's four programmable serial I/O channels can support full-duplex communications at rates of up to 8 Mbits/s. Thanks to the its powerful on-chip processor, the host system is freed from nearly all time-critical, low-level tasks involved with data transfer and channel management. If desired, one of the controller's channels can be programmed to operate at up to 52 Mbits/s while sustaining the full 8 Mbit/s rate on the other three channels.

The CD4400's high-speed, full-duplex channel capabilities and the ability to support complex communication protocols enable it to be used for advanced applications, such as ADSL and SONET. The on-chip ARM controller implements an efficient firmware-driven queue management system, and can be programmed to support popular protocols, including HDLC, Async, Async-HDLC/PPP, and Programmable Sync. The controller's embedded PCI interface is version 2.1-compliant and supports PCI bus mastering for maximum transfer speed and minimum loading of the host system. Fabricated in 0.35-mm CMOS, the CD4400 can operate on supply voltages ranging from 3.3 to 5 V.

Packaged in a 208-pin QFP, the CL-CD4400 is available in sample quantities now. Pricing is $39 each, in 10,000-piece quantities. LG

Cirrus Logic Inc., attn: Mike Leung, 3100 West Warren Ave., Fremont, CA 94538-6423; (510) 226-2041; e-mail: mleung@corp.cirrus.com. **CIRCLE 578**

One-Chip 10/100 "PHYceiver" Reduces Component Count

The ICS1890 integrates all physical-layer functions of the 10Base-T and 100Base-Tx standards from the media-independent interface (MII) to the line-interface magnetics. It integrates a complete 10/100Base-TX physical layer, including adaptive equalization, MLT-3 encode/decode, clock recovery/synthesis, and rate auto-negotiation circuitry. Half- and full-duplex operation can be selected, permitting transfer rates of 10, 20, 100, and 200 Mbits/s.

Designed to reduce component count and board space requirements for NICs, hubs, and switches, it requires only five external passive components and can be configured to work with several types of off-the-shelf magnetics. The 1890's multifunction interface allows easy connection to most MACs and repeater controllers, and can be configured into a 5-bit code-group interface for 100Base-Tx applications.

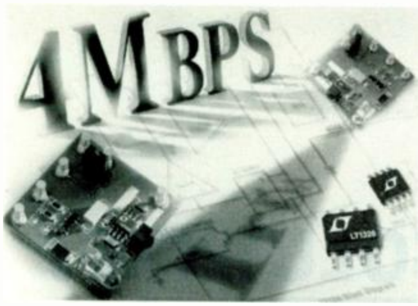
An on-chip station management interface permits exchange of command and status information with all of the 1890's registers. Monitoring of configuration, link status, Auto-Negotiation progress, false carrier detect, and several other fault conditions are simplified with the chip's QuickPoll feature.

Available now, the ICS1890 costs less than $20 each in 10,000-piece quantities. LG

Integrated Circuit Systems Inc., attn: Charen Singh, 2435 Boulevard of the Generals, P.O. Box 968, Valley Forge, PA 19482-0968; (408) 925-9470 fax (408) 925-9460; Internet: http://www.icst.com. **CIRCLE 579**

Compact IrDA Receiver Supports Data At Up To 4 Mbits/s

The LT1328 is an extremely compact infrared data receiver that supports the latest Infrared Data Association (IrDA) specification for transmission at 4 Mbits/s. Housed in an 8-pin MSOP,



it's compatible with IrDA standards such as SIR and FIR, as well as 4ppm, Sharp's ASK format, and most TV remote-control signals. All of the necessary circuitry to convert a detector's current pulses into a TTL-compatible output are included on the chip. Its high-pass filtering attenuates interfering signals such as sunlight, incandescent, and fluorescent bulbs. It requires only 2 mA of current from a single +5-V supply. Available now, the LTI1328 costs $2.25 each in quantities of 1000. LG

***Linear Technology Corp.**, 1630 McCarthy Boulevard, Milpitas, CA 95035-7417, (408) 432-1900; fax (408) 434-6441.*
CIRCLE 601

56-kbit/s Fax/Modem PC Card Supports KFlex Protocols

Designed for notebook, PDA, and desktop computer OEMs, the 56-kbit/s PC Card data/fax modem allows users to download information at significantly higher transfer rates than previously possible. The modem is designed to connect to any standard PC Card slot and uses a combination of on-card hardware and host-based software to perform the modem and fax functions.

While it currently supports the Lucent/Rockwell K56 protocol, its software-based architecture ensures that it will be easily upgradable to the ITU global standard for 56-kbit modems when it's released in 1998. The modem driver software is plug-and-play compatible with Windows 3.x, Windows 95, and Windows NT operating systems, and supports the complete V.34 33-kbit/s modem protocol, the group I and group III fax standards, and the

MNP 2-4 and V.42 error-correction protocols. Available now, the 56-kbit/s PC Card data/fax modem carries a suggested retail price of $234 each, with substantial discounts for OEM quantities. LG

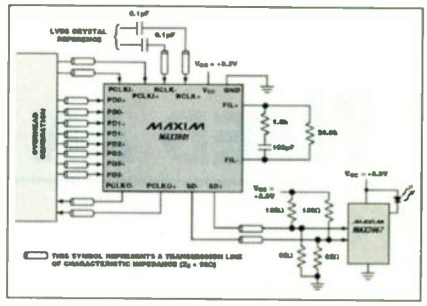
***Smart Modular Technologies Inc.**, 4305 Cushing Pkwy., Fremont, CA 94538; (510) 623-1231; fax (510) 623-1434.* **CIRCLE 602**

622-Mbit Serializer/Deserializer Chips Feature Very Low Power

The MAX3691 4:1 serializer and MAX3680 1:8 deserializer feature high levels of integration and low levels of power consumption which can greatly simplify many 622-Mbit/s SDH/SONET applications. Both devices are fabricated in a 3.3-V bipolar process and consume an average of 265 mW each.

The MAX3691 4:1 serializer is intended for converting four parallel 155-Mbit/s data streams into a single 622-Mbit/s connection. It includes a fully integrated PLL that has a phase/frequency detector, a loop filter/amp, and a voltage-controlled oscillator that synthesizes an internal 622-Mbit/s serial clock from a low-speed reference crystal. The chip's high-speed digital interface is able to accept LVDS-level clock and data inputs, and outputs a 3.3-V differential PECL signal.

Its companion chip, the MAX3680 1:8 deserializer, is designed to convert 622-Mbit/s serial data into an 8-bit, 77-Mbit/s parallel connection. Suitable for use in SDH/SONET transmission systems, ATM/SONET access nodes, and add/drop multiplexers, it includes input and output buffers, an 8-bit shift register, and an 8-bit parallel output register. It also includes a TTL-synchronization input that enables data



realignment and framing. It accepts PECL-compatible serial clock and data inputs, and delivers TTL-compatible outputs.

The MAX3691 4:1 serializer is available now, housed in a 32-pin TQFP. Pricing is $55 each. The MAX3680 1:8 deserializer also is available, housed in a 28-pin SSOP, and costs $34.45. Both prices reflect a lot order size of 1000 pieces. LG

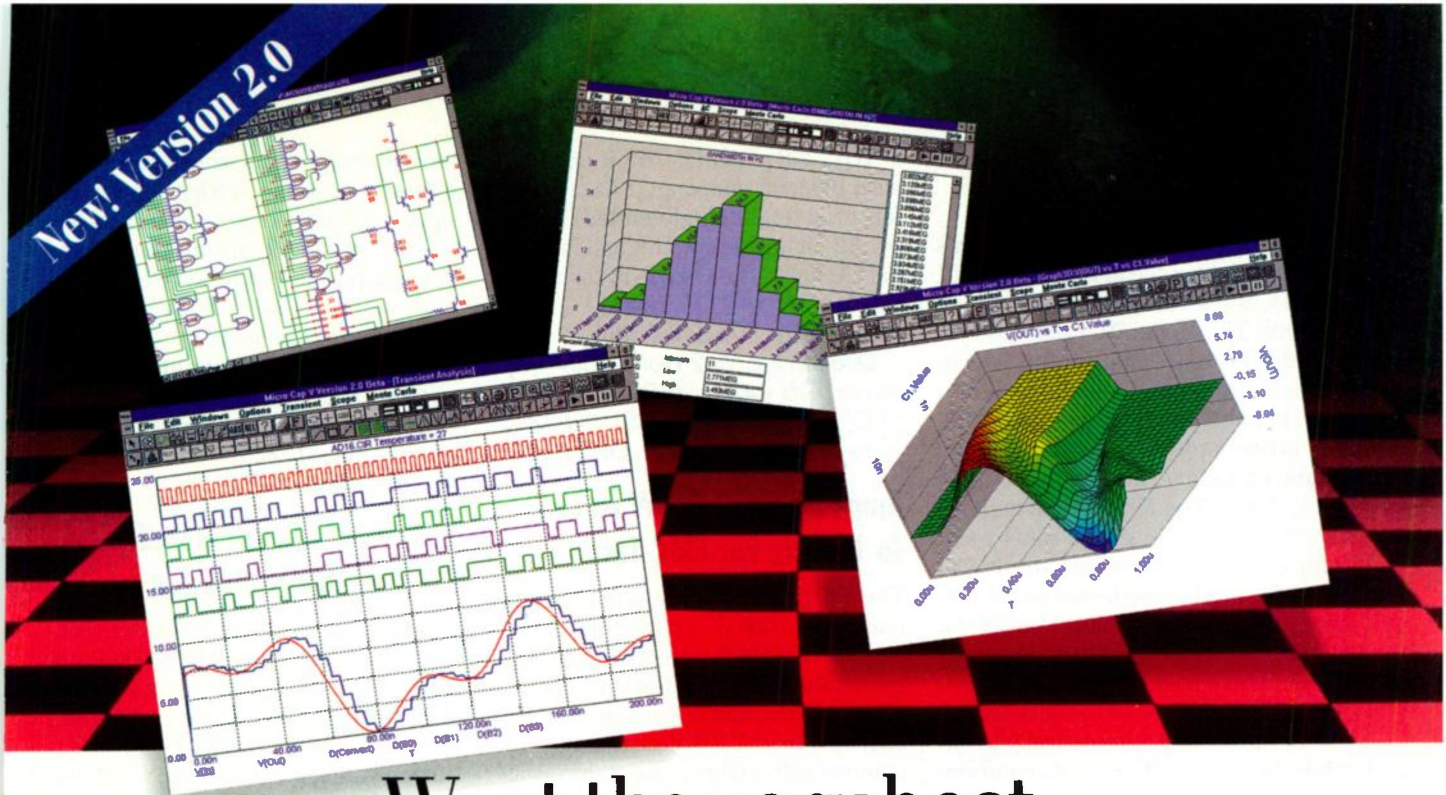
***Maxim Integrated Products**, 120 San Gabriel Dr., Sunnyvale, CA, 94086; (408) 737-7600 ext. 6087.* **CIRCLE 603**

V-Chip Converter Adds Program Blocking To Old TVs

The V-Chip Converter is an inexpensive set-top box that permits users to selectively block shows using the most recently approved TV rating system. It's fully programmable to block or pass any combination of content codes and can be retrofitted to nearly any existing television set. A programmable override code can be used to permit reception of all available broadcasting.

Priced at $60 each, with substantial discounts for OEM and wholesale applications, the V-Chip Converter is available now. LG

***Soundview Technologies Inc.**, 2 Soundview Dr., Greenwich, CT 06830; (203) 809-3303; fax (203) 869-8594.*
CIRCLE 604



Want the very best in Analog/Digital simulation? Introducing Micro-Cap V Version 2.0

Micro-Cap V is a fast, precision, 32-bit analog/digital simulator with an intuitive fifth generation user interface, and a library of more than 10,000 pre-modeled parts. Based on Spice3 and PSpice,™ it offers the best features and capability of both.

Its finely crafted simulation tools include schematic probing, during the run plotting, performance plots, 3D plots, multidimensional stepping, analog and digital behavioral modeling, an optimizing model generator, and Monte Carlo analysis. Compiled models, behavioral primitives, and a huge library of commercial parts make modeling of both analog and digital devices easy. New devices in Version 2.0 include BSIM 1.0, 2.0, and 3.3, sample and holds, Z transforms, and three new animation devices.

We offer the very best in analog/digital simulation and we guarantee it with a 30 day money back guarantee!

You can't lose. Call us for a free brochure and working demo or download the demo from our Web site.

Micro-Cap V runs on PCs under all Windows systems from 3.1 and up. Cost is $3495 complete.

Download the free working demo at www.spectrum-soft.com.

Features

• Mixed Analog/Digital	Yes
• Analog Engine	Spice3 & PSpice™
• Digital Engine	Native PSpice™
• During the Run Plots	Yes
• Analog/Digital Primitives	200+
• Analog/Digital Parts	10,000+
• Performance Plots	Yes
• Parameter Stepping	Multidimensional
• Optimizing Parts Modeler	Yes
• 3D Plots	Yes
• Schematic Probing	Yes
• Behavioral Modeling	Analog & Digital
• Monte Carlo	Yes
• Device Temperatures	Individually Set
• BSIM Devices	Yes. 1.0, 2.0, and 3.3
• Animation Devices	Yes
• Import/export Netlists	Yes
• Guarantee	30 Day Money Back
• Technical Support	By EEs for EEs

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E-mail sales@spectrum-soft.com

READER SERVICE 237

High-Density Switch Boards Include Digital Control

A pair of high-density switching cards are designed for use in the Model 7001 two-slot and Model 7002 10-slot switch systems. The Model 7021 multiplexer-digital I/O card is configured as two independent two-pole multiplexers, one a 1-by-12 bank and the other a 1-by-18. For larger applications they can be combined to form a 1-by-30 two-pole multiplexer. The Model 7022 matrix-digital I/O card offers a five-row-by-six-column configuration for a total of 30 two-pole switches, with each switch acting as a matrix crosspoint. Four of the matrix rows can connect to the switch system's mainframe analog backplane. It can then be used to connect two or more switch cards automatically to expand the matrix. The cards combine switching and digital control on one card. They feature a two-pole Form A contact configuration and can switch a wide range of signals, with maximum capacities of 110 V dc or rms, and 1 A or 30 VA (for resistive loads). Each channel has less than 100 pA of offset current and contact potential is less than 3 mV per contact pair. The Model 7021 and Model 7022 each cost $1295. JN

Keithley Instruments Inc., 28775 Aurora Rd., Cleveland, OH 44139-1891; (800) 552-1115; (216) 248-0400; fax (216) 248-6168; product_info@keithley.com; http://www.keithley.com. CIRCLE 605

PCMCIA Acquisition Cards Now Have FIFO Memories

All Quatech analog I/O PCMCIA cards now come standard with a 2048-sample data FIFO memory and a 2048-entry scan FIFO memory. The FIFO memories, which previously were optional, will significantly reduce CPU overhead. Moreover, the cards will now be able to perform up to their true potential in the Windows environment, according to the company. Affected cards include the DAQP-12 and DAQP-16, which have 12- and 16-bit resolutions, respectively. Both supply eight differential or 16 single-ended inputs, sample rates to 100 kHz, and eight digital I/O channels. The DAQP-208 is a 12-bit system with four differential (eight single-ended) analog inputs, two analog outputs, and four digital I/O lines. The DAQP-308 provides 16-bit accuracy with 100-kHz sampling. It has four differential (eight single-ended) inputs, two 12-bit analog outputs, and four digital I/O lines. The DAQP-12 costs $655, the DAQP-16 $755, the DAQP-208 $755, and the DAQP-308 $855. JN

Quatech Inc., 662 Wolf Ledges Pkwy., Akron, OH 44311; (800) 553-1170; (330) 434-3154; fax (330) 434-1409; http://www.quatech.com. CIRCLE 606

Amps Deliver 500 W At Up To 18 GHz For EMC Test

The 500T family of amplifiers offer a minimum of 500 W of power at frequencies to 18 GHz for electromagnetic-compatibility test applications. The amplifier will not shut down if subjected to extreme load VSWRs. Instead they automatically reduce output during severe load mismatches, and then resume full power operation when the mismatch eases. Testing continues uninterrupted. Power is measured at the output connector after options have been added, not at the TWT output. Front-panel displays show forward and reflected output and a menu of system status data that can be called up with a softkey. An IEEE-488 interface, gain control, VSWR protection, 0-dBm input, and RF sample output port are standard. The series includes the 500T1G2 (1 to 2.5 GHz), 500T2G8 (2.5 to 7.5 GHz), and 500T8G18 (7.5 to 18 GHz). Call for price and availability. JN

Amplifier Research, 160 School House Rd., Souderton, PA 18964-9990; (800) 933-8181; (215) 723-8181; fax (215) 723-5688; www.ar-amps.com. CIRCLE 607

Generator Allows Independent Pulse Parameter Control

A general-purpose pulse generator, the TGP110, offers independent control of pulse width, repetition rate, and variable pulse delay over a range of 0.1 Hz to 10 MHz. Users can generate pulses of a fixed width, regardless of repetition rate, at duty cycles extending down to a in 10^8. Pulse widths range from 50 ns to 5 seconds, with vernier control within each of eight overlapping decade ranges. Delays of 100 ns to 10 seconds are possible, with delays independently adjustable over the same range as pulse width. In addition to continuous mode, the unit can generate single or multiple pulses in response to trigger or gating signals. Other features include selectable delay between sync output and pulse output, and square-wave and double-pulse modes. Call for price and availability information. JN

Thurlby Thandar Instruments Ltd., Glebe Rd., Huntingdon, Cambridgeshire, PE18 7DX, England; phone: +44 (1480) 412451; fax: +44 (1480) 450409. CIRCLE 608

1.3-Gbit/s Tester Handles Rambus DRAM Devices

An addition to the HP 83000 semiconductor test family, the HP 83000 Rambus Series, can test Rambus DRAMs (RDRAMs) at-speed, with eight test sites in parallel. The new series features a 1.3-Gbit/s data rate, which exceeds the current Rambus requirement of 800 Mbits/s. The new testers target production testing of current generation RDRAMs, as well as the characterization and production ramp-up of next-generation Direct RDRAM devices. A timing accuracy of ±50 ps meets the demands of testing the aggressive setup-and-hold times of below 200 ps for Direct RDRAM devices. Prices for the HP 83000 Rambus Series start at $1.2 million. JN

Hewlett-Packard Co., Test and Measurement Org., P.O. Box 50637, Palo Alto, CA; 94303-9512; (800) 452-4844 ext. 5427. CIRCLE 609

Data-Acquisition Board Features 16-Bit Resolution

The DAQ-800 is a multifunction data-acquisition plug-in board for PC/AT and compatible computers. The eight differential channels feature 12-bit, 40-kHz analog-to-digital conversion with programmable gain. The unit also features 32 digital I/O lines and three 16-bit counter-timers. Included is a comprehensive software suite with driver software for most DOS and Windows languages. A Windows-based graphics display and datalogging application also is included. The DAQ-800 costs $295. JN

Omega Engineering Inc., 1 Omega Drive, P.O. Box 4047, Stamford, CT 06907-4047; (800) 826-6342; (203) 359-1660; fax (203) 359-7700; e-mail: info@omega.com; Internet: http://www.omega.com. CIRCLE 610

Multiplexers/Demultiplexers Filter Voltage Spikes

A series of analog multiplexers/demultiplexers that employ an injection-current effect to control filter voltage spikes can reduce component count, which cuts down board-space requirements, thus reducing system cost. The HC4851A, 52A, and 53A eliminate the need for external diode/resistor networks—typically about 40 passive components—that are usually required to keep the analog channel signals within the supply range by filtering out transients (voltage spikes).

Pin-compatible with the MC74HC405x and MC1405x families of analog multiplexers/demultiplexers, the chips also can be used in any applications that mix high-voltage analog with lower-voltage digital logic. The chips can simultaneously multiplex and protect sense lines from overvoltages. Each chip contains the equivalent of about 154 FETs (36 gates) and operates over a power-supply range of 2.0 to 6.0 V and a temperature range of –55 to +125°C.

The circuits are available in various package options—16-pin DIP, SOIC, wide-body SOIC, and TSSOP. In 5000-unit quantities, the multiplexers/demultiplexers sell for $0.96 each, with delivery from stock for small quantities. DB

***Motorola Inc.**, 2501 S. Price Rd., MD G544, Chandler, AZ 85248; Connie Schultejans, (602) 732-2852; Internet: http://sps.motorola.com/cgi-bin/dlsrch*
CIRCLE 611

Speed Special Effects With Image Manipulator

The LF2301 image resampling sequencer can perform image rotation, panning, zooming, warping, and compression, as well as the resampling of digitized images. Both data and computation rates can go as high as 40 MHz, and the chip uses a spiral walk-around technique for static filtering with kernel sizes of up to 15 by 15. In the spiral walk-around scheme, the kernel size can be incremented in steps of up to seven units for a maximum image size of 4096 by 4096 pixels. By making use of second-order address transformation equations, image warping at real-time video rates becomes a reality.

On the LF2301 is a self-sequencing address generator that's designed to filter a two-dimensional image, or remap and resample it from one set of Cartesian coordinates to another. In most video applications, two LF2301s can be used to construct a fast image transformation system in which the chips execute the interpolation algorithms in real time—nearest neighbor, bilinear interpolation, and cubic convolution. Offering double the speed of the discontinued Raytheon TMC2301, it's available 100% screened to MIL-STD-883, Class B, in plastic J-lead LCCs and ceramic PGAs. Prices for the LF2301 start at $33.25 each in 100-unit lots. DB

***Logic Devices Inc.**, 1320 Orleans Dr., Sunnyvale, CA 94089; Herman Nakamura, (408) 542-5400; Internet: http://www.logicdevices.com.*
CIRCLE 612

SGRAM Memory Modules Accelerate Graphics Systems

Available in 2- and 4-Mbyte densities, the MG256 and MG512 synchronous graphics memory modules deliver peak bandwidths of more than 1 Gbyte/s and device access latencies as low as 6.67 ns. The modules come in speed grades of 100, 125, or 133 MHz, and are configured as 144-contact small-outline dual-in-line memory (SO-DIMM) cards that measure 1.21 by 2.66 in. Based on the company's novel MultiBank DRAM core, the memory chips used on the SGRAM modules handle 1, 2, 4, 8, and full-page burst accesses. The modules operate from a 3.3-V supply and use LVTTL signaling over the interface. Production quantities are available now, with prices starting at $20 in lots of 1000 modules. DB

***MoSys Inc.**, 1020 Stewart Dr., Sunnyvale, CA 94086; Andre Hassan, (408) 321-0777.* **CIRCLE 613**

Active Bus Terminator Boosts Bus Data Rates

An active bus terminator chip pumps out (sources and sinks) current on an "as needed" basis to quite noise on bus signal lines, allowing the buses to operate at speeds ranging from 60 to 200 MHz. One such example is the ML6552, which can support many of the new bus interfaces—Rambus, low-voltage TTL, Gunning Transceiver logic plus (GTL+), and series-stub terminated logic (SSTL)—as well as many of the conventional TTL and CMOS bus signaling schemes.

To provide the active termination, an on-chip switching power-supply circuit sinks or sources 1 A with an output voltage of 2.5 V (for a 5-V supply), or 1.5 V (for a 3.3-V supply). The 2.5-V output is used for the Rambus termination, and the 1.5-V level is used for GTL+ and SSTL termination. The output voltage, however, can be set to any value in the range of 1 to 6 V, thus providing designers with additional reference voltages required by Rambus and GTL+ buses. All output voltages are regulated to within 5% of the nominal value. In 1000-unit lots, the ML6552 active terminator sells for $1.60 each and comes housed in an 8-lead SOIC plastic package. DB

***Micro Linear Corp.**, 2092 Concourse Dr., San Jose, CA 95131; Tony Ochoa, (408) 433-5200; or on the web at http://www.microlinear.com.*
CIRCLE 614

Socket 7 CPUs Gain AGP Core Logic Chip Set

The Apollo VP3, a PC core logic chip set that supports the accelerated graphics port (AGP) for Socket 7 CPUs in desktop and portable computers, can be used with Intel Pentium, AMD K5/K6, Cyrix 6x86/M2, and IDT C6 (Centaur) CPUs. The set consists of two chips. One is a single-chip North bridge controller, the VT82C597, which comes in a 472-contact BGA package. The other is the previously released 82C586B PCI to ISA South bridge, which is housed in a 208-lead PQFP.

Multiple DRAM interfaces are supported by the VP3 chip set—fast page mode, EDO, and synchronous DRAMs—as are mixed combinations of the three, with a maximum address range of 1 Gbyte. The AGP interface supports both the 33- and 66-MHz speed options. The chip set has 3.3-V compatible interfaces to main memory, the AGP interface, and PCI buses. In addition, all of those lines can tolerate 5-V signal swings. A sub-3.3-V interface is available to connect to the CPUs. Production quantities of the Apollo VP3 chip set are available immediately; in sample quantities it sells for $39. DB

***VIA Technologies Inc.**, 5020 Brandin Ct., Fremont, CA 94538; Dean Hays, (510) 683-3328; or on the web at http://www.via.com.tw.* **CIRCLE 615**

Which FFT Analyzer? You be the Judge.

The Charges:

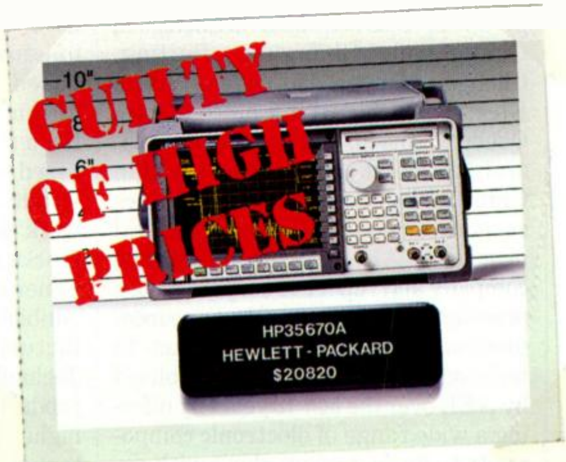
The SR780 FFT Spectrum Analyzer
- Is Faster
- Has a Wider Frequency Range
- Is Easier to Use
- Has More Standard Features
- And Costs Half as Much

The HP35670A Spectrum Analyzer
- Is Slower
- Has a Smaller Frequency Range
- Is Harder to Use
- Has Fewer Standard Features
- And Costs Twice as Much

The Evidence:

Exhibit A

	SR780	HP 35670A
2 Ch. Freq Range	102.4 kHz	51.2 kHz
Real-time BW	102.4 kHz	12.8 kHz
Source Distor.	<-80 dBc(<30kHz)	<-60 dBc(<30kHz)
Swept-Sine	Standard	$1020
1/3 Octave Analysis	Standard	$2040
Arb. Source	Standard	$510
Std. Memory	2 Msamples	500 kSamples
Price w/options	$9,950	$20,820



We're so confident you'll prefer the SR780 two channel spectrum analyzer from Stanford Research Systems over any competing analyzer that we'll send you one to try with no obligation. We're convinced that you will see why customers with applications including modal testing, control system design, filter design, audio research, and environmental noise measurements have switched to the SR780. For a detailed transcript of all the evidence, just call us at (408) 744-9040.

The Verdict:

The SR780 wins on all counts. Don't believe it? We'll let you examine the evidence yourself.

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READER SERVICE 238

JOHN NOVELLINO
TEST & MEASUREMENT

"A thumbnail look at what is happening in the world of distribution."

Future Electronics Acquires AEL

The Chinese electronics market constitutes one of the largest business opportunities in the world, and Future Electronics Inc. has jumped nto the arena with its acquisition of Advanced Electronics Ltd. (AEL), a China-based distributor of Morotola semiconductor products. AEL has offices in Shenzhen, Guangzhou, Shanghai, Beijing, Chengdu, Nanjing, and Wuhan. Future Electronics, based in Pointe Claire, Quebec, Canada, said it would immediately establish liaison offices within China under the Future Electronics corporate name. Y.C. Wong, general manager of AEL, will remain with the company and report to corporate vice president Rick Hawron. The announcement said Future Electronics "plans to build on the excellent base establised by AEL over the last 12 years by offering a wide range of electronic components to its customers along with extensive inventory availability, design engineering personnel, and state-of-the-art electronic commerce and material-management systems."

PMC-Sierra Picks EBV Electronics

EBV Electronics Inc. is now North American distributor for PMC-Sierra's line of high-speed networking semiconductors for ATM, Ethernet, T1/E1, and Sonet/SDH applications. EBV Electronics, a San Diego-based specialist distributor within the Raab Karcher Electronics Group, will provide such services as inventory management, automated warehousing, auto-replenishment, and EDI ordering. "EBV Electronics' semiconductor focus, coupled with their technical sales engineer program, make them the ideal partner to help us meet increased demand and improve service for our customers' engineering and procurement organizations," said Haresh Patel, PMC-Sierra's vice president of sales. "This agreement will give our customers access to the value-added distribution services needed to meet the pressure to dramatically shorten time to market."

Memory, PC-Cards Broaden Line

Bell Microproducts Inc. has broadened its PC card and memory module product line while boosting its contract manufacturing capability. The San Jose-based firm will distribute Simple Technology Inc.'s memory modules, flash storage devices, and PC-card-based network adapters and modems. In addition, Bell Microproducts will work closely with research analysts at the Santa Ana company to evaluate customer needs, ensure component compatibility, and reinforce contract manufacturing capability. "Simple Technology is a good fit in Bell Microproducts' overall strategy of providing higher levels of integration to our customers," said Ron Mabry, senior vice president of semiconductor marketing at Bell Microproducts. In addition to product distribution, Bell Microproducts offers systems integration, testing, kitting, and contract manufacturing of pc-boards and subsystems through its Quadrus Manufacturing Div.

Time Electronics Adds C&K Line

As part of its effort to add vendors and support customers' desire to consolidate purchasing through a select number of component suppliers, Time Electronics has added C&K Components to its line card. C&K, of Watertown, Mass., produces electromechanical products for a wide variety of industrial applications. Time Electronics, a member of Avnet Inc.'s OEM Marketing Group, said adding franchises like C&K is consistent with an intent to offer complete one-stop shopping for interconnect, passive, and electromechanical products. "C&K is one of the world's premier switch vendors," said Harley Feldberg, Time's executive vice president of sales and marketing. "Our partnership not only offers Time customers one of the world's broadest ranges of miniature switches but also the ability to further consolidate the electromechanical vendor base."

Reptron Picks Up IC Line

A line of linear and mixed-signal ICs from Linfinity Microelectronics Inc., Garden Grove, Calif., is now being offered by Reptron Electronics Inc. The ICs are aimed at portable and desktop power systems, as well as data-communications applications. Michael Sivetts, director of worldwide distribution sales at Linfinity, said one factor in the decision to sign on with Reptron was the Tampa, Fla., distributor's value-added services, including the use of Linfinity's backlight inverter in Reptron's fast-growing flat-panel display kitting market. Linfinity's products, particularly the backlight inverter module, will complement Reptron's existing product offerings from Sharp Electronics, notes Gary Bolohan, president of Reptron's Distribution Div. "The Linfinity line also enhances and supports Reptron's technical program to offer customers a customized solution by designing and engineering-in components to serve specific needs," he said.

WESCO Handling Fiber-Optic Cable

WESCO Distribution Inc., Pittsburg, Penn., has become the national distributor for Chromatic Technologies Inc. (CTI), Franklin, Mass. WESCO's Data Communications Div. will sell CTI's broad line of loose-tube and tight-buffered single-mode and multimode optical cables through the distributor's 320 branches and will have access to the company's engineering services. Michael Ludwig, division director and general manager, notes that industry analysts predict that fiber-optic cables will continue to capture increased market share, growing to over 22% of the market for total-premises wiring transmission media this year. "CTI's diverse product line and engineering expertise, combined with our national distribution capabilities will better position WESCO to meet our customers' increasing demand for fiber-optic cable," he said.

Expanded Catalog From Mouser

Mouser Electronics' latest catalog of electronic components has been expanded to include more than 69,000 products from over 135 manufacturers. The catalog is available in paper or CD-ROM form. The latter includes the entire catalog, a new products guide, product and vendor listings, and service options like an order form and credit application, a direct link to Mouser's web site, and more than 1850 spec sheets. To get a free copy of either version, contact Mouser at (800) 992-9943; fax (817) 483-0931; e-mail: catalog@mouser.com; or visit their web site at www.mouser.com.

News Pubs From Hamilton Hallmark

A special edition of Hamilton Hallmark's *Technology Review*, titled "Logic Migration," familiarizes customers with new logic technologies available and helps them select those that best meet their needs. The publication includes comprehensive strategic overviews from the major vendors. Also out is the company's latest product directory: the *Embedded & DSP Product Directory*. The publication offers product information about embedded devices and digital signal processors in an effort to help engineers identify the exact products needed for their unique designs. Quarterly updates of this and other directories are posted on the company's web site, www.hh.avnet.com.

People On The Move

Greg Provenzano was named president and CEO of Insight Electronics Inc., San Diego. He began his career at Insight in 1986 as division manager and Southern California regional manager. In 1991 he became marketing director responsible for Elantec, Siemens, and Xilinx...Lionel Wallace joined EBV Electronics Inc., San Diego, as division manager in Huntsville, Ala. He had been a regional sales manager at Insight Electronics. Karen Gonzalez joined EBV as its first division manager in Tampa, Fla. She had been with All American Semiconductor Inc., Miami...Diana White was promoted to director of product management at Schuster Electronics Inc., Cincinnati, Ohio. Daryl Moore was promoted to corporate product marketing manager.

Gender Equity Thrives In The Information Technology Industry

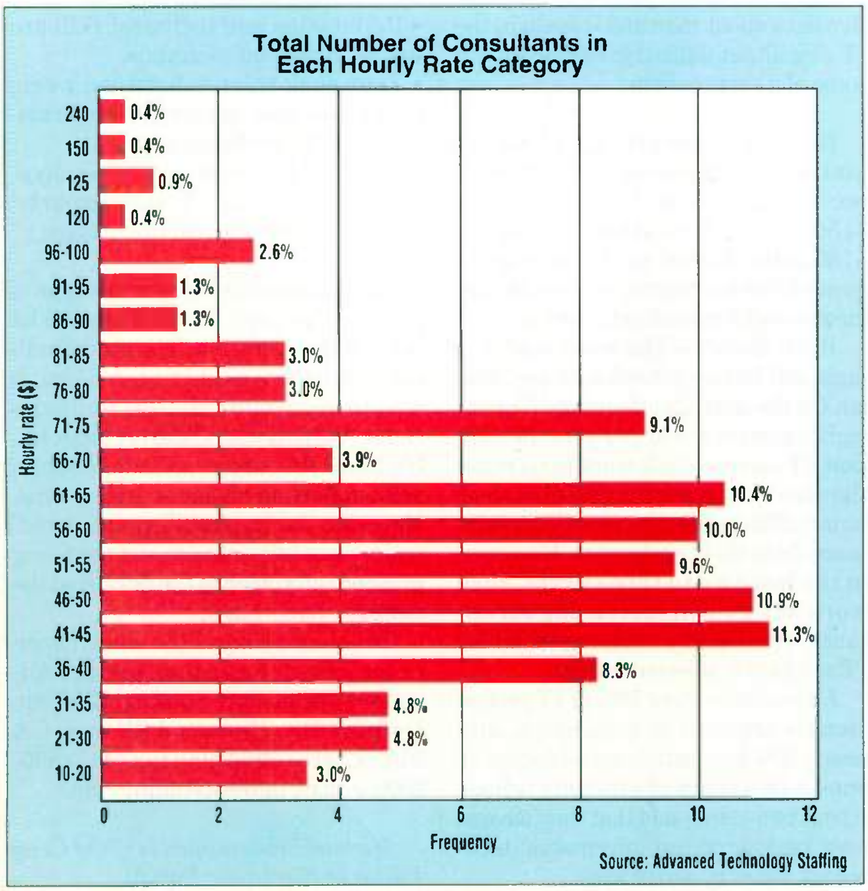
Michael Sciannamea

You're a single male whose life revolves almost completely around computers. You like films, books, and music that most people would consider offbeat. You have a ponytail, and you also have a penchant for wearing black clothes, even in the heat of summer. In other words, you fit the typical profile of an information technology (IT) professional, right? Wrong! In reality, that description couldn't be further from the truth.

A new white paper entitled "Women IT Consultants Are Winning The Wage War" shows that women, although outnumbered by a 4-to-1 margin by their male IT counterparts, share the same types of skills, earnings, and professional goals. These are the basic findings of the study excerpted from a new industry book *The Information Elite* (IT Insights, 1997), written by Dominique S. Black, CEO of Advanced Technology Staffing, Redwood Shores, Calif., and Richard Andreini, president and CEO of Cascade Associates. The results of the study were announced at the recent Women in Technology Conference, held in Santa Clara, Calif.

Reality Vs. Illusion

The above example of the "typical" IT professional is completely debunked in the study. According to the survey, most IT consultants today are likely to be male (80%), but female consultants are on the rise (20%). They tend to be at least 36 years of age, well-educated, certified, and married homeowners with children. On the other hand, not everyone fits that particular mold, either.



Source: Advanced Technology Staffing

In the past, IT professionals tended to be male, partially because men historically far outnumbered women when it came to enrollment in undergraduate, graduate, and postgraduate studies in technical subjects such as engineering, physics, and computer science. However, increasing numbers of women are choosing to study technical subjects. Their proportions in classrooms and lecture halls are rising in all areas of technology.

"Brain power, knowledge, experience, and professionalism measure success in IT consulting, regardless of gender," says Dominique S. Black. "These men and women drive change in new computer technology. First, they don't have to manage daily computer operations—a full-time job in most enterprises. Second, they have much wider knowledge and understanding of emerging technology."

It Keeps Growing And Growing

The opportunities that already exist for the independent IT consultant workforce will continue to grow at a dramatic rate. According to the study, the IT workforce will grow to over 2,000,000 by the year 2000, a 17% per year increase from the present total of 1,250,000. And the future looks even more promising for women. Between 1997 and 2000, the number of female IT consultants will rise from 20% to 30% of the professionals working in the field. They will more than triple the current figure of 250,000 to 700,000. The study analyzes the technical areas of networking, Internet/intranet, client/server, software engineering/development, software quality assurance and testing, applications/management consulting, and legacy applications. The respondents comprised current IT consultants whose hourly rates ranged from $10 to $240 per hour *(see the figure)*.

Another stereotype that the study puts to rest is the idea that IT professionals are "between jobs." As a matter of fact, it's just the opposite. These people consider themselves independent, self-supporting business types. To support that finding, the *San Jose Mercury-News*, San Jose, Calif., in an article published on Feb. 15, asked full-time IT programmers, both male and female, working in Silicon Valley, if they ever considered working as an independent contractor. Most of them said they would, especially after taking into account how many IT consultants they see around them.

What can be concluded from the study is that the number of IT professionals will grow. The white paper also predicts that once an individual establishes himself or herself as an IT consultant, he or she will most likely not return to full-time corporate life.

Facts And Figures

The white paper provides comparative data about men and women in the IT consultant industry. Following are some of its conclusions:

Earnings—The average IT consultant has an income of over $100,000 per year. About 5% make over $150,000 and another 5% make $180,000+. Based on this research, gender has no bearing on the annual income an IT consultant garners.

Work Habits—The work habits of male and female consultants are similar. On the average, they take four-to-eight vacation weeks per year. In addition, IT professionals want to increase the amount of work they do from their home offices, but are meeting resistance from their customers. However, in the last two to three years, such work has gained increasing acceptance. One rapidly evolving trend for IT workers is telecommuting.

Education—Over 70% of IT professionals are college graduates, and nearly 50% have an advanced degree or one-to-two years of graduate school. About two-thirds said that they have at least two significant information-technology industry certificates.

Work Experience—More than 61% of those polled have at least 15 years work experience; 22% have at least 10 years. In the specific area of consultant contracts, 29% have at least 10 years experience, and 15% have at least seven years. There was a wide variety of contract duration periods. Roughly 38% of respondents were contracted for one year; another 39% in the six- to 11-month range. Most of the IT consultants asked preferred longer-term projects.

Life vs. Work—Both male and female IT consultants were asked which professional and personal concerns were of the most importance to them. The results were virtually the same. They both ranked reputation, a balanced life, technical skills, and earnings (in that order) as the most important issues in their lives, both professionally and personally.

Who Are These People?

After all was said and done, the study had four basic conclusions, illustrated in the white paper:

- IT consultants have definite visions on balancing home and work life.
- Reputation and technical skill are just as important as income.
- They seek balance between work, home, how they gather their information, and their education.
- Female IT consultants are equivalent to their male IT counterparts, both professionally and in earnings.

When describing a particular type of person, the word "typical" has to be used with discretion. The study indicates that the typical IT professional is a male in his mid-thirties; well-educated; married with children; has a stable home life; and is an independent, self-supporting business professional. However, the "typical IT professional" will have to take into account the rising presence of women in the field. And the numbers back that up.

To obtain a copy of the white paper, or for more information, contact Advanced Technology Staffing, 220 Twin Dolphin Dr., Redwood Shores, CA 94065; (415) 596-2800; fax (415) 596-2000; e-mail: info@atstaffing.com.

Michael Sciannamea is Chief Copy Editor of Electronic Design.

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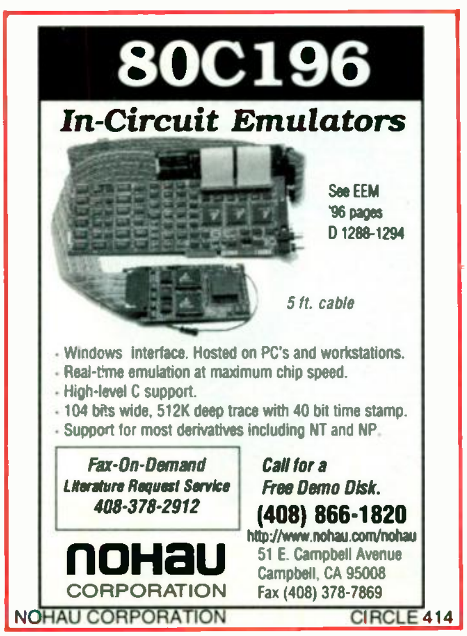
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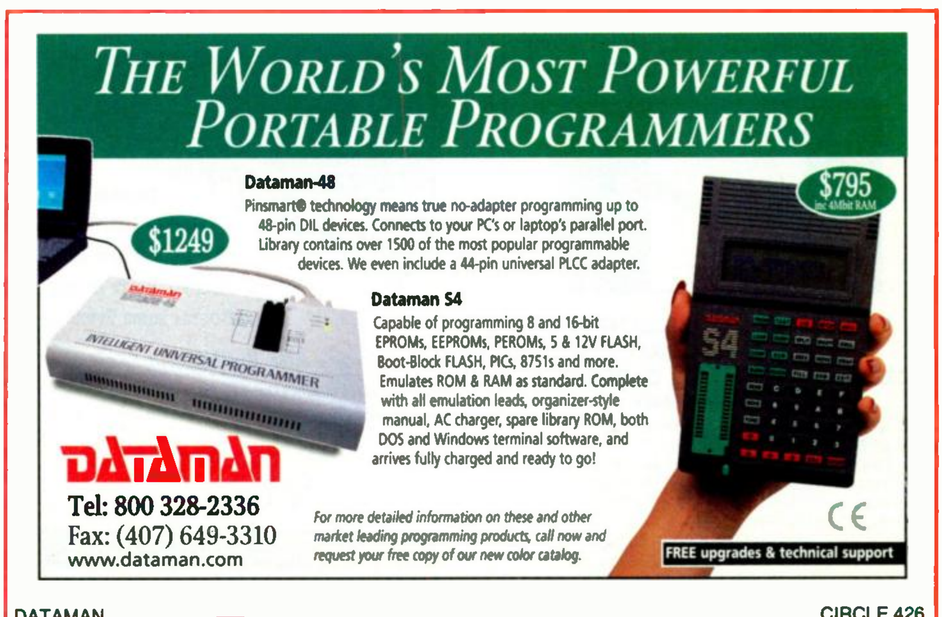
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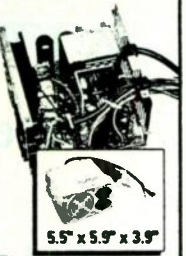

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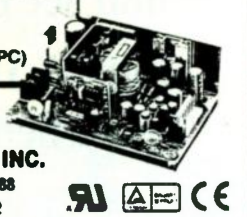

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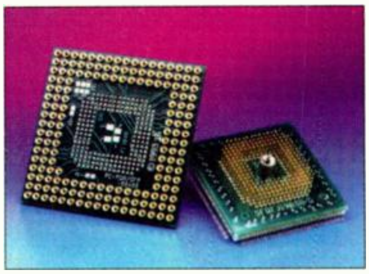

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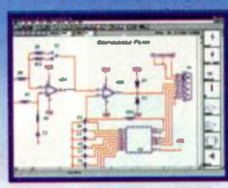

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Director Of Marketing: Walker Johnson
San Jose, CA (408) 441-0550, FAX: (408) 441-6052
Production Manager: Eileen Slavinsky
Hasbrouck Heights, NJ; (201) 393-6093
Marketing Research Administrator: Deborah Eng.
Hasbrouck Heights. NJ; (201) 393-6063

Advertising Sales Staff

Hasbrouck Heights: Judith L. Miller
Sales Asst.: Judy Stone Rodriguez
611 Route #46 West, Hasbrouck Heights, NJ 07604;
Phone: (201) 393-6060, Fax: (201) 393-0204
Boston & Eastern Canada: Ric Wasley
Sales Support: Karen Harrison
60 Hickory Drive, Waltham, MA 02154;
Phone: (617) 890-0891FAX: (617) 890-6131
North Califonia/Colorado: Chuck Signor (408) 441-0550
Chicago/Midwest: Lisa Zurick
Sales Assistant: Dawn Heili
180 N. Stetson Ave., Suite 2555 Chicago, IL 60601;
(312) 861-0880 FAX: (312) 861-0874
North California/Utah/N.Mexico/Arizona:
James Theriault (408) 441-0550
Los Angeles/Orange County/San Diego: Ian Hill
Sales Asst: Patti Kelly 16255 Ventura Blvd.,
Suite 200 Encino, CA 91436;
(818) 990-9000 FAX: (818) 905-1206
San Jose:
Jeff Hoopes, Chuck Signor, James Theriault
Sales Support: Liz Torres & Rachel Ross 2025 Gateway Pl.,
Suite 354 San Jose, CA 95110;
(408) 441-0550 FAX: (408) 441-6052 or (408) 441-7336
Pacific N.W. & Western Canada:
Jeff Hoopes (408) 441-0550
Texas/Southeast: Bill Yarborough
1557 Bracher St. Houston, TX 77055;
Phone: 713-984-7625. FAX: 713-984-7576
Direct Connection Ads & Direct Action Cards:
Kim Stanger (201) 393-6080

General Manager, European Operations: John Allen
36 The Green, South Bar Banbury. Oxford OX 16 9AE, U.K.
Phone: 44 (0)-1- 295-271003 FAX: 44 (0)-1- 295-272801
Netherlands, Belgium: Peter Sanders,
S.I.P.A.S. Rechtestraat 58 1483 Be De Ryp,
Holland Phone: 011-31-299-671303 Fax: 011-31-299 671500
France: Fabio Lancellotti
Defense & Communication
10 Rue St. Jean 75017 Paris France
Phone: 33-142940244. FAX: 33-143872729
Spain/Portugal: Miguel Esteban
Publicidad Internacional Pza.
Descubridor Diego de Ordas,
1 Escalera, 2 Planta 2D 28003 Madrid, Spain
Phone: 91/4416266 FAX: 91/4416549
Scandinavia: Paul Barrett
I.M.P. Hartswood, Hallmark House.
25 Downham Road, Ramsden Heath,
Billiricay, Essex, CM 11 1PV, UK.
Phone:44(0)-1-268-711560, Fax:44(0)-1-268-711567
Germany, Austria, Switzerland: Friedrich Anacker
InterMedia Partners GmbH Deutscher Ring 40
42327 Wuppertal, Germany
Phone: 49 (0) 202 271 690 Fax: 49(0) 202 271 6920
Hong Kong: Kenson Tse
IDG International Marketing Services
Suite 25F, One Capital Place,18 Luard Road,Wanchai, Hong Kong
Tel: 852-2527-9338. Fax: 852-2529-9956
Israel: Igal Elan, Elan Marketing Group
22 Daphna St., Tel Aviv, Israel
Phone:972-3-6952967 FAX: 972-3-268020
Toll Free in Israel only: 177-022-1331
Japan: Hirokazu Morita,
Japan Advertising Communications
Three Star Building 3-10-3-Kanda Jimbocho
Chiyoda-Ku, Tokyo 101, Japan
Phone: 3 3261 4591. FAX:3 3261 6126
Korea: Young Sang Jo,
Business Communications Inc.
K.P.O. Box 1916, Midopa Building 146
Dangju-Dong, Chongo-Ku, Seoul, Korea
Phone: 011-82-2-739-7840 FAX: 011-82-2-732-3662
Taiwan: Charles Liu, President,
Two-way Communications, Co., Ltd.
12F/1, No.99, Sec.2
Tun-Hwa South Road, Taipei, Taiwan.
Phone: 011-886-2-707-5828;FAX: 011-886-2-707-5825
United Kingdom: John Maycock
John Maycock Associates
Provincial House
Solly St. Sheffield S1 4BA
Phone: 0114-2728882. FAX: 0114-2728881

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