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PA41	100V-350V	120mA	2mA	40V/µs
PA42	100V-350V	120mA	2mA	40V/µs
PA85	30V-450V	350mA	25mA	1000V/µs
PA87	100-450V	300mA	3.8mA	20V/µs
PA88	30V-450V	200mA	2mA	30V/µs
PA89	150V-1200V	100mA	6mA	16V/µs

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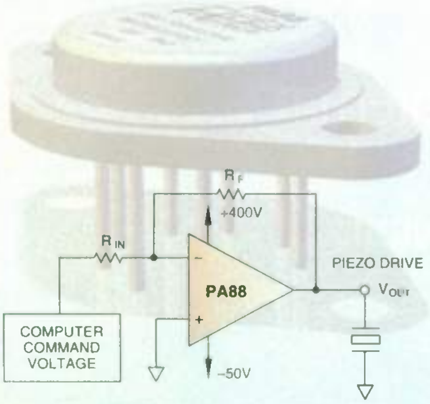
When concerned about system power supply drain or heat buildup, the **PA88** offers cool running with only 2mA max standby current. With a total supply rating of 450V and an output capability of 200mA peak, the **PA88** is up to your design challenges. The **PA88M** is the military screened version.



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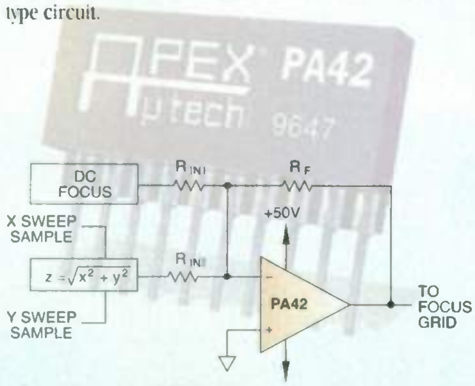

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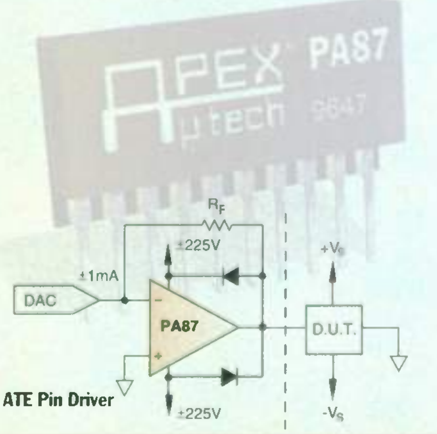
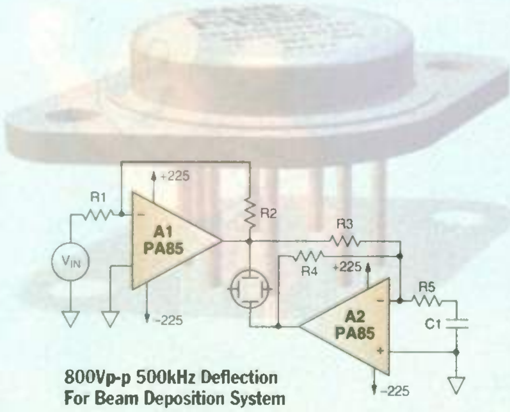


ATE Pin Driver

The Speed Demon

If it's speed you need, the **PA85** is the fastest high voltage op amp you can buy. A slew rate of 1000V/µs, a total supply capability of 450V and peak currents to 350mA, the **PA85** is well suited to high speed drives for PZTs, optical switches and other capacitive loads. The gain bandwidth product of 100MHz insures AC fidelity. It's also available in a military screened version, the **PA85M**.



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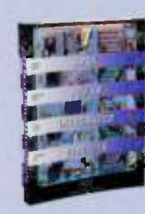

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1976 Certificate of Merit	1992 Certificate of Merit

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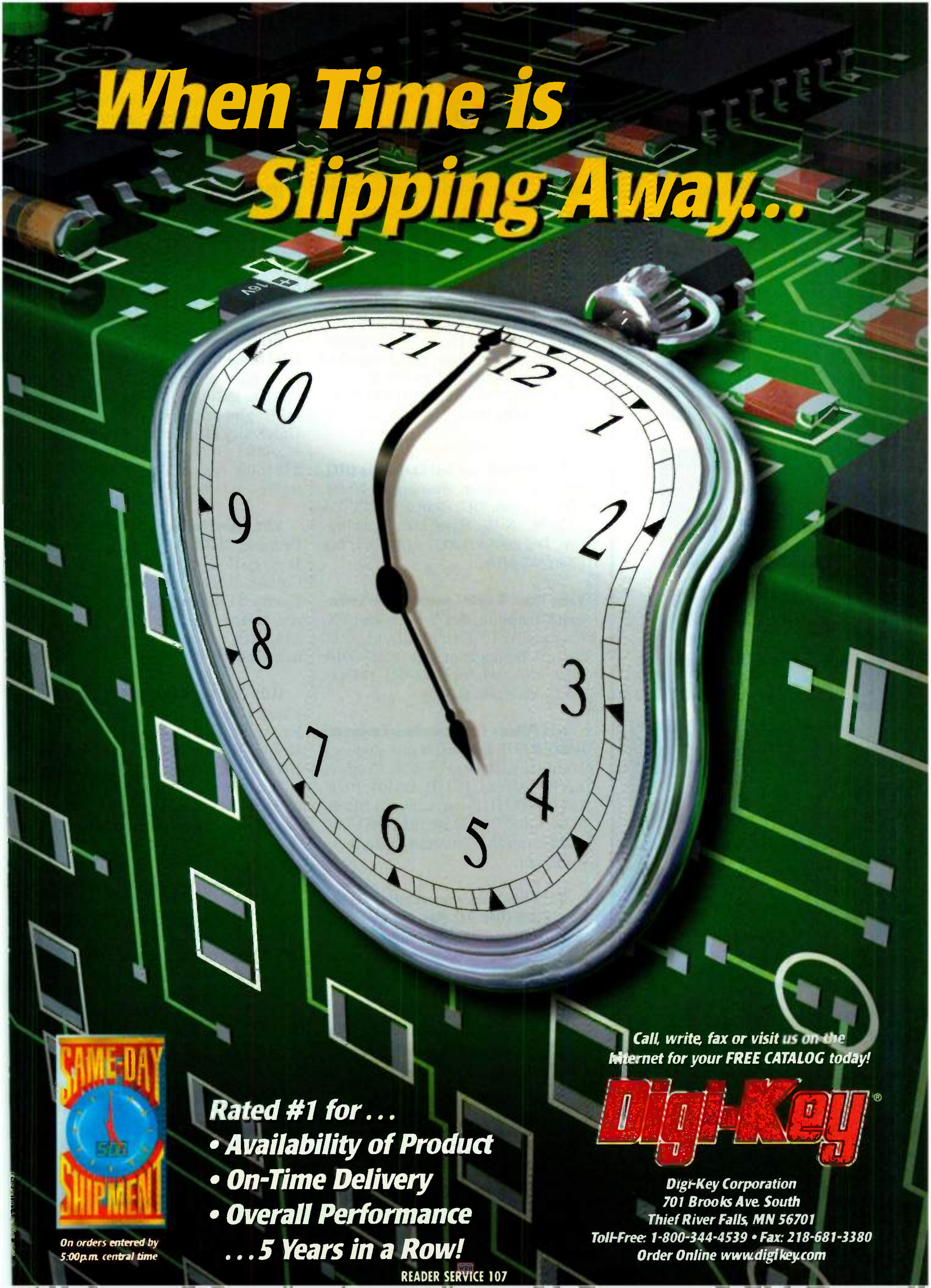
Published by Penton Publishing

Electronic Design Information Group:
Editorial Director: **STEPHEN E. SCRUPSKI** (201) 393-6070
Publisher: **JOHN G. FRENCH** (201) 393-6255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SYSTEMS 97, Oct. 27-31. Munich Trade Fair Center, Munich, Germany. Contact Messe Munchen GmbH, Messegelande, D-80325 Munchen, +49 (89) 51070; fax +49 (89) 51 07506; Internet: http://www.sysems.de; e-mail: info@messe-muenchen.de.

19th Annual International Conference of the IEEE Engineering in Medicine & Biology Society, Oct. 29-Nov. 2. Chicago Marriott Hotel, Chicago, IL. Sally Chapman, Secretariat, National Res. Council of Canada, Bldg. M-55 Rm. 393, Ottawa, KIA OR8, Canada; (613) 993-4005; fax (613) 954-2216.

NOVEMBER

IEEE International Test Conference (ITC), Nov. 1-5. Sheraton Washington Hotel, Washington, DC. Contact ITC, 655 15th St., N.W., Suite 300, Washington, DC 20005; (202) 639-4164; fax (202) 347-6109.

Voice, Video, & Data Communications Conference & Exhibition, Nov. 2-6. Dallas, TX. Contact SPIE Exhibits Dept., P.O. Box 10, Bellingham, WA 98227-0010; (360) 676-3290; fax (360)-647-1445; e-mail: exhibits@spie.org.

IEEE Military Communications Conference (MILCOM '97), Nov. 2-7. Hyatt Regency Monterey, Monterey, CA. Contact Kathy Lukens, P.O. Box 3504, Bldg. 158 O/MO-H1, Sunnyvale, CA 94088-3504; (408) 756-6196; fax (408) 756-6139; e-mail: k-lukens@lmsc.lockheed.com.

IEEE Global Telecommunications Conference (GLOBECOM '97), Nov. 4-8. Phoenix, AZ. Contact Nigel Reynolds, 15436 N. First Ave., Phoenix, AZ 85023; (602) 942-5583; fax (602) 942-4542; e-mail: nigelaz@aol.com.

WESCON '97, Nov. 4-6. San Jose Convention Center and Santa Clara Convention Center, San Jose and Santa Clara, CA. Contact Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045-3194; (800) 877-2668; fax (310) 641-5117; e-mail: wescon@ieee.org.

IEEE Nuclear Science Symposium (NSS '97), Nov. 8-15. Albuquerque, NM. Contact Roger Gearhart, SLAC, Post Office Box 4349, Stanford, California 94309; (415) 926-2709; fax (415) 926-4999.

IEEE Intelligent Transportation Systems Conference (ITS '97), Nov. 9-12. Boston Park Plaza Hotel, Boston, MA. Contact Richard Sparks, 8 Richard Rd., Bedford, Massachusetts 01730; (617) 862-3000; fax (617) 863-0586; e-mail: r.sparks@ieee.org.

IEEE International Conference on Computed Aided Design (ICCAD), November 9-13. Red Lion Hotel, San Jose, California. Contact Ralph H.J.M. Otten, Electrical Engineering Department, Delft University of Technology, Mekelweg 4, 2628 CD, Netherlands, +31 15-2781600; fax +31 15-2786190; otten@et.tudelft.nl.

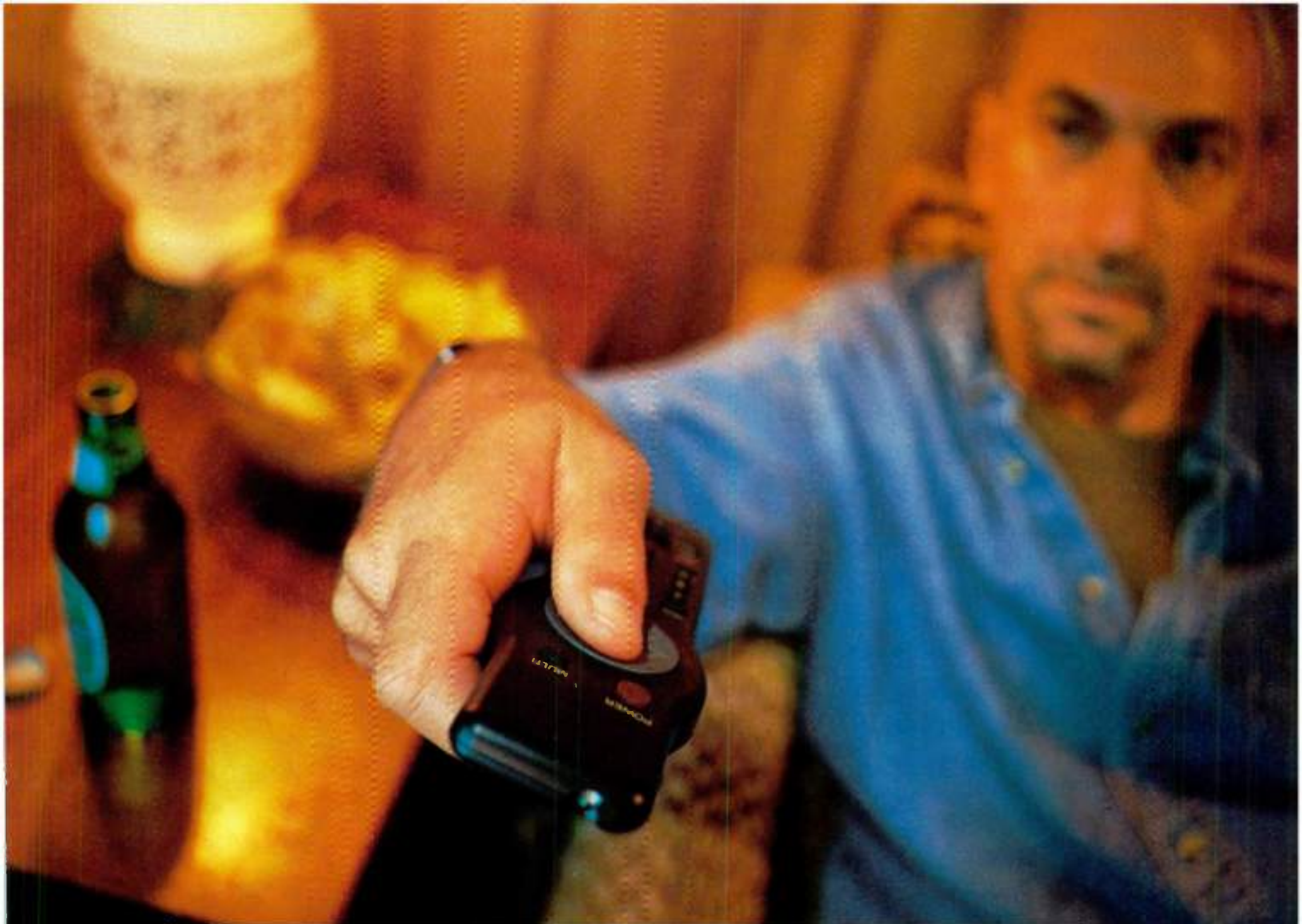
23rd Annual Conference of IEEE Industrial Electronics (IECON '97), Nov. 9-14. Hyatt Regency Hotel, New Orleans, Louisiana. Contact Michael Greene, 200 Broun Hall, Electrical Engineering, Auburn University, Auburn, Alabama 36849-5201; (334) 844-1828; e-mail: greene@eng.auburn.edu.

LEOS '97, November 10-13. Crowne Plaza Parc Fifty Five Hotel, San Francisco, California. Contact Melissa K. Estrin, IEEE/LEOS, 445 Hoes Ln., P.O. Box 1331, Piscataway, New Jersey 08855-1331, (908) 562-3896; fax (908) 562-8434; e-mail: mestrin@ieee.org.

Productronica '97, Nov. 11-14. Messegelande, Munich, Germany. Contact Messe Munchen GmbH, Messegelande, D-80325 Munchen, Germany; +49 (89) 51 07-0; fax +49 (89) 51 07-506; e-mail: info@messe-munchen.de; Internet: http://www.Productronica.de.

Supercomputing '97, November 15-21. San Jose Convention Center, San Jose, California. Contact IEEE Computer Society, 1730 Massachusetts Avenue, N.W., Washington, DC 20036-1992; (202) 371-1013; fax (202) 728-0884; http://www.computer.org.

Asian Test Symposium, Nov. 17-19. Akita, Japan. Contact Y. Takamatsu, +81 89 927-9955; e-mail: takamatsu@cs.ehime-u.ac.jp.



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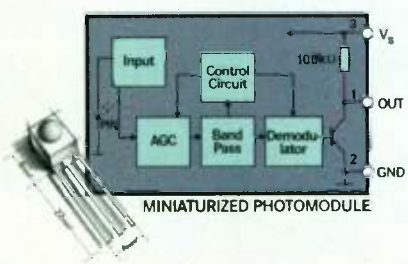

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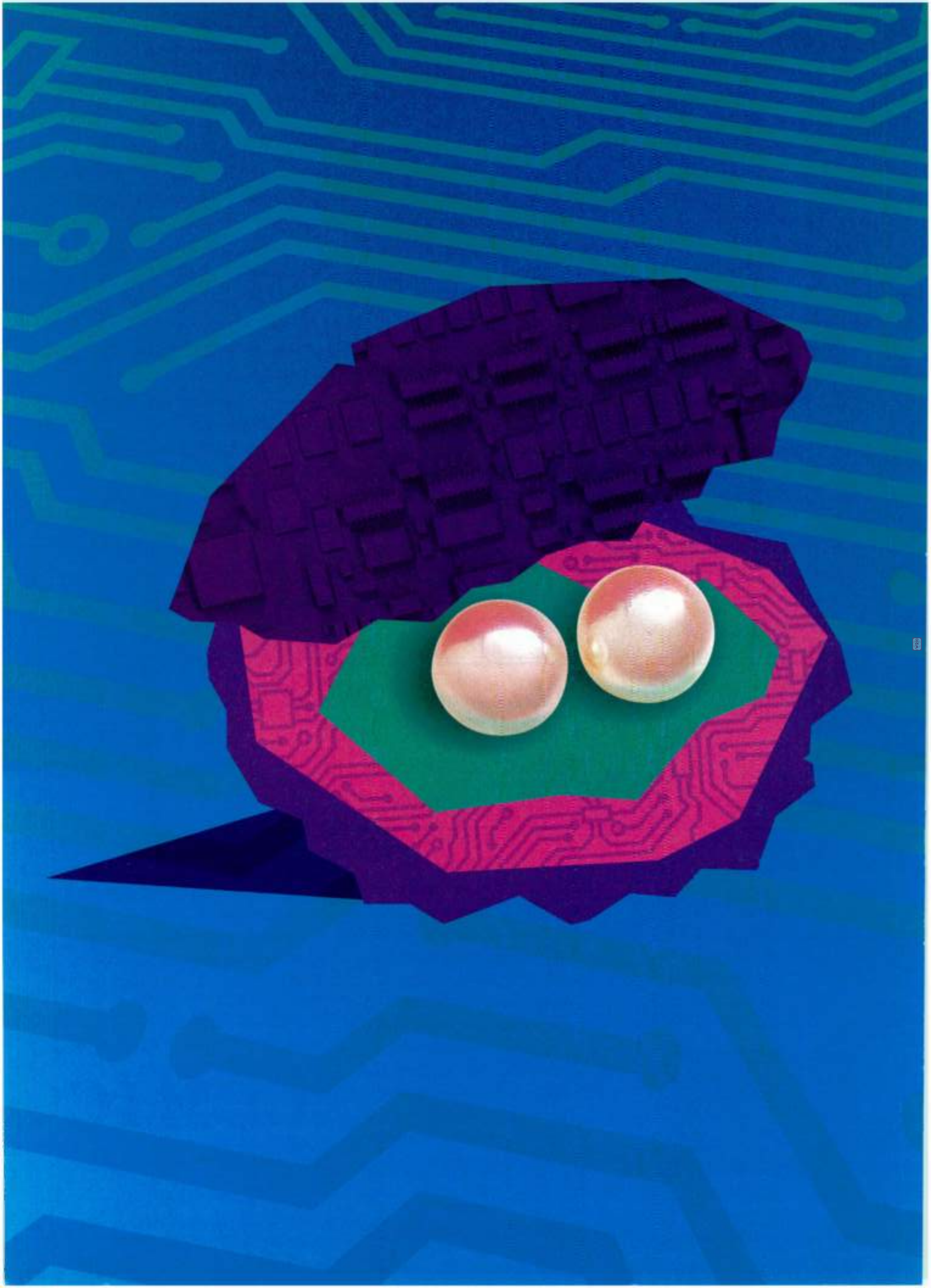

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COMDEX/Fall '97, Nov. 17-21. Las Vegas Convention Center, Las Vegas, NV. Contact Softbank Comdex Inc., 300 First Ave., Needham, MA 02194-2722; (617) 433-1500; Internet: http://www.comdex.dom.

IPC National Conference: Solutions for Ultra-High-Density PWBs, November 20-21. Biltmore Hotel, Santa Clara, California. Contact John Riley, IPC director of education, (847) 509-9700 ext. 308.

DECEMBER

Winter Simulation Conference (WSC '97), Dec. 7-10. Renaissance Waverly Hotel, Atlanta, GA. Contact David Withers, LEXIS-NEXIS, P.O. Box 933, Dayton, OH 45401; e-mail: David.Withers@lexis-nexis.com.

IEEE International Electron Devices Meeting (IEDM), Dec. 7-11. Washington Hilton & Towers, Washington, DC. Contact Phyllis Mahoney, Widerkehr & Assoc., 101 Lakefrorest Blvd., Suite 270, Gaithersburg, MD 20877; (301) 527-0900; fax (301) 527-0994; e-mail: pwmahoney@aol.com.

36th IEEE Conference on Decision & Control, December 8-12. Hyatt Regency, San Diego, California. Contact Ted E. Djaferis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, Massachusetts 01003; (413) 545-3561; fax (413) 545-1993; e-mail: djaferis@ecs.umass.edu.

Workshop on Internet Technology & Systems (WITS), Dec. 9-12. Marriott Hotel, Monterey, California. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, California 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

JANUARY 1998

Seventh Joint Magnetism & Magnetic Materials Conference (INTEMAG), January 6-9. Hyatt Regency Embarcadero Hotel, San Francisco, California. Contact John Nyenhuis, School of ECE, Purdue University West Lafayette, Indiana 47907-1285; (317) 494-3524; fax (317) 494-2706; e-mail: smag@ecn.purdue.edu.

Annual Reliability & Maintainability Symposium/Product Quality & Integrity (RAMS), January 20-22. Anaheim Marriott, Anaheim, California. Contact V.R. Monshaw, Consulting Services, 1768 Lark Lane, Cherry Hill, New Jersey 08003; (609) 428-2342.

Photonics West, January 24-30. San Jose, California. Contact the SPIE Exhibits Dept., Post Office Box 10, Bellingham, Washington 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

Seventh Security Symposium, Jan. 26-29. Marriott Hotel, San Antonio, Texas. Contact USENIX Conference Office, 22672 Lambert Street, Suite 613, Lake Forest, California 92630; (714) 588-8649; fax (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

IEEE Power Engineering Society Winter Meeting, January 31-February 5. Tampa, Florida. Contact Jim Howard, Tampa Electric Co., Post Office Box 111, Tampa, Florida 33601; (813) 228-4653; fax (813) 228-1333; e-mail: j.howard@ieee.org.

FEBRUARY 1998

IEEE International Solid-State Circuits Conference (ISSCC '98), February 5-7. San Francisco Marriott, San Francisco, California. Contact Diane Suiters, Courtesy Associates, 655 15th St. N.W., Washington, DC 20005; (202) 639-4255; fax (202) 347-6109; e-mail: isscc@courtesyassoc.com.

IEEE Applied Power Electronics Conference and Exposition (APEC '98), February 15-19. The Disneyland Hotel, Anaheim, California. Contact Pamela Wagner, Courtesy Associates, 655 15th St., N.W., Suite 300, Washington, DC 20005; (202) 639-4990; fax (202) 347-6109; e-mail: pwagner@courtesyassoc.com.

Conference on Optical Fiber Communication (OFC '98), February 22-27. San Jose Convention Center, San Jose, California. Contact Lisa Myers, OSA Conference Services, 2010 Massachusetts Ave., N.W., Washington, D.C. 20036-1023; (202) 416-1980; fax (202) 416-6100; e-mail: ofc.info@osa.org.

38th Israel Conference on Aerospace Sciences, February 25-26. Tel-Aviv & Haifa. Contact Technion-Israel Institute of Technology, Haifa 32000, Israel; 972-4-8292713; fax, 972-4-8231848; e-mail: alice@aerodyne.technion.ac.il.

MARCH 1998

Sixth Annual Embebbed Systems Conference East, March. 31-April. 2. Chicago's Navy Pier Festival Hall, Chicago, Illinois. Contact Miller Freeman Inc., 600 Harrison Street, San Francisco, California 94107; (415) 905-2354; fax (415) 905-2220; Internet: http://www.embedsyscon.com/.

APRIL 1998

Southeastcon '98, April 10-15. Hyatt Regency, Orlando International Airport, Orlando, Florida. Contact Parveen Ward, ECE Dept., University of Central Florida, Orlando, Florida 32816; (407) 823-2610; fax (407) 823-5835; e-mail: pfw@ece.engr.ucf.edu.

MAY 1998

IEEE International Conference on Evolutionary Computation, May 3-9. Ankorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@akaska.net.

IEEE International Conference on Neural Networks (ICNN '98), May 3-9. Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@akaska.net.

IEEE World Congress on Computational Intelligence, May 3-9. William A. Egan Civic and Convention Center, Anchorage, Alaska. Contact Patrick K. Simpson, Scientific Fishery Systems Inc. Post Office Box 242064, Anchorage, Alaska 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

Seventh IEEE International Fuzzy Systems Conference, May 3-9. Anchorage, AK. Contact Patrick K. Simpson, Scientific Fishery Systems Inc., P.O. Box 242065, Anchorage, AK 99524; (907) 345-7347; fax (907) 345-9769; e-mail: scifish@alaska.net.

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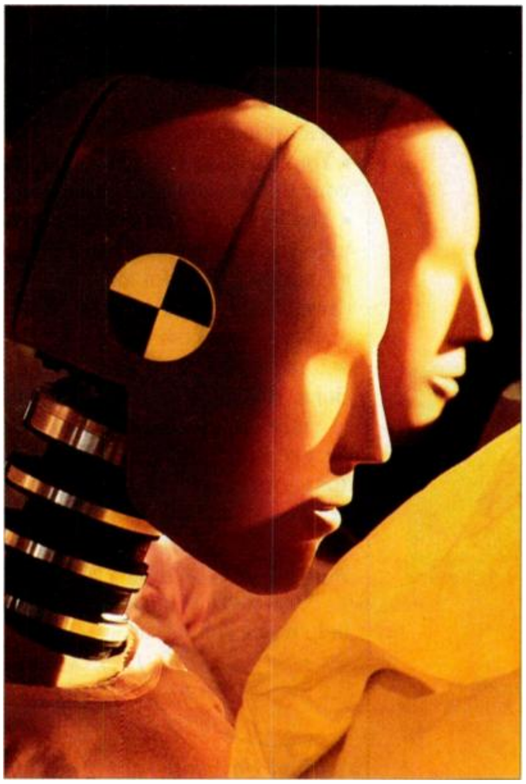

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EDITORIAL

What The Future Holds

Bodynets that link small computerized devices on our eyeglasses and belts with others, or software that can hold a conversation with a human. I have to admit, I'm a sucker for a good futurist. I've read the likes of Toffler, Sagan, and others who've made careers out of predicting what's coming down the road for humankind. I've read Verne, Bradbury, and other science-fiction scribes whose novels stirred the imagination. And when I stand in the check-out line at the supermarket, I always scan the Enquirer or Globe to find out when the world is going to end or the date Elvis is scheduled to reappear in Graceland.

Although I am a sucker for a good futurist, I am by no means a sucker for what they *predict*. I recall reading a book back in the early '60s by the one-time noted psychic Jeanne Dixon, who predicted that the Russians would first land on the Moon. Well, she was wrong about that, and a lot of other things, too. I realized from an early age to be wary of those who predict the future.

Recently, I had the opportunity to listen to Michael Dertouzos, director of the MIT Laboratory for Computer Science, speak about the future. Dertouzos, who has headed the lab since 1974, has a long and impressive list of credentials, including numerous patents. Here's a sampling of what he sees coming our way:

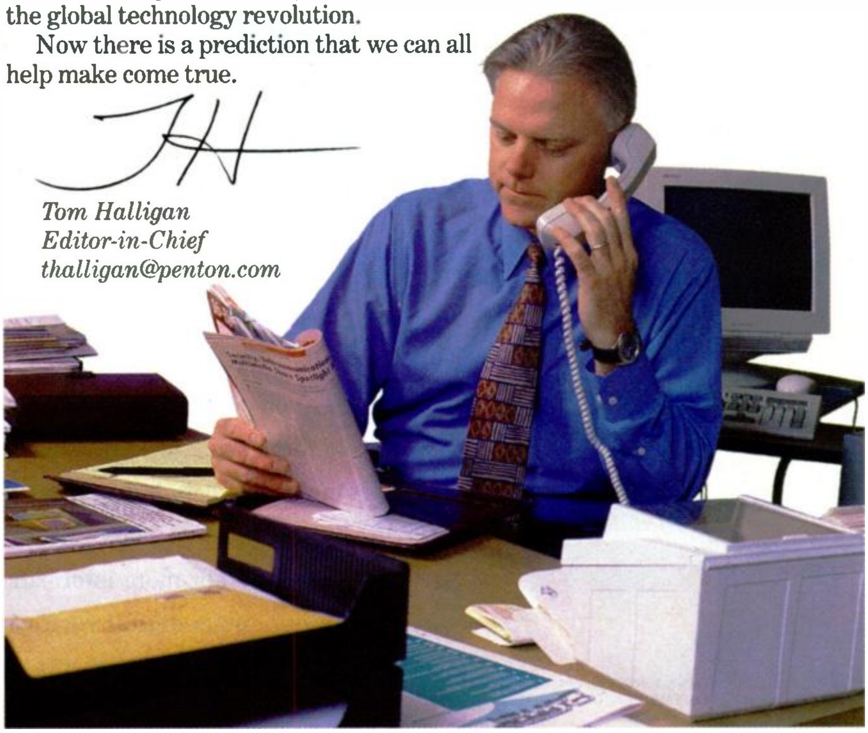
- Keyboards, windows, and menus will be supplanted eventually by speech-understanding programs.
- Your "bodynet" will let you make phone calls, check e-mail, watch TV, and pay your bills as you walk down the street.
- You'll be able to e-mail a caress—and more—as bodysuits, virtual reality, and video technology transform the nature of sex and romance.
- Groupwork, e-forms, automatization, and other "electronic bulldozers" will dramatically increase our productivity.

Dertouzos also is bullish on speech-recognition technology, and gave a demo where he dialed into a computer at MIT that fielded and responded to his questions. He said that the system has about a 90% comprehension rate.

Only time will tell whether Dertouzos' predictions come to pass. But what impressed me most was his call for the technological "haves" to share with the "have-nots." Dertouzos asserts that if we all do not make the effort now, the gap between rich and poor nations will continue to widen. He urged that everyone involved in high-technology should work to ensure that poorer nations share in the global technology revolution.

Now there is a prediction that we can all help make come true.

Tom Halligan
Editor-in-Chief
thalligan@penton.com



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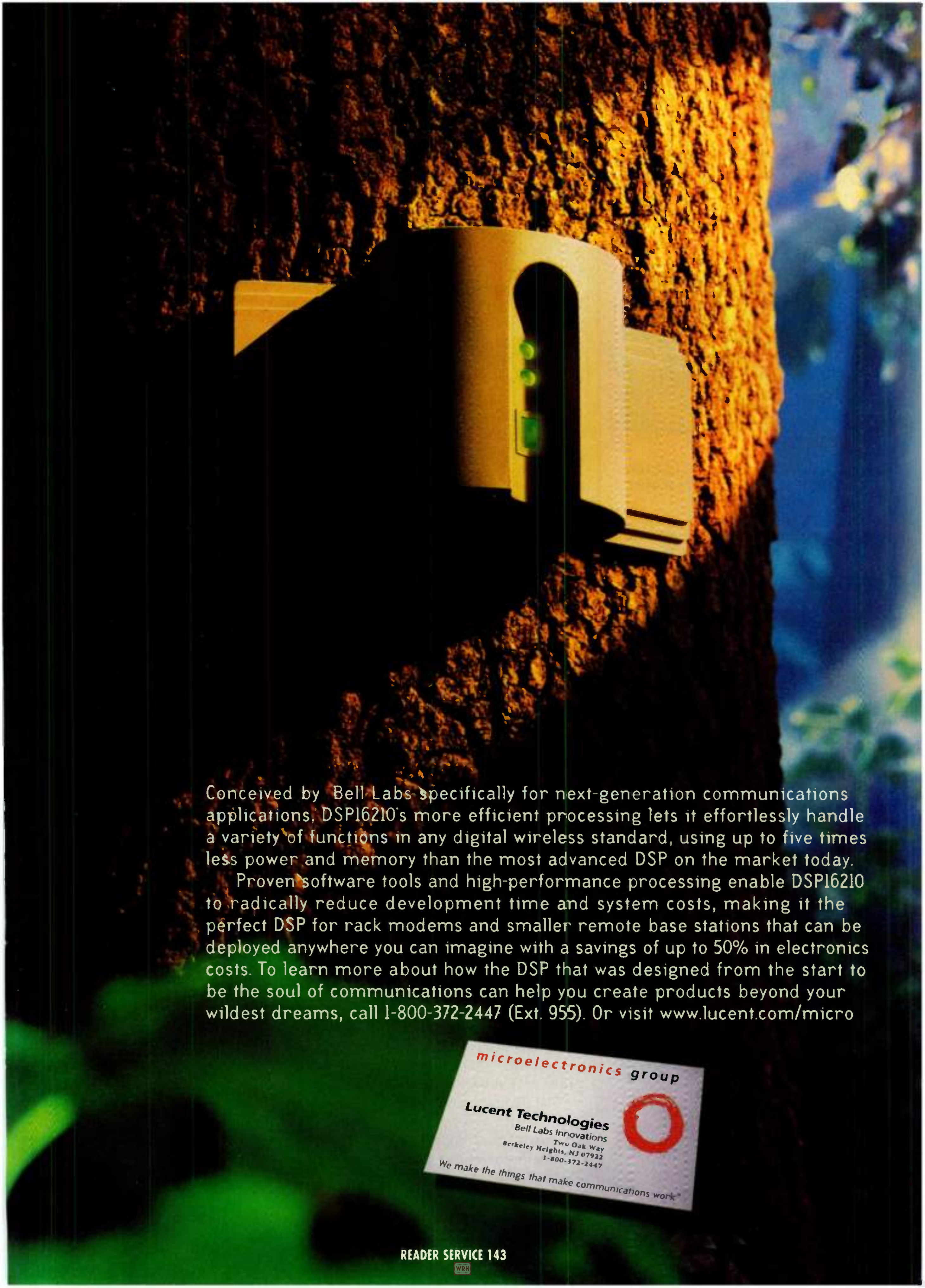
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Judging The Designs Of The Future

For the past number of years, I've served on a panel of judges for a University VLSI Design Contest sponsored by a large and well-known supplier of CAE tools. Although the prizes that are handed out are basically awards of tools for the winning universities and the recognition of the design work, the overall efforts of the students and advisors shows that they possess a broad range of circuit and basic engineering know-how. As a result, they will be able to leverage that knowledge when they enter the industry upon completion of their education.

The entries that already have been received this year for the contest have been loosely divided into two separate categories—novice and experienced. Each entry is judged on its soundness of engineering, clarity of the functional specification, the design methodology selected, and their physical implementation. Whether the entry was submitted from an experienced or inexperienced design team, all of the designs showed extremely creative thinking and practical design implementations. In this instance, all of the contest participants can be considered as "winners" in one form or another. Some of the more notable topics for the entries included a RISC DSP core; a systolic modular multiplier; an implantable cardioverter defibrillator; a systolic neural processor; a hybrid FPGA that combines look-up tables and PLD logic blocks; a monolithic wireless temperature sensor; a 9-bit pipelined 12.5-Msample/s analog-to-digital converter; and a multichip module for a 1-GHz multichip microprocessor.


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All of these entries provide solid explanations of the design approach and trade-offs that had to be made, and the implementation techniques that were applied based on the use of various design tools. Some are more detailed than others, but all of them show that our educational system is working—the students are combining their textbook learning with applied technology to craft designs that may very well compete with commercial products in the near future.

A contest such as this brings to light the positive energy and creativity that the students have, and it also shows the effectiveness of the educational system in preparing them for real design challenges. And, although there were a significant number of constraints that were imposed upon the students by the limited resources of the school, the capability of the available processing, and the length of the school semester, these design engineers of the future will face very similar limitations and challenges if they decide to go to work for a commercial company—such problems as time-to-market issues, process limitations, and so on.

Perhaps more companies in the industry should consider sponsoring design contests to cover all the different areas of technology. Indeed, there are many opportunities to expand the horizons of the students. At the same time, they can provide much-needed help to the universities in the form of design tools, grants, research and development contacts, and so on. I firmly believe that there are many innovative ways the industry can get involved to foster design creativity and innovation while also strengthening one of our most vital resources—the university system—which produces the forthcoming generations of designers and researchers.

The planning and effort that can be seen from the submissions of the students for this contest really gives me a very positive and hopeful feeling about the innovative minds that will soon be entering the commercial market. So, as far as I'm concerned, the judgment is in, and it is a win for everyone.

As always, all of your comments and suggestions on this or other topics that I write about are certainly appreciated. You can e-mail them to me at *dbursky@class.org*.

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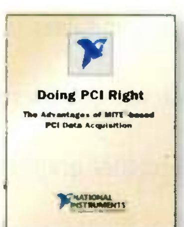

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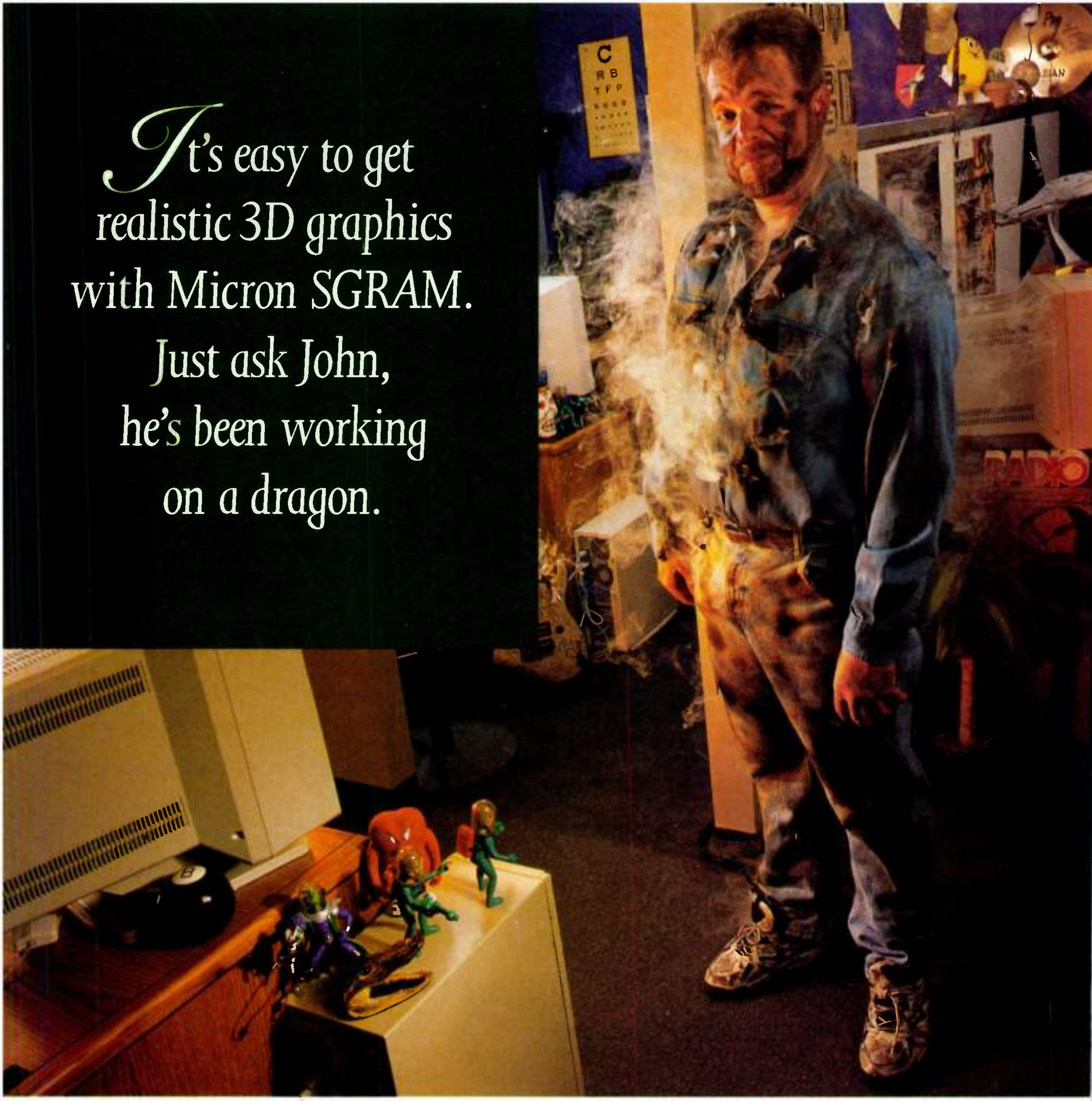

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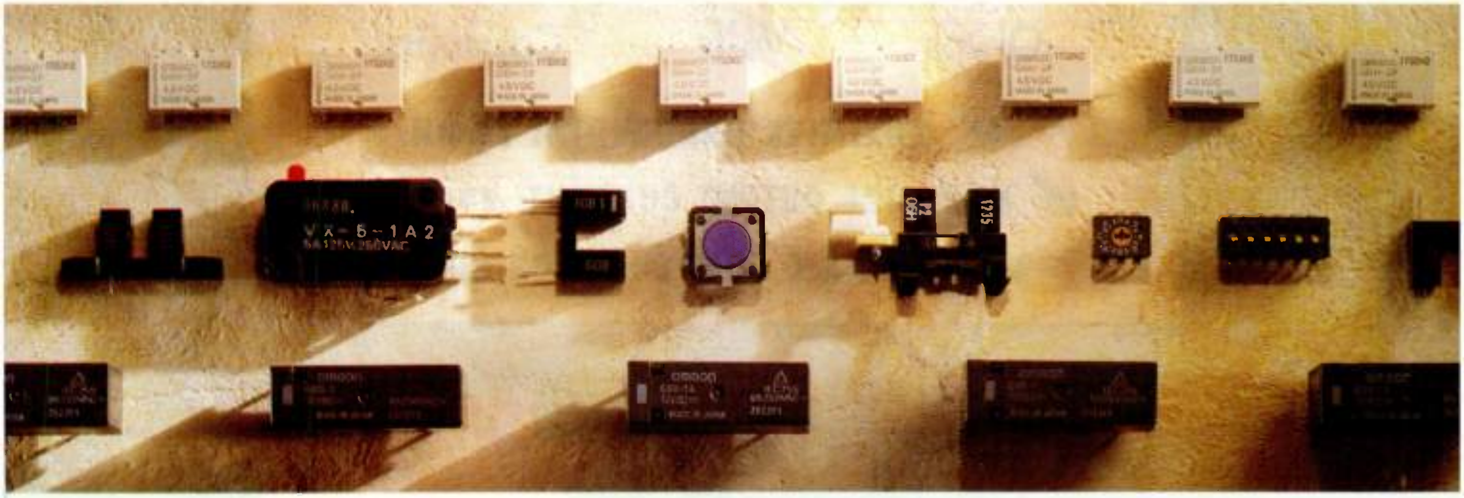

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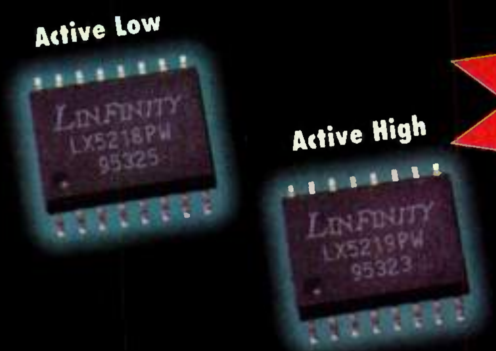

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Programmable Digital Televisions Expected For Next Year

Philips Semiconductor, Sunnyvale, Calif., announced the organization of a Digital Television (DTV) group that will begin immediate development of a programmable DTV. The group will be located at the Sunnyvale facility and is expected to produce DTV-enabled televisions that are fully compatible with the Advanced Television Systems Committee (ATSC) standards. At the core of the programmable DTVs will be the company's high performance TriMedia multimedia processor. This technology offers a number of advantages, including the computational power and flexibility needed to process the broad range of display formats specified in the ATSC standard.

The processor also can provide a wide range of additional services based on the ATSC standard, thanks to its programmable nature. In addition, it supports a reverse communications link for interactive services via the Internet and other media, can decode video to support video-on-demand services over cable-TV connections, and supports built-in video telephony and computer-based applications such as video games. One of its most significant advantages, though, is that as standards change and new services become available, the appropriate software needs simply to be downloaded into the TriMedia-based DTV. This positions the technology well for continued use well into the future.

The DTV sets initially developed by the DTV group will support existing National Television Standards Committee (NTSC) broadcasts and new DTV signals. Sets are expected to become available by the end of 1998. As part of this development effort, the company also is working closely with Philips Sound and Vision and other industry leaders to establish open standards for all of the new services made possible by the DTV environment. To receive additional information on the DTV development effort, contact the company at (408) 991 2000. CA

Computer Telephony Group Seeks Open DSP Interface

Seven computer-telephony companies have come together as a consortium with the intent to develop a new value-adding interface for computer telephony that will separate DSP software issues from the underlying hardware. The specification, to be called the Media Stream Processor (MSP), will allow companies to choose between develop MSP-compliant software or media processing software without having to do both.

The computer telephony industry, which is a heavy user of DSP technology, is by definition an integration industry. It has apparently reached that critical level of maturity where the effort spent dealing with the idiosyncrasies of different hardware platforms is robbing an unacceptable amount of resources from the actual application development. In addition, users want different vendors' software solutions to play on different hardware platforms and vice-versa.

One member of the consortium, BICOM, Monroe, Conn., is developing an optional MSP daughterboard interface. An MSP daughterboard would decouple the development of public network interfaces from the DSP resource board. This would allow hardware vendors to work on innovations in their board-level products while application vendors develop their code without worrying about the effects of hardware changes. At the same time, those developing telephony interfaces can face the daunting international approval process without having to involve the hardware and application people.

The consortium includes: BICOM, Calibre Industries (Diamond Bar, Calif.), Centigram Communications (San Jose, Calif.), Cole Technical Services (York, Pa.), Commetrex (Norcross, Ga.), and Pika Technologies and QNX Software (both of Kanata, Ont., Canada).

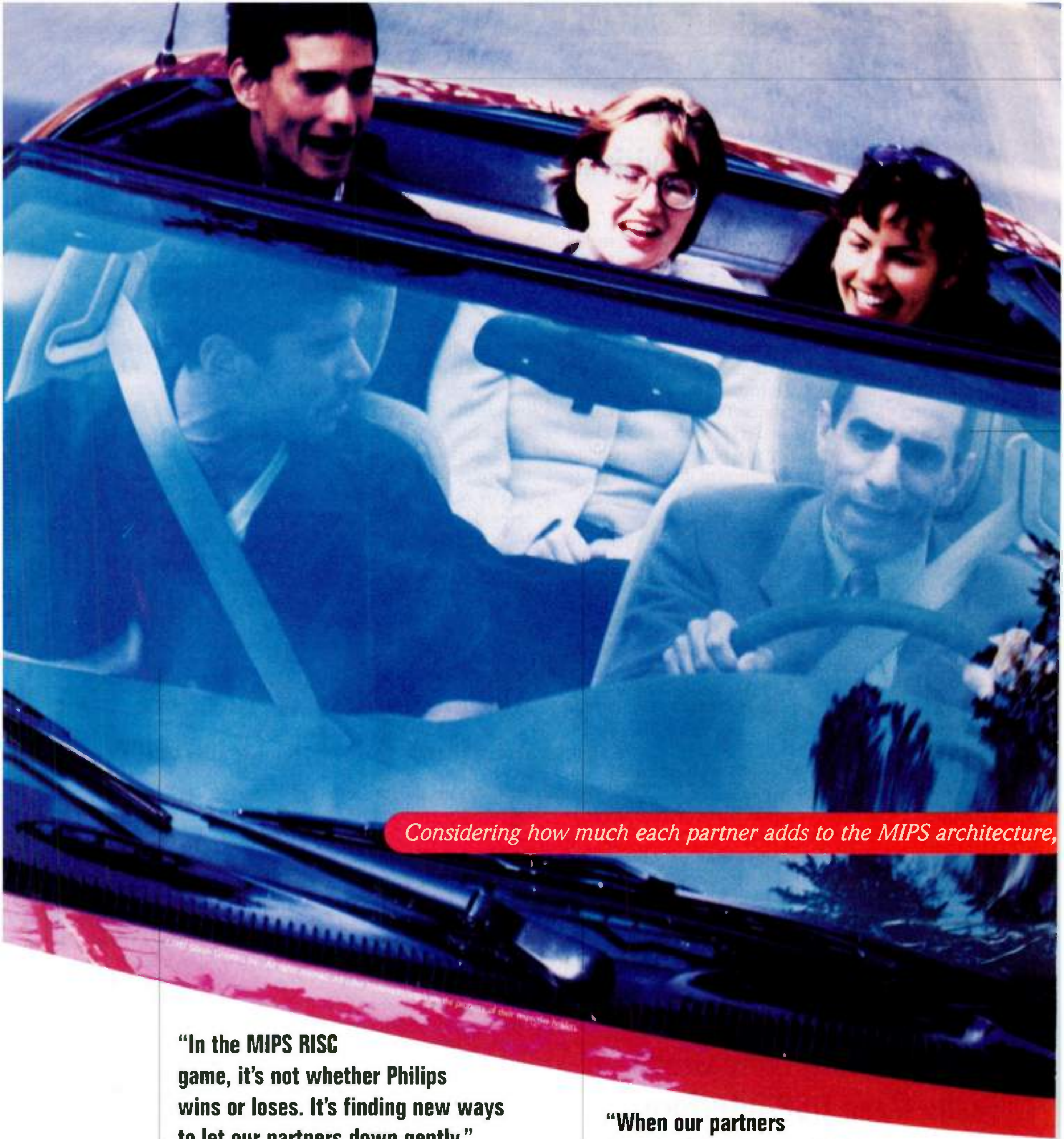
For information, contact Comtrex's Martin Lippman at (770) 242-7775, ext. 370; e-mail: *mlippmann@comtrex.com.* TW

Alliance Targets Verification Solutions For Next Generation

The migration toward a true systems on chip (SOC) design environment brings with it a whole host of challenges. These include issues of increased capacity and complexity, which literally push current verification methodologies to their limits. Complicate the picture by incorporating an embedded processor core into an ASIC design and the interface issues between the design's hardware and software turn into costly risks that if not caught before going to fab could be lethal.

Focusing on this issue, Mentor Graphics, Wilsonville, Ore., has formed an alliance—Seamless Alliance 2000—with ASIC suppliers to provide the tools that will be needed to create next-generation designs. The deliverables of this alliance are specifically intended to reduce the hardware/software co-verification risk and directly address today's most critical issues in electronic product development.

This open alliance partners Mentor with a number of leading embedded microprocessor suppliers, including ARM, Hitachi, Matsushita, Mitsubishi, Motorola, NEC, SGS-Thomson, and Toshiba. Under the guidelines of the program, Mentor and its partners will deliver hardware/software co-verification capabilities to both hardware and software design engineers working on next-generation embedded systems for various applications (e.g., telecom, datacom, and multimedia). They also will provide Seamless CVE customized Processor Support Packages (PSPs) for selected embedded microprocessor cores.



"In the MIPS RISC game, it's not whether Philips wins or loses. It's finding new ways to let our partners down gently."

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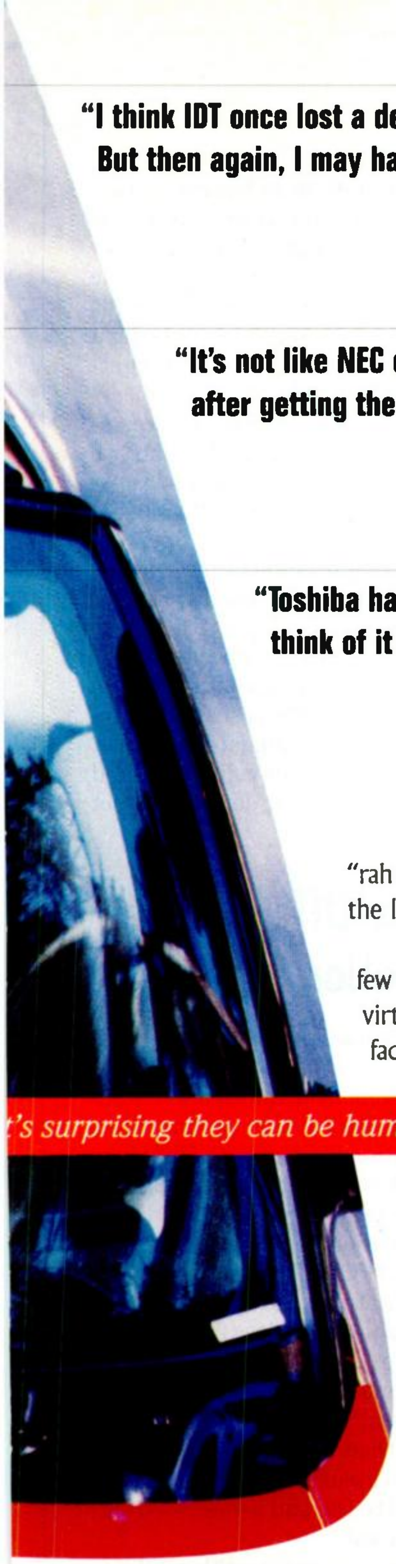

"I think IDT once lost a design win to one of our partners. But then again, I may have just imagined it."

"It's not like NEC calls our MIPS partners to say, WE WON, WE WON after getting the design win. Okay, so we did it once."

"Toshiba has never actually lost a design win. We prefer to think of it more as sharing with our other MIPS partners."

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Now, it would have been nice to have each of the MIPS partners say a few words about their individual strengths. But frankly, each partner has their own virtues and just way too many strong points to mention in one ad. (That, and the fact that they couldn't agree on who would go first.) So to simplify matters, just remember this: each partner is turning out incredible versions of this open, scalable architecture. Which means the partner you select will give you the perfect embedded processor for your design. You can also expect the broadest range of industry leading tools. So your idea gets to market faster. And it gets there for less than those conventional embedded processors.

If you'd like to see the online version of this heartfelt corporate harmony, visit www.TeamMIPS.com.

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In the first step in the program, the partners will send engineers to receive on-site technical training on Seamless CVE from Mentor's Co-design Business Unit. Then they will use this information, coupled with their expertise in embedded cores, to create highly integrated environments for fast execution of embedded software on a virtual prototype of the ASIC. Each PSP will be validated by both Mentor and the partnering vendor to assure a deliverable that offers a high level of performance, accuracy, functionality, and debug capability. As a result, end users of the PSPs can expect a co-verification environment that will enable them to identify and fix design errors in the hardware/software interface before committing to silicon. For further information on the Seamless Alliance 2000, contact Mentor Graphics at (503) 221-1551; *http://www.mentorg.com.* CA

Specification Defines Small Embedded-Board Form Factor

Aimed at the embedded single-board-computer (SBC) market, the EBX form factor is a multivendor standard for non-backplane SBCs. EBX, which stands for "Embedded Board, eXpandable," was co-developed by Ampro Computers Inc., San Jose, Calif., and the Motorola Computer Group, Tempe, Ariz.. The purpose of the standard is to ensure that embedded computing solutions can be designed into space-constrained environments with off-the-shelf components.

The specification offers a standard mechanical design for deeply embedded applications that require a high level of CPU performance and integration, but can't afford the size, cost, or complexity associated with backplanes or card cages. EBX merges the expansion capability of the PC/104+ onto a board measuring just 5.75 by 8 in. A PC Card interface also can be employed. The specification defines the board dimensions and the mounting-hole patterns, including the location for the PC/104+ expansion and recommended zones for the PC Card interface and other common I/O.

The EBX specification is available without licenses or royalties. It can be downloaded from the Internet at *http://www.ampro.com* or *http://www.mot.com/computer.* For more information, contact Ampro at (800) 966 5200 or (408) 360-0200, or Motorola at (800) 759-1107 or (512) 434-1526. RN

Display Technology Eyed As LCD Replacement

Although liquid crystal displays (LCDs) have long dominated the display market, existing limitations in the technology have left the door open for future replacements. One such replacement is the three-color, tunable, vertically stacked organic light-emitting diode (SOLED), which debuted in July from Universal Display Corp. (UDC), Bala Cynwyd, Pa. The company has now taken its development one step further by demonstrating the existence of a transparent, flexible organic light-emitting diode (T-FOLED). This technology holds particular significance because in addition to it being a full color flat-panel-display technology, it's ultra-lightweight, transparent, and conformable.

Taking part in this ongoing development are researchers from Princeton University. Together, the two have shown that it's possible to combine the transparency and flexibility of organic displays into one device. As such, the technology is expected to open the doors to a host of previously infeasible or impractical applications such as conformable, full-color displays for windshields and high-contrast displays attached to curved instrument panels. Moreover, with the demonstrated brightness, energy efficiency, robust nature, and cost effectiveness of the OLEDs, researchers believe that it's a prime replacement candidate for LCDs. Subsequently, UDC its continuing development and commercialization efforts. For further details, contact UDC at (610) 617-4010. CA

Standard Update Offers More Efficient Information Exchange

The Silicon Integration Initiative Inc. (SI2), Austin, Texas, has recently released the an update, version 3.1, to the Pinnacles Component Information Standard (PCIS). Developed as part of the ongoing Electronic Component Information Exchange (ECIX) program, the primary reason for the update was to include the SGML Open Exchange Table Model for a more efficient interchange of information. Also, improvements were made to tags to extend PCIS flexibility.

The ECIX project is dedicated to the development of an architecture that will enable a seamless flow of information from authors, designers, manufacturers, and other creators of component information to the end-customers of that information. Such an architecture will include standards and methodologies, as well as any support software needed to assure that component information will be delivered to the end users electronically and in an agreeable format.

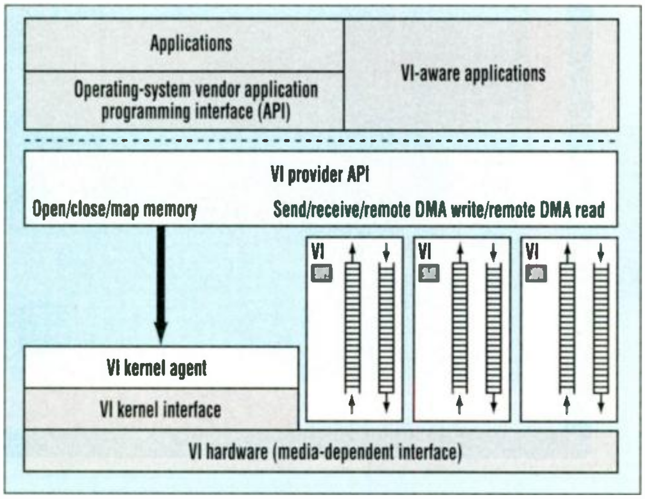
The standard was originally developed through cooperation from five leading electronic component manufacturers: Hitachi, Intel, Philips Semiconductors, National Semiconductor, and Texas Instruments. Continuing work on the standard has brought additional support from Hewlett-Packard, IBM Microelectronics, and DARPA to help expand the PCIS standard and provide an open ECIX architecture. For information on the ECIX project or the standard update, contact SI2 at (512) 342-2244, or visit the ECIX project web site at *http://www.si2.org.* CA

Edited by Roger Engelke

Inter-System Communications Standard To Ease Clustered System Implementation

Although its definition has not been finalized, the virtual-interface architecture (VIA) promises to provide mechanisms for low-latency, high-bandwidth message passing between interconnected nodes and interconnected storage devices (clusters). The VIA specification for clustered systems is being jointly defined by Compaq Computer Corp., Houston, Texas, Intel Corp., Santa Clara, Calif., and Microsoft Corp., Redmond, Wash. It's intended to accelerate the development and reduce the cost of clustered servers, workstations, and I/O devices. Cluster computing is defined as short-distance, high-performance interprocess communications (IPCs) between multiple building blocks. These building blocks comprise servers and/or workstations, as well as I/O subsystems connected directly to the network.

Interconnecting servers, workstations, and I/O devices to form a scaleable computing cluster presents a unique set of communications requirements. Most of those requirements have not been addressed by existing local and wide-area network standards. LANs and WANs typically sacrifice latency for robustness, generality (the ability to handle multiple configurations), and distance—just the opposite of what devices in a cluster would need. Distance and generality in a cluster can usually be sacrificed to reduce latency down to a minimum, as long as reliable and ordered delivery of messages is guaranteed. Such a guarantee is an element of the VIA specification.



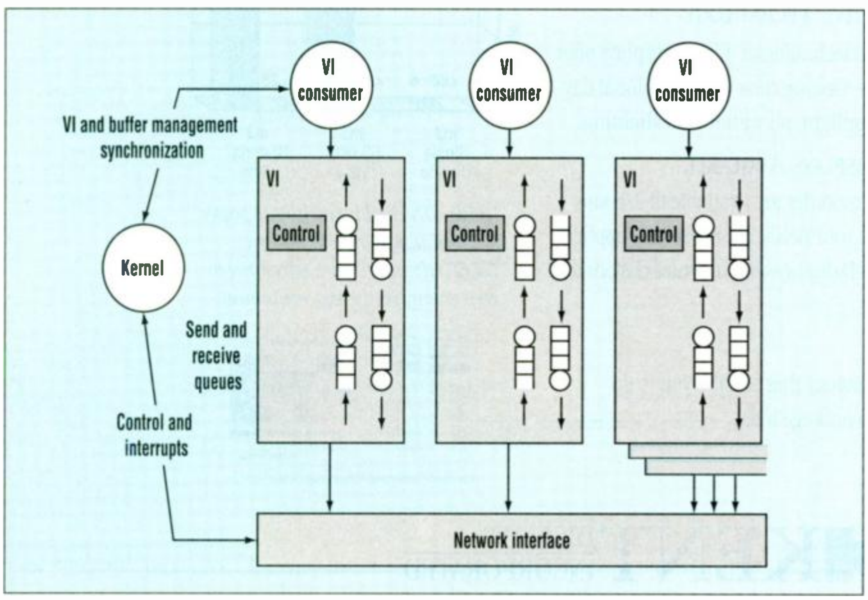
2. In the communications stack, the virtual-interface (VI) provider supplies a low-level interface to the VI consumer. Operating-system and independent software vendors can build higher-level application programming interfaces (APIs) and services to present a higher-level abstraction to the application.

Clusters can be assembled at a fraction of the price of a mainframe, while delivering higher performance and better reliability. To make clustering a reality, there are two key ingredients that are needed: cluster support embedded in shrink-wrapped operating systems, and standards for low-latency cluster communications.

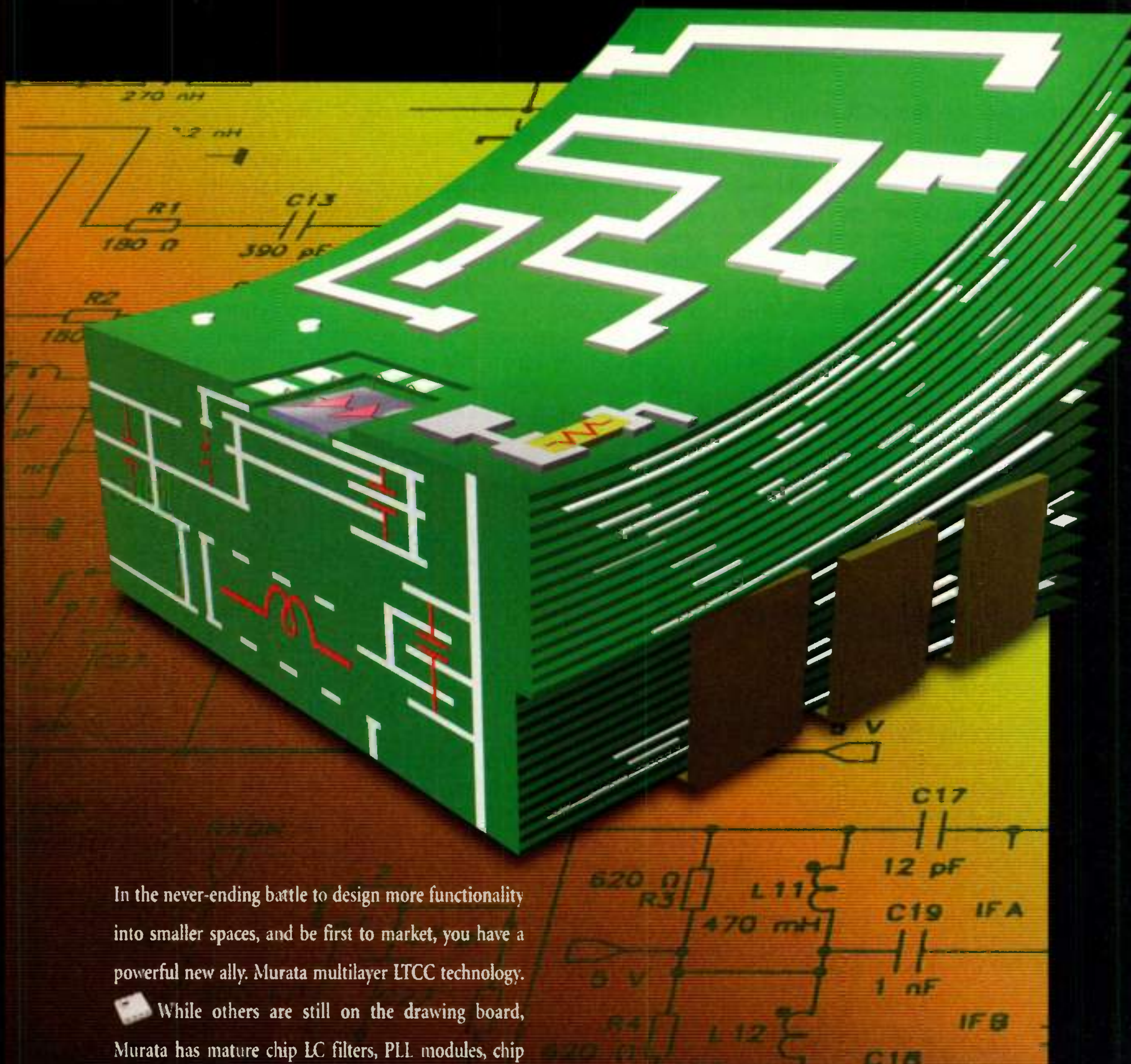
The VIA specification defines a low-level application programming interface (API) and a network interface controller (NIC) with low-overhead communication by using zero-copy semantics. The basic concept provides the illusion of a network interface dedicated to multiple applications simultaneously; e.g. a "virtualized" interface. The VIA model is based on a simple queuing model whose correctness principles are well understood and for which performance can be predicted. The model also provides fully-protected, direct user-level access to the network interface exported through the virtual memory subsystem *(Fig. 1)*.

Included in the VIA functional definition are the following elements: packet descriptors, send-work and receive-work queues, "doorbells," asynchronous status notification, and memory registration. The receive and send packet descriptors describe the scatter/gather operation that will be performed during reception or transmission of the packet. The doorbells are used to notify the network interface that work has been placed on a work queue. The memory registration registers regions of memory with the NIC before they're used in communication.

The architecture allows a VI consumer access to the network interface directly, without operating-system intervention. That access takes place through a pair of send and receive



1. The virtual-interface (VI) architecture, as defined by Compaq Computer, Intel, and Microsoft, allows a VI consumer direct access to the network interface without operating-system intervention. A pair of send and receive cues provide the access.



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work queues referred to as a VI instance. To offer this capability, a process cannot be allowed to interfere with any other process or the kernel that is sharing the network interface. This protection is achieved using the normal page protection mechanisms of the virtual-memory subsystem.

A process can own many VI instances, and in the context of a VI instance, the kernel can be viewed as a process since it has a distinct virtual address space. The direct access to the network interface is only the first step in establishing communications between cooperating processes running on separate servers. The next step is to provide a VI consumer with the illusion of a dedicated, fully-interconnected network infrastructure.

The VIA supports both reliable and unreliable network media. This support allows the proper cost/performance trade-offs to be made and the optimum capability to be chosen for a given application. Reliable networks guarantee that data is received in the order that it was sent. No duplicate packets are received, and all unrecoverable hardware errors are reported to the VI consumer. Reliable network semantics implemented with hardware relieve the communication stack of the burden of implementing reliability in software. Unreliable networks allow the reliability semantics to be implemented in software, and have higher overheads.

The VI provider supplies a low-level interface to the VI consumer. Operating-system vendors will be able to build higher-level APIs and services to present a higher-level abstraction to the application *(Fig. 2)*. Performance-critical applications will use the VI provider directly, while other applications will use services provided by operating-system vendors.

The standardized programmatic software interface of the VIA provides portability between computing platforms and network implementations. The VI provider API contains functions that can be categorized into two major groups: control, and data movement and synchronization. Control functions include opening and closing the NIC, creating or destroying a VI instance or completion queue, connecting or disconnecting a VI endpoint, registering or deregistering a memory region for communication use, and registering a user-defined asynchronous error handler. The data operations include posting a send or remote DMA operation, posting a receive buffer, polling a VI endpoint for completion, waiting on a VI endpoint for completion, polling a completion queue, and waiting on a completion queue.

As part of the API, the VI kernel agent provides functions that require several privileged operations: interrupt processing and synchronization, and registration of buffers. For the interrupt processing and synchronization, the kernel agent synchronizes by supplying the scheduling semantics for blocking calls. As a privileged entity, it controls the hardware interrupts from the VIA on a global and per VI-instance basis.

The kernel agent supports buffer registration and de-registration when the buffers are registered. Enforcement of protection across process boundaries by page ownership is allowed. Privileged kernel processing is required to perform virtual-to-physical address translation and to wire the associated pages into memory.

The VIA specification is currently still in the definition phase and will not be publicly available until the definition is complete. However, requests for information regarding the status of the specification can be sent to *wire@co.intel.com*, while copies of the VIA presentation delivered at this past summer's IEEE Hot Interconnects Conference at Stanford University can be requested from *victoria_j_frazier@ccm.co.intel.com*.

Dave Bursky

Intelligent Device-To-Device Communications Scheme Lets Subsystems Form Seamless Links To Each Other

A protocol for device-to-device communications that can be embedded as firmware into peripherals, and as a software module in PCs, promises to eliminate incompatibility issues when connecting the devices together. Developed by the Hewlett-Packard (HP) Co. Ltd., Bristol, U.K., the JetSend intelligent protocol is an open technology available to appliance manufacturers and software developers who wish to incorporate the scheme into their products. Copies of the specification are available free of charge from the company's JetSend web site at *http://www.jetsend.hp.com*. An appliance development kit also is being made available.

The JetSend technology allows two devices to interconnect, negotiate data types, provide status updates about device operation, and exchange information—all without user intervention. Any information appliance, computer peripheral, or computer system can incorporate the protocol. The protocol provides easy communication across many devices, solving many of the hassles commonly associated with ad hoc, distributed, and mobile communications between historically incompatible devices, according to Paul Burwood, the marketing manger for HP workgroup printers *(see the figure)*.

For example, two JetSend-enabled devices—say a printer and a scanner—could be interconnected. They would exchange operational data to "negotiate" with each other to establish a link. For instance, the scanner would send information about its capabilities: "I am a JetSend device and I can send you images in grayscale or color with up to 24 bits of color depth and in resolutions from 150 to 1200 dots/in." The printer would receive that information and could respond with: "I am a JetSend device; send me 24-bit color at 600 dpi." The scanner would then respond with the image file.

Negotiation

Every exchange potentially involves negotiation of the encoding it-

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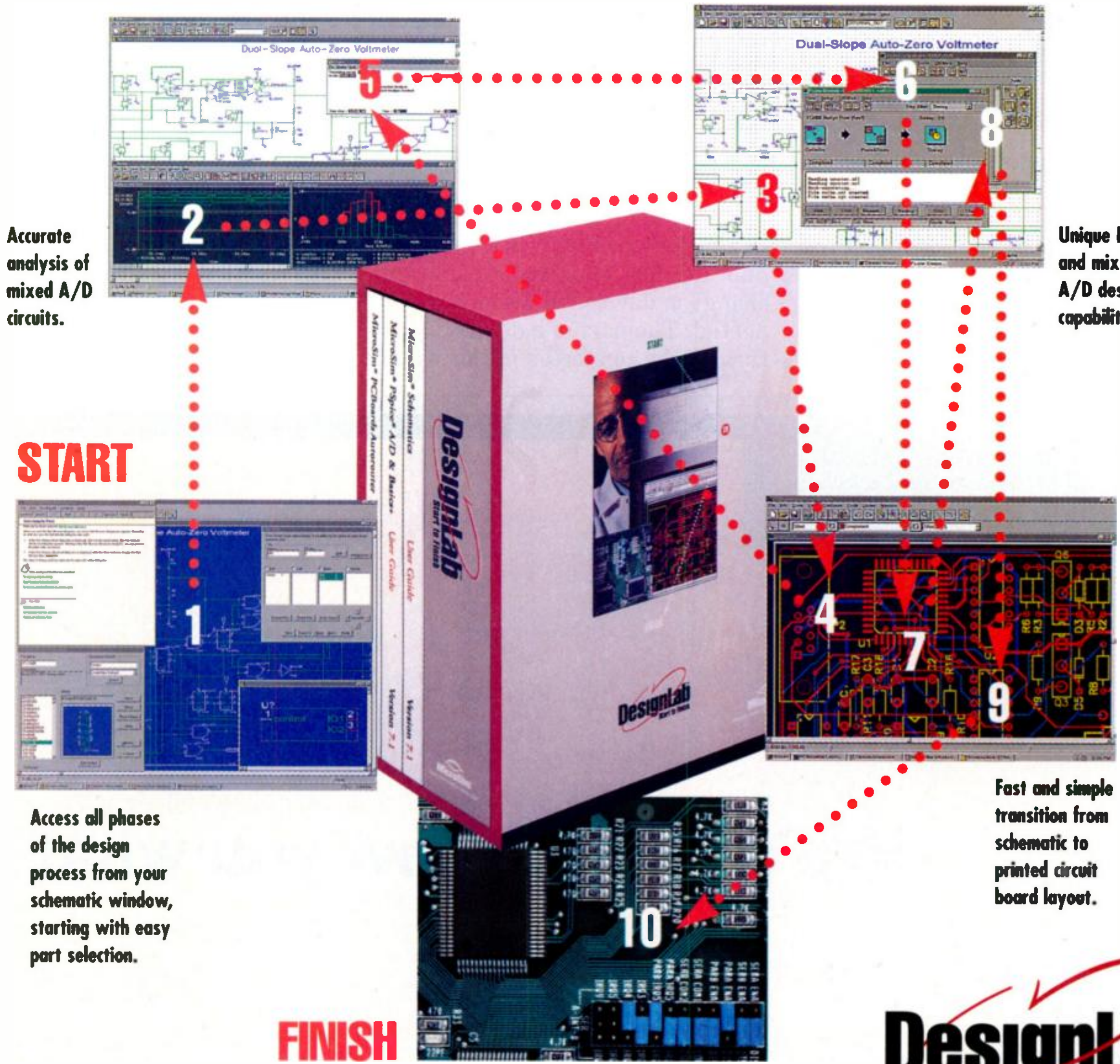

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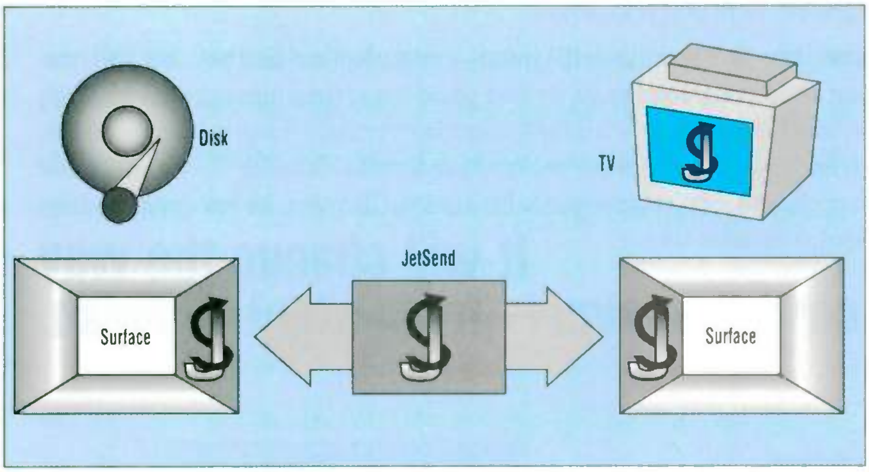

Each information appliance interconnected using the JetSend intelligent protocol has an interface called a surface. Information on surfaces is moved from one device to another after the JetSend protocol negotiates the linkage.

self, the parameters of the chosen encoding, and how the information is to be transferred. The negotiation between the peripherals takes place automatically. If two devices can connect, they can exchange meaningful data, minus drivers, without a lot of intermediary networking complexity, and most importantly, without user intervention.

In JetSend, communications between devices involves a change in one device causing equivalent change in devices to which it is connected. The part of a device's state that can be connected in this way is called its surface. Since JetSend communication takes place entirely via surfaces, the protocol is called a surface-interaction protocol. In such a protocol, surface connection is separate from change propagation; surface connections can be one-to-many, creating a single "virtual surface" shared by all connected devices. When a change takes place on one surface, that change will propagate automatically to all connected surfaces, in effect, maintaining system equilibrium.

Synchronizing Surfaces

JetSend works by synchronizing the surfaces of connected devices. For this to happen, the device surfaces must contain the same type of information that must consist of things that can be rendered perceptible to people (visible, audible, or tangible). The protocol also distinguishes what is transmitted between devices from how it is encoded, thus permitting the scheme to operate over different hardware interconnection approaches. The protocol will work with both fixed-function and programmable devices, governing only how the devices interact, not what they do.

The first type of JetSend device covers anything that captures, stores, computes, or renders user-perceptible information (printers, scanners, storage devices, televisions, network appliances, etc.). The surface of a device is divided into subsurfaces, each containing a unique identifier. Devices that generate electronic material, such as scanners, have a default subsurface called "Out," while consumers such as printers, have a subsurface referred to as "In." JetSend device surface identifiers map to URLs when the device is connected to the Internet. By default, a sending device, such as a scanner, connects to a target device's In surface, but could be directed to connect to a different target subsurface. Similarly, a receiving device would, by default, connect to a source device's Out surface, but can be directed by the user to connect to a different source's subsurface.

A JetSend-enabled computer would have both In and Out surfaces. As a result, the default location to "put" new images or documents to be sent to a PC is the PC's JetSend In surface, which can be mapped to the PC's universal in-box. For outbound images or documents, the data is initially positioned on the Out surface. However, a PC or other devices can have JetSend surfaces with arbitrary identifiers; other devices can only connect to those surfaces of which they are aware. They check a surface address list for a match, and that list can be interrogated and downloaded through normal surface interaction.

A Universal Driver

As part of JetSend, there will be a universal driver for Microsoft Windows, thus enabling applications to send information directly to JetSend devices, or to generate information that can be saved for later exchange. That effectively turns the PC and any host application with a "print" or "send" function into a simple JetSend sending appliance.

Existing peripherals can be converted into JetSend appliances by using JetSend surrogates on supporting host computers, or via dedicated device adapters. When on the host, these surrogates are referred to as "soft appliances" that could be used to get the surfaces to communicate across the Web or other communication interfaces.

A JetSend protocol appliance development kit, the JetSend ADK, includes HP's own implementation of the JetSend protocol, the electronic material specification (data-format specification, and libraries, code samples, reference implementations, middleware, and documentation.) The ADK is available for a license fee of $15,000 and can be used royalty-free. The license fee also includes the use of the JetSend brand name and logo, as well as access to a certification test suite.

Dave Bursky

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- **T1 FDL Hardware Support:** The DS2152 has a full HDLC controller with 16-byte buffers along with a complete Bit-Oriented Code (BOC) controller, allowing the host a full second of processing latency. Even the most heavily loaded host will have time to handle the real-time needs of the FDL.

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Gas-Gauge IC Performs Precise Battery Measurements

This Tiny Chip Improves Battery Management While Reducing Battery Subsystem Size And Cost.

Richard Nass

You know the gauge isn't accurate, but you trust it anyway. You've been burned time and time again, but that doesn't stop you. Even though the battery indicator on your laptop computer or cellular phone shows two of four bars on the battery gauge (50% full), it just can't be. Sure enough, while you're writing that important proposal or making that pivotal call, the device goes south.

The gauges on today's electronics can be very misleading. Often, when the batteries are new, the gauge is accurate. But as the batteries wear, the electronics associated with the gauge don't compensate for that wear. Hence, you're left with a piece of electronics that needs recharging before the indicator says so.

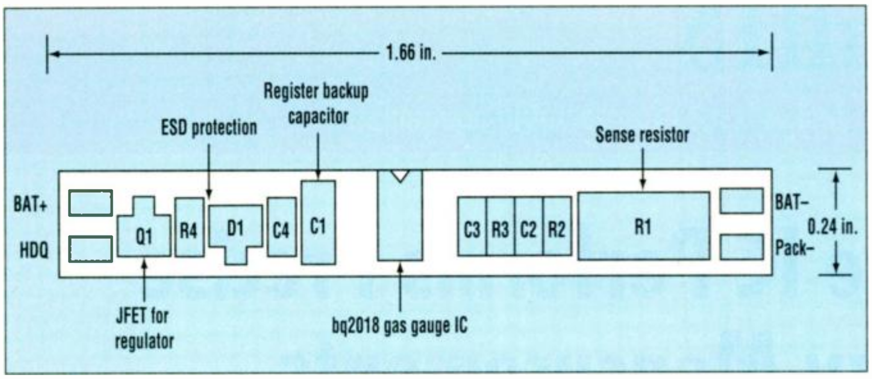
To solve this problem, the designers at Benchmarq Microelectronics Inc., developed the bq2018 Multifunction Charge/Discharge Counter that works with an intelligent host controller. The low-cost chip is housed in a tiny package, an 8-pin, 150-mil SOIC, that allows for easy integration into a battery pack. In fact, the part is small enough to fit in the space between two A-size cells. In an implementation, the part is typically housed on a ready-to-go module, which measures 1.66 by 0.24 in. In addition to the bq2018 gas-gauge IC, the module holds a sense resistor, a capacitor for register backup, a JFET for the regulator, ESD protection, and a few other resistors and capacitors *(Fig. 1)*.

Self Calibrating Chip

The chip self-calibrates and provides state-of-charge information for any type of nickel- or lithium-based rechargeable battery. The bq2018 lets the host controller precisely indicate battery available capacity in friendly, easy-to-understand terms of standby or operating time. For example, a cellular phone with a Li-Ion battery could indicate that the phone can operate for 7 hours and 45 minutes in standby mode or 1 hour and 15 minutes in talk mode.

The bq2018 estimates self-discharge using an internal time base and temperature sensor. The low-power chip operates at less than 80 µA, with a data-retention current of under 50 nA. The part also contains 128 bytes of non-volatile RAM (NVRAM), including 115 bytes of user RAM that can store battery characteristics and chemistry type; charge data; or ID information, including the serial number and manufacturing date *(Fig. 2)*. This eliminates the need for a separate battery ID chip, reducing overall system cost. The remaining 13 bytes contain the capacity-monitoring and status information.

The bq2018 measures the voltage drop across a low-value series sense resistor between the negative terminals of the battery and the battery-pack ground contact. By using the accumulated counts in the charge, discharge, and self-discharge registers, an intelligent host controller can determine battery state-of-charge information. To improve accuracy, an offset count register is available. The system host controller is responsible



1. The bq2018 Multifunction Charge/Discharge Counter, developed by Benchmarq Microelectronics, offers precise measurements for battery charging and discharging. Housed in a tiny, 8-pin, 150-mil SOIC, the chip can be mounted on a board containing all the electronics needed for operation.

for the register maintenance by resetting the charge input and output and the self-discharge registers as needed.

The chip's register backup input (RBI) operates from an external power-storage source, such as a capacitor or a series cell in the battery pack. This technology provides register nonvolatility for periods when the battery is shorted to ground, or when the battery charge state is not sufficient to operate the bq2018. For this situation to occur, the register backup current must be less than 100 nA. Because the bq2018 outputs V_{CC} on the RBI when the voltage level is above 2.8 V, a diode is needed for isolation.

The bq2018 requires an external host system to perform the maintenance on its three registers. Using information from the chip, the host can determine the battery's state of charge, estimate the self discharge, and calculate the average charge and discharge currents. During storage periods, the internal temperature sensor doubles the self-discharge count rate for every 10° above 25°C.

To reduce system cost, power to the monitoring chip can come from an inexpensive external FET, which is tied to the regulator output (REG) pin. The REG is the output of the operational transconductance amplifier that drives an external-pass n-channel JFET to supply an optionally regulated supply. The nominal value of the supply is regulated at 3.7 V.

When the chip's data input/output (HDQ) line remains low for more than 10 seconds and the V_{SRO} is below the programmed minimum level, the chip enters its sleep mode, where all operations are suspended. The sleep mode requires less than 10 µA. A high transition of the HDQ reinitiates the chip. The V_{SRO} is defined as the offset voltage plus the voltage drop between the two current-sense inputs.

A register is available to store the calculated offset, allowing for current calibration. The offset-cancellation register is written by the bq2018 during battery-pack assembly, but is available to the host in case any adjustments are needed later. By adding to or subtracting from the offset value that's stored in the offset register (OFR), the true charge and discharge counts can be accurately calculated.

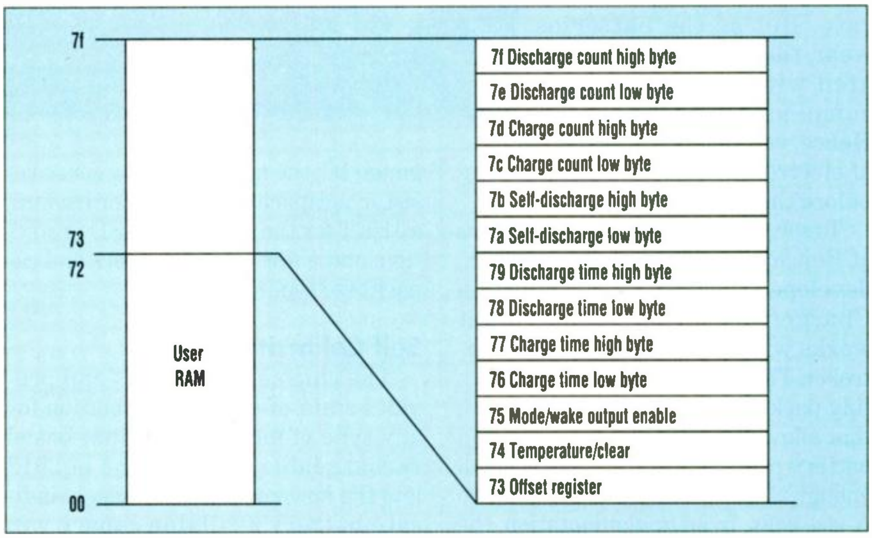
Nickel Or Lithium Batteries

The bq2018 can operate directly from three or four cells based on a nickel chemistry or one lithium-ion cell, as long as the supply-voltage input (V_{CC}) is between 2.8 and 5.5 V. The REG output helps facilitate the power-supply requirements using an external low-threshold n-JFET. A micropower V_{CC} source can be built using this FET *(Fig. 3)*.

The IC accumulates charge and discharge counts into two main count registers, the charge-count register (CCR) and the discharge count register (DCR). The counts are produced by sensing the voltage difference across a low-value resistor between the negative terminals of the battery pack and the battery.

During discharge, the DCR and discharge-time counter (DTC) are active. If V_{SR1} is less than V_{SR2} (the voltage at the two current-sense inputs), there is a discharge. As a result, the DCR counts at a rate of 12.5 µV/hour and the DTC counts at a rate of 1 count/0.8789 seconds. Conversely, during a charge operation, the CCR and charge-time counter (CTC) are active. Here, V_{SR1} is greater than V_{SR2}, causing the CCR to count at the 12.5-µV/hour rate, and the CTC to operate at 1 count/0.8789 seconds.

When the HDQ pin is high and the signal between the current-sense inputs is above the wakeup-output-enable (WOE) threshold, the bq2018 is in its full operating state. That means that the DCR, CCR, DTC, CTC, and self-discharge count register (SCR) are fully operational. In addition, the Wake



2. The bq2018 contains 128 bytes of NVRAM. Battery characteristics and chemistry type, charge data, or ID information can be stored in the lower 115 bytes, while the remaining 13 bytes contain the capacity-monitoring and status information.

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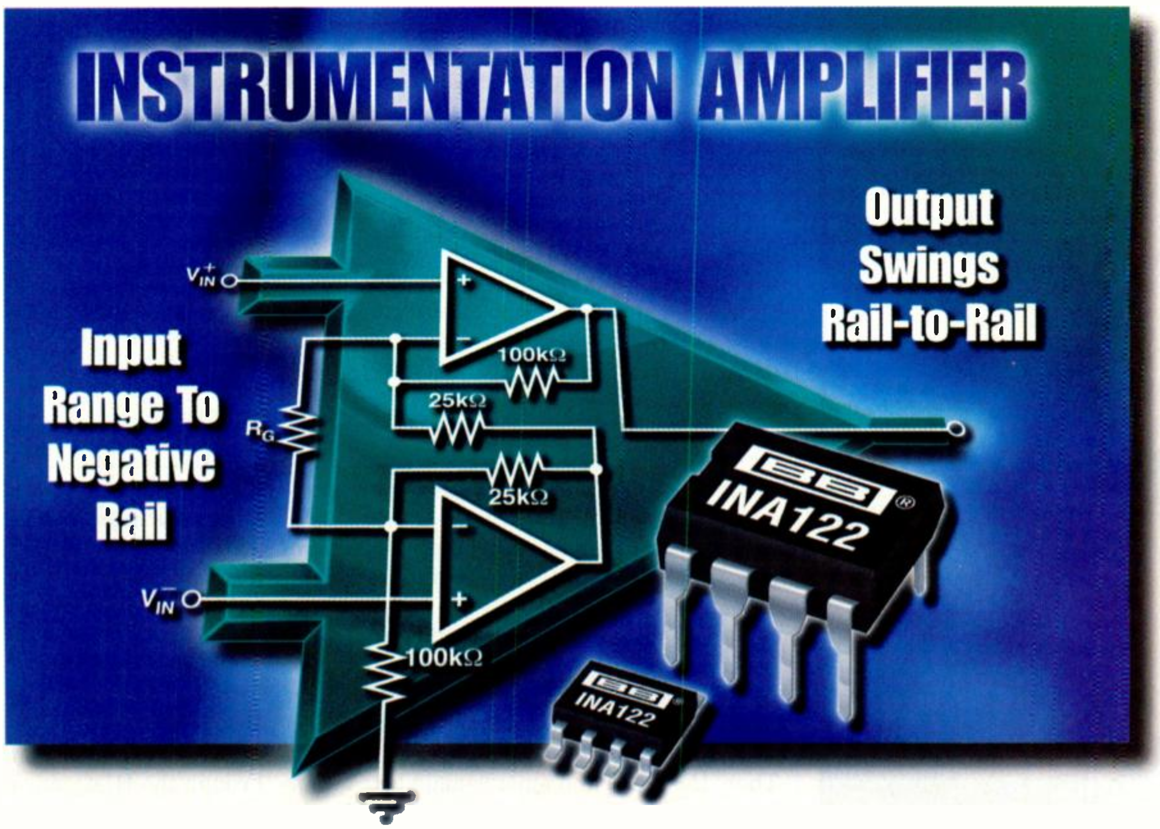

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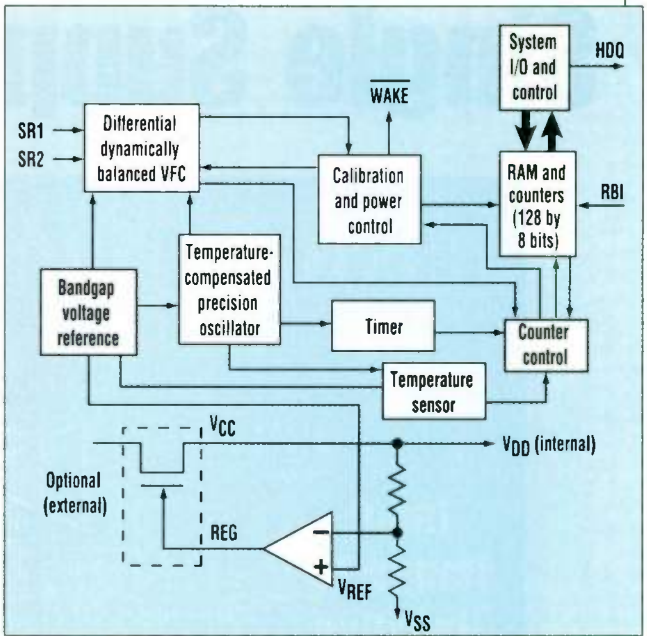
output is low. The Wake output indicates that the charge or discharge activity is above a preprogrammed minimal level. In the full operating state, the internal RAM registers can be accessed.

The gas-gauge IC enters a sleep state if the signal between the current-sense inputs is below the WOE threshold, and the HDQ remains low for longer than 10 seconds. Then, all register counting is suspended. The part stays in this mode until the HDQ returns high.



3. The gas-gauge IC operates from a supply-voltage input (V_{CC}) ranging from 2.8 to 5.5 V. The REG output helps facilitate the power-supply requirements using an external low-threshold n-JFET. This FET also is useful if a micropower V_{CC} source is desired.

The bq2018 can be programmed to measure the voltage offset between the current-sense inputs during pack assembly or at any later time by invoking the calibration mode. This mode is enabled by setting the calibration bit in the Mode-WOE register to 1. Then, the HDQ line must remain low for more than 10 seconds, and the signal between the current-sense inputs must be below the WOE threshold.

Monitors Temperature, Too

An internal temperature sensor sets the value in the temperature register, as well as the self-discharge count-rate value. The register reports the temperature in eight steps of 10°C, from 0°C to 60°C. There's also one value each reserved for a temperature that's either below 0°C or above 60°C. The sensor has a typical accuracy of ±2°C at 25°C.

Communications to the bq2018 are accomplished using a serial interface. It's through this same interface that the host processor can access the chip's registers. A command-based protocol is employed for communications, where the host sends a command byte to the bq2018. The employed protocol is asynchronous return-to-one. Command and data bytes consist of an 8-bit stream with the least-significant bit transmitted first. The maximum transmission rate is 5 kbits/s.

The command protocol can be implemented by the host processor using either polled or interrupt processing. A UART also can be used for communications through the HDQ pin. The communications command can be one of two options—telling the monitor chip to store the succeeding 8 data bits received in a register specified by the command byte or output the 8 bits from a specified register.

The return-to-one data-bit frame contains three elements. The first part starts the transmission (either by the host or the bq2018) by taking the HDQ pin low. The second part is the actual data transmission. The final section stops the transmission by returning the HDQ pin to a high state.

Price And Availability

The bq2018 multifunction charge and discharge controller is available now. For lots of 10,000, the part sells for about $1.75 each. Discounts are available for higher volumes.

Benchmarq Microelectronics Inc., 17919 Waterview Pkwy., Dallas, TX 75252; (972) 437-9195; Internet: http://www.benchmarq.com.

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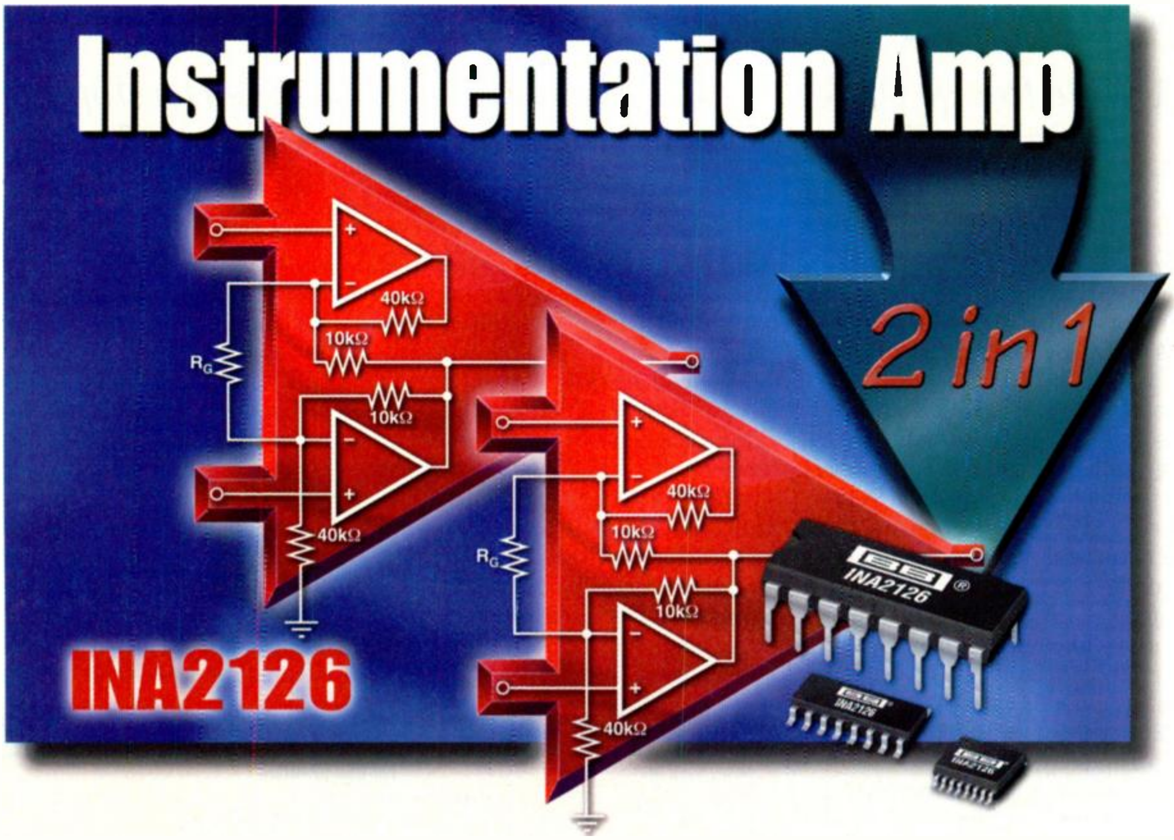

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INA2126 dual precision instrumentation amplifier features excellent performance with very low quiescent current (175μA/channel). In addition, a wide operating voltage range of ±1.35 to ±18V makes INA2126 ideal for low cost portable instrumentation and data acquisition systems.

INA2126 gain can be set easily from 5V/V to 10,000V/V with a single external resistor. Laser trimmed input circuitry provides low offset voltage, low offset voltage drift, and excellent common-mode rejection. INA2126 is perfect for low-level signal acquisition including bridge sensors, RTDs, thermocouples and physiological signals.

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- Wide Supply Range..................................±1.35 to ±18V
- Low Offset Voltage ....250μV max
- Low Offset Drift ....3μV/°C max
- Low Noise...35nV/√Hz
- Gain Equation...$5 + 80k\Omega/R_G$

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Sensors Expo '97 Eyes The Latest In Products, Applications, And Technology

A Wide Range Of Technical Presentations Examine Developments In Sensor Testing, Networking, Packaging, And Interfacing.

Roger Allan

Some 300 exhibitors and a robust technical program highlight the Sensors Expo '97 Conference and Exposition, to be held Oct. 20-23 in Detroit, Mich. *(see "Want to go?" p. 46)*. The conference will examine the latest trends in sensor products, applications and technology. Over 5000 attendees are expected to view more than 50 new products and services and hear a wide range of tutorials and updates on sensor trends. Exhibit booths as well as the technical program will be held at Detroit's Cobo Convention Center, with exhibits open from 10:00 a.m. to 4:00 p.m., Tuesday and Wednesday (Oct. 21 and 22), and 10:00 a.m. to 3:00 p.m. on Thursday, Oct. 23.

As in the past, the conference's technical program is preceded by four all-day tutorials on Monday, Oct 20. The tutorials are courses that delve into the hows and whys of various sensor technologies and their applications *(see the conference program table)*.

Tutorial ADT1, "Digital data acquisition and analysis," is given by Strether Smith, an experienced lecturer and prolific author of experimental mechanics and computer-aided testing techniques. It examines the principles of data acquisition and analysis, including real-world application challenges. Included is an introductory level presentation on the topics of digitizing and sampling theories, signal-conditioning hardware, analog-to-digital converters (ADCs), computer interfaces, and data-analysis techniques.

Eric Udd, president of Blue Road Research, will lecture on "Fiber-optic sensor technology and trends" in Tutorial ADT2. This course will provide an overview of fiber-optic sensor technology and how it is now being used in a variety of industrial applications. It will cover recent developments in implementing high-performance fiber-optic strain sensors that offer unique capabilities.

Tutorial ADT3, "Capacitive and electric field sensors: Design and applications," covers the basics of capacitance sensing, including configurations, shielding, drift-compensation methods, multiple-electrode approaches, and fabrication methods. It will be presented by Darold Wobschall, a faculty-member of the Electrical and Computer Engineering Dept. at the State University of New York at Buffalo, and vice-president of technology at Sensor Plus Inc. The course also will discuss various signal-conditioning methods and applications.

Tutorial ADT4, "Transducer interfacing and signal conditioning fundamentals," will be given by Steve Guinta, central applications customer support group technical manager at Analog Devices. The course reviews the fundamentals of popular transducers like resistance temperature detectors (RTDs), strain gauges, photodiodes, and piezoelectric sensors. It also covers practical circuit techniques, in-

SENSORS EXPO TECHNICAL PROGRAM

Mon., Oct. 20 9:00 a.m.-5:30 p.m.	**All-day tutorials** **ADT1:** Digital data acquisition and analysis **ADT2:** Fiber-optic sensor technology and trends **ADT3:** Capacitive and electric field sensors: Design and applications **ADT4:** Transducer interfacing and signal-conditioning fundamentals
Tues., Oct. 21 9:00-10:30 a.m.	**Seminars** **S1:** Sensor packaging and test: What users need to know
10:45 a.m.-12:15 p.m.	**S2:** Ethernet: A cost-effective strategy for monitoring remote signals and sensors **S3:** Introduction to motion control
2:15-3:45 p.m.	**S4:** The growing role of solid-state magnetic sensors
9:00 a.m.-12:15 p.m.	**Half-day tutorials** **HDT1:** Automotive sensor technologies and applications **HDT2:** How to detect and measure vibration: A practical approach
2:15-5:30 p.m.	**HDT3:** Fundamentals of sensor technology I: Proximity and position **HDT4:** Heavy duty data acquisition: The how and why of VXI
9:00 a.m.-5:30 p.m.	**All-day tracks** **TRK1:** Smart sensors and smart sensor communication
Wed., Oct. 22 9:00-10:30 a.m.	**Seminars** **S5:** Advances in thermistor applications
10:45 a.m.-12:15 p.m.	**S6:** High-precision position measurement with eddy current technology
2:15-3:45 p.m.	**S7:** Integrated approaches to signal conditioning for sensor applications **S8:** The challenge of measuring humidity II: Papers
9:00 a.m.-12:15 p.m.	**Half-day tutorials** **HDT5:** Designing with the IEEE-P1451.2 Smart Sensor Communication standard **HDT6:** The challenge of measuring humidity I: Tutorial
2:15-5:30 p.m.	**HDT7:** Fundamentals of sensor technology II: Temperature **HDT8:** Fundamentals of sensor technology III: Pressure
9:00 a.m.-5:30 p.m.	**All-day tracks** **TRK2:** Applications of MEMS technology in new product development
Thurs.,Oct. 23 10:00-11:30 a.m.	**Question and answer session** **FR1:** The Sensors Magazine wish list—live and free

cluding application examples, and reviews recent advances in monolithic IC sensor technology.

The Technical Program

Testing and packaging are two of the most important and challenging issues in the manufacture of micromachined silicon IC sensors. That's what Theresa Maudie, manager of the Sensor Characterization, Reliability and Media Test Labs at Motorola's Sensor Products Div., will discuss in Seminar SI, "Sensor packaging and test: What users need to know," on Tuesday, Oct. 21, one of four seminars on that day. In her talk, she'll address the packaging and testing challenges from a standpoint of standards, packaging interconnections with device performance, modeling, and reliability. Finding common ground for sensor manufacturers and users on how a sensor should perform while remaining cost-effective, versatile, and compatible with silicon process technology.

Seminar S2, "Ethernet: A cost-effective strategy for monitoring remote signals and sensors," will be presented by Robert Winkler, an engineer with Intelligent Instrumentation Inc. He'll discuss the broad range of networked I/O choices available to link sensors, instruments, and/or processes often located in hostile environments and the role of Ethernet, which has migrated from the office to the factory floor.

Seminar S3, "Introduction to motion control," will be presented by Jim Planinsheck, a trainer and a project specialist at Allen-Bradley's Motion Control Div. He'll define the five main components of a typical motion-control system—motor, feedback sensor, actuator, controller, and communication network—and will address software and hardware issues. The seminar covers the differences between open-loop and closed-loop systems, motion-control buzzwords, and factors that influence the use of motion control for many applications.

Seminar S4, "The growing role of solid-state magnetic sensing," will be presented by Carl H. Smith, a consulting senior physicist at Nonvolatile Electronics (NVE) Inc. who has done primary work on characterizing giant magnetoresistive (GMR) sensors. He'll provide an update on recent innovations in solid-state magnetic sensing. These include Hall effect, magnetoresistive, and GMR sensor technologies. He'll discuss new GMR materials and structures that promise performance levels hitherto unachievable with other sensor technologies.

Tuesday, Oct 21 also will see four half-day-tutorial sessions, HDT1 through HDT4. Session HDTI, "Automotive sensor technologies and applications" is moderated by Joe Giachino, "Mr. Automotive Sensors" who is affiliated with the Ford Motor Co., and Roger Grace of Roger Grace Associates, a high-technology marketing and consulting firm that has done extensive studies of automotive sensor markets. This session will feature six other speakers besides Giachino's opening remarks and Grace's "Automotive sensors—an overview of markets" presentation. They include Jim Seefeldt of SSI Technologies who'll discuss "Active technology alternatives for ABS wheel speed sensors," Kyong M. Park of Kavlico Corp. will talk about "Ceramic capacitive oil deterioration sensors," and Karmit Sidhu of Measurement Specialties will present "High-pressure microfused sensor for diesel applications."

In addition, Jorg Schieferdecker of EG&G Heimann will talk about "Thermopile—A silicon infrared technology for passenger occupancy detection," Heyward Williams of the Maple Consulting Group will discuss "Microwave-based sensors for automotive collision avoidance," and Marek Wlodarczyk of Optran Inc. presents " Embedded fiber-optic combustion pressure sensors for electronic engine control."

Half-day-tutorial Session HDT2, "How to detect and measure vibration: A practical approach," will be presented by Jon Wilson, a lecturer and consultant on measurement and instrumentation. This session will cover the physics of vibration, terminology and concepts, vibration-measurement techniques and their pros and cons, principles of operation, and selection and application criteria.

Thurston Horton, a specialist in sensor education and technology, will present Session HDT3, "Fundamentals of sensor technology I: Proximity and position." He'll outline the basic operating principles and selection criteria for the most common presence-sensing technologies—inductive, capacitive, photoelectric, and magnetically actuated. He'll also discuss timing issues and current technology trends.

Half-day-tutorial HDT4, "Heavy duty data acquisition: The how and why of VXI" will be chaired by Fred Bode, executive director of services and a founding member of the VXIbus Consortium. He also is a publisher of the VXIbus Newsletter and administrative director of the VXIbus Consortium office. In this session, Bode will talk about "VXI architecture and data acquisition." He'll also be joined by National Instruments' Ron Wolfe for a talk on "Data acquisition for PCs to VXI," Paul Worrell of Hewlett-Packard's Measurement Systems Div. for a discussion on "VXI data acquisition solutions for product characterization," and Phil Hollenborst of HP's Lake Stevens Div. for a talk on "VDI data-acquisition solutions for noise and vibration characterization." In this session, attendees will hear from Tektronix's Dave Haworth on "Interoperable instrument drivers," and Kinetic Systems' Bob Cleary on "VXI data acquisition solutions for automotive testing."

Also featured on Tuesday, Oct. 21, will be all-day track TRK1, "Smart sensors and smart sensor communication," with a roster of notable speakers .The session is organized and chaired by Janusz Bryzek, a MEMS pioneer who initiated and chaired the IEEE TC-9

Want to go?

Sensors Expo '97 will be held at the Cobo Convention Center, Detroit, Mich, Oct. 20-23. The official hotel is the Westin in Detroit's Renaissance Center. Reservations can be made by calling (313) 568-8200; fax (313) 568-8666. For additional conference information, contact Expocon Management Associates, 363 Reef Rd., Fairfield, CT 06430-0915; (203) 256-4700; fax (203) 256-4730.

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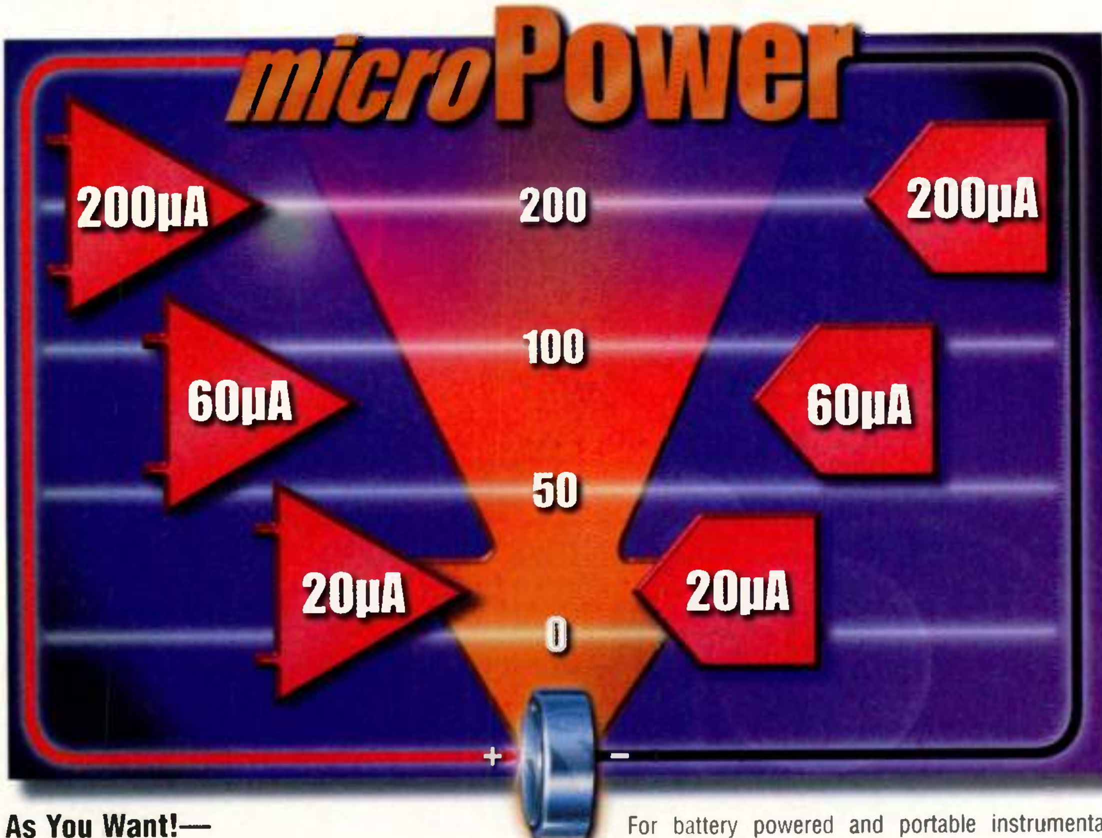

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ADS7817	12	±2.5	2.3	Yes	8-DIP, SO-8, MSOP-8	11369	81
ADS7822	12	+5	0.54	Yes	8-DIP, SO-8, MSOP-8	11358	82
ADS1212	22 at 10Hz, 16 at 1kHz	+5	1.4	Yes	18-DIP, SO-18	11360	83
ADS1213	22 at 10Hz, 16 at 1kHz	+5	1.4	Yes	24-DIP, SO-24	11360	84
ADS1214	22 at 10Hz, 16 at 1kHz	+320mV	1.4	Yes	18-DIP, SO-18	11368	86
ADS1215	22 at 10Hz, 16 at 1kHz	+320mV	1.4	Yes	24-DIP, SO-24	11368	87

IAs

Product	I_Q (µA)	Description	Channels	Packages	FAX*LINE#*	Reader#
INA122	60	Single Supply Instrument Amp	1	SO, DIP	11388	90
INA126	175	Precision Instrument Amp	1, 2	MSOP, SO, DIP	11365	91
INA132	160	Difference Amp	1	SO, DIP	11353	114

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Product	I_Q (µA)	Description	SR (V/µs)	Channels	Packages	FAX*LINE#*	Reader#
OPA336	20	CMOS	0.03	1, 2, 4	SOT-23, MSOP, SO, DIP	11380	115
OPA241	25	Precision	0.01	1	SO, DIP	11406	116
OPA237	170	Gen. Purpose	0.5	1, 2, 4	SOT-23, MSOP, SSOP, SO	11327	117

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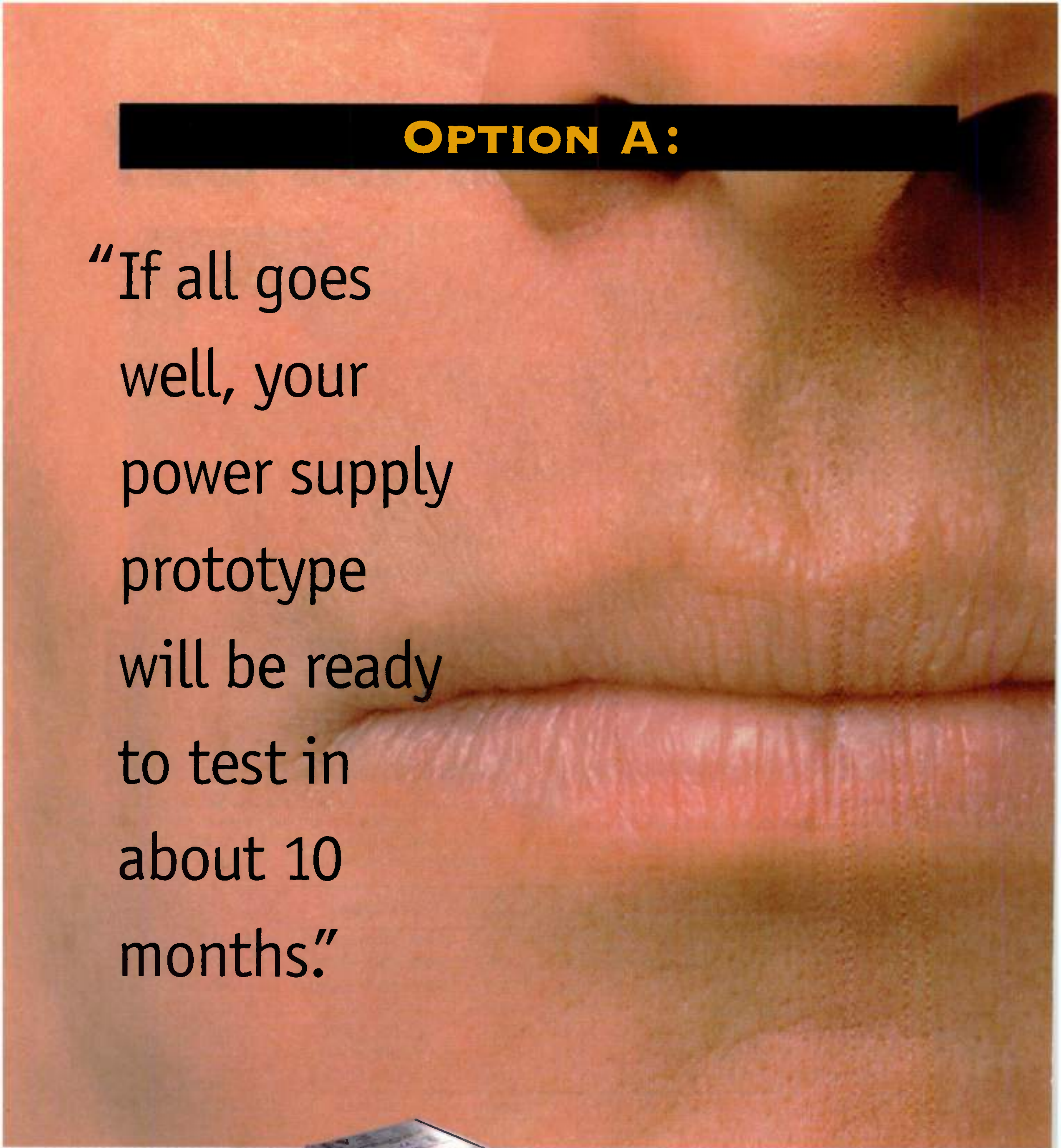

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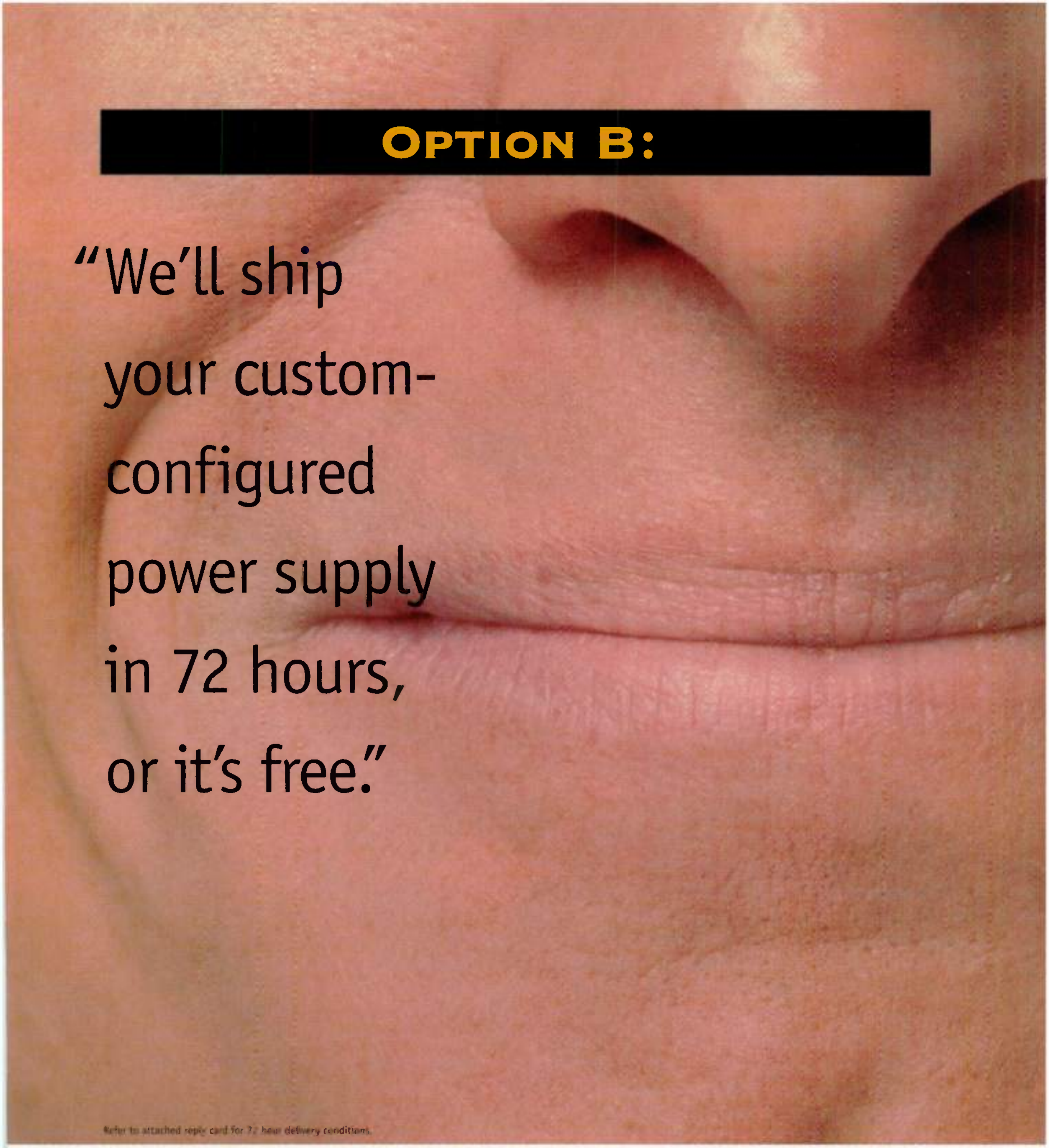

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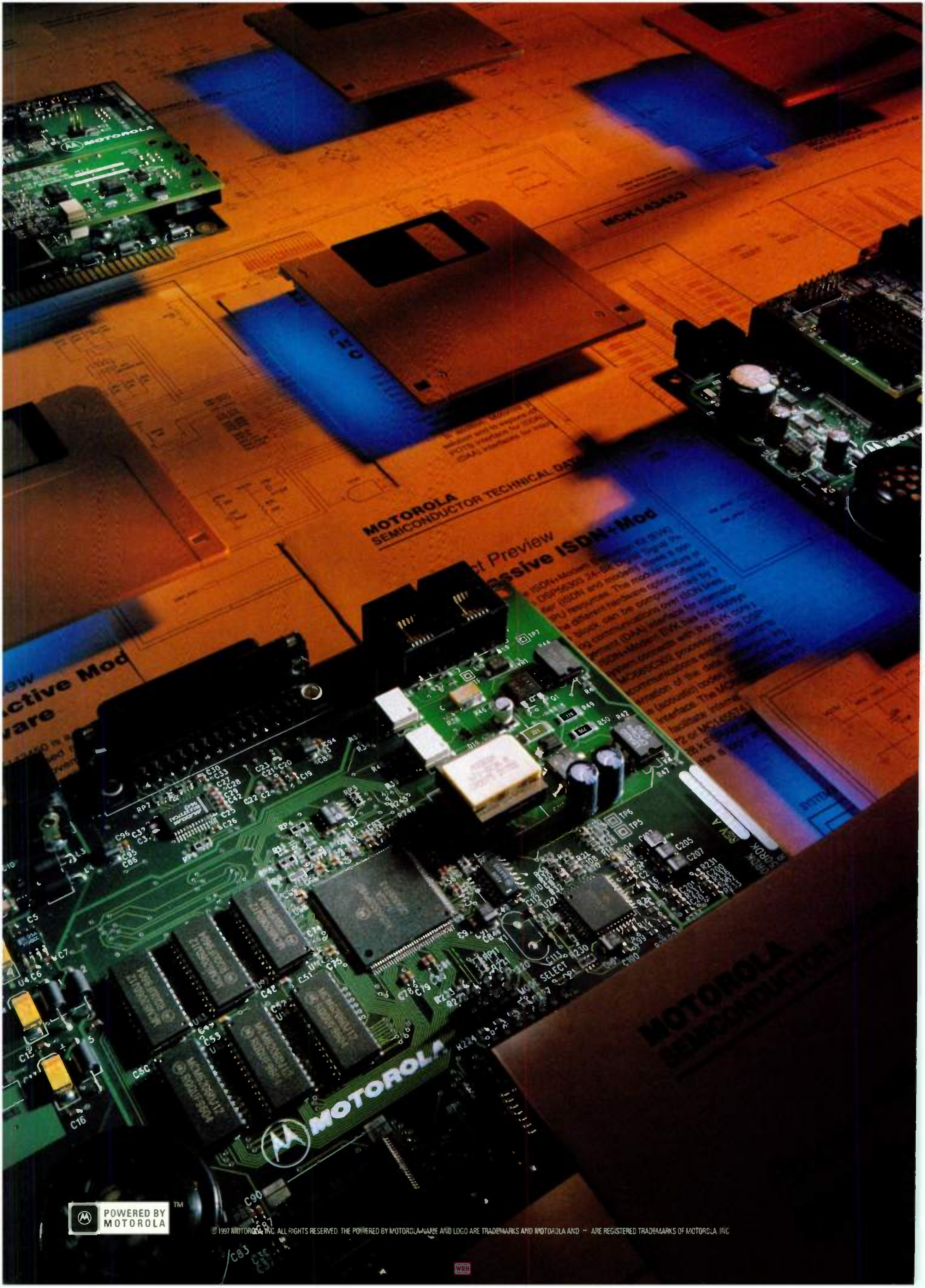
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SINGLE OUTPUT MODULES					
2V	30.0	66	1.8–2.2	1	**A**
2V	60.0	132	1.8–2.2	2	**B**
3.3V	30.0	108	3.0–3.6	1	**D**
3.3V	60.0	216	3.0–3.6	2	**E**
5V	30.0	150	4.5–6.0	1	**G**
5V	60.0	300	4.5–6.0	2	**H**
12V	17.0	204	10.8–13.2	1	**J**
12V	30.0	360	10.8–13.2	2	**K**
15V	14.0	210	13.5–16.5	1	**M**
15V	24.0	360	13.5–16.5	2	**N**
24V	8.5	204	21.6–26.4	1	**P**
24V	15.0	360	21.6–26.4	2	**Q**
28V	12.0	336	25.2–30.8	2	**8**
36V	11.0	396	32.4–39.6	2	**3**
48V	4.0	192	43.2–52.8	1	**S**
48V	8.0	384	43.2–52.8	2	**T**
DUAL OUTPUT MODULES					
12V & 5V	10 & 4	150	±10%	1	**V**
5V & 12V	10 & 4	150	±10%	1	**W**
12V & 12V	10 & 4	150	±10%	1	**Y**
15V & 15V	8 & 3	150	±10%	1	**Z**

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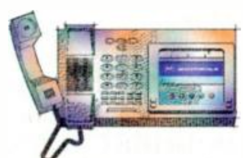

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Smart Sensor Communication Standard Activities. He is a cofounder of NovaSensor Corp. and is now with the Intelligent MEMS Products Group at Maxim Integrated Products.

Speakers in this track include Kang Lee of the National Institute of Standards and Technology (NIST) who'll present "Introduction and overview of the IEEEP1451—a family of proposed smart transducer communication interface standards." He'll be followed by HP's Jay Warrior who'll talk about the "IEEE P1451.1 network-capable application processor information model. Overview and status update." HP Labs' Stan Woods and Boeing's Lee Eccles will present the "IEEE P1451.2 smart transducer interface module. Overview and status update." This will be followed by Boeing's Larry Malchodi who'll talk about the "IEEE P1451.3 distributed multidrop systems. Status update." Next, Steven C. Chen of Aeptec Microsystems will discuss the "IEEE P1451.4 proposed project for mixed-mode communication protocols and transducer electronic data sheet (TEDS) formats."

Other speakers include Robert N. Johnson of Electronics Development Corp. who'll talk about "Implementation of a smart transducer using the IEEE P1451.2 standard interface," Rockwell's Hank Marcy and UCLA's Bill Kaizer who'll present "Integrated wireless sensors," and the University of Michigan's Selden Crary will discuss "Developing optimized compensation algorithms for smart sensors." Other speakers include MCA Technologies' Ali Rastigar on "High-performance smart piezoresistive sensor compensation using electronic trimming," Ted Smith, Michel Chevroulet, and Jean Paul Bardyn of CSEM on "Low-power sensor interfaces," and David Zehrbach and Randy Frank of Motorola on a "Single-chip pressure sensor with integrated microprocessor." During this all-day track, a demonstration will be provided on wireless connectivity for sensors.

On Wednesday. Oct. 22, four seminars will be held—S5 through S8. In S5, "Advances in thermistor applications" presented by William R. Siwek, biomedical applications manager for Thermometrics Inc., information is presented on the selection and design of thermistor sensor assemblies for specific applications. Two types of thermistors will be covered, NTC and PTC. In S6, "High-precision noncontact position measurement with emphasis on eddy current technology," Scott D. Welsby, engineering manager at Kaman Instrumentation's Measuring Systems Product Group, will discuss measurement precision and accuracy trade-offs and will review the technology of noncontact measurement devices. He'll also touch on signal processing considerations.

In Seminar S7, "Integrated approaches to signal conditioning for sensor applications" moderated by Mike Dunbar, who is affiliated with Integrated Sensor Solutions Inc., several papers will be presented on developments in CMOS technology that now allow high-performance precision analog and mixed-signal signal-conditioning ICs for sensors. And in Seminar S8, "The challenge of measuring humidity II: Papers," moderated by Jim Schleckser, president of General Eastern Instruments Inc., several papers will be presented that cover the range of humidity measurement technologies and applications from relative humidity to measurements in the parts-per-billion range.

Also on Wednesday, Oct. 22, are four half-day tutorial sessions, HDT5 through HDT8. HP Lab's project manager Stan Woods will talk about "Designing with the IEEE P1451.2 smart sensor communication standard" in HDT5 The focus is to teach engineers how to design a smart transducer interface module (STIM) as called out in the IEEE P1451.2 draft standard. Attendees will learn about the hardware and software required for such a design. In HDT6, "The challenge of measuring humidity I: Tutorial" by independent consultant Sumner Weisman will focus on the basic gas laws that affect the measurement of humidity. It will look at the concept of vapor pressure, define commonly used measurement units, and describe commonly used humidity sensors.

In HDT7, "Fundamentals of sensor technology, part II: Temperature" by James Sulciner, a veteran of metallurgical, chemical and process engineering, a different broad range of temperature-sensing and measurement applications will be covered with a focus on RTDs. And in HDT8, "Fundamentals of sensor technology III: Pressure" by Jon Wilson, the basic principles and selection criteria of pressure sensing will be presented.

Also on Wednesday, Oct 22, is all-day track TR2, "Applications of MEMS technology in new product development." Moderated by Roger Grace, it includes a dozen notable speakers. Grace will open up the track with his talk "Commercialization of MEMS/MST." This will be followed by "The emerging infrastructure for the commercialization of MEMS/MST technologies" presented by NJIT's Steve Walsh and Hilary Mados, as well as Robert Boylan of RPI. Frank Hartley of JPL will discuss "Micro-pump technology and applications," Ralph Fenner of Hygrometrix will talk about "MEMS shear/stress hygrometry," CSEM's Y. de Coulon, M. Chevroulet, Y. Dupraz, and J. Bergqvist will present an "Inductive microsensor for position and speed," and William Higdon of MTI Analytical Instruments will discuss "Microfluidic applications of MEMS in analytical instruments."

Additional speakers include Texas Instruments Mike Mignardi on "MEMS digital mirror technology for display applications," Northeastern University's Nicol E. McGruer, Paul M. Zavracky, R. Morrison, and Sumit Majumder on "Microswitches and relays," Sentir's Gene Burk on "Silicon micromachined Fabray-Perot interferometer for medical applications," Microsensors Inc.'s Ying Hsu and J. Bruce Totty on a "Silicon microwheel gyro and universal capacitive readout," Ohio State University's Marc Madou on "MEMS chemical sensors for oil degradation," and SSI Technologies' Jim Seefeldt on an "Automotive silicon pressure sensor for automotive applications." Grace will also deliver a talk during this track on "Automotive applications of MEMS."

On the conference's final day, Thursday, Oct. 23, there will be a "Sensors Magazine wish list." This is a hands-on 90-minute question and answer workshop in which veteran sensor expert Dr. David Wobschall will answer audience questions about any sensor application.

HOW VALUABLE	CIRCLE
HIGHLY	531
MODERATELY	532
SLIGHTLY	533

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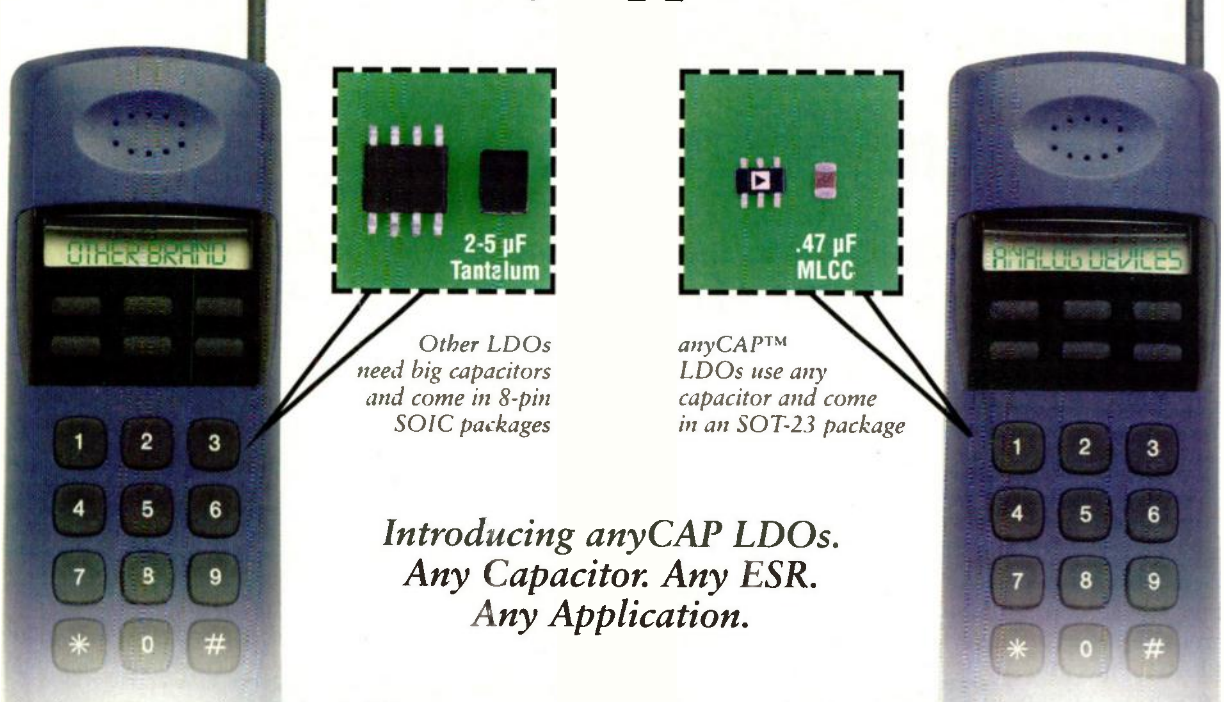

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ADP3302	0.1 V	100	0.8%,	1.4%	SO-8, Dual Output, TCP*	2014
ADP3303	0.18 V	200	0.8%,	1.4%	SO-8, TCP*	2043
ADP3306	0.3 V	300	1.0%,	1.5%	SO-8, TSSOP-14, TCP*	2236
ADP3307	0.08 V	100	0.8%,	1.4%	SOT-23	2300

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Monolithic Silicon Temperature Sensors Challenge Thermistors, RTDs, And Thermocouples

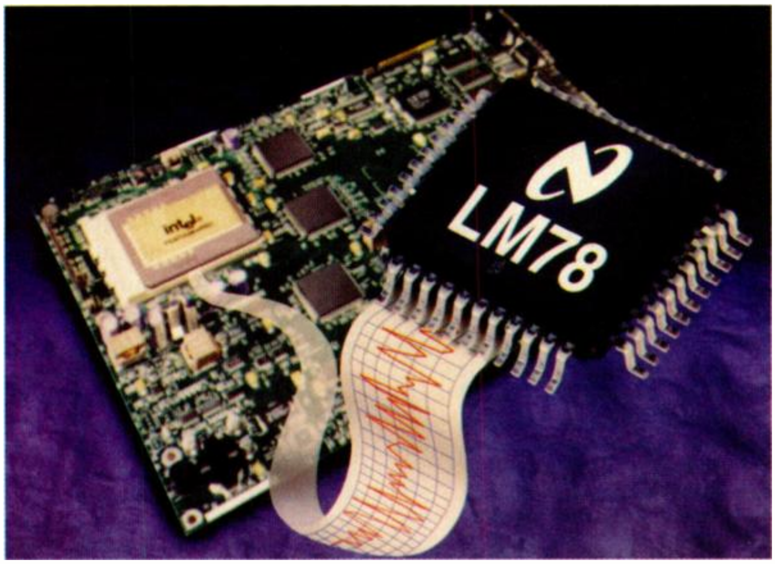
New Sensors Add Linearization And Analog Control Circuits, Along With ADCs And Digital Interface Circuits.

Frank Goodenough

SPECIAL REPORT

Silicon makes both good and bad sensors. Though that may sound contradictory, it's true. Not only is silicon sensitive to light, but it's also sensitive to stress (it's piezoresistive) and to temperature. But if you solve the other sensitivity problems (IC producers have done that) and with a little analog circuit design, silicon becomes a low-cost, reliable, accurate, linear, temperature sensor.

Silicon temperature sensors have advantages and disadvantages relative to the other common temperature sensors: RTDs (resistance temperature detectors), thermocouples, and thermistors. Note that almost any passive device can act as a temperature sensor by calibrating its temperature coefficient.



Art Courtesy: National Semiconductor

Pros And Cons

When they're compared with other types of temperature sensors, silicon temperature sensors offer a number of advantages:

- They're less expensive than RTDs.
- They're significantly more linear than thermistors.
- They're more linear than thermocouples and therefore easier to use (they require simpler signal conditioning).
- They offer a high-level output and are easier to use than RTDs or thermocouples (simpler signal conditioning) that put out mVs or µVs full scale.
- Most silicon temp sensors can be built in IC form and can incorporate other analog or digital functions on-chip.
- While silicon sensors do not have the operating temperature range of RTDs (platinum RTDs are accurate, linear, and repeatable from approximately -250°C to 750°C), their other advantages stand out from below -50°C to over 150°C. Most thermistors cover this temperature range as well, and thermocouples are mandatory at temperatures beyond the range of the RTD.

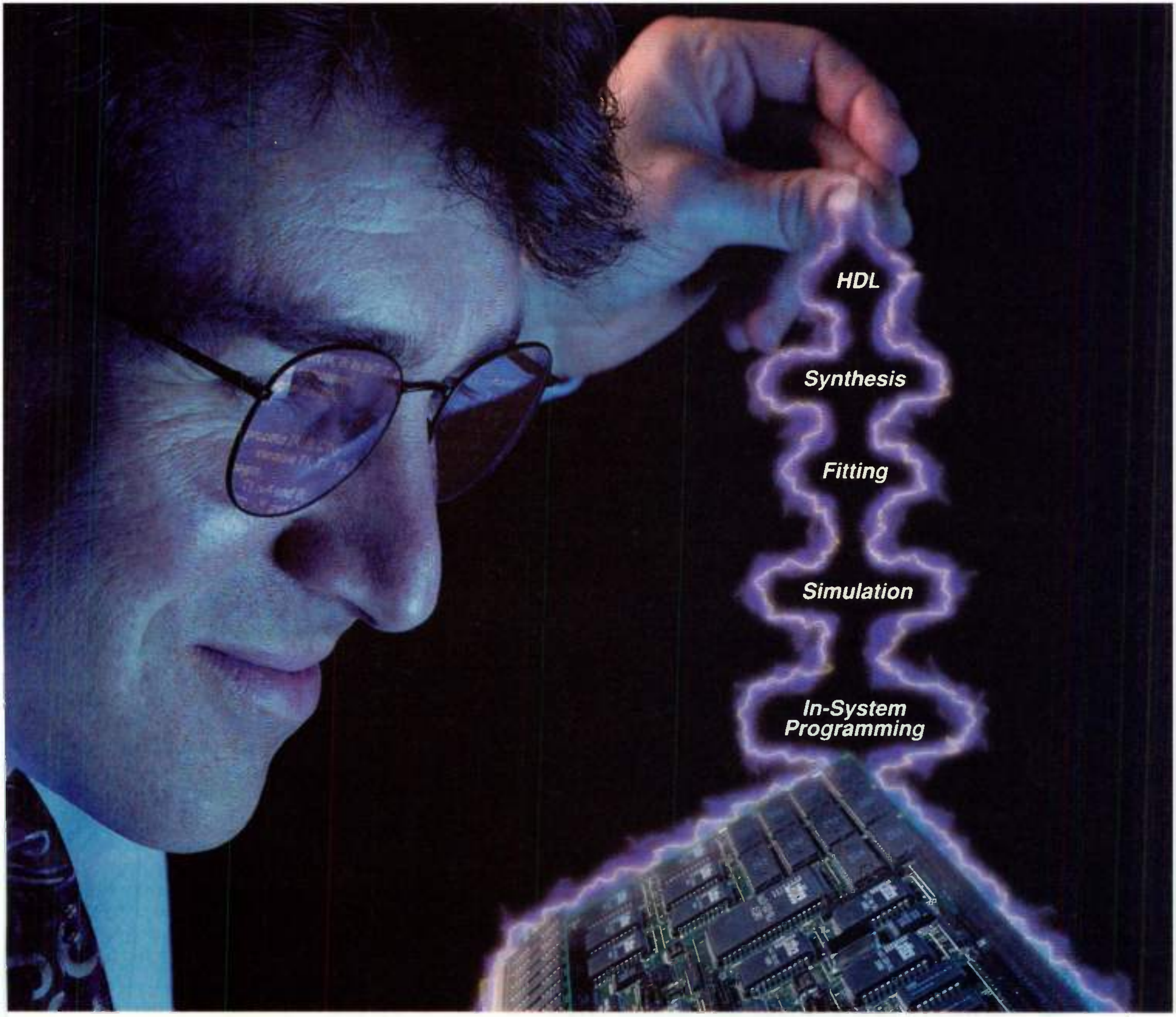
On the other hand, silicon IC sensors also have their shortcomings:

- They're not as accurate or as linear as RTDs.
- They're more costly than thermocouples or thermistors.
- They feature a smaller temperature range than RTDs, thermocouples and a few thermistors.
- Because of their plastic package, they are slower in response than thermocouples.

Silicon IC temperature sensors are not as inexpensive as thermistors. But at less than 50 cents each (in high volumes), they can challenge thermistors in many applications while taking on RTDs and thermocouples in other tasks.

Years ago, several companies had product lines containing bulk-silicon resistor temperature sensors that weren't very accurate and soon faded away. The next step after bulk silicon came the pn junction, which has forward- and back-breakdown temperature coefficients. Then came the bipolar transistor with its several pn junctions and their many individual transfer curves, each with a different temperature coefficient.

The first actual silicon temperature sensors was developed about 20 years ago at Analog Devices.



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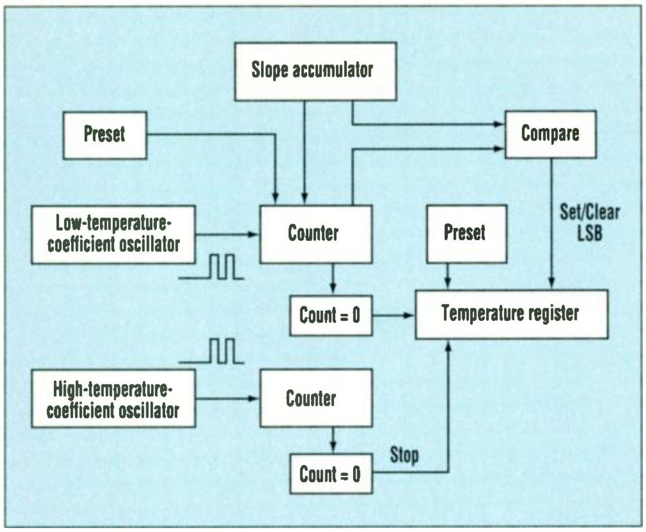
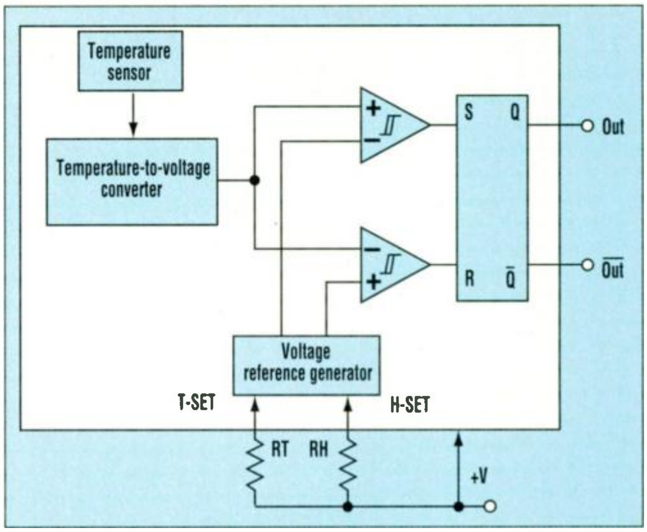


1. The DS1720 from Dallas Semiconductor measures temperature by counting the number of clock cycles an oscillator with a tight temperature coefficient goes through during a gate period. The period is set by another oscillator with a poor temperature coefficient.



2. The user sets the trip temperature and the hysteresis of the Telcom TC07 temperature sensor with a pair of external resistors, RT and RH. The resistors set the output of a voltage reference which goes to the plus input of one comparator and the minus input of the other.

The IC was ultimately marketed as the AD590, a two-terminal device. It put out a constant current that was proportional-to-absolute temperature (PTAT). That is, the current output was proportional to the temperature in Kelvins. Scale factor was 1 µA/K. At room temperature, or 273 K, output current was 273 µA.

Though relatively slow, the AD590 first appeared in a TO-18 metal can. It was then put in a ceramic/metal package about 3/8-in. long and 3/16-in. wide. Response to a temperature change was faster than today's sensors in their plastic TO-92, SOT-23, and SO-8 packages, but the package cost too much (more than that of the IC it contained).

Earlier this year, Analog Devices announced the release of the TMP17, a two-terminal device with similar specifications in an SO-8 package. It runs off 4 to 30 V and typically takes about 9 seconds to respond to within 95% of the final value for a temperature change in a stirred-oil bath. In today's plastic-packaged temperature sensors, the leads carry heat between the heat's source and the sensor, so they must be soldered to the "hot spot."

Bandgap Core

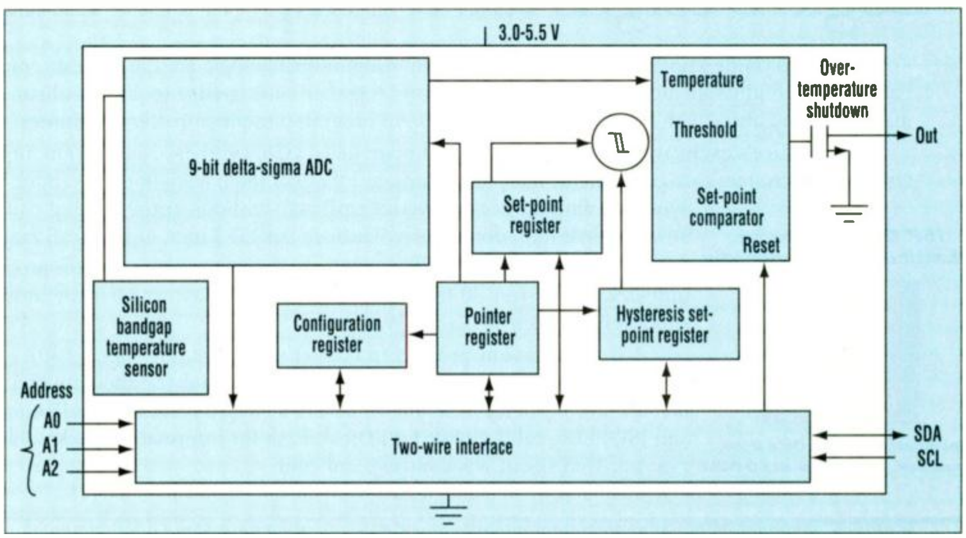
Many silicon temperature sensors take advantage of a basic property of silicon bipolar junction transistors (BJTs) to create a PTAT current: they create a bandgap core. If two identical BJTs operate at a constant ratio (r) of collector current, the difference in their base emitter voltage equals:

$$(kT/q)(\ln r)$$

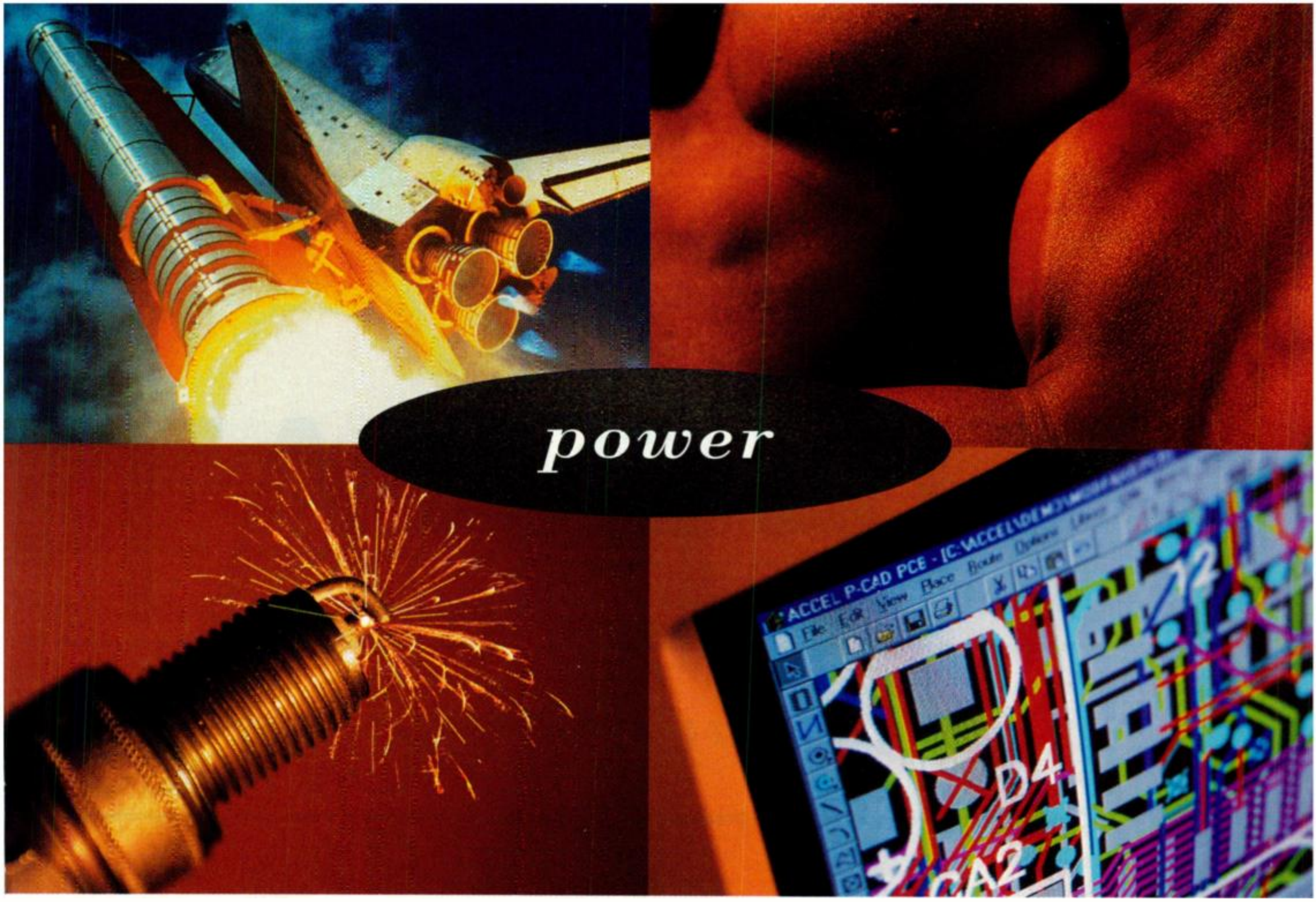
where
k = Boltzman's constant
T = absolute temperature in Kelvins
q = the charge on the electron, and
ln r = the natural log of the ratio r

Since k and q are constant, the difference in voltage is the PTAT value. In the TMP17, the voltage is converted to a PTAT current by a thin-film resistor with a close-to-zero temperature coefficient. The PTAT current also forces the output current to be PTAT. The result is a current source with an output equal to a scale factor multiplied by the temperature in Kelvins.

The use of a low-cost device ($1.18 each in 1000-unit lots) like the TMP17 can improve and simplify temperature measurement where thermistors or other types of temperature sensors are being used. National Semiconductor has a family of similar sensors (the LM134) that goes for the same price.



3. National Semiconductor's LM75 IC temperature sensor operates in a standalone mode or in a controlled mode under the supervision of a host processor.



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However, the basic sensor has 3 terminals. A resistor from the third terminal to the load sets the voltage across the load. Most users run the PTAT current source through a resistor to create a PTAT voltage.

Voltage Wanted

Since most system designers prefer voltage than current, most temperature sensors today put out a voltage proportional to temperature rather than a current. In addition, users want a room temperature-referenced reading in degrees Celsius or Fahrenheit. And since the sensors are ICs, designers have inserted a fixed correction factor that converts signals from absolute temperature in Kelvins to Celsius or Fahrenheit. Their scale factor is in µA/°C or µA/°F *(see the table)*.

As noted above, since these sensors are ICs, it's relatively easy to add some form of analog or digital control or measurement circuitry. A few years ago, Telcom Semiconductor announced one of the first of these simple solid-state thermostats. Like many versions since, besides the temperature-sensing circuitry, it contained a couple of compara-

A SAMPLING OF SILICON IC TEMPERATURE SENSORS

Company and model number	Operating-temperature range	Output	Calibration	Operating-voltage range	Scale factor	Accuracy	Supply current	Package	Price (in 1000-unit lots)
Analog Devices									
ADT41	10 to 125°C	Voltage	Celsius	2.7 to 12 V	10 mV/°C	±1°C (at 25°C) ±2°C (at -40 to 125°C)	NA	SOT-23	$0.50
ADT42	-40 to 125°C	Voltage	Celsius	2.7 to 12 V	10 mV/°C	±1°C (at 25°C) ±2°C (at -40 to 125°C)	NA	SOT-23	$0.50
ADT43	5 to 100°C	Voltage	Celsius	2.7 to 12 V	20 mV/°C	±1°C (at 25°C) ±2°C (at -40 to 125°C)	NA	SOT-23	$0.50
TMP17	-40 to 105°C	Current	Celsius	4 to 30 V	1 µA/°C	±4°C (over temperature)	NA	SO-8	$1.18
TMP35	10 to 125°C	Voltage	Celsius	2.7 to 5.5 V	10 mV/°C	±1°C (at 25°C) ±2°C (at -40 to 125°C)	50 µA	SOT-23	$0.65
TMP36	-40 to 125°C	Voltage	Celsius	2.7 to 5.5 V	10 mV/°C	±1°C (at 25°C) ±2°C (at -40 to 125°C)	50 µA	SO-8	$0.65
TMP37	5 to 100°C	Voltage	Celsius	2.7 to 5.5 V	70 mV/°C	±1°C (at 25°C) ±2°C (at -40 to 125°C)	50 µA	TO-92	$0.65
National Semiconductor									
LM34A/35A	-50 to 300°F/ -55 to 150°C	Voltage	Farenheit/ Celsius	5 to 30/ 4 to 30 V	10 mV/°F/ 10 mV/°C	±2°F/±1°C	163 µA/ 133 µA	TO-46	$8.75/$11.40
LM34/35	-50 to 300°F/ -55 to 150°C	Voltage	Farenheit/ Celsius	5 to 30/ 4 to 30 V	10 mV/°F/ 10 mV/°C	±3°F/±1.5°C	181 µA/ 161 µA	TO-46	$7.30/$8.75
LM34CA/ 35CA	-40 to 230°F/ -40 to 110°C	Voltage	Farenheit/ Celsius	5 to 30/ 4 to 30 V	10 mV/°F/ 10 mV/°C	±3°F/±1.5°C	142 µA/ 116 µA	TO-46, TO-92	$4.00
LM34C/35C	-40 to 230°F/ -40 to 110°C	Voltage	Farenheit/ Celsius	5 to 30/ 4 to 30 V	10 mV/°F/ 10 mV/°C	±3°F/±1.5°C	159 µA/ 141 µA	TO-46, TO-92	$3.10
LM34D/35D	32 to 212°F/ 0 to 100°C	Votlage	Farenheit/ Celsius	5 to 30/ 4 to 30 V	10 mV/°F/ 10 mV/°C	±4°F/±2°C	159 µA/ 141 µA	TO-46, TO-92, SO-8	$0.90/$0.82
LM134-3	-55 to 125°C	Current	Kelvin	1 to 40 V	Set by user	±3°C (over temperature)	1 mA	TO-46	$4.95
LM334	0 to 70°C	Current	Kelvin	1 to 40 V	Set by user	±6°C (over temperature)	1 mA	TO-46, TO-92, SO-8	$0.90
LM45B/45C	-20 to 100°C	Voltage	Celsius	4 to 10 V	10 mV/°C	±3°C/±4°C	160 µA	SOT-23	$0.93/$.90
Telecom Semiconductor									
TC102	-20 to 125°C	Voltage	Celsius	3 to 12 V	10 mV/°C	±8°C (over temperature)	60 mA	SOT-23, TO-92	NA
TC103	-20 to 125°C	Voltage	Celsius	2.2 to 12 V	10 mV/°C	±8°C (over temperature	60 µA	SOT-23, TO-92	NA
TC1132	-20 to 100°C	Voltage	Celsius	3 to 12 V	10 mV/°C	±8°C (over temperature)	80 µA	SOT-23, TO-92	NA
TC1133	-20 to 125°C	Voltage	Celsius	2.2 to 12 V	10 mV/°C	±8°C (over tempeature)	80 µA	SOT-23, TO-92	NA

NA = not available

tors that tripped at two different user-programmed set points. The company hoped that the device might replace the snap-action device that protect motors in many home appliances.

However, they soon found a customer who bought a few and then gave them a volume order—but the customer would not tell the company what it was using the chip for. It turns out that the heat generator, called the Pentium processor, had arrived on the scene and fans were being added to PCs to cool them.

Initially, the system had to be able to shut down if the environment got too hot, and come back on when it had cooled enough so that the microprocessor could survive. This marked the beginning of the "science" of thermal management, a special niche of today's "hot button" power management. Since that early day, Analog Devices, National Semiconductor, Maxim Integrated Products, and Dallas Semiconductor, have joined Telcom in the arena.

Each company has developed proprietary techniques for temperature measurement in order to not step on competitors' patents and/or to adapt to a specific process and/or to come up with a unique approach. For example, Telcom uses a single pn junction to develop a PTAT voltage or current, while Dallas Semiconductor has taken a different tack—all their temperature sensors are essentially digital thermometers/thermostats. To measure temperature, they employ a unique 9-bit analog-to-digital converter (ADC) *(Fig. 1)*. That is not to say that some of the others have not added ADCs.

For example, Dallas Semiconductor's DS1720 digital thermometer/thermostat measures temperature to 9-bit accuracy. It provides three digitally programmed thermal alarm outputs—T-HIGH, T-LOW, and T-COM. T-HIGH goes high when the chip's temperature goes above a user-programmed temperature. T-LOW goes high if the chip's temperature runs below a user-programmed threshold. T-COM goes high when the chip's temperature rises above the T-HIGH threshold, and it stays high until the temperature drops below the T-LOW threshold. All three outputs can be used as control (thermostat) signals.

The DS1720 measures temperature by counting the number of output pulses produced by an oscillator with a low temperature coefficient during a gate period determined by an oscillator with a high-temperature coefficient. The counter is set at a base count that corresponds to -55°C. If the counter reaches zero before the gate period is over, the temperature register, also preset to -55°C, is incremented, indicating that the temperature is above -55°C.

At the same time, the counter is preset with a value determined by the slope accumulator circuit. It compensates for the parabolic behavior of the two oscillators overtemperature by changing the number of counts that the counter must count for each incremental degree in temperature. To obtain the desired 9-bit temperature resolution, both the value in the counter and the number of counts per degrees Celsius (the value in the slope accumulator) at a given temperature must be known. The DS1720 performs this calculation to provide 0.5°C resolution. The data is transmitted to the host via a three-wire serial interface. In addition to the DS1720, Dallas Semiconductor has devices sporting one- and two-wire serial interface links with a processor. The DS1720 comes in an 8-pin SOIC package.

Before jumping into additional advanced "thermal management" ICs, let's take a look at Telcom's basic TC07 *(Fig. 2)*. By connecting the resistor (RT) from the T-SET pin to the supply rail, the user sets the temperature at which the output goes high. A second resistor (RH) from the H-SET pin to the rail sets the hysteresis. That is, RH sets the temperature to which the chip must drop before the latched outputs return to their original state. The resistors set the output of a voltage reference which goes to the plus input of one comparator and the minus input of the other. Depending on the choice of output pin, the thermostat can control either a cooler (a fan) or a heater. Both Analog Devices and National Semiconductor offer similar devices.

Companies Mentioned In This Report

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Wanted: More Features

Once system designers caught on to what was possible, they wanted everything, including a link with the processor, so it could control its own destiny. And the analog community was "ready, willing, and able" to meet the demands of system designers. National's latest "Jack of All Trades" for the "thermal management arena" is the LM75 *(Fig. 3)*. It's a digital temperature sensor and thermal watchdog timer with a two-wire interface. It implements a two-wire I^2C link with a processor.

The LM75 contains a 9-bit delta-sigma ADC and a digital overtemperature detector and the two-wire interface. The host processor can query the chip at any time to read temperature. An open drain overtemperature shutdown (OS) output becomes active when the temperature of the chip exceeds a digitally programmable limit. This output can operate in either a comparator or an interrupt mode. The user programs both the OS threshold and the temperature at which the alarm condition drops out (the hysteresis). As a re-

sult, the chip enables the host to turn itself off if the environment gets too hot to handle. In addition, the user programs the hysteresis. The chip powers up in the comparator mode with a default overtemperature shutdown of 80°C, and 5°C of hysteresis.

Telcom's latest device, the TCN75, is virtually a second source for National's LM75. A serially programmable temperature sensor, it notifies a host when the ambient temperature exceeds a user-programmed setpoint. Hysteresis is similarly programmable. An output labeled INT/COM is programmable as either a simple comparator for thermostat operation or as a "temperature-event" interrupt. The host communicates with the TCN75 via a standard two-wire bus. It lets the host read the current temperature of the chip, and program the setpoint and hysteresis.

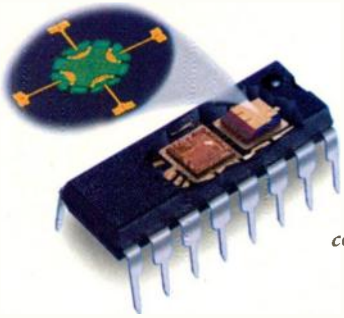
The TCN75 powers up in the comparator mode with a default setpoint of 80°C and 5°C of hysteresis. The defaults allow independent operation as a standalone thermostat without a host. Address inputs let eight TCN75 share a common bus. The TCN75 comes in 8-pin DIPs, SOICs, and tiny TSSOPs. Like the LM75, it sports a 9-bit delta-sigma ADC.

Maxim is the latest company to jump into the silicon temperature-sensor arena. An output of the MAX6501 family of Temperature Resets asserts a logic high when a measured temperature crosses a factory-programmed threshold. And they have been crammed into a tiny 5-pin SOT-23 package. Since the set points are factory programmed, no additional parts are needed.

Two different output circuits are available. The MAX6501/3 comes with an open-drain output intended to interface with a host reset input. The MAX6502/4 has an active-high push-pull output intended to drive fan-control logic. Maxim provides family members with 8 available off-the-shelf standard temperatures: -15°C, 5°C, 45°C, 55°C, 65°C, 75°C, 85°C, and 95°C. Hysteresis is set at 2°C or 10°C by a logic signal.

How Valuable	Circle
Highly	534
Moderately	535
Slightly	536

Motorola's Sensors



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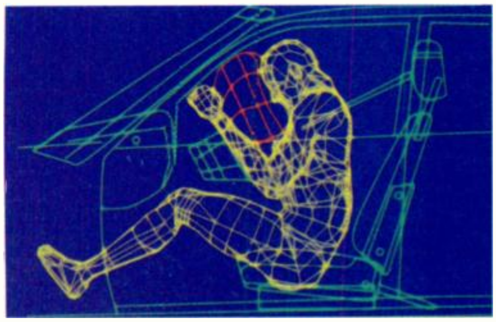

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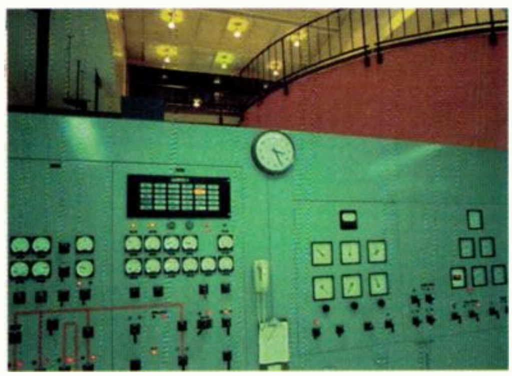

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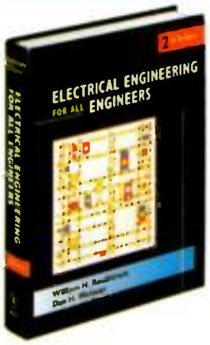

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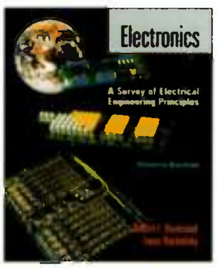

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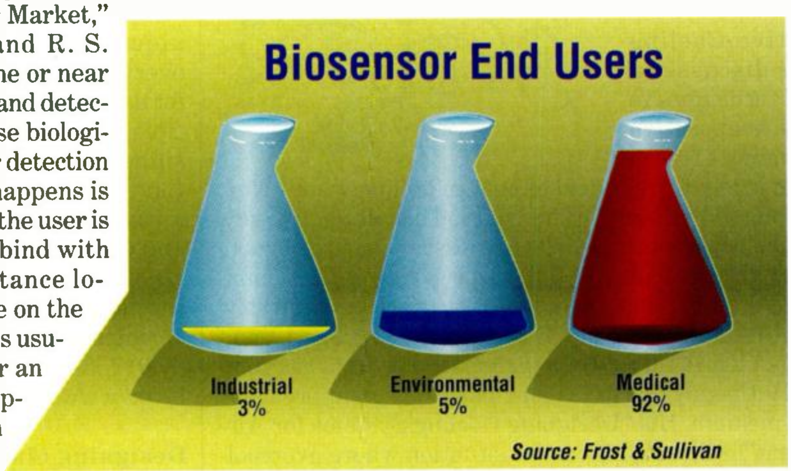
ELECTRONIC DESIGN QUICK LOOK

■ Edited by Mike Sciannamea and Debra Schiff

MARKET FACTS

A Sense Of The Unexpected

At the beginning of their existence, biosensors were expected to change the entire landscape of sensing technology. Well, it's taken them a long time, but biosensing instruments are finally moving from research laboratories into the environmental, industrial, and medical markets. For those who may need a little clarification, biosensors, according to a new report, "An Overview of the World Biosensor Market," by S. D. Kilmetz and R. S. Bridge, are "real-time or near real-time measuring and detection devices which use biological molecules as their detection component." What happens is whatever compound the user is seeking to find will bind with the biological substance located on a membrane on the device. The analysis is usually done with either an electrochemical or optical transduction process. One trend that greatly helped the leap forward for these important devices was the commercial success of hand-held blood analyzers. These instruments are responsible for the reduced time of analysis, drop in cost, and increased miniaturization in the medical diagnostics field. Such names as Diametrics, i-Stat, MediSense, and Nova Biomedical are the major players in the medical point-of-care market. The new names to be on the lookout for, in a variety of markets, are Azur Environmental, Biacore, BioTechnical Resources, Ohmicron, Molecular Devices, Quantech, and Yellow Springs. Last year, according to the report, the worldwide market for biosensors added up to just over $400 million. Frost & Sullivan's projection for the year 2000 expects the world market for biosensors to surpass $500 million. Of the majority of biosensors targeted toward the medical arts and research, 90% comprises blood gas analyzers, electrolyte analyzers, glucose meters, and metabolite analyzers. Over 50% of those biosensors can be attributed to glucose meters. Trends point to a drop, though, in glucose meters, due to noninvasive sensors based on electromosis or infrared technologies. Of the outstanding technologies available in blood analysis, two are amperometric and potentiometric biosensors. They both are used in Biacore's optical biosensor systems. These systems are based on Surface Plasmon Resonance technology, which uses the refractive index of the membrane to pick up the concentrations of a given substance. Units have been priced from $80,000 to $125,000. Two other companies, Affinity Sensors and BioTechnical Resources, offer similar optical systems for different applications. The report asserts that the medical sector will continue to dominate the worldwide biosensor market, especially since better performance and lower prices will be driving the sales. But, because the Food and Drug Administration's regulations take months to complete to approve a new device, it may take longer for the growing market to bring new products to the biosensor arena. Although biosensors are included in some military applications, the two other sectors of the biosensor market belong to environmental (5%) and industrial (3%) applications. These sectors have not skyrocketed into the market because of prohibiting technical and application issues. Currently, the industrial sector only has one biosensor supplier to the food and beverage market—Yellow Springs International. Last year, gross revenue totaled $10.9 million for the industrial sector of the world biosensor market. The environmental sector's tally neared $20 million in the same time period. This market sector saw waste and water sensing instruments and bioluminescent devices from Yellow Springs International and Azur Environmental, respectively, performing well in the market. According to the report, the majority of biosensor technology development is focused on competing with chromatographs, gas sensors, immunoassay kits, refractometers, and mass spectrometers.



For more information, contact Frost & Sullivan, 2525 Charleston Rd., Mountain View, CA 94043; (415) 961-9000; fax (415) 961-5042.—DS

40 YEARS AGO IN ELECTRONIC DESIGN

Editorial: A Problem Is Ventilated

The staggering cost of electronic repairs in the field emphasizes the vital importance of reliability in original equipment design. More often than not, troubles are traced to overheating. This issue has accentuated the need for better thermal design. Authorities in the field of thermal design are in complete agreement on one score. The electronic design engineer is woefully inattentive to the thermal aspects of his design. The usual practice, it seems, is to complete a design, complete the chassis layout, then, observing an unoccupied corner of the chassis, comment, "I guess we can put a fan there."

This situation, exaggerated perhaps, is nevertheless representative. The literature abounds in theoretical approaches to thermal problems. The electronic design engineer has little enough time, and sometimes inadequate background, to permit himself the luxury of an intensive study of thermal design.

In answer to the need for basic, practical design information, this issue of *Electronic Design* is devoted principally to the problems of cooling electronic equipment. We have assembled a variety of articles to present a many-sided picture of the cooling problem and approaches to its solution.

In "A New Evaporative Cooling Technique," Mr. Berner discusses a method employing two old techniques to form a new approach. The evaporative technique is, in itself, not new. It is well known that equipment can reject a great deal of heat in boiling water. Normally, components are immersed directly in the water. This, unfortunately, raises problems of corrosion, insulation, and dielectric losses. The use of good, thermal conductive paths from heat source to sink also is not new. The combination of the two techniques is rather novel and appears to operate admirably.

Mr. Giesecke, in "Motor Design for Fans and Blowers," airs out an aspect of the cooling problem, too often left to the end of a system layout. And, in a comprehensive analysis, Mr. Hathaway discusses four basic design approaches employing air as a cooling medium. His "Designing Cooling Systems for Airborne Electronic Equipment" is directed toward a situation where overcooling is almost as serious a problem as undercooling, involving, as it does, enormous penalties for excess weight. In addition to these stories, *Electronic Design* is presenting a special section in this issue, devoted exclusively to cooling electronic equipment.—GR *(Electronic Design, Oct. 15, 1957, p. 4)*

Much of this Editorial, written by George Rostky, applies equally well today. Thermal design still is often underestimated until it's too late.—SS

Now Back To ICBM

What this country needs is not a good five cent cigar, but rather an eraser key on the typewriter. This is the opinion of the man who has just given up trying to invent it. George Alton, National Administrator of Sales for Clary Corp., manufacturer of business machines, says modern science has solved practically everything except the costliest mistake in American business, the time lost in erasing mistakes on the typewriter. Alton's almost perfect eraser key, the one he has just given up trying to finish, contained a special chemical that erased mistakes perfectly, but had this one defect: By the time the letter reached the addressee, the acid left on the paper had eaten a million small holes in the correspondence. *(Electronic Design, Oct. 15, 1957, p. 13)*

Fortunately, with computer-based word-processing, the days of dealing with hard-copy typewriter mistakes are far behind us, and everything we do on these 200-MHz Windows 95 beauties turns out prefect.—SS

BACK TO SCHOOL

Tektronix Inc. is announcing its sponsorship of a free technical seminar series focusing on emerging video and telecommunications technologies. The series is designed to help design and test engineers in the telecommunications, cable TV, and video industries better understand broadband, video, and wireless systems. Attendees can choose two of four half-day topics offered in the one-day seminar. Session topics include "Digital Theory and Measurements," a course covering various digital television topics from MPEG-2 compression to evaluating video performance; "RF Measurements for Digital Cellular and PCS," a seminar offering techniques for design and manufacturing test of RF components, as well as digital cellular and PCS mobile and base station transmitters and receivers; "Breakthrough Debugging Techniques for Modern Digital," an overview of measurement techniques for debugging bus timing errors, multiple processor designs, and mixed-signal interactions; and "Physical Layer Measurement of Communications Signals," a discussion of telecom and data standards. The seminars will be held in various locations throughout North America through November. Contact Tektronix Inc. at (800) 763-3133 or on the Internet at http://www.tek.com/mbd/w5021.

Designing Multimedia for Maximum Interactivity is designed to help attendees learn design techniques for developing truly interactive learning applications. Discussion topics include "The Importance of Interactivity in Multimedia," "The Three Levels of Interactivity," "Using Development Models and Templates," and "Determining the Benefits of Interactivity." The seminar will be held on Nov. 17-18 at the J.W. Marriott in Atlanta, Ga., and on Dec. 4-5 at the Loews Santa Monica Beach Hotel, Los Angeles, Calif. Seminar fee is $795 which includes all materials, instructions, and refreshments. For more information, contact Influent Technical Seminars, 498 Concord St., Framingham, MA 01702-2357; (888) 333-9088; fax (508) 872-1153; Internet: http://www.influent.com.

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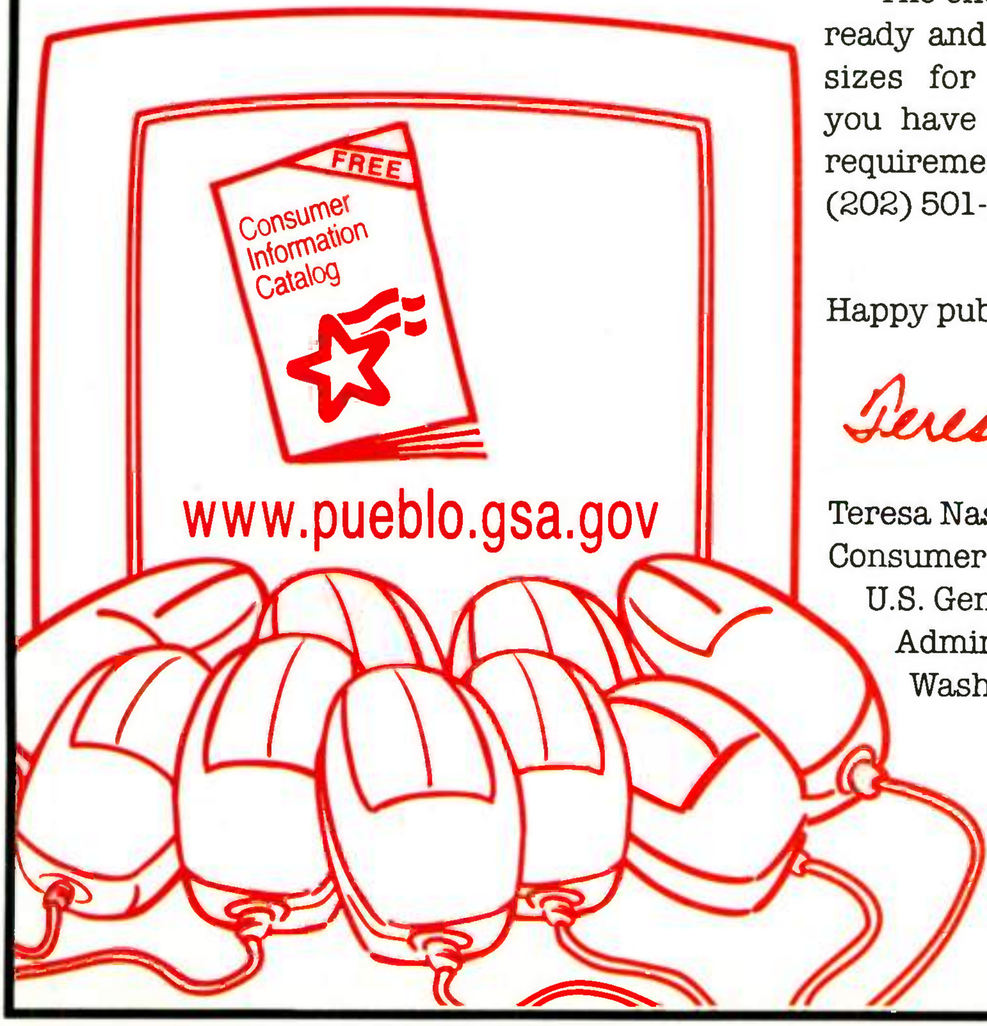

The enclosed ads are camera ready and come in a variety of sizes for easy placement. If you have any special printing requirements, please call me at (202) 501-1794.

Happy publishing!

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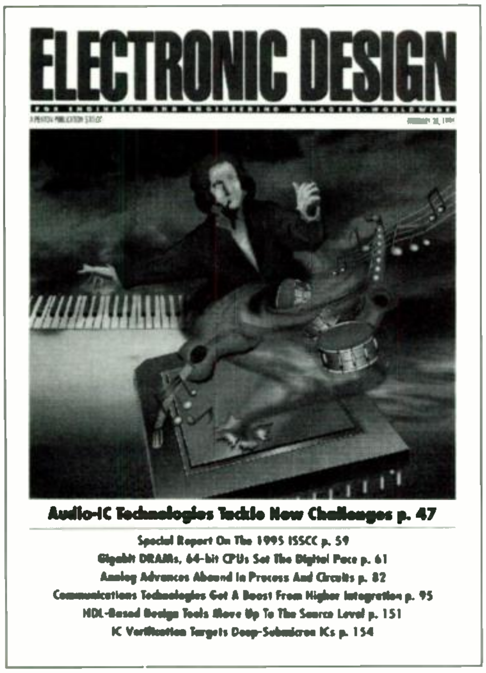
STRATEGIC PARTNERS WORKING TOGETHER

Information has always been a part of the developmental strategy needed for success in the OEM market. In today's fast-paced, competitive global market environment, technology information has become a priority. Systems designers not only want to know what their strategic supply partners are doing today, but where they're going. Designers and suppliers must now work in tandem to align enabling technology with the customer's system requirements. These strategies demand strong partnerships in the development of competitive products.



A third strategic partner completes this alliance. This partner's mission is to observe and report today's product availability by its editorial staff of respected experts, while constantly probing for the next generation of enabling technology. The constant flow of exclusive and vital information helps to bring systems designers and suppliers together as strategic partners. It also provides engineers and engineering managers with an enhanced ability to bring more competitive products to market, faster.

Electronic Design is that strategic information partner — a partner who provides the information that helps the systems designer make those critical decisions that stay the course of the technology road map.

Your Strategic Information Partner.

ELECTRONIC DESIGN

A · PENTON · PUBLICATION

THIS JUST IN...

Tektronix Inc. has announced an agreement to purchase Siemens Communications Test Equipment GmbH (SCTE), a wholly-owned subsidiary of Siemens, Berlin, Germany. The deal was ratified on Sept. 30.

The purchase was expected to help strengthen Tektronix' position in the communications test market. SCTE is recognized as a worldwide leader in the wide-area network protocol analyzer market. As a result of the agreement, SCTE will have the ability to leverage Tektronix' worldwide distribution channels in geographic markets where the Siemens unit previously had little presence.

According to Dan Terpack, president of Tektronix' Measurement Business Division, "Joining forces with SCTE accomplishes several things at once for us. Most immediately, it extends our telecom test offering, and also gives us a very strong position to serve the test needs that are being created by the growth of the Internet."

Claude Balleyguier, president of Textronix' European Operations, said that the union will give his company a strong position in the European communications test market. In addition, the acquisition adds a European development capability in measurement for Tektronix. "These are critical steps in our efforts to build a more global company," said Balleyguier.

Other terms of the agreement are that SCTE's 230 Berlin-based employees are expected to join Tektronix. In addition, approximately 15 employees based in Stockholm, Sweden, and most of its sales force are expected to join. Another major part of the agreement is that Tektronix will take a one-time charge of $15 to $20 million in the second quarter of fiscal 1998 to write-off research and development projects currently underway at SCTE.

Terpack added that "the combination of our strong position in measurement products for digital signals, our expanded strength in communications test, and our expert knowledge of video places us in an excellent position to serve customers who are facing the challenges of converging technologies.—**MS**

TRUDEL TO FORM

JOHN D. TRUDEL
CONTRIBUTING EDITOR

We've been speaking of the Patent Wars--again. I hope that my efforts have triggered enough alarm bells to do some good, as the sell out of our patent system is a major threat to future prosperity and good jobs.

Please write Congress and ask that they block H.R. 400 and S. 507. Tell them that these bills are lethal. As employees, ask that your firm turn the patent sell-out issue over to its CTO or VP of Engineering. It is irresponsible for management to delegate this crucial issue to patent lawyers or lobbyists.

I have gotten much reader feedback. One sent a note explaining the "true" meaning of NAFTA—No American Factories Taking Applications. Another sent excerpts from *Uncertainty of Law and Constitutional Government* by James N. Constant.

It says that the attacks on the Patent System are an example of the "breakdown of the 5th Amendment's right not to have property taken without just compensation." It also notes that the initial attacks on our patent rights came not from the Japanese, but from our own government's agencies and contractors who wanted to use patents for free to serve the national interest.

Apparently there has been a trend in both civil and criminal law to soften the rules for seizure and intrusion. As in Robin Hood's England, bureaucrats can now legally confiscate and sell property. In the Information Age, the most valuable property is knowledge.

Saving our Constitutional Right (article 1, section 8) to own innovations is a worthy cause for engineers. In the end, it's your fight or your loss. If you are so interested, I will keep patent wars updates on my web page.

Enough about patents. Let's move on and speak of innovation. Long ago a smart, wealthy friend, one of my first consulting clients, helped me learn about entrepreneurship. He had started several successful technology firms. He sold the firm I helped him start, became bored, and took a consulting assignment to license a new refrigeration technology.

His engagement failed. No one was building anything. They were downsizing, cutting costs, and sourcing compressors from Japan. That was the end for him. He told me it was time to leave high tech. He bailed out, started a candy company, and has done well.

Years passed. Apple and IBM faded. Bell Labs stopped basic research. Lay-offs and Dilbert-type management became universal. I watched high-innovation organizations that took years to build destroyed in hours. It made me wonder, "Who was right?"

I just examined the Copeland division of Emerson Electric. They invested, invented, patented, and efficiently produced a unique product line. It quickly captured world leadership in refrigeration and air conditioning compressors. Copeland's compliant scroll compressors have higher efficiency, lower noise, better reliability, and half the parts count. Now people, including the Japanese, source from them. Business is great!

It turns out, largely unnoticed, that some people are finally catching on. *You cannot downsize your way to leadership. Business innovation can drive sustainable prosperity.* In industries ranging from paper goods to electronics, small clusters of leaders (6.2% to 8.3% of firms) are using innovation to sustain growth rates in excess of 100% per year.

Maybe we were both right.

John D. Trudel, CMC, provides business innovation consulting to selected clients. Lectures, keynotes, and workshops also are available. He is the author of "High Tech with Low Risk." The Trudel Group, 33470 Chinook Pl., Scappoose, OR 97056; (503) 638-8644; fax (503) 543-6361; e-mail: jtrudel@gstis.net; Internet: http://www.trudelgroup.com.

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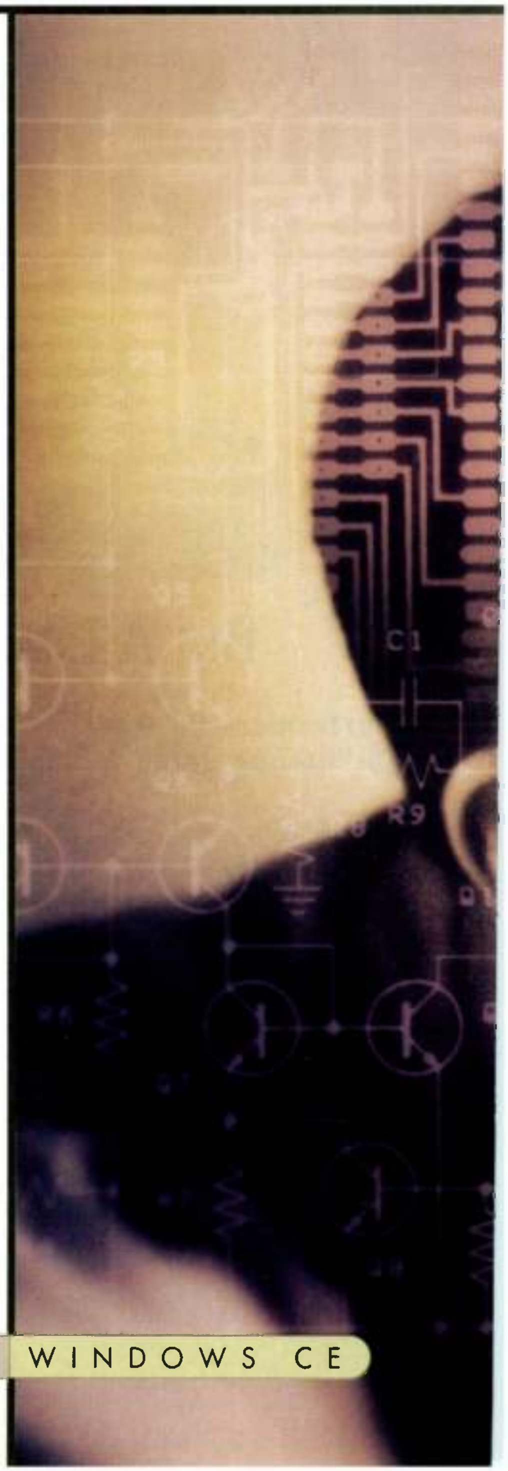

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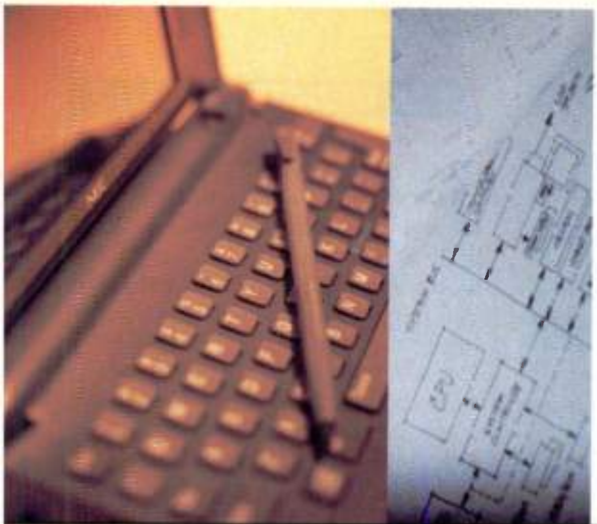

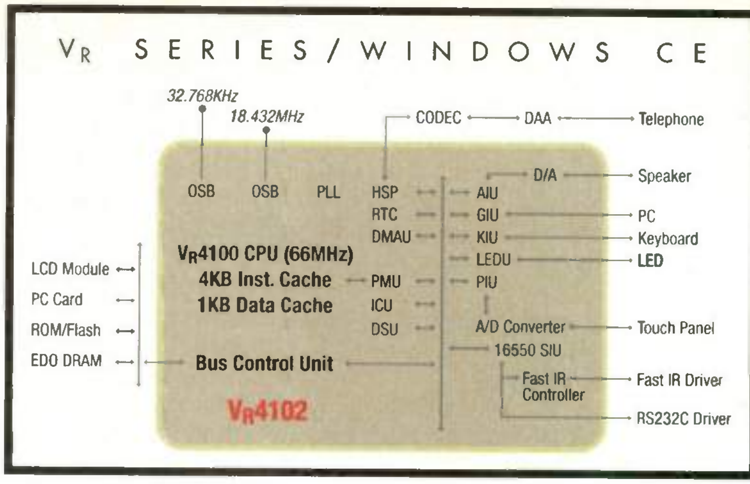

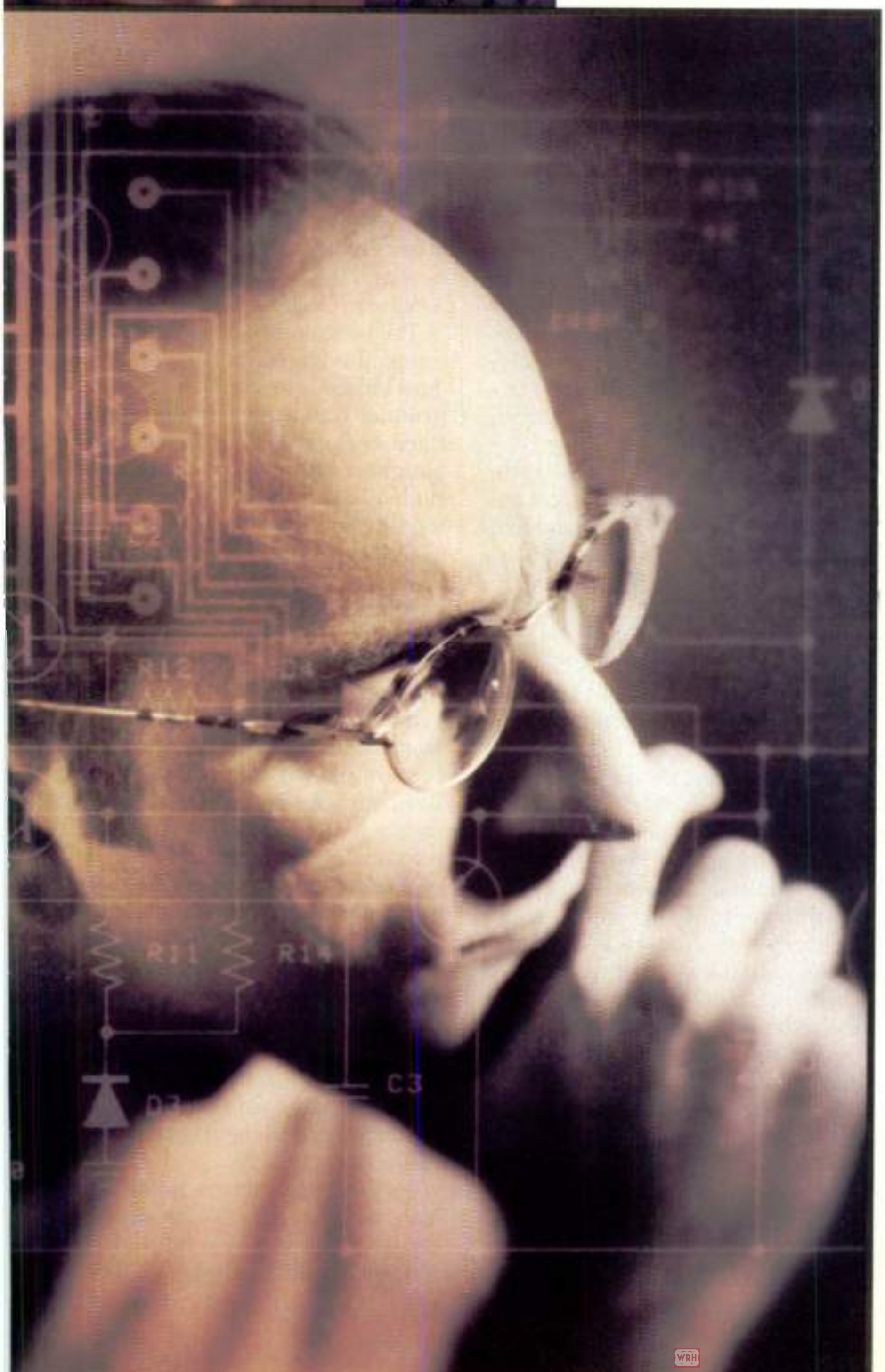

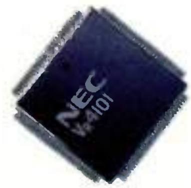

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READER SERVICE 168

Prescriptions By Telephone

It used to be that if you moved out West, especially to the states surrounding the Rocky Mountains, you had to come to the realization that for all the wide-open space, modern conveniences, such as health centers, might not be as accessible as they are in the Big City.

Of course, that fact has changed with the increased migration of people to the region over the past few years, and some of the country's finest medical centers are located in the Mountain West. However, there are many areas in the region where pharmacies and pharmacists are not available. Enter the telepharmacy.

The University of Utah Hospitals & Clinics and Automated Drug Dispensing Systems Inc. (ADDS) have combined computer and communications technology to enable hospital pharmacists to receive and process prescriptions from remote health centers; to counsel patents via interactive video link; to deliver the medications from a stocked dispenser at the health center; and to ensure that the drug dispensed is the one that was ordered.

"This system enables one hospital-based pharmacist to serve clinics and patients throughout the region," said James Jorgenson, M.S. R.Ph., director of Pharmacy at University Hospital. "Given that our service center covers parts of six states, the potential for telepharmacy is practically unlimited."

The system recently went on-line between University Hospital and its Summit Health Center in Park City, Utah, about 26 miles away. The hospital has health centers throughout the state, each of which is a candidate for telepharmacy hookup.

The system works by the health center first faxing the prescription to the hospital, where the pharmacist enters it into the computer. The computer signals the stocked automatic dispensing machine at the health center to release a bottle of the medication. A nurse or medical assistant scans the bar code on the bottle, ensuring that it is the correct medication in the right dose, and then the pharmacist and the patient talk via an interactive video link.

The system also produces a drug monograph or detailed description of the drug with all the information the patient needs with each prescription. The dispensing machine contains supplies of 40 different drugs. The computer program, developed by ADDS, checks the prescription for potential problems such as side effects, interactions, duplication, and contraindications.

Jorgenson says that telepharmacy is important in this part of the country because there are many remote sites where pharmaceuticals and the services of a pharmacist are needed.

Brian Hart, president of ADDS, estimates that the volumes required to support the system are just 20% to 25% of those needed to support conventional pharmacies.

Television monitors at the hospital and health center are linked by a high-speed ISDN telephone connection carrying both video and voice signals, allowing pharmacists and patients to chat as if they were across the counter from each other.

Studies have shown that patients like the system because they get answers to their questions, and are much more likely to comply completely with a doctor's instructions.

University Hospital and ADDS collaborated in developing the system; Utah was the test site. University Hospital is now looking to install the system at its other health centers throughout the state.

"One pharmacist can telecommute to many locations on an as-needed basis, dramatically reducing the need for brick-and-mortar facilities," said Hart. The system can be used in doctors' offices, hospital emergency rooms, nursing homes, assisted living quarters, homeless shelters, and prisons, as well as satellite and rural clinics.

For more information, contact James Jorgenson, M.S., Rh.P., director of Pharmacy, University of Utah Hospitals and Clinics at (801) 585-2189, or ADDS, 85 Rangeway Rd., N. Billerica, MA 01862; (508) 670-0746; fax (508) 670-7250; Internet: http://www.addsinc.com.—**MS**

Y2K UPDATE

Just in case you happen to be a Doubting Thomas or Tina, and you don't believe that the Year 2000 Date Change problem (Y2K) won't have any affect on your life, you might want to read on. According to a story by the *Detroit Free Press*, a fruit and vegetable store in Warren, Ill. is among the first to sue a computer company because its "product is unable to comprehend the year 2000." The complete details to the story can be found at *http://www.freep.com/*.

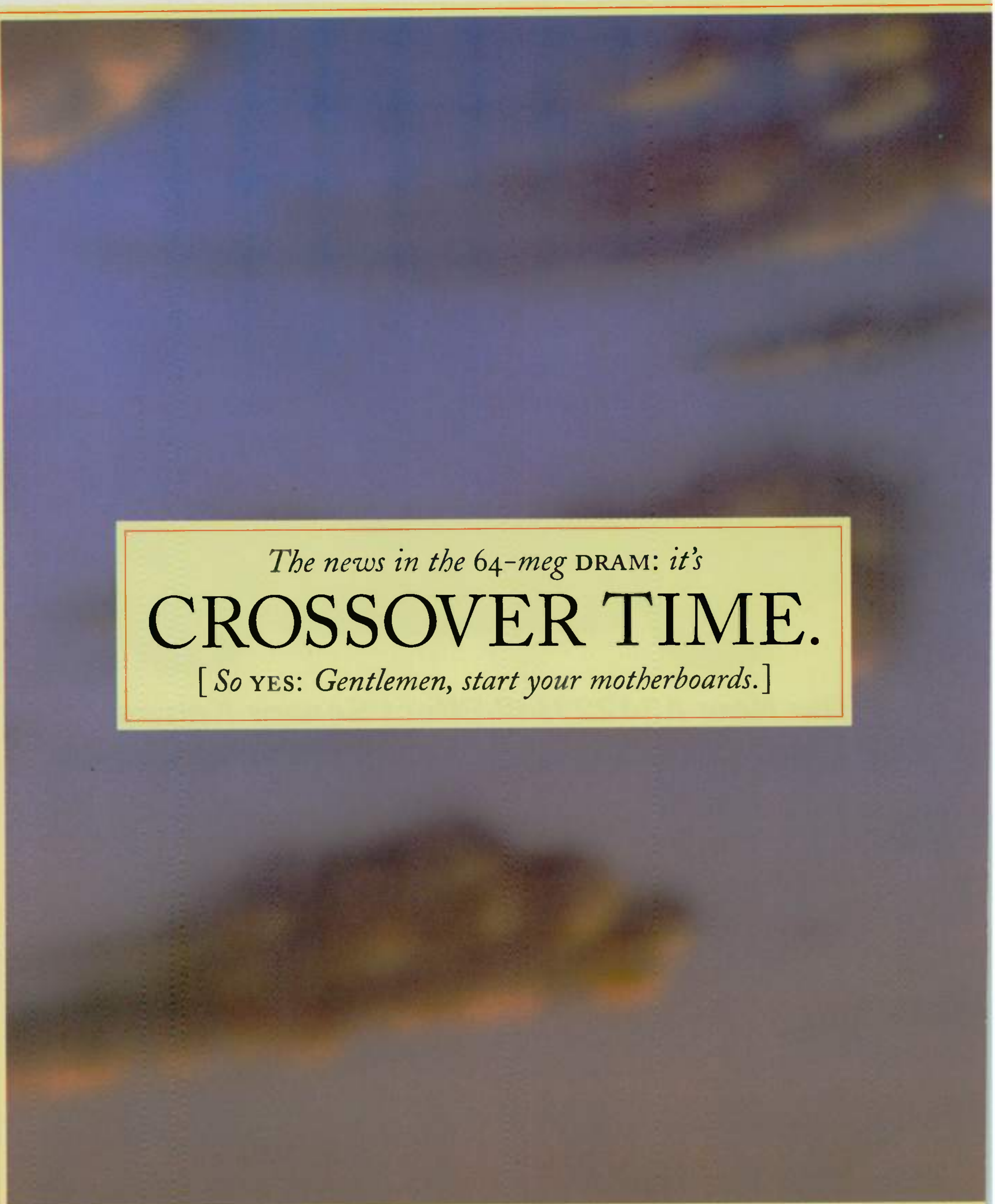
The core of the problem was that the store's registers would crash every time the salesperson would swipe a card that had a 2000 expiration date. The store, Produce Palace International, is seeking at least $10,000, plus legal fees, damages, and other costs. The defendants in the case are Tec-America Corp. and All American Cash Register.

The basis of the suit is that the two companies knew that they sold Produce Palace International a defective product that they couldn't repair. Back in April 1995, Produce Palace bought a $100,000 system that included 10 registers. These machines were designed to deal with inventory as well as regular purchases.

But, not long after the fruit and vegetable dealer bought the system, workers noticed that the system failed to process some charges and the scanner intermittently failed. A year later, however, things got much worse. During their busiest times, the system would crash for four or five hours. All because certain credit cards expired at the end of the century.

According to one of the store's owners, Mark Yarsike, their system failed 105 times between April 30, 1996 and May 6, 1997. The store worked around the problem by doing the transaction by hand, first confirming that the customer actually had the credit in his or her account. When the store closed, the manager would change all the triggering expiration dates to 1999.

Estimated damages, according to Yarsike top hundreds of thousands of dollars in lost revenue and over $50,000 in additional wages.—**DS**



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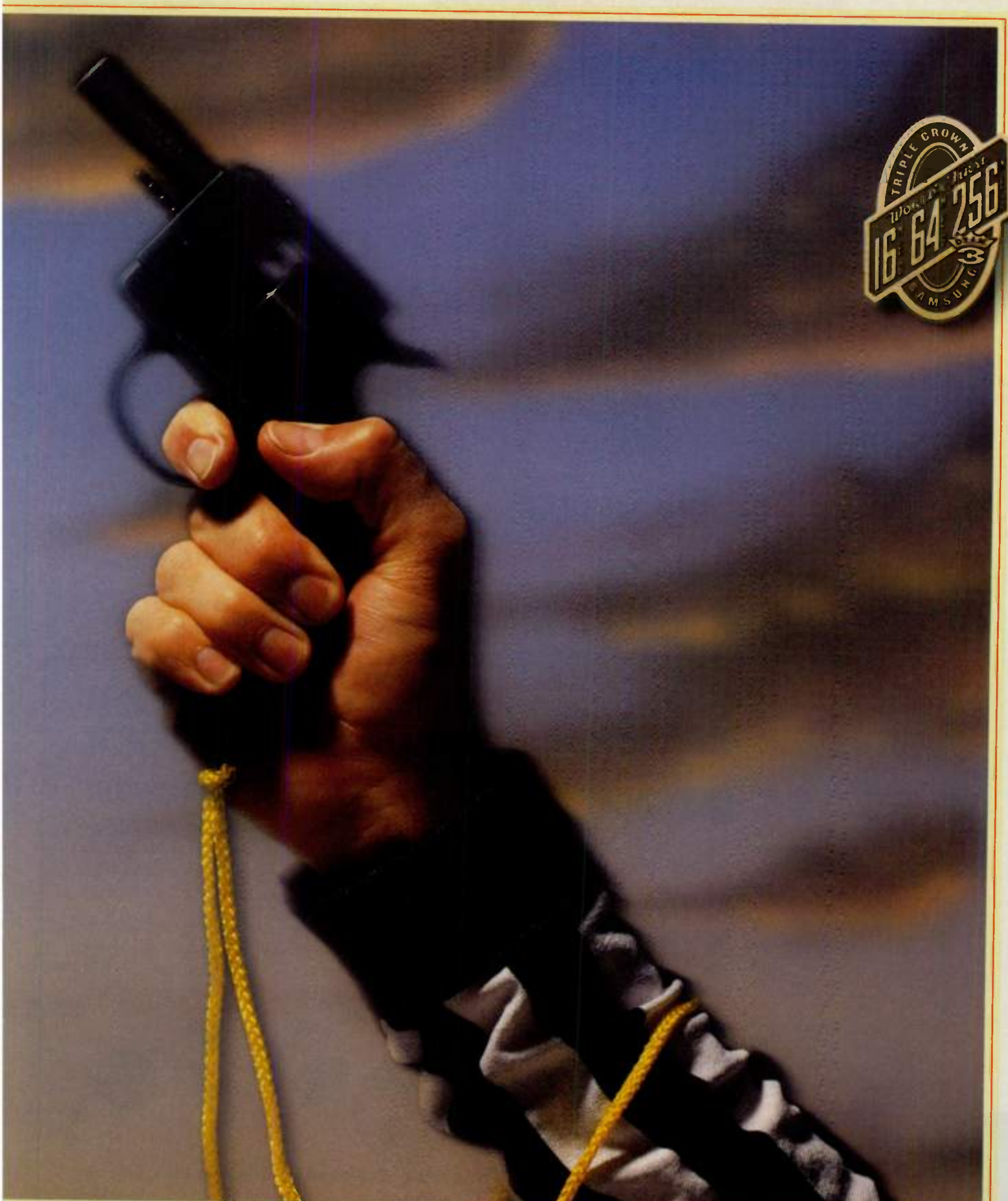

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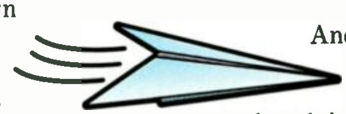
JUST A REMINDER

For those of you who may have forgotten, or simply didn't page through this section in the September 15 issue, the First Annual QuickLook Paper Airplane Contest is underway. We're looking for your submissions, hoping that you'll stun us with your design technique. Remember, the deadline for entries is January 1, 1998.



Just a quick review of the contest guidelines:

• All paper airplanes must be made of (what else?) paper. No balsa wood, thin plastics, or metal sheeting.

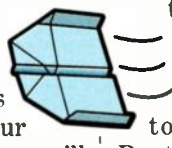
• Designers may use paperclips and/or glue. Be sensible about it, though, **the object of the contest** is to see how many working electronics you can pile onto the plane and still have it work.

• Only fully assembled planes will be allowed to participate in the contest. We don't want to take the fall for any faulty planes because we may not have put the thing together the way you would have done.

• No wingspans larger than 3 ft. If I can't carry it, it's not flying here.

And, because Bob Pease advised that there may be some smart aleck cheatin' types out there, a paper airplane is NOT a sheet of paper wrapped around a transistor radio with the instruction, "Toss Me" tagged on it with a yellow sticky note. But, we do accept airplanes with motors. Personally, I'd like to see a few of those.

The core of the contest is the creative use of electronics. If you can wow the editors of *Electronic Design* with your innovative bit of flying fancy, you'll win. Remember, it's got to be able to fly for at least 12 feet.



Now, our sponsor, 1-800-BATTERIES, has graciously put up 100

1-800-Batteries

lithium batteries for the sake of powering some of the electronics on your planes. The first 100 people to send me a self-addressed, stamped envelope (SASE) will receive one of these batteries. They've also been kind enough to furnish the prizes: first prize is a $150 gift certificate and second prize is a $50 gift certificate, both to be used with 1-800-BATTERIES' catalog.

Send your battery requests and SASE to QuickLook Editors, *Electronic Design*, 611 Route 46 West, Hasbrouck Heights, NJ 07604. Happy flying!—**DS**

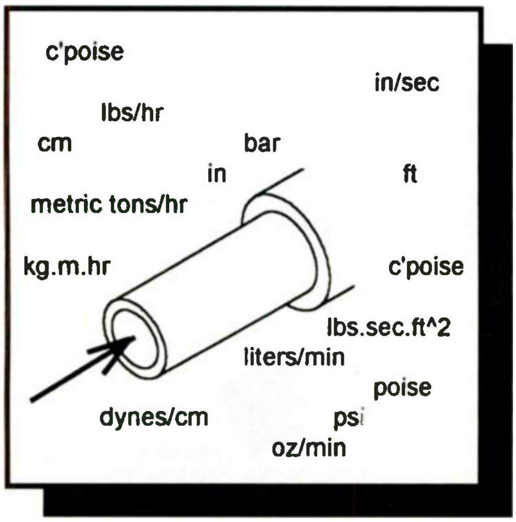
New FLUIDTOOLS with elbows and valves solves pipe and tube flow problems on your PC

Wouldn't it be nice if you could solve flow problems without having to look up all of your data? With FLUIDTOOLS, you can do just that? It's easy as A-B-C.

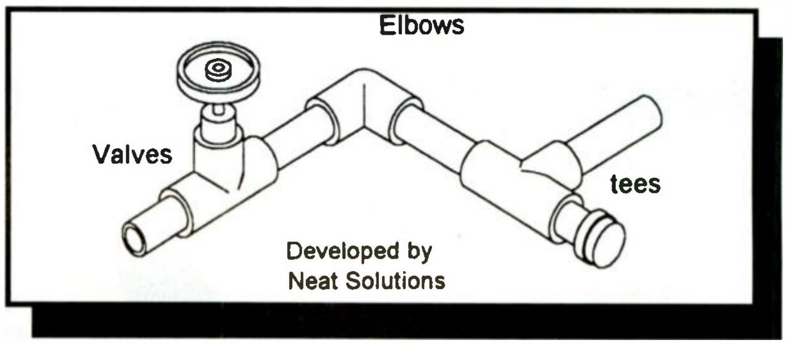
- **Just enter your data in whatever units you wish . . .**
- **Request FLUIDTOOLS to return answers in the units you want . . .**
- **Press "calculate" . . .**

It's that simple!

Program accepts mixed units



FLUIDTOOLS solves liquid and gas flow problems including escaping gas problems. It can solve for diameter, length, flow rate, pressure, or viscosity when doing liquids. Gas problems solve for quantity and DPSI.



Some of the important Features of FLUIDTOOLS . . .

Automatic unit conversion . . . enter data in mixed units and FLUIDTOOLS automatically calculates in the units you want • Friction and expanding gas factors are automatically calculated • All factors can be overridden • Program data base includes elbows, valves, fittings, viscosity, specific gravity and pipe sizes •A wide range of common and uncommon metric and English conversion factors are included and are easily expandable to accept user-defined data • Menus for pipe roughness are provided, or you can key in your own • Program can save all user defined data. All tables can be edited and expanded using the special editor included.

FLUIDTOOLS program disk and user manual $295

System Requirements:

IBM PC line of computers or 100% compatibles
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1394.

August 1995
Sony releases the 1394 camcorder with TI silicon

December 1995
TI is instrumental in the first IEEE specification

July 1996
Another first: TI's software team develops the LYNXSOFT Software V1.0

April 1994
After receiving the "Most Significant Technology" award at Fall COMDEX '93 for its 1394 serial bus, TI releases the first PHY and LINK silicon to market

November 1995
TI forms the first 1394 software development team

June 1996
TI ships the first and only backplane PHY and also introduces a broad range of designer kits

MIXED SIGNAL

QUICKNEWS

Hooray For HollyNet—GTE recently concluded testing of a prototype secure network targeted for the exchange of digital voice, video, and data within the entertainment production community. The tests involved the HollyNet Initiative and GTE's InfoGuard 100. InfoGuard 100 is a commercially available asynchronous transfer mode (ATM) cell encryptor. The testing was successful in that the network security specialists were unable to breach the network or intercept the transmissions.

During the prototype testing, uncompressed video files and a video teleconference that featured whiteboard information was sent from Warner Bros.' studios in Burbank, Calif., to a simulated digital effects studio located in Carson, Calif. Before the test files left the Burbank studios, they were encrypted with InfoGuard 100. Networking specialists from the University of Southern California were assigned to intercept the data from within HollyNet. At the same time, another team of network security specialists from Trident Data Systems tried to break into the network and access the data. Both teams failed and the Carson studio received their information intact. The studio was able to decrypt the information without a hitch.

HollyNet, the high-speed, wide-area network, is designed to connect the computer systems and networks of movie and TV production companies. The network uses ATM technology to send data, video, and voice through the companies at speeds of up to 622 Mbits/s. Currently, the project only extends to the Los Angeles County border. Plans are to expand HollyNet globally, however.

The project is virtually certain to succeed with such major names as Lucasfilm, MCA/Universal, Sony Pictures, Viacom/Paramount, Warner Bros., and the Entertainment Technology Center supporting it. In addition, network security work was performed by the Entertainment Technology Center, Digital Equipment, Fore Systems, GTE, Pacific Bell, Trident Data Systems, TRW, and the University of Southern California.

For more information, contact GTE, 77 A St., Needham Heights, MA 02194-2892; (617) 455-5180; Internet: http://www.gte.com.

How Much For Your Disks?—Bringing solid-state disks into the mainstream, Quantum Corp. has dropped its prices on the entire family of ESP 3000 and ESP 5000 solid-state disks. The company's intent is to compete directly against add-on memory and added caches. The price reductions represent a 10% to 40% decrease.

The lower prices reflect the sinking prices of DRAMs. DRAM is the primary component in a solid-state disk. By avoiding add-on memory and other caches, and using solid-state disks instead, users will be able to use the disks as large caches in Internet/intranet and video applications. Developers of Windows NT systems also will be encouraged to take advantage of the lower prices.

The disks feature access speeds about 30 times faster than those of magnetic media, and have experienced an increase (a doubling, actually) in their I/O speeds to over 5000 requests per second. If a user decides to make a solid-state disk a cache for a disk array, his or her performance can be improved by as much as 60%.

These disks use a single connector attachment, SCA-2, to directly connect to an array without cables. The line is available in volatile and nonvolatile variations. They range from 134 to 804 Mbytes in a 3.5-in. form factor, to 905 Mbytes in a 5.25-in. form factor. In the nonvolatile drives, users will gain an integrated data retention system. This data retention system protects the data in case of a power failure. The volatile systems do not carry this protection.

The solid-state disk drives are priced starting at under $7500.

For more information, contact Quantum Corporation, 500 McCarthy Blvd., Milipitas, CA 95035; (408) 894-4000; Internet: http://www.quantum.com.

Four Heads Are Better Than One—Three giant communications companies and one large communications developer have teamed to define a common Wireless Application Protocol. The object of the protocol is to bring Internet content and advanced applications to digital mobile phones. The companies intend on making the new protocol the standard for a single-protocol application environment.

The end users will be able to manage personal telephone profiles; handle voice, fax, and e-mail messaging; take advantage of information services (transportation, restaurants, hotels, stock trading, banking, directories, etc.); use Internet services; and interface more easily with advanced telephony.

The Wireless Application Protocol will be based on the Handheld Device Markup Language (HDML), the Handheld Device Transport Protocol (HDTP) (developed by Unwired Planet), Smart Messaging (from Nokia), and the Intelligent Terminal Transfer Protocol (ITTP) (from Ericsson). The protocol will be license-free and independent of the airlink standard.

For more information, contact Motorola, 1501 W. Shure Dr., Arlington Heights, IL 60004; (847) 632-5000; fax (847) 632-5834; Internet: http://www.mot.com.

CEOs Need People Skills—A recent study by Christian & Timbers, an executive search firm, says that boards of directors tend to hire CEOs on their skills and experience, but will fire them based on their personality and interpersonal communication skills (or lack thereof). The survey of 40 board members said that the respondents tend to base their hiring decisions solely on the candidates' track records, rather than on their personal fit with the company. This mismatch leads to more firings than any other reason. Actions and attitudes such as being too hard on people, lacking a vision, and lacking interest also were high on the list.

For more information, contact Christian & Timbers, One Corporate Exchange, 25825 Science Park Dr., Suite 400, Cleveland, OH 44122; (216) 464-8710; fax (216) 464-6160; Internet: http://www.ctnet.com.

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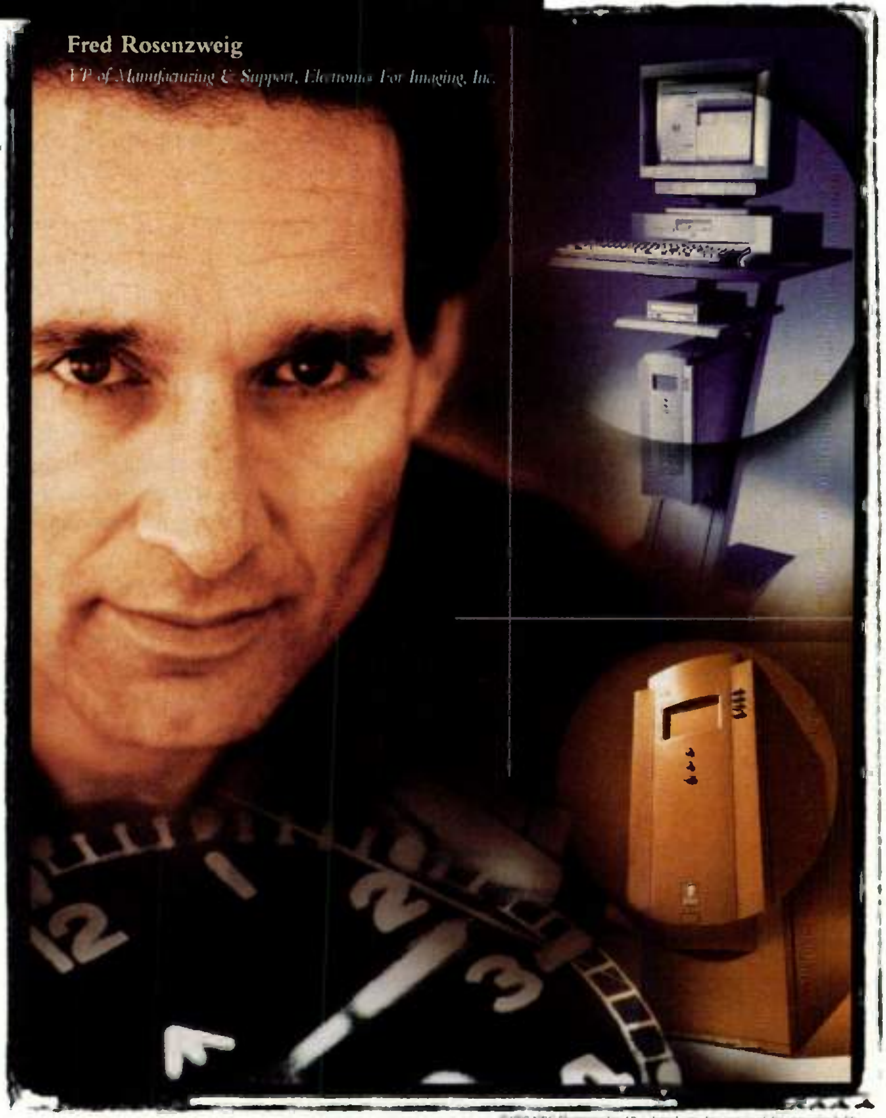

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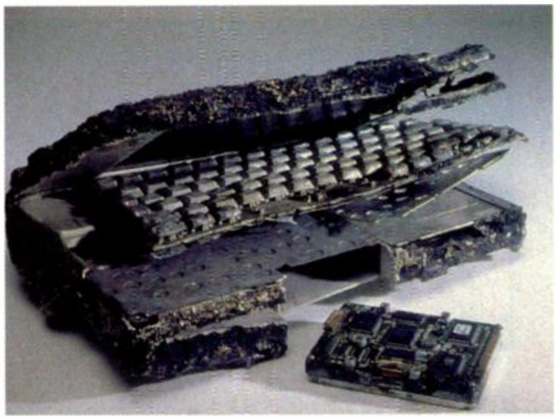
Flooded Hard Drive? Sounds Like A Job For DriveSavers!



It's happened to all of us at one time or another—the crashed drive. But how many of us have drowned our laptops with coffee or soda? Even more distressing, try running over a $6000 Toshiba notebook with a Harley Davidson motorcycle. In that case,you'll have to call DriveSavers directly.

DriveSavers is the data recovery service that the players use when all seems lost, especially for those reports that have to be on the CEO's desk by 5:00 p.m. Typical drive manufacturers and removable cartridge manufacturers who have turned to DriveSavers in their darkest hours include Conner, Epson, Fujitsu, Iomega, Maxtor, Panasonic, Sony, StreamLogic, and SyQuest.

But the company doesn't just handle the big names. It also offers services to individuals and government agencies. DriveSavers rescues data by developing proprietary techniques with these major drive producers. By using these techniques, the company can dive in where most people have backed off.

Don't deep six your computer if it's been damaged by earthquakes, water, fire, or other disasters. In fact, don't give up on your data if your system suffers from stiction, bad actuators, damaged motors, controllers, or control tracks, either. The DriveSavers clean-room facility is fully equipped to deal with these traumatic events.

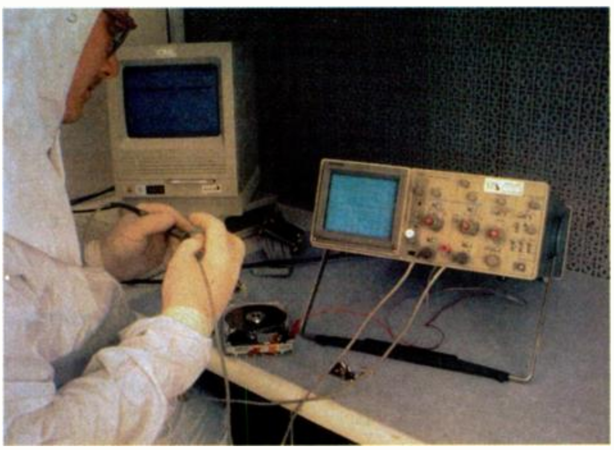
For a small number of the company's recovery work, the drive must be completely dismantled, cleaned, then reassembled so that the read-write heads are in exactly the same position they were in when the failure occurred. This process requires the clean room to prevent dust particles from damaging the hardware components further. As a result of the company's using a clean room to work on mechanical problems that cannot be solved externally, most manufacturers will honor warranties on drives that have been recovered by DriveSavers.

What's more impressive is that DriveSavers data-recovery service runs 24 hours a day. And, according to the company, its recovery rate is 95%. The 24-hour service is enjoyed by customers who send their damaged storage media or laptops to DriveSavers' offices for data recovery. The company also will provide an immediate estimate of recovery charges over the phone before any damaged materials are sent out.

Depending on the amount of work required and backup time involved, DriveSavers can ship recovered data back to the customer on the day it was received. This service goes for severely damaged data as well as software problems such as directory corruption. Directory corruption could be a result of conflicting software, electrical problems, or power surges.

The company's list of satisfied customers is impressive. Major companies whose data have been successfully retrieved include Adobe Systems, American Express, Arthur Andersen & Co., Ben and Jerry's, Eastman Kodak, MGM, Motorola, and Xerox.

A new policy recently enacted by DriveSavers is to rescue data from desktop and notebook computers at no charge for victims of the Grand Forks, N.D. flood. Many of the flood's victims had computers that were totalled out by floods or fires caused by downed electrical lines. Now these hardy survivors have a fee-free friend in DriveSavers. If the company could save data from a Powerbook that sank to the bottom of the Amazon, they could certainly help computers that sat underwater for weeks during the flooding.



Web surfers with data recovery issues can turn to DriveSavers' web site at *http://www.drivesavers.com* for free data recovery information and tips for Macintoshes and PCs. Additionally,, there's stories about "disk-asters," job opportunities, "TEN Good Reasons to Choose DriveSavers," links, Media Coverage, customer testimonials, and contact information. One of the famous testimonials is from a scriptwriter of "The Simpsons" television program who would have lost an entire season's worth of episodes had it not been for DriveSavers. Check out the site for the long list of DriveSavers fans.

For more information, contact DriveSavers, 400 Bel Marin Keys Blvd., Novato, CA 94949; (415) 382-2000; fax (415) 883-0780.

DESIGN NOTES

New 16-Bit, 100ksps A/D Converter Runs on 5V Supply

Design Note 165

Sammy Lum and Kevin R. Hoskins

The LTC®1605 is a new 16-bit, 100ksps ADC from Linear Technology. Its outstanding DC accuracy and ±10V analog input range are ideal for industrial control and instrumentation applications. Its simple I/O, low power and high performance make it easy to design into applications requiring wide dynamic range and high resolution.

Product Features

- No missing codes and ±2LSB max INL over temperature
- Single 5V supply with 55mW typical power dissipation
- ±10V analog input with ±20V overvoltage protection for harsh environments
- Complete ADC contains sample-and-hold and reference
- 28-pin PDIP, SO and SSOP packages

Circuit Description

The LTC1605 converts ±10V analog input signals while operating on a 5V supply. A resistor network is used to attenuate the input signal. This reduced internal signal is digitized by a differential, switched-capacitor, 16-bit SAR ADC at a rate of up to 100ksps. The differential architecture provides high immunity to power supply and other external noise sources. The trimmed 2.5V bandgap reference can be overdriven with an external reference if desired.

The digital interface is simple. Conversions are started using the read-convert (R/$\overline{C}$) pin. Data is available as a 16-bit word or two 8-bit bytes.

AC and DC Performance

Figure 2 shows the fast Fourier transform (FFT) of a ±10V 1kHz sine wave signal digitized at 100ksps by the LTC1605. The LTC1605 achieves a signal-to-noise and distortion (SINAD) of 87.5dB and very low total harmonic distortion (THD) of –101.7dB.

Figure 3 shows an INL error plot for the LTC1605. Guaranteed specifications include ±2.0LSB INL (max) and no missing codes at 16 bits over the industrial temperature range (–40°C to 85°C). The ADC's outstanding accuracy is

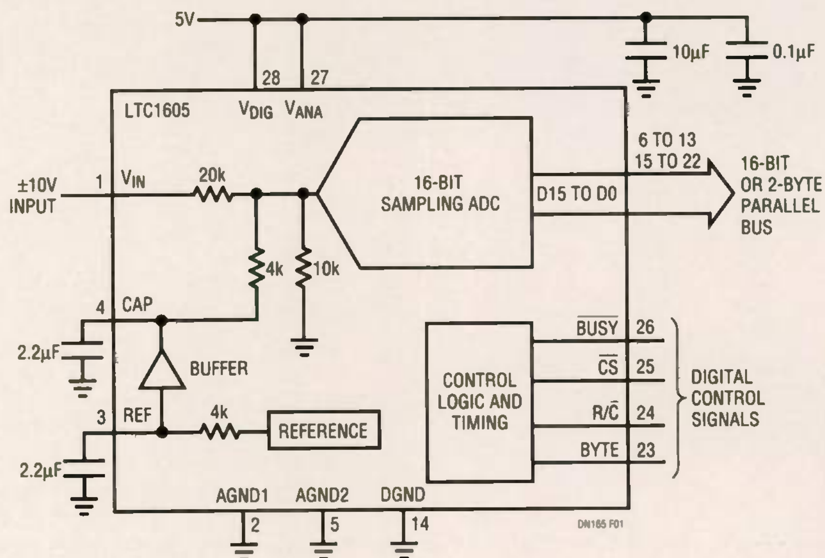


Figure 1. Offering 16-Bit Performance, the LTC1605 Handles ±10V Inputs While Operating on a Single 5V Supply

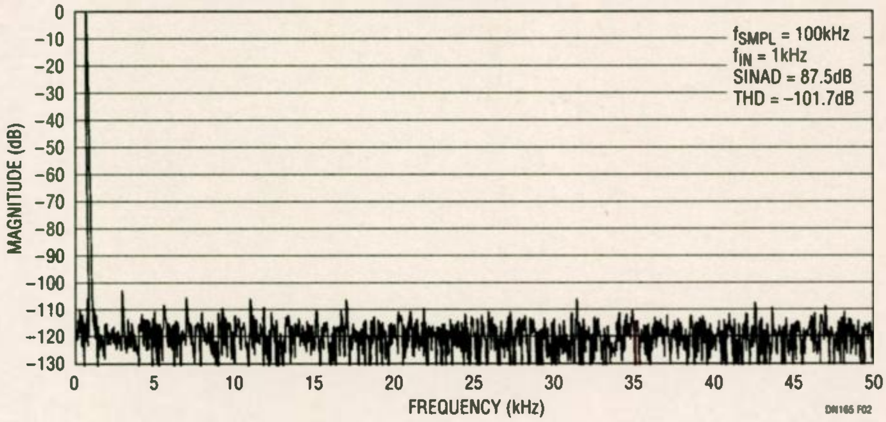


Figure 2. The LTC1605's AC Performance Achieves a 87.5dB SINAD and −101.7dB THD

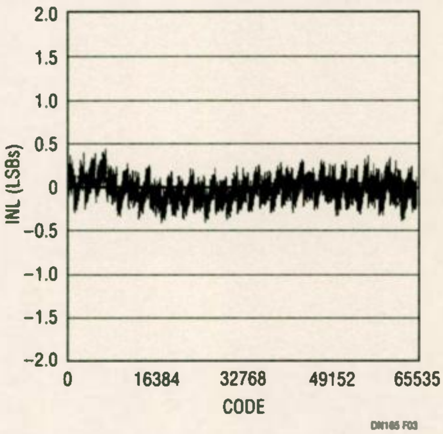


Figure 3. The LTC1605 Achieves Excellent INL Without Cumbersome Autocalibration

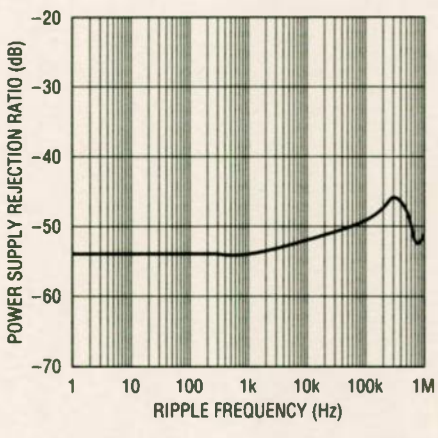


Figure 4. The LTC1605's Differential Architecture Provides Good, Wideband Supply Rejection

assured by factory trimming. For the user, this eliminates the software overhead and calibration time delays associated with autocalibrated ADCs.

One of the benefits of the LTC1605's differential architecture is its high power supply rejection ratio (PSRR). Figure 4 shows the power supply rejection ratio of the LTC1605 as a function of frequency.

High PSRR is important to the LTC1605's conversion accuracy and signal-to-noise performance because, at 16-bit quantization, the LSB magnitude is just 305μV (V_{IN} = $20V_{P-P}$). The LTC1605's high PSRR rejects up to 100mV of power supply noise to below an LSB level.

Applications

With its overvoltage protected ±10V analog input, the LTC1605 fits easily into industrial process control, power management, data acquisition boards and has sufficient speed for multiplexed applications. The LTC1605 is also ideal for wide-dynamic-range applications that use a PGA and lower resolution ADC. For example, the LTC1605 is a simpler solution and will out perform (in terms of DNL, INL and S/N) a 12-bit ADC converting the output of a PGA with a gain range of 1-to-16.

Conclusion

The LTC1605 is a complete 16-bit ADC with a built-in sample-and-hold and reference. Its wide analog input range, overvoltage protection and DC accuracy make it a good candidate for industrial process control, instrumentation and other high dynamic range applications.

For literature on our A/D Converters, call **1-800-4-LINEAR**. For applications help, call (408) 432-1900, Ext. 2453

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STANDARDS WATCH

Mobile NCs Must Get More Intelligent

Richard Nass

The just-released Mobile Network Computer Reference Specification (MNCRS) is intended to make mobile NCs "smarter," giving users access to their data at almost any time, from almost any place. The basic idea is to have almost no local storage in the platform, with the bulk of the storage residing either on a LAN server or with an Internet Service Provider (ISP). The standard will determine how mobile computer screens should look, its power requirements, the method of linking them with networks, and the types of peripheral devices that they support.

The MNCRS was founded by an industry consortium consisting of Apple Computer, Fujitsu, Hitachi, IBM, Lotus Development, Mitsubishi Electric, Netscape Communications, Nokia Mobile Phones, Oracle's Network Computer, Sun Microsystems, and Toshiba. Since the announcement, endorsement of the specification has come from Digital Equipment, Funai Electric, Hugh Symons (U.K.), the Institute for Information Industry (Taiwan), Japan Telecom, Matsushita Electric Industrial, NEC, PeopleSoft, Psion, Secom Information of Tokyo, Telxon, Thomson CSF, and Tokyo Internet.

The types of platforms outlined in the specification include mobile NCs, "smart" cellular phones, and lightweight, handheld mobile devices. There are two commonalities between all the compliant devices. First, they must offer easy access to the Internet or corporate networks. The second is that they must be based on the Java operating system, either running Java natively or in emulation, and either as the only resident operating system or running on top of another operating system, such as Windows 95 or Windows CE.

Java gives software developers a common reference platform on which to write their applications. As a result, the software developers can concentrate on the applications themselves, rather than worry about dealing with the APIs from the different operating systems.

The MNCRS specification identifies three classes of computing devices. The first, called the professional assistant, can support rich Java content with various productivity applications. While handling many of the same functions as a subnotebook computer, it's important to note the this class of device is not intended to replace the subnotebook.

The second type of mobile NC will have less functionality than the professional assistant and will focus primarily on being an information- and Internet-access device. This will mandate Web browsing and basic e-mail support. While support will be included for Java applets, they will be limited in scope (performance and memory consumption). This device will resemble today's PDAs.

The third device class will be a basic messaging, paging, telephony device with the goal of keeping the mobile professional in touch with the office. Limited browser support is required.

The professional assistant would weigh under 2 lbs., have a battery life of 12 to 15 hours, have no rotating media (the storage will be about 30 to 40 Mbytes of flash memory), and will measure about 7 by 9 in. (smaller than a laptop). The bulk of the mobile NC storage would be handled by the ISP, including file storage. Local memory will hold the BIOS, the operating system, and some key applications.

The display size would be capable of showing VGA resolution, including graphics (color is optional). But the display itself would be smaller than a typical laptop's display. The specification calls for a half VGA display with 2 bits/pixel for the professional assistant (320 by 240 pixels). For other classes, the requirement for screen size is fairly flexible. The reason for the half-VGA spec is so the software vendors know what the smallest possible display they would be writing applications for. The supported graphics formats are standard GIF and JPEG. The new MPEG-4 standard, which offers a video compression capability for videoconferencing, can also be employed.

The specification outlines three communication modes. It's important to ensure that the system can distinguish between the three modes and intelligently transition between them.

The full connectivity mode is for when the system is connected over a high-speed attachment such as a LAN or WAN at the rate of several megabits per second. This allows the system to download and install a completely a new version of an application or even a flash update to the operating system.

The low-speed attachment (limited-connectivity) mode is for when the system is connected over a lower speed medium, such as an analog modem or a wireless system at the rate of several kilobits per second. Here, data is selectively downloaded.

Lastly, the off-line mode is used when the system is disconnected with local access only. In this mode, the device will only work with data or applications stored internally.

The Problem With Buses

There are five basic computer architectures out there in Technology Land, with a number of variations on a theme. They break down into circuit-switched (buses and fat trees) or packet-switched models (rings, cubes, and Clos switches). Each topography has some advantages, but their utilization is mostly limited by their particular "aberrant behaviors."

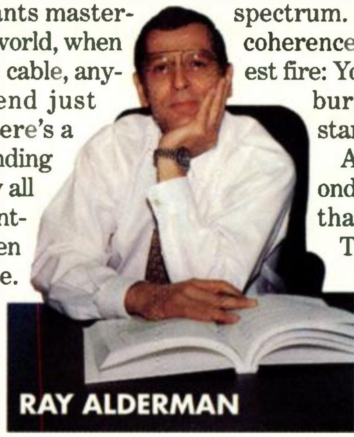
Buses are the most-used circuit-switched architectures in computers today. A bus-based topography is typically made up of a number of nodes (boards or chips) multidropped on a common, shared resource, the bus itself. The bus is divided into functional blocks, like the data-address bus, the control administration bus, the interrupt bus, the arbitration bus, and the power-ground distribution system.

One thing buses do well is overlap the administrative system latencies with the data bus, with the exception of some synchronous bus-functions (clock-based protocols) that are found in buses like PCI. Asynchronous buses like VME tend to be more efficient at overlapping latencies because the protocols aren't tied to one clock line. An example of this latency-reducing technique is the interrupt and arbitration subsystems. While data moves between nodes on the bus, the interrupts and arbitration cycles occur simultaneously, allowing maximum utilization of the shared data path. But that's where the problems begin.

The primary aberrant behavior of a bus is "blocking latency." If a node wants to use the data bus that's already in use, then that node is "blocked." To gain mastership, the node must use the arbitration subsystem and win mastership. If it doesn't attain mastership, it remains blocked and must continue to re-arbitrate.

This blocking behavior creates some pesky problems for computer architects, but it could be worse. The design philosophy of a bus is "make the node who wants mastership suffer, not all the other nodes in the system."

Ethernet CSMA/CD (Carrier Sense Multiple Access/Collision Detect) has the opposite philosophy—"make everyone who wants mastership suffer when any one node wants mastership." In the Ethernet world, when there's no traffic on the cable, anyone who wants to send just jumps out there. If there's a data collision, all the sending nodes detect it and they all back off and start a countdown register that's been loaded with some value. The first node to reach zero gets the cable. After that transaction, everyone collides again, and we go through the same process. This creates a lot of "dead time" on the data bus. About 70% of the bandwidth is spent banging heads in the CSMA/CD arbitration process.


RAY ALDERMAN

What can we do about blocking latency? One small help is cache-coherency. The reason so many nodes need the bus is because they either need data from another place, or they need to put data back where they got it. A coherency system works with "snooping" (reading all addresses coming down the bus to see it you're interested) and "snarfing" (grabbing data from a transaction between two other nodes as it comes by). It's a lot like eavesdropping on conversations, but it reduces the number of blocking incidents on the bus.

Cache coherence is an application- and transaction-mix-dependent solution to blocking latency. There are hundreds of graphs predicting the performance increases you're supposed to enjoy if you use it, but you never seem to get on or above the power curve. Transaction mixes (reads, writes, interrupts, etc) are a dynamic phenomenon, resembling a statistical model more than static curves on a graph, and this makes cache coherence more like snake oil than anything else. On top of that, all cache models have a "knee in the curve" where, when another node is added to the system, overall performance drops significantly. That's why you don't see many six-processor servers. Cache coherence is a latency-management technique, and it works along a small section of the computing spectrum. At the high-end, cache coherence is like managing a forest fire: You just sit back and let it burn itself out. Then, you start over.

All buses have other secondary aberrant behaviors that reduce performance. These are connection (address cycle) and disconnection latency (the "getting off the bus" cycle). This is inherent to all circuit-switched architectures no matter what topography is employed. You can speed up the clocks on synchronous buses or the state machines on asynchronous buses, but the ratio of connection and disconnection latency to data latency remains the same for a fixed-size data transfer.

Why are buses the most-used architecture in computers? Because they're cheap. Each node only needs one interface chip hooked to the bus, but a lot of functions (I/O, memory, processors, etc) can talk to the bus through that one, cheap interface. Secondly, most of today's applications can live with the latencies induced by the circuit-switched model. But as applications become more sophisticated and data-dependent (like signal processing, multiprocessor servers, or real-time video), any shared resource like the bus becomes a problem.

The high-end of the spectrum is where all the other topographies come from, and one day, buses will simply be an era of computer history. What will replace buses in future architectures? On the desktop, we're seeing USB and Firewire. In servers, routers, and other multiprocessing systems, we see crossbar switches. In massively-parallel systems, we see cubes, meshes, and Clos networks.

We're learning that there is no universal architecture any longer. Some applications run better on one architecture than another. So, expect a divergence in how computers are designed in the future.

Ray Alderman is the Executive Director of VITA. He can be reached at exec@vita.com.

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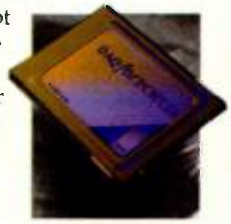

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DESIGN APPLICATION

Ultra2 SCSI Adds Performance, But Requires Extra Design Effort

New Parameters And Design Challenges Can Be Met By Taking Advantage Of LVD Signaling Technology.

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More than 15 years ago, the small-computer system interface (SCSI) provided the amazing data-transfer speed of 1.5 Mbytes/s. Design specifications and practices for hardware were fairly straight forward, not requiring any unusual board design tricks or tools. Since then, the standard has gone through many revisions and upgrades. In 1996, SCSI took a leap forward into Ultra2 SCSI, featuring low-voltage differential (LVD) SCSI signaling. Data rates jumped to 80 Mbytes/s, bringing a host of new design challenges and parameters to deal with at the board design level. To ensure a solid Ultra2 SCSI product design that meets the product users' needs, new design elements have entered into the equation. These include capacitance, skew, and impedance control budgets, along with the modeling of high-speed signals on the board.

After a thorough reading of the SCSI specification, the first step of the basic SCSI design is to pick an SCSI chip that contains a PCI interface. Next, choose a board material and thickness. For our example design, we'll use FR-4 (ε_r= 4.8 microstrip, ε_r= 4.3 stripline) with a 0.062-in. board thickness. Lastly, pick the trace/space dimensions and the copper plating. For Fast and Ultra SE (single-ended) SCSI, use an impedance of around 90 Ω ± 8 Ω. For Fast and Ultra Differential SCSI, the signal trace impedance should be 110 Ω to 135 Ω. Copper platting will be specified as 0.5 oz., plated up to 1 oz. on the outside and 1 oz. inside (t ~ 1.35 mil, 0.5 oz. T ~ 0.7 mil).

The following equations cover impedance calculations for slow-speed microstrip and stripline signals in an SE design.

$$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right) \qquad (1)$$

where Z = trace impedance, ε_r = die-electric constant, h = prepreg height (thickness of board layer), w = trace width, and t = thickness of trace.

Equation 2 (for a stripline single trace) is

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln\left(\frac{4b}{0.67\pi(0.8w + t)}\right) \qquad (2)$$

where b = height between planes (all other variables remain consistent throughout this article).

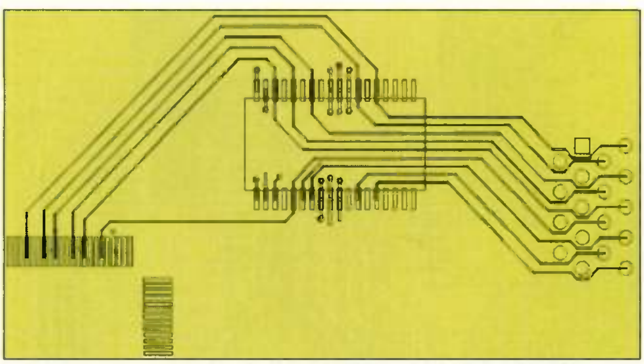
At the speeds that Fast and Ultra SE SCSI run, we aren't too concerned about the Co, Lo, and Vp because good basic design practices will generally cover any issues. For a differential design for slow speed signals, the microstrip impedance is

$$Z_{DIFF} \approx 2 \times Z_0\left(1 - 0.48e^{-96\frac{s}{h}}\right) \qquad (3)$$

and the stripline impedance is

$$Z_{DIFF} \approx 2 \times Z_0\left(1 - 0.347e^{-2.9\frac{s}{b}}\right) \qquad (4)$$

Generally, a trace/space of six and six works well using the microstrip design and the right thickness of prepreg and ε_r. These can be selected using equations 1 and 2 for SE SCSI and 1, 2, 3, and 4 for differential SCSI.



1. In a connector route for single-ended Ultra SCSI, there should be no tees or stubs. The trace lengths should all be very close to balance the signal skew.

Routing Practices

Now let's move on to the routing practices used in SCSI signal lines. SCSI signal routing generally falls into two categories: single- or multiple-connector boards. Single-connector boards are fairly straightforward. Routing from the pins on the chip to the active terminators on the board to the connector is all that's needed. Very simple rules apply here: no t's, stubs, or right angles *(Fig. 1)*. Passive terminators aren't a consideration because Plug-n-Play SCSI doesn't allow them. And, with the current prices for active terminators, a few pennies buys excellent signal quality. Lastly, according to the specification, Ultra SCSI requires active termination.

Multiple-connector SCSI boards can be challenging, depending on whether all the connectors are the same size (8- or 16-bit SCSI, or a mix of 8 and 16 bits). Generally, it's not a good idea to mix connector sizes on differential SCSI buses. Managing the control- and data-signal assignments between different terminators can be a problem, especially with active termination. If a designer is using passive or discrete active termination on the differential SCSI bus, it can be designed so that the transition from 8 to 16 or 16 to 8 bits will keep the upper 8 bits of the data bus terminated in a two-connector design. A three-connector differential design should be avoided if feed-through terminators aren't going to be used. SE SCSI can be done with two, three, or more connector configurations by grouping the control and data signals in such a way that the upper eight data bits are in a separate terminator. The terminator should be controlled independently for correct termination based on the connector and data-path configuration.

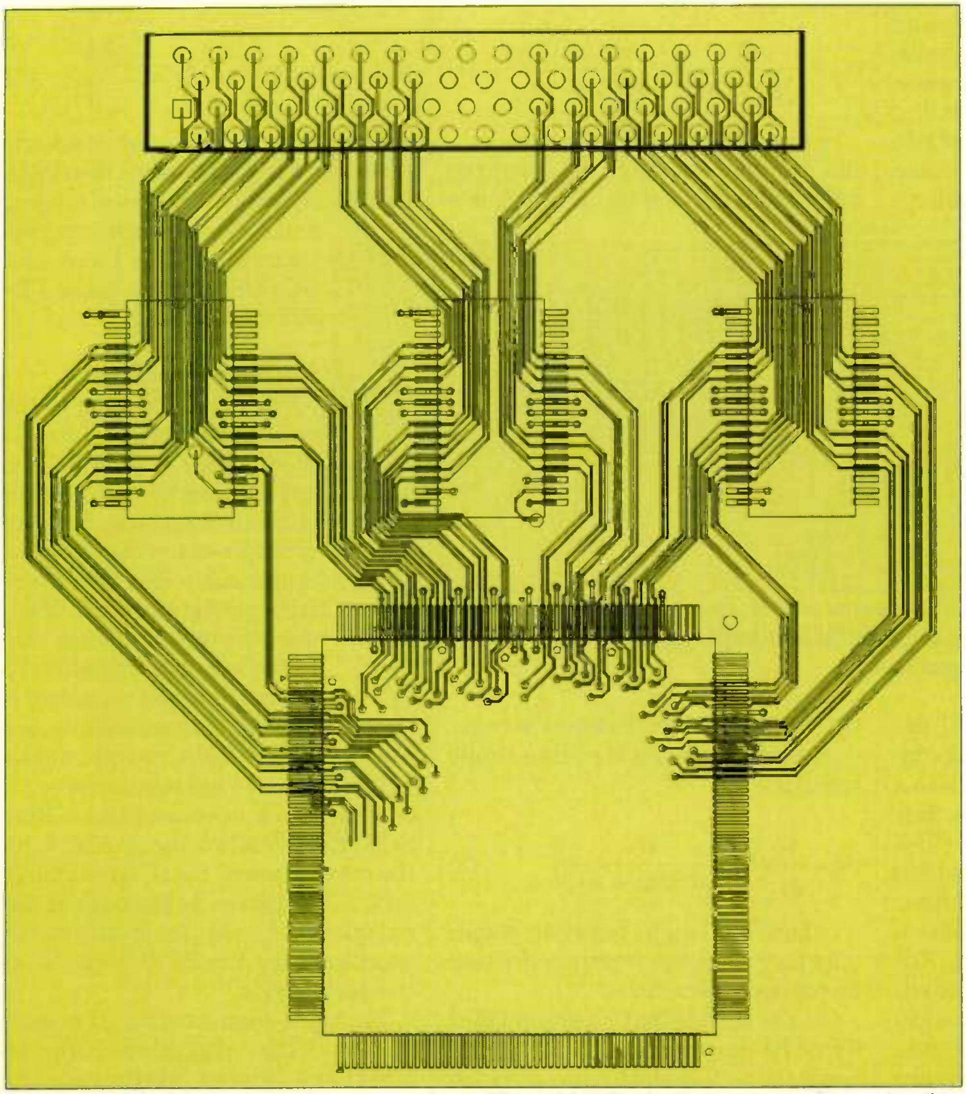
Another element to consider in a Fast, Ultra SE, or differential SCSI board is the use of autotermination configuration circuits. These are circuits that configure the active terminators based on how many and what type of cables are plugged into a board to correctly terminate the SCSI bus.

Ultra2 SCSI is based on low-voltage differential technology (LVD) standards and design practices. One question that must be answered before starting on an Ultra2 SCSI design is whether or not it will be a universal SCSI design. If it will be a universal SCSI design, it will do either SE or LVD SCSI (called multimode). If the board is to be an Ultra2 SCSI design using only LVD terminators, many of the necessary design practices fall into standard high-speed differential signal design practices.

As with any SCSI design, basic choices must be made at the onset, beginning with the SCSI controller chip. The following example employs an Ultra2 LVD/SE SCSI chip with a PCI interface. The chosen board material and thickness is FR-4 (ε_r = 4.7 microstrip, ε_r = 4.3 stripline) and 0.062 in. Lastly, for the trace/space dimensions along with the copper plating, we'll specify 0.5-oz. copper plated, up to 1 oz. on the outside and 1-oz. copper inside (t~1.35 mil, 0.5 oz. T~ .7 mil). For Fast and Ultra SE SCSI, use an impedance of about 90 Ω ± 8 Ω. For the SE part of the board, this will be the target impedance. For the Ultra2/LVD SCSI part, the signal trace impedance should be between 110 Ω and 135 Ω with a target of 120 Ω ± 8 Ω. One of the major challenges for an LVD/SE design is picking a trace/space specification and a board stack-up that will combine to give an impedance that supports both LVD and SE.

Equations 1 through 4 don't really give valid trace/space and stack-up impedance results with Ultra2 and Ultra SCSI speeds. Nor do they account for odd- and even-mode impedances. A coupled conductor pair can support two modes of propagation due to the electro-magnetic fields surrounding it. These modes have different characteristic impedances. An odd-mode impedance occurs when adjacent conductors are of opposite polarity. Even-mode impedance occurs when the polarity is the same. For LVD, the odd mode is always the one of concern because the polarity of the two lines is always opposite.

To design a board that can run both Ultra/SE and Ultra2/LVD SCSI, equations 5 and 6 need to be solved simultaneously. This task is difficult due to the number of unknowns. A better method is to solve equation 5 for 90 Ω, the impedance needed for single-ended operation. Select a



2. In an example showing the routing of low-voltage differential (LVD) signals to an internal connector, the LVD traces for the external connector can be routed on the opposite side of the board, keeping the via count to a minimum.

height, dielectric constant, and thickness, for the equation, then vary the width. Next, place the values of width and height into equation 6 and adjust the spacing to obtain a value of 60 Ω, which is the impedance for one side of a differential pair (120/2)*(see Equation Listings, below)*.

Based on these equations and good manufacturing practices, the best fit occurred with w = 7 mils, s = 5 mils, and h = 15 mils, with $\varepsilon_r = 4.7$. This results in an SE impedance of 89.8 Ω and a differential impedance of 118.2 Ω (2 ´ 59.9). Further accuracy can be obtained if frequency-dependent impedance equations are used. Compare these results to those gained from simulations using speed-sensitive equations run on an Ultra2/Ultra SE PCI board's design database. Here, the best fit was trace = 5 mil and space = 6 mil with a prepreg height of 12.5 mils, specified for 110 to 135 Ω differential and 90 Ω ± 8 Ω singled-ended. This put the actual measured SE impedance at 82 to 90 Ω and the LVD impedance at 100 to 115 Ω.

The SCSI Bus

Some decisions must now be made for the structure of the SCSI bus. This process mainly involves terminator placement, and selection and placement of connectors. Because the design is to be an Ultra2/Ultra SE SCSI implementation of a host adapter, two connectors are needed, one for external cable connections and one for internal connections. Two connector styles are available—HD (high density) or VHDCI (very-high-density cabled interconnect). For Ultra2, it's suggested that VHDCI connectors be used as their capacitive load is about half that of a 68-pin HD connector (3 pF vs. 6-9 pF per pin connection).

For this example, we'll use a VHDCI for the external connector and a 68-pin HD connector for the internal connector. The HD connector is pre-

Equation Listings

$$Z_0 = \frac{120\pi}{2.0\sqrt{2.0\times\pi}\sqrt{\varepsilon_r+1.0}}\ln\left\{1.0+\frac{4.0h}{w'}\left[\frac{14.0+8.0/\varepsilon_r}{11.0}\times\frac{4.0h}{w'}+\sqrt{\left(\frac{14.0+8.0/\varepsilon_r}{11.0}\right)^2+\left(\frac{4.0h}{w'}\right)^2+\frac{1.0+1.0/\varepsilon_r}{2.0}\times\pi^2}\right]\right\} \qquad (5)$$

where:

$$w' = w+\left(\frac{1.0+1.0/\varepsilon_r}{2.0}\right)\times\frac{t}{\pi}\ln\left\{\frac{4e}{\sqrt{\left(\frac{t}{h}\right)^2+\left(\frac{1/\pi}{w/t+1.1}\right)^2}}\right\}$$

$$Z_{0_{even}} = Z_0\times\frac{\sqrt{\varepsilon_{rf}/\varepsilon_{rf_{even}}}}{1.0-\frac{Z_0Q_4}{120\pi}\sqrt{\varepsilon_{rf}}} \qquad (6)$$

where:

$$Q_1 = 0.8695\left(\frac{w}{h}\right)^{0.194} \qquad Q_2 = 1.0+0.7519\times\frac{s}{h}+0.189\left(\frac{s}{h}\right)^{2.31} \qquad Q_3 = 0.1975+\left[16.6+\left(\frac{8.4h}{s}\right)^{6.0}\right]^{-0.387}+\frac{1}{241}\ln\left[\frac{\left(\frac{s}{h}\right)^{10.0}}{1+\left(\frac{h}{3.4s}\right)^{10.0}}\right]$$

$$Q_4 = 2.0\times\frac{Q_1}{Q_2}\times\frac{1}{\left(\frac{w}{h}\right)^{Q_3}\times e^{\left(\frac{-s}{h}\right)}+\left(2.0-e^{\left(\frac{-s}{h}\right)}\right)\times\frac{w}{h}^{-Q_3}} \qquad \varepsilon_{rf} = \frac{\varepsilon_r+1}{2}+\frac{\varepsilon_r-1}{2}\left[\left(1+\frac{12h}{w}\right)^{-0.5}+0.04\left(1.0-\frac{w}{h}\right)^{2.0}\right]$$

$$\varepsilon_{rf_{even}} = 0.5(\varepsilon_r+1.0)+0.5(\varepsilon_r-1.0)\left[1.0+\frac{10.0}{v}\right]^{-ab} \qquad v = \frac{\frac{w}{h}\left(20.0+\left(\frac{s}{h}\right)^{2.0}\right)}{10.0+\left(\frac{s}{h}\right)^{2.0}}+\frac{s}{h}\times e^{\left(\frac{-s}{h}\right)}$$

$$a = 1.0+\frac{1}{49.0}\ln\left[\frac{v^4+\left(\frac{v}{52.0}\right)^{2.0}}{v^4+0.432}\right]+\frac{1}{18.7}\ln\left[1.0+\left(\frac{v}{18.1}\right)^{3.0}\right] \qquad b = 0.564\left(\frac{\varepsilon_r-0.9}{\varepsilon_r+3.0}\right)^{0.053}$$

ferred for infrastructure-transition purposes because a ribbon cable can be used for SE internal connections. Planar boards, motherboards, and other multifunction boards would need to follow the same rules as the host adapter. If the design is to be a backplane board with multiple connectors, such as in a JBOD (just a bunch of disk) or disk array, some additional considerations would need to be included for connector spacing and stub-length management.

The last consideration is where to place the termination. One choice is to use an external plug-on terminator. However, this could be cumbersome because four different kinds of plug-on terminators would be needed for this board, as well as the knowledge of how and when to install them. In addition, if the configuration changed, the user would have to open up the box to make the changes. Even if the board was designed with two VHDCI connectors, instead of one VHDCI and one HD, the user would still have to open the box if the bus configuration changed. The best solution is to employ active universal LVD/SE terminators directly on the board. The universal terminator can detect if the SCSI bus is in SE, LVD, or HVD (high-voltage differential) mode using the DIFFSENS line. The terminator supplier's documentation should supply the correct method to construct the DIFFSENS circuit. Another advantage of using on-board active termination is that cable-connection sensing circuitry can automatically configure the termination for common cabling situations.

The placement of termination will affect the stub length beyond the terminators when only one connector is in use. Stubs should look like lumped elements instead of transmission-line elements. They should be no longer than one-tenth of the wavelength of the highest frequency component at the board propagation velocity. For Ultra or Ultra2 SCSI, the stub length is limited to 0.1 m (about 4 in.).

After all the calculations are made, the final recommended configuration based on the preceding parameters employs an external VHDCI connector, an Ultra2 SCSI chip, multimode terminators, and an internal 68-pin HD connector. This configuration gives the best support to externally connected Ultra2 devices.

Another area in which designers need to concern themselves is the total input capacitance budget. Looking in from the VHDCI connector, the trace-reference plane capacitance is 1.67 pF/in. and the intertrace capacitance is 0.57 pF/in. (2.24 pF/in. total for the differential pair). If the chip has 12 pF/pin, the terminators have 3 pF/pin and connectors 3 pF/pin, leaving 9 pF or 4.02 in. of trace length for routing the board. Note that vias have not been added yet. Also, the REQ/ACK skew must be controlled within ± 200 ps, with a propagation velocity of 7.32 in./ns, which translates into a maximum length delta of ±1.46 in.

When routing commences, the board layout designer must juggle a list of dos and don'ts. LVD signals have low voltage swings. For LVD SCSI, the swing is generally between 270 and 640 mV. This swing makes LVD signals susceptible to influences from TTL and other signals running in parallel. It's important to keep TTL and other high-voltage digital and analog signals away from LVD traces. One way is route the LVD traces on the outer layers and the other signals on inner layers, if it's a multilayer board. Ground guard traces also can protect the LVD traces.

If the LVD traces start on the chip side of the board, keep them there. Don't via them back and forth from one side of the board to the other. There's a capacitive budget that must be lived within while routing the board, and vias eat up the capacitance budget very quickly.

It's important to follow good EMC design practices: no 90° turns on traces; keep 2X spacing between differential pairs when running the parallel traces, if possible; and route each differential pair together. Most board-layout tools with any sophistication will allow differential routing. Use this feature as it will help maintain data-signal quality and EMI tolerance.

When the LVD signals are routed to an internal connector, the LVD traces for the external connector can be routed on the opposite side of the board *(Fig. 2)*. This design helps keep the via count low. The total trace

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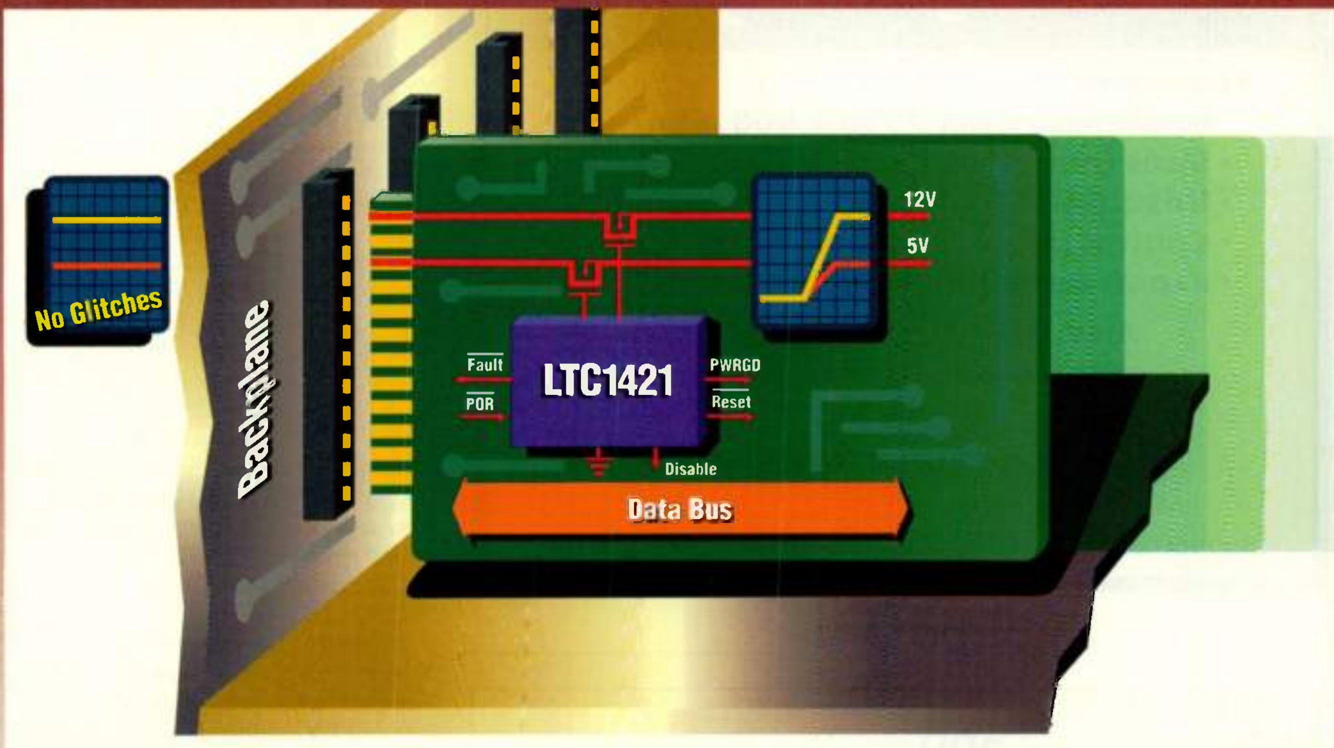

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length from external to internal connector would then measure a little over 7 in., which would give a total capacitive sum of about 35 pF for the complete SCSI bus. This design also will allow for maintaining a REQ/ACK skew of less than ± 1.46 in. or ± 200 ps.

Approved American National Standards can be purchased from ANSI, 11 West 42nd St., 13th Floor, New York, NY 10036; (212) 642-4900 or Global Engineering Documents, 15 Inverness Way East, Englewood, CO 80112-5704; (800) 854-7179 or (303) 792-2181.

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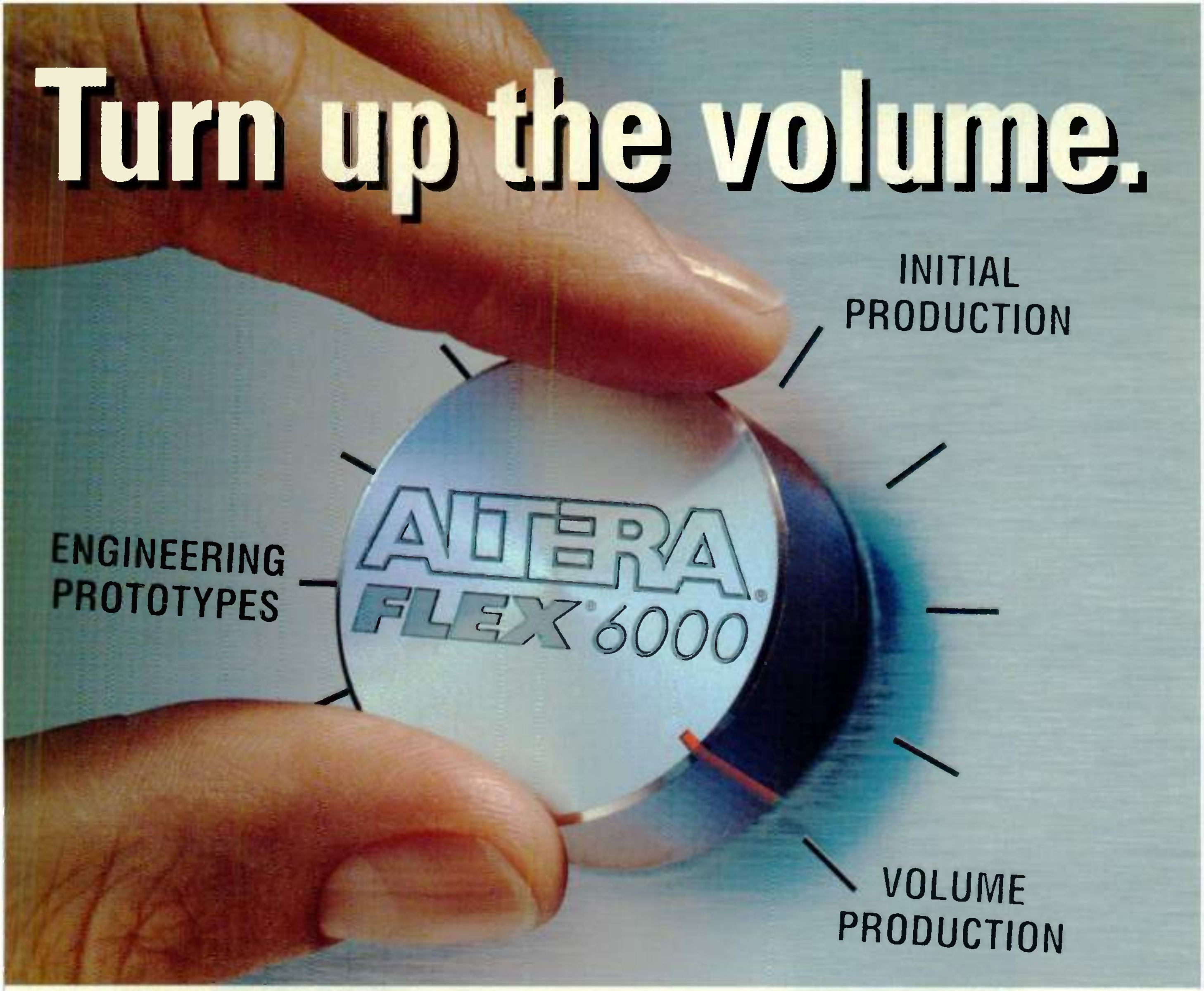

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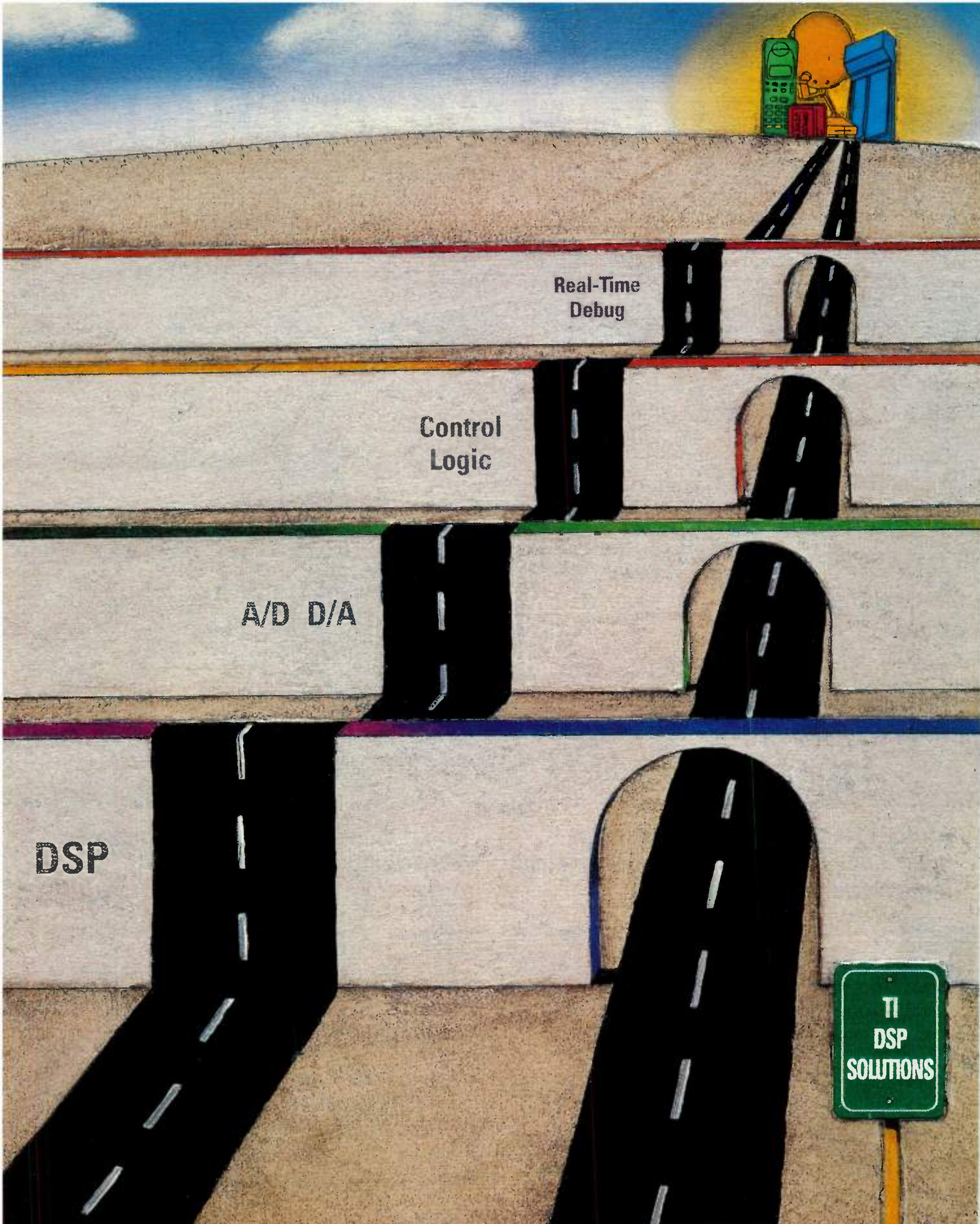

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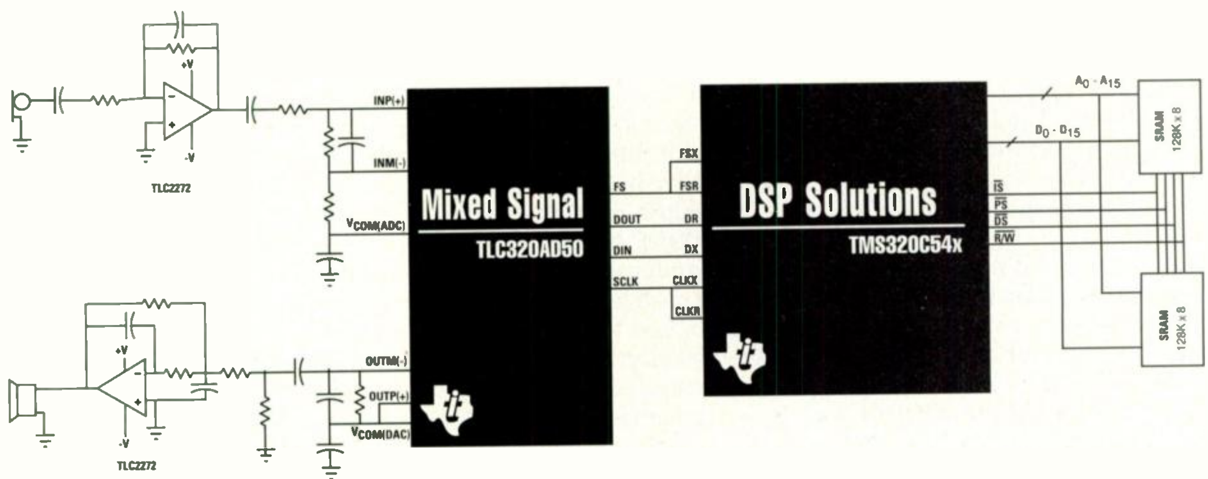

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WHAT'S ON BOARD

Able to deliver graphic performance 50% to 200% better than most other 2D/3D graphics accelerator chips, the Verit 2000 employs a novel RISC-based architecture that includes an on-chip set-up engine and separate pixel-drawing engine. Developed by Rendition Inc., Mountain View, Calif., the V2200 accelerator delivers a 3D WinBench'97 score of greater than 200 and a 2D WinBench score of more than 100. Most accelerators do well in only the 3D or the 2D benchmarks, but not both. The pixel-drawing engine performs per-pixel drawing operations, and includes pixel blending, z-buffering, fog blending, dithering, and specular highlighting. The engine can be controlled by either the internal RISC processor or the triangle engine, and can render a bilinear-filtered, z-buffered, fogged, and blended pixel with both diffused and specular shading in a single cycle. The pixel engine also handles the conversion from YUV color space to RGB color space for video, and the triangle engine offloads triangle launching, thus freeing the RISC engine to set up more asynchronously, rendering any triangle shape or line. That greatly improves overall performance. The chip also includes video capabilities, including a dedicated input port to bring in MPEG 2 or videoconferencing images. In addition, the V2200 supports software DVD implementations by providing hardware support to the MPEG 2 decode process; TV-out also is supported thanks to an internal programmable flicker filter and digital video output port to deliver high-quality NTSC encoded signals. A lower-cost version, the V2100, is targeted at system motherboards. Samples are immediately available. In lots of 10,000 units, the V2200 sells for $30 apiece. Contact the company at (415) 335-5900, or on the Web at http://www.rendition.com.

Able to provide power management functions as well as peripheral control support for Windows CE platforms based on the Hitachi SH-3 RISC CPU, the IT8101 from Integrated Technology Express Inc., Santa Clara, Calif., potentially eliminates the need for custom ASIC and other multichip solutions for CE platforms. The power management logic includes stop-clock capability on each internal support function and two programmable 16-bit timers with prescalers. Support functions included on the IT8101 consist of an LCD controller, a PCMCIA controller, and three communications channels, one of which can be used to implement a 33.6-kbit/s software modem. Another can be used for an IrDA infrared interface, while the last is a UART capable of data rates up to 115.5 kbits/s. An interrupt controller manages requests for service from internal and external peripherals (via the general-purpose I/O bus). The controller can be programmed to assign different levels of priority to each peripheral request and signal the host CPU to indicate which peripheral needs service. The LCD controller provides a resolution of 640 by 240 pixels with from 256 to 64,000 colors or 64 gray scales. It supports an off-chip video memory of 512 kbytes. Samples of the IT8101 are immediately available and sell for $20 apiece in lots of 1000 units. The chip is available in either a 208-lead low-profile QFP or a standard 208-lead PQFP. Contact Edward Chen, (408) 980-8168x230, or on the Web at http://www.iteusa.com.

An enhanced version of the 200-MHz Pentium Pro processor module with 1 Mbyte of level-2 cache has been released by Intel Corp., Santa Clara, Calif.. The larger cache improves the processor efficiency in applications such as on-line transaction processing, data warehousing, and other database-related applications, and allows the CPU to deliver top notch performance in multiprocessor systems. For instance, a four-CPU Hewlett-Packard NetServer LX Pro system was able to break the 10,000 TPC-C benchmark barrier, achieving a price/performance value of just $48.72/tpmC; a Unisys six-way Aquanta HS/6 also set a new record, achieving 12,026 tpmC at a price/performance value of $39.38/tpmC. The Pentium Pro 200-MHz module the 1-Mbyte cache sells for $2675. apiece in 1000-unit lots. Contact Intel at (408) 765-8080 or on the Web at http://www.intel.com.

Power Supply Mounts Directly To VME Backplane

Integrated directly into a 6U VMEbus backplane, the PowerPlane dc-dc power supply eliminates the cables normally required by conventional power supplies by connecting directly to the existing backplane power studs. By employing this approach, designers can save assembly time, space, and cost while improving the dynamic response and load regulation. Because of the space savings that's achieved, a shortened chassis can be employed. By mounting the PowerPlane directly at the load, detrimental voltage drops caused by the inductance and resistance of power cable or bus bars are virtually eliminated. When combined with an ac-dc front end, the PowerPlane supplies 400 to 800 W as well as all the control functions required by a VMEbus chassis. The device can be configured with three or four output voltages.

Tracewell Power Inc., *567 Enterprise Dr., Westerville, OH 43081; (614) 847-9336.* **CIRCLE 554**

UART Improves Performance With Deep FIFO

High performance from a UART is available using the OX16C952. The two-channel part offers data rates up to 3.125 Mbits/s on each channel and 128-byte FIFOs on the transmitters and receivers, thereby reducing the host-CPU overhead. Six modem lines can be operated per channel—four for input and two for output. The chip is software-compatible with standard UARTs, including the 16C450, 550, and 650, and is pin-compatible with the 16C552.

An automated flow control prevents FIFO over run. The FIFO levels are readable to increase performance in poll mode. A programmable baud-rate prescaler allows faster data rates. In addition to a low operating current, the UART offers a power-down mode to further conserve power. The OX16C952 device also is available as a core to be integrated into an ASIC.

Oxford Semiconductor Ltd., *68 Milton Park, Abingdon, Oxon, UK OX14 4RX; (44) 1235 861461; http://www.oxsemi.com.* **CIRCLE 555**

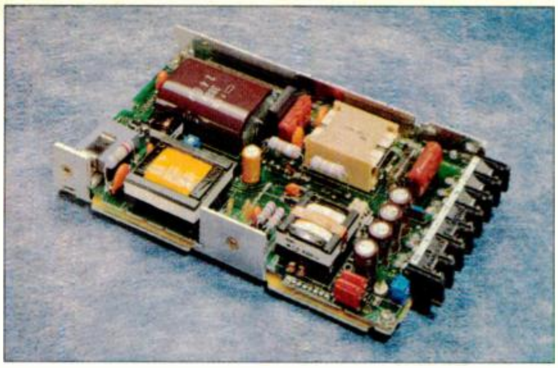
Power Supplies of Distinction from Kepco

Kepco offers three distinctive single output power supply designs in the 15 watt to 1500 watt range. The three designs offer you a range of features to make your designs work better. All models are fully certified to UL/CSA/TÜV EN 60950 LVD.

FAW:

15 watts-150 watts. Low profile, open frame with optional enclosures. Wide range a-c input (85-264V a-c).

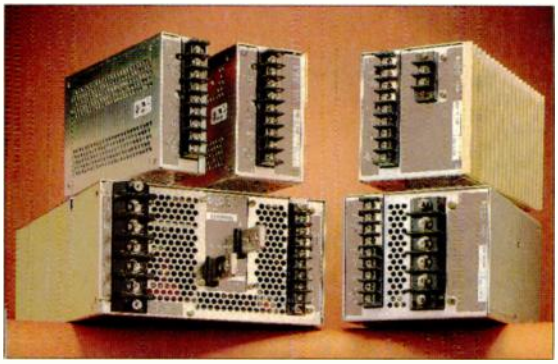
CE — This KEPCO product is backed by a firm 1-YEAR WARRANTY



RAX:

50 watts-1500 watts, fully enclosed. Selectable a-c input.

CE — This KEPCO product is backed by a firm 5-YEAR WARRANTY



RCW:

100 watts-1500 watts, fully enclosed. Wide range a-c input (85-264V a-c) with active power factor correction to suppress the harmonic distortion reflected back on the mains.

CE — This KEPCO product is backed by a firm 5-YEAR WARRANTY

POWER

Nom. Volt	15W	25W	50W	100W	150W	175W	300W	350W	750W	1500W
3.3V			RAX	RAX, RCW		RAX, RCW		RCW	RCW	RCW
5.0V	FAW	FAW	RAX, FAW	RAX, FAW	FAW	RAX	RAX	RCW	RCW	RAX, RCW
12V	FAW	FAW	RAX, FAW	RAX, FAW	FAW	RAX	RAX	RCW	RCW	RAX, RCW
15V	FAW	FAW	RAX, FAW	RAX, FAW	FAW	RAX	RAX	RCW	RCW	RCW
24V	FAW	FAW	RAX, FAW	RAX, FAW	FAW	RAX	RAX	RCW	RCW	RAX, RCW
28V			RAX	RAX, FAW	FAW	RAX	RAX	RCW	RCW	RCW
48V			RAX, FAW	RAX, FAW	FAW	RAX	RAX	RCW	RCW	RAX, RCW

For full technical specifications, write to Dept. NQF-05 or fax or call for Kepco's power supply catalog. If you call, ask for Martin Lachhmanen at extension 5132. He'll be happy to answer your questions.

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READER SERVICE 137

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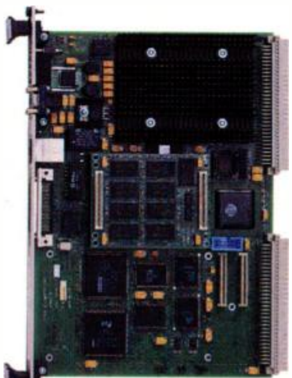

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TUNDRA TERRITORY

READER SERVICE 229

PCI Card Combines UltraSCSI And Fast Ethernet

Functions that previously required two separate add-in cards have now been combined onto one board. The IOBahn adapter employs a PCI connection to handle the bandwidth required by integrating SCSI and Ethernet ports. By blending two separate UltraSCSI (20 Mbytes/s) or UltraWideSCSI (40 Mbytes/s) channels with a Fast Ethernet (100 Mbytes/s) port, overall I/O cost in servers, workstations, and PCs can be reduced.

A bus-mastering card based on the company's INIC-950 SCSI chip and the PCI 2.1 specification, the IOBahn can connect up to 30 SCSI peripherals. Older legacy devices can be configured along with the latest high-performance drives. Having dual SCSI channels also enables faster disk drives to operate on one channel, segregating them from slower devices that would otherwise bog down overall system performance, such as tape drives, scanners, and magneto-optical devices. The Ethernet port can use 10-Mbyte/s 10Base-T or 100-Mbyte/s Fast Ethernet with auto-negotiation, upgrading with a simple software adjustment.

Bundled software includes SmartI/O, a BIOS-resident set-up utility that lets users control which drive and through which channel the computer boots, as well as individual device configuration and adapter termination. The EasiInstall software utility simplifies SCSI and Ethernet software installation under DOS and Windows. Support is included for most popular operating systems, including DOS, Windows 3.11, Windows 95, Windows NT 4.0, NetWare 4.1x, SCO Unix, UnixWare, OS/2 4.0, and Macintosh OS 8. Ethernet drivers are included for Windows 95, Windows NT 4.0, NetWare 4.x, and OS/2. The IOBahn is available now. It is priced at $324 for the UltraSCSI version and $375 for the UltraWideSCSI model.

Initio Corp., 2188-B Del Franco St., San Jose, CA 95131; (408) 577-1919; http://www.initio.com. **CIRCLE 556**

Embedded Graphics Controller Supports Multiple CPU Interfaces

Virtual display and split-screen capability are two of the features of the SED1354 graphics controller, intended for embedded applications such as office-automation equipment and mobile-communications devices. The device is suited for any system using the Microsoft Windows CE operating system or other embedded OS, and is designed to interface to a wide range of 8-, 16-, and 32-bit CPUs from vendors such as Intel, Motorola, NEC, and Hitachi. The SED1354 can display up to 16 bits/pixel on monochrome and color passive LCDs, active matrix TFTs, or EL displays. The chip's virtual-display capability allows for the showing of images larger than the panel by panning. Its split-screen mode supports the display of two separate images simultaneously. The SED1354 supports a flexible operating voltage range from 2.7 to 5.5 V. Power consumption is reduced thanks

(continued on page 87)

(continued from page 86)
to two power-down modes, one in hardware and one in software. In addition, LCD power-sequencing signals help control an external LCD bias power supply and LCD backlight. A 16-bit memory interface supports up to 2 Mbytes of EDO or fast-page-mode DRAM. Panel resolutions can range from 4 by 1 to 800 by 600 pixels. Using an external RAMDAC, images can be simultaneously displayed on both the LCD and CRT. Housed in a 128-pin QFP, the chip is sampling now. Volume production will commence in November. In lots of 10,000, the part sells for $9.70 each.

S-MOS Systems Inc.*, 150 River Oaks Pkwy., San Jose, CA 95134; (408) 922-0200.* **CIRCLE 557**

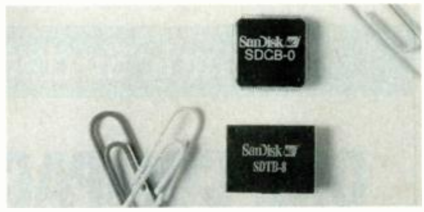
Serial Comm Accelerator Supplies 460-kbit/s Port

The LavaPort PnP Communications Accelerator Board, which runs under Windows 95, lets users exploit the performance capability of their external ISDN Terminal Adapters and V.34 modems, increasing the serial port's maximum bit rate to 460 kbits/s. This ensures that the modem's full bandwidth capability is realized. While high-speed external modems can support these bandwidths, the limiting factor often is the UART. Besides the high performance, the LavaPort PnP provides a number of features to increase the flexibility of the PC's communications. For example, the system can automatically configure itself for any COM and IRQ, even beyond standard COMs 1-4 and IRQ 3 or 4. The board incorporates an expanded 32-byte FIFO buffer, virtually eliminating the possibilities of data over-run errors, even at top speed. An on-board intelligent I/O processor detects flow-control signals at the ports, further off-loading communications overhead from the CPU. The LavaPort PnP sells for $59.95 and is compatible with Windows 95 and Windows NT 4.0.

Lava Computer Mfg. Inc.*, 28A Dansk Court, Rexdale, Ontario, Canada M9W 5V8; (416) 674-5942; http://www.lavalink.com.* **CIRCLE 558**

New Flash Chip Set Stores 64 Mbits

By packaging two 32-Mbit flash-memory die into one standard 56-pin TSOP, designers can now get the advantage of a 64-Mbit IDE-compatible flash chip set. Available in capacities of 2, 4, and 8 Mbytes, the chip set is a two chip solution—the flash memory and the controller, which is housed in a 100-pin TQFP. Because the 64-Mbit part is based on the company's 32-Mbit technology, no hardware or software changes will be required to upgrade an existing system. Data can be transferred at a rate of 4 Mbytes/s to and from the flash memory.



The chip set offers a low power con-
(continued on page 88)

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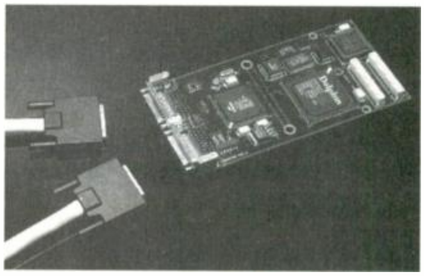
sumption, from 0.66 mW in sleep mode to 200 mW in write mode, both at 3.3 V. The intelligent controller auto-senses whether the chip set should operate at 3.3 or 5 V. Available now in large quantities, the 16-, 32-, and 64-Mbit chip sets sell for $25, $35, and $55, respectively.

SanDisk Corp., 140 Caspian Ct., Sunnyvale, CA 94089; (408) 542-0500; http://www.sandisk.com. CIRCLE 559

SCI Bus Link Adapter Connects PCI, VME

Forming a high-speed data channel between PCI, PMC, and VMEbus systems based on the Scalable Coherent Interface (SCI), the SCI Bus Link can help implement VME-to-VME, VME-to-PCI or PCI-to-PCI connections. This also includes multiple node connections between any mix of VME, PMC and PCI systems. SCI is a standardized interconnect (ANSI/IEEE 1596-1992) providing a transparent, memory-mapped link between multiple nodes over distances up to 25 ft. The modules connect nodes in a point-to-point or ring topology using a 50-pin shielded twisted-pair copper cable with low-noise LVDS signaling. Data is transferred as 16-bit words clocked at a 250-MHz rate, for a raw data rate of 500 Mbyte/s. The SCI Bus Link

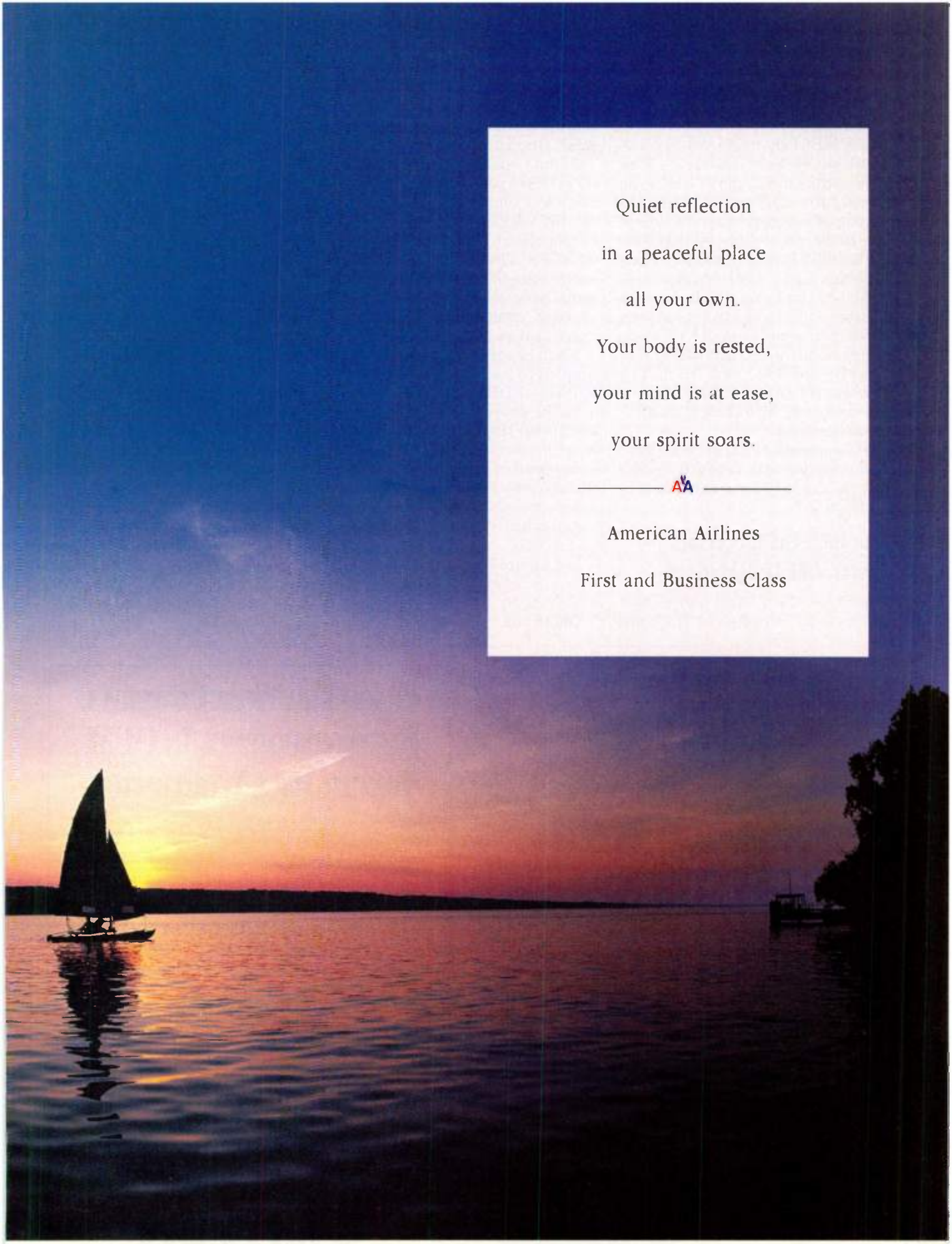


adapter card converts PCI transactions into SCI packets of 64 bytes, and the hardware-implemented SCI protocols ensure reliable delivery with error recovery. Interrupts and atomic operations are supported. One advantage of the SCI Bus Link is that it offers a totally transparent data channel. This means that users simply assign a memory window that maps through the link and into memory in a remote node. This results in a speed increase and a low-latency connection. An effective data rate of 70 Mbytes/s with a latency as low as 2 MICROs is achievable when transferring data between two boards or PCI local buses. Software to initialize the link is provided for Windows NT on Pentium-based systems and for the VxWorks real-time operating system. The SCI Bus Link module is priced at $3250.

Vmetro Inc., 1880 Dairy Ashford, Suite 535, Houston, TX 77077; (281) 584-0728; http://www.vmetro.com.
CIRCLE 560

VME Board Holds PowerPC 769 CPU

A 300-MHZ PowerPC 760 microprocessor is the brains behind a pair of VMEbus boards, the Power4e and the Power4B. According to the company, with a benchmark rating of 14.1 SPECint95 and 13 SPECfp95, the two boards are the fastest ever intro-
(continued on page 90)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all your own.
Your body is rested,
your mind is at ease,
your spirit soars.
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(continued from page 88)
duced. The Power4B supports five-row VME64 connectors as well as 100Base-T4-Fast Ethernet. The Power4e fits in a single 6U slot, even when fully configured with 256 Mbytes of memory. Other features of the Power4e include support for 100Base-TX Ethernet, a PMC mezzanine bus, and a VME64 interface. Based on the PowerPC Reference Platform (PReP), the two boards can handle both real-time and Unix operating systems, including VxWorks 5.3, LynxOS, pSOS+, and OS-9. The Power4e is priced at $5750, while the Power4B costs $6170, both in their basic configurations.

***VI Computer Inc.**, 531 Encinitas Blvd., Suite 114, Encinitas, CA 92024; (760) 632-5823; http://www.vicomp.com.*

CIRCLE 561

Four High-End Processors Power VME Daughtercard

Four PowerPC 740 microprocessor and up to 256 Mbytes of DRAM are the key features that make up the Excalibur multiprocessor daughtercard. One card attached to a 6U VMEbus motherboard offers 2 GFLOPS of performance. When the maximum four cards are connected to a 9U VMEbus motherboard, the performance level jumps to 8 GFLOPS. The high level of performance suits the board for image- and signal-processing applications, such as radar, sonar, medical imaging, and image analysis.

Each processor on the board is coupled to its own bank of 32 or 64 Mbytes of DRAM that's accessed over the processor's local memory bus at 666 Mbytes/s. Memory from other processors is accessed at the same speed over the card's local bus. Global memory and memory on other daughtercards is accessible through the on-board 320-Mbyte/s SKYchannel interface.

***Sky Computers Inc.**, 27 Industrial Ave., Chelmsford, MA 01824; (508) 250-1920; http://www.sky.com.*

CIRCLE 562

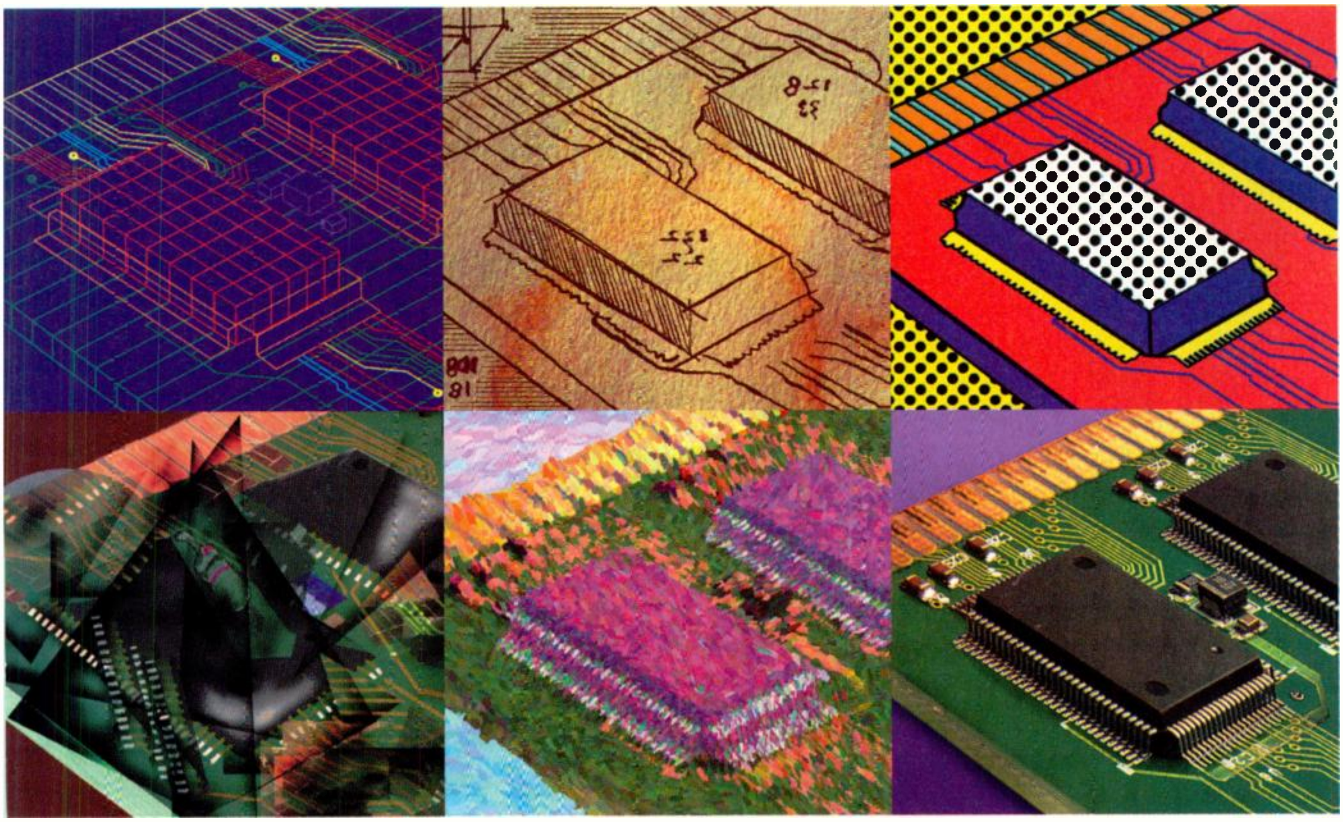
Sparc Board Supports 2eVME Protocol

The CPU-20VTe is a SparcStation 20-compatible board that supports the 2eVME protocol. This means that it can pass data at 110 Mbytes/s over the VMEbus. The protocol increases the available VMEbus bandwidth by reducing the number of handshake signals per transfer from four to two. The 50% reduction in protocol management is then allocated to the data-transfer phases, effectively doubling the bandwidth. The CPU-20VTe contains two Mbus slots to hold up to four 150- or 200-MHz hyperSparc processors. Up to 512 Mbytes of DRAM can be employed. Two SBus slots are available, in addition to an Ethernet and SCSI-2 interface. It runs Solaris, as well as a host of real-time operating systems. Available now, the CPU-20VTe starts at $15,995.

***Force Computers Inc.**, 2001 Logic Drive, San Jose, CA 95124; (800) FORCE-USA or (408) 369-6000; http://www.forcecomputers.com.*

CIRCLE 563

AMP Simulation. It's how top electronics companies make it right before they make it real.



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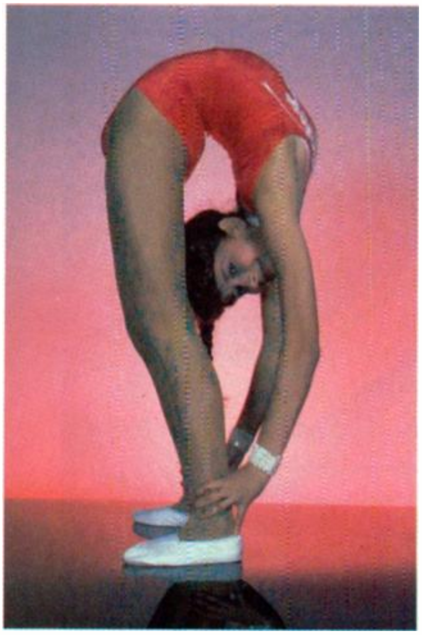
See AMP on the Internet: http://www.amp.com/

READER SERVICE 98



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UPDATE ON EMC SIMULATION

New Simulation Tools Help PC Boards Meet EMC Requirements

The "Old World" (Europe) consists of many countries with their own set of legislations. In contrast, a uniform set of standards exists for engineers within Europe. Since January 1, 1996, the CE Mark is the standard that engineers must adhere to if their company wishes to export their products to several European countries. For example, the CE Mark requests specific data regarding electromagnetic compatibility (EMC). For most designs, the process of achieving the EMC directives of the CE Mark consumes a lot of time, meaning that time-to-market often is delayed.

To accelerate this time-to-market while simultaneously meeting CE's strict EMC directives, the corporate technology department of Siemens AG, Munich, Germany, has evaluated an EMC simulation tool that allows the integration of the EMC simulation into the virtual prototyping process by use of CAD-mechatronics (ELECTRONIC DESIGN, *Sept. 16, 1996, p. 69*). Compared to the current method of physically measuring EMC parameters of the entire product, redesigning the product, producing another prototype, physically measuring again, and repeating this procedure several times, EMC simulation saves time as well as money.

EMC simulation takes place after pc-board layout, with the transferring of layout data to the EMC simulator. This data package contains information about the net geometries, the components, and the setup of the pc board. The designer then adds data regarding the signals on the individual board "wires." Data on the ICs used are provided by IBIS simulation models, which act as a "little brother" to the more traditional Spice models *(see "More about IBIS," p. XX)*. While Spice models might enable reverse engineering, IBIS models do not allow this, which eliminates the need for signing a nondisclosure agreement (NDA) before releasing the models. However, IBIS models can be used for components simulation. (You can find more information, along with some IBIS models, on the World Wide Web at *http://www.eia.org/eig/ibis/ibis.htm*.) Components already on the market also can be modeled by using the default models provided by the software manufacturer.

The Process

Just how does Siemens simulate electromagnetic radiation? It does so by measuring current, taking advantage of the fact that magnetic flux density is directly proportional to the current in a wire. A first step is the "transmission line analysis," where every conduction path—a connection or "wire" on a pc board—is divided into many little segments. For every segment, current and voltage is calculated depending on the time. This result is transferred from the time domain to the frequency domain by fast Fourier transformation (FFT).

An FFT is performed for every single conduction path on the board, followed by a calculation of the magnetic field for each frequency. This calculation is based on the method of moments (MOM). For every segment of the conduction path, a loop antenna is "cre-

Companies Mentioned In This Story

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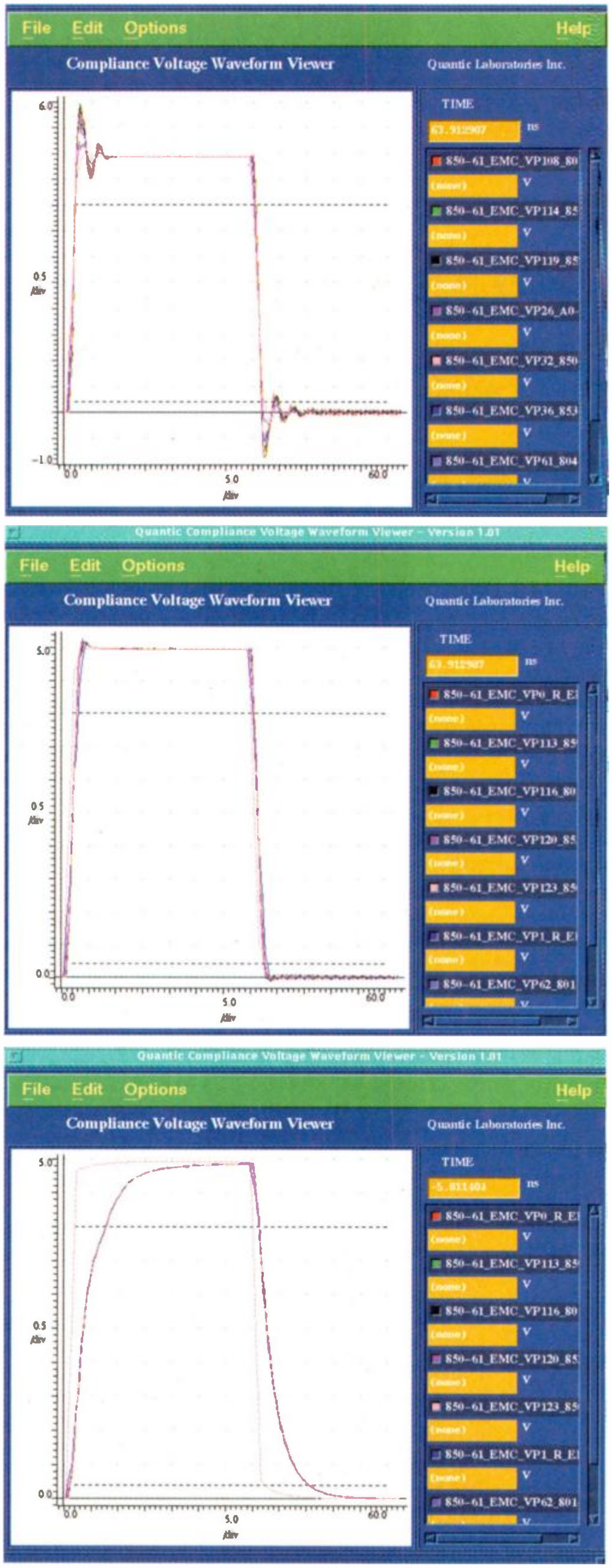
ated" by means of simulation. The EMC simulation software simulates the scanning of the entire pc-board surface by using a simulated reception antenna to "measure" the strength of the magnetic field at a height of 5 mm (about 0.2 in.) above the board. The measurement is performed over the entire frequency range. Physical scanning of the board at an EMC test laboratory would create the same picture.

This method allows the determination of the maximum field intensity at a single point, which means that the engineer gets to know the area with the biggest radiation. "At this point you start looking at the individual conduction paths underneath where you start the optimization," says Peter Kaiser, CAE consultant at the Siemens Corporate Labs. "It's time for the engineer to show his or her skills and experiences." The approach looks quite reasonable: You look for the conduction path with the most radiation. In the example described in this article, this is a clock line.

Now it's time to go back to the currents creating the magnetic field. To decrease the amount of radiated energy, the area of the loop antenna as well as the current must be decreased. The most common methods are to add components such as a series resistor, reroute the conduction path network, place the pc-board track on another layer, or place a component on another board spot. If simulation is performed during the layout phase, these measures can be applied easily, rapidly, and cost-effectively.

The clock line mentioned above forms an oscillating circuit for some frequencies. To attenuate the oscillation, Kaiser's team loaded the pc-board track that's radiating the most into the simulator. A series resistor, whose optimum value is determined by applying several simulation runs, helps minimize radiation. Optimum in this context means that the radiation is minimized on one side and that signal integrity can still be maintained on the other side.



1. Voltage waveforms for resistor values of 0 Ω (a), 80 Ω (b) and 200 Ω (c). The radiation of the fundamental frequency is 10 dBμA/m with the 80-Ω resistor. With higher frequencies, a suppression of up to 25 dBμA/m may be achieved.

Shown is the voltage at such a critical point with no resistor, an 80-Ω resistor, and a 200-Ω resistor *(Fig. 1)*. A resistance of 80 Ω turns out to be the optimum value in this application. The addition of a single resistor helped to decrease electromagnetic radiation by 10 dBμA/m with the 80-Ω resistor. With higher frequencies, a suppression of up to 25 dBμA/m may be achieved. Realizing such a reduction with a single resistor which costs almost nothing compared to the means normally needed to keep the radiation low is a very low-cost solution. "The average improvement of a digital pc board that can be achieved with an EMC simulation tool is about 10 to 15 dBμV/m in far field," claims Kaiser.

The time needed for a simulation run depends on the size of the board and on the number of nets to be calculated. On a Sun Sparc Ultra workstation with 128 Mbytes of RAM, a simulation with 16 address bus lines and a total of 160 connected components was completed within one hour, and the simulation of an entire board took just one night. "The simulation of single nets during the optimization process seldom takes more than 5 minutes," reports Kaiser.

Kaiser's team has been working on EMC simulation for about two years, and carefully looked for a system that best fit the needs of a large company like Siemens. The precondition was always the same: data had to be imported from the layout system.

Three programs have been evaluated: EMC Scan from Canadian manufacturer

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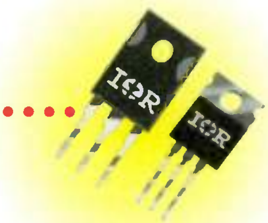

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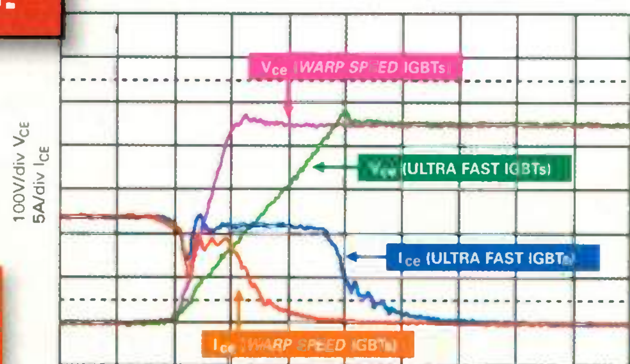

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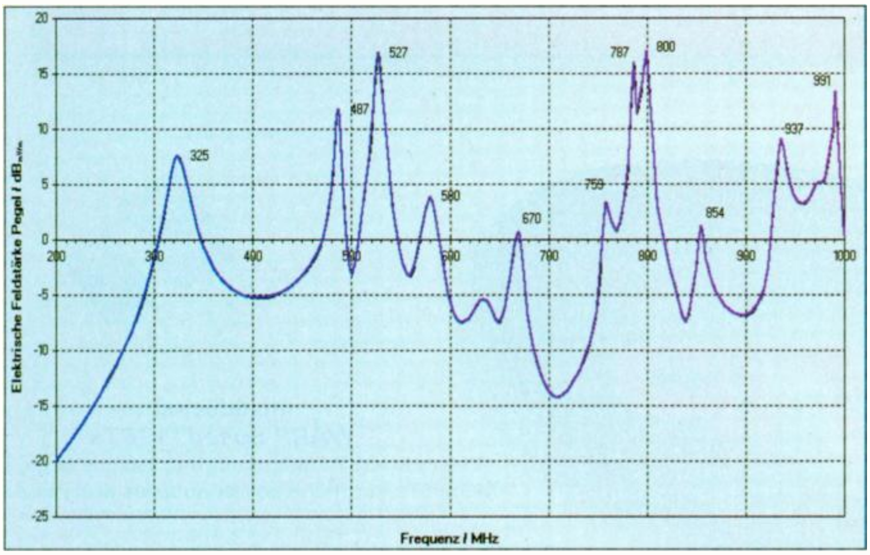


2. Even a case that is supposed to be electromagnetically shielded is only capable of shielding some frequencies. Other frequencies may even be amplified.

Quantic; Quiet from Viewlogic's California subsidiary Quad Design; and Comoran from a German company named Incases. As Kaiser points out, after the first evaluations, Siemens concentrated on Quantic's and Incases' solutions because their algorithms were a better fit for Siemens' needs. "Due to time pressure, we had to decide on one of the two tools within two months," Kaiser adds. "We chose EMC Scan of Quantic, and we also contributed inputs to adapt the early beta version of the program."

When Siemens first evaluated the EMC simulation, the company thought that one person would have to focus on nothing but field simulation for 6 to 12 months, which can be quite expensive. They then began to create libraries and to simulate, which took an entire night. The next morning, they called the design engineer and identified the three conduction paths on his pc board that radiated the most. "These were exactly the same conduction paths which had been identified within several weeks of physical measurements," reports Kaiser. "This result convinced our management to proceed with the project."

Kaiser's team significantly improved the user interface. He claims that with the tool, the first positive results can be achieved after one week, and that the entire tool can be mastered and controlled after four weeks. However, a designer, whose task it is to run the EMC simulation, should be familiar with terms like electrical and magnetic field as well as FFTs before learning how to use the simulation software.

Siemens uses the EMC tool within a mixed virtual prototyping environment where all the relevant data can be exchanged between the individual software tools. For example, their physical harness routing program is CATIA3D from IBM Germany, while Logical Cable from Mentor Graphics is used for the intelligent schematic capture because it has specific capabilities for interconnect and wire harness designs. The 3D CAD program I-DEAS from Structural Dynamics Research and Pro/Engineer from Parametric Technology also are used.

Design Environment

The new version of a design environment dubbed EDAnavigator 2.0 from Xynetix Design Systems Inc., Fishers, N.Y. (formerly Harris EDA) is now becoming more interesting for the design engineer involved in virtual prototyping. For example, the EMI tools from Quantic Labs can be integrated into the EDAnavigator environment, giving Quantic tool users the possibility of using the tools earlier in the design cycle (pre-route analysis). Siemens has not yet evaluated this new solution since it was released this July. According to Xynetix, EDAnavigator 2.0 provides an easier-to-use interface for post-layout analysis with the Quantic tool.

Predict And Prevent

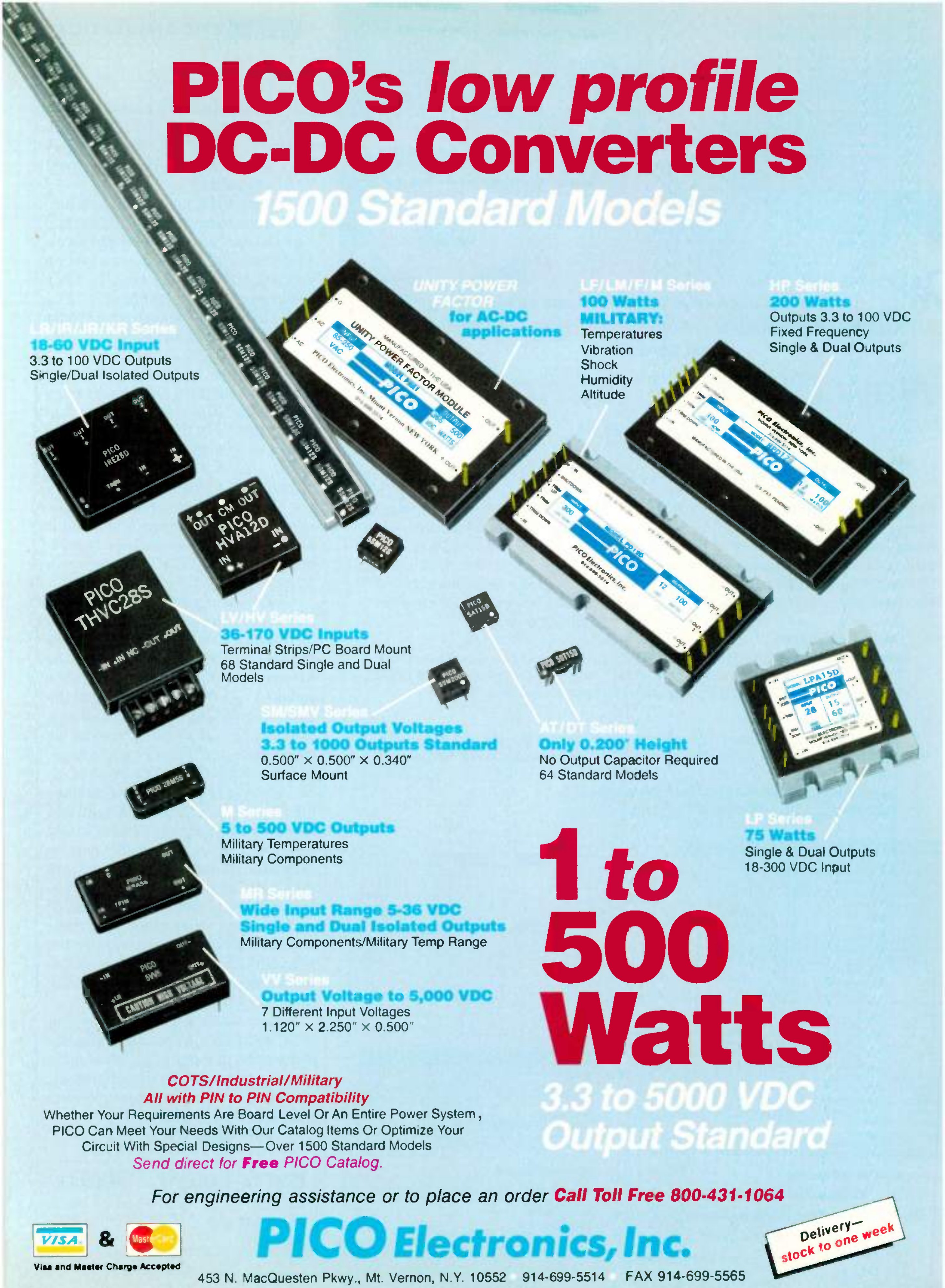
Without EDAnavigator, EMI simulation tools like those from Quantic and Quad Design are only useful for "post-layout analysis," meaning that after the board is placed and routed, you can find out what you did wrong, then you go back and fix it.

As Xynetix points out, this "find and fix" design process is now being replaced by a "predict and prevent" design process, where engineers have tools to help anticipate problems before they occur. EDAnavigator is said to enable electrical engineers to access constraints and resolve conflicts among them before sending the design to layout, improving product performance and eliminating iterations. It provides pre-route analysis for EMI, signal integrity, and thermal and mechanical issues. It does this by integrating commercial EMI and signal-integrity tools such as those from Quantic, Quad Design, and Incases into the EDAnavigator environment, along with its own set of built-in "Design Advisors."

The next step is the examination of the EMC parameters of cases. The EMC simulation of a pc board within a case cannot be handled at this point due to the limited computing power of workstations. As a result, Siemens took a board with a single conduction

More about IBIS

IBIS (Input Output Buffer Information Specification) is a method of providing I/O device characteristics through V/I data without disclosing any circuit/process information. It can be thought of as a behavioral modeling specification suitable for transmission-line simulation of digital systems and is applicable to most digital components. IBIS has a "Golder Parser" program called ibischk2 that parses the model file to verify that the file conforms to the IBIS specification. This free prorgram, available as object code, has executable code developed by contractors for the IBIS Open Forum. All model files must pass the parser before a model can be released to vhdl.org.



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path and simulated the radiation of the case. "Currently, such a simulation still takes one month," says Kaiser. "However, we're jointly working with Quantic on a faster tool."

To start work now, Siemens simulated the antenna without the case and kept the result for reference purposes. They then simulated the entire system and subtracted the results they achieved with the antenna only *(Fig. 2)*. It shows that the case shields only some frequencies and even amplifies other frequencies.

As a result, the question becomes: why does a shielding case amplify some frequencies? The answer is quite simple. At 320 MHz, the slot length of the case is exactly one-half a wavelength. Every peak on the diagram can be assigned to a specific structural part of the case. These results create new questions because in terms of EMC, it would be good if a case only had a minimum number of slots; however, in terms of cooling, the slots are needed.

Cables leading into a case also influence a system's electromagnetic performance. The part of the cable within the case is a receiving antenna and the exterior part is a transmitting aerial for radiated signals generated within the case. "Now we know why it radiates, however, we are working on what we can do against it," Kaiser comments.

Even though EMC simulation of entire systems requires a lot of computing power, it can be handled quite fast because parallel computing can be used effectively. Every frequency may be calculated by another computer. Until now, parallel computation was problematic because the computers had to wait for results from other computers. But here, it is possible to transfer the relevant data for 5 seconds, calculate for two hours, and then transfer back the data for 5 seconds.

Kaiser concludes: "We can say that EMC simulation helps to significantly reduce the amount of physical measurements needed in the laboratory, however, it will not replace physical measurements by 100%."

Alfred Vollmer

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EDA WATCH

Windows NT Vs. Unix: The Road To Abilene Is Paved With Customization

Much of the talk these days in the EDA world revolves around the importance and future of Windows NT versus Unix, especially in the pc-board design corner. As a pragmatist, I have always been more concerned about the productivity and cost-effectiveness of the application tools than the platform on which they reside. All computing platforms and their operating systems have value, but they are simply tools, not battlegrounds for ego, elegance, or holy wars.

In the 1970s and '80s, EDA tools were sold, using traditional sales methods, directly by their developers to very large corporate clients. That is, a salesperson would bypass the design department and call on corporate information centers, group vice presidents, or if he or she was really lucky, the president. The deals often were signed during a Palm Springs golf junket or a cruise to the Bahamas. The engineering management and their design staff would have to live with these decisions, most often at enormous costs per seat. If the "sell" happened at that very high level, price was no object—with easy justification for buying more seats.

The learning curve was a non-issue. And, for any integration issues, there was always that ready and willing, ever-growing consulting group down the hall or on-site at the EDA vendor that added to operating overhead. If the sell was made at a lower level—say to a division vice president or corporate information systems director—and the tools turned out to be less than adequate or too expensive, everything was hush-hush. Reputations and job titles were at stake. It was not so easy in those days to admit mistakes and suggest that perhaps better cost-effective replacement tools were available.

These lower-level decision makers would spend more time justifying why the decision was good than working to keep up with advances or new products that may have been better choices. It was easier to just keep buying into the original decision. And, we can't completely leave out the users, either. Once someone invests an enormous amount of time in a long learning curve, it's hard to think about going back to the training lab while under great pressure to launch products. So for many reasons, once installed, these EDA tools were very difficult to unseat. As a result, there are thousands of high-end (i.e., expensive) Unix seats still in use, with enormous annual maintenance contracts protected by decisions made years ago.

Why is NT becoming the destination platform of choice? Even if you discount the price/performance return on investment (ROI), which is often overwhelming, there are other reasons why NT is attractive for vendors and users. In a corporate enterprise, PCs are most likely to be found on the desks of all the administrative, sales, marketing, operations, and manufacturing groups. Information systems organizations must maintain both Unix and PC worlds in engineering groups because the engineers need PC access to the rest of the enterprise. That's expensive, and mixed computing environments are nightmares. As Windows penetrates the business side of an organization, becoming more robust and compatible along the way, it will naturally penetrate the rest of the business.

The ROI for vendors and customers going to NT is significant. Say we have an application, EDA or other, and the customers want to be able to attach documents to their designs. In Windows/NT, on an application written using object technology, the vendor developer would use NT tools such as OLE or ActiveX with all the underlying functionality already written by the operating-system vendor (Microsoft), simply focusing on the higher-level function. For the same requirement on a Unix application, the developer would have to design and write all the lower-level code before working on the desired function. Unix is very flexible and powerful, but at the same time, this creates additional development and support costs.

The vendor can deliver a function to the customer faster and cheaper, and with less long-term maintenance cost using NT. The user gets an easy-to-install system that not only performs the desired function, but does it like his or her other applications. This means smaller learning curves; after all, Drag and Drop is Drag and Drop whether it's your spreadsheet, word processor, analysis program, or Internet connection.

Can your employees really afford to learn the idiosyncrasies of the implementation of each application in Unix? Even in engineering the term "casual user" is becoming more prevalent. The engineer's tasks throughout a project life cycle are so varied that he or she can't afford to be a master of each application. But, if the paradigms are similar between all the applications, productivity is sufficiently improved by not having to go to the manual every time an application is opened. For doubters out there, sit down with three different vendors' Unix applications and three different Windows/NT applications and try it yourself.

This dilemma brings to mind an old story, "The Road To Abilene." I'll spare you the details and give you the short version. A family living in West Texas took a long drive into Abilene after church one Sunday for ice cream. By the time they arrived home, with everyone frustrated and irritable from the long, hot drive in a crowded car (with no air conditioning), it was discovered through finger pointing and argument that no one really wanted to go in the first place. Someone had just mentioned how good ice cream would taste and, because none of the folks bothered to say what they really thought, they all ended up on a round-trip to Abilene. Lots of EDA tool customers have been on that long road.

Starting in the late 1980s, some EDA entrepreneurs envisioned a market needing more cost-efficient tools on a platform that just happened to be widely-available: the PC. Like any technology, the first entry into lower-cost tools did not have the capability of more mature products, and were adopted on price points alone. Remember the first car that Honda sold in the U.S. 25 years ago; a Civic, pocket-sized, dependable, and listing under $2000?

But these tools have evolved rapidly, thanks in part to low-cost programming and compiling tools, and friendlier programming languages. The tools now available on Windows NT are very sophisticated and capable. And, PC hardware has come a long way. The

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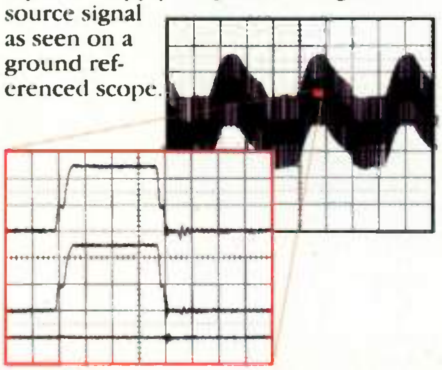

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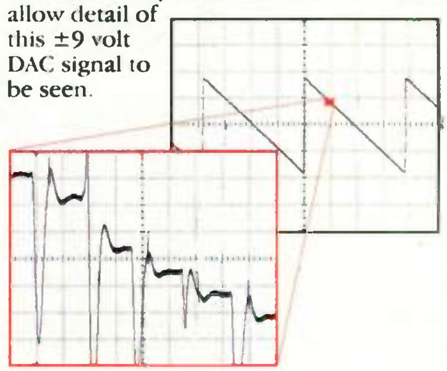

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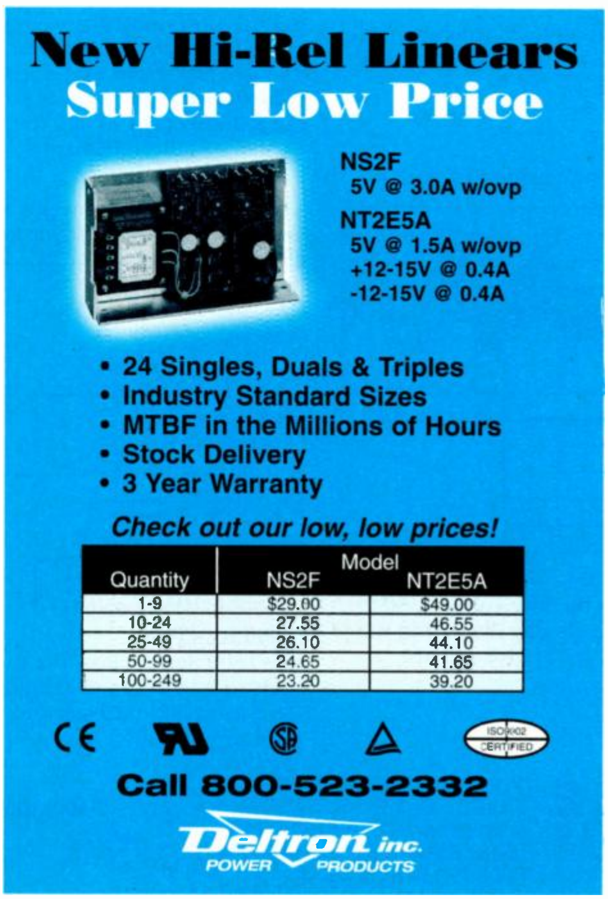

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sales channels now for those visionary EDA entrepreneurs often include regional value-added resellers who are usually engineers selling to engineers. They are mindful of service, cost-effectiveness, quality, ease-of-use, and just plain old getting the job done.

As Microsoft, Intel, and Internet-based vendors continue making unparalleled advances in quality, price, performance, and interoperability, Unix EDA tool developers argue over standards, academic operating-system papers, and why those PCs will never survive. Now it's the 1990s, and many of the EDA tools in use arrived on a customer's dock by way of a round-trip to Abilene. These mature products have tried to stand on their laurels, but have not progressed at the same rate. And, the decision maker doesn't want to justify why it may be time to look at other solutions—that is, if he or she is still around. That decision maker will point to the gigantic investment made in the user's learning curve and in customization and say, "let's just stick it out and hope our vendor finally makes good on those promises to take us forward with lower-cost, better-integrated, and more productive tools."

So, all the argument and issues in the EDA world these days aren't really over NT versus Unix. Rather, it's how 1970s and 1980s-style vendors can upgrade their product's price-performance rating, and how they can accelerate their sales strategies to be a 1990s-style vendor. Until they figure all that out, their customers will still be heading to Abilene. In today's business environment, one thing I'm sure of is that none of them are out working on the golf course or in the Bahamas.

Contributed by Jerry Burwell, vice president of Engineering at ACCEL Technologies Inc., San Diego, Calif.; (619) 554-1000. Burwell has been with ACCEL since 1991. His was previously in management positions in CAD development at GE Calma, and UCC and TI in Dallas. He holds a BS in Applied Mathematics and a CS from the University of North Carolina, Charlotte, N.C.

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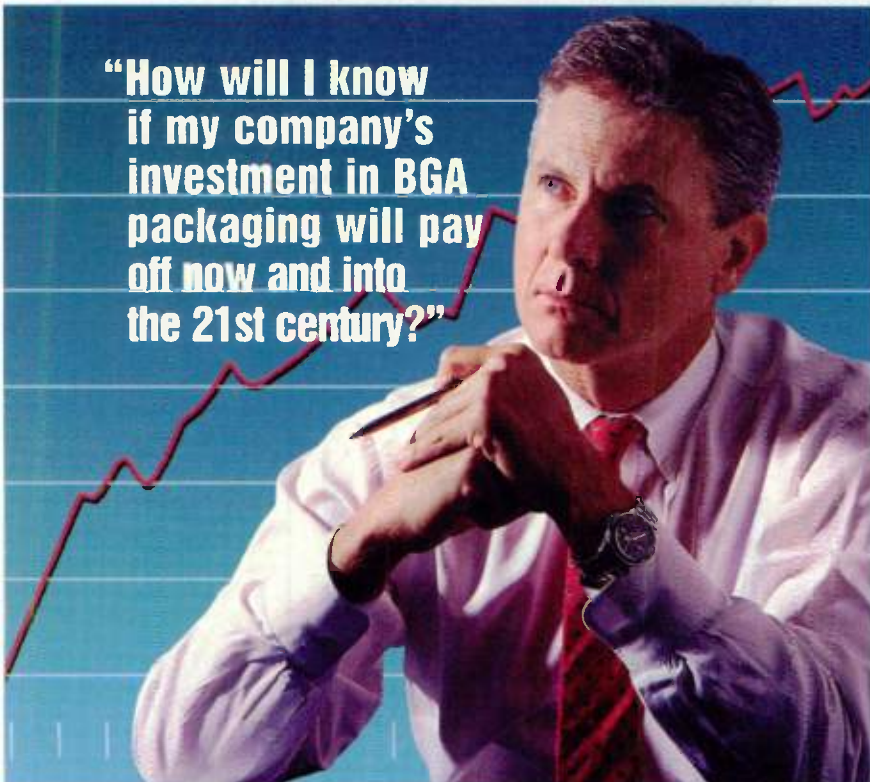

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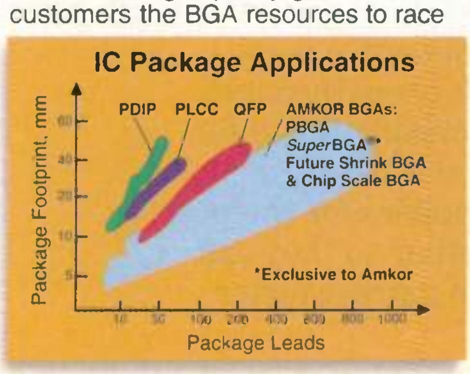

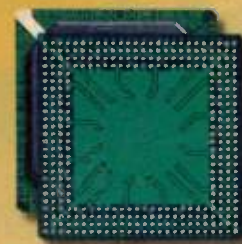

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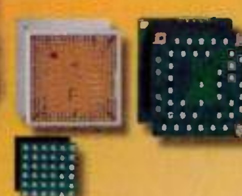

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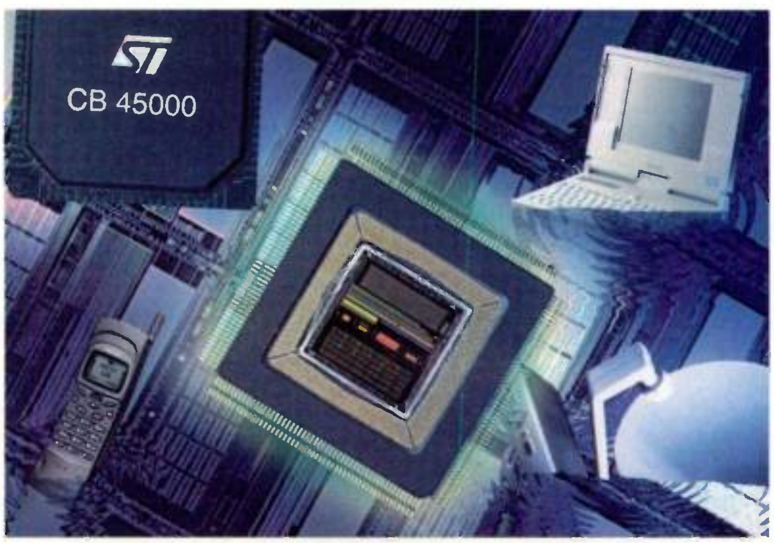
SPECIAL REPORT

Integrating a complete system solution on a single chip is getting easier, thanks to a confluence of technologies and tools that provide the desired density, process technologies, circuit building blocks, and design and analysis capabilities. Yesterday's multimillion gate system is today's single-chip solution, and future solutions will let designers combine tens of millions of logic gates, 100 Mbits or more of DRAM or several megabits of SRAM or flash memory, and mixed-signal functions onto a single chip.

To make such designs possible, semiconductor manufacturers are putting into place deep-submicron CMOS processes that tout drawn feature dimensions ranging from between 0.25 to 0.21 µm, which will typically yield effective gate lengths of between 0.15 and 0.18 µm. With such small features, transistors will dissipate much less power and switch faster, since parasitic capacitance and other performance-detracting factors have been reduced. Lower operating voltages also will be required since the smaller transistors will use thinner oxide layers and electric-field stresses across the oxide must be reduced. As a result, these new generations of logic circuits will require supply voltages of 1.8 and 2.5 V with 3.3-V-capable I/O levels, rather than the 3.3- and 5-V supply levels that are commonly used today.



Art Courtesy: SGS-Thomson

One of the largest challenges facing chip manufacturers is the daunting task of interconnecting the millions of gates and megabytes of memory on the chip. To do this, new metallization schemes that allow five or more levels of interconnections, with pitches of 1.25 µm and even tighter on the first few layers, will provide the connectivity required. Additionally, new planarization schemes such as chemical-mechanical polishing flatten the oxide layer between metal layers to provide an even surface for the next lithography step—eliminating potential optical distortion when the next layer's patterns are formed. Simply put, the flatter the surface and the more precise the lithography, the finer the dimensions that can be created.

The large area of some of these systems-on-a-chip—often approaching an inch on a side—usually means the performance of the designs is dominated by propagation delays rather than by the basic gate delays of the logic elements. Therefore, metal resistance is an important issue as the lines get thinner and longer. Advanced metal combinations such as aluminum-copper or multilayer metal sandwiches will provide lower-resistance interconnections that are less likely to suffer from metal-migration, and will result in higher reliability.

Interconnections, of course, are just one of the challenges that chip designers and silicon manufacturers must face. Designing systems that employ millions of gates is a critical architectural challenge. So is thorough testing of these before fabricating the silicon. To solve some of those issues, designers are developing large libraries of reusable predesigned and pretested functions—intellectual property (IP)—that can be repeatedly deployed in various system designs; some without change, and some with modifications.

Many functions are available in the ASIC manufacturer's design libraries as well as from independent IP suppliers. Designers can select from various licensed architectures of RISC CPUs from companies such as Advanced RISC Machines, IBM, MIPS Technology Div. of Silicon Graphics, Motorola, and Sun Microelectronics. They also can have DSP building blocks from The DSP Group, Lucent Technologies, Motorola, Siemens, Texas Instruments (TI), and others, as well as many internally developed functions, such as data communications and network controllers, ATM segmentation and reassembly blocks, and universal serial bus (USB) controllers.

One of the most sought-after blocks that has become almost every large company's mantra is the DRAM. Such a memory block provides designers with high-density on-chip storage—typically four or more times the density possible than with static memory cells. Although some designers feel integrating DRAM onto a logic chip will drive costs down and will make possible full digital systems-on-a-chip, such chips will actually cost more than than their discrete alternative of the CPU plus memory and other functions.

Rather than view the DRAM as a cost-reducer, embedded DRAM blocks should be viewed as an opportunity to rearchitect traditional system designs and provide value-added capabilities. The rearchitecting should be done to take advantage of the ability to integrate DRAM blocks with almost any word width—8, 16, 128, 1024 bits, and so on. With pinout restrictions removed, very wide on-chip buses can be used to rapidly move data from function to function. That would allow more efficient system operation, resulting in higher system performance without large external buses.

Standardizing Interfaces

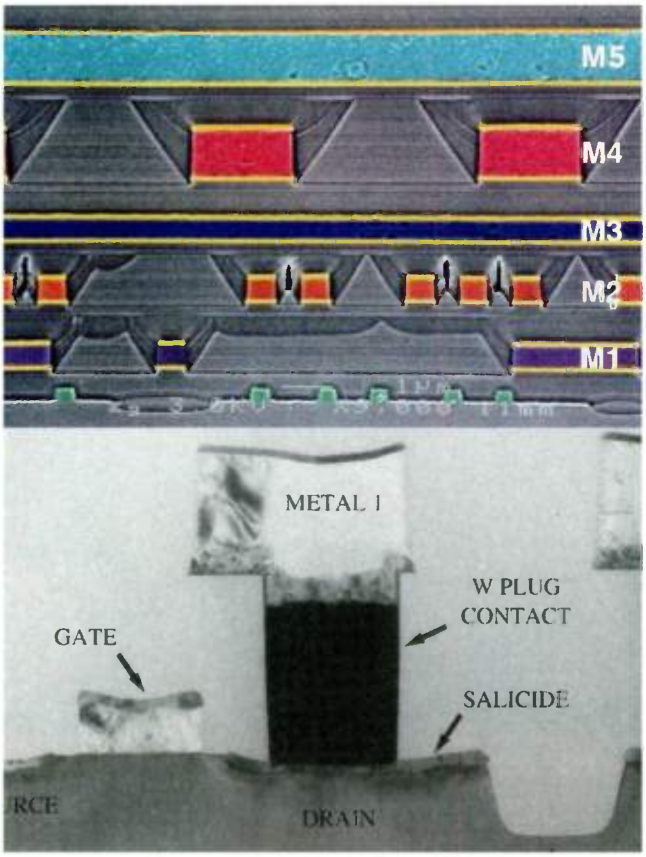
As part of the wave of interest in IP, a new industry organization—the Virtual Socket Interface Alliance (VSIA)—is helping promote some standardization and provide guidelines for the interfaces to blocks of IP that members would either create or use *(see "Unifying the system-chip industry," p. 114)*. By promulgating some type of standardization, it should become easier for blocks of IP from multiple sources to be combined by the system designer and accepted for use by various silicon manufacturers, rather than lock the designer to just one company that has the only process capable of fabricating the block. This also will broaden the choice of functional blocks available to the system designer, since the mixing and matching of blocks from various IP suppliers would be an easy task.

Software tools that can generate variable-size blocks of memory, an n-bit data path or n-bit multiplier, or some other regular function, also are key tools for today's designers. And picking up a tremendous amount of momentum are the high-level design languages (HDLs) such as VHDL and Verilog, which let designers specify functions. The resulting code from the compiled HDLs can then be passed on to logic-synthesis tools that will create the circuit netlists based on a closely coupled cell library.

As a result, system-on-a-chip designs are practical only when the tools, IP (design libraries), and the advanced high-density processes come together. Many companies are now developing such combinations, either with their own software and IP, or by combining "best-of-class" tools and IP from multiple suppliers *(see "Verifying system-on-a-chip designs," p. 116)*. Some ASIC suppliers are focusing on digital-only solutions, while some also can handle mixed-signal functions.

Recent announcements from LSI Logic, Lucent Technologies, NEC, Samsung, Texas Instruments, Toshiba, and VLSI Technology have focused on advanced processes capable of supporting complexities of 8 to 10 million gates, up to 140 Mbits of DRAM, or several megabits of SRAM or flash, and analog blocks such as comparators, analog-to-digital converters (ADCs), and digital-to-analog converters (DACs). However, one process technology doesn't always solve every designer's system problem. As a result, several companies have developed multiple versions of their processes—one version optimized for high density, the other for high speed.

One such combination, available in the G11 product family



1. Very planar inter-metal layers are possible on this multilayer metal process developed by LSI Logic Corp. for its 0.25-µm G11 ASIC process (a). Tungsten plugs, chemical-mechanical polishing, salicided source/drain contacts, and shallow trench isolation are all put to work by VLSI Technology Inc. in its 0.25-µm ASIC process (b). The shallow trenches improve circuit packing density by providing isolation between adjacent transistors.

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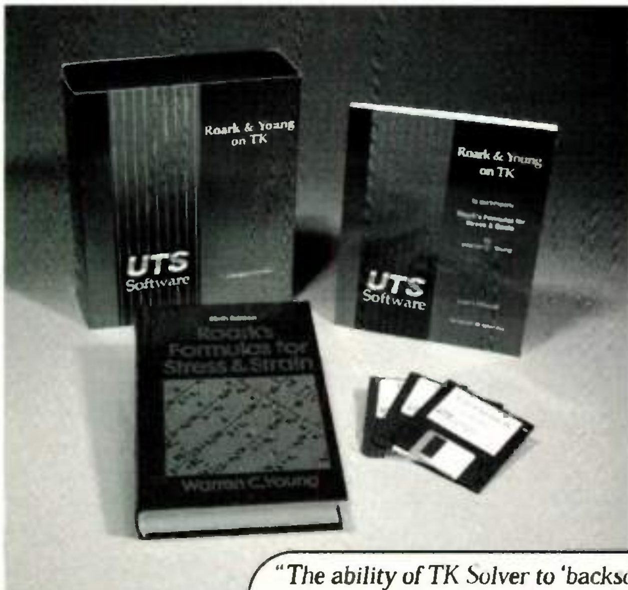

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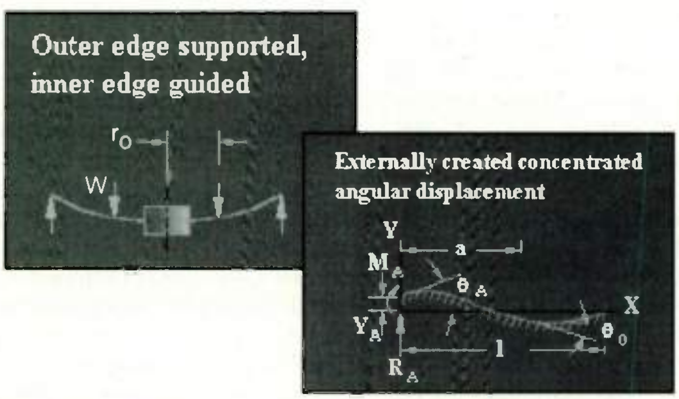

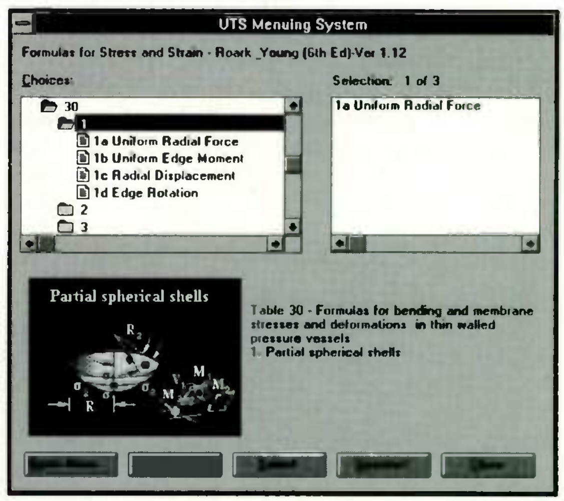

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from LSI Logic, consists of what the company calls a mix-and-match architecture that allows up to 8.1 million usable logic gates (the equivalent of 11 Intel P6 CPUs) on a single chip. Based on two different cell structures and associated libraries, the process allows designers to mix and match the cells from both libraries to meet the varied system demands. The high-performance library is optimized for 2.5-V operation for maximum performance, while the high-density library operates at 1.8 V to minimize power dissipation and allow higher gate density. Power dissipation per gate ranges from about 30 nW/MHz for the low-power cells to 250 nW/MHz for the high-performance cells. Cores from the company's CoreWare library, or other blocks can be implemented in either a library and brought into the system design.

To make the chips, LSI Logic employs up to six levels of metallization with metal-to-metal spacings as tight as 0.7 µm *(Fig. 1a)*. That tight spacing also makes possible dense SRAM cells that will allow designers to pack up to 8 Mbits of SRAM (about half the chip area) onto a system chip. The company's design tools provide a hierarchical design methodology that permits timing closure on complex designs beyond 2 million gates in the shortest possible time. The methodology also can achieve maximum performance by routing performance-critical clocks, global interconnects, and power and ground lines on wider-pitch, low-resistance metal traces.

LSI Logic has signed a deal with Micron Technology to embed Micron's DRAM structures on chips fabricated with the G11 process. By mid-1998, LSI Logic expects to have the Micron 0.25-µm DRAM process integrated into the ASIC design flow. The process will allow designers to combine up to 128 Mbits of single-transistor memory cells along with 8.1 million gates of logic. The first chips to emerge from the joint process will operate from either 2.5- or 3.3-V supplies. Both Micron and LSI Logic will manufacture the merged technology chips. And, to help designers get the most out of the process capabilities, LSI Logic also acquired Mint Technology, a company that specializes in system architecture and system-level design verification.

A slightly different tack has been taken by VLSI Technology which has developed, in conjunction with Hitachi, two processes that each have their own libraries rather than two cell structures based on a single process. The VSC9 and VSC10 processes are based on 0.25- and 0.20-µm minimum features, respectively. Both support 3.3-V I/O levels, and both deliver the same chip densities and have the same basic gate delay of 35 ps (inverter stage), but have been optimized differently.

Maximum logic complexity possible with the processes hits 18 million gates on a 22-by-22-mm chip, almost three times the complexity possible with the company's 0.35-µm process that employs a 1.4-µm minimum metal pitch. The 0.25-µm process focuses on high-speed applications operating at 2.5 V, while the 0.20-µm series minimizes power consumption and operates at 1.8 V. With advanced packaging technology, designers can get I/O pin counts ranging from 80-lead quad-sided flat packages to 1200 connections using flip-chip ball-grid array packages.

The power per gate on the VSC9 process is just 40 nW/MHz and half that

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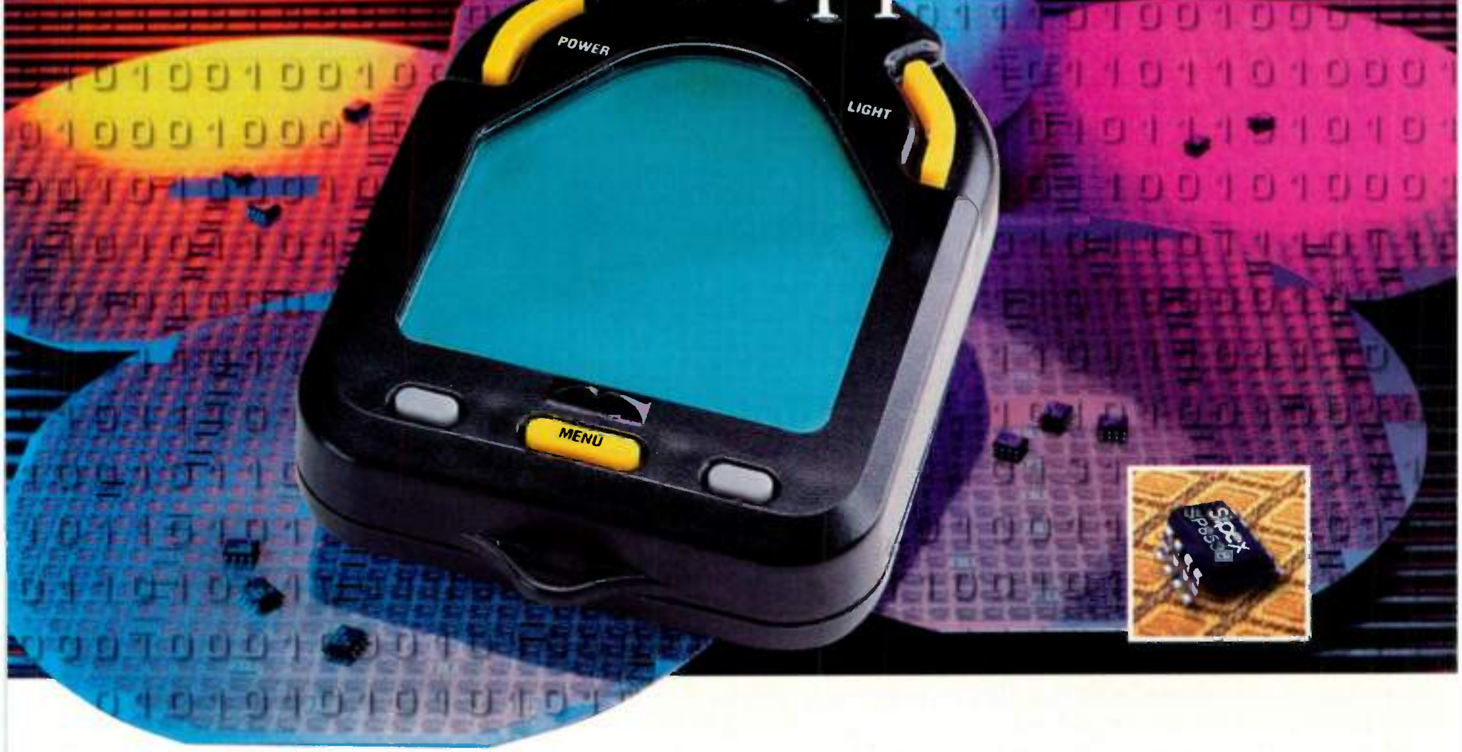

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for the VSC10 process. Up to six levels of metal interconnections with tungsten plugs and chemical-mechanical polishing providing planarization, can be deposited on pitches as small as 0.85 μm, and shallow-trench isolation is used to minimize transistor-to-transistor spacing, allowing designers to pack up to 40,000 gates per mm^2 *(Fig. 1b)*. Rather than focus on DRAM technology for on-chip storage, designers at VLSI Technology shrunk the static RAM memory cell to less than 10.5 μm^2, which would allow a considerable amount of memory to be integrated on the chips.

On the other side of the Pacific, Hitachi has released the HG73M cell-based ASIC design suite. The cell-based design approach integrates up to 140 Mbits of DRAM (with 100-MHz system operation) with high-speed 16-bit H8S or 32-bit SuperH RISC processors, and 5 million logic gates that can operate at 150 MHz. For the DRAM blocks, Hitachi designers developed a micro-module architecture that lets system designers more tightly match memory module size on the custom chip to the needs of the application. Each embedded DRAM block can be configured with 1 to 4 Mbits in 256-kbit increments, and multiple blocks can be concatenated or used independently on the chip. Embedded flash memory can be added to chips designed with the HG73M process, but initially, the choice will be one or the other. A future process enhancement will allow designers to mix logic, DRAM, and flash memory on the same chip.

Gate arrays, embedded arrays, and cell-based designs can be done with the TxC6000 Timeline Technology 0.18-μm CMOS process that Texas Instruments (TI) unveiled last year. The TEX6000 embedded array family and the TSC6000 standard-cell-based family allow designers to craft custom solutions that very efficiently use silicon with large blocks such as DSP chips, network control and interfaces, and 8- or 10-bit video ADCS and DACs.

The TI process is targeted at low-power applications and employs a high-density cell architecture that will allow a 90% reduction in power versus existing ASIC products by running the logic core at levels below 1-V and using small-swing I/O levels. With the core running at 1.8 V, the logic gates typically dissipate about 25 nW/MHz, and can operate with loaded gate delays of about 60 ps (fanout of 2). Up to 30 million gates and 1800 I/O signals can be integrated and then interconnected with up to six levels of metal.

Modularity For Flexibility

A highly modularized process approach developed at Lucent Technologies allows precision analog circuitry to be integrated side by side with biCMOS structures, flash memory, high-density SRAM, and, by mid-1998, blocks of embedded DRAM. Based on 0.25-μm minimum feature sizes, the modular process has a base number of masks required for standard CMOS logic (17 masks). Designers can then incrementally add technology-specific steps in the process flow to integrate biCMOS circuits, flash memory, or precision analog functions *(Fig. 2)*. The latest version of the process also is more mask-efficient than the company's previously released 0.35-μm process, requiring fewer mask steps, thereby producing slightly higher yields.

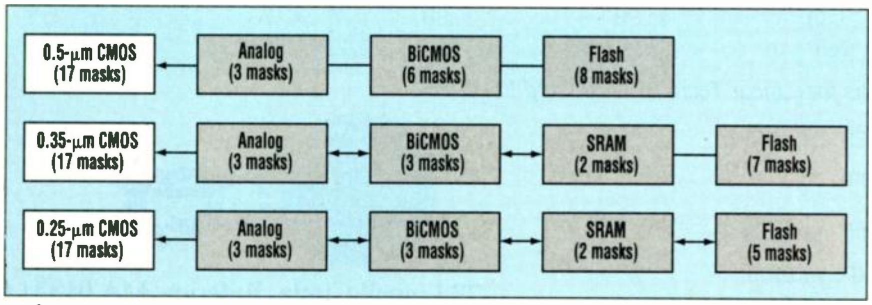
Two versions of the modular process are available—the LV250C series, which is optimized for 2.5-V operation; and the HL250C, which is optimized for 3.3-V systems. The LV series employs drawn gate dimensions of 0.24 μm and logic gates in the family consume 120 nW/MHz, while the HL series has 0.32-μm minimum features and its logic gates consume about 210 nW/MHz apiece. Top operating clock frequencies of the families are 300 and 250 MHz, respectively, for the LV and HL options. For LV-family designs, the memory option list includes up to 4 Mbits of SRAM, 8 Mbits of flash, up to 8 Mbits of ROM, and 4 to 8 Mbits of embedded DRAM. It also includes compiler-based memories such as multiport SRAMs, FIFOs, CAMs, and register files that are part of the company's Silicon Suite design library.

It's also possible to mix and match megagates of logic, megabits of DRAM, flash memory, and analog functions on a chip using 0.35- and 0.25-μm processes from Motorola, SGS-Thomson, and Symbios Logic. Motorola, however, has shifted away from offering generic ASIC design capabilities to the open market. Instead, it has distributed its process know-how and tools to company divisions that focus on market segments (consumer, communications, computing, etc.). Designers can then draw on the ASIC resources to craft system-on-a-chip solutions for sale as a "catalog" item, or custom solutions to fit a specific customer's needs.

Both SGS-Thomson and Symbios (in conjunction with its parent company, Hyundai Electronics Industries) have created 0.35-μm CMOS processes and library and tool suites that will allow them to craft ASICs with up to 2 Mbits of DRAM and over 1 million gates. The SGS HCMOS6 and the Symbios SYM9 processes are optimized for 3.3-V operation, employ up to five levels of metallization, and offer 5-V tolerant I/O lines.

The CB45000 cell library developed by SGS-Thomson for the HCMOS6 process includes over 500 small-scale logic cells and a wide range of complex functions such as DSP cores and 32-bit RISC microprocessors. Special attention was paid to testability. The library supports JTAG boundary scan and includes the necessary macrocells for both edge- and level-sensitive scan design. Built-in self-test options also are available for the blocks of memory created by memory-generation tools.

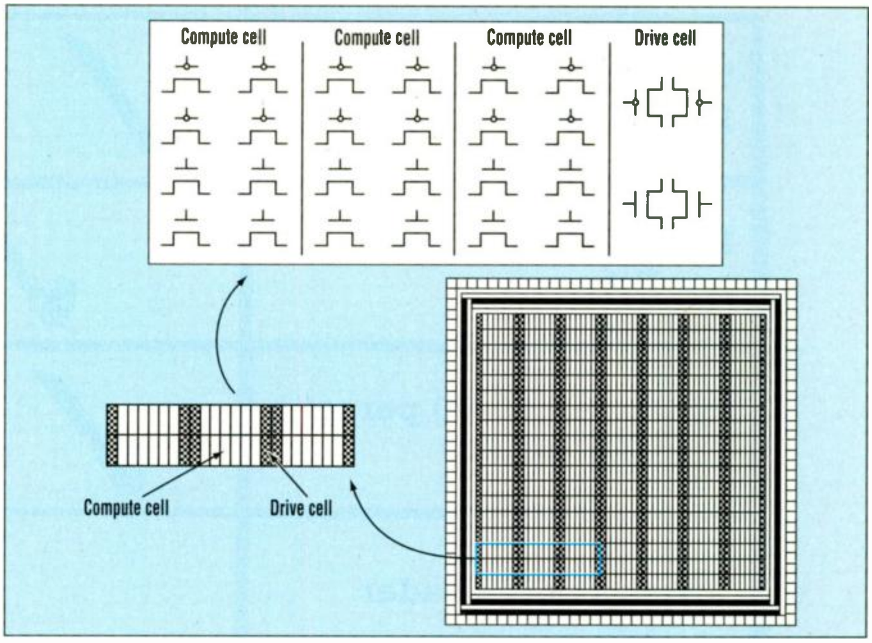
The design library developed by Symbios for its SYM9 process includes over 325 digital core cells including SCSI storage controllers, data networking building blocks, and many



2. This modular process flow, which starts with a 17-mask base, allows Lucent Technology to craft 0.25-μm ASICs. Steps can be added for integrating analog functions, biCMOS circuitry, flash memory, and high-density SRAM on the same chip.

other functions, and an extensive selection of mixed-signal cells. Symbios and Hyundai also are collaborating to develop the next-generation 0.25-µm process for denser circuits.

Also in place at IBM is a 0.25-µm ASIC capability based on a process referred to as SA-12. The process allows designers to pack up to about 3.5 million usable gates on a chip along with large blocks of static RAM, RISC processor cores, and other functions. Optimized for 2.5-V operation, it can interface to systems with 3.3-V I/O signals. Individual gates in the series dissipate about 80 nW/MHz for the low-power library, while the standard library gates consume about 180 nW/MHz. Prior to the release of the process, IBM released the CMOS 5X process, which employs 0.35-µm minimum drawn dimensions and could integrate up to about 1.6 million usable gates.



3. The cell-based array architecture in OKI Semiconductor's 0.35-µm cell-based and gate-array based designs consists of several blocks of compute cells. Each cell contains eight transistors optimized for logic functions (four p- and four n-channel devices) grouped with one drive cell that contains two p- and two n-channel devices optimized to handle heavy loads. These compute and drive cells are then "mirrored" to form larger tiles that are then laid out on the chip.

DRAMs Go Synchronous

Allowing blocks of compiled SRAM and embedded synchronous DRAM on its gate arrays or in its cell libraries, NEC has crafted three families of logic circuits, all based on a 0.18-µm (effective gate length) process—the CB-C10 series of cell-based circuits, the EA-10 series of embedded arrays, and the CMOS-10 series of gate arrays. The EA-10 and CMOS-10 families can support complexities up to 7 million gates, while the CB-C10 process allows up to 20 million gates on a chip. For high-performance systems, the chips can operate at clock speeds of 300 MHz and on a per-gate basis consume as little as 40 nW/MHz when powered by a 2.5-V supply. Second-generation cell libraries and silicon will be recharacterized for operation at 1.8 V for lower-power operation.

One unique aspect of NEC's design is a compact I/O buffer that can be laid out on a 40-µm pad pitch. That results in a maximum I/O density of over 2000 I/O pads per chip. And, like most other ASIC offerings, the I/O signal modes available on the chip include low-voltage differential signaling, high-speed transceiver logic, the PentiumPro version of Gunning transceiver logic (GTL+), pseudo-ECL, stub-series transceiver logic, Rambus, and popular bus interfaces such as USB, IEEE 1394, PCI, and AGP (advanced graphics port).

A third-generation ASIC process based on 0.25-µm features, the TCD-40, was released earlier this year by Toshiba to make the 1TDRAMASIC family of ASICs. It allows up to 128 Mbits of single-transistor (1-T) embedded synchronous DRAM (based on a trench-capacitor storage cell) that can operate at clock rates of 166 MHz. Because the trench cells are in the silicon rather than on top of the silicon, they're inherently more immune to noise and soft errors and provide a more-planar topology onto which additional layers of oxide and metal can be deposited. Both embedded-array (TCD40E) and standard-cell (TCD40C) design options are available.

Although not offering the millions of gates that other companies claim to deliver, Toshiba expects that a typical chip would pack about 410k usable gates and 32 Mbits of memory. The logic gates are available in two performance options—high speed and standard, with the high-speed option offering 80-ps loaded gate delays, and the standard version providing 113-ps loaded delays (2-input NAND with a fanout of five). The standard logic family is designed for operation from a 3.3-V supply, while the high-speed option operates from a 2.5-V supply. Power consumption for the logic gates is typically 290 nW/MHz for the standard family and about 170 nW/MHz for the high-speed series.

The TCD40 process also has a slightly less-dense cousin based on 0.35-µm minimum features that can also handle the single-transistor-cell DRAM blocks—the TCD20 series, which allows up to 32 Mbits of embedded synchronous DRAM and can operate at 133 MHz. For logic-intensive applications, a 3-T DRAM memory cell that doesn't require the trench processing can be used in lieu of the 1-T cell on the 0.35-µm process—the TC220E/C series. The penalty is lower density and lower performance—only 1 Mbit of the 3-T based DRAM that operates in an EDO access mode can be embedded on a chip. An upcoming process will shrink features to 0.25 µm and allow up to 2 Mbits of 3-T DRAM storage to be integrated.

Banking on its own DRAM capabilities, Samsung also has crafted an ASIC design suite. The suite is based on its KG gate arrays, the STD90 standard cell series, and the MDL90, a merged DRAM and logic process that allows up to 24 Mbits of embedded synchronous or EDO DRAM to be integrated with several million gates of logic. The initial versions of the processes are implemented with 0.35-µm minimum features and operate from 3.3-V supplies

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yet offer 5-V tolerant I/O lines, or from 2.5-V supplies with 3.3-V tolerant I/O signals. With the process, functions such as the ARM7TDMI (Thumb) processor can run at 60 MHz, while a core like the Oak DSP can clock at 80 MHz—both a 50% speed improvement over versions fabricated in the company's 0.5-µm process.

Already offering products with embedded DRAM, Mitsubishi Electric offers its 0.35-µm design library that includes a 32-bit RISC processor, the M32R/D, as well as many other megacells. Unveiled last year, the process allows the integration of up to two million usable gates and some of the shortest gate delays for a 3.3-V technology—just 101 ps. Cells in the library offer four levels of speed and power options so that designers can optimize designs for either high speed or low power—per-gate power dissipation is 900 nW/MHz for the highest-performance option.

Clock Distribution Critical

Available as either gate arrays, embedded arrays, or a cell-library, the technology includes a high-performance clock distribution approach that employs a patented fishbone-like clock drive grid and a proprietary clock driver. The driver can power 10,000 flip-flops with a worst-case skew of less than 100 ps, and the clock grid can be

Unifying The System-Chip Industry

The Virtual Socket Interface (VSI) Alliance consists of many companies that have banded together to represent four industry areas: electronic design automation (EDA), systems companies, ASIC suppliers, and intellectual property (IP) or software providers. The Alliance's goal is to unify the system-on-a-chip industry and the technical standards required to enable the mixing and matching of IP from multiple sources. This unification is expected to increase the system-chip industry growth and enable better, faster, more complex chips to be designed in less time, explains John B. Gallagher, marketing director, CAD and design methodology, LSI Logic Corp., Milpitas, Calif.

According to its charter, the Alliance is targeted at defining, developing, authorizing, testing, and promoting open standard specifications relating to data formats, test methodologies, and interfaces. By doing so, it believes it will be easier, more expeditious to mix and match and, otherwise, reuse IP blocks from different companies to design and develop system-level ICs.

On the other hand, the charter clearly states that the Alliance doesn't intend to develop specifications relating to the internal design of IP blocks, functional architectures of subsystem components, fabrication processes, and methods, algorithms, or techniques for EDA tools. However, the organization has set forth the idea of creating intra- and inter-company worldwide IP networks intended to facilitate quick identification, evaluation, exchange, and design-in of IP in the form of system-level macros, cores, or megacells.

According to its published plans, states Gallagher, the Alliance is expected to develop open IP design interface and productization standards. It is said the group will employ a rapid prototyping approach to the development of de facto standards that combine practical design experiences of semiconductor vendors, systems companies, independent IP providers, and EDA vendors. Standards work has begun with the Alliance's baseline proposal called the virtual socket interface.

The Alliance's most promising role is to provide a common language and forum for companies involved in IP creation and use. Another role is for it to be a standards-setting organization to establish test and integration processes for IP. The interoperability of IP has a definite need to be defined and rigorously implemented. As OEMs obtain IP from various sources, they will encounter issues dealing with test, design methodology, and with the level of interaction and support required for various abstractions created for the cores themselves. Setting up this level of standardization is a step in the right direction and is essential to help the industry grow and develop even further.

In the pursuit of these admirable goals, warns Gallagher, wrong directions can be inadvertently taken. For example, some members may unfortunately view the Alliance as a repository of free IP exchange across any and all companies. Investments many companies have made in their IP is too great to share freely. Of course, this precludes exchanging IP based on paid licensing. More to the point, a $5000 membership should not provide open access to IP portfolios worth billions of engineering dollars.

Safeguarding high-value IP is paramount, continues Gallagher. Veteran ASIC suppliers have worked closely with major EDA vendors for years to put in place encryption schemes and protection processes for IP within third-party design environments. The more value the IP has, the more protection it demands because it is a vital element in an ASIC vendor's business strategy.

Most ASIC vendors and system-on-a-chip suppliers focus primarily on developing IP tuned to their unique process technologies. Then, at secondary and tertiary levels and where it makes good business sense, they license IP from other vendors to provide systems customers the proper blend of embedded functions to comply with their engineering requirements. Thus, it is important for the Alliance, as it moves further into its goals, that clear delineation be made between high-value IP and what can be regarded as mid-to-low value IP that is regularly licensed among various companies.

Alliance members or chipless EDA vendors that offer free IP over the World Wide Web generally don't have high-value IP. In this deep-submicron technology era, it does not make good business sense for OEMs to leave major IP and technology decisions to newcomers who have not resolved many emerging issues dealing with high-value IP.

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segmented into several independently clocked subgrids to ease chip layout. The fishbone design includes a built-in, self-balancing clock load function that helps minimize clock skew. The company offers high-performance PLL megacells that have a lock range of 60 to 200 MHz (at 125 MHz, the internal clock has a jitter of less than 100 ps).

Also pushing its process technology to 0.35 µm is Oki Semiconductor. It offers a combination of cell-based and sea-of-gates ASIC capabilities as part of its MSM13Q0000/MSM14Q0000 families. Optimized for 3.3-V operation, the ASIC structures are based on the cell-based array architecture developed by Silicon Architects (now part of Synopsys Inc.). The CBA structures are supported by a library of macros optimized for logic synthesis. Memory blocks can be created with memory compilers that can generate single- and dual-ported RAMs.

In the CBA architecture, groups of compute and driver cells are set up in "mirrored" subarrays on the sea-of-gates chips *(Fig. 3)*. The compute cells

Verifying System-On-A-Chip Designs

Ideally, designers implementing systems-on-a-chip would like to verify an entire design in one shot and achieve complete first-time functional correctness of both digital and analog circuitry. However, no single EDA tool or algorithm can accomplish this. Consequently, systems engineers have to resort to dividing the design into different parts, often simulating each one separately.

This scenario, explains Tedd Corman, director of business systems development at Precedence Inc., Campbell, Calif., splinters into two major issues, which in turn pose certain challenges to the systems engineer. First, there are multiple technologies involved in system-on-a-chip designs: different analog and digital blocks, communications blocks, DSP, embedded processors, dataflow blocks, a myriad of other cores, and lesser megacells and cells. Second, there are multiple vendors supplying specific solutions for design verification of each of those different technologies. For example, there's a vendor with simulation expertise for the communications block; another has know-how at the transistor level for power and timing analysis; and yet another has specific expertise at gate- and behavioral-level analysis.

Each of these two issues, continues Corman, independently or in combination, prevent designers from simulating the system-on-a-chip. Either there are no well-defined interfaces between the technologies required—analog and digital, for instance—and/or simulators designed for each technology are incompatible with each other. As a result, designers use assumptions to bridge the gaps between technologies and simulators while verifying, in isolation, each piece of the system-on-a-chip.

While the assumptions made may initially seem benign, they can lead to design verification results that are inaccurate in subtle but critical ways. For instance, erroneous results of a functional analysis may be used to stimulate transistor-level or timing or power analysis. That analysis may indicate total power consumption at a certain level and as a result a certain type of packaging technology is selected and the design fabricated. When the first chips arrive, they may initially check out "OK," but later in the field, could show signs of premature failure due to overheating under certain conditions.

To avoid such a scenario, system designers must pick and choose model technologies, simulators and simulation methodologies very carefully. Critical questions to ask include: Where do simulation models come from? In what languages are those models written? Do the languages provide enough accuracy? And most importantly, are they compatible with other modeling techniques used and how will the different models interact? This last question is affected most by the simulation methodology chosen.

The most prevalent methodology is to separately run multiple simulators for each type of model used in the verification process. This minimizes concern about model interaction, but only yields information specific to the blocks of the design for which the individual simulators have run. In this instance, the integrity of the simulation results are questionable since assumptions must be made about the relationship between the simulators for different model types. The designer is not given a complete picture of the entire design's performance or correctness.

Another simulation approach that is equally as taxing and challenging is the so-called "gold standard" or designated simulator of choice. This can be either a proprietary, in-house developed tool or an agreed-upon commercial standard. In the latter, designers are trained and expected to use the particular simulator, even if it is less than optimal for a given design flow. Sometimes, costs associated with using a simulator other than this standard are prohibitive—in such instances, designers may have no alternative other than to use inadequate simulation models to avoid the cost of retraining and buying new simulation tools.

There is a third alternative. A growing number of designers are moving toward co-simulation as the more efficient way for verification. Co-simulation extends conventional simulation so that models or intellectual property from multiple sources, multiple levels of model abstraction, and multiple vendors' simulation tools can be used together, simultaneously.

Corman explains "co-simulation is the real-time connection of two or more simulators linked by a synchronization algorithm built into a simulation backplane. These backplanes use standard protocols that are technologically independent of any simulator that has been integrated into the simulation environment. This methodology opens the door to unified control and permits the system engineer to expand or change the simulation configuration, but without retraining or changing the design verification flow. Design problems can be identified early before being propagated throughout the design. Co-simulation provides more comprehensive verification with minimal overhead. That enables designers to obtain reliable verification without making dangerous assumptions.

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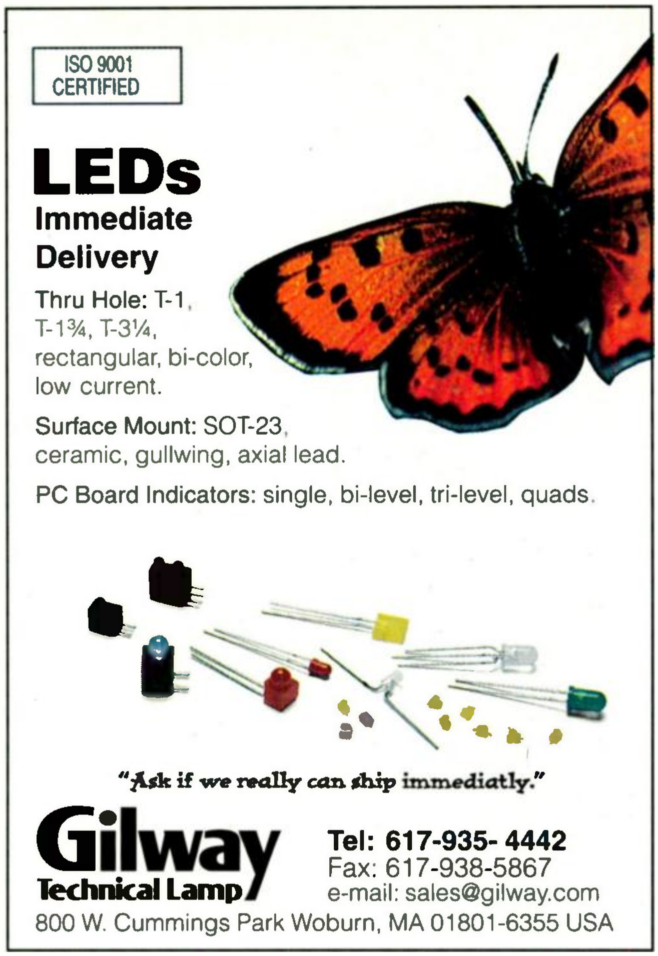

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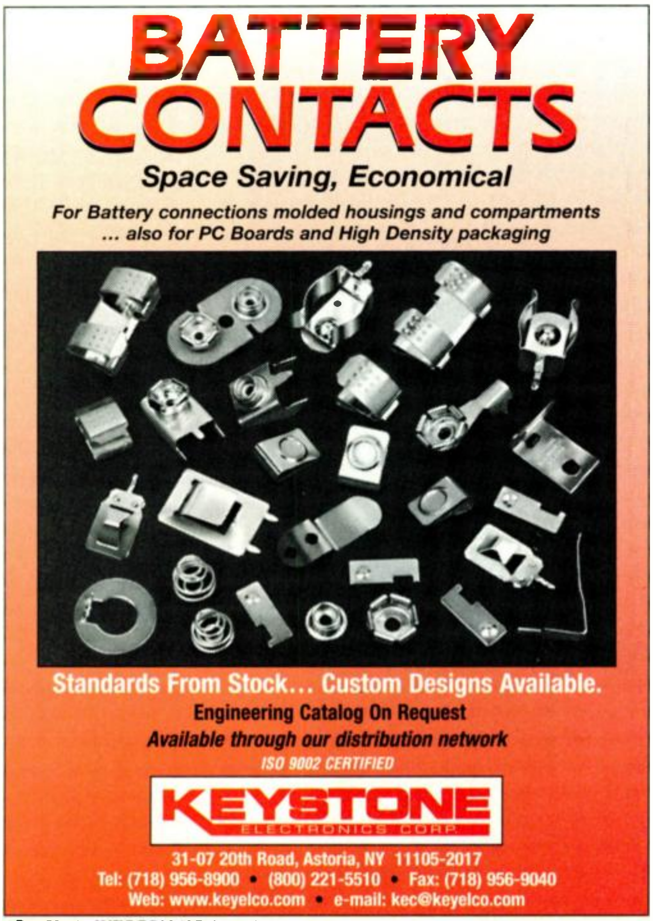

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each consist of eight transistors (four p- and four n-channel devices) optimized for logic, while the driver cells contain four larger transistors (two p- and two n-channel devices) that are optimized to drive heavy loads. On the fixed gate-array options, arrays with over 1 million raw gates are available. With four layers of metal interconnections, the company estimates the usable gate count at just over 60%. For cell-based designs, the company offers a large variety of megacells, including ARM RISC processors, and synchronous and asynchronous memory blocks.

Trimming Standby Power

For low-voltage systems, designers are looking at potential solutions to the problem caused by lowering the threshold voltage. The threshold has to be lowered to allow for low-voltage operation, but as a result, leakage current increases, and that does not bode well for portable systems. Thus, new schemes are being examined—one approach creates variable thresholds in which on-chip circuitry senses the state of the logic and will switch the threshold level of the transistors in the logic circuits to the appropriate value. When the logic is off, the threshold voltage is increased, and when the logic is active, the threshold voltage value is decreased. Several experimental chips have been fabricated to explore this scheme, and it is expected it to be practical by late 1999.

One such project at Toshiba started with a 0.3-µm gate array and switches the threshold level between 0.7 and 0.3 V, depending on the logic state. The scheme employs MOS switch transistors for the active mode and a self-substrate bias circuit for the standby mode. This scheme keeps the leakage levels low during standby. The key concern about the approach is the time required to switch between threshold values—it currently takes about 100 µs to switch from active to standby, and just 100 ns to switch from standby to active values. The active-to-standby time must be reduced to take advantage of the technology.

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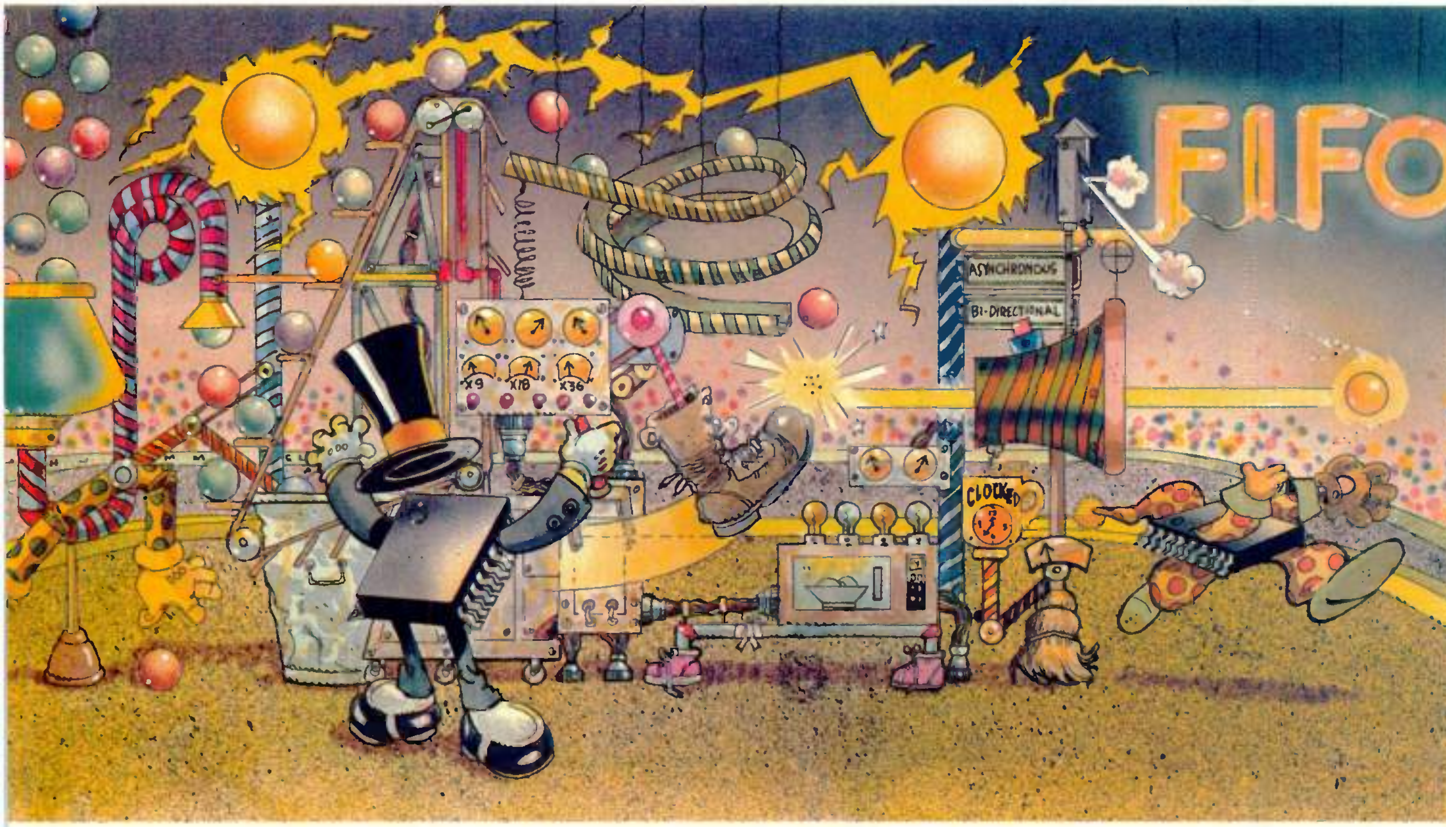

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QS7204	4K x 9 with Buffer Memory	32, 28
Clocked x9 FIFOs		
QS72211	512 x 9 Parallel Synchronous	32
QS72221	1K x 9 Parallel Synchronous	32
QS72231	2K x 9 Parallel Synchronous	32
QS72241	4K x 9 Parallel Synchronous	32
Clocked x18 FIFOs		
QS72215	512 x 18 Parallel Synchronous	68
QS72225	1K x 18 Parallel Synchronous	64
Clocked x36 FIFOs		
QS723611	512 x 36 x 2 Bidirectional Clocked FIFO with Dynamic Bus Sizing	144
QS723620	1K x 36 Clocked FIFO with Dynamic Bus Sizing	132
QS723621	1K x 36 x 2 Bidirectional Clocked FIFO with Dynamic Bus Sizing	144
QS725420A	256 x 36 x 2 Bidirectional Clocked FIFO	132, 144

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	POS-150	75-150	-103	-23	20	11.95
	POS-200	100-200	-102	-24	20	11.95
	POS-300	150-280	-100	-30	20	13.95
	POS-400	200-380	-98	-28	20	13.95
	POS-535	300-525	-93	-26	20	13.95
	POS-765	485-765	-85	-21	22	14.95
NEW	POS-900W	500-900	-95	-26	25	16.95
	POS-1025	685-1025	-84	-23	22	16.95
	POS-1060	750-1060	-90	-11	30*	14.95
	POS-1400	975-1400	-95	-11	30*	14.95
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*Max. Current (mA) @ 8V DC

Notes: Tuning voltage 1 to 16V required to cover freq. range. 1 to 11V for POS-25, 1 to 20V for POS-1060 to -2000. 3dB modulation bandwidth for POS-25 is 60kHz, POS-50 to -1025 is 100kHz, and POS-1060 to -2000 is 1MHz (all typ). Operating temperature range: -55°C to +85°C. 5V tuning models available. Consult RF/IF Designer's Guide or call Mini-Circuits.

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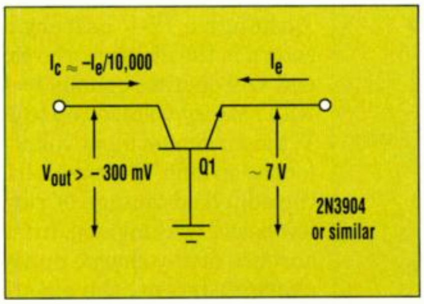
Circle 520

Single-Supply Op-Amp Input Bias-Current Cancellation

W. STEPHEN WOODWARD
Venable Hall, CB3290, University of North Carolina, Chapel Hill, NC 27599-3290; e-mail: woodward@net.chem.unc.edu.

Op-amp performance has advanced dramatically during recent years, but the relative advantages between bipolar input amplifiers and FET types remain the same. FET input parts are still characterized by superior bias current specifications, while bipolar devices retain the edge for better offset voltage tolerances. For example, no non-chopper FETs can match the 80 µV and 400 nV/°C numbers of the bipolar, single-supply LT1013A.

Unfortunately, the large 20-nA (typical) input bias requirement of the '1013 (although already better than most single-supply bipolar op amps) makes it unsuitable for many applications, such as low-level integrate-and-hold circuits, for which it would otherwise be ideal. Moreover, standard bias current cancellation tricks, tremendously effective techniques that are integrated on-chip in dual-supply amplifiers like the OP177 and LT1028, don't work for positive-supply-only devices because the input networks of single-rail amplifiers need a bias current sink. It's obviously impossible to sink current from an input pin that's already referenced to the negative rail. Obviously.



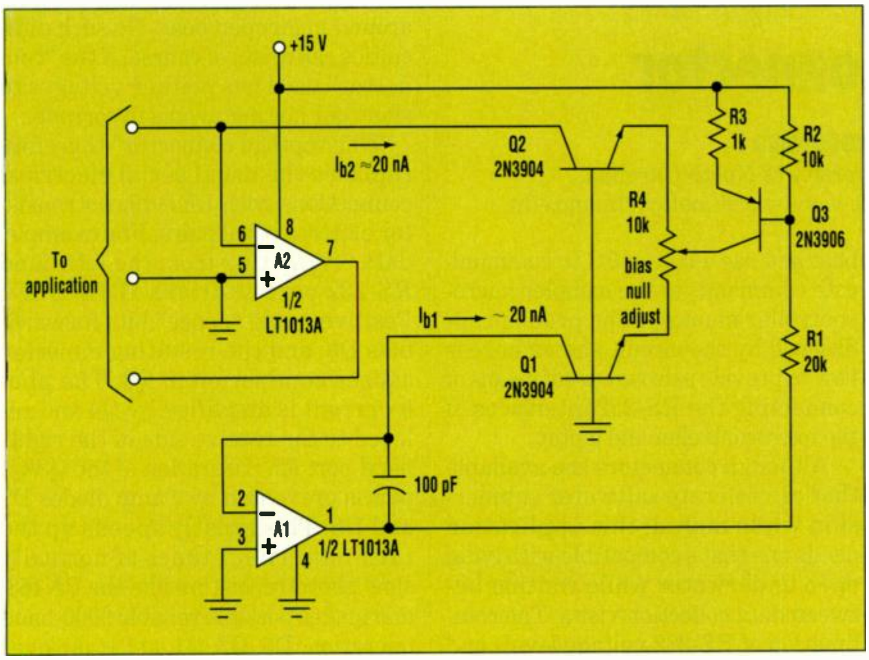
1. Presented last year in Bob Pease's April Fool's column (it actually appeared in *ELECTRONIC DESIGN's* March 18th, 1996 issue) as a brain teaser for readers, this circuit could actually be used to produce a tiny amount of negative current where no other negative voltage source exists.

At least I always *thought* this was impossible. But that was before I read Bob Pease's column (*"What's All This R-C Filter Stuff, Anyhow?"* ELECTRONIC DESIGN, *March 18, 1996, p. 123)* in which he presented a bizarre circuit *(Fig. 1)* as an April 1st joke brain teaser. Amazingly, if the base-emitter junction of any ordinary silicon npn transistor is forced to zener and thereby sink a positive emitter current (I_e), a small *negative* collector current ($I_c \approx -I_e/10{,}000$) will flow even if the collector is as much as a few tenths of a volt *below* ground! Good joke! The reader gets the definite impression, however, that Mr. Pease doesn't think this circuit has much practical potential except for baffling and confusing poor unsuspecting analog EEs. But I think it's perfect for making a tiny amount of negative current where no other negative voltage source exists.

This is exactly the function performed by Q1 and Q2 in Figure 2. A1 adjusts Q3's base voltage until the drive to Q1's emitter produces just enough negative collector current to balance the ≈ –20-nA bias current at A1 pin 2. By doing so, it produces a similar current at Q2's collector and, therefore, A2 pin 6. If R4 is adjusted to compensate for asymmetry between the A1-Q1 and A2-Q2 pairs, A2's bias can be nulled exactly to zero. Notice that the signal inversion provided by Q3 negates the inversion imposed by Q1 and Q2, where emitter-going-positive = collector-going-negative.

Changes in A1's and A2's bias currents due to temperature changes and aging can be expected to track well. And if Q1 and Q2 are closely coupled thermally, the nulling of A2's bias current will be stable with time and temperature. This makes bias-nulled A2 a terrific candidate for inverting-amplifier applications where both voltage and current offset errors are of critical interest.

No fooling.



2. Ideal for inverting-amplifier applications, this circuit acts a bias canceller for single-rail op amps, providing the bias-current sink needed by their input networks.

VOTE!

Read the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a $300 Best-of-Issue award.

Circle 521

Battery-Current Monitor Operates "Over The Top"

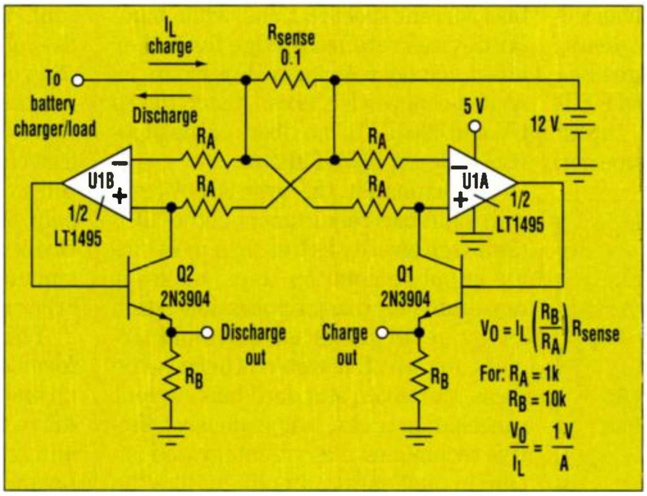
WILLIAM JETT
Linear Technology Corp., 1630 McCarthy Blvd.,
Milpitas, CA 95035-7417; (408) 432-1900; fax (408) 434-0507.

IFD WINNER

Klaus Achleitner, University of Cape Town, Dept. of Chemistry, Rondebosch 7700, Cape Town, South Africa. email: Klaus@psipsy.uct.ac.za. The idea: *"PM DC Motor Speed Control."* Novermber 18, 1996 Issue.

The bidirectional current sensor shown takes advantage of the extended common-mode range (greater than 90 dB) of the LT1495 dual op amp, to sense currents in and out of a 12-V battery while operating from a single 5-V supply *(see the figure)*. This is possible because U1 features "over the top" operation—the ability to operate normally with inputs above the positive supply.

During the charge cycle, op amp U1A controls the current in Q1 so that the voltage drop across R_A is equal to $I_L \times R_{sense}$. This voltage is amplified at the charge output by the ratio of R_A to R_B. During this cycle, amplifier U1B sees a negative offset, which keeps Q2 off and the discharge output low. During the discharge cycle, U1B and Q2 are active and operation is similar to the charge cycle. Although a 12-V battery is shown in the diagram, the circuit will operate equally well with battery voltages up to 36 V, the maximum input voltage for the op amp. The circuit has the added advantage of very low power consumption. In the absence of any charge or discharge current, the circuit draws only 2 µA, the quiescent current of the two amplifiers.



This bidirectional current sensor monitors both charge and discharge currents in battery-powered circuits.

Circle 522

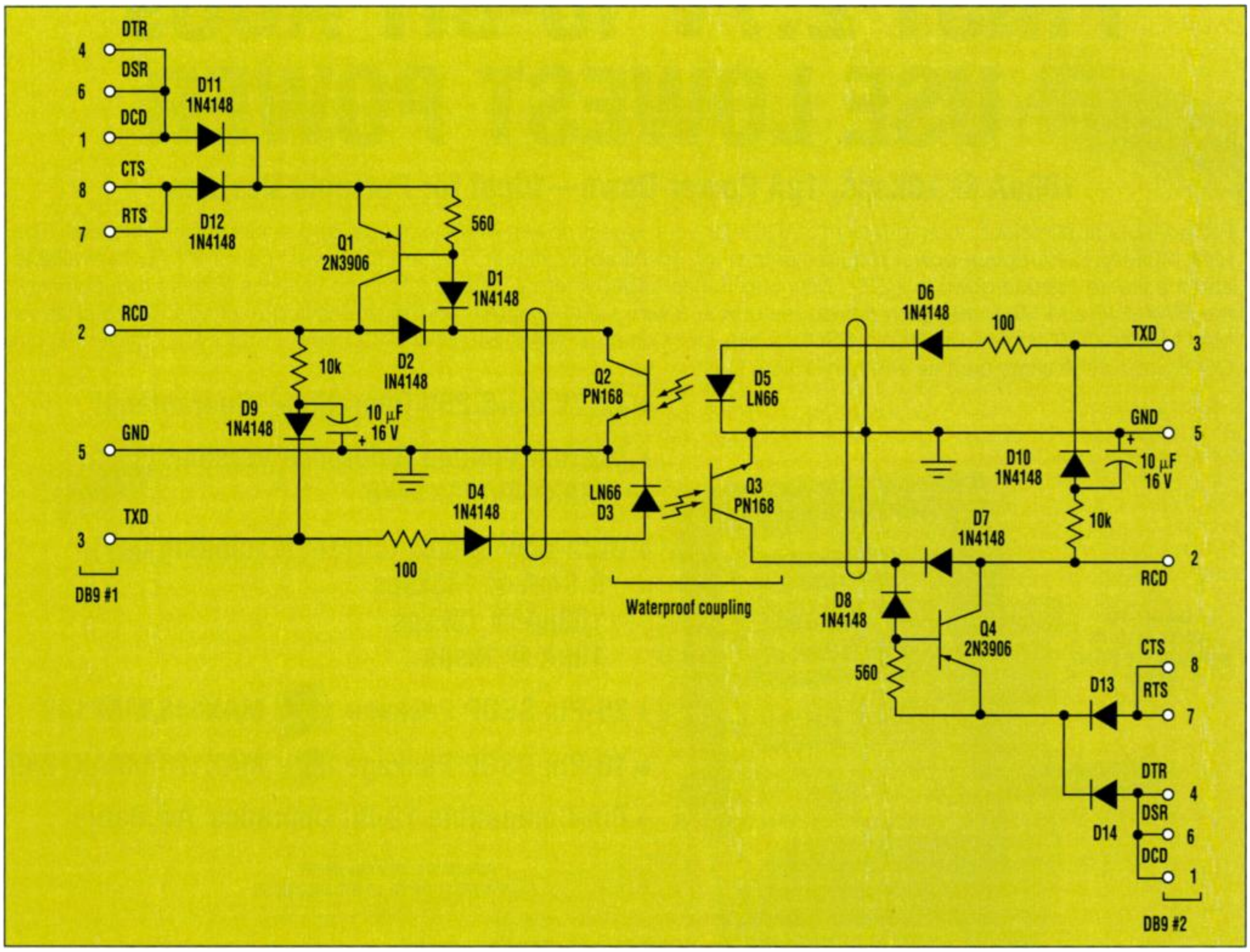
Full-Duplex Optical RS-232 Connector

W. STEPHEN WOODWARD
Venable Hall, CB3290, University of North Carolina,
Chapel Hill, NC 27599-3290; e-mail: woodward@net.chem.unc.edu.

Situations in which the reliability of data communications can benefit from optical isolation are rather common. But the circuit described here was designed in response to an application with the unusual need to optically couple the actual serial *connection* itself. In the application, microprocessor-controlled apparatuses are deployed at shallow underwater sites in river estuaries and salt marshes. These rigs are designed to collect gas samples from the estuarine sediment over time intervals ranging from days to weeks. Periodically, a field worker will visit the sampling sites in a small boat and use a laptop PC to communicate commands to the sampler microcontroller memory. The problem addressed by the circuit shown here is how to provide a drown-proof means of connecting the RS-232 interfaces of the microcontroller and laptop.

Although connectors are available that can tolerate saltwater submersion while mated, this application needs one that's compatible with lying open underwater while waiting between data collection visits. The combination of RS-232 voltage levels and water on connector pins will drive aggressive electrolytic corrosion processes capable of digesting even the best gold plating. Plus there's the fun prospect of trying to clean and dry a wet, salty connector while bobbing around in an open boat. No such difficulties can arise, of course, if the "connector" used has neither voltages to short out nor metal pins to corrode.

This "optical connector" therefore replaces the usual serial electrical connections with LED/phototransistor electrooptical pairs. For example, data originating from the left-hand RS-232 port #1 drives IRLED D3. Positive-going "space" bits forward-bias D3, and the resulting emission causes conduction in Q3. The photocurrent is amplified by Q4 and relayed to the receive side of the right-hand port #2. Saturation of the Q3/Q4 pair is prevented by clamp diodes D7 and D8. This greatly speeds up the turn-on/turn-off times of normally slow phototransistors like the PN168, and makes possible reliable 9600-baud operation. D5, Q2, Q1, etc., take over for data flow in the opposite direction. Assembly of the connector has all



A submersible optically isolated serial connector has neither voltages to short out nor metal pins to corrode.

active components except for Q2, Q3, D3, and D5 mounted in the electronic enclosures of their respective computers. Therefore, only the optical components themselves had to be separately waterproofed, which was accomplished using heatshrink tubing and waterproof glue. Minor modification of inexpensive AMP Inc. nylon connector bodies provided a mechanical foundation for mounting and holding the LEDs and phototransistors in adequate alignment to provide enough coupled gain—once the submerged connector is fished up and the seaweed shaken out, that is!

The optical connector should prove useful in any application in which a robust weather-and-waterproof, galvanically isolated, field-mateable connection is needed; not only submarine ones.

Circle 523

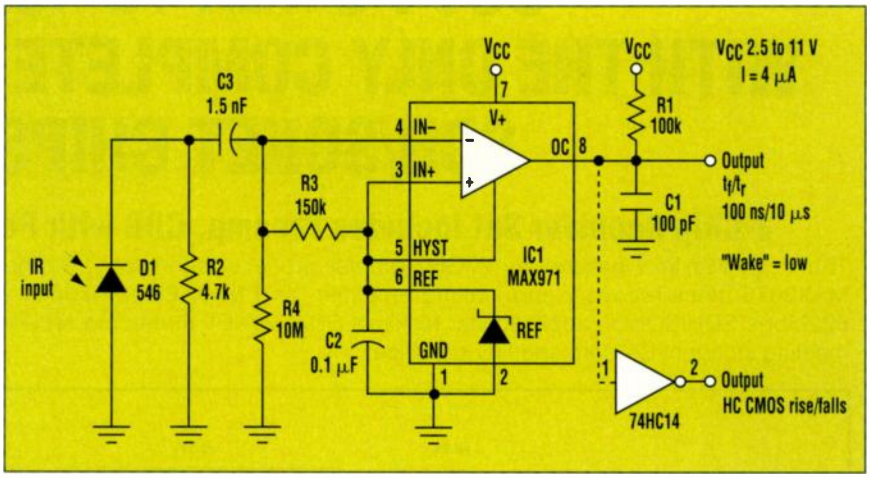
IR Sensor Wakes Up Larger System

JOHN WETTROTH
Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086; (408) 737-7600.

The sensor/monitor circuit shown draws so little supply current that it can remain on continuously in a notebook computer or PDA device *(see the figure)*. Its purpose is to “wake up” the host system when infrared (IR) signals are detected. The circuit's ultra-low current drain (4 µA maximum, 2.5 µA typical) is primarily that of the comparator/reference device IC1.

The circuit is intended for the non-carrier systems common in Infrared Data Association (IrDA) applications, and it operates with carrier protocols such as those of TV remote controllers and Newton/Sharp ASK (an Amplitude Shift Keying protocol developed by Sharp and used in the Apple Newton). The range for 115,000-baud IrDA is limited to about six inches, but for 2400-baud IrDA, it improves to more than one foot.

Bright flashes usually cause false



This low-quiescent-current circuit (4 μA maximum) interrupts the host processor when it detects an IR signal. Applications include IrDA-compatible devices, TV remotes and Newton/Sharp ASK.

triggers. Otherwise, the immunity to ambient light is very good. To handle occasional false triggers, the system simply looks for IR activity after waking and then goes back to sleep if none is present.

The sensor shown (D1), a relatively large-area photodiode packaged in an IR-filter material, produces about 60 μA when exposed to heavy illumination (and 0.4 V when open-circuited). Most such photodiodes are acceptable in this circuit. Operation is in the photovoltaic mode (without applied bias). This mode is slow and not generally used in photodiode circuits, but speed isn't essential here. The photovoltaic mode simplifies the circuit and saves a tremendous amount of power. In a more conventional (photoconductive) configuration, photo currents caused by ambient light and sourced by the bias network would increase the quiescent current about ten times.

V_{REF} and the R3/R4 divider introduce an 18-mV bias between the comparator inputs. Derived from the reference, this bias is independent of the supply voltage. To suppress 60-Hz/120-Hz hum and other low-frequency disturbances, C3 and the R3/R4 divider form a high-pass network whose cutoff frequency is 700 Hz. C3 is normally charged to V_{REF} minus the 18-mV bias, and any voltage produced by photocurrent through R2 adds to the voltage on C3.

Consequently, any IR signal across R2 that exceeds the 18-mV threshold trips the comparator and causes its output to go low (18 mV represents a good trade-off between range, noise immunity, and dc stability). The low value of R2 prevents saturation of the photodiode in ambient light. If saturation is an issue, the R2 value can be lowered further—with a penalty in sensitivity and a boost in speed.

The comparator's input offset voltage (10 mV maximum) sets worst-case extremes of 6 mV and 28 mV for the IR trip threshold, but this spread isn't as big an issue as one might imagine. Typical spreads are much smaller than the maximums, and typical IR signals generate more than 60 mV. A variation in offset affects the amount of overdrive, which therefore affects only the comparator's speed of response.

The circuit's output can trip a set-reset flip-flop or interrupt a sleeping processor. The optional HCMOS gate (preferably a Schmitt-trigger type) can improve the output rise/fall times with very little effect on the overall quiescent current.

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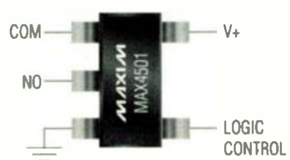
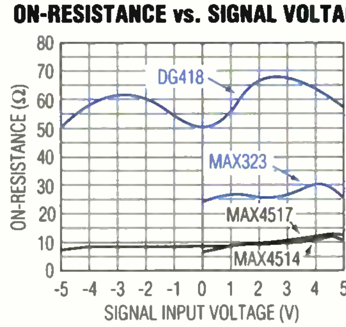
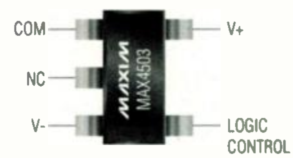


LOGIC INPUT	SWITCH STATE	
	MAX4501/14	MAX4502/15
Low	OFF	ON
High	ON	OFF



Low on-resistance reduces harmonic distortion in audio systems and reduces signal errors in data-acquisition systems.

Dual Supplies



LOGIC INPUT	SWITCH STATE	
	MAX4503/16	MAX4504/17
Low	OFF	ON
High	ON	OFF

PART	FUNCTION	OPERATING SUPPLIES (V)	ON-RESISTANCE (Ω max)	LEAKAGE CURRENT (nA max)	PIN-COMPATIBLE UPGRADE
MAX4501	SPST (NO)	+2 to +12	250	1	TC7S66F
MAX4502	SPST (NC)	+2 to +12	250	1	TC7S66F
MAX4503	SPST (NO)	±2 to ±6	250	1	DG418DY
MAX4504	SPST (NC)	±2 to ±6	250	1	DG417DY
MAX4514	SPST (NO)	+2 to +12	20	1	TC7S66F
MAX4515	SPST (NC)	+2 to +12	20	1	TC7S66F
MAX4516	SPST (NO)	±2 to ±6	20	1	DG418DY
MAX4517	SPST (NC)	±2 to ±6	20	1	DG417DY

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MAY 1998

IEEE/IAS Industrial & Commercial Power Systems Technical Conference (I&CPS), May 4-7. Edmonton, Alberta, Canada. Contact Marty Bince, Modicon Canada Ltd., 5803 86th St., Edmonton, Alberta T6E 2X4, Canada; (403) 468-6673; fax (403) 468-2925.

IEEE International Conference on Acoustics, Speech & Signal Processing (ICASSP '98), May 12-15. Seattle Convention Center, Seattle, WA. Contact Les E. Atlas, Dept. EE(FT 10), University of Washington, Seattle, WA 98195; (206) 685-1315; fax (206) 543-3842; e-mail: atlas@ee.washington.edu.

JUNE 1998

IEEE/MTT-S International Microwave Symposium (MTT 98), June 7-12. Baltimore Convention Center, Baltimore, MD. Contact Steven Stitzer, Westinghouse Electric Corp., P.O. Box 1521, MS 3T15, Baltimore, MD 21203; (410) 765-7348; fax (410) 993-7747.

USENIX 1998 Technical Conference, June 13-17. Marriott Hotel, New Orleans, LA. Contact USENIX Conference Office, 22672 Lambert St., Suite 613, Lake Forest, CA 92630; (714) 588-8649; (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

JULY 1998

IEEE International Geoscience & Remote Sensing Symposium (IGARSS '98), July 6-10. Sheraton Seattle, WA. Contact Tammy I. Stein, IGARSS Business Office, 2610 Lakeway Dr., Seabrook, TX 77586-1587, (281) 291-9222; fax (281) 291-9224; e-mail: tstein@phoenix.net.

IEEE Power Engineering Society Summer Meeting, July 11-17. Sheraton Hotel, San Diego, California. Contact Terry Snow, San Diego Gas & Electric, P.O. Box 1831, San Diego, California 92112; (619) 696-2780; fax (619) 699-5096.

IEEE Power Engineering Society Summer Meeting, July 12-16. Sheraton San Diego Hotel & Marina, San Diego, California. Contact Terry Snow, San Diego Gas & Electric, Post Office Box 1831, San Diego, California 92112; (619) 696-2780; fax (619) 699-5096; e-mail: t.snow@ieee.org.

SPIE's Annual Meeting & Optical Instrumentation Show, July 19-24. San Diego, CA. Contact SPIE Exhibits Dept., P.O. Box 10, Bellingham, WA 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

IEEE Nuclear & Space Radiation Effects Conference (NSREC '98), July 20-24. Newport Beach, CA. Contact Jim Schwank, Sandia National Laboratories, P.O. Box 5800, MS-1083, Albuquerque, NM 87185-1083; (505) 844-8376; fax (505) 844-2991; e-mail: schwanjr@sandia.gov.

AUGUST 1998

AUTOTESTCON '98, Aug. 24-27. Salt Palace Convention Center, Salt Lake City, UT. Contact Robert Myers, Myers/Smith Inc., 3685 Motor Ave., Suite 240, Los Angeles, CA 90034; (310) 287-1463; fax (310) 287-1851; e-mail: bob.myers@ieee.org.

OCTOBER 1998

IEEE International Conference on Systems, Man, & Cybernetics, Oct. 12-14. Hyatt Regency La Jolla, La Jolla, California. Contact M.A. Jafari, Dept. of Industrial Engineering, Rutgers University, Post Office Box 909, Piscataway, New Jersey 08855; (908) 445-3627; (908) 445-5467; e-mail: jafari@gandalf.rutgers.edu.

NOVEMBER 1998

Photonics East & Electronic Imaging International Exhibition, Nov. 1-6. Boston, Massachusetts. Contact SPIE Exhibits Dept., P.O. Box 10, Bellingham, WA 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

Voice, Video & Data Communications Conference & Exhibition, November 1-6. Boston, Massachusetts. Contact SPIE Exhibits Dept., Post Office Box 10, Bellingham, Washington 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhbits@spie.org.

IEEE Global Telecommunications Conference (Globecom '98), Nov. 9-13. Sydney, Australia. Contact Sam Reisenfeld, School of Electrical Engineering, University of Technology, Sydney, P.O. Box 123; Broadway, NSW 2007, Australia; +61 2-330-2435; e-mail: samr@trnasmit.ee.uts.edu.au.

DECEMBER 1998

12th Systems Administration Conference (LISA '98), December 6-11. Marriott Hotel, Boston, Massachusetts. Contact USENIX Conference Office, 22672 Lambert Street, Suite 613, Lake Forest, California 92630; (714) 588-8649; (714) 588-9706; e-mail: conference@usenix.org; Internet: http://www.usenix.org.

JANUARY 1999

Annual Reliability & Maintainability Symposium (RAMS), Jan. 19-21. Washington Hilton, Washington, DC. Contact V.R. Monshaw, Consulting Services, 1768 Lark Lane, Cherry Hill, NJ 08003; (609) 428-2342.

IEEE Power Engineering Society Winter Meeting, Jan. 31-Feb. 4. New York, NY. Contact Frank Schink, 14 Middlebury Lane, Cranford, New Jersey 07016; (908) 276-8847; fax (908) 276-8847.

FEBRUARY 1999

Photonics West, February 6-12. San Jose, CA. Contact SPIE Exhibits Dept., P.O. Box 10, Bellingham, Washington 98227-0010; (360) 676-3290; fax (360) 647-1445; e-mail: exhibits@spie.org.

IEEE International Solid-State Circuits Conference (ISSCC '99), February 15-17. San Francisco Marriott, San Francisco, California. Contact Diane Suiters, Courtesy Associates, 655 15th St., N.W., Washington, DC 20005; (202) 639-4522; fax (202) 347-6109; e-mail: isscc@coutesyassoc.com.

MARCH 1999

Southeastcon '99, Mar. 25-29. Marriott Resort Hotel, Lexington, Kentucky. Contact Don Hill, 1676 Donelwal Drive, Lexington, Kentucky 40511-9021; (606) 257-8487; fax (606) 323-1034; e-mail: d.w.hill@ieee.org.

MAY 1999

IEEE/IAS Industrial & Commercial Power Systems Technical Conference (I&CPS), May 3-6. Nuggett Hotel, Sparks, Nevada. Contact Kerry Flannigan, Sierra-Nevada Power Co., Post Office Box 10100, Reno, Nevada 89520; (702) 689-4848; fax (702) 689-4139.

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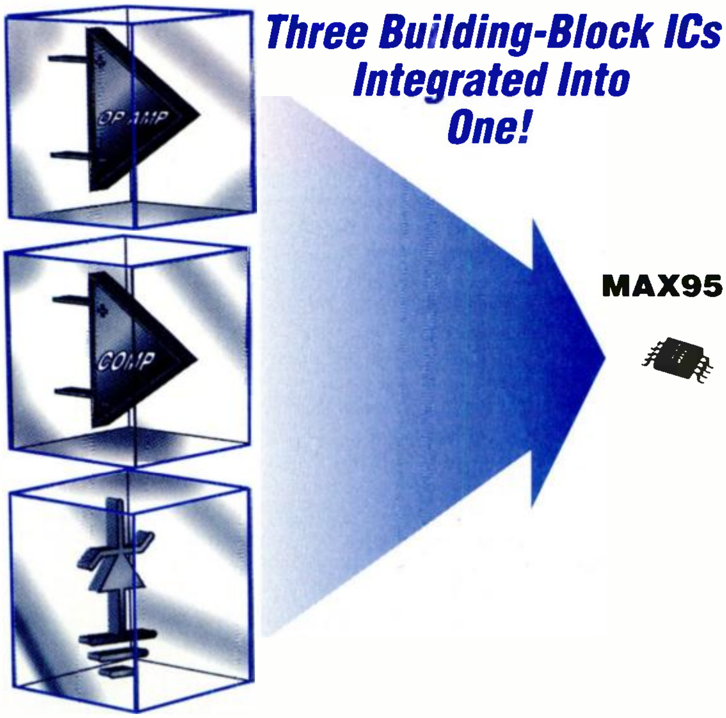

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MAX952		✓	✓	✓	2.7	7	$1.47	8-pin SO/DIP/µMAX†
MAX953	✓		✓		2.4	5	$1.19	8-pin SO/DIP/µMAX†
MAX954		✓	✓		2.4	5	$1.19	8-pin SO/DIP/µMAX†

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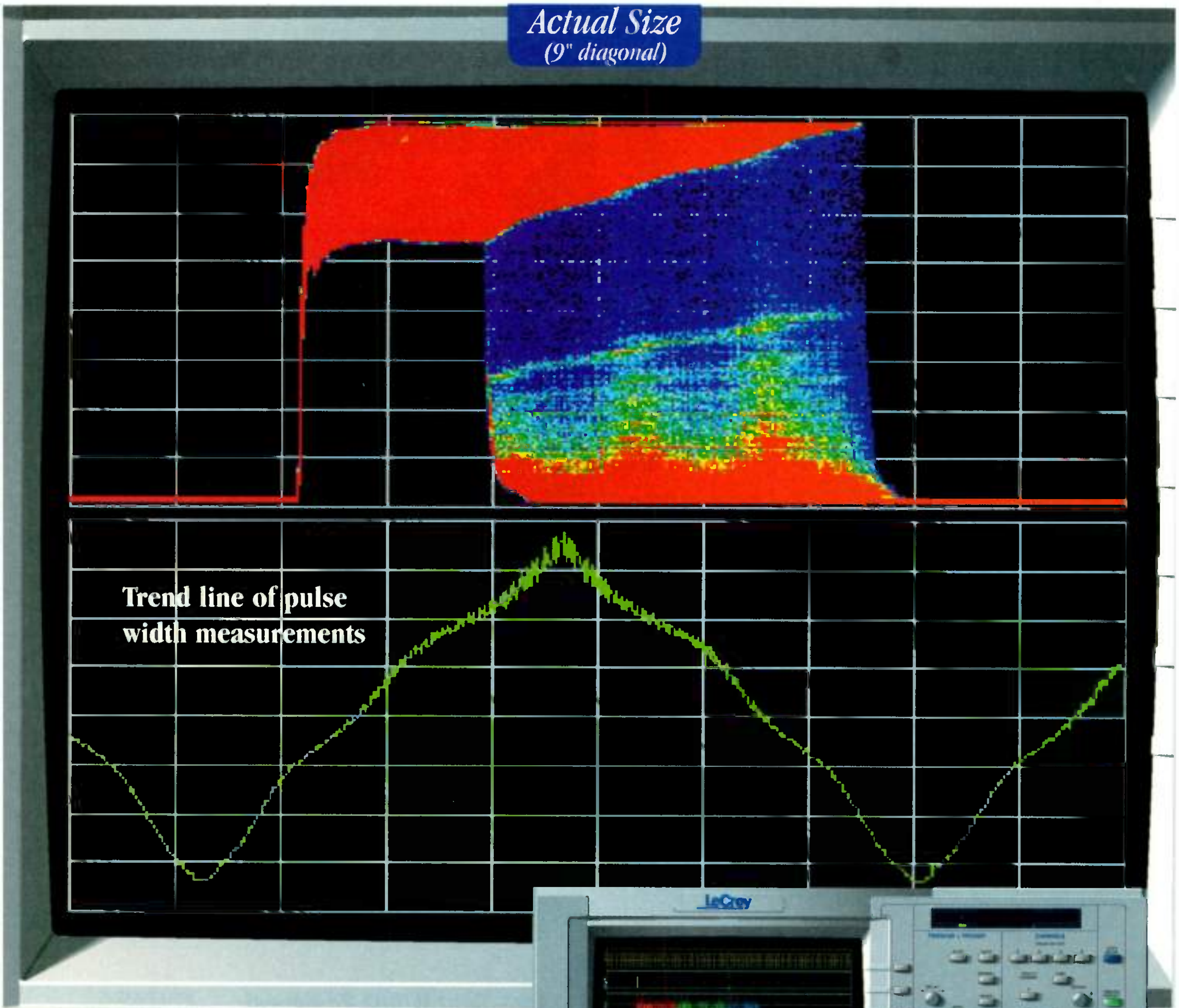

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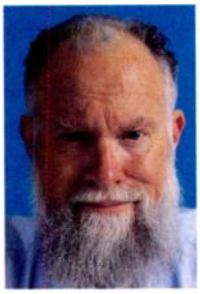
Bob's Mailbox

Dear Bob:

Silly Ideas That Work: Are you aware that the New York City subway system used incandescent bulbs in series strings of five so that they could be powered by 600 V from third-rail track power? To discourage bulb snatching, especially during the Great Depression, they also raised the bulb ratings to 135 V. This prolonged lamp life and made those 40-W bulbs so dim that it discouraged their pilferage.



They also had to introduce counter-clockwise Edison-base threads. That really put a stop to bulb-snatching! Most vandals gave up when the bulbs would not unscrew. Those who succeeded, quickly found that the bulbs were unusable at home. But I'll bet that didn't stop them from hawking them on the street to unsuspecting pedestrians!

On the down side, just like cheap Christmas tree light strings, when a string of five bulbs went dark, a transit worker would replace all five bulbs rather than attempting to locate the faulty one. When you consider that the probability of additional bulb failures in quick succession was high, replacing the whole lot was more efficient!

What Ya Don't Know Won't Hurt Ya: I prefer the charm of an oil or gas lamp with a mantle. You know those Coleman camping lanterns? Unfortunately, I made the mistake of buying a lovely little geiger counter made by a small company, Aware Electronics. The unit is shirtpocket sized and comes with software for data collection via a PC or with an optional counting/display module. It can power its GM tube (900 V dc) by stealing energy from a PC's serial port.

After running all over my neighborhood measuring residual radioactivity of clay coffee mugs, cut crystal glassware, the ledge in my garden, the radon in my water supply, I measured a spare package of mantles. Oops! The normal background count is 14.9 cpm, equal to 10 μR/hour. But the mantles produced almost 12,000 cpm, equal to 8 mR/hour! Almost 1000 X normal background! With 100 mR/year, the average annual human exposure to naturally occurring radiation, carrying an envelope of new mantles in your trouser pocket for 13 hours exceeds it! I heard a tale about someone doing that for weeks, having forgotten that it was there, until a nasty red rash developed on his buttock.

Inhaling the dust while changing the mantles, something thousands of camping enthusiasts have no doubt done, can be quite dangerous. Particulate can imbed in lungs, exposing delicate tissues directly to penetrating beta radiation and even more potent (greater ionizing capability due to mass), though less penetrating, alpha radiation. And you thought the cigarette manufacturers were the only ones hiding carcinogenic complicity!

Older mantles, like this package that I had on the shelf for years, contain thorium to enhance light emission. Thoriated tungsten is used in electron tubes to enhance electron emission. Anyhow, the stuff is very radioactive. When you change old, burned-through mantles, you have a crumbling mess of radioactive debris and dust! Coleman no longer uses Thorium in their mantles. So much for efficient romantic lighting!

IRA A. WILNER
Wilner Associates
via e-mail

For 600-V operation, I'd put four 155-V bulbs in series. These bulbs would be of ZERO value to ordinary consumers who have 115 V—quite dim—yet fairly efficient and bright on 150 V. But, when thorium is outlawed, only outlaws will have thorium??—RAP

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer
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3-V CMOS Gate-Array Family Claims Highest Density

The CLA200 series is a new family of ASICs that includes a range of standard, optimized, and embedded arrays. The ASICs, targeted at high volume power and cost-sensitive applications, are designed in a 3-V CMOS technology. With a gate density of 15,944 raw gates per square millimeter and the use of staggered pads, this architecture is claimed to provide the highest density available among 3-V ASIC solutions. The gate-array family offers 14 fixed-size arrays and up to 785,000 gates with 352 pads. For larger designs, there are optimized arrays that achieve in excess of 3 million gates. However, it's also possible to use embedded arrays that include access to compact custom blocks ranging from programmable controller functions and fast microprocessor cores to memory and DSP elements.

The 200 series is optimized for power-sensitive applications, providing a gate delay of 135 ps for a two-input NAND gate with two loads and a power dissipation of 0.4 μW/Gate/MHz. The family is equipped with split supplies to enable the core logic to be operated at 2 V, reducing the power consumption, and 3 V on the I/O for linking with external 3-V systems. However, the 200 series also supports 5-V tolerant I/Os.

The manufacturer provides cell libraries optimized for synthesis and includes an extensive range of hard and soft macros. Cells include basic logic, oscillators and soft macros from the SystemBuilder library. In addition to compact custom blocks such as RAM and ROM, the 200 series also offers a range of high performance components including PLL and the ARM RISC core to enable system level integration. The 200 series is supported with design kits for several standard CAE systems. A VITAL-compliant library also is available. The design kits support the top down design flow with gate-level sign-off simulation offered by Mentor and Cadence. AV

GEC Plessey Semiconductors, *Cheney Manor, Swindon, Wiltshire, Great Britain, SN2 2QW; phone: +44-17 93/51 8128; fax: +44 17 93/51 84 81.* **CIRCLE 486**

16-Bit CAN Controller Features 64 Kbytes Of OTP Memory

The C164Ci microcontroller offers a 16-bit microprocessor with 64 kbytes of one-time-programmable (OTP) memory with 32-bit access and full CAN 2.0B active periphery on one chip. Additional peripheral modules that are monolithically integrated include a 16 bit 3/6 channel PWM (pulse width modulation) generator, timer, and capture-compare functions with incremental input. This combination makes it possible to use the C164Ci in various real-time applications (e. g., in safety and body control electronics in cars, or for drive control and uninterruptible power supplies in industrial applications).

Interrupt response times are 250 ns and computing power is 10 MIPS at 20 MHz. Furthermore, the device integrates a data memory of 2 kbytes. In the idle state, the device's current consumption is reduced to 1 mA even though the C164CI continues to perform its functions. The IC also features a 10 bit analog-to-digital converter plus a real-time clock that wakes up the chip from standby mode. In medium-sized quantities, the microcontroller costs about $10 (U.S.) per unit. In addition to starter kits, users also can employ specific OTP programming devices with samples as well as an emulator. AV

Siemens AG, *P.O. Box 80 17 09, 81617 Munich, Germany; fax +49 89 636 284 82.* **CIRCLE 487**

Multichannel Audio Decoder Family Targets MPEG-2

A new family of MPEG-2 multichannel audio decoders has been developed in response to the growing popularity of MPEG-2, particularly for DVD video players, set-top boxes, multimedia PCs, digital TV, and high-quality audio equipment. The first product to hit the scene will be the SAA2503 MPEG-2 multichannel audio decoder. It provides a downmix of the MPEG-2 audio datastream, enabling the information contained in the 5+1 or 7+1 MPEG-2 audio channels to be retained when listened to as a stereo output. The ability to decode the MPEG-1 audio layer ensures backwards compatibility with existing Video CDs. According to Philips, the additional audio channel information would be lost without the SAA2503, because only the MPEG-1 stereo audio layer would be heard. The additional information enables a quasi-surroundsound output to be achieved from just two speakers or straightforward stereo as require. A karaoke mode operation also is available.

The SAA2503 decodes MPEG-1 audio layer 2 at 44.1 kHz, MPEG-2 audio layer 2 at 48 kHz, and downsampling of linear PCM modes to 48 kHz. Input is via a bitstream I^2S interface, according toIEC 1937, while output is performed via an IEC958 interface. Control of this single-chip solution is maintained via the I^2C control bus . It can be used in standalone mode because it self-boots from the internal program ROM after power-up. No external DRAM or SRAM is required and a PLL for internal generation of 13.5- or 27-MHz clocks is integrated as well. Operating at 5 V and available in a 100-pin plastic TQFP package, the SAA2503 is priced at about $20 (U.S.) in volumes of more than 1000 pieces. AV

Philips Semiconductors, *International Fulfillment & Sales Support Center (SAA2503), P. O. Box 5066, 2900 EB Capelle a/d IJssel, The Netherlands.* **CIRCLE 488**

Edited by Roger Engelke

Verification Tool Boasts Pre-Synthesis Functional Verification Capabilities

Verification continues to be one of the most nagging problems facing today's designers. The traditional approach of test-vector generation just doesn't cut it anymore because it's almost impossible to generate all of the test vectors required to confidently verify a design. Assuming that you could, the amount of time it would take you to run them would be absurd. And design complexity and capacity only complicates the situation. Bell Labs, Murray Hill, N.J., recognized the need for a verification tool to work with large designs, by developing a tool called FormalCheck. Targeted at the mainstream, it enables designers to increase their design confidence without having to rely solely on simulation.

FormalCheck is the first formal verification tool in a planned family of system-level model checkers. It can conduct functional verification of large design—100K-200K gate level checking or 5000 state variables—whether they're whole chips, large functional blocks, or IP (Intellectual Property). It can verify such large designs because it employs a patented state space reduction algorithm. The tool simply evaluates the smallest subset of the overall design model where a desired behavior can be proven, and then uses this subset to scale up the proof.

Because this approach allows the tool to deal with a smaller problem space, verification of detailed properties on large designs can be conducted in shorter run times than previously possible. As a result, the designer is given the flexibility to attack larger, more complex system-level problems, and to potentially combine hardware and software components with embedded systems.

FormalCheck also employs patented algorithms for model checking and incremental verification. These enable the tool to perform pre-synthesis formal verification and to detect such problems as hidden deadlock and livelock states. One of the benefits of the tool is its ability to work with any design model in a synthesizable subset of both Verilog and VHDL. This ensures that the verified HDL model is synthesizable and allows FormalCheck to be used with other more conventional vector-based verification approaches.

The FormalCheck tool is built on five query templates. These provide everything the user will need to know to perform the verification. Each one consists of three parts: a fulfilling condition that's is the property to be verified; an enabling precondition which is the triggering condition that must be met before the fulfilling behavior is required; and a discharging condition which is the event that signals when the fulfilling condition is no longer needed. Using the templates as a guide, the queries can take the designer as little as a few minutes to write.

Once the queries are written, or the high-level behaviors of the system are specified, the tool sets out to verify the behaviors under all possible stimuli. All located bugs are reported back to the user in the form of an error trace.

One of the problems with traditional vector-based verification techniques is that even the smallest change to the structure of a design invalidates its associated simulation runs. With FormalCheck, though, system-level behaviors are verified in the form of queries that only need to be changed to the extent that expected behaviors change when the underlying logic structures of the design are modified. This fact is significant in terms of design reuse and IP, in which case most of the underlying design and the potential errors contained within the design, often times aren't known to the designer. An added benefit of the FormalCheck tool is its hierarchical approach and extensible architecture, which make it able to perform hardware/software (hardware/software) co-verification.

The FormalCheck verification tool is available now and runs on a SPARC/Solaris workstation. A single user floating license costs $150,000. This price includes the VHDL and Verilog front ends; a graphical user interface with source code viewer; basic query templates; all four formal verification algorithms (the early model, the large model, probabilistic, and autorestrict); and a waveform viewer with back references to source code.

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Series Upgrades Target Reuse Of Designs, Concepts

To assist designers in creating advanced ICs in a shorter period of time than previously possible, MicroSim has introduced a series of significant upgrades and add-on features to its current product offerings. Referred to as Release 8, this new functionality impacts all aspects of the design process.

Two key additions, Design Journal and Design Manager, are available for use with PSpice with Schematics, MicroSim PSpice A/D with Schematics, and MicroSim DesignLab. They are targeted at enabling reuse of designs and design concepts. Design Journal works by allowing engineers to mark checkpoints at different key crossroads in their designs, and then try alternative design directions. The results of these choices can be compared in graphical format, leaving the design engineer free to proceed with the best option. Design Manager acts as an organizer that automatically links together all files, even non-EDA related documents, associated with the design into a single, self-contained entity.

Other features offered in Release 8 are three new Orthogonal Rubberbanding capabilities. These include the Connectivity Watcher, which alerts users to potential connectivity problems, and a Pin-to-Pin Connector that automatically maintains connectivity when two pins are moved apart. Lastly, a Stair Stepping feature displays wires connected to a device in a stair-step arrangement.

Another capability being offered in *(continued on page 136)*

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New high-speed protocols are boosting growth of the pager market world-wide. Philips Semiconductors supports the latest FLEX protocol for high-speed paging, as well as the established POCSAG standard, and our receiver, decoder and controller ICs are backed up by LCD drivers and development support. Take our PCD5008H decoder/controller for FLEX which offers data transfers at up to 6400 bits/s, resulting in increased network capacity, shorter transmission times and fewer paging errors. Or the UAA2080/82, zero-IF two-level FSK receivers, fully POCSAG-compatible, which couple high sensitivity and dynamic range with low power consumption. Our proven POCSAG package also includes the PCD5003 decoder and development tools. No other manufacturer has a wider range of innovative wireless systems products, including discretes, for a wider range of applications. System solutions, silicon and software, are backed by our own systems labs to provide reference designs and support. Contact us for a copy of our new 'Wireless' brochure, or visit our web site. USA phone 1-800-447-1500, ext. 1387. Europe fax +31-40-272-4825, quoting 'WL'. Asia fax +852-2811-9173, quoting 'WL'. Web site: www.semiconductors.philips.com

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(continued from page 134)
Release 8 is a Symbols and Models function that replaces the task of manually creating symbols and linking them to appropriate models. This means that design engineers can automatically create symbols for any manufacturer's models in a manner of minutes.

Price range for Release 8 is from $895 to $14,850, depending on the particular platform and product configuration purchased. All of the Release 8 features can be found in the Design Lab tool. A free full-featured evaluation CD that includes all of the Release 8 capabilities is available by calling 1-800-245-3022. CA

***MicroSim Corp.**, 20 Fairbanks, Irvine, CA 92718; (714) 770-3022; Internet: http://www.microsim.com.*
CIRCLE 565

Tool Addresses Three Key Design-Process Areas

To help design engineers handle the growing complexity of pc-board design, the latest version of PowerPCB, version 2.0, is packed full of a number of advanced features and enhancements targeting three major areas of the design process. These areas are pc-board routing, Design For Test (DFT), and support of Microsoft OLE.

In the first area, improvements to the tool's Dynamic Route Editor allow designers to dynamically route multiple traces simultaneously. Other bus-routing features include options for various via patterns during layer stitching and partial completion. To address issues related to DFT, the tool now supports multiple/variant builds so designers can create pc-board technology variations using a single PowerPCB database. Other features in this area include both test-point status and probe side access pin attributes for testability, and an integration pathway to a suite of assembly, test, repair, and quality management software tools expected to be released by the end of the year. In addition, support for the RS-274-X standard simplifies bareboard manufacture.

In the last area, support for the OLE standard, design engineers can now link and embed OLE objects within PowerPCB design files. Support for the standard also means that PowerPCB can act as an OLE Automation Server allowing users to access the OLE interface using either Microsoft Visual Basic or Visual C++ to interact with core PowerPCB query functions.

PowerPCB 2.0 also offers a host of other significant new features. For example, new commands and data types have been added to the tool to allow support for split and mixed plane operations. PowerPCB's Decal Editor has been updated with PIN Wizard features for Polar and BGA/PGA pattern generation. And, PowerPCB's Graphic Editor offers support for radial placement operations, including grid definition and component arraying feature set. PowerPCB 2.0 costs anywhere from $2500 to $25,000 depending on the configuration purchased. CA

***PADS Software Inc.**, 165 Forest St., Marlborough MA, 01752; (800) 554-7253 or (508) 485 4300.* **CIRCLE 566**

HLD Methodology Gets Boost From Tool Suite

To promote widespread acceptance of high level design (HLD) methodology for field-programmable gate-array (FPGA) designers, a series of three tools will be introduced by Actel before year's end. These tools, developed to make the job of FPGA designers easier, will include the latest version of the company's design tool, Designer Series 3.1.1, an offering of HLD tool suites, and web-based design tools.

The first release in this series, Designer Series 3.1.1, has been upgraded to support devices that include the 1020RH RadHard FPGA in an 84 CQFP package and the 32100DX in 84 PLCC, 160, and 208 PQFP, and 176 TQFP packages. The tool supports nine packages for the 3200DX family and enables designers to use -F, -2 and -3 speed upgrades for many different devices. A 15% speed improvement has been demonstrated for the 32140DX, 32200DX, and 32300DX devices.

The Designer Series 3.1.1 also comes equipped with upgraded database-management software that makes installation and startup easy. In addition, the tool offers datapath macro generation software, known as the ACTgen Macro Builder, that allows datapath macros to be created and saved in seconds. In addition, Designer Series 3.1.1 features a DirectTime function to allow for timing-driven place and route and fully deterministic FPGA designs, and a PinEdit function that offers a drag and drop signal placement utility.

The HLD tool suites in this offering includes HLD tools from Viewlogic's ViewSynthesis FPGA synthesis, SpeedWave VHDL simulator, and Workview Office Schematic-based tools. The web-based tools, are intended to allow designers the ability to evaluate the company's software, determine the applicability of FPGAs for their design needs, familiarize themselves with FPGA HLD methodology, and to evaluate specific device offerings for designs currently in progress. The Designer Series 3.1.1 is available now on both PC and UNIX platforms.

For PCs, the tool will run on either a Windows 3.1, Windows for Workgroups, Windows NT 4.0, or Windows 95 operating system. On a UNIX platform, the tool runs on both the SunOS and Solaris operating systems and HP 9000 workstations running HP-UX operating systems. The tool is free to designers working on up to 8000 gate designs. After this limit, the tool comes bundled with Viewlogic's tools and can cost up to $5000. Call the company directly for pricing. CA

Actel Corp., 955 E. Arques Ave., Sunnyvale, CA 94086; 408 739-1010; http://www.actel.com. **CIRCLE 567**

Upgrade Boasts Improved Utilization And Timing

An upgrade to Altera's Verilog'x'press synthesis product promises to deliver a 30% increase in utilization and a 2X timing performance improvement without manual intervention. Basically, this up-

(continued on page 140)

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READER SERVICE 183

(continued from page 138)
grade, referred to as the PLSM-Verilog module generation capability, takes in Verilog net lists and synthesizes them into a gate-level representation. The Altera MAX+PLUS II development system then takes the Verilog'x'press output, performs low-level optimization, and subsequently places and routes the design for a targeted device. This feature can recognize commonly used logic structures such as adders, and generate modules that take advantage of the specialized architectural features of Altera devices tailored for these structures.

Thanks to the upgrade, the embedded array blocks of the company's FLEX 10K family of devices can be used to efficiently implement memory structures such as RAMs, ROMs, and FIFOs. In addition, the upgrade feature offers improved Verilog synthesis capability for the MAX+PLUS II development system. The PLSM-Verilog module generation capability for Verilog'x'press is available now as a migration product for the MAX+PLUS II development system. In North America, the price for the PC version is $3995. A version that runs on HP and Sun workstations sells for $5495. CA

Altera Corp., 2610 Orchard Pkwy., San Jose, CA., 95134-2020, 408 894-7000. **CIRCLE 568**

Multi-Faceted Synthesis Tool Offers Enhanced Performance For High-End Designs

To address some of the key design issues for the coming generation of microprocessor and structured-custom designs, Synopsys has come up with Synopsys 97. It incorporates synthesis technology aimed at high-performance designs, significant improvements to its Design Compiler product family, and 100 performance enhancements to over 20 of the company's design-automation products.

Synopsys 97 is developed specifically to provide designers with improved synthesis design performance that's significantly higher than was previously possible with the company's current synthesis tools. It also helps IC designers rapidly create high-end designs by providing a predictable synthesis flow for next-generation electronic products.

In particular, the tool targets the complexity, performance, and engineering productivity demands of a broad range of designs, from field-programmable logic devices to complex microprocessors and systems on a chip (SOC). As such, some of the benefits that can be achieved with the Synopsys 97 offering include improved support for rich cell libraries, 1-pass scan insertion, a 10 to 20% pushbutton power reduction, and reduced layout iterations.

One of the key features of Synopsys 97 is the release of Design Compiler featuring new gate-sizing algorithms for improved timing and advanced area op-
(continued on page 142)

(continued from page 140)

timization techniques targeted at cost-sensitive applications. In tests done on timing-critical designs using Design Compiler (achieved with a one-pass compile step), roughly 85% showed timing improvements of on average 23%. In addition, of the designs tested that were constrained by area, an average 18% witnessed an improvement in area.

Another significant feature of Synopsys 97 is a series of three-dimensional delay models implemented in the timing engine. These models make it possible to address the accuracy needs of 0.18-µm silicon technologies. This is particularly critical for designers of microprocessors and high-performance, high-speed designs that often rely on the most advanced silicon technologies to get the speed and performance they need. In the past, designers typically had to handcraft designs to get the required performance. However, with these models in place, along with newly developed gate optimization and timing-prediction technology offered in the Design Compiler tool, designers now have an automated solution. In addition, more comprehensive timing checks were incorporated to ensure that specialized cells perform correctly in the resulting circuit.

Another interesting feature of Synopsys 97 are two algorithms that were integrated in the company's Behavioral Compiler tool. Known as the behavioral optimization of arithmetic and behavioral retiming algorithms, they're able to deliver increased performance and reduced area. In fact, use of these algorithms has created a roughly 15% improvement in quality of results for behavioral and RTL datapath intensive designs. Also included in the Synopsys 97 offering is a new tool known as the ECO Compiler. This tool automatically synthesizes engineering change orders (ECOs) into designs that have already been fully synthesized, placed, and routed. With traditional techniques it can take designers weeks to implement ECOs.

By comparison, the ECO Compiler tool, which works hand in hand with Design Compiler, can handle late stage functional design changes in one day by reusing all of the previous versions of a design. It then can leverage all previous work done in synthesis, as well as place and route, allowing designers to reuse most of their earlier implementation. As a result, changes to the existing net list and layout are minimized. ECO Compiler also can implement changes to a synthesized net list before layout, preserving the investment in optimization of critical paths.

Synopsys 97 is shipping now. Its cost depends on the configuration and the maintenance contract purchased. Contact the company directly for cost inquiries. The ECO compiler is available as an option to Design Compiler and sells in the U.S. for $100,000.

Synopsys Inc.
700 East Middlefield Rd.
Mountain View, CA 94043
(415) 962-5000
http://www.synopsys.com/synopsys_97
CIRCLE 569
CHERYL AJLUNI

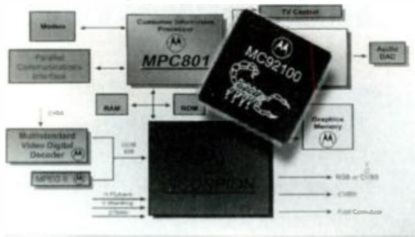
Video-Encoder Chip Adds Digital Graphics To Television-Based Systems

Dubbed the Scorpion chip, the MC92100 graphics and digital video-encoder circuit provides flexible, television-based graphics overlay and mixing capabilities. That allows designers to incorporate interactive features such as Internet browsing, electronic program guides, and other digital information into both new and existing TV-based systems (intelligent TVs, DVD playback systems, and so on).

With the chip, systems can display multiple windows that contain interactive graphics right over traditional video streams on the television screen. As a result, users can watch television and browse the Internet and other information sources at the same time. The graphics capability of the Scorpion matches the resolution and color depth of standard NTSC/PAL baseband video, thus delivering the highest resolution available with existing TV technology.

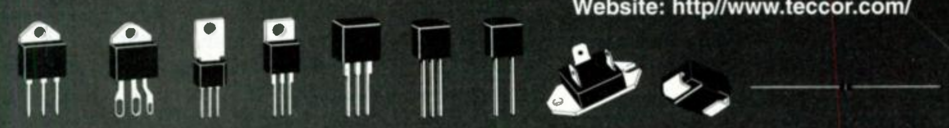
The chip incorporates a selectable square pixel filter. It ensures both computer-based and television-specific graphics are displayed accurately in their intended aspect ratios. An adaptive de-flicker filter checks graphics pixel by pixel to ensure a flicker-free (and thus easier to read) display. Outputs from the video encoder support RGB, composite video, and S-video in both the PAL and NTSC formats. A closed-caption insertion capability as well as Macrovision copyguard capabilities (based on the version 7 standard) are included. A second version of the chip, the MC92101, doesn't include the Macrovision standard.

Intelligent TV Block Diagram



Inputs to the chip include a standard ITU-R-656 input for MPEG2, DVD, and other digital video sources. A wide range of video input formats are supported—YCrCb (4:2:2), RGB16 (565 and 555), as well as 2/4/8-bit color lookup tables. All formats allow alpha mixing and transparency on a pixel or window basis. The circuit also includes a glueless interface to an external processor (PowerPC or ColdFire) as well as a direct interface to an external synchronous DRAM. The closely coupled interfaces gives the chip the bandwidth it needs to support multiple planes of high-quality graphics along with background video and a hardware cursor.

A reference/development system helps designers create prototypes. *(continued on page 146)*



Been paying too much for your CPLDs?

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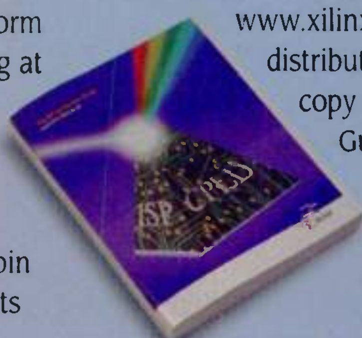
That's why we introduced our new XC9500 ISP CPLD for well under $1.50*. Now you can reduce system costs and design with the industry's most advanced CPLD architecture. In fact, the XC9500 is rapidly becoming the standard for in-system reprogrammability by allowing designers to easily perform unlimited iterations and in-system debugging at the prototyping phase. Plus it offers the added advantage of programming and testing during manufacturing.

Available in densities from 36 to 288 macrocells, the XC9500 features 5ns pin-to-pin speeds and exceeds IEEE 1149.1 requirements for JTAG. Couple this with our "no-risk" pin-locking feature and 10,000 program/erase cycles, and there you have it. The world's most versatile CPLD at a price that's unbeatable.

So, if you want to stay a leg up on the competition, while dramatically cutting costs on your next design, visit our website at www.xilinx.com. Or, give your local distributor a call and ask for a copy of our ISP Application Guide/CPLD Data Book and pricing information. They'll gladly give you a hand.



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(continued from page 144)
The system employs the PowerPC 8xx embedded processor family, which is supported by a number of embedded operating systems, including Microware's OS-9, Wind River's VX Works, ISI's pSOS, and Microsoft's WinCE. Samples of the MC92100 are available immediately. In lots of 50,000 units, the chip sells for less than $20 each when housed in a 208-lead PQFP.

Motorola Inc.
Semiconductor Products Sector
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MD56-102
Phoenix, AZ 85072
Mike Watson, (317) 571-7017
http://www.mot.com/adc
CIRCLE 570
DAVE BURSKY

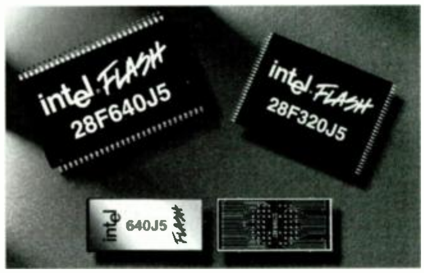
64-Mbit Flash Memories Double The Density Of Previous-Generation Chips

After announcing its two-bit-per-cell storage technology over a year ago, Intel has finally released to production a pair of StrataFlash memory chips that offer double the densities of previously-available chips—32 and 64 Mbits, respectively. Fabricated with 0.4-µm design rules, the 28F320J5 32-Mbit chip achieves the double density in a smaller chip area than the company's 16-Mbit device; the 28F640J5 64-Mbit memory, on the other hand, requires more chip area than what's occupied by the 16-Mbit memory (the 16-Mbit devices are fabricated with 0.6-µm design rules).

Read access times for the 32- and 64-Mbit chips are 120 and 150 ns, respectively, while erase/write cycle time averages 6 µs, based on a 32-byte page register write to the memory array. The I/O data bus is configurable as either 8 or 16 bits wide and can interface to logic with 2.7- to 3.6-V signal levels.

Another significant improvement is the addition of more chip enable lines (three all together), which permit multiple-chip arrays (up to four chips) to be assembled without any external logic, thus simplifying system designs. Moreover, the memories are FlashFile software-compatible and only minor changes are required to migrate from the existing byte-wide 28F016SA/SV, 28F032SA, and word-wide 28F160S5 and 28F320S5.

The Vpp pin has become a control pin, which when held low, provides a hardware write-protect line to prevent accidental writes to the memory array. Furthermore, the use of the common flash interface (CFI) to provide the ROM signature identifier string, and the scalable command set (SCS), designers can plan for future density upgrades and take advantage of the optimized write capabilities of the StrataFlash devices. The memories also are compatible with the TrueFFS flash translation layer developed by M-Systems, which allows StrataFlash-based memory arrays to emulate a hard-disk drive.



The StrataFlash memories operate from a single 5-V supply (both read and store) and are housed in standard 56-lead SSOP, TSOP, and the new microball-grid-array package. In lots of 10,000 units, the 32-Mbit StrataFlash memory sells for $15.40 each, while the 64-Mbit chip goes for $29.90 each in similar quantities. Prices for the space-saving microBGA package are about 10% higher. Samples are available from stock.

Intel Corp.
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Santa Clara, CA 95052-8119
(800) 548-4725
http://www.intel.com
CIRCLE 571
DAVE BURSKY

Low-Noise Fractional PLLs Boost System Performance

The PE3282A phase-locked loop (PLL) is an RF IC intended for satellite, cellular, and other wireless applications in which noise margins and performance are critical. Employing a fractional digital architecture, the PLL is fabricated using an innovative silicon-on-insulator

process to deliver superior noise characteristics and phase stability at low cost. The PE3282A can operate at frequencies up to 1.1 GHz with a demonstrated phase noise of less than –78 dBc/Hz and an integrated phase noise of 0.9° RMS and fractional spurs of –68 dBc or better. With a typical current consumption of 9 mA, the PLL can operate at voltages ranging from 2.7 to 3.6 V. It's supplied in a 20-pin TSSOP with a standard pinout. An evaluation kit contains an assembled synthesizer board and easy-to-use test software. Available during the fourth quarter of 1997, the PE3282A will cost $2.50 each in quantities of 100,000. The evaluation kit costs $399. LG

***Perigrine Semiconductor Corp.**, 6175 Nancy Ridge Dr., San Diego, CA 92121; (619) 455-0660; fax (619) 455-0770; http://www.peregrine.com.*
CIRCLE 572

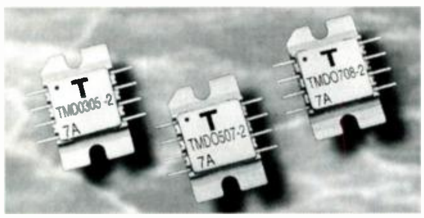
Compact, Low-Cost VCOs For Satellite Applications

The V807ME01 is a VCO intended for PLLs and other satellite applications in which spectral purity and stability are at a premium. It generates 2400 to 2800 MHz within a control range of 1 to 11 V dc while delivering an output power level of 8.5 dBm into a 50-Ω load. The VCO exhibits a typical spectral purity figure of –92 dBc/Hz at 10 kHz from the carrier. Second-order harmonics are attenuated at better than -10 dBc and its linearity is 1.1:1 over its temperature range of –40 to +75°C. Housed in a Mini SMT package, the V807ME01 is available now for $15.95 each. Substantial discounts are available for production-level orders. LG

***Z-Communications Inc.**, 9939 Via Pasar, San Diego, CA 92126; (619) 621-2700; fax (619) 621-2722.*
CIRCLE 573

New Power MMICs Cover Entire C-Band

The TMD0305-2, TMD0507-2, and TMD0708-2 are a family of C-Band MMICs designed for all stages of C-band amplifiers. The TMD0305-2 operates in the 3.7- to 5.1-GHz band; the TMD0507-2 operates in the 5.1- to 7.2-GHz band; and the TMD0708-2 is designed for operation in the 7.1- to 8.5-GHz band. All three components have a P1dB of 33 dBm and



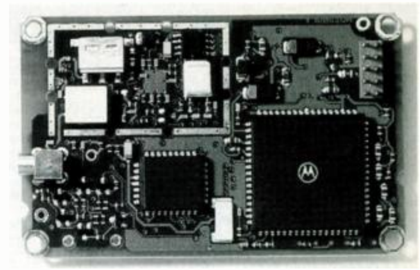
a G1dB of 22 dB. Their integrated architectures and uniform pinout yield cost savings over discrete designs by reducing component count. Available now, all three components are priced at $124 in 100-piece quantities. LG

***Toshiba America**, Electronic Components Inc., 9775 Toledo Way, Irvine, CA 92618-1811; (800) 879-4963; http://www.toshiba.com/taec.*
CIRCLE 574

GPS Modules Feature Fast Lock, Differential Mode

The GT Plus Oncore GPS receiver is a compact, fully functional navigation unit intended for automotive, handheld, marine, and industrial applications. Capable of tracking up to eight satellites at once, it also features differential location capability, which can provide meter-level position resolution. Improved signal processing allows the GT Plus to acquire a "warm start" position fix within 15 seconds, and accomplish a "cold start" in 90 seconds. The unit can reacquire a lost signal in under one second, permitting better operation in urban areas, or locations with dense foliage.

The compact 2.5-by-3.25-by-0.5 in. module has a standard RTCM interface for its differential input data and a NMEA-standard positional data output port. Additional features include a velocity filter with user-selectable time constant, an altitude-hold function, and an 80-mA power feed for applications employing active antennas.

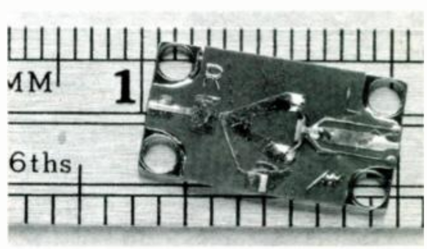


Available now, pricing is available upon request. LG

***Motorola Inc.**, Position and Navigation Systems, 4000 Commercial Ave. Northbrook, IL 60062-1840; (888) 298-5217; (874) 714-7328; fax (874) 714-7324; or on the Internet at: http://www.oncore.motorola.com.*
CIRCLE 575

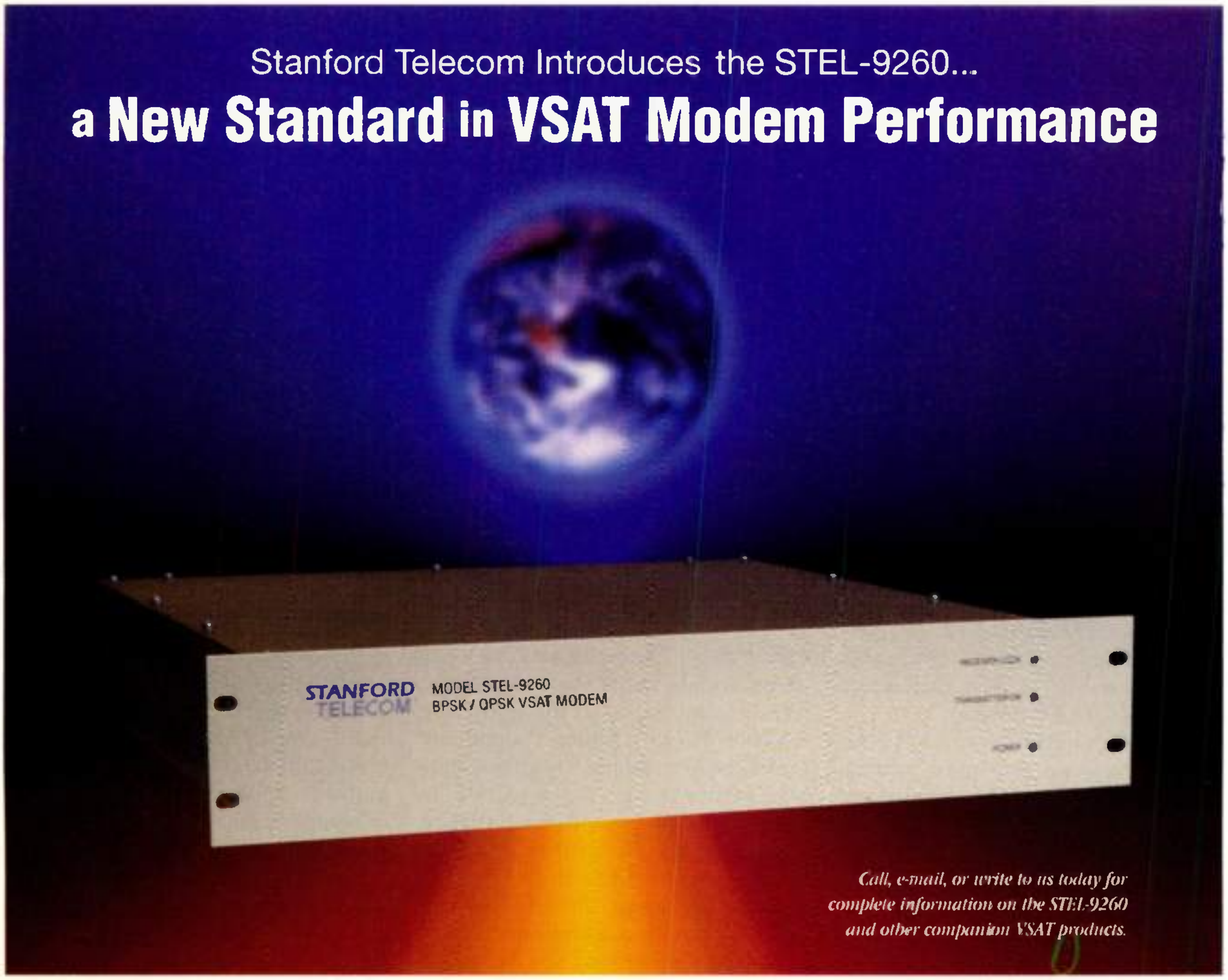
VSAT Converter Mixers Cover Satcom Bands

The MC5xMS family of microstrip carrier mixers offers nearly complete coverage of the satcom communications spectrum. They all operate over the entire 3.5- to 15-GHz range, providing coverage of the S, X, and Ku bands. This allows designers to specify a single mixer for multiple applications, or to produce a "tri-band" product. The mixers feature



very flat conversion loss, typically around 5 dB. Four local oscillator drive levels are available at +7 (MC53MS-7), +10 (MC54MS-7), +13 (MC56MS-7), and +17 dBm (MC57MS-7). Isolation for the LO ports is normally 35 dB, and isolation from LO to IF is typically 38 dB.

Measuring only 0.6-by-0.32-by0.115 inches, the microstrip carrier has a compact form factor that makes it easy to integrate with other microwave compo-
(continued on page 150)



Our new STEL-9260 is a complete VSAT modem in a rack mounted configuration. It is an ideal choice for systems where it is important to incorporate modulator and demodulator functions in a single package. And thanks to Stanford Telecom's advanced engineering techniques, we are able to offer this top performance at extremely low cost.

This complete modem assembly has independent transmit and receive functions - both with programmable bit rates in 1 bps increments. Receive FIR coefficients are programmable to allow the modem to be optimized to both closed and open systems. Significant STEL-9260 features include:

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- Programmable receiver FIR filter allows modem to match system requirements
- Selectable for 110 or 220 VAC at 50 or 60 Hz

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READER SERVICE 184

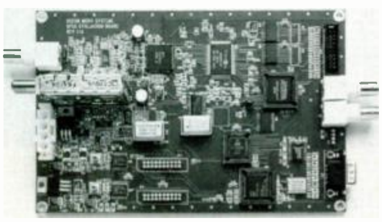
(continued from page 148)
nents. A surface mount version of this product also is available, with the part designator MC5xSMT-7. Pricing is under $100 each in small quantities. LG

Magnum Microwave Corp., 1990 Concourse Dr., San Jose, CA 95131; (408) 42-9898, fax (408) 432-1551; sales@magmicro.com. **CIRCLE 576**

Satellite Decoder Targets Set-Top Boxes

The ODM8511P is a variable-rate QPSK demodulator intended for digital set-top boxes, satellite head ends, VSAT terminals, and PCS base stations. It implements a unique architecture that enables it use a fixed-frequency clock to decode a wide range of symbol rates from 1 to 45 Msymbols/s. The chip includes a QPSK decoder, a multi-rate Viterbi decoder (1/2, 2/3, 3/4, 5/6, and 7/8), a de-interleaver, and Reed-Solomon FEC circuitry.

By coupling a complex multiply function to a polyphase filter, the demodulator can tolerate significant amounts of

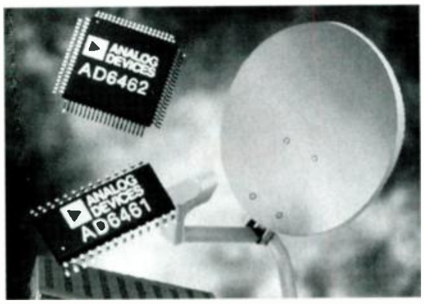


carrier error drift without requiring feedback to the tuner. Overall insertion loss is less than 0.5 dB. Communications with the host system can be accomplished via either a high-speed serial interface or an eight-bit parallel bus. A demonstration board, the ODM8511P, can be purchased to enable designers to evaluate the decoder's performance. Housed in a 100-pin PQFP, the ODM8511P is available now. Pricing is $17.50 each in quantities of 50,000. LG

Odeum Microsystems Inc., 3103 North First St., San Jose, Calif., 95314; attn: Perry Mistry (408) 232-8412; fax (408) 232-8131. **CIRCLE 577**

DBS Receiver Chip Set Supports Multi-Rates

The SATCOM2 chip set combines all of the necessary mixed-signal functions needed to process digital audio/video signals from DBS satellites. Comprised of two chips, the receiver demodulates QPSK signals ranging from 10 to 85 Mbits/s. It integrates a complete receiver front end, including demodulator, baseband filter, ADC, and digital receiver. Input is a standard 480-MHz IF frequency QPSK signal. Output is a standard



MPEG-2 transport data stream. On-chip analog-domain circuitry is used to accommodate the multiple data rates, eliminating the need for switching SAW or discrete filters. Component costs and board-space requirements are further reduced by a pair of on-chip, adjustable bandwidth filters. They optimize bit error rate and reduce noise and distortion. Priced at less than $18 each, the SATCOM receiver chip set is available now. LG

Analog Devices Inc., Ray Stata Technology Center, 804 Woburn St., Wilmington, MA 01887; (617) 937-1428, fax (617) 821-4273. **CIRCLE 578**

One-Chip DBS Receiver Features Multiple Rates

The CQT6010 DBS-XL is a single-chip QPSK demodulator/FEC decoder designed for set-top boxes and other consumer satellite applications in which performance and cost are critical. This highly integrated receiver also incorporates both Reed-Solomon and Viterbi decoding, energy dispersal functions, a pair of six-bit analog-to-digital converters, and an on-chip PLL. Also included is a proprietary variable rate filter that performs both spectral wave shaping and symbol timing synchronization functions.

This variable filter allows the CQT6020 to support any symbol rate from 1 to 45 Mbaud, and an output data rate of 1 to 112.5 Mbits/s. This enables it to support a variety of satellite services, including DVB-S and DSS television, satellite data, and multi-channel audio. The receiver performs carrier recovery digitally, eliminating the need for most analog tuning components. It offers both a three-wire serial and eight-wire parallel host-system interface for easy integration with most microprocessors. Sampling now, the CQT6020 is priced at $10 each in quantities of 100,000. LG

ComQuest Technologies Inc., 357 Encinitas Blvd., Encinitas, CA 92024-3740; (760) 633-1618, fax (760) 633-1677. **CIRCLE 579**

Planar Antennas Shine In DBS, MMDS Applications

The Galaxis family of planar antennas employ advanced multi-element stripline technology and an integrated downconverter. By using a lithographically produced array of resonant elements, these compact, rugged antennas can deliver high performance at prices rivaling conventional dish antennas in satellite receivers, direct-broadcast-satellite (DBS) systems, MMDS, and other applications. Their wide field of reception widens installation alignment tolerances and improves performance in difficult mobile applications.

One of the first commercial applications is the Future 1 series of antennas, intended for use in DBS television products. Operating in the 12.2- to 12.75-GHz band, the American version can receive signals from various services, including DirecTV, Echostar, and Primestar. It boasts a gain of 55 dB and a 0.8-dB noise figure. Bandwidths of up to 2 GHz can be easily obtained for other applications. Versions for foreign applications also are available.

For mobile applications, there's the Space Scanner, an inexpensive 2-axis positioning system. The compact, fully sealed, sea-water-proof positioner weighs less than 15 lbs. and can be used to orient satellite antennas on a variety of mobile platforms. Complete with a remote control head, the Space Scanner runs either on 10 to 16 V dc, or 120 V ac.

Available now, the Marine version of the Future 1 antenna costs $75 in OEM quantities. The Space Scanner two-axis positioner costs $900 in OEM quantities. Pricing for other configurations is available upon request. LG

Galaxis USA Ltd., 30 Nassau St., 4th Floor, Princeton, NJ 08542; (609) 924-1001; fax (609) 924-4442. **CIRCLE 580**

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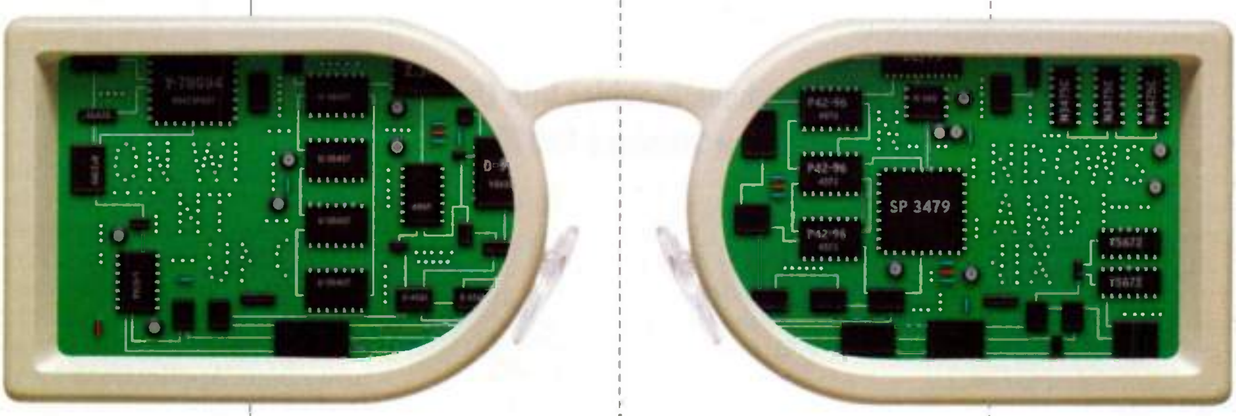

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Multilingual Brochure Talks About Global Sensors

A multilingual brochure from Honeywell's Micro Switch Div., Freeport, Ill., presents the company's 990 Series inductive proximity sensor family. The brochure, which is produced in seven languages, includes technical data on the cost-effective sensors that offer global availability. Honeywell's 990 Series includes a three-wire dc part in 8-, 12-, 18- and 30-mm standard sizes. The English version of the brochure is available on the company's Web site at *http://www.sensing.honeywell.com* in HTML format. The French, German, Italian, Portuguese, and Spanish versions are available in PDF format. For a free copy of the English version, you also can fax at (815) 235-5988. Contact Honeywell's Micro Switch Division at (800) 537-6945, or e-mail them *info@micro.honeywell.com*. LM

CIRCLE 543

Shielding Products Exposed In A 20-Page Color Catalog

AMP Inc., Harrisburg, Pa., presents its line of shielding products in a new 20-page color catalog. The Quietshield family of products minimize the ability of electromagnetic signals to leave or enter an enclosure. Products include profile and I/O gaskets, bent panels, tapes, and custom laminates. In addition to product descriptions and application details, the catalog also includes engineering profiles, specifications, and dimensions. An introductory section explains shielding theory and design challenges. For more information, call (800) 522-6752, or visit AMP online at *http://www.amp.com*. LM

CIRCLE 544

Brochure Explains Both The Company And Its Connectors

A four-page brochure from Advance Rendar Ltd., Solon, Ohio, describes both the company and the wide variety of components that it manufactures. Advance Rendar makes single- and multi-output power connectors typically used in computers, instrumentation, power supplies, and telecom applications. For example, the Quadbloc Plus One is a multi-output power connector that distributes power to four loads from a single source. The company also offers commercial connectors and audio connection devices. For more information, call (216) 349-0755 or fax at (216) 349-0142. LM

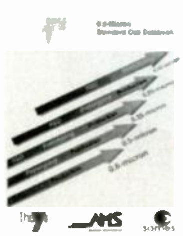
CIRCLE 545

Capacitor/Thermistor Catalog Has Products And Applications

Both product specifications and applications are covered in a new 36-page catalog from Cera-Mite Corp., Grafton, Wis. The publication includes information on the company's extensive line of ceramic disk capacitors and ceramic PTC thermistors. High-voltage mica technology and other specialty high-voltage products are featured in the capacitor section. The thermistor section combines an overview of PTCR technology and applications with information on HVAC motor-start packages and overcurrent protection products. For a copy of the catalog, contact Cera-Mite at (414) 377-3500. You can also fax (414) 377-7309 or e-mail *sales@ceramite.com*. The company's Internet address is *http://www.ceramite.com*. LM

CIRCLE 546

Databook Provides Info On 0.6-µm Standard-Cell ICs



A 760-page databook from Austria Mikro Systeme contains detailed information on the 0.6-µm standard-cell family from AMS and Thesys. The standard cells, which are built in a double-layer-metal CMOS process technology, boast low power consumption, high speed, and noise immunity. The databook includes logic; timing and power-consumption information; cell area; and a brief description of the standard cells. There's also process-derating data and an explanation on interpreting this data. Contact AMS at +43 (03136) 500 for a free copy of the databook. The phone number for their Cupertino, Calif.-based office is (408) 865-1217, and the company's e-mail address is *info@ams.co.at*. In addition, you can download the databook text at *http://www.ams.co.at*. LM

CIRCLE 547

Learn To Invade An Engineer's Personal Cyberspace

Marketing on the Internet: A Guide to Reaching Scientists and Engineers Online is available for free from Cirrus Technology, a high-tech marketing organization located in Worcester, Mass. The report details the psychological aspects of why scientists and engineers use the Internet, and how to best reach them in order to sell products or services. It starts with a perspective on electronic commerce, and then analyzes the psychology behind basic information retention. Finally, the report concludes with information on creating the perfect web site. To get your free copy of the report, call (508) 755-5242, or fill out the request form at *http://www.CirrusMarketing.com*. LM

CIRCLE 548

Check Out Fans And Blowers In A 20-Page Product Guide

Find out about ac and dc fans and blowers in a 20-page color product guide from Comair Rotron, San Ysidro, Calif. The guide provides a quick reference page, specifications for each product, and an overview of the company's design, development, and production capabilities. Product information includes CFM, size and weight, nominal V dc, watts, RPM, bearing type, and operating temperature range. Applications for these products include medical, computer, and automotive equipment. The products are available in standard, modified, or custom versions. For a free copy of the guide, call (619) 661-6688 or e-mail: *sales@comairrotron.com. The company's* Web site is located at *http://www.comairrotron.com*. LM

CIRCLE 549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Keeping It Simple

I just read about engineers being people in the July 17 issue *("Engineers Are People Too," p. 128)*. What is different about design engineers is that they have only one form of competition in their workplace. That competition is to better the product of other engineers. This leads to designs that are smaller, faster, more complex, and more...more...more... in every way except simple.

This leads to over-complicated equipment that only children can use ("So simple, a child can use it."). My daughter taught me to use e-mail, and I still ask her to program the video recorder. Equipment that is so compact (small) that it is easily lost or stolen. My word processor mangles (sorry, *processes*) several thousand words in the time it takes my finger to find the next key to push, and the battery's shelf life is shorter than the operating time.

So, design engineers do steer the world. The marketing people ask for a slightly better product and the engineers add lots of brilliant new features, most of which the accountants remove on cost grounds. (They then put them back in the next version.)

I am one of the few oddballs who do just what is asked for; no more, no less. I've given up the race to outdo others.

I run my own company, and it is slowly beginning to get off the ground; I may even take a salary next year! But I am happy; no more rat race. And the products I make can be understood and used without the need to bring children in as technical advisors.

Bernard Green
SYEMON Electronic Solutions
(Simple Yet Effective Methods Operate Nicely)

Point, Counterpoint

I'm writing in response to "Debate Brews On The Warnings Of A Future Shortage Of Software Programmers And Professionals" *(June 23, p. 167)*.

The article refers to a study by the Computer Industry Project of Stanford University (CIPSU), which mentions a "global shortage of computer programmers and software professionals." The article acknowledges that the study's findings are debatable, but then continues under the unstated assumption that they are worth discussing seriously.

The American Engineering Association (AEA) does not accept these findings, nor those of the Information Technology Association of America (ITAA), which reaches similar conclusions. The AEA, an organization dedicated to enhancing the career climate for practicing technical professionals, finds such "shortage shouting" to be nothing but self-serving announcements.

History has proven these reports are seldom accurate and often have no basis in fact. These reports or studies are often quoted in trade journals and the public press to justify a need to import foreign engineers and scientists.

The study by the ITAA, a trade association of employers of software workers, has the same flaws as the CIPSU study. Their statement of massive information technology job vacancies and present and future shortages is not supported by any data from the U.S. Department of Labor's (DOL) statistics. The data does show huge increases in the supply to meet the industry expansion requirements. A shortage of 10% may be met with only four hours of overtime per week.

If there were a shortage of programmers, computer scientists, and systems analysts, there would be a significant increase in median wages. The DOL's data does not show any evidence of that for 1996 over 1995. Computer programmers were on average receiving an increase in pay of only $25 per week per year and reaching a level of approximately $775 per week in 1996.

AEA President Billy E. Reed said, "These reports always have two things in common; they're never very accurate, and the projected shortage never appears."

Robert N. Bruce
r.n.bruce@ieee.org

Spell-Czeching Down Under

I was taken with your May 12 editorial *("Technology's Weak Link," p. 18)*. It takes months for your publication to reach Australia, but I wanted to comment on it anyway.

I find that spelling, reading, and writing proficiency is not taken for granted; it no longer is insisted upon. Many people live in a strange dreamland where spell- and grammar-checkers in the latest word-processing packages will take care of everything. I am multilingual myself; English is not my first language. My mother tongue is Czech—a curious language which, at the same time, is quite simple—it is almost 100% phoentical, i.e., you read exactly as you write and, in most cases, every letter is pronounced invariably the same way. However, it also is very difficult—Czech grammar would be a nightmare to most English-speaking persons, and is often difficult for the Czechs themselves.

For this reason, I had to learn English twice—first, the written form, then the spoken form. Because of this, I certainly can appreciate the importance of being able to spell correctly. Recently, I tried an experiment: I wrote an article were I purposely used incorrect and similar-looking words like "brought" and "bought," "ant" instead of "and," "capriciously" instead of "capillary," and so on. The editor glanced through it, ran the spell- and grammar-checkers, and gave it back to me without a single query! The only mistake she picked up was the double "the." I was astonished; I then asked her if she actually read the piece. She said, "Oh yes, but you foreigners write such 'correct' English that I had no doubt that it was OK!"

It seems you have the same problems with basic education in the U.S. as we do in Australia. Indeed, the future does not look very bright.

Millan Y. Xeno
via e-mail

PAL Is Friendly To DVDs

In "We've Seen The Future And It Lies In DVD" *(Aug. 18, p. 52)*, there is a curious inference that the chosen DVD audio data compression algorithm is MPEG-2. PAL DVD's in Europe are meant to carry MPEG-1 or MPEG-2 (BC) audio. PAL disks also can carry AC-3 for multichannel and so far, most, if not all, do. There is no standard that NTSC disks have to carry MPEG-2 audio.

Robin Bransbury
rb@dolby.com

Letters to the Editor, including the writer's name, address, and daytime phone number, should be sent to: Letters Editor, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604; fax (201) 393-0204; e-mail: mikemea@class.org. Letters may be edited for space and clarity. Names will be withheld upon request.

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Digital Design and Verification Engineer

Qualified candidate will be responsible for 50% design (full custom CMOS logic and circuit) and 50% verification (generating and maintaining test suite in Assembly language). Must have a minimum of a MSEE with 2+ years experience or a BSEE with 4+ years of experience. Background in computer architecture and CMOS circuit design using SPICE is required. Must also have working experience with VERILOG (preferred) or VHDL. **Job Code: BLED-971**

Product Engineer

Qualified candidate must have 5+ years experience and familiarity with CMOS processing techniques and testing methodology. Must also have hands-on experience in silicon debug to include micro-probing, wafer deprocessing, understanding of schematics and datasheet parameters and characterization of devices across all datasheet parameters and end-use systems. Experience with design of hardware and software of small microcontroller-based systems is required. CMOS mixed signal or digital experience preferred. Background working on microcontroller-based devices with analog I/O a plus. **Job Code: ESED-972**

Applications Engineer

Selected candidate will be responsible for providing technical marketing support for the development and implementation of customer applications dealing with complex operating systems. Will assist sales staff in assessing potential application of company products to meet customer needs and prepare detailed product specifications. A BSEE, minimum of 7 years experience and background with power conversion and low-power analog circuits required. **Job Code: DFED-10972**

Firmware Engineer

Successful candidate will be responsible for the analysis, design, programming, debugging and modification of software and will troubleshoot code for firmware (IC embedded code) applications. Work often involves analog and digital hardware and software operating systems. Must have a minimum of 5 years experience, knowledge of hardware design, as well as the ability to program in machine, assembly and high-level languages, such as C and C++. Experience programming portable electronic applications and battery-powered microcontrollers is preferred. **Job Code: DFED-10971**

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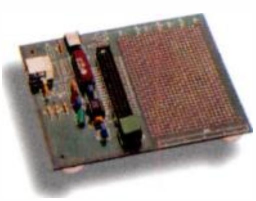

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